

BELL
INDUSTRIES
ELECTRONICS
DISTRIBUTION
DIVISION

1161 N. FAIROAKS AVE.
SUNNYVALE, CA 94088
TEL 408-734-8570
FAX 408-734-8875

F100K ECL Logic Databook and Design Guide

Includes new
300 Series Datasheets





A Corporate Dedication to Quality and Reliability

National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

We are proud of our success . . . it sets a standard for others to achieve. Yet, our quest for perfection is ongoing so that you, our customer, can continue to rely on National Semiconductor Corporation to produce high quality products for your design systems.

A handwritten signature in black ink, reading "Charles E. Sporck". The signature is fluid and cursive, with a large, prominent initial "C".

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

Wir fühlen uns zu Qualität und Zuverlässigkeit verpflichtet

National Semiconductor Corporation ist führend bei der Herstellung von integrierten Schaltungen hoher Qualität und hoher Zuverlässigkeit. National Semiconductor war schon immer Vorreiter, wenn es galt, die Zahl von IC Ausfällen zu verringern und die Lebensdauern von Produkten zu verbessern. Vom Rohmaterial über Entwurf und Herstellung bis zur Auslieferung, die Qualität und die Zuverlässigkeit der Produkte von National Semiconductor sind unübertroffen.

Wir sind stolz auf unseren Erfolg, der Standards setzt, die für andere erstrebenswert sind. Auch ihre Ansprüche steigen ständig. Sie als unser Kunde können sich auch weiterhin auf National Semiconductor verlassen.

La Qualité et La Fiabilité:

Une Vocation Commune Chez National Semiconductor Corporation

National Semiconductor Corporation est un des leaders industriels qui fabrique des circuits intégrés d'une très grande qualité et d'une fiabilité exceptionnelle. National a été le premier à vouloir faire chuter le nombre de circuits intégrés défectueux et a augmenter la durée de vie des produits. Depuis les matières premières, en passant par la conception du produit sa fabrication et son expédition, partout la qualité et la fiabilité chez National sont sans équivalents.

Nous sommes fiers de notre succès et le standard ainsi défini devrait devenir l'objectif à atteindre par les autres sociétés. Et nous continuons à vouloir faire progresser notre recherche de la perfection; il en résulte que vous, qui êtes notre client, pouvez toujours faire confiance à National Semiconductor Corporation, en produisant des systèmes d'une très grande qualité standard.

Un Impegno Societario di Qualità e Affidabilità

National Semiconductor Corporation è un'industria al vertice nella costruzione di circuiti integrati di alta qualità ed affidabilità. National è stata il principale promotore per l'abbattimento della difettosità dei circuiti integrati e per l'allungamento della vita dei prodotti. Dal materiale grezzo attraverso tutte le fasi di progettazione, costruzione e spedizione, la qualità e affidabilità National non è seconda a nessuno.

Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.



Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

F100K ECL DATABOOK

1990 Edition

Family Overview

F100K 300 Series Datasheets

F100K 100 Series Datasheets

11C Datasheets

ECL BiCMOS SRAMs

ECL PALs and ASICs

**F100K ECL Design Guide
and Application Notes**

**Ordering Information and
Physical Dimensions**

1

2

3

4

5

6

7

8

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

| | | | |
|----------------------------|--------------------|-------------------------------|----------------------|
| Abuseable™ | E-Z-LINK™ | MICROWIRE/PLUS™ | SCX™ |
| Anadig™ | FACT™ | MOLE™ | SERIES/800™ |
| ANS-R-TRAN™ | FACT Quiet Series™ | MPA™ | Series 900™ |
| APPST™ | FAIRCAD™ | MST™ | Series 3000™ |
| ASPECT™ | Fairtech™ | Naked-8™ | Series 32000® |
| Auto-Chem Deflasher™ | FAST® | National® | Shelf✓Chek™ |
| BCP™ | 5-Star Service™ | National Semiconductor® | Simple Switcher™ |
| BI-FET™ | Flash™ | National Semiconductor Corp.® | SofChek™ |
| BI-FET IITM | GENIX™ | NAX 800™ | SONIC™ |
| BI-LINE™ | GNX™ | Nitride Plus™ | SPIRE™ |
| BIPLANT™ | GTO™ | Nitride Plus Oxide™ | Staggered Refresh™ |
| BLCT™ | HAMR™ | NML™ | START™ |
| BLX™ | HandiScan™ | NOBUST™ | Starlink™ |
| BMACT™ | HEX 3000™ | NSC800™ | STARPLEX™ |
| Brite-Lite™ | HPCT™ | NSCISE™ | Super-Block™ |
| BSIT™ | I ³ L® | NSX-16™ | SuperChip™ |
| BTL™ | ICMT™ | NS-XC-16™ | SuperScript™ |
| CDD™ | INFOCHEX™ | NTERCOM™ | SYS32™ |
| CheckTrack™ | Integral ISE™ | NURAM™ | TapePak® |
| CIM™ | Intellisplay™ | OXISS™ | TDS™ |
| CIMBUST™ | ISE™ | P2CMOST™ | TeleGate™ |
| CLASIC™ | ISE/06™ | PC Master™ | The National Anthem® |
| Clock✓Chek™ | ISE/08™ | Perfect Watch™ | Time✓Chek™ |
| COMBO® | ISE/16™ | Pharma✓Chek™ | TINA™ |
| COMBO I™ | ISE32™ | PLAN™ | TLCT™ |
| COMBO IITM | ISOPLANAR™ | PLANAR™ | Trapezoidal™ |
| COPST™ microcontrollers | ISOPLANAR-Z™ | PLAYER™ | TRI-CODE™ |
| CRDT™ | KeyScan™ | Plus-2™ | TRI-POLY™ |
| Datachecker® | LMCMOST™ | Polycraft™ | TRI-SAFET™ |
| DENSPA™ | M2CMOST™ | POSilink™ | TRI-STATE® |
| DIB™ | Macrobus™ | POSitalker™ | TURBOTRANSCEIVER™ |
| Digitalker® | Macrocomponent™ | Power + Control™ | VIPT™ |
| DISCERN™ | MAXI-ROM® | POWERplanar™ | VR32™ |
| DISTILL™ | Meat✓Chek™ | QUAD3000™ | WATCHDOG™ |
| DNR® | MenuMaster™ | QUICKLOOK™ | XMOST™ |
| DPVMT™ | Microbus™ data bus | RAT™ | XPUT™ |
| E2CMOST™ | MICRO-DACT™ | RTX16™ | Z START™ |
| ELSTART™ | μtalker™ | SABR™ | 883B/RETSTM |
| Embedded System Processor™ | Microtalker™ | Script✓Chek™ | 883S/RETSTM |
| | MICROWIRE™ | | |

Multewire® is a registered trademark of Multiwire Corporation.

Mylar® and Teflon® are registered trademarks of E.I. DuPont de Nemours Company.

PAL® is a registered trademark of and used under license from Advanced Micro Devices, Inc.

Sentry® is a registered trademark of Schlumberger Limited.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation 2900 Semiconductor Drive, P.O. Box 58090, Santa Clara, California 95052-8090 (408) 721-5000 TWX (910) 339-9240

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and National reserves the right, at any time without notice, to change said circuitry or specifications.

Introduction

National's F100K ECL family has gained acceptance as the standard subnanosecond logic and memory family used in high-speed, next generation systems. The family now includes the F100K 300 Series devices that offer specifications of DC and AC parameters over the full $-4.2V$ to $-5.7V$ V_{EE} operating range and $0^{\circ}C$ to $85^{\circ}C$ case temperature, military versions ($-55^{\circ}C$ to $+125^{\circ}C$), full voltage and temperature compensation, PCC packaging and 2000V minimum ESD protection. Together the 100 Series and 300 Series devices provide a ultra-high performance, cost-effective, easy to use ECL logic family.

F100K Data Book

Product Index and Selection Guide

The Product Index is a numerical list of all device types contained in this book, including one page descriptions on all of National's other ECL devices (SRAMs, PALs and ASICs). The Selection Guide groups the products by function and by family.

Section 1 Family Overview 1-1

Discusses F100K design philosophy and actualization and summarizes the key F100K features and advantages in high speed systems. The features and benefits of the 300 Series devices are brought out in great detail.

Section 2 F100K 300 Series Datasheets . . 2-1

Contains individual data sheets for the F100K 300 Series family devices.

Section 3 F100K 100 Series Datasheets . . 3-1

Contains individual data sheets for the F100K 100 Series family devices.

Section 4 11C Datasheets 4-1

Contains individual data sheets for the 11C devices.

Section 5 ECL BiCMOS SRAMs 5-1

Contains only the first page of each of the ECL BiCMOS SRAM data sheets. For full details refer to the Memory Databook.

Section 6 ECL PALs and ASIC's 6-1

Contains only the first page of each of the 6 ns and 4 ns ECL PAL datasheets, and the entire ECL ASIC datasheet. For full details on the PALs, refer to the Programmable Logic Devices Databook and Design Guide. For full details on the ASIC FGE Series, contact the ASIC Product Marketing Group. For details on the ASIC FGA Series, refer to the FGA Series ASPECT™ ECL Gate Array Datasheet.

F100K Design Guide and Application Notes—Section 7

Chapter 1 Circuit Basics 7-3

Discusses internal circuitry and logic function formation. Also, a sample analysis of noise margins is outlined.

Chapter 2 Logic Design 7-9

Features brief applications of F100K logic arranged according to function.

Chapter 3 Transmission Line Concepts . 7-22

Reviews the concepts of characteristic impedance and propagation delay and discusses termination, mismatch, reflections and associated waveforms.

Chapter 4 System Considerations 7-35

Extends the transmission line approach to the specific configurations, signal levels and parameter values of ECL. Various methods of driving and terminating signal lines are discussed.

Chapter 5 Power Distribution and Thermal Considerations 7-48

Discusses power supply, decoupling and system cooling requirements.

Chapter 6 Testing Techniques7-55

Discusses various methods and techniques used in testing ECL devices (intended for those concerned with customer incoming inspection). Also includes a section on Electrostatic Discharge, what is ESD and how we perform our ESD Classification testing.

Chapter 7 Quality Assurance and Reliability7-62

Reviews the quality and reliability programs currently in use.

Application Notes7-67

Contains several application notes on designing high speed systems using ECL.

Section 8 Ordering Information and Package Outlines 8-1

Alpha-Numeric Index

| | |
|--|-------|
| 11C01 Dual Input OR/NOR Gate | 4-3 |
| 11C05 1 GHz Divide-by-Four Counter | 4-6 |
| 11C06 750 MHz D-Type Flip-Flop | 4-10 |
| 11C70 Master-Slave D-Type Flip-Flop | 4-14 |
| 11C90 650 MHz Prescaler | 4-20 |
| 11C91 650 MHz Prescaler | 4-20 |
| AN-573 Design Considerations for High Speed Architectures | 7-67 |
| AN-582 Using the F100250 for Copper Wire Data Communications | 7-75 |
| AN-650 The ECL System Solution | 7-88 |
| AN-651 10K vs 100K ECL I/O System Considerations | 7-92 |
| AN-682 Terminating F100K ECL Inputs | 7-96 |
| AN-683 300 MHz Dual Eight-Way Multiplexer/Demultiplexer | 7-98 |
| AN-684 F100336 Four Stage Counter/Shift Register | 7-100 |
| AN-685 Using the F100181 ALU and F100179 Carry Look-Ahead | 7-107 |
| F100101 Triple 5-Input OR/NOR Gate | 3-3 |
| F100102 Quint 2-Input OR/NOR Gate | 3-6 |
| F100104 Quint 2-Input AND/NAND Gate | 3-9 |
| F100107 Quint Exclusive OR/NOR Gate | 3-13 |
| F100112 Quad Driver | 3-17 |
| F100113 Quad Driver | 3-21 |
| F100114 Quint Differential Line Receiver | 3-25 |
| F100115 Low Skew Quad Driver | 3-29 |
| F100117 Triple 2-Wide OA/OAI Gate | 3-33 |
| F100118 5-Wide 5-4-4-4-2 OA/OAI Gate | 3-36 |
| F100121 9-Bit Inverter | 3-40 |
| F100122 9-Bit Buffer | 3-43 |
| F100123 Hex Bus Driver | 3-46 |
| F100124 Hex TTL-to-100K ECL Translator | 3-50 |
| F100125 Hex 100K ECL-to-TTL Translator | 3-54 |
| F100126 9-Bit Backplane Driver | 3-58 |
| F100128 Octal Bidirectional ECL/TTL Translator | 3-61 |
| F100130 Triple D Latch | 3-70 |
| F100131 Triple D Flip-Flop | 3-76 |
| F100135 Triple JK Flip-Flop | 3-84 |
| F100136 4-Stage Counter/Shift Register | 3-90 |
| F100141 8-Bit Shift Register | 3-100 |
| F100142 4 x 4 Content Addressable Memory | 3-106 |
| F100150 Hex D Latch | 3-113 |
| F100151 Hex D Flip-Flop | 3-119 |
| F100155 Quad Multiplexer/Latch | 3-125 |
| F100156 Mask/Merge Latch | 3-131 |
| F100158 8-Bit Shift Matrix | 3-137 |
| F100160 Dual Parity Checker/Generator | 3-145 |
| F100163 Dual 8-Input Multiplexer | 3-150 |
| F100164 16-Input Multiplexer | 3-155 |
| F100165 Universal Priority Encoder | 3-160 |
| F100166 9-Bit Comparator | 3-166 |
| F100170 Universal Demultiplexer/Decoder | 3-171 |
| F100171 Triple 4-Input Multiplexer with Enable | 3-176 |
| F100175 Quint 100K-to-10K Latch | 3-181 |
| F100179 Carry Lookahead Generator | 3-187 |

Alpha-Numeric Index (Continued)

| | |
|--|-------|
| F100180 High-Speed 6-Bit Adder | 3-194 |
| F100181 4-Bit Binary/BCD ALU | 3-199 |
| F100182 9-Bit Wallace Tree Adder | 3-206 |
| F100183 2 x 8-Bit Recode Multiplier | 3-214 |
| F100250 Quint Full Duplex Line Transceiver | 3-226 |
| F100301 Low Power Triple 5-Input OR/NOR Gate | 2-3 |
| F100302 Low Power Quint 2-Input OR/NOR Gate | 2-8 |
| F100304 Low Power Quint AND/NAND Gate | 2-13 |
| F100307 Low Power Quint Exclusive OR/NOR Gate | 2-17 |
| F100311 Low Skew 9-Bit Clock Driver | 2-21 |
| F100313 Low Power Quad Driver | 2-22 |
| F100314 Low Power Quint Differential Line Receiver | 2-27 |
| F100321 Low Power 9-Bit Inverter | 2-28 |
| F100322 Low Power 9-Bit Buffer | 2-34 |
| F100324 Low Power Hex TTL-to-ECL Translator | 2-38 |
| F100325 Low Power Hex ECL-to-TTL Translator | 2-43 |
| F100328 Low Power Octal ECL/TTL Bidirectional Translator with Latch | 2-50 |
| F100329 Low Power Octal ECL/TTL Bidirectional Translator with Register | 2-51 |
| F100331 Low Power Triple D Flip-Flop | 2-52 |
| F100336 Low Power 4-Stage Counter/Shift Register | 2-53 |
| F100341 Low Power 8-Bit Shift Register | 2-68 |
| F100343 Low Power Octal Latch | 2-76 |
| F100344 Low Power Octal Latch with Cutoff Drivers | 2-83 |
| F100350 Low Power Hex D Latch | 2-90 |
| F100351 Low Power Hex D Flip-Flop | 2-91 |
| F100352 Low Power Octal Buffer with Cutoff Drivers | 2-98 |
| F100353 Low Power Octal Register | 2-105 |
| F100354 Low Power Octal Register with Cutoff Drivers | 2-112 |
| F100355 Low Power Quad Multiplexer/Latch | 2-119 |
| F100360 Low Power Dual Parity Checker/Generator | 2-128 |
| F100363 Low Power Dual 8-Input Multiplexer | 2-135 |
| F100364 Low Power 16-Input Multiplexer | 2-141 |
| F100370 Low Power Universal Demultiplexer/Decoder | 2-142 |
| F100371 Low Power Triple 4-Input Multiplexer | 2-143 |
| F100393 Low Power 9-Bit ECL-to-TTL Translator with Latch | 2-144 |
| F100395 Low Power 9-Bit ECL-to-TTL Translator with Register | 2-145 |
| FGA Series ASPECT ECL Gate Arrays | 6-11 |
| NM5100/NM100500 ECL I/O 256k BiCMOS SRAM 262,144 x 1 Bit | 5-3 |
| NM5104/NM100504 256k BiCMOS SRAM 64k x 4 Bit | 5-4 |
| NM100492/NM4492 2k x 9 Advanced Self-Timed SRAM (Preliminary) | 5-7 |
| NM100494 64k BiCMOS SRAM 16k x 4 Bit | 5-5 |
| NM10494 64k BiCMOS SRAM 16k x 4 Bit | 5-6 |
| PAL10/10016C4-2 2 ns ECL ASPECT Programmable Array Logic (PLCC) | 6-8 |
| PAL10/10016P4-2 2 ns ECL ASPECT Programmable Array Logic (DIP) | 6-7 |
| PAL10/10016P4A 4 ns ECL Programmable Array Logic | 6-6 |
| PAL10/10016P8 ECL Programmable Array Logic | 6-3 |
| PAL10/10016P8-3 3 ns ECL ASPECT Programmable Array Logic (DIP) | 6-4 |
| PAL10/10016PE8-3 3 ns ECL ASPECT Programmable Array Logic (PLCC) | 6-5 |
| PAL10/10016RD8 ECL Registered Programmable Array Logic | 6-9 |
| PAL10/10016RM4A ECL Registered Programmable Array Logic | 6-10 |

F100K Product Selection Guide

Gates

| Function | Device | Inputs/ Gate | No. of Gates | Leads |
|----------------------------------|--------|-----------------|-----------------|-------------|
| OR/NOR/Exclusive OR | | | | |
| Low Power Triple 5-Input OR/NOR | 100301 | 5 | 3 | 24, 28(PCC) |
| Triple 5-Input OR/NOR | 100101 | 5 | 3 | 24 |
| Low Power Quint 2-Input OR/NOR | 100302 | 2 | 5 | 24, 28(PCC) |
| Quint 2-Input OR/NOR | 100102 | 2 | 5 | 24 |
| Dual Input OR/NOR | 11C01 | 4/5 | 2 | 16 |
| Low Power Quint Exclusive OR/NOR | 100307 | 2 | 5 | 24, 28(PCC) |
| Quint Exclusive OR/NOR | 100107 | 2 | 5 | 24 |
| AND/NAND | | | | |
| Low Power Quint 2-Input AND/NAND | 100304 | 2 | 5 | 24, 28(PCC) |
| Quint 2-Input AND/NAND | 100104 | 2 | 5 | 24 |
| OR-AND/OR-AND-INVERT | | | | |
| Triple 2-Wide OA/OAI | 100117 | 2 | 3 | 24 |
| 5-Wide 5, 4, 4, 4, 2 OA/OAI | 100118 | 5/4/4/4/2 | 1 | 24 |

Flip-Flops

| Function | Device | Clock Edge | Direct Set | Direct Clear | Complementary Outputs | Leads |
|------------------------------|--------|---------------|---------------|-----------------|--------------------------|-------------|
| Low Power Triple D Flip-Flop | 100331 | ↘ | Yes | Yes | Yes | 24, 28(PCC) |
| Triple D Flip-Flop | 100131 | ↘ | Yes | Yes | Yes | 24 |
| Triple J-K Flip-Flop | 100135 | ↘ | Yes | Yes | Yes | 24 |
| Low Power Hex D Flip-Flop | 100351 | ↘ | No | Yes | Yes | 24, 28(PCC) |
| Hex D Flip-Flop | 100151 | ↘ | No | Yes | Yes | 24 |
| 750 MHz D Flip-Flop | 11C06 | ↘ | No | No | Yes | 16 |
| Master-Slave D Flip-Flop | 11C70 | ↘ | Yes | Yes | Yes | 16 |

Latches

| Function | Device | Enable Inputs | Complementary Outputs | Direct Set | Direct Clear | Leads |
|---|--------|------------------|--------------------------|---------------|-----------------|-------------|
| Triple D Latch | 100130 | 4(L) | Yes | Yes | Yes | 24 |
| Low Power Hex D Latch | 100350 | 2(L) | No | Yes | Yes | 24, 28(PCC) |
| Hex D Latch | 100150 | 2(L) | Yes | No | Yes | 24 |
| Low Power Quad 2-Input Mux/Latch | 100355 | 2(L) | No | Yes | Yes | 24, 28(PCC) |
| Quad 2-Input Mux/Latch | 100155 | 2(L) | Yes | No | Yes | 24 |
| Mask-Merge Latch | 100156 | 1(L) | No | No | No | 24 |
| Quint 100K-to-10K Latch | 100175 | 2(L) | No | No | Yes | 24 |
| Low Power 8-Bit Latch | 100343 | 2(L) | No | No | No | 24, 28(PCC) |
| Low Power 8-Bit Latch w/Cutoff Drivers and 25Ω Drive | 100344 | 3(L) | No | No | No | 24, 28(PCC) |







Multiplexers/Demultiplexers/Decoders

| Function | Device | Enable Inputs | Complementary Outputs | Leads |
|-------------------------------------|--------|---------------|-----------------------|-------------|
| Multiplexers | | | | |
| Low Power Quad 2-Input Mux/Latch | 100355 | 2(L) | Yes | 24, 28(PCC) |
| Quad 2-Input Mux/Latch | 100155 | 2(L) | Yes | 24 |
| Low Power Dual 8-Input | 100363 | | No | 24, 28(PCC) |
| Dual 8-Input | 100163 | | No | 24 |
| Low Power 16-Input | 100364 | | No | 24, 28(PCC) |
| 16-Input | 100164 | | No | 24 |
| Low Power Triple 4-Input | 100371 | 1(L) | Yes | 24, 28(PCC) |
| Triple 4-Input | 100171 | 1(L) | Yes | 24 |
| Decoders/Demultiplexers | | | | |
| Low Power Dual 1-of-4/Single 1-of-8 | 100370 | 2(L) & 2(L) | No | 24, 28(PCC) |
| Dual 1 of 4/Single 1 of 8 | 100170 | 2(L) & 2(L) | No | 24 |

Translators

| Function | Device | Enable Inputs | Features | Complementary | Leads |
|---------------------------------------|--------|---------------|-----------|---------------|-------------|
| Low Power Hex TTL-to-100K ECL | 100324 | 1(H) | Flow-thru | Outputs | 24, 28(PCC) |
| Hex TTL-to-100K ECL | 100124 | 1(H) | Flow-thru | Outputs | 24 |
| Low Power Hex 100K ECL-to-TTL | 100325 | | Flow-thru | Inputs | 24, 28(PCC) |
| Hex 100K ECL-to-TTL | 100125 | | Flow-thru | Inputs | 24 |
| Low Power Octal Bidirectional ECL/TTL | 100328 | 1(H) | Latch | | 24, 28(PCC) |
| Low Power Octal Bidirectional ECL/TTL | 100329 | | Register | | 24, 28(PCC) |
| Octal Bidirectional ECL/TTL | 100128 | 1(H) | Latch | | 24 |
| Quint 100K-to-10K | 100175 | 2(H) | Latch | | 24 |
| Low Power 9-Bit ECL-to-TTL | 100393 | 1(H) | Latch | | 24, 28(PCC) |
| Low Power 9-Bit ECL-to-TTL | 100395 | | Register | | 24, 28(PCC) |

Registers/Shift Registers

| Function | Device | Clock Inputs | Complementary Outputs | Leads |
|---|--------|---|-----------------------|-------------|
| Registers | | | | |
| Low Power 8-Bit Register | 100353 |  | No | 24, 28(PCC) |
| Low Power 8-Bit Register w/Cutoff Drivers and 25Ω Drive | 100354 |  | No | 24, 28(PCC) |
| Shift Registers | | | | |
| Low Power 4-Bit Bidirectional Shift Reg. | 100336 |  | Yes | 24, 28(PCC) |
| 4-Bit Bidirectional Shift Reg | 100136 |  | Yes | 24 |
| Low Power 8-Bit Shift Register | 100341 |  | No | 24, 28(PCC) |
| 8-Bit Shift Register | 100141 |  | No | 24 |

New Octals

| Function | Device | 25Ω Drive | Output Cutoff | Leads |
|--------------------------|--------|-----------|---------------|-------------|
| Low Power 8-Bit Latch | 100343 | No | No | 24, 28(PCC) |
| Low Power 8-Bit Latch | 100344 | Yes | Yes | 24, 28(PCC) |
| Low Power 8-Bit Buffer | 100352 | Yes | Yes | 24, 28(PCC) |
| Low Power 8-Bit Register | 100353 | No | No | 24, 28(PCC) |
| Low Power 8-Bit Register | 100354 | Yes | Yes | 24, 28(PCC) |

Buffers/Drivers/Receivers

| Function | Device | Output Polarity | 25Ω Drive | Output Cut-Off | Leads |
|--|--------|-----------------|-----------|----------------|-------------|
| Buffers/Inverters | | | | | |
| Low Power 9-Bit Inverter | 100321 | Inverting | No | No | 24, 28(PCC) |
| 9-Bit Inverter | 100121 | Inverting | No | No | 24 |
| Low Power 9-Bit Buffer | 100322 | Non-Inverting | No | No | 24, 28(PCC) |
| 9-Bit Buffer | 100122 | Non-Inverting | No | No | 24 |
| Low Power 8-Bit Buffer | 100352 | Non-Inverting | Yes | Yes | 24, 28(PCC) |
| Drivers/Bus Drivers | | | | | |
| Low Power Quad Line Driver | 100313 | Differential | No | No | 24, 28(PCC) |
| Quad Line Driver | 100113 | Differential | No | No | 24 |
| Quad Line Driver | 100112 | Differential | No | No | 24 |
| Low Skew Quad Clock Driver | 100115 | Differential | No | No | 16 |
| Low Skew 9-Bit Clock Driver | 100311 | Differential | No | No | 28(PCC) |
| Hex Bus Driver | 100123 | Non-Inverting | Yes | Yes | 24 |
| 9-Bit Backplane Driver | 100126 | Non-Inverting | No | No | 24 |
| Receivers/Transceivers | | | | | |
| Low Power Quint Differential Line Receiver | 100314 | Differential | No | No | 24, 28(PCC) |
| Quint Differential Line Receiver | 100114 | Differential | No | No | 24 |
| Quint Full Duplex Line Transceiver | 100250 | Differential | No | No | 24 |

Counters/Prescalers

| Function | Device | Parallel Entry | Reset | Up/Down | Leads |
|--------------------------------|--------|----------------|-------|---------|-------------|
| Counters | | | | | |
| Low Power 4-Bit Binary Counter | 100336 | S | S/A | Yes | 24, 28(PCC) |
| 4-Bit Binary Counter | 100136 | S | S/A | Yes | 24 |
| 1 GHz Divide-by-Four Counter | 11C05 | | No | No | 16 |
| Prescalers | | | | | |
| 650 MHz Prescaler | 11C90 | | No | No | 16 |
| 650 MHz Prescaler | 11C91 | | No | No | 16 |

Arithmetic Operators

| Function | Device | Features | Leads |
|---|--------|--------------------------|-------------|
| High Speed 6-Bit Adder | 100180 | | 24 |
| Carry Lookahead | 100179 | | 24 |
| 4-Bit Binary/BCD ALU | 100181 | 8 Logic/8 Arithmetic Ops | 24 |
| 9-Bit Wallace Tree Adder | 100182 | Expandable | 24 |
| 2 x 8-Bit Recode Multiplier | 100183 | | 24 |
| Low Power Dual 9-Bit Parity Checker/Generator | 100360 | Expandable | 24, 28(PCC) |
| Dual 9-Bit Parity Checker/Generator | 100160 | Expandable | 24 |
| 9-Bit Comparator | 100166 | Expandable | 24 |
| 8-Input Priority Encoder | 100165 | Dual 4-Bit/Single 8-Bit | 24 |
| 8-Bit Shift Matrix | 100158 | Barrel Shift, Backfill | 24 |
| 4-Bit Mask-Merge/Latch | 100156 | Bit-Selectable Merge | 24 |
| 4 x 4-Bit Content Addressable Memory | 100142 | | 24 |

BiCMOS ECL I/O SRAM Selection Guide

| Part Number | Organization | I/O Level | V _{EE} | Access (ns) | Leads | Temperature Range |
|-------------|--------------|-----------|-----------------|-------------|-------|-------------------|
| NM5100 | 256k x 1 | 100K | -5.2V ±5% | 15 | 24 | 0°C to +85°C |
| NM100500 | 256k x 1 | 100K | -4.2V to -4.8V | 15 | 24 | 0°C to +85°C |
| NM5104 | 64k x 4 | 100K | -5.2V ±5% | 12, 15 | 28 | 0°C to +85°C |
| NM100504 | 64k x 4 | 100K | -4.2V to -4.8V | 15 | 28 | 0°C to +85°C |
| NM100494 | 16k x 4 | 10K | -4.2V to -4.8V | 15, 18 | 28 | 0°C to +85°C |
| NM10494 | 16k x 4 | 100K | -5.2V ±5% | 10, 12, 15 | 28 | 0°C to +75°C |
| NM100492 | 2k x 9 | 100K | -4.2V to -4.8V | 7, 10 | 64 | 0°C to +75°C |
| NM4492 | 2k x 9 | 100K | -5.2V ±5% | 5, 7, 10 | 64 | 0°C to +75°C |

For further information on the ECL SRAMs, see the one page description of each device in this book; or refer to the Memory Databook for full details.

ECL Programmable Logic Selection Guide

| Part Number | T _{PD} (Max) (Note 1) | I _{CC} (Max) | Outputs | | Leads |
|---------------|-----------------------------------|-----------------------|---------------|------------|-------|
| | | | Combinatorial | Registered | |
| PAL1016P8 | 6 ns | -240 mA | 8 | | 24 |
| PAL10016P8 | 6 ns | -240 mA | 8 | | 24 |
| PAL1016P4A | 4 ns | -220 mA | 4 | | 24 |
| PAL10016P4A | 4 ns | -220 mA | 4 | | 24 |
| PAL1016PE8-3 | 3 ns | -180 mA | 8 | | 28 |
| PAL10016PE8-3 | 3 ns | -180 mA | 8 | | 28 |
| PAL1016P8-3 | 3 ns | -180 mA | 8 | | 24 |
| PAL10016P8-3 | 3 ns | -180 mA | 8 | | 24 |
| PAL1016C4-2 | 2 ns | -180 mA | 4 | | 28 |
| PAL10016C4-2 | 2 ns | -180 mA | 4 | | 28 |
| PAL1016P4-2 | 2 ns | -180 mA | 4 | | 24 |
| PAL10016P4-2 | 2 ns | -180 mA | 4 | | 24 |
| PAL1016RD8 | 6 ns | -280 mA | | 8 | 24 |
| PAL10016RD8 | 6 ns | -280 mA | | 8 | 24 |
| PAL1016RM4A | 4 ns | -220 mA | | 4 | 24 |
| PAL10016RM4A | 4 ns | -220 mA | | 4 | 24 |

Note 1: Maximum t_{PD} for combinatorial outputs (commercial operating range). Denotes characteristic speed of family where product has all registered outputs.

For further information on the ECL PALs, see the one page description of the devices in this book; or refer to the Programmable Logic Devices Databook and Design Guide.

ECL Gate Array Selection Guide

FGE Series

| Part Number | Equivalent Gates | Internal Cells | Internal Gate Delay | Leads |
|-------------|----------------------------|----------------|---------------------|-------|
| FGE0050 | 60 | 4 | 225 ps | 24 |
| FGE0500 | 680 | 50 | 225 ps | 84 |
| FGE2000 | 2500 | 224 | 225 ps | 132 |
| FGE2450 | 2840 | 252 | 225 ps | 99 |
| FGE2500 | 2840 | 252 | 225 ps | 156 |
| FGE6300 | 6300 | 560 | 250 ps | 301 |
| FGE6320R | 3500 plus 2.3k Bits RAM | 280 | 250 ps | 301 |

For further information on the ECL FGE Series Gate Arrays, contact the ASIC Product Marketing Group.

FGA Series—ASPECT

| Part Number | Equivalent Gates | Internal Cells | Internal Gate Delay | Leads |
|-------------|----------------------------|-----------------------------|---------------------|-------------------|
| FGA0150 | 269 | 75 | 150 ps | 16, 24, 28 |
| FGA0200 | 269 | 75 | 150 ps | 16, 24, 28 |
| FGA0600 | 792 | 240 | 150 ps | 44, 75 |
| FGA1300 | 1642 | 528 | 150 ps | 75, 109, 116 |
| FGA2800 | 3035 | 1044 | 150 ps | 75, 109, 116 |
| FGA4000 | 4704 | 1600 | 150 ps | 99, 132, 172, 173 |
| FGA8000 | 8000 | 3000 | 150 ps | 99, 132, 172, 173 |
| FGA14000 | 16709 | 5904 | 150 ps | 323 |
| FGA15000 | 16644 | 5920 | 150 ps | 303 |
| FGA30000 | 28486 | 10266 | 150 ps | 323 |
| FGA14040R | 7835 plus 4.6k Bits RAM | 2624 plus 64 x 9 x 8 RAM | 150 ps | 323 |

For further information on the ECL Gate Array devices, see the full description of the FGA Series in this book; or refer to the FGA Series ASPECT™ ECL Gate Array Databook.



Product Status Definitions

Definition of Terms

| Data Sheet Identification | Product Status | Definition |
|--|---------------------------|--|
| Advance Information | Formative or In Design | This data sheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| No Identification Noted | Full Production | This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

National Semiconductor Corporation reserves the right to make changes without further notice to any products herein to improve reliability, function or design. National does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.



Section 1
Family Overview



Section 1 Contents

| | |
|---|------|
| Family Overview | 1-3 |
| Introduction | 1-3 |
| F100K 100 Series Design Philosophy | 1-3 |
| Process Technology | 1-4 |
| Compensation Network | 1-5 |
| Characteristics | 1-6 |
| F100K 300 Series Design Philosophy | 1-7 |
| System Aspects | 1-10 |
| Features | 1-10 |
| System Benefits | 1-11 |
| Packaging | 1-11 |
| Using F100K ECL 300 Series in Military Applications | 1-11 |
| Definitions of Symbols and Terms | 1-12 |



Family Overview

Introduction

Systems designers have found that Emitter Coupled Logic (ECL) circuits offer significant advantages to high-speed systems. These advantages include high switching rates with moderate power consumption, low propagation delays with moderate edge rates, and the ability to drive low impedance transmission lines. Most F100K devices have 50 k Ω pull-down resistors on all the inputs.

The F100K ECL family is the realization of refinements made on ECL design to produce a family of ultrafast logic and memory components. These components are capable of providing ultimate performance for packaged SSI/MSI, are easy to use, and cost effective.

F100K ECL has been accepted as the standard subnanosecond logic and memory family used in high-speed, next generation systems. The advance into complex LSI and gate arrays is fully supported by the F100K SSI/MSI parts.

Beginning in 1989, National introduced a new line of F100K ECL products, known as 300 Series. These 300 Series products are fully compatible with existing F100K 100 Series Products, but offer many improvements. Features include much lower power dissipation, stable DC specifications over a wider supply voltage range, plastic chip carrier (PCC) surface mount packaging, higher electrostatic discharge (ESD) tolerance, and full MIL-STD-883C qualification levels. The 300 Series family includes pin and function compatible versions of several popular 100 Series products, as well as many new proprietary products.

Most of the 300 Series improvements were extensions of F100K 100 Series design and process techniques. This section will begin with an overview of the F100K 100 Series family, and then discuss the 300 Series improvements. Generic references to F100K apply to both Series of products.

F100K 100 Series Design Philosophy

F100K 100 Series was designed to meet four key requirements: high speed at reduced power, high level of on-chip integration, flexible logic functions, and optimum I/O pin assignment.

Subnanosecond Gate Delays

The subnanosecond internal gate delays of F100K 100 Series are obtained by the use of ECL design techniques and the advanced Isoplanar-Z process. Many circuit approaches were carefully considered prior to selecting the optimum gate configuration for the F100K family. The emitter-follower current-switch (E^2 CCL) and current-mode logic (CML) gates were eliminated mainly because of poor capacitive drive and lack of output wired-OR capability; the CML gate has low noise margins. The 2- $\frac{1}{2}$ D, EFL, DCTTL and hysteresis gates were eliminated due to the lack of simultaneous complementary outputs along with difficult temperature and volt-

age compensation characteristics that lead to the loss of system noise immunity.

The choice narrowed down to the current-switch emitter-follower ECL gate which offers the following characteristics:

- High fan-out capability
- Simultaneous complementary outputs
- Excellent AC characteristics
- Compatibility with existing ECL logic and memories
- Internal series gating capability
- Good noise immunity
- Amenable full compensation and extended temperature characteristics
- External wired-OR capability

In order to ease drive requirements all circuit inputs were designed to have similar loading characteristics; i.e., buffers are incorporated where an input pin would normally drive more than one on-chip gate. The on-chip delay incurred by buffering is less than the system delay caused by an output which drives a capacitance of higher than three unit loads. Full compensation was selected for the F100K Family to provide improved switching characteristics. Full compensation results in relatively constant signal levels and thresholds and in improved noise margins over temperature and voltage variations from chip to chip, and thus a tighter AC window in the system environment. A comparison of fully compensated ECL to conventional ECL shows a 2:1 improvement in system AC performance due solely to full compensation (*Figure 1-1*). And, the improved speed has been achieved at reduced power. Power reduction is accomplished by the use of advanced process technology that reduces parasitic capacitances and improves tolerances, by optimum circuit designs using series gating and collector and emitter dotting, and by designing for the use of a $-4.5V$ V_{EE} power supply. F100K 100 Series is specified at a V_{EE} power supply of $-4.2V$ to $-4.8V$, but a $-5.2V \pm 10\%$ power supply can be used to interface with 2 ns ECL families.

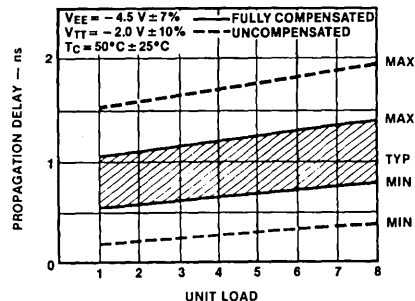


FIGURE 1-1. Comparison of Propagation Delays

TL/F/9908-1

High On-Chip Integration

Higher on-chip integration is made possible by using the 24-pin package to increase the number of signal pins by 62% over the conventional 16-pin package. The emphasis in F100K is to minimize the number of SSI functions and maximize the use of MSI and LSI to reduce wiring delays and thus make more efficient use of the fast on-chip switching technology. Only 10 SSI functions are needed to serve the system needs presently requiring 25 functions in the ECL 10K family.

Flexibility and Pin Assignment

F100K was planned to minimize to total number of logic functions by increasing the flexibility of each function and by making use of more I/O pins. Since next-generation system performance and ease of system designs are major F100K goals, pin assignment is important and was planned to minimize crosstalk, noise coupling and feedthrough, to facilitate OR-ties and to ease power-bus routing. Some of the key considerations in selecting the F100K pin assignments were:

- Locate power pins in the center on opposite sides of the DIP package to ease system design and to provide low-inductance connections to the chip.
- Provide two V_{CC} pins, one for the internal circuit and one for the output buffers, to minimize noise coupling.
- Locate inverting outputs of logically independent gates adjacent to each other. This provides the ability to wire AND-OR-Invert functions with ease.
- Locate common pins such as common Reset and common Clock at pin number 22 and Address or control inputs at pins 19 and 20 for flatpaks. This is to maximize use of Computer Aided Design (CAD) for board layouts.
- When feasible, mode control pins are used to create multipurpose devices.

Process Technology

FAST-Z Process

The F100K 100 Series ECL family is fabricated using an advanced isoplanar technology called FAST-Z. This process makes possible subnanosecond logic delays and very

highly controlled switching characteristics for consistent device-to-device high-speed performance.

The technology can best be described by reviewing the evolution of the transistor structure from the conventional planar and the original Isoplanar II processes to the FAST-Z and FAST-LSI processes (Figure 1-2). The top view shows the area needed for each structure; the dashed area is the center of the isolation region.

As in all Isoplanar technologies, the FAST-Z processes selectively grow a thick oxide between devices instead of the P+ region that is present in the planar process. The oxide needs no separation from the base-collector regions, resulting in a substantial reduction in device and chip size. The base and emitter ends terminate in the oxide wall. The mask openings can therefore overlap onto the isolation oxide making them self-aligned in that direction. This overlap feature means that base and emitter masking does not have to meet the extremely close tolerances that might otherwise be necessary. In addition, the FAST-Z transistor contacts are defined on a single mask layer making them self-aligned in the other direction.

Both the self-alignment feature and the ability to overlap the mask openings onto the isolation oxide provide improved process control. The need to meet extremely close tolerances that otherwise might be necessary is therefore avoided.

The FAST-Z "walled emitter" structures provide a reduction in transistor silicon area of 400 percent as compared to the planar structure. The collector-substrate therefore is also reduced by 400 percent. The collector-base area is reduced by 540 percent. These area reductions, combined with the shallower junctions achieved by well controlled ion implantation processes, provide significantly reduced capacitance and resistance values within the FAST-Z transistor structure. This, in turn, allows higher speeds.

FAST-LSI Process

The 300 Series family is fabricated using an advanced isoplanar technology called FAST-LSI. The FAST-LSI process is similar to FAST-Z, but also includes many improvements which enhance performance, manufacturability, and reliability. Metal alignments have been tightened, shortening the

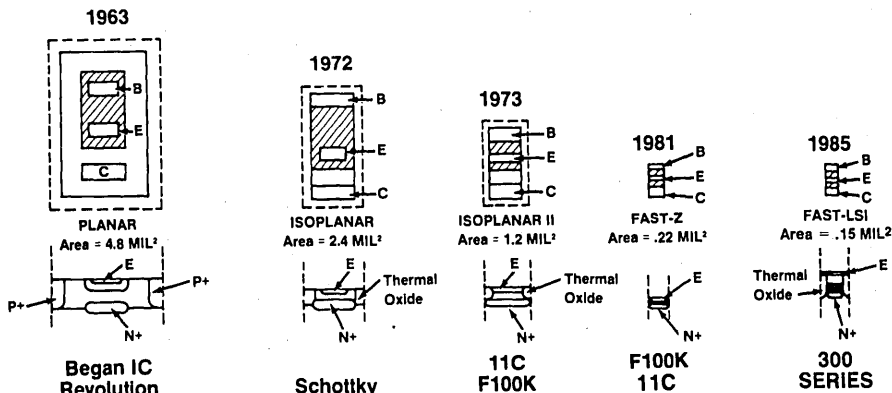


FIGURE 1-2. Evolution of Bipolar Transistor Structures

TL/F/9908-2

distance between base and emitter contacts. This reduces the base capacitance, giving F_{TS} of 8 GHz vs 5 GHz for FAST-Z. Parasitic capacitances are also reduced, allowing products to be designed with lower power consumption.

The FAST-LSI process implements wafer planarization techniques to smooth the interconnect metal transitions, significantly reducing thermal stresses on the die when encapsulated in molded plastic packaging. In addition, these planarization techniques increase metal step coverage to typically 65% for first level metal and 75% for second level metal. Increased metal thicknesses over a step improve current density performance and circuit reliability. First layer metal step coverage is improved by the addition of bird's head planarization after the oxide isolation process. Second layer metal step coverage improvements are provided by a technique known as spun-on-glass, an interlayer dielectric planarization.

FAST-LSI is a fully ion-implanted process, providing more precise control over doping profiles. This not only improves device performance, but also allows tighter manufacturing tolerances on transistor gains and resistor values. These tighter tolerances were exploited in the design of F100K 300 Series to meet the same-speed, half-power targets for the product line. The field oxide in FAST-LSI is doped (vs. undoped in FAST-Z). This lowers current leakage even further while still maintaining the walled emitter structures featured in FAST-Z.

The metal structure of FAST-LSI is also improved. Platinum-silicide is used to provide ohmic contacts to N⁺ and P⁺ regions, as well as Schottky diode contacts to N⁻ regions. The Schottky diodes are used in the design of the high-performance TTL output stages in the 300 Series ECL-TTL level translators. A titanium-tungsten layer is utilized as a diffusion barrier against aluminum migration into the underlying silicon. Finally, both first and second layer metal use a copper-doped aluminum metalization which enhances reliability by providing a high resistance to electromigration.

Compensation Network

The heart of F100K is fully compensated ECL.¹ The basic gate consists of three blocks—the current switch, the output emitter-followers, and the reference or bias network (Figure 1-3). The current switch allows both conjunctive and disjunctive logic. The output emitter-followers provide high drive capability through impedance transformation and allows for increased logic swing. The bias network sets DC thresholds and current-source bias voltages. Temperature compensation at the gate output is achieved by incorporating a cross-connect branch between the complementary

collector nodes of the current switch and driving the current source with a temperature insensitive bias network² (Figure 1-4).

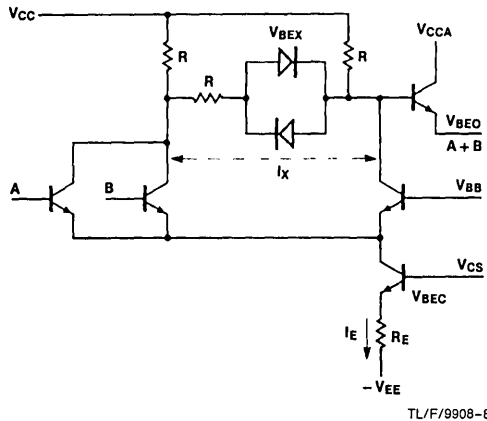


FIGURE 1-4. Temperature Compensation

As junction temperature increases and the forward base-emitter voltage of the output emitter-follower decreases, the collector node of the current switch must become more negative. Since the current-source bias voltage, V_{CS} , is independent of temperature, the switch current increases with temperature due to the temperature dependence of V_{BE3} . The combination of temperature controlled current, I_E , and the cross-connect branch current, I_X , forces the proper temperature coefficient at the collector node of the current switch to null out the V_{BE0} tracking coefficient.³

The schematic for the reference network displays a V_{BE1} amplifier in the bottom left corner (Figure 1-5). Two base-emitter junctions are operated at different current densities, J_1 and J_2 . The resulting voltage difference, V_{BE1} minus V_{BE2} , appears across R_1 and is amplified by the ratio R_2/R_1 . Note that R_2 is used twice, once to generate V_{CS} and once to generate V_{BB} . The different current densities, J_1 and J_2 , result in a positive temperature tracking coefficient across R_2 , which cancels the negative diode-tracking coefficient of V_{BE3} and V_{BE4} . The V_{CS} and the V_{BB} thus generated are temperature insensitive at the extrapolated bandgap voltage of silicon^{1, 2} (approximately 1300 mV).⁴ R_X in the V_{BE} amplifier compensates for process variations of β and ΔV_{BE} .⁵ Voltage regulation is achieved through a shunt regulator shown at the right side of the schematic.

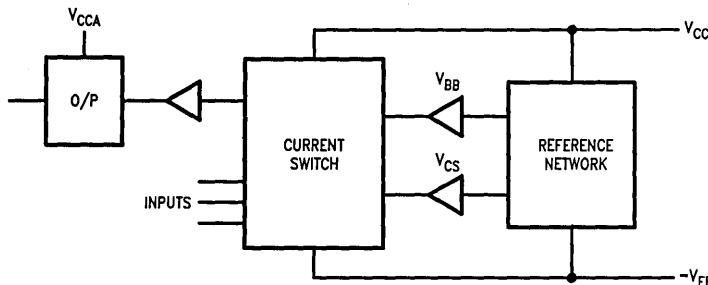


FIGURE 1-3. ECL Gate

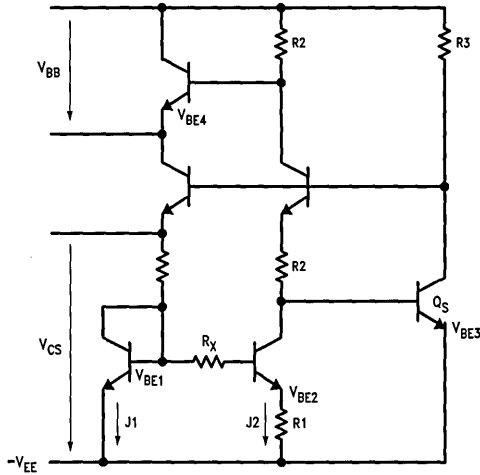


FIGURE 1-5. Reference Network

TL/F/9908-9

Characteristics

F100K compatibility with existing ECL logic families and memories permit direct interface with slower logic families and ensures immediate memory availability. The typical logic swing is 800 mV (Figure 1-6) and all voltage levels are specified with a 50Ω load to -2V at all outputs to provide transmission line drive capability. However, the inherently low output impedance (Figure 1-7) and maximum specified output current, 50 mA, make 25Ω drive possible at any or all outputs. Alternately, of course, higher termination impedances or other termination schemes are also useful.

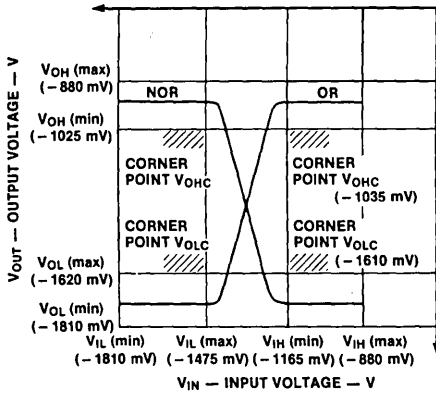


FIGURE 1-6. Transfer Characteristics

TL/F/9908-10

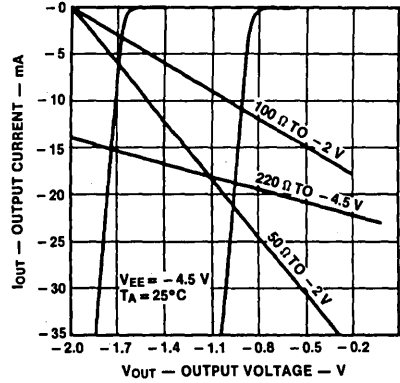
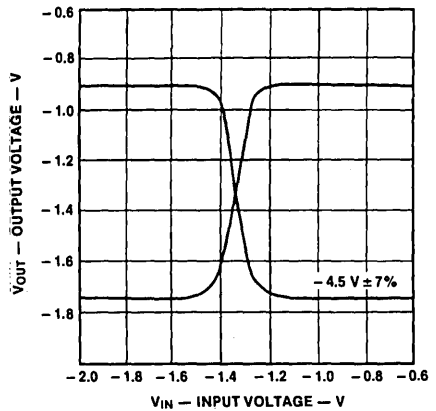


FIGURE 1-7. Output Characteristics vs Output Terminations

TL/F/9908-11

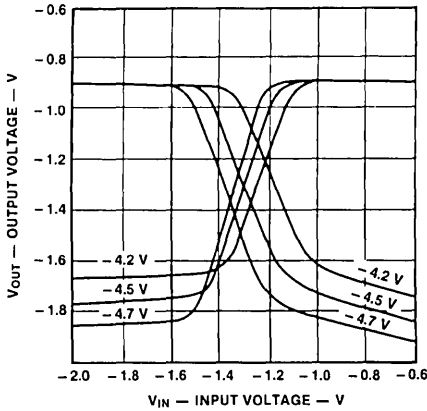
F100K exhibits relatively constant output levels and thresholds over the 0°C to +85°C specified temperature range and -4.2V to -4.8V specified voltage range (Figure 1-8). V_{EE} power supply current is also constant over the specified voltage range (Figure 1-9); therefore:

Fully Compensated ECL (over V_{EE} range)



TL/F/9908-14

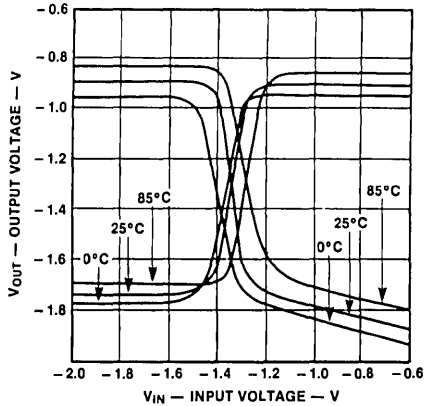
Uncompensated ECL (over V_{EE} range)



TL/F/9908-12

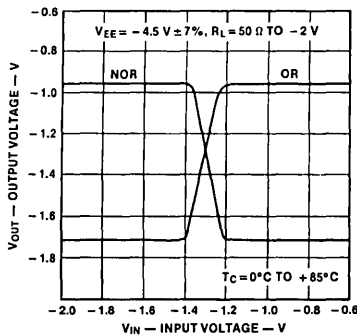
FIGURE 1-8. Transfer Characteristics

Uncompensated ECL (over temperature)



TL/F/9908-13

Fully Compensated ECL (over temperature)

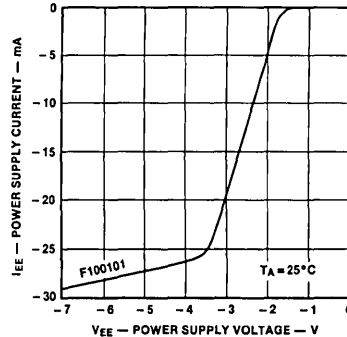


TL/F/9908-15

FIGURE 1-8. Transfer Characteristics (Continued)

- Propagation delay is relatively constant versus power supply voltage variations thus tightening the AC window.
- Power dissipation is a linear function of the supply voltage, reducing worst-case power consumption.

The typical propagation delay of an SSI gate function driving a 50Ω transmission line is 0.75 ns, including package, with a power dissipation of 40 mW resulting in a speed-power product of 30 pJ. For optimized MSI functions, the internal gates can dissipate < 10 mW with average propagation delay of < 0.5 ns, giving a power-speed product of < 5 pJ.



TL/F/9908-16

FIGURE 1-9. Change in I_{EE} vs Change in V_{EE}

F100K has a tighter AC window over the wide range of environmental conditions; thus, the system timing requirements are eased and maximum system clock rates are increased. At the sacrifice of AC performance, the small-signal input impedance was conservatively designed to be positive-real over the frequency range encountered by any circuit input. This provides adequate damping to insure AC stability within the system.

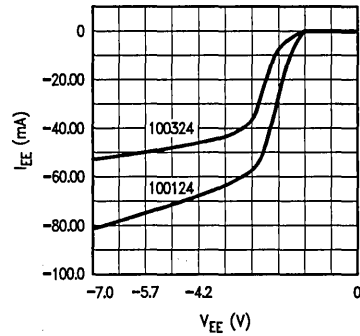
F100K 300 Series Design Philosophy

F100K 300 Series was designed to improve several performance parameters while still maintaining the speed and functionality requirements of the original F100K family. These new improvements enable 300 Series to be used in an even broader range of applications.

Most importantly, 300 Series products all meet F100K's optimized speeds and edge rates, while consulting up to 50% less power. These lower power designs, combined with the manufacturability of the FAST-LSI process (see Process Technology), enabled the 300 Series line to be reliably packaged in plastic leaded chip carrier (PCC) packages. A graph is shown comparing the power consumption of the F100124 and F100324 vs. supply voltage (Figure 1-10). In addition, 300 Series is designed with a more stable voltage reference network, providing a single set of DC specifications across a wider supply voltage range (-4.2V to -5.7V), easing the design of 300 Series into systems which use -5.2V power supplies. Also, 300 Series products have been designed to comply with all MIL-STD-883C requirements, including operation over the full military temperature range of -55°C to +125°C. Finally, electrostatic discharge (ESD) protection diodes have been added to both input and output circuitry, guaranteeing a minimum of 2000V ESD protection for all 300 Series products.

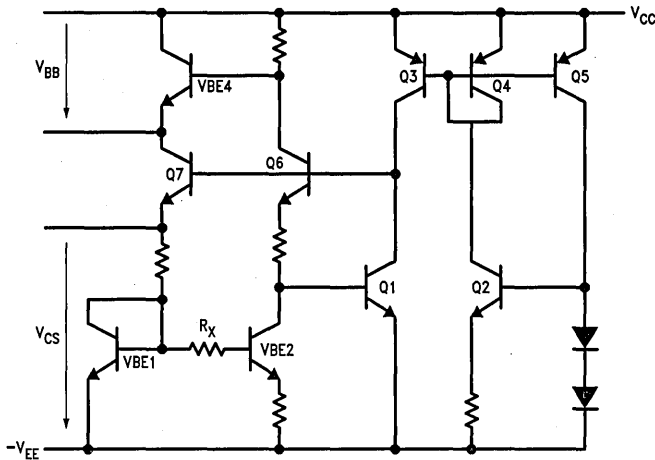


Several new circuits were utilized to achieve the performance improvements. The stabilized DC characteristics across the -4.2V to -5.7V power supply range are achieved through use of an improved reference network (Figure 1-11). This network replaces a resistor with a PNP transistor (Q_3). The collector-emitter voltage of Q_3 varies with V_{CC} , allowing the voltage at the base of Q_6 to remain constant as V_{CC} varies. This, in turn, stabilizes both V_{BB} and V_{CS} , so that as V_{EE} varies from -4.2V to -5.7V , V_{BB} varies no more than 15 mV – 20 mV . (Variation of V_{BB} in F100K 100 Series products over this same voltage range can be as much as 70 mV – 80 mV). The improved stability of 300 Series vs. V_{CC} is reflected in the single set of DC I/O specifications guaranteed across this wider voltage range. These specifications are identical to the F100K 100 Series specifications listed at -4.5V . As shown in Figure 1-12, they increase minimum noise margins guaranteed by 300 Series to 140 mV .



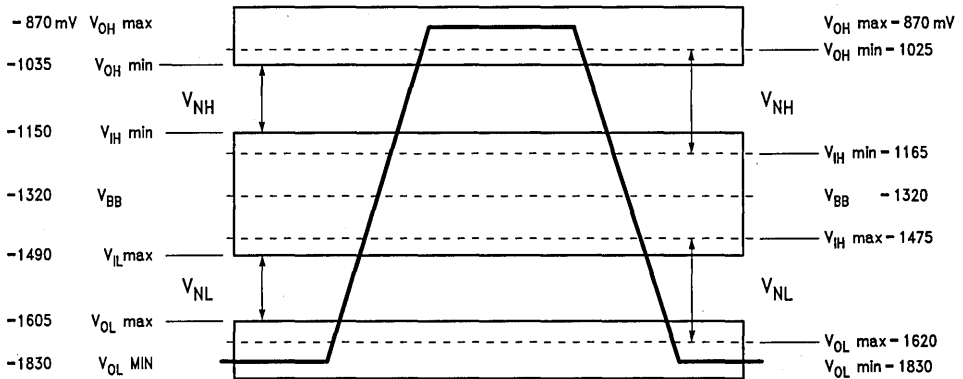
TL/F/9908-17

FIGURE 1-10. 300 Series Power Reduction



TL/F/9908-18

FIGURE 1-11. 300 Series Reference Network



TL/F/9908-19

100 Series Logic

$V_{NH} = 115\text{ mV}$
 $V_{NL} = 115\text{ mV}$
 $V_{EE} = -4.2\text{V}$ to -4.8V

$$V_{NH} = V_{OH\text{ Min}} - V_{IH\text{ Min}}$$

$$V_{NL} = V_{IL\text{ Max}} - V_{OL\text{ Max}}$$

300 Series Logic

$V_{NH} = 140\text{ mV}$
 $V_{NL} = 145\text{ mV}$
 $V_{EE} = -4.2\text{V}$ to -5.7V

FIGURE 1-12. 300 Series Noise Margins

All 300 Series products are designed to operate over the full military temperature range. To achieve this, internal voltage swings were increased to guardband against transistor saturation at temperature extremes. The faster transistor speeds offered by the FAST-LSI process compensated for the increased delays introduced by the wider voltage swings. Some of the more complex products utilize multi-level series gating to achieve higher levels of logic complexity at while reducing gate delays and power consumption. These products employ a Widlar Current Sink (Figure 1-13) to compensate for V_{BE} shifts at -55°C . In this circuit, the emitter resistor is removed from the current source (Q_1), providing more voltage headroom at lower temperatures, and avoiding saturation of the current source at -55°C . A second transistor (Q_2), driven by a voltage biased at $V_{CS} + V_{BE}$, provides V_{CS} at its emitter to drive the current source. This minimizes power by reducing the loading on the reference generator. A temperature-compensated current mirror (Q_3) is employed to control the base voltage of the current source so that it doesn't move regardless of V_{EE} or temperature changes.

Electrostatic discharge (ESD) protection diodes were added to all 300 Series designs (Figure 1-14) specifically in the circuit paths that were most prone to ESD damage on F100K 100 Series products: input-to- V_{CC} , input-to- V_{EE} , and output-to- V_{CC} . These diodes (D_1 , D_2 , and D_3) are utilized to shunt the current caused by an ESD voltage pulse away from either the input or output circuitry. Depending on the polarity of the ESD voltage, the diodes either become forward-biased, directing the current into the supply, or go into reverse breakdown, directing the current into the substrate. Either way, the ESD-caused current is shunted away from the input and output transistors, avoiding damage to the circuitry. The diodes are designed to be rugged enough to guarantee 2000V of ESD protection on all 300 Series products (they typically withstand up to 4000V). Even in providing this protection level, these diodes have a negligible impact on input capacitance. Addition of these diodes typically adds only tenths of picofarads to each product's input capacitance.

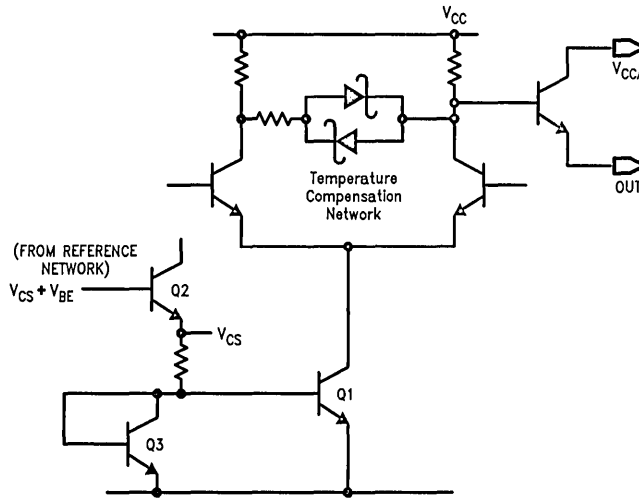


FIGURE 1-13. 300 Series Widlar Current Sink

TL/F/9908-20

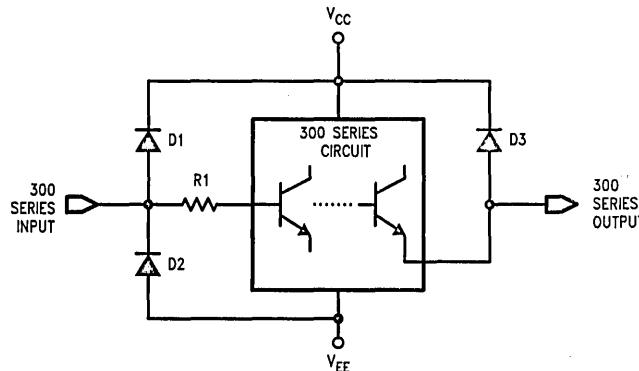


FIGURE 1-14. 300 Series ESD Protection Diodes

TL/F/9908-21

System Aspects

F100K provides high-density digital functions that outperform all other families on the market today. How does this increased circuit performance and higher on-chip density improve system performance?

Propagation delay and transition times vary (AC windows) when functions are operated at the extremes of the specified environmental ranges. With F100K, these variations are reduced and more predictable system timing is achieved. For synchronous machines and very high speed asynchronous systems, timing and its predictability are of utmost importance. Due to F100K constant supply current versus power supply voltage and because of nearly constant levels and thresholds with respect to temperature, voltage variations and gradients, speed skews are minimized.

Not only timing but also maximum system clock rate is affected by the tighter AC window. Thus, with F100K the system designer can use a higher speed value in his worst-case calculations. This can be translated into higher possible system clock rates. Therefore, a machine can perform at up to twice the frequency, solely due to the F100K compensation features. Noise immunity will be of utmost importance in next generation computers, since much of the noise generated within the system is inversely proportional to the switching transition time of the circuits. The F100K transition time is typically 0.7 ns as compared to 2.0 ns in slower ECL families and should therefore increase system crosstalk by the same ratio.

F100K combats the increased system noise by maintaining a virtually invariant noise immunity with variations and gradients in power supply voltage, ambient and junction temperatures. The variation in junction temperatures is much larger than in earlier computer systems because of the mixture of LSI and SSI functions on the same boards.

Features

F100K ECL logic components are designed to be used in high-speed, low-noise systems and offer significant advantages over other logic families. Some of the important features and advantages are summarized below.

Low Propagation Delay

F100K ECL features gate delays that are typically 0.75 ns (750 picoseconds) with counters, registers and flip-flops operating in the 400–500 MHz range. When compared to other logic families such as Schottky TTL or slower ECL families, system performance can be doubled or tripled. Tighter AC distribution helps system timing requirements and increases system clock rates.

Moderate Edge Rates

Because of the nature of current mode switching which uses differential comparison techniques and avoids transistor storage delays, rise times can be controlled by internal time constants without sacrificing throughput delays. Slower rise times minimize ringing and reflections on interconnection wiring and simplify physical design. The typical edge rate for F100K ECL is 1V/ns, only about 80% of the edge rate of Schottky TTL. It can be shown that for ECL circuits, the natural rise and fall times are approximately equal to the propagation delay. This relationship is considered optimum for use in high-speed systems.

Wired-OR Capability

ECL outputs can be wired together where wiring rules permit, to form the positive logic-OR function, thus achieving an extra level of gating at no parts count expense. Data bussing and party line operations are facilitated by this features.

Complementary Outputs

A majority of F100K ECL logic elements have complementary outputs, providing numerous opportunities for reduction of package count and power consumption when mechanizing logic equations. Further, the system incurs no extra penalty in time delay since the complementary ECL outputs switch simultaneously.

A significant advantage to complementary outputs is that, since both the true and complement logic functions are available, I_{CC} imbalance can be minimized either by using both outputs in the design or merely terminating unused outputs. In this way, the constant current characteristic of ECL is not compromised and power supply noise is minimized.

Low Output Impedance, High Current Capacity

As operating speeds are increased to achieve the higher performance levels demanded of digital systems, ordinary wiring begins to exhibit distributed parameter characteristics, as opposed to a lumped capacitance nature at low speeds.

Characteristic impedances of normal wiring and printed circuit interconnections generally fall in the 50 Ω to 250 Ω range. With these low impedance lines and fast transitions, the signals are attenuated by the voltage divider action between the circuit output impedance and the characteristic impedance of the interconnection.

Voltage mode circuits have a HIGH state output impedance of from 50 Ω to 150 Ω and thus exhibit an output *stepped* characteristic, first reaching about 50% of final value and later reaching the final value in another *step*. F100K ECL output impedances under 10 Ω insure a complete, full valued, signal into a transmission line. Also, F100K ECL outputs are specified to drive a 50 Ω load (some devices are specified to drive a 25 Ω load). Outputs are capable of supply 50 mA or more and can thus support the quiescent current required for passive terminations.

Convenient Data Transmission

The complementary high-current outputs of F100K ECL elements are well suited for driving twisted pair or other balanced lines in a differential mode, thereby enhancing field cancellation and minimizing crosstalk between subsystems.

High Common-Mode Noise Rejection

Differential line receivers provide common-mode noise rejection of 1V or more for induced and ground noise. Differential receiving requires less signal swing than single ended and thus allows more reliable interpretation of low signal swings.

Constant Supply Current

The supply current drain of F100K ECL elements is governed by one or more internal constant current sources supplying operating current for differential switches and level shifting networks. Since the current drain is the same regardless of the state of the switches, F100K ECL circuits present constant currents loads to power supplies (*see Complementary Outputs*).

Low Power Loss in Stray Capacitance

Energy is consumed each time a capacitor is charged or discharged so the energy loss rate, or power, goes up with switching frequency. Since the energy stored in a capacitor is proportional to the square of the voltage and F100K ECL signal swings are four to five times less than those of TTL, power loss in stray capacitance may be an order of magnitude less than that of TTL.

Low Noise Generation

In ECL systems, power supply lines are not subjected to the large current spikes common with TTL designs. Inherently, ECL is a constant current family without the totem-pole structures found in TTL circuits which generate the large current spikes. Since ECL voltage swings are much smaller than TTL, the current spikes caused by charging and discharging stray capacitances are much smaller with ECL than with TTL of comparable edge rates.

Low Crosstalk

Induced noise signals are proportional to signal swings and edge rates. The lower swing and slower edge rate of F100K ECL results in low levels of crosstalk.

System Benefits

The National F100K ECL Family offers improvements over other ECL families such as voltage and temperature compensation, higher integration levels, improved packaging, planned pinouts, lower propagation delay and more complementary outputs. These improvements offer measurable advantages to the design(er) of high-performance systems.

Easier Engineering

Designers have increased confidence that designs realized in F100K will operate with good margins over voltage and temperature variations in prototypes, production models and field installations. Less effort need be expended doing detailed voltage and temperature calculations and testing. With noncompensated ECL, noise margins cannot be guaranteed unless both the receiving and transmitting circuit operate at the same temperature and V_{EE} . This can cause a problem when attempting to transfer a breadboard or prototype system to production.

Since output swings and input thresholds remain almost constant over temperature and V_{EE} variations, complex control systems for power supply levels and more-than-adequate cooling are not necessary with F100K. This results in a more economical and better operating system.

Circuit Design

F100K ECL benefits from sound, well-engineered circuit designs. All input pins exhibit *positive/real* input impedance to eliminate system oscillations. Input buffering is used to reduce loads on lines which drive multiple internal gates.

High Performance

The regulation and control of DC and AC parameters achieved by F100K ECL assures that signal timing and propagation delays in critical paths are relatively insensitive to changes or gradients of temperature and supply voltage. Guardbands can be narrower, yet provide a higher degree of confidence due to the elimination of skew between output levels at one location and input threshold at another.

The consistency of response and security of noise margins permit operation at higher clock rates and thus increase system performance.

Easier Debugging

With F100K, debugging of systems can proceed more rapidly than with uncompensated ECL. When a cabinet or enclosure is opened for access in debugging, the resultant change in thermal conditions has almost no effect on F100K signal swings, propagation delays, edge rates or noise margins.

Flexibility

F100K is designed to operate at $-4.5V$ for reduced power dissipation. If compatibility with other ECL families is a requirement, F100K 300 Series guarantees specifications between $-4.2V$ and $-5.7V$ due to its improved voltage compensation features.

Fan-In/Fan-Out

All F100K ECL outputs are specified to drive 50Ω transmission lines; this makes them suitable for driving very-high fan-out loads. In addition, some F100K outputs are specified to drive 25Ω lines, which would be the case if a 50Ω party-line bus terminated at both ends were being driven.

System Design

F100K ECL was designed to be the ultimate standard packaged IC logic family. System design constraints were considered and the F100K family was designed for overall ease of system design and use while making the maximum use of the very fast propagation delay available.

Packaging

The initial package selected for the F100K family was a 24-pin Flatpak, 0.375 inches square, with leads on 50-mil centers, 6 leads per side. This package was chosen because its electrical characteristics minimized performance degradations of the circuit and its small footprint optimized board packing density. For customers who desire to use conventional through-hole assembly technology, the 24-pin ceramic dual in-line package is available as well. By utilizing the available F100K packages, and high chip complexities within the family, the user can achieve system densities two to three times higher than that possible with other ECL logic families.

In addition to the ceramic DIP and ceramic flatpak packages, all 300 Series products also offer a 28-pin plastic leaded chip carrier (PCC) package for low cost, high density surface mount assembly. This package is approximately 0.490 inches square, with J-bend leads on 50-mil centers, 7 leads per side. The leadframe has been designed with extra thermal paths which provide approximately $45^{\circ}C/Wt$ in air flow of 500 linear feet per minute.

For information on thermal resistance please see section on Power Distribution and Thermal considerations.

Using F100K ECL 300 Series in Military Applications

With the introduction of National's F100K ECL 300 Series comes the advent of F100K ECL in military applications. The special concerns addressed in the 300 Series design criteria enables this family to specify operation over the temperature range of $-55^{\circ}C$ to $+125^{\circ}C$, and to comply fully with the requirements of MIL-STD-883 Revision C.

As in the commercial world, with military systems becoming more complex, speed becomes a major consideration. Speeds which are pushing Schottky and CMOS technologies to their maximum performance limits, forcing designers to look to faster logic technologies. But speed, of course, is not the only consideration military designers have to contend with. Power consumption, package/function size, price, ESD susceptibility, radiation tolerance and operation in any of a number of harsh environments must be addressed by a military system designer, and all have been addressed in the design of the F100K 300 Series Family.

The relatively high speed-to-power product of the F100K ECL 300 Series Family allows these products to be used in a wide variety of applications. As systems begin to strain under the 30 MHz–40 MHz limits of some of the more conventional logic families, the 300 Series with its data rates exceeding 100 MHz, becomes a viable solution. The reduced power operation offered by the 300 Series product line eliminates the last barriers inhibiting the extensive usage of ECL in battery powered systems. Mixing F100K ECL 300 Series products with other logic families is also made easier with a variety of level translators and a wide operating voltage range of -4.2V to -5.7V .

The lower power and improved ESD protection will also enhance the overall reliability of these products. The lower power operation will by drawing less current, decrease the package temperature and increase the life expectancy of these products. The 2000V ESD protection helps eliminate the problem of "walking wounded" devices. Those devices which may be weakened by improper handling but not to a point where the damage could be detected. These "walking wounded" devices may eventually drift or even fail during operation, causing in some circumstances, a system failure. The high radiation tolerance of these products, a benefit inherent with the FAST-LSI process, enables these devices to withstand large doses of radiation such as those encountered in space applications.

The -4.2V to -5.7V V_{EE} operating voltage range could be perhaps the most significant feature of this family. One set of AC and DC electrical specifications over this wide voltage supply range means that you will be able to mix 300 Series products with other logic families operating over a much narrower voltage supply range, without requiring separate power supplies. Special care though, should still be taken when mixing F100K ECL 300 Series products with other logic families. These considerations are addressed in more detail in the F100K ECL Design Guide.

Among the many other benefits this family offers is full temperature compensation and high noise immunity. Both of these features are extremely important in the environments military systems are subjected to, or standards to which they must comply. The temperature compensation circuit of F100K ECL ensures stable DC performance over temperature changes in the external environment, as well as temperature fluctuations within a system, or even on one circuit board. The high noise immunity provides clean operation and few system hiccups due to noise, even when operating in a noisy environment.

Definitions of Symbols and Terms

AC SWITCHING PARAMETERS

f_{COUNT} (Count Frequency/Toggle Frequency/Operating Frequency): The maximum repetition rate at which clock pulses may be applied to sequential circuit. Above this frequency the device may cease to function.

t_{AA} (Address Access Time): 50% points of address input pulse to data output pulse.

t_{ACS} (Chip Select Access Time): 50% points of select pulse to data output pulse/leading edges.

t_{H} (Hold Time): The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its continued recognition.

t_{PLH} (Propagation Delay Time): The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} (Propagation Delay Time): The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{RCS} (Chip Select Recovery Time): Data output pulse/trailing edges.

t_{S} (Setup Time): The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the data to be recognized must be maintained at the input to ensure its recognition.

t_{S} (Release Time): The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which the master set or reset must be released (inactive) to ensure valid data is recognized.

t_{TLH} (Transition Time, LOW to HIGH): The time between two specified reference points on a waveform which is changing from LOW to HIGH.

t_{THL} (Transition Time, HIGH to LOW): The time between two specified reference points on a waveform which is changing from HIGH to LOW.

t_{PW} (Pulse Width): The time between 50 percent amplitude points on the leading and trailing edges of a pulse.

t_{PHZ} (Output Disable Time of a TRI-STATE® Output from High Level): The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} (Output Disable Time of a TRI-STATE Output from LOW Level): The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} (Output Enable Time of a TRI-STATE Output to a HIGH Level): The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

tpZL (Output Enable Time of a TRI-STATE Output to a LOW Level): The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW level.

ts, G-G (Skew, Gate to Gate): also referred to as **tOST (Output Skew Time):** the absolute value of the difference between the actual propagation delays for any two outputs of the same device. This applies to any combination of outputs switching LOW to HIGH and/or HIGH to LOW.

tOST (Output Skew Time): the absolute value of the difference between the actual propagation delays for any two outputs of the same device. This applies to any combination of outputs switching LOW to HIGH and/or HIGH to LOW.

tW (Write Pulse Width): 50% points of write enable input pulse.

tWHA (Address Hold Time): 50% points of address pulse to trailing edge of write enable pulse.

tWHCS (Chip Select Hold Time): 50% points of trailing edges of chip select pulse to write enable pulse.

tWHD (Data Hold Time after Write): 50% points of trailing edges of data input pulse to write enable pulse.

tWR (Write Recovery Time): 50% points of trailing edges of write enable pulse to data output pulse.

tWS (Write Disable Time): 50% points of leading edges of write enable pulse to data output pulse.

tWSA (Address Setup Time): 50% points of address pulse to leading edge of write enable pulse.

tWSCS (Chip Select Setup Time): 50% points of leading edges of chip select pulse to write enable pulse.

tWSD (Data Setup Time Prior to Write): 50% points of leading edges of data input pulse to write enable pulse.

CURRENTS

Positive current is defined as conventional current flow *into* a device lead. Negative current is defined as conventional current flow *out of* a device lead.

IEE (Power Supply Current): The current required by each device from the V_{EE} supply. This value represents only the internal current required by the specified device, and does not include the current required for loads or terminations.

ITTL (Supply Current): The current flowing into the V_{TTL} supply terminal of a circuit with the specified input conditions and the outputs open. When not specified, input conditions are chosen to guarantee worst-case operation.

I_{IH} (Input Current HIGH): The current flowing into a device lead with the specified V_{IH} applied to the input. This value represents the worst case DC input load that a device presents to a driving element.

I_{IL} (Input Current LOW): The current flowing into a device lead with the specified V_{IL} applied to the input.

IOH (Output HIGH Current): The current flowing out of the output when it is in the HIGH state. For a turned-off open-collector output with a specified HIGH output voltage applied, the I_{OH} is the leakage current.

IOL (Output LOW Current): The current flowing into an output when it is in the LOW state.

IOS (Output Short Circuit Current): The current flowing out of a HIGH-state output when that output is short circuited to ground (or other specified potential).

IOZH (Output OFF Current HIGH): The current flowing into a disable TRI-STATE output with a specified HIGH output voltage applied.

IOZL (Output OFF Current LOW): The current flowing out of a disabled TRI-STATE output with a specified LOW output voltage applied.

VOLTAGES

All voltage values are referenced to V_{CC} (or ground) which is the most positive potential in an ECL system.

V_{BB} (Bias Voltage): The internally generated reference voltage which is used to set the input and output threshold levels.

V_{CC} (Circuit Ground): This is the most positive potential in the ECL system and it is used as the reference level for other voltages.

V_{CCA} (Separate Circuit Ground): The circuit ground for the buffered current switch. Outside the package, the V_{CC} and V_{CCA} leads should be connected to the common V_{CC} distribution. Internally, the separation of V_{CC} and V_{CCA} insures that any change in load currents during switching does not cause a change in V_{CC} through the small but finite inductance of the V_{CCA} bond wire and package lead.

V_{CS} (Current Source Voltage): The internally generated potential used to control the level of the active current source.

V_{EE} (Power Supply Voltage): This potential is the system power supply voltage and it is the most negative potential in the system.

V_{EES} (Substrate V_{EE}): These pins (on the PCC package only) provide extra thermal conduction paths, therefore reducing θ_{JA} . These pins must be connected to the V_{EE} plane or not connected at all.

V_{TTL} Supply Voltage: The range of the TTL power supply voltage over which the device is guaranteed to operate within the specified limits.

V_{IH} (Input Voltage HIGH): The range of input voltages that represents a logic HIGH level in the system.

V_{IH} (Max): The most positive V_{IH} .

V_{IH} (Min): The most negative V_{IH} . This value represents the guaranteed input HIGH threshold for the device.

V_{IL} (Input Voltage LOW): The range of input voltages that represents a logic LOW level in the system.

V_{IL} (Max): The most positive V_{IL} . This value represents the guaranteed input LOW threshold for the device.

V_{IL} (Min): The most negative V_{IL} .

V_{OH} (Output Voltage HIGH): The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a HIGH level at the output.

V_{OH} (Max): The most positive V_{OH} under the specified input and loading conditions.

V_{OH} (Min): The most negative V_{OH} under the specified input and loading conditions.

V_{OHC}: The output HIGH corner point or guaranteed HIGH threshold voltage with the inputs set to their respective threshold levels.

V_{OL} (Output Voltage LOW): The range of voltages at an output terminal with the specified output loading and with the inputs conditioned to establish a LOW level at the output.

V_{OL} (Max): The most positive V_{OL} under the specified input and loading conditions.

V_{OL} (Min): The most negative V_{OL} under the specified input and loading conditions.

V_{OLC} : The output LOW corner point or guaranteed LOW threshold voltage with the inputs set to their respective threshold levels.

V_{NH} (HIGH Level Noise Margin): Noise margin between the output HIGH level of a driving circuit and the input HIGH threshold level of its driven load. A conservative value for V_{NH} is the difference between V_{OHC} and V_{IH} (Min).

V_{NL} (LOW Level Noise Margin): Noise margin between the output LOW level of a driving circuit and the input LOW threshold level of its driven load. A conservative value for V_{NL} is the difference between V_{IL} (Max) and V_{OLC} .

References

1. H.H. Muller, W.K. Owens, and P.W.J. Verhofstadt, "Fully Compensated Emitter-Coupled Logic: Eliminating the Drawbacks of Conventional ECL", *IEEE Journal of Solid-State Circuits*, October 1973, pp. 362-367.
2. R.R. Marley, "On-Chip Temperature Compensation for ECL", *Electronic Products*, March 1, 1971.
3. V.A. Dhaka, J.E. Muschinske, and W.K. Owens, "Subnanosecond Emitter-Coupled Logic Gate Circuit Using Isoplanar II", *IEEE Journal of Solid-State Circuits*, October 1973, pp. 368-372.
4. R.J. Widlar, "New Developments in IC Voltage Regulators", *ISSCC Digital Technical Papers*, February 1970, pp. 157-159.
5. W.K. Owens, "Temperature Compensated Voltage Regulator Having Beta Compensating Means", United States Patent, No. 3,731,648, December 25, 1973.



Section 2
F100K 300 Series
Datasheets



Section 2 Contents

| | |
|--|-------|
| F100301 Low Power Triple 5-Input OR/NOR Gate | 2-3 |
| F100302 Low Power Quint 2-Input OR/NOR Gate | 2-8 |
| F100304 Low Power Quint AND/NAND Gate | 2-13 |
| F100307 Low Power Quint Exclusive OR/NOR Gate | 2-17 |
| F100311 Low Skew 9-Bit Clock Driver | 2-21 |
| F100313 Low Power Quad Driver | 2-22 |
| F100314 Low Power Quint Differential Line Receiver | 2-27 |
| F100321 Low Power 9-Bit Inverter | 2-28 |
| F100322 Low Power 9-Bit Buffer | 2-34 |
| F100324 Low Power Hex TTL-to-ECL Translator | 2-38 |
| F100325 Low Power Hex ECL-to-TTL Translator | 2-43 |
| F100328 Low Power Octal ECL/TTL Bidirectional Translator with Latch | 2-50 |
| F100329 Low Power Octal ECL/TTL Bidirectional Translator with Register | 2-51 |
| F100331 Low Power Triple D Flip-Flop | 2-52 |
| F100336 Low Power 4-Stage Counter/Shift Register | 2-53 |
| F100341 Low Power 8-Bit Shift Register | 2-68 |
| F100343 Low Power Octal Latch | 2-76 |
| F100344 Low Power Octal Latch with Cutoff Drivers | 2-83 |
| F100350 Low Power Hex D Latch | 2-90 |
| F100351 Low Power Hex D Flip-Flop | 2-91 |
| F100352 Low Power Octal Buffer with Cutoff Drivers | 2-98 |
| F100353 Low Power Octal Register | 2-105 |
| F100354 Low Power Octal Register with Cutoff Drivers | 2-112 |
| F100355 Low Power Quad Multiplexer/Latch | 2-119 |
| F100360 Low Power Dual Parity Checker/Generator | 2-128 |
| F100363 Low Power Dual 8-Input Multiplexer | 2-135 |
| F100364 Low Power 16-Input Multiplexer | 2-141 |
| F100370 Low Power Universal Demultiplexer/Decoder | 2-142 |
| F100371 Low Power Triple 4-Input Multiplexer | 2-143 |
| F100393 Low Power 9-Bit ECL-to-TTL Translator with Latch | 2-144 |
| F100395 Low Power 9-Bit ECL-to-TTL Translator with Register | 2-145 |

F100301

Low Power Triple 5-Input OR/NOR Gate

General Description

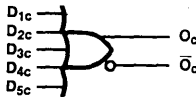
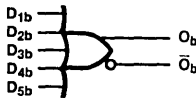
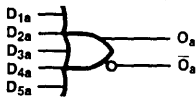
The F100301 is a monolithic triple 5-input OR/NOR gate. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 23% power reduction of the F100101
- 2000V ESD protection
- Pin/function compatible with F100101
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

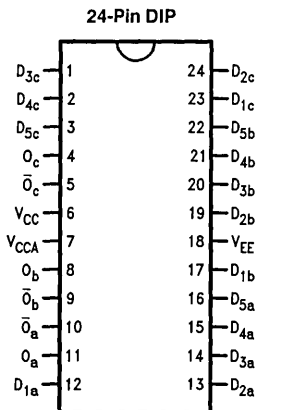
Logic Symbol



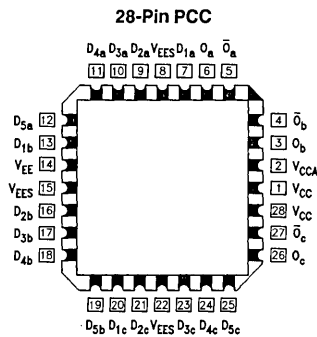
| Pin Names | Description |
|---|----------------------------|
| D _{na} , D _{nb} , D _{nc} | Data Inputs |
| O _a , O _b , O _c | Data Outputs |
| \bar{O}_a , \bar{O}_b , \bar{O}_c | Complementary Data Outputs |

TL/F/10579-1

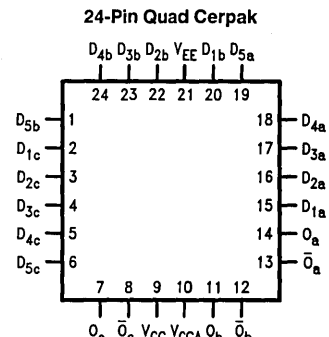
Connection Diagrams



TL/F/10579-2



TL/F/10579-4



TL/F/10579-3

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------------|----------------------|-------|-------|-------|-------|---|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH(Max)} or V _{IL(Min)} Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | |
| V _{OHc} | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH(Min)} or V _{IL(Max)} Loading with 50Ω to -2.0V |
| V _{OLc} | Output LOW Voltage | | | -1610 | mV | |
| V _{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs |
| V _{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL(Min)} |
| I _{IH} | Input HIGH Current | | | 240 | μA | V _{IN} = V _{IH(Max)} |
| I _{EE} | Power Supply Current | -29 | -17 | -15 | mA | Inputs Open |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND

| Symbol | Parameter | T _C = 0°C | | T _C = +25°C | | T _C = +85°C | | Units | Conditions |
|--------------------------------------|---|----------------------|------|------------------------|------|------------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output | 0.50 | 1.10 | 0.50 | 1.15 | 0.50 | 1.20 | ns | Figures 1 and 2 (Note 1) |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 1.20 | 0.40 | 1.20 | 0.40 | 1.20 | ns | Figures 1 and 2 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Recommended Operating Conditions

| | |
|------------------------------------|-----------------|
| Case Temperature (T _C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V _{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version (Continued)**PCC and Cerpak AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.50 | 1.00 | 0.50 | 1.05 | 0.50 | 1.10 | ns | Figures 1 and 2 (Note 2) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 1.10 | 0.40 | 1.10 | 0.40 | 1.10 | ns | Figures 1 and 2 |
| $t_{S, G-G}$ | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.**Note 2:** The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.**Military Version—Preliminary****DC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|----------------------|-------|-------|---------|---------------------------------|---|---------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH(Max)}$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH(Min)}$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH(Min)}$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH(Min)}$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL(Min)}$ | 1, 2, 3 | |
| I_{IH} | Input HIGH Current | | 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | 1, 2, 3 | |
| | | | 340 | μA | $-55^\circ C$ | | | |
| I_{EE} | Power Supply Current | -32 | -12 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.**Note 2:** Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.**Note 4:** Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics**

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ\text{C}$ | | $T_C = +25^\circ\text{C}$ | | $T_C = +125^\circ\text{C}$ | | Units | Conditions | Notes |
|------------------------|---|---------------------------|------|---------------------------|------|----------------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.40 | 1.70 | 0.40 | 1.50 | 0.40 | 1.80 | ns | Figures 1 and 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.20 | 0.30 | 1.20 | 0.30 | 1.20 | ns | | 4 |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ\text{C}$ | | $T_C = +25^\circ\text{C}$ | | $T_C = +125^\circ\text{C}$ | | Units | Conditions | Notes |
|------------------------|---|---------------------------|------|---------------------------|------|----------------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.40 | 1.50 | 0.40 | 1.30 | 0.40 | 1.60 | ns | Figures 1 and 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.10 | 0.30 | 1.10 | 0.30 | 1.10 | ns | | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

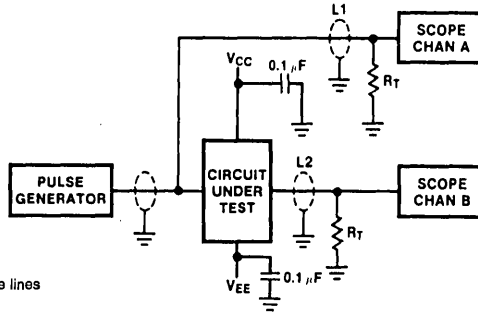
Note 2: Screen tested 100% on each device at $+25^\circ\text{C}$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ\text{C}$, Subgroup A9, and at $+125^\circ\text{C}$ and -55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ\text{C}$, $+125^\circ\text{C}$, and -55°C temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Test Circuitry

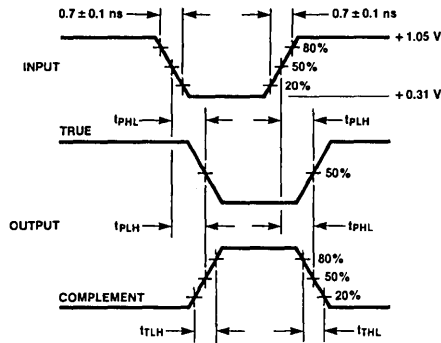


Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance $\leq 3 pF$

TL/F/10579-5

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10579-6

FIGURE 2. Propagation Delay and Transition Times



F100302

Low Power Quint 2-Input OR/NOR Gate

General Description

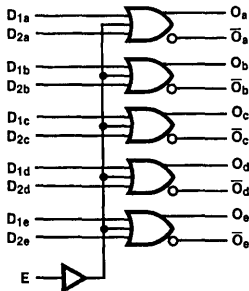
The F100302 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 43% power reduction of the F100102
- 2000V ESD protection
- Pin/function compatible with F100102
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

Logic Symbol



TL/F/10580-1

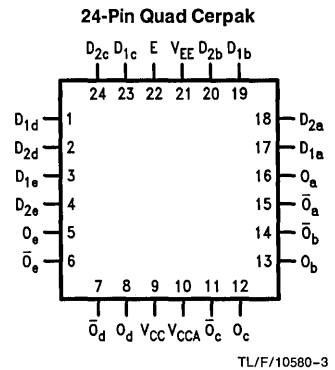
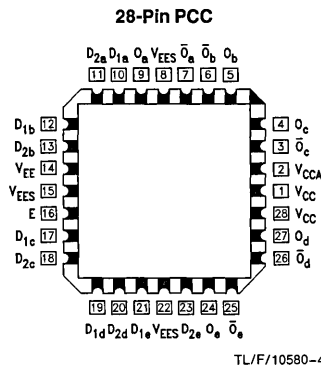
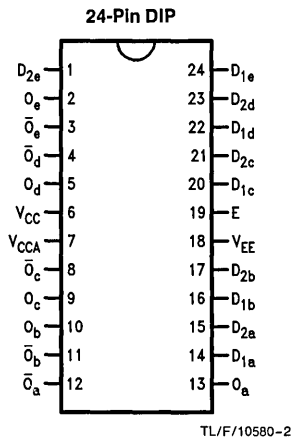
| Pin Names | Description |
|----------------------------------|----------------------------|
| D _{na} -D _{ne} | Data Inputs |
| E | Enable Input |
| O _a -O _e | Data Outputs |
| O _a -O _e | Complementary Data Outputs |

Truth Table

| D _{1X} | D _{2X} | E | O _X | O _X |
|-----------------|-----------------|---|----------------|----------------|
| L | L | L | L | H |
| L | L | H | H | L |
| L | H | L | H | L |
| L | H | H | H | L |
| H | L | L | H | L |
| H | L | H | H | L |
| H | H | L | H | L |
| H | H | H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level

Connection Diagrams



Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|-----------------------------|-----------------|
| Case Temperature (T_C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V_{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|----------------------|-------|-------|-------|-------|---|---------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(Min)}$ | |
| I_{IH} | Input HIGH Current | | | 240 | μA | $V_{IN} = V_{IH(Max)}$ | |
| I_{EE} | Power Supply Current | -45 | -36 | -20 | mA | Inputs Open | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0°C$ | | $T_C = +25°C$ | | $T_C = +85°C$ | | Units | Conditions |
|-----------|--|-------------|------|---------------|------|---------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} | Propagation Delay Data to Output | 0.50 | 1.15 | 0.50 | 1.15 | 0.50 | 1.25 | ns | Figures 1 and 2 (Note 1) |
| t_{PHL} | | | | | | | | | |
| t_{PLH} | Propagation Delay Enable to Output | 1.10 | 1.90 | 1.10 | 1.90 | 1.20 | 2.00 | ns | |
| t_{PHL} | | | | | | | | | |
| t_{TLH} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 1.20 | 0.40 | 1.20 | 0.40 | 1.20 | ns | Figures 1 and 2 |
| t_{THL} | | | | | | | | | |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Commercial Version (Continued)**PCC and Cerpak AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.50 | 1.05 | 0.50 | 1.05 | 0.50 | 1.15 | ns | Figures 1 and 2 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 1.10 | 1.80 | 1.10 | 1.80 | 1.20 | 1.90 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 1.10 | 0.40 | 1.10 | 0.40 | 1.10 | ns | Figures 1 and 2 |
| $t_{S,G-G}$ | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.**Note 2:** The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.**Military Version—Preliminary****DC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$ (Note 3)

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|----------------------|-------|-------|---------|---------------------------------|---|---------------------------------------|------------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH(Max)}$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH(Max)}$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH(Max)}$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH(Max)}$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | | 1, 2, 3, 4 |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | | 1, 2, 3, 4 |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | | 1, 2, 3 |
| I_{IH} | Input HIGH Current | | 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ | | 1, 2, 3 |
| | | | 340 | μA | $-55^\circ C$ | $V_{IN} = V_{IL} (Min)$ | | |
| I_{EE} | Power Supply Current | -48 | -17 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.**Note 2:** Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.**Note 4:** Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.30 | 1.80 | 0.40 | 1.50 | 0.40 | 1.70 | ns | Figures 1 and 2 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.60 | 2.60 | 0.80 | 2.30 | 0.80 | 2.80 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.20 | 0.30 | 1.20 | 0.30 | 1.20 | ns | | 4 |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.30 | 1.60 | 0.40 | 1.30 | 0.40 | 1.50 | ns | Figures 1 and 2 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.60 | 2.40 | 0.80 | 2.10 | 0.80 | 2.60 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.10 | 0.30 | 1.10 | 0.30 | 1.10 | ns | | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

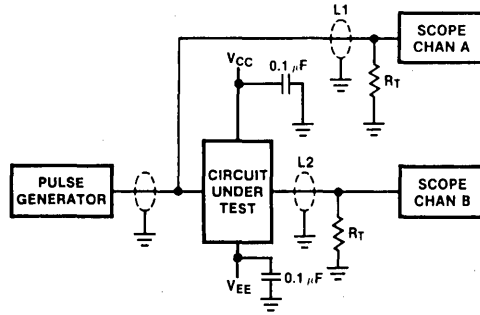
Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 100 ps with multiple outputs switching.

Test Circuitry



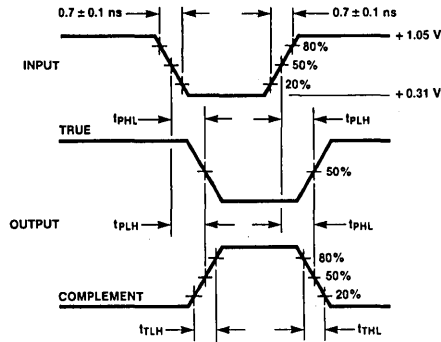
TL/F/10580-5

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10580-6

FIGURE 2. Propagation Delay and Transition Times

F100304

Low Power Quint AND/NAND Gate

General Description

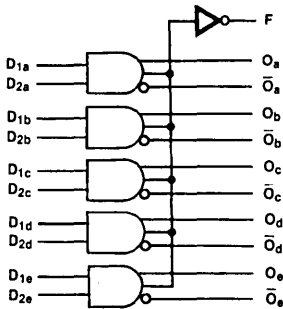
The F100304 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

Features

- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with F100104
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

Logic Symbol



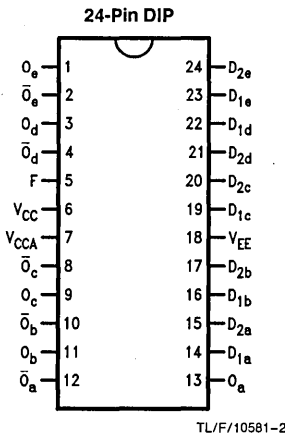
TL/F/10581-1

Logic Equation

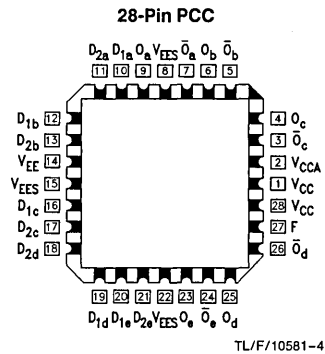
$$F = \overline{(D_{1a} \cdot D_{2a})} + (D_{1b} \cdot D_{2b}) + D_{1c} \cdot D_{2c} + (D_{1d} \cdot D_{2d}) + (D_{1e} \cdot D_{2e}).$$

| Pin Names | Description |
|-------------------------------------|----------------------------|
| D _{na} -D _{ne} | Data Inputs |
| F | Function Output |
| O _a -O _e | Data Outputs |
| \overline{O}_a - \overline{O}_e | Complementary Data Outputs |

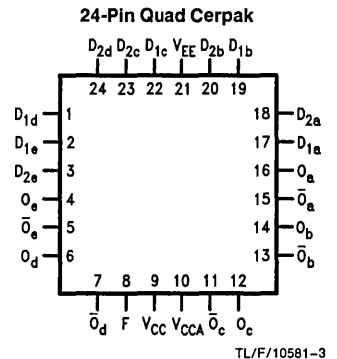
Connection Diagrams



TL/F/10581-2



TL/F/10581-4



TL/F/10581-3

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|-----------------------------|-----------------|
| Case Temperature (T_C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V_{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|--|-------|-------|------------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |
| I_{IH} | Input High Current D _{2a} -D _{2e} D _{1a} -D _{1e} | | | 250 350 | μA | $V_{IN} = V_{IH}(\text{Max})$ | |
| I_{EE} | Power Supply Current | -69 | -43 | -30 | mA | Inputs open | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0°C$ | | $T_C = +25°C$ | | $T_C = +85°C$ | | Units | Conditions |
|------------------------|---|-------------|------|---------------|------|---------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D _{na} -D _{ne} to O, \bar{O} | 0.40 | 1.75 | 0.40 | 1.65 | 0.40 | 1.75 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.00 | 2.60 | 1.00 | 2.60 | 1.15 | 3.20 | ns | |
| t_{TLH} t_{TFL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.20 | 0.35 | 1.20 | 0.35 | 1.20 | ns | |

Commercial Version (Continued)**PCC and Cerpak AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{ne}$ to O, \bar{O} | 0.40 | 1.55 | 0.40 | 1.45 | 0.40 | 1.55 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.00 | 2.40 | 1.00 | 2.40 | 1.15 | 3.00 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.15 | 0.35 | 1.10 | ns | |
| $t_{S,G-G}$ | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version—Preliminary**DC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|--|-------|------------|---------|---------------------------------|--|------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL}(\text{Min})$ | 1, 2, 3 | |
| I_{IH} | Input High Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$ | | 250 350 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH}(\text{Max})$ | 1, 2, 3 | |
| | $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$ | | 350 500 | μA | $-55^\circ C$ | | | |
| I_{EE} | Power Supply Current | -75 | -25 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups, 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{ne}$ to O, \bar{O} | 0.30 | 1.90 | 0.40 | 1.80 | 0.30 | 2.30 | ns | Figures 1 and 2 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 0.80 | 2.90 | 0.90 | 2.80 | 0.90 | 3.40 | ns | | 4 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.20 | 1.80 | 0.30 | 1.60 | 0.20 | 2.00 | ns | | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{ne}$ to O, \bar{O} | 0.30 | 1.95 | 0.30 | 1.85 | 0.30 | 1.95 | ns | Figures 1 and 2 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 0.90 | 2.80 | 0.90 | 2.80 | 1.05 | 3.40 | ns | | 4 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | | |

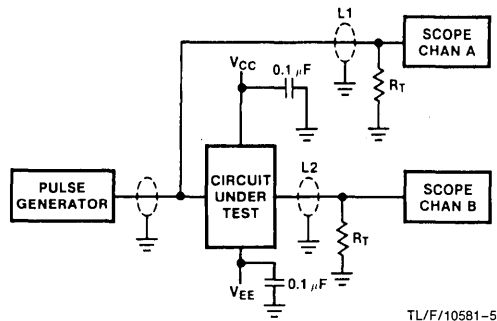
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Test Circuitry



Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

Switching Waveforms

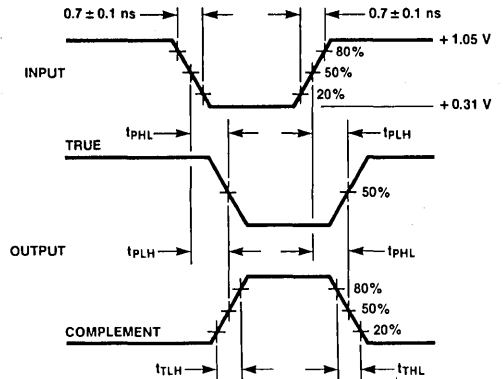


FIGURE 2. Propagation Delay and Transition Times

F100307

Low Power Quint Exclusive OR/NOR Gate

General Description

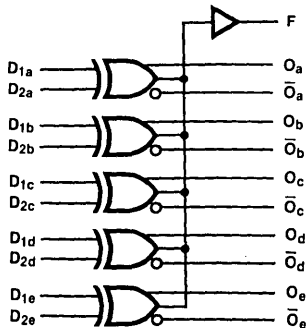
The F100307 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs. All inputs have 50 kΩ pull-down resistors.

Features

- Low Power Operation
- 2000V ESD protection
- Pin/function compatible with F100107
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

Logic Symbol



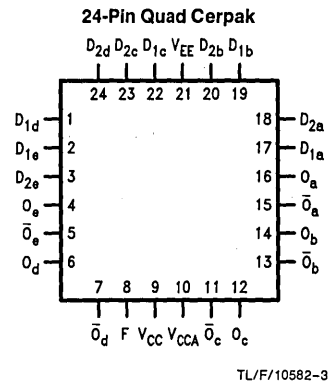
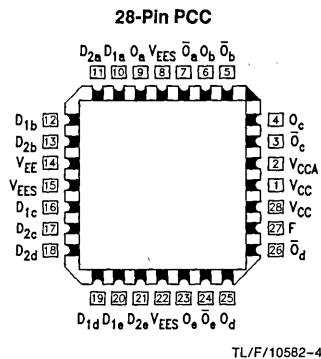
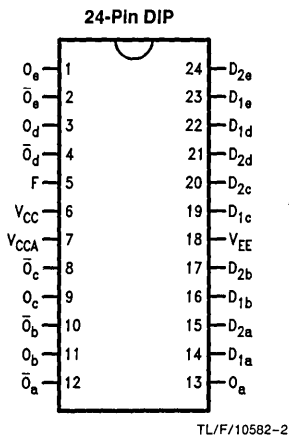
TL/F/10582-1

Logic Equation

$$F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$$

| Pin Names | Description |
|-----------------------|----------------------------|
| $D_{na}-D_{ne}$ | Data Inputs |
| F | Function Output |
| O_a-O_e | Data Outputs |
| $\bar{O}_a-\bar{O}_e$ | Complementary Data Outputs |

Connection Diagrams



Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|-----------------------------|-----------------|
| Case Temperature (T_C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V_{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|--|-------|-------|------------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ | |
| I_{IH} | Input HIGH Current D _{2a} -D _{2e} D _{1a} -D _{1e} | | | 250 350 | μA | $V_{IN} = V_{IH} (Max)$ | |
| I_{EE} | Power Supply Current | -69 | -43 | -30 | mA | Inputs Open | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D _{2a} -D _{2e} to O, \bar{O} | 0.55 | 1.90 | 0.55 | 1.80 | 0.55 | 1.90 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay D _{1a} -D _{1e} to O, \bar{O} | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.15 | 2.75 | 1.15 | 2.75 | 1.15 | 3.00 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.20 | 0.35 | 1.20 | 0.35 | 1.20 | ns | |

Commercial Version (Continued)**PCC and Cerpak AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O} | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O} | 0.55 | 1.50 | 0.55 | 1.40 | 0.55 | 1.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.15 | 2.55 | 1.15 | 2.55 | 1.15 | 2.80 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | |
| $t_{S,G-G}$ | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.**Military Version—Preliminary****DC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|--|-------|-------|---------|------------------------------------|--|---------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}$ (Max) or V_{IL} (Min) | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}$ (Min) or V_{IL} (Max) | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}$ (Min) or V_{IL} (Max) | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}$ (Min) or V_{IL} (Max) | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min) | 1, 2, 3 | |
| I_{IH} | Input High Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$ | | 250 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max) | 1, 2, 3 | |
| | | | 350 | μA | $-55^\circ C$ | | | |
| I_{EE} | Power Supply Current | | 350 | μA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3 | |
| | | -63 | -30 | mA | | | | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.**Note 2:** Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.**Note 3:** Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.**Note 4:** Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O} | 0.45 | 2.10 | 0.45 | 2.00 | 0.45 | 2.10 | ns | Figures 1 and 2 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O} | 0.45 | 1.90 | 0.45 | 1.80 | 0.45 | 1.90 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.05 | 2.95 | 1.05 | 2.95 | 1.05 | 3.20 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.20 | 0.35 | 1.20 | 0.35 | 1.20 | ns | | 4 |

Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O} | 0.45 | 2.10 | 0.45 | 2.00 | 0.45 | 2.10 | ns | Figures 1 and 2 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O} | 0.45 | 1.90 | 0.45 | 1.80 | 0.45 | 1.90 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.05 | 2.95 | 1.05 | 2.95 | 1.05 | 3.20 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | | 4 |

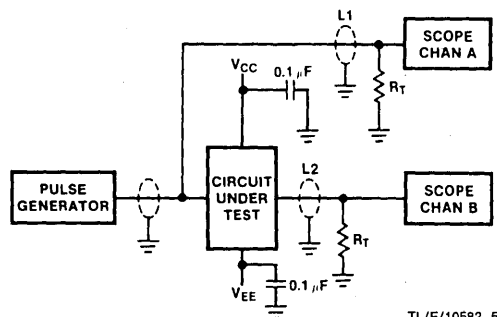
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Test Circuitry



Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = equal length 50 Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

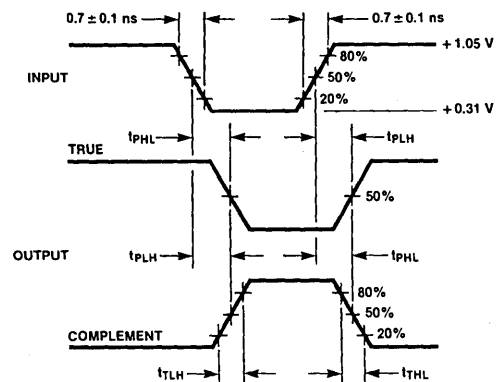
All unused outputs are loaded with 50 Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

TL/F/10582-5

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10582-6

FIGURE 2. Propagation Delay and Transition Times

F100311

Low Skew 1:9 Differential Clock Driver

General Description

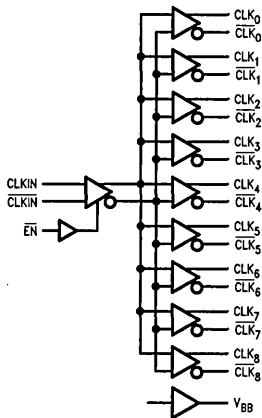
The F100311 contains nine low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input (CLKIN, $\overline{\text{CLKIN}}$). If a single-ended input is desired, the V_{BB} output pin may be used to drive the remaining input line. A HIGH on the enable pin ($\overline{\text{EN}}$) will force a LOW on all of the CLK_n outputs and a HIGH on all of the $\overline{\text{CLK}}_n$ output pins. A LOW on $\overline{\text{EN}}$ will return control of the $\text{CLK}_n/\overline{\text{CLK}}_n$ outputs back to the $\text{CLKIN}/\overline{\text{CLKIN}}$ inputs.

The skew specifications on the F100311 are fully tested and guaranteed.

Features

- Low output to output skew (≤ 75 ps)
- 2000V ESD protection
- 1:9 low skew clock driver
- Differential inputs and outputs

Logic Symbol



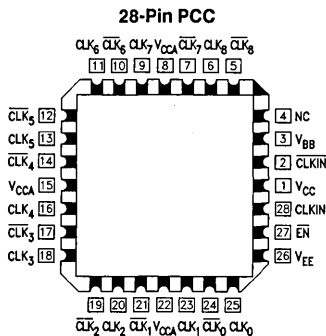
TL/F/10648-1

| Pin Names | Description |
|--|----------------------------|
| CLKIN, $\overline{\text{CLKIN}}$ | Differential Clock Inputs |
| $\overline{\text{EN}}$ | Enable |
| CLK_{0-8} , $\overline{\text{CLK}}_{0-8}$ | Differential Clock Outputs |
| V_{BB} | V_{BB} Output |
| NC | No Connect |

Truth Table

| CLKIN | $\overline{\text{CLKIN}}$ | $\overline{\text{EN}}$ | CLK_n | $\overline{\text{CLK}}_n$ |
|-------|---------------------------|------------------------|----------------|---------------------------|
| L | H | L | L | H |
| H | L | L | H | L |
| X | X | H | L | H |

Connection Diagram



TL/F/10648-2



F100313 Low Power Quad Driver

General Description

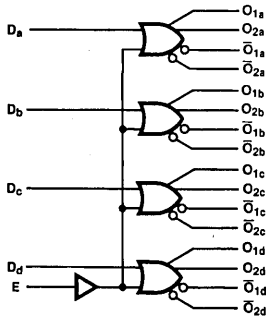
The F100313 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features

- 50% power reduction of the F100113
- 2000V ESD protection
- Pin/function compatible with F100113 and F100112
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

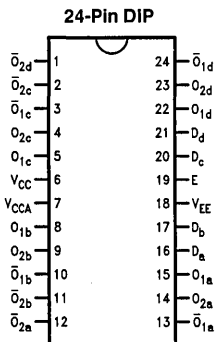
Logic Symbol



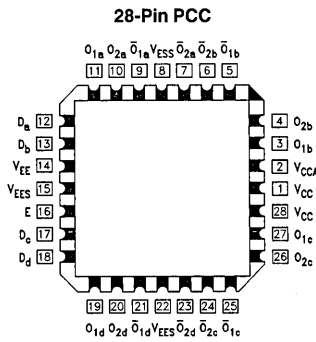
TL/F/10249-3

| Pin Names | Description |
|---|----------------------------|
| D _a -D _d | Data Inputs |
| E | Enable Input |
| O _{na} -O _{nd} | Data Outputs |
| O _{na} -bar-O _{nd} -bar | Complementary Data Outputs |

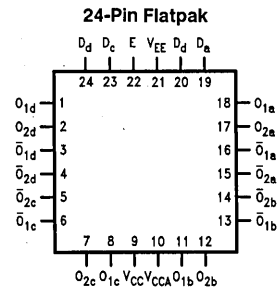
Connection Diagrams



TL/F/10249-1



TL/F/10249-4



TL/F/10249-2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG}) -65°C to +150°C

Maximum Junction Temperature (T_J)

Ceramic +175°C

Plastic +150°C

V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V

Input Voltage (DC) V_{EE} to +0.5V

Output Current (DC Output HIGH) -50 mA

ESD (Note 2) ≥2000V

Recommended Operating Conditions

Case Temperature (T_C)

Commercial 0°C to +85°C

Military -55°C to +125°C

Supply Voltage (V_{EE})

Commercial -5.7V to -4.2V

Military -5.7V to -4.2V

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------------|----------------------|-------|-------|------------|-------|---|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | | |
| V _{OHC} | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs |
| V _{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) |
| I _{IH} | Input HIGH Current | | | 350 240 | μA | V _{IN} = V _{IH} (Max) Data Enable |
| I _{EE} | Power Supply Current | -59 | | -29 | mA | Inputs Open |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND

| Symbol | Parameter | T _C = 0°C | | T _C = +25°C | | T _C = +85°C | | Units | Conditions |
|--------------------------------------|---|----------------------|------|------------------------|------|------------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output | 0.55 | 1.30 | 0.55 | 1.30 | 0.55 | 1.40 | ns | Figures 1 and 2 (Note 1) |
| t _{PLH} t _{PHL} | Propagation Delay Enable to Output | 0.80 | 1.80 | 0.80 | 1.80 | 0.80 | 1.90 | ns | |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.30 | 0.45 | 1.30 | ns | Figures 1 and 2 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 150 ps with multiple outputs switching.

Commercial Version (Continued)**PCC and Cerpak AC Electrical Characteristics**

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.55 | 1.20 | 0.55 | 1.20 | 0.55 | 1.30 | ns | Figures 1 and 2 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.80 | 1.70 | 0.80 | 1.70 | 0.80 | 1.80 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.30 | 0.45 | 1.30 | ns | Figures 1 and 2 |
| $t_{s, G-G}$ | Skew, Gate to Gate | TBD | | TBD | | TBD | | ns | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 150 ps with multiple outputs switching.

Military Version — Preliminary**DC Electrical Characteristics**

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ C \text{ to } +125^\circ C$$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|----------------------|-------|------------|---------|---------------------------------|--|---------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL}(\text{Min})$ | 1, 2, 3 | |
| I_{IH} | Input HIGH Current | | 350 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH}(\text{Max})$ | 1, 2, 3 | |
| | Data Enable | | 500 340 | μA | $-55^\circ C$ | | | |
| I_{EE} | Power Supply Current | -65 | -20 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Switching Waveforms

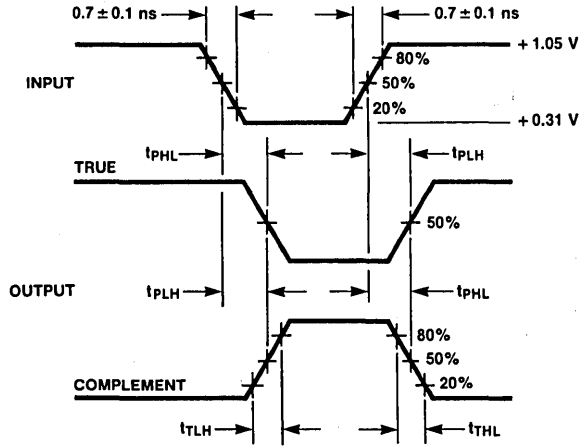


FIGURE 2. Propagation Delay and Transition Times

TL/F/10249-6

F100314

Low Power Quint Differential Line Receiver

General Description

The F100314 is a monolithic quint differential line receiver with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single-ended reception. When used in single-ended operation the apparent input threshold of the true inputs is 25 mV to 30 mV higher (positive) than the threshold of the complementary inputs. Unlike other F100K ECL devices, the inputs do not have input pull-down resistors.

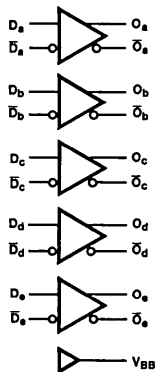
Active current sources provide common-mode rejection of 1.0V in either the positive or negative direction. A defined

output state exists if both inverting and non-inverting inputs are at the same potential between V_{EE} and V_{CC} . The defined state is logic HIGH on the \bar{O}_a - \bar{O}_e outputs.

Features

- 35% power reduction of the F100114
- 2000V ESD protection
- Pin/function compatible with F100114
- Voltage compensated operating range = -4.2V to -5.7V

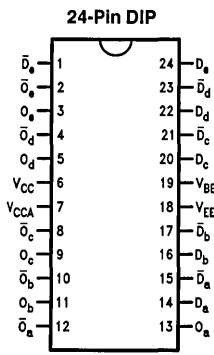
Logic Symbol



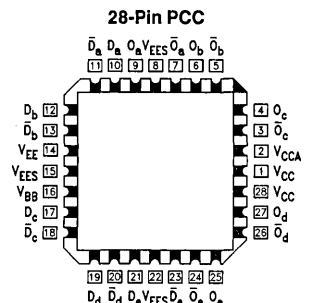
TL/F/10260-1

| Pin Names | Description |
|---------------------------|----------------------------|
| D_a - D_e | Data Inputs |
| \bar{D}_a - \bar{D}_e | Inverting Data Inputs |
| O_a - O_e | Data Outputs |
| \bar{O}_a - \bar{O}_e | Complementary Data Outputs |

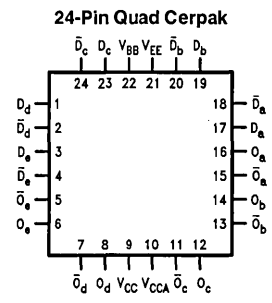
Connection Diagrams



TL/F/10260-2



TL/F/10260-4



TL/F/10260-3



F100321

Low Power 9-Bit Inverter

General Description

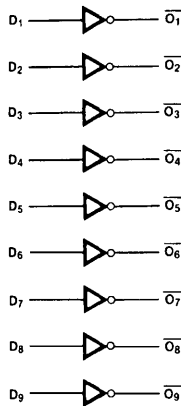
The F100321 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors.

Features

- 30% power reduction of the F100121
- 2000V ESD protection
- Pin/function compatible with F100121
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

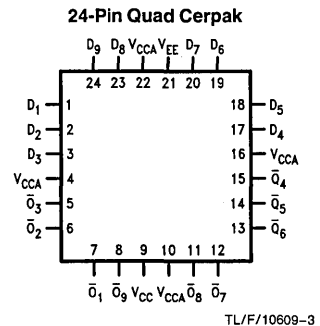
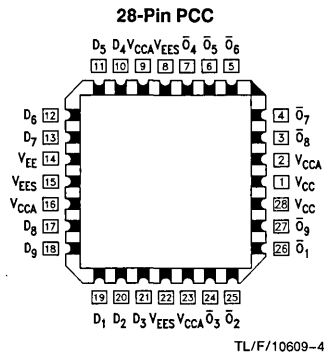
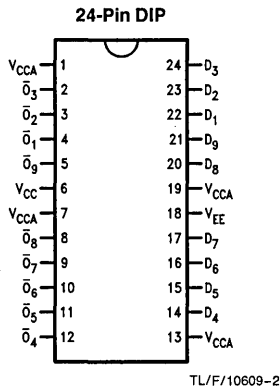
Logic Symbol



| Pin Names | Description |
|---------------------------|--------------|
| D_1 - D_9 | Data Inputs |
| \bar{O}_1 - \bar{O}_9 | Data Outputs |

TL/F/10609-1

Connection Diagrams



Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|-----------------------------|-----------------|
| Case Temperature (T_C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V_{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|----------------------|-------|-------|-------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH}$ (Max) or V_{IL} (Min) | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}$ (Min) or V_{IL} (Max) | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}$ (Min) | |
| I_{IH} | Input HIGH Current | | | 240 | μA | $V_{IN} = V_{IH}$ (Max) | |
| I_{EE} | Power Supply Current | -65 | | -30 | mA | Inputs Open | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.45 | 0.45 | 1.45 | 0.45 | 1.55 | ns | Figures 1 and 2 (Note 1) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.20 | 0.35 | 1.20 | 0.35 | 1.20 | ns | Figures 1 and 2 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

PCC and Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.25 | 0.45 | 1.25 | 0.45 | 1.35 | ns | Figures 1 and 2 (Note 2) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | Figures 1 and 2 |
| $t_{s,G-G}$ | Skew, Gate to Gate | | TBD | | TBD | | TBD | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Military Version — Preliminary**DC Electrical Characteristics**
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | | | | |
|-----------|----------------------|-------|-------|---------|---------------------------------|--|------------------------------------|---------|--|------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 | | | |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | | | | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 | | | |
| | | -1085 | | mV | $-55^\circ C$ | | | | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | | | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | | | | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | | | | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$ | 1, 2, 3 | | | | |
| I_{IH} | Input HIGH Current | | 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | 1, 2, 3 | | | | |
| | | | 340 | μA | $-55^\circ C$ | | | | | | |
| I_{EE} | Power Supply Current | -70 | -25 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3 | | | | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table 1) on each manufactured lot at $-55^\circ C$, $+25^\circ C$ and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version — Preliminary (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.30 | 1.80 | 0.40 | 1.45 | 0.40 | 1.80 | ns | Figures 1 and 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.20 | 0.30 | 1.20 | 0.30 | 1.20 | ns | | 4 |

Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.30 | 1.80 | 0.40 | 1.45 | 0.40 | 1.80 | ns | Figures 1 and 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.20 | 0.30 | 1.20 | 0.30 | 1.20 | ns | | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

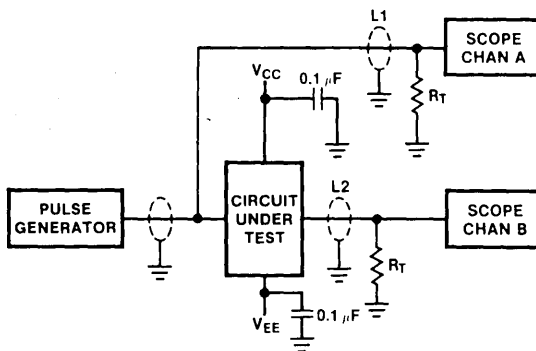
Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Test Circuitry



Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

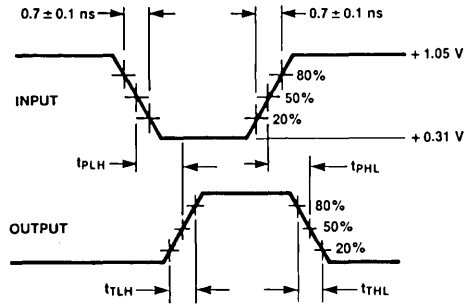
All unused outputs are loaded with 50Ω to GND

$C_L =$ Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

TL/F/10609-5

Switching Waveforms



TL/F/10609-6

FIGURE 2. Propagation Delay and Transition Times



F100322

Low Power 9-Bit Buffer

General Description

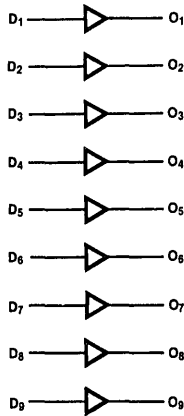
The F100322 is a monolithic 9-bit buffer. The device contains nine non-inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Features:

- 30% power reduction of the F100122
- 2000V ESD protection
- Pin/function compatible with F100122
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

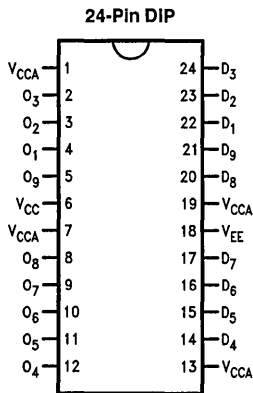
Logic Symbol



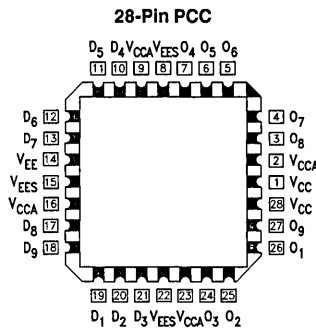
| Pin Names | Description |
|---------------------------------|--------------|
| D ₁ , D ₉ | Data Inputs |
| O ₁ , O ₉ | Data Outputs |

TL/F/10608-1

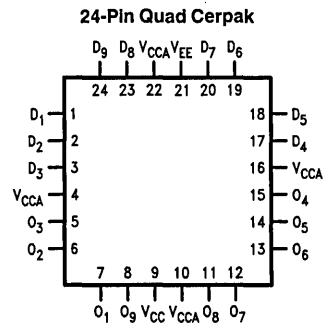
Connection Diagrams



TL/F/10608-2



TL/F/10608-4



TL/F/10608-3

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |

| | |
|---------------------------------|--------|
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|------------------------------------|-----------------|
| Case Temperature (T _C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V _{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-------------------|----------------------|-------|-------|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |
| I _{IH} | Input HIGH Current | | | 240 | μA | V _{IN} = V _{IH} (Max) | |
| I _{EE} | Power Supply Current | -65 | | -30 | mA | Inputs Open | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND

| Symbol | Parameter | T _C = 0°C | | T _C = +25°C | | T _C = +85°C | | Units | Conditions |
|--------------------------------------|---|----------------------|------|------------------------|------|------------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output | 0.45 | 1.45 | 0.45 | 1.45 | 0.45 | 1.55 | ns | Figures 1 and 2 (Note 1) |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.20 | 0.35 | 1.20 | 0.35 | 1.20 | ns | Figures 1 and 2 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

PCC and Cerpak AC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND

| Symbol | Parameter | T _C = 0°C | | T _C = +25°C | | T _C = +85°C | | Units | Conditions |
|--------------------------------------|---|----------------------|------|------------------------|------|------------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay Data to Output | 0.45 | 1.25 | 0.45 | 1.25 | 0.45 | 1.35 | ns | Figures 1 and 2 (Note 2) |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | Figures 1 and 2 |
| t _{S,G-G} | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Military Version—Preliminary DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | | Notes |
|-----------|----------------------|-------|-------|---------|---------------------------------|--|---------------------------------------|------------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | | 1, 2, 3, 4 |
| V_{IL} | Input HIGH Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | | 1, 2, 3, 4 |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$ | | 1, 2, 3 |
| I_{IH} | Input HIGH Current | | 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | | 1, 2, 3 |
| | | | 340 | μA | $-55^\circ C$ | | | |
| I_{EE} | Power Supply Current | -70 | -25 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.30 | 1.80 | 0.40 | 1.60 | 0.40 | 1.80 | ns | Figures 1 and 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.20 | 0.30 | 1.20 | 0.30 | 1.20 | ns | | 4 |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.30 | 1.80 | 0.40 | 1.60 | 0.40 | 1.80 | ns | Figures 1 and 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.20 | 0.30 | 1.20 | 0.30 | 1.20 | ns | | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$, only Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

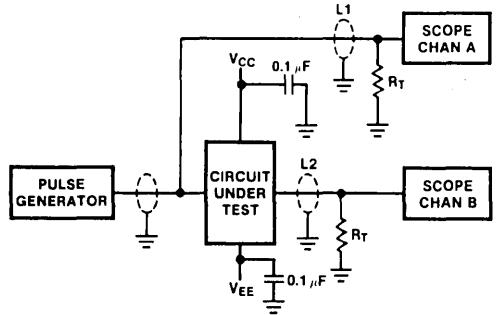
Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 200 ps with multiple outputs switching.

Test Circuit

Notes:

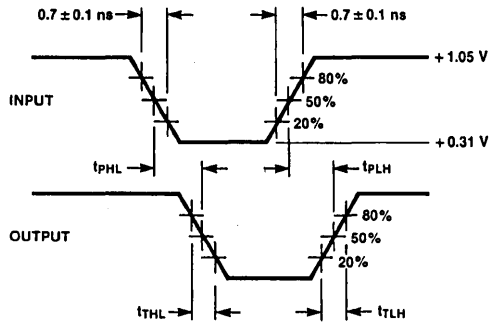
- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/10608-5

FIGURE 1. AC Test Circuit

Switching Waveforms



TL/F/10608-6

FIGURE 2. Propagation Delay and Transition Times



F100324

Low Power Hex TTL-to-ECL Translator

General Description

The F100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. The output levels are voltage compensated over the full $-4.2V$ to $-5.7V$ range.

When the circuit is used in the differential mode, the F100324, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

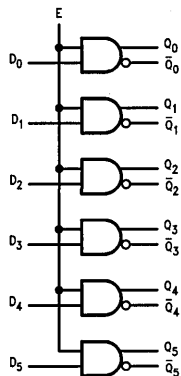
The F100324 is pin and function compatible with the F100124 with similar AC performance, but features power dissipation roughly half of the F100124 to ease system cooling requirements.

Features

- Pin/function compatible with F100124
- Meets F100124 AC specifications
- 50% power reduction of the F100124
- Differential outputs
- 2000V ESD protection
- $-4.2V$ to $-5.7V$ operating range

Ordering Code: See Section 8

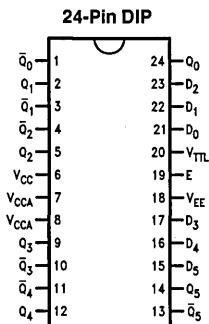
Logic Diagram



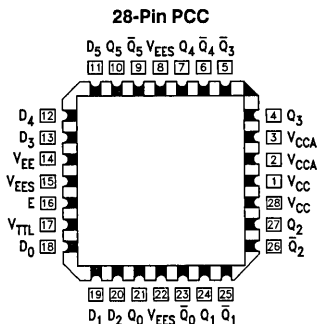
TL/F/9878-4

| Pin Names | Description |
|---------------------------|----------------------------|
| D_0 – D_5 | Data Inputs |
| E | Enable Input |
| Q_0 – Q_5 | Data Outputs |
| \bar{Q}_0 – \bar{Q}_5 | Complementary Data Outputs |

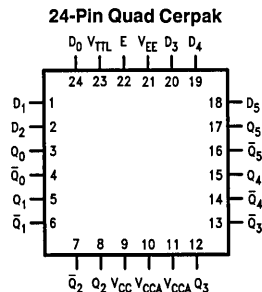
Connection Diagrams



TL/F/9878-1



TL/F/9878-3



TL/F/9878-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| V _{TTL} Pin Potential to Ground Pin | +6.0V to -0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|------------------------------------|-----------------|
| Case Temperature (T _C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V _{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------------|--|--------------|-------|-----------|-------|---|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | | |
| V _{OHC} | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | 5.0 | V | Guaranteed HIGH Signal for All Inputs |
| V _{IL} | Input LOW Voltage | 0 | | 0.8 | V | Guaranteed LOW Signal for All Inputs |
| V _{CD} | Input Clamp Diode Voltage | -1.2 | | | V | I _{IN} = -18 mA |
| I _{IH} | Input HIGH Current Data Enable | | | 20 120 | μA | V _{IN} = +2.4V, All Other Inputs V _{IN} = GND |
| | Input HIGH Current Breakdown Test, All Inputs | | | 1.0 | mA | V _{IN} = +5.5V, All Other Inputs = GND |
| I _{IL} | Input LOW Current Data Enable | -0.9 -5.4 | | | mA | V _{IN} = +0.4V, All Other Inputs V _{IN} = V _{IH} |
| I _{EE} | V _{EE} Power Supply Current | -70 | -45 | -22 | mA | All Inputs V _{IN} = +4.0V |
| I _{TTL} | V _{TTL} Power Supply Current | | 25 | 38 | mA | All Inputs V _{IN} = GND |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electric Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data and Enable to Output | 0.50 | 3.00 | 0.50 | 2.90 | 0.50 | 3.00 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |

PCC and Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|----------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data and Enable to Output | 0.50 | 2.80 | 0.50 | 2.70 | 0.50 | 2.80 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |
| t_{S-G-G} | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in the propagation delays between each of the outputs.

Military Version—Preliminary

DC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | | Notes |
|-----------|---------------------|-------|-------|---------|---------------------------------|--|---------------------------------------|------------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| | Cutoff Voltage | | -1950 | mV | $0^\circ C$ to $+125^\circ C$ | OE or DIR Low | | |
| | | | -1915 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | 2.0 | 5.0 | V | $-55^\circ C$ to $+125^\circ C$ | Over V_{TTL} , V_{EE} , T_C Range | | 1, 2, 3, 4 |
| V_{IL} | Input LOW Voltage | 0.0 | 0.8 | V | $-55^\circ C$ to $+125^\circ C$ | Over V_{TTL} , V_{EE} , T_C Range | | 1, 2, 3, 4 |
| I_{IH} | Input HIGH Current | | 20 | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{IN} = +2.7V$ | | 1, 2, 3 |
| | Breakdown Test | | 100 | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{IN} = +5.5V$ | | |

Military Version—Preliminary (Continued)

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$, $V_{TTL} = +4.5V$ to $+5.5V$ (Continued)

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes |
|-----------|-----------------------------------|--------------|------|-------|---------------------------------|-----------------------------|---------|
| I_{IL} | Input LOW Current Data Enable | -0.9 -5.4 | | mA | $-55^\circ C$ to $+125^\circ C$ | $V_{IN} = +0.5V$ | 1, 2, 3 |
| V_{FCD} | Input Clamp Diode Voltage | | -1.2 | V | $-55^\circ C$ to $+125^\circ C$ | $I_{IN} = -18 mA$ | 1, 2, 3 |
| I_{EE} | V_{EE} Power Supply Current | -70 | -22 | mA | $-55^\circ C$ to $+125^\circ C$ | All Inputs $V_{IN} = +4.0V$ | 1, 2, 3 |
| I_{TTL} | V_{TTL} Power Supply Current | | 38 | mA | $-55^\circ C$ to $+125^\circ C$ | All Inputs $V_{IN} = GND$ | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Ceramic Dual-In-Line Package AC Electric Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|----------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data and Enable to Output | 0.50 | 3.00 | 0.50 | 2.90 | 0.30 | 3.30 | ns | Figures 1 and 2 | 1, 2, 3, |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | | 4 |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data and Enable to Output | 0.50 | 3.00 | 0.50 | 2.90 | 0.30 | 3.30 | ns | Figures 1 and 2 | 1, 2, 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | | 4 |

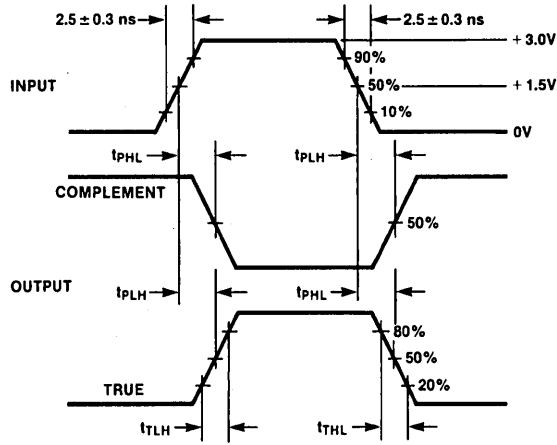
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

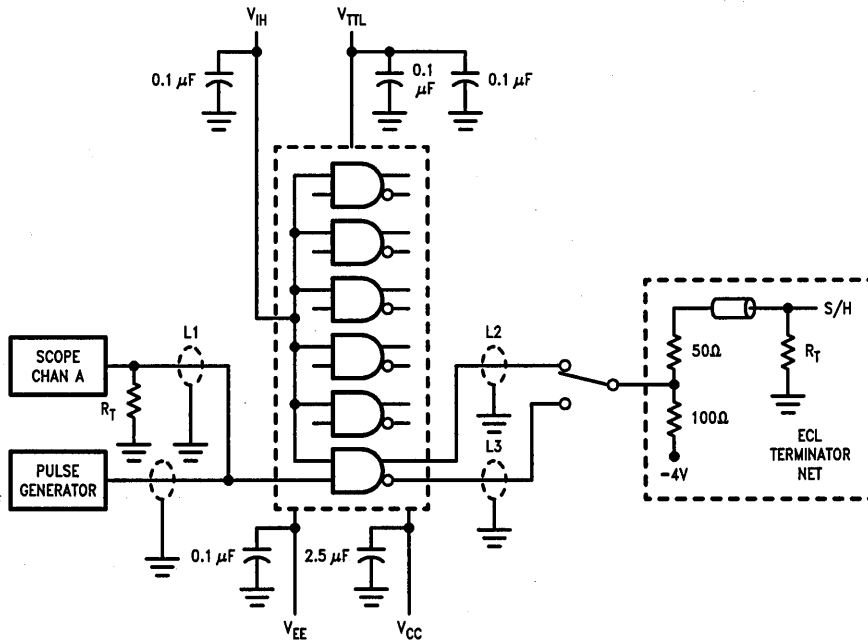
Switching Waveform



TL/F/9878-6

FIGURE 1. Propagation Delay and Transition Times

Test Circuit



TL/F/9878-5

FIGURE 2. AC Test Circuit

Notes:

$V_{CC}, V_{CCA} = 0V, V_{EE} = -4.5V, V_{TTL} = +5.0V, V_{IH} = +3.0V$

$L1, L2$ and $L3 =$ equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling $0.1\mu F$ from GND to V_{CC}, V_{EE} and V_{TTL}

All unused outputs are loaded with 50Ω to GND

$C_L =$ Fixture and stray capacitance ≤ 3 pF

F100325

Low Power Hex ECL-to-TTL Translator

General Description

The F100325 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation, or for use in Schmitt trigger applications. All inputs have 50k Ω pull-down resistors. When the inputs are either unconnected or at the same potential the outputs will go low.

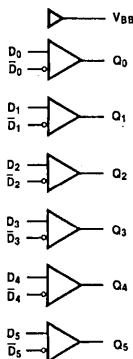
When used in single-ended operation the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The V_{EE} and V_{TTL} power may be applied in either order.

Features

- Pin/function compatible with F100125
- Meets F100125 AC specifications
- 50% power reduction of the F100125
- Differential inputs with built in offset
- Standard FAST[®] outputs
- 2000V ESD protection
- -4.2V to -5.7V operating range

Ordering Code: See Section 8

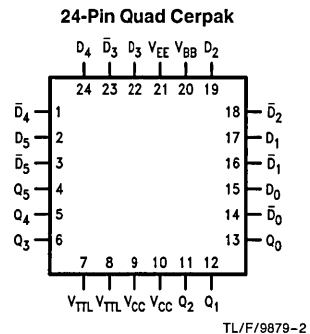
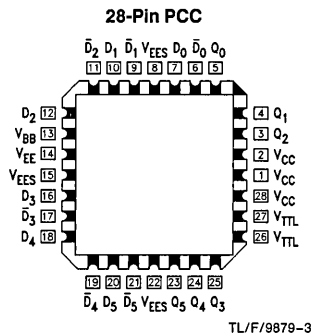
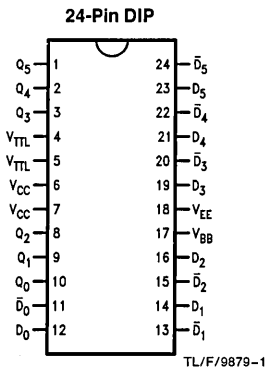
Logic Diagram



TL/F/9879-4

| Pin Names | Description |
|---------------------------|-----------------------|
| D_0 – D_5 | Data Inputs |
| \bar{D}_0 – \bar{D}_5 | Inverting Data Inputs |
| Q_0 – Q_5 | Data Outputs |

Connection Diagrams



Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| V_{TTL} Pin Potential to Ground Pin | +6.0V to -0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|-----------------------------|-----------------|
| Case Temperature (T_C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V_{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------|---------------------------------|----------------|-------|----------------|-------|--|
| V_{BB} | Output Reference Voltage | -1380 | -1320 | -1260 | mV | $I_{V_{BB}} = -2.1$ mA |
| V_{IH} | Single-Ended Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB}) |
| V_{IL} | Single-Ended Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB}) |
| V_{OH} | Output HIGH Voltage | 2.5 | | | V | $I_{OH} = -2.0$ mA |
| V_{OL} | Output LOW Voltage | | | 0.5 | V | $I_{OL} = 20$ mA |
| V_{DIFF} | Input Voltage Differential | 150 | | | mV | Required for Full Output Swing |
| V_{CM} | Common Mode Voltage | $V_{CC} - 2.0$ | | $V_{CC} - 0.5$ | V | |
| I_{IH} | Input HIGH Current | | | 350 | μA | $V_{IN} = V_{IH}(\text{Max})$, $D_0-D_5 = V_{BB}$, $\bar{D}_0-\bar{D}_5 = V_{IL}(\text{Min})$ |
| I_{IL} | Input LOW Current | 0.5 | | | μA | $V_{IN} = V_{IL}(\text{Min})$, $D_0-D_5 = V_{BB}$ |
| I_{OS} | Output Short-Circuit Current | -150 | | -60 | mA | $V_{OUT} = GND^*$ |
| I_{EE} | V_{EE} Power Supply Current | -37 | -27 | -17 | mA | $D_0-D_5 = V_{BB}$ |
| I_{TTL} | V_{TTL} Power Supply Current | | 45 | 65 | mA | $D_0-D_5 = V_{BB}$ |

*Test one output at a time.

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|-------------------------------------|-------------------|------|---------------------|------|---------------------|------|-------|----------------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.80 | 3.50 | 0.90 | 3.70 | 1.00 | 4.00 | ns | $C_L = 15$ pF Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 1.60 | 4.30 | 1.70 | 4.50 | 1.80 | 4.80 | ns | $C_L = 50$ pF Figures 1 and 3 |

PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|-------------------------------------|-------------------|------|---------------------|------|---------------------|------|-------|----------------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.80 | 3.30 | 0.90 | 3.50 | 1.00 | 3.80 | ns | $C_L = 15$ pF Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 1.60 | 4.10 | 1.70 | 4.30 | 1.80 | 4.60 | ns | $C_L = 50$ pF Figures 1 and 3 |
| t_{S-G-G} | Skew Gate to Gate | | TBD | | TBD | | TBD | ps | PCC only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in the propagation delays between each of the outputs.

Truth Table

| Inputs | | Outputs |
|----------|-------------|---------|
| D_n | \bar{D}_n | Q_n |
| L | H | L |
| H | L | H |
| L | L | L |
| H | H | L |
| Open | Open | L |
| V_{EE} | V_{EE} | L |
| L | V_{BB} | L |
| H | V_{BB} | H |
| V_{BB} | L | H |
| V_{BB} | H | L |

H = HIGH Voltage Level

L = LOW Voltage Level

Military Version—Preliminary

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$, $C_L = 50$ pF, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes |
|------------|--------------------------------|-------|-------|---------|------------------------------------|--|------------|
| V_{BB} | Output Reference Voltage | -1380 | -1260 | mV | $-55^\circ C$ to $+125^\circ C$ | $I_{V_{BB}} = -3 \mu A$, $V_{EE} = -4.2V$ $I_{V_{BB}} = -2.1$ mA, $V_{EE} = -5.7V$ | 1, 2, 3 |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB}) | 1, 2, 3, 4 |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB}) | 1, 2, 3, 4 |
| V_{OH} | Output HIGH Voltage | 2.5 | | mV | $0^\circ C$ to $+125^\circ C$ | $I_{OH} = -2.0$ mA $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | 1, 2, 3 |
| | | 2.4 | | | $-55^\circ C$ | | |
| V_{OL} | Output LOW Voltage | | 0.5 | mV | $-55^\circ C$ to $+125^\circ C$ | $I_{OL} = 20$ mA | |
| V_{DIFF} | Input Voltage Differential | 150 | | mV | $-55^\circ C$ to $+125^\circ C$ | Required for Full Output Swing | 1, 2, 3 |
| V_{CM} | Common Mode Voltage | -2000 | -500 | mV | $-55^\circ C$ to $+125^\circ C$ | | 1, 2, 3, 4 |
| I_{IH} | Input HIGH Current | | 350 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$, $D_0-D_5 = V_{BB}$, $\bar{D}_0-\bar{D}_5 = V_{IL}(\text{Min})$ | 1, 2, 3 |
| | | | 500 | | $-55^\circ C$ | | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IL}(\text{Min})$, $D_0-D_5 = V_{BB}$ | 1, 2, 3 |
| I_{OS} | Output Short Circuit Current | -150 | -60 | mA | $-55^\circ C$ to $+125^\circ C$ | $V_{OUT} = GND$ Test One Output at a Time | 1, 2, 3 |
| I_{CEX} | Output HIGH Leakage Current | | 250 | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{OUT} = 5.5V$ | 1, 2, 3 |
| I_{EE} | V_{EE} Power Supply Current | -35 | -12 | mA | $-55^\circ C$ to $+125^\circ C$ | $D_0-D_5 = V_{BB}$ | 1, 2, 3 |
| I_{TTL} | V_{TTL} Power Supply Current | | 65 | mA | $-55^\circ C$ to $+125^\circ C$ | $D_0-D_5 = V_{BB}$ | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|-----------|-------------------------------------|---------------------|------|---------------------|------|----------------------|------|-------|---|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} | Propagation Delay Data to Output | 1.50 | 5.00 | 1.60 | 4.70 | 1.70 | 5.70 | ns | $C_L = 50$ pF <i>Figures 1 and 3</i> | 1, 2, 3 |
| t_{PHL} | | | | | | | | | | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|-------------------------------------|---------------------|------|---------------------|------|----------------------|------|-------|----------------------------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 1.50 | 5.00 | 1.60 | 4.70 | 1.70 | 5.70 | ns | $C_L = 50$ pF Figures 1 and 3 | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Switching Waveform

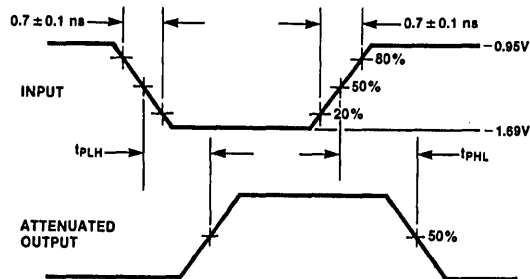
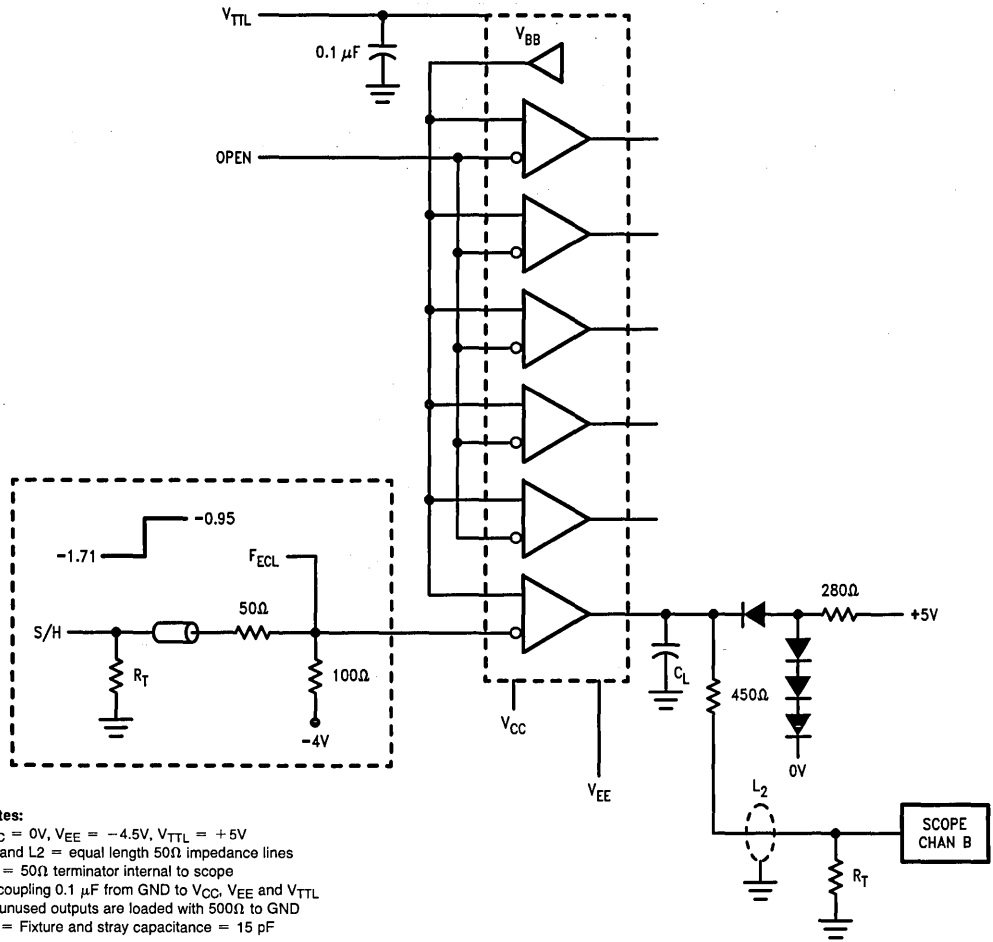


FIGURE 1. Propagation Delay

TL/F/9879-6

Test Circuits



Notes:
 $V_{CC} = 0V$, $V_{EE} = -4.5V$, $V_{TTL} = +5V$
 L_1 and L_2 = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1\ \mu F$ from GND to V_{CC} , V_{EE} and V_{TTL}
 All unused outputs are loaded with 500Ω to GND
 C_L = Fixture and stray capacitance = $15\ pF$

FIGURE 2. AC Test Circuit for 15 pF Loading

TL/F/9879-5

Test Circuits (Continued)

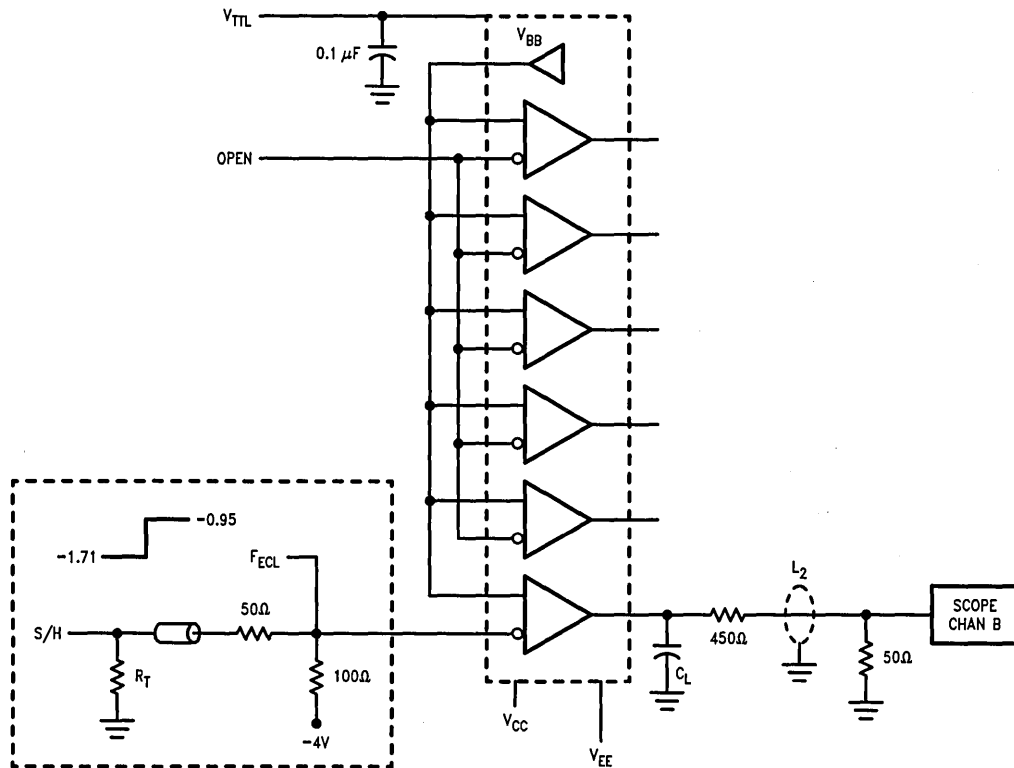


FIGURE 3. AC Test Circuit for 50 pF Loading

TL/F/9879-8

Notes:

- $V_{CC} = 0V$, $V_{EE} = -4.5V$, $V_{TTL} = +5V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 R_T = 50Ω terminator internal to scope
 Decoupling $0.1\ \mu F$ from GND to V_{CC} , V_{EE} and V_{TTL}
 All unused outputs are loaded with 500Ω to GND
 C_L = Fixture and stray capacitance = $50\ pF$

F100328

Low Power Octal ECL/TTL Bi-Directional Translator with Latch

General Description

The F100328 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the F100328 transparent.

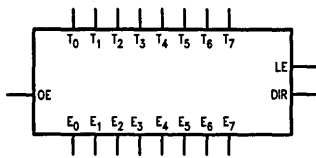
The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is $-2.0V$, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The F100328 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 k Ω pull-down resistors.

Features

- Identical performance to the F100128 at 50% of the supply current
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- FAST® TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = $-4.2V$ to $-5.7V$

Logic Symbol

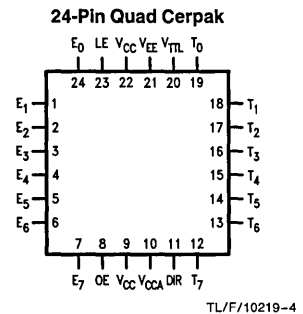
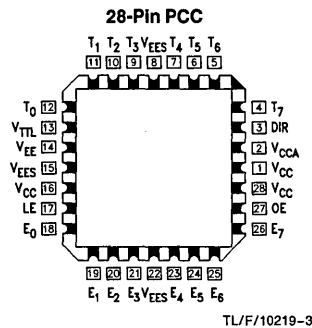
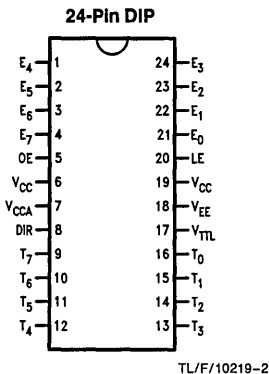


TL/F/10219-1

| Pin Names | Description |
|--------------------------------|-------------------------|
| E ₀ -E ₇ | ECL Data I/O |
| T ₀ -T ₇ | TTL Data I/O |
| OE | Output Enable Input |
| LE | Latch Enable Input |
| DIR | Direction Control Input |

All pins function at 100K ECL levels except for T₀-T₇.

Connection Diagrams



F100329
Low Power Octal ECL/TTL Bidirectional Translator with Register
General Description

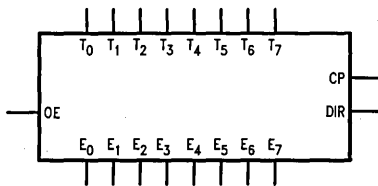
The F100329 is an octal registered bidirectional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of the translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP) even though only one output is enabled at the time.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is $-2.0V$, presenting a high impedance to the data bus. This high impedance reduces the termination power and prevents loss of low state noise margin when several loads share the bus.

The F100329 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have $50\text{ k}\Omega$ pull-down resistors.

Features

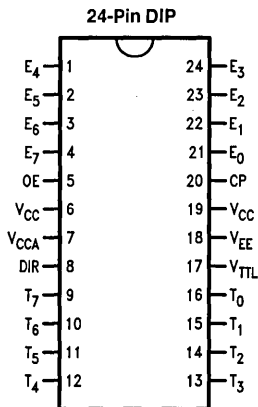
- Bidirectional translation
- ECL high impedance outputs
- Registered outputs
- FAST TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = $-4.2V$ to $-5.7V$

Logic Symbol


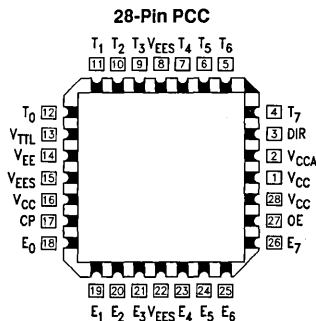
TL/F/10583-1

| Pin Names | Description |
|--------------------------------|---|
| E ₀ -E ₇ | ECL Data I/O |
| T ₀ -T ₇ | TTL Data I/O |
| OE | Output Enable Input |
| CP | Clock Pulse Input (Active Rising Edge) |
| DIR | Direction Control Input |

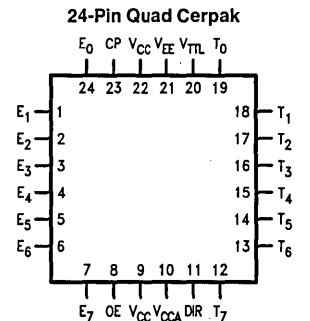
All pins function at 100K ECL levels except for T₀-T₇.

Connection Diagrams


TL/F/10583-2



TL/F/10583-3



TL/F/10583-4

F100331 Low Power Triple D Flip-Flop

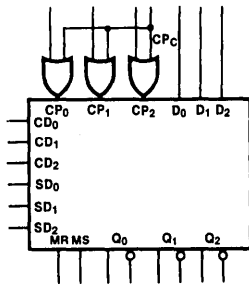
General Description

The F100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set, Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 k Ω pull-down resistors.

Features

- 35% power reduction of the F100131
- 2000V ESD protection
- Pin/function compatible with F100131
- Voltage compensated operating range = -4.2V to -5.7V

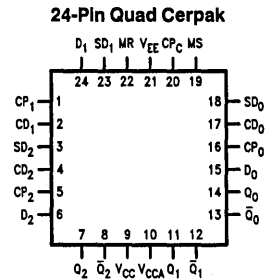
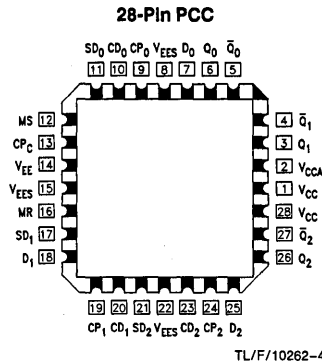
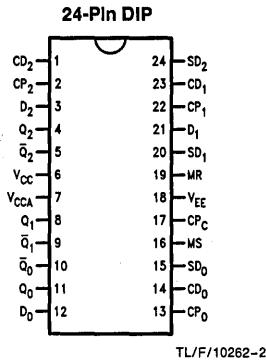
Logic Symbol



TL/F/10262-1

| Pin Names | Description |
|---------------------------|--------------------------------|
| CP_0 - CP_2 | Individual Clock Inputs |
| CP_C | Common Clock Input |
| D_0 - D_2 | Data Inputs |
| CD_0 - CD_2 | Individual Direct Clear Inputs |
| SD_n | Individual Direct Set Inputs |
| MR | Master Reset Input |
| MS | Master Set Input |
| Q_0 - Q_2 | Data Outputs |
| \bar{Q}_0 - \bar{Q}_2 | Complementary Data Outputs |

Connection Diagrams



F100336

Low Power 4-Stage Counter/Shift Register

General Description

The F100336 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable (\overline{CEP} , \overline{CET}) inputs are provided for ease of cascading in multistage counters. One Count Enable (\overline{CET}) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation, D_3 is the Serial Data input. In counting operations the Terminal Count (\overline{TC}) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the \overline{TC} output repeats the Q_3 output. The dual nature of this \overline{TC}/Q_3 output and the D_0/\overline{CET} input means that one interconnection from one stage to the next higher stage serves as the link for

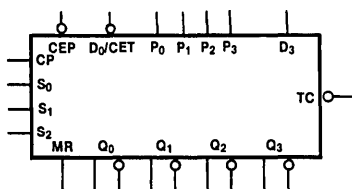
multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 k Ω pull-down resistors.

Features

- 30% power reduction of the F100136
- 2000V ESD protection
- Pin/function compatible with F100136
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

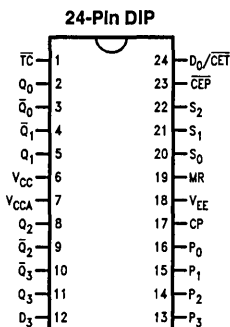
Logic Symbol



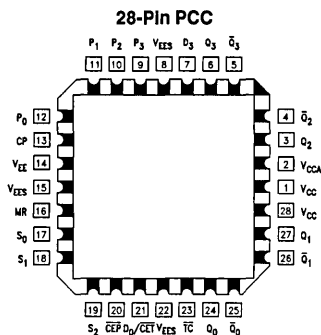
TL/F/10584-1

| Pin Names | Description |
|---------------------------------|--|
| CP | Clock Pulse Input |
| \overline{CEP} | Count Enable Parallel Input (Active LOW) |
| D_0/\overline{CET} | Serial Data Input/Count Enable |
| S_0-S_2 | Select Inputs |
| MR | Master Reset Input |
| P_0-P_3 | Preset Inputs |
| D_3 | Serial Data Input |
| \overline{TC} | Terminal Count Output |
| Q_0-Q_3 | Data Outputs |
| $\overline{Q}_0-\overline{Q}_3$ | Complementary Data Outputs |

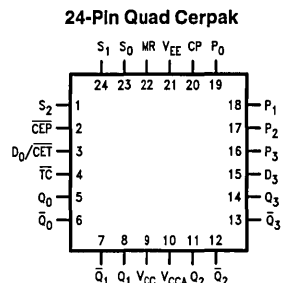
Connection Diagrams



TL/F/10584-2

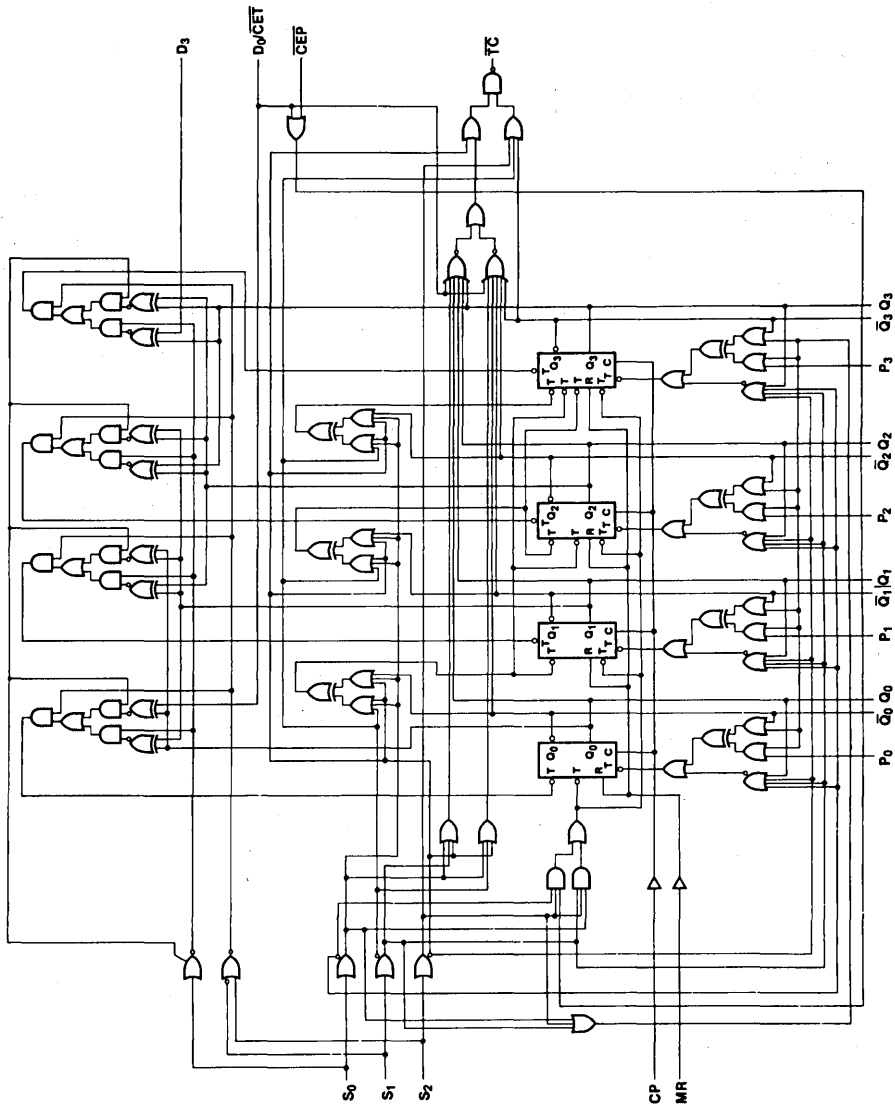


TL/F/10584-4



TL/F/10584-3

Logic Diagram



TL/F/10584-5

Function Select Table

| S ₂ | S ₁ | S ₀ | Function |
|----------------|----------------|----------------|---------------|
| L | L | L | Parallel Load |
| L | L | H | Complement |
| L | H | L | Shift Left |
| L | H | H | Shift Right |
| H | L | L | Count Down |
| H | L | H | Clear |
| H | H | L | Count Up |
| H | H | H | Hold |

Truth Table

Q₀ = LSB

| Inputs | | | | | | | | Outputs | | | | | Mode |
|--------|----------------|----------------|----------------|------------------|-----------------------------------|----------------|----|-----------------------------|------------------|------------------|------------------|------------------|---|
| MR | S ₂ | S ₁ | S ₀ | \overline{CEP} | D ₀ / \overline{CET} | D ₃ | CP | Q ₃ | Q ₂ | Q ₁ | Q ₀ | \overline{TC} | |
| L | L | L | L | X | X | X | ↗ | P ₃ | P ₂ | P ₁ | P ₀ | L | Preset (Parallel Load) |
| L | L | L | H | X | X | X | ↗ | \overline{Q}_3 | \overline{Q}_2 | \overline{Q}_1 | \overline{Q}_0 | L | Invert |
| L | L | H | L | X | X | X | ↗ | D ₃ | Q ₃ | Q ₂ | Q ₁ | D ₃ | Shift Left |
| L | L | H | H | X | X | X | ↗ | Q ₂ | Q ₁ | Q ₀ | D ₀ | Q ₃ * | Shift Right |
| L | H | L | L | L | L | X | ↗ | (Q ₀₋₃) minus 1 | | | | ⊖ | Count Down |
| L | H | L | L | H | L | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | ⊖ | Count Down with \overline{CEP} not active |
| L | H | L | L | X | H | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Count Down with \overline{CET} not active |
| L | H | L | H | X | X | X | ↗ | L | L | L | L | H | Clear |
| L | H | H | L | L | L | X | ↗ | (Q ₀₋₃) plus 1 | | | | ⊕ | Count Up |
| L | H | H | L | H | L | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | ⊕ | Count Up with \overline{CEP} not active |
| L | H | H | L | X | H | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Count Up with \overline{CET} not active |
| L | H | H | H | X | X | X | ↗ | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Hold |
| H | L | L | L | X | X | X | X | L | L | L | L | L | Asynchronous Master Reset |
| H | L | L | H | X | X | X | X | L | L | L | L | L | |
| H | L | H | L | X | X | X | X | L | L | L | L | L | |
| H | L | H | H | X | X | X | X | L | L | L | L | L | |
| H | H | L | L | X | H | X | X | L | L | L | L | H | |
| H | H | L | H | X | X | X | X | L | L | L | L | H | |
| H | H | H | L | X | X | X | X | L | L | L | L | H | |
| H | H | H | H | X | X | X | X | L | L | L | L | H | |

- ⊖ = L if Q₀-Q₃ = LLLL
H if Q₀-Q₃ ≠ LLLL
- ⊕ = L if Q₀-Q₃ = HHHH
H if Q₀-Q₃ ≠ HHHH
- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Don't Care
- ↗ = LOW-to-HIGH Transition

*Before the clock, \overline{TC} is Q₃
After the clock, \overline{TC} is Q₂

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|----------------------|--------------|-------|--------------|-------|---|------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |
| I_{IH} | Input HIGH Current | | | 240 | μA | $V_{IN} = V_{IH}(\text{Max})$ | |
| I_{EE} | Power Supply Current | -198 -220 | | -100 -100 | mA | Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Recommended Operating Conditions

| | |
|-----------------------------|-----------------|
| Case Temperature (T_C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V_{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|--|------|--|------|--|------|-------|-------------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{shift} | Shift Frequency | 250 | | 250 | | 250 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Q_n, \bar{Q}_n | 0.70 | 1.90 | 0.70 | 1.90 | 0.80 | 2.00 | ns | Figures 1 and 3 (Note 1) |
| t_{PLH} t_{PHL} | Propagation Delay CP to $\bar{T}C$ (Shift) | 1.30 | 3.80 | 1.30 | 3.80 | 1.40 | 3.90 | ns | Figures 1, 7, 8 (Note 1) |
| t_{PLH} t_{PHL} | Propagation Delay CP to $\bar{T}C$ (Count) | 1.60 | 4.60 | 1.60 | 4.60 | 1.60 | 5.00 | ns | Figures 1 and 9 (Note 1) |
| t_{PLH} t_{PHL} | Propagation Delay MR to Q_n, \bar{Q}_n | 1.10 | 2.50 | 1.10 | 2.50 | 1.20 | 2.60 | ns | Figures 1 and 4 (Note 1) |
| t_{PLH} t_{PHL} | Propagation Delay MR to $\bar{T}C$ (Count) | 2.00 | 4.00 | 2.00 | 4.00 | 2.20 | 4.10 | ns | Figures 1, 12 (Note 1) |
| t_{PHL} | Propagation Delay MR to $\bar{T}C$ (Shift) | 1.60 | 3.20 | 1.60 | 3.20 | 1.70 | 3.40 | ns | Figures 1, 10, 11 (Note 1) |
| t_{PLH} t_{PHL} | Propagation Delay D_0/\overline{CET} to $\bar{T}C$ | 1.20 | 3.20 | 1.20 | 3.20 | 1.40 | 3.70 | ns | Figures 1 and 5 (Note 1) |
| t_{PLH} t_{PHL} | Propagation Delay S_n to $\bar{T}C$ | 0.90 | 4.00 | 0.90 | 4.20 | 1.00 | 4.80 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.20 | 0.35 | 1.20 | 0.35 | 1.20 | ns | Figures 1 and 3 |
| t_s | Setup Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n MR (Release Time) | 1.00 1.30 1.35 1.90 4.40 2.60 | | 1.00 1.30 1.35 1.90 4.40 2.60 | | 1.00 1.30 1.35 1.90 4.40 2.60 | | ns | Figure 6 |
| t_h | Hold Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n | 0.40 0.50 0.30 0.40 -0.40 | | 0.40 0.50 0.30 0.40 -0.40 | | 0.40 0.50 0.30 0.40 -0.40 | | ns | Figure 6 |
| $t_{pw(H)}$ | Pulse Width HIGH CP, MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|--|------|--|------|--|------|-------|-------------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{shift} | Shift Frequency | 300 | | 300 | | 300 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Q_n, \bar{Q}_n | 0.70 | 1.70 | 0.70 | 1.70 | 0.80 | 1.80 | ns | Figures 1 and 3 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay CP to $\bar{T}C$ (Shift) | 1.30 | 3.60 | 1.30 | 3.60 | 1.40 | 3.70 | ns | Figures 1, 7, 8 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay CP to $\bar{T}C$ (Count) | 1.60 | 4.40 | 1.60 | 4.40 | 1.60 | 4.80 | ns | Figures 1 and 9 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay MR to Q_n, \bar{Q}_n | 1.10 | 2.30 | 1.10 | 2.30 | 1.20 | 2.40 | ns | Figures 1 and 4 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay MR to $\bar{T}C$ (Count) | 2.00 | 3.80 | 2.00 | 3.80 | 2.20 | 3.90 | ns | Figures 1 and 12 (Note 2) |
| t_{PHL} | Propagation Delay MR to $\bar{T}C$ (Shift) | 1.60 | 3.00 | 1.60 | 3.00 | 1.70 | 3.20 | ns | Figures 1, 10, 11 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay D_0/\overline{CET} to $\bar{T}C$ | 1.20 | 3.00 | 1.20 | 3.00 | 1.40 | 3.50 | ns | Figures 1 and 5 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay S_n to $\bar{T}C$ | 0.90 | 3.80 | 0.90 | 4.00 | 1.00 | 4.60 | ns | |
| t_{LH} t_{HL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | Figures 1 and 3 |
| t_s | Setup Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n MR (Release Time) | 0.90 1.20 1.25 1.80 4.30 2.50 | | 0.90 1.20 1.25 1.80 4.30 2.50 | | 0.90 1.20 1.25 1.80 4.30 2.50 | | ns | Figure 6 |
| t_h | Hold Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n | 0.30 0.40 0.20 0.30 -0.50 | | 0.30 0.40 0.20 0.30 -0.50 | | 0.30 0.40 0.20 0.30 -0.50 | | ns | Figure 6 |
| $t_{pw(H)}$ | Pulse Width HIGH CP, MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 |
| $t_{S, G-G}$ | Skew, Gate to Gate | | TBD | | TBD | | TBD | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.**Note 2:** The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Military Version—Preliminary

DC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ\text{C to } +125^\circ\text{C}$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|----------------------|-------|-------|-------|-----------------|---|---------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | 0°C to +125°C | $V_{IN} = V_{IH} \text{ (Max)}$ or $V_{IL} \text{ (Min)}$ | Loading with 50Ω to -2.0V | 1, 2, 3 |
| | | -1085 | -870 | mV | -55°C | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | 0°C to +125°C | $V_{IN} = V_{IH} \text{ (Min)}$ or $V_{IL} \text{ (Max)}$ | Loading with 50Ω to -2.0V | 1, 2, 3 |
| | | -1830 | -1555 | mV | -55°C | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | 0°C to +125°C | $V_{IN} = V_{IH} \text{ (Min)}$ or $V_{IL} \text{ (Max)}$ | Loading with 50Ω to -2.0V | 1, 2, 3 |
| | | -1085 | | mV | -55°C | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | 0°C to +125°C | $V_{IN} = V_{IH} \text{ (Min)}$ or $V_{IL} \text{ (Max)}$ | Loading with 50Ω to -2.0V | 1, 2, 3 |
| | | | -1555 | mV | -55°C | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | -55°C to +125°C | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | -55°C to +125°C | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | -55°C to +125°C | $V_{EE} = -4.2V$ $V_{IN} = V_{IL} \text{ (Min)}$ | 1, 2, 3 | |
| I_{IH} | Input HIGH Current | | 240 | μA | 0°C to +125°C | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} \text{ (Max)}$ | 1, 2, 3 | |
| | | | 340 | μA | -55°C | | | |
| I_{EE} | Power Supply Current | -208 | -100 | mA | -55°C to +125°C | Inputs Open $V_{EE} = -4.2V \text{ to } -4.8V$ $V_{EE} = -4.2V \text{ to } -5.7V$ | 1, 2, 3 | |
| | | -230 | -100 | | | | | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)

Ceramic Dual-In-Line Package AC Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ$ | | Units | Conditions | Notes |
|--------------------------------------|--|--|------|--|------|--|------|-------|-------------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{shift} | Shift Frequency | 200 | | 200 | | 200 | | MHz | Figures 2 and 3 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Q_n, \bar{Q}_n | 0.60 | 2.10 | 0.60 | 2.10 | 0.70 | 2.20 | ns | Figures 1 and 3 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay CP to $\bar{T}C$ (Shift) | 1.20 | 4.00 | 1.20 | 4.00 | 1.30 | 4.10 | ns | Figures 1, 7, 8 | |
| t_{PLH} t_{PHL} | Propagation Delay CP to $\bar{T}C$ (Count) | 1.50 | 4.80 | 1.50 | 4.80 | 1.50 | 5.20 | ns | Figures 1 and 9 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay MR to Q_n, \bar{Q}_n | 1.00 | 2.70 | 1.00 | 2.70 | 1.10 | 2.80 | ns | Figures 1 and 4 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay MR to $\bar{T}C$ (Count) | 1.90 | 4.20 | 1.90 | 4.20 | 2.10 | 4.30 | ns | Figures 1, 12 | |
| t_{PHL} | Propagation Delay MR to $\bar{T}C$ (Shift) | 1.50 | 3.40 | 1.50 | 3.40 | 1.60 | 3.60 | ns | Figures 1, 10, 11 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay $D_0/\bar{C}E\bar{T}$ to $\bar{T}C$ | 1.10 | 3.40 | 1.10 | 3.40 | 1.30 | 3.90 | ns | Figures 1 and 5 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay S_n to $\bar{T}C$ | 0.80 | 4.20 | 0.80 | 4.40 | 0.90 | 5.00 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.35 | 1.20 | 0.35 | 1.20 | ns | Figures 1 and 3 | 4 |
| t_s | Setup Time D_3 P_n $D_0/\bar{C}E\bar{T}$ $\bar{C}E\bar{P}$ S_n MR (Release Time) | 1.20 1.50 1.55 2.10 4.60 2.80 | | 1.20 1.50 1.55 2.10 4.60 2.80 | | 1.20 1.50 1.55 2.10 4.60 2.80 | | ns | Figure 6 | 4 |
| t_h | Hold Time D_3 P_n $D_0/\bar{C}E\bar{T}$ $\bar{C}E\bar{P}$ S_n | 0.60 0.70 0.50 0.60 -0.30 | | 0.60 0.70 0.50 0.60 -0.30 | | 0.60 0.70 0.50 0.60 -0.30 | | ns | Figure 6 | 4 |
| $t_{\text{pw(H)}}$ | Pulse Width HIGH CP, MR | 2.20 | | 2.20 | | 2.20 | | ns | Figures 3 and 4 | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroups A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroups A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Military Version—Preliminary (Continued)

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|--|------|--|------|--|------|-------|-------------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{shift} | Shift Frequency | 200 | | 200 | | 200 | | MHz | Figures 2 and 3 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Q_n , \bar{Q}_n | 0.60 | 2.10 | 0.60 | 2.10 | 0.70 | 2.20 | ns | Figures 1 and 3 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay CP to \bar{T}_C (Shift) | 1.20 | 4.00 | 1.20 | 4.00 | 1.30 | 4.10 | ns | Figures 1, 7, 8 | |
| t_{PLH} t_{PHL} | Propagation Delay CP to \bar{T}_C (Count) | 1.50 | 4.80 | 1.50 | 4.80 | 1.50 | 5.20 | ns | Figures 1, 9 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay MR to Q_n , \bar{Q}_n | 1.00 | 2.70 | 1.00 | 2.70 | 1.10 | 2.80 | ns | Figures 1 and 4 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay MR to \bar{T}_C (Count) | 1.90 | 4.20 | 1.90 | 4.20 | 2.10 | 4.30 | ns | Figures 1 and 12 | |
| t_{PHL} | Propagation Delay MR to \bar{T}_C (Shift) | 1.50 | 3.40 | 1.50 | 3.40 | 1.60 | 3.60 | ns | Figures 1, 10, 11 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay D_0/\overline{CET} to \bar{T}_C | 1.10 | 3.40 | 1.10 | 3.40 | 1.30 | 3.90 | ns | Figures 1 and 5 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay S_n to \bar{T}_C | 0.80 | 4.20 | 0.80 | 4.40 | 0.90 | 5.00 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | Figures 1 and 3 | 4 |
| t_s | Setup Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n MR (Release Time) | 1.20 1.50 1.55 2.10 4.60 2.80 | | 1.20 1.50 1.55 2.10 4.60 2.80 | | 1.20 1.50 1.55 2.10 4.60 2.80 | | ns | Figure 6 | 4 |
| t_h | Hold Time D_3 P_n D_0/\overline{CET} \overline{CEP} S_n | 0.60 0.70 0.50 0.60 -0.30 | | 0.60 0.70 0.50 0.60 -0.30 | | 0.60 0.70 0.50 0.60 -0.30 | | ns | Figure 6 | 4 |
| $t_{pw(H)}$ | Pulse Width HIGH CP, MR | 2.20 | | 2.20 | | 2.20 | | ns | Figures 3 and 4 | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

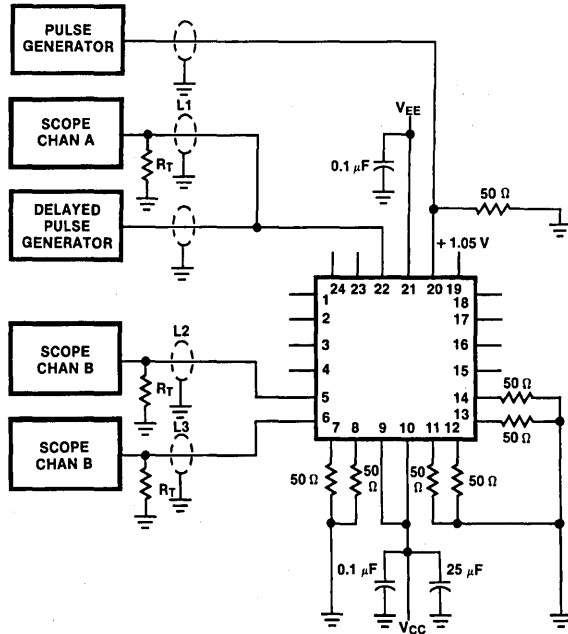
Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 250 ps with multiple outputs switching.

Test Circuitry



Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1, L2 \text{ and } L3 = \text{equal length } 50\Omega \text{ impedance lines}$
 $R_T = 50\Omega \text{ terminator internal to scope}$
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L = \text{Fixture and stray capacitance } \leq 3 \text{ pF}$
 Pin numbers shown are for flatpak;
 for DIP see logic symbol

FIGURE 1. AC Test Circuit

TL/F/10584-6

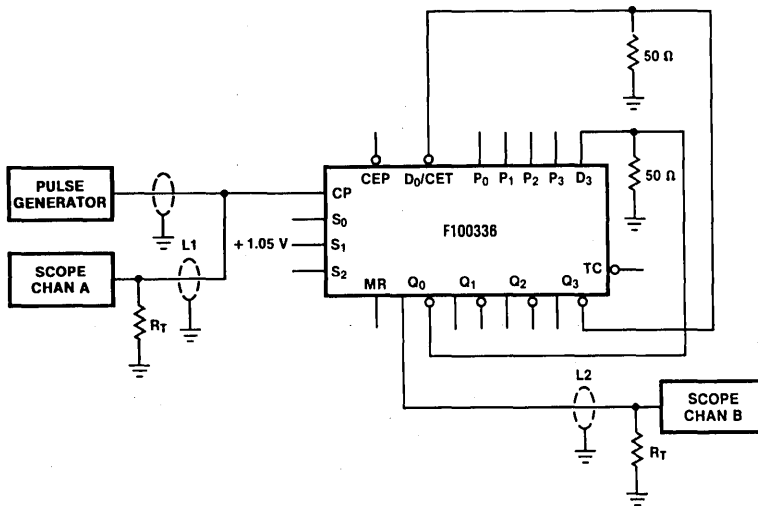


FIGURE 2. Shift Frequency Test Circuit (Shift Left)

TL/F/10584-7

Notes:
 For shift right mode, $+1.05V$ is applied at S_0 .
 The feedback path from output to input should be as short as possible.

Switching Waveforms

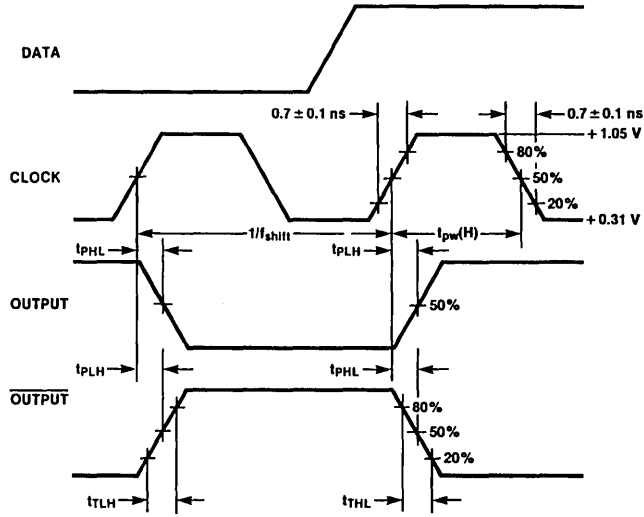


FIGURE 3. Propagation Delay (Clock) and Transition Times

TL/F/10584-8

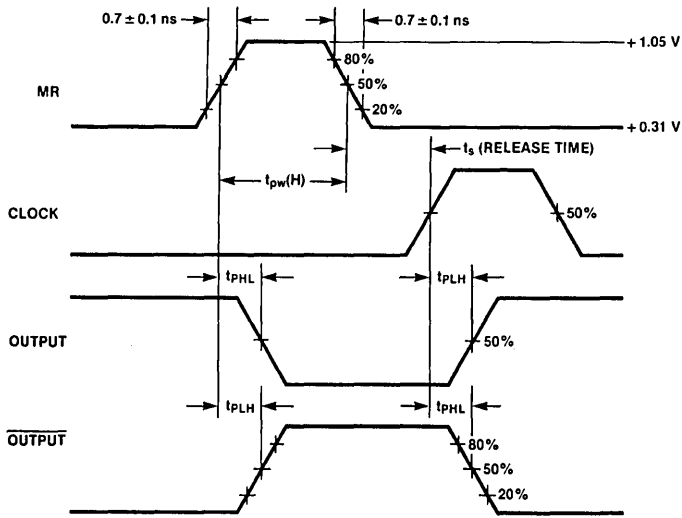


FIGURE 4. Propagation Delay (Reset)

TL/F/10584-9

Switching Waveforms (Continued)

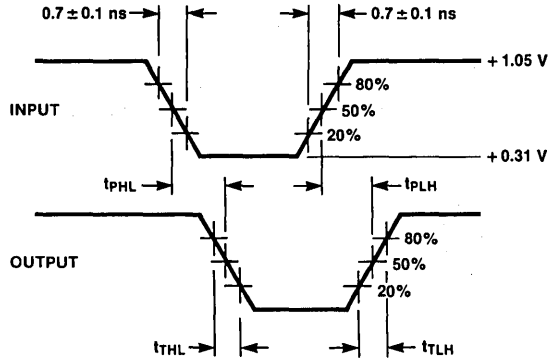
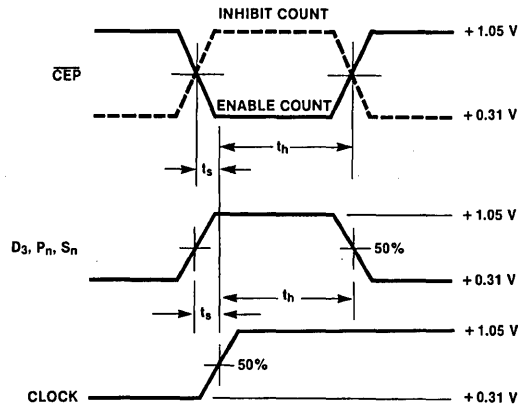


FIGURE 5. Propagation Delay (Serial Data, Selects)

TL/F/10584-10

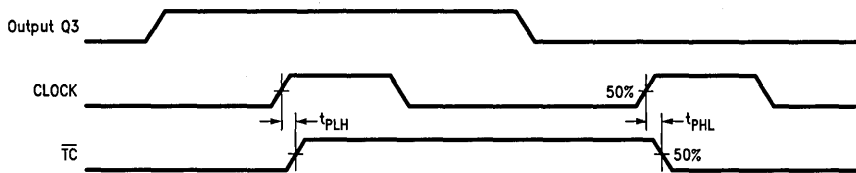


TL/F/10584-11

Notes:

- t_s is the minimum time before the transition of the clock that information must be present at the data input.
- t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Setup and Hold Time

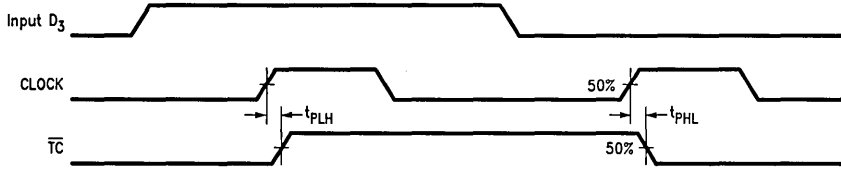


TL/F/10584-15

Note: Shift Right Mode; $S_0 = H, S_1 = H, S_2 = L$.

FIGURE 7. Propagation Delay, Clock to Terminal Count (Shift Right Mode)

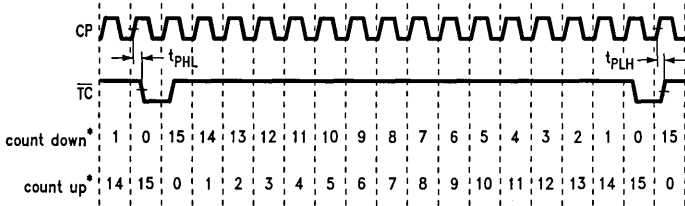
Switching Waveforms (Continued)



Note: Shift Left Mode; $S_0 = L, S_1 = H, S_2 = L$.

TL/F/10584-16

FIGURE 8. Propagation Delay, Clock to Terminal Count (Shift Left Mode)



TL/F/10584-17

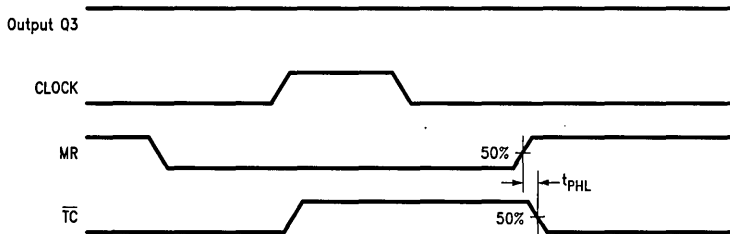
Note:

*Decimal representation of binary outputs.

Count Up: $S_0 = L, S_1 = H, S_2 = H$; Count Down: $S_0 = L, S_1 = L, S_2 = H$.

Measurement taken at 50% point of waveform.

FIGURE 9. Propagation Delay, Clock to Terminal Count (Count Up and Count Down Modes)

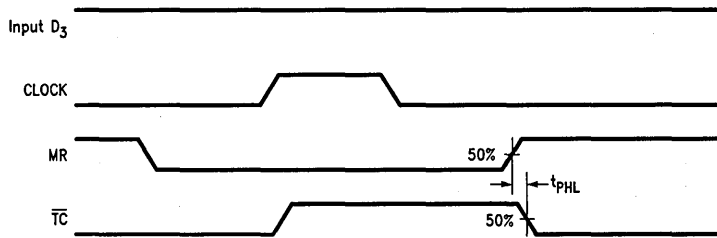


TL/F/10584-18

Note: Shift Right Mode; $S_0 = H, S_1 = H, S_2 = L$.

FIGURE 10. Propagation Delay, Master Reset to Terminal Count (Shift Right Mode)

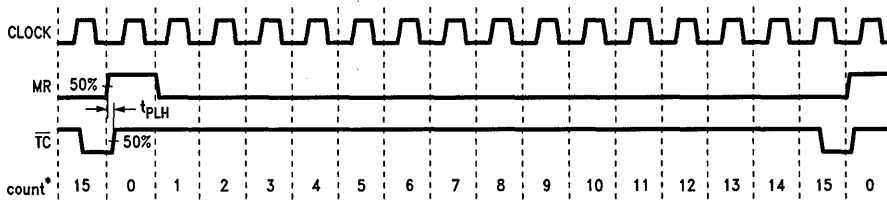
Switching Waveforms (Continued)



TL/F/10584-19

Note: Shift Left Mode; $S_0 = L, S_1 = H, S_2 = L$.

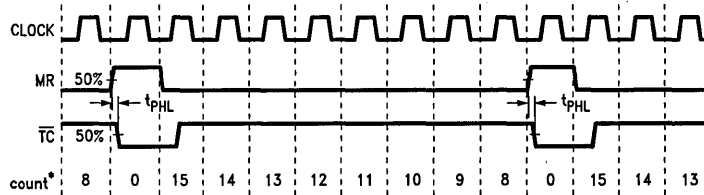
FIGURE 11. Propagation Delay, Master Reset to Terminal Count (Shift Left Mode)



TL/F/10584-20

Note:

*Decimal representation of binary outputs. Count Up Mode: $S_0 = L, S_1 = H, S_2 = H$.



TL/F/10584-21

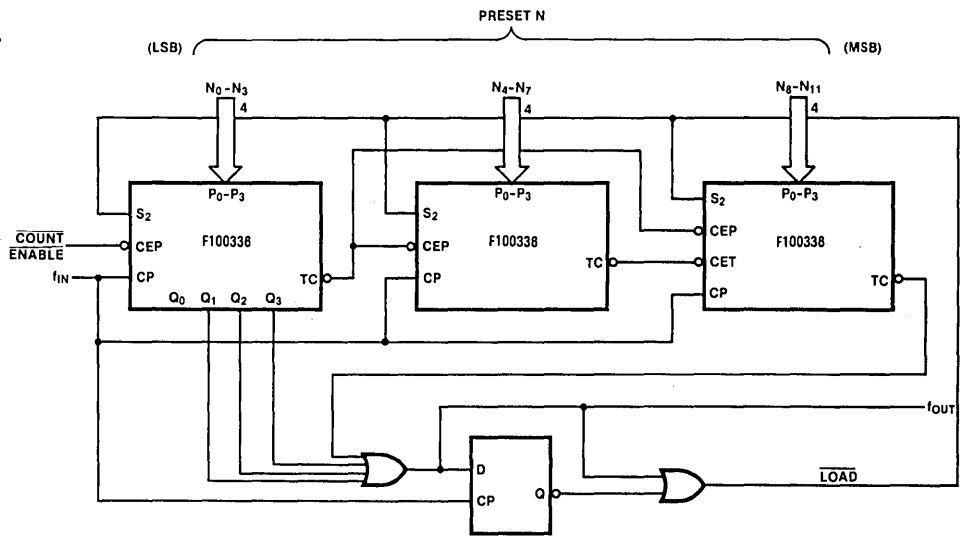
Note:

*Decimal representation of binary outputs. Count Down Mode: $S_0 = L, S_1 = L, S_2 = H$.

FIGURE 12. Propagation Delay, Master Reset to Terminal Count (Count Up and Count Down Modes)

Applications

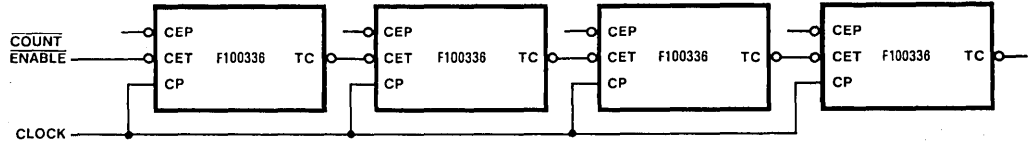
3-Stage Divider, Preset Count Down Mode



Note: If $S_0 = S_1 = S_2 = \text{LOW}$, then $T_C = \text{LOW}$

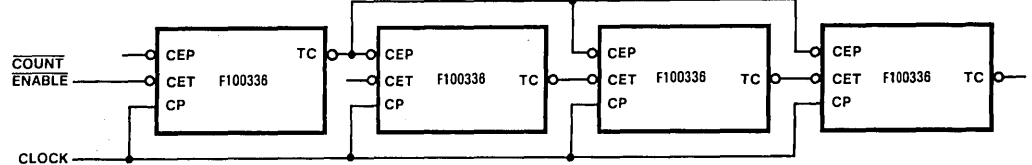
TL/F/10584-12

Slow Expansion Scheme



TL/F/10584-13

Fast Expansion Scheme



TL/F/10584-14



F100341

Low Power 8-Bit Shift Register

General Description

The F100341 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1 , which are internally decoded to select either "parallel entry", "hold", "shift left" or "shift right" as de-

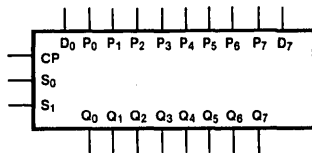
scribed in the Truth Table. All inputs have 50 k Ω pull-down resistors.

Features

- 35% power reduction of the F100141
- 2000V ESD protection
- Pin/function compatible with F100141
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

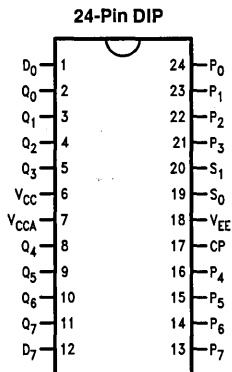
Logic Symbol



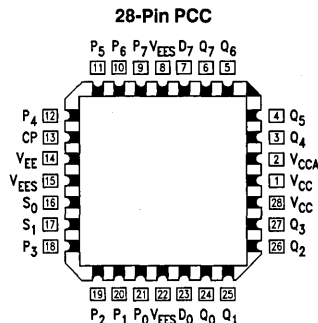
TL/F/9880-1

| Pin Names | Description |
|------------|-----------------|
| CP | Clock Input |
| S_0, S_1 | Select Inputs |
| D_0, D_7 | Serial Inputs |
| P_0-P_7 | Parallel Inputs |
| Q_0-Q_7 | Data Outputs |

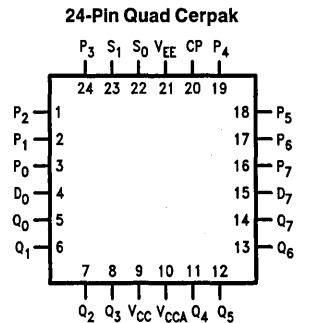
Connection Diagrams



TL/F/9880-2

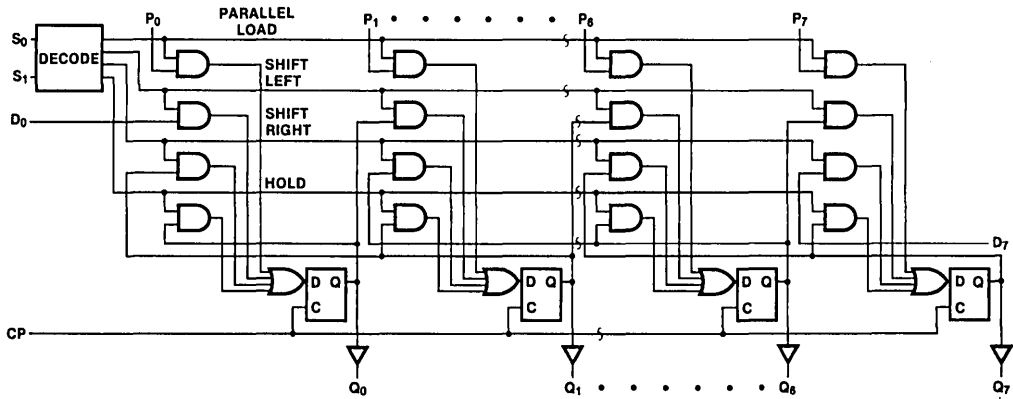


TL/F/9880-4



TL/F/9880-3

Logic Diagram



TL/F/9880-5

Truth Table

| Function | Inputs | | | | | Outputs | | | | | | | |
|---------------|----------------|----------------|----------------|----------------|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | D ₇ | D ₀ | S ₁ | S ₀ | CP | Q ₇ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ | Q ₀ |
| Load Register | X | X | L | L | ↗ | P ₇ | P ₆ | P ₅ | P ₄ | P ₃ | P ₂ | P ₁ | P ₀ |
| Shift Left | X | L | L | H | ↗ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ | Q ₀ | L |
| Shift Left | X | H | L | H | ↗ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H |
| Shift Right | L | X | H | L | ↗ | L | Q ₇ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ |
| Shift Right | H | X | H | L | ↗ | H | Q ₇ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ |
| Hold | X | X | H | H | X | No Change | | | | | | | |
| Hold | X | X | X | X | H | | | | | | | | |
| Hold | X | X | X | X | L | | | | | | | | |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 ↗ = LOW-to-HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|------------------|----------------------|--------------|-------|------------|----------|---|------------------------------|
| | | | | | | | |
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V _{OHc} | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OLc} | Output LOW Voltage | | | -1610 | mV | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for all Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for all Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |
| I _{IH} | Input HIGH Current | | | 240 | μA | V _{IN} = V _{IH} (Max) | |
| I _{EE} | Power Supply Current | -157 -167 | | -75 -75 | mA mA | Inputs Open V _{EE} = -4.2V to -4.8V V _{EE} = -4.2V to -5.7V | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Recommended Operating Conditions

| | |
|------------------------------------|-----------------|
| Case Temperature (T _C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V _{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{max} | Max Clock Frequency | 400 | | 400 | | 400 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.90 | 1.90 | 1.00 | 2.00 | 1.00 | 2.10 | ns | Figures 1 and 3 (Note 1) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.30 | 0.35 | 1.30 | 0.35 | 1.30 | ns | Figures 1 and 3 |
| t_s | Setup Time D_n, P_n S_n | 0.65 1.60 | | 0.65 1.60 | | 0.65 1.60 | | ns | Figure 4 |
| t_h | Hold D_n, P_n S_n | 0.80 0.60 | | 0.80 0.60 | | 0.80 0.60 | | ns | |
| $t_{pw(H)}$ | Pulse Width HIGH CP | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

Note 1: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

PCC and Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{max} | Max Clock Frequency | 425 | | 425 | | 425 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.90 | 1.70 | 1.00 | 1.80 | 1.00 | 1.90 | ns | Figures 1 and 3 (Note 1) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.20 | 0.35 | 1.20 | 0.35 | 1.20 | ns | Figures 1 and 3 |
| t_s | Setup Time D_n, P_n S_n | 0.55 1.50 | | 0.55 1.50 | | 0.55 1.50 | | ns | Figure 4 |
| t_h | Hold Time D_n, P_n S_n | 0.70 0.50 | | 0.70 0.50 | | 0.70 0.50 | | ns | |
| $t_{pw(H)}$ | Pulse Width HIGH CP | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |
| $t_{s, G-G}$ | Skew, Gate to Gate | | TBD | | TBD | | TBD | ns | PCC Only (Note 2) |

Note 1: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Note 2: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version—Preliminary

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|----------------------|-------|-------|---------|---------------------------------|--|---------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Current | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$ | 1, 2, 3 | |
| I_{IH} | Input High Current | | 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ | 1, 2, 3 | |
| | | | 340 | μA | $-55^\circ C$ | $V_{IN} = V_{IH} (Max)$ | | |
| I_{EE} | Power Supply Current | -168 | -55 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3 | |
| | | -178 | -55 | mA | | $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$ | | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$ and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{max} | Max Clock Frequency | 400 | | 400 | | 300 | | MHz | Figures 2 and 3 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.50 | 2.50 | 0.70 | 2.30 | 0.70 | 2.80 | ns | Figures 1 and 3 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.90 | 0.30 | 1.80 | 0.30 | 1.90 | ns | | |
| t_s | Setup Time | | | | | | | | Figure 4 | 4 |
| | D_n, P_n S_n | 0.60 1.70 | | 0.60 1.60 | | 0.60 2.40 | | ns | | |
| t_h | Hold Time | | | | | | | | Figure 4 | 4 |
| | D_n, P_n S_n | 0.90 0.50 | | 0.90 0.50 | | 0.90 0.50 | | ns | | |
| $t_{pw(H)}$ | Pulse Width HIGH | | | | | | | | Figure 3 | 4 |
| | CP | 2.00 | | 2.00 | | 2.00 | | ns | | |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{max} | Max Clock Frequency | 425 | | 425 | | 350 | | MHz | Figures 2 and 3 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.50 | 2.50 | 0.70 | 2.30 | 0.70 | 2.80 | ns | Figures 1 and 3 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.90 | 0.30 | 1.80 | 0.30 | 1.90 | ns | | |
| t_s | Setup Time | | | | | | | | Figure 4 | 4 |
| | D_n, P_n S_n | 0.60 1.70 | | 0.60 1.60 | | 0.60 2.40 | | ns | | |
| t_h | Hold Time | | | | | | | | Figure 4 | 4 |
| | D_n, P_n S_n | 0.90 0.50 | | 0.90 0.50 | | 0.90 0.50 | | ns | | |
| $t_{pw(H)}$ | Pulse Width HIGH | | | | | | | | Figure 3 | 4 |
| | CP | 2.00 | | 2.00 | | 2.00 | | ns | | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specifications which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for the switching of a single output. Delays may vary up to 0.40 ns if multiple outputs are switching simultaneously.

Test Circuitry

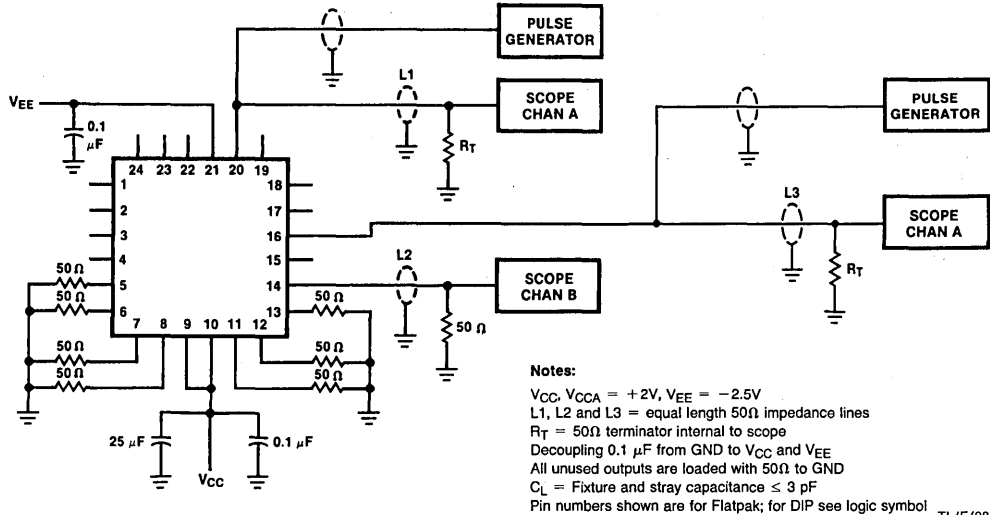
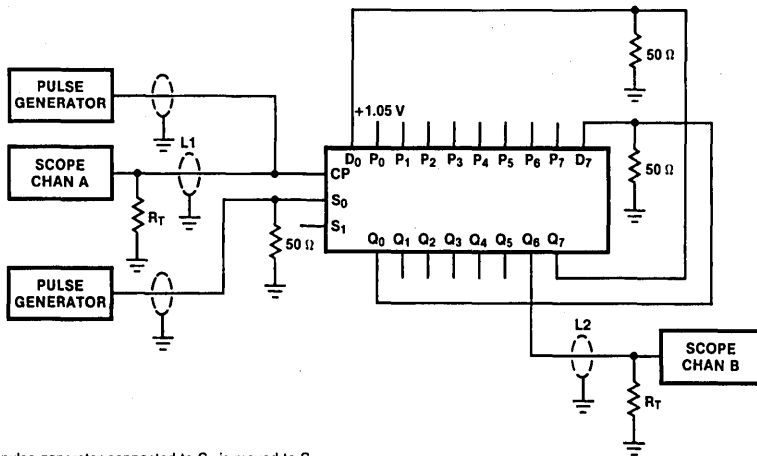


FIGURE 1. AC Test Circuit

TL/F/9880-6



Notes:

For shift right mode pulse generator connected to S_0 is moved to S_1 .

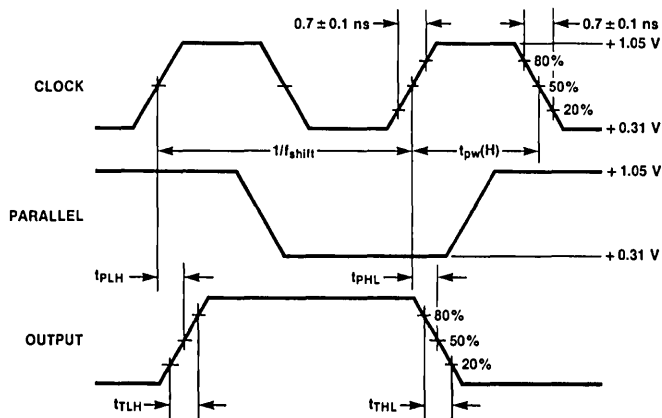
Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.

The feedback path from output to input should be as short as possible.

FIGURE 2. Shift Frequency Test Circuit (Shift Left)

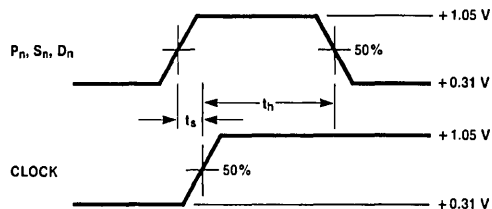
TL/F/9880-7

Switching Waveforms



TL/F/9880-8

FIGURE 3. Propagation Delay and Transition Times



Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

TL/F/9880-9

FIGURE 4. Setup and Hold Times



F100343 Low Power 8-Bit Latch

General Description

The F100343 contains eight D-type latches, individual inputs, (D_n), outputs (Q_n), a common enable pin (\bar{E}), and a latch enable pin (\bar{LE}). A Q output follows its D input when both \bar{E} and \bar{LE} are LOW. When either \bar{E} or \bar{LE} (or both) are HIGH, a latch stores the last valid data present on its D input prior to \bar{E} or \bar{LE} going HIGH.

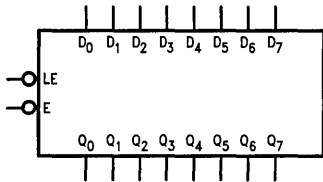
The F100343 outputs are designed to drive a 50Ω termination resistor to $-2.0V$. All inputs have $50\text{ k}\Omega$ pull-down resistors.

Features

- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = $-4.2V$ to $-5.7V$

Ordering Code: See Section 8

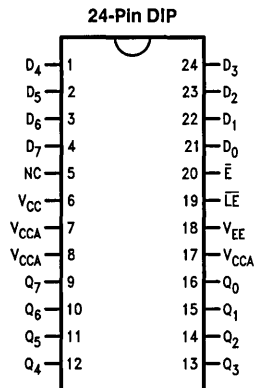
Logic Symbol



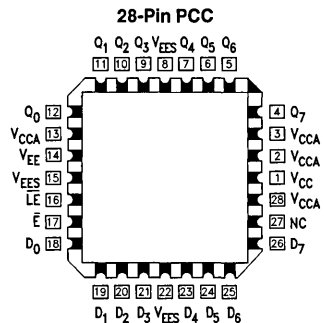
TL/F/10250-1

| Pin Names | Description |
|---------------|--------------------|
| D_0 - D_7 | Data Inputs |
| \bar{E} | Enable Input |
| \bar{LE} | Latch Enable Input |
| Q_0 - Q_7 | Data Inputs |
| NC | No Connect |

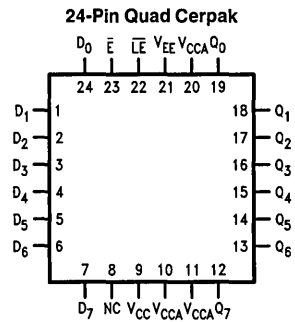
Connection Diagrams



TL/F/10250-2

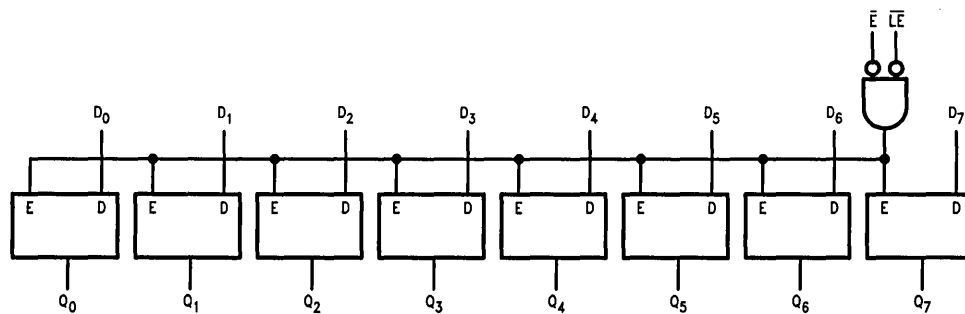


TL/F/10250-4



TL/F/10250-3

Logic Diagram



TU/F/10250-5

Truth Table

| Inputs | | | Outputs |
|----------------|-----------|------------|----------------|
| D _n | \bar{E} | \bar{LE} | Q _n |
| L | L | L | L |
| H | L | L | H |
| X | H | X | Latched* |
| X | X | H | Latched* |

*Retains data present before either \bar{LE} or \bar{E} went HIGH

H = HIGH voltage level

L = LOW voltage level

X = Don't's care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG}) -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J)
 Ceramic $+175^{\circ}\text{C}$
 Plastic $+150^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50 mA

ESD (Note 2) $\geq 2000\text{V}$

Recommended Operating Conditions

Case Temperature (T_C)

Commercial 0°C to $+85^{\circ}\text{C}$
 Military -55°C to $+125^{\circ}\text{C}$

Supply Voltage (V_{EE})

Commercial -5.7V to -4.2V
 Military -5.7V to -4.2V

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ to -5.7V , $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|----------------------|------------|-------|------------|---------------|---|---|
| | | | | | | | |
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH}$ (Max) or V_{IL} (Min) | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}$ (Min) or V_{IL} (Max) | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}$ (Min) | |
| I_{IH} | Input HIGH Current | | | 240 | μA | $V_{IN} = V_{IH}$ (Max) | |
| I_{EE} | Power Supply Current | -95 -97 | | -55 -55 | mA | Inputs Open $V_{EE} = -4.2\text{V}$ to -4.8V $V_{EE} = -4.2\text{V}$ to -5.7V | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ to -5.7V , $V_{CC} = V_{CCA} = \text{GND}$

| Symbol | Parameter | $T_C = 0^{\circ}\text{C}$ | | $T_C = +25^{\circ}\text{C}$ | | $T_C = +85^{\circ}\text{C}$ | | Units | Conditions |
|------------------------|---|---------------------------|------|-----------------------------|------|-----------------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 0.70 | 2.00 | 0.70 | 2.00 | 0.70 | 2.20 | ns | Figures 1, 2, 3 (Note 1) |
| t_{PLH} t_{PHL} | Propagation Delay \overline{LE} , \overline{E} to Output | 1.40 | 2.90 | 1.40 | 2.90 | 1.60 | 3.10 | ns | Figures 1, 2, 3 (Note 1) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 2.00 | 0.45 | 2.00 | ns | Figures 1, 3 |
| t_s | Setup Time D_0 - D_7 | 1.0 | | 1.0 | | 1.1 | | ns | Figures 1, 4 |
| t_h | Hold Time D_0 - D_7 | 0.1 | | 0.1 | | 0.1 | | ns | Figures 1, 4 |
| $t_{pw(H)}$ | Pulse Width HIGH \overline{LE} , \overline{E} | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1, 4 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)

PCC and Cerpack AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 0.70 | 1.80 | 0.70 | 1.80 | 0.70 | 2.00 | ns | Figures 1, 2, 3 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay \overline{LE} , \overline{E} to Output | 1.40 | 2.70 | 1.40 | 2.70 | 1.60 | 2.90 | ns | Figures 1, 2, 3 (Note 2) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.90 | 0.45 | 1.90 | 0.45 | 1.90 | ns | Figures 1, 3 |
| t_s | Setup Time D_0-D_7 | 0.90 | | 0.90 | | 1.00 | | ns | Figures 1, 4 |
| t_h | Hold Time D_0-D_7 | 0.0 | | 0.0 | | 0.0 | | ns | Figures 1, 4 |
| $t_{pw(H)}$ | Pulse Width HIGH \overline{LE} , \overline{E} | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1, 4 |
| $t_{S, G-G}$ | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version — Preliminary

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|---------------------|-------|-------|---------|---------------------------------|--|------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$ | 1, 2, 3 | |

Military Version — Preliminary (Continued)

DC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes |
|----------|----------------------|--------------|------------|---------|---------------------------------|---|---------|
| I_{IH} | Input HIGH Current | | 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | 1, 2, 3 |
| | | | 340 | μA | $-55^\circ C$ | | |
| I_{EE} | Power Supply Current | -100 -105 | -35 -35 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$ | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 0.50 | 2.70 | 0.50 | 2.30 | 0.50 | 2.80 | ns | Figures 1, 2, 3 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay \overline{LE} , \overline{E} to Output | 0.90 | 3.40 | 1.0 | 3.10 | 1.10 | 3.90 | ns | Figures 1, 2, 3 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | Figures 1, 3 | 4 |
| t_s | Setup Time D_0-D_7 | 0.60 | | 0.60 | | 0.60 | | ns | Figures 1, 4 | 4 |
| t_h | Hold Time D_0-D_7 | 1.50 | | 1.50 | | 1.70 | | ns | Figures 1, 4 | 4 |
| $t_{pw(H)}$ | Pulse Width HIGH \overline{LE} , \overline{E} | 2.40 | | 2.40 | | 2.40 | | ns | Figures 1, 4 | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version — Preliminary (Continued)

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 0.50 | 2.70 | 0.50 | 2.30 | 0.50 | 2.80 | ns | Figures 1, 2, 3 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay $\overline{LE}, \overline{E}$ to Output | 0.90 | 3.40 | 1.0 | 3.10 | -1.10 | 3.90 | ns | Figures 1, 2, 3 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | Figures 1, 3 | 4 |
| t_s | Setup Time D_0-D_7 | 0.60 | | 0.60 | | 0.60 | | ns | Figures 1, 4 | 4 |
| t_h | Hold Time D_0-D_7 | 1.50 | | 1.50 | | 1.50 | | ns | Figures 1, 4 | 4 |
| $t_{pw(H)}$ | Pulse Width HIGH $\overline{LE}, \overline{E}$ | 2.40 | | 2.40 | | 2.40 | | ns | Figures 1, 4 | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

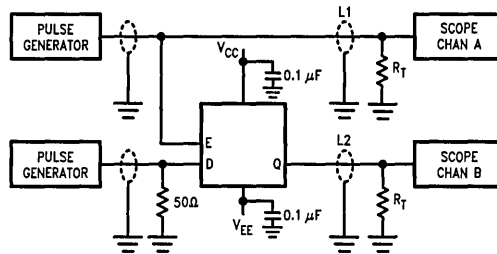


FIGURE 1. AC Test Circuit

TL/F/10250-6

Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = equal length 50 Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 µF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50 Ω to GND

$C_L =$ Fixture and stray capacitance ≤ 3 pF

Switching Waveforms

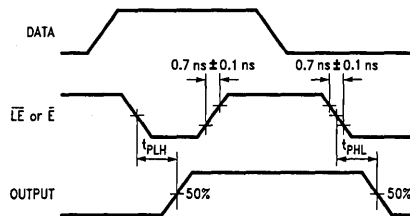


FIGURE 2. Propagation Delays

TL/F/10250-7

Switching Waveforms (Continued)

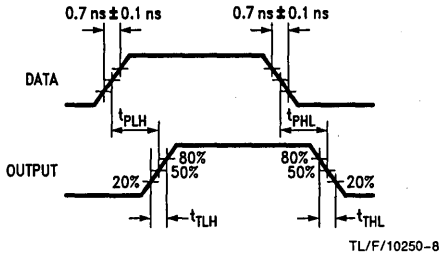


FIGURE 3. Propagation and Transition Times

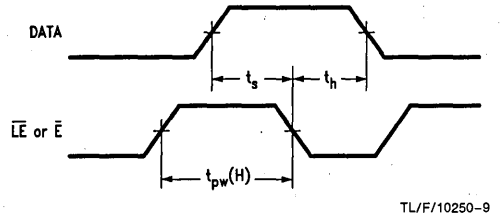


FIGURE 4. Setup, Hold and Pulse Width Times

F100344

Low Power 8-Bit Latch with Cut-Off Drivers

General Description

The F100344 contains eight D-type latches, individual inputs (D_n), outputs (Q_n), a common enable pin (\bar{E}), latch enable (\bar{LE}), and output enable pin (\bar{OEN}). A Q output follows its D input when both \bar{E} and \bar{LE} are LOW. When either \bar{E} or \bar{LE} (or both) are HIGH, a latch stores the last valid data present on its D input prior to \bar{E} or \bar{LE} going HIGH.

A HIGH on \bar{OEN} holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is $-2.0V$, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

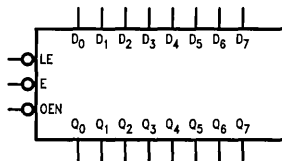
The F100344 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have $50\text{ k}\Omega$ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = $-4.2V$ to $-5.7V$

Ordering Code: See Section 8

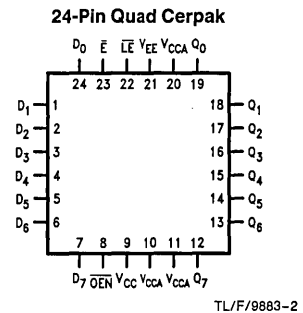
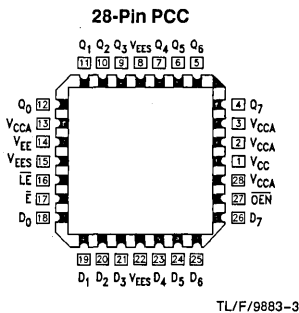
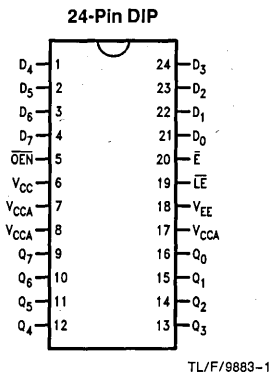
Logic Symbol



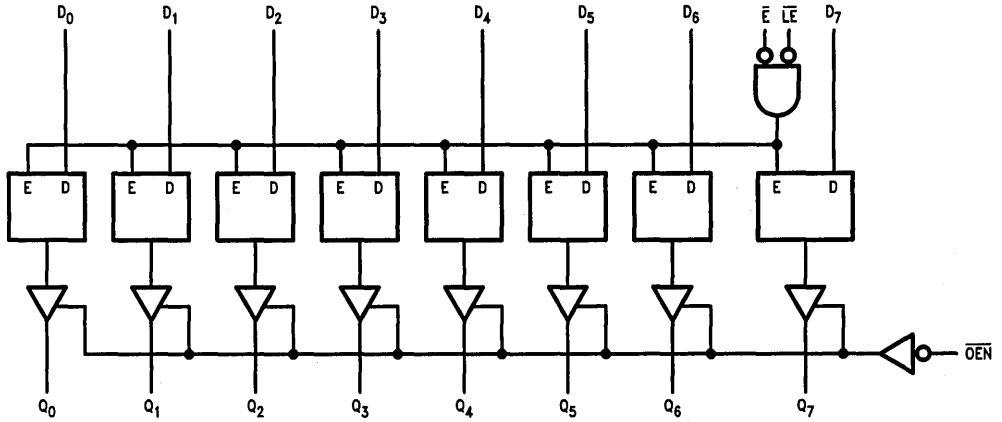
TL/F/9883-4

| Pin Names | Description |
|---------------|---------------------|
| D_0 - D_7 | Data Inputs |
| \bar{E} | Enable Input |
| \bar{LE} | Latch Enable Input |
| \bar{OEN} | Output Enable Input |
| Q_0 - Q_7 | Data Outputs |

Connection Diagrams



Logic Diagram



TL/F/9883-5

Truth Table

| Inputs | | | | Outputs |
|----------------|-----------|------------|-------------|----------------|
| D _n | \bar{E} | \bar{LE} | \bar{OEN} | Q _n |
| L | L | L | L | L |
| H | L | L | L | H |
| X | H | X | L | Latched* |
| X | X | H | L | Latched* |
| X | X | X | H | Cutoff |

*Retains data present before either \bar{LE} or \bar{E} go HIGH.

- H = HIGH Voltage level
- L = LOW Voltage level
- Cutoff = lower-than-LOW state
- X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |
| Output Current (DC Output HIGH) | -100 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|------------------------------------|-----------------|
| Case Temperature (T _C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V _{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-------------------|----------------------|--------------|-------|------------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 25Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 25Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | mV | | |
| V _{OL} Z | Cutoff LOW Voltage | | | -1950 | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | \overline{OEN} = HIGH |
| V _{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |
| I _{IH} | Input HIGH Current | | | 240 | μA | V _{IN} = V _{IH} (Max) | |
| I _{EE} | Power Supply Current | -178 -185 | | -85 -85 | mA | Inputs Open V _{EE} = -4.2V to -4.8V V _{EE} = -4.2V to -5.7V | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND

| Symbol | Parameter | T _C = 0°C | | T _C = +25°C | | T _C = +85°C | | Units | Conditions |
|--------------------------------------|---|----------------------|------|------------------------|------|------------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay D _n to Output | 0.90 | 2.10 | 0.90 | 2.10 | 1.00 | 2.30 | ns | Figures 1, 2 (Note 1) |
| t _{PLH} t _{PHL} | Propagation Delay \overline{LE} , \overline{E} to Output | 1.60 | 3.10 | 1.60 | 3.10 | 1.80 | 3.40 | ns | Figures 1, 2 (Note 1) |
| t _{PZH} t _{PHZ} | Propagation Delay \overline{OEN} to Output | 1.60 | 4.20 | 1.60 | 4.20 | 1.60 | 4.20 | ns | Figures 1, 2 (Note 1) |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 2.00 | 0.45 | 2.00 | ns | Figures 1, 3 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** (Continued) $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|-------------|---------------------------|-------------------|-----|---------------------|-----|---------------------|-----|-------|--------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_s | Setup Time D_0-D_7 | 1.0 | | 1.0 | | 1.1 | | ns | Figures 1, 3 |
| t_h | Hold Time D_0-D_7 | 0.1 | | 0.1 | | 0.1 | | ns | Figures 1, 3 |
| $t_{pw(H)}$ | Pulse Width HIGH LE, E | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1, 3 |

PCC and Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 0.90 | 1.90 | 0.90 | 1.90 | 1.00 | 2.10 | ns | Figures 1, 2 (Note 2) |
| t_{PLH} t_{PHL} | Propagation Delay LE, E to Output | 1.60 | 2.90 | 1.60 | 2.90 | 1.80 | 3.20 | ns | Figures 1, 2 (Note 2) |
| t_{PZH} t_{PHZ} | Propagation Delay OEN to Output | 1.60 | 4.00 | 1.60 | 4.00 | 1.60 | 4.00 | ns | Figures 1, 2 (Note 2) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.90 | 0.45 | 1.90 | 0.45 | 1.90 | ns | Figures 1, 3 |
| t_s | Setup Time D_0-D_7 | 0.90 | | 0.90 | | 1.00 | | ns | Figures 1, 3 |
| t_h | Hold Time D_0-D_7 | 0.0 | | 0.0 | | 0.0 | | ns | Figures 1, 3 |
| $t_{pw(H)}$ | Pulse Width HIGH LE, E | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1, 3 |
| $t_s, G-G$ | Skew, Gate to Gate | | TBD | | TBD | | TBD | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version—Preliminary**DC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | | Notes |
|-----------|---------------------|-------|-------|-------|-------------------------------|--|---------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 25Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 25Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | | -1555 | mV | $-55^\circ C$ | | | |

Military Version—Preliminary (Continued)**DC Electrical Characteristics** (Continued)
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|----------------------|--------------|------------|---------|-----------------|---|-------------------------|---------|
| V_{OLZ} | Cutoff LOW Voltage | | -1950 | mV | 0°C to +125°C | $V_{IN} = V_{IH}$ (MIN) or V_{IL} (Max) | $\overline{OEN} = HIGH$ | 1, 2, 3 |
| | | | -1850 | | -55°C | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | -55°C to +125°C | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | -55°C to +125°C | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | -55°C to +125°C | $V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min) | 1, 2, 3 | |
| I_{IH} | Input HIGH Current | | 240 | μA | 0°C to +125°C | $V_{EE} = -5.7V$ $V_{IN} = V_{IH}$ (Max) | 1, 2, 3 | |
| | | | 340 | μA | -55°C | | | |
| I_{EE} | Power Supply Current | -195 -205 | -65 -65 | mA | -55°C to +125°C | Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$ | 1, 2, 3 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|--------------|---------------------|--------------|----------------------|--------------|-------|--------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 0.50 | 2.60 | 0.70 | 2.60 | 0.70 | 3.10 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay \overline{LE} , \overline{E} to Output | 0.80 | 3.30 | 1.00 | 3.30 | 1.10 | 4.80 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{PZH} t_{PHZ} | Propagation Delay \overline{OEN} to Output | 1.00 0.70 | 4.00 3.00 | 1.10 0.70 | 3.80 2.80 | 1.20 0.70 | 4.70 3.20 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | Figures 1, 3 | 4 |
| t_s | Setup Time D_0-D_7 | 1.50 | | 1.50 | | 1.70 | | ns | Figures 1, 3 | 4 |
| t_h | Hold Time D_0-D_7 | 0.60 | | 0.60 | | 0.60 | | ns | Figures 1, 3 | 4 |
| $t_{pw}(H)$ | Pulse Width HIGH \overline{LE} , \overline{E} | 2.40 | | 2.40 | | 2.40 | | ns | Figures 1, 3 | 4 |

Military Version—Preliminary (Continued)

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|--------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 0.50 | 2.60 | 0.70 | 2.60 | 0.70 | 3.10 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{PLH} t_{PHL} | Propagation Delay \overline{LE} , \overline{E} to Output | 0.80 | 3.30 | 1.10 | 3.30 | 1.10 | 4.80 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{PZH} t_{PHZ} | Propagation Delay \overline{OEN} to Output | 1.00 | 4.00 | 1.10 | 3.80 | 1.20 | 4.70 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | Figures 1, 3 | 4 |
| t_s | Setup Time D_0-D_7 | 1.50 | | 1.50 | | 1.70 | | ns | Figures 1, 3 | 4 |
| t_h | Hold Time D_0-D_7 | 0.60 | | 0.60 | | 0.60 | | ns | Figures 1, 3 | 4 |
| $t_{pw}(H)$ | Pulse Width HIGH \overline{LE} , \overline{E} | 2.40 | | 2.40 | | 2.40 | | ns | Figures 1, 3 | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

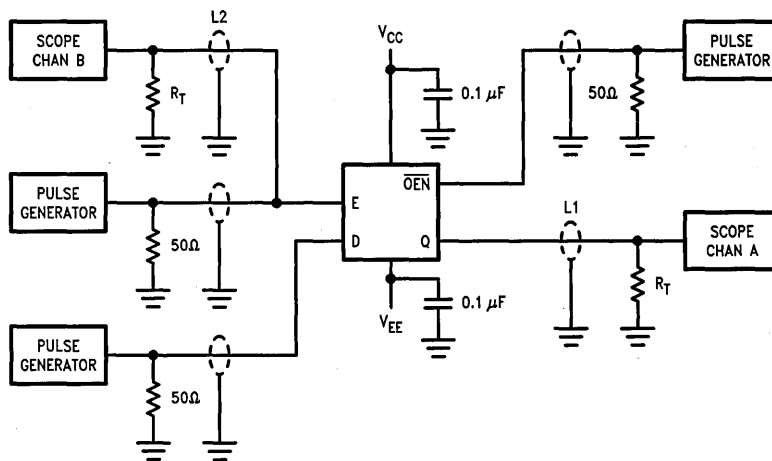
Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry



Notes:

V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$

L1 and L2 = equal length 50 Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μF from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50 Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

TL/F/9883-6

Switching Waveforms

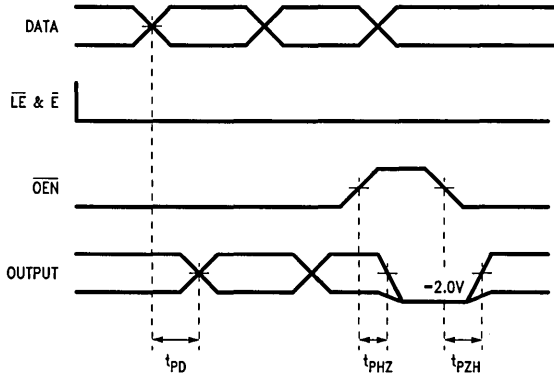


FIGURE 2. Propagation Delay and Cutoff Times

TL/F/9883-7

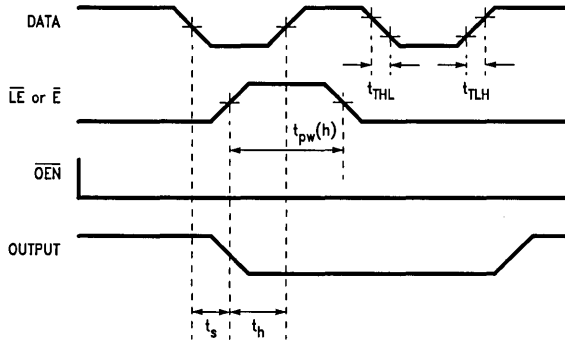


FIGURE 3. Setup, Hold and Pulse Width Times

TL/F/9883-8

F100350 Low Power Hex D-Latch

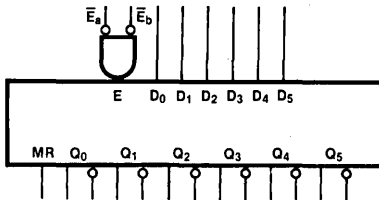
General Description

The F100350 contains six D-type latches with true and complement outputs, a pair of common Enables (\bar{E}_a and \bar{E}_b), and a common Master Reset (MR). A Q output follows its D input when both \bar{E}_a and \bar{E}_b are LOW. When either \bar{E}_a or \bar{E}_b (or both) are HIGH, a latch stores the last valid data present on its D input before \bar{E}_a or \bar{E}_b went HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 k Ω pull-down resistors.

Features

- 20% power reduction of the F100150
- 2000V ESD protection
- Pin/function compatible with F100150
- Voltage compensated operating range = -4.2V to -5.7V

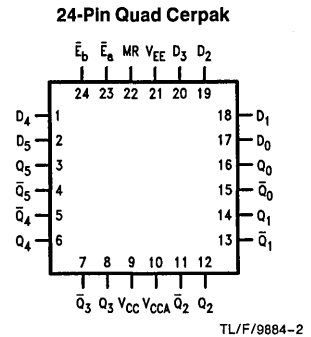
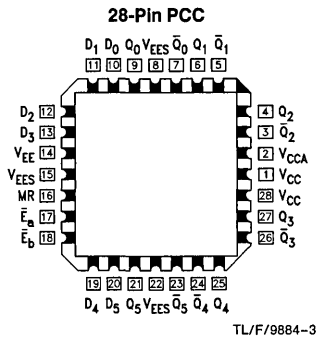
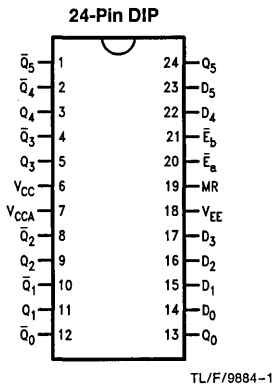
Logic Symbol



TL/F/9884-10

| Pin Names | Description |
|--------------------------------|-----------------------------------|
| D ₀ -D ₅ | Data Inputs |
| \bar{E}_a , \bar{E}_b | Common Enable Inputs (Active LOW) |
| MR | Asynchronous Master Reset Input |
| Q ₀ -Q ₅ | Data Outputs |
| \bar{Q}_0 - \bar{Q}_5 | Complementary Data Outputs |

Connection Diagrams



F100351

Low Power Hex D Flip-Flop

General Description

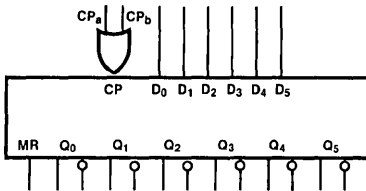
The F100351 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 k Ω pull-down resistors.

Features

- 40% power reduction of the F100151
- 2000V ESD protection
- Pin/function compatible with F100151
- Voltage compensated operating range: -4.2V to -5.7V

Ordering Code: See Section 8

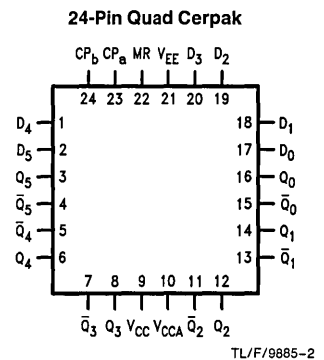
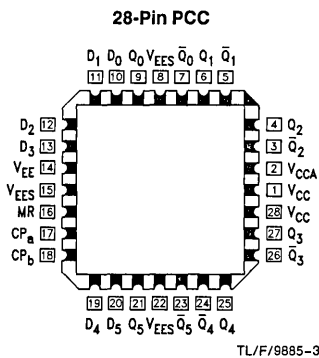
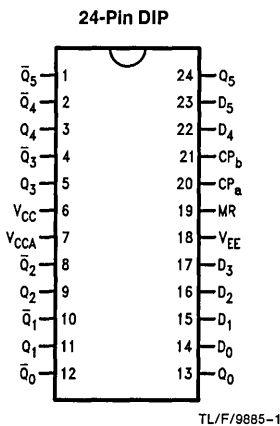
Logic Symbol



TL/F/9885-11

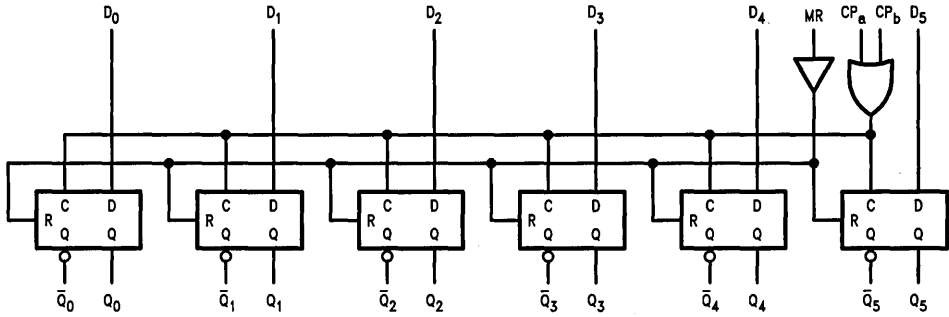
| Pin Names | Description |
|-----------------------------------|---------------------------------|
| D ₀ –D ₅ | Data Inputs |
| CP _a , CP _b | Common Clock Inputs |
| MR | Asynchronous Master Reset Input |
| Q ₀ –Q ₅ | Data Outputs |
| \bar{Q}_0 – \bar{Q}_5 | Complementary Data Outputs |

Connection Diagrams



2

Logic Diagram



TL/F/9885-4

Truth Tables (Each Flip-flop)

Synchronous Operation

| Inputs | | | | Outputs |
|--------|--------|--------|----|------------|
| D_n | CP_a | CP_b | MR | $Q_n(t+1)$ |
| L | ↗ | L | L | L |
| H | ↗ | L | L | H |
| L | L | ↗ | L | L |
| H | L | ↗ | L | H |
| X | H | ↗ | L | $Q_n(t)$ |
| X | ↗ | H | L | $Q_n(t)$ |
| X | L | L | L | $Q_n(t)$ |

Asynchronous Operation

| Inputs | | | | Outputs |
|--------|--------|--------|----|------------|
| D_n | CP_a | CP_b | MR | $Q_n(t+1)$ |
| X | X | X | H | L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 t = Time before CP positive transition
 t+1 = Time after CP positive transition
 ↗ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|------------------------------------|-----------------|
| Case Temperature (T _C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V _{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-------------------|---|-------|-------|-------------------|-------|---|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs |
| V _{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) |
| I _{IH} | Input HIGH Current MR D ₀ -D ₅ CP _a , CP _b | | | 350 240 350 | μA | V _{IN} = V _{IH} (Max) |
| I _{EE} | Power Supply Current | -129 | | -62 | mA | Inputs Open |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND

| Symbol | Parameter | T _C = 0°C | | T _C = +25°C | | T _C = +85°C | | Units | Conditions |
|--------------------------------------|--|----------------------|------|------------------------|------|------------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f _{max} | Toggle Frequency | 375 | | 375 | | 375 | | MHz | Figures 2 and 3 |
| t _{PLH} t _{PHL} | Propagation Delay CP _a , CP _b to Output | 0.80 | 2.00 | 0.80 | 2.0 | 0.90 | 2.10 | ns | Figures 1 and 3 |
| t _{PLH} t _{PHL} | Propagation Delay MR to Output | 1.10 | 2.30 | 1.10 | 2.30 | 1.20 | 2.40 | ns | Figures 1 and 4 |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.70 | 0.45 | 1.80 | ns | Figures 1 and 3 |

Commercial Version (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** (Continued) $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|-------------|--|-------------------|-----|---------------------|-----|---------------------|-----|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_s | Setup Time D_0 - D_5 | 0.40 | | 0.40 | | 0.40 | | ns | Figure 5 |
| | MR (Release Time) | 1.60 | | 1.60 | | 1.60 | | | Figure 4 |
| t_h | Hold Time D_0 - D_5 | 1.00 | | 1.00 | | 1.00 | | ns | Figure 5 |
| $t_{pw(H)}$ | Pulse Width HIGH CP_a , CP_b , MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 |

PCC and Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{max} | Toggle Frequency | 375 | | 375 | | 375 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP_a , CP_b to Output | 0.80 | 1.80 | 0.80 | 1.80 | 0.90 | 1.90 | ns | Figures 1 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 1.10 | 2.10 | 1.10 | 2.10 | 1.20 | 2.20 | ns | Figures 1 and 4 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.60 | 0.45 | 1.70 | ns | Figures 1 and 3 |
| t_s | Setup Time D_0 - D_5 | 0.30 | | 0.30 | | 0.30 | | ns | Figure 5 |
| | MR (Release Time) | 1.50 | | 1.50 | | 1.50 | | | Figure 4 |
| t_h | Hold Time D_0 - D_5 | 0.90 | | 0.90 | | 0.90 | | ns | Figure 5 |
| $t_{pw(H)}$ | Pulse Width HIGH CP_a , CP_b , MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 |
| $t_{s, G-G}$ | Skew, Gate-to-Gate | | TBD | | TBD | | TBD | ps | (PCC only) (Note 1) |

Note 1: Gate-to-gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version—Preliminary**DC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | | Notes |
|-----------|---------------------|-------|-------|-------|-------------------------------|--|---------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | | -1555 | mV | $-55^\circ C$ | | | |

Military Version—Preliminary (Continued)

DC Electrical Characteristics (Continued)

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^{\circ}C$ to $+125^{\circ}C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes |
|----------|---|-------|-------------------|---------|-----------------------------------|---|------------|
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^{\circ}C$ to $+125^{\circ}C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^{\circ}C$ to $+125^{\circ}C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^{\circ}C$ to $+125^{\circ}C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$ | 1, 2, 3 |
| I_{IH} | Input HIGH Current | | | | | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | 1, 2, 3 |
| | MR D ₀ -D ₅ CP _a , CP _b | | 300 250 520 | μA | $0^{\circ}C$ to $+125^{\circ}C$ | | |
| I_{IH} | MR D ₀ -D ₅ CP _a , CP _b | | 450 350 750 | μA | $-55^{\circ}C$ | | |
| | Power Supply Current | -146 | -96 | mA | $-55^{\circ}C$ to $+125^{\circ}C$ | Inputs Open | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^{\circ}C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^{\circ}C$ | | $T_C = +25^{\circ}C$ | | $T_C = +125^{\circ}C$ | | Units | Conditions | Notes |
|------------------------|--|----------------------|------|----------------------|------|-----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{max} | Toggle Frequency | 375 | | 375 | | 375 | | MHz | Figures 2 and 3 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP _a , CP _b to Output | 0.80 | 2.20 | 0.80 | 2.20 | 0.90 | 2.40 | ns | Figures 1 and 3 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 1.20 | 2.90 | 1.30 | 3.00 | 1.20 | 3.10 | ns | Figures 1 and 4 | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.70 | 0.45 | 1.80 | ns | Figures 1 and 3 | 4 |
| t_s | Setup Time D ₀ -D ₅ | 0.70 | | 0.70 | | 0.70 | | ns | Figure 5 | |
| | MR (Release Time) | 2.30 | | 2.30 | | 2.60 | | | Figure 4 | |
| t_h | Hold Time D ₀ -D ₅ | 0.70 | | 0.70 | | 0.70 | | ns | Figure 5 | |
| $t_{pw(H)}$ | Pulse Width HIGH CP _a , CP _b , MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 | |

Military Version—Preliminary (Continued)

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|--|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{max} | Toggle Frequency | 375 | | 375 | | 375 | | MHz | Figures 2 and 3 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP _a , CP _b to Output | 0.80 | 2.00 | 0.80 | 2.00 | 0.90 | 2.20 | ns | Figures 1 and 3 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 1.20 | 2.70 | 1.30 | 2.80 | 1.20 | 2.90 | ns | Figures 1 and 4 | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.60 | 0.45 | 1.70 | ns | Figures 1 and 3 | 4 |
| t_s | Setup Time D ₀ -D ₅ | 0.60 | | 0.60 | | 0.60 | | ns | Figure 5 | |
| | MR (Release Time) | 2.20 | | 2.20 | | 2.50 | | | Figure 4 | |
| t_h | Hold Time D ₀ -D ₅ | 0.60 | | 0.60 | | 0.60 | | ns | Figure 5 | |
| $t_{pw(H)}$ | Pulse Width HIGH CP _a , CP _b , MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$, Temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table 1) on each Mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$, and $-55^\circ C$ Temperature, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$ and $-55^\circ C$ Temperature (design characterization data).

Test Circuitry

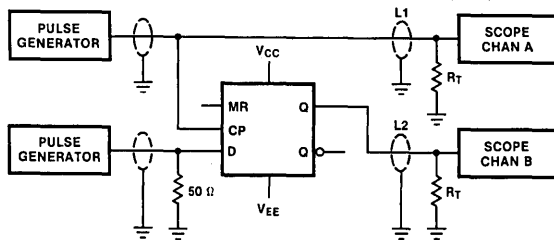


FIGURE 1. AC Test Circuit

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance $\leq 3 pF$

TL/F 9885-5

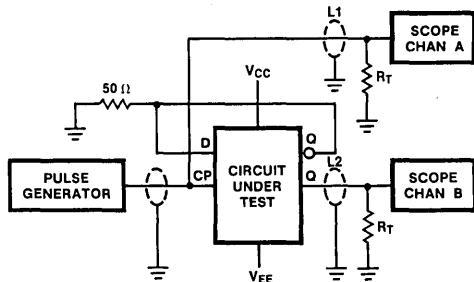


FIGURE 2. Toggle Frequency Test Circuit

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Jig and stray capacitance $\leq 3 pF$

TL/F 9885-6

Switching Waveforms

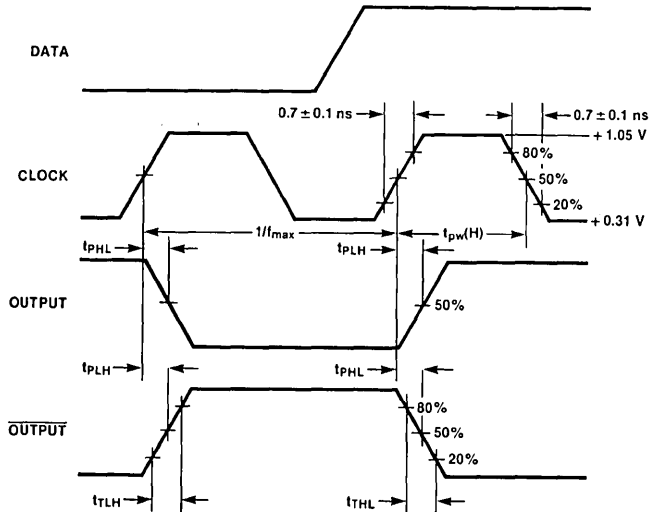


FIGURE 3. Propagation Delay (Clock) and Transition Times

TL/F/9885-7

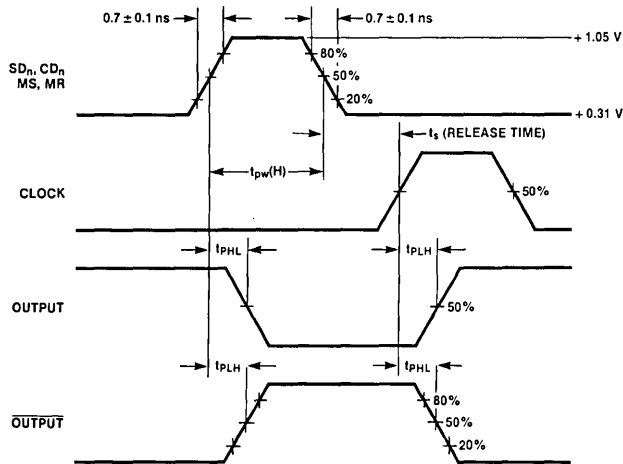
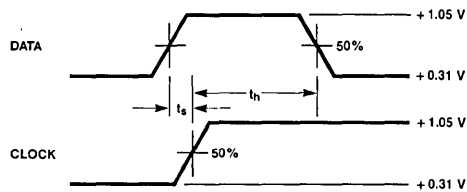


FIGURE 4. Propagation Delay (Reset)

TL/F/9885-8



TL/F/9885-9

Notes:

- t_s is the minimum time before the transition of the clock that information must be present at the data input.
- t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time



F100352

Low Power 8-Bit Buffer with Cut-Off Drivers

General Description

The F100352 contains an 8-bit buffer, individual inputs (D_n), outputs (Q_n), and a data output enable pin (\overline{OEN}). A Q output follows its D input when the \overline{OEN} pin is LOW. A HIGH on \overline{OEN} holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is $-2.0V$, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

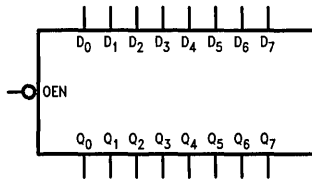
The F100352 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have $50\text{ k}\Omega$ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = $-4.2V$ to $-5.7V$

Ordering Code: See Section 8

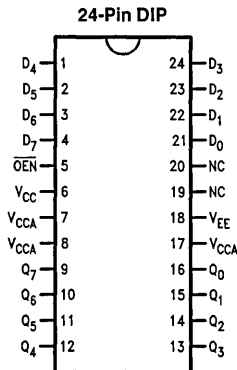
Logic Symbol



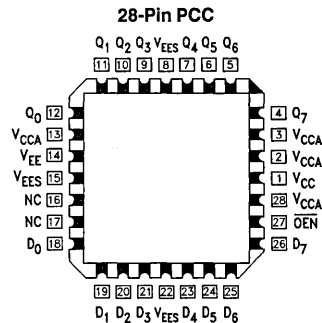
TL/F/10248-1

| Pin Names | Description |
|------------------|---------------------|
| D_0 – D_7 | Data Inputs |
| \overline{OEN} | Output Enable Input |
| Q_0 – Q_7 | Data Outputs |
| NC | No Connect |

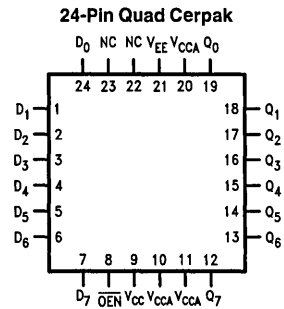
Connection Diagrams



TL/F/10248-2

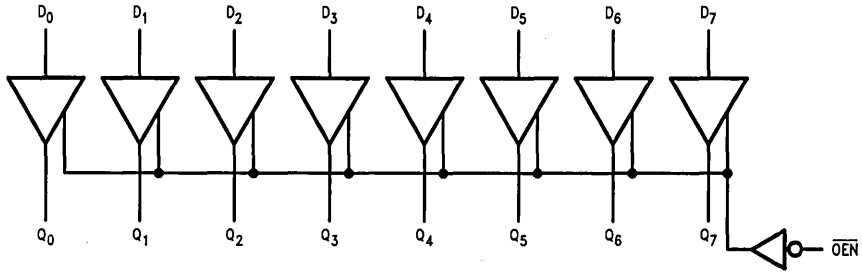


TL/F/10248-4



TL/F/10248-3

Logic Diagram



TL/F/10248-5

Truth Table

| Inputs | | Outputs |
|--------|-------------------------|---------|
| Dn | $\overline{\text{OEN}}$ | Qn |
| L | L | L |
| H | L | H |
| X | H | Cutoff |

H = HIGH Voltage Level
 L = LOW Voltage Level
 Cutoff = Lower-than-LOW State
 X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG}) -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J)
 Ceramic $+175^{\circ}\text{C}$
 Plastic $+150^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -100 mA

ESD (Note 2) $\geq 2000\text{V}$

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$ to -5.7V , $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|----------------------|------------------|---------|----------------|---------------|---|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ Loading with 25Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ Loading with 25Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | |
| V_{OLZ} | Cut-Off LOW Voltage | | | -1950 | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ $\overline{\text{OEN}} = \text{HIGH}$ |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ |
| I_{IH} | Input HIGH Current | | | 240 | μA | $V_{IN} = V_{IH}(\text{Max})$ |
| I_{EE} | Power Supply Current | -138 -143 | | -70 -70 | mA | Inputs Open $V_{EE} = -4.2\text{V}$ to -4.8V $V_{EE} = -4.2\text{V}$ to -5.7V |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Recommended Operating Conditions

Case Temperature (T_C)
 Commercial 0°C to $+85^{\circ}\text{C}$
 Military -55°C to $+125^{\circ}\text{C}$

Supply Voltage (V_{EE})
 Commercial -5.7V to -4.2V
 Military -5.7V to -4.2V

Commercial Version (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Dn to Output | 0.70 | 2.00 | 0.70 | 2.00 | 0.70 | 2.20 | ns | Figures 1, 2 (Note 1) |
| t_{PZH} t_{PHZ} | Propagation Delay \overline{OEN} to Output | 1.60 | 4.20 | 1.60 | 4.20 | 1.60 | 4.20 | ns | Figures 1, 2 (Note 1) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 2.00 | 0.45 | 2.00 | ns | Figures 1, 2 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.**PCC and Cerpak AC Electrical Characteristics** $V_{EE} = 4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Dn to Output | 0.70 | 1.80 | 0.70 | 1.80 | 0.70 | 2.00 | ns | Figures 1, 2 (Note 2) |
| t_{PZH} t_{PHZ} | Propagation Delay \overline{OEN} to Output | 1.60 | 4.00 | 1.60 | 4.00 | 1.60 | 4.00 | ns | Figures 1, 2 (Note 2) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.90 | 0.45 | 1.90 | 0.45 | 1.90 | ns | Figures 1, 2 |
| $t_{S,G-G}$ | Skew, Gate to Gate | | TBD | | TBD | | TBD | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.**Note 2:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version—Preliminary

DC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ\text{C to } +125^\circ\text{C}$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|----------------------|--------------|-------|---------------|--|---|---------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ\text{C to } +125^\circ\text{C}$ | $V_{IN} = V_{IH(\text{Max})}$ or $V_{IL(\text{Min})}$ | Loading with 25Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | -55°C | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ\text{C to } +125^\circ\text{C}$ | $V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$ | Loading with 25Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | -55°C | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ\text{C to } +125^\circ\text{C}$ | $V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$ | Loading with 25Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | -55°C | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ\text{C to } +125^\circ\text{C}$ | $V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$ | Loading with 25Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | -55°C | | | |
| V_{OLZ} | Cut-Off LOW Voltage | | -1950 | mV | $0^\circ\text{C to } +125^\circ\text{C}$ | $V_{IN} = V_{IH(\text{Min})}$, or $V_{IL(\text{Max})}$ | $\overline{OEN} = \text{HIGH}$ | 1, 2, 3 |
| | | | -1850 | | -55°C | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ\text{C to } +125^\circ\text{C}$ | Guaranteed HIGH signal for All inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ\text{C to } +125^\circ\text{C}$ | Guaranteed LOW signal for All inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ\text{C to } +125^\circ\text{C}$ | $V_{EE} = 4.2V$ $V_{IN} = V_{IL(\text{Min})}$ | 1, 2, 3 | |
| I_{IH} | Input HIGH Current | | 240 | μA | $0^\circ\text{C to } +125^\circ\text{C}$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH(\text{Max})}$ | 1, 2, 3 | |
| | | | 340 | μA | -55°C | | | |
| I_{EE} | Power Supply Current | -145 -150 | -55 | mA | $-55^\circ\text{C to } +125^\circ\text{C}$ | Inputs Open $V_{EE} = -4.2V \text{ to } -4.8V$ $V_{EE} = -4.2V \text{ to } -5.7V$ | 1, 2, 3 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at -55°C , $+25^\circ\text{C}$, and $+125^\circ\text{C}$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at -55°C , $+25^\circ\text{C}$, and $+125^\circ\text{C}$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C + 125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|--------------|---------------------|--------------|---------------------|--------------|-------|--------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Dn to Output | 0.30 | 2.60 | 0.50 | 2.40 | 0.50 | 2.70 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{PZH} t_{PHZ} | Propagation Delay \overline{OEN} to Output | 1.20 0.70 | 5.00 3.00 | 1.40 0.70 | 4.20 2.80 | 1.20 0.70 | 4.30 3.20 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | Figures 1, 2 | 4 |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C + 125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|--------------|---------------------|--------------|---------------------|--------------|-------|--------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay Dn to Output | 0.30 | 2.60 | 0.50 | 2.40 | 0.50 | 2.70 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{PZH} t_{PHZ} | Propagation Delay \overline{OEN} to Output | 1.20 0.70 | 5.00 3.00 | 1.40 0.70 | 4.20 2.80 | 1.20 0.70 | 4.30 3.20 | ns | Figures 1, 2 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | Figures 1, 2 | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

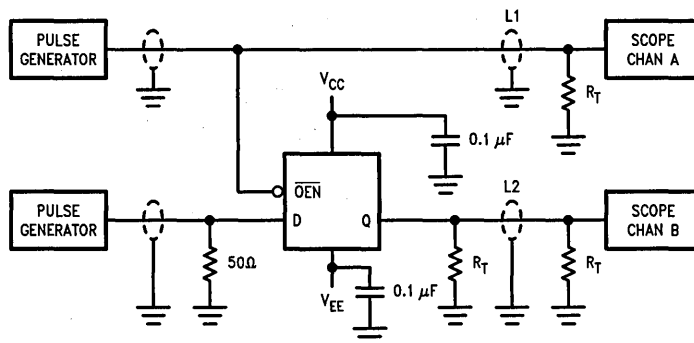


FIGURE 1. AC Test Circuit

TL/F/10248-6

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

Switching Waveforms

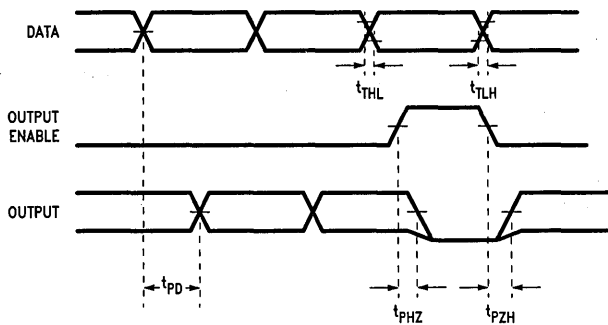


FIGURE 2. Propagation Delay, Cut-Off and Transition Times

TL/F/10248-7

F100353 Low Power 8-Bit Register

General Description

The F100353 contains eight D-type edge triggered, master/slave flip-flops with individual inputs (D_n), true outputs (Q_n), a clock input (CP), and a common clock enable pin (\overline{CEN}). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the \overline{CEN} input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

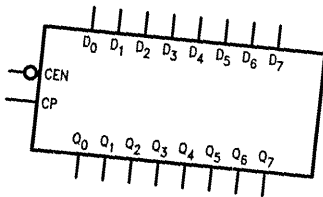
The F100353 output drivers are designed to drive 50 Ω termination to -2.0V. All inputs have 50 k Ω pull-down resistors.

Features

- ▣ Low power operation
- ▣ 2000V ESD protection
- ▣ Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

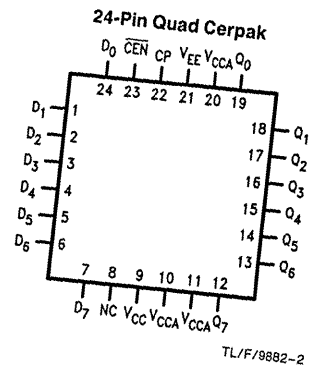
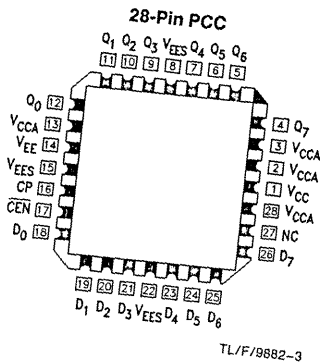
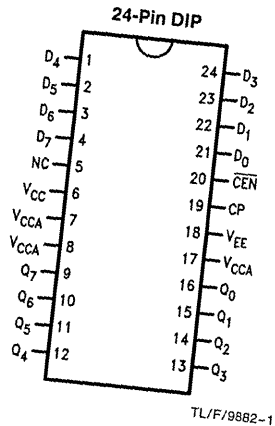
Logic Symbol



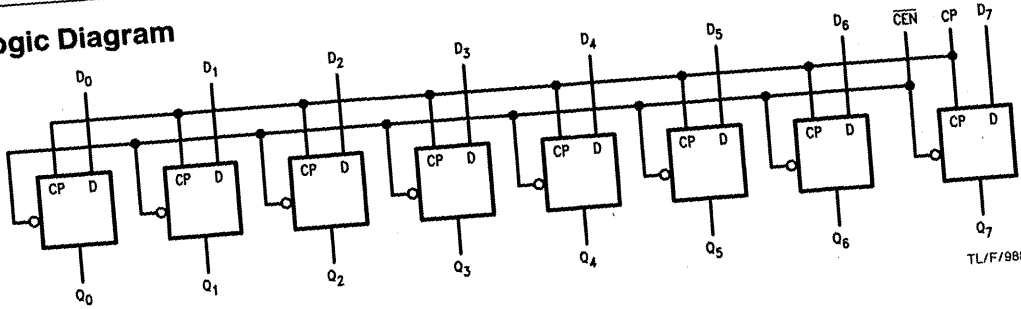
TL/F/9882-4

| Pin Names | Description |
|------------------|----------------------------------|
| D_0 - D_7 | Data Inputs |
| \overline{CEN} | Clock Enable Input |
| CP | Clock Input (Active Rising Edge) |
| Q_0 - Q_7 | Data Outputs |
| NC | No Connect |

Connection Diagrams



Logic Diagram



Truth Table

| Inputs | | | Outputs |
|--------|------------------|----|---------|
| D_n | \overline{CEN} | CP | Q_n |
| L | L | ↗ | L |
| H | L | ↗ | H |
| X | X | L | NC |
| X | X | H | NC |
| X | H | X | NC |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 NC = No Change
 ↗ = LOW to HIGH Transition

F100353 Low Power 8-Bit Register

General Description

The F100353 contains eight D-type edge triggered, master/slave flip-flops with individual inputs (D_n), true outputs (Q_n), a clock input (CP), and a common clock enable pin (\overline{CEN}). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the \overline{CEN} input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

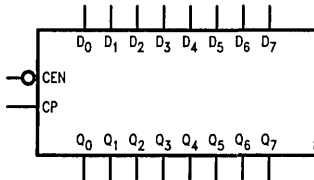
The F100353 output drivers are designed to drive 50 Ω termination to -2.0V. All inputs have 50 k Ω pull-down resistors.

Features

- ▣ Low power operation
- ▣ 2000V ESD protection
- ▣ Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

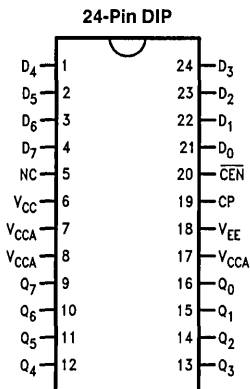
Logic Symbol



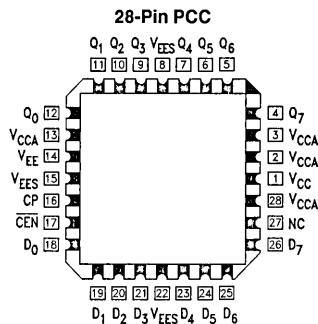
TL/F/9882-4

| Pin Names | Description |
|------------------|----------------------------------|
| D_0 - D_7 | Data Inputs |
| \overline{CEN} | Clock Enable Input |
| CP | Clock Input (Active Rising Edge) |
| Q_0 - Q_7 | Data Outputs |
| NC | No Connect |

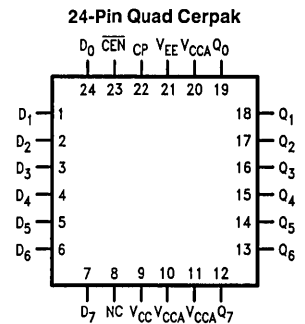
Connection Diagrams



TL/F/9882-1

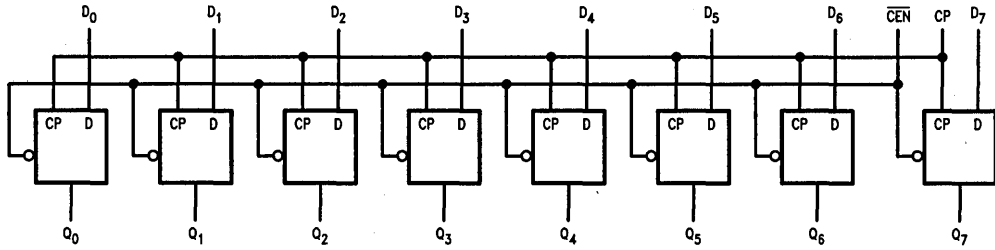


TL/F/9882-3



TL/F/9882-2

Logic Diagram



TL/F/9882-5

Truth Table

| Inputs | | | Outputs |
|----------------|-----|----|----------------|
| D _n | CEN | CP | Q _n |
| L | L | ↗ | L |
| H | L | ↗ | H |
| X | X | L | NC |
| X | X | H | NC |
| X | H | X | NC |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 NC = No Change
 ↗ = LOW to HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|------------------|----------------------|--------------|-------|------------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V _{OHC} | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for all Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for all Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |
| I _{IH} | Input HIGH Current | | | 240 | μA | V _{IN} = V _{IH} (Max) | |
| I _{EE} | Power Supply Current | -119 -122 | | -61 -61 | mA | Inputs Open V _{EE} = -4.2V to -4.8V V _{EE} = -4.2V to -5.7V | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND

| Symbol | Parameter | T _C = 0°C | | T _C = +25°C | | T _C = +85°C | | Units | Conditions |
|--------------------------------------|---|----------------------|------|------------------------|------|------------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f _{max} | Toggle Frequency | 425 | | 425 | | 425 | | MHz | Figures 2, 3 |
| t _{PLH} t _{PHL} | Propagation Delay CP to Output | 1.40 | 3.00 | 1.40 | 3.00 | 1.50 | 3.10 | ns | Figures 1, 3 (Note 1) |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 2.00 | 0.45 | 2.00 | ns | Figures 1, 3 |
| t _s | Setup Time | | | | | | | | |
| | D _n | 1.10 | | 1.10 | | 1.10 | | | |
| | CEN (Disable Time) | 0.40 | | 0.40 | | 0.40 | | ns | Figures 1, 4 |
| | CEN (Release Time) | 1.10 | | 1.10 | | 1.10 | | | |
| t _h | Hold Time | | | | | | | | |
| | D _n | 0.10 | | 0.10 | | 0.10 | | ns | Figures 1, 5 |
| t _{pw(H)} | Pulse Width HIGH CP | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1, 3 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Commercial Version (Continued)**PCC and Cerpac AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{max} | Toggle Frequency | 425 | | 425 | | 425 | | MHz | Figures 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 1.40 | 2.80 | 1.40 | 2.80 | 1.50 | 2.90 | ns | Figures 1, 3 (Note 2) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.90 | 0.45 | 1.90 | 0.45 | 1.90 | ns | Figures 1, 3 |
| t_s | Setup Time D_n \overline{CEN} (Disable Time) \overline{CEN} (Release Time) | 1.00 0.30 1.00 | | 1.00 0.30 1.00 | | 1.00 0.30 1.00 | | ns | Figures 1, 4 |
| t_h | Hold Time D_n | 0 | | 0 | | 0 | | ns | Figures 1, 5 |
| $t_{pw(H)}$ | Pulse Width HIGH CP | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1, 3 |
| $t_{s, G-G}$ | Skew, Gate to Gate | | TBD | | TBD | | TBD | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.**Note 2:** The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.**Military Version—Preliminary****DC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | | Notes |
|-----------|---------------------|-------|-------|---------|---------------------------------|--|---------------------------------------|------------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}$ (Max) or V_{IL} (Min) | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}$ (Min) or V_{IL} (Max) | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for all Inputs | | 1, 2, 3, 4 |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for all Inputs | | 1, 2, 3, 4 |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL}$ (Min) | | 1, 2, 3 |

Military Version—Preliminary (Continued)**DC Electrical Characteristics** (Continued)
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes |
|----------|----------------------|--------------|-----|---------|---------------------------------|---|---------|
| I_{IH} | Input HIGH Current | | 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | 1, 2, 3 |
| | | | 340 | μA | $-55^\circ C$ | | |
| I_{EE} | Power Supply Current | -125 -130 | -50 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open $V_{EE} = -4.2V$ to $-4.8V$ $V_{EE} = -4.2V$ to $-5.7V$ | 1, 2, 3 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|---------------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|--------------|--------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{max} | Toggle Frequency | 400 | | 400 | | 400 | | MHz | Figures 2, 3 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.70 | 3.30 | 0.80 | 3.10 | 0.80 | 3.80 | ns | Figures 1, 3 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | | 4 |
| t_s | Setup Time | | | | | | | | | |
| | D_n | 0.60 | | 0.60 | | 0.60 | | | ns | Figures 1, 4 |
| | \overline{CEN} (Disable Time) | 0.90 | | 0.70 | | 0.90 | | | | |
| \overline{CEN} (Release Time) | 1.40 | | 1.40 | | 2.10 | | | | | |
| t_h | Hold Time | D_n | 0.30 | 0.30 | | 0.30 | | ns | Figures 1, 5 | 4 |
| $t_{pw(H)}$ | Pulse Width HIGH | CP | 2.00 | 2.00 | | 2.00 | | ns | Figures 1, 3 | 4 |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|---------------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|--------------|--------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{max} | Toggle Frequency | 425 | | 425 | | 425 | | MHz | Figures 2, 3 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 1.30 | 3.20 | 1.30 | 3.20 | 1.40 | 3.30 | ns | Figures 1, 3 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 2.00 | 0.45 | 2.00 | ns | | 4 |
| t_s | Setup Time | | | | | | | | | |
| | D_n | 1.30 | | 1.30 | | 1.30 | | | ns | Figures 1, 4 |
| | \overline{CEN} (Disable Time) | 0.60 | | 0.60 | | 0.60 | | | | |
| \overline{CEN} (Release Time) | 1.30 | | 1.30 | | 1.30 | | | | | |
| t_h | Hold Time | D_n | 0.30 | 0.30 | | 0.30 | | ns | Figures 1, 5 | 4 |
| $t_{pw(H)}$ | Pulse Width HIGH | CP | 2.00 | 2.00 | | 2.00 | | ns | Figures 1, 3 | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$, temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

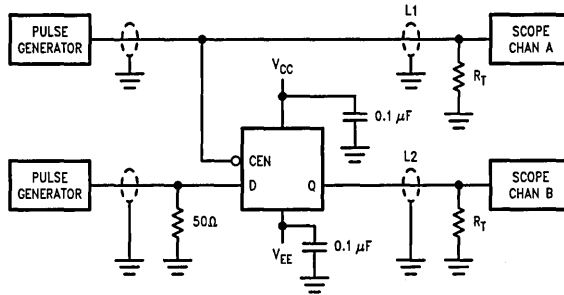


FIGURE 1. AC Test Circuit

TL/F/9882-6

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

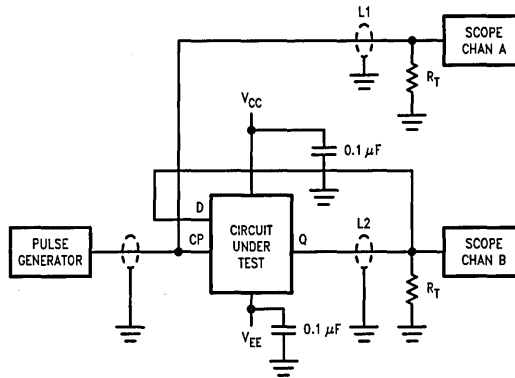


FIGURE 2. Toggle Frequency Test Circuit

TL/F/9882-7

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Jig and stray capacitance ≤ 3 pF

Switching Waveforms

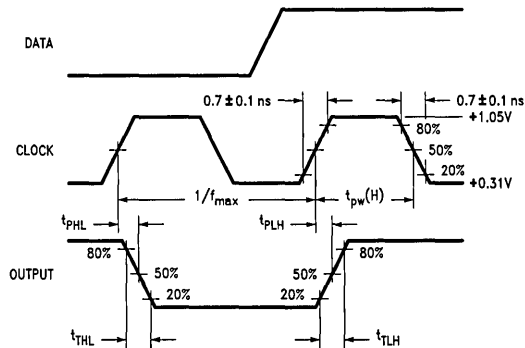


FIGURE 3. Propagation Delay (Clock) and Transition Times

TL/F/9882-8

Switching Waveforms (Continued)

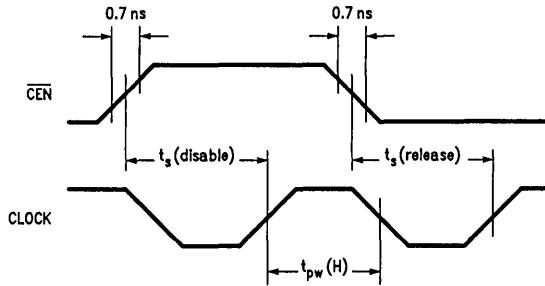


FIGURE 4. Setup and Pulse Width Times

TL/F/9882-9

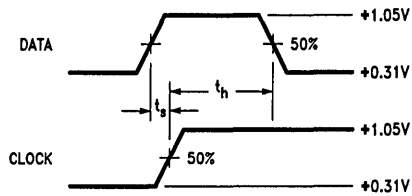


FIGURE 5. Data Setup and Hold Time

TL/F/9882-10

Note 1: t_s is the minimum time before the transition of the clock that information must be present at the data input.

Note 2: t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.



F100354

Low Power 8-Bit Register with Cut-Off Drivers

General Description

The F100354 contains eight D-Type edge triggered, master/slave flip-flops with individual inputs (D_n), true outputs (Q_n), a clock input (CP), an output enable pin (\overline{OEN}), and a common clock enable pin (\overline{CEN}). Data enters the master when CP is LOW and transfers to the slave when CP goes HIGH. When the \overline{CEN} input goes HIGH it overrides all other inputs, disables the clock, and the Q outputs maintain the last state.

A Q output follows its D input when the \overline{OEN} pin is LOW. A HIGH on \overline{OEN} holds the outputs in a cut-off state. The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is $-2.0V$, presenting a high

impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

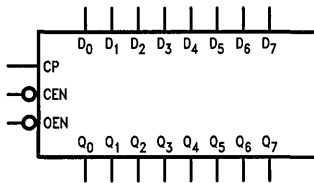
The F100354 outputs are designed to drive a doubly terminated 50Ω transmission line (25Ω load impedance). All inputs have $50\text{ k}\Omega$ pull-down resistors.

Features

- Cut-off drivers
- Drives 25Ω load
- Low power operation
- 2000V ESD protection
- Voltage compensated operating range = $-4.2V$ to $-5.7V$

Ordering Code: See Section 8

Logic Symbol

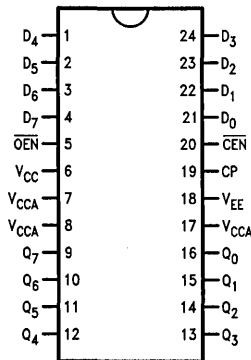


TL/F/10610-1

| Pin Names | Description |
|------------------|----------------------------------|
| D_0 - D_7 | Data Inputs |
| \overline{CEN} | Clock Enable Input |
| CP | Clock Input (Active Rising Edge) |
| \overline{OEN} | Output Enable Input |
| Q_0 - Q_7 | Data Outputs |

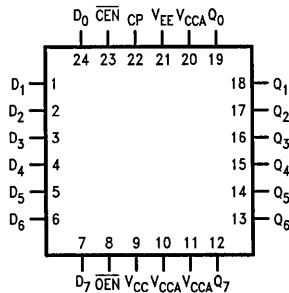
Connection Diagrams

24-Pin DIP



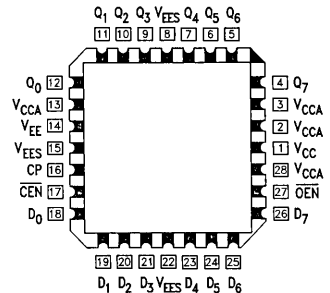
TL/F/10610-2

24-Pin Quad Cerpak



TL/F/10610-3

28-Pin PCC



TL/F/10610-4

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG}) -65°C to +150°C

Maximum Junction Temperature (T_J)

Ceramic +175°C

Plastic +150°C

V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V

Input Voltage (DC) V_{EE} to +0.5V

Output Current (DC Output HIGH) -100 mA

ESD (Note 2) ≥2000V

Commercial Version

DC Electrical Characteristics

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

Recommended Operating Conditions

Case Temperature (T_C)

Commercial 0°C to +85°C

Military -55°C to +125°C

Supply Voltage (V_{EE})

Commercial -5.7V to -4.2V

Military -5.7V to -4.2V

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-------------------|----------------------|--------------|-------|--------------|-------|---|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) Loading with 25Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) Loading with 25Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | |
| V _{OL} Z | Cutoff LOW Voltage | | | -1950 | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) OEN = HIGH |
| V _{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs |
| V _{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) |
| I _{IH} | Input HIGH Current | | | 240 | μA | V _{IN} = V _{IH} (Max) |
| I _{EE} | Power Supply Current | -202 -209 | | -105 -105 | mA | Inputs Open V _{EE} = -4.2V to -4.8V V _{EE} = -4.2V to -5.7V |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{Max} | Toggle Frequency | 250 | | 250 | | 250 | | MHz | Figures 1 and 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 1.40 | 3.00 | 1.40 | 3.00 | 1.50 | 3.10 | ns | Figures 1 and 4 (Note 1) |
| t_{PZH} t_{PHZ} | Propagation Delay OEN to Output | 1.60 | 4.20 | 1.60 | 4.20 | 1.60 | 4.20 | ns | Figures 3 and 7 (Note 1) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 2.00 | 0.45 | 2.00 | ns | Figures 1 and 4 |
| t_s | Setup Time D_n \overline{CEN} (Disable Time) \overline{CEN} (Release Time) | 1.10 0.40 1.10 | | 1.10 0.40 1.10 | | 1.10 0.40 1.10 | | ns | Figures 2 and 5 |
| t_h | Hold Time D_n | 0.10 | | 0.10 | | 0.10 | | ns | Figures 1 and 6 |
| $t_{pw(H)}$ | Pulse Width High CP | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1 and 4 |

Note 1: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

PCC and Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|-----------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{Max} | Toggle Frequency | 250 | | 250 | | 250 | | MHz | Figures 1 and 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 1.40 | 2.80 | 1.40 | 2.80 | 1.50 | 2.90 | ns | Figures 1 and 4 (Note 2) |
| t_{PZH} t_{PHZ} | Propagation Delay OEN to Output | 1.60 | 4.00 | 1.60 | 4.00 | 1.60 | 4.00 | ns | Figures 3 and 7 (Note 2) |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.90 | 0.45 | 1.90 | 0.45 | 1.90 | ns | Figures 1 and 4 |
| t_s | Setup Time D_n \overline{CEN} (Disable Time) \overline{CEN} (Release Time) | 1.00 0.30 1.00 | | 1.00 0.30 1.00 | | 1.00 0.30 1.00 | | ns | Figures 2 and 5 |
| t_h | Hold Time D_n | 0.00 | | 0.00 | | 0.00 | | ns | Figures 1 and 6 |
| $t_{pw(H)}$ | Pulse Width High CP | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1 and 4 |
| $t_{s, G-G}$ | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Note 2: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Military Version—Preliminary

DC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ C \text{ to } +125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|----------------------|-------|-------|---------|--|---|--|------------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with $25\Omega \text{ to } -2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with $25\Omega \text{ to } -2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with $25\Omega \text{ to } -2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with $25\Omega \text{ to } -2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{OLZ} | Cutoff LOW Voltage | | -1950 | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | $\overline{OEN} = \text{HIGH}$ | 1, 2, 3 |
| | | | -1850 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C \text{ to } +125^\circ C$ | Guaranteed HIGH Signal for All Inputs | | 1, 2, 3, 4 |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C \text{ to } +125^\circ C$ | Guaranteed LOW Signal for All Inputs | | 1, 2, 3, 4 |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C \text{ to } +125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL}(\text{Min})$ | | 1, 2, 3 |
| I_{IH} | Input HIGH Current | | 240 | μA | $0^\circ C \text{ to } +125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH}(\text{Max})$ | | 1, 2, 3 |
| | | | 340 | μA | $-55^\circ C$ | | | |
| I_{EE} | Power Supply Current | -215 | -85 | mA | $-55^\circ C \text{ to } +125^\circ C$ | Inputs Open $V_{EE} = -4.2V \text{ to } -4.8V$ $V_{EE} = -4.2V \text{ to } -5.7V$ | | 1, 2, 3 |
| | | -225 | -85 | | | | | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{Max} | Toggle Frequency | 200 | | 250 | | 200 | | MHz | Figures 1 and 4 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.9 | 3.70 | 1.0 | 3.20 | 1.20 | 3.90 | ns | Figures 1 and 4 | 1, 2, 3, 5 |
| t_{PZH} t_{PHZ} | Propagation Delay OEN to Output | 1.20 | 5.0 | 1.60 | 4.20 | 1.40 | 4.30 | ns | Figures 3 and 7 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | Figures 1 and 4 | 4 |
| t_s | Setup Time D_n \overline{CEN} (Disable Time) \overline{CEN} (Release Time) | 1.30 0.60 1.30 | | 1.30 0.60 1.30 | | 1.30 0.60 1.30 | | ns | Figures 2 and 5 | 4 |
| t_h | Hold Time D_n | 0.30 | | 0.30 | | 0.30 | | ns | Figures 1 and 6 | 4 |
| $t_{pw(H)}$ | Pulse Width HIGH CP | 2.4 | | 2.4 | | 2.4 | | ns | Figures 1 and 4 | 4 |

Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|-----------------|------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{Max} | Toggle Frequency | 200 | | 250 | | 200 | | MHz | Figures 1 and 4 | 4 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.9 | 3.70 | 1.0 | 3.20 | 1.20 | 3.90 | ns | Figures 1 and 4 | 1, 2, 3, 5 |
| t_{PZH} t_{PHZ} | Propagation Delay OEN to Output | 1.20 | 5.0 | 1.60 | 4.20 | 1.40 | 4.30 | ns | Figures 3 and 7 | 1, 2, 3, 5 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 2.50 | 0.40 | 2.40 | 0.40 | 2.70 | ns | Figures 1 and 4 | 4 |
| t_s | Setup Time D_n \overline{CEN} (Disable Time) \overline{CEN} (Release Time) | 0.60 0.90 1.40 | | 0.60 0.70 1.40 | | 0.60 0.90 2.10 | | ns | Figures 2 and 5 | 4 |
| t_h | Hold Time D_n | 0.30 | | 0.30 | | 0.30 | | ns | Figures 1 and 6 | 4 |
| $t_{pw(H)}$ | Pulse Width HIGH CP | 2.00 | | 2.00 | | 2.00 | | ns | Figures 1 and 4 | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

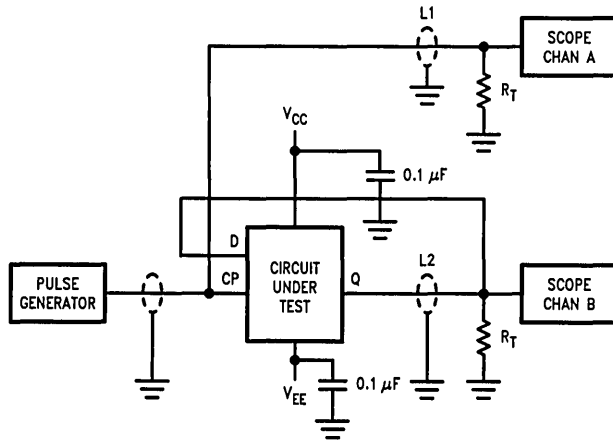
Note 2: Screen tested 100% on each device at $+25^\circ C$, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Note 5: The propagation delay specified is for single output switching. Delays may vary up to 300 ps with multiple outputs switching.

Test Circuitry

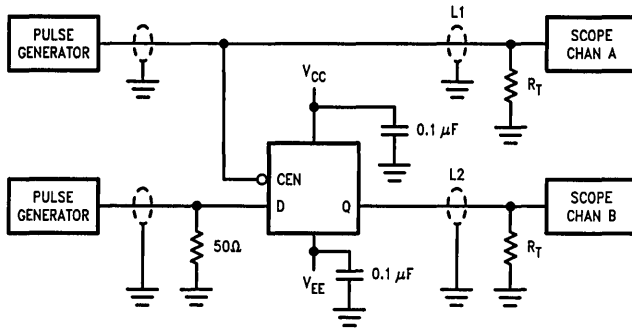


TL/F/10610-5

FIGURE 1. Toggle Frequency Test Circuit

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance ≤ 3 pF

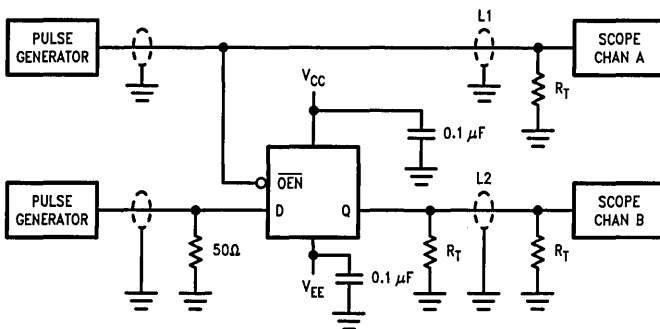


TL/F/10610-6

FIGURE 2. AC Test Circuit

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance ≤ 3 pF



TL/F/10610-7

FIGURE 3. AC Test Circuit

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance ≤ 3 pF

Switching Waveforms

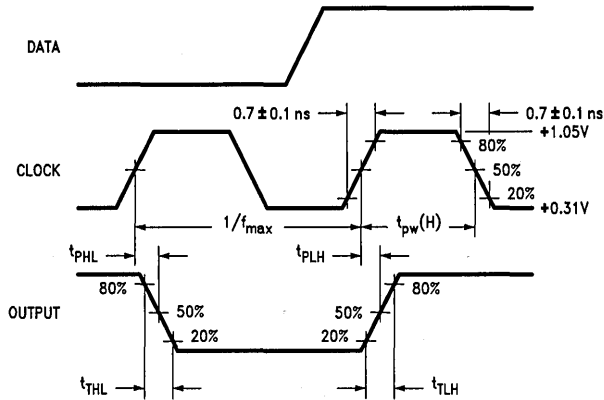


FIGURE 4. Propagation Delay (Clock) and Transition Times

TL/F/10610-8

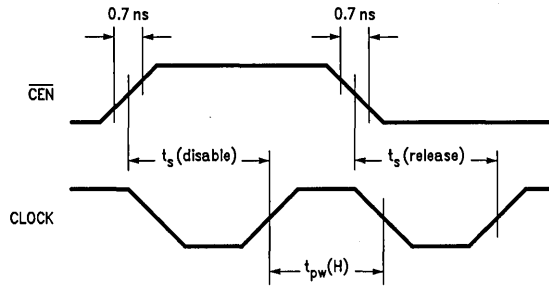


FIGURE 5. Setup and Pulse Width Times

TL/F/10610-9

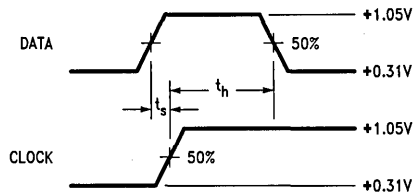


FIGURE 6. Data Setup and Hold Time

TL/F/10610-10

Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.
 t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

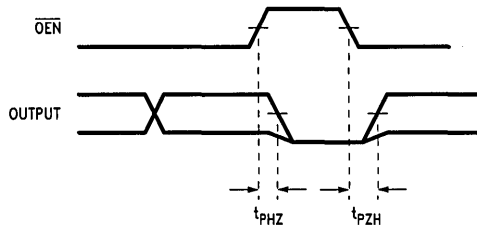


FIGURE 7. Cutoff Times

TL/F/10610-11

F100355

Low Power Quad Multiplexer/Latch

General Description

The F100355 contains four transparent latches, each of which can accept and store data from two sources. When both Enable (\bar{E}_n) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1 , the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1 . A positive-going signal on either Enable input

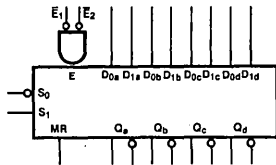
latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 k Ω pulldown resistors.

Features

- Greater than 40% power reduction of the F100155
- 2000V ESD protection
- Pin/function compatible with F100155
- Voltage compensated operating range = -4.2V to -5.7V

Ordering Code: See Section 8

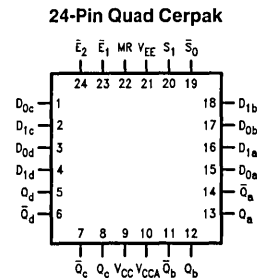
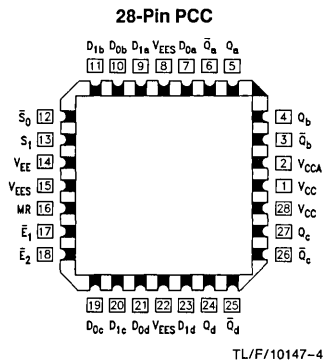
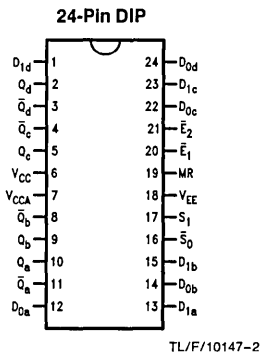
Logic Symbol



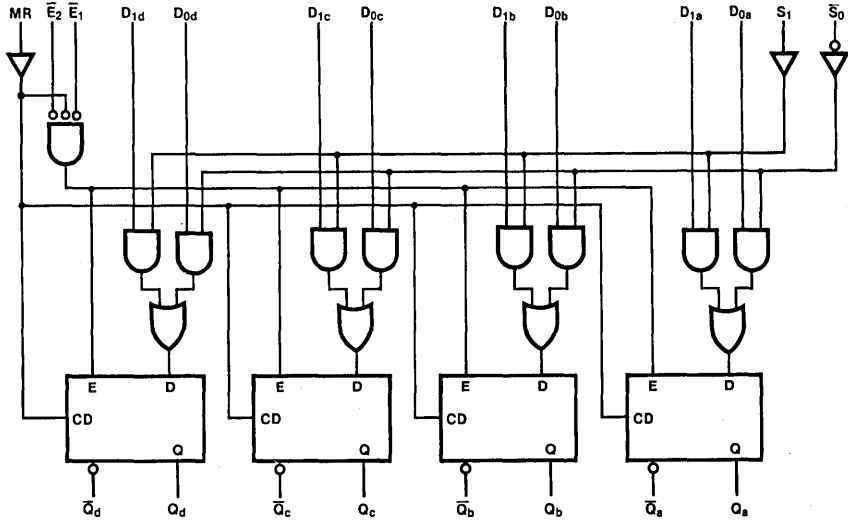
TL/F/10147-1

| Pin Names | Description |
|------------------------|----------------------------|
| \bar{E}_1, \bar{E}_2 | Enable Inputs (Active LOW) |
| \bar{S}_0, S_1 | Select Inputs |
| MR | Master Reset |
| $D_{na}-D_{nd}$ | Data Inputs |
| Q_a-Q_d | Data Outputs |
| $\bar{Q}_a-\bar{Q}_d$ | Complementary Data Outputs |

Connection Diagrams



Logic Diagram



TL/F/10147-5

Operating Mode Table

| Controls | | | | Outputs |
|-------------|-------------|-------|-------------|-------------------|
| \bar{E}_1 | \bar{E}_2 | S_1 | \bar{S}_0 | Q_n |
| H | X | X | X | Latched* |
| X | H | X | X | Latched* |
| L | L | L | L | D_{0x} |
| L | L | H | L | $D_{0x} + D_{1x}$ |
| L | L | L | H | L |
| L | L | H | H | D_{1x} |

*Stores data present before \bar{E} went HIGH

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Truth Table

| Inputs | | | | | | | Outputs | |
|--------|-------------|-------------|-------|-------------|----------|----------|-------------|----------|
| MR | \bar{E}_1 | \bar{E}_2 | S_1 | \bar{S}_0 | D_{1x} | D_{0x} | \bar{Q}_x | Q_x |
| H | X | X | X | X | X | X | H | L |
| L | L | L | H | H | H | X | L | H |
| L | L | L | H | H | L | X | H | L |
| L | L | L | L | L | X | H | L | H |
| L | L | L | L | L | X | L | H | L |
| L | L | L | H | L | H | X | L | H |
| L | L | L | H | L | X | H | L | H |
| L | L | L | H | X | L | L | H | L |
| L | H | X | X | X | X | X | Latched* | Latched* |
| L | X | H | X | X | X | X | Latched* | Latched* |

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|---|-------|-------|--------------------------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for ALL Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for ALL Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |
| I_{IH} | Input HIGH Current \bar{S}_0, S_1 \bar{E}_1, \bar{E}_2 $D_{na}-D_{nd}$ MR | | | 220 350 340 430 | μA | $V_{IN} = V_{IH}(\text{Max})$ | |
| I_{EE} | Power Supply Current | -87 | | -40 | mA | Inputs Open | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode) | 0.60 | 1.90 | 0.60 | 1.90 | 0.70 | 2.00 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode) | 1.00 | 2.60 | 1.00 | 2.60 | 1.20 | 2.70 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_1, \bar{E}_2 to Output | 0.80 | 2.00 | 0.80 | 2.00 | 0.80 | 2.10 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 0.80 | 2.30 | 0.80 | 2.30 | 0.80 | 2.30 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.60 | 1.40 | 0.60 | 1.40 | 0.60 | 1.40 | ns | Figures 1 and 2 |
| t_S | Setup Time $D_{na}-D_{nd}$ | 0.90 | | 0.90 | | 0.90 | | ns | Figure 4 |
| | \bar{S}_0, S_1 | 1.70 | | 1.70 | | 1.70 | | | Figure 3 |
| | MR (Release Time) | 1.50 | | 1.50 | | 1.50 | | | |
| t_H | Hold Time $D_{na}-D_{nd}$ | 0.40 | | 0.40 | | 0.40 | | ns | Figure 4 |
| | \bar{S}_0, S_1 | 0.00 | | 0.00 | | 0.00 | | | |
| $t_{pw}(L)$ | Pulse Width LOW \bar{E}_1, \bar{E}_2 | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |
| $t_{pw}(H)$ | Pulse Width HIGH MR | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

Commercial Version (Continued)

PCC and Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|----------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode) | 0.60 | 1.70 | 0.60 | 1.70 | 0.70 | 1.80 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode) | 1.00 | 2.40 | 1.00 | 2.40 | 1.20 | 2.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_1, \bar{E}_2 to Output | 0.80 | 1.80 | 0.80 | 1.80 | 0.80 | 1.90 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 0.80 | 2.10 | 0.80 | 2.10 | 0.80 | 2.10 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.60 | 1.30 | 0.60 | 1.30 | 0.60 | 1.30 | ns | Figures 1 and 2 |
| t_S | Setup Time $D_{na}-D_{nd}$ | 0.80 | | 0.80 | | 0.80 | | ns | Figure 4 |
| | \bar{S}_0, S_1 | 1.60 | | 1.60 | | 1.60 | | | Figure 3 |
| | MR (Release Time) | 1.40 | | 1.40 | | 1.40 | | | |
| t_H | Hold Time $D_{na}-D_{nd}$ | 0.30 | | 0.30 | | 0.30 | | ns | Figure 4 |
| | \bar{S}_0, S_1 | -0.10 | | -0.10 | | -0.10 | | | |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E}_1, \bar{E}_2 | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |
| $t_{pw(H)}$ | Pulse Width HIGH MR | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |
| t_{S-G-G} | Skew Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in the propagation delays between each of the outputs.

Military Version — Preliminary

DC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ C \text{ to } +125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|---|-------|--------------------------|---------|--|--|---------------------------------------|---------------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to $-2.0V$ | 1,2,3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1,2,3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1,2,3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C \text{ to } +125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1,2,3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C \text{ to } +125^\circ C$ | Guaranteed HIGH Signal for ALL Inputs | 1,2,3,4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C \text{ to } +125^\circ C$ | Guaranteed LOW Signal for ALL Inputs | 1,2,3,4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C \text{ to } +125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL}(\text{Min})$ | 1,2,3 | |
| I_{IH} | Input HIGH Current \bar{S}_0, S_1 \bar{E}_1, \bar{E}_2 $D_{na}-D_{nd}$ MR | | 220 350 340 430 | μA | $0^\circ C \text{ to } +125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH}(\text{Max})$ | 1,2,3 | |
| | | | 320 500 490 630 | | μA | | | $-55^\circ C$ |
| I_{EE} | Power Supply Current | -95 | -32 | mA | $-55^\circ C \text{ to } +125^\circ C$ | Inputs Open | 1,2,3 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$ Temp., Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table 1) on each Mfg. lot at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ Temp., Subgroups 1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version — Preliminary (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|-------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode) | 0.40 | 2.30 | 0.50 | 2.20 | 0.50 | 2.60 | ns | Figures 1 and 2 | 1,2,3 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode) | 0.60 | 3.00 | 0.80 | 2.70 | 0.80 | 3.20 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_1, \bar{E}_2 to Output | 0.50 | 2.60 | 0.60 | 2.30 | 0.70 | 2.70 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 0.60 | 2.80 | 0.70 | 2.60 | 0.70 | 2.90 | ns | Figures 1 and 3 | 1,2,3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.40 | 1.90 | 0.40 | 1.90 | 0.40 | 1.90 | ns | Figures 1 and 2 | 4 |
| t_S | Setup Time $D_{na}-D_{nd}$ | 0.90 | | 0.90 | | 0.90 | | ns | Figure 4 | 4 |
| | \bar{S}_0, S_1 | 2.40 | | 2.40 | | 2.40 | | | | |
| | MR (Release Time) | 1.50 | | 1.50 | | 1.50 | | | Figure 3 | |
| t_H | Hold Time $D_{na}-D_{nd}$ | 0.40 | | 0.40 | | 0.40 | | ns | Figure 4 | 4 |
| | \bar{S}_0, S_1 | 0.00 | | 0.00 | | 0.00 | | | | |
| $t_{pw}(L)$ | Pulse Width LOW \bar{E}_1, \bar{E}_2 | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 | 4 |
| $t_{pw}(H)$ | Pulse Width HIGH MR | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 | 4 |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|-------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode) | 0.40 | 2.30 | 0.50 | 2.20 | 0.50 | 2.60 | ns | Figures 1 and 2 | 1,2,3 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode) | 0.60 | 3.00 | 0.80 | 2.70 | 0.80 | 3.20 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_1, \bar{E}_2 to Output | 0.50 | 2.60 | 0.60 | 2.30 | 0.70 | 2.70 | ns | | |

Switching Waveforms

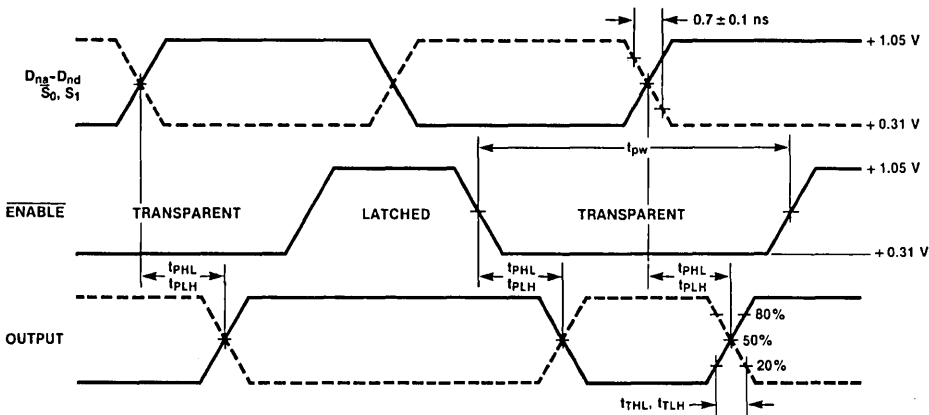


FIGURE 2. Enable Timing

TL/F/10147-7

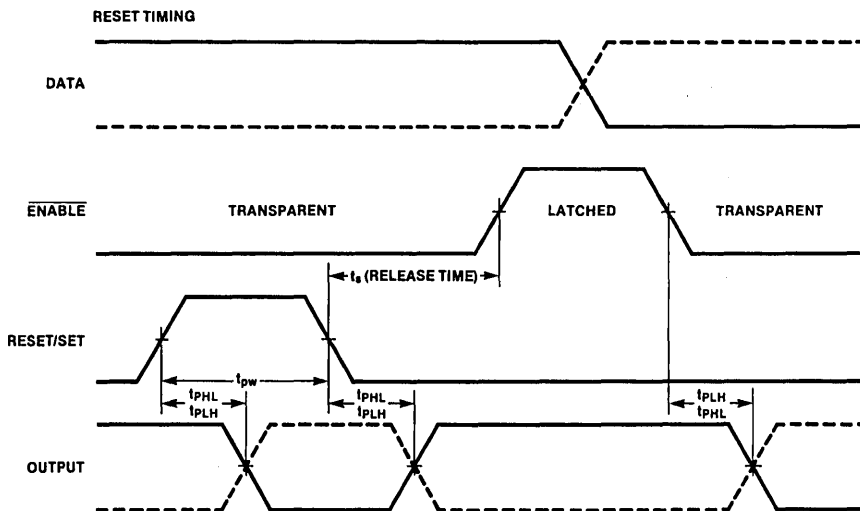
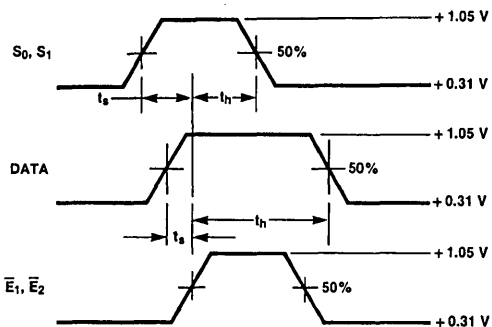


FIGURE 3. Reset Timing

TL/F/10147-8



TL/F/10147-9

FIGURE 4. Data Setup and Hold Times

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.



F100360 Low Power Dual Parity Checker/Generator

General Description

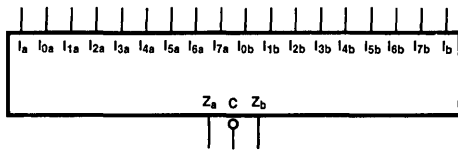
The F100360 is a dual parity checker/generator. Each half has nine inputs; the output is HIGH when an even number of inputs are HIGH. One of the nine inputs (I_a or I_b) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits. The F100360 also has a Compare (\bar{C}) output which allows the circuit to compare two 8-bit words. The \bar{C} output is LOW when the two words match, bit for bit. All inputs have 50 k Ω pulldown resistors.

Features

- Lower power than F100160
- 2000V ESD protection
- Pin/function compatible with F100160
- Voltage compensated operating range = $-4.2V$ to $-5.7V$
- Min to Max propagation delay 35% tighter than F100160

Ordering Code: See Section 8

Logic Symbol

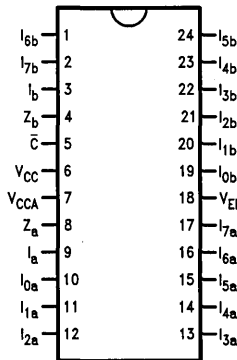


| Pin Names | Description |
|----------------------------|--------------------|
| I_a, I_b, I_{na}, I_{nb} | Data Inputs |
| Z_a, Z_b | Parity Odd Outputs |
| \bar{C} | Compare Output |

TL/F/10611-1

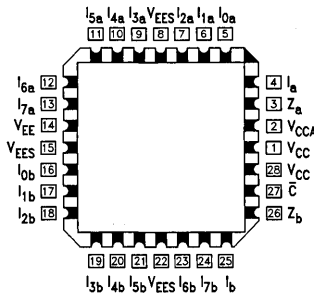
Connection Diagrams

24-Pin DIP



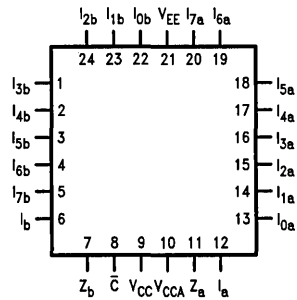
TL/F/10611-2

28-Pin PCC



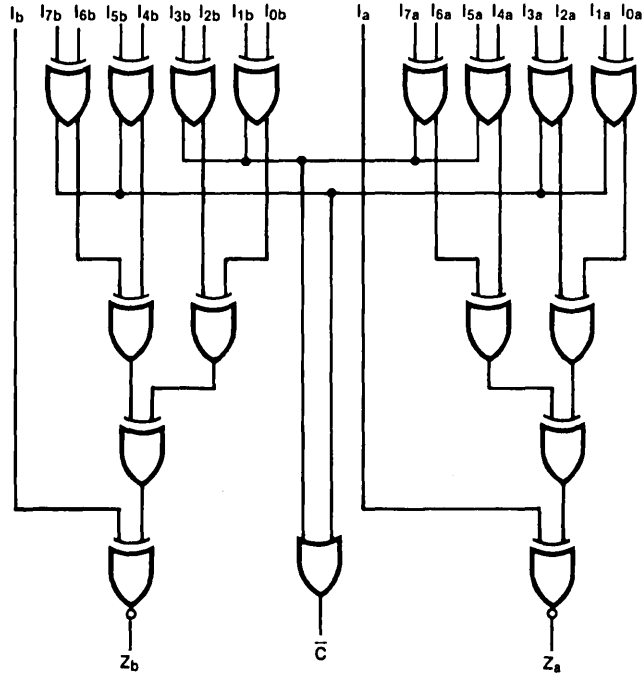
TL/F/10611-4

24-Pin Quad Cerpak



TL/F/10611-3

Logic Diagram



TL/F/10611-5

Truth Table (Each Half)

| Sum of HIGH Inputs | Output Z |
|--------------------|----------|
| Even | HIGH |
| Odd | LOW |

Comparator Function

$$\bar{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$$

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|-----------------------------|-----------------|
| Case Temperature (T_C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V_{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0°C$ to $+85°C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|----------------------|-------|-------|------------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH}$ (Max) or V_{IL} (Min) | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}$ (Min) or V_{IL} (Max) | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}$ (Min) | |
| I_{IH} | Input HIGH Current | | | 340 240 | μA | $V_{IN} = V_{IH}$ (Max) | |
| I_{EE} | Power Supply Current | -100 | | -50 | mA | Inputs Open | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|--------------------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|---------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay I _{na} , I _{nb} to Z _a , Z _b | 1.10 | 2.75 | 1.10 | 2.75 | 1.10 | 2.75 | ns | Figures 1 & 2 |
| t _{PLH} t _{PHL} | Propagation Delay I _{na} , I _{nb} to \bar{C} | 1.10 | 2.80 | 1.10 | 2.80 | 1.10 | 2.80 | ns | |
| t _{PLH} t _{PHL} | Propagation Delay I _a , I _b to Z _a , Z _b | 0.50 | 1.20 | 0.60 | 1.30 | 0.60 | 1.30 | ns | |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | |

PCC and Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|--------------------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | Propagation Delay I _{na} , I _{nb} to Z _a , Z _b | 1.10 | 2.75 | 1.10 | 2.75 | 1.10 | 2.75 | ns | Figures 1 & 2 |
| t _{PLH} t _{PHL} | Propagation Delay I _{na} , I _{nb} to \bar{C} | 1.10 | 2.80 | 1.10 | 2.80 | 1.10 | 2.80 | ns | |
| t _{PLH} t _{PHL} | Propagation Delay I _a , I _b to Z _a , Z _b | 0.50 | 1.20 | 0.60 | 1.30 | 0.60 | 1.30 | ns | |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | |
| t _{s,G-G} | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC only Note 1 |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version — Preliminary

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Notes | |
|-----------|--|-------|------------|---------|---------------------------------|--|------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL} (Min)$ | 1, 2, 3 | |
| I_{IH} | Input HIGH Current I_a, I_b I_{na}, I_{nb} | | 340 240 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | 1, 2, 3 | |
| | | | 490 340 | μA | $-55^\circ C$ | | | |
| I_{EE} | Power Supply Current | -110 | -50 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version — Preliminary (Continued)**Ceramic Dual-In-Line Package AC Electrical Characteristics** $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|---------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay I_{na}, I_{nb} to Z_a, Z_b | 1.00 | 2.95 | 1.00 | 2.95 | 1.00 | 2.95 | ns | Figures 1 & 2 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay I_{na}, I_{nb} to \bar{C} | 1.00 | 3.00 | 1.00 | 3.00 | 1.00 | 3.00 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay I_a, I_b to Z_a, Z_b | 0.40 | 1.40 | 0.50 | 1.50 | 0.50 | 1.50 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | | 4 |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|---------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay I_{na}, I_{nb} to Z_a, Z_b | 1.00 | 2.95 | 1.00 | 2.95 | 1.00 | 2.95 | ns | Figures 1 & 2 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay I_{na}, I_{nb} to \bar{C} | 1.00 | 3.00 | 1.00 | 3.00 | 1.00 | 3.00 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay I_a, I_b to Z_a, Z_b | 0.40 | 1.40 | 0.50 | 1.50 | 0.50 | 1.50 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.10 | 0.35 | 1.10 | 0.35 | 1.10 | ns | | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$ temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Test Circuitry

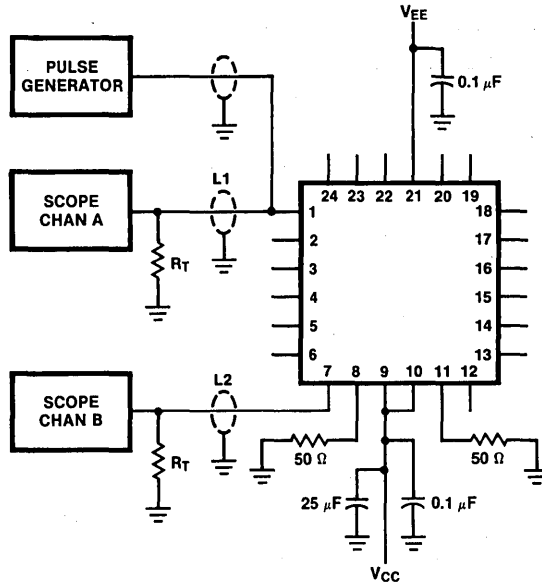


FIGURE 1. AC Test Circuit

TL/F/10611-6

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

Switching Waveforms

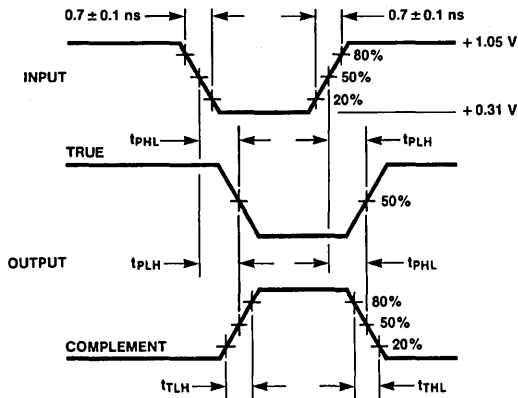


FIGURE 2. Propagation Delay and Transition Times

TL/F/10611-7

F100363

Low Power Dual 8-Input Multiplexer

General Description

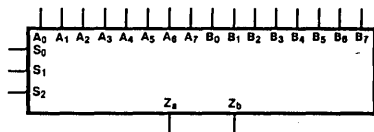
The F100163 is a dual 8-input multiplexer. The Data Select (S_n) inputs determine which bit (A_n and B_n) will be presented at the outputs (Z_a and Z_b respectively). The same bit (0-7) will be selected for both the Z_a and Z_b output. All inputs have 50 k Ω pulldown resistors.

Features

- 50% power reduction of the F100163
- 2000V ESD protection
- Pin/function compatible with F100163
- Voltage compensated operating range = -4.2V to -5.7V
- Tighter min to max propagation delay than F100163

Ordering Code: See Section 8

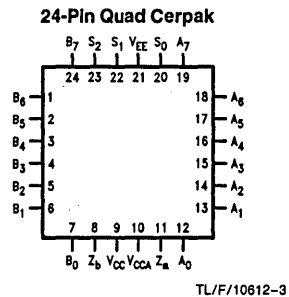
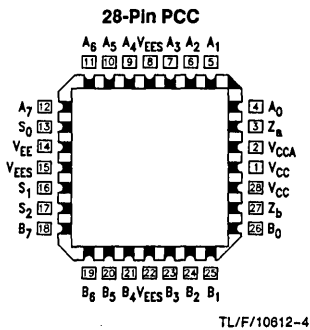
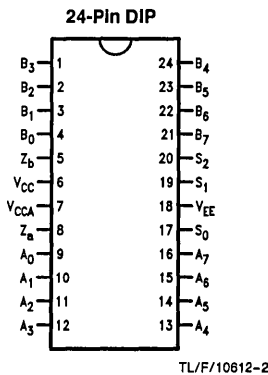
Logic Symbol



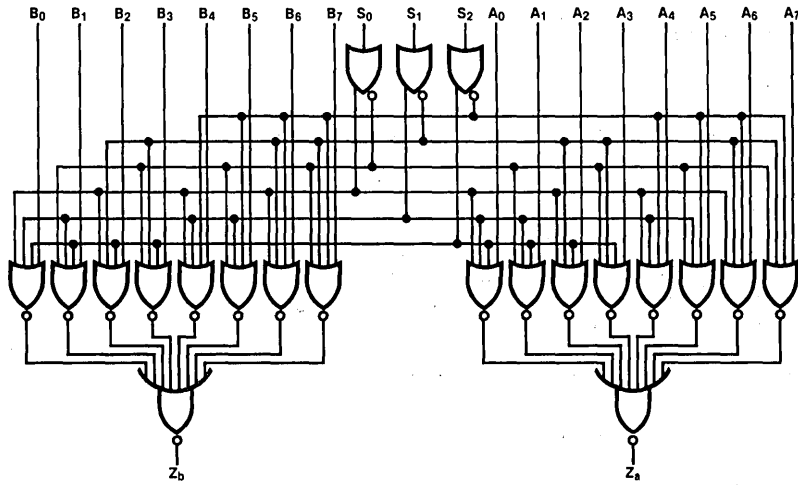
TL/F/10612-1

| Pin Names | Description |
|------------|--------------------|
| S_0-S_2 | Data Select Inputs |
| A_0-A_7 | A Data Inputs |
| B_0-B_7 | B Data Inputs |
| Z_a, Z_b | Data Outputs |

Connection Diagrams



Logic Diagram



TL/F/10612-5

Truth Table

| Inputs | | | | | | | | | | Outputs | | |
|----------------|----------------|----------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------|----------------|
| Select | | | Data | | | | | | | | | |
| S ₂ | S ₁ | S ₀ | A ₇ B ₇ | A ₆ B ₆ | A ₅ B ₅ | A ₄ B ₄ | A ₃ B ₃ | A ₂ B ₂ | A ₁ B ₁ | A ₀ B ₀ | Z _a | Z _b |
| L | L | L | | | | | | | | L | L | L |
| L | L | L | | | | | | | | H | L | H |
| L | L | H | | | | | | | L | | L | L |
| L | L | H | | | | | | L | H | | L | H |
| L | H | L | | | | | | | | | L | L |
| L | H | L | | | | | | | | | L | H |
| L | H | H | | | | | | L | H | | L | L |
| L | H | H | | | | | | | | | L | H |
| H | L | L | | | | L | H | | | | L | L |
| H | L | L | | | | | | | | | L | H |
| H | L | H | | | L | H | | | | | L | L |
| H | L | H | | | | | | | | | L | H |
| H | H | L | | L | | | | | | | L | L |
| H | H | L | | H | | | | | | | L | H |
| H | H | H | L | | | | | | | | L | L |
| H | H | H | H | | | | | | | | L | H |

H = HIGH Voltage Level
 L = LOW Voltage Level
 Blank = X = Don't Care

Recommended Operating Conditions

Case Temperature (T_c)
 Commercial
 Military
 Supply Voltage (V_{EE})
 Commercial
 Military

0°C to +55°C
 -55°C to +0°C
 -5.7V to -4.2V
 -5.7V to -4.2V

(Note 1)
 Devices are required, unless otherwise specified, to meet the following operating conditions.
 -65°C to +150°C

+175°C
 +150°C
 -7.0V to +0.5V
 V_{EE} to +0.5V
 -50 mA
 ≥2000V

Temperature (T_j)

V_{EE} = -4.2V to -5.7V, V_{CC} = V_{CCA} = GND, T_c = 0°C to +85°C (Note 3)
 Input Current (DC)
 Output Current (DC Output HIGH)
 ESD (Note 2)

Commercial Version

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-------------------|----------------------|-------|-------|-------|-------|--|---------------------------------------|
| | | | | | | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OH} C | Output HIGH Voltage | -1035 | -1165 | -1610 | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Guaranteed HIGH Signal for All Inputs |
| V _{OL} C | Output LOW Voltage | -1830 | -870 | -1475 | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Guaranteed LOW Signal for All Inputs |
| V _{IH} | Input HIGH Voltage | 0.50 | 265 | 340 | μA | V _{IN} = V _{IL} (Min) | Inputs Open |
| V _{IL} | Input LOW Voltage | -80 | -40 | -40 | mA | V _{IN} = V _{IH} (Max) | Inputs Open |
| I _{IL} | Input LOW Current | | | | | | |
| I _{IH} | Input HIGH Current | | | | | | |
| I _{EE} | Power Supply Current | | | | | | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
 Note 2: ESD testing conforms to MIL-STD-883, Method 3015.
 Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

| Symbol | Parameter | T _c = 0°C | | T _c = +25°C | | T _c = +85°C | | Units | Conditions |
|---|-----------|--|------|------------------------|------|------------------------|------|-------|------------|
| | | Min | Max | Min | Max | Min | Max | | |
| | | Propagation Delay A ₀ -A ₇ , B ₀ -B ₇ to Output | 0.70 | 1.65 | 0.80 | 1.70 | 0.80 | | |
| Propagation Delay S ₀ -S ₂ to Output | 1.30 | 2.60 | 1.40 | 2.70 | 1.40 | 2.70 | | | |
| Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.30 | 0.45 | 1.30 | | | |

2

AC Electrical Characteristics

5.7V, $V_{CC} = V_{CCA} = GND$

| Parameter | $T_c = 0^\circ C$ | | $T_c = +25^\circ C$ | | $T_c = +85^\circ C$ | | Units | Conditions |
|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | Min | Max | Min | Max | Min | Max | | |
| Propagation Delay A_0-A_7, B_0-B_7 to Output | 0.70 | 1.65 | 0.80 | 1.70 | 0.80 | 1.80 | ns | Figures 1 and 2 |
| Propagation Delay S_0-S_2 to Output | 1.30 | 2.60 | 1.40 | 2.70 | 1.40 | 2.70 | ns | |
| Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |
| Skew, Gate to Gate | | | | | | | TBD | |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version—Preliminary

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_c = -55^\circ C$ to $+125^\circ C$

| Symbol | Parameter | Min | Max | Units | T_c | Conditions | Note |
|-----------|----------------------|-------|------------|---------|-------------------------------|---|------------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | 1, 2, 3 |
| V_{OL} | Output LOW Voltage | -1085 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | | 1, 2, 3 |
| V_{OHC} | Output HIGH Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | 1, 2, 3, 4 |
| V_{OLC} | Output LOW Voltage | -1830 | -1555 | mV | $0^\circ C$ to $+125^\circ C$ | | 1, 2, 3, 4 |
| V_{IH} | Input HIGH Voltage | -1035 | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | 1, 2, 3, 4 |
| V_{IL} | Input LOW Voltage | -1085 | -1555 | mV | $0^\circ C$ to $+125^\circ C$ | | 1, 2, 3, 4 |
| I_{IH} | Input HIGH Current | -1165 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | | 1, 2, 3, 4 |
| I_{IL} | Input LOW Current | -1830 | -1475 | mV | $0^\circ C$ to $+125^\circ C$ | | 1, 2, 3, 4 |
| I_{EE} | Power Supply Current | 0.50 | 265 340 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IH} (Max)$ | 1, 2, 3, 4 |
| | | | 385 490 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH} (Max)$ | 1, 2, 3, 4 |
| | | | -30 | mA | $0^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3, 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking to guarantee junction temperature equilibrium immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold" considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------------|
| Storage Temperature (T_{STG}) | -65°C to +150°C |
| Maximum Junction Temperature (T_J) | |
| Ceramic | +175°C |
| Plastic | +150°C |
| V_{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V_{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| ESD (Note 2) | ≥2000V |

Recommended Operating Conditions

| | |
|-----------------------------|-----------------|
| Case Temperature (T_C) | |
| Commercial | 0°C to +85°C |
| Military | -55°C to +125°C |
| Supply Voltage (V_{EE}) | |
| Commercial | -5.7V to -4.2V |
| Military | -5.7V to -4.2V |

Commercial Version

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions | |
|-----------|---|-------|-------|------------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -870 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | -1705 | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ | |
| I_{IH} | Input HIGH Current S_n A_n, B_n | | | 265 340 | μA | $V_{IN} = V_{IH} (Max)$ | |
| I_{EE} | Power Supply Current | -80 | | -40 | mA | Inputs Open | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|-----------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} | Propagation Delay A_0 - A_7 , B_0 - B_7 to Output | 0.70 | 1.65 | 0.80 | 1.70 | 0.80 | 1.80 | ns | Figures 1 and 2 |
| t_{PHL} | | | | | | | | | |
| t_{PLH} | Propagation Delay S_0 - S_2 to Output | 1.30 | 2.60 | 1.40 | 2.70 | 1.40 | 2.70 | | |
| t_{PHL} | | | | | | | | | |
| t_{TLH} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |
| t_{THL} | | | | | | | | | |

Commercial Version (Continued)**PCC and Cerpak AC Electrical Characteristics**

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND$$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|----------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_0-A_7, B_0-B_7 to Output | 0.70 | 1.65 | 0.80 | 1.70 | 0.80 | 1.80 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay S_0-S_2 to Output | 1.30 | 2.60 | 1.40 | 2.70 | 1.40 | 2.70 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |
| $t_{s, G-G}$ | Skew, Gate to Gate | TBD | | TBD | | TBD | | ps | PCC Only (Note 1) |

Note 1: Gate to gate skew is defined as the difference in propagation delays between each of the outputs.

Military Version—Preliminary**DC Electrical Characteristics**

$$V_{EE} = -4.2V \text{ to } -5.7V, V_{CC} = V_{CCA} = GND, T_C = -55^\circ C \text{ to } +125^\circ C$$

| Symbol | Parameter | Min | Max | Units | T_C | Conditions | Note | |
|-----------|----------------------|---------------------|------------|---------|------------------------------------|--|---------------------------------------|---------|
| V_{OH} | Output HIGH Voltage | -1025 | -870 | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | -870 | mV | $-55^\circ C$ | | | |
| V_{OL} | Output LOW Voltage | -1830 | -1620 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | -1830 | -1555 | mV | $-55^\circ C$ | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | mV | $0^\circ C$ to $+125^\circ C$ | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to $-2.0V$ | 1, 2, 3 |
| | | -1085 | | mV | $-55^\circ C$ | | | |
| V_{OLC} | Output LOW Voltage | | -1610 | mV | $0^\circ C$ to $+125^\circ C$ | | | |
| | | | -1555 | mV | $-55^\circ C$ | | | |
| V_{IH} | Input HIGH Voltage | -1165 | -870 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed HIGH Signal for All Inputs | 1, 2, 3, 4 | |
| V_{IL} | Input LOW Voltage | -1830 | -1475 | mV | $-55^\circ C$ to $+125^\circ C$ | Guaranteed LOW Signal for All Inputs | 1, 2, 3, 4 | |
| I_{IL} | Input LOW Current | 0.50 | | μA | $-55^\circ C$ to $+125^\circ C$ | $V_{EE} = -4.2V$ $V_{IN} = V_{IL}(\text{Min})$ | 1, 2, 3 | |
| I_{IH} | Input HIGH Current | S_n A_n, B_n | 265 | μA | $0^\circ C$ to $+125^\circ C$ | $V_{EE} = -5.7V$ $V_{IN} = V_{IH}(\text{Max})$ | 1, 2, 3 | |
| | | | 385 490 | μA | $-55^\circ C$ | | | |
| I_{EE} | Power Supply Current | -87 | -30 | mA | $-55^\circ C$ to $+125^\circ C$ | Inputs Open | 1, 2, 3 | |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups 1, 2, 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $-55^\circ C$, $+25^\circ C$, and $+125^\circ C$, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL} .

Military Version—Preliminary (Continued)

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay A_0-A_7, B_0-B_7 to Output | 0.50 | 2.40 | 0.60 | 2.30 | 0.70 | 3.00 | ns | Figures 1 and 2 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay S_0-S_2 to Output | 0.80 | 3.00 | 0.90 | 2.80 | 1.00 | 3.40 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.90 | 0.40 | 1.80 | 0.30 | 2.10 | ns | | 4 |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = -55^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +125^\circ C$ | | Units | Conditions | Notes |
|------------------------|---|---------------------|------|---------------------|------|----------------------|------|-------|-----------------|---------|
| | | Min | Max | Min | Max | Min | Max | | | |
| t_{PLH} t_{PHL} | Propagation Delay A_0-A_7, B_0-B_7 to Output | 0.50 | 2.40 | 0.60 | 2.30 | 0.70 | 3.00 | ns | Figures 1 and 2 | 1, 2, 3 |
| t_{PLH} t_{PHL} | Propagation Delay S_0-S_2 to Output | 0.80 | 3.00 | 0.90 | 2.80 | 1.00 | 3.40 | ns | | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.90 | 0.40 | 1.80 | 0.30 | 2.10 | ns | | 4 |

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals $-55^\circ C$), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at $+25^\circ C$ temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at $+25^\circ C$, Subgroup A9, and at $+125^\circ C$ and $-55^\circ C$, temperatures, Subgroups A10 and A11.

Note 4: Not tested at $+25^\circ C$, $+125^\circ C$, and $-55^\circ C$ temperature (design characterization data).

Test Circuitry

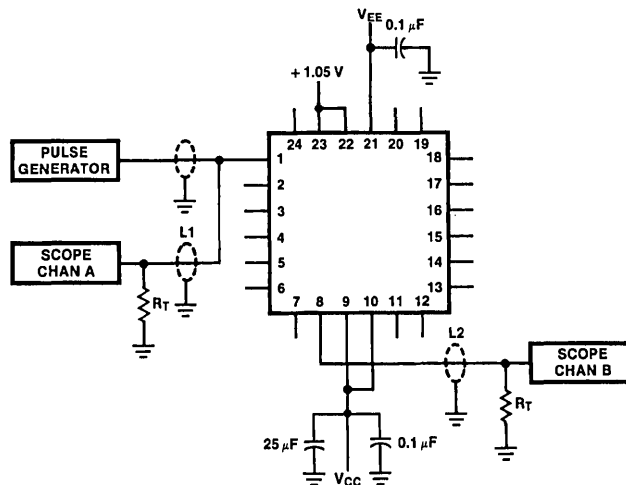


FIGURE 1. AC Test Circuit

TL/F/10612-6

Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

$L1$ and $L2 =$ equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling $0.1\mu F$ from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

$C_L =$ Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

Switching Waveforms

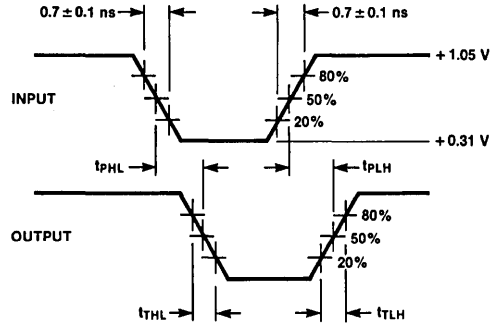


FIGURE 2. Propagation Delay and Transition Times

TL/F/10612-7

F100364

Low Power 16-Bit Multiplexer

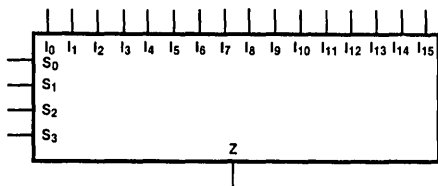
General Description

The F100364 is a 16-input multiplexer. Data paths are controlled by four Select lines (S_0 – S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data. All inputs have 50 k Ω pulldown resistors.

Features

- 35% power reduction of the F100164
- 2000V ESD protection
- Pin/function compatible with F100164
- Voltage compensated operating range = $-4.2V$ to $-5.7V$

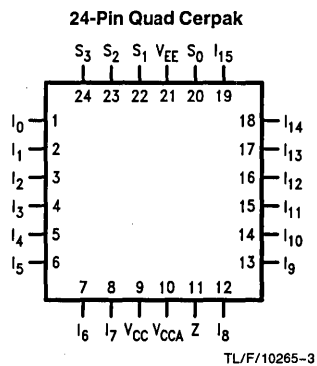
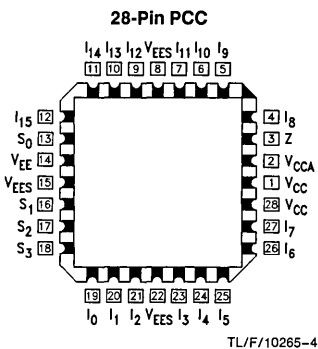
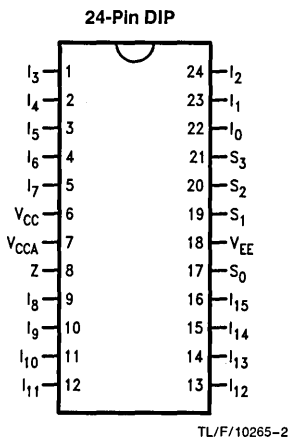
Logic Symbol



TL/F/10265-1

| Pin Names | Description |
|------------------|---------------|
| I_0 – I_{15} | Data Inputs |
| S_0 – S_3 | Select Inputs |
| Z | Data Output |

Connection Diagrams



F100370

Low Power Universal Demultiplexer/Decoder

General Description

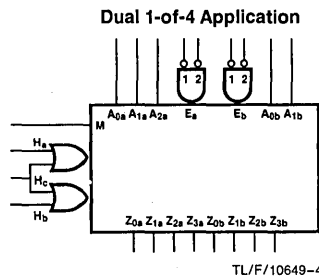
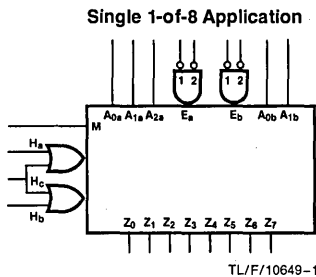
The F100370 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable (\bar{E}) inputs. Pin assignments for the \bar{E} inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables (\bar{E}_{1a} to \bar{E}_{1b} , \bar{E}_{2a} to \bar{E}_{2b}). Signals applied to auxiliary inputs H_a , H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are A_{0a} , A_{1a} and A_{0b} , A_{1b} with A_{2a} unused (i.e., left open, tied to V_{EE} or with

LOW signal applied). In the 1-of-8 mode, the Address inputs are A_{0a} , A_{1a} , A_{2a} with A_{0b} and A_{1b} LOW or open. All inputs have 50 k Ω pulldown resistors.

Features

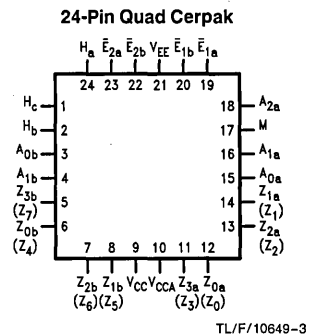
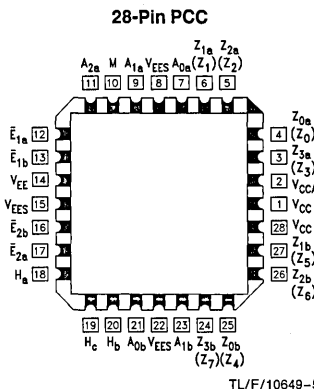
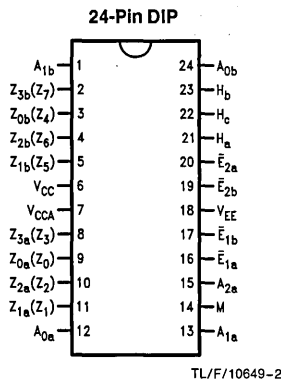
- 35% power reduction of the F100170
- 2000V ESD protection
- Pin/function compatible with F100170
- Voltage compensated operating range = -4.2V to -5.7V

Logic Symbols



| Pin Names | Description |
|---------------------------------|--|
| A_{na} , A_{nb} | Address Inputs |
| \bar{E}_{na} , \bar{E}_{nb} | Enable Inputs |
| M | Mode Control Input |
| H_a | Z_0 - Z_3 (Z_{0a} - Z_{3a}) Polarity Select Input |
| H_b | Z_4 - Z_7 (Z_{0b} - Z_{3b}) Polarity Select Input |
| H_c | Common Polarity Select Input |
| Z_0 - Z_7 | Single 1-of-8 Data Outputs |
| Z_{na} , Z_{nb} | Dual 1-of-4 Data Outputs |

Connection Diagrams



F100371

Low Power Triple 4-Input Multiplexer with Enable

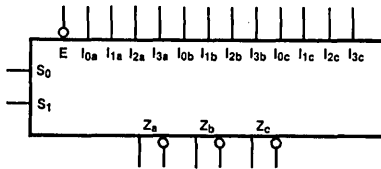
General Description

The F100371 contains three 4-input multiplexers which share a common decoder (inputs S_0 and S_1). Output buffer gates provide true and complement outputs. A HIGH on the Enable input (\bar{E}) forces all true outputs LOW (see Truth Table). All inputs have 50 k Ω pull-down resistors.

Features

- 35% power reduction of the F100171
- 2000V ESD protection
- Pin/function compatible with F100171
- Voltage compensated operating range = -4.2V to -5.7V

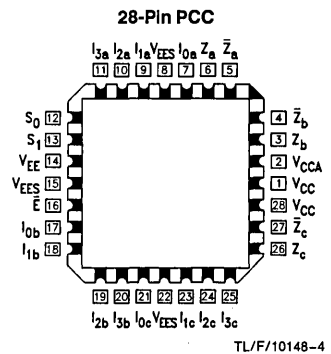
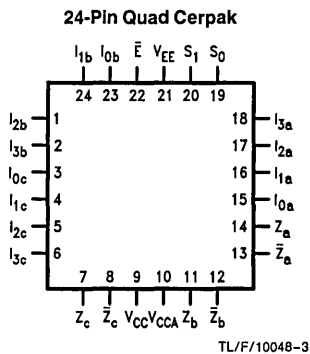
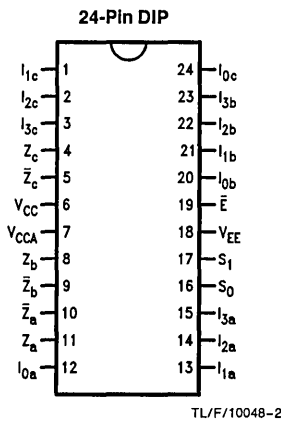
Logic Symbol



TL/F/10048-1

| Pin Names | Description |
|-----------------------|----------------------------|
| $I_{0x}-I_{3x}$ | Data Inputs |
| S_0, S_1 | Select Inputs |
| E | Enable Input (Active LOW) |
| Z_a-Z_c | Data Outputs |
| $\bar{Z}_a-\bar{Z}_c$ | Complementary Data Outputs |

Connection Diagrams



F100393

Low Power 9-Bit ECL-to-TTL Translator with Latches

General Description

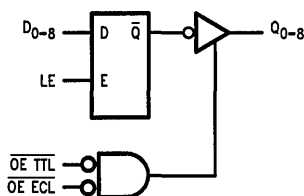
The F100393 is a 9-bit translator for converting F100K logic levels to FAST® TTL logic levels. A LOW on the latch enable (LE) latches the data at the input state. A HIGH on the LE makes the latches transparent. A HIGH on either the ECL or TTL output enable (\overline{OE} ECL or \overline{OE} TTL), holds the outputs in a high impedance state.

The F100393 is designed with FAST® TTL, 64 mA outputs for Bus Driving capability. All ECL inputs have 50 k Ω pull down resistors. When the inputs are either unconnected or at the same potential, the outputs will go LOW.

Features

- 64 mA I_{OL} drive capability
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Latched outputs
- FAST® TTL outputs

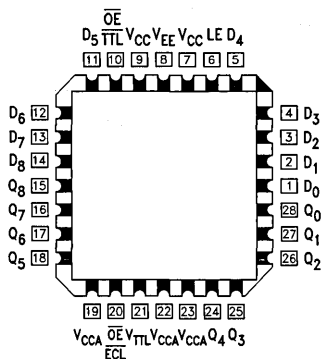
Logic Symbol



TL/F/10650-1

| Pin Names | Description |
|---------------------|---------------------|
| D_0 - D_8 | Data Inputs (ECL) |
| Q_0 - Q_8 | Data Outputs (TTL) |
| LE | Latch Enable Input |
| \overline{OE} TTL | Output Enable (TTL) |
| \overline{OE} ECL | Output Enable (ECL) |

Connection Diagram



TL/F/10650-2

F100395

Low Power 9-Bit ECL-to-TTL Translator with Registers

General Description

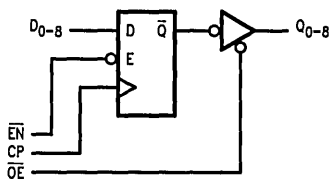
The F100395 is a 9-bit translator for converting F100K logic levels to FAST® TTL logic levels. A high on the output enable (\overline{OE}) holds the TTL outputs in a high impedance state. A low on the clock enable (\overline{EN}) transfers the data on the inputs to the outputs on a Low-to-High clock transition. A high on \overline{EN} will not change the state of the outputs.

The F100395 is designed with FAST® TTL, 64 mA outputs for Bus Driving capability. All inputs have 50 k Ω pull down resistors. When the inputs are either unconnected or at the same potential, the outputs will go LOW.

Features

- 64 mA I_{OL} drive capability
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Registered outputs
- FAST TTL outputs

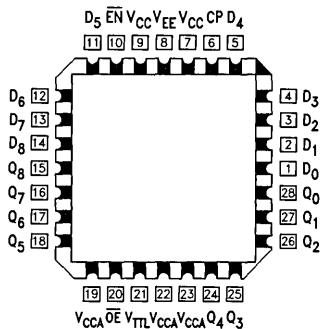
Logic Symbol



TL/F/10651-1

| Pin Names | Description |
|-----------------|--------------------|
| D_0-D_8 | Data Inputs (ECL) |
| Q_0-Q_8 | Data Outputs (TTL) |
| \overline{OE} | Output Enable |
| \overline{EN} | Clock Enable |
| CP | Clock Pulse |

Connection Diagram



TL/F/10651-2



Section 3
F100K 100 Series
Datasheets



Section 3 Contents

| | |
|--|-------|
| F100101 Triple 5-Input OR/NOR Gate | 3-3 |
| F100102 Quint 2-Input OR/NOR Gate | 3-6 |
| F100104 Quint 2-Input AND/NAND Gate | 3-9 |
| F100107 Quint Exclusive OR/NOR Gate | 3-13 |
| F100112 Quad Driver | 3-17 |
| F100113 Quad Driver | 3-21 |
| F100114 Quint Differential Line Receiver | 3-25 |
| F100115 Low Skew Quad Driver | 3-29 |
| F100117 Triple 2-Wide OA/OAI Gate | 3-33 |
| F100118 5-Wide 5-4-4-4-2 OA/OAI Gate | 3-36 |
| F100121 9-Bit Inverter | 3-40 |
| F100122 9-Bit Buffer | 3-43 |
| F100123 Hex Bus Driver | 3-46 |
| F100124 Hex TTL-to-100K ECL Translator | 3-50 |
| F100125 Hex 100K ECL-to-TTL Translator | 3-54 |
| F100126 9-Bit Backplane Driver | 3-58 |
| F100128 Octal Bidirectional ECL/TTL Translator | 3-61 |
| F100130 Triple D Latch | 3-70 |
| F100131 Triple D Flip-Flop | 3-76 |
| F100135 Triple JK Flip-Flop | 3-84 |
| F100136 4-Stage Counter/Shift Register | 3-90 |
| F100141 8-Bit Shift Register | 3-100 |
| F100142 4 x 4 Content Addressable Memory | 3-106 |
| F100150 Hex D Latch | 3-113 |
| F100151 Hex D Flip-Flop | 3-119 |
| F100155 Quad Multiplexer/Latch | 3-125 |
| F100156 Mask/Merge Latch | 3-131 |
| F100158 8-Bit Shift Matrix | 3-137 |
| F100160 Dual Parity Checker/Generator | 3-145 |
| F100163 Dual 8-Input Multiplexer | 3-150 |
| F100164 16-Input Multiplexer | 3-155 |
| F100165 Universal Priority Encoder | 3-160 |
| F100166 9-Bit Comparator | 3-166 |
| F100170 Universal Demultiplexer/Decoder | 3-171 |
| F100171 Triple 4-Input Multiplexer with Enable | 3-176 |
| F100175 Quint 100K-to-10K Latch | 3-181 |
| F100179 Carry Lookahead Generator | 3-187 |
| F100180 High-Speed 6-Bit Adder | 3-194 |
| F100181 4-Bit Binary/BCD ALU | 3-199 |
| F100182 9-Bit Wallace Tree Adder | 3-206 |
| F100183 2 x 8-Bit Recode Multiplier | 3-214 |
| F100250 Quint Full Duplex Line Transceiver | 3-226 |

F100101

Triple 5-Input OR/NOR Gate

General Description

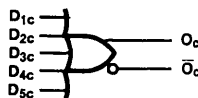
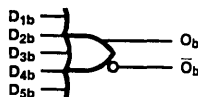
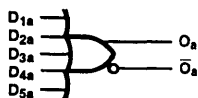
The F100101 is a monolithic triple 5-input OR/NOR gate. All inputs have 50 k Ω pull-down resistors and all outputs are buffered.

Refer to the F100301 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

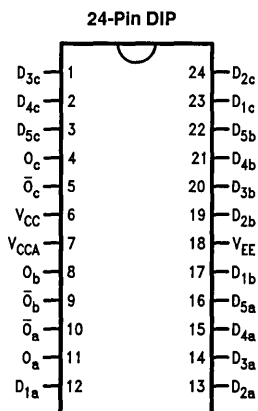
Logic Symbol



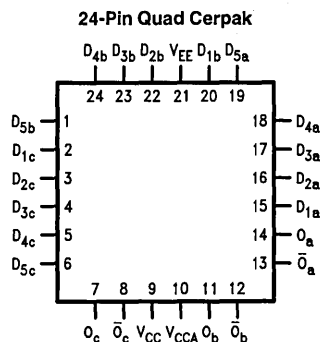
TL/F/9835-3

| Pin Names | Description |
|-----------------------------------|----------------------------|
| D_{na}, D_{nb}, D_{nc} | Data Inputs |
| O_a, O_b, O_c | Data Outputs |
| $\bar{O}_a, \bar{O}_b, \bar{O}_c$ | Complementary Data Outputs |

Connection Diagrams



TL/F/9835-1



TL/F/9835-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_j) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------|-----|-----|-----|---------|-------------------------|
| I_{IH} | Input HIGH Current | | | 350 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -38 | -26 | -18 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.50 | 1.15 | 0.50 | 1.15 | 0.55 | 1.30 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.20 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.50 | 0.95 | 0.50 | 0.95 | 0.55 | 1.10 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | ns | |

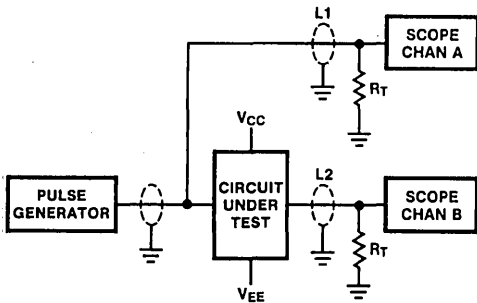


FIGURE 1. AC Test Circuit

TL/F/9835-5

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50 Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50 Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

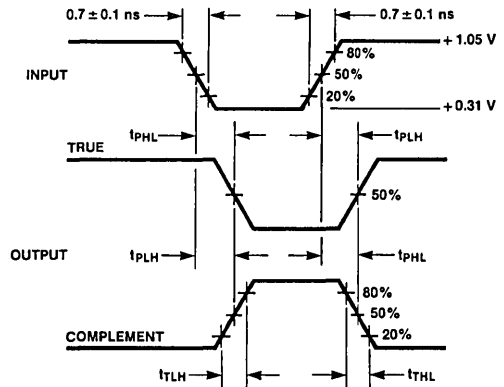


FIGURE 2. Propagation Delay and Transition Times

TL/F/9835-6



F100102 Quint 2-Input OR/NOR Gate

General Description

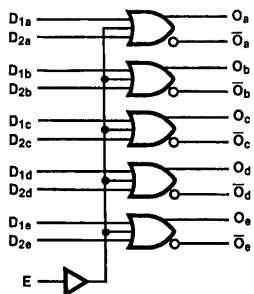
The F100102 is a monolithic quint 2-input OR/NOR gate with common enable. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Refer to the F100302 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

Logic Symbol



TL/F/9836-3

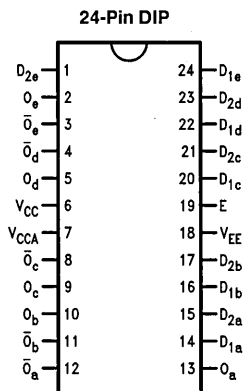
| Pin Names | Description |
|----------------------------------|----------------------------|
| D _{na} -D _{ne} | Data Inputs |
| E | Enable Input |
| O _a -O _e | Data Outputs |
| O _a -O _e | Complementary Data Outputs |

TABLE 1. F100102 Truth Table

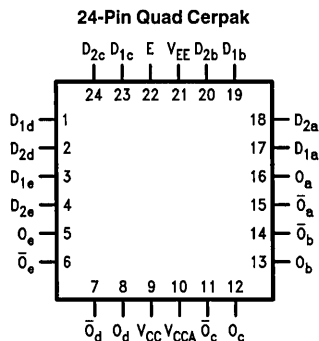
| D _{1X} | D _{2X} | E | O _X | O _X |
|-----------------|-----------------|---|----------------|----------------|
| L | L | L | L | H |
| L | L | H | H | L |
| L | H | L | H | L |
| L | H | H | H | L |
| H | L | L | H | L |
| H | L | H | H | L |
| H | H | L | H | L |
| H | H | H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level

Connection Diagrams



TL/F/9836-1



TL/F/9836-2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-----------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | +150°C |
| Case Temperature under Bias (T _C) | 0°C to +85°C |

| | |
|---|--------------------------|
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| Operating Range (Note 2) | -5.7V to -4.2V |

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-------|-------|-------|--|---------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | V _{IN} = V _{IH(Max)} or V _{IL(Min)} | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | mV | | |
| V _{OHC} | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH(Min)} or V _{IL(Max)} | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL(Min)} | |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-----|-------|-------|--|---------------------------|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | V _{IN} = V _{IH(Max)} or V _{IL(Min)} | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | mV | | |
| V _{OHC} | Output HIGH Voltage | -1030 | | | mV | V _{IN} = V _{IH(Min)} or V _{IL(Max)} | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1595 | mV | | |
| V _{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL(Min)} | |

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-----|-------|-------|--|---------------------------|
| V _{OH} | Output HIGH Voltage | -1035 | | -880 | mV | V _{IN} = V _{IH(Max)} or V _{IL(Min)} | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | | -1620 | mV | | |
| V _{OHC} | Output HIGH Voltage | -1045 | | | mV | V _{IN} = V _{IH(Min)} or V _{IL(Max)} | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL(Min)} | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--------------------------------------|-----|-----|------------|---------|------------------------|
| I_{IH} | Input HIGH Current Data Enable | | | 350 300 | μA | $V_{IN} = V_{IH(Max)}$ |
| I_{EE} | Power Supply Current | -80 | -55 | -38 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.35 | 0.45 | 1.15 | 0.45 | 1.40 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.95 | 2.15 | 0.95 | 2.15 | 0.95 | 2.20 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.20 | ns | |

Cerpak AC Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.15 | 0.45 | 0.95 | 0.45 | 1.20 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.95 | 1.95 | 0.95 | 1.95 | 0.95 | 2.00 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.10 | ns | |

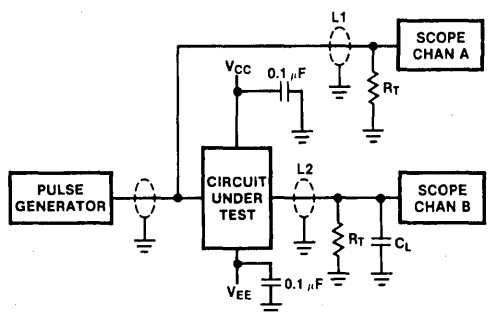


FIGURE 1. AC Test Circuit

TL/F/9836-5

Notes:

- $V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

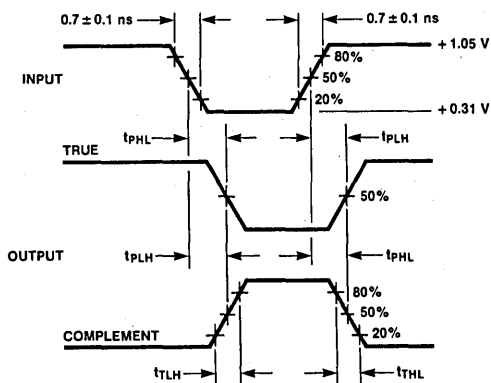


FIGURE 2. Propagation Delay and Transition Times

TL/F/9836-6



F100104 Quint AND/NAND Gate

General Description

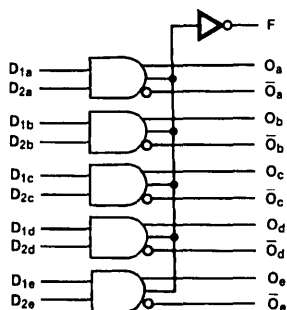
The F100104 is monolithic quint AND/NAND gate. The Function output is the wire-NOR of all five AND gate outputs. All inputs have 50 kΩ pull-down resistors.

Refer to the F100304 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

Logic Symbol



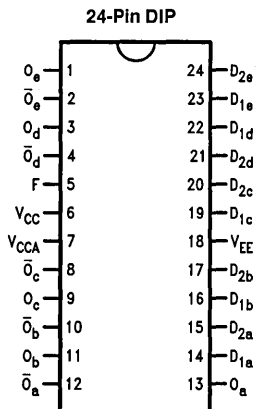
TL/F/9837-3

Logic Equation

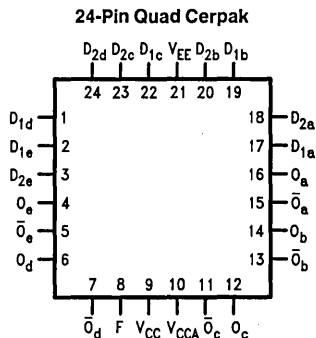
$$F = \overline{(D_{1a} \cdot D_{2a})} + (D_{1b} \cdot D_{2b}) + D_{1c} \cdot D_{2c} + (D_{1d} \cdot D_{2d}) + (D_{1e} \cdot D_{2e})$$

| Pin Names | Description |
|----------------------------------|----------------------------|
| D _{na} -D _{ne} | Data Inputs |
| F | Function Output |
| O _a -O _e | Data Outputs |
| \bar{O}_a - \bar{O}_e | Complementary Data Outputs |

Connection Diagrams



TL/F/9837-1



TL/F/9837-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|---------|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

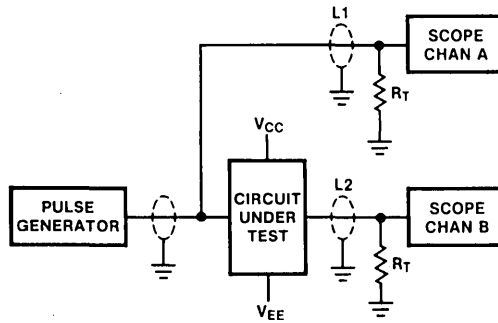
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--|-----|-----|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$ | | | 250 350 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -96 | -66 | -46 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{ne}$ to O, \bar{O} | 0.40 | 1.75 | 0.40 | 1.65 | 0.40 | 1.75 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.00 | 2.60 | 1.00 | 2.60 | 1.15 | 3.20 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.70 | 0.35 | 1.55 | 0.35 | 1.70 | ns | |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{ne}$ to O, \bar{O} | 0.40 | 1.55 | 0.40 | 1.45 | 0.40 | 1.55 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.00 | 2.40 | 1.00 | 2.40 | 1.15 | 3.00 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 1.60 | 0.35 | 1.45 | 0.35 | 1.60 | ns | |

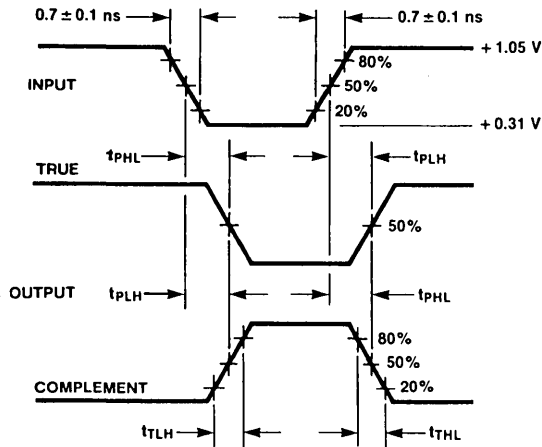


TL/F/9837-5

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- $C_L =$ Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit



TL/F/9837-6

FIGURE 2. Propagation Delay and Transition Times

F100107

Quint Exclusive OR/NOR Gate

General Description

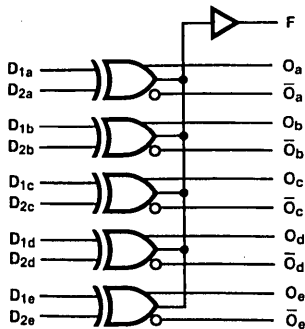
The F100107 is monolithic quint exclusive-OR/NOR gate. The Function output is the wire-OR of all five exclusive-OR outputs.

Refer to the F100307 datasheet for:

- PCC Packaging
- Lower Power
- Military Versions
- Extended Voltage Specs (-4.2V to -5.7V)

Ordering Code: See Section 8

Logic Symbol



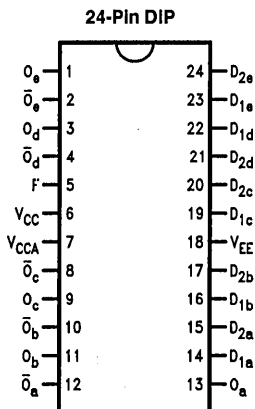
TL/F/9838-3

Logic Equation

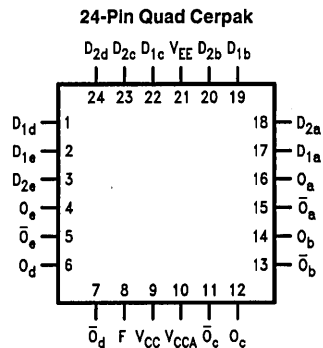
$$F = (D_{1a} \oplus D_{2a}) + (D_{1b} \oplus D_{2b}) + (D_{1c} \oplus D_{2c}) + (D_{1d} \oplus D_{2d}) + (D_{1e} \oplus D_{2e})$$

| Pin Names | Description |
|-----------------------|----------------------------|
| $D_{na}-D_{ne}$ | Data Inputs |
| F | Function Output |
| O_a-O_e | Data Outputs |
| $\bar{O}_a-\bar{O}_e$ | Complementary Data Outputs |

Connection Diagrams



TL/F/9838-1



TL/F/9838-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--|-----|-----|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current $D_{2a}-D_{2e}$ $D_{1a}-D_{1e}$ | | | 250 350 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -96 | -66 | -46 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics

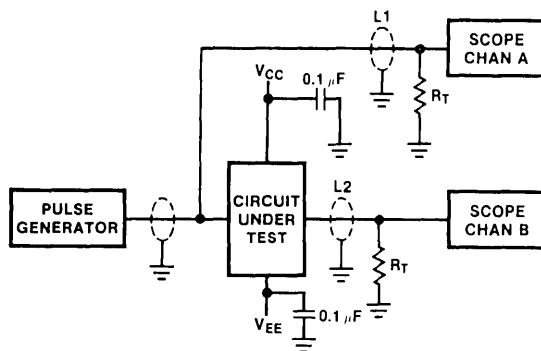
$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O} | 0.55 | 1.90 | 0.55 | 1.80 | 0.55 | 1.90 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O} | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.15 | 2.75 | 1.15 | 2.75 | 1.15 | 3.00 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.65 | 0.45 | 1.80 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{2a}-D_{2e}$ to O, \bar{O} | 0.55 | 1.70 | 0.55 | 1.60 | 0.55 | 1.70 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay $D_{1a}-D_{1e}$ to O, \bar{O} | 0.55 | 1.50 | 0.55 | 1.40 | 0.55 | 1.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay Data to F | 1.15 | 2.55 | 1.15 | 2.55 | 1.15 | 2.80 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.55 | 0.45 | 1.70 | ns | |

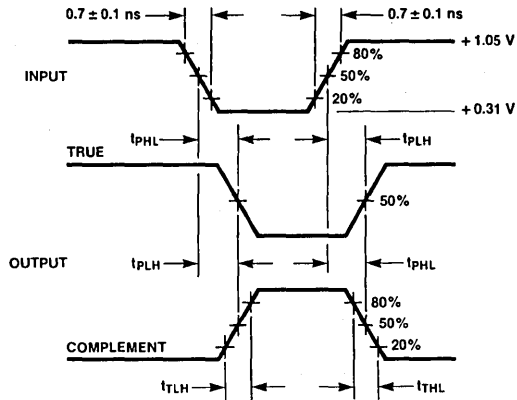


TL/F/9838-5

Notes:

- V_{CC} , $V_{CCA} = +2V$, $V_{EE} = -2.5V$
- $L1$ and $L2 =$ equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- $C_L =$ Fixture and stray capacitance $\leq 3 pF$

FIGURE 1. AC Test Circuit



TL/F/9838-6

FIGURE 2. Propagation Delay and Transition Times

F100112 Quad Driver

General Description

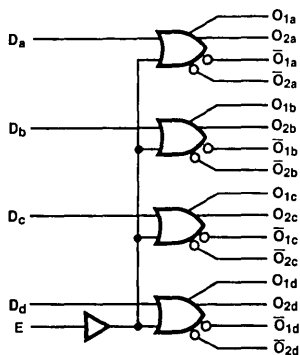
The F100112 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Refer to the F100313 Datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

Logic Symbol

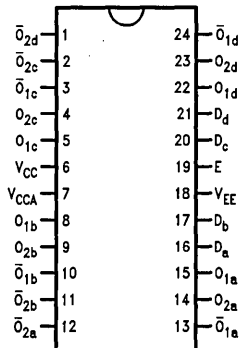


TL/F/9839-1

| Pin Names | Description |
|----------------------------------|----------------------------|
| D _a -D _d | Data Inputs |
| E | Enable Input |
| O _{na} -O _{nd} | Data Outputs |
| O _{na} -O _{nd} | Complementary Data Outputs |

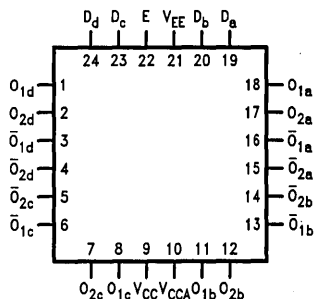
Connection Diagrams

24-Pin DIP



TL/F/9839-2

24-Pin Quad Cerpak



TL/F/9839-3



Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--------------------------------------|------|-----|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current Data Enable | | | 550 450 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -106 | -73 | -51 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.55 | 1.50 | 0.55 | 1.40 | 0.45 | 1.60 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.65 | 2.00 | 0.65 | 1.90 | 0.65 | 2.00 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.50 | 0.45 | 1.60 | ns | |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.55 | 1.30 | 0.55 | 1.20 | 0.45 | 1.40 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.65 | 1.80 | 0.65 | 1.70 | 0.65 | 1.80 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

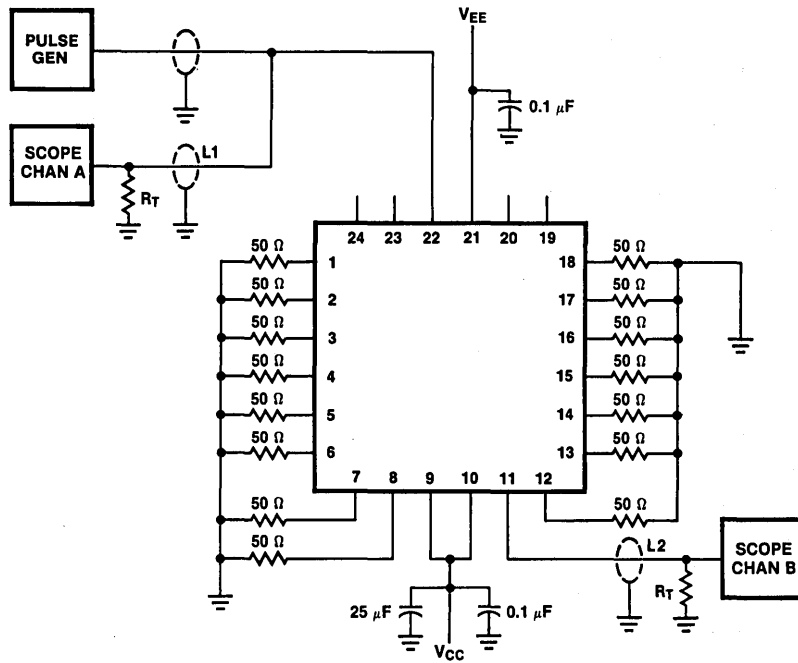


FIGURE 1. AC Test Circuit

TL/F/9839-5

Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

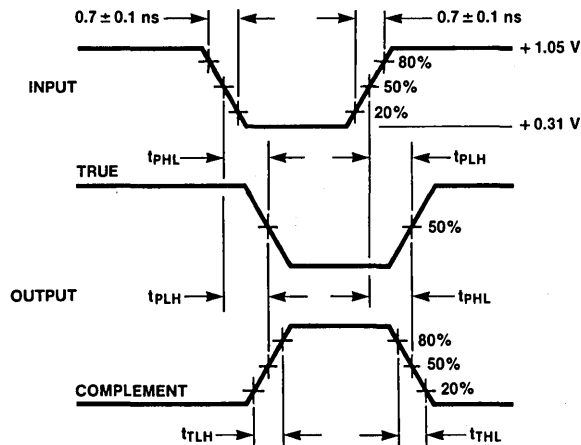


FIGURE 2. Propagation Delay and Transition Times

TL/F/9839-6

F100113 Quad Driver

General Description

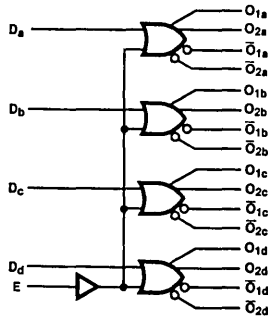
The F100113 is a monolithic quad driver with two OR and two NOR outputs and common enable. The common input is buffered to minimize input loading. If the D inputs are not used the Enable can be used to drive sixteen 50Ω lines. All inputs have 50 kΩ pull-down resistors and all outputs are buffered.

Refer to the F100313 Datasheet for:

PCG Packaging
Lower Power
Military Versions
Extended Voltage Specs (-4.2V to -5.7V)

Ordering Code: See Section 8

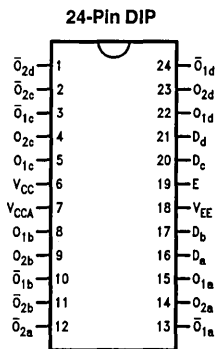
Logic Symbol



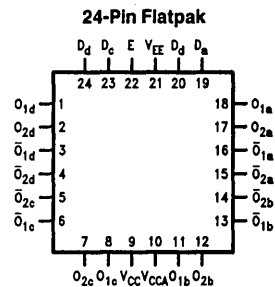
TL/F/9840-3

| Pin Names | Description |
|-----------------------------|----------------------------|
| D_a-D_d | Data Inputs |
| E | Enable Input |
| $O_{na}-O_{nd}$ | Data Outputs |
| $\bar{O}_{na}-\bar{O}_{nd}$ | Complementary Data Outputs |

Connection Diagrams



TL/F/9840-1



TL/F/9840-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|-----------------------------------|------|-----|------------|---------|------------------------|
| I_{IH} | Input HIGH Current Data Enable | | | 550 350 | μA | $V_{IN} = V_{IH(max)}$ |
| I_{EE} | Power Supply Current | -116 | -80 | -56 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.40 | 0.45 | 1.35 | 0.45 | 1.40 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.55 | 1.90 | 0.55 | 1.90 | 0.55 | 1.90 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.50 | 0.45 | 1.60 | ns | |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.20 | 0.45 | 1.15 | 0.45 | 1.20 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.55 | 1.70 | 0.55 | 1.70 | 0.55 | 1.70 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

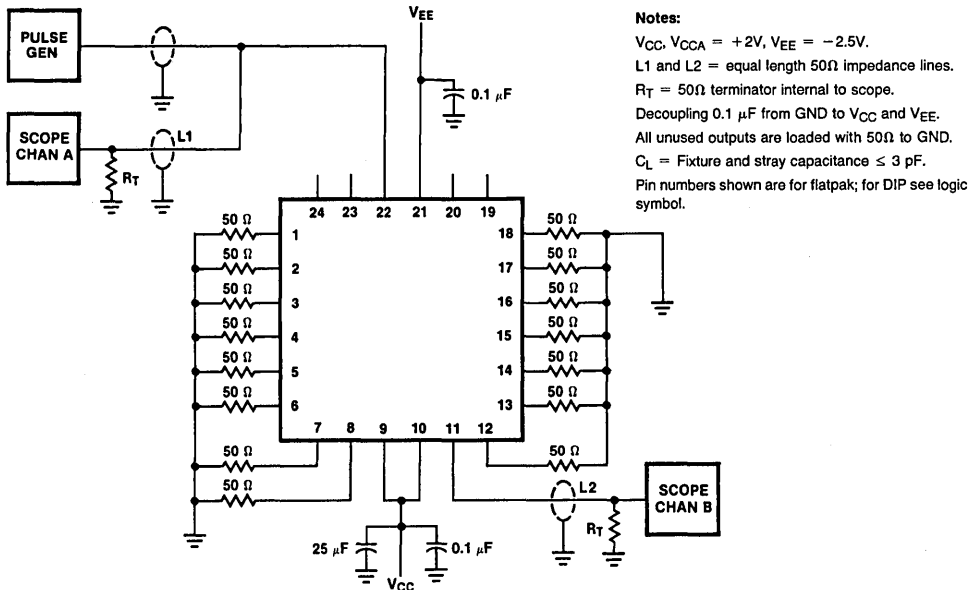


FIGURE 1. AC Test Circuit

TL/F/9840-5

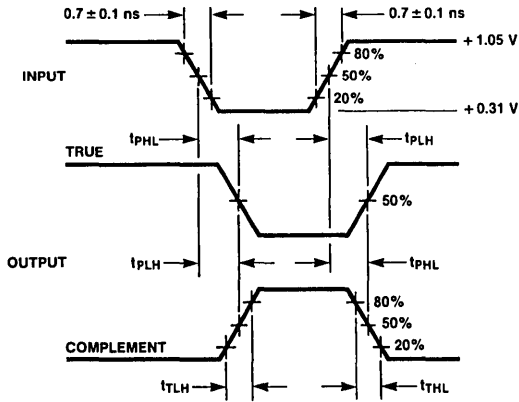


FIGURE 2. Propagation Delay and Transition Times

TL/F/9840-6

F100114

Quint Differential Line Receiver

General Description

The F100114 is a monolithic quint differential line receiver with emitter-follower outputs. An internal reference supply (V_{BB}) is available for single-ended reception. When used in single-ended operation the apparent input threshold of the true inputs is 25 mV to 30 mV higher (positive) than the threshold of the complementary inputs. Unlike other F100K ECL devices, the inputs do not have input pull-down resistors.

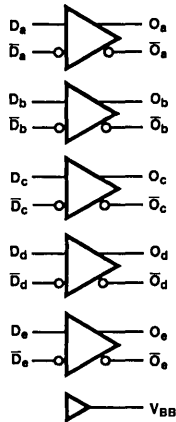
Active current sources provide common-mode rejection of 1.0V in either the positive or negative direction. A defined output state exists if both inverting and non-inverting inputs are at the same potential between V_{EE} and V_{CC} . The defined state is logic HIGH on the \bar{O}_a - \bar{O}_e outputs.

Refer to the F100314 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs ($-4.2V$ to $-5.7V$)

Ordering Code: See Section 8

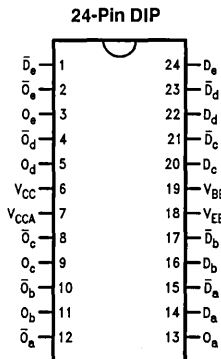
Logic Symbol



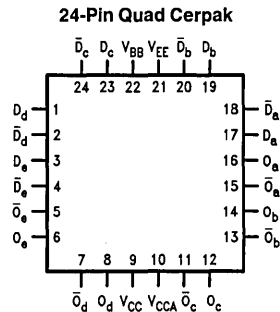
TL/F/9841-3

| Pin Names | Description |
|---------------------------|----------------------------|
| D_a - D_e | Data Inputs |
| \bar{D}_a - \bar{D}_e | Inverting Data Inputs |
| O_a - O_e | Data Outputs |
| \bar{O}_a - \bar{O}_e | Complementary Data Outputs |

Connection Diagrams



TL/F/9841-1



TL/F/9841-2

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C)

0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin

-7.0V to $+0.5\text{V}$

Input Voltage (DC)

V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH)

-50mA

Operating Range (Note 2)

-5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|------------------------------------|-------|-------|-------|-------|---|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{BB} | Output Reference Voltage | -1380 | -1320 | -1260 | mV | $I_{V_{BB}} = -250\mu\text{A}$ | |
| V_{IH} | Single-Ended Input HIGH Voltage | -1165 | | | mV | Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB}) | |
| V_{IL} | Single-Ended Input LOW Voltage | | | -1475 | mV | Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB}) | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|------------------------------------|-------|-------|-------|-------|---|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{BB} | Output Reference Voltage | -1396 | -1320 | -1244 | mV | $I_{V_{BB}} = -250\mu\text{A}$ | |
| V_{IH} | Single-Ended Input HIGH Voltage | -1150 | | | mV | Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB}) | |
| V_{IL} | Single-Ended Input LOW Voltage | | | -1475 | mV | Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB}) | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|------------------------------------|-------|-------|-------|-------|---|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{BB} | Output Reference Voltage | -1396 | -1320 | -1244 | mV | $I_{V_{BB}} = -250\mu\text{A}$ | |
| V_{IH} | Single-Ended Input HIGH Voltage | -1165 | | | mV | Guaranteed HIGH Signal for All Inputs (with one input tied to V_{BB}) | |
| V_{IL} | Single-Ended Input LOW Voltage | | | -1490 | mV | Guaranteed LOW Signal for All Inputs (with one input tied to V_{BB}) | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------|----------------------------|------|-----|-----|---------|--|
| V_{DIFF} | Input Voltage Differential | 150 | | | mV | Required for Full Output Swing |
| V_{CM} | Common Mode Voltage | | | 1.0 | V | Permissible $\pm V_{CM}$ with Respect to V_{BB} |
| I_{IH} | Input HIGH Current | | | 50 | μA | $V_{IN} = V_{IH} (Max)$, $D_a - D_e = V_{BB}$, $\bar{D}_a - \bar{D}_e = V_{IL} (Min)$ |
| I_{CBO} | Input Leakage Current | -10 | | | μA | $V_{IN} = V_{EE}$, $D_a - D_e = V_{BB}$, $\bar{D}_a - \bar{D}_e = V_{IL} (Min)$ |
| I_{EE} | Power Supply Current | -106 | -73 | -51 | mA | $D_a - D_e = V_{BB}$, $\bar{D}_a - \bar{D}_e = V_{IL} (Min)$ |

Ceramic Dual-In-Line Package AC Electrical Characteristics

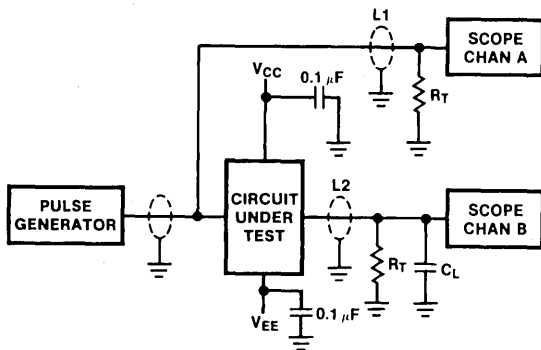
$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.55 | 1.90 | 0.60 | 2.00 | 0.70 | 2.40 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.55 | 1.30 | 0.45 | 1.20 | 0.45 | 1.40 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.55 | 1.70 | 0.60 | 1.80 | 0.70 | 2.20 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.55 | 1.20 | 0.45 | 1.10 | 0.45 | 1.30 | ns | |



TL/F/9841-5

Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

FIGURE 1. AC Test Circuit

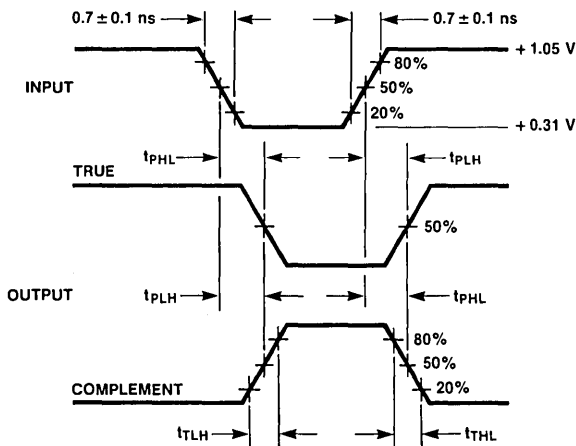


FIGURE 2. Propagation Delay and Transition Times

TL/F/9841-6

F100115

Low-Skew Quad Clock Driver

General Description

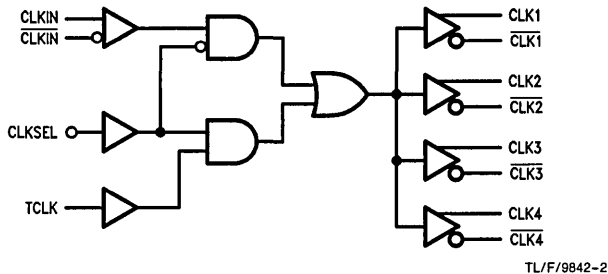
The F100115 contains four low skew differential drivers, designed for generation of multiple, minimum skew differential clocks from a single differential input. This device also has the capability to select a secondary single-ended clock source for use in lower frequency system level testing.

Features

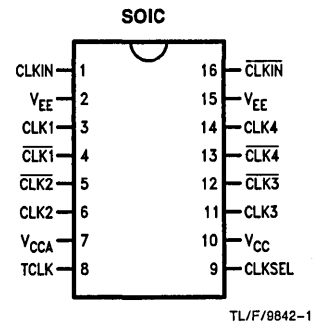
- Low output to output skew (≤ 75 ps)
- Differential inputs and outputs
- Small outline package
- Ideal for applications which require the low skew distribution of a clock signal to multiple outputs
- Secondary clock available for system level testing

Ordering Code: See Section 8

Logic Diagram



Connection Diagram



| Pin Names | Description |
|---|----------------------------|
| CLKIN, CLKIN | Differential Clock Inputs |
| CLK ₁₋₄ , CLK ₁₋₄ | Differential Clock Outputs |
| TCLK | Test Clock Input† |
| CLKSEL | Clock Input Select† |

†TCLK and CLKSEL are single-ended inputs, with internal 50 k Ω pulldown resistors.

Truth Table

| CLKSEL | CLKIN | CLKIN | TCLK | CLK _N | CLK _N |
|--------|-------|-------|------|------------------|------------------|
| L | L | H | X | L | H |
| L | H | L | X | H | L |
| H | X | X | L | L | H |
| H | X | X | H | H | L |

L = Low Voltage Level
H = High Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{CC} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50 mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|------------------------------------|-------|-------|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH(\text{Max})}$ or $V_{IL(\text{Min})}$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Single-Ended Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Single-Ended Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(\text{Min})}$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|------------------------------------|-------|-----|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH(\text{Max})}$ or $V_{IL(\text{Min})}$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Single-Ended Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Single-Ended Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(\text{Min})}$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|------------------------------------|-------|-----|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH(\text{Max})}$ or $V_{IL(\text{Min})}$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH(\text{Min})}$ or $V_{IL(\text{Max})}$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Single-Ended Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Single-Ended Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(\text{Min})}$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

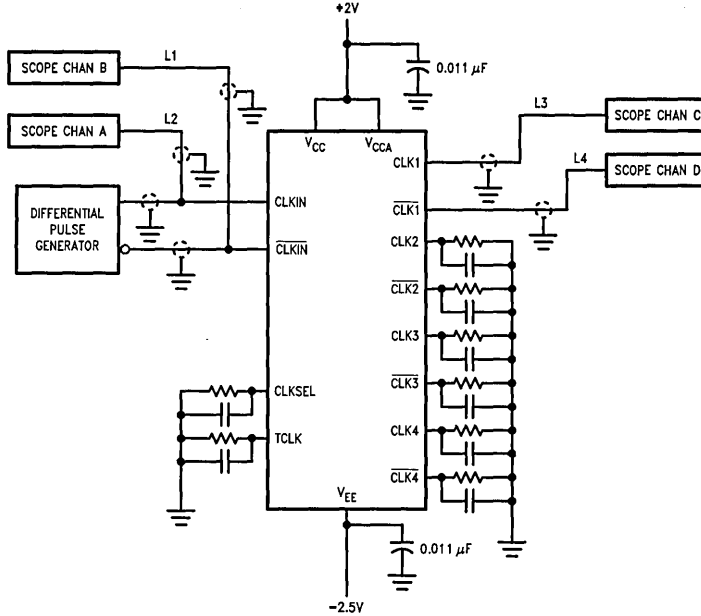
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------|---|---------------|-----|-------------------|-------------------------------|--------------------------------|
| V_{DIFF} | Input Voltage Differential | 150 | | | mV | Required for Full Output Swing |
| V_{CM} | Common Mode Voltage | $V_{CC} - 2V$ | | $V_{CC} - 0.5V$ | V | |
| I_{IH} | Input High Current CLKIN, \overline{CLKIN} TCLK CLKSEL | | | 107 300 260 | μA μA μA | $V_{IN} = V_{IH(Max)}$ |
| I_{CBO} | Input Leakage Current | -10 | | | μA | $V_{IN} = V_{EE}$ |
| I_{EE} | Power Supply Current | -70 | | -30 | mA | |

AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|--------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay CLKIN, \overline{CLKIN} to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$ | 0.63 | 0.83 | 0.65 | 0.85 | 0.70 | 0.93 | ns | Figures 1, 3 |
| t_{PLH} t_{PHL} | Propagation Delay, TCLK to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$ | 0.50 | 1.20 | 0.50 | 1.20 | 0.50 | 1.20 | ns | Figures 1, 2 |
| t_{PLH} t_{PHL} | Propagation Delay, CLKSEL to $CLK_{(1-4)}$, $\overline{CLK}_{(1-4)}$ | 0.60 | 1.40 | 0.60 | 1.40 | 0.60 | 1.40 | ns | Figures 1, 2 |
| t_{SG-G} | Skew Gate to Gate (Note 1) | | 75 | | 75 | | 75 | ps | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.35 | 0.80 | 0.30 | 0.75 | 0.25 | 0.75 | ns | Figures 1, 4 |

Note 1: Maximum output skew for any one device.



- Note 1: Shown for testing CLKIN to CLK1 in the differential mode.
- Note 2: L1, L2, L3 and L4 = equal length 50 Ω impedance lines.
- Note 3: All unused inputs and outputs are loaded with 50 Ω in parallel with ≤ 3 pF to GND.
- Note 4: Scope should have 50 Ω input terminator internally.

FIGURE 1. AC Test Circuit

TL/F/9842-3

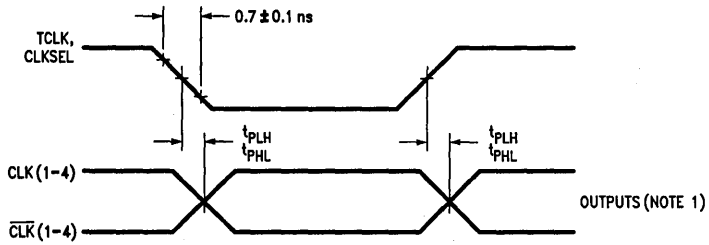


FIGURE 2. Propagation Delay, TCLK, CLKSEL to Outputs

TL/F/9842-4

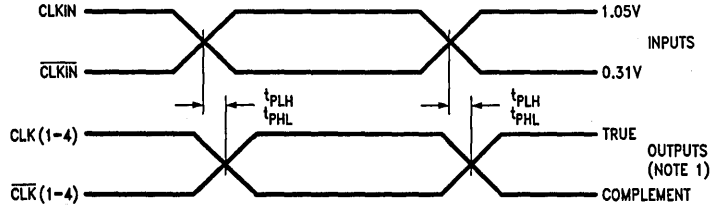


FIGURE 3. Propagation Delay, CLKIN/CLKIN to Outputs

TL/F/9842-5

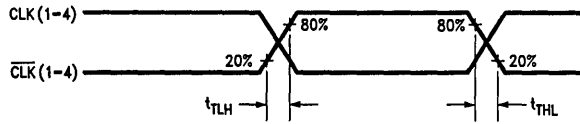


FIGURE 4. Transition Times

TL/F/9842-6

Note 1: The output to output skew, which is defined as the difference in the propagation delays between each of the four outputs on any one 100115 shall not exceed 75 ps.

F100117

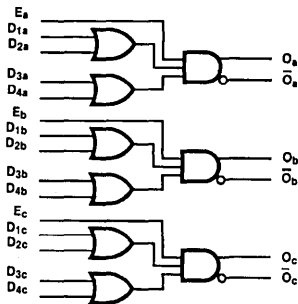
Triple 2-Wide OA/OAI Gate

General Description

The F100117 is a monolithic triple 2-wide OR/AND gate with true and complement outputs. All inputs have 50 k Ω pull-down resistors and all outputs are buffered.

Ordering Code: See Section 8

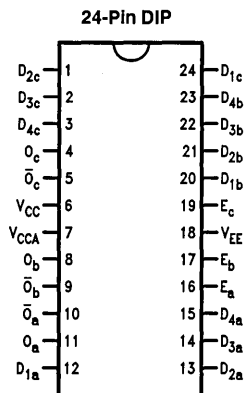
Logic Symbol



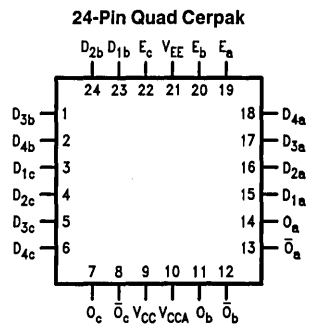
TL/F/9843-3

| Pin Names | Description |
|----------------------------------|----------------------------|
| D _{na} -D _{nc} | Data Inputs |
| E _a -E _c | Enable Inputs |
| O _a -O _c | Data Outputs |
| \bar{O}_a - \bar{O}_c | Complementary Data Outputs |

Connection Diagrams



TL/F/9843-1



TL/F/9843-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------------------|-----|-----|-----|---------|-------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 260 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -79 | -54 | -37 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.90 | 2.60 | 0.90 | 2.50 | 0.90 | 2.60 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.90 | 2.40 | 0.90 | 2.30 | 0.90 | 2.40 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay Enable to Output | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.20 | 0.45 | 1.10 | 0.45 | 1.20 | ns | |

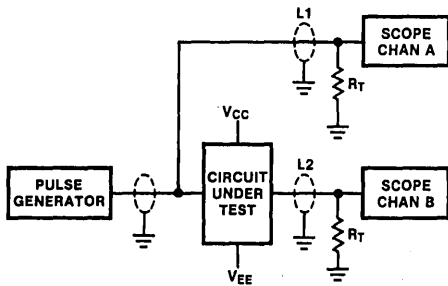


FIGURE 1. AC Test Circuit

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- $L1$ and $L2 =$ equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- $C_L =$ Fixture and stray capacitance $\leq 3 pF$

TL/F/9843-5

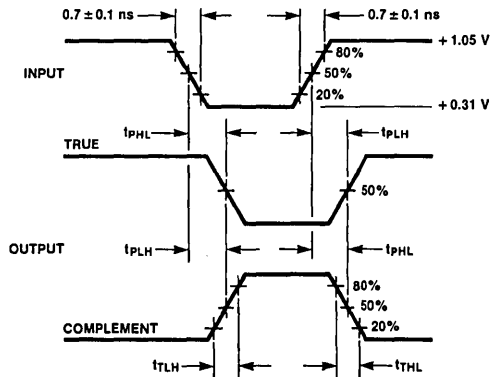


FIGURE 2. Propagation Delay and Transition Times

TL/F/9843-6



F100118

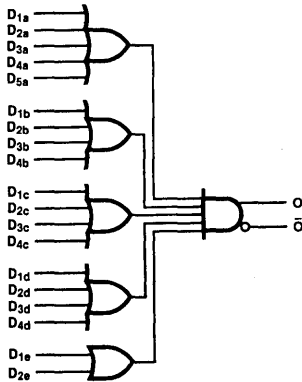
5-Wide 5, 4, 4, 4, 2 OA/OAI Gate

General Description

The F100118 is a monolithic 5-wide 5, 4, 4, 4, 2 OR/AND gate with true complementary outputs. All inputs have 50 k Ω pull-down resistors and all outputs are buffered.

Ordering Code: See Section 8

Logic Symbol

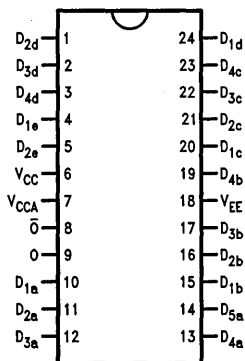


| Pin Names | Description |
|-----------------|--------------|
| $D_{na}-D_{ne}$ | Data Inputs |
| O, \bar{O} | Data Outputs |

TL/F/9844-3

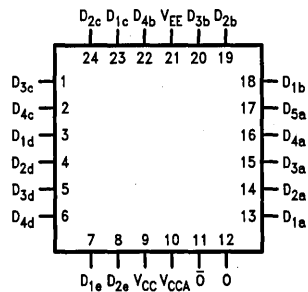
Connection Diagrams

24-Pin DIP



TL/F/9844-1

24-Pin Quad Cerpak



TL/F/9844-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

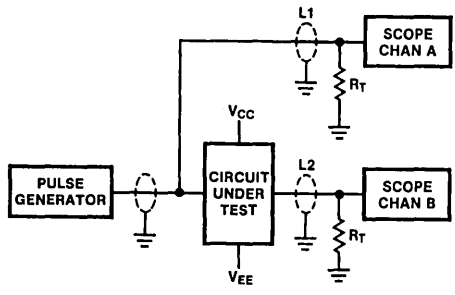
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------------------|-----|-----|-----|---------|-------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 350 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -92 | -69 | -42 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.85 | 2.50 | 0.95 | 2.50 | 0.95 | 2.70 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.50 | 0.45 | 1.60 | ns | |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.85 | 2.30 | 0.95 | 2.30 | 0.95 | 2.50 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

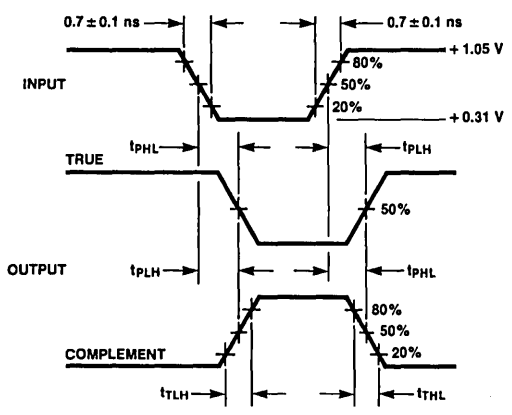


TL/F/9844-5

FIGURE 1. AC Test Circuit

Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF



TL/F/9844-6

FIGURE 2. Propagation Delay and Transition Times



F100121 9-Bit Inverter

General Description

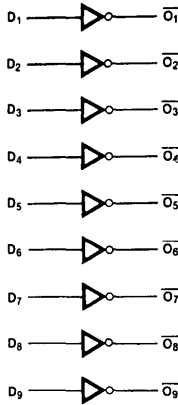
The F100121 is a monolithic 9-bit inverter. The device contains nine inverting buffer gates with single input and output. All inputs have 50 kΩ pull-down resistors.

Refer to the F100321 Datasheet for:

- PCC Packaging
- Lower Power
- Military Versions
- Extended Voltage Specs (-4.2V to -5.7V)

Ordering Code: See Section 8

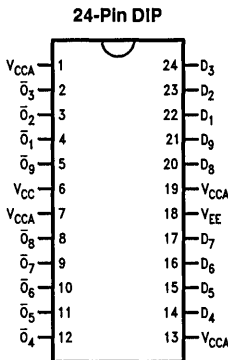
Logic Symbol



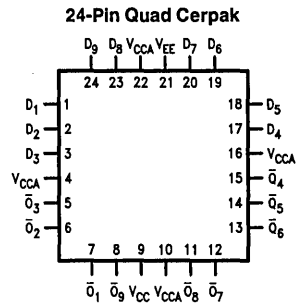
TL/F/9845-3

| Pin Names | Description |
|--------------------------------|--------------|
| D ₁ -D ₉ | Data Inputs |
| \bar{O}_1 - \bar{O}_9 | Data Outputs |

Connection Diagrams



TL/F/9845-1



TL/F/9845-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------|-----|-----|-----|---------|-------------------------|
| I_{IH} | Input HIGH Current | | | 350 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -96 | -70 | -46 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.60 | 0.45 | 1.45 | 0.45 | 1.60 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.40 | ns | |

Cerpak AC Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.40 | 0.45 | 1.25 | 0.45 | 1.40 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |

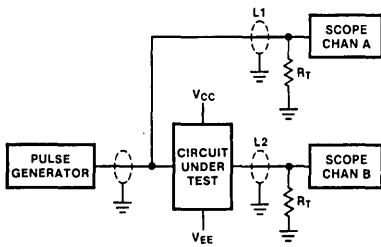


FIGURE 1. AC Test Circuit

TL/F/9845-5

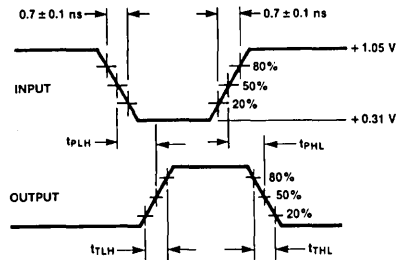


FIGURE 2. Propagation Delay and Transition Times

TL/F/9845-6

Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

$L1$ and $L2$ = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope.

Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE} .

All unused outputs are loaded with 50Ω to GND.

C_L = Fixture and stray capacitance $\leq 3 pF$.

F100122

9-Bit Buffer

General Description

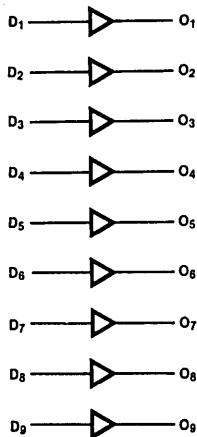
The F100122 is a monolithic 9-bit buffer. The device contains nine non-inverting buffer gates with single input and output. All inputs have 50 k Ω pull-down resistors and all outputs are buffered.

Refer to the F100322 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

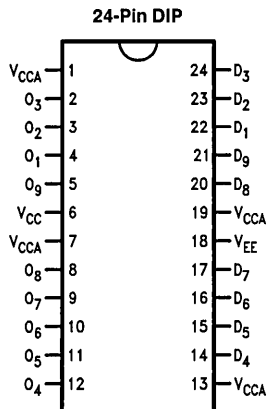
Logic Symbol



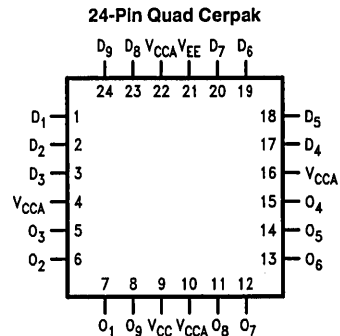
TL/F/9846-3

| Pin Names | Description |
|---------------------------------|--------------|
| D ₁ , D ₉ | Data Inputs |
| O ₁ , O ₉ | Data Outputs |

Connection Diagrams



TL/F/9846-1



TL/F/9846-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------|-----|-----|-----|---------|-------------------------|
| I_{IH} | Input HIGH Current | | | 350 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -96 | -70 | -46 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.60 | 0.45 | 1.45 | 0.45 | 1.60 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.40 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.45 | 1.40 | 0.45 | 1.25 | 0.45 | 1.40 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.30 | ns | |

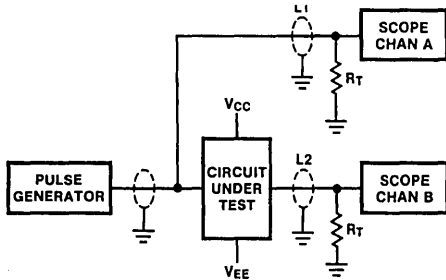


FIGURE 1. AC Test Circuit

TL/F/9846-5

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- $L1$ and $L2 =$ equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- $C_L =$ Fixture and stray capacitance $\leq 3 pF$

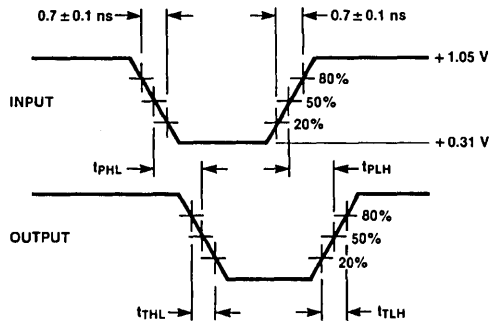


FIGURE 2. Propagation Delay and Transition Times

TL/F/9846-6



F100123 Hex Bus Driver

General Description

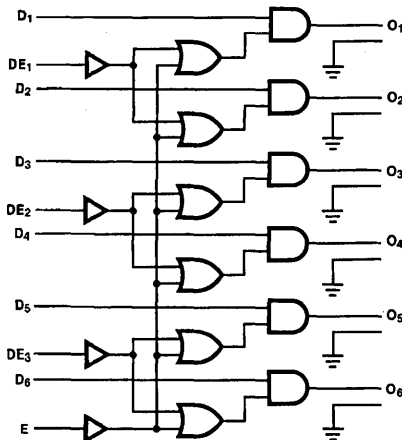
The F100123 is a monolithic device containing six bus drivers capable of driving terminated lines with terminations as low as 25Ω. To reduce crosstalk, each output has its respective ground connection. Transition times were designed to be longer than on other F100K devices. The driver itself performs the positive logic AND of a data input (D₁-D₆) and the OR of two select inputs (E and either DE₁, DE₂ or DE₃).

Enabling of data is possible in multiples of two, i.e., 2, 4 or all 6 paths. All inputs have 50 kΩ pull-down resistors.

The output voltage LOW level is designed to be more negative than normal ECL outputs (cut off state). This allows an emitter-follower output transistor to turn off when the termination supply is -2.0V and thus present a high impedance to the data bus.

Ordering Code: See Section 8

Logic Symbol

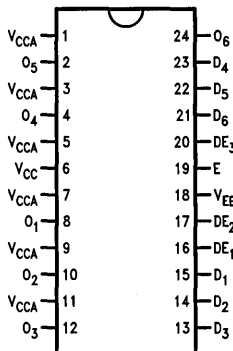


TL/F/9847-2

| Pin Names | Description |
|----------------------------------|---------------------|
| D ₁ -D ₆ | Data Inputs |
| DE ₁ -DE ₃ | Dual Enable Inputs |
| E | Common Enable Input |
| O ₁ -O ₆ | Data Outputs |

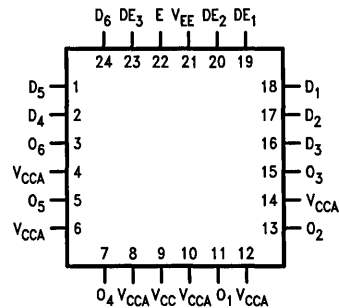
Connection Diagrams

24-Pin DIP



TL/F/9847-1

24-Pin Quad Cerpak



TL/F/9847-3

DC Electrical Characteristics $V_{EE} = -4.8V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|-------------------------------------|-------|-----|-------|---------|--|--------------------------------------|
| V_{OH} | Output HIGH Voltage | -1035 | | -870 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 25 Ω to -2.0V |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 25 Ω to -2.0V |
| V_{OL} | Output LOW Voltage Cut-Off State | | | -2200 | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 25 Ω to -2.3V |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ | |

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current Common Enable Data and Dual Enable | | | 330 260 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -235 | -170 | -113 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

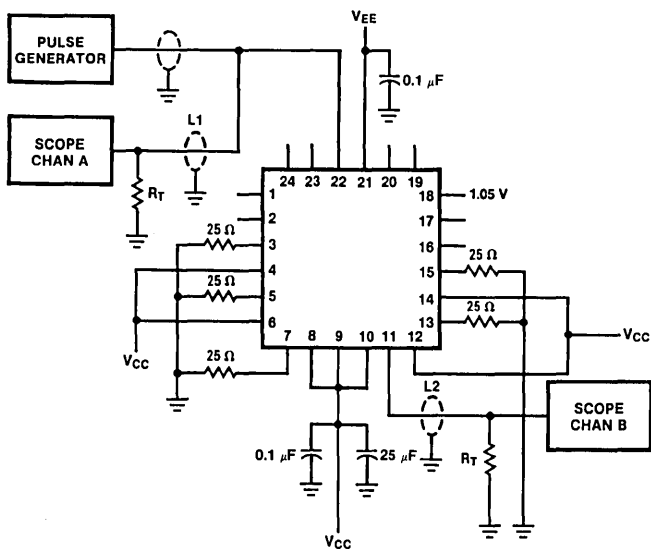
| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|-----------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} | Propagation Delay | 2.00 | 4.30 | 1.95 | 4.30 | 2.00 | 4.60 | ns | Figures 1 and 2 |
| t_{PHL} | Data to Output | 1.00 | 2.40 | 1.00 | 2.40 | 1.10 | 2.60 | | |
| t_{PLH} | Propagation Delay | 2.30 | 4.70 | 2.00 | 4.70 | 2.30 | 5.10 | | |
| t_{PHL} | Dual Enable to Output | 1.40 | 3.00 | 1.40 | 3.00 | 1.40 | 3.40 | | |
| t_{PLH} | Propagation Delay | 2.60 | 5.40 | 2.50 | 5.30 | 2.80 | 5.80 | | |
| t_{PHL} | Common Enable to Output | 1.50 | 3.20 | 1.50 | 3.30 | 1.50 | 3.60 | ns | |
| t_{TLH} | Transition Time 20% to 80%, 80% to 20% | 0.70 | 2.10 | 0.70 | 1.80 | 0.70 | 2.20 | ns | |
| t_{THL} | | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | | |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|-----------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} | Propagation Delay | 2.00 | 4.10 | 1.95 | 4.10 | 2.00 | 4.40 | ns | Figures 1 and 2 |
| t_{PHL} | Data to Output | 1.00 | 2.20 | 1.00 | 2.20 | 1.10 | 2.40 | | |
| t_{PLH} | Propagation Delay | 2.30 | 4.50 | 2.00 | 4.50 | 2.30 | 4.90 | | |
| t_{PHL} | Dual Enable to Output | 1.40 | 2.80 | 1.40 | 2.80 | 1.40 | 3.20 | | |
| t_{PLH} | Propagation Delay | 2.60 | 5.20 | 2.50 | 5.10 | 2.80 | 5.60 | | |
| t_{PHL} | Common Enable to Output | 1.50 | 3.00 | 1.50 | 3.10 | 1.50 | 3.40 | ns | |
| t_{TLH} | Transition Time 20% to 80%, 80% to 20% | 0.70 | 2.00 | 0.70 | 1.70 | 0.70 | 2.10 | ns | |
| t_{THL} | | 0.45 | 1.30 | 0.45 | 1.20 | 0.45 | 1.30 | | |

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

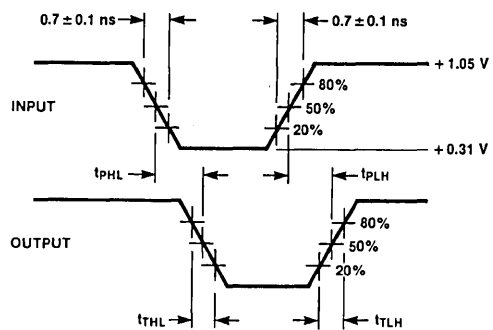
Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.



Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 C_L = Fixture and stray capacitance $\leq 3 pF$
 Pin numbers shown are for flatpak; for DIP see logic symbol

TL/F/9847-5

FIGURE 1. AC Test Circuit



TL/F/9847-6

FIGURE 2. Propagation Delay and Transition Times



F100124 Hex TTL-to-ECL Translator

General Description

The F100124 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable input (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator or as a differential line driver. The output levels are voltage compensated.

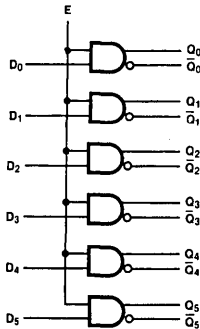
When the circuit is used in the differential mode, the F100124, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The V_{EE} and V_{TTL} power may be applied in either order.

Refer to the F100324 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs ($-4.2V$ to $-5.7V$)

Ordering Code: See Section 8

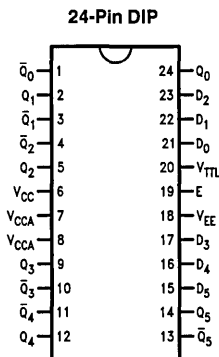
Logic Symbol



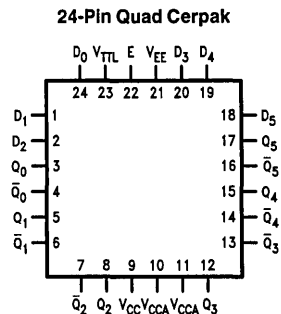
TL/F/9848-3

| Pin Names | Description |
|---------------------------|----------------------------|
| D_0 – D_5 | Data Inputs |
| E | Enable Input |
| Q_0 – Q_5 | Data Outputs |
| \bar{Q}_0 – \bar{Q}_5 | Complementary Data Outputs |

Connection Diagrams



TL/F/9848-1



TL/F/9848-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-----------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | +150°C |
| Case Temperature under Bias (T _C) | 0°C to +85°C |

| | |
|--|---------------------------|
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| V _{TTL} Pin Potential to Ground Pin | +6.0V to -0.5V |
| Input Voltage (DC) | -0.5V to V _{TTL} |
| Output Current (DC Output HIGH) | -50 mA |
| Operating Range (V _{EE}) (Note 2) | -5.7V to -4.2V |

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-------|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V _{OH} C | Output HIGH Voltage | -1030 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1595 | | | |

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1035 | | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1045 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$, $T_C = 0^\circ C$ to $+85^\circ C$

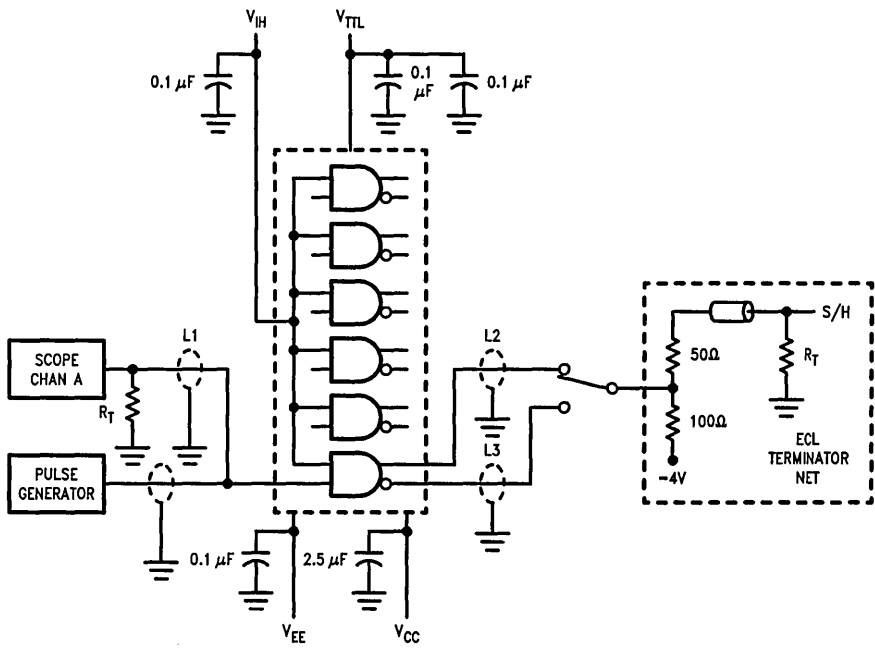
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-----------|--|-------------------------------|------|-----------|---------|--|
| V_{IH} | Input HIGH Voltage | 2.0 | | 5.0 | V | Guaranteed HIGH Signal for All Inputs |
| V_{IL} | Input LOW Voltage | 0 | | 0.8 | V | Guaranteed LOW Signal for All Inputs |
| V_{CD} | Input Clamp Diode Voltage | -1.5 | | | V | $I_{IN} = -10$ mA |
| I_{IH} | Input HIGH Current Data Enable | | | 20 120 | μA | $V_{IN} = +2.4V$, All Other Inputs $V_{IN} = GND$ |
| | Input HIGH Current Breakdown Test, All Inputs | | | 1.0 | mA | $V_{IN} = +5.5V$, All Other Inputs = GND |
| I_{IL} | Input LOW Current Data Enable | -1.6 -9.6 | | | mA | $V_{IN} = +0.4V$, All Other Inputs $V_{IN} = V_{IH}$ |
| | I_{EE} | V_{EE} Power Supply Current | -140 | -96 | -52 | mA |
| I_{TTL} | V_{TTL} Power Supply Current | | 44 | 75 | mA | All Inputs $V_{IN} = GND$ |

Ceramic Dual-In-Line Package AC Electric Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data and Enable to Output | 0.50 | 3.00 | 0.50 | 2.90 | 0.50 | 3.00 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data and Enable to Output | 0.50 | 2.80 | 0.50 | 2.70 | 0.50 | 2.80 | ns | Figures 1 and 2 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |



TL/F/9848-5

FIGURE 1. AC Test Circuit

- Notes:**
 $V_{CC}, V_{CCA} = +0V, V_{EE} = -4.5V, V_{TTL} = +5.0V, V_{IH} = +3.0V$
 $L1, L2$ and $L3 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC}, V_{EE} and V_{TTL}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance $\leq 3 pF$

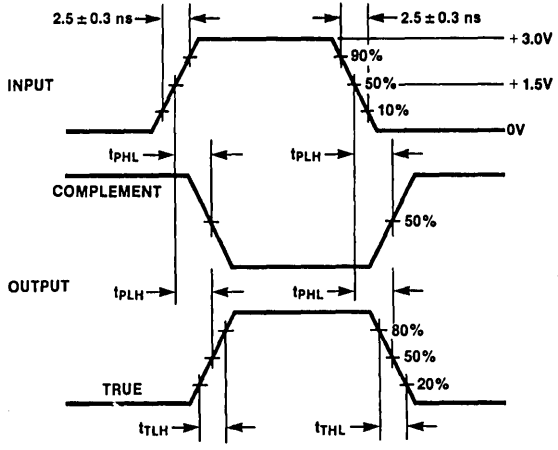


FIGURE 2. Propagation Delay and Transition Times

TL/F/9848-6



F100125 Hex ECL-to-TTL Translator

General Description

The F100125 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation or for use in Schmitt trigger applications. All inputs have 50 k Ω pull-down resistors; therefore, the outputs will go LOW when the inputs are left unconnected.

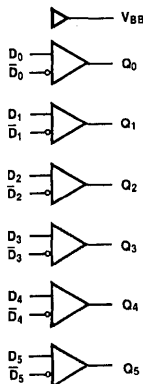
When used in the differential mode, the inputs have a common mode rejection of +1V, making this device tolerant of ground offsets and transients between the signal source and the translator. The V_{EE} and V_{TTL} power may be applied in either order.

Refer to the F100325 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

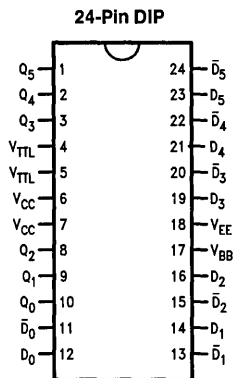
Logic Symbol



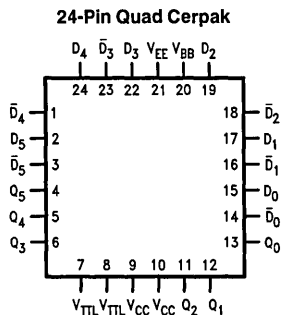
TL/F/9849-3

| Pin Names | Description |
|---------------------------|-----------------------|
| D_0 - D_5 | Data Inputs |
| \bar{D}_0 - \bar{D}_5 | Inverting Data Inputs |
| Q_0 - Q_5 | Data Outputs |

Connection Diagrams



TL/F/9849-1



TL/F/9849-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-----------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | +150°C |
| Case Temperature under Bias (T _C) | 0°C to +85°C |

| | |
|--|--------------------------|
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| V _{TTL} Pin Potential to Ground Pin | +6.0V to -0.5V |
| Input Voltage (DC) | V _{EE} to +0.5V |
| Output Current (DC Output HIGH) | -50 mA |
| Operating Range (Note 2) | -5.7V to -4.2V |

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) |
|-----------------|---------------------------------|-------|-------|-------|-------|---|
| V _{BB} | Output Reference Voltage | -1380 | -1320 | -1260 | mV | I _{VBB} = -2.1 mA |
| V _{IH} | Single-Ended Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs (with One Input Tied to V _{BB}) |
| V _{IL} | Single-Ended Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs (with One Input Tied to V _{BB}) |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) |
|-----------------|---------------------------------|-------|-------|-------|-------|---|
| V _{BB} | Output Reference Voltage | -1396 | -1320 | -1244 | mV | I _{VBB} = -2.1 mA |
| V _{IH} | Single-Ended Input HIGH Voltage | -1150 | | -880 | mV | Guaranteed HIGH Signal for All Inputs (with One Input Tied to V _{BB}) |
| V _{IL} | Single-Ended Input LOW Voltage | -1810 | | -1490 | mV | Guaranteed LOW Signal for All Inputs (with One Input Tied to V _{BB}) |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) |

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) |
|-----------------|---------------------------------|-------|-------|-------|-------|---|
| V _{BB} | Output Reference Voltage | -1396 | -1320 | -1244 | mV | I _{VBB} = -2.1 mA |
| V _{IH} | Single-Ended Input HIGH Voltage | -1150 | | -880 | mV | Guaranteed HIGH Signal for All Inputs (with One Input Tied to V _{BB}) |
| V _{IL} | Single-Ended Input LOW Voltage | -1810 | | -1490 | mV | Guaranteed LOW Signal for All Inputs (with One Input Tied to V _{BB}) |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------|--------------------------------|------|-----|-----|---------|--|
| V_{OH} | Output HIGH Voltage | 2.5 | | | V | $I_{OH} = -2.0$ mA $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ |
| V_{OL} | Output LOW Voltage | | | 0.5 | V | $I_{OL} = 20$ mA |
| V_{DIFF} | Input Voltage Differential | 150 | | | mV | Required for Full Output Swing |
| V_{CM} | Common Mode Voltage | | | 1.0 | V | Permissible $\pm V_{CM}$ with Respect to V_{BB} |
| I_{IH} | Input HIGH Current | | | 350 | μA | $V_{IN} = V_{IH} (Max)$, $D_0-D_5 = V_{BB}$, $\bar{D}_0-\bar{D}_5 = V_{IL} (Min)$ |
| I_{IL} | Input LOW Current | 0.5 | | | μA | $V_{IN} = V_{IL} (Min)$, $D_0-D_5 = V_{BB}$ |
| I_{OS} | Output Short-Circuit Current | -100 | | -40 | mA | $V_{OUT} = GND^*$ |
| I_{EE} | V_{EE} Power Supply Current | -85 | -60 | -40 | mA | $D_0-D_5 = V_{BB}$ |
| I_{TTL} | V_{TTL} Power Supply Current | | 75 | 115 | mA | $D_0-D_5 = V_{BB}$ |

*Test one output at a time.

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|-------------------------------------|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.80 | 3.50 | 0.90 | 3.70 | 1.00 | 4.00 | ns | Figures 1 and 2 |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|-------------------------------------|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 0.80 | 3.30 | 0.90 | 3.50 | 1.00 | 3.80 | ns | Figures 1 and 2 |

Truth Table

| Inputs | | Outputs |
|----------|-------------|---------|
| D_n | \bar{D}_n | Q_n |
| L | H | L |
| H | L | H |
| L | L | U |
| H | H | U |
| Open | Open | L |
| V_{EE} | V_{EE} | L |
| L | V_{BB} | L |
| H | V_{BB} | H |
| V_{BB} | L | H |
| V_{BB} | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
U = Undefined

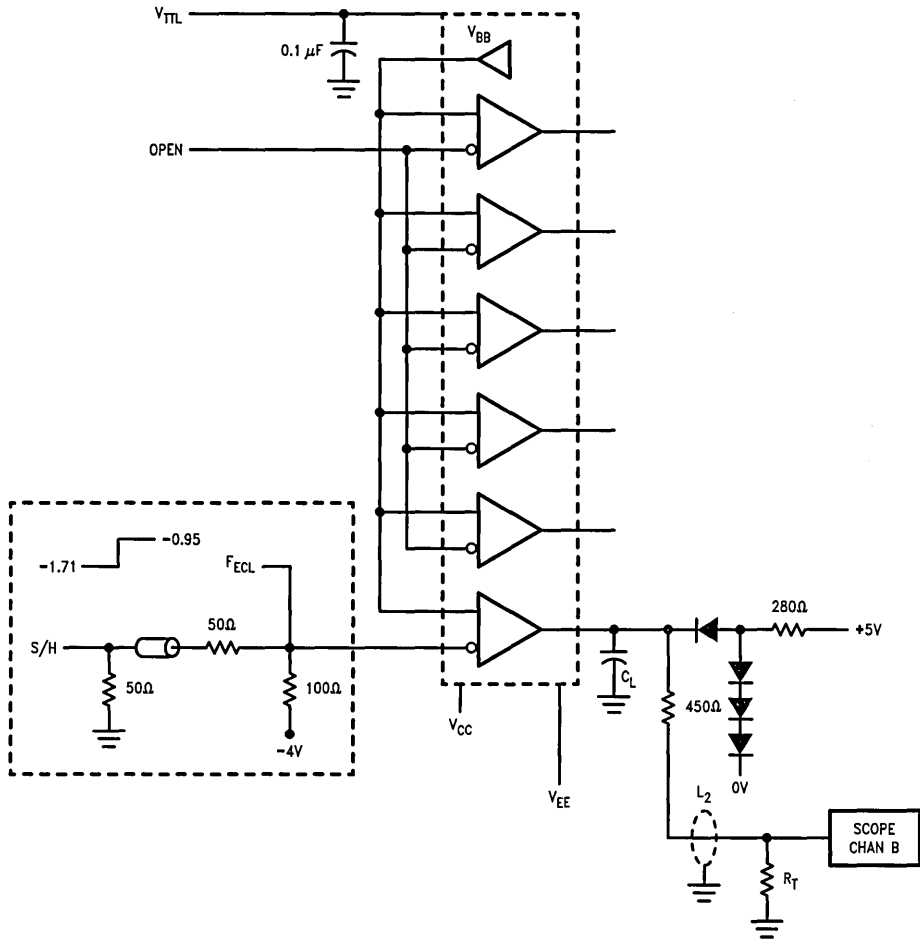


FIGURE 1. AC Test Circuit

TL/F/9849-5

Notes:

- V_{CC} = 0V, V_{EE} = -4.5V, V_{TTL} = +5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
- All unused outputs are loaded with 500Ω to GND
- C_L = Fixture and stray capacitance = 15 pF

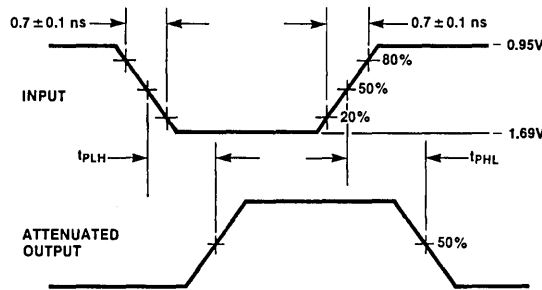


FIGURE 2. Propagation Delay Times

TL/F/9849-6



F100126 9-Bit Backplane Driver

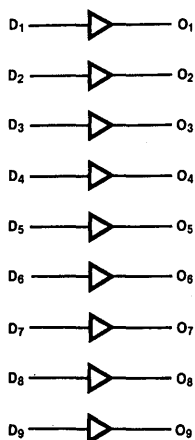
General Description

The F100126 contains nine independent, high-speed, buffer gates each with a single input and a single output. The gates are non-inverting. These buffers are useful in bus-oriented systems where minimal output loading or bus isolation is desired. The output transition times are longer to minimize noise when used as a backplane driver. All inputs have 50 k Ω pull-down resistors.

tion is desired. The output transition times are longer to minimize noise when used as a backplane driver. All inputs have 50 k Ω pull-down resistors.

Ordering Code: See Section 8

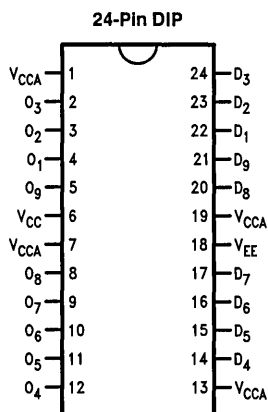
Logic Symbol



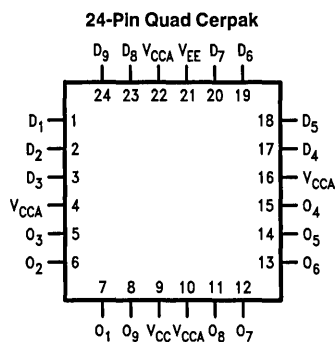
TL/F/9850-3

| Pin Names | Description |
|--------------------------------|--------------|
| D ₁ –D ₉ | Data Inputs |
| O ₁ –O ₉ | Data Outputs |

Connection Diagrams



TL/F/9850-1



TL/F/9850-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{EE} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------|-----|-----|-----|---------|-------------------------|
| I_{IH} | Input HIGH Current | | | 350 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -96 | -70 | -46 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 1.05 | 2.75 | 1.05 | 2.75 | 1.05 | 2.75 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 1.15 | 3.40 | 1.15 | 3.40 | 1.05 | 3.40 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 1.05 | 2.55 | 1.05 | 2.55 | 1.05 | 2.55 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 1.15 | 3.30 | 1.15 | 3.30 | 1.05 | 3.30 | ns | |

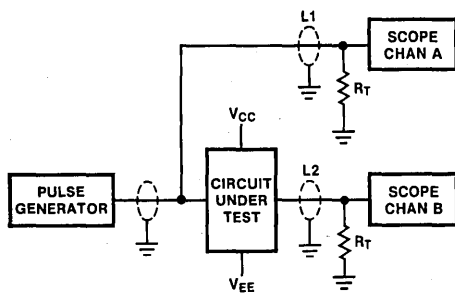


FIGURE 1. AC Test Circuit

TL/F/9850-5

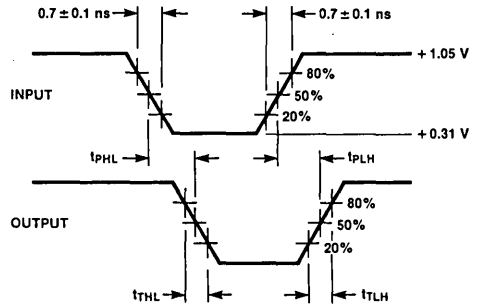


FIGURE 2. Propagation Delay and Transition Times

TL/F/9850-6

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50 Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50 Ω to GND
- $C_L =$ Fixture and stray capacitance ≤ 3 pF

F100128

ECL/TTL Bi-Directional Translator

General Description

The F100128 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the F100128 transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is $-2.0V$, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The F100128 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have $50\text{ k}\Omega$ pull-down resistors.

Features

- Bi-directional translation
- ECL high impedance outputs
- Latched outputs
- FAST® TTL outputs
- TRI-STATE® outputs

Refer to the F100328 datasheet for:

PCC Packaging

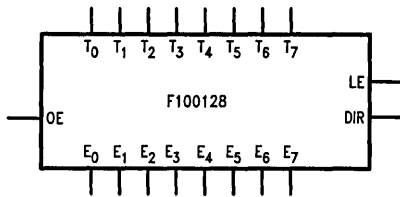
Lower Power

Military Versions

Extended voltage specs ($-4.2V$ to $-5.7V$)

Ordering Code: See Section 8

Logic Symbol



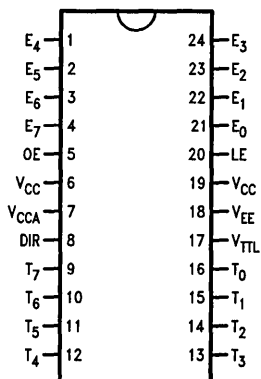
TL/F/9851-3

| Pin Names | Description |
|--------------------------------|-------------------------|
| E ₀ -E ₇ | ECL Data I/O |
| T ₀ -T ₇ | TTL Data I/O |
| OE | Output Enable Input |
| LE | Latch Enable Input |
| DIR | Direction Control Input |

All pins function at 100K ECL levels except for T₀-T₇.

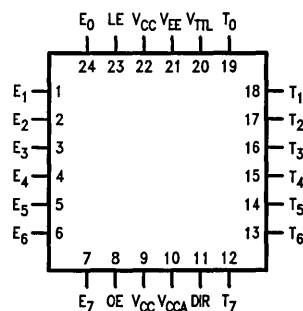
Connection Diagrams

24-Pin DIP



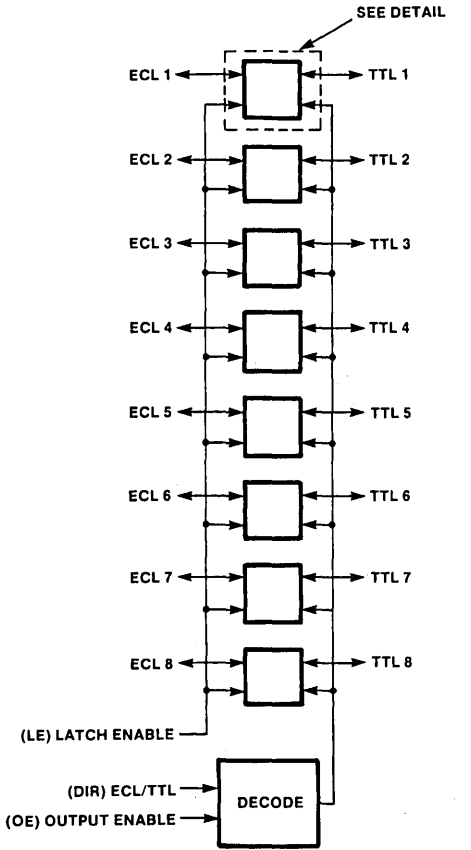
TL/F/9851-1

24-Pin Quad Cerpak



TL/F/9851-2

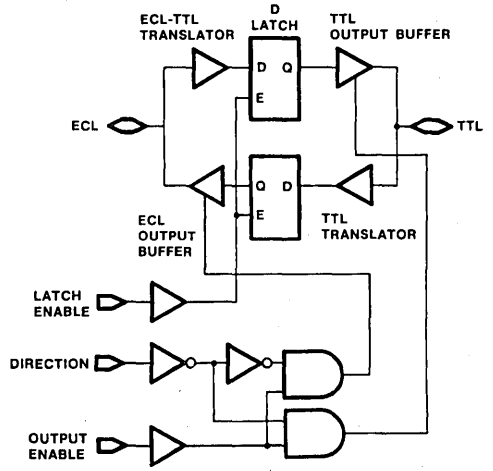
Functional Diagram



TL/F/9851-4

Note: LE, DIR and OE use ECL logic levels

Detail



TL/F/9851-5

Truth Table

| OE | DIR | LE | ECL Port | TTL Port | Notes |
|----|-----|----|---------------|----------|-------|
| L | X | L | LOW (Cut-Off) | Z | |
| L | L | H | Input | Z | 1, 3 |
| L | H | H | LOW (Cut-Off) | Input | 2, 3 |
| H | L | L | L | L | 1, 4 |
| H | L | L | H | H | 1, 4 |
| H | L | H | X | Latched | 1, 3 |
| H | H | L | L | L | 2, 4 |
| H | H | L | H | H | 2, 4 |
| H | H | H | Latched | X | 2, 3 |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------------------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature | +150°C |
| Case Temperature under Bias | 0°C to +85°C |
| V _{EE} Pin Potential to Ground Pin | -7.0V to +0.5V |
| V _{TTL} Pin Potential to Ground Pin | +6.0V to -0.5V |
| ECL Input Voltage (DC) | V _{EE} to +0.5V |
| ECL Output Current (DC Output HIGH) | -50 mA |
| TTL Input Voltage (Note 2) | -0.5V to +7.0V |
| TTL Input Current (Note 2) | -30 mA to +5.0 mA |

Voltage Applied to Output in HIGH State

TRI-STATE Output -0.5V to +5.5V

Current Applied to TTL

Output in LOW State (Max) Twice the Rated I_{OL} (mA)

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

| | | | |
|-------------------------|------------------|--------------|----------------|
| Supply Voltage (Note 1) | V _{EE} | 0°C to +85°C | -5.7V to -4.2V |
| | V _{TTL} | | +4.5V to +5.5V |

Note 1: Parametric values specified at V_{EE} = -4.2V to -4.8V.

TTL-to-ECL DC Electrical Characteristics

V_{EE} = -4.2V to -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------------|--|-------|-------|-------|-------|--|
| V _{OH} | Output High Voltage | -1020 | -955 | -870 | mV | V _{EE} = -4.2V, 50Ω to -2V |
| | | -1025 | | -880 | mV | V _{EE} = -4.5V, 50Ω to -2V |
| | | -1035 | | -880 | mV | V _{EE} = -4.8V, 50Ω to -2V |
| V _{OL} | Output Low Voltage | -1810 | -1705 | -1605 | mV | V _{EE} = -4.2V, 50Ω to -2V |
| | | -1810 | | -1620 | mV | V _{EE} = -4.5V, 50Ω to -2V |
| | | -1830 | | -1620 | mV | V _{EE} = -4.8V, 50Ω to -2V |
| | Cutoff Voltage | | -2000 | -1930 | mV | OE or DIR Low, V _{EE} = -4.2V, 50Ω to -2V |
| | | | -2000 | -1950 | mV | V _{EE} = -4.5V, 50Ω to -2V |
| | | | -2000 | -1950 | mV | V _{EE} = -4.8V, 50Ω to -2V |
| V _{OHC} | Output High Voltage Corner Point High | -1030 | | | mV | V _{EE} = -4.2V, 50Ω to -2V |
| | | -1035 | | | mV | V _{EE} = -4.5V, 50Ω to -2V |
| | | -1045 | | | mV | V _{EE} = -4.8V, 50Ω to -2V |
| V _{OLC} | Output Low Voltage Corner Point Low | | | -1595 | mV | V _{EE} = -4.2V, 50Ω to -2V |
| | | | | -1610 | mV | V _{EE} = -4.5V, 50Ω to -2V |
| | | | | -1610 | mV | V _{EE} = -4.8V, 50Ω to -2V |
| V _{IH} | Input High Voltage | 2.0 | | | V | Over V _{TTL} , V _{EE} , T _C Range |
| V _{IL} | Input Low Voltage | | | 0.8 | V | Over V _{TTL} , V _{EE} , T _C Range |
| I _{IH} | Input High Current | | | 70 | μA | V _{IN} = +2.7V |
| | Breakdown Test | | | 1.0 | mA | V _{IN} = +5.5V |
| I _{IL} | Input Low Current | | | -1.0 | mA | V _{IN} = +0.5V |
| V _{FCD} | Input Clamp Diode Voltage | | | -1.2 | V | I _{IN} = -18 mA |
| I _{EE} | V _{EE} Supply Current | -250 | -175 | -125 | mA | LE Low, OE and DIR High |

ECL-to-TTL DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$, $C_L = 50$ pF, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------|-------------------------------|-------|-----|-------|---------|--|
| V_{OH} | Output High Voltage | 2.7 | 3.1 | | V | $I_{OH} = -3$ mA, $V_{TTL} = 4.75V$ $I_{OH} = -3$ mA, $V_{TTL} = 4.50V$ |
| | | 2.4 | 2.9 | | V | |
| V_{OL} | Output Low Voltage | | 0.3 | 0.5 | V | $I_{OL} = 24$ mA, $V_{TTL} = 4.50V$ |
| V_{IH} | Input High Voltage | -1150 | | -870 | mV | $V_{EE} = -4.2V$ |
| | | -1165 | | -880 | mV | $V_{EE} = -4.5V$ |
| | | -1165 | | -880 | mV | $V_{EE} = -4.8V$ |
| V_{IL} | Input Low Voltage | -1810 | | -1475 | mV | $V_{EE} = -4.2V$ |
| | | -1810 | | -1475 | mV | $V_{EE} = -4.5V$ |
| | | -1810 | | -1490 | mV | $V_{EE} = -4.8V$ |
| I_{IH} | Input High Current | | | 200 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{IL} | Input Low Current | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ |
| I_{OZHT} | TRI-STATE Current Output High | | | 70 | μA | $V_{OUT} = +2.7V$ |
| I_{OZLT} | TRI-STATE Current Output Low | | | -1.0 | mA | $V_{OUT} = +0.5V$ |
| I_{OS} | Output Short-Circuit Current | -60 | | -225 | mA | $V_{OUT} = 0.0V$, $V_{TTL} = +5.5V$ |
| I_{TTL} | V_{TTL} Supply Current | | 155 | 200 | mA | TTL Outputs Low TTL Outputs High TTL Outputs in TRI-STATE |
| | | | 90 | 120 | mA | |
| | | | 120 | 160 | mA | |

Cerpak TTL-to-ECL AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = 25^\circ C$ | | $T_C = 85^\circ C$ | | Units | Conditions |
|-------------|---|-------------------|-----|--------------------|-----|--------------------|-----|-------|---------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} | T_n to E_n (Transparent) | 1.0 | 3.3 | 1.0 | 3.3 | 1.0 | 3.3 | ns | Figures 1 & 2 |
| t_{PHL} | | 1.1 | 3.7 | 1.1 | 3.7 | 1.4 | 4.3 | ns | |
| t_{PLH} | LE to E_n | 2.2 | 4.6 | 2.2 | 4.6 | 2.7 | 5.4 | ns | Figures 1 & 2 |
| t_{PHL} | | 2.0 | 4.3 | 2.0 | 4.3 | 2.4 | 5.0 | ns | |
| t_{PZH} | OE to E_n (Cutoff to High) | 1.4 | 4.5 | 1.4 | 4.5 | 1.5 | 5.0 | ns | Figures 1 & 2 |
| t_{PHZ} | DIR to E_n (High to Cutoff) | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | ns | Figures 1 & 2 |
| t_{PHZ} | OE to E_n (High to Cutoff) | 1.0 | 3.5 | 1.0 | 3.5 | 1.0 | 4.0 | ns | Figures 1 & 2 |
| t_{set} | T_n to LE | 1.0 | | 1.0 | | 1.0 | | ns | Figures 1 & 2 |
| t_{hold} | T_n to LE | 2.0 | | 2.0 | | 2.0 | | ns | Figures 1 & 2 |
| $t_{pw(H)}$ | Pulse Width High, LE | 2.0 | | 2.0 | | 2.0 | | ns | Figures 1 & 2 |
| t_{TLH} | Transition Time 20% to 80%, 80% to 20% | 0.6 | 1.6 | 0.6 | 1.6 | 0.6 | 1.6 | ns | Figures 1 & 2 |
| t_{THL} | | | | | | | | | |

Cerpak ECL-to-TTL AC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -4.8V, V_{TTL} = +4.5V \text{ to } +5.5V, C_L = 50 \text{ pF}$

| Symbol | Parameter | T _C = 0°C | | T _C = 25°C | | T _C = 85°C | | Units | Conditions |
|--------------------------------------|---|----------------------|-------------|-----------------------|-------------|-----------------------|--------------|-------|---------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | E _n to T _n (Transparent) | 2.5 2.0 | 6.5 5.5 | 2.5 2.0 | 6.5 5.5 | 3.0 2.0 | 8.0 6.0 | ns | Figures 3 & 4 |
| t _{PLH} t _{PHL} | LE to T _n | 3.0 2.5 | 7.5 6.5 | 3.0 2.5 | 7.5 6.5 | 3.5 3.0 | 9.5 7.0 | ns | Figures 3 & 4 |
| t _{PZH} t _{PZL} | OE to T _n (Enable Time) | 3.0 4.0 | 7.5 9.5 | 3.0 4.0 | 7.5 9.5 | 3.5 4.5 | 8.5 10.0 | ns | Figures 3 & 5 |
| t _{PHZ} t _{PLZ} | OE to T _n (Disable Time) | 3.0 2.5 | 9.5 8.0 | 3.0 2.5 | 9.5 8.0 | 3.5 3.5 | 11.0 10.0 | ns | Figures 3 & 5 |
| t _{PHZ} t _{PLZ} | DIR to T _n (Disable Time) | 2.5 2.5 | 10.0 8.5 | 2.5 2.5 | 10.0 8.5 | 3.0 3.5 | 10.0 10.0 | ns | Figures 3 & 6 |
| t _{set} | E _n to LE | 1.5 | | 1.5 | | 1.5 | | ns | Figures 3 & 4 |
| t _{hold} | E _n to LE | 3.5 | | 3.5 | | 3.5 | | ns | Figures 3 & 4 |
| tpw(H) | Pulse Width High, LE | 2.0 | | 2.0 | | 2.0 | | ns | Figures 3 & 4 |

Ceramic Dual-In-Line Package TTL-to-ECL AC Electrical Characteristics

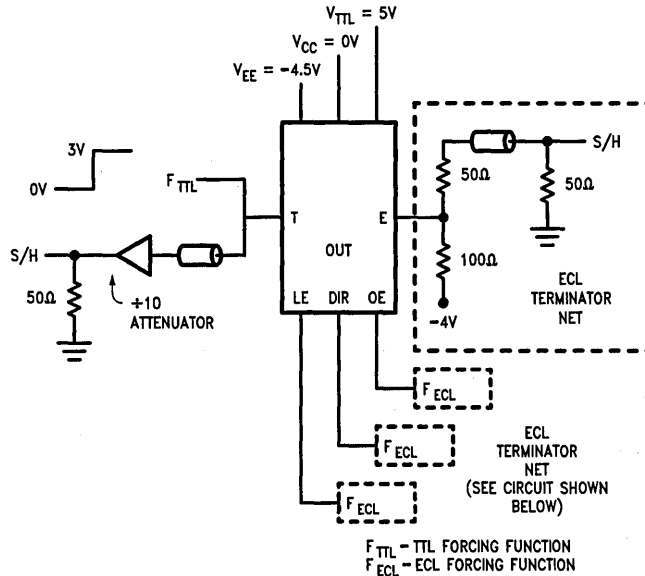
 $V_{EE} = -4.2V \text{ to } -4.8V, V_{TTL} = +4.5V \text{ to } +5.5V, V_{CC} = V_{CCA} = \text{GND}$

| Symbol | Parameter | T _C = 0°C | | T _C = 25°C | | T _C = 85°C | | Units | Conditions |
|--------------------------------------|---|----------------------|------------|-----------------------|------------|-----------------------|------------|----------|---------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PLH} t _{PHL} | T _N to E _n (Transparent) | 1.0 1.1 | 3.3 3.7 | 1.0 1.1 | 3.3 3.7 | 1.0 1.4 | 3.3 4.3 | ns ns | Figures 1 & 2 |
| t _{PLH} t _{PHL} | LE to E _n | 2.2 2.0 | 4.6 4.3 | 2.2 2.0 | 4.6 4.3 | 2.7 2.4 | 5.4 5.0 | ns ns | Figures 1 & 2 |
| t _{PZH} | OE to E _n (Cutoff to High) | 1.4 | 4.5 | 1.4 | 4.5 | 1.5 | 5.0 | ns | Figures 1 & 2 |
| t _{PHZ} | DIR to E _n (High to Cutoff) | 1.0 | 4.0 | 1.0 | 4.0 | 1.0 | 4.0 | ns | Figures 1 & 2 |
| t _{PHZ} | OE to E _n (High to Cutoff) | 1.0 | 3.5 | 1.0 | 3.5 | 1.0 | 4.0 | ns | Figures 1 & 2 |
| t _{set} | T _n to LE | 1.0 | | 1.0 | | 1.0 | | ns | Figures 1 & 2 |
| t _{hold} | T _n to LE | 2.0 | | 2.0 | | 2.0 | | ns | Figures 1 & 2 |
| tpw(H) | Pulse Width High, LE | 2.0 | | 2.0 | | 2.0 | | ns | Figures 1 & 2 |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 0.6 | | 1.0 | | 1.6 | | ns | Figures 1 & 2 |

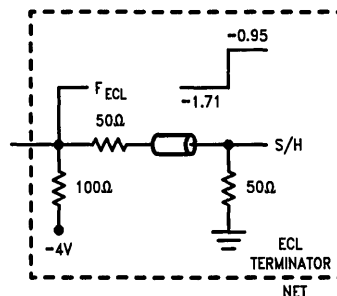
Ceramic Dual-In-Line Package ECL-to-TTL AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{TTL} = +4.5V$ to $+5.5V$, $V_{CC} = V_{CCA} = GND$, $C_L = 50$ pF

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = 25^\circ C$ | | $T_C = 85^\circ C$ | | Units | Conditions |
|-------------|---------------------------------|-------------------|------|--------------------|------|--------------------|------|-------|---------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} | E_n to T_n (Transparent) | 2.5 | 6.5 | 2.5 | 6.5 | 3.0 | 8.0 | ns | Figures 3 & 4 |
| t_{PHL} | E_n to T_n (Transparent) | 2.0 | 5.5 | 2.0 | 5.5 | 2.0 | 6.0 | ns | Figures 3 & 4 |
| t_{PLH} | LE to T_n | 3.0 | 7.5 | 3.0 | 7.5 | 3.5 | 9.5 | ns | Figures 3 & 4 |
| t_{PHL} | LE to T_n | 2.5 | 6.5 | 2.5 | 6.5 | 3.0 | 7.0 | ns | Figures 3 & 4 |
| t_{PZH} | OE to T_n | 3.0 | 7.5 | 3.0 | 7.5 | 3.5 | 8.5 | ns | Figures 3 & 5 |
| t_{PZL} | OE to T_n (Enable Time) | 4.0 | 9.5 | 4.0 | 9.5 | 4.5 | 10.0 | ns | Figures 3 & 5 |
| t_{PHZ} | OE to T_n | 3.0 | 9.5 | 3.0 | 9.5 | 3.5 | 11.0 | ns | Figures 3 & 5 |
| t_{PLZ} | OE to T_n (Disable Time) | 2.5 | 8.0 | 2.5 | 8.0 | 3.5 | 10.0 | ns | Figures 3 & 5 |
| t_{PHZ} | DIR to T_n | 2.5 | 10.0 | 2.5 | 10.0 | 3.0 | 10.0 | ns | Figures 3 & 6 |
| t_{PLZ} | DIR to T_n (Disable Time) | 2.5 | 8.5 | 2.5 | 8.5 | 3.5 | 10.0 | ns | Figures 3 & 6 |
| t_{set} | E_n to LE | 1.5 | | 1.5 | | 1.5 | | ns | Figures 3 & 4 |
| t_{hold} | E_n to LE | 3.5 | | 3.5 | | 3.5 | | ns | Figures 3 & 4 |
| $t_{pw(H)}$ | Pulse Width High, LE | 2.0 | | 2.0 | | 2.0 | | ns | Figures 3 & 4 |



TL/F/9851-6



TL/F/9851-12

FIGURE 1. TTL to ECL AC Test Circuit

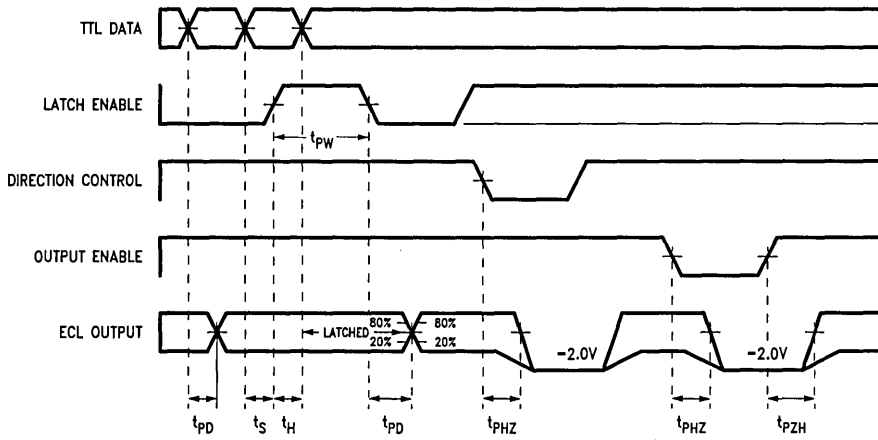
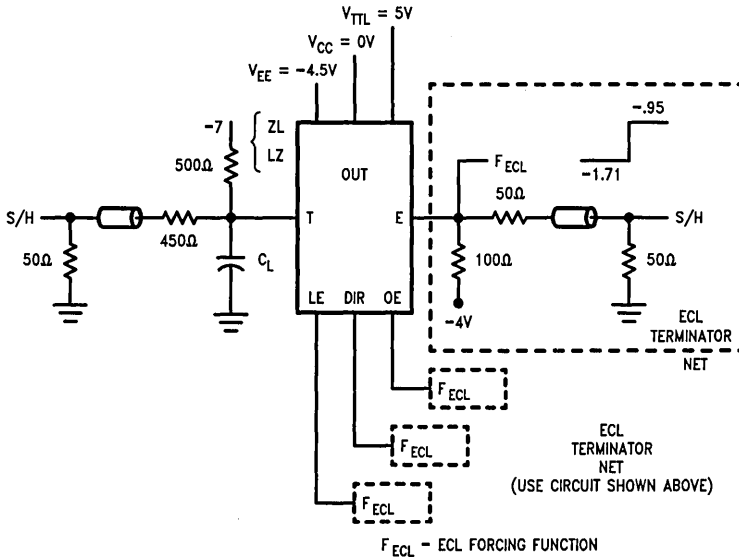


FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

TL/F/9851-7



ECL TERMINATOR NET (USE CIRCUIT SHOWN ABOVE)

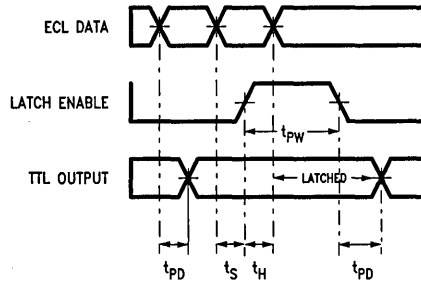
F_{ECL} - ECL FORCING FUNCTION

TL/F/9851-8

$C_L = 50$ pF including stray and jig capacitance.

Note: 50Ω to ground termination must be included on ECL I/O pins not monitored by a 50Ω scope to prevent oscillatory feedback.

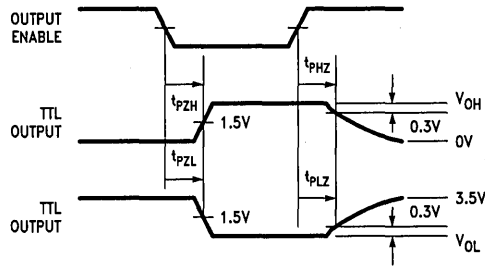
FIGURE 3. ECL-to-TTL AC Test Circuit



TL/F/9851-9

Note: DIR is LOW, OE is HIGH

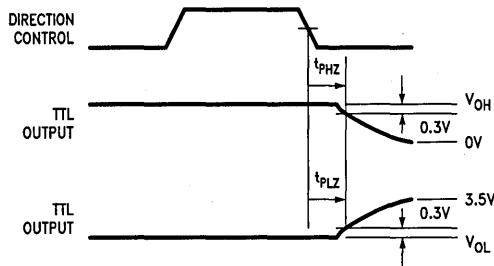
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times



TL/F/9851-13

Note: DIR is LOW, LE is HIGH

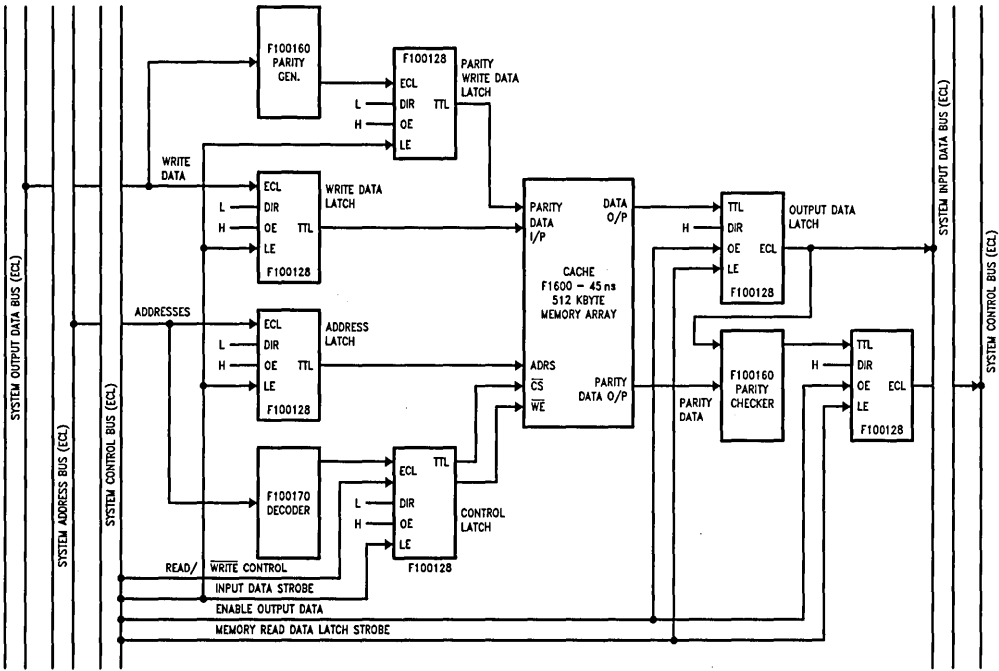
FIGURE 5. ECL-to-TTL Transition; OE to TTL Output, Enable and Disable Times



TL/F/9851-14

Note: OE and LE are HIGH

FIGURE 6. ECL-to-TTL Transition; DIR to TTL Output, Disable Time



TL/F/9851-10

FIGURE 5. Applications Diagram—MOS/TTL SRAM Interface Using F100128 ECL-TTL Latched Translator



F100130 Triple D Latch

General Description

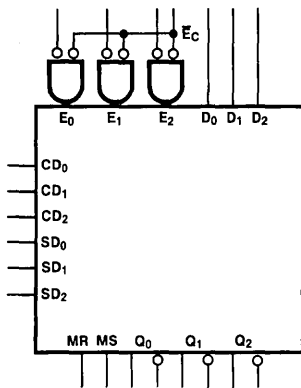
The F100130 contains three D-type latches with true and complement outputs and with Common Enable (\bar{E}_C), Master Set (MS) and Master Reset (MR) inputs. Each latch has its own Enable (\bar{E}_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. The Q output follows its Data (D) input when both \bar{E}_n and \bar{E}_C are LOW (transparent mode). When either \bar{E}_n or \bar{E}_C

(or both) are HIGH, a latch stores the last valid data present on its D_n input before \bar{E}_n or \bar{E}_C goes HIGH.

Both Master Reset (MR) and Master Set (MS) inputs override the Enable inputs. The individual CD_n and SD_n also override the Enable inputs. All inputs have 50 k Ω pull-down resistors.

Ordering Code: See Section 8

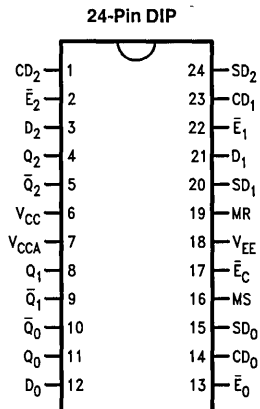
Logic Symbol



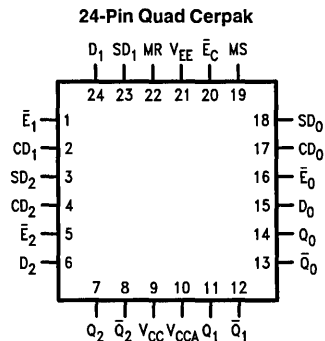
| Pin Names | Description |
|----------------------------------|---------------------------------------|
| CD ₀ -CD ₂ | Individual Direct Clear Inputs |
| SD ₀ -SD ₂ | Individual Direct Set Inputs |
| \bar{E}_0 - \bar{E}_2 | Individual Enable Inputs (Active LOW) |
| \bar{E}_C | Common Enable Input (Active LOW) |
| D ₀ -D ₂ | Data Inputs |
| MR | Master Reset Input |
| MS | Master Set Input |
| Q ₀ -Q ₂ | Data Outputs |
| \bar{Q}_0 - \bar{Q}_2 | Complementary Data Outputs |

TL/F/9852-3

Connection Diagrams

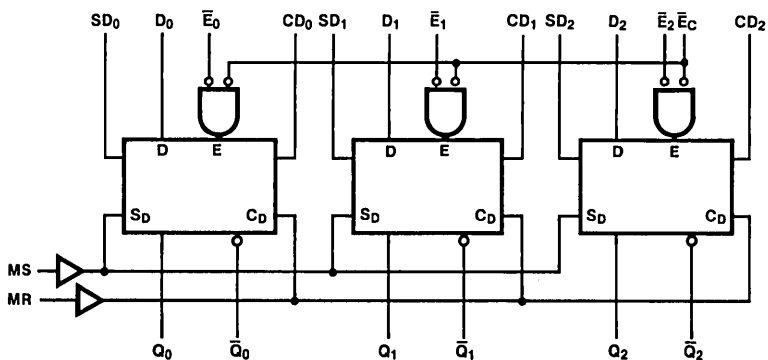


TL/F/9852-1



TL/F/9852-2

Logic Diagram



TL/F/9852-5

Truth Tables (Each Latch)

Latch Operation

| Inputs | | | | | Outputs |
|--------|-------------|-------------|--------------|--------------|----------|
| D_n | \bar{E}_n | \bar{E}_C | MS SD_n | MR CD_n | Q_n |
| L | L | L | L | L | L |
| H | L | L | L | L | H |
| X | H | X | L | L | Latched* |
| X | X | H | L | L | Latched* |

Asynchronous Operation

| Inputs | | | | | Outputs |
|--------|-------------|-------------|--------------|--------------|---------|
| D_n | \bar{E}_n | \bar{E}_C | MS SD_n | MR CD_n | Q_n |
| X | X | X | H | L | H |
| X | X | X | L | H | L |
| X | X | X | H | H | U |

*Retains data presented before \bar{E} positive transition

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

U = Undefined

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Maximum Junction Temperature (T_j) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{EE} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

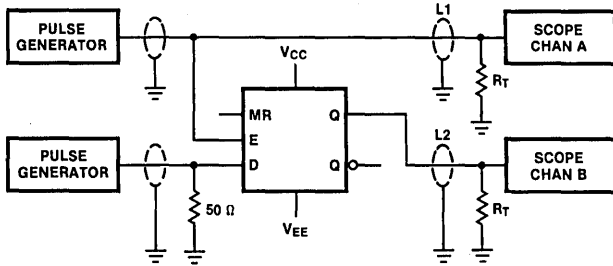
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------|------|------|-----|---------|-------------------------------|
| I_{IH} | Input HIGH Current | | | | | $V_{IN} = V_{IH}(\text{Max})$ |
| | D_n | | | 350 | μA | |
| | CD_n, SD_n | | | 530 | | |
| | \bar{E}_n | | | 240 | | |
| | \bar{E}_C, MR, MS | | | 450 | | |
| | | | | | | |
| I_{EE} | Power Supply Current | -149 | -106 | -74 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|---------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output (Transparent Mode) | 0.50 | 1.80 | 0.50 | 1.70 | 0.50 | 1.90 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_C to Output | 0.65 | 2.10 | 0.75 | 2.00 | 0.75 | 2.10 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay CD_n, SD_n, \bar{E}_n to Output | 0.50 | 2.00 | 0.60 | 1.75 | 0.60 | 2.00 | ns | <i>Figures 1, 2 and 3</i> |
| t_{PLH} t_{PHL} | Propagation Delay MS, MR to Output | 1.10 | 2.50 | 1.10 | 2.40 | 1.10 | 2.60 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | <i>Figures 1 and 2</i> |
| t_s | Setup Time D_0-D_2 | 0.90 | | 0.70 | | 0.90 | | ns | <i>Figures 3 and 4</i> |
| | CD_n, SD_n (Release Time) | 1.20 | | 1.10 | | 1.40 | | | |
| | MR, MS (Release Time) | 1.90 | | 1.90 | | 2.00 | | | |
| | | | | | | | | | |
| t_h | Hold Time D_0-D_2 | 0.60 | | 0.60 | | 0.80 | | ns | <i>Figure 4</i> |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E}_n, \bar{E}_C | 2.00 | | 2.00 | | 2.00 | | ns | <i>Figure 2</i> |
| $t_{pw(H)}$ | Pulse Width HIGH CD_n, SD_n, MR, MS | 2.00 | | 2.00 | | 2.00 | | ns | <i>Figure 3</i> |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|--------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output (Transparent Mode) | 0.50 | 1.60 | 0.50 | 1.50 | 0.50 | 1.70 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_C to Output | 0.65 | 1.90 | 0.75 | 1.80 | 0.75 | 1.90 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay CD_n, SD_n, \bar{E}_n to Output | 0.50 | 1.80 | 0.60 | 1.55 | 0.60 | 1.80 | ns | Figures 1, 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay MS, MR to Output | 1.10 | 2.30 | 1.10 | 2.20 | 1.10 | 2.40 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | Figures 1 and 2 |
| t_s | Setup Time D_0-D_2 | 0.80 | | 0.60 | | 0.80 | | ns | Figures 3 and 4 |
| | CD_n, SD_n (Release Time) | 1.10 | | 1.00 | | 1.30 | | | |
| | MR, MS (Release Time) | 1.80 | | 1.80 | | 2.00 | | | |
| t_h | Hold Time D_0-D_2 | 0.50 | | 0.50 | | 0.70 | | ns | Figure 4 |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E}_n, \bar{E}_C | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |
| $t_{pw(H)}$ | Pulse Width HIGH CD_n, SD_n, MR, MS | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |



Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2$ = equal length 50 Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50 Ω to GND
 $C_L =$ Fixture and stray capacitance ≤ 3 pF

TL/F/9852-6

FIGURE 1. AC Test Circuit

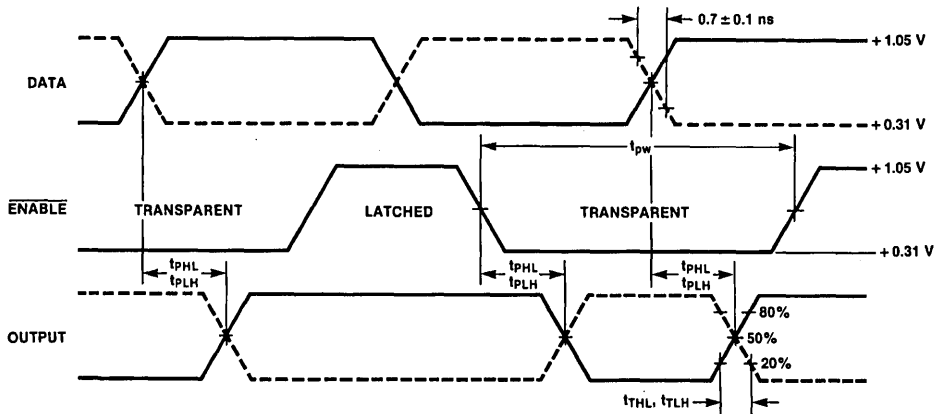
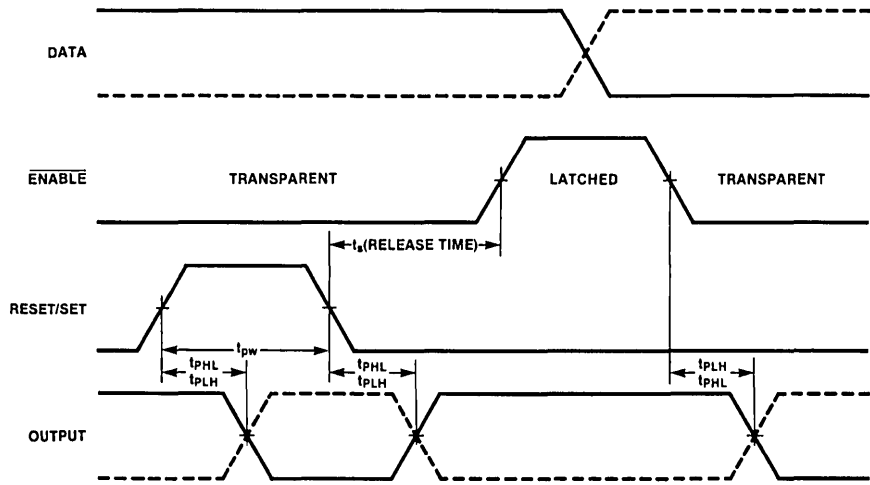


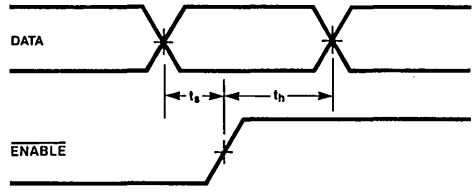
FIGURE 2. Enable Timing

TL/F/9852-7



TL/F/9852-8

FIGURE 3. Reset Timing



Notes:
 t_s is the minimum time before the transition of the enable that information must be present at the data input.
 t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

TL/F/9852-9

FIGURE 4. Data Setup and Hold Time



F100131 Triple D Flip-Flop

General Description

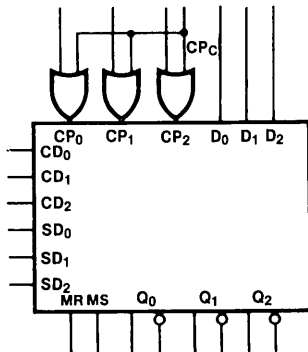
The F100131 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a Common Clock (CP_C), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual Clock (CP_n), Direct Set (SD_n) and Direct Clear (CD_n) inputs. Data enters a master when both CP_n and CP_C are LOW and transfers to a slave when CP_n or CP_C (or both) go HIGH. The Master Set,

Master Reset and individual CD_n and SD_n inputs override the Clock inputs. All inputs have 50 k Ω pull-down resistors. Refer to the F100331 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

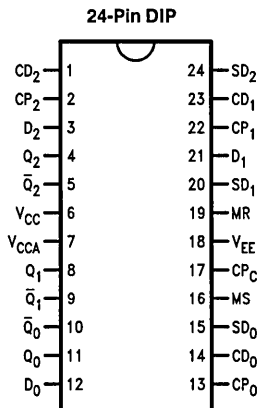
Logic Symbol



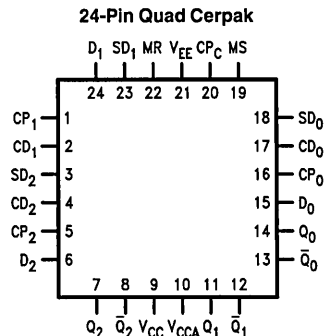
TL/F/9853-3

| Pin Names | Description |
|---------------------------|--------------------------------|
| CP_0 - CP_2 | Individual Clock Inputs |
| CP_C | Common Clock Input |
| D_0 - D_2 | Data Inputs |
| CD_0 - CD_2 | Individual Direct Clear Inputs |
| SD_n | Individual Direct Set Inputs |
| MR | Master Reset Input |
| MS | Master Set Input |
| Q_0 - Q_2 | Data Outputs |
| \bar{Q}_0 - \bar{Q}_2 | Complementary Data Outputs |

Connection Diagrams

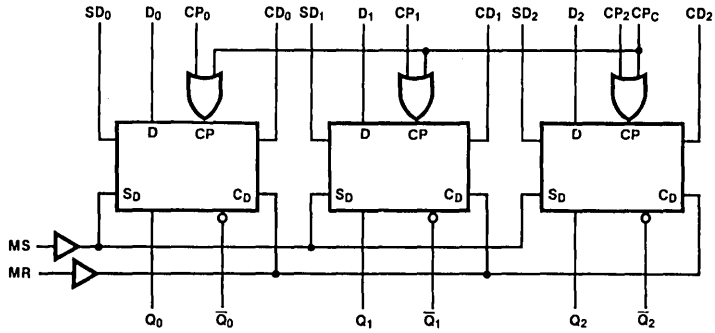


TL/F/9853-1



TL/F/9853-2

Logic Diagram



TL/F/9853-5

Truth Tables (Each Flip-Flop)

Synchronous Operation

| Inputs | | | | | Outputs |
|----------------|-----------------|-----------------|-----------------------|-----------------------|----------------------|
| D _n | CP _n | CP _C | MS SD _n | MR CD _n | Q _n (t+1) |
| L | ↗ | L | L | L | L |
| H | ↗ | L | L | L | H |
| L | L | ↗ | L | L | L |
| H | L | ↗ | L | L | H |
| X | L | L | L | L | Q _n (t) |
| X | H | X | L | L | Q _n (t) |
| X | X | H | L | L | Q _n (t) |

Asynchronous Operation

| Inputs | | | | | Outputs |
|----------------|-----------------|-----------------|-----------------------|-----------------------|----------------------|
| D _n | CP _n | CP _C | MS SD _n | MR CD _n | Q _n (t+1) |
| X | X | X | H | L | H |
| X | X | X | L | H | L |
| X | X | X | H | H | U |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 U = Undefined
 t = Time before CP Positive Transition
 t+1 = Time after CP Positive Transition
 ↗ = LOW to HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
Maximum Junction Temperature (T_j) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
Input Voltage (DC) V_{EE} to $+0.5\text{V}$
Output Current (DC Output HIGH) -50mA
Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|---------|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|-------------------|---------|-------------------------|
| I_{IH} | Input HIGH Current CP_n, D_n MS, MR, CP_C CD_n, SD_n | | | 240 450 530 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -149 | -106 | -74 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions | |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{max} | Toggle Frequency | 325 | | 325 | | 325 | | MHz | Figures 2 and 3 | |
| t_{PLH} t_{PHL} | Propagation Delay CP_C to Output | 0.75 | 2.40 | 0.75 | 2.15 | 0.70 | 2.30 | ns | Figures 1 and 3 | |
| t_{PLH} t_{PHL} | Propagation Delay CP_n to Output | 0.70 | 2.20 | 0.70 | 2.00 | 0.70 | 2.20 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay CD_n, SD_n to Output | 0.70 | 1.90 | 0.70 | 1.70 | 0.70 | 1.80 | ns | $CP_n, CP_C = L$ | Figures 1 and 4 |
| t_{PLH} t_{PHL} | | 0.70 | 2.10 | 0.70 | 2.00 | 0.70 | 2.20 | | $CP_n, CP_C = H$ | |
| t_{PLH} t_{PHL} | Propagation Delay MS, MR to Output | 1.10 | 2.70 | 1.10 | 2.60 | 1.10 | 2.70 | ns | $CP_n, CP_C = L$ | |
| t_{PLH} t_{PHL} | | 1.05 | 3.05 | 1.05 | 2.95 | 1.05 | 3.05 | | $CP_n, CP_C = H$ | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.20 | 0.45 | 1.80 | 0.45 | 1.90 | ns | Figures 1, 3 and 4 | |
| t_s | Setup Time D_n | 0.90 | | 0.70 | | 0.90 | | ns | Figure 5 | |
| | CD_n, SD_n (Release Time) | 1.50 | | 1.30 | | 1.50 | | | Figure 4 | |
| | MS, MR (Release Time) | 2.50 | | 2.30 | | 2.50 | | | | |
| t_h | Hold Time D_n | 0.60 | | 0.60 | | 0.80 | | ns | Figure 5 | |
| $t_{pw}(H)$ | Pulse Width HIGH $CP_n, CP_C, CD_n,$ SD_n, MR, MS | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 | |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions | |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|---------------------------------------|--------------------|
| | | Min | Max | Min | Max | Min | Max | | | |
| f_{max} | Toggle Frequency | 350 | | 350 | | 350 | | MHz | Figures 2 and 3 | |
| t_{PLH} t_{PHL} | Propagation Delay CP _C to Output | 0.75 | 2.20 | 0.75 | 1.95 | 0.70 | 2.10 | ns | Figures 1 and 3 | |
| t_{PLH} t_{PHL} | Propagation Delay CP _n to Output | 0.70 | 2.00 | 0.70 | 1.80 | 0.70 | 2.00 | ns | | |
| t_{PLH} t_{PHL} | Propagation Delay CD _n , SD _n to Output | 0.70 | 1.70 | 0.70 | 1.50 | 0.70 | 1.60 | ns | CP _n , CP _C = L | Figures 1 and 4 |
| t_{PLH} t_{PHL} | | 0.70 | 1.90 | 0.70 | 1.80 | 0.70 | 2.00 | | CP _n , CP _C = H | |
| t_{PLH} t_{PHL} | Propagation Delay MS, MR to Output | 1.10 | 2.50 | 1.10 | 2.40 | 1.10 | 2.50 | ns | CP _n , CP _C = L | |
| t_{PLH} t_{PHL} | | 1.05 | 2.85 | 1.05 | 2.75 | 1.05 | 2.85 | | CP _n , CP _C = H | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.00 | 0.45 | 1.60 | 0.45 | 1.70 | ns | Figures 1, 3 and 4 | |
| t_s | Setup Time | | | | | | | ns | Figure 5 | |
| | D _n | 0.80 | | 0.60 | | 0.80 | | | | |
| | CD _n , SD _n (Release Time) MS, MR (Release Time) | 1.40 2.40 | | 1.20 2.20 | | 1.40 2.40 | | | Figure 4 | |
| t_h | Hold Time D _n | 0.50 | | 0.50 | | 0.70 | | ns | Figure 5 | |
| $t_{pw}(H)$ | Pulse Width HIGH CP _n , CP _C , CD _n , SD _n , MR, MS | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 and 4 | |

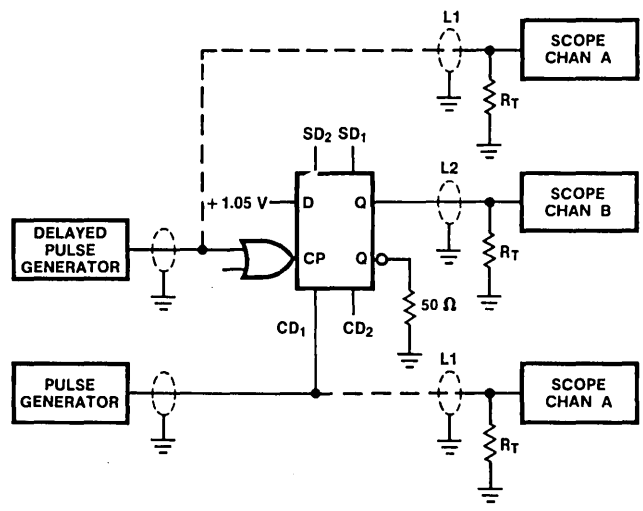


FIGURE 1. AC Test Circuit

TL/F/9853-6

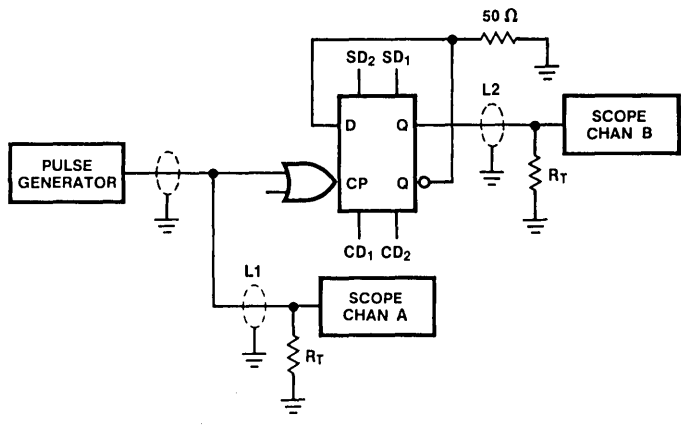


FIGURE 2. Toggle Frequency Test Circuit

TL/F/9853-7

Note:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 L1 and L2 = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance ≤ 3 pF

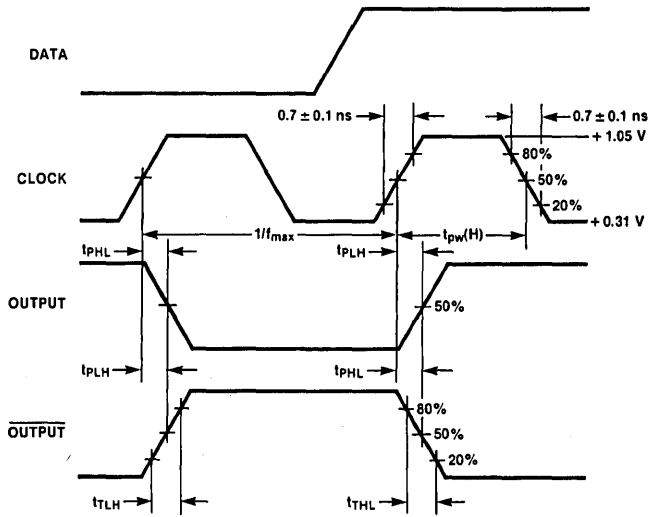


FIGURE 3. Propagation Delay (Clock) and Transition Times

TL/F/9853-8

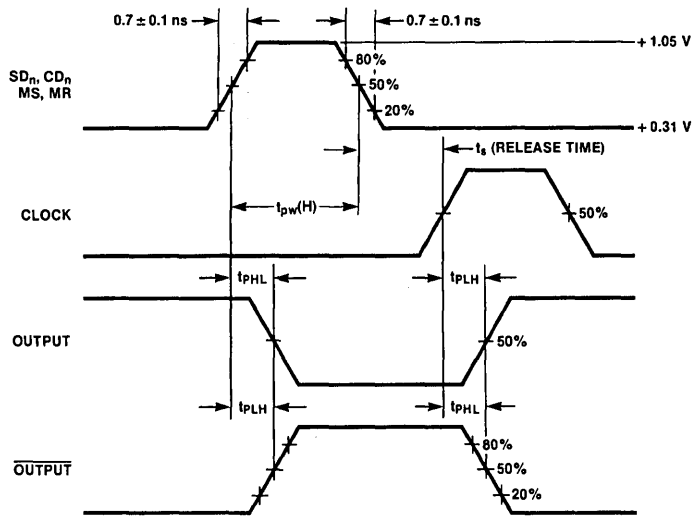
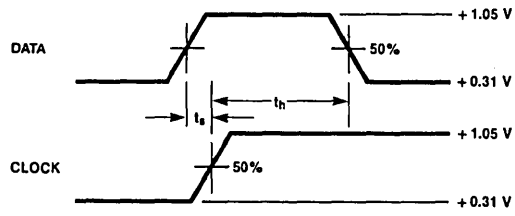


FIGURE 4. Propagation Delay (Resets)

TL/F/9853-9



TL/F/9853-10

FIGURE 5. Data Setup and Hold Time**Note:**

t_s is the minimum time before the transition of the clock that information must be present at the data input.
 t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.



F100135 Triple J-K Flip-Flop

General Description

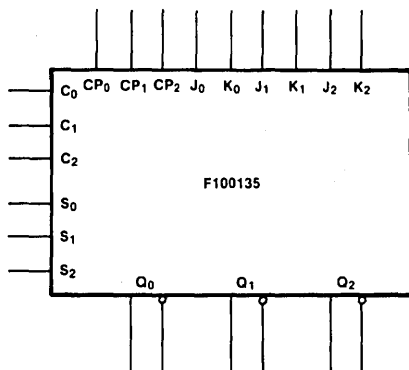
The F100135 contains three J-K, edge-triggered master-slave flip-flops with true and complement outputs. All have individual Clock (CP_n), Clear (C_n), and Set (S_n) inputs. Clocking occurs on the rising edge of CP_n . All inputs have 50 k Ω pull-down resistors.

Features

- Toggle frequency 750 MHz Typical
- Propagation delay 2.2 ns max
- Outputs specified to drive a 50 Ω load

Ordering Code: See Section 8

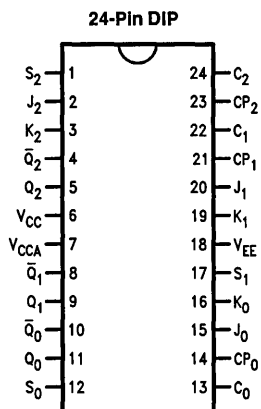
Logic Symbol



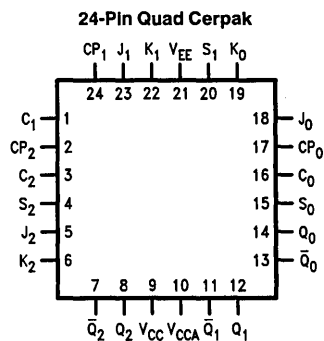
TL/F/9854-3

| Pin Names | Description |
|---------------------------|----------------------------|
| J_0 - J_2 | J Inputs |
| K_0 - K_2 | K Inputs |
| S_0 - S_2 | Direct Set Inputs |
| C_0 - C_2 | Direct Clear Inputs |
| CP_0 - CP_2 | Clock Inputs |
| Q_0 - Q_2 | Data Outputs |
| \bar{Q}_0 - \bar{Q}_2 | Complementary Data Outputs |

Connection Diagrams

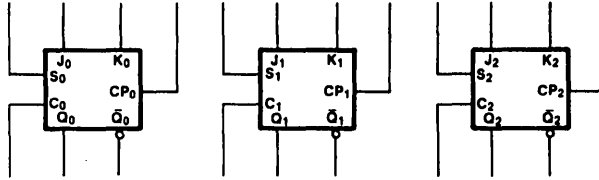


TL/F/9854-1



TL/F/9854-2

Logic Diagram



TL/F/9854-5

Truth Tables (Each Flip-Flop)

Synchronous Operation

| Inputs | | | | | Outputs |
|--------|-------|--------|-------|-------|---------------------|
| J_n | K_n | CP_n | S_n | C_n | $Q_n(t + 1)$ |
| L | L | ↗ | L | L | $Q_n(t)$ |
| L | H | ↗ | L | L | L |
| H | L | ↗ | L | L | H |
| H | H | ↗ | L | L | $\overline{Q_n(t)}$ |
| X | X | H | L | L | $Q_n(t)$ |
| X | X | L | L | L | $Q_n(t)$ |

Asynchronous Operation

| Inputs | | | | | Outputs |
|--------|-------|--------|-------|-------|---------|
| J_n | K_n | CP_n | S_n | C_n | Q_n |
| X | X | X | H | L | H |
| X | X | X | L | H | L |
| X | X | X | H | H | U |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

U = Undefined

t = Time before CP Positive Transition

t + 1 = Time after CP Positive Transition

↗ = LOW-to-HIGH Transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
Maximum Junction Temperature (T_j) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
Input Voltage (DC) V_{EE} to $+0.5\text{V}$
Output Current (DC Output HIGH) -50 mA
Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V , V_{CC} = V_{CCA} = GND, T_C = 0°C to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|---------|---------|---------|-------|---|---------------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.2V , V_{CC} = V_{CCA} = GND, T_C = 0°C to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|---------|-----|---------|-------|---|---------------------------------------|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V _{OH} C | Output HIGH Voltage | -1030 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1595 | | | |
| V _{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.8V , V_{CC} = V_{CCA} = GND, T_C = 0°C to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|---------|-----|---------|-------|---|---------------------------------------|
| V _{OH} | Output HIGH Voltage | -1035 | | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1045 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

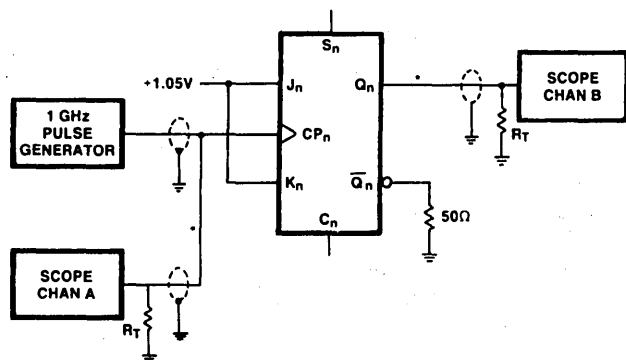
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------------------|------|------|-----|---------|-------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 350 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -195 | -150 | -90 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|----------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{max} | Toggle Frequency | 600 | | 600 | | 600 | | MHz | Figure 1 |
| t_{PLH} t_{PHL} | Propagation Delay CP_n to Output | 0.70 | 2.20 | 0.70 | 2.00 | 0.70 | 2.20 | ns | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay C_n, S_n to Output | 0.90 | 1.80 | 0.90 | 2.00 | 0.90 | 2.40 | ns | $CP_n = L, CP_n = H$ |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.40 | 0.30 | 1.40 | 0.30 | 1.40 | ns | Figures 2 and 3 |
| t_s | Setup Time J_n, K_n to CP_n C_n, S_n (Release Time) | 0.90 1.50 | | 0.70 1.30 | | 0.90 1.50 | | ns | |
| t_H | Hold Time J_n, K_n to CP_n | 0.80 | | 0.80 | | 0.80 | | ns | |
| $t_{pw(H)}$ | Pulse Width HIGH CP_n, C_n, S_n | 2.00 | | 2.00 | | 2.00 | | ns | |

Cerpak AC Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|----------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{max} | Toggle Frequency | 650 | | 650 | | 650 | | MHz | Figure 1 |
| t_{PLH} t_{PHL} | Propagation Delay CP_n to Output | 0.70 | 2.00 | 0.70 | 1.80 | 0.70 | 2.00 | ns | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay C_n, S_n to Output | 0.90 | 1.60 | 0.90 | 1.80 | 0.90 | 2.20 | ns | $CP_n = L, CP_n = H$ |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.30 | 1.30 | 0.30 | 1.30 | 0.30 | 1.30 | ns | Figures 2 and 3 |
| t_s | Setup Time J_n, K_n to CP_n C_n, S_n (Release Time) | 0.80 1.40 | | 0.60 1.20 | | 0.80 1.40 | | ns | |
| t_H | Hold Time J_n, K_n to CP_n | 0.70 | | 0.70 | | 0.70 | | ns | |
| $t_{pw(H)}$ | Pulse Width HIGH CP_n, C_n, S_n | 2.00 | | 2.00 | | 2.00 | | ns | |

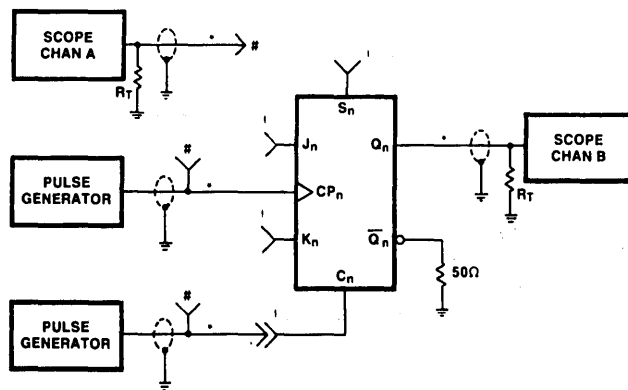


TL/F/9854-6

FIGURE 1. Toggle Frequency Test Circuit

Notes:

- $V_{CC} = V_{CCA} = +2V$
- $V_{EE} = -2.5V$
- * = equal electrical length 50Ω lines
- $R_T = 50\Omega$ termination
- Decouple power supplies with 0.1 μF from V_{CC} and V_{EE} to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Load all unused outputs with 50Ω to GND
- Set pulse generator output level for 740 mV p-p at a frequency of 10 MHz as measured at the clock input pin of the device under test. Do not readjust this voltage for frequencies up to f_{max} . The pad isolates the generator output for D.U.T. input impedance variations. Signal voltage measured at the D.U.T. input will vary as input impedance varies with frequency.



TL/F/9854-7

FIGURE 2. AC Test Circuit

Notes:

- $V_{CC} = V_{CCA} = +2V$
- $V_{EE} = -2.5V$
- Decouple power supplies with 0.1 μF from V_{CC} and V_{EE} to GND
- $R_T = 50\Omega$ termination
- Load all unused outputs with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- * = equal electrical length 50Ω lines
- # = Connect Scope CHAN A to pulse generator as required
- † = Connect pulse generator to input under test; else connect input to voltage source set to +1.05 volts for logic HIGH or +0.31 volts for logic LOW
- Consult truth table for appropriate logical condition

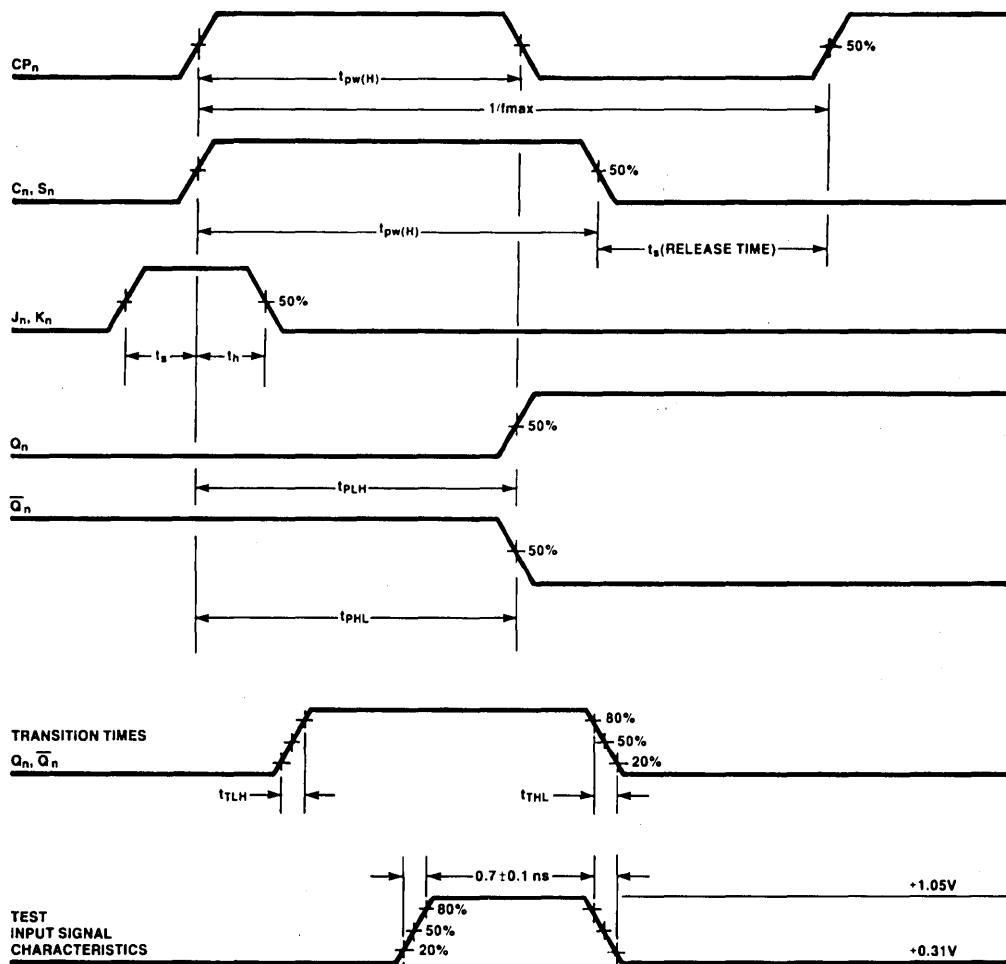


FIGURE 3. Propagation Delays and Setup and Hold Time

TL/F/9854-8



F100136 4-Stage Counter/Shift Register

General Description

The F100136 operates as either a modulo-16 up/down counter or as a 4-bit bidirectional shift register. Three Select (S_n) inputs determine the mode of operation, as shown in the Function Select table. Two Count Enable (\overline{CEP} , \overline{CET}) inputs are provided for ease of cascading in multistage counters. One Count Enable (\overline{CET}) input also doubles as a Serial Data (D_0) input for shift-up operation. For shift-down operation, D_3 is the Serial Data input. In counting operations the Terminal Count (\overline{TC}) output goes LOW when the counter reaches 15 in the count/up mode or 0 (zero) in the count/down mode. In the shift modes, the \overline{TC} output repeats the Q_3 output. The dual nature of this \overline{TC}/Q_3 output and the D_0/\overline{CET} input means that one interconnection from one stage to the next higher stage serves as the link for

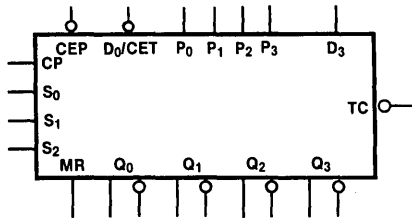
multistage counting or shift-up operation. The individual Preset (P_n) inputs are used to enter data in parallel or to preset the counter in programmable counter applications. A HIGH signal on the Master Reset (MR) input overrides all other inputs and asynchronously clears the flip-flops. In addition, a synchronous clear is provided, as well as a complement function which synchronously inverts the contents of the flip-flops. All inputs have 50 k Ω pull-down resistors.

Refer to the F100336 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

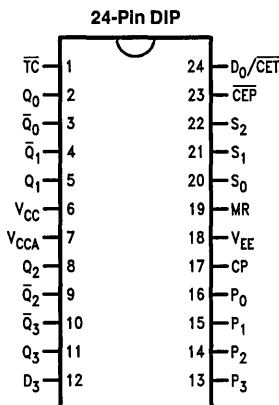
Logic Symbol



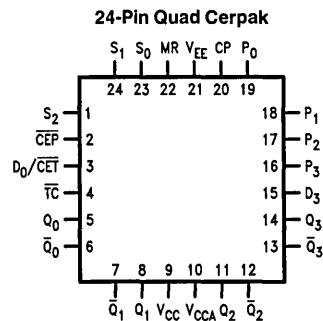
TL/F/9855-3

| Pin Names | Description |
|----------------------|--|
| CP | Clock Pulse Input |
| \overline{CEP} | Count Enable Parallel Input (Active LOW) |
| D_0/\overline{CET} | Serial Data Input/Count Enable |
| | Trickle Input (Active LOW) |
| S_0-S_2 | Select Inputs |
| MR | Master Reset Input |
| P_0-P_3 | Preset Inputs |
| D_3 | Serial Data Input |
| \overline{TC} | Terminal Count Output |
| Q_0-Q_3 | Data Outputs |
| $\overline{Q_0-Q_3}$ | Complementary Data Outputs |

Connection Diagrams

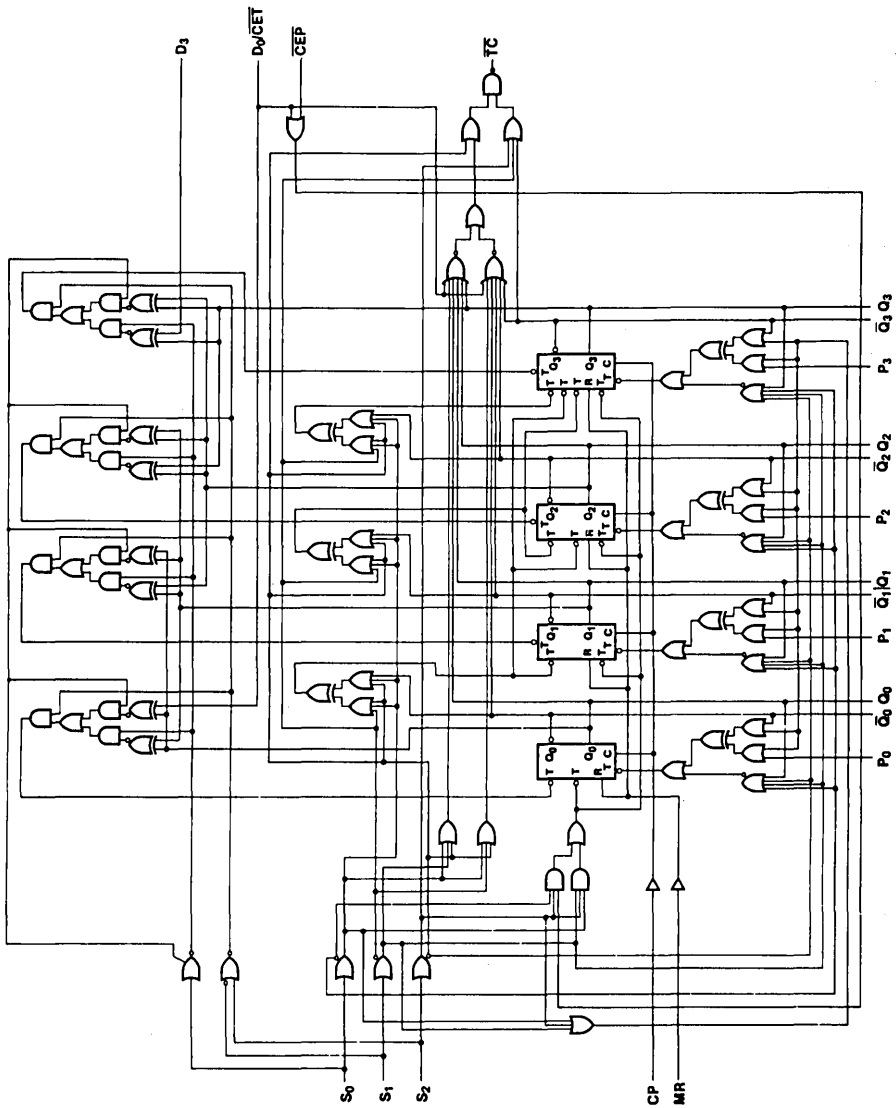


TL/F/9855-1



TL/F/9855-2

Logic Diagram



TL/F/9855-5

Function Select Table

| S ₂ | S ₁ | S ₀ | Function |
|----------------|----------------|----------------|---------------|
| L | L | L | Parallel Load |
| L | L | H | Complement |
| L | H | L | Shift Left |
| L | H | H | Shift Right |
| H | L | L | Count Down |
| H | L | H | Clear |
| H | H | L | Count Up |
| H | H | H | Hold |

Truth Table

Q₀ = LSB

| Inputs | | | | | | | | Outputs | | | | | | |
|--------|----------------|----------------|----------------|-------------------------|--|----------------|------------|-----------------------------|-------------------------|-------------------------|-------------------------|------------------------|--|--|
| MR | S ₂ | S ₁ | S ₀ | $\overline{\text{CEP}}$ | D ₀ / $\overline{\text{CET}}$ | D ₃ | CP | Q ₃ | Q ₂ | Q ₁ | Q ₀ | $\overline{\text{TC}}$ | Mode | |
| L | L | L | L | X | X | X | \nearrow | P ₃ | P ₂ | P ₁ | P ₀ | L | Preset (Parallel Load) | |
| L | L | L | H | X | X | X | \nearrow | $\overline{\text{Q}}_3$ | $\overline{\text{Q}}_2$ | $\overline{\text{Q}}_1$ | $\overline{\text{Q}}_0$ | L | Invert | |
| L | L | H | L | X | X | X | \nearrow | D ₃ | Q ₃ | Q ₂ | D ₁ | D ₃ | Shift Left | |
| L | L | H | H | X | X | X | \nearrow | Q ₂ | Q ₁ | Q ₀ | D ₀ | Q ₃ * | Shift Right | |
| L | H | L | L | L | L | X | \nearrow | (Q ₀₋₃) minus 1 | | | | ⊖ | Count Down | |
| L | H | L | L | H | L | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | ⊖ | Count Down with $\overline{\text{CEP}}$ not active | |
| L | H | L | L | X | H | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Count Down with $\overline{\text{CET}}$ not active | |
| L | H | L | H | X | X | X | \nearrow | L | L | L | L | H | Clear | |
| L | H | H | L | L | L | X | \nearrow | (Q ₀₋₃) plus 1 | | | | ⊕ | Count Up | |
| L | H | H | L | H | L | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | ⊕ | Count Up with $\overline{\text{CEP}}$ not active | |
| L | H | H | L | X | H | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Count Up with $\overline{\text{CET}}$ not active | |
| L | H | H | H | X | X | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Hold | |
| H | L | L | L | X | X | X | X | L | L | L | L | L | Asynchronous Master Reset | |
| H | L | L | H | X | X | X | X | L | L | L | L | L | | |
| H | L | H | L | X | X | X | X | L | L | L | L | L | | |
| H | L | H | H | X | X | X | X | L | L | L | L | L | | |
| H | H | L | L | X | H | X | X | L | L | L | L | H | | |
| H | H | L | H | X | X | X | X | L | L | L | L | H | | |
| H | H | H | L | X | X | X | X | L | L | L | L | H | | |
| H | H | H | H | X | X | X | X | L | L | L | L | H | | |

- ⊖ = L if Q₀-Q₃ = LLLL
 H if Q₀-Q₃ ≠ LLLL
- ⊕ = L if Q₀-Q₃ = HHHH
 H if Q₀-Q₃ ≠ HHHH
- H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 \nearrow = LOW-to-HIGH Transition

*Before the clock, $\overline{\text{TC}}$ is Q₃
 After the clock, $\overline{\text{TC}}$ is Q₂

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C
 Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C) 0°C to +85°C
 V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V
 Input Voltage (DC) V_{EE} to +0.5V
 Output Current (DC Output HIGH) -50 mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-------|-------|-------|--|---------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V _{OHC} | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-----|-------|-------|--|---------------------------|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V _{OHC} | Output HIGH Voltage | -1030 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1595 | | | |
| V _{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-----|-------|-------|--|---------------------------|
| V _{OH} | Output HIGH Voltage | -1035 | | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V _{OHC} | Output HIGH Voltage | -1045 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

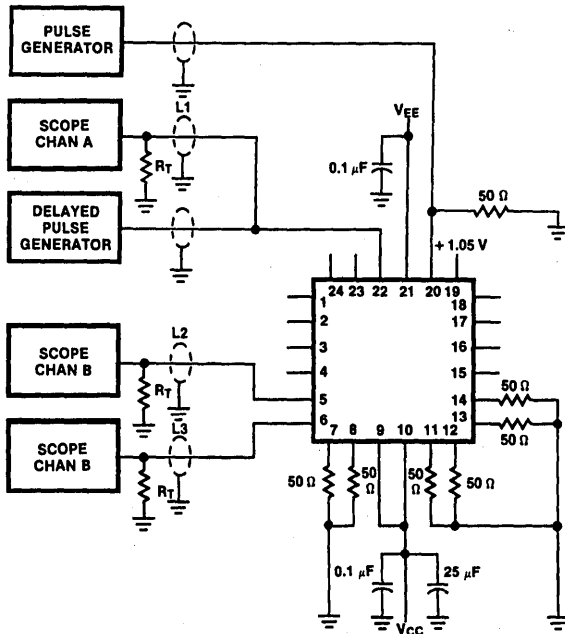
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------------------|----------------------|------|------|------|---------|-------------------------|
| I_{IH} | Input HIGH Current | | | | | $V_{IN} = V_{IH} (Max)$ |
| | P_n, S_n | | | 180 | μA | |
| | \overline{CEP} | | | 200 | | |
| | MR | | | 240 | | |
| | D_3 | | | 280 | | |
| | CP | | | 390 | | |
| D_0/\overline{CET} | | | 530 | | | |
| I_{EE} | Power Supply Current | -283 | -195 | -136 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{shift} | Shift Frequency | 250 | | 250 | | 250 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Q_n, \overline{Q}_n | 0.85 | 2.10 | 0.85 | 2.10 | 0.85 | 2.25 | ns | Figures 1 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to \overline{TC} | 1.90 | 4.80 | 1.90 | 4.60 | 1.90 | 5.20 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Q_n, \overline{Q}_n | 1.20 | 2.95 | 1.35 | 2.95 | 1.20 | 3.10 | ns | Figures 1 and 4 |
| t_{PLH} t_{PHL} | Propagation Delay MR to \overline{TC} | 2.20 | 4.80 | 2.20 | 4.80 | 2.20 | 5.30 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay D_0/\overline{CET} to \overline{TC} | 1.40 | 3.20 | 1.40 | 3.20 | 1.40 | 3.50 | ns | Figures 1 and 5 |
| t_{PLH} t_{PHL} | Propagation Delay S_n to \overline{TC} | 0.90 | 3.80 | 1.00 | 3.80 | 1.00 | 4.30 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | Figures 1 and 3 |
| t_s | Setup Time | | | | | | | ns | Figure 6 |
| | D_3 | 1.20 | | 1.20 | | 1.20 | | | |
| | P_n | 1.70 | | 1.70 | | 1.70 | | | |
| | $D_0/\overline{CET}, \overline{CEP}$ | 1.45 | | 1.45 | | 1.45 | | | |
| | S_n | 3.30 | | 3.30 | | 3.30 | | | |
| | MR (Release Time) | 2.60 | | 2.60 | | 2.60 | | | |
| t_h | Hold Time | | | | | | | ns | Figure 6 |
| | D_3 | 0.20 | | 0.20 | | 0.20 | | | |
| | P_n | 0.10 | | 0.10 | | 0.10 | | | |
| | $D_0/\overline{CET}, \overline{CEP}$ | 0.20 | | 0.20 | | 0.20 | | | |
| | S_n | -0.90 | | -0.90 | | -0.90 | | | |
| $t_{pw(H)}$ | Pulse Width HIGH CP, MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{shift} | Shift Frequency | 250 | | 250 | | 250 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Q_n, \overline{Q}_n | 0.85 | 1.90 | 0.85 | 1.90 | 0.85 | 2.05 | ns | Figures 1 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to \overline{TC} | 1.90 | 4.60 | 1.90 | 4.40 | 1.90 | 5.00 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Q_n, \overline{Q}_n | 1.20 | 2.75 | 1.35 | 2.75 | 1.20 | 2.90 | ns | Figures 1 and 4 |
| t_{PLH} t_{PHL} | Propagation Delay MR to \overline{TC} | 2.20 | 4.60 | 2.20 | 4.60 | 2.20 | 5.10 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay D_0/\overline{CET} to \overline{TC} | 1.40 | 3.00 | 1.40 | 3.00 | 1.40 | 3.30 | ns | Figures 1 and 5 |
| t_{PLH} t_{PHL} | Propagation Delay S_n to \overline{TC} | 0.90 | 3.60 | 1.00 | 3.60 | 1.00 | 4.10 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | Figures 1 and 3 |
| t_s | Setup Time | | | | | | | ns | Figure 6 |
| | D_3 | 1.10 | | 1.10 | | 1.10 | | | |
| | P_n | 1.60 | | 1.60 | | 1.60 | | | |
| | $D_0/\overline{CET}, \overline{CEP}$ | 1.35 | | 1.35 | | 1.35 | | | |
| | S_n | 3.20 | | 3.20 | | 3.20 | | | |
| | MR (Release Time) | 2.50 | | 2.50 | | 2.50 | | | |
| t_h | Hold Time | | | | | | | ns | Figure 6 |
| | D_3 | 0.10 | | 0.10 | | 0.10 | | | |
| | P_n | 0 | | 0 | | 0 | | | |
| | $D_0/\overline{CET}, \overline{CEP}$ | 0.10 | | 0.10 | | 0.10 | | | |
| | S_n | -1.00 | | -1.00 | | -1.00 | | | |
| $t_{pw(H)}$ | Pulse Width HIGH CP, MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 |



Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1, L2 \text{ and } L3 = \text{equal length } 50\Omega \text{ impedance lines}$
 $R_T = 50\Omega \text{ terminator internal to scope}$
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L = \text{Fixture and stray capacitance } \leq 3 \text{ pF}$
 Pin numbers shown are for flatpak;
 for DIP see logic symbol

FIGURE 1. AC Test Circuit

TL/F/9855-6

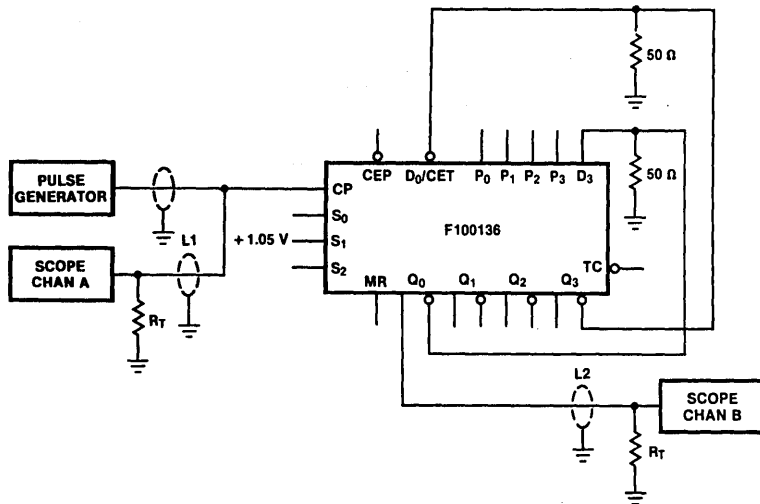
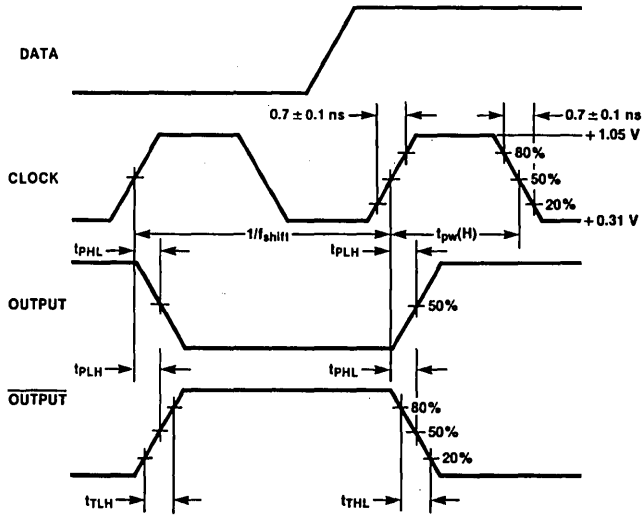


FIGURE 2. Shift Frequency Test Circuit (Shift Left)

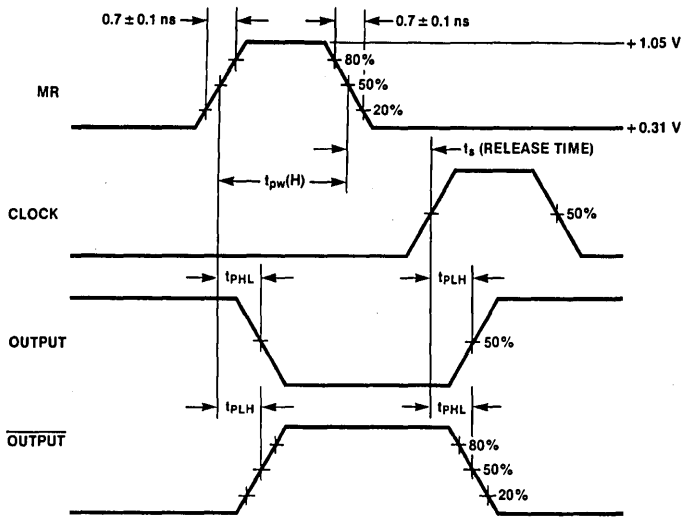
TL/F/9855-7

Notes:
 For shift right mode, $+1.05V$ is applied at S_0 .
 The feedback path from output to input should be as short as possible.



TL/F/9855-8

FIGURE 3. Propagation Delay (Clock) and Transition Times



TL/F/9855-9

FIGURE 4. Propagation Delay (Reset)

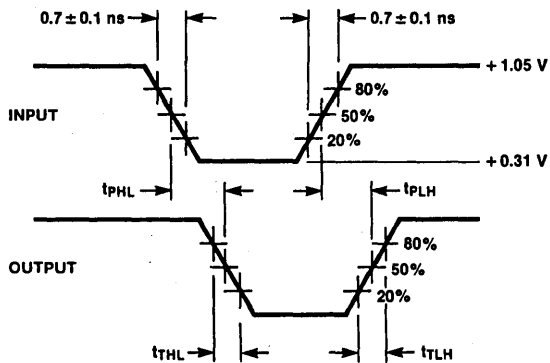
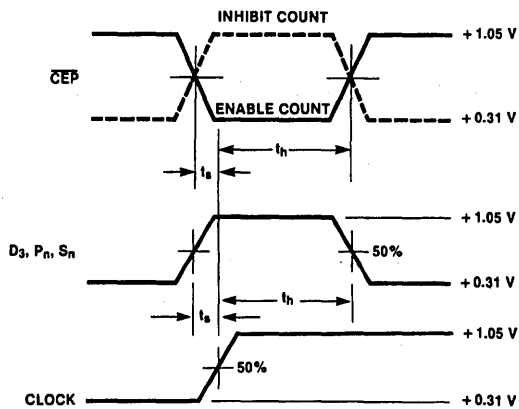


FIGURE 5. Propagation Delay (Serial Data, Selects)

TL/F/9855-10



TL/F/9855-11

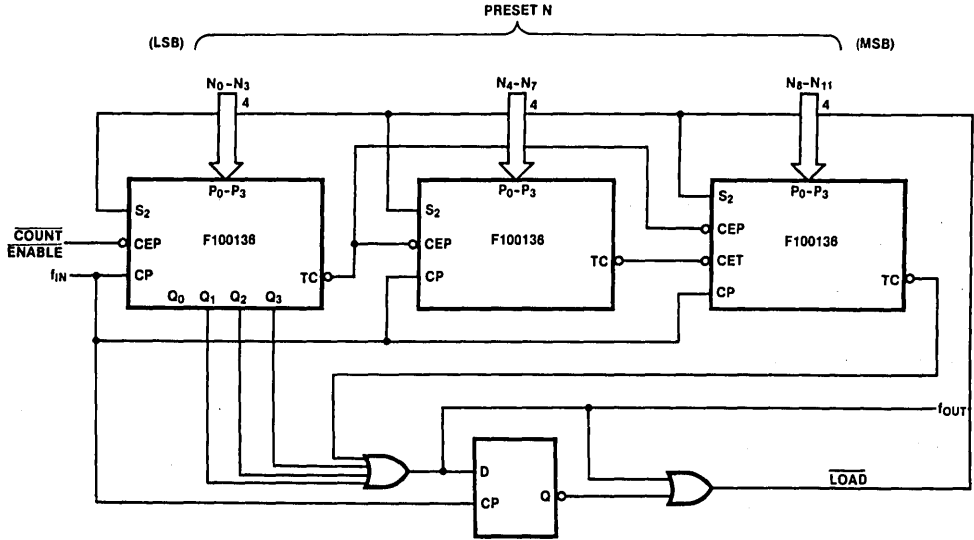
Notes:

- t_s is the minimum time before the transition of the clock that information must be present at the data input.
- t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 6. Setup and Hold Time

Applications

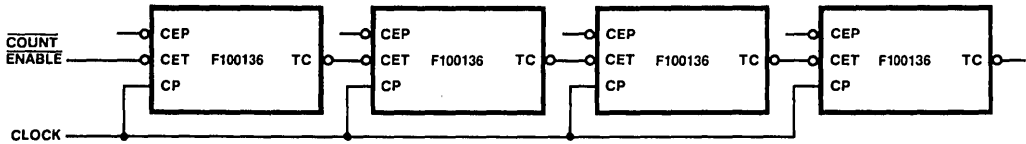
3-Stage Divider, Preset Count Down Mode



Note: If $S_0 = S_1 = S_2 = \text{LOW}$, then $T_C = \text{LOW}$

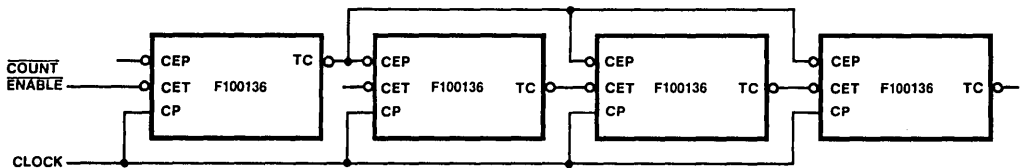
TL/F/9855-12

Slow Expansion Scheme



TL/F/9855-13

Fast Expansion Scheme



TL/F/9855-15



F100141

8-Bit Shift Register

General Description

The F100141 contains eight edge-triggered, D-type flip-flops with individual inputs (P_n) and outputs (Q_n) for parallel operation, and with serial inputs (D_n) and steering logic for bidirectional shifting. The flip-flops accept input data a setup time before the positive-going transition of the clock pulse and their outputs respond a propagation delay after this rising clock edge.

The circuit operating mode is determined by the Select inputs S_0 and S_1 , which are internally decoded to select either

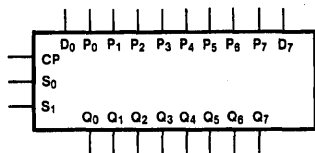
"parallel entry", "hold", "shift left" or "shift right" as described in the Truth Table. All inputs have 50 k Ω pull-down resistors.

Refer to the F100341 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

Logic Symbol

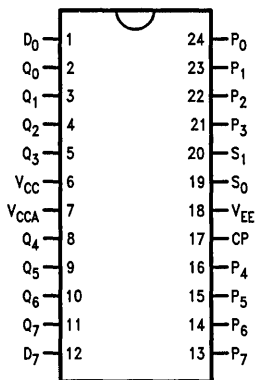


TL/F/9856-1

| Pin Names | Description |
|------------|-----------------|
| CP | Clock Input |
| S_0, S_1 | Select Inputs |
| D_0, D_7 | Serial Inputs |
| P_0-P_7 | Parallel Inputs |
| Q_0-Q_7 | Data Outputs |

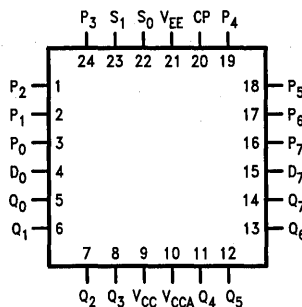
Connection Diagrams

24-Pin DIP



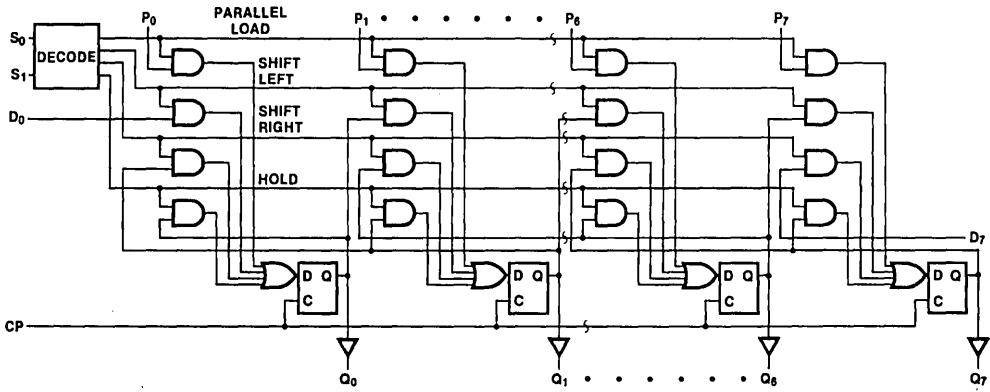
TL/F/9856-2

24-Pin Quad Cerpak



TL/F/9856-3

Logic Diagram



TL/F/9856-5

Truth Table

| Function | Inputs | | | | | Outputs | | | | | | | |
|---------------|----------------|----------------|----------------|----------------|----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| | D ₇ | D ₀ | S ₁ | S ₀ | CP | Q ₇ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ | Q ₀ |
| Load Register | X | X | L | L | ↗ | P ₇ | P ₆ | P ₅ | P ₄ | P ₃ | P ₂ | P ₁ | P ₀ |
| Shift Left | X | L | L | H | ↗ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ | Q ₀ | L |
| Shift Left | X | H | L | H | ↗ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H |
| Shift Right | L | X | H | L | ↗ | L | Q ₇ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ |
| Shift Right | H | X | H | L | ↗ | H | Q ₇ | Q ₆ | Q ₅ | Q ₄ | Q ₃ | Q ₂ | Q ₁ |
| Hold | X | X | H | H | X | No Change | | | | | | | |
| Hold | X | X | X | X | H | | | | | | | | |
| Hold | X | X | X | X | L | | | | | | | | |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 ↗ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C
Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C) 0°C to +85°C
V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V
Input Voltage (DC) V_{EE} to +0.5V
Output Current (DC Output HIGH) -50 mA
Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-------|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V _{OH} C | Output HIGH Voltage | -1030 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1595 | | | |
| V _{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1035 | | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1045 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current D_n, P_n, S_n CP | | | 220 550 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -238 | -170 | -119 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{shift} | Shift Frequency | 275 | | 275 | | 255 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.90 | 2.40 | 1.10 | 2.30 | 1.10 | 2.50 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |
| t_S | Setup Time D_n, P_n S_n | 0.85 2.20 | | 0.85 2.20 | | 0.85 2.20 | | ns | Figure 4 |
| t_H | Hold D_n, P_n S_n | 0.60 0.10 | | 0.60 0.10 | | 0.60 0.10 | | ns | |
| $t_{pw(H)}$ | Pulse Width HIGH CP | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{shift} | Shift Frequency | 300 | | 300 | | 280 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP to Output | 0.90 | 2.20 | 1.10 | 2.10 | 1.10 | 2.30 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | |
| t_S | Setup Time D_n, P_n S_n | 0.75 2.10 | | 0.75 2.10 | | 0.75 2.10 | | ns | Figure 4 |
| t_H | Hold D_n, P_n S_n | 0.50 0 | | 0.50 0 | | 0.50 0 | | ns | |
| $t_{pw(H)}$ | Pulse Width HIGH CP | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

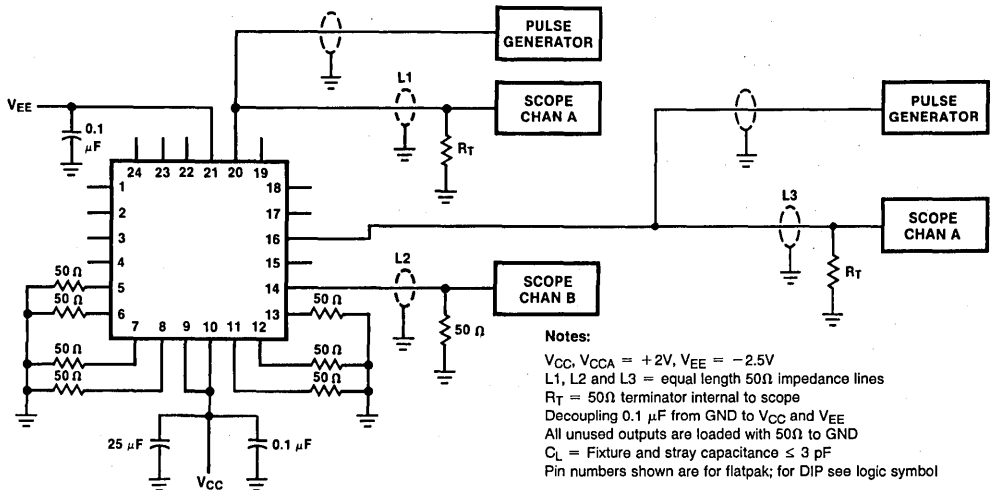
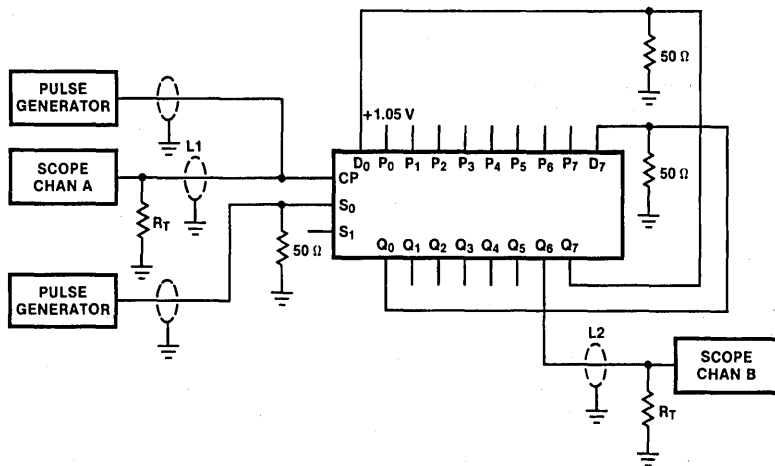


FIGURE 1. AC Test Circuit

TL/F/9856-6

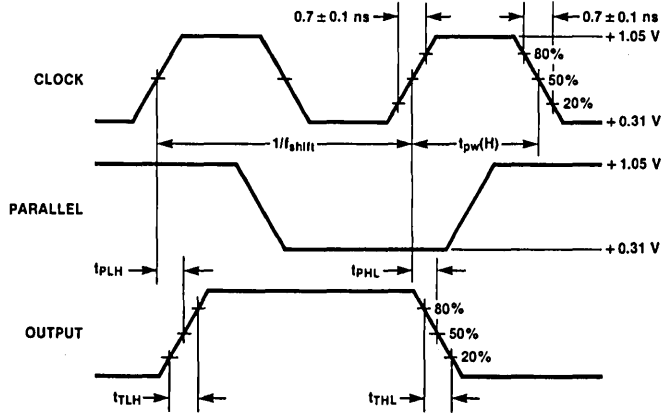


Notes:

For shift right mode pulse generator connected to S_0 is moved to S_1 .
 Pulse generator connected to S_1 has a LOW frequency 99% duty cycle, which allows occasional parallel load.
 The feedback path from output to input should be as short as possible.

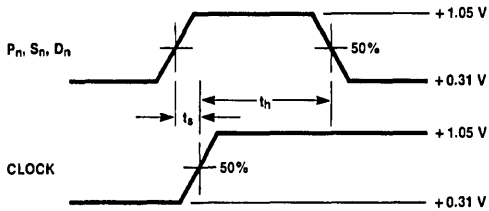
FIGURE 2. Shift Frequency Test Circuit (Shift Left)

TL/F/9856-7



TL/F/9856-8

FIGURE 3. Propagation Delay and Transition Times



Note:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

TL/F/9856-9

FIGURE 4. Setup and Hold Times



F100142

4 x 4-Bit Content Addressable Memory

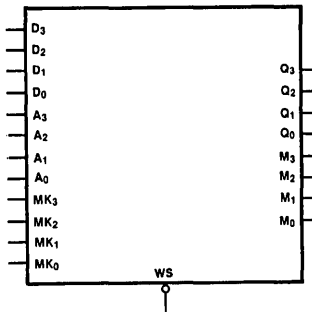
General Description

The F100142 is a 4 word by 4-bit Content Addressable Memory (CAM). Reading is accomplished when an address select input (A_0, A_1, A_2, A_3) is LOW and the write strobe input (\overline{WS}) is HIGH. The corresponding stored word appears on the data outputs (Q_0-Q_3). Writing can be performed to individual bits of a word or to the whole word. (A LOW on an address select input enables a 4-bit word.) A LOW on a bit mask input (MK_0, MK_1, MK_2, MK_3) enables a bit within all four 4-bit words. Write data is presented on the data inputs (D_0, D_1, D_2, D_3) and is latched into the addressed bit latch when the write strobe input (\overline{WS}) is LOW. Hence, the bit

mask inputs are used to selectively store data bit-wise within an addressed word. During writing, the data input word is simultaneously compared to each of the stored memory words. A search/compare is performed by placing a LOW on the bit mask inputs and presenting a data pattern to the data inputs. Corresponding to the bit mask inputs, the match outputs (M_0-M_3) go LOW if a data bit of the pattern matches the respective stored bit. A HIGH on any bit mask input forces a LOW on the respective match output. Each input has a 50 k Ω (typical) pull-down resistor to V_{EE} .

Ordering Code: See Section 8

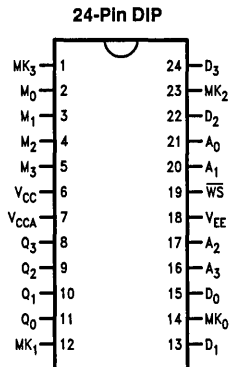
Logic Symbol



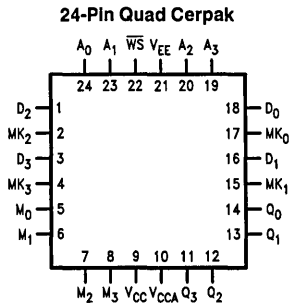
TL/F/9857-3

| Pin Names | Description |
|-----------------|--------------------|
| MK_0-MK_3 | Data Mask Inputs |
| A_0-A_3 | Address Inputs |
| D_0-D_3 | Data Inputs |
| \overline{WS} | Write Strobe Input |
| M_0-M_3 | Match Outputs |
| Q_0-Q_3 | Data Outputs |

Connection Diagrams

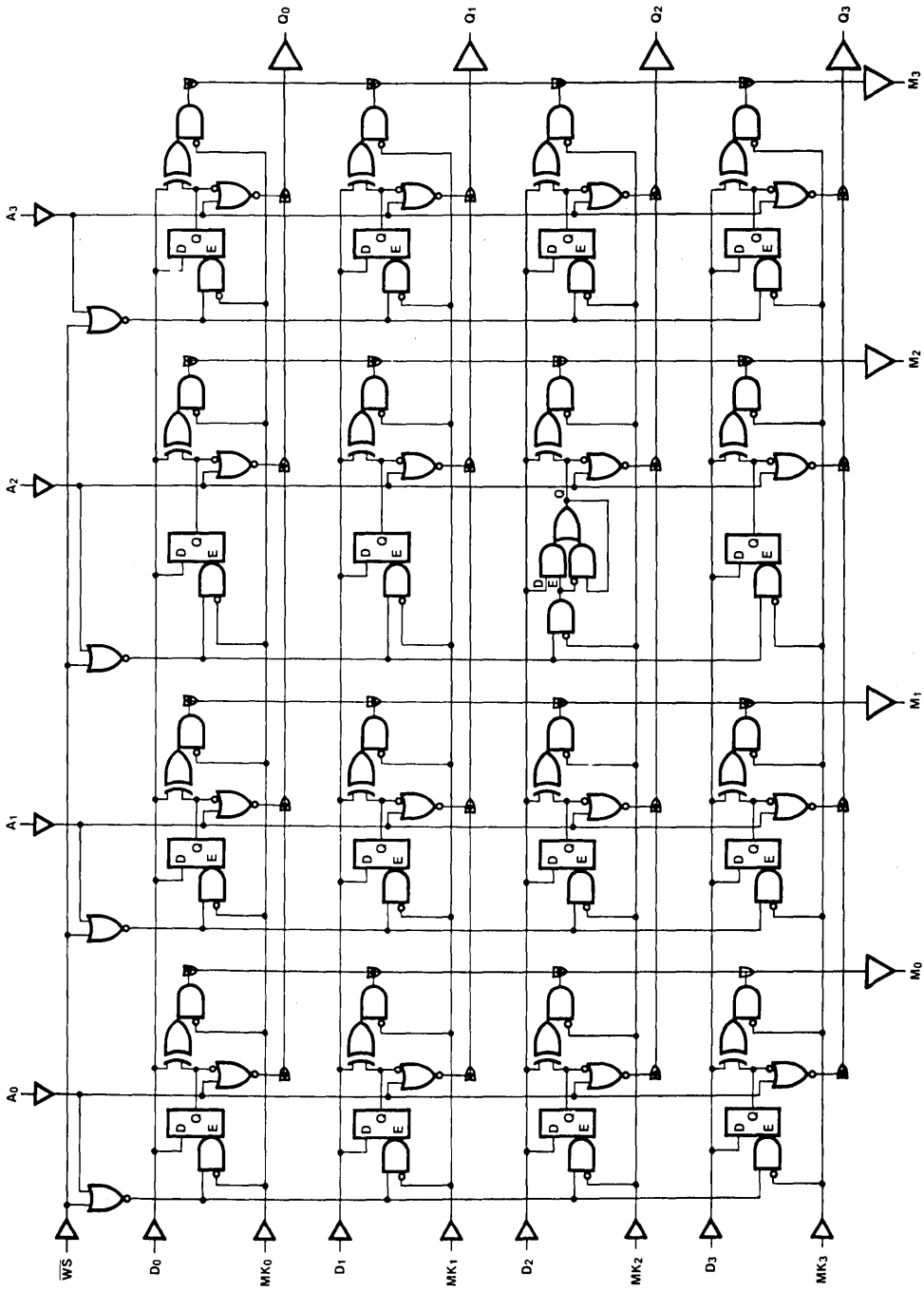


TL/F/9857-1



TL/F/9857-2

Logic Diagram



TL/F/8857-5

100142

Truth Table

| Operation | Inputs | | | | Flip-Flop | Outputs | |
|---------------------|-----------------|----------------------------------|----------------------------------|--------------------------------------|-----------|----------------------------------|----------------------------------|
| | \overline{WS} | A_i | D_j | MK_j | Q_{ij} | M_i | Q_j |
| | \overline{WS} | A_0 A_1 A_2 A_3 | D_0 D_1 D_2 D_3 | MK_0 MK_1 MK_2 MK_3 | | M_0 M_1 M_2 M_3 | Q_0 Q_1 Q_2 Q_3 |
| Write Disabled | X | H | X | X | NC | X | L |
| | X | L | X | H | NC | L | Q_{ijn-1} |
| Write | L | L | H | L | H | L | H |
| | L | L | L | L | L | L | L |
| Read | H | L | X | X | H | X | H |
| | H | L | X | X | L | X | L |
| Match Masked | H | X | X | H | NC | L | X |
| Match Not Satisfied | H | L | H | L | L | H | L |
| | H | H | H | L | L | H | L |
| | H | H | L | L | H | H | L |
| | H | L | L | L | H | H | H |
| Match Satisfied | H | L | H | L | H | L | H |
| | H | H | H | L | H | L | L |
| | H | H | L | L | L | L | L |
| | H | L | L | L | L | L | L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 NC = No Change from Previous State
 \overline{WS} = Write Strobe
 A_i = Address for ith Word
 D_j = Data for jth Bit

MK_j = Data Mask for jth Bit
 H = Mask
 Q_{ij} = Cell State for ith Word, jth Bit
 M_i = Match Output of ith Word
 L = True
 Q_j = Data Output of jth Bit
 Q_{n-1} = Previous Cell State

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C
Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C) 0°C to +85°C
V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V
Input Voltage (DC) V_{EE} to +0.5V
Output Current (DC Output HIGH) -50 mA
Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-------|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V _{OH} C | Output HIGH Voltage | -1030 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1595 | | | |
| V _{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1035 | | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1045 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------------------|------|------|------|---------|-------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 200 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -288 | -190 | -114 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{AD} | Address to Data Out | 1.20 | 4.40 | 1.20 | 4.30 | 1.20 | 4.50 | ns | Figures 2 and 3 |
| t_{DM} | Data In to Match Out Time | 1.60 | 3.70 | 1.60 | 3.60 | 1.60 | 3.80 | ns | Figure 5 |
| t_{MM} | Mask In to "Enable Partial" Match Out Time | 1.20 | 3.90 | 1.20 | 3.90 | 1.20 | 4.00 | ns | |
| t_{DD} | Data In to New Data Out | 1.70 | 4.40 | 1.70 | 4.40 | 1.70 | 4.60 | ns | Figure 2 |
| t_{WD} | Write to New Data Out | 2.50 | 5.40 | 2.50 | 5.20 | 2.30 | 5.10 | ns | |
| t_{AM} | Address to Match | 2.50 | 4.60 | 2.50 | 4.60 | 2.50 | 4.90 | ns | |
| t_{MD} | Mask to Data | 2.20 | 4.90 | 2.20 | 4.80 | 2.20 | 5.00 | ns | |
| t_{WSM} | WS to Match | 2.80 | 4.90 | 2.80 | 4.80 | 2.80 | 5.10 | ns | |
| t_W | Write Pulse Width | 1.30 | | 1.30 | | 1.30 | | ns | |
| t_{AS} | Address Setup before Write Time | 1.40 | | 1.40 | | 1.40 | | ns | Figure 1 |
| t_{AH} | Address Hold after Write Time | 1.40 | | 1.40 | | 1.40 | | ns | |
| t_{DS} | Data In Setup before Write Time | 0.60 | | 0.60 | | 0.60 | | ns | |
| t_{DH} | Data In Hold after Write Time | 1.10 | | 1.10 | | 1.10 | | ns | |
| t_{MH} | Mask In Hold Write Time | 2.50 | | 2.50 | | 2.50 | | ns | |
| t_{MS} | Mask In Setup Write Time | 1.10 | | 1.10 | | 1.10 | | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.50 | 2.30 | 0.50 | 2.30 | 0.50 | 2.30 | ns | Figure 2 |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{AD} | Address to Data Out | 1.20 | 4.20 | 1.20 | 4.10 | 1.20 | 4.30 | ns | Figures 2 and 3 |
| t_{DM} | Data In to Match Out Time | 1.60 | 3.50 | 1.60 | 3.40 | 1.60 | 3.60 | ns | Figure 5 |
| t_{MM} | Mask In to "Enable Partial" Match Out Time | 1.20 | 3.70 | 1.20 | 3.70 | 1.20 | 3.80 | ns | |
| t_{DD} | Data In to New Data Out | 1.70 | 4.20 | 1.70 | 4.20 | 1.70 | 4.40 | ns | Figure 2 |
| t_{WD} | Write to New Data Out | 2.50 | 5.20 | 2.50 | 5.00 | 2.30 | 4.90 | ns | |
| t_{AM} | Address to Match | 2.50 | 4.40 | 2.50 | 4.40 | 2.50 | 4.70 | ns | |
| t_{MD} | Mask to Data | 2.20 | 4.70 | 2.20 | 4.60 | 2.20 | 4.80 | ns | |
| t_{WSM} | WS to Match | 2.80 | 4.70 | 2.80 | 4.60 | 2.80 | 4.90 | ns | |
| t_W | Write Pulse Width | 1.20 | | 1.20 | | 1.20 | | ns | |
| t_{AS} | Address Setup before Write Time | 1.30 | | 1.30 | | 1.30 | | ns | Figure 1 |
| t_{AH} | Address Hold after Write Time | 1.30 | | 1.30 | | 1.30 | | ns | |
| t_{DS} | Data In Setup before Write Time | 0.50 | | 0.50 | | 0.50 | | ns | |
| t_{DH} | Data In Hold after Write Time | 1.00 | | 1.00 | | 1.00 | | ns | |
| t_{MH} | Mask In Hold Write Time | 2.40 | | 2.40 | | 2.40 | | ns | |
| t_{MS} | Mask In Setup Write Time | 1.00 | | 1.00 | | 1.00 | | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.50 | 2.20 | 0.50 | 2.20 | 0.50 | 2.20 | ns | Figure 2 |

Switching Waveforms

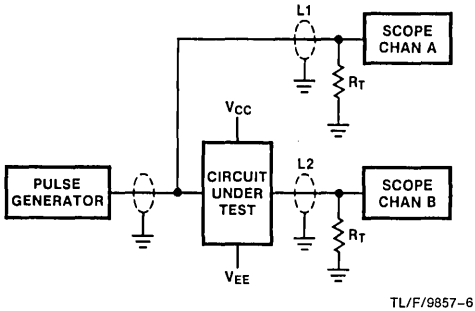


FIGURE 1. AC Test Circuit

TL/F/9857-6

Note:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1, L2 and L3 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF

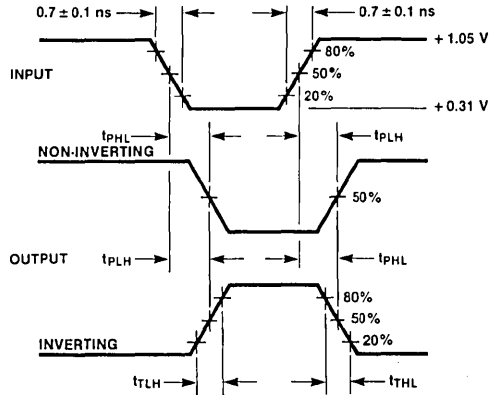


FIGURE 2. Output Rise and Fall Times and Waveforms

TL/F/9857-7

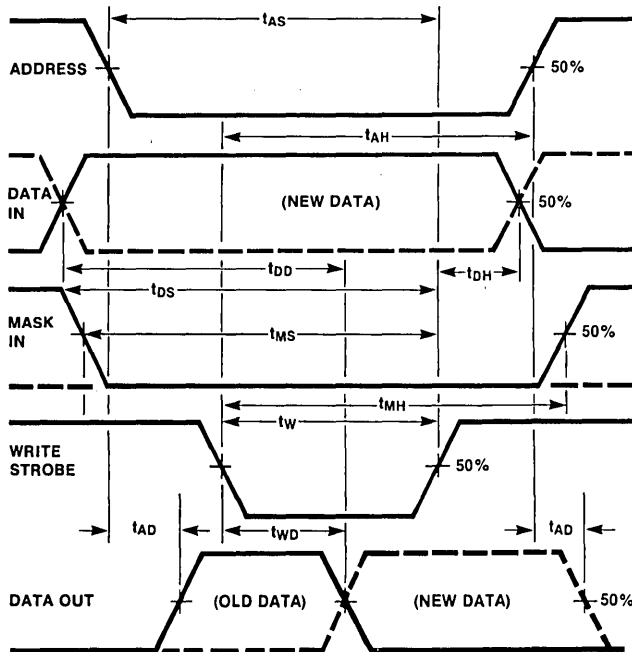


FIGURE 3. Write Mode and Read/Write Mode Waveforms

TL/F/9857-8

Switching Waveforms (Continued)

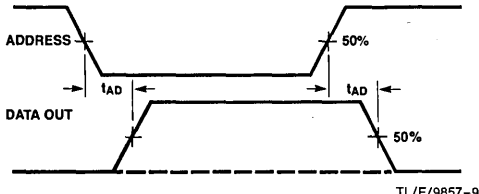


FIGURE 4. Read Mode Waveforms

TL/F/9857-9

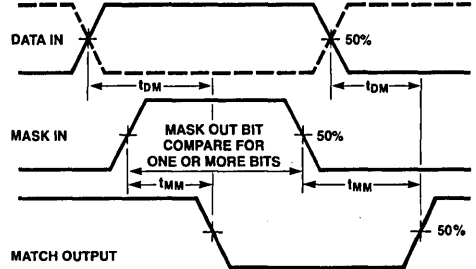


FIGURE 5. Search Mode Waveforms

TL/F/9857-10

Application

The F100142 is an ideal choice for the register file unit of a bit-slice processor. *Figure 5* shows the configuration of four F100145s into a 16 x 16 register file. The write enables (WE_1 , WE_2) and output enables (OE_1 , OE_2) are configured to allow access to one array of sixteen 16-bit registers or two arrays of sixteen 8-bit registers. Simultaneous read and write addressing is made possible with separate buses. Also, reading and then writing to the same address is easily and efficiently done by tying one write enable to an output enable.

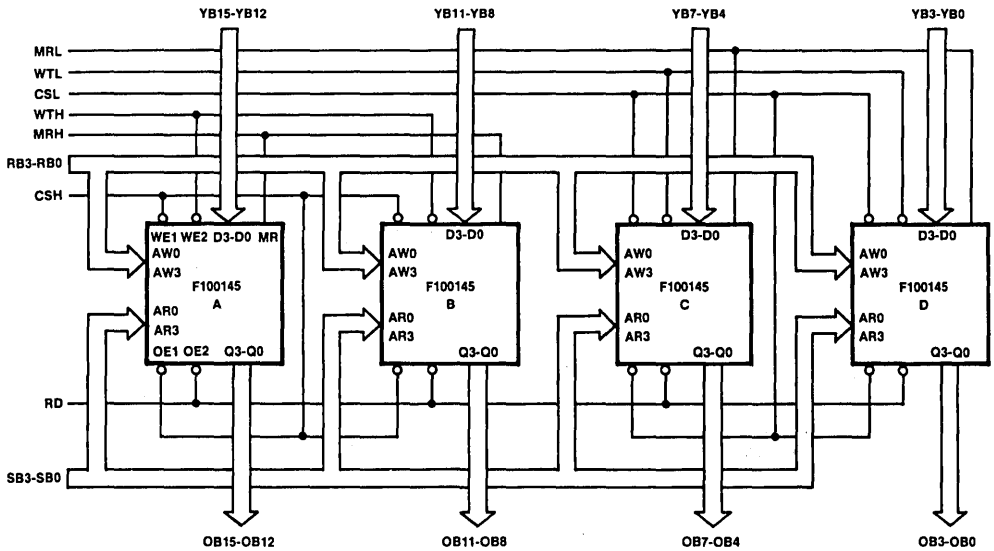


FIGURE 5. 16 x 16 Register File (Two 16 x 8 Register Files)

TL/F/9857-11

F100150 Hex D Latch

General Description

The F100150 contains six D-type latches with true and complement outputs, a pair of common Enables (\bar{E}_a and \bar{E}_b), and a common Master Reset (MR). A Q output follows its D input when both \bar{E}_a and \bar{E}_b are LOW. When either \bar{E}_a or \bar{E}_b (or both) are HIGH, a latch stores the last valid data present on its D input before \bar{E}_a or \bar{E}_b went HIGH. The MR input

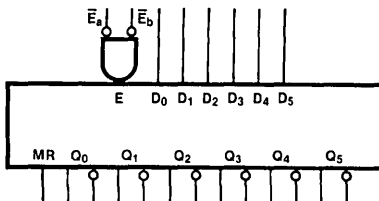
overrides all other inputs and makes the Q outputs LOW. All inputs have 50 k Ω pull-down resistors.

Refer to the F100350 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

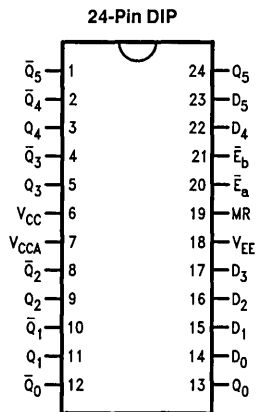
Logic Symbol



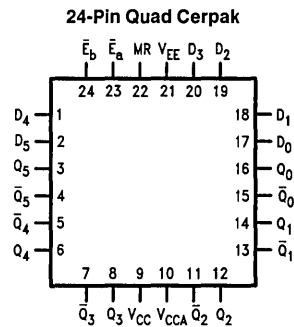
TL/F/9858-3

| Pin Names | Description |
|--------------------------------|-----------------------------------|
| D ₀ -D ₅ | Data Inputs |
| \bar{E}_a, \bar{E}_b | Common Enable Inputs (Active LOW) |
| MR | Asynchronous Master Reset Input |
| Q ₀ -Q ₅ | Data Outputs |
| \bar{Q}_0 - \bar{Q}_5 | Complementary Data Outputs |

Connection Diagrams

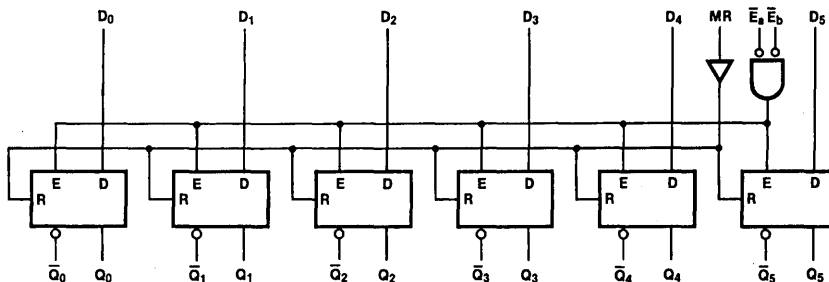


TL/F/9858-1



TL/F/9858-2

Logic Diagram



TL/F/9858-5

Truth Tables (Each Latch)

Latch Operation

| Inputs | | | | Outputs |
|--------|-------------|-------------|----|----------|
| D_n | \bar{E}_a | \bar{E}_b | MR | Q_n |
| L | L | L | L | L |
| H | L | L | L | H |
| X | H | X | L | Latched* |
| X | X | H | L | Latched* |

*Retains data present before \bar{E} positive transition

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Asynchronous Operation

| Inputs | | | | Outputs |
|--------|-------------|-------------|----|---------|
| D_n | \bar{E}_a | \bar{E}_b | MR | Q_n |
| X | X | X | H | L |

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

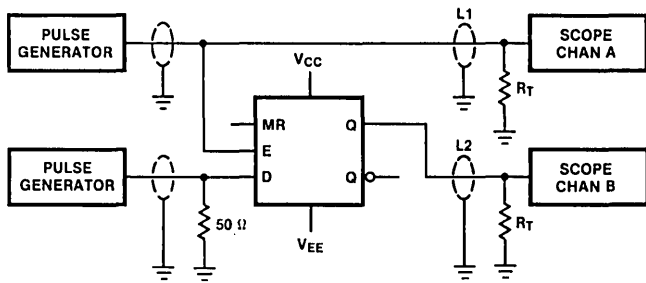
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|-------------------|---------|-------------------------------|
| I_{IH} | Input HIGH Current MR D_n \bar{E}_a, \bar{E}_b | | | 450 340 520 | μA | $V_{IN} = V_{IH}(\text{Max})$ |
| I_{EE} | Power Supply Current | -159 | -113 | -79 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output (Transparent Mode) | 0.45 | 1.50 | 0.50 | 1.40 | 0.50 | 1.50 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_a, \bar{E}_b to Output | 0.75 | 2.05 | 0.75 | 1.85 | 0.75 | 2.05 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 0.80 | 2.40 | 0.90 | 2.40 | 0.90 | 2.60 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.60 | 0.45 | 1.60 | ns | Figures 1 and 2 |
| t_s | Setup Time D_0-D_5 MR (Release Time) | 0.70 2.10 | | 0.70 2.10 | | 0.70 2.10 | | ns | Figures 3 and 4 |
| t_h | Hold Time, D_0-D_5 | 0.70 | | 0.70 | | 0.70 | | ns | Figure 4 |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E}_a, \bar{E}_b | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |
| $t_{pw(H)}$ | Pulse Width HIGH, MR | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output (Transparent Mode) | 0.45 | 1.30 | 0.50 | 1.20 | 0.50 | 1.30 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_a, \bar{E}_b to Output | 0.75 | 1.85 | 0.75 | 1.65 | 0.75 | 1.85 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 0.80 | 2.20 | 0.90 | 2.20 | 0.90 | 2.40 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.50 | 0.45 | 1.50 | ns | Figures 1 and 2 |
| t_s | Setup Time D_0-D_5 MR (Release Time) | 0.60 2.00 | | 0.60 2.00 | | 0.60 2.00 | | ns | Figures 3 and 4 |
| t_h | Hold Time, D_0-D_5 | 0.60 | | 0.60 | | 0.60 | | ns | Figure 4 |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E}_a, \bar{E}_b | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |
| $t_{pw(H)}$ | Pulse Width HIGH, MR | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

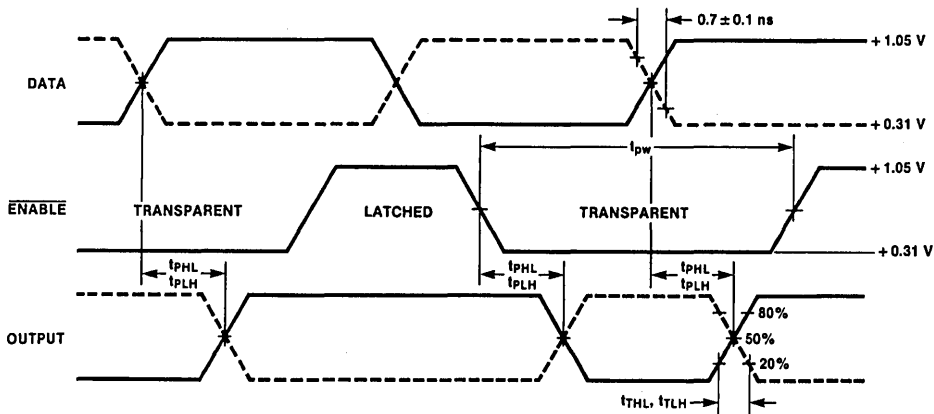


Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance $\leq 3 pF$

TL/F/9858-6

FIGURE 1. AC Test Circuit



TL/F/9858-7

FIGURE 2. Enable Timing

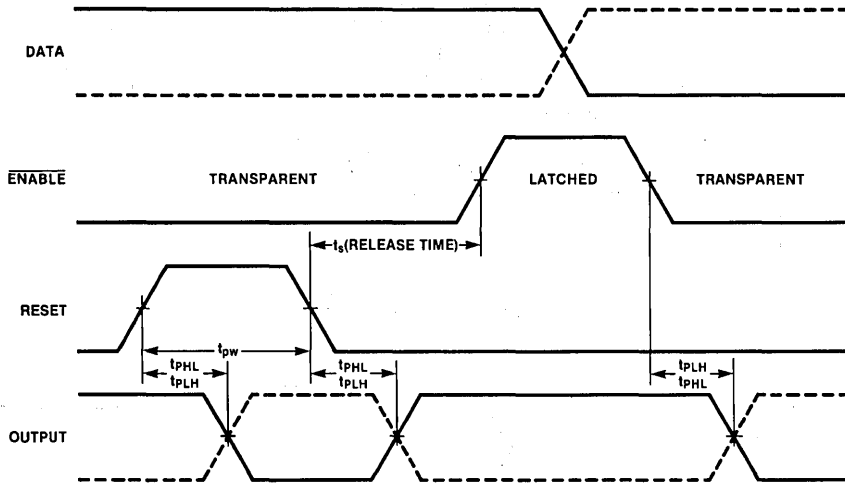
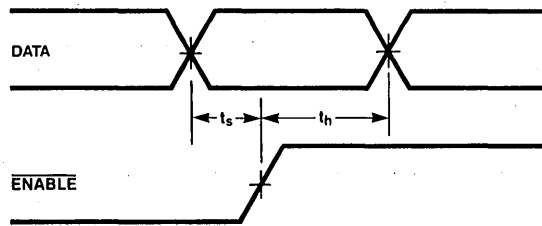


FIGURE 3. Reset Timing

TL/F/9858-8



TL/F/9858-9

Notes:

- t_s is the minimum time before the transition of the enable that information must be present at the data input.
- t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

FIGURE 4. Data Setup and Hold Time

F100151 Hex D Flip-Flop

General Description

The F100151 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs (CP_a and CP_b) and common Master Reset (MR) input. Data enters a master when both CP_a and CP_b are LOW and transfers to the slave when CP_a and CP_b (or both) go HIGH. The MR input overrides all other inputs

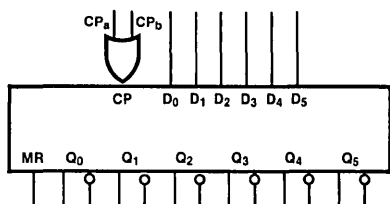
and makes the Q outputs LOW. All inputs have 50 k Ω pull-down resistors.

Refer to the F100351 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

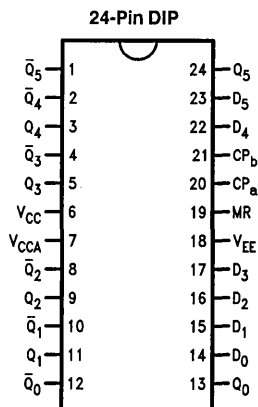
Logic Symbol



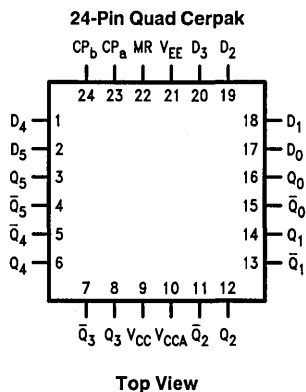
TL/F/9859-3

| Pin Names | Description |
|---------------------------|---------------------------------|
| D_0 - D_5 | Data Inputs |
| CP_a , CP_b | Common Clock Inputs |
| MR | Asynchronous Master Reset Input |
| Q_0 - Q_5 | Data Outputs |
| \bar{Q}_0 - \bar{Q}_5 | Complementary Data Outputs |

Connection Diagrams

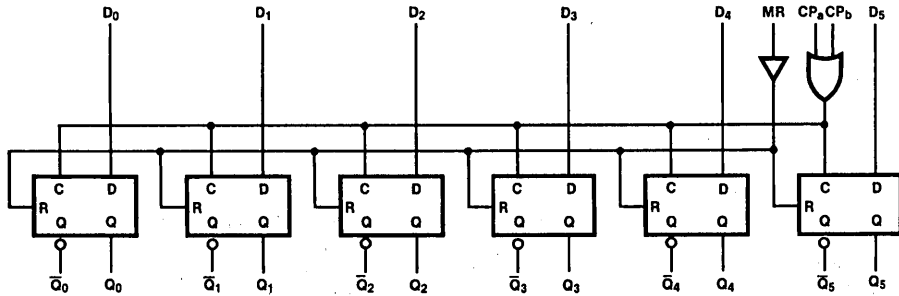


TL/F/9859-1



TL/F/9859-2

Logic Diagram



TL/F/9859-5

Truth Table (Each Flip-flop)

Synchronous Operation

| Inputs | | | | Outputs |
|--------|--------|--------|----|------------|
| D_n | CP_a | CP_b | MR | $Q_n(t+1)$ |
| L | ↗ | L | L | L |
| H | ↗ | L | L | H |
| L | L | ↗ | L | L |
| H | L | ↗ | L | H |
| X | H | ↗ | L | $Q_n(t)$ |
| X | ↗ | H | L | $Q_n(t)$ |
| X | L | L | L | $Q_n(t)$ |

Asynchronous Operation

| Inputs | | | | Outputs |
|--------|--------|--------|----|------------|
| D_n | CP_a | CP_b | MR | $Q_n(t+1)$ |
| X | X | X | H | L |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

t = Time before CP positive transition

t+1 = Time after CP positive transition

↗ = LOW-to-HIGH transition

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|---------|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

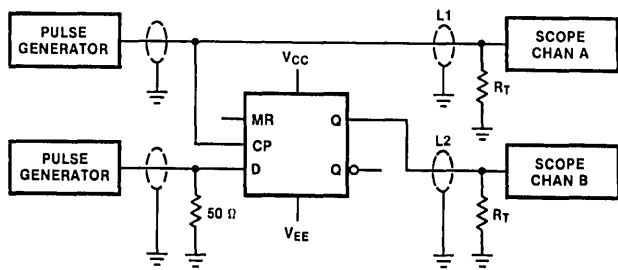
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|-------------------|---------|-------------------------|
| I_{IH} | Input HIGH Current MR D ₀ -D ₅ CP _a , CP _b | | | 450 225 520 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -210 | -155 | -98 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|----------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{max} | Toggle Frequency | 375 | | 375 | | 375 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP _a , CP _b to Output | 0.80 | 2.20 | 0.80 | 2.20 | 0.90 | 2.40 | ns | Figures 1 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 1.20 | 2.90 | 1.30 | 3.00 | 1.20 | 3.10 | ns | Figures 1 and 4 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.70 | 0.45 | 1.80 | ns | Figures 1 and 3 |
| t_s | Setup Time D ₀ -D ₅ MR (Release Time) | 0.70 2.30 | | 0.70 2.30 | | 0.70 2.60 | | ns | Figure 5 Figure 4 |
| t_h | Hold Time D ₀ -D ₅ | 0.70 | | 0.70 | | 0.70 | | ns | Figure 5 |
| $t_{pw(H)}$ | Pulse Width HIGH CP _a , CP _b , MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

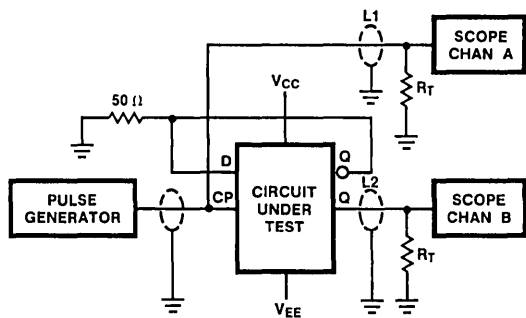
| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|----------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| f_{max} | Toggle Frequency | 375 | | 375 | | 375 | | MHz | Figures 2 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay CP _a , CP _b to Output | 0.80 | 2.00 | 0.80 | 2.00 | 0.90 | 2.20 | ns | Figures 1 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 1.20 | 2.70 | 1.30 | 2.80 | 1.20 | 2.90 | ns | Figures 1 and 4 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.60 | 0.45 | 1.70 | ns | Figures 1 and 3 |
| t_s | Setup Time D ₀ -D ₅ MR (Release Time) | 0.60 2.20 | | 0.60 2.20 | | 0.60 2.50 | | ns | Figure 5 Figure 4 |
| t_h | Hold Time D ₀ -D ₅ | 0.60 | | 0.60 | | 0.60 | | ns | Figure 5 |
| $t_{pw(H)}$ | Pulse Width HIGH CP _a , CP _b , MR | 2.00 | | 2.00 | | 2.00 | | ns | Figures 3 and 4 |



Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance ≤ 3 pF

TL/F/9859-6

FIGURE 1. AC Test Circuit



Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Jig and stray capacitance ≤ 3 pF

TL/F/9859-7

FIGURE 2. Toggle Frequency Test Circuit

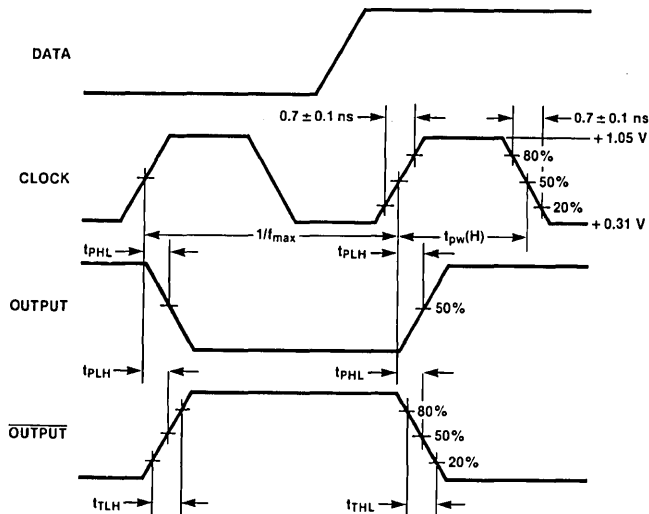


FIGURE 3. Propagation Delay (Clock) and Transition Times

TL/F/9859-8

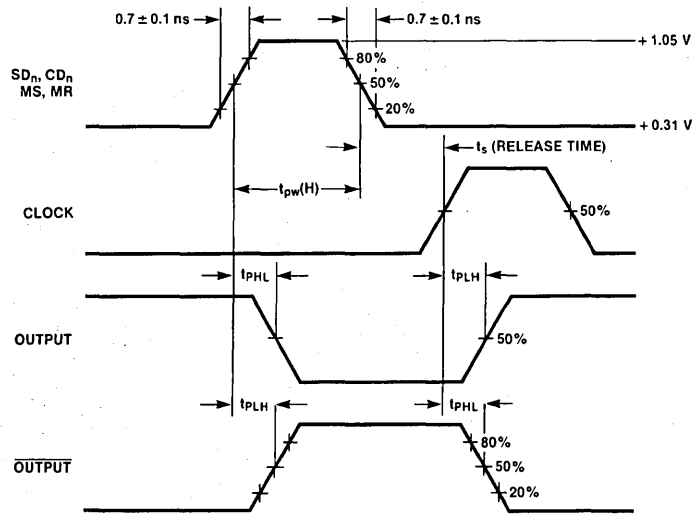
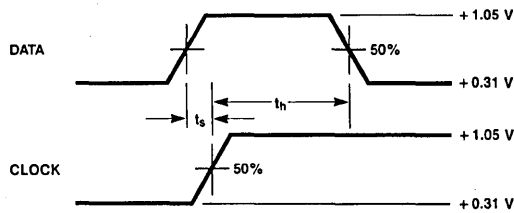


FIGURE 4. Propagation Delay (Reset)

TL/F/9859-9



TL/F/9859-10

Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time

F100155

Quad Multiplexer/Latch

General Description

The F100155 contains four transparent latches, each of which can accept and store data from two sources. When both Enable (\bar{E}_n) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1 , the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from ei-

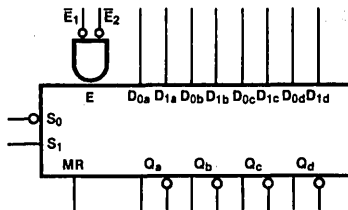
ther D_0 or D_1 . A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 k Ω pulldown resistors.

Refer to the F100355 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

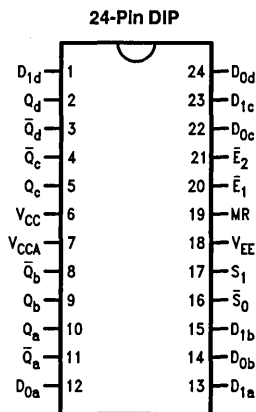
Logic Symbol



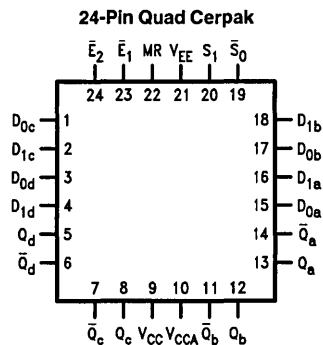
TL/F/9860-3

| Pin Names | Description |
|------------------------|----------------------------|
| \bar{E}_1, \bar{E}_2 | Enable Inputs (Active LOW) |
| \bar{S}_0, S_1 | Select Inputs |
| MR | Master Reset |
| $D_{na}-D_{nd}$ | Data Inputs |
| Q_a-Q_d | Data Outputs |
| $\bar{Q}_a-\bar{Q}_d$ | Complementary Data Outputs |

Connection Diagrams

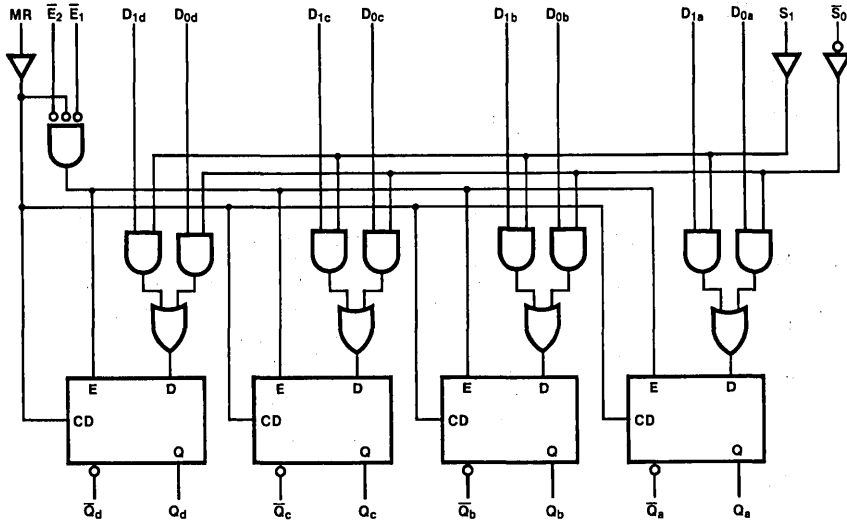


TL/F/9860-1



TL/F/9860-2

Logic Diagram



TL/F/9860-5

Operating Mode Table

| Controls | | | | Outputs |
|-------------|-------------|-------|-------------|-------------------|
| \bar{E}_1 | \bar{E}_2 | S_1 | \bar{S}_0 | Q_n |
| H | X | X | X | Latched* |
| X | H | X | X | Latched* |
| L | L | L | L | D_{0x} |
| L | L | H | L | $D_{0x} + D_{1x}$ |
| L | L | L | H | L |
| L | L | H | H | D_{1x} |

*Stores data present before \bar{E} went HIGH

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

Truth Table

| Inputs | | | | | | Outputs | | |
|--------|-------------|-------------|-------|-------------|----------|----------|-------------|----------|
| MR | \bar{E}_1 | \bar{E}_2 | S_1 | \bar{S}_0 | D_{1x} | D_{0x} | \bar{Q}_x | Q_x |
| H | X | X | X | X | X | X | H | L |
| L | L | L | H | H | H | X | L | H |
| L | L | L | H | H | L | X | H | L |
| L | L | L | L | L | X | H | L | H |
| L | L | L | L | L | X | L | H | L |
| L | L | L | L | H | X | X | H | L |
| L | L | L | H | L | L | L | H | L |
| L | H | X | X | X | X | X | Latched* | Latched* |
| L | X | H | X | X | X | X | Latched* | Latched* |

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C
Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C) 0°C to +85°C
V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V
Input Voltage (DC) V_{EE} to +0.5V
Output Current (DC Output HIGH) -50 mA
Operating Range (Note 2) -5.0V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-------|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V _{OHC} | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V _{OHC} | Output HIGH Voltage | -1030 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1595 | | | |
| V _{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1035 | | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V _{OHC} | Output HIGH Voltage | -1045 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OLC} | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|-----|--------------------------|---------|-------------------------------|
| I_{IH} | Input HIGH Current \bar{S}_0, S_1 \bar{E}_1, \bar{E}_2 $D_{na}-D_{nd}$ MR | | | 220 350 340 430 | μA | $V_{IN} = V_{IH}(\text{Max})$ |
| I_{EE} | Power Supply Current | -133 | -95 | -66 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristic $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode) | 0.50 | 1.90 | 0.60 | 1.85 | 0.50 | 1.90 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay \bar{S}_0, S_1 to Output (Transparent Mode) | 1.50 | 3.50 | 1.50 | 3.40 | 1.50 | 3.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_1, \bar{E}_2 to Output | 0.90 | 2.50 | 1.00 | 2.40 | 1.00 | 2.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 0.90 | 3.00 | 0.90 | 2.90 | 0.90 | 3.00 | ns | <i>Figures 1 and 3</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.60 | 2.30 | 0.60 | 2.20 | 0.45 | 2.30 | ns | <i>Figures 1 and 2</i> |
| t_s | Setup Time $D_{na}-D_{nd}$ | 0.90 | | 0.90 | | 0.90 | | ns | <i>Figure 4</i> |
| | \bar{S}_0, S_1 | 2.40 | | 2.40 | | 2.70 | | | <i>Figure 3</i> |
| | MR (Release Time) | 1.50 | | 1.50 | | 1.50 | | | |
| t_H | Hold Time $D_{na}-D_{nd}$ | 0.40 | | 0.40 | | 0.40 | | ns | <i>Figure 4</i> |
| | \bar{S}_0, S_1 | -0.70 | | -0.70 | | -0.70 | | | |
| $t_{pw}(L)$ | Pulse Width LOW \bar{E}_1, \bar{E}_2 | 2.00 | | 2.00 | | 2.00 | | ns | <i>Figure 2</i> |
| $t_{pw}(H)$ | Pulse Width HIGH MR | 2.00 | | 2.00 | | 2.00 | | ns | <i>Figure 3</i> |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $D_{na}-D_{nd}$ to Output (Transparent Mode) | 0.50 | 1.70 | 0.60 | 1.65 | 0.50 | 1.70 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay \bar{S}_1, S_1 to Output (Transparent Mode) | 1.50 | 3.30 | 1.50 | 3.20 | 1.50 | 3.30 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E}_1, \bar{E}_2 to Output | 0.90 | 2.30 | 1.00 | 2.20 | 1.00 | 2.30 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$ (Continued)

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 0.90 | 2.80 | 0.90 | 2.70 | 0.90 | 2.80 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.60 | 2.20 | 0.60 | 2.10 | 0.45 | 2.20 | ns | Figures 1 and 2 |
| t_S | Setup Time $D_{na}-D_{nd}$ | 0.80 | | 0.80 | | 0.80 | | ns | Figure 4 |
| | \bar{S}_0, S_1 | 2.30 | | 2.30 | | 2.60 | | | |
| | MR (Release Time) | 1.40 | | 1.40 | | 1.40 | | | Figure 3 |
| t_H | Hold Time $D_{na}-D_{nd}$ | 0.30 | | 0.30 | | 0.30 | | ns | Figure 4 |
| | \bar{S}_0, S_1 | -0.80 | | -0.80 | | -0.80 | | | |
| $t_{pw}(L)$ | Pulse Width LOW \bar{E}_1, \bar{E}_2 | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |
| $t_{pw}(H)$ | Pulse Width HIGH MR | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

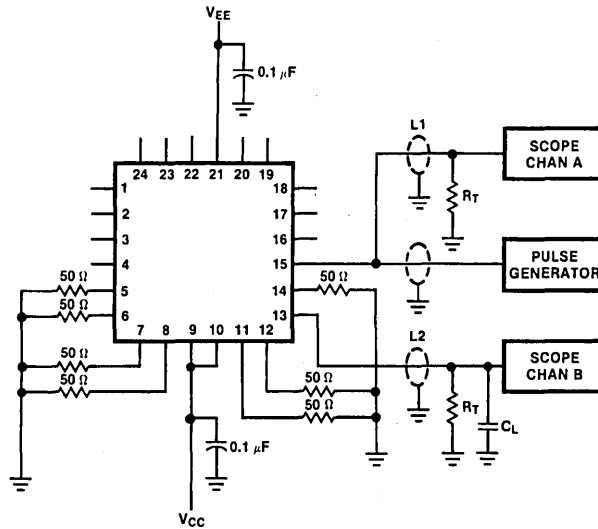


FIGURE 1. AC Test Circuit

TL/F/9860-6

Notes:

$V_{CC}, V_{CCA} = +2V$, $V_{EE} = -2.5V$

L_1 and L_2 = equal length 50Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling $0.1\ \mu F$ from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50Ω to GND

C_L = Fixture and stray capacitance $\leq 3\ pF$

Pin numbers shown are for flatpak; for DIP see logic symbol

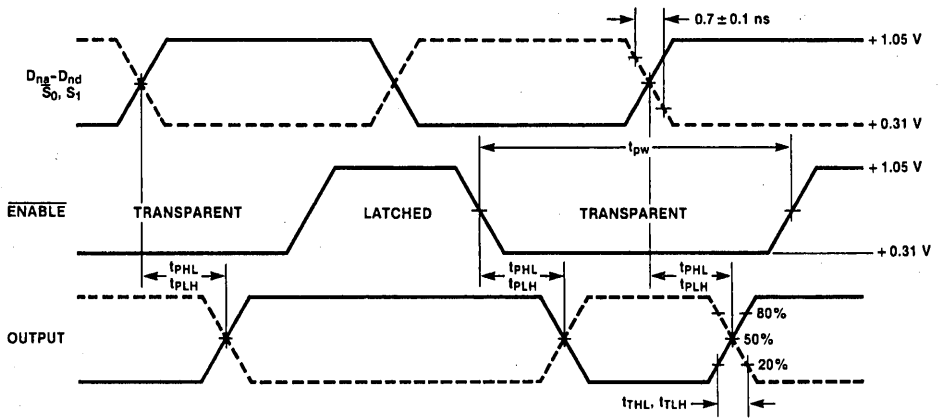


FIGURE 2. Enable Timing

TL/F/9860-7

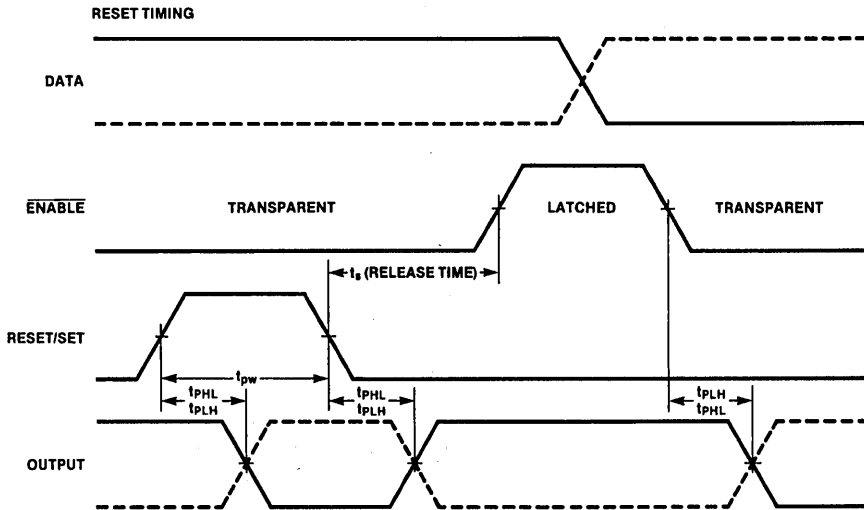


FIGURE 3. Reset Timing

TL/F/9860-8

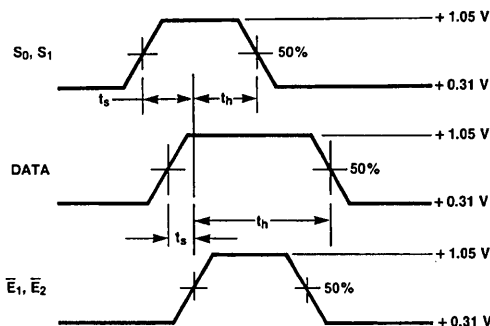


FIGURE 4. Data Setup and Hold Times

TL/F/9860-9

Notes:

t_s is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

F100156 Mask-Merge/Latch

General Description

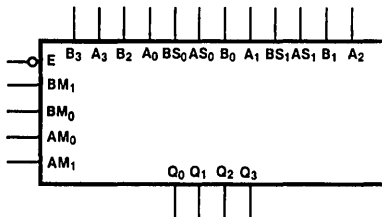
The F100156 merges two 4-bit words to form a 4-bit output word. The AM_n enable allows the merge of A into B by one, two or three places (per the AS_n value) from the left. The BM_n enable similarly allows the merge of B into A from the left (per the BS_n value). The B merge overrides the A merge when both are enabled. This means A first merges into B and B then merges into the A merge. If the B address is

equal to or greater than the A address, then outputs are forced to B.

The merge outputs feed four latches, which have a common enable (\bar{E}) input. All inputs have a 50 k Ω (typical) pull-down resistor tied to V_{EE} .

Ordering Code: See Section 8

Logic Symbol



TL/F/9861-3

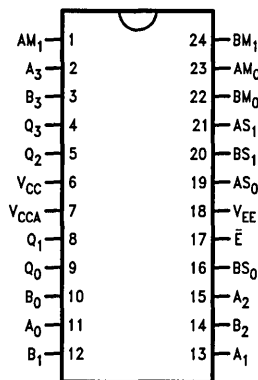
Note:

When \bar{E} is HIGH, Q_n outputs do not change.
When \bar{E} is LOW, $Q_n = A$ or B depending on which is selected.

| Pin Names | Description |
|--------------|---------------------------------|
| \bar{E} | Latch Enable Input (Active LOW) |
| A_0-A_3 | A Data Inputs |
| B_0-B_3 | B Data Inputs |
| AM_0, AM_1 | A Merge Enable Inputs |
| BM_0, BM_1 | B Merge Enable Inputs |
| AS_0, AS_1 | A Address Inputs |
| BS_0, BS_1 | B Address Inputs |
| Q_0-Q_3 | Data Outputs |

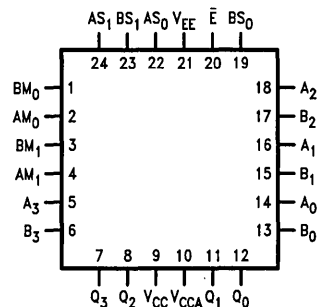
Connection Diagrams

24-Pin DIP



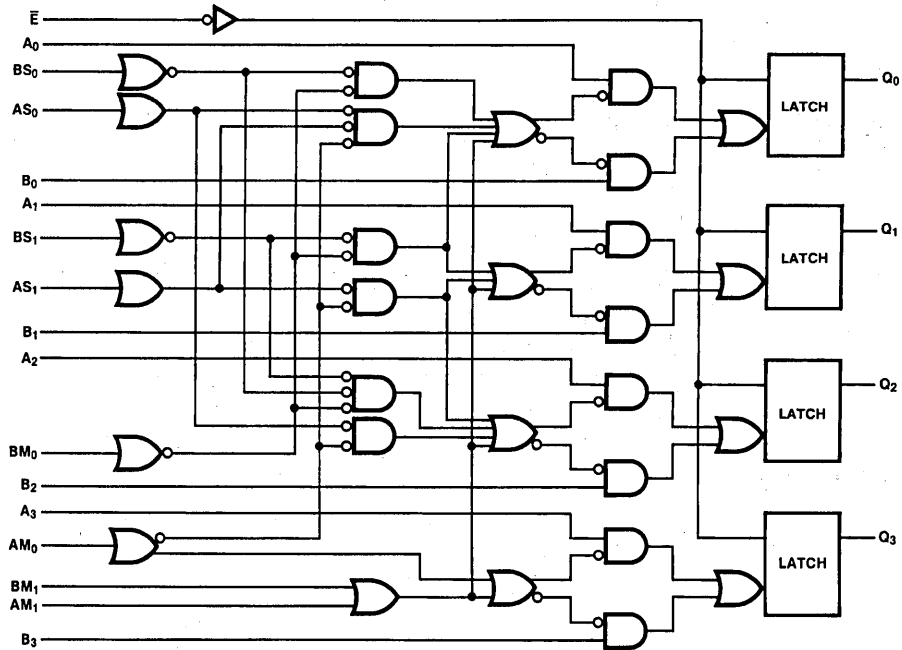
TL/F/9861-1

24-Pin Quad Cerpak



TL/F/9861-2

Logic Diagram



TL/F/9861-5

Truth Table

| Inputs | | | | | | | | | Outputs | | | | Remarks |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------|----------------|----------------|----------------|----------------|------------------------------------|
| Merge Enables | | | | Addresses | | | | \bar{E} | Q ₀ | Q ₁ | Q ₂ | Q ₃ | |
| BM ₁ | BM ₀ | AM ₁ | AM ₀ | BS ₁ | BS ₀ | AS ₁ | AS ₀ | | | | | | |
| X | X | H | X | X | X | X | X | L | B ₀ | B ₁ | B ₂ | B ₃ | Select B |
| H | X | X | X | X | X | X | X | L | B ₀ | B ₁ | B ₂ | B ₃ | |
| L | L | L | L | X | X | X | X | L | A ₀ | A ₁ | A ₂ | A ₃ | Select A |
| L | L | L | H | X | X | L | L | L | B ₀ | B ₁ | B ₂ | B ₃ | Merge A → B |
| L | L | L | H | X | X | L | H | L | A ₀ | B ₁ | B ₂ | B ₃ | |
| L | L | L | H | X | X | H | L | L | A ₀ | A ₁ | B ₂ | B ₃ | |
| L | L | L | H | X | X | H | H | L | A ₀ | A ₁ | A ₂ | B ₃ | |
| L | H | L | L | L | L | X | X | L | A ₀ | A ₁ | A ₂ | A ₃ | Merge B → A |
| L | H | L | L | L | H | X | X | L | B ₀ | A ₁ | A ₂ | A ₃ | |
| L | H | L | L | H | L | X | X | L | B ₀ | B ₁ | A ₂ | A ₃ | |
| L | H | L | L | H | H | X | X | L | B ₀ | B ₁ | B ₂ | A ₃ | |
| L | H | L | H | L | L | L | H | L | A ₀ | B ₁ | B ₂ | B ₃ | Merge A → B |
| L | H | L | H | L | L | H | L | L | A ₀ | A ₁ | B ₂ | B ₃ | |
| L | H | L | H | L | L | H | H | L | A ₀ | A ₁ | A ₂ | B ₃ | |
| L | H | L | H | L | H | H | L | L | B ₀ | A ₁ | B ₂ | B ₃ | Merge A → B then Merge B → A |
| L | H | L | H | L | H | H | H | L | B ₀ | A ₁ | A ₂ | B ₃ | |
| L | H | L | H | H | L | H | H | L | B ₀ | B ₁ | A ₂ | B ₃ | |
| L | H | L | H | H | H | H | H | L | B ₀ | B ₁ | B ₂ | B ₃ | B Address ≥ A Address |
| L | H | L | H | H | H | H | L | L | B ₀ | B ₁ | B ₂ | B ₃ | |
| L | H | L | H | H | H | L | H | L | B ₀ | B ₁ | B ₂ | B ₃ | |
| L | H | L | H | H | H | L | L | L | B ₀ | B ₁ | B ₂ | B ₃ | |
| L | H | L | H | H | L | L | L | L | B ₀ | B ₁ | B ₂ | B ₃ | |
| L | H | L | H | H | L | L | L | L | B ₀ | B ₁ | B ₂ | B ₃ | |
| L | H | L | H | H | L | L | L | L | B ₀ | B ₁ | B ₂ | B ₃ | |
| L | H | L | H | H | L | L | L | L | B ₀ | B ₁ | B ₂ | B ₃ | |
| X | X | X | X | X | X | X | X | H | Q ₀ | Q ₁ | Q ₂ | Q ₃ | Latch |
| Before Start | At Start | After End | At End | | | | | | | | | | |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

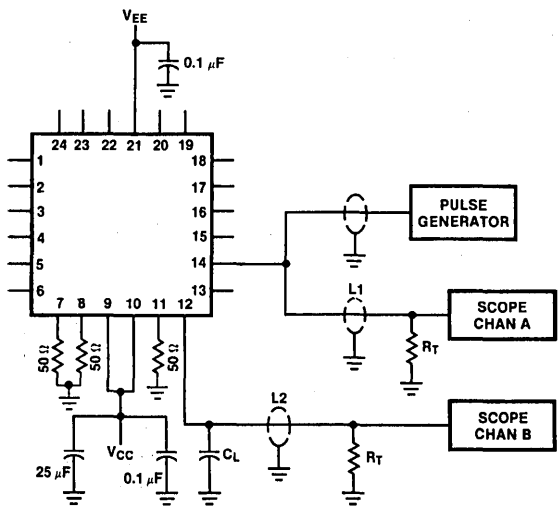
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|------|---------|-------------------------|
| I_{IH} | Input HIGH Current $A_n, B_n, BM_n, AM_n, BS_n, AS_n, \bar{E}$ | | | 265 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -235 | -161 | -107 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to Outputs (Transparent Mode) | 0.45 | 1.90 | 0.50 | 1.80 | 0.50 | 2.00 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to Outputs | 1.00 | 2.50 | 1.00 | 2.40 | 1.00 | 2.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode) | 1.20 | 3.70 | 1.20 | 3.70 | 1.20 | 3.80 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.90 | 0.45 | 1.80 | 0.45 | 1.90 | ns | |
| t_s | Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n | 0.80 2.90 | | 0.80 2.90 | | 0.80 2.90 | | ns | Figure 3 |
| t_H | Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n | 2.10 0.80 | | 2.10 0.80 | | 2.10 0.80 | | ns | |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E} | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

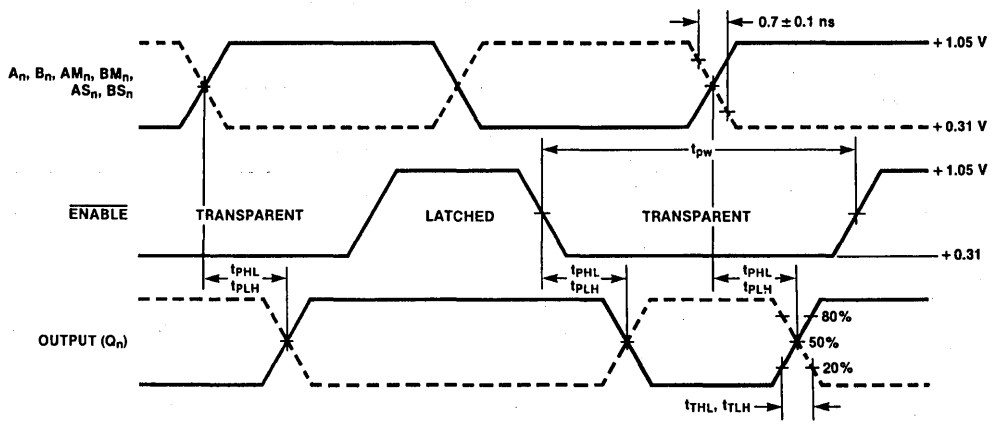
| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to Outputs (Transparent Mode) | 0.45 | 1.70 | 0.50 | 1.60 | 0.50 | 1.80 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to Outputs | 1.00 | 2.30 | 1.00 | 2.20 | 1.00 | 2.30 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay AM_n, BM_n, AS_n, BS_n to Outputs (Transparent Mode) | 1.20 | 3.50 | 1.20 | 3.50 | 1.20 | 3.60 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.70 | 0.45 | 1.80 | ns | |
| t_s | Setup Time A_n, B_n AM_n, BM_n, AS_n, BS_n | 0.70 2.80 | | 0.70 2.80 | | 0.70 2.80 | | ns | Figure 3 |
| t_H | Hold Time A_n, B_n AM_n, BM_n, AS_n, BS_n | 2.00 0.70 | | 2.00 0.70 | | 2.00 0.70 | | ns | |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E} | 2.00 | | 2.00 | | 2.00 | | ns | Figure 2 |



TL/F/9861-6

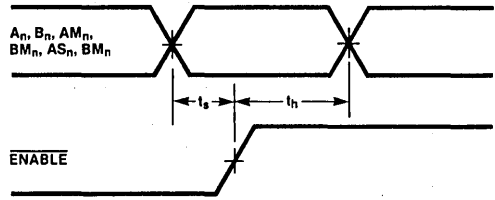
Notes:
 $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
 $L1$ and $L2 =$ equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 $C_L =$ Fixture and stray capacitance ≤ 3 pF
 Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit



TL/F/9861-7

FIGURE 2. Enable Timing



TL/F/9861-8

Notes:
 t_s is the minimum time before the transition of the enable that information must be present at the designated input.
 t_h is the minimum time after the transition of the enable that information must remain unchanged at the designated input.

FIGURE 3. Data Setup and Hold Times

F100158 8-Bit Shift Matrix

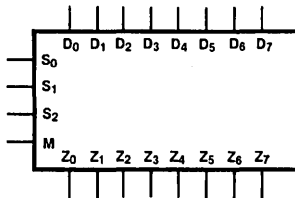
General Description

The F100158 contains a combinatorial network which performs the function of an 8-bit shift matrix. Three control lines (S_n) are internally decoded and define the number of places which an 8-bit word present at the inputs (D_n) is shifted to the left and presented at the outputs (Z_n). A Mode Control input (M) is provided which, if LOW, forces LOW all out-

puts to the right of the one that contains D_7 . This operation is sometimes referred to as *LOW backfill*. If M is HIGH, an end-around shift is performed such that D_0 appears at the output to the right of the one that contains D_7 . This operation is commonly referred to as *barrel shifting*. All inputs have 50 k Ω pull-down resistors.

Ordering Code: See Section 8

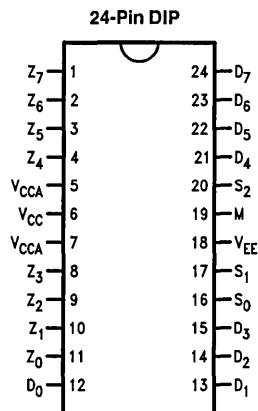
Logic Symbol



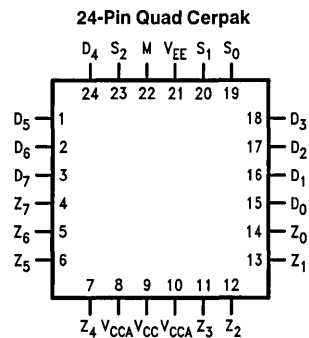
TL/F/9862-3

| Pin Names | Description |
|---------------|--------------------|
| D_0 - D_7 | Data Inputs |
| S_0 - S_2 | Select Inputs |
| M | Mode Control Input |
| Z_0 - Z_7 | Data Outputs |

Connection Diagrams

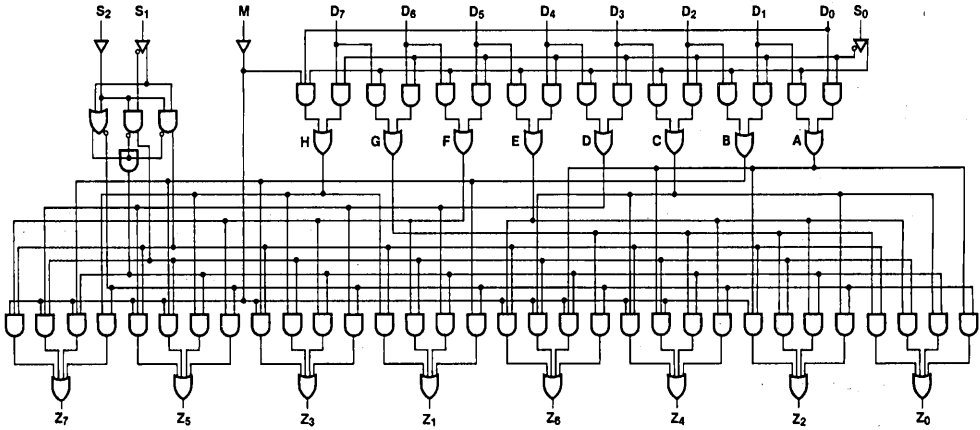


TL/F/9862-1



TL/F/9862-2

Logic Diagram



TL/F/9862-5

Truth Table

| Inputs | | | | Outputs | | | | | | | |
|--------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| M | S ₀ | S ₁ | S ₂ | Z ₀ | Z ₁ | Z ₂ | Z ₃ | Z ₄ | Z ₅ | Z ₆ | Z ₇ |
| X | L | L | L | D ₀ | D ₁ | D ₂ | D ₃ | D ₄ | D ₅ | D ₆ | D ₇ |
| L | H | L | L | D ₁ | D ₂ | D ₃ | D ₄ | D ₅ | D ₆ | D ₇ | L |
| L | L | H | L | D ₂ | D ₃ | D ₄ | D ₅ | D ₆ | D ₇ | L | L |
| L | H | H | L | D ₃ | D ₄ | D ₅ | D ₆ | D ₇ | L | L | L |
| L | L | L | H | D ₄ | D ₅ | D ₆ | D ₇ | L | L | L | L |
| L | H | L | H | D ₅ | D ₆ | D ₇ | L | L | L | L | L |
| L | L | H | H | D ₆ | D ₇ | L | L | L | L | L | L |
| L | H | H | H | D ₇ | L | L | L | L | L | L | L |
| H | H | L | L | D ₁ | D ₂ | D ₃ | D ₄ | D ₅ | D ₆ | D ₇ | D ₀ |
| H | L | H | L | D ₂ | D ₃ | D ₄ | D ₅ | D ₆ | D ₇ | D ₀ | D ₁ |
| H | H | H | L | D ₃ | D ₄ | D ₅ | D ₆ | D ₇ | D ₀ | D ₁ | D ₂ |
| H | L | L | H | D ₄ | D ₅ | D ₆ | D ₇ | D ₀ | D ₁ | D ₂ | D ₃ |
| H | H | L | H | D ₅ | D ₆ | D ₇ | D ₀ | D ₁ | D ₂ | D ₃ | D ₄ |
| H | L | H | H | D ₆ | D ₇ | D ₀ | D ₁ | D ₂ | D ₃ | D ₄ | D ₅ |
| H | H | H | H | D ₇ | D ₀ | D ₁ | D ₂ | D ₃ | D ₄ | D ₅ | D ₆ |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|---------|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

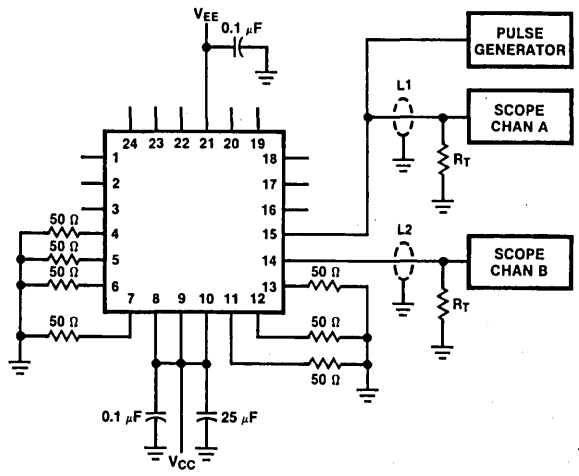
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------------------|------|------|-----|---------|-------------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 220 | μA | $V_{IN} = V_{IH}(\text{Max})$ |
| I_{EE} | Power Supply Current | -205 | -140 | -95 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 1.10 | 2.80 | 1.10 | 2.70 | 1.10 | 2.80 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay M to Output | 1.15 | 4.20 | 1.25 | 4.20 | 1.15 | 4.20 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay S_n to Output | 1.70 | 4.20 | 1.70 | 4.20 | 1.70 | 4.20 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.50 | 2.30 | 0.50 | 2.30 | 0.50 | 2.30 | ns | |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 1.10 | 2.60 | 1.10 | 2.50 | 1.10 | 2.60 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay M to Output | 1.15 | 4.00 | 1.25 | 4.00 | 1.15 | 4.00 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay S_n to Output | 1.70 | 4.00 | 1.70 | 4.00 | 1.70 | 4.00 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.50 | 2.20 | 0.50 | 2.20 | 0.50 | 2.20 | ns | |

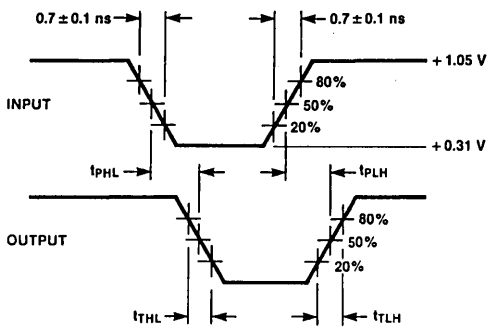


TL/F/9862-6

Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V.
- L1 and L2 = equal length 50Ω impedance lines.
- R_T = 50Ω terminator internal to scopes.
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
- All unused outputs are loaded with 50Ω to GND.
- C_L = fixture and stray capacitance ≤ 3 pF.
- Pin numbers shown are for flatpak; for DIP refer to logic symbol.

FIGURE 1. AC Test Circuit



TL/F/9862-7

FIGURE 2. Propagation Delay and Transition Times

Applications

The following technique uses two ranks of F100158s to shift a 64-bit word from 0 to 63 places. Although two stage delays are required (one for each rank), the total shift takes only about 4 ns. This technique performs a bit shift on each 8-bit byte in the first rank and then a modulo-8 byte shift on the 64-bit word in the second rank.

Basic 16-Bit 0-7 Place Shifter

Figure 3 shows the basic 0-7 place shift technique which can be expanded to accommodate any word length.

Each 8-bit byte requires a pair of F100158s operating in the LOW backfill mode. The address lines for each pair of ICs are driven out of phase by three OR gates. Inputs for the two ICs are taken from two bytes transposed in order; outputs are transposed and emitter-OR tied. One device shifts right from location 0 and the other shifts left from location 7. The bits shifted off one pair are picked up by the next pair of F100158s or—in the case of the last one in the rank—returned to the first device. The net result is a 0-7 place shift of the entire word.

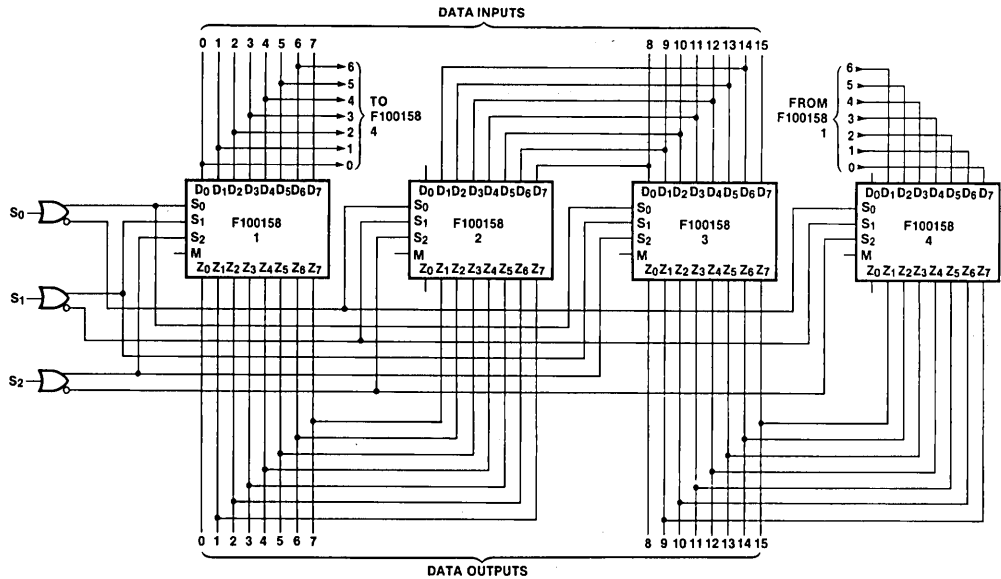


FIGURE 3. Basic 16-Bit 0-7 Place Shifter

TL/F/9862-8

Applications (Continued)

Expanding to 64-Bit Word and 64-Place Shift

The basic 0-7 place shift technique can be expanded to accommodate a 64-bit word shifted from 0 to 63 places, however, two ranks of F100158s are required (Figure 4). The first rank is identical to the one illustrated in Figure 3 except it contains a total of 16 devices. The second rank consists of eight additional F100158s connected in the modulo-8 configuration shown in Figure 5.

The modulo-8 rank is used to simulate an 8-bit simultaneous shift since the F100158 cannot shift in 8-bit jumps. The modulo-8 configuration is achieved by wiring the first rank and the output device to the second rank as illustrated in Figure 5. The LSB of each output byte in the first rank is wired to one of the eight inputs of the first F100158 in the

second rank. The next least significant bit of each first-rank F100158 pair, however, is connected to the inputs of the second F100158 in the second rank. The other first-ranked outputs are connected in a similar fashion to the remainder of the second-rank inputs. Ultimately, the outputs of the second rank must then be connected to reform the final usable 64-bit word so that the bits are again ordered from 0-63.

The effect is that each single-location shift in the second rank appears to be an eight place shift in the final word due to the way the inputs and outputs of the second rank are connected. The combination of the two ranks produces the 64-place shift of the entire word.

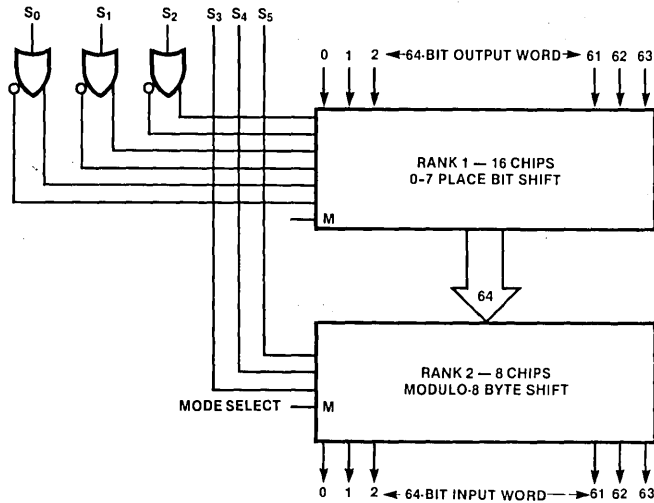


FIGURE 4. 64-Bit 0-63 Place Barrel Shifter

TL/F/9862-9

Applications (Continued)

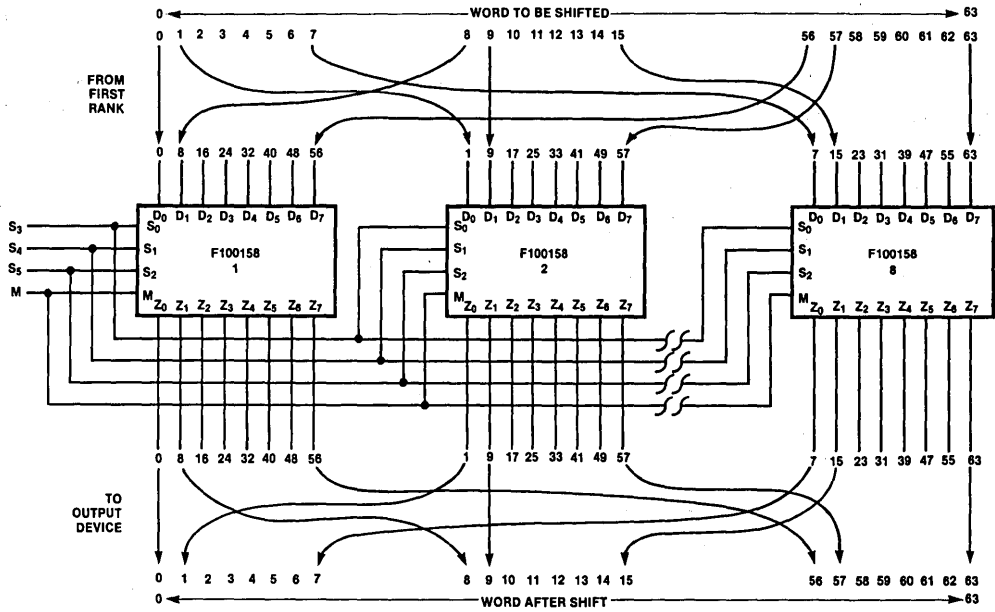


FIGURE 5. Modulo-8 Shift

TL/F/9862-10

F100160

Dual Parity Checker/Generator

General Description

The F100160 is a dual parity checker/generator. Each half has nine inputs; the output is HIGH when an even number of inputs are HIGH. One of the nine inputs (I_a or I_b) has the shorter through-put delay and is therefore preferred as the expansion input for generating parity for 16 or more bits.

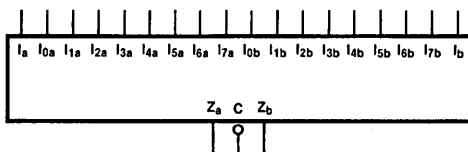
The F100160 also has a Compare (\bar{C}) output which allows the circuit to compare two 8-bit words. The \bar{C} output is LOW when the two words match, bit for bit. All inputs have 50 k Ω pulldown resistors.

Refer to the F100360 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

Logic Symbol

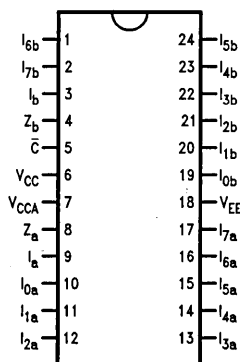


| Pin Names | Description |
|----------------------------|--------------------|
| I_a, I_b, I_{na}, I_{nb} | Data Inputs |
| Z_a, Z_b | Parity Odd Outputs |
| \bar{C} | Compare Output |

TL/F/9863-3

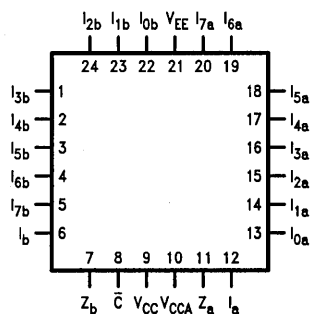
Connection Diagrams

24-Pin DIP



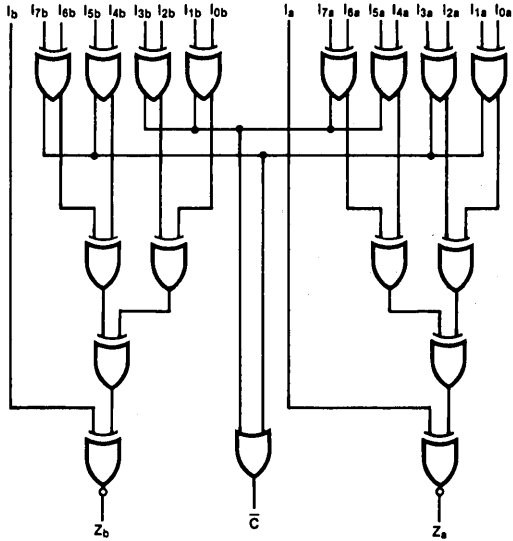
TL/F/9863-1

24-Pin Quad Cerpak



TL/F/9863-2

Logic Diagram



TL/F/9863-5

Truth Table (Each Half)

| Sum of HIGH Inputs | Output Z |
|--------------------|----------|
| Even | HIGH |
| Odd | LOW |

Comparator Function

$$\bar{C} = (I_{0a} \oplus I_{1a}) + (I_{2a} \oplus I_{3a}) + (I_{4a} \oplus I_{5a}) + (I_{6a} \oplus I_{7a}) + (I_{0b} \oplus I_{1b}) + (I_{2b} \oplus I_{3b}) + (I_{4b} \oplus I_{5b}) + (I_{6b} \oplus I_{7b})$$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature −65°C to +150°C
Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C) 0°C to +85°C
 V_{EE} Pin Potential to Ground Pin −7.0V to +0.5V
Input Voltage (DC) V_{EE} to +0.5V
Output Current (DC Output HIGH) −50 mA
Operating Range (Note 2) −5.7V to −4.2V

DC Electrical Characteristics

$V_{EE} = -4.5V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | −1025 | −955 | −880 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to −2.0V |
| V_{OL} | Output LOW Voltage | −1810 | −1705 | −1620 | | | |
| V_{OHC} | Output HIGH Voltage | −1035 | | | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to −2.0V |
| V_{OLC} | Output LOW Voltage | | | −1610 | | | |
| V_{IH} | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ | |

DC Electrical Characteristics

$V_{EE} = -4.2V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | −1020 | | −870 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to −2.0V |
| V_{OL} | Output LOW Voltage | −1810 | | −1605 | | | |
| V_{OHC} | Output HIGH Voltage | −1030 | | | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to −2.0V |
| V_{OLC} | Output LOW Voltage | | | −1595 | | | |
| V_{IH} | Input HIGH Voltage | −1150 | | −870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | −1810 | | −1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ | |

DC Electrical Characteristics

$V_{EE} = -4.8V$, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | −1035 | | −880 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ | Loading with 50Ω to −2.0V |
| V_{OL} | Output LOW Voltage | −1830 | | −1620 | | | |
| V_{OHC} | Output HIGH Voltage | −1045 | | | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ | Loading with 50Ω to −2.0V |
| V_{OLC} | Output LOW Voltage | | | −1610 | | | |
| V_{IH} | Input HIGH Voltage | −1165 | | −880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | −1830 | | −1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at −4.2V to −4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--|------|-----|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current I_a, I_b I_{na}, I_{nb} | | | 340 240 | μA | $V_{IN} = V_{IH (Max)}$ |
| I_{EE} | Power Supply Current | -115 | -82 | -57 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay I_{na}, I_{nb} to Z_a, Z_b | 1.30 | 4.30 | 1.30 | 4.10 | 1.30 | 4.30 | ns | <i>Figures 1 & 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay I_{na}, I_{nb} to \bar{C} | 1.20 | 3.30 | 1.20 | 3.10 | 1.20 | 3.30 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay I_a, I_b to Z_a, Z_b | 0.50 | 1.60 | 0.50 | 1.50 | 0.50 | 1.60 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.50 | 0.45 | 1.60 | ns | |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay I_{na}, I_{nb} to Z_a, Z_b | 1.30 | 4.10 | 1.30 | 3.90 | 1.30 | 4.10 | ns | <i>Figures 1 & 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay I_{na}, I_{nb} to \bar{C} | 1.20 | 3.10 | 1.20 | 2.90 | 1.20 | 3.10 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay I_a, I_b to Z_a, Z_b | 0.50 | 1.40 | 0.50 | 1.30 | 0.50 | 1.40 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | |

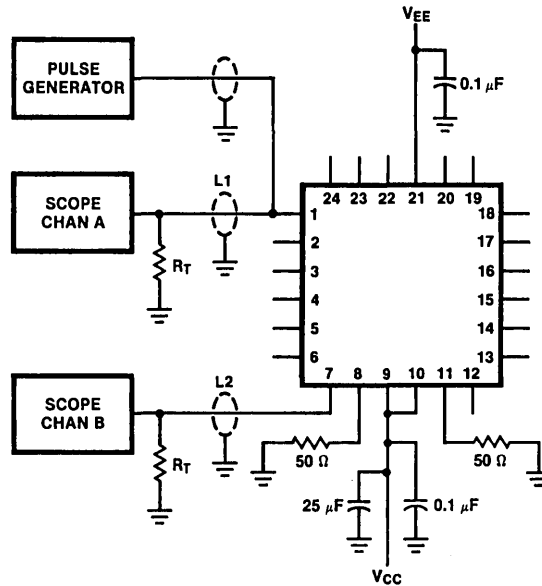


FIGURE 1. AC Test Circuit

TL/F/9863-6

Notes: $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$ L1 and L2 = equal length 50 Ω impedance lines $R_T = 50\Omega$ terminator internal to scopeDecoupling 0.1 μF from GND to V_{CC} and V_{EE} All unused outputs are loaded with 50 Ω to GND C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol

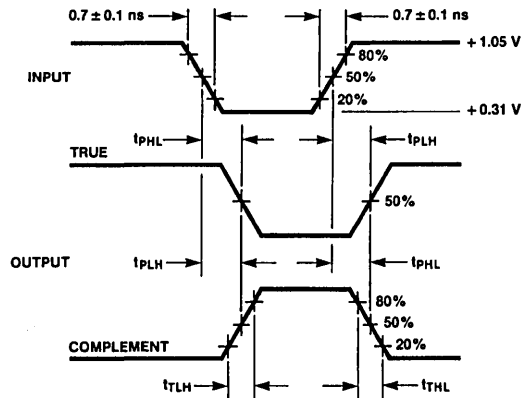


FIGURE 2. Propagation Delay and Transition Times

TL/F/9863-7



F100163 Dual 8-Input Multiplexer

General Description

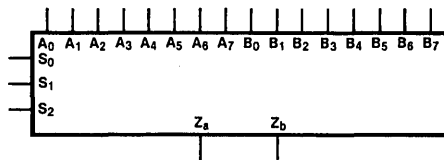
The F100163 is a dual 8-input multiplexer. The Data Select (S_n) inputs determine which bit (A_n and B_n) will be presented at the outputs (Z_a and Z_b respectively). The same bit (0-7) will be selected for both the Z_a and Z_b output. All inputs have 50 k Ω pulldown resistors.

Refer to the F100363 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs ($-4.2V$ to $-5.7V$)

Ordering Code: See Section 8

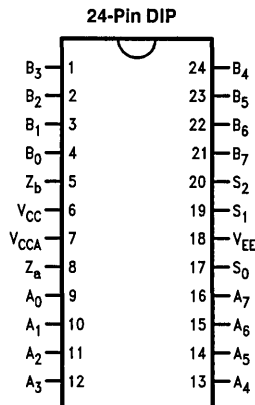
Logic Symbol



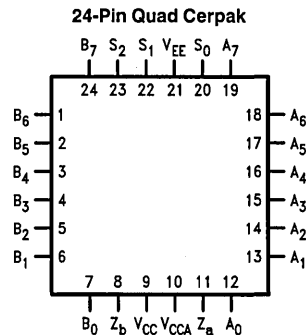
TL/F/9864-3

| Pin Names | Description |
|---------------|--------------------|
| S_0 - S_2 | Data Select Inputs |
| A_0 - A_7 | A Data Inputs |
| B_0 - B_7 | B Data Inputs |
| Z_a , Z_b | Data Outputs |

Connection Diagrams

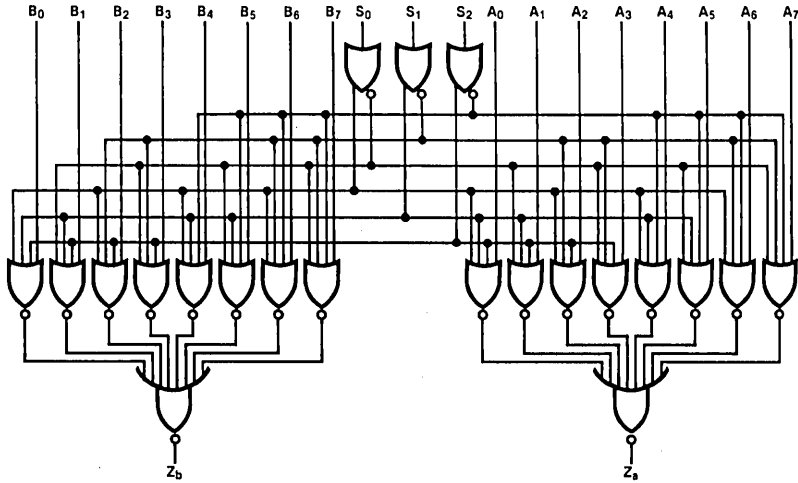


TL/F/9864-1



TL/F/9864-2

Logic Diagram



TL/F/9864-5

Truth Table

| Select | | | Data | | | | | | | | Outputs | |
|----------------|----------------|----------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|--|
| S ₂ | S ₁ | S ₀ | A ₇ B ₇ | A ₆ B ₆ | A ₅ B ₅ | A ₄ B ₄ | A ₃ B ₃ | A ₂ B ₂ | A ₁ B ₁ | A ₀ B ₀ | Z _a Z _b | |
| L | L | L | | | | | | | | L | L | |
| L | L | L | | | | | | | | H | H | |
| L | L | H | | | | | | | L | | L | |
| L | L | H | | | | | | H | | | H | |
| L | H | L | | | | | | L | | | L | |
| L | H | L | | | | | L | | | | H | |
| L | H | H | | | | | H | | | | L | |
| L | H | H | | | | | | H | | | H | |
| H | L | L | | | | L | | | | | L | |
| H | L | L | | | L | | | | | | H | |
| H | L | H | | | H | | | | | | L | |
| H | L | H | | L | | | | | | | H | |
| H | H | L | | L | | | | | | | L | |
| H | H | L | | H | | | | | | | H | |
| H | H | H | L | | | | | | | | L | |
| H | H | H | H | | | | | | | | H | |

H = HIGH Voltage Level
 L = LOW Voltage Level
 Blank = X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Maximum Junction Temperature (T_j) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{EE} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|-------|--|---------------------------------------|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current S_n A_n, B_n | | | 265 340 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -153 | -110 | -76 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_0-A_7, B_0-B_7 to Output | 0.55 | 1.65 | 0.60 | 1.70 | 0.65 | 1.80 | ns | <i>Figures 1 & 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay S_0-S_2 to Output | 1.10 | 2.80 | 1.10 | 2.80 | 1.20 | 3.10 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.50 | 1.85 | 0.55 | 1.80 | 0.50 | 1.80 | ns | |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|--------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_0-A_7, B_0-B_7 to Output | 0.55 | 1.45 | 0.60 | 1.50 | 0.65 | 1.60 | ns | <i>Figures 1 & 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay S_0-S_2 to Output | 1.10 | 2.60 | 1.10 | 2.60 | 1.20 | 2.90 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.50 | 1.75 | 0.55 | 1.70 | 0.50 | 1.70 | ns | |

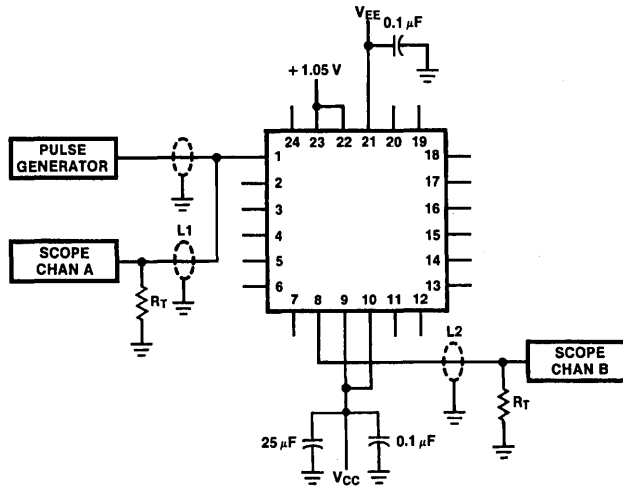


FIGURE 1. AC Test Circuit

TL/F/9864-6

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling $0.1\ \mu F$ from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- $C_L =$ Fixture and stray capacitance $\leq 3\ pF$
- Pin numbers shown are for flatpak; for DIP see logic symbol

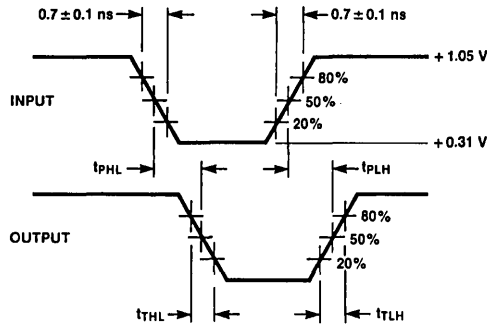


FIGURE 2. Propagation Delay and Transition Times

TL/F/9864-7

F100164

16-Input Multiplexer

General Description

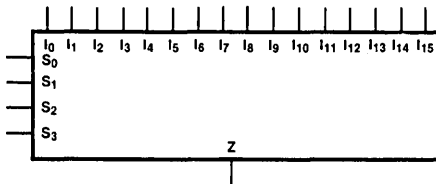
The F100164 is a 16-input multiplexer. Data paths are controlled by four Select lines (S_0 – S_3). Their decoding is shown in the truth table. Output data polarity is the same as the selected input data. All inputs have 50 k Ω pulldown resistors.

Refer to the F100364 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (–4.2V to –5.7V)

Ordering Code: See Section 8

Logic Symbol

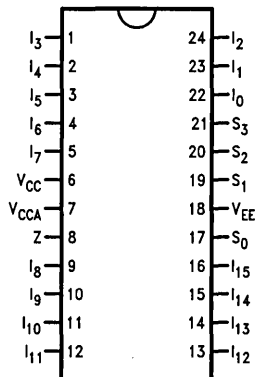


TL/F/9865-3

| Pin Names | Description |
|------------------|---------------|
| I_0 – I_{15} | Data Inputs |
| S_0 – S_3 | Select Inputs |
| Z | Data Output |

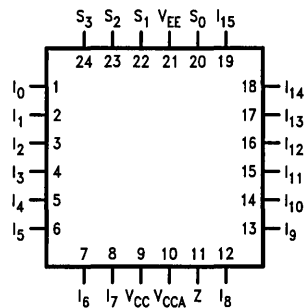
Connection Diagrams

24-Pin DIP



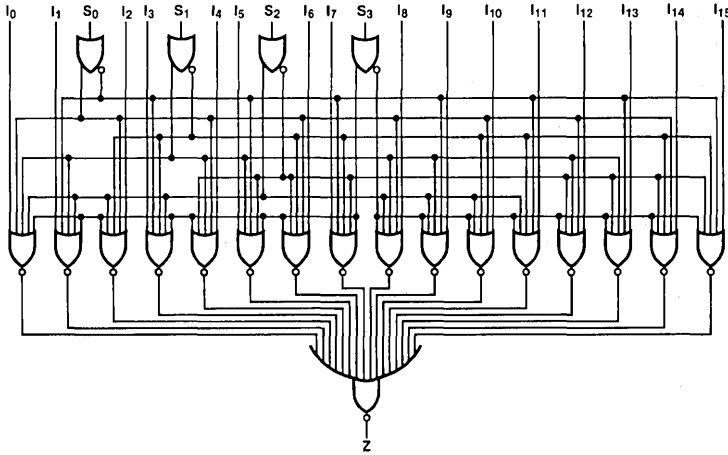
TL/F/9865-1

24-Pin Quad Cerpak



TL/F/9865-2

Logic Diagram



TL/F/9865-5

Truth Table

| Select Inputs | | | | Output |
|----------------|----------------|----------------|----------------|-----------------|
| S ₀ | S ₁ | S ₂ | S ₃ | Z |
| L | L | L | L | I ₀ |
| H | L | L | L | I ₁ |
| L | H | L | L | I ₂ |
| H | H | L | L | I ₃ |
| L | L | H | L | I ₄ |
| H | L | H | L | I ₅ |
| L | H | H | L | I ₆ |
| H | H | H | L | I ₇ |
| L | L | L | H | I ₈ |
| H | L | L | H | I ₉ |
| L | H | L | H | I ₁₀ |
| H | H | L | H | I ₁₁ |
| L | L | H | H | I ₁₂ |
| H | L | H | H | I ₁₃ |
| L | H | H | H | I ₁₄ |
| H | H | H | H | I ₁₅ |

H = HIGH Voltage Level
 L = LOW Voltage Level

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--|------|-----|-------------------|---------|-------------------------|
| I_{IH} | Input HIGH Current I_{in} S_0, S_1 S_2, S_3 | | | 280 240 200 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -105 | -70 | -49 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay I_0-I_{15} to Output | 0.80 | 2.20 | 0.90 | 2.35 | 0.90 | 2.55 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay S_0, S_1 to Output | 1.45 | 3.10 | 1.45 | 3.20 | 1.55 | 3.60 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay S_2, S_3 to Output | 1.10 | 2.45 | 1.10 | 2.50 | 1.20 | 2.80 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay I_0-I_{15} to Output | 0.80 | 2.00 | 0.90 | 2.15 | 0.90 | 2.35 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay S_0, S_1 to Output | 1.45 | 2.90 | 1.45 | 3.00 | 1.55 | 3.40 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay S_2, S_3 to Output | 1.10 | 2.25 | 1.10 | 2.30 | 1.20 | 2.60 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

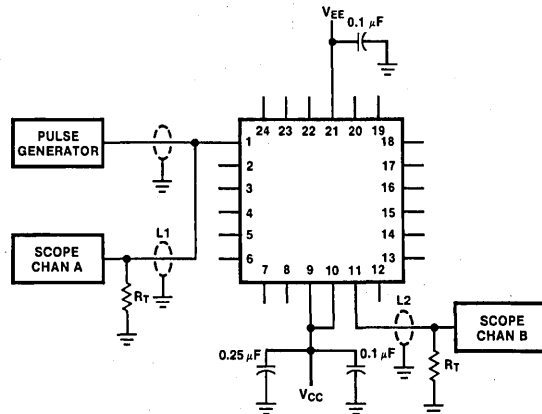
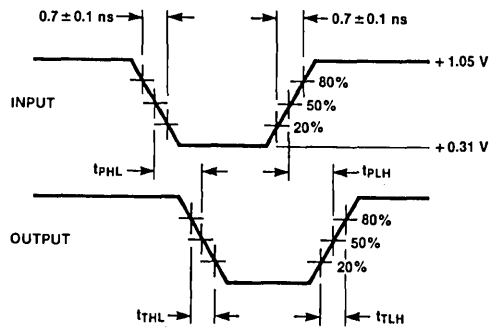


FIGURE 1. AC Test Circuit

TL/F/9865-6



TL/F/9865-7

FIGURE 2. Propagation Delay and Transition Times

Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

L1 and L2 = equal length 50 Ω impedance lines

$R_T = 50\Omega$ terminator internal to scope

Decoupling 0.1 μ F from GND to V_{CC} and V_{EE}

All unused outputs are loaded with 50 Ω to GND

C_L = Fixture and stray capacitance ≤ 3 pF

Pin numbers shown are for flatpak; for DIP see logic symbol



F100165 Universal Priority Encoder

General Description

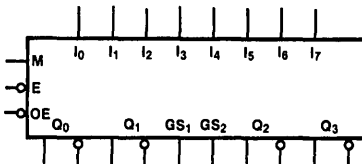
The F100165 contains eight input latches with a common Enable (\bar{E}) followed by encoding logic which generates the binary address of the highest priority input having a HIGH signal. The circuit operates as a dual 4-input encoder when the Mode Control (M) input is LOW, and as a single 8-input encoder when M is HIGH. In the 8-input mode, Q_0 , Q_1 and Q_2 are the relevant outputs, I_0 is the highest priority input and GS_1 is the relevant Group Signal output. In the dual mode, Q_0 , Q_1 and GS_1 operate with I_0 – I_3 , Q_2 , Q_3 and GS_2

operate with I_4 – I_7 . A GS output goes LOW when its pertinent inputs are all LOW.

Inputs are latched when \bar{E} goes HIGH. A HIGH signal on the Output Enable (\bar{OE}) input forces all Q outputs LOW and GS outputs HIGH. Expansion to accommodate more inputs can be done by connecting the GS output of a higher priority group to the \bar{OE} input of the next lower priority group. All inputs have 50 k Ω pulldown resistors.

Ordering Code: See Section 8

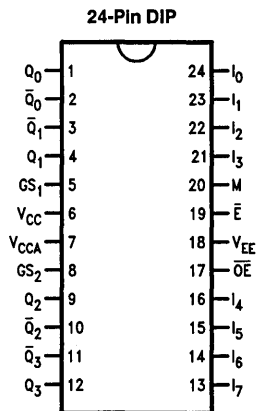
Logic Symbol



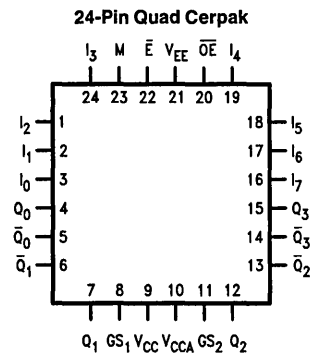
TL/F/9866-3

| Pin Names | Description |
|---------------------------|----------------------------------|
| I_0 – I_7 | Data Inputs |
| \bar{E} | Enable Input (Active LOW) |
| \bar{OE} | Output Enable Input (Active LOW) |
| M | Mode Control Input |
| GS_1 – GS_2 | Group Signal Outputs |
| Q_0 – Q_3 | Data Outputs |
| \bar{Q}_0 – \bar{Q}_3 | Complementary Data Outputs |

Connection Diagrams



TL/F/9866-1



TL/F/9866-2

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------------------|------|------|-----|---------|-------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 230 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -200 | -140 | -77 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Condition |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|--------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay I_0-I_7 to $Q_0-Q_3, \bar{Q}_0-\bar{Q}_3$ (Transparent Mode) | 1.10 | 4.10 | 1.10 | 4.10 | 1.10 | 4.60 | ns | Figures 1 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay I_0-I_7 to GS_1-GS_2 (Transparent Mode) | 1.30 | 3.90 | 1.30 | 3.90 | 1.30 | 4.20 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{OE} to $Q_0-Q_3, \bar{Q}_0-\bar{Q}_3$ | 1.00 | 3.00 | 1.00 | 3.00 | 1.10 | 3.30 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{OE} to GS_1-GS_2 | 1.10 | 2.60 | 1.10 | 2.60 | 1.20 | 2.80 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay M to $Q_0-Q_3, \bar{Q}_0-\bar{Q}_3$ | 0.90 | 3.60 | 1.00 | 3.60 | 1.00 | 3.80 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to $Q_0-Q_3, \bar{Q}_0-\bar{Q}_3$ | 1.50 | 4.70 | 1.50 | 4.60 | 1.50 | 5.00 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.40 | 0.45 | 1.50 | ns | Figures 1, 2 and 3 |
| t_s | Setup Time I_0-I_7 | 1.00 | | 0.90 | | 1.00 | | ns | Figure 4 |
| t_H | Hold Time I_0-I_7 | 1.20 | | 1.20 | | 1.20 | | ns | |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E} | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|--------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay I_0-I_7 to $Q_0-Q_3, \bar{Q}_0-\bar{Q}_3$ (Transparent Mode) | 1.10 | 3.90 | 1.10 | 3.90 | 1.10 | 4.40 | ns | Figures 1 and 3 |
| t_{PLH} t_{PHL} | Propagation Delay I_0-I_7 to GS_1-GS_2 (Transparent Mode) | 1.30 | 3.70 | 1.30 | 3.70 | 1.30 | 4.00 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{OE} to $Q_0-Q_3, \bar{Q}_0-\bar{Q}_3$ | 1.00 | 2.80 | 1.00 | 2.80 | 1.10 | 3.10 | ns | Figures 1 and 2 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{OE} to GS_1-GS_2 | 1.10 | 2.40 | 1.10 | 2.40 | 1.20 | 2.60 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay M to $Q_0-Q_3, \bar{Q}_0-\bar{Q}_3$ | 0.90 | 3.40 | 1.00 | 3.40 | 1.00 | 3.60 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to $Q_0-Q_3, \bar{Q}_0-\bar{Q}_3$ | 1.50 | 4.50 | 1.50 | 4.40 | 1.50 | 4.80 | ns | Figures 1 and 3 |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.40 | 0.45 | 1.30 | 0.45 | 1.40 | ns | Figures 1, 2 and 3 |
| t_s | Setup Time I_0-I_7 | 0.90 | | 0.80 | | 0.90 | | ns | Figure 4 |
| t_H | Hold Time I_0-I_7 | 1.10 | | 1.10 | | 1.10 | | ns | |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E} | 2.00 | | 2.00 | | 2.00 | | ns | Figure 3 |

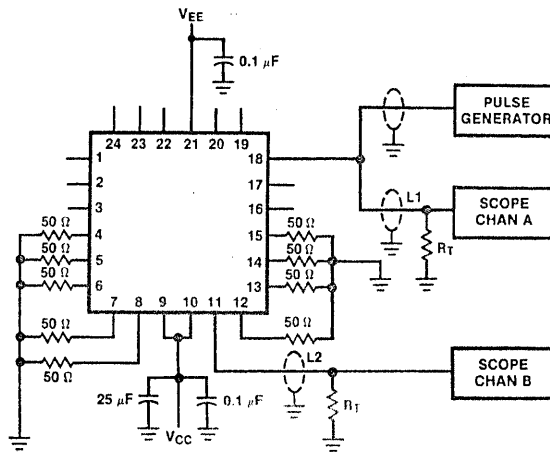
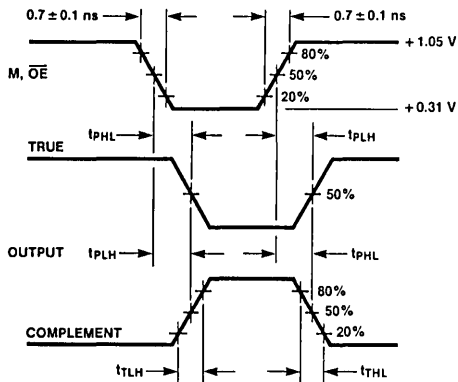


FIGURE 1. AC Test Circuit

FL/F/8806-6

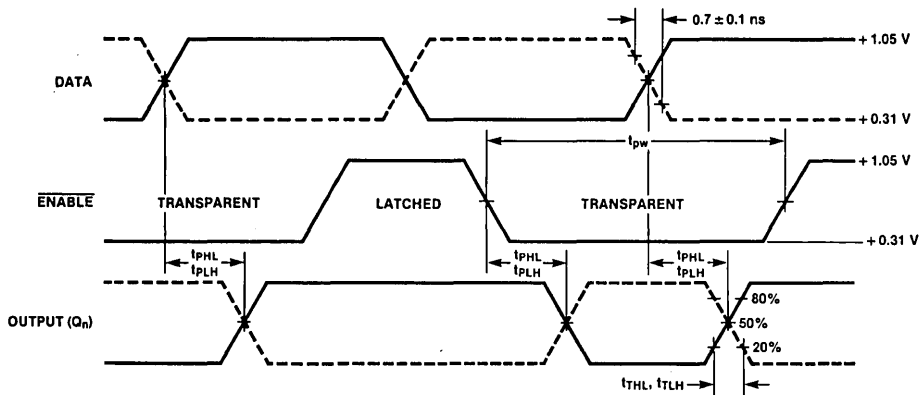


TL/F/9866-7

FIGURE 2. Propagation Delay (M, \overline{OE}) and Transition Times

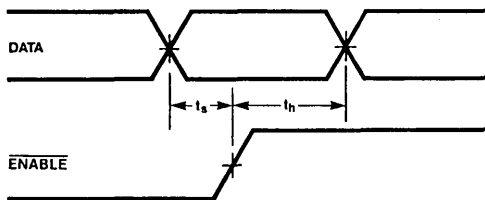
Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- $C_L =$ Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/9866-8

FIGURE 3. Enable Timing



TL/F/9866-9

FIGURE 4. Setup and Hold Times

Notes:

- t_s is the minimum time before the transition of the enable that information must be present at the data input.
- t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.



F100166 9-Bit Comparator

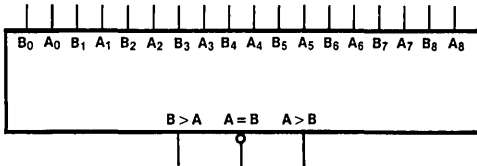
General Description

The F100166 is a 9-bit magnitude comparator which compares the arithmetic value of two 9-bit words and indicates whether one word is greater than, or equal to, the other.

Other functions can be generated by the wire-OR of the outputs. All inputs have 50 k Ω pulldown resistors.

Ordering Code: See Section 8

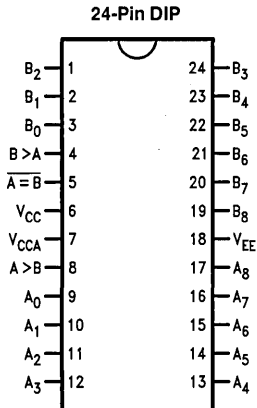
Logic Symbol



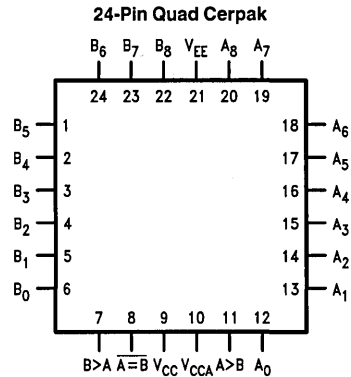
TL/F/9867-3

| Pin Names | Description |
|--------------------------------|---|
| A ₀ -A ₈ | A Data Inputs |
| B ₀ -B ₈ | B Data Inputs |
| A > B | A Greater than B Output |
| B > A | B Greater than A Output |
| $\overline{A = B}$ | Complement A Equal to B Output (Active LOW) |

Connection Diagrams

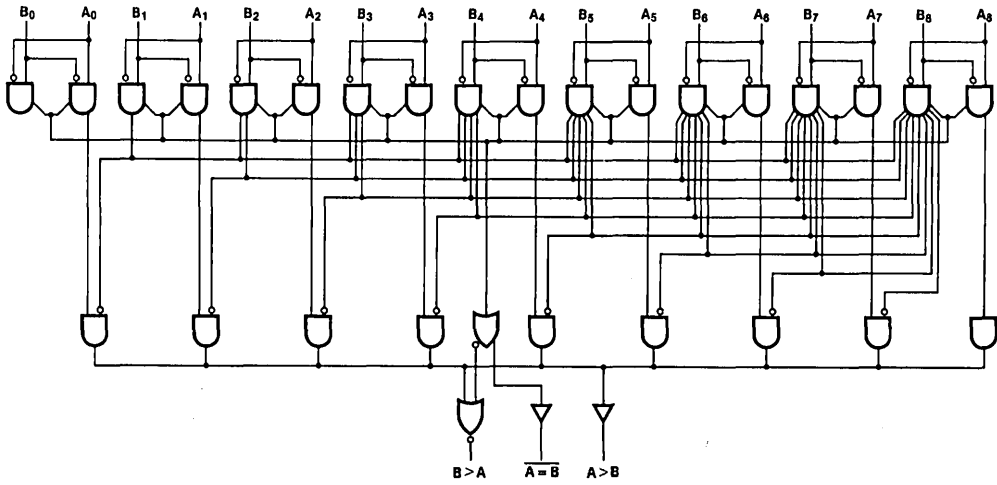


TL/F/9867-1



TL/F/9867-2

Logic Diagram



TL/F/9867-5

Truth Table

| Inputs | | | | | | | | | Outputs | | |
|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------|-------|-------|
| A ₈ B ₈ | A ₇ B ₇ | A ₆ B ₆ | A ₅ B ₅ | A ₄ B ₄ | A ₃ B ₃ | A ₂ B ₂ | A ₁ B ₁ | A ₀ B ₀ | A > B | B > A | A = B |
| H L | | | | | | | | | H | L | H |
| L H | | | | | | | | | L | H | H |
| A ₈ = B ₈ | H L | | | | | | | | H | L | H |
| A ₈ = B ₈ | L H | | | | | | | | L | H | H |
| A ₈ = B ₈ | A ₇ = B ₇ | H L | | | | | | | H | L | H |
| A ₈ = B ₈ | A ₇ = B ₇ | L H | | | | | | | L | H | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | H L | | | | | | H | L | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | L H | | | | | | L | H | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | H L | | | | | H | L | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | L H | | | | | L | H | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | H L | | | | H | L | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | L H | | | | L | H | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | A ₃ = B ₃ | H L | | | H | L | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | A ₃ = B ₃ | L H | | | L | H | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | A ₃ = B ₃ | A ₂ = B ₂ | H L | | H | L | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | A ₃ = B ₃ | A ₂ = B ₂ | L H | | L | H | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | A ₃ = B ₃ | A ₂ = B ₂ | A ₁ = B ₁ | H L | H | L | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | A ₃ = B ₃ | A ₂ = B ₂ | A ₁ = B ₁ | L H | L | H | H |
| A ₈ = B ₈ | A ₇ = B ₇ | A ₆ = B ₆ | A ₅ = B ₅ | A ₄ = B ₄ | A ₃ = B ₃ | A ₂ = B ₂ | A ₁ = B ₁ | A ₀ = B ₀ | L | L | L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 Blank = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.0V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------------------|------|------|------|---------|-------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 250 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -238 | -170 | -119 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 1.40 | 3.50 | 1.40 | 3.50 | 1.40 | 3.90 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.55 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay Data to Output | 1.40 | 3.30 | 1.40 | 3.30 | 1.40 | 3.70 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.45 | 0.45 | 1.40 | 0.45 | 1.40 | ns | |

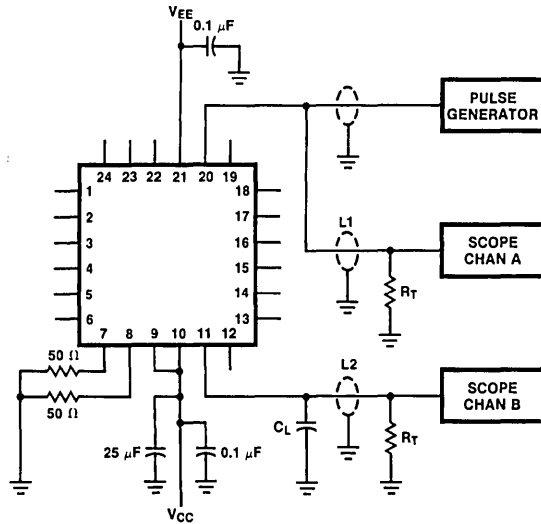
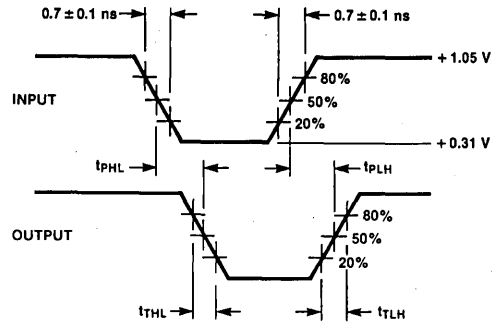


FIGURE 1. AC Test Circuit

TL/F/9867-6

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- $C_L =$ Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/9867-7

FIGURE 2. Propagation Delay and Transition Times

F100170 Universal Demultiplexer/Decoder

General Description

The F100170 universal demultiplexer/decoder functions as either a dual 1-of-4 decoder or as a single 1-of-8 decoder, depending on the signal applied to the Mode Control (M) input. In the dual mode, each half has a pair of active-LOW Enable (\bar{E}) inputs. Pin assignments for the \bar{E} inputs are such that in the 1-of-8 mode they can easily be tied together in pairs to provide two active-LOW enables (\bar{E}_{1a} to \bar{E}_{1b} , \bar{E}_{2a} to \bar{E}_{2b}). Signals applied to auxiliary inputs H_a , H_b and H_c determine whether the outputs are active HIGH or active LOW. In the dual 1-of-4 mode the Address inputs are A_{0a} , A_{1a} and

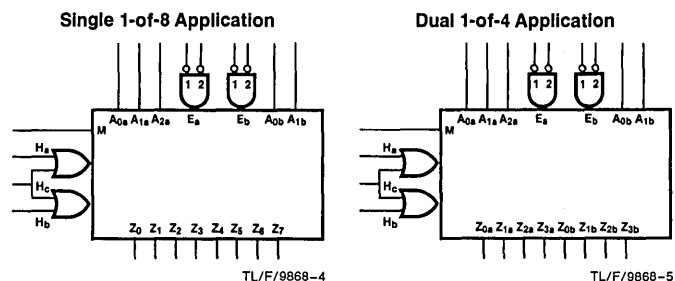
A_{0b} , A_{1b} with A_{2a} unused (i.e., left open, tied to V_{EE} or with LOW signal applied). In the 1-of-8 mode, the Address inputs are A_{0a} , A_{1a} , A_{2a} with A_{0b} and A_{1b} LOW or open. All inputs have 50 k Ω pulldown resistors.

Refer to the F100370 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs (-4.2V to -5.7V)

Ordering Code: See Section 8

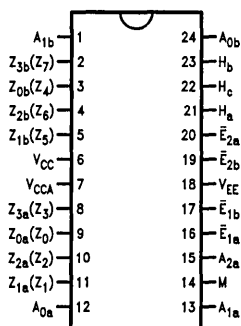
Logic Symbols



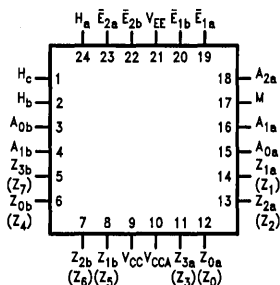
| Pin Names | Description |
|---------------------------------|--|
| A_{na} , A_{nb} | Address Inputs |
| \bar{E}_{na} , \bar{E}_{nb} | Enable Inputs |
| M | Mode Control Input |
| H_a | Z_0-Z_3 ($\bar{Z}_{0a}-\bar{Z}_{3a}$) Polarity Select Input |
| H_b | Z_4-Z_7 ($\bar{Z}_{0b}-\bar{Z}_{3b}$) Polarity Select Input |
| H_c | Common Polarity Select Input |
| Z_0-Z_7 | Single 1-of-8 Data Outputs |
| Z_{na} , Z_{nb} | Dual 1-of-4 Data Outputs |

Connection Diagrams

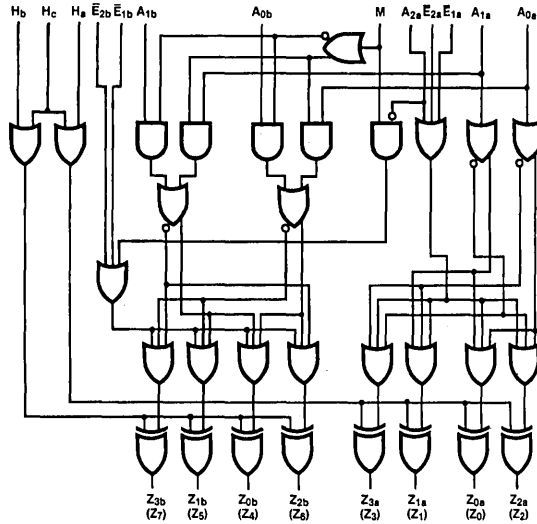
24-Pin DIP



24-Pin Quad Cerpak



Logic Diagram



TL/F/9868-6

Note: (Z_n) for 1-of-4 applications.

Truth Tables

Dual 1-of-4 Mode (M = A_{2a} = H_c = LOW)

| Inputs | | | Active HIGH Outputs (H _a and H _b Inputs HIGH) | | | | | Active LOW Outputs (H _a and H _b Inputs LOW) | | | |
|----------------------------------|----------------------------------|------------------------------------|--|------------------------------------|------------------------------------|------------------------------------|------------------------------------|--|------------------------------------|------------------------------------|------------------------------------|
| \bar{E}_{1a} \bar{E}_{1b} | \bar{E}_{2a} \bar{E}_{2b} | A _{1a} A _{1b} | A _{0a} A _{0b} | Z _{0a} Z _{0b} | Z _{1a} Z _{1b} | Z _{2a} Z _{2b} | Z _{3a} Z _{3b} | Z _{0a} Z _{0b} | Z _{1a} Z _{1b} | Z _{2a} Z _{2b} | Z _{3a} Z _{3b} |
| H | X | X | X | L | L | L | L | H | H | H | H |
| X | H | X | X | L | L | L | L | H | H | H | H |
| L | L | L | L | H | L | L | L | L | H | H | H |
| L | L | L | H | L | H | L | L | H | L | H | H |
| L | L | H | L | L | L | H | L | H | H | L | H |
| L | L | H | H | L | L | L | H | H | H | H | L |

Single 1-of-8 Mode (M = HIGH; A_{0b} = A_{1b} = H_a = H_b = LOW)

| Inputs | | | | | Active HIGH Outputs* (H _c Input HIGH) | | | | | | | |
|-------------|-------------|-----------------|-----------------|-----------------|---|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| \bar{E}_1 | \bar{E}_2 | A _{2a} | A _{1a} | A _{0a} | Z ₀ | Z ₁ | Z ₂ | Z ₃ | Z ₄ | Z ₅ | Z ₆ | Z ₇ |
| H | X | X | X | X | L | L | L | L | L | L | L | L |
| X | H | X | X | X | L | L | L | L | L | L | L | L |
| L | L | L | L | L | H | L | L | L | L | L | L | L |
| L | L | L | L | H | L | H | L | L | L | L | L | L |
| L | L | L | H | L | L | L | H | L | L | L | L | L |
| L | L | L | H | H | L | L | L | H | L | L | L | L |
| L | L | H | L | L | L | L | L | L | H | L | L | L |
| L | L | H | L | H | L | L | L | L | L | H | L | L |
| L | L | H | H | L | L | L | L | L | L | L | H | L |
| L | L | H | H | H | L | L | L | L | L | L | L | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

*for H_c = LOW, output states are complemented
 $\bar{E}_1 = \bar{E}_{1a}$ and \bar{E}_{1b} wired; $\bar{E}_2 = \bar{E}_{2a}$ and \bar{E}_{2b} wired

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

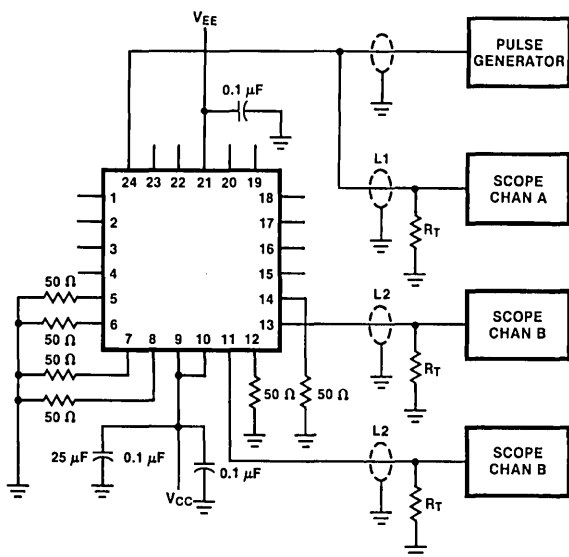
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|------------|---------|------------------------|
| I_{IH} | Input HIGH Current $H_C, A_{0a}, A_{1a}, A_{2a}$ All Others | | | 310 250 | μA | $V_{IN} = V_{IH(Max)}$ |
| I_{EE} | Power Supply Current | -153 | -109 | -76 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay E_{na}, E_{nb} to Output | 0.90 | 2.30 | 0.90 | 2.20 | 0.90 | 2.30 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay A_{na}, A_{nb} to Output | 1.00 | 2.80 | 1.00 | 2.70 | 1.00 | 2.90 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay H_a, H_b, H_c to Output | 1.00 | 3.00 | 1.00 | 2.90 | 1.00 | 3.00 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay M to Output | 1.50 | 3.90 | 1.60 | 3.80 | 1.60 | 3.90 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.80 | ns | |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay E_{na}, E_{nb} to Output | 0.90 | 2.10 | 0.90 | 2.00 | 0.90 | 2.10 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay A_{na}, A_{nb} to Output | 1.00 | 2.60 | 1.00 | 2.50 | 1.00 | 2.70 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay H_a, H_b, H_c to Output | 1.00 | 2.80 | 1.00 | 2.70 | 1.00 | 2.80 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay M to Output | 1.50 | 3.70 | 1.60 | 3.60 | 1.60 | 3.70 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.70 | ns | |

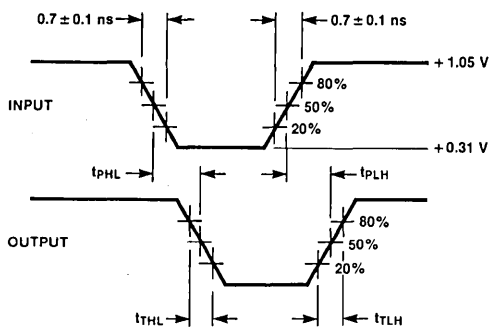


TL/F/9868-7

FIGURE 1. AC Test Circuit

Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol



TL/F/9868-8

FIGURE 2. Propagation Delay and Transition Times



F100171

Triple 4-Input Multiplexer with Enable

General Description

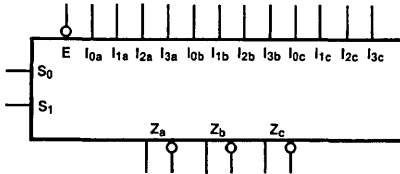
The F100171 contains three 4-input multiplexers which share a common decoder (inputs S_0 and S_1). Output buffer gates provide true and complement outputs. A HIGH on the Enable input (\bar{E}) forces all true outputs LOW (see Truth Table). All inputs have 50 k Ω pull-down resistors.

Refer to the F100371 datasheet for:

- PCC packaging
- Lower power
- Military versions
- Extended voltage specs ($-4.2V$ to $-5.7V$)

Ordering Code: See Section 8

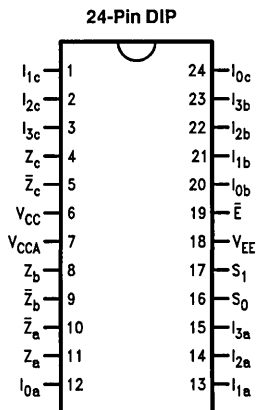
Logic Symbol



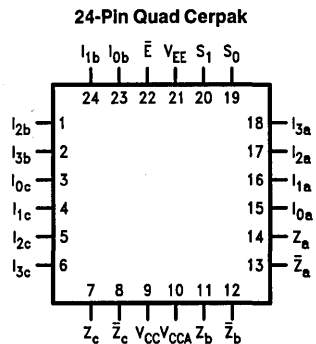
TL/F/9869-3

| Pin Names | Description |
|-----------------------|----------------------------|
| $I_{0x}-I_{3x}$ | Data Inputs |
| S_0, S_1 | Select Inputs |
| \bar{E} | Enable Input (Active LOW) |
| Z_a-Z_c | Data Outputs |
| $\bar{Z}_a-\bar{Z}_c$ | Complementary Data Outputs |

Connection Diagrams

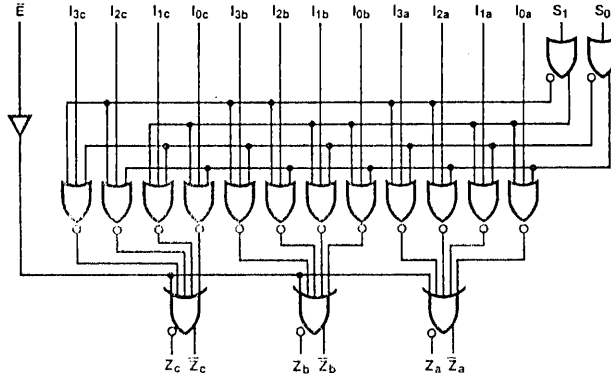


TL/F/9869-1



TL/F/9869-2

Logic Diagram



TL/F/9869-5

Truth Table

| Inputs | | | Outputs |
|-----------|-------|-------|----------|
| \bar{E} | S_0 | S_1 | Z_n |
| L | L | L | I_{0x} |
| L | H | L | I_{1x} |
| L | L | H | I_{2x} |
| L | H | H | I_{3x} |
| H | X | X | L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

| | |
|---------------------------------------|--|
| Case Temperature under Bias (T_C) | 0°C to $+85^{\circ}\text{C}$ |
| V_{EE} Pin Potential to Ground Pin | -7.0V to $+0.5\text{V}$ |
| Input Voltage (DC) | V_{EE} to $+0.5\text{V}$ |
| Output Current (DC Output HIGH) | -50mA |
| Operating Range (Note 2) | -5.7V to -4.2V |

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|---------|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--|------|-----|------------|---------|------------------------|
| I_{IH} | Input HIGH Current $I_{0x}-I_{3x}$ S_0, S_1, \bar{E} | | | 340 300 | μA | $V_{IN} = V_{IH(max)}$ |
| I_{EE} | Power Supply Current | -114 | -80 | -56 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $I_{0x}-I_{3x}$ to Output | 0.45 | 1.70 | 0.45 | 1.60 | 0.50 | 1.70 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay S_0, S_1 to Output | 0.90 | 2.40 | 0.90 | 2.60 | 1.00 | 3.00 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to Output | 0.65 | 2.40 | 0.65 | 2.30 | 0.75 | 2.40 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.60 | 0.45 | 1.60 | ns | |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $I_{0x}-I_{3x}$ to Output | 0.45 | 1.50 | 0.45 | 1.40 | 0.50 | 1.50 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay S_0, S_1 to Output | 0.90 | 2.20 | 0.90 | 2.40 | 1.00 | 2.80 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to Output | 0.65 | 2.20 | 0.65 | 2.10 | 0.75 | 2.20 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.50 | 0.45 | 1.50 | ns | |

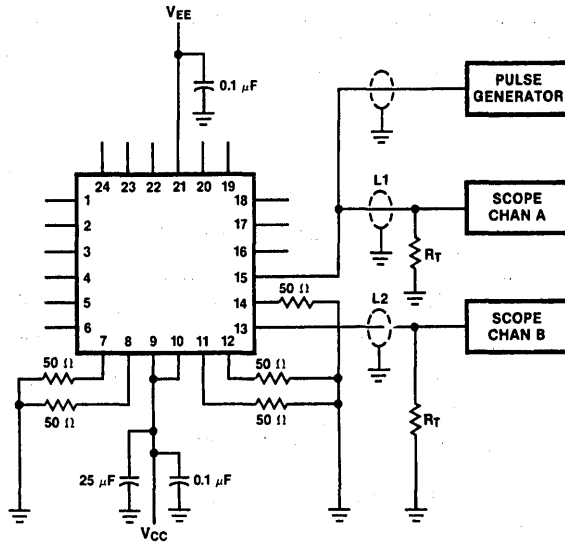


FIGURE 1. AC Test Circuit

TL/F/9869-6

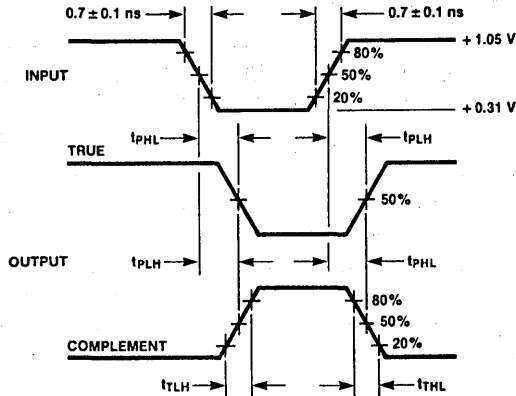


FIGURE 2. Propagation Delay and Transition Times

TL/F/9869-7

Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

F100175

Quint Latch 100K In/10K Out

General Description

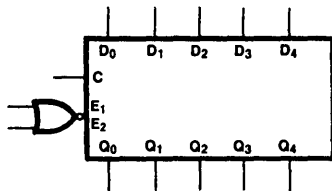
The F100175 is a 5-bit latch with temperature and voltage compensated 100K compatible inputs and voltage compensated 10K compatible outputs. Each latch has one data input and one output. All five latches share a common clear input and one output. All inputs have 50 k Ω pull-down resistors.

Features

- Outputs specified to drive a 50 Ω load
- Available in 16-pin ceramic DIP
- 100K compatible inputs/10K compatible outputs

Ordering Code: See Section 8

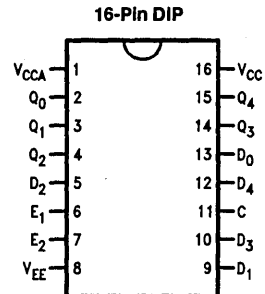
Logic Symbol



TL/F/9870-2

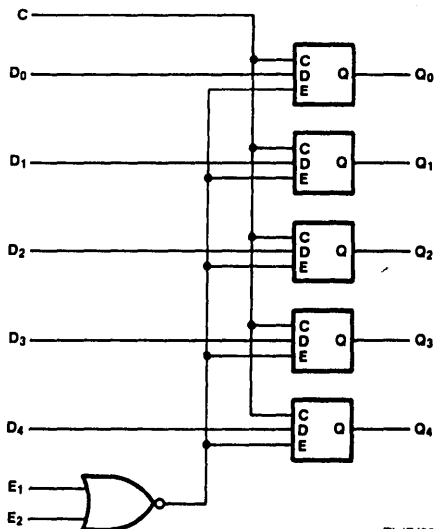
| Pin Names | Description |
|---------------------------------|-------------------------|
| D ₀ -D ₄ | 100K Data Inputs |
| E ₁ , E ₂ | 100K Enable Inputs |
| C | 100K Common Clear Input |
| Q ₀ -Q ₄ | 10K Data Outputs |

Connection Diagram



TL/F/9870-1

Logic Diagram



TL/F/9870-3

Truth Table

| Inputs | | | | Output |
|----------------|----------------|----------------|---|------------------|
| D _n | E ₁ | E ₂ | C | Q _n |
| H | L | L | X | H |
| L | L | L | X | L |
| X | H | X | L | Q _{n-1} |
| X | X | H | L | Q _{n-1} |
| X | H | X | H | L |
| X | X | H | H | L |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

 Q_{n-1} = Previous State

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature Under Bias (T_A) | -55°C to +125°C |
| Maximum Junction Temperature (T_J) | +150°C |
| Supply Voltage | -8V |
| Input Voltage (DC) | -5.2V to +0V |
| Output Current (DC Output HIGH) | -55 mA |
| Operating Range | -5.72V to -4.68V |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Recommended Operating Conditions

| | Min | Typ | Max |
|-------------------------------|--------|-------|--------|
| Supply Voltage (V_{EE}) | -5.72V | -5.2V | -4.68V |
| Ambient Temperature (T_A) | 0°C | | +75°C |

DC Electrical Characteristics

$V_{EE} = -5.2V$, $V_{CC} = V_{CCA} = GND$, $T_A = 0^\circ C$ to $+75^\circ C$ (Notes 1, 2)

| Symbol | Parameter | Temp | Min | Typ | Max | Units | Conditions |
|-----------|-------------------------|---------------------|-------|-----|-------|---------|--|
| V_{OH} | Output HIGH Voltage | $T_A = 0^\circ C$ | -1000 | | -840 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ |
| | | $T_A = +25^\circ C$ | -960 | | -810 | mV | |
| | | $T_A = +75^\circ C$ | -900 | | -720 | mV | |
| V_{OL} | Output LOW Voltage | $T_A = 0^\circ C$ | -1870 | | -1665 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ |
| | | $T_A = +25^\circ C$ | -1850 | | -1650 | mV | |
| | | $T_A = +75^\circ C$ | -1830 | | -1625 | mV | |
| V_{OHC} | Output HIGH Voltage | $T_A = 0^\circ C$ | -1020 | | | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ |
| | | $T_A = +25^\circ C$ | -980 | | | mV | |
| | | $T_A = +75^\circ C$ | -920 | | | mV | |
| V_{OLC} | Output LOW Voltage | $T_A = 0^\circ C$ | | | -1645 | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ |
| | | $T_A = +25^\circ C$ | | | -1630 | mV | |
| | | $T_A = +75^\circ C$ | | | -1605 | mV | |
| V_{IH} | Input HIGH Voltage | | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs |
| V_{IL} | Input LOW Voltage | | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I_{IH} | Input HIGH Current | | | | 290 | | $V_{IN} = V_{IH} (Max)$ |
| I_{IL} | Input LOW Current | | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ |
| I_{EE} | V_{EE} Supply Current | | -125 | -90 | -50 | mA | Inputs Open |

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in *Figure 4*.

DC Electrical Characteristics

$V_{EE} = -4.68V$, $V_{CC} = V_{CCA} = GND$, $T_A = 0^\circ C$ to $+75^\circ C$ (Notes 1, 2)

| Symbol | Parameter | Temp | Min | Typ | Max | Units | Conditions |
|-----------|-------------------------|---------------------|-------|-----|-------|---------|--|
| V_{OH} | Output HIGH Voltage | $T_A = 0^\circ C$ | -1000 | | -840 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ |
| | | $T_A = +25^\circ C$ | -960 | | -810 | mV | |
| | | $T_A = +75^\circ C$ | -900 | | -720 | mV | |
| V_{OL} | Output LOW Voltage | $T_A = 0^\circ C$ | -1870 | | -1665 | mV | $V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ |
| | | $T_A = +25^\circ C$ | -1850 | | -1650 | mV | |
| | | $T_A = +75^\circ C$ | -1830 | | -1625 | mV | |
| V_{OHC} | Output HIGH Voltage | $T_A = 0^\circ C$ | -1020 | | | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ |
| | | $T_A = +25^\circ C$ | -980 | | | mV | |
| | | $T_A = +75^\circ C$ | -920 | | | mV | |
| V_{OLC} | Output LOW Voltage | $T_A = 0^\circ C$ | | | -1645 | mV | $V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ |
| | | $T_A = +25^\circ C$ | | | -1630 | mV | |
| | | $T_A = +75^\circ C$ | | | -1605 | mV | |
| V_{IH} | Input HIGH Voltage | | -1150 | | -880 | mV | Guaranteed HIGH Signal for All Inputs |
| V_{IL} | Input LOW Voltage | | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I_{IH} | Input HIGH Current | | | | 290 | | $V_{IN} = V_{IH} (Max)$ |
| I_{IL} | Input LOW Current | | 0.50 | | | μA | $V_{IN} = V_{IL} (Min)$ |
| I_{EE} | V_{EE} Supply Current | | -125 | -90 | -50 | mA | Inputs Open |

Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in *Figure 4*.

DC Electrical Characteristics

 $V_{EE} = -5.72V, V_{CC} = V_{CCA} = GND, T_A = 0^\circ C \text{ to } +75^\circ C \text{ (Notes 1, 2)}$

| Symbol | Parameter | Temp | Min | Typ | Max | Units | Conditions |
|------------------|--------------------------------|------------------------|-------|-----|-------|-------|---|
| V _{OH} | Output HIGH Voltage | T _A = 0°C | -1000 | | -840 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) |
| | | T _A = +25°C | -960 | | -810 | mV | |
| | | T _A = +75°C | -900 | | -720 | mV | |
| V _{OL} | Output LOW Voltage | T _A = 0°C | -1870 | | -1665 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) |
| | | T _A = +25°C | -1850 | | -1650 | mV | |
| | | T _A = +75°C | -1830 | | -1625 | mV | |
| V _{OHC} | Output HIGH Voltage | T _A = 0°C | -1020 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) |
| | | T _A = +25°C | -980 | | | mV | |
| | | T _A = +75°C | -920 | | | mV | |
| V _{OLC} | Output LOW Voltage | T _A = 0°C | | | -1645 | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) |
| | | T _A = +25°C | | | -1630 | mV | |
| | | T _A = +75°C | | | -1605 | mV | |
| V _{IH} | Input HIGH Voltage | | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs |
| V _{IL} | Input LOW Voltage | | -1810 | | -1490 | mV | Guaranteed LOW Signal for All Inputs |
| I _{IH} | Input HIGH Current | | | | 290 | | V _{IN} = V _{IH} (Max) |
| I _{IL} | Input LOW Current | | 0.50 | | | μA | V _{IN} = V _{IL} (Min) |
| I _{EE} | V _{EE} Supply Current | | -125 | -90 | -50 | mA | Inputs Open |

Loading with
50Ω to -2.0V

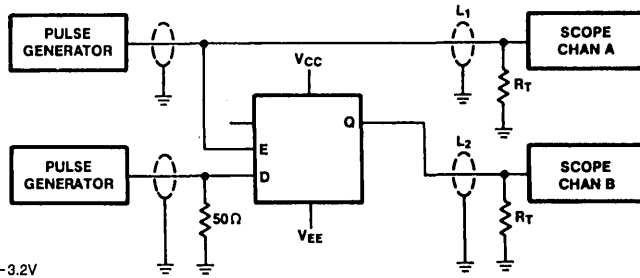
Note 1: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 2: The specified limits shown in the DC Characteristics can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining transverse air flow of 2.5 meters/s (500 linear feet/min) over the device either mounted in the test socket or on the printed circuit board. Test voltage values are given in the DC Operating Conditions and defined in Figure 4.

AC Electrical Characteristics

 $V_{EE} = -5.2V \pm 10\%, V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | T _A = 0°C | | T _A = +25°C | | T _A = +75°C | | Units | Conditions |
|--|---|----------------------|------|------------------------|------|------------------------|------|-------|---------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PDLH} t _{PDHL} | Propagation Delay Data to Output | 1.10 | 2.60 | 1.10 | 2.75 | 1.10 | 3.00 | ns | Figures 1 & 2 |
| t _{PDLH} t _{PDHL} | Propagation Delay Enable to Output | 1.20 | 3.40 | 1.20 | 3.50 | 1.20 | 3.75 | ns | Figures 1 & 3 |
| t _{PDHL} | Propagation Delay Clear to Output | 1.30 | 3.20 | 1.30 | 3.20 | 1.30 | 3.20 | ns | Figures 1, 3 & 4 |
| t _S | Setup Time D ₀ -D ₄ | | 2.50 | | 2.50 | | 2.50 | ns | Figures 1 & 5 |
| t _H | Hold Time D ₀ -D ₄ | | 0.50 | | 0.50 | | 0.50 | ns | |
| t _{TLH} t _{THL} | Transition Time 20% to 80%, 80% to 20% | 1.10 | 3.25 | 1.20 | 3.25 | 1.20 | 3.50 | ns | Figures 1, 2, 3 & 4 |

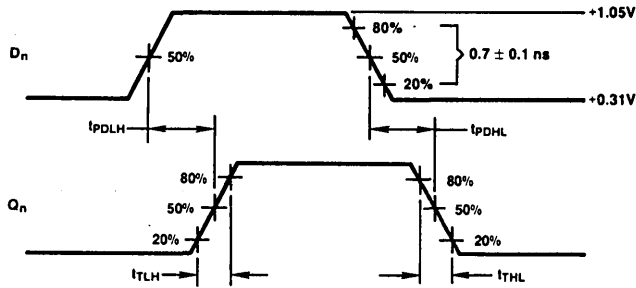


Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -3.2V$
 $L1$ and $L2$ = equal length 50Ω impedance lines
 $R_T = 50\Omega$ terminator internal to scope
 Decoupling 0.1 μf from GND to V_{CC} and V_{EE}
 All unused outputs are loaded with 50Ω to GND
 C_L = Fixture and stray capacitance ≤ 3 pF

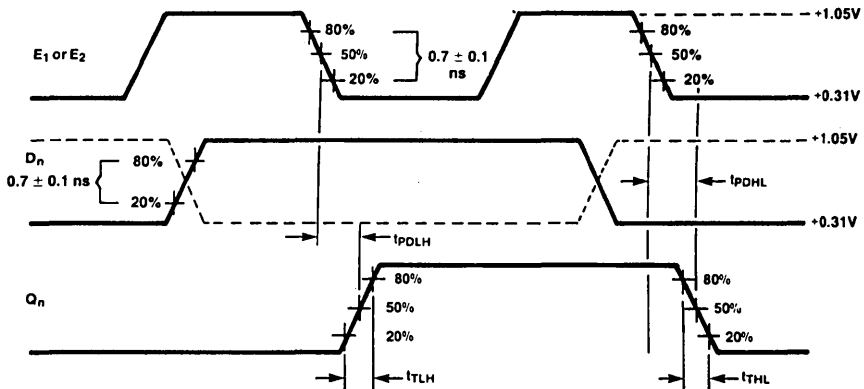
TL/F/9870-4

FIGURE 1. AC Test Circuit



TL/F/9870-5

FIGURE 2. Data Propagation Delay @ $T_A = +25^\circ C$



TL/F/9870-6

FIGURE 3. Enable Propagation Delay @ $T_A = +25^\circ C$

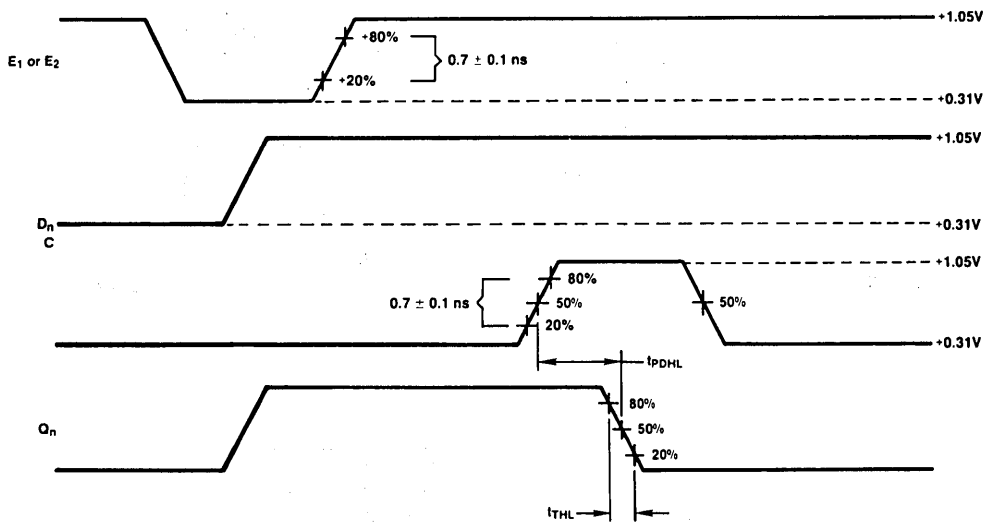


FIGURE 4. Clear Propagation Delay @ $T_A = +25^\circ C$

TL/F/9870-7

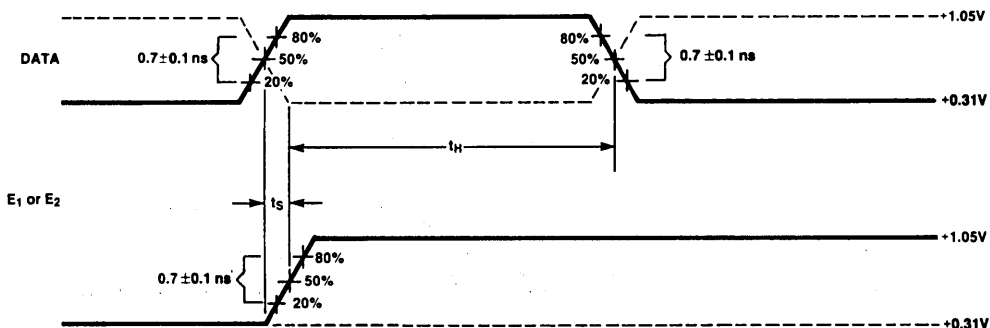


FIGURE 5. Data Setup and Hold Time

TL/F/9870-8

F100179

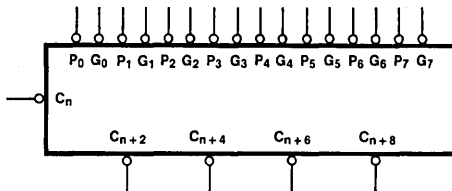
Carry Lookahead Generator

General Description

The F100179 is a high-speed Carry Lookahead Generator intended for use with the F100180 6-bit fast Adder and the F100181 4-bit ALU. All inputs have 50 kΩ pulldown resistors.

Ordering Code: See Section 8

Logic Symbol

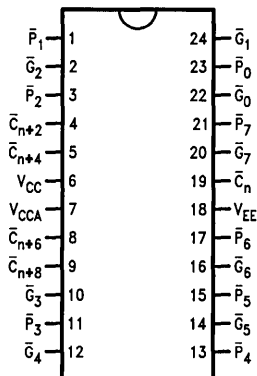


TL/F/9871-3

| Pin Names | Description |
|--|-------------------------------------|
| \bar{C}_n | Carry Input (Active LOW) |
| $\bar{P}_0 - \bar{P}_7$ | Carry Propagate Inputs (Active LOW) |
| $\bar{G}_0 - \bar{G}_7$ | Carry Generate Inputs (Active LOW) |
| $\bar{C}_{n+2}, \bar{C}_{n+4}$ $\bar{C}_{n+6}, \bar{C}_{n+8}$ | Carry Outputs |

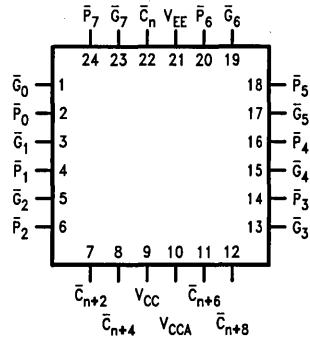
Connection Diagrams

24-Pin DIP



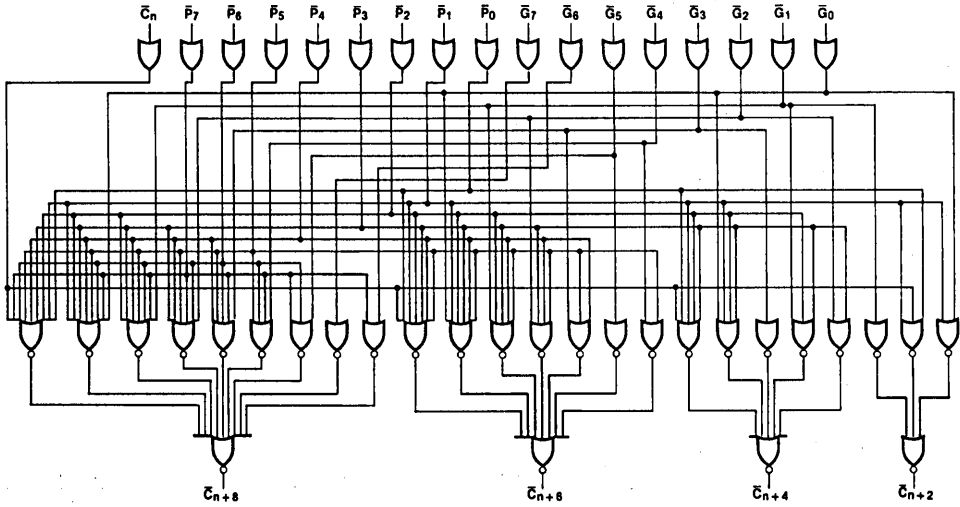
TL/F/9871-1

24-Pin Quad Cerpak



TL/F/9871-2

Logic Diagram



TL/F/9871-5

Truth Tables

\bar{C}_{n+2} Output

| Inputs | | | | | Output |
|------------------------|-------------|-------------|-------------|-------------|-----------------|
| \bar{C}_n | \bar{G}_0 | \bar{P}_0 | \bar{G}_1 | \bar{P}_1 | \bar{C}_{n+2} |
| X | X | X | L | X | L |
| X | L | X | X | L | L |
| L | X | L | X | L | L |
| All other combinations | | | | | H |

$$\bar{C}_{n+2} = \bar{G}_1 \cdot (\bar{P}_1 + \bar{G}_0) \cdot (\bar{P}_1 + \bar{P}_0 + \bar{C}_n)$$

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

\bar{C}_{n+4} Output

| Inputs | | | | | | | | | Output |
|------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------------|
| \bar{C}_n | \bar{G}_0 | \bar{P}_0 | \bar{G}_1 | \bar{P}_1 | \bar{G}_2 | \bar{P}_2 | \bar{G}_3 | \bar{P}_3 | \bar{C}_{n+4} |
| X | X | X | X | X | X | X | L | X | L |
| X | X | X | X | X | L | X | X | L | L |
| X | X | X | L | X | X | L | X | L | L |
| X | L | X | X | L | X | L | X | L | L |
| L | X | L | X | L | X | L | X | L | L |
| All other combinations | | | | | | | | | H |

$$\bar{C}_{n+4} = \bar{G}_3 \cdot (\bar{P}_3 + \bar{G}_2) \cdot (\bar{P}_3 + \bar{P}_2 + \bar{G}_1) \cdot (\bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{G}_0) \cdot (\bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{P}_0 + \bar{C}_n)$$

Truth Tables (Continued)

 \bar{C}_{n+6} Output

| Inputs | | | | | | | | | | | | | Output |
|------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------------|
| \bar{C}_n | \bar{G}_0 | \bar{P}_0 | \bar{G}_1 | \bar{P}_1 | \bar{G}_2 | \bar{P}_2 | \bar{G}_3 | \bar{P}_3 | \bar{G}_4 | \bar{P}_4 | \bar{G}_5 | \bar{P}_5 | \bar{C}_{n+6} |
| X | X | X | X | X | X | X | X | X | X | X | L | X | L |
| X | X | X | X | X | X | X | X | X | L | X | X | L | L |
| X | X | X | X | X | X | X | L | X | X | L | X | L | L |
| X | X | X | X | X | L | X | X | L | X | L | X | L | L |
| X | X | X | L | X | X | L | X | L | X | L | X | L | L |
| X | L | X | X | L | X | L | X | L | X | L | X | L | L |
| L | X | L | X | L | X | L | X | L | X | L | X | L | L |
| All other combinations | | | | | | | | | | | | | H |

$$\bar{C}_{n+6} = \bar{G}_5 \cdot (\bar{P}_5 + \bar{G}_4) \cdot (\bar{P}_5 + \bar{P}_4 + \bar{G}_3) \cdot (\bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{G}_2)$$

- $(\bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{G}_1) \cdot (\bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{G}_0)$
- $(\bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{P}_0 + \bar{C}_n)$

 \bar{C}_{n+8} Output

| Inputs | | | | | | | | | | | | | | Output | | | |
|------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----------------|
| \bar{C}_n | \bar{G}_0 | \bar{P}_0 | \bar{G}_1 | \bar{P}_1 | \bar{G}_2 | \bar{P}_2 | \bar{G}_3 | \bar{P}_3 | \bar{G}_4 | \bar{P}_4 | \bar{G}_5 | \bar{P}_5 | \bar{G}_6 | \bar{P}_6 | \bar{G}_7 | \bar{P}_7 | \bar{C}_{n+8} |
| X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | L | X | L |
| X | X | X | X | X | X | X | X | X | X | X | X | X | L | X | X | L | L |
| X | X | X | X | X | X | X | X | X | X | X | L | X | X | L | X | L | L |
| X | X | X | X | X | X | X | X | X | L | X | X | L | X | L | X | L | L |
| X | X | X | X | X | X | X | L | X | X | L | X | L | X | L | X | L | L |
| X | X | X | X | X | L | X | X | L | X | L | X | L | X | L | X | L | L |
| X | X | X | L | X | X | L | X | L | X | L | X | L | X | L | X | L | L |
| X | L | X | X | L | X | L | X | L | X | L | X | L | X | L | X | L | L |
| L | X | L | X | L | X | L | X | L | X | L | X | L | X | L | X | L | L |
| All other combinations | | | | | | | | | | | | | | | | | H |

$$\bar{C}_{n+8} = \bar{G}_7 \cdot (\bar{P}_7 + \bar{G}_6) \cdot (\bar{P}_7 + \bar{P}_6 + \bar{G}_5) \cdot (\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{G}_4)$$

- $(\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{G}_3) \cdot (\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{G}_2)$
- $(\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{G}_1)$
- $(\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{G}_0)$
- $(\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{P}_0 + \bar{C}_n)$

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current $\bar{C}_N, \bar{G}_0-\bar{G}_7$ $\bar{P}_0-\bar{P}_7$ | | | 250 340 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -220 | -150 | -100 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|-------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $\bar{C}_n, \bar{G}_0-\bar{G}_7, \bar{P}_0-\bar{P}_7$ to \bar{C}_{n+x} | 1.10 | 2.90 | 1.10 | 2.90 | 1.10 | 3.00 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.80 | 0.45 | 1.80 | 0.45 | 1.80 | ns | |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|-------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay $\bar{C}_n, \bar{G}_0-\bar{G}_7, \bar{P}_0-\bar{P}_7$ to \bar{C}_{n+x} | 1.10 | 2.70 | 1.10 | 2.70 | 1.10 | 2.80 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.70 | 0.45 | 1.70 | 0.45 | 1.70 | ns | |

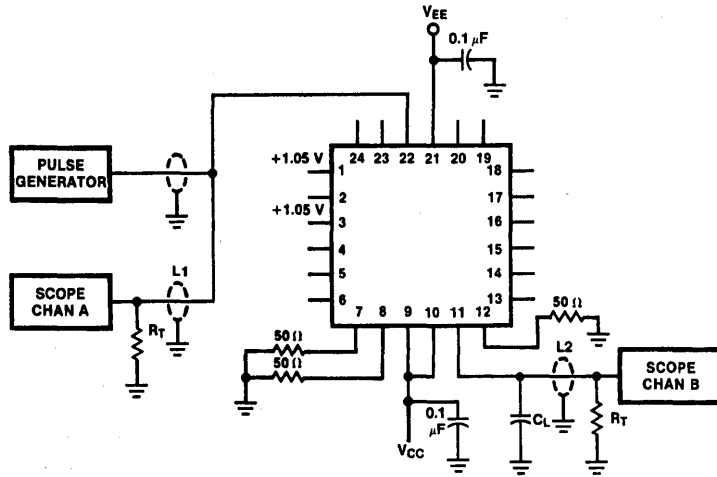


FIGURE 1. AC Test Circuit

TL/F/9871-6

Notes:

- $V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$
- $L1$ and $L2$ = equal length 50Ω impedance lines
- $R_T = 50\Omega$ terminator internal to scope
- Decoupling $0.1 \mu F$ from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

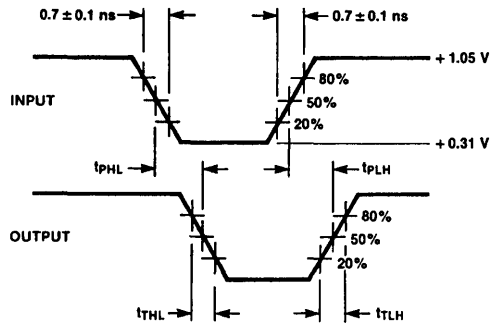
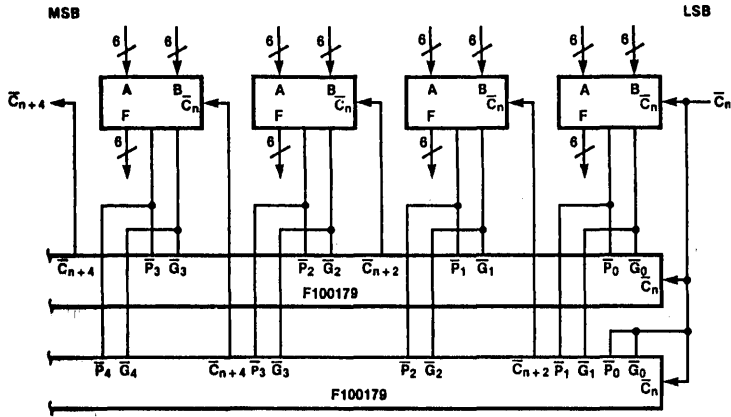


FIGURE 2. Propagation Delay and Transition Times

TL/F/9871-6

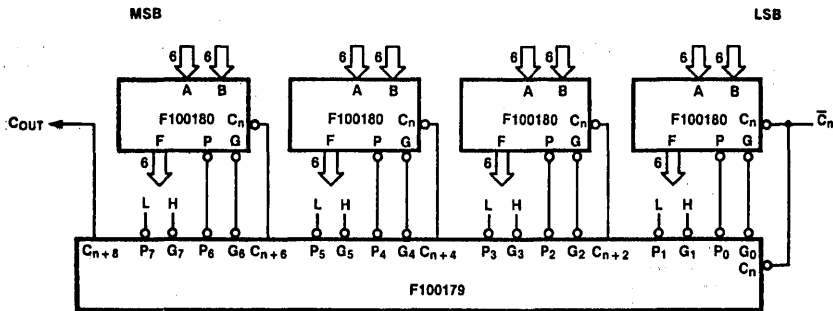
Applications

Fast Adder and Carry Lookahead



TL/F/9871-8

24-Bit Adder Using One Carry Lookahead



TL/F/9871-9



F100180 High-Speed 6-Bit Adder

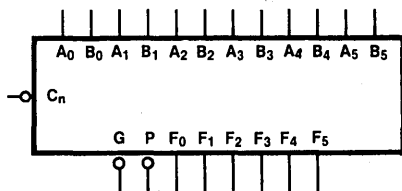
General Description

The F100180 is a high-speed 6-bit adder capable of performing a full 6-bit addition of two operands. Inputs for the adder are active-LOW Carry, Operand A, and Operand B; outputs are Function, active-LOW Carry Generate, and ac-

tive-LOW Carry Propagate. When used with the F100179 Full Carry Lookahead as a second order lookahead block, the F100180 provides high-speed addition of very long words. All inputs have 50 k Ω pull-down resistors.

Ordering Code: See Section 8

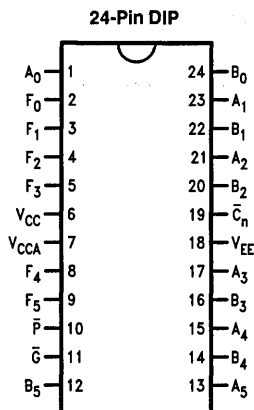
Logic Symbol



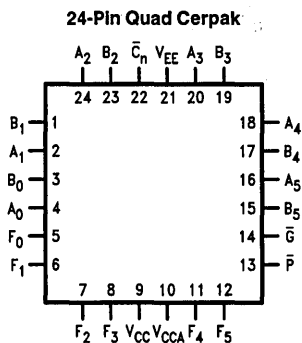
TL/F/9872-3

| Pin Names | Description |
|--------------------------------|-------------------------------------|
| A ₀ -A ₅ | Operand A Inputs |
| B ₀ -B ₅ | Operand B Inputs |
| \overline{C}_n | Carry Input (Active LOW) |
| \overline{G} | Carry Generate Output (Active LOW) |
| \overline{P} | Carry Propagate Output (Active LOW) |
| F ₀ -F ₅ | Function Outputs |

Connection Diagrams

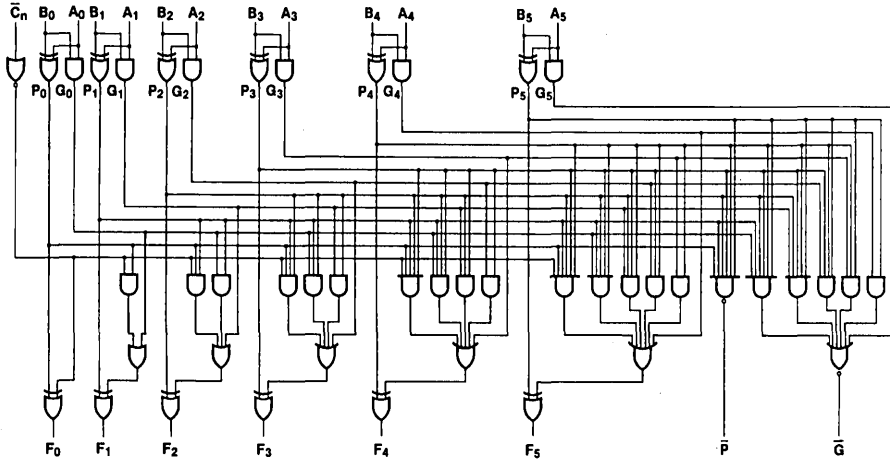


TL/F/9872-1



TL/F/9872-2

Logic Diagram



TL/F/9872-5

Logic Equations

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

$$i = 0, 1, 2, 3, 4, 5$$

$$F_0 = P_0 \oplus C_n$$

$$F_1 = P_1 \oplus (G_0 + P_0 C_n)$$

$$F_2 = P_2 \oplus (G_1 + P_1 G_0 + P_1 P_0 C_n)$$

$$F_3 = P_3 \oplus (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n)$$

$$F_4 = P_4 \oplus (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_n)$$

$$F_5 = P_5 \oplus (G_4 + P_4 G_3 + P_4 P_3 G_2 + P_4 P_3 P_2 G_1 + P_4 P_3 P_2 P_1 G_0 + P_4 P_3 P_2 P_1 P_0 C_n)$$

$$\bar{P} = \bar{P}_0 \bar{P}_1 \bar{P}_2 \bar{P}_3 \bar{P}_4 \bar{P}_5$$

$$\bar{G} = \bar{G}_5 + P_5 \bar{G}_4 + P_5 P_4 \bar{G}_3 + P_5 P_4 G_3 \bar{G}_2 + P_5 P_4 P_3 P_2 \bar{G}_1 + P_5 P_4 P_3 P_2 P_1 \bar{G}_0$$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{EE} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|--|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|----------------------------------|------|------|------|---------|-------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 220 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -290 | -195 | -135 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to F_n | 1.10 | 4.70 | 1.10 | 4.60 | 1.10 | 4.70 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to \bar{F} | 1.00 | 3.00 | 1.00 | 3.00 | 1.00 | 3.30 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to \bar{G} | 1.40 | 3.90 | 1.40 | 3.80 | 1.40 | 3.90 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{C}_n to F_n | 1.10 | 4.00 | 1.10 | 3.90 | 1.10 | 4.00 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.40 | 0.45 | 2.30 | 0.45 | 2.40 | ns | |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|--|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to F_n | 1.10 | 4.50 | 1.10 | 4.40 | 1.10 | 4.50 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to \bar{F} | 1.00 | 2.80 | 1.00 | 2.80 | 1.00 | 3.10 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to \bar{G} | 1.40 | 3.70 | 1.40 | 3.60 | 1.40 | 3.70 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{C}_n to F_n | 1.10 | 3.80 | 1.10 | 3.70 | 1.10 | 3.80 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.30 | 0.45 | 2.20 | 0.45 | 2.30 | ns | |

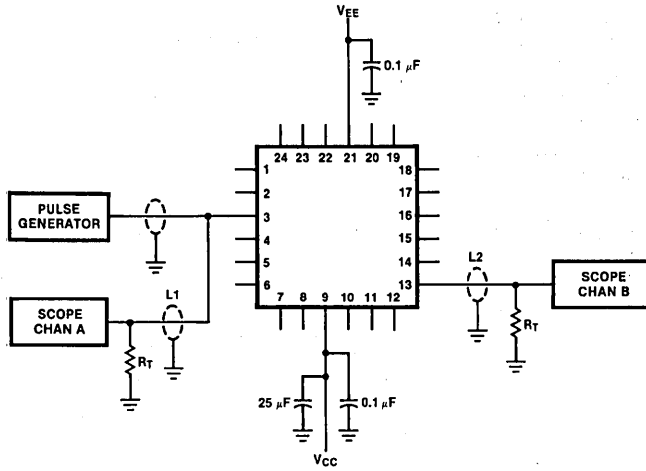


FIGURE 1. AC Test Circuit

TL/F/9872-6

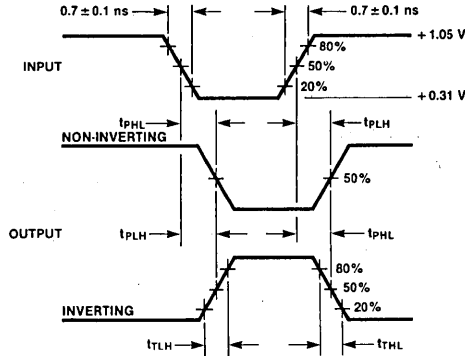


FIGURE 2. Propagation Delay and Transition Times

TL/F/9872-7

Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

F100181

4-Bit Binary/BCD Arithmetic Logic Unit

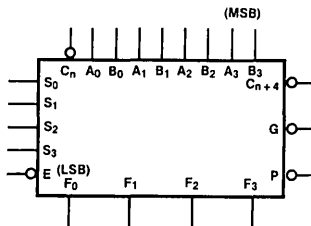
General Description

The F100181 performs eight logic operations and eight arithmetic operations on a pair of 4-bit words. The operating mode is determined by signals applied to the Select (S_n) inputs, as shown in the Function Select table. In addition to performing binary arithmetic, the circuit contains the necessary correction logic to perform BCD addition and subtraction. Output latches are provided to reduce overall package count and increase system operating speed. When the latches are not required, leaving the Enable (\bar{E}) input LOW makes the latches transparent.

The circuit uses internal lookahead carry to minimize delay to the F_n outputs and to the ripple Carry output, \bar{C}_{n+4} . Group Carry Lookahead Propagate (\bar{P}) and Generate (\bar{G}) outputs are also provided, which are independent of the Carry input \bar{C}_n . The \bar{P} output goes LOW when a plus operation produces fifteen (nine for BCD) or when a minus operation produces zero. Similarly, \bar{G} goes LOW when the sum of A and B is greater than fifteen (nine for BCD) in a plus mode, or when their difference is greater than zero in a minus mode. All inputs have 50 k Ω pull-down resistors.

Ordering Code: See Section 8

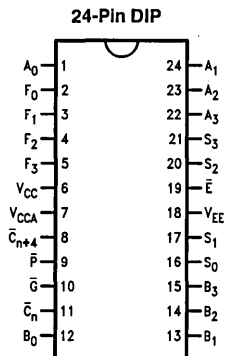
Logic Symbol



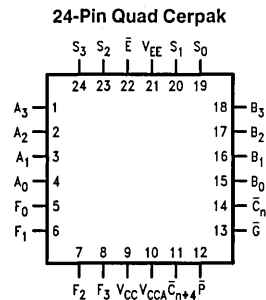
TL/F/9873-4

| Pin Names | Description |
|-----------------|---|
| A_0-A_3 | Word A Operand Inputs |
| B_0-B_3 | Word B Operand Inputs |
| \bar{C}_n | Carry Input (Active LOW) |
| S_0-S_3 | Function Select Inputs |
| \bar{E} | Latch Enable Input (Active LOW) |
| \bar{P} | Carry Lookahead Propagate Output (Active LOW) |
| \bar{G} | Carry Lookahead Generate Output (Active LOW) |
| \bar{C}_{n+4} | Carry Output |
| F_0-F_3 | Function Outputs |

Connection Diagrams

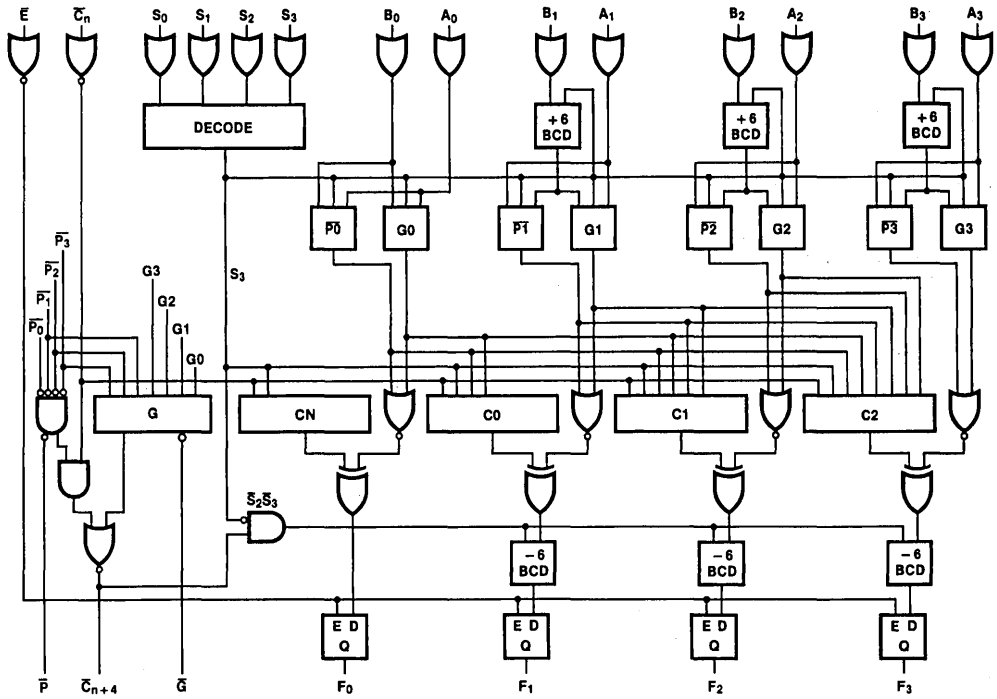


TL/F/9873-1



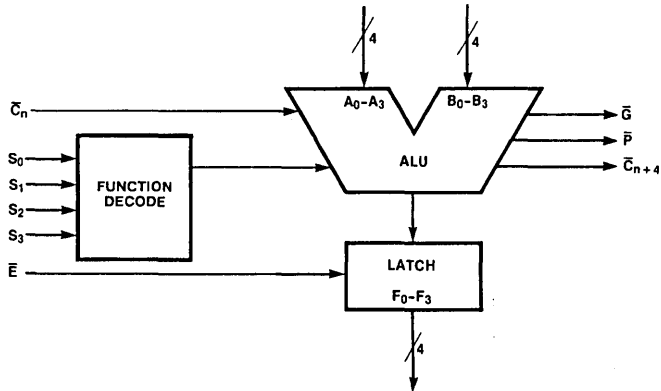
TL/F/9873-2

Logic Diagram



TL/F/9873-5

Block Diagram



TL/F/9873-6

Functional Description

There are two modes of operation: Arithmetic and Logic. The S_3 input controls these two modes:

$S_3 = \text{LOW}$ for Arithmetic mode

$S_3 = \text{HIGH}$ for Logic mode

The arithmetic mode includes decimal and binary arithmetic operations. S_2 is the control input: with $S_3 = \text{LOW}$,

$S_2 = \text{LOW}$ for Decimal Arithmetic (BCD)

$S_2 = \text{HIGH}$ for Binary Arithmetic

DECIMAL ARITHMETIC OPERATION

Addition

$F = A \text{ plus } B \text{ plus } C_n$. Arguments A and B are directly applied to the inputs. The circuit automatically performs the "+6" and "-6" logic correction internally.

Subtraction

$F = A \text{ minus } B \text{ plus } C_n$. Arguments A and B are directly applied to the inputs. The circuit automatically takes the nines complement of B and adds "+6". A "-6" adjustment is made if the subtraction algorithm calls for it. If there is a carry out, the result is a positive number. With no carry out, the result is a negative number expressed in its nines complement form. Therefore, to perform a subtraction with

results in the tens complement form, an initial carry should be forced into the lowest order bit, i.e., set $\bar{C}_n = \text{LOW}$.

(tens complement of B) = (nines complement of B) + 1

$F = B \text{ minus } A \text{ plus } C_n$. Operation is similar to and results are the same as $F = A \text{ minus } B \text{ plus } C_n$.

BINARY ARITHMETIC OPERATION

Addition

$F = A \text{ minus } B \text{ plus } C_n$. Arguments A and B are directly applied to the inputs.

Subtraction

$F = A \text{ minus } B \text{ plus } C_n$. Arguments A and B are directly applied to the inputs. The circuit automatically takes the ones complement of B (by inverting B internally). If there is a carry out the result is a positive number. With no carry out, the result is a negative number expressed in its ones complement form. Therefore, to perform a subtraction with results in the twos complement form, an initial carry should be forced into the lowest order bit, i.e., set $\bar{C}_n = \text{LOW}$.

(twos complement of B) = (ones complement of B) + 1

$F = B \text{ minus } A \text{ plus } C_n$. Operation is similar and results are the same as $F = A \text{ minus } B \text{ plus } C_n$.

Function Table

| S_3 | S_2 | S_1 | S_0 | F_n Function | G_n | P_n | Outputs | | |
|-------|-------|-------|-------|---|-----------------|-------------------------|-----------------|-------------|-----------|
| | | | | | (n = 0 to 3) | (n = 0 to 3) | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| L | L | L | L | $F_n = A \text{ plus } B \text{ plus } C_n$ (BCD) | $A_n D_n$ | $A_n + D_n$ | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| L | L | L | H | $F_n = A \text{ minus } B \text{ plus } C_n$ (BCD) | $A_n \bar{B}_n$ | $A_n + \bar{B}_n$ | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| L | L | H | L | $F_n = B \text{ minus } A \text{ plus } C_n$ (BCD) | $\bar{A}_n B_n$ | $\bar{A}_n + B_n$ | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| L | L | H | H | $F_n = 0 \text{ minus } B \text{ plus } C_n$ (BCD) | L | \bar{B}_n | \bar{C}_{n+4} | H | \bar{P} |
| L | H | L | L | $F_n = A \text{ plus } B \text{ plus } C_n$ (Binary) | $A_n B_n$ | $A_n + B_n$ | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| L | H | L | H | $F_n = A \text{ minus } B \text{ plus } C_n$ (Binary) | $A_n \bar{B}_n$ | $A_n + \bar{B}_n$ | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| L | H | H | L | $F_n = B \text{ minus } A \text{ plus } C_n$ (Binary) | $\bar{A}_n B_n$ | $\bar{A}_n + B_n$ | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| L | H | H | H | $F_n = 0 \text{ minus } B \text{ plus } C_n$ (Binary) | L | \bar{B}_n | \bar{C}_{n+4} | H | \bar{P} |
| H | L | L | L | $F_n = A_n B_n + \bar{A}_n \bar{B}_n$ | $A_n B_n$ | $A_n + B_n$ | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| H | L | L | H | $F_n = A_n \bar{B}_n + \bar{A}_n B_n$ | $A_n \bar{B}_n$ | $A_n + \bar{B}_n$ | \bar{C}_{n+4} | \bar{G} | \bar{P} |
| H | L | H | L | $F_n = A_n + B_n$ | A_n | \bar{B}_n | \bar{C}_{n+4} | \bar{G}_x | \bar{P} |
| H | L | H | H | $F_n = A_n$ | A_n | H | \bar{C}_{n+4} | \bar{G} | L |
| H | H | L | L | $F_n = \bar{B}_n$ | L | B_n | \bar{C}_{n+4} | H | \bar{P} |
| H | H | L | H | $F_n = B_n$ | L | \bar{B}_n | \bar{C}_{n+4} | H | \bar{P} |
| H | H | H | L | $F_n = A_n B_n$ | L | $\bar{A}_n + \bar{B}_n$ | \bar{C}_{n+4} | H | \bar{P} |
| H | H | H | H | $F_n = \text{LOW}$ | L | H | \bar{C}_n | H | L |

H = HIGH Voltage Level

L = LOW Voltage Level

$$\bar{P} = \bar{P}_0 + \bar{P}_1 + \bar{P}_2 + \bar{P}_3$$

$$\bar{G} = \bar{G}_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$$

$$\bar{C}_{n+4} = \bar{G} \cdot (\bar{P} + \bar{C}_n)$$

Arithmetic Operations

$$F_n = \bar{G}_n + \bar{P}_n \oplus C_i \quad i = 0 \text{ to } 3$$

Logic Operations

$$F_n = G_n + \bar{P}_n$$

Internal Equations for Carry Lookahead

(i = 0, 1, 2, 3)

$$C_0 = C_n + S_3$$

$$C_1 = G_0 + P_0 C_n + S_3$$

$$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_n + S_3$$

$$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n + S_3$$

Internal Equations for +6 Logic

$$D_0 = B_0$$

$$D_1 = \bar{B}_1$$

$$D_2 = B_1 B_2 + \bar{B}_1 \bar{B}_2$$

$$D_3 = B_1 + B_2 + B_3$$

$$\bar{G}_x = \bar{G}_3 P_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$$

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to +150°C
Maximum Junction Temperature (T_J) +150°C

Case Temperature under Bias (T_C) 0°C to +85°C
V_{EE} Pin Potential to Ground Pin -7.0V to +0.5V
Input Voltage (DC) V_{EE} to +0.5V
Output Current (DC Output HIGH) -50 mA
Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-------|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1035 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V _{OH} C | Output HIGH Voltage | -1030 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1595 | | | |
| V _{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

DC Electrical Characteristics

V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-------------------|---------------------|-------|-----|-------|-------|---|------------------------------|
| V _{OH} | Output HIGH Voltage | -1035 | | -880 | mV | V _{IN} = V _{IH} (Max) or V _{IL} (Min) | Loading with 50Ω to -2.0V |
| V _{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V _{OH} C | Output HIGH Voltage | -1045 | | | mV | V _{IN} = V _{IH} (Min) or V _{IL} (Max) | Loading with 50Ω to -2.0V |
| V _{OL} C | Output LOW Voltage | | | -1610 | | | |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V _{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL} (Min) | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

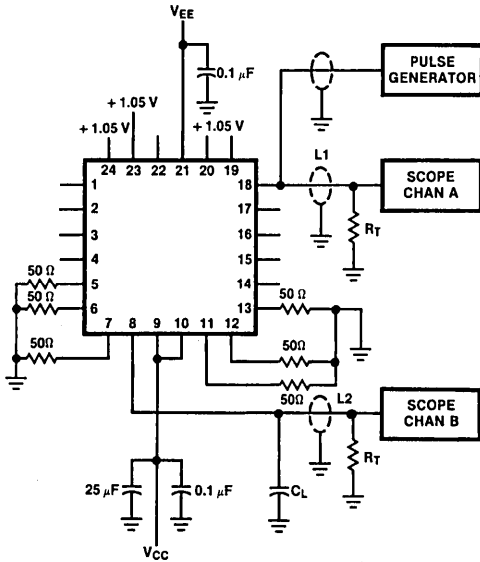
| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--|------|------|------------|---------|-------------------------|
| I_{IH} | Input HIGH Current S_n, \bar{E} All Others | | | 350 250 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -300 | -210 | -130 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|----------------------|-------|----------------------|------|----------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to F_n | 2.00 | 6.90 | 2.10 | 6.80 | 2.30 | 7.40 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to \bar{P}, \bar{G} | 1.40 | 4.70 | 1.40 | 4.40 | 1.40 | 4.70 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to \bar{C}_{n+4} | 2.00 | 6.50 | 2.00 | 6.50 | 2.10 | 6.80 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{C}_n to F_n | 1.60 | 5.10 | 1.60 | 5.20 | 1.60 | 5.50 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay \bar{C}_n to \bar{C}_{n+4} | 1.30 | 3.00 | 1.40 | 3.00 | 1.40 | 3.10 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay S_n to F_n | 1.40 | 8.80 | 1.50 | 8.60 | 1.50 | 9.00 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay S_n to \bar{P}, \bar{G} | 1.70 | 7.40 | 2.00 | 5.90 | 2.00 | 6.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay S_n to \bar{C}_{n+4} | 2.70 | 10.10 | 2.80 | 8.50 | 2.90 | 8.70 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to F_n | 1.00 | 3.40 | 0.90 | 3.60 | 1.10 | 3.80 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.70 | 0.45 | 2.60 | 0.45 | 2.70 | ns | <i>Figures 1 and 2</i> |
| t_s | Setup Time A_n, B_n S_n \bar{C}_n | 7.60 8.70 4.80 | | 7.60 8.50 5.00 | | 8.10 9.60 5.30 | | ns | <i>Figure 3</i> |
| t_h | Hold Time A_n, B_n S_n \bar{C}_n | 0.10 0.60 0.60 | | 0.10 0.60 0.60 | | 0.10 0.60 0.60 | | ns | |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E} | 2.00 | | 2.00 | | 2.00 | | ns | <i>Figure 2</i> |

Cerpak AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|----------------------|------|----------------------|------|----------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to F_n | 2.00 | 6.70 | 2.10 | 6.60 | 2.30 | 7.20 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to \bar{F}, \bar{G} | 1.40 | 4.50 | 1.40 | 4.20 | 1.40 | 4.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay A_n, B_n to \bar{C}_{n+4} | 2.00 | 6.30 | 2.00 | 6.30 | 2.10 | 6.60 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{C}_n to F_n | 1.60 | 4.90 | 1.60 | 5.00 | 1.60 | 5.30 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay \bar{C}_n to \bar{C}_{n+4} | 1.30 | 2.80 | 1.40 | 2.80 | 1.40 | 2.90 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay S_n to F_n | 1.40 | 8.60 | 1.50 | 8.40 | 1.50 | 8.80 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay S_n to \bar{F}, \bar{G} | 1.70 | 7.20 | 2.00 | 5.70 | 2.00 | 6.30 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay S_n to \bar{C}_{n+4} | 2.70 | 9.90 | 2.80 | 8.30 | 2.90 | 8.50 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to F_n | 1.00 | 3.20 | 0.90 | 3.40 | 1.10 | 3.60 | ns | <i>Figures 1 and 2</i> |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.60 | 0.45 | 2.50 | 0.45 | 2.60 | ns | <i>Figures 1 and 2</i> |
| t_s | Setup Time A_n, B_n S_n \bar{C}_n | 7.50 8.60 4.70 | | 7.50 8.40 4.90 | | 8.00 9.50 5.20 | | ns | <i>Figure 3</i> |
| t_h | Hold Time A_n, B_n S_n \bar{C}_n | 0 0.50 0.50 | | 0 0.50 0.50 | | 0 0.50 0.50 | | ns | |
| $t_{pw(L)}$ | Pulse Width LOW \bar{E} | 2.00 | | 2.00 | | 2.00 | | ns | <i>Figure 2</i> |

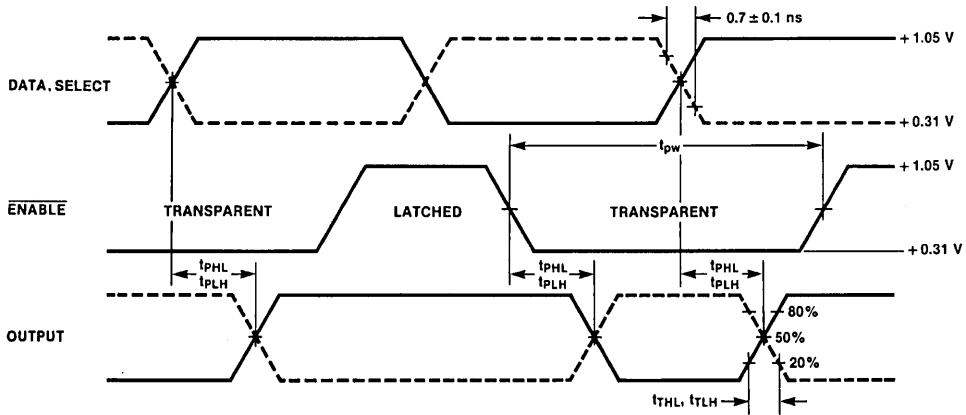


Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
- All unused outputs are loaded with 50Ω to GND
- C_L = Fixture and stray capacitance ≤ 3 pF
- Pin numbers shown are for flatpak; for DIP see logic symbol

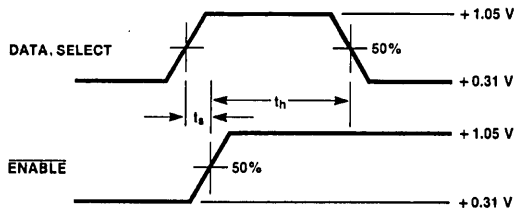
TL/F/9873-7

FIGURE 1. AC Test Circuit



TL/F/9873-8

FIGURE 2. Enable Timing



TL/F/9873-9

FIGURE 3. Setup and Hold Times

Notes:

- t_s is the minimum time before the transition of the enable that information must be present at the data input.
- t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.



F100182 9-Bit Wallace Tree Adder

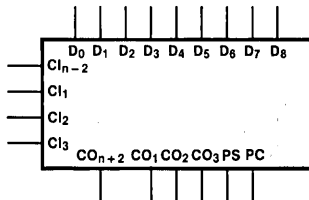
General Description

The F100182 is a 9-bit Wallace tree adder. It is designed to assist in performing high-speed hardware multiplication. The device is designed to add 9 bits of data 1-bit-slice wide and handle the carry-ins from the previous slices. The F100182 is easily expanded and still maintains four levels of delay regardless of input string length. In conjunction with the

F100183 Recode Multiplier, the F100179 Carry Lookahead, and the F100180 High-speed Adder, the F100182 assists in performing parallel multiplication of two signed numbers to produce a signed two's complement product. See F100183 data sheet for additional information. All inputs have 50 k Ω pull-down resistors.

Ordering Code: See Section 8

Logic Symbol

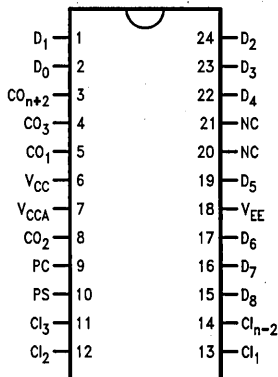


TL/F/9874-3

| Pin Names | Description |
|--|----------------------|
| D ₀ -D ₈ | Data Inputs |
| Cl ₁ -Cl ₃ , Cl _{n-2} | Carry Inputs |
| CO ₁ -CO ₃ , CO _{n+2} | Carry Outputs |
| PS | Partial Sum Output |
| PC | Partial Carry Output |

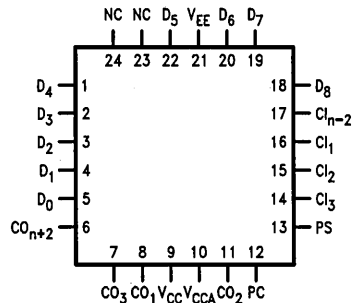
Connection Diagrams

24-Pin DIP



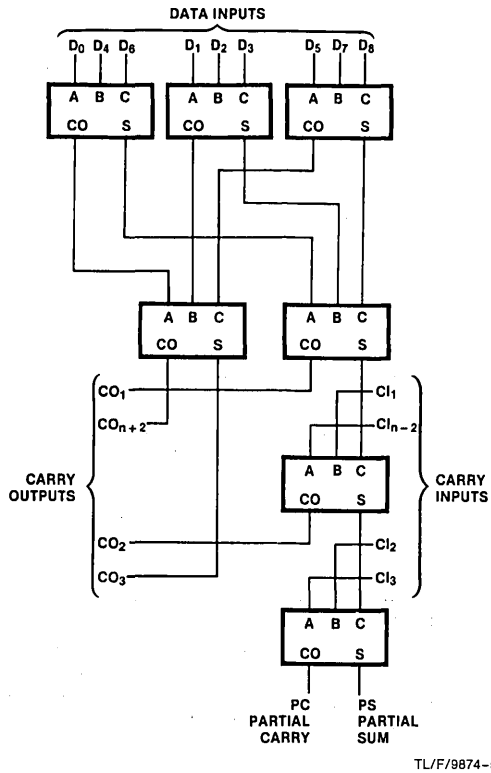
TL/F/9874-1

24-Pin Quad Cerpak

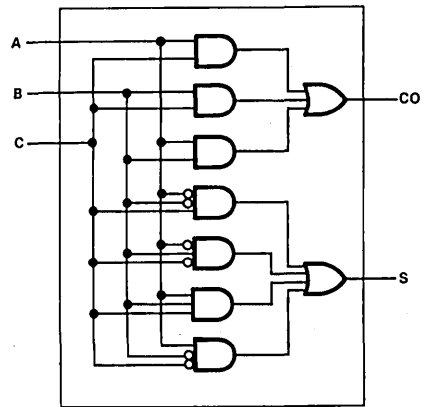


TL/F/9874-2

Logic Diagram



Adder Logic Diagram



Adder Truth Table

| Inputs | | | Outputs | |
|--------|---|---|---------|----|
| A | B | C | S | CO |
| L | L | L | L | L |
| L | L | H | H | L |
| L | H | L | H | L |
| L | H | H | L | H |
| H | L | L | H | L |
| H | L | H | L | H |
| H | H | L | L | H |
| H | H | H | H | H |

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$

Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$

V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$

Input Voltage (DC) V_{EE} to $+0.5\text{V}$

Output Current (DC Output HIGH) -50mA

Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|---------|---------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|---------|-----|---------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|---|------|------|------|---------|-------------------------|
| I_{IH} | Input HIGH Current CI_1-CI_3, CI_{n-2} $D_1, D_3, D_4, D_5, D_6, D_8$ | | | 300 | μA | $V_{IN} = V_{IH} (Max)$ |
| | D_0, D_2, D_7 | | | 250 | | |
| I_{EE} | Power Supply Current | -260 | -180 | -125 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to CO_{n+2} | 1.40 | 4.50 | 1.40 | 4.50 | 1.50 | 4.70 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay D_n to CO_1 | 1.30 | 4.80 | 1.30 | 4.70 | 1.50 | 5.00 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to CO_2 | 2.20 | 6.20 | 2.20 | 6.10 | 2.30 | 6.40 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to CO_3 | 1.30 | 4.70 | 1.40 | 4.70 | 1.50 | 5.00 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to PS, PC | 2.50 | 7.20 | 2.50 | 7.20 | 2.70 | 7.40 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay CI_{n-2}, CI_1 to CO_2 | 1.00 | 3.50 | 1.00 | 3.40 | 1.10 | 3.70 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay CI_{n-2}, CI_1 to PS, PC | 1.50 | 4.50 | 1.50 | 4.45 | 1.60 | 4.60 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay CI_3, CI_2 to PS, PC | 0.80 | 3.30 | 0.80 | 3.20 | 0.90 | 3.60 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.60 | 0.45 | 1.60 | 0.45 | 1.60 | ns | <i>Figures 1 and 2</i> |

Cerpak AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to CO_{n+2} | 1.40 | 4.30 | 1.40 | 4.30 | 1.50 | 4.50 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay D_n to CO_1 | 1.30 | 4.60 | 1.30 | 4.50 | 1.50 | 4.80 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to CO_2 | 2.20 | 6.00 | 2.20 | 5.90 | 2.30 | 6.20 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to CO_3 | 1.30 | 4.50 | 1.40 | 4.50 | 1.50 | 4.80 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to PS, PC | 2.50 | 7.00 | 2.50 | 7.00 | 2.70 | 7.20 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay Cl_{n-2}, Cl_1 to CO_2 | 1.00 | 3.30 | 1.00 | 3.20 | 1.10 | 3.50 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay Cl_{n-2}, Cl_1 to PS, PC | 1.50 | 4.30 | 1.50 | 4.25 | 1.60 | 4.40 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay Cl_3, Cl_2 to PS, PC | 0.80 | 3.10 | 0.80 | 3.00 | 0.90 | 3.40 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 1.50 | 0.45 | 1.50 | 0.45 | 1.50 | ns | <i>Figures 1 and 2</i> |

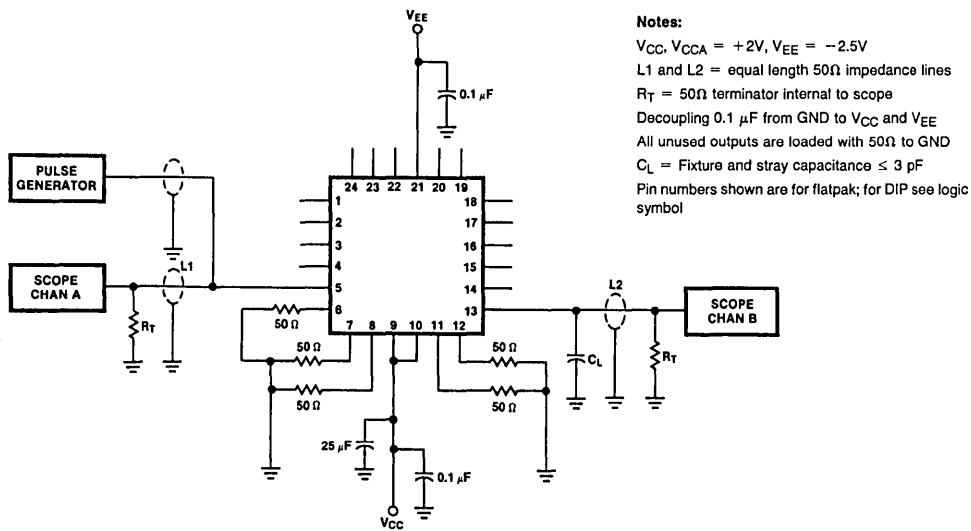


FIGURE 1. AC Test Circuit

TL/F/9874-7

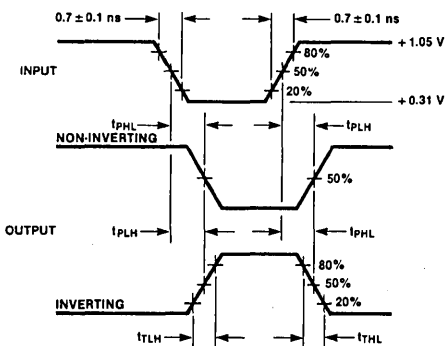
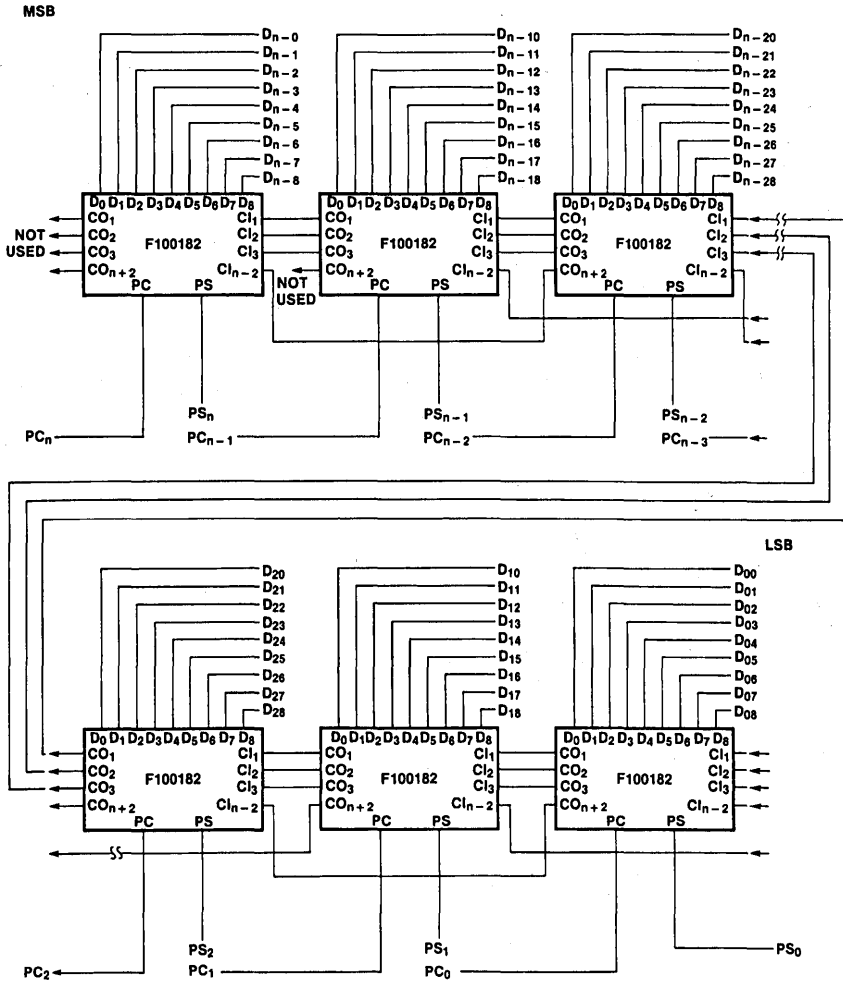


FIGURE 2. Propagation Delay and Transition Times

TL/F/9874-8

Application

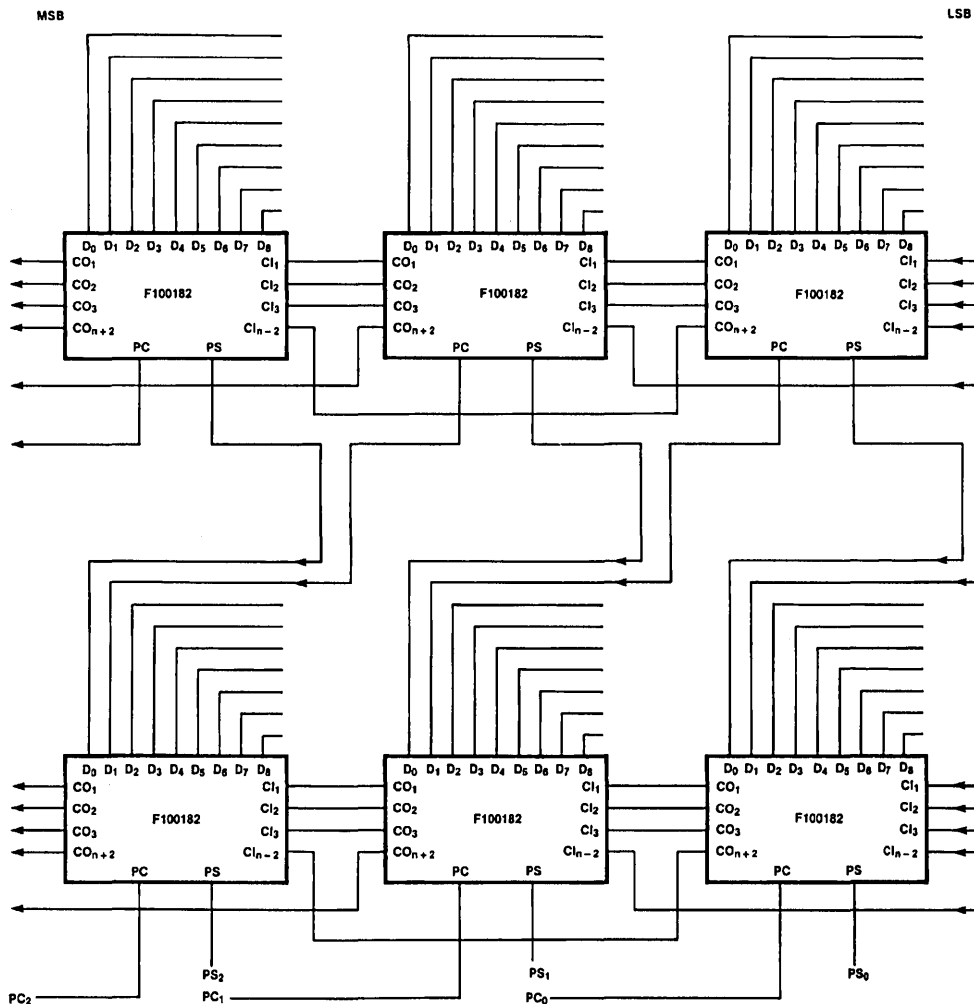
Typical Horizontal Interconnection of 9-Bit Wallace Tree Adders F100182



TL/F/9874-9

Application (Continued)

16-Bit Vertical Expansion of Wallace Tree Adders



TL/F/9874-10



F100183

2 x 8-Bit Recode Multiplier

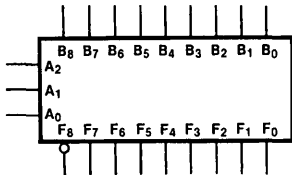
General Description

The F100183 is a 2 x 8-bit recode multiplier designed to perform high-speed hardware multiplication. In conjunction with the F100182 Wallace Tree Adder, the F100179 Carry Lookahead, and the F100180 High-speed Adder, the

F100183 performs parallel multiplication of two signed numbers in twos complement form to produce a signed twos complement product. All inputs have 50 kΩ pull-down resistors.

Ordering Code: See Section 8

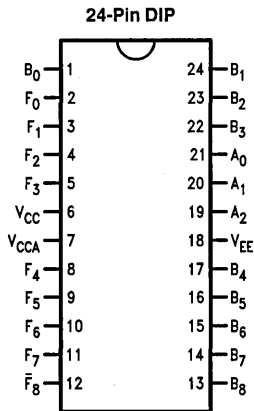
Logic Symbol



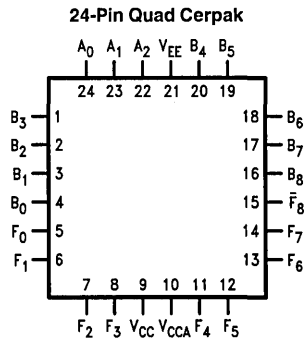
TL/F/9875-3

| Pin Names | Description |
|--------------------------------|----------------------------|
| A ₀ -A ₂ | Multiplier (Recode) Inputs |
| B ₀ -B ₈ | Multiplicand Inputs |
| F ₀ -F ₇ | Partial Product Outputs |
| F ₈ $\bar{}$ | Sign Extension Output |

Connection Diagrams

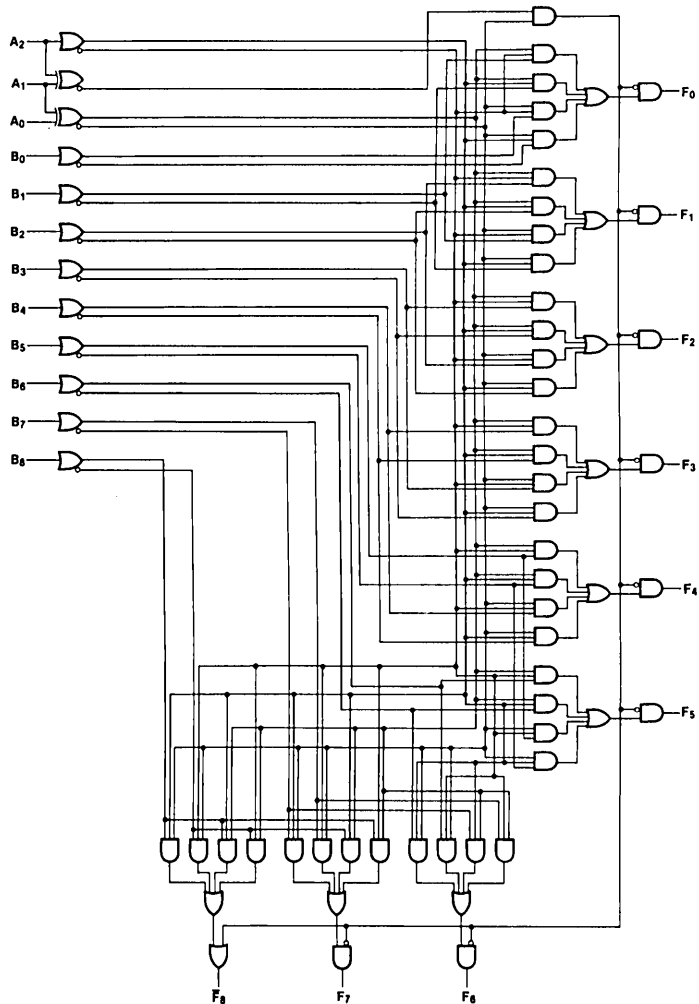


TL/F/9875-1



TL/F/9875-2

Logic Diagram



TL/F/9875-5

Truth Table

| Inputs | | | Recode Mode | Outputs | | | | | | | | |
|----------------|----------------|----------------|-------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| A ₂ | A ₁ | A ₀ | | \bar{F}_8 | F ₇ | F ₆ | F ₅ | F ₄ | F ₃ | F ₂ | F ₁ | F ₀ |
| L | L | L | 0 | H | L | L | L | L | L | L | L | L |
| L | L | H | +1 | \bar{B}_8 | B ₈ | B ₇ | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ |
| L | H | L | +1 | \bar{B}_8 | B ₈ | B ₇ | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ |
| L | H | H | +2 | \bar{B}_8 | B ₇ | B ₆ | B ₅ | B ₄ | B ₃ | B ₂ | B ₁ | B ₀ |
| H | L | L | -2 | B ₈ | \bar{B}_7 | \bar{B}_6 | \bar{B}_5 | \bar{B}_4 | \bar{B}_3 | \bar{B}_2 | \bar{B}_1 | \bar{B}_0 |
| H | L | H | -1 | B ₈ | \bar{B}_8 | \bar{B}_7 | \bar{B}_6 | \bar{B}_5 | \bar{B}_4 | \bar{B}_3 | \bar{B}_2 | \bar{B}_1 |
| H | H | L | -1 | B ₈ | \bar{B}_8 | \bar{B}_7 | \bar{B}_6 | \bar{B}_5 | \bar{B}_4 | \bar{B}_3 | \bar{B}_2 | \bar{B}_1 |
| H | H | H | 0 | H | L | L | L | L | L | L | L | L |

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature -65°C to $+150^{\circ}\text{C}$
 Maximum Junction Temperature (T_J) $+150^{\circ}\text{C}$

Case Temperature under Bias (T_C) 0°C to $+85^{\circ}\text{C}$
 V_{EE} Pin Potential to Ground Pin -7.0V to $+0.5\text{V}$
 Input Voltage (DC) V_{EE} to $+0.5\text{V}$
 Output Current (DC Output HIGH) -50mA
 Operating Range (Note 2) -5.7V to -4.2V

DC Electrical Characteristics

$V_{EE} = -4.5\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-------|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1035 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.2\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1020 | | -870 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1810 | | -1605 | | | |
| V_{OHC} | Output HIGH Voltage | -1030 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1595 | | | |
| V_{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

DC Electrical Characteristics

$V_{EE} = -4.8\text{V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|---------------------|-------|-----|-------|---------------|--|---|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH}(\text{Max})$ or $V_{IL}(\text{Min})$ | Loading with 50 Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH}(\text{Min})$ or $V_{IL}(\text{Max})$ | Loading with 50 Ω to -2.0V |
| V_{OLC} | Output LOW Voltage | | | -1610 | | | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL}(\text{Min})$ | |

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Parametric values specified at -4.2V to -4.8V .

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

DC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $T_C = 0^\circ C$ to $+85^\circ C$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|----------|--|------|------|--------------------------|---------|-------------------------|
| I_{IH} | Input HIGH Current B ₀ -B ₈ A ₀ A ₁ A ₂ | | | 215 215 285 310 | μA | $V_{IN} = V_{IH} (Max)$ |
| I_{EE} | Power Supply Current | -250 | -170 | -115 | mA | Inputs Open |

Ceramic Dual-In-Line Package AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A ₀ -A ₂ to F ₀ -F ₇ | 1.10 | 3.90 | 1.10 | 3.80 | 1.10 | 4.20 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay A ₀ -A ₂ to \bar{F}_8 | 0.90 | 3.20 | 1.00 | 3.10 | 1.00 | 3.60 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay B ₀ -B ₈ to F ₀ -F ₇ | 0.80 | 2.20 | 0.90 | 2.15 | 0.90 | 2.50 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay B ₈ to \bar{F}_8 | 0.80 | 2.00 | 0.90 | 2.00 | 0.90 | 2.50 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.50 | 0.45 | 2.40 | 0.45 | 2.60 | ns | <i>Figures 1 and 2</i> |

Cerpak AC Electrical Characteristics
 $V_{EE} = -4.2V$ to $-4.8V$, $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_C = 0^\circ C$ | | $T_C = +25^\circ C$ | | $T_C = +85^\circ C$ | | Units | Conditions |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|-------|------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay A ₀ -A ₂ to F ₀ -F ₇ | 1.10 | 3.70 | 1.10 | 3.60 | 1.10 | 4.00 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay A ₀ -A ₂ to \bar{F}_8 | 0.90 | 3.00 | 1.00 | 2.90 | 1.00 | 3.40 | ns | |
| t_{PLH} t_{PHL} | Propagation Delay B ₀ -B ₈ to F ₀ -F ₇ | 0.80 | 2.00 | 0.90 | 1.95 | 0.90 | 2.30 | ns | <i>Figures 1 and 2</i> |
| t_{PLH} t_{PHL} | Propagation Delay B ₈ to \bar{F}_8 | 0.80 | 1.80 | 0.90 | 1.80 | 0.90 | 2.30 | ns | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 0.45 | 2.40 | 0.45 | 2.30 | 0.45 | 2.50 | ns | <i>Figures 1 and 2</i> |

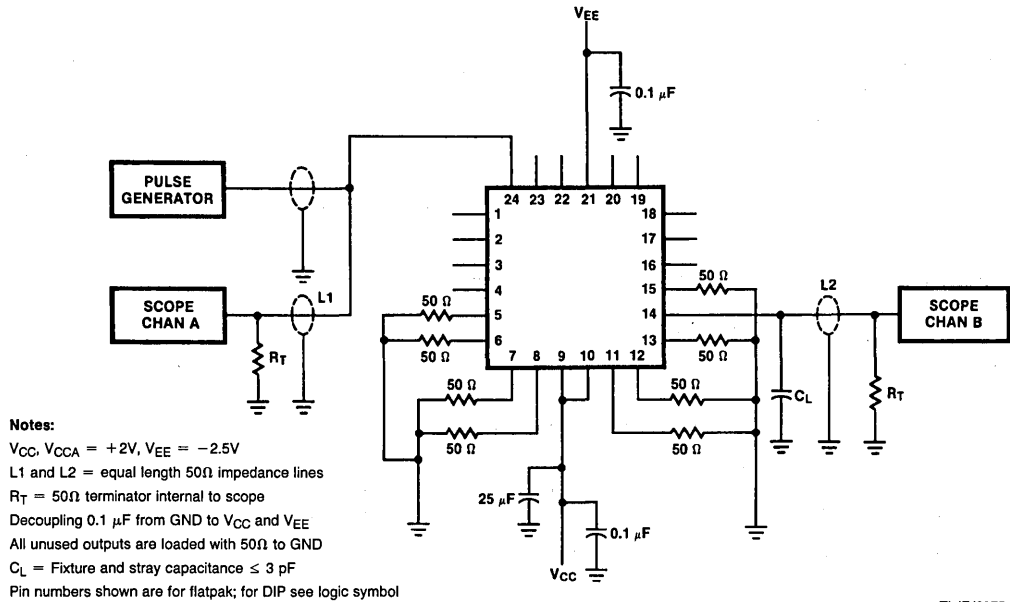


FIGURE 1. AC Test Circuit

TL/F/9875-6

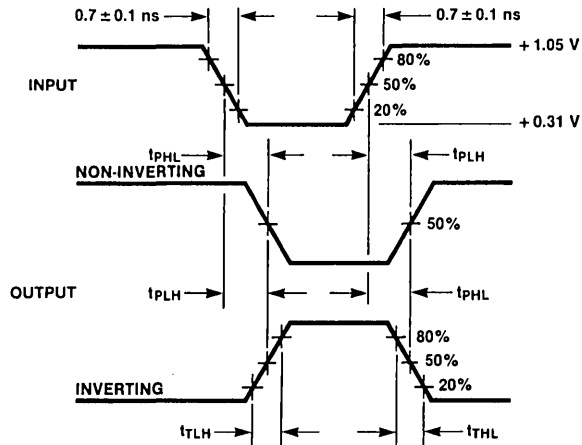


FIGURE 2. Propagation Delay and Transition Times

TL/F/9875-7

Application

F100183 is a 2 x 8-bit recode multiplier that performs parallel multiplication using two's complement arithmetic. In multiplying, the multiplier is partitioned into recode groups, then each recode group operates on the multiplicand to provide a partial product at the same time. The F100183, 2 x 8-bit recode multiplier provides partial products in 3.6 ns.

The F100182, 9-Bit Wallace Tree Adder combines the partial products to obtain the partial sum and partial carries in an additional 10.7 ns. Then the Carry Lookahead generator and 6-bit adder combine the results of a 16 x 16-bit multiply

for a total of 24.3 ns. The propagation delays and package count for implementing various size multipliers are listed in Tables I and II.

Multiplication of two's complement binary numbers is accomplished by first obtaining all the partial products. Then the weighted partial products are added together to yield the final result. In the Wallace Tree method of multiplication the sign bit is treated the same as the rest of the bits to obtain a signed result.

TABLE I. Propagation Delay Summation*

| Array Size | Recode Multiplier 100183 | Wallace Tree Adder 100182 | High-speed Adder 100180 | Carry Lookahead 100179 | = | Total (Max) Delay |
|----------------------------|--------------------------|---------------------------|-------------------------|------------------------|---|-------------------|
| 16 x 16 | 3.6 | 10.7 | 7.3 | 2.7 | = | 24.3 ns |
| 17 x 17 thru 24 x 24 | 3.6 | 21.4 | 7.3 | 2.7 | = | 35.0 ns |
| 25 x 25 thru 48 x 48 | 3.6 | 21.4 | 7.3 | 5.4 | = | 37.7 ns |
| 49 x 49 thru 72 x 72 | 3.6 | 21.4 | 7.3 | 8.1 | = | 40.4 ns |
| 73 x 73 | 3.6 | 32.1 | 7.3 | 10.8 | = | 53.8 ns |

*Worst case, Flatpak

Application (Continued)

TABLE II. Package Count

| | 100102 100117 | 100183 | 100182 | 100180 | 100179 | | Total |
|---------|------------------|--------|--------|--------|--------|---|-------|
| 16 x 16 | 6 | 16 | 32 | 6 | 2 | = | 62 |
| 18 x 18 | 7 | 27 | 38 | 6 | 2 | = | 70 |
| 24 x 24 | 9 | 36 | 60 | 8 | 2 | = | 115 |
| 32 x 32 | 11 | 64 | 96 | 11 | 4 | = | 186 |
| 36 x 36 | 13 | 80 | 116 | 12 | 4 | = | 225 |
| 64 x 64 | 24 | 256 | 328 | 22 | 6 | = | 634 |

For a quick review of the twos complement number format see Table III. Note that subtraction is accomplished by adding the negative number. An example of changing from a positive number to a negative number is shown.

1011 negative number-5

0100 bits inverted

+0001 add one

0101 Results 5

TABLE III. Twos Complement Format

| Sign Bit | Magnitude | | | Decimal Number |
|----------|----------------|----------------|----------------|----------------|
| | 2 ² | 2 ¹ | 2 ⁰ | |
| 0 | 1 | 1 | 1 | +7 |
| 0 | 1 | 1 | 0 | +6 |
| 0 | 1 | 0 | 1 | +5 |
| 0 | 1 | 0 | 0 | +4 |
| 0 | 0 | 1 | 1 | +3 |
| 0 | 0 | 1 | 0 | +2 |
| 0 | 0 | 0 | 1 | +1 |
| 0 | 0 | 0 | 0 | +0 |
| 1 | 1 | 1 | 1 | -1 |
| 1 | 1 | 1 | 0 | -2 |
| 1 | 1 | 0 | 1 | -3 |
| 1 | 1 | 0 | 0 | -4 |
| 1 | 0 | 1 | 1 | -5 |
| 1 | 0 | 1 | 0 | -6 |
| 1 | 0 | 0 | 1 | -7 |
| 1 | 0 | 0 | 0 | -8 |

Multiplication Algorithm

In the multiplication algorithm used, the multiplier ($Y_n \dots Y_0$) is partitioned into recode groups and each recode group operates on the multiplicand ($X_n \dots X_0$) as in *Figure 4*. The F100183, 2 x 8-bit recode multiplier partitions the multiplier ($X_n \dots X_0$) into groups of eight and the multiplicand ($Y_n \dots Y_0$) into groups of two. Each recode group is two bits wide but requires three bits to determine the partial products. Table IV lists the significance of the various recode groups. The partial product is ± 0 , \pm multiplicand, or \pm two times the multiplicand. A forced zero is required to establish the least significant bit of the first recode group. By connecting recode multipliers in parallel the partial products are available at the same time. The weighted partial products ($A_n \dots A_0$, $B_n \dots B_0$) ... are added together using F100182, 9-bit Wallace Tree Adders. The results of the partial sum and partial

carry are combined together using Carry Lookahead generators and 6-bit adders. An example of using recode multiplication is shown in *Figure 3*: multiplier (117₁₀) 01110101 times multiplicand (105₁₀) 01101001. The first recode group 010 requires adding the multiplicand; the second recode group 010 also requires adding the multiplicand; the third group 110 requires subtracting the multiplicand (the same as inverting each digit and adding 1); the fourth group 011 requires adding twice the multiplicand. Combining the results of four groups, 12285₁₀, we have the correct answer.

TABLE IV. Recode Product

| Recode Group | | | Recode Value | Partial Product |
|--------------|-------|-----------|--------------|---------------------------------|
| Y_{i+1} | Y_i | Y_{i-1} | | |
| 0 | 0 | 0 | +0 | Add zero |
| 0 | 0 | 1 | +1 | Add multiplicand |
| 0 | 1 | 0 | +1 | Add multiplicand |
| 0 | 1 | 1 | +2 | Add twice the multiplicand |
| 1 | 0 | 0 | -2 | Subtract twice the multiplicand |
| 1 | 0 | 1 | -1 | Subtract the multiplicand |
| 1 | 1 | 0 | -1 | Subtract the multiplicand |
| 1 | 1 | 1 | -0 | Subtract zero |

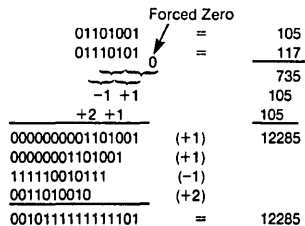


FIGURE 3. Recode Multiplication Example

TL/F/9875-8

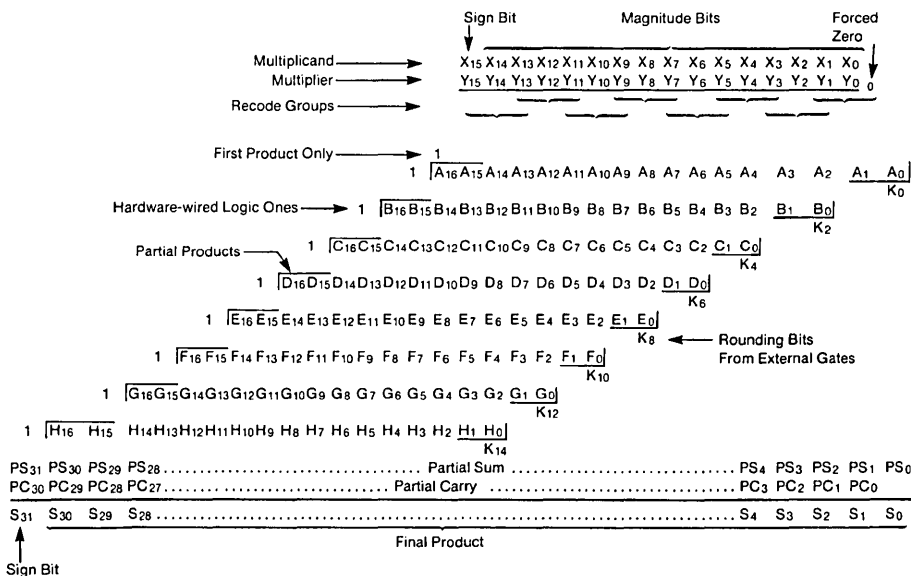


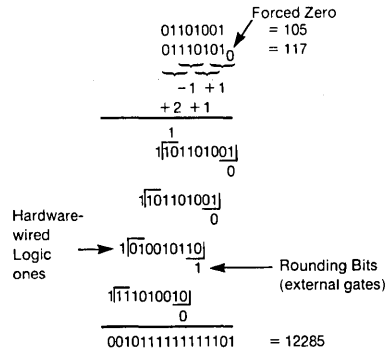
FIGURE 4. 16 x 16 Multiply

TL/F/9875-9

Hardware Implementation

For the hardware implementation of the F100183 recode multiplier the sign bit is connected to the B_8 input, and B_7 through B_0 are the magnitude bits. Two extend the word length greater than eight bits, the B_0 and B_8 inputs of adjacent devices are connected together (see *Figure 7*). The device outputs F_0 through F_7 are used as the partial products; these correspond to A_0 through A_7 , or A_8 through A_{15} , or B_0 through B_7 , etc. To reduce the hardware, the \bar{F}_8 bit (A_{16} in *Figure 7*) is used as the sign bit of the partial product. The sign bits are extended by using hardware wired logic "1s". The ones are located in front of each partial product with an extra "1" at the sign bit of the first partial product as in *Figure 4*. The logic "1s" are wired as inputs into the Wallace Tree Adders as shown in *Figure 6*. If the recode group requires the multiplicand to be added, then the F100183 outputs the correct partial products to be added. But when the recode group requires that the multiplicand be subtracted, then the F100183 outputs the ones complement. External gates are required to generate a "1" to be added to the ones complement to complete the twos complement for the partial product (*Figure 7*). These external gates generate the rounding bits, $K_0 \dots K_n$, which are input to the Wallace Tree Adder. *Figures 4, 6* and *7* show the location. An example of multiplication which has the rounding bits and the hardware wired logic "1s" is shown in *Figure 5*.

The weighted partial products are added together using F100182, 9-bit Wallace Tree Adders as shown in *Figure 6*. The output is a partial sum and partial carry which can be reduced to the final product using Carry Lookahead and 6-bit adders. See *Figure 8*.



TL/F/9875-10

FIGURE 5. Example of Multiplication Using Rounding Bits

Hardware Implementation (Continued)

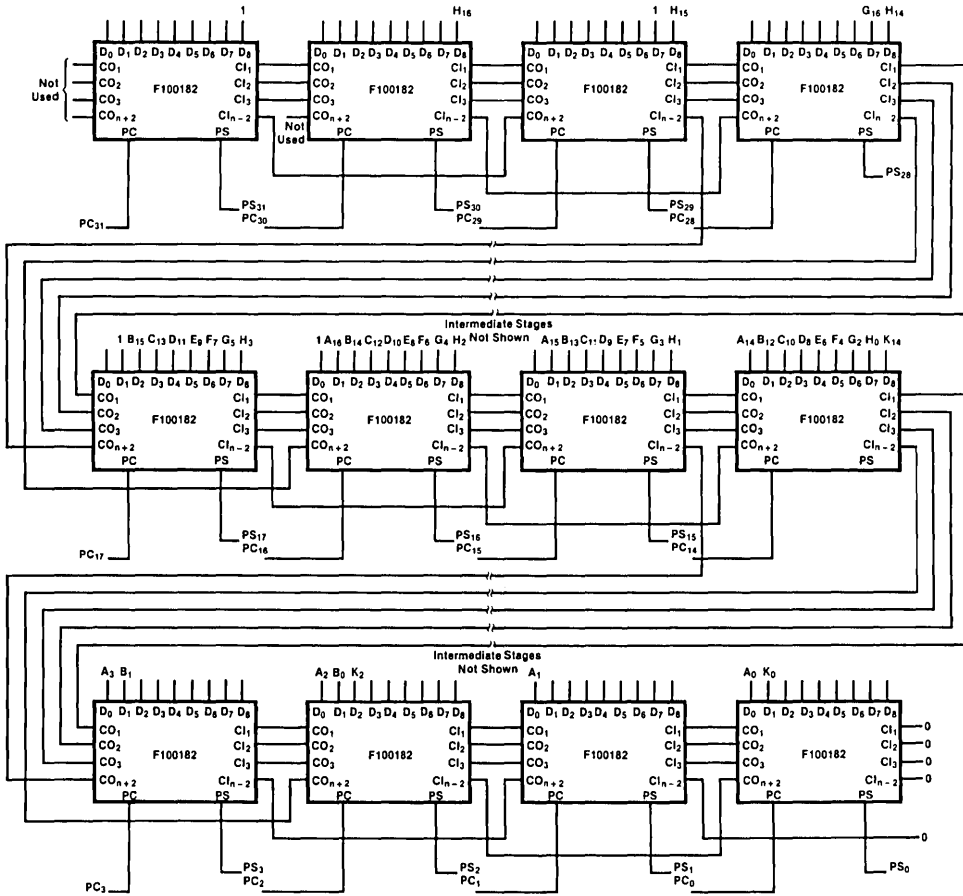


FIGURE 6. F100182 Hook-up for 16 x 16 Multiplier

TL/F/9875-11

Hardware Implementation (Continued)

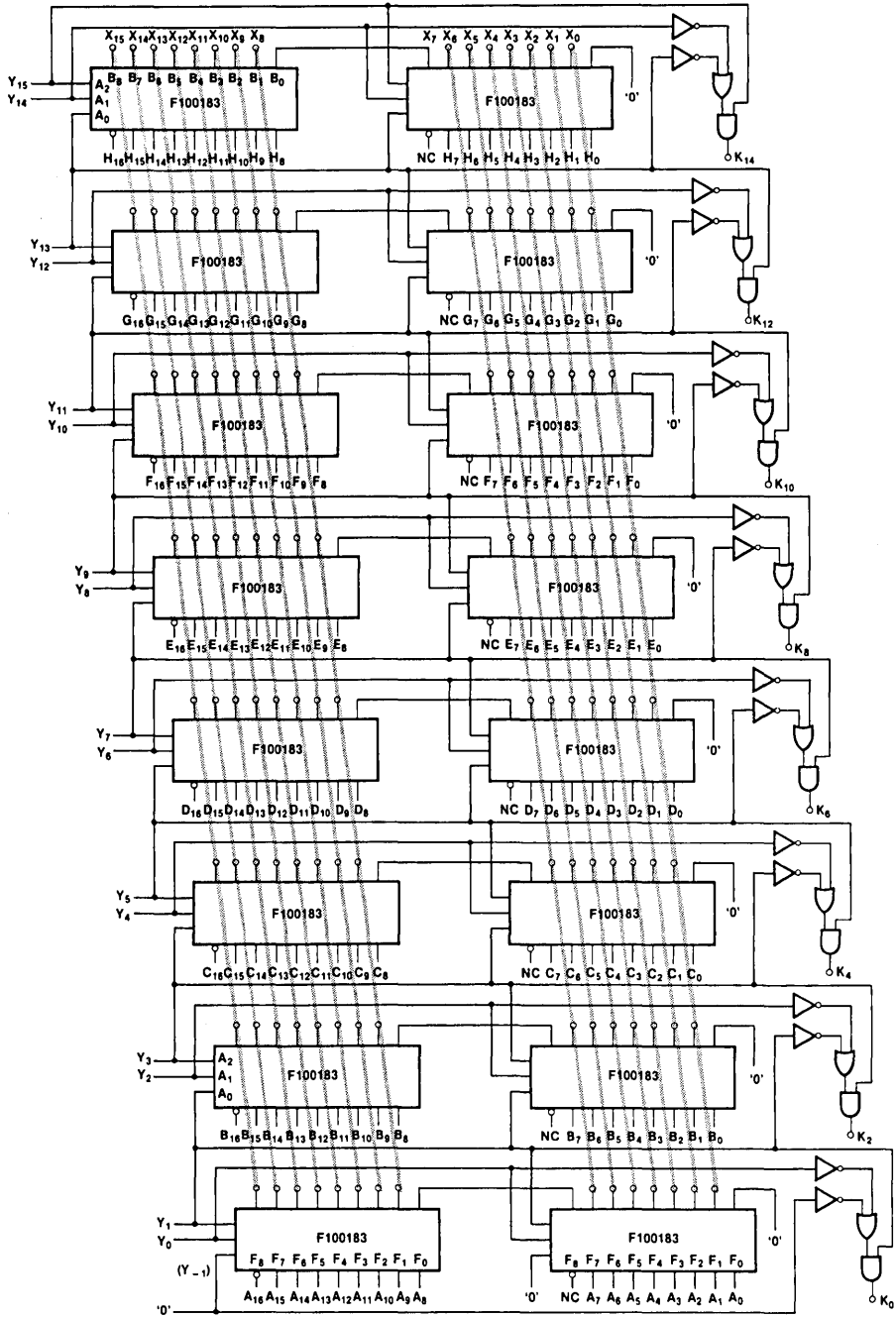


FIGURE 7. F100183 Hook-Up for 16 x 16 Multiplier

TL/F/9875-12

Hardware Implementation (Continued)

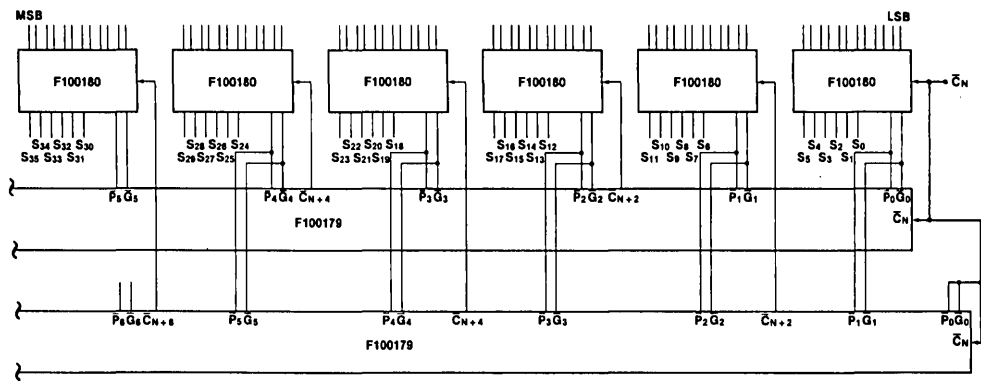


FIGURE 8. Final Summation for 16 x 16 Multiplier

TL/F/9875-13



F100250 Quint Full Duplex Line Transceiver

General Description

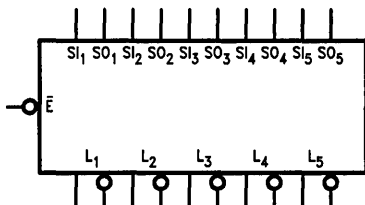
The F100250 is a quint line transceiver capable of simultaneously transmitting and receiving differential mode signals on a twisted pair line. Each transceiver has a signal input S_{IN} , a signal output S_{OUT} and two differential line inputs/outputs L and \bar{L} . Signals received from the lines L and \bar{L} can be stored in an internal latch. The line outputs are designed to drive twisted pair lines. The ENABLE input is common to all five transceivers.

Features

- Full duplex operation
- Common mode noise immunity of $\pm 1V$

Ordering Code: See Section 8

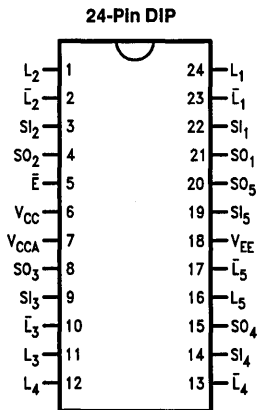
Logic Symbol



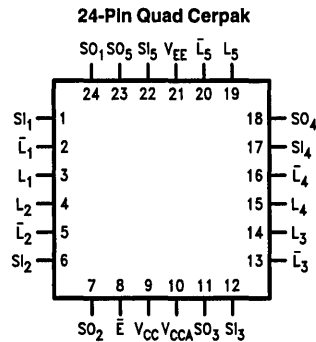
TL/F/9876-3

| Pin Names | Description |
|------------------|----------------------------------|
| \bar{E} | Common Enable |
| S_{in} | 100K Signal Inputs |
| S_{On} | 100K Signal Outputs |
| L_n, \bar{L}_n | Differential Line Inputs/Outputs |

Connection Diagrams

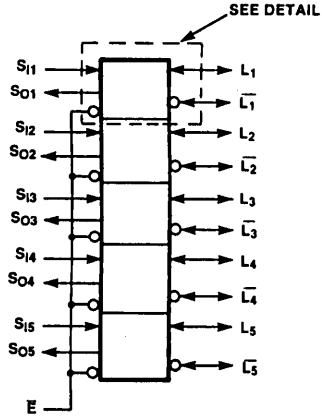


TL/F/9876-1



TL/F/9876-2

Logic Diagram



TL/F/9876-6

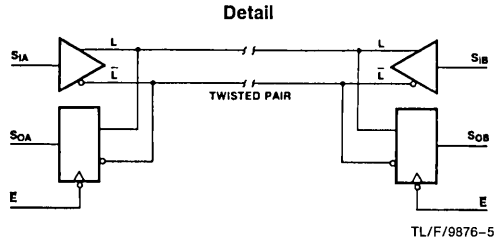


FIGURE 1. Interconnection of Two F100250 Circuits, Duplex Mode Operation

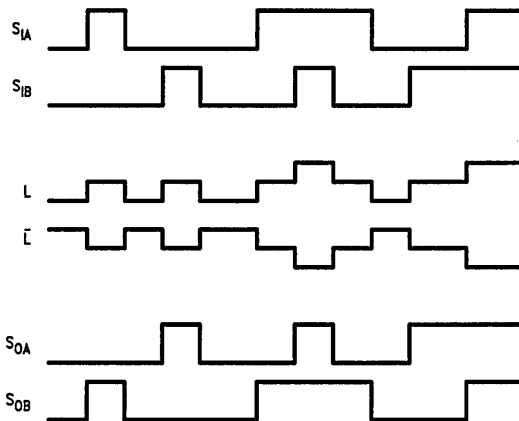
Truth Table

| \bar{E} | S_{IA} | S_{IB} | S_{OA} | S_{OB} | L | \bar{L} |
|-----------|----------|----------|---------------|---------------|-----------------|-----------------|
| H | X | X | $S_{OA}(n-1)$ | $S_{OB}(n-1)$ | * | * |
| L | L | L | L | L | U_L | U_H |
| L | L | H | H | L | $(U_L + U_H)/2$ | $(U_L + U_H)/2$ |
| L | H | L | L | H | $(U_L + U_H)/2$ | $(U_L + U_H)/2$ |
| L | H | H | H | H | U_H | U_L |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 n-1 = Previous State
 * = Dependent on S_{IA} and S_{IB}

$U_L \approx -1.27V$
 $U_H \approx -0.27V$
 $(U_L + U_H)/2 \approx -0.77V$

Functional Waveform



TL/F/9876-15

Absolute Maximum Ratings

Above which the useful life may be impaired. (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature: -65°C to +150°C
Maximum Junction Temperature (T_J): +150°C

Case Temperature under Bias (T_C): 0°C to +85°C
V_{EE} Pin Potential to Ground Pin: -7.0V to +0.5V
Input Voltage (DC): V_{EE} to +0.5V
Output Current (DC Output HIGH): -50 mA
Operating Range (Note 2): -5.7V to -4.2V

DC Electrical Characteristics

V_{EE} = -4.2V to -4.8V unless otherwise specified, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-----------------|--|------|-----|------------|----------|--|
| I _{IH} | Input HIGH Current S _{In} E | | | 200 250 | μA μA | V _{IN} = V _{IH(Max)} |
| I _{EE} | Power Supply Current | -300 | | -180 | mA | Inputs Open |

DC Electrical Characteristics

V_{EE} = -4.5V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) |
|------------------|--------------------------|-------|-------|-------|-------|---|
| V _{OH} | Output HIGH Voltage | -1025 | -955 | -880 | mV | Loading with 50Ω to -2.0V V _{IN} = V _{IH(Max)} or V _{IL(Min)} V _{IN} = V _{IH(Min)} or V _{IL(Max)} |
| V _{OL} | Output LOW Voltage | -1810 | -1705 | -1620 | mV | |
| V _{OHc} | Output HIGH Voltage | -1035 | | | mV | |
| V _{OLc} | Output LOW Voltage | | | -1610 | mV | |
| V _{KH} | Line Output HIGH Voltage | -370 | | -220 | mV | No Load |
| V _{KL} | Line Output LOW Voltage | -1400 | | -1090 | mV | V _{IN} = V _{IH(Max)} or V _{IL(Min)} |
| V _{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL(Min)} |

DC Electrical Characteristics

V_{EE} = -4.2V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C (Note 3)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) |
|------------------|--------------------------|-------|-----|-------|-------|---|
| V _{OH} | Output HIGH Voltage | -1020 | | -870 | mV | Loading with 50Ω to -2.0V V _{IN} = V _{IH(Max)} or V _{IL(Min)} V _{IN} = V _{IH(Min)} or V _{IL(Max)} |
| V _{OL} | Output LOW Voltage | -1810 | | -1605 | mV | |
| V _{OHc} | Output HIGH Voltage | -1030 | | | mV | |
| V _{OLc} | Output LOW Voltage | | | -1595 | mV | |
| V _{KH} | Line Output HIGH Voltage | -350 | | -200 | mV | No Load |
| V _{KL} | Line Output LOW Voltage | -1300 | | -990 | mV | V _{IN} = V _{IH(Max)} or V _{IL(Min)} |
| V _{IH} | Input HIGH Voltage | -1150 | | -870 | mV | Guaranteed HIGH Signal for All Inputs |
| V _{IL} | Input LOW Voltage | -1810 | | -1475 | mV | Guaranteed LOW Signal for All Inputs |
| I _{IL} | Input LOW Current | 0.50 | | | μA | V _{IN} = V _{IL(Min)} |

DC Electrical Characteristics

 $V_{EE} = -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0^{\circ}C \text{ to } +85^{\circ}C \text{ (Note 3)}$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions (Note 4) | |
|-----------|--------------------------|-------|-----|-------|-------|--|------------------------------|
| V_{OH} | Output HIGH Voltage | -1035 | | -880 | mV | $V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ | Loading with 50Ω to -2.0V |
| V_{OL} | Output LOW Voltage | -1830 | | -1620 | mV | | |
| V_{OHC} | Output HIGH Voltage | -1045 | | | mV | $V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$ | |
| V_{OLC} | Output LOW Voltage | | | -1610 | mV | | |
| V_{KH} | Line Output HIGH Voltage | -400 | | -250 | mV | No Load | |
| V_{KL} | Line Output LOW Voltage | -1500 | | -1190 | mV | $V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ | |
| V_{IH} | Input HIGH Voltage | -1165 | | -880 | mV | Guaranteed HIGH Signal for All Inputs | |
| V_{IL} | Input LOW Voltage | -1830 | | -1490 | mV | Guaranteed LOW Signal for All Inputs | |
| I_{IL} | Input LOW Current | 0.50 | | | μA | $V_{IN} = V_{IL(Min)}$ | |

Note 1: Unless specified otherwise on individual data sheet.

Note 2: Parametric values specified at -4.2V to -4.8V.

Note 3: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 4: Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Ceramic Dual-In-Line Package AC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0^{\circ}C \text{ to } +85^{\circ}C$

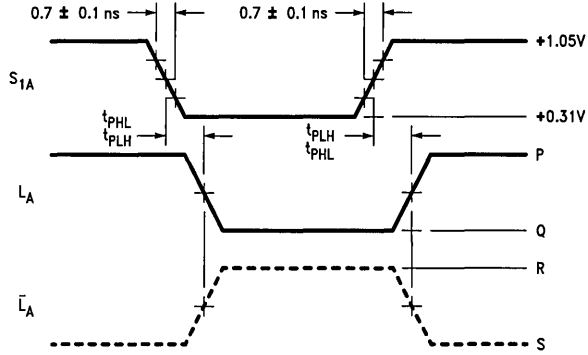
| Symbol | Parameter | $T_C = 0^{\circ}C$ | | $T_C = +25^{\circ}C$ | | $T_C = +85^{\circ}C$ | | Units | Conditions |
|------------------------|--|--------------------|-----|----------------------|-----|----------------------|-----|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay S_1 to L, \bar{L} | 1.1 | 2.4 | 1.1 | 2.4 | 1.2 | 2.6 | ns | Figures 2 and 4 |
| t_{PLH} t_{PHL} | Propagation Delay L, \bar{L} to S_0 | 1.2 | 2.8 | 1.2 | 2.9 | 1.3 | 3.0 | ns | Figures 3 and 5 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to S_0 | 1.2 | 2.6 | 1.2 | 2.7 | 1.3 | 2.9 | ns | Figures 3 and 5 |
| t_{THL} t_{TLH} | Transition Time 20% to 80%, 80% to 20% | 0.5 | 2.0 | 0.5 | 2.0 | 0.5 | 2.0 | ns | |
| t_S | Setup Time L, \bar{L} | 1.3 | | 1.3 | | 1.5 | | ns | Figure 3 |
| t_H | Hold Time L, \bar{L} | 1.3 | | 1.3 | | 1.5 | | ns | |

Cerpak AC Electrical Characteristics

 $V_{EE} = -4.2V \text{ to } -4.8V, V_{CC} = V_{CCA} = GND, T_C = 0^{\circ}C \text{ to } +85^{\circ}C$

| Symbol | Parameter | $T_C = 0^{\circ}C$ | | $T_C = +25^{\circ}C$ | | $T_C = +85^{\circ}C$ | | Units | Conditions |
|------------------------|--|--------------------|-----|----------------------|-----|----------------------|-----|-------|-----------------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{PLH} t_{PHL} | Propagation Delay S_1 to L, \bar{L} | 1.1 | 2.2 | 1.1 | 2.2 | 1.2 | 2.4 | ns | Figures 2 and 4 |
| t_{PLH} t_{PHL} | Propagation Delay L, \bar{L} to S_0 | 1.2 | 2.6 | 1.2 | 2.7 | 1.3 | 2.8 | ns | Figures 3 and 5 |
| t_{PLH} t_{PHL} | Propagation Delay \bar{E} to S_0 | 1.2 | 2.4 | 1.2 | 2.5 | 1.3 | 2.7 | ns | Figures 3 and 5 |
| t_{THL} t_{TLH} | Transition Time 20% to 80%, 80% to 20% | 0.5 | 1.9 | 0.5 | 1.9 | 0.5 | 1.9 | ns | |
| t_S | Setup Time L, \bar{L} | 1.3 | | 1.3 | | 1.5 | | ns | Figure 3 |
| t_H | Hold Time L, \bar{L} | 1.3 | | 1.3 | | 1.5 | | ns | |

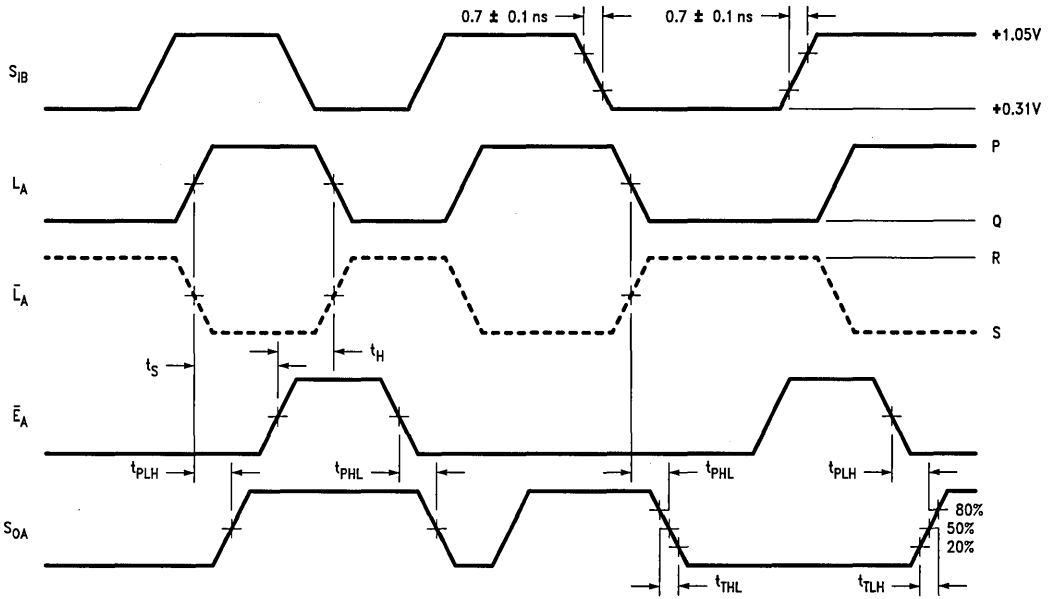
Switching Waveforms



TL/F/9876-8

Notes: $S_{1B} = L$ then $P = (U_L + U_H)/2, Q = U_L, R = U_H, S = (U_L + U_H)/2$
 $S_{1B} = H$ then $P = U_H, Q = (U_L + U_H)/2, R = (U_L + U_H)/2, S = U_L$ } L, \bar{L} loaded with another F100250

FIGURE 2. S_1 to Differential Line



TL/F/9876-9

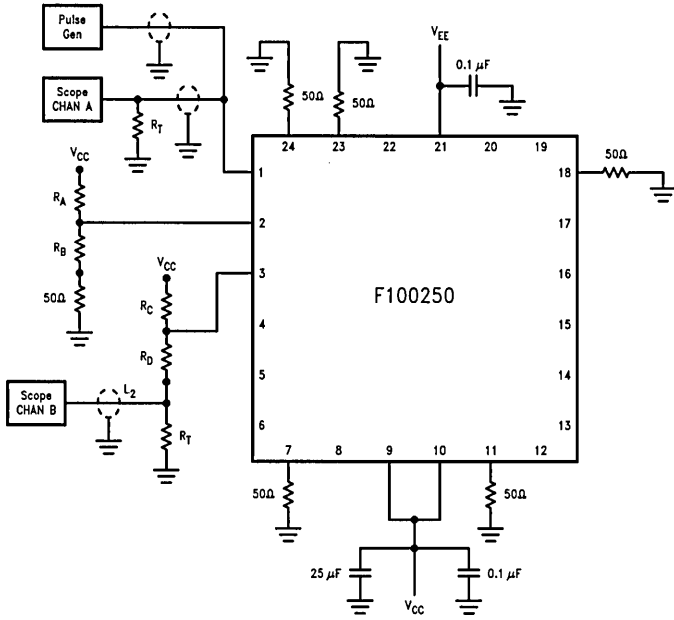
Notes: $S_{1A} = L$ then $P = (U_L + U_H)/2, Q = U_L, R = U_H, S = (U_L + U_H)/2$
 $S_{1A} = H$ then $P = U_H, Q = (U_L + U_H)/2, R = (U_L + U_H)/2, S = U_L$ } L, \bar{L} loaded with another F100250

t_S is the minimum time before the transition of the enable that information must be present at the data input.

t_H is the minimum time before the transition of the enable that information must remain unchanged at the data input.

FIGURE 3. Differential Line to S_0

Test Circuitry

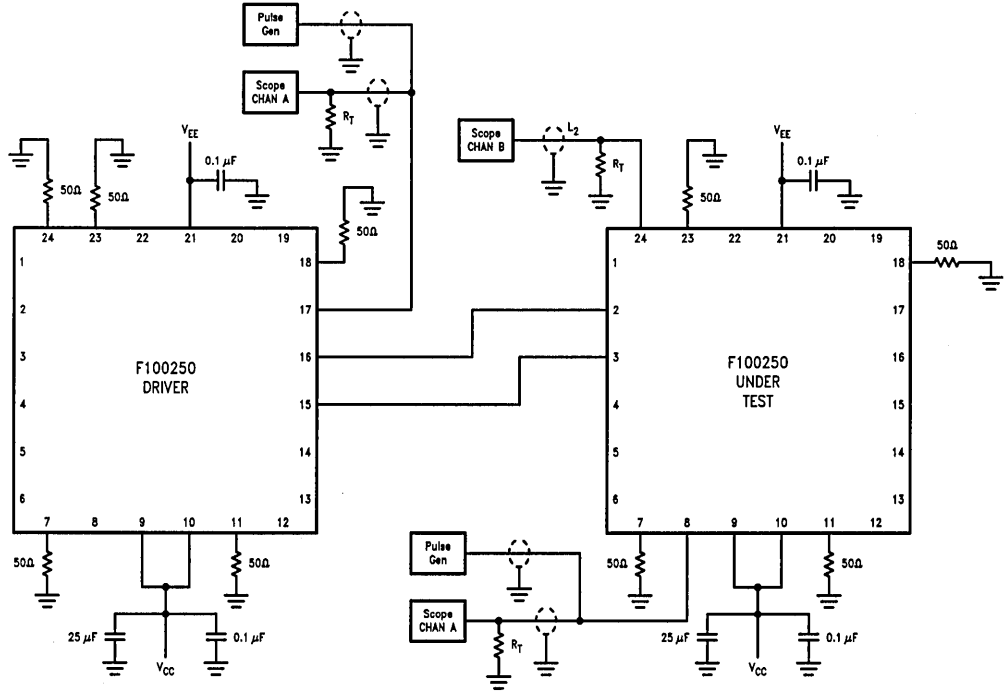


Notes:

- V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V
- L1 and L2 = equal length 50Ω impedance lines.
- R_T = 50Ω terminator internal to scope.
- Decoupling 0.1 μF from GND to V_{CC} and V_{EE}.
- All unused outputs are loaded with 50Ω to GND.
- C_L = fixture and stray capacitance ≤ 3 pF.
- L and L̄ terminated by F100250 or Thevenin equivalent.
- Signal levels will be a percentage of full swing if using equivalent network.
- R_A = 91Ω, R_B = 500Ω, R_C = 220Ω, R_D = 71.5Ω for S_{IB} = L.
- R_A = 220Ω, R_B = 71.5Ω, R_C = 91Ω, R_D = 500Ω for S_{IB} = H.

TL/F/9876-13

FIGURE 4. AC Test Circuit SI to Differential Line



TL/F/9876-14

Notes:

- VCC, VCCA = +2V, VEE = -2.5V
- L1 and L2 = equal length 50Ω impedance lines.
- RT = 50Ω terminator internal to scope.
- Decoupling 0.1 μF from GND to VCC and VEE.
- All unused outputs are loaded with 50Ω to GND.
- CL = fixture and stray capacitance ≤ 3 pF.

FIGURE 5. AC Test Circuit Differential Line to S₀ and E̅ to S₀



Section 4
11C Datasheets



Section 4 Contents

| | |
|---|------|
| 11C01 Dual Input OR/NOR Gate | 4-3 |
| 11C05 1 GHz Divide-by-Four Counter | 4-6 |
| 11C06 750 MHz D-Type Flip-Flop | 4-10 |
| 11C70 Master-Slave D-Type Flip-Flop | 4-14 |
| 11C90/11C91 650 MHz Prescalers | 4-20 |

11C01

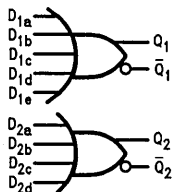
Dual 5-4 Input OR/NOR Gate

General Description

The 11C01 is a voltage-compensated ECL dual 5-4 input OR/NOR gate. The circuit has standard internal voltage compensation with DC parameters identical to 10K ECL devices.

Ordering Code: See Section 8

Logic Symbol

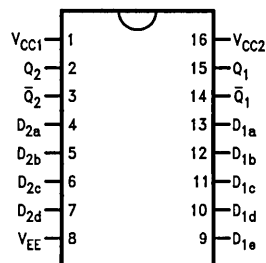


TL/F/9888-2

| Pin Names | Description |
|---|-------------|
| D _{1a} -D _{1e} , D _{2a} -D _{2d} | Data Inputs |
| Q ₁ , Q ₁ \bar , Q ₂ , Q ₂ \bar | Outputs |

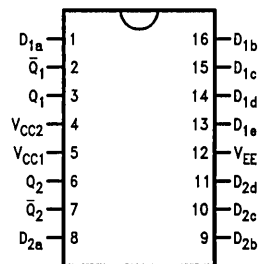
Connection Diagrams

16-Pin DIP



TL/F/9888-1

16-Pin Flatpak



TL/F/9888-3

Truth Tables

| In | | | | | Out | |
|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|-----------------------|
| D _{1a} | D _{1b} | D _{1c} | D _{1d} | D _{1e} | Q ₁ | Q ₁ \bar |
| L | L | L | L | L | L | H |
| H | X | X | X | X | H | L |
| X | H | X | X | X | H | L |
| X | X | H | X | X | H | L |
| X | X | X | H | X | H | L |
| X | X | X | X | H | H | L |

| In | | | | Out | |
|-----------------|-----------------|-----------------|-----------------|----------------|-----------------------|
| D _{2a} | D _{2b} | D _{2c} | D _{2d} | Q ₂ | Q ₂ \bar |
| L | L | L | L | L | H |
| H | X | X | X | H | L |
| X | H | X | X | H | L |
| X | X | H | X | H | L |
| X | X | X | H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|------------------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | +150°C |
| Supply Voltage Range | -7.0V to GND |
| Input Voltage (DC) | V _{EE} to GND |
| Output Current (DC Output HIGH) | -50 mA |
| Operating Range | -5.5V to -4.75V |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Recommended Operating Conditions

| | Min | Typ | Max | Units |
|---------------------------------------|------|------|-------|-------|
| Supply Voltage (V _{EE}) | -5.5 | -5.2 | -4.75 | V |
| Ambient Temperature (T _A) | 0 | | +75 | °C |

DC Electrical Characteristics

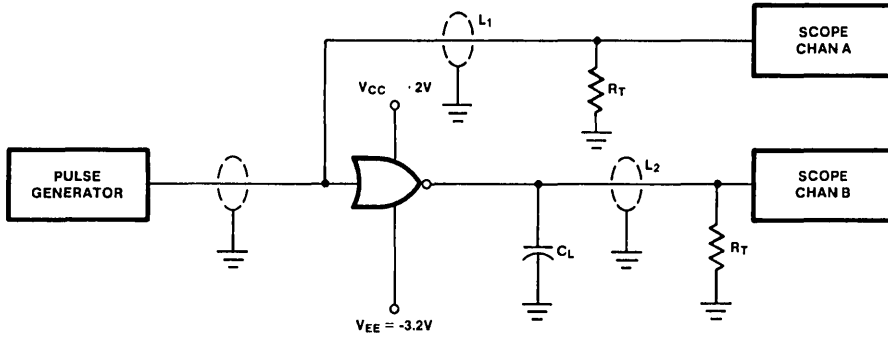
V_{EE} = -5.2V, V_{CC} = GND

| Symbol | Parameter | Min | Typ | Max | Units | T _A | Conditions |
|------------------|----------------------|-------------------------|-----|-------------------------|-------|-----------------------|--|
| V _{OH} | Output Voltage HIGH | -1000 -960 -900 | | -840 -810 -720 | mV | 0°C +25°C +75°C | V _{IN} = V _{IH} (Max) or V _{IL} (Min) per Truth Table Loading is 50Ω to -2.0V |
| V _{OL} | Output Voltage LOW | -1870 -1850 -1830 | | -1665 -1650 -1625 | mV | 0°C +25°C +75°C | |
| V _{OHC} | Output Voltage HIGH | -1020 -980 -920 | | | mV | 0°C +25°C +75°C | |
| V _{OLC} | Output Voltage LOW | | | -1645 -1630 -1605 | mV | 0°C +25°C +75°C | |
| V _{IH} | Input Voltage HIGH | -1145 -1105 -1045 | | -840 -810 -720 | mV | 0°C +25°C +75°C | Guaranteed Input Voltage HIGH for All Inputs |
| V _{IL} | Input Voltage LOW | -1870 -1850 -1830 | | -1490 -1475 -1450 | mV | 0°C +25°C +75°C | Guaranteed Input Voltage LOW for All Inputs |
| I _{IH} | Input Current HIGH | | | 350 | μA | +25°C | V _{IN} = V _{IH} (Max) |
| I _{IL} | Input Current LOW | 0.5 | | | μA | +25°C | V _{IN} = V _{IL} (Min) |
| I _{EE} | Power Supply Current | -30 | -24 | | mA | +25°C | Inputs and Outputs Open |

AC Electrical Characteristics

V_{EE} = -5.2V, T_A = +25°C

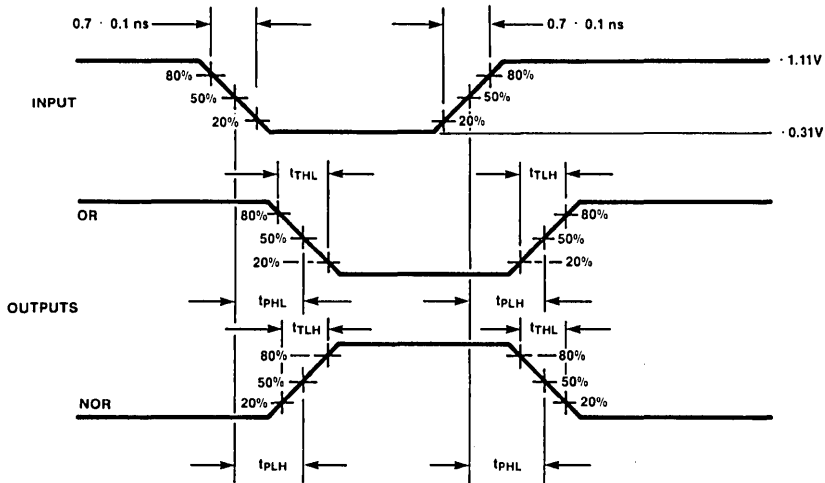
| Symbol | Parameter | Flatpak | | | DIP | | | Units | Conditions |
|------------------|---|---------|-----|------|------|------|------|-------|--------------|
| | | Min | Typ | Max | Min | Typ | Max | | |
| t _{PLH} | Propagation Delay LOW to HIGH | 0.45 | 0.7 | 0.95 | 0.60 | 0.90 | 1.15 | ns | See Figure 1 |
| t _{PHL} | Propagation Delay HIGH to LOW | 0.45 | 0.7 | 0.95 | 0.60 | 0.90 | 1.15 | ns | |
| t _{TLH} | Output Transition Time LOW to HIGH (20% to 80%) | | 0.7 | 0.95 | | 0.90 | 1.15 | ns | |
| t _{THL} | Output Transition Time HIGH to LOW (80% to 20%) | | 0.7 | 0.95 | | 0.90 | 1.15 | ns | |



TL/F/9888-4

Notes:

- L1 and L2 = equal length 50Ω impedance lines
- $R_T = 50\Omega$ Termination of scope
- Decoupling $0.1\ \mu\text{F}$ from GND to V_{EE} and V_{CC}
- $C_L \leq 3\ \text{pF}$



TL/F/9888-5

Notes:

- Jig setup with no circuit under test
- $V_{CC1} = V_{CC2} = +2.0\text{V}$
- $V_{EE} = -3.2\text{V}$

FIGURE 1. Switching Circuit and Waveforms



11C05 1 GHz Divide-By-Four Counter

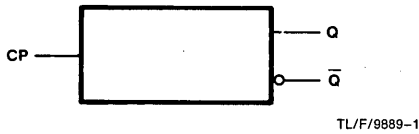
General Description

The 11C05 is an ECL Divide-By-Four Counter with a maximum operating frequency above 1 GHz over the 0°C to +75°C temperature range. The input may be DC or AC (capacitively) coupled to the signal source. The emitter follower

outputs (Q and \bar{Q}) are capable of driving 50Ω lines. The outputs are voltage-compensated and provide standard ECL output levels.

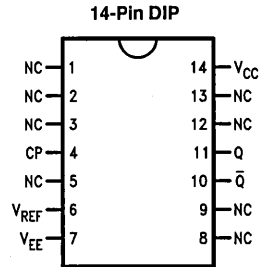
Ordering Code: See Section 8

Logic Symbol

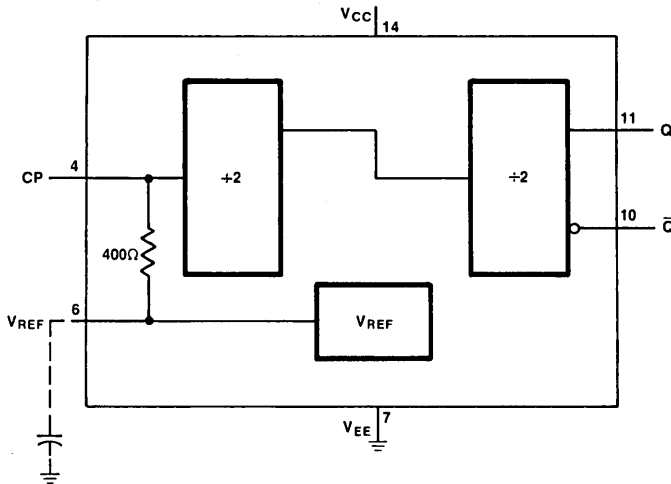


| Pin Names | Description |
|------------------|-----------------|
| CP | Clock Input |
| V _{REF} | Reference Input |
| Q, \bar{Q} | Counter Outputs |

Connection Diagram



Logic Diagram



Absolute Maximum Ratings

Above which the useful life may be impaired

| | |
|--|------------------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | +150°C |
| Supply Voltage Range | -7.0V to GND |
| Input Voltage (DC) | V _{EE} to GND |
| Output Current (DC Output HIGH) | -50 mA |
| Operating Range | -5.5V to -4.75V |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Recommended Operating Conditions

| | Min | Typ | Max |
|---------------------------------------|--------|-------|--------|
| Supply Voltage (V _{EE}) | | | |
| Commercial | -5.25V | -5.0V | -4.75V |
| Military | -5.5V | -5.0V | -4.75V |
| Ambient Temperature (T _A) | | | |
| Commercial | 0°C | | +75°C |
| Military | -55°C | | +125°C |

Commercial DC Electrical CharacteristicsV_{EE} = 5.0V, V_{CC} = GND

| Symbol | Parameter | Min | Typ | Max | Units | T _A | Conditions |
|------------------|-------------------------|-------|-------|-------|-------|----------------|--|
| V _{OH} | Output Voltage HIGH | -1060 | -995 | -910 | mV | 0°C | V _{IN} = V _{IH} or V _{IL} , Loading 50Ω to -2V |
| | | -1025 | -960 | -880 | mV | +25°C | |
| | | -980 | -910 | -830 | mV | +75°C | |
| V _{OL} | Output Voltage LOW | -1810 | -1705 | -1620 | mV | 0°C to +75°C | |
| V _{IH} | Input Voltage HIGH | -2.45 | | | V | 0°C | Guaranteed Input HIGH |
| | | -2.50 | | | V | +25°C | |
| | | -2.60 | | | V | +75°C | |
| V _{IL} | Input Voltage LOW | | | -3.25 | V | 0°C | Guaranteed Input LOW |
| | | | | -3.30 | V | +25°C | |
| | | | | -3.40 | V | +75°C | |
| I _{EE} | Power Supply Current | -90 | -65 | | mA | +25°C | Input Open |
| V _{EE} | Supply Voltage Range | -5.25 | -5.0 | -4.75 | V | 0°C to +75°C | |
| V _{REF} | Input Reference Voltage | | -2.9 | | V | +25°C | |

Military DC Electrical CharacteristicsV_{EE} = -5.0V, V_{CC} = GND

| Symbol | Parameter | Min | Typ | Max | Units | T _A | Conditions |
|------------------|-------------------------|-------|-------|-------|-------|-----------------|---|
| V _{OH} | Output Voltage HIGH | -1100 | -1030 | -950 | mV | -55°C | V _{IN} = V _{IH} or V _{IL} , Loading 100Ω to -2V |
| | | -980 | -910 | -820 | mV | +25°C | |
| | | -910 | -820 | -720 | mV | +125°C | |
| V _{OL} | Output Voltage LOW | -1810 | -1705 | -1620 | mV | -55°C to +125°C | |
| V _{IH} | Input Voltage HIGH | -2.35 | | | V | -55°C | Guaranteed Input HIGH |
| | | -2.50 | | | V | +25°C | |
| | | -2.70 | | | V | +125°C | |
| V _{IL} | Input Voltage LOW | | | -3.15 | V | -55°C | Guaranteed Input LOW |
| | | | | -3.30 | V | +25°C | |
| | | | | -3.50 | V | +125°C | |
| I _{EE} | Power Supply Current | -90 | -65 | | mA | +25°C | Input Open |
| V _{EE} | Supply Voltage Range | -5.5 | -5.0 | -4.75 | V | -55°C to +125°C | |
| V _{REF} | Input Reference Voltage | | -2.9 | | V | +25°C | |

Commercial and Military AC Electrical Characteristics

$V_{EE} = -5V$, $V_{CC} = GND$, $T_A = -55^\circ C$ to $+125^\circ C$ unless otherwise noted

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-------------|------------------------------------|------|-----|-----|------------|---|
| f_{COUNT} | Maximum Sinusoidal Input Frequency | 1000 | | | MHz | 0°C to +75°C |
| | | 950 | | | | -55°C to +125°C |
| f_{COUNT} | Minimum Sinusoidal Input Frequency | | 25 | | MHz | AC Coupled 800 mV Peak-to-Peak Input (Note 2) |
| SR_{MIN} | Slew Rate of Squarewave | | 50 | | V/ μs | (Note 1) |

Note 1: Very low frequency operation is possible as long as sufficient slew rate of the input pulse edges is maintained.

Note 2: Input drive shall not exceed 1.5V peak-to-peak max.

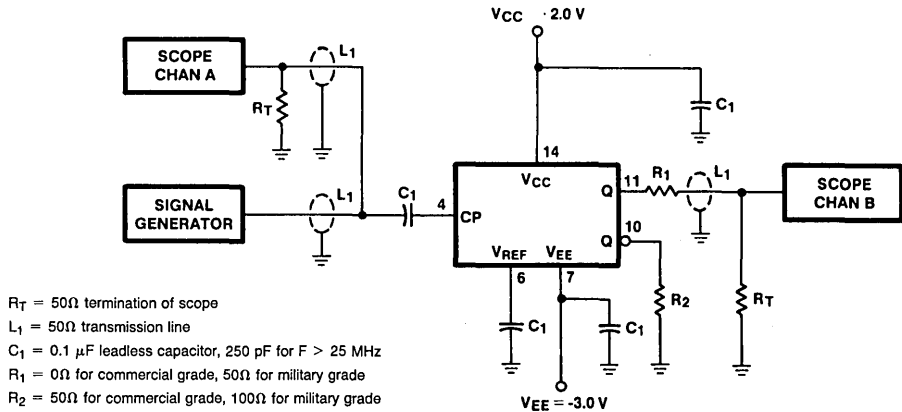
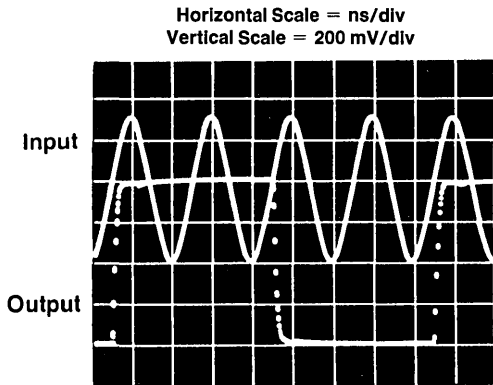


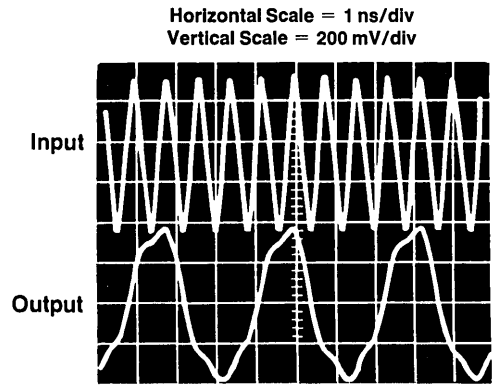
FIGURE 1. AC Test Circuit

TL/F/9889-4



25 MHz Operation

TL/F/9889-5



1.2 GHz Operation

TL/F/9889-6

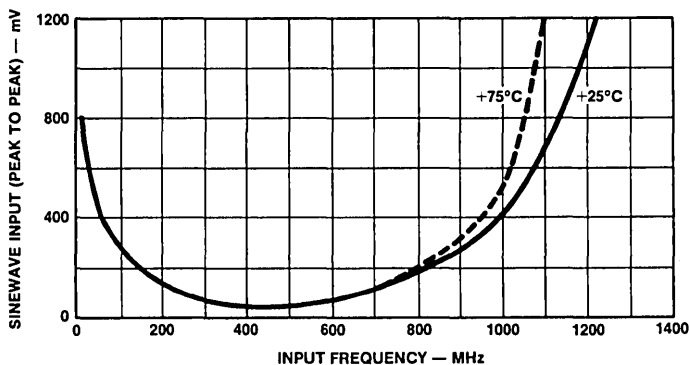


FIGURE 2. AC Input Requirements

TL/F/9889-7

Note: Trigger amplitudes refer to the circuit end of the input cable as opposed to the signal generator end.

A DC coupled input should be designed to provide specified V_{IH} and V_{IL} levels. For AC coupling, an external resistor may or may not be necessary depending on the application. If an input signal is always present, only the capacitor is required because an internal 400Ω resistor connected between CP and V_{REF} centers the AC signal about mid-threshold. For applications in which an input signal is not

always present, AC coupling requires that an external $10\text{K}\Omega$ resistor be connected between CP and V_{EE} . This offsets the input sufficiently to avoid extreme sensitivity to noise when no signal is present. Otherwise, noise triggering can lead to oscillation at about 450 MHz. For best operation, both outputs should be equally loaded.



11C06

750 MHz D-Type Flip-Flop

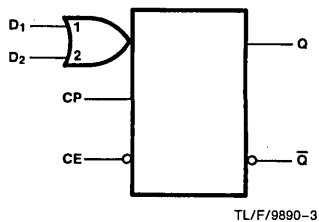
General Description

The 11C06 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 750 MHz. Designed primarily for high-speed prescaling, it can also be used in any application which does not require preset inputs. The circuit is voltage-compensated, which makes input thresholds and

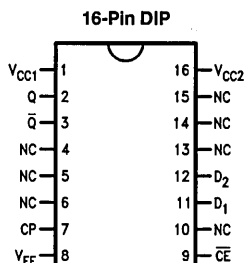
output levels insensitive to V_{EE} variations. Complementary Q and \bar{Q} outputs are provided, as are two Data inputs, Clock and Clock Enable inputs. The 11C06 is pin-compatible with the Motorola MC1690L but is a higher-frequency replacement.

Ordering Code: See Section 8

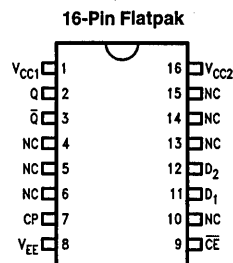
Logic Symbol



Connection Diagrams



TL/F/9890-1



TL/F/9890-2

| Pin Names | Description |
|-----------------|---------------------------|
| D_n | Data Input |
| CP | Clock Input |
| \overline{CE} | Clock Enable (Active LOW) |
| Q, \bar{Q} | Outputs |

Truth Table

| \overline{CE} | CP | D | Q_n |
|-----------------|----|---|-----------|
| L | L | X | Q_{n-1} |
| L | H | X | Q_{n-1} |
| L | | L | L |
| L | | H | H |
| H | X | X | Q_{n-1} |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 = LOW to HIGH Transition
 Q_{n-1} = Previous State

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|------------------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | +150°C |
| Supply Voltage Range | -7.0V to GND |
| Input Voltage (DC) | V _{EE} to GND |
| Output Current (DC Output HIGH) | -50 mA |

| | |
|---------------------------------------|----------------|
| Operating Range | -5.7V to -4.7V |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Recommended Operating Conditions

| | Min | Typ | Max |
|---------------------------------------|-------|-------|-------|
| Supply Voltage (V _{EE}) | -5.7V | -5.2V | -4.7V |
| Ambient Temperature (T _A) | 0°C | | +75°C |

DC Electrical Characteristics

V_{EE} = -5.2V, V_{CC} = GND

| Symbol | Parameter | Min | Typ | Max | Units | T _A | Conditions |
|------------------|---|-------------------------|-----|-------------------------|----------------|-----------------------|---|
| V _{OH} | Output Voltage HIGH | -1000 | | -840 | mV | 0°C | V _{IN} = V _{IH} (Max) or V _{IL} (Min) per Truth Table Loading 50Ω to -2V |
| | | -960 | | -810 | mV | +25°C | |
| | | -900 | | -720 | mV | +75°C | |
| V _{OL} | Output Voltage LOW | -1870 | | -1635 | mV | 0°C | |
| | | -1850 | | -1620 | mV | +25°C | |
| | | -1830 | | -1595 | mV | +75°C | |
| V _{OHc} | Output Voltage HIGH | -1020 | | | mV | 0°C | V _{IN} = V _{IH} (Min) or V _{IL} (Max) for D _n Inputs Loading 50Ω to -2V |
| | | -980 | | | mV | +25°C | |
| | | -920 | | | mV | +75°C | |
| V _{OLc} | Output Voltage LOW | | | -1615 | mV | 0°C | |
| | | | | -1600 | mV | +25°C | |
| | | | | -1575 | mV | +75°C | |
| V _{IH} | Input Voltage HIGH | -1135 -1095 -1035 | | -840 -810 -720 | mV mV mV | 0°C +25°C +75°C | Guaranteed Input Voltage HIGH for All Inputs |
| V _{IL} | Input Voltage LOW | -1870 -1850 -1830 | | -1500 -1485 -1460 | mV mV mV | 0°C +25°C +75°C | Guaranteed Input Voltage LOW for All Inputs |
| I _{IH} | Input Current HIGH Clock Input Data Input | | | 250 270 | μA μA | +25°C +25°C | V _{IN} = V _{IH} (Max) |
| | | | | | | | |
| I _{IL} | Input Current LOW | 0.5 | | | μA | +25°C | V _{IN} = V _{IH} (Min) |
| I _{EE} | Power Supply Current | -59 | -40 | | mA | +25°C | All Inputs Open |

AC Electrical Characteristics

V_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|------------------------|----------------------------|-----|-----|-----|-------|--------------------|
| t _{PHL} | Propagation Delay (CP-Q) | 0.7 | 1.0 | 1.2 | ns | See Figure 1 |
| t _{PLH} | Propagation Delay (CP-Q) | 0.7 | 1.0 | 1.2 | ns | |
| t _{TLH} | Transition Time 20% to 80% | 0.5 | 0.8 | 1.0 | ns | |
| | | 0.5 | 0.8 | 1.0 | ns | |
| t _s | Set-up Time | | 0.2 | | ns | |
| t _H | Hold Time | | 0.2 | | ns | |
| f _{TOG (MAX)} | Toggle Frequency (CP) | 650 | 750 | | MHz | See Figure 2, Note |

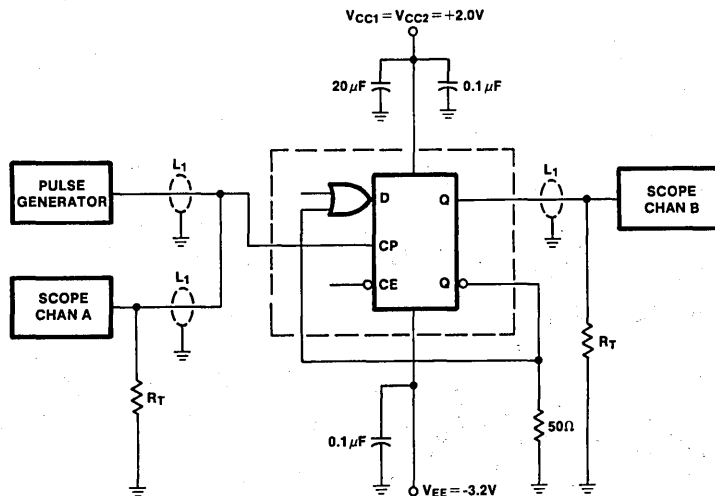
Note: The device is guaranteed for f_{TOG} (CP) ≥ 600 MHz, f_{TOG} (CE) ≥ 550 MHz over the 0°C to +75°C temperature range.

Functional Description

While the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The next transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master causing the new information to appear on the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous

master-slave changes when the clock has slow rise or fall times.

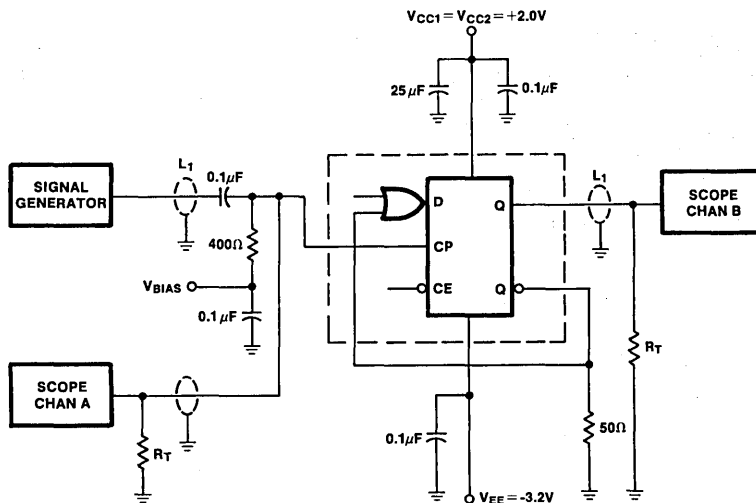
The CP and \overline{CE} inputs are logically identical, but physical constraints associated with the Dual-In-Line package make the \overline{CE} input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, \overline{CE} should go HIGH while CP is still HIGH.



$R_T = 50\Omega$ termination of scope
 $L_1 = 50\Omega$ impedance lines
 All input transition times are $2.0\text{ ns} \pm 0.2\text{ ns}$

TL/F/9890-4

FIGURE 1. Propagation Delay (CP to Q)

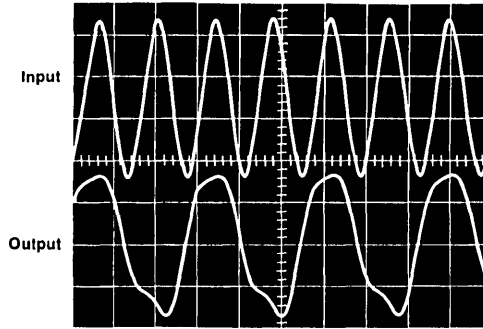


$R_T = 50\Omega$ termination of scope
 $L_1 = 50\Omega$ impedance lines
 Adjust V_{BIAS} for +0.7V baseline of
 800 mV peak-to-peak sinewave input.
 All input transition times are $2.0\text{ ns} \pm 0.2\text{ ns}$

TL/F/9890-5

FIGURE 2. Toggle Frequency Test Circuit

Typical Waveforms



700 MHz Operation

Horizontal Scale = 1.0 ns/div
Vertical Scale = 200 mV/div

TL/F/9890-6



11C70

Master-Slave D-Type Flip-Flop

General Description

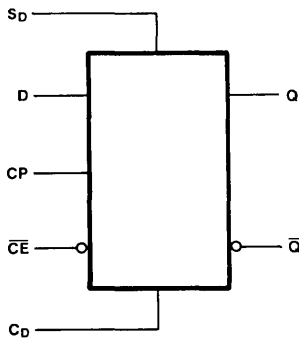
The 11C70 is a high-speed ECL D-Type Master-Slave Flip-Flop capable of toggle rates over 650 MHz. Designed primarily for communications and instrumentation, it can also be used in other digital applications and is fully compatible with 10K ECL. Asynchronous Direct Set and Direct Clear inputs are provided which override the clock.

The circuit is voltage-compensated, which makes output levels and input thresholds insensitive to V_{EE} variations.

This also allows operation with ECL supply voltage V_{EE} of $-5.2V$ or with TTL supply V_{CC} of $+5.0V$. Each input has an internal $50\text{ k}\Omega$ pull-down resistor, which allows unused inputs to be left open. Open emitter-follower outputs accommodate a variety of loading and terminating schemes. The 11C70 is pin-compatible with the Motorola MC1670 but is a higher-frequency replacement.

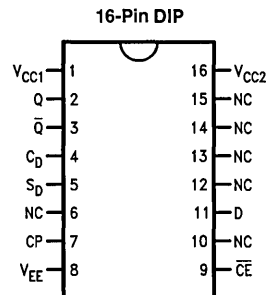
Ordering Code: See Section 8

Logic Symbol



TL/F/9891-2

Connection Diagram



TL/F/9891-1

| Pin Names | Description |
|-------------------|---------------------------|
| $\overline{C_E}$ | Clock Enable (Active LOW) |
| CP | Clock Pulse |
| D | Data Input |
| Q, \overline{Q} | Outputs |
| S_D | Direct Set |
| C_D | Direct Clear |

Truth Table

| Inputs | | | | | Q_{t+1} | Operation |
|--------|-------|---|------------------|------------|-----------|---------------|
| S_D | C_D | D | $\overline{C_E}$ | CP | | |
| H | L | X | X | X | H | Direct Set |
| L | H | X | X | X | L | Direct Clear |
| H | H | X | X | X | — | Intermediate |
| L | L | X | H | \nearrow | Q_t | Disable Clock |
| L | L | H | L | \nearrow | H | Clocked Set |
| L | L | L | L | \nearrow | L | Clocked Clear |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

\nearrow = LOW to HIGH Transition

t, t+1 = Time Before and After Clock Positive Transition

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|------------------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | +150°C |
| Supply Voltage Range | -7.0V to GND |
| Input Voltage (DC) | V _{EE} to GND |
| Output Current (DC Output HIGH) | -50 mA |
| Operating Range | -5.7V to -4.7V |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Recommended Operating Conditions

| | Min | Typ | Max |
|---------------------------------------|-------|-------|-------|
| Supply Voltage (V _{EE}) | -5.7V | -5.2V | -4.7V |
| Ambient Temperature (T _A) | 0°C | | +75°C |

DC Electrical CharacteristicsV_{EE} = -5.2V, V_{CC} = GND

| Symbol | Parameter | Min | Typ | Max | Units | T _A | Conditions |
|------------------|--|-------------------------|-----|-------------------------|----------------|-----------------------|---|
| V _{OH} | Output Voltage HIGH | -1000 | | -840 | mV | 0°C | V _{IN} = V _{IHA} or V _{ILB} per Truth Table Loading 50Ω to -2V |
| | | -960 | | -810 | mV | +25°C | |
| | | -900 | | -720 | mV | +75°C | |
| V _{OL} | Output Voltage LOW | -1870 | | -1665 | mV | 0°C | |
| | | -1850 | | -1620 | mV | +25°C | |
| | | -1850 | | -1595 | mV | +75°C | |
| V _{OHC} | Output Voltage HIGH | -1020 | | | mV | 0°C | V _{IN} = V _{IHB} or V _{ILA} for D Input Loading 50Ω to -2V |
| | | -980 | | | mV | +25°C | |
| | | -920 | | | mV | +75°C | |
| V _{OLC} | Output Voltage LOW | | | -1615 | mV | 0°C | |
| | | | | -1600 | mV | +25°C | |
| | | | | -1575 | mV | +75°C | |
| V _{IH} | Input Voltage HIGH | -1135 -1095 -1035 | | -840 -810 -720 | mV | 0°C +25°C +75°C | Guaranteed Input Voltage HIGH for All Inputs |
| V _{IL} | Input Voltage LOW | -1870 -1850 -1830 | | -1500 -1485 -1460 | mV | 0°C +25°C +75°C | Guaranteed Input Voltage LOW for All Inputs |
| I _{IH} | Input Current HIGH Clock Input Data Input S _D and C _D | | | 250 270 550 | μA μA μA | +25°C | V _{IN} = V _{IHA} |
| I _{IL} | Input Current LOW | 0.5 | | | μA | +25°C | V _{IN} = V _{IHB} |
| I _{EE} | Power Supply Current | -48 | | | mA | +25°C | All Inputs Open |

AC Electrical CharacteristicsV_{EE} = -5.2V, V_{CC} = GND, T_A = +25°C

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|-------------------------------------|---|-----|-----|-----|-------|---------------------|
| t _{PLH} , t _{PHL} | Propagation Delay (CP-Q) | | 1.1 | 1.4 | ns | See Figures 3 and 4 |
| t _{PLH} , t _{PHL} | Propagation Delay (S _D -Q̄, C _D -Q) | | 1.3 | 1.7 | ns | |
| t _{TLH} | Transition Time 20% to 80% | | 0.9 | 1.3 | ns | |
| t _{THL} | Transition Time 80% to 20% | | 0.9 | 1.3 | ns | |
| f _{TOG (MAX)} | Toggle Frequency (CP) | 550 | 650 | | MHz | See Figure 2 |

Note: This device is guaranteed for f_{TOG(max)} ≥ 500 MHz over the 0°C to +75°C temperature range.

Functional Description

Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master-slave changes when the clock has slow rise or fall times. While the clock is LOW, the slave is in a HOLD condition and information present on the D input is gated into the master. When the clock goes HIGH, it locks the master into its present state, making it insensitive to the D input, causing the new information to appear on the outputs.

The CP and \overline{CE} inputs are logically identical, but physical constraints associated with the Dual In-Line package make the \overline{CE} input slower at the upper end of the toggle range. To prevent new data from entering the master on the next CP LOW cycle, \overline{CE} should be HIGH while CP is still HIGH.

A HIGH signal on S_D or C_D will override the clocked inputs and force Q or \overline{Q} , respectively, to go HIGH. If both C_D and S_D are HIGH, the two output voltages will be somewhere between the HIGH and LOW levels and thus, cannot be usefully defined.

When the input signals for the 11C70 come from other ECL circuits, either 11CXX series or 10K types, these circuits will automatically provide appropriate signal swings, provided, of course, that these circuits are operated within their ratings and that due consideration is given to terminations appropriate to the particular application, as discussed in the F100K ECL Design Guide (Section 5 of Databook).

For applications where the clock signal comes from a circuit type other than ECL (in high frequency prescaling, for example) it is generally necessary to use external components to shift the signal levels and center them about the 11C70 input threshold region. A typical biasing scheme is shown in Figure 1. Resistors R1 and R2 are chosen such that the

quiescent voltage at the CP input is $-1.3V$ with respect to the V_{CC} terminal of the 11C70. Also indicated is the coupling from \overline{Q} back to the D input to make a simple toggle. The clock source should be designed to provide a signal swing in the range of 400 mV to 1200 mV, peak-to-peak, over the specified frequency and temperature range. To avoid saturating the input transistor, and thus limiting the frequency capability, the positive peak of the clock should not be more positive than $-0.4V$ with respect to V_{CC} .

The 11C70 outputs have no internal pull-down resistors. When driving a microstrip line terminated at the far end by a resistor returned to $-2V$ (w.r.t. V_{CC}), the quiescent I_{OH} current in the line performs the pull-down function when the output starts to go LOW. For series termination or for short unterminated lines, a 270 Ω resistor to V_{EE} will provide adequate pull-down current. The outputs switch slightly faster when both outputs are equally loaded than if only one output is loaded. Equal and opposite changes in Q and \overline{Q} load currents tend to cancel the effects of the small inductance of the V_{CC} pin.

The test arrangements illustrate the use of split power supplies, with a 2V V_{CC} and $-3.2V$ V_{EE} . This is done as a matter of instrumentation convenience, since it allows the outputs to be connected via 50 Ω cables directly to the sampling scope inputs, which have 50 Ω internal terminations. By thus avoiding the use of probes, test correlation problems between supplier and user are minimized. In actual applications, only a single power supply is needed, and ground can be assigned to V_{CC} , as in ECL systems or to V_{EE} side as in TTL systems. RF bypass capacitors are recommended in either case.

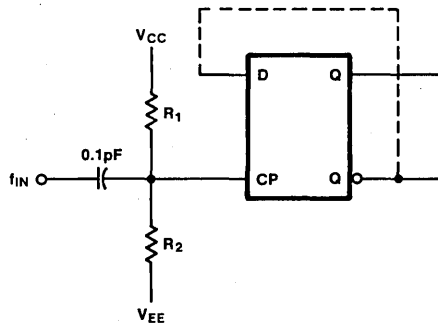
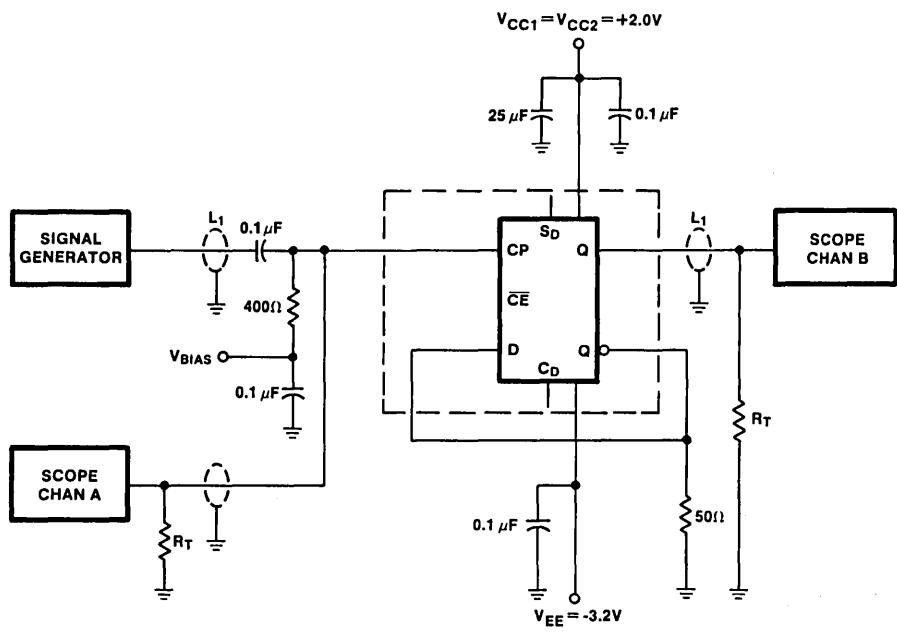


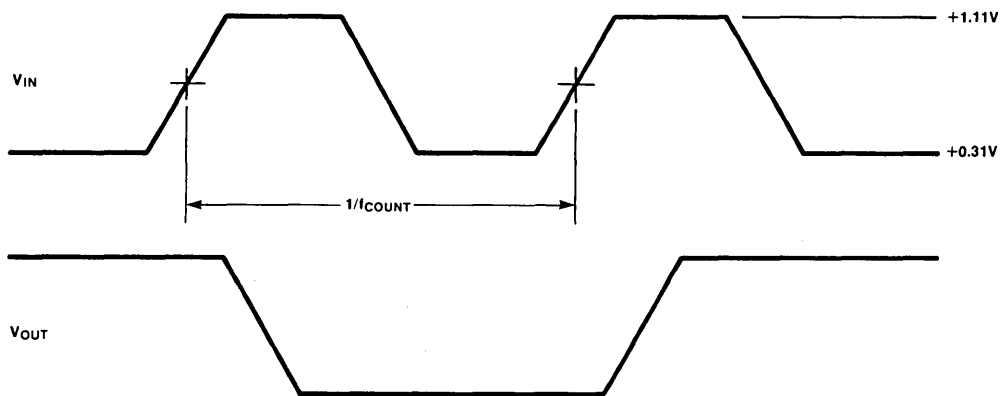
FIGURE 1. Input Biasing for AC Coupled Triggering

TL/F/9891-3



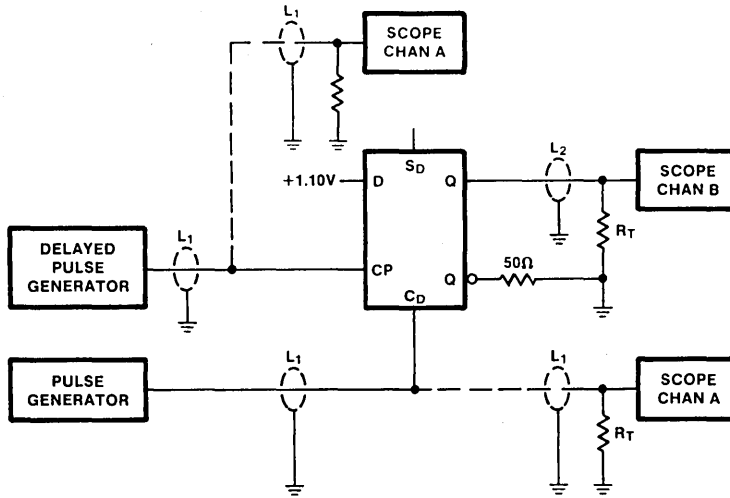
TL/F/9891-4

$R_T = 50\Omega$ termination of scope
 $L_1 = 50\Omega$ impedance lines
 Adjust V_{BIAS} for $\pm 0.7V$ baseline of
 800 mV peak-to-peak sinewave input



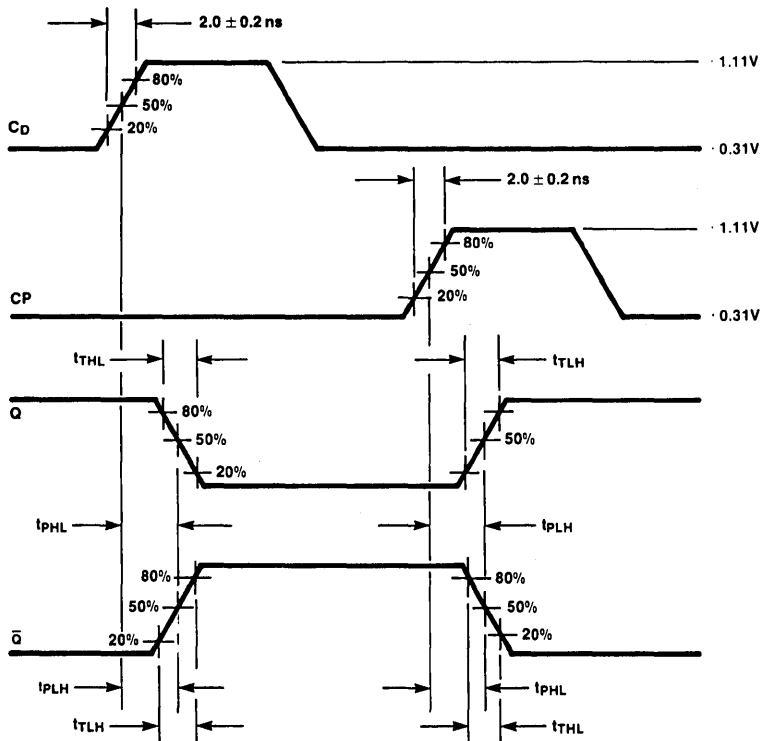
TL/F/9891-5

FIGURE 2. Toggle Frequency Test Circuit



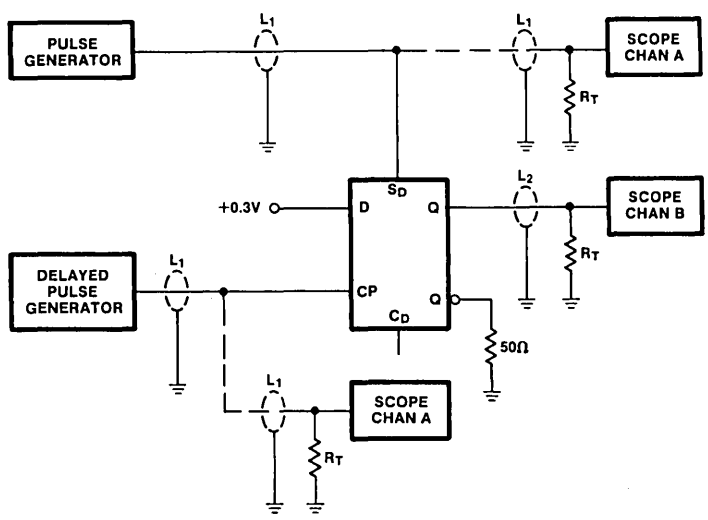
TL/F/9891-6

$V_{CC1} = V_{CC2} = +2.0V$
 $V_{EE} = -3.2V$
 $R_T = 50\Omega$ termination of scope
 $L_1, L_2 =$ equal 50Ω impedance lines
 All input transition times are $2.0\text{ ns} \pm 0.2\text{ ns}$



TL/F/9891-7

FIGURE 3. Propagation Delay and C_D Test Circuit



TL/F/9891-8

$V_{CC1} = V_{CC2} = +2.0V$
 $V_{EE} = -3.2V$
 $R_T = 50\Omega$ termination of scope
 $L_1, L_2 =$ equal 50Ω impedance lines
 All input transition times are $2.0 \text{ ns} \pm 0.2 \text{ ns}$

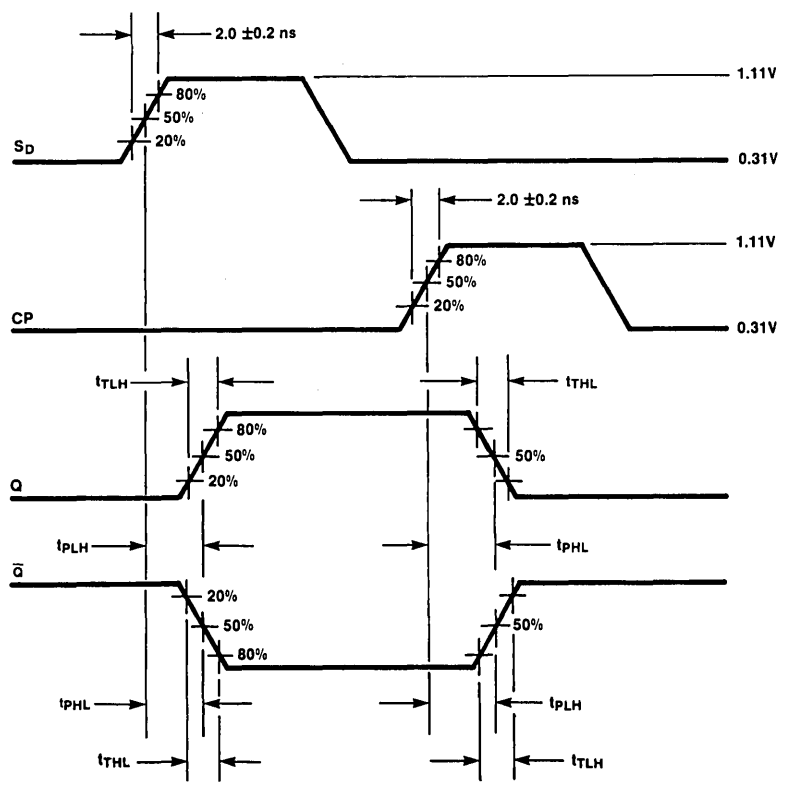


FIGURE 4. Propagation Delay and S_D Test Circuit

TL/F/9891-9



11C90/11C91 650 MHz Prescalers

General Description

The 11C90 and 11C91 are high-speed prescalers designed specifically for communication and instrumentation applications. All discussions and examples in this data sheet are applicable to the 11C91 as well as the 11C90.

The 11C90 will divide by 10 or 11 and the 11C91 by 5 or 6, both over a frequency range from DC to typically 650 MHz. The division ratio is controlled by the Mode Control. The divide-by-10 or -11 capability allows the use of pulse swallowing techniques to control high-speed counting modulus by lower-speed circuits. The 11C90 may be used with either ECL or TTL power supplies.

In addition to the ECL outputs Q and \bar{Q} , the 11C90 contains an ECL-to-TTL converter and a TTL output. The TTL output operates from the same V_{CC} and V_{EE} levels as the counter, but a separate pin is used for the TTL circuit V_{EE} . This minimizes noise coupling when the TTL output switches and

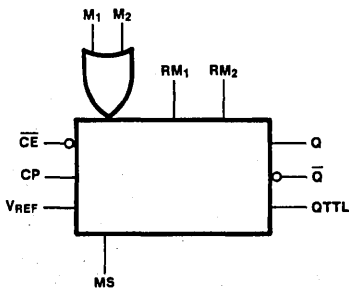
also allows power consumption to be reduced by leaving the separate V_{EE} pin open if the TTL output is not used.

To facilitate capacitive coupling of the clock signal, a 400Ω resistor (V_{REF}) is connected internally to the V_{BB} reference. Connecting this resistor to the Clock Pulse input (CP) automatically centers the input about the switching threshold. Maximum frequency operation is achieved with a 50% duty cycle.

Each of the Mode Control inputs is connected to an internal $2\text{ k}\Omega$ resistor with the other end uncommitted (RM_1 and RM_2). An M input can be driven from a TTL circuit operating from the same V_{CC} by connecting the free end of the associated $2\text{ k}\Omega$ resistor to V_{CCA} . When an M input is driven from the ECL circuit, the $2\text{ k}\Omega$ resistor can be left open or, if required, can be connected to V_{EE} to act as a pull-down resistor.

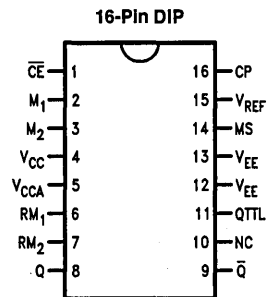
Ordering Code: See Section 8

Logic Symbol



TL/F/9892-2

Connection Diagram



TL/F/9892-1

| Pin Names | Description |
|--------------|--------------------------------------|
| \bar{CE} | Count Enable Input (Active LOW) |
| CP | Clock Pulse Input |
| M_n | Count Modulus Control Input |
| MS | Asynchronous Master Set Input |
| Q, \bar{Q} | ECL Outputs |
| QTTL | TTL Output |
| RM_n | $2\text{ k}\Omega$ Resistor to M_n |
| V_{REF} | 400Ω Resistor to V_{BB} |

Absolute Maximum Ratings

Above which the useful life may be impaired

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|------------------------|
| Storage Temperature | -65°C to +150°C |
| Maximum Junction Temperature (T _J) | +150°C |
| Supply Voltage Range | -7.0V to GND |
| Input Voltage (DC) | V _{EE} to GND |
| Output Current (DC Output HIGH) | -50 mA |
| Operating Range | -5.7V to -4.7V |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Recommended Operating Conditions

| | Min | Typ | Max |
|---------------------------------------|-------|-------|--------|
| Ambient Temperature (T _A) | | | |
| Commercial | 0°C | | +75°C |
| Military | -55°C | | +125°C |
| Supply Voltage (V _{EE}) | | | |
| Commercial | -5.7V | -5.2V | -4.7V |
| Military | -5.7V | -5.2V | -4.7V |

TTL Input/Output Operation**DC Electrical Characteristics**

Over Operating Temperature and Voltage Range unless otherwise noted, Pins 12 and 13 = GND

| Symbol | Parameter | Min | Typ (Note 3) | Max | Units | Conditions |
|-----------------|--|-----|-----------------|------|-------|--|
| V _{IH} | Input HIGH Voltage M ₁ and M ₂ Inputs | | 4.1 | | V | Guaranteed Input HIGH Threshold Voltage (Note 4), V _{CC} = V _{CCA} = 5.0V |
| V _{IL} | Input LOW Voltage M ₁ and M ₂ Inputs | | 3.3 | | V | Guaranteed Input LOW Threshold Voltage (Note 4), V _{CC} = V _{CCA} = 5.0V |
| V _{OH} | Output HIGH Voltage QTTL Output | 2.3 | 3.3 | | V | V _{CC} = V _{CCA} = Min, I _{OH} = -640 μA |
| V _{OL} | Output LOW Voltage QTTL Output | | 0.2 | 0.5 | V | V _{CC} = V _{CCA} = Min, I _{OL} = 20.0 mA |
| I _{IL} | Input LOW Current M ₁ and M ₂ Inputs | | -2.3 | -5.0 | mA | V _{CC} = V _{CCA} = Max, V _{IN} = 0.4V, Pins 6, 7 = V _{CC} |
| I _{SC} | Output Short Circuit Current | -20 | -35 | -80 | mA | V _{CC} = V _{CCA} = Max, V _{OUT} = 0.0V, Pin 14 = V _{CC} |

AC Electrical CharacteristicsV_{CC} = V_{CCA} = 5.0V Nominal, V_{EE} = GND, T_A = +25°C

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|--------------------------------------|---|------------|------------|-----|-------|---|
| t _{PLH} t _{PHL} | Propagation Delay, (50% to 50%) CP to QTTL | 6 | 10 | 14 | ns | See Figure 1 |
| t _{PLH} | Propagation Delay, (50% to 50%) MS to QTTL | | 12 | 17 | ns | |
| t _s | Mode Control Setup Time | 4 | 2 | | ns | |
| t _h | Mode Control Hold Time | 0 | -2 | | ns | |
| t _{TLH} | Output Rise Time (20% to 80%) | | 10 | | ns | |
| t _{THL} | Output Fall Time (80% to 20%) | | 2 | | ns | |
| f _{MAX} | Count Frequency | 550 600 | 650 650 | | MHz | -55°C to +125°C 0°C to +75°C Clock Input AC Coupled 350 mV Peak-to-Peak Sinewave (Note 5) |

ECL Operation—Commercial Version

DC Electrical Characteristics

 $V_{CC} = V_{CCA} = \text{GND}, V_{EE} = -5.2\text{V}$

| Symbol | Parameter | Min | Typ | Max | Units | T _A | Conditions |
|------------------|--|-------------------------|----------------------|-------------------------|-------|-------------------------|--|
| V _{OH} | Output HIGH Voltage Q and \bar{Q} | -1060 -1025 -980 | -995 -960 -910 | -905 -880 -805 | mV | 0°C +25°C +75°C | Load = 50Ω to -2V |
| V _{OL} | Output LOW Voltage Q and \bar{Q} | -1820 | -1705 | -1620 | mV | 0°C to +75°C | |
| V _{IH} | Input HIGH Voltage | -1135 -1095 -1035 | | -840 -810 -720 | mV | 0°C +25°C +75°C | Guaranteed Input HIGH Signal (Note 6) |
| V _{IL} | Input LOW Voltage | -1870 -1850 -1830 | | -1500 -1485 -1460 | mV | 0°C +25°C +75°C | Guaranteed Input LOW Signal |
| I _{IH} | Input HIGH Current CP Input (Note 1) MS Input M ₁ and M ₂ Input | | | 400 400 250 | μA | +25°C +25°C +25°C | V _{IN} = V _{IHA} |
| I _{IL} | Input LOW Current | 0.5 | | | μA | +25°C | V _{IN} = V _{ILB} |
| I _{EE} | Power Supply Current | -110 -119 | -75 | | mA | 0°C to +75°C | Pins 6, 7, 13 not connected |
| V _{EE} | Operating Supply Voltage Range | -5.7 | -5.2 | -4.7 | V | 0°C to +75°C | |
| V _{REF} | Reference Voltage | -1550 | | -1150 | mV | +25°C | V _{RM1} = V _{RM2} = -5.2V I _N = -10.0 μA |

AC Electrical Characteristics

 $T_A = 0^\circ\text{C to } +75^\circ\text{C}, V_{CC} = V_{CCA} = \text{GND}, V_{EE} = -5.2\text{V}$

| Symbol | Parameter | 0°C Typ | +25°C | | | +75°C Typ | Units | Conditions |
|--------------------------------------|---|------------|-------|------|-----|--------------|-------|--|
| | | | Min | Typ | Max | | | |
| t _{PLH} t _{PHL} | Propagat Delay, (50% to 50%) CP to Q | 1.8 | 1.3 | 2.0 | 3.0 | 2.5 | ns | Output: R _L = 50Ω to -2.0V |
| t _{PLH} | Propagat Delay, (50% to 50%) MS to Q | 3.7 | | 4.0 | 6.0 | 4.5 | ns | Input: t _{ri} = t _{fi} = 2.0 ± 0.1 ns (20% to 80%) See Figure 1 |
| t _s | Setup Time, M to CP | 2.0 | 4.0 | 2.0 | | 2.0 | ns | |
| t _h | Hold Time, M to CP | -2.0 | 0.0 | -2.0 | | -2.0 | ns | |
| t _{TLH} | Output Rise Time (20% to 80%) | 1.0 | | 1.0 | 2.0 | 1.0 | ns | |
| t _{THL} | Output Fall Time (80% to 20%) | 1.0 | | 1.0 | 2.0 | 1.0 | ns | |
| f _{MAX} | Maximum Clock Frequency | 650 | 600 | 650 | | 625 | MHz | AC Coupled Input 350 mV Peak-to-Peak. f _{MAX} is Guaranteed to be 575 MHz Min at 0°C to +75°C. |

ECL Operation—Military Version

DC Electrical Characteristics

$$V_{CC} = V_{CCA} = \text{GND}, V_{EE} = -5.2\text{V}$$

| Symbol | Parameter | Min | Typ | Max | Units | T _A | Conditions |
|------------------|--|-------------------------|-----------------------|-------------------------|-------|--------------------------|--|
| V _{OH} | Output HIGH Voltage Q and \bar{Q} | -1100 -980 -910 | -1030 -910 -820 | -900 -820 -670 | mV | -55°C +25°C +125°C | Load = 100Ω to -2V |
| V _{OL} | Output LOW Voltage Q and \bar{Q} | -1820 | -1705 | -1620 | mV | -55°C to +125°C | |
| V _{IH} | Input HIGH Voltage | -1190 -1095 -975 | | -905 -810 -690 | mV | -55°C +25°C +125°C | Guaranteed Input HIGH Signal (Note 6) |
| V _{IL} | Input LOW Voltage | -1890 -1850 -1800 | | -1525 -1485 -1435 | mV | -55°C +25°C +125°C | Guaranteed Input LOW Signal |
| I _{IH} | Input HIGH Current CP Input (Note 1) MS Input M ₁ and M ₂ Input | | | 400 400 250 | μA | +25°C +25°C +25°C | V _{IN} = V _{IHA} |
| I _{IL} | Input LOW Current | 0.5 | | | μA | +25°C | V _{IN} = V _{ILB} |
| I _{EE} | Power Supply Current | -110 | -75 | | mA | +25°C | Pins 6, 7, 13 not connected |
| | | | | -119 | | mA | |
| V _{EE} | Operating Supply Voltage Range | -5.7 | -5.2 | -4.7 | V | -55°C to +125°C | |
| V _{REF} | Reference Voltage | -1550 | | -1150 | mV | +25°C | V _{RM1} = V _{RM2} = -5.2V I _N = -10.0 μA |

AC Electrical Characteristics

$$T_A = -55^\circ\text{C to } +125^\circ\text{C}, V_{CC} = V_{CCA} = \text{GND}, V_{EE} = -5.2\text{V}$$

| Symbol | Parameter | -55°C Typ | +25°C | | | +125°C Typ | Units | Conditions |
|--------------------------------------|--|--------------|-------|------|-----|---------------|-------|---|
| | | | Min | Typ | Max | | | |
| t _{PLH} t _{PHL} | Propagation Delay, (50% to 50%) CP to Q | 1.5 | 1.3 | 2.0 | 3.0 | 3.0 | ns | Output: R _L = 50Ω to -2.0V |
| t _{PLH} | Propagation Delay, (50% to 50%) MS to Q | 3.5 | | 4.0 | 6.0 | 5.0 | ns | Input: t _{ri} = t _{fi} = 2.0 ± 0.1 ns (20% to 80%) See Figure 1 |
| t _s | Setup Time, M to CP | 2.0 | 4.0 | 2.0 | | 2.0 | ns | |
| t _h | Hold Time, M to CP | -2.0 | 0.0 | -2.0 | | -2.0 | ns | |
| t _{TLH} | Output Rise Time (20% to 80%) | 1.0 | | 1.0 | 2.0 | 1.0 | ns | |
| t _{THL} | Output Fall Time (80% to 20%) | 1.0 | | 1.0 | 2.0 | 1.0 | ns | |
| f _{MAX} | Maximum Clock Frequency | 700 | 600 | 650 | | 600 | MHz | AC Coupled Input 350 mV Peak-to-Peak. f _{MAX} is Guaranteed to be 550 MHz Min at -55°C to +125°C. |

Note 1: Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

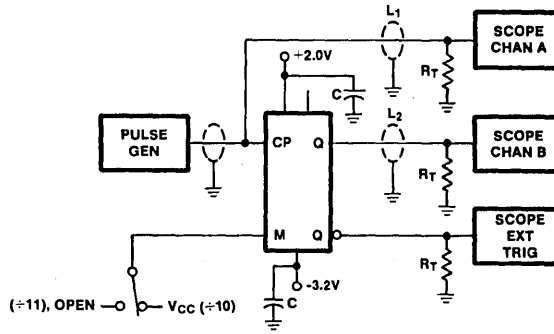
Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Typical limits are at V_{CC} = 5.0V and T_A = +25°C.

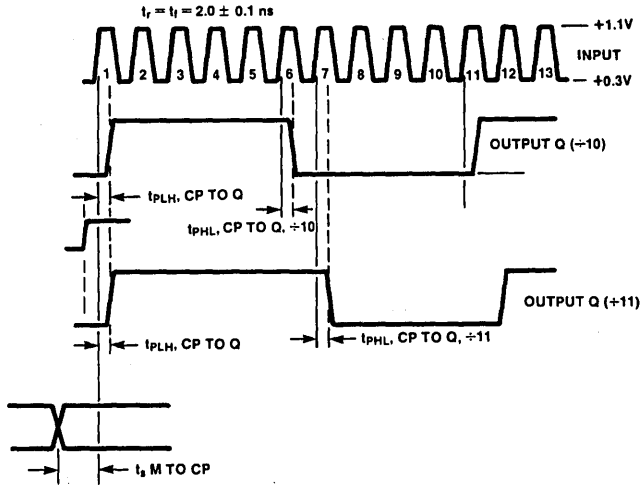
Note 4: The M₁ and M₂ threshold specifications are normally referenced to the V_{CC} potential, as shown in the ECL operation tables. Using V_{EE} (GND) as the reference, as in normal TTL practice, effectively makes the threshold vary directly with V_{CC}. Threshold is typically 1.3V below V_{CC} (e.g., +3.7V at V_{CC} = +5V). A signal swing about threshold of ±0.4V is adequate, which gives the state V_{IH} and V_{IL} values. The internal 2 kΩ resistors are intended to pull TTL outputs up to the required V_{IH} range, as discussed in the Functional Description and shown in Figure 5.

Note 5: TTL Output Signal swing is guaranteed at f_{MAX} over temperature range.

Note 6: M₁ or M₂ can be tied to V_{CC} for fixed divide-by-ten operation.



TL/F/9892-3



TL/F/9892-4

Conditions:

- V_{CC} = +2.0V
- V_{EE} = -3.2V
- R_T = 50Ω (scope input impedance)
- C_L = Jig and stray capacitance < 5.0 pF
- L₁ = L₂ = equal 50Ω impedance lines
- C = 0.1 pF

Note 7: Use high impedance to test Q_{TTL}.
Connect pin 13 to V_{EE}.

Note 8: For High frequency test use AC coupled input as in Figure 3.
Adjust input amplitude to 350 mV peak-to-peak.

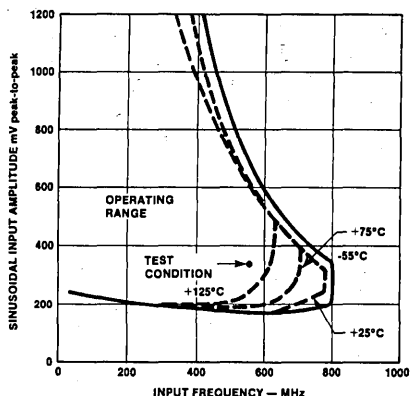
FIGURE 1. AC Test Circuit

Functional Description

The 11C90 contains four ECL Flip-Flops, an ECL to TTL converter and a Schottky TTL output buffer with an active pull-up. Three of the Flip-Flops operate as a synchronous shift counter driving the fourth Flip-Flop operating as an asynchronous toggle. The internal feedback logic is such that the TTL output and the Q ECL output are HIGH for six clock periods and LOW for five clock periods. The Mode Control (M) inputs can modify the feedback to make the output HIGH for five clock periods and LOW for five clock periods, as indicated in the Count Sequence Table.

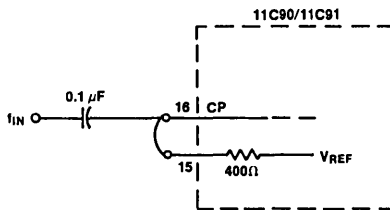
The feedback logic is such that the instant the output goes HIGH, the circuit is already committed as to whether the output period will be 10 or 11 clock periods long. This means that subsequent changes in an M input signal, including decoding spikes, will have no effect on the current output period. The only timing restriction for an M input signal is that it be in the desired state at least a setup time before the clock that follows the HLLL state shown in the table. The allowable propagation delay through external logic to an M input is maximized by designing it to use the positive transition of the 11C90 output as its active edge. This gives an allowable delay of ten clock periods, minus the CP to Q delay of the 11C90 and the M to CP setup time. If the external logic uses the negative output transition as its active edge, the allowable delay is reduced to five clock periods minus the previously mentioned delay and setup time.

Capacitively coupled triggering is simplified by the 400Ω resistor which connects pin 15 to the internal V_{BB} reference. By connecting this to the CP input, as shown in Figure 3, the clock is automatically centered about the input threshold. A clock duty cycle of 50% provides the fastest operation, since the Flip-Flops are Master-Slave types with offset clock thresholds between master and slave. This feature ensures that the circuit will operate with clock waveforms having very slow rise and fall times, and thus, there is no maximum frequency restriction. Recommended minimum and maximum clock amplitude as a function of a frequency and temperature are shown in the graph labeled Figure 2. When the CP or any other input is driven from another ECL circuit, normal ECL termination methods are recommended. One method is indicated in Figure 4. Other ECL termination methods are discussed in the F100K ECL Design Guide (Section 5 of Databook).



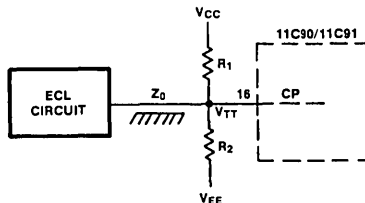
TL/F/9892-5

FIGURE 2. AC Coupled Triggering Characteristics



TL/F/9892-10

FIGURE 3. Capacitively Coupled Clcking



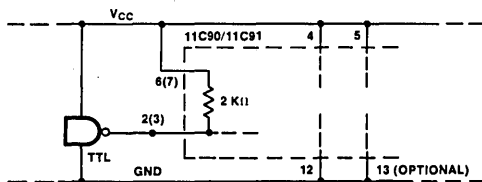
TL/F/9892-11

| | | | |
|------------------|------|-----|-----|
| Z ₀ Ω | 50 | 75 | 100 |
| R ₁ Ω | 80.6 | 121 | 162 |
| R ₂ Ω | 130 | 196 | 261 |

V_{EE} = -5.2V, V_{CC} = 0V, V_{TT} = -2.0V

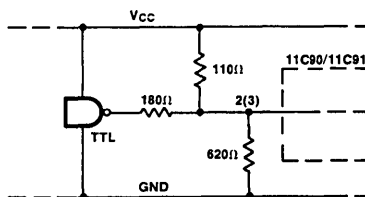
FIGURE 4. Clcking by ECL Source via Terminated Line

When an M input is to be driven from a TTL output operating from the same V_{CC} and ground (V_{EE}), the internal 2 kΩ resistor can be used to pull the TTL output up as shown in Figure 5. Some types of TTL outputs will only pull up to within two diode drops of V_{CC}, which is not high enough for 11C90 inputs. The resistor will pull the signal up through the threshold region, although this final rise may be somewhat slow, depending on wiring capacitance. A resistor network that gives faster rise and also lower impedance is shown in Figure 6.



TL/F/9892-12

FIGURE 5. Clcking by ECL Source with TTL Source



TL/F/9892-13

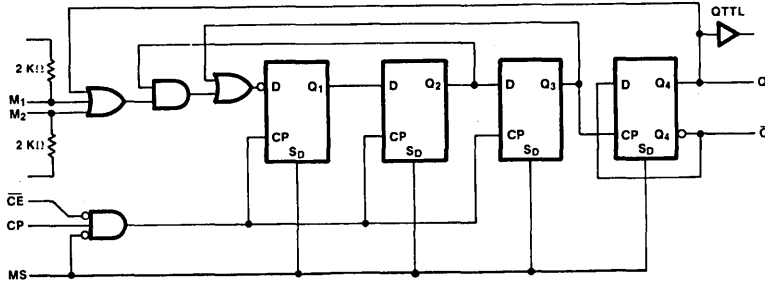
FIGURE 6. Faster Low Impedance TTL to ECL Interface

Functional Description (Continued)

The ECL outputs have no pull-down resistors and can drive series or parallel terminated transmission lines. For short interconnections that do not require impedance matching, a 270Ω to 510Ω resistor to V_{EE} can be used to establish the V_{OL} level. Both V_{CC} pins must always be used and should

be connected together as close to the package as possible. Pin 12 must always be connected to the V_{EE} side of the supply, while pin 13 is required only if the TTL output is used. Low impedance V_{CC} and V_{EE} distribution and RF bypass capacitors are recommended to prevent crosstalk.

Logic Diagram 11C90



TL/F/9892-6

Note: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many internal functions are achieved more efficiently than shown.

Count Sequence Table 11C90

| | Q ₁ | Q ₂ | Q ₃ | Q ₄ (QTTL) | |
|-------|----------------|----------------|----------------|-----------------------|-------|
| | H | H | H | H | ← ÷11 |
| → ÷10 | L | H | H | H | |
| | L | L | H | H | |
| | L | L | L | H | |
| | H | L | L | H | |
| | H | H | L | H | |
| | L | H | H | L | |
| | L | L | H | L | |
| | L | L | L | L | |
| | L | L | L | L | |
| | H | L | L | L | |
| | H | H | L | L | |

TL/F/9892-7

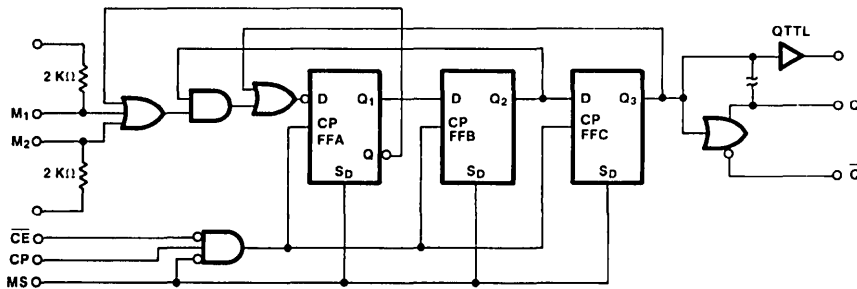
Note: A HIGH on MS forces all Qs HIGH.

Operating Mode Table 11C90

| Inputs | | | | Output Response |
|--------|----|----------------|----------------|-----------------|
| MS | CE | M ₁ | M ₂ | |
| H | X | X | X | Set HIGH |
| L | H | X | X | Hold |
| L | L | L | L | ÷ 11 |
| L | L | H | X | ÷ 10 |
| L | L | X | H | ÷ 10 |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

Logic Diagram 11C91



TL/F/9892-8

Count Sequence Table 11C91

| | Q ₁ | Q ₂ | Q ₃ (Q _{TTL}) | |
|------|----------------|----------------|------------------------------------|------|
| | H | H | H | ← ÷6 |
| → ÷5 | L | H | H | |
| | L | L | H | |
| | L | L | L | |
| | H | L | L | |
| | H | H | L | |

TL/F/9892-9

Note: A HIGH on MS forces all Qs HIGH.

Operating Mode Table 11C91

| MS | Inputs | | | Output Response |
|----|--------|----------------|----------------|-----------------|
| | CE | M ₁ | M ₂ | |
| H | X | X | X | Set HIGH |
| L | H | X | X | Hold |
| L | L | L | L | ÷6 |
| L | L | X | H | ÷5 |
| L | L | H | X | ÷5 |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care



Section 5
ECL BiCMOS SRAMs



Section 5 Contents

| | |
|---|-----|
| NM5100/NM100500 ECL I/O 256k BiCMOS SRAM 262,144 x 1 Bit | 5-3 |
| NM5104/NM100504 256k BiCMOS SRAM 64k x 4 Bit | 5-4 |
| NM100494 64k BiCMOS SRAM 16k x 4 Bit | 5-5 |
| NM10494 64k BiCMOS SRAM 16k x 4 Bit | 5-6 |
| NM100492/NM4492 2k x 9 Advanced Self-Timed SRAM (Preliminary) | 5-7 |

NM5100/NM100500 ECL I/O 256k BiCMOS SRAM

262,144 x 1 Bit

General Description

The NM5100 and NM100500 are a 262,144-bit fully static, asynchronous, random access memories organized as 262,144 words by 1 bit. The devices are based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM5100 operates with a supply voltage of $-5.2V \pm 5\%$, yet the input and output voltage levels are temperature compensated 100k ECL compatible. The NM100500 operates with a $-4.2V$ to $-4.8V$ supply voltage.

Reading the memory is accomplished by pulling the chip select (\bar{S}) pin LOW while the write enable (\bar{W}) pin remains HIGH allowing the memory contents to be displayed on the output pin (Q). The output pin will remain inactive (LOW) if either the chip select (\bar{S}) pin is HIGH or the write enable (\bar{W}) pin is LOW.

Writing to the device is accomplished by having the chip select (\bar{S}) and the write enable (\bar{W}) pins LOW. Data on the

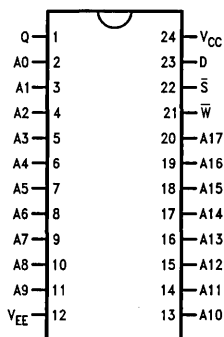
input pin will then be written into the memory address specified on the address pins (A0-A17).

Features

- 15 ns/18 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skew
- Temperature compensated F100k ECL I/O
- Power supply $-5.2V \pm 5\%$ (NM5100)
- Power supply $-4.2V$ to $-4.8V$ (NM100500)
- Low power dissipation $< 1.1W$
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 24-pin flatpack

Connection Diagrams

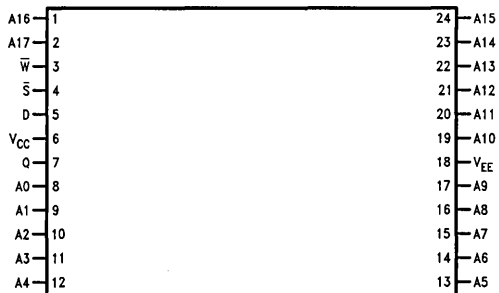
400 Mil Ceramic DIP



Top View

TL/D/9451-1

365 x 535 Ceramic Flatpack
(30 Mil Lead Pitch)



TL/D/9451-2

Top View

Pin Names

| | |
|-----------------|----------------|
| A0-A17 | Address Inputs |
| \bar{S} | Chip Select |
| \bar{W} | Write Enable |
| Q | Data Out |
| D | Data In |
| V _{CC} | Ground |
| V _{EE} | Power |



NM100504/NM5104 256k BiCMOS SRAM 64k x 4

General Description

The NM5104 and NM100504 are 262,144-bit fully static, asynchronous, random access memories organized as 65,536 words by 4 bits. The device is based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM5104 operates with a supply voltage of $-5.2V \pm 5\%$, yet the input and output voltage levels are temperature compensated 100K ECL compatible. The NM100504 operates with a $-4.2V$ to $-4.8V$ supply voltage.

Reading the memory is accomplished by pulling the chip select (\bar{S}) pin LOW while the write enable (\bar{W}) pin remains HIGH allowing the memory contents to be displayed on the output pins (Q0-Q3). The output pins will remain inactive (LOW) if either the chip select (\bar{S}) pin is HIGH or the write enable (\bar{W}) pin is LOW.

Writing to the device is accomplished by having the chip select (\bar{S}) and the write enable (\bar{W}) pins LOW. Data on the

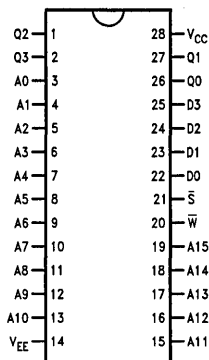
input pins will then be written into the memory address specified on the address pins (A0-A15).

Features

- Speed Grades: 12 ns/15 ns/18 ns
- Speed Grades: 15 ns/18 ns (NM100504)
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100K ECL I/O
- Power supply $-5.2V$ to $\pm 5\%$ (NM5104)
- Power supply $-4.2V$ to $-4.8V$ (NM100504)
- Low power dissipation $<1.4W$ @ 50 MHz
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 28-pin flatpak and 28-pin ceramic DIP

Connection Diagrams

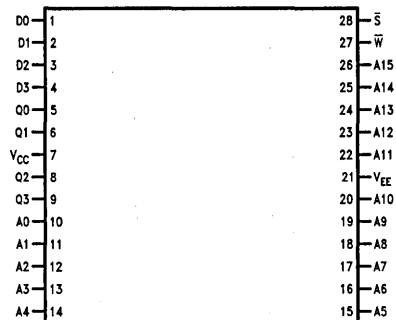
28-Pin Ceramic DIP



Top View

TL/D/10390-1

28-Pin Ceramic Flatpak
(30 Mil Lead Pitch)



Top View

TL/D/10390-2

Pin Names

| | |
|-----------------|----------------|
| A0-A15 | Address Inputs |
| \bar{S} | Chip Select |
| \bar{W} | Write Enable |
| Q0-Q3 | Data Out |
| D0-D3 | Data In |
| V _{CC} | Ground |
| V _{EE} | Power |

NM100494 64k BiCMOS SRAM 16k x 4 Bit

General Description

The NM100494 is a 65,536-bit fully static, asynchronous, random access memory organized as 16,384 words by 4 bits. The device is based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

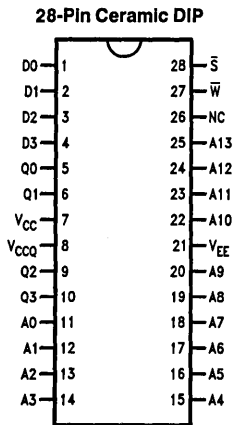
The NM100494 operates with a -4.2V to -4.8V supply voltage. Reading the memory is accomplished by pulling the chip select (\bar{S}) pin LOW while the write enable (\bar{W}) pin remains HIGH allowing the memory contents to be displayed on the output pins (Q0–Q3). The output pins will remain inactive (LOW) if either the chip select (\bar{S}) pin is HIGH or the write enable (\bar{W}) pin is LOW.

Writing to the device is accomplished by having the chip select (\bar{S}) and the write enable (\bar{W}) pins LOW. Data on the input pins will then be written into the memory address specified on the address pins (A0–A13).

Features

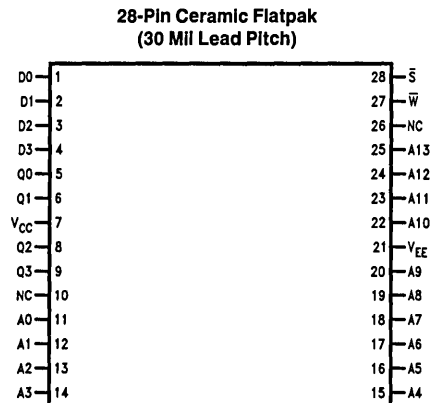
- 15 ns/18 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- Temperature compensated F100K ECL I/O
- Power supply -4.2V to -4.8V
- Low power dissipation $<1.3\text{W}$ @ 50 MHz
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 28-pin flatpak and 28-pin ceramic DIP

Connection Diagrams



Top View

TL/D/10391-2



Top View

TL/D/10391-3

Pin Names

| | |
|-----------|----------------|
| A0–A13 | Address Inputs |
| \bar{S} | Chip Select |
| \bar{W} | Write Enable |
| Q0–Q3 | Data Out |
| D0–D3 | Data In |
| V_{CC} | Ground |
| V_{EE} | Power |



NM10494 64k BiCMOS SRAM 16k x 4 Bit

General Description

The NM10494 is a 65,536-bit fully static, asynchronous, random access memory organized as 16,384 words by 4 bits. The device is based on National's advanced one micron BiCMOS III process. This process utilizes advanced lithography and processing techniques with double polysilicon and double metal bringing high density CMOS to performance driven ECL designs. National's combination of high performance technology and speed optimized circuit designs results in a very high speed memory device.

The NM10494 operates with a supply voltage of $-5.2V \pm 5\%$, and the input and output voltage levels are 10k ECL I/O compatible.

Reading the memory is accomplished by pulling the chip select (\bar{S}) pin LOW while the write enable (\bar{W}) pin remains HIGH allowing the memory contents to be displayed on the output pins (Q0-Q3). The output pins will remain inactive (LOW) if either the chip select (\bar{S}) pin is HIGH or the write enable (\bar{W}) pin is LOW.

Writing to the device is accomplished by having the chip select (\bar{S}) and the write enable (\bar{W}) pins LOW. Data on

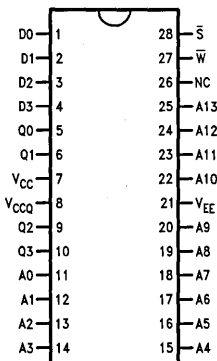
the input pins will then be written into the memory address specified on the address pins (A0-A13).

Features

- 10 ns/12 ns/15 ns speed grades over the commercial temperature range
- Balanced read and write cycle times
- Write cycle timing allows 33% of cycle time for system skews
- 10k ECL I/O
- Power supply $-5.2V \pm 5\%$
- Low power dissipation $< 1.3W$ @ 50 MHz
- Soft error rate less than 100 FIT
- Over 2000V ESD protection
- One micron BiCMOS III process technology
- Over 200 mA latch-up immunity
- Low inductance, high density 28-pin flatpak and 28-pin ceramic DIP

Connection Diagrams

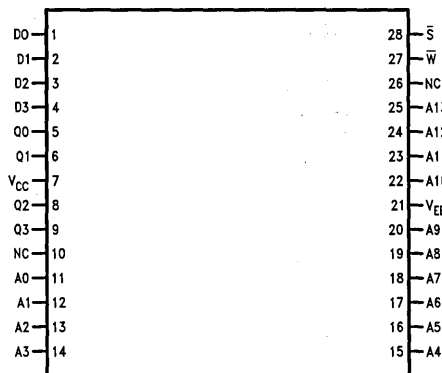
28-Pin Ceramic DIP



TL/D/10393-2

Top View

28-Pin Ceramic Flatpak (30 Mil Lead Pitch)



TL/D/10393-3

Top View

Pin Names

| | |
|-----------------|----------------|
| A0-A13 | Address Inputs |
| \bar{S} | Chip Select |
| \bar{W} | Write Enable |
| Q0-Q3 | Data Out |
| D0-D3 | Data In |
| V _{CC} | Ground |
| V _{EE} | Power |

NM100492/NM4492 2k x 9 Advanced Self-Timed SRAM

Features

- Extremely fast access time
 - 5 ns Max (NM4492)
 - 7 ns Max (NM100492)
- Power supply: $-5.2V \pm 5\%$ (NM4492)
- Power supply: $-4.2V$ to $-4.8V$ (NM100492)
- Completely self-timed read and write cycle
- On-chip input and output registers
- Modest power consumption—2W at 7 ns, <1.5W at 100 MHz
- On-chip parity checking—with odd address parity mode pin
- Clock enable input simplifies pipeline control
- Scan diagnostics supported by on-chip scan registers
- High speed ceramic flatpak
- High speed TapePak™ package under development
- I/O compatible with F100k standard

General Description

The NM100492/NM4492 is an extremely high performance 2k x 9 SRAM. It is the first of a family of similar 9-bit wide SRAMs designed specifically for very high speed ECL computer applications such as register files, writable control stores, cache RAMs, cache tag RAMs, and address translation lookaside buffers. The NM100492/NM4492 offers several features which are very desirable in such applications.

ADVANCED SELF-TIMED ARCHITECTURE

This advanced self-timed RAM simplifies the system design of extremely fast memory arrays by minimizing the impact of timing skews on the cycle time of the memory array. All input signals (address, data and control signals) are registered on-chip by a transition of the clock. By registering all inputs with minimal setup and hold times (setup + hold = 2 ns) the troublesome skews inherent with traditional static RAM timing requirements are significantly reduced. With skew problems minimized, very short cycle times become practical. Output registers (self-timed on-chip) hold output data valid for an extended portion of the cycle easing system read timing requirements.

HIDDEN WRITE CYCLE MODE

The hidden write cycle timing allows relaxed data bus timing. This will often ease system setup and hold requirements for the data output bus. Hidden write timing is essentially a technique for interleaving reads and writes. This advanced self-timed SRAM supports hidden write timing more conveniently in the system than first generation self-timed SRAM's, due to the unique control signal functions defined for write enable (\bar{W}) and chip select (\bar{S}). By keeping the output register active (with the last read data) during a write cycle, this device greatly simplifies the timing of interleaved memory architectures. This mode may be very useful in cache and register file applications, where multiple sources and/or destinations may be interleaved within each machine cycle.

PARITY CHECKING

The device also offers several convenient features which may be useful in specific applications. One such feature is the on-chip parity checking function. For systems where parity checking is desirable this device will check for odd parity on the 9-bit data input field, and will check for either even or odd parity (depending on the polarity of the parity mode pin —PM) on the 11-bit address field combined with the address parity input. Odd parity is met when the number of highs in the field is odd. Address parity checking can be conveniently disabled if desired, allowing data field only parity checking. If either the data or address demonstrates a parity error, then the parity error output flag is set. The polarity of the error output flag facilitates emitter dot ORing several error outputs for minimal delay. The parity checking feature is benign in the sense that if parity checking is not desired, the output can simply be ignored without detrimental effects to normal operation.

SERIAL SCAN DIAGNOSTICS REGISTERS

Another convenient feature provided on-chip is the scan diagnostics register. For system designs where scan diagnostics are included, this device allows observing the state of the input registers (scan out) and forcing the state of the input and output registers (scan in). For writable control store applications the control store can be loaded via the serial channel (scan in), simplifying circuit board layout by eliminating the wide parallel data input bus structure. For systems where scan diagnostics are not desired, the scan enable input can simply be left open allowing the on-chip pulldown device to disable scan functions and provide normal SRAM functionality.

PIPELINE CONTROL

Yet a third convenient feature is the clock enable input. This control simplifies starting and stopping pipeline operations in pipelined systems. It reduces, and may eliminate, the need to gate the clock signal external to the RAM. This feature is also benign since the on-chip pulldown device will ensure normal operation if the clock enable is not used.

MODEST POWER CONSUMPTION

Modest power consumption is achieved without compromising device speed through very unique and innovative circuit design techniques (patents applied for). Power consumption is predominately dependent on clock frequency (1/cycle time) allowing a reduction in power at lower operating frequency.

F100K COMPATIBLE I/O

The device is I/O compatible with standard temperature compensated F100K ECL logic, allowing trouble free interfacing in high performance ECL systems.



Section 6
ECL PALs and ASICs



Section 6 Contents

| | |
|--|------|
| PAL10/10016P8 ECL Programmable Array Logic | 6-3 |
| PAL10/10016P8-3 3 ns ECL ASPECT Programmable Array Logic (DIP) | 6-4 |
| PAL10/10016PE8-3 3 ns ECL ASPECT Programmable Array Logic (PLCC) | 6-5 |
| PAL10/10016P4A 4 ns ECL Programmable Array Logic | 6-6 |
| PAL10/10016P4-2 2 ns ECL ASPECT Programmable Array Logic (DIP) | 6-7 |
| PAL10/10016C4-2 2 ns ECL ASPECT Programmable Array Logic (PLCC) | 6-8 |
| PAL10/10016RD8 ECL Registered Programmable Array Logic | 6-9 |
| PAL10/10016RM4A ECL Registered Programmable Array Logic | 6-10 |
| FGA Series ASPECT ECL Gate Arrays | 6-11 |

PAL10/10016P8

ECL Programmable Array Logic

General Description

The PAL1016P8/10016P8 is the first member of an ECL programmable logic device family possessing common electrical characteristics, utilizing an easily accommodated programming procedure, and produced with National Semiconductor's advanced oxide-isolated process. This family includes combinatorial, and registered output devices.

These devices are fabricated using National's proven Ti-W (Titanium-Tungsten) fuse technology to allow fast, efficient, and reliable programming.

This family allows the designer to quickly implement the defined logic function by removing the fuses required to properly configure the internal gates and/or registers. Product terms with all fuses removed assume a logical high state. All devices in this series are provided with an output polarity fuse that, if removed, will permit any output to independently provide a logic low when the equation is satisfied. When these fuses are intact the outputs provide a logic true (most positive voltage level) in response to the input conditions defined by the applicable equation. All input and I/O pins have on-chip 50 k Ω pull-down resistors.

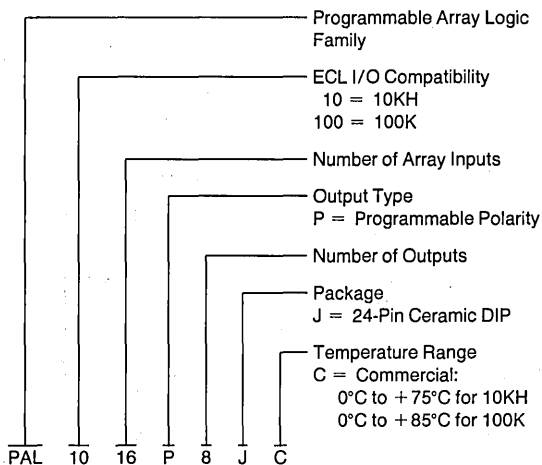
Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams to create fuse maps representing the programmed device.

All devices in this family can be programmed using conventional programmers. After the device has been programmed and verified, an additional fuse may be removed to inhibit further verification or programming. This "security" feature can provide a proprietary circuit which cannot easily be duplicated.

Features

- $t_{PD} = 6$ ns max
- Eight combinatorial outputs with programmable polarity
- Programmable replacement for conventional ECL logic
- Both 10KH and 100K I/O compatible versions
- Simplifies prototyping and board layout
- 24-pin thin DIP packages.
- Programmed on conventional TTL PLD programmers
- Security fuse to prevent direct copying
- Reliable titanium-tungsten fuses

Ordering Information





PRELIMINARY

PAL10/10016P8-3 (DIP Only) 3 ns ECL ASPECT™ Programmable Array Logic

General Description

The PAL10/10016P8-3 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor's ASPECT (Advanced Single Poly Emitter Coupled Technology) process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of applications—specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016P8-3 logic array has a total of 16 complementary input pairs, 64 product terms and 8 programmable polarity output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisfied when all array inputs which are connected to it (via intact fuses) are in the correct state as defined by the equation for that

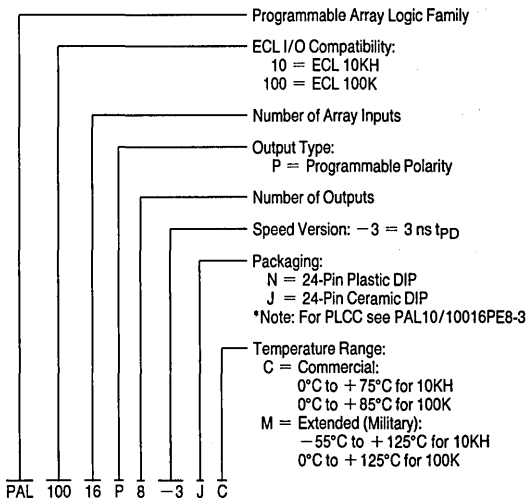
product term. Each output function is provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by industry standard TTL PLD programmers. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

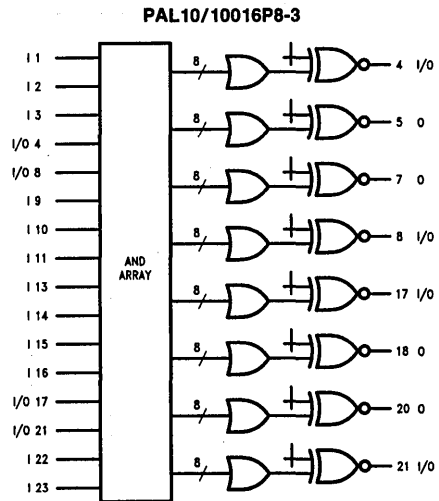
Features

- High speed: $t_{PD} = 3$ ns max
- Programmable replacement for ECL logic
- Both 100K and 10 KH I/O compatible versions
- Eight output functions with programmable polarity
- Improved programmability tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully supported by PLAN™ software
- Commercial and Military ranges

Ordering Information



Block Diagram



TL/L/10714-1

PAL10/10016PE8-3 (PLCC Only) 3 ns ECL ASPECT™ Programmable Array Logic

General Description

The PAL10/10016PE8-3 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor's ASPECT (Advanced Single Poly Emitter Coupled Technology) process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of applications—specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016PE8-3 logic array has a total of 16 complementary input pairs, 64 product terms and 8 programmable polarity output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisfied when all array inputs which are connected to it (via intact fuses) are in the correct state as defined by the equation for that

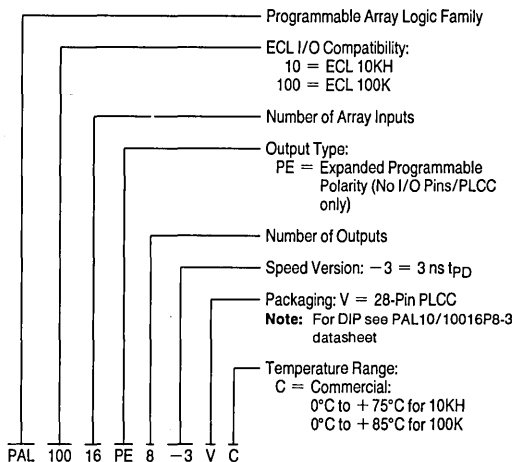
product term. Each output function is provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by industry standard conventional TTL PLD programmers. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

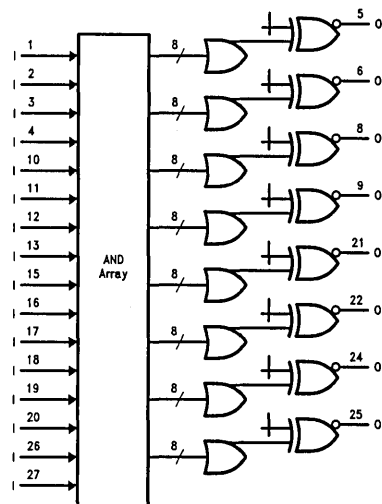
Features

- High speed: t_{PD} 3 ns max
- Full 28-pin function (all pins used)
- Programmable replacement for ECL logics
- Both 100K and 10 KH I/O compatible versions
- Eight output functions with programmable polarity
- Security fuse to prevent direct copying
- Fully supported by PLAN and other industrial software
- High density-high performance 28-pin PLCC package

Ordering Information



Block Diagram



TL/L/10712-1



PAL10/10016P4A

4 ns ECL Programmable Array Logic

General Description

The PAL1016P4A and PAL10016P4A are members of the National Semiconductor ECL PAL[®] family. The PAL10/10016P4A is a functional subset of the PAL10/10016P8 (6 ns tpd) and is compatible in pinout, JEDEC map format, and programming algorithm. The ECL PAL family utilizes National Semiconductor's advanced oxide-isolated process and proven Titanium-Tungsten (Ti-W) fuse technology to provide user-programmable logic to replace conventional ECL SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PAL devices is greater than 4:1.

This family allows the systems engineer to customize his chip by opening fuse links to configure AND and OR gates to perform his desired logic function. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can easily be modified during prototype checkout or production.

The PAL transfer function is the familiar sum-of-products implemented with a single array of fusible links. The PAL device incorporates a programmable AND array driving a fixed OR array. The AND term logic matrix incorporates 16 complementary inputs and 32 product terms. The 32 product terms are grouped into four OR functions with eight product terms each. All devices in this series are provided with output polarity fuses. These fuses permit the designer to configure each output independently to provide either a logic true (by leaving the fuse intact) or a logic false (by programming the fuse) when the equation defining that output is satisfied.

Product terms with all fuses programmed assume a logical high state, while product terms connected to both the true

and complement of any input assume a logical low state. All product terms in an unprogrammed part are logically low.

Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams for logic editing.

These ECL PAL devices may be programmed on many PLD programmers. Programming is accomplished using TTL voltage levels. Once programmed and verified, an additional fuse may be programmed to disable further verification. This feature gives the user a proprietary circuit which is difficult to copy.

Features

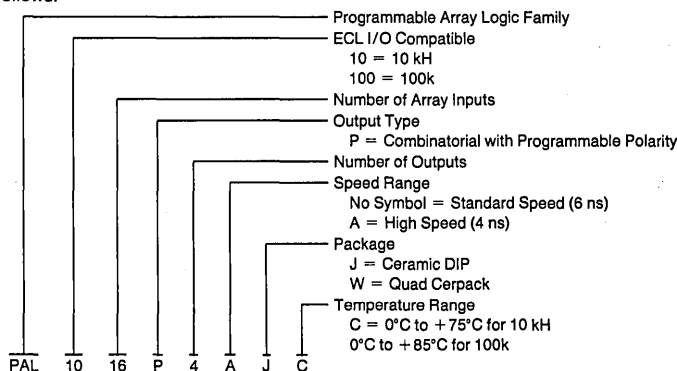
- High speed:
Combinatorial outputs
tpd = 4 ns max
- Both 10 KH and 100K I/O compatible versions
- Four output functions; sixteen dedicated inputs
- Individually programmable polarity for all logic outputs
- Reliable titanium-tungsten fuses
- Security fuse to prevent direct copying
- Programmed on many PLD programmers
- Fully Supported by PLAN[™] Software
- Packaging:
24-pin thin DIP (0.300")
24-pin QUAD CERPAK

Applications

- Programmable replacement for ECL logic
- Address or instruction decoding

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



PAL10/10016P4-2 (DIP Only) 2 ns ECL ASPECT™ Programmable Array Logic

General Description

The PAL10/10016P4-2 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor's ASPECT (Advanced Single Poly Emitter Coupled Technology) process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016P4-2 logic array has a total of 16 complementary input pairs, 32 product terms and 4 programmable polarity output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisfied when all array inputs which are connected to it (via intact fuses) are in the correct state as defined by the equation for that

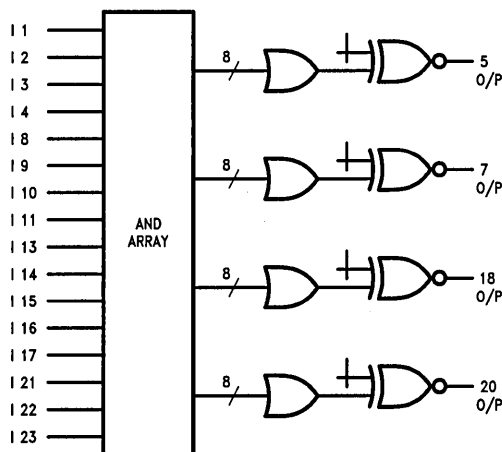
product term. Each output function is provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by industry standard TTL PLD programmers. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

Features

- Highest speed: $t_{PD} = 2.5$ ns max
- Programmable replacement for ECL logic
- Both 100K and 10 KH I/O compatible versions
- Four output functions with programmable polarity
- Improved programmability tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLAN™ Software
- Commercial and Military ranges

Block Diagram PAL10/10016P4-2



$V_{EE} = 12, V_{CC} = 24, V_{CC0} (5, 7) = 6$
 $V_{CC0} (18, 20) = 19$
 Pinout applies to 24-pin DIP

TL/L/10711-1



PRELIMINARY

PAL10/10016C4-2 (PLCC Only) 2 ns ECL ASPECT™ Programmable Array Logic

General Description

The PAL10/10016C4-2 is a member of the National Semiconductor 28-pin high speed ECL PAL® family. This device utilizes National Semiconductor's ASPECT (Advanced Single Poly ECL Technology) Process with a newly developed tungsten fuse technology to provide the highest-speed user-programmable replacements for conventional ECL SSI-MSI logic with significant chip-count reduction. The JEDEC fuse-map format and programming algorithm of this device is compatible with those of all prior ECL PAL products from National.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016C4-2 logic array has a total of 16 complementary input pairs, 32 product terms and 4 complementary output functions. Each output function is the OR-sum of 8 product terms. Each product term is satisfied when all array inputs which are connected to it (via intact fuses) are in the correct state. Complementary outputs eliminate the need

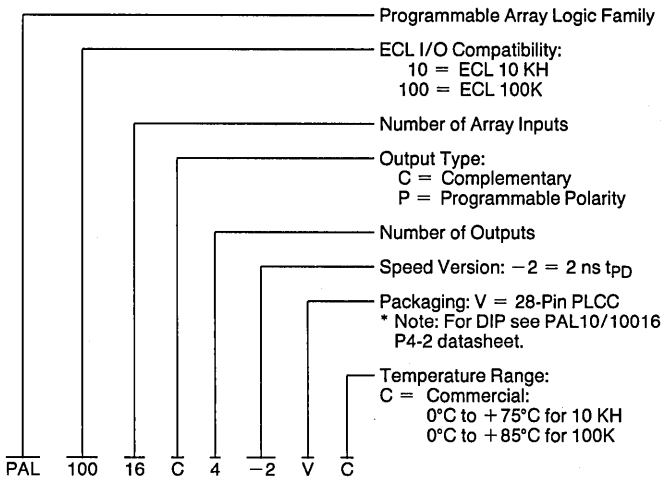
for external inverters and allow for more convenient output OR-tying. They are also suitable for differential sensing for increased noise immunity. All input pins have on-chip 50 kΩ pull-down resistors.

Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by several conventional TTL PLD programming units. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

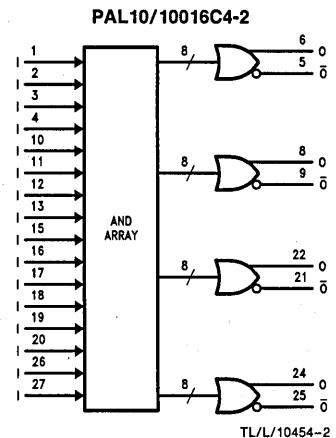
Features

- Highest speed: $t_{PD} = 2 \text{ ns max}$
- Full 28-pin function
- Programmable replacement for ECL logic
- Both 100K and 10 KH I/O compatible versions
- Four output functions with complementary outputs
- Improved programmability tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLAN™ Software
- High density-High performance 28-pin PLCC package

Ordering Information



Block Diagram



$V_{EE} = 14, V_{CC} = 28, V_{CC0} (5, 6, 8, 9) = 7$
 $V_{CC0} (21, 22, 24, 25) = 23$
 Pinout applies to 28-pin PLCC

PAL10/10016RD8 ECL Registered Programmable Array Logic

General Description

The registered ECL PAL10/10016RD8 is offered in 10KH or 100K compatible versions. A maximum propagation delay of 6 ns (input to output) characterizes the performance of this ECL PAL® series. The ECL PAL family utilizes National Semiconductor's advanced oxide-isolated process and proven Titanium Tungsten (Ti-W) fuse technology to provide user-programmable logic to replace conventional ECL SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PAL devices is greater than 4:1.

This family allows the system engineer to customize the chip by opening fuse links to configure AND and OR gates to perform the desired logic function. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can easily be modified during prototype checkout or production.

The PAL transfer function is the familiar sum-of-products implemented with a single array of fusible links. The PAL device incorporates a programmable AND array driving a fixed OR array. The AND term logic matrix incorporates 16 complementary inputs and 64 product terms. The 64 product terms are grouped into eight OR functions with eight product terms each. All devices in this family are provided with output polarity fuses. These fuses permit the designer to configure each output independently to produce either a logic high (by leaving the fuse intact) or a logic low (by programming the fuse) when the equation defining that output is satisfied. In addition, the ECL PAL family offers these options:

- Output registers
- Dual (split) clocks

Product terms with all fuses programmed assume a logical high state, while product terms connected to both the true and complement of any input assume a logical low state. All product terms in an unprogrammed part are logically low. All input and I/O pins have on-chip 50 k Ω pull-down resistors. Registers consist of D-type flip-flops which are loaded in response to the low-to-high transition of the clock input(s).

Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams for logic editing.

These ECL PAL devices may be programmed on several TTL PLD programmers. Programming is accomplished with TTL voltage levels. Once the PAL is programmed and verified, an additional security fuse may be programmed to defeat verification. This feature gives the user a proprietary circuit which is difficult to copy.

Features

- High speed:
 - Combinatorial outputs
tpd = 6 ns max
 - Registered outputs
 $t_{su} = 5$ ns min
 $t_{clk} = 3.5$ ns max
 $f_{max} = 117$ MHz max
- Both 10 KH and 100K I/O compatible versions
- Eight output functions with feedback; eight dedicated inputs
- Eight registered outputs
- Individually programmable polarity on all logic outputs
- Output enable gate on all registered outputs
- Reliable Titanium Tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLANT™ Software
- Packaging:
 - 24-pin thin DIP (0.300")
 - 24-pin QUAD CERPAK

Applications

- Programmable replacement for ECL logic
- Programmable state machine
- Address or instruction decoding



PAL 10/10016RM4A

ECL Registered Programmable Array Logic

General Description

The PAL10/10016RM4A is a member of the National Semiconductor ECL PAL® family. The ECL PAL Series-A is characterized by 4 ns maximum propagation delays (combinatorial input-to-output). The pinout, JEDEC fuse-map format and programming algorithm of these devices are compatible with those of all prior ECL PAL products from National. Series-A ECL PAL devices are manufactured using National Semiconductor's advanced oxide-isolated process with proven titanium-tungsten fuse technology to provide high-speed user-programmable replacements for conventional ECL SSI/MSI logic with significant chip-count reduction.

Programmable logic devices provide convenient solutions for a wide variety of application-specific functions, including random logic, custom decoders, state machines, etc. By programming fuse links to configure AND/OR gate connections, the system designer can implement custom logic as convenient sum-of-products Boolean functions. System prototyping and design iterations can be performed quickly using these off-the-shelf products.

The PAL10/10016RM logic array has a total of 16 complementary input pairs, 32 product terms and four output functions; each output function is the OR-sum of 8 product terms. The 16RM4A provides an edge-triggered D-type register on each of its four outputs. Registers allow the PAL device to implement sequential logic circuits. Polarity fuses allow each output to be active-high or active-low.

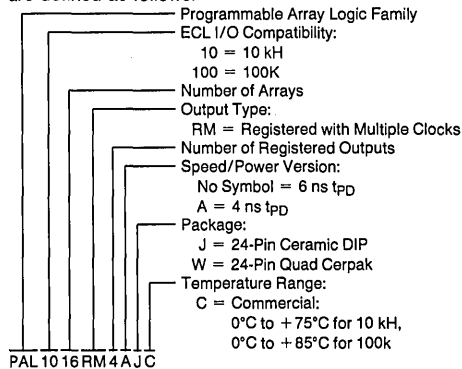
Programming equipment and software make PAL design development quick and easy. Programming is accomplished using TTL voltage levels and is therefore supported by several conventional TTL PLD programming units. After programming and verifying the logic array, an additional security fuse may be programmed to prevent direct copying of proprietary logic designs.

Features

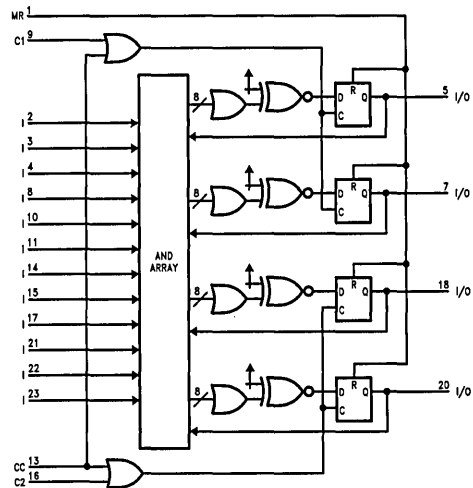
- High speed:
 - $t_{SU} = 3 \text{ ns min}$
 - $t_{CLK} = 2 \text{ ns max}$
 - $f_{MAX} = 200 \text{ MHz max (registered)}$
 - $t_{PD} = 4 \text{ ns max (combinatorial)}$
- Programmable replacement for ECL SSI/MSI logic
- Both 10 KH and 100K I/O compatible versions
- Four registered output functions with I/O pin feedback; twelve dedicated inputs
- Individually programmable polarity on all logic outputs
- Reliable Titanium Tungsten fuses
- Security fuse to prevent direct copying
- Programmed on conventional TTL PLD programmers
- Fully Supported by PLAN™ Software
- Packaging:
 - 24-pin thin DIP (0.300")
 - 24-pin Quad Cerpak

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Block Diagram



TL/L/9772-2

$V_{EE} = 12, V_{CC} = 24, V_{CCO} (5,7) = 6, V_{CCO} (18,20) = 19$
 Pinout applies to 24-pin DIP.

FGA Series ASPECT™ ECL Gate Arrays

General Description

The FGA Series is a new generation of ECL gate arrays based on National's ASPECT process. These advanced ECL gate arrays, ranging from 200 to over 30,000 equivalent gates, offer typical internal propagation delays of 150 ps and consume thirty percent less power than conventional ECL arrays. (Refer to Table I.)

With system clock frequencies up to 1.2 GHz, the speed domain of Gallium Arsenide, FGA Series gate arrays are especially well-suited for such high-performance applications as mainframe and supermini computers, fiber-optic communications, and many military and aerospace systems.

With only internal cells and I/O cells, FGA Series arrays are easy to use. Designers can implement logic using two-level or three-level series gating circuit structures within an array, with no complex signal mixing rules required. An extensive macro library, common to all FGA Series arrays, contains more than eighty SSI/MSI logic functions and 36 supporting I/O macros. In addition, internal macros may be grouped to form re-usable "soft macros" with even greater functional complexity.

All FGA Series gate arrays feature CAD-programmable speed/power options that allow the designer to maximize performance by individually assigning the switching speed and output drive currents for each internal macro. The speed/power feature provides maximum ECL speed where needed, yet allows overall chip power to remain at air-coolable levels. On-chip termination to $-2V$ for the internal output emitter followers further reduces power consumption.

All FGA Series products interface with ECL 100K, ECL 10K and ECL 10KH components, and, except for the FGA200, FGA14000, FGA14040R, and FGA30000, are fully FAST®/TTL compatible. The TTL interface eliminates requirements for separate off-chip signal converters in mixed logic level systems, thereby resulting in reduced board space and cost, as well as avoiding the performance and reliability penalties associated with off-chip signal converters.

In addition to providing superior speed/power performance with high density, the ASPECT process is scalable to sub-micron dimensions. FGA Series arrays are designed to accommodate multiple ASPECT process generations to allow designs implemented today to migrate to tomorrow's arrays based on future ASPECT processes.

Features

- New generation ECL gate arrays with complexity to 30,000 equivalent logic gates
- Manufactured with 1.5-micron ASPECT process
- CAD-programmable speed/power options
- 150 ps typical internal delay
- Flexible array architecture with only two cell types: Internal cells and I/O cells
 - F100K, 10K or 10KH ECL-compatible I/Os
 - Mixable ECL/TTL I/Os
- Allows large number of simultaneously switching outputs

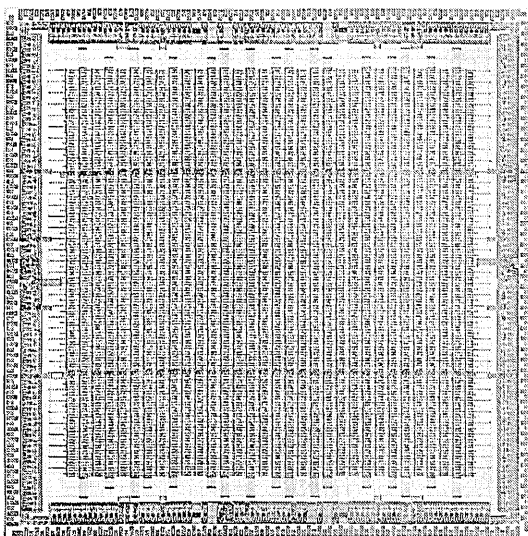


FIGURE 1. FGA Series Gate Array

Note 1: FGA150, 600, 1300, 4000 and 15000 offer mixable ECL/TTL I/Os.

TL/U/10560-1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|---|
| Storage Temperature (T _{STG}) | -65°C to +150°C |
| Maximum Junction Temp. (T _J) | +150°C |
| Case Temp. under Bias (T _C) | -55°C to +125°C |
| V _{EE} Pin Potential to V _{CC} Pins (V _{MAX}) | -7.0V to +0.5V |
| Input Voltage (DC) (V _I) | V _{EE} to (V _{CC} + 0.5V) |
| Output Current (DC Output HIGH) (I _O) | -50 mA |
| Operating Range ECL (V _{EE}) | -5.7V to -4.2V |
| Operating Range TTL (V _{TTL}) | 4.5V to 5.5V |

Note: Stresses greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Specifications

All FGA Series gate arrays operate from a standard ECL power supply and an additional -2V supply (V_{TT}) which terminates internal cell emitter followers to reduce power consumption. With F100K inputs and outputs, the FGA series is designed to operate from a standard 100K power supply, although a standard 10K power supply may be used instead. When used for mixed ECL/TTL operations, an additional power supply is required. The following table provides the power requirements for each allowable interface configuration.

Power Supply Requirements

| I/O | V _{CC} (V) | V _{TT} (V)(Note 2) | V _{EE} (V) | V _{TTL} (V) | Arrays |
|------------|---------------------|-----------------------------|---------------------|----------------------|--|
| F100K | GND | -1.9 to -2.1 | -4.2 to -5.7 | — | All |
| F10K | GND | -1.9 to -2.1 | -4.7 to -5.7 | — | |
| F100K/TTL | GND | -1.9 to -2.1 | -4.2 to -5.7 | 4.5 to 5.5 | Except FGA200, FGA14000, FGA14040R and FGA 30000 |
| F10K/TTL | GND | -1.9 to -2.1 | -4.7 to -5.7 | 4.5 to 5.5 | |
| Pseudo TTL | V _{TTL} | (V _{TTL} -2) ±0.1 | GND | 4.75 to 5.25 | |

F100K ECL DC Characteristics

V_{EE} = -4.5V, V_{TT} = -2V, V_{CC} = V_{CCA} = GND, T_J = -10°C to +125°C (Note 3)

| Symbol | Parameter | Conditions (Note 4) | | Min | Typ | Max | Units |
|--------------------------|---------------------|---|--------------------------|-------|-------|-------|-------|
| V _{OH} | Output HIGH Voltage | V _{IN} = V _{IH} (max) | Loaded with 50Ω to -2.0V | -1035 | -955 | -870 | mV |
| V _{OL} | Output LOW Voltage | or V _{IL} (min) | | -1830 | -1705 | -1605 | mV |
| V _{IH} (Note 5) | Input HIGH Voltage | Guaranteed HIGH Signal for All Inputs | | -1125 | | -880 | mV |
| V _{IL} (Note 5) | Input LOW Voltage | Guaranteed LOW Signal for All Inputs | | -1810 | | -1520 | mV |

Note 1: Unless otherwise specified contractually.

Note 2: For internal cell output emitter follower termination to save power.

Note 3: Equilibrium temperature

Note 4: Conditions for testing are chosen to guarantee operation under worst case conditions.

Note 5: Forcing one input at a time. Apply V_{IH} (max) or V_{IL} (min) to all other inputs.

F10K ECL DC Characteristics $V_{EE} = -5.2V, V_{TT} = -2V, V_{CC} = V_{CCA} = GND$

| Parameter | Conditions | Junction Temperature | | | | Units |
|------------------------|--|----------------------|-------|-------|-------|-------|
| | | 0°C | 25°C | 65°C | 125°C | |
| V_{OH} Max | $V_{IH} = V_{IH}$ Max $V_{IL} = V_{IL}$ Min | -897 | -862 | -810 | -732 | mV |
| V_{OH} Min | | -1112 | -1077 | -1025 | -947 | mV |
| V_{OL} Max | | -1656 | -1644 | -1620 | -1584 | mV |
| V_{OL} Min | | -1920 | -1920 | -1920 | -1920 | mV |
| V_{IH} Max (Note 1) | | -888 | -858 | -810 | -738 | mV |
| V_{IL} Min (Note 1) | | -1920 | -1920 | -1920 | -1920 | mV |
| V_{IHA} Min (Note 1) | | -1209 | -1172 | -1125 | -1045 | mV |
| V_{ILA} Max (Note 1) | | -1604 | -1567 | -1520 | -1440 | mV |

TTL DC Characteristics over Operating Temperature Range
 $V_{CC} = 5V \pm 5\%, T_J = -10^\circ C \text{ to } +125^\circ C$

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|-----------|---|---|-----------------------------------|-----|------|------|---------|
| V_{OH} | Output HIGH Voltage | $I_{OH} = -400 \mu A$ | $V_{CC} = 4.75V$ | 2.7 | 3.0 | — | V |
| V_{OL} | Output LOW Voltage | $I_{OH} = 8.0 \text{ mA}/20 \text{ mA}$ | $V_{CC} = 4.75V$ | — | 0.25 | 0.5 | V |
| V_{IH} | Input HIGH Voltage | | | 2.0 | — | — | V |
| V_{IL} | Input LOW Voltage | | | — | — | 0.80 | V |
| I_{IH} | Input HIGH Current (Note 2) | $V_{CC} = 5.25V, V_{IN} = 2.4V$ | | — | — | 40 | μA |
| I_{IL} | Input LOW Current (Note 2) | $V_{CC} = 5.25V, V_{IN} = 0.4V$ | | — | — | -400 | μA |
| I_{OZH} | Output OFF Current HIGH | $V_{CC} = 5.25V, V_{OUT} = 2.4V$ | | — | — | 40 | μA |
| I_{OZL} | Output OFF Current LOW | $V_{CC} = 5.25V, V_{OUT} = 0.4V$ | | — | — | -40 | μA |
| I_{OS} | Output Off Short Circuit Current (Note 3) | 8/20 mA Driver | $V_{CC} = 5.25V$ $V_{OUT} = 0$ | -15 | — | -130 | mA |

Note 1: Forcing one input at a time. Apply V_{IH} (max) or V_{IL} (min) to all other inputs.

Note 2: Current per input.

Note 3: Not more than one output should be shorted at a time. Output should not be shorted for more than one second.

FGA Series ECL Gate Array Family

TABLE I. The FGA Gate Array Series

| Description | FGA0150 | FGA0200 | FGA0600 | FGA1300 | FGA4000 | FGA14000 | FGA14040R | FGA15000 | FGA30000 |
|--------------------------|-----------------------------------|-----------------------------------|-----------------|-----------------------------|------------------------------|----------|-----------------|----------|----------|
| Equivalent Gates | 269 | 269 | 792 | 1642 | 4704 | 16709 | 7853 + 4.6K RAM | 16644 | 28486 |
| Internal Cells (MAU) | 75 | 75 | 240 | 528 | 1600 | 5904 | 2624 Plus RAM | 5920 | 10266 |
| Internal Gate Delay | 150PS | 150PS | 150PS | 150PS | 150PS | 150PS | 150PS | 150PS | 150PS |
| Speed/Power Options | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| 100K/10K/10KH Compatible | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes | Yes |
| ECL/TTL Mixed I/O | 22 | 0 | 36 | 72 | 128 | 0 | 0 | 220 | 0 |
| ECL Only I/O | 0 | 22 | 12 | 0 | 0 | 256 | 256 | 0 | 256 |
| Power/Ground | 6 | 6 | 12 | 40 | 48 | 56 | 56 | 72 | 56 |
| Typical Power (W) | 0.5-1.0 | 0.5-1.0 | 0.5-1.5 | 1-3 | 3-6 | 10-20 | 10-20 | 10-20 | 15-30 |
| Standard Packages | 16, 24 Metal Flat 28 PLCC/LDCC | 16, 24 Metal Flat 28 PLCC/LDCC | 44LDCC 75PGA | 109PGA 116LDCC 75PGA* | 173PGA 172LDCC 99PGA** | 323PGA | 323PGA | 303PGA | 323PGA |
| Available | Now | Now | Now | Now | Now | Now | Now | Now | 1Q90 |

*Maximum of 48 I/O

**Maximum of 64 I/O

ASPECT Process

FGA Series arrays use a National proprietary process called ASPECT which uses conservative 1.5-micron design rules to achieve VLSI density and 150 ps typical internal gate delays at thirty percent of conventional ECL power consumption levels.

ASPECT is the first bipolar process to use polysilicon for emitter and base structures. Polysilicide serves as a source of impurities for both the emitter and the base. This permits the fabrication of extremely shallow (500Å below the surface) emitters and narrow base regions. The combination of shallow emitters and base leads to transistors with a very high switching speed. ASPECT also uses polysilicon resistors.

Such resistors exhibit low junction capacitance, making them ideal passive elements for high-speed logic circuits.

An important feature is the self-aligning process used in ASPECT gate arrays. This insensitivity to misalignment makes ASPECT a high-yield process and enables the move to smaller geometries with less difficulty than conventional bipolar processes.

Array Organization

Electrical components (transistors, resistors, diodes and capacitors) are organized into repeating structures called cells, Macros, which are the basic building blocks of gate array logic design, are built by interconnecting the components in one or more cells.

Array Organization (Continued)

The FGA Series employs only two cell types: internal cells and I/O cells. The internal cells are the workhorses of the array, where most of the circuit logic is implemented. All signals going to or coming from the outside world must exit or enter the array through an I/O cell. Since all signal level conversions are performed in the I/O cells, no signal mixing takes place within the array, thus simplifying the design effort. Cell types and their functions are described in greater detail in the following paragraphs.

The bonding pads are located around the periphery of the array. In addition to performing I/O functions, some of the pads are reserved for power and ground busses. Biasing occurs in dedicated routing channels and is optimally performed automatically by placement and routing CAD software.

All FGA Series arrays employ three-layer metalization for signals and bussing. The first metal layer connects components within macros and makes horizontal connections between macros. Layer two is primarily for vertical connections between macros, while layer three contains most of the power bussing. Future versions of the ASPECT process may include four metal layers. In that case, first-layer metal would not be needed to connect macros, thus eliminating routing channels and increasing gate counts for a given die size.

Internal Cell and Logic Complexity

The basic internal cell in an FGA Series array is called a "minimum addressable unit", or MAU. It is the smallest portion of the chip that a CAD system can access for placing or routing.

The number of elements in this minimum cell is actually smaller than on any competing array. In fact, this small, compact cell structure, said to have a fine granularity, increases efficiency. In general, the larger the cell, the greater the likelihood that some cell resources go unused, thereby decreasing efficiency.

Single-level, two-level, and three-level series gated ECL structures are used in FGA Series arrays to implement various logic functions. Series gating allows complex logic functions to be implemented with fewer gates while maintaining optimum performance. Additional logic complexity at no cost in cell utilization may be gained in internal cells by connecting the outputs together (emitter dotting) to form wired-OR functions.

Speed/power options can be used to assign the current settings in each internal cell macro. This feature allows the designer to maximize speed when needed, yet minimize the power consumption. The termination of internal output emitter followers to a $-2V$ internal bus further reduces power consumption.

Typically, internal cell utilization of eighty-five percent is considered optimum. Designs can be completed with up to one-hundred percent utilization; however placement and routing at this level sometimes requires special interactive layout.

The FGA Macro Library contains a number of physical macros with MSI-level complexity. The final portion of this data sheet includes a representative sample of macros included in the FGA Series Macro Library. Full documentation for all macros, including specifications, can be found in the FGA Series Macro Library Reference Manual.

I/O and Interface Capabilities

I/O cells in the FGA Series are capable of performing input, output, transceiver logic and ECL/TTL conversion functions. The array's I/O organization is flexible, with each signal pad supported by a dedicated I/O cell. An incoming signal can enter the internal array through any I/O cell and, after completing the logic implementation, can then exit the array through any I/O cell without restriction.

The flexible functionality of individual I/O cells can be especially useful in system applications requiring latched inputs and outputs. The ability of an FGA Series I/O cell to be

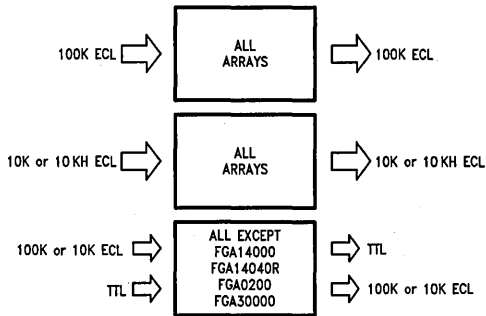
I/O and Interface Capabilities

(Continued)

configured as a latch saves having to use an internal cell for this function. In addition, although most ECL devices drive 50Ω loads, I/Os can be paired to drive 25Ω loads.

Each I/O cell offers a choice of signal termination options. For relatively short signal paths, designers may build series-terminated outputs, simplifying designs in systems where placing termination resistors on the board is not practical. To minimize noise, internal pull-down resistors are provided to keep unused inputs from floating.

Either F100K, 10K, or 10KH interface capability is available on all FGA Series arrays. All input thresholds and logic levels must uniformly belong to the same ECL family. Likewise, the output interface must be the same as that used for input. With the exception of the FGA0200, FGA14000, FGA14040R and FGA30000, each I/O can also be a mixable ECL/TTL I/O. This means that every I/O can be independently configured as either ECL or TTL. The TTL I/O is capable of producing totem-pole, open-collector, or three-state output levels. *Figure 2* illustrates the acceptable interface options for FGA Series arrays.



TL/U/10560-5

FIGURE 2. Interface Capabilities

Embedded RAM

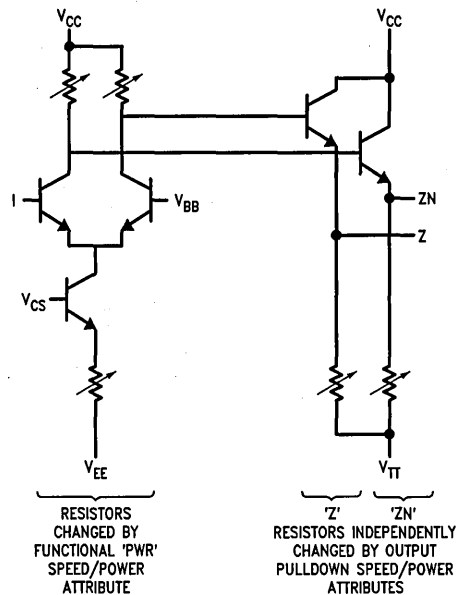
The embedded RAM block is a self-timing memory device with the capabilities of supporting various memory configurations, different bit select patterns, output power options, and different clock systems. The embedded RAM block contains 576 bits, and is organized as 64 words by 9 bits. There are 8 RAM blocks in the FGA14040R with the total of 4608 bits. Each embedded RAM block has its own built-in decoder and control circuit, thus improving system performance and reliability while saving board space. The embedded RAM has three modes of operation, Normal mode, Scan mode and Test mode. At high power operation, the typical access time is 3.75 ns and the worst case access time is 5 ns. Two output drive options, 0.6 mA and 1.2 mA, are available to support the driving capabilities of the embedded RAM. Note that the memory is called self-timed memory device because it generates and shapes its own write strobe internally. This pulse is generated off of the rising edge of the clock which is applied to the embedded RAM.

Speed/Power Options

Speed/power options are a feature of all FGA Series gate arrays. This feature allows the designer to maximize speed where needed, yet minimize overall chip power consumption.

Two sets of macros are available for each logic function in the FGA arrays, the standard macros and the double macros (see Table IV). The double macros use two times as much current as standard macros, and are designed for use in the critical circuitry. These two macro types can be used interchangeably within the same chip.

Essentially, speed/power options are used to assign one or two current values (high = 0.3 mA, low = 0.15 mA) to the current source which controls switching speed; and one of two current values (high = 0.6 mA, low = 0.3 mA) to the true and complement outputs for output drive currents. The latter setting permits zero power consumption for unused outputs. *Figure 3* illustrates circuit options for each of the three settings.



TL/U/10560-6

FIGURE 3. Speed/Power Options

The speed/power options are assigned during schematic capture. Default values for each setting may be specified during schematic capture as well. Designers may use the speed/power options to fine tune the design after placement and routing simply by returning to schematic capture and reassigning values without having to repeat placement and routing.

The examples in Table III illustrate how speed/power options can affect propagation delay vs. power consumption at the macro level. Additional speed/power tradeoffs are listed in "Macro Performance Examples" later in this data sheet.

Speed/Power Options (Continued)

TABLE III. Macro Speed/Power Tradeoffs

| Macro | | Speed (ps) | Power (mW) |
|-------------------|------|------------|------------|
| 2-Input NOR ORN02 | High | 235 | 2.5 |
| | Low | 410 | 1.2 |
| D Flip-Flop DFI01 | High | 415 | 7.5 |
| | Low | 680 | 5.6 |

TABLE IV. Current Setting of Speed/Power Options

| Current μ A | Standard Macro (S) | | Double Macros (D) | |
|-----------------|--------------------|-----------|-------------------|-----------|
| | High Speed | Low Power | High Speed | Low Power |
| Source Current | 300 | 150 | 600 | 300 |
| OEF Current | 600 | 300 | 600 | 300 |

AC Specifications

FGA Series macro propagation delays are specified as MIN, TYP, and MAX values, with variations due to process, power supply and temperature, as shown in the "AC Performance Variations" table.

Macro Performance Examples

The following pages contain performance specifications for some important internal cell macros. Complete information, including design rules and application notes, can be found in the FGA Series Design Manual and FGA Series Macro Library.

AC Performance Variations

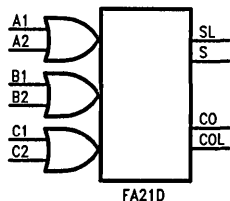
| Variation Type | Derating from Typical (%) (Note 2) | |
|----------------|------------------------------------|------------------|
| | Minimum (Note 1) | Maximum (Note 3) |
| Temperature | -10 | 15 |
| Voltage | ~0 | ~0 |
| Process | -20 | 20 |
| Total | -30% | 35% |

Note 1: Minimum: $T_J = 0^\circ\text{C}$, $V_{EE} = -4.8\text{V}$, Best Case Process

Note 2: Typical: $T_J = 25^\circ\text{C}$, $V_{EE} = -4.5\text{V}$, Normal Process

Note 3: Maximum: $T_J = 125^\circ\text{C}$, $V_{EE} = -4.2\text{V}$, Worst Case Process

FA21D One Bit Full Adder with Gates Inputs



TL/U/10560-7

Propagation Delay (units in ps)

| From Inputs | To Output | High Power | | | Low Power | | |
|-------------|-----------|------------|-----|-----|-----------|-----|-----|
| | | Min | Typ | Max | Min | Typ | Max |
| A1, A2 | S | 330 | 410 | 550 | 420 | 530 | 710 |
| A1, A2 | S | 380 | 470 | 640 | 420 | 530 | 710 |
| B1, B2 | S | 380 | 470 | 640 | 470 | 580 | 790 |
| B1, B2 | S | 450 | 560 | 760 | 490 | 620 | 830 |
| C1, C2 | S | 200 | 250 | 340 | 200 | 250 | 340 |
| C1, C2 | S | 240 | 300 | 400 | 280 | 350 | 480 |
| A1, A2 | CO | 190 | 230 | 310 | 190 | 240 | 330 |
| A1, A2 | CO | 190 | 240 | 330 | 290 | 360 | 490 |
| B1, B2 | CO | 240 | 300 | 400 | 260 | 330 | 450 |
| B1, B2 | CO | 260 | 330 | 450 | 380 | 470 | 640 |
| C1, C2 | CO | 240 | 300 | 400 | 260 | 330 | 450 |
| C1, C2 | CO | 260 | 330 | 450 | 380 | 470 | 640 |

Macro Performance Examples (Continued)

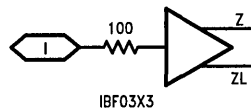
Current in Base Macro

| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| IEE (mA) | | | |
| HIGH | 1.36 | 1.80 | 2.26 |
| LOW | 0.92 | 1.20 | 1.52 |
| ITT (mA) | | | |
| HIGH | 0.21 | 0.30 | 0.39 |
| LOW | 0.21 | 0.30 | 0.39 |

Current in Macro Outputs

| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| ITT (mA) | | | |
| HIGH | 0.42 | 0.60 | 0.78 |
| LOW | 0.21 | 0.30 | 0.39 |

IBF03X2(3) Input Buffer



IBF03X3

TL/U/10560-8

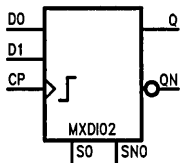
Propagation Delay (units in ps)

| From Input | To Outputs | Min | Typ | Max |
|------------|------------|-----|-----|-----|
| I | Z, ZL | 220 | 280 | 380 |
| I | Z, ZL | 220 | 280 | 380 |

Current in Base Macro

| Min | Typ | Max |
|-----------------|------|------|
| IEE (mA) | | |
| 0.60 | 0.80 | 1.0 |
| ITT (mA) | | |
| 0.84 | 1.20 | 1.56 |

MXDIO2—D Flip Flop with Multiplexed Data Inputs



TL/U/10560-9

Propagation Delay (units in ps)

| From Input | To Output | High Power | | | Low Power | | |
|------------|-----------|------------|-----|-----|-----------|-----|-----|
| | | Min | Typ | Max | Min | Typ | Max |
| CP | Q | 340 | 420 | 570 | 530 | 660 | 890 |
| CP | Q | 300 | 380 | 510 | 530 | 660 | 890 |
| CP | QN | 340 | 430 | 580 | 540 | 670 | 910 |
| CP | QN | 310 | 390 | 530 | 540 | 680 | 920 |

Current in Base Macro

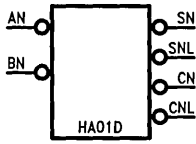
| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| IEE (mA) | | | |
| HIGH | 0.92 | 1.20 | 1.52 |
| LOW | 0.68 | 0.90 | 1.14 |
| ITT (mA) | | | |
| HIGH | 0.84 | 1.20 | 1.56 |
| LOW | 0.84 | 1.20 | 1.56 |

Current in Macro Outputs

| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| ITT (mA) | | | |
| HIGH | 0.42 | 0.60 | 0.78 |
| LOW | 0.21 | 0.30 | 0.39 |

Macro Performance Examples (Continued)

HA01D—Half Adder



TL/U/10560-10

Propagation Delay (units in ps)

| From Inputs | To Output | High Power | | | Low Power | | |
|-------------|-----------|------------|-----|-----|-----------|-----|-----|
| | | Min | Typ | Max | Min | Typ | Max |
| AN | SN ↗ | 160 | 200 | 270 | 160 | 200 | 270 |
| AN | SN ↘ | 170 | 210 | 280 | 200 | 250 | 340 |
| AN | CN ↗ | 150 | 190 | 250 | 140 | 180 | 240 |
| AN | CN ↘ | 150 | 190 | 250 | 190 | 230 | 310 |
| BN | SN ↗ | 200 | 250 | 340 | 190 | 240 | 330 |
| BN | SN ↘ | 230 | 290 | 390 | 270 | 340 | 460 |
| BN | CN ↗ | 200 | 250 | 340 | 200 | 250 | 340 |
| BN | CN ↘ | 220 | 280 | 370 | 270 | 340 | 460 |

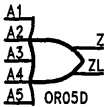
Current in Base Macro

| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| IEE (mA) | | | |
| HIGH | 0.68 | 0.90 | 1.13 |
| LOW | 0.46 | 0.60 | 0.76 |

Current in Macro Outputs

| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| ITT (mA) | | | |
| HIGH | 0.42 | 0.60 | 0.78 |
| LOW | 0.21 | 0.30 | 0.39 |

OR05D—5 Input OR Gate



TL/U/10560-11

Propagation Delay (units in ps)

| From Input | To Outputs | High Power | | | Low Power | | |
|------------|------------|------------|-----|-----|-----------|-----|-----|
| | | Min | Typ | Max | Min | Typ | Max |
| A | Z, ZL ↗ | 160 | 200 | 270 | 180 | 230 | 310 |
| A | Z, ZL ↘ | 160 | 200 | 270 | 200 | 250 | 340 |

Current in Base Macro

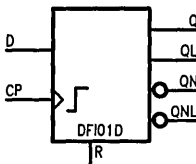
| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| IEE (mA) | | | |
| HIGH | 0.45 | 0.60 | 0.75 |
| LOW | 0.23 | 0.30 | 0.38 |

Current in Macro Outputs

ITT (mA) for each macro output used:

| Power ATT | Min | Typ | Max |
|-----------|------|------|------|
| HIGH | 0.42 | 0.60 | 0.78 |
| LOW | 0.21 | 0.30 | 0.39 |

DFI01D—D Flip Flop with Reset



TL/U/10560-12

Propagation Delay (units in ps)

| From Inputs | To Output | High Power | | | Low Power | | |
|----------------|-----------|------------|-----|-----|-----------|-----|-----|
| | | Min | Typ | Max | Min | Typ | Max |
| CP | Q ↗ | 340 | 420 | 570 | 500 | 620 | 840 |
| CP | Q ↘ | 350 | 430 | 580 | 380 | 480 | 650 |
| CP | QN ↗ | 310 | 390 | 530 | 400 | 500 | 680 |
| CP | QN ↘ | 340 | 430 | 580 | 400 | 490 | 670 |
| CP LOW | | | | | | | |
| R | Q ↗ | 300 | 380 | 510 | 550 | 680 | 920 |
| R | Q ↘ | 350 | 430 | 590 | 490 | 610 | 820 |
| CP HIGH | | | | | | | |
| R | Q ↗ | 370 | 460 | 620 | 560 | 710 | 950 |
| R | QN ↗ | 370 | 460 | 630 | 520 | 650 | 880 |

Macro Performance Examples (Continued)

Current In Base Macro

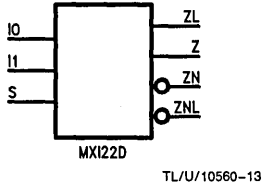
| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| IEE (mA) | | | |
| HIGH | 1.13 | 1.50 | 1.88 |
| LOW | 0.69 | 0.90 | 1.14 |
| ITT (mA) | | | |
| HIGH | 0.84 | 1.20 | 1.56 |
| LOW | 0.84 | 1.20 | 1.56 |

Current In Macro Outputs

| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| ITT (mA) | | | |
| HIGH | 0.42 | 0.60 | 0.78 |
| LOW (Note 1) | 0.21 | 0.30 | 0.39 |

Note 1: Output Q is hard wired to 0.6 mA current source and cannot be assigned power attributes.

MXI22D—2:1 Multiplexer



Propagation Delay (units in ps)

| From Input | To Output | High Power | | | Low Power | | |
|------------|-----------|------------|-----|-----|-----------|-----|-----|
| | | Min | Typ | Max | Min | Typ | Max |
| I | Z | 170 | 210 | 280 | 190 | 230 | 310 |
| I | Z | 170 | 210 | 280 | 230 | 290 | 390 |
| I | ZN | 160 | 200 | 270 | 160 | 200 | 270 |
| I | ZN | 170 | 210 | 280 | 200 | 250 | 340 |
| S | Z | 240 | 300 | 400 | 320 | 400 | 540 |
| S | Z | 240 | 300 | 400 | 320 | 400 | 540 |
| S | ZN | 230 | 290 | 390 | 260 | 330 | 450 |
| S | ZN | 230 | 290 | 390 | 260 | 330 | 450 |

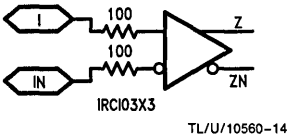
Current In Base Macro

| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| IEE (mA) | | | |
| HIGH | 0.68 | 0.90 | 1.13 |
| LOW | 0.46 | 0.60 | 0.76 |

Current In Macro Outputs

| Power ATT | Min | Typ | Max |
|-----------------|------|------|------|
| ITT (mA) | | | |
| HIGH | 0.42 | 0.60 | 0.78 |
| LOW | 0.21 | 0.30 | 0.39 |

IRCI03X2 (3)—Differential Input Buffer



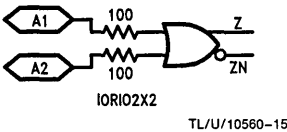
Propagation Delay (units in ps)

| From Inputs | To Output | Min | Typ | Max |
|-------------|-----------|-----|-----|-----|
| I, IN | Z | 120 | 150 | 210 |
| I, IN | Z | 120 | 150 | 210 |
| I, IN | ZN | 120 | 150 | 210 |
| I, IN | ZN | 120 | 150 | 210 |

Current In Base Macro

| Min | Typ | Max |
|-----------------|------|------|
| IEE (mA) | | |
| 0.60 | 0.80 | 1.0 |
| ITT (mA) | | |
| 0.84 | 1.20 | 1.56 |

I0RI02X2—2 Input OR/NOR Gate



Propagation Delay (units in ps)

| From Input | To Outputs | Min | Typ | Max |
|------------|------------|-----|-----|-----|
| A | Z | 190 | 240 | 320 |
| A | Z | 180 | 230 | 310 |
| A | ZN | 160 | 200 | 270 |
| A | ZN | 200 | 250 | 340 |

Current In Base Macro

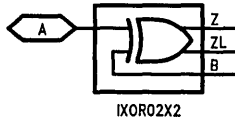
| Min | Typ | Max |
|-----------------|------|-----|
| IEE (mA) | | |
| 0.60 | 0.80 | 1.0 |

Current In Macro Outputs

| Min | Typ | Max |
|-----------------|------|------|
| ITT (mA) | | |
| 0.84 | 1.20 | 1.56 |

Macro Performance Examples (Continued)

IXOR02X2—2 Input XOR Gate



IXOR02X2

TL/U/10560-16

Propagation Delay (units in ps)

| From Input | To Outputs | Min | Typ | Max |
|------------|------------|-----|-----|-----|
| A | Z, ZL | 210 | 270 | 370 |
| A | Z, ZL | 190 | 240 | 320 |
| A | Z, ZL | 330 | 410 | 550 |
| A | Z, ZL | 300 | 380 | 510 |

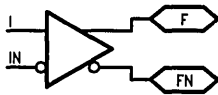
Current in Base Macro

| Min | Typ | Max |
|-----------------|------|-----|
| IEE (mA) | | |
| 1.20 | 1.60 | 2.0 |

Current in Macro Outputs

| Min | Typ | Max |
|-----------------|------|------|
| ITT (mA) | | |
| 0.84 | 1.20 | 1.56 |

RCRI5OX3—Differential Output Buffer



RCRI5OX3

TL/U/10560-17

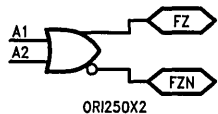
Propagation Delay (units in ps)

| From Inputs | To Outputs | Min | Typ | Max |
|-------------|------------|-----|-----|-----|
| I, IN | FZ, FZN | 400 | 470 | 640 |
| I, IN | FZ, FZN | 300 | 370 | 500 |

Current in Base Macro

| Min | Typ | Max |
|-----------------|------|------|
| IEE (mA) | | |
| 4.35 | 5.80 | 7.25 |

Propagation Delay (units in ps)



ORI25OX2

TL/U/10560-18

| From Input | To Output | Min | Typ | Max |
|------------|-----------|-----|-----|-----|
| A | FZ | 290 | 360 | 490 |
| A | FZ | 290 | 360 | 490 |
| A | FZN | 280 | 350 | 470 |
| A | FZN | 290 | 360 | 490 |

Current in Base Macro

| Min | Typ | Max |
|-----------------|------|------|
| IEE (mA) | | |
| 4.95 | 6.60 | 8.25 |

Current in Macro Outputs

| Min | Typ | Max |
|-------------------|------|------|
| IVCCA (mA) | | |
| 23.8 | 28.0 | 32.2 |

Macro Cells Library

Internal Macros

| Name | Function | Cells |
|---------------------------|-------------------------------------|-------|
| BUFFERS, INVERTERS | | |
| BF01 | Buffer | 1 |
| BFI01 | Buffer/Inverter | 2 |
| RCR01D | Differential Receiver/Buffer | 1 |
| RCR11D | Differential Receiver/Buffer | 1 |
| RCRI01 | Differential Receiver/Buffer | 2 |
| RCRN01 | Inverting Differential Receiver | 1 |
| GATES | | |
| ANI02 | 2-Input AND/NAND | 2 |
| OAI23D | 3-3 OR/AND—Invert | 2 |
| OAI23S | 3-3 OR/AND—Invert, 1.2 mA loef | 4 |
| OAI24 | 4-4 OR/AND—Invert | 2 |
| OAI32DT | 2-2-2 OR/AND—Invert | 3 |
| OAI44D | 4-3-3-3 OR/AND—Invert | 4 |
| OAI44S | 4-3-3-3 OR/AND—Invert | 4 |
| OAI46 | 5-4-5-6 OR/AND—Invert | 5 |
| OAI55DT | 5-4-3-2-1 OR/AND—Invert | 5 |
| OAI66DT | 6-6-4-4-2-2 OR/AND—Invert | 7 |
| OR02 | 2-Input OR | 2 |
| OR02D | 2-Input OR | 1 |
| OR05 | 5-Input OR | 1 |
| OR05D | 5-Input OR | 1 |
| ORI02 | 2-Input OR/NOR | 2 |
| ORI02D | 2-Input OR/NOR | 2 |
| ORI02S | 2-Input OR/NOR | 4 |
| ORI05 | 5-Input OR/NOR | 2 |
| ORI05D | 5-Input OR/NOR | 2 |
| ORI05S | 5-Input OR/NOR, 1.2 mA loef | 4 |
| ORI08 | 8-Input OR/NOR | 2 |
| ORI08D | 8-Input OR/NOR | 2 |
| ORI012D | 12-Input OR/NOR | 3 |
| ORN02 | 2-Input NOR | 2 |
| ORN02D | 2-Input NOR | 1 |
| ORN05 | 5-Input NOR | 1 |
| ORN05D | 5-Input NOR | 1 |
| 2OR02D | Dual 2-Input OR, 0.6 mA loef | 2 |
| 4OR02S | Quad 2-Input OR, 1.2 mA loef | 4 |
| XOR04 | 4-Input XOR | 4 |
| XOR09 | 9-Input XOR | 8 |
| XORI03DT | 3-Input XOR/XNOR | 3 |
| XORI03ST | 3-Input XOR/XNOR, 1.2 mA loef | 4 |
| XORI22D | Gated 2-Input XOR/XNOR | 2 |
| XORI22S | Gated 2-Input XOR/XNOR, 1.2 mA loef | 4 |
| XORI23 | Gated 2-Input XOR/XNOR | 2 |
| XORN04D | 4-Input XNOR | 3 |
| XORN04S | 4-Input XNOR, 1.2 mA loef | 5 |
| XORN06DT | 6-Input XNOR | 5 |

Macro Cells Library (Continued)

Internal Macros (Continued)

| Name | Function | Cells |
|-------------------------------|---|-------|
| DECODERS, MULTIPLEXERS | | |
| DCE02DT | 2:4 Decoder with Enable | 4 |
| DCE22 | 2:4 Decoder with Enable | 4 |
| MX22 | 2:1 MUX | 1 |
| MX34 | 4:1 MUX, 3 Select Inputs | 3 |
| MXI02 | 2:1 MUX, Low Enable, OR Gated Select, Comp. Outputs | 3 |
| MXI02DT | 2:1 MUX, Low Enable, Complement Outputs | 2 |
| MXI02ST | 2:1 MUX, Low Enable, 1.2 mA loef | 4 |
| MXI04 | 4:1 MUX, Low Enable, Complement Outputs | 4 |
| MXI04DT | 4:1 MUX, Complement Outputs | 3 |
| MXI08ST | 8:1 MUX, High Enable, Comp. Outputs 1.2 mA loef | 9 |
| MXI22 | 2:1 MUX, Low Enable, OR Gated Select, Comp. Outputs | 2 |
| MXI22D | 2:1 MUX | 2 |
| MXI24DT | 4:1 MUX, Low Enable, Complementary Outputs | 4 |
| 2MX04DT | Dual 4:1 Multiplexer | 6 |
| 2SELI04D | Dual 4:1 Multiplexer | 5 |
| 4MXI22D | Quad 2:1 Multiplexer | 8 |
| 4MXI22S | Quad 2:1 Multiplexer, 1.2 mA loef | 5 |
| LATCHES, MUX LATCHES | | |
| LAI01 | D Latch with Reset and 2-Input OR Enable | 2 |
| FLIP-FLOPS | | |
| 2DFN04 | Dual D Flip-Flop with a Common Clock | 4 |
| DFI01 | M/S D Flip-Flop with Asynchronous Reset | 4 |
| DFI01D | M/S D Flip-Flop with Asynchronous Reset | 4 |
| DFI02 | M/S D Flip-Flop with Set, Reset, Gated Data & Clock | 4 |
| DFI02D | M/S D Flip-Flop with Set, Reset, Gated Data & Clock | 4 |
| DFI02DT | M/S D Flip-Flop with Active Low Enable | 4 |
| DFI04 | M/S D Flip-Flop, Positive Edge Triggered | 3 |
| DFI21 | M/S D Flip-Flop with Asynchronous Reset | 3 |
| DFI22 | M/S D Flip-Flop with Scan Input | 4 |
| DFS02DT | M/S D Flip-Flop with Scan Input | 5 |
| DFS02ST | M/S D Flip-Flop with Scan Input, 1.2 mA loef | 7 |
| DFS21DT | M/S D Flip-Flop with Scan Input, Data Enable | 5 |
| DFS21ST | M/S D Flip-Flop with Scan Input, Data Enable, 1.2 mA loef | 7 |
| JKI02 | M/S JN-K Flip-Flop | 4 |
| MXDI02 | M/S D Flip-Flop with Multiplexed Data Input | 4 |
| COMPARATORS | | |
| None Available at This Time | | |
| MISCELLANEOUS | | |
| AD01 | 1-Bit Carry Look Ahead Adder | 3 |
| FA21D | 1-Bit Full Adder w/Gated Inputs | 4 |
| FA21S | 1-Bit Full Adder w/Gated Inputs, 1.2 mA loef | 8 |
| HA01D | 1-Bit Half Adder | 2 |
| HLI01 | High-Low Level Generator with Temperature Diode | 1 |
| MEMORY | | |
| IDC02X2 | Shared Input Buffer, 0.6 mA loef | 1 |
| IDC12X2 | Shared Input Buffer, 0.6 mA loef | 1 |
| MTX50X2 | Shared Output Buffer, 50Ω | 1 |
| RS69D | 64 X 9 RAM | |

Macro Cells Library (Continued)

Input Macros

| Name | Function | Cells |
|-------------------------------|---|-------|
| BUFFERS, INVERTERS | | |
| IBF02X2 (3) | High Fan-Out Buffer, 10 mA loef (Note 1) | 1 |
| IBF03X2 (3) | Input Buffer, 0.6 mA loef | 1 |
| IBF103X2 (3) | Input Buffer, Complementary Outputs, 0.6 mA loef | 1 |
| IBFN03X2 | Input Buffer, Inverting 0.6 mA loef | 1 |
| DIFFERENTIAL RECEIVERS | | |
| ICKD0X2 | Differential Input Clock Driver, 18 mA loef (Note 1) | 2 |
| ICKD0X3 | Differential Input Clock Driver, 18 mA loef (Note 1) | 2 |
| ICKD1X2 | Differential Input Clock Driver, 18 mA loef (Note 2) | 2 |
| IRCI02X2 (3) | Differential Input Buffer, Comp. Outputs, 10 mA loef | 2 |
| IRCI03X2 (3) | Differential Input Buffer, Comp. Outputs, 0.6 mA loef | 2 |
| GATES | | |
| IOR02X2 | 2-Input OR, 0.6 mA loef | 2 |
| IORI02X2 | 2-Input OR/NOR, 0.6 mA loef | 2 |
| IORN02X2 | 2-Input NOR, 0.6 mA loef | 2 |
| IXOR02X2 | 2-Input XOR, 0.6 mA loef | 1 |
| IXORN2X2 | 2-Input XNOR, 0.6 mA loef | 1 |

MISCELLANEOUS

| | | |
|------------|-----------------------------|---|
| IN00X2 (3) | Input Pad (Zero Resistance) | 1 |
|------------|-----------------------------|---|

Note 1: ICKD0X2 and ICKD0X3 uses two external cells for electrical connection and cover, respectively, 90 and 50 internal cells for clock distribution.

Note 2: ICKD12X2 uses two external cells for electrical connection and covers 44 internal cells for clock distribution.

Output Macros

| Name | Function | Cells |
|---------------------------|---|-------|
| BUFFERS, INVERTERS | | |
| BF50X2 (3) | Output Buffer, 50Ω, F100K | 1 |
| BFI50X3 | Complementary Output Buffer, 50Ω, F100K | 2 |
| BFN50X2 | Output Inverter, 50Ω, F100K | 1 |
| RCRI50X3 | Differential Output Buffer, 50Ω, F100K | 2 |
| GATES | | |
| OR220X2 | 2-Input OR, 25Ω, F100K | 1 |
| OR1220X2 | 2-Input OR/NOR, 25Ω, F100K | 2 |
| OR250X2 | 2-Input OR, 50Ω, F100K | 1 |
| ORN250X2 | 2-Input NOR, 50Ω, F100K | 1 |
| ORI250X2 | 2-Input OR/NOR, 50Ω, F100K (FGA 14K) | 2 |
| ORI250X3 | 2-Input OR/NOR, 50Ω, F100K (FGA 4K) | 2 |
| OR450X2 | 4-Input OR, 50Ω, F100K | 1 |
| ORN450X2 | 4-Input NOR, 50Ω, F100K | 1 |
| ORI450X2 | 4-Input OR/NOR, 50Ω, F100K | 2 |
| BUS DRIVERS | | |
| BD20X2 | 2-Input OR, 25Ω, F100K | 1 |
| BDN20X2 (3) | 2-Input NOR, 25Ω, F100K | 1 |

Macro Cells Library (Continued)**Transceivers**

| Name | Function | Cells |
|-------------|--|-------|
| TR20X3 | 2-Input OR ECL Transceiver, 25 Ω | 1 |
| TRN20X3 | 2-Input NOR ECL Transceiver, 25 Ω | 1 |
| TRN50X2 (3) | 2-Input NOR ECL Transceiver, 50 Ω | 1 |

Miscellaneous

| Name | Function | Cells |
|-------------|------------------------------|-------|
| OUT00X2 (3) | Output Pad (Zero Resistance) | 1 |

TTL Macros

| Name | Function | Cells |
|------|----------|-------|
|------|----------|-------|

INPUT BUFFERS

| | | |
|---------|-----------------------------|---|
| TED11X3 | TTL Input Buffer | 1 |
| TES11X3 | TTL Input Buffer (+5V Only) | 1 |

OUTPUT BUFFERS

| | | |
|----------|------------------------------------|---|
| TOBD01X3 | 8 mA TTL Output Buffer | 1 |
| TOBD11X3 | 20 mA TTL Output Buffer | 1 |
| TOBS11X3 | 20 mA TTL Output Buffer (+5V Only) | 1 |

TRANSCIVERS

| | | |
|----------|---------------------------------|---|
| TTRD11X3 | 20 mA TTL Transceiver | 1 |
| TTRS01X3 | 8 mA TTL Transceiver (+5V Only) | 1 |



Section 7
**F100K ECL Design Guide
and Application Notes**



Section 7 Contents

| | |
|--|-------|
| Chapter One—Circuit Basics | 7-3 |
| Chapter Two—Logic Design | 7-9 |
| Chapter Three—Transmission Line Concepts | 7-22 |
| Chapter Four—System Considerations | 7-35 |
| Chapter Five—Power Distribution and Thermal Considerations | 7-48 |
| Chapter Six—Testing Techniques | 7-55 |
| Chapter Seven—Quality Assurance and Reliability | 7-62 |
| AN-573 Design Considerations for High Speed Architectures | 7-67 |
| AN-582 Using the F100250 for Copper Wire Data Communications | 7-75 |
| AN-650 The ECL System Solution | 7-88 |
| AN-651 10K vs 100K ECL I/O System Considerations | 7-92 |
| AN-682 Terminating F100K ECL Inputs | 7-96 |
| AN-683 300 MHz Dual Eight-Way Multiplexer/Demultiplexer | 7-98 |
| AN-684 F100336 Four Stage Counter/Shift Register | 7-100 |
| AN-685 Using the F100181 ALU and F100179 Carry Look-Ahead | 7-107 |

Chapter 1 Circuit Basics

Introduction

ECL circuits, except for the simplest elements, are schematically formidable and many of the specified parameters are relatively unfamiliar to system designers. The relationships between external parameters and internal circuitry are best determined by individually examining the fundamental sub-circuits of a simple element. System variables such as supply voltage tolerances and temperature have predictable effects on circuit parameters, thus allowing a systematic evaluation of noise margins.

Basic ECL Switch

At the bottom of every ECL circuit, literally and figuratively, is a current source. In the basic ECL switch (*Figure 1-1*), a logic operation consists of steering the current through either of two return paths to V_{CC} ; the state of the switch can be detected from the resultant voltage drop across $R1$ or $R2$. The net voltage swing is determined by the value of the resistors and the magnitude of the current. Further, these two values are chosen to accomplish the charging and discharging of all of the parasitic capacitances at the desired switching rate.

Required Input Signal

The voltage swing required to control the state of the switch is relatively small due to the exponential change of emitter current with base-emitter voltage and to the differential mode of operation. For example, starting from a condition where the two base voltages are equal, which causes the current to divide equally between $Q1$ and $Q2$, an increase of V_{IN} by 125 mV causes essentially all of the current to flow through $Q1$. Conversely, decreasing V_{IN} by 125 mV causes essentially all of the current to flow through $Q2$. Thus the minimum signal swing required to accomplish switching is 250 mV centered about V_{BB} . The signal swing is made larger (approximately 750 mV) to provide noise immunity and to allow for differences between the V_{BB} of one circuit and the output voltage levels of another circuit driving it.

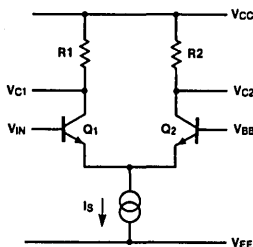


FIGURE 1-1. Basic ECL Switch

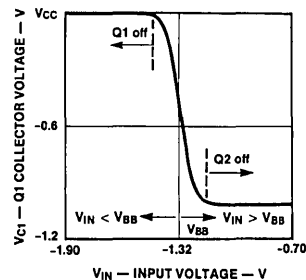
TL/F/9905-1

Transition Region

If the voltage at the collector of $Q1$ is monitored while varying V_{IN} above and below the value of V_{BB} , the relationship between V_{C1} and V_{IN} appears as shown in *Figure 1-2*. Note that the horizontal axis of the graph is centered on V_{BB} ; this emphasizes the importance of V_{BB} in fixing the location of the transition region. The shape of the transition (or threshold) region is governed by the transistor characteristics and the value of current to be switched. Both of these factors are determined by the circuit designer. The shape of the transition region is essentially invariant over a broad range of conditions, due to the matching of transistor characteristics inherent with IC technology and because the transistors are at the same temperature. The inherent matching of IC resistors assures equal voltage swings at the two collectors.

Emitter-Follower Buffers

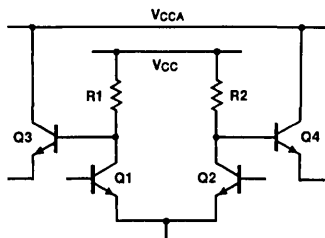
In *Figure 1-2*, V_{C1} ranges from V_{CC} (ground) when $Q1$ is off to approximately $-0.90V$ when $Q1$ is conducting all of the source current. To make these voltage levels compatible with the voltages required to drive the input of another current switch, emitter followers are added as shown in the buffered current switch (*Figure 1-3*). In addition to translating V_{C1} and V_{C2} downward, the emitter followers also isolate the collector nodes from load capacitance and provide current gain. Since the output impedance of the emitter followers is low (approximately 7Ω), ECL circuits can drive transmission lines—coaxial cables, twisted pairs, and etched circuits—having characteristic impedances of 50Ω or more.



TL/F/9905-2

FIGURE 1-2. V_{C1} - V_{IN} Transition Region

Emitter-Follower Buffers (Continued)



TL/F/9905-3

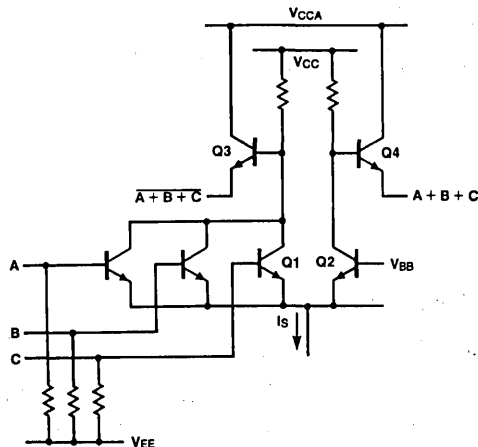
FIGURE 1-3. Buffered Current Switch

In this buffered current switch, the collectors of Q3 and Q4 return to a separate ground lead, V_{CCA} . This separation insures that any changes in load currents during switching do not cause a change in V_{CC} through the small but finite inductance of the V_{CCA} bond wire and package lead. Outside the package, the V_{CC} and V_{CCA} leads should be connected to the common V_{CC} distribution.

For internal functions of complex circuits where loading is minimal, the buffer transistors are scaled down to maintain high switching speeds with modest source currents. For service as output buffers, the emitter followers are designed for a maximum rated output current of 50 mA. For standardization of testing, detailed specifications on guaranteed min/max output levels apply when an output is loaded with 50Ω returned to $-2V$. The emitter followers have no internal pull-down resistors; consequently, there is maximum design flexibility when optimizing line terminations and using wired-OR techniques for combinatorial logic or data bussing.

Multiple Inputs

The buffered switch of *Figure 1-3* is essentially an ECL line receiver circuit with the bases of both Q1 and Q2 available for receiving differential signals. With one input connected to the V_{BB} terminal, the switch can receive a signal transmitted in a single-ended mode or it can act as a buffer or logic inverter. To perform the OR and NOR of two or more functions, additional transistors are connected in parallel with Q1 as indicated in *Figure 1-4*. When any input is HIGH, its associated transistor conducts the source current and Q2 is turned off; this causes the collector of Q1 to go LOW and the collector of Q2 to go HIGH, with the emitters of Q3 and Q4 following the collectors of Q1 and Q2 respectively. When two or more inputs are HIGH, the results are the same. Thus, with a HIGH level defined as a True or logic "1" signal, Q3 provides the NOR of the inputs while Q4 simultaneously provides the OR. In addition to the logic design flexibility afforded by the availability of both the assertion and negation, the Q3 and Q4 outputs can drive both conductors of a differential pair for data transmission. Also shown in *Figure 1-4* are the pull-down resistors, nominally $50\text{ k}\Omega$, connected between ECL inputs and the negative supply. These resistors serve the purpose of holding unused inputs in the LOW state by sinking I_{CBO} current and preventing the build-up of charge on input capacitances. Accordingly, most non-essential ECL inputs are designed to be active HIGH. When such inputs are not used, the pull-down resistors eliminate the need for external wiring to hold them LOW.



TL/F/9905-4

FIGURE 1-4. Input Expansion by Parallel Transistors

Power Conservation, Complementary Functions

Power dissipation in an ECL circuit is due in part to the output load currents and in part to the internal operating currents. Load currents depend on system design factors and are discussed in Chapter 5. In the basic switch (*Figure 1-1*), power dissipation is fixed by the source current and the supply voltage, whether the circuit is in a quiescent or transient state. There is no mechanism for causing a current spike such as occurs in TTL circuits, and thus the power dissipation is not a function of switching frequency.

A distinct advantage of the ECL switch is the ease of forming both the assertion and negation of a function without additional time delay or complexity. This is very significant in complex MSI functions, since it helps to maximize the efficiency of the internal logic while minimizing chip area and power consumption. Since most 100K ECL devices have complementary outputs, the system designer has similar opportunities to reduce package count and power consumption while enhancing logic efficiency and reducing throughput times.

Series Gating, Wired-AND

Quite often in ECL elements, the circuitry required to generate functions is much simpler than the detailed logic diagrams suggest. In addition to readily available complementary functions and the wired-OR option, other techniques providing high performance with low part count are series gating and wired collectors. These are illustrated in principle by the simplified schematics of *Figures 1-5* and *1-6*.

Series Gating, Wired-AND (Continued)

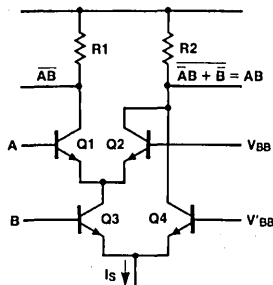


FIGURE 1-5. Series/Parallel Gating

TL/F/9905-5

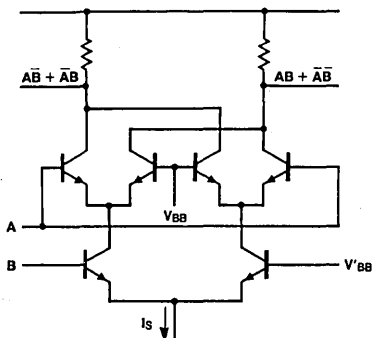


FIGURE 1-6. Exclusive-OR/NOR

TL/F/9905-6

In *Figure 1-5*, if both A and B are HIGH, then Q1 and Q3 conduct and I_S flows through R1, making the collector of Q1 go LOW, thereby achieving the NAND of A and B. Connecting the collectors of Q2 and Q4 to the same load resistor provides the AND of A and B. If the collectors of Q3 and Q4 were interchanged, a different pair of functions of A and B would be produced. Similarly, a third functional pair is achieved by interchanging the collectors of Q1 and Q2. For Q3 and Q4 to operate at a lower voltage level than Q1 and Q2, the voltage level of B is translated downward from the normal ECL levels and V'_{BB} is similarly translated downward from the V_{BB} voltage. In the slightly more complex circuit in *Figure 1-6*, another pair of transistors is added to obtain the Exclusive-OR and Exclusive-NOR functions.

Connecting transistors in series is not limited to two levels of decision making; three levels are shown in the simplified schematic of an octal decoding tree (*Figure 1-7*). If the three input signals are all HIGH, Q1 conducts through Q9 and Q13 to make the collector of Q1 LOW. In all, there are eight possible paths through which the source current can return to the positive supply. A LOW signal at the collector of any one of the transistors in the top row represents a unique combination of the three input signals. This 1-of-8 decoding circuit illustrates very clearly how ECL design techniques make the most efficient use of components and power to generate complex functions. This same set of switches, with the upper collectors wired in two sets of four collectors each, generates the binary sum and its complement of the three input signals.

The Current Source, Output Regulation

All elements of the F100K circuits use a transistor current source illustrated in *Figure 1-8*. Source current is determined by an internally generated reference voltage V_{CS} , the emitter resistor R_S and the base-emitter voltage of Q5. The reference voltage is designed to remain fixed with respect to the negative supply V_{EE} , which makes I_S independent of supply voltage.

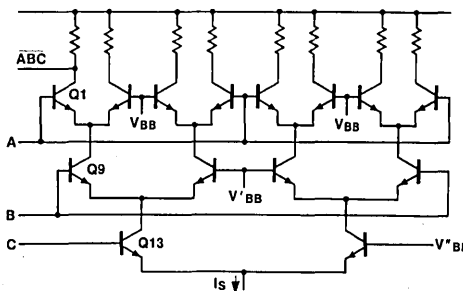


FIGURE 1-7. Octal Decoding Tree

TL/F/9905-7

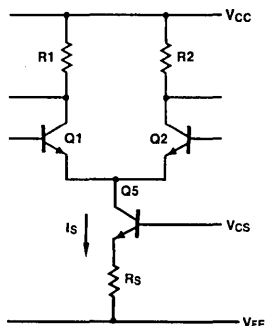


FIGURE 1-8. Constant Current Source for a Switch

TL/F/9905-8

Regulating the current source (I_S) simplifies system design because output voltage and switching parameters are not sensitive to V_{EE} changes. Output voltage levels are determined primarily by the voltage drops across R1 and R2 resulting from the collector currents of Q1 and Q2. Since the collector current of the conducting transistor (Q1 or Q2) is determined by I_S and the transistor α , the voltage drop across the collector load resistor is not sensitive to V_{EE} variations. For example, a 1V change in V_{EE} changes the output level V_{OL} by only 30 mV.

Switching parameters are affected by transistor characteristics, the collector resistor (R1 or R2), stray capacitances, and the amount of current being switched. In other forms of ECL where source currents change with V_{EE} , switching parameters are directly affected. This sensitivity is essentially eliminated in F100K circuits by regulating I_S against V_{EE} changes.

Power dissipation in an ECL switch is the product of I_S and V_{EE} . By holding I_S constant with V_{EE} , incremental changes in dissipation are linear with V_{EE} changes. In non-regulated ECL, I_S increases with V_{EE} causing switch dissipation to change more rapidly with V_{EE} .

Threshold Regulation

As previously discussed, the input threshold region of an ECL switch is centered on the internal reference V_{BB} . In F100K circuits, the on-chip bias driver holds V_{BB} constant with respect to V_{CC} , thus minimizing changes in input thresholds with V_{EE} . For a V_{EE} change of 1V, for example, V_{BB} changes by approximately 25 mV.

With output voltage levels and input thresholds regulated, F100K circuits tolerate large differences in V_{EE} between a driving and a receiving circuit and still maintain good noise margins. For example, a driving circuit operated with $-4.2V$ and receiving circuit operated with $-5.7V$ experience a LOW state noise margin loss of only 30 mV to 40 mV compared to the ideal case of both circuits with $V_{EE} = -4.5V$. This insensitivity to V_{EE} simplifies the design of system power distribution and regulation.

Temperature Compensation

In F100K circuits, input thresholds are made insensitive to temperature by regulating V_{BB} . Output voltage levels are made insensitive to temperature by a correction factor designed into the current source and by a simple network connected between the bases of the output transistors as shown in Figure 1-9.

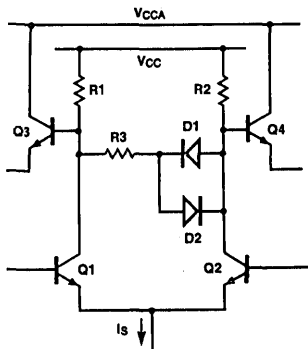


FIGURE 1-9. Temperature Compensation

With Q1 conducting and Q2 off, most of the source current flows through R1, while a small amount flows through R2, D1 and R3. If the chip temperature increases, the source current is made to increase, causing an increase in the voltage drop of sufficient magnitude across R1 to offset the decrease in base-emitter voltage of Q3. The voltage drop across R1 increases with temperature at the rate of approximately $1.5 \text{ mV}/^\circ\text{C}$, while the voltage drop across D1 decreases at the same rate. This means that there is a net voltage increase of $3 \text{ mV}/^\circ\text{C}$ across the series combination of R2 and R3. This increase is equally divided between the two resistors since R3 is equal to R2 (and R1); thus the voltage at the base of Q4 goes negative by $1.5 \text{ mV}/^\circ\text{C}$, offsetting the decrease in the base-emitter voltage of Q4. When Q2 is on and Q1 is off, the same relationships apply except that most of the current flows through R2, and D2 conducts instead of D1. F100K change rates for V_{OH} , V_{BB} , and V_{OL} are approximately 0.06, 0.08 and $0.1 \text{ mV}/^\circ\text{C}$, respectively.

The stabilization of output levels against changes in temperature provides significant advantages to both the user and manufacturer. In testing, an extended thermal stabilization period is not required, nor is an elaborate air cooling arrangement necessary to obtain correlation of test results between user and supplier. In a system, the output signal swing of a circuit does not depend on its temperature, therefore temperature differences do not cause a mismatch in signal levels between various locations. With temperature gradients thus eliminated as a system constraint, the design of the cooling system is greatly simplified.

Noise Margins

The most conservative values of ECL noise margins are based on the DC test conditions and limits listed on the data sheets. Acceptance limits on V_{OH} and V_{OL} are identified on a symbolic waveform in Figure 1-10, with the boundaries of the input threshold region also identified. The HIGH-state noise margin is usually defined as the difference between $V_{OH(\text{Min})}$ and $V_{IH(\text{Min})}$, with the LOW-state margin defined as the difference between $V_{OL(\text{Max})}$ and $V_{IL(\text{Max})}$. These two differences are identified as V_{NH} and V_{NL} respectively. The worst case input and output test points are also identified on the OR gate transfer function shown in Figure 1-11. The transition region indicated by the solid line is applicable when the internal reference V_{BB} has the design center value of $-1.32V$ for F100K circuits. The transition regions indicated by the dashed lines represent the lot-to-lot displacement resulting from the normal production tolerances on V_{BB} , which amount to $\pm 40 \text{ mV}$ for F100K circuits. Using F100K circuit values as an example, the dashed curve on the right correlates with a V_{BB} value of $-1.280V$, and the input test voltage $V_{IH(\text{Min})}$ is $-1.165V$, for a net difference of 115 mV. Similarly, the dashed curve on the left applies when V_{BB} is $-1.360V$ with $V_{IL(\text{Max})}$ specified as $-1.475V$, which also gives a net difference of 115 mV. The points V_{OHc} and V_{OLc} are commonly referred to as the *corner points* because of their location on the transfer function of worst case circuits.

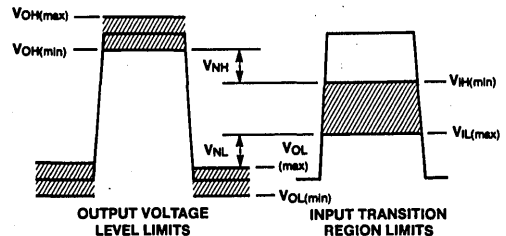


FIGURE 1-10. Identifying Specification Limits on Input and Output Voltage Levels

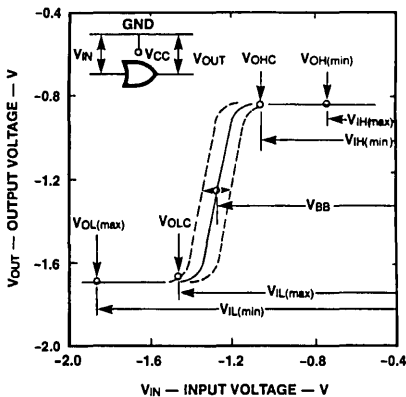
In actual system operation, the noise margins V_{NH} and V_{NL} are quite conservative because of the way $V_{IH(\text{Min})}$ and $V_{IL(\text{Max})}$ are defined. From the transfer function of Figure 1-11, for example, $V_{IH(\text{Min})}$ is defined as a value of input voltage which causes a worst-case output to decrease from $V_{OH(\text{Min})}$ to V_{OHc} . This change in V_{OH} amounts to only 10 mV for F100K circuits. Thus, if a worst case OR gate has a quiescent input of $V_{OH(\text{Min})}$, a superimposed negative-going disturbance of amplitude V_{NH} causes an output change of only 10 mV, assuming that the time duration of the disturbance is sufficient for the OR gate to respond fully. In

Noise Margins (Continued)

contrast, a system fault does not occur unless the superimposed noise at the OR input is of sufficient amplitude to cause the output response to extend into the threshold region(s) of the load(s) driven by the OR gate. In general, noise becomes intolerable when it propagates through a string of gates and arrives at the input of a regenerative circuit (flip-flop, counter, shift register, etc.) with sufficient amplitude to reach the V_{BB} level.

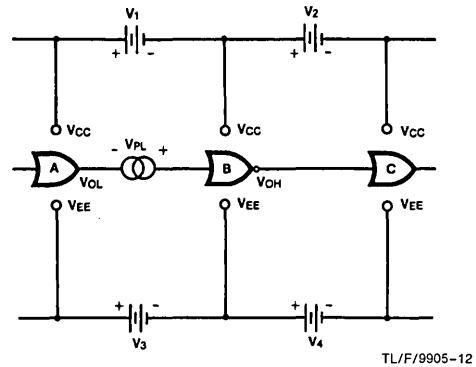
The critical requirement for propagating either a signal or noise through a string of gates is that each output must exhibit an excursion to the V_{BB} level of the next gate in the string, assuming, of course, that the time duration is sufficient to allow full response. If the excursion at the input of a particular gate either falls short or exceeds V_{BB} , the effect on its output response is magnified by the voltage gain of the gate. On the voltage transfer function of a gate, the slope in the transition region is not, strictly speaking, constant. However, for input signal excursions of about ± 50 mV on either side of V_{BB} , a value of 5.5 may be used for the voltage gain. For example, if the noise (or signal) excursion at the input of a gate falls short of V_{BB} by 20 mV, the gate output response is 110 mV less. Another useful relationship is that if the input voltage of a gate is equal to V_{BB} , the output voltage is also equal to V_{BB} , within perhaps 30 mV.

To determine the combined effects of circuit and system parameters on noise propagation through a string of gates, refer to *Figure 1-12*. The voltages V_1 and V_2 represent differences in ground potential, while V_3 and V_4 are V_{EE} differences. The output of gate A is in the quiescent LOW state and V_{PL} is a positive-going disturbance voltage. Now, how large can V_{PL} be without causing propagation through gate C? For a starting point, assume all three gates are identical with typical parameters; V_{EE} is -4.5 V, the ground drops are zero, and there are no temperature gradients. Voltage parameters of F100K circuits are used. With typical circuits and the idealized environment, the maximum tolerable value of V_{PL} for propagation is the difference between the nominal V_{BB} of -1.320 V and nominal V_{OL} of -1.705 V, or 385 mV. The following steps treat each non-ideal factor separately and the required reduction in V_{PL} is calculated.



TL/F/9905-11

FIGURE 1-11. Location of Test Points and Threshold on a Transfer Function



TL/F/9905-12

FIGURE 1-12. Arrangement for Noise Propagation Analysis

Non-Typical V_{BB} of Gate B: Specifications provide for V_{BB} variations of ± 40 mV. If the V_{BB} of gate B is 40 mV more negative than nominal, V_{PL} must be reduced by the same amount.

$$\Delta V_{PL} = -40 \text{ mV}$$

$$V_{PL} = 385 - 40 = 345 \text{ mV}$$

Non-Typical V_{OL} of Gate A: V_{OL} limits are -1.620 V to -1.810 V corresponding to the $\pm 3\sigma$ points on the distribution. Statistically, this means that 98% of the circuits have V_{OL} values of -1.650 V or lower. Since this value differs from the nominal V_{OL} by 55 mV, V_{PL} must be reduced accordingly.

$$\Delta V_{PL} = -55 \text{ mV}$$

$$V_{PL} = 345 - 55 = 290 \text{ mV}$$

Difference in Ground (V_{CC}) Potential between Gates A and B: Since the V_{CC} lead of Gate B is the reference potential for input voltages, V_1 in the polarity shown effectively makes the V_{OL} of Gate A more positive. Minimizing ground drops is one of the system designer's tasks (*Chapter 5*) and its effect on noise margins emphasizes its importance. For this analysis, a value of 30 mV is assumed.

$$\Delta V_{PL} = 30 \text{ mV}$$

$$V_{PL} = 290 - 30 = 260 \text{ mV}$$

Difference in V_{EE} between Gates A and B: In the polarity shown, V_3 reduces the supply voltage for Gate A since it is assumed that Gate B has V_{EE} of -4.5 V. The indicated polarities of V_1 and V_3 seem to be in conflict if it is assumed that V_3 represents only ohmic drops along the V_{EE} bus. Since V_3 may, however, be caused by the use of different power supplies or regulators as well as by ohmic drops, the polarities may exist as indicated. In any actual situation, the designer can usually predict the directions of supply current flow by observation of the physical arrangement. As mentioned earlier, a 1V change in V_{EE} causes a V_{OL} change 30 mV, or 3%. Assuming a value of 0.5V for V_3 and adding the 30 mV of V_1 , the net reduction in supply voltage for Gate A is 0.53V. Using 3% of this reduction as the change in V_{OL} gives a positive V_{OL} shift of 16 mV, which is a reduction of noise margin.

$$\Delta V_{PL} = -16 \text{ mV}$$

$$V_{PL} = 260 - 16 = 244 \text{ mV}$$

If the net supply voltage of Gate A is assumed to be -4.5 V, then V_1 and V_3 cause Gate B to have a greater supply voltage. This, in turn, causes the V_{BB} of Gate B to go more negative at the rate of 25 mV/V of V_{EE} change, or 2.5%.

Noise Margins (Continued)

Thus, for the same values of V_1 and V_3 , the required reduction of V_{PL} is only 13 mV instead of the 16 mV computed above.

Non-Typical V_{BB} of Gate B: This was considered earlier for its effect at the input of Gate B. It must also be considered for its effect on the excursions of the output voltage of Gate B. Since the net input voltage of Gate B ($V_{OL} + V_{PL}$) reaches the V_{BB} level of Gate B, the output excursion also extends to the V_{BB} level and perhaps 30 mV beyond (more negative). This means that the output excursion of Gate B could be 90 mV more negative than the nominal V_{BB} of Gate C. This excess excursion must be divided by the voltage gain of Gate B to determine exactly how much V_{PL} must be reduced as compensation.

$$\Delta V_{PL} = -90/5.5 = -16 \text{ mV}$$

$$V_{PL} = 244 - 16 = 228 \text{ mV}$$

Non-Typical V_{BB} of Gate C: The V_{BB} of Gate C could be 40 mV more positive than the nominal value of -1.320V . Dividing by the voltage gain of Gate B gives the necessary reduction of V_{PL} .

$$\Delta V_{PL} = -40/5.5 = -7 \text{ mV}$$

$$V_{PL} = 228 - 7 = 221 \text{ mV}$$

Difference in V_{CC} Potential between Gates B and C: For the polarity shown, V_2 makes the net voltage at the C input more negative with respect to the V_{CC} lead of Gate C. Assume 30 mV for V_2 as was done for V_1 .

$$\Delta V_{PL} = -30/5.5 = -5.0 \text{ mV}$$

$$V_{PL} = 217 - 5 = 212 \text{ mV}$$

Difference in V_{EE} between Gates B and C: In the polarity shown, V_4 reduces the supply voltage for Gate C, as does V_2 . As previously mentioned, V_{BB} changes with V_{EE} at a rate of 25 mV/V, or 2.5%. Assuming a value of 0.5V for V_4 ,

as was done for V_2 , adding V_2 gives a net V_{EE} reduction of 0.53V. This makes the V_{BB} of Gate C about 13 mV more positive, with respect to its own V_{CC} lead. This must be divided by the gain of Gate B to determine the effect on the permissible value of V_{PL} .

$$\Delta V_{PL} = -13/5.5 \approx -2 \text{ mV}$$

$$V_{PL} = 212 - 2 = 210 \text{ mV}$$

At this point the more conservatively defined V_{NL} (Figure 1-10) should be evaluated and compared with V_{PL} . Subtracting the values of $V_{OL(\text{Max})}$ and $V_{IL(\text{Max})}$, a value of 145 mV for V_{NL} is obtained.

The primary advantage of using V_{NH} and V_{NL} as the limits of tolerable noise is that they provide for simultaneous appearance of noise on inputs and outputs. Whatever the system designer's preference regarding noise margin definitions, the important factor is to recognize that the ΔV_{CC} and ΔV_{EE} between devices decrease the noise margins and therefore should be minimized.

References

1. Marley, R.R., "On-Chip Temperature Compensation for ECL", *Electronic Products*, (March 1, 1971).
2. Marley, R.R., "Design Considerations of Temperature Compensated ECL," *IEEE International Convention*, (March, 1971).
3. Widlar, R.J., "Local IC Regulator for Logic Circuits," *Computer Design*, (May, 1971).
4. Widlar, R.J., "New Developments in IC Voltage Regulators," *ISSCC Digest of Technical Papers*, (February, 1970).
5. Muller, H.H., Owens, W.K., Verhofstadt, P.W.J., "Fully Compensated ECL," *ISSCC Digest of Technical Papers*, (February, 1973).

Chapter 2 Logic Design

Introduction

The F100K family is comprised of SSI, MSI, LSI, logic functions, gate arrays, BiCMOS SRAMs, and PALs. The latest addition to the F100K family is the 300 Series. 300 Series devices are functionally equivalent redesigns of existing F100K devices, but with added enhancements such as: lower power, PCC packaging, extended operating voltage range, military versions and ESD protection of 2000V (minimum).

This chapter covers basic gates and flip-flops, as well as applications using MSI functions. In most cases a 300 Series redesign is available in place of the referenced 100 Series part. Refer to the Applications section of this data-book for the latest publications using ECL logic. Gate Arrays, PALs, and MSI are covered in separate publications. All BiCMOS SRAM applications are included in the Memory Databook.

National F100K ECL logic symbols use the positive logic or "active-HIGH" option of MIL-STD-806B. Logic '1' or "active-High" is the more positive voltage, nearest ground (typically $-0.955V$). Logic '0' or "active-LOW" is the more negative level, nearest V_{EE} (typically $-1.705V$).

OR/NOR Gates

The most basic F100K ECL circuit is the OR/NOR gate (*Figure 2-1*). If the input (A or B) voltages are more negative than the reference voltage V_{BB} , Q1 and Q2 are cut off (non-conducting) and Q3 conducts, holding the collector of Q3

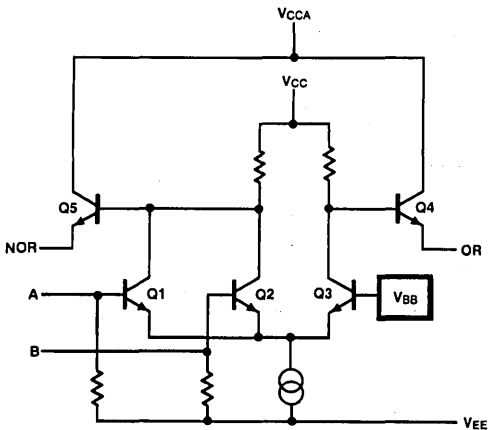
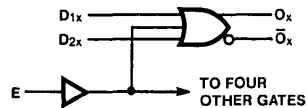


FIGURE 2-1. Basic ECL Gate

TL/F/9899-1

LOW. Since the base of Q4 is LOW, the pull-down resistor or terminator connected to its emitter makes the OR output LOW. The base of Q5 is HIGH (near ground) and its emitter pulls the NOR output HIGH. If either input is more positive than V_{BB} , Q1 or Q2 conducts and Q3 is cut off. This makes the base of Q4 HIGH, resulting in a HIGH at the OR output. At the same time, the base of Q5 is LOW and the pull-down resistors or terminator pulls the NOR output LOW. Detailed information concerning F100K ECL circuit basics may be found in Chapter 1.

The F100K family includes two OR/NOR-gate devices. The F100101 is a triple 5-input OR/NOR and the F100102 is a quint 2-input OR/NOR with common enable. One element of the F100102 is shown in *Figure 2-2*; the corresponding truth table is Table 2-1.



TL/F/9899-2

FIGURE 2-2. F100102 OR/NOR Gate

TABLE 2-1. F100102 Truth Table

| D_{1x} | D_{2x} | E | O_x | \bar{O}_x |
|----------|----------|---|-------|-------------|
| L | L | L | L | H |
| L | L | H | H | L |
| L | H | L | H | L |
| L | H | H | H | L |
| H | L | L | H | L |
| H | L | H | H | L |
| H | H | L | H | L |
| H | H | H | H | L |

H = HIGH Voltage Level

L = LOW Voltage Level

Wired-OR Function

A wired-OR function can be implemented simply by connecting the appropriate outputs external to the package (see *Figure 2-3*). Each output is buffered so that the internal logic is not affected by the wire-OR. This is a positive logic OR, not to be confused with a DTL wired-AND or the internal series gating used for some ECL functions. This wired-OR is especially useful in implementing data busses. For further information see Chapter 4.

Wired-OR Function (Continued)

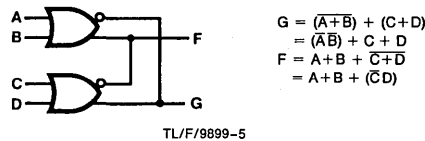
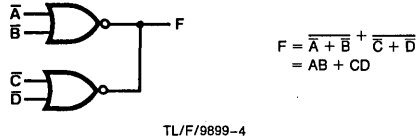
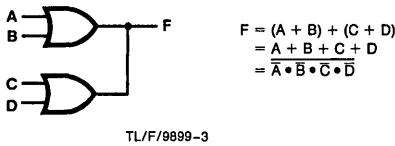


FIGURE 2-3. Wired-OR Function

AND Function

The positive logic AND function is directly available in F100K ECL (F100104). There are two other approaches which can be taken to solve the problem of implementing an AND.

The first solution is indicated in Figure 2-4. A positive logic OR gate can be redrawn as a negative logic AND gate. To take advantage of this requires active-LOW input terms; but, since practically every F100K circuit provides complementary outputs, this should not be a problem.

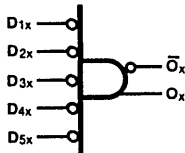


FIGURE 2-4. F100101 Redrawn as AND/NAND Gate

The second possible solution is to use devices in a manner other than that intended, at the cost of package efficiency. The F100117 may be used as a triple 3-input AND/NAND by connecting only one input on each of the OR gates. The F100179 may be used as a single 9-input AND gate by connecting the inputs to \overline{C}_n and \overline{G}_7 through \overline{G}_0 . The \overline{P}_n inputs are left open (LOW) and the output is taken from \overline{C}_{n+8} .

OR-AND, OR-AND-Invert Gates

The F100117 is a triple 2-wide OR-AND, OR-AND-Invert Gate. The logic diagram and truth table for one section of the F100117 are shown in Figure 2-5 and Table 2-2, respectively. The F100118 5-wide OA/OAI has OR inputs of 5, 4, 4, 4, and 2.

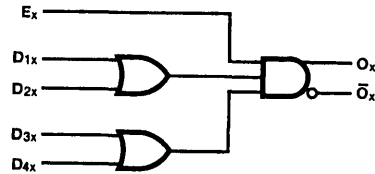


FIGURE 2-5. F100117 OA/OAI Gate

TABLE 2-2. F100117 Truth Table

| E _x | D _{1x} | D _{2x} | D _{3x} | D _{4x} | O _x | O _x [̄] |
|----------------|-----------------|-----------------|-----------------|-----------------|----------------|-----------------------------|
| H | H | X | H | X | H | L |
| H | X | H | X | H | H | L |
| X | L | L | X | X | L | H |
| X | X | X | L | L | L | H |
| L | X | X | X | X | L | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Exclusive-OR/Exclusive-NOR Gate

The F100107 is a quint exclusive OR/NOR gate. In addition to providing the exclusive-OR/exclusive-NOR of the five input pairs, a comparison output is available. If the five pairs of inputs are identical, bit by bit, then the common output will be LOW.

Flip-Flops and Latches

Flip-flops and latches are treated together due to their similarity. The only difference is that latch outputs follow the inputs whenever the enable is LOW, whereas a flip-flop changes output states only on the LOW-to-HIGH clock transition.

The advantage of an edge-triggered flip-flop is that the outputs are stable except while the clock is rising; a latch has better data-to-output propagation delay while the enable is kept active.

Both latches and flip-flops are available three to a package with individual as well as common controls and six to a package with only common controls. There are a total of four parts as indicated below.

| | Triple w/Individual Controls | Hex w/Common Controls |
|------------|------------------------------|-----------------------|
| Flip-Flops | F100131 | F100151 |
| Latches | F100130 | F100150 |

Figure 2-6 shows the equivalent logic diagram of 1/3 of an F100131. The internal clock is the OR of two clock inputs, one common to the other two flip-flops. The OR clock input permits common or individual control of the three flip-flops. In addition, one input may be used as a clock input and the other as an active-LOW enable.

Flip-Flops and Latches (Continued)

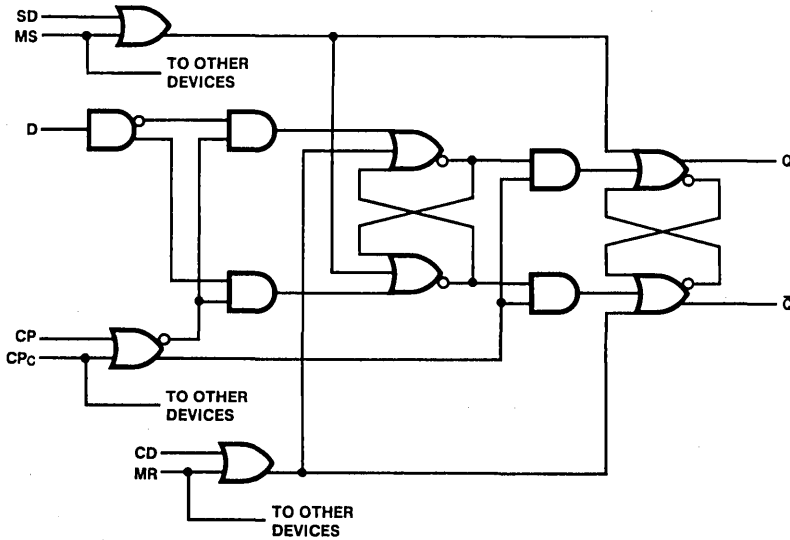


FIGURE 2-6. F100131 D Flip-Flop

TL/F/9899-8

When the clock is LOW, the slave is held steady and the information on the D input is permitted to enter the master. The transition from LOW to HIGH locks the master in its present state making it insensitive to the D input. This transition simultaneously connects the slave to the master, causing the new information to appear at the outputs. Master and slave clock thresholds are internally offset in opposite directions to avoid race conditions or simultaneous master/slave changes when the clock has slow rise or fall times.

The Clear and Set Direct for each flip-flop are the OR of two inputs, one common to the other two flip-flops. The output levels of a flip-flop are unpredictable if both the Set and Clear Direct inputs are active.

The outputs of all F100K flip-flops and latches are buffered. This means that they can be OR-wired; noise appearing on the outputs cannot affect the state of the internal latches.

Table 2-3 is the truth table for the F100131 flip-flop. The truth table for the F100130 latch is similar except the enables are active LOW whereas the F100131 clocks are edge triggered.

TABLE 2-3. F100131 Truth Table

| D _n | CP _n | CP _c | MS SD _n | MR CD _n | Q _n (t + 1) |
|----------------|-----------------|-----------------|-----------------------|-----------------------|------------------------|
| L | | L | L | L | L |
| H | | L | L | L | H |
| L | L | | L | L | L |
| H | L | | L | L | H |
| X | H | X | L | L | Q _n (t) |
| X | X | H | L | L | Q _n (t) |
| X | X | X | H | L | H |
| X | X | X | L | H | L |
| X | X | X | H | H | U |

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care
 U = Undefined
 t, t + 1 = Time before and after CP positive transition

If eight flip-flops are desired, such as for pipeline register applications, the F100141 Shift Register can be used. Neither reset nor complementary outputs are available. The Select inputs may be used to mechanize a clock enable as shown in Figure 2-7.

Flip-Flops and Latches (Continued)

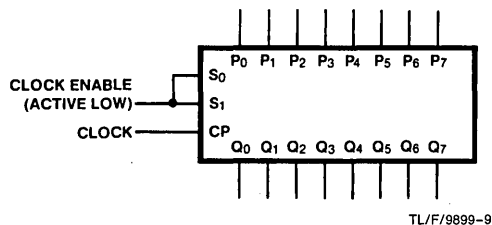


FIGURE 2-7. F100141 as Octal D Flip-Flop

Counters

The F100136 operates either as a modulo-16 up/down counter or as a 4-bit bidirectional shift register. It has three Select inputs which determine the mode of operation as shown in Table 2-4. In addition, a Terminal Count output, and two Count Enables are provided for easy expansion to longer counters. A detailed truth table for the F100136 is included in the specification sheet. To achieve the highest possible speed, complementary outputs should be equally terminated, i.e., if Q_2 is used, \bar{Q}_2 should be equally terminated even if not used. If neither output of a particular stage is used, then both outputs can be left open.

TABLE 2-4. F100136 Function Select Table

| S ₀ | S ₁ | S ₂ | Function |
|----------------|----------------|----------------|-------------|
| L | L | L | Load |
| L | L | H | Count Down |
| L | H | L | Shift Left |
| L | H | H | Count Up |
| H | L | L | Complement |
| H | L | H | Clear |
| H | H | L | Shift Right |
| H | H | H | Hold |

H = HIGH Voltage Level
L = LOW Voltage Level

VARIABLE MODULUS COUNTERS

An F100136 can act as a programmable divider by presetting it via the parallel inputs, counting down to minimum and then presetting it again to start the next cycle. Figure 2-8 shows a one-stage counter capable of dividing by 2 to 15. S_0 and S_1 are unconnected (therefore LOW) and the counter thus is in either the Count Down or Parallel Load mode, depending on whether S_2 is HIGH or LOW, respectively. \overline{CEP} and \overline{CET} are also LOW, enabling counting when S_2 is HIGH. Immediately after the counter is preset to N, which must be greater than one, the \overline{LOAD} signal goes HIGH and the F100136 starts counting down on the next clock. When it counts down to one, the \overline{LOAD} signal goes LOW and pre-setting will occur on the next clock rising edge. Generating the \overline{LOAD} signal on the count of one, rather than zero, makes up for the clock pulse used in presetting.

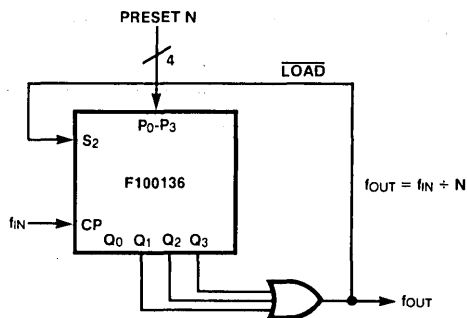


FIGURE 2-8. 1-Stage Counter

A 3-stage programmable divider is shown in Figure 2-9. The \overline{TC} output of the first stage enables counting in the upper stages, while the \overline{TC} output of the second stage also enables counting in the third stage. The D-input signal to the flip-flop is normally HIGH and thus \bar{Q} is normally LOW. When both the second and third stage counters have counted down to zero, the \overline{TC} output of the third stage goes LOW. When the first stage subsequently counts down to one, the D signal goes LOW, as does \overline{LOAD} . Presetting thus occurs on the next clock and \bar{Q} goes HIGH to end the \overline{LOAD} signal and permit counting to resume on the next clock.

In Figure 2-8, the maximum clock frequency is determined by the sum of the propagation delays from CP to Q and the OR gate, plus the setup time from S to CP. The maximum frequency is approximately 220 MHz for typical units or 170 MHz for worst-case units. In Figure 2-9 the critical path is CP to Q of the first stage plus both OR gates, plus the S to CP set-up time of the counters. Typical and worst-case maximum frequencies are 190 MHz and 140 MHz respectively.

INTERCONNECTING COUNTERS

The terminal count and count enable connections provide an easy method of interconnecting the F100136 counter to achieve longer counts. Figure 2-10 shows a method that uses few connections but has a drawback. The counters are fully synchronous, since the clock arrives at all devices at the same time; the only drawback is that the count enables have to "trickle" down the chain. This results in a lower maximum counting rate since it drastically increases the set-up time from enable to clock.

Figure 2-11 shows a method for partially overcoming these drawbacks. The enable to clock set-up is now one \overline{CET} to \overline{TC} propagation delay plus one \overline{CEP} to CP set-up. The count speed is thus increased. This is best seen by assuming that all stages except the second are at terminal count. At the next clock pulse, the second counter reaches terminal count and the first stage exits terminal count. The command to suppress counting in the third and fourth (and subsequent) stages arrives very quickly (via \overline{CEP}). The terminal count from the second stage propagates via \overline{TC} and \overline{CEP} to the high order stages, but has a full 15 counts to do so.

Counters (Continued)

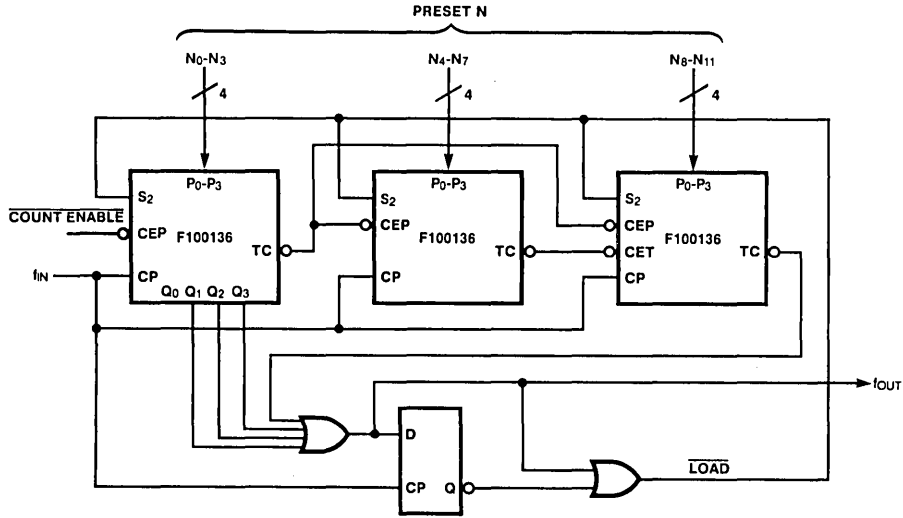


FIGURE 2-9. 3-Stage Programmable Divider

TL/F/9899-11

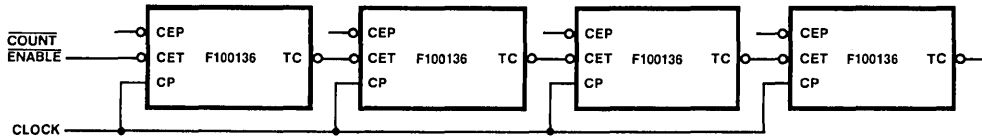


FIGURE 2-10. Slow Expansion Scheme

TL/F/9899-12

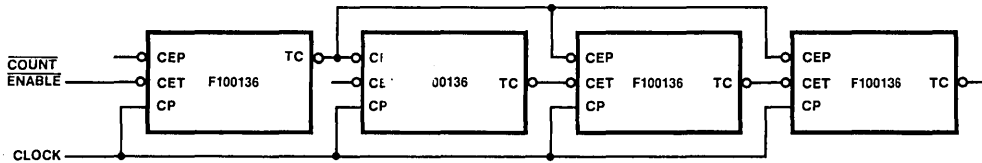


FIGURE 2-11. Fast Expansion Scheme

TL/F/9899-29

Counters (Continued)

DECODING OUTPUTS

Since the complementary outputs from each stage are available, it is an easy matter to decode any value. (Clearly, if many values needed to be decoded one would choose a decoder chip.) *Figure 2-12* shows an F100136 and 1/3 F100101 interconnected to decode 1001 (NINE). Both complementary outputs of NINE are available and there is a spare input on the decoding gate.

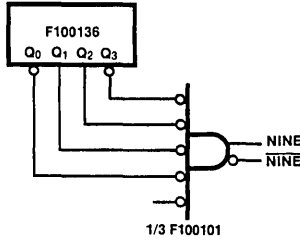


FIGURE 2-12. Decoding States of F100136

Shift Registers

The F100141 is an 8-bit universal shift register. It can be used for parallel-to-serial or serial-to-parallel conversion and it will shift left or right. The truth table is shown in Table 2-5.

TABLE 2-5. F100141 Truth Table

| S ₁ | S ₀ | CP | Mode |
|----------------|----------------|----|--|
| L | L | | Parallel Load |
| L | H | | Shift Left (Q ₀ → Q ₇) |
| H | L | | Shift Right (Q ₇ → Q ₀) |
| H | H | X | Hold |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Figure 2-13 shows the F100141 used as a 7-bit serial-to-parallel converter. When Initialize (INIT) becomes active, the next clock pulse presets the register to '10000000', and Register-Full (REG-FULL) becomes inactive. Each time a data bit becomes available, Data-Available (DATA-AVAIL) must be made active during one clock LOW-to-HIGH tran-

sition. This clocks the bit into the register moves the flag bit closer to Q₀. When the seventh data bit is entered, the flag bit reaches Q₀ and REG-FULL becomes active. The seven data bits may be removed at this time (Q₁ to Q₇) and the conversion is complete.

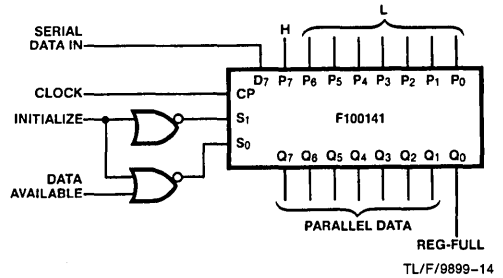


FIGURE 2-13. Serial-to-Parallel Conversion

Table 2-6 summarizes the control inputs and corresponding F100141 modes for this circuit.

TABLE 2-6. Select Inputs Truth Table

| INIT | DATA-AVAIL | S ₁ | S ₀ | Mode |
|------|------------|----------------|----------------|-------------|
| L | L | H | H | Hold |
| L | H | H | L | Shift Right |
| H | L | L | L | Preset |
| H | H | L | L | (Illegal) |

H = HIGH Voltage Level
L = LOW Voltage Level

Figure 2-15 shows a parallel-to-serial converter using the F100136 counter. *Figure 2-14* shows the associated timing diagram. Each time the external device has taken a bit of data, it makes the signal Serial-Data-Accept (SERIAL-DATA-ACPT) HIGH. The shift register shifts right which makes the next bit available and the counter counts up. The Serial-Data-Accept term must be synchronized with the clock. The counter counts to eight after the eighth data bit has been accepted and Parallel-Data-Request (PARALLEL-DATA-RQST) becomes active HIGH. When the device supplying data makes the next byte available, Parallel-Data-Ready (PARALLEL-DATA-RDY) goes HIGH. On the next clock pulse the shift register loads the new data byte and the counter clears to zero. Table 2-7 shows the operating mode as a function of the control inputs.

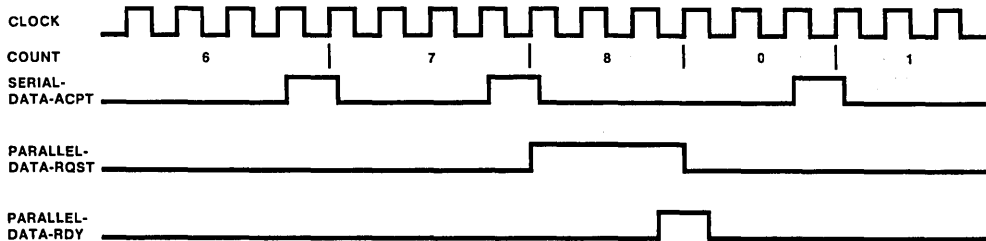


FIGURE 2-14. Timing Diagram Parallel-to-Serial Converter

TL/F/9899-15

Shift Registers (Continued)

TABLE 2-7. Parallel-to-Serial Converter Truth Table

| PARALLEL-DATA-RDY | SERIAL-DATA-ACPT | Shift Register | | | Counter | | | |
|-------------------|------------------|----------------|----------------|-------------|----------------|----------------|----------------|----------|
| | | S ₁ | S ₀ | Mode | S ₀ | S ₁ | S ₂ | Mode |
| L | L | H | H | Hold | H | H | H | Hold |
| L | H | H | L | Shift Right | L | H | H | Count Up |
| H | L | L | L | Load | H | L | H | Clear |

H = HIGH Voltage Level
L = LOW Voltage Level

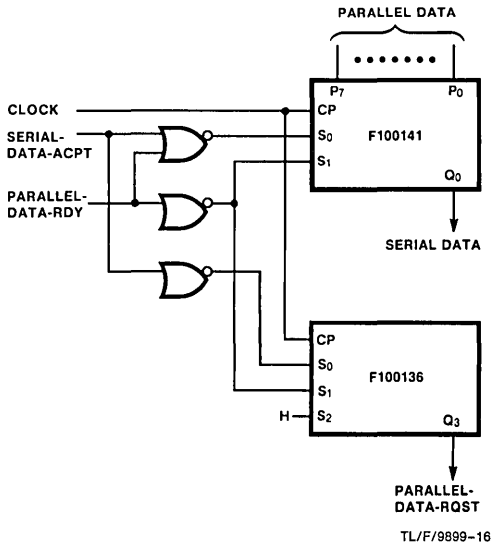


FIGURE 2-15. Parallel-to-Serial Converter

Multiplexers

Multiplexers send one of several inputs to a single output. The function can be implemented with standard gates or bus drivers and the wired-OR connection. *Figure 2-16* shows the F100123 Hex Bus Driver used as a wired-OR multiplexer. The F100123 devices could be in physically different parts of the system, since they can drive double-terminated busses.

The F100155 is a quad 2-input multiplexer with transparent latches. The device has two select terms and can accept data from either, neither, or both (OR) sources.

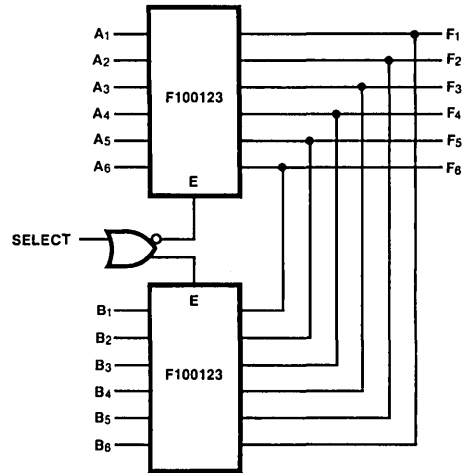


FIGURE 2-16. Wired-OR Multiplexer

The F100163 is a dual 8-input multiplexer with common selects. The F100164 is a single 16-input multiplexer.

The F100163 and F100164 do not feature complementary outputs or an enable for wired-ORing. The F100171 is a triple 4-input multiplexer with enable and complementary outputs.

Figure 2-17 shows an F100164 multiplexer and F100136 connected to convert 16-bit parallel data to single-bit serial data. A gate is added to provide complementary serial data. If the input data is stable, then the output data is stable from 6.4 ns after a clock until 2.5 ns after the next clock. This would insure valid data 50% of the time at a clock rate of 100 MHz. Terminal Count on the counter can be used as a term to indicate the last bit is being transmitted. This can be used as a clock enable to the register containing the parallel data. The propagation delay through the register is masked by the propagation delay through the counter.

Multiplexers (Continued)

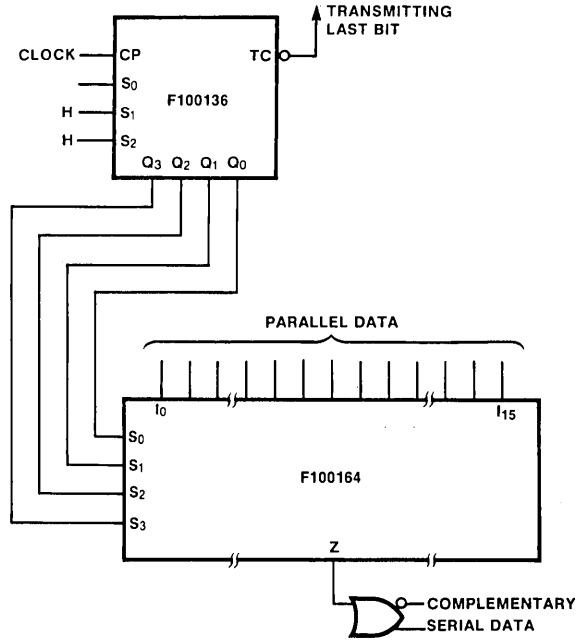


FIGURE 2-17. Parallel-to-Serial Data Transmission

TL/F/9899-18

Decoder

The F100170 is a universal demultiplexer/decoder. It can function as either a dual 1-of-4 decoder or as a single 1-of-8 decoder. The outputs can be either active HIGH or active LOW.

If the M input is LOW, then the F100170 is configured as a dual 1-of-4 decoder. Both A_{2a} and H_c must be LOW. Table 2-8 is a truth table for each half of the F100170; the two halves are completely independent. The truth table is shown for active-HIGH outputs; for active-LOW outputs, H_x is made LOW.

TABLE 2-8. Dual 1-of-4 Mode Truth Table

| Inputs | | | | Active-HIGH Outputs (H _a and H _b Inputs HIGH) | | | |
|----------------|----------------|-----------------|-----------------|--|-----------------|-----------------|-----------------|
| \bar{E}_{1a} | \bar{E}_{2a} | A _{1a} | A _{0a} | Z _{0a} | Z _{1a} | Z _{2a} | Z _{3a} |
| \bar{E}_{1b} | \bar{E}_{2b} | A _{1b} | A _{0b} | Z _{0b} | Z _{1b} | Z _{2b} | Z _{3b} |
| H | X | X | X | L | L | L | L |
| X | H | X | X | L | L | L | L |
| L | L | L | L | H | L | L | L |
| L | L | L | H | L | H | L | L |
| L | L | H | L | L | L | H | L |
| L | L | H | H | L | L | L | H |

M = A_{2a} = H_c = LOW
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

TABLE 2-9. Single 1-of-8 Mode Truth Table

| Inputs | | | | Active-HIGH Outputs (H _c Input HIGH) | | | | | | | | |
|-------------|-------------|-----------------|-----------------|--|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| \bar{E}_1 | \bar{E}_2 | A _{2a} | A _{1a} | A _{0a} | Z ₀ | Z ₁ | Z ₂ | Z ₃ | Z ₄ | Z ₅ | Z ₆ | Z ₇ |
| H | X | X | X | X | L | L | L | L | L | L | L | L |
| X | H | X | X | X | L | L | L | L | L | L | L | L |
| L | L | L | L | L | H | L | L | L | L | L | L | L |
| L | L | L | L | H | L | H | L | L | L | L | L | L |
| L | L | L | H | L | L | L | H | L | L | L | L | L |
| L | L | L | H | H | L | L | L | H | L | L | L | L |
| L | L | H | L | L | L | L | L | L | H | L | L | L |
| L | L | H | L | H | L | L | L | L | L | H | L | L |
| L | L | H | H | L | L | L | L | L | L | L | H | L |
| L | L | H | H | H | L | L | L | L | L | L | L | H |

M = HIGH;
 A_{0b} = A_{1b} = H_a = H_b = LOW
 E₁ = E_{1a} and E_{1b} Wired; E₂ = E_{2a} and E_{2b} Wired
 H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Don't Care

If the M input is HIGH, then the F100170 is configured as a single 1-of-8 decoder. A_{0b}, A_{1b}, H_a, and H_b must all be LOW. Table 2-9 is a truth table for the F100170 in single 1-of-8 mode. The truth table is shown for active-HIGH outputs; for active-LOW outputs, H_c is mode LOW.

Figure 2-18 and Table 2-10 show a universal decimal decoder and the decode table, respectively. The sense of the outputs can be easily modified. The entire decoder may be enabled with a LOW at the Function input.

Decoder (Continued)

TABLE 2-10. Output Selection

| A ₀ -A ₃ Weighted Input | Selected Output per Input Code | | | | |
|---|--------------------------------|------|-------------|------------------|------|
| | 8421 | 5421 | Excess 3 | Excess 3 Gray | 2421 |
| 0 | 0 | 0 | 3 | 2 | 0 |
| 1 | 1 | 1 | 4 | 6 | 1 |
| 2 | 2 | 2 | 5 | 7 | 2 |
| 3 | 3 | 3 | 6 | 5 | 3 |
| 4 | 4 | 4 | 7 | 4 | 4 |
| 5 | 5 | 8 | 8 | 12 | 11 |
| 6 | 6 | 9 | 9 | 13 | 12 |
| 7 | 7 | 10 | 10 | 15 | 13 |
| 8 | 8 | 11 | 11 | 14 | 14 |
| 9 | 9 | 12 | 12 | 10 | 15 |

Figure 2-19 shows a scheme to decode five lines with a 1-of-32 decoder. Inputs A₀, A₁, and A₂ are connected to the address select inputs of all four decoders in parallel. Both the true and complement of the two high order addresses are formed and then ANDed together at the decoder enable inputs.

Figure 2-20 shows a 1-of-64 decoder which uses the LOW outputs of one F100170 to enable one-of-eight F100170 devices whose address inputs are connected together. The unused enable inputs may be used to enable all 64 outputs. The 64 outputs may be either active HIGH or LOW. The propagation delay from address to any output is 4.5 ns maximum.

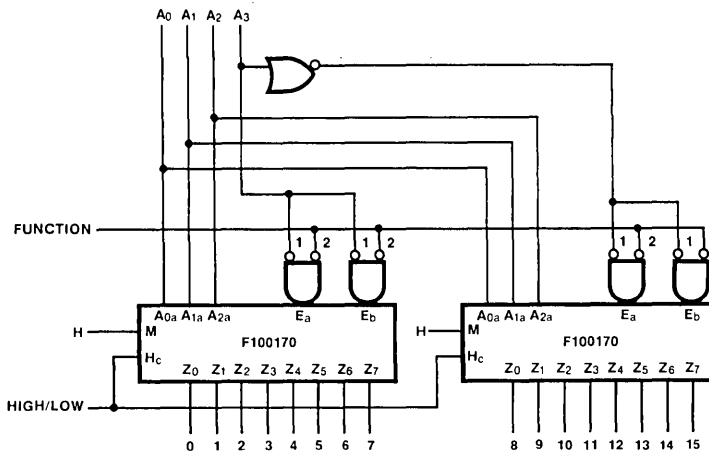


FIGURE 2-18. Universal Decimal Decoder

TL/F/9899-19

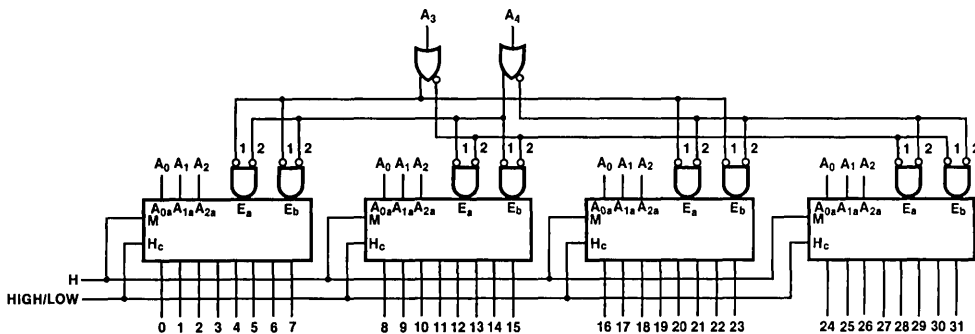


FIGURE 2-19. 1-of-32 Decoder

TL/F/9899-20

Decoder (Continued)

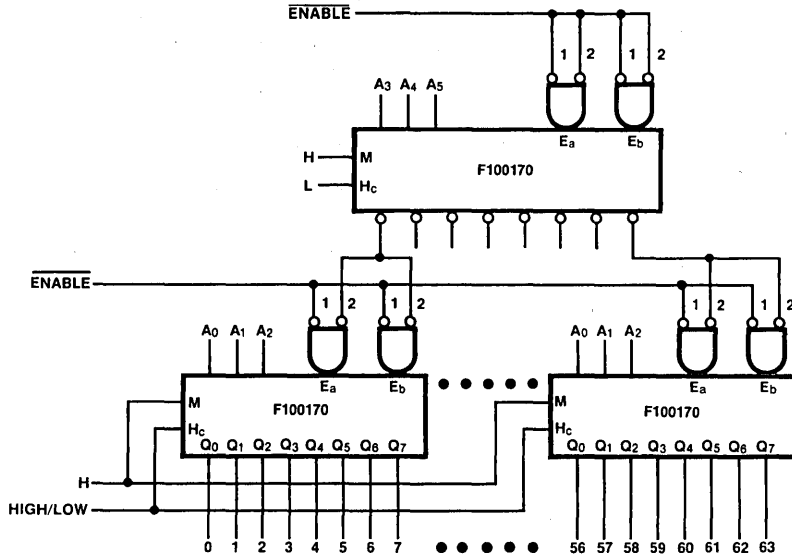


FIGURE 2-20. 1-of-64 Decoder

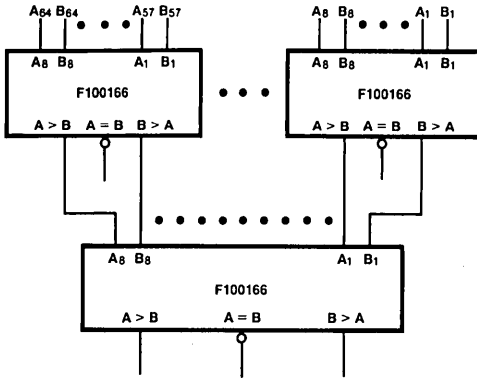
TL/F/9899-21

Comparators

The F100166 is a 9-bit magnitude comparator which compares the arithmetic value of two 9-bit words and indicates either $A > B$, $A < B$, or $A = B$.

The unequal outputs are active HIGH so that expansion is simple, *Figure 2-21* indicates how two 64-bit words may be compared in 5.4 ns typical. If desired, the $A = B$ outputs of the first rank may be OR-wired to obtain an active-LOW $A = B$ in 2.7 ns typical.

The F100107 Quint Exclusive-OR/NOR may be used as a 5-bit identity comparator with a propagation delay of 2.0 ns typical. The F100160 Parity Checker/Generator may also be used as an identity comparator.



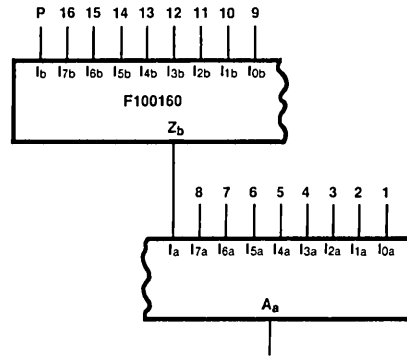
TL/F/9899-24

FIGURE 2-21. 64-Bit Magnitude Comparator

Parity Generator/Checker

The F100160 is a dual 9-bit parity checker/generator. The output (of each section) is HIGH when an even number of inputs are HIGH. Thus, to generate odd parity on eight bits, the ninth input would be held HIGH. One of the nine inputs on each half has a shorter propagation (I_a , I_b) delay and is thus preferred for expansion.

Figure 2-22 shows how to build a 16-bit parity checker using a single F100160. The typical propagation delay from the longest input is 4.05 ns. This circuit can be turned into a parity generator by replacing "P" at input I_b with a LOW or HIGH for even or odd parity, respectively.



TL/F/9899-25

FIGURE 2-22. 16-Bit Parity Checker/Generator

Arithmetic Logic Unit

The F100181 is a 4-bit binary/BCD ALU with a typical propagation delay of 4.5 ns. Output latches are provided to reduce system package count. When the latches are not required, they may be made transparent. Table 2-11 summarizes the functions available in the F100181. Table 2-12 is a summary of add times as a function of word width using the F100181 and, optionally, the F100179 Lookahead Carry Generator. These are calculated using maximum times for flatpak at 25°C from the data sheets and assume zero interconnection times. Further, it is assumed that the S (function select) inputs are available very early; their delay paths are ignored. The F100181 specification sheet indicates how the parts are interconnected.

TABLE 2-11. F100181 Functions

| S ₃ | S ₂ | S ₁ | S ₀ | Function | Note |
|----------------|----------------|----------------|----------------|------------------|---|
| L | L | L | L | A Plus B BCD | |
| L | L | L | H | A Minus B BCD | |
| L | L | H | L | B Minus A BCD | |
| L | L | H | H | O Minus A BCD | |
| L | H | L | L | A Plus B Binary | |
| L | H | L | H | A Minus B Binary | |
| L | H | H | L | B Minus A Binary | |
| L | H | H | H | O Minus B Binary | |
| H | L | L | L | Identity | $F = A \cdot B + \bar{A} \cdot \bar{B}$ |
| H | L | L | H | XOR | $F = A \cdot \bar{B} + \bar{A} \cdot B$ |
| H | L | H | L | OR | $F = A + B$ |
| H | L | H | H | A | $F = A$ |
| H | H | L | L | Inverse | $F = \bar{B}$ |
| H | H | L | H | B | $F = B$ |
| H | H | H | L | AND | $F = A \cdot B$ |
| H | H | H | H | Zero | $F = \text{LOW}$ |

H = HIGH Voltage Level
L = LOW Voltage Level

Arithmetic Logic Unit (Continued)

TABLE 2-12. Summary of Add Times Using F100181

| Bits | Ripple Carry | 1 F100179 Lookahead Carry | 2 F100179 Lookahead Carries |
|------|--------------|---------------------------|-----------------------------|
| 8 | 11.3 | n/a | n/a |
| 16 | 16.9 | 11.9 | n/a |
| 32 | 28.1 | 14.7 | 14.6 |
| 64 | 50.5 | n/a | 17.4 |

Ripple Carry = $(A \text{ or } B \text{ to } C_n + 4) + (C_n \text{ to } F) + ((D - 2)C_n \text{ to } C_{n+4})$
 where D = number of 100181 devices

16-Bit, 1 Lookahead = $(A \text{ or } B \text{ to } P \text{ or } G) + (C_n \text{ to } F) + (t_p \text{ of } 100179)$

32-Bit, 1 Lookahead = $(A \text{ or } B \text{ to } P \text{ or } G) + (C_n \text{ to } F) + (t_p \text{ of } 100179) + (C_n \text{ to } C_{n+4} \text{ of last stage})$

32-Bit, 2 Lookaheads = $(A \text{ or } B \text{ to } P \text{ or } G) + (C_n \text{ to } F) + (2t_p \text{ of } 100179)$

64-Bit, 2 Lookaheads = $(A \text{ or } B \text{ to } P \text{ or } G) + (C_n \text{ to } F) + (2t_p \text{ of } 100179) + (C_n \text{ to } C_{n+4} \text{ of last stage})$

Multipliers

The F100182 Wallace Tree Adder and F100183 Recode Multiplier can be combined to build extremely fast parallel multipliers. The F100183 data sheet has detailed applications information; Table 2-13 is a summary of delay times and package counts for various operand sizes. The times are typical and do not include interconnection delays.

TABLE 2-13. Multiplier Summary

| Operand Size | Delay (ns) | Device Count |
|--------------|------------|--------------|
| 16 × 16 | 16 | 62 |
| 24 × 24 | 22 | 115 |
| 32 × 32 | 24 | 186 |
| 64 × 64 | 26 | 634 |

TTL/F100K Interfacing—Translators

The problem of mixing F100K ECL logic levels with TTL logic levels can be easily overcome with the use of level translators. Level translators are designed to convert the input level of one logic family to a level which is consistent with that of another logic family. This enables designers to take advantage of the high speeds offered by F100K ECL in critical system paths and to use other logic families in areas where speed is not as essential. National's wide range of level translators offer designers a solution for most level translation applications.

The F100124 and F100324 are hex translators designed for converting TTL logic levels to F100K ECL logic levels. Both products are functionally interchangeable, as are all the 300

Series redesigns. On the F100124 or F100324, a common Enable input (E), when LOW, holds all inverting ECL outputs HIGH and all true ECL outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver.

The F100125 and F100325 are hex F100K ECL-to-TTL translators. F100K ECL-to-TTL level translation is probably the most common application for translators today. Logic designers can take advantage of the high speeds offered by ECL and the high densities offered by TTL memories (DRAMs). The F100125 and F100325 have outputs which are compatible with standard or Schottky TTL. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single ended operation, or for use in Schmitt trigger applications.

For applications which require wider bit functions the F100393 or the F100395 may be more appropriate. The F100393 is a 9-bit F100K ECL-to-TTL level translator with latched outputs and the F100395 is a 9-bit F100K ECL-to-TTL translator with registers. Both products are designed with FAST TTL outputs capable of driving loads of up to 64 mA. A LOW on the latch enable (LE) input of the F100393, latches the data at the input state. A HIGH on the LE makes the latches transparent. A HIGH on either the ECL or TTL output enable (\overline{OE} ECL or \overline{OE} TTL) inputs, holds the outputs in a high impedance state. For the F100395, a HIGH on the output enable (\overline{OE}) holds the TTL outputs in a high impedance state. A LOW on the clock enable (\overline{EN}) transfers the data on the inputs to the outputs on a LOW-to-HIGH transition. A high on the \overline{EN} input will not change the state of the outputs.

Some applications may require bi-directional level translation on one chip. That is, the ability to direct the translation in either the F100K ECL-to-TTL direction, or in the TTL-to-F100K ECL direction. The F100128 and F100328 accomplish this task. The F100128 and the F100328 are Octal F100K ECL/TTL Bi-Directional Translators with Latched outputs. The direction of the translation for these devices is determined by the DIR input, a LOW is for ECL-to-TTL translation and a HIGH is for TTL-to-ECL translation. A LOW on the output enable input (OE), holds the ECL outputs in a cut-off state and the TTL outputs in a high impedance state. The latched outputs of these devices are controlled by the latch enable input (LE). A HIGH on the LE, latches the data at both inputs even though only one output is enabled at the time (T_n or E_n as determined by the DIR input). A LOW on the LE input makes the latches transparent.

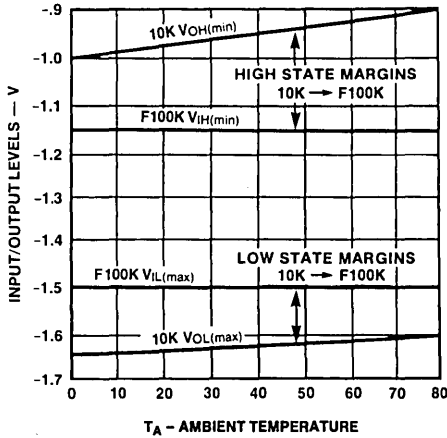
The F100329 is an Octal F100K ECL/TTL Bi-directional Translator similar to the F100328, but employs the use of registers instead of latches. The direction of the translation is also controlled by the DIR input. A LOW on the DIR input will translate in the ECL-to-TTL direction and a HIGH will translate in the TTL-to-ECL direction. A LOW on the output enable input (OE) of the F100329 holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. The outputs change synchronously with the rising edge of the clock input (CP), even though only one output is enabled at a time (E_n or T_n , as determined by the DIR input).

10K/F100K Interfacing

The problem caused by mixing 10K ECL and F100K ECL is illustrated in *Figures 2-25 and 2-26*. 10K output levels and input thresholds vary with temperature whereas F100K levels and thresholds remain essentially constant. This means that the noise margins vary with temperature, even if the temperatures of the driving and receiving circuits track. Perhaps the worst case is shown in *Figure 2-26*, which illustrates F100K driving 10K.

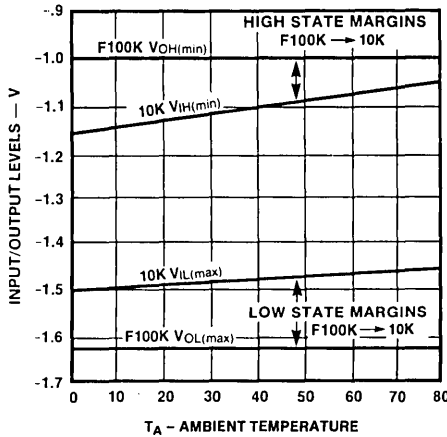
At +75°C, the high margins are seen to be less than 100 mV. Clearly this would not represent acceptable DC margins in any real system.

If the use of 10K ECL in an F100K system is unavoidable, it is recommended that all interfacing be done differentially. This is illustrated in *Figure 2-27* which is applicable for either direction.



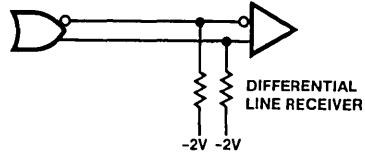
TL/F/9899-26

FIGURE 2-25. 10K ECL Driving 100K ECL



TL/F/9899-27

FIGURE 2-26. 100K ECL Driving 10K ECL



TL/F/9899-28

FIGURE 2-27. Interfacing 10K and F100K



Chapter 3 Transmission Line Concepts

Introduction

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

Simplifying Assumptions

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

Characteristic Impedance

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_0 . Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal charge or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (3-1)$$

where L_0 = inductance per unit length, C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in Henries, C_0 in Farads.

Propagation Velocity

Propagation velocity v and its reciprocal, delay per unit length δ , can also be expressed in terms of L_0 and C_0 . A consistent set of units is nanoseconds, microhenries and picofarads, with a common unit of length.

$$v = \frac{1}{\sqrt{L_0 C_0}} \quad \delta = \sqrt{L_0 C_0} \quad (3-2)$$

Equations 3-1 and 3-2 provide a convenient means of determining the L_0 and C_0 , of a line when delay, length and impedance are known. For a length l and delay T , δ is the ratio T/l . To determine L_0 and C_0 , combine Equations 3-1 and 3-2.

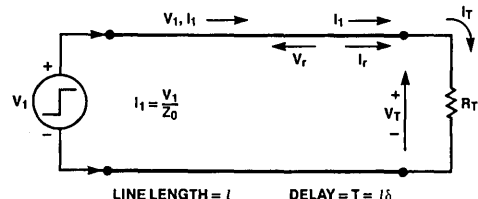
$$L_0 = \delta Z_0 \quad (3-3)$$

$$C_0 = \frac{\delta}{Z_0} \quad (3-4)$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.¹⁻³

Termination and Reflection

A transmission line with a terminating resistor is shown in Figure 3-1. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0 .



TL/F/9900-1

FIGURE 3-1. Assigned Polarities and Directions for Determining Reflections

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T . From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator. From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T .

When R_T is not equal to Z_0 , the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T . Therefore, at the instant the initial wave arrives at R_T , another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This *reflected* wave, indicated by V_r and I_r in Figure 3-1, starts to return toward the generator. Applying

Termination and Reflection (Continued)

Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following.

$$I_1 + I_r = I_T = \text{current into } R_T \quad (3-5)$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

$$\text{thus } I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T} \quad (3-6)$$

$$\text{also } I_1 = \frac{V_1}{Z_0} \text{ and } I_r = -\frac{V_r}{Z_0}$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1 , Z_0 and R_T .

$$\frac{V_1 - V_r}{Z_0} - \frac{V_r}{Z_0} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1 \left(\frac{1}{Z_0} - \frac{1}{R_T} \right) = V_r \left(\frac{1}{R_T} + \frac{1}{Z_0} \right) \quad (3-7)$$

$$V_r = V_1 \left(\frac{R_T - Z_0}{R_T + Z_0} \right) = \rho_L V_1$$

The term in parenthesis is called the coefficient of reflection ρ . With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between -1 and $+1$ respectively. The subscript L indicates that ρ refers to the coefficient at the load end of the line.

Equation 3-7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r \quad (3-8)$$

then $V_T = V_1 (1 + \rho_L)$.

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L . Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_0}{R_T + Z_0} = 2 \left(\frac{R_T}{R_T + Z_0} \right)$$

Substituting in Equation 3-8 gives

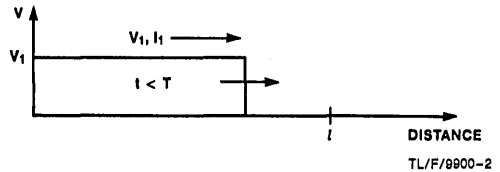
$$V_T = 2 \left(\frac{R_T}{R_T + Z_0} \right) V_1 \quad (3-9)$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_0 driving a load R_T , except that the amplitude of V_T is doubled.

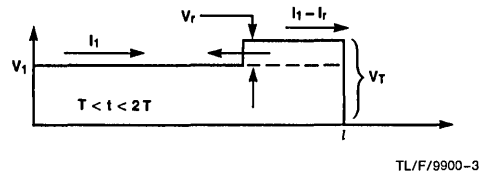
The arrow indicating the direction of V_r in Figure 3-1 correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1 . This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in Equation 3-7 that if V_r is positive it is because R_T is greater than Z_0 . In turn, this means that the initial current I_r is larger than the final quiescent current, dictated by V_1 and R_T . Hence, I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1 .

It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T . With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0 , i.e., R_T is already accounted for in the magnitude of V_r . The relationships between incident and reflected signals are represented in Figure 3-2 for both cases of mismatch between R_T and Z_0 .

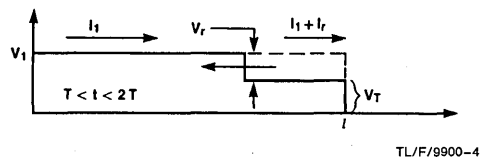
The incident wave is shown in Figure 3-2a, before it has reached the end of the line. In Figure 3-2b, a positive V_r is returning to the generator. To the left of V_r the current is still I_1 , flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r . In Figure 3-2c, the reflection coefficient is negative, producing a negative V_r . This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.



a. Incident Wave



b. Reflected Wave for $R_T > Z_0$



c. Reflected Wave for $R_T < Z_0$
FIGURE 3-2. Reflections for $R_T \neq Z_0$

Source Impedance, Multiple Reflections

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r . The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S .

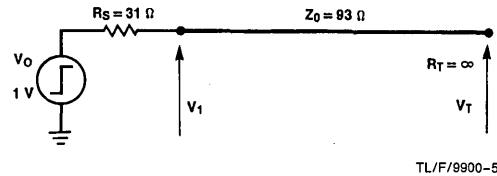
$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \quad (3-10)$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

$$V_T = V_1 + V_r \text{ and } I_T = I_1 - I_r \quad (3-11)$$

If neither source impedance nor terminating impedance matches Z_0 , multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 3-3*. The source is a step function of 1V amplitude occurring at time t_0 . The initial value of V_1 starting down the line is 0.75V due to the voltage divider action of Z_0 and R_S . The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.

The amplitude and persistence of the ringing shown in *Figure 3-3* become greater with increasing mismatch between the line impedance and source and load impedances. Re-



$$\rho_S = \frac{31 - 93}{31 + 93} = -0.5$$

$$\rho_L = \frac{\infty - 93}{\infty + 93} = +1$$

Initially: $V_1 = \frac{Z_0}{Z_0 + R_S} \cdot V_0 = \frac{93}{124} \cdot 1 = 0.75V$

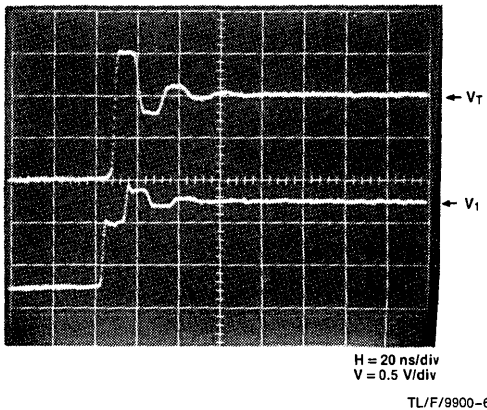


FIGURE 3-3. Multiple Reflections Due to Mismatch at Load and Source

ducing R_S (*Figure 3-3*) to 13Ω increases ρ_S to $-0.75V$, and the effects are illustrated in *Figure 3-4*. The initial value of V_T is 1.8V with a reflection of 0.9V from the open end. When this reflection reaches the source, a reflection of $0.9V \times -0.75V$ starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative going. In turn, a negative-going reflection of $0.9V \times -0.75V$ starts back toward the source. This negative increment is again multiplied by -0.75 at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is

$$V_T - V'_T = (1 + \rho_L) V_1 - (1 + \rho_L) V_1 \rho_L^2 \rho_S^2 \quad (3-12)$$

$$= (1 + \rho_L) V_1 (1 - \rho_L^2 \rho_S^2)$$

The factor $(1 - \rho_L^2 \rho_S^2)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.

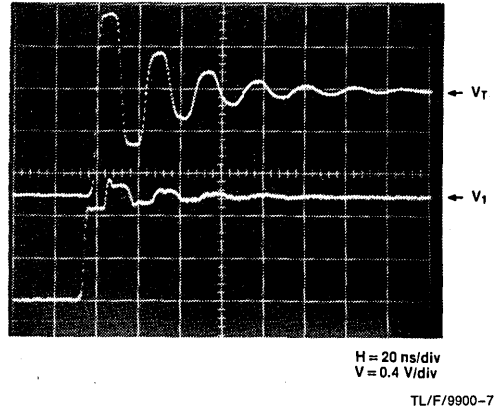


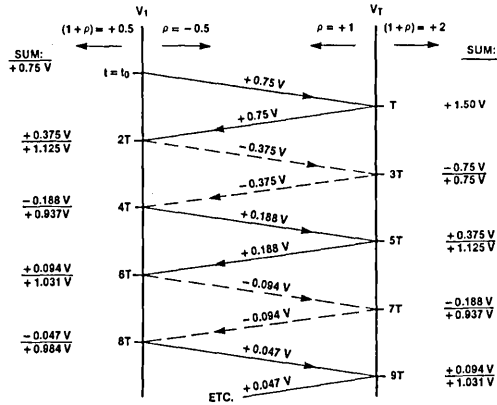
FIGURE 3-4. Extended Ringing when R_S of *Figure 3-3* is Reduced to 13Ω

Lattice Diagram

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram.⁴ A lattice diagram for the line conditions of *Figure 3-3* is shown in *Figure 3-5*.

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of $2T$, starting at t_0 for V_1 and T for V_T . The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and $(1 + \rho)$ at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 1V, as they must with a 1V source driving an open-ended line.

Lattice Diagram (Continued)



TL/F/9900-8

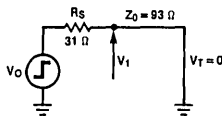
FIGURE 3-5. Lattice Diagram for the Circuit of Figure 3-3

Shorted Line

The open-ended line in Figure 3-3 has a reflection coefficient of +1 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of -1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in Figure 3-6a with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. Figure 3-6b shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about +0.75V, which is inverted at the shorted end and returned toward the source as -0.75V. Arriving back at the source end of the line, this voltage is multiplied by (1 + ρ_S), causing a -0.37V net change in V_1 . Concurrently, a reflected voltage of +0.37V (-0.75V times ρ_S of -0.5) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in Figure 3-6c. The amplitude decreases by 50% with each successive occurrence as it did in Figure 3-6b.

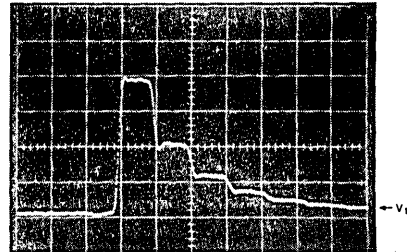


TL/F/9900-9

$$\rho_S = -0.5$$

$$\rho_L = \frac{0 - 93}{0 + 93} = -1$$

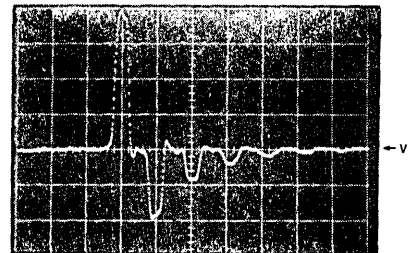
a. Reflection Coefficients for Shorted Line



H = 10 ns/div
V = 0.2 V/div

TL/F/9900-10

b. Input Pulse Duration > Line Delay



H = 10 ns/div
V = 0.2 V/div

TL/F/9900-11

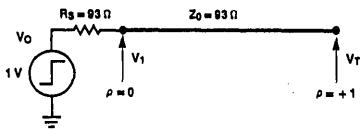
c. Input Pulse Duration < Line Delay

FIGURE 3-6. Reflections of Long and Short Pulses on a Shorted Line

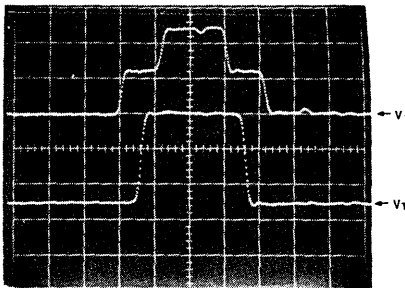
Series Termination

Driving an open-ended line through a source impedance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 3-7* shows a 93Ω line driven from a 1V generator through a source impedance of 93Ω . The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude ($1 + \rho_L = 2$). The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.

An ECL output driving a series terminated line requires a pull-down resistor to V_{EE} , as indicated in *Figure 3-8*. The resistor R_0 shown in *Figure 3-8* symbolizes the output resistance of the ECL gate. The relationships between R_0 , R_S , R_E and Z_0 are discussed in Chapter 4.



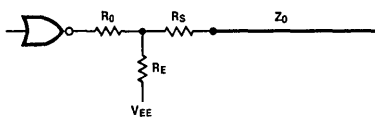
TL/F/9900-12



H = 10 ns/div
V = 0.4 V/div

TL/F/9900-13

FIGURE 3-7. Series Terminated Line and Waveforms

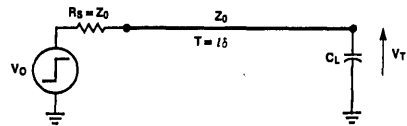


TL/F/9900-14

FIGURE 3-8. ECL Element Driving a Series Terminated Line

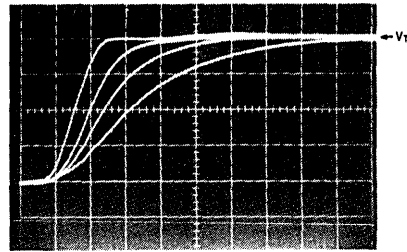
Extra Delay with Termination Capacitance

Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 3-9* shows how the output waveform changes with increasing load capacitance. *Figure 3-9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T . A capacitive load at the end of the line causes an extra delay ΔT due to the increase in rise time of the output signal. The midpoint of the output is used as a criterion because the propagation delay of an ECL circuit is measured between the 50% points of the input and output signals.



TL/F/9900-15

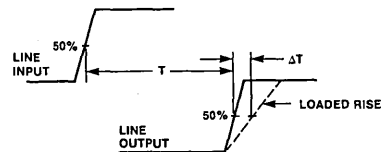
a. Series Terminated Line with Load Capacitance



H = 1 ns/div
V = 0.2 V/div

TL/F/9900-16

b. Output Rise Time Increase with Increasing Load Capacitance

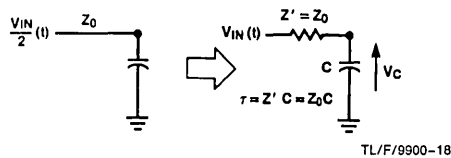


TL/F/9900-17

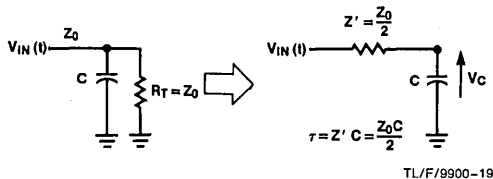
c. Extra Delay ΔT Due to Rise Time Increase

FIGURE 3-9. Extra Delay with Termination Capacitance

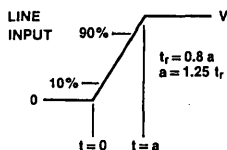
Extra Delay with Termination Capacitance (Continued)



a. Thevenin Equivalent for Series Terminated Case



b. Thevenin Equivalent for Parallel Terminated Case



TL/F/9900-20

$$v_{in}(t) = \frac{V}{a} [tu(t) - (t-a)u(t-a)]$$

$$u(t) = \begin{cases} 0 & \text{for } t < 0 \\ 1 & \text{for } t > 0 \end{cases}$$

$$u(t-a) = \begin{cases} 0 & \text{for } t < a \\ 1 & \text{for } t > a \end{cases}$$

$$V_{IN}(S) = \frac{V}{as^2} (1 - e^{-as})$$

$$V_C(S) = \frac{V}{ar} \cdot \frac{1}{s^2(s + 1/\tau)} (1 - e^{-as})$$

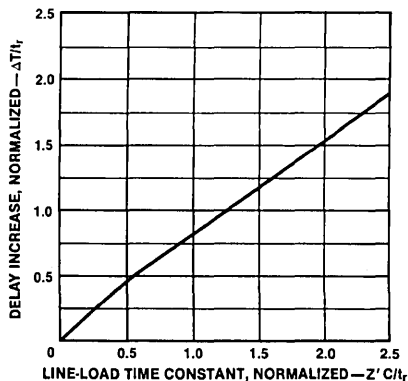
$$v_c(t) = \frac{V}{a} [t - \tau(1 - e^{-t/\tau})] u(t) - \frac{V}{a} [(t-a) - \tau(1 - e^{-(t-a)/\tau})] u(t-a)$$

c. Equations for Input and Output Voltages

FIGURE 3-10. Determining the Effect of End-of-Line Capacitance

The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 3-10*. One general solution serves both series and parallel termination cases by using an impedance Z' and a time constant τ , defined in *Figure 3-10a* and *3-10b*. Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At large ratios of τ/a (where a = ramp time), measured delays exceed calculated values by approximately 7%. *Figure 3-11*, based on measured values, shows the increase in delay to the 50% point as a function of the $Z'C$ time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100Ω series terminated line with 30 pF load capacitance at the end of the line and a no-load rise time of 3 ns for the input signal. From *Figure 3-10a*, Z' is equal to 100Ω; the ratio $Z'C/t_r$ is 1. From the graph, the ratio $\Delta T/t_r$ is 0.8. Thus the increase in the delay to the 50% point of the output waveform is 0.8 t_r , or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

Had the 100Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z' would be 50Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50Ω and parallel terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.



TL/F/9900-21

FIGURE 3-11. Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to T_r

Distributed Loading Effects on Line Characteristics

When capacitive loads such as ECL inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time.⁵ *Figure 3-12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 3-12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns apart, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 3-12b*, the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at $\approx -10\%$) for half its duration. This is about the same reflection that would occur if the 93 Ω line had a middle section with an impedance reduced to 75 Ω .

With a number of capacitors distributed all along the line of *Figure 3-12a*, the combined reflections modify the observed input waveform as shown in the top trace of *Figure 3-12c*. The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T >$

Z_0). This analogy is strengthened by observing the effect of reducing R_T from 93 Ω to 75 Ω , which leads to the middle waveform of *Figure 3-12c*. Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 3-12c* the source resistance R_S is reduced from 93 Ω to 75 Ω , restoring both the initial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.

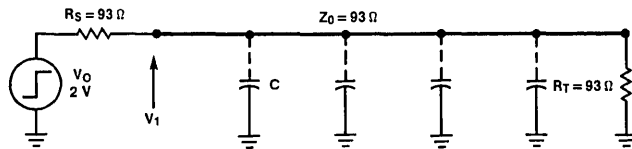
The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_0 along that portion of the line where the loads are connected.⁶ Denoting this length of line as l , the distributed value C_D of the load capacitance is as follows.

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_0 in *Equation 3-1* to determine the reduced line impedance Z'_0 .

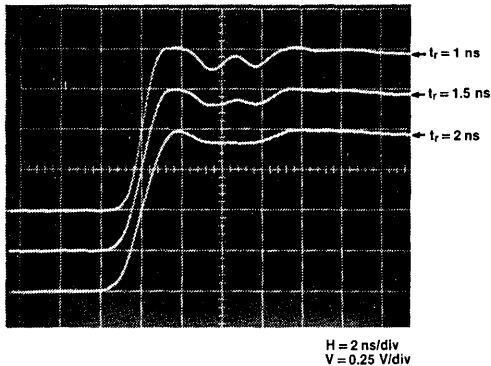
$$Z'_0 = \sqrt{\frac{L_0}{C_0 + C_D}} = \sqrt{\frac{L_0}{C_0 \left(1 + \frac{C_D}{C_0}\right)}} \quad (3-13)$$

$$Z'_0 + \frac{\sqrt{\frac{L_0}{C_0}}}{\sqrt{1 + \frac{C_D}{C_0}}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$



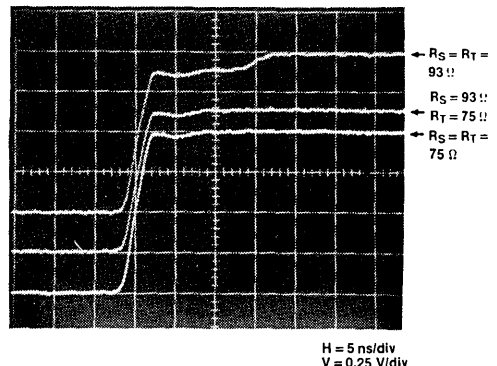
a. Arrangement for Observing Capacitive Loading Effects

TL/F/9900-22



b. Capacitive Reflections Merging as Rise Time Increases

TL/F/9900-23



c. Matching the Altered Impedance of a Capacitively Loaded Line

TL/F/9900-24

FIGURE 3-12. Capacitive Reflections and Effects on Line Characteristics

Distributed Loading Effects on Line Characteristics (Continued)

In the example of *Figure 3-12c*, the total load capacitance is 33 pF while the total intrinsic line capacitance $/C_0$ is 60 pF. (Note that the ratio C_D/C_0 is the same as C_L/C_0 .) The calculated value of the reduced impedance is thus

$$Z'_0 = \frac{93}{\sqrt{1 + \frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\Omega \quad (3-14)$$

This correlates with the results observed in *Figure 3-12c* when R_T and R_S are reduced to 75Ω.

The distributed load capacitance also increases the line delay, which can be calculated from *Equation 3-2*.

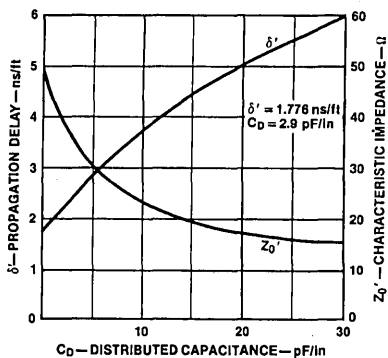
$$\begin{aligned} \delta' &= \sqrt{L_0(C_0 + C_D)} = \sqrt{L_0 C_0} \sqrt{1 + \frac{C_D}{C_0}} \\ &= \delta \sqrt{1 + \frac{C_D}{C_0}} \end{aligned} \quad (3-15)$$

The line used in the example of *Figure 3-12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with *Equation 3-15*.

$$l\delta' = l\delta \sqrt{1.55} = 6\sqrt{1.55} = 7.5 \text{ ns} \quad (3-16)$$

Equation 3-15 can be used to predict the delay for a given line and load. The ratio C_D/C_0 (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_0 .

A plot of Z' and δ' for a 50Ω line as a function of C_D is shown in *Figure 3-13*. This figure illustrates that relatively modest amounts of load capacitance will add appreciably to the propagation delay of a line. In addition, the characteristic impedance is reduced significantly.



TL/F/9900-25

FIGURE 3-13. Capacitive Loading Effects on Line Delay and Impedance

Worst case reflections from a capacitively loaded section of transmission line can be accurately predicted by using the modified impedance of *Equation 3-9*.⁶ When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows.

$$\rho = \frac{Z'_0 - Z_0}{Z'_0 + Z_0} \quad (3-17)$$

Mismatched Lines

Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted-pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted-pair, line impedance changes run about 5% to 10% and reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 3-14* and analyzed in the lattice diagram of *Figure 3-15*. Line 1 is driven in the series terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ are determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 3-14*, the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows.

$$\rho_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \frac{93 - 50}{143} = +0.3 \quad (3-18)$$

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows.

$$V_{1r} = \rho_{12} V_1 = +0.3V_1 \quad (3-19a)$$

$$V_2 = (1 + \rho_{12}) V_1 = +1.3 V_1 \quad (3-19b)$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

$$\rho_{23} = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39 - 93}{132} = -0.41 \quad (3-20)$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows.

$$\begin{aligned} V_{2r} &= \rho_{23} V_2 = -0.41 V_2 \\ &= (-0.41)(1.3) V_1 \\ &= -0.53 V_1 \end{aligned} \quad (3-21a)$$

$$\begin{aligned} V_3 &= (1 + \rho_{23}) V_2 = 0.59 V_2 \\ &= (0.59)(1.3) V_1 \\ &= 0.77 V_1 \end{aligned} \quad (3-21b)$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is +1. This effectively cancels the voltage divider action between R_S and Z_1 .

$$\begin{aligned} V_4 &= (1 + \rho_L) V_3 = (1 + \rho_L)(1 + \rho_{23}) V_2 \\ &= (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12}) V_1 \\ &= (1 + \rho_L)(1 + \rho_{23})(1 + \rho_{12}) \frac{V_0}{2} \end{aligned} \quad (3-22)$$

$$V_4 = (1 + \rho_{23})(1 + \rho_{12}) V_0$$

Thus, *Equation 3-22* is the general expression for the initial step of output voltage for three lines when the input is series terminated and the output is open-ended.

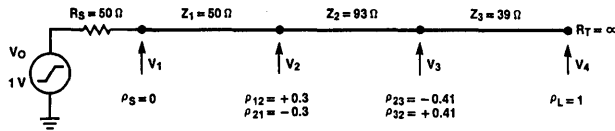
Mismatched Lines (Continued)

Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in Figure 3-15 have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_O . Lines 2 and 3 have the same delay time; therefore, the two aforementioned increments arrive at the output simultaneously at time $5T$ on the lattice diagram (Figure 3-15).

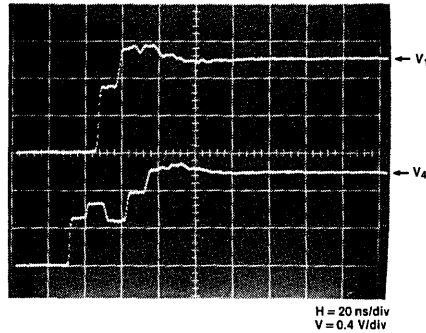
In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. Figure 3-16 shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest im-

pedance line in the middle, at least three output voltage increments with the same polarity as V_O occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_O . The third increment of output voltage has the opposite polarity, for the time delay ratios of Figure 3-16.

When transmitting logic signals, it is important that the initial step of line output voltage pass through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series terminated sequence of three mismatched lines, the middle line should have the highest impedance.

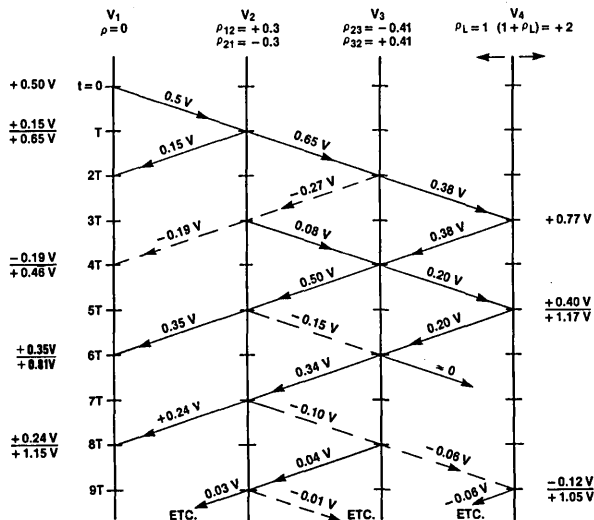


TL/F/9900-26



TL/F/9900-27

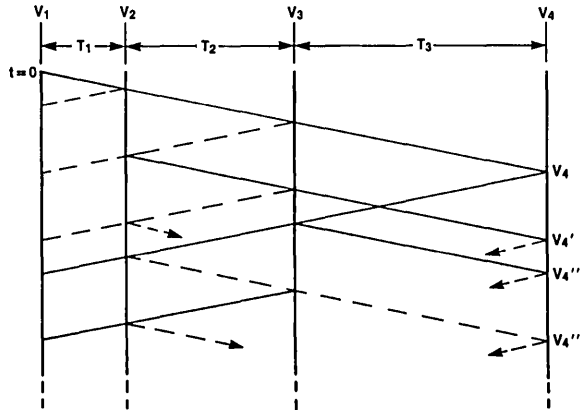
FIGURE 3-14. Reflections from Mismatched Lines



TL/F/9900-28

FIGURE 3-15. Lattice Diagram for the Circuit of Figure 3-14

Mismatched Lines (Continued)



TL/F/9900-29

FIGURE 3-16. Lattice Diagram for Three Lines with Delay Ratios 1:2:3

Rise Time versus Line Delay

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 3-17*, which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 3-17b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1V. At time T later, V_T rises to 0.5V, i.e., $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time $2T$, causing a net change of $-0.4V$, i.e., $(1 + \rho_S)(-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time $3T$. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time $4T$.

In *Figure 3-17c*, the input rise time (0% to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to $2T$.

The input rise time is increased to $4T$ in *Figure 3-17d*, with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 3-17e*, which shows V_1 (t_r still set for $4T$) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time $2T$ earlier. The value of V_1 in *Figure 3-17d* can be calculated by starting with the 1V input ramp.

$$V_1 = \frac{1}{t_r} \cdot t \quad \text{for } 0 \leq t \leq 4T \quad (3-23)$$

$$= 1V \quad \text{for } t \geq 4T$$

The reflection from the end of the line is

$$V_r = \frac{\rho_L(t - 2T)}{t_r} \quad (3-24)$$

the portion of the reflection that appears at the input is

$$V'_r = \frac{(1 + \rho_S)\rho_L(t - 2T)}{t_r} \quad (3-25)$$

the net value of the input voltage is the sum.

$$V'_1 = \frac{t}{t_r} + \frac{(1 + \rho_S)\rho_L(t - 2T)}{t_r} \quad (3-26)$$

The peak value of the input voltage in *Figure 3-17d* is determined by substituting values and letting t equal $4T$.

$$V'_1 = 1 + \frac{(0.8)(-0.5)(4T - 2T)}{t_r} \quad (3-27)$$

$$= 1 - 0.4(0.5) = 0.8V$$

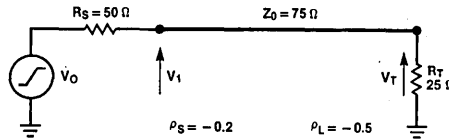
After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time $6T$. For the general case of repeated reflections, the net voltage $V_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$.

Rise Time versus Line Delay (Continued)

$$\begin{aligned}
 V'_{1(t)} &= V_1(t) && \text{for } 0 < t < 2T \\
 V'_{1(t)} &= V_1(t) + (1 + \rho_S) \rho_L V_1(t-2T) && \text{for } 2T < t < 4T \\
 V'_{1(t)} &= V_1(t) + (1 + \rho_S) \rho_L V_1(t-2T) && + (1 + \rho_S) \rho_S \rho_L^2 V_1(t-4T) && (3-28) \\
 &&& \text{for } 4T < t < 6T \\
 V'_{1(t)} &= V_1(t) + (1 + \rho_S) \rho_L V_1(t-2T) && + (1 + \rho_S) \rho_S \rho_L^2 V_1(t-4T) && + (1 + \rho_S) \rho_S^2 \rho_L^3 V_1(t-6T) \\
 &&& \text{for } 6T < t < 8T, \text{ etc.}
 \end{aligned}$$

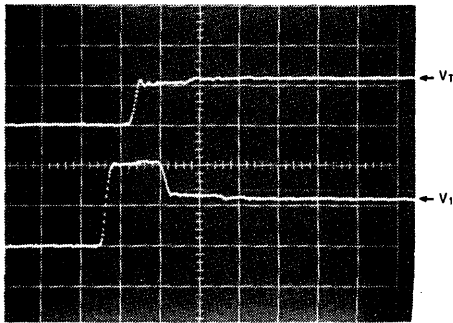
The voltage at the output end of the line is expressed in a similar manner.

$$\begin{aligned}
 V_T(t) &= 0 && \text{for } 0 < t < T \\
 V_T(t) &= (1 + \rho_L) V_1(t-T) && \text{for } T < t < 3T \\
 V_T(t) &= (1 + \rho_L) V_1(t-T) && + (1 + \rho_L) \rho_S \rho_L V_1(t-3T) && (3-29) \\
 &&& \text{for } 3T < t < 5T \\
 V_T(t) &= (1 + \rho_L) V_1(t-T) && + (1 + \rho_L) \rho_S \rho_L V_1(t-3T) && + (1 + \rho_L) \rho_S^2 \rho_L^2 V_1(t-5T) \\
 &&& \text{for } 5T < t < 7T, \text{ etc.}
 \end{aligned}$$



TL/F/9900-30

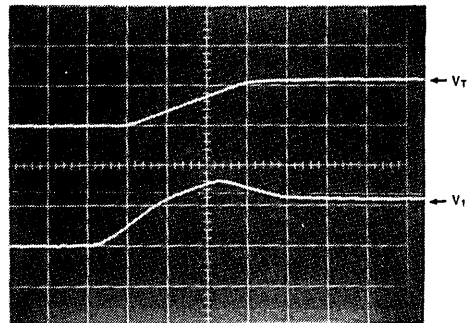
a. Test Arrangement for Rise Time Analysis



H = 10 ns/div
V = 0.5 V/div

TL/F/9900-31

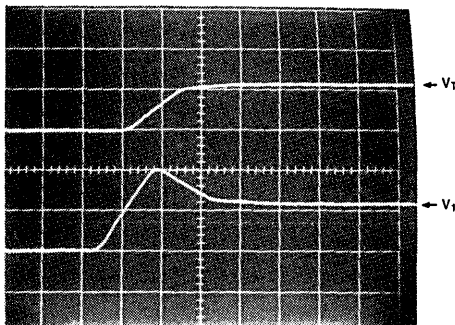
b. Line Voltages for $t_r \ll T$



H = 10 ns/div
V = 0.5 V/div

TL/F/9900-33

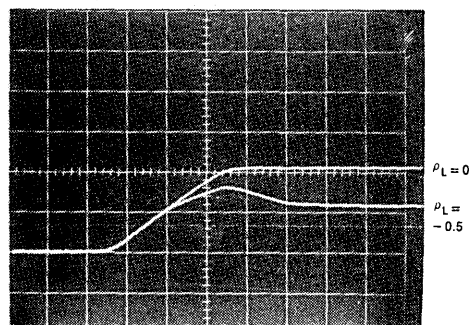
d. Line Voltages for $t_r = T$



H = 10 ns/div
V = 0.5 V/div

TL/F/9900-32

c. Line Voltages for $t_r = 2T$



H = 10 ns/div
V = 0.5 V/div

TL/F/9900-34

e. Input Voltage with and without Reflection

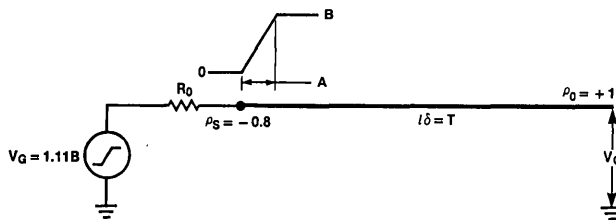
FIGURE 3-17. Line Voltages for Various Ratios of Rise Time to Line Delay

Ringing

Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

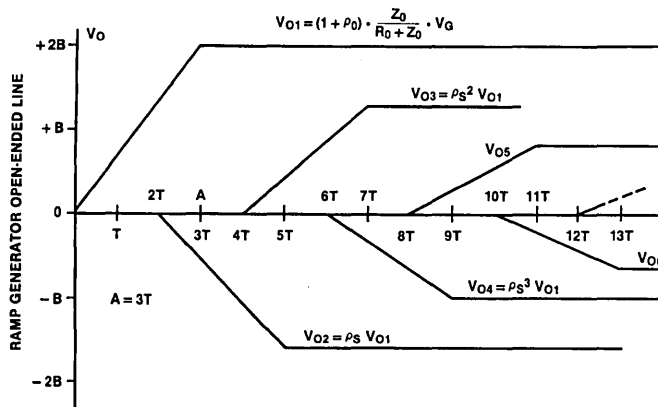
When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 3-18*. The incident wave is a ramp of amplitude B and rise duration A . The reflection coefficient at the open-ended line output is $+1$ and the source reflection coefficient is assumed to be -0.8 , i.e., $R_0 = Z_0/9$.

Figure 3-18b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T . The time scale reference is the line output and the first increment of output voltage V_0 rises to $2B$ in the time interval A . Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by -0.8 and returns toward the end of the line. This negative-going ramp starts at time $2T$ (twice the line delay) and doubles to $-1.6B$ at time $2T + A$. The negative-going increment also generates a reflection of amplitude $-0.8B$ which makes the round trip to the source and back, appearing at time $4T$ as a positive ramp rising to $+1.28B$ at time $4T + A$. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.



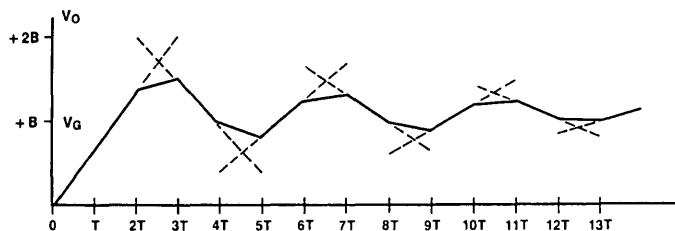
a. Ramp Generator Driving Open-Ended Line

TL/F/9900-35



b. Increments of Output Voltage Treated Individually

TL/F/9900-36



c. Net Output Signal Determined by Superposition
 FIGURE 3-18. Basic Relationships Involved in Ringing

TL/F/9900-37

Ringings (Continued)

In *Figure 3-18c*, the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (i.e., 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 3-18c shows that the peak of each excursion is reached when the earlier of the two constituent ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by ECL or TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 3-18*. Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increment is zero.

Summary

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they

are intended to focus attention on the general methods used to determine the interactions between high-speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept, i.e., mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. ECL input capacitance increases the rise time at the end of the line, thus increasing the effective delay. With parallel termination, i.e., at the end of the line, loads can be distributed along the line. ECL input capacitance modifies the line characteristics and should be taken into account when determining line delay.

References

1. Metzger, G. and Vabre, J., *Transmission Lines with Pulse Excitation*, Academic Press, (1969).
2. Skilling, H., *Electric Transmission Lines*, McGraw-Hill, (1951).
3. Matick, R., *Transmission Lines for Digital and Communication Networks*, McGraw-Hill, (1969).
4. Millman, J. and Taub, H., *Pulse Digital and Switching Waveforms*, McGraw-Hill, (1965).
5. "Time Domain Reflectometry", *Hewlett-Packard Journal*, Vol. 15, No. 6, (February 1964).
6. Feller, A., Kaupp H., and Digiacomia, J., "Crosstalk and Reflections in High-Speed Digital Systems", *Proceedings, Fall Joint Computer Conference*, (1965).

Chapter 4 System Considerations

Introduction

All of National's ECL input and output impedances are designed to accommodate various methods of driving and terminating interconnections. Controlled wiring impedance makes it possible to use simplified equivalent circuits to determine limiting conditions. Specific guidelines and recommendations are based on assumed worst-case combinations. Many of the recommendations may seem conservative, compared to typical observations, but the intent is to help the designer achieve a reliable system in a reasonable length of time with a minimum amount of redesign.

PC Board Transmission Lines

Strictly speaking, transmission lines are not always required for F100K ECL but, when used, they provide the advantages of predictable interconnect delays as well as reflection and ringing control through impedance matching. Two common types of PC board transmission lines are microstrip and stripline, *Figure 4-1*. Stripline requires multilayer construction techniques; microstrip uses ordinary double-clad boards. Other board construction techniques are wire wrap, stitch weld and discrete wired.

Stripline, *Figure 4-1b*, is used where packing density is a high priority because increasing the interconnect layers provides short signal paths. Boards with as many as 14 layers have been used in ECL systems.

Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. In *Figure 4-1a*, the ground plane can be a part of the V_{EE} distribution as long as adequate bypassing from V_{EE} to V_{CC} (ground) is provided. Also, signal routing is simplified and an extra voltage plane is obtained by bonding two microstrip structures back to back, *Figure 4-1c*.

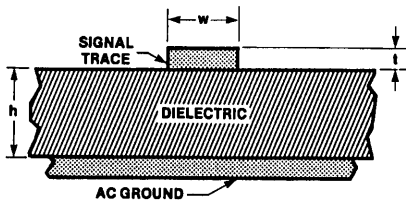
Microstrip

Equation 4-1 relates microstrip characteristic impedance to the dielectric constant and dimensions.¹ Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance no less than the trace width.

$$Z_0 = \left(\frac{60}{\sqrt{0.475 \epsilon_r + 0.67}} \right) \ln \left(\frac{4h}{0.67(0.8w + t)} \right) \quad (4-1)$$

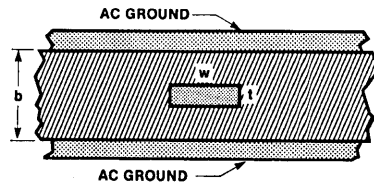
$$= \left(\frac{87}{\sqrt{\epsilon_r + 1.41}} \right) \ln \left(\frac{5.98h}{0.8w + t} \right)$$

where h = dielectric thickness, w = trace width, t = trace thickness, ϵ_r = board material dielectric constant relative to air.



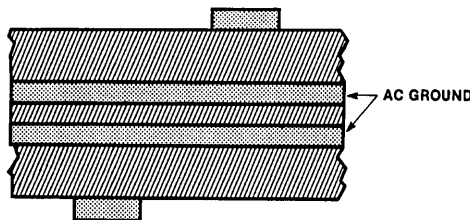
a. Microstrip

TL/F/9901-1



b. Stripline

TL/F/9901-2



c. Composite Microstrip

TL/F/9901-3

FIGURE 4-1. Transmission Lines on Circuit Boards

PC Board Transmission Lines (Continued)

Equation 4-1 was developed from the impedance formula for a wire over ground plane transmission line, Equation 4-2.

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}} \right) \ln \left(\frac{4h}{d} \right) \quad (4-2)$$

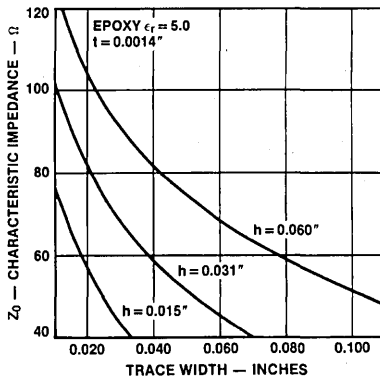
where d = wire diameter, h = distance from ground to wire center.

Comparing Equation 4-1 and 4-2, the term $0.67 (0.8 w + t)$ shows the equivalence between a round wire and a rectangular conductor. The term $0.475 \epsilon_r + 0.67$ is the *effective dielectric constant* for microstrip ϵ_{eff} , considering that a microstrip line has a compound dielectric consisting of the board material and air. The effective dielectric constant is determined by measuring propagation delay per unit of line length and using the following relationship.

$$\delta = 1.016 \cdot \sqrt{\epsilon_{\text{eff}}} \text{ ns/ft} \quad (4-3)$$

where δ = propagation delay, ns/ft.

Propagation delay is a property of the dielectric material rather than line width or spacing. The coefficient 1.016 is the reciprocal of the velocity of light in free space. Propagation delay for microstrip lines on glass-filled G-10 epoxy boards is typically 1.77 ns/ft, yielding an effective dielectric constant of 3.04.

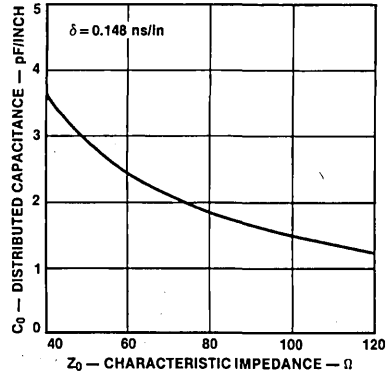


TL/F/9901-4

FIGURE 4-2. Microstrip Impedance Versus Trace Width, G-10 Epoxy

Using $\epsilon_r = 5.0$ in Equation 4-1, Figure 4-2 provides microstrip line impedance as a function of width for several G-10 epoxy board thicknesses. Figure 4-3 shows the related C_0 values, useful for determining capacitive loading effects on line characteristics, (Equation 3-15).

System designers should ascertain tolerances on board dimensions, dielectric constant and trace width etching in order to determine impedance variations. If conformal coating is used the effective dielectric constant of microstrip is increased, depending on the coating material and thickness.



TL/F/9901-5

FIGURE 4-3. Microstrip Distributed Capacitance Versus Impedance, G-10 Epoxy

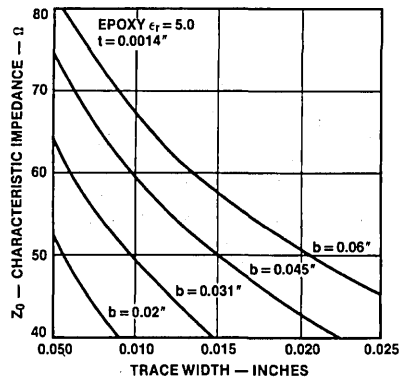
Stripline

Stripline conductors are totally embedded. As a result, the board material determines the dielectric constant. G-10 epoxy boards have a typical propagation delay of 2.26 ns/ft. Equation 4-4 is used to calculate stripline impedances.^{1,2}

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}} \right) \ln \left(\frac{4b}{0.67 \pi (0.8 w + t)} \right) \quad (4-4)$$

where b = distance between ground planes, w = trace width, t = trace thickness, $w/(b-t) < 0.35$ and $t/b < 0.25$.

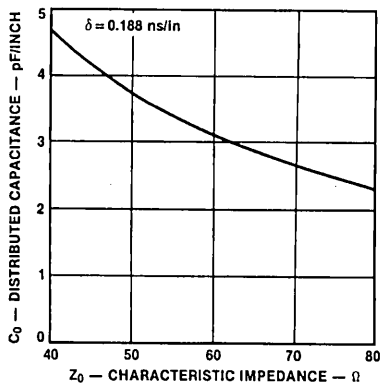
Figure 4-4 shows stripline impedance as a function of trace width, using Equation 4-4 and various ground plane separations for G-10 glass-filled epoxy boards. Related values of C_0 are plotted in Figure 4-5.



TL/F/9901-6

FIGURE 4-4. Stripline Impedance Versus Trace Width, G-10 Epoxy

PC Board Transmission Lines (Continued)



TL/F/9901-7

FIGURE 4-5. Stripline Distributed Capacitance Versus Impedance, G-10 Epoxy

Wire Wrap

Wire-wrap boards are commercially available with three voltage planes, positions for several 24-pin Dual-In-Line Packages (DIP), terminating resistors, and decoupling capacitors. The devices are mounted on socket pins and interconnected with twisted pair wiring. One wire at each end of the twisted pair is wrapped around a signal pin, the other around a ground pin. The #30 insulated wire is uniformly twisted to provide a nominal 93Ω impedance line. Positions for Single-In-Line Package (SIP) terminating resistors are close to the inputs to provide good termination characteristics.

Stitch Weld

Stitch-weld boards are commercially available with three voltage planes and buried resistors between planes. The devices are mounted on terminals and interconnected with insulated wires that are welded to the backside of the terminals. The insulated wires are placed on a controlled thickness over the ground plane to provide a nominal impedance of 50Ω. The boards are available for both DIPs and flatpaks. Use of flatpaks can increase package density and provide higher system performance.

Discrete Wired

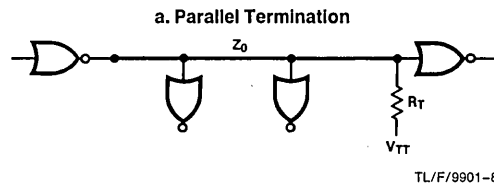
Custom Multiwire* boards are available with integral power and ground planes. Wire is placed on a controlled thickness above the ground plane to obtain a nominal impedance line of 55Ω. Then holes are drilled through the wire and board. Copper is deposited in the drilled holes by an additive-electrolysis process which bonds each wire to the wall of the holes. Devices are soldered on the board to make connection to the wires.

*Multiwire is a registered trademark of the Multiwire Corporation.

Parallel Termination

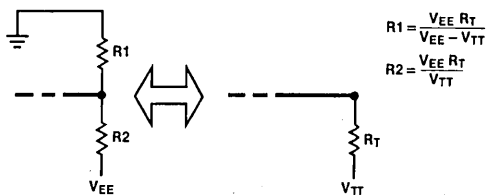
Terminating a line at the receiving end with a resistance equal to the characteristic line impedance is called parallel termination, *Figure 4-6a*. F100K circuits do not have internal pull-down resistors on outputs, so the terminating resistor must be returned to a voltage more negative than V_{OL} to establish the LOW-state output voltage from the emitter follower. A -2V termination return supply is commonly used. This minimizes power consumption and correlates with standard test specifications for ECL circuits. A pair of resistors connected in series between ground (V_{CC}) and the V_{EE}

supply can provide the Thevenin equivalent of a single resistor to -2V if a separate termination supply is not available, *Figure 4-6b*. The average power dissipation in the Thevenin equivalent resistors is about 10 times the power dissipation in the single resistor returned to -2V, as shown in *Figures 5-10* and *5-13*. For either parallel termination method, decoupling capacitors are required between the supply and ground (Chapter 6).



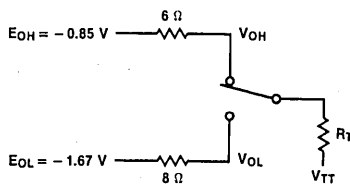
TL/F/9901-8

b. Thevenin Equivalent of R_T and V_{TT}



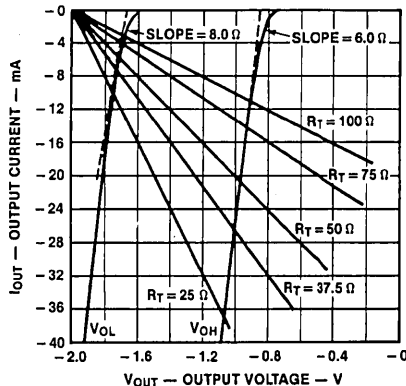
TL/F/9901-9

c. Equivalent Circuit for Determining Approximate V_{OH} and V_{OL} Levels



TL/F/9901-10

d. F100K Output Characteristic with Terminating Resistor R_T Returned to $V_{TT} = -2.0V$



TL/F/9901-11

FIGURE 4-6. Parallel Termination

PC Board Transmission Lines (Continued)

F100K output transistors are designed to drive low-impedance loads and have a maximum output current rating of 50 mA. The circuits are specified and tested with a 50Ω load returned to -2V. This gives nominal output levels of -0.955V at 20.9 mA and -1.705V at 5.9 mA. Output levels will be different with other load currents because of the transistor output resistance. This resistance is nonlinear with load current since it is due, in part, to the base-emitter voltage of the emitter follower, which is logarithmic with output current. With the standard 50Ω load, the effective source resistance is approximately 6Ω in the HIGH state and 8Ω in the LOW state.

The foregoing values of output voltage, output current, and output resistance are used to estimate quiescent output levels with different loads. An equivalent circuit is shown in Figure 4-6c. The ECL circuit is assumed to contain two internal voltage sources E_{OH} and E_{OL} with series resistances of 6Ω and 8Ω respectively. The values shown for E_{OH} and E_{OL} are -0.85V and -1.67V respectively.

The linearized portion of the F100K output characteristic can be represented by two equations:

$$\text{For } V_{OH}: V_{OUT} = -850 - 6 I_{OUT}$$

$$\text{For } V_{OL}: V_{OUT} = -1670 - 8 I_{OUT}$$

where I_{OUT} is in mA, V_{OUT} is in mV.

If the range of I_{OUT} is confined between 8 mA to 40 mA for V_{OH} , and 2 mA to 16 mA for V_{OL} , the output voltage can be estimated within ± 10 mV (Figure 4-6d).

An ECL output can drive two or more lines in parallel, provided the maximum rated current is not exceeded. Another consideration is the effect of various loads on noise margins. For example, two parallel 75Ω terminations to -2V (Figure 4-6d) give output levels of approximately -1.000V and -1.716V. Noise margins are thus 35 mV less in the HIGH state and 11 mV more in the LOW state, compared to 50Ω load conditions. Conversely, a single 75Ω load to -2V causes noise margins 38 mV greater in the HIGH state and 11 mV less in the Low state, compared to a 50Ω load.

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_0 . The ratio of the reflected voltage to the incident voltage V_i is the reflection coefficient ρ .

$$\frac{V_r}{V_i} = \rho = \frac{R_T - Z_0}{R_T + Z_0} \quad (4-5)$$

The initial signal swing at the termination is the sum of the incident and reflected voltages. The ratio of termination signal to incident signal is thus:

$$\frac{V_T}{V_i} = 1 + \rho = \frac{2R_T}{R_T + Z_0} \quad (4-6)$$

The degree of reflections which can be tolerated varies in different situations, but to allow for worst-case circuits, a good rule of thumb is to limit reflections to 15% to prevent excursions into the threshold region of the ECL inputs connected along the line. The range of permissible values of R_T as a function of Z_0 and the reflection coefficient limitations can be determined by rearranging Equation 4-5.

$$R_T = Z_0 \frac{1 + \rho}{1 - \rho} \quad (4-7)$$

Using 15% reflection limits as examples, the range of the R_T/Z_0 ratio is as follows.

$$\frac{1.15}{0.85} > \frac{R_T}{Z_0} > \frac{0.85}{1.15} \quad 1.35 > \frac{R_T}{Z_0} > 0.74 \quad (4-8)$$

The permissible range of the R_T/Z_0 ratio determines the tolerance ranges for R_T and Z_0 . For example, using the foregoing ratio limits, R_T tolerances of $\pm 10\%$ allow Z_0 tolerance limits of +22% and -19%; R_T tolerances of $\pm 5\%$ allow Z_0 tolerance limits of +28% and -23%.

An additional requirement on the maximum value of R_T is related to the value of quiescent I_{OH} current needed to insure sufficient negative-going signal swing when the ECL driver switches from the HIGH state to the LOW state. The npn emitter-follower output of the ECL circuit cannot act as a voltage source driver for negative-going transitions. When the voltage at the base of the emitter follower starts going negative as a result of an internal state change, the output current of the emitter follower starts to decrease. The transmission line responds to the decrease in current by producing a negative-going change in voltage. The ratio of the voltage change to the current change is, of course, the characteristic impedance Z_0 . Since the maximum decrease in current that the line can experience is from I_{OH} to zero, the maximum negative-going transition which can be produced is the product $I_{OH} Z_0$.

If the $I_{OH} Z_0$ product is greater than the normal negative-going signal swing, the emitter follower responds by limiting the current change, thereby controlling the signal swing. If, however, the $I_{OH} Z_0$ product is too small, the emitter follower is momentarily turned off due to insufficient forward bias of its base-emitter junctions, causing a discontinuous negative-going edge such as the one shown in Figure 4-14. In the output-LOW state the emitter follower is essentially non-conducting for V_{OL} values more positive than about -1.55V. Using this value as a criterion and expressing I_{OH} and V_{OH} in terms of the equivalent circuit of Figure 4-6c, an upper limit on the value of R_T can be developed.

$$\begin{aligned} \Delta V &= I_{OH} Z_0 > 1.55 - |V_{OH}| \\ \left(\frac{E_{OH} - V_{TT}}{R_0 + R_T} \right) Z_0 &> 1.55 - \left| \frac{V_{TT} R_0 = E_{OH} R_T}{R_0 + R_T} \right| \\ R_T &< \frac{(E_{OH} - V_{TT}) Z_0 - (1.55 - |V_{TT}|) R_0}{1.55 - |E_{OH}|} \end{aligned} \quad (4-9)$$

For a V_{TT} of -2V, R_0 of 6Ω and E_{OH} of -0.85V, Equation 4-9 reduces to

$$R_T < 1.64 Z_0 + 3.86\Omega$$

For $Z_0 = 50\Omega$, the emitter follower cuts off during a negative-going transition if R_T exceeds 86Ω. Changing the voltage level criteria to -1.60V to insure continuous conduction in the emitter follower gives an upper limit of 77Ω for a 50Ω line. For a line terminated at the receiving end with a resistance to -2V, a rough rule-of-thumb is that termination resistance should not exceed line impedance by more than 50%. This insures a satisfactory negative-going signal swing to ECL inputs connected along the line. The quiescent V_{OL} level, after all reflections have damped out, is determined by R_T and the ECL output characteristic.

Input Impedance

The input impedance of ECL circuits is predominately capacitive. A single-function input has an effective value of about 1.5 pF for F100K flatpak, as determined by its effect on reflected and transmitted signals on transmission lines.

Input Impedance (Continued)

In practical calculations, a value of 2 pF should be used. Approximately one third of this capacitance is attributed to the internal circuitry and two thirds to the flatpak pin and internal bonding.

For F100K flatpak circuits, multiple input lines may appear to have up to 3 pF to 4 pF but never more. For example, in the F100102, an input is connected internally to all five gates, but because of the philosophy of buffering these types of inputs in the F100K family this input appears as a unit load with a capacitance of approximately 2 pF. For applications such as a data bus, with two or more outputs connected to the same line, the capacitance of a passive-LOW output can be taken as 2 pF.

Capacitive loads connected along a transmission line increase the propagation delay of a signal along the line. The modified delay can be determined by treating the load capacitance as an increase in the intrinsic distributed capacitance of the line, discussed in Chapter 3. The intrinsic capacitance of any stubs which connect the inputs to the line should be included in the load capacitance. The intrinsic capacitance per unit length for G-10 epoxy boards is shown in Figure 4-3 and 4-5 for microstrip and stripline respectively. For other dielectric materials, the intrinsic capacitance C_0 can be determined by dividing the intrinsic delay δ (Equation 4-3) by the line impedance Z_0 .

The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to a rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough, however, the first reflection returning from the end of the stub adds to the attenuated incident wave while it is still rising. The sum of the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines (Figure 4-10). The same considerations apply when the termination resistance is not connected at the end of the line; a section of line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

Series Termination

Series termination requires a resistor between the driver and transmission line, Figure 4-7. The receiving end of the line has no termination resistance. The series resistor value should be selected so that when added to the driver source resistance, the total resistance equals the line impedance. The voltage divider action between the net series resistance and the line impedance causes an incident wave of half amplitude to start down the line. When the signal arrives at the unterminated end of the line, it doubles and is thus restored to a full amplitude. Any reflections returning to the source are absorbed without further reflection since the line and source impedance match. This feature, source absorption, makes series termination attractive for interconnection paths involving impedance discontinuities, such as occur in backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step

signal. The initial signal at the driver end is half amplitude, rising to full amplitude only after the reflection returns from the open end of the line. In Figure 4-7, one load is shown connected at point D, away from the line end. This input receives a full amplitude signal with a continuous edge if the distance l to the open end of the line is within recommended lengths for unterminated line (Figure 4-10).

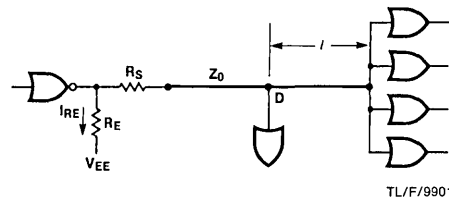


FIGURE 4-7. Series Termination

The signal at the end has a slower rise time than the incident wave because of capacitive loading. The increase in rise time to the 50% point effectively increases the line propagation delay, since the 50% point of the signal swing is the input signal timing reference point. This added delay as a function of the product line impedance and load capacitance is discussed in Chapter 3.

Quiescent V_{OH} and V_{OL} levels are established by resistor R_E (Figure 4-7), which also acts with V_{EE} to provide the negative-going drive into R_S and Z_0 when the driver output goes to the LOW state. To determine the appropriate R_E value, the driver output can be treated as a simple mechanical switch which opens to initiate the negative-going swing. At this instant, Z_0 acts as a linear resistor returned to V_{OH} . Thus the components form a simple circuit of R_E , R_S and Z_0 in a series, connected between V_{EE} and V_{OH} . The initial current in this series circuit must be sufficient to introduce a 0.38V transient into the line, which then doubles at the load end to give 0.75V swing.

$$I_{RE} = \frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.38}{Z_0} \quad (4-10)$$

Any I_{OH} current flowing in the line before the switch opens helps to generate the negative swing. This current may be quite small, however, and should be ignored when calculating R_E .

Increasing the minimum signal swing into the line by 30% to 0.49V insures sufficient pull-down current to handle reflection currents caused by impedance discontinuities and load capacitance. The appropriate R_E value is determined from the following relationship.

$$\frac{V_{OH} - V_{EE}}{R_E + R_S + Z_0} \geq \frac{0.49}{Z_0} \quad (4-11)$$

For the R_E range normally used, quiescent V_{OH} averages approximately 0.955V and $V_{EE} = -4.5V$. The value of R_S is equal to Z_0 minus R_0 (R_0 averages 7 Ω). Inserting these values and rearranging Equation 4-11 gives the following.

$$R_E \leq 5.23 Z_0 + 7\Omega \quad (4-12)$$

Power dissipation in R_E is listed in Figure 5-14. The power dissipation in R_E is greater than in R_T of a parallel termination to $-2V$, but still less than the two resistors of the Thevenin equivalent parallel termination, see Figure 5-10, 5-13 and 5-14.

The number of driven inputs on a series terminated line is limited by the voltage drop across R_S in the quiescent HIGH state, caused by the finite input currents of the ECL loads. I_{IH} values are specified on data sheets for various types of

Series Termination (Continued)

inputs, with a worst-case value of 265 μA for simple gate inputs. The voltage drop subtracts from the HIGH-state noise margin as outlined in *Figure 4-8a*.

However, there is more HIGH-state noise margin initially, because there is less I_{OH} with the R_E load than with the standard 50 Ω load to $-2V$. This makes V_{OH} more positive; the increase ranges from 43 mV for a 50 Ω line to 82 mV for a 100 Ω line. Using this V_{OH} increase as a limit on the voltage drop across R_S assures that the HIGH-state noise margin is as good as in the parallel terminated case. Dividing the V_{OH} increase by $R_S + R_0 (= Z_0)$ gives the allowed load input current (I_X) in *Figure 4-8a*. This works out to 0.86 mA for a 50 Ω line, 0.92 mA for a 75 Ω line and 0.82 mA for a 100 Ω line. Load input current greater than these values can be tolerated at some sacrifice in noise margin. If, for example, an additional 50 mV loss is feasible, the maximum values of current become 1.86 mA, 1.59 mA and 1.32 mA for 50 Ω , 75 Ω and 100 Ω lines respectively.

An ECL output can drive more than one series terminated line, as suggested in *Figure 4-8b*, if the maximum rated output current of 50 mA is not exceeded. Also, driving two or more lines requires a lower R_E value. This makes the quiescent I_{OH} higher and consequently V_{OH} lower, due to the voltage drop across R_0 . This voltage drop decreases the HIGH-state noise margin, which may become the limiting factor (rather than the maximum rated current), depending on the particular application.

The appropriate R_E value can be determined using Equation 4-13 for $V_{EE} = -4.5V$.

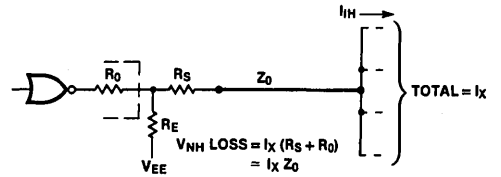
$$\frac{1}{R_E} \geq \frac{1}{6.23 Z_1 - R_{S1}} + \frac{1}{6.23 Z_2 - R_{S2}} + \frac{1}{6.23 Z_3 - T_{S3}} \quad (4-13)$$

Circuits with multiple outputs (such as the F100112) provide an alternate means of driving several lines simultaneously (*Figure 4-8c*). Note, each output should be treated individually when assigning load distribution, line impedance, and R_E value.

Unterminated Lines

Lines can be used without series or parallel termination if the line delay is short compared to the signal rise time. Ringing occurs because the reflection coefficient at the open (receiving) end of the line is positive (nominally +1) while the reflection coefficient at the driving end is negative (approximately -0.8). These opposite polarity reflection coefficients cause any change in signal voltage to be reflected back and forth, with a polarity change each time the signal is reflected from the driver. Net voltage change on the line is thus a succession of increments with alternating polarity and decreasing magnitude. The algebraic sum of these increments is if the observed ringing. The general relationships among rise time, line delay, overshoot and undershoot are discussed in Chapter 3, using simple waveforms for clarity.

Excessive overshoot on the positive-going edge of the signal drives input transistors into saturation. Although this does not damage an ECL input, it does cause excessive recovery times and makes propagation delays unpredict-



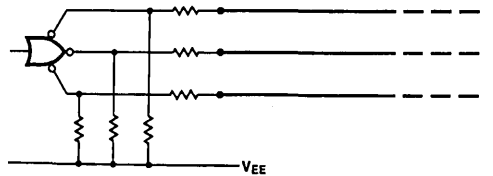
TL/F/9901-13

a. Noise Margin Loss Due to Load Input Current



TL/F/9901-14

b. Driving Several Lines from one Output



TL/F/9901-15

c. Using Multiple Output Element for Load Sharing

FIGURE 4-8. Loading Considerations for Series Termination

able. Undershoot (following the overshoot) must also be limited to prevent signal excursions into the threshold region of the loads. Such excursions could cause exaggerated transition times at the driven circuit outputs, and could also cause multiple triggering of sequential circuits. Signal swing, exclusive of ringing, is slightly greater on unterminated lines than on parallel terminated lines; I_{OH} is less and I_{OL} is greater with the R_E load, (*Figure 4-9a*) making V_{OH} higher and V_{OL} lower.

For worst case combinations of driver output and load input characteristics, a 35% overshoot limit insures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.

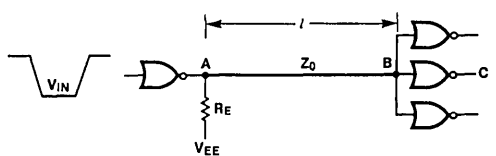
For distributed loading, ringing is satisfactorily controlled if the 2-way modified line delay does not exceed the 20% to 80% rise time of the driver output. This relationship can be expressed as follows, using the symbols from Chapter 3 and incorporating the effects of load capacitance on line delay.

$$t_r = 2T' = 2\ell \delta' = 2\ell \delta \sqrt{1 + \frac{C_L}{\ell C_0}}$$

Solving this expression for the line length (ℓ):

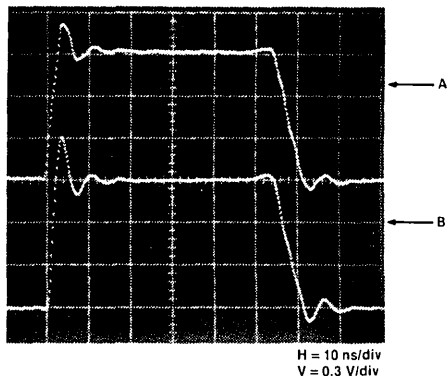
$$\ell_{\max} = \frac{1}{2} \sqrt{\left(\frac{C_L}{C_0}\right)^2 + \left(\frac{t_r}{\delta}\right)^2} - \frac{C_L}{2C_0} \quad (4-14)$$

Unterminated Lines (Continued)



TL/F/9901-16

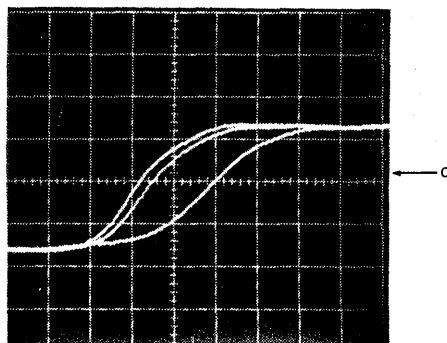
a. Unterminated Line



H = 10 ns/div
V = 0.3 V/div

TL/F/9901-17

b. Line Voltages Showing Stair-step Trailing Edges



H = 1 ns/div
V = 0.3 V/div

TL/F/9901-18

c. Load Gate Output Showing Net Propagation Increase for Increasing Values of R_E : 330 Ω , 510 Ω , 1 k Ω

FIGURE 4-9. Effect on R_E Value on Trailing-Edge Propagation

The shorter the rise time, the shorter the permissible line length. For F100K ECL, the minimum rise time from 20% to 80% is specified as 0.5 ns. Using this rise time and 2 pF per fan-out load, calculated maximum line lengths for G-10 epoxy microstrip are listed in Figure 4-10a. The length (l) in the table is the distance from the terminating resistor to the input of the device(s). For F100K ECL the case described in Figure 4-10a is the only one calculated, since all other combinations are approximately the same. For other combinations of rise time, impedance, fan-out or line char-

acteristics (δ and C_0), maximum lengths are calculated using Equation 4-14. For the convenience of those who are also using 10K ECL, maximum recommended lengths of unterminated lines are listed in Figure 4-10b to 4-10e.

| Z_0 | Number of Fan-Out Loads | | | |
|-------|-------------------------|------|------|------|
| | 1 | 2 | 3 | 4 |
| 50 | 1.37* | 1.13 | 0.95 | 0.81 |
| 62 | 1.33 | 1.07 | 0.87 | 0.70 |
| 75 | 1.25 | 0.95 | 0.75 | 0.61 |
| 90 | 1.18 | 0.85 | 0.66 | 0.53 |
| 100 | 1.15 | 0.82 | 0.61 | 0.49 |

*Length in inches.
Unit load = 2 pF, δ = 0.148 ns/inch

FIGURE 4-10a. F100K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Distributed Loading

| Z_0 | Number of Fan-Out Loads | | | | |
|-------|-------------------------|------|------|------|------|
| | 2 | 3 | 4 | 6 | 8 |
| 50 | 4.15* | 3.75 | 3.45 | 2.85 | 2.45 |
| 62 | 3.95 | 3.50 | 3.15 | 2.55 | 2.10 |
| 75 | 3.75 | 3.25 | 2.85 | 2.25 | 1.85 |
| 90 | 3.55 | 3.00 | 2.60 | 2.00 | 1.60 |
| 100 | 3.45 | 2.85 | 2.45 | 1.85 | 1.45 |

*Length in inches.
Unit load = 3 pF, δ = 0.148 ns/in.

FIGURE 4-10b. 10K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Distributed Loading

| Z_0 | Number of Fan-Out Loads | | | | |
|-------|-------------------------|------|------|------|------|
| | 1 | 2 | 4 | 6 | 8 |
| 50 | 4.40* | 3.65 | 2.60 | 1.90 | 1.40 |
| 62 | 4.30 | 3.45 | 2.30 | 1.60 | 1.15 |
| 75 | 4.20 | 3.20 | 2.05 | 1.40 | 0.95 |
| 90 | 4.05 | 2.95 | 1.75 | 1.05 | 0.65 |
| 100 | 3.90 | 2.80 | 1.60 | 0.90 | 0.50 |

*Length in inches.
Unit load = 3 pF, δ = 0.148 ns/in.

FIGURE 4-10c. 10K Maximum Worst-Case Line Lengths for Unterminated Microstrip, Concentrated Loading

| Z_0 | Number of Fan-Out Loads | | | | |
|-------|-------------------------|------|------|------|------|
| | 2 | 3 | 4 | 6 | 8 |
| 50 | 3.30* | 3.00 | 2.70 | 2.25 | 2.90 |
| 62 | 3.15 | 2.80 | 2.50 | 2.00 | 1.65 |
| 75 | 3.00 | 2.60 | 2.25 | 1.80 | 1.45 |
| 90 | 2.80 | 2.40 | 2.05 | 1.55 | 1.25 |

*Length in inches.
Unit load = 3 pF, δ = 0.188 ns/in.

FIGURE 4-10d. 10K Maximum Worst-Case Line Lengths for Unterminated Stripline, Distributed Loading

Unterminated Lines (Continued)

| Z ₀ | Number of Fan-Out Loads | | | | |
|----------------|-------------------------|------|------|------|------|
| | 1 | 2 | 4 | 6 | 8 |
| 50 | 3.45* | 2.85 | 2.00 | 1.50 | 1.10 |
| 62 | 3.40 | 2.70 | 1.80 | 1.30 | 0.90 |
| 75 | 3.30 | 2.55 | 1.60 | 1.10 | 0.75 |
| 90 | 3.15 | 2.35 | 1.40 | 0.85 | 0.50 |
| 100 | 3.10 | 2.20 | 1.25 | 0.70 | 0.40 |

*Length in inches.
Unit load = 3 pF, δ = 0.188 ns/in.

FIGURE 4-10e. 10K Maximum Worst-Case Line Lengths for Unterminated Stripline, Concentrated Loading

A load capacitance concentrated at the end of the line restricts line length more than a distributed load does. Maximum recommended lengths for fiberglass epoxy dielectric and a 0.5 ns rise time are listed in *Figure 4-10* for microstrip. For line impedances not listed, linear interpolation can be used to determine appropriate line lengths. Appropriate line lengths for dielectric materials with a different propagation constant δ can be determined by multiplying the listed values by the fiberglass epoxy δ and then dividing by the δ of the other material. For example, a line length for a material which has a microstrip δ of 0.1 ns/inch is determined by multiplying the length given in the microstrip table (for a desired impedance and load) by 0.148 and dividing by 0.1.

Resistor R_E must provide the current for the negative-going signal at the driver output. Line input and output waveforms are noticeably affected if R_E is too large, as shown in *Figure 4-9b*. The negative-going edge of the signal falls in stair-step fashion, with three distinct steps visible at point A. The waveform at point B shows a step in the middle of the negative-going swing. The effect of different R_E values on the net propagation time through the line and the driven loads is evident in *Figure 4-9c* which shows the output signal of one driven gate in a multiple exposure photograph. The horizontal sweep (time axis) was held constant with respect to the input signal of the driver. The earliest of the three output signals occurs with an R_E value of 330Ω. Changing R_E to 510Ω increases the net propagation delay by 0.3 ns, the horizontal offset between the first and second signals. Changing R_E to 1 kΩ produces a much greater increase in net propagation delay, indicating that the negative-going signal at B contains several steps. In practice, a satisfactory negative-going signal results when the R_E value is chosen to give an initial negative-going step of 0.6V at the driving end of the line. This gives an upper limit on the value of R_E, as shown in Equation 4-15.

$$\text{initial step} = \Delta l \cdot Z_0 = \frac{(V_{OH} - V_{EE}) Z_0}{R_E + Z_0} \geq 0.6$$

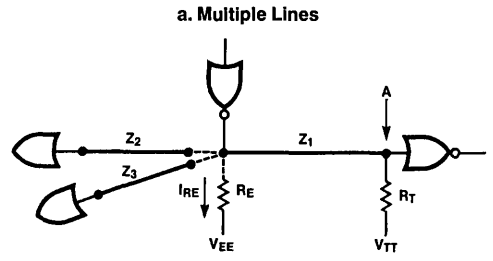
$$R_E \leq 6.25 Z_0 \quad (4-15)$$

An ECL output can drive two or more unterminated lines, provided each line length and loading combination is within the recommended constraints. The appropriate R_E value is determined from Equation 4-15, using the parallel impedance of the two or more lines for Z₀.

An ECL output can simultaneously drive terminated and unterminated lines, although the negative-going edge of the signal shows two or more distinct steps when the stubs are long unless some extra pull-down current is provided. *Figure 4-11a* shows an ECL circuit driving a parallel terminated line, with provision for connecting two worst-case untermi-

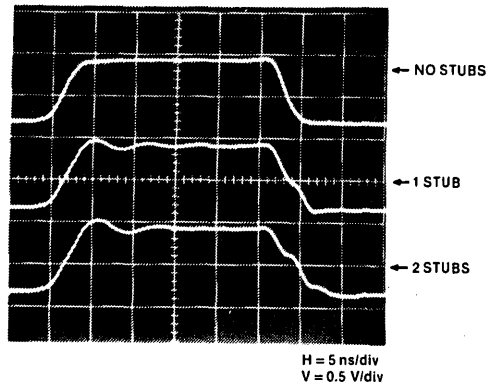
nated lines to the driver output. Waveforms at the termination resistor (point A) are shown in the multiple exposure photograph of *Figure 4-11b*. The upper trace shows a normal signal without stubs connected to the driver. The middle trace shows the effect of connecting one stub to the driver. The step in the negative-going edge indicates that the quiescent I_{OH} current through R_T is not sufficient to cause a full signal for both lines. The relationship between the quiescent I_{OH} current through R_T and the negative-going signal swing was discussed earlier in connection with parallel termination.

The bottom trace in *Figure 4-11* shows the effect of connecting two stubs to the driver output. The steps in trailing edge are smaller and more pronounced. The deteriorated trailing edge of either the middle or lower waveform increas-



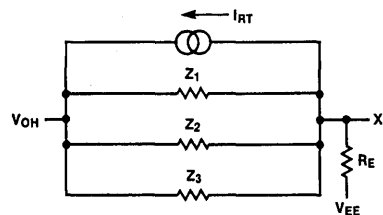
TL/F/9901-19

b. Waveforms at Termination Point A



TL/F/9901-20

c. Equivalent Circuit for Determining Initial Negative Voltage Step at the Driver Output



TL/F/9901-21

FIGURE 4-11. Driving Terminated and Unterminated Lines in Parallel

Unterminated Lines (Continued)

es the switching time of the circuit connected to point A. If this extra delay cannot be tolerated, additional pull-down current must be provided. One method uses a resistor to V_{EE} as suggested in *Figure 4-11a*. The initial negative-going step at point A should be about 0.7V to insure a good fall rate through the threshold region of the driven gate. The initial step at the driver output should also be 0.7V. If the driver output is treated as a switch that opens to initiate the negative-going signal, the equivalent circuit of *Figure 4-11c* can be used to determine the initial voltage step at the driver output (point X). The value of the current source I_{RT} is the quiescent I_{OH} current through R_T . Using Z' to denote the parallel impedance of the transmission lines and ΔV for the desired voltage step at X, the appropriate value of R_E can be determined from the following equation, using absolute values to avoid polarity confusion.

$$R_E = \left(|V_{EE}| - |V_{OH}| - \Delta V \right) \cdot \left(\frac{Z'}{|\Delta V| - |I_{RT}Z'|} \right)$$

For a sample calculation, assume that R_T and the line impedances are each 100 Ω , V_{OH} is -0.955V, ΔV is 0.750V, V_{EE} is -4.5V and V_{TT} is -2V. I_{RT} is thus 10.45 mA and the calculated value of R_E is 232 Ω . In practice, this value is on the conservative side and can be increased to the next larger (10%) standard value with no appreciable sacrifice in propagation through the gate at point A.

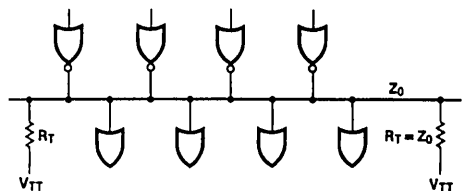
Again, the foregoing example is based on worst-case stub lengths (the longest permissible). With shorter stubs, the effects are less pronounced and a point is reached where extra pull-down current is not required because the reflection from the end of the stub arrives back at the driver while the original signal is still falling. Since the reflection is also negative going, it combines with and reinforces the falling signal at the driver, eliminating the steps. The net result is a smoothly falling signal but with increased fall time compared to the stubless condition.

The many combinations of line impedance and load make it practically impossible to define just with stub length begins to cause noticeable steps in the falling signal. A rough rule-of-thumb would be to limit the stub length to one-third of the values given in *Figure 4-10*.

Data Bussing

Data bussing involves connecting two or more outputs and one or more inputs to the same signal line, (*Figure 4-12*). Any one of the several drivers can be enabled and can apply data to the line. Load inputs connected to the line thus receive data from the selected source. This method of steering data from place to place simplifies wiring and tends to minimize package count. Only one of the drivers can be enabled at a given time; all other driver outputs must be in the LOW state. Termination resistors matching the line impedance are connected to both ends of the line to prevent reflections. For calculating the modified delay of the line (*Chapter 3*) the capacitance of a LOW (unselected) driver output should be taken as 2 pF.

An output driving the line sees an impedance equal to half the line impedance. Similarly, the quiescent I_{OH} current is higher than with a single termination. For line impedance less than 100 Ω , the I_{OH} current is greater than the data sheet test value, with a consequent reduction of HIGH-state noise margin. This loss can be eliminated if necessary by



TL/F/8901-22

FIGURE 4-12. Data Bus or Party Line

using multiple output gates (F100112) and paralleling two outputs for each driver. In the quiescent LOW state, termination current is shared among all the output transistors on the line. This sharing makes V_{OL} more positive than if only one output were conducting all of the current. For example, a 100 Ω line terminated at both ends represents a net 50 Ω DC load, which is the same as the data sheet condition for V_{OL} . If one worst-case output were conducting all the current, the V_{OL} would be -1.705V. If another output with identical DC characteristics shares the load current equally, the V_{OL} level shifts upward by about 25 mV. Connecting two additional outputs for a total of four with the same characteristics shifts V_{OL} upward another 22 mV. Connecting four more identical outputs shifts V_{OL} upward another 20 mV. Thus the V_{OL} shift for eight outputs having identical worst-case V_{OL} characteristics is approximately 67 mV. In practice, the probability of having eight circuits with worst-case V_{OL} characteristics is quite low. The output with the highest V_{OL} tends to conduct most of the current. This limits the upward shift to much less than the theoretical worst-case value. In addition, the LOW-state noise margin is specified greater than the HIGH-state margin to allow for V_{OL} shift when outputs are paralleled.

In some instances a single termination is satisfactory for a data bus, provided certain conditions are fulfilled. The single termination is connected in the middle of the line. This requires that for each half of the line, from the termination to the end, the line length and loading must comply with the same restrictions as unterminated lines to limit overshoot and undershoot to acceptable levels. The termination should be connected as near as possible to the electrical mid-point of the line, in terms of the modified line delay from the termination to either end. Another restriction is that the time between successive transitions, i.e., the nominal bit time, should not be less than 15 ns. This allows time for the major reflections to damp out and limits additive reflections to a minor level.

Wired-OR

In general-purpose wired-OR logic connections, where two or more driver outputs are expected to be in the HIGH state simultaneously, it is important to minimize the line length between the participating driver outputs, and to place the termination as close as possible to the mid-point between the two most widely separated sources. This minimizes the negative-going disturbances which occur when one HIGH output turns off while other outputs remain HIGH. The driver output going off represents a sudden decrease in line current, which in turn generates a negative-going voltage on the line. A finite time is required for the other driver outputs (quiescently HIGH) to supply the extra current. The net re-

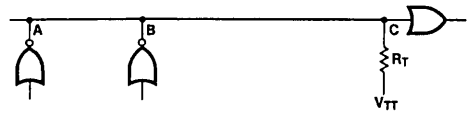
Wired-OR (Continued)

sult is a "V" shaped negative glitch whose amplitude and duration depend on three factors: current that the off-going output was conducting, the line impedance, and the line length between outputs. If the separation between outputs is kept within about one inch, the transient will not propagate through the driven load circuits.

If a wired-OR connection cannot be short, it may be necessary to design the logic so that the signal on the line is not sampled for some time after the normal propagation delay (output going negative) of the element being switched. Normal propagation delay is defined as the case where the element being switched is the only one on the line in the HIGH state, resulting in the line going LOW when the element switches. In this case, the propagation delay is measured from the 50% point on the input signal of the off-going element to the 50% point of the signal at the input farthest away from the output being switched. The extra wiring time required in the case of a severe negative glitch is, in a worst-case physical arrangement, twice the line delay between the off-going output and the nearest quiescently HIGH output, plus 2 ns.

An idea of how the extra waiting time varies with physical arrangement can be obtained by qualitatively comparing the signal paths in *Figure 4-13*. With the outputs at A and B quiescently HIGH, the duration of the transient observed at C is longer if B is the off-going output than if A is the off-going element. This is because the negative-going voltage generated at B must travel to A, whereupon the corrective signal is generated, which subsequently propagates back toward C. Thus the corrective signal lags behind the initial transient, as observed at C, by twice the line delay between A and B. On the other hand, if the output at A generates the negative-going transient, the corrective response starts

when the transient reaches point B. Consequently, the transient duration observed at C is shorter by twice the line delay from A to B.



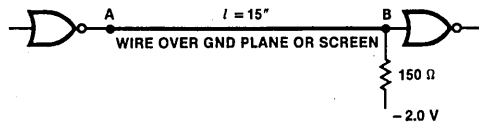
TL/F/9901-23

FIGURE 4-13. Relative to Wired-OR Propagation

Backplane Interconnections

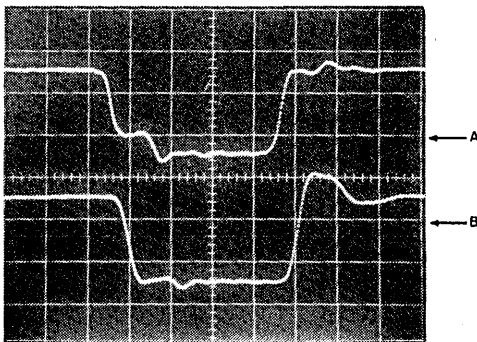
Several types of interconnections can be used to transmit a signal between logic boards. The factors to be considered when selecting a particular interconnection for a given application are cost, impedance discontinuities, predictability of propagation delay, noise environment, and bandwidth. Single-ended transmission over an ordinary wire is the most economical but has the least predictable impedance and propagation delay. At the opposite end of the scale, coaxial cable is the most costly but has the best electrical characteristics. Twisted pair and similar parallel wire interconnection cost and quality fall in between.

For single-wire transmission through the backplane, a ground plane or ground screen (Chapter 5) should be provided to establish a controlled impedance. A wire over a ground plane or screen has a typical impedance of 150Ω with variations on the order of $\pm 33\%$, depending primarily on the distance from ground and the configuration of the ground. *Figure 4-14* illustrates the effects of impedance variations with a 15-inch wire parallel terminated with 150Ω to $-2V$. *Figure 4-14b* shows source and receiver waveforms when the wire is in contact with a continuous ground plane.



TL/F/9901-24

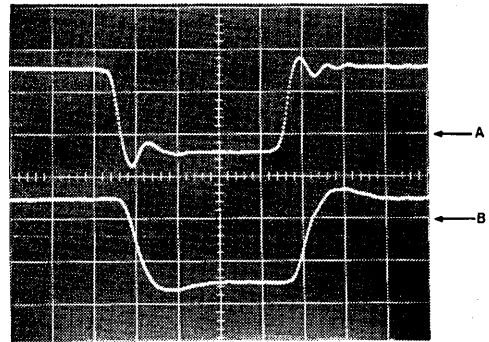
a. Wire over Ground Plane or Screen



H = 5 ns/div
V = 0.4 ns/div

TL/F/9901-25

b. Wire in Contact with Ground Plane



H = 5 ns/div
V = 0.4 V/div

TL/F/9901-26

c. Wire Spaced $\frac{1}{8}$ " from Ground Screen

FIGURE 4-14. Parallel Terminated Backplane Wire

Backplane Interconnections (Continued)

The negative-going signal at the source shows an initial step of only 80% of a full signal swing. This occurs because the quiescent HIGH-state current I_{OH} (about 7 mA) multiplied by the impedance of the wire (approximately 90Ω) is less than the normal signal swing, and this condition allows the driver emitter follower to turn off. The negative-going signal at the receiving end is greater by 25% ($1 + \rho = 1.25$). The receiving end mismatch causes a negative-going reflection which returns to the source and establishes the V_{OL} level. The positive-going signal at the source shows a normal signal swing, with the receiving end exhibiting approximately 25% overshoot.

Figure 4-14c shows waveforms for a similar arrangement, but with the wire about $\frac{1}{8}$ inch from a ground screen. The impedance of the wire is greater than 150Ω termination, but small variations in impedance along the wire cause intermediate reflections which tend to lengthen the rise and fall times of the signal. As a result, the received signal does not exhibit pronounced changes in slope as would be expected if a 200Ω constant impedance line were terminated with 150Ω .

Series source resistance can also be used with single wire interconnections to absorb reflection. Figure 4-15a shows a 16-inch wire with a ground screen driven through a source resistance of 100Ω . The waveforms (Figure 4-15b) show that although reflections are generated, they are largely absorbed by the series resistor, and the signal received at the load exhibits only slight changes and overshoot. Series termination techniques can also be used when the signal into the wire comes from the PC board transmission line. Figure 4-16a illustrates a 12-inch wire over a ground screen, with 12-inch microstrip lines at either end of the wire. The output is heavily loaded (fan-out of 8) and the combination of impedances produces a variety of reflections at the input to the first microstrip line, shown in the upper trace of Figure 4-16b. The lower trace shows the final output; a comparison between the two traces shows the effectiveness of damping in maintaining an acceptable signal at the output. Figure 4-16c shows the signals at the input to the driving gate and at the output of the load gate, with a net through-put time of 8.5 ns. The circuit in Figure 4-16a is a case of mismatched transmission lines, discussed in Chapter 3.

Signal propagation along a single wire tends to be fast because the dielectric medium is mostly air. However, impedance variations along a wire cause intermediate reflections which tend to increase rise and fall times, effectively increasing propagation delay. Effective propagation delays are in the range of 1.5 to 2.0 ns per foot of wire. Load capacitance at the receiving end also increases rise and fall time (Chapter 3), further increasing the effective propagation delay.

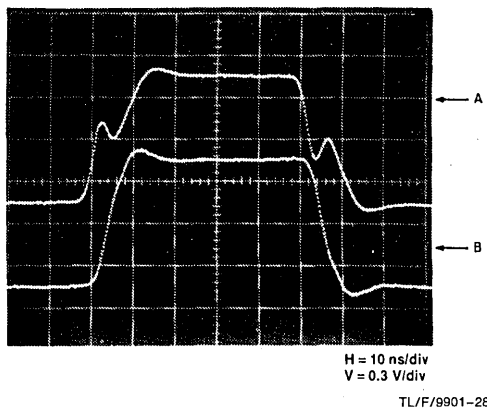
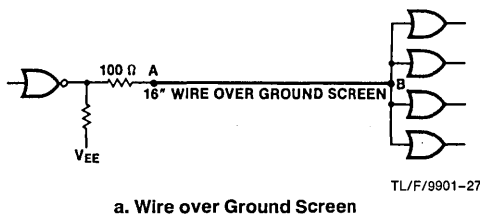
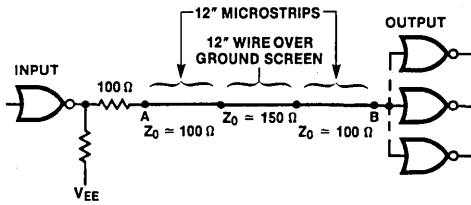


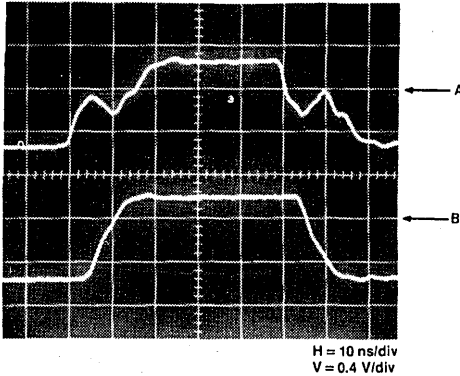
FIGURE 4-15. Series Terminated Backplane Wire

Backplane Interconnections (Continued)



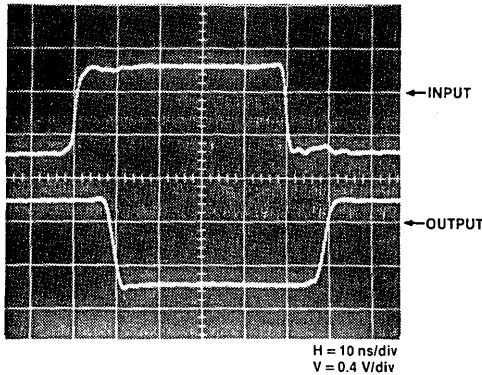
a. Backplane Wire Interconnecting PC Board Lines

TL/F/9901-29



b. Signals into the First Microstrip and at the Loads

TL/F/9901-30



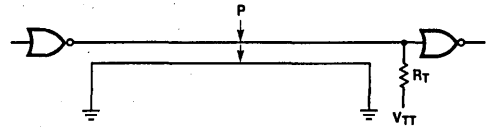
c. Input to Driving Gate and Output of Load Gate

TL/F/9901-31

FIGURE 4-16. Signal Path with Sequence of Microstrip, Wire, Microstrip

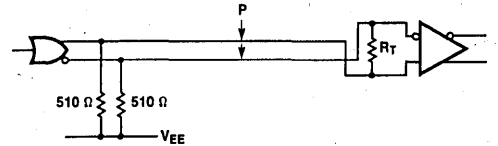
Better control of line impedance and faster propagation can be achieved with a twisted pair. A twisted pair of AWG 26 Teflon* insulated wires, two twists per inch, exhibits a propagation delay of 1.33 ns/ft and an impedance of 115Ω. Twisted pair lines are available in a variety of sizes, impedances and multiple-pair cables. Figure 4-17a illustrates sin-

*Teflon is a registered trademark of E.I. du Pont de Nemours Company.



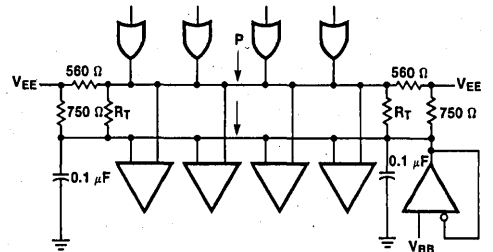
a. Single-ended Twisted Pair

TL/F/9901-32



b. Differential Transmission Reception

TL/F/9901-33



c. Backplane Data Bus

TL/F/9901-34

FIGURE 4-17. Twisted Pair Connections

gle-ended driving and receiving. In addition to improved propagation velocity, the magnetic fields of the two conductors tend to cancel, minimizing noise coupled into adjacent wiring.

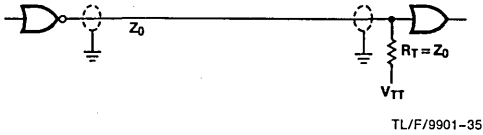
Differential line driving and receiving complementary gates as the driver and an F100114 line receiver is illustrated in Figure 4-17b. Differential operation provides high noise immunity, since common mode input voltages between -0.55V and -3.0V are rejected. The differential mode is recommended for communication between different parts of a system, because it effectively nullifies ground voltage differences. For long runs between cabinets or near high power transients, interconnections using shielded twisted pair are recommended.

Twisted pair lines can be used to implement party line type data transfer in the backplane, as indicated in Figure 4-17c. Only one driver should be enabled at a given time; the other outputs must be in the VOL state. The VBB reference voltage is available on pin 22 of the flatpack and pin 19 of the dual-in-line package for the F100114.

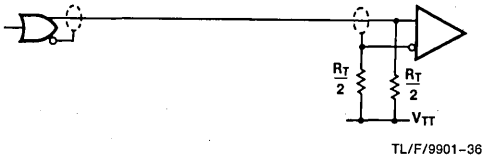
In the differential mode, a twisted pair can send high-frequency symmetrical signals, such as clock pulses, of 100 MHz over distances of 50 to 100 feet. For random data, however, bit rate capability is reduced by a factor of four or five due to line rise effects on time jitter.³

Backplane Interconnections (Continued)

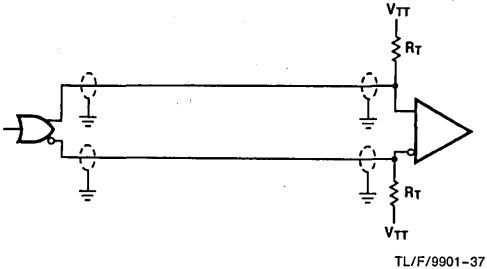
Coaxial cable offers the highest frequency capability. In addition, the outer conductor acts as a shield against noise, while the uniformity of characteristics simplifies the task of matching time delays between different parts of the system. In the single-ended mode, *Figure 4-18a*, 50 MHz signals can be transferred over distances of 100 feet. For 100 MHz operation, lengths should be 50 feet or less. In the differential mode, *Figures 4-18b, c*, the line receiver can recover smaller signals, allowing 100 MHz signals to be transferred up to 100 feet. The dual cable arrangement of *Figure 4-18c* provides maximum noise immunity. The delay of coaxial cables depends on the type of dielectric material, with typical delays of 1.52 ns/ft for polyethylene and 1.36 ns/ft for cellular polyethylene.



a. Single-Ended Coaxial Transmission



b. Differential Coaxial Transmission



c. Differential Transmission with Grounded Shields

FIGURE 4-18. Coaxial Cable Connections

References

1. Kaupp, H. R., "Characteristics of Microstrip Transmission Lines," *IEEE Transaction on Electronic Computers*, Vol. EC-16 (April, 1967).
2. Harper, C. A., *Handbook of Wiring, Cabling and Interconnections for Electronics*. New York: McGraw-Hill, 1972.
3. True, K. M., "Transmission Line Interface Elements," *The TTL Applications Handbook*, Chapter 14 (August 1973), pp. 14-1-14-14.



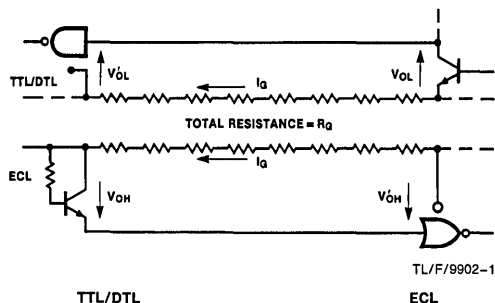
Chapter 5 Power Distribution and Thermal Considerations

Introduction

High-speed circuits generally consume more power than similar low-speed circuits. At the system level, this means that the power supply distribution system must handle the larger current flow; the larger power dissipation places a greater demand on the cooling system. The direct current (DC) voltage drop along ground busses affects noise margins for all types of ECL circuits. Voltage drops along V_{EE} busses have only a slight effect on F100K circuits, but they require consideration to obtain the performance available from the family.

Logic Circuit Ground, V_{CC}

The positive potential V_{CC} and V_{CCA} in ECL circuits is the reference voltage for output voltages and input thresholds and should therefore be the ground potential. When two circuits are connected in a single-ended mode, any difference in ground potentials decreases the noise margins, as discussed in *Chapter 1*. This effect for TTL/DTL circuits, as well as for ECL circuits, is illustrated in *Figure 5-1*. The following analysis assumes some average value of current flowing through the distributed resistance along the ground path between two circuits. For the indicated direction of I_G , the shift in ground potential *decreases* the LOW-state noise margin of the TTL/DTL circuits and the HIGH-state noise margin of the ECL circuits. If I_G is flowing in the opposite direction, it *increases* these noise margins, but *decreases* the noise margins when the drivers are in the opposite state. For tabulation of ground currents in ECL, the designs must include termination currents as well as I_{EE} operating currents. ECL logic boards which use microstrip or stripline techniques generally have large areas of ground metal. This causes the ground resistance to be quite low and thus minimizes noise margin loss between pairs of circuits on the same board.



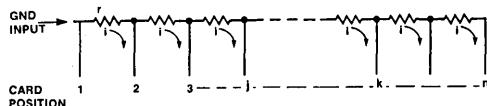
TTL/DTL ECL

$$V'_{OL} = V_{OL} + I_G R_G \qquad V'_{OH} = V_{OH} + I_G R_G$$

$$I_G R_G = (V'_{OL} - V_{OL}) = \text{Noise Margin Decrease} = I_G R_G = (V'_{OH} - V_{OH})$$

FIGURE 5-1. Effect of Ground Resistance on Noise Margins

In practice, two communicating circuits might be located on widely separated PC cards with other PC cards in between. The net resistance then includes the incremental resistance of the ground distribution bus from card to card, while the ground current is successively increased by the contribution from each card. *Figure 5-2* illustrates a distribution bus for a row of cards with incremental resistances along the bus.



r = Incremental Bus Resistance between Positions
 i = Average Ground Current per Card

FIGURE 5-2. Ground Shift Along a Row of PC Cards

The ground shift can be estimated by first determining an average value of current per card based on the number of packages, the mix of SSI and MSI, and the number and types of terminations. With n cards in the row, an average ground current (i) per card, and an incremental bus resistance (r) between card positions, the bus voltage drops between the various positions can be determined as follows:

$$\begin{aligned} \text{between positions 1 and 2: } v_{1-2} &= (n-1)ir \\ \text{between positions 1 and 3: } v_{1-3} &= (n-1)ir + (n-2)ir \\ \text{between positions 1 and 4: } v_{1-4} &= (n-1)ir + (n-2)ir + (n-3)ir \\ \text{between 1 and } n: \quad v_{1-n} &= ir \{ (n-1) + (n-2) + (n-3) + \dots + [n - (n-1)] \} \\ &= ir [1 + 2 + 3 + \dots + (n-1)] \\ v_{1-n} &= ir \sum_{1}^{n-1} n \end{aligned}$$

For a row of 15 cards, for example, the total ground shift between positions 1 and 15 is expressed as in Equation 5-1.

$$\begin{aligned} v_{1-15} &= ir \sum_{1}^{14} n = ir (1 + 2 + 3 + \dots + 13 + 14) \\ &= 105ir \end{aligned} \tag{5-1}$$

Logic Circuit Ground, V_{CC} (Continued)

The ground shift between any two card positions j and k can be determined as follows for the general case.

$$\begin{aligned}
 v_{j-k} &= (n - j) ir + [n - (j + 1)] ir + \\
 &\quad [n - (j + 2)] ir \\
 &\quad + \dots + [n - [j + (k-j-1)]] ir \\
 &= (k - j) nir - ir [j + (j + 1) + (j + 2) \\
 &\quad + \dots + [j + (k-j-1)]] \quad (5-2)
 \end{aligned}$$

$$v_{j-k} = (k - j) nir - ir \sum_j^{k-1} n = ir [(k - j)n - \sum_j^{k-1} n]$$

In a row of 15 cards, the ground shift between positions four and nine, for example, is determined as follows.

$$\begin{aligned}
 v_{j-k} &= ir [(9 - 4)15 - (4 + 5 + 6 + 7 + 8)] \quad (5-3) \\
 &= ir (75 - 30) = 45 ir
 \end{aligned}$$

The ground shift between the same number of positions further down the row is less because of the decreasing current along the row. Consider the ground shift between card positions 10 and 15.

$$\begin{aligned}
 v_{10-15} &= ir [(15 - 10)15 - \\
 &\quad (10 + 11 + 12 + 13 + 14)] \quad (5-4) \\
 &= ir (75 - 60) = 15 ir
 \end{aligned}$$

These examples illustrate several principles the designer should consider regarding the ground distribution bus and assignment of card positions. The bus resistance should be kept as low as possible by making the cross-sectional areas as large as practical. Logic cards which represent the heaviest current drain should be located nearest the end where ground comes into the row of cards. Cards with single-ended logic wiring between them should be assigned to positions as close together as possible. Conversely, if the ground shift between two card positions represents an unacceptable loss of noise margin, then the differential transmission and reception method i.e., twisted pair, should be used for logic wiring between them, thereby eliminating ground shift as a noise margin factor.

Conductor Resistances

Conductors with large cross-sectional areas are required to maintain low voltage drops along power busses. For convenience, *Figure 5-3* lists the resistance per foot and the cross-sectional area for more common sizes of annealed copper wire. Other characteristics and a complete list of sizes can be found in standard wire tables. A useful rule-of-thumb regarding resistances and, hence, areas is: as gauge numbers increase, resistance doubles with every third gauge number; e.g., the resistance per foot of #10 wire is 1 m Ω , for #13 wire it is 2 m Ω . Similarly, the resistance per foot of #0 wire is 0.078 m Ω , which is half that of #2 wire.

For calculations involving conductors having rectangular cross sections, it is often convenient to work with sheet resistance, particularly for power distribution on PC cards. Copper resistivity is usually given in ohm-centimeters, indicating the resistance between opposing faces of a 1 cm cube. The sheet resistance of a conductor is obtained by dividing the resistivity by the conductor thickness. These relationships follow.

| AWG B & S Gauge | Resistance m Ω Per Foot | Cross-Sectional Area Square Inches |
|-----------------|--------------------------------|------------------------------------|
| #2 | 0.156 | 5.213×10^{-2} |
| #6 | 0.395 | 2.062×10^{-2} |
| #10 | 0.999 | 8.155×10^{-3} |
| #12 | 1.588 | 5.129×10^{-3} |
| #18 | 6.385 | 1.276×10^{-3} |
| #22 | 16.14 | 5.046×10^{-4} |
| #26 | 40.81 | 1.996×10^{-4} |
| #30 | 103.2 | 7.894×10^{-5} |

FIGURE 5-3. Resistance and Cross-Sectional Area of Several Sizes of Annealed Copper Wire

Copper resistivity = $\rho = 1.724 \times 10^{-6} \Omega \text{cm} @ 20^\circ \text{C}$

$$\text{Resistance of a conductor} = \rho \frac{l}{A} = \rho \frac{l}{tw}$$

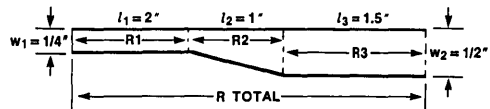
where: l = length t = thickness w = width

$$\text{Sheet resistance } \rho_S = \frac{\rho}{t} \Omega \text{ per } \frac{l}{w}$$

The length/width ratio (l/w) is dimensionless; therefore, the resistance of a length of conductor of uniform thickness can be calculated by first determining the number of "squares," then multiplying by the sheet resistance. For example, a conductor one-eighth inch wide and three inches long has 24 squares; its resistance is 24 times the sheet resistance. Since many thickness dimensions are given in inches, it is convenient to express the resistivity in ohm-inch, as follows.

$$\rho (\Omega \text{in.}) = \rho (\Omega \text{cm}) \div 2.54 = 6.788 \times 10^{-7} \Omega \text{in.}$$

The use of sheet resistance and the "squares" concept is illustrated by calculating the resistance of the conductor shown in *Figure 5-4*. Assume the conductor is a 1 oz. copper cladding with a 0.0012 inch minimum thickness on a PC card.



TL/F/9902-3

FIGURE 5-4. Conductor of Uniform Thickness but Non-Uniform Cross Section

$$\begin{aligned}
 \text{Sheet resistance} &= \rho_S = \frac{\rho}{t} \\
 &= 5.657 \times 10^{-4} \Omega \text{ per square}
 \end{aligned}$$

The number of squares S for the rectangular sections are as follows.

$$S_1 = \frac{l_1}{w_1} = 8 \quad S_3 = \frac{l_3}{w_2} = 3$$

The middle average segment of the conductor has a trapezoidal shape. The average of w_1 and w_2 can be used as the effective width, within 1% accuracy, if the w_2/w_1 ratio is 1.5 or less. Otherwise, a more exact result is obtained as follows.

$$S_2 = \frac{l_2}{w_2 - w_1} \ln \left(\frac{w_2}{w_1} \right) = 4 \ln 2 = 2.77 \text{ squares} \quad (5-5)$$

$$\begin{aligned}
 \text{Total } R &= R_1 + R_2 + R_3 = \rho_S (S_1 + S_2 + S_3) \\
 &= 7.51 \text{ m}\Omega
 \end{aligned}$$

Conductor Resistances (Continued)

As another example, assume that a 1 oz. trace must carry a 200 mA current six inches with a voltage drop less than 10 mV.

$$R_{\max} = \frac{V_{\max}}{I} = \frac{0.01}{0.2} = 0.05\Omega$$

$$0.05 = \rho_s \frac{l}{w} \tag{5-6}$$

$$\frac{w}{l} = 20 \rho_s$$

$$w = 120 \rho_s = (120) 5.657 \times 10^{-4} = 67.9 \times 10^{-3}$$

∴ minimum trace width, $w = 68$ mils

At a higher current level, consider the voltage drop in a conductor 20 mils thick, 1.25 inches wide and 3 feet long carrying a 50A current.

$$\rho_s = \frac{6.788 \times 10^{-7}}{2 \times 10^{-2}} = 3.364 \times 10^{-5} \Omega \text{ per square}$$

$$V = IR = (50) (3.364 \times 10^{-5}) \frac{36}{1.25} \tag{5-7}$$

$$= 0.0484 = 48.4 \text{ mV}$$

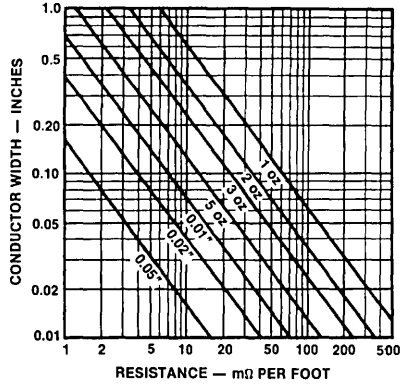
Sheet resistances for various copper thicknesses are listed in Figure 5-5. Standard thicknesses and tolerances for copper cladding are tabulated in Figure 5-6 and resistance per foot as a function of width is shown in Figure 5-7.

| Weight or Thickness | Sheet Resistance Ω per Square | Thickness | Sheet Resistance Ω per Square |
|---------------------|--------------------------------------|--------------------|--------------------------------------|
| 2 oz. | 2.715×10^{-4} | 0.02 in. | 3.364×10^{-5} |
| 3 oz. | 1.886×10^{-4} | 0.05 in. | 1.358×10^{-5} |
| 5 oz. | 1.077×10^{-4} | $\frac{1}{16}$ in. | 1.086×10^{-5} |
| 0.01 in. | 6.788×10^{-5} | $\frac{1}{4}$ in. | 2.715×10^{-6} |

FIGURE 5-5. Sheet Resistance for Various Thicknesses of Copper

| Nominal Thickness | | Nominal Weight oz/ft ² | Tolerances By | |
|-------------------|--------|--------------------------------------|---------------|----------|
| in. | mm | | Weight, % | in. |
| 0.0007 | 0.0178 | $\frac{1}{2}$ | + 10 | + 0.0002 |
| 0.0014 | 0.0355 | | | + 0.0004 |
| 0.0028 | 0.0715 | 2 | + 10 | + 0.0007 |
| | | | | - 0.0003 |
| 0.0042 | 0.1065 | 3 | + 10 | + 0.0006 |
| 0.0056 | 0.1432 | | | + 0.0006 |
| 0.0070 | 0.1780 | 5 | + 10 | + 0.0007 |
| 0.0084 | 0.2130 | | | + 0.0008 |
| 0.0098 | 0.2460 | 7 | + 10 | + 0.001 |
| 0.014 | 0.3530 | | | + 0.0014 |
| 0.0196 | 0.4920 | 14 | + 10 | + 0.002 |

FIGURE 5-6. Thickness and Tolerances for Copper Cladding



TL/F/9902-4

FIGURE 5-7. Conductor Resistance vs Thickness and Width

Temperature Coefficient

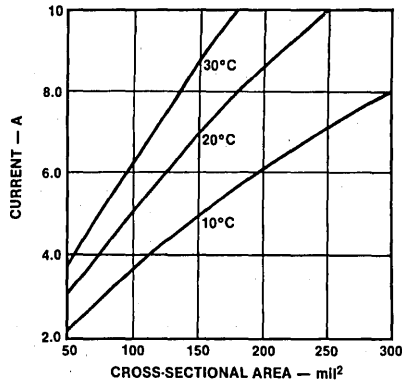
The resistances in Figures 5-3, 5-5, and 5-7, as well as those used in the sample calculations, are 20°C values. Since copper resistivity has a temperature coefficient of approximately 0.4%/°C, the resistance at a temperature (T) can be determined as follows.

$$R_T = R_{20^\circ\text{C}} [1 + 0.004 (T + 20^\circ\text{C})]$$

$$\text{At } 55^\circ\text{C:} \tag{5-8}$$

$$R = R_{20^\circ\text{C}} [1 + 0.004 (55^\circ\text{C} - 20^\circ\text{C})] = 1.14 R_{20^\circ\text{C}}$$

When specifying power bus dimensions for PC cards containing many IC packages, designers should bear in mind that excessive current densities can cause the copper temperature to rise appreciably. Figure 5-8 illustrates the ohmic heating effect of various current densities.¹



TL/F/9902-5

FIGURE 5-8. Temperature Rise with Current Density in PC Board Traces

Distribution Impedance

Power busses should have low AC impedance, as well as low DC resistance, to prevent propagation of extraneous disturbances along the distribution system. As far as current or voltage changes are concerned, power and ground buses appear as transmission lines; thus their impedances can be affected by shape, spacing and dielectric. The effect of geometry on impedance is illustrated in the two arrangements of Figure 5-9. The same cross-sectional area of copper is used, but the two round wires have an impedance of about 75Ω while the flat conductors have an impedance determined as follows.

$$Z_0 = \frac{377 d}{\sqrt{\epsilon} h} \text{ for } \frac{d}{h} < 0.1$$

With a Mylar®* or Teflon®* dielectric ($\epsilon = 2.3$) two miles thick, impedance of the flat conductor pair is only 0.5Ω . Power line impedance can be reduced by periodically connecting RF-type capacitors across the line.

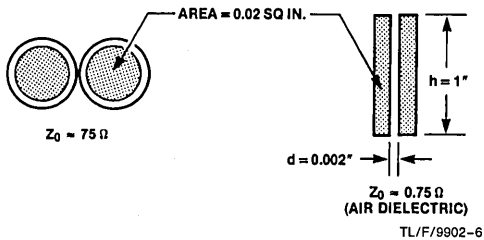


FIGURE 5-9. Effect of Geometry on Power Bus Impedance

*Mylar and Teflon are registered trademarks of E.I. du Pont de Nemours Company.

Ground on PC Cards

It is essential to assign one layer of copper cladding almost exclusively to ground. This provides low-impedance, non-interfering return paths for the current changes which travel along signal traces when the IC outputs change state. These currents flow from the V_{CCA} pins of the IC packages, through the output transistors, then into the loads and the stray capacitances. These stray capacitances exist from an output to V_{EE} , output to ground, and to other signal lines. Thus, displacement currents through stray capacitances flow in many paths, but must ultimately return through ground to the output transistor where they originated. To reduce the length and impedance of the return path, the ground metal should cover as large an area as possible and one decoupling capacitor should be provided for every one to two IC packages. Additional capacitors may be needed for multiple output devices. These capacitors should be ceramic, monolithic or other RF types in the $0.01 \mu\text{F}$ to $0.1 \mu\text{F}$ range.

The load current returning to an IC package through ground metal is predictable, both in magnitude and in the return path. Since the magnetic and capacitive coupling between a signal trace and the underlying ground provides the transmission line characteristic, it follows that the load current flowing through the signal trace is accompanied by a ground return current equal in magnitude but opposite in direction. For example, in a 50Ω terminator I_{OL} is 5.9 mA, I_{OH} is 20.9 mA. Then signal change will cause about 15 mA current change and, as this current change propagates along the signal trace, a current of -15 mA advances along the

ground directly underneath the signal trace. Therefore, if there is an interruption in the ground, the return current is forced to go around it. The 15 mA current change can be reduced by terminating the complementary output of the signal. Then a signal change will direct the current from true output to the complement output reducing the Δ currents in the ground plane. When it is necessary to interrupt the ground plane, the interruptions should be kept as short as possible; every effort should be made to locate them away from overlying signal lines. When the ground plane is interrupted for short signal lines between packages, these lines should be at right angles to signal lines on the other side to minimize coupling. V_{EE} and V_{TT} distribution lines can also act as the return side of transmission lines, as long as decoupling capacitors to ground are placed in the immediate areas where the signal return current must continue through ground.

Several connections along the edge of a PC card should be assigned to ground to accommodate backplane signal ground. These should be spaced at one-half to one inch intervals to minimize the average path length for signal return currents and to simulate a distributed connection to the backplane signal ground.

Not enough emphasis can be placed on the requirement for a good ground. All input signals are referenced to internal V_{BB} and the V_{BB} is referenced to V_{CC} (ground). Any variation from one side of the board to the other affects the noise margins. To help eliminate some of the variations a separate V_{CCA} is provided on F100K ECL circuits to power the output drivers and leave the V_{CC} going to internal circuitry unaffected.

Backplane Construction

In order to take complete advantage of the speeds inherent in F100K ECL it is desirable to construct the backplane as a multilayer printed circuit board. Generally, two internal layers are devoted to ground and V_{EE} and the signals occupy the outside layers. Where power densities are very high, it may be necessary to supplement the power layers with external busses (see Backplane Interconnections, Chapter 4). If it is necessary to use wires to augment the interconnection provided by the traces, less critical signals should use the wires. The wires will exhibit an impedance which can be calculated with the wire-over-ground formula

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \log_{10} \frac{4h}{d} \quad (5-9)$$

where d is diameter, h is distance to ground, and ϵ is dielectric constant.

Bear in mind that if the ground plane is buried inside the board, then both h and ϵ are made up of multiple components.

Termination Supply, V_{TT}

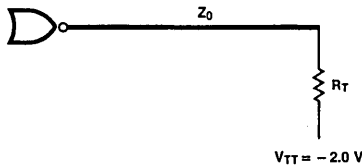
A separate return voltage for the termination resistors offers a way to minimize power dissipation in systems extensively using parallel termination techniques. A $-2V$ V_{TT} value represents an optimum speed/power trade-off, allowing sufficient termination current to discharge load capacitances while minimizing the average power consumption. Figure 5-10 shows the average values of current, IC power dissipation and resistor power dissipation for various values of the termination resistor R_T returned to $-2V$. Average values are determined by calculating the output HIGH and output LOW values, then taking the average. These 50% duty cy-

Termination Supply, V_{TT} (Continued)

cle values are useful in determining the current drain on the $-2V$ supply and the contribution to dissipation on the logic boards. Peak values of termination current are approximately 60% greater than the average values listed.

DC regulation of the $-2V$ supply is not critical; a variation of $\pm 5\%$ causes a change in output levels of ± 12 mV for 50Ω terminations or ± 7 mV for 100Ω terminations.

The high frequency characteristics of the V_{TT} distribution are extremely important. Ideally, a solid voltage plane should be devoted to V_{TT} . If this is not feasible, the V_{TT} distribution should form a grid using orthogonal traces. In any case, decoupling capacitors to ground should be used to reduce the high frequency impedance.



TL/F/9902-7

| R_T Ω | I_{avg} mA | P_D (avg) mW | |
|-------------------|-----------------|----------------|----------|
| | | IC Output | Resistor |
| 50 | 14 | 14 | 13 |
| 62 | 11 | 12 | 11 |
| 75 | 9.3 | 9.5 | 9.1 |
| 90 | 8.1 | 8.2 | 7.9 |
| 100 | 7.3 | 7.3 | 7.1 |
| 150 | 5.0 | 4.9 | 5.0 |

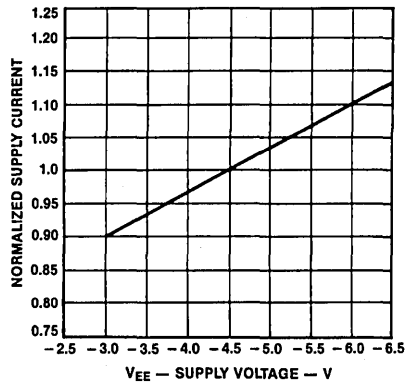
FIGURE 5-10. Average Current and Power Dissipation for Parallel Termination to $-2V$

If the terminators used are in Single In-line Packages (SIP) or Dual-in-line Packages (DIP) as opposed to discrete resistors, particular attention must be given to decoupling in order to maintain a solid V_{TT} voltage inside the package. This is necessary to avoid crosstalk due to mutual inductance to V_{TT} . SIPs have been developed which have multiple V_{TT} connections and on-board decoupling capacitors.

V_{EE} Supply

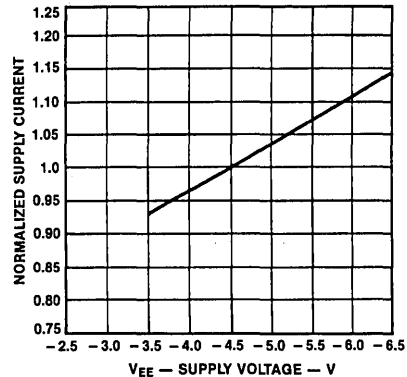
The value of V_{EE} is not critical for F100K since all circuits in the family operate over the range of $-4.2V$ to $-5.7V$. Decoupling capacitors to ground should be used on each card, as previously discussed in connection with the ground on PC cards. In addition, each card should use $1 \mu F$ to $10 \mu F$ decoupling capacitors near the points where V_{EE} enters the card.

The current drain for the V_{EE} supply for each circuit type can be determined from the data sheet specifications. For V_{EE} values other than $-4.5V$, the current drain varies as shown in Figure 5-11 and 5-12 for SSI and MSI elements respectively. These graphs are made from data from the F100101 and F100179.



TL/F/9902-8

FIGURE 5-11. Supply Current vs Supply Voltage for F100101



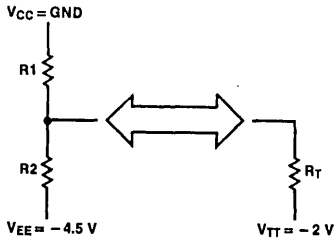
TL/F/9902-9

FIGURE 5-12. Supply Current vs Supply Voltage for F100179

Series dividers used to obtain Thevenin equivalent parallel terminations increase the current load on the V_{EE} supply, as do the pull-down resistors to V_{EE} used with series termination. Average V_{EE} current and resistor dissipation for Thevenin equivalent terminations are listed in Figure 5-13 for several representative values of equivalent resistance. The average values apply for 50% duty cycle. Peak current values are approximately 11% greater. Dissipation in the IC output transistor is the same as in Figure 5-10. Average dissipation and I_{EE} current for several values of pull-down resistance to V_{EE} are listed in Figure 5-14. The R_E values are appropriate for series termination of transmission lines with impedances listed in the Z_0 column, determined from Equation 4-12. Peak current values are approximately 12% greater than average values.

Figures 5-10, 13 and 14 show that the Thevenin equivalent parallel termination method leads to ten times as much dissipation in the resistors as in the single resistor returned to $-2V$. Similarly, the dissipation in R_E for series termination is three times the dissipation in the parallel termination resistor to $-2V$.

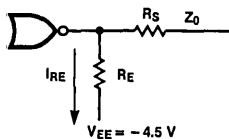
V_{EE} Supply (Continued)



TL/F/9902-10

| R _T Ω | R ₁ Ω = 1.80 R _T | R ₂ Ω = 2.25 R _T | I _{EE} (avg) mA | P _D (avg) mW Resistors |
|---------------------|---|---|-----------------------------|--------------------------------------|
| 50 | 90 | 113 | 28.2 | 109 |
| 62 | 112 | 140 | 22.7 | 87.9 |
| 75 | 135 | 169 | 18.8 | 72.7 |
| 82 | 148 | 185 | 17.2 | 66.5 |
| 90 | 162 | 203 | 15.7 | 60.5 |
| 100 | 180 | 225 | 14.1 | 54.5 |
| 120 | 216 | 270 | 11.7 | 45.4 |
| 150 | 270 | 338 | 9.4 | 36.3 |

FIGURE 5-13. Series Divider for Thevenin Equivalent Terminations



TL/F/9902-11

| Z ₀ Ω | R _E Ω | I _{EE} (avg) mA | P _D (avg) mW | |
|---------------------|---------------------|-----------------------------|-------------------------|----------------|
| | | | IC Output | R _E |
| 50 | 269 | 9.8 | 12.9 | 25.8 |
| 62 | 331 | 7.9 | 10.4 | 20.6 |
| 75 | 399 | 6.5 | 8.6 | 16.8 |
| 90 | 477 | 5.4 | 7.1 | 13.9 |
| 100 | 530 | 4.9 | 6.5 | 12.7 |
| 120 | 634 | 4.1 | 5.4 | 10.6 |
| 150 | 791 | 3.2 | 4.2 | 8.1 |

FIGURE 5-14. Average Current and Power Dissipation Using Pull-Down Resistor to V_{EE}

Thermal Considerations

System cooling requirements for ECL circuits are based on three considerations: (1) the need to minimize temperature gradients between circuits communicating in the single-ended mode, (2) the need to control the temperature environment of each circuit to assure that the parameters stay within guaranteed limits, and (3) the need to insure that the maximum rated junction temperature is not exceeded.

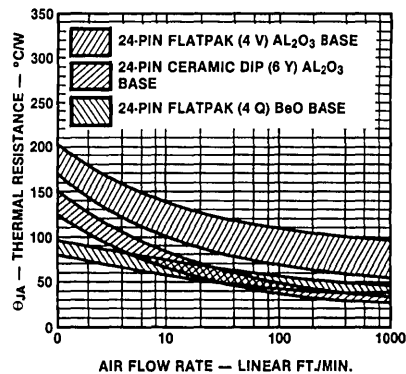
Temperature gradients are of no practical concern with F100K circuits since they are temperature compensated;

their output voltage levels and input thresholds change very little with temperature, as discussed in *Chapter 1*. With uncompensated ECL circuits, output voltage levels and input thresholds vary with temperature. This causes a loss of noise margin when driving and receiving circuits are operating at different temperatures. Loss of HIGH-state noise margin occurs when the receiving circuit is at the higher temperature, amounting to approximately 1 mV/°C of temperature gradient. When the driving circuit is at the higher temperature, the LOW-state margin decreases by approximately 0.5 mV/°C of gradient. The system designer must consider noise margin loss, due to temperature gradients.

Each DC parameter limit on the F100K data sheets applies over the entire 0°C to +85°C case temperature. For uncompensated ECL circuits, parameter limits have different values for different ambient temperatures. Further, ambient temperature specifications are based on a minimum air flow rate of 400 linear feet per minute. Thermal equilibrium must be established for incoming test results of uncompensated ECL circuits to be valid. The time required to attain equilibrium can vary considerably, depending on the internal dissipation of the particular IC type and details of the thermal arrangement. Normally, an adequate waiting time is three to five minutes after power is applied.

The maximum rated junction temperature of F100K circuits is +150°C. An individual IC junction temperature can be determined by multiplying power dissipation by the junction-to-air thermal resistance θ_{JA} and adding the result to the ambient air temperature. The power dissipation is V_{EE} times I_{EE}, from the data sheet, plus the dissipation in the output transistors from *Figure 5-10* or *5-14*. Thermal resistance is shown in *Figure 5-15* as a function of cooling air flow rate. This figure applies when the IC is mounted on a board with the air flowing in a plane parallel to the board and perpendicular to the long axis of the IC package. When air temperature, flow rate and package power dissipation are known, junction temperature is determined as follows.

$$T_J = T_A + P_D \theta_{JA} \quad (5-10)$$



TL/F/9902-12

FIGURE 5-15. Junction-to-Air Thermal Resistance vs Air Flow Rate

Thermal Considerations (Continued)

Conversely, when the maximum rate junction temperature (+150°C), the package power dissipation, and the air temperature are known, the minimum flow rate can be determined by first determining the maximum thermal resistance.

$$\text{Maximum } \theta_{JA} = \frac{(150^\circ - T_A)}{P_D} \quad (5-11)$$

For this value of θ_{JA} the minimum flow rate is determined from *Figure 5-15*.

When the system designer plans to depend on natural convection for cooling, it is recommended that thermal tests be conducted to determine actual conditions. The effectiveness of natural convection for cooling varies greatly. For

instance, on a densely packed logic board in a horizontal attitude in still air, the effective ambient temperature for an IC varies with its position. An IC in the middle of the board is subjected to air that is partially heated by surrounding ICs. Additionally, the temperature of the board rises due to heat flow through the component leads. These effects can cause a much higher junction temperature than might be expected.

Reference

1. Harper, C.A., Editor, *Handbook of Wiring, Cabling and Interconnecting for Electronics*, McGraw-Hill, 1972.

Chapter 6 Testing Techniques

Introduction

The purpose of this chapter is to assist personnel involved with incoming inspection and qualification testing, by discussing the various methods and techniques used in testing ECL devices.

Testing includes verifying functionality, checking DC parametric limits and measuring AC performance. These tasks are particularly difficult for ECL devices in light of the broad range of products: RAMs, PROMs, gate arrays, and logic circuits. Correlation between supplier and user is extremely important. Recognizing the differences between high-volume instantaneous testing, as performed by the supplier, and the user's concern for long term performance in a given operating environment, National guarantees the data sheet limits as specified, although testing may be performed by alternate methods.

Tester Selection

Although many makes and types of automatic test systems are available and in use today, not all are capable of testing ECL RAMs, PROMs, logic and gate arrays.

Logic and gate array testers require DC Accuracy, subnanosecond AC test capability, and the ability to change software for each device. Software capability and the number of test pins available are major considerations in choosing a gate array tester. Functional, DC and threshold tests are successfully performed on automatic test equipment, but subnanosecond propagation delays are difficult to measure accurately.

The use of dedicated testers to perform high-volume memory testing is very common. Testers containing hardware addressing capability are usually the most efficient. Although basic DC testing is similar for any device type, RAM and PROM functional testing usually require special addressing capabilities to test for pattern sensitivity. The pattern generators and output comparators must have minimum skew to obtain maximum tester accuracy. Functional and AC tests are performed simultaneously; then, DC and threshold tests are performed.

The following considerations must be taken into account when selecting a tester.

Noise

Since the voltage swing on ECL input and output levels is only about 800 mV, it is very important that the power supplies and voltage drivers be extremely clean and free of spikes, hum, or any other type of noise.

DC Resolution

The threshold measurements ($V_{IH (Min)}$, $V_{IL (Max)}$) require that input voltage be extremely accurate and repeatable,

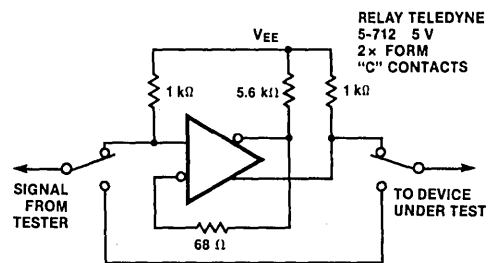
i.e., if the $V_{IL (Max)}$ is specified as $-1.475V$, a voltage source of $-1.475 \pm 5 \text{ mV}$ is not adequate to accurately test the part. Ideally, the driver and the output comparators should have an accuracy of $\pm 1 \text{ mV}$.

Current Capability

Since ECL is noted for high current requirements, power supplies for V_{EE} should be capable of supplying current with a 25% reserve over the highest powered parts. This reserve should be included because power supplies tend to get noisy when approaching the current clamp. Some ECL LSI parts dissipate over 4.5W; therefore, with a V_{EE} of $-4.5V$, the power supply must provide well over 1A.

Edge Rates

When testing edge-triggered sequential logic parts such as flip-flops and shift registers, it is important that the rise and fall times of the clock pulses be fast, clean and free from overshoot. If the clock edges are not adequate, the deficiency can be overcome using a Schmitt trigger as shown in *Figure 6-1*.



TL/F/9903-1

FIGURE 6-1. Typical Schmitt Trigger Circuit

The 68Ω resistor provides hysteresis by positive feedback, thus improving the edge rates. When energized, the relay provides a path to bypass the Schmitt trigger, so the input currents of the device under test can be measured.

Functional Testing

The functional operation and truth table for all device types are checked using automatic test equipment. For memory devices, pattern sensitivity and AC characteristics are also tested automatically. Functional testing is usually performed before DC testing. Logic parts are functionally tested in all modes of operation. The inputs are driven using typical V_{IH} and V_{IL} values. The outputs are compared against relaxed V_{OH} and V_{OL} limits. The V_{IH} , V_{IL} , V_{OH} and V_{OL} limits are tested during DC testing.

DC Testing

An automatic tester is used to test all DC parameters listed on the individual data sheet for each input and output. The device may have to be preconditioned to obtain the correct output logic state. The cable length should be kept to a minimum to insure signal integrity.

Threshold Measurements

Threshold measurement on an automatic tester is probably the most difficult DC test and the test most prone to oscillation. When testing, take one input at a time to threshold; all other inputs remain at full V_{IH} or V_{IL} levels. For example, to test a flip-flop, make sure the output is LOW before test, take the data pin to HIGH threshold, and apply the clock pulse. Verify that the HIGH has been transferred to the output. Next, apply LOW threshold to the data input and clock it through; use hard levels on the clock (full V_{IH} and V_{IL}). Check that the output pin goes LOW.

Bench Testing

Occasionally, it is necessary to obtain data not easily available from an automatic tester. This is accomplished by testing devices in a universal test board. The typical test circuit board is double-clad copper. All input/output pins go to single-pole, triple-throw switches so that V_{IH} , V_{IL} or a 50Ω terminating resistor can be connected. Leadless $0.05\mu\text{F}$ capacitors decouple all pins to V_{CC} (+2V) at the socket pins. Access to the device under test is made via banana sockets to the X-Y plotter.

V_{IH}/V_{OUT} Plot—The input ramp supply is 0V to -2V varied by a multi-turn potentiometer. The input voltage (V_{IN}) versus output voltage (V_{OUT}) is plotted on an X-Y recorder using the test setup shown in Figure 6-2.

V_{OUT}/I_{OUT} Plot—The output voltage (V_{OUT}) versus output current (I_{OUT}) can be plotted using the test setup shown in Figure 6-3.

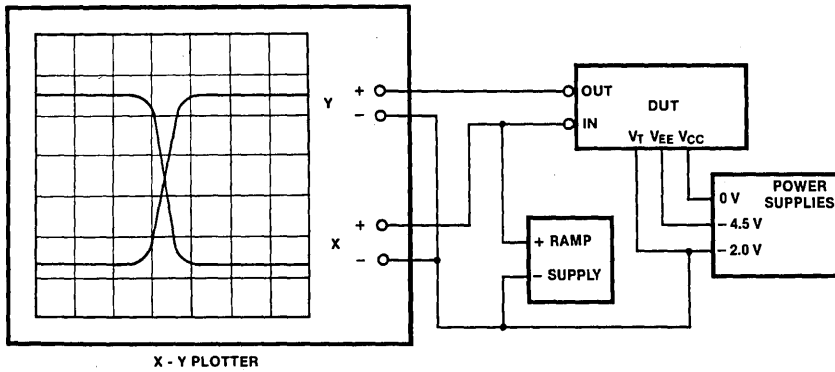


FIGURE 6-2. V_{IN}/V_{OUT} Transfer Characteristics

TL/F/9903-2

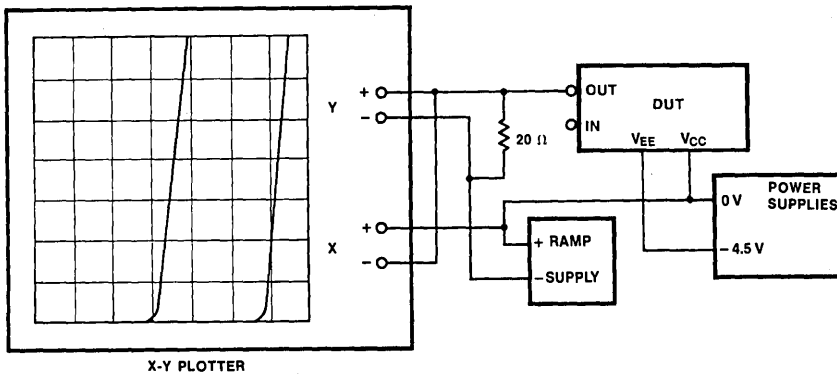


FIGURE 6-3. V_{OUT}/I_{OUT} Characteristics

TL/F/9903-3

AC Testing

Because few automatic measurements systems have sufficient accuracy to perform subnanosecond testing, AC testing of ECL is one of the most difficult tests to accomplish. To obtain subnanosecond accuracy usually requires special test fixtures and equipment. The physical location of the test fixture, the input driver and the output comparator is very important.

Depending upon the accuracy and repeatability of the automatic tester, a bench setup may be required for correlation. Comparing an air line with known propagation delay to the test setup is recommended.

AC Test Fixtures

Test fixture design plays a pivotal role in insuring that undistorted waveforms are applied to the Device Under Test (D.U.T.) and that the device output can be monitored correctly.

Board Construction and Layout

ECL AC bench test fixtures are built on a double-clad printed circuit board or on a multilayer printed circuit board with semi-rigid coax. The power planes are shorted at the device and brought out to banana sockets with the decoupling capacitors at the device. Transmission lines of 50Ω are maintained from soldered-on BNC or SMA connectors to the D.U.T. Sense lines from the D.U.T. output and input pins to the connectors must be of electrically equal length. For input pins, care must be taken to insure that the force and sense lines are brought directly to the point that makes contact with the D.U.T. For output pins, only the output sense lines are used to monitor the signals. The force lines are disconnected at the device to minimize signal distortion. Special care must be taken to minimize crosstalk and stray capacitance in the area of the D.U.T. For correlation, flat-paks are not tested in sockets but are clamped to the traces of a multilayer PC board. Dual in-line devices are plugged into individual pin sockets instead of normal test sockets. Due to equipment limitations and for correlation, the amplitude, offset, rise and fall time are set up with no device in the test socket.

The bench test fixture to measure toggle frequency utilizes the principles described in the preceding paragraph except that the feedback path between the output and data input is as short as possible.

Output Termination

All outputs should be terminated with $50\Omega \pm 1\%$ resistors. This is especially important for complementary outputs.

When bench testing, the device is offset by $+2V$; V_{EE} is $-2.5V$; V_{CC} , V_{CCA} is $+2V$. Then the 50Ω input impedance of the sampling oscilloscope acts as the termination resistor to $0V$. The input and output coaxial cable to the oscilloscope should be cut to exactly the same electrical length.

Decoupling

Not enough emphasis can be put on the importance of good decoupling on the D.U.T. because oscillations can give erroneous test results. A sampling scope should be used to make sure that oscillation is not occurring.

The value of capacitors used depends on the type of tester used and the frequency of test. Some testers use pulse test; in other words, for each individual test in a program, V_{EE} is powered up and down. On this type of tester, electrolytic-type (i.e., large value) capacitors cannot be used because of the time constant needed to charge the capacitor.

Always start with the minimum decoupling needed to achieve good results, perhaps merely a capacitor between V_{CC} and V_{EE} . Capacitors should be placed as close as possible to the D.U.T. to eliminate as much inductance as possible. Only low-inductance capacitors should be used; leadless monolithic ceramic capacitors are very effective.

There are no rigid decoupling rules, and each device type may have its own decoupling requirements. A typical decoupling technique that works well on most F100K devices is to place $0.01 \mu F$ to $0.1 \mu F$ monolithic ceramic capacitors in the following locations.

- If no offset is used:
 - between V_{EE} ($-4.5V$) and V_{CC} , V_{CCA} ($0V$)
 - between V_{TT} ($-2V$) and ground ($0V$)
- If $+2V$ offset is used:
 - between V_{CC} , V_{CCA} ($+2V$) and ground ($0V$)
 - between V_{EE} ($-2.5V$) and ground ($0V$)
- In most cases, V_{CCA} and V_{CC} should be shorted as close to the D.U.T. as possible. However, if the V_{CCA} and V_{CC} pins are physically separated, individual decoupling capacitors may be necessary.
- For DC test only place a $0.001 \mu F$ capacitor:
 - between an input pin and V_{EE}
 - between an output pin and V_{CCA}

Decoupling problems will appear mainly at threshold test. If certain outputs fail, try the decoupling technique, described in the preceding paragraph, on those outputs and the associated inputs. With testers that use the power-hold method, such as the Sentry®, large electrolytics can be used in parallel with smaller ($0.01 \mu F$) disk capacitors for the high-frequency bypass.

ELECTROSTATIC DISCHARGE

Introduction

The study of ESD failures began in earnest back when system designers, faced with very expensive assembly and post-assembly rework, began investigating system failures in great detail. In the course of their study, they checked all the records to determine which devices has passed earlier testing, but had failed once in the system. The data clearly indicated that something in the handling process resulted in higher attrition rates among the devices. Reliability physicists examined the failed devices in minute detail, in some cases subjecting them to examination under high powered scanning electron microscopes.

The problem was found to be one of electrical overstress, and further investigation determined that the cause of the overstress was a phenomenon called electrostatic discharge (or ESD).

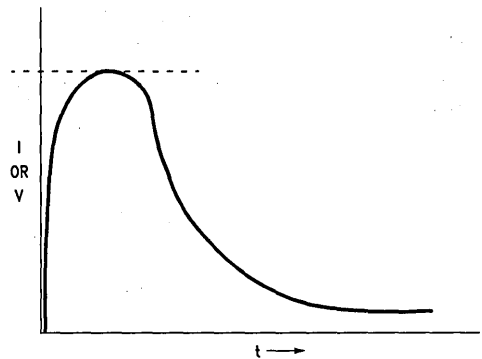
Explanation of How ESD Occurs

The concept of electrostatic discharge is easily understood. Electrostatic energy is static electricity, a stationary charge which can build up in either a nonconductive material or in an ungrounded conductive material. This charge can occur in one of two ways, either through polarization, which occurs when a conductive material is exposed to a magnetic field, or triboelectric effects, which occur when two surfaces contact and then separate, leaving one positively charged and one negatively charged. Friction between two materials increases triboelectric charge by increasing the surface area that comes in contact. A good example of this phenomenon would be the charge one accumulates walking across a nylon carpet. The discharge occurs when one reaches for a doorknob or other conductive surface. The types of ESD with which we will be concerned fall into the category of triboelectric effects. Within this category, various materials have differing potentials for charge. Asbestos, nylon, human and animal hair and wool have a high positive triboelectric potential. Silicon has one of the highest negative triboelectric potentials, followed by such materials as polyurethane, polyester and rayon. Cotton, wood, steel and paper all tend to be relatively neutral, which makes cotton clothing and steel table tops excellent ESD protective materials in environments where ESD problems can be anticipated.

The intensity of the charge is inversely proportional to the relative humidity. As humidity decreases, ESD problems increase. For example, walking across a carpet will generate a 1.5 kV charge at 90%RH, but will generate 35 kV at 10%RH. When an object storing a static charge comes in

contact with another object, the charge will attempt to find a path to ground, discharging into the contacted object. Although the current level is extremely low (typically less than 0.1 nanoamp), the voltage can be as high as 35-50 kV.

The degree of damage caused by electrostatic discharge is a function of the size of the charge (which is determined by the capacitance of the charged object) and the rate at which it is discharged (determined by the resistance into which it is discharged). This relationship can be shown with a waveform (*Figure 1*) that utilizes what is termed a double exponential decay pulse. With such a pulse, 99% of the energy will be dissipated in five time constants, with each time constant established by the resistance and capacitance mentioned above. Where both are low, the discharge rate will be rapid enough to cause damage if the object into which discharge occurs is a semiconductor. As resistance and capacitance increase, both the discharge rate and the risk of damage decrease.



TL/F/9903-6

FIGURE 1. Ideal RC Waveform

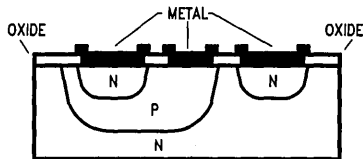
It is estimated that the value of devices lost to ESD could run as high as \$1 billion per year. Most electrostatic damage is caused by the handling of devices by personnel who have not taken adequate precautions. One would expect this in light of the fact that the capacitance of the human body ranges from 50 to 200 pF. The ESD characteristics of work surfaces and of materials passing through the area should not be ignored, however, in an attempt to concentrate on the human effect.

Types of ESD Damage

The damage caused by ESD results from the charge's tendency to seek the shortest path to ground, overstressing any electrical interfaces in that path. There are several different types of damage that result, and each of these tends to be typical of specific component technologies and elements.

Dielectric Breakdown

Dielectric breakdown occurs when the voltage across an oxide exceeds its dielectric breakdown strength. The single most important factor in this breakdown is the oxide thickness (Figure 2). Thinner oxide is more susceptible to electrostatic punch-through, which leaves a permanent low-resistance short through the oxide. Where there are pin holes or other weaknesses in the oxide, damage will be possible at lower charge levels. It should be noted that semiconductor manufacturers have reduced oxide thicknesses as they have reduced the overall size of the devices. ESD sensitivity has therefore increased dramatically.



TL/F/9903-7

FIGURE 2. Bipolar Transistor

Electrostatic charge which does not actually result in a breakdown can cause lattice damage in the oxide, lowering its ability to withstand subsequent ESD exposure. A weakened lattice will also have a lower breakdown threshold voltage, and this mechanism is voltage dependent.

Thermal Secondary Breakdown or Junction Burnout

Junction burnout is a significant failure mechanism for bipolar devices, and tends to be power dependent rather than voltage dependent. The interface (or junction) between a P-type diffusion and an N-type diffusion normally has a positive temperature coefficient at low temperatures (that is, increased temperature will result in increased resistance). When a reverse-biased pulse is applied, the junction dissipates heat in its very narrow depletion region, and the temperature increases rapidly. If enough energy is applied, the temperature of the junction will reach a point at which the temperature coefficient of the silicon will turn negative (that is, at which increased temperature will result in decreased resistance). Since the area of the junction is not uniform, hot spots occur. When the melting temperature of silicon (1415°C) is reached as a result of the ensuing thermal runaway condition, junction melting occurs in the localized area. If there is an additional energy available after the initiation of melt, the hot spot can grow into a filament short. The longer the pulse, the wider the resultant filament short.

After the occurrence of the transient, the silicon will resolidify. In a relatively short pulse, a hot spot may form, but not grow completely across the junction. As a result, the damage may not manifest itself immediately as a junction short but will appear at a later time as a result of electromigration. Shrinking geometries will decrease junction areas, and this should increase the susceptibility of these devices to ESD related junction problems.

Metallization Melt

Semiconductor interconnect metallization typically has a small cross-sectional area and limited current carrying capability. As feature sizes continue to be reduced, metallization cross-section will be reduced as well. Reducing metallization line width by half and metallization thickness by half reduces the current carrying capability of that metallization stripe by 75%. Metallization melt, which is a power-dependent failure mechanism, is more likely to occur during short duration, high current pulses, since the only available heat sink (the bonding pad) is nearby and the heat dissipated in the metallization does not have time to flow into the surrounding areas. It can also occur as a side effect during junction melt.

Latent Failures

Immediate failure resulting from ESD exposure is easily determined: the device no longer works. A failed device may be removed from the lot or from the subassembly in which it is installed, and it represents no further reliability risk to the system. There are, however, devices which have been exposed to ESD but which have not immediately failed. Unfortunately, there has never been sufficient data dealing with the long-term reliability of devices which have survived ESD exposure, although some experts feel that two to five devices are degraded for every one that fails. It should be obvious from an examination of the failure mechanisms described above that there can be significant degradation without immediate failure. Damage can manifest itself in either a shortening of the device's lifetime (a possible cause for many of the infant mortality failures seen during burn-in) or in electrical performance shifts, many of which cause the device to fail electrical test limits.

ESD Protective Measures

It should be obvious then that there are three principal considerations when dealing with ESD. The first is that the device should be designed in a manner that minimizes ESD sensitivity and incorporates some ESD protective features. The second is that both manufacturers and users must understand the ESD susceptibility of the devices with which they are dealing. Thirdly, both user and manufacturer must understand the generation of and sources of ESD charges well enough to establish proper precautions throughout their plants.

Device Design

The continuing development of faster and more complex ICs makes it unlikely that we will see a return to thicker oxide layers or larger junctions. Early ICs used fairly simple clamping diodes on the inputs to protect them against voltage transients in the system. Similar, but more complex protective networks can be employed to provide ESD protection. An example of such circuitry is shown in Figure 3 as it is employed in the design of the F100K 300 Series family. Electrostatic discharge (ESD) protection diodes were added to all 300 Series designs specifically in the circuit paths that were most prone to ESD damage on F100K 100 Series products: input-to-V_{CC}, input-to-V_{EE}, and output-to-V_{CC}.

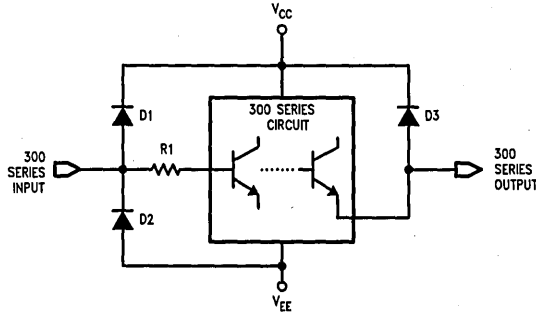


FIGURE 3. 300 Series ESD Protection Circuitry

TL/F/9903-9

These diodes (D1, D2 and D3) are utilized to shunt the current caused by an ESD voltage pulse away from either the input or output circuitry. Depending on the polarity of the ESD voltage, the diodes either become forward-biased, directing the current into the supply, or go into reverse breakdown, directing the current into the substrate. Either way the ESD-caused current is shunted away from the input and output transistors, avoiding damage to the circuitry. The diodes are designed to be rugged enough to guarantee 2000V of ESD protection on all 300 Series products (they typically withstand up to 4000V). Even in providing this protection level, these diodes have a negligible impact on input capacitance. Addition of these diodes typically adds only tenths of picofarads to each product's input capacitance.

Assessing ESD Tolerance Levels

As awareness of the importance of addressing ESD concerns spread, many experts felt that ESD testing had to be uniform if results were to be shared. Method 3015 of MIL-STD-883 was created for the purpose of allowing manufacturers to assess the ESD tolerance levels of the devices they offered and to allow users to determine the ESD sensitivity of the parts with which they were assembling systems. Method 3015 has established a test circuit (see Figure 4) which approximates the resistance and capacitance found in the human body (which continues to provide the major source of destructive ESD). The testing is performed by charging the capacitor in the test circuit and then discharging that capacitor into the unit under test. After testing, a device will be classified as either Class 1, those devices which exhibit ESD-induced failure or degradation at levels between zero volts and 1,999V; or Class 2, those which may exhibit ESD sensitivity at levels between 2,000V and 3,999V; or Class 3, those devices which may exhibit ESD sensitivity at levels above 4,000V but have passed all testing up to that level. This testing is performed on a sample basis at initial device qualification and need not be repeated unless the device is redesigned. The testing is considered destructive, even for those devices which do not fail.

A device may be characterized as Class 1 in lieu of testing at a manufacturer's discretion. Some manufacturers, concerned with the possibility of latent damage due to inadequate protection of devices which test as Class 2, and concerned that static charges resulting from handling can run as high as 50 kV, have elected to treat all of their devices as Class 1, thus ensuring that consistent implementation of common handling procedures will provide maximum protection for all devices.

Data generated by an RADC study of electrostatic discharge susceptibility (VZAP-1, Spring 1983) would seem to support that kind of a conservative approach. The data (see Figure 5) shows the point at which failure first occurred for a given device. It indicates that there are a number of devices which can be expected to fail between 2 kV and 5 kV, but few that will survive beyond 10 kV.

Those devices which are classified as Class 1 must be marked with one equilateral triangle, and those classified as Class 2 must be marked with two equilateral triangles to identify them as static sensitive. (Class 3 devices will have no top mark designator.)

TABLE I. Device ESD Failure Threshold Classification

| MIL Class | ESD Tolerance | Top Mark Designation |
|-----------|------------------|--------------------------|
| Class 1 | 0V to 1,999V | One triangle (i.e., ▲) |
| Class 2 | 2,000V to 3,995V | Two triangles (i.e., ▲▲) |
| Class 3 | 4,000V and above | No mark |

ESD Precautionary Measures

ESD protective measures fall into two categories: those which shield the device from ESD and those which control the occurrence of ESD. ESD shielding can be accomplished by either grounding all of the device leads together, thus providing a more direct path to ground, or by surrounding the device with insulating material that would keep ESD from reaching the device. The first method is most practical during device assembly and environmental test, the second during shipment and storage. However, neither can be utilized during electrical testing.

Most of the handling of ICs, however, occurs during electrical testing. Testing cannot be performed if the device's leads are shorted together, nor can it take place if the device is within an insulated container. Control of ESD during testing is therefore extremely important. This is accomplished through the grounding of all potential sources of ESD. Stainless steel work surfaces connected to ground

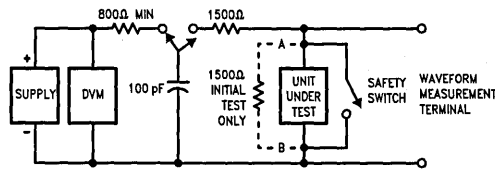


FIGURE 4. ESD Test Circuit

TL/F/9903-8

through an appropriate resistive element provide a harmless bleed-off of any charge that occurs. Requiring that all personnel who handle devices wear ground straps can effectively eliminate the human body and its clothing as sources of ESD. It is also important to minimize the handling of devices. This can be partially accomplished through the use of automated test handlers, which allow the devices to be loaded into the testers from ESD-protective rails and returned to those rails from the tester. Equally important is the elimination of any unnecessary testing or test insertions. Semiconductor manufacturers have decreased the number of test insertions for many devices by combining parametric, functional and switching tests onto a single insertion test program. Users have minimized handling by relying more heavily on the testing performed by their vendors and by eliminating incoming testing. Pick-and-place systems and other automated board assembly hardware have also helped to minimize device handling. Most systems manufacturers have also implemented procedures that minimize the handling of boards and subassemblies in order to ensure that devices receive no potentially damaging exposure to ESD after board assembly.

Effective control of ESD, however, cannot be accomplished unless the entire work area is designed around ESD concerns. At the National Mil/Aero facilities, all work areas in which parts may be handled or through which parts may pass have ESD-protective flooring in addition to grounded work surfaces, ground straps for all operators, and other protective features. This level of attention to detail is essential to the minimization of ESD problems.

Summary

Electrostatic discharge will continue to be a major concern for those who use semiconductor devices. As device geometries continue to shrink, the ESD sensitivity of devices will increase. Only through proper handling and packaging, and through proper attention to ESD concerns will we be able to ensure that long term reliability of key systems is not negatively affected by ESD problems.

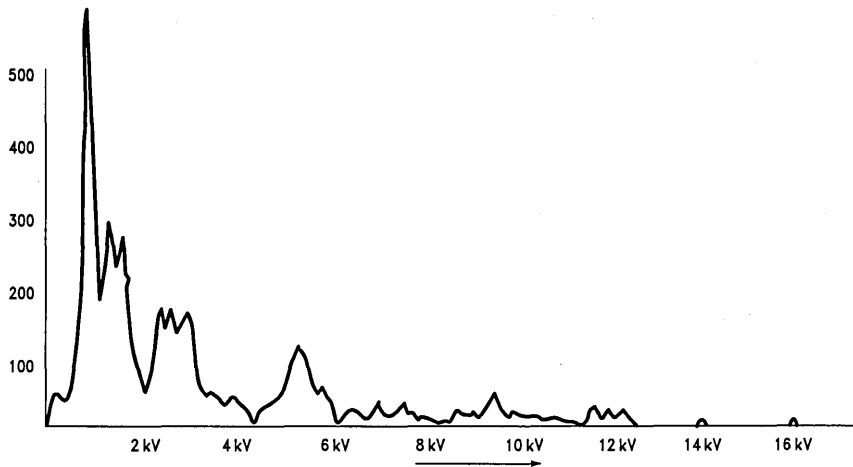


FIGURE 5. Failure Rate at Ascending ESD Voltages

TL/F/9903-10



Chapter 7

Quality Assurance and Reliability

Introduction

F100K ECL is manufactured to strict quality and reliability standards. Product conformance to these standards is insured by careful monitoring of the following functions: (1) incoming quality inspection, (2) process quality control, (3) quality assurance, and (4) reliability.

Incoming Quality Inspection

Purchased piece parts and raw materials must conform to purchase specifications. Major monitoring programs are the inspection of package piece parts, inspection of raw silicon wafers, and inspection of bulk chemicals and materials. Two other important functions of incoming quality inspection are to provide real-time feedback to vendors and in-house engineering, and to define and initiate quality improvement programs.

Package Piece Parts Inspection

Each shipment of package piece parts is inspected and accepted or rejected based on AQL sampling plans. Inspection tests include both inherent characteristics and functional use tests. Inherent characteristics include physical dimensions, color, plating quality, material purity, and material density. Functional use tests for various package piece parts include die attach, bond pull, seal, lid torque, salt atmosphere, lead fatigue, solderability, and mechanical strength. In these tests, the piece parts are sent through process steps that simulate package assembly. The units are then destructively tested to determine whether or not they meet the required quality and reliability levels.

Silicon Wafer Inspection

Each shipment of raw silicon wafers is accepted or rejected based on AQL sampling plans. Raw silicon wafers are subjected to non-destructive and destructive tests. Included in the testing are flatness, physical dimensions, resistivity, oxygen and carbon content, and defect densities. The test results are used to accept or reject the lot.

Bulk Chemical and Material Inspection

Bulk chemicals and materials play an important role in any semiconductor process. To insure that the bulk chemicals and materials used in processing F100K wafers are the highest quality, they are stringently tested for trace impurities and particulate or organic contamination. Mixtures are also analyzed to verify their chemical make-up.

Incoming inspection is only the first step in determining the acceptability of bulk chemicals and materials. After acceptance, detailed documentation is maintained to correlate process results to various vendors and to any variations found in mixture consistency.

Process Quality Control

Process quality is maintained by establishing and maintaining effective controls for monitoring the wafer fabrication process, reporting the results of the monitors, and initiating valid measurement techniques for improving quality and reliability levels.

Methods of Control

The process quality control program utilizes the following methods of control: (1) process audits, (2) environmental monitors, (3) process monitors, (4) lot acceptance inspections, (5) process qualifications, and (6) process integrity audits. These methods of control, defined below, characterize visually and electrically the wafer fabrication operation.

Process Audit—Audits concerning manufacturing operator conformance to specification. These are performed on all operations critical to product quality and reliability.

Environmental Monitor—Monitors concerning the process environment, i.e., water purity, air temperature/humidity, and particulate count.

Process Monitor—Periodic inspection at designated process steps for verification of manufacturing inspection and maintenance of process average. These inspections provide both attribute and variables data.

Lot Acceptance—Lot by lot sampling. This sampling method is reserved for those operations deemed as critical and, as such, requiring special attention.

Process Qualification—Complete distributional analysis is run to specified tolerance averages and standard deviations. These qualifications are typically conducted on deposition and evaporation processes, i.e., epi, aluminum, vapox, and backside gold.

Process Integrity Audit—Special audits conducted on oxidation and metal evaporation processes (CV drift—oxidation; SEM evaluation—metal evaporation).

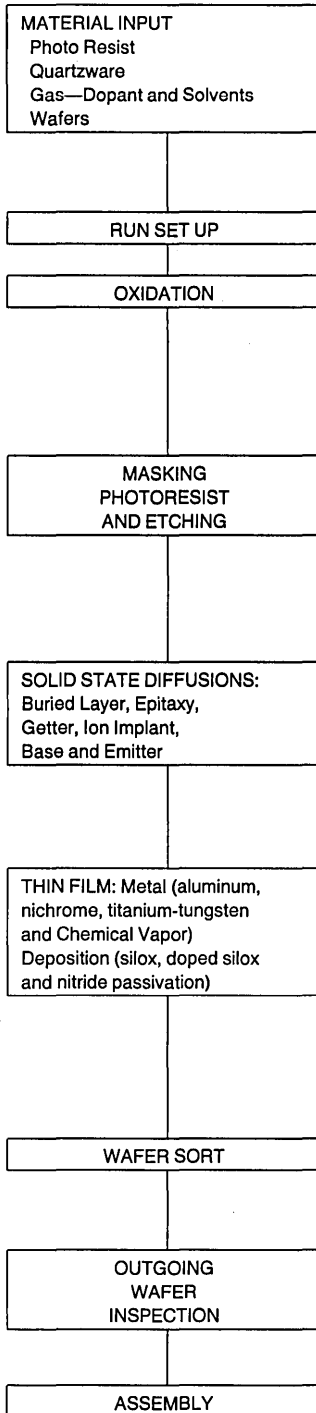
Data Reporting

Process quality control data is recorded on an attribute or variable basis as required; control charts are maintained on a regular basis. This data is reviewed at periodic intervals and serves as the basis for judging the acceptability of specific processes. Summary data from the various process quality control operations are relayed to cognizant line, engineering and management personnel in real time so that, if appropriate, the necessary corrective actions can be immediately taken.

Process Flow

Figure 7-1 shows the integration of the various methods of control into the wafer fabrication process flow. The process flow chart contains examples of the process quality controls and inspections utilized in the manufacturing operation.

Process Quality Control (Continued)



Process Controls (Examples)

- A. Environmental
- B. Chemical supplies
- C. Substrate examination (resistivity, flatness, thickness, crystal perfection, etc.)
- D. Photoresist evaluation
- E. Mask inspections

- A. Process audit

- A. Process audit/qualification
- B. Environmental
- C. Process monitors (thickness, pinhole and crack measurements)
- D. C V Plotting
- E. Calibration

- A. Process audits
- B. Environmental
- C. Visual examinations
- D. Photoresist evaluation (preparation, storage, application, baking, development and removal)
- E. Etchant controls
- F. Exposure controls (intensity, uniformity)

- A. Process audits/qualification
- B. Environmental
- C. Temperature profiling
- D. Quartz cleaning
- E. Calibration
- F. Electrical tests (resistivity, breakdown voltages, etc.)

- A. Process audits/qualification
- B. Environmental
- C. Visual examinations
- D. Epitaxy controls (thickness, resistivity cleaning, visual examination)
- E. Metallization controls (thickness, temperature cleaning, SEM, C V plotting)
- F. Glassivation controls (thickness, dopant concentration, pinhole and crack measurements)

- A. Process audit
- B. Environmental
- C. Visual examinations

- A. Process audit
- B. Inspection

FIGURE 7-1. Process Flow Chart

Quality Assurance

To assure that all product shipped meets both internal National specifications for standard product and customer specifications in the case of negotiated specs, a number of QA inspections throughout the assembly process flow (Figure 7-2) are required. A flow, much more detailed than the one presented in Figure 7-2, governs the assembly of the devices and the performance of the environmental, mechanical and electrical tests.

Reliability

A number of programs, among them qualification testing, reliability monitoring, failure analysis, and reliability data collection and presentation, are maintained.

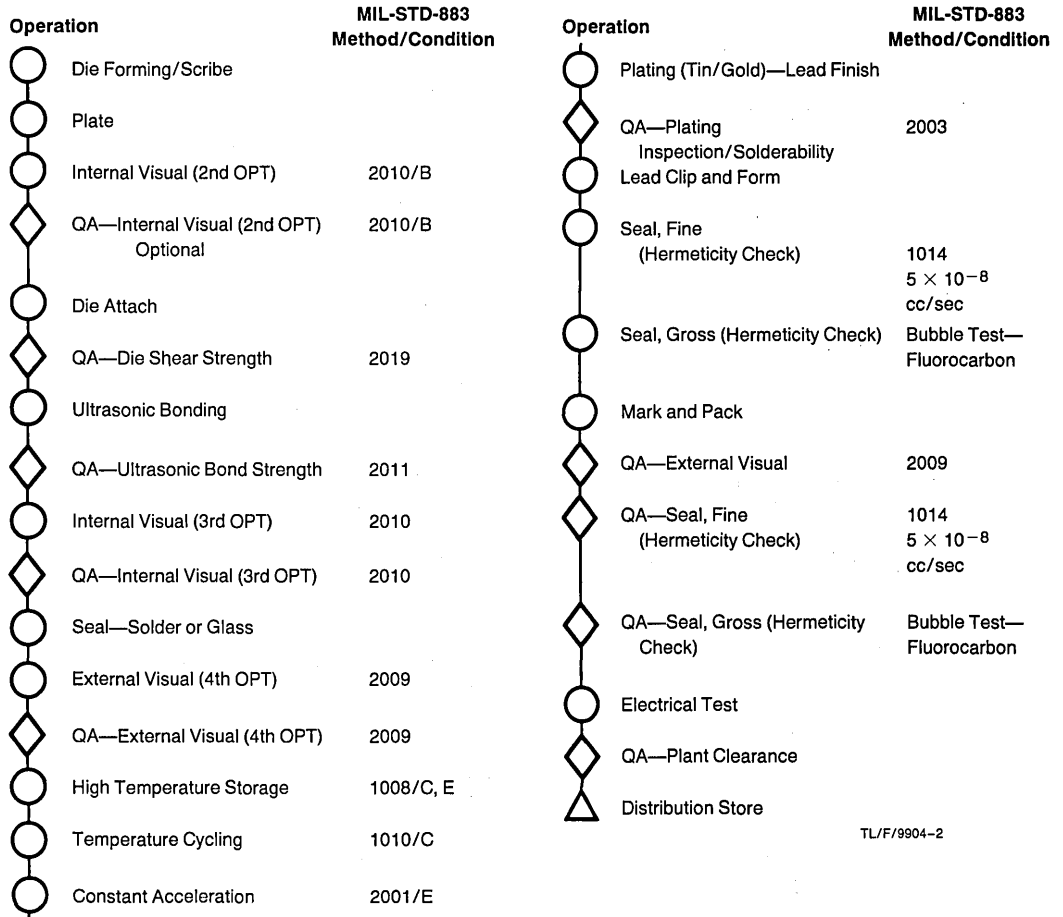
Qualification Programs

All products receive reliability qualification prior to the product being released for shipment. Qualification is required for (1) new product designs, (2) new fabrication processes or

(3) new packages or assembly processes. Stress tests are run and the results are evaluated against existing reliability levels. These results must be better than or equal to current product for the new product to receive qualification.

New Product Designs—Receive, as a minimum, +125°C operating life tests. Readouts are normally scheduled at 168 hours, 1168 hours and 2168 hours. The samples stressed are electrically good units from initial wafer runs. Additional life testing, consisting of high-temperature operating life test, 85/85 humidity bias tests and bias pressure pot (BPTH) tests, may be run as deemed necessary. Redesigns of existing device layouts are considered to be new product designs, and full qualification is necessary.

New Fabrication Processes—Qualifications are designed to evaluate the new process against the current process. Stress tests consist of operating life test, high-temperature operating life test, 85/85 humidity bias test and/or biased



TL/F/9904-1

FIGURE 7-2. Generalized Process Flow

TL/F/9904-2

Reliability (Continued)

pressure pot (BPTH) test. In addition, package environment tests may be performed. Evaluations are performed on various products throughout the development stages of the new process. Units stressed are generally from split wafer runs. All processing is performed as a single wafer lot up to the new process steps, where the lot is split for the new and the current process steps. Then the wafers are recombined, and again processed as a single wafer lot. This allows for controlled evaluation of the new process against the standard process. Both significant modifications to existing process and transferring existing products to new fabrication plants are treated as a new process.

New Packages or Assembly Processes—Qualifications are performed for new package designs, changes to existing piece parts, changes in piece part vendors, and significant modification to assembly process methods. In general, samples from three assembly runs are stressed to a matrix shown in Table 7-1. In addition, +100°C operating life tests, 85/85 humidity bias tests, biased pressure pot (BPTH) tests and unbiased pressure pot tests are performed.

Reliability Monitors

Reliability testing of mature products is performed to establish device failure rates, and to identify problems occurring in production. Samples are obtained on a regular basis from production. These units are stressed with operating life tests or package environmental tests. The results of these tests are summarized and reported on a monthly basis. When a problem is identified, the respective engineering group is notified, and production is stopped until corrective action is taken.

Current testing levels are in excess of 14,000 units per year stressed with operating life tests, and 23,000 units per year stressed with package environmental tests.

Failure Analysis

Failure analysis is performed on all units failing reliability stress tests. Failure analysis is offered as a service to support manufacturing and engineering, and to support customer returns and customer requested failure studies. The failure analysis procedure used has been established to provide a technique of sequential analysis. This technique is based on the premise that each step of analysis will provide information of the failure without destroying information to be obtained from subsequent steps. The ultimate purpose is to uncover all underlying failure mechanisms through complete, in-depth, defect analysis. The procedure places great emphasis on electrical analysis, both external before decapsulation, and internal micro-probing. Visual examinations with high magnification microscopes or SEM analysis are used to confirm failure mechanisms. Results of the failure analysis are recorded and, if abnormalities are found, reported to engineering and/or manufacturing.

Data Collection and Presentation

Product reliability is controlled by first stressing the product, and then feeding back results to manufacturing and engineering. This feedback takes two forms. There is a formal monthly Reliability Summary distributed to all groups. The summary shows current product failure rates, highlights problem areas, and shows the status of qualification and corrective action programs. Less formal feedback is obtained by including reliability personnel at all product meetings, which gives high visibility to the reliability aspects of various products. As a customer service, product reliability data is compiled and made available upon request.

TABLE 7-1. Package Environmental Stress Matrix

| Test | MIL-STD-883 | |
|---|--------------|---|
| | Method | Condition |
| GROUP B | | |
| Subgroup 1 Physical Dimensions | 2016 | |
| Subgroup 2 Resistance to Solvents | 2015 | |
| Subgroup 3 Solderability | 2003 | Soldering Temperature of 260 ± 10°C |
| Subgroup 5 Bond Strength (1) Thermocompression (2) Ultrasonic or Wedge | 2011 | (1) Test Condition C or D (2) Test Condition C or D |
| GROUP C | | |
| Subgroup 2 Temperature Cycling Constant Acceleration | 1010 2001 | Test Condition C (−65°C to +150°C) Test Condition E (30 kg), Y ₁ Orientation and X ₁ Orientation Test Condition D (20 kg) for Packages over 5 gram weight or with Seal Ring Greater than 2 inches |
| Seal (a) Fine (b) Gross Visual Examination End-Point Electrical Parameters | 1014 | |

Reliability (Continued)

TABLE 7-1. Package Environmental Stress Matrix (Continued)

| Test | MIL-STD-883 | |
|--|-------------|---|
| | Method | Condition |
| GROUP D | | |
| Subgroup 1 Physical Dimensions | 2016 | |
| Subgroup 2 Lead Integrity | 2004 | Test Condition B2 (Lead Fatigue) |
| Seal | 1014 | As Applicable |
| (a) Fine | | |
| (b) Gross | | |
| Lid Torque | 2024 | As Applicable |
| Subgroup 3 Thermal Shock | 1011 | Test Condition B (–55°C to +125°C) 15 Cycles Minimum |
| Temperature Cycling | 1010 | Test Condition C (–65°C to +150°C) 100 Cycles Minimum |
| Moisture Resistance | 1004 | |
| Seal | 1014 | |
| (a) Fine | | |
| (b) Gross | | |
| Visual Examination | | |
| End-Point Electrical Parameters | | |
| Subgroup 4 Mechanical Shock | 2002 | Test Condition B (1500g, 0.5 ms) |
| Vibration, Variable Frequency | 2007 | Test Condition A (20g) |
| Constant Acceleration | 2001 | Same as Group C, Subgroup 2 |
| Seal | | |
| (a) Fine | | |
| (b) Gross | | |
| Visual Examination | | |
| End-Point Electrical Parameters | | |
| Subgroup 5 Salt Atmosphere | 1009 | Test Condition A Minimum (24 Hours) |
| Seal | 1014 | As Applicable |
| (a) Fine | | |
| (b) Gross | | |
| Visual Examination | | |
| Subgroup 6 Internal Water-Vapor Content | 1018 | |
| Subgroup 7 Adhesion of Lead Finish | 2025 | |

Design Considerations for High Speed Architectures

National Semiconductor
Application Note 573
Mike Arden



AN-573

INTRODUCTION

Users and software developers are placing increasing demands on the systems manufacturer to improve the performance of his products. Quite often, these demands can be reduced to two fundamental characteristics of the system, memory array size and system speed. Larger and larger memory arrays are required to support the memory intensive demands of new software applications. Furthermore, as software complexity increases, the system is burdened with more and more software overhead. Greater operating speeds are demanded out of a system in order to support the enlarged software demands without burdening the user with a less responsive system.

Historically, memory array sizes could be improved with the implementation of larger TTL memory devices. The improved density and availability of semiconductor memory devices over the past twenty years is well known. Memory density has improved at roughly a geometric growth rate. To some extent, the memory device could be treated as an ever increasing, self contained black box. The techniques used to integrate a 256k DRAM are virtually identically to those required of a 1k DRAM. It was up to the semiconductor manufacturer (and in his best interest) to maintain a logical progression from one device generation to the next. During this same period of time, small to mid-level systems (personal computers, workstations, graphic display stations, etc.) were in their infancy. Eventhough, processors were fairly low in speed and performance, software sophistication was low. Not long ago, systems operating at eight MHz with 32k of memory were highly respected workhorses. Now, systems are moving into 25 MHz speeds with multi megabyte memories and are pushing into the dual digit MIP ranges.

To satisfy these demands, systems manufacturers are finding themselves more and more involved with ECL device families. ECL devices have always provided improved speeds over TTL devices. In the past, the improved speed was always at the cost of lower memory density, increase power demands, and greater difficulty in system design and integration. For the manufacturer with low power or high density applications, ECL devices were not an acceptable solution. While a large memory array could be constructed out of ECL 256-bit or 1k memories, the array typically became so large and power hungry that it became cost prohibitive. Furthermore, processor engines were typically not available to make use of this high speed memory.

With the advent of the National Semiconductor's BiCMOS ECL memory products, the traditional shortcomings related to density and power consumption have been eliminated. ECL memories rival their TTL counterparts in density and power consumption. In addition, these memories retain the traditional ECL speed advantage over their TTL cousins. Furthermore, ECL system environments offer distinct advantages over TTL environments which can enhance system performance.

System Environments (ECL vs TTL)

As mentioned previously, for low speed/performance systems, ECL devices are more difficult to integrate into a system than TTL devices. This is due to the particular electrical requirements for ECL devices. Correctly implementing an ECL device is more than simply connecting an output of one device to an input of another. The system environment that an ECL device is placed in is defined (loading, network terminations, line impedances, etc.) and the device is designed specifically for this environment. A TTL device on the other hand is not designed for any particular system environment. While this aids the TTL device in fitting into general use applications, it is a major stumbling block for high speed applications.

For example, TTL device outputs are designed for load conditions related to TTL input conditions. *Figure 1a* shows a common (databook) TTL test load configuration. This load is an approximation of multiple TTL input loads. When the output is in the HIGH state ($\geq 2.4V$), the load will sink a minimum of 4.0 mA. Conversely, when the output is in the LOW state ($\leq 0.4V$), the load will source a minimum of 8.0 mA. These are common V_{OH}/I_{OH} and V_{OL}/I_{OL} DC conditions. The device is designed and tested to this set of conditions. As long as the device is placed in an environment such that signal paths are relatively short, the TTL output will behave as expected. However, if the device is placed into a transmission line environment the output characteristics will change depending on the characteristics of the signal line. (A transmission line environment exists if the overall length of the signal path is a significant (0.25) fraction of the rise/fall time of the device output. The greater the fraction, the more the environmental effects.) If the transmission line network is designed for this type of loading, then there is a clean signal transmission; unfortunately, it is very difficult to obtain such a network for TTL devices. If the network is not characteristic of this load, then signal reflections and distortions result. These can delay signal propagation speeds through the system and affect overall system performance.

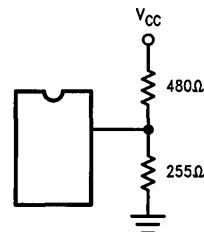


FIGURE 1a. Databook

TL/D/10098-1

Theoretically, a transmission line network can be designed for a TTL load. *Figure 1b* shows the Thevenin equivalent of the TTL load. This equivalent load has the same loading properties as the original load. From this Thevenin load, a transmission line matching load can be derived (see *Figure 1c*). The transmission line load is equivalent to the databook load with the exception of the physical propagation delay of the transmission line. A device output will behave exactly the same with this load as it would with the databook load. The signal itself would be delayed by the transmission line, but not distorted. A device input at the other end of the line would see an undistorted TTL output waveform.

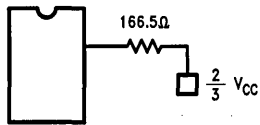


FIGURE 1b. Equivalent Loading

TL/D/10098-2

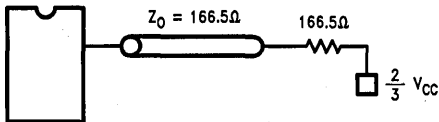


FIGURE 1c. Transmission Line Match

TL/D/10098-3

Unfortunately, TTL systems are not designed with this type of loading scheme. *Figure 2* shows a more commonly found environment. Note that the signal line impedances are lower than the ideal. High impedances in printed circuit boards are difficult to manufacture and are not commonly found. Quite often 75Ω – 100Ω is an upper limit. Also, the transmission line is unterminated. The ideal transmission line load used a 166.5Ω resistor terminated to $3.33V$. Terminated lines would require an additional power supply and many discrete resistors to implement. These differences equate to reflections on the signal paths. These reflections can result in delays in data transmission.

Figure 3a shows IV curves of TTL inputs and outputs in the HIGH state. These curves can be equated to time domain reflection diagrams illustrating the signal integrity. For the example of a 100Ω environment, *Figure 3b* shows the resulting waveforms. For this example, any input at the far end of the line will receive a relatively clean signal. The signal is above the V_{IH} level at $t = T$ and data can be properly identified. The slight bump at $t = 3T$ only cleans up the signal futher. The problem arises if another input is placed near the device output. Due to the reflection from the far end of the line, the input at A (device 2) has to wait until $t = 2T$ before it receives clear identifiable data! Furthermore, any input placed somewhere between the output and the end of the transmission line will see some distorted signal which may not provide a valid data transition until $t = 1.5T$. This example is relatively simple; even still, such a reflected delay can amount to a significant percentage of the overall cycle rate and can cause a marked degradation in system speed. Depending on the type of routing scheme used, and the actual impedances of the PCB, even greater delays can occur.

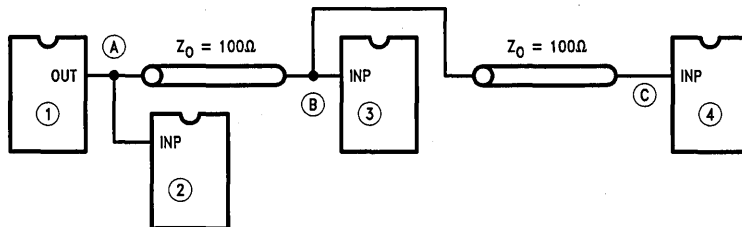


FIGURE 2. "Typical" Application

TL/D/10098-4

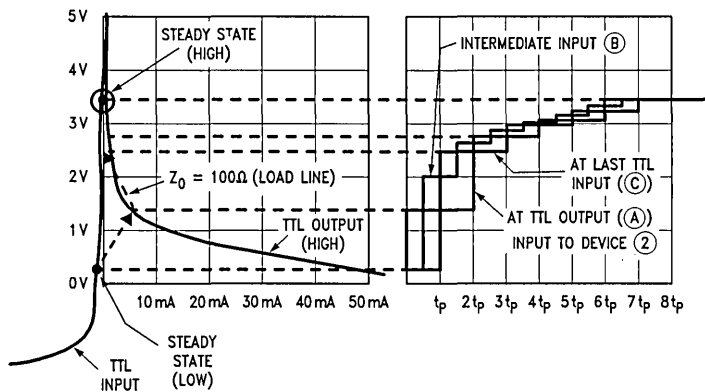


FIGURE 3a. TTL Transition to High State

FIGURE 3b. Reflection Diagram for Transition to High State

TL/D/10098-5

For ECL devices placed into their specified environment, reflections are not a concern. ECL devices are designed specifically for (50Ω) transmission line networks. Figure 4a shows the databook load for ECL devices. This load is not only the test load for the device, it is also the specified load for the system environment. This load is a Thevenin equivalent and can be easily translated into an equivalent transmission line load (see Figure 4b). As was the case with the idealized TTL transmission line load (Figure 1c), this load will transmit data cleanly with only the physical delay of the transmission line being a factor in propagation speeds.

Unlike the typical TTL application, the typical ECL application utilizes this loading scheme (see Figure 4c). Consequently, there are no reflections or distortions of the signal transitions. Figure 5a shows the IV curves of ECL output LOW and HIGH conditions. Figure 5b shows the resulting time domain reflection diagram. This signal is cleanly propagated along the network until it arrives at the end of the line. Due to the fact that it is a properly terminated transmission line, there is no reflection. Any input placed along the line will see a clean signal transition delayed by the propagation delay of the line to that point! The worst case delay for the signal is $t = T$

ECL Load Matching

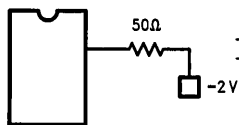


FIGURE 4a. Databook Load

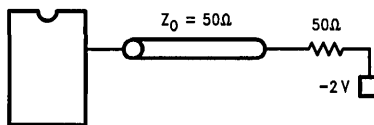


FIGURE 4b. Transmission Line Match

TL/D/10098-6

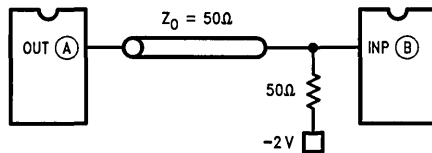


FIGURE 4c. "Typical" Application

TL/D/10098-7

Data Transmission on ECL Systems

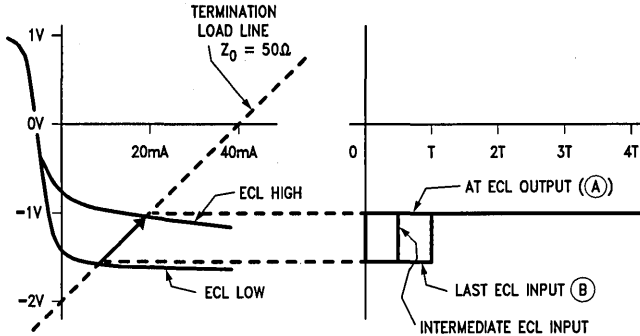


FIGURE 5a. ECL Transition to High State

FIGURE 5b. Reflection Diagram for Transition to High State

TL/D/10098-8

ECL System Design Considerations

Due to the terminated impedance environment required by ECL devices, there are a few basic routing rules which must be followed. Before designing an ECL system, an understanding of these basic routing conditions should be understood. Some of the basic considerations are discussed here; a more comprehensive discussion can be found in the National F100K ECL User's Handbook.

The most straight forward connection method was shown in Figure 4c. This method simply places a 50Ω resistor at the input to the next device to provide a series terminated load. In some cases, it is desirable to connect several outputs to a common bus. This is particularly desirable for ECL devices

since they have open emitter outputs and are specifically designed to be used in wired-or bus configurations. Figure 6a shows a typical "party line" connection. In this case, care must be taken to minimize the physical distance between the two outputs. If the distance is large enough, the signal line between the two outputs will act as a transmission line (Figure 6b). For the output in device 1 this doesn't cause a problem, because it is at one end of the transmission line. However, device 2 is in the middle of the transmission line. The output in device 2 sees the equivalent of a 25Ω transmission line for some length of time. This causes impedance mismatches at the terminated load and results in signal reflections.

Party Lines

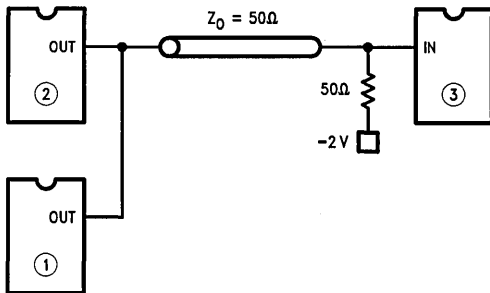


FIGURE 6a

TL/D/10098-9

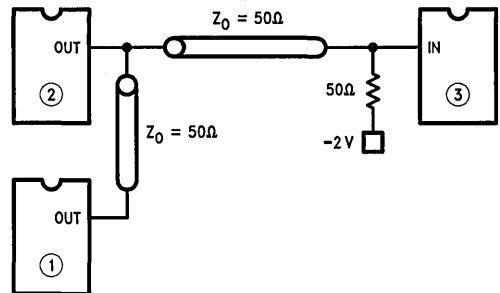
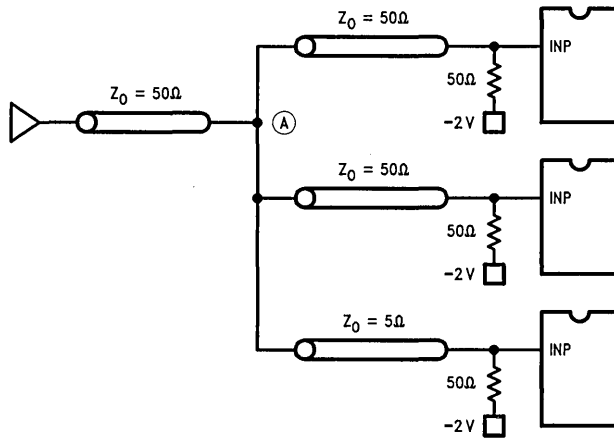


FIGURE 6b

TL/D/10098-10

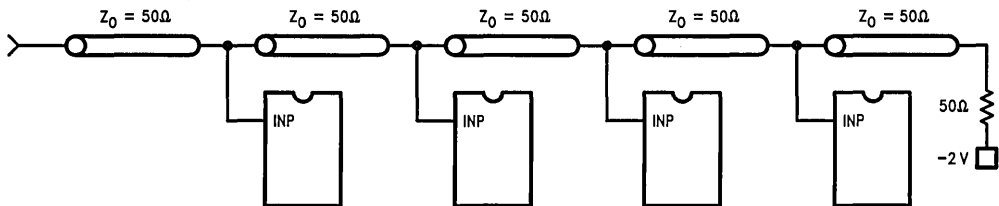
Figure 7a shows an incorrect signal termination method. The parallel terminations cause the impedance that the device output sees to drop to 16.7Ω . An impedance mismatch occurs at node A where the transmission lines split. Reflec-

tions and disturbed signal integrity can result. A correct termination method for bus configurations is shown in Figure 7b. This configuration has only one terminated load and maintains a 50Ω environment throughout.



TL/D/10098-11

FIGURE 7a. Incorrect (For High Speed Applications)



TL/D/10098-12

FIGURE 7b. ECL Bussing Terminations

ECL PCB Design Considerations

In order to design a printed circuit board for an ECL system, many factors have to be considered. The ultimate goal is to develop a PCB with transmission line impedances as close to 50Ω as possible. In order to accomplish this, the geometry of the board itself and the properties of the ECL device must be considered.

Figure 8 shows a PCB cross-section of several μstrip transmission lines. The factors affecting the overall impedance of the board are the metal thicknesses, widths, heights, and spacings; and the dielectric constants and thicknesses of the dielectric materials. For example, the impedance of a microstrip line can be found from:

$$Z_0 = [87/\sqrt{\epsilon_r + 1.41}] * \ln [4.98h/(0.8w + t)]$$

where h = dielectric thickness, w = trace width, t = trace thickness, ε_r = dielectric constant of board material relative to air.

This formula can be used to calculate the undisturbed or "unloaded" impedance of the PCB. Packaged devices have

inherent capacitive and inductive characteristics which can load a PCB transmission line. What is desired from the system point of view is that the final or "loaded" impedance of the board is equal to 50Ω. The capacitance of the device affects the final impedance of the PCB. Figure 9 shows a discrete RLCM model of the transmission line network shown in Figure 8 and Figure 10 shows the effect of adding a device to this network. Capacitors CD1, CD2 are the capacitances of two device inputs. These capacitors are parallel to the capacitors of the transmission line and thus increase the overall capacitance of the transmission line. The inductors (LD1, LD2) are the inductances of two device inputs. Though these inductors are parallel to the transmission line, they do not affect the overall characteristics of the transmission line because they lead into an open circuit (they device itself). Consequently, the dominant effect of adding devices to a PCB is the increased capacitance of the PCB.

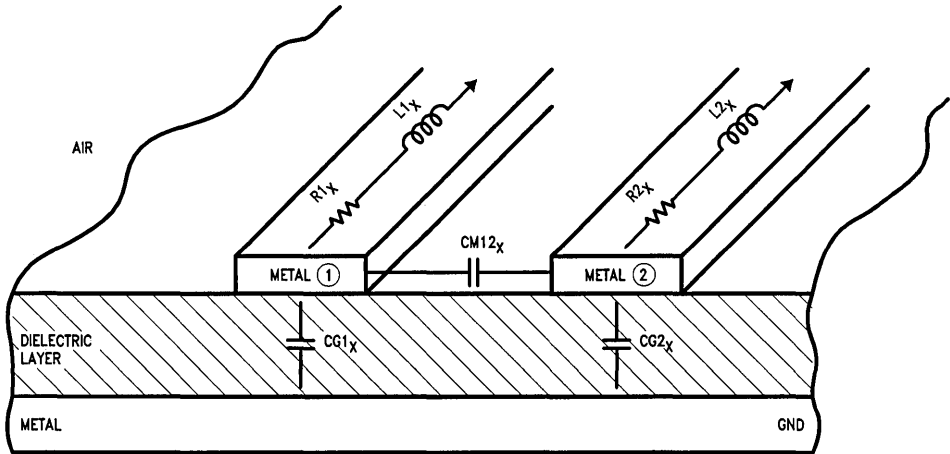


FIGURE 8. Geometric Model of PCB

TL/D/10098-13

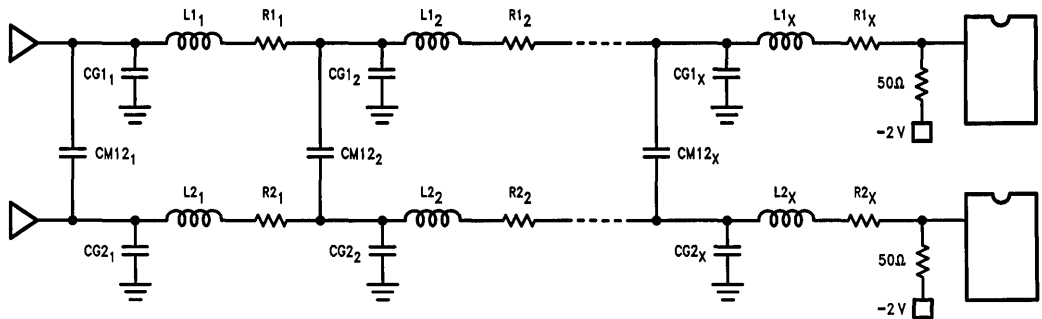
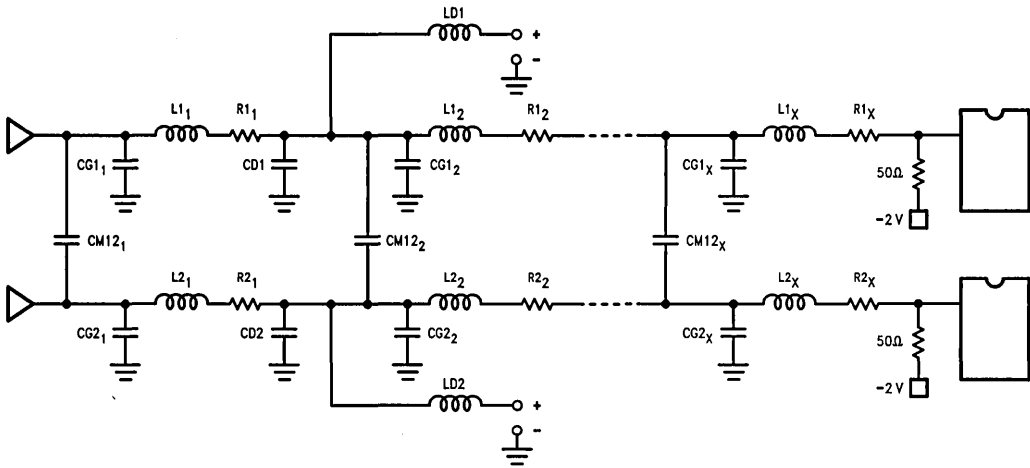


FIGURE 9. RLCM Network Model for PCB (Unloaded)

TL/D/10098-14



TL/D/10098-15

FIGURE 10. RLCM Network Model for PCB (Unloaded)

For example, an unloaded PCB transmission line could have the following properties:

$$C_0 \text{ (characteristic capacitance)} \approx 1.44 \text{ pF/cm}$$

$$L_0 \text{ (characteristic inductance)} \approx 3.61 \text{ nH/cm}$$

Since the impedance of a transmission line is equal to the square root of inductance divided by the capacitance,

$$Z_0 \text{ (characteristic impedance)} \approx 50.1 \Omega \text{ [unloaded]}.$$

If we want to place 5 devices along this line (10 cm in length) and each device has an input capacitance $C_{dut} = 2 \text{ pF}$, the resulting impedance of the transmission line would be:

$$Z_0' \text{ (loaded)} = \sqrt{L_0} / \sqrt{C_0 + C_{dut}}$$

$$= \sqrt{3.61 \text{ nH/cm}} / \sqrt{[1.44 \text{ pF/cm} + (2 \text{ pF/device} * 5 \text{ devices/10 cm)]}}$$

$$\approx 38.5 \Omega$$

This impedance is significantly lower than the 50Ω impedance which is needed. Consequently, the designer must design his unloaded board to a sufficiently high impedance so that after the board is populated it will measure 50Ω .

Modeling of Loaded Transmission Lines

Using the RLCM model shown in *Figure 10*, a SPICE model can be constructed to evaluate the effects of increased device capacitance on the PCB.

Figures 11–13 show the output from such a SPICE model; the transition modeled is a low to high transition at nominal ECL levels. The transmission line model was tuned to a specific capacitance value for the device. As expected, the SPICE output predicts an underdamped condition for the unpopulated board (*Figure 11*). The transition first overshoots and then undershoots the nominal V_{IH} level. As capacitance is added, the transition gets closer and closer to the ideal matched condition. *Figure 12* shows the effects of an "overloaded" line. In this case, the capacitance of the device is not totally compensated by the PCB. Consequently, the signal undershoots and then overshoots the nominal V_{IH} level.

Figure 13 shows the resulting signal of a tuned "loaded" transmission line. Due to the design of the transmission line, the added capacitance of the device is compensated by the intentional addition of increased line inductance.

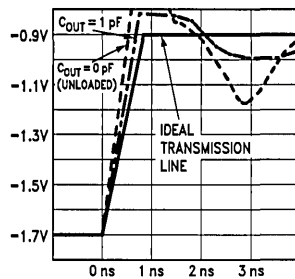
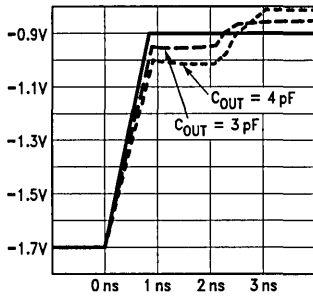


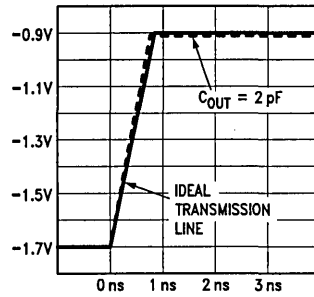
FIGURE 11

TL/D/10098-16



TL/D/10098-17

FIGURE 12



TL/D/10098-18

FIGURE 13

Summary

For maximum performance, layout and construction requirements on printed circuit boards for next generation systems must become more demanding. While at first glance, designing with ECL devices poses more difficulties for a system designer than TTL devices, if the goal is to obtain high system performance then ECL devices offer significant ad-

vantages. Because of the fact that they are designed specifically for high speed environments, the ECL device is easier to integrate into a high speed system. With the geometries and characteristics of the printed circuit board and the device considered as a unit, a network can be designed to produce a clean controlled impedance environment for an ECL device much easier than for a comparable TTL device.

Using the F100250 for Copper Wire Data Communications

National Semiconductor
Application Note 582
Jim Mears



AN-582

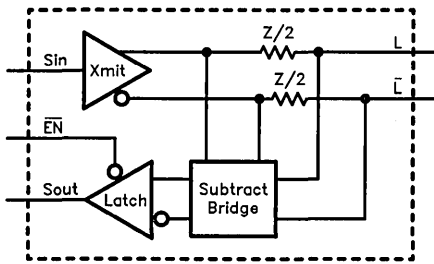
Ideal "digital" signals do not exist, especially when the signal must travel from source to destination over any current-carrying conductor. The world of "digital" signals is truly the world of high-frequency analog and radio-frequency (RF) amplifiers and energy transmission systems. This is especially true for the case of high-speed copper wire data communications networks. The problems of sending signals over the wire interface, whether a printed circuit board or a coaxial cable, require a knowledge of transmission line theory.

To effectively use devices like the F100250 Line Transceiver in high-speed data communications networks, the system designer needs to be acquainted with several subjects among which are: the effects of using pulse excitation on a transmission line, a knowledge of the various forms and modes of data-transmission-line circuit operation, familiarity with the problems of working with long transmission lines, a working knowledge of the driver and receiver, their electrical characteristics, and where and how to use them. This applications note cannot treat the whole subject of "digital" data transmission since the scope of that subject could and has filled whole volumes. This note will touch upon the transmission line topic in conjunction with offering helpful suggestions on how to more effectively use the F100250 Line Transceiver.

F100250 DESCRIPTION AND OPERATING FEATURES

The F100250 is a quintuple, differential-line transceiver with the unique capability of being able to transmit and receive differential-mode signals simultaneously on the same transmission line. The F100250 is part of the National Semiconductor F100K ECL family. As such it shares ECL interface signal characteristics in common with the F100K family.

The circuit of the F100250 (*Figure 1*) is comprised of a line transmitter with differential output, a differential receiver with transparent latch, signal separation circuitry, and internal line termination circuitry. The transmitter is a single-ended input to differential-output amplifier which connects to the line through an active-resistive bridge network. This network provides the correct driving-point and termination impedances for the transmission line and forms part of the received-signal separation circuitry.



TL/F/9564-1

FIGURE 1. F100250 Block Diagram

The receiver consists of a voltage subtractor and hysteresis circuit followed by an amplifier and emitter-follower output. The receiver has a common-mode voltage immunity of $\pm 1V$. The possibility of oscillation in response to slow rise or fall times is reduced by using hysteresis; and the ability to detect noisy signals is improved. The typical hysteresis level of the F100250 is 50 mV.

The receiver incorporates a transparent latch for data retention in synchronous-type operations. The level-sensitive, latch ENABLE pin simultaneously controls the operation of all latches in the part. Data present on the line inputs (L and \bar{L}) prior to taking ENABLE high is retained in the latch, assuming proper setup and hold timing is met. The latch is fully transparent when ENABLE is low.

Termination is provided internally for 30 AWG twisted-pair lines which have a nominal impedance of 150Ω . Higher or lower impedance values may be accommodated by use of a suitable external termination network.

Bi-Directionality

The hallmark of the F100250 is its ability to simultaneously send and receive differential-mode NRZ signals over the same line. This operational mode is known as "baseband full-duplex". By contrast, full-duplex operation is normally accomplished using frequency-division multiplex (FDM) techniques. A common example of which is the 103 or 212A telephone line modem. The F100250 uses a balanced-bridge to separate the transmitted and received baseband signals.

The F100250 can also operate in a uni-directional manner. It is suggested that the input to the transmitter for the unused direction be held at a fixed mark or space level. The ECL signal inputs (Sin 1-5) incorporate $50\text{ k}\Omega$ pull-down resistors for the purpose of holding the unused input at a low (inactive) logic level.

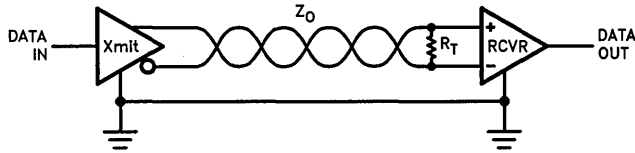
The F100250 cannot operate in a party-line or multi-drop mode due primarily to the fact that the transmitter outputs cannot be turned off (i.e., made high-Z or TRI-STATE[®]). Also, connecting more than two devices to the line would cause a multiple mismatch to occur since the device's output is self-terminating. This restriction should present few problems since the primary use for the F100250 will be in the highest speed point-to-point type applications.

SUITABLE TYPES OF TRANSMISSION LINES

Twisted-Pair Lines

The F100250 is designed for operation over 150Ω , 30 AWG twisted-pair lines. However, it will operate with a variety of other line types and impedances if an appropriate termination method is used as will be shown in the application example.

Twisted-pair transmission lines (*Figure 2*) are available shielded and unshielded, singly and in multi-pair cables, in popular ribbon configurations and in combinations of these. Impedances range from 93Ω for 32 AWG solid, unshielded, ribbon cable to 124Ω , 25 AWG, multiple, individually-



TL/F/9564-2

Note: $R_T = Z_0$

FIGURE 2. Terminating Differential Twisted Pair

shielded pair and the aforementioned 150 Ω , 30 AWG, unshielded, individual pair. Twisted-pair lines exhibit substantial attenuation and dispersion. This may be seen as the rounding and slowing of fast rise-time signals as they travel down the line. Attenuation can range from 10 dB to over 30 dB per 100 feet at 100 MHz. Propagation velocities range from 0.66 to 0.78 the speed of light (1.3 ns to 1.6 ns/ft). In addition, the electrical characteristics of twisted-pair lines do not permit their analysis by the more traditional methods used for coaxial lines. For this reason, the engineer designing twisted-pair wire transmission systems must be equipped to take and interpret measurements on the particular line type chosen for the application. This is the best, and in some cases the only, way in which the capabilities and limitations of the particular driver-line-receiver combination may be understood. Test equipment and fixturing will be described later in this note to help in making meaningful measurements.

Multiple-Pair Cables

Multiple twisted pair cables are a popular method of interconnecting computing equipment and peripheral devices. Additional considerations must be given when using these types of cables. Some of these are: pair-to-pair coupling and capacitance, pair-to-shield capacitance and pair-to-pair relative propagation delay difference. For example, the propagation delay of a single pair in the cable may be 1.5 ns/lineal-foot and the relative delay between pairs is 0.5 ns/lineal-foot. The design value for the actual per-unit delay would be 1.45 ns to 1.55 ns/lineal-foot. That is, the cable will exhibit a pair-to-pair per-unit-length delta-delay of 0.10 ns. This delta-delay value can be considered additive per unit length between any two given pairs. However, the overall delay value for a length of the cable will be that of the pair with the longest electrical delay. The overall rel-

ative delay of the cable will be the difference between those pairs with the longest and shortest electrical lengths. This is an important delay factor to be considered in determining the minimum unit interval (hence, the maximum data rate) which can be propagated by the network.

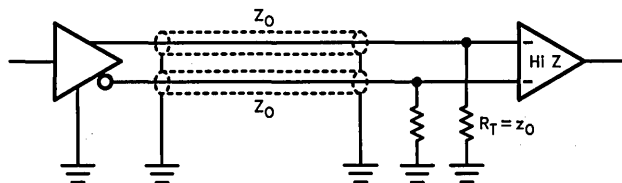
There is another point to remember when determining the delay of multi-pair cables. The delay figures specified in cable data sheets (when given) are normally expressed as delay-per-unit cable length. This value is greater than the actual delay-per-lineal-foot of the pair itself because the layers of pairs are laid-up in a spiral wrap. The fact that the outer pairs traverse a greater distance due to the spiral wrap usually means that they have greater delay per unit cable length than the inner layers of pairs.

Coaxial Cables

Coaxial cables offer a near ideal transmission medium for "digital" data communications signals. Among their more desirable features are: a high degree of shielding, wide bandwidth capability, high velocities of propagation and low attenuation at high frequencies. Coaxial cables are now available paired and in multiple (or ribbon) configurations. Impedances range from 50 Ω to 125 Ω for standard coaxial cables and up to 200 Ω for twinaxial cables. Appendices A and B give a partial list of available coaxial cable with abbreviated data.

Ribbon coax offers a convenient and compact transmission line with mass-termination connector capability. Normally available in 75 Ω and 93 Ω versions, it has excellent shielding properties because of its foil shielding. Available types have moderate attenuation and high propagation velocity.

Terminating coaxial cables is easily done with a parallel termination resistor or by terminating each coax individually as shown in Figure 3.



TL/F/9564-3

FIGURE 3. Terminating Coaxial Cables

As with twisted-pair cables, the electrical length of both coaxial cables used for the differential pair must be the same. It is usually desirable to temperature-cycle and flex the cable prior to cutting and measuring to electrical length. This will relieve stresses resulting from manufacturing and storage on spools. Without stress-relieving, the cable may change in physical length and therefore in electrical length with unpredictable results for network timing.

Measuring the Electrical Length of Cables

Measurement of the electrical length of cables, coaxial or twisted-pair, can be done using a time-domain reflectometer (TDR) which measures physical length by determining the round-trip delay of a fast rise-time pulse signal. The TDR can also be used to check for defects in the cable such as shorts or opens and impedance discontinuities caused by sharp bends or kinks. However, the accuracy of the TDR, usually 1%, does not allow precise length or timing measurements to be made, especially on very short or long lengths. More precise measurements require the use of multi-frequency phase delay techniques using a vector voltmeter or network analyzer and precision frequency sources.

Transmission Lines on Printed Circuit Boards

Printed circuit wiring may also be used as interconnections for the F100250. Line impedances of 75Ω to 100Ω are easily achieved with conventional manufacturing technologies. The main points to observe when laying out differential networks on printed wiring boards are: that both conductors be the same electrical length and that they are the same impedance. This will insure that no skewing of the differential

signal occurs at the receiver input. Skewing appears as an offset in input differential voltage to the receiver.

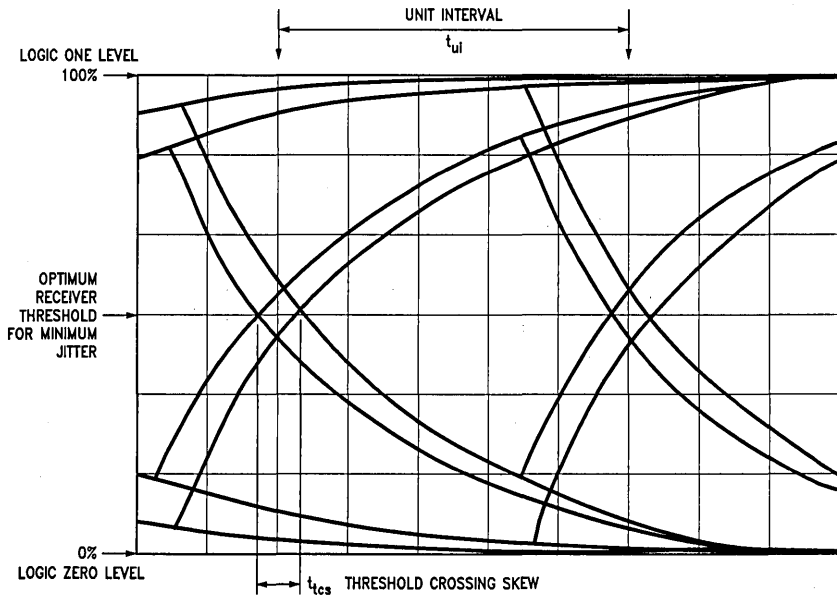
A wealth of information on printed wiring design is contained in the "F100K ECL Databook and Design Guide". Differential techniques are also covered.

Estimating Signal Quality

Before proceeding to the F100250 data transmission system design example, some concepts and terms for the various signal aberrations which will be encountered need to be defined.

Signal quality is concerned with the variation between the ideal instants of the original data signal and the actual transition times of the recovered data signal (Figure 5). Recovered data transitions may be displaced in time from their ideal instants. This is caused by a new wave arriving at the receiver before the previous wave has reached its final value. This is termed "intersymbol interference". It can be reduced by making the unit interval of the signal long with respect to the rise (or fall) time of the signal at the receiver input. Reducing the modulation rate for a given line length or vice versa will reduce this form of interference.

Another form of received-signal distortion present with synchronous signalling, like NRZ, is "isochronous distortion". This is the ratio of the unit interval to the absolute value of the maximum measured difference between the actual and theoretical significant instants. In other words, it is the percentage of the unit interval that is peak-to-peak time jitter of the data signal (Figure 4). If the peak-to-peak time jitter were one-half of the unit interval, the isochronous distortion would be 50%.



$$\text{Peak-to-Peak Jitter} = \frac{t_{tcs}}{t_{ui}} \times 100\%$$

TL/F/9564-4

FIGURE 4. Estimating Peak-to-Peak Jitter

"Bias distortion" is the shortening of the duration of the mark-bits with respect to the space-bits or the reverse (*Figure 5*). It may be caused by a shift of the receiver threshold, asymmetrical driver output levels or both. Together, bias distortion and intersymbol interference are called "systemic distortion". This is because their magnitudes are determined by data transmission system characteristics. Other forms of randomly-occurring distortion such as noise and crosstalk are called "fortuitous distortion". These are due to factors outside the data transmission system.

Signal Quality Measurement

Measurements of signal quality on any transmission system should always be designed to show the effects of intersymbol interference and bias distortion. This means that the test signal must be capable of showing both effects. The use of

a simple NRZ dotting pattern (a signal with 50% duty cycle and frequency of one-half bit-time) cannot show intersymbol interference due to its symmetry. It can show bias distortion as a change in duty cycle for the recovered dotting pattern.

The use of a random NRZ data pattern can show both types of interference by its unpredictable bit sequence. A pseudo-random NRZ data generator built from standard F100K ECL devices is shown in *Figure 6*. This circuit is capable of producing a random sequence (2E20)-1 bits in length at frequencies up to about 240 MHz. When the data produced by this circuit is transmitted over the line and viewed on a suitable oscilloscope, a so-called "binary eye pattern" will be seen. This pattern results from the superposition of alternating mark and space bits during each unit interval. It is so called because the pattern's center resembles an eye.

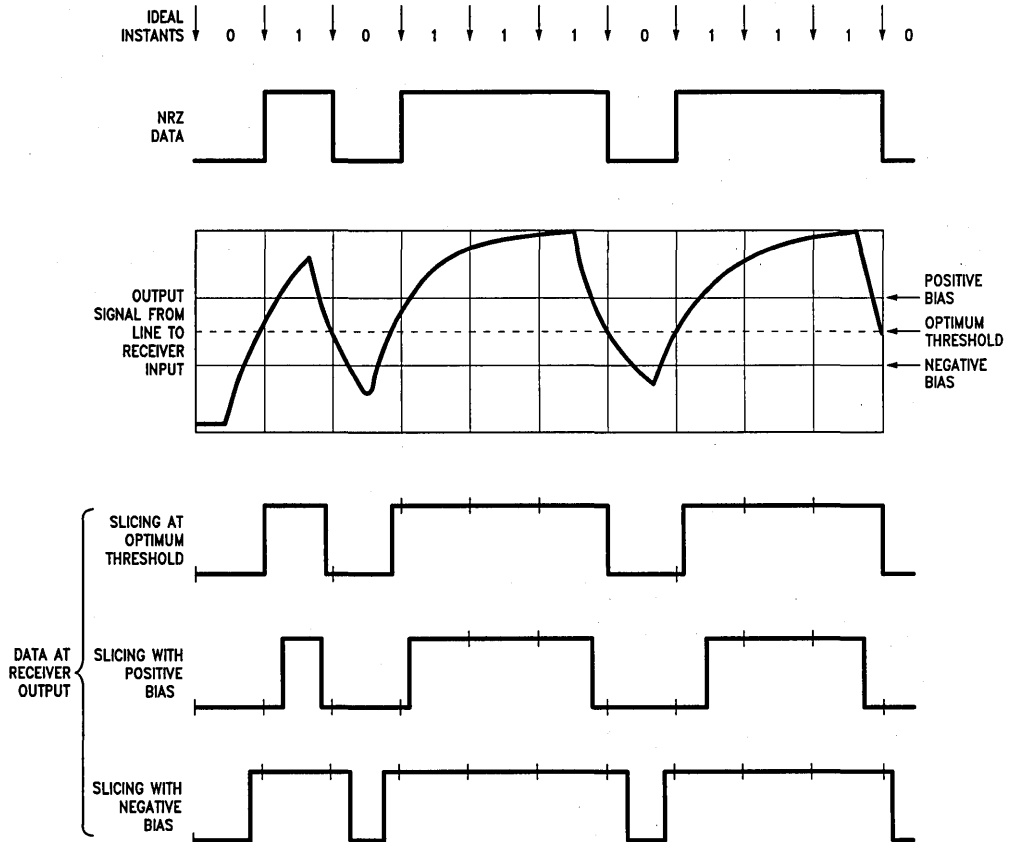
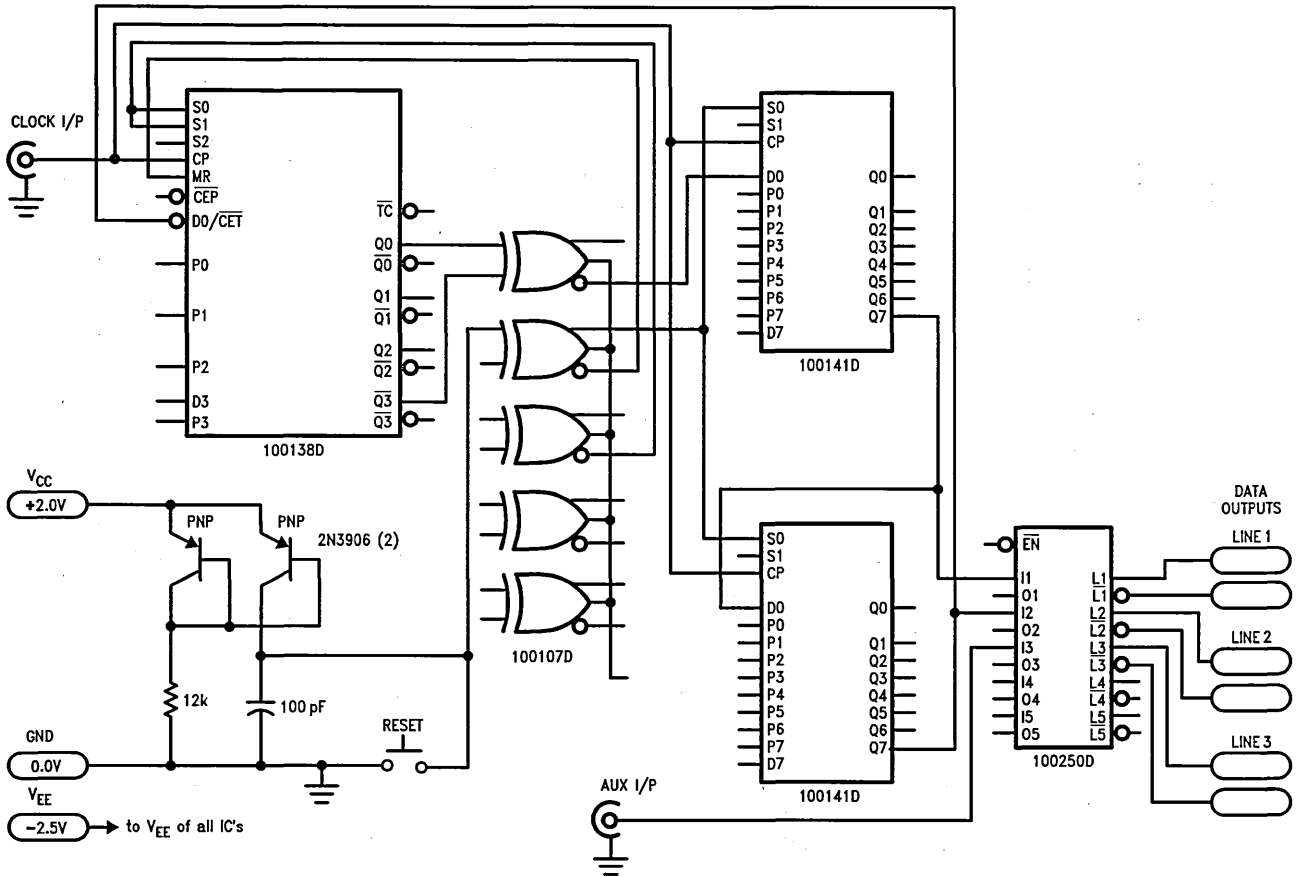


FIGURE 5. Bias Distortion

TL/F/9564-5



Note 1: Termination resistors not shown.

Note 2: Split supplies for test equipment convenience.

Note 3: Clock input 230 MHz max.

FIGURE 6. F100250 Differential Line Test Circuit

TL/F/9564-6

The eye-pattern is a useful tool to measure data signal quality (Figure 7). The spread of transitions crossing the receiver input threshold can be used as a direct measure of isochronous distortion (peak-to-peak jitter). Rise and fall time can be measured by using the self-references of 0% and 100% resulting from the long sequence of mark and space bits.

The noise margin of the system can be measured as the height of the trace above or below the receiver threshold level at the sampling instant. The eye-pattern can even be used to determine the characteristic impedance of the transmission line. The method is discussed in Appendix C.

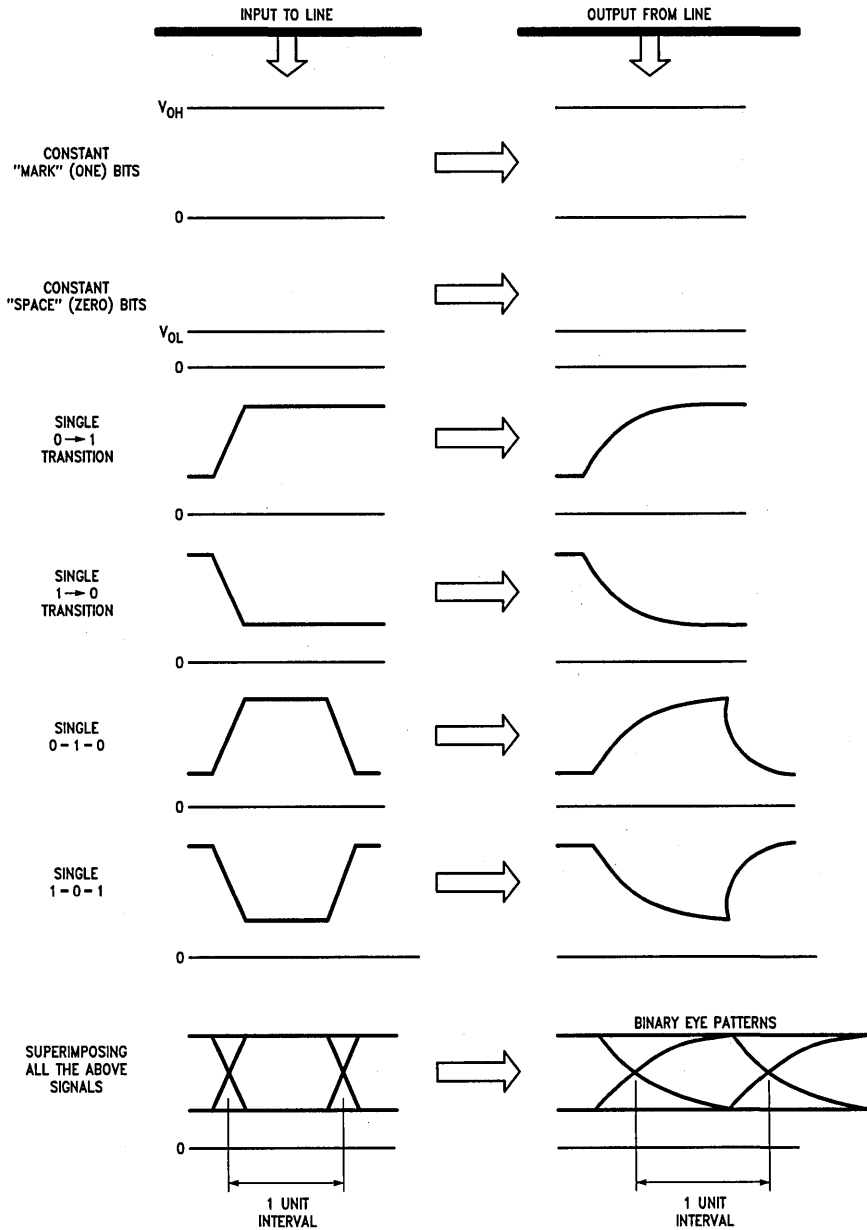


FIGURE 7. Formation of the Binary Eye Pattern

TL/F/9564-7

The eye-pattern gives, in some ways, the minimum peak-to-peak transition jitter for a given line length, type, pulse code, and modulation rate. This is because the pattern results from intersymbol interference and reflections (if present). Minimum jitter conditions only result if: 1) the mark and space signal levels from the driver are symmetrical and the receiver's threshold is set at the mid-point of these levels; 2) the line is terminated in its characteristic impedance; and 3) propagation delays through both transmitter and receiver for both logic states is symmetrical and without relative skew. Signal quality is reduced if any of these conditions is not met.

The decision threshold shown by the displayed eye-pattern for a particular driver and modulation rate shows the effects of receiver bias (or threshold ambiguity) and offset. The slope is small in the threshold region for signals with greater

than 20% isochronous distortion. Therefore, small amounts of bias produce large increases in isochronous distortion. A good practice is to design systems to have less than 5% transition spread as shown in the eye-pattern. This minimizes the effects due to bias and simplifies design requirements for line transmitters and receivers.

Application Example— Putting the F100250 to Work

The F100250 excels at transmitting over twisted pair wiring. *Figure 8* shows an example using 50 meters of 106 Ω , 26 AWG, unshielded pair. The pair used is one of 25 in a multi-pair cable specifically designed for digital signal transmission. Note that termination resistors have been added for improved impedance matching to the F100250 line terminals. The scope photos in *Figures 9a* and *9b* show the composite signal conditions at the receiver input. Two pseudo-random signals, 10 MHz and 50 MHz, are present on the line in this example.

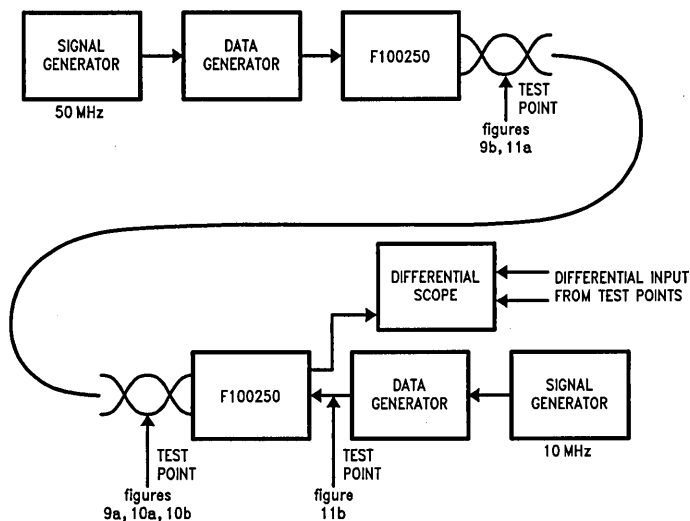
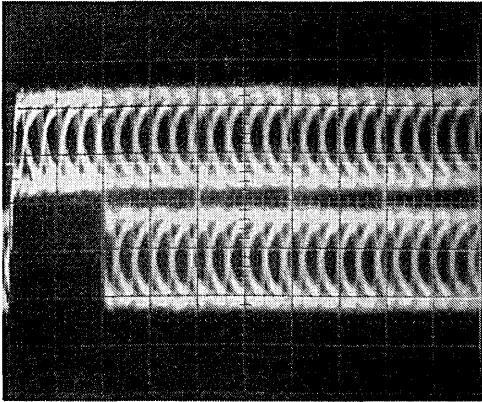


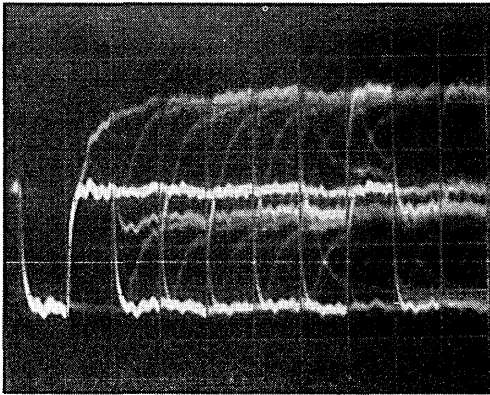
FIGURE 8. Twisted Pair Test Circuit

TL/F/9564-8



TL/F/9564-9

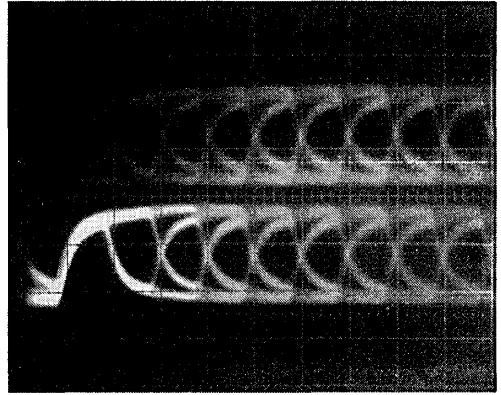
FIGURE 9a. Composite Signal at Receiver Input (50 MHz) Showing Both 10 MHz and 50 MHz Signals on the Line (Differential Mode)



TL/F/9564-10

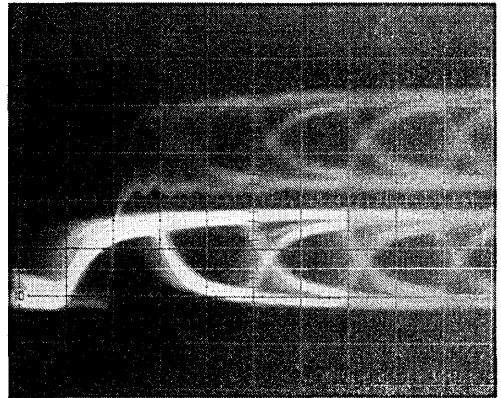
FIGURE 9b. Composite Signal at Transmitter Output (50 MHz) Showing Both 10 MHz and 50 MHz Signals on the Line (Differential Mode)

Figure 9a shows the composite signal at the receiver input for the 50 MHz signal. Note that both signals appear with the received signal (50 MHz) "riding on" the locally transmitted signal (10 MHz). *Figure 9b* shows the 50 MHz signal as transmitted. Signal attenuation is approximately 2 dB for the 50 MHz signal.



TL/F/9564-11

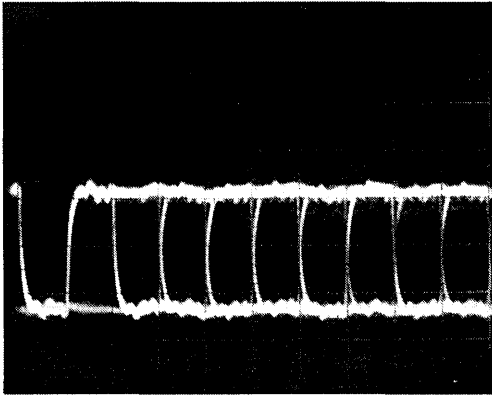
FIGURE 10a. 50 MHz Signal at Receiver Input. (Intensification Due to Overlapping 10 MHz Signal) 20 ns/div. Horiz.



TL/F/9564-12

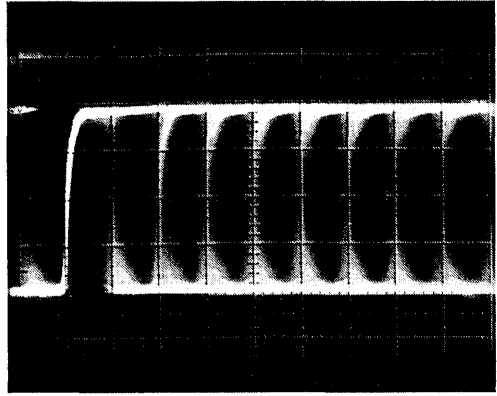
FIGURE 10b. 50 MHz Signal at Receiver Input. 10 ns/div. Horiz. Peak-to-Peak Jitter is Less Than 40% Total.

Figures 10a and *10b* show the 50 MHz signal at the receiver input. The peak-to-peak jitter from all sources is about 40% maximum. *Figure 11a* shows the 50 MHz signal at the line input (differential mode) and *Figure 11b* shows the recovered 50 MHz signal at the receiver output. The effective jitter can be seen in the recovered signal. It is important to note that the F100250 exhibits no threshold shift which would contribute to bias distortion.



TL/F/9564-13

FIGURE 11a. 50 MHz Signal at Transmitter Output (Line Input)



TL/F/9564-14

FIGURE 11b. 50 MHz Signal at Receiver Output (Recovered Signal). Shows Effect of Jitter on Output.

APPENDIX A—TWISTED PAIR CABLES

| Cable Type | Manufacturer | AWG Wire Size | Z_0 Ω | V_p | C_0 pF/ft | Attenuation 6 dBV Limit k Feet |
|-----------------------|--------------|---------------|-------------------|-------|----------------|--------------------------------------|
| TWISTED PAIR | | | | | | |
| Unshielded | Com'l | 28 | 100 | 0.66 | 15.5 | 0.77 |
| | | 28 | 120 | 0.78 | 11.0 | 0.9 |
| | | 26 | 106 | 0.66 | 12.0 | 2.7 |
| | | 24 | 100 | 0.66 | 15.5 | 2.1 |
| | | 24 | 120 | 0.66 | 12.8 | 2.5 |
| | | 24 | 100 | 0.78 | 12.5 | 2.1 |
| | | 22 | 100 | 0.66 | 15.5 | 3.0 |
| Individually Shielded | Com'l | 24 | 100 | 0.78 | 12.5 | 2.1 |
| | | 25 | 124 | 0.66 | 12.2 | 1.9 |

APPENDIX B—COAXIAL CABLES

| Cable Type | Manufacturer | Part Number | Z_0 Ω | V_p | C_0 pF/ft | Attenuation dB/100 ft @ 100 MHz |
|------------------|--------------|--|-------------------|-------|----------------|---------------------------------------|
| COAXIAL | | | | | | |
| Single | Com'l | RG-59/U | 75 | 0.78 | 17.3 | 3.0 |
| | Belden | 8281 | 75 | 0.66 | 21.0 | 2.7 |
| Dual | Belden | 9555 | 75 | 0.66 | 20.5 | 3.4 |
| | Alpha | 9845 | 75 | 0.66 | 20.5 | 3.4 |
| Single | Com'l | RG-62/U RG-62A/U RG-62B/U MIL-C-17F | 93 | 0.84 | 13.5 | 2.7 |
| | Belden | 9393 | 93 | 0.78 | 14.0 | 8.8 |
| | Alpha | 9063B | 125 | 0.84 | 9.6 | 1.5 |
| TWINAXIAL | | | | | | |
| | Com'l | RG-22B/U | 95 | 0.66 | 16.0 | 3.0 |
| | Belden | 8227 9207 9815 | 100 | 0.66 | 15.5 | 4.1 |
| | Belden | 9271 9860 | 124 | 0.66 | 12.2 | 5.0 |
| | Belden | 9182 | 150 | 0.78 | 8.8 | 4.3 |
| | Belden | 9851 | 200 | 0.76 | 6.7 | 4.0 @ 50 MHz |
| RIBBON | | | | | | |
| | Belden | 9K750XX | 75 | 0.78 | 17.1 | 7.5 |
| | | 9K930XX | 93 | 0.78 | 14 ± 2 | 5.0 |

**APPENDIX C—
MEASURING CABLE IMPEDANCE**

The impedance of a length of cable may be determined from simple measurements using the eye pattern. Either of two methods may be used. In one method the voltage reflection from a known termination is used to calculate Z_0 . The second method uses direct resistance measurement to find Z_0 .

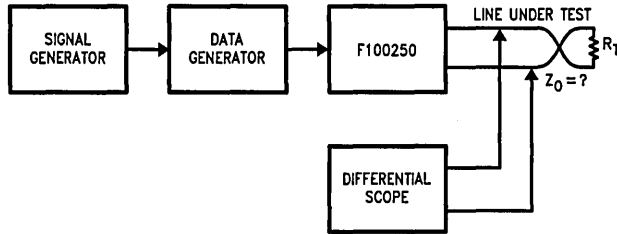
Voltage (Indirect) Method

In the voltage method (Figure C1), the signal generator frequency is set such that the unit interval of the eye pattern is

about twice the round-trip delay of the line to be measured. The peak voltage (V_{peak}) of the eye pattern cell is measured (Figure C2a) with a known value termination resistor at the far end of the line. Next, the voltage at the end of the bit cell (V_{nom}) is measured. The line impedance can then be calculated using the following formula to about 5% accuracy.

$$Z_0 = R_t * ((2 * V_{peak} / V_{nom}) - 1)$$

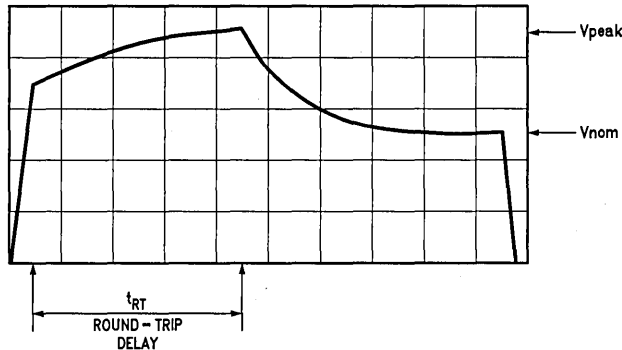
For the waveform shown in Figure C2b, a 51Ω, 5% resistor is used as the termination. The peak line voltage is 390 mV. The voltage at the end of the bit cell is 240 mV. This gives a line impedance of 114.7Ω.



TL/F/9564-15

R_T = Suitable fixed resistor (voltage method) or 250Ω to 300Ω variable resistor (cermet potentiometer) for direct method

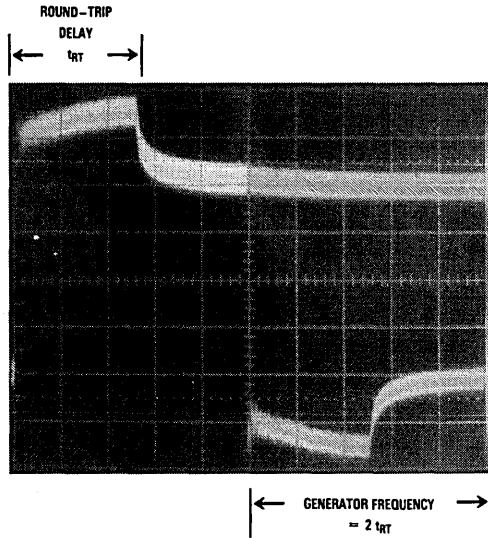
FIGURE C1. Line Impedance Test Setup



TL/F/9564-16

$$Z_0 = R_t \left(\frac{2 V_{peak}}{V_{nom}} - 1 \right)$$

FIGURE C2a



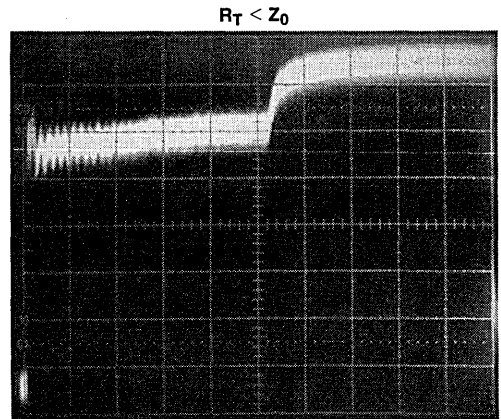
TL/F/9564-17

FIGURE C2b. Voltage Method Waveform

Incidentally, the round-trip delay of the line, represented by the rising portion of the waveform, is 520 ns. Since the cable sample is 50 meters (164 ft.) long, the delay per foot can be estimated to be 1.6 ns per foot. (The data sheet for the cable sample used specified the delay of the pair as 1.575 ns to 1.6 ns per foot and the impedance as 101.5Ω to 105Ω.)

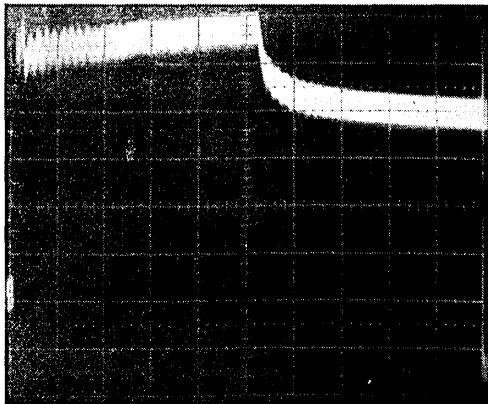
Resistance (Direct) Method

The same test setup is used as for the voltage method. A variable resistor is substituted for the fixed termination. The value chosen should be in the range of 250Ω to 300Ω.



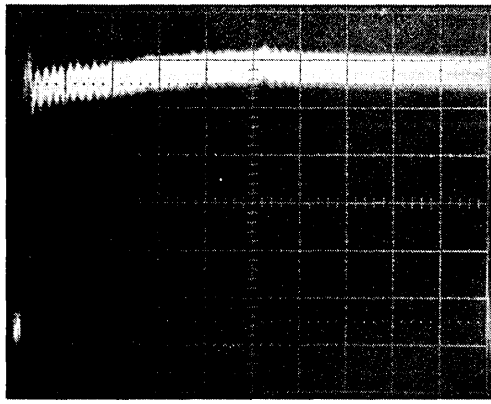
TL/F/9564-18

FIGURE C3a. Under-Terminated

$R_T > Z_0$ 

TL/F/9564-19

FIGURE C3b. Over-Terminated

 $R_T = Z_0$ 

TL/F/9564-20

FIGURE C3c. Terminated

Figures C3a through C3c illustrate the three possible conditions of termination which can be achieved. Figure C3a shows the under-terminated condition where the termination value is greater than the line impedance. Figure C3b is the over-terminated condition where the termination value is less than the line impedance. Finally, Figure C3c shows the condition where the termination is adjusted to match the line impedance. When this condition is achieved, the value of the termination variable resistor, and hence the line impedance, may be read using an Ohmmeter.

Using the direct method to measure the same pair sample gave a value of 105.9Ω for the line impedance. This method is preferred since it is simple and accurate.

BIBLIOGRAPHY

"Application Note 62—Time Domain Reflectometry", Hewlett-Packard Co., 1964.

Ramo, S., J.R. Whinnery, and T. Van Duzer, *Fields and Waves in Communications Electronics*, 1965, New York: Wiley.

Kirsten, F., "Pulse Response of Coaxial Cables", Counting Note No. CC2-1A, Lawrence Radiation Laboratory.

Langford-Smith, F. (editor), *Radiotron Designer's Handbook*, 1953, Amalgamated Wireless Valve Co. Pty. Ltd.: Sidney, Australia.

Gaiser, R., "Two-Wire DC Baseband System for Two-Way Simultaneous Data Transmission at High Speeds", *Conference Record of 1970 International Conference on Telecommunications*, Paper 70-CP-283-COM, pp. 16-33 to 16-41.

Metzger, G. and J.P. Vabre, *Transmission Lines with Pulse Excitation*, 1969, New York, Academic Press.

Krauss, J.D., Ph.D., *Antennas*, 1950, New York, McGraw-Hill.

Nahman, N.S. and R.L. Wigington, "Transient Analysis of Coaxial Cables Considering Skin Effect", *IRE Proceedings*, Vol. 45, Feb. 1957, pp. 166-174.

Nahman, N.S., "A Discussion on the Transient Analysis of Coaxial Cables Considering High Frequency Losses", *IRE Transactions on Circuit Theory*, Vol. CT-9, No. 2, June 1962, pp. 144-152.

Nahman, N.S. and D.R. Holt; "Transient Analysis of Coaxial Cables Using the Skin Effect Approximation $A+B\sqrt{s}$ ", *IEEE Transactions on Circuit Theory*, Vol. 9, No. 5, Sept. 1972, pp. 443-451.

Nahman, N.S., "A Note on the Transition (Rise) Time Versus Line Length in Coaxial Cables", *IEEE Transactions on Circuit Theory (Correspondence)*, Vol. CT-20, No. 2, Mar. 1973, pp. 165-167.

Magnusson, P.C., "Transient Wavefronts on Lossy Transmission Lines—Effect of Source Resistance", *IEEE Transactions on Circuit Theory (Correspondence)*, Vol. CT-15, Sept. 1968, pp. 290-292.

Turin, G.L., "Steady-State and Transient Analysis of Lossy Coaxial Cables", *IRE Proceedings (Correspondence)*, Vol. 45, June 1957, pp. 878-879.

The ECL System Solution

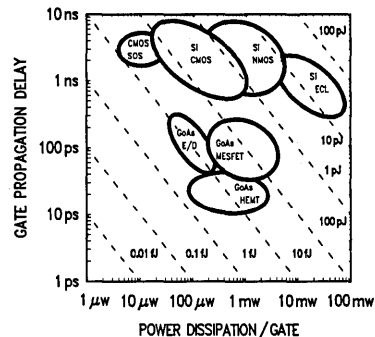
National Semiconductor
Application Note 650
Jeff Bunce



Emitter-Coupled-Logic (ECL) has always been the ugly sister in the world of digital bipolar integrated circuit technology, since its introduction in the early 1960's. ECL has been shunned by the average designer due to its large gate power consumption (mW/gate in the early days) and the need for controlled impedance circuit boards to minimize noise and signal reflections. Non-TTL level power supplies and non-TTL I/O levels have also made ECL unfavorable to the typical system designer. The only people daring enough to take on the challenges of ECL were the system architects needing to handcraft their CPUs/interfaces for optimum performance. In most other instances, the inherently slower TTL and CMOS logic was tolerable, providing an adequate way to complete the task at hand without having to go through the pain of incorporating transmission line theory in board design. The world of system design has changed however, and ignorance is no longer bliss. TTL/CMOS logic families have advanced to the point where their edge rates and propagation delays demand controlled impedance board design to avoid the same pitfalls that have always been present with ECL.

Forced understanding of transmission line theory for TTL and CMOS has the hidden benefit of making ECL more palatable to the modern system designer. As long as the effort needs to be expended in understanding the problem, why not use the technology that truly offers maximum performance at minimum cost? ECL offers the speed that TTL and CMOS technologies never will, and the affordability and levels of integration unattainable by GaAs and other compound semiconductors. Key to understanding these arguments is that the same advances in process technology that are used to enhance CMOS and TTL logic are invariably used to advance ECL's state of the art. The subsequent improvements result in even faster speeds for ECL at significantly reduced power consumption. GaAs is inherently more expensive than silicon based technologies (due to scarcity of materials and excessive manufacturing costs). Although gate-for-gate GaAs may offer faster logic than ECL, the key variables impacting component delay are not the circuitry and devices for SSI logic, rather interconnect on the die and packaging. GaAs is also much more difficult to manufacture from a materials handling viewpoint and will probably never offer the low costs and levels of density ECL affords. GaAs is a niche product that is best suited for specialty applications, but it has been, is now, and probably always will be the technology of the future. Contrary to the smoke and mirrors GaAs houses use to promote ultra high speed GaAs circuits, GaAs only offers a 1.5 to 3× improvement in speed over silicon ECL in real operating conditions away from the security of the supercooled environment of the lab. ECL offers 10 to 100× or more the levels of integration of GaAs at a fraction of the cost.

ECL has also made a number of in roads to maintain its leadership position in the world of silicon base logic. Over the years, ECL has taken advantage of CMOS/TTL processing innovation such that it has overcome its significant power consumption, reducing it from mW/gate to μ W/gate. High speed system design controlled impedance boards are a requirement now for logic families. Contrary to TTL/CMOS, ECL offers zero skew balanced differential outputs which further simplify logic design as well as minimizing power supply and output switching noise. ECL also offers the end user the ability to "wire-OR" outputs together, generating a positive logic "OR" without the expense of additional components. In addition, National (via Fairchild) introduced the first commercially available temperature and voltage compensated ECL logic family. Unlike CMOS and TTL, ECL's temperature and voltage compensation makes the logic much more insensitive to environmental changes which is extremely important for the military designer. This compensation also eases design verification and system debugging by eliminating intermittent problems which can be masked by opening a system cabinet or taking it into an air conditioned lab for inspection.



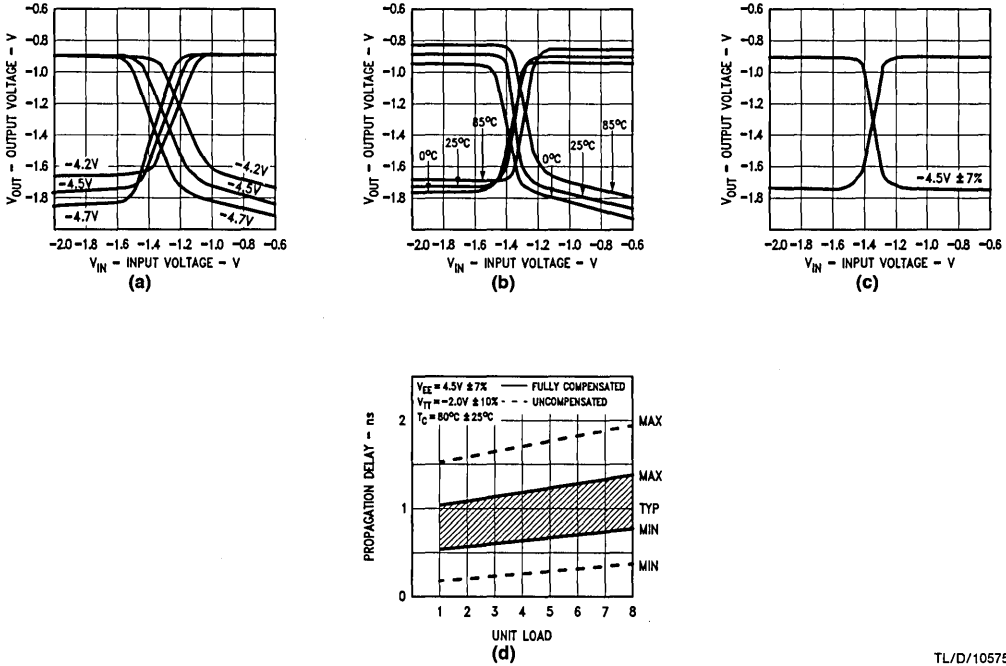
TL/D/10575-1

FIGURE 1. Technology Speed/Power Curve

Fully temperature and voltage compensated logic offers much tighter AC specifications (i.e. minimum AC skew) across the entire power supply/temperature range because the logic is regulated and not allowed to drift with environmental changes. These tighter skew windows become increasingly important in local back planes, local distribution of clocks and other control signals, as well as in distributed systems such as modern CAD workstation environments where host-server(s) communication is critical to improving total system throughput. *Figure 2* below shows how compensation results in much tighter windows for DC levels as well as AC switching parameters versus those for uncompensated logic.

ECL has come a long way since its early days of the egg fryer SSI/MSI functions and high speed low density SRAMs. Today National is the world premier commodity ECL supplier with the broadest base of ECL product families in the industry. National's offerings include: BiCMOS SRAMs with

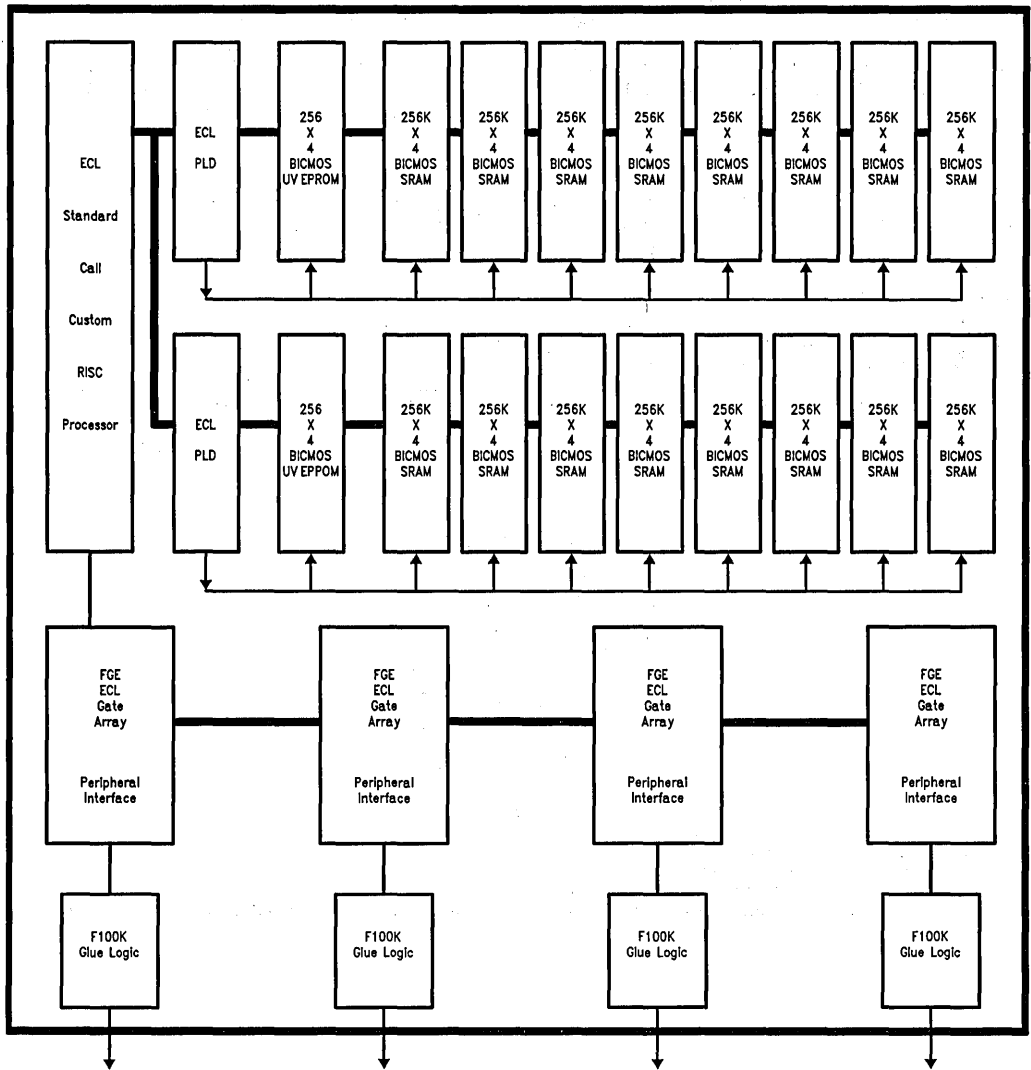
ECL I/O for cache or high speed bulk memory, the world's first BiCMOS UV EPROM for microcode store, ECL Standard Cell families for custom high speed CPU design, ECL Gate Arrays for custom CPU and interface design, ECL PLDs for user programmable glue logic, and F100K for glue logic. Today's designer has entire ECL toolkit available for system design (see Figure 3).



- (a) DC output tracking for ECL logic uncompensated for power supply voltage.
- (b) DC output tracking for ECL uncompensated for temperature.
- (c) DC output tracking for fully voltage and temperature compensated ECL.
- (d) AC Switching Skew for Compensated versus Uncompensated ECL logic.

TL/D/10575-2

FIGURE 2. Comparison of Voltage and Temperature Compensated ECL Logic versus Uncompensated ECL Logic



TL/D/10575-3

FIGURE 3. High Speed ECL I/O Based CPU

National is committed to the military aerospace market for ECL and is capable of offering any of its commercially available ECL products as military grade of "military like" devices on customer demand. National's BICMOS SRAMs (based on BiCMOS III) combines the best of both CMOS and ECL worlds by melding the low power high density CMOS for the memory array with the ECL for high speed I/O, decoders, and sense amps. National offers a wide variety of very high speed ECL I/O SRAMs including 256k x 1, 64k x 4 and 16k x 4 organizations. Development is well under way on a family of 1 Meg ECL I/O SRAMs with access times of 15 ns or less.

Additionally, National is supporting the designer with soon to be announced BiCMOS ECL I/O 2k x 9 Advanced Self Timed RAM having a maximum access time of 5, 7, 10 ns. National also has developed a BiCMOS ECL I/O UV EPROM, pin compatible with the 10149 ECL fuse PROM, in 5, 7, and 10 ns speed grades. This UV erasable ECL I/O EPROM can be used as high speed core CPU microcode store or as a programmable decoder and is programmed with standard TTL levels from readily available PROM programmers. Higher density BiCMOS UV EPROMs in development will soon be able to be used as CPU boot ROMs or for program storage.

National's ASPECT™ process has been utilized to provide the military system designer with high speed, high density fully temperature/voltage compensated ECL I/O standard cell capability. Our standard cell library includes mega cells such as a 64-bit floating point ALU processor, a 64-bit floating point multiply processor, multi-port register files, 32-bit barrel shifter, 64-bit funnel shifter, as well as a number of user configurable soft mega cell functions and the standard assortment of gate functions. These cells provide the system architect with the building blocks to design a high speed RISC (reduced instruction set computer) processor tailored for specific applications. Similarly, National's ECL gate array family offers a lower cost, faster turn-around time solution for the CPU/controller design as well as custom interface/glue logic. National's ECL PALs provide high speed glue logic with the flexibility of user programmability using stan-

dard PAL programming hardware. Last but not least, National's F100K family is the work horse that rounds out the family, delivering SSI/MSI/LSI logic functions. From AND/NAND and OR/NOR gates to ALUs, Wallace Tree Adders, and Carry Look Ahead Generators, F100K is a complete logic family that provides the glue needed to tie together the larger ECL building blocks. National's F100K family also includes low skew drivers excellent for clock distribution and back plane drivers and bidirectional ECL-to-TTL level translators which allows the high speed ECL system to interface to the slower TTL/CMOS peripherals or subsystems.

In addition to offering a military processed F100K product line, National will soon be offering a fully 883C compliant F100K family subset, initially with approximately 30 device types.

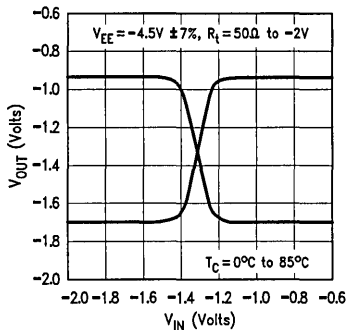
10K vs 100K ECL I/O System Considerations

National Semiconductor
Application Note 651
Eric Hall



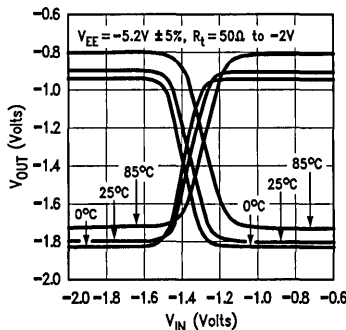
INTRODUCTION

System designers have long realized the advantages of Emitter Coupled Logic (ECL) for high speed systems. This logic family is based on a differential amplifier and has small signal swings to prevent transistor saturation when switching, thus increasing the switching speed. ECL offers high fanout capability and the ability to drive low impedance transmission lines. National's BiCMOS SRAMs have this high speed logic incorporated in their inputs and outputs, thus remaining compatible with existing ECL logic, while at the same time they take advantage of a high density CMOS memory array. ECL logic comes in two different families; 100K logic in which the input and output voltage levels are temperature compensated (*Figure 1*), and 10K logic in which the input and output voltage levels vary over temperature (*Figure 2*). In National's BiCMOS SRAMs both 100K and 10K I/O levels are voltage compensated. This application note will focus on the possible problems of mixing these two logic families and solutions to these problems.



TL/D/10576-1

FIGURE 1. 100K BICMOS III—Compensated ECL



TL/D/10576-2

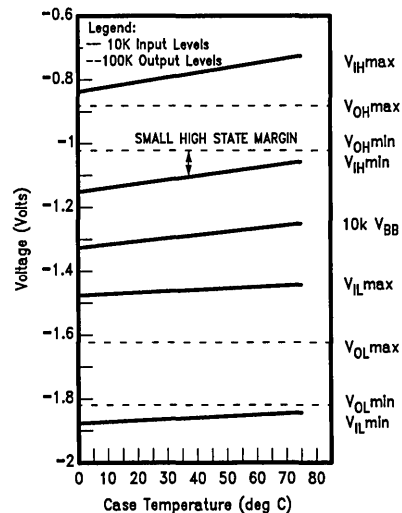
FIGURE 2. 10K BICMOS III—Uncompensated ECL

100K OUTPUTS DRIVING 10K INPUTS

From the graph of DC specification levels (*Figure 3*) one can see that at hot temperatures there is only 20 mV of margin between 100K V_{OHmin} and 10K V_{IHmin} . The shrinking margin as temperature increases is due to the decrease in the base to emitter voltage (V_{BE}) of a bipolar junction transistor. The input reference voltage (V_{BB}) for 10K tracks this temperature dependence while the 100K output levels remain constant across temperature. With this small voltage margin at hot combined with system noise and transmission line bus drop, the 10K inputs may not distinguish a high level from the 100K driver. For this reason it is recommended using 100K drivers to 10K inputs only when the system temperature is maintained below 35°C where there is greater than 100 mV of margin. The graph also shows 20 mV of margin between 100K V_{OLmin} and 10K V_{ILmin} at hot temperature. This will not result in a functionality problem since these levels are far away from V_{BB} and the 10K input will easily recognize the low level.

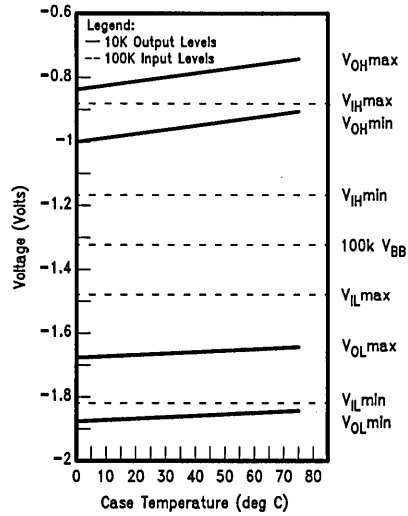
10K OUTPUTS DRIVING 100K INPUTS

There are no functionality problems incurred in driving 100K inputs with 10K outputs (*Figure 4*). The only possible concern would be that the 100K input is driven slightly into saturation at hot where 10K V_{OHmax} is 160 mV higher than 100K V_{IHmax} . However, shmoos plots show there is no measurable speed degradation in National's BiCMOS SRAMs if this scenario were employed (*Figure 5*).



TL/D/10576-3

FIGURE 3. 100K Driving 10K



TL/D/10576-4

FIGURE 4. 10K Driving 100K

Device NM100504 64k x 4 BiCMOS SRAM
 Temp : 85°C
 Shmoo : TAVQV vs V_{IH}
 Comment : $V_{EE} = -5.0V$

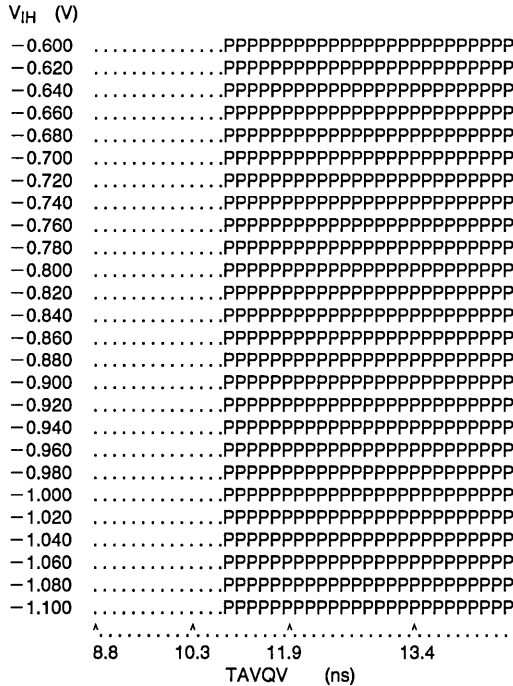


FIGURE 5. Shmoo of 100K Device to 10K Input Levels

101K

Besides temperature compensation, the other main difference between 10K and 100K logic is the recommended supply voltage; -4.2V to -4.8V for 100K, and -4.94V to -5.46V for 10K. However, National's 100K SRAMs will perform just as well at $-5.2\text{V} \pm 5\%$ since they are fully voltage and temperature compensated.

The use of 100K parts at 10K supplies is commonly referred to as 101K. In fact using the 100K BiCMOS SRAMs at the higher supply voltage will yield better speed (8% decrease in TAVQV), increased alpha particle immunity (from 76 FIT at -4.5V to 9 FIT at -5.2V), at only approximately a 16% power increase.

SYSTEM DESIGN CONSIDERATIONS

100K and 10K logic can be used in the same circuit if the necessary tradeoffs are understood. It has already been mentioned that the system temperature be kept below 35°C when driving 10K inputs with 100K outputs. The reason for this is for increased noise margin. There are several key factors to controlling system noise: the use of decoupling capacitors, ground planes, and matching termination impedance. Current spikes from outputs switching are a major cause of noise on V_{CC} . Bypass capacitors between V_{CC} and V_{EE} and between V_{CC} and V_{TT} (termination voltage of -2.0V) will help absorb or source current as needed to reduce the transient spikes. Capacitor values of $0.01 \mu\text{F}$ to $0.1 \mu\text{F}$ are recommended and one capacitor per chip

should be used. The use of a dedicated ground plane should be employed in the multilayer board where the chips are mounted. The importance of a dedicated ground plane is in reducing the resistance in the V_{CC} lines. Since V_{IL} , V_{IH} and V_{BB} are all referenced to V_{CC} , this will directly affect the noise margin (Figure 6). When possible, two ground planes should be used. One should be used for V_{CC} , which is the high supply for all the logic internal to the chip, and another separate plane should be used for V_{CCQ} , which provides a separate ground path for the switching output current. In this case decoupling capacitors should be used between V_{CC} and V_{EE} and between V_{CCQ} and V_{TT} . Also important is the use of an AC ground to minimize crosstalk. An AC ground can be any DC signal; V_{EE} or V_{TT} for example. These AC grounds should run between any parallel signal lines. Finally all signal lines should be terminated to reduce reflections which can cause signal errors. Since ECL outputs do not have internal pull down resistors, a terminating resistor to a voltage more negative than V_{OL} ($V_{TT} = -2.0\text{V}$ is recommended) should be used. The terminating resistor should match the impedance of the transmission line, otherwise the reflection voltage will be

$$V_R = V_{OUT} \left[\frac{R_t - Z_0}{R_t + Z_0} \right]$$

where R_t is the termination resistance and Z_0 is the line impedance. The output levels are specified at $R_t = 50\Omega$. A much more detailed discussion of transmission line theory can be found in reference 1.

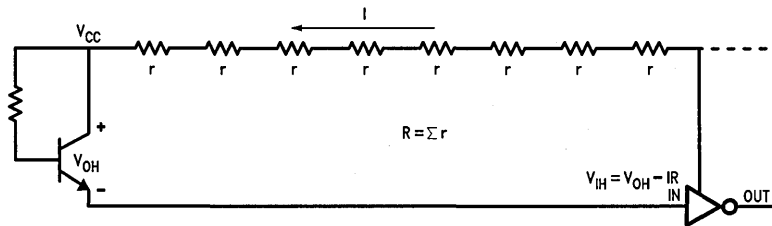


FIGURE 6. Reduced Voltage Margin Due to Resistive V_{CC} Line

TL/D/10576-5

CASE HISTORY

A major customer has been successfully using National's 256k x 1 BiCMOS 100K I/O SRAM in their 10K I/O system for over a year now. Their secret was to follow the basic formula outlined above: they used one 0.01 μ F decoupling capacitor per memory chip, had a solid ground plane, and had matching termination impedance of 50 Ω or 100 Ω for all signal lines. They also have taken advantage of the speed and alpha improvement by using a -5.2V supply. Another noteworthy point is that this customer uses the DIP package, which is inherently noisier due to higher inductive leads than National's ceramic flat pack.

SUMMARY

When mixing the two ECL families, the following considerations must be taken into account. The two families have different V_{BB} input reference voltages which implies that when mixing I/O types, the system temperature must

be monitored. Special attention must be given to V_{OH} margin at higher temperatures when 100K outputs drive 10K inputs. As well, soft saturation may occur at hot when 10K outputs drive 100K inputs, although National's BiCMOS SRAMs do not suffer speed degradation in such a case. In addition, allowing enough noise margin through proper decoupling, termination and supply of ground planes is always important. Another option available to system designers is 101K which uses 10K supply levels but has 100K I/O. By being aware of all these guidelines, the fastest silicon logic (ECL) together with the density and drive capability of BiCMOS can be used together in either mix or match 10K or 100K systems.

REFERENCES

1. Matick, R., *Transmission Lines for Digital and Communication Networks*, McGraw-Hill, (1969).

Terminating F100K ECL Inputs

National Semiconductor
Application Note 682
The ECL Applications Staff



INTRODUCTION

Many F100K designs require that certain inputs be preset to a HIGH or LOW level. Because of the construction of the F100K input circuitry, a LOW can be realized by simply leaving the input OPEN. However, a HIGH must be terminated in a special way, as simply tying the input to V_{CC}/V_{CCA} is unacceptable.

DESIGN CONSIDERATIONS

The ranges of V_{IH} and V_{IL} at $V_{EE} = -4.5V$ are $-880 mV$ to $-1165 mV$ and $-1475 mV$ to $-1810 mV$ respectively.

By staying within these ranges, the input conditions are assured. *Figure 1* shows the voltage versus current for the F100K input transistor. If the input is tied to V_{CC}/V_{CCA} the input transistor saturates (Point D) which can damage internal circuitry. The best V_{IH} to realize a HIGH is a voltage drop of $0.9V$ below V_{CC}/V_{CCA} . As can be seen from the graph, this locates the quiescent point on the flat part of the curve (Point C) midway within the acceptable range of V_{IH} . *Figure 2* shows three ways in which a HIGH can be realized on the input. These circuits allow the user to maintain constant input signals at optimum levels of V_{EE} and temperature. Each circuit can handle multiple fanouts, the number depending upon the maximum current capability of the circuit. The designer should be aware that although *Figures 2A*, *2B* and *2C*

supply ECL compatible signal levels, they differ in power consumption and susceptibility to changes in temperature and V_{EE} .

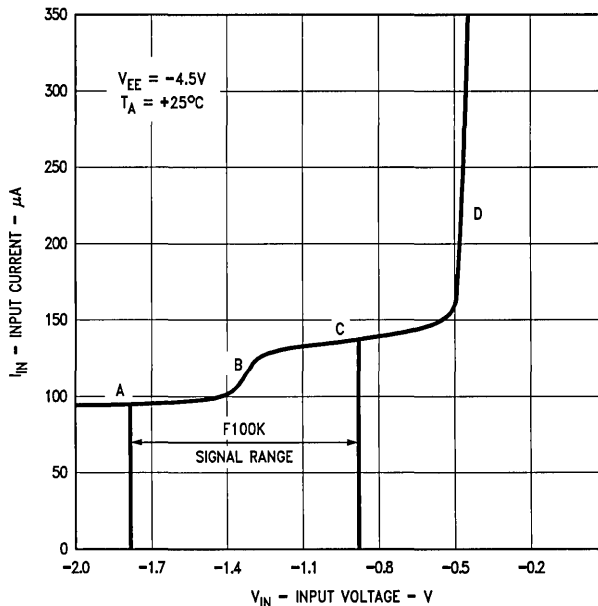
For designs where there are multiple unused inputs and extra logic gates available, fanout from the unused gates is possible. As an example of this, one gate of the F100102 is capable of driving ten quiescent inputs at voltage and current levels typical of F100K as shown in *Figure 3*.

Figure 4 shows, in more detail, the F100K pull-up scheme and the input circuitry. Although the circuits of *Figure 2* are good examples, a detailed circuit analysis must include the $50 k\Omega$ input resistor. In *Figure 4A*, the resistor (R_D) which sets the diode biasing current is in parallel with the $50 k\Omega$ input resistor. Likewise, the circuit of *Figure 4B* shows that R_2 is in parallel with the input resistor.

The point to emphasize is never tie an F100K input to V_{CC}/V_{CCA} in order to realize a HIGH preset. Instead, the following is recommended:

- For a LOW level—leave input open or tie to V_{EE} .
- For a HIGH level—tie input to a diode drop or $0.9V$ below V_{CC}/V_{CCA} .

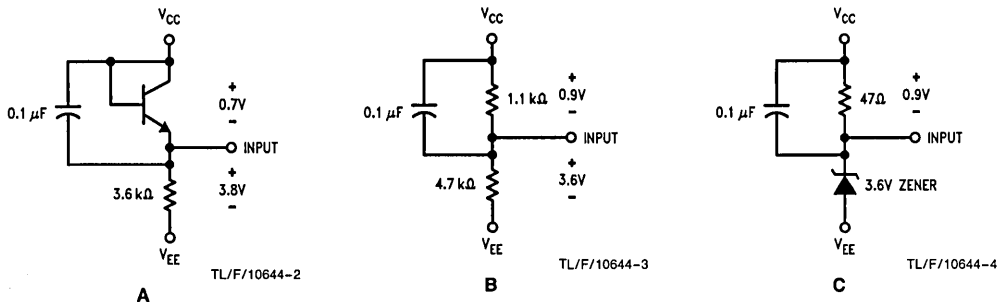
Remember also that the $50 k\Omega$ input resistor must be considered in the circuit parameter calculations.



A— $50 k\Omega$ Pull-Down Current
B—Transition (Switching) Region
C—Base Current plus $50 k\Omega$
D—Input Transistor Saturation

TL/F/10644-1

FIGURE 1. Input Characteristics



Note: Nominal values are shown.

FIGURE 2. Equivalent Circuits for HIGH Termination

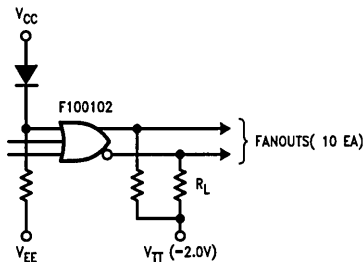


FIGURE 3. Utilizing Unused Gates to Terminate Multiple HIGHs and LOWs

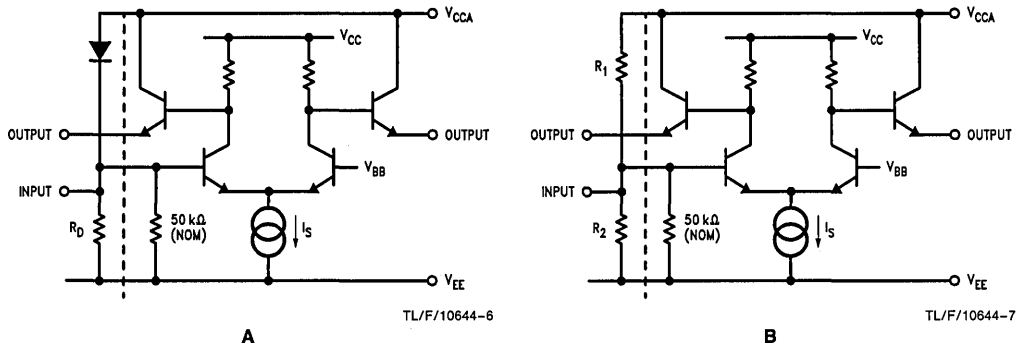


FIGURE 4. Pull-Up Circuit Examples

300 MHz Dual Eight-Way Multiplexer/Demultiplexer

National Semiconductor
 Application Note 683
 The ECL Applications Staff



INTRODUCTION

High speed multiplexing and demultiplexing is an integral part of the fast expanding telecommunications market, and can be used successfully in inter-computer and intra-computer wide-path communications. The National family of F100K ECL components provides an excellent solution to this design problem. This applications note describes a data transmission scheme that can transfer information at the rate of 75 Mbytes per second using only four twisted pair transmission lines.

Using F100341 8-Bit Shift Registers as parallel to serial and serial to parallel converters it is possible to design a simple

mux/demux that can operate at speeds as high as 300 MHz (*Figure 1*). The data to be multiplexed onto the transmission lines are applied as 16 bits (2 bytes) in parallel to the inputs of the F100341s where they are loaded into the registers under control of a synchronization pulse (SYNC). The mode of the F100341s is then changed to shift right and the data is transmitted on the output lines at the clock rate. When the last bit has been shifted out, the register is loaded with the next data to be transmitted.

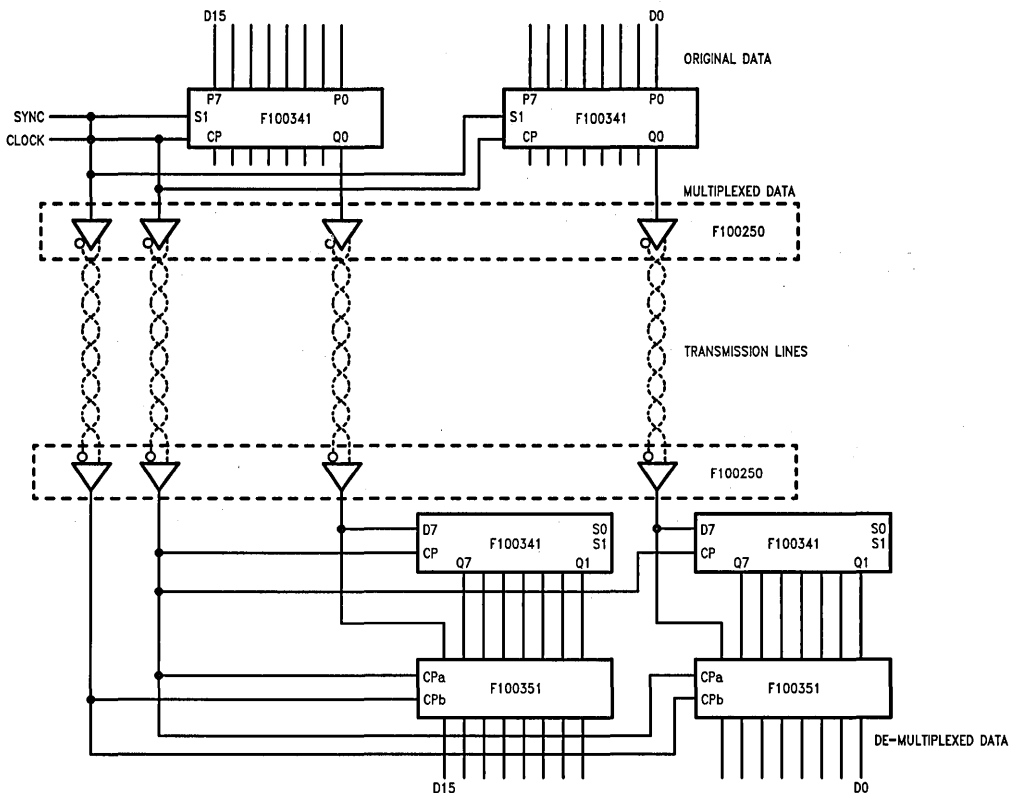


FIGURE 1. 300 MHz Dual Eight-Way Multiplexer/Demultiplexer

TL/F/10645-1

The clock signal (CLOCK) is a free-running 300 MHz square wave and the synchronization signal (SYNC) goes low for one clock cycle in every eight. These two signals are transmitted along with the data to facilitate synchronized reception at the other end.

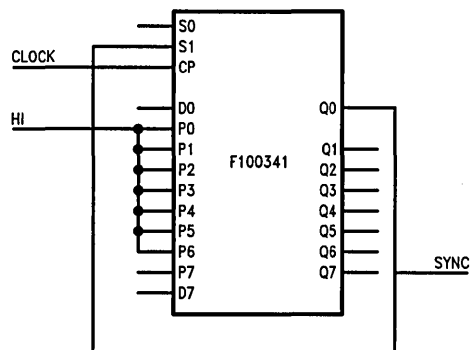
At the receiving end, the F100341s are used as simple shift registers that accomplish the task of demultiplexing the data. The SYNC signal controls the loading of the F100351 receiver registers.

CLOCK AND SYNC GENERATION

The CLOCK signal in this application is a 300 MHz square wave generated with a voltage controlled oscillator coupled with a phase-locked loop. However, any available clock signal may be used at a frequency of DC to 300 MHz.

The SYNC signal is generated with the use of another F100341 connected as in *Figure 2*. This circuit is self starting, requiring no initialization for proper operation. When

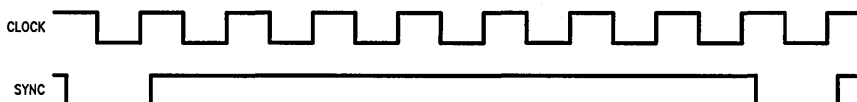
the SYNC signal is low, the data present at the parallel load inputs (P0–P7) are loaded into the register on the next clock pulse. When SYNC goes high (as a result of loading the high value on P0), the mode of the F100341 is changed to shift right and the low loaded from P7 is shifted across the F100341 and appears on the SYNC wire eight cycles later. This in turn causes the F100341 to load again and the cycle repeats. The SYNC signal is high for seven clock cycles and low for one cycle, allowing it to be used as the synchronization pulse for the mux/demux circuit.



TL/F/10645-2

FIGURE 2. SYNC Pulse Generator

CLOCK AND SYNC WAVEFORMS



TL/F/10645-3

F100336 Four-Stage Counter/Shift Register

National Semiconductor
Application Note 684
ECL Applications Staff



INTRODUCTION

Many system designs require bi-directional counting and shifting functions. In most cases these functions are separate and unique requirements within the system design. For this reason, separate catalog parts are available. In some cases however, there is a requirement to have a device that will allow both counting and shifting functions. This is especially true in arithmetic, timing, sequential, or communication applications. National offers a very versatile counter/shift register in the F100336. This application note describes its function in detail and offers some simple uses.

DESCRIPTION

The F100336 contains four synchronous, presettable flip-flops. Synchronous operation is provided by having all flip-flops clocked simultaneously so that all output changes coincide. This mode of operation eliminates counting spikes on the outputs which are normally associated with asynchronous counters. The clock input is buffered and triggers the four flip-flops on the rising (positive-going) edge.

The counters are fully programmable allowing the outputs to be set to either a HIGH (1) or LOW (0). As presetting is synchronous, setting low levels on the select inputs (S_0 - S_2) (see Table I) disables the counter and causes the outputs to agree with the parallel inputs (P_3 - P_0) on the next rising edge of the clock. Loading is accomplished regardless of the levels of the two enables (\overline{CEP} , \overline{CET}).

TABLE I. Function Select Table

| S_2 | S_1 | S_0 | Function |
|-------|-------|-------|---------------|
| L | L | L | Parallel Load |
| L | L | H | Complement |
| L | H | L | Shift Left |
| L | H | H | Shift Right |
| H | L | L | Count Down |
| H | L | H | Clear |
| H | H | L | Count Up |
| H | H | H | Hold |

The F100336 features both synchronous and asynchronous clear functions. The synchronous clear is performed by setting a binary five (101B) at the select inputs. On the next rising edge of the clock, the outputs will be forced LOW (0000) regardless of the levels at the enable inputs. A buffered asynchronous master reset (MR) is provided to clear all outputs LOW (0000) regardless of the levels of the clock, select, or enable inputs.

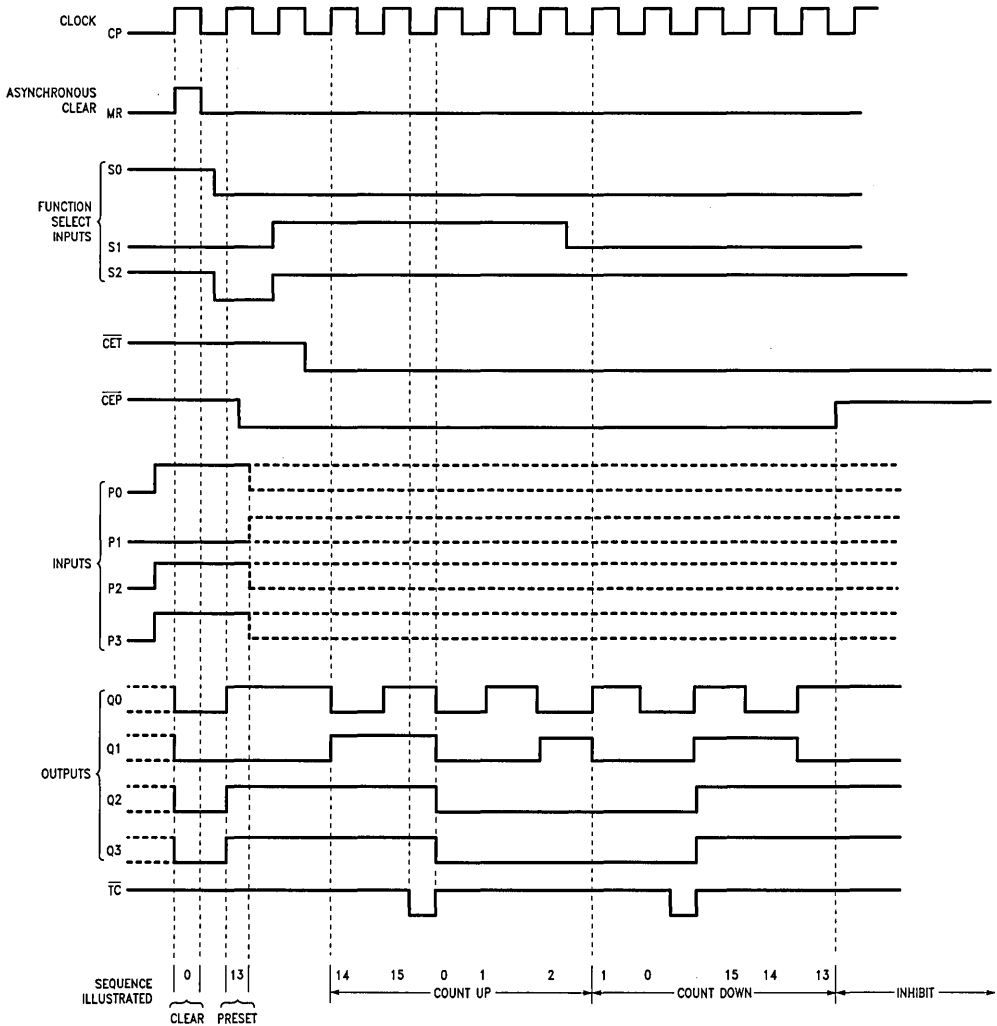
Count up/count down functions are selected with the select inputs (S_2 - S_0). These are synchronous operations and the outputs will increment/decrement in value on the rising edge of the clock. Both count enable inputs (\overline{CEP} , \overline{CET}) must be true (LOW) to count. The terminal count output (\overline{TC}) becomes active-LOW when the count reaches zero in the DOWN mode or fifteen in the UP mode. Its duration is approximately equal to one period of the clock. The \overline{TC} output is not recommended for use as a clock or synchronous reset for flip-flops. See Figure 1 for timing relationships in UP/DOWN counting.

In simple ripple-carry cascading applications the terminal count \overline{TC} is fed forward to enable the trickle enable (\overline{CET}) input. This method is increasingly inefficient as the counting chain lengthens. The upper limit of the clock frequency is determined by the clock-to-terminal-count delay of the first stage, the cumulative trickle-enable (\overline{CET})-to-terminal-count delay of the intermediate stages, and the trickle-enable-to-clock delay of the last stage. For faster counting rates a carry-lookahead scheme is necessary. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to change over from MAX to MIN in the UP mode, or from MIN to MAX in the DOWN mode. Since the final count cycle takes 16 clocks to complete, there is ample time for the ripple to propagate through the intermediate stages. The critical timing that limits the counting rate is the clock-to-terminal-count of the first stage plus the parallel-enable-to-clock (\overline{CEP}) setup time of the last stage. Figure 2 shows the connections for the fast-carry counting scheme.

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (Preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
5. Inhibit counting.



Note: A MR overrides enables, data, and count inputs.

TL/F/10646-1

FIGURE 1. F100336 Used as Binary Up/Down Counter

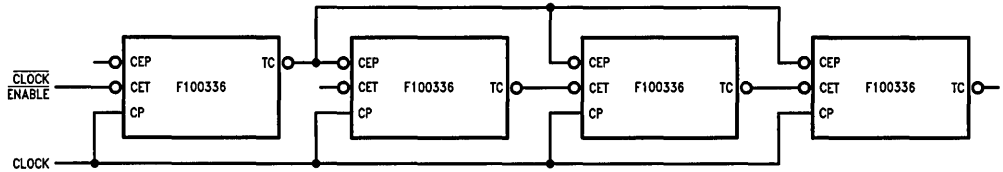


FIGURE 2. Fast Carry Counting Scheme

TL/F/10646-2

Shift right/left modes are performed by making the appropriate selection on the selection inputs (S_2-S_0). Each rising edge of the clock will cause the outputs to shift once in the direction which is selected. For shift-left operation, input D_3 is used as the serial input. For shift-right operation, input \overline{CET}/D_0 is used as the serial input. During shift operation the terminal count output reflects the level at the Q_3 output and the enables are "don't cares". See Figure 3 for shift operation timing relationships and shift sequences.

The F100336 provides two special modes of operation. The complement mode performs a one's complement of the outputs (Q_3-Q_0) on the rising edge of the clock input regardless of the levels at the enable inputs. The hold feature is asynchronous and simply stops counting or shifting operations. Both complement and hold are performed with proper selection of the select inputs. For a complete truth table of the F100336 operation, refer to Table II.

DESIGN CONSIDERTIONS

Presetting the parallel inputs (P_3-P_0) may require a mixture of HIGH's and LOW's. A LOW may be preset by leaving the respective input open as the F100336 has a 50 k Ω resistor to V_{EE} on the parallel inputs. A HIGH must never be made by tying the input to V_{CC}/V_{CCA} . This saturates the input transistor. Instead the input is set at a diode drop below V_{CC}/V_{CCA} for a preset HIGH.

Unused output pairs (\overline{Q}_n/Q_n) may be left unterminated. However, unused single outputs should be terminated to balance current switching in the outputs. For further details on system design considerations refer to the *F100K ECL Design Guide*. For AC/DC performance specifications and critical timing parameters refer to the F100336 datasheet.

APPLICATIONS

Figures 4 and 5 demonstrate the use of the F100336 as UP/DOWN BCD counters. One additional gate is required to detect the limit count. Notice the alternate gate methods in Figure 4. The F100304 shows the classical AND/NAND design similar to TTL and the F100302 shows the OR/NOR design of ECL.

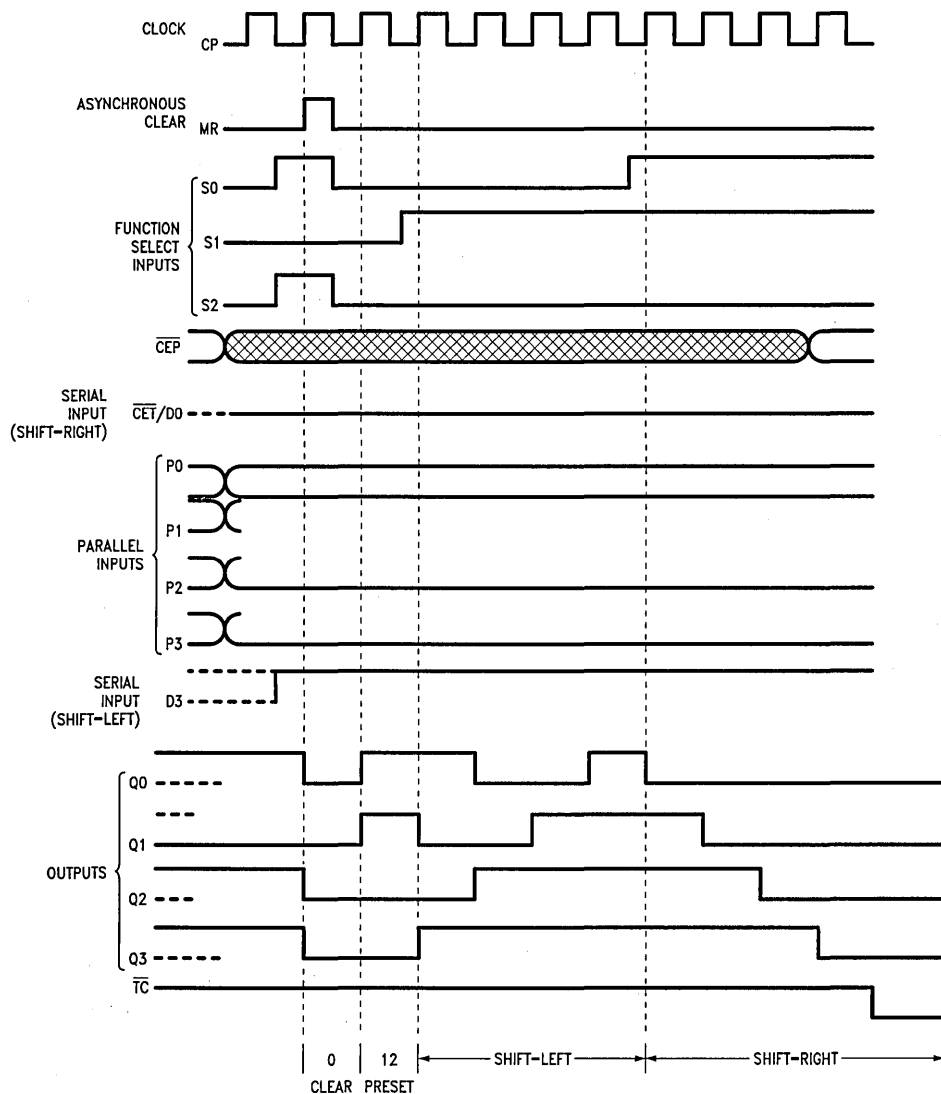
Figure 6 incorporates the use of a F100331 triple D-type flip-flop. By using one stage of the F100331, a 50/50 duty cycle can be realized from the divider.

An 8-bit parallel-to-serial shifter can be constructed by cascading two F100336's as shown in Figure 7. The third counter reloads another 8-bit data word after eight serial counts.

TYPICAL, CLEAR, LOAD, AND COUNT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary twelve.
3. Shift-left using D_3 as serial input.
4. Shift-right using \overline{CET}/D_0 as serial input.



- Note 1:** In shift-right mode \overline{TC} follows the Q_3 output.
Note 2: In shift-left mode \overline{TC} follows the D_3 input.
Note 3: \overline{CET} is a "don't care" during shifting.

FIGURE 3. F100336 Used as Bi-Directional Shift Register

TL/F/10646-3

Truth Table

Q₀ = LSB

TABLE II. Truth Table

| Inputs | | | | | | | | Outputs | | | | | Mode |
|--------|----------------|----------------|----------------|-------------------------|---------------------|----------------|----|---|-------------------------|-------------------------|-------------------------|------------------|--|
| MR | S ₂ | S ₁ | S ₀ | $\overline{\text{CEP}}$ | D ₀ /CET | D ₃ | CP | Q ₃ | Q ₂ | Q ₁ | Q ₀ | TC | |
| L | L | L | L | X | X | X | ↗ | P ₃ | P ₂ | P ₁ | P ₀ | L | Preset (Parallel Load) |
| L | L | L | H | X | X | X | ↗ | $\overline{\text{Q}}_3$ | $\overline{\text{Q}}_2$ | $\overline{\text{Q}}_1$ | $\overline{\text{Q}}_0$ | L | Invert |
| L | L | H | L | X | X | X | ↗ | D ₃ | Q ₃ | Q ₂ | Q ₁ | D ₃ | Shift Left |
| L | L | H | H | X | X | X | ↗ | Q ₂ | Q ₁ | Q ₀ | D ₀ | Q ₃ * | Shift Right |
| L | H | L | L | L | L | X | ↗ | (Q ₀ -Q ₃) minus 1 | | | | ⊖ | Count Down |
| L | H | L | L | H | L | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | ⊖ | Count Down with $\overline{\text{CEP}}$ not active |
| L | H | L | L | X | H | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Count Down with $\overline{\text{CET}}$ not active |
| L | H | L | H | X | X | X | ↗ | L | L | L | L | H | Clear |
| L | H | H | L | L | L | X | ↗ | (Q ₀ -Q ₃) plus 1 | | | | ⊕ | Count Up |
| L | H | H | L | H | L | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | ⊕ | Count Up with $\overline{\text{CEP}}$ not active |
| L | H | H | L | X | H | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Count Up with $\overline{\text{CET}}$ not active |
| L | H | H | H | X | X | X | X | Q ₃ | Q ₂ | Q ₁ | Q ₀ | H | Hold |
| H | L | L | L | X | X | X | X | L | L | L | L | L | Asynchronous Master Reset |
| H | L | L | H | X | X | X | X | L | L | L | L | L | |
| H | L | H | L | X | X | X | X | L | L | L | L | L | |
| H | L | H | H | X | X | X | X | L | L | L | L | L | |
| H | H | L | L | X | L | X | X | L | L | L | L | L | |
| H | H | L | L | X | H | X | X | L | L | L | L | L | |
| H | H | L | H | X | X | X | X | L | L | L | L | L | |
| H | H | H | L | X | X | X | X | L | L | L | L | L | |
| H | H | H | H | X | X | X | X | L | L | L | L | L | |

- ⊖ = L if Q₀-Q₃ = LLLL
H if Q₀-Q₃ ≠ LLLL
- ⊕ = L if Q₀-Q₃ = HHHH
H if Q₀-Q₃ ≠ HHHH
- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Don't Care
- ↗ = LOW-to-HIGH Transition

*Before the clock, TC is Q₃
After the clock, TC is Q₂

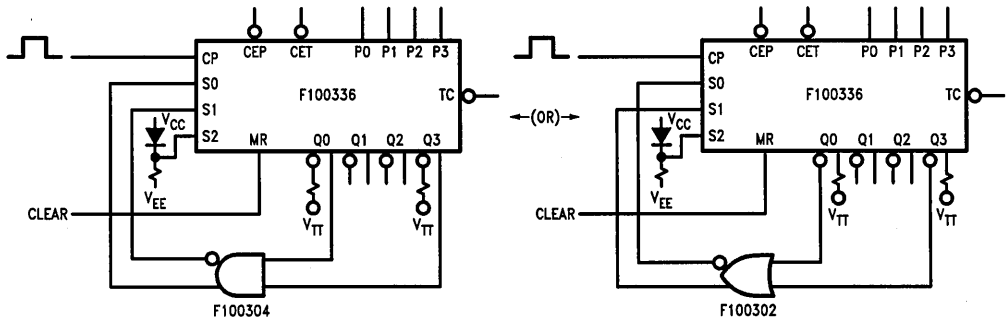


FIGURE 4. BCD Up Counter (0-9)

TL/F/10646-4

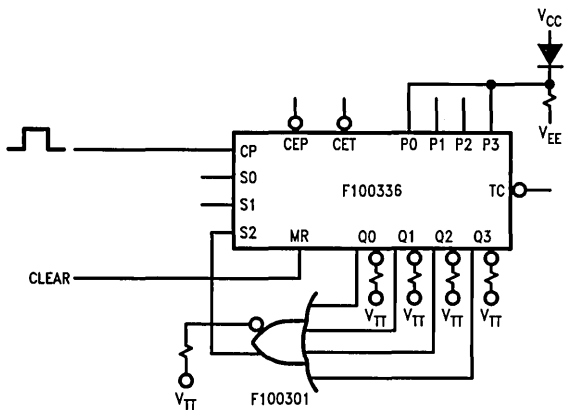


FIGURE 5. BCD Down Counter (9-0)

TL/F/10646-5

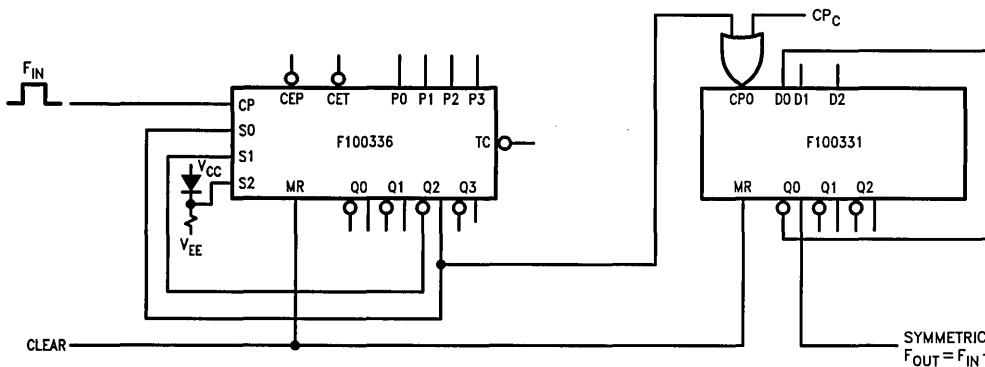


FIGURE 6. Divide by Five

SYMMETRICAL
 $F_{OUT} = F_{IN} \div 5$

TL/F/10646-6

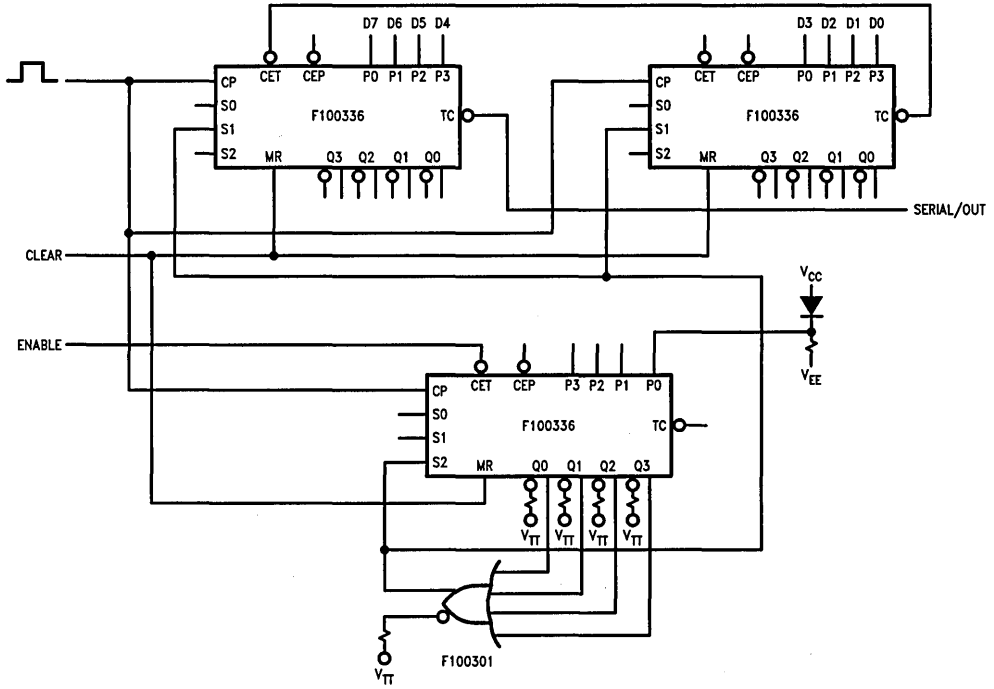


FIGURE 7. 8-Bit Shift Left

TL/F/10646-7

Using the F100181 ALU and F100179 Carry-Lookahead

National Semiconductor
Application Note 685
ECL Applications Staff



INTRODUCTION

Speed is of paramount importance in the arithmetic unit of a system design. The National F100181 Arithmetic Logic Unit (ALU) in conjunction with the F100179 Carry-Lookahead offer a high-performance and efficient design solution. Besides the obvious performance benefits, they offer both temperature and voltage compensation which leads to better performance stabilization throughout the guaranteed ranges. Better noise immunity over TTL devices and more efficient designs by using wired-OR logic and complementary outputs are also benefits offered by these devices. This application note describes the function of the F100181 and F100179, offers configurations for their use, and gives a detailed timing analysis of the function settling times.

F100181 FUNCTIONAL DESCRIPTION

The F100181 is an ALU capable of performing sixteen arithmetic and logic operations on two 4-bit words. The operating mode is selected by four function-select lines (S_3-S_0). Arithmetic operations are selected when S_3 is LOW, and logic operations are selected when S_3 is HIGH. When S_3 is LOW, the arithmetic mode can be selected between binary and binary coded decimal (BCD) with the S_2 input [S_2 is LOW (BCD); S_2 is HIGH (binary)]. The remaining function-select inputs S_1, S_0 select between addition, subtraction, and the basic logical operations (refer to Table I).

Provision for simple ripple-carry cascading is available with the carry output ($C_n + 4$). A carry unit (C_n) is provided for use with arithmetic operations. In BCD mode, it can be used to perform a ten's complement result in subtraction. Likewise, in binary mode, it can be used to perform a two's complement result in subtraction.

A full carry-lookahead scheme is implemented for fast, simultaneous group carry generation by means of propagate (\bar{P}) and generate (\bar{G}) carries. When used in conjunction with the F100179 carry-lookahead generator, high-speed arithmetic operations can be performed. Table II presents the equations for internal carry-lookahead and $C_n + 4, P, \bar{G}$ for the F100181. Refer to the data sheet on the F100181.

F100179 FUNCTIONAL DESCRIPTION

The F100179 is a high-speed, carry-lookahead generator capable of anticipating a carry across eight 4-bit adders/ALU's. Carry, generate carry, and propagate carry functions are provided to perform full carry-lookahead across n-bit words. Table III presents the four carry output equations. For detailed AC/DC specifications, refer to the F100179 data sheet.

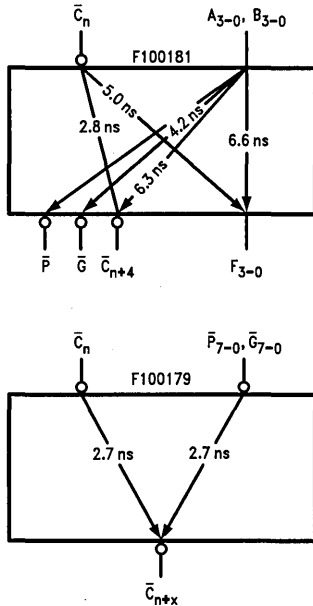
TABLE I. F100181 Carry Output Equations

| S_3 | S_2 | S_1 | S_0 | F_n Function | G_n | P_n | Outputs | | |
|-------|-------|-------|-------|---|------------------|-------------------------|-----------|-------------|-----------|
| | | | | | (n = 0 to 3) | (n = 0 to 3) | $C_n + 4$ | \bar{G} | \bar{P} |
| | | | | | Internal Signals | | $C_n + 4$ | \bar{G} | \bar{P} |
| L | L | L | L | $F_n = A \text{ Plus } B \text{ Plus } C_n \text{ (BCD)}$ | $A_n D_n$ | $A_n + D_n$ | $C_n + 4$ | \bar{G} | \bar{P} |
| L | L | L | H | $F_n = A \text{ Minus } B \text{ Plus } C_n \text{ (BCD)}$ | $A_n \bar{B}_n$ | $A_n + \bar{B}_n$ | $C_n + 4$ | \bar{G} | \bar{P} |
| L | L | H | L | $F_n = B \text{ Minus } A \text{ Plus } C_n \text{ (BCD)}$ | $\bar{A}_n B_n$ | $\bar{A}_n + B_n$ | $C_n + 4$ | \bar{G} | \bar{P} |
| L | L | H | H | $F_n = 0 \text{ Minus } B \text{ Plus } C_n \text{ (BCD)}$ | L | \bar{B}_n | $C_n + 4$ | H | \bar{P} |
| L | H | L | L | $F_n = A \text{ Plus } B \text{ Plus } C_n \text{ (Binary)}$ | $A_n B_n$ | $A_n + B_n$ | $C_n + 4$ | \bar{G} | \bar{P} |
| L | H | L | H | $F_n = A \text{ Minus } B \text{ Plus } C_n \text{ (Binary)}$ | $A_n \bar{B}_n$ | $A_n + \bar{B}_n$ | $C_n + 4$ | \bar{G} | \bar{P} |
| L | H | H | L | $F_n = B \text{ Minus } A \text{ Plus } C_n \text{ (Binary)}$ | $\bar{A}_n B_n$ | $\bar{A}_n + B_n$ | $C_n + 4$ | \bar{G} | \bar{P} |
| L | H | H | H | $F_n = 0 \text{ Minus } B \text{ Plus } C_n \text{ (Binary)}$ | L | \bar{B}_n | $C_n + 4$ | H | \bar{P} |
| H | L | L | L | $F_n = A_n B_n + \bar{A}_n \bar{B}_n$ | $A_n B_n$ | $A_n + B_n$ | $C_n + 4$ | \bar{G} | \bar{P} |
| H | L | L | H | $F_n = A_n \bar{B}_n + \bar{A}_n B_n$ | $A_n \bar{B}_n$ | $A_n + \bar{B}_n$ | $C_n + 4$ | \bar{G} | \bar{P} |
| H | L | H | L | $F_n = A_n + B_n$ | A_n | \bar{B}_n | $C_n + 4$ | \bar{G}_x | \bar{P} |
| H | L | H | H | $F_n = A_n$ | A_n | H | $C_n + 4$ | \bar{G} | L |
| H | H | L | L | $F_n = \bar{B}_n$ | L | B_n | L | H | \bar{P} |
| H | H | L | H | $F_n = B_n$ | L | \bar{B}_n | L | H | \bar{P} |
| H | H | H | L | $F_n = A_n B_n$ | L | $\bar{A}_n + \bar{B}_n$ | L | H | \bar{P} |
| H | H | H | H | $F_n = \text{LOW}$ | L | H | L | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level

APPLICATIONS

Logic symbol representations of the F100179 and F100181 are shown in *Figure 1* with propagation delay paths. The times shown are maximum values at nominal room temperature (25°C) and power supply voltage ($V_{EE} = -4.5V$) for a flatpak package. The propagation delays from the select inputs (F100181) are ignored since it is assumed that the mode of operation is set prior to application of the input word operands.



TL/F/10647-1

FIGURE 1. F100179/F100181 Propagation Delays

TABLE II. F100181 Carry Output Equations

$$\begin{aligned}\bar{P} &= \bar{P}_0 + \bar{P}_1 + \bar{P}_2 + \bar{P}_3 \\ \bar{G} &= \bar{G}_3 + \bar{P}_3\bar{G}_2 + \bar{P}_3\bar{P}_2\bar{P}_1 + \bar{P}_3\bar{P}_2\bar{P}_1\bar{G}_0 \\ \bar{C}_{n+4} &= \bar{G} \cdot (\bar{P} + \bar{C}_n)\end{aligned}$$

Internal Equations for Carry-Lookahead

(i = 0, 1, 2, 3)

$$C_0 = C_n + S_3$$

$$C_1 = G_0 + P_0C_n + S_3$$

$$C_2 = G_1 + P_1G_0 + P_1P_0C_n + S_3$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n + S_3$$

RIPPLE CARRY CALCULATION

Figure 2 shows the schematic for simple n-stage cascading, incorporating ripple carry. Regardless of the width of the adder, all stages have a sum and carry from the A, B inputs in 6.6 ns. However, this represents the true sum and carry for stage one. For each succeeding stage, the \bar{C}_n -to- \bar{C}_{n+4} and \bar{C}_n -to-F propagation delays must be considered. Therefore, for n-stages the total settling time for the function outputs during addition is:

$$t_{sum} = t_{[A, B, \text{to-F}]} + (n-2) t_{[\bar{C}_n \text{ to } \bar{C}_{n+4}]} + t_{[\bar{C}_n \text{ to-F}]}$$

A 32-bit wide adder requires eight stages ($n = 8$). The propagation time of the operand inputs (A, B) to the function outputs (F) of the first stage is 6.6 ns. The propagation time of the carry input (\bar{C}_n) to the function outputs of the last stage is 5.0 ns. Each middle stage has a propagation delay, \bar{C}_n to the carry output (\bar{C}_{n+4}), of 2.8 ns. The total settling time of the function outputs is then:

$$t_{sum} = 6.6 + (8-2)(2.8) + 5.0 = 28.4 \text{ ns}$$

Figure 3 shows graphically the settling times of each of the eight stages.

TABLE III. F100179 Carry Output Equations

$$\begin{aligned}\bar{C}_{n+2} &= \bar{G}_1 \cdot (\bar{P}_1 + \bar{G}_0) \cdot (\bar{P}_1 + \bar{P}_0 + \bar{C}_n) \\ \bar{C}_{n+4} &= \bar{G}_3 \cdot (\bar{P}_3 + \bar{G}_2) \cdot (\bar{P}_3 + \bar{P}_2 + \bar{G}_1) \cdot (\bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{G}_0) \\ &\quad \cdot (\bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{P}_0 + \bar{C}_n) \\ \bar{C}_{n+6} &= \bar{G}_5 \cdot (\bar{P}_5 + \bar{G}_4) \cdot (\bar{P}_5 + \bar{P}_4 + \bar{G}_3) \cdot (\bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{G}_2) \\ &\quad \cdot (\bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{G}_1) \cdot (\bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{G}_0) \\ &\quad \cdot (\bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{P}_0 + \bar{C}_n) \\ \bar{C}_{n+8} &= \bar{G}_7 \cdot (\bar{P}_7 + \bar{G}_6) \cdot (\bar{P}_7 + \bar{P}_6 + \bar{G}_5) \cdot (\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{G}_4) \\ &\quad \cdot (\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{G}_3) \cdot (\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{G}_2) \\ &\quad \cdot (\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{G}_1) \\ &\quad \cdot (\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{G}_0) \\ &\quad \cdot (\bar{P}_7 + \bar{P}_6 + \bar{P}_5 + \bar{P}_4 + \bar{P}_3 + \bar{P}_2 + \bar{P}_1 + \bar{P}_0 + \bar{C}_n)\end{aligned}$$

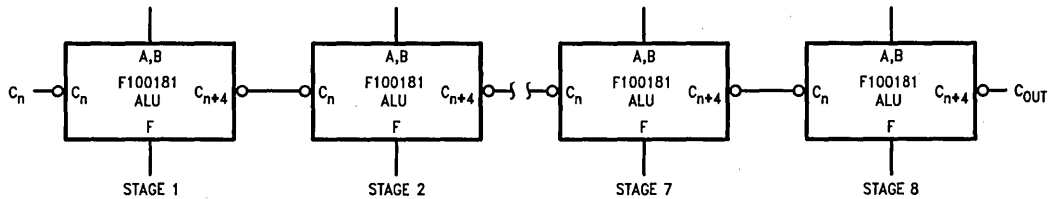


FIGURE 2. Ripple Carry

TL/F/10647-2

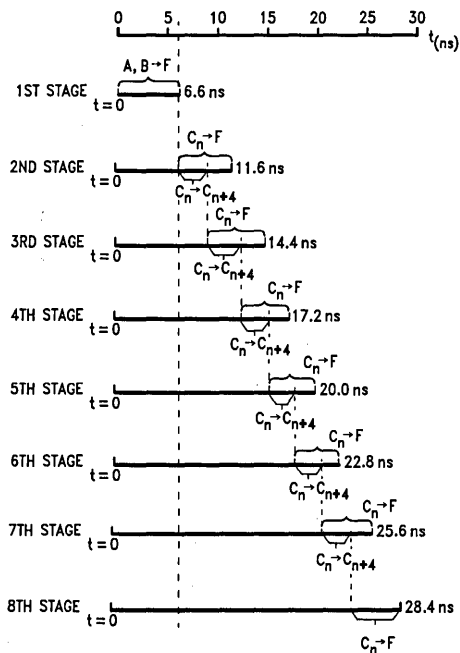


FIGURE 3. Timing Line Diagram for 32-Bit ALU

TL/F/10647-3

1-LEVEL CARRY-LOOKAHEAD CALCULATION

Figure 4 shows a 16-bit adder using one level of carry-lookahead for every two ALU's. The reason for this arrangement is that the F100179 does not provide every $\overline{C_{n+x}}$, but instead provides $\overline{C_{n+2}}$, $\overline{C_{n+4}}$, $\overline{C_{n+6}}$, and $\overline{C_{n+8}}$. One F100179 is capable of providing carry-lookahead for 32 bits. The timing line diagram for the 16-bit ALU with one level of carry-lookahead is given in Figure 5. The equation which describes each 32-bit stage is given by:

$$t_{sum} = t[A,B-to-P,G] + t[\overline{C_n-to-F}] + t[\overline{C_n-to-C_{n+4}}] + t[P,G-to-\overline{C_{n+2}}]$$

To expand this scheme past 32 bits (eight ALU's) requires that the adder be broken into 32-bit groups connected with ripple carries since group generate and propagate are not available from the F100179. Each 32-bit group past the first one adds one F100179 P, G-to- $\overline{C_{n+x}}$ time to establish the carry into the next 32-bit group. Figure 6 shows this method of interconnection.

FAST 16-Bit 1-Level Carry-Lookahead

Another method for implementing a 16-bit adder with faster carry propagation is shown in Figure 7. In this example, the full capability of the F100179 is used by forcing carry propagation through the odd-order stages. The carry outputs, $\overline{C_{n+x}}$, are then used to supply the appropriate carry bit to succeeding stages. The equation describing the critical path becomes:

$$t_{sum} = t[A,B-to-P,G] + t[P,G-to-\overline{C_{n+x}}] + t[\overline{C_n-to-F}]$$

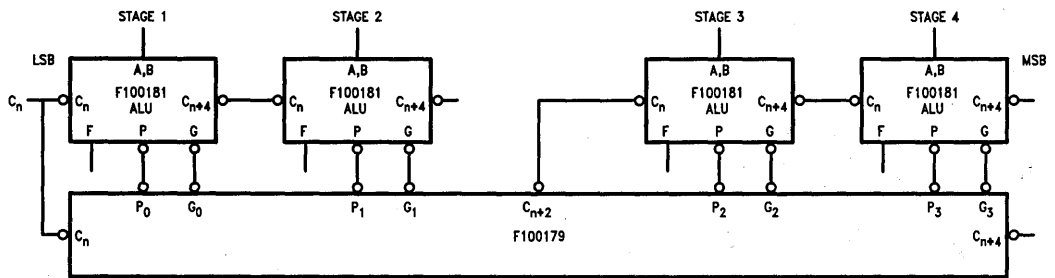


FIGURE 4. 1-Level Carry-Lookahead

TL/F/10647-4

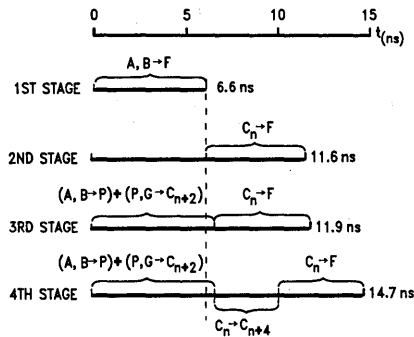


FIGURE 5. Timing Line Diagram for 16-Bit ALU with 1-Level Carry-Lookahead

TL/F/10647-5

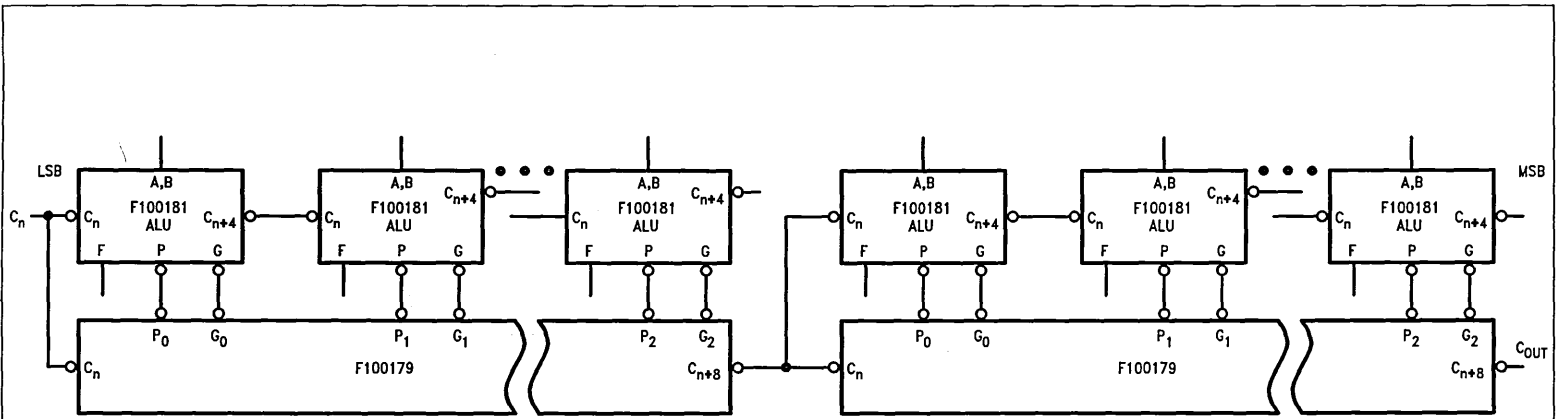


FIGURE 6. Expansion Past 32 Bits for 1-Level Carry-Lookahead

TL/F/10647-6

7-111

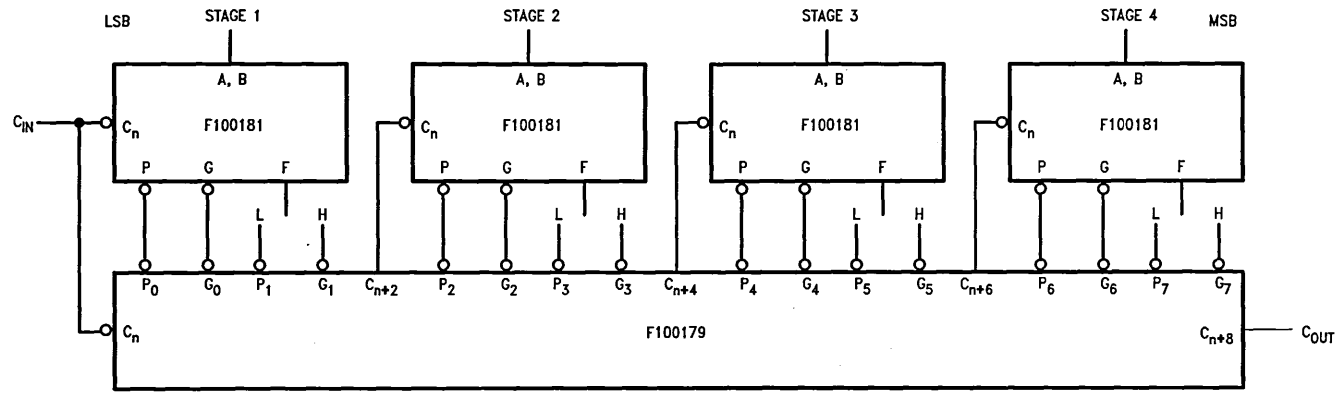
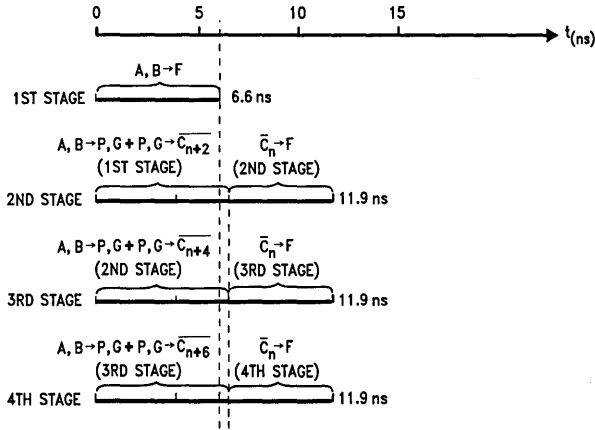


FIGURE 7. Fast 16-Bit 1-Level Carry-Lookahead

TL/F/10647-7



TL/F/10647-8

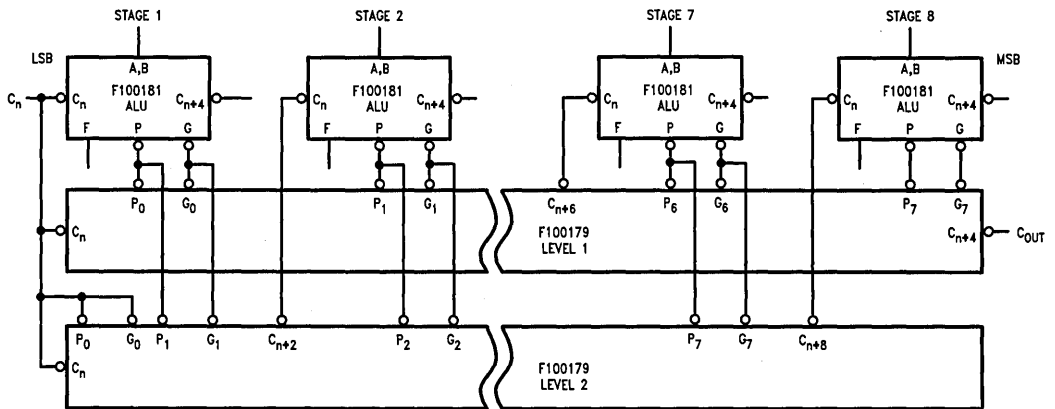
FIGURE 8. Timing Line Diagram For Fast 16-Bit 1-Level Carry-Lookahead

TWO-LEVEL CARRY-LOOKAHEAD CALCULATION

The word widths of 32 bits or more, a two-level carry-lookahead scheme like that shown in Figure 9 is preferred. One of the two F100179's generates a carry for the even-numbered ALU's; the other generates a carry for the odd-numbered ALU's. The timing line diagram for this method is given in Figure 10. The equation describing the 32-bit summation is:

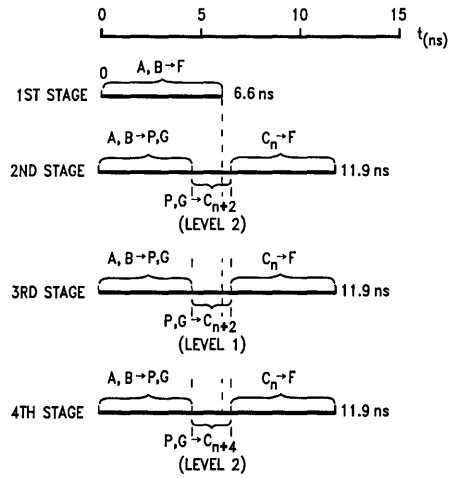
$$t_{sum} = t_{[A,B,to-P,G]} + t_{[P,G,to-C_n+x]} + t_{[C_n-to-F]}$$

This scheme can be expanded past 32 bits as in the previous case by interconnecting 32 bit groups with ripple carries. Each 32-bit group past the first adds one $t_{[P,G-to-C_n+x]}$ delay to the total add time. Table IV summarizes the add times for all three schemes discussed in this application note.



TL/F/10647-9

FIGURE 9. 2-Level Carry-Lookahead



TL/F/10647-10

FIGURE 10. Timing Line Diagram for 32-Bit ALU with 2-Level Carry-Lookahead

TABLE IV. Summary of Add Times

| Bits | Stages | with Ripple Carry (ns) | with (1) F100179 (ns) | with (2) F100179 (ns) |
|------|--------|------------------------------|-----------------------------|-----------------------------|
| 8 | 2 | 11.6 | n/a | n/a |
| 16 | 4 | 17.2 | 14.7 | 11.9 |
| 32 | 8 | 28.4 | 14.7 | 11.9 |
| 64 | 16 | 50.8 | 17.4 | 14.6 |



Section 8
**Ordering Information and
Physical Dimensions**



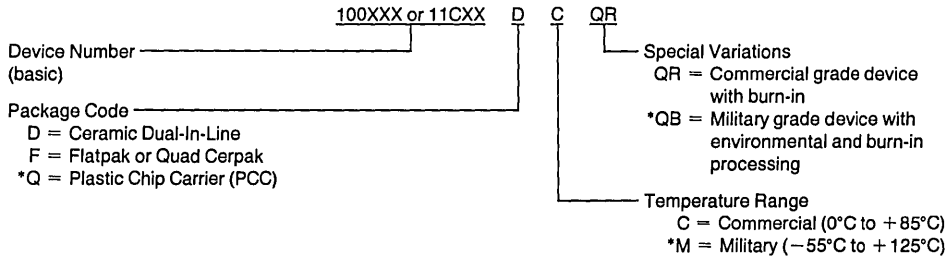
Section 8 Contents

| | |
|----------------------------|-----|
| Ordering Information | 8-3 |
| Physical Dimensions | 8-4 |
| Bookshelf | |
| Distributors | |

ORDER INFORMATION



The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

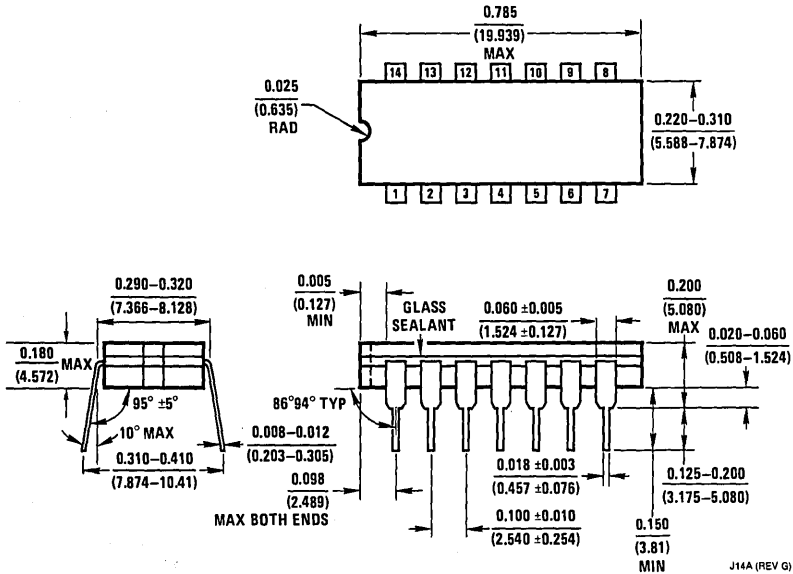


For most current packaging information, contact product marketing.



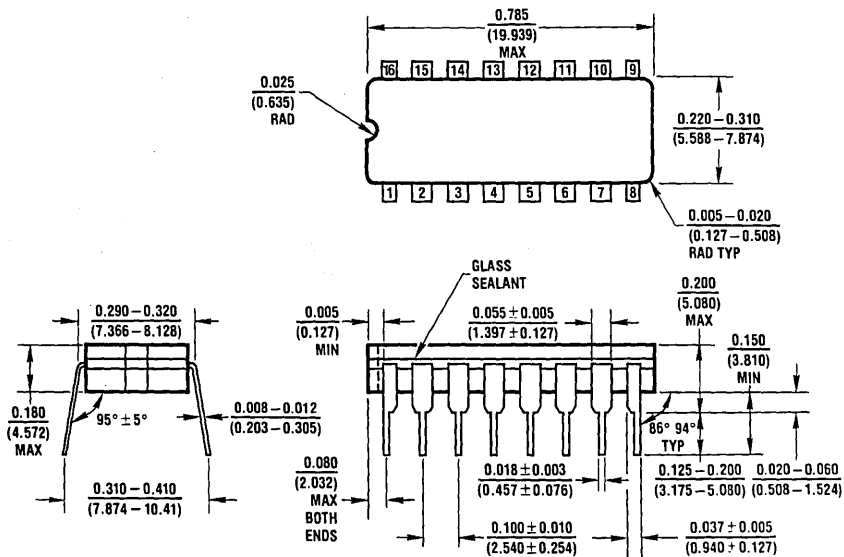
All dimensions are in inches (millimeters)

**14 Lead Ceramic Dual In-Line Package (D)
NS Package Number J14A**



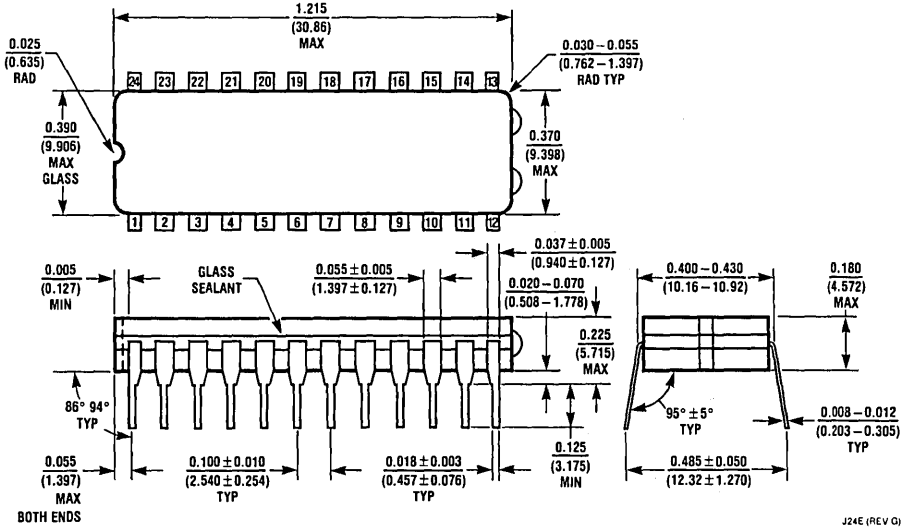
J14A (REV G)

**16 Lead Ceramic Dual In-Line Package (D)
NS Package Number J16A**

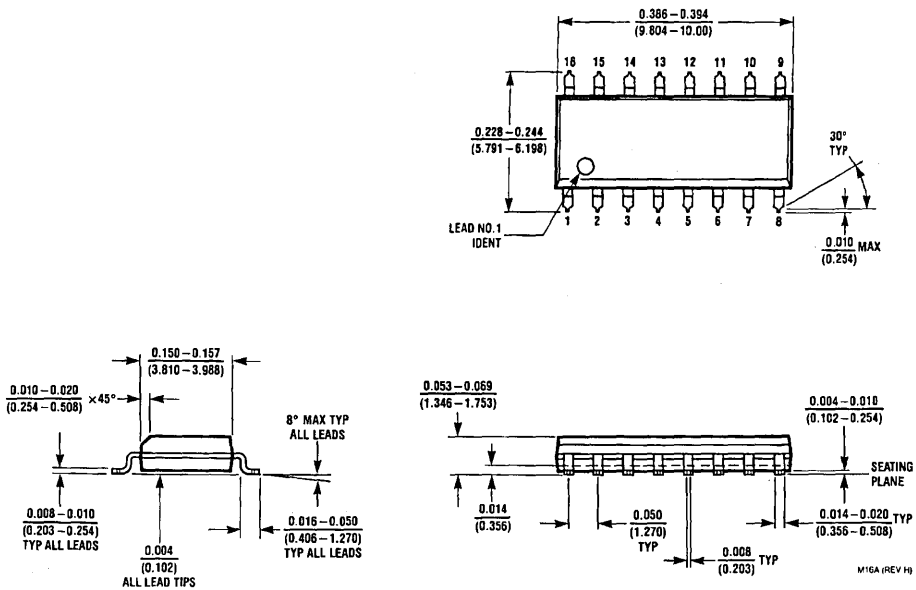


J16A (REV K)

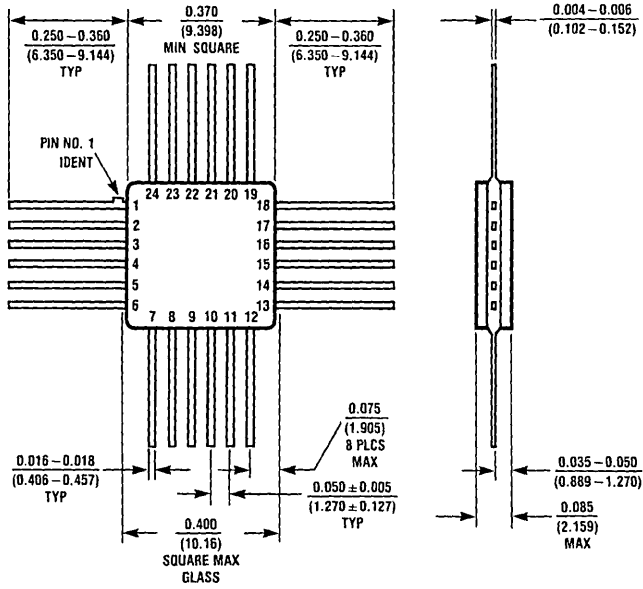
24 Lead Ceramic Dual In-Line Package (0.400" Wide) (D) NS Package Number J24E



16 Lead Small Outline Integrated Circuit (S) NS Package Number M16A



24 Lead Quad Cerpak (F) NS Package Number W24B



W24B (REV C)

NOTES

NOTES



Bookshelf of Technical Support Information

National Semiconductor Corporation recognizes the need to keep you informed about the availability of current technical literature.

This bookshelf is a compilation of books that are currently available. The listing that follows shows the publication year and section contents for each book.

Please contact your local National sales office for possible complimentary copies. A listing of sales offices follows this bookshelf.

We are interested in your comments on our technical literature and your suggestions for improvement.

Please send them to:

Technical Communications Dept. M/S 16-300
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090

ALS/AS LOGIC DATABOOK—1990

Introduction to Advanced Bipolar Logic • Advanced Low Power Schottky • Advanced Schottky

ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS—1987

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

CMOS LOGIC DATABOOK—1988

CMOS AC Switching Test Circuits and Timing Waveforms • CMOS Application Notes • MM54HC/MM74HC
MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

DATA ACQUISITION LINEAR DEVICES—1989

Active Filters • Analog Switches/Multiplexers • Analog-to-Digital Converters • Digital-to-Analog Converters
Sample and Hold • Temperature Sensors • Voltage Regulators • Surface Mount

DATA COMMUNICATION/LAN/UART DATABOOK—1990

LAN IEEE 802.3 • High Speed Serial/IBM Data Communications • ISDN Components • UARTs
Modems • Transmission Line Drivers/Receivers

DISCRETE SEMICONDUCTOR PRODUCTS DATABOOK—1989

Selection Guide and Cross Reference Guides • Diodes • Bipolar NPN Transistors
Bipolar PNP Transistors • JFET Transistors • Surface Mount Products • Pro-Electron Series
Consumer Series • Power Components • Transistor Datasheets • Process Characteristics

DRAM MANAGEMENT HANDBOOK—1989

Dynamic Memory Control • Error Detection and Correction • Microprocessor Applications for the
DP8408A/09A/17/18/19/28/29 • Microprocessor Applications for the DP8420A/21A/22A
Microprocessor Applications for the NS32CG821

EMBEDDED SYSTEM PROCESSOR DATABOOK—1989

Embedded System Processor Overview • Central Processing Units • Slave Processors • Peripherals
Development Systems and Software Tools

F100K DATABOOK—1990

Family Overview • 300 Series (Low-Power) Datasheets • 100 Series Datasheets • 11C Datasheets
ECL BiCMOS SRAM, ECL PAL, and ECL ASIC Datasheets • Design Guide • Circuit Basics • Logic Design
Transmission Line Concepts • System Considerations • Power Distribution and Thermal Considerations
Testing Techniques • Quality Assurance and Reliability • Application Notes

FACT™ ADVANCED CMOS LOGIC DATABOOK—1990

Description and Family Characteristics • Ratings, Specifications and Waveforms
Design Considerations • 54AC/74ACXXX • 54ACT/74ACTXXX • Quiet Series: 54ACQ/74ACQXXX
Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA

FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK—Rev. 1—1988

Circuit Characteristics • Ratings, Specifications and Waveforms • Design Considerations • 54F/74FXXX

FAST® APPLICATIONS HANDBOOK—1990

Reprint of 1987 Fairchild FAST Applications Handbook

Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders
Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design
FAST Characteristics and Testing • Packaging Characteristics

GENERAL PURPOSE LINEAR DEVICES DATABOOK—1989

Continuous Voltage Regulators • Switching Voltage Regulators • Operational Amplifiers • Buffers • Voltage Comparators
Instrumentation Amplifiers • Surface Mount

GRAPHICS HANDBOOK—1989

Advanced Graphics Chipset • DP8500 Development Tools • Application Notes

INTERFACE DATABOOK—1988

Transmission Line Drivers/Receivers • Bus Transceivers • Peripheral Power Drivers • Display Drivers
Memory Support • Microprocessor Support • Level Translators and Buffers • Frequency Synthesis • Hi-Rel Interface

LINEAR APPLICATIONS HANDBOOK—1986

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LS/S/TTL DATABOOK—1989

Contains former Fairchild Products

Introduction to Bipolar Logic • Low Power Schottky • Schottky • TTL • TTL—Low Power

MASS STORAGE HANDBOOK—1989

Rigid Disk Pulse Detectors • Rigid Disk Data Separators/Synchronizers and ENDECs
Rigid Disk Data Controller • SCSI Bus Interface Circuits • Floppy Disk Controllers • Disk Drive Interface Circuits
Rigid Disk Preamplifiers and Servo Control Circuits • Rigid Disk Microcontroller Circuits • Disk Interface Design Guide

MEMORY DATABOOK—1990

PROMs, EPROMs, EEPROMs • TTL I/O SRAMs • ECL I/O SRAMs

MICROCONTROLLER DATABOOK—1989

COP400 Family • COP800 Family • COPS Applications • HPC Family • HPC Applications
MICROWIRE and MICROWIRE/PLUS Peripherals • Microcontroller Development Tools

MICROPROCESSOR DATABOOK—1989

Series 32000 Overview • Central Processing Units • Slave Processors • Peripherals
Development Systems and Software Tools • Application Notes • NSC800 Family

PROGRAMMABLE LOGIC DATABOOK & DESIGN MANUAL—1990

Product Line Overview • Datasheets • Designing with PLDs • PLD Design Methodology • PLD Design Development Tools
Fabrication of Programmable Logic • Application Examples

REAL TIME CLOCK HANDBOOK—1989

Real Time Clocks and Timer Clock Peripherals • Application Notes

RELIABILITY HANDBOOK—1986

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510
The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices
Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization
Quality Assurance and Reliability Engineering • Reliability and Documentation • Commercial Grade Device
European Reliability Programs • Reliability and the Cost of Semiconductor Ownership
Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program
883B/RETSM Products • MILS/RETSM Products • 883/RETSM Hybrids • MIL-M-38510 Class B Products
Radiation Hardened Technology • Wafer Fabrication • Semiconductor Assembly and Packaging
Semiconductor Packages • Glossary of Terms • Key Government Agencies • AN/ Numbers and Acronyms
Bibliography • MIL-M-38510 and DESC Drawing Cross Listing

SPECIAL PURPOSE LINEAR DEVICES DATABOOK—1989

Audio Circuits • Radio Circuits • Video Circuits • Motion Control Circuits • Special Function Circuits
Surface Mount

TELECOMMUNICATIONS—1990

Line Card Components • Integrated Services Digital Network Components • Analog Telephone Components
Application Notes

NATIONAL SEMICONDUCTOR CORPORATION DISTRIBUTORS

ALABAMA

Huntsville
 Arrow Electronics
 (205) 837-6955
 Bell Industries
 (205) 837-1074
 Hamilton/Avnet
 (205) 837-7210
 Pioneer Technology
 (205) 837-9300
 Time Electronics
 (205) 721-1133

ARIZONA

Chandler
 Hamilton/Avnet
 (602) 231-5100
 Phoenix
 Arrow Electronics
 (602) 437-0750
 Tempe
 Anthem Electronics
 (602) 966-6600
 Bell Industries
 (602) 966-7800
 Time Electronics
 (602) 967-2000

CALIFORNIA

Agora Hills
 Bell Industries
 (818) 706-2608
 Zeus Components
 (818) 889-3838
 Anaheim
 Time Electronics
 (714) 934-0911
 Chatsworth
 Anthem Electronics
 (818) 700-1000
 Arrow Electronics
 (818) 701-7500
 Hamilton Electro Sales
 (818) 700-6500
 Time Electronics
 (818) 998-7200
 Costa Mesa
 Avnet Electronics
 (714) 754-6050
 Hamilton Electro Sales
 (714) 641-4159
 Cypress
 Bell Industries
 (714) 895-7801
 Gardena
 Bell Industries
 (213) 515-1800
 Hamilton/Avnet
 (213) 217-6751
 Irvine
 Anthem Electronics
 (714) 768-4444
 Ontario
 Hamilton/Avnet
 (714) 989-4602
 Rocklin
 Anthem Electronics
 (916) 624-9744
 Bell Industries
 (916) 652-0414
 Sacramento
 Hamilton/Avnet
 (916) 925-2216
 San Diego
 Anthem Electronics
 (619) 453-9005
 Arrow Electronics
 (619) 565-4800
 Hamilton/Avnet
 (619) 571-7510
 Time Electronics
 (619) 586-1331

San Jose
 Anthem Electronics
 (408) 453-1200
 Pioneer Technology
 (408) 954-9100
 Zeus Components
 (408) 629-4789
 Sunnyvale
 Arrow Electronics
 (408) 745-6600
 Bell Industries
 (408) 734-8570
 Hamilton/Avnet
 (408) 743-3355
 Time Electronics
 (408) 734-9888
 Thousand Oaks
 Bell Industries
 (805) 499-6821
 Torrance
 Time Electronics
 (213) 320-0880
 Tustin
 Arrow Electronics
 (714) 838-5422
 Yorba Linda
 Zeus Components
 (714) 921-9000

COLORADO

Englewood
 Anthem Electronics
 (303) 790-4500
 Arrow Electronics
 (303) 790-4444
 Hamilton/Avnet
 (303) 799-7800

CONNECTICUT

Cheshire
 Time Electronics
 (203) 271-3200
 Danbury
 Hamilton/Avnet
 (203) 797-2800
 Norwalk
 Pioneer Standard
 (203) 853-1515
 Wallingford
 Arrow Electronics
 (203) 265-7741
 Waterbury
 Anthem Electronics
 (203) 575-1575

FLORIDA

Allamonte Springs
 Bell Industries
 (407) 339-0078
 Pioneer Technology
 (407) 834-9090
 Clearwater
 Pioneer Technology
 (813) 536-0445
 Deerfield Beach
 Arrow Electronics
 (305) 429-8200
 Bell Industries
 (305) 421-1997
 Pioneer Technology
 (305) 428-8877
 Fort Lauderdale
 Hamilton/Avnet
 (305) 971-2900
 Time Electronics
 (305) 484-7778
 Lake Mary
 Arrow Electronics
 (407) 333-9300
 Largo
 Bell Industries
 (813) 541-4434

Orlando
 Time Electronics
 (407) 841-6565
 Oviedo
 Zeus Components
 (407) 365-3000
 St. Petersburg
 Hamilton/Avnet
 (813) 576-3930
 Winter Park
 Hamilton/Avnet
 (407) 628-3888

GEORGIA

Duluth
 Arrow Electronics
 (404) 497-1300
 Norcross
 Bell Industries
 (404) 662-0923
 Hamilton/Avnet
 (404) 447-7500
 Pioneer Technology
 (404) 448-1711
 Time Electronics
 (404) 448-4448

ILLINOIS

Addison
 Pioneer Electronics
 (708) 437-9680
 Bensenville
 Hamilton/Avnet
 (708) 860-7780
 Elk Grove Village
 Anthem Electronics
 (708) 640-6066
 Bell Industries
 (708) 640-1910
 Itasca
 Arrow Electronics
 (708) 250-0500
 Urbana
 Bell Industries
 (217) 328-1077
 Wood Dale
 Time Electronics
 (708) 350-0610
INDIANA
 Carmel
 Hamilton/Avnet
 (317) 844-9333
 Fort Wayne
 Bell Industries
 (219) 423-3422
 Indianapolis
 Advent Electronics Inc.
 (317) 872-4910
 Arrow Electronics
 (317) 243-9353
 Bell Industries
 (317) 634-8200
 Pioneer Standard
 (317) 573-0880

IOWA

Cedar Rapids
 Advent Electronics
 (319) 363-0221
 Arrow Electronics
 (319) 395-7230
 Bell Industries
 (319) 395-0730
 Hamilton/Avnet
 (319) 362-4757

KANSAS

Lenexa
 Arrow Electronics
 (913) 541-9542
 Hamilton/Avnet
 (913) 888-8900

MARYLAND

Columbia
 Anthem Electronics
 (301) 995-6640
 Arrow Electronics
 (301) 995-0003
 Hamilton/Avnet
 (301) 995-3500
 Time Electronics
 (301) 964-3090
 Zeus Components
 (301) 997-1118
 Gaithersburg
 Pioneer Technology
 (301) 921-0860

MASSACHUSETTS

Andover
 Bell Industries
 (508) 474-8880
 Lexington
 Pioneer Standard
 (617) 861-9200
 Zeus Components
 (617) 863-8800
 Norwood
 Gerber Electronics
 (617) 769-6000
 Peabody
 Hamilton/Avnet
 (508) 531-7430
 Time Electronics
 (508) 532-6200
 Wilmington
 Anthem Electronics
 (508) 657-5170
 Arrow Electronics
 (508) 658-0900

MICHIGAN

Ann Arbor
 Bell Industries
 (313) 971-9093
 Grand Rapids
 Arrow Electronics
 (616) 243-0912
 Hamilton/Avnet
 (616) 243-8805
 Pioneer Standard
 (616) 698-1800
 Livonia
 Arrow Electronics
 (313) 665-4100
 Pioneer Standard
 (313) 525-1800
 Novi
 Hamilton/Avnet
 (313) 347-4720
 Southfield
 R. M. Electronics, Inc.
 (313) 262-1582
 Wyoming
 R. M. Electronics, Inc.
 (616) 531-9300

MINNESOTA

Eden Prairie
 Anthem Electronics
 (612) 944-5454
 Pioneer Standard
 (612) 944-3355
 Edina
 Arrow Electronics
 (612) 830-1800
 Time Electronics
 (612) 835-1250
 Minnetonka
 Hamilton/Avnet
 (612) 932-0600

NATIONAL SEMICONDUCTOR CORPORATION DISTRIBUTORS (Continued)

MISSOURI

Chesterfield
Hamilton/Avnet
(314) 537-1600
St. Louis
Arrow Electronics
(314) 567-6888
Pioneer Standard
(314) 432-4350
Time Electronics
(314) 391-6444

NEW HAMPSHIRE

Hudson
Bell Industries
(603) 882-1133
Manchester
Arrow Electronics
(603) 668-6968
Hamilton/Avnet
(603) 624-9400

NEW JERSEY

Cherry Hill
Hamilton/Avnet
(609) 424-0100
Fairfield
Anthem Electronics
(201) 227-7960
Hamilton/Avnet
(201) 575-3390
Marlton
Arrow Electronics
(609) 596-8000
Parsippany
Arrow Electronics
(201) 538-0900
Pine Brook
Nu Horizons Electronics
(201) 882-8300
Pioneer Standard
(201) 575-3510
Time Electronics
(201) 882-4611

NEW MEXICO

Albuquerque
Alliance Electronics Inc.
(505) 292-3360
Arrow Electronics
(505) 243-4566
Bell Industries
(505) 292-2700
Hamilton/Avnet
(505) 345-0001

NEW YORK

Amityville
Nu Horizons Electronics
(516) 226-6000
Binghamton
Pioneer
(607) 722-9300
Buffalo
Summit Electronics
(716) 887-2600
Commack
Anthem Electronics
(516) 864-6600
Fairport
Pioneer Standard
(716) 381-7070
Time Electronics
(716) 383-8853
Hauppauge
Arrow Electronics
(516) 231-1000
Hamilton/Avnet
(516) 434-7413
Time Electronics
(516) 273-0100
Port Chester
Zeus Components
(914) 937-7400

Rochester

Arrow Electronics
(716) 427-0300
Hamilton/Avnet
(716) 475-9130
Summit Electronics
(716) 334-8110
Ronkonkoma
Zeus Components
(516) 737-4500
Syracuse
Hamilton/Avnet
(315) 437-2641
Time Electronics
(315) 432-0355
Westbury
Hamilton/Avnet Export Div.
(516) 997-8668
Woodbury
Pioneer Electronics
(516) 921-8700

NORTH CAROLINA

Charlotte
Pioneer Technology
(704) 527-8188
Time Electronics
(704) 522-7600
Durham
Pioneer Technology
(919) 544-5400
Raleigh
Arrow Electronics
(919) 876-3132
Hamilton/Avnet
(919) 878-0810
Winston-Salem
Arrow Electronics
(919) 725-8711

OHIO

Centerville
Arrow Electronics
(513) 435-5563
Bell Industries
(513) 435-8660
Bell Industries-Military
(513) 434-8231
Cleveland
Pioneer
(216) 587-3600
Dayton
Hamilton/Avnet
(513) 439-6700
Pioneer Standard
(513) 236-9900
Zeus Components
(914) 937-7400
Dublin
Time Electronics
(614) 761-1100
Solon
Arrow Electronics
(216) 248-3990
Hamilton/Avnet
(216) 831-3500
Westerville
Hamilton/Avnet
(614) 882-7004

OKLAHOMA

Tulsa
Arrow Electronics
(918) 252-7537
Hamilton/Avnet
(918) 252-7297
Pioneer Standard
(918) 492-0546
Radio Inc.
(918) 587-9123

OREGON

Beaverton
Almac-Stroum Electronics
(503) 629-8090
Anthem Electronics
(503) 643-1114
Arrow Electronics
(503) 645-6456
Hamilton/Avnet
(503) 627-0201
Lake Oswego
Bell Industries
(503) 635-6500
Portland
Time Electronics
(503) 684-3780

PENNSYLVANIA

Horsham
Anthem Electronics
(215) 443-5150
Pioneer Technology
(215) 674-4000
King of Prussia
Time Electronics
(215) 337-0900
Monroeville
Arrow Electronics
(412) 856-7000
Pittsburgh
Hamilton/Avnet
(412) 281-4150
Pioneer
(412) 782-2300

TEXAS

Austin
Arrow Electronics
(512) 835-4180
Hamilton/Avnet
(512) 837-8911
Pioneer Standard
(512) 835-4000
Time Electronics
(512) 399-3051
Carrollton
Arrow Electronics
(214) 380-6464
Time Electronics
(214) 241-7441
Dallas
Hamilton/Avnet
(214) 404-9906
Pioneer Standard
(214) 386-7300
Houston
Arrow Electronics
(713) 530-4700
Pioneer Standard
(713) 988-5555
Richardson
Anthem Electronics
(214) 238-7100
Zeus Components
(214) 783-7010
Stafford
Hamilton/Avnet
(713) 240-7733
UTAH
Midvale
Bell Industries
(801) 255-9611
Salt Lake City
Anthem Electronics
(801) 973-8555
Arrow Electronics
(801) 973-6913
Hamilton/Avnet
(801) 972-4300
West Valley
Time Electronics
(801) 973-8181

WASHINGTON

Belleuve
Almac-Stroum Electronics
(206) 643-9992
Bothell
Anthem Electronics
(206) 483-1700
Kent
Arrow Electronics
(206) 575-4420
Redmond
Bell Industries
(206) 885-9963
Hamilton/Avnet
(206) 881-6697
Time Electronics
(206) 882-1600

WISCONSIN

Brookfield
Arrow Electronics
(414) 792-0150
Mequon
Taylor Electric
(414) 241-4321
Waukesha
Bell Industries
(414) 547-8879
Hamilton/Avnet
(414) 784-4516

CANADA

WESTERN PROVINCES

Burnaby
Hamilton/Avnet
(604) 437-6667
Semad Electronics
(604) 420-9889
Calgary
Hamilton/Avnet
(403) 250-9380
Semad Electronics
(403) 252-5664
Zentronics
(403) 272-1021
Edmonton
Zentronics
(403) 468-9306
Richmond
Zentronics
(604) 273-5575
Saskatoon
Zentronics
(306) 955-2207
Winnipeg
Zentronics
(204) 694-1957

EASTERN PROVINCES

Mississauga
Hamilton/Avnet
(416) 677-7432
Time Electronics
(416) 672-5300
Zentronics
(416) 564-9600
Nepean
Hamilton/Avnet
(613) 226-1700
Zentronics
(613) 226-8840
Ottawa
Semad Electronics
(613) 727-8325
Pointe Claire
Semad Electronics
(514) 694-0860
St. Laurent
Hamilton/Avnet
(514) 335-1000
Zentronics
(514) 737-9700
Willowdale
ElectroSonic Inc.
(416) 494-1666

SALES OFFICES

ALABAMA

Huntsville
(205) 721-9367

ARIZONA

Tempe
(602) 966-4563

CALIFORNIA

Inglewood
(213) 645-4226

Roseville
(916) 786-5577

San Diego
(619) 587-0666

Santa Clara
(408) 562-5900

Tustin
(714) 259-8880

Woodland Hills
(818) 888-2602

COLORADO

Boulder
(303) 440-3400

Colorado Springs
(719) 578-3319

Englewood
(303) 790-8090

CONNECTICUT

Hamden
(203) 288-1560

FLORIDA

Boca Raton
(407) 997-8133

Orlando
(407) 629-1720

St. Petersburg
(813) 577-5017

GEORGIA

Norcross
(404) 441-2740

ILLINOIS

Schaumburg
(708) 397-8777

INDIANA

Carmel
(317) 843-7160

Fort Wayne
(219) 484-0722

IOWA

Cedar Rapids
(319) 395-0090

KANSAS

Overland Park
(913) 451-4402

MARYLAND

Hanover
(301) 796-8900

MASSACHUSETTS

Burlington
(617) 221-4500

MICHIGAN

Grand Rapids
(616) 940-0588

W. Bloomfield
(313) 855-0166

MINNESOTA

Bloomington
(612) 854-8200

MISSOURI

St. Louis
(314) 569-9830

NEW JERSEY

Paramus
(201) 599-0955

NEW MEXICO

Albuquerque
(505) 884-5601

NEW YORK

Fairport
(716) 223-7700

Melville
(516) 351-1000

Wappinger Falls
(914) 298-0680

NORTH CAROLINA

Raleigh
(919) 832-0661

OHIO

Dayton
(513) 435-6886

Independence
(216) 524-5577

ONTARIO

Mississauga
(416) 678-2920

Nepean
(613) 596-0411

OREGON

Portland
(503) 639-5442

PENNSYLVANIA

Horsham
(215) 672-6767

PUERTO RICO

Rio Piedras
(809) 758-9211

QUEBEC

Pointe Claire
(514) 426-2992

TEXAS

Austin
(512) 346-3990

Houston
(713) 771-3547

Richardson
(214) 234-3811

UTAH

Salt Lake City
(801) 322-4747

WASHINGTON

Bellevue
(206) 453-9944

WISCONSIN

Brookfield
(414) 782-1818

National Semiconductor Corporation

2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 721-5000
TWX: (910) 339-9240

SALES OFFICES (Continued)**INTERNATIONAL
OFFICES****Electronica NSC de Mexico SA**

Juventino Rosas No. 118-2
Col Guadalupe Inn
Mexico, 01020 D.F. Mexico
Tel: 52-5-524-9402

**National Semicondutores
Do Brasil Ltda.**

Av. Brig. Faria Lima, 1383
6.0 Andor-Conj. 62
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
Fax: (55/11) 211-1181 NSBR BR

National Semiconductor GmbH

Industriestrasse 10
D-8080 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor (UK) Ltd.

The Maple, Kembrey Park
Swindon, Wiltshire SN2 6UT
United Kingdom
Tel: (07-93) 61-41-41
Telex: 444-674
Fax: (07-93) 69-75-22

National Semiconductor Benelux

Vorstlaan 100
B-1170 Brussels
Belgium
Tel: (02) 6-61-06-80
Telex: 61007
Fax: (02) 6-60-23-95

National Semiconductor (UK) Ltd.

Ringager 4A, 3
DK-2605 Brøndby
Denmark
Tel: (02) 43-32-11
Telex: 15-179
Fax: (02) 43-31-11

National Semiconductor S.A.

Centre d'Affaires-La Boursiere
Bâtiment Champagne, B.P. 90
Route Nationale 186
F-92357 Le Plessis Robinson
France
Tel: (1) 40-94-88-88
Telex: 631065
Fax: (1) 40-94-88-11

National Semiconductor (UK) Ltd.

Unit 2A
Clonskeagh Square
Clonskeagh Road
Dublin 14
Tel: (01) 69-55-89
Telex: 91047
Fax: (01) 69-55-89

National Semiconductor S.p.A.

Strada 7, Palazzo R/3
I-20089 Rozzano
Milanofiori
Italy
Tel: (02) 8242046/7/8/9
Twx: 352647
Fax: (02) 8254758

National Semiconductor S.p.A.

Via del Cararaggio, 107
00147 Rome
Italy
Tel: (06) 5-13-48-80
Fax: (06) 5-13-79-47

National Semiconductor (UK) Ltd.

Stasjonsvn 18
Postboks 15
N-1361 Billingstadsletta
Norway
Tel: 47-2-849362
Fax: 47-2-848104

National Semiconductor AB

P.O. Box 1009
Grosshandlarvaegen 7
S-121 23 Johanneshov
Sweden
Tel: 46-8-7228050
Fax: 46-8-7229095
Telex: 10731 NSC S

National Semiconductor GmbH

Calle Agustin de Foxa, 27 (9°D)
28036 Madrid
Spain
Tel: (01) 733-2958
Telex: 46133
Fax: (01) 733-8018

**National Semiconductor
Switzerland**

Alte Winterthurerstrasse 53
Postfach 567
CH-8304 Wallisellen-Zurich
Switzerland
Tel: (01) 830-2727
Telex: 828-444
Fax: (01) 830-1900

National Semiconductor

Kauppakartanonkatu 7 A22
SF-00930 Helsinki
Finland
Tel: (90) 33-80-33
Telex: 126116
Fax: (90) 33-81-30

National Semiconductor

Postbus 90
1380 AB Weesp
The Netherlands
Tel: (0-29-40) 3-04-48
Telex: 10-956
Fax: (0-29-40) 3-04-30

**National Semiconductor Japan
Ltd.**

Sanseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-ku
Tokyo 160 Japan
Tel: 3-299-7001
Fax: 3-299-7000

National Semiconductor

Hong Kong Ltd.
Suite 513, 5th Floor,
Chinachem Golden Plaza,
77 Mody Road, Tsimshatsui East,
Kowloon, Hong Kong
Tel: 3-7231290
Telex: 52996 NSSEA HX
Fax: 3-3112536

National Semiconductor

(Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004
Victoria, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458

**National Semiconductor (PTE),
Ltd.**

200 Cantonment Road 13-01
Southpoint
Singapore 0208
Tel: 2252226
Telex: RS 33877

**National Semiconductor (Far East)
Ltd.**

Taiwan Branch
P.O. Box 68-332 Taipei
7th Floor, Nan Shan Life Bldg.
302 Min Chuan East Road,
Taipei, Taiwan R.O.C.
Tel: (86) 02-501-7227
Telex: 22837 NSTW
Cable: NSTW TAIPEI

**National Semiconductor (Far East)
Ltd.**

Korea Branch
13th Floor, Dai Han Life Insurance
63 Building,
60, Yoido-dong, Youngdeungpo-ku,
Seoul, Korea 150-763
Tel: (02) 784-8051/3, 785-0696/8
Telex: 24942 NSPKLO
Fax: (02) 784-8054