



Using an LCD with the NS486SXF Evaluation Board
NS486SXF Application Note

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Introduction

The NS486SXF Embedded Microprocessor includes an on-chip LCD controller capable of driving a variety of supertwist LCD panels. Although no direct LCD connector was included on the NS486SXF Evaluation Board (EVB), the LCD signals were routed to the 40-pin feature connector. This provides a fairly simple way to interface an LCD to the evaluation board, which could be useful to designers who wish to evaluate the LCD controller, prototype their system design on the Evaluation Board, or develop and debug software for a display system using an LCD.

This application note describes a hardware and software reference design that interfaces a 320x240 LCD panel with four levels of gray scale to the NS486SXF EVB. This document also discusses interfacing and software issues that are applicable to any LCD system using the NS486SXF LCD controller.

Overview

The LCD panels supported by the NS486SXF include self-contained screen drivers and provide a fairly simple interface to the NS486SXF. The SXF LCD controller directly drives four LCD data lines and three LCD clocks. The remaining signals used by most LCD controllers include LCD driver and contrast voltages, power, and ground. Some LCD panels require an additional clock signal that is easily generated from the NS486SXF LCD clocks, which is documented in the NS486SXF Datasheet and this application note. Finally, some LCD controllers provide a display enable signal, while others require switching of the LCD driver voltage.

Unfortunately, most LCD panels require careful sequencing of signals. In the case of LCD panels that provide an enable signal, generally only the LCD clocks and the enable must be sequenced. For LCD panels without a display enable, one or more of the voltage inputs must be sequenced with the LCD clocks. In both cases, damage to the LCD panel can result if the proper power-up and power-down sequencing is not followed.

This application note describes an interface to an Optrex DMF50081NB-FW panel, which is a 320x240 LCD panel with a built in backlight. This panel provides a display enable signal, which slightly reduces the complexity of the power sequencing.

In addition to the hardware required, this application note describes the software used to demonstrate the proper programming of the NS486SXF LCD controller for this design.

Optrex Signals

The Optrex DMF50081NB-FW LCD panel used requires the following signals:

| | | |
|----------------------|---------------------------------------|--|
| FLM | Frame Signal | Identical to the NS486SXF CLF signal. |
| LP | Data Latch Signal | Identical to the NS486SXF CL1 signal. |
| CP | Clock Signal for Shifting Serial Data | Identical to the NS486SXF CL2 signal. |
| M | Alternate Signal for LCD Drive | Called “WF” in NS486SXF Datasheet. This signal alternates every frame. |
| V _{ADJ} | Power Supply for LCD Control | Adjusts the contrast of the LCD display. |
| V _{CC} | Power Supply for Logic (+5V) | +5V. |
| V _{SS} | Power Supply (0V,GND) | Ground. |
| V _{EE} | Power Supply for LCD Driving | Voltage for LCD drivers. |
| D0 | Display Data 0 | Data Bit. Identical to NS486SXF LCD0 signal. |
| D1 | Display Data 1 | Data Bit. Identical to NS486SXF LCD1 signal. |
| D2 | Display Data 2 | Data Bit. Identical to NS486SXF LCD2 signal. |
| D3 | Display Data 3 | Data Bit. Identical to NS486SXF LCD3 signal. |
| D _{ISP OFF} | Display Enable (enabled when high) | Enables the LCD panel when at logic high. |

Nine of the signals interface directly to the NS486SXF. The remaining four signals are created on the LCD interface hardware.

The “Dispoff” signal, contrary to its name, enables the LCD when at logic high. This pin can be considered active-low to make its name and function consistent.

Schematic Overview

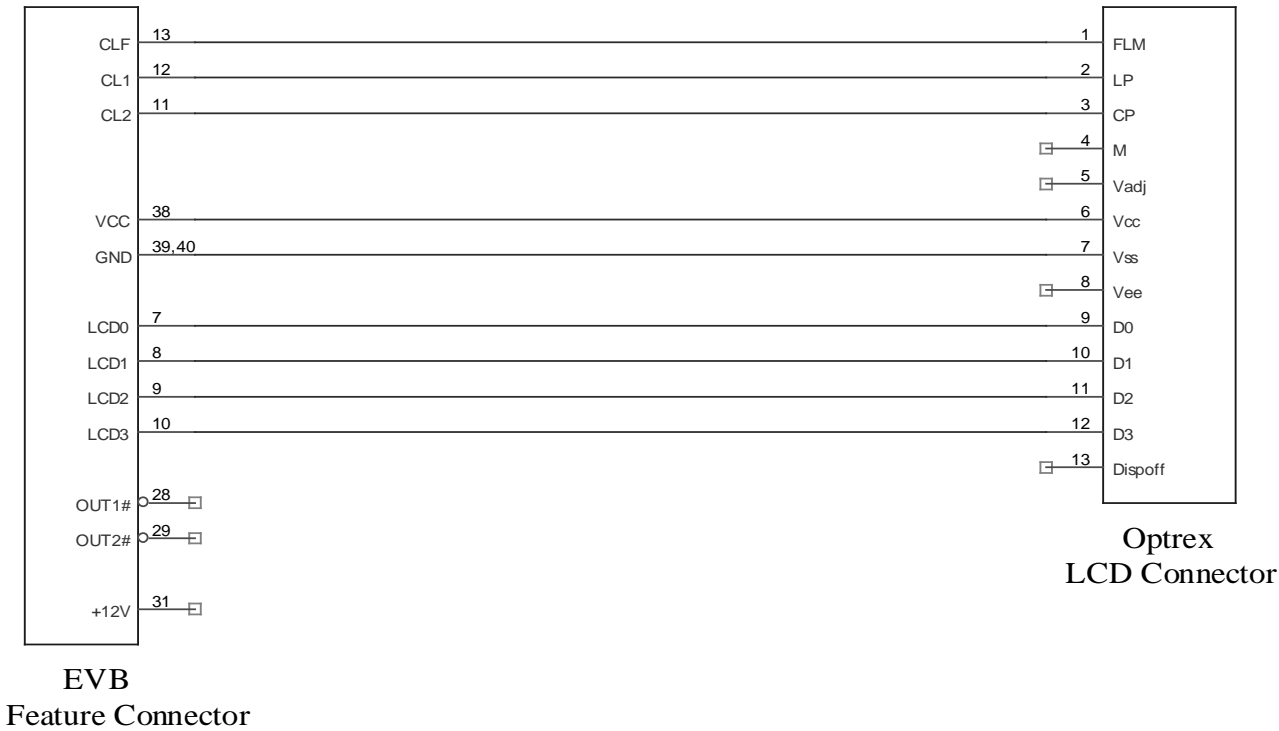
Appendix C contains the schematics for the LCD hardware required to interface the Optrex LCD panel to the NS486SXF Evaluation Board. For clarity, the schematics have been broken down into five portions, each of which shows a specific functional connection. The schematics are also embedded in the following sections that explain each block.

Schematic: LCD - Direct Connections

The following diagram shows the 9 signals on the Optrex LCD connector that can be connected directly to the NS486SXF Feature Connector.

The four LCD data and three LCD clock signals connect directly to the LCD.

The Optrex LCD used does not require sequencing of the +5V Vcc signal, so this signal is connected directly to the SXF Feature Connector, as is the digital ground (GND). Some LCD panels do require the +5V signal to be sequenced with the LCD clocks and other signals. For these panels, additional logic, similar to that shown in the ‘LCD - “Dispoﬀ” Signal Generation’ section should be included.



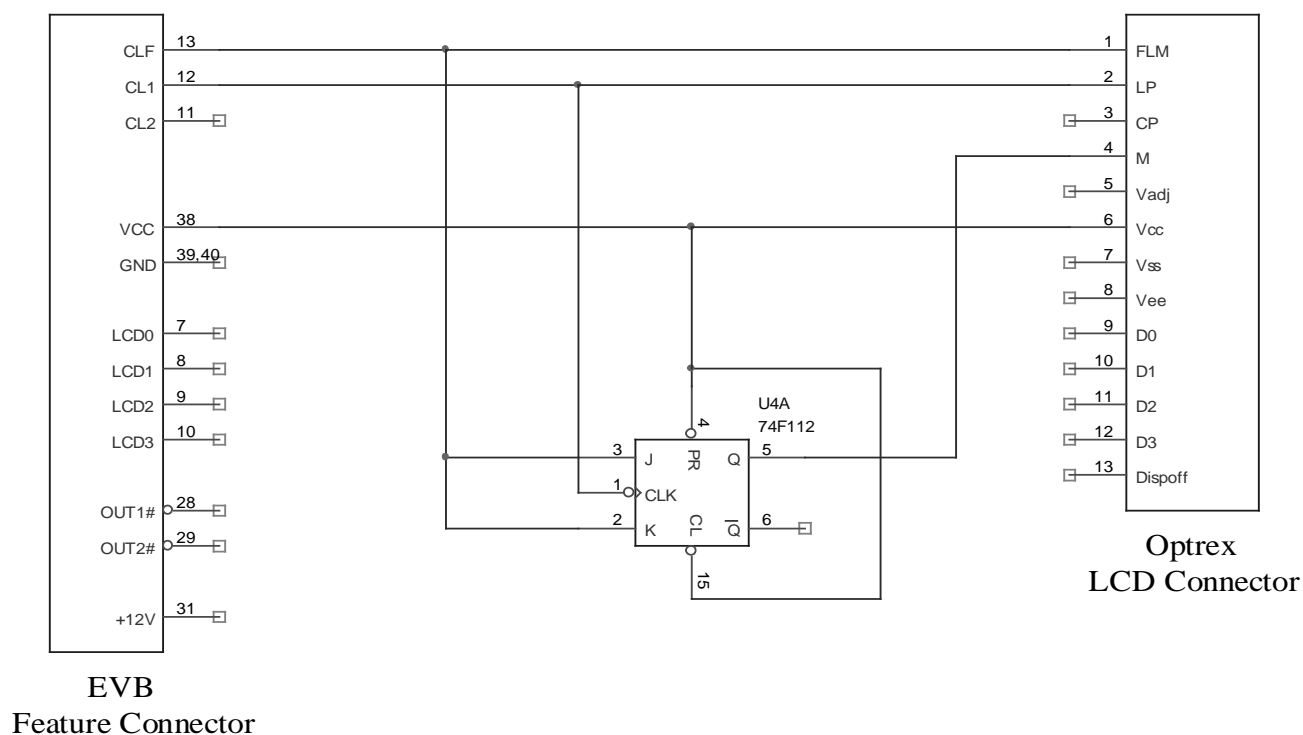
LCD - Direct Connections

Schematic: LCD - “M” Signal Generation

The Optrex LCD panel requires an M signal, which is a clock signal that alternates every frame. This signal is called the WF signal in the NS486SXF Datasheet. The circuitry shown here is taken from the NS486SXF Datasheet. Many LCD panels do not require this signal.

A J-K flip-flop is used to generate the M signal. The CL1 signal is used to clock the flip-flop, which will trigger the flip-flop once per row of LCD data. However, the CLF signal, which is connected to the J and K inputs of the flip-flop will be low except during the first row of the frame. Therefore, once per frame the J and K inputs will be high, causing the flip-flop output to toggle. The rest of the time, the flip-flop will maintain the current output.

Note: the power and ground signals for the 74F112 flip-flop are not shown, but should be connected to VCC and GND respectively. Also, the NS486SXF Datasheet shows the PR# input connected to the RESET# signal so that the flip-flop starts in a known state at reset. However, the RESET# signal was not connected to the feature connector until a recent EVB revision, so this signal was simply tied high. Since the flip-flop is used in toggle-mode, the initial output state is not important.



LCD - "M" Signal Generation

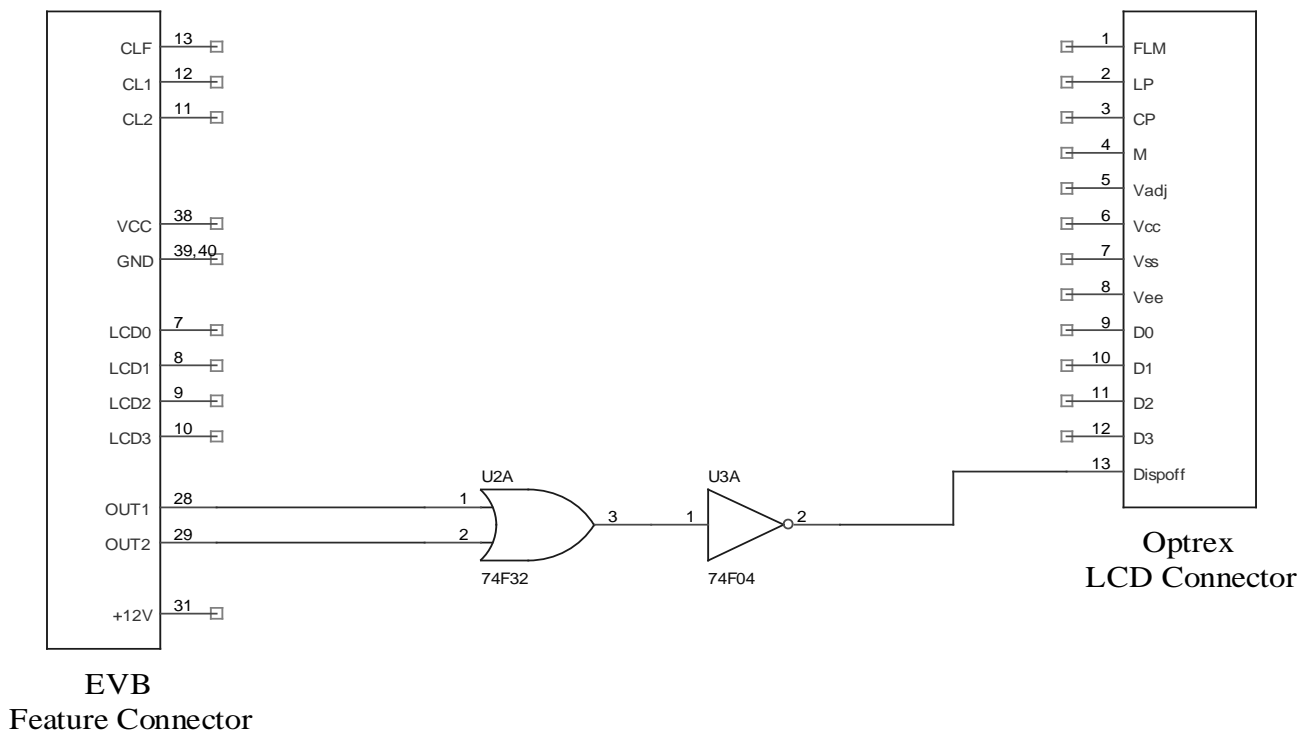
Schematic: LCD - “Dispoff” Signal Generation

The Optrex LCD provides a display enable signal. On the Optrex LCD, this is the only signal that must be sequenced with the LCD clocks. This signal should be held low (LCD disabled) until the LCD clock signals (CLF, CL1, and CL2) are running. Shortly after the LCD clocks are running, the enable signal should be changed to a high level (LCD enabled). Additional information on power sequencing is contained later in this application note.

To control the display enable signal, a simple NOR gate is connected to the OUT1# and OUT# signals on the feature connector. These two signals, which are not on the earliest revision of the evaluation board (but can be added easily), are general-purpose output bits found on the external UART on the Evaluation Board. These signals are easy to control through software, so they provide a good way to enable the LCD.

The two signals are NOR’ed so that both must be low before the LCD will be enabled. These pins are high on reset. Technically, only one of these signals is required to enable the Optrex LCD. However, the use of the two pins reduces the possibility of UART code accidentally turning on the LCD when the LCD clocks are not running. The register bit in the UART that controls the OUT2 signal is often set (causing this pin to go low) by UART code. This is because on certain Super I/O type UARTs, this bit is used to enable UART interrupts. However, the OUT2 bit is rarely used. This is a weak protection mechanism. See the section on power sequencing for additional information on LCD panel protection.

Note: in the following schematic an OR and NOT gate is used to implement a NOR. These two gates can be substituted with a 74F02 (NOR) if desired. The power and ground signals for the logic are not shown, but should be connected to VCC and GND respectively.



LCD - "Dispoff" Signal Generation

Schematic: LCD - Voltage Generation

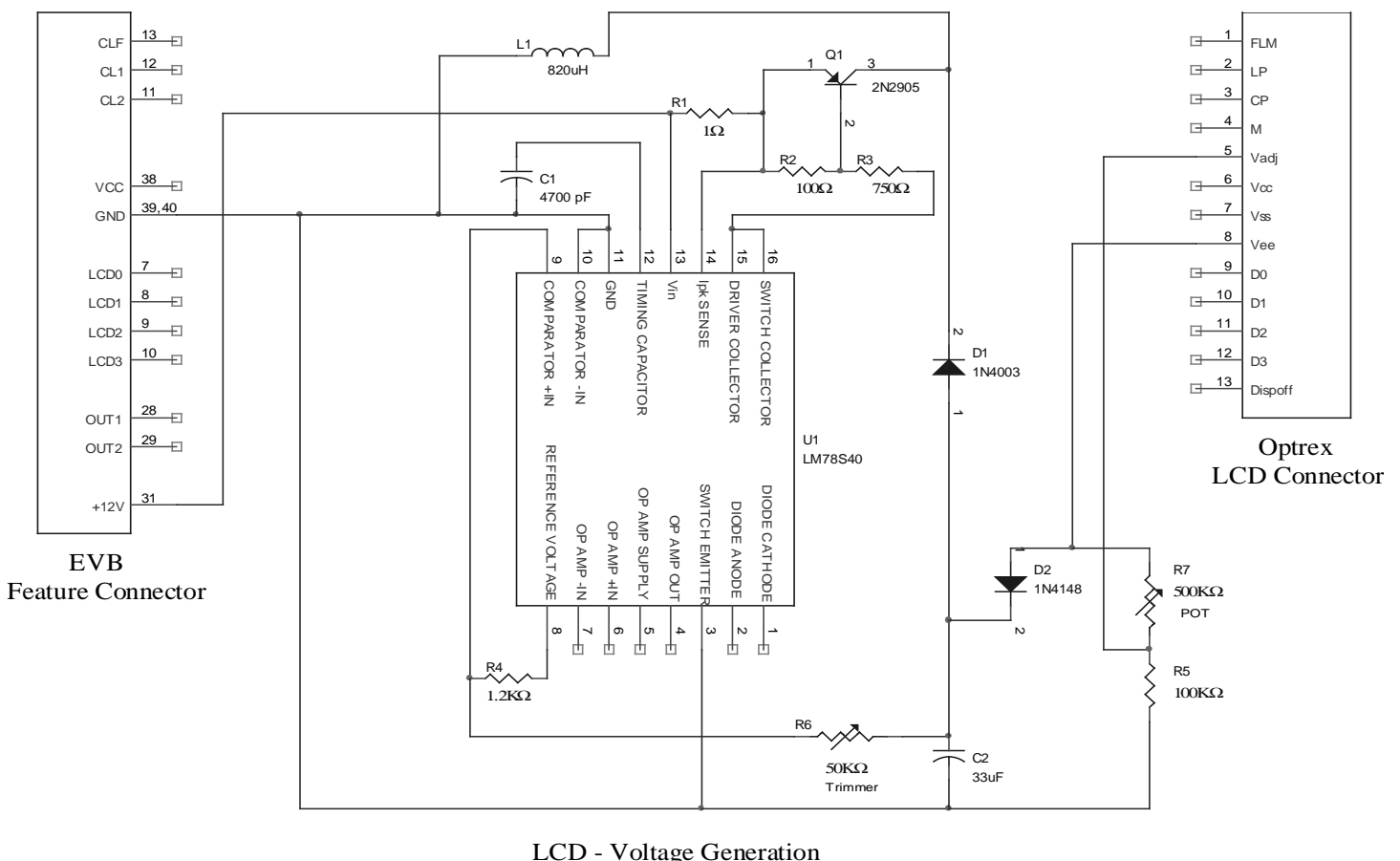
The Optrex LCD requires four voltage levels. Two are the standard voltage and ground, and can be connected directly to the NS486SXF Feature Connector. The other two voltages must be generated by the interface circuitry.

The Optrex LCD panel requires a Vee voltage of -22V to -25V and a Vadj voltage of -5V to -25V. The Vee voltage is used for the internal LCD drivers and is held constant. The Vadj voltage provides for contrast adjustment, and can be varied within the allowable range during operation to obtain proper contrast.

The following circuit was used to produce these two voltage levels. This circuitry was adapted from an application note for the National Semiconductor LM78S40. With the component values we chose, this circuit produces voltages from about -10V to -50V. The position of the 50K Ω trimmer (R6) is used to adjust the output voltage, which is connected to Vee on the LCD panel. To produce the Vadj voltage, a simple voltage divisor using a 500K Ω POT and 100K Ω resistor is used. This will allow Vadj to be varied between from -5V to Vee.

Additional information on calibrating and testing this circuit, as well as important notes on power sequencing, can be found later in this application note.

The National Semiconductor LM78S40 Datasheet and Application Note (AN-711) can both be found on the World Wide Web. Search for "LM78S40" at <http://www.national.com/design/>. When this application note was written, the information could be found directly at <http://www.national.com/pf/LM/LM78S40.html>, although this address is subject to change.

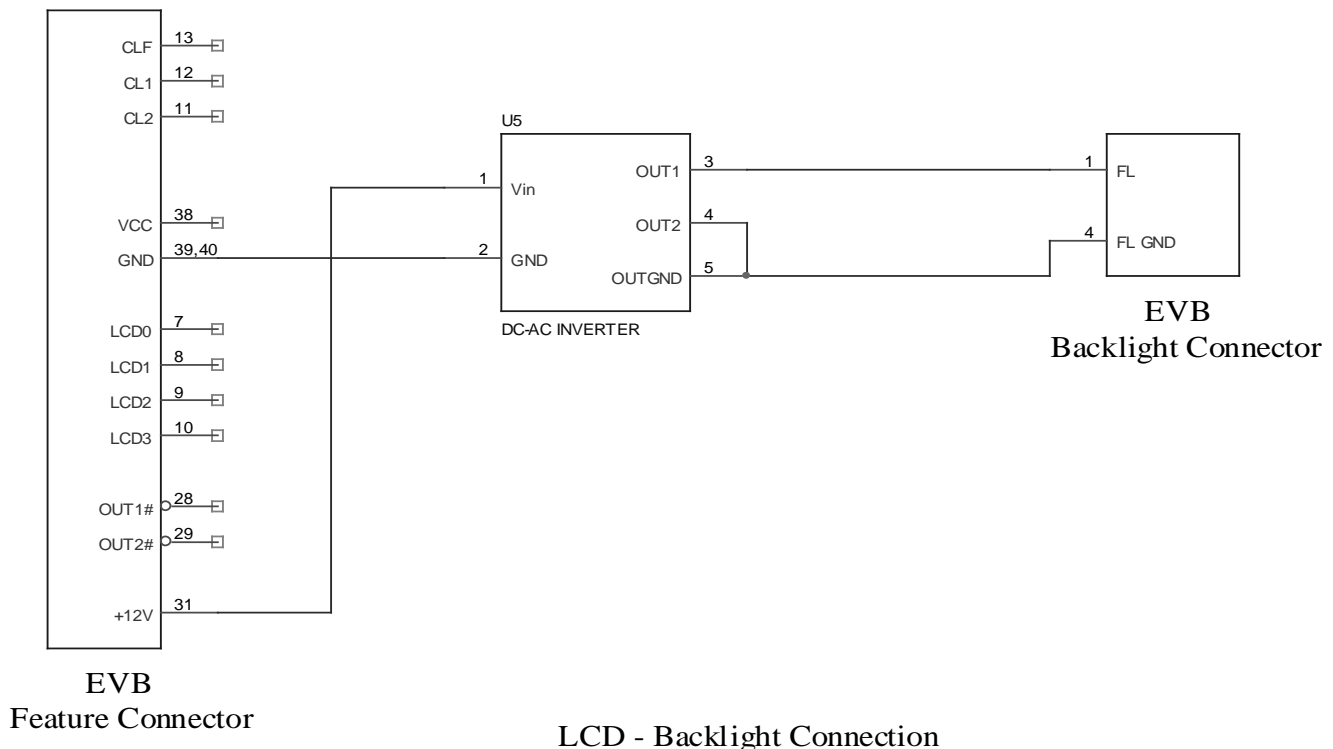


Schematic: LCD - Backlight Connection

The built-in backlight for the Optrex LCD uses a four-pin connector that is separate from the 14-pin connector used by the LCD panel.

A TDK CXA-L10L DC-AC inverter is used to generate the proper AC voltage for the backlight. The following schematic shows the proper connections for this part.

The AC output to the backlight is approximately 170V AC.



Layout and Connection Suggestions

This section discusses how we (the NS486SXF group) built the circuitry shown in the schematics and the physical connections and housings used.

All circuitry was hand soldered on a 3" by 4.5" of prototyping board. However, several headers and ribbon cables were used so that the LCD panel itself could be plugged and unplugged from the prototype board, and the board could be plugged and unplugged from the EVB Feature Connector. This allowed us to interchange components and test the circuitry.

The prototyping board itself has three headers on it. One is a 14-pin header that contains all of the signals that come from the EVB Feature Connector. A second 14-pin header contains the signals that connect to the 14-pin LCD connector on the Optrex LCD panel. Finally a four-pin header contains the signals that connect to the four-pin backlight plug on the Optrex LCD.

The Optrex LCD backlight connector is a four-pin plug on the end of two wires that run to the backlight. This plug connects directly to the four-pin header on the prototype board.

The Optrex 14-pin LCD connector is simply 14 connector holes on the LCD panel. To this connector, a 14-pin ribbon cable was separated and soldered. The other end of this ribbon cable was connected to a 14-pin connector that plugs directly onto the 14-pin header on the circuit board. To make the soldering to the LCD easier, the same pin order as on the Optrex LCD was kept on the 14-pin header.

The other 14-pin header on the circuit board contains all the signals that come from the NS486SXF EVB Feature Connector. These pins are in the approximate order as the signals used from the Feature Connector.

A plastic casing (basically a box with no top) a little wider and taller than the LCD panel was used to hold the circuit board, mountings for the LCD, socket connector to go to the Evaluation Board, and adjustment for the 500K Ω POT. The circuit board was simply screwed to the inside of this casing. The 500K Ω POT was bolted to the side of the casing so that the adjustment knob is on the side of the casing. A 14-pin IDC type plug was mounted on another side of the casing. The inside of this plug is connected through a ribbon cable to a 14-pin connector that plugs into the 14-pin header on the prototype board with the Feature Connector signals. This allows us to connect or disconnect the circuit board from the plug on the casing to exchange circuit boards if needed. The final connection is a 14-pin connector that connects the LCD hardware IDC plug to the 40-pin Feature Connector on the Evaluation Board. We used a 14-pin ribbon cable with a 14-pin connector that fits the IDC plug on one side, and a 40-pin right-angle connector that plugs directly into the NS486SXF Evaluation Board Feature Connector. The 14-pin ribbon cable was separated and soldered to the correct pins on the 40-pin right angle connector.

Finally, four 1.75" tall spacers were bolted to the casing so that the LCD panel could be attached above the LCD circuitry in the casing. The LCD itself essentially becomes the lid to the plastic casing.

This layout produced a simple, modular LCD system that can easily be assembled or disassembled, is fairly rugged, and can easily be connected to the NS486SXF Evaluation Board.

LCD Protection and Signal Sequencing

DC voltages can damage the liquid crystal in LCD panels. Therefore, LCD panels typically require certain power sequencing steps to protect the LCD from damage. The specific sequencing requirements vary between different models of LCD panels.

The Optrex panel used in this application note has a fairly simple power sequencing. All power voltages (V_{cc} , V_{ss} , V_{ee} , and V_{adj}) should be present before the display is enabled. The V_{adj} signal can be varied in the allowable range at any time. Before enabling the display, the LCD clock signals should be started. This is done by setting up the NS486SXF LCD controller in software. Once the three LCD clock signals are started, the display can be enabled.

When powering down the Optrex LCD, the LCD enable signal (Dispoff) should be set low to disable the LCD. After this, the LCD clocks can be stopped by programming the NS486SXF.

In the design shown in this application note, all voltages to the LCD are active whenever the Evaluation Board Is turned on. As shown earlier, the external UART OUT signals are used to enable the LCD panel after the LCD clocks are enabled, and disable the LCD panel before removing the LCD clock signals.

The Optrex DMF50081 Datasheet does not specify time constraints for enabling the display after starting the clock signals or disabling the display after stopping the clock signals. Therefore, a generic 1ms delay is used in the LCD code for this application note. The sequencing is as follows:

1. The voltage levels (V_{cc} , V_{ss} , V_{ee} , and V_{adj}) are generated whenever the SXF EVB is powered on.
2. The LCD software enables the LCD clocks (FLM, LP, CP, and M).
3. 1ms delay.
4. The LCD software enables the display by setting Dispoff high.
5. The LCD panel is left on for five seconds, so that the user can see the image on the LCD screen.
6. The LCD software disables the display by setting Dispoff low.
7. 1ms delay.
8. The LCD software disables the LCD clocks.
9. The voltage levels are removed when the Evaluation Board is powered off.

Enabling the LCD without the LCD clocks present should be avoided. The design in this datasheet does not have any hardware protection to prevent a situation in which the display is enabled but the clocks are not running. It is recommended that additional hardware protection circuitry be used in products using an LCD display. This circuitry would disable the LCD panel if the LCD clocks were inadvertently stopped. Please contact the specific LCD manufacturer for information on specific protection requirements and application notes on implementing this hardware protection.

As a final note, the Optrex display datasheet does not indicate any specific timing requirements for the sequencing (as noted above). Therefore, it is safe to remove power from the evaluation board or reset the board when the LCD is enabled. It is recommended that the LCD always be powered down in the proper order: disable LCD, remove clocks, then remove voltage levels. However, if for some reason the LCD power down code can not be executed, it is safe to simply reset the board or remove power from the EVB.

LCD Protection and Signal Sequencing - Other LCD Panels

Many LCD panels provide a display enable signal and will have similar power sequencing requirements to the Optrex panel. However, several other LCD panels have more rigid power sequencing requirements. This section briefly discusses the requirements for the Sharp LM32P10 LCD panel, which has more rigid power sequencing requirements.

The Sharp LM32P10 does not have a display enable signal. Instead, the digital voltage (VDD), clock signals, and driver voltage (VEE) must be properly sequenced. The required power-up sequence is as follows:

1. Establish VDD (+5V) voltage level
2. Start LCD clock signals and data signals
3. Establish VEE voltage level

The allowable range between step 1 and 2 is 0-20ms. The allowable range between step 2 and 3 is 0-100ms. This means that two voltage levels, VDD and VEE, must be switched during the power-on stage. The power-down sequence is the opposite of the power-up sequence.

Since power inputs must be switched, the LM32P10 panel would require additional circuitry (over the Optrex design in this application note) to implement the power sequencing. The VEE signal can not simply be gated through logic as the Dispoﬀ signal on the Optrex display is. Instead, a relay or other type of switching mechanism must be used. Application notes are available from Sharp that detail proper power sequencing and protection.

The Sharp LM32P10, as well as several Alps LCD panels, have been interfaced to the NS486SXF. The power sequencing logic is the only major difference required for the different panels. The Alps panel used provided a display enable signal, but also required sequencing of VEE.

NSDEMO Software

The NSDEMO program, provided in source code with the NS486SXF Evaluation Board, includes sample LCD code that works with the LCD hardware described in this application note. The latest version of the NSDEMO code can be obtained from the World Wide Web at <http://www.national.com/ns486/ns486sxf.html>.

Overview

The file “LCDTEST.C” implements a simple LCD application. This function “LCD_Test()” is called from the “main()” routine in “MAIN.C”. The “LCD_Test()” function performs the following steps:

1. Sets up the DMA controller for use with the LCD controller
2. Initialize the LCD controller
3. Turns on the LCD
4. Waits for five seconds
5. Turns off the LCD

The code is well documented and easy to follow. A National Semiconductor logo, in 320x240x2 format (2 bits per pixel), is included in the NSDEMO program as an array, found in the file “LCDBM.C”. This array also includes the “Gray Scale Lookup Table” used by the NS486SXF LCD controller to provide high-quality gray scale output.

The “Gray Scale Lookup Table” (GLUT) data was generated by experimentation. NSDEMO uses a fixed GLUT that has a 75% duty cycle for dark-gray and a 50% duty-cycle for light-gray. The dark-gray entries for even rows is shifted by 1 step from the dark-gray entries for odd rows. This GLUT was shown (in experimentation) to provide good quality with the LCD hardware described in this application note. It is possible to dynamically update the GLUT during operation to provide even better gray-scale output. However, the 16 words of GLUT data used in NSDEMO proved sufficient for this application.

The “LCD_Test()” code uses DMA functions also included in NSDEMO to initialize the DMA for use by the LCD. This is fairly straight-forward, and well documented in the code. The byte count for the DMA transfer is set to 19,232. This is the size of the array in “LCDBM.C” which contains the 320x240x2 bitmap and the 32 bytes of GLUT data.

Frequency Calculations

After setting up the DMA controller, the LCDTEST code initializes the LCD controller. The trickiest part of the LCD controller setup is determining the divisor to write to the LCD_CFG2 register to generate the proper LCD clocks. Most LCD panels operate at somewhere near 60Hz. The Optrex LCD display used in this application provided the best quality output at just over 70Hz. Therefore, the NSDEMO code programs the LCD controller as close to 70Hz as possible.

The following formula can be used to determine the divisor to use when programming the NS486SXF LCD controller:

$$\text{Div} = \frac{\text{OSC_CLK}}{\text{F} * \left(\frac{\text{Rows} * \text{Columns}}{4} + (\text{Rows} * \text{Offset}) \right)}$$

In this formula, “Div” is the LCD divisor programmed in the NS486SXF. “OSC_CLK” is the oscillator clock speed of the NS486SXF (e.g., 50MHz for 25MHz CPU speed). “F” is the refresh frequency of the LCD panel. “Rows” is the number of rows on the LCD (e.g., 320 in a 320-240 LCD). “Columns” is the number of columns on the LCD. And “Offset” is the number of offsets programmed in the NS486SXF LCD controller. “Offset” is actually one greater than the value programmed in bits 3-0 of the LCD_CFG3 register, and can go from 1 to 16.

If you know the target refresh frequency (e.g., 70Hz), simply plug in the values and start with an offset of 1. The above equation would yield a divisor of 36.7 on a 320x240 display when OSC_CLK is 50MHz, F is 70Hz, and Offset is 1. The closest divisor the NS486SXF LCD controller supports is 36. The following equation can be used to determine the refresh rate when the other parameters are known:

$$\text{F} = \frac{\text{OSC_CLK}}{\text{Div} * \left(\frac{\text{Rows} * \text{Columns}}{4} + (\text{Rows} * \text{Offset}) \right)}$$

Using the divisor of 36 and other values from the previous calculation (except for refresh rate, which is being calculated here) a rate of 71.4Hz is obtained.

Once the divisor is generating a refresh rate close to that desired, the “Offset” value can be increased to slow down the refresh rate slightly. For example, in the above calculations it was determined that the divisor of 36 results in a 71.4Hz refresh rate. But we initially wanted a 70Hz refresh rate. Using an offset of 2 results in a rate of 70.6Hz, and an offset of 3 results in a rate of 69.7Hz. These two results are close to the target frequency.

In practice, it is best to experiment with the divisor and offset to generate an optimal LCD image for the particular LCD panel used. The above equations make this easy.

The equations were determined from the LCD figures in the NS486SXF datasheet. Each CL2 clock (the dot clock) shifts out 4 bits of data. Therefore $((\text{Rows} * \text{Columns}) / 4)$ represents the number of CL2 clocks per frame. The programmed offset adds a delay after each row, so $(\text{Rows} * \text{Offset})$ is added to the number of CL2 clocks. The OSC_CLK divided by the programmed LCD divisor is the frequency of CL2. Given this info, the previous equations were easy to determine.

It should be noted that the NS486SXF LCD controller supports 28 divisors. 21 of these can be used when the SXF is operating above 16MHz (OSC_CLK of 32MHz). Appendix A shows the resulting refresh rate for the supported divisors at 20 and 25MHz operation (OSC_CLK of 40 and 50MHz).

Power Sequencing

After the DMA and LCD controllers are set up, NSDEMO enables the LCD panel. This is done as follows:

1. Set OUT1 active (OUT1 bit high, OUT1# pin low)
2. Delay 1ms
3. Enable the LCD controller (turn signals on)
4. Delay 1ms
5. Set OUT2 active (OUT2 bit high, OUT2# pin low)

As mentioned before, the Optrex LCD display enable signal is only activated when both OUT1# and OUT2# are active. NSDEMO sequences these two pins separately to support other types of LCD panels that require additional power sequencing steps. In a system that required a power sequencing step before the LCD signals are started (such as the Sharp display documented earlier), the OUT1# signal could be used directly (or inverted) to trigger the correct power sequencing logic.

All the Rest

After enabling the LCD panel, NSDEMO simply waits 5 seconds, then performs the power down sequence. This is the opposite of the power up steps outlined above. At this point the DMA channel could be masked off if desired; however, NSDEMO just leaves it alone since the LCD controller will not drive the DMA request when it is disabled.

Testing the Hardware

After building the LCD hardware, it should be tested before connecting the LCD panel to avoid damaging the LCD itself. All checks should be performed at the connector that goes to the LCD panel. The following checks should be performed:

1. Connect the LCD hardware, without the LCD panel, to the evaluation board and turn on power to the board. At this point check that Vcc is at +5V. Check that Vss is at +0V (ground). The Dispoff signal should be low (display disabled).
2. With the board still powered on, check the Vee voltage. Adjust the 50K Ω trimmer until Vee is at -24V.
3. With the board still powered on, check the Vadj voltage. Make sure that it goes from about -5V to -24V by adjusting the 500K Ω Pot.
4. Check the AC voltage between the two pins on the LCD backlight connector. They should be at around 170V. If desired the LCD backlight can be connected (with the power off) to the hardware (do not connect the other LCD connector). When the evaluation board is on, the backlight should light up. **Note: this AC voltage could be high enough to cause physical harm. Please perform this check carefully, and only if you are comfortable with performing this check. Due to the simple connection of the DC-AC Inverter, this voltage is unlikely to be in a state that would harm the LCD backlight.**

The other checks require stepping through the NSDEMO code. The SSI, Pharlap, or On-Time tools included with the evaluation board may be used to perform these tests. Note that the Pharlap evaluation version debugger (bedbug) does not support source-level debugging, so it may be easier to use the SSI or On-Time tools. Information on running NSDEMO is included with the evaluation board. After loading NSDEMO with the debugger of choice, the following tests may be performed.

1. Go to the LCD_Test() function.
2. Set a breakpoint and run to the 1ms delay after the LCD signals are started (the second 1ms delay).
3. At this point, check that the Dispoff signal is still low and other voltages are correct as tested earlier.
4. Check that the FLM, LP, CP, and M clock signals are running. On a 25MHz evaluation board, these signals should be close to the following values:
 5. FLM (CLF) 71Hz
 6. LP (CL1) 17.8kHz
 7. CP (CL2) 1375Hz
 8. M 142Hz
9. Now step or break after the second LCD enable step (break in the “LCD is running” code).
10. Check that all signals are the same except Dispoff, which should now be high.

You may want to step through the rest of the LCD code and make sure the Dispoff signal (first) and the LCD clocks (second) are stooped as indicated in the code.

At this point, if all tests were passed, it should be safe to power down the board, connect the LCD panel, and run NSDEMO. You may want to break at the point where the LCD is running (so that the LCD image is not shut off after 5 seconds). If all is working, you should see a National Semiconductor logo on the LCD using all four gray levels. You may need to adjust the contrast (500K Ω Pot) to see the image well. If anything appears to be wrong, shut off power immediately to avoid damaging the LCD, and go recheck the signals as described earlier.

Please email any questions or problems you have to ns486@arador.nsc.com.

Appendix A - LCD Refresh Rate Table

The following table shows the refresh rates generated by the NS486SXF LCD controller for in a 320x240 configuration with one offset. The results were generated from the formula shown earlier. Adding offsets will slow the refresh frequency shown, thus allowing fine tuning of the output.

| Divisor | 25MHz | 20MHz | LCD_CFG2 (7-3) |
|---------|--------|--------|----------------|
| 4 | 643.00 | 514.40 | 0x40 |
| 6 | 428.67 | 342.94 | 0x48 |
| 8 | 321.50 | 257.20 | 0x80 |
| 10 | 257.20 | 205.76 | 0x50 |
| 12 | 214.33 | 171.47 | 0x88 |
| 14 | 183.72 | 146.97 | 0x58 |
| 16 | 160.75 | 128.60 | 0xC0 |
| 18 | 142.89 | 114.31 | 0x60 |
| 20 | 128.60 | 102.88 | 0x90 |
| 22 | 116.91 | 93.53 | 0x68 |
| 24 | 107.17 | 85.73 | 0xC8 |
| 26 | 98.92 | 79.14 | 0x70 |
| 28 | 91.86 | 73.49 | 0x98 |
| 36 | 71.44 | 57.16 | 0xA0 |
| 40 | 64.30 | 51.44 | 0xD0 |
| 44 | 58.45 | 46.76 | 0xA8 |
| 52 | 49.46 | 39.57 | 0xB0 |
| 56 | 45.93 | 36.74 | 0xD8 |
| 72 | 35.72 | 28.58 | 0xE0 |
| 88 | 29.23 | 23.38 | 0xE8 |
| 104 | 24.73 | 19.78 | 0xF0 |

Divisor is the total divisor programmed in the LCD Configuration Register 2 (LCD_CFG2). There are two components, a binary and an integer divisor. The Divisor in the table is the total programmed divisor, or the binary divisor times the integer divisor.

The 25MHz and 20MHz tables list the refresh rate (in Hz). This number is the number of times per second the entire LCD image will be updated. Please note that the LCD panels generally only support a small range of frequencies around the 60 or 70Hz. Also note, some of these entries may be too fast for the DMA controller to handle, so the smaller divisors may not be useable.

The LCD_CFG2 column lists the value of bits 7-3 programmed in LCD Configuration Register 2 for the given divisor. The lower three bits indicate the screen size and gray-scale mode, and should be logically OR'ed with this value before programming it in the register. Bits 2 and 1 of the LCD_CFG2 register select the screen size of the LCD. Bit 1 of the LCD_CFG2 register selects 1 or 2 bits per pixel operation. Consult the datasheet for specifics.

Appendix B - Bill of Materials

This is the bill of materials for the main components for the LCD system documented in this application note. This list includes all components shown in the schematics, but does not include physical components (casing, cables, plugs, etc.)

Please note that the power parameters for the discrete components are what we used, but may not be appropriate for all designs. No analysis was done on the required parameters of the resistors, capacitors, and inductor. Although we used “F” family logic (74F112, etc.) other families would work just as well if they interface correctly to the LCD panel.

| Ref | Part/Value | Description | Manufacturer | Misc |
|-----|---------------|--|--------------|-------------------------|
| U1 | LM78S40 | Universal Switching Regulator | NSC | |
| U2 | 74F32 | Quad 2-Input OR gate, 14-pin Dip | NSC | |
| U3 | 74F04 | Hex Inverter, 14-pin Dip | NSC | |
| U4 | 74F112 | Dual JK Flip-Flop, 16-pin Dip | NSC | |
| U5 | CXA-L10L | DC-AC Inverter | TDK | Digi-Key OP006-ND |
| R1 | 1 Ω | Carbon Resistor, 1/8W 5% | | |
| R2 | 100 Ω | Carbon Resistor, 1/8W 5% | | |
| R3 | 750 Ω | Carbon Resistor, 1/8W 5% | | |
| R4 | 1.2K Ω | Carbon Resistor, 1/8W 5% | | |
| R5 | 100K Ω | Carbon Resistor, 1/8W 5% | | |
| R6 | 50K Ω | Cermet Trimmer (Variable Resistor) | Bourns | |
| R7 | 500K Ω | Potentiometer Linear Taper 1/4” MTG | Caltronics | |
| Q1 | 2N2905 | Transistor | NSC | |
| L1 | 820 μ H | Inductor, 40mA DC | J.W. Miller | |
| C1 | 4700pF | Capacitor, Molded Monolithic, 63V | | |
| C2 | 33 μ F | Capacitor, Tantalum, 35V | | |
| D1 | 1N4003 | Diode | | |
| D2 | 1N4148 | Diode | | |
| | DMF50081NB-FW | LCD Panel, 320x240, blue/white | Optrex | Digi-Key OP320240-ND |

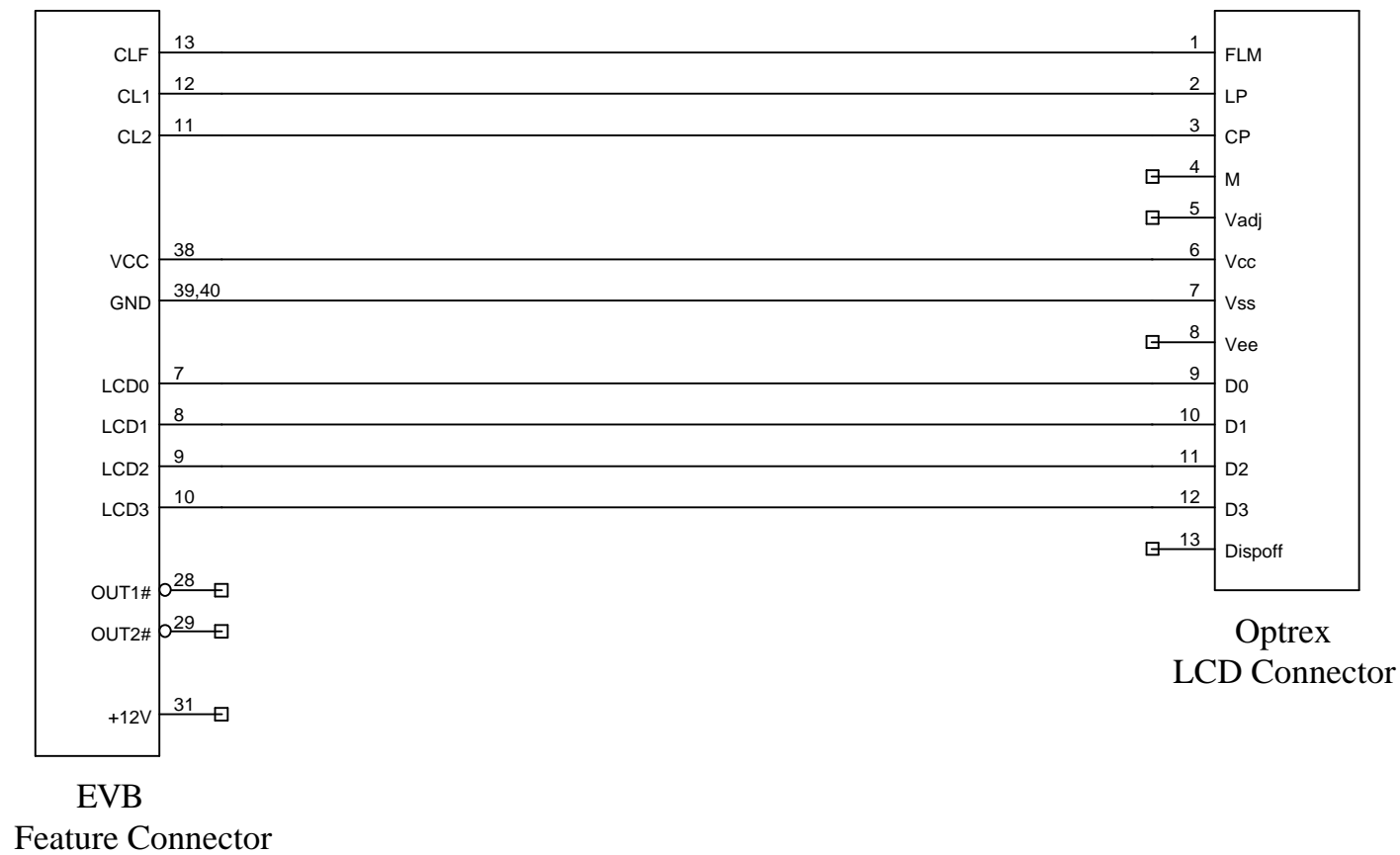
Manufacturer indicates the brand of part used on the prototypes at National Semiconductor, but other equivalent parts may be available.

Datasheets for the Optrex LCD panel and TDK DC-AC Inverter are available from the manufacturers and/or distributors, and may be a useful reference, as their components are not described in this application note.

Appendix C - Schematics

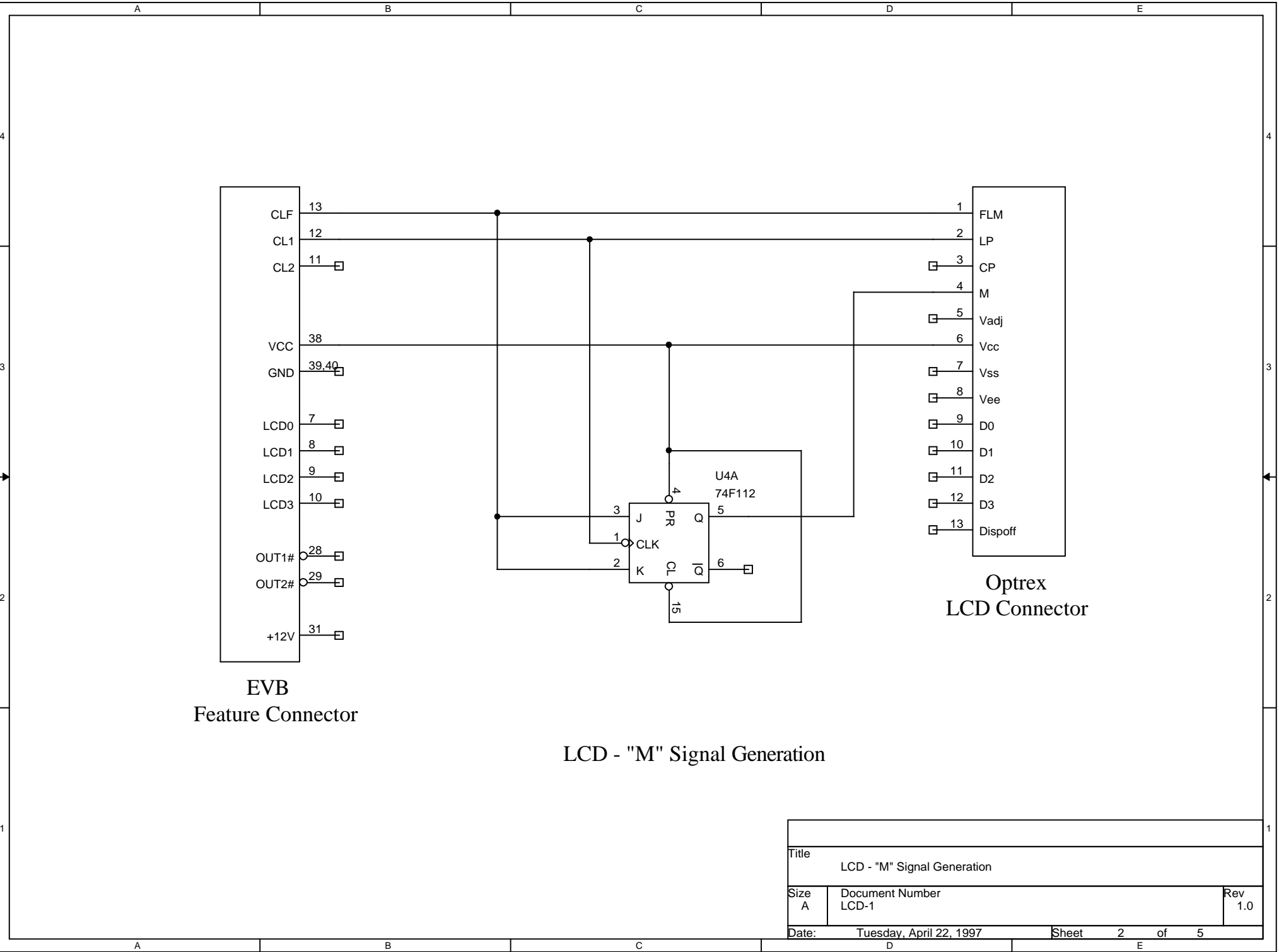
The following five pages are the schematics for the hardware described in this document. They are broken down into functional components as described in this application note.

1. LCD - Direct Connections
2. LCD - “M” Signal Generation
3. LCD - “Dispoff” Signal Generation
4. LCD - Voltage Generation
5. LCD - Backlight Connection



LCD - Direct Connections

| | | | |
|-----------------------------------|--------------------------|--------------|------------|
| | | | 1 |
| Title LCD - Direct Connections | | | |
| Size A | Document Number LCD-1 | | Rev 1.0 |
| Date: Tuesday, April 22, 1997 | | Sheet 1 of 5 | |

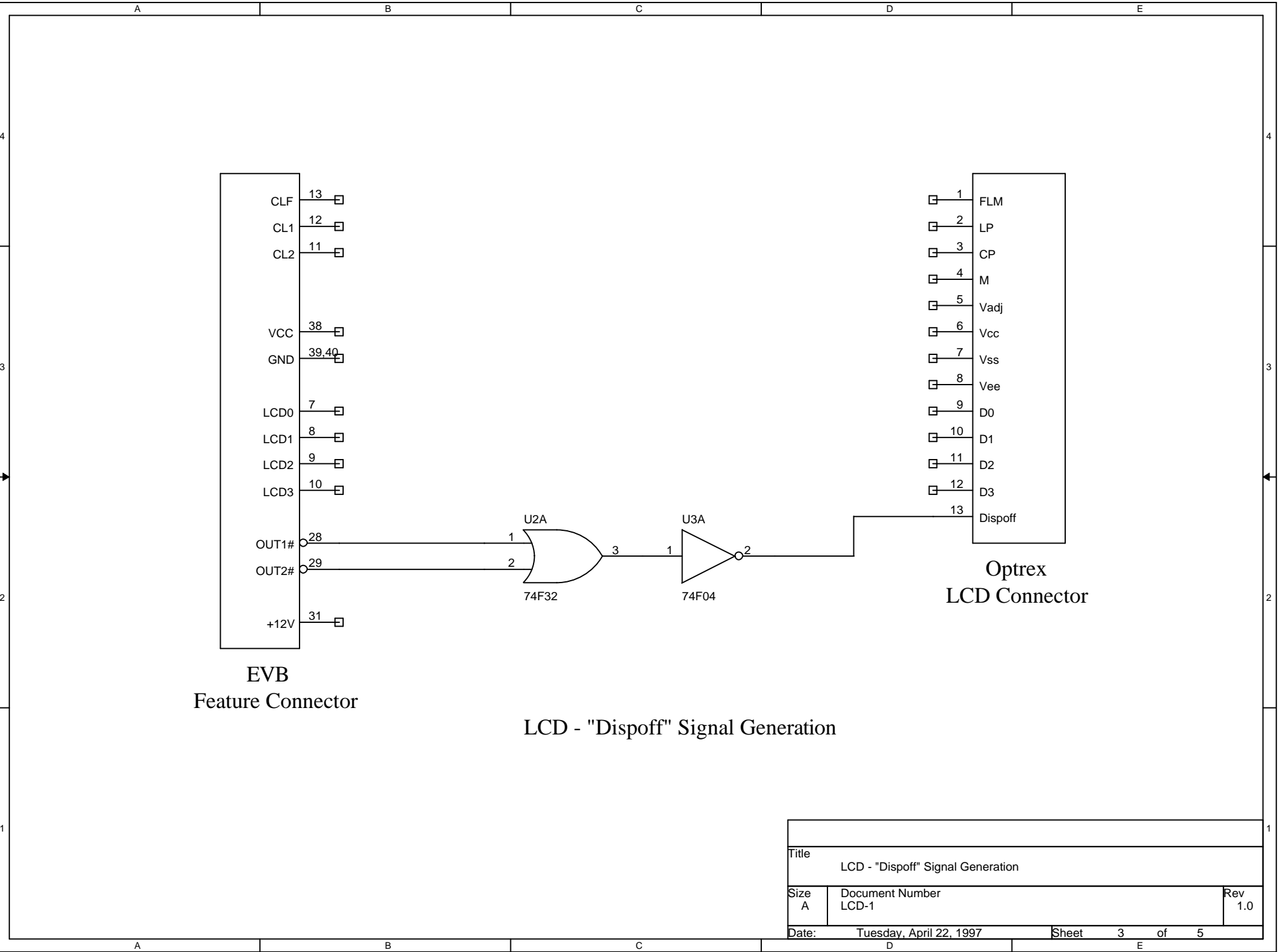


EVB
Feature Connector

Optrex
LCD Connector

LCD - "M" Signal Generation

| | | |
|-------------------------------|-----------------|-----|
| Title | | |
| LCD - "M" Signal Generation | | |
| Size | Document Number | Rev |
| A | LCD-1 | 1.0 |
| Date: Tuesday, April 22, 1997 | | |
| Sheet 2 of 5 | | |



EVB
Feature Connector

Optrex
LCD Connector

LCD - "Dispoff" Signal Generation

| | | |
|-----------------------------------|-----------------|-----|
| Title | | |
| LCD - "Dispoff" Signal Generation | | |
| Size | Document Number | Rev |
| A | LCD-1 | 1.0 |
| Date: Tuesday, April 22, 1997 | | |
| Sheet 3 of 5 | | |

