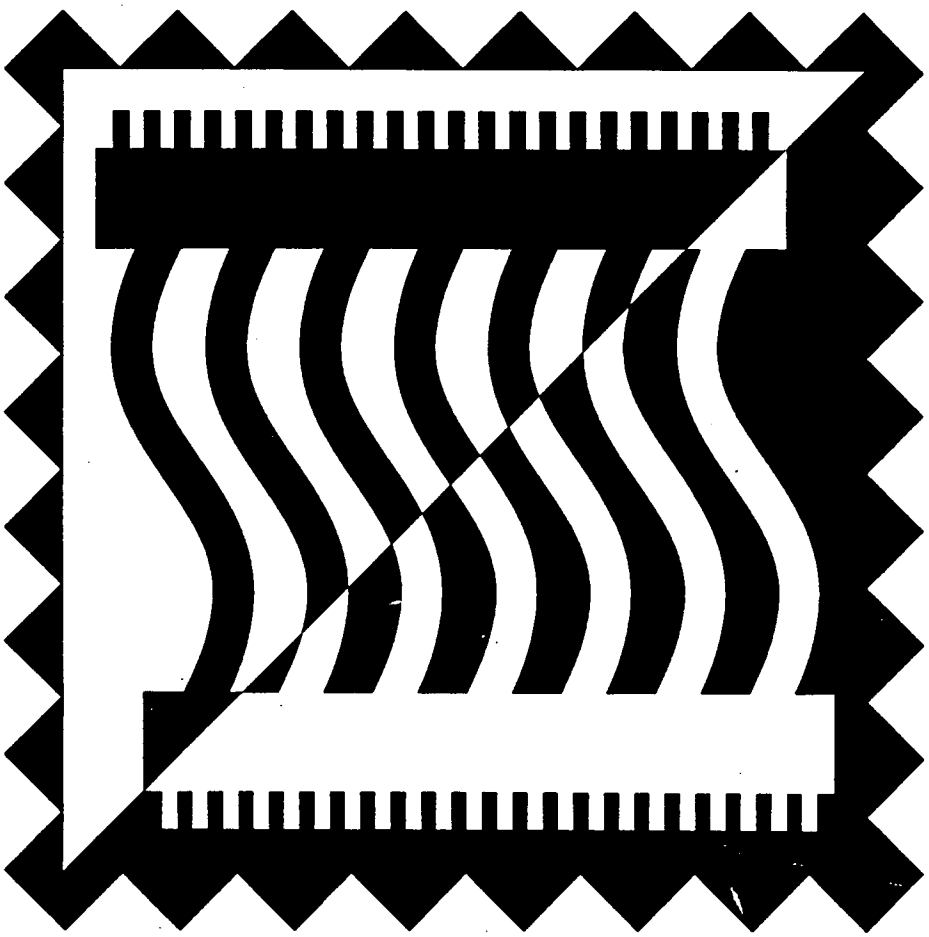
53CF94/96-2
Fast SCSI Controller

NCR



Data Manual

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Preface

SCSI Specifications

This manual assumes some prior knowledge of current and proposed SCSI standards. For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10018
(212) 642-4900
Ask for document number X3.131-1986 (SCSI-1)

Global Engineering Documents
2805 McGaw
Irvine, CA 92714
(800)-854-7179 or (714) 261-1455
Ask for document number X3.131-198X (SCSI-2)

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia*

Prentice Hall
Englewood Cliffs, NJ 07632
(201) 767-5937
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

NCR SCSI Electronic Bulletin Board
(719) 574-0424

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Chapter One
Fast SCSI Controller Introduction

General Description

The 53CF94 and 53CF96 are high performance CMOS devices designed to maximize SCSI transfer rates. They are pin-compatible with the NCR 53C94 and 53C96 Advanced SCSI Controllers, and conform to ANSI standards X3.131-1986 (SCSI-1) and X3.131-199X (SCSI-2). The Fast SCSI Controller (FSC) includes all the functionality of the 53C94/96, plus additional features including Fast SCSI, NCR TolerANT® technology, a 24-bit transfer counter, and a part-unique ID code which includes the chip revision level.

The 53CF9X Family is a second-generation SCSI controller that reduces protocol overhead by performing common SCSI sequences in hardware, in response to a single command. The 53CF94 and 53CF96 will operate at sustained data transfer rates up to 10 MB/s in synchronous mode and 7 MB/s in asynchronous mode. Refer to the *Data Transfer Rate* section in *Chapter 2, Functional Description*. The 53CF94 has on-chip 48 mA drivers for single-ended transmission, while the 53CF96 offers both single-ended and differential mode operation in a single 100-pin Quad Flat Pack (QFP) package.

The microprocessor bus width is eight bits. It may be configured separately from the 16-bit DMA bus (a dual bus configuration) or to share the lower half with the DMA bus (a single bus configuration). The chip operates in four different host bus configurations, two single bus modes and two dual bus modes. The dual bus architecture separates the Data Bus and the Processor Address Data Bus, two high-traffic information flows in the system, to maximize efficiency and throughput. The modes are selected by strapping the Mode 0 and Mode 1 signals high or low. The configuration modes are described fully in the *Host Bus Configuration* section of Chapter 2, *Functional Description*. They are illustrated in *Appendix B, Bus Configurations*.

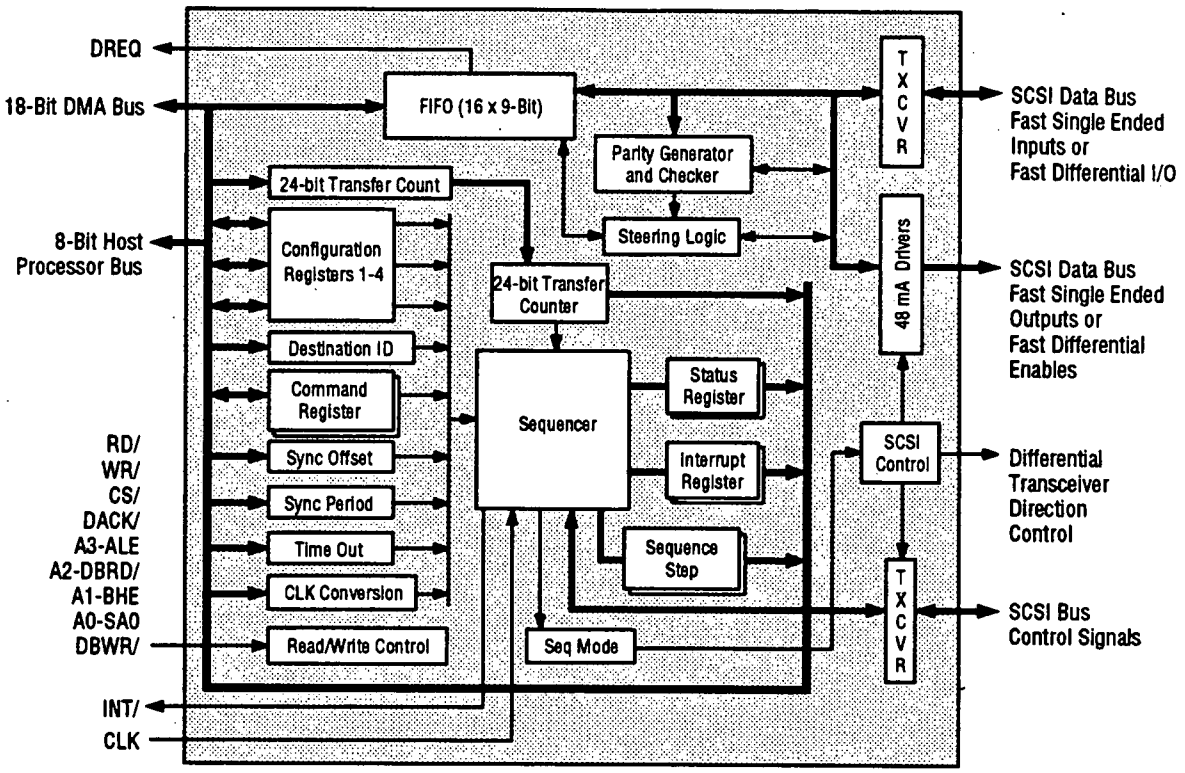
NCR TolerANT Technology

The 53CF94/96 features NCR TolerANT Technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI REQ, ACK, Data and Parity signals to be actively driven high faster than passive pull-up drivers. Active Negation is enabled by setting bit 2 in the Configuration 4 register. TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signal to eliminate unwanted transitions without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps to eliminate the double clocking of data, which is the single biggest data reliability problem with the SCSI interface. The benefits of TolerANT include increased immunity to noise when the signal is going high, increased performance due to balanced duty cycles, and improved Fast SCSI transfer rates. It can be used in both single-ended and differential mode. TolerANT is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

Features

- SCSI-2 compatible
- Up to 7 MB/s sustained asynchronous SCSI transfer rate
- Up to 10 MB/s sustained synchronous SCSI transfer rate
- NCR TolerANT technology provides:
  - Active negation pad cells on the SCSI Data, Parity, REQ and ACK pins to improve Fast SCSI-2 performance in single-ended and differential modes
  - Input signal conditioning on the REQ and ACK lines
- 24-bit transfer counter eliminates inter-sector transfer delays and allows single transfers up to 16 MB
- 20 MB/s DMA interface
- SCSI-2 tagged-queuing
- Improved scatter/gather operation
- Software compatible with 53C90 family
- On-chip 48 mA drivers
- Control logic for differential transceivers
- 8-bit multiplexed and non-multiplexed address/data bus interface
- DMA Burst Mode, Byte Control Mode, Threshold 8 mode, Save Residual Byte option, Misaligned Transfer handling supported
- Parity generation, optional checking
- Parity pass-through
- Supports clock frequencies from 10-40 MHz
- Low power CMOS
- 84-pin PLCC and 100-pin QFP
- Minimum 2K volts ESD protection
- Latch-up protection greater than 100 mA
- Typical 350 mV SCSI bus hysteresis
- Voltage feed-through protection

Figure 1-1. Functional Block Diagram



Chapter Two
Functional Description

The Fast SCSI Controller (FSC) has a command set that allows it to perform common SCSI sequences at hardware speed without host intervention. Its on-chip FIFO may be accessed simultaneously by the SCSI bus and either the microprocessor or the host DMA controller. All command, data, status and message bytes pass through the FIFO on the way to or from the SCSI bus. Most FSC commands have two versions: DMA and non-DMA. When DMA instructions are used, data will pass between memory and the SCSI bus with the FIFO acting as temporary storage when the DMA channel is temporarily shut down by a higher priority event, such as DRAM refresh.

The FIFO also helps speed execution during non-DMA transfers. For example, in initiator role, the microprocessor will load the Command Descriptor Block (CDB) and optionally, one or three message bytes into the FIFO. It will then issue one of several selection commands and wait for an interrupt. The FSC will wait for bus free, arbitrate for the bus until it acquires it, send the message bytes followed by the CDB, then generate an interrupt. Meanwhile, a multi-tasking host may continue with other tasks.

The 53CF94/96 is the newest member of the NCR 53C90 family, with additional features such as Fast SCSI transfer rates, a 24-bit transfer counter, an ID register, NCR TolerANT, and improved scatter/gather operation. The 24-bit transfer counter and the ID register are described in Chapter Four, *Registers*.

Typical SCSI Operation

In target role, the microprocessor will enable selection and then wait for an interrupt. Eventually an initiator will select the FSC. It will then automatically step through the selection and command phases before generating an interrupt. When the interrupt occurs, the entire CDB will be in the FIFO along with any message bytes sent by the initiator.

After the selection phase has been successfully completed, the FSC may transfer bytes in any SCSI information phase whether it is operating in initiator or target role. The FSC supports disconnect/reselect in both initiator and target roles, making high performance multi-threaded systems easy to implement.

The FSC may transfer data phase bytes across the bus synchronously, at speeds up to 10 MB/s, or asynchronously, at speeds up to 7 MB/s. Refer to the *Data Transfer Rate* section in this chapter for more information. The difference between asynchronous and synchronous operation is transparent to the user except that the synchronous offset and the synchronous transfer period registers must be programmed prior to synchronous data transfer. The default, after hardware or software reset, is asynchronous transmission.

Data phase bytes will usually be transferred using DMA. The microprocessor will program an external DMA controller, program the FSC transfer count register, issue one of several FSC data transfer commands, then wait for an interrupt. The DMA controller and the FSC will transfer all the data without microprocessor intervention.

To end the SCSI transaction, the FSC target will place a status byte and a message byte in the FIFO. It will then issue one of two single commands which will cause the FSC to first assert Status phase, send the first byte, assert Message In phase, send the second byte, disconnect from the SCSI bus (after the initiator releases Acknowledge [ACK]) and interrupt the microprocessor.

The end of a SCSI transaction is similar for an FSC initiator except that it receives two bytes into its FIFO. The initiator prevents the target from disconnecting by holding ACK asserted on the bus while the microprocessor examines the status and message bytes. If both bytes are acceptable, the Message Accepted command is used to instruct the FSC to release ACK, which allows the target to disconnect and causes the initiator to interrupt its host and report the disconnect. If the status and message bytes are not acceptable, the host could first issue the Set Attention (ATN) command before issuing the Message Accepted command. This instructs the FSC to assert ATN before releasing ACK, which should cause the target to request Message Out phase rather than disconnect.

Bus Initiated Sequences

- Selection
- Reselection
- SCSI bus reset

Selection or reselection sequences occur in the disconnected state when the FSC is selected or reselected by another initiator or target, if the Enable Selection or Reselection command has previously been received by the FSC.

In addition to responding to bus initiated events, the FSC may initiate a bus event by using one of several selection or reselection commands. If one of these commands starts executing, *the Enable Selection or Reselection command will be cleared* after arbitration has been won, preventing the FSC from responding to a Select or Reselect command. Normally the microprocessor will have 250 ms (ANSI recommended selection time-out period) after the chip disconnects from the bus to re-enable bus initiated events. If the time-out period is exceeded, an initiator or target attempting to connect to the FSC may time-out and abort.

If, on the other hand, the bus initiated event occurs before the command starts executing, the FIFO and command register will be cleared and any further writes by the microprocessor will be ignored until the Interrupt register is read. Since a selection or reselection command requires that something be placed in the FIFO, these bytes will be lost, as will any command written to the Command register. The interrupt handler that services a selection or reselection command will have to examine the bits in the Interrupt register to determine if the FSC selected another device, or if it was selected by another device. The former case will cause a Function Complete Interrupt, the latter case will cause a Selection or Reselection interrupt.

Bus Initiated Selection

When the FSC has been selected as a target, the following data will be in its FIFO:

- Bus ID
- Identify message
- Optional two-byte command queuing message
- Command Descriptor Block (CDB)

The bus ID will always be present and will always be one byte. It is an un-encoded version of the state of the bus during Selection phase. Any SCSI data bits that were true during Selection phase will be set. The target ID must always be set. In arbitrating systems, the initiator ID must also be set. The initiator ID is optional in non-arbitrating systems. If parity checking is enabled, parity must be valid during the bus initiated selection. If parity is not valid, the FSC will not respond to bus initiated selection.

The identify message, if sent, will also be placed in the FIFO. The identify message is optional in SCSI-1 systems but will always be one byte if it is used. In SCSI-2 systems a one or three byte message will be sent, consisting of the one-byte identify message and an optional two-byte command queuing message. If the FSC is selected with ATN false, it will store a null byte (00) in the FIFO behind the bus ID, then begin requesting command phase bytes. A detected parity error will cause the FSC to interrupt and stop, if parity checking is enabled.

If the FSC is selected with ATN true and the SCSI-2 bit is not set, it will request one message byte and place it in the FIFO behind the bus ID. Then it requests Command phase bytes unless the message byte is not a valid identify message (bit 7 in the Config 3 register is not set), or a parity error is detected, which will cause the FSC to interrupt and stop. The Sequence Step register can then be examined to determine what events have been completed.

If the FSC is selected with ATN true and the SCSI-2 bit set, the FSC will examine both the message byte and the ATN signal to determine how many bytes to request. If the first byte is a valid identify message and if ATN goes false after receiving the first byte, the FSC will change to Command phase. If the first byte is a valid identify message byte and ATN is still true, it will request two more message bytes. After requesting the message bytes, the FSC requests Command phase bytes unless one of the following situations occurs:

1) The first byte is not a valid identify message
2) A parity error is detected
3) ATN goes false between the second and third bytes
4) ATN remains true but the SCSI-2 bit is false.

All of these conditions cause the FSC to interrupt and stop.

To determine if one of the above situations has occurred, examine the Sequence Step register.

The CDB will always begin at the third or fifth byte in the FIFO, assuming selection completed normally. The CDB may be 6, 10 or 12 bytes long. Thus, in SCSI-2, the entire FIFO may be filled if a tagged-queuing 12-byte command is used.

Bus Initiated Reselection

The FSC will allow itself to be reselected as an initiator by a target if it has previously received the Enable Selection/Reselection command. If the sequence completes normally, the following information will be in the FIFO:

- Bus ID
- Identify message
- Optional 2-byte queue tag message

The bus ID will always be present and will always be one byte. It is an un-encoded version of the state of the bus during Reselection phase.

The identify message will always be present and will always be one byte.

If queue tagging is enabled, and the target is sending a queue tag message, the target will also send two queue tag message bytes.

Bus Initiated Reset

A SCSI bus initiated reset will be recognized by the FSC at any time. When SCSI RST/ pulses true, the FSC will disconnect from the bus and reset its internal sequencer. If bit 6 in Config l register is not set, the FSC will generate a SCSI reset detected interrupt.

Stacked Commands

The Command register is a two-deep, eight-bit read/write register used to give commands to the FSC. If DMA commands are to be stacked, the Transfer Count must be loaded prior to loading the respective command. Command stacking should only be usedduring Data In and Data Out. If stacked commands are used in Initiator mode, it is recommended that the Features Enable bit in the Config 2 register be set. This will cause the SCSI phase lies to be latched at the end of a command.

Parity Checking and Generation

The FSC has six bits that control parity generation and checking. Four of these bits can be accessed by the user and are described in Table 2-1. If parity checking is disabled, the FSC does not check for parity errors. In this document, the word *detected* in conjunction with *parity error* should be understood to imply that parity checking has previously been enabled.

In Target role, detected parity errors will set the Parity Error bit (bit 5 in the Status register) and clear the Command register without causing an interrupt. In Initiator role, detected parity errors will set the Parity Error bit and assert ATN (Attention) prior to releasing ACK (Acknowledge). Parity errors occurring after a phase change to Synchronous Data In are handled slightly different in Initiator mode. Refer to Chapter 5, *Command Set*, for more information on initiator commands.

Configuration 2 register bit 2, the Target Bad Parity Abort bit, allows special handling for parity errors. When this bit is set, the chip will abort a Receive command or Receive Data command if bad parity is received from the SCSI bus. If a parity error occurs when the Target Bad Parity Abort bit is set, the Status Register Parity Error bit (bit 5) will be set, but no additinal bits will be set in the Interrupt or Status registers after bad parity is detected. The Transfer Counter and FIFO Flags registers contain a record of how many bytes were transferred before the command was aborted.

For additional information on the parity bits, refer to the register descriptions.

The 53CF94, 95, and 96 have two parity pins (DBP0, DBP1) that may always be used by the DMA, and may be used by the host processor if configured for Bus Configuration Mode One. In

Mode Two and Mode Three, the processor connects to the FIFO on an 8-bit bus only. In these modes, the internal parity generator creates parity to send to the SCSI bus.

When the DBP pins are enabled, parity may pass between the SCSI and host buses without change or may be generated by the FSC from the data byte. Whether generated internally or externally, the parity bit is always loaded into the FIFO along with the data byte. From there on, it moves through the FIFO along with the data byte. The FIFO may be accessed by three buses: SCSI bus, microprocessor bus or host DMA bus.

If parity test mode is enabled, the DBP0 is a duplicate of DB7 and DBP1 is a duplicate of DB15. This is true both for data flowing from the FIFO to the SCSI Data Bus (SDB) pins or data flowing from the FIFO to the Host Data Bus (DB) pins.

The FSC flags parity errors as data comes into the FIFO from the SCSI bus, or as it leaves the FIFO on its way out to the SCSI bus.

Host Bus Configuration

The DMA and microprocessor buses may be configured in one of the four ways shown below.

Mode Description

Zero Single bus; 8-bit DMA, 8-bit processor bus.

One Single bus; 16-bit DMA, 8-bit processor bus.

Two Dual bus; 8 or 16-bit DMA bus with byte control and 8-bit multiplexed processor address/data bus.

Three Dual bus; 16-bit DMA bus and 8-bit non-multiplexed processor bus.

Table 2-1. Parity Control

Control Bit	Data Direction	Bit Set	Bit Not Set
Parity Checking Config 1, bit 4	**SCSI to FIFO**	Enable parity checking and error reporting. SDBP loaded into FIFO	Disable parity checking and error reporting. Parity generator to FIFO
Test parity Config 1, bit 5	**FIFO to SCSI**	SDBP is replica of SDB7	FIFO to SDBP
	FIFO to memory	DBP0 is replica of DB7 DBP1 is replica of DB15	FIFO to DBP0, DBP1
DMA parity Config 2, bit 0	**DACK/ to FIFO**	DBP to FIFO	Parity generator to FIFO
	FIFO to SCSI	Enable parity checking and error reporting	Disable parity checking and error reporting
Register parity Config 2, bit 1	**CS/ to FIFO**	DBP to FIFO	Parity generator to FIFO
	FIFO to SCSI	Enable parity checking and error reporting	Disable parity checking and error reporting

The operating mode is selected by the Mode 1 and Mode 0 strapping pins; refer to Chapter 3, *Pin Descriptions*, for the setting of each mode. The four operating modes are labeled Mode Zero through Mode Three. These names are derived from the binary encoded state of the mode configuration pins with the Mode 1 pin being the most significant bit. Refer to Appendix B, *Bus Configurations*, for configuration diagrams. In both single bus modes, the DMA and the microprocessor share the same data bus. Therefore, CS/ and DACK/ must never be true at the same time when operating in single bus mode. Conversely, both dual bus modes have separate data buses for DMA and microprocessor, which may be active simultaneously provided CS/ is not accessing the FIFO.

Bus Configuration Mode Zero

In this mode, the 16-bit FSC becomes functionally identical to the 8-bit NCR 53C90B. Bus Configuration Mode 0, a single-bus configuration, is primarily for testing purposes. In this mode, the PAD bus is not used and the Data bus is configured for 8-bit operations. The DB bus handles both the microprocessor interface and DMA activity over the DB7-0 lines with DBP0 for parity; the DB15-8 lines are not used.

In this mode, the register address is carried by the A3-0 lines and is latched into the chip on the high to low transition of CS/. The direction of the access is determined by the RD/ and WR/ pins. CS/ must also be active. In Bus Configuration Mode Zero, DMA read data is driven by the chip when DACK/ is true.

Note: The WR/ and DBWR/ strobes must be tied together in the single bus configurations.

Bus Configuration Mode One

In Bus Configuration Mode One, another single-bus configuration, the PAD bus is not used and the Data bus is configured for 16-bit operations. In this mode, the register address is carried by the A3-0 lines and is latched into the chip on the high to low transition of CS/. The direction of the access is determined by the RD/ and WR/ pins. CS/ must also be active.

In this mode, registers are accessed over the DB7-0 lines with DBP0 for parity. For non-FIFO access, DBP0 into the chip is ignored and DBP0 out of the chip is zero. For FIFO read accesses, FIFO parity is passed out of the chip to DBP0. If the Register Parity Enable bit is not set in the Configuration 2 Register for FIFO write accesses, FIFO parity is generated by the chip; if the register parity is enabled, DBP0 is passed into the FIFO. DMA transfers occur over the DB15-0 lines with DBP1 and DBP0 for parity, or over DB7-0 with DBP0 for parity.

Note: The WR/ and DBWR/ strobes must be tied together in the single bus configurations.

Bus Configuration Mode Two

In this dual-bus mode, 8 or 16-bit operations are supported by the DMA Data bus. The microprocessor interface is supported by the PAD bus. FIFO parity is not available for data transfers over the PAD bus, and the Register Parity Enable bit (bit 1) of the Configuration 2 Register should not be set. The direction of transfer is determined by the RD/ and WR/ lines. CS/ must be active during PAD bus accesses.

In Bus Configuration Mode Two, register addresses and register data are multiplexed on the PAD bus. The register address on the PAD3-0 lines is latched into the chip on the high to low transition of ALE (A3).

In bus configuration mode two, the Data bus default configuration is for 16-bit DMA transfers. Pin A2 functions as the Data bus read signal (DBRD/), which drives the DMA read data. Byte Control Mode, described under *DMA Operation*, is only available in Bus Configuration Mode Two. The bus width configurations are listed in Chapter Three, Signal Descriptions.

Bus Configuration Mode Three

Like Bus Configuration Mode Two, this dual bus mode is configured for 16-bit transfers. Bus Configuration Mode Three differs from Mode Two in that byte control mode is not available, and the register address is carried by the A3-A0 lines.

In this dual bus mode interface, DMA operations are supported by the DB bus, and the microprocessor interface is supported by the PAD bus. FIFO parity is not available for data transfers over the PAD bus, and the Register Parity Enable bit (bit 1 of the Configuration 2 register) should not be set. The direction of transfer is determined by the RD/ and WR/ lines. CS/ must be active during PAD bus accesses.

In Bus Configuration Mode Three, transfers occur on the microprocessor interface over the PAD bus, which operates as a non-multiplexed data only bus. The register address is carried by the A3-0 lines and is latched into the chip on the high to low transition of CS/.

DMA Operation

The FSC supports 8-bit and 16-bit DMA transfers, as well as misaligned transfers. The on-chip FIFO allows the FSC to support normal and burst mode transfers. The DMA interface protocol runs asynchronous to the chip clock. The DMA Request signal (DREQ) is asserted when the DMA is ready for a transfer to or from the DMA channel. DREQ is asserted only when the DMA Acknowledge signal (DACK/) is inactive, and is released on the leading edge of DACK/. DREQ remains asserted until the chip receives as many DACKs as it needs or can handle.

DMA Threshold

The threshold is the number of bytes in the FIFO that trigger DREQ. For DMA read, DREQ will be asserted when the FIFO contains at least the threshold number of bytes. For DMA write, the FIFO must be able to accept this number of bytes. For 8-bit DMA operation the normal threshold is one byte. For 16-bit operation the normal threshold is two bytes (one word). The transfer counter is always decremented by the number of bytes transferred, regardless of the size of the transfer threshold.

Normal DMA Mode

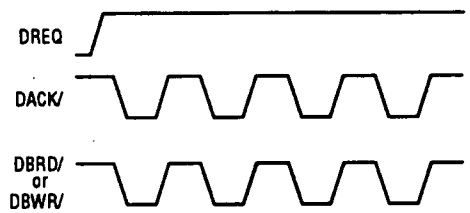
In normal operation, DREQ will remain true until the FIFO empties or fills, depending on the direction of the transfer. Figure 2-1 illustrates the case where the threshold is always exceeded. This is typical of a DMA interface that is slower than the SCSI device to which the system is connected.

Normal DMA mode tends to monopolize the DMA bus, and will slow the entire system down to the performance level of the SCSI device to which the chip is connected. In single-threaded systems, however, this remains the most efficient method of transferring data as long as important events, like DRAM refresh, can interrupt the DMA transfer.

In Bus Configuration Mode Zero, the FIFO may be accessed as an 8-bit device only. In Mode One, it may be accessed as a 16-bit device only. In Modes Two and Three, the FIFO may be accessed as either eight or 16 bits wide, depending on how the external DMA controller sets the signals BHE and A0.

The three 16-bit modes are complicated by the possibility of having a transfer begin or end on an odd byte address in system memory. Such transfers are called "misaligned." To accommodate this possibility, the FSC can be programmed to handle the first and last DMA transfer uniquely. One method of handling the single residual byte is discussed in the *Save Residual Byte* bit description below. The residual byte is the modulo 2 remainder at the end of a 16-bit DMA data stream. For additional information, refer to *Misaligned Transfers*.

Figure 2-1. Normal DMA Mode



Enhanced DMA Operation

DMA Burst Mode

Burst Mode, or Alternate DMA Mode, is a special mode devised for the 8237 DMA controller. If the controller being used has timings similar to the 8237, then burst mode guarantees that exactly four words will be transferred at one time until the transfer count drops below eight. Since many systems use one of the 8237 channels for DRAM refresh and since the 8237 will not recognize a higher priority request until it finishes its current transfer, Burst Mode gives the best transfer rate without sacrificing memory integrity.

DMA burst mode is enabled by setting both the Threshold Eight and the Alternate DMA Mode bits in the Config 3 register. Threshold Eight causes the FSC to delay assertion of DREQ until it can transfer eight bytes (four words). Alternate DMA mode causes the FSC to deassert DREQ after the third word transfer (or the seventh byte transfer if configured for 8-bit DMA), causing an 8237 DMA controller to relinquish the bus after exactly eight bytes have been transferred.

This regular surrendering of the DMA channel has benefits for two common DMA interface problems. For DMA controllers that do not recognize higher priority requests until the current device finishes, the FSC can periodically force DMA arbitration. This allows DRAM refresh and other operations to occur during SCSI operations. For DMA controllers that are much faster than the SCSI peripheral to which the system is connected, bus efficiency is improved by ensuring that the FSC has data to transfer while the DMA controller is controlling the bus.

DMA Burst mode can be enabled in any bus configuration. DMA Burst mode affects the deassertion of DREQ and assertion of DACK/ for DMA reads and writes.

Deassertion of DREQ

For most of the Burst Mode DMA transfer, exactly eight bytes will be transferred in each burst. However, if the number of bytes to be transferred is not an exact multiple of eight, then the FSC switches out of Burst Mode for the last one to seven bytes. The last bytes are transferred in Normal DMA mode where DREQ goes true and stays true as long as the FIFO is able to transfer data; DACK/ cycles true then false for each transfer. Because DACK/ must cycle true then false for every DMA transfer in this mode, Normal Mode is sometimes referred to as Single Transfer Mode.

- Single Transfer Mode: DREQ goes true and stays true as long as the FIFO is able to transfer data. DACK/ cycles true then false for every transfer.
- Multiple DMA transfers per DREQ: In Bus Configuration Modes Zero and One, DREQ is deasserted after the trailing edge of RD/. In Bus Configuration Mode Two, DREQ is deasserted after the trailing edge of DBWR/ or DBRD/. In Bus Configuration Mode Three, DREQ is deasserted after the trailing edge of DACK/ of the next-to-last DMA transfer. In Bus Configuration Mode Three, DACK/ toggles for each DMA read cycle. In other modes, DACK/ remains asserted throughout multiple transfers. DBWR/, DBRD/, or RD/ toggles for each DMA transfer.

DMA Read

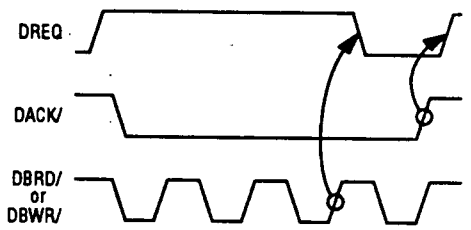
When DMA Burst Mode is enabled, the method by which DMA read data is transferred to the system bus depends on the bus configuration mode. The DMA read data is enabled onto the DB bus by DACK/ and either the RD/ or DBRD/ input signal, as described below.

- *Bus Configuration Modes Zero and One.* DMA read data is enabled when both RD/ and DACK/ are true. For multiple DMA transfers, DACK/ remains asserted throughout the multiple transfers and RD/ toggles for each transfer.
- *Bus Configuration Mode Two.* Data is enabled when both DBRD/ and DACK/ are true. For multiple DMA transfers, DACK/ remains asserted throughout the multiple transfers and DBRD/ toggles for each transfer.
- *Bus Configuration Mode Three.* Data is enabled when DACK/ is true. DACK/ toggles for each DMA transfer.

DMA Write

In DMA burst mode, the functionality of DACK/ and DBWR/ is unchanged for single DMA transfers per DREQ. For multiple DMA transfers per DREQ, DACK/ remains asserted throughout the multiple transfers and DBWR/ toggles for each transfer.

Figure 2-2. DMA Burst Mode



Misaligned Transfers

The 53CF94/96 family accommodates block data transfers beginning or ending on odd byte or odd word addresses in system memory. Such addresses are termed "misaligned." An odd byte is defined as one in which the address contains A0=1; an odd word is defined as one in which the address contains A1 = 1. Misaligned transfers differ depending on the type of transfer and whether they occur at the start or end of the transfer.

Note: None of the misaligned transfer techniques in this section are needed in Mode Two if Byte Control Mode is enabled.

Memory in 16-bit systems is structured such that words occupy two bytes and begin on an even address. An even address has its least significant bit equal to zero.

Words Aligned on Word Boundaries

Word Address 4
Word Address 2
Word Address 0

Even addresses are also known as word addresses, or word boundaries. When a word starts on a word boundary, the low byte of the word will be in an even byte address, while the high byte of the word will be in an odd byte address.

Two Bytes per Word

High byte of word	Low byte of word
Byte address 3	Byte address 2
Byte address 1	Byte address 0

When the word is written to an odd address, the low byte of the word resides in the upper half of a system word address. Its high byte resides in the lower half of the next system word address.

Misaligned Boundary

	High byte of word
Low byte of word	

Misaligned Transfers, Start of Transfer

Asynchronous/Synchronous, Sending Data to the SCSI Bus

If the transfer starts on an odd byte boundary, the first byte can always be preloaded into the FIFO by programmed I/O in either synchronous or asynchronous mode. To preload the FIFO, the microprocessor simply places the first byte in the FIFO before issuing the DMA command (any of the initiator or target transfer commands). Once the byte has been preloaded, a non-DMA transfer command can be issued, resulting in transfer over the SCSI bus of the preloaded byte. At this point, a DMA Transfer command can be issued to transfer the remainder of the data block. In each case, the transfer counter should be programmed with the number of bytes to be transferred by DMA.

Note: The FIFO cannot be preloaded when the FSC is in Target Synchronous Data Out phase.

Synchronous, Receiving Data from the SCSI Bus

Initiator Synchronous Data In

For initiator Synchronous Data In (data flowing into the FIFO from the SCSI bus), the Reserve FIFO Byte option may be used for transfers that begin on an odd address. Bit 7 of the Configuration 2 register enables this feature. The FIFO Bottom register can be loaded with the lower half of the destination word and a DMA Transfer Information command issued. When the first 16-bit word is moved via DMA from the FIFO to memory, the low byte will be overwritten with a copy of itself. The transfer counter should reflect the number of bytes transferred by DMA, including the extra byte not transferred on the SCSI bus. The Reserve FIFO byte is actually the bottom stage of the FIFO. Writing to the FIFO Bottom register will clear the Reserved FIFO Byte bit The high byte of this first word will be the first byte received over the SCSI bus. Subsequent bytes will be aligned as words and transferred 16 bits at a time.

Note: The Reserve FIFO Byte Enable bit must be set before the phase changes to Synchronous Data In. This means that the bit must be set before issuing the Select command.

Note: Reserve FIFO Byte is the only byte that can be loaded into the FIFO during the initiator Synchronous Data In phase. Any additional writes to the FIFO could corrupt FIFO data, or inerfere with the FSC's internal count of the outstanding REQ/ACK offset.

Target Asynchronous/Synchronous and Initiator Asynchronous

Option1: A non-DMA Receive Data/Transfer Information command can be used for the first byte and a DMA Receive Data/Transfer Information command for all subsequent words. Do not stack DMA commands with non-DMA commands.

Option 2: The Reserve FIFO byte can be preloaded with the lower half of the destination word and a DMA Transfer Information command issued; the transfer counter should reflect the number of bytes transferred by DMA, including the extra byte not transferred on the SCSI bus.

Note: In Target Synchronous mode the 53CF94 maintains an offset count between the number of REQs issued and the number of DACKs received (this is a measure of the unallocated space in the FIFO). Once the offset reaches 15, no further REQs are issued (even if the synchronous offset would allow further REQs), therefore only one byte may be preloaded. Loss of synchronization will occur in Option 1 if the FIFO is preloaded at the beginning of each series of back-to-back transfers.

Misaligned Transfers, End of Transfer

When there is a single byte remaining to be transferred at the end of a data block, the Save Residual Byte bit controls whether DREQ will be asserted. The Save Residual Byte feature, which is enabled by setting bit 2 in the Config-3 register, is operational only when the chip is receiving data, and when the chip is configured for 16-bit DMA. Its default state is not set, to maintain compatibility with earlier versions of the device which did not have this bit. When the bit is not set, DREQ will be asserted for the last byte of a data block.

In Bus Configuration Modes One and Three, this last DMA transfer will be a 16-bit transfer with the upper eight bits being driven to ones. Since the FSC can tell that only one byte was transferred rather than a word, the transfer counter is decre-

mented by one to zero. In Bus Configuration Mode Two, this last transfer will be either eight or 16 bits, depending on the external DMA controller. In either case, the transfer counter will decrement to zero.

When the Save Residual Byte bit is set, DREQ will not be asserted if there is a single byte left to be transferred across the DMA at the end of a data block. The microprocessor must move this last byte out from the FIFO. If the processor does not retrieve the residual byte, the byte is, in effect, preloaded into the FIFO and combined with other bytes during the next transfer. See *Misaligned Transfers, Start of Transfer* for more information on FIFO preloading.

Last Byte Transfer from Memory to SCSI Bus

If the transfer ends on an odd byte boundary, the transfer counter can be programmed for the total number of bytes minus one, the last byte can be transferred to the FIFO by programmed I/O, and a non-DMA transfer command used to flush the byte out to the SCSI bus. Save Residual Byte has no effect on transfers from memory to the SCSI bus.

Last Byte from SCSI to Memory

Target Synchronous /Asynchronous and Initiator Asynchronous

Option 1: The Save Residual Byte flag can be set and the transfer counter programmed for the total number of bytes to be transferred. The end of transfer interrupt will be generated when all the bytes have been transferred on the SCSI bus and one byte remains in the FIFO (DREQ will be deasserted). The residual byte can be removed by I/O. If the Save Residual Byte bit is not set, a 16-bit DMA transfer will result and the lower half of the byte will contain the last byte, with the upper byte driven to all ones.

Option 2: The transfer counter can be programmed for the number of bytes to be transferred minus one, and a DMA command issued. A non-DMA command can be used for the last byte of the transfer.

Initiator Synchronous Data In

Option 1: The Save Residual Byte bit can be set and the transfer counter programmed for the total number of bytes to be transferred. The initator will issue two (one if 8-bit transfer) ACKs for each DACK received; when the transfer counter decrements to one, DREQ will be deasserted, one additional ACK will be issued (not correlated to a DACK), and the end of transfer interrupt will be generated. The residual byte can be read by I/O. The DMA offset counter correctly reflects the offset between the number of ACKs generated and the number of bytes read from the FIFO by DMA. The offset counter is decremented when the final ACK is issued.

Option 2: The transfer counter can be programmed for the number of bytes to be transferred minus one, and a DMA command issued. A non-DMA command can be used for the last byte of the transfer.

Byte Control Mode

In Bus Configuration Mode Two, Byte Control Mode can be enabled by setting bit 5 of the Configuration 2 register. Byte Control mode allows the DMA controller to select the number of bytes placed on the data bus on each DMA transfer. This bus configuration uses multiplexed address and data on the PAD bus during microprocessor accesses. In this bus configuration, pin A3 functions as the Address Latch Enable (ALE) for the PAD bus, and pin A2 functions as the data bus read signal (DBRD/), which drives the DMA read data. Pins A1 and A0 have no effect unless

Byte Control Mode is enabled. When Byte Control Mode is enabled, an external controller uses BHE (A1) and SA0 (A0) to indicate whether the transfer consists of the low byte only, the high byte only, or both bytes together. The pin configuration options are illustrated in Chapter Three, *Signal Descriptions.*

Threshold Eight Mode

Threshold Eight mode causes the FSC to wait until eight bytes or more can be transferred before it requests service from the external DMA controller. Since the DMA bus can operate at speeds five to ten times greater than typical SCSI devices, this mode allows SCSI operations to effectively run in parallel with other processes.

The Threshold Eight bit in Config 3 changes the threshold to eight bytes for both 8-bit and 16-bit DMA operation. Refer to the description for the Configuration 3 register in Chapter 4, *Registers.* Threshold Eight mode is enabled by setting bit 0 in the Configuration 3 register and is valid in any bus configuration. Threshold Eight mode operates only during SCSI Data In or Data Out phase.

Note: When enabling this mode, the synchronous data offset can only be set to seven or less.

Threshold Eight mode causes DREQ to remain false until the FIFO can accommodate an eight-byte transfer. This improves DMA bus efficiency by keeping the chip off this bus until it can transfer at least eight bytes. With Threshold Eight enabled, the chip retains control of the DMA channel as long as one transfer can be accommodated. The transfer continues in normal mode whenever the Transfer Counter drops below eight bytes and the threshold drops to one transfer.

The following conditions must be true for a DMA Threshold Eight transfer to occur:

- Threshold Eight mode is enabled
- Transfer Counter indicates eight or more bytes
- The FIFO can accommodate an 8-byte transfer as follows:
  - FIFO contains at least eight bytes of data to transfer to memory, or
  - at least the top eight bytes of the FIFO are empty to receive the eight-byte transfer from memory.

If the Threshold Eight mode is enabled during DMA burst mode, the DMA burst is limited to a maximum of four transfers. This feature forces the chip to periodically relinquish control of the DMA channel, allowing other devices to gain access to the bus to perform such operations as memory refresh.

SCSI Input and Output Pins

The FSC SCSI data bus has a set of input pins and a set of output pins. This allows the FSC to be used in either single-ended mode or differential mode. In single-ended mode, the inputs are usually connected to the outputs on the circuit board. In differential mode, the SDI/ (SCSI Data Input) pins become bi-directional data pins, while the SDO/ (SCSI Data Output) pins become enable signals for external differential transceivers. Separate enables are required because, during arbitration, one data bus signal becomes an output while the other seven must be inputs. Two signals, TGS and IGS, control the direction of the external transceivers, allowing the FSC to dynamically switch between initiator and target roles.

Data Transfer Rate

Performance numbers for the FSC are based on single-ended connection to the SCSI bus with no external transceivers. In a differential system, external transceivers are required. This will slow asynchronous transmission by the propagation delay of the chosen transceiver, but will not slow synchronous transmission.

Asynchronous Operation

The asynchronous transmission rate will vary with cable length and the CLK period. The FSC can reach sustained transfer rates of 7 MB/s on short (one foot) cables using typical devices operating at or near nominal voltage and temperature. The typical transfer rate on a six meter cable is 4 MB/s using two typical FSCs talking to each other. The worst case asynchronous transmission rate, over voltage, temperature, and process variations is 3 MB/s on a maximum length (six feet), single-ended cable and 4 MB/s on a one foot cable.

The asynchronous transmission rate is only slightly affected by the CLK frequency when sending data. The FSC will drive the data bus for a minimum of one CLK period (plus any additional time required to meet the ANSI required 55 ns setup time) before asserting REQ or ACK. The CLK frequency does not affect the asynchronous transfer rate when receiving data. When the Enable Active Negation bit is set (Config 4 bit 2), the 53CF94/96 can transfer data asynchronously at up to 7 MB/s.

Synchronous Operation

The synchronous data transmission period is equal to the CLK input frequency multiplied by the encoded value in the Synchronous Transfer Period register. Sustained synchronous transfer rates of 10 MB/s are attainable across the commercial voltage and temperature range.

The 53CF94/96 can transfer synchronous SCSI data in both initiator and target modes at transfer rates up to 10 MB/s, using an input clock frequency of 40 MHz. The SCSI-1 and Fast SCSI-2 minimum timing requirements are listed below:

Mode	Setup	Hold	Assert/Negate
SCSI-1	55 ns	100 ns	90 ns
Single-ended Fast SCSI-2	25 ns	35ns	30 ns
Differential Fast SCSI-2	35 ns	45 ns	30 ns

To support maximum Fast SCSI transfer rates and SCSI-1 transfer requirements, the FASTSCSI (bit 4) and FASTCLK (bit 3) bits have been added to the Configuration 3 register. They modify the SCSI state machine to provide fast and normal synchronous timings depending upon the clock frequency. Full description of the operations of these bits and the required clock frequencies are provided in the Configuration 3 register description in Chapter 4, *Registers*.

During synchronous SCSI transfers, the assertion and deassertion of the REQ and ACK signals is programmable using the FASTCLK bit and other bits in the Synchronous Offset register. The input clock duty cycle affects the half clock assertion/deassertion delays. For more information, see the Synchronous Offset register description in Chapter 4, *Registers*.

Chip Reset

The FSC has the following three levels of reset: Hard, Soft, and Disconnect.

Hard Reset

A hard reset is executed at power up, when using the Reset Chip command, or when the RESET pin is asserted by external hardware. It stops all chip operations, resets all functions in the chip, and returns the chip to a disconnected state. The Reset Chip command remains at the top of the Command Register FIFO, which locks the chip and all registers in a reset state until a NOP command is issued.

Soft Reset

A soft reset is applied when the SCSI Bus reset condition is received through the RSTI/ pin, or when the Reset SCSI Bus command is issued, which asserts the RSTO/ pin. This condition resets the following subset of the functions reset by the hard reset:

- Resets DMA interface
- Resets bus-initiated selection/reselection module
- Resets command sequence module
- Resets Sequence Step and clears Sequencer Mode bits (Enable Select/Reselect = 0, Target = 0, Initiator = 0)
- Initializes Command register FIFO to empty
- Releases all SCSI signals except RSTO/
- Resets disconnect, initiator, and target command modules

The Reset SCSI Bus command will cause the RSTO/ signal to be asserted. When an external device on the bus responds, the RSTI/ signal will also be asserted. See Chapter 5, *Commands*, for further description of this command.

A SCSI Bus reset may occur in any mode. The RSTI/ signal is asserted by another SCSI device on the bus, and returns the chip to a disconnected state. The chip generates a SCSI Reset interrupt to the microprocessor if the interrupt is not disabled by bit 6 of the Configuration 1 register. If the SCSI bus reset is still active when the microprocessor clears the interrupt, a new interrupt is generated. This new interrupt must be serviced.

The Reset SCSI Bus command asserts the SCSI RSTO/ pin for approximately 25 µs and returns the chip to disconnected status. No interrupt is generated when the command is completed. However, since the RSTI/ pin is externally connected to the RSTO/ pin, a SCSI reset interrupt is generated if the interrupt is not disabled by Bit 6 of the Configuration 1 register.

Disconnect Reset

The disconnect reset is caused by various circumstances that result in the chip becoming disconnected from the SCSI bus, as described below:

- The Target Mode Disconnect, Disconnect Sequence, or Terminate Sequence command is issued to the chip.
- The chip is in initiator mode and the SCSI bus changes to the bus free state.
- The Select or Reselect command terminates with a selection timeout.

A disconnect reset resets the following subset of the functions reset by the Soft Reset:

- Sequencer Mode bits are cleared (target = 0 and initiator = 0).
- Initializes Command register FIFO to empty.
- Releases all SCSI signals except RSTO/
- Resets disconnect, initiator, and target command modules.

Chapter Three
Signal Descriptions

This chapter contains signal descriptions and pin diagrams for the 84-pin PLCC and 100-pin QFP packages. The signal descriptions are the same for the 53CF94 and 96. A slash (/) indicates an active low signal, B = bidirectional signal, I = input signal, and O = output signal. Figures 3-1 through 3-3 are the pin diagrams for each chip. Figure 3-4 is a functional signal grouping for the chip.

Table 3-1. Microprocessor and DMA Interface Pins

Pin No. 53CF94-2	Pin No. 53CF96-2	Signal	I/O	Description
63-66 68-71	90-93 96-99	PAD7-0	B	Bidirectional, active-high processor address-data bus with internal 400 µA pull-ups. When the mode pins are strapped for dual-bus operation, these pins allow the processor to access the internal registers of the chip at the same time the DMA bus is active. In multiplexed mode, address and data share this bus. In non-multiplexed mode, these pins are for data only. In single bus mode these pins are not used. Refer to Appendix B, *Bus Configurations*, for connection diagrams.
3-10 77-84	8-15 19-26	DB15-0	B	Bidirectional, active-high data bus with internal 400 µA pull-ups. When the mode pins are strapped for dual-bus operation, these pins are the 16-bit DMA data bus. In single bus mode, the processor accesses internal registers on the lower eight bits, while the DMA accesses the FIFO using all 16 bits. In Byte Control mode, BHE and SA0 allow DMA data to be transferred on the lower half, or the upper half, or the entire 16-bit DB bus.
11	27	DBP1	B	Odd parity for DB15-8
1	16	DBP0	B	Odd parity for DB7-0
59-60	84-85	A2-DBRD/, A3-ALE	I	In non-multiplexed mode, these TTL inputs are address bits 3 and 2. In multiplexed mode, they become ALE and DBRD/. The address on the PAD bus will be internally latched when ALE switches from high to low. DBRD/ is the read signal for the DB bus.

Table 3-1. Microprocessor and DMA Interface Pins, Continued

Pin No. 53CF94-2	Pin No. 53CF96-2	Signal	I/O	Description
57-58	82-83	A0-SA0, A1-BHE	I	In non-multiplexed mode, these pins are address inputs 1 and 0. In multiplexed mode with Byte Control, these pins are defined as BHE and SA0. Byte Control mode is available in Bus Configuration Mode Two only (Refer to the Host Bus Configuration section in Chapter 2, *Functional Description)* when bit 5 in the Config 2 register is set. These pins are not used in multiplexed non-byte control mode.
74	2	DBWR/	I	Active-low, DMA write signal which strobes DB15-0 data into the FIFO when DACK/ is true. In single bus mode, DBWR/ must be tied to WR/.
56	81	CS/	I	Active-low chip select. This TTL input enables eight-bit access to internal registers during read or write. CS/ uses the address inputs to access any register, includ ing the FIFO while DACK/ accesses only the FIFO. CS/ and DACK/ must never be active simultaneously in single bus mode, but may both be true in dual bus mode provided that CS/ is not accessing the FIFO.
55	80	RD/	I	Active-low register read signal. This TTL input allows internal registers to drive the data bus when either CS/ or DACK/ is also true. Refer to Appendix B, *Bus Configurations.*
54	79	WR/	I	Active-low register write signal. This TTL input causes the FSC to write data into its internal registers when CS/ is also true.

BHE	SA0	Bytes Transferred On
0	0	DB7-0 and DBP0
0	1	None
1	0	DB15-0 and DBP1 and DBP0
1	1	DB15-8 and DBP1

Table 3-1. Microprocessor and DMA Interface Pins, Continued

Pin No. 53CF94-2	Pin No. 53CF96-2	Signal	I/O	Description
52	76	INT/	O	Active-low, open-drain interrupt signal to the microprocessor. It is asserted on the rising edge of CLK. It may be cleared by reading the interrupt register, by a host hardware reset, or the Reset command (but not by a SCSI reset). This output cannot be masked by the user.
72	100	DREQ	O	Tri-state, active-high DMA request signal to the DMA controller. DREQ will remain true as long as the FIFO 1) contains at least one word (or one byte if 8-bit mode) to send to memory during DMA read, or 2) has room for one more word (or byte if 8-bit mode) during DMA write. If Threshold Eight mode is enabled, DREQ remains asserted as long as the FIFO can accommodate an 8-byte transfer.
73	1	DACK/	I	Active-low DMA acknowledge from the DMA controller. DACK/ accesses the FIFO only, while CS/ accesses any register including the FIFO. CS/ and DACK/ must never be true simultaneously in single bus mode.
53	77	RESET	I	Active-high chip reset. Reset must be asserted for at least two CLK periods after the voltage on the power pins has reached minimum V_{DD}.
61	86	CLK	I	Square wave clock input which generates internal chip timing. The maximum frequency is 40 MHz. The minimum frequency for asynchronous SCSI is 10 MHz. The minimum frequency for synchronous SCSI is 12 MHz. The synchronous transmission period is equal to the CLK period multiplied by the value in the synchronous transfer period register. The asynchronous transmission rate is indirectly affected by the CLK period. Refer to the *Data Transfer Rate* section of Chapter 2, *Functional Description.*

Table 3-2. SCSI Pins

Pin No. 53CF94-2	Pin No. 53CF96-2	Signal	I/O	Description
23-26 28-32	42-45 48-52	SDO7-0/, SDOP/	O	48 mA, open drain SCSI data/parity output bus. In single-ended mode (DIFFM/ not asserted) these pins are active-low SCSI data signals. In differential mode (DIFFM/ asserted) these outputs are used to control the direction of external differential transceivers, with high meaning output to the SCSI bus, low meaning input from the SCSI bus. These signals are totem pole outputs when Active Negation is enabled and the chip is active on the SCSI bus.
12-20	29-37	SDI7-0/, SDIP/	B	Schmitt trigger, active-low SCSI data/parity input bus. In single-ended mode (DIFFM/ not asserted) these inputs areSCSI data bus inputs. In differential mode, (DIFFM/ asserted) these pins are bidirectional data and parity signals for external tranceivers.
34-35, 43	56-57 66	SELO/, BSYO/, RSTO/	O	48 mA, open-drain SCSI outputs. In single-ended mode, these signals are active low. In differential mode, they are active high. The Reset SCSI Bus command will cause the FSC to drive RSTO/ true for 25-40 µs, depending on CLK frequency and clock conversion factor. Refer to the *Miscellaneous Commands* section in Chapter 5, *Command Set.*
36	58	REQO/	O	48 mA, open-drain, SCSI output. Asserted only in target mode. The signal becomes a totem pole output when Active Negation is enabled and the chip is active on the SCSI bus.
37	59	ACKO/	O	48 mA, open-drain, SCSI output. Driven by the FSC in initiator mode only. The signal becomes a totem pole output when Active Negation is enabled and the chip is active on the SCSI bus.

Table 3-2. SCSI Pins

Pin No. 53CF94-2	Pin No. 53CF96-2	Signal	I/O	Description
42	65	ATNIO/	B	48 mA, open-drain output, Schmitt trigger input. In initiator mode it is an output, and will be automatically asserted when the FSC detects an incoming parity error, or may be asserted by certain FSC commands. In target mode, this signal is an input.
39-41	62-64	MSGIO/, C/DIO, I/OIO	B	SCSI phase signals. They are 48 mA outputs in target mode, and Schmitt trigger inputs in initiator mode.
45-49	69-73	SELI/, BSYI/, REQI/ ACKI/ RSTI/	I	Schmitt trigger, active-low SCSI input signals.

Table 3-3. Transceiver Control Pins

Pin No. (53CF96-2)	Signal	I/O	Description
4	IGS	O	Active-high initiator group select. This output is high when the FSC is in initiator mode. It is used in differential mode to enable the initiator signals (ACKO/, and ATNIO/). When high, the FSC drives these signals.
6	TGS	O	Active-high target group select. This output is high whenever the FSC is in target mode. It is used in differential mode to enable the target signals (REQO/, MSGIO/, C/DIO, and I/OIO).

Table 3-4. Configuration Pins

Pin No. 53CF94-2	Pin No. 53CF96-2	Signal	I/O	Description
50-51	74-75	Mode 1, Mode 0	I	These TTL input pins configure the PAD bus, DB bus and the address/byte control bus (A3-ALE, A2-DBRD, A1-BHE,A0-SA0) as shown below. Refer to *Appendix B* for configuration diagrams.

Mode 1	Mode 0	Register Address	Register Data	Register Width	DMA Configuration
0	0	A3-A0	DB	8	Single bus, 8-bit processor, 8-bit DMA
0	1	A3-A0	DB	16	Single bus, 8-bit processor, 16-bit DMA
1	0	PAD 3-0	PAD	16	Dual bus, multi-plexed, byte control
1	1	A3-A0	PAD	8/16	Dual bus, 8-bit processor,16-bit DMA

-	87	DIFFM/		Differential mode enable. When this pin is high, the FSC operates in single-ended mode. When this pin is grounded, the FSC operates in differential mode, with bidirectional SCSI data on the SDI/ pins and active-high transceiver enables on the SDO/ pins.

Table 3-5. Power and Ground Pins

PLCC Pin Number	QFP Pin Number	Signal	Description
21, 62	38, 88	V_{DD}	+ 5 V power input
2, 22, 27, 33, 38, 44, 67 75*, 76*	5, 7, 17, 18, 40, 41, 46, 47, 54, 55, 60, 61, 67, 68, 94, 95	V_{SS}	Ground. NCR recommends a ground plane be used.

* *53CF94-2 only.*

Figure 3-1. NCR 53CF94-2 Pin Configuration

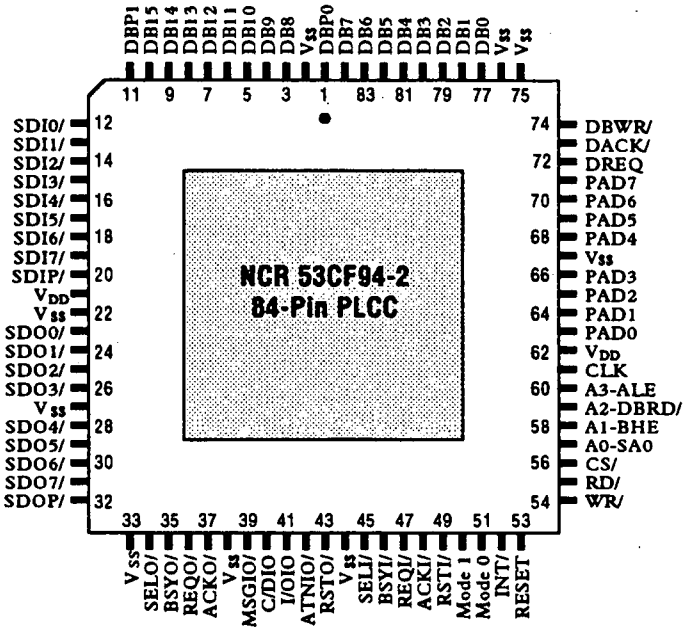


Figure 3-2. NCR 53CF96-2 Pin Configuration

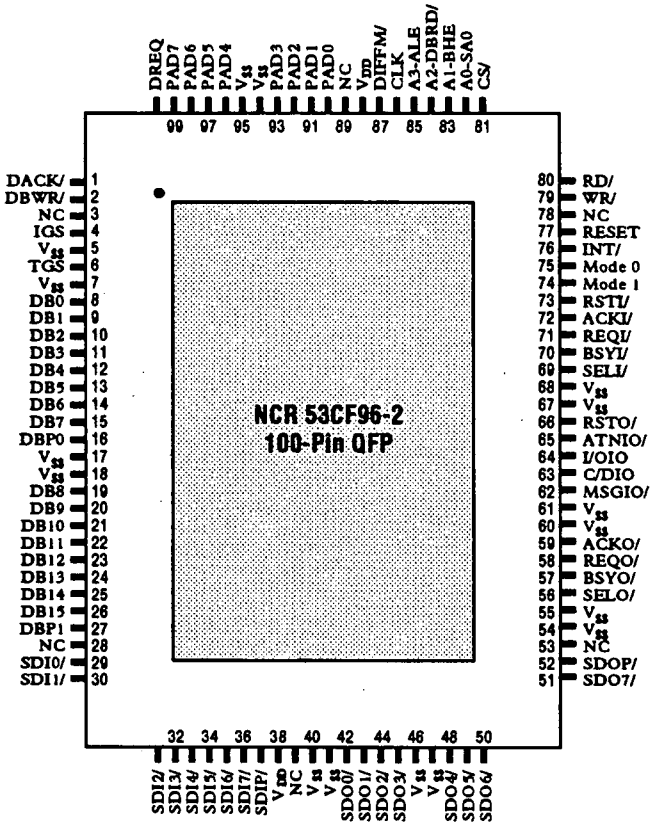
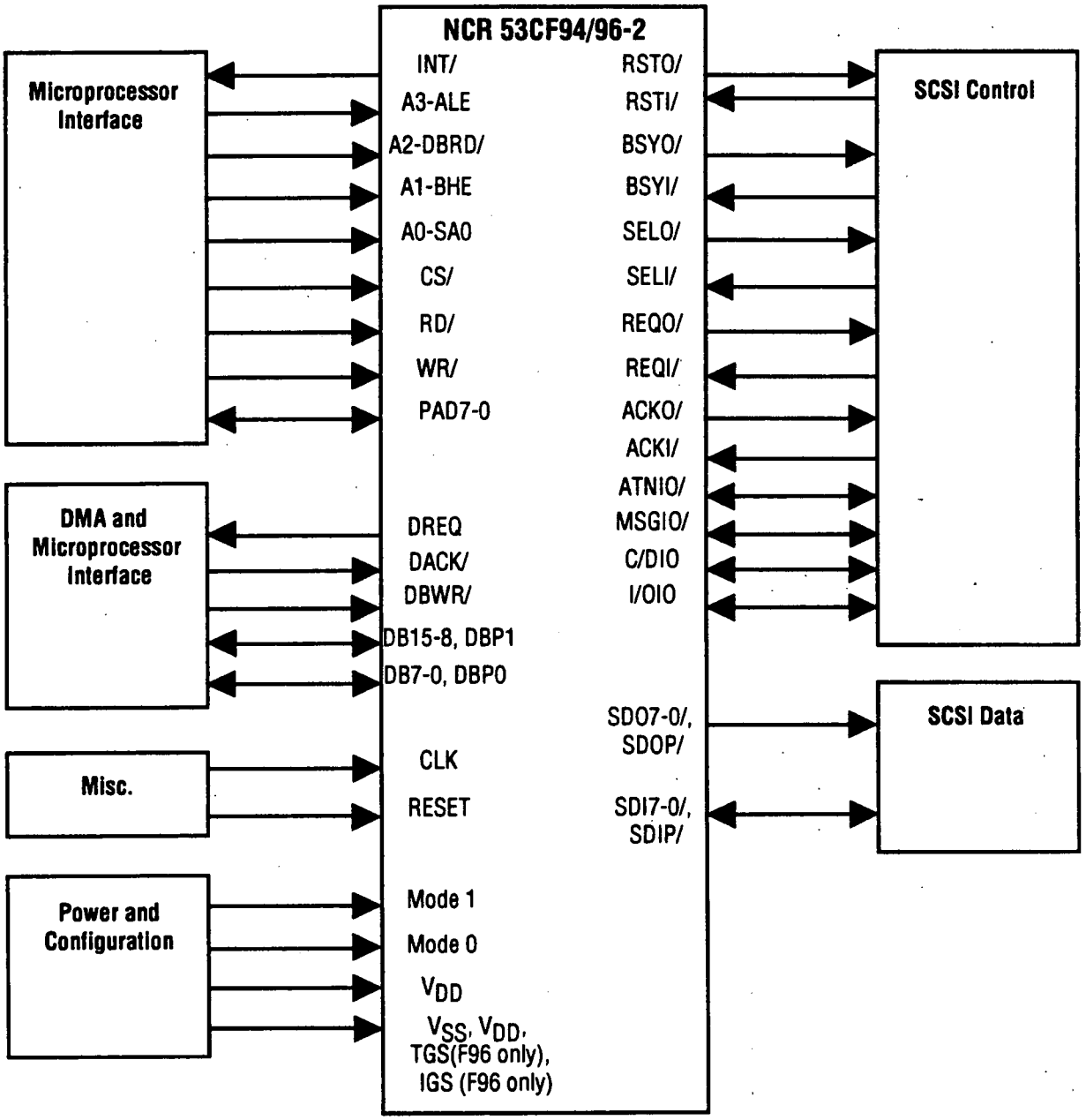


Figure 3-5. Functional Signal Grouping



Chapter Four
Registers

This chapter contains descriptions of all FSC registers. A register summary is provided in Appendix A, *Register Summary*. All register values are given in hexadecimal. The terms set and assert are used to refer to bits that are programmed to binary one. Similarly, the terms reset, clear or deassert are used to refer to bits that are programmed to binary zero. Some FSC registers have different meanings during reads than writes. When CS/ is true, the register being accessed is determined by either RD/ or WR/ together with the address pins A0-3. The FIFO may be accessed using either CS/ or DACK/ together with RD/ or WR/. Address pins A0-3 are ignored when DACK/ is active, but must be driven when CS/ is active. The FSC registers must not be read while they are in transition, especially the FIFO, FIFO Flags, and the Transfer Counter registers.

Reserved bits should always be set to zero and should be masked when read. All register bits in the 53CF94/96 are cleared to zero after a hard reset, except as noted below.

Register	Bit(s)	Reset Value
Transfer Count	All	Indeterminate
Transfer Counter	All	Indeterminate
Command	All	Indeterminate
Select/Reselect Bus ID	2-0	Indeterminate
Status	2-0	Indeterminate
Clock Conversion Factor	2-0	010
Synchronous Transfer Period	4-0	00101

Table 4-1. Register Set

Address (hex)	Read	Write
00	Transfer Counter Low	Transfer Count Low
01	Transfer Counter Mid	Transfer Count Mid
02	FIFO	FIFO
03	Command	Command
04	Status	Destination ID
05	Interrupt	Select/Reselect Time-out
06	Sequence step	Synchronous Transfer Period
07	FIFO Flags	Synchronous Offset
08	Configuration 1	Configuration 1
09	Reserved	Clock Conversion Factor
0A	Reserved	Test Mode
0B	Configuration 2	Configuration 2
0C	Configuration 3	Configuration 3
0D	Configuration 4	Configuration 4
0E	Transfer Counter High/ID	Transfer Count High
0F	Reserved	FIFO Bottom

Register 00, 01
Transfer Count
(Write Only)

These two registers, together with the Transfer Count High register (0Eh), form a 24-bit register which stores the Transfer Count value for DMA operations. They specify the number of bytes that are to be transferred over the SCSI bus. Values written to these two registers will be stored internally and loaded into the transfer counter by any DMA command. These values remain unchanged while the transfer counter decrements. Thus, successive blocks of equal size may be transferred without reprogramming the count. They may be reprogrammed any time after the previous DMA operation has started, whether it has finished or not. When the Features Enable bit is clear (which disables the Transfer Count High register), a zero value in registers 00 and 01 specifies a maximum length count of 64K. When the Features Enable bit is set, and the Transfer Count High register is enabled, zeros specify a maximum length count of 16 MB. These registers are not changed by any reset. Their states are unpredictable after power-up.

Register 00, 01
Transfer Counter
(Read Only)

Default>>>

X	X	X	X	X	X	X	X

These registers combine with the Transfer Counter High Register (0Eh) to form a 24-bit transfer counter. A read from these addresses will return the value currently in the counter. DMA commands use the counter to terminate a transfer. When the counter decrements to zero, the Terminal Count bit in the Status register will be set, indicating the current transfer is complete. Any DMA command will load the transfer count into the counter. A DMA NOP (80 hex) will load the counter while the non-DMA NOP (00) will not.

During SCSI Data phases, the transfer counter decrements on the leading edge of:

Target	**Decremented by**
Data In phase	DACK/
Data Out phase	REQO/
Initiator	**Decremented by**
Synchronous Data In	ACKO/
Asynchronous Data In	DACK/
Data Out	DACK/

Note that DACK/ can decrement the counter even if RD/ or WR/ do not go true. False DACK/s can cause the counter to get out of sync with the data stream, leading to subtle errors that are difficult to trace. When false DACK/s are expected to interfere with a temporarily suspended DMA operation, the DREQ Hi-Z bit in Config 2 should be set while the DMA is suspended.

The counter counts bytes. It decrements by one when transferring a single byte, or by two when transferring a word.

With two exceptions, non-DMA commands do not use the counter. During bus initiated selection and during the Target Receive Command sequence, the FSC decodes the group code field of the CDB (Command Descriptor Block), loads the counter with the number of bytes in the CDB, then decrements once for every byte received.

Register 02
FIFO Register
(Read/Write)

Default>>>

X	X	X	X	X	X	X	X

The FIFO is a 16 by 9-bit First-In-First-Out buffer between the SCSI bus and memory. Read Chapter 2, *Functional Description,* to understand its use during SCSI transactions.

The SCSI bus may transfer 8 or 9-bit bytes to the FIFO, depending on the parity control bit settings (refer to *Table 2-1*). The microprocessor may transfer 8 or 9-bit bytes to the FIFO using CS/ and RD/ or WR/, and the address bits. An external DMA controller may transfer 8 or 9-bit bytes or 16 or 18-bit words (depending on chip configuration, byte control inputs and the parity control bits – refer to *Tables 2-1, 3-1, and 3-4*) to the FIFO using DACK/ and RD/ or WR/. When accessed by CS/, the address bits must be valid. When accessed by DACK/, the address bits are ignored.

The bottom FIFO element and the FIFO flags are initialized to zero after hardware reset or the Chip Reset command and at the beginning of bus initiated selection or reselection. The contents of the rest of the FIFO are not changed by any reset but when the flags are zero, successive FIFO reads will access the bottom register. This register changes during any DMA or SCSI bus activity. The default value of this register is 00.

Register 03
Command Register
(Read/Write)

ENDMA				CMD			
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	X	X	X

The Command register is a two deep, 8-bit read/write register used to give commands to the FSC. Up to two commands may be stacked in the Command register. The second command may be written before the FSC completes (or even starts) the first. Reset Chip, Reset SCSI Bus, set Attention Immediate, and Target Stop DMA execute immediately (within four cycles of being loaded); all others wait for the previous command to complete. The last executed (or executing) command will remain in the Command register and may be read by the microprocessor. Reading the Command register has no effect on its contents. The internal sequencer maintains a working copy of the bottom of the command FIFO. The following conditions will cause the working copy to be cleared, so that the next command will fall through into the sequencer:

1) Hardware reset
2) Software reset
3) SCSI bus reset
4) SCSI bus disconnect
5) Bus initiated selection or reselection
6) Select command
7) Reconnect command if ATN is set
8) Select or Reselect time-out
9) Target Terminate command
10) Parity error detected in target mode
11) Assertion of ATN in target mode
12) Any phase change in initiator mode
13) Illegal command

Notes:

1) Non-DMA Send commands should not be stacked
2) Commands that transfer data in one direction should not be stacked with commands that transfer data in the opposite direction
3) After a hardware reset or Reset Chip command, a NOP is required to fill the Command register.

If two commands are placed in the command register, two interrupts may result. If the first interrupt is not serviced before the second finishes, the second interrupt is stacked behind the first. The first interrupt must be serviced before issuing a third command. When the Interrupt register is read by the host to service the first interrupt, the contents of the Status register, Sequence Step register, and Interrupt register will change to describe the second interrupt. When using stacked commands, the Features Enable bit (Config 2, bit 6) should be set to latch the SCSI phase bit in the Status register at the completion of each stacked command

Bit 7 Enable DMA

When bit 7 is set, the command is a DMA instruction. When it is not set, the command is a non-DMA instruction. DMA instructions will load the internal byte counter with the value in the transfer count register, without changing the count register. If the transfer terminates prematurely, the bits in the Status, Sequence Step, and Interrupt registers will indicate why.

Bits 6-0 Command Code

The FSC commands are shown in *Table 5-1*. Bits 6, 5 and 4 specify a mode group, as illustrated in the table below. Commands from the miscellaneous group may be issued at any time. Commands from the disconnected, target or initiator groups will only be accepted by the FSC if it is in the same mode as the command when it falls to the bottom of the command FIFO. Otherwise, an illegal command interrupt will be generated. For example, after a hardware or software reset, the

FSC will be in the disconnected state. A command from either the target group or the initiator group will cause an Illegal Command interrupt. An Enable Selection/Reselection command by itself will not change modes. However, if another SCSI device then selects the FSC, it will be in the target state; if another device reselects the FSC, it will then be in the initiator state. Similarly, any select command will place the FSC in Initiator mode, while the Reselect Sequence command will place the FSC in Target mode.

Bits 6, 5, 4	Command Mode
000	Miscellaneous
001	Initiator
010	Target
100	Disconnected State

Register 04
Status Register
(Read Only)

INT	GE	PE	TC	VGC	SCSI Phase		
7	6	5	4	3	2	1	0

Default>>

0	0	0	0	0	X	X	X

The status register contains important flags that indicate certain events have occurred. Bits 7-3 are latched until the interrupt register is read. The phase bits are not normally latched. They may be latched (for stacked commands) by setting Config 2, bit 6. The Default value of this register is 00.

Bit 7 Interrupt

This bit is set whenever the FSC drives the INT/ output true. It may be polled. It is buffered from the actual output so that in wired-OR (shared interrupt) designs, this bit will indicate whether the FSC is attempting to interrupt the microprocessor. Hardware reset, the Reset command, or a read from the Interrupt register will release an active INT/ signal and also clear this bit.

Bit 6 Gross Error

This bit is set when one of the following occurs:

1) The top of the FIFO is overwritten
2) The top of the Command register has been overwritten
3) Direction of DMA transfer is opposite to the direction of the SCSI transfer
4) An unexpected phase change in initiator role during Synchronous Data phase

These conditions do not cause an interrupt; a gross error may be detected only while servicing another interrupt. This bit is cleared by reading the interrupt register if the interrupt output is asserted. It will also be cleared by a hardware reset or the Reset command, but not SCSI reset.

Bit 5 Parity Error

This bit will be set if parity checking is enabled in the Config 1 register and the FSC detects a SCSI parity error on incoming command, data, status or message bytes. Detected parity errors will not cause an interrupt, they are merely reported along with other interrupt-causing events. If a parity error is detected during an initiator Information In phase, ATN is automatically asserted on the SCSI bus.

This bit will be cleared by reading the Interrupt register if the interrupt output is asserted. Hardware reset or the Reset Chip command will clear this bit, but not SCSI reset.

Bit 4 Terminal Count

This bit is set when the transfer counter decrements to zero. It is not set by loading a zero into the Transfer Counter register, but resets when the Transfer Count is loaded. Since a DMA NOP (80 hex) command will load the transfer counter, it will also clear this bit. A non-DMA NOP (00) will not load the counter and will not clear this bit. Reading the Interrupt register will not clear this bit. Hardware reset or the Reset Chip command will clear it, but SCSI reset will not.

Bit 3 Valid Group Code

When the FSC is selected, this bit decodes the group code field in the first byte of the CDB (Command Descriptor Block). If the group code matches one defined in ANSI X3.131-1986, this bit will be set. An undefined group code (designated reserved by the ANSI committee) leaves it not set. If the SCSI-2 bit is set in the Config 2 register, Group 2 commands will be recognized as ten-byte commands and this bit will be set. If the SCSI-2 bit is cleared, Group 2 commands will be treated as reserved commands. Groups 3 and 4 are always treated as reserved commands. A reserved group command will cause the FSC to request six command bytes. The FSC recognizes Group 6 as six-byte vendor unique commands and Group 7 as ten-byte vendor unique commands. The Valid Group Code bit will be cleared by reading the Interrupt register if the interrupt output is asserted. It will also be cleared by a hardware reset or the Reset Chip command, but not by a SCSI reset.

Bits 2-0 (Phase Bits)

These bits indicate the phase on the SCSI bus. They may be latched or unlatched, depending on Config 2, bit 6.

When not latched, they indicate the phase at the time the Status register was read. In keeping with the ANSI definition of the phase signals, these bits must be stable during any Status register read that follows an interrupt generated by the FSC.

The phase bits may be latched to permit stacking FSC commands. When the latch is enabled, the SCSI phase is latched upon command completion. These values are latched only if the Features Enable bit (bit 6) is set in the Configuration-2 register. The transparent latch is reopened when the Interrupt register is read.

Bit 2 1 0	SCSI Bus Phase
0 0 0	Data Out
0 0 1	Data In
0 1 0	Command
0 1 1	Status
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Message Out
1 1 1	Message In

Register 04
Destination ID
(Write Only)

Default>>>

X	X	X	X	X	0	0	0

The least significant three bits of this register specify the encoded destination bus ID for a selection or reselection command. These bits are binary encoded, with 000 0111 representing device ID 7 which appears as 80 (hex) on the SCSI bus. The most significant five bits are reserved. The destination ID is not changed by any reset; the states of these bits are unpredictable after power-up.

Register 05
Interrupt Register
(Read Only)

SRST	ILCMD	DIS	BS	FC	RESEL	SATN	SEL
7	6	5	4	3	2	1	0

Default>>>

0	0	0	0	0	0	0	0

This 8-bit register is used in conjunction with the Status register and Sequence Step register to determine the cause of an interrupt. Reading this register when the interrupt output is true will clear all three registers. The entire Interrupt register will be cleared (00) by a hardware reset or the Reset command, but not SCSI reset. The default value of this register is 00.

Note: Ths register should only be read when an interrupt is pending. The Sequence Step and Status registers should be read prior to reading this register.

Bit 7 SCSI Reset Detected

This bit is set if SCSI Reset Reporting is enabled in the Config 1 register and the chip detects a reset on the SCSI bus.

Bit 6 Illegal Command

This bit is set when a reserved code is placed in the Command register or when the command is from a mode group different than the mode the FSC is currently in. Refer to the *Command Register* definition. An interrupt is generated when this bit is set.

Bit 5 Disconnect

In initiator mode, this bit is set when the target disconnects or a Selection or Reselection timeout occurs. When the FSC is in target mode, this bit is set if a Terminate Sequence or Command Complete Sequence command causes the FSC to disconnect from the bus.

Bit 4 Bus Service
This bit indicates that another device is requesting service. In target mode, it is set whenever the initiator asserts ATN (Attention). In initiator mode, it is set whenever the target is requesting an Information Transfer phase.

Bit 3 Function Complete
This bit will be set after any target mode command has completed. In initiator mode, it is set after a target has been selected (before transferring any command phase bytes), after Command Complete finishes, or after a Transfer Information command when the target is requesting Message In phase.

Bit 2 Reselected
This bit is set during Reselection phase to indicate that the FSC has been reselected as an initiator.

Bit 1 Selected With ATN
This bit is set during Selection phase to indicate that the FSC has been selected as a target and that Attention (ATN) was asserted on the SCSI bus.

Bit 0 Selected
This bit is set during Selection phase to indicate that the FSC has been selected as a target and that ATN was false during selection.

Register 05
Time-Out
(Write Only)

This 8-bit, write-only register specifies the amount of time the FSC will wait for a response during selection or reselection. (The FSC has no way to time-out if it never wins arbitration, it will keep trying indefinitely until it wins.) The Time-Out register is normally loaded to specify a time-out period of 250 ms to comply with the ANSI standard. The register value (RV) may be calculated from:

$$\frac{\text{(time-out period) (CLK frequency)}}{\text{8192 (clock conversion factor)}}$$

For example, at 25 MHz, the register value that gives a 250 ms time-out period is 153 decimal or 99 hexadecimal. The clock conversion factor is defined in the description of write address 09. To compute the register value using the above formula when the clock conversion factor is zero, use 8, the number of clocks, rather than zero. The Time-Out register remains unchanged by any reset, and the states of these bits are unpredictable after power-up.

Register 06
Sequence Step
(Read Only)

Reserved				SOM	SS2	SS1	SS0
7	6	5	4	3	2	1	0
Default>>>							
X	1	0	0	0	0	0	0

The lower three bits of this register are used to indicate how far the internal sequencer was able to proceed in executing a sequenced command. This counter will be incremented at certain points in sequenced commands to aid in error recovery if the command does not complete normally.

Bits 7-4 Reserved

Bit 3 Synchronous Offset Max

When this bit is clear, the synchronous offset counter has reached its maximum value.

Bits 2-0 Sequence Step

The sequence step counter is set to zero at the beginning of certain commands. The counter is then incremented at specific points in the various algorithms to aid in error recovery. The possible states are described in *Chapter 5, Command Set.*

Register 06
Synchronous Transfer Period
(Write Only)

7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 4-0 of this register specify the minimum time between leading edges of successive REQ (Request) or ACK (Acknowledge) pulses. Synchronous data will be transmitted or received at the rate of one byte every "n" Clocks (CLK). The variable "n" is related to the register value and the data transfer rate as shown below.

40 MHz Clock (FASTCLK bit set)

FAST SCSI bit value	Register Value (h)	Clocks per byte	Transfer Rate MB/sec
1	4	4	10.0
1	5	5	8.0
1	6	6	6.6
1	7	7	5.7
X	8	8	5.0
0	9	9	4.4
0	A	10	4.0
0	B	11	3.6
0	C	12	3.3
0	D	13	3.0
0	E	14	2.8
0	F	15	2.6
0	10	16	2.5
0	11	17	2.3
0	12	18	2.2
0	13	19	2.1
0	14	20	2.0

25 MHz Clock (FASTCLK bit clear)

FAST SCSI bit value	Register Value (h)	Clocks per byte	Transfer Rate MB/sec
0	5	5	5.0
0	6	6	4.2
0	7	7	3.6
0	8	8	3.1
0	9	9	2.8
0	A	10	2.5
0	B	11	2.3
0	C	12	2.1
0	D	13	1.9

The upper three bits are reserved by NCR. This register defaults to 5 after hardware RESET or the Reset Chip command (but not SCSI reset). Refer to the descriptions for the FASTCLK and FASTSCSI bits (Config 3 bits 3 and 4) for information on Fast SCSI operation.

Note: Any combination not listed in the above tables violates ANSI standards, and should not be used.

Register 07
FIFO Flags
(Read Only)

SS2	SS1	SS0	FF4	FF3	FF2	FF1	FF0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

The least significant five bits of this register indicate how many bytes are currently in the FIFO. The value is binary encoded. The flags should not be polled while transferring data because they will not be stable while the SCSI interface is changing the contents of the FIFO.

The upper three bits are duplicates of the Sequence Step register bits in normal mode. If Test Mode is enabled, bit 5 is set to indicate that the offset counter is not zero. Not zero means that synchronous data may continue to be transferred. Zero means that the synchronous offset count has expired and the FSC will not transfer any more data until it receives an acknowledge.

Register 07
Synchronous Offset
(Write Only)

Bits 7-6 of this register control when the REQ and ACK signals deassert by selecting one of four input clock edges. These bits only affect a Synchronous Data In or Synchronous Data Out phase. The control over deassertion of these signals is measured in input clock cycles and is dependent on the status of the FASTCLK bit (Config 3 bit 3), as shown below.

FASTCLK Status	Synchronous Offset Register, bits 7-6	REQ/ACK Deassertion Delay (input clock cycles)
1	00	No Delay (Default)
1	01	1/2 clock
1	10	1 clock
1	11	1 1/2 clocks
0	00	No Delay
0	01	1/2 clock early
0	10	1 clock
0	11	1/2 clock

Bits 5 and 4 control when REQ or ACK asserts by selecting one of four input clock edges. Assertion of the REQ and ACK signals is not dependent on the FASTCLK bit. The assertion delay is shown below:

Synchronous Offset Register bits 5, 4	REQ/ACK Assertion Delay (in input clock cycles)
00	0 (Default)
01	1/2 clock
10	1 clock
11	1 1/2 clocks

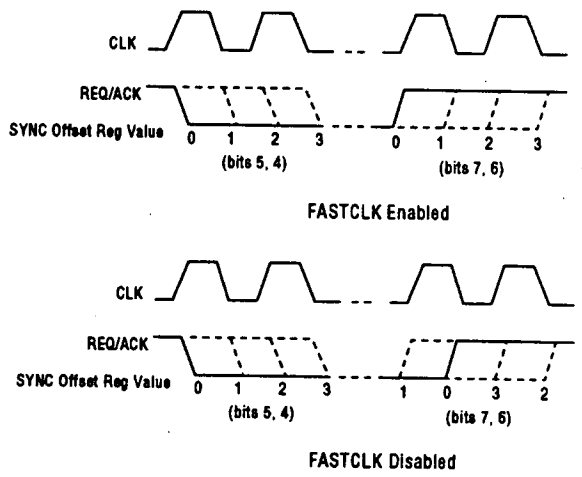
The least significant four bits of this register specify whether the FSC will transfer data phase bytes synchronously or asynchronously. *Zero specifies asynchronous transfer.* Any other value specifies the synchronous offset, the number of data phase bytes that may be sent synchronously without an acknowledge (either REQ or ACK), depending on whether the FSC is in initiator or target mode.

When transmitting to the SCSI bus, the FSC will stop sending bytes when it reaches this offset, and thereafter send one byte for every acknowledge it receives from the other SCSI device.

When receiving from the SCSI bus, the FSC will send an acknowledge every time a byte is removed from its FIFO on the DMA interface. The maximum offset of fifteen allows a receiving FSC to store data in its FIFO while the external DMA controller gains control of the memory bus. The maximum offset is 15 for non-burst mode operation, and seven for burst mode.

The synchronous offset is cleared (00) by hardware reset or a software Chip Reset, but not SCSI reset.

Figure 4-1. REQ/ACK Deassertion Delay



Note: The input clock duty cycle affects the half clock assertion/deassertion delays.

Register 08
Configuration 1 (Config 1)
(Read/Write)

Slow	SRD	PTest	PChk	CTEST	My Bus ID		
7	6	5	4	3	2	1	0
Default>>							
0	0	0	0	0	X	X	X

This 8-bit read/write register specifies various operating conditions for the FSC. Any bit pattern written to this register may be read back and should be identical. The default value of this register is 00.

Bit 7 Slow Cable Mode

Slow cable mode is needed when cabling conditions cause SCSI bus violations. It compensates for excessive capacitive loading on the SCSI data signals by inserting an extra CLK period between data being asserted on the bus and REQ or ACK being driven true. This bit is cleared (0) by hardware reset or the Reset command, but not SCSI reset.

Bit 6 SCSI Reset Reporting Interrupt Disable

This bit disables the reporting of a SCSI Reset. If the SCSI Reset signal goes true when this bit is set, the FSC will disconnect from the SCSI bus and remain idle in the disconnected state without interrupting the host. If the bit is not set the FSC will respond to the SCSI Reset by first interrupting the host. This bit is cleared by hardware reset or the Chip Reset command, but not SCSI reset.

Bit 5 Parity Test Mode

When bit 5 is set, the parity bit will equal bit 7 when unloading the FIFO to either the SCSI bus or the microprocessor bus. This allows parity errors to be created so that hardware and software may be tested. This bit must not be set during normal operation. Refer to *Parity Checking and Generation* in Chapter 2, *Functional Description*. This bit is cleared (0) by hardware reset or the Chip Reset command, but not SCSI reset.

Bit 4 Enable Parity Checking

When this bit is set, the FSC will check parity on incoming SCSI bytes during any information transfer phase except when receiving pad bytes. Detected parity errors will cause the Parity Error bit to be set in the Status register but will not cause an interrupt. In initiator role, bad parity will also set ATN (Attention) on the SCSI bus. When this bit is not set, parity will not be checked, the bit in the Status register will not be set, and ATN will not be asserted. Refer to *Parity Checking and Generation* in Chapter 2, *Functional Description*. This bit is cleared by hardware reset or the Reset command, but not by a SCSI reset.

Bit 3 Chip Test Mode Enable

When this bit is set, the chip is placed in a special test mode which enables the Test register at address 0A (hex). Once it has been set, the chip must be reset (hard or soft but not SCSI) before normal operation can begin. This bit should not be set during normal operation. This bit is cleared by hardware reset or the Reset command, but not SCSI reset.

Bit 2-0 My Bus ID

This bit field is the bus ID of this device. It is the ID to which the FSC responds during bus initiated selection or reselection, and the ID that the FSC uses to arbitrate for the bus. This three-bit field is binary encoded. It is not changed by any reset; after power-up the states of these bits are unpredictable.

Register 09
Clock Conversion
(Write Only)

Reserved					Clock Conversion Bits		
7	6	5	4	3	2	1	0
Default>>>							
?	?	?	?	?	?	?	?

This register must be set according to the CLK (Clock) input frequency. All timings longer than 400 ns depend on this register correctly agreeing with the CLK frequency. The clock conversion factor is equal to the binary encoded version of the least significant three bits. It should be set to one of the seven values below.

CLK Frequency (MHz)	Clock Conversion Factor
10	2
10.01 to 15	3
15.01 to 20	4
20.01 to 25	5
25.01 to 30	6
30.01 to 35	7
35.01 to 40	0

Note: a Clock Conversion factor of 0 indicates eight clocks.

These bits must never be loaded with a binary 1. Hardware reset or the Reset command will set the clock conversion register to 2. SCSI reset will not affect it. The upper five bits of this register are reserved.

Register 0A
Test Register
(Write Only)

		Reserved			Hi-z	I	T
7	6	5	4	3	2	1	0
Default>>>							
?	?	?	?	?	?	?	?

This register is enabled by setting the special test mode bit in Config 1 at address 08. After test mode has been entered, a hardware reset or the Reset command must occur before normal operation can begin. These bits must not be set during normal chip operation.

Bits 7-4 Reserved

Bit 3 Reserved (This bit must be set to 0)

Bit 2 All outputs to high impedance
When this bit is set, all bidirectional and all output pins go to high impedance and will not significantly load a TTL or compatible device.

Bit 1 Initiator Mode
When this bit is set, the FSC is artificially forced into initiator mode. Any initiator command will be accepted by the FSC. For example, a Set ATN command will cause ATN to be driven on the SCSI bus even if the FSC is disconnected.

Bit 0 Target Mode
When this bit is set, the FSC is artificially forced into target mode. Any target command will be accepted by the FSC. For example, a DMA command will load or unload the FIFO and set the SCSI phase, Data and REQ signals even if arbitration and selection have not occurred.

Register 0B
Configuration 2 Register (Config 2) (Read/Write)

RFB	FE	EBC	DHZ	SCSI2	BPA	RPE	DPE
7	6	5	4	3	2	1	0
Default>>>							
?	?	?	?	?	?	?	?

After hardware reset or the Reset command the bits in this register are all cleared, which makes the chip compatible with 53C90 software. Any bit pattern written to this register may be read back and should be identical. The default value of this register is 00.

Bit 7 Reserve FIFO byte

This bit allows 16-bit DMA reads to begin on misaligned word boundaries for initiator Synchronous Data In. It must be set before the phase changes to Synchronous Data In.

Synchronous Data In requires DMA to move data through the FIFO – the microprocessor must not access the FIFO. When this bit is set, a single byte is reserved in the bottom of the FIFO when the phase changes to Synchronous Data In. This reserved byte will become the low byte of the first 16-bit word that the FSC will transfer to memory using DMA, and the first byte received across the SCSI bus will become the high byte of the first word.

While servicing the interrupt for a phase change to Synchronous Data In on a misaligned boundary, the microprocessor should copy the byte at Address 0 from its own memory to FSC register 0F (hex), then issue the Transfer Information command. When the FSC writes its first word to memory (via DMA) it will overwrite the low byte (which is not part of the current SCSI data block) with the value placed in register 0F. Thus the low byte of the first word will be overwritten with a copy of itself, and the high byte will be the first byte received over the SCSI bus. The remaining bytes will be aligned on word boundaries and will be transferred 16 bits at a time.

This bit has no effect for phases other than initiator Synchronous Data In. The FSC can determine whether the transfer is synchronous or not by the value in the Synchronous Transfer register.

This bit is cleared by a hardware reset, the Reset command, or a write to register 0F (hex) after an interrupt for synchronous data. This bit is not affected by SCSI bus reset. The transfer count must be over-programmed by one (for the reserve byte) to use this feature.

Bit 6 Features Enable

This bit is cleared by hardware reset or the software Reset command, and is not affected by SCSI reset. When set, this bit enables all of the following features:

- The SCSI phase is latched at each command completion. This permits simpler software routines for stacked commands. When this bit is not set, the phase bits reported in the Status register are live indicators of the state of the SCSI phase lines.
- During differential mode operation when the SCSI phase changes from in to out, the SCSI Data In and Parity lines are delayed two or three CLKs before asserting. When the phase changes from out to in, the SCSI Data Out and Parity lines are delayed two or three CLKs before deasserting. At 40 MHz, this provides a minimum 50 ns turn-off time for the external transceivers. This will improve SCSI Data timings in differential mode by preventing electrical bus contention between the chip and the SCSI bus transceivers when the bus changes phase.
- The Transfer Counter High (0E) register is enabled, which will extend the transfer counter from 16 to 24 bits. If other conditions are met, setting this bit will also allow the chip revision code to be read (see the Transfer Counter High register description for more information on this feature).

Bit 5 Enable Byte Control

When the mode strapping pins are set to Bus Configuration Mode Two (mode 1 = 1 and mode 0 = 0) this bit will enable byte control on

the DMA interface. In Mode Two, the byte control inputs BHE and A0 instruct the FSC to transfer data on the low byte or the high byte, or both bytes of a 16-bit word. When this bit is not set, the byte control inputs are ignored. Hardware reset or the Reset command will leave this bit not set, while SCSI reset will not affect it.

Bit 4 DREQ High Impedance

When this bit is set, the DREQ output (DMA request) goes to high impedance and will not significantly load a TTL compatible device. This is useful when several devices share the DMA request line (known as wired-OR). When this bit is set, the FSC will ignore any activity on the DACK/ (DMA acknowledge) input.

When this bit is cleared, the DREQ output will be driven to TTL high or low voltages. When this bit is cleared, DACK/ is able to decrement the transfer counter and load or unload the FIFO, depending on WR/ or RD/. DACK/ should not pulse true without RD/ or WR/ because the transfer counter may decrement without transferring any data. Refer to the *Transfer Counter* register description.

Bit 3 SCSI-2

Setting this bit allows the FSC to support two new features adopted in SCSI-2: the 3-byte message exchange for Tagged-Queuing and Group 2 commands. These features can also be set independently in the Config 3 register.

Tagged-Queuing

When this bit is set and the FSC is selected with ATN (Attention), it will request either one or three message bytes depending on whether ATN remains true or goes false. If ATN is still true after the first byte has been received, the FSC may request two more message bytes before switching to Command phase. If ATN goes false, it will switch to Command phase after the first message byte. When the bit is not set it will request a single message byte (as a target) when selected with ATN, and abort the selection sequence (as an initiator) if the target does not switch to Command phase after one message byte has been transferred. Refer to *Bus Initiated Selection* in Chapter 2, *Functional Description.*

Group 2 Commands

When the SCSI-2 bit is set, Group 2 commands are recognized as 10-byte commands. Receiving a Group 2 command with this bit set will set the Valid Group Code bit in the status register. If the SCSI-2 bit is not set the FSC will treat Group 2 commands as reserved commands, it will request only six bytes in Command phase, and will not set the Valid Group Code status bit.

Bit 2 Target Bad Parity Abort

When this bit is set, the FSC will abort a Receive command or Receive Data Sequence command when the FSC detects a parity error.

Bit 1 Register Parity Enable

When this bit is set, parity from the host DBP pins will be loaded into the FIFO when CS/ and WR/ are both true. When this bit is not set the FSC generates parity from the host data bus, when CS/ and WR/ are both true, and places it in the FIFO along with the data from which it was generated.

When the FSC is moving data from the FIFO to the SCSI bus, it will flag outgoing parity errors only if the DMA Parity Enable bit is set.

Bit 0 DMA Parity Enable

When this bit is set, parity from the host DBP pins will be loaded into the FIFO when DACK/ and WR/ are both true. When this bit is not set, the FSC generates parity from the host data bus when DACK/ and WR/ are both true and places it in the FIFO along with the data from which it was generated.

When the FSC is moving data from the FIFO to the SCSI bus, it will flag outgoing parity errors only if the Register Parity Enable bit is set.

Register 0C
Configuration 3 Register (Config 3) (Read/Write)

IMRC	QTE	CDB10	FCLK	FSCSI	SRB	ADMA	T8
7	6	5	4	3	2	1	0

Default>>>

0 0 0 0 0 0 0 0

After a hardware reset or a software Chip Reset the bits in this register are all cleared, which makes the chip compatible with 53C90 software. Any bit pattern written to this register may be read back and should be identical.

Bit 7 ID Message Reserved Check

This bit allows a second level of checking for the validity of an ID message. The most significant bit of an ID Message byte is always checked, and must be one, or the chip interrupts. When this bit is set, bits 5-3 of the ID Message are also checked and must be zero, or the chip interrupts. This check occurs in two cases; if the chip is Selected with ATN true, or during Reselection. If the validation check fails, the Selection or Reselection sequence halts and the chip generates an interrupt.

Bit 6 Queue Tag Enable

When this bit is set, the 53CF94/96 can receive 3-byte messages during bus-initiated Select With ATN. This feature is also enabled by setting bit 3 in the Configuration 2 register. The message bytes consist of a one-byte identify message and a two-byte queue tag message. The middle byte is the tagged queue message itself and the last byte is the tag value (0 to 255). When this bit is set, the second byte is checked to see if it is a valid queue tagging message. If the value of the byte is not 20, 21, or 22h, the sequence halts and an interrupt is generated. When this bit is not set, the chip aborts the Select with ATN sequence after it receives one Identify Message byte, if ATN is still asserted.

Bit 5 (CDB10)

When this bit is set, 10-byte Group 2 commands are recognized as valid Command Descriptor Blocks (CDB). The Target command sequence receives ten Group 2 command bytes and sets the Valid Group Code bit (Status register, bit 3). When this bit is not set, the Target command sequence receives only six Group 2 command bytes and does not set the Valid Group Code bit. The group code defines how many bytes are in the CDB, and is used to determine how many bytes to request while driving Command Phase. This feature is also enabled or disabled by setting or clearing bit 3 in the Configuration 2 register.

Bit 4 (FASTSCSI)

Bit 3 (FASTCLK)

These bits are used to inform the device that it is connected to a fast clock, and to select between Fast SCSI timings and SCSI-1 timings. Fast SCSI operation requires a 40 MHz clock. A fast clock is one with a frequency greater than 25 MHz. These bits affect the SCSI transfer rate as follows:

Bit 4	Bit 3	Min clocks/byte asynch	Min clocks/byte synch	SyncTransfer (MB/s)
X	0	2	5	5
0	1	3	8	5
1	1	3	4	10

Bit 2 Save Residual Byte

The residual byte is the modulo 2 remainder at the end of a 16-bit DMA data stream. If Byte Control is used (hardware configured for Bus Configuration Mode Two and bit 5 set in Config 2), this feature should not be used.

When this bit is set, DREQ will not be asserted for the last residual byte at the end of a receive transfer, if such residue exists. The microprocessor should remove the residual byte from the FIFO. If this bit is not set and

the transfer ends with a single byte left over, DREQ will be asserted and a subsequent 16-bit DMA transfer will contain the last byte on the lower half of the bus.

The upper byte will be driven to all ones. This bit should not be used in 8-bit DMA mode or during any SCSI phase except Data In or Data Out (it is ignored in Data Out). It is left not set by hardware reset or the Chip Reset command, but is not affected by SCSI reset.

Bit 1 Alternate DMA Mode

This bit may be set only when the Threshold Eight bit (bit 0) in this register is set. All possible combinations for using bits 1 and 0 of this register are shown in the table below:

Bit 1	Bit 0	Function
0	0	Normal DMA mode
0	1	Threshold Eight Mode
1	0	Reserved
1	1	DMA Burst Mode

Setting this bit modifies the DMA interface to take advantage of the demand mode using an 8237A DMA controller when the Threshold Eight bit is also set. Refer to the description for *DMA Burst Mode* in Chapter 2, *Functional Description.* When DMA burst mode is enabled, all but the last DMA burst will be four words (or eight bytes if 8-bit DMA) long. The last burst may be one to four words (or one to eight bytes), depending on the modulo 8 remainder left in the transfer counter.

When this bit is set, DMA data is strobed into or out of the FSC during DMA reads and writes as described below:

•*DMA Write*

For multiple DMA writes per DREQ, DACK/ remains asserted while DBWR/ toggles for each write. The functionality of DACK/ and DREQ are unchanged for single DMA writes per DREQ.

•*DMA Read*

1) In Bus Configuration Modes Zero and One (Refer to *Host Bus Configuration* in Chapter 2) during multiple DMA transfers, DACK/ remains asserted while RD/ toggles for each DMA transfer. If the Alternate DMA bit is not set, the FSC outputs data when DACK/ is true, RD/ need not be true.

2) In Bus Configuration Mode Two during multiple DMA transfers, DACK/ remains asserted while DBRD/ toggles for each transfer. The FSC outputs data when both DACK/ and DBRD/ are true.

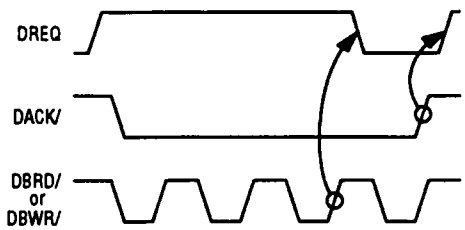
3) In Bus Configuration Mode Three, DACK/ must toggle for each DMA read. The FSC outputs data when DACK/ is true; RD/ need not be true.

If the burst consists of one transfer, DREQ will obey the non-burst timings. If the burst consists of two or more transfers, DREQ will obey the burst mode timings. If the FSC is operating as an initiator and a phase change occurs before the first DREQ has been acknowledged, DREQ will obey the non-burst timings. Otherwise, DREQ will obey the burst mode timings.

If less than eight bytes remain as a burst begins at the end of a transfer, the FSC will switch out of burst mode for the last one to seven bytes; these bytes are transferred in Normal DMA mode.

CAUTION: Burst Mode and Save Residual Byte Mode should not be used together in Initiator mode if back-to-back transfers are possible.

Figure 4-10. Alternate DMA Mode



Bit 0 Threshold Eight

Setting this bit causes the FSC to delay assertion of DREQ (DMA Request) until it can transfer eight bytes (four words). This higher threshold applies only to SCSI data phases. The threshold for all other phases is one byte for 8-bit DMA mode, or one word for 16-bit DMA mode. This bit must be set if using Alternate DMA mode.

When Threshold Eight is set, the maximum synchronous offset is limited to seven. DREQ will go true during DMA reads and writes as described below.

- *DMA Write to FIFO*
  DREQ is true whenever the top eight bytes of the FIFO are empty.
- *DMA Read from FIFO*
  1) End of transfer

  a) Target mode: DREQ is set when the transfer counter is zero or ATN is set.

  b) Initiator Synchronous Data In: DREQ is true when the transfer counter is less than eight.

  c) Initiator mode, not Synchronous Data In: DREQ is true when the transfer counter is zero, or after any phase change.

  2) Not end of transfer

  a) Initiator Synchronous Data In: DREQ is true if the transfer counter is greater than seven and the bottom eight bytes of the FIFO are full.

  b) Not Initiator Synchronous Data in: DREQ is true whenever the bottom eight bytes of the FIFO are full.

Register 0D
Configuration 4 (Config 4)
(Read/Write)

Reserved					EAN	8DMA	BBTE
7	6	5	4	3	2	1	0
Default>>							
0	0	0	0	0	0	0	

The undefined bits in this register are set to zero on reads and ignored on writes. This register is reset to zero on power-up or chip reset, but not on SCSI reset.

Bits 7-3 Reserved

Bit 2 Active Negation Enable

When enabled, the SCSI data, parity, REQ/, and ACK/ outputs actively drive to both high and low logic levels: refer to TolerANT information in chapter one. This bit should be set when transferring data at fast SCSI rates.

Bit 1 Transfer Counter Test Mode

When this bit is set, the transfer counter is split into three eight-bit segments. Each segment of the counter is decremented simultaneously whenever an event occurs that would decrement the transfer counter as a whole in normal mode. This bit should be used for testing purposes only.

Bit 0 Back-to Back Transfer Enable

When this bit is set, the 53CF94/96 can accept back-to-back transfers while in Initiator Synchronous Data In mode, whether odd or even aligned, giving the ability to support scatter-gather operations. Odd-aligned transfers are handled as follows (for a 512-byte block):

1. Load the transfer counter with a value of one and issue a Transfer Info command.
2. On the interrupt from the 53CF94/96 read one byte from the FIFO using programmed I/O and place into memory. This is the first byte of the odd-aligned bock

3. Load the transfer counter with a value of 511 and issue a Transfer Info command
4. On the interrupt from the 53CF94/96, read one byte from the FIFO using programmed I/O and place it into memory. This is the last byte of the odd-aligned block, and the transfer is now completed.

The recommended value of this bit is one. It may be cleared to maintain compatibility with earlier versions of the device.

Register 0E
Transfer Counter High/ID Register (Read/Write)

RES	Family ID				Rev Level		
7	6	5	4	3	2	1	0
Default>>>							
1	0	0	1	0	0	1	0

This register extends the Transfer Counter to 24 bits. Like the other transfer count registers, this register is not affected by any reset condition. This register is only enabled when the Features Enable bit is set. Refer to the descriptions for Registers 00 and 01 for additional information on the Transfer Counter.

Reading this register can also provide the chip revision code when the following conditions are met: 1) a hardware reset has occurred; and 2) the register has not been loaded with a transfer count. The following bit descriptions apply when the above conditions are met.

Bit 7 Reserved
This bit is currently set to one and should not be used.

Bits 6- 3 Chip Family ID
These bits identify the chip family, and are currently fixed at 0100.

Bits 2-0 Revision Level
These bits identify the current revision level of the chip, and are currently set to 010.

Register 0F
FIFO Bottom
(Write Only)

This register is used only during Initiator Synchronous Data In to align 16-bit DMA transfers to word boundaries. When Config 2, bit 7 is set and the phase changes to Initiator Synchronous Data In, the FSC reserves a byte in the bottom of the FIFO. If the microprocessor writes a byte to this register after the interrupt (for Synchronous Data In), the byte will become the low byte of the first word transferred out from the FIFO to the external DMA controller. The first byte received across the SCSI bus will become the high byte of the first 16-bit word transferred to memory.

Chapter 5
Command Set

All 53CF94/96 instructions may be issued in two forms: DMA and non-DMA. DMA commands move data between memory and the SCSI bus, while non-DMA commands move data between the FIFO and the SCSI bus. Non-DMA commands require the microprocessor to move data between the FIFO and memory. DMA commands require an external DMA controller to move data between the FIFO and memory. A command that is issued to the Command Register with bit 7 of the Command register set is a DMA command. A command that is issued with bit 7 not set is a non-DMA command. DMA commands will load the transfer counter with the value in the Transfer Counter register, so the Transfer Counter register must be loaded before any DMA command is issued. The word "sequence" in the command name is used to indicate that the Sequence Step register will be affected by executing the command. Check the Sequence Step register after using these commands to verify the command completed normally or to aid in data recover if the command did not complete normally.

Table 5-1. 53CF94/96 Command Set

Non-DMA	DMA	Command Register	Command	Interrupt
		7 6 5 4 3 2 1 0	**MISCELLANEOUS GROUP**	
00	80	X 0 0 0 0 0 0 0	NOP	no
01	-	0 0 0 0 0 0 0 1	Flush FIFO	no
02	-	0 0 0 0 0 0 1 0	Reset chip	no
03	-	0 0 0 0 0 0 1 1	Reset SCSI bus	yes*
			DISCONNECTED STATE GROUP	
40	C0	X 1 0 0 0 0 0 0	Reselect sequence	yes
41	C1	X 1 0 0 0 0 0 1	Select without ATN sequence	yes
42	C2	X 1 0 0 0 0 1 0	Select with ATN sequence	yes
43	C3	X 1 0 0 0 0 1 1	Select with ATN and stop sequence	yes
44	C4	X 1 0 0 0 1 0 0	Enable selection/reselection	no
45	-	0 1 0 0 0 1 0 1	Disable selection/reselection	yes
46	C6	X 1 0 0 0 1 1 0	Select with ATN3 sequence	yes
47	C7	X 1 0 0 0 1 1 1	Reselect3 sequence	yes

Table 5-1. 53CF94/96 Command Set (Continued)

Non-DMA	DMA	Command Register	Command	Interrupt
			INITIATOR GROUP	
10	90	X 0 0 1 0 0 0 0	Transfer information	yes
11	91	X 0 0 1 0 0 0 1	Initiator command complete sequence	yes
12	-	0 0 0 1 0 0 1 0	Message accepted	yes
18	98	X 0 0 1 1 0 0 0	Transfer pad	yes
1A	-	0 0 0 1 1 0 1 0	Set ATN	no
1B	-	0 0 0 1 1 0 1 1	Reset ATN	no
			TARGET GROUP	
20	A0	X 0 1 0 0 0 0 0	Send message	yes
21	A1	X 0 1 0 0 0 0 1	Send status	yes
22	A2	X 0 1 0 0 0 1 0	Send data	yes
23	A3	X 0 1 0 0 0 1 1	Disconnect sequence	yes
24	A4	X 0 1 0 0 1 0 0	Terminate sequence	yes
25	A5	X 0 1 0 0 1 0 1	Target command complete sequence	yes
27	-	0 0 1 0 0 1 1 1	Disconnect	no
28	A8	X 0 1 0 1 0 0 0	Receive message	yes
29	A9	X 0 1 0 1 0 0 1	Receive command	yes
2A	AA	X 0 1 0 1 0 1 0	Receive data	yes
2B	AB	X 0 1 0 1 0 1 1	Receive command sequence	yes
04	-	0 0 0 0 0 1 0 0	Target abort DMA	no**

* The command will cause an interrupt, if the SCSI Reset Reporting is not disabled in the Config-1 Register.

** The command itself does not cause an interrupt. However, it may allow a stalled command to finish and generate an interrupt.

Note: a dash (-) in the DMA column means that the transfer counter is loaded but no DMA operation occurs.

Illegal Commands

Writing an illegal command to the command register will cause an illegal command interrupt to be generated. An illegal command is any command outside of the specified mode commands or any unsupported command. An illegal command interrupt must be cleared prior to writing another command to the command register.

Stacked Commands

The Command register is a two-deep, eight-bit read/write register used to give commands to the FSC. If DMA commands are to be stacked, the transfer count must be loaded prior to loading the respective command. Command stacking should only be used during Data In and Data Out phase. If stacking is used in initiator mode, it is recommended that the Features Enable bit in Config 2 be set. This will cause the SCSI phase lines to be latched at the end of a command.

Miscellaneous Command Group

Miscellaneous commands can be executed and are valid in any mode.

Table 5-2. Miscellaneous Commands

DMA	Non-DMA	Mnemonic
80	00	No Operation (NOP)
-	01	Flush FIFO
-	02	Reset chip
-	03	Reset SCSI bus

NOP

No-Operation (NOP). The FSC requires this command only after hardware reset or the Reset Chip command to free the Command register. A DMA NOP (80 hex) may be used to load the transfer counter with the value in the Transfer Count register. No interrupt is generated from this command.

Flush FIFO

The flush FIFO command initializes the FIFO to the empty condition by resetting the FIFO flags and setting the bottom byte of the FIFO to zero.

Reset Chip

This command resets all functions in the chip and returns it to a disconnected state. The command has the same effect as a hardware reset, with the exception that Reset chip cannot change between single-ended mode or differential mode.

Reset SCSI Bus

This command will assert the RSTO/ (SCSI Reset Output) signal for T2 µs, where

T2 = 130 (CLK period) (CCF)

CCF = Clock Conversion Factor. Refer to the description of *Write Register 09* in Chapter 4. For CCF = 0, indicating 8 clocks, substitute 8 for 0 in this calculation. CLK is the clock input to the FSC. This command does not cause an interrupt; however, since RSTI/ may be externally connected to RSTO/ (in single-ended mode), an interrupt will be generated unless it is disabled in the Config 1 register.

Disconnected State Command Group

If any of the disconnected state commands are received by the FSC when it is not in the disconnected state, the command will be ignored, the command register will be cleared, and the FSC will generate an illegal command interrupt.

Table 5-3. Disconnected State Commands

DMA	Non-DMA	Mnemonic
C0	40	Reselect Sequence
C1	41	Select without ATN sequence
C2	42	Select with ATN sequence
C3	43	Select with ATN and stop sequence
C4	44	Enable selection and reselection
-	45	Disable selection and reselection
C6	46	Select with ATN3 sequence
C7	47	Reselect3 Sequence

Reselect Sequence

This command will cause the FSC target to arbitrate for the bus and then enter the Reselection phase when it wins arbitration. The Identify message, required by SCSI protocol, must either be placed in the FIFO by the microprocessor before issuing the command; or must be transferred by DMA, which involves setting the transfer count to one and setting up the external DMA controller. In either case, the Time-Out and Destination ID registers must have been programmed previously. The sequence will terminate early if a Reselect time-out occurs. If it terminates normally, a Function Complete interrupt will occur.

Select Without ATN Sequence

This command will cause the FSC initiator to arbitrate for the bus, enter the Selection phase when it wins, and send the CDB (Command Descriptor Block). The 6, 10 or 12-byte CDB must have either been placed in the FIFO previously by the microprocessor; or must be transferred by DMA, which involves setting the transfer count to 6, 10 or 12 and programming the external DMA controller. In either case, the Time-Out and Destination ID registers must have been programmed previously. This command terminates early if a reselection time-out occurs, the target does not assert Command phase or the target removes Command phase too early. If it terminates normally, a Function Complete and Bus Service interrupt will be generated.

Select with ATN Sequence

This command will cause the FSC initiator to arbitrate for the bus, select a device with ATN true, then send one message phase byte followed by 6, 10 or 12 Command phase bytes. The message and command bytes must have either been placed in the FIFO by the microprocessor or must be transferred by DMA, which involves setting the transfer count to 7, 11 or 13 and programming the external DMA controller. In either case, the Time-Out and Destination ID registers must have previously been programmed. This command terminates early if a select time-out occurs, the target does not assert Message Out phase followed by Command phase, or the target removes Command phase early. If it completes normally, a Function Complete and Bus Service interrupt will be generated.

Select with ATN and Stop Sequence

This command should be used in place of Select With ATN when multiple message phase bytes are to be sent (for example, a synchronous negotiation message). The command will select a target with ATN asserted, send one message phase byte that had previously been stored in the FIFO, generate a Bus Service interrupt and a Function Complete interrupt, and stop. After the interrupt, the FIFO may be filled with other message bytes. A Transfer Information command will then transfer bytes with ATN true until the FIFO empties. If a DMA Transfer Information command is used, ATN will remain true until the transfer counter decrements to zero.

Table 5-4. Target Selected without ATN Sequence

Sequence Step	Interrupt Register	Interpretation
210	76543210	
000	00000001	Selected, loaded bus ID into FIFO, loaded null-byte message into FIFO
001	00000001	Stopped in Command phase due to parity error; some command descriptor block bytes may not have been received; check FIFO flags
001	00010001	Same as above, initiator asserted ATN during Command phase
010	00000001	Selected, received entire command descriptor block; check Valid Group Code bit
010	00010001	Same as above, initiator asserted ATN during Command phase

Table 5-5. Target Selected with ATN Sequence (SCSI-2 Bit Not Set)

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped due either to parity error or invalid ID message
0 0 0	0 0 0 1 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped because ATN remained true after first message byte
0 0 1	0 0 0 0 0 0 1 0	Stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags
0 0 1	0 0 0 1 0 0 1 0	Stopped in Command phase; parity error and ATN true
0 1 0	0 0 0 0 0 0 1 0	Selection complete; received one message byte and the entire com mand descriptor block
0 1 0	0 0 0 1 0 0 1 0	Same as above, initiator asserted ATN during Command phase

Table 5-6. Target Selected with ATN Sequence (SCSI-2 Bit Set)

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN, stored bus ID and one message byte; stopped due to either parity error or invalid ID message
0 0 1	0 0 0 0 0 0 1 0	Initiator released ATN after one message byte received. Stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags
0 0 1	0 0 0 1 0 0 1 0	Initiator released ATN after one message byte received. Stopped in Command phase; parity error and ATN true
0 1 0	0 0 0 0 0 0 1 0	Initiator released ATN after one message byte received. Selection complete; received one message byte and the entire command de scriptor block
0 1 0	0 0 0 1 0 0 1 0	Same as above, initiator asserted ATN during Command phase
1 0 0	0 0 0 0 0 0 1 0	Parity error during second or third message byte
1 0 0	0 0 0 1 0 0 1 0	ATN remained true after third message byte
1 0 1	0 0 0 0 0 0 1 0	Received 3 message bytes then stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags
1 0 1	0 0 0 1 0 0 1 0	Stopped in Command phase; parity error and ATN true
1 1 0	0 0 0 0 0 0 1 0	Selection complete; received three message bytes and the entire command descriptor block

Table 5-7. Initiator Select without ATN Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected
0 1 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert command phase
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer because target prematurely changed phase
1 0 0	0 0 0 1 1 0 0 0	Select sequence complete

Table 5-8. Initiator Select with ATN Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN still asserted by FSC.
0 1 0	0 0 0 1 1 0 0 0	Arbitration, selection, and Message out complete; sent one message byte with ATN true, then released ATN; stopped because target did not assert Command phase after message byte was sent.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change; Some CDB bytes may not have been sent; check FIFO flags.
1 0 0	0 0 0 1 1 0 0 0	Selection With ATN Sequence complete. One message byte and all command bytes have been sent.

Table 5-9. Initiator Select with ATN and Stop Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN still asserted by FSC.
0 0 1	0 0 0 1 1 0 0 0	Message out complete; sent one message byte; ATN on.

Enable Selection/Reselection

After receiving this command, the FSC will respond to bus initiated selection or reselection. A command that causes the FSC to select or reselect will cancel this command. This command must be re-issued within 250 ms after the FSC disconnects to preserve ANSI recommended timings. If DMA is enabled, incoming information will be placed in memory. If DMA is not enabled, incoming information will remain in the FIFO.

Disable Selection/Reselection

This command disables an earlier Enable Selection/Reselection command. If bus initiated selection or reselection has not begun when this command is received by the FSC, it will generate a Function Complete interrupt. If bus initiated selection or reselection has begun, this command (and all other commands) will be ignored. Refer to *Bus Initiated Selection* and *Bus Initiated Reselection* in Chapter 2, *Functional Description.*

Once this command is loaded into the Command register, any bus-initiated selection or reselection that is already requested begins immediately. Since there is no delay in execution of the selection or reselection, the Function Complete Interrupt bit will not be set inadvertently if the selection or reselection sequence continues after this command has been loaded.

Select with ATN3 Sequence

This command is similar to the Select With ATN command, but sends three message bytes instead of one. It will cause the FSC initiator to arbitrate for the bus, select a device with ATN true, send three Message phase bytes, deassert ATN, then send 6, 10 or 12 command phase bytes. The message and command bytes must have either been placed in the FIFO by the microprocessor or must be transferred by DMA. This involves setting the transfer count to 9, 13 or 15 and programming the external DMA controller. In either case, the Time-Out and Destination ID registers must have previously been programmed. This command terminates early if a selection time-out occurs, the target does not assert Message Out phase followed by Command phase, or the target removes Command phase early. If it completes normally, a Function Complete and Bus Service interrupt will be generated.

Reselect3 Sequence

This command reselects an initiator and sends three message bytes: a one-byte Identify Message and a two-byte Queue Tag message. If DMA is not enabled, the three message bytes must be loaded into the FIFO before this command is issued.

Table 5-10. Initiator Select with ATN3 Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN still asserted by FSC.
0 1 0	0 0 0 1 1 0 0 0	Sent 1, 2 or 3 message bytes; stopped because target prematurely changed from Message Out phase or did not assert Command phase after third message byte; ATN released only if third message byte was sent.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change; some CDB bytes may not have been sent; check FIFO flags.
1 0 0	0 0 0 1 1 0 0 0	Selection With ATN3 Sequence complete. Three message bytes and all command bytes were sent.

Initiator Command Group

If the FSC is not in initiator state when it receives one of these commands, the command will be ignored, an Illegal Command interrupt will be generated and the Command register will be cleared. Refer to the description of the *Command Register* in Chapter 4, *Registers*.

If BSY goes false while the FSC is connected as an initiator, it will generate a disconnected interrupt. The interrupt output will occur 1.5 to 3.5 CLK cycles after BSY goes false.

When the FSC receives the last byte of a Message In phase, it will leave ACK (Acknowledge) asserted on the bus to prevent the target from sending any more bytes until the initiator decides to accept or reject the message. If the initiator accepts the command, it will issue a Message Accepted command. If the initiator does not accept the message, a Set ATN command should be issued before the Message Accepted command, causing the target to change to Message Out phase. For non-DMA commands, an empty FIFO means that the last byte has been sent. For DMA commands, the transfer counter signals the last byte.

If parity checking is enabled and the FSC detects a parity error while in Initiator mode, it will automatically assert ATN prior to deasserting ACK for the byte which has the error. The one exception is after a phase change to Synchronous Data In, and is described as follows.

If the Synchronous Offset register is non-zero (synchronous) and the phase changes to Data In, the DMA interface is immediately disabled and the reporting of a parity error during Data In phase is delayed. The phase change to Data In will: latch the FIFO flags to indicate how many bytes were in the FIFO (these bytes will be lost); clear the FIFO; load the FIFO with the first Data In byte; generate an interrupt; and continue to load the FIFO with incoming Data In bytes as long as the target sends them, but not more than the specified offset. To continue receiving Data In bytes, the microprocessor would normally issue the Transfer Information command to re-enable the DMA interface. If parity checking is enabled and a parity error occurred on a previous input phase (Message In or Status), then the parity error flag will be set in the Status register and ATN will be set on the SCSI bus. If a parity error occurred during the Data In phase, the parity bit will not be set nor will ATN be asserted until after the FSC receives the subsequent Transfer Information command.

Table 5-11. Initiator Commands

DMA	Non-DMA	Mnemonic
90	10	Transfer Information
91	11	Initiator Command Complete Sequence
-	12	Message Accepted
98	18	Transfer Pad
-	1A	Set ATN (Attention)
-	1B	Reset ATN

Transfer Information

This command can be used to send or receive any Information phase bytes, but is most often used for data transfer. **Note:** For synchronous transfer, DMA must be used. The FSC will continue to transfer information until one of the following terminating events occurs:

- Transfer is complete. Successful completion will generate a Bus Service interrupt. For a DMA Transfer Information, the transfer is complete when the transfer counter decrements to zero, the FIFO is empty and the target asserts REQ for the next byte. For non-DMA Transfer Information in which the FSC is sending bytes to the SCSI bus, the transfer is complete when the FIFO empties and the target asserts REQ for the next byte. For non-DMA Transfer Information in which the FSC is receiving bytes from the SCSI bus, transfer is complete after one byte is received and the target asserts REQ for the next byte. Thus non-DMA Transfer Information commands will generate an interrupt for every byte received.
- If the phase is Message Out, the FSC removes ATN prior to asserting ACK for the last byte of the message. For non-DMA, the FIFO flags indicate the last byte. For DMA, the transfer counter indicates the last byte.
- Target changes phase. The FSC clears the Command register and generates a Bus Service interrupt after the target asserts REQ for the next byte.
- Target releases BSY (Busy). The FSC generates a Disconnected interrupt.
- The FSC receives the last byte of a Message In phase. (For non-DMA every byte is assumed to be the last byte. For DMA, the transfer counter signals the last byte). The FSC leaves ACK asserted and generates a Function Complete interrupt.

  All Message In and Status phase transfers are handled one byte at a time. If DMA is enabled, the next byte will not be received until the current byte has been written to buffer memory and the FIFO is empty. If DMA is not enabled, each byte will create an interrupt.

Initiator Command Complete Sequence

This command will cause the FSC to receive a status byte followed by a message byte. It terminates early if the target does not assert Message In phase, or if the target disconnects. After receiving the message byte, the FSC leaves ACK asserted on the bus to allow the initiator to assert ATN if the message is unacceptable.

Message Accepted

This command deasserts the ACK signal on the SCSI bus. Any of the commands that receive bytes during message phase will leave ACK asserted after receiving the last message byte. To accept the message, issue this command. To reject the message, set ATN then issue this command.

Transfer Pad

Transfer Pad is usually an error recovery technique. It is useful when a target requests more bytes than an initiator has to send, or when an initiator must receive and discard a number of bytes from a target.

When transmitting to the SCSI bus, Transfer Pad will fill the FIFO with null bytes and send them to the SCSI bus. When receiving from the SCSI bus, Transfer Pad will receive bytes, place them on the top of the FIFO and discard them from the bottom of the FIFO.

When sending pad bytes to the SCSI bus, DMA must be enabled. No DMA requests are actually made, but the FSC uses the transfer counter to end the transfer.

The command terminates under the same conditions as the Transfer Information command, except that the FSC does not leave ACK asserted on the last byte of a Message In phase. If the command terminates before the transfer counter reaches zero (due to phase change or disconnect) the FIFO may contain pad bytes.

Set ATN

This command asserts attention on the SCSI bus. No interrupt is generated from this command. ATN stays asserted until the last byte of a message out phase. This command will not preempt a command in progress; attention will be asserted after the current command is completed.

DMA commands use the transfer counter to indicate the last byte. For non-DMA commands, the last byte means that the FIFO is empty. For DMA transfers, the last byte means that the transfer counter is zero. ATN will also be released if the target disconnects prematurely.

Reset ATN

This command causes ATN to be released. It does not cause an interrupt.

This command must not be used when connected to a device supporting the Common Command Set (CCS). The FSC obeys CCS protocol by releasing ATN on the last byte of a Message Out phase. The Reset ATN command is provided for older devices which do not respond properly to the ATN condition.

Target Command Group

If the FSC receives any of these commands when it is not in target state, it will ignore the command, clear the Command register, and generate an Illegal Command interrupt. Refer to the *Command Register* description in Chapter 4.

Normal completion of these commands will cause a Function Complete interrupt. If ATN is asserted, the Bus Service bit will be set in the Status register and an interrupt will be generated. If the FSC was idle when ATN was asserted, a Bus Service interrupt will be generated, the Function Complete bit will be zero, and the Command register will be cleared.

Table 5-12. Target Commands

DMA	Non-DMA	Mnemonic
A0	20	Send Message
A1	21	Send Status
A2	22	Send Data
A3	23	Disconnect Sequence
A4	24	Terminate Sequence
A5	25	Target Command Complete Sequence
-	27	Disconnect
A8	28	Receive Message
A9	29	Receive Command
AA	2A	Receive Data
AB	2B	Receive Command Sequence
-	04	Target Abort DMA

Send Message

This command will cause the FSC to assert Message In phase and send bytes until the FIFO is empty or the transfer counter is zero (if DMA).

Send Status

This command will cause the FSC to assert Status phase and send bytes until the FIFO is empty or the transfer counter is zero (if DMA).

Send Data

This command will cause the FSC to assert Data In phase and send bytes until the FIFO is empty or the transfer counter is zero (if DMA).

Disconnect Sequence

This command will cause the FSC to assert Message In phase, send two bytes, then disconnect from the SCSI bus. Normally, the first byte will be a Save Data Pointers message and the second will be a Disconnect message. These bytes must be loaded into the FIFO by the microprocessor, or may be loaded by DMA. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set and an interrupt will be generated, but the FSC will not disconnect.

Table 5-13. Target Disconnect Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 0 1 1 0 0 0	Sent one message byte; stopped because initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent two message bytes; stopped because initiator set ATN.
0 1 0	0 0 1 0 1 0 0 0	Disconnect Sequence complete; disconnected, bus is free.

Terminate Sequence

This command will cause the FSC to first assert Status phase, send one byte; then assert Message In phase, send one more byte, and disconnect. These bytes must be loaded into the FIFO by the microprocessor, or may be loaded by DMA. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set and an interrupt will be generated, but the FSC will not disconnect. If ATN is not asserted by the initiator, a disconnect interrupt is generated.

Target Command Complete Sequence

This command is similar to Terminate Sequence, but is used for linked commands. It will cause the FSC to first assert Status phase, send one byte, then assert Message In phase and send one more byte. The message byte will normally be a Command Complete message. If ATN is asserted by the initiator, the Bus Service and Function Complete bits will be set and an interrupt will be generated, but the FSC will not disconnect. If ATN is not asserted by the initiator, a function complete interrupt is generated.

Disconnect

This command causes the FSC to release all SCSI bus signals except RSTO (once triggered, RSTO is driven true for 25 µs or so, depending on CLK frequency and clock conversion factor). The FSC returns to the Disconnected state without generating an interrupt.

Receive Message

This command will cause the the FSC to assert Message Out phase and receive one byte, then generate a function complete interrupt.

Receive Command

This command will cause the FSC to assert Command phase and receive bytes from the initiator. For non-DMA Receive command, only one byte per interrupt may be received. DMA Receive Command will interrupt after the transfer counter decrements to zero. This command terminates by generating a function complete interrupt.

Table 5-14. Target Terminate Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 0 1 1 0 0 0	Sent one status byte; stopped because initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent status and message bytes; stopped because initiator set ATN.
0 1 0	0 0 1 0 1 0 0 0	Terminate Sequence complete; disconnected, bus is free.

Table 5-15. Target Command Complete Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 0	0 0 0 1 1 0 0 0	Sent one status byte; stopped because initiator set ATN.
0 0 1	0 0 0 1 1 0 0 0	Sent status and message bytes; stopped because initiator set ATN.
0 1 0	0 0 0 0 1 0 0 0	Command Complete Sequence complete.

Receive Data

This command will cause the FSC to assert Data Out phase and receive bytes from the initiator. For non-DMA Receive Data, only one byte per interrupt may be received. DMA Receive Data will interrupt after the transfer counter decrements to zero. This command terminates by generating a function complete interrupt.

Receive Command Sequence

This command will cause the FSC to assert Command phase and receive a number of bytes, which will vary according to the group code field of the first byte. If the SCSI-2 bit is set in the Config 2 register, Group 2 commands will be recognized as 10-byte commands. If the SCSI-2 bit is cleared, Group 2 commands will be recognized as reserved commands. Groups 3 and 4 are always reserved. The FSC will request six bytes for reserved commands, six bytes for Group 6 vendor unique commands, and 10 bytes for Group 7 vendor unique commands.

Table 5-16. Target Receive Command Sequence

Sequence Step	Interrupt Register	Interpretation
2 1 0	7 6 5 4 3 2 1 0	
0 0 1	0 0 0 0 1 0 0 0	Stopped during command transfer due to parity error; check FIFO flags.
0 0 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to parity error; ATN asserted by initiator.
0 1 0	0 0 0 0 1 0 0 0	Received entire command descriptor block.
0 1 0	0 0 0 1 1 0 0 0	Received entire CDB, initiator asserted ATN.

Target Abort DMA

The Target Abort DMA command allows the microprocessor to stop a target data transfer command whose progress has been halted due to inactivity on the DMA channel. One potential application is a system containing a microprocessor and an intelligent buffer controller that handles buffer management. The microprocessor sets up the buffer controller and over-programs the transfer counter prior to issuing a SCSI transfer command to the chip. When the buffer controller runs out of buffers, it interrupts the microprocessor. The microprocessor stops the chip and commands it to disconnect from the SCSI bus.

Note: The Target Abort DMA command should be used with extreme caution. Before using this command, verify that the removal of DREQ by this command does not confuse the system's DMA controller.

The abort DMA command executes from the top of the command FIFO. If there is a stacked command waiting to execute, it is overwritten and the Gross Error bit (Status Register 6) is set. The abort DMA command clears itself from the command stack after being decoded.

The abort DMA command can only be used when all of the following conditions are true:

1) Either the Target Send Data or Target Receive Data command is operating
2) The DMA controller has halted
3) The chip is in a steady state:

   Send Data - the DMA FIFO is empty

   Receive Asynchronous Data - The FIFO is full (FIFO Flags Register = 10h), or the Transfer Counter is zero (Status Register bit 4 = 1)

   Receive Synchronous Data - The Transfer Counter is zero, or the Offset Counter is at maximum value (Sequence Step Register bit 3 = 0)

When these conditions are true, the chip halts with DREQ asserted. If the chip is in Synchronous Transfer mode when halted, some ACK responses from the SCSI bus may not have been received and remain outstanding. Upon receiving the Abort DMA command, the chip resets the DMA interface, including the DREQ output pin, and terminates the command in progress. The chip completes any ongoing SCSI process. Send Asynchronous Data transfers complete immediately. Send Synchronous Data transfers complete when the offset counter is zero. Receive Asynchronous Data transfers complete immediately. Data left in the FIFO should be removed by the microprocessor. Receive Synchronous Data operations complete when all outstanding SCSI ACKs have been received. No extra bits are set in the Interrupt Status or Status registers. The microprocessor receives the interrupt from the command that was in progress, and the command FIFO is cleared.

Chapter 6
Electrical Characteristics

DC Electrical Characteristics

Absolute Maximum Stress Ratings

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Storage temperature	T_{STG}	-	-	-55	150	°C
Supply voltage	V_{DD}	-	-	-0.5	7.0	V
Input voltage	V_{IN}	-	-	V_{SS}- 0.5	V_{DD}+ 0.5	V
Latch-up current	I_{LU}	-	-2V < V_{PIN} < + 8V	± 100	-	mA
Electrostatic discharge	ESD**	all	Human body model 100 pF at 1.5K ohms	2000	-	V

* *Conditions that exceed the absolute maximum stress limits may destroy the device. Conditions that exceed the operating limits may cause the device to function incorrectly.*

***Tested according to MIL-STD-8836, Method 3015.7*

Operating Conditions

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Supply voltage	V_{DD}	-	-	4.75	5.25	V
Supply current	I_{DD}	-	Static*	-	1	mA
Supply current	I_{DD}	-	Dynamic	-	50	mA
Ambient temperature	T_A	-	-	0	70	°C
Thermal resistance, junction/ambient	Θ_{JA}					
84-pin PLCC				-	32	°C/V
100-pin QFP				-	65	°C/V
Rise Time	t_r	**	-	1	-	V/ns
Fall Time	t_f	**	-	1	-	V/ns

* *Static means: all inputs are deasserted, all outputs floating, and all bidirectional pins configured as inputs.*

** *These timings apply to all pins without Schmitt triggers.*

Inputs

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	-	2.0	V_{DD} + 0.5	V
Input low voltage	V_{IL}	-	-	V_{SS} –0.5	0.8	V
Input leakage current	I_{IN}	Non-SCSI	$0 < V_{IN} < V_{DD}$	–10	10	µA
Hysteresis	V_H	SCSI	-	300	400	mV
Input leakage current	I_{IL}	SCSI	$0 < V_{IN} < V_{DD}$	–10	10	µA
Capacitance	C_{IN}		-	-	10	pF

Outputs

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Output high voltage	V_{OH}	DREQ, IGS, TGS	I_{OH}= –2 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	DREQ, IGS, TGS, INT/	I_{OL}= 4 mA	V_{SS}	0.4	V
Output low voltage*	V_{OL}	RSTO/, SELO, ACKO/, REQO/, SDOP/, BSYO/, SDO7-0	I_{OL}= 48 mA	V_{SS}	0.5	V
Hi Z state leakage	I_{OZ}	-	$0 < V_{OUT} < V_{DD}$	–10	10	µA
Fall Time	T_F	SCSI pins	SCSI termination	5.2	14.7	ns
Capacitance	C_{OUT}	-	-	-	10	pF

* TolerANT Active Negation not enabled

Bidirectional Pins

Parameter	Symbol	Pins	Test Conditions	Min	Max	Unit
Input high voltage	V_{IH}	-	-	2.0	V_{DD}+ 0.5	V
Input low voltage	V_{IL}	-	-	V_{SS}–0.5	0.8	V
Output high voltage*	V_{OH}	SCSI inputs	I_{OH}= –2 mA	2.4	V_{DD}	V
Output low voltage	V_{OL}	SCSI inputs	I_{OL}= 4 mA	V_{SS}	0.4	V
Output low voltage*	V_{OL}	SDO7-0, SDOP, REQO/, ACKO/	I_{OL}= 48 mA	V_{SS}	0.5	V
Hysteresis	V_H	SCSI	-	300	400	mV
Input leakage	I_I	SCSI	$0 < V_{IN} < V_{DD}$	–10	10	µA
Input current, low	I_{IL}	DB15-0, DBP1-0, PAD7-0	V_{IN}= 0	–400	-100	µA
Input current, high	I_{IH}	DB15-0, DBP1-0, PAD7-0	V_{IN}= V_{DD}	0	10	µA
Hi Z pull-up current	I_{PU}	DB15-0, DBP1-0, PAD7-0	V_{IN}= 0	-400	-100	µA
Capacitance	C_{IO}		-	-	10	pF

* TolerANT Active Negation not enabled

NCR TolerANT Active Negation Technology Electrical Characteristics[1]

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{OH}	Output high voltage	I_{OH} = 3.2 mA	2.5	3.1	3.5	V
V_{OL}	Output low voltage	I_{OL} = 48 mA	0.1	0.2	0.5	V
I_{OH} [1]	Output high current	V_{OH} = 2.5 Volts	2.5	15	24	mA
I_{OL}	Output low current	V_{OL} = 0.5 Volts	100	150	200	mA
I_{OSH} [1]	Short-circuit output high current	Output driving low, pin shorted to V_{DD} supply[2]			625	mA
I_{OSL}	Short-circuit output current, low	Output driving high, pin shorted to V_{SS} supply			95	mA
dV_H/dt	Slew rate, low to high	Figure 6-24	0.15	0.23	0.49	V/ns
dV_L/dt	Slew rate, high to low	Figure 6-24	0.19	0.37	0.67	V/ns

Note: *These values are guaranteed by periodic characterization. SCSI RESET pin has 10kΩ (nominal) pull-up resistor*

[1] Active Negation outputs only: Data, Parity, REQ, ACK

[2] Single pin only; irreversible damage may occur if sustained

Figure 6-24. Rise and Fall Time Test Conditions

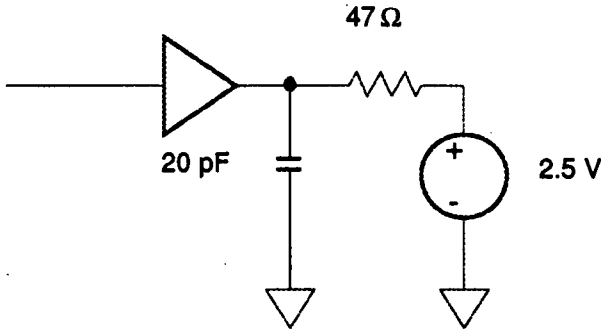


Figure 6-25. SCSI Input Filtering

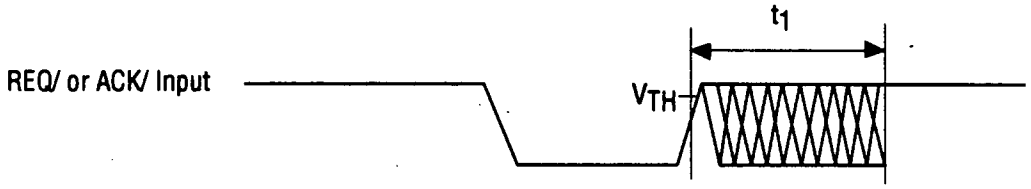


Figure 6-26. Hysteresis of SCSI Receiver

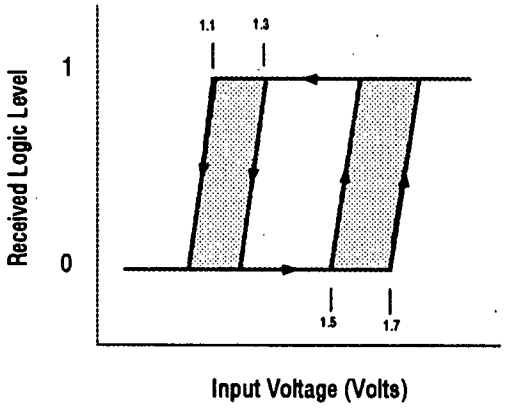


Figure 6-27. Input Current as a Function of Input Voltage

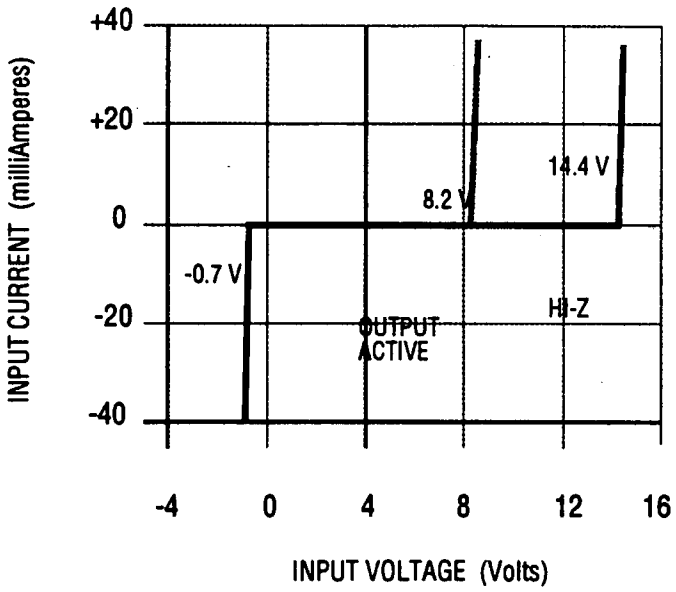
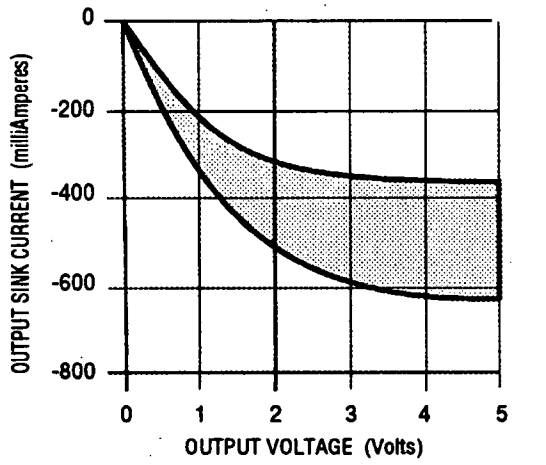
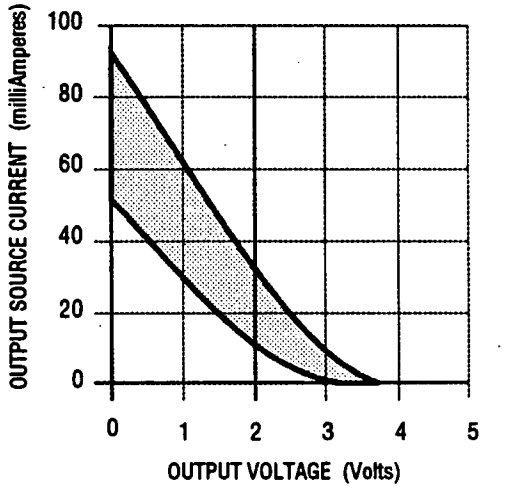


Figure 6-28. Output Current as a Function of Output Voltage



Output Sink Current as a Function of Output Voltage (I_{OL})



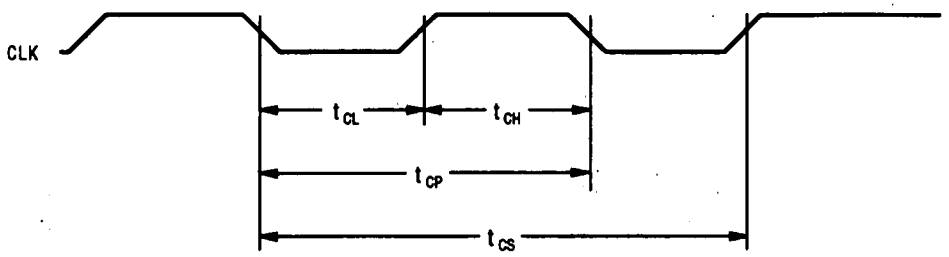
Output Source as a Function of Output Voltage (I_{OH})

AC Electrical Characteristics

The AC characteristics described in this section apply over the operating voltage and temperature range, 4.75 V≥ V_{DD}≥ 5.25 V and 0°C ≥T_A≥ 70°C. Output timing is based on simulation under worst case conditions (4.75 V, 70°C) and worst case processing using the following termination. All timings in this specification are taken from the 10% and 90% points with respect to the specified V_{OL} and V_{OH} of the waveforms.

Pin	Termination
DREQ, TGS, IGS, SDIP/, SDI7/-O/, PAD7-0	50 pF
INT/	50 pF,2.2K pull-up
DB15-0, DBP0, DBP1	80 pF
SDOP/, SDO7/-0/, RSTO/, SELO/, BSYO/, ATNIO/, MSGIO/, C/DIO, I/OIO, REQO/, ACKO/	200 pF, 110 pullup, 165 pulldown

Figure 6-1. Clock Input



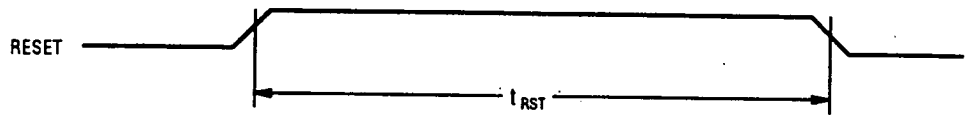
Parameter (FASTCLK bit cleared)	Symbol	Min	Max	Units	Notes
Clock frequency, asynchronous SCSI	t_{CPA}	10	25	MHz	2
Clock frequency, synchronous SCSI	t_{CPS}	12	25	MHz	2
Clock high time	t_{CH}	14.58	-	ns	1
Clock low time	t_{CL}	14.58	-	ns	1
Clock period	t_{CP}	40	100	ns	-
Synchronization latency = $t_{CP} + t_{CL}$	t_{CS}	t_{CP}	$t_{CL} + t_{CP}$	-	-

Parameter (FASTCLK bit set)	Symbol	Min	Max	Units	Notes
Clock frequency, asynchronous SCSI	t_{CPA}	20	40	MHz	2
Clock frequency, synchronous SCSI	t_{CPS}	20	40	MHz	2
Clock high time	t_{CH}	0.4	0.6	ns	-
Clock low time	t_{CL}	0.4	0.6	ns	-
Clock period	t_{CP}	25	50	ns	-
Synchronization latency = $t_{CP} + t_{CL}$	t_{CS}	t_{CP}	$2 * t_{CP}$	-	-

1) *For synchronous SCSI data transmission, CLK must also meet the following:* $2t_{CP} + t_{CL} \geq 97.92$ *ns and* $2t_{CP} + t_{CH} \geq 97.92$ *ns*

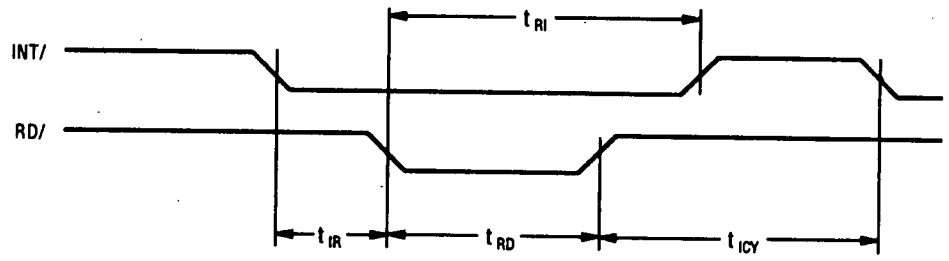
2) *Minimum frequencies to meet ANSI timing specifications.*

Figure 6-2. Reset Input



Parameter	Symbol	Min	Max	Units	Notes
RESET pulse width	t_{RST}	500	-	ns	-

Figure 6-3. Interrupt Output



Parameter	Symbol	Min	Max	Units	Notes
INT/ low to Interrupt register read	t_{IR}	0	-	ns	2
RD/ pulse width	t_{RD}	50	-	ns	1
RD/ low to INT/ high	t_{RI}	0	100	ns	-
RD/ high to INT/ low	t_{ICY}	t_{CS}	-	ns	-

1) *Refer to the register read specifications for the timing requirements of CS/, RD/, and address for reading the Interrupt register.*

2) *The Interrupt register should not be read when INT/ is false.*

Register Interface, DB and Nonmultiplexed PAD Bus

Parameter	Symbol	Min	Max	Units	Notes
Address setup to CS/ low	t_1	0	-	ns	1
Address hold from CS/ low	t_2	30	-	ns	-
CS/ high to CS/ low	t_3	30	-	ns	-
CS/ low to read data valid	t_4	-	65	ns	3
CS/ setup to RD/ low	t_5	0	-	ns	4, 7
RD/ pulse width	t_6	30	-	ns	-
RD/ high to CS/ high	t_7	0	-	ns	4
RD/ low to data valid	t_8	-	30	ns	5
RD/high to data bus disable	t_9	2	30	ns	-
CS/ setup to WR/ low	t_{10}	0	-	ns	6, 7
WR/ pulse width	t_{11}	30	-	ns	-
WR/ high to CS/ high	t_{12}	0	-	ns	6
Data setup to WR/ high	t_{13}	15	-	ns	-
Data hold after WR/ high	t_{14}	0	-	ns	-
WR/ high to CS/ low	t_{15}	30	-	ns	-
WR/ high to WR/ low	t_{16}	40	-	ns	-

1) *CS/ must make a high to low transition to latch a new register address.*

2) *For single bus mode (mode zero or mode one) DACK/ must be inactive during all register accesses. WR/ must be tied to DBWR.*

3) *t_8 must also be satisfied.*

4) *If RD/ is held low, the time from CS/ low to stable data is t_4 and the output disable time from CS/ high is t_9.*

5) *t_4 must also be satisfied.*

6) *If WR/ is held low, the data setup to CS/ high is 10ns minimum; data hold from CS/ high is 30 ns minimum; t_3 is 60 ns minimum.*

7) *If DMA is active, the FIFO must not be accessed.*

Figure 6-4. RegisterRead, DB and Nonmultiplexed PAD Bus

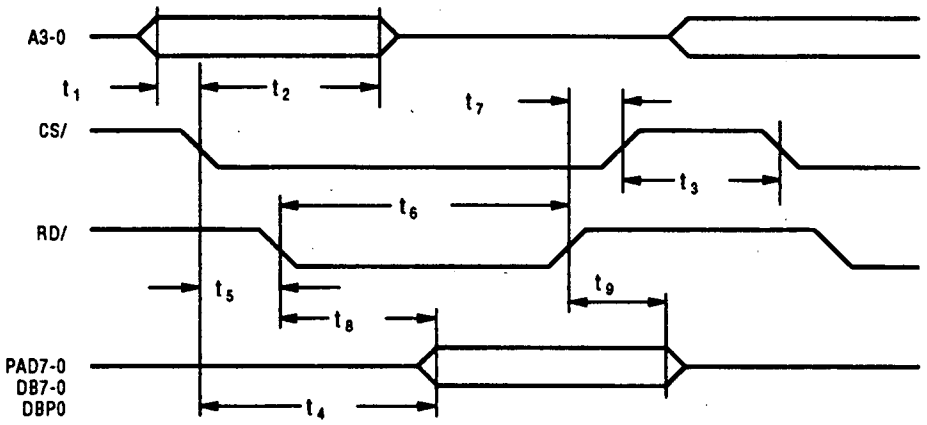
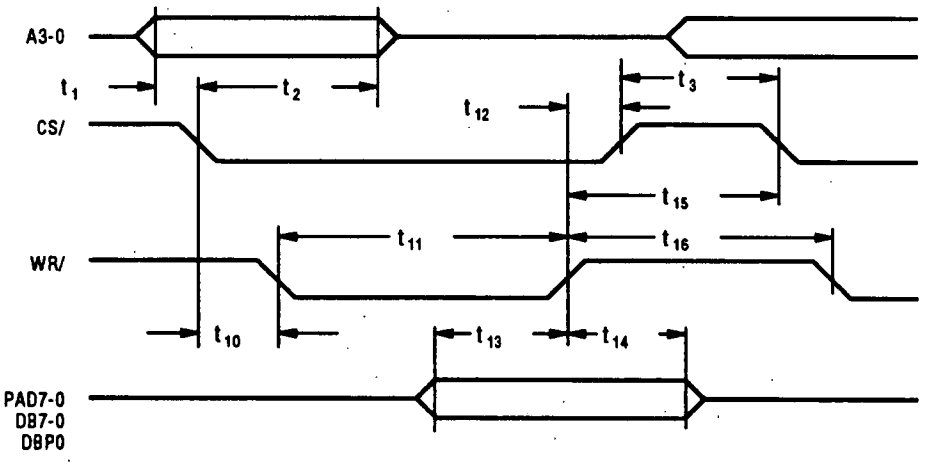


Figure 6-5. Register Write, DB and Nonmultiplexed PAD Bus



Register Interface, Multiplexed PAD Bus

Parameter	Symbol	Min	Max	Units	Notes
Address setup to ALE low	t_1	10	-	ns	-
Address hold from ALE low	t_2	10	-	ns	-
ALE pulse width	t_3	20	-	ns	-
ALE low CS/ low	t_4	10	-	ns	-
CS/ low to data	t_5	-	65	ns	3
CS/ high to ALE high	t_6	50	-	ns	-
CS/ setup to RD/ low	t_7	0	-	ns	1, 4
RD/ pulse width	t_8	30	-	ns	-
RD/ high to CS/ high	t_9	0	-	ns	4
RD/ low to data valid	t_{10}	-	30	ns	5
RD/high to data bus disable	t_{11}	2	30	ns	-
CS/ setup to WR/ low	t_{12}	0	-	ns	1, 6
WR/ pulse width	t_{13}	30	-	ns	-
WR/ high to CS/ high	t_{14}	0	-	ns	6
Data setup to WR/ high	t_{15}	15	-	ns	-
Data hold from WR/ high	t_{16}	0	-	ns	-
WR/ high to ALE high	t_{17}	50	-	ns	-

1) If DMA is active, the FIFO register must not be accessed.

2) ALE must pulse to capture a new register address.

3) t_{10} must also be satisfied.

4) If RD/ is held low, the time from CS/ low to stable data is t_5 and the data release time from CS/ high is t_{11}.

5) t_5 must also be satisfied.

6) If WR/ is held low, data setup to CS/ high is 10 ns and data hold from CS/ high is 30 ns minimum.

Figure 6-6. Register Read, Multiplexed PAD Bus

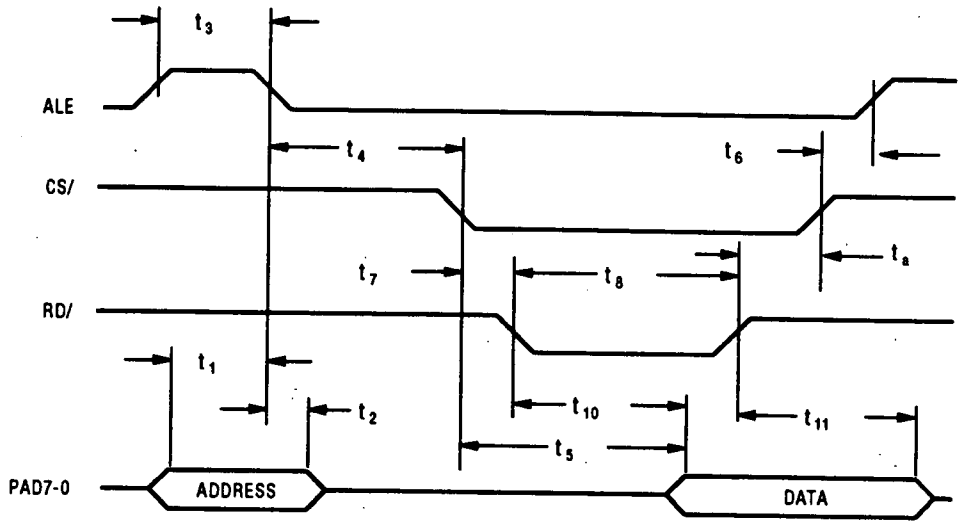
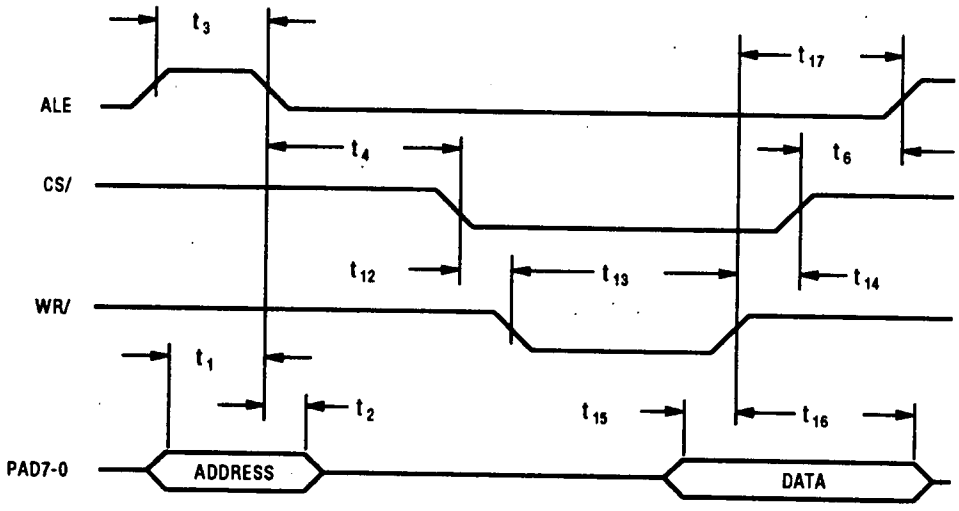


Figure 6-7. Register Write, Multiplexed PAD Bus



DMA Interface Without Byte Control (Configuration Modes 0, 1, and 3 only)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ low to DREQ low	t_1	-	30	ns	5
DACK/ high to DREQ high	t_2	-	30	ns	-
DACK/ high to DACK/ low	t_3	12	-	ns	4
DACK/ pulse width	t_4	40	-	ns	-
DACK/ period (low to low)	t_5	95	-	ns	-
DACK/ period (high to high)	t_6	t_{CS} + 25	-	ns	6
DACK/ low to data valid	t_7	30	-	ns	-
Dack/ high to data bus disable	t_8	2	25	ns	-
DACK/ low to DBWR/ low	t_9	0	-	ns	4
DBWR/ pulse width	t_{10}	30	-	ns	-
DBWR/ high to DACK/ high	t_{11}	0	-	ns	4
Data setup to DBWR/	t_{12}	15	-	ns	-
Data hold to DBWR/	t_{13}	0	-	ns	-
DBWR/ high to DBWR/ low	t_{14}	25	-	ns	-

1) *Alternate DMA is disabled.*

2) *For single bus mode (mode zero or mode one) CS/ must be inactive while DACK is active.*

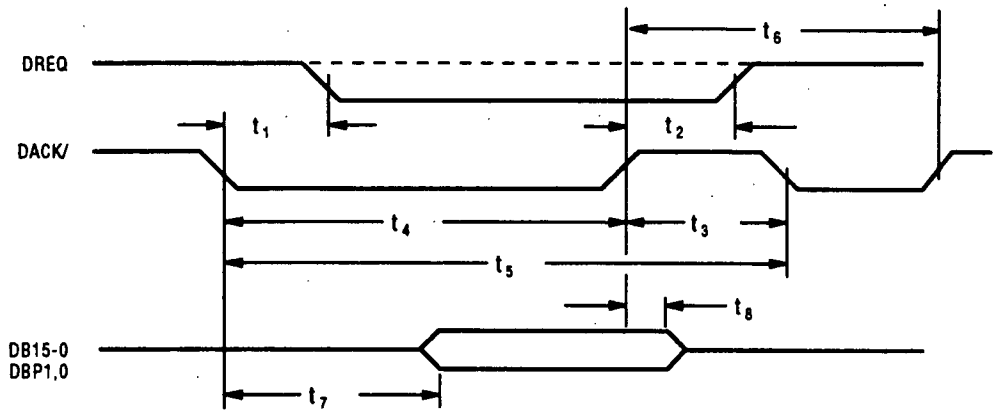
3) *DACK/ must toggle once for each access.*

4) *DBWR/ edges may precede or follow DACK/ edges. Recommended values are:* $t_9 \geq 0$ *and* $t_{11} \geq 0$. *If DBWR/ is held low, the data setup to DACK/ high 10 ns minimum; data hold from DACK/ high is 15 ns mimimum; and* t_3 *is 40 ns mimimum.*

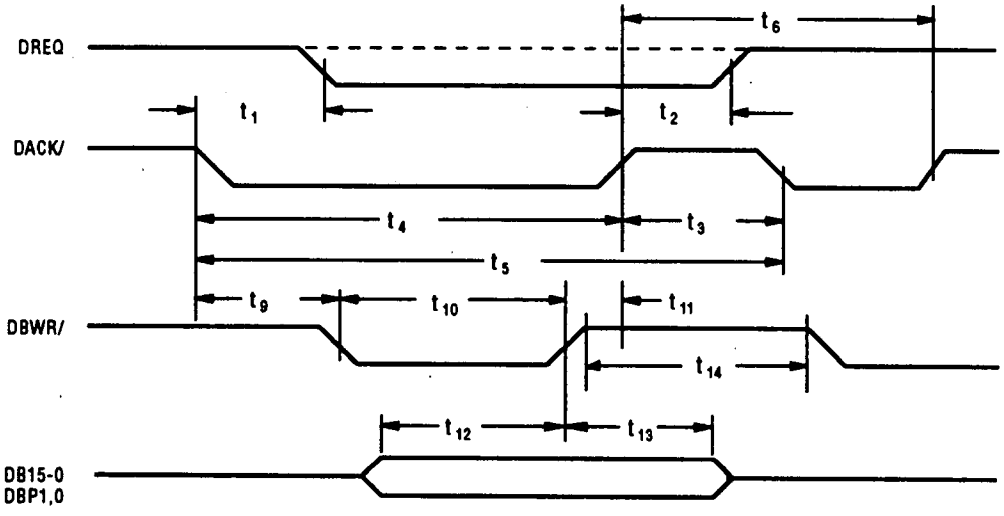
5) *DREQ may stay high if the FIFO has room to accept another word (or byte if byte mode) during DMA write, or send another word (or byte if byte mode) during DMA read. If the current DMA acknolowdge cycle fills the FIFO (write) or empties the FIFO (read), then DREQ will go low.*

6) *Minimum high to high DACK/ period transfer is:*
t_{CS} + 50 − t_3 *for asynchronous SCSI and* t_{CS} + 25 *for synchronous SCSI.*

Figure 6-8. DMA Read Without Byte Control (Configuration modes 0, 1, and 3 only)



Fgure 6-9. DMA Write Without Byte Control (Configuration modes 0, 1, and 3 only)



DMA Interface With Byte Control (Configuration mode 2 only)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ low to DREQ low	t_1	-	30	ns	7
DACK/ high to DREQ high	t_2	-	30	ns	7
DACK/ high to DACK/ low	t_3	12	-	ns	2
DACK/ pulse width	t_4	45	-	ns	-
DACK/ period (low to low)	t_5	95	-	ns	-
DACK/ period (high to high)	t_6	t_{cs} + 25	-	ns	-
BHE, SA0 setup to DBRD/ low	t_7	20	-	ns	-
BHE, SA0 hold from DBRD/ high	t_8	20	-	ns	-
DACK/ low to DBRD/ low	t_9	0	-	ns	5
DBRD/ pulse width	t_{10}	35	-	ns	-
DBRD/ high to DACK high	t_{11}	0	-	ns	5
DBRD/ to data valid	t_{12}	35	-	ns	-
DBRD/ high to data bus disable	t_{13}	2	35	ns	-
BHE, SA0 setup to DBWR/ low	t_{14}	20	-	ns	-
BHE, SA0 hold from DBWR/ high	t_{15}	20	-	ns	-
DACK/ low to DBWR/ low	t_{16}	0	-	ns	6
DBWR/ pulse width	t_{17}	30	-	ns	-
DBWR/ high to DACK high	t_{18}	0	-	ns	6
Data setup to DBWR/ high	t_{19}	15	-	ns	-
Data hold from DBWR/ high	t_{20}	0	-	ns	-
DBWR/ high to DBWR/ low	t_{21}	25	-	ns	-

1) *Alternate DMA is disabled.*
2) *For single bus mode, (mode zero or mode one) CS/ must be inactive.*
3) *DACK/ must toggle once for each access.*
4) *DBRD/ trailing edge may precede or follow DACK/ trailing edge. The recommended value is:* $t_{11} \geq 0$. *If DBRD/ is held low past DACK/, the time from DACK/ low to stable data is 30 ns max, and the time from DACK/ high to data bus disable is 2 ns min and 25 ns max.*
5) *DBWR/ trailing edge may precede or follow DACK/ trailing edge. The recommended value is:* $t_{18} \geq 0$. *If DBWR/ is held past DACK/, the data setup to DACK/ high is 10 ns minimum, data hold from DACK/ high is 10 ns minimum.*
6) *DREQ may stay high if the FIFO has room to accept more data during DMA write, or send more data during DMA read. If the current DMA acknowledge cycle fills the FIFO (write) or empties the FIFO (read), then DREQ will go low.*

Figure 6-10. DMA Read With Byte Control (Configuration mode 2 only)

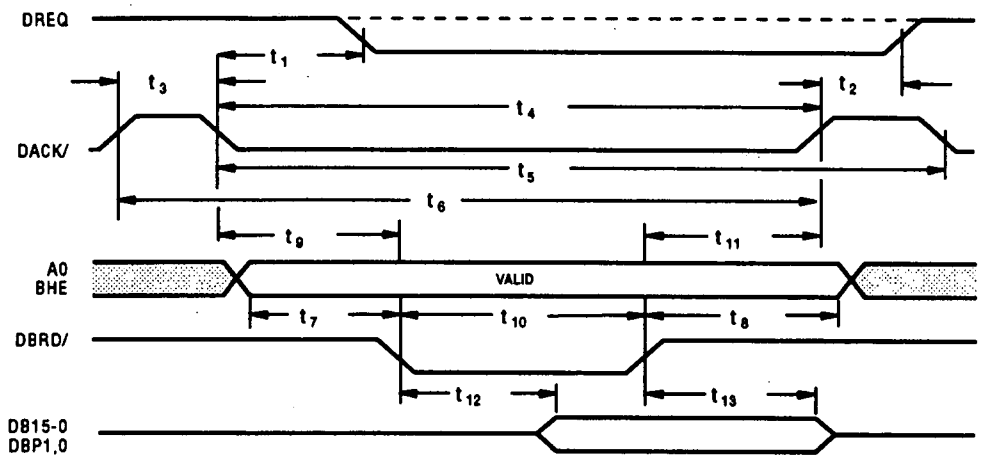
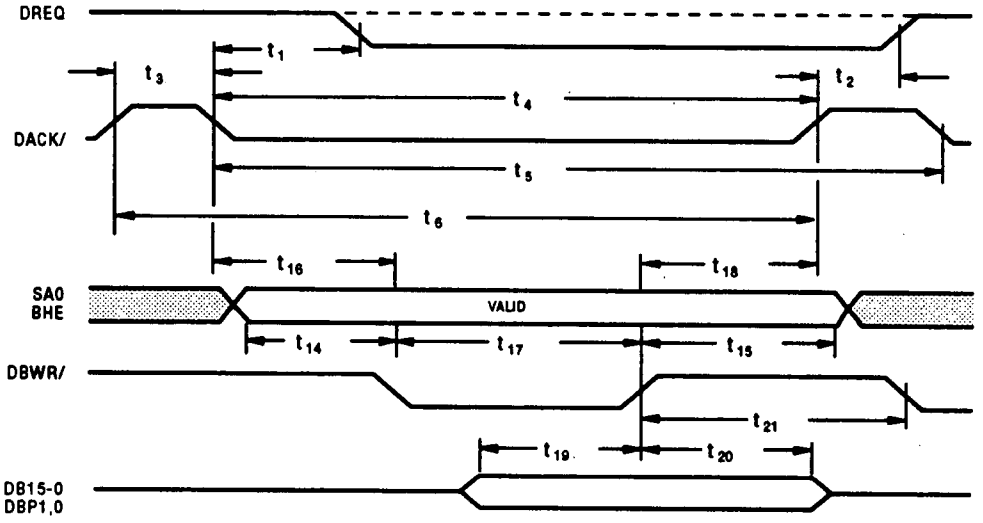


Figure 6-11. DMA Write With Byte Control (Configuration mode 2 only)



Burst Mode DMA Interface (Bus Configuration Modes 0, 1)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ high to DREQ high	t_1	-	30	ns	3
DACK/ low to DREQ low	t_2	-	30	ns	1
DACK/ high to DACK/ low	t_3	60	-	ns	-
DACK/ pulse width	t_4	70	-	ns	-
RD/ high to DREQ low	t_5	90	-	ns	2
DACK/ low to RD/ low	t_6	0	-	ns	-
RD/ pulse width	t_7	70	-	ns	-
RD/ high to RD/ low	t_8	60	-	ns	-
RD/ low to data valid	t_9	55	-	ns	-
RD/ high to data bus disable	t_{10}	-	45	ns	-
RD/ low to RD/ low	t_{11}	130	-	ns	-
RD/ high to RD/ high	t_{12}	t_{CS}+ 50	-	ns	-
DBWR/ high to DREQ low	t_{13}	90	-	ns	2
DACK/ low to DBWR/ low	t_{14}	0	-	ns	-
DBWR/ pulse width	t_{15}	70	-	ns	-
DBWR/ high to DBWR/ low	t_{16}	60	-	ns	-
Data setup to DBWR/ high	t_{17}	15	-	ns	-
Data hold from DBWR/ high	t_{18}	0	-	ns	-
DBWR/ low to DBWR/ low	t_{19}	160	-	ns	-
DBWR/ high to DBWR/ high	t_{20}	t_{CS}+ 50	-	ns	-

1) *Single DMA transfer only.*

2) *Multiple DMA transfers only.*

3) *Assertion pending. If the FIFO is empty during DMA read, or full during DMA write, then assertion will not be pending.*

Figure 6-12. Burst Mode DMA Read (Bus Configuration Modes 0, 1)

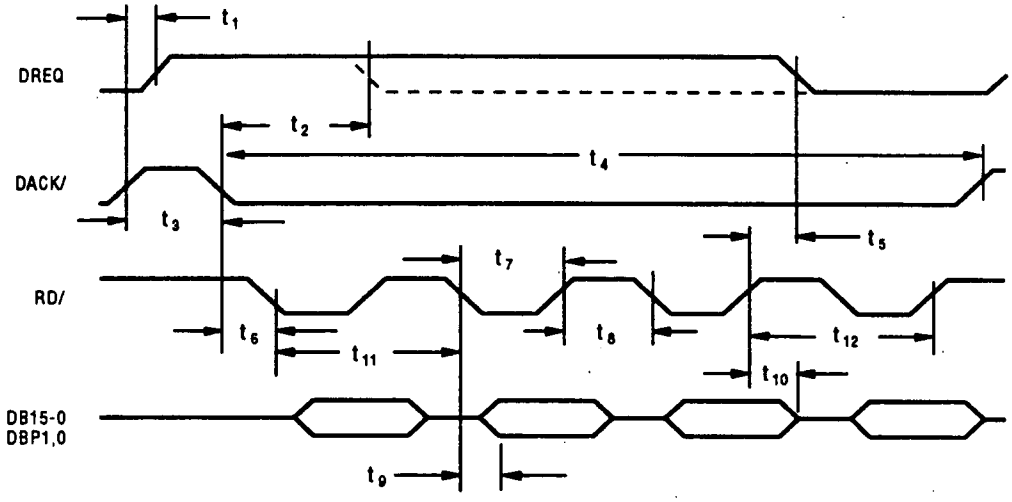
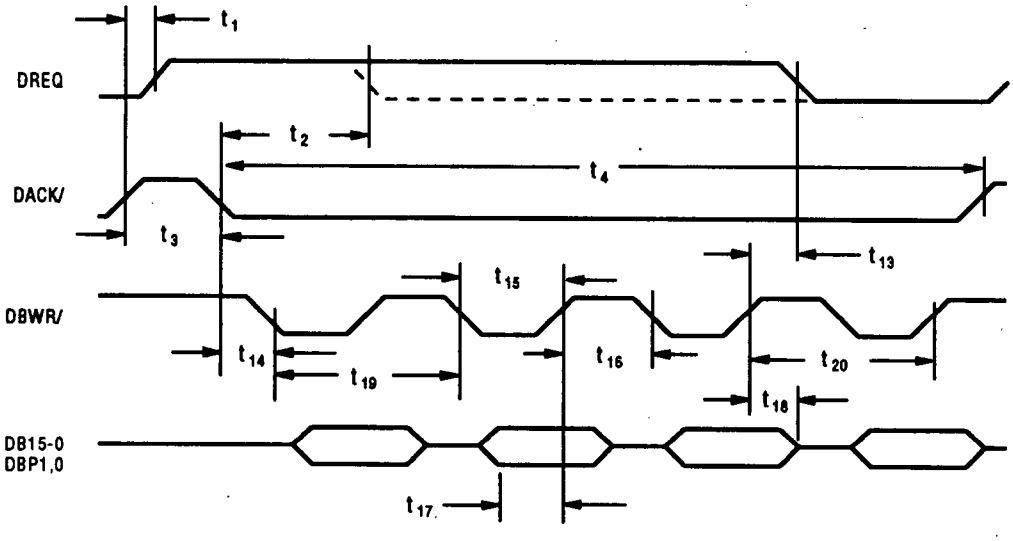


Figure 6-13. Burst Mode DMA Write (Bus Configuration Modes 0, 1)



Burst Mode DMA Interface With Byte Control (Bus Configuration Mode 2)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ high to DREQ high	t_1	-	30	ns	3
DACK/ low to DREQ low	t_2	-	30	ns	1
DACK/ high to DACK/ low	t_3	60	-	ns	-
DACK/ pulse width	t_4	70	-	ns	-
DBRD/ high to DREQ low	t_5	90	-	ns	2
BHE, SA0 setup to DBRD/ low	t_6	20	-	ns	-
BHE, SA0 hold after DBRD/ high	t_7	20	-	ns	-
DACK/ low to DBRD/ low	t_8	0	-	ns	-
DBRD/ pulse width	t_9	70	-	ns	-
DBRD/ high to DBRD/ low	t_{10}	60	-	ns	-
DBRD/ low to data valid	t_{11}	55	-	ns	-
DBRD/ high to data bus disable	t_{12}	-	45	ns	-
DBRD/ low to DBRD/ low	t_{13}	130	-	ns	-
DBRD/ high to DBRD/ high	t_{14}	t_{CS}+ 50	-	ns	-
DBWR/ high to DREQ low	t_{15}	90	-	ns	2
BHE, SA0 setup to DBWR/ low	t_{16}	20	-	ns	-
BHE, SA0 hold after DBWR/ high	t_{17}	20	-	ns	-
DACK/ low to DBWR/ low	t_{18}	0	-	ns	-
DBWR/ pulse width	t_{19}	70	-	ns	-
DBWR/ high to DBWR/ low	t_{20}	60	-	ns	-
Data setup to DBWR/ high	t_{21}	15	-	ns	-
Data hold from DBWR/ high	t_{22}	0	-	ns	-
DBWR/ low to DBWR/ low	t_{23}	160	-	ns	-
DBWR/ high to DBWR/ high	t_{24}	t_{CS}+ 50	-	ns	-

1) Single DMA transfer only.

2) Multiple DMA transfers only.

3) Assertion pending. If the FIFO is empty during DMA read, or full during DMA write, then assertion will not be pending.

Figure 6-14. Burst Mode DMA Read With Byte Control (Bus Configuration Mode 2)

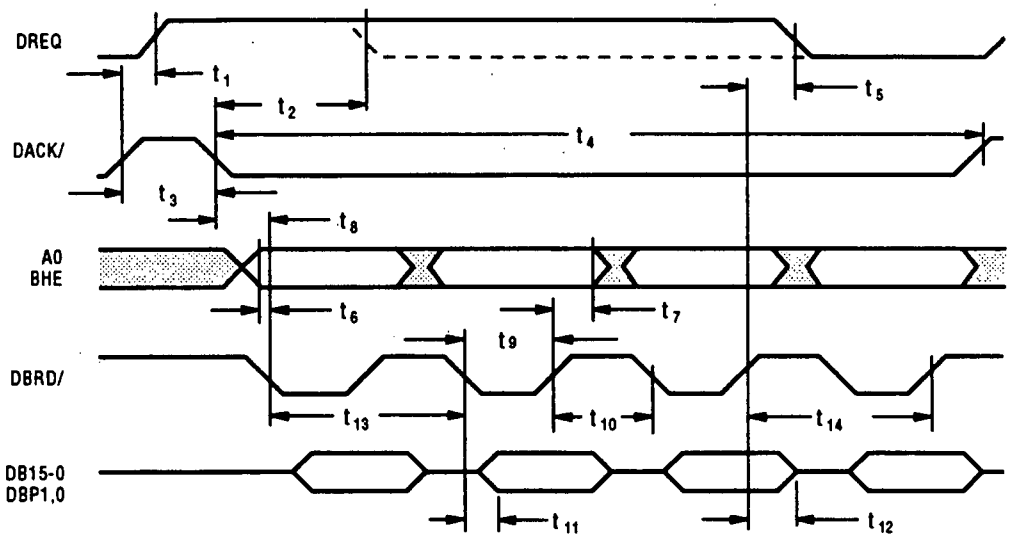
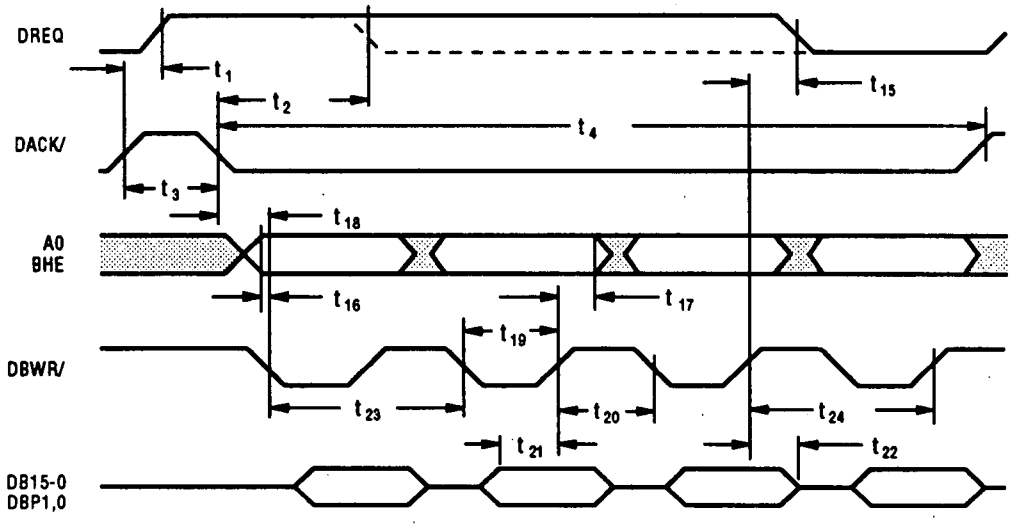


Figure 6-15. Burst Mode DMA Write With Byte Control (Bus Configuration Mode 2)



Burst Mode DMA Interface (Bus Configuration Mode 3)

Parameter	Symbol	Min	Max	Units	Notes
DACK/ high to DREQ high	t_1	-	30	ns	3
DACK/ low to DREQ low	t_2	-	30	ns	1
DACK/ pulse width	t_3	70	-	ns	-
DACK/ high to DACK/ low	t_4	60	-	ns	-
DACK/ low to data valid	t_5	35	-	ns	-
DACK/ high to data bus disable	t_6	-	25	ns	-
DACK/ low to DACK/ low	t_7	160	-	ns	-
DACK/ high to DACK/ high	t_8	t_{CS}+ 50	-	ns	-
DACK/ high to DREQ low	t_9	90	-	ns	2
DBWR/ low to DACK/ low	t_{10}	TBD	-	ns	-
Data setup to DACK/ high	t_{11}	15	-	ns	-
Data hold from DACK/ high	t_{12}	0	-	ns	-

1) Single DMA transfer only.

2) Multiple DMA transfers only.

3) Assertion pending. If the FIFO is empty during DMA read, or full during DMA write, then assertion will not be pending.

4) DACK/ is used for DMA reads and writes. DACK/ must toggle, and is assumed to be coincident with an external read signal.

Figure 6-16. Burst Mode DMA Read
(Bus Configuration Mode 3)

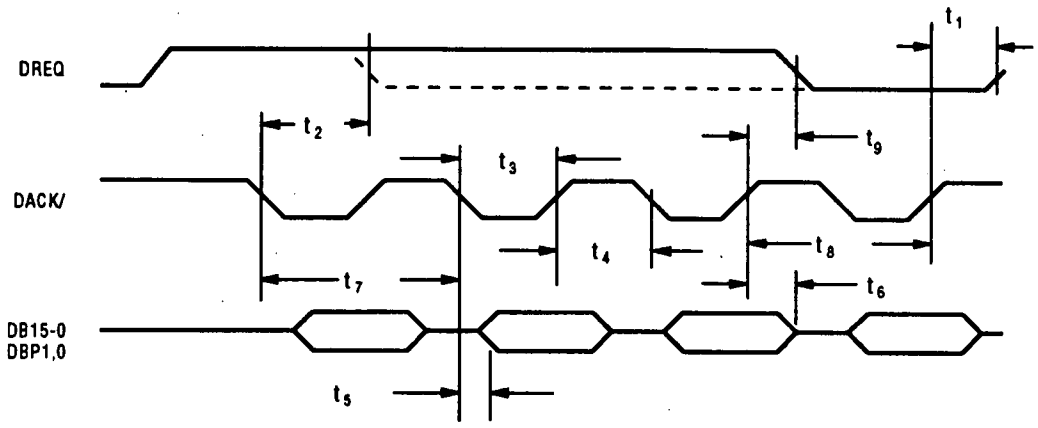
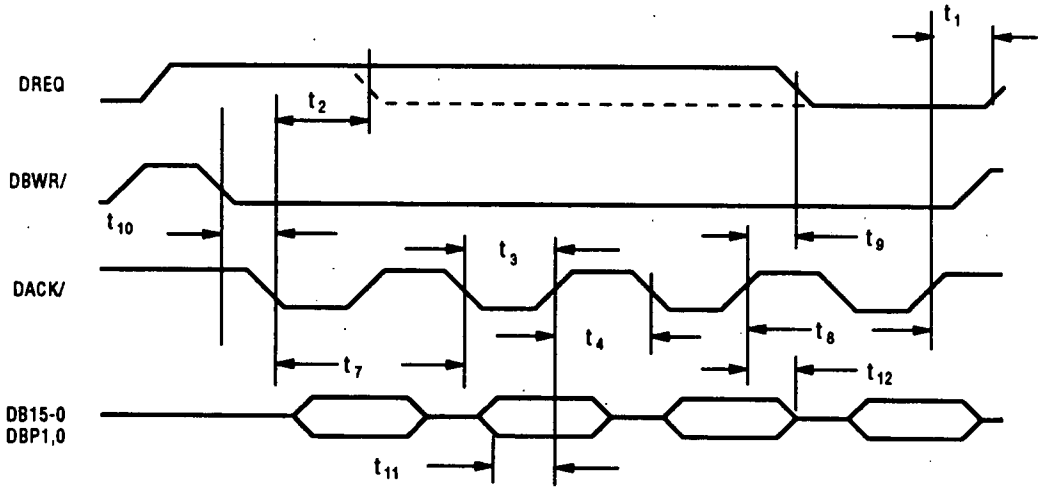


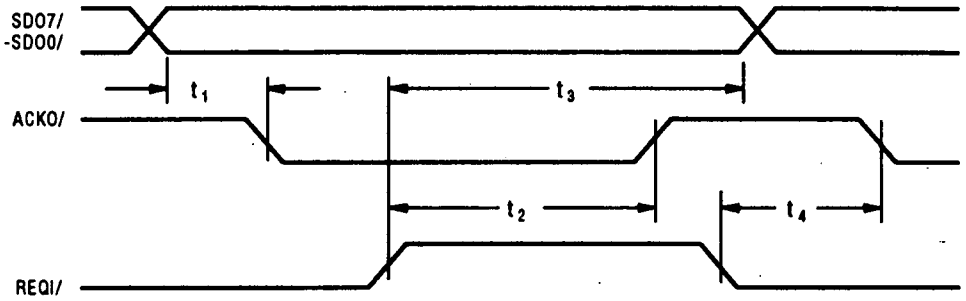
Figure 6-17. Burst Mode DMA Write
(Bus Configuration Mode 3)



SCSI Timings

Initiator Asynchronous Send

Figure 6-18. Initiator Asynchronous Send



Single-Ended Mode

Parameter	Symbol	Min	Max	Units
Data setup to ACKO/ low	t_1	60	-	ns
REQI/ high to ACKO/ high	t_2	-	50	ns
Data hold from REQI/ high	t_3	5	-	ns
REQI/ low to ACKO/ low (data already set up)	t_4	-	50	ns

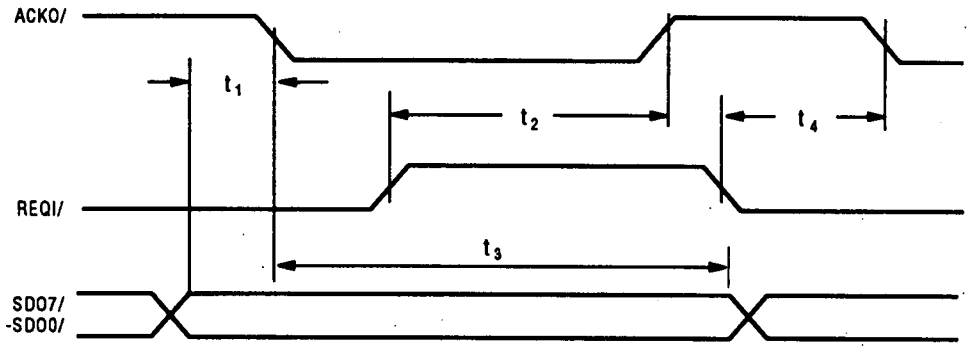
Differential Mode*

Parameter	Symbol	Min	Max	Units
Data setup to ACKO/ low	t_1	70	-	ns
REQI/ high to ACKO/ high	t_2	-	25	ns
Data hold from REQI/ high	t_3	-	50	ns
REQI/ low to ACKO/ low (data already setup)	t_4	-	25	ns

* Note Data for Differential Mode refers to SDI7/ - SDI0/

Initiator Asynchronous Receive

Figure 6-19. Initiator Asynchronous Receive



Single-Ended Mode

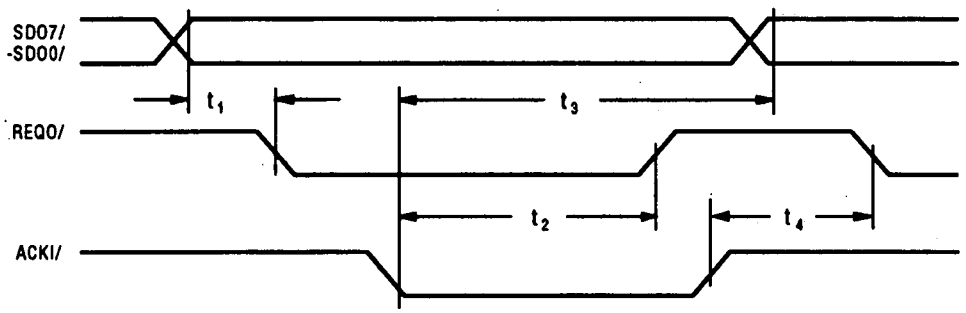
Parameter	Symbol	Min	Max	Units
Data setup to ACKO/ low	t_1	0	-	ns
REQI/ high to ACKO/ high	t_2	-	25	ns
Data hold from ACKO/ low	t_3	0	-	ns
REQI/ low to ACKO/ low (data already set up)	t_4	-	30	ns

Differential Mode

Parameter	Symbol	Min	Max	Units
Data setup to ACKO/ low	t_1	0	-	ns
REQI/ high to ACKO/ high	t_2	-	25	ns
Data hold from ACKO/low	t_3	0	-	ns
REQI/ low to ACKO/ low (data already setup)	t_4	-	30	ns

Target Asynchronous Send

Figure 6-20. Target Asynchronous Send



Single-Ended Mode

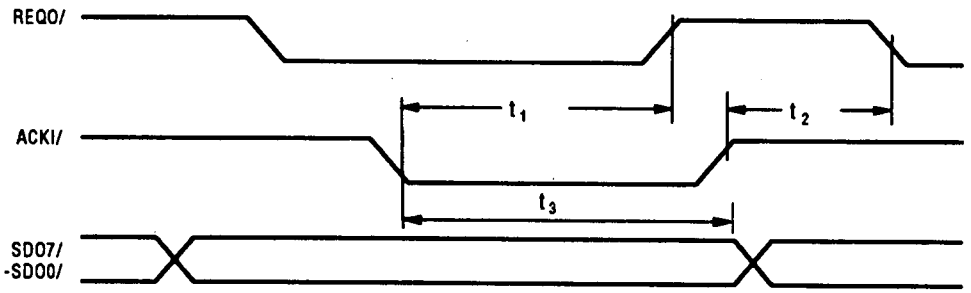
Parameter	Symbol	Min	Max	Units
Data setup to REQO/ low	t_1	60	-	ns
ACKI/ low to REQO/ high	t_2	-	50	ns
Data hold from ACKI/ low (FIFO not empty)	t_3	5	-	ns
ACKI/ high to REQO/ low (Data already set up)	t_4	-	45	ns

Differential Mode

Parameter	Symbol	Min	Max	Units
Data setup to REQO/ low	t_1	70	-	ns
ACKI/ low to REQO/ high	t_2	-	30	ns
Data hold from ACKI/ high (FIFO not empty)	t_3	5	-	ns
ACKI/ high to REQO/ low (Data already set up)	t_4	-	30	ns

Target Asynchronous Receive

Figure 6-21. Target Asynchronous Receive



Single-Ended Mode

Parameter	Symbol	Min	Max	Units
ACKI/ low to REQO/ high	t_1	-	50	ns
ACKI/ high to REQO/ low (FIFO not full)	t_2	-	45	ns
Data hold from ACKI/ low	t_3	5	-	ns

Differential Mode

Parameter	Symbol	Min	Max	Units
ACKI/ low to REQO/ high	t_1	-	30	ns
ACKI/ high to REQO/ low (FIFO not full)	t_2	-	30	ns
Data hold from ACKI/ low	t_3	5	-	ns

Target and Initiator Synchronous Transfers

Figure 6-22. Target and Initiator Synchronous Output

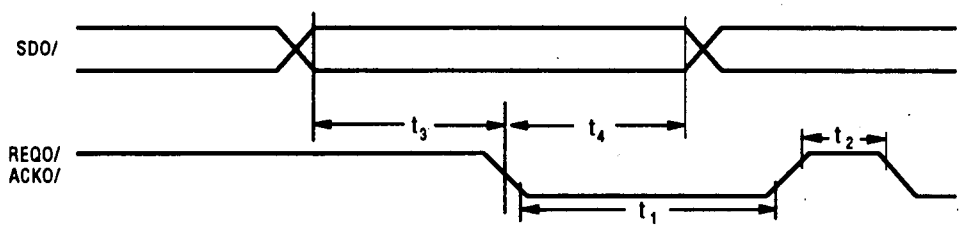
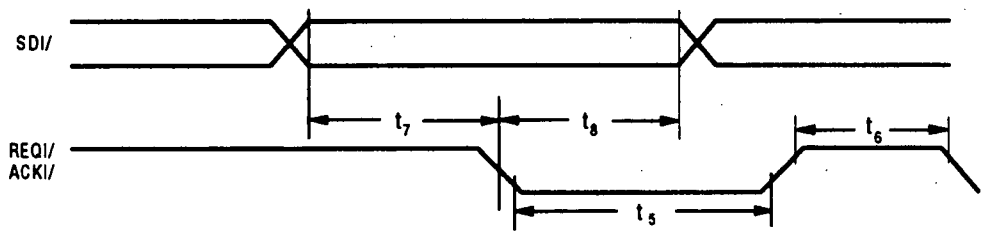


Figure 6-23. Target and Initiator Synchronous Input



SCSI-1 Single-Ended Transfers (5 MB/s)

Parameter	Symbol	Min	Max	Units
REQO/ or ACKO/ assertion period	t_1	90	-	ns
REQO/ or ACKO/ negation period	t_2	90	-	ns
Data setup to REQO/ or ACKO/ low	t_3	65	-	ns
Data hold from ACKO/ or REQO/ low	t_4	100	-	ns
REQI/ or ACKI/ assertion period	t_5	90	-	ns
REQI/ or ACKI/ negation period	t_6	90	-	ns
Data setup to REQI/ low or ACKI/ low	t_7	0	-	ns
Data hold from REQI/ low or ACKI/ low	t_8	45	-	ns

SCSI-1 Differential Transfers (5MB/s)

Parameter	Symbol	Min	Max	Units
REQO/ or ACKO/ assertion period	t_1	90	-	ns
REQO/ or ACKO/ negation period	t_2	90	-	ns
Data setup to REQO/ or ACKO/ low	t_3	65	-	ns
Data hold from REQO/ orACKO/ low	t_4	100	-	ns
REQI/ or ACKI/ assertion period	t_5	90	-	ns
REQI/ or ACKI/ negation period	t_6	90	-	ns
Data setup to REQI/ low or ACKI/ low	t_7	0	-	ns
Data hold from REQI/ low or ACKI/ low	t_8	45	-	ns

Fast SCSI-2 Single-Ended Transfers (10 MB/s)

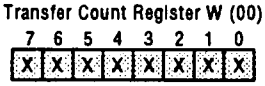
Parameter	Symbol	Min	Max	Units
REQO/ or ACKO/ assertion period	t_1	30	-	ns
REQO/ or ACKO/ negation period	t_2	30	-	ns
Data setup to REQO/ or ACKO/ low	t_3	25	-	ns
Data hold from REQO/ or ACKO/ low	t_4	35	-	ns
REQI/ or ACKI/ assertion period	t_5	24	-	ns
REQI/ or ACKI/ negation period	t_6	24	-	ns
Data setup to REQI/ low or ACKI/ low	t_7	0	-	ns
Data hold from REQI/ low or ACKI/ low	t_8	10	-	ns

Fast SCSI-2 Differential Transfers (10 MB/s)

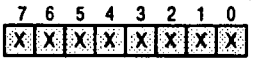
Parameter	Symbol	Min	Max	Units
REQO/ or ACKO/ assertion period	t_1	40	-	ns
REQO/ or ACKO/ negation period	t_2	40	-	ns
Data setup to REQO/ or ACKO/ low	t_3	35	-	ns

Appendix A
Register Summary

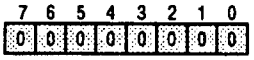
Transfer Count Register W (00)



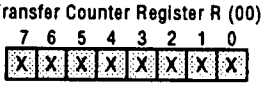
Transfer Count Register W (01)



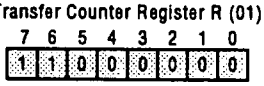
FIFO Register R/W (02)



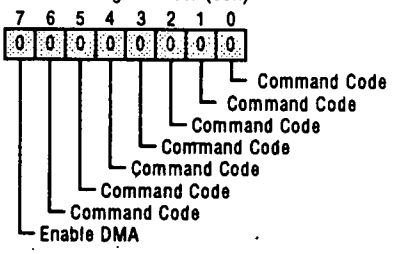
Transfer Counter Register R (00)



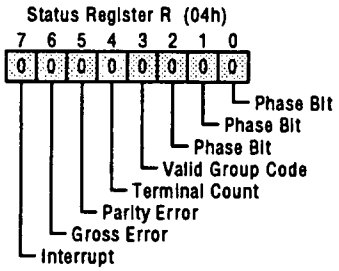
Transfer Counter Register R (01)



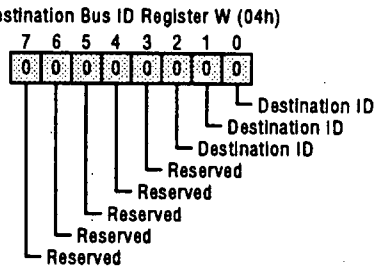
Command Register R/W (03h)



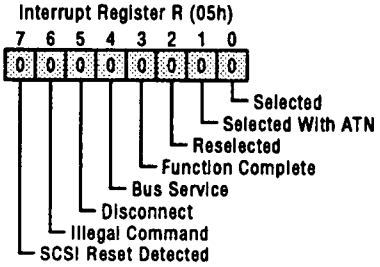
Status Register R (04h)



Destination Bus ID Register W (04h)

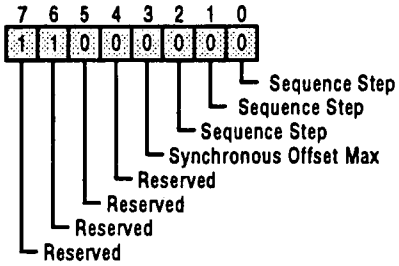


Interrupt Register R (05h)

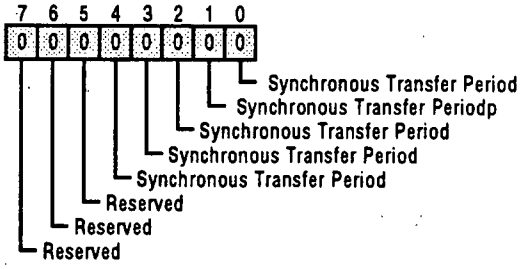


Select/ Reselect
Time-Out Register W (05h)

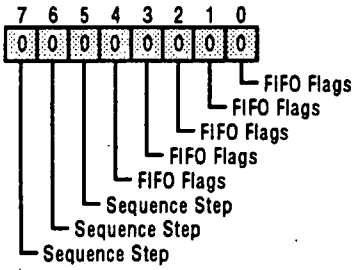
Sequence Step Register R (06h)



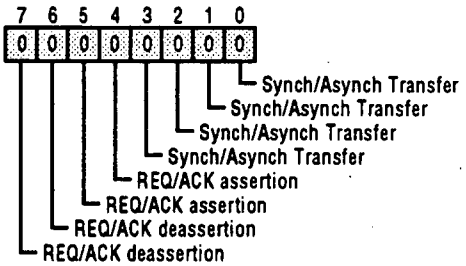
Synchronous Transfer Period Register W (06h)



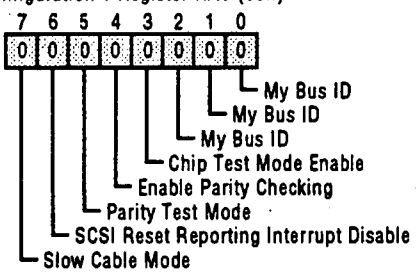
FIFO Flags Sequence Step Register R (07h)



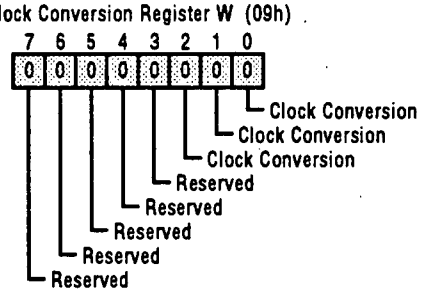
Synchronous Offset Register W (07h)



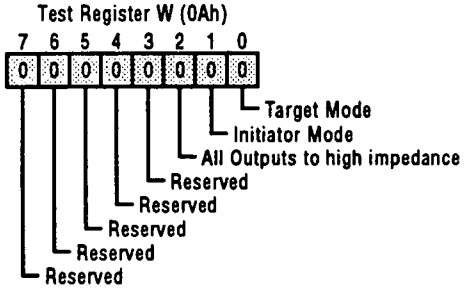
Configuration 1 Register R/W (08h)



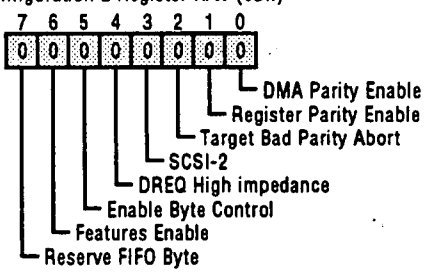
Clock Conversion Register W (09h)



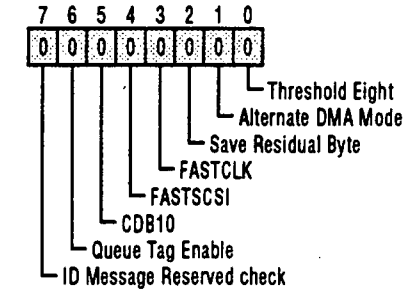
Test Register W (0Ah)



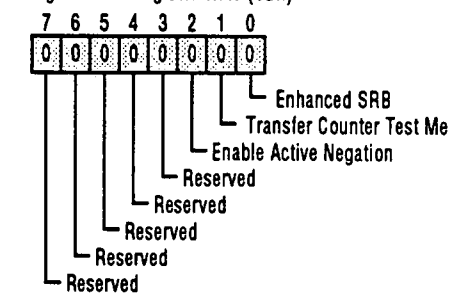
Configuration 2 Register R/W (0Bh)



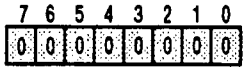
Configuration 3 Register R/W (0Ch)



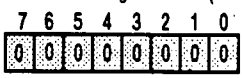
Configuration 4 Register W/W (0Dh)



Transfer Counter High/ID Register R/W (0Eh)



FIFO Bottom Register R/W (0Fh)



Appendix B
Bus Configurations

Figure B-1. Mode Zero
(Single bus, 8-bit DMA, 8-bit processor)

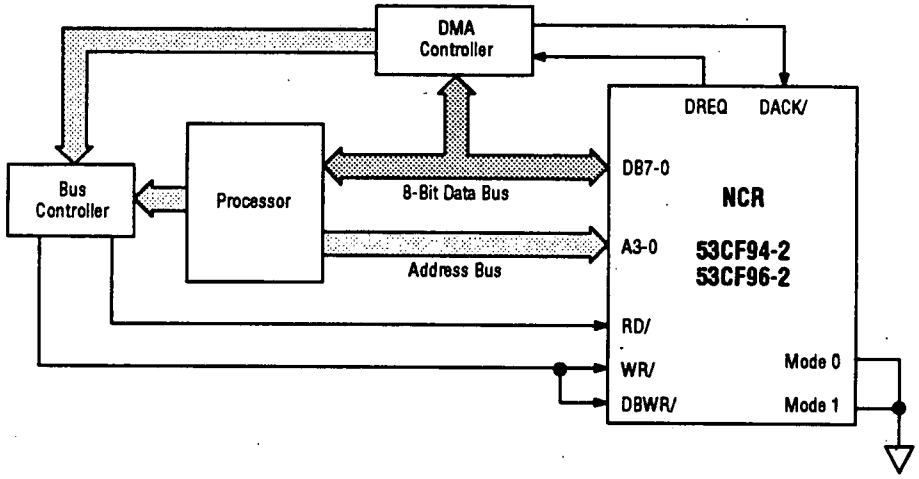


Figure B-2. Mode One
(Single bus, 16-bit DMA, 8-bit processor bus)

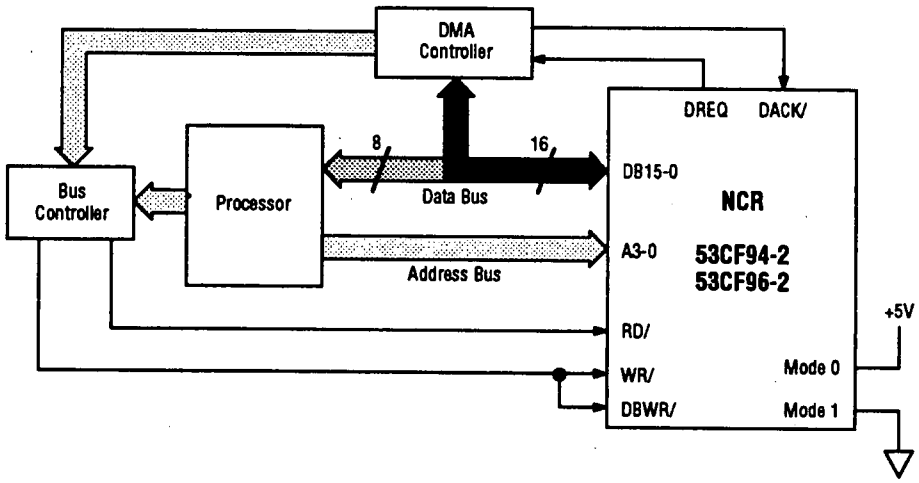


Figure B-3. Mode Two
(Dual bus, 8 or 16-bit DMA bus with byte control and 8-bit multiplexed processor address/data bus)

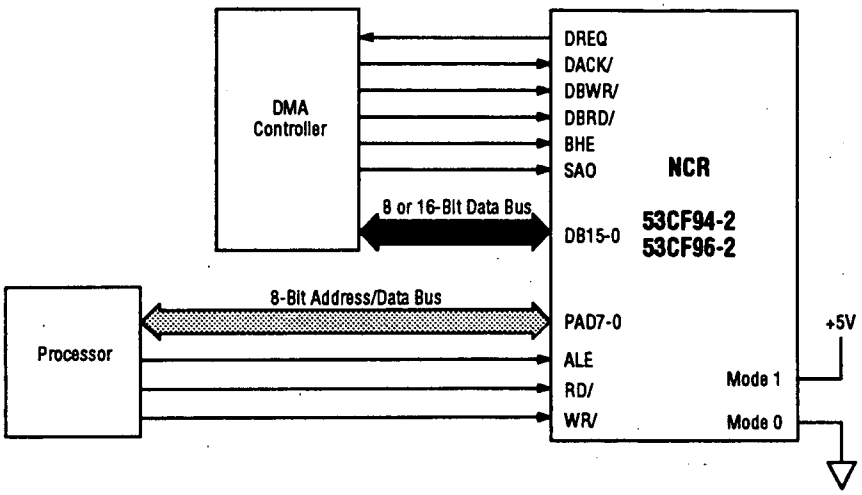
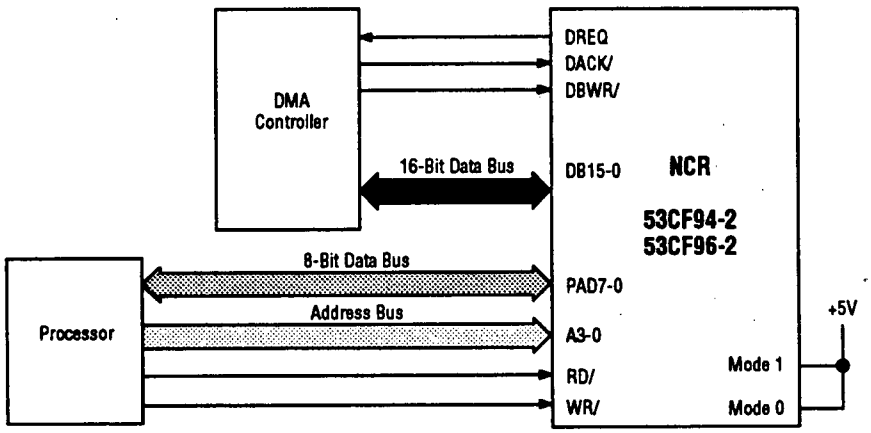


Figure B-4. Mode Three
(Dual bus, 16-bit DMA bus and 8-bit processor bus)



Appendix C
Wiring Diagrams

Figure C-1. 53CF94 and 53CF96
Single-Ended SCSI Bus Interface

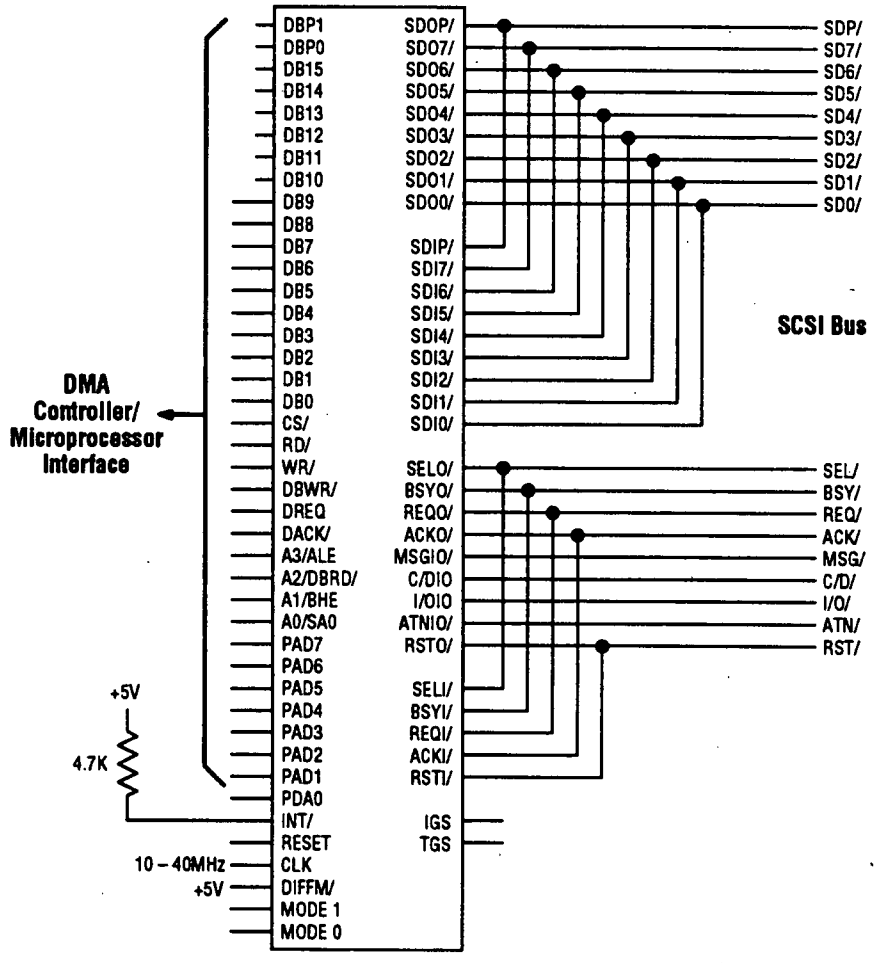
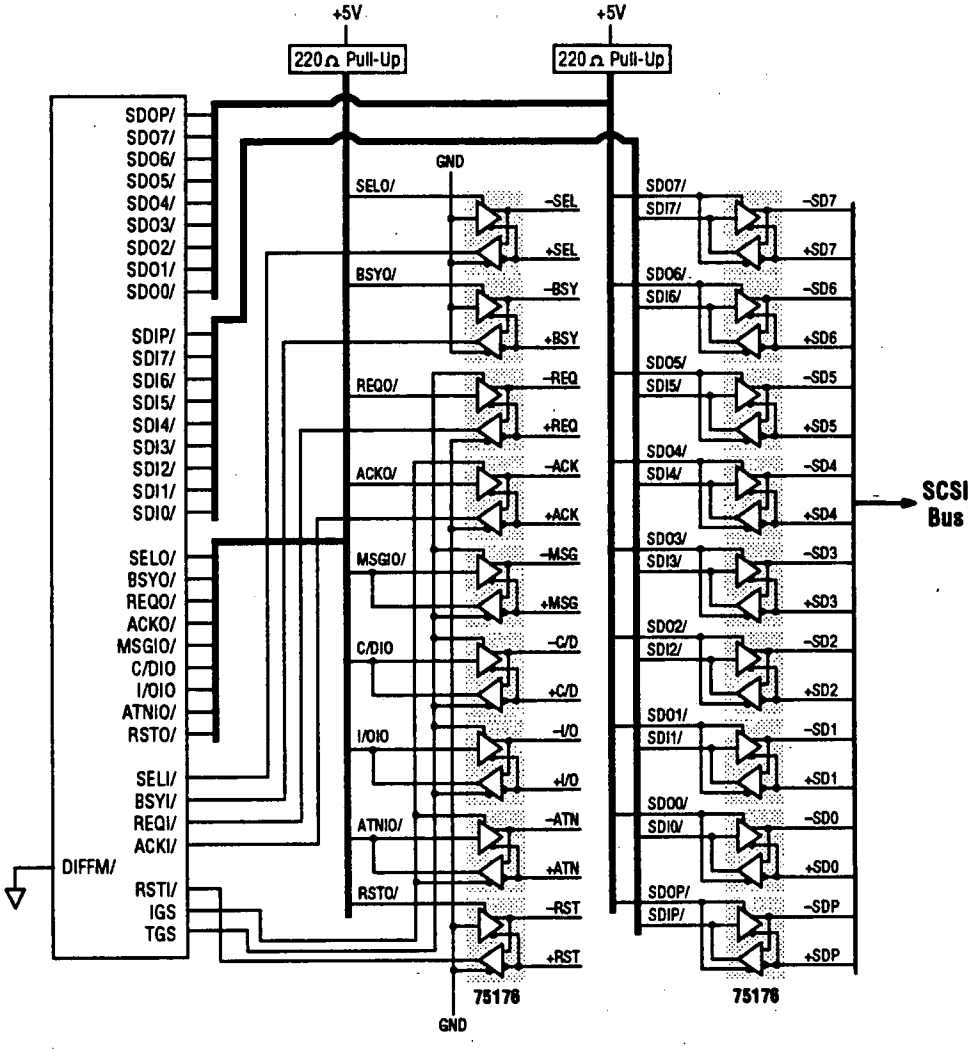
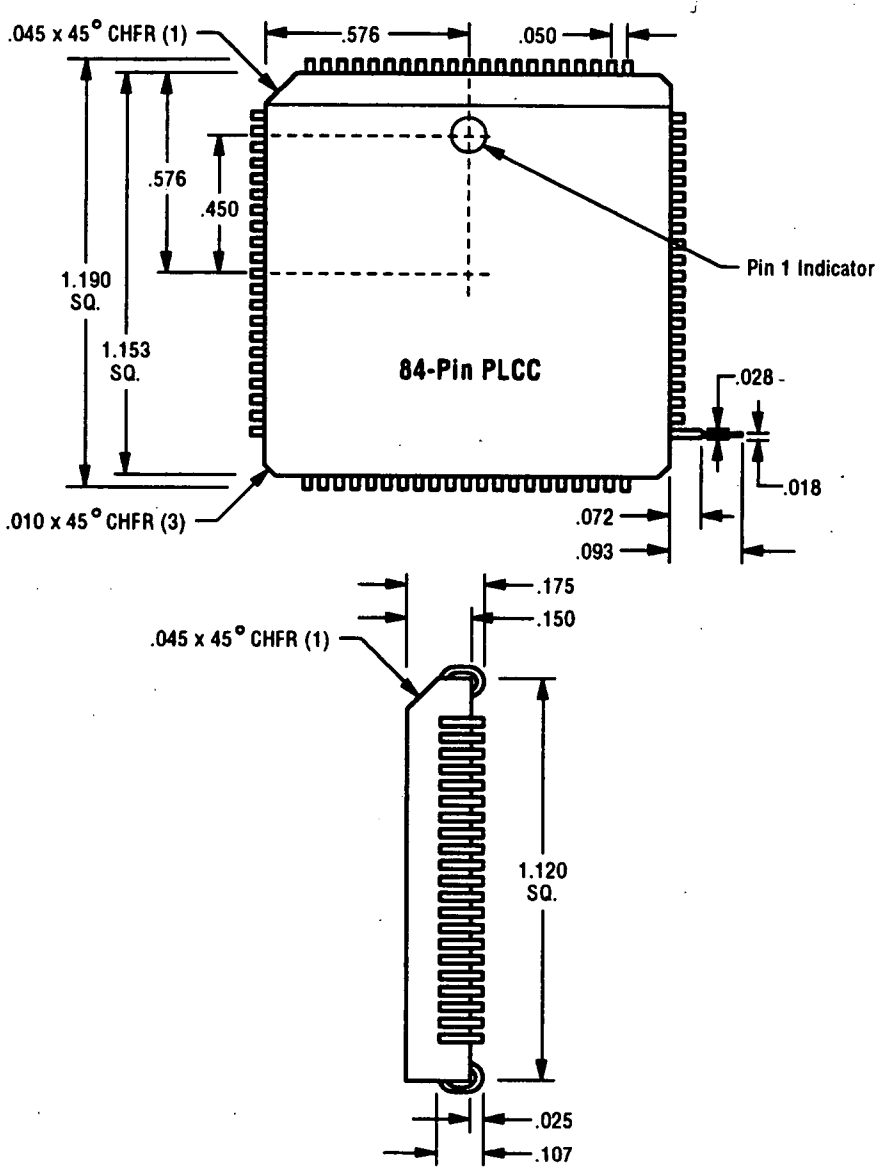


Figure C-2. 53CF96
Differential SCSI Bus Interface



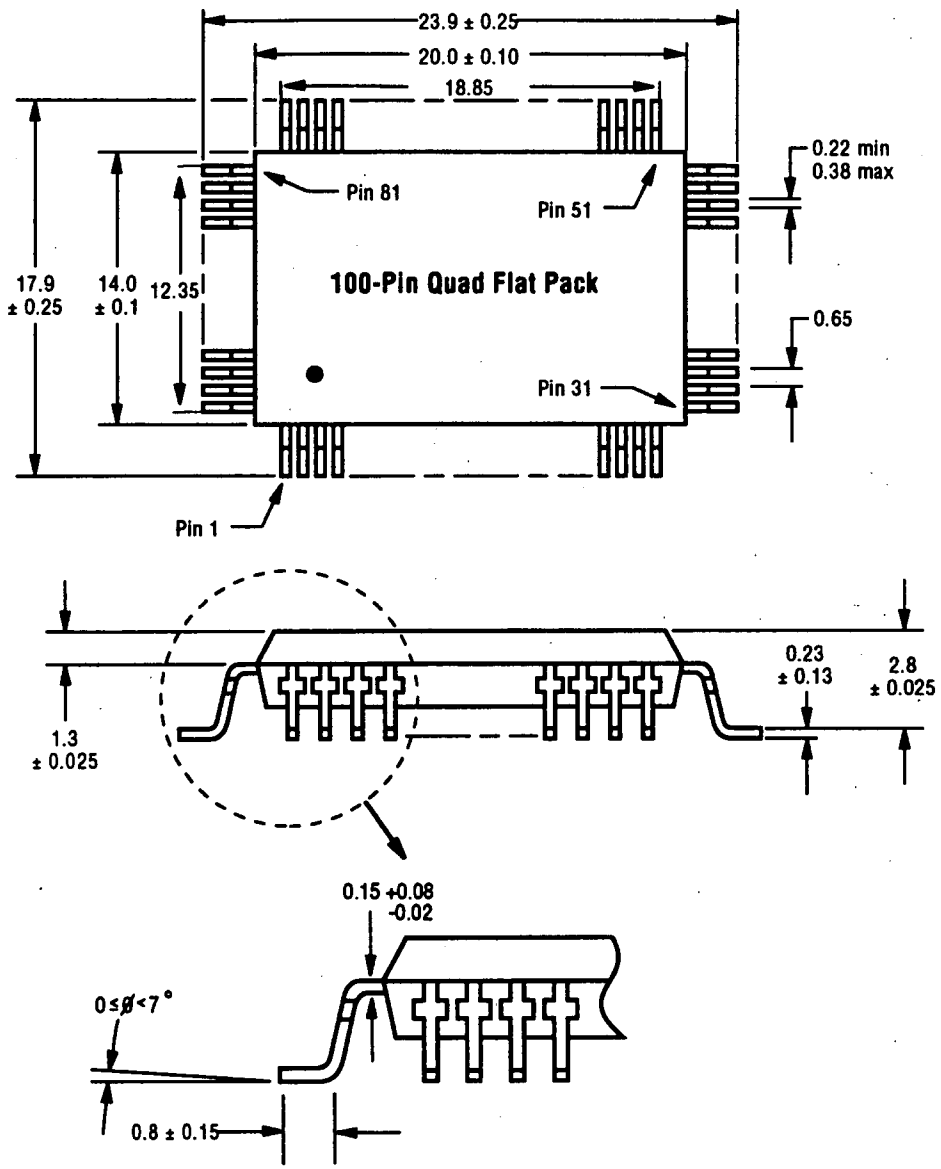
Appendix D
Mechanical Drawings

Figure D-1. 84-Pin PLCC



Note: All dimensions are in inches

Figure D-2. 100-Pin Quad Flat Pack



Note: All dimensions are in millimeters

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