NEC Microcomputers, Inc.

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Application Note 8

PRELIMINARY

μPD765 SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

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APPLICATIONS NOTE #8

NEC uPD765C Single/Double Density Floppy Disk Controller

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INTRODUCTION

The Floppy Disk Drive (FDD) has proven to be one of the most popular peripherals on the market today. The development of double density recording and the use of both sides of the diskette, has allowed a fourfold increase in recording capability. This increased capability has resulted in a large number of new Floppy Disk Controller (FDC) designs to be undertaken. The uPD765 has been developed to allow the designer to take full advantage of these new floppy disk capabilities as well as to design a more sophisticated disk system. The 15 instructions which the uPD765 will perform enhance system throughput and minimize support from the processor. There are several signals generated within the uPD765 (such as VCO Sync and MFM Mode) which greatly reduce the amount of supporting hardware required to make a working floppy disk system.

This Application Note presents a complete Floppy Disk Controller design, and allows you to add or subtract the features you feel are important. However, the design shown in this Application Note is not the only configuration which is possible with the uPD765. This design should be used as a building block in satisfying your particular requirements.

Whichever FDC design approach is selected, an early decision which must be made is whether or not Direct Memory Access (DMA) is required. The uPD765 will operate in either a DMA or a Non-DMA configured system. The Non-DMA configuration usually results in a simple interrupt-driven system. An interrupt-driven system yields the minimum amount of hardware and system complexity, but if double density recording (MFM) is to be done, then extremely tight timing constraints result. In single density recording (FM) the processor has 32 us (normally) and 29 us (worst-case) between interrupts, but in double density these numbers reduce to 16 us (normally) and 13 us (worst-case). As a result, in the interrupt-driven system the processor must be capable of servicing interrupts at a very high rate. If this places an undue load on the processor or seriously inhibits system throughput rate, then the DMA approach represents an excellent solution to the time constraint problem.

A complete detailed design as well as a detailed software flow chart is given for a DMA-driven system. This approach was not chosen for the design example because it is better, but merely because this example covers more possible user configurations. The flow chart shown at the end of this Application Note is especially useful because it both shows the proper sequence of events and provides detailed information so that software can be written to control the uPD765.

SYSTEM BLOCK DIAGRAM

Figure 1 shows how the 765 may be configured in a typical system. The uPD765 may be easily interfaced to any of the popular microprocessors such as uPD8080A,

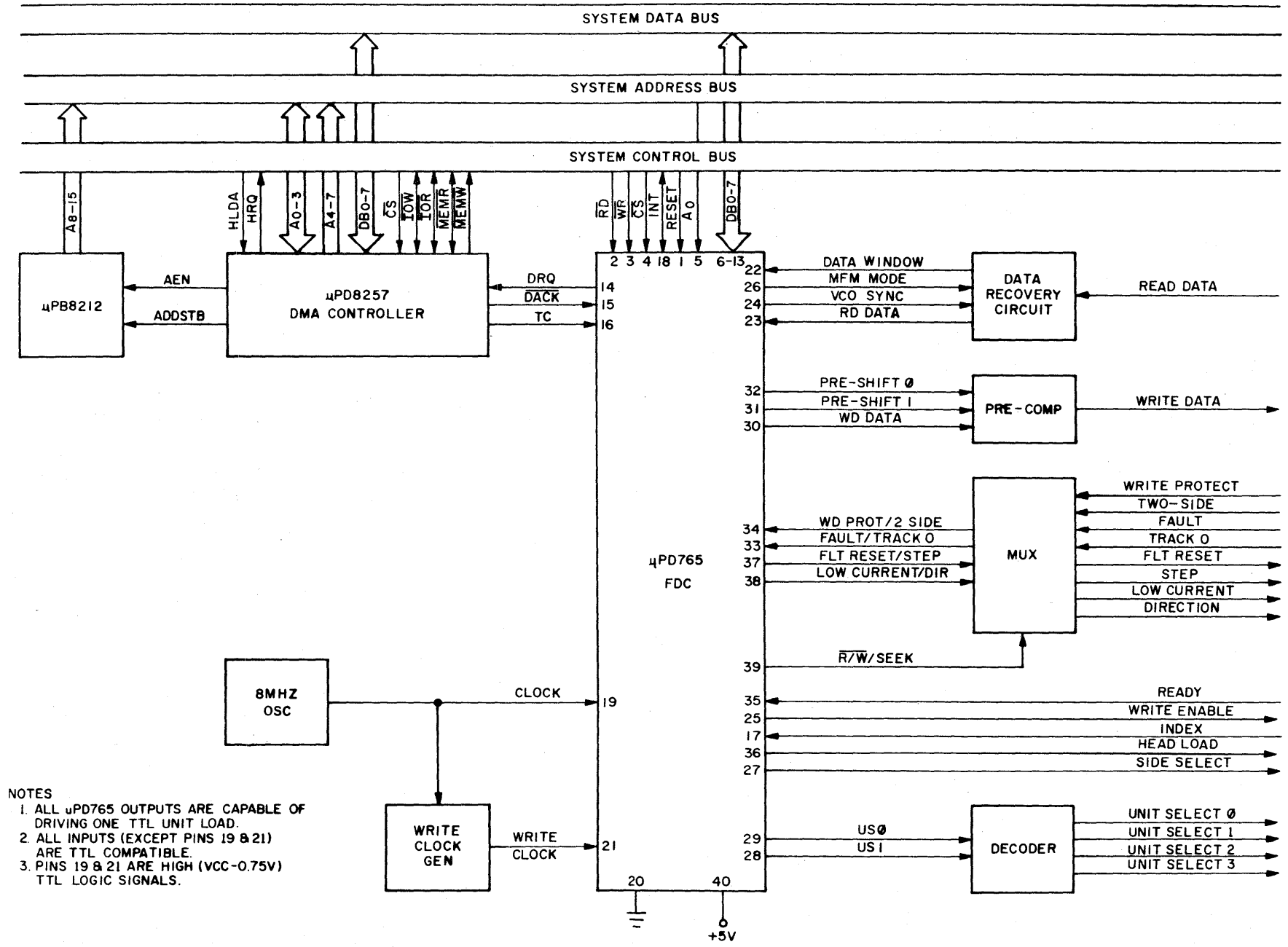

FIGURE 1
SYSTEM BLOCK DIAGRAM OF A FLOPPY DISK CONTROLLER

uPD8085A, uPD780 (Z80™), 6800, 6502, etc. If the FDC is to be interrupt-driven instead of DMA-driven, then the uPB8212 and the uPD8257 (or other hardware associated with the DMA Controller) may be eliminated and their functions will be taken over by the processor.

Two clocks are required by the uPD765. The clock on pin 18 (CLK) is typically 8 MHz, and may be totally asynchronous with the processor or system clock. The Write Clock on pin 21 (WCK) controls the rate at which data is sent to the drive electronics (for writing onto the diskette) and is either 500 KHz or 1 MHz, depending upon whether single or double density data is to be written (see page 5 of Data Sheet). There are 19 lines which interface to the floppy disk drive. Several of these signals may be connected directly to the drive. Other signals require demultiplexing, decoding or signal conditioning The external circuits that perform these functions require typically only 5.5 TTL I.C.'s. The DMA interface consists of only three signals: DRQ (DMA Request, pin 14), DACK-NOT (DMA Acknowledge, pin 15) and TC (Terminal Count, pin 16). These three signals interface directly to the uPD8257 DMA Controller as well as many other popular DMA Controller I.C.'s.

PROCESSOR INTERFACE

Command Sequence

The uPD765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor to the uPD765, and the result after execution of the command may also be a multi-byte transfer back from the uPD765 to the processor. Because of this multi-byte interchange of information between the uPD765 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The uPD765 receives all information required to perform a particular operation from the processor.

Execution Phase: The uPD765 performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are returned to the processor.

The processor interface is simple, consisting of RD-NOT (Read, pin 2), WR-NOT (Write, pin 3), CS-NOT (Chip Select, pin 4), INT (Interrupt, pin 18), RESET (pin 1), Ao (Address Line, pin 5) and an 8-bit Bidirectional Data Bus (pins 6-13). The Read/Write signals RD-NOT and WR-NOT transfer data from the processor to the Data Bus. The polarity of Ao (pin 5) determines whether the Main Status Register or the Data Register is present on the Data Bus.

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Table 1 shows the relationship between the Status/Data Registers and the RD-NOT, WR-NOT and Ao.

Table 1: Selection of Status or Data Register

CS-NOT	Ao	RD-NOT	WR-NOT	FUNCTION	DIRECTION OF SIGNAL ON DATA BUS
0	0	0	1	Read Status Register	Out FDC Data Bus into Processor
0	0	1	0	Illegal	
0	0	0	0	Illegal	
0	1	0	0	Illegal	
0	1	0	1	Read from Data Register	Out FDC Data Bus into Processor
0	1	1	0	Write into Data Register	Out Processor into FDC Data Bus
1	X	X	X	Not Selected	

The Main Status Register may be read by the processor at any time. When the processor wishes to read the Main Status Register, CS-NOT (Chip Select, pin 4) must be low (0). There are four signals which are gated with CS-NOT. These are:

- RD-NOT Read, Pin 2
- WR-NOT Write, Pin 3
- Ao Data/Status Register Select, Pin 5
- DB0-DB7 Data Bus, Pins 6 - 13

During the execution phase of any of the data transfer commands, it is <u>not</u> necessary to have CS-NOT=0 in order to transfer data between the processor and uPD765 However, during the command and result phase, it <u>is</u> necessary to have CS-NOT=0 for proper transfer between the processor and uPD765.

The Main Status Register is a single 8-bit register as shown in Table 2.

Table 2: Main Status Register Contents

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 Busy	D0B	Drive number 0 is in the Seek mode.
DB1	FDD 1 Busy	D1B	Drive number 1 is in the Seek mode.
DB2	FDD 2 Busy	D2B	Drive number 2 is in the Seek mode.
DB3	FDD 3 Busy	D3B	Drive number 3 is in the Seek mode.
DB4	FDC Busy	CB	When a command is in process. This bit goes high upon receipt of the first byte in the command phase and remains high until the last byte has been read out in the result phase.
DB5	Non-DMA mode	NDM	The FDC is in the non-DMA mode. This bit is set only during execution mode. When DB5 goes low, execution phase has ended.
DB6	Data Input/Output	DIO	Indicates direction of data transfer (i.e., command or result phase) between FDC and Data Register. DIO=1 when transfer is from 765 Data Register to the processor. and DIO=0 when transfer is from the processor to the 765 Data Register.
DB7	Request for Master	RQM	Indicates Data Register is ready to send data to or receive data from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor during the command and result phases.

Since the uPD765 operates asynchronously from the processor, it is necessary to read the Main Status Register before any command word is written or any result word is read from the uPD765. Bits 6 and 7 in the Main Status Register tell the direction in which the uPD765 is prepared to handle data on the Data Bus (DB6=DIO), and whether the FDC is ready to accept or output a data byte (DB7=RQM). Before each byte of the command phase is written into the uPD765, the Main Status Register must be read and the states of DB7 and DB6 must be RQM=1 and DIO=0. After the first byte in the command phase is output to the uPD765 (by WR-NOT=0), then RQM will go low (0). Depending upon the command selected, RQM may remain low for as long as 50 us or as little as 2 us. While RQM=0, the uPD765 is internally setting up the operation to be performed. After RQM goes high (1) the next byte in the command phase may be output to the uPD765. This "hand-shaking" (reading bits 6 and 7 in the Main Status Register before each byte is read or written from or to the uPD765) must be done during both command and result phases.

The timing diagrams in Figures 2 through 6 show the necessary event sequences in the command, execution and result phases of each of the instructions. It is important to note that six of the instructions do not have all three phases; Figures 5 and 6 show how to treat these special cases. The Seek and Recalibrate instructions do not have any result phase, and hence both must have a Sense Interrupt Status Command immediately following them.

The instruction set for the uPD765 is shown at the end of this Application Note. All bytes shown in the command phase of each instruction must be written into the uPD765 in the order shown (opcode first). In the result phase it is necessary to read all bytes (even if you don't need them) in order to fully terminate the instruction. All bytes must be sent in the command phase and all bytes read in the result phase. The sequence of these bytes is shown in the instruction table, and no "shortening" of any of the instructions is allowed.

After the Specify Command has been sent to the uPD765, the unit select lines US0 (pin 29) and US1 (pin 28) will automatically go into a scan mode. All four FDD's will be scanned by the uPD765 which will be looking for a change in the ready line from any of the drives. If the ready line from any of the drives should change state (such as due to the door opening or closing) then the uPD765 will generate an interrupt. When status register 0 (ST0) is read (after Sense Interrupt Status instruction has been issued) one will find that one of the drives will be in the "not ready" mode. This scanning of the ready line by the uPD765 occurs continuously between instructions, thus allowing the processor to know which drives are "off line".

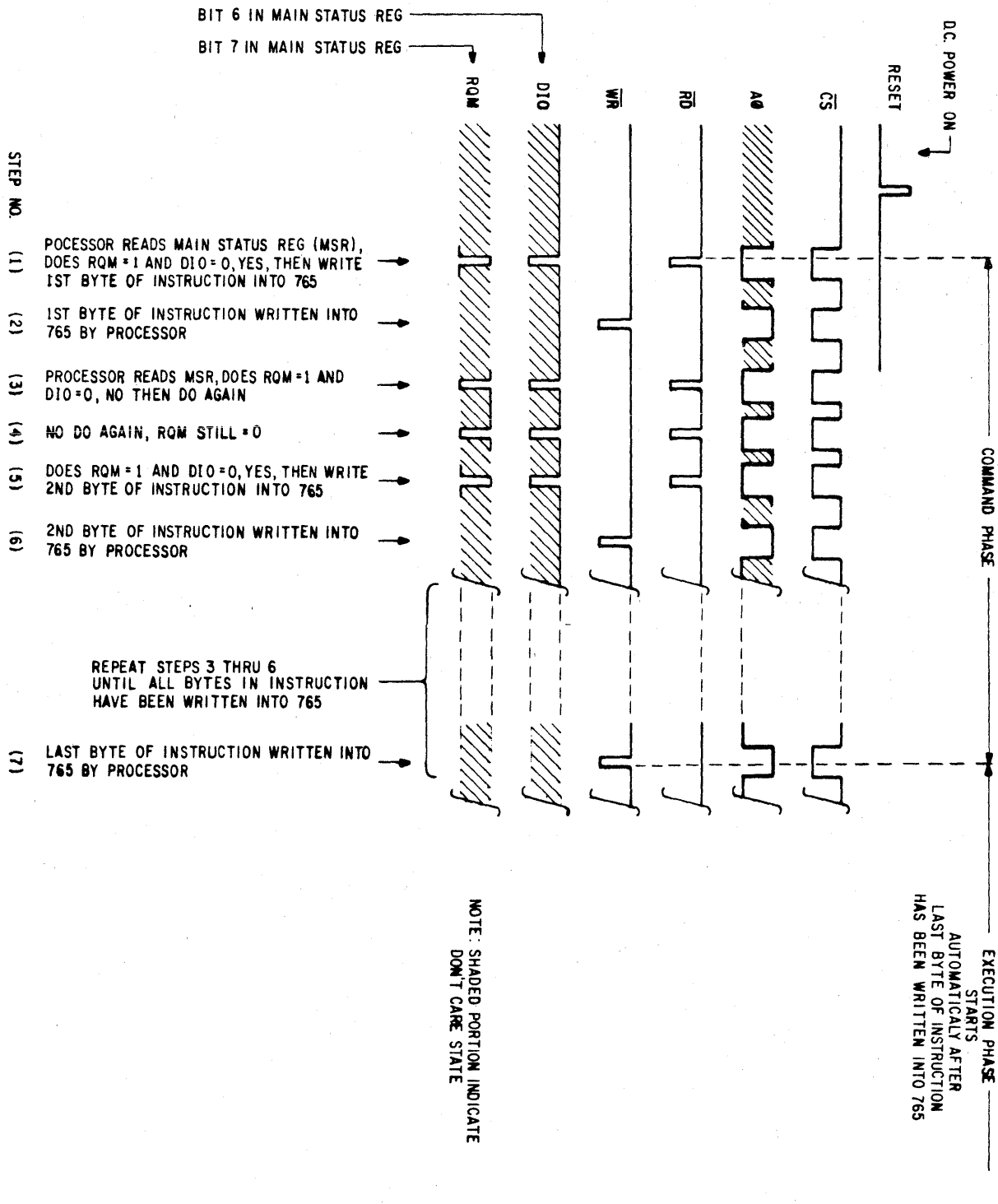


FIGURE 2
COMMAND PHASE
(SAME FOR ALL INSTRUCTIONS)

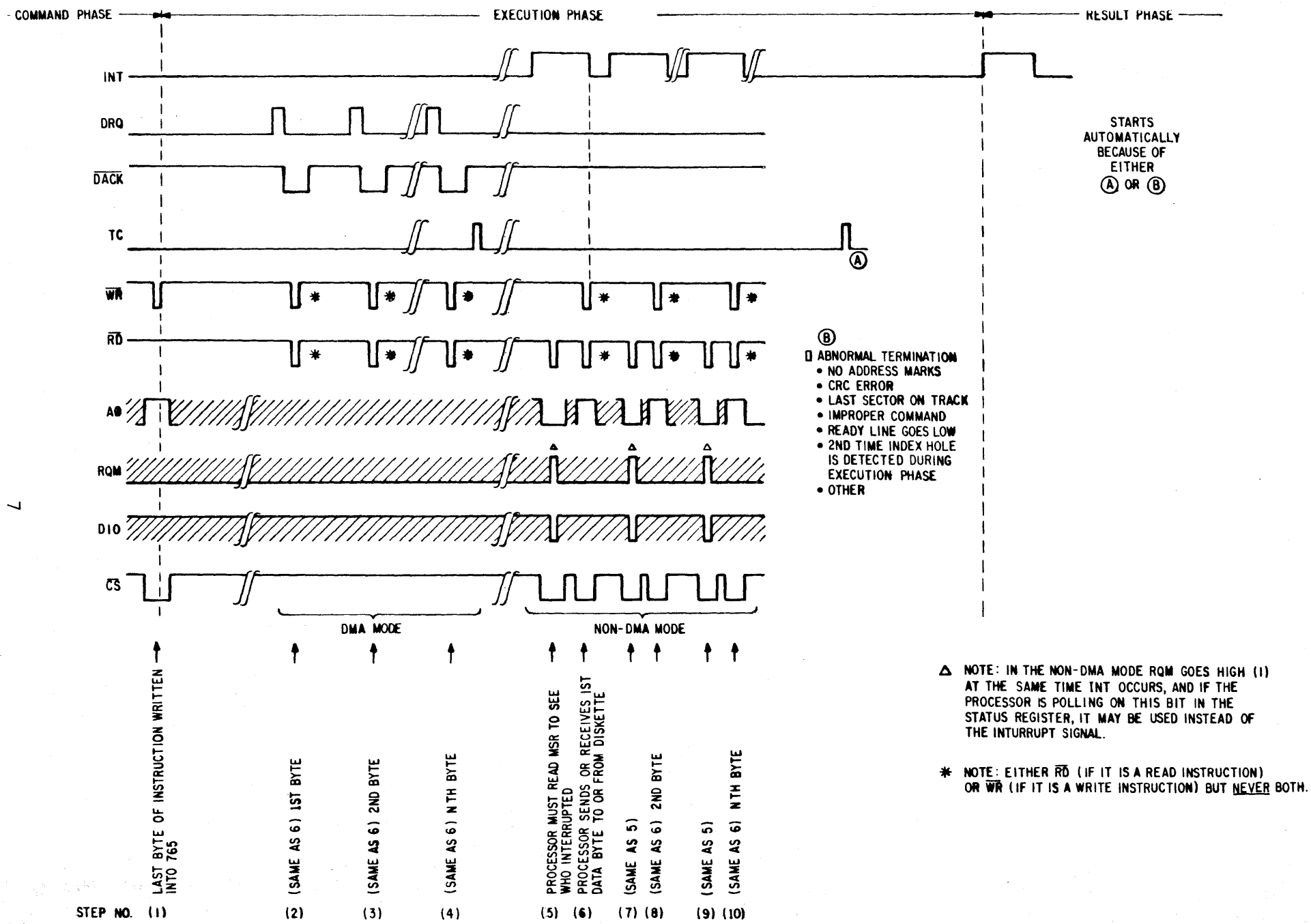


FIGURE 3
EXECUTION PHASE OF ALL READ OR WRITE INSTRUCTIONS

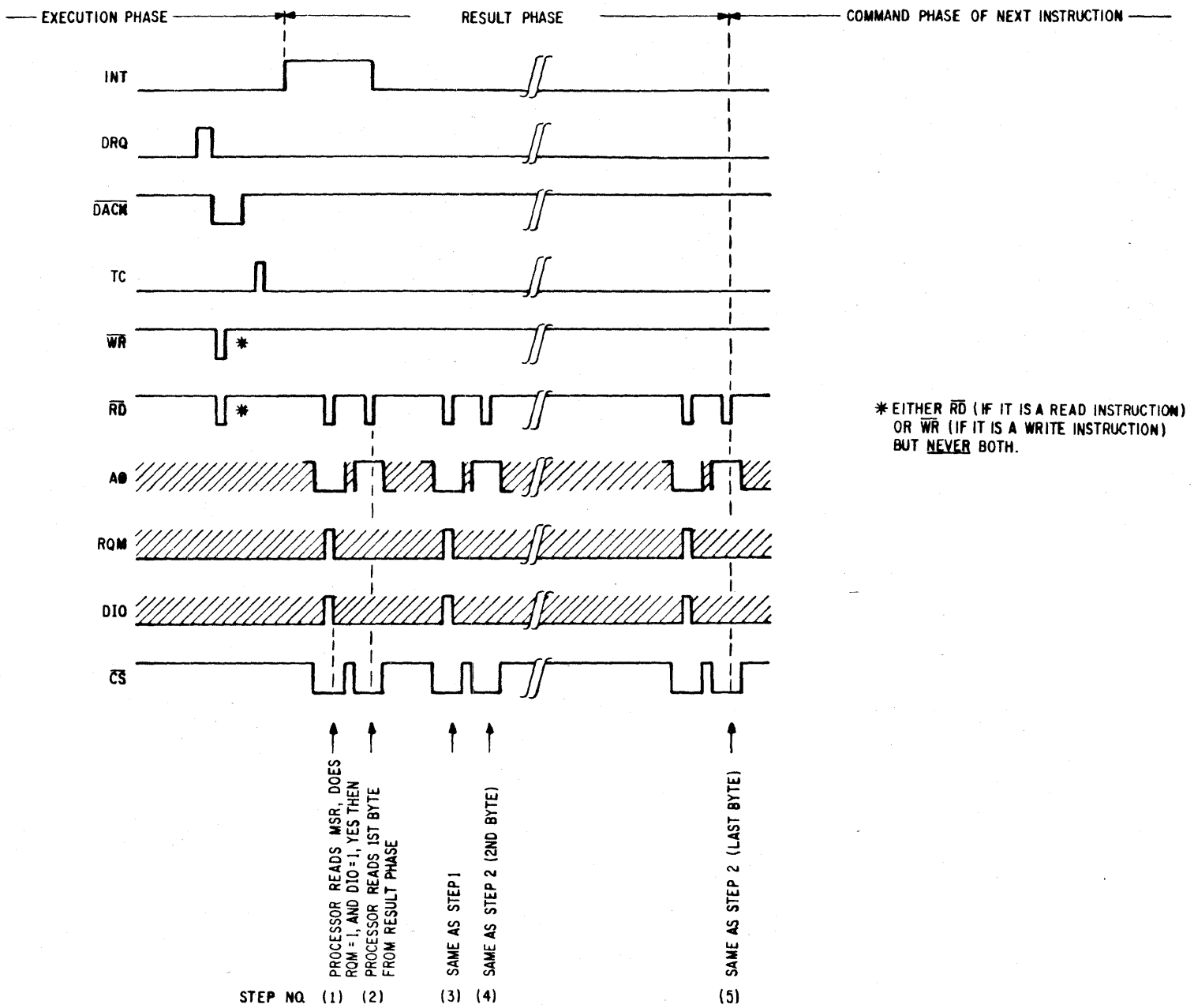


FIGURE 4
RESULT PHASE OF ALL READ OR WRITE INSTRUCTIONS

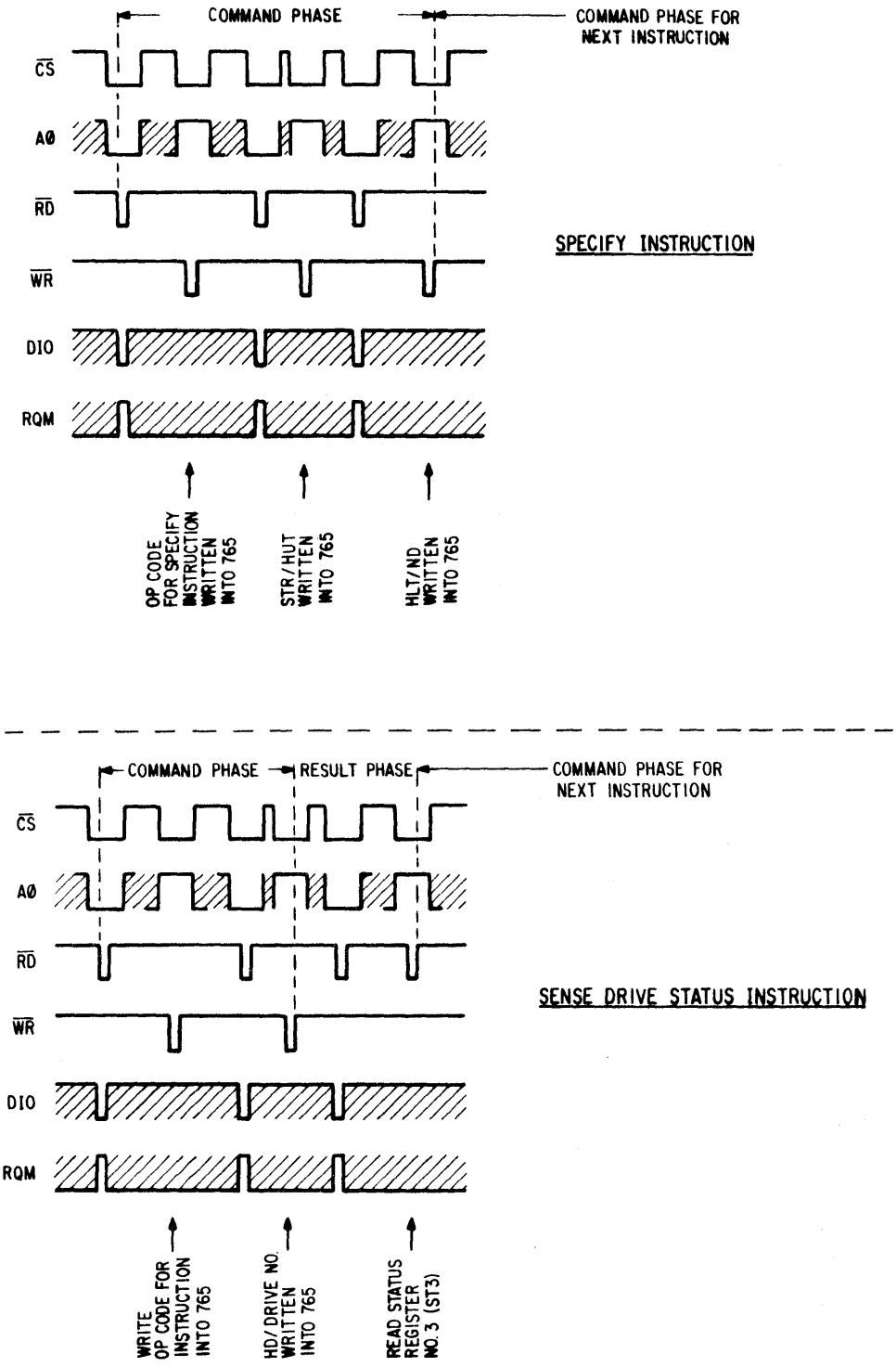
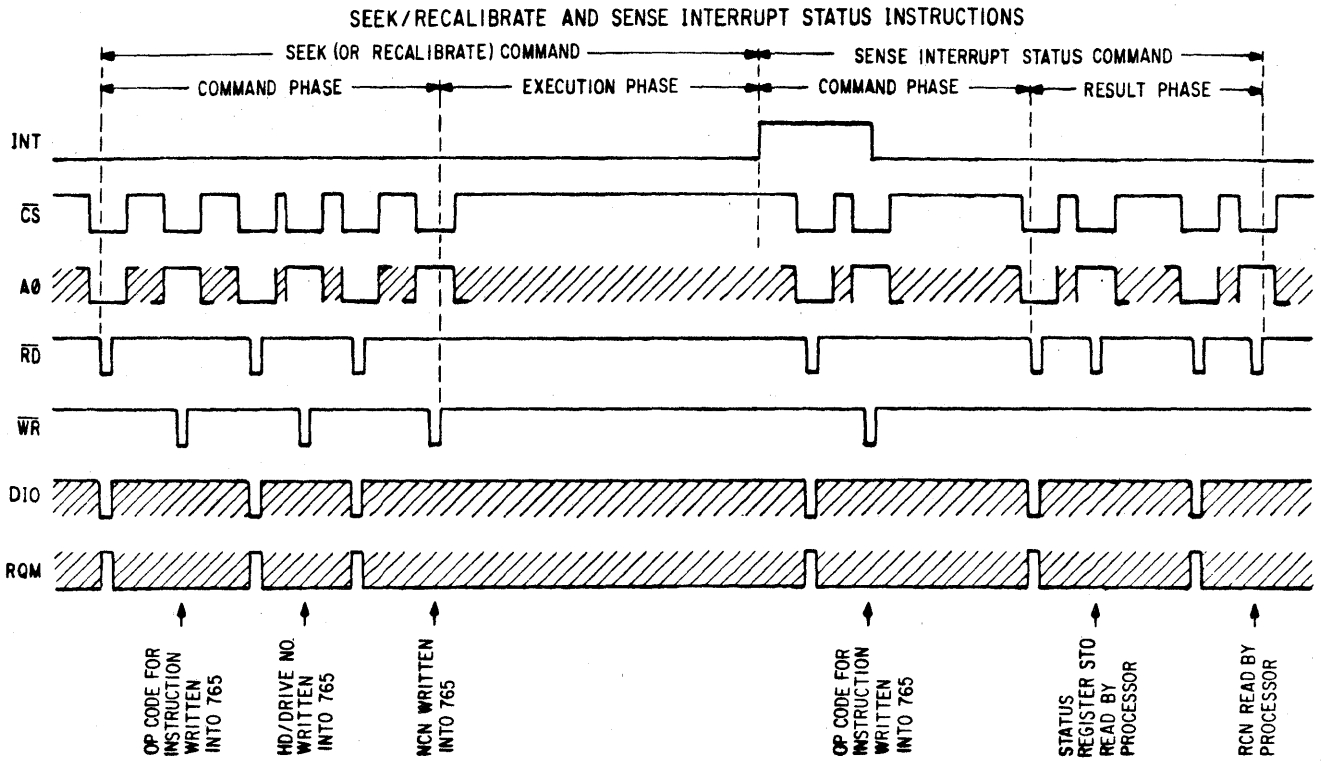


FIGURE 5
SPECIFY AND SENSE DRIVE STATUS INSTRUCTION



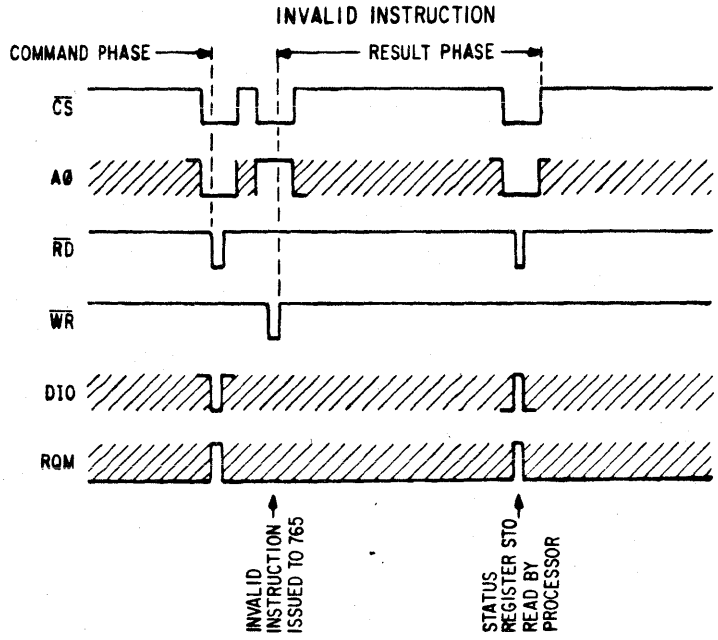


FIGURE 6
SEEK, RECALIBRATE, SENSE INTERRUPT STATUS AND INVALID INSTRUCTIONS

FLOPPY DISK DRIVE INTERFACE

The schematic (see Figure 18) shows how to interface the uPD765 to either standard or minifloppies. Several of the signals from the uPD765 interface directly to the floppy, while others are slightly more complex. A 74LS240 (U4) converts four multiplexed lines coming out of the uPD765 to eight lines, which are sent to the floppy. The RW-NOT/SEEK (pin 39) signal controls the multiplexer. When RW-NOT/SEEK is low (0) the uPD765 has a Read or Write operation in process and the signals Write Protect (pin 34), Fault (pin 33), Fault Reset (pin 37) and Low Current (pin 38) are active coming out of the uPD765. However, when RW-NOT/SEEK is high (1), a Seek operation is in process and 2-Sided (pin 34), Track 0 (pin 33), Step (pin 37) and Direction (pin 38) are active.

If only two floppy disk drives are to be used, then no further decoding is necessary of the Unit Select 0 (pin 29) and Unit Select 1 (pin 28) lines. These lines, as their names imply, perform the drive selection function. If four drives are used then a simple binary decoder, such as a 74LS139 (U5) will decode these two lines to four lines. The uPD765 is set up internally to handle four drives; there are four track counters inside, so that the uPD765 knows at all times the positions of the R/W heads on all four drives.

The algorithm for precompensation is computed within the 765 (Single Level Pre-Compensation). However, the amount of precompensation is controlled in external hardware. A shift register and a four-to-one decoder are all that are required externally to perform precompensation.

U6 (74LS175) is configured as a 4-bit shift register and half of U7 (74LS153) performs the four-to-one decoding. The shift register generates the Early, Normal and Late signals. Pre-Shift 0 (pin 32) and Pre-Shift 1 (pin 31) select which of the above signals are sent to the drive. The signal WR Data (Pin 30) is uncompensated Write Data. The amount of precompensation is controlled by the clock signal to the shift register U6. An 8 MHz clock is shown which would result in 125 ns of precompensation. (Consult your drive manufacturer for the proper value. A typical range for most standard floppy disk drives is 125 ns to 250 ns.)

The schematic in Figure 18 shows most of the configurations which are possible with both standard and minifloppies. However, it is highly unlikely that anyone would want all the optional features shown. As a result one should read the notes at the bottom of the schematic carefully and eliminate the necessary IC's before starting to build this controller.

Figures 7 through 11 show the sequence of events which occur at the uPD765/drive interface for each of the instructions. Detailed timing information for each of these signals is provided in the uPD765 Data Sheet.

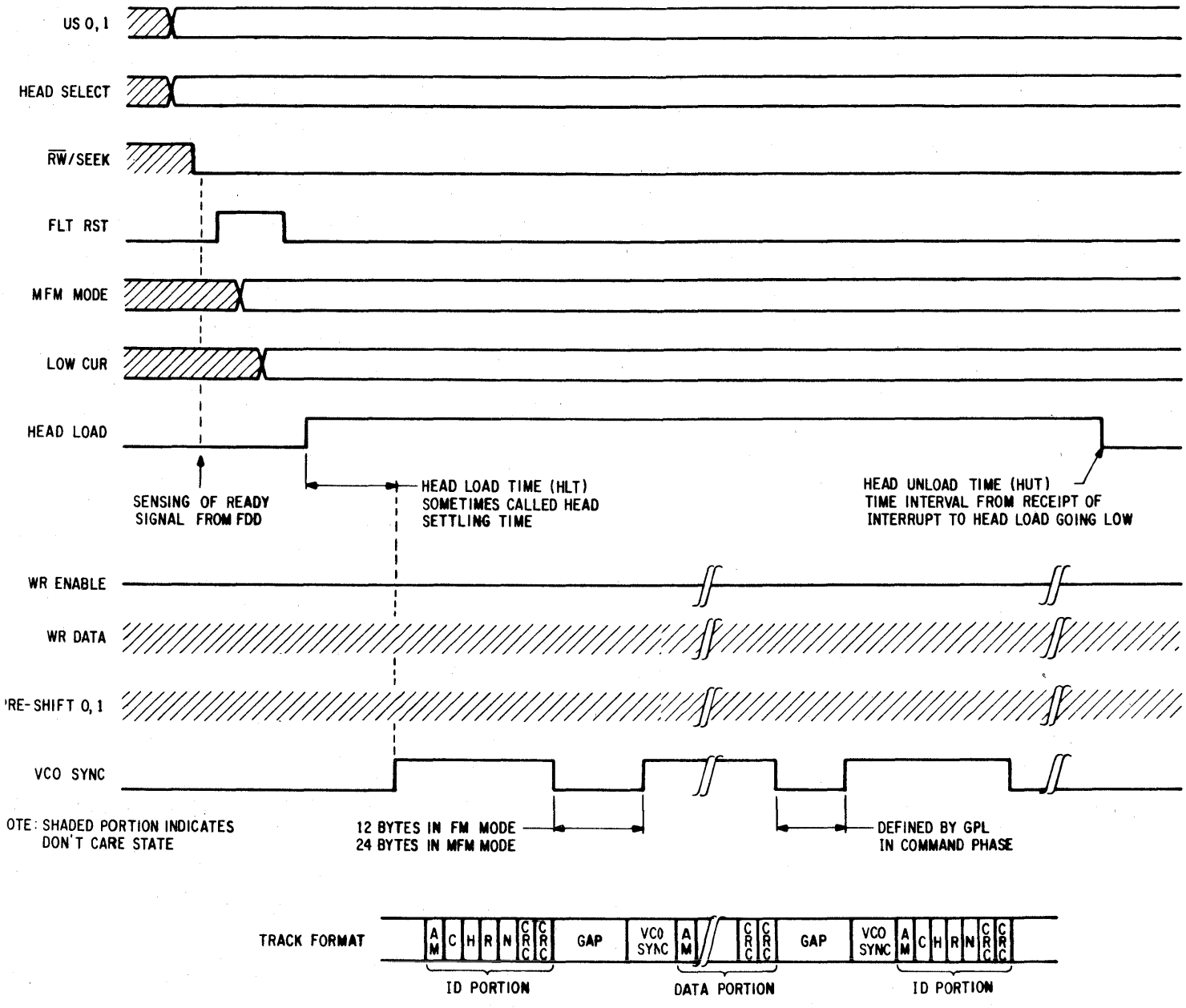


FIGURE 7
TIMING AT FDD INTERFACE
READ DATA, READ DELETED DATA, READ A TRACK, SCAN, AND READ ID INSTRUCTIONS

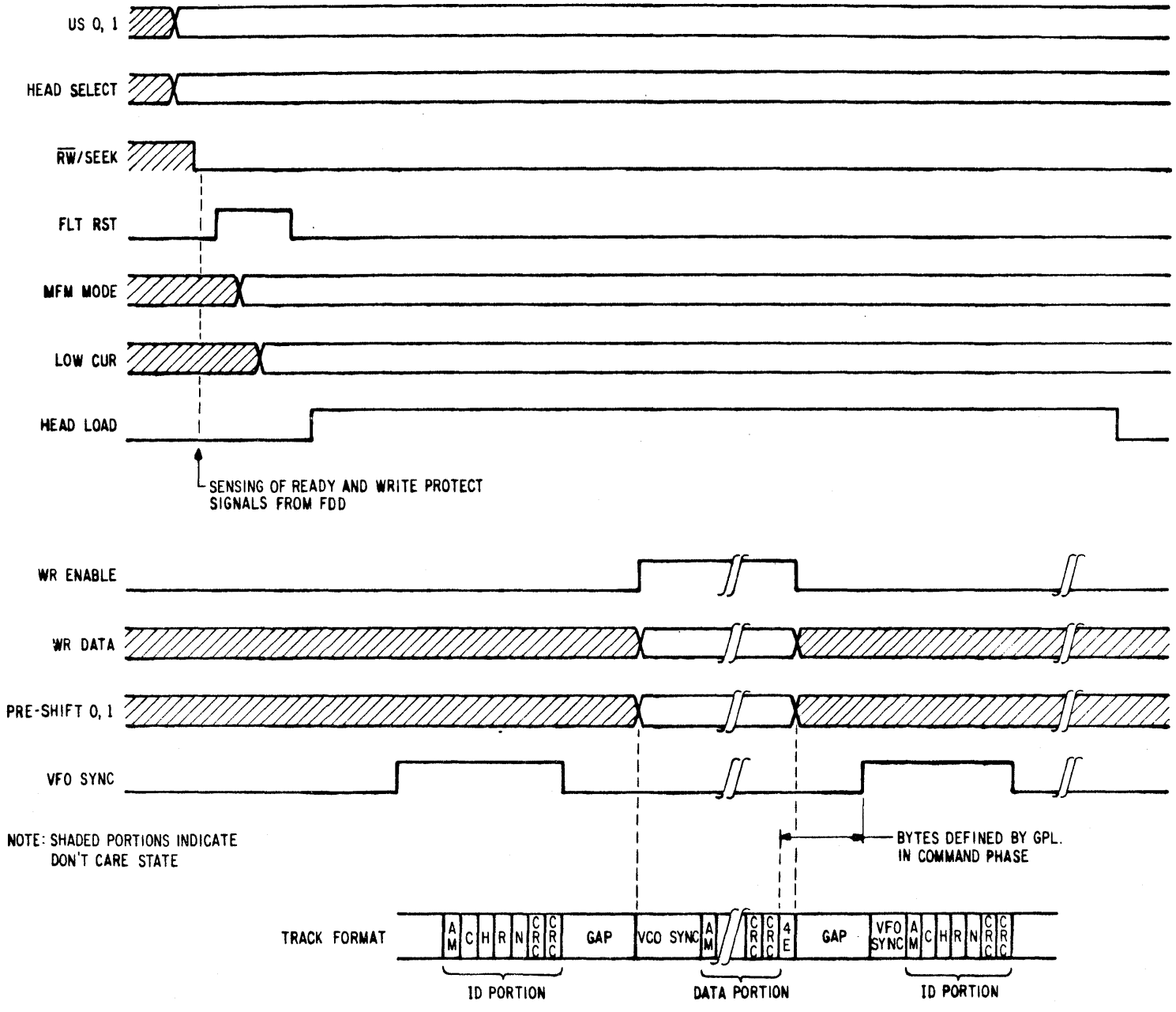


FIGURE 8
TIMING AT FDD INTERFACE
WRITE DATA AND WRITE DELETED DATA INSTRUCTIONS

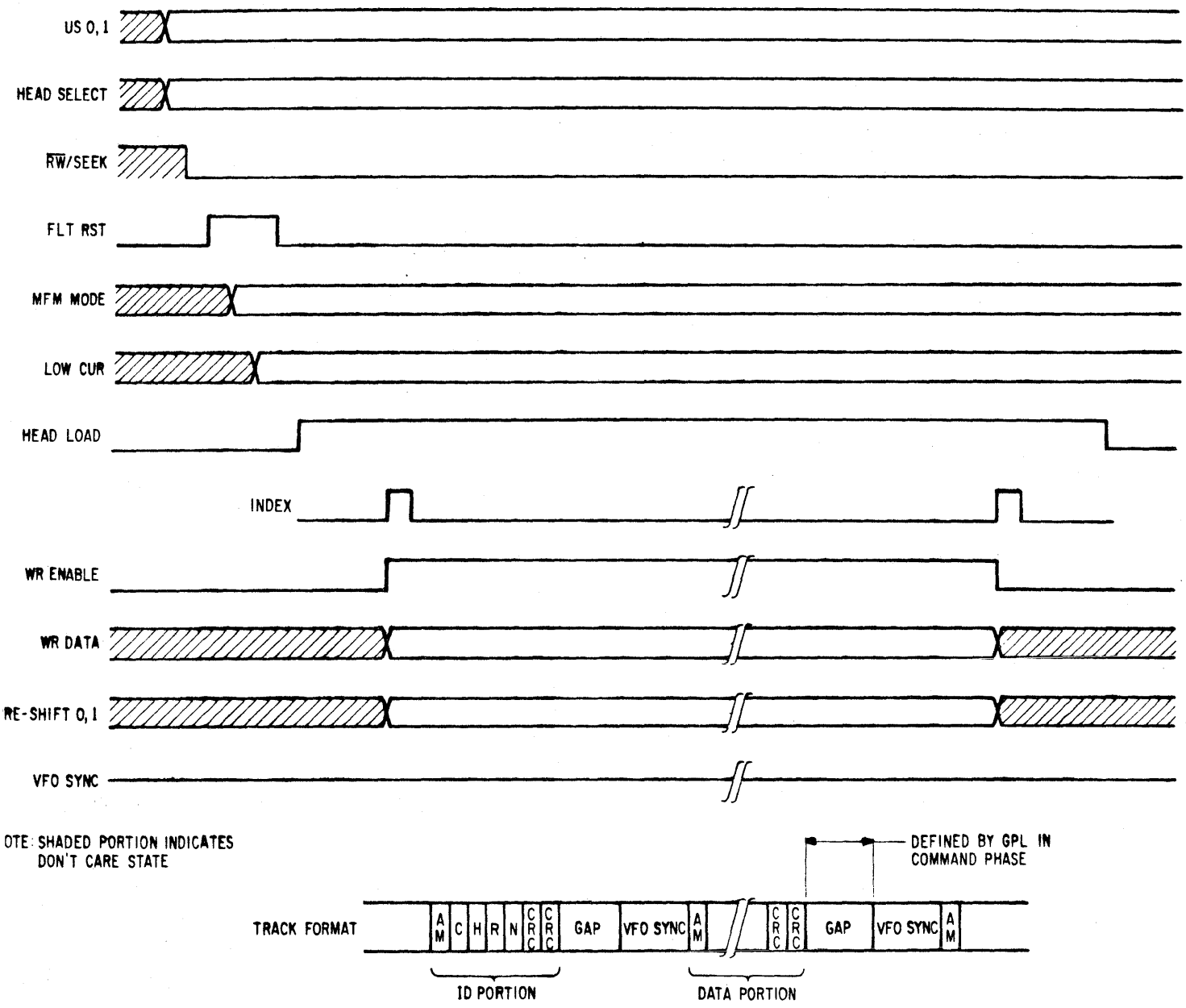


FIGURE 9
TIMING AT FDD INTERFACE
FORMAT A TRACK INSTRUCTION

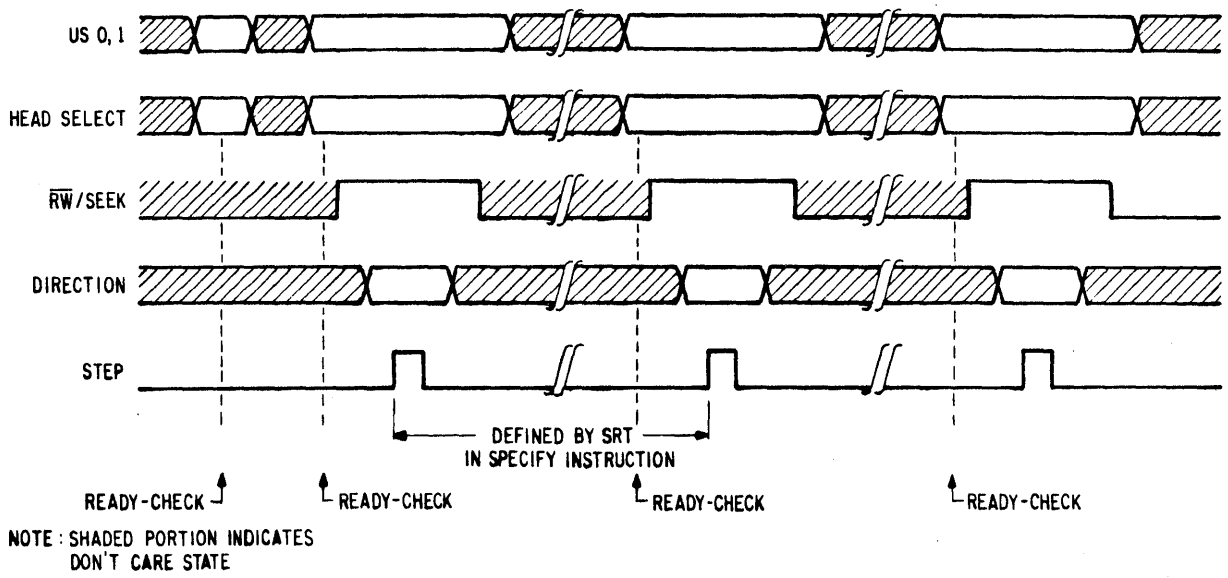


FIGURE 10
TIMING AT FDD INTERFACE
SEEK AND RECALIBRATE INSTRUCTION

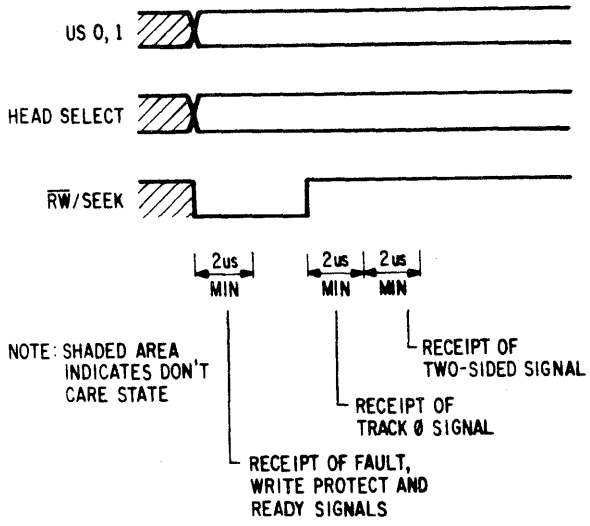


FIGURE 11
TIMING AT FDD INTERFACE
SENSE DEVICE STATUS INSTRUCTION

DATA RECOVERY CIRCUITS

Single-density recording did not require anything more elaborate than a one-shot circuit for data separation and, as a result, data recovery from the floppy disk was rather easy. But, double-density data exhibits a greater percentage of peak-shift (time distortions during play-back from magnetic recordings) per cell, and hence requires a more sophisticated data recovery circuit. The uPD765 provides two signals which greatly simplify this normally sticky problem:

(1) VCO Sync (pin 24) This signal holds the VCO in the PLL circuit at center frequency.

(2) MFM Mode (pin 26) This signal tells the PLL whether the uPD765 is programmed for FM or MFM operation.

In the Read mode, the VCO Sync signal goes true after the R/W head has been loaded and the head settling time (head load time) has elapsed. (See bottom of Figure 7.) The VCO Sync goes false between the ID Field and the Data Field; and after the Data Field. This is done to blank out discontinuities which appear in these gaps when the Write current is turned on and off. When VCO Sync is true, valid data is coming off the diskette and the data recovery circuit does not have to be configured to accommodate any abnormal conditions.

The MFM mode signal is high (logic 1) when the unit has been programmed to receive MFM (double density) data and is low (logic 0) for FM (single density) data. This signal allows the data recovery circuit to switch between single and double density modes of operation.

The uPD765 requires a Data Window signal (pin 22) which brackets the data coming from the drive. Figure 12 shows the timing relationship between these signals. Note how the Data Window brackets both the beginning and center of the cell. Also note that either polarity Data Window signal is acceptable to the uPD765. When single density (FM) data is to be processed, times shown in Figure 12 must be multiplied by two. For minifloppies the times shown in Figure 12 must be multiplied by two (for double density minifloppies) and by four (for single density minifloppies).

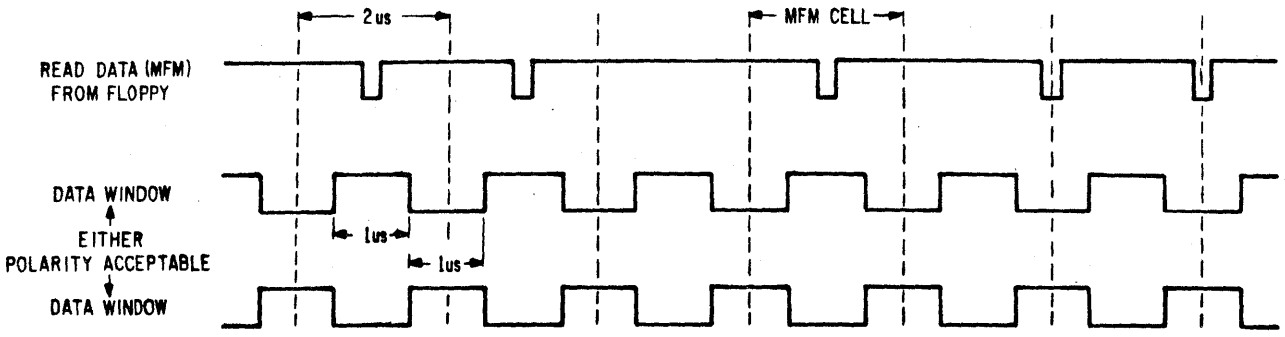


FIGURE 12
DATA WINDOW SIGNAL REQUIRED BY uPD765

A convenient way to generate this Data Window signal is with a Phase Locked Loop (PLL). The PLL tracks the playback signal from the drive and performs the function of an adaptive low-pass filter. Many excellent technical articles have been written on the virtues of the PLL in this application, and it is only necessary to say that the PLL will work very well for data recovery of floppy disk data if two key factors are remembered:

(1) The data must be periodic in nature. (FM and MFM data exhibit this characteristic if they are adequately pre- or post-compensated.)

(2) Adequate allowances must be made for both the VCO Sync period and the discontinuities on the diskette which result when the Write current was turned on or off.

PHASE LOCKED LOOP DATA RECOVERY CIRCUIT

Figure 13 shows a design for a phase locked loop data recovery circuit interfaced to the uPD765. The circuit operates from a single +5V power supply and is implemented primarily with digital I.C.'s. The only analog circuitry is the low pass filter circuit (R4, R7, R8 and C1) and two transistors (Q1 and Q2) which interface to it. I.C.'s U1 and U2 are the heart of the PLL circuit; these generate two 1 MHz signals fr (reference) and fo (signal). The two counter outputs U1-12 and U2-12 are phase locked after acquisition and lock have occurred in the loop. Counter U1 is a free-running counter and simply counts down the VCO output (U5-7). Counter U2 is pre-loaded to all zeros every time a flux reversal is read from the floppy disk drive. U8-5 and U8-8 perform the function of synchronizing the playback data from the drive to the VCO output, as well as generating the load pulse to counter U2-9.

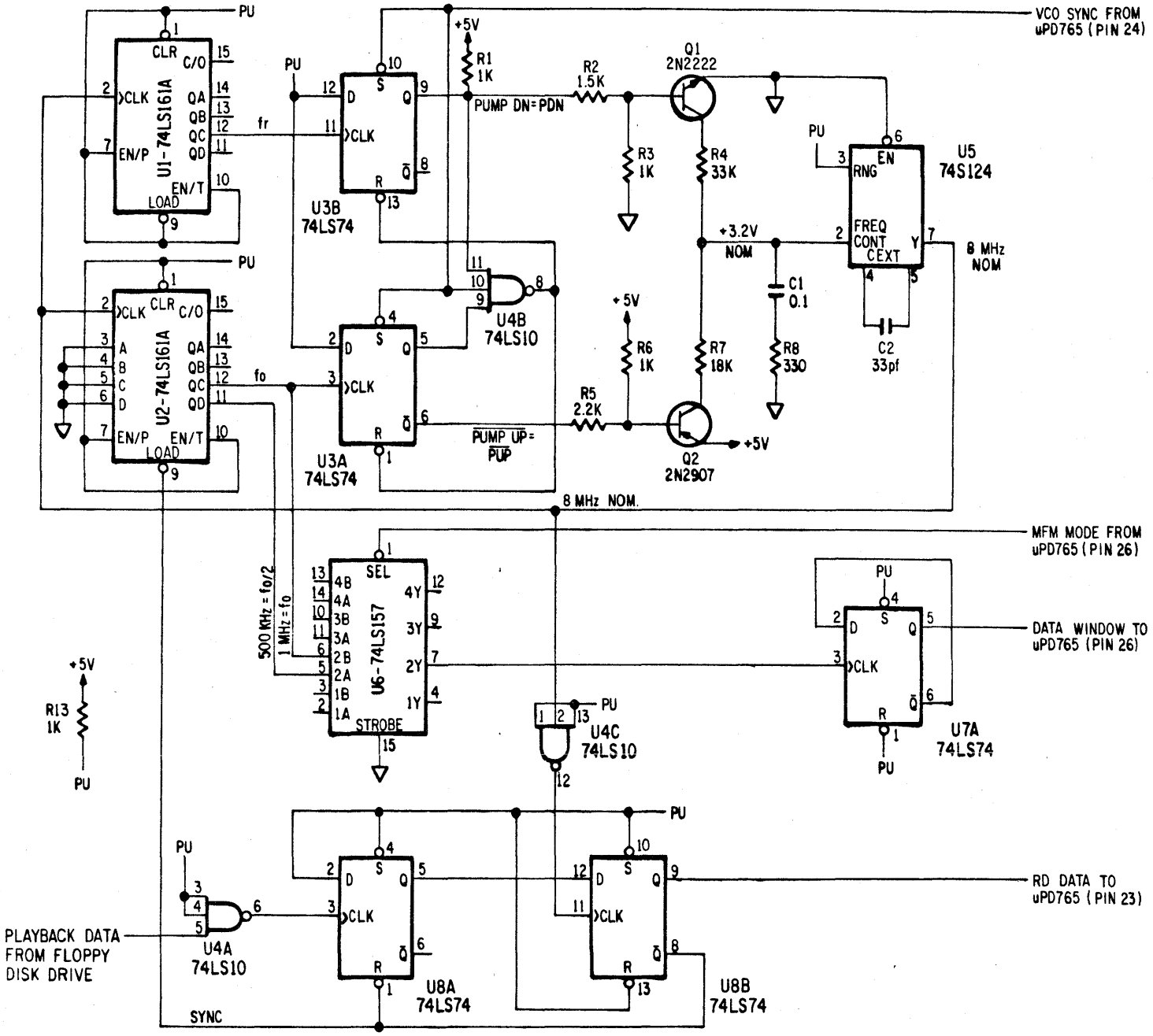
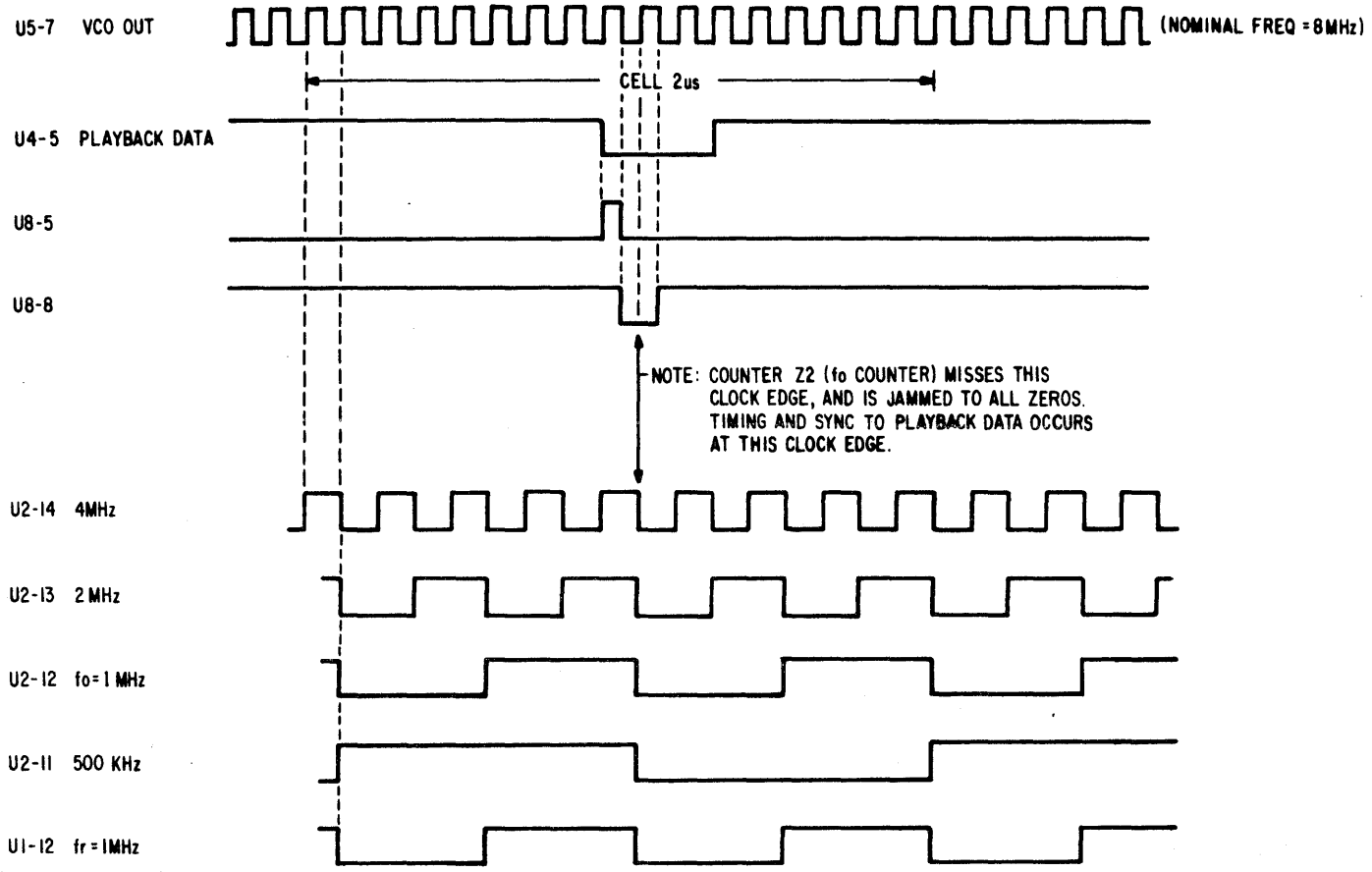


FIGURE 13
PHASE LOCKED LOOP FOR FM/MFM ENCODED DATA

Figures 14 and 15 show the timing relationship between these signals under both ideal and worst-case bit patterns. Note in Figure 15 how the RD Data pulse moves around within the Data Window under worst-case peak shift conditions. With this circuit, peak-shifts of up to 375 ns (500 ns theoretical maximum) may be tolerated in MFM encoded data before read errors will be encountered.



NOTE: fr AND fo ARE PHASE LOCKED AFTER LOOP HAS ACQUIRED AND LOCKED.

FIGURE 14
SYNCRONIZATION OF fo COUNTER WITH FDD DATA

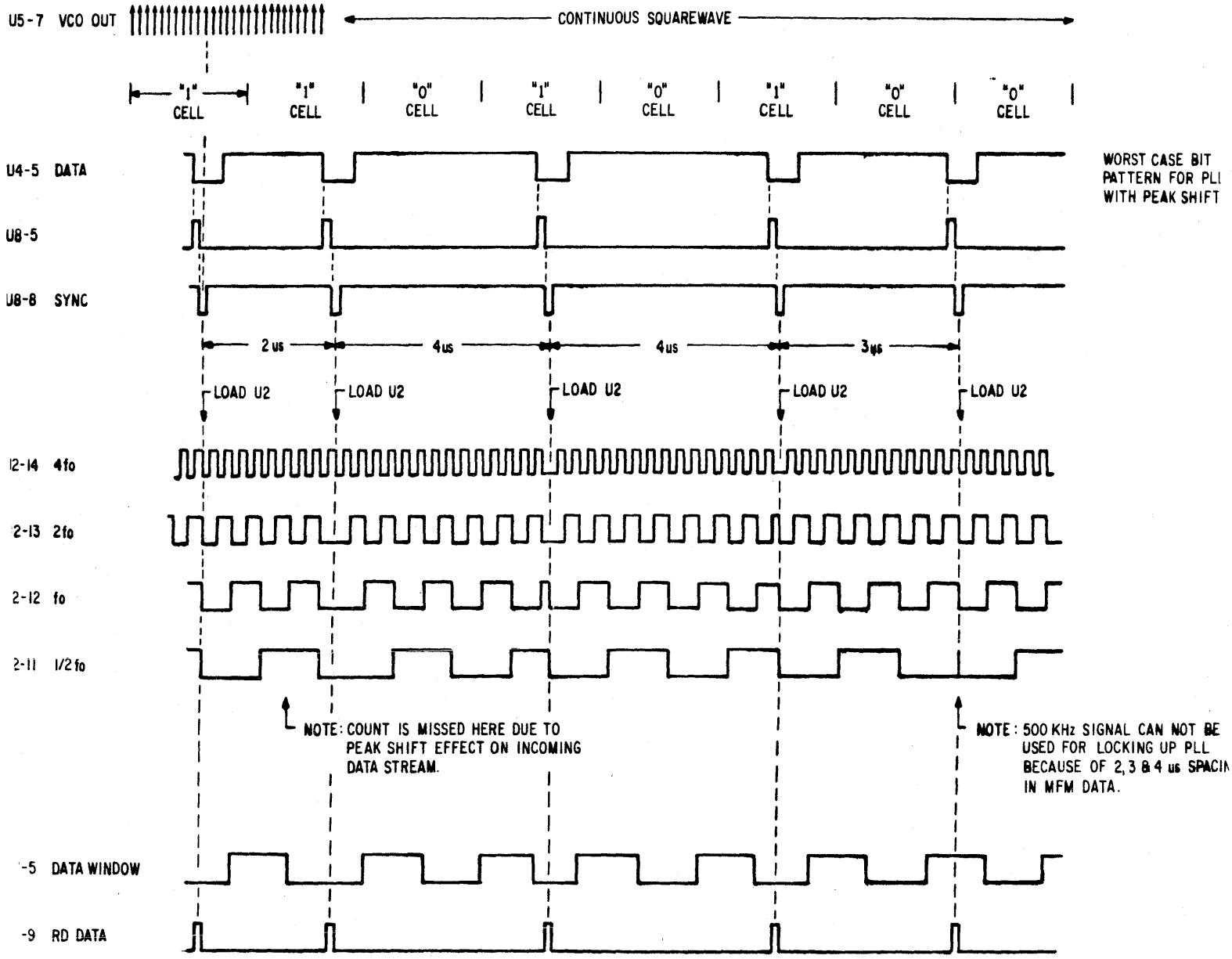
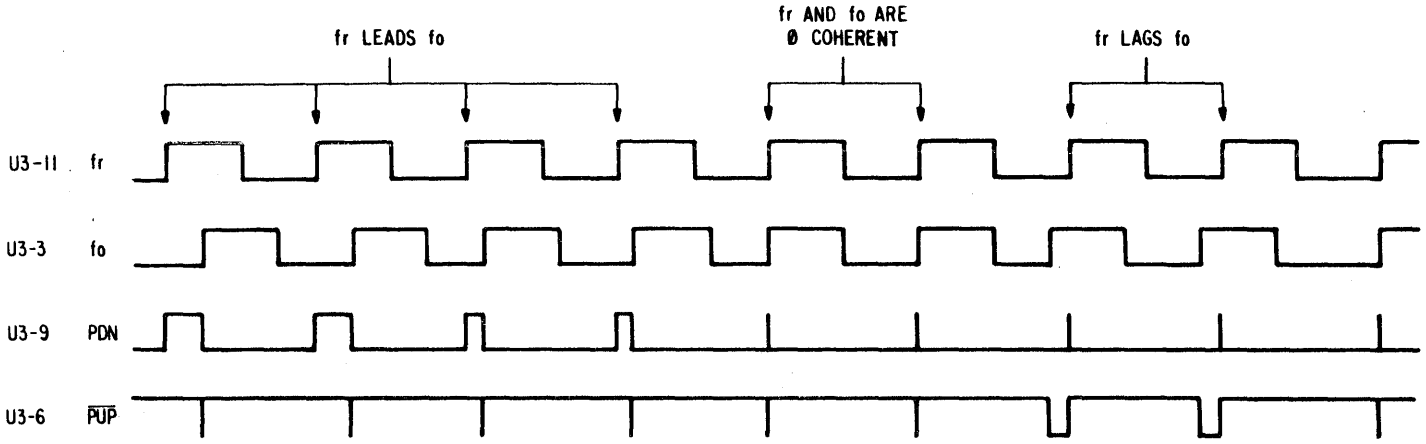


FIGURE 15
fo COUNTER SYNC WITH PEAK SHIFT

U3-5, U3-9 and U4-8 form a digital phase comparator circuit. U3-5 and U3-9 toggle to a high (1) state whenever a positive edge is generated by U2-12 or U1-12 respectively. When U3-5 and U3-9 are both high (1), U4-8 goes low and resets both flip-flops to their low (0) state, and another cycle begins. The amount of time which U3-5 remains high (1) compared to U3-9 determines whether transistor Q2 remains on longer than Q1. Transistor Q2 charges C1, while Q1 discharges it. If Q2 remains on longer than Q1, there will be a net increase in the charge on (and hence voltage across) C1. As the voltage across C1 increases, the frequency out of U5-7 will also increase. This increase in the VCO frequency will cause U1-12 to reach a positive transition sooner than U2-12, which will decrease the voltage across C1 (negative feedback). R7 and C1 determine the charging timing constant, while R4 and C1 determine the discharging timing constant. R8 is a damping resistor (an essential component!) which minimizes overshoots and undershoots. Figure 16 shows the operation of the phase comparator under various conditions of fr and fo.



NOTE: PDN CONTROLS Q1, AND PUP CONTROLS Q2, WHICH DISCHARGE AND CHARGE CAPACTOR C1. RESISTOR CAPACTOR NETWORK R4, R7, R8 AND C1 CHANGE THE PULSE WIDTH MODULATED SIGNALS PDN AND PUP (WHICH ARE A DIRECT FUNCTION OF PHASE DIFFERENCES BETWEEN fr AND fo), INTO A D.C. LEVEL, AS SEEN AT U5-2. THE LEVEL AT U5-2 IS NORMINALLY +3.25V.

FIGURE 16
PHASE COMPARATOR

Careful note should be made of the functions of VCO Sync (output from uPD765, pin 24). It is connected to U3-10, U3-4 and U4-10, and when VCO Sync is low (0), both transistors Q1 and Q2 are held in the ON state. This causes the voltage across C1 to be approximately +3.25V and the VCO output U5-7 to be 8 MHz. R4 and R7 should be adjusted when VCO Sync is low so that the frequency of the signal at U6-7 does in fact equal exactly 8 MHz. This effectively clamps the VCO output to mid-range and inhibits it from being affected by noise (head not lowered) or erroneous signals (write current glitches). When VCO Sync goes high, it can be assumed that valid data is being received from the drive. The

result is that the loop's response is very clean, acquisition and lock occur in a very orderly manner, and one does not have to worry about spurious or false lock conditions.

Using the MFM mode signal (pin 26), the uPD765 selects either 500 KHz or 1 MHz for input to U7-3. For single-density data 500 KHz is selected, while double-density data requires 1 MHz. U7-5 is simply a flip-flop which toggles at the 1/4 and 3/4 duration points in a data cell, thereby generating the Data Window signal shown in Figure 12.

SYNCHRONOUS COUNTER DATA RECOVERY CIRCUIT

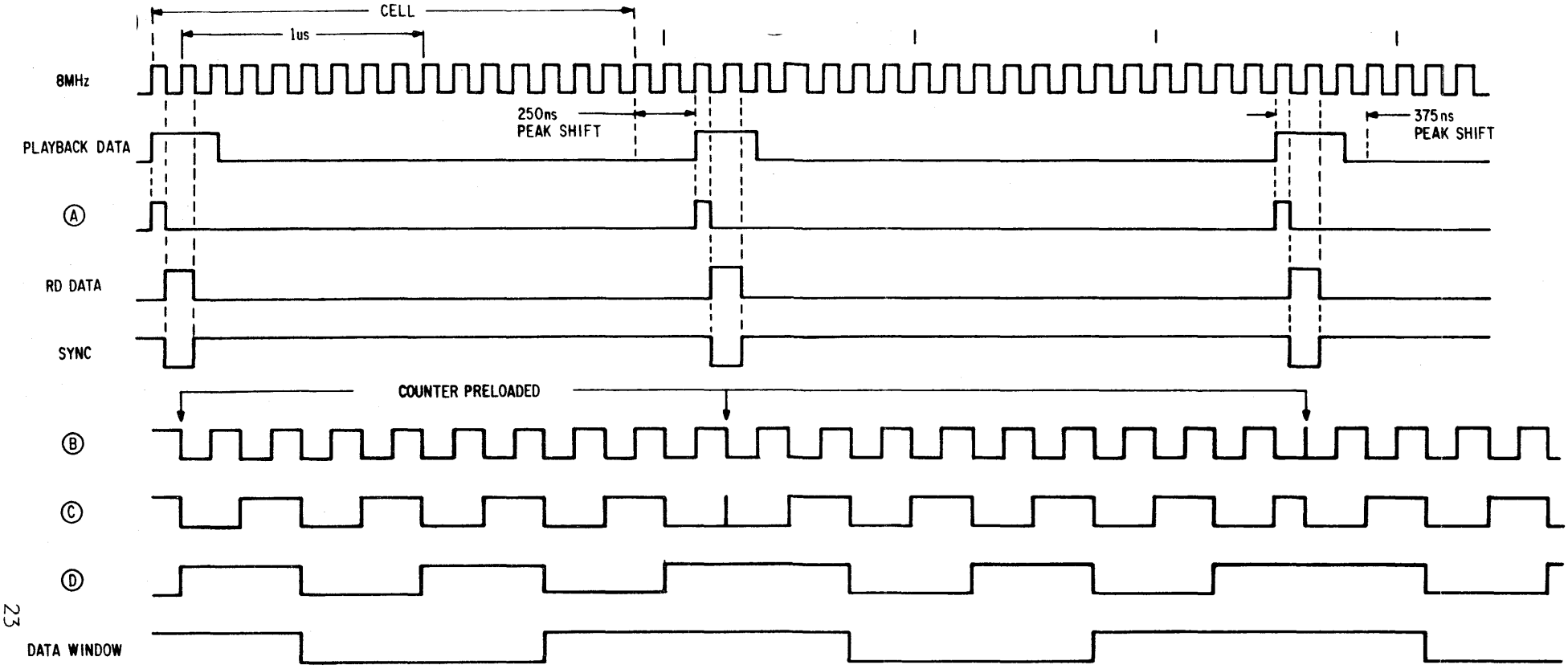
Figure 17 shows an alternate solution to the phase locked loop; it is simply a synchronous counter circuit. The synchronous counter circuit consists of a binary counter which is preloaded with a fixed value on each Read pulse from the drive. The counter's output is the Data Window signal to the uPD765. The two flip-flops in Z1 merely synchronize the data from the drive to the 8 MHz clock, and set up the Sync pulse which will preload the counter (Z2). Z1-8 controls the width of the Sync pulse so that it overlaps only one positive edge of the 8 MHz clock. The positive edge of the 8 MHz clock which appears in the Sync pulse window is the one which preloads the counter. Note how Z2-11 is fed back to Z2-6 to ensure that, regardless of the pulse spacing (2, 3 or 4 us), the polarity of the Data Window is never reversed during a data stream.

The VCO Sync signal from the uPD765 (pin 24) performs the same function as it did for the PLL design. That is, it inhibits the RD Data and Data Window signals from being generated until valid information is detected from the drive. It also masks out write current glitches which would otherwise appear on each side of the data field. In fact, this simple data recovery circuit would not work reliably if it were not for the VCO Sync signal.

By switching the 8 MHz clock to 4 MHz, the synchronous counter circuit can be made to operate at single-density rates. Minifloppies can be used with this design if the clock rate is divided in half again (to 2 MHz). The MFM mode signal (pin 26) from the uPD765 should be used to switch the clock rate to the data recovery circuit.

The synchronous counter data recovery circuit is a much simpler design than the PLL, and works almost as well. Both designs, however, require that the data from the drive be adequately pre- or post-compensated so that peak-shifts are kept well below 500 ns. The PLL does offer some very distinct advantages over the synchronous counter approach. Because of the PLL's feedback and low-pass filter characteristics, it adapts to the drive's pulse stream; thus the VCO's center frequency is always optimized for the data. As a result, the Data Window is able to handle early or late peak-shifts equally as well with no bias. Also speed (rpm of the diskette) variations and track-to-track variations (pulse crowding on inner tracks) can be handled somewhat better with a PLL.

The two data recovery circuits discussed above should be used as guides in helping you design your own circuit. These designs were presented merely to help you understand the uPD765, and do not in any sense represent the only approaches possible.



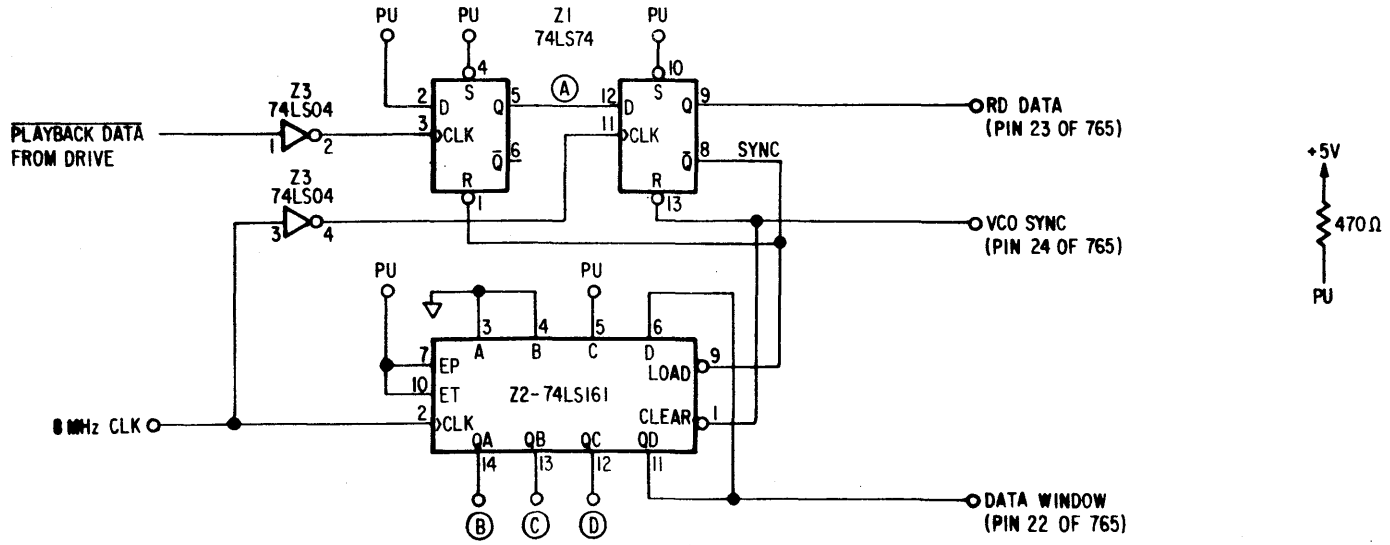
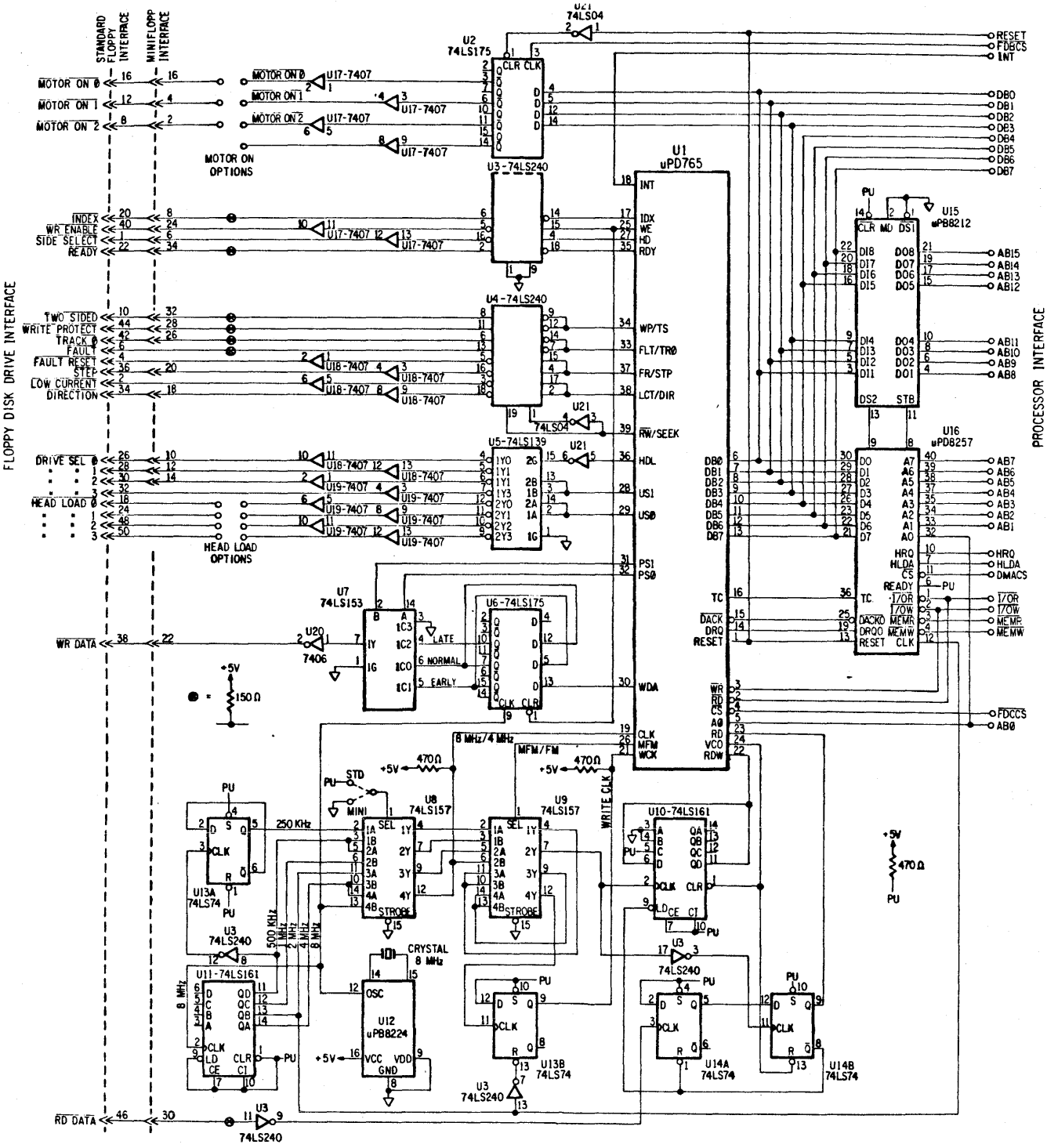


FIGURE 17
SYNCRONOUS COUNTER DATA RECOVERY CIRCUIT



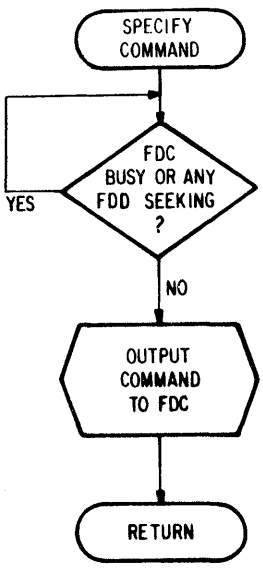
OPTIONAL CONFIGURATIONS

1. IF EITHER MINIFLOPPIES OR STANDARD FLOPPIES ARE TO BE USED, BUT NOT BOTH, THEN REMOVE U8 AND REPLACE WITH 4 JUMPERS.
2. IF ONLY ONE HEAD LOAD COMMAND IS NEEDED, THEN REPLACE U21-6 WITH A 7406 (U20) AND REMOVE 2/3 OF U19 (U19-6,8,10 & 12).
3. IF ONLY SINGLE DENSITY OR DOUBLE DENSITY IS REQUIRED BUT NOT BOTH, THEN REMOVE U9 AND REPLACE WITH 4 JUMPERS.
4. IF ONLY STANDARD FLOPPIES ARE USED, THEN REMOVE U2, 2/3 OF U17 (U17-2,4,6 & 8), AND 1/2 OF U13 (U13A).
5. IF EXTERNAL 8 MHz CLOCK IS AVAILABLE, THEN REMOVE U12.
6. IF THE 765 IS OPERATED IN AN INTERRUPT DRIVEN MODE (NON DMA), THEN REMOVE U15 AND U16.
7. IF PRE-COMPENSATION IS NOT REQUIRED, THEN REMOVE U6 AND U7.

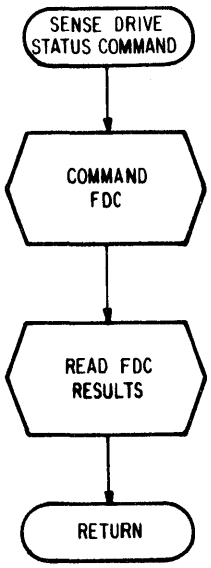
FIGURE 18
FLOPPY DISK CONTROLLER SCHEMATIC

GENERAL FLOW CHART OF uPD765C

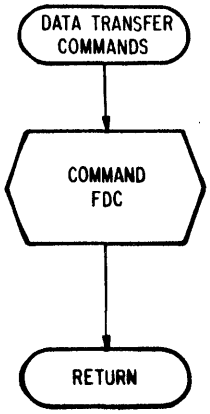
Figure 19 shows a very generalized program flow for the uPD765 command phase. It breaks down the fifteen commands into Specify, Sense Drive Status, and twelve others. (The fifteenth, Sense Interrupt Status, is only used in response to an interrupt.) The Specify command sets up three internal timers and establishes whether DMA operation is to be performed, and is typically only performed after power on. It has neither an execution phase nor a result phase. The Sense Drive Status command can be performed between data transfer commands to obtain the status of the selected drive. The status of the drive is available immediately and thus there is no execution phase. The twelve other commands: Read Data, Read Deleted Data, Write Data, Write Deleted Data, Read a Track, Read ID, Format a Track, Scan Equal, Scan Low or Equal, Scan High or Equal, Recalibrate, Seek, all involve the disk drive and usually take many milliseconds to be performed. Since it is inefficient to tie up the processor for a long time, these data transfer commands may be performed without need of the processor (DMA mode only) until the execution phase is complete. At the end of the execution phase the uPD765 interrupts the processor to signal the completion of the command.



NOTE : NO EXECUTION PHASE
NO RESULT PHASE



NOTE: NO EXECUTION PHASE



NOTE: FDC AUTOMATICALLY ENTERS EXECUTION PHASE UPON COMPLETION OF COMMAND PHASE. RECEIPT OF EITHER DMA REQUESTS OR INTERRUPT SIGNALS INDICATES BEGINING OF EXECUTION PHASE.

FIGURE 19
GENERALIZED COMMAND PHASE FLOW CHART

Figure 20 shows the detailed steps of the command phase. The first entry point labeled "Command FDC" checks the status register to see if the uPD765 is busy, or the disk drive is busy. The second entry point "Output Command to FDC" is used when it is known that the uPD765 is ready for a new command.

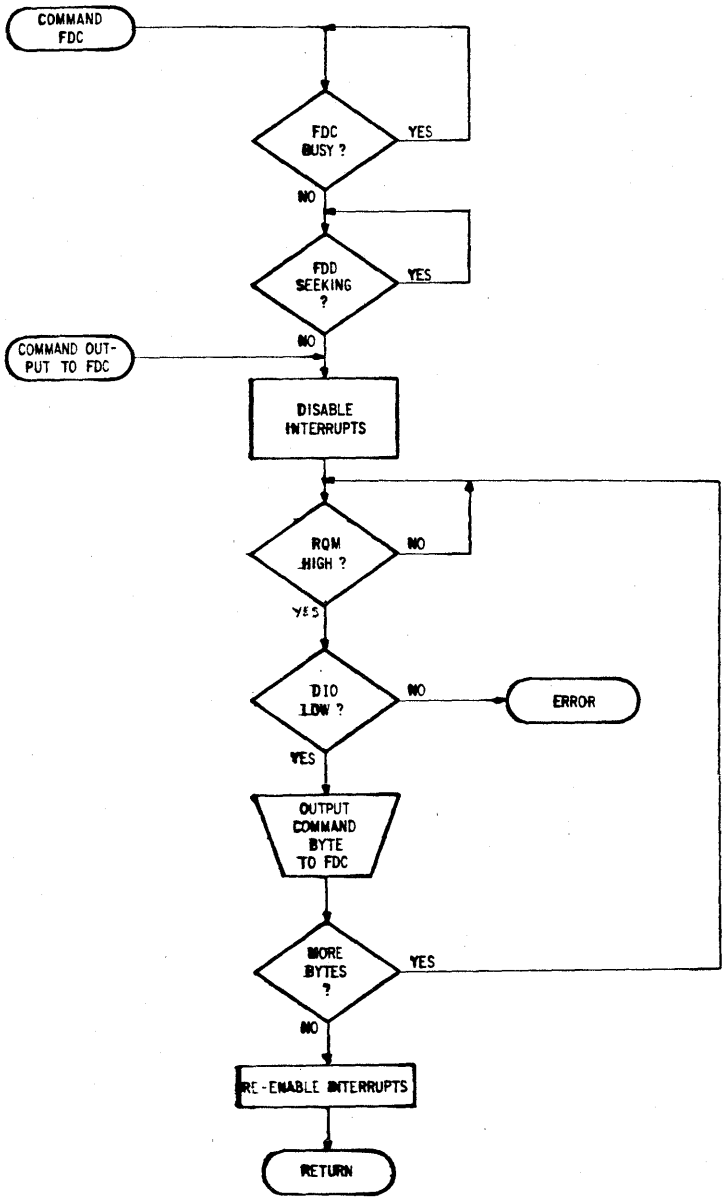


FIGURE 20
DETAIL COMMAND PHASE FLOW CHART

Figure 21 shows how to process interrupts from the uPD765. Note that the data transfer commands (Read, Write, etc.) are treated differently than Seek/Recalibrate commands. Further note that there are two other interrupts: Attention and Invalid. When the data transfer commands terminate, their result phase has started and it is only necessary to read the results from the uPD765. After the byte is read, in the result phase the interrupt is automatically reset. If the interrupt is from a Seek/Recalibrate command terminating, then a Sense Interrupt Status command must be executed to properly end the Seek/Recalibrate command. In this sense the Seek/Recalibrate commands do not really have their own result phase, but rather they rely on the result phase of the Sense Interrupt Status command. The attention interrupt occurs whenever any disk drive goes from not-ready to ready or vice versa. This allows the processor to detect the removal or insertion of a diskette. The invalid interrupt occurs when an invalid command is issued.

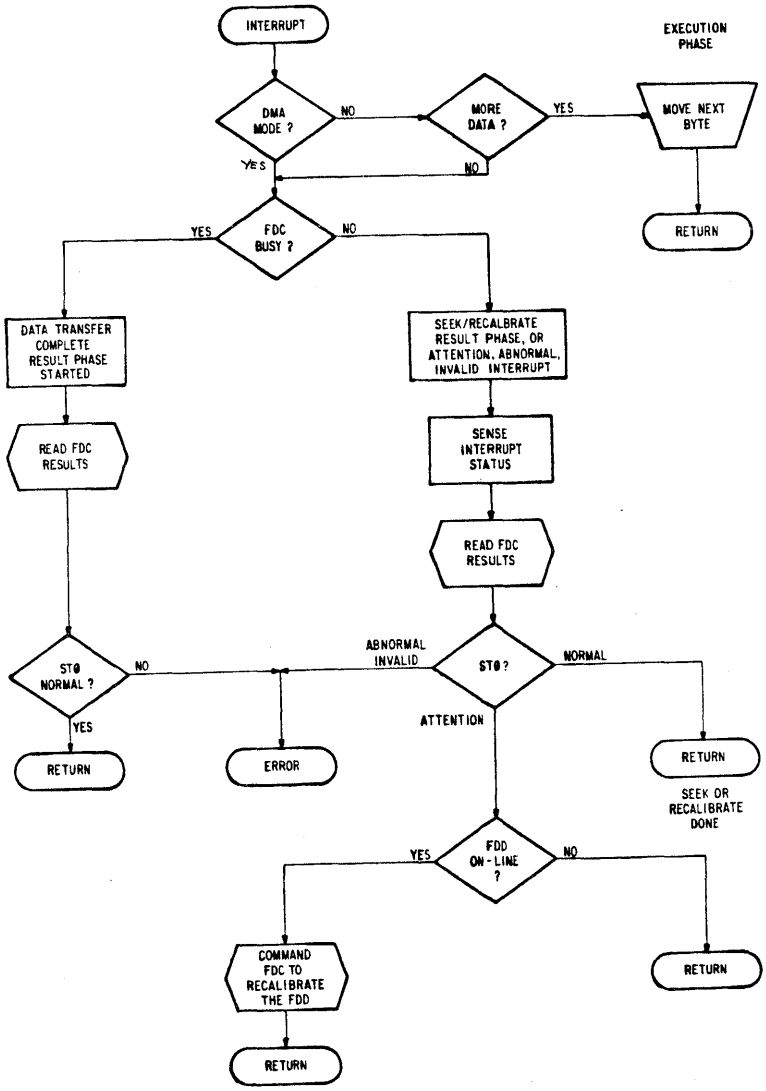


FIGURE 21
INTERRUPT PROCESSING

Figure 22 shows the detailed steps necessary in the result phase. The flow chart shows that the processor need not count the bytes to be read in the result phase, but may merely watch the FDC busy bit in the Main Status Register. When this bit goes "low", it indicates that all bits in the result phase have been read, and the uPD765 is now ready for the next command.

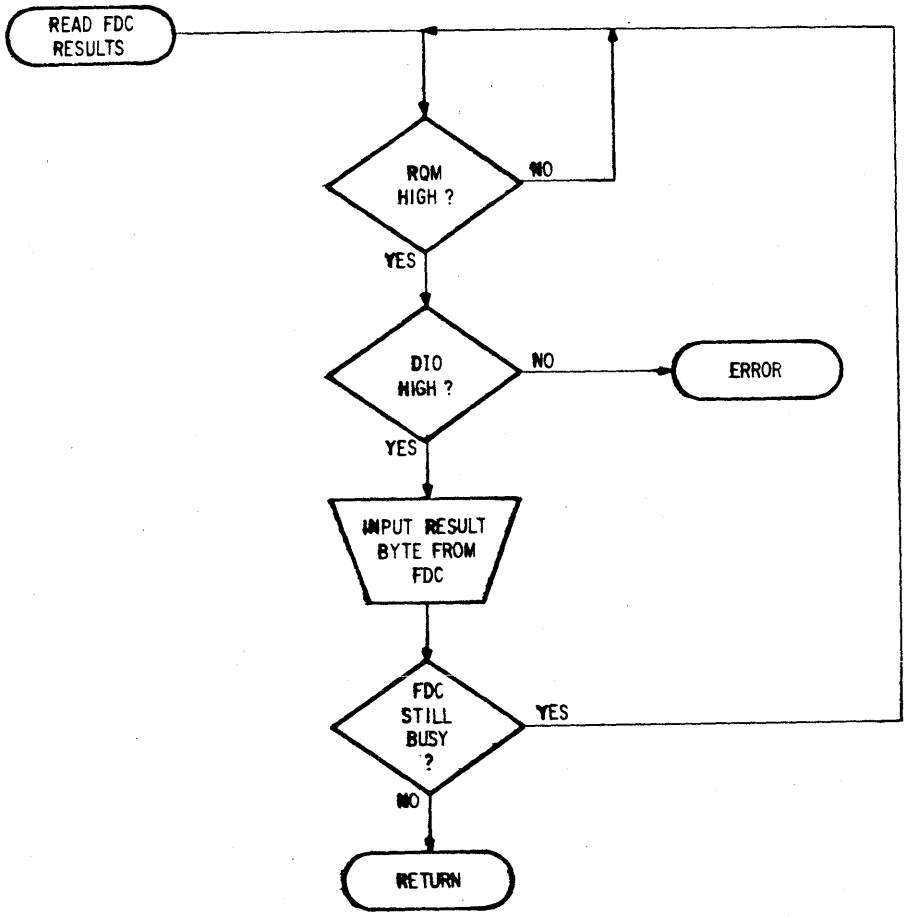


FIGURE 22
DETAIL RESULT PHASE FLOW CHART

APPENDICES

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information during Execution Phase
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire cylinder
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

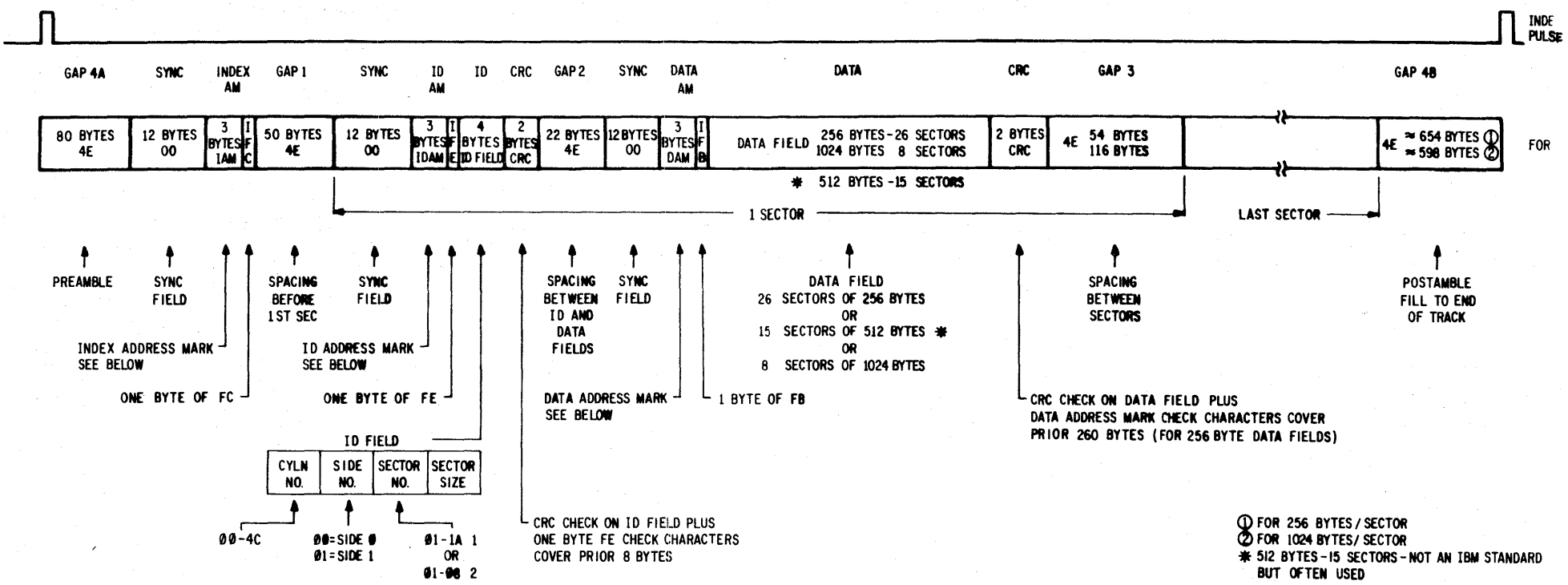
PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
SCAN HIGH OR EQUAL										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

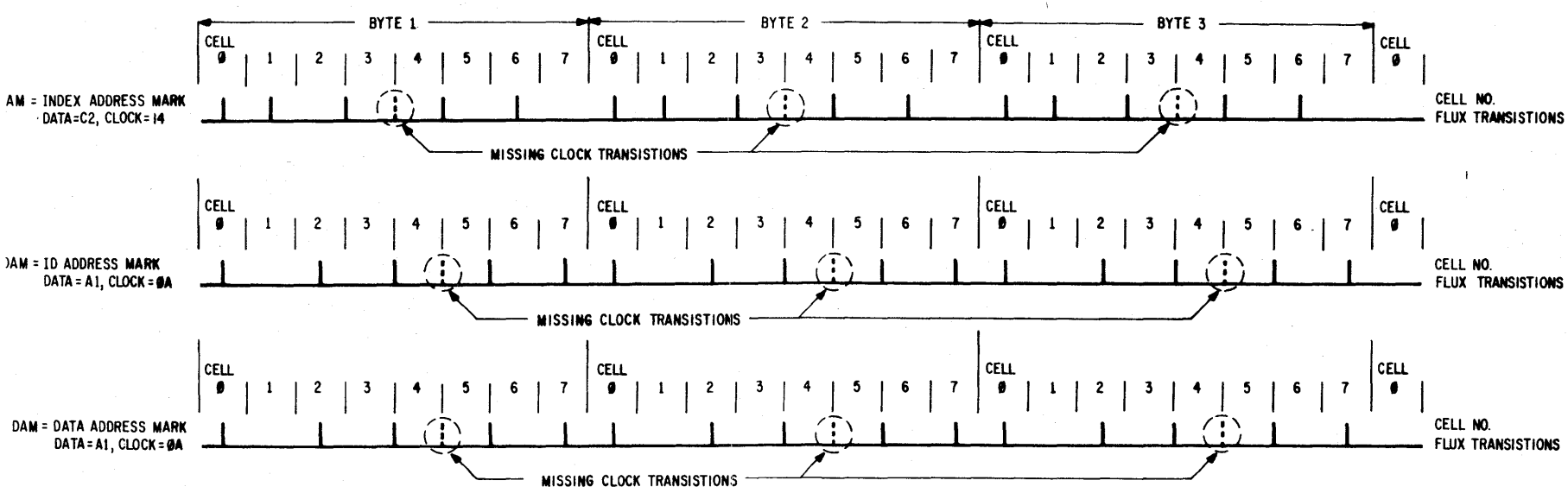
PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	STO								Status information at the end of seek-operation about the FDC
	R	PCN								
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT						HUT		
	W	HLT						ND		
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	ST 3								Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	NCN								
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	Invalid Codes								Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0								ST 0 = 80 (16)

COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1)
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync. Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 256 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (0 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Must be defined for each of the four drives.
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.





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