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Applications Note

Product Name: 82C602 Notebook Companion Chip
Title: Description of the 82C602 in Notebook Mode
Date:

The notebook mode of the OPTi 82C602 chip provides general purpose multiplexers, latches, and logic to anticipate future integrated system designs. This mode is enabled through a strap option that operates as described below.

General Features

The 82C602, in Notebook Mode, provides:

- Multiplexers for interrupt and DMA request scanning
- A byte-wide tri-state buffer
- A decoder for DMA acknowledge signal generation
- An XD-SD bus buffer
- An RTC with CMOS RAM
- Miscellaneous logic.

The attached circuit diagram illustrates the internal logic of the notebook mode.

Power-Saving Features

Signals with tri-state options are listed below. See the attached circuit diagram for a logic representation of these tri-state mechanisms.

- The signals SD[7:0] and XD[7:0] are tri-stated from a logic combination of ATTRIS# (pin 58), ROMCS# (pin 5), ROMCS#/RTCD# (pin 50), and DWE#/KBDCS# (pin 22).
- The signals DACK0-7#, KBDCS#, SMEMR#, and SMEMW# are tri-stated when the input signal ATTRIS# is low.
- The signals DO0# and DO0-7 are tri-stated when the input signal DTRIS# is low.

All other signals are driven to their normal state, usually inactive.

The power to the RTC can be disconnected during system suspend mode even while the rest of the chip remains powered. This feature results in extremely low standby power consumption and is described in the “Reducing Suspend Power Consumption” section that follows.

Strap Settings

At reset time (RST# input low), the 82C602 must sense certain XD bus signal states in order to enable notebook mode.

- XD1 must be sensed low for notebook mode.
- XD3 must be sensed high for operational mode.
- XD4 must be sensed low to enable the internal RTC.

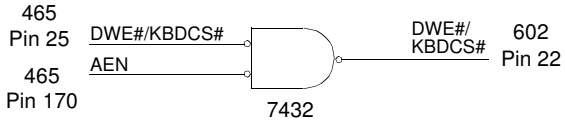
Usually, XD1 and XD4 are pulled to ground by a 4.7kohm resistor; XD3 and the remaining lines (XD0, XD2, and XD5-7) are pulled high by a 10kohm resistor (on the other lines only to prevent floating). Using any strap settings other than those suggested here will leave the 82C602 chip in an undefined state.

Design Notes

The following information is important for proper incorporation of the 82C602 in 82C463MV and 82C465MV system designs.

1. The 82C463MV does not qualify its RTCD# and KBDCS# signals with M/IO# low from the CPU. Therefore, these two chip select signals must be qualified externally with M/IO#, as shown in the attached schematics, before they are presented to the 82C602. The 82C465MV does not require this external qualification.

2. When the 82C465MV is used with the 82C602 and is strapped for its L2 cache mode, the KBDCS# output is combined with the DWE# output. Therefore, this KBDCS#/DWE# signal must be externally qualified with the AEN signal as follows:



3. Note that the 82C602 is a single-voltage part, usually selected as 5V. It has no provisions for 3.3V-to-5V translation. In most cases this limitation is unimportant, as the '602 is primarily an AT-bus interface device. However, for implementations that provide 3.3V input signals, the designer should be aware that 3.3V levels on 5V inputs draw excessive idle current (on the order of 1mA per input).

   For example, the 74244 buffer could be used to buffer eight of the CPU address lines to the AT bus. However, when the system is put into suspend mode, any buffer inputs that remain at 3.3V will cause a current draw and create an undesirable situation for low-power suspend mode operation.

4. In its notebook mode, the 82C602 chip has been qualified for operation at 3.3V. However, the internal RTC still requires 5V for proper operation. RTCVCC, pin 57, provides VCC to the RTC during active mode. The VBATT, pin 55, provides power only to maintain the RTC clock and CMOS data during power down modes and is connected to a 2.4V-4.0V battery.

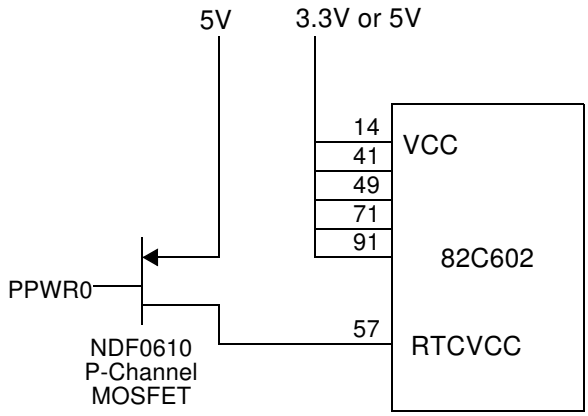
Reducing Suspend Power Consumption

The RTCVCC pin supplies analog circuit power to the RTC during run mode and must always be 5V, regardless of whether the rest of the chip is powered at 5V or 3.3V.

To save power during low-power suspend mode (when the rest of the chip is still powered), this pin may be disconnected from the supply voltage. It is important that the supply be *disconnected,* not simply brought to ground. A p-channel MOSFET is ideal for this purpose. The gate of the MOSFET can be controlled by PPWR0 or PPWR1 from the power control latch.

For example, PPWR0 may be used to switch off RTCVCC by using a P-channel MOSFET as shown in Figure 1. The auto-toggle feature of the PPWR0 line must be enabled, with 82C463MV/465MV configuration register bits 54h[4]=1, 54h[0]=0, and 68h[0]=1. Setting bits 68h[3:2]=10 provides the necessary recovery time to the RTC analog VCC. With this implementation, the MOSFET will switch off the power of the analog VCC only during suspend mode; the only current flow through the analog VCC is leakage current (less than 1µA).

Figure 1 Example of RTCVCC Switching Circuit



The MOSFET used for testing at OPTi is a National Semiconductor NDF0610, which has a typical gate threshold voltage of -2.4V (-3.5V max / -1V min).

82C602 Power Consumption Measurements

Using the circuit of Figure 1, the power consumption of the 82C602 Notebook Mode in use with the OPTi 463MV demonstration board is shown in Tables 1 and 2.

Table 1 Typical Current Consumption for RTC Power

	Normal	Suspend
Analog VCC	< 1.5µA	~1µA
VBAT	~1µA	~1µA

Table 2 Typical Current Consumption for Digital Power

Digital VCC = 3.3V		Digital VCC = 5V	
Normal	**Suspend**	**Normal**	**Suspend**
< 4mA	< 30µA	< 4mA	250µA

Internal Real-Time Clock (RTC)

The internal RTC of the 82C602 is functionally compatible with the DS1285/MC146818B. The following sub-sections will give detailed functional and register features of the on-chip RTC of the 82C602.

RTC Features

- System wake-up capability -- alarm interrupt output active in battery back-up mode
- 4.5V to 5.5V operation
- 114 bytes of general non-volatile storage
- Direct clock/calendar replacement for IBM® AT-compatible computers and other applications
- Less than 1.0µA load under battery operation
- 14 bytes for clock/calendar and control
- BCD or binary format for clock and calendar data
- Calendar in day of the week, day of the month, months, and years, with automatic leap-year adjustment
- Time of day in seconds, minutes, and hours
  - 12- or 24-hour format
  - Optional daylight saving adjustment
- Three individually maskable interrupt event flags:
  - Periodic rates from 122µs to 500ms
  - Time-of-day alarm once-per-second to-once-per-day
  - End-of-clock update cycle.

RTC Overview

The on-chip RTC is a low-power microprocessor peripheral providing a time-of-day clock and 100 year calendar with alarm features and battery operation. The RTC supports 3.3V systems. Other RTC features include three maskable interrupt sources, square-wave output, and 114 bytes of general non-volatile storage.

Wake-up capability is provided by an alarm interrupt, which is active in battery back-up mode.

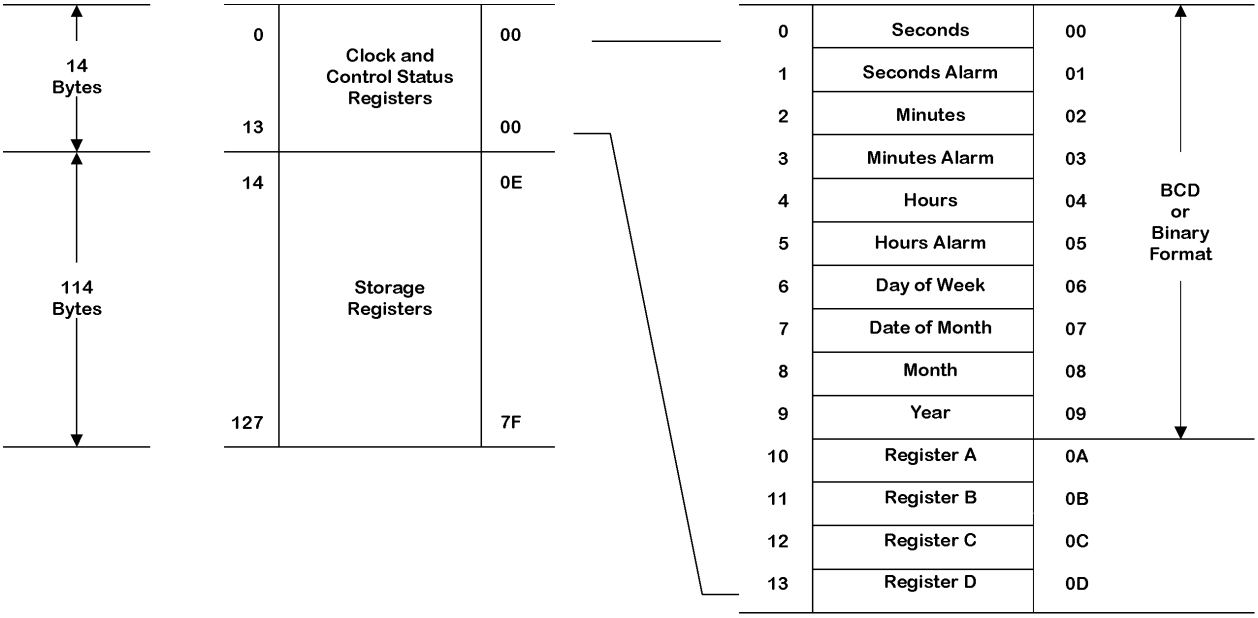
The RTC write-protects the clock, calendar, and storage registers during power failure. A back-up battery then maintains data and operates the clock and calendar.

The on-chip RTC is a fully compatible real-time clock for PC/AT-compatible computers and other applications. The only external components are a 32.768kHz crystal and a back-up battery.

RTC Address Map

The on-chip RTC provides 14 bytes of clock and control/status registers and 114 bytes of general non-volatile storage. Figure 2 illustrates the address map for the RTC.

Figure 2 RTC Address Map



Programming the RTC

The time-of-day, alarm, and calendar bytes can be written in either the BCD or binary format (see Table 3).

These steps may be followed to program the time, alarm, and calendar:

1. Modify the contents of Register B:
   a. Write a 1 to the UTI bit to prevent transfers between RTC bytes and user buffer.
   b. Write the appropriate value to the data format (DF) bit to select BCD or binary format for all time, alarm, and calendar bytes.
   c. Write the appropriate value to the hour format (HF) bit.
2. Write new values to all the time, alarm, and calendar locations.
3. Clear the UTI bit to allow update transfers.

On the next update cycle, the RTC updates all ten bytes in the selected format.

Table 3 Time, Alarm, and Calendar Formats

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
0	Seconds	0-59	00h-3Bh	00h-59h
1	Seconds Alarm	0-59	00h-3Bh	00h-59h
2	Minutes	0-59	00h-3Bh	00h-59h
3	Minutes Alarm	0-59	00h-3Bh	00h-59h
4	Hours, 12-hour Format	1-12	01h-OCh am 81h-8Ch pm	01h-12h am 82h-92h pm
	Hours, 24-hour Format	0-23	00h-17h	00h-23h

Address	RTC Bytes	Range		
		Decimal	Binary	Binary-Coded Decimal
5	Hours Alarm, 12-hour Format	1-12	01h-OCh am 81h-8Ch pm	01h-12h am 82h-92h pm
	Hours Alarm, 24-hour Format	0-23	00h-17h	00h-23h
6	Day of Week (1 = Sunday)	1-7	01h-07h	01h-07h
7	Day of Month	1-31	01h-1Fh	01h-31h
8	Month	1-12	01h-0Ch	01h-12h
9	Year	0-99	00h-63h	00h-99h

Square-wave Output

The RTC divides the 32.768kHz oscillator frequency to produce the 1Hz update frequency for the clock and calendar. Thirteen taps from the frequency divider are fed to a 16:1 multiplexer circuit. The output of this mux is fed to the SQW output and periodic interrupt generation circuitry. The four least-significant bits of Register A, RS[3:0], select among the 13 taps (see Table 4).

Interrupts

The RTC allows three individually selected interrupt events to generate an interrupt request. These three interrupt events are:

1. The periodic interrupt, programmable to occur once every 122µs to 500ms.
2. The alarm interrupt, programmable to occur once-per-second to once-per-day, is active in battery back-up mode, providing a “wake-up” feature.
3. The update-ended interrupt, which occurs at the end of each update cycle.

Each of the three interrupt events is enabled by an individual interrupt enable bit in Register B. When an event occurs, its event flag bit in Register C is set. If the corresponding event enable bit is also set, then an interrupt request is generated. The interrupt request flag bit (INTF) of Register C is set with every interrupt request. Reading Register C clears all flag bits, including INTF, and makes INT# high-impedance.

Two methods can be used to process RTC interrupt events:

1. Enable interrupt events and use the interrupt request output to invoke an interrupt service routine.
2. Do not enable the interrupts and use a polling routine to periodically check the status of the flag bits.

The individual interrupt sources are described in detail in the following sub-sections.

Table 4 Square-Wave Frequency/Periodic Interrupt Rate

Register A Bits				Square-Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
0	0	0	0	None		None	
0	0	0	1	256	Hz	3.90625	ms
0	0	1	0	128	Hz	7.8125	ms
0	0	1	1	8.192	kHz	122.070	µs
0	1	0	0	4.096	kHz	244.141	µs
0	1	0	1	2.048	kHz	488.281	µs
0	1	1	0	1.024	kHz	976.5625	µs
0	1	1	1	512	Hz	1.953125	ms
1	0	0	0	256	Hz	3.90625	ms
1	0	0	1	128	Hz	7.8125	ms
1	0	1	0	64	Hz	15.625	ms
1	0	1	1	32	Hz	31.25	ms
1	1	0	0	16	Hz	62.5	ms

Register A Bits				Square-Wave		Periodic Interrupt	
RS3	RS2	RS1	RS0	Frequency	Units	Period	Units
1	1	0	1	8	Hz	125	ms
1	1	1	0	4	Hz	250	ms
1	1	1	1	2	Hz	500	ms

Periodic Interrupt

The mux output used to drive the SQW output also drives the interrupt generation circuitry. If the periodic interrupt event is enabled by writing a 1 to the periodic interrupt enable bit (PIE) in Register C, an interrupt request is generated once every 122µs to 500ms. The period between interrupts is selected by the same bits in Register A that select the square-wave frequency (see Table 4). Setting OSC[2:0] in Register A to 011 does not affect the periodic interrupt timing.

Alarm Interrupt

The alarm interrupt is active in battery back-up mode, providing a “wake-up” capability. During each update cycle, the RTC compares the hours, minutes, and seconds bytes with the three corresponding alarm bytes. If a match of all bytes is found, the alarm interrupt event flag bit, AF in Register C, is set to 1. If the alarm event is enabled, an interrupt request is generated.

An alarm byte may be removed from the comparison by setting it to a “don't care” state. An alarm byte is set to a “don't care” state by writing a 1 to each of its two most significant bits. A “don't care” state may be used to select the frequency of alarm interrupt events as follows:

A. If none of the three alarm bytes is “don't care,” the frequency is once per day, when hours, minutes, and seconds match.

B. If only the hour alarm byte is “don't care”, the frequency is once per hour when minutes and seconds match.

C. If only the hour and minute alarm bytes are “don't care”, the frequency is once per minute when seconds match.

D. If the hour, minute, and second alarm bytes are “don't care”, the frequency is once per second.

Update Cycle Interrupt

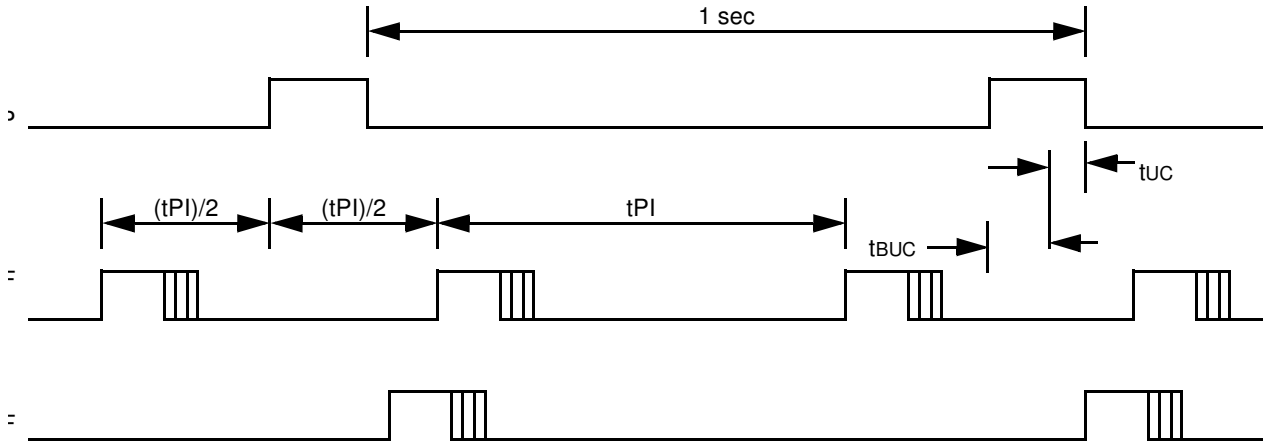
The update cycle ended flag bit (UF) in Register C is set to a 1 at the end of an update cycle. If the update interrupt enable bit (UIE) of Register B is 1, and the update transfer inhibit bit (UTI) in Register B is 0, then an interrupt request is generated at the end of each update cycle.

Accessing RTC bytes

Time and calendar bytes read during an update cycle may be in error. Three methods to access the time and calendar bytes without ambiguity are:

1. Enable the update interrupt event to generate interrupt requests at the end of the update cycle. The interrupt handler has a maximum of 999ms to access the clock bytes before the next update cycle begins (see Figure 3).
2. Poll the update-in-progress bit (UIP) in Register A. If UIP = 0, the polling routine has a minimum of tBUC time to access the clock bytes (see Figure 3).
3. Use the periodic interrupt event to generate interrupt requests every tPI time, such that UIP=1 always occurs between the periodic interrupts. The interrupt handler has a minimum of tPI/2 + tBUC time to access the clock bytes (see Figure 3).

Figure 3 Update-Ended/Periodic Interrupt Relationship



RTC Time-Base Crystal

The RTC's time-base oscillator is designed to work with an external piezoelectric 32.768kHz crystal. A crystal can be represented by its electrical equivalent circuit and associated parameters as shown in Figure 4 and Table 5, respectively.

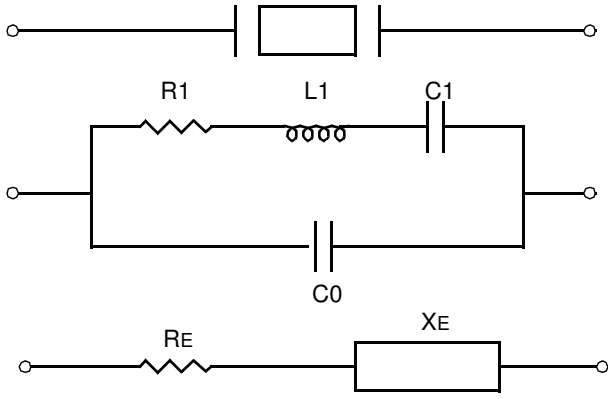
L1, C1, and R1 form what is known as the motional arm of the circuit. C0 is the sum of the capacitance between electrodes and the capacitance added by the leads and mounting structure of the crystal. The equivalent impedance of the crystal varies with the frequency of oscillation.

There are two frequencies at which the crystal impedance appears purely resistive ($X_E = 0$). They're indicated by two points on the graph, known as the series resonant (F_S) and anti-resonant (F_A) frequencies. Oscillators operating the crystal at the resonant frequency (F_S) are termed series resonant circuits, whereas those that operate the crystal around F_A are termed parallel resonant. The on-chip RTC uses a parallel resonant oscillator circuit. The frequency of oscillation in this mode lies between F_S and F_A and is dictated by the effective load capacitance appearing across the crystal inputs, as explained next.

Table 5 Crystal Parameters

Parameter	Symbol	Value	Unit
Nominal Frequency	F	32.768	kHz
Load Capacitance	C_L	6	pF
Motional Inductance	L1	9076.66	H
Motional Capacitance	C1	2.6 x 10-3	pF
Motional Resistance	R1	27	Kohm
Shunt Capacitance	C0	1.1	pF

Figure 4 Quartz Crystal Equivalent Circuit



RTC Oscillator

The parallel resonant RTC oscillator circuit is comprised of an inverting micro-power amplifier with a PI-type feedback network. Figure 5 illustrates a block diagram of the oscillator circuit with the crystal as part of the PI-feedback network. The oscillator circuit ensures that the crystal is operating in the parallel resonance region of the impedance curve.

The actual frequency at which the circuit will oscillate depends on the load capacitance, C_L. This parameter is the dynamic capacitance of the total circuit as measured or computed across the crystal terminals.

A parallel resonant crystal like the DT-26 is calibrated at this load using a parallel oscillator circuit. C_L is computed from C_{L1} and C_{L2} as given below:

$$C_L = (C_{L1} * C_{L2}) / (C_{L1} + (C_{L2})$$

The RTC's C_{L1} and C_{L2} values are trimmed to provide approximately a load capacitance (C_L) of 6pF across crystal terminals. This is to match the specified load capacitance (6pf) at which the recommended DT-26 crystal is calibrated to resonate at the nominal frequency of 32.768kHz. Referring to the impedance graph of Figure 5, "A" indicates the point of resonance when C_L equals the specified load capacitance of the crystal.

Time Keeping Accuracy

The accuracy of the frequency of oscillation depends on:

- Crystal frequency tolerance
- Crystal frequency stability
- Crystal aging
- Effective load capacitance in oscillator circuit
- Board layout

Crystal Frequency Tolerance. The frequency tolerance parameter is the maximum frequency deviation from the nominal frequency (in this case 32.768kHz) at a specified temperature, expressed in ppm (parts per million) of nominal frequency. In the case of the Grade A DT-26 crystal, this parameter is ±20 ppm at 25°C.

Crystal Frequency Stability. This parameter, dependent on the angle and type of cut, is defined as the maximum frequency deviation from the nominal frequency over a specified temperature range, expressed in ppm or percentage of nominal frequency.

Figure 5 shows a typical curve of frequency variation with temperature for the KDS DT-26 crystal.

Figure 5 RTC Oscillator Circuit Block Diagram

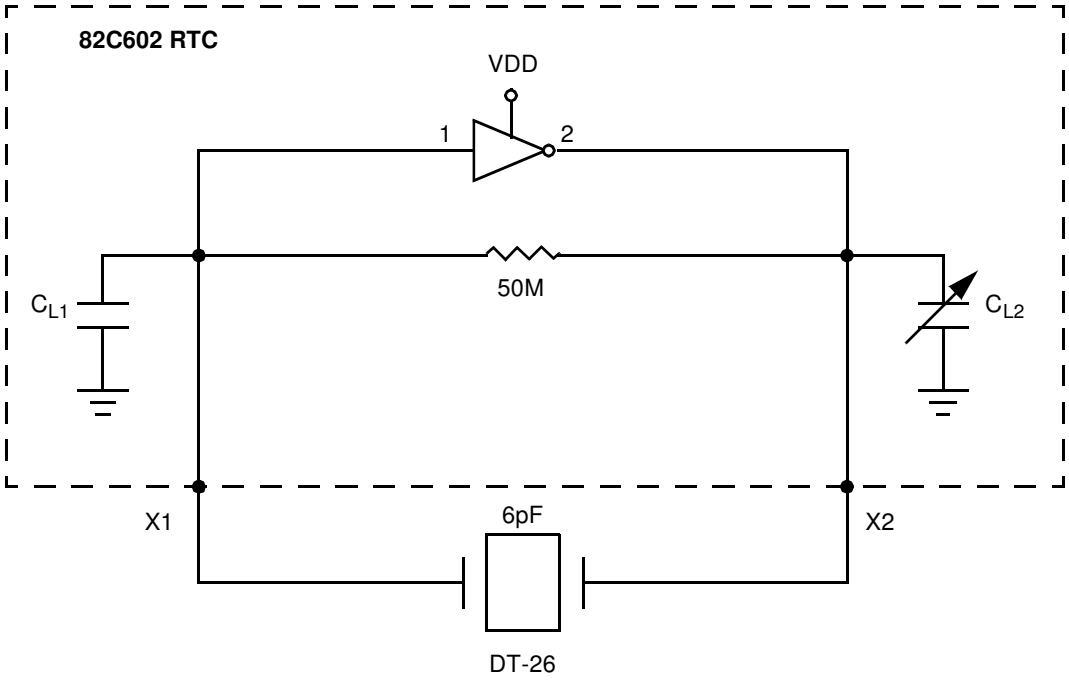
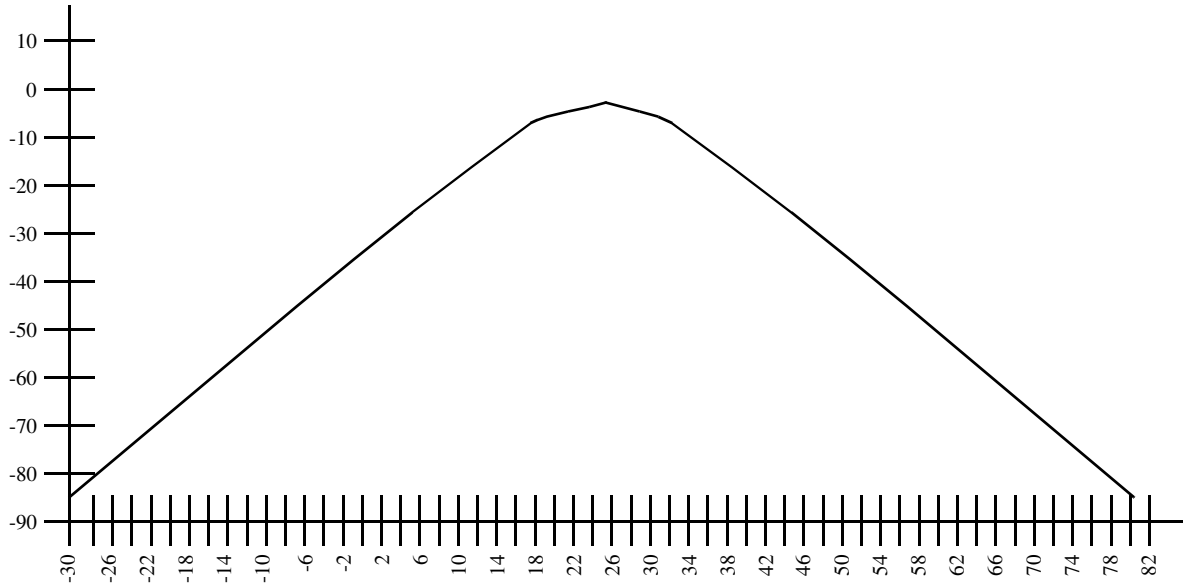


Figure 6 Typical Temperature Characteristics



Crystal Aging. As a crystal ages, some frequency shift may be observed. Drift with age is specified to be typically 4 ppm for the first year and 2 ppm per year for the life of the KDS DT-26 crystal.

Load Capacitance. For a parallel resonant calibrated crystal, the crystal manufacturer specifies the load capacitance at which the crystal will "parallel" resonate at the nominal frequency. From the graph of Figure 5, increasing the effective load capacitance by hanging additional capacitors on either of the X1 or the X2 pin will effectively lower the resonant frequency point "A" toward Fs. The deviation of the frequency Fl with load capacitance is given by:

$$F_L = F_S (1 + C1/2 (C0 + C_L))$$

where C1 is the crystal motional capacitance and C0 is the crystal shunt stray capacitance, as explained above. C_L is the effective load capacitance across the crystal inputs.

Allowing for capacitance due to board layout traces leading to the X1and X2 pins, the RTC is trimmed internally to provide an effective load capacitance of less than 6pF. Connecting a 6pF crystal directly to the X1 and X2 pins will cause the clock to oscillate approximately 24 ppm faster than the nominal frequency of 32.768kHz, for reason explained previously.

For maximum accuracy, it is recommended that a small trim capacitor (< 8pF) be hooked to the X2 pin to move the resonant point closer to the nominal frequency. The graph of Figure 7 shows the variation of frequency with additional load capacitance on the X2 pin of the RTC.

Translating the data in Figure 7 into a practical rule of thumb: for every additional 1.54pF capacitance on the X2 pin, the frequency will decrease by 0.8Hz or a ΔF/F of -24.4 ppm around 82.768kHz.

Board Layout. Given the high input impedance of the crystal input pins X1 and X2, care should be taken to route high-speed switching signal traces away from them. Preferably a ground-plane layer should be used around the crystal area to isolate capacitive-coupling of high frequency signals. The traces from the crystal leads to the X1 and X2 pins must be kept short with minimal bends. A good rule of thumb is to keep the crystal traces within 5mm of the X1 and X2 pins.

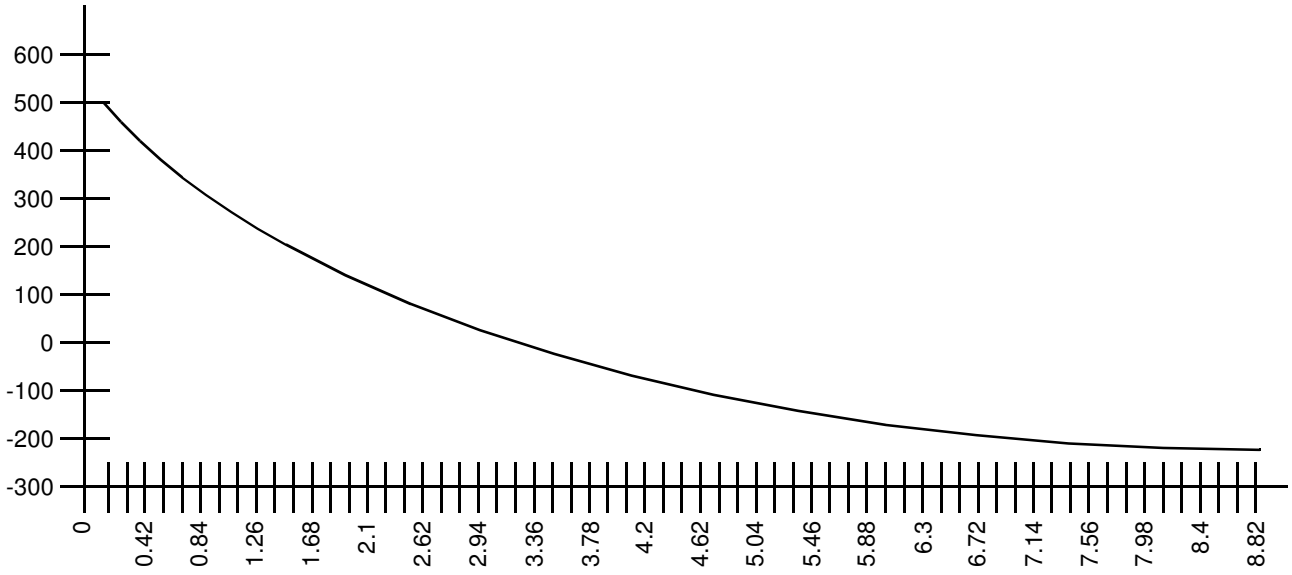
Finally, a 0.1µF ceramic by-pass capacitor should be placed close to the VCC pin of the RTC to provide an improved supply into the clock

Oscillator Start-up. Barring accuracy issues, the RTC will oscillate with any 32.768kHz crystal. When hooked to the X1 and X2 pins in certain configurations, however, passive components can lead to oscillator start-up problems:

Excessive loading on the crystal input pins X1 and X2

Use of a resistive feedback element across the crystal.

Figure 7 Frequency Variation Versus Load Capacitance



Values above 10pF on either the X1 or X2 pin must be avoided. The feedback element is build into the RTC for start-up and no resistive feedback external to the part is required.

Oscillator Control

When power is first applied to the RTC and VCC is above V_{PFD}, the internal oscillator and frequency divider are turned on by writing a 010 pattern to bits 4 through 6 of Register A. A pattern of 011 behaves as 010 but additionally transforms Register C into a read/write register. This allows the 32.768kHz output on the square-wave pin to be turned on. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. Any other pattern to these bits keeps the oscillator off.

Power-Down/Power-Up Cycle

The RTC's power-up/power-down cycles are different. The RTC continuously monitors VCC for out-of-tolerance. During a power failure, when VCC falls below V_{PFD} (2.53V typical), the RTC write-protects the clock and storage registers. The power source is switched to BC when VCC is less than V_{PFD} and BC is greater than V_{PFD}, or when VCC is less than V_{BC} and V_{BC} is less than V_{PFD}. RTC operation and storage data are sustained by a valid back-up energy source. When VCC is above V_{PFD}, the power source is VCC. Write-protection continues for t_{CSR} time after VCC rises above V_{PFD}.

The RTC continuously monitors VCC for out-of-tolerance. During a power failure, when VCC falls below V_{PFD} (4.17V typical), the RTC write-protects the clock and storage regis-

ters. When VCC is below V_{BC} (3V typical), the power source is switched to BC. RTC operation and storage data are sustained by a valid back-up energy source. When VCC is above V_{BC}, the power source is VCC. Write-protection continues for t_{CSR} time after VCC rises above V_{PFD}.

Control/Status Registers

The four control/status registers of the RTC are accessible regardless of the status of the update cycle (see Table 6).

Register A

Register A programs the frequency of the periodic event rate, and oscillator operation. Register A provides the status of the update cycle. See Table 7 for Register A's format.

Register B

Register B enables the update cycle transfer operation, square-wave output-interrupt events, and daylight saving adjustment. Register B selects the clock and calendar data formats. See Table 8 for Register B's format.

Register C

Register C is a read-only event status register. See Table 9 for Register C's format.

Register D

Register D is a read-only data integrity status register. See Table 10 for Register D's format.

Table 6 Control/Status Registers Summary

Register	Loc. (Hex)	Read	Write	Bit Name and State on Reset															
				7 (MSB)		6		5		4		3		2		1		0 (LSB)	
A	0A	Yes	Yes[1]	UIP	NA	OSC2	NA	OSC1	0	OSC0	0	RS3	NA	RS2	NA	RS1	NA	RS0	NA
B	0B	Yes	Yes	UTI	NA	PIE	0	AIE	0	UIE	0	SQWE	0	DF	NA	HF	NA	DSE	NA
C	0C	Yes	No[2]	INTF	0	PF	0	AF	0	UF	0	-	0	32KE	0	-	0	-	0
D	0D	Yes	No	VRT	NA	-	0	-	0	-	0	-	0	-	0	-	0	-	0

Note NA = Not Affected
1. Except Bit 7
2. Read/write only when OSC[2:0] in Register A is 011 (binary).

Table 7 Register A

Bit(s)	Type	Default	Function
7	RO		UIP - Update-In-Progress: This read-only bit is set prior to the update cycle. When UIP equals 1, an RTC update cycle may be in progress. UIP is cleared at the end of each update cycle. This bit is also cleared when the update transfer inhibit (UTI) bit in Register B is 1.
6:4			OSC[2:0] - Oscillator Control Bits 2 through 0: These three bits control the state of the oscillator and divider stages. A pattern of 010 enables RTC operation by turning on the oscillator and enabling the frequency divider. A pattern of 11X turns the oscillator on, but keeps the frequency divider disabled. When 010 is written, the RTC begins its first update after 500ms.
3:0			RS[3:0] - Rate Select Bits 3 through 0: These bits select one of the 13 frequencies for the SQW output and the periodic interrupt rate, as shown in Table 3.

Table 8 Register B

Bit(s)	Type	Default	Function
7	R/W		UTI - Update Transfer Inhibit: This bit inhibits the transfer of RTC bytes to the user buffer. 1 = Inhibits transfer and clears UIE0 = Allows Transfer
6	R/W		PIE - Periodic Interrupt Enable: This bit enables an interrupt request due to a periodic interrupt event. 1 = Enabled 0 = Disabled

Bit(s)	Type	Default	Function
5	R/W		AIE - Alarm Interrupt Enable: This bit enables an interrupt request due to an alarm interrupt event. 1 = Enabled 0 = Disabled
4	R/W		UIE - Update Cycle Interrupt Enable: This bit enables an interrupt request due to an update ended interrupt event. 1 = Enabled 0 = Disabled The UIE bit is automatically cleared when the UTI bit equals 1.
3	R/W		SQWE - Square-wave Enable: This bit enables the square-wave output. 1 = Enabled 0 = Disabled and Held Low
2	R/W		DF - Data Format: This bit selects the numeric format in which the time, alarm, and calendar bytes are represented. 1 = Binary 0 = BCD
1	R/W		HF - Hour Format: This bit selects the time-of-day and alarm hour format. 1 = 24-Hour Format 0 = 12-Hour Format
0	R/W		DSE - Daylight Saving Enable: This bit enables daylight saving time adjustments when written to 1. On the last Sunday in October, the first time the RTC increments past 1:59:59 AM, the time falls back to 1:00:00 am. On the first Sunday in April, the time springs forward from 2:00:00 am to 3:00:00 am.

Table 9 Register C

Bit(s)	Type	Default	Function
7	R/W		INTF - Interrupt Request Flag: This flag is set to a 1 when any of the following is true; AIE = 1 and AF = 1 PIE = 1 and PF = 1 UIE = I and UF=1 Reading Register C clears this bit.
6	R/W		PF - Periodic Event Flag: This bit is set to a 1 every tPI time, where tPI is the time period selected by the settings of RS[3:0] in Register A. Reading Register C clears this bit.
5	R/W		AF - Alarm Event Flag: This bit is set to a 1 when an alarm event occurs. Reading Register C clears this bit.
4	R/W		UF - Update Event Flag: This bit is set to a 1 at the end of the update cycle. Reading Register C clears this bit.
3:0	R/W	0000	NU - Not Used - This bit is always set to 0.

Table 10 Register D

Bit(s)	Type	Default	Function
7	RO		VRT - Valid RAM and Time: 1 = Valid backup energy source 0 = Backup energy source is depleted When the backup energy source is depleted (VRT = 0), data integrity of the RTC and storage registers is not guaranteed.
6:0	RO		NU - Not Used - These bits are always set to 0.

Pin Assignment

The following tables provide the pin definitions for 82C602 notebook mode. Separate tables list the signal pins and power/grounds pins. Signals that are functionally similar with the same pin on other 82C602 modes are denoted with an asterisk.

Power Pins

Pin	'804 Mode Signal	I/O	'804 Mode Signal Description
14 41 71 91	VCC	P	+5V or +3.3V Power
57	RTC VCC	P	+5V RTC Power
55	VBAT	P	Standby battery VCC to RTC
49	Must be tied high	P	Internal enable signal
3 15 28 40 52 66 78 90	VSS	P	Ground

Signal Pins

Pin	Signal	Drive (mA)	I/O	Description (Notebook Mode)
1	DRQ7		I	DMA channel 7 request
2	DACK-MUX0		I	Encoded DACKs
4	DACK-MUX1		I	
5	DACK-MUX2		I	
6	DI1		I	Data buffer input 0-1
7	DI0		I	
8	IRQ14		I	Interrupt request inputs
9	IRQ12		I	
10	IRQ10		I	
11	IRQ7		I	
12	IRQ6		I	
13	IRQ4		I	
16	IOR#*		I	I/O Read

Signal Pins (Continued)

Pin	Signal	Drive (mA)	I/O	Description (Notebook Mode)
17	IOW#*		I	I/O Write
18	RQMX3	6	O	Mux of DRQ 1,3,6,7
19	RQMX2	6	O	Mux of IRQ10,15, DRQ0,5
20	RTCAS		I	RTC command line
21	KBCLK		I	Keyboard clock input for demuxing
22	DWE#/ KBDCS#		I	Muxed DRAM write / keyboard CS
23	RST#*		I	Reset input to '602 logic
24	KBCLK2		I	Keyboard clock / 2 input for demuxing
25	RQMX0	4	O	Mux of IRQ1,3,7,14
26	Reserved*			For test purposes
27	RQMX1	4	O	Mux of IRQ4,6,8,12
29	DI7		I	Data buffer inputs 2-7
30	DI6		I	
31	DI5		I	
32	DI4		I	
33	DI3		I	
34	DI2		I	
35	DO0	4	O	Data buffer outputs 0-7
36	DO1	4	O	
37	DO2	4	O	
38	DO3	4	O	
39	DO4	4	O	
42	DO5	4	O	
43	DO6	4	O	
44	DO7	4	O	
45	IRQ3		I	Interrupt request inputs
46	IRQ1		I	
47	DTRIS#		I	Data buffer tristate control
48	ROMCS#		I	XD bus buffer enable decode
49	VCC		I	Must be tied high

Signal Pins (Continued)

Pin	Signal	Drive (mA)	I/O	Description (Notebook Mode)
50	ROMCS#/ RTCD#		I	ROM CS and RTC command line
51	IRQ15		I	Interrupt request input
53	X1*			RTC 32kHz crystal connection
54	X2*			
55	VBATT*			RTC/CMOS battery input
56	IRQ8*		OC	RTC alarm output
58	ATTRIS#		I	Tri-states AT-bus outputs
59	DACK0#	6	O	DMA acknowledge outputs
60	DACK1#	6	O	
61	DACK2#	6	O	
62	DACK3#	6	O	
63	DACK5#	6	O	
64	DACK6#	6	O	
65	DACK7#	6	O	
67	KBDCS#	6	O	DWE#/KBDCS# decoded by AEN
68	MEMR#*		I	Memory read
69	MEMW#*		I	Memory write
70	ATCYC#		I	AT cycle indication
72	DRQ5		I	DMA request input
73	SMEMR#*	24	O	SMEMR# with tri-state control
74	SMEMW#*	24	O	SMEMW# with tri-state control
75	DO0#	8	O	Inverted DO0
76	RSTDRV	24	O	Inverted RST#
77	AEN		I	Input only

Signal Pins (Continued)

Pin	Signal	Drive (mA)	I/O	Description (Notebook Mode)
79	SD0	24	I/O	SD Bus
80	SD1*	24	I/O	
81	SD2*	24	I/O	
82	SD3*	24	I/O	
83	SD4*	24	I/O	
84	SD5*	24	I/O	
85	SD6*	24	I/O	
86	SD7*	24	I/O	
87	DRQ0		I	DMA request input
88	XD0*	6	I/O	XD Bus
89	XD1*	6	I/O	(Strap XD1 low for '804 mode)
92	XD2*	6	I/O	
93	XD3*	6	I/O	(Strap XD3 high for normal operation)
94	XD4*	6	I/O	(Strap XD4 low to enable RTC)
95	XD5*	6	I/O	
96	XD6*	6	I/O	
97	XD7*	6	I/O	
98	DRQ1		I	DMA request inputs
99	DRQ3		I	
100	DRQ6		I	

Figure 8 Pin Diagram

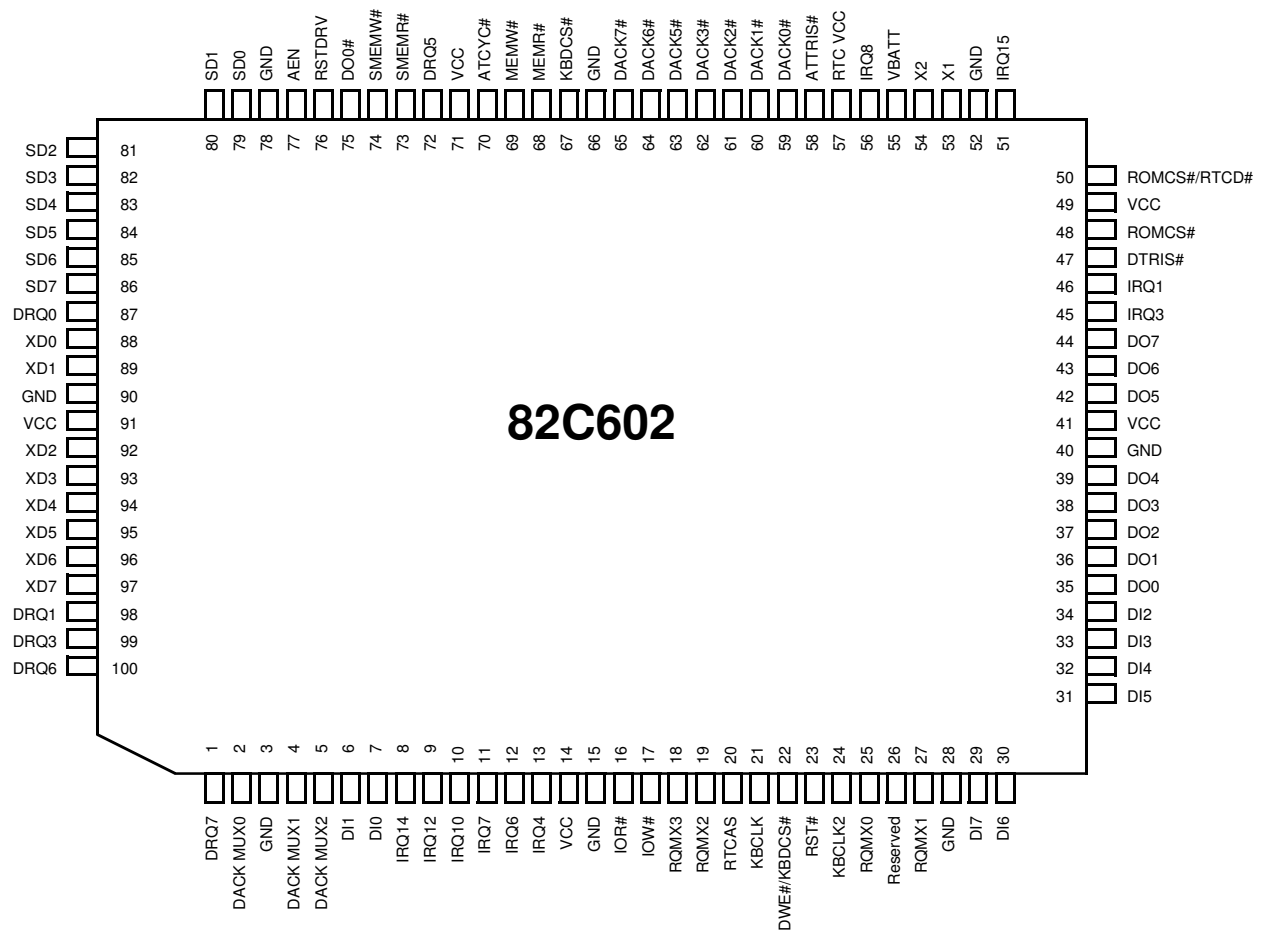
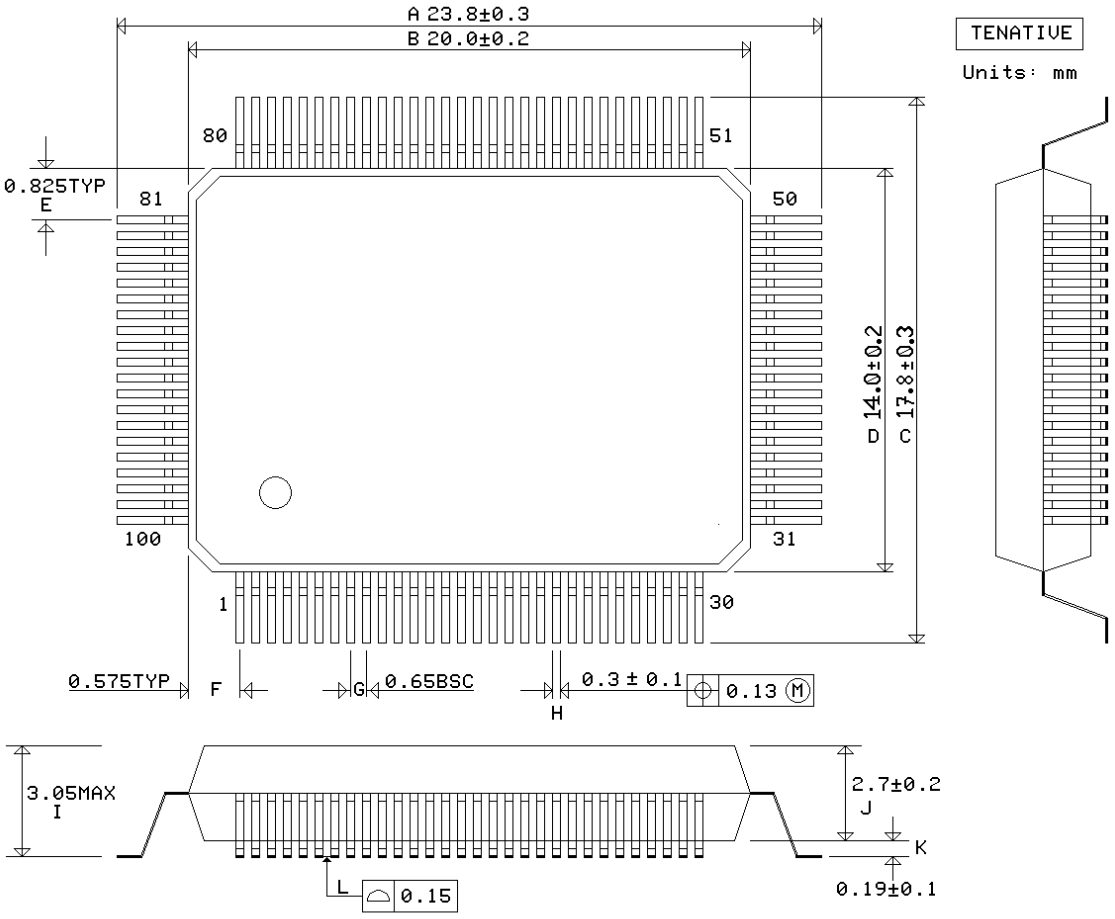
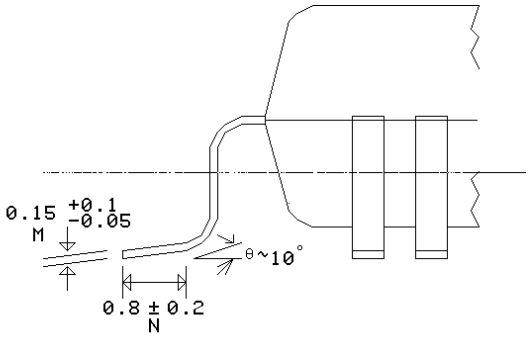


Figure 9 Mechanical Package





DIM	MILLIMETERS		INCHES		DESCRIPTION
	MIN	MAX	MIN	MAX	
A	23.5	24.1	.925"	.949"	Maximum Width LEAD TO LEAD
B	19.8	20.2	.779"	.795"	Maximum Width PACKAGE ENVELOPE
C	17.5	18.1	.689"	.713"	Maximum Height LEAD TO LEAD
D	13.8	14.2	.543"	.559"	Maximum Height PACKAGE ENVELOPE
E	0.825 TYP		.0325" TYP		LEAD CENTER TO PERP. LEAD PLANE
F	0.575 TYP		.0226" TYP		LEAD CENTER TO PERP. LEAD PLANE
G	0.65 BSC		.0256" BSC		LEAD TO LEAD CENTER SPACING
H	0.2	0.4	.008"	.016"	LEAD WIDTH
I	——	3.05	——	.120"	PACKAGE HEIGHT LEAD PLANE TO TOP
J	2.5	2.9	.098"	.114"	MAXIMUM THICKNESS PACKAGE ENVELOPE
K	0.09	0.29	.0035"	.0114"	LEAD PLANE TO PACKAGE BOTTOM
L	——	0.15	——	.006"	LEAD PLANE SKEW
M	0.1	0.25	.004"	.010"	LEAD THICKNESS
N	0.6	1.0	.024"	.039"	LEAD FOOTPRINT

Attach Schematic (915-2000-018)