Tech Brief:

Anatomy of a hyperSPARC Module

Microprocessor technology is continuously evolving in complexity in order to meet the demands of today's high-performance applications. Through advanced packaging technology, ROSS has increased the speed and reliability, reduced the size, and facilitated the manufacturability of its CPU chip sets in order to address the market's requirements.

ROSS' hyperSPARC chip set utilizes multi-die packaging (MDP) in which multiple die are connected through a multi-layer substrate in a single package to achieve higher clock frequencies, lower power consumption, less capacitive loading, and smaller board-surface requirements. The hyperSPARC chip set is comprised of the superscalar RT620 Central Processing Unit (CPU), the RT625 Cache Controller, Memory Management, and Tag Unit (CMTU), and four RT627 Cache Data Units (CDUs) for 256 Kbytes of second-level cache. The chip set supports uniprocessing (Level 1 MBus) or multiprocessing (Level 2 MBus).

The RT620, hyperSPARC's primary processing unit, consists of an 8-Kbyte instruction cache and five execution units: an Arithmetic and Logic Unit (ALU), a load/Store unit, a Branch/Call unit (for processing control transfer instructions), a floating-point adder, and a floating-point multiplier unit. The RT620 contains two register files: 136 integer resisters configured as eight register windows, and 32 separate floating-point registers in the floating-point unit.

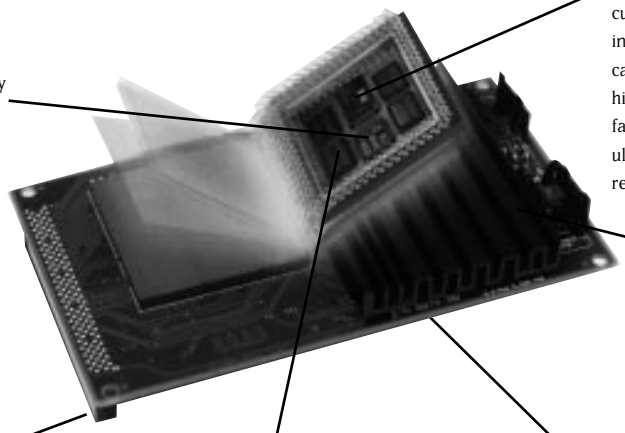
The hyperSPARC chip set delivers world-class performance in multi-die packaging.

hyperSPARC's second-level cache is built around the RT625 CMTU, a combined cache controller and memory management unit that supports shared-memory, symmetric multiprocessing. The cache controller portion supports 256 Kbytes of cache, made up of four RT627 CDUs. The RT625 contains 4-Kbytes of on-chip cache tags. The cache is physically tagged and virtually indexed so that the RT625's cache coherency logic can quickly determine snoop hits and misses for multiprocessing applications without stalling the RT620's access to the cache. Both copy-back and write-through caching modes are supported.

The memory management portion (MMU) of the RT625 is a SPARC Reference MMU with a 64-entry, fully set-associative Translation Lookaside Buffer (TLB) that supports 4096 contexts. The RT625 contains a read buffer and a write buffer for buffering the 32-byte cache lines in and out of the second-level cache.

The RT627 is a high speed SRAM that is custom-designed for hyperSPARC's cache requirements. It is organized as four arrays of 16-Kbyte static memory with byte-write logic, registered inputs, and data-in and data-out latches. The RT627 provides a zero-wait-state cache to the CPU with no pipeline penalty (i.e., stalls) for loads and stores that hit the cache. The RT627 is designed specifically for hyperSPARC, so it doesn't require glue logic for interfacing to the RT620 (CPU) and the RT625 (CMTU).

RT625 CMTU: The RT625 is a combined Cache Controller and Memory Management Unit optimized for multiprocessing. It features a SPARC Reference MMU, cache controller, cache tag memory (supports up to 256-KBytes of second-level cache), read and write buffers, and asynchronous bus interface. The RT625 supports the SPARC MBus Level 2 protocol for multiprocessing systems.



RT620 CPU: The RT620 is a high performance full-custom CMOS implementation of integrated SPARC integer and floating-point logic, with an on-chip cache for instructions. Combining a superscalar, highly-pipelined architecture with advanced manufacturing technology allows the RT620 to achieve ultra-high performance without requiring software recompilation.

Reliability: Specially designed for ROSS' hyperSPARC modules, heat sinks provide effective thermal management to ensure hyperSPARC's reliability in a wide range of applications and environments.

Connector: The MBus connector is a controlled-impedance type based on a microstrip configuration that provides a controlled characteristic impedance plus very low inductance and capacitance. Separate power and ground blades are provided for isolation and to prevent noise transference. The connector is a SPARC standard.

RT627 CDU: The RT627 Cache Data Unit is organized as four arrays of 16-KByte static memory with a built-in, one-deep write buffer pipeline, byte write logic, registered inputs, data-in and data-out latches, and data forwarding logic for the write buffer. The RT627 is designed specifically for hyperSPARC, requiring no glue logic for interfacing to the RT620 and RT625.

MBus Module: hyperSPARC conforms to the SPARC-standard MBus specifications and is populated with either one or two hyperSPARC MDPs. Specially designed are both uni- and multiprocessing daughtercards. These modules provide an easy and inexpensive upgrade path for SPARCstation users.

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