S3 Incorporated

86CM65 Aurora64V+ Dual Display Accelerator

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S3 Incorporated
P.O. Box 58058
Santa Clara, CA 95052-8058

NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When numerical modifiers such as K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

NOTICES

Additional information may be obtained from:

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Section 1: Introduction

High-Performance Graphics Accelerator Core

- Integrated 64-bit graphics accelerator /RAMDAC/clock-synthesizer core enables desktop-level performance
- Supports VGA, SVGA, and XGA flat panel displays
- Provides 1280x1024x8-bit, 75 Hz refresh, non-interlaced CRT mode
- 3.3V/5V operation

Direct Interface to Broad Range of LCDs

- Support for VGA, SVGA and XGA dual-scan/single-scan color panels with 8-bit, 16-bit, and 24-bit interfaces
- Support for VGA, SVGA and XGA TFT color panels with 9-bit, 12-bit and18-bit (1 pixel/clock and 2 pixels/clock) interfaces
- Advanced frame rate control and dithering algorithms provide up to 16.7 million colors
- Panel data polarity switching for EMI reduction
- Auto-expansion and centering for VGA text and graphics modes on SVGA and XGA panels

Industry-Leading Simultaneous Display Capability

- CRT and flat panel refresh rates are independently programmable to allow optimum image quality via DuoView architecture
- Simultaneous TV/flat panel display

Multimedia Acceleration

- Integrated S3 Streams Processor enables 30 frames-per-second, full-screen, 24-bit playback of full motion video
- Mixed-format (simultaneous YUV and RGB) data in video memory
- Blending of graphics and video streams of different color depths
- High-quality hardware scaling using filtered interpolation
- Color key/chroma key control of graphic/video overlay placement

Comprehensive Power Management

- Self-refresh and slow-refresh DRAM support
- Standby and low power suspend modes
- Hardware and software suspend support
- DPMS
- S3 Dynamic Power Management

64x64x2 Pixel Hardware Pop-up Icon

- Available in all modes
- 8 separate bitmaps can be stored

Integrated Programmable Frequency Synthesizers

- Dual, independent frequency synthesizers for DAC and memory control
- DCLK up to 110 MHz @ 3.3V, 135 MHz @ 5V
- MCLK up to 50 MHz @ 3.3V

S3 Scenic Highway Video Bus For Low-Cost Multimedia Solutions

- ZV Port compliant
- Glueless 8- or 16-bit interface to video digitizers
- Glueless, bi-directional interface to S3 Scenic/MX2 MPEG decoder

Integrated TV Encoder

- Direct output to NTSC/PAL monitors
- Composite or SVideo format

Flexible Memory Support

- Fast page or EDO DRAMs
- 1-MByte with 2 256Kx16 DRAMs
- 2-MBytes with 4 256Kx16 DRAMs
- 2-MBytes with 1 512Kx32 DRAM
- 4-MBytes with 2 512Kx32 DRAMs

24-bit True-Color RAMDAC

Glueless PCI Local Bus Interface

PowerPC™ Support: Bi-endian Byte Ordering

Monitor Plug and Play Support: VESA® DDC

256-pin PBGA Package

- 27.0 mm x 27.0 mm footprint
- 1.27 mm ball pitch

The S3® 86CM65 Aurora64V+™ dual display accelerator is the first in a series of highly-integrated flat-panel controller products to be offered by S3 with the goal of providing better-than-desktop features and performance to the notebook computer market. It combines a 64-bit memory interface and graphics engine with a 24-bit high-performance 135 MHz RAMDAC, a flat panel interface capable of controlling the latest STN and TFT panels, S3's Scenic Highway™ multimedia interface and Streams Processor™ video acceleration technology, and direct NTSC/PAL output. These elements, designed around S3's DuoView™ architecture, provide the performance, flexibility, and display quality necessary for premium multimedia notebook computer systems. Comprehensive, flexible hooks are provided to simplify graphics subsystem power management.

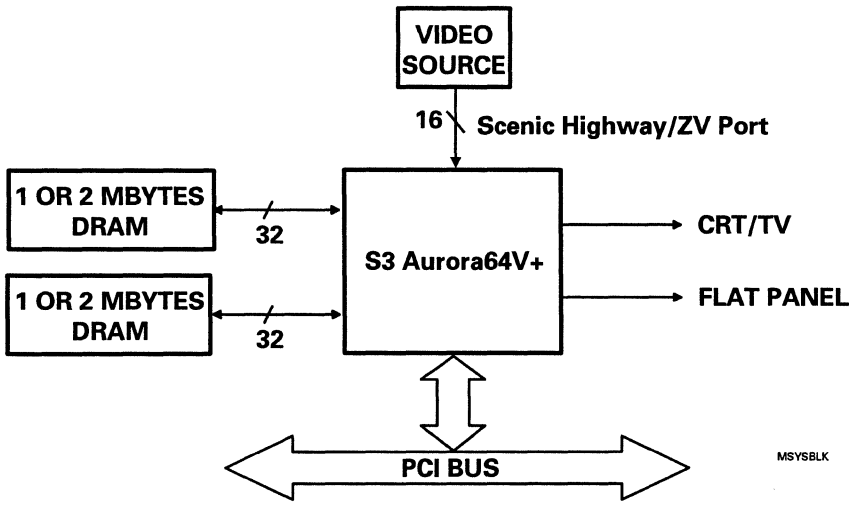


Figure 1-1. System Block Diagram

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Thermal Resistance Θ_{JC}		5		°C/W
Thermal Resistance Θ_{JA} (Still Air)		27		°C/W
Junction Temperature			125	°C
Case Temperature			105	°C

2.2 MECHANICAL DIMENSIONS

The 86CM65 comes in a 256-pin BGA package. The mechanical dimensions are given in Figure 2-1.

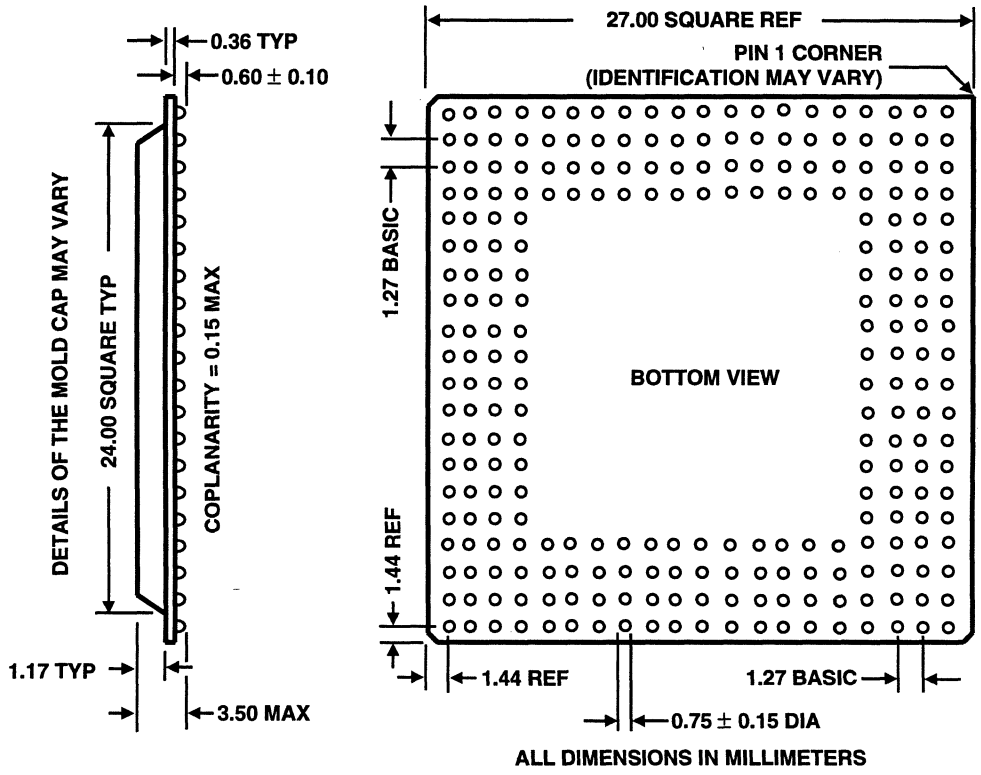


Figure 2-1. 256-pin BGA Mechanical Dimensions

Section 3: Pins

3.1 PINOUT DIAGRAMS

The 86CM65 comes in a 256-pin BGA package. The pin locations for this package are shown in Figure 3-1. Refer to the pin lists later in this section for pin names associated with each pin.

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17	B18	B19	B20
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17	C18	C19	C20
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20
E1	E2	E3	E4													E17	E18	E19	E20
F1	F2	F3	F4													F17	F18	F19	F20
G1	G2	G3	G4													G17	G18	G19	G20
H1	H2	H3	H4													H17	H18	H19	H20
J1	J2	J3	J4						86CM65							J17	J18	J19	J20
K1	K2	K3	K4						Top View							K17	K18	K19	K20
L1	L2	L3	L4													L17	L18	L19	L20
M1	M2	M3	M4													M17	M18	M19	M20
N1	N2	N3	N4													N17	N18	N19	N20
P1	P2	P3	P4													P17	P18	P19	P20
R1	R2	R3	R4													R17	R18	R19	R20
T1	T2	T3	T4													T17	T18	T19	T20
U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17	U18	U19	U20
V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12	V13	V14	V15	V16	V17	V18	V19	V20
W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16	W17	W18	W19	W20
Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	Y10	Y11	Y12	Y13	Y14	Y15	Y16	Y17	Y18	Y19	Y20

Figure 3-1. Aurora64V+ Pin Locations (Top View)

3.2 PIN DESCRIPTIONS

The following table provides a brief description of each pin on 86CM65. The following abbreviations are used for pin types.

I - Input signal
O - Output signal
B - Bidirectional signal

Some pins have multiple names. This either reflects the different functions performed by those pins depending on the bus configuration selected by power-on-strapping or multiplexed pins whose functions are selected via a register bit setting. The pin definitions and functions are given for each possible case.

Table 3-1. Pin Descriptions

Symbol	Type	Description
PCI BUS INTERFACE		+
Address and Data		
AD[31:0]	B	Multiplexed Address/Data Bus. A bus transaction (cycle) consists of an address phase followed by one or more data phases.
$\overline{\text{C/BE[3:0]}}$	I	Bus Command/Data Byte Enables. These signals carry the bus command during the address phase and the byte enables during the data phase.
Bus Control		
SCLK	I	PCI System Clock.
$\overline{\text{INTA}}$	O	Interrupt Request.
$\overline{\text{IRDY}}$	I	Initiator Ready. A bus data phase is completed when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted on the same cycle.
$\overline{\text{TRDY}}$	O	Target Ready. A bus data phase is completed when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted on the same cycle.
$\overline{\text{DEVSEL}}$	O	Device Select. 86CM65 drives this signal active when it decodes its address as the target of the current access.
IDSEL	I	Initialization Device Select. This input is the chip select for PCI configuration register reads/writes.
$\overline{\text{RESET}}$	I	System Reset. Asserting this signal forces the registers and state machines to a known state.
$\overline{\text{FRAME}}$	I	Cycle Frame. This signal is asserted by the bus master to indicate the beginning of a bus transaction. It is deasserted during the final data phase of a bus transaction.
PAR	O	Parity. 86CM65 asserts this signal to verify even parity during reads.
$\overline{\text{STOP}}$	O	Stop. 86CM65 asserts this signal to indicate a target disconnect.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Description
CLOCK CONTROL		
XIN	I	Reference Frequency Input. If an external 14.318 MHz crystal is used, it is connected between XOUT and this pin. A stable external frequency source can also be input via this pin. If this is done, the input must be the same voltage as AVDD. If PD11 is strapped low at power-on, this becomes the DCLK (dot clock) input, bypassing the internal oscillator. This is normally only used for test purposes.
XOUT	O	Crystal Output. This pin drives the crystal via an internal oscillator.
DISPLAY MEMORY INTERFACE		
Address and Data		
MA[9:0]	O	Memory Address Bus. The video memory row and column addresses are multiplexed on these lines. MA9 is output on pin M17 when the memory type is 512Kx32.
PD[63:0]	B	Display Memory Pixel Data Bus Lines 63:0. PD[28:0] are also used as the system configuration strapping bits, providing system configuration and setup information upon power-on reset. See Section 5 for a description of this function.
Memory Control		
$\overline{RAS0}$	O	Row Address Strobe.
$\overline{CAS[7:0]}$	O	Column Address Strobe Lines 7:0.
$\overline{WE}$	O	Write Enable.
$\overline{OE}$	O	Output Enable.
CRT VIDEO INTERFACE		
COMP		Compensation. This pin is tied to VDD through a 0.1 µF capacitor.
VREF		Voltage Reference. This pin is tied to VSS through a 0.1 µF capacitor.
RSET		Reference Resistor. This pin is tied to VSS through an external resistor to control the full-scale current value.
AR	O	Analog Red. Analog red output to the CRT monitor. In TV output mode (CR3D_0 = 1), the output is determined by the setting of CR3D_3-1.
AB	O	Analog Blue. Analog blue output to the CRT monitor.
AG	O	Analog Green. Analog green output to the CRT monitor. In TV output mode (CR3D_0 = 1), the output is determined by the setting of CR3D_3-1.
HSYNC	B	Horizontal Sync.
VSYNC	B	Vertical Sync.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Description
FLAT PANEL INTERFACE		
FPD[35:0]	O	Flat Panel Data. The meanings of these outputs vary depending on the type of panel. See Section 11 for tables listing all output combinations.
FPDE/ MOD	O	Flat Panel Display Enable/AC Modulation Signal. When a TFT panel is being driven, this is the display enable signal. When an STN panel is being driven, this is by default the display enable signal, which is not normally used but may be required for external panel control. If SR34_7 = 1, this is the AC modulation signal for those panels that require it.
FPSCLK	O	Flat Panel Shift Clock. This is the shift (dot) clock for LCD panels.
FPHSYNC/LP	O	Flat Panel HSYNC. This is the HSYNC signal for TFT panels and the LP (line pulse or new line start) signal for STN panels.
FPVSYNC/FLM	O	Flat Panel VSYNC. This is the VSYNC signal for TFT panels and the FLM (first line marker or new frame start) signal for STN panels.
FPPOL	O	Flat Panel Polarity. If SR1A_5 = 1, this signal tells the panel that the polarity of the data is reversed, thereby minimizing the number of data lines switching in each cycle. This is used in a few highly advanced panels. If SR1A_5= 0, this is the ROMEN output.
PWM	O	Pulse Width Modulation. This signal is output on pin M17 when the memory type is not 512Kx32 (CR68_6 = 1) and SR52_0 = 1.
FLAT PANEL POWER CONTROL		
ENAVDD	O	Enable VDD. This signal is driven high to external logic to initiate a flat panel power up sequence. It is driven low a programmable time (SR41_2) after the panel control signals and ENAVEE are driven low when 86CM65 is placed in Standby or Suspend Mode or if the flat panel is shut off via SR31_4.
ENAVEE	O	Enable VEE. This signal is driven high a programmable time (SR41_3) after ENAVDD is driven high during a flat panel power up sequence. This signals external logic to turn on the bias voltage to the flat panel. It is driven low when 86CM65 is placed in Standby or Suspend Mode or if the flat panel is shut off via SR40_4. This signals external logic to turn off the bias voltage to the flat panel.
STANDBY	I	Standby. If SR44_4 = 0, driving the STANDBY pin high initiates Standby mode and driving it low initiates exiting of Standby. If SR44_4 = 1, the system is always trying to go into Standby mode and 4 SCLK high pulses on the STANDBY pin either prevent this or take the system out of Standby, resetting the timer in either case.
SUSPEND	I	Suspend. This pin is active when SR42_0 = 1. A low to high transition initiates a Suspend mode sequence and a high to low sequence initiates exiting from Suspend mode.
CLK32	I	32 kHz Clock. An external TTL 32 kHz source is connected to this pin. It is used for panel power sequencing and video memory refresh when in Suspend mode.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Description
MISCELLANEOUS FUNCTIONS		
$\overline{\text{ROMEN}}$	O	ROM Enable. This signal provides the chip output enable input for BIOS ROM reads. It is multiplexed with the FPPOL signal and is selected when SR1A_5 = 0.
RA[15:0}	O	ROM Address Bus. These signals are multiplexed on PD lines. If a video BIOS is used, it must be immediately shadowed after boot up.
RD[7:0]	I	ROM Data Bus. These signals are multiplexed on PD lines. If a video BIOS is used, it must be immediately shadowed after boot up.
$\overline{\text{STWR}}$	O	Strobe Write. If SR1A_4 is set to 1, pin C3 acts as STWR. This signal is asserted whenever a write is made to CR5C. It is used to enable a General Output Port latch. MCLK is output instead of this signal if SR15_2 = 1. MCLK output is used only for test purposes.
GOP0	O	General Output Port. When SR1A_4 is cleared to 0, pin C3 acts as GOP0. The content of CR5C_0 is reflected on this pin when this bit is programmed.
SPCLK	I/O	Serial Port Clock. This is the clock for serial data transfer, either for I^2C or DDC2 monitor data communications. As an output, it is programmed via MMFF20_0. As an input, its status is read via MMFF20_2. In either case the serial port must be enabled by setting MMFF20_4 to 1. PD[26:25] can be strapped to allow I/O (E2H or E8H) port access to the Serial Port register while 86CM65 is disabled.
SPDAT	I/O	Serial Port Data. This is the data signal for serial data transfer, either for I^2C or DDC2 monitor data communications. As an output, it is programmed via MMFF20_1. As an input, its status is read via MMFF20_3. In either case the serial port must be enabled by setting MMFF20_4 to 1. PD[26:25] can be strapped to allow I/O (E2H or E8H) port access to the Serial Port register while 86CM65 is disabled.

Table 3-1. Pin Descriptions (Continued)

Symbol	Type	Description
ZV PORT		
LD[15:0]	I	Data. YUV input from PC Card
LCLK	I	Clock. PCLK input from PC Card
HS	I	HSYNC. HREF input from PC Card
VS	I	VSYNC. VSYNC input from PC Card
SCENIC HIGHWAY		
Scenic/MX2 Mode		
LD[7:0]	I/O	LPB Data. These lines carry compressed data to the Scenic/MX2 and video data from the Scenic/MX2.
LCLK	I	LPB Clock. This clock controls transactions between 86CM65 and the all Scenic Highway peripherals.
$\overline{\text{VREQ}}$/VRDY	O	Video Request/Ready. This signal is part of the the data transfer protocol between 86CM65 and the Scenic/MX2.
$\overline{\text{CREQ}}$/CRDY	I	Scenic/MX2 Request/Ready. This signal is part of the the data transfer protocol between 86CM65 and the Scenic/MX2.
LPBEN	O	LPB Device Enable. This signal is connected to the Scenic/MX2 chip enable input. The output level is controlled via SRD_0. This bit must be programmed to 1 to enable the Scenic/MX2.
Video 8 and 16 Modes		
LD[15:0]	I	LPB Data Bus [15:0]. Video data input. LD[7:0] are used for 8-bit interfaces.
HS	I	HSYNC. HSYNC input signaling the transition from one line to the next.
VS	I	VSYNC. VSYNC input signaling the transition from one frame to the next.
ODD	I	Odd/Even Field. High = odd field input from digitizer. Low = even field input. This input is active on pin M17 when the memory type is not 512Kx32 and SR52_0 = 0.
POWER AND GROUND		
VDDCORE	I	Analog power supply to the core logic
VDDCRT	I	Digital power supply to the CRT block pads
VDDFPI	I	Digital power supply to the flat panel block pads
VDDLPB	I	Digital power supply to the LPB block pads
VDDMEM	I	Digital power supply to the memory subsystem pads
VDDSYS	I	Digital power supply to the system bus interface pads
AVDD	I	Analog power supply (RAMDAC). This must be the same voltage as VDDCORE.
CLKAVDD[1:2]	I	Analog power supply (1 = MCLK synthesizer, 2 = DCLK synthesizer). This must be the same voltage as VDDCORE
VSSPAD	I	Digital ground (dirty)
VSSCORE	I	Digital ground (core)
VSSSUB	I	Digital ground (substrate)
AVSS	I	Analog ground

3.3 PIN LISTS

Table 3-2 lists all 86CM65 pins alphabetically. Table 3-3 lists all pins in numerical order.

Table 3-2. Alphabetical Pin Listing

Name	PIN(S)
AB	G2
AD[31:16]	V1, W1, V2, W2, Y1, Y2, U3, W3, U4, W4, V4, Y4, W5, V5, Y5, V6,
AD[15:0]	W8, U9, W9,V9, Y9, W10, V10, Y10, V11, Y11, W12, V12, Y12, W13, V13, Y13
AG	G1
AR	F2
AVDD	D1, F3, F4,
AVSS	C1, D3, E3, F1, G3,
$\overline{\text{CAS}}$[7:0]	Y14, W14, K18, J18, V14, U14, J19, H20
$\overline{\text{C/BE}}$[3:0]	V3, Y6, Y8, W11
CLK32	T1
CLKAVDD[1:2]	C2, E4
COMP	E2
$\overline{\text{CREQ}}$/CRDY	L1
$\overline{\text{DEVSEL}}$	W7
EMCLK	N1
EDCLK	A1
ENAVDD	A2
ENAVEE	B2
FLM	A3
FPD[35:27]	A14, B14, C14, D14, A13, B13, C13, A12, B12,
FPD[26:18]	C12, D12, A11, B11, C11, A10, B10, C10, A9,
FPD[17:9]	B9, C9, A8, B8, C8, D8, A7, B7, C7,
FPD[8:0]	A6, B6, C6, D6, A5, B5, C5, A4, B4
FPSCLK	B3
FPDE	B15
FPHSYNC	C4
FPPOL	C15
FPVSYNC	A3
$\overline{\text{FRAME}}$	W6
GOP0	C3
HS	K1
HSYNC	H1
IDSEL	Y3
$\overline{\text{INTA}}$	U2
$\overline{\text{IRDY}}$	V7
LCLK	M1
LD[15:0]	R2, R1, P4, P3, P2, P1, N3, N2, L3, L2, K3, K2, J3, J2, J1, H3
LP	C4

Table 3-2. Alphabetical Pin Listing (Continued)

Name	PIN(S)
LPBEN	N1
MA[9:0]	M17, L18, L19, M19, N18, N19, N20, M18, M20, L20
MOD	B15
ODD	M17
$\overline{OE}$	K19
PAR	V8
PD[63:48]	V16, W16, T17, U17, V17, W17, Y17, V15, W15, Y18, W18, V18, U18, T18, R18, P18,
PD[47:32]	C16, A17, B17, C17, D17, E17, G18, H18, H19, F18, E18, D18, C18, B18, A18, B16,
PD[31:16]	P19, R19, T19, U19, V19, W19, Y19, Y15, Y16, Y20, W20, V20, U20, T20, R20, P20,
PD[15:0]	A16, A19, B19, C19, D19, E19, F19, G19, G20, F20, E20, D20, C20, B20, A20, A15
PWM	M17
RA[15:0]	A16, A19, B19, C19, D19, E19, F19, G19, G20, F20, E20, D20, C20, B20, A20, A15
$\overline{RAS0}$	K20
RD[7:0]	Y16, Y20, W20, V20, U20, T20, R20, P20
$\overline{RESET}$	R3
$\overline{ROMEN}$	C15
RSET	E1
SCLK	U1
SPCLK	M2
SPDAT	M3
STANDBY	T2
$\overline{STOP}$	U8
$\overline{STWR}$	C3
SUSPEND	T3
$\overline{TRDY}$	Y7
VDDFPI	D5, D10, D13
VDDCORE	D16, K17, L4, U10
VDDCRT	G4
VDDLPB	J4
VDDMEM	G17, N17, U15
VDDSYS	T4, U7, U12
$\overline{VREQ}$/VRDY	K1
VREF	D2
VS	L1
VSSCORE	D9, D11, J17, K4, L17, M4, U11
VSSPAD	D4, D7, D15, F17, H4, H17, N4, P17, R4, U5, U6, U13, U16
VSSSUB	R17
VSYNC	H2
$\overline{WE}$	J20
XIN	A1
XOUT	B1

Table 3-3. Numerical Pin Listing

Number	Name	Number	Name
A1	XIN/EDCLK	C1	AVSS
A2	ENAVDD	C2	CLKAVDD1
A3	FPVSYNC/FLM	C3	$\overline{\text{STWR}}$/GOP0
A4	FPD1	C4	FPHSYNC/LP
A5	FPD4	C5	FPD2
A6	FPD8	C6	FPD6
A7	FPD11	C7	FPD9
A8	FPD15	C8	FPD13
A9	FPD18	C9	FPD16
A10	FPD21	C10	FPD19
A11	FPD24	C11	FPD22
A12	FPD28	C12	FPD26
A13	FPD31	C13	FPD29
A14	FPD35	C14	FPD33
A15	PD0/RA0	C15	FPPOL/ROMEN
A16	PD15/RA15	C16	PD47
A17	PD46	C17	PD44
A18	PD33	C18	PD35
A19	PD14/RA14	C19	PD12/RA12
A20	PD1/RA1	C20	PD3/RA3
B1	XOUT	D1	AVDD
B2	ENAVEE	D2	VREF
B3	FPSCLK	D3	AVSS
B4	FPD0	D4	VSSPAD
B5	FPD3	D5	VDDFPI
B6	FPD7	D6	FPD5
B7	FPD10	D7	VSSPAD
B8	FPD14	D8	FPD12
B9	FPD17	D9	VSSCORE
B10	FPD20	D10	FPFPI
B11	FPD23	D11	VSSCORE
B12	FPD27	D12	FPD25
B13	FPD30	D13	VDDFPI
B14	FPD34	D14	FPD32
B15	FPDE/MOD	D15	VSSPAD
B16	PD32	D16	VDDCORE
B17	PD45	D17	PD43
B18	PD34	D18	PD36
B19	PD13/RA13	D19	PD11/RA11
B20	PD2/RA2	D20	PD4/RA4

Table 3-3. Numerical Pin Listing (Continued)

Number	Name	Number	Name
E1	RSET	K1	VREQ/VRDY/HS
E2	COMP	K2	LD4
E3	AVSS	K3	LD5
E4	CLKAVDD2	K4	VSSCORE
E17	PD42	K17	VDDCORE
E18	PD37	K18	CAS5
E19	PD10/RA10	K19	OE
E20	PD5/RA5	K20	RAS0
F1	AVSS	L1	CREQ/CRDY/VS
F2	AR	L2	LD6
F3	AVDD	L3	LD7
F4	AVDD	L4	VDDCORE
F17	VSSPAD	L17	VSSCORE
F18	PD38	L18	MA8
F19	PD9/RA9	L19	MA7
F20	PD6/RA6	L20	MA0
G1	AG	M1	LCLK
G2	AB	M2	SPCLK
G3	AVSS	M3	SPDAT
G4	VDDCRT	M4	VSSCORE
G17	VDDMEM	M17	ODD/MA9/PWM
G18	PD41	M18	MA2
G19	PD8/RA8	M19	MA6
G20	PD7/RA7	M20	MA1
H1	HSYNC	N1	LPBEN/EMCLK
H2	VSYNC	N2	LD8
H3	LD0	N3	LD9
H4	VSSPAD	N4	VSSPAD
H17	VSSPAD	N17	VDDMEM
H18	PD40	N18	MA5
H19	PD39	N19	MA4
H20	CAS0	N20	MA3
J1	LD1	P1	LD10
J2	LD2	P2	LD11
J3	LD3	P3	LD12
J4	VDDLPB	P4	LD13
J17	VSSCORE	P17	VSSPAD
J18	CAS4	P18	PD48
J19	CAS1	P19	PD31
J20	WE	P20	PD16/RD0

Table 3-3. Numerical Pin Listing (Continued)

Number	Name	Number	Name
R1	LD14	V3	C/BE3
R2	LD15	V4	AD21
R3	RESET	V5	AD18
R4	VSSPAD	V6	AD16
R17	VSSSUB	V7	IRDY
R18	PD49	V8	PAR
R19	PD30	V9	AD12
R20	PD17/RD1	V10	AD9
T1	CLK32	V11	AD7
T2	STANDBY	V12	AD4
T3	SUSPEND	V13	AD1
T4	VDDSYS	V14	CAS3
T17	PD61	V15	PD56
T18	PD50	V16	PD63
T19	PD29	V17	PD59
T20	PD18/RD2	V18	PD52
U1	SCLK	V19	PD27
U2	INTA	V20	PD20/RD4
U3	AD25	W1	AD30
U4	AD23	W2	AD28
U5	VSSPAD	W3	AD24
U6	VSSPAD	W4	AD22
U7	VDDSYS	W5	AD19
U8	STOP	W6	FRAME
U9	AD14	W7	DEVSEL
U10	VDDCORE	W8	AD15
U11	VSSCORE	W9	AD13
U12	VDDSYS	W10	AD10
U13	VSSPAD	W11	C/BE0
U14	CAS2	W12	AD5
U15	VDDMEM	W13	AD2
U16	VSSPAD	W14	CAS6
U17	PD60	W15	PD55
U18	PD51	W16	PD62
U19	PD28	W17	PD58
U20	PD19/RD3	W18	PD53
V1	AD31	W19	PD26
V2	AD29	W20	PD21/RD5

Table 3-3. Numerical Pin Listing (Continued)

Number	Name
Y1	AD27
Y2	AD26
Y3	IDSEL
Y4	AD20
Y5	AD17
Y6	$\overline{C/BE2}$
Y7	$\overline{TRDY}$
Y8	$\overline{C/BE1}$
Y9	AD11
Y10	AD8
Y11	AD6
Y12	AD3
Y13	AD0
Y14	$\overline{CAS7}$
Y15	PD24
Y16	PD23/RD7
Y17	PD57
Y18	PD54
Y19	PD25
Y20	PD22/RD6

Section 4: Electrical Data

4.1 MAXIMUM RATINGS

Table 4-1. Absolute Maximum Ratings

Ambient temperature	0° C to 70° C
Storage temperature	-40° C to 125° C
DC Supply Voltage	-0.5V to 7.0V
I/O Pin Voltage with respect to V_{SS}	-0.5V to V_{DD}+0.5V

4.2 DC SPECIFICATIONS

Note: In all cases below, analog and digital VDD = 3.3V or 5V ± 5% and the operating temperature is 0° C to 70° C.

Table 4-2. RAMDAC/Clock Synthesizer DC Specifications

Symbol	Parameter	Min	Typical	Max	Unit
VREF	Internal voltage reference	1.10	1.235	1.35	V

Table 4-3. RAMDAC Characteristics

	Min	Typical	Max	Unit
Resolution Each DAC		8		bits
LSB Size		66		µA
Integral Linearity Error			± 1	LSB
Differential Linearity Error			± 1	LSB
Output Full-Scale Current	15.4	17.6	19.8	mA
DAC to DAC Mismatch			5%	
Power Supply Rejection Ratio			0.5	%/ % AVDD
Output Compliance	0.0		1.5	V
Output Capacitance			30	pF
Glitch Impulse		75		pV-Sec

Table 4-4. Digital DC Specifications (VDD = 3.3/5V ± 5%, Operating Temperature 0° C to 70° C)

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage	-0.5	0.8	V
V_{IH}	Input High Voltage	2.4	V_{DD} +0.5	V
V_{OL}	Output Low Voltage		V_{SS} + 0.4	V
V_{OH}	Output High Voltage	2.4		V
I_{OL1}	Output Low Current	4 (Note 1)		
I_{OH1}	Output Low Current	-2		
I_{OL2}	Output Low Current	6 (Note 2)		
I_{OH2}	Output Low Current	-3		
I_{OL3}	Output Low Current	8 (Note 3)		mA
I_{OH3}	Output High Current	-4		mA
I_{OL4}	Output Low Current	12 (Note 4)		
I_{OH4}	Output Low Current	-6		
I_{OL5}	Output Low Current	16 (Note 5)		mA
I_{OH5}	Output High Current	-8		mA
I_{OL6}	Output Low Current	24 (Note 6)		mA
I_{OH6}	Output High Current	-12		mA
I_{OZ}	Output Tri-state Current		1	µA
C_{IN}	Input Capacitance		5	pF
C_{OUT}	Output Capacitance		5	pF
I_{CC}	Power Supply Current		TBD (Note 7)	mA

Notes for Table 4-4

1. I_{OL1}, I_{OH1} for ENAVDD, ENAVEE
2. I_{OL2}, I_{OH2} for FPD[36:0], FPDE, FPPOL at 3.3V with SR40_0 = 0
3. I_{OL3}, I_{OH3} for pins $\overline{\text{ROMEN}}$, $\overline{\text{INTA}}$, $\overline{\text{STWR}}$, HSYNC, VSYNC, $\overline{\text{BLANK}}$, MA[8:0], $\overline{\text{CAS[7:0]}}$, PD[63:0], AD[31:0], LD[7:0], $\overline{\text{VREQ}}$/VRDY, SPCLK, SPD, FPD[36:0] (5V if SR40_0 = 0), FPVSYNC, FPHSYNC
4. I_{OL4}, I_{OH4} for FPD[36:0] FPDE, FPPOL at 3.3V with SR40_0 = 1
5. I_{OL5}, I_{OH5} for pins $\overline{\text{OE}}$, $\overline{\text{WE}}$, $\overline{\text{RAS[1:0]}}$, FPD[36:0] (5V if SR40_0 = 1)
6. I_{OL6}, I_{OH6} for pins PAR, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{TRDY}}$
7. I_{CC} measured for a resolution of 1024x768x8 with a 75 MHz DCLK and a 50 MHz MCLK at 25°C and 5V.
8. The pin names used in these notes are the primary ones. An output signal multiplexed on one of these pins has the same drive level.

4.3 AC SPECIFICATIONS

Note: All AC timings are based on an 80 pF test load.

4.3.1 RAMDAC AC Specifications

Table 4-5. RAMDAC AC Specifications

Parameter	Typical	Max	Unit	Notes
DAC Output Delay	5		ns	1
DAC Output Rise/Fall Time	3		ns	2
DAC Output Settling Time	15		ns	
DAC-to-DAC Output Skew	2	5	ns	3

Notes for Table 4-5

1. Measured from the 50% point of VCLK to the 50% point of full scale transition
2. Measured from 10% to 90% full scale
3 With DAC outputs equally loaded

Table 4-6. RAMDAC Output Specifications

Description	I_{OUT} (mA)	V_{OUT} (V)	BLANK	Input Data
White	17.6 typical	0.66 typical	1	FFH
Data	Data	Data	1	Data
Data (sync)	Data	Data	1	Data
Black	0	0	1	00H
Black (sync)	0	0	1	00H
BLANK	0	0	0	Don't Care

Note

1. Condition for V_{OUT} is a 75 Ohm doubly terminated load, RSET = 147 Ohms and use of internal VREF.

4.3.2 Clock Timing

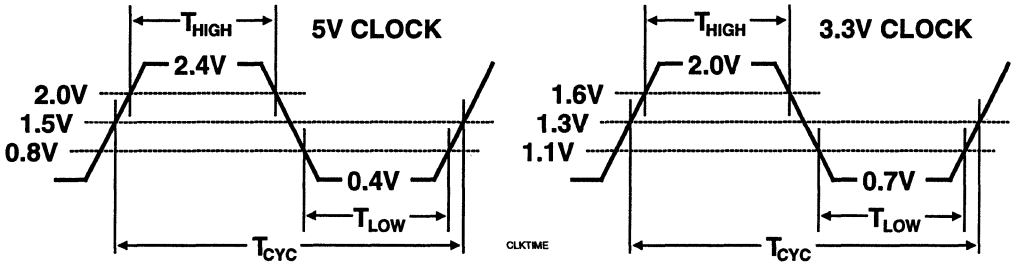


Figure 4-1. Clock Waveform Timing

Table 4-7. Clock Waveform Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{CYC}	SCLK Cycle Time	30	125	ns	1
	LCLK Cycle Time	30	200	ns	
	MCLK Cycle Time	20	100	ns	
	DCLK Cycle Time (VGA Mode)	25	100	ns	1
	DCLK Cycle Time (Enhanced Mode)	12.5	100	ns	1, 2
	FPDCLK Cycle Time	TBD	TBD	ns	
	CLK32 Cycle Time	TBD	TBD	ns	
T_{HIGH}	SCLK High Time	12	80	ns	
	LCLK High Time	12	160	ns	
	FPDCLK High Time	TBD	TBD	ns	
	CLK32 High Time	TBD	TBD	ns	
T_{LOW}	SCLK Low Time	12	80	ns	
	FPDCLK Low Time	TBD	TBD	ns	
	CLK32 Low Time	TBD	TBD	ns	
	LCLK Low Time	12	160	ns	
	SCLK Slew Rate	1	4	V/ns	3
	LCLK Slew Rate	1	4	v/nS	3
	FPDCLK Slew Rate	TBD	TBD	v/nS	
	CLK32 Slew Rate	TBD	TBD	v/nS	

Notes

1. $f_{DCLK} \geq 1/2\ f_{SCLK}$ to ensure valid writes to the PLLs.
2. For DCLK rates above 80 MHz, clock doubling is used. The maximum DCLK rate with clock doubling is 67.5 MHz.
3. Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to peak portion of the clock waveform.

4.3.3 Input/Output Timing

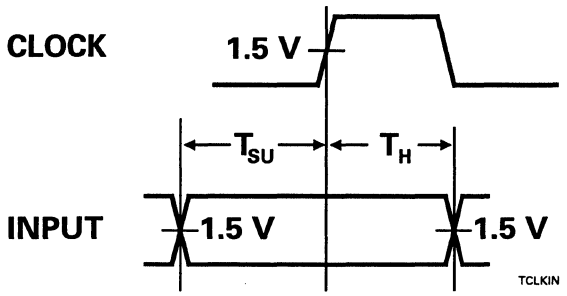


Figure 4-2. Input Timing

Table 4-8. SCLK-Referenced Input Timing

PCI Bus			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	AD[31:0], C/BE[3:0], FRAME, IRDY, IDSEL setup	7	ns
T_H	AD[31:0] hold	1	ns
T_H	C/BE[3:0], FRAME, IRDY, IDSEL hold	1	ns
T_{SU}	STANDBY setup	TBD	ns
T_H	STANDBY hold	TBD	ns

Table 4-9. CLK32-Referenced Input Timing

Symbol	**Parameter**	**Min**	**Units**
T_{SU}	SUSPEND setup	TBD	ns
T_H	SUSPEND hold	TBD	ns

Table 4-10. MCLK-Referenced Input Timing

Symbol	Parameter	Min	Units
T_{SU}	MD[63:0] setup to MCLK high (2-cycle EDO)	0	ns
T_H	MD[63:0] hold from MCLK high (2-cycle EDO)	12.5	ns
T_{SU}	MD[63:0] setup to following $\overline{CAS}$ low (1-cycle EDO)	0	ns
T_H	MD[63:0] hold from following $\overline{CAS}$ low (1-cycle EDO)	15	ns
T_{SU}	MD[63:0] setup to $\overline{CAS}$ high (fast page)	0	ns
T_H	MD[63:0] hold from $\overline{CAS}$ high (fast page)	15	ns

Note

1. The timing reference in each of the three cases above is to the event that causes the latching of the read data. The MCLK used to latch 2-cycle EDO data is an internal signal that cannot be directly observed. The $\overline{CAS}$ signals used to latch read data in the other operational modes are derived from the internal MCLK.

Table 4-11. LCLK-Referenced Input Timing

Scenic/MX2 Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[7:0] setup	10	ns
T_H	LD[7:0] hold	9	ns
T_{SU}	$\overline{CREQ}$/CRDY	6	ns
T_H	$\overline{CREQ}$/CRDY	8	ns
SAA7110 Interface			
Symbol	**Parameter**	**Min**	**Units**
T_{SU}	LD[7:0] setup (also LD[15:8] for 16-bit interface)	6	ns
T_H	LD[7:0] hold (also LD[15:8] for 16-bit interface)	8	ns
T_{SU}	HS setup	6	ns
T_H	HS hold	7	ns
T_{SU}	VS setup	6	ns
T_H	VS hold	7	ns
T_{SU}	ODD setup	TBD	ns
T_H	ODD hold	TBD	ns

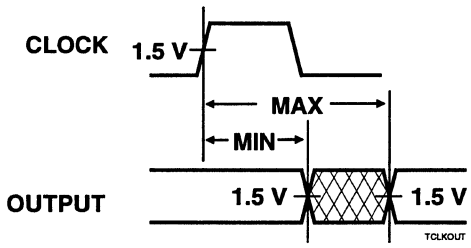


Figure 4-3. Output Timing

The minimum delay is the minimum time after the clock edge that the valid signal state from the previous cycle will begin transition to the next state (become invalid).

The maximum delay is the maximum time after the clock edge that the signal state is valid for the next cycle.

Table 4-12. SCLK-Referenced Output Timing

PCI Bus				
Parameter	**Min**	**Max**	**Units**	**Notes**
AD[31:0] valid delay	2	16	ns	1
$\overline{\text{DEVSEL}}$, PAR delay	2	11	ns	Medium $\overline{\text{DEVSEL}}$ timing used
$\overline{\text{STOP}}$ delay	2	11	ns	
$\overline{\text{TRDY}}$ delay	2	11	ns	
$\overline{\text{INTA}}$ delay	2	11	ns	

Note

1. Due to the timing for $\overline{\text{TRDY}}$ for read cycles, data is not sampled on the clock edge immediately following its becoming valid. This guarantees the PCI 2.0 specification time of 11 ns.

Table 4-13. CLK32-Referenced Output Timing

Parameter	**Min**	**Max**	**Units**	**Notes**
ENAVDD, ENAVEE active delay	TBD	TBD	ns	

Table 4-14. MCLK-Referenced Output Timing

Parameter	Min	Max	Units	Notes
PD[63:0] valid delay	2	7/11	ns	1
MA[8:0] valid delay	1.5	8	ns	
$\overline{\text{CAS}}$[7:0] active delay	1	5.5	ns	
$\overline{\text{CAS}}$[7:0] inactive delay	1	5.5	ns	
$\overline{\text{RAS0}}$ active delay	1	5	ns	
$\overline{\text{RAS0}}$ inactive delay	1	6.5	ns	
$\overline{\text{OE}}$ active delay	1.5	4.5	ns	
$\overline{\text{WE}}$ active delay	1.5	4.5	ns	

Note

1. The max delay is 7 ns for 1-cycle operation and 11 ns for 2-cycle operation.

Table 4-15. LCLK-Referenced Output Timing

Scenic/MX2 Interface				
Parameter	**Min**	**Max**	**Units**	**Notes**
$\overline{\text{VREQ}}$/VRDY active delay	2	11	ns	7 ns typ
LD[7:0] valid delay	2	15	ns	8 ns typ
LD[7:0] tri-state from LCLK	7	15	ns	

Table 4-16. FPSCLK-Referenced Output Timing

Parameter	Min	Max	Units	Notes
FPD[36:0] valid delay	0	10	ns	
FPDE, FPPOL, FPVSYNC, FPHSYNC active delay	0	10	ns	

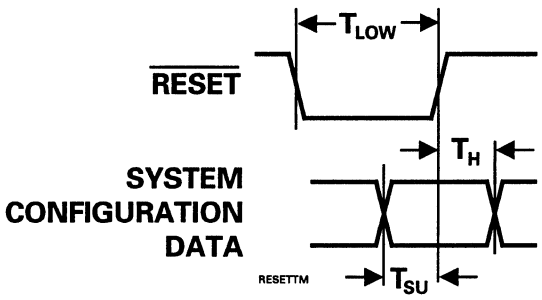


Figure 4-4. Reset Timing

Table 4-17. Reset Timing

Symbol	Parameter	Min	Units
T_{LOW}	$\overline{\text{RESET}}$ active pulse width	400	ns
T_{SU}	PD[28:0] setup to $\overline{\text{RESET}}$ inactive	20	ns
T_H	PD[28:0] hold from $\overline{\text{RESET}}$ inactive	10	ns

Section 5: Reset and Power Control

The RESET signal resets the internal state machines in the 86CM65 and places all registers in their power-on default states. All output pins are tri-stated except OE, which must be driven high to prevent the memory from driving data onto the power-on strapping pins described in the next section.

5.1 CONFIGURATION STRAPPING

The PD[28:0] pins are pulled low internally and can be individually pulled high through 10 KΩ resistors. These pull-ups and pull-downs do not affect normal operation of the pins as part of the pixel data bus, but they do force the pins to a definite state during reset. At the rising edge of the reset signal, this state is sampled, the result is inverted and the data loaded into the CR36, CR37, CR68 and CR6F registers. The data is used for system configuration. The definitions of the PD[28:0] strapping bits at the rising edge of the reset signal are shown in Table 5-1.

Important Note: As described above, the signal levels on PD[28:0] are inverted before being latched in the various strapping bit registers. Since PD[28:0] all have internal pull-downs, the default values for each of the strapping bits is 1. The value latched at reset can be changed to 0 by adding an external pull-up to the appropriate pin. After reset, the strapping bits are written and read normally, i.e., there is no inversion of the register values.

Strapping bits 7-5 define the display memory size. However, the BIOS determines this value directly and writes it to CR36_7-5 after reset. Therefore, systems do not need to strap the PD[7:5] pins. Other pins may also not require strapping, depending on the design.

5.2 BOUNDARY SCAN

Boundary scanning is enabled when PD9 is pulled high at reset. All digital pins become inputs except the SPCLK pin (M2) and the RESET pin (R3). SPCLK is the output pin for the boundary scan and RESET cannot be tested and must not be connected.

The tester drives high logic to all digital inputs. It then sequentially drives and holds each input low and records the state of the SPCLK pin. If all pin connections are good, the output will be perfect square wave. If this pattern is broken, the location of the incorrect signal level in the sequence identfies the bad connection.

Any sequence of the digital inputs can be used. The digital inputs to be tested are all pins except the following:

SPCLK
RESET
XIN
XOUT
VREF
COMP
RSET
AR
AB
AG
All analog and digital powers and grounds

Table 5-1. Definition of Strapping Bits at the Rising Edge of the Reset Signal

Note: The CR Bit Values in this table are the latched values as software would read or write them. To latch a 0 at reset, an external pull-up resistor must be connected to the appropriate PD pin as explained by the note on the previous page.

CR Bits	PD Pins	CR Bit Value	Function
CR36_1-0	**Reserved**		
	Memory Page Mode Select		
CR36_3-2	3-2	00	1-cycle extended data out (EDO) mode
		01	Reserved
		10	Extended data out (EDO) mode
		11	Fast page mode
CR36_4	**Reserved**		
	Display Memory Size		
CR36_7-5	7-5	000	4 MBytes (valid only with 512Kx32 DRAMs)
		001	Reserved
		010	Reserved
		011	Reserved
		100	2 MBytes
		101	Reserved
		110	1 MByte (valid only with 256Kx16 DRAMs)
		111	Reserved
CR37_0	**Reserved**		
	Boundary Scan		
CR37_1	9	0	Allows testing for bad solder connections
		1	Normal operation
CR37_2	**Reserved**		
	Clock Select		
CR37_3	11	0	Use external DCLK on the XIN and external MCLK on the LPBEN pin (test purposes only)
		1	Use internal DCLK, MCLK
CR37_4	**Reserved**		
	Panel Type		
CR37_7-5	15-13		OEM-specific coding for identifying up to 8 panel types
	$\overline{\text{CAS}}$/$\overline{\text{OE}}$ Low Stretch		
CR68_1-0	17-16	00	approximately 6.5 ns stretch (nominal)
		01	approximately 5 ns stretch (nominal)
		10	approximately 3.5 ns stretch (nominal)
		11	No stretch

Table 5-1. Definition of Strapping Bits at the Rising Edge of the Reset Signal (Continued)

CR Bits	PD Pins	CR Bit Value	Function
	$\overline{RAS}$ Low Timing Select		
CR68_2	18	0	4.5 MCLKs
		1	3.5 MCLKs
	$\overline{RAS}$ Pre-Charge Timing Select		
CR68_3	19	0	3.5 MCLKs
		1	2.5 MCLKs
	Memory Type Select		
CR68_6	22	0	512Kx32 DRAMs
		1	256Kx16 DRAMs
CR68_7-5	**Reserved**		
CR6F_0	**Reserved**		
	Serial Port I/O Address Select		
CR6F_1	25	0	Serial Port register mapped as I/O port at address 000E8H
		1	Serial Port register mapped as I/O port at address 000E2H
	Serial Port Address Type Select		
CR6F_2	26	0	Serial Port register mapped at the I/O port defined by PD25 or at its MMIO address (offset FF20)
		1	Serial Port register is accessed at its MMIO address (offset FF20) only (no I/O)
	$\overline{WE}$ Delay		
CR6F_4-3	28-27	00	3 units delay
		01	2 units delay
		10	1 unit delay
		11	no delay

5.3 FLAT PANEL POWER SEQUENCING

The flat panel may be damaged if the bias voltage VEE is applied to the liquid crystal material without enabling the control and data signals to the panel, which require VDD. the 86CM65 supplies the ENAVDD and ENAVEE signals to control power up/down sequencing of LCD panels. These signals drive external power management components which eventually drive panel VDD and panel VEE.

At the end of a power down sequence, the 86CM65 is in its idle power down state. This status is indicated by SR46_6. After power up or a system reset, 86CM65 stays in idle power down state. The BIOS must program SR42_5 = 1 to initiate software Standby, program all mode settings, then program SR42_5 = 0 to exit Standby. This initiates a power up sequence.

Sequencing timing is shown in Figure 5-1. The t_1 and t_2 values can each be programmed to 32 or 128 ms via bits 2 and 3 of SR41. The default is 32 ms for both t_1 and t_2.

At the end of a power up sequence, the 86CM65 is in its idle power up state. This status is indicated by SR46_7.

Enabling flat panel display (SR31_4 = 1) automatically generates a panel power up sequence. Disabling flat panel display (clearing SR31_4 to 0) automatically generates a panel power down sequence.

The PWM signal, whcih can control panel contrast, is also sequenced. See Figure 11-8.

5.4 POWER MANAGEMENT

The operational modes can be classified by the following three categories:

- Normal mode
- Standby mode
- Suspend mode

5.4.1 Normal Mode

During the Normal mode of operation, the flat panel is active. The CPU can access video memory and I/O registers and normal refresh to the video memory is provided. In this mode, the 86CM65 provides a number of automatic power management functions. These turn off power to certain internal blocks when these blocks are inactive.

5.4.2 Standby Mode

In Standby, the 86CM65 suspends all display-related memory activities. The CPU can still access video memory and I/O registers. In summary, the following occur in Standby mode:

- Most of the dot clocks (DCLKs) are gated off

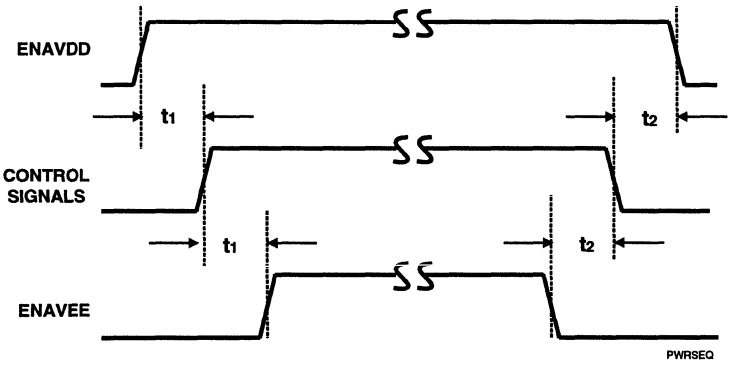


Figure 5-1. Flat Panel Power Sequencing

- No clock is provided to the CRT controllers
- The RAMDAC is in low-power mode
- The CPU can access and modify the video display memory and CLUTs

Standby mode is controlled by three different methods. These are:

- STANDBY input pin, a bit defining the operation of this pin and a hardware Standby enable bit
- Activity bit
- Software Standby bit

The function of the STANDBY pin is enabled when SR42 _4 is set to 1. The activity function is enabled by setting SR43_6 to 1. This means that internal chip activity (register access, Graphic Engine busy, etc.) is used as a criterion for entering or leaving Standby. Software Standby is controlled by SR42_5. Only one of these functions should be enabled/used at a time. Typically, the BIOS will use the software bit during mode changes, with both the hardware and activity enable bits disabled. After the mode is set, the BIOS will then disable software Standby and enable hardware Standby. The activity function provides additional flexibility and may not be required.

The second Standby setup function is to specify a timeout value controlling the time between initiation of Standby and the actual entering of that state. The Standby timer is programmed with a timeout value in SR43_5-0, with SR43_7 specifying whether the timeout value units are seconds or minutes.

The STANDBY pin has two operational modes. If SR44_4 = 0 and hardware Standby is enabled, the Standby sequence is initiated by a low to high transition on the STANDBY pin. This starts the timeout counter. If the STANDBY pin remains in a high logic state until the timer expires and a panel power down sequence is completed (see Section 5.3), the system enters Standby. If the STANDBY pin transitions from high to low before the idle power down state is reached, a power up sequence is generated (if required), the timer is reset and normal operation continues.

Once in Standby state, a high to low transition of the STANDBY pin initiates exiting of this state. This transition causes a panel power on sequence. When this is complete, normal operation is restored and the timer is reset.

If SR44_4 = 1, the Standby timeout counter begins counting when hardware Standby is enabled (SR42_4 = 1). If the STANDBY pin is not taken from low to high before the timer expires and the power down sequence is complete, the system enters Standby. Every rising edge of the Standby pin will either reset the timer (if not in Standby) or take the system out of Standby. Thus, in this mode, the STANDBY pin becomes an activity pin. As soon as Standby is exited and the power up sequence is complete, the Standby timer resets and starts counting again. The activity pulses on the STANDBY pin must be exactly 4 SCLKs wide.

Summarizing, if SR44_4 = 0, driving the STANDBY pin high initiates Standby mode and driving it low initiates exiting of Standby. If SR44_4 = 1, the system is always trying to go into Standby mode and 4 SCLK high pulses on the STANDBY pin either prevent this or take the system out of Standby, resetting the timer in either case.

If the activity function is enabled, this starts the timeout counter. If no internal chip activity is detected before the timer expires, a panel power down sequence is initiated. At the end of the power down sequence, the Standby state is entered. If activity is detected before the timer expires, the timer is reset and counting restarts. This sequence continues as long as the activity function is enabled. Once in Standby state, any chip activity causes a panel power on sequence. When this is complete, normal operation is restored except that the Standby timeout counter is again active.

If the software Standby bit (SR42_5) is set, this starts the timeout counter. If the bit is not cleared before the timer expires, the Standby state entry sequence is executed. If the software Standby bit is cleared before the timer expires, the timer is reset and normal operation continues. Once in Standby state, clearing the software Standby bit to 0 causes a panel power on sequence. When this is complete, normal operation is restored.

If Standby is initiated while any chip activity is in progress, any current transaction is completed first. If Standby is initiated after a Suspend request is initiated but before Suspend is entered, the Standby request will be delayed until after Suspend is exited.

If a power up sequence is requested while a power down sequence is being executed, it will be delayed and executed immediately after the power down sequence completes. Power up sequences do not use the timer. If the system is already in its idle power down state (CR46_6 reads 1) when a Suspend request is made, the power down sequence will not be done.

Standby mode status can be read via SR46 _5 (0 = off; 1 = on).

5.4.3 Suspend Mode

The following occur in Suspend mode:

- Register data bits are retained
- DCLK and MCLK oscillators are shut off
- No CPU accesses are allowed
- DRAM refresh clock rate set to 32 KHz
- All pins are deactivated except for the SUSPEND and DRAM control pins
- DAC and TV encoder are powered down

Suspend mode is controlled by two different methods. These are:

- SUSPEND input pin and a hardware Suspend enable bit
- Software Suspend bit

When hardware Suspend is used, the Suspend debounce timer is programmed with a value of 62.5 µs (SR42_7-6 = 00b) or 2 seconds (SR42_7-6 = 01b. Hardware Suspend is enabled by setting SR42_0 to 1. The Suspend sequence is initiated by a low to high transition of the SUSPEND pin. If after the debounce period, the SUSPEND pin is still high, a power down sequence is initiated (if the system is not already in its idle power down state) followed by entry to the Suspend state.

Software-initiated Suspend is entered by setting SR42_1 to 1. Since CPU access is not allowed in Suspend mode, exiting requires that the SUSPEND pin be driven from high to low. Exiting of Suspend clears SR42_1 to 0.

If supported by the DRAMs, slow DRAM refresh can be selected (SR29_7-6 = 01b or 10b). This uses the 32 KHz clock. If supported, the DRAM will be placed in self refresh mode (SR29_7-6 = 11b). The system BIOS must program the correct choice of refresh type supported by the DRAM.

The delay before the clock synthesizer PLLs are turned off is programmable via SR45_1-0.

If Suspend mode is initiated while any chip activity is in progress, any current transaction is completed first. If Suspend mode is initiated while the chip is in Standby mode, Standby is interrupted and resumed (assuming the request is still active) after leaving Suspend.

Hibernate mode is executed by the system. It is entered when the system reads the contents of the registers and DRAM and stores it to disk before activating Suspend. Once the data is saved, power to the 86CM65 can be turned off. The stored data is used after power-on reset to return the 86CM65 to its operating state before entering Hibernate mode.

5.5 MIXED 3.3 VOLT AND 5 VOLT OPERATION

The 86CM65 provides mixed 3.3V and 5V operation. The choice of voltage levels for the various subsystems is left to the system designer. Care must be taken that the choices are consistent with the choice of external components, e.g., 3.3V memory must be used if the memory power plane is supplied with 3.3V.

Only the RAMDAC power is directly programmable. The automatic setting is read from SR1B_0 (0 = 5V; 1 = 3.3V). The internal setting can be over ridden via SR1A_7 (0 = 3.3V; 1 = 5V).

The drive strength of the flat panel data output drivers can be set at 6 or 12 mA for 3.3V operation or at 8 or 16 mA for 5V operation. SR40_0 pro-

vides this option. The lower drive levels (6/8 mA) must be used with XGA panels.

5.6 GREEN PC SUPPORT

The 86CM65 provides support for the VESA Display Power Management Signaling (DPMS) protocol by allowing independent control of the HSYNC and VSYNC signals. To use this capability, the bit pattern xxxx0110b must be written to the SR8 register to unlock access to the SRD register. Bits 5-4 of SRD then control the state of HSYNC and bits 7-6 of SRD control the state of VSYNC.

Section 6: PCI Bus Interface

The pinout and other specifications for the 86CM65 are in complete conformance with Revision 2.1 of the the PCI specification. No glue logic is required.

6.1 PCI CONFIGURATION

The Vendor ID register (Index 00H) in the PCI Configuration space is hardwired to 5333H to specify S3 Incorporated as the vendor. The Device ID register is hardwired to 8811.

Bits 10-9 of the Status register (Index 06H) are hardwired to 01b to specify medium $\overline{\text{DEVSEL}}$ timing. The Class Code register (Index 08H) is hardwired to 30000xxH to specify that the 86CM65 is a VGA compatible device. Bits 3-0 of the Base Address 0 register (Index 10H) are hardwired to 00H. This indicates that the "prefetchable" bit is cleared to 0, the base register can be located anywhere in a 32-bit address space and the base register is located in memory space.

When the 86CM65 powers up in a PCI configuration, it defaults to linear addressing and memory mapped I/O enabled at a relocatable base address of 7000 0000H. This allows the PCI system to reconfigure as required for plug and play.

6.2 PCI CONTROLS

The 86CM65 provides several methods of controlling PCI Bus operation. PCI disconnects are enabled via CR66_3 and CR66_7. The RAMDAC snoop method is selected via CR34_0. PCI master abort handling during RAMDAC snooping can be disabled via CR34_1. PCI retry handling during RAMDAC snooping can be disabled via CR34_2. PCI read burst cycles can be disabled via CR3A_7.

Section 7: Display Memory

The 86CM65 supports a DRAM-based video frame buffer. This section describes the configurations supported, the functional timing for memory accesses and the operation of various register bits that affect memory timing and operation. It also describes how access to display memory is controlled to maximize graphics performance.

7.1 DISPLAY MEMORY CONFIGURATIONS

The 86CM65 uses fast page mode or extended data out (EDO) DRAMs for its frame buffer. EDO DRAMs must be capable of 1-cycle operation with the MCLK frequency used in the design. The type of DRAM operation used is specified via CR36_3-2, which can be programmed at reset via power-on strapping of PD[3:2]. The default is fast page.

Either 256Kx16 dual-$\overline{CAS}$ or 512Kx32 quad-$\overline{CAS}$-DRAMs are supported. These two types cannot be mixed. A Tech Note lists recommended DRAMs.

Figure 7-1 shows 1- and 2-MByte configurations using 256Kx16 DRAMS. Either fast page or EDO memory can be used. The PD bus with 1 MByte of memory is 32 bits. This reduces performance

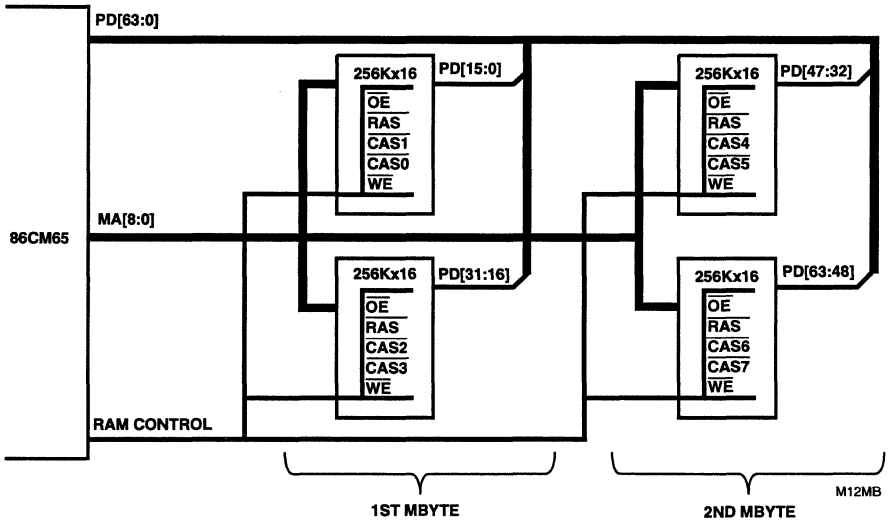


Figure 7-1. 256Kx16 DRAM Configurations

and the number of video modes available as compared with 64-bit PD bus operation.

Figure 7-2 shows 2- and 4-MByte configurations using 512Kx32 DRAMs. The PD bus with 2 MBytes of memory is 32 bits. This reduces performance and the number of video modes available as compared with 64-bit PD bus operation. Note that pin M17 is automatically configured as MA9 when 512Kx32 DRAMs are specified.

Table 7-1 Memory Size/PD Bus Width Specification

CR36_7-5	Mem. Type	Size/Width
001	256Kx16	1 MB/32-bitj
010	512Kx32	2 MB/32-bit
011	256Kx16	2 MB/64-bit
111	512Kx32	4 MB/64-bit

7.2 DISPLAY MEMORY REFRESH

The 86CM65 supports several DRAM refresh methods. For normal operation, it uses the standard $\overline{CAS}$ before $\overline{RAS}$ method. The functional timing for this can be found in any standard DRAM data book.

The number of refresh cycles performed per horizontal line is determined by bit 6 of CR11. If bit 2 of CR3A is set to 1, the number of refresh cycles per horizontal line is determined by the setting of bits 1-0 of CR3A. Refreshes are performed during the horizontal blanking period.

During power saving modes, 86CM65 supports slow refresh based on the 32 MHz clock or self-refresh, assuming the DRAMs can support these. The desired selection is made via SR29_7-6 as follows:

00 = Normal (8 ms)
01 = 16 ms slow refresh
10 = 64 ms slow refresh
11 = self-refresh

The system BIOS needs to be aware of the DRAM capabilities and set these bits appropriately.

7.3 DISPLAY MEMORY FUNCTIONAL TIMING

Figure 7-3 shows the functional timing for a fast page mode read cycle. This also shows how certain parameters for various control signals can be adjusted to meet the access time require-

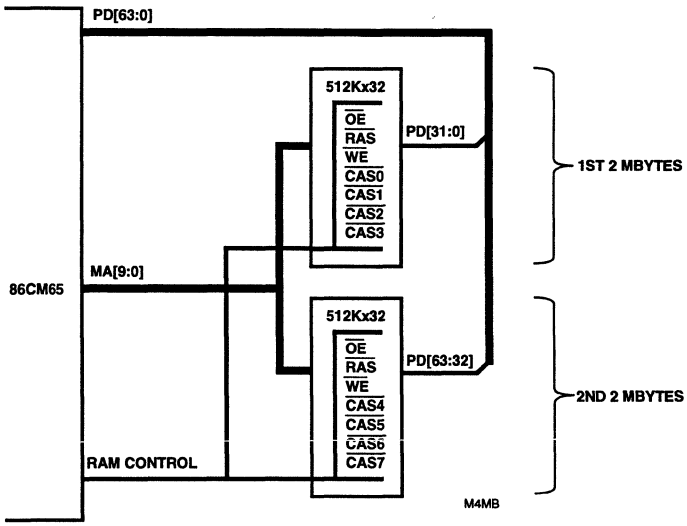


Figure 7-2. 512Kx32 DRAM Configurations

ments of a variety of DRAMs. Bits 1-0 of CR68 allow the pulse widths of the $\overline{CAS}$ and $\overline{OE}$ signals to be adjusted. Bit 2 of CR68 and bit 15 of MM81EC allow adjustment of the $\overline{RAS}$ low time. Bit 3 of CR68 and bit 16 of MM81EC allow adjustment of the $\overline{RAS}$ precharge (high) time. The settings in CR68 can be made by power-on strapping of PD[23:16] at reset. All settings can be changed by programming after reset.

Figure 7-4 shows the functional timing for a fast page mode write cycle. The $\overline{RAS}$ and $\overline{CAS}$ signals can be adjusted as explained for the read cycle above. The $\overline{WE}$ can be delayed via bits 4-3 of CR6F.

Figure 7-5 shows the functional timing for a fast page mode write follwing a read cycle. This is a 1-wait state cycle.

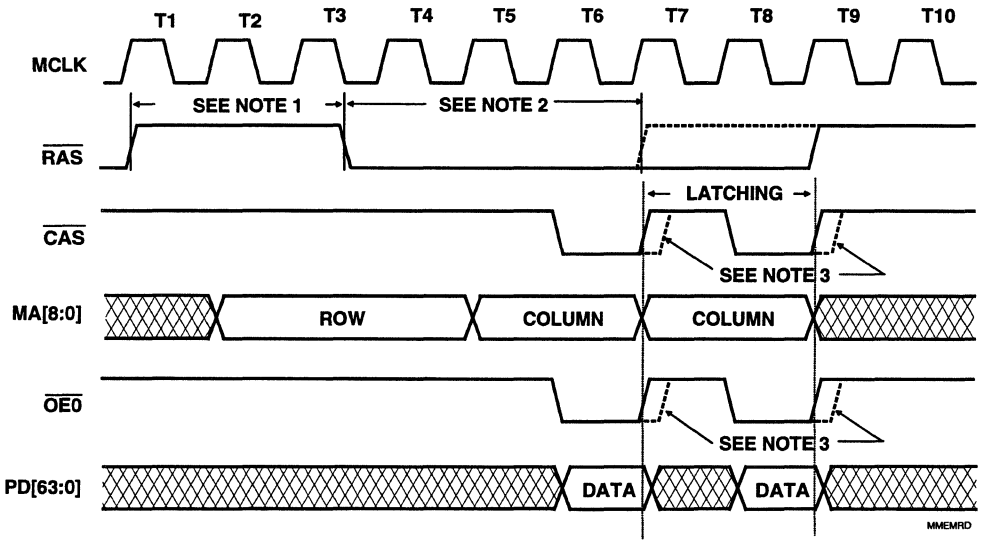


Figure 7-3. Fast Page Mode Read Cycle

Notes

1. The minimum $\overline{RAS}$ precharge time can be adjusted from 2.5 to 3.5 MCLKs via CR68_3, to 1.5 MCLKs via MM81EC_16, and reduced by 0.5 MCLK via CR58_7.
2. This figure shows a $\overline{RAS}$ low time for a single column access of 3.5 MCLKs. (The dashed line shows the $\overline{RAS}$ signal if the second page mode cycle were to be eliminated.) This $\overline{RAS}$ active time can be changed to 4.5 MCLKs via CR68_2 or to 2.5 MCLKs via MM81EC_15 and increased by 0.5 MCLK via CR58_7.
3. The $\overline{CAS}$ and $\overline{OE}$ active (low) times can be stretched via bits 1-0 of CR68.

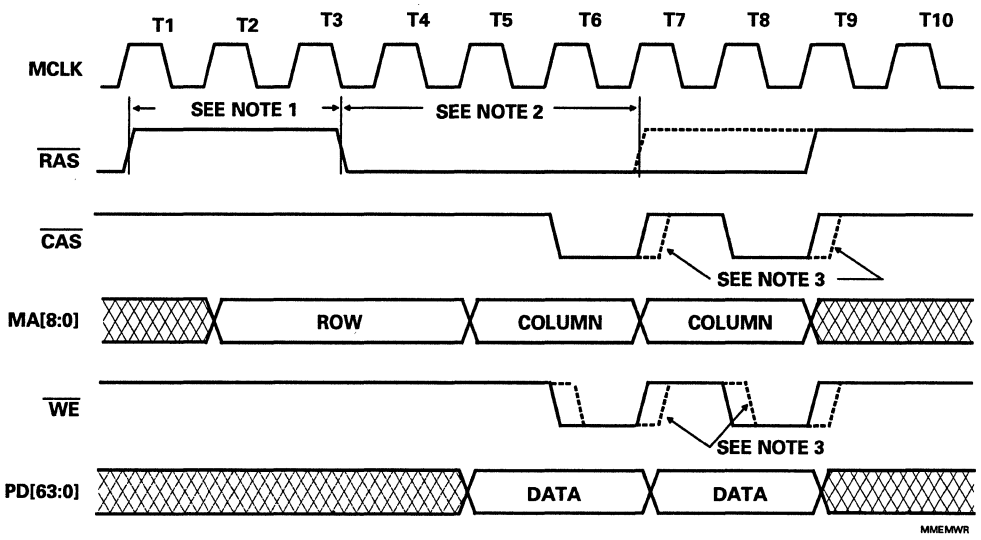


Figure 7-4. Fast Page Mode Write Cycle

Notes

1. The minimum $\overline{RAS}$ precharge time can be adjusted from 2.5 to 3.5 MCLKs via CR68_3, to 1.5 MCLKs via MM81EC_16, and reduced by 0.5 MCLK via CR58_7.
2. This figure shows a $\overline{RAS}$ low time for a single column access of 3.5 MCLKs. (The dashed line shows the $\overline{RAS}$ signal if the second page mode cycle were to be eliminated.) This $\overline{RAS}$ active time can be changed to 4.5 MCLKs via CR68_2 or to 2.5 MCLKs via MM81EC_15 and increased by 0.5 MCLK via CR58_7.
3. The $\overline{CAS}$ active (low) time can be stretched via bits 1-0 of CR68 and the $\overline{WE}$ active time delayed via bits 4-3 of CR6F.

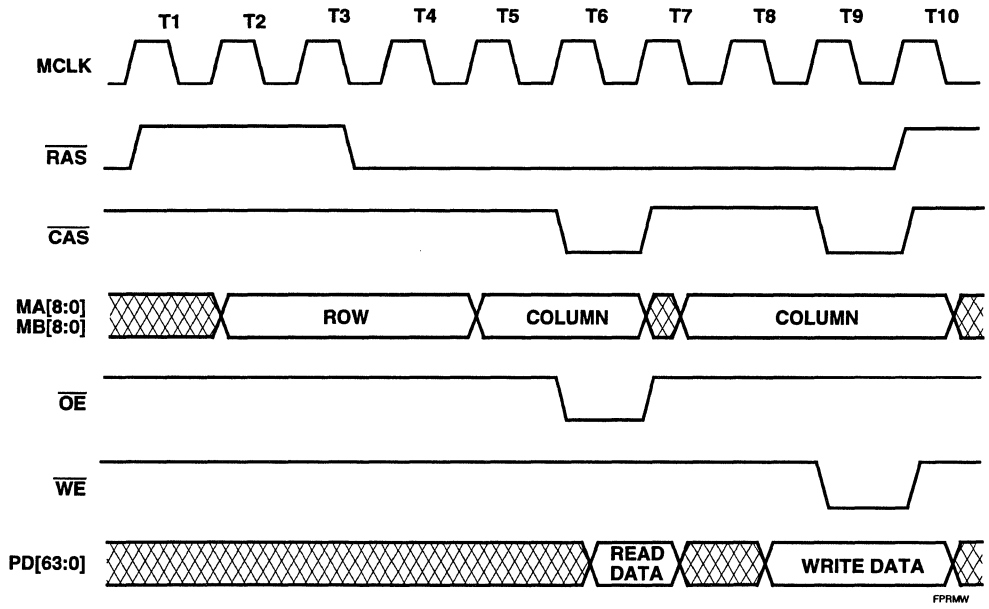


Figure 7-5. Fast Page Write Following a Read Cycle

If EDO memory is used, the 86CM65 must be configured for 1-cycle operation (CR36_3-2 = 11b). However, the 86CM65 will not always initiate 1-cycle operation. Some operations, such as linear addressing (direct CPU accesses to the frame buffer) are always done using 2-cycle EDO accesses.

Figure 7-6 shows the functional timing for a 2-cycle EDO mode read cycle. One difference between an EDO read cycle and a fast page mode read cycle is that EDO memory holds the data valid longer, allowing it to be latched one cycle later (rising edges of T8 and T10). This allows the use of slower access time memory or a faster MCLK. Therefore, the last page access (or first for a single access) is one MCLK longer. Note that

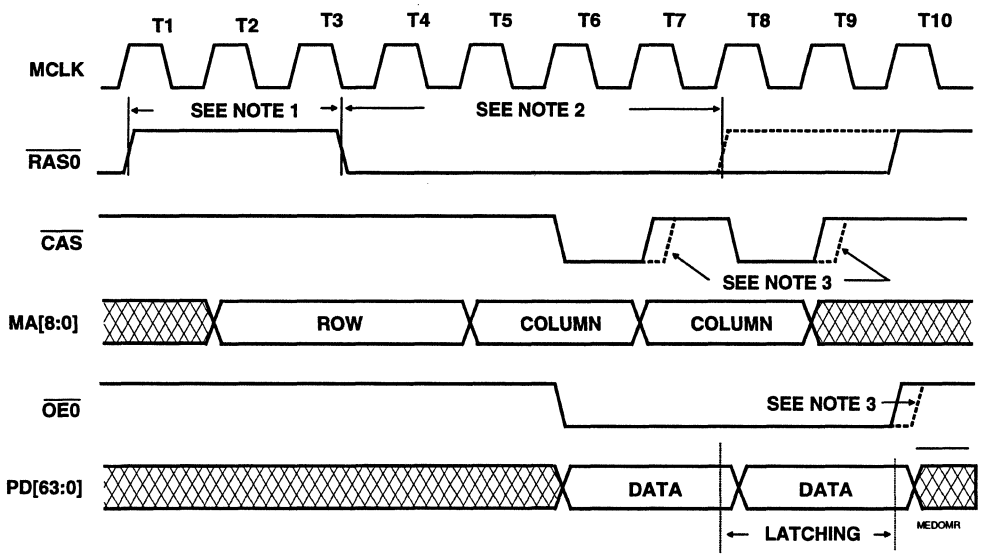


Figure 7-6. 2-cycle EDO Mode Read Cycle

Notes

1. The minimum $\overline{RAS}$ precharge time can be adjusted from 2.5 to 3.5 MCLKs via CR68_3, to 1.5 MCLKs via MM81EC_16, and reduced by 0.5 MCLK via CR58_7.
2. This figure shows a $\overline{RAS}$ low time for a single column access of 3.5 MCLKs. (The dashed line shows the $\overline{RAS}$ signal if the second page mode cycle were to be eliminated.) This $\overline{RAS}$ active time can be changed to 4.5 MCLKs via CR68_2 or to 2.5 MCLKs via MM81EC_15 and increased by 0.5 MCLK via CR58_7.
3. The $\overline{CAS}$ and $\overline{OE}$ active (low) times can be stretched via bits 1-0 of CR68.

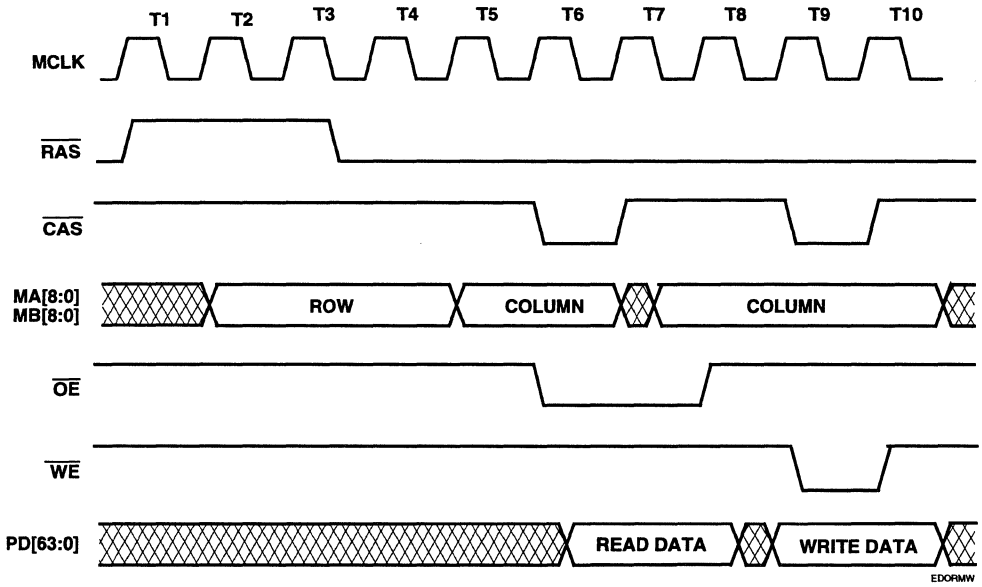


Figure 7-7. 2-cycle EDO Write Following a Read Cycle

$\overline{RAS}$, the last $\overline{CAS}$ and $\overline{OE}$ are all stretched the extra MCLK and $\overline{OE}$ is held low for the entire cycle instead of being pulsed as in a fast page mode cycle.

The timing adjustments for $\overline{RAS}$ and for $\overline{CAS}$/$\overline{OE}$/$\overline{WE}$ as described above for a fast page mode read cycle also apply to EDO cycles. Note that if the minimum $\overline{RAS}$ active time is specified as 3.5 MCLKs, the actual minimum for a single EDO read cycle will be 4.5 MCLKs.

A 2-cycle EDO write cycle is functionally the same as a fast page mode write cycle.

Figure 7-7 shows the functional timing for an EDO mode write following a read cycle. Since read data is latched later than for a fast page mode cycle, there is less time available between the read and write.

The functional timing for 1-cycle EDO reads and writes is provided by Figure 7-8. The DRAM drives valid read data after the $\overline{CAS}$ falling edge in T5. The chip latches the data on the next falling $\overline{CAS}$ edge. Note that a dummy cycle is required at the end to latch the last read. Write data is latched by the DRAM on the falling edge of $\overline{CAS}$. No dummy cycle is required, so $\overline{RAS}$ rises one cycle earlier than shown in Figure 7-8 and the last $\overline{CAS}$ shown in the figure does not occur.

Figure 7-9 shows a write following a read cycle with 1-cycle EDO operation. A dummy cycle is added between the read and write.

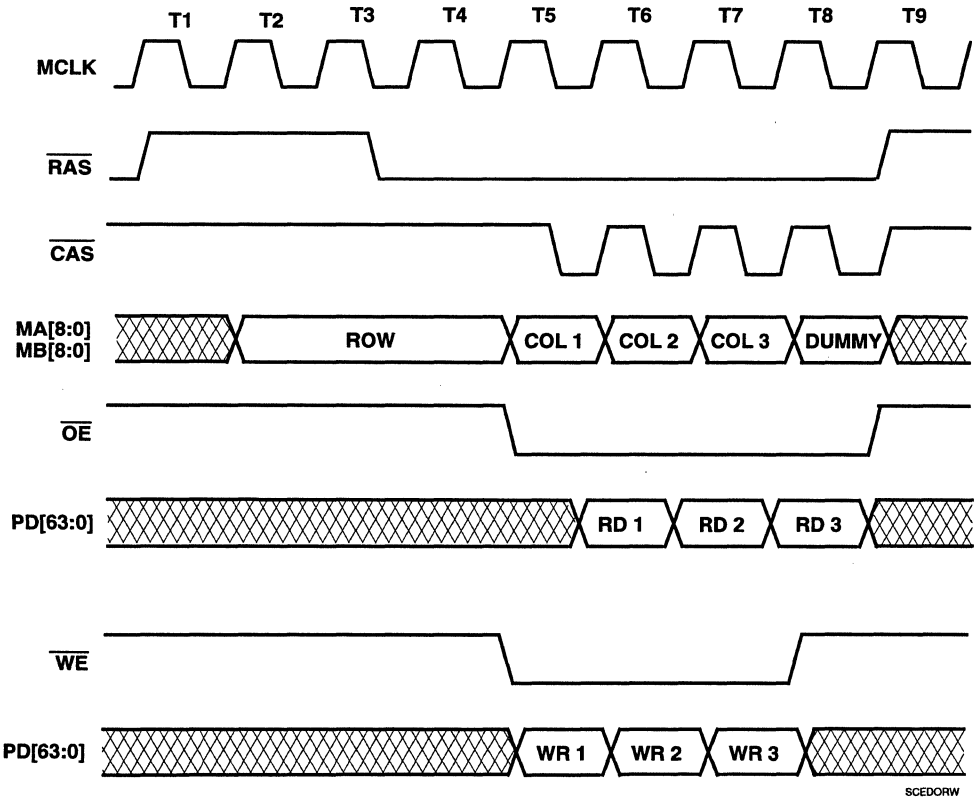


Figure 7-8. 1-Cycle EDO Mode Read/Write

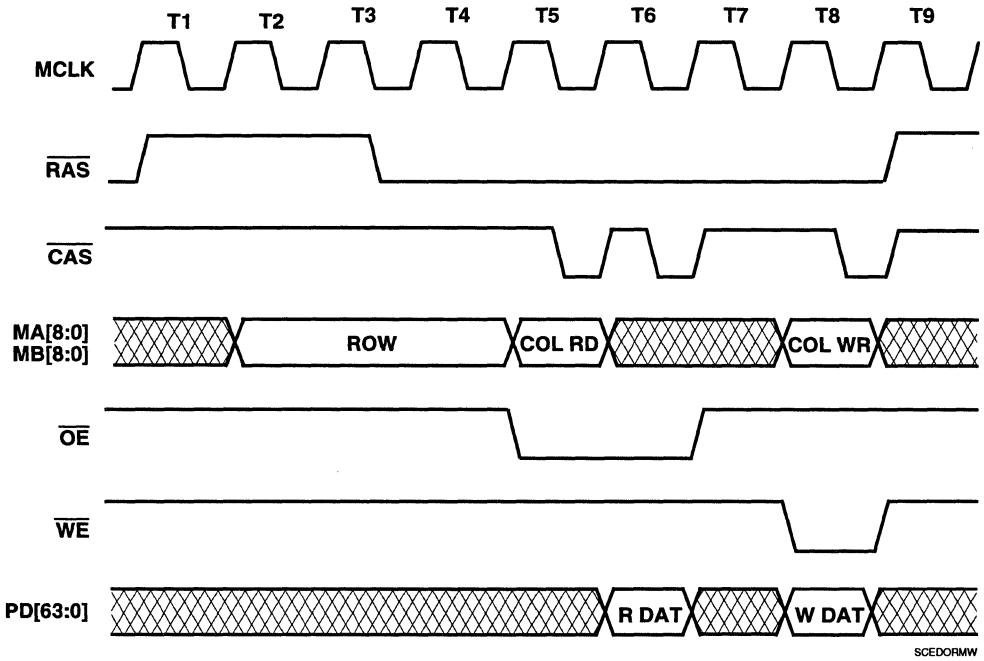


Figure 7-9. 1-cycle EDO Write Following a Read Cycle

7.4 DISPLAY MEMORY ACCESS CONTROL

A number of processes compete for access to display memory. These competing processes are (in decreasing order of access priority):

- Font fetch (text mode)
- Primary Stream high (N parameter)
- Secondary Stream high (N parameter)
- DRAM refresh
- Controller 2 high
- STN read high
- STN write high
- Hardware cursor fetch
- Hardware icon
- LPB writes (M parameter)
- CPU accesses (M parameter)
- Graphics Engine accesses (M parameter)
- Primary Stream low (N parameter)
- Secondary Stream low (N parameter)
- Controller 2 low
- STN read low
- STN write low

The processes with high and low priorities have associated threshold register fields (MM81EC, bits 14-10 and 9-5, SR29). If the current FIFO slots empty count is equal to or above the threshold level for a process, that process is given its low priority. Once the threshold is passed, the process is given its high priority.

The primary and secondary stream processes are responsible for screen refreshing and are associated with the N parameter. N parameters are provided for the following:

Primary Stream - CR60_7-0
Secondary Stream - CR72_7-0
Controller 2 - CR73_6-0
STN - CR75_7_0

RAM refresh and hardware cursor fetch occur during blanking when FIFO fetches are not occurring. (RAM refresh can also occur outside of the blanking interval.) The other processes are associated with the M parameter (CR54_2, 7-3 for the CPU and Graphics Engine, CR76_5-0 for the LPB). Note that these are not the same as the PLL M and PLL N parameters used to specify the clock synthesizer frequencies.

When the 86CM65 transfers data from display memory to the primary or secondary stream FIFO, the N parameter specifies the number of MCLKs available for FIFO filling before memory control is given up for M parameter processes. Note that this parameter is only effective when both FIFO threshold values are equal to or above the threshold level and therefore have low priority. Because of this, the FIFO threshold values have by far the greatest effect on performance. The N and M parameter settings will normally have little effect and can be left at their initial BIOS settings.

When N is effective and when N MCLKs have been used or the FIFO is filled, whichever comes first, the 86CM65 then allows the other display memory processes access to memory. Filling of the FIFO also stops at the end of active display. FIFO filling cannot begin again until the scan line position defined by the Start Display FIFO register (CR3B), which is normally programmed with a value 5 less than the value programmed in CR0 (horizontal total). This provides time during the horizontal blanking period for RAM refresh and hardware cursor fetch.

The M parameter specifies the number of MCLKs available for the processes shown in the bullet list above. When this number of MCLKs has occurred, memory control is returned for FIFO filling. If during the processing period controlled by the M parameter there is time when there are no memory access requests and the M value has not been reached, control is immediately returned to FIFO filling as specified by the N parameter.

Note that the M and N parameters should only be changed with the screen turned off. This is done by setting bit 5 of SR1 to 1.

Section 8: Clock Synthesis and Control

The 86CM65 contains two phase-locked loop (PLL) frequency synthesizers. These generate the DCLK (video clock) and MCLK (memory clock signals for the graphics controller block.

8.1 CLOCK SYNTHESIS

Each PLL scales a single reference frequency input on the XIN pin. By placing a parallel-resonant crystal between the XOUT output pin and the XIN pin, the reference frequency is generated by the 86CM65's internal oscillator. Alternately, a CMOS-compatible clock input can be connected to XIN to provide the reference frequency.

The frequency synthesized by each PLL is determined by the following equation:

$$f_{OUT} = \frac{(M+2)}{(N+2)\times 2^R} \times f_{REF}$$

where R = 0, 1, 2 or 3

Programmed PLL M and PLL N values should be consistent with the following constraints:

1. $135MHz \leq \frac{(M+2)f_{REF}}{(N+2)} \leq 270MHz$

2. min N ≥ 1

Note that values used for the parameters are the integer equivalents of the programmed value. In particular, the R value is the code, not the actual frequency divisor.

The PLL M value can be programmed with any integer value from 1 to 127 for MCLK and 1 to 255 for DCLK. The binary equivalent of this value is programmed in bits 6-0 of SR11 for the MCLK and in bits 7-0 of SR13, SR22 or SR24 for the DCLK. The PLL feedback loop frequency from the voltage controlled oscillator stage is scaled by dividing that frequency by (M+2).

The PLL N value can be programmed with any integer value from 1 to 31 for MCLK or 1 to 63 for DCLK. The binary equivalent of this value is programmed in bits 4-0 of SR10 for the MCLK and in bits 5-0 of SR12, SR21 or SR23 for the DCLK. The reference frequency is divided by (N+2) before being fed to the phase detector stage of the PLL.

The PLL R value is a 2-bit range value that can be programmed with any integer value from 0 to 3. The R value is programmed in bits 6-5 of SR 10 for MCLK and bits 7-6 of SR12, SR21 or SR23 for DCLK. This value codes the selection of a frequency divider for the PLL output. This is shown Table 8-1.

Table 8-1. PLL R Parameter Decoding

R-Range Code	Frequency Divider
00	1
01	2
10	4
11	8

The entire PLL block diagram is shown in Figure 8-1.

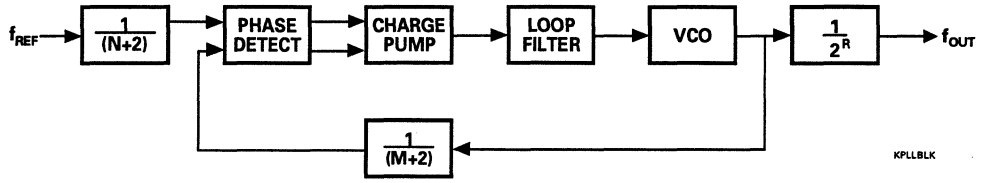


Figure 8-1. PLL Block Diagram

The following sequence may be followed to arrive at M and N values for any mode.

1. Calculate an R which does not violate the following constrains:

   $135MHz < 2^R \times f_{OUT} \leq 270MHz$

2. Start with N1 = 1 and calculate:

   $$M = [\frac{f_{OUT} \times (N+2) \times 2^R}{f_{REF}}] - 2$$

3. Determine if the following constraint is met:

   $$0.995\ f_{OUT} < \frac{(M+2)\ f_{REF}}{(N+2)\ 2^R} < 1.005\ f_{OUT}$$

4. If the constraint in step 3 is met, the M and N values used will generate the desired frequency (within the specified tolerance). If the constrain is not met, repeat steps 2 and 3 with N increased by 1 each time until the constraint in step 3 is met. Note that multiple combinations of M and N are possible for a given output frequency.

8.2 CLOCK REPROGRAMMING

If 3C2_3-2 = 00b, the DCLK PLL parameters are taken from SR22 and SR23. The default values generate a frequency of 25.125 MHz. This is the DCLK frequency generated at power on to support standard VGA operation.

If 3C2_3-2 = 01b, the DCLK PLL parameters are taken from SR24 and SR25. The default values generate a frequency of 28.322.

For Enhanced mode operation, 3C2_3-2 are programmed to 11b and the DCLK PLL values are taken from SR12 and SR13. No default values are defined for these registers.

New DCLK PLL parameter values can be programmed at any time. They can be loaded in one of two ways. If bit 5 of SR15 is cleared to 0, the new DCLK frequency is loaded by setting bit 1 of SR15 to 1. Bit 1 of SR15 should be left at a value of 1. Actual loading will be delayed for a short but variable period of time.

The alternate approach to loading the new DCLK frequency is to toggle bit 5 of SR15 by programming it to a 1 and then a 0. This immediately loads the DCLK (and MCLK) frequencies (no variable delay). For example, pseudocode to change DCLK to the frequency specified by PLL parameter values of 34H and 56H is:

```
3C2 ⇐ 6FH  ; DCLK specified by
           ; SR12 and SR13
3C4 ⇐ 12H  ; SR12 index
3C5 ⇐ 34H  ; SR12 PLL value
3C4 ⇐ 13H  ; SR13 index
3C5 ⇐ 56H  ; SR13 PLL value
3C4 ⇐ 15H  ; SR15 index
3C5 ⇐ RMW  ; Use read/modify/write to
           ; set bit 5 to 1 and leave
           ; other bits unchanged
3C5 ⇐ RMW  ; Use read/modify/write to
           ; clear bit 5 to 0 and
           ; leave other bits
           ; unchanged
```

Either loading approach should work. The second (immediate loading) approach helps with system testing since the timing of the load is predictable. The first approach (via bit 1 of SR15) has the advantage of separating the loading of DCLK from that of MCLK.

After power-up, all MCLK frequency changes must be made by re-programming SR10 and SR11. If bit 5 of SR15 is cleared to 0, the new frequency does not take effect until a 1 has been written to bit 0 of SR15. This bit must then be cleared to 0 to prevent repeated loading. Actual loading will be delayed for a short but variable period of time.

As explained above for DCLK, toggling bit 5 of SR15 (0,1,0) immediately loads both the DCLK values in the register pair selected by 3C2_3-2 and the MCLK values in SR10 and SR11.

8.3 CLOCK SELECTION AND CONTROL

MCLK is used to drive the memory interface and Graphics Engines. It normally is the MCLK generated by the internal clock synthesizer. However, other clocks can be used as well as shown in Figure 8-2. SR27_3-0 are programmed to make the selection.

DCLK is generated by the internal clock synthesizer. DCLK1 is the pixel rate associated with the controller 1 path. This is the path that includes the Streams Processor. DCLK2 is the pixel rate associate with the controller 2 path. How these are derived is shown in Figure 8-2. The first MUX selection is made via SR28_3-2 and the second via SR28_7-4.

Bit 0 of CR67 provides the option to invert DCLKA.

In color mode 8, the internal RAMDAC requires two clocks. The normal internal DCLK frequency is divided by two via bit 4 of SR15 to provide the standard pixel clock input. Undivided DCLK1 provides the other input. This clock can be inverted via bit 6 of SR15.

Certain 4 bits/pixel modes require that DCLK1 be halved. This is done with bit 6 of AR10 set to 1 and bit 4 of CR3A cleared to 0 and is enabled by setting bit 4 or SR15 to 1.

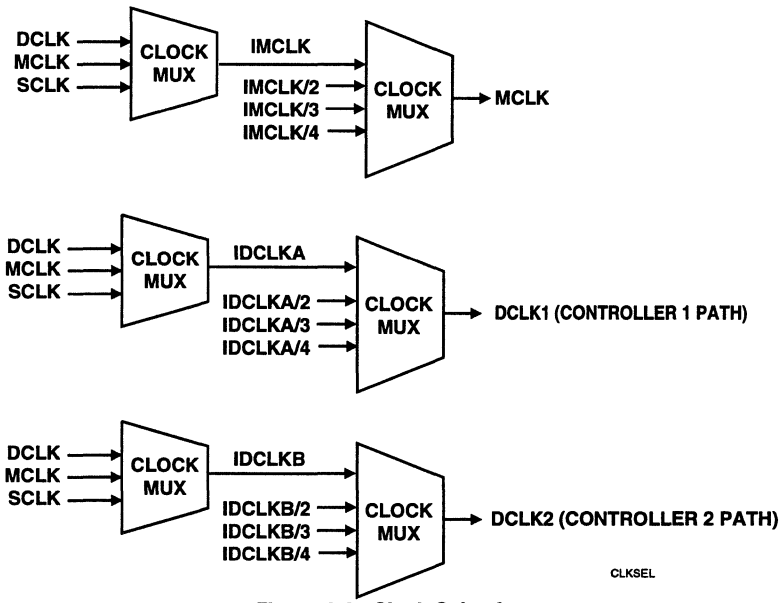


Figure 8-2. Clock Selection

Section 9: Streams Processor

The S3 Streams Processor processes data from the graphics frame buffer, composes it and outputs the result to the internal DACs for generation of the analog RGB outputs to the monitor. The general data flow is shown in Figure 9=1. Note that the DAC shown in this figure is inside the 86CM65.

9.1 INPUT STREAMS

The processor can compose data from up to 4 independent streams as shown in Figure 9=1.

1. Primary Stream - RGB graphics data
2. Secondary Stream - RGB or YUV/YCbCr (video) data from another region within the frame buffer
3. Hardware Icon - 64x64x4 (or 128x128x2).
4. Hardware Cursor - 64x64x2 cursor, either Microsoft or X-11 definition.

Regardless of the input formats, the Streams Processor creates a composite RGB-24 (8.8.8) output to the DACs. This means that, for example, RGB-8 pseudo-color graphics data can be overlaid with true-color-equivalent (24 bits/pixel) video data. The result is improved video quality and/or reduced memory bandwidth requirements as compared with systems that require both graphics and video to be stored in the same

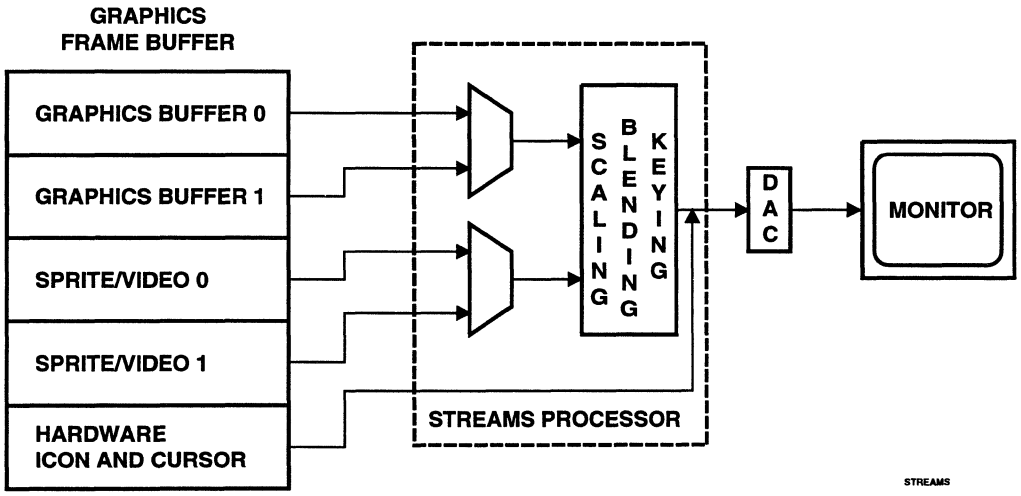


Figure 9-1. Streams Processor

frame buffer format. In certain modes, the Streams Processor also saves memory bandwidth by eliminating the need to save and restore the overlay background since the background (primary stream) is never overwritten in the frame buffer.

Streams Processor support is not available for clock-doubled 8 bits/pixel modes, interlaced graphics modes and standard VGA modes except for modes D, E, 10, 12 and 13.

Bits 3-2 of CR67 specify the Streams Processor mode of operation. If they are cleared to 00b, Streams Processor operation is disabled. They are programmed to 01b when the primary stream is VGA mode D, E, 10, 12 or 13 (the only supported modes). A secondary stream can be overlaid on the primary stream. CR67_3-2 are set to 11b to support an Enhanced mode primary stream and a secondary stream.

9.1.1 Primary Stream Input

The primary stream is generated by reading the RGB pixel data written to the frame buffer by the graphics controller. The format for this data can be any of the following as selected via bits 26-24 of MM8180.

- RGB-8 (Although not shown in Figure 1, the frame buffer data is first passed through the internal RAMDACs color lookup table (CLUT), where it is palettized before being passed to the Streams Processor.
- KRGB-16 (1.5.5.5) - The K bit is the color key.
- RGB-16 (5.6.5)
- XRGB-32 (X.8.8.8) - X is the ignored upper byte.

9.1.2 Secondary Stream Input

The secondary stream is generated by reading pixel data from a separate section of the frame buffer than that used to generate the primary screen. This might be RGB data written by the graphics controller, such as a sprite used by game programmers for moving objects. It could also be RGB, YUV or YCbCr data written to the frame buffer by some video source (CPU, decoder, digitizer). The format for this data can be any of the following as selected via bits 26-24 of MM8190.

- YCbCr-16 (4.2.2), 16 - 240 input range
- YUV-16 (4.2.2), 0 -255 input range
- KRGB-16 (1.5.5.5) - The K bit is the color key.
- YUV (2.1.1)
- RGB-16 (5.6.5)
- XRGB-32 (X.8.8.8) - X is the ignored upper byte.

The data can be passed through unscaled or scaled up horizontally and vertically by an arbitrary amount. YCbCr/YUV data is color space converted and all data is converted to RGB-24 (8.8.8) format.

9.1.3 Hardware Icon and Cursor Generation

Hardware icon and cursor generation is explained in Section 16. The icon overlays everything but the cursor. The cursor overlays all other image sources.

9.1.4 Frame Buffer Organization/ Double Buffering

For each stream to be used, the starting location (offset) in the frame buffer and the stride (byte offset between vertically adjacent pixels on the screen) must be specified. Both the primary and the secondary streams can be double buffered as depicted in Figure 9=1. This means that duplicate frame buffer storage can be provided for both the primary and secondary image (or for either one of them). With double buffering, the programmer can rapidly switch from one primary or secondary image to the other. In addition, having two images allows more time for updating one image while the other is being displayed. Defining the frame buffer organization and implementing double buffering are done via the register fields described in Table 4-1. LPB stands for Local Peripheral Bus.

Table 9=1. Register Fields Used For Specifying Frame Buffer Organization and Double Buffering

Register Field	Description
MM81C0_21-0	Primary Display Buffer Address 0. This is the starting address (offset) in the frame buffer for 1 primary graphics image.
MM81C4_21-0	Primary Display Buffer Address 1. This is the starting address (offset) in the frame buffer for a second primary graphics image.
MM81C8_11-0	Primary Stream Stride. This is the byte offset in the frame buffer from a pixel in a given primary image display line to the pixel directly below it on the next display line. The stride must be the same for both primary buffers.
MM81CC_0	Primary Stream Buffer Select 0 = Primary frame buffer starting address 0 (MM81C0_21-0) used for primary stream 1 = Primary frame buffer starting address 1 (MM81C4_21-0) used for primary stream
MM81CC_2-1	Secondary Stream Buffer Select 00 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream 01 = Secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream 10 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by LPB starting address register selected by bit 4 of this register. 11 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bit 4 of this register.
MM81CC_4	LPB Input Buffer Select 0 = LPB frame buffer starting address 0 (MMFF0C_21-0) used for LPB input 1 = LPB frame buffer starting address 1 (MMFF10_21-0) used for LPB input
MM81CC_5	LPB Input Buffer Select Loading 0 = The value programmed in bit 4 of this register takes effect immediately 1 = The value programmed in bit 4 of this register takes effect at the end of the next frame (completion of writing all the data for a frame into the frame buffer)
MM81CC_6	LPB Input Buffer Select Toggle 0 = End of frame (completion of writing all the data fro a from into the frame buffer) has no effect on the setting of bit 4 of this register 1 = End of frame causes the setting of bit 4 of this register to toggle

Table 9=1. Register Fields Used For Specifying Frame Buffer Organization and Double Buffering (continued)

Register Field	Description
MM81CC_7	Dropped Frame Writing 0 = The dropped frames specified in bits 10-8 of this register are written to the frame buffer 1 = The dropped frames specified in bits 10-8 of this register are not written to the frame buffer
MM81CC_10-8	Frame Dropping Value = 1 less than the number of frames to drop between captured frames Bit 7 of this register determines whether or not the dropped frames are written to the frame buffer.
MM81D0_21-0	Secondary Display Buffer Address 0. This is the starting address (offset) in the frame buffer for 1 secondary graphics or video image.
MM81D4_21-0	Secondary Display Buffer Address 0. This is the starting address (offset) in the frame buffer for a second secondary graphics or video image.
MM81D8_11-0	Secondary Stream Stride. This is the byte offset in the frame buffer from a pixel in a given secondary image display line to the pixel directly below it on the next display line. The stride must be the same for both secondary buffers.
MMFF0C_21-0	LPB Frame Buffer Address 0. This is the starting address (offset) in the frame buffer for one image buffer into which is written data from the LPB. The secondary stream can be generated from this buffer.
MMFF10_21-0	LPB Frame Buffer Address 1. This is the starting address (offset) in the frame buffer for a second image buffer into which is written data from the LPB. The secondary stream can be generated from this buffer.
MM81CC_6	LPB Input Buffer Select Toggle 0 = End of frame (completion of writing all the data fro a from into the frame buffer) has no effect on the setting of bit 4 of this register 1 = End of frame causes the setting of bit 4 of this register to toggle

The secondary stream can be generated from data written to the frame buffer via the LPB when LPB mode is enabled. In this case, the Secondary Display Buffer Address 0 and the LPB Frame Buffer Address 0 will normally be the same, as will the Address 1's for both the secondary stream and the LPB input if double buffering is used. The various LPB control bits described in Table 9=1 allow complete hardware control of the capture and display of video data using either single or double buffering.

9.2 INPUT PROCESSING

Different processing options are available for the primary and secondary input streams. These are explained next.

9.2.1 Primary Stream Processing

The primary stream input RGB format is converted (if required) to RGB-24 (8.8.8) format. Each color byte is padded as required with low order zeros. After this conversion, the data can be passed through unscaled or scaled up horizontally and vertically by a factor of 2 via bits 30-28 of MM8180. For MM8180_30-28 = 001, horizontal scaling is done via replication. If these bits are programmed to 010, horizontal scaling is done using interpolation. Vertical scaling is automatic and uses line replication. The 2x scaling allows a 320x240 image (as used by many games) to be displayed at a full-screen 640x480 resolution.

9.2.2 Secondary Stream Processing

The secondary stream input format is converted (if required) to RGB-24 (8.8.8) format. For YUV/YCbCr inputs, the required color space conversion is automatically performed. Before conversion, the data can be passed through unscaled or scaled up horizontally and/or vertically by arbitrary factors. Horizontal scaling uses filtering for interpolation. Vertical scaling uses line replication. The register fields involved in scaling up the secondary stream are described in Table 9=2. Figure 9=2 graphically describes the various fields.

For example, assume a 10x10 window that is to be scaled up horizontally by a factor of 2.5. The filter characteristics are set for bi-linear (2x to 4x stretch). The starting line width is 10 pixels and the ending line width is 25 pixels. The DDA horizontal accumulator initial value is 2 (10-1) - (25-1) = -6. The K1 horizontal factor is 10-1 = 9. The K2 horizontal factor is 10-25 = -15. Programming these parameters with these values results in a 2.5x horizontal stretch for the secondary stream window.

9.3 COMPOSITION/OUTPUT

A variety of output types can be composed from the streams described above. The compose modes are:

1. MM81A0_26-24 = 000b - Secondary stream overlaid on the primary stream in an opaque rectangular window. This is the default mode and can be used, for example, for a video window overlaying the graphics screen. Note that this mode will not work for the case where the user needs to pull down a graphics window over the video since the graphics window is defined as being under the video window. Color keying (number 5 in this list) must be used for this purpose.
2. MM81A0_26-24 = 001b - Primary stream overlaid on the secondary stream in an opaque rectangular window. This could be used, for example, to provide graphics captions for a video window. The video is not visible behind the rectangular graphics window.

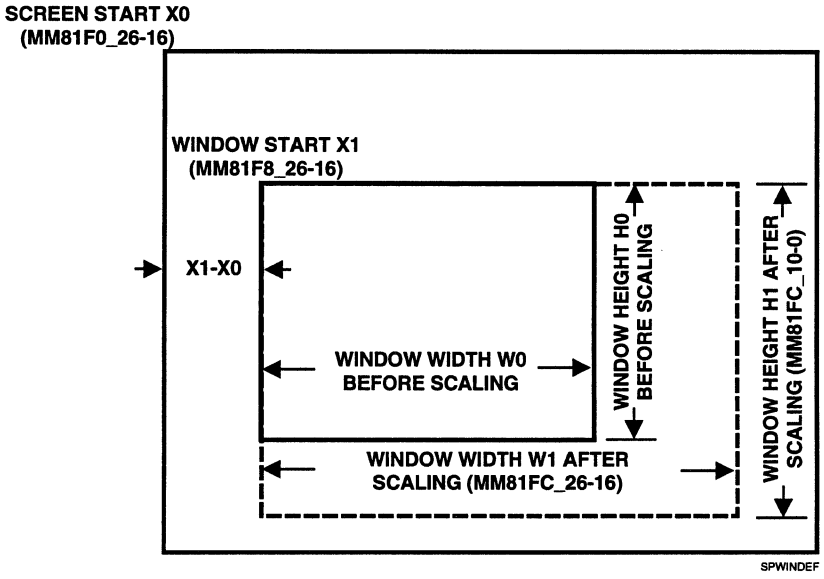


Figure 9-2. Screen Definition Parameters

Table 9=2. Register Fields Used For Scaling Up the Secondary Stream

Register Field	Description
MM8190_30-28	Filter Characteristics 000 = Secondary stream (pass-through) 001 = Secondary stream, linear, 0-2-4-2-0, for X stretch 010 = Secondary stream, bi-linear, for 2X to 4X stretch 011 = Secondary stream, linear, 1-2-2-2-1, for 4X stretch This selection applies only to horizontal scaling.
MM8190_11-0	DDA Horizontal Accumulator Initial Value. Value = 2 (W0-1) - (W1-1), where W0 is the line width in pixels before scaling and W1 is the line width after scaling. This is a signed value.
MM8198_10-0,	K1 Horizontal Factor. Value = W0-1, where W0 is the line width in pixels before scaling. This is a signed value.
MM8198_26-16	K2 Horizontal Factor. Value = W0-W1, where W0 is the line width in pixels before scaling and W1 is the line width after scaling. This is a signed value.
MM81E0_10-0,	K1 Vertical Factor. Value = [height (in lines) of the initial output window (before scaling)] -1. The initial output window height is the vertical resolution of the data written to the frame buffer and is shown as H0 in Figure 9=2.
MM81E4_10-0,	K2 Vertical Factor. Value = 2's complement of [height (in lines) of the initial output window (before scaling)] - [height (in lines) of the final output window (after scaling)] The initial output window height is the vertical resolution of the data written to the frame buffer and is shown as H0 in Figure 9=2. The final value is the same height value that is programmed in MM81FC_10-0 and is shown as H1 in Figure 9=2. This value is then the 2's complement of (H1 - H0).
MM81E8_11-0,	DDA Vertical Accumulator Initial Value. Value = 2's complement of [height (in lines) of the output window after scaling] -1. This is the same height value that is programmed in MM81FC_10-0 and is shown as H1 in Figure 9=2.

3. MM81A0_26-24 = 010b - Secondary stream blended with the primary stream on a pixel by pixel basis within the secondary stream window. This is used to provide a dissolve between two scenes.
4. MM81A0_26-24 = 011b - Secondary stream blended with the primary stream on a pixel by pixel basis within the secondary stream window. This is used to provide a fade between two scenes.
5. MM81A0_26-24 = 101b - Secondary stream overlaid on the primary stream in an irregular window. This requires a color key. This would be used, for example, for game sprites. Only the graphics area behind the sprite shape would be covered up.
6. MM81A0_26-24 = 110b - Primary stream overlaid on the secondary stream in an irregular window. This requires a color/chroma key. This case allows, for example, graphics text to overlay video with the video appearing around and even inside of the text characters.

9.3.1 Opaque Rectangular Overlaying

These modes are items 1 and 2 in the compose modes list. When one of these modes is used, the programmer can invoke a feature called opaque overlay control. This is enabled by setting MM81DC_31 to 1. If MM81A0_26-24 = 000b (secondary stream on top), then MM81DC_30 must

be cleared to 0 to also specify secondary stream on top. Similarly, If MM81A0_26-24 = 001b (primary stream on top), then MM81DC_30 must be set to 1 to also specify primary stream on top. The next step is to define when to stop fetching pixels for a line from memory and when to restart fetching them. The goal is to not fetch those pixels in the background window that are covered up by the opaque rectangular overlay window, thus saving memory bandwidth.

The first pixel that does not need to be fetched is at horizontal position X1 shown in Figure 10-2. This is programmed in MM8158_26-16. The starting pixel position for the background (X0) is programmed in MM81F0_26-16. The difference (X1 - X0) must be converted into quadwords and then programmed in MM81DC_12-3. The value is (X1 - X0) x bytes per pixel/8. If the result is a fraction, it is rounded up to the next highest integer to ensure that the first pixel not fetched in inside the opaque overlay window. Note that if the secondary stream is in the background, then the value is (X0 - X1) x bytes per pixel/8, again rounded up.

Pixel fetching must start again before or at the last pixel position of the opaque overlay window. Using the terms in Figure 10-2, this position is (X1 - X0) + W1, with W1 programmed in MM81FC_26-16 (secondary stream is on top). Converting to quadwords, the value is [(X1 - X0) + W1] x bytes per pixel/8. If the result is a fraction, the result is truncated to the next lowest integer (minus 1) and programmed in MM81DC_28-19. Note that if the secondary stream is in the background, then (X0 - X1) is used and W1 is the value in MM81F4_26-16 (primary stream is on top).

Opaque overlay control cannot be used with keying or blending and should never be enabled when one of these modes is being used.

9.3.2 Blending

These modes are items 3 and 4 in the compose modes list. The blender accepts the primary and secondary pixel streams and blends them with an arithmetic weighting. The result is then overlaid with the cursor stream. Both blender inputs are RGB 8.8.8 from the outputs of the primary stream interpolator and secondary stream color space converter. Note that blending makes sense only when both streams are defined. In addition, when blending is selected, the concept of background/foreground or top and bottom window has no meaning.

Two types of blending are provided: dissolve and fade.

When dissolve is chosen, the output pixels are generated using the following equation:

[Pp x Kp + Ps x (8 - Kp)]/8

Pp and Ps are the primary and secondary stream pixel colors respectively, both RGB 8.8.8. Kp is the primary stream weighting factor. It is a 3-bit value programmed in MM81A0_12-10. This weight value is applied to each of the three color values for the pixel. If Kp = 0, only the secondary stream is displayed. As Kp is increased, more of the pixel color from the primary stream is blended into output. At the maximum (Kp = 7 or 111b), 7/8ths of the color will be due to the primary stream and 1/8th will be due to the secondary stream. Therefore, by starting with the primary stream only, then overlaying the secondary stream with Kp values decreasing from 7 to 0, the overlay window can be dissolved gradually from primary stream to secondary stream. Note that when the Kp value is reprogrammed, its new value does not take effect until the next VSYNC, so it can be reprogrammed during frame display without disruptive effects.

When fade is chosen, the output pixels are generated using the following equation:

[Pp x Kp + Ps x Ks]/8, where Kp + Ks must be ≤ 8.

Ks is the secondary stream weighting factor. It is a 3-bit value programmed in MM81A0_4-2. This weight value is applied to each of the three color values for the pixel. Note that when fading is selected, the default values for Kp and Ks (both 0) result in a color value of 0. As with Kp, when the Ks value is reprogrammed, its new value does not take effect until the next VSYNC.

9.3.3 Color/Chroma Keying

These modes are items 5 and 6 in the compose modes list. Keying is a way of selecting on a pixel by pixel basis which stream will be displayed. Color keying is used when the stream source is in RGB format (graphics). This is always the case for the primary stream. Chroma keying is used when the stream source is YUV or YCbCr (video). The secondary stream source can be either graphics or video, so either color or chroma keying might be used. If 81A0_26-24 (compose mode) = 101b and MM8184_28 = 1, the color key is compared with the primary stream pixel. If there is a match, the corresponding secondary stream pixel is displayed. If 81A0_26-24 = 110b and MM8184_28 = 1, the color or chroma key is compared with the secondary stream pixel. If there is a match, the corresponding primary stream pixel is displayed.

If the input format is KRGB-16 (1.5.5.5), selected when MM8180_26-24 or MM8190_26_24 = 011b, the most significant bit of each pixel value is used as a color key as long as MM8184_28 is cleared to 0. When the most significant pixel bit is a 0, the other stream pixel is displayed.

For other RGB input types (as specified by MM8180_26-24), a color key must be defined. This is done by programming MM8184_23-0 with a specific RGB 8.8.8 color value. MM8184_28 must be set to 1 to enable use of this value. The number of bits to compare for each color is specified in MM8184_26-24. If there is a color match with the keyed stream pixel, the corresponding other stream pixel is displayed.

If the secondary stream input format is YUV or YCbCr, the chroma key is specified as a range of color values. The lower bound value is defined in MM8184_23-16. The upper bound value is defined in MM8194_23-0. If the secondary stream pixel color value falls within this range (inclusive of the lower and upper bounds), the Streams Processor displays the corresponding pixel from the primary stream. If the secondary stream pixel color is outside this range, the secondary stream pixel is displayed.

9.3.4 Window Location

The starting X,Y coordinates and window size for the primary stream are specified in MM81F0 and MM81F4 respectively. The starting X,Y coordinates and window size for the secondary stream are specified in MM81F8 and MM81FC respectively.

9.4 STREAMS FIFO CONTROL

The streams FIFO can be reconfigured to optimize performance for various operating modes. The FIFO is 24 8-byte slots deep. By programming MM81EC_4-0, the FIFO can be reconfigured to assign all 24 slots to either the primary or secondary stream. Allocations of 16-8 and 12-12 slots between the two streams are also possible. As an example, if only a primary stream is being displayed, optimal performance is generated by assigning all 24 FIFO slots to the primary stream.

No matter what the allocation, FIFO thresholds must be specified for the primary and secondary streams. This is done via MM81EC_16-12 for the primary stream and MM81EC_10-6 for the secondary stream. When the FIFO empties to the threshold level, an internal signal is generated requesting the memory controller to begin refilling the FIFO. The programmed threshold levels must never exceed the corresponding FIFO depths. The optimal settings for the threshold levels will be system and operating mode dependent and will have to be determined by trial and error.

Section 10: CRT/TV Interface

The 86CM65 provides analog RGB output to a CRT or NTSC/PAL output to a television. Only one of these modes can be active at a time. TV output is selected when CR3D_0 = 1. If CR3D_0 = 0 (default), CRT output is generated. External logic must direct the output to the appropriate device.

10.1 CRT OUTPUT

CRT analog RGB output (AR, AG, AB) is generated by three internal 8-bit DACs. For 8 bits/pixel CRT modes, the DACs are fed by one of two internal color look-up table (CLUT) RAMs. The source CLUT for the DACs depends on the CRT/flat panel output configuration, as explained in the DuoView section of Section 11. Each CLUT provides 256 6-bit words for each color. A clock doubled mode is also provided for 8 bits/pixel modes. A 24-bit CLUT bypass is provided for 15/16- and 24-bit color modes. A special 640x480x24 mode is provided to allow true color operation with 1 MByte of memory. Figure 10-1 shows the internal block diagram for the DACs and one of the CLUTs.

10.1.1 Operating Modes

Depending on the setting of CR67_3-2, the following operating modes are available:

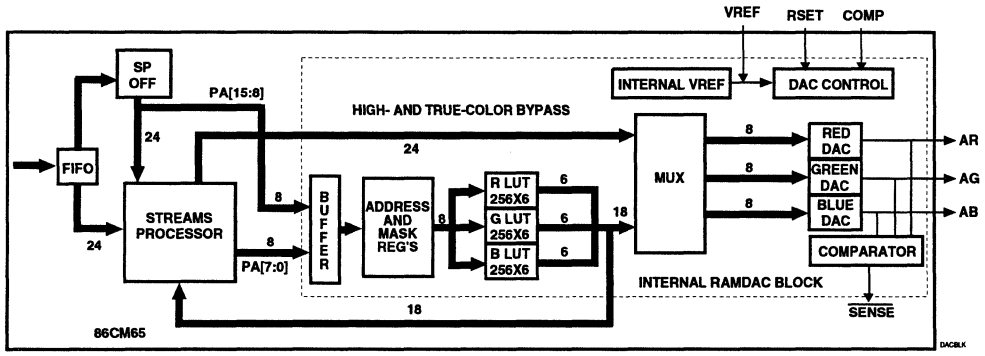


Figure 10-1. Internal RAMDAC Block Diagram

Table 10-1 86CM65 Color Modes

Color Mode	CR67 Bits 7-4	PA Bits	MAX DCLK	MAX Pixel Rate	Description
0	0000	7:0	80 MHz	80 MHz	8-bit pseudo-color (CLUT) - Default
8	0001	15:0	67.5 MHz	135 MHz	Two 8-bit pseudo-color (CLUT)
9	0011	15:0	80 MHz	80 MHz	15-bit high-color (CLUT Bypass)
10	0101	15:0	80 MHz	80 MHz	16-bit high-color (CLUT Bypass)
12	0111	23:0	75 MHz	25 MHz	640x480x24-bit packed (CLUT Bypass)
13	1101	23:0	50 MHz	50 MHz	24-bit true-color (CLUT Bypass)

- Streams Processor Off
- Streams Processor On
- Streams Processor On - secondary stream overlaid on VGA Mode 13 background

With the Streams Processor off (CR67-3-1 = 00b), data from the video FIFO (memory) is processed by another 86CM65 module and then passed directly to the RAMDAC. This mode is used for those video modes not supported by the Streams Processor. This includes all VGA modes except modes D, E, 10, 12 and 13, all interlaced modes and the clock-doubled 8 bits/pixel mode.

With the Streams Processor on (CR67_3-2 = 11b), memory data is passed directly to the Streams Processor. 8 bits/pixel (palettized) data is passed directly to the RAMDAC, where it is interpreted by the color look-up table and returned to the Streams Processor as RGB666. This and other input data types are converted to RGB888 (if required) and then sent to the RAMDAC via the high and true color bypass.

10.1.2 Color Modes

The 86CM65 internal RAMDAC provides 6 color modes of the following 3 primary types:

1. 8 bits (low byte of the internal pixel address bus) are latched each pixel clock and are used to select a CLUT location.
2. 16 bits (low two bytes of the internal pixel address bus) are latched each pixel clock. These select two consecutive CLUT locations, the data from which is clocked out to the DACs at twice the pixel clock rate.
3. 15 or 16 bits (lower two bytes of the internal pixel address bus) or 24 bits (all three bytes of the internal address bus) are transferred directly to the DACs each pixel clock.

Each of the 6 color modes is listed in Table 10-1. The desired mode is selected by programming bits 7-4 of CR67.

10.1.2.1 8 Bits/Pixel - Mode 0

Mode 0 is selected by setting bits 7-4 of CR67 to 0000b. In this mode, the low 8 internal pixel address bus bits are ANDed with the contents of the Pixel Read Mask register (3C6H). The result of the AND operation selects one of 256 CLUT locations. This results in the output of 6 bits of color information to each of the DACs.

10.1.2.2 Output-doubled 8 Bits/Pixel - Mode 8

This mode is selected by setting bits 7-4 of CR67 to 0001b. In this mode, latching of pixel data from the lower two bytes of the internal pixel data bus is based on the pixel clock (VCLK) and output of pixel data from the latches to the DACs is based on an internal clock running at twice the VCLK rate. Either bit 4 or bit 6 of SR15 must be set to 1 when this mode is selected and bit 7 of SR18 must also be set to 1.

This mode processes two pixels per VCLK with a maximum VCLK rate of 67.5 MHz. This results in an effective pixel output clock rate of 135 MHz.

The internal pixel bus bits are ANDed with the contents of the Pixel Read Mask register. The result of the AND operation selects one of 256 CLUT locations. This results in the output of 6 bits of color information to each of the DACs.

10.1.2.3 15/16-Bits/Pixel - Modes 9 and 10

These modes are selected by setting bits [7:4] of CR67 to 0011b (15 bits/pixel) or 0101b (16 bits/pixel). In either case, one pixel is transferred on the lower two bytes of the internal pixel bus each VCLK cycle. This data is sent directly to the DACs via the CLUT bypass.

10.1.2.4 Packed 24 Bits/Pixel- Mode 12

This mode is selected by setting bits 7-4 of CR67 to 0111b. It is used for a resolution of 640x480x24. Each pixel is stored in 24 bits of memory, allowing operation with 1 MByte of memory. The internal hardware cursor can be used in this mode but no acceleration is provided.

10.1.2.5 24 Bits/Pixel - Mode 13

This mode is selected by setting bits [7:4] of CR67 to 1101b. One pixel is transferred to the DACs each VCLK cycle via the CLUT bypass. The byte coding for the internal pixel address bus is shown in Figure 10-4.

10.2 RAMDAC REGISTER ACCESS

The standard VGA RAMDAC register set (3C6H - 3C9H) is used to access the internal DAC registers and the two CLUTs. SR47_1-0 control the updating of the CLUTs. If SR47_1-0 = 00b, CLUT1 and CLUT2 are both enabled. A write will update both CLUTs identically (mirroring). If SR47_1-0 = 01b, a write will update only CLUT1. If SR47_1-0 = 10b, a write will update only CLUT2.

10.3 RAMDAC SNOOPING

Setting bit 5 of the Command PCI configuration space register (Index 04H) to 1 causes the 86CM65 to snoop for RAMDAC writes. This means that the 86CM65 will write the data to its local RAMDAC but will not claim the cycle by asserting $\overline{\text{DEVSEL}}$. This allows the ISA controller to also generate a write cycle to a secondary RAMDAC. The 86CM65 always provides the data for RAMDAC reads.

If bit 5 of the PCI Command register is cleared to 0, the 86CM65 claims all RAMDAC read and write cycles.

Bits 2-0 of CR34 allow handling of PCI master aborts and retries to be individually enabled or disabled during RAMDAC cycles.

If DAC snooping is enabled, the programmer must ensure that SR47_1-0 are set correctly so that the appropriate CLUT or CLUTs will be updated.

10.4 $\overline{\text{SENSE}}$ GENERATION

The internal RAMDAC contains analog voltage comparators. These drive the internal $\overline{\text{SENSE}}$ signal active low whenever the output on any of the AR, AG or AB pins exceeds 330 mV ± 20%. The state of this internal signal can be read via bit 4 of 3C2H. This information can be used to detect the existence and type of monitor (color/mono) connected to the system.

10.5 TV OUTPUT

The AR and AG (analog red and green) outputs can be programmed to output signals capable of driving a TV monitor. This capability is enabled by setting bit 0 of CR3D to 1. Controller 1 with Streams Processor operation is automatically selected as the source of data (via the TV encoder) to the RAMDAC.

Any type of input data can be displayed on a TV. If full intelaced output is desired, double buffering must be used as explained in the digitizer section of the LPB section.

The output types are controlled by CR3D_3-1 as shown in the following table:

Table 10-2 TV Output Options

CR3D bits 3-1	AG	AR	Notes
x00	Luma	Chroma	S-Video
011	Comp	Comp	
111	Comp	BB	

As shown in Table 10-2, a single S-Video output is available, with the luminance output on the AG pin and the chromanance output on the AR pin. Alternately, the single composite signal can be output on both AG and AR or a blackburst (BB) signal can replace the composite signal on the AR pin. The black burst signal contains syncs, $\overline{\text{BLANK}}$ and color burst information without active video data and is useful for synchronization when video editing.

Bit 5 of CR3D selects between NTSC (= 0) and PAL (= 1) output. Bit 4 selects between color (= 0) and black and white (= 1) output.

Section 11: Flat Panel Interface

The 86CM65 supports a variety of color STN and TFT flat panels. Flat panel display is enabled by setting SR31_4 = 1. This section describes the control and data interfaces for each type. Operation of a flat panel in conjunction with a CRT is also described.

11.1 STN PANEL SUPPORT

STN panel support is selected when SR39_1-0 = 10b.

11.1.1 STN Panel Selection

The 86CM65 supports either a single-scan (SS-STN) or a dual-scan (DD-STN) STN panel. The type is selected via SR30_0 as follows:

0 = DD-STN panel
1 = SS-STN panel

When DD-STN panel operation is selected, frame acceleration is automatically used in all modes of operation. This means the panel will be refreshed at twice the CRT rate. For example, if the flat panel timing registers are programmed for a refresh rate of 60 Hz, the actual refresh rate will be be 120 Hz.

SR3D_2-0 define the pixel data bus size as follows:

000 = 16-bit STN
001 = 8-bit STN
010 = 24-bit STN

Pixel data is output on some combination of the the FPD[35:0] pins, depending on the pixel data bus size. This is shown in Table 11-1. Note that proper data output requires that SR3D_3 be programmed to 1.

11.1.2 STN Panel Timing

Functional timings for the data outputs of all the STN panel configurations listed in Table 11-1 are given in Figures 11-1 through 11-6.

11.1.3 STN Panel Control

Selection of an STN panel configures several pins specifically for STN control.

The polarity of the flat panel data can be changed to active low by programming SR32_4 to 1. The drive strength of the panel data is specified via SR3D-6. The drive strength for the clock is specified via SR3D_7.

The modulation (MOD) signal is output on pin B15 for STN panels when SR34_7 = 1. The modulation period is defined by SR34_6-0. SR35_4 selects the MOD clock. If MOD is not enabled, B15 outputs the FPDE display enable signal. The polarity of FPDE can be changed to active low by programming SR32_5 to 1.

Pin C4 provides the LP signal. The polarity of LP can be changed to active low by programming SR32_6 to 1.

Several controls are provided for LP and FPSCLK during vertical blanking. FPSCLK is normally stopped during non-display time by setting SR40_5 to 1. When SR3D_4 = 0, LP will run during vertical blanking. Setting SR3D_4 to 1 disables LP

Table 11-1. STN Flat Panel Data Outputs

SR30_0	1	1	1	0	0	0
SR39_1-0	10	10	10	10	10	10
SR3D_2-0	001	000	010	010	000	010
Pin Name	**SS-STN 8**	**SS-STN 16**	**SS-STN 24**	**DD-STN 8**	**DD-STN 16**	**DD-STN 24**
FPD0	R0	R0	R0	LD0	LD0	LD0
FPD1	G0	G0	G0			LD9
FPD2	B0	B0	B0	LD1	LD1	LD1
FPD3	R1	R1	R1			
FPD4	G1	G1	G1	LD2	LD2	LD2
FPD5	B1	B1	B1			
FPD6	R2	R2	R2	LD3	LD3	LD3
FPD7	G2	G2	G2			LD10
FPD8		B2	B2		LD4	LD4
FPD9		R3	R3			
FPD10		G3	G3		LD5	LD5
FPD11		B3	B3			
FPD12		R4	R4		LD6	LD6
FPD13		G4	G4			LD11
FPD14		B4	B4		LD7	LD7
FPD15		R5	R5			
FPD16			G5			LD8
FPD17			B5			
FPD18			R6	UD0	UD0	UD0
FPD19			G6			UD9
FPD20			B6	UD1	UD1	UD1
FPD21			R7			
FPD22			G7	UD2	UD2	UD2
FPD23			B7			
FPD24				UD3	UD3	UD3
FPD25						UD10
FPD26					UD4	UD4
FPD27						
FPD28					UD5	UD5
FPD29						
FPD30					UD6	UD6
FPD31						UD11
FPD32					UD7	UD7
FPD33						
FPD34						UD8
FPD35						

during vertical blank. If SR3D_4 = 0 and SR3D_5 = 1, FPSCLK is disabled during the first line of vertical blanking. If SR40_5 = 0, FPSCLK runs continuously. FPSCLK can be delayed via SR40_3-1.

Pin A3 provides the FLM (first line marker) signal. The polarity of FLM can be changed to active low by programming SR32_7 to 1.

Setting SR40_4 to 1 forces all flat panel data and control signals to logic 0.

11.1.4 STN Frame Rate Control

Frame rate control (FRC) for STN panels is used to display more grayscale levels than would normally be possible based on the 1 bit/color input. Each color bit is turned on or off over a series of frames to simulate intermediate colors.

Frame rate control is enabled automatically for STN panels. The number of frames over which bits are turned on or off to generate a single color determines the number of grayscale levels and is programmed in SR39_4-3 as follows:

00= 16 levels
01 = 8 levels
10 = Reserved
11 = Reserved

FRC weighting values are programmed via SR37 and SR38. SR3A, SR3B and SR3C are used to tune the frame rate control for optimum quality. The algorithms and techniques used are proprietary.

11.1.5 STN Panel Dithering

Dithering is used to increase the apparent number of colors displayed. This is enabled by setting SR36_7-6 as follows:

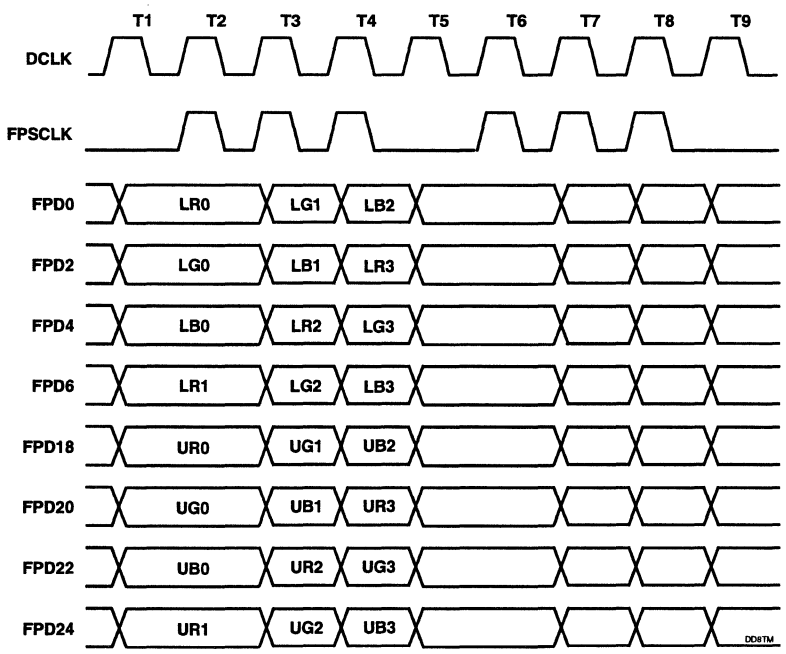


Figure 11-1. 8-bit Color DD-STN Panel Timing

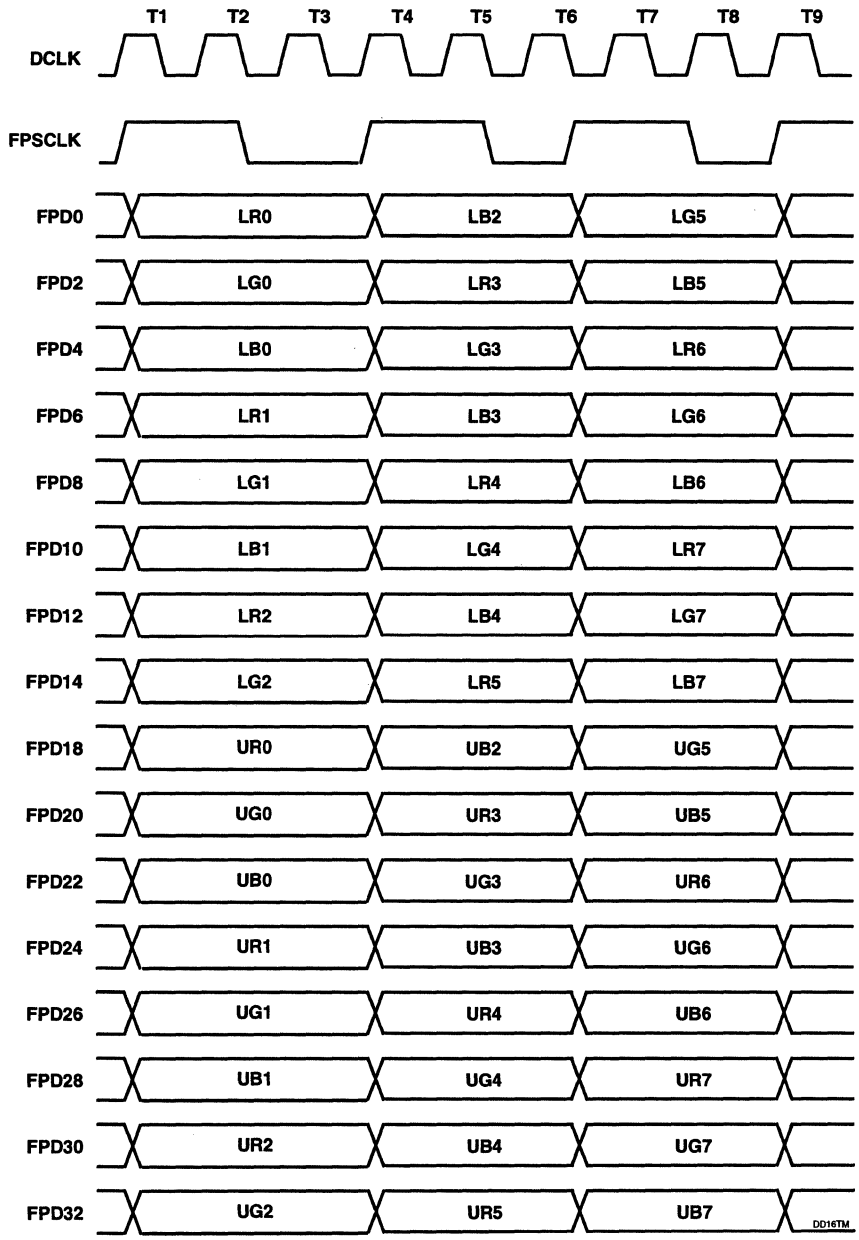


Figure 11-2. 16-bit Color DD-STN Panel Timing

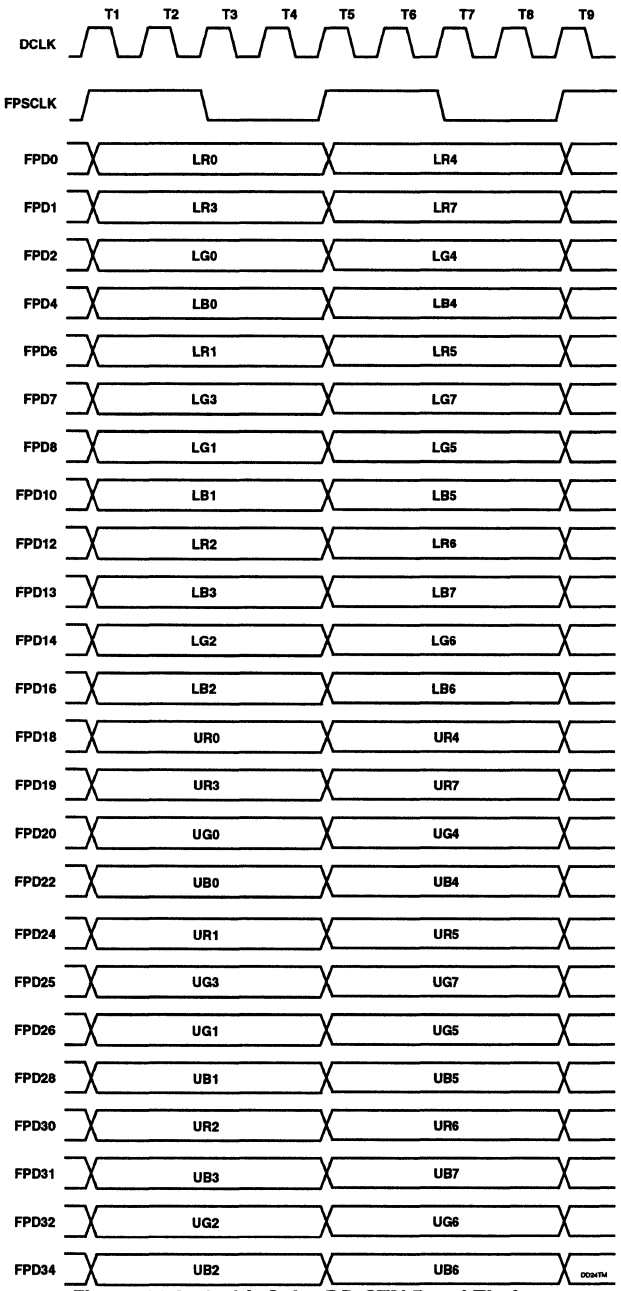


Figure 11-3. 24-bit Color DD-STN Panel Timing

00 = Dithering disabled
01 = Dither in all modes
10 = Dither in graphics modes only (no text)
11 = Dither in graphics modes with 8 bpp or more

The base color is selected by programming SR36_5-3 as follows:

000 = 8 bits (no dithering)
011 = 3 bits (8-level FRC)
100 = 4 bits (16-level FRC)

SR36_0 selects the number of bits of the 8-bit color value to use for dithering as follows:

0 = 2 bits (2x2 dither pattern)
1 = 4 bits (4x4 dither pattern)

Typically, a 2x2 dither pattern is used with 16-level FRC and a 4x4 pattern with 8-level FRC.

11.1.6 Dual-Scan STN Frame Buffer

DD-STN panel operation requires off-screen video memory. The amount of memory is programmed in SR50 and SR51. The starting location of the DD-STN memory is specified in SR4F. These values are all programmed by the video BIOS at reset.

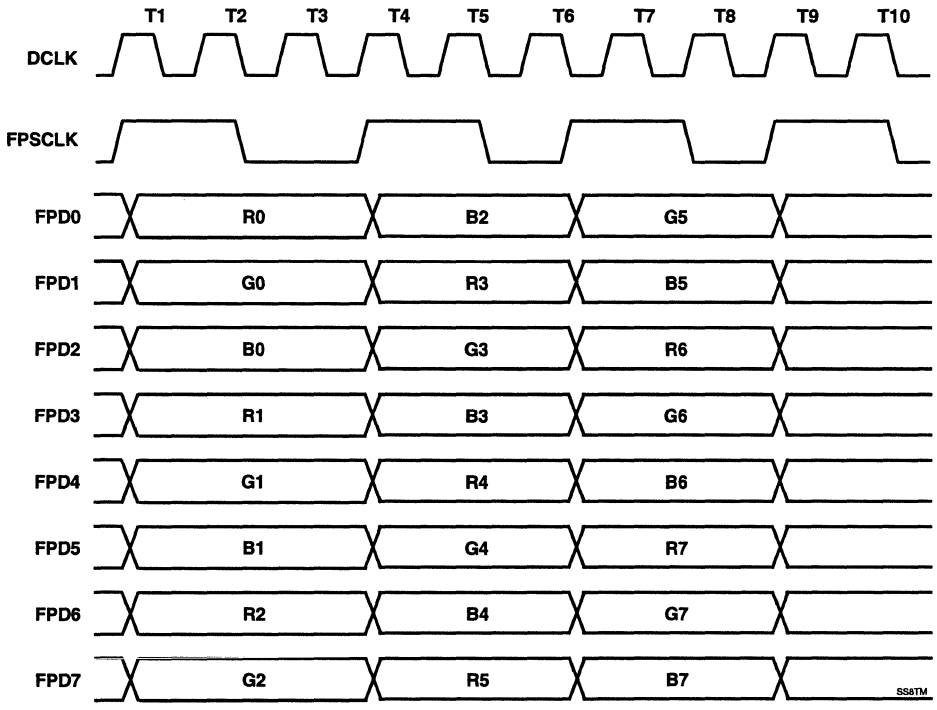


Figure 11-4. 8-bit Color SS-STN Panel Timing

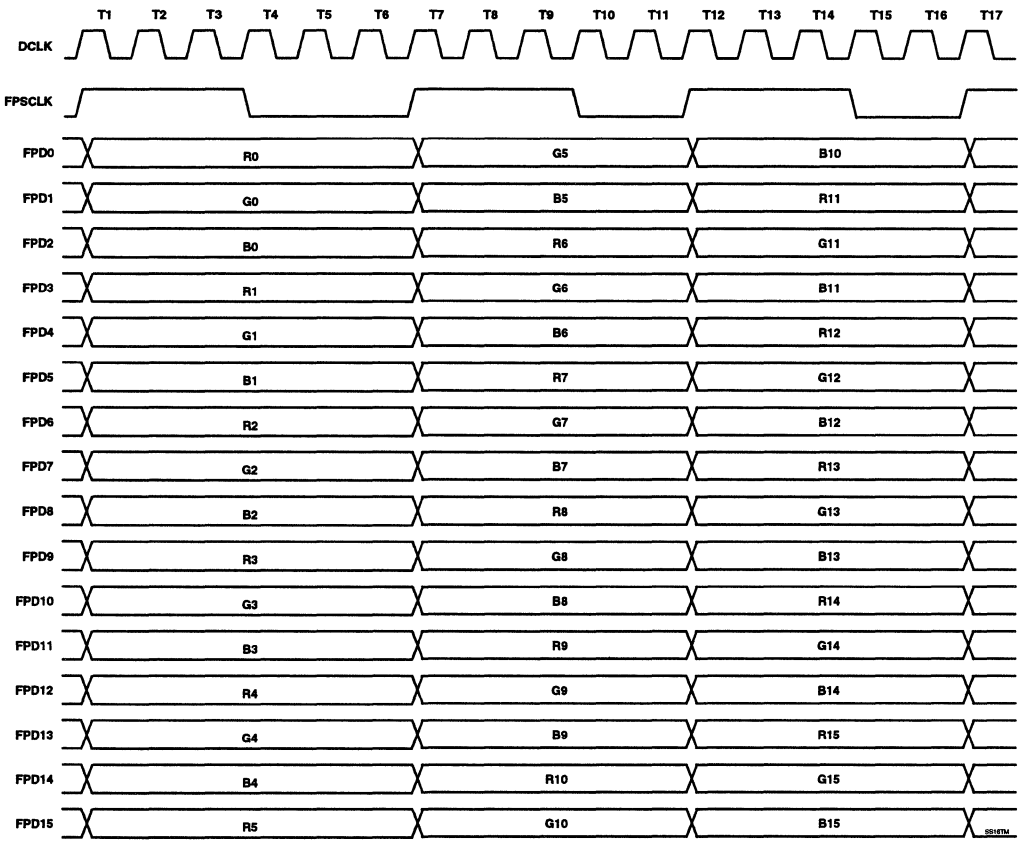


Figure 11-5. 16-bit Color SS-STN Panel Timing

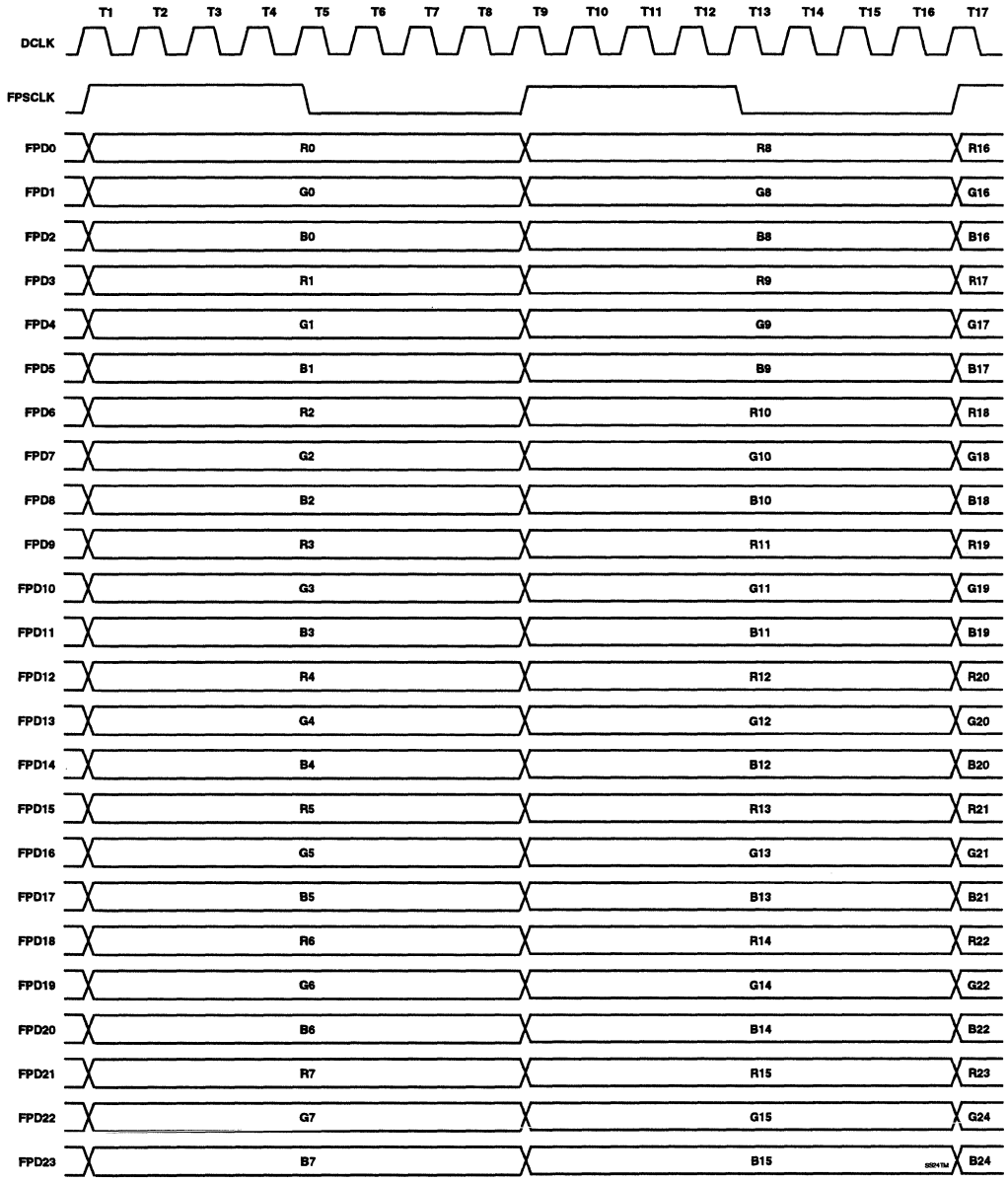


Figure 11-6. 24-bit Color SS-STN Panel Timing

11.2 TFT PANEL SUPPORT

TFT panel support is selected when SR39_1-0 = 00b.

11.2.1 TFT Panel Selection

SR3D_2-0 define the pixel data bus size as follows:

000 = 1 pixel/clock TFT (9-, 12-, 15-, 18-bit)
001 = 1 pixel/clock TFT (24-bit)
010 = 2 pixels/clock TFT (2x9-, 2x12-, 2x18-bit)

The 2 pixels per clock modes halve the clock rate and clock two pixels on the falling edge of FPSCLK, thereby lowering EMI levels. SR40_6 is set to 1 to support this mode of operation.

Pixel data is output on some combination of the FPD[35:0] pins. The data outputs are shown in Table 11-2. Note that proper data output requires that SR3D_3 be programmed to 1.

11.2.2 TFT Panel Timing

TFT panel timing is very similar to CRT timing, with the FPDE signal functionally equivalent to the CRT BLANK signal (inverted). Functional timing for an 24-bit TFT panel clocked at one pixel per FPSCLK and a 36-bit (2x18) panel clocked at 2 pixels/FPSCLK are shown in Figure 11-7. Timings are the same for all types of TFT panels clocked at 1 pixel/FPSCLK, as is the case for all types of TFT panels clocked at 2 pixels/FPSCLK.

11.2.3 TFT Panel Control

Selection of a TFT panel configures several pins specifically for TFT control. The drive strengths of the panel clock and data are specified via SR3D_7-6.

The polarity of the flat panel data can be changed to active low by programming SR32_4 to 1.

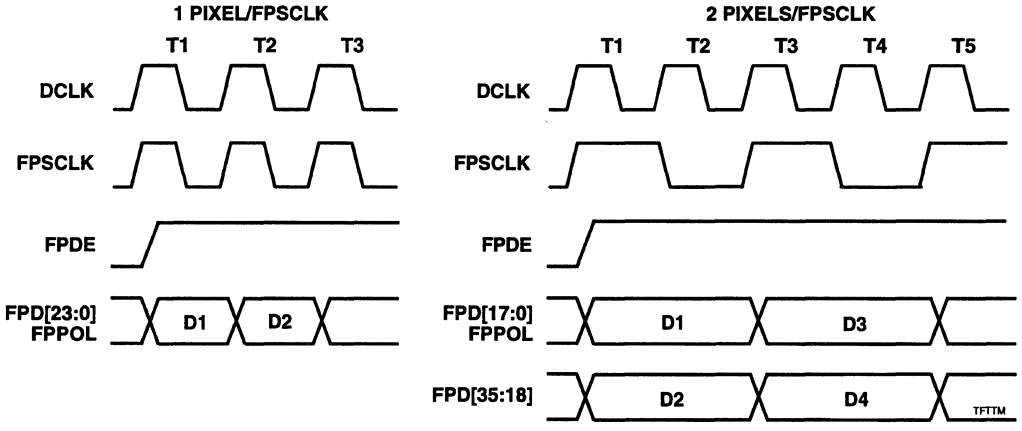


Figure 11-7. TFT Panel Timing

Table 11-2. TFT Flat Panel Data Outputs

SR30_0	1	1	1	1	1	1	1	1	1
SR36_5-3	011	011	100	100	101	101	110	110	000
SR39_1-0	00	00	00	00	00	00	00	00	00
SR3D_2-0	000	010	000	010	000	010	000	010	001
Pin Name	**TFT 9**	**TFT 2x9**	**TFT 12**	**TFT 2x12**	**TFT 15**	**TFT 2x15**	**TFT 18**	**TFT 2x18**	**TFT 24**
FPD0							R0	R00	R2
FPD1								R10	R0
FPD2					R0	R00	R1	R01	R3
FPD3						R10		R11	
FPD4			R0	R00	R1	R01	R2	R02	R4
FPD5				R10		R11		R12	
FPD6	R0	R00	R1	R01	R2	R02	R3	R03	R5
FPD7		R10		R11		R12		R13	R1
FPD8	R1	R01	R2	R02	R3	R03	R4	R04	R6
FPD9		R11		R12		R13		R14	
FPD10	R2	R02	R3	R03	R4	R04	R5	R05	R7
FPD11		R12		R13		R14		R15	
FPD12							G0	G00	G2
FPD13								G10	G0
FPD14					G0	G00	G1	G01	G3
FPD15						G10		G11	
FPD16			G0	G00	G1	G01	G2	G02	G4
FPD17				G10		G11		G12	
FPD18	G0	G00	G1	G01	G2	G02	G3	G03	G5
FPD19		G10		G11		G12		G13	G1
FPD20	G1	G01	G2	G02	G3	G03	G4	G04	G6
FPD21		G11		G12		G13		G14	
FPD22	G2	G02	G3	G03	G4	G04	G5	G05	G7
FPD23		G12		G13		G14		G15	
FPD24							B0	B00	B2
FPD25								B10	B0
FPD26					B0	B00	B1	B01	B3
FPD27						B10		B11	
FPD28			B0	B00	B1	B01	B2	B02	B4
FPD29				B10		B11		B12	
FPD30	B0	B00	B1	B01	B2	B02	B3	B03	B5
FPD31		B10		B11		B12		B13	B1
FPD32	B1	B01	B2	B02	B3	B03	B4	B04	B6
FPD33		B11		B12		B13		B14	
FPD34	B2	B02	B3	B03	B4	B04	B5	B05	B7
FPD35		B12		B13		B14		B15	

Pin B15 becomes the FPDE display enable signal. The polarity of this signal can be changed to active low by setting SR32_5 to 1.

Pin C4 becomes the FPHSYNC signal. The polarity of this signal can be changed to active low by setting SR32_6 to 1.

Pin A3 becomes the FPVSYNC signal. The polarity of this signal can be changed to active low by setting SR32_7 to 1.

Pin C15 is the FPPOL polarity indicator signal for those panels that support it. It is available when SR40_7 = 1 and SR1A_5 = 1. FPPOL is supported for 18- and 24-bit 1 pixel/clock modes and for 2x18-bit 2 pixels/clock mode. Timing for this signal is shown in Figure 11-7.

SR40_5 allows FPSCLK to be turned on (=0) or off (=1) during non-display time. FPSCLK can be delayed via SR40_3-1.

11.2.4 TFT Panel Dithering

As with STN panels, dithering is used to increase the apparent number of colors displayed. This is enabled by setting SR36_7-6 appropriately as follows:

00 = dithering disabled
01 = dithering enabled in all modes
10 = dither in graphics (not text) modes
11 = dither in graphics modes with 8bpp or more color

SR36_0 selects the dither pattern as follows:

0 = 2x2 pattern
1 = 4x4 pattern

The base color is selected by programming SR36_5-3 as follows:

000 = 8 bits (no dithering - 24-bit TFT
011 = 3 bits (9-bit TFT)
100 = 4 bits (12-bit TFT)
110 = 6 bits (18-bit TFT)

Note that all other values are illegal.

11.3 FLAT PANEL DISPLAY ENHANCEMENTS

The 86CM65 features automatic centering for display modes that are smaller than the panel size. Additionally, horizontal and vertical expansion for both graphics and text modes enables low resolution modes to fill the entire available display area.

11.3.1 Automatic Centering

Automatic horizontal centering is enabled via SR54_4. Automatic vertical centering is enabled via SR56_4.

11.3.2 Horizontal Compensation

SR54_1-0 enable horizontal expansion for text modes. SR55_1-0 specify which text modes get expanded. SR54_3-2 enable horizontal expansion for graphics modes. SR55_4-2 specify which graphics modes get expanded. SR54_4 enables horizontal centering.

11.3.3 Vertical Compensation

SR56_1-0 enable vertical expansion for text modes. SR57_1-0 specify which text modes get expanded. SR56_3-2 enable vertical expansion for graphics modes. SR55_6-2 specify which graphics modes get expanded. SR56_4 enables vertical centering.

11.3.4 Pulse Width Modulation

A pulse width modulation (PWM) signal is available to control panel brightness or contrast. PWM support is enabled for 256Kx16 DRAM configurations by setting SR52_0 to 1. This enables output of the PWM signal on pin M17. PWM cannot be used with 512Kx32 DRAM configurations or with the ODD input function. SR52_1 specifies the PWM clock source. SR52_6-4 specify the clock divide used to determine the final PWM pulse width (period). The duty cycle of the PWM pulse is controlled via SR53.

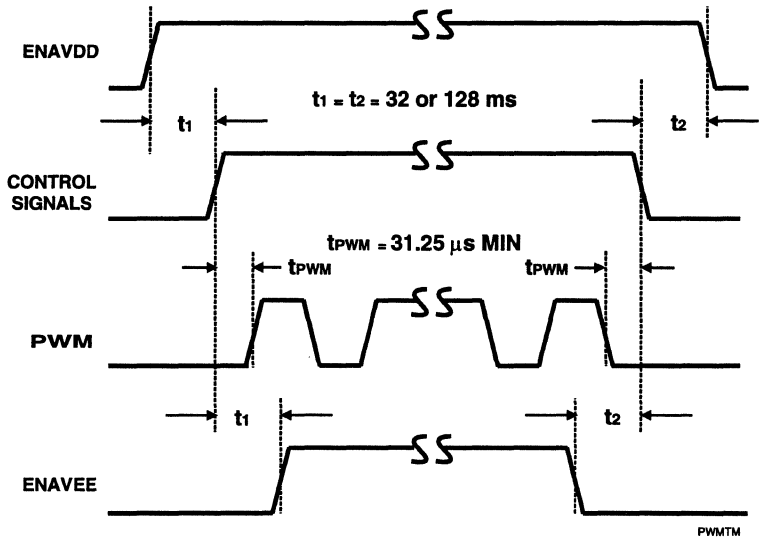


Figure 11-8. PWM Timing

PWM active timing is coordinated with panel power sequencing. This is shown in Figure 11-8.

11.3.5 Blinking

Character blinking can be set via CR43_3 to every 32 (= 0) or 64 (=1) frames. Cursor blinking can be set via CR43_6-5 as follows:

00 = blink every 16 frames
01 = blink every 32 frames
10 = blink every 64 frames

11.4 DuoView DISPLAY

The 86CM65 has two CRT controllers as shown in Figure 11-9. Either can be used to drive a CRT and either can be used to drive a flat panel. The Streams Processor can be used only in conjunction with controller 1. In addition, controller 2 can only be used to display Enhanced modes (not VGA) and does not provide flat panel expansion and centering.

The DCLK rate used by each controller path can be individually specified. This provides a tremendous degree of flexibility, including the ability to display one image on the CRT and a completely different image on the flat panel, each using different CRT timings. This section explains how to take advantage of this flexibility.

11.4.1 DuoView Display Setup

Flat panel controller usage is defined by SR31_1 as follows:

0 = Use controller 1 (via Streams Processor)
1 = Use controller 2 (no Streams Processor, VGA)

The controller used by the CRT/TV is defined by SR31_2 as follows:

0 = Use controller 1 (via Streams Processor)
1 = Use controller 2 (no Streams Processor, VGA)

Each controller has an associated color look-up table (CLUT). By default, CLUT1 and CLUT2 will be enabled and mirrored for CPU writes. The hardware cursor and hardware icon, if enabled,

are shared by both controllers. By default, they are controlled by controller 1.

The controller choices are based on the following considerations.

LCD or CRT/TV Only

Use controller 1.

Simultaneous Display

Use controller 1 for both CRT/TV and flat panel.

This is a variation of DuoView where the CRT and flat panel images are displayed with almost identical timings. Normally, the flat panel timings are compromised for CRT VESA timings. Video output using the Streams Processor is displayed on both screens, as are the hardware cursor and/or hardware icon, if enabled.

DuoView Display

For this case, the CRT uses one controller and the flat panel uses the other. The choice depends on the potential display of video, which requires the Streams Processor, the need to display standard VGA modes or the need to have automatic expansion/centering, all of which require controller 1. Therefore, if video is desired on the CRT, this is assigned controller 1 and the flat panel is assigned controller 2. Note that this means that automatic centering/expansion is not available for the panel. The assignments are reversed if video output is desired on the flat panel. Note that only one screen can display video in this mode.

The DCLK rate for the controller 1 path is selected via SR28_3-0. The DCLK rate for the controller 2 path is selected via SR28_7-4.

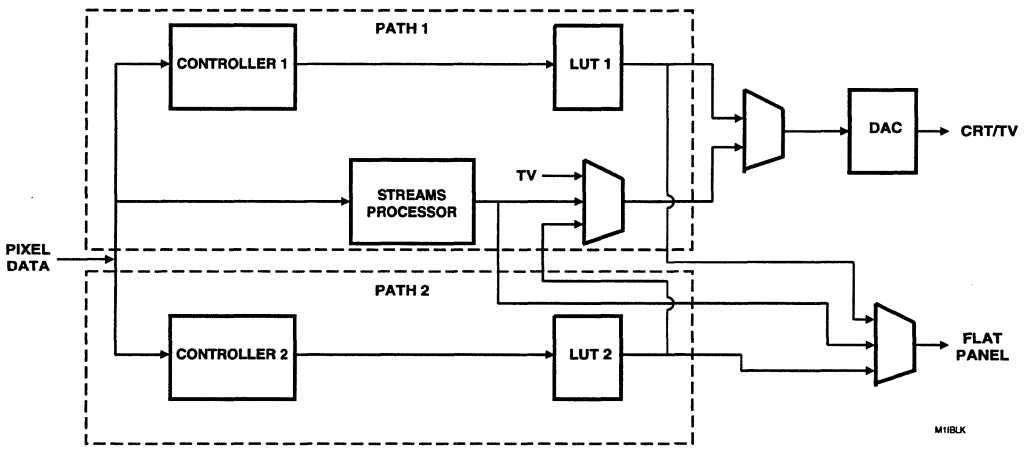


Figure 11-9. Internal Data Paths

In DuoView mode, the hardware cursor can be displayed on either screen. SR31_7 = 0 selects cursor control by controller 1 and SR31_7 = 1 selects cursor control by controller 2. The hardware icon can also be displayed on either screen. SR31_6 = 0 selects icon control by controller 1 and SR31_6 = 1 selects icon control by controller 2.

In DuoView, if a text mode is used for one display, a text mode must also be used for the other display. The same is true for graphics modes. In other words, text and graphics modes cannot be mixed. If the same image is to be displayed on both the CRT/TV and the flat panel but with different timings, both controllers must be used and the Streams Processor and VGA modes are not available.

11.4.2 DuoView Programming

86CM65 has a large number of paired registers for control of timings and resolutions for CRT/TV display. For example, there are two Horizontal Total (CR0) registers, one associated with CRT controller 1 and the other with CRT controller 2. Both have the same address, and control of read/write access to these registers is provided by a number of bits in SR26. SR26_3 controls write access to the CRT controller 1 registers. A value of 0 (default) enables writes. SR26_2 controls write access to the CRT controller 2 registers. A value of 0 (default) disables write access. Using these controls, a single write can update either of the paired registers or both.

Bit 0 and 1 of SR26 control read access of the paired registers.

The following CRTC registers (or register bits) are paired:

CR0-CR9; CRC; CRD; CR10-CR18; CR22; CTR22_7; CR24; CR31_6; CR33_6-3; CR34_4; CR35_5-4; CR3A_4-3; CR3B; CR3C; CR42_5; CR43; CR51; CR63, CR65; CR66_0; CR67; CR69; CR71

In addition, there are a number of shared registers. This means that both controller 1 and controller 2 obtain information from the same register. The shared registers are:

CRA; CRB; CRE; CRF; AR11; SR1_5; SR3_5-0; SR4_3, 1; GR5_6-5; CR31_3; CR32_6; CR38; CR39

Paired and shared registers and bits are noted in the register descriptions.

A separate set of CRT timing registers is provided for flat panel operation. These are SR60 - SR6F, except SR67 is reserved. The values to be programmed in these registers are fixed for a given panel (not mode dependent as with a CRT). Therefore, they should be programmed only at reset. These registers are used by controller 1 if SR31_1 = 0 and by controller 2 if SR31_1 = 1.

11.4.3 DuoView Programming Example

The following steps show how to program the 86CM65 to operate the flat panel using Controller 2 at a resolution of 800x600 at 60 Hz and the CRT using Controller 1 at a resolution of 640x480 at 60 Hz.

1. Boot for 800x600 60 Hz flat panel operation
2. Enable Controller 1 and Controller 2 (SR26 = 04H)
3. Set VESA Mode 103 (800x600 60 Hz)
4. Disable Controller 2 (SR26 = 00H)
5. Set VESA Mode 101 (640x480 60 Hz)
6. Set flat panel to Controller 2 (SR31_1 = 1)
7. Set CRT to Controller 2 (SR31_2 = 0)
8. Set DCLK PLL to 75 MHz (SR12 = 42, SR13 = 28)
9. Set Controller 1 clock to PLL/3 = 25 MHz and Controller 2 clock to PLL/2 = 37 MHz (SR28 = 48H)
10. Lock the timing registers (CR35 = F0H)

Section 12: Local Peripheral Bus

Local Peripheral Bus (LPB) operation is enabled by setting MMFF00_0 to 1. This provides the following interfaces:

- S3 Scenic/MX2™ MPEG Audio/Video Decoder (glueless, bi-directional)
- Philips® Video Digitizers (8- or 16-bit interface)
- Host Video Data (Pass-through. This allows decimation of 32-bit CPU data being written to the frame buffer.
- ZV Port (compliant with Release 007)

The hardware interfaces are clocked by LCLK. This requires that MMFF00_24 be set to 1. Pass-through operation is clocked by SCLK by clearing MMFF00_24 to 0.

The internal block diagram for the LPB is shown in Figure 12-1.

12.1 Scenic/MX2 INTERFACE

The hardware interface to the Scenic/MX2 is shown in Figure 12-2.

The Scenic/MX2 interface is selected by setting MMFF00_3-1 to 000b. This interface is fully bi-directional. Scenic/MX2 registers can be accessed, compressed data sent and decompressed video data received.

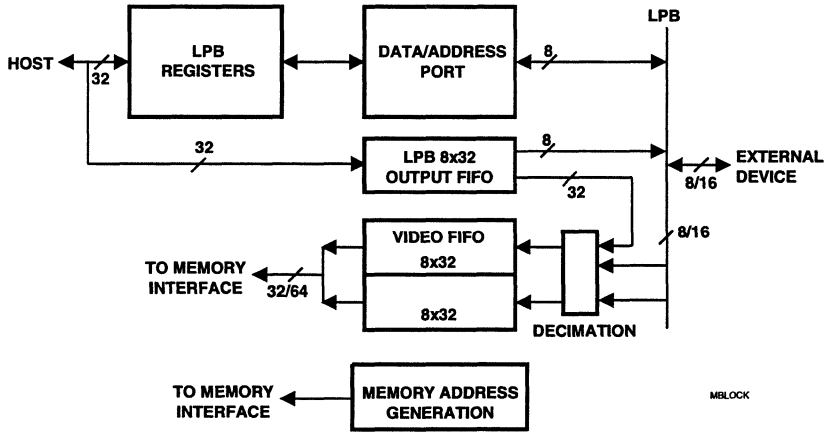


Figure 12-1. LPB Internal Block Diagram

12.1.1 Scenic/MX2 Register/Memory Access

To read/write a Scenic/MX2 register or private memory location (other than to transfer compressed data), the LPB Direct Read/Write Address register (MMFF14) is written. The new register/memory data is then written to MMFF18. For a write access, this write triggers the sequence shown in Figure 12-3 if the Scenic/MX2 is ready to receive the data ($\overline{\text{CREQ}}$/CRDY remains high). One cycle after 86CM65 asserts its $\overline{\text{VREQ}}$/VRDY signal, it sends the address in three byte writes. The first byte is composed of bits 23-16 of MMFF14. The three upper bits are 000b to define this as a write. Bit 4 is 1 for a register access and 0 for a memory access. Bits 3-0 are bits 19-16 of the address. The second byte is bits 15-8 of MMFF14 and the third byte is bits 7-0. The data immediately follows in four byte writes. Data is written in the opposite byte order to that for the address, i.e., least significant byte (bits 7-0) first and most significant byte (bits 31-24) last. The 86CM65 then deasserts $\overline{\text{VREQ}}$/VRDY. The Host repeats the above sequence for another write if required.

If the Scenic/MX2 is not ready to receive data, it drives its $\overline{\text{CREQ}}$/CRDY signal low during the A0-0 byte (LSB) of the address phase. The 86CM65 then delays sending the data until the Scenic/MX2 raises $\overline{\text{CREQ}}$/CRDY. This is depicted in Figure 12-4.

Figure 12-5 shows a Scenic/MX2 register/memory read when the Scenic/MX2 is ready to provide data. This is indicated by the Scenic/MX2 holding the $\overline{\text{CREQ}}$/CRDY high throughout the cycle. The three upper bits of the first address byte are 001 to define a read.

If the Scenic/MX2 is not ready to provide data, it drives its $\overline{\text{CREQ}}$/CRDY signal low during the address phase. The 86CM65 then waits until the Scenic/MX2 raises $\overline{\text{CREQ}}$/CRDY and provides register data. This is depicted in Figure 12-6.

To prevent data starvation and deal with request contention, the following protocol is followed.

- No transaction can be initiated if the bus is active
- There is one dead cycle on the bus following all transactions

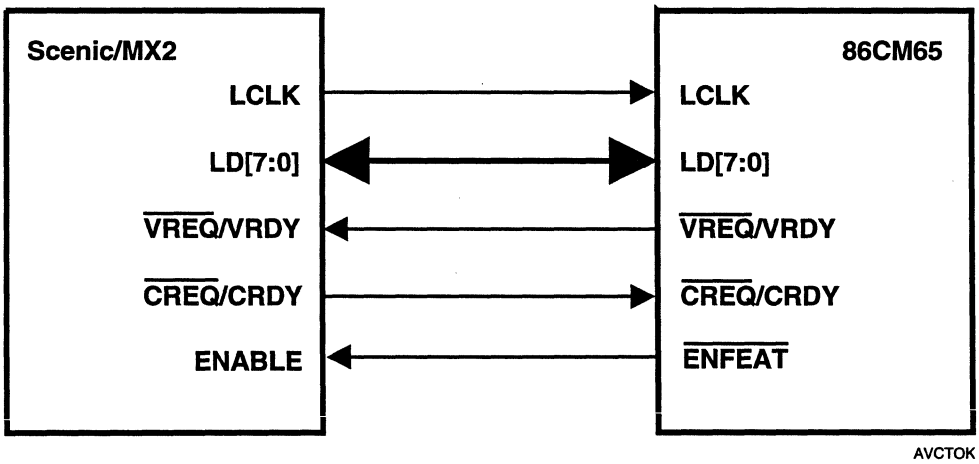


Figure 12-2. 86CM65 to Scenic/MX2 Interface

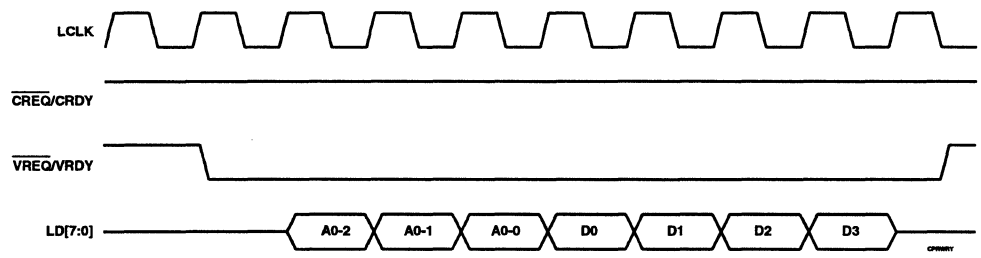


Figure 12-3. Scenic/MX2 Write (Scenic/MX2 Ready)

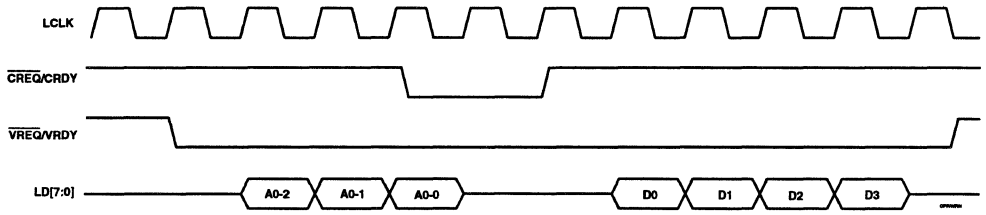


Figure 12-4. Scenic/MX2 Write (Scenic/MX2 Not Ready)

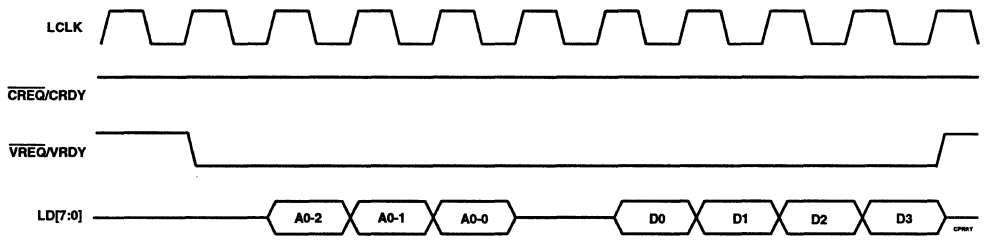


Figure 12-5. Scenic/MX2 Read (Scenic/MX2 Ready)

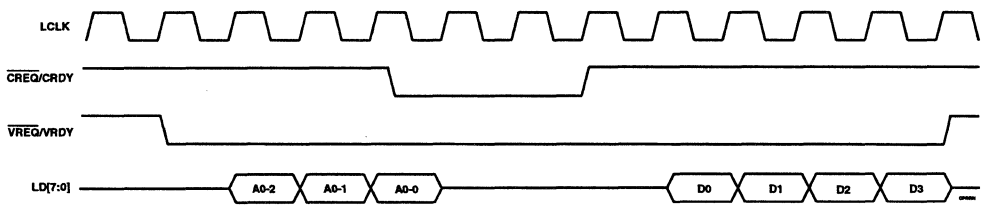


Figure 12-6. Scenic/MX2 Read (Scenic/MX2 Not Ready)

- One device may not initiate a transaction until the second cycle following the completion of a transaction initiated by the other device
- Neither device may initiate a transaction until the third cycle following the completion of a transaction initiated by itself
- If $\overline{\text{CREQ}}$/CRDY and $\overline{\text{VREQ}}$/VRDY are both driven low on the same cycle (request contention), $\overline{\text{CREQ}}$/CRDY (the Scenic/MX2) wins.

12.1.2 Scenic/MX2 Compressed Data Transfer

The 86CM65 has an output FIFO for handling the transfer of compressed video data from the Host to the Scenic/MX2 (see Figure 12-1). The Host must first check the number of empty slots (MMFF04_3-0), then send no more than this many doublewords (32 bits) of compressed data to the FIFO. An eight doubleword address range (FF40H - FF5CH) is provided for this FIFO. Writes to any of these addresses are directed to the FIFO.

MMFF00_17-16 are programmed to specify the number of doublewords of data to burst to the Scenic/MX2. A write to the output FIFO then initiates a compressed data write to the Scenic/MX2. This is depicted in Figure 12-7 for a burst count of 2 (MMFF00_17-16 = 01b) for the case where the Scenic/MX2 is ready to receive the data. The address and first doubleword are transferred exactly as for a register/memory write. Following doublewords in the burst are each separated by one dead cycle. The address has no meaning except for the upper three bits, which are forced to 110b by hardware to specify a compressed data transfer. Note that burst writes that end because the FIFO is empty (as opposed to the maximum burst count being reached) hold $\overline{\text{VREQ}}$/VRDY low for one more cycle than is shown in Figure 12-7.

The Scenic/MX2 cannot accept a burst larger than eight doublewords. If MMFF00_17-16 are programmed to 11b (burst all) and eight doublewords are loaded into the FIFO, software must ensure that the FIFO is empty before loading more data into the FIFO.

A compressed data transfer when the Scenic/MX2 is not ready to receive data is almost the same as a register write for the same circumstances (see Figure 12-4). The only difference is that after the Scenic/MX2 returns its CRDY signal, additional doubleword packets may be burst to the Scenic/MX2 as shown in Figure 12-7.

The Scenic/MX2 can stop a compressed data transfer by pulling $\overline{\text{CREQ}}$/CRDY low for one (and only one) cycle during byte three of any doubleword. This is shown in Figure 12-8.

An output FIFO empty interrupt can be enabled by setting MMFF08_17 to 1. The status is read via bit 1 of this same register.

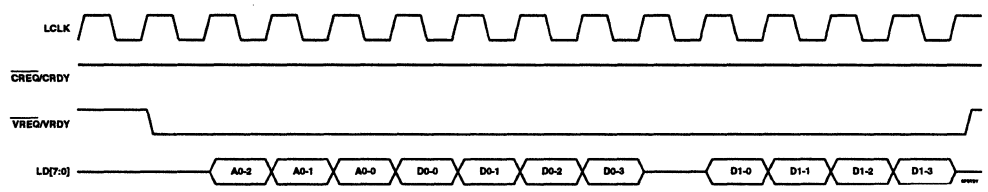


Figure 12-7. Scenic/MX2 Compressed Transfer (Ready)

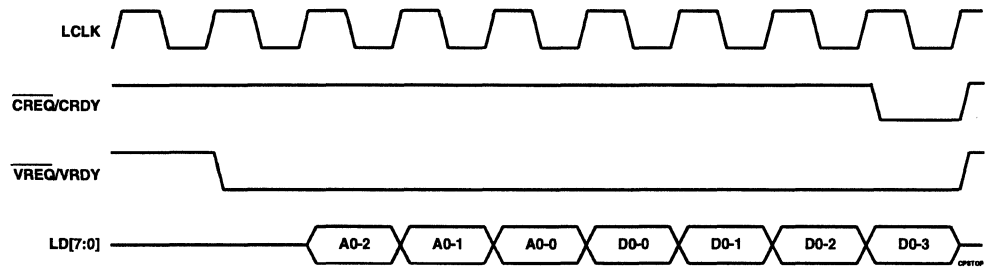


Figure 12-8. Scenic/MX2 Stopping a Compressed Xfer

12.1.3 Scenic/MX2 Video Capture

The following setup is done for Scenic/MX2 video capture:

- The 86CM65 is placed in Scenic/MX2 mode (MMFF00_3-1 = 000b).
- One or two frame buffer starting addresses are defined (MMFF0C, MMFF10). One is required. The second is required for double buffering.
- The horizontal and vertical decimation registers are programmed (MMFF2C, MMFF30). This is optional.
- The line stride is programmed (MMFF34_10-0). This is not required if HSYNCs are not being sent.

The 86CM65 signals its readiness to accept data by driving VREQ/VRDY high. This is done automatically when the 86CM65 does not need to drive this signal low such as to initiate a register access or to indicate an LPB video FIFO full state. The Scenic/MX2 responds by sending a VSYNC (CREQ/CRDY low for one cycle) followed by an HSYNC (CREQ/CRDY low for two cycles). This is shown in Figure 12-9. As indicated in the figure, the time between VSYNC and HSYNC is variable. The HSYNC sequence occurs after each line, but may not occur before the first line, depending on how the Scenic/MX2 is programmed.

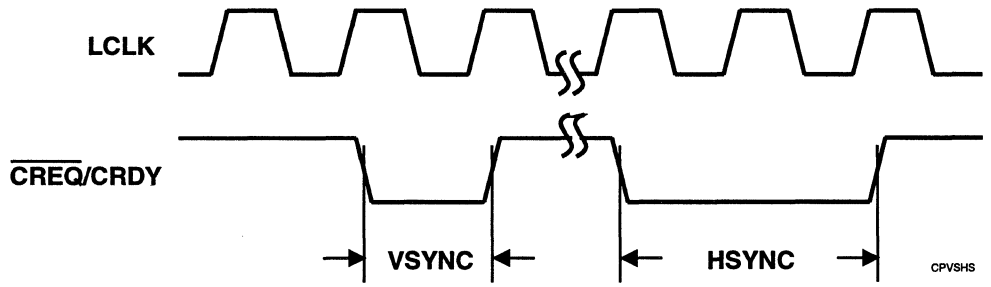


Figure 12-9. Scenic/MX2 VSYNC and HSYNC Protocols

After the VSYNC/HSYNC sequence, the Scenic/MX2 can pull CREQ/CRDY low at any time and begin sending data three clocks later. This is shown in Figure 12-10. The 86CM65 assumes data has begun any time CREQ/CRDY is held low for more than two cycles. When the Scenic/MX2 is sending the last byte, it drives CREQ/CRDY high. The Scenic/MX2 must always send data in 4-byte packets. If it has fewer to send for the last packet, it must pad the transmission with dummy writes to create a 4-byte packet.

Figure 12-10 shows what happens when the 86CM65 is ready to receive all the data. If the 86CM65 cannot accept more data, such as when its LPB video FIFO is full, it drives its VREQ/VRDY signal low during the first byte phase of a 4-byte packet. All bytes starting with this one are rejected by the 86CM65 and must be resent by the Scenic/MX2 after the 86CM65 drives its VREQ/VRDY signal high again. This is depicted in Figure 12-11, where the Dn0 byte, which is the first byte of the nth 4-byte packet, is rejected. When the 86CM65 can accept more data, it drives VREQ/VRDY high. The Scenic/MX2 drives CREQ/CRDY high (two cycles later) and then drives it low when it is ready to resend the data.

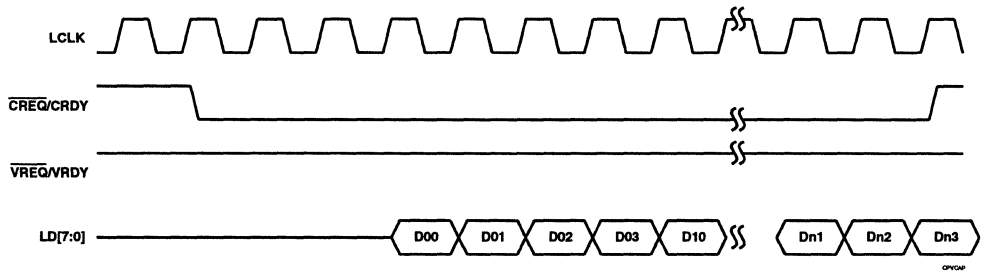


Figure 12-10. Scenic/MX2 Video Input (86CM65 Ready)

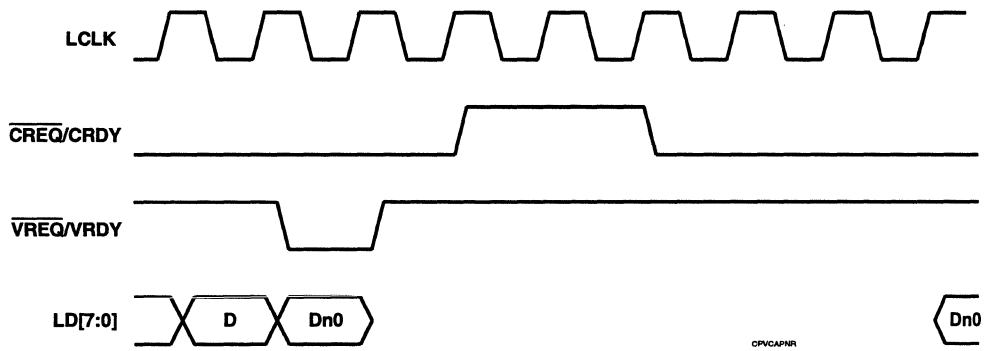


Figure 12-11. Scenic/MX2 Video Input (86CM65 Not Ready

The resend of Dn0 and subsequent bytes starts two cycles later.

When the 86CM65 receives an HSYNC from the Scenic/MX2, it adds the line offset (MMFF34_10-0) to the previous line starting address and starts writing the next data at that location. In this way, for example, it can transfer 640-byte lines into a frame buffer configured for 1024-byte lines. If HSYNCs are not sent, memory will be written in a contiguous manner.

12.2 DIGITIZER INTERFACE

86CM65 provides a glueless interface to the Philips digitizer in Video 16 mode (MMFF00_3-1 = 001b) as shown in Figure 12-12. This section describes the interface to the Philips SAA7110 digitizer.

As an alternative, the Scenic/MX2 provides a glueless interface to the SAA7110. In this case, the Scenic/MX2 converts the 16-bit data to 8-bit data and also provides the I^2C interface to the SAA7110. The 86CM65 then receives the video data, clock and controls from the Scenic/MX2. The Scenic/MX2 documentation describes this interface.

12.2.1 I^2C Interface for SAA7110

SAA7110 registers are programmed via a serial I^2C interface. This interface is described in Section 13.

12.2.2 SAA7110 Video Input

The following setup is done for SAA7110 video input:

- The 86CM65 is placed in Video 16 mode (MMFF00_3-1 = 001b)
- Byte swapping is disabled by setting MMFF00_6 to 1.
- The correct vertical and horizontal sync polarities are specified (MMFF00_9, 10).
- One or two frame buffer starting addresses are defined (MMFF0C, MMFF10). One is required. The second is required for double buffering.

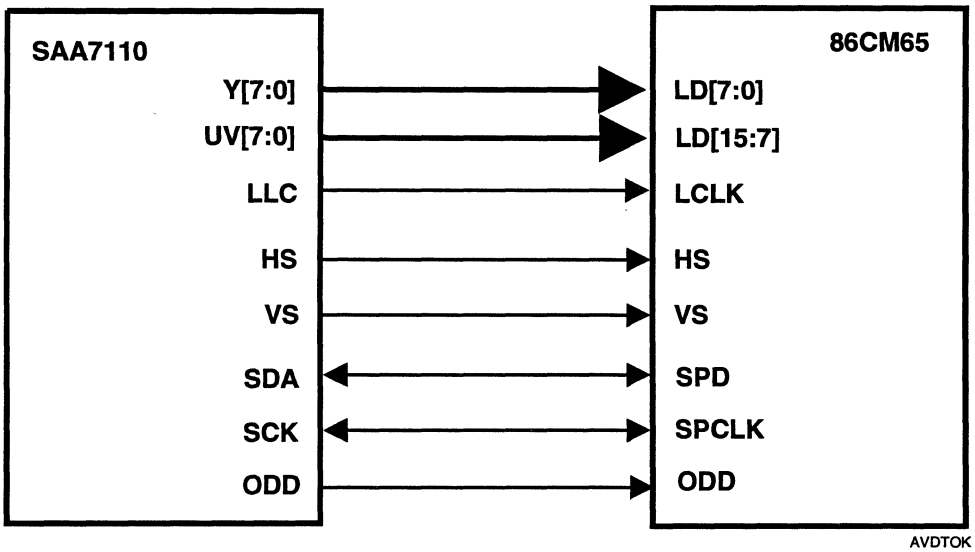


Figure 12-12. 86CM65 to SAA7110 Digitizer Interface

- The horizontal and vertical decimation registers are programmed (MMFF2C, MMFF30). This is optional.
- The video input window size (height in lines and width in pixels) is programmed in MMFF24.
- The video data horizontal and vertical offsets are programmed in MMFF28.
- The line offset (stride) is programmed (MMFF34_10-0).

The SAA7110 then sends video data as shown in Figure 12-13. In this figure, both VSYNC (VS) and HSYNC (HS) have active high polarity. The vertical offset (MMFF28_24-16) is 1, meaning the first line is skipped. The horizontal offset HO (MMFF28_11-0) is 1, meaning that the first data starts one clock after the second HS goes low. HS goes high again some time after the last byte of the line, whose position is specified by the line width (LW) programmed in MMFF24_11-0. The widths of the VS and HS pulses shown may vary.

To provide a full interlaced video output to a TV set, double buffering must be used. One buffer (LPB address 0) specifies the start of the even field data. The other buffer (LPB address 1) specifies the start of the odd field data. The Streams Processor buffer starting addresses must be correspondingly programmed. MMFF00_30 is set to 1 to direct the incoming data to the proper buffer based on the state of the ODD input. If required, the ODD signal can be inverted before it is sampled by setting MMFF00_29 to 1. Pin M17 in configured as the ODD input when the memory type is 256Kx16 and PWM operation is disabled (SR52_0 = 0).

The state of the ODD signal can be read via MMFF04_20. MMFF04_21 can be read to determine which buffer is being used to store incomming data.

If digitizer output to a CR or flat panel is required, alternate frames of the video input must be discarded (not written to memory) by setting bit 5 of MMFF00 to 1.

If the digitizer has an 8-bit interface, Video 8 In mode is selected by programming MMFF00_3-1 to 010b.

12.3 HOST PASS-THROUGH

When pass-through mode is enabled (MMFF00_3-1 = 100b), the CPU can write 32-bit data to the output FIFO and have this data passed directly to the decimation block (bypassing the LPB bus). The data are sent exactly as for compressed video data to an MPEG decoder. The data will then be decimated according to the programming of MMFF2C (horizontal) and MMFF30 (vertical) and then passed to the video FIFO to be written to display memory. This path is shown in Figure 12-1.

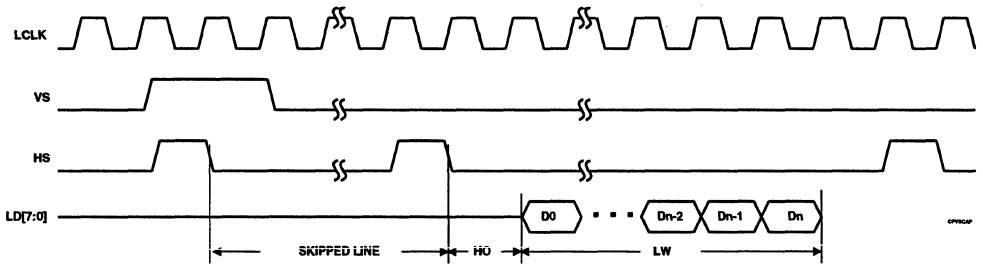


Figure 12-13. Video 8 In or 16 Mode Input

When the Host sends an HSYNC (MMFF00_12 = 1) or VSYNC (MMFF00_11), the decimation registers are re-loaded. Therefore, the Host must ensure that at least 5 clocks pass between the sync and the start of data to allow time for this reloading.

Pass-through is not supported if big-endian addressing is being used.

12.4 ZV PORT INTERFACE

The ZV Port, or Zoomed Video Port, allows direct transmission of video data from a PC Card to the 86CM65. The 86CM65 supports ZV Port operation when its LPB function is enabled (MMFF00_0 = 1) and LCLK is selected (MMFF00_24 = 1). The following setup is done for ZV Port operation:

- Video 16 mode is selected (MMFF00_3-1 = 001b)
- The ZV Port enable bit is set (MMFF00_31 = 1)
- MMFF090_9 and MMFF00_10 must be set to 1 to specify active high HSYNC (HS) and VSYNC (VS).
- Byte swapping is disabled by setting MMFF00_6 to 1.
- One or two frame buffer starting addresses are defined (MMFF0C, MMFF10). One is required. The second is required for double buffering.
- The horizontal and vertical decimation registers are programmed (MMFF2C, MMFF30). This is optional.
- The video input window size (height in lines and width in pixels) is programmed in MMFF24.
- The video data horizontal and vertical offsets are programmed in MMFF28.
- The line offset (stride) is programmed (MMFF34_10-0).

During ZV Port operation, the 86CM65 automatically detects even and odd video fields based on the state of HS on the falling edge of VS.

The interface is shown in Figure 12-14.

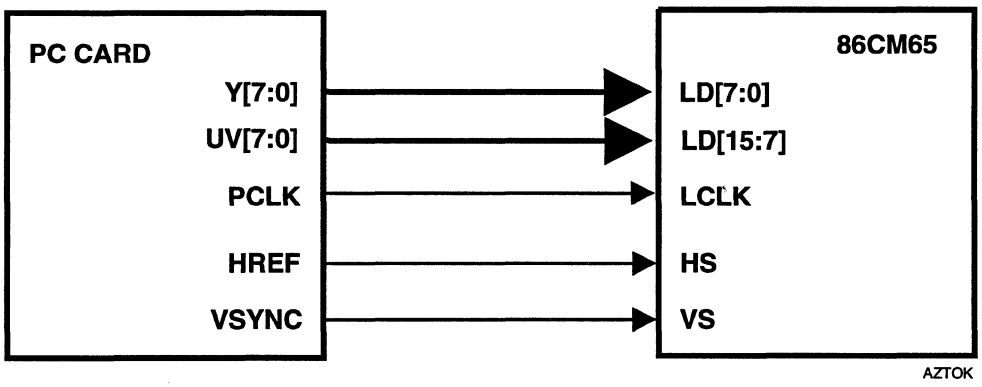


Figure 12-14. ZV Port Interface

Section 13: Miscellaneous Functions

This section explains the video BIOS ROM interface, the General I/O Ports and interrupt generation.

13.1 VIDEO BIOS ROM INTERFACE

For mobile systems, the video BIOS is usually part of the system ROM. A separate ROM interface is supported for testing purposes.

The RD[7:0] (ROM data) and RA[15:0] (ROM address) signals are multiplexed on the PD[23:16] and PD[15:0] pins respectively. The $\overline{\text{ROMEN}}$ (ROM chip enable) signal is multiplexed with the FPPOL signal. $\overline{\text{ROMEN}}$ is selected when SR1A_5 = 0. The BIOS ROM must be shadowed immediately after reset (as the PCI standard requires) and BIOS access disabled to prevent interference with graphics operation.

13.2 GENERAL INPUT PORT

The 86CM65 provides a 4-bit General Input Port (GIP) as part of its LPB function. The following steps are required to implement it.

1. Disable all other LPB uses.
2. Enable sensing of the desired input data on LD[7:4].
3. If the LPB General Output Port function is also in use, ensure that the correct output data is programmed in MMFF1C_3-0.
4. Program SR1A_4 to 1 to select $\overline{\text{STWR}}$.
5. Write (anything) to CR5C. The data on LD[7:4] are latched 2 DCLKs later into MMFF1C_7-4. (This also drives the contents of MMFF1C_3-0 onto LD[3:0] and generates the $\overline{\text{STWR}}$ pulse on pin C3. The

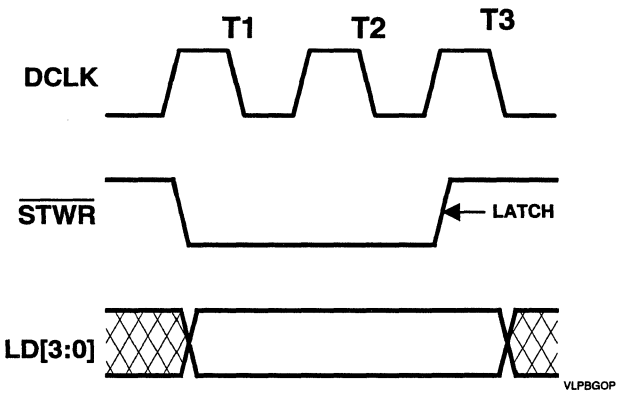


Figure 13-1. General I/O Port Timing

input data is latched on the rising edge of STWR. See Figure 13-1)

6. Disable sensing of input data on LD[7:4].

13.3 GENERAL OUTPUT PORT

The 86CM65 provides a 4-bit General Output Port (GOP) as part of its LPB function. To implement this:

1. Disable all other LPB uses.
2. Program the desired output in MMFF1C_4-0.
4. Program SR1A_4 to 1 to enable output of STWR on pin C3.
5. Write (anything) to CR5C. The data in MMFF1C_3-0 are immediately driven onto LD[3:0] and the STWR pulse is generated. The rising edge of STWR (2 DCLKs after it is asserted) can be used to latch the data into an external device. The data is held valid for 1/2 DCLK after this edge. See Figure 13-2.

The 86CM65 also provides a 1-bit GOP on a dedicated pin. To implement this:

1. Clear SR1A_4 to 0b to make pin C3 act as GOP0.
2. Program the desired output in CR5C_0. This statically drives the state of CR5C_0 onto the GOP0 pin. This pin will continue to reflect the register bit states as long as SR1A_4 = 0. The value in CR5C_0 can be reprogrammed at any time.

13.4 SERIAL COMMUNICATIONS PORT

A serial communications port is implemented in the MMFF20 register. Bit 4 is set to 1 to enable the interface. The clock is written to bit 0 (= 0) and data to bit 1 (= 0), driving the SPCLK and SPD pins low respectively. The state of the SPCLK pin can be read via bit 2 and the state of the SPD pin can be read via bit 3. The SPCLK and SPD pins are tri-stated when their corresponding control bits are reset to 0, allowing other devices to drive the serial bus.

Typical uses for the serial port are for DDC monitor communications and I^2C interfacing. When SPCLK and SPD are tri-stated, the 86CM65 can detect an I^2C start condition (SPD driven low while SPCLK is not driven low). This condition is generated by another I^2C master that wants control of the I^2C bus. If bit 19 of MMFF08 is set to 1, detection of a start condition generates an interrupt and sets bit 3 of MMFF08 to 1. If bit 24 of MMFF08 is set to 1, the 86CM65 drives SPCLK low to generate I^2C wait states until the Host can clear the interrupt and service the I^2C bus.

If PD26 is strapped low at reset, strapping of PD25 selects either E2H (PD25 pulled high) or E8H (PD25 pulled low) as the I/O port address for the Serial Port register. This allows the ports to be used for serial communications, typically I^2C, even when the 86CM65 is not enabled.

13.5 INTERRUPT GENERATION

Whatever the mode of operation (VGA or Enhanced), bit 4 of CR32 must be set to 1 to enable interrupt generation. When an enabled interrupt is generated, INTA is pulled low.

When the 86CM65 is being operated in VGA mode (CR67_0 = 0), only a vertical retrace can generate an interrupt. This is enabled when bit 5 of CR11 is cleared to 0 and a 1 has been programmed into bit 4 of CR11. When an interrupt occurs, it is cleared by writing a 0 to bit 4 of CR11. The interrupt must then be re-enabled by writing a 1 to the same bit. Note that the BIOS clears both bit 4 and bit 5 of CR11 to 0 during power-on, a mode set or a reset. Thus, interrupt generation is disabled until bit 4 is set to 1.

When the 86CM65 is being operated in Enhanced mode (CR67_0 = 1), interrupts can be generated by a vertical retrace, Graphics Engine busy, command FIFO overflow and command FIFO empty. These interrupts are enabled and cleared and their status reported via 42E8H.

Multiple interrupts can be enabled at the same time in Enhanced mode. The interrupt pin will remain asserted until all interrupt status bits are cleared.

Section 14: Basic Software Functions

This section describes some of the basic operations required to program 86CM65.

14.1 CHIP WAKEUP

The following program wakes up the 86CM65. This is required for systems that do not use the S3 style of video BIOS, e.g, UNIX.

```
mov dx,3c3h        ; Video Subsystem Enable register address
mov al,01h         ; bit 0 = 1, enable graphics display
out dx,al          ; write new bit values to 3c3h
mov dx,3cch        ; Miscellaneous Output Read register
in al,dx           ; Read 3cch
[load CRTCs]       ; program CRTC registers
mov dx,3C6h        ; DAC Mask register address
mov al,FFh         ; DAC Mask register initialization value
out dx,al          ; Initialize DAC mask and release BLANK signal
  .
  .
  .
```

14.2 REGISTER ACCESS

S3 has added a number of graphics registers to the standard VGA set. These can be locked when not in use to prevent accidental access and unlocked when access is requires. This section explains how this is done.

14.2.1 Unlocking the S3 Registers

The S3 registers (CR30 and higher plus the Enhanced Commands registers) must be unlocked before they can be accessed by the CPU. The code to do this is:

Note: Byte operations are used in the following examples for clarity. Word operations, e.g.,

mov ax, 4838h
out dx,ax

should be used for efficiency instead of the operations used in the first example below.

```
; Write code to SR8 to provide access to the S3 extended Sequencer registers
(SR9-SRFF)
;
   mov dx,3c4h        ; copy index register address into dx
   mov al,08h         ; copy index for SR8 register into al
   out dx,al          ; write index to index register
   inc dx             ; increment dx to 3c5h (data register address)
   mov al,06h         ; copy unlocking code (xxxx0110b, x=don't care) to al
   out dx,al          ; write the unlocking code to the data register
   dec dx             ; restore the index register address to dx
;
; Write code to CR38 to provide access to extended CRTC registers CR2D-CR3F
;
   mov dx,3d4h        ; copy index register address into dx
   mov al,38h         ; copy index for CR38 register into al
   out dx,al          ; write index to index register
   inc dx             ; increment dx to 3D5h (data register address)
   mov al,48h         ; copy unlocking code (01xx10xxb, x=don't care) to al
   out dx,al          ; write the unlocking code to the data register
   dec dx             ; restore the index register address to dx
;
; Write code to CR39 to provide access to extended CRTC registers CR40-CRFF
;
; dx is already loaded with 3D4h because of the previous instruction
;
   mov al,39h         ; copy index for CR39 register into al
   out dx,al          ; write index to index register
   inc dx             ; increment dx to 3D5h (data register address)
   mov al,0a5h        ; copy unlocking code to al (the code a5H also unlocks
                      ; access to configuration registers CR36, CR37 and CR68
   out dx,al          ; write the unlocking code to the data register
   dec dx             ; restore the index register address to dx
;
; Set bit 0 in CR40 to enable access to the Enhanced Programming registers.
;
; dx is already loaded with 3D4h because of previous instruction
   mov al,40h         ; copy index for CR40 register into al
   out dx,al          ; write index to index register
   inc dx             ; increment dx to 3D5h (data register address)
   in al,dx           ; read register data for read/modify/write operation
   or al,1            ; set bit 0 to 1
   out dx,al          ; write the unlocking code to the data register
   dec dx             ; restore the index register address to dx
```

14.2.2 Locking the S3 Registers

Relocking the S3 registers is done by repeating the code used to unlock the registers except:

1. The values written to the SR8, CR38 and CR39 registers must change at least one of the significant bits in the valid code pattern. For example, 00h will always accomplish this.

2. After first verifying that the Graphics Engine is not busy (bit 9 of 9AE8H is 0), bit 0 of CR40 must be cleared to 0. A read-modify-write cycle must be used instead of the code used above to prevent overwriting of any changes made to bits 7-1 in CR40 since reset.

```
mov dx,3d4h        ; copy index register address into dx
mov al,40h         ; copy index for CR40 register into al
out dx,al          ; write index to index register
inc dx             ; increment dx to 3D5h (data register address)
in al,dx           ; read content of CR40 into al
and al,0feh        ; clear bit 0 to 0
out dx,al          ; write to CR40 to lock the Enhanced Commands registers
dec dx             ; restore the index register address to dx
```

14.3 TESTING FOR THE PRESENCE OF AN 86CM65 CHIP

After unlocking, an 86CM65 chip can be identified via CR2E. The following code aborts the driver program and returns to DOS if an 86CM65 chip is not found.

```
mov dx,3d4h        ; copy index register address into dx
mov al,2eh         ; copy index for CR2E register into al
out dx,al          ; write index to index register
inc dx             ; increment dx to 3D5h (data register address)
in al,dx           ; read content of CR2E into al
cmp al,12h         : compare chip ID to the desired chip ID (12h)
jne not_12         ; jump to a label if chip ID does not match desired ID
.                  ; 86CM65 found - continue with setup
.
.
```

Specific revisions of the chip can be identified via CR2F. The PCI configuration space device and revision ID fields can also be used to identify the chip.

14.4 GRAPHICS MODE SETUP

Some programs may require a graphics mode other than that provided by standard operation. For example, a DOS game may require a resolution of 640x400x8 (VESA mode 100) instead of the standard DOS mode, e.g., mode 03. The following code fragment shows how this is done.

```
mov ax,4f02h       ; VESA super VGA mode function call
mov bx,100h        ; mode 100
int 10h            ; call video BIOS
```

Section 15: VGA Compatibility Support

This section describes 86CM65 support for standard VGA and VESA Super VGA graphics standards.

15.1 VGA COMPATIBILITY

The 86CM65 is compatible with the VGA standard. These modes are not accelerated using the Graphics Engine. However, other design features provide excellent VGA performance.

Several of the standard VGA registers have been modified or extended in the 86CM65. Table 15-1 describes these changes.

Table 15-1. Standard VGA Registers Modified or Extended in the 86CM65

Register	Change to Standard VGA Definition
CR0	Extension bit 8 is bit 0 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size. The flat panel equivalent is SR60.
CR1	Extension bit 8 is bit 1 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size. The flat panel equivalent is SR61.
CR2	Extension bit 8 is bit 2 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size. The flat panel equivalent is SR62.
CR3	The length of the blanking pulse defined in this register can be extended by 64 DCLKs via bit 3 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size. The flat panel equivalent is SR63.
CR4	Extension bit 8 is bit 4 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size. The flat panel equivalent is SR64.
CR5	The length of the HSYNC pulse defined in this register can be extended by 32 DCLKs via bit 5 of CR5D. Bit 5 of CR35 controls access to this register. Bit 7 of CR43 doubles the parameter size. The flat panel equivalent is SR65.
CR6	In addition to the standard VGA extensions (bit 8 is bit 0 of CR7, bit 9 is bit 5 of CR47), bit 10 is bit 0 of CR5E. Bit 4 of CR35 controls access to this register. The flat panel equivalent is SR68.
CR7	Bit 4 of CR35 controls access to bits 0, 2, 3, 5 and 7 of this register.
CR9	Bit 4 of CR35 controls access to bit 5 of this register.
CRC	The display start address is a 20-bit value for the 86CM65. The extension bits (20-16) are bits 4-0 of CR69.
CRE	The cursor location address is a 20-bit value for the 86CM65. The extension bits (20-16) are bits 4-0 of CR69.

CR10	In addition to the standard VGA extensions (bit 8 is bit 2 of CR7, bit 9 is bit 7 of CR7), bit 10 is bit 4 of CR5E. Bit 4 of CR35 controls access to this register. The flat panel equivalent is SR6C.
CR11	Bit 4 of CR35 controls access to bits 3-0 of this register. Bit 6 (3/5 refresh cycles per line) can be overridden by CR3A_2-0. Setting bit 1 of CR33 to 1 disables the write protect effect of bit 7 of this register on bits 1 and 6 of CR7. The flat panel equivalent is SR6D.
CR12	In addition to the standard VGA extensions (bit 8 is bit 1 of CR7, bit 9 is bit 6 of CR7), bit 10 is bit 1 of CR5E. The flat panel equivalent is SR69.
CR13	Bit 2 of CR43 is the old extension bit (bit 8) of this register. Bits 5-4 of CR51 are the new extension bits (bits 9-8) of this register.
CR15	In addition to the standard VGA extensions (bit 8 is bit 3 of CR7, bit 9 is bit 5 of CR9), bit 10 is bit 2 of CR5E. Bit 4 of CR35 controls access to this register. The flat panel equivalent is SR6A.
CR16	Bit 4 of CR35 controls access to this register. The flat panel equivalent is SR6B.
CR17	Bit 5 of CR35 controls access to bit 2 of this register.
CR18	In addition to the standard VGA extensions (bit 8 is bit 4 of CR7, bit 9 is bit 6 of CR9), bit 10 is bit 6 of CR5E.
AR00-AR0F	Bit 6 of CR33 controls access to these registers.
3C6H-3C9H	Bit 4 of CR33 controls writes to these registers.

For a detailed discussion of VGA programming, see *Programmer's Guide to the EGA, VGA and Super VGA Cards, 3rd Edition* by Richard F. Ferraro (Addison-Wesley Publishing Company, Inc).

15.2 VESA SUPER VGA SUPPORT

The 86CM65 supports the extended (Super) VGA modes defined by VESA. All modes are accelerated by the Graphics Engine except for the planar (4 bits/pixel) ones.

Section 16: Enhanced Mode Programming

Enhanced mode provides a level of performance far beyond what is possible with the VGA architecture. Hardware line drawing, BitBLT, rectangle fill and other drawing functions are implemented. Also implemented are data manipulation functions, such as data extension, data source selection, and read/write bitplane control. Hardware clipping is supported by 4 registers that define a rectangular clipping area. While in Enhanced mode, the display memory bit map can be updated in two ways. One is to have the CPU write directly to memory. (This is also possible in non-Enhanced modes via paging.) The other is to have the CPU issue commands to the Graphics Engine, which then controls pixel updating. This section explains these two methods and provides a comprehensive set of Enhanced mode programming examples.

16.1 LINEAR ADDRESSING FOR DIRECT VIDEO MEMORY CPU ACCESSES

Linear addressing is useful when software requires direct access to display memory. Enhanced mode operation must be enabled before linear addressing is enabled. This means that bit 0 of 4AE8H is set to 1 to enable Enhanced mode functions and bit 3 of CR31 is set to 1 to specify Enhanced mode memory mapping.

The 86CM65 provides linear addressing of up to 2 MBytes of display memory. The Graphics Engine busy flag, bit 9 of 9AE8H, should be verified to be 0 (not busy) before linear addressing is enabled by setting bit 4 of CR58 to 1. The size of the linear address window is set via bits 1-0 of CR58. The base address for the linear addressing window is set via CR59 and CR5A (or via the Base Address 0 (Index 10H) PCI configuration register).

For operation in real mode, the linear addressing window size can be set to 64 KBytes. The base address for the window is set to A0000H by programming bits 31-16 of the window position in CR59-CR5A to 000AH. The memory page offset (64K bank) specified in bits 4-0 of CR6A is added to the linear addressing window position base address, allowing access to up to 4 MBytes of display memory through a 64-KByte window.

The above discussion applies when the 86CM65 is programmed for backwards-compatible MMIO operation. See Section 16.3.2 for instructions on how to perform linear addressing when new MMIO is enabled.

16.2 VIDEO MEMORY ACCESS THROUGH THE GRAPHICS ENGINE

When updating the display bitmap through the Graphics Engine, all CPU data moves through the Pixel Data Transfer registers (E2E8H and E2EAH). These can be memory mapped as explained in Memory Mapping of Enhanced Mode Registers later in this section.

The Graphics Engine manipulates the bits for each pixel to assign a color index or true color value, which is then translated via a programmable RAMDAC before being displayed on a CRT. Selected bits in a pixel can be masked off from being displayed by programming the DAC Mask register (3C6H). The 86CM65 can manipulate 64 bits each clock cycle, from two 32-bit pixels to eight 8-bit pixels.

Figure 16-1 is a flowchart for the process of updating the color of each pixel. Start at the block labeled 'New Color' in the middle of Figure 16-1. At this stage, a color has been determined that may or may not be used to update a pixel in the bitmap. How this color is determined will be covered later.

The first hurdle for the new color is the color compare process. If this is turned off (bit 8 of BEE8H, Index 0EH = 0), the new color is passed to the Write Mask register (AAE8H). If the plane to which the pixel update is directed has been masked off in this register, no update occurs. Otherwise, the new color value is written to the bitmap.

If color compare is enabled (bit 8 of BEE8H, Index 0EH = 1), the new color value (source) is compared to a color value programmed into the Color Compare (B2E8H) register. The sense of the color comparison is determined by the SRC NE (source not equal) bit (bit 7) of BEE8H, Index 0EH. If this bit is 0, the new pixel color value is passed to the write mask only when the source color does not match the color in the Color Compare register. If this bit is 1, the new pixel color value is passed to the write mask only when the source color matches the color in the Color Compare register. If the new pixel color value is not passed to the write mask, no update occurs. Notice that the source color is used for the comparison, as opposed to the destination (bitmap) color used by the standard VGA color compare operation.

The new color is the result of a logical mix performed on a color source and the current color in the bitmap. For example, the color source could be XORed with the bitmap color. The new color can also be selected by operating on only the color source or the bitmap color, e.g., NOT color source. Both the color source and the logical mix operation are specified in either the Background Mix register (B6E8H) or the Foreground Mix register (BAE8H). Which of these two registers is used is determined by the settings of bits [7:6] of the Pixel Control register (BEE8H, Index 0AH).

To set up the pixel color updating scheme, the programmer specifies one of four color sources by writing bits 6-5 of the Background Mix and Foreground Mix registers. The color sources are:

- Background Color register (A2E8H)
- Foreground Color register (A6E8H)
- CPU (via the Pixel Data Transfer registers (E2E8H, E2EAH))
- Current display bitmap color index

One of 16 logical operations is chosen by writing bits 3-0 of the Background Mix and Foreground Mix registers. Examples of logical operations are making the new pixel color index equal to the NOT of the current bitmap color index or making the new index equal to the XOR of the source and current bitmap indices.

When the logical operation and color source have been specified in the Background and Foreground Mix registers, bits 7-6 of the Pixel Control register are written to specify the source of the mask bit

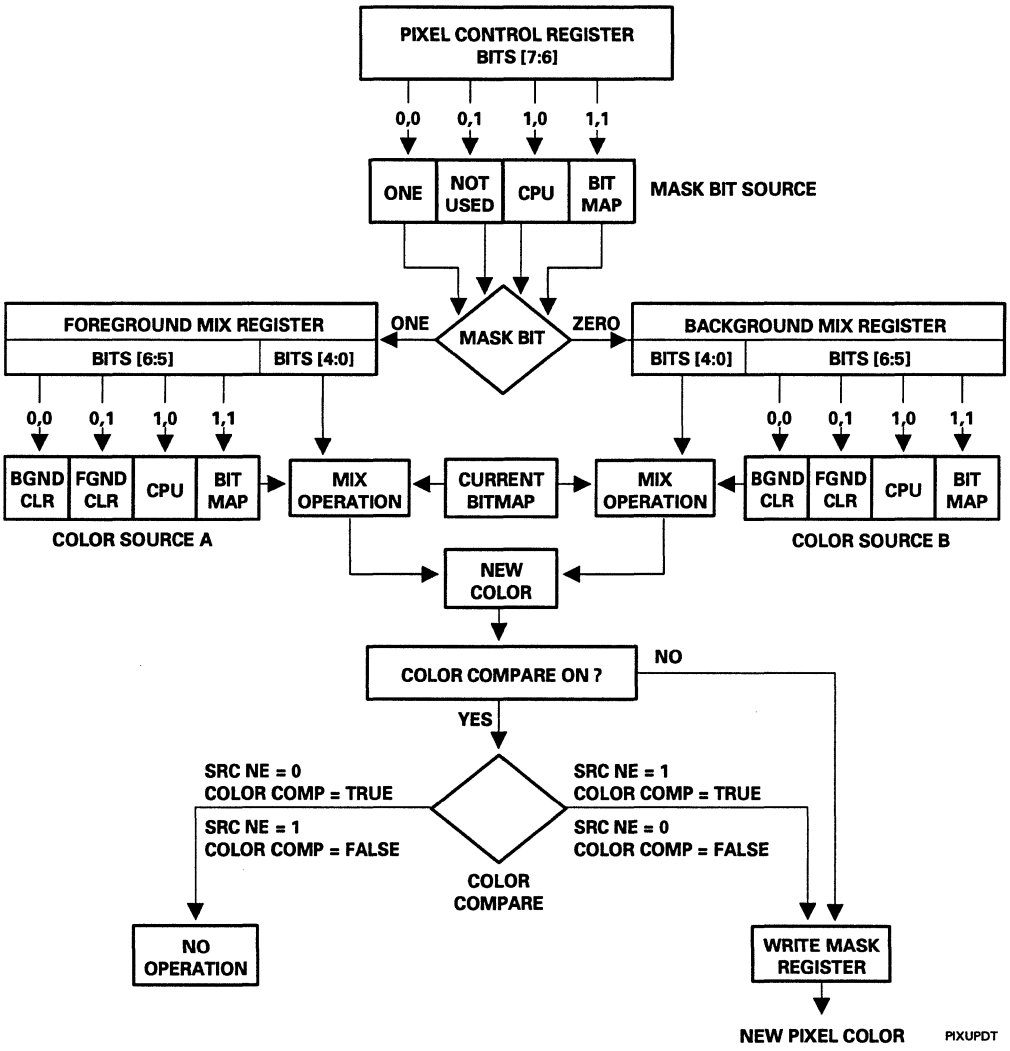


Figure 16-1. Pixel Update Flowchart

value. If the resulting mask bit is a 'ONE', the Foreground Mix register is used to determine the color source and mix. If the mask bit is a 'ZERO', the Background Mix register is used to determine the color source and mix. There are three sources for the mask bit value:

- Always ONE (Foreground Mix register used)
- CPU (via the Pixel Data Transfer registers (E2E8H, E2EAH))
- Bitmap

Setting bits 7-6 to 00b sets the mask bit to 'ONE'. All drawing updates to the video bitmap use the Foreground Mix register settings. This setup is used to draw solid lines, through-the-plane image transfers to display memory and BitBLTs.

If bits 7-6 are set to 10b, the mask bit source is the CPU. After the draw operation command is issued to the Drawing Command register (9AE8), a mask bit corresponding to every pixel drawn on the display must be provided via the Pixel Data Transfer register(s). If the mask bit is 'ONE', the Foreground Mix register is used. If the mask bit is 'ZERO', the Background Mix register is used. Note that if the color source is the CPU, the mask bit source cannot also be the CPU, and vice versa. This setup is used to transfer monochrome images such as fonts and icons to the screen.

If bits 7-6 are set to 11b, the current display bit map is selected as the mask bit source. The Read Mask register (AAE8H) is set up to indicate the active planes. When all bits of the read-enabled planes for a pixel are a 1, the mask bit 'ONE' is generated. If any one of the read-enabled planes is a 0, then a mask bit 'ZERO' is generated. If the mask bit is 'ONE', the Foreground Mix register is used. If the mask bit is 'ZERO', the Background Mix register is used. Note that if the color source is the bitmap, the mask bit source cannot also be the bitmap, and vice versa. This setting is used to BitBLT patterns and character images.

16.3 MEMORY MAPPING OF REGISTERS

The 86CM65 provides two memory-mapped I/O (MMIO) schemes. One method is identical to that provided by the Trio64 and provides compatibility with older software. This provides memory mapping of a limited number of Enhanced mode registers plus the LPB and Streams Processor registers. Packed register access is also provided. The second method incorporates linear addressing and provides memory mapping of all registers, including the packed registers. The second method also allows big or little endian addressing. Each of these MMIO methods is described below.

16.3.1 Backward-Compatible MMIO

Most of the Enhanced registers can be memory-mapped (MMIO). This function is enabled by setting bits 5-4 of CR53 to 10b.

Image writes normally made via I/O addresses E2E8H and E2EAH (the Pixel Data Transfer registers) are made instead by accessing any memory location in the 32-KByte address space from A0000H to A7FFFH. This allows efficient use of the MOVSW and MOVSD assembly language commands. Accesses must be to even word or doubleword addresses, depending on the specification of the bus width via bits 10-9 of 98E8H. Software must not make E2E8H, E2EAH writes beyond the A7FFFH range.

Accesses to the Enhanced command registers are made to particular locations in the A8000H to AFFFFH address range as shown in Table 16-1. Both 16-bit reads and writes are supported. Only 32-bit writes (bit 9 of BEE8H_E set to 1) are supported.

If MMIO is enabled, bit 7 of SR9 allows register access to be either I/O or MMIO or MMIO only.

Table 16-1 Enhanced Registers Memory Mapping

Register Mnemonic	I/O Address (Hex) MMIO = Axxxx	Register Mnemonic (Packed)	Packed MMIO Address (Hex) (Axxxx)
CUR_Y, CUR_X	82E8, 86E8	ALT_CURXY	8100, 8102
DESTY_AXSTP, DESTX_DIASTP	8AE8, 8EE8	ALT_STEP	8108, 810A
ERR_TERM	92E8		8110
CMD	9AE8		8118
SHORT_STROKE	9EE8		811C
BKGD_COLOR	A2E8		8120
FRGD_COLOR	A6E8		8124
WRT_MASK	AAE8		8128
RD_MASK	AEE8		812C
COLOR_CMP	B2E8		8130
BKGD_MIX, FRGD_MIX	B6E8, BAE8	ALT_MIX	8134, 8136
SCISSORS_T, SCISSORS_R	BEE8_1, BEE8_2		8138, 813A
SCISSORS_B, SCISSORS_R	BEE8_3, BEE8_4		813C, 813E
PIX_CNTL, MULT_MISC2	BEE8_A, BEE8_D		8140, 8142
MULT_MISC, READ_SEL	BEE8_E, BEE8_F		8144
MIN_AXIS_PCNT, MAJ_AXIS_PCNT	BEE8_0, 96E8	ALT_PCNT	8148, 814A
PIX_TRANS	E2E8, E2EA	PIX-TRANS	

For improved performance, most of the Enhanced mode registers can also be written (but not read) via a packed configuration. The 16-bit registers are paired so that two registers can be accessed via a single 32-bit write. The addresses for this packed configuration are given in Table 16-1. The packed register access function is enabled when MMIO is enabled.

The 86CM65 supports the Trio64 MMIO scheme when bits 4-3 of CR53 are programmed to 10b and bit 5 of CR53 is cleared to 0. In addition, the LPB and Streams Processor registers are also accessible in the A8000H - AFFFFH window. If bit 5 of CR53 is set to 1, the registers are accessible in the B8000H - BFFFFH window. However, image writes cannot be made to B0000H - B7FFFH. This region and the entire A0000H - AFFFFH region are left free for VGA memory and other uses.

The Trio64 scheme is also available as explained in the previous paragraph when bit 4-3 of CR53 are set to 11b. In this case, the registers can be accessed either by this scheme or by the new MMIO explained in the next section.

16.3.2 New MMIO

The new MMIO method for the 86CM65 provides a 64-MByte addressing window starting at the base address specified in CR59-5A. This space is divided into a 32-MByte space for little endian (Intel-style) addressing and a 32-MByte space for big endian (Power PC-style) addressing. All registers and data transfer locations are mapped into this area as shown in Table 16-2.

Table 16-2 New MMIO Addresses

Lower 32 MBytes - Little Endian Addressing	
Description	**Offset From Base (Hex)**
Linear Addressing (16M)	000 0000 - 0FF FFFF
Image Data Transfer (32K)	100 0000 - 100 7FFF
PCI Configuration Space Registers	100 8000 - 100 8043
Packed Enhanced Registers	100 8100 - 100 814A
Streams Processor Registers	100 8180 - 100 81FF
Current Y Position Register	100 82E8
CRT VGA 3B? Registers	100 83B0 - 100 83Bx
CRT VGA 3C? Registers	100 83C0 - 100 83Cx
CRT VGA 3D? Registers	100 83D0 - 100 83Dx
Subsystem Status Enhanced Register (42E8H)	100 8504
Advanced Function Control Register (4AE8H)	100 850C
Enhanced Registers	100 86E8 - 100 EEEA
Local Peripheral Bus Registers	100 FF00 - 100 FF5C

The new MMIO (only) is enabled by setting bits 4-3 of CR53 to 01b. It is also enabled in conjunction with the old MMIO scheme when bits 4-3 of CR53 are set to 11b. This is the default configuration, allowing PCI software immediate access to all registers and the ability to relocate the address space. To allow MMIO accesses only, bits 1-0 of the PCI Command register (offset 04H) can be programmed to 10b.

With the new MMIO enabled, the first 16 MBytes of each 32M address space (big and little endian) are dedicated to linear addressing. A maximum of 2 MBytes of each address space (starting at the lowest address of the space) is usable with the 86CM65. The base address is taken from bits 31-26 of the linear address window position (bits 7-2 of CR59 or the high order 6 bits of the PCI Base Address 0). This is concatenated with the display memory address specified by the programmer.

In addition to enabling the new MMIO, the programmer must also enable linear addressing and specify the window size exactly as required for the old linear addressing. Note that since only bits 31-26 are used to specify the base address, A0000H cannot be specified and the 64K banking scheme possible with the old linear addressing cannot be used with the new linear addressing.

When big endian addressing is used, the required byte swapping for linear addressing is specified by bits 2-1 of CR53. This applies to both reads and writes.

16.4 PROGRAMMING

Three different programming schemes are available, I/O, standard MMIO and packed register MMIO. Examples of how each is used to assign vertical and horizontal coordinates to Current X and Y Position registers (82E8H and 86E8H) are:

I/O Format:

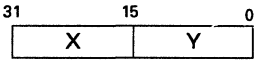
```
MOV  DX,CUR_X
MOV  AX,X
OUT  DX,AX
MOV  DX,CUR_Y
MOV  AX,Y
OUT  DX,AX
```

Standard MMIO Format:

```
Enable MMIO
Point ES to A000H
Load x and y values into AX and BX
MOV  ES:[CUR_Y], BX
MOV  ES:[CUR_X], AX
```

Packed Register MMIO:

```
Enable MMIO
Point ES to A000H
Load the x and y values into EAX (y value in the low word and x value in the high word), I.e.,
```




```
MOV  ES:[ALT_CURXY], EAX
```

The packed register MMIO scheme is the most efficient and is used where appropriate in the programming examples provided later in this section. All assume that the ES register points to A000H.

16.4.1 Notational Conventions

The REGMNEMONIC on the left hand side of the arrow is the register mnemonic of the I/O port being written into. Text following a ';' is a comment.

```
REGMNEMONIC ⇐ XXXXH                ; Load a hexadecimal value into the register.
REGMNEMONIC ⇐ XXXXD                ; Load a decimal value into the register.
REGMNEMONIC ⇐ XXXX                 ; Load a decimal value into the register
REGMNEMONIC ⇐ XXXXXXXXXXXXXXXXB   ; Load a binary value into the register.
```

Image transfers (CPU pixel data writes to the frame buffer) are notated as follows:

```
COUNT
PIX_TRANS ⇐ IMAGEDATA
```

The COUNT is the number of CPU writes. PIX_TRANS means either the E2E8H, E2EAH pixel transfer registers or the 32K memory space from A0000H to A7FFFH as explained in Section 16.3.1 above.

16.4.2 Initial Setup

All examples assume the desired mode is selected.

The Bitmap Access Through the Graphics Engine section earlier in this section explains in detail how the colors, mixes and the data extensions are set for each example. These registers need not be set repeatedly before a series of draw commands if they use the same colors, mixes and data extension.

All bitmap updates are affected by the settings in the clipping registers (BEE8H, Indices 1-4) and the choice of internal or external clipping (BEE8H, Index E, bit 5). These must be set up so they include the area being drawn into.

If color compare is to be used, it must be enabled by setting bit 8 of BEE8H, Index 0EH to 1. Bit 7 of this register determines whether a TRUE or FALSE comparison allows the pixel update to continue. The comparison color is programmed into the Color Compare register (B2E8).

All planes are enabled for writing unless explicitly set otherwise in an example. This is done via the Write Mask register (AAE8H).

16.4.3 Programming Examples

This section provides programming examples for the following Enhanced mode drawing operations:

- Solid Line
- Textured Line
- Rectangle Fill Solid
- Image Transfer—Through the Plane
- Image Transfer—Across the Plane
- BitBLT—Through the Plane
- BitBLT—Across the Plane
- PatBLT—Through the Plane
- PatBLT—Across the Plane
- Short Stroke Vectors
- Programmable Hardware Cursor

Some programming steps are repeated in multiple examples. They are explained in detail at their first occurrence. Therefore, readers are encouraged to work through the examples from first to last. The register mnemonics used in the examples are listed in Table 15-1. Other mnemonics used are:

Mnemonic	Description
NEW	Mix = 00111b in bits 4-0 of BAE8H or B6E8H. This overwrites the present bitmap color value with a new value.
XOR	Mix = 00101b in bits 4-0 of BAE8H or B6E8H. The current bitmap color is XORed with the new color.

16.4.3.1 Solid Line

This command draws a one pixel wide solid line from screen coordinates x1,y1 to x2,y2. Bresenham parameters are used to define the line. The Pixel Control register (BEE8H, Index AH) must be set to A000H to select the Foreground Mix register to specify the color source and mix type.

Setup:

Drawing a line using axial coordinates requires programming the axial step constant into the Destination Y-Position/Axial Step Constant (8AE8H) register (DESTY_AXSTP), the diagonal step constant into the Destination X-Position/Diagonal Step Constant (8EE8H) register (DESTX_DIASTP) and the error term into the Error Term (92E8H) register (ERR_TERM). Calculation of these Bresenham parameters is based on the MAX and MIN parameters as calculated below.

MAX = maximum(ABS(x2–x1), ABS(y2–y1))
MIN = minimum(ABS(x2–x1), ABS(y2–y1))

where maximum means choose the largest of the two terms in parentheses and minimum means choose the smallest. ABS means take the absolute value of the expression.

Bits 7-5 of the Drawing Command (9AE8H) register (CMD) specify the drawing direction. Setting bit 7 to 1 means that the Y drawing direction is positive (y1 < y2). Clearing bit 7 to 0 means the Y drawing direction is negative (y1 > y2). Setting bit 6 to 1 means that Y is the major (longer) axis (ABS(x2–x1) > ABS(y2–y1)). Clearing bit 6 to 0 means that X is the major axis. Setting bit 5 to 1 means that the X drawing direction is positive (x1 < x2). Clearing bit 5 to 0 means that the X drawing direction is negative (x1 > x2). These values replace the DDD sequence in the write to the CMD register shown in the pseudocode below.

The mix NEW represents a setting of 0111b in bits 3-0 of the Foreground Mix (BAE8H) register (FRGD_MIX). This overwrites the present bitmap color value with a new value.

The remainder of the setup is:

```
ES:[FRGD_MIX] ⇐ 0027H              ; color source is FRGD_COLOR, mix type is NEW
ES:FRGD_COLOR] ⇐ 00000002H         ; color index
ES:[PIXEL_CNTL] ⇐ A000H            ; FRGD_MIX provides color source and mix type
```

Drawing Operation:

```
                    31        15        0
ES:[ALT_CURXY] ⇐    | x1      | y1      |   ; set starting coordinate

ES:[MAJ_AXIS_PCNT] ⇐ MAX - 1       ; length in pixels of the major axis - 1
                    31        15        0
ES:[ALT_STEP] ⇐     |2*(MIN–MAX)| 2*MIN |   ; diagonal and axial step constants

If the X drawing direction is positive then
    ES:[ERR_TERM] ⇐ 2 * MIN – MAX          ; error term
else if the X drawing direction is negative
    ES[ERR_TERM] ⇐ 2 * MIN – MAX – 1       ; error term
ES:[CMD] ⇐ 00100000DDD10001b       ; Draw line command (bits 15-13, 11), draw (as opposed to
                                   ; just move current position)(bit 4), bit 0 is always 1
```

16.4.3.2 Textured Line

The line draw command can be used to draw a one pixel wide textured line from screen coordinates x1,y1 to x2,y2. The texture is created by (1) setting bits 7-6 of the Pixel Control register (BEE8H, Index AH) to A080H to specify the CPU as the source of the mask bit selecting the mix register, (2) specifying a background and foreground color, (3) setting bit 8 of the Command register (9AE8H) to 1 (wait for CPU data) and (4) setting bit 1 of the Command register to 1 (multi-pixel). When the pattern bit sent by the CPU is a 1, the Foreground Mix register specifies the color source and mix. When the bit is a 0, the Background Mix register specifies the color source and mix. This example uses the mix NEW for the foreground mix, XOR for the background mix, foreground color index 2 and background color index 4. The 32-bit line texture/pattern (PATTERN) is 00110000111100110011000011110011b. This requires that bits 10-9 of the Command register be set to 10b to specify a 32-bit bus.

Setup:

The XOR mix corresponds to a setting of 0101b in bits 3-0 of the Background Mix (B6E8H) register (BKGD_MIX). See the Solid Line example for an explanation of other parameters and registers used in this example.

```
                    31          15          0
ES:[ALT_MIX] ⇐      | 0027H     | 0005H     |   ; FRGD_COLOR is color source and NEW is mix,
                                                  ; BKGD_COLOR is color source and XOR is mix

ES:[FRGD_COLOR] ⇐ 00000002H      ; color index
ES:[BKGD_COLOR] ⇐ 00000004H      ; color index
ES:[PIXEL_CNTL] ⇐ A080H          ; mask data selecting mix register is provided by the CPU
```

Drawing Operation:

```
                    31          15          0
ES:[ALT_CURXY] ⇐    | x1        | y1        |   ; set starting coordinates

ES:[MAJ_AXIS_PCNT ⇐ MAX - 1                     ; length in pixels of the major axis - 1
                    31          15          0
ES:[ALT_STEP] ⇐     | 2*(MIN–MAX) | 2*MIN    |   ; diagonal and axial step constants

If the X drawing direction is positive then
    ES:[ERR_TERM] ⇐ 2 * MIN – MAX               ; error term
else if the X drawing direction is negative
    ES[ERR_TERM] ⇐ 2 * MIN – MAX – 1            ; error term
ES:[CMD] ⇐ 00100101DDD10011b     ; Draw line (bits 15-13, 11), 32-bit bus (bits 10-9), wait for data
                                 ; from the CPU (bit 8), draw (bit 4), multi-pixel (bit 1)

COUNT (of PATTERN dwords) = (MAX + 31)/32 (See Note)
PIX_TRANS ⇐ 00110000111100110011000011110011b   ; Output PATTERN to Pixel Data Transfer
                                                ; registers COUNT times
```

Note

The COUNT of the number of writes required by the CPU is a function of the number of bits to be transferred and the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of the Drawing Command register (9AE8H)). The number of bits transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy

bits to meet this requirement. For example, if the transfer width is 8 bits and nine bits are to be transferred for the line, two bytes must be written per line, with the upper 7 bits of the second byte padded. In general, the number of padding bits per line will vary from 0 to (n-1), where n is the transfer width in bits.

With a transfer width of 8 bits, the number of byte writes required per line can be determined from the formula n = (MAX+7)/8, with n being truncated to an integer if the result contains a fraction. Thus a MAX = 11 transfer requires (11+7)/8 = 2 1/4 = 2 bytes. The formulas for all transfer widths are given below.

8-bit transfers: COUNT = (MAX+7)/8 bytes
16-bit transfers: COUNT = (MAX+15)/16 words
32-bit transfers: COUNT = (MAX+31)/32 dwords

16.4.3.3 Rectangle Fill Solid

This command draws a solid rectangle with its top left corner at x1,y1, height = HEIGHT and width = WIDTH. The Pixel Control register (BEE8H, Index AH) must be set to A000H to select the Foreground Mix register to specify the color source and mix type. This example uses the mix NEW and color index 2. The drawing direction (bits 7-5 in the write to the CMD register below) is set to X positive, X major and Y positive (101b).

Setup:

```
ES:[FRGD_MIX] ⇐ 0027H              ; color source is FRGD_COLOR, NEW mix type
ES:[FRGD_COLOR] ⇐ 00000002H        ; color index
ES:[PIXEL_CNTL] ⇐ A000H            ; FRGD_MIX specifies the color source and mix type
```

Drawing Operation:

```
ES:[ALT_CURXY] ⇐ | x1 | y1 |       ; set starting coordinates
                 31   15   0

ES:[ALT_PCNT] ⇐ | WIDTH-1 | HEIGHT-1 |   ; rectangle width
                31        15          0

ES:[CMD] ⇐ 0100000010110001b       ; Draw rectangle (bits 15-13, 11), draw (bit 4)
```

Note

The rectangle can be defined by specifying any one of the four corners and setting bits 7-5 accordingly. Always select X as the major axis (bit 6 =0). No matter how the rectangle is defined, it always fills from left to right and top to bottom.

Corner	X direction (bit 5)	Y direction (bit 7)
top left	positive (1)	positive (1)
top right	negative (0)	positive (1)
bottom left	positive (1)	negative (0)
bottom right	negative (0)	negative (0)

16.4.3.4 Image Transfer—Through the Plane

This command transfers a rectangular image from the CPU to the display memory through the plane. "through the plane" means the complete color index is transferred for each pixel, e.g., in 8 bits/pixel mode, one byte is required to transfer one pixel to memory. The image is stored as an array of pixels arranged in row major fashion (consecutively increasing memory addresses). The Pixel Control register must be set to A000H to select the Foreground Mix register to specify the color source and mix type. The color source must be specified as the CPU. Bit 12 of the Command register must be set to 1 (swap ON) for Intel-type architectures. Bit 8 of the Command register must be set to 1 (wait for CPU data) and bits 6 and 5 must also be set to 1 to specify X as the major axis and a left-to-right drawing direction. This example uses a mix type of NEW and x1,y1 is the top left corner of the rectangle on the screen. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH. Doublword CPU writes are supported by setting bits 10-9 of the Command register to 10b.

Setup:

```
ES:[FRGD_MIX] ⇐ 0047H          ; color source is the CPU, mix type is NEW
ES:[PIXEL_CNTL] ⇐ A000H        ; FRGD_MIX is the source for color source and mix type
```

Drawing Operation:

```
                    31          15          0
ES:[ALT_CURXY] ⇐   |     x1    |     y1    |   ; set destination starting coordinates

                    31          15          0
ES:[ALT_PCNT] ⇐    | WIDTH-1   | HEIGHT-1  |   ; rectangle width

Wait for Graphics Engine not busy   ; loop till bit 9 of 9AE8H register is 0
ES:[CMD] ⇐ 01010101D0110001b        ; Draw rectangle (bits 15-13, 11), swap ON (bit 12),
                                    ; 32-bit transfers (bits 10-9), wait for CPU data (bit 8),
                                    ; always X Major (bit 6) & X Positive (bit 5), draw (bit 4)
```

COUNT (of image pixel data to transfer) = (See Note)
PIX_TRANS ⇐ IMAGEDATA; Output image data to the Pixel Data Transfer registers for COUNT dwords.

Note

The COUNT of the number of writes required by the CPU is a function of the number of pixels to be transferred, the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of the Drawing Command register (9AE8H)) and the color depth (bits/pixel). The number of pixels transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy pixels to meet this requirement. For example, at 4 bits/pixel, each byte holds two pixels. If the transfer width is one byte and three pixels are to be transferred per line, two bytes must be written per line, with the upper nibble of the second byte a dummy pixel. If the transfer width is 16 bits, from one to three dummy pixels may be required to make the number of pixels per line an even multiple of 16. The number of word writes required per line can be determined from the formula n = (W+3)/4, with n being truncated to an integer if the result contains a fraction. Thus a six pixel transfer requires (6+3)/4 = 2.25 = 2 words. This is then multiplied by the height of the image (in pixels) to determine the COUNT of words to be transferred. Similar procedures apply to every other combination of the variables affecting the COUNT. The formulas for all cases are given below, where W is the width of the image and H is the height of the image, both in pixels.

COUNT for 4 bits/pixel modes

8-bit transfers: COUNT = (W+1)/2 * H bytes
16-bit transfers: COUNT = (W+3)/4 * H words
32-bit transfers: COUNT = (W+7)/8 * H dwords

COUNT for 8 bits/pixel modes

8-bit transfers: COUNT = W * H bytes
16-bit transfers: COUNT = (W+1)/2 * H words
32-bit transfers: COUNT = (W+3)/4 * H dwords

COUNT for 16 bits/pixel modes

8-bit transfers: Do not use this combination
16-bit transfers: COUNT = W * H words
32-bit transfers: COUNT = (W+1)/2 * H dwords

COUNT for 32 bits/pixel modes

8-bit transfers: COUNT = Do not use this combination
16-bit transfers: COUNT = 2W * H words
32-bit transfers: COUNT = W * H dwords

Note that in 32 bits/pixel modes, the upper byte is a dummy byte providing padding for a 24-bit pixel.

16.4.3.5 Image Transfer—Across the Plane

The image transfer command can also be used to transfer a rectangular image from the CPU to the display memory across the plane. "across the plane" means that each bit sent by the CPU is stored in display memory as a single pixel. These pixels are arranged in row major fashion (consecutively increasing memory addresses). An "across the plane" transfer is created by (1) setting bits 7-6 of the Pixel Control register (BEE8H, Index AH) to A080H to specify the CPU as the source of the mask bit selecting the mix register, (2) specifying a background and foreground color, (3) setting bit 8 of the Command register (9AE8H) to 1 (wait for CPU data) and (4) setting bit 1 of the Command register to 1 (multi-pixel). When the pattern bit sent by the CPU is a 1, the Foreground Mix register specifies the color source and mix. When the bit is a 0, the Background Mix register specifies the color source and mix. This example uses a mix type of NEW, and x1,y1 is the top left corner of the rectangle on the screen. The height and width of the rectangle (in pixels) are HEIGHT and WIDTH. The monochrome image is translated so that pixels corresponding to a 1 in the bit image are given color index 4 and pixels corresponding to a 0 in the bit image are given color index 0. This example uses word transfers from the CPU as specified by setting bits 10-9 of the Command register to 01b for a 16-bit bus width.

Setup:

```
                    31          15          0
ES:[ALT_MIX] ⇐      | 0027H     | 0005H     |     ; FRGD_COLOR color source and mix is NEW
                                                  ; BKGD_COLOR is color source and mix is XOR
ES:[FRGD_COLOR] ⇐ 00000004H      ; foreground color index 4
ES:[BKGD_COLOR] ⇐ 00000000H      ; background color index 0
ES:[PIXEL_CNTL] ⇐ A080H          ; selection of mix register is based on data from the CPU
```

Drawing Operation:

```
                    31          15          0
ES:[ALT_CURXY] ⇐    | x1        | y1        |     ; set destination starting coordinates

                    31          15          0
ES:[ALT_PCNT] ⇐     | WIDTH-1   | HEIGHT-1  |     ; rectangle width

Wait for Graphics Engine not busy   ; loop till bit 9 of 9AE8H register is 0
CMD ⇐ 01010011D0110011b             ; Draw rectangle (bits 15-13, 11), swap ON (bit 12),
                                    ; 16-bit transfers (bits 10-9), wait for CPU data (bit 8),
                                    ; always X Major (bit 6) & X Positive (bit 5), draw (bit 4),
                                    ; multi-pixel (bit 1)
```

COUNT (of image pixel data to transfer) = ((WIDTH +15)/16)*HEIGHT words
PIX_TRANS ⇐ IMAGEDATA; Output image data to Pixel Transfer register for COUNT words

Notes

The COUNT of the number of writes required by the CPU is a function of the number of pixels to be transferred and the width of the transfer (8, 16 or 32 bits as specified by bits 10-9 of 9AE8H). Except for the case where bits 10-9 of 9AE8H are 11b, the number of pixels transferred per line must be an even multiple of the transfer width. If this is not the case, the last write per line must be padded with one or more dummy pixels to meet this requirement. For example, if the transfer width is 8 bits and nine pixels are to be transferred per line, two bytes must be written per line, with the upper 7 bits of the second byte padded. In general, the number of padding bits per line will vary from 0 to (n-1), where n is the transfer width in bits.

With a transfer width of 8 bits, the number of byte writes required per line can be determined from the formula n = (W+7)/8, with n being truncated to an integer if the result contains a fraction. Thus a 13-bit pixel transfer requires (13+7)/8 = 2.5 = 2 bytes. This is then multiplied by the height of the image (in pixels) to determine the COUNT of bytes to be transferred. Similar procedures apply to every other combination of the variables affecting the COUNT. The formulas for all cases are given below, where W is the width of the image and H is the height of the image, both in pixels.

8-bit transfers: COUNT = (W+7)/8 * H bytes (9AE8H_10-9 = 00b)
16-bit transfers: COUNT = (W+15)/16 * H words (9AE8H_10-9 = 01b)
32-bit transfers: COUNT = (W+31)/32 * H dwords (9AE8H_10-9 = 10b)
New 32-bit transfers: COUNT = (((W+7)/8*H)+3)/4 dwords (9AE8H_10-9 = 11b) (Trio32 only)

The differences between the two 32-bit transfer options are:

1. For 9AE8H_10-9 set to 10b, every line of the transfer must start with a fresh doubleword. In other words, all unneeded bits in a doubleword transfer for a given line are discarded. After a rectangular image is transferred, the current drawing position is a the bottom left, meaning the next rectangle, if drawn, will be below the previous rectangle.
2. For 9AE8H_10-9 set to 11b, only bits from the end of the line width to the next byte boundary are discarded. Data for the next line begins with the next byte. After a rectangular image is transferred, the current drawing position is a the top right, meaning the next rectangle, if drawn, will be to the right of the previous rectangle.

To write to a single plane, set the foreground mix to 'logical one' (0002H), the background mix to 'logical zero' (0001H), and the Write Mask register (AAE8H) to select the desired (single) plane for updates.

16.4.3.6 BitBLT—Through the Plane

This command copies a source rectangular area in display memory to another location in display memory. The Pixel Control register must be set to A000H to select the Foreground Mix register to specify the color source and mix type. The color source must be specified as the bitmap (display memory). Bit 6 of the Command register must be set to 1 to specify X as the major axis. For this example, assume x1,y1 is the top left corner of the source rectangle in display memory and x2,y2 is the top left corner of the destination rectangle. The rectangles can be overlapping or disjoint. The height and width (in pixels) of the rectangle being copied are HEIGHT and WIDTH.

Setup:

First, the values of the Srcx, Srcy, Destx and Desty must be determined.

Case 1: Source and destination rectangles do not overlap

For X Positive, Y Positive: Srcx = x1, Srcy = y1, Destx = x2, Desty = y2

Case 2: Source and destination rectangles overlap

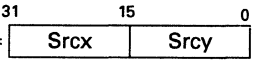
```
If x1 > x2
    then if X Positive, Srcx = x1, Destx = x2
else
    Srcx = x1 + WIDTH –1, Destx = x2 + WIDTH –1          ; X Negative

If y1 > y2
    then if Y Positive, Srcy = y1, Desty = y2
else
    Srcy = y1 + HEIGHT –1, Desty = y2 + HEIGHT –1        ; Y Negative

ES:[PIXEL_CNTL] ⇐ A000H          ; FRGD_MIX is the source of color source and mix type
ES:[FRGD_MIX] ⇐ 0067H            ; color source is display memory and mix type is NEW
```

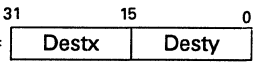
Draw Operation:

ES:[ALT_CURXY] ⇐



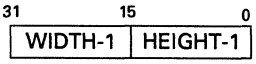
; set starting coordinates

ES:[ALT_STEP] ⇐



; set destination coordinates

ES:[ALT_PCNT] ⇐



; rectangle width and height

```
ES:[CMD] ⇐ 11000000D0D10001b     ; BitBLT (bits 15-13, 11), always X Major (bit 6) , draw (bit 4)
```

16.4.3.7 BitBLT—Across the Plane

This uses the same command as a BitBLT through the plane. However, instead of copying complete pixels (with color affected only by the mix), this 'across the plane" transfer uses only the bits in the color planes specified by setting the Read Mask register (AEE8H), e.g., bit 3 of every pixel, to determine the destination rectangle. With more than one plane enabled for read, if all the bits in the planes enabled for read are '1's then a '1' is read. If a bit in any one of the planes enabled for read is a '0', then '0' is read. An "across the plane" transfer is created by (1) setting bits 7-6 of the Pixel Control register (BEE8H, Index AH) to A0C0H to specify the bitmap as the source of the mask bit selecting the mix register, (2) programming the Read and Write Mask registers to specify the plane to read from and write to and (3) setting bit 1 of the Command register to 1 (multi-pixel). In this example, when the bit read is a 1, a 1 is copied as specified by the foreground mix. When the bit read is a 0, a 0 is copied as specified by the background mix. Assume x1,y1 is the top left corner of the source rectangle on the display, and x2,y2 is the top left corner of the destination rectangle. The image is read from plane 0 and written to plane 2. The rectangles could be overlapping or disjoint. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

First, the values of the Srcx, Srcy, Destx and Desty must be determined.

Case 1: Source and destination rectangles do not overlap

For X Positive, Y Positive: Srcx = x1, Srcy = y1, Destx = x2, Desty = y2

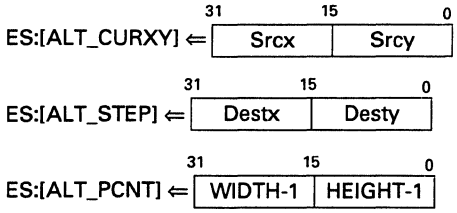
Case 2: Source and destination rectangles overlap

```
If x1 > x2
    then if X Positive, Srcx = x1, Destx = x2
else
    Srcx = x1 + WIDTH –1, Destx = x2 + WIDTH –1          ; X Negative

If y1 > y2
    then if Y Positive, Srcy = y1, Desty = y2
else
    Srcy = y1 + HEIGHT –1, Desty = y2 + HEIGHT –1        ; Y Negative

ES:[PIXEL_CNTL] ⇐ A0C0H          ; data from display memory selects mix register
                  31      15    0
ES:[ALT_MIX] ⇐   | 0002H | 0001H |   ; result of foreground mix is always logical 1,
                                     ; result of background mix is always logical 0
ES:[RD_MASK] ⇐ 00000001H         ; read from plane 0
ES:[WRT_MASK] ⇐ 00000004H        ; plane 2 enabled for write
```

Draw Operation:




```
ES:[CMD] ⇐ 11000000D0D10001b    ; BitBLT (bits 15-13, 11), always X Major (bit 6) , draw (bit 4),
                                ; multi-pixel (bit 1)
```

Note

It is possible to translate a monochrome image, e.g., text fonts, stored in a single plane in display memory into a 2-color image. This is accomplished by setting the mix registers differently and setting the desired background and foreground colors. If the source bit is a '1', then the corresponding pixel at the destination is colored with the foreground color index. The destination pixel is colored with the background color index if the corresponding source bit is a '0'. The setup for this is as follows:

```
ES:[WRT_MASK] ⇐ FFFFFFFFH       ; enable all planes for writing
ES:[FRGD_MIX] ⇐ 0027H           ; color source foreground, mix type NEW
ES:[BKGD_MIX] ⇐ 0007H           ; color source background, mix type NEW
ES:[FRGD_COLOR] ⇐ 00000004H     ; foreground color
ES:[BKGD_COLOR] ⇐ 00000001H     ; background color
```

16.4.3.8 PatBLT—Pattern Fill Through the Plane

An 8x8 pixel pattern is initially copied into an off-screen area of display memory using an image transfer operation or a direct write (linear addressing). This command then repeatedly tiles this source pattern into a destination rectangle of arbitrary size. The colors of the destination pixels are affected only by the mix selected. The destination rectangle must not overlap the source pattern. Each copy is aligned to an 8-pixel boundary (x coordinate = 0, 8, etc.), with pixels outside the destination rectangle boundary not being drawn. The Pixel Control register must be set to A000H to select the Foreground Mix register to specify the color source and mix type. The color source must be specified as the bitmap (display memory). Bit 6 of the Command register must be set to 1 to specify X as the major axis. In this example, assume x1,y1 is the top left corner of the pixel pattern and x2,y2 is the top left corner of the destination rectangle. The height and width (in pixels) of the rectangle are HEIGHT and WIDTH.

Setup:

```
ES:[PIXEL_CNTL] ⇐ A000H          ; FRGD_MIX is the source of color source and mix type
ES:[FRGD_MIX] ⇐ 0067H            ; color source is display memory, mix type is NEW
```

Draw Operation

```
                    31          15          0
ES:[ALT_CURXY] ⇐   |    x1     |    y1     |   ; set starting coordinates

                    31          15          0
ES:[ALT_STEP] ⇐    |    x2     |    y2     |   ; set destination coordinates

                    31          15          0
ES:[ALT_PCNT] ⇐    | WIDTH-1   | HEIGHT-1  |   ; rectangle width and height
```

```
ES:[CMD] ⇐ 11100000D0D10001b     ; PatBLT (bits 15-13,11), always X Major (bit 6) , draw (bit 4)
```

16.4.3.9 PatBLT—Pattern Fill Across the Plane

This uses the same command as a PatBLT through the plane. However, instead of copying complete pixels (with color affected only by the mix), this 'across the plane" transfer uses only the bits in the color planes specified by setting the Read Mask register (AEE8H), e.g., bit 3 of every pixel, to determine the destination rectangle. With more than one plane enabled for read, if all the bits in the planes enabled for read are '1's then a '1' is read. If a bit in any one of the planes enabled for read is a '0', then '0' is read. An "across the plane" transfer is created by (1) setting bits 7-6 of the Pixel Control register (BEE8H, Index AH) to A0C0H to specify the bitmap as the source of the mask bit selecting the mix register, (2) programming the Read and Write Mask registers to specify the plane to read from and write to and (3) setting bit 1 of the Command register to 1 (multi-pixel). In this example, when the bit read is a 1, a 1 is copied as specified by the foreground mix. When the bit read is a 0, a 0 is copied as specified by the background mix. In this example, assume x1,y1 is the top left corner of the pixel pattern and x2,y2 is the top left corner of the destination rectangle. The image is read from plane 0 and written to plane 2. The height and width of the destination rectangle are HEIGHT and WIDTH.

Setup:

```
ES:[PIXEL_CNTL] ⇐ A0C0H          ; data from display memory selects mix register
                  31      15     0
ES:[ALT_MIX] ⇐   | 0002H | 0001H |   ; result of foreground mix is always logical 1,
                                      ; result of background mix is always logical 0
ES:[RD_MASK] ⇐ 00000001H         ; read from plane 0
ES:[WRT_MASK] ⇐ 00000004H        ; plane 2 enabled for write
```

Draw Operation:

```
                  31      15     0
ES:[ALT_CURXY] ⇐ |  x1   |  y1   |   ; set starting coordinates

                  31      15     0
ES:[ALT_STEP] ⇐  |  x2   |  y2   |   ; set destination coordinates

                  31      15     0
ES:[ALT_PCNT] ⇐  | WIDTH-1 | HEIGHT-1 |   ; rectangle width and height
```

```
ES:[CMD] ⇐ 11100000D0D10011b     ; PatBLT (bits 15-13, 11), always X Major (bit 6) , draw (bit 4),
                                  ; multi-pixel (bit 1)
```

Note

To expand the source mono pattern into a 2-color pattern, set the foreground mix to 27H, the background mix to 7H and the foreground and background colors as desired. Also set the write mask (AAE8H) to FFFFFFFFH. This needs to be set only once. It is altered only by another write.

16.4.3.10 Short Stroke Vectors

This command rapidly draws short lines (up to 15 pixels in length). Such lines are constrained to one of the 8 directions at 45 degree increments starting at 0 degrees. The current point x1,y1 is set and a NOP command is issued to set all the desired drawing parameters without actually writing a pixel. For example, bit 2 (Last Pixel Off) would be set to 1 (OFF) for drawing connected lines until the last line is drawn. The short stroke vector parameters are then loaded in the Short Stroke Vector Transfer (9EE8H) register (SHORT_STROKE). Two vectors can be defined at a time, one in the low byte and one in the high byte. For the low byte, bits [7:5] define the direction, with bit 4 set to '1' for a draw operation or to '0' for a move current position operation. Bits 3-0 define the length of the short line. Let SSVD0, SSVD1, ...SSVDN–1 bytes be the short stroke vector data for N lines.

Setup:

```
ES:[PIXEL_CNTL] ⇐ A000H          ; FRGD_MIX is the source of color source and mix type
ES:[FRGD_MIX] ⇐ 0027H            ; use the foreground color, mix type NEW
ES:[FRGD_COLOR]⇐ 00000004H       ; foreground color index 4
```

Draw Operation:

```
                                 31          15          0
ES:[ALT_CURXY] ⇐                 | x1        | y1        |   ; set starting coordinates
```

```
ES:[CMD] ⇐ 00010010XXX11111b     ; NOP (bits 15-13, 11), byte swap (bit 12), 16-bit transfers
                                 ; (bits 10-9) , draw (bit 4), radial drawing direction (bit 3),
                                 ; last pixel off (bit 2), multi-pixel (bit 1)
```

While space available in the FIFO

```
ES:[SHORT_STROKE] ⇐ SSVD1 SHL 8 + SSVD0 ; SSVD1 shifted to high byte, SSVD0 in low byte
ES:[SHORT_STROKE] ⇐ SSVD3 SHL 8 + SSVD2 ; byte swap turned on to read vectors out in
                                        ; correct order
            .
            .
            .
ES:[SHORT_STROKE] ⇐ SSVDN-1 SHL 8 + SSVDN-2
```

16.4.3.11 Programmable Hardware Cursor

A programmable cursor is supported which is compatible with the Microsoft Windows (bit 4 of CR55 = 0) and X11 (bit 4 of CR55 = 1) cursor definitions. The cursor size is 64 pixels wide by 64 pixels high, with the cursor pattern stored in an off-screen area of display memory. Two monochrome images 64 bits wide by 64 bits high (512 bytes per image) define the cursor shape. The first bit image is an AND mask and the second bit image is an XOR mask. The following is the truth table for the cursor display logic.

AND Bit	XOR Bit	Displayed (Microsoft Windows)	Displayed (X11)
0	0	Cursor Background Color	Current Screen Pixel
0	1	Cursor Foreground Color	Current Screen Pixel
1	0	Current Screen Pixel	Cursor Background Color
1	1	NOT Current Screen Pixel	Cursor Foreground Color

The hardware cursor color is taken from the Hardware Graphics Cursor Foreground Stack (CR4A) and the Hardware Graphics Cursor Background Stack (CR4B) registers. Each of these is a stack of three 8-bit registers. The stack pointers are reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). The color value is then programmed by consecutive writes (low byte, second byte, third byte) to the appropriate (foreground or background) register.

Enabling/Disabling the Cursor

The hardware cursor is disabled when a VGA-compatible mode is in use. It can be enabled or disabled when in Enhanced mode (bit 0 of 4AE8H = 1), as follows.

```
CR39 ⇐ A0H                    ; Unlock System Control registers
CR45_0 ⇐ 1                    ; Enable hardware cursor
CR45_0 ⇐ 0                    ; Disable hardware cursor
CR39 ⇐ 00H                    ; Lock System Control registers
```

Positioning the Cursor

The cursor can be positioned at any point on the display, with the X,Y coordinates ranging from 0 to 2047. This enables the full cursor images to be displayed on the screen and partial cursor images to be displayed at the right edge and the bottom edge of the screen. The cursor offset OX,OY has to be set to 0,0 for a 1024x768 resolution. If X is > (1024 – 64) or Y is > (768 – 64), then a partial cursor is visible at the right edge or top edge of the screen respectively. Note that if Y ≥ 768 then the cursor is not visible; it is residing in the off-screen area.

A partial cursor image can be displayed at the left edge or the top edge of the screen. To enable partial cursor display at the top edge of the screen, Y is set to 0 and the Y offset register is set to OY (range from 0 to 63). This displays the bottom 64–OY rows of the cursor image at the currently set X position and the top edge of the screen. Similarly, a partial cursor can be displayed at the left edge of the screen by setting X to 0 and the X offset register to OX (range from 0 to 63). This displays the right 64–OX columns of the cursor image at the currently set X and the left edge of the screen. The following pseudocode illustrates cursor positioning.

```
CR39 ⇐ A0H                              ; Unlock System Control registers
CR46_10-8 ⇐ MS 3 bits of X cursor position
CR47_7-0 ⇐ LS 8 bits of X cursor position
```

CR49_7-0 ⇐ LS 8 bits of Y cursor position
CR4E_5-0 ⇐ Cursor Offset X position
CR4F_5-0 ⇐ Cursor Offset Y position
CR48_10-8 ⇐ MS 3 bits of Y cursor position
CR39 ⇐ 00H ; Lock System Control registers

The cursor position is updated by the hardware once each frame. Therefore, the programmer should ensure that the position is re-programmed no more than once for each vertical sync period.

Programming the Cursor Shape

The AND and the XOR cursor image bitmaps are 512 bytes each. These bitmaps are word interleaved in a contiguous area of display memory, i.e., AND word 0, XOR word 0, AND word 1, XOR word 1 ... AND word 255, XOR word 255. The starting location must be on a 1024-byte boundary. This location is programmed into the Hardware Graphics Cursor Start Address registers (CR4C and CR4D) as follows:

CR39 ⇐ A0H ; Unlock System Control registers
CR4C_11-8 ⇐ MS 4 bits of the cursor storage start 1024-byte segment.
CR4D ⇐ LS 8 bits of the cursor storage start 1024-byte segment
CR39 ⇐ 0 ; Lock System Control registers

The value programmed is the 1024-byte segment of display memory at which the beginning of the hardware cursor bit pattern is located. For example, for an 800x600x8 mode on a 1 MByte system, there are 1024 1K segments. Programming CR4C_11-8 with 3H and CR4D with FEH specifies the starting location as the 1022nd (0-based) 1K segment. The cursor pattern is programmed (using linear addressing) at FF800H offset from the base address of the frame buffer.

Cursor Destination

If in dual image mode, select the cursor controller source. SR31_7 = 0 selects controller 1; SR31_7 = 1 selects controller 2. This determines on which screen the cursor will appear.

Note

If the cursor is not 64 bits by 64 bits, the given images should be padded to make the cursor image 64 bits by 64 bits. The padded area should be made transparent by padding the extra AND mask bits with '1's and the extra XOR bits by '0's.

16.4.3.12 Programmable Hardware Icon

86CM65 provides a programmable hardware icon that is displayable in all modes, including VGA text and graphics modes. Only the hardware cursor (available only in Enhanced modes) has precedence over the hardware icon for overlaying on the text/graphics/video.

The setup for using a hardware icon involves two steps.

1. Up to 8 icons are defined in contiguous memory at a frame buffer base address location defined by SR4E. Each icon is defined in memory as 64 consecutive lines of pixels with 64 pixels per line and 2 bits/pixel, thus requiring 1 KByte of memory per icon. The two bits per pixel are stored in memory in the same manner as the AND and XOR masks for the hardware cursor. That is, one word of bit 1 is stored, then one word of bit 2, a second word of bit 1, a second word of bit 2, etc. Corresponding bit 1's and bit 2's are used to select the icon pixel colors.
2. Four icon colors are programmed in SR49. This address contains a stack of of twelve 8-bit registers that can be written sequentially with automatic address indexing. This allows rapid specification of four 24-bit colors (Color0 to Color3). For color depths less than 24 bits, the appropriate number of bits are taken from the lsb's of the registers, e.g., the low order 8 bits are used for 8 bits/pixel modes.

To use an icon, do the following:

1. Enable the hardware icon by setting SR48_0 to 1.
2. Select one of eight icon maps via SR48_6-4.
3. Specify the color of each pixel. The programmer first selects a color mode via SR48_1 as follows:
   0 = 4 opaque colors
   1 = 3 opaque colors and 1 transparent color

   When this bit is cleared to 0, the two bits programmed for each pixel in the icon memory are interpreted as follows:
   00 = Color0
   01 = Color1
   10 = Color2
   11 = Color3

   When this bit is set to 1, the two bits programmed for each pixel in the icon memory are interpreted as follows:
   00 = Color0
   01 = Color1
   10 = Color2
   11 = Transparent (the current frame buffer pixel is not overwritten)
4. Specify the final size of the icon. If SR48_2 = 0, the horizontal size is 64 pixels. If SR48_2 = 1, the horizontal size is 128 pixels. If SR48_3 = 0, the vertical size is 64 pixels. If SR48_3 = 1, the vertical size is 128 pixels. In both case, the expansion is done by pixel doubling.
5. If in dual image mode, select the icon controller source. SR31_6 = 0 selects controller 1; SR31_6 = 1 selects controller 2. This determines on which screen the image will appear.
6. Program the icon location on the screen. The horizontal coordinate of the upper left hand edge of the icon is programmed in SR4A and SR4B. the vertical coordinate of the upper left hand edge of the icon is specified in SR4C and SR4D.

16.5 RECOMMENDED READING

Graphics Programming for the 8514/A by Jake Richter and Bud Smith (M&T Publishing, Inc) provides extensive explanations and examples for programming most of the bits in the S3 Enhanced Registers. This book may be out of print.

Programmer's Guide to the EGA, VGA and Super VGA Cards, 3rd Edition by Richard F. Ferraro (Addison-Wesley Publishing Company, Inc) includes a section on programming for S3 accelerator chips.

Section 17: Standard VGA Register Descriptions

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). A question mark in an address stands for a hexadecimal value of either 'B' or 'D'. If bit 0 of the Miscellaneous Output Register (3C2H, Write) is set to 1, the address is based at 3DxH for color emulation. If this bit is reset to 0, the address is based at 3BxH for monochrome emulation. If a register or bit is noted as paired, there are two identical registers or bit at that address, with access controlled via SR26. One register or bit is used by controller 1 and the other for controller 2. If a register or bit is noted as shared, there is a single register or bit shared by controller 1 or controller 2.

See Appendix A for a table listing each register in this section and its page number.

17.1 GENERAL REGISTERS

This section describes general input status and output control registers.

Miscellaneous Output Register (MISC)

Write Only — Address: 3C2H
Read Only — Address: 3CCH
Power-On Default: 00H

This register controls miscellaneous output signals. A hardware reset sets all bits to zero.

7	6	5	4	3	2	1	0
SYNPOL/ VERT SIZE		PGSL	= 0	CLK 1	SEL 0	ENB RAM	IOA SEL

Bit 0 IOA SEL - I/O Address Select
0 = Monochrome emulation. Address based at 3Bx
1 = Color emulation. Address based at 3Dx

Bit 1 ENB RAM - Enable CPU Display Memory Access
0 = Disable access of the display memory from the CPU
1 = Enable access of the display memory from the CPU

Bits 3–2 Clock Select - Select the Video Clock Frequency
00 = Selects the DCLK PLL parameters in SR22 and SR23. The default generates a 25.175 MHz DCLK for 640 horizontal pixels
01 = Selects the DCLK PLL parameters in SR24 and SR25. The default generates a 28.322 MHz DCLK for 720 horizontal pixels
10 = Reserved
11 = Selects the DCLK PLL parameters in SR12 and SR13. This setting is used for all Enhanced modes.

The selected DCLK PLL parameter values are loaded into the PLL when bit 1 of SR15_1 is set to 1 or when SR15_5 is programmed to 1 and then 0.

Bit 4 Reserved = 0

Bit 5 PGSL -Select High 64K Page
0 = Select the low 64K page of memory
1 = Select the high 64K page of memory

Bits 7-6 SYNCPOL/VERT SIZE - Sync Polarity/Vertical Size

Bit 7	Bit 6	VSYNC Polarity	HSYNC Polarity	Vertical Size (lines)
0	0	+	+	Reserved
0	1	+	-	200 (double scanned)
1	0	-	+	350
1	1	-	-	480

+ = positive sync pulse
- = negative sync pulse

Vertical Size = vertical resolution of the graphics source

This vertical size is used when CR70_1 is set to 1 to enable graphics mode vertical expansion. During simultaneous display, SR32_2-1 control the polarity of the the VSYNC and HSYNC signals.

Feature Control Register (FCR_WT, FCR_AD)

Write Only Address: 3?AH
Read Only Address: 3CAH
Power-On Default: 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	VSSL	= 0	= 0	= 0

Bits 2–0 Reserved = 0

Bit 3 VSSL - Vertical Sync Type Select
0 = Enable normal vertical sync output to the monitor
1 = The 'vertical sync' output is the logical OR of 'vertical sync' and 'vertical active display enable' (an internal signal)

Bits 7–4 Reserved = 0

Input Status 0 Register (STATUS_0)

Read Only Address: 3C2H
Power-On Default: Undefined

This register indicates the status of the VGA adapter.

7	6	5	4	3	2	1	0
CRT INTPE	= 0	= 0	MON SENS	= 0	= 0	= 0	= 0

Bits 3–0 Reserved = 0

Bit 4 MON SENS - Monitor Sense Status
0 = The internal $\overline{\text{SENSE}}$ signal is a logical 0
1 = The internal $\overline{\text{SENSE}}$ signal is a logical 1

Bits 6–5 Reserved = 0

Bits 7 CRT INTPE - CRT Interrupt Status
0 = Vertical retrace interrupt cleared
1 = Vertical retrace interrupt pending

See Section 13.5 for an explanation of interrupt generation.

Input Status 1 Register (STATUS_1)

Read Only Address: 3?AH
Power-On Default: Undefined

This register indicates video sync timing and video wraparound.

7	6	5	4	3	2	1	0
		TST-VDT					
= 0	= 0	1	0	VSY	= 1	R	DTM

Bit 0 $\overline{\text{DTM}}$ - Display Mode Inactive
0 = The display is in the display mode.
1 = The display is not in the display mode. Either the horizontal or vertical retrace period is active

Bit 1 Reserved = 0

Bit 2 Reserved = 1

Bit 3 VSY - Vertical Sync Active
0 = Display is in the display mode
1 = Display is in the vertical retrace mode

Bits 5–4 TST-VDT - Video Signal Test
Video Data Feedback 1,0. These bits are feedback video signals to do read back tests. These bits are selectively connected to two of the eight color outputs of the attribute controller. Bits 5 and 4 of the color plane enable register (AR12) control the multiplexer for this video output observation.

Bits 7–6 Reserved = 0

Video Subsystem Enable Register

Write Only Address: 3C3H
Power-On Default: 00H

7	6	5	4	3	2	1	0
							CHIP
R	R	R	R	R	R	R	ENB

Bit 0 CHIP ENB - Chip Enable
0 = 86CM65 disabled
1 = 86CM65 enabled

Bits 7–1 Reserved

17.2 SEQUENCER REGISTERS

The sequencer registers are located at two-byte address spaces. These registers are accessed by first writing the data to the index register of the sequencer at I/O address 3C4H and then writing to or reading from the data register at 3C5H. A word write of both address and data at 3C4H can also be performed.

Sequencer Index Register (SEQX)

Read/Write Address: 3C4H
Power-On Default: Undefined

This register is loaded with a binary value that indexes the sequencer register for read/write data. This value is referred to as the "Index Number" of the SR register in this document.

7	6	5	4	3	2	1	0
R	R	R	SEQ ADDRESS				

Bits 4–0 SEQ ADDRESS - Sequencer Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–5 Reserved

Sequencer Data Register (SEQ_DATA)

Read/Write Address: 3C5H
Power-On Default: Undefined

This register is the data port for the sequencer register indexed by the Sequencer Index register (3C4H).

7	6	5	4	3	2	1	0
SEQ DATA							

Bit 7–0 SEQ DATA - Sequencer Register Data
Data to the sequencer register indexed by the sequencer address index.

Reset Register (RST_SYNC) (SR0)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 00H

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	SYN RST	ASY RST

Bit 0 $\overline{\text{ASY}}$ RST - Asynchronous Reset

This bit is for VGA software compatibility only. It has no function for 86CM65.

Bit 1 $\overline{\text{SYN}}$ RST - Synchronous Reset

This bit is for VGA software compatibility only. It has no function for 86CM65.

Bits 7–2 Reserved = 0

Clocking Mode Register (CLK_MODE) (SR1)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 01H

This register controls the operation mode of dot clock and character clock.

7	6	5	4	3	2	1	0
= 0	= 0	SCRN OFF	SHF 4	CCLK 1/2	SHF LD	= 0	8DC

Bit 0 8DC - 8 Dot Clock Select
0 = Character clocks 9 dots wide are generated
1 = Character clocks 8 dots wide are generated

Bit 1 Reserved = 0

Bit 2 SHF LD - Load Serializers Every Second Character Clock
0 = Load the video serializer every character clock
1 = Load the video serializers every other character clock

Bit 3 CCLK 1/2 - Internal Character Clock Divided by 2
0 = Internal character clock unchanged
1 = Halve the frequency of the character clock

This bit is used for horizontal pixel doubling.

Bit 4 SHF 4 - Load Serializers Every Fourth Character Clock
0 = Load the serializers every character clock cycle
1 = Load the serializers every fourth character clock cycle

Bit 5 SCRN OFF - Screen Off
0 = Screen is turned on.
1 = Screen is turned off

This bit is effective only when CR71_1 = 0.

Note: This bit is shared.

Bits 7–6 Reserved = 0

Enable Write Plane Register (EN_WT_PL) (SR2)

Read/Write Address: 3C5H, Index 02H
Power-On Default: 00H

This register selects write protection or write permission for CPU write access into video memory.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	EN.WT.PL.			

Bits 3–0 EN.WT.PL - Enable Write to a Plane
0 = Disables writing into the corresponding plane
1 = Enables the CPU to write to the corresponding color plane

Bits 7–4 Reserved = 0

Character Font Select Register (CH_FONT_SL) (SR3)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 03H
Shared

7	6	5	4	3	2	1	0
= 0	= 0	SLA 2	SLB 2	SLA 1	0	SLB 1	0

In text modes, bit 3 of the attribute byte normally turns the foreground intensity on or off. This bit can be redefined to be a switch between two character sets. The switch is enabled when there is a difference between the value of character font select A and character font select B bits. Memory Mode (SR4) register bit 1 = 1 (extended memory) enables all bits of this function; otherwise character fonts 0 and 4 are available. 256 KBytes of video memory support 8 character sets. This register is reset to 0 asynchronously during a system reset.

Bits 4, 1–0 SLB - Select Font B
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of the attribute byte is a logical 1, according to the following table:

Bits 4,1,0	Font Table Location	Bits 4, 1,0	Font Table Location
000	First 8K of plane 2	100	Second 8K of plane 2
001	Third 8K of plane 2	101	Fourth 8K of plane 2
010	Fifth 8K of plane 2	110	Sixth 8K of plane 2
011	Seventh 8K of plane 2	111	Eighth 8K of plane 2

Bits 5, 3–2 SLA - Select Font A
This value selects the portion of plane 2 used to generate text character fonts when bit 3 of attribute byte is a logical 0, according to the same table as the character font select A.

Bits 7–6 Reserved = 0

Memory Mode Control Register (MEM_MODE) (SR4)

Read/Write Address: 3C5H, Index 04H
Power-On Default: 00H

This register controls CPU memory addressing mode.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	CHN 4M	SEQ MODE	EXT MEM	= 0

Bit 0 Reserved = 0

Bit 1 EXT MEM - Extended Memory Access
0 = Memory access restricted to 16/32 KBytes
1 = Allows complete memory access to 256 KBytes. Required for VGA

Note: This bit is shared.

Bit 2 SEQ MODE - Sequential Addressing Mode
This bit affects only CPU write data accesses into video memory. Bit 3 of this register must be 0 for this bit to be effective.
0 = Enables the odd/even addressing mode. Even addresses access planes 0 and 2. Odd addresses access planes 1 and 3
1 = Directs the system to use a sequential addressing mode

Bit 3 CHN 4M - Select Chain 4 Mode
0 = Enables odd/even mode.
1 = Chain 4 Mode. This bit selects modulo 4 addressing for CPU access to display memory. A logical 1 directs the two lower order bits of the CPU address used to select the plane in video memory to be accessed as follows:

A1	A0	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

Note: This bit is shared.

Bits 7–4 Reserved = 0

17.3 CRT CONTROLLER REGISTERS

The CRT controller registers are located at two locations in I/O address space. These registers are accessed by first writing to the index register of the CRT controller and then accessing the data register. The index register is located at I/O address 3?4H and the CRT Controller Data register is at 3?5H. Which address is used (3BX or 3DX) depends on bit 0 of the Miscellaneous Output register at 3C2H. A word write of both address and data at 3?4H can also be performed.

CRT Controller Index Register (CRTC_ADR) (CRX)

Read/Write Address: 3?4H
Power-On Default: 00H

This register is loaded with a binary value that indexes the CRT controller register where data is to be accessed. This value is referred to as the "Index Number" of the CR register (CR00–18). This register is also used as an index to the S3 VGA registers, the System Control Registers and the System Extension registers.

7	6	5	4	3	2	1	0
CRTC ADDRESS							

Bits 7–0 CRTC ADDRESS - CRTC Register Index
A binary value indexing the register where data is to be accessed.

CRT Controller Data Register (CRTC_DATA) (CRT)

Read/Write Address: 3?5H
Power-On Default: Undefined

This register is the data port for the CRT controller register indexed by the CRT Controller Address register.

7	6	5	4	3	2	1	0
CRTC DATA							

Bits 7–0 CRTC DATA - CRTC Register Data
Data to the CRT controller register indexed by the CRT controller address index.

Horizontal Total Register (H_TOTAL) (CR0)

Read/Write Address: 3?5H, Index 00H
Power-On Default: Undefined Paired

This register defines the number of character clocks from HSYNC going active to the next HSYNC going active. In other words, it is the total time required for both the displayed and non-displayed portions of a single scan line. Bit 8 of this value is bit 0 of CR5D.

7	6	5	4	3	2	1	0
HORIZONTAL TOTAL							

Bits 7–0 HORIZONTAL TOTAL.
9-bit Value = (number of character clocks in one scan line) - 5. This register contains the least significant 8 bits of this value.

Horizontal Display End Register (H_D_END) (CR1)

Read/Write Address: 3?5H, Index 01H
Power-On Default: Undefined Paired

This register defines the number of character clocks for one line of the active display. Bit 8 of this value is bit 1 of CR5D.

7	6	5	4	3	2	1	0
HORIZONTAL DISPLAY END							

Bits 7–0 HORIZONTAL DISPLAY END
9-bit Value = (number of character clocks of active display) - 1. This register contains the least significant 8 bits of this value.

Start Horizontal Blank Register (S_H_BLNK) (CR2)

Read/Write Address: 3?5H, Index 02H
Power-On Default: Undefined Paired

This register specifies the value of the character clock counter at which the $\overline{\text{BLANK}}$ signal is asserted. Bit 8 of this value is bit 2 of CR5D.

7	6	5	4	3	2	1	0
START HORIZONTAL BLANK							

Bits 7–0 START HORIZONTAL BLANK
9-bit Value = character clock value at which horizontal blanking begins. This register contains the least significant 8 bits of this value.

End Horizontal Blank Register (E_H_BLNK) (CR3)

Read/Write Address: 3?5H, Index 03H
Power-On Default: Undefined Paired

This register determines the pulse width of the $\overline{\text{BLANK}}$ signal and the display enable skew.

7	6	5	4	3	2	1	0
R	DSP-SKW 1	DSP-SKW 0	END HORIZONTAL BLANK				

Bits 4–0 END HORIZONTAL BLANK
7-bit Value = least significant 7 bits of the character clock counter value at which time horizontal blanking ends. To obtain this value, add the desired $\overline{\text{BLANK}}$ pulse width in character clocks to the Start Horizontal Blank value, which is also in character clocks. The 5 least significant bits of this sum are programmed into this field. The sixth bit is programmed into bit 7 of CR5. The seventh bit is programmed into bit 3 of CR5D.

Bits 6–5 DSP-SKW - Display Skew
These two bits determine the amount of display enable skew. Display enable skew control provides sufficient time for the CRT Controller to access the display buffer to obtain a character and attribute code, access the character generator font, and then go through the Horizontal Pixel Panning register in the Attribute Controller. Each access requires the display enable signal to be skewed one character clock unit so the video output is synchronous with the HSYNC and VSYNC signals. The bit values and amount of skew are shown in the following table:
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved

Start Horizontal Sync Position Register (S_H_SY_P) (CR4)

Read/Write Address: 3?5H, Index 04H
Power-On Default: Undefined Paired

This register is used to adjust the screen center horizontally and to specify the character position at which HSYNC becomes active. Bit 8 of this value is bit 4 of CR5D.

7	6	5	4	3	2	1	0
START HORIZONTAL SYNC POSITION							

Bits 7–0 START HORIZONTAL SYNC POSITION.
9-bit Value = character clock counter value at which HSYNC becomes active. This register contains the least significant 8 bits of this value.

End Horizontal Sync Position Register (E_H_SY_P) (CR5)

Read/Write Address: 3?5H, Index 05H
Power-On Default: Undefined Paired

This register specifies when the HSYNC signal becomes inactive and the horizontal skew. The HSYNC pulse defined by this register can be extended by 32 DCLKs via bit 5 of CR5D.

7	6	5	4	3	2	1	0
EHB b5	HOR-SKW 1	0	END HORIZONTAL SYNC POS				

Bits 4–0 END HORIZONTAL SYNC POS
6-bit Value = 6 least significant bits of the character clock counter value at which time HSYNC becomes inactive. To obtain this value, add the desired HSYNC pulse width in character clocks to the Start Horizontal Sync Position value, also in character clocks. The 5 least significant bits of this sum are programmed into this field. The sixth bit is programmed into bit 5 of CR5D.

Bits 6–5 HOR-SKW - Horizontal Skew
These bits control the skew of the HSYNC signal. A binary 00 equals no HSYNC delay. For some modes, it is necessary to provide an HSYNC signal that takes up the entire blanking interval. Some internal timings are generated by the falling edge of the HSYNC signal. To guarantee the signals are latched properly, HSYNC is asserted before the end of the display enable signal, and then skewed several character clock times to provide the proper screen centering.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 EHB b5
End Horizontal Blanking bit 5.

Vertical Total Register (V_TOTAL) (CR6)

Read/Write Address: 3?5H, Index 06H
Power-On Default: Undefined Paired

This register specifies the number of scan lines from one VSYNC active to the next VSYNC active. The scan line counter resets to 0 at this point. Bit 8 is bit 0 of CR7. Bit 9 is bit 5 of CR7. Bit 10 is bit 0 of CR5E.

7	6	5	4	3	2	1	0
VERTICAL TOTAL							

Bits 7–0 VERTICAL TOTAL
11-bit Value = (number of scan lines from VSYNC active to the next VSYNC active) - 2.
This register contains the least significant 8 bits of this value.

CRTC Overflow Register (OVFL_REG) (CR7)

Read/Write Address: 3?5H, Index 07H
Power-On Default: Undefined Paired

7	6	5	4	3	2	1	0
VRS 9	VDE 9	VT 9	LCM 8	SVB 8	VRS 8	VDE 8	VT 8

This register provides extension bits for fields in other registers.

Bit 0 Bit 8 of the Vertical Total register (CR6)

Bit 1 Bit 8 of the Vertical Display End register (CR12)

Bit 2 Bit 8 of the Vertical Retrace Start register (CR10)

Bit 3 Bit 8 of the Start Vertical Blank register (CR15)

Bit 4 Bit 8 of the Line Compare register (CR18)

Bit 5 Bit 9 of the Vertical Total register (CR6)

Bit 6 Bit 9 of the Vertical Display End register (CR12)

Bit 7 Bit 9 of the Vertical Retrace Start register (CR10)

Preset Row Scan Register (P_R_SCAN) (CR8)

Read/Write Address: 3?5H, Index 08H
Power-On Default: Undefined Paired

This register is used for the pixel scrolling and panning, and text formatting and vertical scrolling.

7	6	5	4	3	2	1	0
= 0	BYTE-PAN 1	0	PRE-SET ROW SCAN COUNT				

Bits 4–0 PRE-SET ROW SCAN COUNT
Value = starting row within a character cell for the first character row displayed after vertical retrace. This allows a partial character row to be displayed at the top of the display and is used for scrolling.

Bits 6–5 BYTE-PAN
Value = number of bytes to pan. The number of pixels to pan is specified in AR13.

Bit 7 Reserved = 0

Maximum Scan Line Register (MAX_S_LN) (CR9)

Read/Write Address: 3?5H, Index 09H
Power-On Default: Undefined Paired

This register specifies the number of scan lines per character row and provides one scanning control bit and two overflow bits.

7	6	5	4	3	2	1	0
DBL SCN	LCM 9	SVB 9	MAX SCAN LINE				

Bits 4–0 MAX SCAN LINE
Value = (number of scan lines per character row) - 1

Bit 5 SVB 9
Bit 9 of the Start Vertical Blank Register (CR15)

Bit 6 LCM 9
Bit 9 of the Line Compare Register (CR18)

Bit 7 DBL SCN
0 = Normal operation
1 = Enables double scanning operation. Each line is displayed twice by repeating the row scan counter and video memory address. Vertical parameters in the CRT controller are not affected.

Cursor Start Scan Line Register (CSSL) (CRA)

Read/Write Address: 3?5H, Index 0AH
Power-On Default: Undefined Shared

The cursor start register defines the row scan of a character line where the cursor begins.

7	6	5	4	3	2	1	0
= 0	= 0	CSR OFF	CSR CURSOR START SCAN LINE				

Bits 4–0 CSR CURSOR START SCAN LINE
Value = (starting cursor row within the character cell) - 1. When the cursor start register is programmed with a value greater than the cursor end register, no cursor is generated.

Bit 5 CSR OFF
0 = Turns on the text cursor
1 = Turns off the text cursor

Bits 7–6 Reserved = 0

Cursor End Scan Line Register (CESL) (CRB)

Read/Write Address: 3?5H, Index 0BH
Power-On Default: Undefined Shared

This register defines the row scan of a character line where the cursor ends.

7	6	5	4	3	2	1	0
= 0	CSR-SKW 1	0	CURSOR END SCAN LINE				

Bits 4–0 CURSOR END SCAN LINE
Value = ending scan line number within the character cell for the text cursor. If the value of the cursor start scan line is greater than the value of cursor end line, then no cursor is generated.

Bits 6–5 CSR-SKW - Cursor Skew
These bits control the delay skew of the cursor signal. Cursor skew delays the text cursor by the selected number of clocks. For example, a skew of 1 moves the cursor right one character position on the screen.
00 = Zero character clock skew
01 = One character clock skew
10 = Two character clock skew
11 = Three character clock skew

Bit 7 Reserved = 0

Start Address High Register (STA(H)) (CRC)

Read/Write Address: 3?5H, Index 0CH
Power-On Default: Undefined Paired

15	14	13	12	11	10	9	8
DISPLAY START ADDRESS (HIGH)							

20-bit Value = the first address after a vertical retrace at which the display on the screen begins on each screen refresh. These along with bits 2-0 of CR69 are the high order start address bits.

Start Address Low Register (STA(L)) (CRD)

Read/Write Address: 3?5H, Index 0DH
Power-On Default: Undefined Paired

7	6	5	4	3	2	1	0
DISPLAY START ADDRESS (LOW)							

Start address (low) contains the 8 low order bits of the address.

Cursor Location Address High Register (CLA(H)) (CRE)

Read/Write Address: 3?5H, Index 0EH
Power-On Default: Undefined Shared

15	14	13	12	11	10	9	8
CURSOR LOCATION ADDRESS (HIGH)							

20-bit Value = the cursor location address of the video memory where the text cursor is active. This register along with bits 2-0 of CR69 are the high order bits of the address.

Cursor Location Address Low Register (CLA(L)) (CRF)

Read/Write Address: 3?5H, Index 0FH
Power-On Default: Undefined Shared

7	6	5	4	3	2	1	0
CURSOR LOCATION ADDRESS (LOW)							

Cursor location address (low) contains the 8 low order bits of the address.

Vertical Retrace Start Register (VRS) (CR10)

Read/Write Address: 3?5H, Index 10H
Power-On Default: Undefined Paired

7	6	5	4	3	2	1	0
VERTICAL RETRACE START							

Bits 7–0 VERTICAL RETRACE START.
11-bit Value = scan line counter value at which VSYNC becomes active. These are the low-order 8 bits. Bit 8 is bit 2 of CR7. Bit 9 is bit 7 of CR7. Bit 10 is bit 4 of CR5E.

Vertical Retrace End Register (VRE) (CR11)

Read/Write Address: 3?5H, Index 11H
Power-On Default: 0xH Paired

This register controls the vertical interrupt and CR0-7

7	6	5	4	3	2	1	0
LOCK R0-7	REF 3/5	DIS VINT	CLR VINT	VERTICAL RETRACE END			

Bits 3–0 VERTICAL RETRACE END
Value = least significant 4 bits of the scan line counter value at which VSYNC goes inactive. To obtain this value, add the desired VSYNC pulse width in scan line units to the CR10 value, also in scan line units. The 4 least significant bits of this sum are programmed into this field. This allows a maximum VSYNC pulse width of 15 scan line units.

Bit 4 $\overline{\text{CLR}}$ VINT - Clear Vertical Retrace Interrupt
0 = Vertical retrace interrupt cleared
1 = The flip-flop is able to catch the next interrupt request

At the end of active vertical display time, a flip-flop is set for a vertical interrupt. The output of this flip-flop goes to the system interrupt controller. The CPU has to reset this flip-flop by writing a logical 0 to this bit while in the interrupt process, then set the bit to 1 to allow the flip-flop to catch the next interrupt request. Do not change the other bits in this register. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on.

Bit 5 DIS VINT - Disable Vertical Interrupt
0 = Vertical retrace interrupt enabled if CR32_4 = 1
1 = Vertical interrupt disabled. This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on

Bit 6 REF 3/5 - Refresh Cycle Select
0 = Three DRAM refresh cycles generated per horizontal line
1 = Five DRAM refresh cycles generated per horizontal line. Selecting five refresh cycles allows use of the VGA chip with slow sweep rate displays (15.75 KHz). This bit is cleared to 0 by the BIOS during a mode set, a reset, or power-on. This setting can be overridden via bits 1-0 of CR3A

Bit 7 LOCK R0-7 - Lock Writes to CRT Controller Registers
0 = Writing to all CRT Controller registers enabled
1 = Writing to all bits of the CRT Controller registers CR0–CR7 except bit 4 of CR7 (LCM8) disabled. This bit is set to 1 by the BIOS during a mode set, a reset or power-on

Vertical Display End Register (VDE) (CR12)

Read/Write Address: 3?5H, Index 12H
Power-On Default: Undefined Paired

The vertical display enable end register defines 8 bits of the 10-bit address of the scan line where the display on the screen ends. Bit 8 and Bit 9 are bits 1 and 6 of CR7. Bit 10 is bit 1 of CR5E.

7	6	5	4	3	2	1	0
VERTICAL DISPLAY END							

Bit 7–0 VERTICAL DISPLAY END
11-bit Value = (number of scan lines of active display) - 1. This register contains the least significant 8 bits of this value.

Offset Register (SCREEN-OFFSET) (CR13)

Read/Write Address: 3?5H, Index 13H
Power-On Default: Undefined Paired

This register specifies the logical line width of the screen and is sometimes called the screen pitch. The starting memory address for the next display row is larger than the current row by two, four or eight times this amount. Bits 5-4 of CR51 are extension bits 9-8 of this register.

7	6	5	4	3	2	1	0
LOGICAL SCREEN WIDTH							

Bits 7–0 LOGICAL SCREEN WIDTH
10-bit Value = quantity that is multiplied by 2 (word mode), 4 (doubleword mode) or 8 (quadword mode) to specify the difference between the starting byte addresses of two consecutive scan lines. This register contains the least significant 8 bits of this value. The addressing mode is specified by bit 6 of CR14 and bit 3 of CR17. Setting bit 3 of CR31 to 1 forces doubleword mode.

Underline Location Register (ULL) (CR14)

Read/Write Address: 3?5H, Index 14H
Power-On Default: Undefined Paired

This register specifies the horizontal row scan position of underline and display buffer addressing modes.

7	6	5	4	3	2	1	0
= 0	DBWD MODE	CNT BY4	UNDER LINE LOCATION				

Bits 4–0 UNDER LINE LOCATION
5-bit Value = (scan line count of a character row on which an underline occurs) -1

Bit 5 CNT BY4 - Select Count by 4 Mode
0 = The memory address counter depends on bit 3 of CR17 (count by 2)
1 = The memory address counter is incremented every four character clocks

The CNT BY4 bit is used when double word addresses are used.

Bit 6 DBLWD MODE - Select Doubleword Mode
0 = The memory addresses are byte or word addresses
1 = The memory addresses are doubleword addresses

Bit 7 Reserved = 0

Start Vertical Blank Register (SVB) (CR15)

Read/Write Address: 3?5H, Index 15H
Power-On Default: Undefined Paired

This register specifies the scan line at which the vertical blanking period begins. Bit 8 is bit 3 of CR7. Bit 9 is bit 5 of CR9. Bit 10 is bit 2 of CR5E.

7	6	5	4	3	2	1	0
START VERTICAL BLANK							

Bits 7–0 START VERTICAL BLANK.
11-bit value = (scan line count at which $\overline{\text{BLANK}}$ becomes active) - 1. This register contains the least significant 8 bits of this value.

End Vertical Blank Register (EVB) (CR16)

Read/Write Address: 3?5H, Index 16H
Power-On Default: Undefined Paired

This register specifies the scan line count value when the vertical blank period ends.

7	6	5	4	3	2	1	0
END VERTICAL BLANK							

Bits 7–0 END VERTICAL BLANK
Value = least significant 8 bits of the scan line counter value at which vertical blanking ends. To obtain this value, add the desired width of the vertical blanking pulse in scan lines to the value in the Start Vertical Blank register, also in scan lines. The 8 least significant bits of this sum are programmed into this field. This allows a maximum vertical blanking pulse of 255 scan line units.

CRTC Mode Control Register (CRT_MD) (CR17)

Read/Write Address: 3?5H, Index 17H
Power-On Default: 00H Paired

This register is a multifunction control register, with each bit defining a different specification.

7	6	5	4	3	2	1	0
RST	BYTE MODE	ADW 16K	= 0	WRD MODE	VT X2	4BK HGC	2BK CGA

Bit 0 $\overline{2BK}$ CGA - Select Bank 2 Mode for CGA Emulation
0 = Row scan counter bit 0 is substituted for memory address bit 13 during active display time
1 = Memory address bit 13 appears on the memory address output bit 13 signal of the CRT controller

This bit allows memory mapping compatibility with the IBM CGA graphics mode.

Bit 1 $\overline{4BK}$ HGC - Select Bank 4 Mode for HGA Emulation
0 = Row scan counter bit 1 is substituted for memory address bit 14 during active display time
1 = Memory address bit 14 appears on the memory address output bit 14 signal of the CRT controller

The combination of this bit and bit 0 of this register allows compatibility with Hercules HGC graphics memory mapping.

Bit 2 VT X2 - Select Vertical Total Double Mode
0 = Horizontal retrace clock selected
1 = Horizontal retrace clock divided by two selected

This bit selects horizontal retrace clock or horizontal retrace clock divided by two as the clock that controls the vertical timing counter. If the vertical retrace counter is clocked with the horizontal retrace clock divided by 2, then the vertical resolution is double.

Bit 3 CNT BY2 - Select Word Mode
0 = Memory address counter is clocked with the character clock input, and byte mode addressing for the video memory is selected
1 = Memory address counter is clocked by the character clock input divided by 2, and word mode addressing for the video memory is selected

Bit 4 Reserved = 0

Bit 5 $\overline{\text{ADW}}$ 16K - Address Wrap
0 = When word mode is selected by bit 6 of this register, memory address counter bit 13 appears on the memory address output bit 0 signal of the CRT controller and the video memory address wraps around at 16 KBytes
1 = When word mode is selected by bit 6 of this register, memory address counter bit 15 appears on the memory address output bit 0 signal of the CRT controller

This bit is useful in implementing IBM CGA mode.

Bit 6 BYTE MODE - Select Byte Addressing Mode
0 = Word mode shifts all memory address counter bits down one bit, and the most significant bit of the counter appears on the least significant bit of the memory address output
1 = Byte address mode

Bit 7 $\overline{\text{RST}}$ - Hardware Reset
0 = Vertical and horizontal retrace pulses always inactive
1 = Vertical and horizontal retrace pulses enabled

This bit does not reset any other registers or outputs.

Line Compare Register (LCM) (CR18)

Read/Write Address: 3?5H, Index 18H
Power-On Default: Undefined Paired

This register is used to implement a split screen function. When the scan line counter value is equal to the content of this register, the memory address counter is cleared to 0. The linear address counter then sequentially addresses the display buffer starting at address 0. Each subsequent row address is determined by the addition of the Offset (CR13) register content. Bit 8 is bit 4 of CR7. Bit 9 is bit 6 of CR9. Bit 10 is bit 6 of CR5E.

7	6	5	4	3	2	1	0
LINE COMPARE POSITION							

Bit 7–0 LINE COMPARE POSITION
11-bit Value = number of scan lines at which the screen is split into screen A and screen B. This register contains the least significant 8 bits of this value.

CPU Latch Data Register (GCCL) (CR22)

Read Only Address: 3?5H, Index 22H
Power-On Default: Undefined Paired

This register is used to read the CPU latch in the Graphics Controller.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER CPU LATCH - N							

Bits 7–0 GRAPHICS CONTROLLER CPU LATCH - N
Bits 1-0 of GR4 select the latch number N (3-0) of the CPU Latch.

Attribute Index Register (ATC_F/I) (CR24)

Read Only Address: 3?5H, Index 24H, 26H
Power-On Default: Undefined Paired

This register is used to read the value of the Attribute Controller Index register and its associated internal address flip-flop (AFF). It can be read at either index 24H or 26H.

7	6	5	4	3	2	1	0
AFF	= 0	ENV	ATTRIBUTE CONTROLLER INDEX				

Bits 4–0 ATTRIBUTE CONTROLLER INDEX
This value is the Attribute Controller Index Data at I/O port 3C0H.

Bit 5 ENV- Enable Video Display
This is the setting of bit 5 of 3C0H, indicating video display enabled status (1 = enabled).

Bit 6 Reserved = 0

Bit 7 $\overline{\text{AFF}}$
Inverted Internal Address flip-flop

17.4 GRAPHICS CONTROLLER REGISTERS

The graphics controller registers are located at a two byte I/O address space. These registers are accessed by first writing an index to the Graphics Address register (at 3CEH) and then accessing the Data register (at 3CFH).

Graphics Controller Index Register (GRC_ADR)

Read/Write Address: 3CEH
Power-On Default: Undefined

This register is loaded with a binary index value that determines which graphics controller register will be accessed. This value is referred to as the "Index Number" of the GR register (GR0–6).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	GR CONT ADDRESS			

Bits 3–0 GR CONT ADDRESS - Graphics Controller Register Index
A binary value indexing the register where data is to be accessed.

Bits 7–4 Reserved = 0

Graphics Controller Data Register (GRC_DATA)

Read/Write Address: 3CFH
Power-On Default: Undefined

This register is the data port for the graphics controller register indexed by the Graphics Controller Index register.

7	6	5	4	3	2	1	0
GRAPHICS CONTROLLER DATA							

Bit 7–0 GRAPHICS CONTROLLER DATA
Data to the Graphics Controller register indexed by the graphics controller address.

Set/Reset Data Register (SET/RST_DT) (GR0)

Read/Write Address: 3CFH, Index 00H
Power-On Default: Undefined

This register represents the value written to all 8 bits of the respective memory plane when the CPU executes a memory write in write modes 0 and 3.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	SET/RESET DATA			

Bits 3–0 SET/RESET DATA
These bits become the color value for CPU memory write operations. In write mode 0, the set/reset data can be enabled on the corresponding bit of the Enable Set/Reset Data register. In write mode 3, there is no effect on the Enable Set/Reset Data register.

Bits 7–4 Reserved = 0

Enable Set/Reset Data Register (EN_S/R_DT) (GR1)

Read/Write Address: 3CFH, Index 01H
Power-On Default: Undefined

These bits enable the set/reset data, and affect write mode 0.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	ENB SET/RST DATA			

Bits 3–0 ENB SET/RST DATA
When each bit is a logical 1, the respective memory plane is written with the value of the Set/Reset Data register. A logical 0 disables the set/reset data in a plane, and that plane is written with the value of CPU write data.

Bits 7–4 Reserved = 0

Color Compare Register (COLOR-CMP) (GR2)

Read/Write Address: 3CFH, Index 02H
Power-On Default: Undefined

These bits represent a 4-bit color value to be compared. In read mode 1, the CPU executes a memory read, the read data is compared with this value and returns the results. This register works in conjunction with the Color Don't Care register.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COLOR COMPARE DATA			

Bits 3–0 COLOR COMPARE DATA
This value becomes the reference color used to compare each pixel. Each of the 8-bit positions of the read data are compared across four planes and a logical 1 is returned in each bit position for which the colors match.

Bits 7–4 Reserved = 0

Raster Operation/Rotate Count Register (WT_ROP/RTC) (GR3)

Read/Write Address: 3CFH, Index 03H
Power-On Default: Undefined

This register selects a raster operation function and indicates the number of bits the CPU data will be rotated (right) on the video memory write operation.

7	6	5	4	3	2	1	0
			RST-OP				
= 0	= 0	= 0	1	0	ROTATE-COUNT		

Bits 2–0 ROTATE-COUNT
These bits define a binary encoded value of the number of positions to right-rotate data during a CPU memory write. To write non-rotated data, the CPU must preset a count of 0.

Bits 4–3 RST-OP - Select Raster Operation
The data written to memory can operate logically with the data already in the processor latches. This function is not available in write mode 1. The logical functions are defined as follows:
00 = No operation
01 = Logical AND with latched data
10 = Logical OR with latched data
11 = Logical XOR with latched data

The logical function specified by this register is applied to data being written to memory while in modes 0, 2 and 3.

Bits 7–5 Reserved = 0

Read Plane Select Register (RD_PL_SL) (GR4)

Read/Write Address: 3CFH, Index 04H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
						RD-PL-SL	
= 0	= 0	= 0	= 0	= 0	= 0	1	0

The contents of this register represent the memory plane from which the CPU reads data in read mode 0. This register has no effect on the color compare read mode (read mode 1). In odd/even mode, bit 0 is ignored. Four memory planes are selected as follows:

Bits 1–0 RD-PL-SL - Read Plane Select
The memory plane is selected as follows:
00 = Plane 0
01 = Plane 1
10 = Plane 2
11 = Plane 3

Bits 7–2 Reserved = 0

Graphics Controller Mode Register (GRP_MODE) (GR5)

Read/Write Address: 3CFH, Index 05H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
	SHF-MODE		O/E	RD		WRT-MD	
= 0	256	O/E	MAP	CMP	= 0	1	0

This register controls the mode of the Graphics Controller as follows:

Bit 1–0 WRT-MD - Select Write Mode
These bits select the CPU write mode into video memory. The function of each mode is defined as follows:
00 = Write Mode 0. Each of four video memory planes is written with the CPU data rotated by the number of counts in the rotate register. If the Set/Reset register is enabled for any of four planes, the corresponding plane is written with the data stored in the set/reset register. Raster operations and bit mask registers are effective
01 = Write Mode 1. Each of four video memory planes is written with the data in the processor latches. These latches are loaded during previous CPU read operations. Raster operation, rotate count, set/reset data, enable set/reset data and bit mask registers are not effective
10 = Write Mode 2. Memory planes 0-3 are filled with 8 bits of the value of CPU write data bits 0-3, respectively. For example, if write data bit 0 is a 1, eight 1's are written to memory plane 0. The data on the CPU data bus is treated as the color value. The Bit Mask register is effective as the Mask register. A logical 1 in the Bit Mask register sets the corresponding pixel in the addressed byte to the color specified on the data bus. A logical 0 in the Bit Mask register sets the corresponding pixel in the addressed byte to the corresponding pixel in the processor latches. The Set/Reset, Enable Set/Reset and Rotate Count registers are ignored
11 = Write Mode 3. Each of four video memory planes is written with 8 bits of the color value contained in the set/reset register for that plane. The Enable Set/Reset register is not effective. Rotated CPU write data is ANDed with the bit mask register to form an 8-bit value that performs the same function as the Bit Mask register in write modes 0 and 2. This write mode can be used to fill an area with a single color and pattern

Bit 2 Reserved = 0

Bit 3 RD CMP - Enable Read Compare
0 = The CPU reads data from the video memory planes. The plane is selected by the Read Plane Select register. This is called read mode 0
1 = The CPU reads the results of the logical comparison between the data in four video memory planes selected by the contents of the Color Don't Care register and the contents of the Color Compare register. The result is a 1 for a match and 0 for a mismatch on each pixel. This is called read mode 1

Bit 4 O/E MAP - Select Odd/Even Addressing
0 = Standard addressing.
1 = Odd/even addressing mode selected. Even CPU addresses access plane 0 and 2, while odd CPU addresses access plane 1 and 3. This option is useful for emulating the CGA compatible mode. The value of this bit should be the inverted value programmed in bit 2 of the Sequencer Memory Mode register (SR4). This bit affects reading of display memory by the CPU

Bit 5 SHF-MODE - Select Odd/Even Shift Mode
0 = Normal shift mode
1 = The video shift registers in the graphics section are directed to format the serial data stream with even-numbered bits from both planes on the even-numbered planes and odd-numbered bits from both planes on the odd planes

Bit 6 SHF-MODE - Select 256 Color Shift Mode
0 = Bit 5 in this register controls operation of the video shift registers
1 = The shift registers are loaded in a manner that supports the 256 color mode

Bit 7 Reserved = 0

Memory Map Mode Control Register (MISC_GM) (GR6)

Read/Write Address: 3CFH, Index 06H
Power-On Default: Undefined

This register controls the video memory addressing.

7	6	5	4	3	2	1	0
				MEM-MAP		CHN	TXT
= 0	= 0	= 0	= 0	1	0	O/E	/GR

Bit 0 $\overline{\text{TXT}}$/GR - Select Text/Graphics Mode
0 = Text mode display addressing selected
1 = Graphics mode display addressing selected. When set to graphics mode, the character generator address latches are disabled

Bit 1 CHN O/E - Chain Odd/Even Planes
0 = A0 address bit unchanged
1 = CPU address bit A0 is replaced by a higher order address bit. The content of A0 determines which memory plane is to be addressed. A0 = 0 selects planes 0 and 2, and A0 = 1 selects planes 1 and 3. This mode can be used to double the address space into video memory

Bits 3–2 MEM-MAP - Memory Map Mode
These bits control the address mapping of video memory into the CPU address space. The bit functions are defined below.
00 = A0000H to BFFFFH (128 KBytes)
01 = A0000H to AFFFFH (64 KBytes)
10 = B0000H to B7FFFH (32 KBytes)
11 = B8000H to BFFFFH (32 KBytes)

Bits 7–4 Reserved = 0

Color Don't Care Register (CMP_DNTC) (GR7)

Read/Write Address: 3CFH, Index 07H
Power-On Default: Undefined

This register is effective in read mode 1, and controls whether the corresponding bit of the Color Compare Register is to be ignored or used for color comparison.

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	COMPARE PLANE SEL			

Bits 3–0 COMPARE PLANE SEL - Compare Plane Select
0 = The corresponding color plane becomes a don't care plane when the CPU read from the video memory is performed in read mode 1
1 = The corresponding color plane is used for color comparison with the data in the Color Compare register

Bits 7–4 Reserved = 0

Bit Mask Register (BIT_MASK) (GR8)

Read/Write Address: 3CFH, Index 08H
Power-On Default: Undefined

Any bit programmed to 0 in this register will cause the corresponding bit in each of four memory planes to be immune to change. The data written into memory in this case is the data which was read in the previous cycle, and was stored in the processor latches. Any bit programmed to 1 allows unimpeded writes to the corresponding bits in the plane.

7	6	5	4	3	2	1	0
BIT MASK							

Bits 7–0 BIT MASK
A logical 0 means the corresponding bit of each plane in memory is set to the corresponding bit in the processor latches. A logical 1 means the corresponding bit of each plane in memory is set as specified by other conditions.

17.5 ATTRIBUTE CONTROLLER REGISTERS

The attribute controller registers are located at the same byte I/O address for writing address and data. An internal address flip-flop (AFF) controls the selection of either the attribute index or data registers. To initialize the address flip-flop (AFF), an I/O read is issued at address 3BAH or 3DAH. This presets the address flip-flop to select the index register. After the index register has been loaded by an I/O write to address 3C0H, AFF toggles and the next I/O write loads the data register. Every I/O write to address 3C0H toggles this address flip-flop. However, it does not toggle for I/O reads at address 3C0H or 3C1H. The Attribute Controller Index register is read at 3C0H, and the Attribute Controller Data register is read at address 3C1H.

Attribute Controller Index Register (ATR_AD)

Read/Write Address: 3C0H
Power-On Default: Undefined

This register is loaded with a binary index value that determines which attribute controller register will be accessed. This value is referred to as the "Index Number" of the AR register (AR0–14).

7	6	5	4	3	2	1	0
R	R	ENB PLT	ATTRIBUTE ADDRESS				

Bits 4–0 ATTRIBUTE ADDRESS
A binary value that points to the attribute controller register where data is to be written.

Bit 5 ENB PLT - Enable Video Display
0 = Video display access to the palette registers disabled. The Attribute Controller register can be accessed by the CPU
1 = Display video using the palette registers enabled (normal display operation). The palette registers (AR0–ARF) cannot be accessed by the CPU

This bit is effective only in 8-bit PA mode (CR67_4 = 0).

Bits 7–6 Reserved

Attribute Controller Data Register (ATR_DATA)

Read/Write Address: R: 3C1H/W: 3COH
Power-On Default: Undefined

This register is the data port for the attribute controller register indexed by the Attribute Controller Index register.

7	6	5	4	3	2	1	0
ATTRIBUTE DATA							

Bits 7–0 ATTRIBUTE DATA
Data to the attribute controller register indexed by the attribute controller address.

Palette Registers (PLT_REG) (AR00-0F)

Read/Write Address: 3C1H/3C0H, Index 00H-0FH
Power-On Default: Undefined

These are 16, 6-bit registers pointed to by the index and color code. They allow a dynamic mapping between the text attribute or graphics color input and the display color on the CRT screen.

7	6	5	4	3	2	1	0
		SECONDARY			PRIMARY		
= 0	= 0	SR	SG	SB	R	G	B

Bits 5–0 PALETTE COLOR
The six bit display color, bits 5-0 are output as SR, SG/I, SB/V, R, G and B, respectively.

Bits 7–6 Reserved = 0

Attribute Mode Control Register (ATR_MODE) (AR10)

Read/Write
Power-On Default: 00H

Address: 3C1H/3C0H, Index 10H

The contents of this register controls the attribute mode of the display function.

7	6	5	4	3	2	1	0
SEL V54	256 CLR	TOP PAN	= 0	ENB BLNK	ENB LGC	MONO ATRB	TX/GR

Bit 0 $\overline{TX}$/GR - Select Graphics Mode
0 = Selects text attribute control mode
1 = Selects graphics control mode

Bit 1 MONO ATRB - Select Monochrome Attributes
0 = Selects color display text attributes
1 = Selects monochrome display text attributes

Bit 2 ENB LGC - Enable Line Graphics
0 = The ninth dot of a text character (bit 0 of SR1 = 0) is the same as the background
1 = Special line graphics character codes enabled

When this bit is set to 1, it forces the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0H through DFH. For other characters, the ninth dot is the same as the background.

Bit 3 ENB BLNK - Enable Blinking
0 = Selects the background intensity for the text attribute input
1 = Selects blink attribute in text modes

This bit must also be set to 1 for blinking graphics modes. The blinking counter is operated by the vertical retrace counter (VRTC) input. It divides the VRTC input by 32. The blinking rates are ON for 16 VRTC clocks and OFF for 16 VRTC clocks. In the graphics mode, when blink is activated, the most significant color bit (bit 3) for each dot is inverted alternately, thus allowing two different colors to be displayed for 16 VRTC clocks each.

When the cursor is displayed in the text mode, it is blinked at a rate of ON for 8 VRTC clocks and OFF for 8 VRTC clocks (period by 16 frames). The displayed characters are independently blinked at the rate of 32 frames as above.

Bit 4 Reserved = 0

Bit 5 TOP PAN - Top Panning Enable
0 = Line compare has no effect on the output of the pixel panning register
1 = Forces the output of the pixel panning register to 0 after matching line compare until VSYNC occurs in the CRT controller. At the top of screen the output of the Pixel Panning register returns to its programmed value. This bit allows a top portion of a split screen to be panned.

Bit 6 256 CLR - Select 256 Color Mode
0 = 4 bits of video (translated to 6 bits by the palette) are output every internal dot-clock cycle
1 = Two 4-bit sets of video data are assembled to generate 8-bit video data at half the frequency of the internal dot-clock

Bit 7 SEL V54 - Select V[5:4]
0 = In VGA, mode, bits 5-4 of video output are generated by the attribute palette registers. Bits 7-6 of video output are always generated by bits 3-2 of AR14
1 = Bits 5-4 of video output are generated by bits 1-0 of AR14

Border Color Register (BDR_CLR) (AR11)

Read/Write
Power-On Default: 00H
Address: 3C1H/3C0H, Index 11H
Shared

7	6	5	4	3	2	1	0
BORDER COLOR							

Bits 7–0 Border Color. This 8-bit register determines the border color displayed on the CRT screen. The border is an area around the screen display area.

This register is only effective in 8-bit PA modes (CR67_4 = 0). See also CR33_5.

Color Plane Enable Register (DISP_PLN) (AR12)

Read/Write
Power-On Default: 00H
Address: 3C1H/3C0H, Index 12H

This register enables the respective video memory color plane 3–0 and selects video color outputs to be read back in the display status.

7	6	5	4	3	2	1	0
= 0	= 0	VDT-SEL 1	0	DISPLAY PLANE ENBL			

Bits 3–0 DISPLAY PLANE ENBL
A 0 in any of these bits forces the corresponding color plane bit to 0 before accessing the internal palette. A 1 in any of these bits enables the data on the corresponding color plane.

Bits 5–4 VDT-SEL - Video Test Select
These bits select two of the eight bit color outputs to be available in the Input Status 1 register. The output color combinations available on the status bits are as follows:

D STS MUX		STS 1	
Bit 5	**Bit 4**	**Bit 5**	**Bit 4**
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Bits 7–6 Reserved = 0

Horizontal Pixel Panning Register (H_PX_PAN) (AR13)

Read/Write Address: 3C1H/3C0H, Index 13H
Power-On Default: 00H

This register specifies the number of pixels to shift the display data horizontally to the left. Pixel panning is available in both text and graphics modes. It is not available with Enhanced mode memory mappings (CR31_3 = 1).

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	NUMBER OF PAN SHIFT			

Bits 3–0 NUMBER OF PAN SHIFT
This register selects the number of pixels to shift the display data horizontally to the left. In the 9 pixels/character text mode, the output can be shifted a maximum shift of 8 pixels. In the 8 pixels/character text mode and all graphics modes, except 256 color mode, a maximum shift of 7 pixels is possible. In the 256 color mode, bit 0 of this register must be 0 resulting in only 4 panning positions per display byte. The panning is controlled as follows:

	Number of pixels shifted in		
Bits 3–0	**9 pixel/char.**	**8 pixel/char.**	**256 color mode**
0000	1	0	0
0001	2	1	–
0010	3	2	1
0011	4	3	–
0100	5	4	2
0101	6	5	–
0110	7	6	3
0111	8	7	–
1000	0	–	–

Bits 7–4 Reserved = 0

Pixel Padding Register (PX_PADD) (AR14)

Read/Write Address: 3C1H/3C0H, Index 14H
Power-On Default: 00H

This register specifies the high-order bits of video output when pixel padding is enabled and disabled in the 256 color mode.

7	6	5	4	3	2	1	0
				PIXEL PADDING			
= 0	= 0	= 0	= 0	V7	V6	V5	V4

Bits 1–0 PIXEL PADDING V5, V4
These bits are enabled with a logical 1 of bit 7 of AR10, and can be used in place of the V5 and V4 bits from the Palette registers to form the 8-bit digital color value output.

Bits 3–2 PIXEL PADDING V7, V6
In all modes except 256 color mode, these bits are the two high-order bits of the 8-bit digital color value output.

Bits 7–4 Reserved = 0

17.6 RAMDAC REGISTERS

All of the RAMDAC registers described in this section are physically located inside Aurora.

DAC Mask Register (DAC_AD_MK)

Read/Write Address: 3C6H
Power-On Default: Undefined

This register is the pixel read mask register to select pixel video output. The CPU can access this register at any time.

7	6	5	4	3	2	1	0
DAC ADDRESS MASK							

Bits 7–0 DAC ADDRESS MASK
The contents of this register are bit-wise logically ANDed with the pixel select video output (PA[7:0]). This register is initialized to FFH by the BIOS during a video mode set.

DAC Read Index Register (DAC_RD_AD)

Write Only Address: 3C7H
Power-On Default: Undefined

This register contains the pointer to one of 256 palette data registers and is used when reading the color palette.

7	6	5	4	3	2	1	0
DAC READ ADDRESS							

Bits 7–0 DAC READ ADDRESS
Each time the color code is written to this register, it identifies that a read sequence will occur. A read sequence consists of three successive byte reads from the RAMDAC data register at I/O address 3C9H. The least significant 6 bits of each byte taken from the RAMDAC data register contain the corresponding color value, and the most significant 2 bits contain zeros. The order is red byte first, then green, and finally blue. The sequence of events for a read cycle is:

1. Write the color code to this register (RAMDAC Read Index) at address 3C7H.
2. The contents of the location in the color look-up table pointed to by the color code are transferred to the RAMDAC data register at address 3C9H.
3. Three bytes are read back from the RAMDAC data register.
4. The contents of this register auto-increment by one.

5. Go to step 2.

The effects of writing to the RAMDAC data register during a three-byte read cycle or reading from the RAMDAC data register during a 3-byte write cycle (i.e., interrupting the sequence) are undefined and may change the look-up table contents.

DAC Status Register (DAC_STS)

Read Only Address: 3C7H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
= 0	= 0	= 0	= 0	= 0	= 0	DAC-STS	

Bits 1–0 DAC-STS - RAMDAC Cycle Status
The last executing cycle was:
00 = Write Palette cycle
11 = Read Palette cycle

Reads from the RAMDAC Write Index at address 3C8H or the DAC status register at address 3C7H do not interfere with read or write cycles and may take place at any time.

Bits 7–2 Reserved = 0

DAC Write Index Register (DAC_WR_AD)

Read/Write Address: 3C8H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
DAC WRITE ADDRESS							

Bits 7–0 DAC WRITE ADDRESS
This register contains the pointer to one of 256 palette data registers and is used during a palette load. Each time the color code is written to this register, it identifies that a write sequence will occur. A write sequence consists of three successive byte writes to the DAC data register at I/O address 3C9H. The least significant 6 bits of each byte are concatenated to form the value placed in the 18-bit data register. The order is red byte first, then green, and finally blue. Once the third byte has been written, the value in the data register is written to the location pointed to by the color code. The sequence of events for a write cycle is:

1. Write the color code to this register (DAC Write Index) at address 3C8H.
2. Three bytes are written to the DAC Data register at address 3C9H.

3. The contents of the DAC data register are transferred to the location in the color look-up table pointed to by the color code.
4. The DAC Write Index register auto-increments by 1.
5. Go to step 2.

RAMDAC Data Register (DAC_DATA)

Read/Write Address: 3C9H
Power-On Default: Undefined

This register is a data port to read or write the contents of the location in the color look-up table pointed to by the DAC Read Index or the DAC Write Index registers.

7	6	5	4	3	2	1	0
DAC READ/WRITE DATA							

Bits 7–0 DAC READ/WRITE DATA
To prevent "snow flicker" on the screen, an application reading data from or writing data to the DAC Data register should ensure that the $\overline{\text{BLANK}}$ input to the RAMDAC is asserted. This can be accomplished either by restricting data transfers to retrace intervals, checking bit 3 of the Input Status 1 register (3?AH) to determine when retrace is occurring, or by using the screen-off bit in the Clocking Mode register of the sequencer (bit 5 of SR1).

Section 18: Extended Sequencer Register Descriptions

The following registers are located in Sequencer Register address space not used by standard VGA. An appropriate value must be programmed in SR8 to unlock access to these registers.

In the following register descriptions, 'U' stands for undefined or unused and 'R' stands for reserved (write = 0, read = U). See Appendix A for a table listing each register in this section and its page number.

18.1 MISCELLANEOUS EXTENDED SEQUENCER REGISTERS

Unlock Extended Sequencer Register (SR8)

Read/Write Address: 3C5H, Index 08H
Power-On Default: 00H

Loading xxxx0110b (e.g., 06H) unlocks accessing of all the S3 extensions (SR9 - SR6F) to the standard VGA Sequencer register set. (x = don't care).

7	6	5	4	3	2	1	0
R	R	R	R	=0	=1	=1	=0

Extended Sequencer 9 Register (SR9)

Read/Write Address: 3C5H, Index 09H
Power-On Default: 00H

This register controls the powerdown for the Controller 1 dot clock (DCLK). There are two types of DCLK used in Controller 1: the virtual DCLK is used on logic which is affected by flat panel horizontal expansion while the true DCLK is used on logic which is not affected by flat panel horizontal expansion.

7	6	5	4	3	2	1	0
MMIO	C1SU2	C1SB2	C1SU1	C1SB1	C1P1	R	R

Bits 1-0 Reserved

Bit 2 C1P1 - Controller 1 Powerdown Enable 1
0 = Controller 1 virtual DCLK is not turned off when CR67_3-2=11
1 = Controller 1 virtual DCLK is turned off when CR67_3-2=11

This bit should be programmed to 1 by the BIOS during reset.

Bit 3 C1SB1 - Controller 1 Standby Enable 1
0= Controller 1 virtual DCLK is not turned off in Standby mode
1= Controller 1 virtual DCLK is turned off in Standby mode

This bit should be programmed to 1 by the BIOS during reset.

Bit 4 C1SU1 - Controller 1 Suspend Enable 1
0 = Controller 1 virtual DCLK is not turned off in Suspend mode
1 = Controller 1 virtual DCLK is turned off in Suspend mode

This bit should be programmed to 1 by the BIOS during reset.

Bit 5 Controller 1 Standby Enable 2
0 = Controller 1 true DCLK is not turned off in Standby mode
1 = Controller 1 true DCLK is turned off in Standby mode

This bit should be programmed to 1 by the BIOS during reset.

Bit 6 Controller 1 Suspend Enable 2
0 = Controller 1 true DCLK is not turned off in Suspend mode
1 = Controller 1 true DCLK is turned off in Suspend mode

This bit should be programmed to 1 by the BIOS during reset.

Bit 7 MMIO-ONLY - Memory-mapped I/O register access only
0 = When MMIO is enabled, both programmed I/O and memory-mapped I/O register accesses are allowed
1 = When MMIO is enabled, only memory-mapped I/O register accesses are allowed to extended (non-standard VGA) registers. Both I/O and MMIO accesses can be made to standard VGA registers.

Extended Sequencer A Register (SRA)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 0AH

7	6	5	4	3	2	1	0
2 MCLK	R	PD-NTRI	R	R	R	R	R

Bits 4-0 Reserved

Bit 5 PD-NTRI - PD[63:0] Not Tri-stated
0 = PD[63:0] tri-stated
1 = PD[63:0] not tri-stated

The default value of 0 reduces power consumption. The pins are enabled for output only as needed.

Bit 6 Reserved

Bit 7 2MCLK - 2 MCLK CPU writes to memory
0 = 3 MCLK memory writes
1 = 2 MCLK memory writes

Setting this bit to 1 improves performance for systems using an MCLK less than 57 MHz. For MCLK frequencies between 55 and 57 MHz, bit 7 of SR15 should also be set to 1 if linear addressing is being used.

Extended Sequencer D Register (SRD)

Read/Write Address: 3C5H, Index 0DH
Power-On Default: 00H

This register provides feature connector control and also provides independent control of the HSYNC and VSYNC signals, therefore supporting the VESA DPMS (Display Power Management Control) standard.

7	6	5	4	3	2	1	0
VSY-CTL		HSY-CTL					LPB
1	0	1	0	R	R	R	EN

Bit 0 LPBEN - LPBEN Pin Control
0 = LPBEN pin is held at logic 0
1 = LPBEN pin is held at logic 1

This pin is used to enable/disable Scenic Highway video decoders.

Bits 3–1 Reserved

Bits 5–4 HSY-CTL - HSYNC Control
00 = Normal operation
01 = HSYNC = 0
10 = HSYNC = 1
11 = Reserved

Bits 7–6 VSY-CTL - VSYNC Control
00 = Normal operation
01 = VSYNC = 0
10 = VSYNC = 1
11 = Reserved

MCLK Value Low Register (SR10)

Read/Write Address: 3C5H, Index 10H
Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR11 generate an MCLK value of 45 MHz. All other MCLK values must be specified by programming of SR10 and SR11. Loading of a new value is enabled by either bit 0 or bit 5 of SR15.

7	6	5	4	3	2	1	0
R	PLL R VALUE		PLL N-DIVIDER VALUE				

Bits 4-0 PLL N-DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-31) divider used to scale the input to the MCLK PLL. See Section 8 for a detailed explanation.

Bits 6-5 PLL R VALUE
These bits contain the binary equivalent of the integer (1, 2, 4, 8) range value used to scale the output of the MCLK PLL. See Section 8 for a detailed explanation.

Bit 7 Reserved

MCLK Value High Register (SR11)

Read/Write Address: 3C5H, Index 11H
Power-On Default: See description below.

The power-on default value for this register in conjunction with the power-on default value for SR10 generate an MCLK value of 45 MHz. All other MCLK values must be specified by programming of SR10 and SR11. Loading of a new value is enabled by either bit 0 or bit 5 of SR15.

7	6	5	4	3	2	1	0
R	PLL M-DIVIDER VALUE						

Bits 6-0 PLL M-DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-127) divider used in the feedback loop of the MCLK PLL. See Section 8 for a detailed explanation.

Bit 7 Reserved

Enhanced Mode DCLK Value Low Register (SR12)

Read/Write Address: 3C5H, Index 12H
Power-On Default: Undefined

SR12 and SR13 are selected as the source of the DCLK PLL parameter values when 3C2H_3-2 = 11b. This setting is used for all Enhanced modes. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0.

7	6	5	4	3	2	1	0
PLL R VALUE		PLL N-DIVIDER VALUE					

Bits 5-0 PLL N-DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-63) divider used to scale the input to the DCLK PLL. See Section 8 for a detailed explanation.

Bits 7-6 PLL R VALUE
These bits contain the binary equivalent of the integer (1, 2, 4, 8) range value used to scale the output of the DCLK PLL. See Section 8 for a detailed explanation.

Enhanced Mode DCLK Value High Register (SR13)

Read/Write Address: 3C5H, Index 13H
Power-On Default: Undefined

SR12 and SR13 are selected as the source of the DCLK PLL parameter values when 3C2H_3-2 = 11b. This setting is used for all Enhanced modes. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0.

7	6	5	4	3	2	1	0
PLL M-DIVIDER VALUE							

Bits 7-0 PLL M- DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-255) divider used in the feedback loop of the DCLK PLL. See Section 8 for a detailed explanation.

CLKSYN Control 1 Register (SR14)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 14H

7	6	5	4	3	2	1	0
EXT DCLK	EXT MCLK	LTS	CLR CNT	M TEST	EN CNT	MPLL PD	DPLL PD

Bit 0 DPLL PD - Power down DCLK PLL
0 = DCLK PLL powered
1 = DCLK PLL powered down

This bit is used for S3 test purposes only.

Bit 1 MPLL PD - Power down MCLK PLL
0 = MCLK PLL powered
1 = MCLK PLL powered down

This bit is used for S3 test purposes only.

Bit 2 EN CNT - Enable clock synthesizer counters
0 = Clock synthesizer counters disabled
1 = Clock synthesizer counters enabled

This bit is used for S3 test purposes only.

Bit 3 M TEST - MCLK Test
0 = Test DCLK
1 = Test MCLK

This bit is used for S3 test purposes only.

Bit 4 CLR CNT - Clear clock synthesizer counters
0 = No effect
1 = Clear the clock synthesizer counters

This bit is used for S3 test purposes only.

Bit 5 LTS - LPBEN Pin Tri-state
0 = LPBEN pin (N1) has normal function
1 = LPBEN pin (N1) is tri-stated

Setting this bit to 1 allows pin N1 to act as an input. This is enabled by setting bit 6 of this register to 1.

Bit 6 EXT MCLK - External MCLK Select
0 = MCLK provided by internal PLL
1 = MCLK is input on pin N1. PD11 must also be strapped low on power-on reset.

An external MCLK is only used for S3 test purposes.

Bit 7 EXT DCLK - External DCLK Select
0 = DCLK provided by internal PLL
1 = DCLK is input on pin A1. PD11 must also be strapped low on power-on reset.

An external DCLK is only used for S3 test purposes.

CLKSYN Control 2 Register (SR15)

Read/Write Address: 3C5H, Index 15H
Power-On Default: 00H

7	6	5	4	3	2	1	0
2 CYC MWR	DCLK\ INV	CLK LOAD	DCLK/ 2	R	MCLK OUT	DRFQ EN	MFRQ EN

Bit 0 MFRQ EN - Enable new MCLK frequency load
0 = Register bit clear
1 = Load new MCLK frequency

When new MCLK PLL values are programmed, this bit is set to 1 to load these values in the PLL. The loading may be delayed a small but variable amount of time. This bit should be cleared to 0 after loading to prevent repeated loading. Alternately, use bit 5 of this register to produce an immediate load.

Bit 1 DFRQ EN - Enable new DCLK frequency load
0 = Register bit clear
1 = Load new DCLK frequency

When new DCLK PLL values are programmed, this bit is set to 1 to load these values in the PLL. 3C2H_3-2 select the source of the DCLK PLL values. The loading may be delayed a small but variable amount of time. Use bit 5 of this register to produce an immediate load.

Bit 2 MCLK OUT - Output internally generated MCLK
0 = Pin C3 has its normal function
1 = Pin C3 outputs the internally generated MCLK if SR1A_4 = 1

This is used only for testing.

Bit 3 DCLK OUT - Output internally generated DCLK
0 = Pin M1 has its normal function (LCLK input)
1 = Pin M1 outputs the internally generated DCLK

This is used only for testing.

Bit 4 DCLK/2 - Divide DCLK by 2
0 = DCLK unchanged
1 = Divide DCLK by 2

Either this bit or bit 6 of this register must be set to 1 for clock doubled RAMDAC operation (mode 0001).

Bit 5 CLK LOAD - MCLK, DCLK load
0 = Clock loading is controlled by bits 0 and 1 of this register
1 = Load MCLK and DCLK PLL values immediately

To produce an immediate MCLK and DCLK load, program this bit to 1 and then to 0. 3C2H_3-2 select the source of the DCLK PLL values. This register must never be left set to 1.

Bit 6 DCLK INV - Invert DCLK
0 = DCLK unchanged
1 = Invert DCLK

Either this bit or bit 4 of this register must be set to 1 for clock doubled RAMDAC operation (mode 0001).

Bit 7 2 CYC MWR - Enable 2 cycle memory write
0 = 3 MCLK memory write
1 = 2 MCLK memory write

Setting this bit to 1 bypasses the VGA logic for linear addressing when bit 7 of SRA is set to 1. This can allow 2 MCLK operation for MCLK frequencies between 55 and 57 MHz.

CLKSYN Test High Register (SR16)

Read/Write Address: 3C5H, Index 16H
Power-On Default: 00H

This register is reserved for S3 testing of the internal clock synthesizer.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

CLKSYN Test Low Register (SR17)

Read Only
Power-On Default: 00H

Address: 3C5H, Index 17H

This register is reserved for S3 testing of the internal clock synthesizer.

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

RAMDAC/CLKSYN Control Register (SR18)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 18H

7	6	5	4	3	2	1	0
CLKx 2	CLUT WR	DAC PD	TST BLUE	TST GRN	TST RED	TST RST	TST EN

Bit 0 TST EN - Enable test counter
0 = RAMDAC test counter disabled
1 = RAMDAC test counter enabled

This bit is used for S3 test purposes only.

Bit 1 TST RST - Reset test counter
0 = No effect
1 = Reset the RAMDAC test counter

This bit is used for S3 test purposes only.

Bit 2 TST RED - Test red data
0 = No effect
1 = Place red data on internal data bus

This bit is used for S3 test purposes only.

Bit 3 TST GRN - Test green data
0 = No effect
1 = Place green data on internal data bus

This bit is used for S3 test purposes only.

Bit 4 TST BLUE - Test blue data
0 = No effect
1 = Place blue data on internal data bus

This bit is used for S3 test purposes only.

Bit 5 DAC PD - RAMDAC power-down
0 = RAMDAC powered up unless SR20_0 = 1 and SR31_5 = 0
1 = RAMDAC powered down

When the RAMDAC is powered down, the RAMDAC memory retains its data. Software should set this bit when only a flat panel (no CRT/TV) is being driven.

Bit 6 LUT WR - CLUT write cycle control
0 = 2 DCLK CLUT write cycle (default)
1 = 1 DCLK CLUT write cycle

Bit 7 CLKx2 - Enable clock doubled mode
0 = RAMDAC clock doubled mode (0001) disabled
1 = RAMDAC clock doubled mode (0001) enabled

This bit must be set to 1 when mode 0001 is specified in bits 7-4 of CR67 or SRC. Either bit 4 or bit 6 of SR15 must also be set to 1.

Extended Sequencer 1A Register (SR1A)

Read/Write Address: 3C5H, Index 1AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
DACP	R	PC15	PC3	R	R	R	R

Bits 3-0 Reserved

Bit 4 PC3 - Pin C3 Select
0 = Pin C3 is $\overline{\text{GOP0}}$
1 = Pin C3 is $\overline{\text{STWR}}$

Bit 5 PC15 - Pin C15 Select
0 = Pin C15 is $\overline{\text{ROMEN}}$
1 = Pin C15 is FPPOL

Bit 6 Reserved

Bit 7 DACP - DAC Power
0 = RAMDAC and CLUTs powered with 3.3V
1 = RAMDAC and CLUTs powered with 5V

This bit overrides the automatic settings indicated by SR1B_0.

Extended Sequencer 1B Register (SR1B)

See Bit Descriptions Address: 3C5H, Index 1BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
FDCK	R	R	R	R	R	R	DP

Bit 0 DP - DAC Power (Read Only)
0 = The RAMDAC and CLUTs are powered with 5V
1 = The RAMDAC and CLUTs are powered with 3.3V

The internal RAMDAC autosenses its voltage input and generates a signal that is latched in this register bit. This can be read by the BIOS, which can then force a specific voltage by programming SR1A_7.

Bits 6–1 Reserved (Read/Write)

Bit 7 FDCK - Force DCLK Source
0 = DCLK PLL parameter source is specified by 3C2_3-2
1 = DCLK PLL parameter source is forced to SR12 and SR13 regardless of the setting of 3C2_3-2

Extended Sequencer 1C Register (SR1C)

Read/Write Address: 3C5H, Index 1CH
Power-On Default: 00H

All non-reserved bits in this register should be programmed to 1 by the BIOS during reset.

7	6	5	4	3	2	1	0
LSU	LSB	LP	TVSU	TVSB	TVP	R	R

Bits 1-0 Reserved

Bit 2 TVP - TV Encoder Powerdown Enable
0 = TV Encoder clock is not turned off when TV Encoder is disabled
1 = TV Encoder clock is turned off when TV Encoder is disabled

Bit 3 TVSB - TV Encoder Standby Enable
0 = TV Encoder clock is not turned off in Standby mode
1 = TV Encoder clock is turned off in Standby mode

Bit 4 TVSU - TV Encoder Suspend Enable
0 = TV Encoder clock is not turned off in Suspend mode
1 = TV Encoder clock is turned off in Suspend mode

Bit 5 LP - LPB Powerdown Enable
0 = LPB LCLK is not turned off when LPB is disabled
1 = LPB LCLK is turned off when LPB is disabled

Bit 6 LSB - LPB Standby Enable
0 = LPB LCLK is not turned off in Standby mode
1 = LPB LCLK is turned off in Standby mode

Bit 7 LSU - LPB Suspend Enable
0 = LPB LCLK is not turned off in Suspend mode
1 = LPB LCLK is turned off in Suspend mode

Extended Sequencer 1D Register (SR1D)

Read/Write Address: 3C5H, Index 1DH
Power-On Default: 00H

This register controls the powerdown for the Stream Processor (SP) dot clock (DCLK). The SP DCLK consists of two branches: branch 1 of the SP DCLK is used on stream processor logic which can be turned off when the SP is disabled (CR67_3-2 = 00), while branch 2 of the SP DCLK is used on SP logic that cannot be turned off when the SP is disabled.

All non-reserved bits in this register should be programmed to 1 by the BIOS during reset.

7	6	5	4	3	2	1	0
SSU2	SSB2	SSU1	SSB1	SP1	R	R	R

Bits 2-0 Reserved

Bit 3 SP1 - Stream Processor Powerdown Enable 1
0 = SP DCLK branch 1 is not turned off when SP is disabled
1 = SP DCLK branch 1 is turned off when SP is disabled

Bit 4 SSB1 - Stream Processor Standby Enable 1
0 = SP DCLK branch 1 is not turned off in Standby mode
1 = SP DCLK branch 1 is turned off in Standby mode

Bit 5 SSU1 - Stream Processor Suspend Enable 1
0 = SP DCLK branch 1 is not turned off in Suspend mode
1 = SP DCLK branch 1 is turned off in Suspend mode

Bit 6 SSB2 - Stream Processor Standby Enable 2
0 = SP DCLK branch 2 is not turned off in Standby mode
1 = SP DCLK branch 2 is turned off in Standby mode

Bit 7 SSU2 - Stream Processor Suspend Enable 2
0 = SP DCLK branch 2 is not turned off in Suspend mode
1 = SP DCLK branch 2 is turned off in Suspend mode

Power Management 5 Register (SR1E)

Read/Write Address: 3C5H, Index 1EH
Power-On Default: 00H

All non-reserved bits in this register should be programmed to 1 by the BIOS during reset.

7	6	5	4	3	2	1	0
BSE	R	R	C2SU	C2SB	C2PD	R	C1PD

Bit 0 C1PD - Controller 1 Powerdown Enable
0 = Controller 1 DCLK is not turned off when Controller 1 is not enabled
1 = Controller 1 DCLK is turned off when Controller 1 is not enabled

Controller 1 is enabled when SR31_1 = 0 or when SR31_2 = 0 and SR31_4 = 1)

Bit 1 Reserved

Bit 2 C2PD - Controller 2 Power Down Enable
0 = Controller 2 DCLK is not turned off when Controller 2 is not enabled
1 = Controller 2 DCLK is turned off when Controller 2 is not enabled

Controller 2 is enabled when SR31_1 = 1 or when SR31_2 = 1 and SR31_4 = 1)

Bit 3 C2SB - Controller 2 Power Down During Standby
0 = Controller 2 is not powered down during Standby
1 = Controller 2 is powered down during Standby

Bit 4 C2SU - Controller 2 Power Down During Suspend
0 = Controller 2 is not powered down during Suspend
1 = Controller 2 is powered down during Suspend

Bits 6-5 Reserved

Bit 7 BSE - Bus Interface Suspend Enable
0 = Bus interface SCLK is not turned off dursing Suspend
1 = Bus interface SCLK is turned off during Suspend

Extended Sequencer 1F Register (SR1F)

Read/Write Address: 3C5H, Index 1FH
Power-On Default: 00H

All non-reserved bits in this register should be programmed to 1 by the BIOS during reset.

7	6	5	4	3	2	1	0
PFIE	R	MSE	CSPE	LPBE	BSE	DMSE	GESE

Bit 0 GESE - Graphics Engine Suspend Enable
0 = GE MCLK is not turned off in Suspend mode
1 = GE MCLK is turned off in Suspend mode

Bit 1 DMSE - Data Manager Suspend Enable
0 = DM MCLK is not turned off in Suspend mode
1 = DM MCLK is turned off in Suspend mode

Bit 2 BSE - Bus Interface Unit MCLK Suspend Enable
0 = MCLK branch going to bus interface is not turned off in Suspend mode
1 = MCLK branch going to bus interface is turned off in Suspend mode

Bit 3 LPBE - LPB MCLK Suspend Enable
0 = MCLK branch going to LPB is not turned off in Suspend mode
1 = MCLK branch going to LPB is turned off in Suspend mode

Bit 4 CSPE - Controller 1/Controller 2/Streams Processor MCLK Suspend Enable
0 = MCLK going to Controller 1, Controller 2, and the Streams Processor is not turned off in Suspend mode
1 = MCLK going to Controller 1, Controller 2, and the Stream Processor is turned off in Suspend mode

Bit 5 MSE - MCLK Suspend Enable
0 = All branches of MCLK are not turned off in Suspend mode regardless of the settings of the other non-reserved bits of this register
1 = All branches of MCLK can be turned off in Suspend mode depending on the settings of the other non-reserved bits of this register

Bit 6 Reserved

Bit 7 FPIE - Flat Panel Interface MCLK Suspend Enable
0 = MCLK branch going to the Flat Panel Interface is not turned off in Suspend mode
1 = MCLK branch going to the Flat Panel Interface is turned off in Suspend mode

*

Extended Sequencer 20 Register (SR20)

Read/Write Address: 3C5H, Index 20H
Power-On Default: 00H

7	6	5	4	3	2	1	0
PSE	R	R	MPSE	DPSE	DSUE	DSBE	R

Bit 0 Reserved

Bit 1 DSBE - DAC Standby Enable
0 = DAC is not turned off in Standby mode
1 = DAC is turned off in Standby mode

Bit 2 DSUE - DAC Suspend Enable
0 = DAC is not turned off in Suspend mode
1 = DAC is turned off in Suspend mode

Bit 3 DPSE - DCLK PLL Suspend Enable
0 = DCLK PLL is not turned off in Suspend mode
1 = DCLK PLL is turned off in Suspend mode

This bit is OR-ed with SR14_0.

Bit 4 MPSE - MCLK PLL Suspend Enable
0 = MCLK PLL is not turned off in Suspend mode
1 = MCLK PLL is turned off in Suspend mode

This bit is OR-ed with SR14_0.

Bits 6-5 Reserved

Bit 7 PSE - Pads Suspend Enable
0 = Suspend mode has no effect on pads
1 = Suspend mode puts the pads in Suspend configuration

Extended Sequencer 21 Register (SR21)

Read/Write Address: 3C5H, Index 21H
Power-On Default: 00H

7	6	5	4	3	2	1	0
C2LE	C2LS	C2LP	LUT2	C1LE	C1LS	MS	LUT1

Bit 0 LUT1 - Disable CLUT1
0 = CLUT1 enabled
1 = CLUT1 disabled (powered down)

Bit 1 MS - Disable Monitor Sense
0 = Monitor sense circuit enabled
1 = Monitor sense circuit disabled (powered down)

Bit 2 C1LS - Controller 1 CLUT Standby Enable
0 = Controller 1 CLUT is not powered down in Standby mode
1 = Controller 1 CLUT is powered down in Standby mode

The BIOS must program this bit to 1 after each reset.

Bit 3 C1LE - Controller 1 CLUT Standby Enable
0 = Controller 1 CLUT is not powered down in Suspend mode
1 = Controller 1 CLUT is powered down in Suspend mode

The BIOS must program this bit to 1 after each reset.

Bit 4 LUT2 - Disable CLUT2
0 = CLUT2 enabled
1 = CLUT2 disabled (powered down)

Bit 5 C2LP - Controller 2 CLUT Powerdown Enable
0 = Controller 2 CLUT is not powered down when Controller 2 is not enabled
1 = Controller 2 CLUT is powered down when Controller 2 is not enabled

The BIOS must program this bit to 1 after each reset.

Bit 6 C2LS - Controller 2 CLUT Standby Enable
0 = Controller 2 CLUT is not powered down in Standby mode
1 = Controller 2 CLUT is powered down in Standby mode

The BIOS must program this bit to 1 after each reset.

Bit 7 C2LE - Controller 2 CLUT Standby Enable
0 = Controller 2 CLUT is not powered down in Suspend mode
1 = Controller 2 CLUT is powered down in Suspend mode

The BIOS must program this bit to 1 after each reset.

VGA DCLK0 Value Low Register (SR22)

Read/Write Address: 3C5H, Index 22H
Power-On Default: See description below

SR22 and SR23 are selected as the source of the DCLK PLL parameter values when 3C2H_3-2 = 00b. The power-on default value for this register in conjunction with the power-on default value for SR23 generate a DCLK value of 25.175 MHz. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0.

7	6	5	4	3	2	1	0
PLL R VALUE		PLL N-DIVIDER VALUE					

Bits 5-0 N-DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-31) divider used to scale the input to the DCLK PLL. See Section 8 for a detailed explanation.

Bits 7-6 PLL R VALUE
These bits contain the binary equivalent of the integer (1, 2, 4, 8) range value used to scale the output of the DCLK PLL. See Section 8 for a detailed explanation.

VGA DCLK0 Value High Register (SR23)

Read/Write Address: 3C5H, Index 23H
Power-On Default: See description below.

SR22 and SR23 are selected as the source of the DCLK PLL parameter values when 3C2H_3-2 = 00b. The power-on default value for this register in conjunction with the power-on default value for SR22 generate a DCLK value of 25.175 MHz. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0.

7	6	5	4	3	2	1	0
PLL M-DIVIDER VALUE							

Bits 7-0 PLL M- DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-127) divider used in the feedback loop of the DCLK PLL. See Section 8 for a detailed explanation.

VGA DCLK0 Value Low Register (SR24)

Read/Write Address: 3C5H, Index 24H
Power-On Default: See description below

SR24 and SR25 are selected as the source of the DCLK PLL parameter values when 3C2H_3-2 = 01b. The power-on default value for this register in conjunction with the power-on default value for SR25 generate a DCLK value of 28.322 MHz. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0.

7	6	5	4	3	2	1	0
PLL R VALUE		PLL N-DIVIDER VALUE					

Bits 5-0 N-DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-31) divider used to scale the input to the DCLK PLL. See Section 8 for a detailed explanation.

Bits 7-6 PLL R VALUE
These bits contain the binary equivalent of the integer (1, 2, 4, 8) range value used to scale the output of the DCLK PLL. See Section 8 for a detailed explanation.

VGA DCLK0 Value High Register (SR25)

Read/Write Address: 3C5H, Index 25H
Power-On Default: See description below.

SR24 and SR25 are selected as the source of the DCLK PLL parameter values when 3C2H_3-2 = 01b. The power-on default value for this register in conjunction with the power-on default value for SR24 generate a DCLK value of 28.322 MHz. Loading of new values occurs when either SR15_1 is set to 1 or SR15_5 is programmed to 1 and then 0.

7	6	5	4	3	2	1	0
PLL M-DIVIDER VALUE							

Bits 7-0 PLL M- DIVIDER VALUE
These bits contain the binary equivalent of the integer (1-127) divider used in the feedback loop of the DCLK PLL. See Section 8 for a detailed explanation.

Paired Register Read/Write Select Register (SR26)

Read/Write Address: 3C5H, Index 26H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	DC1W	EC2W	DR	DSR

Bit 0 DSR - Disable Selected Controller 1 Reads
0 = Data for all paired register reads comes from the controller 1 registers
1 = Reads of CR0-CR7, CR10-12, CR15-16 from controller 1 are disabled. Read data is provided from the corresponding paired registers in controller 2

This bit is only effective if bit 1 of this register is cleared to 0.

Bit 1 DR - Disable Controller 1 Reads
0 = Data for all paired register reads comes from the controller 1 registers
1 = Reads of all paired controller 1 registers are disabled. Read data is provided from the corresponding paired registers in controller 2

Setting this bit to 1 overrides the setting of bit 0 of this register.

Bit 2 EC2W - Enable Controller 2 Writes
0 = Writes to controller 2 registers are disabled
1 = Writes to controller 2 registers are enabled.

Note that by default, writes to controller 1 registers (controlled by bit 3 of this register) are enabled and writes to controller 2 registers are disabled. Software can selectively write to only controller 1 registers, only controller 2 registers or to both with one write (mirroring) by enabling writes to both.

Bit 3 DC1W - Disable Controller 1 Writes
0 = Writes to controller 1 registers are enabled
1 = Writes to controller 1 registers are disabled

See the note for bit 2 of this register.

Note: If this bit is set to 1, any subsequent writes to any SR register will be directed to SR26 (the index is locked). Therefore, no writes to SR registers (except SR26) should be made if this bit is set to 1.

Bits 7-4 Reserved

MCLK Control Register (SR27)

Read/Write Address: 3C5H, Index 27H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	IMCLK MUX2		IMCLK MUX1	

Bits 1-0 IMCLK MUX1
00 = IMCLK = MCLK
01 = IMCLK = DCLK
10 = IMCLK = MCLK
11 = IMCLK = SCLK

If CR37_3 = 0, the XIN pin becomes the EDCLK (external DCLK) input and the LPBEN pin becomes the EMCLK (external MCLK) input. SR14_6 selects whether the external MCLK or PLL-generated MCLK is used. SR14_7 selects whether the external DCLK or PLL-generated DCLK is used.

Note: These bits should not be changed at the same time as bits 3-2 of this register (at least 10 SCLKs must intervene).

Bits 3-2 IMCLK MUX2
00 = MCLK = IMCLK
01 = MCLK = IMCLK/2
10 = MCLK = IMCLK/3
11 = MCLK = IMCLK/4

Note: These bits should not be changed at the same time as bits 1-0 of this register (at least 10 SCLKs must intervene)..

Bits 7-4 Reserved

DCLK Control Register (SR28)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 28H

7	6	5	4	3	2	1	0
IDCLKB MUX2		IDCLKB MUX1		IDCLKA MUX2		IDCLKA MUX1	

Bits 1-0 IDCLKA MUX1
00 = IDCLKA = DCLK
01 = IDCLKA = DCLK
10 = IDCLKA = MCLK
11 = IDCLKA = SCLK

If CR37_3 = 0, the XIN pin becomes the EDCLK (external DCLK) input and the LPBEN pin becomes the EMCLK (external MCLK) input. SR14_7 selects whether the external DCLK or PLL-generated DCLK is used. SR14_6 selects whether the external MCLK or PLL-generated MCLK is used.

Note: These bits should not be changed at the same time as bits 3-2 of this register (at least 10 SCLKs must intervene).

Bits 3-2 IDCLKA MUX2
00 = DCLK1 = IDCLKA
01 = DCLK1 = IDCLKA/2
10 = DCLK1 = IDCLKA/3
11 = DCLK1 = IDCLKA/4

DCLK1 is the pixel clock for the controller 1 path (includes the Streams Processor).

Note: These bits should not be changed at the same time as bits 1-0 of this register (at least 10 SCLKs must intervene).

Bits 5-4 IDCLKB MUX1
00 = IDCLKB = DCLK
01 = IDCLKB = DCLK
10 = IDCLKB = MCLK
11 = IDCLKB = SCLK

If CR37_3 = 0, the XIN pin becomes the EDCLK (external DCLK) input and the LPBEN pin becomes the EMCLK (external MCLK) input. SR14_7 selects whether the external DCLK or PLL-generated DCLK is used. SR14_6 selects whether the external MCLK or PLL-generated MCLK is used.

Note: These bits should not be changed at the same time as bits 7-6 of this register (at least 10 SCLKs must intervene).

Bits 7-6 IDCLKB MUX2
00 = DCLK2 = IDCLKB
01 = DCLK2 = IDCLKB/2
10 = DCLK2 = IDCLKB/3
11 = DCLK2 = IDCLKB/4

DCLK2 is the pixel clock for the controller 2 path (no Streams Processor).

Note: These bits should not be changed at the same time as bits 5-4 of this register (at least 10 SCLKs must intervene).

FIFO Threshold Register (SR29)

Read/Write Address: 3C5H, Index 29H
Power-On Default: 00H

7	6	5	4	3	2	1	0
CONT2 FIFO		STN READ FIFO				STN W FIFO	

Bits 1-0 STN W FIFO - STN Write FIFO Threshold
00 = 2 slots filled
01 = 4 slots filled
10 = 8 slots filled
11 = 12 slots filled

When this many slots are filled in this 16-slot FIFO, a request is generated to the memory manager to begin emptying the FIFO. This is used to maximize the efficiency of the the memory interface.

Bits 5-2 STN READ FIFO - STN Read FIFO Threshold

Value = Number of STN read FIFO slots

When the FIFO empties down to this value, a high priority memory access request is generated.

Bits 7-6 CONT2 FIFO - Controller 2 FIFO Threshold
00 = 2 slots filled
01 = 4 slots filled
10 = 8 slots filled
11 = 12 slots filled

When the FIFO empties down to this value, a high priority memory access request is generated.

18.2 FLAT PANEL REGISTERS

Architecture Configuration Register (SR30)

Read/Write Address: 3C5H, Index 30H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	PST

Bit 0 PCT - Panel Scan Type
0 = Dual-scan STN panel
1 = TFT or single-scan STN panel

Bits 7-1 Reserved

Flat Panel Display Mode Register (SR31)

Read/Write Address: 3C5H, Index 31H
Power-On Default: 00H

7	6	5	4	3	2	1	0
CD	ID	R	FPD	CT	DACS	FPS	CTM

Bit 0 CTM - CRT Test Mode
0 = Standard flat panel operation
1 = CRT RGB data output on FP[23:0]

This bit is used for test purposes. It allows direct viewing of either CRT or TV encoder data before it reaches the CLUT/RAMDAC.

Bit 1 FPS - Flat Panel Data Source
0 = Controller 1 is flat panel source (Streams Processor available)
1 = Controller 2 is flat panel source (Streams Processor not available)

This bit is valid only if SR31_0 = 0.

Bit 2 DACS - DAC Source Select
0 = Controller 1 is DAC source (Streams Processor available)
1 = Controller 2 is DAC source (Streams Processor not available)

If TV mode is selected (CR3D_0 = 1), controller 1 is automatically selected as the DAC source.

Bit 3 BLUT - Bypass CLUT Test Mode
0 = Normal operation
1 = Force bypass of Controller 1 and Controller 2 CLUTs in all modes

This bit is for test purposes only.

Bit 4 FPE - Flat Panel Display Enable
0 = Disable flat panel display
1 = Enable flat panel display

Setting this bit to 1 triggers a panel power-on sequence and turns on the clocks to the flat panel logic. Clearing this bit to 0 triggers a panel power-down sequence and disables the clocks to the flat panel logic.

Bit 5 Reserved

Bit 6 ID - Icon Destination Select
0 = Hardware icon controlled by controller 1
1 = Hardware icon controlled by controller 2

The hardware icon is available in any video mode. This bit determines on which screen the icon will appear in dual image mode (both controllers being used).

Bit 7 CD - Cursor Destination Select
0 = Hardware cursor controlled by controller 1
1 = Hardware cursor controlled by controller 2

The hardware cursor is only available in Enhanced mode (not VGA). This bit determines on which screen the cursor will appear in dual display mode (both controllers being used).

Flat Panel Polarity Control Register (SR32)

Read/Write Address: 3C5H, Index 32H
Power-On Default: 00H

7	6	5	4	3	2	1	0
VSP	HSP	DEP	FPDP	R	CVSP	CHSP	MIT

Bit 0 MIT - Memory Interface Tri-state
0 = No effect
1 = Tri-state all memory interface signals

Bit 1 CHSP - CRT HSYNC Polarity During Simultaneous Display
0 = HSYNC polarity is active high
1 = HSYNC polarity is active low

This bit controls HSYNC polarity (instead of 3C2H_6 Write Only) when simultaneous display is used (SR31_4 = 1 AND SR31_1 = SR31_2).

Bit 2 CVSP - CRT VSYNC Polarity During Simultaneous Display
0 = VSYNC polarity is active high
1 = VSYNC polarity is active low

This bit controls VSYNC polarity (instead of 3C2H_7 Write Only) when simultaneous display is used (SR31_4 = 1 AND SR31_1 = SR31_2).

Bit 3 Reserved

Bit 4 FPDP - Flat Panel Data Polarity
0 = Active high
1 = Active low

Bit 5 DEP - FPDE Polarity
0 = Active high
1 = Active low

Bit 6 HSP - FPHSYNC Polarity
0 = Active high
1 = Active low

For STN panels, this is the LP signal.

Bit 7 VSP - FPVSYNC Polarity
0 = Active high
1 = Active low

For STN panels, this is the FLM signal.

Flat Panel AC Modulation Register (SR34)

Read/Write Address: 3C5H, Index 34H
Power-On Default: 00H

This register only applies to STN panels that require a MOD input.

7	6	5	4	3	2	1	0
ME	MODULATION PERIOD						

Bits 6-0 MODULATION PERIOD

Value = (width of MOD pulse in clock period units) - 1

The clock units (line or frame) are selected via SR35_4.

Bit 7 ME - Modulation Enable
0 = Pin B15 is FPDE
1 = Enable output of MOD signal on pin B15

Flat Panel Modulation Clock Select Register (SR35)

Read/Write Address: 3C5H, Index 35H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	MODC	R	R	R	R

Bits 3-0 Reserved

Bit 4 MODC - MOD Clock Select
0 = Line clock
1 = Frame clock

Bits 7-5 Reserved

Flat Panel Dither Control Register (SR36)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 36H

7	6	5	4	3	2	1	0
DTR CON		DTR BASE COLOR			DTR BIT SELECT		

Bit 0 DBS - Dither Bit Select
0 = 2 bits selected (2x2 dither pattern)
1 = 4 bits selected (4x4 dither pattern)

Bits 2-1 Reserved

Bits 5-3 DTR BASE COLOR
000 = 8 bits selected (no dithering)
001 = Reserved
010 = Reserved
011 = 3 bits selected
100 = 4 bits selected
101 = 5 bits selected
110 = 6 bits selected
111 = Reserved

Bits 7-6 DTR CON - Dither Control
00 = Dithering disabled
01 = Dithering in all modes
10 = Dither in graphics modes (not text)
11 = Dither in graphics modes with 8 bpp or more color

Flat Panel FRC Weight Select RAM Pointer Register (SR37)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 37H

7	6	5	4	3	2	1	0
R	R	R	R	WEIGHT SELECT POINTER			

Bits 3-0 WEIGHT SELECT POINTER

Value = offset from the base address of the weight decoding RAM

Bits 7-4 Reserved

Flat Panel FRC Weight Select RAM Data Register (SR38)

Read/Write Address: 3C5H, Index 38H
Power-On Default: 00H

7	6	5	4	3	2	1	0
WEIGHT SELECT DATA							

Bits 7-0 WEIGHT SELECT DATA

The actual value will be supplied by S3 for specific panels.

Flat Panel FRC Control Register (SR39)

Read/Write Address: 3C5H, Index 39H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	FRC GRAY		R	PANEL TYPE	

Bit 1-0 PANEL TYPE
00 = TFT panel
01 = Reserved
10 = STN panel. This setting enables FRC operation.
11 = Reserved

Bit 2 Reserved

Bits 4-3 FRC GRAY - Frame Rate Control Gray Level Select
00 = 16 levels
01 = 8 levels
10 = Reserved
11 = Reserved

Bit 7-5 Reserved

Flat Panel FRC Tuning 1 Register (SR3A)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 3AH

7	6	5	4	3	2	1	0
TUNING DATA 15-8							

The actual value will be supplied by S3 for specific panels. This is the Most Significant Byte of the tuning data.

Flat Panel FRC Tuning 2 Register (SR3B)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 3BH

7	6	5	4	3	2	1	0
TUNING DATA 7-0							

The actual value will be supplied by S3 for specific panels. This is the Least Significant Byte of the tuning value.

Flat Panel FRC Tuning 3 Register (SR3C)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 3CH

7	6	5	4	3	2	1	0
R	R	R	R	R	STN	TUNING 3	

Bits 1-0 TUNING 3

The actual value will be supplied by S3 for specific panels.

Bit 2 STM - STN Test Mode
0 = Normal operation
1 = STN Test Mode

This test mode is reserved for factory testing.

Bits 7-3 Reserved

Flat Panel Configuration Register (SR3D)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 3DH

7	6	5	4	3	2	1	0
SCDS	FPDS	SCS	LPS	CFGS	FP DATA FORMAT		

Bits 2-0 FP DATA FORMAT
000 = 16-bit STN; 1 pixel/clock TFT (9-, 12-, 15- or 18-bit)
001 = 8-bit STN; 1 pixel/clock TFT (24-bit)
010 = 24-bit STN; 2 pixels/clock TFT (2x9-bit, 2x12-bit, 2x15, 2x18-bit)

All other values are reserved. The STN definition applies if SR39_1-0 = 10b and the TFT definition applies if SR39_1-0 = 00b.

Bit 3 CFGS - Pin Configuration Select for Flat Panel Data Signals
0 = Illegal value
1 = Pin configuration shown in Tables 11-1 and 11-2.

Note: This bit must be programmed to 1.

Bit 4 LPS - LP Stop (STN panels only)
0 = LP and FPSCLK enabled during vertical blank
1 = LP and FPSCLK disabled during vertical blank

Bit 5 SCS - Shift Clock Stop (STN panels only)
0 = FPSCLK enabled during the first line of vertical blanking
1 = FPSCLK disabled during the first line of vertical blanking

This bit is valid only if SR3D_4 = 0.

Bit 6 FPDS - Flat Panel Data Drive Strength
0 = Drive strength is 6 mA at 3.3V or 8 mA at 5V
1 = Drive strength is 12 mA at 3.3V or 16 mA at 5V

This bit affects FPD[23:0], PFDE and FPPOL. FPSCLK drive strength is controlled by SR3D_7. This bit must be = 0 for 36-bit XGA panels.

Bit 7 SCDS- Shift Clock Drive Strength
0 = FPSCLK drive strength is 6 mA at 3.3V or 8 mA at 5V
1 = FPSCLK drive strength is 12 mA at 3.3V or 16 mA at 5V

Flat Panel Pin Configuration Register (SR40)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 40H

7	6	5	4	3	2	1	0
POL	SCS	SCM	FPOFF	FPSCLK DELAY			R

Bit 0 Reserved

Bit 3-1 FPSCLK DELAY

Value = number of nanoseconds to delay FPSCLK

Bit 4 FPOFF - Flat Panel Data and Control Signals Low
0 = Normal operation for flat panel outputs
1 = Force all flat panel data and control signals to logic 0

Bit 5 SCM - Shift Clock Mask
0 = Allow the shift clock (FPSCLK) output to toggle during the non-display interval
1 = Force the shift clock (FPSCLK) output low during the non-display interval

The proper setting of this bit is panel-specific.

Bit 6 SCS - Shift Clock Select (TFT only)
0 = Pixels are clocked on the falling edge of FPSCLK
1 = Pixels are clocked on both the rising and falling edge of FPSCLK

Not all TFT panels provide the double-edge clocking mode.

Bit 7 POL - Polarity Enable (TFT only)
0 = FPPOL pin output disabled
1 = FPPOL pin output enabled

Polarity is available for 18- and 24-bit 1 pixel/clock modes and 2x18-bit 2 pixels/clock mode.

Flat Panel Power Sequence Control Register (SR41)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 41H

7	6	5	4	3	2	1	0
STR		R	R	PUP	PDWN	R	R

Bits 1-0 Reserved

Bit 2 PDWN - Power Down Phase
0 = FPVEE low to FP signals inactive and FP signals inactive to FPVDD low = 32 ms
1 = FPVEE low to FP signals inactive and FP signals inactive to FPVDD low = 128 ms

Bit 3 PUP - Power Up Phase
0 = FPVDD high to FP signals active and FP signals active to FPVEE high = 32 ms
1 = FPVDD high to FP signals active and FP signals active to FPVEE high = 128 ms

Bits 5-4 Reserved

Bits 7-6 STR - Standby Timer Resolution
00 = 1 second
01 = 1 minute
10 = 1 msec
11 = 64 msec

Flat Panel Power Management Control Register (SR42)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 42H

7	6	5	4	3	2	1	0
SDB TIMER		SSTB	HSTB	R	R	SSUS	R

Bit 0 Reserved

Bit 1 SSUS - Software Suspend
0 = Software suspend disabled
1 = Software suspend enabled

Bits 3-2 Reserved

Bit 4 HSTB - Hardware Standby
0 = Hardware standby disabled
1 = Hardware standby enabled

Bit 5 SSTB - Software Standby
0 = Software standby disabled
1 = Software standby enabled

The BIOS must set this bit to 1 after a power-on reset, program the desired mode and then clear this bit to 0 to initiate a power-up sequence.

Bits 7-6 SDB TIMER - Suspend Debounce Timer
00 = 62.5 µs
01 = 2 seconds
1x = Immediate (used for testing)

Flat Panel Standby Control Register (SR43)

Read/Write Address: 3C5H, Index 43H
Power-On Default: 01H

7	6	5	4	3	2	1	0
R	ACT	STANDBY TIMEOUT VALUE					

Bits 5-0 STANDBY TIMEOUT VALUE

Value = number of units to count before Standby mode is entered

The type of unit (second or minute) is selected via bit 7 of this register. Note that the default timeout value is 1 second.

Bit 6 ACT - Activity Enable
0 = Normal standby mode
1 = Activity function enabled

Bit 7 Reserved

Flat Panel Power Management Register (SR44)

Read/Write Address: 3C5H, Index 44H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	STBP	R=0	R=0	R=0	R=0

Bits 3-0 Reserved = 0000b

Bit 4 STBP - Standby Pin
0 = To cause entry to Standby, the STANDBY pin must go high (which starts the Standby counter) and remain high until the idle power down state is reached after the Standby counter expires. Standby is exited when the STANDBY pin goes low. Hardware Standby must be enabled (SR42_4 = 1)
1 = The Standby counter begins counting when hardware Standby is enabled (SR42_4 = 1). Each rising edge of the STANDBY pin resets the counter (if not in Standby) or takes the system out of Standby. When the system reaches the idle power up state after exiting Standby, the Standby counter begins recounting.

Bits 7-5 Reserved

Flat Panel PLL Power Management Register (SR45)

Read/Write Address: 3C5H, Index 45H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	REFRESH		PLL WAIT	

Bits 1-0 PLL WAIT
00 = 2 ms
01 = 4 ms
10 = 8 ms
11 = 16 ms

This is the time from entering Suspend to powering-down of the PLLs and from leaving Suspend to powering-up of the PLLs.

Bits 3-2 REFRESH
00 = Normal (8 ms)
01 = 16 ms slow refresh
10 = 64 ms slow refresh
11 = Self-refresh DRAM

Selections other than normal are used during Suspend. The DRAM must be able to support the selected refresh type.

Bits 7-4 Reserved

Flat Panel Power Management Status Register (SR46)

Read Only
Power-On Default: 00H

Address: 3C5H, Index 46H

7	6	5	4	3	2	1	0
IDPUP	IDPDN	STBS	R	R	R	R	R

Bits 4-0 Reserved

Bit 5 STBS - Standby Status
0 = Not in Standby mode
1 = In Standby mode

Bit 6 IDPDN - Idle Power Down State
0 = Not in idle power down state
1 = In idle power down state

This is the state immediately after a panel power down sequence.

Bit 7 IDPUP - Idle Power Up State
0 = Not in idle power up state
1 = In idle power up state

This is the state immediately after a panel power up sequence.

CLUT Control Register (SR47)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 47H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	CLUT SELECT	

Bits 1-0 CLUT SELECT
00 = CLUT1 and CLUT2 enabled and mirrored for CPU writes
01 = CLUT1 only for CPU writes and reads mapped at 3C7H, 3C8H, 3C9H
10 = CLUT2 only for CPU writes and reads mapped at 3C7H, 3C8H, 3C9H
11 = Reserved

Bits 7-2 Reserved

Icon Mode Register (SR48)

Read/Write Address: 3C5H, Index 48H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	ICON MAP			2Y	2X	IMOD	IEN

Bit 0 IEN - Icon Enable
0 = Hardware icon disabled
1 = Hardware icon enabled

Bit 1 IMOD - Icon Mode
0 = 4 opaque colors
1 = 3 opaque colors and 1 transparent color

When this bit is cleared to 0, the color of each icon pixel (2 bits/pixel) is defined as:
00 = Color 0
01 = Color 1
10 = Color 2
11 = Color 3

When this bit is set to 1, the color of each icon pixel (2 bits/pixel) is defined as:
00 = Color 0
01 = Color 1
10 = Color 2
11 = Transparent (the current frame buffer pixel is not overwritten)

The hardware icon colors are defined in SR49.

Bit 2 2X - Double X
0 = Horizontal size is 64 pixels
1 = Horizontal size is 128 pixels

If this bit is set to 1, each pixel is duplicated in the horizontal direction.

Bit 3 2Y - Double Y
0 = Vertical size is 64 pixels
1 = Vertical size is 128 pixels

If this bit is set to 1, each pixel is duplicated in the vertical direction.

Bits 6-4 ICON MAP
000 = Select hardware icon map 0
001 = Select hardware icon map 1
010 = Select hardware icon map 2
011 = Select hardware icon map 3
100 = Select hardware icon map 4
101 = Select hardware icon map 5
110 = Select hardware icon map 6
111 = Select hardware icon map 7

The icon maps are located in contiguous memory starting at the location programmed in SR4E.

Bit 7 Reserved

Icon Color Stack Register (SR49)

Read/Write Address: 3C5H, Index 49H
Power-On Default: Undefined

This register allows four 24 bits/pixel colors to be defined for the hardware icon. Twelve 8-bit indexed registers are stacked at this address. A read of SR48 resets the index to 0. Each read or write of this register increments the index by 1, so the entire content can be read/written via successive accesses. The colors used for the icon are selected via SR48_1. Colors data for color depths other than 24 bits/pixel use the appropriate number of low-order bits.

7	6	5	4	3	2	1	0
COLOR DATA							

Bits 7-0 COLOR DATA

Index 0 = Color 0 low (blue) byte
Index 1 = Color 0 middle (green) byte
Index 2 = Color 0 high (red) byte
Index 3 = Color 1 low (blue) byte
Index 4 = Color 1 middle (green) byte
Index 5 = Color 1 high (red) byte
Index 6 = Color 2 low (blue) byte
Index 7 = Color 2 middle (green) byte
Index 8 = Color 2 high (red) byte
Index 9 = Color 3 low (blue) byte
Index A = Color 3 middle (green) byte
Index B = Color 3 high (red) byte

Icon X Position High Register (SR4A)

Read/Write Address: 3C5H, Index 4AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	R	R	X POSITION HIGH		

Bits 1-0 X POSITION HIGH

Value = High order 3 bits of the icon horizontal coordinate

The low order bits are found in SR4B.

Bits 7-2 Reserved

Icon X Position Low Register (SR4B)

Read/Write Address: 3C5H, Index 4BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
X POSITION LOW							

Bits 7-0 X POSITION LOW

Value = Low order 8 bits of the icon horizontal coordinate

The high order 3 bits are found in SR4A.

Icon Y Position High Register (SR4C)

Read/Write Address: 3C5H, Index 4CH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	R	R	Y POSITION HIGH		

Bits 1-0 Y POSITION HIGH

Value = High order 3 bits of the icon vertical coordinate

The low order bits are found in SR4D.

Bits 7-2 Reserved

Icon Y Position Low Register (SR4D)

Read/Write Address: 3C5H, Index 4DH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
Y POSITION LOW							

Bits 7-0 Y POSITION LOW

Value = Low order 8 bits of the icon vertical coordinate

The high order 3 bits are found in SR4C.

Icon Address Register (SR4E)

Read/Write Address: 3C5H, Index 4EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
ICON ADDRESS							

Bits 7-0 ICON ADDRESS

Value = Base address in the frame buffer for the hardware icon maps

The address is specified in 8K increments if the memory size is 2 MBytes or less and in 8K increments starting at the 2-MByte boundary if the memory size is 4 MBytes. The selection of a specific icon map is made via SR48_6-4.

Dual-Scan STN Data Address Register (SR4F)

Read/Write Address: 3C5H, Index 4FH
Power-On Default: 00H

7	6	5	4	3	2	1	0
DD-STN DATA ADDRESS ADJUSTMENT							

Bits 7-0 DD-STN DATA ADDRESS ADJUSTMENT

Value = Number of 8K units to reserve between the top of video memory and the start of the STN data area.

Dual-Scan STN Frame Buffer Size Low Register (SR50)

Read/Write Address: 3C5H, Index 50H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DD-STN FRAME BUFFER SIZE LOW							

Bits 7-0 DD-STN FRAME BUFFER SIZE LOW

Value = lower byte of the STN frame buffer size in quadwords

The STN frame buffer size in quadwords is calculated using the following equation:

Frame Buffer Size = Horizontal size (in quadwords) x 1/2 vertical size (in lines)

Horizontal Size = [(SR61+1) x 3 x 8/64] quadwords rounded up to the nearest integer. Note that the value programmed in SR61 is in 8-pixel characters and data in the frame buffer is 3 bits/pixel. An equivalent formula is:

Horizontal Size = horizontal resolution in pixels x 3/64 (rounded up).

1/2 Vertical Size = 1/2 [SR69 + 1] or:

1/2 Vertical Size = 1/2 vertical resolution in lines

Dual-Scan STN Frame Buffer Size High Register (SR51)

Read/Write Address: 3C5H, Index 51H
Power-On Default: 00H

7	6	5	4	3	2	1	0
DD-STN FRAME BUFFER SIZE HIGH							

Bits 7-0 DD-STN FRAME BUFFER SIZE HIGH

Value = upper byte of STN frame buffer size in quadwords

See SR50 for an explanation of how to determine the value to be programmed in this register.

Flat Panel PWM Register (SR52)

Read/Write Address: 3C5H, Index 52H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	PWM CLOCK DIVIDE			R	R	PSC	PWM

Bit 0 PWM - Pulse Width Modulation Enable
0 = PWM disabled
1 = PWM enabled

If the DRAM type is not 512Kx32 and this bit is set to 1, pin M17 acts as the PWM signal.

Bit 1 PSC - PWM Source Clock Select
0 = Generate PWM signal from the 14.31818 MHz reference clock
1 = Generate PWM signal from the PCI clock (SCLK)

Bits 3-2 Reserved

Bits 6-4 PWM CLOCK DIVIDE
000 = PWM source clock is not pre-divided
001 = PWM source clock is pre-divided by 1.5
010 = PWM source clock is pre-divided by 2
100 = PWM source clock is pre-divided by 3

All other values are reserved.

PWM clock frequency = PWM source clock/pre-divisor/256

The inversion of this is the PWM period used in the PWM duty cycle specification in SR53.

Bit 7 Reserved

Flat Panel PWM Duty Cycle Register (SR53)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 53H

7	6	5	4	3	2	1	0
PWM DUTY CYCLE							

Bits 7-0 PWM DUTY CYCLE

Value = 256 (x/p)

where x = high time of the PWM signal and p = period of the PWM signal, both in nanoseconds. The period is determined as explained for SR52_6-4. A programmed value of 00H causes the PWM signal to be DC low. A programmed value of FFH causes the PWM signal to be DC high.

Flat Panel Horizontal Compensation 1 Register (SR54)

Read/Write
Power-On Default: 00H

Address: 3C5H, Index 54H

7	6	5	4	3	2	1	0
FPLG	R	R	HCE	GRAPH EXP		TEXT EXP	

Bits 1-0 TEXT EXP - Text Mode Horizontal Expansion
00 = Horizontal expansion disabled
01 = Horizontal expansion enabled up to a maximum expansion factor of 1.25.
10 = Reserved
11 = Horizontal expansion enabled up to the horizontal panel size. For VGA panels, 9-dot text modes will be forced to 8-dot text modes

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 800 columns to limit the expansion and eliminate the undesirable visual effects.

Bits 3-2 GRAPH EXP - Graphics Mode Horizontal Expansion
00 = Horizontal expansion disabled
01 = Horizontal expansion enabled up to a maximum expansion factor of 1.25.
10 = Reserved
11 = Horizontal expansion enabled up to the horizontal panel size. For VGA panels, 9-dot text modes will be forced to 8-dot text modes

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 800 columns to limit the expansion and eliminate the undesirable visual effects.

Bit 4 HCE - Horizontal Centering Enable
0 = Horizontal centering disabled
1 = Horizontal centering enabled

Bits 6-5 Reserved

Bit 7 FPLG - Flat Panel Line Graphics Enable
0 = The ninth dot of a text character (SR1_0 = 0) is the same color as the background
1 = Special line graphics character codes enabled

This bit performs the same function as AR10_2 in CRT mode.

Flat Panel Horizontal Compensation 2 Register (SR55)

Read/Write Address: 3C5H, Index 55H
Power-On Default: 00H

The bits in this register control enabling of horizontal expansion in specific text/graphics modes. They are effective only if text mode horizontal expansion is enabled via SR54_1-0. Horizontal expansion for all other modes not controlled by these bits is controlled by SR54_3-0.

7	6	5	4	3	2	1	0
			1024C	800C	640C	80C	40C

Bit 0 40C - 40-character Text Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 40-character text mode
1 = Horizontal expansion enabled in 40-character text mode

This bit is effective only if text mode horizontal expansion is enabled via SR54_1-0.

Bit 1 80C - 80-character Text Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 80-character text mode
1 = Horizontal expansion enabled in 80-character text mode

This bit is effective only if text mode horizontal expansion is enabled via SR54_1-0.

Bit 2 640C - 640-column Graphics Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 640-column graphics mode
1 = Horizontal expansion enabled in 640-column graphics mode

This bit is effective only if graphics mode horizontal expansion is enabled via SR54_3-2.

Bit 3 800C - 800-column Graphics Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 800-column graphics mode
1 = Horizontal expansion enabled in 800-column graphics mode

This bit is effective only if graphics mode horizontal expansion is enabled via SR54_3-2.

Bit 4 1024C - 1024-column Graphics Mode Horizontal Expansion Enable
0 = Horizontal expansion disabled in 1024-column graphics mode
1 = Horizontal expansion enabled in 1024-column graphics mode

This bit is effective only if graphics mode horizontal expansion is enabled via SR54_3-2.

Bits 7-5 Reserved

Flat Panel Vertical Compensation 1 Register (SR56)

Read/Write Address: 3C5H, Index 56H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	VCE	GRAPH EXP		TEXT EXP	

Bits 1-0 TEXT EXP - Text Mode Vertical Expansion
00 = Vertical expansion disabled
01 = Vertical expansion enabled up to a maximum of 480 lines
10 = Reserved
11 = Vertical expansion enabled up to the vertical panel size

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 480 lines to limit the expansion and eliminate the undesirable visual effects.

Bits 3-2 GRAPH EXP - Graphics Mode Vertical Expansion
00 = Vertical expansion disabled
01 = Vertical expansion enabled up to a maximum of 480 lines
10 = Reserved
11 = Vertical expansion enabled up to the horizontal panel size.

The 11b setting will normally be used unless the expansion causes the text to look bad. In this case, the 01 setting can be used for panels larger than 480 lines to limit the expansion and eliminate the undesirable visual effects.

Bit 4 VCE - Vertical Centering Enable
0 = Vertical centering disabled
1 = Vertical centering enabled

Bits 7-5 Reserved

Flat Panel Vertical Compensation 2 Register (SR57)

Read/Write Address: 3C5H, Index 57H
Power-On Default: 00H

The bits in this register control enabling of vertical expansion in specific text/graphics modes. Vertical expansion for all other modes not controlled by these bits is controlled by SR56_3-0.

7	6	5	4	3	2	1	0
R	768G	600G	480G	200G	350G	200T	350T

Bit 0 350T - 350-line Text Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 350-line text mode
1 = Vertical expansion enabled in 350-line text mode

This bit is effective only if text mode vertical expansion is enabled via SR56_1-0.

Bit 1 200T - 200/400-line Text Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 200/400-line text mode
1 = Vertical expansion enabled in 200/400-line text mode

This bit is effective only if text mode vertical expansion is enabled via SR56_1-0.

Bit 2 350G - 350-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 350-line graphics mode
1 = Vertical expansion enabled in 350-line graphics mode

Bit 3 200G - 200/400-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 200/400-line graphics mode
1 = Vertical expansion enabled in 200/400-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_3-2.

Bit 4 480G - 480-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 480-line graphics mode
1 = Vertical expansion enabled in 480-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_3-2.

Bit 5 600G - 600-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 600-line graphics mode
1 = Vertical expansion enabled in 600-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_3-2.

Bit 6 768G - 768-line Graphics Mode Vertical Expansion Enable
0 = Vertical expansion disabled in 768-line graphics mode
1 = Vertical expansion enabled in 768-line graphics mode

This bit is effective only if graphics mode vertical expansion is enabled via SR56_3-2.

Bit 7 Reserved

Flat Panel Horizontal Border Register (SR58)

Read Only Address: 3C5H, Index 58H
Power-On Default: 00H

7	6	5	4	3	2	1	0
FP HORIZONTAL BORDER 7-0							

Bits 7-0 FP HORIZONTAL BORDER 7-0

9-bit Value = number of character clocks per horizontal line not used by the video image.

Bit 8 of this value is in SR59_0.

Flat Panel Horizontal Expansion Factor Register (SR59)

Read Only Address: 3C5H, Index 59H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	HORIZ EXP FACTOR			R	R	R	HB8

Bit 0 HB8 - Flat Panel Horizontal Border Bit 8

Bits 7-0 are in SR58.

Bits 3-1 Reserved

Bits 6-4 HORIZ EXP FACTOR
000 = panel size < image size
001 = 1 1/8x image size > panel size ≥ image size
010 = illegal
011 = 1 1/4x image size > panel size ≥ 1 1/8x image size
100 = 1 1/2x image size > panel size ≥ 1 1/4x image size
101 = illegal
110 = 2x image size > panel size ≥ 1 1/2x image size
111 = panel size ≥ 2x image size

Bit 7 Reserved

Flat Panel Vertical Border Register (SR5A)

Read Only
Power-On Default: 00H

Address: 3C5H, Index 5AH

7	6	5	4	3	2	1	0
FP VERTICAL BORDER 7-0							

Bits 7-0 FP VERTICAL BORDER 7-0

9-bit Value = number of lines not used by the video image

Bit 8 of this value is SR5B_0.

Flat Panel Vertical Expansion Factor Register (SR5B)

Read Only
Power-On Default: 00H

Address: 3C5H, Index 5BH

7	6	5	4	3	2	1	0
VERT EXP FACTOR				LRI	VCD	VED	VB8

Bit 0 VB8 - Flat Panel Vertical Border Bit 8

Bits 7-0 are in SR5A.

Bit 1 VED - Vertical Expansion Detect
0 = No vertical expansion
1 = Automatic vertical expansion is being done or would be being done if enabled.

This bit is used only for test puposes.

Bit 2 VCD - Vertical Centering Detect
0 = No vertical centering
1 = Automatic vertical centering is being done (it must be enabled)

This bit is used only for test puposes.

Bit 3 LRI - Line Repeat Indicator
0 = Current scan line will be repeated on the next scan line
1 = Current scan line will not be repeated on on the next scan line

This bit is used only for test puposes.

Bits 7-4 VERT EXP FACTOR
0000 = No expansion
0001 = Illegal
0010 = Double every third line
0011 = Expand 16-line text to 19-line text
0100 = Double every fifth line
0101 = Expand 14-line text to 19-line text
0110 = Double every fourth line
0111 = Double every second line
1000 = Double every line
1001 = Double three lines and triple the fourth, repeat
1010 = Expand 8-line text to 19-line text
1011 = Double four lines and triple the fifth, repeat
1100 = Double two lines and triple the third, repeat
1101 = Illegal
1110 = Double one line and triple the second, repeat
1111 = Quadruple every line

Flat Panel Display Enable Position Control Register (SR5C)

Read/Write Address: 3C5H, Index 5CH
Power-On Default: Undefined

The fields in this register are effective only for Enhanced modes (8 bits/pixel or higher). The BIOS should program this register to 77H on reset.

7	6	5	4	3	2	1	0
FPDEC2				FPDEC1			

Bits 3-0 FPDEC1 - Flat Panel Display Enable Control 1

value = starting position of the horizontal and vertical display enables for Controller 1

This field should normally be left at its default value of 0111b. A smaller value causes the display enables to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the display enables to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Bits 7-4 FPDEC2 - Flat Panel Display Enable Control 2

value = starting position of the horizontal and vertical display enables for Controller 2

This field should normally be left at its default value of 0111b. A smaller value causes the display enables to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the display enables to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Flat Panel/CRT Sync Position Control Register (SR5D)

Read/Write Address: 3C5H, Index 5DH
Power-On Default: 77H

The fields in this register are effective only for Enhanced modes (8 bits/pixel or higher). The BIOS should program this register to 77H on reset.

7	6	5	4	3	2	1	0
FP/CRTSC2				FP/CRTSC1			

Bits 3-0 FP/CRTSC1 - Flat Panel/CRT Sync Control 1

value = starting position of the horizontal and vertical syncs for Controller 1

This field should normally be left at its default value of 0111b. A smaller value causes the syncs to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the syncs to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

Bits 7-4 FP/CRTSC2 - Flat Panel Sync Control 2

value = starting position of the horizontal and vertical display enables for Controller 2

This field should normally be left at its default value of 0111b. A smaller value causes the syncs to be moved earlier by the difference between the programmed value and the nominal value. A larger value causes the syncs to be moved later by the difference between the programmed value and the nominal value. Each difference unit causes a shift of 1 DCLK.

FIFO Control Register (SR5F)

Read/Write Address: 3C5H, Index 5FH
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	C2FR	SRF	SWF	C2F	C1F

Bit 0 Controller 1 FIFO
0 = Normal operation
1 = Controller 1 FIFO memory access requests disabled

This bit is used only for test purposes. When set , CR22_7 must also be set for Controller 1.

Bit 1 C2F - Controller 2 FIFO
0 = Normal operation
1 = Controller 2 FIFO memory access requests disabled

This bit is used only for test purposes. When set , CR22_7 must also be set for Controller 2.

Bit 2 SWF - STN Write FIFO
0 = Normal operation
1 = STN write FIFO memory access requests disabled

This bit is used only for test purposes.

Bit 3 SRF - STN Read FIFO
0 = Normal operation
1 = STN read FIFO memory access requests disabled

This bit is used only for test purposes.

Bit 4 C2FR - Controller 2 FIFO Rate
0 = 2 MCLK reads for Controller 2 FIFO
1 = 2 MCLK reads for Controller 2 FIFO

This bit is set to 1 when 1-cycle EDO operation is selected (CR36_3-2 = 00b)

Bits 7-5 Reserved

Flat Panel Horizontal Total Register (SR60)

Read/Write Address: 3C5H, Index 60H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL TOTAL 7-0							

Bits 7-0 FP HORIZONTAL TOTAL 7-0

9-bit Value = [number of character clocks in one scan line] - 5

A character clock is always 8 FPSCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66_0.

Flat Panel Horizontal Panel Size Register (SR61)

Read/Write Address: 3C5H, Index 61H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL PANEL SIZE 7-0							

Bits 7-0 FP HORIZONTAL PANEL SIZE 7-0

9-bit Value = [horizontal panel resolution in character clocks] - 1

A character clock is always 8 FPSCLKs (FP dot clocks). For example, for a VGA panel with a horizontal resolution of 640, the programmed value would be the binary equivalent of [640/8] - 1. The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66_1.

Flat Panel Horizontal Blank Start Register (SR62)

Read/Write Address: 3C5H, Index 62H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL BLANK START 7-0							

Bits 7-0 FP HORIZONTAL BLANK START 7-0

9-bit Value = character clock counter value at which blanking begins

A character clock is always 8 FPSCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66_2.

Flat Panel Horizontal Blank End Register (SR63)

Read/Write Address: 3C5H, Index 63H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	FP HORIZONTAL BLANK END 4-0				

Bits 4-0 FP HORIZONTAL BLANK END 4-0

6-bit Value = least significant 6 bits of the character clock counter value at which blanking ends

A character clock is always 8 FPSCLKs (FP dot clocks). To obtain this value, add the desired width of the vertical blanking pulse in character clocks to the value in the FP Horizontal Blank Start register, also in character clocks. The 5 least significant bits of this value are programmed into this field. The programmed value is independent of horizontal compensation and applies to all modes. Bit 5 of this value is SR65_7. If the horizontal blank period is more than 64 character clocks, then SR66_3 must be set to 1.

Bits 7-5 Reserved

Flat Panel Horizontal Sync Start Register (SR64)

Read/Write Address: 3C5H, Index 64H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP HORIZONTAL SYNC START 7-0							

Bits 7-0 FP HORIZONTAL SYNC START 7-0

8-bit Value = character clock counter value at which the horizontal sync pulse (LP) becomes active

A character clock is always 8 FPSCLKs (FP dot clocks). The programmed value is independent of horizontal compensation and applies to all modes. Bit 8 of this value is SR66_4.

Flat Panel Horizontal Sync End Register (SR65)

Read/Write Address: 3C5H, Index 65H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
BE5	R	R	FP HORIZONTAL SYNC END 4-0				

Bits 4-0 FP HORIZONTAL SYNC END 4-0

5-bit Value = least significant 5 bits of the character clock counter value at which the horizontal sync pulse (LP) becomes inactive

A character clock is always 8 FPSCLKs (FP dot clocks). To obtain this value, add the desired width of the horizontal sync pulse in character clocks to the value in the FP Horizontal Sync Start register. The 5 least significant bits of this value are programmed into this field. The programmed value is independent of horizontal compensation and applies to all modes. If the horizontal sync period is more than 32 character clocks, SR66_5 must be set to 1.

Bits 6-5 Reserved

Bit 7 BE5 - FP Horizontal Sync End Bit 5

Bits 4-0 are in this register.

Flat Panel Horizontal Overflow Register (SR66)

Read/Write Address: 3C5H, Index 66H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HSE5	HSS8	HBP	HBS8	HPS8	HT8

Bit 0 FP Horizontal Total Bit 8

Bits 7-0 are in SR60.

Bit 1 FP Horizontal Panel Size Bit 8

Bits 7-0 are in SR61.

Bit 2 FP Horizontal Blank Start Bit 8

Bits 7-0 are in SR62.

Bit 3 FP Horizontal Blank Period
0 = Flat panel horizontal blank period is 64 character clocks or less
1 = Flat panel horizontal blank period is greater than 64 character clocks

See SR 63_4-0.

Bit 4 FP Horizontal Sync Start Bit 8

Bits 7-0 are in SR64.

Bit 5 FP Horizontal Sync Period
0 = Flat panel horizontal sync period is 32 character clocks or less
1 = Flat panel horizontal sync period is greater than 32 character clocks

See SR65_4-0.

Bits 7-6 Reserved

Flat Panel Vertical Total Register (SR68)

Read/Write Address: 3C5H, Index 68H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL TOTAL 7-0							

Bits 7-0 FP VERTICAL TOTAL 7-0

11-bit Value = [number of scan lines from one vertical sync pulse (FLM) active to the next vertical sync pulse active] - 2

The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6E_2-0.

Flat Panel Vertical Panel Size Register (SR69)

Read/Write Address: 3C5H, Index 69H
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL PANEL SIZE 7-0							

Bits 7-0 FP VERTICAL PANEL SIZE 7-0

11-bit Value = [vertical panel resolution in scan lines] - 1

For example, for a VGA panel with a vertical resolution of 480, the programmed value would be the binary equivalent of 480 - 1. The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6E_6-4.

Flat Panel Vertical Blank Start Register (SR6A)

Read/Write Address: 3C5H, Index 6AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL BLANK START 7-0							

Bits 7-0 FP VERTICAL BLANK START 7-0

11-bit Value = scan line counter value at which blanking begins

The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6F_2-0.

Flat Panel Vertical Blank End Register (SR6B)

Read/Write Address: 3C5H, Index 6BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL BLANK END 7-0							

Bits 7-0 FP VERTICAL BLANK END 7-0

Value = least significant 8 bits of the scan line counter value at which blanking ends

To obtain this value, add the desired width of the vertical blanking pulse in scan lines to the value in the FP Vertical Blank Start register, also in scan lines. The 8 least significant bits of this value are programmed into this field. The programmed value is independent of vertical compensation and applies to all modes.

Flat Panel Vertical Sync Start Register (SR6C)

Read/Write Address: 3C5H, Index 6CH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
FP VERTICAL SYNC START 7-0							

Bits 7-0 FP VERTICAL SYNC START 7-0

11-bit Value = [scan line counter value at which the vertical sync pulse (FLM) becomes active] -1

The programmed value is independent of vertical compensation and applies to all modes. Bits 10-8 of this value are SR6F_6-4.

Flat Panel Vertical Sync End Register (SR6D)

Read/Write Address: 3C5H, Index 6DH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	R	R	FP VERTICAL SYNC END 3-0			

Bits 3-0 FP VERTICAL SYNC END 3-0

4-bit Value = least significant 4 bits of the character clock counter value at which the vertical sync pulse (FLM) becomes inactive

To obtain this value, add the desired width of the vertical sync pulse in scan lines to the value in the FP Vertical Sync Start register, also in scan lines. The 4 least significant bits of this value are programmed into this field. The programmed value is independent of vertical compensation and applies to all modes.

Bits 7-4 Reserved

Flat Panel Vertical Overflow 1 Register (SR6E)

Read/Write Address: 3C5H, Index 6EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	VPS10-8			R	VT10-8		

Bits 2-0 VT10-8 - FP Vertical Total Bits 10-8

Bits 7-0 are in SR68.

Bit 3 Reserved

Bits 6-4 VPS10-8 - FP Vertical Panel Size Bits 10-8

Bits 7-0 are in SR69.

Bit 7 Reserved

Flat Panel Vertical Overflow 2 Register (SR6F)

Read/Write Address: 3C5H, Index 6FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	VSS10-8			R	VBS10-8		

Bits 2-0 VBS10-8 - FP Vertical Blank Start Bits 10-8

Bits 7-0 are in SR6A.

Bit 3 Reserved

Bits 6-4 VSS10-8 - FP Vertical Sync Start Bits 10-8

Bits 7-0 are in SR6C.

Bit 7 Reserved

Section 19: Extended CRTC Register Descriptions

The 86CM65 has additional registers to extend the functions beyond VGA. These registers are located in CRT Controller address space at locations not used by the IBM® VGA. All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, CR38 and/or CR39 must be loaded with a changed key pattern (see the register descriptions). The registers will remain unlocked until the key pattern is reset by altering a significant bit. If a register or bit is noted as paired, there are two identical registers or bit at that address, with access controlled via SR26. One register or bit is used by controller 1 and the other for controller 2. If a register or bit is noted as shared, there is a single register or bit shared by controller 1 or controller 2.

In the following register descriptions, 'R' stands for reserved (write =0, read = undefined). See Appendix A for a table listing each register in this section and its page number.

CRT Test 1 Register (CTR22)

Read/Write — Address: 3?5H, Index 22H
Power-On Default: 00H — Paired

This register is accessible at Index 22H (instead of CR22) when CR39 = A5H.

7	6	5	4	3	2	1	0
TDD	R	R	R	R	R	R	R

Bits 6-0 Reserved

Bit 7 TDD - Test DAC Data
0 = Normal operation
1 = 24 bits of data are provided to the DAC by internal counters.

This bit must be set for the appropriate controller when either SR5F_0 = 1 (disabling Controller 1 frame buffer accesses) or SR5F_1 = 1 (disabling Controller 2 frame buffer accesses).

Device ID High Register (CR2D)

Read Only Address: 3?5H, Index 2DH
Power-On Default: 88H

This register should contain the same value as the upper byte of the PCI Device ID (Index 02H) register.

7	6	5	4	3	2	1	0
CHIP ID HIGH							

Bits 7–0 CHIP ID HIGH

value = 88H (hardwired)

Device ID Low Register (CR2E)

Read Only Address: 3?5H, Index 2EH
Power-On Default: 12H

7	6	5	4	3	2	1	0
CHIP ID LOW							

Bits 7–0 CHIP ID LOW

value = 12H (hardwired)

Revision Register (CR2F)

Read Only Address: 3?5H, Index 2FH
Power-On Default: xxH

7	6	5	4	3	2	1	0
REVISION LEVEL							

Bits 7–0 REVISION LEVEL

This value will vary by chip revision.

Chip ID/REV Register (CR30)

Read Only Address: 3?5H, Index 30H
Power-On Default: E1H

When the software detects EH in the upper nibble of this register, it should then use CR2D, CR2E and CR2F for chip ID information.

7	6	5	4	3	2	1	0
CHIP ID				REVISION STATUS			

Bits 7–0 CHIP ID AND REVISION STATUS

Memory Configuration Register (CR31)

Read/Write Address: 3?5H, Index 31H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	HST DFF	R	R	ENH MAP	VGA 16B	SCRN 2.PG	R

Bit 0 Reserved

Bit 1 SCRN 2.PG - Enable Two-Page Screen Image
0 = Normal Mode
1 = Enable 2K x 1K x 4 map image screen for 1024 x 768 or 800 x 600 screen resolution, or 2K x 512 x 8 map image screen for 640 x 480 screen resolution

Bit 2 VGA 16B - Enable VGA 16-bit Memory Bus Width
0 = 8-bit memory bus operation
1 = Enable 16-bit bus VGA memory read/writes

This is useful in VGA text modes when VGA graphics controller functions are typically not used.

Bit 3 ENH MAP - Use Enhanced Mode Memory Mapping
0 = Force IBM VGA mapping for memory accesses
1 = Force Enhanced Mode mappings

Setting this bit to 1 overrides the settings of bit 6 of CR14 and bit 3 of CR17 and causes the use of doubleword memory addressing mode. Also, the function of bits 3-2 of GR6 is overridden with a fixed 64K map at A0000H.

Note: This bit is forced to 1 for Controller 2 operation.

Bits 5–4 Reserved

Bit 6 HST DFF - Enable High Speed Text Display Font Fetch Mode
0 = Normal font access mode
1 = Enable high speed text display

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz. See bit 5 of CR3A.

Note: This bit is paired.

Bit 7 Reserved

Backward Compatibility 1 Register (CR32)

Read/Write Address: 3?5H, Index 32H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	VGA FXPG	R	INT EN	R	FCCH	R	R

Bits 1–0 Reserved

Bit 2 FCCH - Force Character Clock High
0 = Normal character clock
1 = Force horizontal timings to be based on undivided DCLK even if SR1_3 is set to 1 to divide DCLK by 2

Bit 3 Reserved

Bit 4 INT EN -Interrupt Enable
0 = All interrupt generation disabled
1 = Interrupt generation enabled

Bit 5 Reserved

Bit 6 VGA FXPG - Use Standard VGA Memory Wrapping
0 = Memory accesses extending past a 256K boundary do not wrap
1 = Memory accesses extending past a 256K boundary wrap at the boundary

The standard 256K VGA memory page always ends on a natural 256K boundary and accesses beyond this boundary will wrap. If the starting address is moved via bits 4-0 of CR69 (or bits 5-4 of CR31 and bits 1-0 of CR51), the 256K page may not end on a 256K boundary and accesses past the boundary will not wrap. This is the case when this bit is cleared to 0. For standard VGA compatibility when the page base address is moved, this bit is set to 1 to cause wrapping at a 256K boundary.

Note: This bit is forced to 0 for Controller 2 operation.

Bit 7 Reserved

Backward Compatibility 2 Register (CR33)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 33H

7	6	5	4	3	2	1	0
R	LOCK PLTW	BDR SEL	LOCK DACW	VCLK= -DCK	R	DIS VDE	R

Bit 0 Reserved

Bit 1 DIS VDE - Disable Vertical Display End Extension Bits Write Protection
0 = VDE protection enabled
1 = Disables the write protect setting of the bit 7 of CR11 on bits 1 and 6 of CR7

Bit 2 Reserved

Bit 3 VCLK = -DCK - VCLK is Inverted DCLK
0 = VCLK is determined by other bit settings
1 = VCLK is forced to inverted DCLK

Note: This bit is paired.

Bit 4 LOCK DACW - Lock RAMDAC Writes
0 = Enable writes to RAMDAC registers
1 = Disable writes to RAMDAC registers

Note: This bit is paired.

Bit 5 BDR SEL - Blank/Border Select
0 = $\overline{\text{BLANK}}$ active time is defined by CR2 and CR3
1 = $\overline{\text{BLANK}}$ is active during entire display inactive period (no border)

Note: This bit is paired.

Bit 6 LOCK PLTW - Lock Palette/Border Color Registers
0 = Unlock Palette/Border Color registers
1 = Lock Palette/Border Color registers

Note: This bit is paired.

Bit 7 Reserved

Backward Compatibility 3 Register (CR34)

Read/Write Address: 3?5H, Index 34H
Power-On Default: 00H

7	6	5	4	3	2	1	0
LOCK CLKS	R	LOCK 8/9D	ENB SFF	R	PCI RET	PCI ABT	PCI SNP

Bit 0 PCI SNP - PCI DAC snoop method
0 = Handling of PCI master aborts and retries during DAC cycles controlled by bits 1 and 2 of this register
1 = PCI master aborts and retries are not handled during DAC cycles

Bit 1 PCI ABT - PCI master aborts during DAC cycles
0 = PCI master aborts handled during DAC cycles
1 = PCI master aborts not handled during DAC cycles

Bit 0 of this register must be cleared to 0 for this bit to be effective.

Bit 2 PCI RET - PCI retries during DAC cycles
0 = PCI retries handled during DAC cycles
1 = PCI retries not handled during DAC cycles

Bit 0 of this register must be cleared to 0 for this bit to be effective.

Bit 3 Reserved

Bit 4 ENB SFF - Enable Start Display FIFO Fetch Register
0 = Start Display FIFO Fetch register (CR3B) disabled
1 = Start Display FIFO Fetch register (CR3B) enabled

Note: This bit is paired.

Bit 5 LOCK 8/9D - Lock 8/9 Dots
0 = Bit 0 of SR1 is unlocked
1 = Bit 0 of SR1 is locked

This bit locks/unlocks selection of either an 8 dot or 9 dot character clock.

Bit 6 Reserved

Bit 7 LOCK CLKS - Lock Clock Select
0 = Bits 3-2 of 3C2H are unlocked
1 = Bits 3-2 of 3C2H are locked

This bit locks/unlocks selection of the the DCLK frequency.

CRT Register Lock Register (CR35)

Read/Write
Power-On Default: 00H
Address: 3?5H, Index 35H
Paired

7	6	5	4	3	2	1	0
LOCK CR12	LOCK CR1	LOCK HTMG	LOCK VTMG	R	R	R	R

Bits 3–0 Reserved

Bit 4 LOCK VTMG - Lock Vertical Timing Registers
0 = Vertical timing registers are unlocked
1 = The following vertical timing registers are locked:

CR6
CR7 (bits 7,5,3,2,0)
CR9 (bit 5)
CR10
CR11 (bits 3-0)
CR15
CR16

CR6, CR7 registers are also locked by bit 7 of the Vertical Retrace End register (CR11).

Bit 5 LOCK HTMG - Lock Horizontal Timing Registers
0 = Horizontal timing registers are unlocked
1 = The following horizontal timing registers are locked:

CR00
CR1
CR2
CR3
CR4
CR5
CR17 (bit 2)

All these registers (except bit 2 of CR17) are also locked by bit 7 of the Vertical Retrace End register (CR11).

Bit 6 LOCK CR1
0 = CR1 and 3C2H_6 unlocked
1 = CR1 and 3C2H_6 locked

Bit 7 LOCK CR12
0 = CR12 and 3C2H_7 unlocked
1 = CR12 and 3C2H_7 locked

Configuration 1 Register (CR36)

Read/Write* Address: 3?5H, Index 36H
Power-On Default: Depends on Strapping

* Bits 1-0 are read only. The other bits can be written only after 0A5H is written to CR39.

This register samples the reset state from PD bus pins [7:0]. These pins have internal pull-downs and their states are inverted, so non-reserved register bits will default to 1 if the corresponding pin is not pulled up. Other configuration strapping bits are found in CR37 and CR68 and CR6F.

7	6	5	4	3	2	1	0
MEM SIZE			R	MEM TYPE		R	R

Bits 1-0 Reserved

Bit 3-2 MEM TYPE
00 = 1-cycle Extended Data Out (EDO) operation
01 = Reserved
10 = 2-cycle EDO mode
11 = Fast page mode

Bit 4 Reserved

Bits 7-5 MEM SIZE
000 = 4 MBytes (valid only for 512Kx32 DRAMs)
100 = 2 MBytes
110 = 1 MByte (valid only for 256Kx16 DRAMs)

All other values are reserved. These PD bits should not be strapped, as they are over-written by the BIOS after boot up.

Configuration 2 Register (CR37)

Read/Write* Address: 3?5H, Index 37H
Power-On Default: Depends on Strapping

* These bits can be written only after 0A5H is written to CR39.

This register samples the reset state from PD bus pins [15:7]. These pins have internal pull-downs and their states are inverted, so non-reserved register bits will default to 1 if the corresponding pin is not pulled up. Other configuration strapping bits are found in CR36, CR68 and CR6F.

7	6	5	4	3	2	1	0
PANEL TYPE			R	CS	R	BS	R

Bit 0 Reserved

Bit 1 BS - Boundary Scan
0 = Boundary scanning enabled (allows testing for bad solder connections. See Section 5.)
1 = Boundary scanning disabled (normal operation)

Bit 2 Reserved

Bit 3 CS - Clock Select
0 = Use external DCLK and MCLK (test purposes only)
1 = Use internal DCLK, MCLK

Bits 4 Reserved

Bits 7-5 PANEL TYPE

OEMs can strap PD[15:13] to allow identification of up to 8 different panel types. The coding used is defined by each OEM.

Register Lock 1 Register (CR38)

Read/Write Address: 3?5H, Index 38H
Power-On Default: 00H Shared

Loading 01xx10xx (e.g., 48H) into this register unlocks the extended CRTC registers from CR2D through CR3F for read/writes. (x = don't care)

7	6	5	4	3	2	1	0
= 0	= 1			= 1	= 0		

Register Lock 2 Register (CR39)

Read/Write Address: 3?5H, Index 39H
Power-On Default: 00H Shared

Loading 101xxxxx (e.g., A0H) unlocks the extended CRTC registers from CR40 through CRFF for reading/writing (x = don't care). Loading A5H allows bits 7-2 of CR36, bits 7-0 of CR37, bits 7-0 of CR68 and bits 7-0 of CR6F to be written and alsoselects the CTR registers at Indexes 22H-29H instead of the CR registers at those same indices.

7	6	5	4	3	2	1	0
= 1	= 0	= 1					

Miscellaneous 1 Register (CR3A)

Read/Write Address: 3?5H, Index 3AH
Power-On Default: 00H

7	6	5	4	3	2	1	0
PCIRB DISA	R	HST DFW	ENH 256	TOP MEM	ENB RFC	REF-CNT 1	0

Bits 1–0 REF-CNT - Alternate Refresh Count Control
00 = Refresh Count 0
01 = Refresh Count 1
10 = Refresh Count 2
11 = Refresh Count 3

If enabled by setting bit 2 of this register to 1, these bits override the refresh count in bit 6 of CR11 and specify the number of refresh cycles per horizontal line.

Bit 2 ENB RFC - Enable Alternate Refresh Count Control
0 = Alternate refresh count control (bits 1-0) is disabled
1 = Alternate refresh count control (bits 1-0) is enabled

Bit 3 TOP MEM - Enable Top of Memory Access
0 = Top of memory access disabled
1 = Simultaneous VGA text and Enhanced modes are enabled. CPU and CRTC accesses are then directed to the top 32- or 64-KByte area of display memory depending on whether address bit 13 is 0 or 1 respectively.

Note: This bit is paired.

Bit 4 ENH 256 - Enable 8 Bits/Pixel or Greater Color Enhanced Mode
0 = Attribute controller shift registers configured for 4-bit modes
1 = Attribute controller shift register configured for 8-, 16- and 24/32-bit color Enhanced modes

Note: This bit is paired.

Bit 5 HST DFW - Enable High Speed Text Font Writing
0 = Disable high speed text font writing
1 = Enable high speed text font writing

Setting this bit to 1 is only required for DCLK rates greater than 40 MHz. See bit 6 of CR31.

Bit 6 Reserved

Bit 7 PCIRB DISA - PCI Read Bursts Disabled
0 = PCI read burst cycles enabled
1 = PCI read burst cycles disabled

Note: Bit 7 of CR66 must be set to 1 before this bit is set to 1.

Start Display FIFO Register (CR3B)

Read/Write — Address: 3?5H, Index 3BH
Power-On Default: 00H — Paired

This value must lie in the horizontal blanking period and is typically 5 less than the value programmed in CR0. This parameter helps to ensure that adequate time is available during horizontal blanking for activities such as RAM refresh that require control of the display memory. Bit 9 of this value is bit 6 of CR5D. This register must be enabled by setting bit 4 of CR34 to 1 and CR63_4-3 to 01b.

7	6	5	4	3	2	1	0
START DISPLAY FIFO FETCH							

Bits 7–0 START DISPLAY FIFO FETCH
9-bit Value = the time in character clocks from the active display start until the restart of fetching of FIFO data after the start of horizontal blanking. This register contains the low-order 8 bits of this value.

Interlace Retrace Start Register (CR3C)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 3CH
Paired

This value allows determination of the even/odd row active display starting positions when operating in an interlaced mode. This register is enabled by bit 5 of CR42.

7	6	5	4	3	2	1	0
INTERLACE RETRACE START POSITION							

Bits 7–0 INTERLACE RETRACE START POSITION
Value = offset in terms of character clocks for Interlaced mode start/end in even/odd frames.

NTSC/PAL Control Register (CR3D)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 3DH

7	6	5	4	3	2	1	0
R	R	N/P	B/W	TV OUTPUT			TV

Bit 0 TV - Enable TV Mode
0 = Disable TV mode
1 = Enable TV mode

Bit 3-1 TV OUTPUT
x00 = AG = luma; AR = chroma (S-Video)
011 = AG = composite; AR = composite (NTSC/PAL)
111 = AG = composite; AR = black burst (NTSC/PAL)

All other values are reserved

Bit 4 B/W - Black and White Video
0 = Color TV output
1 = Black and white TV output

Bit 5 N/P = NTSC/PAL
0 = NTSC output
1 = PAL output

Bits 7-6 Reserved

System Configuration Register (CR40)

Read/Write
Power-On Default: 30H

Address: 3?5H, Index 40H

7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	EN ENH

Bit 0 EN ENH - Enable Enhanced Register Access
0 = Enhanced register access disabled
1 = Enhanced register (x2E8H) access enabled

Bits 7–1 Reserved

BIOS Flag Register (CR41)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 41H

7	6	5	4	3	2	1	0
BIOS-FLAG-REGISTER-1							

Bits 7–0 BIOS-FLAG-REGISTER-1
Used by the video BIOS.

Mode Control Register (CR42)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 42H

7	6	5	4	3	2	1	0
R	R	INTL MODE	R	R	R	R	R

Bits 4–0 Reserved

Bit 5 INTL MODE - Interlaced Mode
0 = Noninterlaced
1 = Interlaced

This bit enables the function of CR3C.

Note: This bit is paired.

Bits 7–6 Reserved

Extended Mode Register (CR43)

Read/Write Address: 3?5H, Index 43H
Power-On Default: 00H Paired

7	6	5	4	3	2	1	0
HCTR X2	CURSOR BLINK		R	CHR BLNK	R	R	R

Bits 2–0 Reserved

Bit 3 CHR BLNK - Character Blink Control
0 = Blink every 32 frames
1 = Blink every 64 frames

Bit 4 Reserved

Bits 6–5 CURSOR BLINK
00 = Blink every 16 frames
01 = Blink every 32 frames
1x = Blink every 64 frames

Bit 7 HCTR X2 - Horizontal Counter Double Mode
0 = Disable horizontal counter double mode
1 = Enable horizontal counter double mode (horizontal CRT parameters are doubled)

Hardware Graphics Cursor Mode Register (CR45)

Read/Write Address: 3?5H, Index 45H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	HWGC 1280	R	R	R	HWGC ENB

Bit 0 HWGC ENB - Hardware Graphics Cursor Enable
0 = Hardware graphics cursor disabled in any mode
1 = Hardware graphics cursor enabled in Enhanced mode

Bits 3-1 Reserved

Bit 4 HWGC 1280 - Hardware Cursor Right Storage
0 = Function disabled
1 = For 4 bits/pixel, the last 256 bytes in each 1-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. For 8 bits/pixel, the last 512 bytes in each 2-KByte line of the hardware cursor start address become the hardware graphics cursor storage area. In either case, bits 1-0 of CR4D must be 11b.

Bits 7–5 Reserved

Hardware Graphics Cursor Origin-X Registers (CR46, CR47)

Read/Write Address: 3?5H, Index 46H, 47H
Power-On Default: 0000H

The high order three bits are written into CR46 and the low order byte is written into CR47.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG X (H)			HWGC ORG X (L)							

Bits 10–0 HWGC ORG X(H) (L) - X-Coordinate of Cursor Left Side

Bits 15–11 Reserved

Hardware Graphics Cursor Origin-Y Registers (CR48, CR49)

Read/Write Address: 3?5H, Index 48H, 49H
Power-On Default: Undefined

The high order three bits are written into CR48 and the low order byte is written into CR49.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	HWGC ORG Y (H)			HWGC ORG Y (L)							

Bits 10–0 HWGC ORG Y (H)(L) - Y-Coordinate of Cursor Upper Line
The cursor X, Y position is registered upon writing HWGC ORG Y (H).

Bits 15–11 Reserved

Hardware Graphics Cursor Foreground Color Stack Register (CR4A)

Read/Write Address: 3?5H, Index 4AH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR FOREGROUND STACK (0-2)							

Bits 7–0 TRUE COLOR FOREGROUND STACK (0-2)

Three foreground color registers are stacked at this address. The stack pointer (common with CR4B) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4A) increments the stack pointer by 1, so three writes provide 24 bits of true color information.

Hardware Graphics Cursor Background Color Stack Register (CR4B)

Read/Write Address: 3?5H, Index 4BH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
TRUE COLOR BACKGROUND STACK (0-2)							

Bits 7–0 TRUE COLOR BACKGROUND STACK (0-2)

Three background color registers are stacked at this address. The stack pointer (common with CR4A) is reset to 0 by reading the Hardware Graphics Cursor Mode register (CR45). Each write to this register (CR4B) increments the stack pointer by 1, so three writes provide 24 bits of true color information.

Hardware Graphics Cursor Storage Start Address Registers (CR4C, CR4D)

Read/Write Address: 3?5H, Index 4CH, 4DH
Power-On Default: Undefined

The high order four bits are written into CR4C and the low order byte is written into CR4D.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	HWGC STA(H)				HWGC STA(L)							

Bits 11–0 HWGC STA(H)(L) - Hardware Graphics Cursor Storage Start Address

Bits 15–12 Reserved

Hardware Graphics Cursor Pattern Display Start X-PXL-Position Register (CR4E)

Read/Write Address: 3?5H, Index 4EH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START X-POS					

Bits 5–0 HWGC PAT DISP START X-POS - HWGC Pattern Display Start-X Pixel Position

This value is the offset (in pixels) from the left side of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the left border of the display.

Bits 7–6 Reserved

Hardware Graphics Cursor Pattern Disp Start Y-PXL-Position Register (CR4F)

Read/Write Address: 3?5H, Index 4FH
Power-On Default: Undefined

7	6	5	4	3	2	1	0
R	R	HWGC PAT DISP START Y-POS					

Bits 5–0 HWGC PAT DISP START Y-POS - HWGC Pattern Display Start-Y Pixel Position

This value is the offset (in pixels) from the top of the 64x64 cursor pixel pattern from which the cursor is displayed. This allows a partial cursor to be displayed at the top of the display.

Bits 7–6 Reserved

Extended System Cont 1 Register (CR50)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 50H

7	6	5	4	3	2	1	0
GE-SCR-W 1	0	PXL-LNGH 1	0	R	R	R	GESW 2

Bit 0 Extension bit 2 of the screen width definition. See bits 7-6 below.

Bits 3-1 Reserved

Bits 5–4 PXL-LNGH - Pixel Length Select
00 = 1 byte (Default). This corresponds to a pixel length of 4 or 8 bits/pixel in 42E8H_7
01 = 2 bytes. 16 bits/pixel
10 = Reserved
11 = 4 bytes. 32 bits/pixel

These bits select the pixel length for Enhanced mode command execution through the Graphics Engine.

Bits 7–6 GE-SCR-W - Graphics Engine Command Screen Pixel Width
Bit 0 of this register is the most significant bit of this definition.
000 = 1024 (or 2048 if bit 1 of CR31 =1) (Default)
001 = 640
010 = 800 (or 1600x1200x4 if bit 2 of 4AE8H = 0)
011 = 1280
100 = 1152
101 = Reserved
110 = 1600
111 = Reserved

Extended System Control 2 Register (CR51)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 51H
Paired

7	6	5	4	3	2	1	0
R	R	LOG-SCR-W 9	8	R	R	R	R

Bits 3–0 Reserved

Bits 5–4 LOG-SCR-W - Logical Screen Width Bits 9-8
These are two extension bits of the Offset register (CR13)

Bits 7–6 Reserved

Extended BIOS Flag 1 Register (CR52)

Read/Write Address: 3?5H, Index 52H
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-1							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-1

See the S3 video BIOS documentation for the coding of this register.

Extended Memory Control 1 Register (CR53)

Read/Write Address: 3?5H, Index 53H
Power-On Default: See Bit Descriptions

7	6	5	4	3	2	1	0
R	SWP NBL	MMIO WIN	MMIO SELECT		BIG ENDIAN LIN ADDR		R

Bit 0 Reserved

Bits 2-1 BIG ENDIAN LIN ADDR - Big Endian Data Byte swap (linear addressing only)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Reserved

Bits 4-3 MMIO SELECT
00 = Disable MMIO
01 = New MMIO (relocatable) enabled (Default for PCI)
10 = Trio64-type MMIO enabled at window selected by bit 5 of this register
11 = Trio64-type MMIO and new MMIO enabled

Refer to the MMIO explanation in Section 16 for more information.

Bit 5 MMIO WIN - Trio64-type MMIO Window
0 = Trio64-type MMIO window enabled at A8000H - AFFFFH. A0000H - A7FFF available for image transfers (Default)
1 = Trio64-type MMIO window enabled at B8000H - BFFFFH. A0000H - B7FFFH are not used (no image transfer area)

Bits 4-3 of this register must be programmed to 10b for this bit to be effective.

Bit 6 SWP NBL - Swap Nibbles
0 = No nibble swap (Default)
1 = Swap nibbles in each byte of a linear memory address read or write operation

Bit 7 Reserved

Extended Memory Control 2 Register (CR54)

Read/Write Address: 3?5H, Index 54H
Power-On Default: 00H

7	6	5	4	3	2	1	0
M PARAMETER					M	BIG ENDIAN	

Bits 1–0 BIG ENDIAN - Big Endian Data Byte Swap (not linear addressing or image writes)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Swap according to $\overline{BE[3:0]}$ (VL-Bus) or $\overline{C/BE[3:0]}$ (PCI)

Byte enable settings for a bit setting of 11b:
0000 = Swap all bytes in doublewords (bytes reversed)
0011 = Swap bytes within selected word
1100 = Swap bytes within selected word
All other values = no swap

Bits 2, 7–3 M PARAMETER
6-bit Value = maximum number of MCLKs that the CPU and Graphics Engine can use to access memory before giving up control of the memory bus. Bit 2 is the high order bit of this value. The M parameter for LBP accesses is specified in CR76_5-0.

Extended RAMDAC Control Register (CR55)

Read/Write Address: 3?5H, Index 55H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	MS /X11	R	R	R	R

Bits 3–0 Reserved

Bit 4 MS/X11 - Hardware Cursor MS/X11 Mode
0 = MS-Windows mode (Default)
1 = X11-Windows mode

This bit select the type of decoding used for the 64x64x2 storage array of the hardware graphics cursor. See the Programming the Hardware Cursor section for a description of the decoding.

Bits 7–5 Reserved

External Sync Control 1 Register (CR56)

Read/Write Address: 3?5H, Index 56H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	DIS VSYN	DIS HSYN	R

Bit 0 Reserved

Bit 1 DIS HSYN - Tri-state off HSYNC
0 = HSYNC output buffer tri-stated on
1 = HSYNC output buffer tri-stated off

Bit 2 DIS VSYN - Tri-state off VSYNC
0 = VSYNC output buffer tri-stated on
1 = VSYNC output buffer tri-stated off

Bits 7–3 Reserved

Linear Address Window Control Register (CR58)

Read/Write Address: 3?5H, Index 58H
Power-On Default: 10H

7	6	5	4	3	2	1	0
RAS PRE	R	R	ENB LA	R	R	LAW-SIZE 1	0

Bits 1–0 LAW-SIZE - Linear Address Window Size
00 = 64 KBytes (Default)
01 = 1 MByte
10 = 2 MBytes
11 = Reserved

The 64K window is not available if new MMIO is enabled (CR53_3 = 1).

Bits 3-2 Reserved

Bit 4 ENB LA - Enable Linear Addressing
0 = Disable linear addressing
1 = Enable linear addressing (Default)

Enabling linear addressing disables access to the A000H-AFFFH region unless banking is enabled via bit 0 of CR31, the window size is set to 64K via bits 1-0 of this register and A000H is specified as the base in CR59-5A.

Bits 6–5 Reserved

Bit 7 RAS PRE - RAS Pre-charge Time Adjust
0 = $\overline{RAS}$ pre-charge (high) time is defined by CR68_3 or MM81EC_16 (Default)
1 = $\overline{RAS}$ pre-charge (high) time is decreased by 0.5 MCLKs over that specified by CR68_3 and the corresponding $\overline{RAS}$ low time (CR68_2) is increased by 0.5 MCLKs. This leaves the total cycle time unchanged.

Linear Address Window Position Registers (CR59-5A)

Read/Write Address: 3?5H, Index 59H-5AH
Power-On Default: 0000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LINEAR-ADDRESS-WINDOW-POSITION															

CR59 contains the upper byte (15-8) and CR5A contains the lower byte (7-0). These registers specify the Linear Address Window Position in 32-bit CPU address space. The Linear Address Window resides on a 64KB, 1MB or 2MB memory boundary (size-aligned boundary). Some LSBs of this register (illustrated by "xx..xx" in the following table) are ignored because of the size-aligned boundary scheme.

LAW Size	Linear Address Window Position Register Bit(s)									
64KB	31-25	24	23	22	21	20	19	18	17	16
1MB	31-25	24	23	22	21	20	xx	xx	xx	xx
2MB	31-25	24	23	22	21	xx	xx	xx	xx	xx

Bits 15–0 LINEAR-ADDRESS-WINDOW-POSITION - LA Window Position Bits 31-16
16-bit Value = the linear address window position in 32-bit CPU address space.

Bits 31-23 are common with bits 31-23 of the base address programmed into the PCI Base Address 0 register at address 10H-12H. Writes to these bits in either register will also be written to the other. In general, the bits should be programmed via the PCI configuration register. Writes to CR59 and CR5A should be read-modify- writes that do not change bits 31-23.

If a 64K window is specified and bit 0 of CR31 is set to 1, bits 5-0 of CR6A specify the 64K page of display memory to be accessed through a 64K window located at the address specified in these registers.

If new MMIO is enabled (CR53_3 = 1), the address is taken from bits 31-26 (CR59_7-2) or the high order 6 bits of the PCI Base Address 0 register. This is concatenated with the display memory address specified by the programmer.

General Output Port Register (CR5C)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 5CH

7	6	5	4	3	2	1	0
GENERAL-OUT-PORT							

Bits 7–0 GENERAL-OUT-PORT

This register can be used in a variety of ways. See Section 13 for a complete description.

Extended Horizontal Overflow Register (CR5D)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 5DH
Paired

7	6	5	4	3	2	1	0
R	SFF 8	EHS 6	SHS 8	EHB 7	SHB 8	HDE 8	HT 8

Bit 0 HT 8 - Horizontal Total (CR0) Bit 8

Bit 1 HDE 8 - Horizontal Display End (CR1) Bit 8

Bit 2 SHB 8 - Start Horizontal Blank (CR2) Bit 8

Bit 3 EHB 7 - End Horizontal Blank (CR3) Bit 6

Bit 4 SHS 8 - Start Horizontal Sync Position (CR4) Bit 8

Bit 5 EHS 6 - End Horizontal Sync (CR5) Bit 6

Bit 6 SFF 8 - Start FIFO Fetch (CR3B) Bit 8

Bit 7 Reserved

Extended Vertical Overflow Register (CR5E)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 5EH
Paired

7	6	5	4	3	2	1	0
R	LCM 10	R	VRS 10	R	SVB 10	VDE 10	VT 10

Bit 0 VT 10 - Vertical Total (CR6) Bit 10

Bit 1 VDE 10 - Vertical Display End (CR12) Bit 10

Bit 2 SVB 10 - Start Vertical Blank (CR15) Bit 10

Bit 3 Reserved

Bit 4 VRS 10 - Vertical Retrace Start (CR10) Bit 10

Bit 5 Reserved

Bit 6 LCM 10 - Line Compare Position (CR18) Bit 10

Bit 7 Reserved

Extended Memory Control 3 Register (CR60)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 60H

7	6	5	4	3	2	1	0
PRIMARY STREAM FIFO N PARAMETER							

Bits 7-0 PRIMARY STREAM FIFO N PARAMETER
Value = Number of MCLKs allocated to screen refresh FIFO filling before control of the memory bus is relinquished. This value is effective only when the FIFO is at or above its threshold value (low priority).

Extended Memory Control 4 Register (CR61)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 61H

7	6	5	4	3	2	1	0
R	BIG ENDIAN		R	R	R	R	R

Bits 4-0 Reserved

Bits 6-5 BIG ENDIAN - Big Endian Data Bye Swap (image writes only)
00 = No swap (Default)
01 = Swap bytes within each word
10 = Swap all bytes in doublewords (bytes reversed)
11 = Reserved

Bit 7 Reserved

Start FIFO Fetch Register (CR63)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 63H
Paired

7	6	5	4	3	2	1	0
R	R	R	FIFO FETCH		R	R	R

Bits 2-0 Reserved

Bits 4-3 FIFO FETCH - Start Display FIFO Fetch
00 = Start FIFO fetch on falling edge of the internal HSYNC signal
01 = Start FIFO fetch at horizontal total (CR34_4 = 0) or at value programmed in CR3B (CR34_4 = 1)
10 = Start FIFO fetch on rising edge of the internal HSYNC signal delayed by 4 character clocks
11 = Start FIFO fetch on rising edge of the internal HSYNC signal delayed by 6 character clocks

Bits 7-5 Reserved

Extended Miscellaneous Control Register (CR65)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 65H
Paired

7	6	5	4	3	2	1	0
			DLY BLANK				
R	R	R	1	0	R	R	R

Bits 2-0 Reserved

Bits 4-3 DLK BLANK - Delay $\overline{\text{BLANK}}$ by DCLK
00 = No delay of $\overline{\text{BLANK}}$
01 = Delay $\overline{\text{BLANK}}$ for 1 DCLK
10 = Delay $\overline{\text{BLANK}}$ for 2 DCLKs (required for color mode 12)
11 = Delay $\overline{\text{BLANK}}$ for 3 DCLKs

Bits 7-5 Reserved

Extended Miscellaneous Control 1 Register (CR66)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 66H

7	6	5	4	3	2	1	0
PCI DE	R	R	R	PCI DIS	R	SW RST	EN ENH

Bit 0 EN ENH - Enable Enhanced Functions
0 = Disable enhanced functions
1 = Enable enhanced functions

This bit is a duplicate of 4AE8_0. Writing to this location also update the bit value at the other location.

Note: This bit is paired.

Bit 1 SW RST - Software Reset
0 = No function
1 = Software reset of the Graphics Engine

Setting this bit has the same function as setting 42E8H (write)_15-14 to 10b.

Bit 2 Reserved

Bit 3 PCI DIS - PCI Disconnect
0 = No effect
1 = An attempt to write data with the Command FIFO or LPB output FIFO full or to read data with the Command FIFO not empty generates a PCI bus disconnect cycle

Bit 7 of this register must also be set to 1 to enable this feature.

Bits 6-4 Reserved

Bit 7 PCI DE - PCI bus disconnect enable
0 = PCI bus disconnect disabled
1 = PCI bus disconnect enabled

Setting this bit to 1 allows PCI burst cycles to be interrupted if AD[1:0] ≠ 00b or if the address during the burst goes outside the address ranges supported by the 86CM65. See also bit 3 of this register.

Extended Miscellaneous Control 2 Register (CR67)

Read/Write
Power-On Default: 00H
Address: 3?5H, Index 67H
Paired

7	6	5	4	3	2	1	0
COLOR MODE				STREAMS MODE			VCLK PHS
3	2	1	0			R	

Bit 0 VCLK PHS - VCLK Phase With Respect to DCLK
0 = VCLK is 180° out of phase with DCLK (inverted)
1 = VCLK is in phase with DCLK

Bit 1 Reserved

Bits 3–2 STREAMS MODE
00 = Streams Processor disabled
01 = Secondary stream overlaid on VGA mode background
10 = Reserved
11 = Full Streams Processor operation (primary and secondary streams from all supported sources)

The Streams Processor should only be enabled or disabled during the VSYNC period.

Bits 7–4 COLOR MODE - RAMDAC Color Mode
0000 = Mode 0: 8-bit color, 1 pixel/VCLK
0001 = Mode 8: 8-bit color, 2 pixels/VCLK
0011 = Mode 9: 15-bit color, 1 pixel/VCLK
0101 = Mode 10: 16-bit color, 1 pixel/VCLK
0111 = Mode 12: 640x480x24-bit color (packed), 1 pixel/VCLK
1101 = Mode 13: 24-bit color, (not packed) 1 pixel/VCLK

All other mode values are reserved.

Configuration 3 Register (CR68)

Read/Write Address: 3?5H, Index 68H
Power-On Default: Depends on Strapping

This is of the power-on strapping bits (along with CR36, CR37 and CR6F) . PD[23:16] are sampled on power-on reset and their states are written to bits 7-0 of this register. These pins have internal pull-downs and the states of pins are inverted, so this register will default to FFH if no pins are pulled up. A5H must be written to CR39 to provide read/write access to this register.

7	6	5	4	3	2	1	0
		BIOS		RAS -	RAS -		
R	3	2	1	PCG	LOW	CAS/OE STR	

Bits 1-0 $\overline{CAS}$,$\overline{OE}$ Stretch Time
00 = approximately 6.5 ns stretch (nominal)
01 = approximately 5 ns stretch (nominal)
10 = approximately 3.5 ns stretch (nominal)
11 = no stretch

This parameter adjusts the timing for the rising edges of the $\overline{CAS}$ and $\overline{OE}$ signals. This allows stretching of the signal active time for $\overline{CAS}$ and $\overline{OE}$ to allow more time for valid pixel data to be available. The delay time shown above is an approximation. It is affected by both process and signal loading and must be measured for each design.

Bit 2 $\overline{RAS}$-LOW - $\overline{RAS}$ Low Timing Select
0 = 4.5 MCLKs
1 = 3.5 MCLKs

This parameter specifies the length of the $\overline{RAS}$ active time for a single row/column access. $\overline{RAS}$ may be held low longer to accommodate additional page mode accesses to the same row.

Bit 3 $\overline{RAS}$-PCG - $\overline{RAS}$ Precharge Timing Select
0 = 3.5 MCLKs
1 = 2.5 MCLKs

When $\overline{RAS}$ goes high to end a memory cycle, this parameter specifies the minimum period it must be held high before beginning another memory access cycle.

Bits 6-4 BIOS - Reserved for use by the video BIOS.

Bit 7 Reserved

Extended System Control 3 Register (CR69)

Read/Write — Address: 3?5H, Index 69H
Power-On Default: 00H — Paired

7	6	5	4	3	2	1	0
R	R	R	R	R	DISP-START-ADDR		

Bits 2–0 DISP-START-ADDR
This field contains the upper 3 bits (18-16) of the display start address, allowing addressing of up to 2 MBytes of display memory.

Bits 7–3 Reserved

Extended System Control 4 Register (CR6A)

Read/Write — Address: 3?5H, Index 6AH
Power-On Default: 00H — Paired

7	6	5	4	3	2	1	0
R	R	R	CPU-BASE-ADDRESS				

Bits 4–0 CPU-BASE-ADDRESS
This field contains the upper 5 bits (18-14) of the CPU base address, allowing accessing of up to 2 MBytes of display memory via 64K pages. If linear addressing is enabled and a 64 KByte window is specified, these bits specify the 64K page to be accessed at the base address specified in CR59 and CR5A. Otherwise, the base address is normally at A000H.

Bits 7–5 Reserved

Extended BIOS Flag 3 Register (CR6B)

Read/Write Address: 3?5H, Index 6BH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-3							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-3
This register is reserved for use by the S3 BIOS.

Extended BIOS Flag 4 Register (CR6C)

Read/Write Address: 3?5H, Index 6CH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-4							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-4
This register is reserved for use by the S3 BIOS.

Extended BIOS Flag 5 Register (CR6D)

Read/Write Address: 3?5H, Index 6DH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-5							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-5
This register is reserved for use by the S3 BIOS.

Extended BIOS Flag 6 Register (CR6E)

Read/Write Address: 3?5H, Index 6EH
Power-On Default: 00H

7	6	5	4	3	2	1	0
EXT-BIOS-FLAG-REGISTER-6							

Bits 7–0 EXT-BIOS-FLAG-REGISTER-6
This register is reserved for use by the S3 BIOS.

Configuration 4 Register (CR6F)

Read/Write Address: 3?5H, Index 6FH
Power-On Default: Depends on Strapping

This is the fourth byte of power-on strapping bits. PD[28:24] are sampled at reset and the values are written to bits 4-0 of this register. A5H must be written to CR39 to provide read/write access to this register. Non-reserved bits will power up with a value of 1 if the corresponding pins are not pulled high.

7	6	5	4	3	2	1	0
R	R	R	WE DELAY		IOEN	IOSEL	R

Bit 0 Reserved

Bit 1 IOSEL - Serial Port I/O Address Select
0 = MMFF20 is accessed at I/O address 000E8H
1 = MMFF20 is accessed at I/O address 000E2H

Bit 2 of this register must be cleared to 0 for this bit to have effect.

Bit 2 IOEN - Serial Port Address Type Select
0 = MMFF20 is accessed at the I/O port defined in bit 1 of this register or at its MMIO address
1 = MMFF20 is accessed at its MMIO address only (no I/O)

Enabling I/O access allows the serial port to be used for I^2C communications when the 86CM65 is disabled.

Bits 4-3 WE Delay
00 = 3 units delay
01 = 2 units delay
10 = 1 unit delay
11 = 0 units delay

Both the rising and falling edges of $\overline{WE}$ are delayed by the amount specified in these bits.

Bits 7-5 Reserved

Dual Image Control Register (CR71)

Read/Write
Power-On Default: 00H

Address: 3?5H, Index 71H
Paired

7	6	5	4	3	2	1	0
R	R	SOFF	R	R	R	SOC	R

Bit 0 Reserved

Bit 1 SOC - Screen Off Control
0 = Use SR1_5 for screen off control
1 = Use CR71_5 for screen off control

SR1_5 is a shared bit, so both screens have to be on or off if this bit is used. CR71_5 is paired, allowing independent on/off selection for each screen.

Bits 4-2 Reserved

Bit 5 SOFF - Screen Off
0 = Screen on
1 = Screen off

This is the same as blanking. The control signals are still active.

Bits 7-6 Reserved

Extended Memory Control 5 Register (CR72)

Read/Write) Address: 3?5H, Index 72H
Power-On Default: 00H

7	6	5	4	3	2	1	0
SECONDARY STREAM FIFO N PARAMETER							

Bits 7-0 SECONDARY STREAM FIFO N PARAMETER
Value = Number of MCLKs allocated to screen refresh FIFO filling before control of the memory bus is relinquished. This value is effective only when the FIFO is at or above its threshold value (low priority).

Extended Memory Control 6 Register (CR73)

Read/Write) Address: 3?5H, Index 73H
Power-On Default: 00H

7	6	5	4	3	2	1	0
MIUS	CONTROLLER 2 FIFO N PARAMETER						

Bits 6-0 CONTROLLER 2 FIFO N PARAMETER
Value = Number of MCLKs allocated to screen refresh FIFO filling before control of the memory bus is relinquished. This value is effective only when the FIFO is at or above its threshold value (low priority) as specified in SR29_7-6.

Bit 7 MIUS - MIU Synchronization
0 = synchronize Memory Interface Unit (MIU) control registers every MCLK rising edge
1 = synchronize MIU control registers on the first MCLK rising edge after every falling edge of CLK32 (32 KHz clock).

The MIU control registers are written using SCLK. They must then be synchronized to MCLK. Setting this bit to 1 causes this synchronization to occur less frequently, thereby reducing power consumption.

Extended Memory Control 7 Register (CR74)

Read/Write) Address: 3?5H, Index 73H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	R	R	R	SFR	R	R

Bits 1-0 Reserved

Bit 2 SFR - SNT FIFO Rate
0 = 2 MCLK STN FIFO reads/writes
1 = 1 MCLK STN FIFO reads/writes for 1-cycle EDO operation (CR36_3-2 = 00b)

Extended Memory Control 8 Register (CR75)

Read/Write) Address: 3?5H, Index 75H
Power-On Default: 00H

7	6	5	4	3	2	1	0
STN FIFO N PARAMETER							

Bits 7-0 STN FIFO N PARAMETER
Value = Number of MCLKs allocated to screen refresh FIFO filling before control of the memory bus is relinquished. This value is effective only when the FIFO is at or above its threshold value (low priority) as specified in SR29.

Extended Memory Control 9 Register (CR76)

Read/Write) Address: 3?5H, Index 76H
Power-On Default: 00H

7	6	5	4	3	2	1	0
R	R	LPB M PARAMETER					

Bits 5-0 LPB M PARAMETER

Value = maximum number of MCLKs that the LPB can use to access memory before giving up control of the memory bus.

Bits 7-6 Reserved

Section 20: Enhanced Commands Register Descriptions

These registers support the Enhanced mode drawing commands. Access to these registers is enabled via bit 0 of the System Configuration register (CR40).

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Subsystem Status Register

Read Only Address: 42E8H
Power-On Default: 0000H

This read-only register provides information on interrupt status, monitor I.D. and the number of bits per pixel. See the Subsystem Control (42E8H, Write Only) register for details on enabling and clearing interrupts.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	PXL LNG	R	R	R	FIFO EMP	FIFO OVF	GE BSY	VSY INT

Bit 0 VSY INT - Vertical Sync Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 1 GE BSY - Graphics Engine Busy Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 2 FIFO OVF - Command FIFO Overflow Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bit 3 FIFO EMP - Command FIFO Empty Interrupt Status
0 = No interrupt
1 = Interrupt generated if enabled

Bits 4–6 Reserved

Bit 7 PXL LNG - Pixel Length (# of bit planes)
0 = 4-bit
1 = 8-bit

This reflects the number of bit planes when CR50_5-4 = 00b.

Bits 15-8 Reserved

Subsystem Control Register

Write Only Address: 42E8H
Power-On Default: 0000H

This register allows each of several interrupt sources to be enabled or disabled. Interrupt status (Subsystem Status (42E8H, Read Only) can be cleared. This register also controls the software reset of the graphics engine.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GE-RST				FIFO-ENB		GE	VSY					FIFO	FIFO	GEB	VSY
1	0	R	R	EMP	OVF	BSY	ENB	R	R	R	R	CLE	CLO	CLR	CLR

Bit 0 VSY CLR - Clear Vertical Sync Interrupt Status
0 = No change
1 = Clear

Bit 1 GEB CLR - Clear Graphics Engine Busy Interrupt Status
0 = No change
1 = Clear

Bit 2 FIFO CLO - Clear Command FIFO Overflow Interrupt Status
0 = No change
1 = Clear

Bit 3 FIFO CLE - Clear Command FIFO Empty Interrupt Status
0 = No change
1 = Clear

Bits 7–4 Reserved

Bit 8 VSY ENB - Vertical Sync Interrupt Enable
0 = Disable
1 = Enable if CR32_4 = 1

Bit 9 GE BSY- Graphics Engine Busy Interrupt Enable
0 = Disable
1 = Enable if CR32_4 = 1

Bit 10 FIFO-ENB OVF - Command FIFO Overflow Interrupt Enable
0 = Disable
1 = Enable if CR32_4 = 1

Bit 11 FIFO-ENB EMP - Command FIFO Empty Interrupt Enable
0 = Disable
1 = Enable if CR32_4 = 1

Bits 13–12 Reserved

Bits 15–14 GE-RST - Graphics Engine Software Reset
00 = No change
01 = Graphics Engine enabled
10 = Reset
11 = Reserved

Advanced Function Control Register

Read/Write Address: 4AE8H
Power-On Default: 0000H

This register enables or disables the Enhanced display functions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	LA	R	ENH PL	R	ENB EHFC

Bit 0 ENB EHFC - Enable Enhanced Functions
0 = Enable VGA and VESA planar (4 bits/pixel) modes
1 = Enable all other modes (Enhanced and VESA non-planar)

Bit 1 Reserved

Bit 2 ENH PL - Enhanced mode pixel length
0 = 4 bits/pixel enhanced mode
1 = 8 or more bits/pixel enhanced mode

CR50_5-4 are used to differentiate between 8-, 16- and 32-bit pixel lengths.

Bit 3 Reserved

Bit 4 LA - Enable Linear Addressing
0 = Disable linear addressing
1 = Enable linear addressing

This bit is ORed with bit 4 of CR58 and is equivalent to it.

Bits 15–5 Reserved

Current Y-Position Register

Read/Write Address: 82E8H
Power-On Default: Undefined

For line draws (solid, textured, short stroke or polyline), rectangle draws and image transfers, writing to this register defines the vertical screen coordinate at which the first pixel will be drawn. For BitBLTs, this is the vertical coordinate for the upper left hand corner of the destination. For PatBLTs, this is the vertical coordinate of the upper left hand corner of the off-screen pattern. Reading this register produces the current vertical drawing coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CURRENT Y-POSITION											

Bits 11–0 CURRENT Y-POSITION

Bits 15–12 Reserved

Current X-Position Register

Read/Write Address: 86E8H
Power-On Default: Undefined

For line draws (solid, textured, short stroke or polyline), rectangle draws and image transfers, writing to this register defines the horizontal screen coordinate at which the first pixel will be drawn. For BitBLTs, this is the horizontal coordinate for the upper left hand corner of the destination. For PatBLTs, this is the horizontal coordinate of the upper left hand corner of the off-screen pattern. Reading this register produces the current horizontal drawing coordinate.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	CURRENT X-POSITION											

Bits 11–0 CURRENT X-POSITION

Bits 15–12 Reserved

Destination Y-Position/Axial Step Constant Register

Read/Write Address: 8AE8H
Power-On Default: Undefined

For BitBLTs and PatBLTs, this register defines the vertical position for the top of the destination rectangle. For solid and textured line draws, this is axial step constant used in the definition of the line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DESTINATION Y-POSITION											

Bits 11–0 DESTINATION Y-POSITION

Bits 15–12 Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER AXIAL STEP CONSTANT													

Axial Step Constant = 2 * (min(|dx|,|dy|)) In other words, when drawing a line from point A to point B, determine the change in the X coordinate from A to B and the change in the Y coordinate from A to B. Take the smaller of the two changes and multiply its absolute value by 2.

Bits 13–0 LINE PARAMETER AXIAL STEP CONSTANT

Bits 15–14 Reserved

Destination X-Position/Diagonal Step Constant Register

Read/Write Address: 8EE8H
Power-On Default: Undefined

For BitBLTs and PatBLTs, this register defines the horizontal position for the left side of the destination rectangle. For solid and textured line draws, this is diagonal step constant used in the definition of the line.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DESTINATION X-POSITION											

Bits 11–0 DESTINATION X-POSITION

Bits 15–12 Reserved

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER DIAGONAL STEP CONSTANT													

Diagonal Step Constant = 2 * [min(|dx|,|dy|) - max(|dx|,|dy|)]. See the Destination Y-Position/Axial Step Constant (8AE8H) register for an explanation of the terms used in this equation.

Bits 13–0 LINE PARAMETER DIAGONAL STEP CONSTANT

Bits 15–14 Reserved

Line Error Term Register

Read/Write Address: 92E8H
Power-On Default: Undefined

This register specifies the initial error term for solid and textured line draws.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LINE PARAMETER/ERROR TERM													

Error Term = 2 * min(|dx|,|dy|) - max(|dx|,|dy| - 1 if the starting X < the ending X
Error Term = 2 * min(|dx|,|dy|) - max(|dx|,|dy| if the starting X ≥ the ending X

See the Destination Y-Position/Axial Step Constant (8AE8H) register for an explanation of the terms used in these equations.

Bits 13–0 LINE PARAMETER/ERROR TERM

Bits 15–14 Reserved

Major Axis Pixel Count Register

Read/Write Address: 96E8H
Power-On Default: Undefined

This register specifies the length (in pixels) of the major (longest) axis for solid and textured lines and the width for rectangles, image transfers, BitBLTs and PatBLTs.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	RECTANGLE WIDTH/LINE PARAMETER MAX											

Bits 11–0 RECTANGLE WIDTH/LINE PARAMETER MAX
The value is the number of pixels along the major axis - 1.

Bits 15–12 Reserved

Graphics Processor Status Register

Read Only Address: 9AE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO-STATUS						HDW		FIFO-STATUS							
9	10	11	12	13	AE	BSY	R	1	2	3	4	5	6	7	8

Bits 7–0 FIFO-STATUS

In the following table, the leftmost column represents the value of FIFO status bit 1 (register bit 7). Each column to the right represents the value of the next higher FIFO status bit. A value of 0 read from any particular status bit position guarantees at least as many open FIFO slots as the number of that status bit. For example, if a 0 is read from status bit 6 (register bit 2), there are at least 6 open FIFO slots. Bits 15-11 provide the upper 5 FIFO status bits.

0000000000000 = 13 FIFO slots available
0000000000001 = 12 FIFO slots available
0000000000011 = 11 FIFO slots available
0000000000111 = 10 FIFO slots available
0000000001111 = 9 FIFO slots available
0000000011111 = 8 FIFO slots available
0000000111111 = 7 FIFO slots available
0000001111111 = 6 FIFO slots available
0000011111111 = 5 FIFO slots available
0000111111111 = 4 FIFO slots available
0001111111111 = 3 FIFO slots available
0011111111111 = 2 FIFO slots available
0111111111111 = 1 FIFO slots available
1111111111111 = 0 FIFO slots available

Bit 8 Reserved

Bit 9 HDW BSY - Hardware (Graphics Engine) Busy
0 = not busy
1 = busy - graphics command is executing

Bit 10 AE - All FIFO Slots Empty
0 = At least one FIFO slot is occupied
1 = All FIFO slots empty

Bits 15–11 FIFO-STATUS
These are the upper 5 bits of the FIFO status. See bits 7-0 for the interpretation.

Drawing Command Register

Write Only Address: 9AE8H
Power-On Default: Undefined

This register specifies the drawing command and a number of associated control parameters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CMD-TYPE			BYTE		BUS SIZE		WAIT	DRWG-DIR.			DRAW	DIR	LAST	PX	
2	1	0	SWP	R	1	0	YES	2	1	0	YES	TYP	POF	MD	= 1

Bit 0 This bit must always be programmed to 1.

Bit 1 PX MD - Select Across the Plane Pixel Mode
0 = Single pixel transferred at a time
1 = Multiple pixels transferred at a time (across the plane mode)

Bit 2 LAST POF - Last Pixel Off
0 = Last pixel of line or vector draw will be drawn
1 = Last pixel of line or vector draw will not be drawn

Bit 3 DIR TYP - Select Radial Direction Type
0 = x-y (axial)
1 = Radial

Bit 4 DRAW YES - Draw Pixel
0 = Move the current position only - don't draw
1 = Draw pixel(s)

Bits 7–5 DRWG-DIR - Select Drawing Direction
In the following table, radial drawing angle is measured counterclockwise from the X axis. For axial line draws, the line is drawn from left to right or a +X and from right to left for a -X, down for a +Y and up for a -Y. X or Y maj specifies the longest axis.

7–5	Radial (bit 3 = 1)	x-y (Axial - bit 3 = 0)
000	0°	–Y,X maj,–X
001	45°	–Y,X maj,+X
010	90°	–Y,Y maj,–X
011	135°	–Y,Y maj,+X
100	180°	+Y,X maj,–X
101	225°	+Y,X maj,+X
110	270°	+Y,Y maj,–X
111	315°	+Y,Y maj,+X

Bit 8 WAIT YES - Wait for CPU Data
0 = Use Graphics Engine-based data
1 = Wait for data to be transferred to or from the CPU through the E2E8H port

Bits 10–9 BUS SIZE - Select image write (E2E8H, E2EAH) bus transfer width
00 = 8 bits
01 = 16 bits
10 = 32 bits. All doubleword bits beyond the image rectangle width are discarded. Each line starts with a fresh doubleword. The current drawing position ends up one pixel below the lower left hand corner of the image rectangle.
11 = 32 bits. This setting applies only to image transfers across the plane (each bit transferred is converted to a pixel). Only bits from the end of the line width to the next byte boundary are discarded. Data for the next line begins with the next byte. The current drawing position ends up one pixel to the right of the top right corner of the image rectangle.

This parameter applies only to writing data through the Pixel Data Transfer (E2E8H, E2EAH) registers (programmed I/O or memory-mapped I/O).

Bit 11 Reserved

Bit 12 BYTE SWP - Enable Byte Swap
0 = High byte first, low byte second
1 = Low byte first, high byte second

Bits 15–13 CMD-TYPE - Select Command Type

000 = NOP. This is used to set up short stroke vector drawing without writing a pixel.
001 = Draw Line. If bit 3 of this register is cleared to 0, the axial step constant, diagonal step constant and error term are used to draw the line. If bit 3 is set to 1, the line will be drawn at the angle specified by bits 7-5 and with a length in pixels as specified by the Major Axis Pixel Count (96E8H) register.
010 = Rectangle Fill. The position, width and height of a rectangle are defined. The rectangle is filled with a solid color if it not used for an image transfer.
110 = BitBLT. A rectangle of defined location, width and height is moved to another defined location in display memory.
111 = PatBLT. An 8x8 pixel patterned rectangle of defined location is transferred repeatedly to a destination rectangle of defined location, width and height. The pattern copy is always aligned to an 8 pixel boundary and transfers continue until the pattern is tiled into the entire destination rectangle. The starting X coordinate of the source pattern rectangle should always be on an 8 pixel boundary.

Short Stroke Vector Transfer Register

Write Only Address: 9EE8H
Power-On Default: Undefined

This register defines two short stroke vectors. These are drawn one at a time based on the setting of the BYTE SWAP bit (bit 12) in the Command (9AE8H) register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRWG-DIR			DRW	PIXEL-LENGTH				DRWG-DIR.			DRW	PIXEL-LENGTH			
2	1	0	-MV	3	2	1	0	2	1	0	-MV	3	2	1	0

Bits 3–0 PIXEL-LENGTH
Value = # pixels - 1

Bit 4 DRW -MV - Draw Pixel
0 = Move current position only - don't draw
1 = Draw pixel

Bits 7–5 DRWG-DIR.- Select Drawing Direction (measured counterclockwise from the X axis)
000 = 0°
001 = 45°
010 = 90°
011 = 135°
100 = 180°
101 = 225°
110 = 270°
110 = 315°

Bits 15–8 These bits duplicate bits 7-0 to define the second short stroke vector.

Background Color Register

Read/Write Address: A2E8H
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when this color value is used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BACKGROUND COLOR															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BACKGROUND COLOR															

Bits 31–0 BACKGROUND COLOR
If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Foreground Color Register

Read/Write Address: A6E8H
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when this color value is used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FOREGROUND COLOR															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FOREGROUND COLOR															

Bits 31–0 FOREGROUND COLOR
If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Bitplane Write Mask Register

Read/Write Address: AAE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE WRITE MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT-PLANE WRITE MASK															

Bits 31–0 BIT-PLANE WRITE MASK
If bit i = 0, bitplane i is not updated
If bit i = 1, bitplane i is updated

Bits 31-0 control planes 31-0 respectively. If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Bitplane Read Mask Register

Read/Write Address: AEE8H
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BIT-PLANE READ MASK															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIT-PLANE READ MASK															

Bits 31–0 BIT-PLANE READ MASK
If bit i = 0, bitplane i is not used as a data source
If bit i = 1, bitplane i is used as a data source

Bit-plane read mask for BitBLT and image transfer functions. Bits 31-0 control planes 31-0 respectively. If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Color Compare Register

Read/Write Address: B2E8H
Power-On Default: Undefined

This register contains the color value that is compared against the current bitmap color if the color compare option is turned on by setting bit 8 of the Pixel Control (BEE8H, Index 0EH) to 1. Bit 7 of the Pixel Control register determines whether a match or a non-match results in a pixel update.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMPARISON COLOR WITH SOURCE															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
COMPARISON COLOR WITH SOURCE															

Bits 31–0 COMPARISON COLOR WITH SOURCE
If bit 9 of BEE8_EH is set to 1 for programmed I/O (not MMIO), this becomes a 32-bit register. If bit 9 of BEE8_EH is cleared to 0, this is two 16-bit registers. In 32 bpp mode with 16-bit registers, the upper and lower doublewords are read or written sequentially, depending on the state of the RSF flag (bit 4 of BEE8H, Index EH). If RSF = 0, the lower 16 bits are accessed. If RSF = 1, the upper 16 bits are accessed. The RSF flag toggles automatically when a doubleword is read or written.

Background and Foreground Mix Registers

Read/Write Address: B6E8H (Background), BAE8H (Foreground)
Power-On Default: Undefined

See the Enhanced Mode Bitmap Accessing Through the Graphics Engine section in the Functional Description for a detailed explanation of how and when these registers are used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									CLR-SRC			MIX-TYPE			
R	R	R	R	R	R	R	R	R	1	0	R	3	2	1	0

Bits 3–0 MIX-TYPE - Select Mix Type
In the general case, a new color is defined. A logical operation such as AND or OR is then performed between it and the current bitmap color. If the bitplane to be written is enabled, the result of this logical "mix" is written to the bitmap as the new pixel color. The following table shows the mix types available (! = logical NOT).

0000	!current	1000	!current OR !new
0001	logical zero	1001	current OR !new
0010	logical one	1010	!current OR new
0011	leave current as is	1011	current OR new
0100	!new	1100	current AND new
0101	current XOR new	1101	!current AND new
0110	!(current XOR new)	1110	current AND !new
0111	new	1111	!current AND !new

Bit 4 Reserved

Bits 6–5 CLR-SRC - Select Color Source
00 = Background Color register is the color source
01 = Foreground Color register is the color source
10 = CPU data (the CPU is the color source)
11 = Display memory (the display memory is the color source)

Bits 15–7 Reserved

Read Register Data Register

Read Only Address: BEE8H
Power-On Default: Undefined

A read of this register produces a read of the register specified by bits 2-0 of the Read Register Select (BEE8H, Index 0FH) register. Each read of BEE8H causes the read index (bits 2-0 of BEE8H, Index 0FH) to increment by one. Registers BEE8H, Indices 0H to 0EH, 9AE8H and 42E8H can thus be rapidly read by successive reads from BEE8H.

Note: Writes to the BEE8H registers (except the read index register, Index 0FH) are pipelined. Therefore, to correctly read back a write to one of these registers, issue a NOP drawing command (a write to 9AE8H with bits 15-13 programmed to 000b) immediately after the BEE8H register write. Next, write the desired register index to BEE8H, Index 0FH and read the data from BEE8H.

The BEE8H registers are written directly by writing to BEE8H with the appropriate register index in bits 15-12.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Minor Axis Pixel Count Register

Write Only Address: BEE8H, Index 0H
Power-On Default: Undefined

This register specifies the height for rectangles, image transfers, BitBLTs and PatBLTs.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	RECTANGLE HEIGHT											

Bits 11–0 RECTANGLE HEIGHT
Value = (number of pixels in the height of the rectangle) - 1

Bits 15–12 INDEX = 0H

Top Scissors

Write Only Address: BEE8H, Index 1H
Power-On Default: Undefined

This register specifies the top of the clipping rectangle. It is the lowest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	CLIPPING TOP LIMIT											

Bits 11–0 CLIPPING TOP LIMIT

Bits 15–12 INDEX = 1H

Left Scissors

Write Only Address: BEE8H, Index 2H
Power-On Default: Undefined

This register specifies the left side of the clipping rectangle. It is the lowest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	CLIPPING LEFT LIMIT											

Bits 11–0 CLIPPING LEFT LIMIT

Bits 15–12 INDEX = 2H

Bottom Scissors

Write Only Address: BEE8H, Index 3H
Power-On Default: Undefined

This register specifies the bottom of the clipping rectangle. It is the highest Y value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	CLIPPING BOTTOM LIMIT											

Bits 11–0 CLIPPING BOTTOM LIMIT

Bits 15–12 INDEX = 3H

Right Scissors

Write Only Address: BEE8H, Index 4H
Power-On Default: Undefined

This register specifies the right side of the clipping rectangle. It is the highest X value that will be drawn.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	CLIPPING RIGHT LIMIT											

Bits 11–0 CLIPPING RIGHT LIMIT

Bits 15–12 INDEX = 4H

Pixel Control Register

Write Only Address: BEE8H, Index 0AH
Power-On Default: Undefined

See Bitmap Access Through the Graphics Engine in the Enhanced Mode Programming section for an explanation of how and when bits 7-6 of this register are used when writing a pixel to display memory.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DT-EX-SRC							
1	0	1	0	R	R	R	R	1	0	R	R	R	R	R	R

Bits 5–0 Reserved

Bits 7–6 DT-EX-SRC - Select Mix Register
00 = Foreground Mix register is always selected
01 = Reserved
10 = CPU data determines Mix register selected
11 = Display memory current value determines Mix register selected

Bits 11–8 Reserved

Bits 15–12 INDEX = 0AH

Multifunction Control Miscellaneous 2 Register

Write Only Address: BEE8H, Index 0DH
Power-On Default: D000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
=1	=1	=0	=1	=0	=0	=0	=0	=0	SRC-BASE			=0	DST=BASE		

Bits 2–0 DST-BASE - Destination Base Address
000 = First destination memory address is in the 1st MByte of display memory
001 = First destination memory address is in the 2nd MByte of display memory
010 = First destination memory address is in the 3rd MByte of display memory
011 = First destination memory address is in the 4th MByte of display memory

This field supersedes bits 1-0 of BEE8H, Index E if any of these 3 bits are set to 1.

Bit 3 Reserved

Bits 6–4 SRC-BASE - Source Base Address
000 = First source memory address is in the 1st MByte of display memory
001 = First source memory address is in the 2nd MByte of display memory
010 = First source memory address is in the 3rd MByte of display memory
011 = First source memory address is in the 4th MByte of display memory

This field supersedes bits 3-2 of BEE8H, Index E if any of these three bits are set to 1.

Bits 11–7 Reserved

Bits 15–12 INDEX = 0DH

Multifunction Control Miscellaneous Register

Write Only
Address: BEE8H, Index 0EH
Power-On Default: E000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	R	1C EDO	CMR 32B	ENB CMP	SRC NE	R	EXT CLIP	RSF	SRC-BA 21	20	DEST-BA 21	20

Bits 1–0 DEST-BA 21 20 - Destination Base Address Bits 21-20
00 = First destination memory address is in the 1st MByte of display memory
01 = First destination memory address is in the 2nd MByte of display memory
10 = First destination memory address is in the 3rd MByte of display memory
11 = First destination memory address is in the 4th MByte of display memory

This field is superseded by bits 2-0 of BEE8H, Index D if any of the BEE8H Index D bits is set to 1.

Bits 3–2 SRC-BA 21 20 - Source Base Address Bits 21-20
00 = First source memory address is in the 1st MByte of display memory
01 = First source memory address is in the 2nd MByte of display memory
10 = First source memory address is in the 3rd MByte of display memory
11 = First source memory address is in the 4th MByte of display memory

This field is superseded by bits 6-4 of BEE8H Index D if any of the BEE8H Index D bits is set to 1.

Bit 4 RSF - Select Upper Word in 32 Bits/Pixel Mode
0 = Selects lower 16 bits for accesses to 32-bit registers in 32 bpp mode
1 = Selects upper 16 bits for accesses to 32-bit registers in 32 bpp mode

Bit 5 EXT CLIP - Enable External Clipping
0 = Only pixels inside the clipping rectangle are drawn
1 = Only pixels outside the clipping rectangle are drawn

Bit 6 Reserved

Bit 7 SRC NE - Don't Update Bitmap if Source Not Equal to Color Compare Color
0 = Don't update current bitmap if the Color Compare (B2E8) register value is equal to the color value of the source bitmap
1 = Don't update current bitmap if the Color Compare (B2E8) register value is not equal to the color value of the source bitmap

This bit is only active if bit 8 of this register is set to 1.

Bit 8 ENB CMP - Enable Color Compare
0 = Disable color comparison
1 = Enable color comparison

Bit 9 CMR 32B - Select 32-Bit Command Registers
0 = Command registers (A2E8H, A6E8H, AAE8H, AEE8H, B2E8H) are 16-bit
1 = Command registers (A2E8H, A6E8H, AAE8H, AEE8H, B2E8H) are 32-bit. Byte and word accesses cannot be made.

This bit applies to programmed I/O accesses only and is a don't care for MMIO accesses.

Bit 10 1C EDO - Disable 1-cycle EDO Operation
0 = Allow 1-cycle EDO operation
1 = Disable 1-cycle EDO operation

Bit 11 Reserved = 0

Bits 15–12 INDEX = 0EH

Read Register Select Register

Write Only Address: BEE8H, Index 0FH
Power-On Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	R	R	R	R	R	R	R	R	READ-REG-SEL			

Bits 3–0 READ-REG-SEL - Read Register Select

When BEE8H is read, the value returned is determined by this read register index according to the following:
0000 = BEE8H, Index 0H
0001 = BEE8H, Index 1H
0010 = BEE8H, Index 2H
0011 = BEE8H, Index 3H
0100 = BEE8H, Index 4H
0101 = BEE8H, Index 0AH
0110 = BEE8H, Index 0EH
0111 = 9AE8H (Bits 15-13 of the read data are forced to 0)
1000 = 42E8H (Bits 15-12 of the read data are forced to 0)
1001 = Reserved
1010 = BEE8H, Index 0DH

The read register index increments by one with each reading of BEE8H.

Bits 11–4 Reserved

Bits 15–12 INDEX = 0FH

Pixel Data Transfer Register

Write Only Address: E2E8H
Power-On Default: Undefined

All data from the CPU to the Graphics Engine must pass through this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMAGE WRITE DATA															

Bits 15–0 IMAGE WRITE DATA

Pixel Data Transfer - Extension Register

Write Only Address: E2EAH
Power-On Default: Undefined

This register is an extension of E2E8H for 32-bit operations.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IMAGE WRITE DATA															

Bits 15–0 IMAGE WRITE DATA

Section 21: Streams Processor Register Descriptions

Streams Processor registers can only be accessed via memory-mapped I/O. The register identifier MMxxxx means that this register is memory mapped at offset xxxx.

Primary Stream Control (MM8180)

Read/Write Address: 8180H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	PSFC			R	PSIDF			R	R	R	R	R	R	R	R

Bits 23-0 Reserved

Bits 26-24 PSIDF - Primary Stream Input Data Format
000 = RGB-8 (CLUT)
001 = Reserved
010 = Reserved
011 = KRGB-16 (1.5.5.5)
100 = Reserved
101 = RGB-16 (5.6.5)
110 = RGB-24 (8.8.8)
111 = XRGB-32 (X.8.8.8)

Bit 27 Reserved

Bits 30-28 PSFC - Primary Stream Filter Characteristics
000 = Primary stream
001 = Primary stream for 2X stretch (replication)
010 = Primary stream, bi-linear for 2X stretch (interpolation)
Other values reserved

Bit 31 Reserved

Color/Chroma Key Control (MM8184)

Read/Write Adds: 8184H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G/U/Cb KEY (LOW)								B/V/Cr KEY (LOW)							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	KC	R	RGB CC			R/Y KEY (LOW)							

Bits 7-0 B/V/Cr key value (lower bound for chroma)

Bits 15-8 G/U/Cb key value (lower bound for chroma)

Bits 23-16 R/Y key value (lower bound for chroma)

Bits 26-24 RGB CC - RGB Color Comparison Precision
000 = Compare bit 7 of RGB (compare red bit 7's, green bit 7's and blue bit 7's)
001 = Compare bits 7-6 of RGB
010 = Compare bits 7-5 of RGB
011 = Compare bits 7-4 of RGB
100 = Compare bits 7-3 of RGB
101 = Compare bits 7-2 of RGB
110 = Compare bits 7-1 of RGB
111 = Compare bits 7-0 of RGB

Bit 27 Reserved

Bit 28 KC - Key Controll
0 = Extract key data from input stream key bit (if present). (KRGB-16, 1.5.5.5 only)
If the K bit is 0, the pixel from the other stream is used (transparent). If the K bit is 1, the key bit streams pixel is used (opaque)
1 = Enable color or chroma keying for all modes other than KRGB-16

Bits 31-29 Reserved

Secondary Stream Control (MM8190)

Read/Write Address: 8190H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DDA HORIZONTAL ACCUMULATOR											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	SFC				SDIF			R	R	R	R	R	R	R	R

Bits 11-0 DDA Horizontal Accumulator Initial Value

Value = 2 (W0-1) - (W1-1), where W0 is the line width in pixels before scaling and W1 is the line width in pixels after scaling. This is a signed value.

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 23-12 Reserved

Bits 26-24 SDIF - Secondary Stream Input Data Format
000 = Reserved
001 = YCbCr-16 (4.2.2), 16-240 input range
010 = YUV-16 (4.2.2), 0-255 input range
011 = KRGB-16 (1.5.5.5)
100 = YUV (2.1.1)
101 = RGB-16 (5.6.5)
110 = RGB-24 (8.8.8)
111 = XRGB-32 (X.8.8.8

When this field is programmed, the value does not take effect until the next VSYNC.

Bit 27 Reserved

Bits 30-28 SFC - Secondary Stream Filter Characteristics
000 = Secondary stream
001 = Secondary stream, linear, 0-2-4-2-0, for X stretch
010 = Secondary stream, bi-linear, for 2X to 4X stretch
011 = Secondary stream, linear, 1-2-2-2-1, for 4X stretch
Other values reserved

When this field is programmed, the value does not take effect until the next VSYNC.

Bit 31 Reserved

Chroma Key Upper Bound (MM8194)

Read/Write Address: 8194H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
U/Cb KEY (UPPER)								V/Cr KEY (UPPER)							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	Y KEY (UPPER)							

Bits 7-0 V/Cr key value (upper bound)

Bits 15-8 U/Cb key value (upper bound)

Bits 23-16 Y key value (upper bound)

Bits 31-24 Reserved

Secondary Stream Stretch/Filter Constants (MM8198)

Read/Write Address: 8198H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K2 HORIZONTAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	K1 HORIZONTAL SCALE FACTOR										

Bits 10-0 K1 Horizontal Scale Factor

Value = W0-1, where W0 is the width in pixels of the initial output window (before scaling)

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 15-11 Reserved

Bits 26-16 K2 Horizontal Scale Factor

Value = W0-W1, where W0 is the initial (unscaled) window width in pixels and W1 is the final output window width in pixels. This is a signed value and will always be negative.

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-27 Reserved

Blend Control (MM81A0)

Read/Write Address: 81A0H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	KP			R	R	R	R	R	KS			R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	COMP MODE			R	R	R	R	R	R	R	R

Bits 1-0 Reserved

Bits 4-2 Ks

Value = secondary stream blend coefficient

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 9-5 Reserved

Bits 12-10 Kp

Value = primary stream blend coefficient

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 23-13 Reserved

Bits 26-24 Compose Mode
000 = Secondary stream opaque overlay on primary stream
001 = Primary stream opaque overlay on secondary stream
010 = Dissolve, [Pp x Kp + Ps x (8 - Kp)]/8, ignore Ks
011 = Fade, [Pp x Kp + Ps x Ks]/8, where Kp + Ks must be ≤ 8
100 = Reserved
101 = Color key on primary stream (secondary stream overlay on primary stream)
110 = Color or chroma key on secondary stream (primary stream overlay on secondary stream)
111 = Reserved

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-27 Reserved

Primary Stream Frame Buffer Address 0 (MM81C0)

Read/Write Address: 81C0H
Power-on Default: Undefined

If a primary stream is enabled, this register specifies the starting address in the frame buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIMARY BUFFER ADDRESS 0															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	PRIMARY BUFFER ADDRESS 0					

Bits 21-0 Value = Primary stream frame buffer starting address 0

This value must be quadword aligned.

Bits 31-22 Reserved

Primary Stream Frame Buffer Address 1 (MM81C4)

Read/Write Address: 81C4H
Power-on Default: Undefined

If the primary stream is double buffered, this register specifies the starting address in the frame buffer for the second buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRIMARY BUFFER ADDRESS 1															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	PRIMARY BUFFER ADDRESS 1					

Bits 21-0 Value = Primary stream frame buffer starting address 1

This value must be quadword aligned.

Bits 31-22 Reserved

Primary Stream Stride (MM81C8)

Read/Write Address: 81C8H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	PRIMARY STREAM STRIDE											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 Primary stream stride

Value = byte offset of vertically adjacent pixels in the primary stream buffer(s)

If double buffering is used, the stride must be the same for both buffers.

Bits 31-12 Reserved

Double Buffer/LPB Support (MM81CC)

Read/Write Address: 81CCH
Power-on Default: xxxxxx00H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	LST	LSL	LIS	R	SBS		PBS
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 PBS - Primary Stream Buffer Select
0 = Primary frame buffer starting address 0 (MM81C0_21-0) used for the primary stream
1 = Primary frame buffer starting address 1 (MM81C4_21-0) used for the primary stream

Bits 2-1 SBS - Secondary Stream Buffer Select
00 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream
01 = Secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream
10 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream. Which alternative applies is determined by LPB starting address register selected by bit 4 of this register
11 = Secondary frame buffer starting address 0 (MM81D0_21-0) used for the secondary stream and LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input stream OR secondary frame buffer starting address 1 (MM81D4_21-0) used for the secondary stream and LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input stream. Which alternative applies is determined by the LPB starting address register selected by bit 4 of this register

Bit 3 Reserved

Bit 4 LIS - LPB Input Buffer Select
0 = LPB frame buffer starting address 0 (MMFF0C_21-0) used for the LPB input
1 = LPB frame buffer starting address 1 (MMFF10_21-0) used for the LPB input

This bit selects the starting address for writing LPB data into the frame buffer. When the value programmed to this bit takes effect is determined by the setting of bit 5 of this register. This bit can be toggled at the completion of writing all the data for a frame to the frame buffer via bit 6 of this register

Bit 5 LSL - LPB Input Buffer Select Loading
0 = The value programmed into bit 4 of this register takes effect immediately
1 = The value programmed into bit 4 of this register takes effect at the next end of frame (completion of writing all the data for a frame into the frame buffer)

Bit 6 LST - LPB Input Buffer Select Toggle
0 = End of frame (completion of writing all the data for a frame into the frame buffer) has no effect on the setting of bit 4 of this register
1 = End of frame causes the setting of bit 4 of this register to toggle

Bits 31-7 Reserved

Secondary Stream Frame Buffer Address 0 (MM81D0)

Read/Write Address: 81D0H
Power-on Default: Undefined

If a secondary stream is enabled, this register specifies the starting address in the frame buffer

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY BUFFER ADDRESS 0															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 0					

Bits 21-0 Value = Secondary stream frame buffer starting address 0

This value must be quadword aligned.

Bits 31-22 Reserved

Secondary Stream Frame Buffer Address 1 (MM81D4)

Read/Write Address: 81D4H
Power-on Default: Undefined

If the secondary stream is double buffered, this register specifies the starting address in the frame buffer for the second buffer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECONDARY BUFFER ADDRESS 1															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	SECONDARY BUFFER ADDRESS 1					

Bits 21-0 Value = Secondary stream frame buffer starting address 1

This value must be quadword aligned.

Bits 31-22 Reserved

Secondary Stream Stride (MM81D8)

Read/Write Address: 81D8H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	SECONDARY STREAM STRIDE											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 Secondary stream stride

Value = byte offset of vertically adjacent pixels in the secondary stream buffer(s)

If double buffering is used, the stride must be the same for both buffers.

Bits 31-12 Reserved

Opaque Overlay Control (MM81DC)

Read/Write Address: 81DCH
Power-on Default: Undefined except bits 31-30 are 00b.

When an opaque overlay mode is being used (bits 26-24 of MM81A0 = 000b or 001b), the fields in this register can be programmed to eliminate the fetching of the pixels for the rectangular area under the top (opaque) window. This reduces the memory bandwidth requirements. The bottom window should be full-screen when this feature is enabled. None of the fields in this register have an effect unless bit 31 is set to 1. Note that only horizontal coordinates must be specified. The vertical coordinates are handled automatically by the hardware.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	PIXEL STOP FETCH										R	R	R
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
OOC	TSS	R	PIXEL RESUME FETCH										R	R	R

Bits 2-0 Reserved

Bits 12-3 Pixel Stop Fetch

Value = [Offset in quadwords from the background starting pixel horizontal position to the first pixel of the line not to be fetched from memory (hidden background)] + 1 quadword

If the primary stream is the background, MM81F0_26-16 define the starting position for each line in the background window (X0) and MM81F8_26-16 define the first pixel position for each line in the top window (X1). The latter is the first background pixel that does not need to be fetched. The value programmed in this field is then [(X1 - X0) x bytes per pixel/8] +1. If the result is a fraction, it is rounded up the next highest integer. This gives the required quadword offset (O) for this field. This value is also used in the calculation for the field value of bits 28-19 of this register.

If the secondary stream is the background, the value is [(X0 - X1) x bytes per pixel/8] + 1.

Bits 18-13 Reserved

Bits 28-19 Pixel Resume Fetch

Value = {Offset in quadwords from the background starting pixel horizontal position to the line position of the resumption of pixel fetching from memory (i.e., visible background)} - 1 quadword

The value is determined by adding the Pixel Stop Fetch field value (O) above (bits 12-3) to the width in quadwords of the top window (W). The width of the top window in pixels (P) is found in MM81F4_26-16 if the primary stream is on top and in MM81FC_26-16 if the secondary stream is on top. W in quadwords = P x bytes per pixel/8. If this is a fraction, the result is truncated to the next lowest integer. The value in this field is then [W + O] - 1.

Bit 29 Reserved

Bit 30 TSS - Top Stream Select
0 = Secondary stream on top
1 = Primary stream on top

Bit 31 OOC - Opaque Overlay Control Enable
0 = Opaque overlay control disabled
1 = Opaque overlay control enabled

K1 Vertical Scale Factor (MM81E0)

Read/Write Address: 81E0H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K1 VERTICAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 K1 Vertical Scale Factor

Value = [height (in lines) of the initial output window (before scaling)] - 1

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-11 Reserved

K2 Vertical Scale Factor (MM81E4)

Read/Write Address: 81E4H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	K2 VERTICAL SCALE FACTOR										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 10-0 K2 Vertical Scale Factor

Value = [height (in lines) of the initial output window (before scaling)] - [height (in lines) of the final output window (after scaling)]

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-11 Reserved

DDA Vertical Accumulator Initial Value (MM81E8)

Read/Write Address: 81E8H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	DDA VERTICAL ACCUMULATOR											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 11-0 DDA Vertical Accumulator Initial Value

Value = 2's complement of [height (in lines) of the output window after scaling] - 1

When this field is programmed, the value does not take effect until the next VSYNC.

Bits 31-12 Reserved

Streams FIFO and RAS Controls (MM81EC)

Read/Write Address: 81ECH
Power-on Default: 00003000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RL	PFIFO THRESHOLD					SFIFO THRESHOLD					FIFO ALLOCATION				
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	EWS	R	RP

Bits 4-0 Streams FIFO Allocation
00000 = Primary Stream = 24 slots, Secondary Stream = 0 slots
01000 = Primary Stream = 16 slots, Secondary Stream = 8 slots
01100 = Primary Stream = 12 slots, Secondary Stream =12 slots
10000 = Primary Stream = 8 slots, Secondary Stream = 16 slots
11000 = Primary Stream = 0 slots, Secondary Stream = 24 slots

All other values are reserved and must not be programmed. Each slot holds one quadword.

Bits 9-5 Secondary FIFO Threshold

Value = Number of secondary FIFO slots

When the secondary FIFO empties down to this value, an internal signal is generated requesting re-filling of the secondary FIFO. This value must be less than or equal to the secondary stream FIFO size specified in bits 4-0.

Bits 14-10 Primary FIFO Threshold

Value = Number of primary FIFO slots

When the primary FIFO empties down to this value, an internal signal is generated requesting re-filling of the primary FIFO. This value must be less than or equal to the primary stream FIFO size specified in bits 4-0.

Bit 15 RL - $\overline{RAS}$ Low Time Control
0 = $\overline{RAS}$ low time specified by CR68_2 (3.5 or 4.5 MCLKs)
1 = RAS low time = 2.5 MCLKs

Bit 16 RP - $\overline{RAS}$ Pre-Charge Control
0 = $\overline{RAS}$ pre-charge specified by CR68_3 (2.5 or 3.5 MCLKs)
1 = $\overline{RAS}$ pre-charge = 1.5 MCLKs

Bit 17 Reserved

Bit 18 EWS - EDO Memory Wait State Control (LPB Memory Cycles Only)
0 = Standard 2-cycle memory operation
1 = 1-cycle EDO memory operation (requires EDO memory capable of this)

Bits 31-19 Reserved

Primary Stream Window Start Coordinates (MM81F0)

Read/Write Address: 81F0H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	PRIMARY STREAM Y-START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	PRIMARY STREAM X-START										

Bits 10-0 Primary Stream Y-Start

Value = Screen line number +1 of the first line of the primary stream window

Bits 15-11 Reserved

Bits 26-16 Primary Stream X-Start

Value = Screen pixel number +1 of the first pixel of the primary stream window

Bits 31-27 Reserved

Primary Stream Window Size (MM81F4)

Read/Write Address: 81F4H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	PRIMARY STREAM HEIGHT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	PRIMARY STREAM WIDTH										

Bits 10-0 Primary Stream Height

Value = Number of lines displayed in the primary stream window

Bits 15-11 Reserved

Bits 26-16 Primary Stream Width

Value = Number of pixels -1 displayed in each line in the primary stream window

Bits 31-27 Reserved

Secondary Window Start Coordinates (MM81F8)

Read/Write Address: 81F8H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SECONDARY STREAM Y-START										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	SECONDARY STREAM X-START										

Bits 10-0 Secondary Stream Y-Start

Value = Screen line number +1 of the first line of the secondary stream window

Bits 15-11 Reserved

Bits 26-16 Secondary Stream X-Start

Value = Screen pixel number +1 of the first pixel of the secondary stream window

Bits 31-27 Reserved

Secondary Window Size (MM81FC)

Read/Write Address: 81FCH
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	SECONDARY STREAM HEIGHT										
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	SECONDARY STREAM WIDTH										

Bits 10-0 Secondary Stream Height

Value = Number of lines displayed in the secondary stream window

Bits 15-11 Reserved

Bits 26-16 Secondary Stream Width

Value = Number of pixels -1 displayed in each line in the primary stream window

Bits 31-27 Reserved

Section 22: Local Peripheral Bus Register Descriptions

LPB registers can only be accessed via memory-mapped I/O. The register identifier MMxxxx means that the register is memory mapped at offset xxxx from the base address.

LPB Mode (MMFF00)

Read/Write Address: FF00H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	LBA	CHS	CVS	LHS	LVS	R	R	CBS	SF	LR	LPB MODE			LE
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ZV	BAS	IOD	R	R	ILC	SNO	CS	R	VFT		R	R	R	MBS	

Bit 0 LE - LPB Enable
0 = LPB Disabled
1 = LPB Enabled

Once enabled, the LPB is reset either by a system reset or via bit 4 of this register.

Bits 3-1 LPB MODE
000 = Scenic/MX2 Mode. Pins K1 and L1 act as $\overline{\text{VREQ}}$/VRDY and $\overline{\text{CREQ}}$/CRDY respectively.
001 = Video 16 Mode. Pins K1 and L1 act as HS and VS respectively. This mode is also used for ZV Port operation.
010 = Video 8 In Mode. Pins K1 and L1 to act as HS and VS respectively and the 86CM65 expects video data in 8-bit units (LD[7:0]).
100 = Pass-through Mode. 32-bit data from the output FIFO is passed directly to the decimation input to the video FIFO. This allows decimation of CPU-provided data.

All other values are reserved.

Bit 4 LR- LPB Reset
0 = No effect
1 = Reset LPB

This bit should be set and then reset before switching between LPB modes.

Bit 5 SF - Skip Frames
0 = Write all received frames to memory
1 = Write every other received frame to memory (1, 3, etc.)

Bit 6 CBS - Color Byte Swap
0 = Incoming video is in U_{01}, Y_0, V_{01}, Y_1 format, byte swap enabled
1 = Incoming video is in Y_0, U_{01}, Y_1, V_{01} format (e.g., SAA7110), no byte swap

Bits 8-7 Reserved

Bit 9 LVS - LPB Vertical Sync Input Polarity
0 = LPB vertical sync input is active low
1 = LPB vertical sync input is active high

Bit 10 LHS - LPB Horizontal Sync Input Polarity
0 = LPB horizontal sync input is active low
1 = LPB horizontal sync input is active high

Bit 11 CVS - CPU VSYNC (Write Only)

Writing a 1 to this bit causes the 86CM65 to do whatever functions it is programmed to do upon receipt of a VSYNC. For example, values programmed in certain registers only take effect at the next VSYNC.

Bit 12 CHS - CPU HSYNC (Write Only)

Writing a 1 to this bit causes the 86CM65 to do whatever functions it is programmed to do upon receipt of an HSYNC.

Bit 13 LBA - Load Base Address (Write Only)

Writing a 1 to this bit immediately loads the base address currently being pointed to.

Bits 15-14 Reserved

Bits 17-16 MBS - Maximum LPB to Scenic/MX2 Compressed Data Burst Size (Scenic/MX2 mode only)
00 = Burst 1 32-bit word
01 = Burst 2 32-bit words
10 = Burst 3 32-bit words
11 = Burst all 32-bit words (until empty)

With a setting of 11b, software must ensure that no more than eight 32-bit words are burst to the Scenic/MX2 in a single burst. For example, if the FIFO is full (8 entries), no more entries should be written until the burst is complete.

Bits 20-18 Reserved

Bits 22-21 VFT - Video FIFO Threshold
00 = 1 FIFO slot
01 = 2 FIFO slots
10 = 4 FIFO slots
11 = 6 FIFO slots

When this many slots are filled in the video FIFO, a request is generated to the memory manager to begin emptying the FIFO. This is used to maximize the efficiency of the memory interface.

Bit 23 Reserved

Bit 24 CS - LPB Clock Source
0 = LPB clock driven by SCLK
1 = LPB clock driven by LCLK

LCLK is used when an external peripheral is connected to the LPB. SCLK is used for pass-through mode.

Bit 25 SNO - Sync Non-Overlap
0 = No effect
1 = Don't add stride after first HSYNC

This bit must be set when the first HSYNC does not occur within the VSYNC active period.

Bit 26 ILC - Invert LCLK
0 = Use LCLK as received
1 = Invert the LCLK input

Bits 28-27 Reserved

Bit 29 IOD - Invert Odd/Even Frame Indicator
0 = Odd/Even frame indicator unchanged
1 = Odd/Even fram indicator inverted

This inverts either the input on the ODD pin or the automatic odd/even frame indicator generated during ZV Port operation.

Bit 30 BAS - Base Address Select
0 = Normal operation
1 = Use state of the odd/even frame indicator (as affected by bit 29 of this register) to select LPB base address 0 or LPB base address 1

This bit and bit 29 are used to support display of interlaced TV output.

Bit 31 ZV- ZV Port Enable
0 = ZV Port operation disabled
1 = ZV Port operation enabled

This enables automatic detection of odd/even fields when the LPB is operated in Video 16 mode.

LPB FIFO Status (MMFF04)

Read Only Address: FF04H
Power-on Default: 00000008H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	OFAE	OFE	OFF	R	R	R	R	R	R	R	OFIFO STATUS			
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VF1AE	VF1E	VF1F	R	R	R	R	R	R	VF0AE	BST	ODDS	R	R	R	R

Bits 3-0 LPB Output FIFO Status
0000 = 0 FIFO slots free
0001 = 1 FIFO slot free
0010 = 2 FIFO slots free
0011 = 3 FIFO slots free
0100 = 4 FIFO slots free
0101 = 5 FIFO slots free
0110 = 6 FIFO slots free
0111 = 7 FIFO slots free
1000 = 8 FIFO slots free

Each slot contains 4 bytes

Bits 10-4 Reserved

Bit 11 OFF - LPB Output FIFO Full
0 = Output FIFO not full
1 = Output FIFO full

Bit 12 OFE - LPB Output FIFO Empty
0 = Output FIFO not empty
1 = Output FIFO empty

Bit 13 OFAE - LPB Output FIFO Almost Empty
0 = Output FIFO has something other than 1 slot filled
1 = Output FIFO has one slot filled

Bits 19-14 Reserved

Bit 20 ODD Pin Signal Input Status
0 = ODD pin input is low
1 = ODD pin input is high

Bit 21 BST - Base Address Select Status
0 = LPB base address 0 selected for storage of video data
1 = LPB base address 1 selected for storage of video data

Bit 22 VF0AE - LPB Video FIFO 0 Almost Empty
0 = Video FIFO 0 has something other than 1 slot filled
1 = Video FIFO 0 has one slot filled

Bits 28-23 Reserved

Bit 29 VF1F - LPB Video FIFO 1 Full
0 = Video FIFO 1 not full
1 = Video FIFO 1 full

Bit 30 VF1E - LPB Video FIFO 1 Empty
0 = Video FIFO 1 not empty
1 = Video FIFO 1 empty

Bit 31 VF1AE - LPB Video FIFO 1 Almost Empty
0 = Video FIFO 1 has something other than 1 slot filled
1 = Video FIFO 1 has one slot filled

LPB Interrupt Flags (MMFF08)

Read/Write Address: FF08H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	SPS	EFI	ELI	FEI
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	SPW	R	R	R	R	SPM	EFM	ELM	FEM

Bit 0 FEI - LPB Output FIFO Empty Interrupt Status
0 = No interrupt
1 = LPB output FIFO empty

Writing a 1 to this bit clears the interrupt.

Bit 1 ELI - End of Line Interrupt Status
0 = No interrupt
1 = The 86CM65 has received an HSYNC input on pin K1

Writing a 1 to this bit clears the interrupt.

Bit 2 EFI - End of Frame Interrupt Status
0 = No interrupt
1 = The 86CM65 has received a VSYNC input on pin L1

Writing a 1 to this bit clears the interrupt.

Bit 3 SPS - Serial Port Start Detect Interrupt Status
0 - No interrupt
1 = The 86CM65 has detected a serial port start condition

A serial port start condition occurs when pin M3 is driven low by another device while pin M2 is not being driven low. Writing a 1 to this bit clears the interrupt.

Bits 15-4 Reserved

Bit 16 FEM - LPB Output FIFO Empty Interrupt Enable Mask
0 = LPB output FIFO empty interrupt disabled
1 = LPB output FIFO empty interrupt enabled

Bit 17 ELM - End of Line Interrupt Enable Mask
0 = End of Line interrupt disabled
1 = End of Line interrupt enabled

Bit 18 EFM - End of Frame Interrupt Enable Mask
0 = End of frame interrupt disabled
1 = End of frame interrupt enabled

Bit 19 SPM - Serial Port Start Detect Interrupt Mask
0 = Serial port start detect interrupt disabled
1 = Serial port start detect interrupt enabled

Bits 23-20 Reserved

Bit 24 SPW - Serial Port Wait
0 = Release SPCLK to float high
1 = Drive SPCLK low upon receipt of a serial port start condition

Setting this bit to 1 enables serial port wait states until the host is ready to process the data.

Bit 31-25 Reserved

LPB Frame Buffer Address 0 (MMFF0C)

Read/Write Address: FF0CH
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB BUFFER ADDRESS 0															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	LPB BUFFER ADDRESS 0					

Bits 21-0 LPB Frame Buffer Address 0

Value = starting address 0 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer

This value will normally be the same as the secondary stream frame buffer address 0. The value must start on an 8-byte boundary.

Bits 31-22 Reserved

LPB Frame Buffer Address 1 (MMFF10)

Read/Write Address: FF10H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB BUFFER ADDRESS 1															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	LPB BUFFER ADDRESS 1					

Bits 21-0 LPB Frame Buffer Address 1

Value = starting address 1 (offset in bytes from the start of the frame buffer) for writing LPB data to the frame buffer

This value will normally be the same as the secondary stream frame buffer address 1. Both address 0 and address 1 are defined when double buffering is used. The value must start on an 8-byte boundary.

Bits 31-22 Reserved

LPB Direct Read/Write Address (MMFF14)

Read/Write Address: FF14H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB DIRECT READ/WRITE ADDRESS															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	TT			LPB READ/WRITE ADDRESS				

Bits 20-0 LPB Direct Read/Write Address

Value = address of Scenic/MX2 register to read/write

Bits 23-21 TT - Transaction Type (Scenic/MX2)
000 = Register write
001 = Register read
110 = Compressed video data write from the output FIFO. This value is automatically generated by hardware when data is written to the output FIFO.

Bits 31-24 Reserved

LPB Direct Read/Write Data (MMFF18)

Read/Write Address: FF18H
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LPB DIRECT READ/WRITE DATA															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
LPB DIRECT READ/WRITE DATA															

Bits 31-0 LPB Direct Read/Write Data

A write to this register triggers a read/write sequence based on the address information in MMFF14_23-0.

LPB General Purpose Input/Output Port (MMFF1C)

Read/Write - see bit definitions Address: FF1CH
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	LPB GIP				LPB GOP			
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bits 3-0 LPB General Purpose Output Data Port

These bits are driven onto the LPB LD[3:0] lines whenever a write is performed to CR5C. STWR is asserted (low) at this time for use as an enable strobe for latching the data into an external buffer.

Bits 7-4 LPB General Purpose Input Data Port (Read only)

Whenever a write is performed to CR5C, STWR is asserted (low). This strobe can be used to enable a register to drive data onto any or all of the LD[7:4] lines. This data is then latched into these bits.

Bits 31-8 Reserved

Serial Port (MMFF20)

Read/Write Address: FF20H
Power-on Default: 00000000H

This register can also be accessed at I/O ports E2H or E8H. See the Serial Communications Port description in Section 4.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	B4M	B3M	B2M	B1M	B0M	R	R	R	SPE	SDR	SCR	SDW	SCW
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit 0 SCW - Serial Clock Write
0 = Pin M2 is driven low
1 = Pin M2 is tri-stated

Pin M2 carries the DDC/I^2C clock, depending on the operational mode. When pin M2 is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 2 of this register.

Bit 1 SDW - Serial Data Write
0 = Pin M3 is driven low
1 = Pin M3 is tri-stated

Pin M3 carries the DDC/I^2C data, depending on the operational mode. When pin M3 is tri-stated, other devices may drive this line. The actual state of the pin is read via bit 3 of this register.

Bit 2 SCR - Serial Clock Read (Read Only)
0 = Pin M2 is low
1 = Pin M2 is tri-stated (no device is driving this line)

Bit 3 SDR - Serial Data Read (Read Only)
0 = Pin M3 is low
1 = Pin M3 is tri-stated (no device is driving this line)

Bit 4 SPE - Serial Port Enable
0 = Use of bits 1-0 of this register disabled
1 = Use of bits 1-0 of this register enabled

Bits 5-7 Reserved

Bit 8 B0M - Bit 0 Mirror (Read Only)
0 = Pin M2 is driven low
1 = Pin M2 is tri-stated

Bit 9 B1M - Bit 1 Mirror (Read Only)
0 = Pin M3 is driven low
1 = Pin M3 is tri-stated

Bit 10 B2M - Bit 2 Mirror (Read Only)
0 = Pin M2 is low
1 = Pin M2 is tri-stated (no device is driving this line)

Bit 11 B3M -Bit 3 Mirror (Read Only)
0 = Pin M3 is low
1 = Pin M3 is tri-stated (no device is driving this line)

Bit 12 B4M - Bit 4 Mirror (Read Only)
0 = Use of bits 1-0 of this register disabled
1 = Use of bits 1-0 of this register enabled

This bit mirrors bit 4 and allows reading of this data on byte lane 2 at I/O address E2H.

Bits 31-13 Reserved

LPB Video Input Window Size (MMFF24)

Read/Write Address: FF24H
Power-on Default: Undefined

This register applies only to Video 8 In or Video 16 mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	VIDEO INPUT LINE WIDTH											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	VIDEO INPUT WINDOW HEIGHT								

Bits 11-0 Video Input Line Width

Value = [# pixels x 2] - 2 for Video 8 mode
Value = # pixels -2 for Video 16 mode

This is the width of the displayed line after the offset specified in MMFF28_11-0. Before the 2 is subtracted, the number of pixels must be a multiple of 4. For example, in Video 16 mode, if the line width is 637 pixels, this must be rounded up to 640. The programmed value is then 640 - 2 = 638.

Bits 15-12 Reserved

Bits 24-16 Video Input Window Height

Value = [height in lines of each video input frame] - 1

This is the number of displayed lines - 1 after the offset specified in MMFF28_24_16.

Bits 31-25 Reserved

LPB Video Data Offsets (MMFF28)

Read/Write Address: FF28H
Power-on Default: Undefined

This register applies only to Video 8 In or Video 16 mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	HORIZONTAL VIDEO DATA OFFSET											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R	R	R	VERTICAL VIDEO DATA OFFSET								

Bits 11-0 Horizontal Video Data Offset

Value = [number of LCLKs between HSYNC and the start of valid pixel data] - 2

Bits 15-12 Reserved

Bits 24-16 Vertical Video Data Offset

Value = number of HSYNCs between VSYNC and the first valid data line

Bits 31-25 Reserved

LPB Horizontal Decimation Control (MMFF2C)

Read/Write Address: FF2CH
Power-on Default: Undefined

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO DATA BYTE MASK															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VIDEO DATA BYTE MASK															

Bits 31-0 Video Data Byte Mask

Each 32 bytes of video data input is compared with this mask. If a bit in this mask is 1, the corresponding byte is discarded. If a bit is a 0, the corresponding byte is passed to the video memory. In Video 16 mode, each bit masks 2 bytes. In pass-through mode, each bit masks 4 bytes. Normally, decimation starts with bit 0 after an HSYNC. If a horizontal video data offset is specified in MMFF28_11-0 (video 8 or 16 modes only), decimation aligns with the start of data after the offset.

LPB Vertical Decimation Control (MMFF30)

Read/Write Address: FF30H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VIDEO DATA LINE MASK															
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VIDEO DATA LINE MASK															

Bits 31-0 Video Data Line Mask

Each 32 lines of video data input is compared with this mask. If a bit in the mask is 0, the corresponding line is discarded. If a bit is a 1, the corresponding line is passed to the video memory. If a vertical video data offset is specified in MMFF28_24-16 (video 8 or 16 modes only), decimation does not align with the starting line after the offset and instead starts from VSYNC.

LPB Line Stride (MMFF34)

Read/Write Address: FF34H
Power-on Default: 00000000H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	LINE STRIDE											
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
R	R	R	R	R		R	R	R	R	R	R	R	R	R	R

Bits 11-0 Line Stride

Value = byte offset of vertically adjacent pixels

This offset is added to the line starting address each HSYNC to get the new line starting address. Each line must begin on an 8-byte boundary.

Bits 31-12 Reserved

LPB Output FIFO (MMFF40)

Read/Write Address: FF40H, FF44H...,FF5CH
Power-on Default: 00000000H

Writes to any of the addresses in this 8 doubleword address range will be transferred to the LPB input FIFO. This allows efficient use of the MOVSD assembly language instruction. Accesses must be to doubleword addresses.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTPUT FIFO DATA															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OUTPUT FIFO DATA															

Bits 31-0 Output FIFO Data

Note: Software must never transfer more compressed data than there is room for in the output FIFO. This information is read from MMFF04_3-0.

Section 23: PCI Register Descriptions

The PCI specification defines a configuration register space. These registers allow device relocation, device independent system address map construction and automatic configurations. The 86CM65 provides a subset of these registers, which are described below.

The configuration register space occupies 256 bytes. When a configuration read or write command is issued, the AD[7:0] lines contain the address of the register in this space to be accessed. The 86CM65 supports or returns 0 for the first 64 bytes of this space.

In the following register descriptions, 'R' stands for reserved (write = 0, read = undefined). See Appendix A for a table listing each of the registers in this section and its page number.

Vendor ID

Read Only Address: 00H
Power-On Default: 5333H

This read-only register identifies the device manufacturer.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vendor ID															

Bits 15–0 Vendor ID

This is hardwired to 5333H to identify S3 Incorporated.

Device ID

Read Only Address: 02H
Power-On Default: 8812H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device ID															

Bits 15–0 Device ID

This is hardwired to 8812H

Command

Read/Write Address: 04H
Power-On Default: 0000H

This register controls which types of PCI cycles the 86CM65 can generate and respond to.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	DAC SNP	R	R	R	MEM	I/O

Bit 0 I/O - Enable Response to I/O Accesses
0 = Response to I/O space accesses is disabled
1 = Response to I/O space accesses enabled

Bit 1 MEM - Enable Response to Memory Accesses
0 = Response to memory space accesses is disabled
1 = Response to memory space accesses enabled

Bits 4–2 Reserved

Bit 5 DAC SNP - RAMDAC Register Access Snooping
0 = 86CM65 claims and responds to all RAMDAC register access cycles
1 = 86CM65 performs RAMDAC register writes but does not claim the PCI cycle. RAMDAC register read accesses are performed by the 86CM65.

Bits 15–6 Reserved

Status

Read/Write Address: 06H
Power-On Default: 0200H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	DEVSEL		Reserved								

Bits 8–0 Reserved

Bits 10–9 DEVSEL - Device Select Timing

This is hardwired to 01 to select medium $\overline{\text{DEVSEL}}$ timing.

Bits 15–11 Reserved

Class Code

Read Only Address: 08H
Power-On Default: 300004xH

This register is hardwired to 300004xH. The 3 specifies that the 86CM65 is a VGA-compatible display controller. The "x" in the revision ID will change with each revision.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGRAMMING INTERFACE								REVISION ID							
31	**30**	**29**	**28**	**27**	**26**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
BASE CLASS CODE								SUB-CLASS							

Base Address 0

Read/Write Address: 12H (high) 10H (low)
Power-On Default: 0000 0000H

This is a 32-bit register in PCI configuration space that provides for address relocation. The 86CM65 maps the upper 6 bits of the register to the Linear Address Window Position register CR59_7-2. Consequently, these bits map to system address bits [31:26].

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	PREF = 0	TYPE =00		MSI = 0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BASE ADDRESS 0						R	R	R	R	R	R	R	R	R	R

Bit 0 MSI - Memory Space Indicator

This is hardwired to 0 to specify that the base registers map into memory space

Bits 2–1 TYPE - Type of Address Relocation

This is hardwired to 00b (locate anywhere in 32-bit address space)

Bit 3 PREF - Prefetchable

This is hardwired to 0 (does not meet the prefetchable requirements)

Bits 22–4 Reserved

Bits 31–23 BASE ADDRESS 0

See the description for the Linear Address Window Position registers (CR59, CR5A). Writes to CR59 will also update this field.

BIOS ROM Base Address

Read/Write Address: 32H (high) 30H (low)
Power-On Default: 000C 0000H

This is a 32-bit register in PCI configuration space that provides for video BIOS ROM address relocation.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	ADE

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BIOS ROM BASE ADDRESS															

Bit 0 ADE - Address Decode Enable
0 = Accesses to the BIOS ROM address space defined in this register are disabled
1 = Accesses to the BIOS ROM address space defined in this register are enabled

Bits 15–1 Reserved

Bits 31–16 BIOS ROM BASE ADDRESS

These are the upper 16 bits of the BIOS ROM address.

Interrupt Line

Read/Write Address: 3CH
Power-On Default: 00H

This register contains interrupt line routing information written by the POST program during power-on initialization.

7	6	5	4	3	2	1	0
INTERRUPT LINE							

Bits 7–0 INTERRUPT LINE

Interrupt Pin

Read Only Address: 3DH
Power-On Default: 01H

7	6	5	4	3	2	1	0
INTERRUPT PIN							

Bits 7–0 INTERRUPT PIN

This is hardwired to a value of 1 to specify that $\overline{\text{INTA}}$ is the interrupt pin used.

Appendix A: Register Reference

This Appendix contains tables listing all the registers in each of categories corresponding to Sections 17-25 of this data book.

- VGA
- Extended Sequencer
- Extended CRTC
- Enhanced Commands
- Streams Processor
- LPB
- PCI Configuration Space

Within each table, registers are listed in order of increasing addresses/indices. Name, address, register bit descriptions with read/write status and the page number of the detailed register description are provided for each register. All addresses and indices are hexadecimal values.

A.1 VGA REGISTERS

? = B for monochrome, D for color.

Table A-1. VGA Registers

Address	Index Bit(s)		Register Name Bit Description	Description Page
General or External Registers				
3C2			**Miscellaneous Output**	**17-1**
	0	W	Color emulation. Address based at 3Dx	
	1	W	Enable CPU access of video memory	
	3-2	W	Video DCLK select. Enable DCLK PLL loading	
	4	W	Reserved	
	5	W	Select the high 64K page of memory	
	6	W	Make HSYNC an active low signal	
	7	W	Make VSYNC an active low signal	
	7-6	W	(Alternate) Vertical graphics resolution	
3CC			**Miscellaneous Output**	**17-1**
	0	R	Color emulation. Address based at 3Dx	
	1	R	Enable CPU access of video memory	
	3-2	R	Video DCLK select. Enable DCLK PLL loading	
	4	R	Reserved	
	5	R	Select the high 64K page of memory	
	6	R	Make HSYNC an active low signal	
	7	R	Make VSYNC an active low signal	
	7-6	R	(Alternate) Vertical graphics resolution	
3?A			**Feature Control**	**17-3**
	2-0	W	Reserved	
	3	W	VSYNC is ORed with the internal display enable signal	
	7-4	W	Reserved	
3CA			**Feature Control**	**17-3**
	2-0	R	Reserved	
	3	R	VSYNC is ORed with the internal display enable signal	
	7-4	R	Reserved	
3C2			**Input Status 0**	**17-3**
	3-0	R	Reserved	
	4	R	The internal SENSE signal is a logical 1	
	6-5	R	Reserved	
	7	R	Vertical retrace interrupt to the CPU is pending	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?A			**Input Status 1**	**17-4**
	0	R	The display in not in active display mode	
	1	R	Reserved	
	2	R	Reserved =1	
	3	R	Vertical retrace period is active	
	5-4	R	Feedback of two color outputs for test purposes	
	7-6	R	Reserved	
3C3			**Video Subsystem Enable**	**17-4**
	0	W	Enable 86CM65	
	7-1	R/W	Reserved	
Sequencer Registers				
3C4			**Sequencer Index**	**17-5**
	4-0	R/W	Index to the sequencer register to be accessed	
	7-5	R/W	Reserved	
3C5			**Sequencer Data**	**17-5**
	7-0	R/W	Data to or from the sequencer register accessed	
3C5	**00**		**Reset (SR0)**	**17-6**
	0	R/W	Asynchronous reset (not functional for the Trio64V+)	
	1	R/W	Synchronous reset (not functional for the Trio64V+)	
	7-2	R/W	Reserved	
3C5	**01**		**Clocking Mode (SR1)**	**17-6**
	0	R/W	Character clocks are 8 dots wide	
	1	R/W	Reserved	
	2	R/W	Load the video serializers every second character clock	
	3	R/W	The internal character clock is 1/2 the DCLK frequency	
	4	R/W	Load the video serializers every fourth character clock	
	5	R/W	Screen is turned off - Shared	
3C5	**02**		**Enable Write Plane (SR2)**	**17-7**
	3-0	R/W	Enables a CPU write to the corresponding color plane	
	7-4	R/W	Reserved	
3C5	**03**		**Character Font Select (SR3)**	**17-8**
	4, 1-0	R/W	Select Font B - Shared	
	5,3-2	R/W	Select Font A - Shared	
	7-6	R/W	Reserved	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**04**		**Memory Mode Control (SR4)**	**17-9**
	0	R/W	Reserved	
	1	R/W	Memory access to 256K allowed (required for VGA) - Shared	
	2	R/W	Sequential addressing for CPU video memory accesses	
	3	R/W	Modulo 4 addressing for CPU video memory accesses - Shared	
	7-4	R/W	Reserved	
CRT Controller Registers				
3?4			**CRT Controller Index**	**17-10**
	7-0	R/W	Index to the CRTC register to be accessed	
3?5			**CRT Controller Data**	**17-10**
	7-0	R/W	Data to or from the CRTC register accessed	
3?5	**00**		**Horizontal Total (CR0) - Paired**	**17-11**
	7-0	R/W	Number of characters in a line -5	
3?5	**01**		**Horizontal Display End (CR1) - Paired**	**17-11**
	7-0	R/W	One less than the total number of displayed characters	
3?5	**02**		**Start Horizontal Blank (CR2) - Paired**	**17-12**
	7-0	R/W	Character count where horizontal blanking starts	
3?5	**03**		**End Horizontal Blank (CR3) - Paired**	**17-12**
	4-0	R/W	End position of horizontal blanking	
	6-5	R/W	Display enable skew in character clocks	
	7	R/W	Reserved	
3?5	**04**		**Start Horizontal Sync Position (CR4) - Paired**	**17-13**
	7-0	R/W	Character count where HSYNC goes active	
3?5	**05**		**End Horizontal Sync Position (CR5) - Paired**	**17-13**
	4-0	R/W	Position where HSYNC goes inactive	
	6-5	R/W	Horizontal retrace end delay in character clocks	
	7	R/W	End horizontal blanking bit 5	
3?5	**06**		**Vertical Total (CR6) - Paired**	**17-14**
	7-0	R/W	Number of lines - 2	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	07		**CRTC Overflow (CR7) - Paired**	17-14
	0	R/W	Vertical total bit 8	
	1	R/W	Vertical display end bit 8	
	2	R/W	Vertical retrace start bit 8	
	3	R/W	Start vertical blank bit 8	
	4	R/W	Line compare bit 8	
	5	R/W	Vertical total bit 9	
	6	R/W	Vertical display end bit 9	
	7	R/W	Vertical retrace start bit 9	
3?5	08		**Preset Row Scan (CR8) - Paired**	17-15
	4-0	R/W	Line where first character row begins	
	6-5	R/W	Number of bytes to pan horizontally	
	7	R/W	Reserved	
3?5	09		**Maximum Scan Line (CR9) - Paired**	17-15
	4-0	R/W	Character height in scan lines -1	
	5	R/W	Start vertical blank bit 9	
	6	R/W	Line compare bit 9	
	7	R/W	Double scanning (repeat each line) enabled	
3?5	0A		**Cursor Start Scan Line (CRA) - Shared**	17-16
	4-0	R/W	Cursor starting line within the character cell	
	5	R/W	Turns off the cursor	
	7-6	R/W	Reserved	
3?5	0B		**Cursor End Scan Line (CRB) - Shared**	17-16
	4-0	R/W	Cursor ending line within the character cell	
	6-5	R/W	Cursor skew to right in characters	
	7	R/W	Reserved	
3?5	OC		**Start Address High (CRC) - Paired**	17-17
	7-0	R/W	Bits 15-8 of the display start address	
3?5	OD		**Start Address Low (CRD) - Paired**	17-17
	7-0	R/W	Bits 7-0 of the display start address	
3?5	OE		**Cursor Location Address High (& Hardware Cursor Foreground Color in Enhanced Mode) (CRE) - Shared**	17-17
	7-0	R/W	Bits 15-8 of the cursor location start address	
3?5	OF		**Cursor Location Address Low (& Hardware Cursor Background Color in Enhanced Mode) (CRF) - Shared**	17-17
	7-0	R/W	Bits 7-0 of the cursor location start address	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**10**		**Vertical Retrace Start (CR10 - Paired**	**17-18**
	7-0	R/W	Vertical retrace start in scan lines	
3?5	**11**		**Vertical Retrace End (CR11) - Paired**	**17-18**
	3-0	R/W	Vertical retrace end in scan lines	
	4	R/W	Clear the vertical retrace interrupt flip-flop	
	5	R/W	Disable vertical interrupts	
	6	R/W	Five RAM refresh cycles per horizontal line	
	7	R/W	Lock writes to CR0-CR7	
3?5	**12**		**Vertical Display End (CR12) - Paired**	**17-19**
	7-0	R/W	Number of scan lines of active video	
3?5	**13**		**Offset (CR13) - Paired**	**17-19**
	7-0	R/W	Memory start address jump from one scan line to the next	
3?5	**14**		**Underline Location (CR14) - Paired**	**17-20**
	4-0	R/W	Horizontal scan line where underline occurs	
	5	R/W	Memory address counter increment is 4 character clocks	
	6	R/W	Memory accessed as doublewords	
	7	R/W	Reserved	
3?5	**15**		**Start Vertical Blank (CR15) - Paired**	**17-20**
	7-0	R/W	Horizontal scan line where vertical blanking starts	
3?5	**16**		**End Vertical Blank (CR16) - Paired**	**17-21**
	7-0	R/W	Horizontal scan line where vertical blanking ends	
3?5	**17**		**CRTC Mode Control (CR17) - Paired**	**17-21**
	0	R/W	Enable bank 2 mode for CGA emulation	
	1	R/W	Enable bank 4 mode for CGA emulation	
	2	R/W	Use horizontal retrace clock divided by 2	
	3	R/W	Enable count by 2 mode	
	4	R/W	Reserved	
	5	R/W	Enable CGA mode address wrap	
	6	R/W	Use byte address mode	
	7	R/W	Horizontal and vertical retrace signals enabled	
3?5	**18**		**Line Compare (CR18) - Paired**	**17-23**
	7-0	R/W	Line at which memory address counter cleared to 0	
3?5	**22**		**CPU Latch Data (CR22) - Paired**	**17-23**
	7-0	R	Value in the CPU latch in the graphics controller	
3?5	**24,26**		**Attribute Controller Flag/Index - Paired**	**17-24**
	5-0	R	Value of the attribute controller index data at 3C0H	
	6	R	Reserved	
	7	R	State of inverted internal address flip-flop	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
Graphics Controller Registers				
3CE			**Graphics Controller Index**	**17-25**
	3-0	R/W	Index to the graphics controller register to be accessed	
	7-4	R/W	Reserved	
3CF			**Graphics Controller Data**	**17-25**
	7-0	R/W	Data to or from the graphics controller register accessed	
3CF	**00**		**Set/Reset (GR0)**	**17-26**
	3-0	R/W	Color value for CPU memory writes	
	7-4	R/W	Reserved	
3CF	**01**		**Enable Set/Reset (GR1)**	**17-26**
	3-0	R/W	Enable planes for writing GR0 data	
	7-4	R/W	Reserved	
3CF	**02**		**Color Compare (GR2)**	**17-27**
	3-0	R/W	Reference color for color compare operations	
	7-4	R/W	Reserved	
3CF	**03**		**Raster Operation/Rotate Counter (GR3)**	**17-27**
	2-0	R/W	Number of right rotate positions for a CPU memory write	
	4-3	R/W	Select raster operation (logical function)	
	7-5	R/W	Reserved	
3CF	**04**		**Read Plane Select (GR4)**	**17-28**
	1-0	R/W	Select planes for reading	
	7-2	R/W	Reserved	
3CF	**05**		**Graphics Controller Mode (GR5)**	**17-29**
	1-0	R/W	Select write mode	
	2	R/W	Reserved	
	3	R/W	Enable read compare operation	
	4	R/W	Select odd/even addressing	
	5	R/W	Select odd/even shift mode - Shared	
	6	R/W	Select 256 color shift mode - Shared	
	7	R/W	Reserved	
3CF	**06**		**Memory Map Mode Control (GR6)**	**17-30**
	0	R/W	Select graphics mode memory addressing	
	1	R/W	Chain odd/even planes	
	3-2	R/W	Select memory mapping	
	7-4	R/W	Reserved	
3CF	**07**		**Color Don't Care (GR7)**	**17-31**
	3-0	R/W	Select color plane used for color comparison	
	7-4	R/W	Reserved	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3CF	**08**		**Bit Mask (GR8)**	**17-31**
	7-0	R/W	Each bit is a mask for the corresponding memory plane bit	
Attribute Registers				
3C0			**Attribute Controller Index**	**17-32**
	4-0	R/W	Index to the attribute controller register to be accessed	
	5	R/W	Enable video display	
	7-6	R/W	Reserved	
3C1/0			**Attribute Controller Data**	**17-33**
	7-0	R/W	Data to or from the attribute controller register accessed	
3C1/0	**00–0F**		**Palette Register (AR0–ARF)**	**17-33**
	5-0	R/W	Color value	
	7-6	R/W	Reserved	
3C1/0	**10**		**Attribute Mode Control (AR10)**	**17-34**
	0	R/W	Select graphics mode	
	1	R/W	Select monochrome display	
	2	R/W	Enable line graphics characters	
	3	R/W	Enable blinking	
	4	R/W	Reserved	
	5	R/W	Enable top panning	
	6	R/W	Select 256 color mode	
	7	R/W	Bits 5-4 of video output come from AR14_1-0	
3C1/0	**11**		**Border Color (AR11) - Shared**	**17-35**
	7-0	R/W	Border color value	
3C1/0	**12**		**Color Plane Enable (AR12)**	**17-35**
	3-0	R/W	Display plane enable	
	5-4	R/W	Select inputs to bits 5-4 of 3?AH	
	7-6	R/W	Reserved	
3C1/0	**13**		**Horizontal Pixel Panning (AR13)**	**17-36**
	3-0	R/W	Number of pixels to shift the display to the left	
	7-4	R/W	Reserved	
3C1/0	**14**		**Pixel Padding (AR14)**	**17-37**
	1-0	R/W	Bits 5-4 of the video output if AR10_7 = 1	
	3-2	R/W	Bits 7-6 of the video output	
	7-4	R/W	Reserved	

Table A-1. VGA Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
RAMDAC Registers				
3C6			**DAC Mask**	**17-38**
	7-0	R/W	Pixel read mask	
3C7			**DAC Read Index**	**17-38**
	7-0	W	Index to palette register to be read	
3C7			**DAC Status**	**17-39**
	1-0	R	Shows whether previous DAC cycle was a read or write	
	7-2	R	Reserved	
3C8	–		**DAC Write Index**	**17-39**
	7-0	R/W	Index to palette register to be written	
3C9			**DAC Data**	**17-40**
	7-0	R/W	Data from register pointed to by DAC Read or Write Index	

A.2 EXTENDED SEQUENCER REGISTERS

Table A-2. Extended Sequencer Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**08**		**Unlock Extended Sequencer (SR8)**	**18-1**
	7-0	R/W	Load xxxx0110b to unlock SR9-SR1C	
3C5	**09**	**R/W**	**Extended Sequencer 9**	**18-2**
	6-0	R/W	Reserved = 1	
	7	R/W	Memory-mapped I/O only (no PIO)	
3C5	**0A**		**Extended Sequencer A (SRA)**	**18-3**
	4-0	R/W	Reserved	
	5	R/W	PD[63:0] not tri-stated	
	6	R/W	Reserved	
	7	R/W	2 MCLK memory writes	
3C5	**0D**		**Extended Sequencer D (SRD)**	**18-4**
	0	R/W	Drive LPBEN pin with logic 1	
	3-1	R/W	Reserved	
	3-1	R/W	Reserved	
	5-4	R/W	HSYNC control for Green PC requirements	
	7-6	R/W	VSYNC control for Green PC requirements	
3C5	**09**		**Extended Sequencer 9 (SR9)**	**18-2**
	1-0	R/W	Reserved	
	2	R/W	Controller 1 virtual DCLK off when CR67_3-2 = 11b	
	3	R/W	Controller 1 virtual DCLK off in Standby	
	4	R/W	Controller 1 virtual DCLK off in Suspend	
	5	R/W	Controller 1 true DCLK off in Standby	
	6	R/W	Controller 1 true DCLK off in Suspend	
	7	R/W	MMIO-only	
3C5	**10**		**MCLK Value Low (SR10)**	**18-5**
	4-0	R/W	MCLK N-divider value	
	6-5	R/W	MCLK R value	
	7	R/W	Reserved	
3C5	**11**		**MCLK Value High (SR11)**	**18-5**
	6-0	R/W	MCLK M-divider value	
	7	R/W	Reserved	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**12**		**DCLK Value Low (SR12)**	**18-6**
	5-0	R/W	DCLK N-divider value	
	7-6	R/W	DCLK R value	
3C5	**13**		**DCLK Value High (SR13)**	**18-6**
	7-0	R/W	DCLK M-divider value	
3C5	**14**		**CLKSYN Control 1 (SR14)**	**18-7**
	0	R/W	DCLK PLL powered down (test only)	
	1	R/W	MCLK PLL powered down (test only)	
	3	R/W	Test MCLK (test only)	
	4	R/W	Clear clock synthesizer counters (test only)	
	5	R/W	Pin 146 tri-stated	
	6	R/W	MCLK is input on pin N1 (test only)	
	7	R/W	DCLK is input on pin A1 (test only)	
3C5	**15**		**CLKSYN Control 2 (SR15)**	**18-8**
	0	R/W	Load new MCLK frequency	
	1	R/W	Load new DCLK frequency	
	2	R/W	MCLK output on pin C3 (test only)	
	3	R/W	DCLK output on pin M1 (test only)	
	4	R/W	Divide DCLK by 2	
	5	R/W	Load MCLK and DCLK PLL values immediately	
	6	R/W	Invert DCLK	
	7	R/W	Enable 2 MCLK memory writes	
3C5	**16**		**CLKSYN Test High (SR16)**	**18-9**
	7-0	R/W	Reserved	
3C5	**17**		**CLKSYN Test High (SR17)**	**18-10**
	7-0	R/W	Reserved	
3C5	**18**		**RAMDAC/CLKSYN Control (SR18)**	**18-10**
	0	R/W	RAMDAC test counter enabled (test only)	
	1	R/W	Reset RAMDAC test counter	
	2	R/W	Place red data on internal data bus (test only)	
	3	R/W	Place green data on internal data bus (test only)	
	4	R/W	Place blue data on internal data bus (test only)	
	5	R/W	Power-down RAMDAC	
	6	R/W	Select 1 cycle CLUT write	
	7	R/W	RAMDAC clock doubled mode enabled	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**1A**		**Extended Sequencer 1A (SR1A)**	**18-11**
	3-0	R/W	Reserved	
	5-4	R/W	Select functions of pins C3 and C15	
	6	R/W	Reserved	
	7	R/W	RAMDAC and CLUTs powered with 5V (overrides SR1B_0)	
3C5	**1B**		**Extended Sequencer 1B (SR1B)**	**18-12**
	0	R	RAMDAC and CLUTs powered with 5V	
	7-1	R/W	Reserved = 1	
3C5	**1C**		**Extended Sequencer 1C (SR1C)**	**18-12**
	1-0	R/W	Reserved	
	2	R/W	TV encoder clock off when encoder disabled	
	3	R/W	TV encoder clock off in Standby	
	4	R/W	TV encoder clock off in Suspend	
	5	R/W	LCLK off when LPB disabled	
	6	R/W	LCLK off in Standby	
	7	R/W	LCLK off in Suspend	
3C5	**1D**		**Extended Sequencer 1D (SR1D)**	**18-13**
	2-0	R/W	Reserved	
	3	R/W	SP DCLK branch 1 off when SP disabled	
	4	R/W	SP DCLK branch 1 off in Standby	
	5	R/W	SP DCLK branch 1 off in Suspend	
	6	R/W	SP DCLK branch 2 off in Standby	
	7	R/W	SP DCLK branch 2 off in Suspend	
3C5	**1E**		**Extended Sequencer 1E (SR1E)**	**18-14**
	0	R/W	Controller 1 DCLK off when Controller 1 disabled	
	1	R/W	Reserved	
	2	R/W	Controller 2 DCLK off when Controller 2 disabled	
	3	R/W	Controller 2 DCLK off in Standby	
	4	R/W	Controller 2 DCLK off in Standby	
	6-5	R/W	Reserved	
	7	R/W	Bus interface SCLK off in Suspend	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**1F**		**Extended Sequencer 1F (SR1F)**	**18-15**
	0	R/W	GE MCLK off in Suspend	
	1	R/W	DM MCLK off in Suspend	
	2	R/W	BIU MCLK off in Suspend	
	3	R/W	LPB MCLK off in Suspend	
	4	R/W	Controller 1 and 2/SP MCLK off in Suspend	
	5	R/W	Enable MCLK off in Suspend	
	6	R/W	Reserved	
	7	R/W	Flat panel MCLK branch off in Suspend	
3C5	**20**		**Extended Sequencer 20 (SR20)**	**18-16**
	0	R/W	Reserved	
	1	R/W	DAC off in Standby	
	2	R/W	DAC off in Suspend	
	3	R/W	DCLK PLL off in Suspend	
	4	R/W	MCLK PLL off in Suspend	
	6-5	R/W	Reserved	
	7	R/W	Pads in suspend configuration in Suspend	
3C5	**21**		**Extended Sequencer 21 (SR21)**	**18-17**
	0	R/W	Disable CLUT1	
	1	R/W	Disable monitor sense circuit	
	2	R/W	CLUT1 powered down in Standby	
	3	R/W	CLUT1 powered down in Suspend	
	4	R/W	Disable CLUT2	
	5	R/W	CLUT2 powered down when Controller 2 diasabled	
	6	R/W	CLUT2 powered down in Standby	
	7	R/W	CLUT2 powered down in Suspend	
3C5	**22**		**DCLK0 Value Low (SR22)**	**18-18**
	5-0	R/W	DCLK0 N-divider value	
	7-6	R/W	DCLK0 R value	
3C5	**23**		**DCLK0 Value High (SR23)**	**18-18**
	7-0	R/W	DCLK0 M-divider value	
3C5	**24**		**DCLK1 Value Low (SR24)**	**18-19**
	5-0	R/W	DCLK1 N-divider value	
	7-6	R/W	DCLK1 R value	
3C5	**25**		**DCLK1 Value High (SR25)**	**18-19**
	7-0	R/W	DCLK1 M-divider value	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**26**		**Paired Register Read/Write Select (SR26)**	**18-20**
	0	R/W	Certain CRTC register reads are disabled for controller 1	
	1	R/W	Reads of all paired controller 1 registers are disabled	
	2	R/W	Enable writes to controller 2 registers	
	3	R/W	Disable writes to controller 1 registers	
	7-4	R/W	Reserved	
3C5	**27**		**MCLK Control (SR27)**	**18-21**
	1-0	R/W	Select IMCKL source	
	3-2	R/W	Select MCLK divider	
	7-4	R/W	Reserved	
3C5	**28**		**DCLK Control (SR28)**	**18-22**
	1-0	R/W	Select IDCKLA source	
	3-2	R/W	Select DCLK1 divider	
	5-4	R/W	Select IDCKLB source	
	7-6	R/W	Select DCLK2 divider	
3C5	**29**		**Flat Panel Frame Buffer (SR29)**	**18-23**
	1-0	R/W	STN write FIFO threshold	
	5-2	R/W	STN read FIFO threshold	
	7-6	R/W	Controller 2 FIFO threshold	
3C5	**30**		**Architectural Configuration (SR30)**	**18-24**
	0	R/W	Select single or dual-scan panel	
	7-1	R/W	Reserved	
3C5	**31**		**Flat Panel Display Mode (SR31)**	**18-24**
	0	R/W	CRT test mode	
	1	R/W	Select flat panel data source	
	2	R/W	Select CRT/TV data source	
	3	R/W	Controller test mode	
	4	R/W	Enable flat panel display	
	5	R/W	Reserved	
	6	R/W	Hardware icon controlled by controller 2	
	7	R/W	Hardware cursor controlled by controller 2	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**32**		**Flat Panel Polarity Control (SR32)**	**18-26**
	0	R/W	Tri-state memory interface signals	
	1	R/W	CRT HSYNC polarity during simultaneous display	
	2	R/W	CRT VSYNC polarity during simultaneous display	
	3	R/W	Reserved	
	4	R/W	Flat panel data polarity	
	5	R/W	FPDE polarity is active low	
	6	R/W	FPHSYNC/LP polarity is active low	
	7	R/W	FPVSYNC/FLM polarity is active low	
3C5	**34**		**Flat Panel AC Modulation (SR34)**	**18-27**
	6-0	R/W	Clock period units for MOD pulse	
	7	R/W	Enable MOD output on pin B15	
3C5	**35**		**Flat Panel Modulation Clock Select (SR35)**	**18-27**
	3-0	R/W	Reserved	
	4	R/W	MOD clock select	
	7-5	R/W	Reserved	
3C5	**36**		**Flat Panel Dither Control (SR36)**	**18-28**
	0	R/W	Select number of bits for dithering	
	2-1	R/W	Reserved	
	5-3	R/W	Select number of bits in the base color	
	7-6	R/W	Dither control	
3C5	**37**		**Flat Panel FRC Weight Select RAM (SR37)**	**18-28**
	3-0	R/W	Weight select value pointer	
	7-4	R/W	Reserved	
3C5	**38**		**Flat Panel FRC Weight Select RAM Data (SR38)**	**18-29**
	7-0	R/W	Weight select data	
3C5	**39**		**Flat Panel Algorithm Control (SR39)**	**18-29**
	1-0	R/W	Select STN or TFT panel type	
	2	R/W	Reserved	
	4-3	R/W	Select FRC gray levels	
	7-5	R/W	Reserved	
3C5	**3A**		**Flat Panel FRC Tuning 1 (SR3A)**	**18-30**
	7-0	R/W	FRC tuning data 15-8	
3C5	**3B**		**Flat Panel FRC Tuning 2 (SR3B)**	**18-30**
	7-0	R/W	FRC tuning data 7-0	
3C5	**3C**		**Flat Panel FRC Tuning 3 (SR3C)**	**18-30**
	1-0	R/W	FRC tuning	
	2	R/W	STN test mode	
	7-2	R/W	Reserved	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**3D**		**Flat Panel Configuration 1 (SR3D)**	**18-31**
	2-0	R/W	Data output format	
	3	R/W	Panel output configuration select	
	4	R/W	Disable LP and FPSCLK during vertical blank	
	5	R/W	Disable FPSCLK during first line of vertical blank	
	6	R/W	Select flat panel data drive strength	
	7	R/W	Select the FPSCLK drive stregth	
3C5	**40**		**Flat Panel Dither Control (SR40)**	**18-32**
	0	R/W	Reserved	
	3-1	R/W	FPSCLK delay	
	4	R/W	Force flat panel data and control signals low	
	5	R/W	FPSCLK forced low during non-display interval	
	6	R/W	Double edge pixel clocking for TFT panels	
	7	R/W	Enable FPPOL output	
3C5	**41**		**Flat Panel Power Sequence Control (SR41)**	**18-33**
	1-0	R/W	Reserved	
	2	R/W	Power down phase timing	
	3	R/W	Power up phase timing	
	5-4		Reserved	
	7-6	R/W	Standy timer resolution	
3C5	**42**		**Flat Panel Power Management Control (SR42)**	**18-33**
	0	R/W	Reserved	
	1	R/W	Enable software suspend	
	3-2	R/W	Reserved	
	4	R/W	Enable hardware standby	
	5	R/W	Enable software standby	
	7-6	R/W	Suspend debounce timer value	
3C5	**43**		**Flat Panel Standby Control (SR43)**	**18-34**
	5-0	R/W	Standby timer timeout value	
	6	R/W	Enable activity mode	
	7	R/W	Reserved	
3C5	**44**		**Flat Panel Power Management (SR44)**	**18-34**
	3-0	R/W	Reserved	
	4	R	Specify STANDBY pin function	
	7-5	R	Reserved	
3C5	**45**		**Flat Panel PLL Power Management (SR45)**	**18-35**
	1-0	R/W	Suspend to PLL power down time	
	3-2	R/W	Select DRAM refresh type	
	7-4	R/W	Reserved	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**46**		**Flat Panel Power Management Status (SR46)**	**18-36**
	4-0	R	Reserved	
	5	R	1 = in Standby mode	
	6	R	1 = in idle power down state	
	7	R	1 = in idle power up state	
3C5	**47**		**CLUT Control (SR47)**	**18-36**
	1-0	R/W	Select CLUT for reads and writes	
	7-2	R/W	Reserved	
3C5	**48**		**Icon Mode (SR48)**	**18-37**
	0	R/W	Enable hardware icon	
	1	R/W	Select icon mode	
	2	R/W	Double X size	
	3	R/W	Double Y size	
	6-4	R/W	Select icon map	
	7	R/W	Reserved	
3C5	**49**		**Icon Color Stack (SR49)**	**18-38**
	7-0	R/W	Values for four 24 bits/pixel colors	
3C5	**4A**		**Icon X Position High (SR4A)**	**18-39**
	1-0	R/W	High order 3 bits of icon horizontal position	
	7-2	R/W	Reserved	
3C5	**4B**		**Icon X Position Low (SR4B)**	**18-39**
	7-0	R/W	Low order 8 bits of icon horizontal position	
3C5	**4C**		**Icon Y Position High (SR4C)**	**18-40**
	1-0	R/W	High order 3 bits of icon vertical position	
	7-2	R/W	Reserved	
3C5	**4D**		**Icon Y Position Low (SR4D)**	**18-40**
	7-0	R/W	Low order 8 bits of icon vertical position	
3C5	**4E**		**Icon Address (SR4E)**	**18-41**
	7-0	R/W	Icon map base address	
3C5	**4F**		**Dual-Scan STN Data Address (SR4F)**	**18-41**
	7-0	R/W	STN panel data start address adjustment	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**50**		**Dual-Scan STN Frame Buffer Size Low (SR50)**	**18-42**
	7-0	R	STN frame buffer size low byte	
3C5	**51**		**Dual-Scan STN Frame Buffer Size High (SR51)**	**18-42**
	7-0	R	STN frame buffer size high byte	
3C5	**52**		**Flat Panel PWM Register (SR52)**	**18-43**
	0	R/W	Enable PWM	
	1	R/W	PWM source clock select	
	3-2	R/W	Reserved	
	6-4	R/W	PWM clock divide	
		R/W	Reserved	
3C5	**53**		**Flat Panel PWM Duty Cycle (SR53)**	**18-44**
	7-0	R/W	Specify PWM duty cycle	
3C5	**54**		**Flat Panel Horizontal Compensation 1 (SR54)**	**18-44**
	1-0	R/W	Text mode horizontal expansion	
	3-2	R/W	Graphics mode horizontal expansion	
	4	R/W	Enable horizontal centering	
	6-5	R/W	Reserved	
	7	R/W	Enable line graphics character codes	
3C5	**55**		**Flat Panel Horizontal Compensation 2 (SR55)**	**18-45**
	0	R/W	Enable 40-character text mode horizontal expansion	
	1	R/W	Enable 80-character text mode horizontal expansion	
	2	R/W	Enable 640-column graphics mode horizontal expansion	
	3	R/W	Enable 800-column graphics mode horizontal expansion	
	4	R/W	Enable 1024-column graphics mode horizontal expansion	
		R/W	Reserved	
3C5	**56**		**Flat Panel Horizontal Compensation 1 (SR56)**	**18-46**
	1-0	R/W	Text mode vertical expansion	
	3-2	R/W	Graphics mode vertical expansion	
	4	R/W	Enable vertical centering	
	7-5	R/W	Reserved	
3C5	**57**		**Flat Pane Vertical Compensation 1 (SR57)**	**18-47**
	0	R/W	Enable 350-line text mode vertical expansion	
	1	R/W	Enable 200/400-line text mode vertical expansion	
	2	R/W	Enable 350-line graphics mode vertical expansion	
	3	R/W	Enable 200/400-line graphics mode vertical expansion	
	4	R/W	Enable 480-line graphics mode vertical expansion	
	5	R/W	Enable 600-line graphics mode vertical expansion	
	6	R/W	Enable 768-line graphics mode vertical expansion	
	7	R/W	Reserved	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**58**		**Flat Panel Horizontal Border (SR58)**	**18-48**
	7-0	R	Character clocks per horizontal line not used by video image	
3C5	**59**		**Flat Panel Horizontal Expansion Factor (SR59)**	**18-48**
	0	R	Bit 8 of SR58	
	3-1	R	Reserved	
	6-4	R	Horizontal expansion factor	
	7	R	Reserved	
3C5	**5A**		**Flat Panel Vertical Border (SR5A)**	**18-49**
	7-0	R	Number of lines not used by video image	
3C5	**5B**		**Flat Panel Horizontal Expansion Factor (SR5B)**	**18-49**
	0	R	Bit 8 of SR5A	
	1	R	Automatic vertical expansion detect	
	2	R	Automatic vertical centering detect	
	3	R	0 = Current scan line will be repeated on next scan line	
	6-4	R	Vertical expansion factor	
	7	R	Reserved	
3C5	**5C**		**Flat Panel Display Enable Position Control (SR5C)**	**18-50**
	3-0	R/W	Display enable start postion for Controller 1	
	7-4	R/W	Display enable start position for Controller 2	
3C5	**5D**		**Flat Panel/CRT Sync Position Control (SR5D)**	**18-51**
	3-0	R/W	Sync start position for Controller 1	
	7-4	R/W	Sync start position for Controller 2	
3C5	**5F**		**FIFO Control (SR5F)**	**18-51**
	0	R/W	Controller 1 FIFO memory access requests disabled (test)	
	1	R/W	Controller 2 FIFO memory access requests disabled (test)	
	2	R/W	STN Write FIFO memory access requests disabled (test)	
	3	R/W	SNT READ FIFO memory access requests disabled (test)	
	4	R/W	1 MCLK reads for Controller 2 FIFO	
	7-5	R/W	Reserved	
3C5	**60**		**Flat Panel Horizontal Total (SR60)**	**18-52**
	7-0	R/W	character clocks/line - 5	
3C5	**61**		**Flat Panel Horizontal Panel Size (SR61)**	**18-53**
	7-0	R/W	Horizontal panel resolution - 1	
3C5	**62**		**Flat Panel Horizontal Blank Start (SR63)**	**18-53**
	7-0	R/W	Character clock counter value at blank start	
3C5	**63**		**Flat Panel Horizontal Blank End (SR63)**	**18-54**
	4-0	R/W	Character clock counter value at blank end	
	7-5	R/W	Reserved	

Table A-2. Extended Sequencer Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3C5	**64**		**Flat Panel Horizontal Sync Start (SR64)**	**18-54**
	7-0	R/W	Character clock counter value at sync start	
3C5	**65**		**Flat Panel Horizontal Sync End (SR65)**	**18-55**
	4-0	R/W	Character clock counter value at sync end	
	6-5	R/W	Reserved	
	7	R/W	Horizontal sync end bit 5	
3C5	**66**		**Flat Panel Horizontal Overflow (SR66)**	**18-55**
	0	R/W	Flat panel horizontal total bit 8	
	1	R/W	Flat panel horizontal panel size bit 8	
	2	R/W	Flat panel horizontal blank start bit 8	
	3	R/W	Flat panel horizontal blank period greater than 64 char clocks	
	4	R/W	Flat panel horizontal sync start bit 8	
	5	R/W	Flat panel horizontal sync period greater than 32 char clocks	
	7-6	R/W	Reserved	
3C5	**68**		**Flat Panel Vertical Total (SR68)**	**18-56**
	7-0	R/W	Scan lines between vertical syncs - 2	
3C5	**69**		**Flat Panel Vertical Panel Size (SR69)**	**18-57**
	7-0	R/W	Vertical panel resolution - 1	
3C5	**6A**		**Flat Panel Vertical Blank Start (SR6A)**	**18-57**
	7-0	R/W	Scan line counter value at blank start - 1	
3C5	**6B**		**Flat Panel Vertical Blank End (SR6B)**	**18-58**
	4-0	R/W	Scan line counter value at blank end	
	7-5	R/W	Reserved	
3C5	**6C**		**Flat Panel Vertical Sync Start (SR6C)**	**18-58**
	7-0	R/W	Scan line counter value at sync start - 1	
3C5	**6D**		**Flat Panel Vertical Sync End (SR6D)**	**18-59**
	3-0	R/W	Scan line counter value at sync end	
	7-4	R/W	Reserved	
3C5	**6E**		**Flat Panel Vertical Overflow 1 (SR6E)**	**18-59**
	2-0	R/W	Flat panel vertical total bits 10-8	
	3	R/W	Reserved	
	6-4	R/W	Flat panel vertical panel size bits 10-8	
	7	R/W	Reserved	
3C5	**6F**		**Flat Panel Vertical Overflow 2 (SR6F)**	**18-60**
	2-0	R/W	Flat panel vertical blank start bits 10-8	
	3	R/W	Reserved	
	6-4	R/W	Flat panel vertical sync start bits 10-8	
	7	R/W	Reserved	

A.3 EXTENDED CRTC REGISTERS

All of these registers are read/write protected at power-up by hardware reset. In order to read/write these registers, the Register Lock 1 register (CR38) must be loaded with a binary unlock key pattern (see the register description). CTR registers are unlocked by setting CR39 = A5H. The registers will remain unlocked until the key pattern is reset. ? = B for monochrome, D for color.

Table A-3. Extended CRTC Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**22**	R/W	**CRT Test 1(CTR22)**	**19-1**
	6-0	R/W	Reserved	
	7	R/W	Provide pixel data to DAC (Test) - Paired	
3?5	**2D**		**Device ID High (CR2D)**	**19-2**
	7-0	R	High byte of device ID (88H)	
3?5	**2E**		**Device ID Low (CR2E)**	**19-2**
	7-0	R	Low byte of device ID (12H)	
3?5	**2F**		**Revision (CR2F)**	**19-2**
	7-0	R	4x	
3?5	**30**		**Chip ID/Rev (CR30)**	**19-3**
	7-0	R	Chip Identification - E1H	
3?5	**31**		**Memory Configuration (CR31)**	**19-3**
	0	R/W	Reserved	
	1	R/W	Enable two-page screen image	
	2	R/W	Enable VGA 16-Bit Memory Bus Width	
	3	R/W	Use Enhanced mode memory mapping	
	5-4	R/W	Reserved	
	6	R/W	Enable high speed text display font fetch mode - Paired	
	7	R/W	Reserved	
3?5	**32**		**Backward Compatibility 1 (CR32)**	**19-4**
	1-0	R/W	Reserved	
	2	R/W	Force internal dot clock to be not divided by 2	
	3	R/W	Reserved	
	4	R/W	Enable interrupt generation	
	5	R/W	Reserved	
	6	R/W	Standard VGA memory wrap at 256K boundary	
	7	R/W	Reserved	

Table A-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**33**		**Backward Compatibility 2 (CR33)**	**19-5**
	0	R/W	Reserved	
	1	R/W	Disable write protection provided by CR11_7 on CR7_1,6	
	2	R/W	Reserved	
	3	R/W	VCLK is inverted DCLK - Paired	
	4	R/W	Disable writes to RAMDAC registers (3C6H-3C9H) - Paired	
	5	R/W	BLANK signal active during non-active video period - Paired	
	6	R/W	Disable writes to AR0-ARF registers - Paired	
	7	R/W	Reserved	
3?5	**34**		**Backward Compatibility 3 (CR34)**	**19-6**
	0	R/W	PCI DAC snoop method select	
	1	R/W	Disable PCI master abort handling during DAC snoop	
	2	R/W	Disable PCI retry handling during DAC snoop	
	3	R/W	Reserved	
	4	R/W	Enable Display Start FIFO Fetch register (CR3B) - Paired	
	5	R/W	Force to 8 dots/character text mode	
	6	R/W	Reserved	
	7	R/W	Lock 3C2H_3-2 (DCLK select)	
3?5	**35**		**CRT Register Lock (CR35) - Paired**	**19-7**
	3-0	R/W	Reserved	
	4	R/W	Lock Vertical Timing registers	
	5	R/W	Lock Horizontal Timing registers	
	6	R/W	Lock CR1 and 3C2H_6	
	7	R/W	Lock CR12 and 3C2H_7	
3?5	**36**		**Configuration 1 (CR36)**	**19-8**
	1-0	R/W	Reserved	
	3-2	R/W	Select Memory page mode (fast page, EDO or 1-cycle EDO)	
	4	R/W	Reserved	
	7-5	R/W	Define display memory size	
3?5	**37**		**Configuration 2 (CR37)**	**19-8**
	0	R/W	Reserved	
	1	R/W	Disable test mode (outputs tri-stated)	
	2	R/W	Reserved	
	3	R/W	Use internal MCLK, DCLK	
	4	R/W	Reserved	
	7-5	R/W	Define panel type	

Table A-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**38**		**Register Lock 1 (CR38) - Shared**	**19-10**
	7-0	R/W	Unlock S3 VGA registers (CR30-CR3C)	
3?5	**39**		**Register Lock 2 (CR39) - Shared**	**19-10**
	7-0	R/W	Unlock System Control and System Extension registers	
	1-0	R/W	Select alternate refresh count per horizontal line	
	2	R/W	Enable alternate refresh count (CR3A_1-0)	
	3	R/W	Enable simultaneous VGA text and Enhanced modes - Paired	
	4	R/W	Enable 8-, 16- or 24/32-bit color Enhanced modes - Paired	
	5	R/W	Enable high speed text font writing	
	6	R/W	Reserved	
	7	R/W	Disable PCI bus read burst cycles	
3?5	**3A**		**Miscellaneous 1 (CR3A)**	**19-10**
3?5	**3B**		**Start Display FIFO Fetch (CR3B) - Paired**	**19-11**
	7-0	R/W	Specify start of display FIFO fetches for screen refreshing	
3?5	**3C**		**Interlace Retrace Start (CR3C) - Paired**	**19-12**
	7-0	R/W	Specify interlaced mode retrace start position	
3?5	**3D**		**NTSC/PAL Control (CR3D)**	**19-12**
	0	R/W	Enable TV mode	
	3-1	R/W	Select TV output	
	4	R/W	Select black and white video	
	5	R/W	Select NTSC or PAL	
	7-6	R/W	Reserved	

Table A-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**40**		**System Configuration (CR40)**	**19-13**
	0	R/W	Enable Enhanced mode register access	
	7-1	R/W	Reserved	
3?5	**41**		**BIOS Flag (CR41)**	**19-13**
	7-0	R/W	Used by the video BIOS	
3?5	**42**		**Mode Control (CR42)**	**19-13**
	4-0	R/W	Reserved	
	5	R/W	Select Interlaced mode - Paired	
	7-6	R/W	Reserved	
3?5	**43**		**Extended Mode (CR43) - Paired**	**19-14**
	2-0	R/W	Reserved	
	3	R/W	Select character blink rate	
	4	R/W	Reserved	
	6-5	R/W	Select cursor blink rate	
	7	R/W	Enable horizontal counter double mode	
3?5	**45**		**Hardware Graphics Cursor Mode (CR45)**	**19-14**
	0	R/W	Enable hardware graphics cursor	
	3-1	R/W	Reserved	
	4	R/W	Set up space at right of bit map for hardware cursor	
	7-5	R/W	Reserved	

Table A-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**46–47**		**Hardware Graphics Cursor Origin-X (CR46-CR47)**	**19-15**
	10-0	R/W	X-coordinate of the hardware cursor left side	
	15-11	R/W	Reserved	
3?5	**48–49**		**Hardware Graphics Cursor Origin-Y (CR48-CR49)**	**19-15**
	10-0	R/W	Y-coordinate of the hardware cursor upper line	
	15-11	R/W	Reserved	
3?5	**4A**		**Hardware Graphics Cursor Foreground Stack (CR4A)**	**19-16**
	7-0	R/W	Hardware cursor foreground color (3 registers)	
3?5	**4B**		**Hardware Graphics Cursor Background Stack (CR4B)**	**19-16**
	7-0	R/W	Hardware cursor background color (3 registers)	
3?5	**4C–4D**		**Hardware Graphics Cursor Start Address (CR4C-CR4D)**	**19-16**
	12-0	R/W	Hardware cursor start address	
	15-13	R/W	Reserved	
3?5	**4E**		**Hardware Graphics Cursor Pattern Display Start X-Pixel Position (CR4E)**	**19-17**
	5-0	R/W	Hardware cursor display start x-coordinate	
	7-6	R/W	Reserved	
3?5	**4F**		**Hardware Graphics Cursor Pattern Display Start Y-Pixel Position (CR4F)**	**19-17**
	5-0	R/W	Hardware cursor display start y-coordinate	
	7-6	R/W	Reserved	

Table A-3. Extended CRTC Registers (continued)

Add dress	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**50**		**Extended System Cont 1 (CR50)**	**19-18**
	0	R/W	Most significant bit of screen width definition (see bits 7-6)	
	3-1	R/W	Reserved	
	5-4	R/W	Pixel length select	
	7-6	R/W	With bit 0, screen width definition	
3?5	**51**		**Extended System Cont 2 (CR51) - Paired**	**19-18**
	3-0	R/W	Reserved	
	5-4	R/W	Logical screen width bits 9-8	
	7-6	R/W	Reserved	
3?5	**52**		**Extended BIOS Flag 1 (CR52)**	**19-19**
	7-0	R/W	Used by the video BIOS	
3?5	**53**		**Extended Memory Cont 1 (CR53)**	**19-19**
	0	R/W	Reserved	
	2-1	R/W	Big endian byte swap select for linear addressing	
	4-3	R/W	Memory-mapped I/O type select	
	5	R/W	MMIO window select (A8000H or B8000H)	
	6	R/W	Enable nibble swap	
	7	R/W	Reserved	
3?5	**54**		**Extended Memory Cont 2 (CR54)**	**19-20**
	1-0	R/W	Big endian byte swap select (not linear addressing or image transfers)	
	2, 7-3	R/W	Specify M parameter for CPU and Graphics Engine accesses	
3?5	**55**		**Extended DAC Control (CR55)**	**19-20**
	3-0	R/W	Reserved	
	3	R/W	Reserved	
	4	R/W	Enable X-11 windows hardware cursor mode	
	7-5	R/W	Reserved	
3?5	**56**		**External Sync Cont 1 (CR56)**	**19-21**
	0	R/W	Reserved	
	1	R/W	HSYNC output buffer tri-stated	
	2	R/W	VSYNC output buffer tri-stated	
	7-3	R/W	Reserved	

Table A-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**58**		**Linear Address Window Control (CR58)**	**19-22**
	1-0	R/W	Linear addressing window size	
	3-2	R/W	Reserved	
	4	R/W	Enable linear addressing	
	6-5	R/W	Reserved	
	7	R/W	RAS pre-charge timing adjustment	
3?5	**59-5A**		**Linear Address Window Position (CR59-5A)**	**19-23**
	15-0	R/W	Linear addressing window position bits 31-16	
3?5	**5C**		**General Out Port (CR5C)**	**19-24**
	7-0	R/W	General Output Port	
3?5	**5D**		**Extended Horizontal Overflow (CR5D)**	**19-24**
	0	R/W	Horizontal total bit 8 (CR0)	
	1	R/W	Horizontal display end bit 8 (CR1)	
	2	R/W	Start horizontal blank bit 8 (CR2)	
	3	R/W	End horizontal blank bit 7 (CR3, CR5)	
	4	R/W	Start horizontal sync position bit 8 (CR4)	
	5	R/W	End horizontal sync position bit 6 (CR5)	
	6	R/W	Start FIFO Fetch bit 8 (CR3B)	
	7	R/W	Reserved	
3?5	**5E**		**Extended Vertical Overflow (CR5E)**	**19-25**
	0	R/W	Vertical total bit 10 (CR6)	
	1	R/W	Vertical display end bit 10 (CR12)	
	2	R/W	Start vertical blank bit 10 (CR15)	
	3	R/W	Reserved	
	4	R/W	Vertical retrace start bit 10 (CR10)	
	5	R/W	Reserved	
	6	R/W	Line compare position bit 10 (CR18)	
	7	R/W	Reserved	
3?5	**60**		**Extended Memory Control 3 (CR60)**	**19-25**
	7-0	R/W	Specify N parameter for primary stream FIFO control	
3?5	**61**		**Extended Memory Control 4 (CR61)**	**19-26**
	4-0	R/W	Reserved	
	6-5	R/W	Big endian byte swap select for image writes	
	7	R/W	Reserved	
3?5	**63**		**Horizontal Timing Control (CR63)- Paired**	**19-26**
	2-0	R/W	Delay horizontal timing parameters by DCLKs	
	4-3	R/W	Delay horizontal timing parameters by character clocks	
	7-5	R/W	Reserved	

Table A-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**65**		**Extended Miscellaneous Control (CR65)- Paired**	**19-27**
	2-0	R/W	Reserved	
	4-3	R/W	Delay BLANK by DCLK	
	7-5	R/W	Reserved	
3?5	**66**		**Extended Miscellaneous Control 1 (CR66)**	**19-27**
	0	R/W	Enable enhanced functions - Paired	
	1	R/W	Software reset of the Graphics Engine	
	2	R/W	Reserved	
	3	R/W	PCI disconnect on write with FIFO full or read with FIFO empty	
	6-4	R/W	Reserved	
	7	R/W	Enable PCI bus disconnect	
3?5	**67**		**Extended Miscellaneous Control 2 (CR67) - Paired**	**19-28**
	0	R/W	VCLK is in phase with DCLK	
	1	R/W	Reserved	
	3-2	R/W	Streams Processor mode select	
	7-4	R/W	Select RAMDAC color mode	
3?5	**68**		**Configuration 3 (CR68)**	**19-29**
	1-0	R/W	CAS, OE stretch time selection	
	2	R/W	RAS low timing select	
	3	R/W	RAS precharge timing select	
	6-4	R/W	Video BIOS area	
	7	R/W	Reserved	
3?5	**69**		**Extended System Control 3 (CR69) - Paired**	**19-30**
	2-0	R/W	Display start address bits 18-16	
	7-3	R/W	Reserved	
3?5	**6A**		**Extended System Control 4 (CR6A)**	**19-30**
	4-0	R/W	CPU base address bits 18-14	
	7-5	R/W	Reserved	
3?5	**6B**		**Extended BIOS Flag 3 (CR6B)**	**19-31**
	7-0	R/W	Used by the video BIOS	
3?5	**6C**		**Extended BIOS Flag 4 (CR6C)**	**19-31**
	7-0	R/W	Used by the video BIOS	
3?5	**6D**		**Extended BIOS Flag 5 (CR6D)**	**19-31**
	7-0	R/W	Used by the video BIOS	
3?5	**6E**		**Extended BIOS Flag 6 (CR6E)**	**19-32**
	7-0	R/W	Used by the video BIOS	

Table A-3. Extended CRTC Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
3?5	**6F**		**Configuration 4 (CR6F)**	**19-32**
	0	R/W	Reserved	
	1	R/W	Select I/O address for Serial Port register	
	2	R/W	Disable effect of bit 1 of this register	
	4-3	R/W	WE delay	
	7-5	R/W	Reserved	
3?5	**71**		**Extended Miscellaneous Control 2 (CR71) - Paired**	**19-33**
	0	R/W	Reserved	
	1	R/W	Screen off bit select	
	4-2	R/W	Reserved	
	5	R/W	Screen off	
	7-6	R/W	Reserved	
3?5	**72**		**Extended Memory Control 5 (CR72)**	**19-34**
	7-0	R/W	Secondary stream FIFO N parameter value	
3?5	**73**		**Extended Memory Control 6 (CR73)**	**19-34**
	7-0	R/W	Controller 2 FIFO N parameter value	
3?5	**74**		**Extended Memory Control 7 (CR74**	**19-35**
	1-0	R/W	Reserved	
	2	R/W	1 MCLK STN FIFO reads/writes	
	7-3	R/W	Reserved	
3?5	**75**		**Extended Memory Control 8 (CR75)**	**19-35**
	7-0	R/W	STN FIFO N parameter value	
3?5	**76**		**Extended Memory Control 9 (CR76)**	**19-35**
	5-0	R/W	LPB M parameter value	
	7-6	R/W	Reserved	

A.4 ENHANCED COMMANDS REGISTERS

This section lists the registers which support the enhanced drawing functions. All of these registers are enabled only if bit 0 of the System Configuration register (CR40) is set to 1.

Table A-4. Enhanced Commands Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
42E8			**Subsystem Status**	**20-1**
	0	R	Vertical sync interrupt status	
	1	R	Graphics Engine busy interrupt status	
	2	R	Command FIFO overflow interrupt status	
	3	R	Command FIFO empty interrupt status	
	6-4	R	Reserved	
	7	R	4 or 8 bit planes	
	15-8	R	Reserved	
42E8			**Subsystem Control**	**20-2**
	0	W	Clear vertical sync interrupt status	
	1	W	Clear Graphics Engine busy interrupt status	
	2	W	Clear Command FIFO overflow interrupt status	
	3	W	Clear Command FIFO empty interrupt status	
	7-4	W	Reserved	
	8	W	Vertical sync interrupt enabled	
	9	W	Graphics Engine busy interrupt enabled	
	10	W	Command FIFO overflow interrupt enabled	
	11	W	Command FIFO empty interrupt enabled	
	13-12	W	Reserved	
	15-14	W	Graphics Engine software reset selection	
4AE8			**Advanced Function Control**	**20-3**
	0	R/W	Enable Enhanced mode functions	
	1	R/W	Reserved	
	2	R/W	Specify 4 bits/pixel Enhanced mode	
	3	R/W	Reserved	
	4	R/W	Enable linear addressing	
	15-5	R/W	Reserved	
82E8			**Current Y-Position**	**20-4**
	11-0	R/W	Pixel vertical screen coordinate	
	15-12	R/W	Reserved	
86E8			**Current X-Position**	**20-4**
	11-0	R/W	Pixel horizontal screen coordinate	
	15-12	R/W	Reserved	

Table A-4. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
8AE8			**Destination Y Position/Axial Step Constant**	**20-5**
	11-0/ 13-0	R/W	Specifies ending vertical coordinate or axial step constant for a number of drawing commands	
	15-12	R/W	Reserved (Bits 15-14 for step constant)	
8EE8			**Destination X Position/Diagonal Step Constant**	**20-5**
	11-0/ 13-0	R/W	Specifies ending horizontal coordinate or diagonal step constant for a number of drawing commands	
	15-12	R/W	Reserved (Bits 15-14 for step constant)	
92E8			**Line Error Term**	**20-6**
	13-0	R/W	Error term for line draws	
	15-14	R/W	Reserved	
96E8			**Major Axis Pixel Count**	**20-6**
	11-0	R/W	Length of the longest axis (pixels - 1)	
	15-12	R/W	Reserved	
9AE8			**Graphics Processor Status**	**20-7**
	7-0	R	Low 8 bits of field showing FIFO slots available (see bits 15-11)	
	8	R	Reserved	
	9	R	Graphics Engine busy	
	10	R	All FIFO slots empty	
	15-11	R	High 5 bits of FIFO status (see bits 7-0)	
9AE8			**Drawing Command**	**20-8**
	0	W	Must be programmed to 1	
	1	W	Select across the plane pixel mode	
	2	W	Last pixel will not be drawn	
	3	W	Select radial drawing direction	
	4	W	Draw pixels	
	7-5	W	Select drawing direction	
	8	W	Wait for CPU data	
	10-9	W	Select system bus size	
	11	W	Reserved	
	12	W	Enable byte swap	
	15-13	W	Select command type	

Table A-4. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
9EE8			**Short Stroke Vector Transfer**	**20-10**
	3-0	W	Length of vector 1 (pixels - 1)	
	4	W	Draw pixels	
	7-5	W	Select drawing direction	
	15-8	W	Duplicate of bits 7-0 to define second short stroke vector	
A2E8			**Background Color**	**20-11**
	31-0	R/W	Background color value	
A6E8			**Foreground Color**	**20-11**
	31-0	R/W	Foreground Color value	
AAE8			**Bitplane Write Mask**	**20-12**
	31-0	R/W	Each bit enables updating of corresponding bit plane	
AEE8			**Bitplane Read Mask**	**20-12**
	31-0	R/W	Each bit enables reading of corresponding bit plane	
B2E8			**Color Compare**	**20-13**
	31-0	R/W	Color value to be compared with current bitmap color	
B6E8			**Background Mix**	**20-13**
	3-0	W	Select mix type	
	4	W	Reserved	
	6-5	W	Select color source	
	15-7	W	Reserved	
BAE8			**Foreground Mix**	**20-13**
	3-0	W	Select mix type	
	4	W	Reserved	
	6-5	W	Select color source	
	15-7	W	Reserved	
BEE8			**Read Register Data**	**20-14**
	15-0	R	Data from register selected by bits 2-0 of BEE8H_E	
BEE8	**0**		**Minor Axis Pixel Count**	**20-15**
	11-0	W	Rectangle height (pixels - 1)	
	15-12	W	Reserved	
BEE8	**1**		**Top Scissors**	**20-15**
	11-0	W	Top side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**2**		**Left Scissors**	**20-15**
	11-0	W	Left side of the clipping rectangle	
	15-12	W	Reserved	

Table A-4. Enhanced Commands Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
BEE8	**3**		**Bottom Scissors**	**20-16**
	11-0	W	Bottom side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**4**		**Right Scissors**	**20-16**
	11-0	W	Right side of the clipping rectangle	
	15-12	W	Reserved	
BEE8	**A**		**Pixel Control**	**20-16**
	5-0	W	Reserved	
	7-6	W	Select mix register	
	11-8	W	Reserved	
	15-12	W	0AH (index)	
BEE8	**D**		**Multifunction Control Miscellaneous 2**	**20-17**
	2-0	W	Destination base address location in memory	
	3	W	Reserved	
	6-4	W	Source base address location in memory	
	11-7	W	Reserved	
	15-12	W	0DH (index)	
BEE8	**E**		**Multifunction Control Miscellaneous**	**20-18**
	1-0	W	Destination base address bits 21-20	
	3-2	W	Source base address bits 21-20	
	4	W	Select upper word for 32-bit register accesses	
	5	W	Only pixels outside the clipping rectangle are drawn	
	6	W	Reserved	
	7	W	Don't update bitmap if source is not equal to color compare color	
	8	W	Enable color comparison	
	9	W	Select 32-bit command registers	
	11-10	W	Reserved	
	15-12	W	0EH (index)	
BEE8	**F**		**Read Register Select**	**20-19**
	2-0	W	Select register to be read	
	11-4	W	Reserved	
	15-12	W	0FH (index)	
E2E8			**Pixel Data Transfer**	**20-20**
	15-0	W	Data transfer register (CPU to Graphics Engine) - low word	
E2EA			**Pixel Data Transfer-Extension**	**20-20**
	15-0	W	Data transfer register (CPU to Graphics Engine) - high word	

A.5 STREAMS PROCESSOR REGISTERS

Table A-5. Streams Processor Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
8180			**Primary Stream Control**	**21-1**
	23-0	R/W	Reserved	
	26-24	R/W	Primary stream input data format	
	27	R/W	Reserved	
	30-28	R/W	Primary stream filter characteristics	
	31	R/W	Reserved	
8184			**Color/Chroma Key Control**	**21-2**
	7-0	R/W	B/V/Cr key value (lower bound for chroma)	
	15-8	R/W	G/U/Cb key value (lower bound for chroma)	
	23-16	R/W	R/Y key value (lower bound for chroma)	
	26-24	R/W	RGB color comparison precision	
	27	R/W	Reserved	
	28	R/W	Color key control (full compare or bit 16 of 1.5.5.5)	
	31-29	R/W	Reserved	
8190			**Secondary Stream Control**	**21-3**
	11-0	R/W	DDA horizontal accumulator initial value	
	23-12	R/W	Reserved	
	26-24	R/W	Secondary stream input data format	
	27	R/W	Reserved	
	30-28	R/W	Secondary stream filter characteristics	
	31	R/W	Reserved	
8194			**Chroma Key Upper Bound**	**21-4**
	7-0	R/W	V/Cr key value (upper bound)	
	15-8	R/W	U/Cb key value (upper bound)	
	23-16	R/W	Y key value (upper bound)	
	31-24	R/W	Reserved	
8198			**Secondary Stream Stretch/Filter Constants**	**21-4**
	10-0	R/W	K1 horizontal scale factor	
	15-11	R/W	Reserved	
	26-16	R/W	K2 horizontal scale factor	
	31-27	R/W	Reserved	

Table A-5. Streams Processor Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
81A0			**Blend Control**	**21-5**
	1-0	R/W	Reserved	
	4-2	R/W	Secondary stream blend coefficient	
	9-5	R/W	Reserved	
	12-10	R/W	Primary stream blend coefficient	
	23-13	R/W	Reserved	
	26-24	R/W	Compose mode	
	31-27	R/W	Reserved	
81C0			**Primary Stream Frame Buffer Address 0**	**21-6**
	21-0	R/W	Primary stream frame buffer starting address 0	
	31-22	R/W	Reserved	
81C4			**Primary Stream Frame Buffer Address 1**	**21-6**
	21-0	R/W	Primary stream frame buffer starting address 1	
	31-22	R/W	Reserved	
81C8			**Primary Stream Stride**	**21-7**
	11-0	R/W	Primary stream stride	
	31-12	R/W	Reserved	
81CC			**Double Buffer/LPB Support**	**21-7**
	0	R/W	Select primary frame buffer address 1	
	2-1	R/W	Select secondary frame buffer address	
	3	R/W	Reserved	
	4	R/W	Select LPB frame buffer start address 1	
	5	R/W	LPB input buffer select loading at end of frame	
	6	R//w	Selected LPB input buffer toggles at end of frame	
	31-7	R/W	Reserved	
81D0			**Secondary Stream Frame Buffer Address 0**	**21-9**
	21-0	R/W	Secondary stream frame buffer starting address 0	
	31-22	R/W	Reserved	
81D4			**Secondary Stream Frame Buffer Address 1**	**21-9**
	21-0	R/W	Secondary stream frame buffer starting address 1	
	31-22	R/W	Reserved	
81D8			**Secondary Stream Stride**	**21-10**
	11-0	R/W	Secondary stream stride	
	31-12	R/W	Reserved	

Table A-5. Streams Processor Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
81DC			**Blend Control**	**21-10**
	2-0	R/W	Reserved	
	12-3	R/W	Pixel stop fetch position	
	18-13	R/W	Reserved	
	28-19	R/W	Pixel start fetch position	
	29	R/W	Reserved	
	30	R/W	Primary stream on top	
	31	R/W	Enable opaque overlay control	
81E0			**K1 Vertical Scale Factor**	**21-12**
	10-0	R/W	K1 vertical scale factor	
	31-11	R/W	Reserved	
81E4			**K2 Vertical Scale Factor**	**21-12**
	10-0	R/W	K2 vertical scale factor	
	31-11	R/W	Reserved	
81E8			**DDA Vertical Accumulator Initial Value**	**21-13**
	11-0	R/W	DDA vertical accumulator initial value	
	31-12	R/W	Reserved	
81EC			**Streams FIFO and RAS Controls**	**21-13**
	4-0	R/W	Streams FIFO allocation	
	9-5	R/W	Secondary FIFO threshold	
	14-10	R/W	Primary FIFO threshold	
	15	R/W	RAS low time control	
	16	R/W	RAS precharge control	
	17	R/W	Reserved	
	18	R/W	Specify memory size for LPB memory cycles	
	31-19	R/W	Reserved	
81F0			**Primary Stream Window Start Coordinates**	**21-14**
	10-0	R/W	Primary stream Y start	
	15-11	R/W	Reserved	
	26-16	R/W	Primary stream X start	
	31-27	R/W	Reserved	
81F4			**Primary Stream Window Size**	**21-15**
	10-0	R/W	Primary stream height	
	15-11	R/W	Reserved	
	26-16	R/W	Primary stream width	
	31-27	R/W	Reserved	

Table A-5. Streams Processor Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
81F8			**Secondary Stream Window Start Coordinates**	**21-15**
	10-0	R/W	Secondary stream Y start	
	15-11	R/W	Reserved	
	26-16	R/W	Secondary stream X start	
	31-27	R/W	Reserved	
81FC			**Secondary Stream Window Size**	**21-16**
	10-0	R/W	Secondary stream height	
	15-11	R/W	Reserved	
	26-16	R/W	Secondary stream width	
	31-27	R/W	Reserved	

A.6 LOCAL PERIPHERAL BUS REGISTERS

Table A-6. Local Peripheral Bus Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF00			**LPB Mode**	**22-1**
	0	R/W	Enable LPB	
	3-1	R/W	LPB mode	
	4	R/W	Reset LPB	
	5	R/W	Write every other received frame to memory	
	6	R/W	No byte swap for incoming video	
	8-7	R/W	Reserved	
	9	R/W	LPB vertical sync is active high	
	10	R/W	LPB horizontal sync is active high	
	11	W	CPU VSYNC	
	12	W	CPU HSYNC	
	13	W	Load base address currently pointed to	
	15-14	R/W	Reserved	
	17-16	R/W	Maximum compressed data bust size	
	20-18	R/W	Reserved	
	22-21	R/W	Video FIFO threshold	
	23	R/W	Reserved	
	24	R/W	LPB clock driven by LCLK	
	25	R/W	Don't add stride after first HSYNC	
	26	R/W	Invert the LCLK input	
	30-27	R/W	Reserved	
	31	R/W	Reserved	
FF04			**LPB FIFO Status**	**22-4**
	3-0	R	LPB output FIFO status	
	10-4	R	Reserved	
	11	R	LPB output FIFO full	
	12	R	LPB output FIFO empty	
	13	R	LPB output FIFO almost empty	
	21-14	R	Reserved	
	20	R	LPB video FIFO 0 full	
	21	R	LPB video FIFO 0 empty	
	22	R	LPB video FIFO 0 almost empty	
	28-23	R	Reserved	
	29	R	LPB video FIFO 1 full	
	30	R	LPB video FIFO 1 empty	
	31	R	LPB video FIFO 1 almost empty	

Table A-6. Local Peripheral Bus Registers (continued)

Add dress	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF08			**LPB Interrupt Flags**	**22-5**
	0	R/W	LPB Output FIFO empty	
	1	R/W	HSYNC (end of line) input on pin 202	
	2	R/W	VSYNC (end of frame) input on pin 203	
	3	R/W	Serial port start condition detected	
	15-4	R/W	Reserved	
	16	R/W	Enable LPB output FIFO empty interrupt	
	17	R/W	Enable HSYNC (end of line) input interrupt	
	18	R/W	Enable VSYNC (end of frame) input interrupt	
	19	R/W	Enable serial port start condition detect interrupt	
	23-20	R/W	Reserved	
	24	R/W	Drive SPCLK low on receipt of a serial port start condition	
	31-25	R/W	Reserved	
FF0C			**LPB Frame Buffer Address 0**	**22-7**
	21-0	R/W	LPB frame buffer address 0	
	31-22	R/W	Reserved	
FF10			**LPB Frame Buffer Address 1**	**22-7**
	21-0	R/W	LPB frame buffer address 1	
	31-22	R/W	Reserved	
FF14			**LPB Direct Read/Write Address**	**22-8**
	20-0	R/W	Address of MPEG decoder address to read/write	
	23-21	R/W	MPEG decoder transaction type	
	31-24	R/W	Reserved	
FF18			**LPB Direct Read/Write Data**	**22-8**
	31-0	R/W	LPB direct read/write data	
FF1C			**LPB General Purpose Input/Output Port**	**22-9**
	3-0	R/W	General purpose output data port	
	7-4	R	General purpose input data port	
	31-8	R/W	Reserved	

Table A-6. Local Peripheral Bus Registers (continued)

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
FF20			**Serial Port**	**22-9**
	0	R/W	0 = Serial clock write on pin 205, 1 = pin 205 tri-state	
	1	R/W	0 = Serial data write on pin 206, 1 = pin 206 tri-state	
	2	R	0 = Serial clock low on pin 205, 1 = pin 205 tri-state	
	3	R	0 = Serial data low on pin 206, 1 = pin 206 tri-state	
	4	R/W	Enable serial port function	
	5-7	R/W	Reserved	
	8	R	Bit 0 mirror (data on byte lane 2 at E2H)	
	9	R	Bit 1 mirror (data on byte lane 2 at E2H)	
	10	R	Bit 2 mirror (data on byte lane 2 at E2H)	
	11	R	Bit 3 mirror (data on byte lane 2 at E2H)	
	12	R	Bit 4 mirror (data on byte lane 2 at E2H)	
	31-13	R/W	Reserved	
FF24			**LPB Video Input Window Size**	**22-11**
	11-0	R/W	Video input line width	
	15-12	R/W	Reserved	
	24-16	R/W	Video input window height	
	31-25	R/W	Reserved	
FF28			**LPB Video Data Offsets**	**22-12**
	11-0	R/W	Horizontal video data offset	
	15-12	R/W	Reserved	
	24-16	R/W	Vertical video data offset	
	31-25	R/W	Reserved	
FF2C			**LPB Horizontal Decimation Control**	**22-12**
	31-0	R/W	Video data byte mask	
FF30			**LPB Vertical Decimation Control**	**22-13**
	7-0	R	Video data line mask	
FF34			**LPB Line Stride**	**22-13**
	11-0	R/W	Line stride	
	31-12	R/W	Reserved	
FF40			**LPB Output FIFO**	**22-14**
	31-0	R/W	Output FIFO data	

A.7 PCI CONFIGURATION SPACE REGISTERS

When a PCI configuration read or write command is issued, AD[7:0] contain the address of the register in the configuration space to be accessed.

Table A-7. PCI Configuration Space Registers

Address	Index Bit(s)	R/W	Register Name Bit Description	Description Page
00			**Vendor ID**	**23-1**
	15-0	R	Hardwired to 5333H	
02			**Device ID**	**23-2**
	15-0	R	Hardwired to 8812H	
04			**Command**	**23-2**
	0	R/W	Response to I/O space accesses enabled	
	1	R/W	Response to memory space accesses enabled	
	4-2	R/W	Reserved	
	5	R/W	Enable DAC snooping	
	15-6	R/W	Reserved	
06			**Status**	**23-3**
	8-0	R/W	Reserved	
	10-9	R/W	Hardwired to select medium device select timing	
	15-11	R/W	Reserved	
08			**Class Code**	**23-3**
	31-0	R	Hardwired to indicate VGA-compatible display controller and revision level	
10			**Base Address 0**	**23-4**
	0	R/W	Hardwired to indicate base registers map into memory space	
	2-1	R/W	Hardwired to allow mapping anywhere in 32-bit address space	
	3	R/W	Hardwired to indicate does not meet prefetchable requirements	
	22-4	R/W	Reserved	
	31-23	R/W	Base address 0	
30			**BIOS Base Address**	**23-5**
	0	R/W	Enable access to BIOS ROM address space	
	15-1	R/W	Reserved	
	31-16	R/W	Upper 16 bits of BIOS ROM address	
3C			**Interrupt Line**	**23-3**
	7-0	R/W	Interrupt line routing information	
3D			**Interrupt Pin**	**23-6**
	7-0	R	Hardwired to specify use of INTA	

Appendix B: Panel Programming Examples

Programming Example: VGA TFT (640 x 480)

Panel Type: VGA			
Horizontal resolution	640	640	640
Vertical resolution	480	480	480
Dot Clock (MHz)	25.175	31.500	31.500
Horizontal freq (kHz)	31.5	37.9	37.5
Refresh rate (Hz)	60.0	72.0	75.0

Register	Description	Register Value
SR30	Architecture Configuration	01 or 11
SR31	FP Display Mode	10 or D2
SR32	FP Pin Control	06 or F6
SR33	Reserved	00
SR34	FP AC Modulation	01
SR35	FP Miscellaneous Control	10
SR36	FP Dither Control	00, F0, A1, 59
SR37	FP Weight Decode Pointer	00
SR38	FP Weight Decode	00
SR39	FP Algorithm Control	00
SR3A	FP FRC Tuning 1	00
SR3B	FP FRC Tuning 2	00
SR3C	FP FRC Tuning 3	00
SR3D	FP Configuration	01, 00, 02
SR3E	Reserved	00
SR3F	Reserved	00
SR40	FP Pin Configuration	8x, Cx, Ex, 8x
SR41	FP Power Sequence Ctl	00 or 0C
SR42	FP Power Mngmt Ctl	91 or B3
SR43	FP Standby Ctl	01 or 41
SR44	FP Power Mngmt	01 or 10
SR45	FP PLL Power Mngmt	00, 01, 02, 03
SR46	FP Power Mngmt Status	read only
SR47	CLUT Control	00, 01, 02
SR48	Icon Mode	00
SR49	Icon Color Stack	00
SR4A	Icon X Position High	00
SR4B	Icon X Position Low	00
SR4C	Icon Y Position High	00
SR4D	Icon Y Position Low	00
SR4E	Icon Address	00
SR4F	STN Data Address	00

Register	Description	Register Value		
SR50	STN FBSize Low	1F		
SR51	STN FB Size High	1C		
SR52	PWM Control	20, 21		
SR53	PWM Duty Cycle	F7		
SR54	FP H. Compensation	1F		
SR55	FP H. Compensation Ctl	03		
SR56	FP V. Compensation	1F		
SR57	FP V. Compensation Ctl	0F		
SR58	FP H. Border	read only		
SR59	FP H. Expansion Factor	read only		
SR5A	FP V. Border	read only		
SR5B	FP V. Expansion Factor	read only		
SR5C	FP Display Enable Position	77		
SR5D	FP Syncs Position	77		
SR5E	Reserved	00		
SR5F	Reserved	00		
SR60	FP H. Total	5F	63	64
SR61	FP H. Panel Size	4F	4F	4F
SR62	FP H. Blank Start	50	50	4F
SR63	FP H. Blank End	02	06	07
SR64	FP H. Sync Start	52	53	52
SR65	FP H. Sync End	9E	98	9A
SR66	FP H. Overflow 1	00	00	00
SR67	Reserved	00	00	00
SR68	FP V. Total	0B	06	F2
SR69	FP V. Panel Size	DF	DF	DF
SR6A	FP V. Blank Start	E7	E7	DF
SR6B	FP V. Blank End	04	FF	F2
SR6C	FP V. Sync Start	E9	E8	E0
SR6D	FP V. Sync End	0B	0B	03
SR6E	FP V. Overflow 1	12	12	11
SR6F	FP V. Overflow 2	11	11	11

Programming Example: SVGA TFT (800 x 600)

Panel Type: SVGA				
Horizontal resolution	800	800	800	800
Vertical resolution	600	600	600	600
Dot Clock (MHz)	36.000	40.000	50.000	49.500
Horizontal freq (kHz)	35.1	37.9	48.1	46.9
Refresh rate (Hz)	56	60	72	75

Register Description		Register Value
SR30	Architecture Configuration	01 or 11
SR31	FP Display Mode	10 or D2
SR32	FP Pin Control	06 or F6
SR33	Reserved	00
SR34	FP AC Modulation	01
SR35	FP Miscellaneous Control	10
SR36	FP Dither Control	00, F0, A1, 59
SR37	FP Weight Decode Pointer	00
SR38	FP Weight Decode	00
SR39	FP Algorithm Control	00
SR3A	FP FRC Tuning 1	00
SR3B	FP FRC Tuning 2	00
SR3C	FP FRC Tuning 3	00
SR3D	FP Configuration	01, 00, 02
SR3E	Reserved	00
SR3F	Reserved	00
SR40	FP Pin Configuration	8x, Cx, Ex, 8x
SR41	FP Power Sequence Ctl	00 or 0C
SR42	FP Power Mngmt Ctl	91 or B3
SR43	FP Standby Ctl	01 or 41
SR44	FP Power Mngmt	01 or 10
SR45	FP PLL Power Mngmt	00, 01, 02, 03
SR46	FP Power Mngmt Status	read only
SR47	CLUT Control	00, 01, 02
SR48	Icon Mode	00
SR49	Icon Color Stack	00
SR4A	Icon X Position High	00
SR4B	Icon X Position Low	00
SR4C	Icon Y Position High	00
SR4D	Icon Y Position Low	00
SR4E	Icon Address	00
SR4F	STN Data Address	00

Register Description		Register Value			
SR50	STN FBSize Low	87			
SR51	STN FB Size High	2C			
SR52	PWM Control	20, 21			
SR53	PWM Duty Cycle	F7			
SR54	FP H. Compensation	1F			
SR55	FP H. Compensation Ctl	07			
SR56	FP V. Compensation	1F, 15			
SR57	FP V. Compensation Ctl	1F, 0F			
SR58	FP H. Border	read only			
SR59	FP H. Expansion Factor	read only			
SR5A	FP V. Border	read only			
SR5B	FP V. Expansion Factor	read only			
SR5C	FP Display Enable Position	77			
SR5D	FP Syncs Position	77			
SR5E	Reserved	00			
SR5F	Reserved	00			
SR60	FP H. Total	7B	7F	7D	7F
SR61	FP H. Panel Size	63	63	63	63
SR62	FP H. Blank Start	63	63	63	63
SR63	FP H. Blank End	1E	02	00	02
SR64	FP H. Sync Start	67	69	6B	66
SR65	FP H. Sync End	90	19	1A	10
SR66	FP H. Overflow 1	00	00	00	00
SR67	Reserved	00	00	00	00
SR68	FP V. Total	6F	72	98	6F
SR69	FP V. Panel Size	57	57	57	57
SR6A	FP V. Blank Start	57	57	57	57
SR6B	FP V. Blank End	6F	72	98	6F
SR6C	FP V. Sync Start	58	58	7C	58
SR6D	FP V. Sync End	0A	0C	02	0B
SR6E	FP V. Overflow 1	22	22	22	22
SR6F	FP V. Overflow 2	22	22	22	22

Programming Example: XGA TFT (1024 x 768)

Panel Type: XGA			
Horizontal resolution	1024	1024	1024
Vertical resolution	768	768	768
Dot Clock (MHz)	65.00	75.000	78.750
Horizontal freq (kHz)	48.4	57.5	60
Refresh rate (Hz)	60	70	75

Register Description		Register Value
SR30	Architecture Configuration	01 or 11
SR31	FP Display Mode	10 or D2
SR32	FP Pin Control	06 or F6
SR33	Reserved	00
SR34	FP AC Modulation	01
SR35	FP Miscellaneous Control	10
SR36	FP Dither Control	00, F0, A1, 59
SR37	FP Weight Decode Pointer	00
SR38	FP Weight Decode	00
SR39	FP Algorithm Control	00
SR3A	FP FRC Tuning 1	00
SR3B	FP FRC Tuning 2	00
SR3C	FP FRC Tuning 3	00
SR3D	FP Configuration	01, 00, 02
SR3E	Reserved	00
SR3F	Reserved	00
SR40	FP Pin Configuration	8x, Cx, Ex, 8x
SR41	FP Power Sequence Ctl	00 or 0C
SR42	FP Power Mngmt Ctl	91 or B3
SR43	FP Standby Ctl	01 or 41
SR44	FP Power Mngmt	01 or 10
SR45	FP PLL Power Mngmt	00, 01, 02, 03
SR46	FP Power Mngmt Status	read only
SR47	CLUT Control	00, 01, 02
SR48	Icon Mode	00
SR49	Icon Color Stack	00
SR4A	Icon X Position High	00
SR4B	Icon X Position Low	00
SR4C	Icon Y Position High	00
SR4D	Icon Y Position Low	00
SR4E	Icon Address	00
SR4F	STN Data Address	00

Register Description		Register Value		
SR50	STN FBSize Low	FF		
SR51	STN FB Size High	47		
SR52	PWM Control	20, 21		
SR53	PWM Duty Cycle	F7		
SR54	FP H. Compensation	1F, 15		
SR55	FP H. Compensation Ctl	0F, 07		
SR56	FP V. Compensation	1F, 15		
SR57	FP V. Compensation Ctl	3F, 1F, 0F		
SR58	FP H. Border	read only		
SR59	FP H. Expansion Factor	read only		
SR5A	FP V. Border	read only		
SR5B	FP V. Expansion Factor	read only		
SR5C	FP Display Enable Position	77		
SR5D	FP Syncs Position	77		
SR5E	Reserved	00		
SR5F	Reserved	00		
SR60	FP H. Total	A3	A1	9F
SR61	FP H. Panel Size	7F	7F	7F
SR62	FP H. Blank Start	7F	7F	7F
SR63	FP H. Blank End	06	04	02
SR64	FP H. Sync Start	83	83	82
SR65	FP H. Sync End	94	94	8E
SR66	FP H. Overflow 1	00	00	00
SR67	Reserved	00	00	00
SR68	FP V. Total	24	24	1E
SR69	FP V. Panel Size	FF	FF	FF
SR6A	FP V. Blank Start	FF	FF	FF
SR6B	FP V. Blank End	24	24	1E
SR6C	FP V. Sync Start	02	02	00
SR6D	FP V. Sync End	08	08	03
SR6E	FP V. Overflow 1	23	22	23
SR6F	FP V. Overflow 2	32	32	32

Appendix C: Panel Attachment Examples

Panel Hook-Up Diagram – Hitachi Color TFT 1024 x 768

Aurora64V+ 80 Pin IDS Connector J22 or J23	Signal Names	BGA Pin's #	DATA BIT DESCRIPTION	Hitachi Color TFT TX31D02VC1CAA 1024 x 768
				CN1(Molex)
3	FPDCLK	B3		DCLK (CN1-2)
6	FPHSYNC	C4		HSYNC (CN1-4)
8	FPVSYNC	A3		VSYNC (CN1-5)
64	FPVDE	B15		DTMG (CN1-61)
10	FPD0	B4	First Pixel Red Data	RA0 (CN1-7)
11	FPD1	A4		RA1 (CN1-8)
13	FPD2	C5		RA2 (CN1-10)
14	FPD3	B5		RA3 (CN1-11)
16	FPD4	A5		RA4 (CN1-13)
17	FPD5	D6		RA5 (CN1-14)
19	FPD6	C6	First Pixel Green Data	GA0 (CN1-16)
20	FPD7	B6		GA1 (CN1-17)
22	FPD8	A6		GA2 (CN1-19)
23	FPD9	C7		GA3 (CN1-20)
25	FPD10	B7		GA4 (CN1-22)
26	FPD11	A7		GA5 (CN1-23)
28	FPD12	D8	First Pixel Blue Data	BA0 (CN1-25)
29	FPD13	C8		BA1 (CN1-26)
31	FPD14	B8		BA2 (CN1-28)
32	FPD15	A8		BA3 (CN1-29)
34	FPD16	C9		BA4 (CN1-31)
35	FPD17	B9		BA5 (CN1-32)
37	FPD18	A9	Second Pixel Red Data	RB0 (CN1-34)
38	FPD19	C10		RB1 (CN1-20)
40	FPD20	B10		RB2 (CN1-37)
41	FPD21	A10		RB3 (CN1-38)
43	FPD22	C11		RB4 (CN1-40)
44	FPD23	B11		RB5 (CN1-41)
46	FPD24	A11	Second Pixel Green data	GB0 (CN1-43)
47	FPD25	D12		GB1 (CN1-44)
49	FPD26	C12		GB2 (CN1-46)
50	FPD27	B12		GB3 (CN1-47)
52	FPD28	A12		GB4 (CN1-49)
53	FPD29	C13		GB5 (CN1-50)
55	FPD30	B13	Second Pixel Blue Data	BB0 (CN1-52)
56	FPD31	A13		BB1 (CN1-53)
58	FPD32	D14		BB2 (CN1-55)
59	FPD33	C14		BB3 (CN1-56)
61	FPD34	B14		BB4 (CN1-58)
62	FPD35	A14		BB5 (CN1-59)
71, 73	VDD_LCD	n/a		VDD(3.3V) only
75	VDD_LCD	n/a		Pins 63, 64 and 65
74	FPPOL	C15		
77	VEE_LCD			n/a
2, 4, 5, 7	GND	n/a		VSS Pins are
9, 12, 15	GND	n/a		1, 3, 6, 9, 12, 15, 18
18, 21, 24	GND	n/a		21, 24, 27, 30, 33, 36,,
27, 30, 33	GND	n/a		39, 42, 45, 48, 51, 54,,
6, 39, 42	GND	n/a		57, 60, 66, 67, and 68
45, 48, 51	GND	n/a		
54, 57, 60	GND	n/a		
63, 65, 79	GND	n/a		

Panel Hook-Up Diagram – Sharp Color DSTN 640 x 480 16 Bit

AURORA64V+ 64 & 10 Pin Connector	Signal Name	BGA Pin	Sharp Color DSTN LM64C08P
Resolution			640X480
Interface			16 Bit
3	FPDCLK	B3	XCK (CN1-3)
6	FPHSYNC	C4	LP (CN1-2)
8	FPVSYNC	A3	YD (CN1-1)
64	FPVDE	B15	n/c
10	FPD0	B4	DL0 (CN2-17)
11	FPD1	A4	
13	FPD2	C5	DL1 (CN2-18)
14	FPD3	B5	
16	FPD4	A5	DL2 (CN2-19))
17	FPD5	D6	
19	FPD6	C6	DL3 (CN2-20))
20	FPD7	B6	
22	FPD8	A6	DL4 (CN2-21)
23	FPD9	C7	
25	FPD10	B7	DL5 (CN2-22)
26	FPD11	A7	
28	FPD12	D8	DL6 (CN2-23)
29	FPD13	C8	
31	FPD14	B8	DL7 (CN2-24)
32	FPD15	A8	
34	FPD16	C9	
35	FPD17	B9	
37	FPD18	A9	DU0 (CN1-8)
38	FPD19	C10	
40	FPD20	B10	DU1 (CN1-9)
41	FPD21	A10	
43	FPD22	C11	DU2 (CN1-10)
44	FPD23	B11	
46	FPD24	A11	DU3 (CN1-11)
47	FPD25	D12	
49	FPD26	C12	DU4 (CN1-12)
50	FPD27	B12	
52	FPD28	A12	DU5 (CN1-13)
53	FPD29	C13	
55	FPD30	B13	DU6 (CN1-14)
56	FPD31	A13	
58	FPD32	D14	DU7 (CN1-15)
59	FPD33	C14	
61	FPD34	B14	
62	FPD35	A14	
	(+1.8V Min)		Vcon(CN1–12)
71	VDD_LCD		(+5V)(CN1-5)
73, 75	VDD_LCD		On/Off(CN1-4)
77	VEE_LCD	Adjust with R43	Vee(+27V)CN1-7
2, 4, 5, 7, 9, 12, 15	GND	N/A	Vss (CN1-6)
18, 21, 24, 27, 30, 42	GND	N/A	Vss (CN2-16, 25)
27, 30, 33, 36, 39, 51	GND	N/A	
45, 48, 51, 54, 57, 60	GND	N/A	
63, 65, 79	GND	N/A	
J24(PIN 1)	(+12V)		To BKL inverter

Panel Hook-Up Diagram – Sharp Color DSTN 640 x 480 16 Bit

AURORA64V+ 64 & 10 Pin Connector	Signal Name	BGA Pin	Sharp Color DSTN LM64C15/35P
Resolution			640X480
Interface			16 Bit
3	FPDCLK	B3	XCK (CN1-10)
6	FPHSYNC	C4	LP (CN1-6)
8	FPVSYNC	A3	YD (CN1-4)
64	FPVDE	B15	n/c
10	FPD0	B4	DL0 (CN1-11)
11	FPD1	A4	
13	FPD2	C5	DL1 (CN1-13)
14	FPD3	B5	
16	FPD4	A5	DL2 (CN1-17)
17	FPD5	D6	
19	FPD6	C6	DL3 (CN1-19)
20	FPD7	B6	
22	FPD8	A6	DL4 (CN1-1)
23	FPD9	C7	
25	FPD10	B7	DL5 (CN1-3)
26	FPD11	A7	
28	FPD12	D8	DL6 (CN1-5)
29	FPD13	C8	
31	FPD14	B8	DL7 (CN1-7)
32	FPD15	A8	
34	FPD16	C9	
35	FPD17	B9	
37	FPD18	A9	DU0 (CN1-28)
38	FPD19	C10	
40	FPD20	B10	DU1 (CN1-26)
41	FPD21	A10	
43	FPD22	C11	DU2 (CN1-24)
44	FPD23	B11	
46	FPD24	A11	DU3 (CN1-22)
47	FPD25	D12	
49	FPD26	C12	DU4 (CN1-23)
50	FPD27	B12	
52	FPD28	A12	DU5 (CN1-25)
53	FPD29	C13	
55	FPD30	B13	DU6 (CN1-29)
56	FPD31	A13	
58	FPD32	D14	DU7 (CN1-31)
59	FPD33	C14	
61	FPD34	B14	
62	FPD35	A14	
	(+1.8V Min)		Vcon(CN1–12)
71	VDD_LCD		Vdd(CN1-14, 16)
73, 75	VDD_LCD		On/Off(CN1-18)
77	VEE_LCD	Adjust with R43	N/A
2, 4, 5, 7, 9, 12, 15	GND	N/A	Vss (CN1-2, 8, 9)
18, 21, 24, 27, 30, 42	GND	N/A	Vss(CN1-15, 21)
27, 30, 33, 36, 39, 51	GND	N/A	Vss(CN1-27, 30)
45, 48, 51, 54, 57, 60	GND	N/A	
63, 65, 79	GND	N/A	
J24(PIN 1)	(+12V)		To BKL inverter

Panel Hook-Up Diagram – Sharp Color DSTN 800 x 600 16 Bit

AURORA64V+ 64 & 10 Pin Connector	Signal Name	BGA Pin	Sharp Color DSTN LM80C03P
Resolution			800X600
Interface			16 Bit
3	FPDCLK	B3	XCK (CN1-10)
6	FPHSYNC	C4	LP (CN1-6)
8	FPVSYNC	A3	YD (CN1-4)
64	FPVDE	B15	n/c
10	FPD0	B4	DL0 (CN1-11)
11	FPD1	A4	
13	FPD2	C5	DL1 (CN1-13)
14	FPD3	B5	
16	FPD4	A5	DL2 (CN1-17)
17	FPD5	D6	
19	FPD6	C6	DL3 (CN1-19)
20	FPD7	B6	
22	FPD8	A6	DL4 (CN1-1)
23	FPD9	C7	
25	FPD10	B7	DL5 (CN1-3)
26	FPD11	A7	
28	FPD12	D8	DL6 (CN1-5)
29	FPD13	C8	
31	FPD14	B8	DL7 (CN1-7)
32	FPD15	A8	
34	FPD16	C9	
35	FPD17	B9	
37	FPD18	A9	DU0 (CN1-28)
38	FPD19	C10	
40	FPD20	B10	DU1 (CN1-26)
41	FPD21	A10	
43	FPD22	C11	DU2 (CN1-24)
44	FPD23	B11	
46	FPD24	A11	DU3 (CN1-22)
47	FPD25	D12	
49	FPD26	C12	DU4 (CN1-23)
50	FPD27	B12	
52	FPD28	A12	DU5 (CN1-25)
53	FPD29	C13	
55	FPD30	B13	DU6 (CN1-29)
56	FPD31	A13	
58	FPD32	D14	UD7 (CN1-31)
59	FPD33	C14	
61	FPD34	B14	
62	FPD35	A14	
	(+1.8V Min)		Vcon(CN1–12)
71	VDD_LCD		Vdd(CN1-14, 16)
73, 75	VDD_LCD		On/Off(CN1-18)
77	VEE_LCD	Adjust with R43	N/A
2, 4, 5, 7, 9, 12, 15	GND	N/A	Vss (CN1-2, 8, 9)
18, 21, 24, 27, 30, 42	GND	N/A	Vss(CN1-15, 21)
27, 30, 33, 36, 39, 51	GND	N/A	Vss(CN1-27, 30)
45, 48, 51, 54, 57, 60	GND	N/A	
63, 65, 79	GND	N/A	
J24(PIN 1)	(+12V)		To BKL inverter

Panel Hook-Up Diagram – Hitachi Color STN 640 x 480 16 Bit

Aurora64V+ 64 & 10 Pin IDC Connector	Signal's Names	BGA Pin's #	Hitachi Color STN LMG9460ZUCC 640 x 480(16 Bit)
J22 or J23			CN1(Hirose)
3	FPDCLK	B3	CL2 (CN1-10)
6	FPHSYNC	C4	CL1 (CN1-6)
8	FPVSYNC	A3	FLM (CN1-4)
64	FPVDE	B15	n/a
10	FPD0	B4	LD0 (CN1-11)
11	FPD1	A4	
13	FPD2	C5	LD1 (CN1-13)
14	FPD3	B5	
16	FPD4	A5	LD2 (CN1-17)
17	FPD5	D6	
19	FPD6	C6	LD3 (CN1-19)
20	FPD7	B6	
22	FPD8	A6	LD4 (CN1-1)
23	FPD9	C7	
25	FPD10	B7	LD5 (CN1-3)
26	FPD11	A7	
28	FPD12	D8	LD6 (CN1-5)
29	FPD13	C8	
31	FPD14	B8	LD7 (CN1-7)
32	FPD15	A8	
34	FPD16	C9	
35	FPD17	B9	
37	FPD18	A9	UD0 (CN1-28)
38	FPD19	C10	
40	FPD20	B10	UD1 (CN1-26)
41	FPD21	A10	
43	FPD22	C11	UD2 (CN1-24)
44	FPD23	B11	
46	FPD24	A11	UD3 (CN1-22)
47	FPD25	D12	
49	FPD26	C12	UD4 (CN1-23)
50	FPD27	B12	
52	FPD28	A12	UD5 (CN1-25)
53	FPD29	C13	
55	FPD30	B13	UD6 (CN1-29)
56	FPD31	A13	
58	FPD32	D14	UD7 (CN1-31)
59	FPD33	C14	
61	FPD34	B14	
62	FPD35	A14	
71, 73	VDD_LCD	n/a	Disp off Pin 18
73, 75	VDD_LCD	n/a	VDD Pin 14, 16
74	FPPOL	C15	n/a
			VCON Pin 12
77	VEE_LCD		n/a
2, 4, 5, 7	GND	n/a	GNDS Pins
9, 12, 15	GND	n/a	2, 8, 9, 15
18, 21, 24	GND	n/a	21, 27 and 30
27, 30, 33	GND	n/a	
36, 39, 42	GND	n/a	
45, 48, 51	GND	n/a	
54, 57, 60, 79	GND	n/a	

Panel Hook-Up Diagram – Hitachi Color STN 800 x 600 16 Bit

Aurora64V+ 64 & 10 Pin IDC Connector	Signal's Names	BGA Pin's #	Hitachi Color STN LMG9900ZWCC 800 x 600 (16 Bit)
J22 or J23			CN1(Hirose)
3	FPDCLK	B3	CL2 (CN1-10)
6	FPHSYNC	C4	CL1 (CN1-6)
8	FPVSYNC	A3	FLM (CN1-4)
64	FPVDE	B15	n/a
10	FPD0	B4	LD0 (CN1-11)
11	FPD1	A4	
13	FPD2	C5	LD1 (CN1-13)
14	FPD3	B5	
16	FPD4	A5	LD2 (CN1-17)
17	FPD5	D6	
19	FPD6	C6	LD3 (CN1-19)
20	FPD7	B6	
22	FPD8	A6	LD4 (CN1-1)
23	FPD9	C7	
25	FPD10	B7	LD5 (CN1-3)
26	FPD11	A7	
28	FPD12	D8	LD6 (CN1-5)
29	FPD13	C8	
31	FPD14	B8	LD7 (CN1-7)
32	FPD15	A8	
34	FPD16	C9	
35	FPD17	B9	
37	FPD18	A9	UD0 (CN1-28)
38	FPD19	C10	
40	FPD20	B10	UD1 (CN1-26)
41	FPD21	A10	
43	FPD22	C11	UD2 (CN1-24)
44	FPD23	B11	
46	FPD24	A11	UD3 (CN1-22)
47	FPD25	D12	
49	FPD26	C12	UD4 (CN1-23)
50	FPD27	B12	
52	FPD28	A12	UD5 (CN1-25)
53	FPD29	C13	
55	FPD30	B13	UD6 (CN1-29)
56	FPD31	A13	
58	FPD32	D14	UD7 (CN1-31)
59	FPD33	C14	
61	FPD34	B14	
62	FPD35	A14	
71, 73	VDD_LCD	n/a	Disp off Pin 18
73, 75	VDD_LCD	n/a	VDD Pin 14, 16
74	FPPOL	C15	n/a
			VCON Pin 12
77	VEE_LCD		n/a
2, 4, 5, 7	GND	n/a	GNDS Pins
9, 12, 15	GND	n/a	2, 8, 9, 15
18, 21, 24	GND	n/a	21, 27 and 30
27, 30, 33	GND	n/a	
36, 39, 42	GND	n/a	
45, 48, 51	GND	n/a	
54, 57, 60, 79	GND	n/a	

Panel Hook-Up Diagram – Hitachi Color STN 800 x 600 16 Bit

Aurora64V+ 64 & 10 Pin IDC Connector	Signal's Names	BGA Pin's #	Hitachi Color STN LMG9960ZWCC 800 x 600 (16 Bit)
J22 or J23			CN1(Hirose)
3	FPDCLK	B3	CL2 (CN1-10)
6	FPHSYNC	C4	CL1 (CN1-6)
8	FPVSYNC	A3	FLM (CN1-4)
64	FPVDE	B15	n/a
10	FPD0	B4	LD0 (CN1-11)
11	FPD1	A4	
13	FPD2	C5	LD1 (CN1-13)
14	FPD3	B5	
16	FPD4	A5	LD2 (CN1-17)
17	FPD5	D6	
19	FPD6	C6	LD3 (CN1-19)
20	FPD7	B6	
22	FPD8	A6	LD4 (CN1-1)
23	FPD9	C7	
25	FPD10	B7	LD5 (CN1-3)
26	FPD11	A7	
28	FPD12	D8	LD6 (CN1-5)
29	FPD13	C8	
31	FPD14	B8	LD7 (CN1-7)
32	FPD15	A8	
34	FPD16	C9	
35	FPD17	B9	
37	FPD18	A9	UD0 (CN1-28)
38	FPD19	C10	
40	FPD20	B10	UD1 (CN1-26)
41	FPD21	A10	
43	FPD22	C11	UD2 (CN1-24)
44	FPD23	B11	
46	FPD24	A11	UD3 (CN1-22)
47	FPD25	D12	
49	FPD26	C12	UD4 (CN1-23)
50	FPD27	B12	
52	FPD28	A12	UD5 (CN1-25)
53	FPD29	C13	
55	FPD30	B13	UD6 (CN1-29)
56	FPD31	A13	
58	FPD32	D14	UD7 (CN1-31)
59	FPD33	C14	
61	FPD34	B14	
62	FPD35	A14	
71, 73	VDD_LCD	n/a	Disp off Pin 18
73, 75	VDD_LCD	n/a	VDD Pin 14, 16
74	FPPOL	C15	n/a
			VCON Pin 12
77	VEE_LCD		n/a
2, 4, 5, 7	GND	n/a	GNDS Pins
9, 12, 15	GND	n/a	2, 8, 9, 15
18, 21, 24	GND	n/a	21, 27 and 30
27, 30, 33	GND	n/a	
36, 39, 42	GND	n/a	
45, 48, 51	GND	n/a	
54, 57, 60, 79	GND	n/a	

Panel Hook-Up Diagram – Toshiba Color TFT 800 x 600 18 Bit

Aurora64V+ (M65)			Toshiba color TFT
64 & 10 Pin IDC Connector	Signal Name	BGA Pin	NL8060AC24-01
			800X600 (18 Bit)
3	FPDCLK	B3	NCLK (CN1-p1)
6	FPHSYNC	C4	n/a
8	FPVSYNC	A3	n/a
64	FPVDE	B15	ENAB (CN2-p8)
10	FPD0	B4	R0 (CN1-p3)
11	FPD1	A4	
13	FPD2	C5	R1 (CN1-p4)
14	FPD3	B5	
16	FPD4	A5	R2 (CN1-p5)
17	FPD5	D6	
19	FPD6	C6	R3 (CN1-p6)
20	FPD7	B6	
22	FPD8	A6	R4 (CN1-p7)
23	FPD9	C7	
25	FPD10	B7	R5 (CN1-p8)
26	FPD11	A7	
28	FPD12	D8	G0 (CN1-p10)
29	FPD13	C8	
31	FPD14	B8	G1 (CN1-p11)
32	FPD15	A8	
34	FPD16	C9	G2 (CN1-p12)
35	FPD17	B9	
37	FPD18	A9	G3 (CN1-p13)
38	FPD19	C10	
40	FPD20	B10	G4 (CN1-p14)
41	FPD21	A10	
43	FPD22	C11	G5 (CN1-p15)
44	FPD23	B11	
46	FPD24	A11	B0 (CN2-p2)
47	FPD25	D12	
49	FPD26	C12	B1 (CN2-p3)
50	FPD27	B12	
52	FPD28	A12	B2 (CN2-p4)
53	FPD29	C13	
55	FPD30	B13	B3 (CN2-p5)
56	FPD31	A13	
58	FPD32	D14	B2 (CN2-p6)
59	FPD33	C14	
61	FPD34	B14	B3 (CN2-p7)
62	FPD35	A14	
71	VDD_LCD	N/A	VDD(CN2-p9)
73, 75	VDD_LCD	N/A	VDD(CN2-p10)
77	VEE_LCD		N/A
2, 4, 5, 7, 9, 12, 15	GND	N/A	GND (CN1-p2, 9)
18, 21, 24, 27, 30	GND	N/A	GND (CN2-p1)
33, 36, 39, 42	GND	N/A	
45, 48, 51, 54, 57	GND	N/A	
60, 79	GND	N/A	

Panel Hook-Up Diagram – Hitachi Color TFT 800 x 600

Aurora64V+			Hitachi (8x6 TFT) TX26D81VC1CAA-1	
64 & 10 Pin IDC Connector	Signal Name	BGA Pin Number	CN1 40 Pin (Hirose)	Signal Description
3	FPDCLK	B3	2	DCLK
6	FPHSYNC	C4	4	HSYNC
8	FPVSYNC	A3	5	VSYNC
64	FPVDE	B15	37	DTMG
10	FPD0	B4	9	R0
11	FPD1	A4		
13	FPD2	C5	10	R1
14	FPD3	B5		
16	FPD4	A5	11	R2
17	FPD5	D6		
19	FPD6	C6	13	R3
20	FPD7	B6		
22	FPD8	A6	14	R4
23	FPD9	C7		
25	FPD10	B7	15	R5
26	FPD11	A7		
28	FPD12	D8	19	G0
29	FPD13	C8		
31	FPD14	B8	20	G1
32	FPD15	A8		
34	FPD16	C9	21	G2
35	FPD17	B9		
37	FPD18	A9	23	G3
38	FPD19	C10		
40	FPD20	B10	24	G4
41	FPD21	A10		
43	FPD22	C11	25	G5
44	FPD23	B11		
46	FPD24	A11	29	B0
47	FPD25	D12		
49	FPD26	C12	30	B1
50	FPD27	B12		
52	FPD28	A12	31	B2
53	FPD29	C13		
55	FPD30	B13	33	B3
56	FPD31	A13		
58	FPD32	D14	34	B4
59	FPD33	C14		
35	FPD34	B14	35	B5
62	FPD35	A14		
71	VDD_LCD	N/A	39	VDD (+5V)
73, 75	VDD_LCD	N/A	40	VDD (+5V)
74	FPPOL	C15	N/A	
77	VEE_LCD		N/A	N/A
2, 4, 5, 7	GND	N/A	1, 3, 6, 7, 8	VSS
9, 12, 15	GND	N/A	12, 16, 17, 18	VSS
8, 21, 24	GND	N/A	22, 26, 27, 28	VSS
27, 30, 33	GND	N/A	32, 36	VSS
36, 39, 42	GND	N/A		
45, 48, 51	GND	N/A		
54, 57, 60, 79	GND	N/A		

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FP Registers for TFT Panels		
Reg	**Panel Size**	
	Parameters/registers	
	Horizontal resolution	
	Vertical resolution	
	Dot Clock (MHz)	
	Horizontal freq (kHz)	
	Refresh rate (Hz)	
SR30		
SR31		
SR32		
SR33		
SR34		
SR35		
SR36		
SR37		
SR37		
SR38		
SR39		
SR3A		
SR3B		
SR3C		
SR3D		
SR3E		
SR3F		
SR40		
SR41		
SR42		
SR43		
SR44		
SR45		
SR46		
SR47		
SR48		
SR49		
SR4A		
SR4B		
SR4C		
SR4D		
SR4E		
SR4F		
SR50		
SR51		
SR52		
SR53		
SR54		
SR55		
SR56		
SR57		
SR58		

SR59		
SR5A		
SR5B		
SR5C		
SR5D		
SR5E		
SR5F		
SR60		
SR61		
SR62		
SR63		
SR64		
SR65		
SR66		
SR67		
SR68		
SR69		
SR6A		
SR6B		
SR6C		
SR6D		
SR6E		
SR6F		

S3 Incorporated

86CM65 Dual Display Accelerator

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