LH77790A/B
Embedded Microcontroller

Thermal & Electrical Specification

Version 1.0

SHARP

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Preliminary LH77790A/B Thermal & Electrical Specification (Version 1.0)
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THERMAL & ELECTRICAL SPECIFICATION

OVERVIEW

Portable devices are becoming more and more prevalent in our daily life. They are used as personal information managers, communication devices, digital cameras, handheld games, bar-code scanners, medical equipment, electronic instrumentation, and navigation systems. There are significant design challenges for portable devices. Low cost is a top priority for high volume products. Low power is a must for long battery life. High performance is critical for computationally-intensive applications such as PDAs, GPS, and 2-D scanners. Communication capabilities and effective user interface are integral parts of any portable device. Last, but not least, superior product development support tools are crucial to reducing time-to-market.

The SYSTEM ON CHIP Team at Sharp has designed the LH77790A/B Embedded Microcontroller (a.k.a. 790A/B) to meet the above challenges in portable design. The LH77790A/B, powered by an ARM7DI™, is a complete system on chip with a high level of integration to satisfy a wide range of customer requirements and expectations.

The 790A/B combines a 32-bit ARM7DI RISC engine, a number of essential peripherals (UARTs, Counter/Timers, PIOs, PWMs, etc...), LCD controller, cache, and on-chip SRAM. This high level of integration lowers overall system cost, reduces development cycle time and accelerates product introduction. The 790A/B's fully static design, power management unit, dual voltage operation (3.3 V/5 V), fast interrupt response time, on-chip cache and SRAM, powerful instruction set, and very low power RISC core provide high performance at low current draw. The on-chip LCD controller, UARTs, IrDA/DASK, and the programmable peripheral interface (PPI) are well suited for wireless, cable, and visual communication requirements. Other features like, watchdog timer, programmable memory interface, on-chip SRAM/DRAM controllers and debug support provides a high level of flexibility.

Please check our website at www.sharpsma.com or with your local SHARP sales office for the latest Thermal and Electrical Specifications and/or errata sheets. These documents will contain the latest parameters for the LH77790A/B.

FEATURES

- Highly Integrated Single Chip
- 32-Bit ARM7DI RISC Core
  - Built-In Debug and ICE Support
  - Fast Interrupt Response
  - Powerful Instruction Set
- 26-bit External Address Bus
  - 512MB Addressable Space
- 16-bit External Data Bus
- 2KB Data/Instruction Cache
  - 4 Way Set Associative
  - Write Back Policy
  - Flexible Modes of Operation
- 2KB Static RAM
  - Expandable to 4KB Without Cache
- Low Power
- High Performance
- Programmable Clock and Power Management
- Programmable Monochrome LCD Controller
  - 1024 (V) x 2048 (H)
  - Four Gray Shades
  - Frame buffer in Main Memory
- On-Chip Interrupt Controller
  - Six External Interrupts
  - Seven Internal Interrupts
  - ARM7DI Wake-Up
- Three UARTs - 16C450-class
  - Full Modem Support on UART0
  - Partial Modem Support on UART1
  - IrDA-1.0/DASK Support on UART2
- IrDA/DASK IR Interface
  - IrDA-1.0 (2.4 kbps to 115.2 kbps)
  - DASK (2.4 kbps to 57.6 kbps)
- Three Pulse Width Modulator Channels
  - PWM0 and PWM1 have 8-Bit Resolution
  - PWM2 has 16-Bit Resolution
- Flexible Memory Interface
  - Six Multiplexeled Chip Enables/ CAS pins
  - Two RAS pins
  - Fully Programmable
  - Six SRAM Banks (64MB each)
  - Two DRAM Banks (128MB each)
  - User/System Access Privileges
- On-Chip DRAM Controller
  - Fast Page Mode
  - Normal Mode
  - CAS before RAS Refresh
- Programmable Peripheral Interface (PPI)
  - 24 Programmable I/O Signals
  - Three Modes of Operation
- Three 16-Bit Counter/Timer Channels
  - Six Modes of Operation
  - Binary or BCD Counting
- Hardware Watchdog Timer
  - Eight Time-out Intervals
  - Protection Mechanism
  - Three Time-out Actions
- Little Endian
- JTAG Interface
- Dual Supply Voltage
  - 5 V TTL - 25 MHz
  - 3.3 V LVTTL - 16.7 MHz

DEVELOPMENT ENVIRONMENT

The 790A/B Evaluation Board (part number LU7790H2A) and the ARM Software Development ToolKit (part number LU7V211H1) give users full access to the power and features of the 790A/B and provide a complete integrated environment for development. Users will be able to develop, benchmark, and profile both hardware and software easily and quickly.

BLOCK DIAGRAM

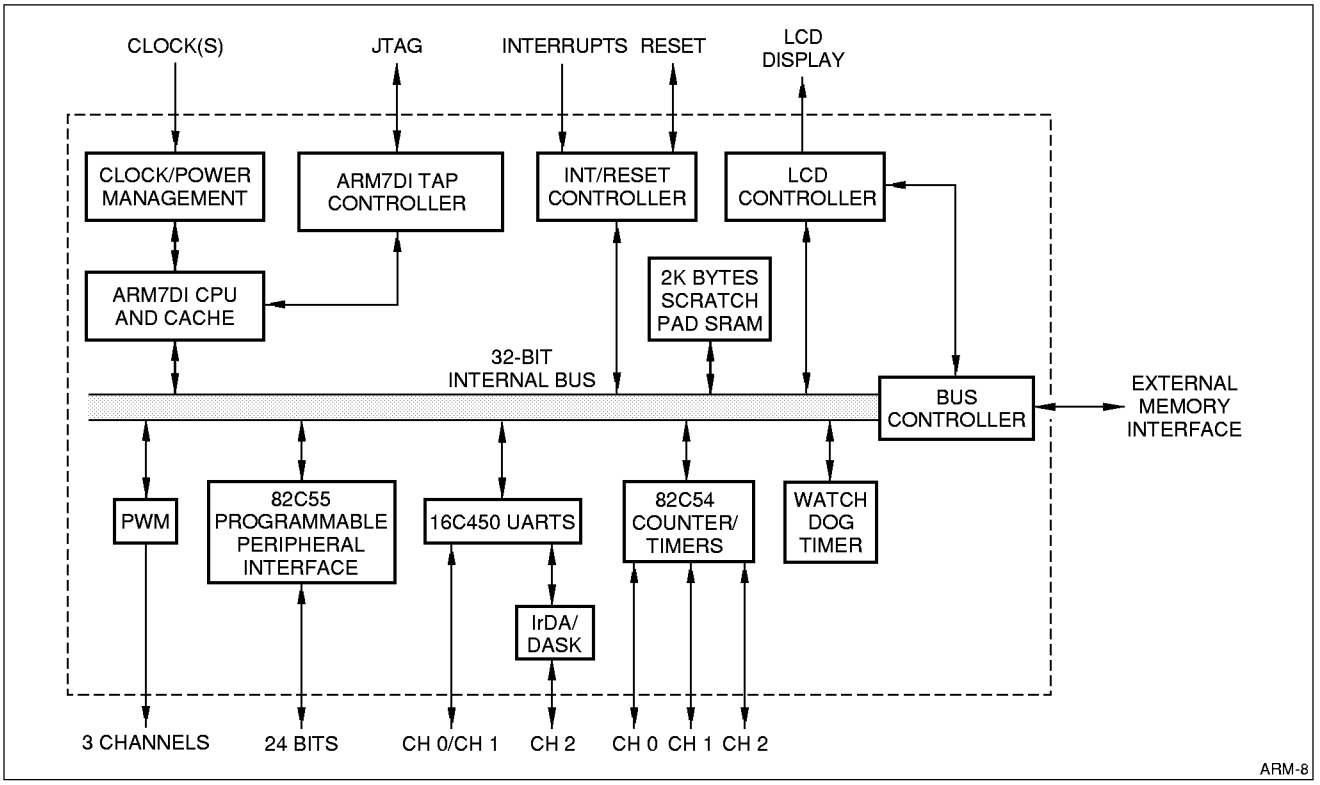

Figure 1-1. LH77790A/B Block Diagram

PIN DESCRIPTION

Table 2-1.
Pin Description

PIN(S)	NAME	DIRECTION	DESCRIPTION
EXTERNAL BUS INTERFACE			
36 - 31, 28 - 21, 18 - 11, 8 - 5	A[25:0]	O	External Address bus. The 790A/B will provide a 26-bit address to external memories and peripherals.
60 - 55, 52 - 47, 42 - 41, 38 - 37	D[15:0]	I/O	External 16-Bit data bus.
72	$\overline{OE}$	O	Output Enable for external memory and peripherals. $\overline{OE}$ allows external memory and peripherals to drive the data bus and is asserted LOW during a read access and HIGH during a write access.
71	$\overline{WE}$	O	Write Enable for external memory and peripherals. During a write access, this pin is driven LOW. During a read access, this pin is driven HIGH.
70 - 65	$\overline{CE}$ [5:0]/ $\overline{CAS}$ [5:0]	O	These pins provide the Chip Enable/Column Address Select signals allowing direct connection to standard external memory/peripheral devices. The pins act as $\overline{CAS}$ when interfacing to DRAMs and as $\overline{CE}$ otherwise. They are fully programmable by the system designer and can support byte enables.
62 - 61	$\overline{RAS}$ [1:0]	O	Row Address Select pins for DRAM Bank 0 and Bank 1.
74	$\overline{WAIT}$	I	External Memory Wait. Allows the use of slow memories. The 790A/B generates external $\overline{WAIT}$ cycles (EWC) in response to activating $\overline{WAIT}$. $\overline{WAIT}$ is sampled on the HIGH to LOW transition on XCLK. To add one EWC, $\overline{WAIT}$ must be active prior to sampling in the last cycle (beginning of the last cycle) of a memory transfer. If $\overline{WAIT}$ continues to be active (when sampled) in subsequent cycles, more EWC will be added. Once $\overline{WAIT}$ is deactivated, the 790A/B will complete the memory transfer.
73	$\overline{BW}$	O	Byte Wide Access. $\overline{BW}$ is LOW when the ARM7DI executes a store/load byte instruction. $\overline{BW}$ is HIGH when the ARM7DI Core executes a store/load word instruction or an instruction fetch. $\overline{BW}$ does not depend on the bus size of the external memory/peripheral device. $\overline{BW}$ is valid during an external memory access. It can be used by an external address decoder to generate extra chip/byte enables. $\overline{BW}$ is a don't care during DRAM refresh.
169	$\overline{BB}$	I	Byte Boot selects between x8 or x16 for the boot memory. The 790A/B samples and captures the state of $\overline{BB}$ on the rising edge of $\overline{RESETI}$ allowing $\overline{BB}$ to change state after Reset. If $\overline{BB}$ is LOW the 790A/B will boot from a x8 memory. If $\overline{BB}$ is HIGH, the 790A/B will boot from a x16 memory. This pin is normally tied LOW for x8 boot memory or HIGH for x16 boot memory.
COUNTERS/TIMERS INTERFACE			
123, 121, 117	CTGATE[2:0]	I	Counter/Timer control gate input signals.
124, 122, 118	CTOUT[2:0]	O	Counter/Timer output signals.
INTERRUPT INTERFACE			
107 - 102	INT[5:0]	I	External interrupt input signals.

Table 2-1.
Pin Description (cont'd)

PIN(S)	NAME	DIRECTION	DESCRIPTION
LCD CONTROLLER INTERFACE			
91	CP2	O	Shift/Pixel Clock.
92	CP1	O	Line Pulse/HSYNC.
93	MCLK	O	AC Modulation Signal.
94	S	O	Frame Pulse/VSYNC.
95	LCDCNTL	O	LCD Control Signal.
84 - 77	VD[7:0]	O	Video Data.
PROGRAMMABLE PERIPHERAL INTERFACE			
139 - 135, 128 - 126 149 - 145, 142 - 140 159 - 155, 152 - 150	PA[7:0] PB[7:0] PC[7:0]	I/O	Parallel ports A, B, and C signals. Signals have programmable access and can function as Input, Output or Controls (port C only). PB[7:2] and PC[2:0] are multiplexed with UART's modem signals
PWM INTERFACE			
98 - 96	PWM[2:0]	O	Pulse Width Modulator output signals.
UARTS INTERFACE			
114, 112, 108	RxD[2:0]	I	UART serial data input signals. RxD2 also doubles as the digital input for the IR interface.
115, 113, 111	TxD[2:0]	O	UART serial data output signals. TxD2 also doubles as the digital output for the IR interface.
150, 151	$\overline{\text{RTS}}$ [1:0]	O	Request To Send for UART0 and UART1. Multiplexed with PC0 and PC1 respectively.
145, 146	$\overline{\text{CTS}}$ [1:0]	I	Clear To Send for UART0 and UART1. Multiplexed with PB3 and PB4 respectively.
142, 147	$\overline{\text{RI}}$ [1:0]	I	Ring Indicator for UART0 and UART1. Multiplexed with PB2 and PB5 respectively.
152	$\overline{\text{DTR0}}$	O	Data Terminal Ready for UART0 only. Multiplexed with PC2.
149	$\overline{\text{DSR0}}$	I	Data Set Ready for UART0 only. Multiplexed with PB7.
148	$\overline{\text{DCD0}}$	I	Data Carrier Detect for UART0 only. Multiplexed with PB6.
RESET AND EXTERNAL CLOCKS			
101	$\overline{\text{RESETI}}$ **	I	Chip and JTAG TAP Controller Reset Input. $\overline{\text{RESETI}}$ has a built-in glitch detector. $\overline{\text{RESET0}}$ will be driven LOW after a valid reset is detected for as long as $\overline{\text{RESETI}}$ is driven LOW. JTAG reset, $\overline{\text{TRST}}$, is internally connected to $\overline{\text{RESETI}}$.
119	$\overline{\text{RESET0}}$	O	Chip Reset Output. It will be driven LOW during: (1) Chip Reset (2) WDT Timeout Reset (3) Software Controlled Reset
3	XCLK	I	The 790A/B External Clock Input pin. Duty cycle is 50%.

NOTE: **JTAG Reset, $\overline{\text{TRST}}$, is internally connected to $\overline{\text{RESETI}}$. IEEE 1149.1 – 1990 Standard requires JTAG inputs to be pulled up to a good logic level to achieve normal operations.

Table 2-1.
Pin Description (cont'd)

PIN(S)	NAME	DIRECTION	DESCRIPTION
RESET AND EXTERNAL CLOCKS (CONT'D)			
162	XCLKDIS	O	XCLKDIS is an active HIGH output pin that can be used to disable external clock circuitry and will result in reducing current consumption to micro-amperes. XCLKDIS is HIGH in Sleep and Stop modes. Connecting this pin to the external clock circuitry, allows the 790A/B to go into Stop mode by disabling the external clock.
116	UCLK	I	UART/DASK Demodulator External clock input signal. Duty cycle is 50%.
125	CTCLK	I	Counter/Timer External clock input signal. Duty cycle is 50%.
JTAG INTERFACE**			
160	TCK	I	JTAG Test/EmbeddedICE™ clock input signal. Must be pulled-up for normal operation (56 kΩ is recommended for compatibility with ARM's EmbeddedICE)
161	TMS	I	JTAG Test/EmbeddedICE mode select input signal. Must be pulled-up for normal operation (56 kΩ is recommended for compatibility with ARM's EmbeddedICE)
165	TDI	I	JTAG Test/EmbeddedICE data input signal. Must be pulled-up for normal operation (56 kΩ is recommended for compatibility with ARM's EmbeddedICE)
166	TDO	O	JTAG Test/EmbeddedICE data output signal.
RESERVED INTERFACE			
170	ADBE	I	Reserved. Must be tied HIGH for normal operation.
167	TEST0	I	Reserved. Must be tied LOW for normal operation.
168	TEST1	O	Reserved. No connect.
171	TEST2	I	Reserved. Must be tied LOW for normal operation
172	TEST3	O	Reserved. No connect.
POWER SIGNALS			
9, 19, 29, 39, 53, 63, 75, 85, 99, 109, 129, 143, 153, 163, 173	V_{CC}	I	Power. All LH77790A/B are 5 V/ 3.3 V.
4, 10, 20, 30, 40, 54, 64, 76, 86, 100, 110, 120, 130, 144, 154, 164, 174	V_{SS}	I	Ground. All ground pins must be used.
NO CONNECT			
1, 2, 43, 44, 45, 46, 87, 88, 89, 90, 131, 132, 133, 134, 175, 176	NC	—	No Connects.

NOTE: **JTAG Reset, $\overline{\text{TRST}}$, is internally connected to $\overline{\text{RESETI}}$. IEEE 1149.1 – 1990 Standard requires JTAG inputs to be pulled up to a good logic level to achieve normal operations.

Table 2-2.
Pinout

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	NC	45	NC	89	NC	133	NC
2	NC	46	NC	90	NC	134	NC
3	XCLK	47	D4	91	CP2	135	PA3
4	V_{SS}	48	D5	92	CP1	136	PA4
5	A0	49	D6	93	MCLK	137	PA5
6	A1	50	D7	94	S	138	PA6
7	A2	51	D8	95	LCDCNTL	139	PA7
8	A3	52	D9	96	PWM0	140	PB0
9	V_{CC}	53	VCC	97	PWM1	141	PB1
10	V_{SS}	54	VSS	98	PWM2	142	PB2/$\overline{RI1}$
11	A4	55	D10	99	V_{CC}	143	V_{CC}
12	A5	56	D11	100	V_{SS}	144	V_{SS}
13	A6	57	D12	101	$\overline{RESETI}$	145	PB3/$\overline{CTS1}$
14	A7	58	D13	102	INT0	146	PB4/$\overline{CTS0}$
15	A8	59	D14	103	INT1	147	PB5/$\overline{RI0}$
16	A9	60	D15	104	INT2	148	PB6/$\overline{DCD0}$
17	A10	61	$\overline{RAS0}$	105	INT3	149	PB7/$\overline{DSR0}$
18	A11	62	$\overline{RAS1}$	106	INT4	150	PC0/$\overline{RTS1}$
19	V_{CC}	63	V_{CC}	107	INT5	151	PC1/$\overline{RTS0}$
20	V_{SS}	64	V_{SS}	108	RxD0	152	PC2/$\overline{DTR0}$
21	A12	65	$\overline{CE0/CAS0}$	109	V_{CC}	153	V_{CC}
22	A13	66	$\overline{CE1/CAS1}$	110	V_{SS}	154	V_{SS}
23	A14	67	$\overline{CE2/CAS2}$	111	TxD0	155	PC3
24	A15	68	$\overline{CE3/CAS3}$	112	RxD1	156	PC4
25	A16	69	$\overline{CE4/CAS4}$	113	TxD1	157	PC5
26	A17	70	$\overline{CE5/CAS5}$	114	RxD2	158	PC6
27	A18	71	$\overline{WE}$	115	TxD2	159	PC7
28	A19	72	$\overline{OE}$	116	UCLK	160	TCK
29	V_{CC}	73	$\overline{BW}$	117	CTGATE0	161	TMS
30	V_{SS}	74	$\overline{WAIT}$	118	CTOUT0	162	XCLKDIS
31	A20	75	V_{CC}	119	$\overline{RESETO}$	163	V_{CC}
32	A21	76	V_{SS}	120	V_{SS}	164	V_{SS}
33	A22	77	VD0	121	CTGATE1	165	TDI
34	A23	78	VD1	122	CTOUT1	166	TDO
35	A24	79	VD2	123	CTGATE2	167	TEST0
36	A25	80	VD3	124	CTOUT2	168	TEST1
37	D0	81	VD4	125	CTCLK	169	$\overline{BB}$
38	D1	82	VD5	126	PA0	170	ADBE
39	V_{CC}	83	VD6	127	PA1	171	TEST2
40	V_{SS}	84	VD7	128	PA2	172	TEST3
41	D2	85	V_{CC}	129	V_{CC}	173	V_{CC}
42	D3	86	V_{SS}	130	V_{SS}	174	V_{SS}
43	NC	87	NC	131	NC	175	NC
44	NC	88	NC	132	NC	176	NC

ABSOLUTE MAXIMUM RATINGS

Table 3.
Absolute Maximum Ratings

PARAMETER	SYMBOL	ABSOLUTE MAXIMUM RATING	UNIT
Supply Voltage	V_{CC}	-0.3 to 6.0	V
Input Voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output Voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Storage Temperature	T_{STG}	-40 to +125	°C
Power Dissipation (Package Limit)	PD_{PKG}	1	W

NOTE: These are stress ratings for transient conditions only. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the device.

RECOMMENDED OPERATING CONDITIONS

Table 4.
LH77790A/B (5 V Operation) Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Supply Voltage	V_{SS}	0	0	0	V
Clock Frequency	F_{XCLK}	0	—	25	MHz
Operating Temperature	T_{OPR}	0	—	70	°C

NOTE: Unused input pins should be pulled low or high to their inactive state.

Table 5.
LH77790A/B (3.3 V Operation) Recommended Operating Conditions

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V
Clock Frequency	F_{XCLK}	0	—	16.7	MHz
Operating Temperature	T_{OPR}	0	—	70	°C

NOTE: Unused input pins should be pulled low or high to their inactive state.

DC SPECIFICATIONS

(Over Recommended Operating Voltage & Temperature Conditions)

Table 6.
LH77790A/B (5 V Range) DC Specifications

PARAMETER	SYMBOL	TEST CONDITION[3]	MIN.	MAX.	UNIT
Input Low Voltage[1]	V_{IL}		0	0.8	V
Input High Voltage[1]	V_{IH}		2.0	V_{CC}	V
Input Low Voltage[2]	V_{IL}		0	0.2	V
Input High Voltage[2]	V_{IH}		V_{CC} - 0.2	V_{CC}	V
Output Low Voltage[1]	V_{OL}	I_{OL} = 2 mA, V_{CC} = 4.5 V	—	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = -2 mA, V_{CC} = 4.5 V	2.4	—	V
Output Low Voltage[2]	V_{OL}	I_{OL} = 200 µA, V_{CC} = 4.5 V	—	0.2	V
Output High Voltage[2]	V_{OH}	I_{OH} = -200 µA, V_{CC} = 4.5 V	V_{CC} - 0.2	—	V
Input Leakage Current	I_{LI}	V_{IN} = 0 V to V_{CCMAX}	-5	5	µA
High Impedance (OFF-State) Output Leakage Current	I_{OZ}	V_{IN} = 0 V to V_{CCMAX}	-5	5	µA
Operating Current (Active Mode)	I_{CCAT}	Condition 1	—	115	mA
Operating Current (Standby Mode)	I_{CCSB}	Condition 2	—	4	mA
Operating Current (Sleep Mode)	I_{CCSL}	Condition 3	—	2	mA
Operating Current (Stop Mode)	I_{CCST}	Condition 4	—	80	µA

NOTES:

1. TTL
2. CMOS
3. Condition 1 (Active Mode):
   - CMOS Input levels (Note 2)
   - Recommended Operating Conditions (Table 4)
   - XCLK Frequency = 25 MHz

   Condition 2 (Standby Mode):
   - Same as Condition 1 with Core and Peripherals halted. DRAM Refresh is active.

   Condition 3 (Sleep Mode):
   - Same as Condition 2 with DRAM Refresh disabled.

   Condition 4 (Stop Mode):
   - Same as Condition 3 with XCLK stopped.

Table 7.
LH77790A/B (3.3 V Range) DC Specifications

PARAMETER	SYMBOL	TEST CONDITION[3]	MIN.	MAX.	UNIT
Input Low Voltage[1]	V_{IL}		0	0.8	V
Input High Voltage[1]	V_{IH}		2.0	V_{CC}	V
Input Low Voltage[2]	V_{IL}		0	0.2	V
Input High Voltage[2]	V_{IH}		V_{CC} - 0.2	V_{CC}	V
Output Low Voltage[1]	V_{OL}	I_{OL} = 1 mA, V_{CC} = 3 V	—	0.4	V
Output High Voltage[1]	V_{OH}	I_{OH} = -1 mA, V_{CC} = 3 V	2.4	—	V
Output Low Voltage[2]	V_{OL}	I_{OL} = 100 µA, V_{CC} = 3 V	—	0.2	V
Output High Voltage[2]	V_{OH}	I_{OH} = -100 µA, V_{CC} = 3 V	V_{CC} - 0.2	—	V
Input Leakage Current	I_{LI}	V_{IN} = 0 V to V_{CCMAX}	-5	5	µA
High Impedance (OFF-State) Output Leakage Current	I_{OZ}	V_{IN} = 0 V to V_{CCMAX}	-5	5	µA
Operating Current (Active Mode)	I_{CCAT}	Condition 1	—	60	mA
Operating Current (Standby Mode)	I_{CCSB}	Condition 2	—	2	mA
Operating Current (Sleep Mode)	I_{CCSL}	Condition 3	—	1	mA
Operating Current (Stop Mode)	I_{CCST}	Condition 4	—	40	µA

NOTES:

1. TTL
2. CMOS
3. Condition 1 (Active Mode):
   - CMOS Input levels
   - Recommended Operating Conditions (Table 4)
   - XCLK Frequency = 16 MHz

   Condition 2 (Standby Mode):
   - Same as Condition 1 with Core and Peripherals halted. DRAM Refresh is active.

   Condition 3 (Sleep Mode):
   - Same as Condition 2 with DRAM Refresh disabled.

   Condition 4 (Stop Mode):
   - Same as Condition 3 with XCLK stopped.

AC TEST CONDITIONS

Table 8.
AC Test Conditions[1]

PARAMETER	RATING	UNIT
Input Pulse Levels	V_{SS} to V_{CC}	V
Input Rise and Fall Times	5	ns
Input and Output Timing Ref. Levels	1.5	V
Output Load[2]	50	pF

NOTE:
1. Applies to LH77790A/B (3.3 V and 5.0 V ranges)
2. Includes scope and jig capacitance

PIN CAPACITANCE

Table 9.
Pin Capacitance[1]

PARAMETER	SYMBOL	MAX.	UNIT
Input Capacitance[2]	C_{IN}	10	pF
Output Capacitance[2]	C_{OUT}	20	pF
I/O Capacitance[2]	C_{IO}	20	pF

NOTE:
1. Applies to LH77790A/B (3.3 V and 5.0 V ranges)
2. Measurement Condition: All pins are set to 0 V except measured pin.

AC SPECIFICATIONS

(Over Recommended Operating Voltage, Temperature & AC Test Conditions)

External Clocks

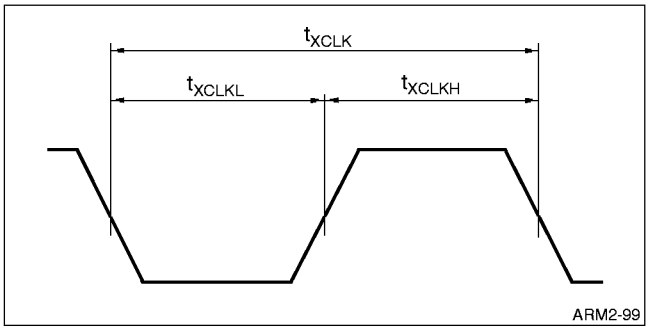

Figure 1. System Clock AC Timing

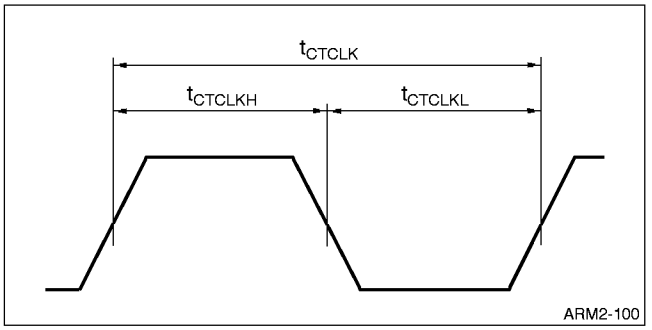

Figure 2. External Counters/Timers Clocks AC Timing

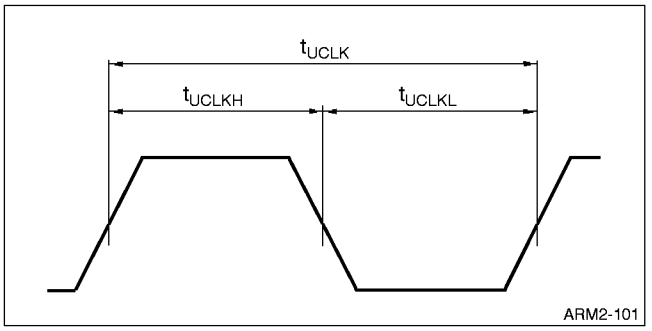

Figure 3. External UARTs/DASK Clock AC Timing

Table 10.
External Clocks AC Specifications

PARAMETER	DESCRIPTION	LH77790A/B (3.3 V RANGE)		LH77790A/B (5.0 V RANGE)		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{XCLK}	XCLK (System Clock) Period	60	—	40	—	ns
t_{XCLKH}	XCLK High Time	1/2	—	1/2	—	t_{XCLK}
t_{XCLKL}	XCLK Low Time	1/2	—	1/2	—	t_{XCLK}
t_{CTCLK}	CTCLK (Counters/Timers External Clock) Period	2	—	2	—	t_{XCLK}
t_{CTCLKH}	CTCLK High Time	1	—	1	—	t_{XCLK}
t_{CTCLKL}	CTCLK Low Time	1	—	1	—	t_{XCLK}
t_{UCLK}[1]	UCLK (UARTs/DASK External Clock) Period	2	—	2	—	t_{XCLK}
t_{UCLKH}[1]	UCLK High Time	1	—	1	—	t_{XCLK}
t_{UCLKL}[1]	UCLK Low Time	1	—	1	—	t_{XCLK}

NOTE:

1. When UCLK is used as a DASK Demodulator Clock, use a 14.318 MHz Oscillator (50% Duty).

SRAM/DRAM Interface

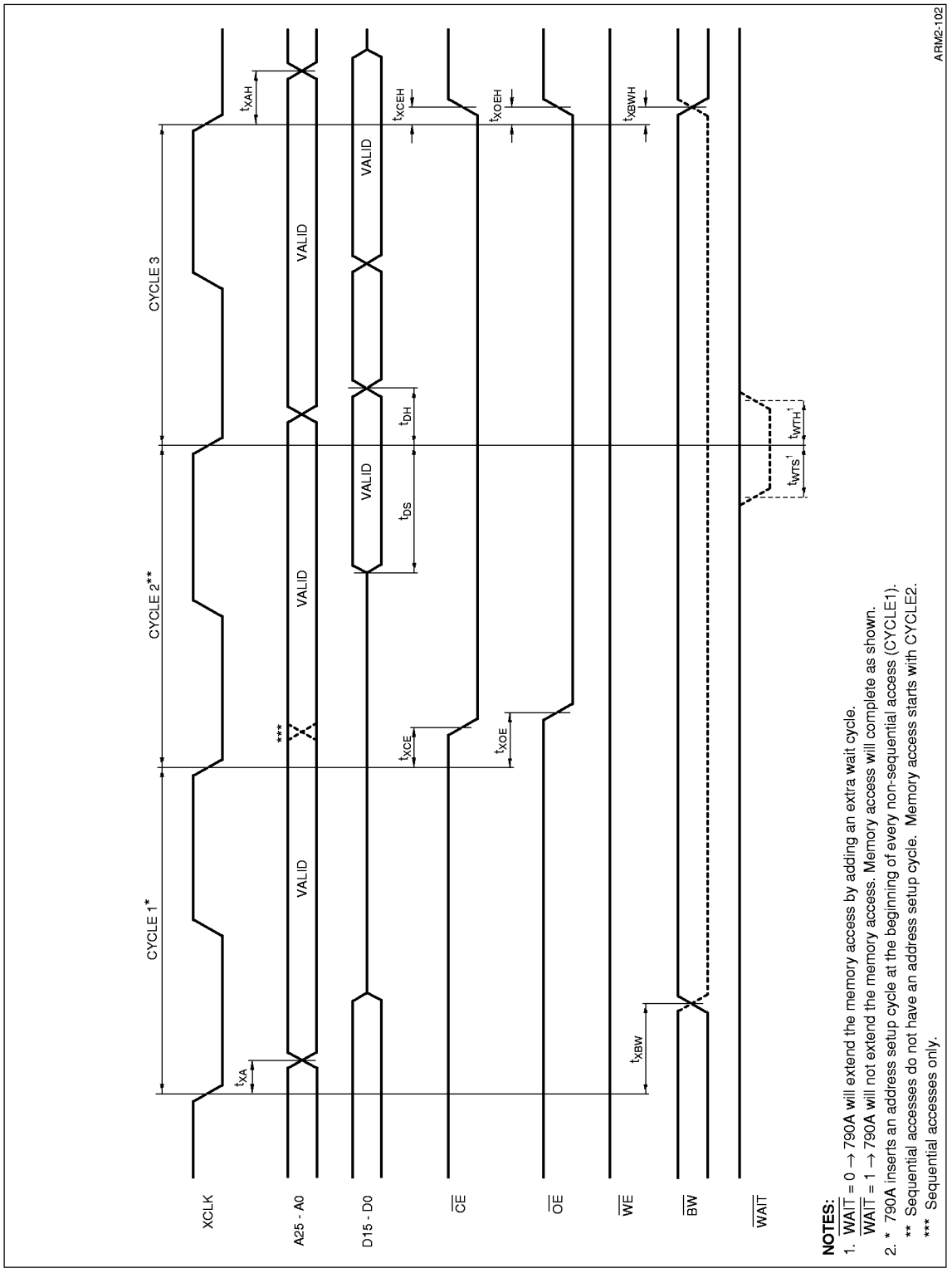

Figure 4. SRAM Read Access AC Timing

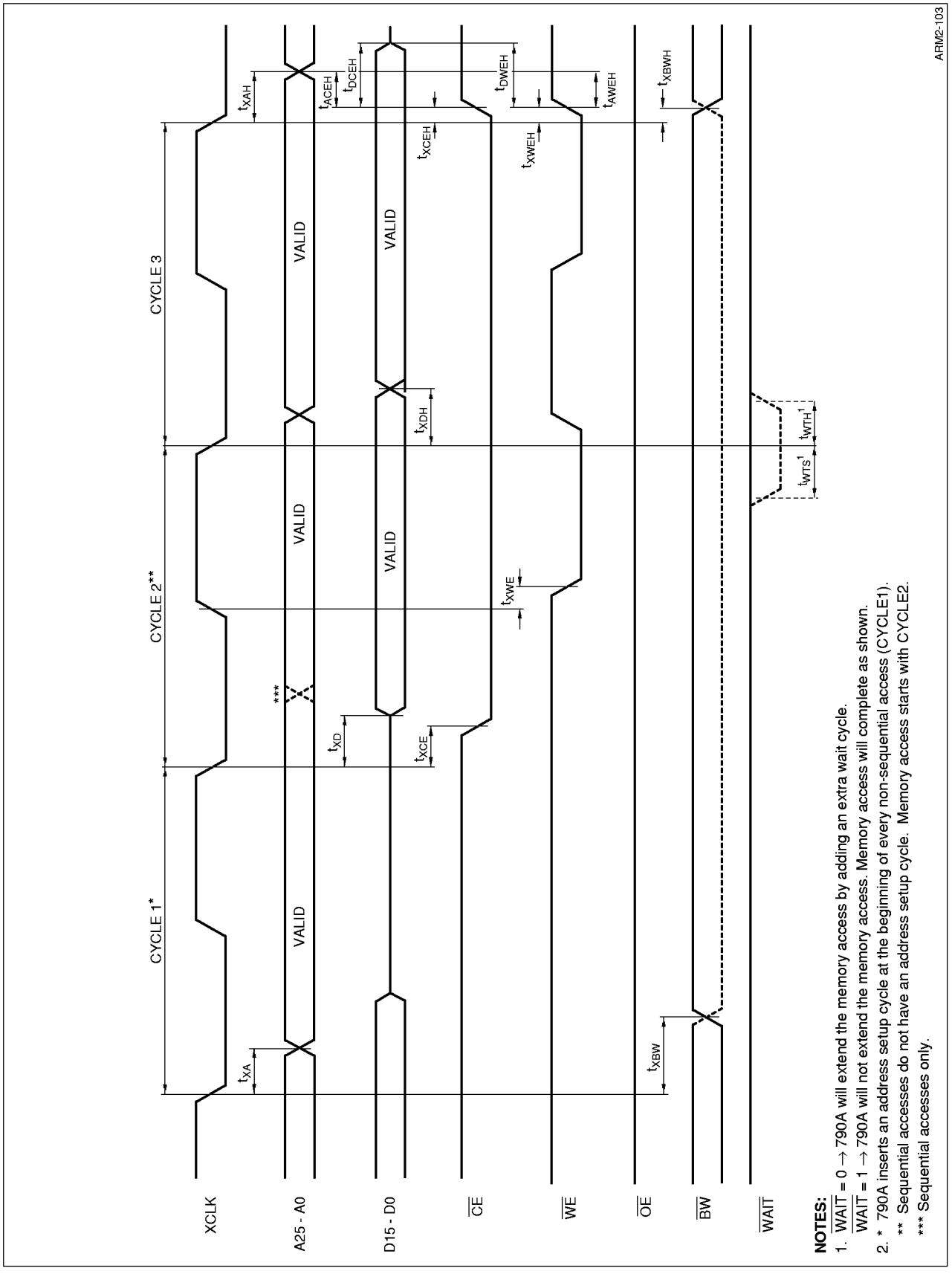

Figure 5. SRAM Write Access AC Timing

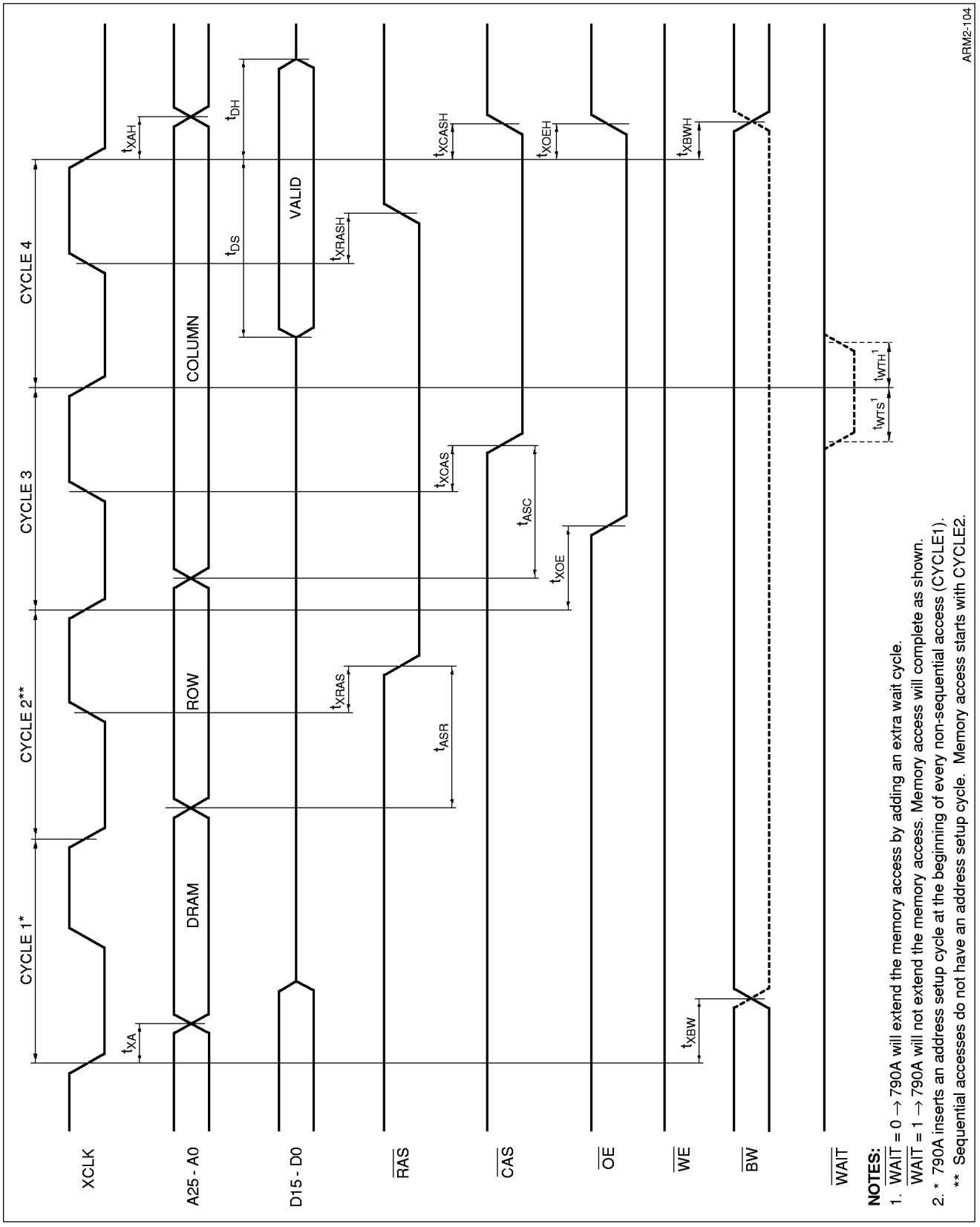

Figure 6. DRAM Read Access AC Timing

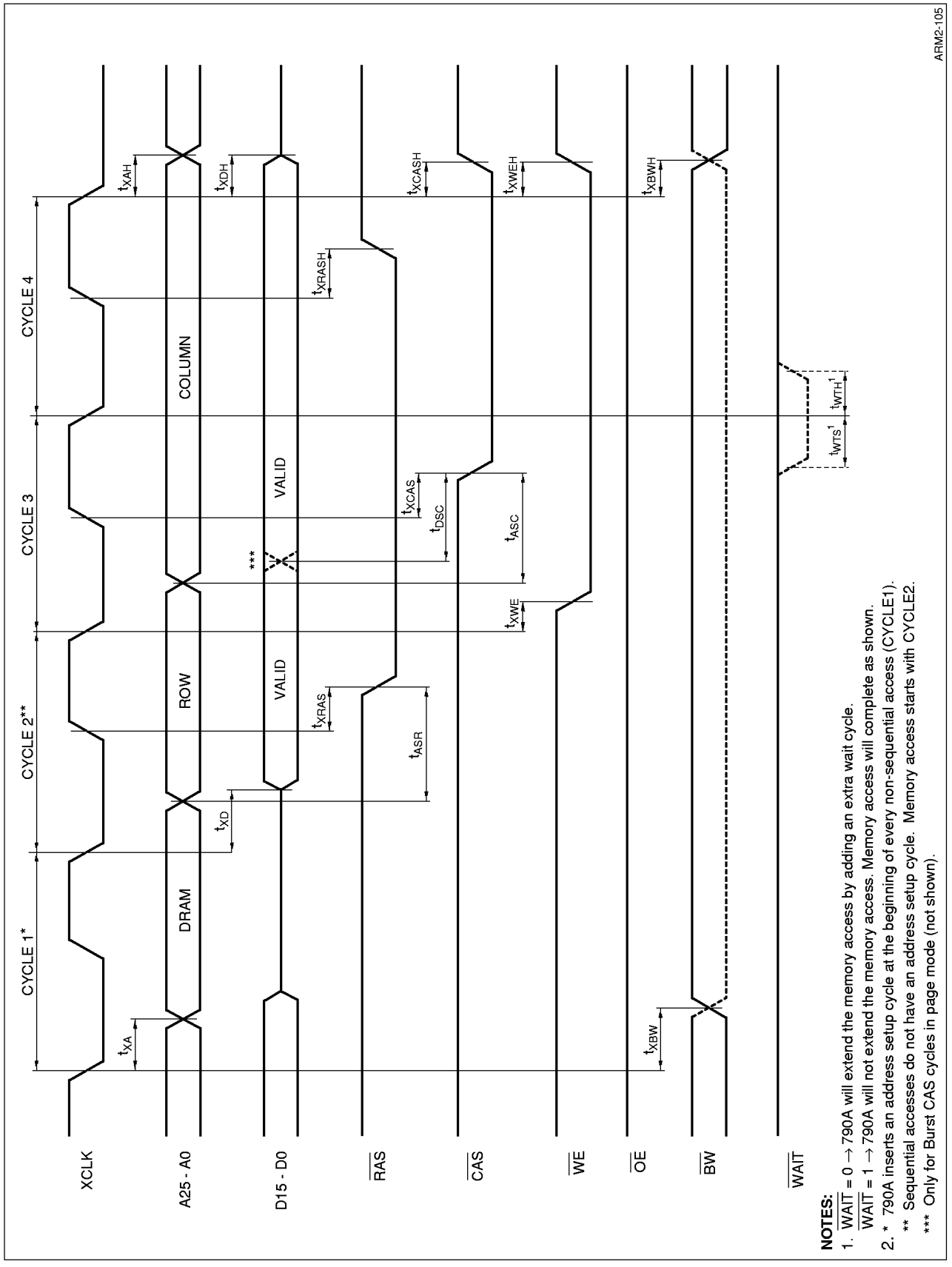

Figure 7. DRAM Write Access AC Timing

Table 11.
SRAM/DRAM AC Specifications

PARAMETER	DESCRIPTION	LH77790A/B (3.3 V RANGE)		LH77790A/B (5.0 V RANGE)		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{XA}	XCLK↓ to Address Valid	—	41	—	33	ns
t_{XAH}	Address Hold relative to XCLK↓	4	—	4	—	ns
t_{XCE}	XCLK↓ to $\overline{CE}$ Active	—	41	—	27	ns
t_{XCEH}	$\overline{CE}$ Hold relative to XCLK↓	4	—	4	—	ns
t_{XWE} (SRAM)	XCLK↑ to $\overline{WE}$ Active (SRAM)	—	35	—	30	ns
t_{XWE} (DRAM)	XCLK↓ to $\overline{WE}$ Active (DRAM)	—	40	—	35	ns
t_{XWEH}	$\overline{WE}$ Hold relative to XCLK↓	4	—	4	—	ns
t_{WTS}	$\overline{WAIT}$ Setup relative to XCLK↓	10	—	10	—	ns
t_{WTH}	$\overline{WAIT}$ Hold relative to XCLK↓	6	—	6	—	ns
t_{XD}	XCLK↓ to Write Data Valid	—	44	—	32	ns
t_{XDH}[1]	Write Data Hold relative to XCLK↓	4	—	4	—	ns
t_{XOE}	XCLK↓ to $\overline{OE}$ Active	—	31	—	25	ns
t_{XOEH}	$\overline{OE}$ Hold relative to XCLK↓	4	—	4	—	ns
t_{DS}	Read Data Setup relative to XCLK↓	13	—	9	—	ns
t_{DH}[1, 3, 4]	Read Data Hold relative to XCLK↓	21	—	19	—	ns
t_{XBW}	XCLK↓ to $\overline{BW}$ Valid	—	35	—	28	ns
t_{XBWH}	$\overline{BW}$ Hold relative to XCLK↓	4	—	4	—	ns
t_{AWEH}	Address Hold relative to $\overline{WE}$ Inactive	0	—	0	—	ns
t_{DWEH}	Data Hold relative to $\overline{WE}$ Inactive	0	—	0	—	ns
t_{ACEH}	Address Hold relative to $\overline{CE}$ Inactive	0	—	0	—	ns
t_{DCEH}	Data Hold relative to $\overline{CE}$ Inactive	0	—	0	—	ns
t_{XRAS}	XCLK↑ to $\overline{RAS}$ Valid	—	26	—	21	ns
t_{XRASH}	$\overline{RAS}$ Hold relative to XCLK↑	2	—	2	—	ns
t_{XCAS}	XCLK↑ to $\overline{CAS}$ Valid	—	32	—	26	ns
t_{XCASH}	$\overline{CAS}$ Hold relative to XCLK↓	4	—	4	—	ns
t_{ASR}	DRAM Row Address Setup relative to $\overline{RAS}$↓	10	—	4	—	ns
t_{ASC}	DRAM Column Address Setup relative to $\overline{CAS}$↓	10	—	5	—	ns
t_{DSC}[2]	DRAM Write Data Setup relative to $\overline{CAS}$↓	10	—	5	—	ns

NOTES:

1. Measures hold time on data bus until data changes. The change could either be a state change or Hi-Impedance change.
2. This parameter is the setup time when both data and $\overline{CAS}$ become valid in the same cycle (Burst CAS cycles in Page Mode).
3. Minimum Data Hold Time with respect to $\overline{CE}$, $\overline{OE}$, and address invalid is 0 ns (SRAM).
4. Minimum Data Hold Time with respect to $\overline{CAS}$ and $\overline{OE}$ invalid is 0 ns (DRAM).

Programmable Peripheral Interface, PPI

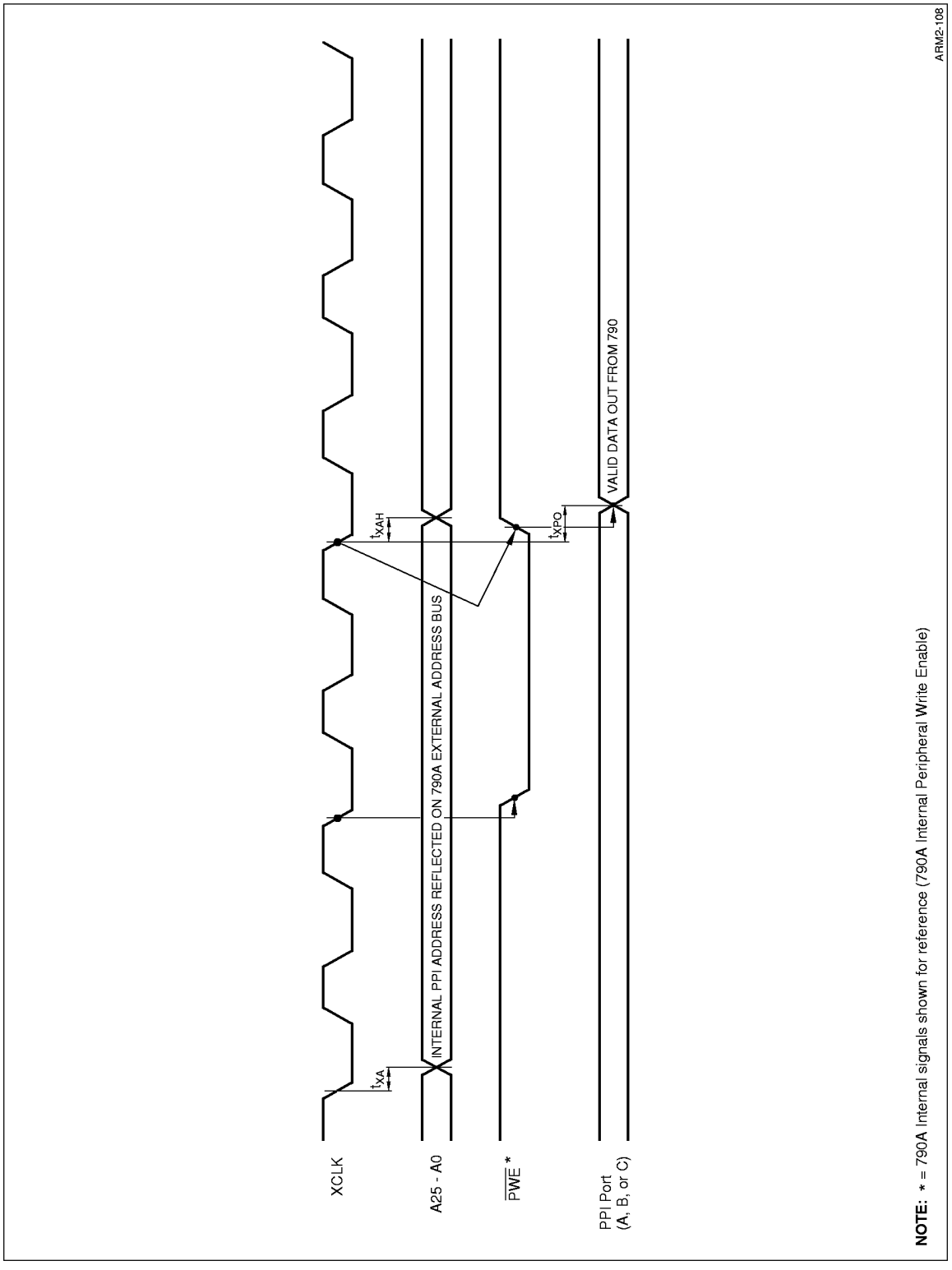

Figure 8. Programmable Peripheral Interface (MODE 0, OUTPUT) AC Timing

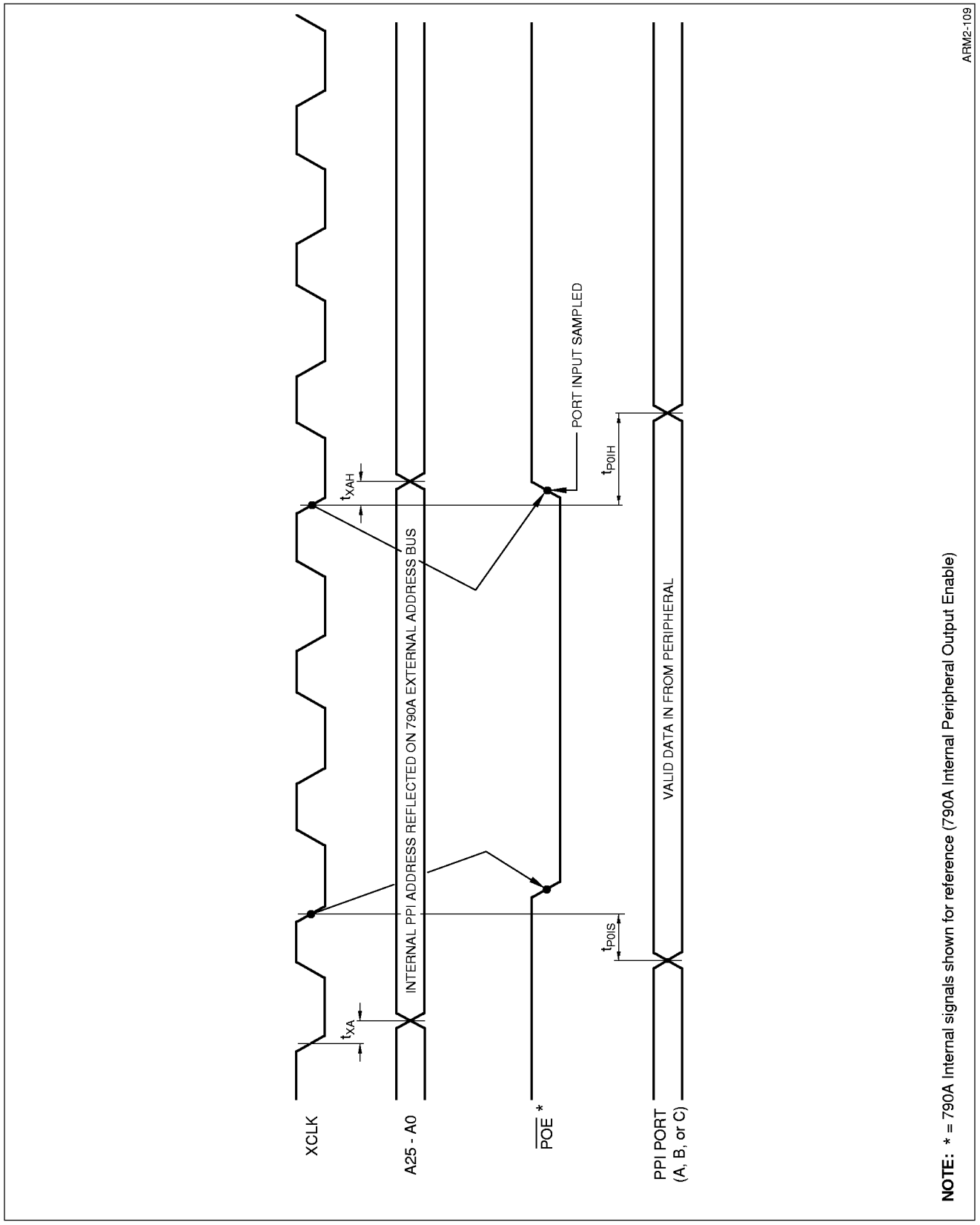

Figure 9. Programmable Peripheral Interface (MODE 0, INPUT) AC Timing

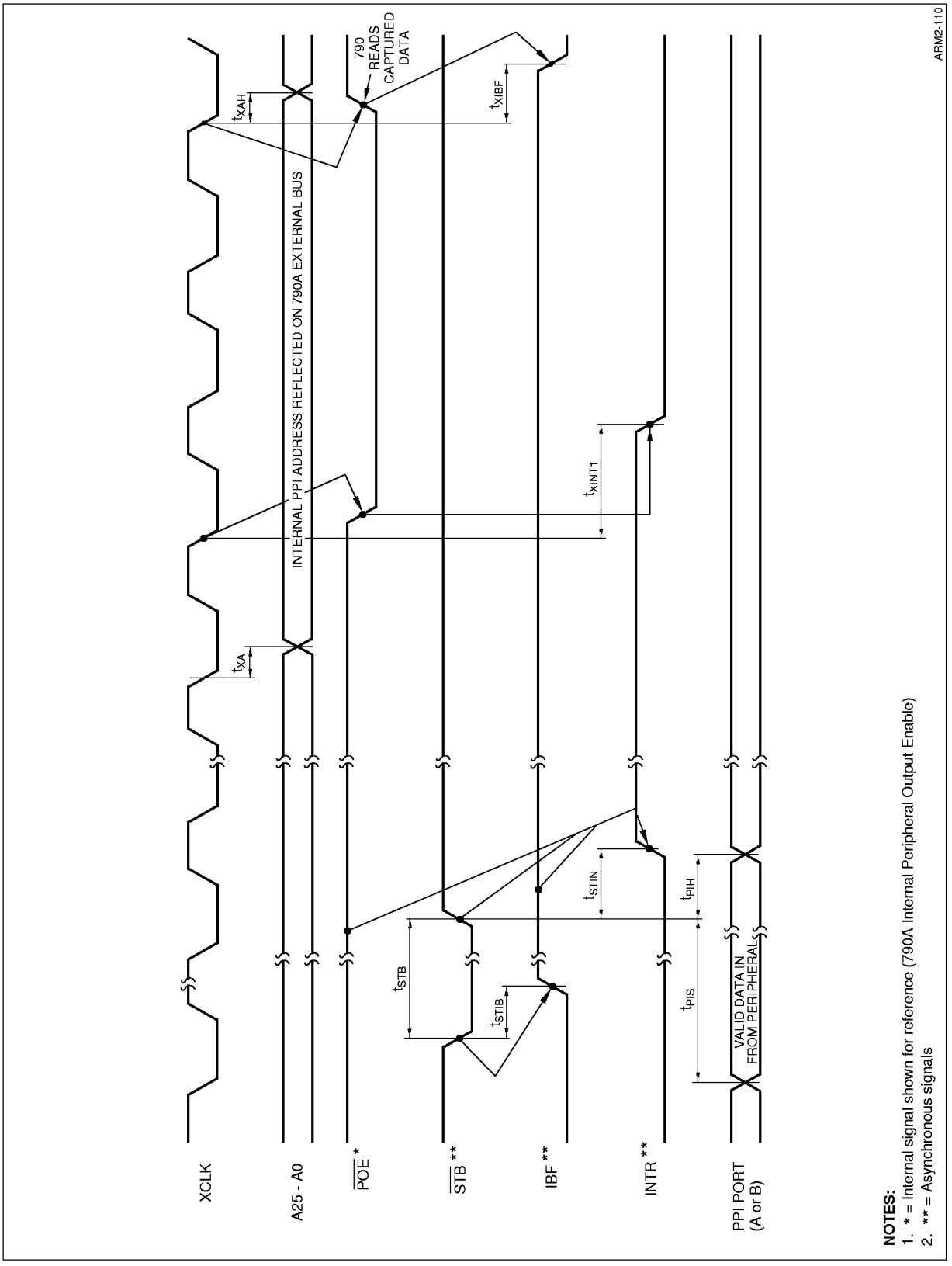

Figure 10. Programmable Peripheral Interface (MODE 1, INPUT) AC Timing

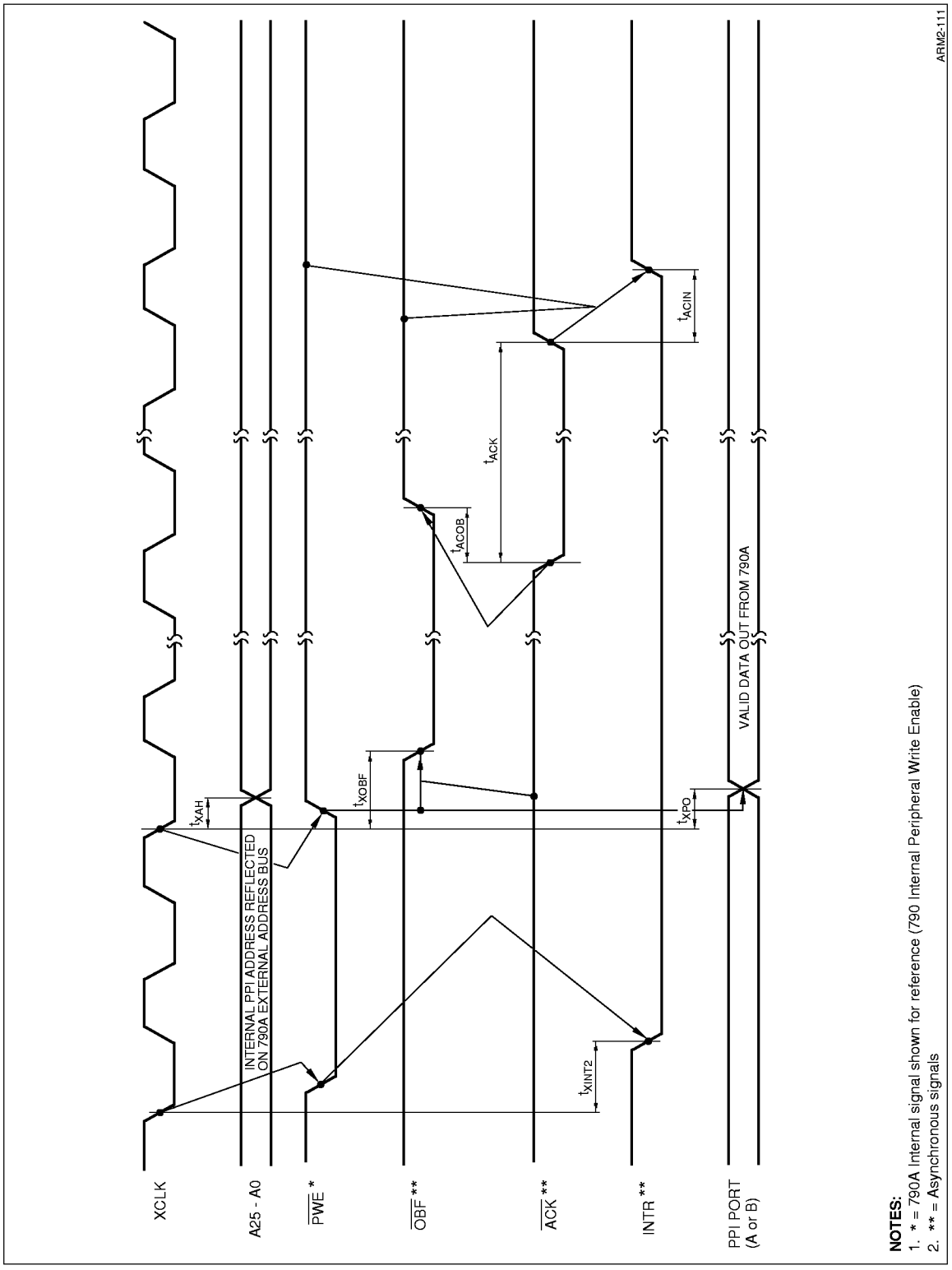

Figure 11. Programmable Peripheral Interface (MODE 1, OUTPUT) AC Timing

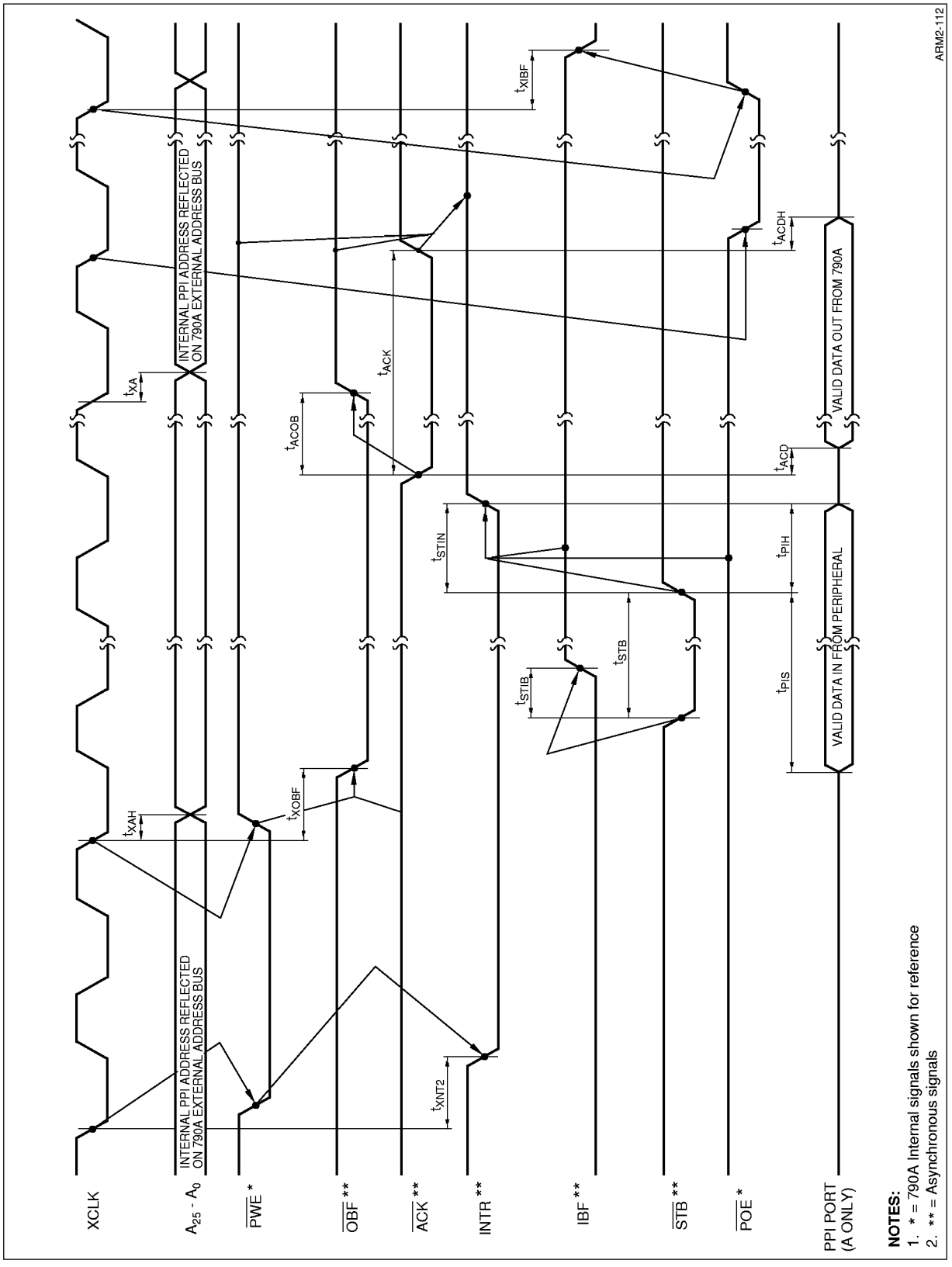

Figure 12. Programmable Peripheral Interface (MODE 2, BIDIRECTIONAL) AC Timing

The PPI has three different modes of operation shown in Figures 8 - 12. Modes 1 and 2 assign alias names to port C when used as control signals depending on the mode of operation. Table 12 shows a cross reference between the alias names which are used in the AC timing diagrams for modes 1 and 2 and the 790A/B external I/O names.

Table 12.
PPI/790 Cross Reference

ALIAS	MODE 1 (INPUT)		MODE 1 (OUTPUT)		MODE 2 (BIDIRECTIONAL)
	PORT A	PORT B	PORT A	PORT B	PORT A
$\overline{STB}$	PC4	PC2	—	—	PC4
IBF	PC5	PC1	—	—	PC5
INTR	PC3	PC0	PC3	PC0	PC3
$\overline{OBF}$	—	—	PC7	PC1	PC7
$\overline{ACK}$	—	—	PC6	PC2	PC6

Table 13.
PPI AC Specifications

PARAMETER	DESCRIPTION	LH77790A/B (3.3 V RANGE)		LH77790A/B (5.0 V RANGE)		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{XPO}	XCLK↓ to Data Out Valid	—	54	—	41	ns
T_{P0IS}	Port Input Setup relative to XCLK↓ (MODE 0)	40	—	41	—	ns
t_{STIB}	$\overline{STB}$ ↓ to IBF↑	—	34	—	27	ns
t_{PIS}	Port Input Setup relative to $\overline{STB}$ ↑ (MODES 1 & 2)	12	—	12	—	ns
t_{P0IH}	Port Input Hold relative to XCLK↓ (MODE 0)	10	—	7	—	ns
t_{PIH}	Port Input Hold relative to $\overline{STB}$ ↑ (MODES 1 & 2)	10	—	7	—	ns
t_{STIN}	$\overline{STB}$ ↓ to INTR↑	—	32	—	25	ns
t_{XINT1}	XCLK↓ to INTR↓ (MODE 1 Input)	—	78	—	57	ns
t_{XIBF}	XCLK↓ to IBF↓	—	52	—	40	ns
t_{STB}	$\overline{STB}$ Pulse Width	17	—	14	—	ns
t_{XINT2} (Bit A)	XCLK↓ to INTR↓ (MODE 1 Output & MODE 2)	—	86	—	56	ns
t_{XINT2} (Port B)	XCLK↓ to INTR↓ (MODE 1 Output & MODE 2)	—	57	—	44	ns
t_{XOBF}	XCLK↓ to $\overline{OBF}$ ↓	—	57	—	44	ns
t_{ACK}	$\overline{ACK}$ Pulse Width	15	—	12	—	ns
t_{ACIN}	$\overline{ACK}$ ↑ to INTR↑	—	34	—	27	ns
t_{ACOB}	$\overline{ACK}$ ↓ to $\overline{OBF}$ ↑	—	44	—	28	ns
t_{ACD}	$\overline{ACK}$ ↓ to Data Out Valid	—	39	—	27	ns
t_{ACDH}	Data Out Hold relative to $\overline{ACK}$ ↑	6	—	6	—	ns

External Reset

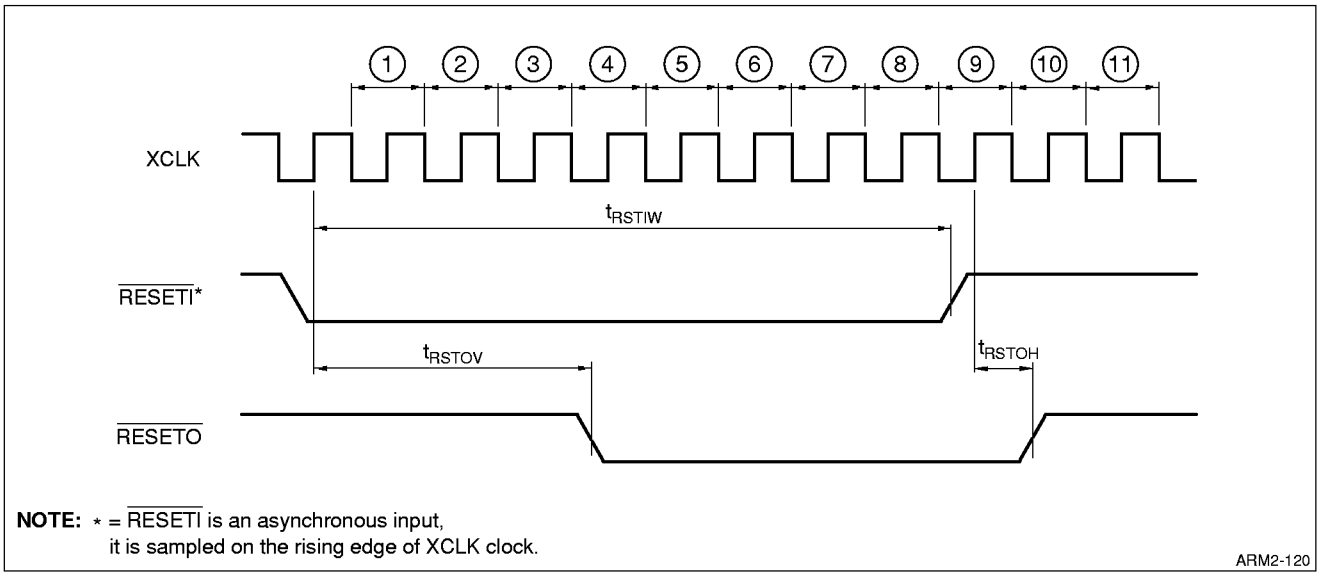

Figure 13. LH77790A/B External Reset AC Timing

Table 14.
External Reset AC Specifications

PARAMETER	DESCRIPTION	LH77790A/B (3.3 V RANGE)			LH77790A/B (5.0 V RANGE)			UNIT
		MIN.	TYPICAL	MAX.	MIN.	TYPICAL	MAX.	
t_{RSTIW}	$\overline{RESETI}$ Pulse Width (Once Sampled Low)	8.5	—	—	8.5	—	—	XCLK
t_{RSTOV}	$\overline{RESETO}$ Valid (Once $\overline{RESETI}$ Sampled Low)	—	3.5	—	—	3.5	—	XCLK
t_{RSTOH}	$\overline{RESETO}$ Hold (Once $\overline{RESETI}$ Sampled High)	—	1	—	—	1	—	XCLK

LCD Controller

The LCD controller signals (VD[7:0], CP1, CP2, S, MCLK, LCDCNTL) are fully programmable to drive most common passive LCD panels. The 'Basic Timing' section of chapter 10 (LCD Controller) in the LH77790A/B User Guide, best describes the relationship between the output signals and the control registers in the LCD controller. The following tables and equations are repeated here for convenience.

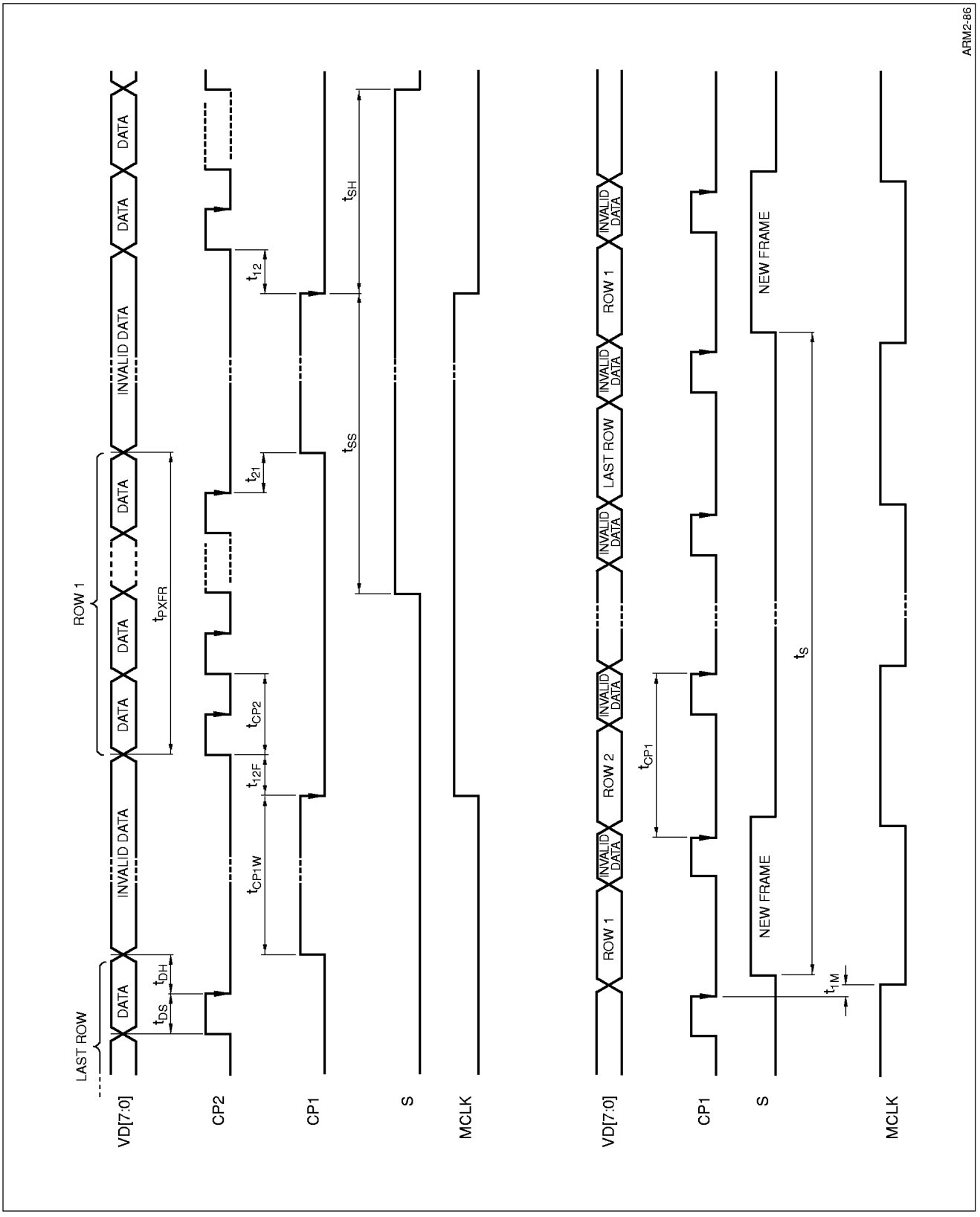

Figure 14. LCD Controller AC Timing

Table 15.
LCD Controller Parameter Description

PARAMETER	DESCRIPTION
DUTY[1]	Number of CP1 Pulses per Frame (LCD_DUTY)
BC[1]	Number of Memory Bytes in a Horizontal Line (LCD_BC)
CP1W[1]	Line Pulse High Width (LCD_CP1W)
CLKDIV[1]	Clock Frequency Divider (LCD_CLKDIV)
$t_{LCD\_in\_CLK}$	LCD Input Clock from Power Management Unit
t_{lcdclk}	LCD Reference Clock (Output of Clock Divider)
t_S	Frame Pulse Period
t_{CP1}	Line Pulse Period
t_{CP2}	Shift Clock Period
t_{PXFR}	Pixels Transfer Time per Line
t_{CP1W}	Line Pulse High Width Time
t_{12}	Current Frame CP1 ↓ to Current Frame CP2 ↑
t_{12F}	Current Frame CP1 ↓ to next frame CP2 ↑
t_{21}	CP2 ↓ to CP1 ↑
t_{DS}	Data Setup time
t_{DH}	Data Hold time
t_{SS}	S signal Setup time
t_{SH}	S signal Hold time
t_{1M}	CP1 ↓ to MCLK Inverting

The following equations[1] and parameters describe the relationship between LCD input Clock, S, CP1, CP2, and MCLK.

$t_{lcdclk} = CLKDIV \times t_{LCD\_in\_CLK}$ ($t_{LCD\_in\_CLK}$ = XCLK Period)

$t_S = t_{CP1} \times DUTY$

$t_{CP1} = t_{PXFR} + t_{CP1W} + t_{12}$

NOTE :

1. Decimal equivalent values must be used in timing equations.

t_{PXFR}, t_{CP1W}, and t_{CP2} vary from one display mode to another. Their typical values are listed in Table 16.

Table 16.
Typical AC Timing for LCD Controller (3.3 V and 5.5 V Ranges)

DISPLAY MODE	t_{PXFR}	t_{CP1W}	t_{CP2}
1a (4-bit)	$2 \times BC \times t_{CP2}$	$(CP1W + 1/2) \times t_{CP2}$	$2 \times t_{lcdclk}$
1b (8-bit)	$BC \times t_{CP2}$	$(CP1W + 1/2) \times t_{CP2}$	$4 \times t_{lcdclk}$
2	$BC \times t_{CP2}$	$(CP1W + 1/2) \times t_{CP2}$	$4 \times t_{lcdclk}$
3a (4-bit)	$2 \times BC \times t_{CP2}$	$(CP1W - 1/2) \times t_{CP2}$	$4 \times t_{lcdclk}$
3b (8-bit)	$BC \times t_{CP2}$	$(CP1W) \times t_{CP2}$	$8 \times t_{lcdclk}$
4	$BC \times t_{CP2}$	$(CP1W + 1/2) \times t_{CP2}$	$8 \times t_{lcdclk}$
5	$2 \times BC \times t_{CP2}$	$(CP1W - 1/2) \times t_{CP2}$	$4 \times t_{lcdclk}$
6	$BC \times t_{CP2}$	$(CP1W + 1/2) \times t_{CP2}$	$8 \times t_{lcdclk}$

Other timing parameters are shown in table 17.

Table 17.
Other Typical LCD AC Timing Parameters
(3.3 V and 5.0 V Ranges)

VARIABLE	VALUE
t_{DS}	$1/2 \times t_{CP2}$
t_{DH}	$1/2 \times t_{CP2}$
t_{12}	$1/2 \times t_{CP2}$
t_{12F}	Variable[2]
t_{21}	$1/2 \times t_{CP2}$
t_{SH}	$3.5 \times t_{CP2}$
t_{SS}	$t_{PXFR} + t_{CP1W} - t_{SH}$
t_{1M}[3]	0

NOTES:
1. Actual timing may vary from those calculated depending on current instruction executed, memory speed, DRAM Refresh Rate, . . . etc.
2. Since this delay happens once a frame, its effect on the frame rate is small, t_{12} will be used in the timing equations.
3. MCLK clock changes on a falling edge of CP1 clock as programmed by LCD_MCLKW register.

PACKAGE SPECIFICATIONS

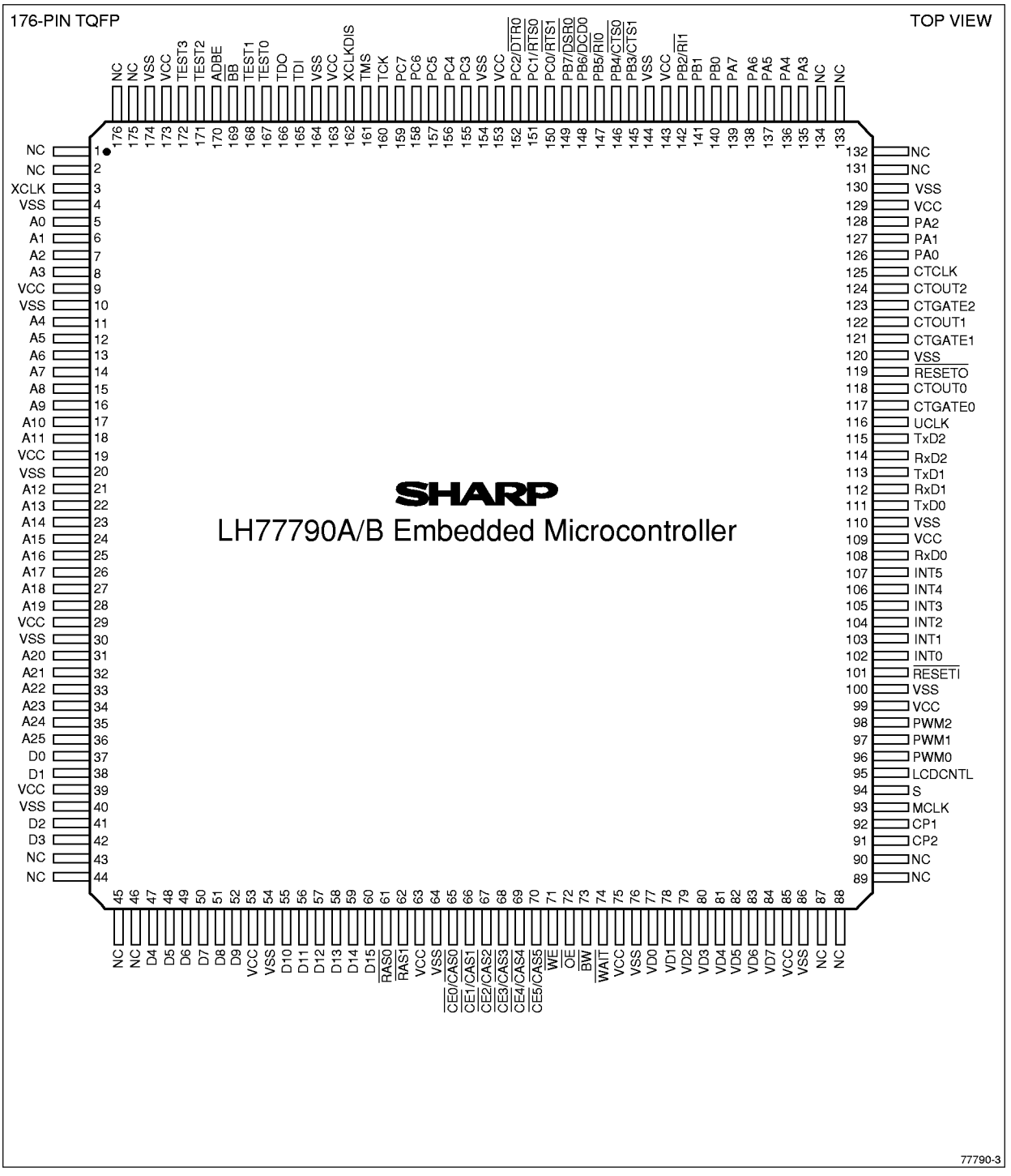

Figure 15. LH77790A/B 176-Lead TQFP (Thin Quad Flat Pack) Pin Assignment

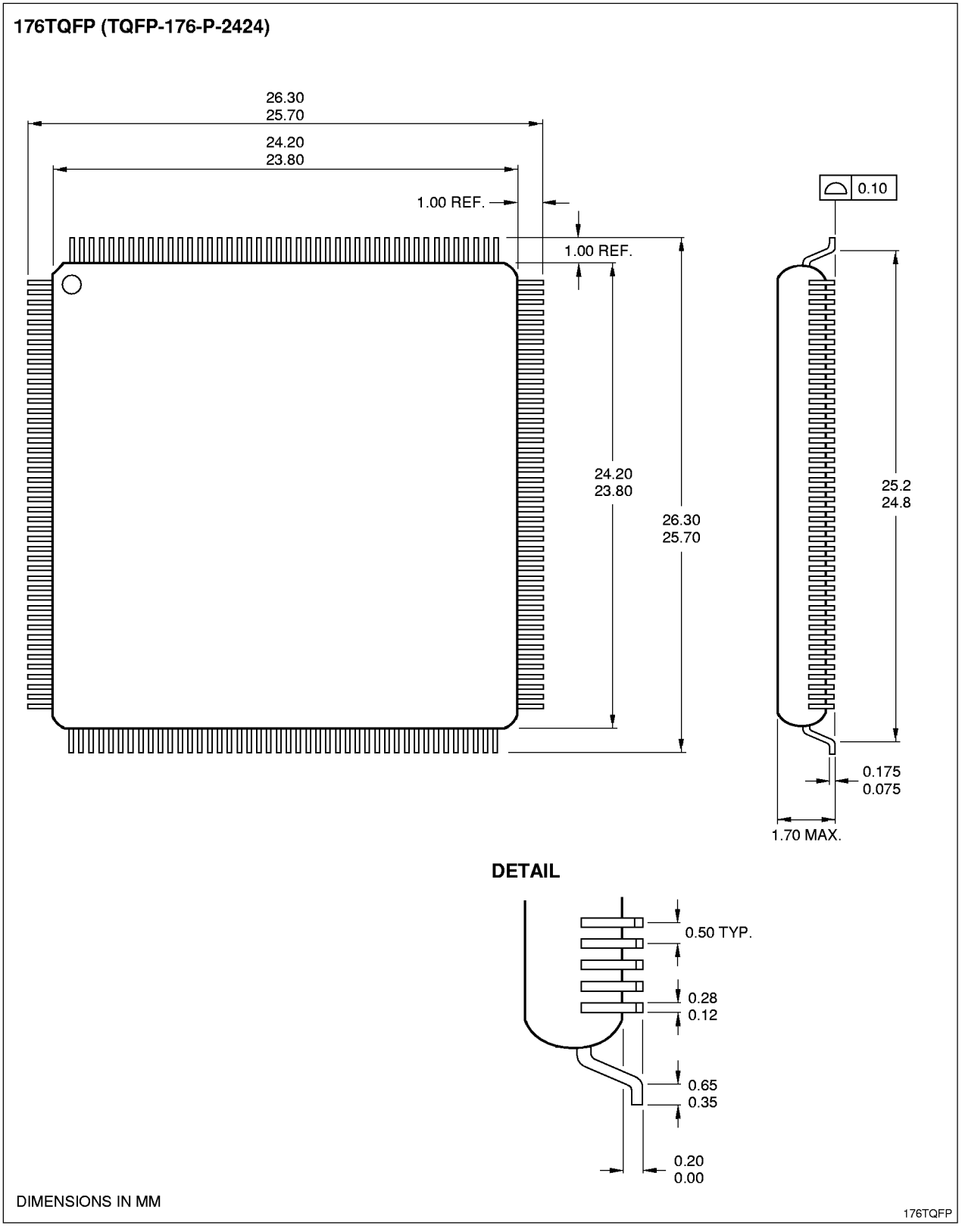

Figure 16. LH77790A/B 176-Lead TQFP (Thin Quad Flat Pack) Package Specification

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