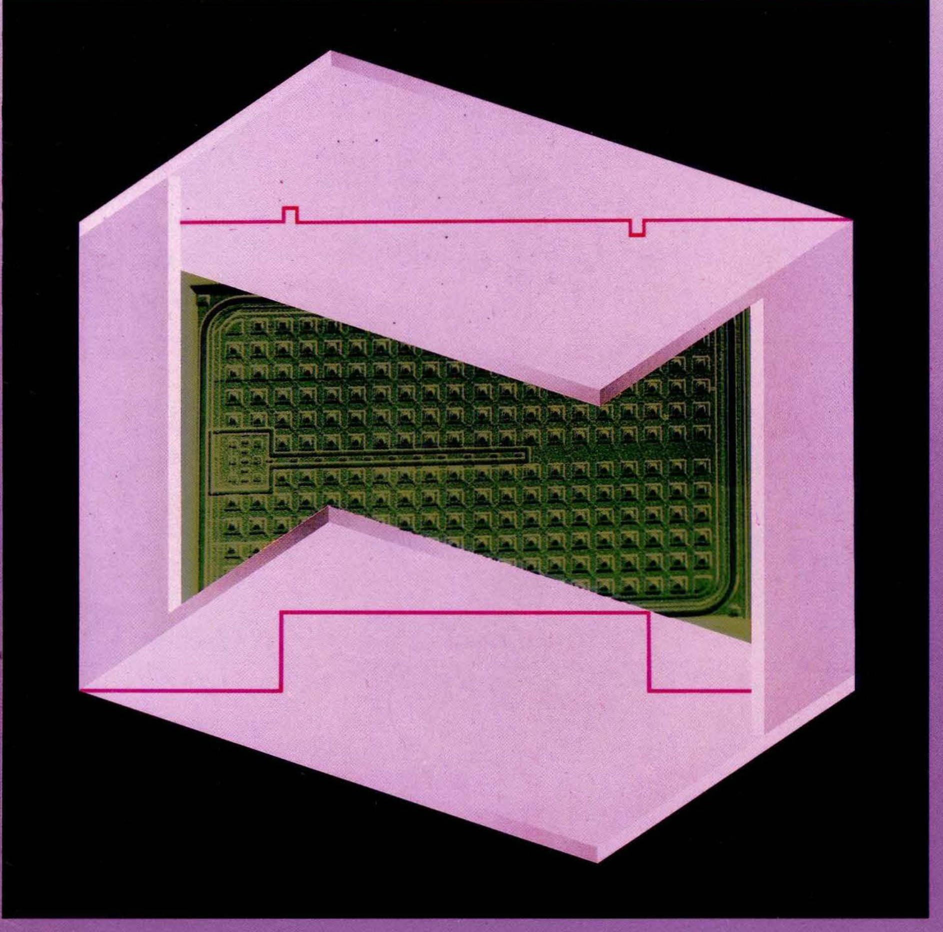
SIEMENS

SIPMOS Components

Data Book 1987/88



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SIPMOS
Components

Data Book 1987/88

Siemens Aktiengesellschaft

SMD Literature List

This data book also contains components for surface mounting (SMD). The small signal transistors of the series BSS 84, BSS 87, BSS 123, BSS 131 and BSS 138 now offer the same advantages as MOS components for automatic assembly.

A **new series of publications** provides information on basic and special aspects of SMD technology. Up to now the series comprises the following titles:

Title	Ordering no.
An Introduction to Surface Mounting	B3-B3289-X-X-7600
Recommendations for PCB Layouts	B3-B3580-X-X-7600
Test Strategies and Test Procedures for SMD Assemblies	B9-B3533-X-X-7600
SMD Automatic Placement System MS-72	B9-M36-X-X-7600
SMD Automatic Placement System HS-180	B9-M34-X-X-7600
Recommendations for SMD Soldering (in preparation)	–

The above mentioned literature can be obtained from your nearest Siemens Office or Representative.

Moreover we would like to draw your attention to our relevant data books:

Title	Ordering no.
Discrete Semiconductors for Surface Mounting	B3-B3497-X-X-7600
Passive Components for Surface Mounting (in preparation)	B4-B3586-X-X-7600

These books can be ordered against a cover charge from your nearest Siemens Office or Representative.

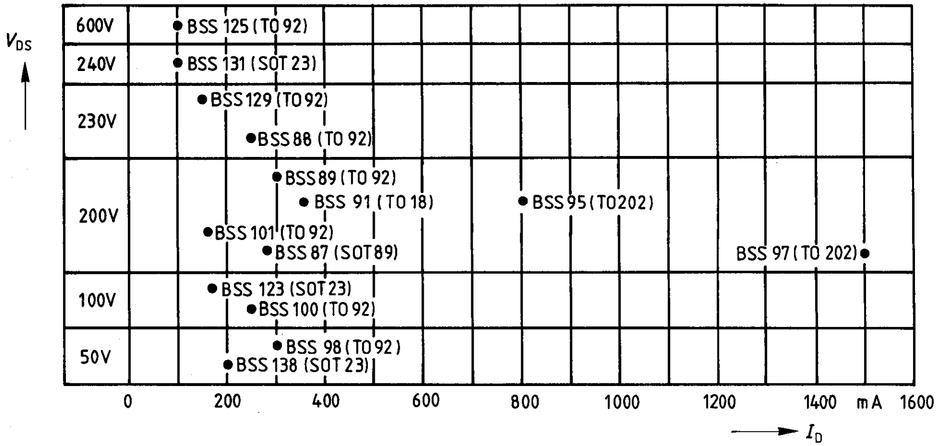
SMD ≙ **S**urface **M**ounted **D**evice

Contents, Summary of Types
Selection Guide, Ordering Codes
Cross Reference, Symbols, Terms, Standards

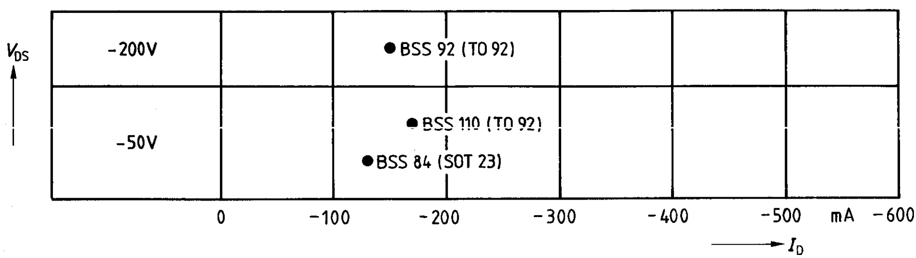
Contents

Summary of Types

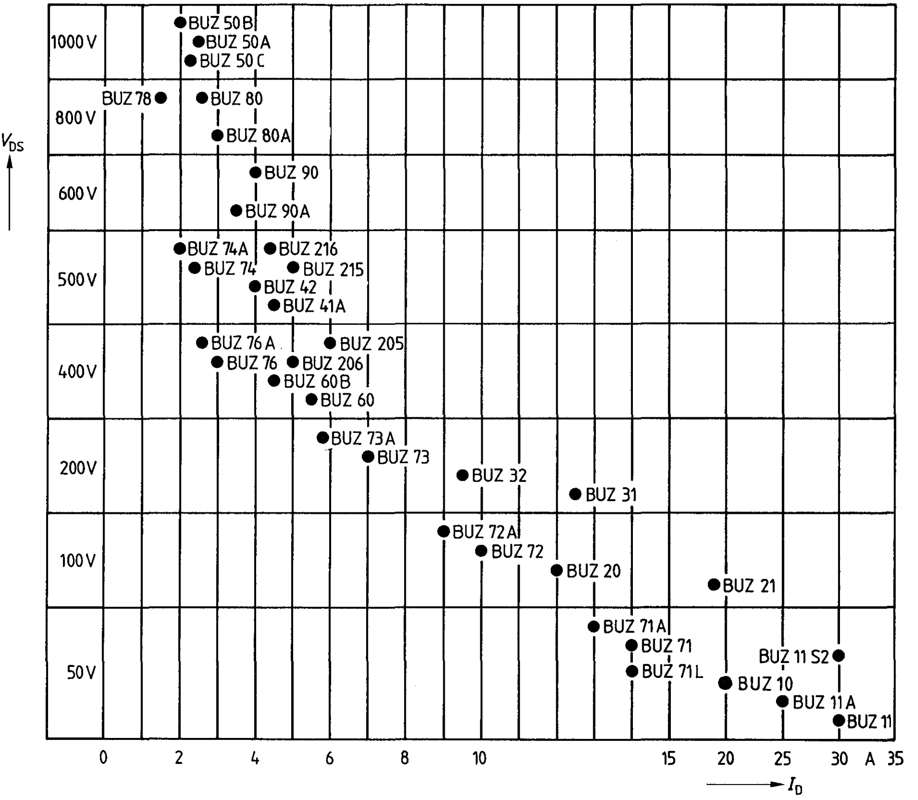
Small signal transistors in case TO 18, TO 92, TO 202, SOT 23 and SOT 89 (N-channel)



Small signal transistors in plastic package TO 92 and SOT 23 (P-channel)



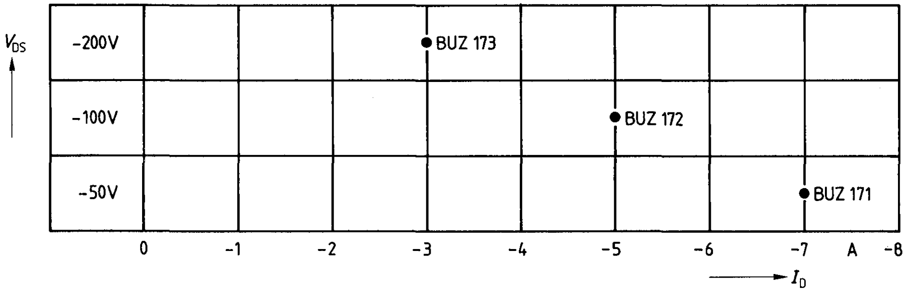
Power transistors in plastic package
14 A 3 in acc. with DIN 41869 or TO 220 AB in acc. with JEDEC
(N-channel)



Summary of Types

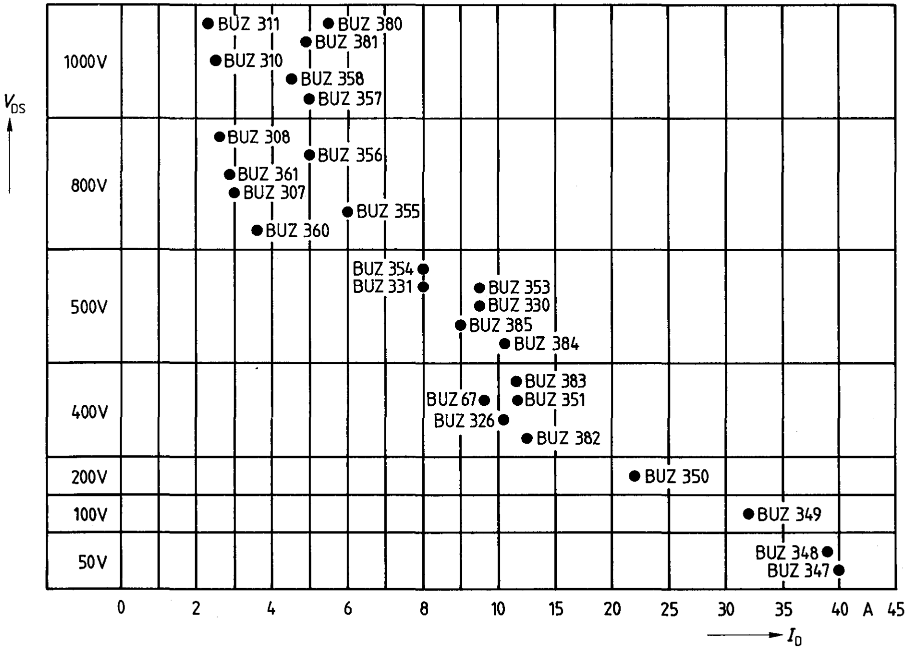
Power transistors in plastic package
14 A3 in acc. with DIN 41869 or TO 220 AB in acc. with JEDEC

(P-channel)



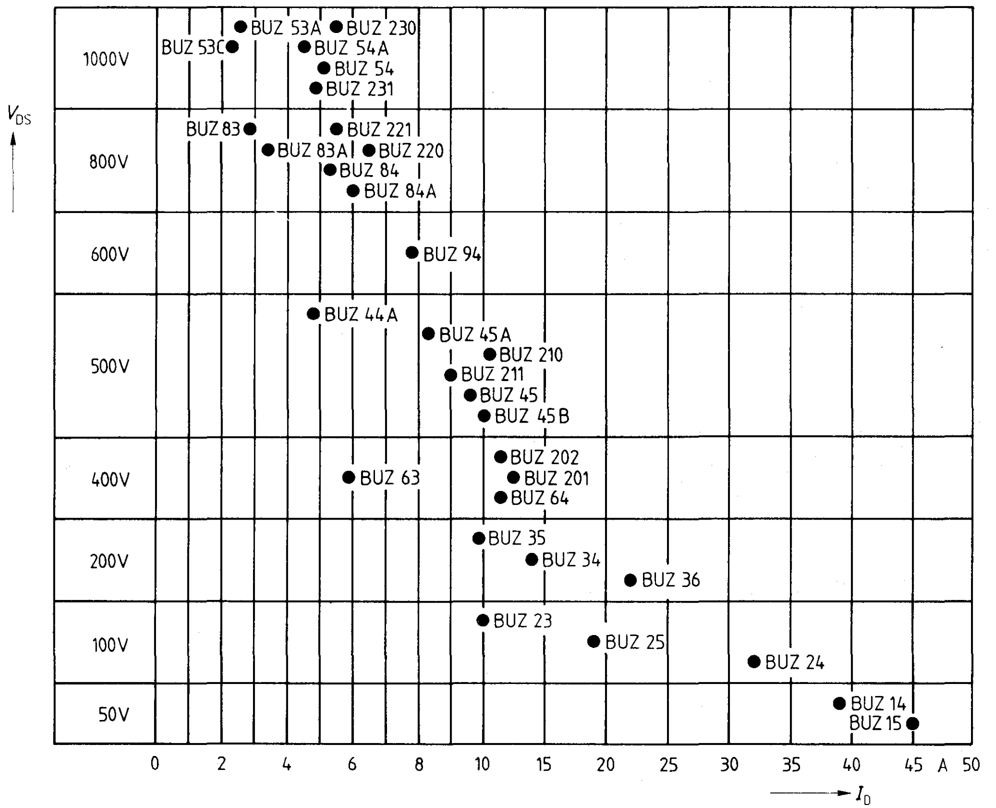
Power transistors in plastic package
15 in acc. with DIN 41869 or TO 218 AA (TOP 3) in acc. with JEDEC

(N-channel)



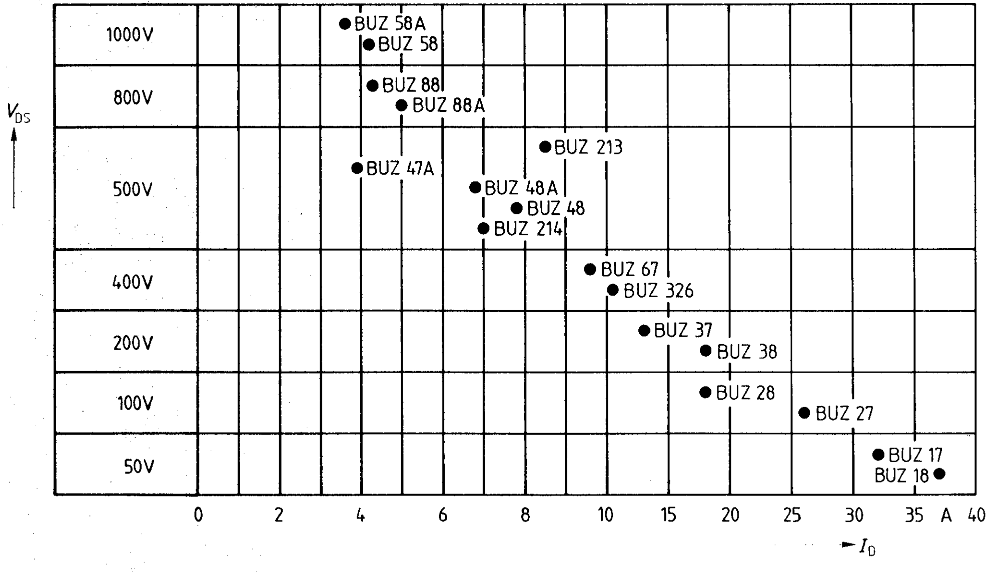
Power transistors in metal case
3 A2 in acc. with DIN 41 872 or TO 204 (TO 3) in acc. with JEDEC

(N-channel)



Power transistors in plastic package
TO 238 AA in acc. with JEDEC

(N-channel)



Small signal transistors – brief characteristics

Type	Channel	V_{DS} V	I_D mA	$R_{DS(on)}$ Ω	Package	Page
BSS 84	P	–50	–130	10,0	SOT 23	72
S BSS 110	P	–50	–170	10,0	TO 92	128
S BSS 92	P	–200	–150	20,0	TO 92	97
BSS 138	N	50	200	3,5	SOT 23	153
S BSS 98	N	50	300	3,5	TO 92	113
S BSS 123	N	100	170	6,0	SOT 23	133
BSS 100	N	100	250	6,0	TO 92	118
S BSS 101	N	200	160	12,0	TO 92	123
S BSS 87	N	200	280	6,0	SOT 89	77
S BSS 89	N	200	300	6,0	TO 92	87
BSS 91	N	200	350	6,0	TO 18	92
S BSS 95	N	200	800	6,0	TO 202	102
S BSS 97	N	200	1500	2,0	TO 202	107
S BSS 129[2]	N	230	150	20,0	TO 92	143
S BSS 88	N	230	250	8,0	TO 92	82
BSS 131	N	240	100	16,0	SOT 23	148
S BSS 125	N	600	100	40,0	TO 92	138

Power transistors – brief characteristics

Type	Channel	V_{DS} V	I_D A	$R_{DS(on)}$ Ω	Package	Page
Drain-source voltage $V_{DS}=50$ V						
S BUZ 171	P	–50	–7	0,4	TO 220	568
S BUZ 71A	N	50	13	0,12	TO 220	436
BUZ 71	N	50	14	0,1	TO 220	430
BUZ 71L	N	50	14	0,1	TO 220	442
S BUZ 10	N	50	20	0,08	TO 220	160
S BUZ 11A	N	50	25	0,06	TO 220	172
S BUZ 11	N	50	30	0,04	TO 220	166
BUZ 11S2	N	50	30	0,04	TO 220	178
BUZ 17	N	50	32	0,04	TO 238	196
S BUZ 18	N	50	37	0,03	TO 238	202
S BUZ 14	N	50	39	0,04	TO 3	184
BUZ 348	N	50	39	0,04	TO 218	718
BUZ 347	N	50	40	0,03	TO 218	712
S BUZ 15	N	50	45	0,03	TO 3	190

Power transistors – brief characteristics

Type	Channel	V_{DS} V	I_D A	$R_{DS(on)}$ Ω	Package	Page
Drain-source voltage $V_{DS}=100$ V						
BUZ 172	P	–100	–5	0,8	TO 220	574
S BUZ 72A	N	100	9,0	0,25	TO 220	454
S BUZ 23	N	100	10	0,2	TO 3	220
S BUZ 72	N	100	10	0,2	TO 220	448
S BUZ 20	N	100	12	0,2	TO 220	208
BUZ 28	N	100	18	0,1	TO 238	244
S BUZ 21	N	100	19	0,1	TO 220	214
S BUZ 25	N	100	19	0,1	TO 3	232
S BUZ 27	N	100	26	0,06	TO 238	238
BUZ 349	N	100	32	0,06	TO 218	724
S BUZ 24	N	100	32	0,06	TO 3	226
Drain-source voltage $V_{DS}=200$ V						
BUZ 173	P	–200	–3	2,0	TO 220	580
S BUZ 73A	N	200	5,8	0,6	TO 220	466
S BUZ 73	N	200	7,0	0,4	TO 220	460
S BUZ 32	N	200	9,5	0,4	TO 220	256
S BUZ 35	N	200	9,9	0,4	TO 3	268
S BUZ 31	N	200	12,5	0,2	TO 220	250
BUZ 37	N	200	13	0,2	TO 238	280
S BUZ 34	N	200	14	0,2	TO 3	262
S BUZ 36	N	200	22	0,12	TO 3	274
S BUZ 38	N	200	18	0,12	TO 238	286
BUZ 350	N	200	22	0,12	TO 218	730
Drain-source voltage $V_{DS}=400$ V						
S BUZ 76A	N	400	2,6	2,5	TO 220	490
S BUZ 76	N	400	3,0	1,8	TO 220	484
S BUZ 60B	N	400	4,5	1,5	TO 220	406
BUZ 206[1]	N	400	5,0	1,5	TO 220	604
S BUZ 60	N	400	5,5	1,0	TO 220	400
S BUZ 63	N	400	5,9	1,0	TO 3	412
BUZ 205[1]	N	400	6,0	1,0	TO 220	598
S BUZ 67	N	400	9,6	0,4	TO 238	424
S BUZ 326	N	400	10,5	0,5	TO 218	694
S BUZ 64	N	400	11,5	0,4	TO 3	418
BUZ 202[1]	N	400	11,5	0,5	TO 3	592
S BUZ 351	N	400	11,5	0,4	TO 218	736
BUZ 383[1]	N	400	11,5	0,5	TO 218	808
BUZ 201[1]	N	400	12,5	0,4	TO 3	586
BUZ 382[1]	N	400	12,5	0,4	TO 218	802

S Preferred types

[1]) FREDFET with fast-recovery reverse diode
[2]) Depletion mode

Power transistors – brief characteristics

Type	Channel	V_{DS} V	I_D A	$R_{DS(on)}$ Ω	Package	Page
Drain-source voltage V_{DS} = 500 V						
S BUZ 74A	N	500	2,0	4,0	TO 220	478
S BUZ 74	N	500	2,4	3,0	TO 220	472
BUZ 47A	N	500	2,0	3,9	TO 238	328
S BUZ 42	N	500	4,0	2,0	TO 220	298
BUZ 216[1])	N	500	4,4	2,0	TO 220	640
S BUZ 41A	N	500	4,5	1,5	TO 220	292
S BUZ 44A	N	500	4,8	1,5	TO 3	304
BUZ 215[1])	N	500	5,0	1,5	TO 220	634
BUZ 48A	N	500	6,8	0,8	TO 238	340
BUZ 214[1])	N	500	7,0	0,8	TO 238	628
S BUZ 48	N	500	7,8	0,6	TO 238	334
BUZ 331	N	500	8,0	0,8	TO 218	706
S BUZ 354	N	500	8,0	0,8	TO 218	748
S BUZ 45A	N	500	8,3	0,8	TO 3	316
BUZ 213[1])	N	500	8,5	0,6	TO 238	622
S BUZ 211[1])	N	500	9,0	0,8	TO 3	616
BUZ 385[1])	N	500	9,0	0,8	TO 218	820
BUZ 330	N	500	9,5	0,6	TO 218	700
S BUZ 353	N	500	9,5	0,6	TO 218	742
S BUZ 45	N	500	9,6	0,6	TO 3	310
BUZ 45B	N	500	10	0,5	TO 3	322
S BUZ 210[1])	N	500	10,5	0,6	TO 3	610
BUZ 384[1])	N	500	10,5	0,6	TO 218	814
Drain-source voltage V_{DS} = 600 V						
BUZ 90A	N	600	3,5	2,5	TO 220	556
BUZ 90	N	600	4,0	2,0	TO 220	550
BUZ 94	N	600	7,8	0,9	TO 3	562
Drain-source voltage V_{DS} = 800 V						
BUZ 78	N	800	1,5	8,0	TO 220	496
S BUZ 80	N	800	2,6	4,0	TO 220	502
S BUZ 308	N	800	2,6	4,0	TO 218	676
S BUZ 83	N	800	2,9	4,0	TO 3	514
BUZ 361[1])	N	800	2,9	4,5	TO 218	784
S BUZ 80A	N	800	3,0	3,0	TO 220	508
S BUZ 307	N	800	3,0	3,0	TO 218	670
S BUZ 83A	N	800	3,4	3,0	TO 3	520
BUZ 360[1])	N	800	3,6	3,0	TO 218	778
BUZ 88	N	800	4,3	2,0	TO 238	538
S BUZ 88A	N	800	5,0	1,5	TO 238	544
S BUZ 356	N	800	5,0	2,0	TO 218	760
S BUZ 84	N	800	5,3	2,0	TO 3	526
BUZ 221[1])	N	800	5,5	2,0	TO 3	652
S BUZ 84A	N	800	6,0	1,5	TO 3	532
S BUZ 355	N	800	6,0	1,5	TO 218	754
BUZ 220	N	800	6,5	1,5	TO 3	646

Power transistors – brief characteristics

Type	Channel	V_{DS} V	I_D A	$R_{DS(on)}$ Ω	Package	Page
Drain-source voltage V_{DS} = 1000 V						
S BUZ 50B	N	1000	2,0	8,0	TO 220	352
BUZ 50C	N	1000	2,3	6,0	TO 220	358
BUZ 53C	N	1000	2,3	6,0	TO 3	370
S BUZ 311	N	1000	2,3	6,0	TO 218	688
S BUZ 50A	N	1000	2,5	5,0	TO 220	346
S BUZ 310	N	1000	2,5	5,0	TO 218	682
S BUZ 53A	N	1000	2,6	5,0	TO 3	364
BUZ 58A	N	1000	3,6	2,6	TO 238	394
S BUZ 58	N	1000	4,2	2,0	TO 238	388
S BUZ 54A	N	1000	4,5	2,6	TO 3	382
S BUZ 358	N	1000	4,5	2,6	TO 218	772
BUZ 231[1])	N	1000	4,9	2,6	TO 3	664
BUZ 381[1])	N	1000	4,9	2,6	TO 218	796
S BUZ 357	N	1000	5,0	2,0	TO 218	766
S BUZ 54	N	1000	5,1	2,0	TO 3	376
BUZ 230[1])	N	1000	5,5	2,0	TO 3	658
BUZ 380[1])	N	1000	5,5	2,0	TO 218	790

S Preferred types

[1]) FREDFET with fast-recovery reverse diode

Small signal transistors

Type	Ordering code	Page
BSS 84	Q62702-S393	72
BSS 87	Q62702-S453	77
BSS 88	Q62702-S454	82
BSS 89	Q62702-S455	87
BSS 91	Q62702-S457	92
BSS 92	Q62702-S458	97
BSS 95	Q62702-S461	102
BSS 97	Q62702-S463	107
BSS 98	Q62702-S464	113

Type	Ordering code	Page
BSS 100	Q62702-S483	118
BSS 101	Q62702-S484	123
BSS 110	Q62702-S489	128
BSS 123	Q62702-S507	133
BSS 125	Q62702-S505	138
BSS 129	Q62702-S510	143
BSS 131	Q62702-S554	148
BSS 138	Q62702-S558	153

Power transistors

Type	Ordering code	Page
BUZ 10	C67078-A1300-A2	160
BUZ 11	C67078-A1301-A2	166
BUZ 11A	C67078-A1301-A3	172
BUZ 11S2	C67078-A1301-A5	178
BUZ 14	C67078-A1000-A2	184
BUZ 15	C67078-A1001-A2	190
BUZ 17	C67078-A1600-A2	196
BUZ 18	C67078-A1601-A2	202
BUZ 20	C67078-A1302-A2	208
BUZ 21	C67078-A1308-A2	214
BUZ 23	C67078-A1002-A2	220
BUZ 24	C67078-A1003-A2	226
BUZ 25	C67078-A1011-A2	232
BUZ 27	C67078-A1602-A2	238
BUZ 28	C67078-A1608-A2	244
BUZ 31	C67078-A1304-A2	250
BUZ 32	C67078-A1310-A2	256
BUZ 34	C67078-A1005-A2	262
BUZ 35	C67078-A1014-A2	268
BUZ 36	C67078-A1018-A2	274
BUZ 37	C67078-A1603-A2	280
BUZ 38	C67078-A1611-A2	286
BUZ 41A	C67078-A1306-A3	292
BUZ 42	C67078-A1311-A2	298
BUZ 44A	C67078-A1007-A3	304
BUZ 45	C67078-A1008-A2	310
BUZ 45A	C67078-A1008-A3	316
BUZ 45B	C67078-A1008-A4	322
BUZ 47A	C67078-A1604-A2	328
BUZ 48	C67078-A1605-A2	334
BUZ 48A	C67078-A1605-A3	340
BUZ 50A	C67078-A1307-A3	346
BUZ 50B	C67078-A1307-A4	352

Type	Ordering code	Page
BUZ 50C	C67078-A1307-A5	358
BUZ 53A	C67078-A1009-A3	364
BUZ 53C	C67078-A1009-A5	370
BUZ 54	C67078-A1010-A2	376
BUZ 54A	C67078-A1010-A3	382
BUZ 58	C67078-A1607-A2	388
BUZ 58A	C67078-A1607-A3	394
BUZ 60	C67078-A1312-A2	400
BUZ 60B	C67078-A1312-A4	406
BUZ 63	C67078-A1016-A2	412
BUZ 64	C67078-A1017-A2	418
BUZ 67	C67078-A1610-A2	424
BUZ 71	C67078-A1316-A2	430
BUZ 71A	C67078-A1316-A3	436
BUZ 71L	C67078-A1316-A5	442
BUZ 72	C67078-A1313-A2	448
BUZ 72A	C67078-A1313-A3	454
BUZ 73	C67078-A1317-A2	460
BUZ 73A	C67078-A1317-A3	466
BUZ 74	C67078-A1314-A2	472
BUZ 74A	C67078-A1314-A3	478
BUZ 76	C67078-A1315-A2	484
BUZ 76A	C67078-A1315-A3	490
BUZ 78	C67078-A1318-A2	496
BUZ 80	C67078-A1309-A2	502
BUZ 80A	C67078-A1309-A3	508
BUZ 83	C67078-A1012-A2	514
BUZ 83A	C67078-A1012-A3	520
BUZ 84	C67078-A1013-A2	526
BUZ 84A	C67078-A1013-A3	532
BUZ 88	C67078-A1609-A2	538
BUZ 88A	C67078-A1609-A3	544
BUZ 90	C67078-A1321-A2	550
BUZ 90A	C67078-A1321-A3	556

Ordering Codes

Power transistors

Type	Ordering code	Page
BUZ 94	C67078-A1019-A2	562
BUZ 171	C67078-A1450-A2	568
BUZ 172	C67078-A1451-A2	574
BUZ 173	C67078-A1452-A2	580
BUZ 201	C67078-A1101-A2	586
BUZ 202	C67078-A1107-A2	592
BUZ 205	C67078-A1401-A2	598
BUZ 206	C67078-A1403-A2	604
BUZ 210	C67078-A1102-A2	610
BUZ 211	C67078-A1100-A2	616
BUZ 213	C67078-A1700-A2	622
BUZ 214	C67078-A1701-A2	628
BUZ 215	C67078-A1400-A2	634
BUZ 216	C67078-A1402-A2	640
BUZ 220	C67078-A1103-A2	646
BUZ 221	C67078-A1104-A2	652
BUZ 230	C67078-A1105-A2	658
BUZ 231	C67078-A1106-A2	664
BUZ 307	C67078-A3100-A2	670
BUZ 308	C67078-A3109-A2	676
BUZ 310	C67078-A3101-A2	682
BUZ 311	C67078-A3102-A2	688

Type	Ordering code	Page
BUZ 326	C67078-A3112-A2	694
BUZ 330	C67078-A3105-A2	700
BUZ 331	C67078-A3119-A2	706
BUZ 347	C67078-A3115-A2	712
BUZ 348	C67078-A3116-A2	718
BUZ 349	C67078-A3113-A2	724
BUZ 350	C67078-A3317-A2	730
BUZ 351	C67078-A3103-A2	736
BUZ 353	C67078-A3104-A2	742
BUZ 354	C67078-A3106-A2	748
BUZ 355	C67078-A3107-A2	754
BUZ 356	C67078-A3108-A2	760
BUZ 357	C67078-A3110-A2	766
BUZ 358	C67078-A3111-A2	772
BUZ 360	C67078-A3204-A2	778
BUZ 361	C67078-A3200-A2	784
BUZ 380	C67078-A3205-A2	790
BUZ 381	C67078-A3206-A2	796
BUZ 382	C67078-A3207-A2	802
BUZ 383	C67078-A3308-A2	808
BUZ 384	C67078-A3206-A2	814
BUZ 385	C67078-A3210-A2	820

Ferranti	Siemens
ZVN0330L	BUZ76
ZVN0335L	BUZ76
ZVN0340L	BUZ76
ZVN0345L	BUZ74
ZVN0350L	BUZ74A
ZVN1208L	BUZ72A
ZVN1209L	BUZ72A
ZVN1209M	BUZ23
ZVN12A2L	BUZ71A
ZVN12A3L	BUZ71A

General Electric	Siemens
D84CL1	BUZ72A
D84CL2	BUZ72A
D84CN1	BUZ73A
D84CN2	BUZ73A
D84CQ1	BUZ76
D84CQ2	BUZ76
D84CR1	BUZ74
D84CR2	BUZ74
D84DK1	BUZ71A
D84DL2	BUZ21
D84DL4	BUZ20
D84DM2	BUZ32
D84DM4	BUZ32
D84DN1	BUZ32
D84DN2	BUZ32
D84DN4	BUZ32
D84DQ1	BUZ60
D84DQ2	BUZ60
D84DQ3	BUZ60B
D84DQ4	BUZ60B
D84DR1	BUZ41A
D84DR2	BUZ41A
D84EK1	BUZ11/11A
D84EK2	BUZ11A
D84EM1	BUZ21
D86DL1	BUZ25
D86DL2	BUZ25
D86DL4	BUZ23
D86DM2	BUZ35
D86DN1	BUZ35
D86DN2	BUZ35
D86DN4	BUZ35

General Electric	Siemens
D86DQ1	BUZ63
D86DQ2	BUZ63
D86DR1	BUZ44A
D86DR2	BUZ44A
D86EL1	BUZ24
D86EL2	BUZ24
D86EN1	BUZ36
D86EN2	BUZ36
D86EQ1	BUZ64
D86EQ2	BUZ64
D86ER2	BUZ45A
D86FL2	BUZ24

Hitachi	Siemens
2SK308	BUZ23
2SK312	BUZ64
2SK319	BUZ60B
2SK320	BUZ41A
2SK349	BUZ326
2SK350	BUZ353
2SK351	BUZ84
2SK382	BUZ74A
2SK383	BUZ72
2SK398	BUZ23
2SK415	BUZ307
2SK428	BUZ72
2SK440	BUZ73A

I. R.	Siemens
2N6756	BUZ25
2N6758	BUZ35
2N6760	BUZ63
2N6762	BUZ44A
2N6763	BUZ24
2N6764	BUZ24
2N6765	BUZ36
2N6767	BUZ64
IRF120	BUZ23
IRF122	BUZ23
IRF130	BUZ25
IRF132	BUZ23
IRF140	BUZ24
IRF142	BUZ25
IRF150	BUZ24

I.R.	Siemens
IRF152	BUZ24
IRF230	BUZ35
IRF231	BUZ35
IRF232	BUZ35
IRF240	BUZ36
IRF242	BUZ34
IRF243	BUZ34
IRF252	BUZ36
IRF253	BUZ36
IRF330	BUZ63
IRF331	BUZ63
IRF340	BUZ64
IRF341	BUZ64
IRF352	BUZ64
IRF353	BUZ64
IRF430	BUZ44A
IRF431	BUZ44A
IRF432	BUZ44A
IRF433	BUZ44A
IRF440	BUZ45A
IRF441	BUZ45A
IRF452	BUZ45B
IRF520	BUZ72A
IRF522	BUZ72A
IRF530	BUZ21
IRF532	BUZ72A
IRF541	BUZ11S2
IRF542	BUZ21
IRF620	BUZ73A
IRF630	BUZ32
IRF631	BUZ32
IRF642	BUZ31
IRF720	BUZ76
IRF721	BUZ76
IRF722	BUZ76A
IRF723	BUZ76A
IRF730	BUZ60
IRF731	BUZ60
IRF732	BUZ60B
IRF733	BUZ60B
IRF820	BUZ74
IRF821	BUZ74
IRF822	BUZ74A
IRF823	BUZ74A

Cross Reference

I.R.	Siemens
IRF830	BUZ41A
IRF831	BUZ41A
IRF832	BUZ42
IRF833	BUZ42
Motorola	**Siemens**
MTH5N100	BUZ358
MTH5N90	BUZ358
MTH6N90	BUZ358
MTH7N45	BUZ354
MTH7N50	BUZ354
MTH8N35	BUZ351
MTH8N40	BUZ351
MTM10N08	BUZ23
MTM10N10	BUZ23
MTM10N15	BUZ34
MTM12N08	BUZ23
MTM12N10	BUZ23
MTM12N18	BUZ34
MTM12N20	BUZ34
MTM15N18	BUZ34
MTM15N20	BUZ34
MTM20N08	BUZ25
MTM20N10	BUZ25
MTM20N15	BUZ36
MTM25N08	BUZ24
MTM25N10	BUZ24
MTM35N05	BUZ14
MTM4N45	BUZ44A
MTM4N50	BUZ44A
MTM5N35	BUZ63
MTM5N40	BUZ63
MTM5N95	BUZ54A
MTM5N100	BUZ54A
MTM6N55	BUZ94
MTM6N60	BUZ94
MTM7N18	BUZ35
MTM7N20	BUZ35
MTM7N50	BUZ45A
MTM8N10	BUZ23
MTM8N15	BUZ35
MTM8N18	BUZ35
MTM8N20	BUZ35
MTP10N05	BUZ71A
MTP10N08	BUZ72A

Motorola	Siemens
MTP10N10	BUZ72A
MTP12N08	BUZ20
MTP12N10	BUZ20
MTP12N18	BUZ31
MTP12N20	BUZ31
MTP14N05A	BUZ71
MTP15N05	BUZ71A
MTP1N100	BUZ50B
MTP1N95	BUZ50B
MTP20N08	BUZ21
MTP20N10	BUZ21
MTP25N05	BUZ11A
MTP25N06	BUZ11S2
MTP2N45	BUZ74A
MTP2N50	BUZ74A
MTP2N90	BUZ50B
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MTP3N35	BUZ76A
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MTP5N35	BUZ60
MTP5N40	BUZ60
MTP7N15	BUZ73
MTP7N18	BUZ73
MTP7N20	BUZ73
MTP8N10	BUZ72A
MTP8N18	BUZ32
MTM8N20	BUZ32
RCA	**Siemens**
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RFK12N40	BUZ64
RFK25N18	BUZ36
RFK25N20	BUZ36
RFK35N08	BUZ24
RFK35N10	BUZ24
RFK45N05	BUZ15

RCA	Siemens
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RFM12N10	BUZ23
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RFP12N20	BUZ31
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RFP18N10	BUZ21
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RFP4N35	BUZ76
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SGS	**Siemens**
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BUZ10A	BUZ71A
BUZ71	BUZ71
BUZ71A	BUZ71A
BUZ72A	BUZ72A
BUZ76	BUZ76
BUZ76A	BUZ76A
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SEF130	BUZ25
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SEF152	BUZ24
SEF230	BUZ35
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SGS	Siemens
SEF232	BUZ35
SEF233	BUZ35
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SEF631	BUZ32
SEF632	BUZ32
SEF633	BUZ73
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SEF830	BUZ41A
SEF831	BUZ41A
SEF832	BUZ42
SEF833	BUZ42
SEFM10N08	BUZ23
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SEFM12N08	BUZ23

SGS	Siemens
SEFM12N10	BUZ23
SEFM15N18	BUZ36
SEFM15N20	BUZ34
SEFM25N08	BUZ24
SEFM25N10	BUZ24
SEFM35N05	BUZ14
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SGSP330	BUZ74
SGSP331	BUZ76A
SGSP332	BUZ76A
SGSP361	BUZ21
SGSP362	BUZ21
SGSP365	BUZ60
SGSP366	BUZ60
SGSP367	BUZ31

SGS	Siemens
SGSP369	BUZ41A
SGSP382	BUZ11A
SGSP561	BUZ25
SGSP562	BUZ25
SGSP565	BUZ63
SGSP566	BUZ63
SGSP567	BUZ35
SGSP569	BUZ44A
SGSP571	BUZ24
SGSP572	BUZ24
SGSP575	BUZ64
SGSP576	BUZ64
SGSP577	BUZ36
SGSP579	BUZ45B
SGSP592	BUZ15

Siliconix	Siemens
BUP62	BUZ63
BUP64	BUZ44A
BUP65	BUZ46
BUP66	BUZ44A
BUP67	BUZ44A
BUP70	BUZ44A
BUP71	BUZ44A
VN0400D	BUZ10
VN0800A	BUZ25
VN0800D	BUZ21
VN0801A	BUZ25
VN0801D	BUZ20
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VN1001D	BUZ20
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VN3500A	BUZ63
VN3500D	BUZ60
VN3501A	BUZ63
VN4000A	BUZ63
VN4000D	BUZ60
VN4001D	BUZ60B
VN4500D	BUZ41A
VN4501A	BUZ44A
VN4501D	BUZ42
VN4502A	BUZ44A
VN5000D	BUZ41A

Cross Reference

Siliconix	Siemens
VN5001A	BUZ44A
VN5001D	BUZ42
VN5002A	BUZ44A
VNM002A	BUZ63
VNN002A	BUZ44A
VNP002A	BUZ44A

Unitrode	Siemens
UFN120	BUZ23
UFN130	BUZ25
UFN132	BUZ23
UFN140	BUZ24
UFN142	BUZ25
UFN150	BUZ24
UFN152	BUZ24
UFN230	BUZ35
UFN231	BUZ35
UFN232	BUZ35
UFN233	BUZ35
UFN240	BUZ36
UFN241	BUZ36
UFN242	BUZ34

Unitrode	Siemens
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UFN330	BUZ63
UFN331	BUZ63
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UFN620	BUZ73A
UFN621	BUZ73A
UFN630	BUZ73

Unitrode	Siemens
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UFN633	BUZ73
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UFN821	BUZ74
UFN822	BUZ74A
UFN823	BUZ74A
UFN830	BUZ41A
UFN831	BUZ41A
UFN832	BUZ42
UFN833	BUZ42

Symbols, Terms, Standards

Symbols

C	Capacitance
C_{DS}	Drain-source capacitance
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance
C_{iss}	Input capacitance
C_{mi}	Miller capacitance
C_{oss}	Output capacitance
C_{rss}	Reverse transfer capacitance
$D = \frac{t}{T}$	Duty cycle
di/dt	Diode current transconductance
f	Frequency
g_{fs}	Forward transconductance
I_D	Continuous drain current (dc drain current)
$I_{D\,puls}$	Pulsed drain current
I_{DR}	Continuous reverse drain current (dc current, reverse diode)
I_{DRM}	Pulsed reverse drain current (pulsed dc current, reverse diode)
I_{DSS}	Zero gate voltage drain current

Symbols

I_F	Forward on-current
I_{GSS}	Gate-source leakage current
P_D	Power dissipation
P_{DM}	Maximum power dissipation
Q_{Gate}	Gate charge
Q_{rr}	Reverse recovery charge
R_{ch}	Channel resistance
R_D	N^- epi layer resistance
$R_{DS\,(on)}$	Drain-source on-state resistance
R_G	Gate path resistance
R_{GS}	Gate-source resistance
R_L	Load resistance
$R_{th\,JA}$	Thermal resistance (chip-air)
$R_{th\,JC}$	Thermal resistance (chip-case)
$R_{th\,JSR}$	Thermal resistance (chip-substrate rear side)
$t_{d\,(off)}$	Turn-off delay time
$t_{d\,(on)}$	Turn-on delay time
t_f	Fall time
t_{off}	Turn-off time
t_{on}	Turn-on time
t_p	Pulse time
t_r	Rise time
t_{rr}	Reverse recovery time
T_A	Ambient temperature
T_C	Case temperature
T_j	Operating temperature, chip temperature
T_{sold}	Soldering temperature (max.)
T_{SR}	Temperature of substrate rear side
T_{stg}	Storage temperature
$V_{(BR)\,DSS}$	Drain-source breakdown voltage
V_{CC}	Supply voltage, switching-time measurement
V_{DGR}	Drain-gate voltage
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
$V_{GS\,(th)}$	Gate threshold voltage
V_i	Input voltage
V_{is}	Isolation test voltage
V_{op}	Operating voltage
V_{SD}	Diode forward on-voltage
Z_i	Internal impedance
$Z_{th\,JC}$	Transient thermal impedance (chip-case)

Terms

Ambient temperature	T_A
Capacitance	C
Case temperature	T_C
Channel resistance	R_{ch}
Continuous drain current (dc drain current)	I_D
Continuous reverse drain current (dc current, reverse diode)	I_{DR}
Diode current transconductance	di/dt
Diode forward on-voltage	V_{SD}
Drain-gate voltage	V_{DGR}
Drain-source breakdown voltage	$V_{(BR)\,DSS}$

Terms

Drain-source capacitance	C_{DS}
Drain-source on-state resistance	$R_{DS\,(on)}$
Drain-source voltage	V_{DS}
Duty cycle	$D = \frac{t}{T}$
Fall time	t_f
Forward on-current	I_F
Forward transconductance	g_{fs}
Frequency	f
Gate-drain capacitance	C_{GD}
Gate charge	Q_{Gate}
Gate path resistance	R_G
Gate-source capacitance	C_{GS}
Gate-source leakage current	I_{GSS}
Gate-source resistance	R_{GS}
Gate-source voltage	V_{GS}
Gate threshold voltage	$V_{GS\,(th)}$
Input capacitance	C_{iss}
Input voltage	V_i
Internal impedance	Z_i
Isolation test voltage	V_{is}
Load resistance	R_L
Maximum power dissipation	P_{DM}
Miller capacitance	C_{mi}
N^- epi layer resistance	R_D
Operating temperature, chip temperature	T_j
Operating voltage	V_{op}
Output capacitance	C_{oss}
Power dissipation	P_D
Pulsed drain current	$I_{D\,puls}$
Pulsed reverse drain current (pulsed dc current, reverse diode)	I_{DRM}
Pulse time	t_p
Reverse recovery charge	Q_{rr}
Reverse recovery time	t_{rr}
Reverse transfer capacitance	C_{rss}
Rise time	t_r
Soldering temperature (max.)	T_{sold}
Storage temperature	T_{stg}
Supply voltage, switching-time measurement	V_{CC}
Temperature of substrate reverse side	T_{SR}
Thermal resistance (chip-air)	$R_{th\,JA}$
Thermal resistance (chip-case)	$R_{th\,JC}$
Thermal resistance (chip-substrate reverse side)	$R_{th\,JSR}$
Transient thermal impedance (chip-case)	$Z_{th\,JC}$
Turn-off delay time	$t_{d\,(off)}$
Turn-off time	t_{off}
Turn-on delay time	$t_{d(on)}$
Turn-on time	t_{on}
Zero gate voltage drain current	I_{DSS}

Standards

Special units may also be taken from the following documents:
IEC Publication 147-0C, Part 0, IEC Publication 147-1, Part 1 and Publication 147-2G Part 2, DIN 41782, DIN 41791, Part 9, DIN 41792, Part 6, DIN 41858, Diode: DIN 41741.

Technical Information
Explanation of Data Sheet Parameters
Quality Specifications

Technical Information

General

SIPMOS® transistors are self-blocking field-effect transistors with the terminals gate, source and drain. Applying a voltage between the gate and the source causes the channel resistance between the drain and the source to be driven. As with bipolar transistors, a distinction is made between N-channel and P-channel transistors. N-channel types are driven with a positive gate-source voltage and block positive drain-source voltages. With P-channel types the voltage polarities are reversed. SIPMOS transistors have an unsymmetrical blocking response, i. e. they can only block in the drain-source direction. In the opposite direction, the reverse diode is conducting.
There is a larger range of N-channel transistors than P-channel transistors. The reason for this is the essentially better conductivity of the N channel. With MOS transistors of the same blocking voltage and chip area, the drain-source on-resistance $R_{DS\,(on)}$ of a P-channel transistor is more than twice as high as that of an N-channel transistor. Production is also more costly for P-channel models, meaning that the price/performance ratio is distinctly in favor of the N-channel transistor. With appropriate drive arrangements each N-channel transistor may be used in place of a P-channel transistor.

Features

- Voltage-controlled
- High-power switching capability
- Easy to parallel
- Fast switching
- No storage time
- High cutoff frequency
- High current handling capability
- High voltage loading
- No second breakdown
- Linear characteristics

Applications (a selection)

- Power supply units
- Motor speed control
- DC converters
- Inverters
- Proximity switches
- Switched-mode power supplies (SMPS)
- Broadband amplifiers
- AF amplifiers
- Ultrasonic generators
- Uninterruptible power supplies
- Flickerfree data monitors

SIPMOS ≙ Siemens-Power-Metal-Oxide-Semiconductor

1 Technology
1.1 Design of a SIPMOS transistor

SIPMOS transistors have a vertical design with a double-implanted (DIMOS) channel structure (cf. fig. 1).
In an N-channel SIPMOS transistor there is an N^+ substrate with a drain metalization below. Above the N^+ substrate is an N^- epi layer the width of which depends on the drain-source breakdown voltage, and doping concentration. Next comes the gate made of N^+ polysilicon; it is embedded in an isolating silicon dioxide layer and serves as an implantation mask for the P region (barrier region) and the N^+ source region. The source metalization covers the entire structure and thus parallels the individual transistor cells on the chip.

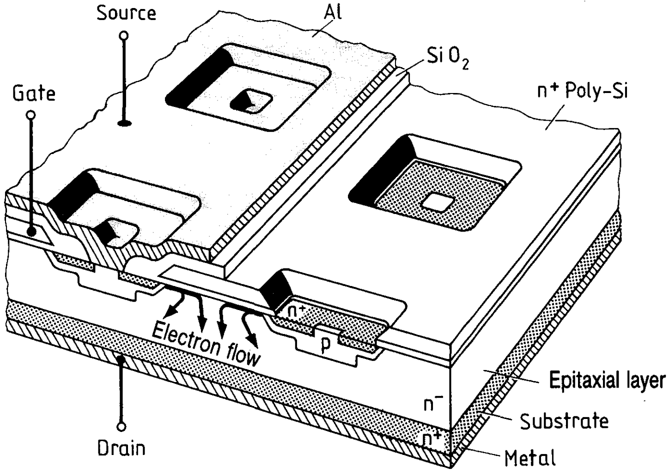


Figure 1 Design of an N-channel SIPMOS transistor

The source metalization forms a secure short circuit between the N^+ and P source regions (cf. fig. 2a). In this way the base-emitter junction of the parasitic vertical N^+PN^- bipolar transistor is shorted. This is essential if it is to be to prevented from turning on during dynamic conditions. Even with high rates of rise of voltage between drain and source, e. g. of magnitude $>2 \times 10^4$ V/µs, and in pure transistor operation, the parasitic NPN transistors are not turned on by currents through the drain-source capacitance. This effect must however be considered if high rates of commutation occur in the reverse diode. The base-collector diode (PN^- junction) then corresponds to the SIPMOS reverse diode.

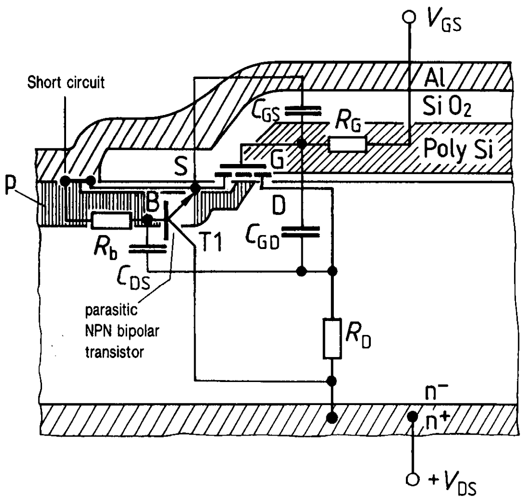


Figure 2a Parasitic bipolar transistor in a cross section of an N-channel SIPMOS

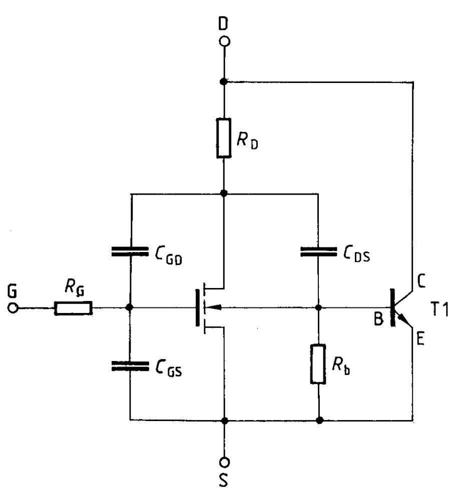


Figure 2b Equivalent circuit diagram with parasitic bipolar transistor

The vertical design of the transistors ensures, i. a. optimal utilization of the chip area, good dissipation of heat, and high drain-source breakdown voltages. The previously mentioned double implantation with its extremely short channel lengths results in very high rates of current rise. The chip of small signal transitors is incorporated in the various packages by the socalled alloy method. This procedure is used for chips of small dimensions and low power and has proved worth in the assembly of millions of transistors. Power transistors are incorporated in their package by epoxy bonding, using an epoxy two-component adhesive with a high content of silver. The adhesive features high thermal and electrical conductivity.
The basic advantage as compared to soldering is the flexibility, which is particulary important for alternating power loads. With small signal transistors contact is established by gold wires in the nailhead procedure, while the leads of power transistor chips are contacted by ultrasonic bonding. Like the chip metalization the wires are made of aluminum. In both cases the thickness of the wires is determined by the maximum permissible drain current.

1.2 Equivalent circuit diagram

It may be assumed that complex admittances and path resistances occur between the connections. With the transistor in the blocking condition the admittances between the connections exhibit capacitive characteristics. These capacitances are: drain-source capacitance C_{DS}, gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} (also known as Miller capacitance C_{mi}). The gate path resistance R_G of a few Ohms magnitude is very much dependent on the chip geometry. In the drain-source path during the turned-on state, the drain-source resistance occurs $R_{DS\,(on)}$, which mainly consists of the sum of the N^- epitaxial layer resistance R_D and the channel resistance R_{ch} (cf. fig. 3).

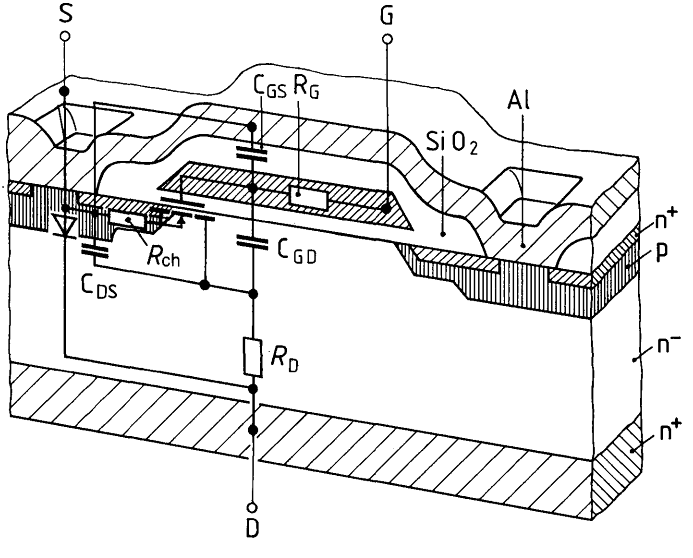


Figure 3 Cross section through an N-channel SIPMOS transistor showing the admittances of the equivalent circuit diagram

In the case of low-voltage transistors ($V_{DS} \leq 100$ V) the channel resistance R_{ch} is dominant; with high blocking types ($V_{DS} > 100$ V) it is the epi layer resistance R_D that dominates. This results in the simplified equivalent circuit diagrams of figures 4a and 4b. The equivalent circuit diagrams shown here are only approximations, of course, because there can be as many as 6000 individual transistor cells paralleled on one chip. You are therefore dealing with distributed capacitances and path resistances, which (in large part) alter as a function of the drain-source voltage.

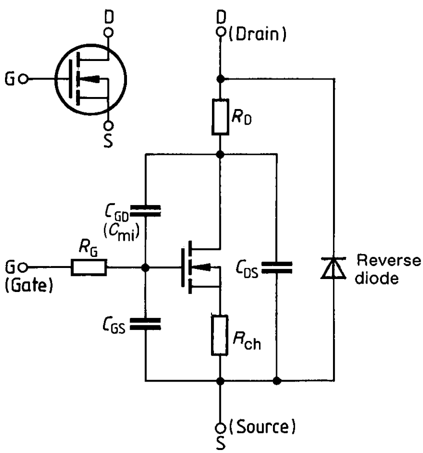


Figure 4a Graphical symbol and equivalent circuit diagram of an N-channel SIPMOS

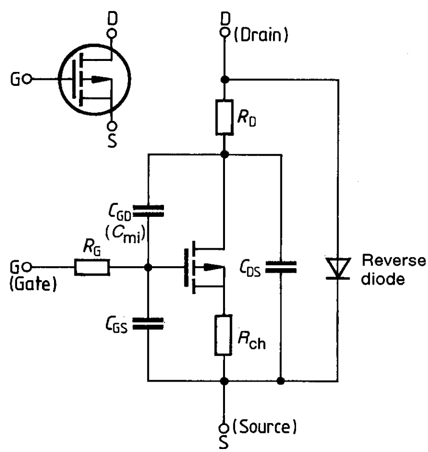


Figure 4b Graphical symbol and equivalent circuit diagram of a P-channel SIPMOS

The voltage dependence of the gate-drain or Miller capacitance has serious effects on the switching behavior. In a simplified representation, a sudden rise in Miller capacitance by a factor of about 10 (cf. fig. 5a) can be seen when there are drain-source voltages that are smaller than or equal to the gate-source drive voltage. In fact, this increase in capacitance sets in somewhat earlier and increases exponentially towards the idealized surge point (cf. curves in data sheets).
The capacitances given in the equivalent circuit diagram cannot be measured individually, of course, they are only to be regarded as interrelated quantities (cf. fig. 5b). There is – neglecting the path resistances – the following relationship between them:

input capacitance	$C_{iss} \approx C_{GS} + C_{GD}$
reverse-transfer capacitance	$C_{rss} \approx C_{GD} (C_{GD} \triangleq C_{mi})$
output capacitance	$C_{oss} \approx C_{DS} + C_{mi}$

The tabulated details in the data book refer to a specific operating point.

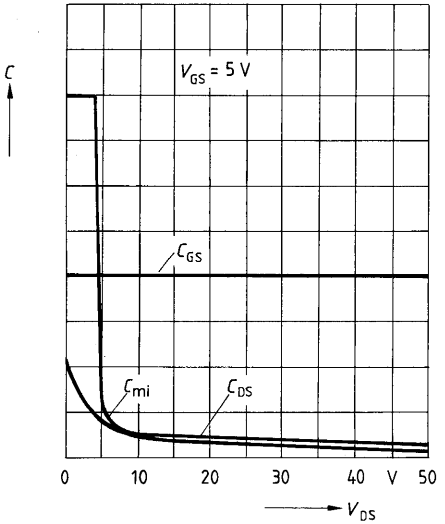


Figure 5 a SIPMOS capacitances of equivalent circuit diagram versus drain-source voltage

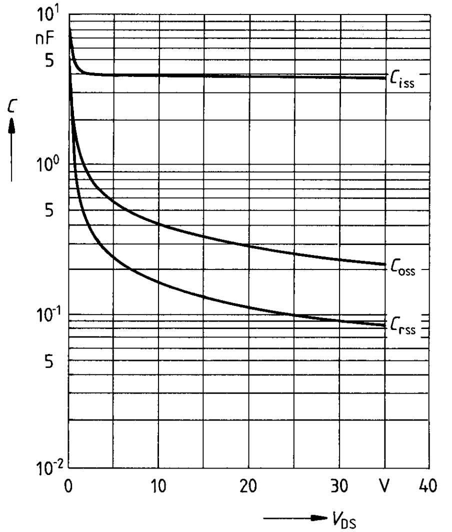


Figure 5 b Interrelated capacitances versus drain-source voltage, taking the BUZ 45 as an example
Parameters: $V_{GS} = 0$, $f = 1$ MHz

1.3 Characteristics

If there is positive drain-source voltage at an N-channel transistor with a drive voltage V_{GS} of 0 V, a temperature and voltage-dependent drain current will flow. This zero gate voltage drain current is specified in the data sheets and amounts to typically a few nA. If the gate-source drive voltage is increased, the transistor remains non-conductive until the gate-source threshold voltage $V_{GS\,(th)}$ is reached. If the drive voltage is increased beyond the gate threshold voltage, the drain current increases according to the transfer characteristic ($I_D = f(V_{GS})$, fig. 6). The transconductance is not linear, lying in the region between 1 S and 20 S and it depends on the transistor type (cf. data sheet).

Description	Small signal transistor	Power transistor
Gate threshold voltage $V_{GS\,(th)}$	0.5...2.8 V at $I_D = 1$ mA	2.1...4 V at $I_D = 1$ mA
Temperature coefficient	−3 mV/°C	−5 mV/°C

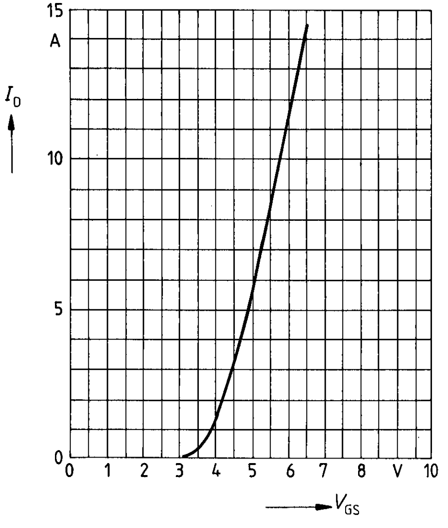


Figure 6 Typical transfer characteristic taking the BUZ 45 as an example
Parameters: 80 μs pulse test, V_{DS} = 25 V, T_j = 25 °C

With a gate-source voltage of less than the threshold voltage the transistor is completely blocked. A negative gate-source voltage will not increase the blocking capability, i. e. the entire family of characteristic curves can be passed with drive voltages of one polarity.
The maximum value of the gate-source voltage is ±20 V (±10 V with small signal transistors) and it is limited by the thickness of the oxide. This value may not be exceeded, even for a short period, because otherwise a breakdown may occur and destroy the transistor. If the drain current is measured as a function of the drain-source voltage with the gate-source drive voltage as parameter, the output characteristic curves (cf. fig. 7 a) are obtained.
In on-state the transistor behaves like an ohmic resistance, i. e. negative drain currents may also flow. In the III quadrant of the characteristics an ohmic response will, of course, only appear in as much as the threshold voltage of the reverse diode has not yet been exceeded (cf. fig. 7 b). This behavior is especially important if rectifier circuits are to be implemented with very low forward voltages or if the reverse recovery time of the reverse diode is to be shortened by increased driving of the transistor.

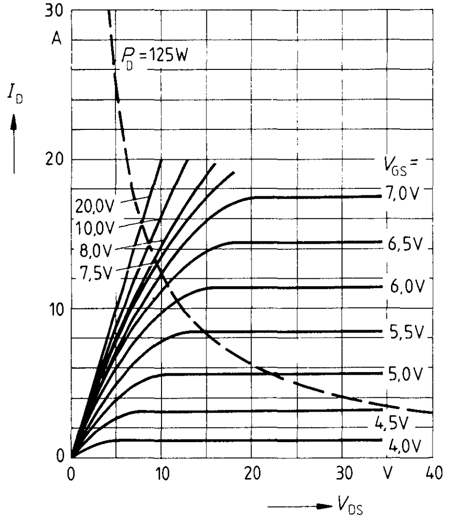


Figure 7 a Typical output characteristics taking the BUZ 45 as an example
Parameters: 80 μs pulse test; T_C = 25 °C

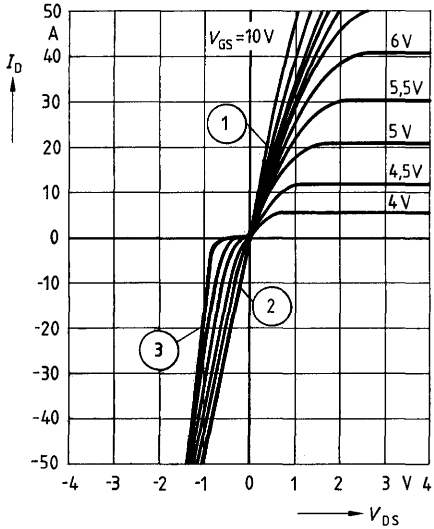


Figure 7 b Output characteristics with reverse diode response
① Transistor output characteristics
② Reverse diode characteristics; forward
③ Reverse diode characteristics; reverse

1.4 Switching behavior

As SIPMOS transistors are voltage-controlled, they do not require any drive current in the steady operating state, but every change in operating state causes charge/discharge currents of the input capacitances. While these currents are of virtually no significance in the AF range (analog operation), they must be taken into account in RF applications and switching operations. Since SIPMOS transistors are primarily used as switches, the switching behavior will be explained in detail.

The switching time of a SIPMOS transistor is determined solely by charging and discharging the input capacitances. The switching time of SIPMOS transistors can be varied over a wide range as the internal impedance Z_i of the drive circuit can be chosen freely. The high internal impedance is limited by the thermal loading capacity due to increasingly occurring switching losses. In case of a low internal impedance the charge/discharge current of the input capacitances is limited by the gate path resistance and the inductance of the drive circuit.

Switching behavior with a resistive load

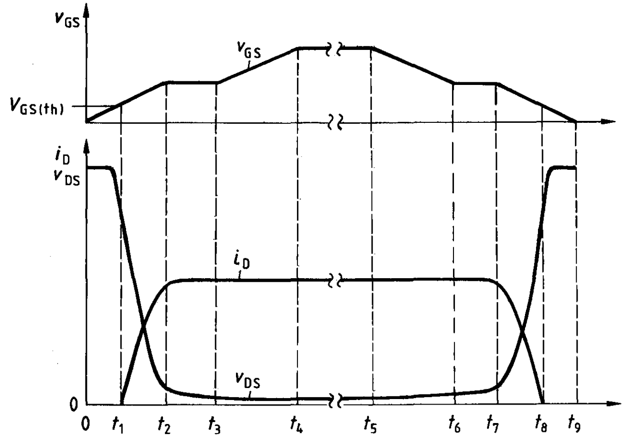
A drive generator with defined internal impedance Z_i, which supplies a square-wave output voltage, is used (cf. test circuit for switching times).

Turn-on procedure

The transistor is driven at time t_0 (cf. fig. 8). The gate-source voltage V_{GS} rises in accordance with the charging process which results from the input capacitance C_{iss} and the internal impedance Z_i of the drive circuit.

As soon as the threshold voltage is reached at time t_1 the transistor starts to conduct. The drain-source voltage drops in proportion to the increasing voltage drop across the load resistance.

Figure 8 Switching behavior with a resistive load



In the period between t_1 and t_2 the drain current increases. The Miller capacitance, which is small at this time, is discharged by the drain-source voltage swing and at the same time the gate-source voltage increases in accordance with the transfer characteristic (cf. fig. 6).
At time t_2 the drain-source voltage V_{DS} is equal to the gate-source voltage V_{GS}. At this point the greatly increased Miller capacitance comes into effect.
In the period between t_2 and t_3 the transistor operates as a Miller integrator, i.e. the gate-source voltage remains constant, whereas the gate charging current flows across the Miller capacitance and leads to a further decrease in the drain-source voltage.
At time t_3 the drain-source voltage has reached the end of the analog region of the output characteristic and the Miller capacitance has reached its maximum value. In the period between t_3 and t_4 the input capacitance C_{iss} is charged to the level of the applied drive voltage. At the same time the channel resistance is further reduced. This can be seen from the shearing of the family of curves in the resistive region of the characteristics.
At time t_4 the transistor has reached its lowest forward resistance ("on" resistance $R_{DS(on)}$ (corresponding to the residual drain-source voltage divided by the drain current).

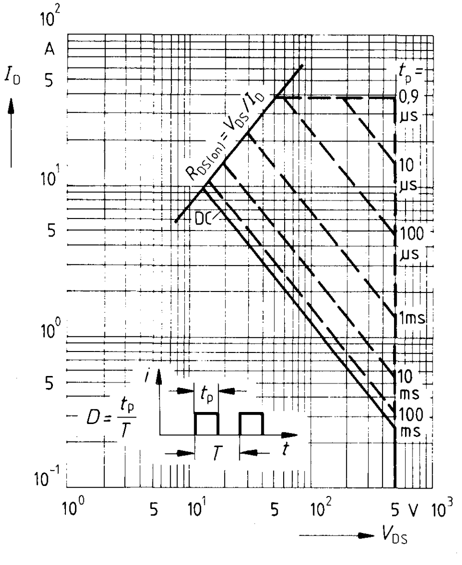
Turn-off procedure

The turn-off procedure is initiated at the time t_5 by switching off the drive voltage. The input capacitance C_{iss}, which is at maximum at this time, discharges through the internal impedance Z_i of the drive generator. The gate-source voltage decreases to a value at which the instantaneous drain current is still able to conduct in the resistive region of the characteristics.
This is reached at time t_6 when the on-resistance has slightly increased.
In the period between t_6 and t_7 the transistor again acts as a Miller integrator, i.e. the gate-source voltage remains constant, whereas the entire gate drive current flows across the still higher Miller capacitance and leads to a rise in the drain-source voltage.
At time t_7 the instantaneous gate-source voltage and the drain-source voltage are identical, i.e. the Miller capacitance falls to a low value.
In the period between t_7 and t_8 the now smaller Miller capacitance is charged in proportion to the rapidly rising drain-source voltage. At the same time the drain current decreases according to the voltage drop at the load resistance, the gate-source voltage drops as well. At the time t_8 the threshold value is reached and the transistor is completely turned off. The input capacitance is then discharged to the level of the drive voltage in the period between t_8 and t_9.

1.5 Safe operating area (SOA)

The SIPMOS transistor is an extremely rugged component because of the technology on which it is based. Its cellular structure has the effect of favorably distributing the heat dissipation in the chip, and the positive temperature coefficient of all the regions involved in conducting currents ensures that it is self-stabilizing. The source metalization forms a reliable short circuit for the base-emitter path of the parasitic bipolar transistor contained in the transistor. In this way, this bipolar transistor is prevented from being turned on and possibly causing a second breakdown under all operating conditons (except where excessive commutation of the reverse diode current occurs).
The high current handling capability of a SIPMOS transistor is especially worth mentioning. For example, a pulsed drain current four times as high as the maximum DC drain current is permissible.
This pulsed drain current may even be carried for a short time at maximum drain-source breakdown voltage (cf. fig. 9), but in this case the maximum drain-source breakdown voltage must not be exceeded, even for a short time. In addition to the maximum ratings specified in the data sheet for the DC drain current, the thermal resistance (junction cooling medium) determines the drain current actually permitted in operation.

Figure 9 SOA = Safe Operating Area taking the BUZ 45 as an example
Parameters: $D = 0{,}01$, $T_C = 25\ °C$



SOA = Safe **O**perating **Area**

1.6 SIPMOS reverse diode

Owing to the technical transistor design, a current flows through the PN junction from source to drain when the drain-source voltage is negative. This diode function is an integral element of the SIPMOS transistor and is specified in the data sheets. The forward voltage of the reverse diode is 1 ... 1.5 V. The reverse recovery time depends on the type and amounts to approx. 150 ns for 50 V types, rising to approx. 1800 ns with increasing transistor reverse voltage.
When SIPMOS transistors are used in bridge circuits with an inductive load, the reverse diode assumes the function of the necessary free-wheel diode. With reverse voltages greater than 200 V this can lead to problems owing to the relatively long reverse recovery times during commutation.

FREDFET

The FREDFET was developed in order to simplify design.
Fig. 10 shows a full bridge circuit with FREDFETs. This circuit is fully operable without additional protective components. Using special doping with heavy metal Siemens has succeeded in giving the FET reverse diode FRED characteristics without affecting other parameters of the transistor. The reverse current charge is reduced by several orders of magnitude by the super-fast reverse diode, therefore the maximum reverse current i_2 is accordingly reduced during commutation (cf. fig. 11). Consequently, the parasitic bipolar transistor can no longer turn on and overloading of T_2 is prevented at the same time.

Figure 10 Full bridge circuit with FREDFET

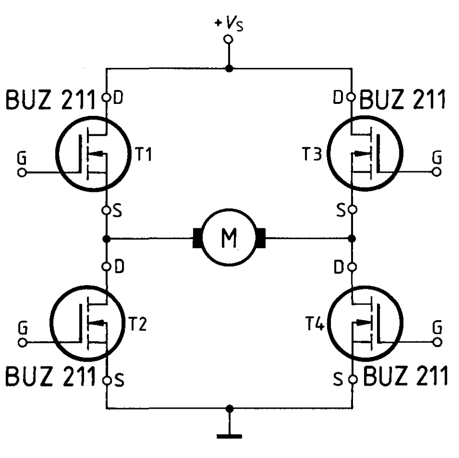
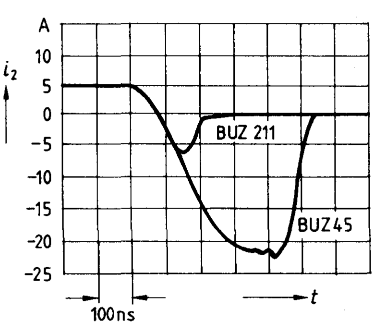


Figure 11 An example of reverse current sequence of the FREDFET BUZ 211 compared with a BUZ 45



FREDFET ≙ **F**ast-**R**ecovery-**E**pitaxial-**D**iode-**F**ield-**E**ffect-**T**ransistor

1.1 MOS handling

- The input (gate-source) must be protected against voltages at these levels:
  - small signal transistors: ± 10 V
  - power transistors: ± 20 V

  Even short-term voltages in excess of these levels can destroy transistors.
- MOSFETs have to be protected against electrostatic charges. The general handling regulations for electrostatic-discharge sensitive (ESDS) devices should be observed. This sensitivity of the devices increases with decreasing chip area and the resulting smaller input capacitance C_{iss}.
- To protect such transistors against electrostatic charge during shipping, they are packed in anti-static containers. When SIPMOS transistors are assembled, the same regulations should be observed as generally apply to MOS devices.
- In circuit design, it should be observed that the transistor is not operated with open-circuited terminals.

1.2 Use of subscripts

1.2.1 Voltages

Two subscripts are used, defining the points between which a voltage is measured. Positive potentials of the point defined by the first subscript correspond to positive values of the voltage referred to the point defined by the second subscript (reference point), e.g. V_{GS}.

1.2.2 Currents

At least one subscript is used. Positive currents that appear in the component at the point defined by the first subscript correspond to positive values of current, e.g. I_{GS}.

1.3 Absolute maximum ratings

The limits stated in the data sheets are absolute limit values. Exceeding one of these limits can lead to the destruction of the component, even if the other limits are not fully utilized. If not otherwise specified, the maximum ratings apply to 25 °C.

1.3.1 Drain-source voltage V_{DS}

Maximum permissible value of the voltage between drain and source.

1.3.2 Drain-gate voltage V_{DGR}

Maximum permissible value of the voltage between drain and gate, when bridging gate-source connections with a predefined resistance.

1.3.3 Continuous drain current I_D

Maximum permissible value of the direct current at the drain connection.

1.3.4 Pulsed drain current $I_{D\ puls}$

Maximum permissible peak value of the drain current during pulse operation as specified in the diagram "safe operating area" for a respective pulse width and duty cycle. For individual pulses higher values are permitted at a maximum transistor drive. Those values can be obtained upon request.

1.3.5 Gate-source voltage V_{GS}

Maximum permissible value of the voltage between gate and source.

1.3.6 Peak gate-source voltage $V_{GS\ (peak)}$

Maximum permitted non-repetitive peak value between gate and source.

In continuous operation the voltage should not exceed ± 10 V.

1.3.7 Maximum power dissipation P_D

Maximum permissible power dissipation of the transistor.

1.3.8 Operating temperature range T_j

The range of the permissible chip temperature, within which the transistor may be operated continuously.

1.3.9 Storage temperature range T_{stg}

The temperature range within which the transistor may be stored or transported without electrical load.

1.3.10 Maximum soldering temperature T_{sold}

The maximum permissible temperature during soldering at the terminals of the component, at a specified distance from the case and for a specified length of time. (see section 7.3).

1.3.11 Thermal resistance $R_{th\ JC}$

Thermal resistance between chip and case at thermal equilibrium.

1.3.12 Thermal resistance $R_{th\ JA}$

Thermal resistance between chip and ambient air at thermal equilibrium.

1.3.13 Thermal resistance $R_{th\ JSR}$

Thermal resistance between chip and substrate metalization reverse side at thermal equilibrium. This thermal resistance applies to SOT 23 and SOT 89 packages.

1.3.14 Isolation test voltage V_{is}

An isolation test between drain connection and base plate is carried out for the TO 238 package. Measurement is subject to a dc test voltage specified by DIN 57558 and standard climate at 23 °C and 50% relative humidity in accordance with DIN 50014, as well as short-circuited drain-source-gate connections. DIN 57558 requirements are met.

1.3.15 Humidity category

The data is specified according to DIN 40040.

1.3.16 Climatic category

The data is specified according to DIN IEC 68-1.

1.4 Electrical characteristics

The values stated under "electrical characteristics" are to be taken as typical values. In many cases, these electrical characteristics are supplemented by limit values.
The values apply to 25 °C if no other temperature is specified.

1.4.1 Drain-source breakdown voltage $V_{(BR)\ DSS}$

The voltage between the drain and source at a specified drain current; gate and source short-circuited.

1.4.2 Gate threshold voltage $V_{GS\ (th)}$ (operational voltage)

The value of the gate-source voltage at a specified drain current and at a specified drain-source voltage.

1.4.3 Zero gate voltage drain current I_{DSS}

The value of the drain current at a specified drain-source voltage and short-circuited gate-source. This value applies to 25 °C and a specified higher chip temperature.

1.4.4 Gate-source leakage current I_{GSS}

The value of the gate leakage current at a specified gate-source voltage and short-circuited drain-source.

1.4.5 Drain-source on-state resistance $R_{DS\ (on)}$

The value of the resistance between the drain and source at a specified gate-source voltage and drain current.

1.4.6 Forward transconductance g_{fs}

Ratio between the change in drain current for a given change in gate-source voltage at specified drain-source voltage and specified drain current.

1.4.7 Input capacitance C_{iss}

That capacitance measured between gate and source connections with drain-source connections short-circuited for ac voltages. The values of the dc voltage between gate-source and drain-source connections, as well as the measuring frequency are specified.

1.4.8 Output capacitance C_{oss}

That capacitance measured between the drain and source connections with the gate-source connections short-circuited for ac voltages. The values of the dc voltage between gate-source and drain-source connections, as well as the measuring frequency are specified.

1.4.9 Reverse transfer capacitance C_{rss}

That capacitance measured between drain and gate with the source connected to ground. The values of the dc voltage between gate-source and drain-source, as well as the measuring frequency are specified.

1.4.10 Turn-on time $t_{on} = t_{d\ (on)} + t_r$

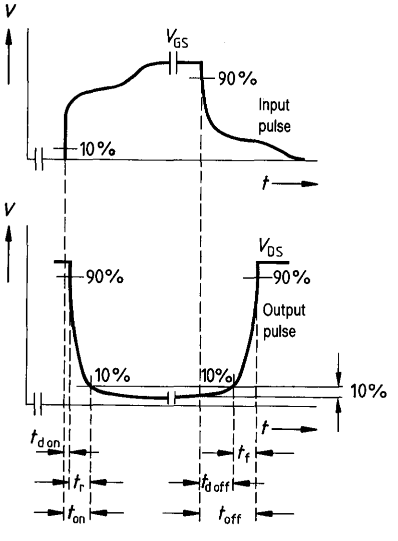
Sum of:
the turn-on delay time $t_{d\ (on)}$ measured between the 10% value of the gate-source voltage and the 90% value of the drain-source voltage, and the rise time t_r measured between the 90% value and the 10% value of the drain-source voltage.
Circuitry and parameter are specified.

1.4.11 Turn-off time $t_{off} = t_{d\,(off)} + t_f$

Sum of:

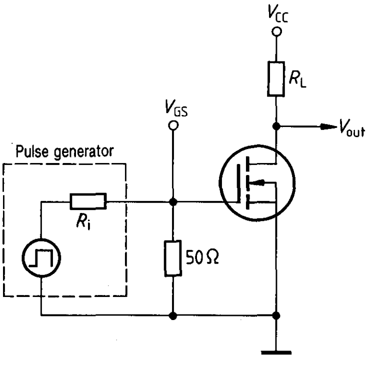
the turn-off delay time $t_{d\,(off)}$ measured between the 90 % value of the gate-source voltage and the 10 % value of the drain-source voltage, and the fall time t_f measured between the 10 % value and the 90 % value of the drain-source voltage. Circuitry and parameter are specified.

Definition of switching times



t	Time axis
$t_{d\,(off)}$	Turn-off delay time
$t_{d\,(on)}$	Turn-on delay time
t_f	Fall time
t_{on}	Turn-on time
t_{off}	Turn-off time
t_r	Rise time
V	Voltage axis
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage

Test circuit for measuring the switching time



R_L = 10 Ω power transistors (BUZ★★)
R_L = 100 Ω small signal transistors (BSS★★★)

1.5. Reverse diode characteristics

1.5.1 Continuous reverse drain current I_{DR}

Maximum permissible value of the dc forward current at specified case temperature T_C and ambient temperature T_A.

1.5.2 Pulsed reverse drain current I_{DRM}

Maximum permissible peak value of the reverse diode current for pulse operation. The duty cycle is the same as the one specified for the transistor.

1.5.3 Diode forward on-voltage V_{SD}

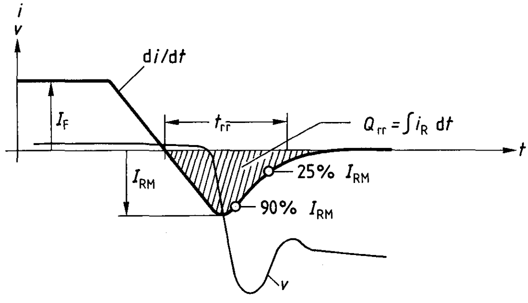
Diode forward voltage between source and drain in the on-state. The forward current I_F, the voltage V_{GS}, and the chip temperature T_j are specified.

1.5.4 Reverse recovery time t_{rr} and reverse recovery charge Q_{rr}

Respectively stated is a typical value for the test and auxiliary conditions specified in the data sheet (refer to figure according to DIN 41782). For FREDFETs[1], maximum values have been specified.

1.5.5 Repetitive peak reverse current I_{RM}

The typical value for the repetitive peak reverse current of the reverse diode is specified in the data sheets for FREDFETs.



1.6 Diagrams

1.6.1 Power dissipation $P_D = f(T)$

The maximum permitted dissipated power is given versus ambient temperature (T_A) or case temperature (T_C).

1.6.2 Typical output characteristic $I_D = f(V_{DS})$

The typical dependence of the drain current I_D on the drain-source voltage V_{DS} is plotted at a specified gate-source voltage V_{GS}. Case temperature and pulse width are also specified.

1.6.3 Safe operating area $I_D = f(V_{DS})$

The maximum permitted drain current I_D is shown versus drain-source voltage V_{DS} for loads of continuous dc current and of pulses of various widths with the specified duty cycle. The maximum permitted case temperature is specified. Within this area all values of I_D and V_{DS} are permitted, if the transistor is not thermally overloaded by these conditions. The $R_{DS\,(on)}$ limit is only attainable with gate voltages $\geq$ 10 V.

1.6.4 Typical transfer characteristic $I_D = f(V_{GS})$

The diagram shows the typical dependence of the drain-current I_D on the gate-source voltage V_{GS}, where the chip temperature T_j, the pulse width and the drain-source voltage V_{DS} are specified.

1.6.5 Typical on-state resistance $R_{DS\,(on)} = f(I_D)$

The typical on-state resistance $R_{DS\,(on)}$ is plotted, versus drain current I_D at T_C = 25 °C and at various gate-source voltages.

[1] FREDFET ≙ **F**ast-**R**ecovery-**E**pitaxial-**D**iode-**F**ield-**E**ffect-**T**ransistor. Transistors with a fast switching reverse diode.

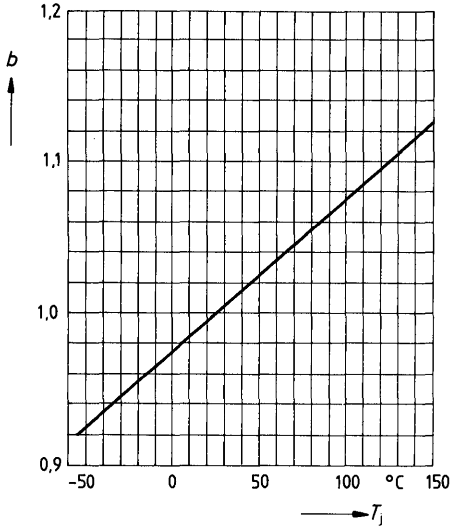
1.6.6 On-state resistance $R_{DS\,(on)} = f\,(T_j)$

The on-state resistance is shown versus chip temperature over the permitted operating range. The 98% and the 2% curves show *no* guaranteed limits, but are only empirical values and are valid for a specified dc drain current I_D at the given gate voltage V_{GS}.

1.6.7 Drain-source breakdown voltage $V_{(BR)\,DSS}$

A constant "b" is given versus chip temperature over the permitted operating temperature range, where the following mathematical relationship applies:

$V_{(BR)\,DSS}\,(T_j) = b \times V_{(BR)\,DSS}$ (25 °C). The voltage $V_{(BR)\,DSS}$ (25 °C) is the stated data sheet value.



1.6.8 Typical transconductance, $g_{fs} = f\,(I_D)$

The typical transconductance curve is shown versus drain current. The pulse width, the drain-source voltage V_{DS} and the chip temperature T_j are specified.

1.6.9 Gate threshold voltage $V_{GS\,(th)} = f\,(T_j)$

The diagram shows the spread of gate threshold voltage $V_{GS\,(th)}$ versus chip temperature T_j at the following parameters: $V_{DS} = V_{GS}$ and I_D.

1.6.10 Typical capacitances $C = f\,(V_{DS})$

The typical characteristics of the input capacitance C_{iss}, output capacitance C_{oss} and the reverse transfer capacitance C_{rss} are shown versus the drain-source voltage V_{DS} at a frequency $f = 1$ MHz and a gate-source voltage $V_{GS} = 0$ *V*.

1.6.11 Drain current $I_D = f\,(T)$

The maximum permitted dc drain current is shown versus case temperature T_C or ambient temperature T_A with a fully turned-on transistor, i.e. $V_{GS} \geq 10$ V.

1.6.12 Typical and maximum forward characteristics of the "reverse diode" $I_F = f\,(V_{SD})$

The pulsed dc current of the reverse diode I_{DR} versus reverse diode forward voltage (V_{SD}) is shown. The pulse width and the chip temperature T_j are specified.

1.6.13 Transient thermal resistance $Z_{thJC} = f\,(t)$

The diagramm shows the curve of transient thermal resistance Z_{thJC} at the specified duty cycle $D = t_p/T$ versus the load time (pulse width).

1.6.14 Typical gate-source voltage $V_{GS} = f(Q_{Gate})$

The diagram shows the typical characteristic of the required gate charge with the given gate-source and drain-source voltages in order to switch on the corresponding SIPMOS transistor to the specified current.

The gate charge comprises the charge Q_{GS} that is required to charge up the gate-source capacitance C_{GS}. During this phase – after the gate threshold voltage $V_{GS(th)}$ has been reached – the drain current increases to its specified value and the drain-source voltage then decreases. However, until this voltage V_{DS} has decreased to its residual level, the gate-drain capacitance (Miller capacitance) must be discharged. This charge portion is defined as the gate-drain charge Q_{GD}.

The charge $Q_G = Q_{GS} + Q_{GD}$ is not enough to switch the transistor fully on, because the residual voltage and the drain-source on-state resistance have not yet reached a minimum. It is only with a charge corresponding to a gate-source voltage V_{GS} of 10 V that the on-state resistance and hence the static losses are optimized. This total charge $Q_{G(tot)}$ is dependent on the drain-source voltage to be switched; the level of the drain-current to be switched has only a small influence on the total charge required.

The diagram was produced for the measurements according to the test circuit shown in para. 1.7.8 with constant current, e.g. 1.5 mA. This gives the user the possibility, according to $Q = i \times t$, of setting the charging current or the on-time as required, or of correspondingly dimensioning the drive circuit.

Example

A 100 kHz switched-mode power supply is to be switched by a BUZ 71A:

Given: Voltage $V_{DS} = 40$ V
On-time $t_{on} = 100$ ns
Frequency $f = 100$ kHz
Current $I_{D\,puls} = 18$ A
Drive voltage $V_{GS} = 10$ V

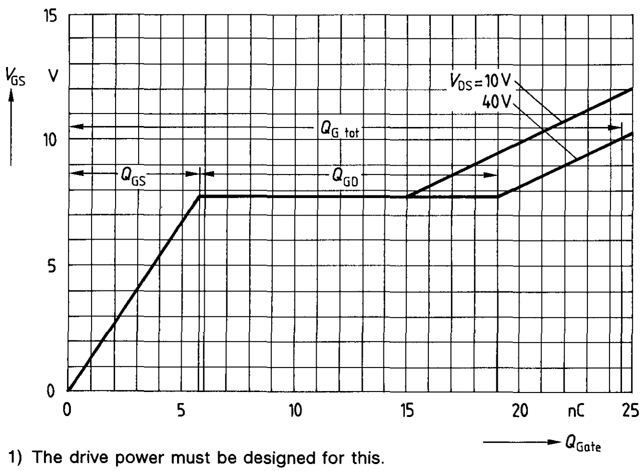
Required: Drive current I_{Drive}
Drive power P_{Drive}

1st calculation: $Q_{Gtot} = 24.5$ nC

$$I_{Drive} = \frac{24.5\text{ nC}}{100\text{ ns}} = 245\text{ mA}$$ [1]

For the turn-on process the average drive power is:

2nd calculation $P_{Drive} = Q_{Gtot} \times V_{GS} \times f$
$= 24.5\text{ nC} \times 10\text{ V} \times 100\text{ kHz}$
$= 245$ mW



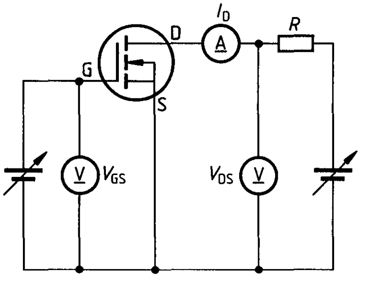
Typical gate charge in the BUZ 71A example
Parameter $I_{D\,puls} = 18$ A

1) The drive power must be designed for this.

1.7 Test circuits (according to DIN 41792, sheet 6, and IEC 147–2G)

The temperature values for the specified parameters, stated in the data sheets, are to be adhered to during the respective measurements.

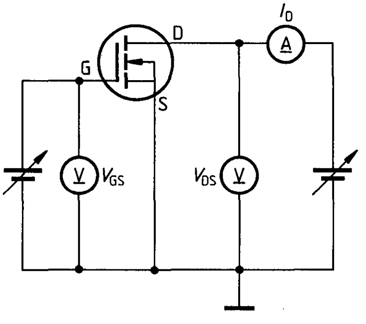
1.7.1 Drain current I_D, I_{DSS}



Basic circuit diagram for the measurement of the drain current I_D and the zero gate voltage drain current I_{DSS}.

R serves as protective resistor. The specified gate-source voltage V_{GS} is set. If V_{GS} is specified to be 0 V, gate and source must be short-circuited.

1.7.2 Drain-source on-state resistance $R_{DS\ (on)}$



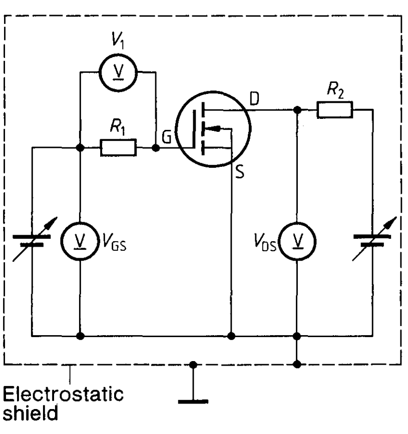
Schematic circuit diagram to measure the drain-source on-state resistance $R_{DS\ (on)}$.

Generally, the drain-source on-state resistance $R_{DS(on)}$ is measured in the saturation range. The internal resistance of the voltmeter V_{DS} must be considerably higher than the on-resistance $R_{DS\ (on)}$.

1.7.3 Gate threshold voltage $V_{GS\ (th)}$

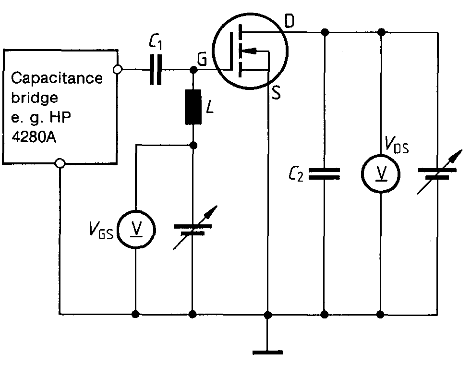
(See basic circuit diagram for measuring the drain current I_D.) The gate-source voltage, equal in value to the drain-source voltage V_{DS}, is increased slowly from zero until the specified drain current I_D is reached.

1.7.4 Gate-source leakage current I_{GSS}



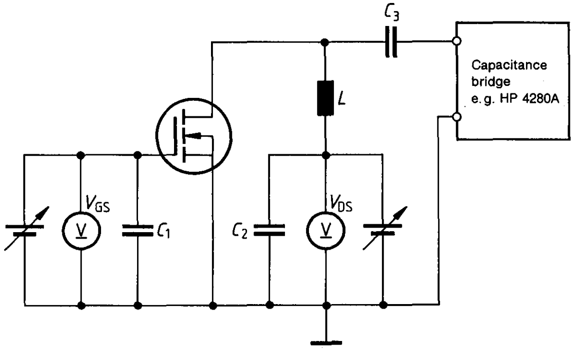
Schematic circuit diagram to measure the gate-source leakage current I_{GSS}.
R_1 and R_2 serve as protective resistors. The value of R_1 should be lower than $V_{GS}/100\ I_{GSS}$. V_1 is a very sensitive voltmeter with an internal resistance of at least 100 times the value of R_1. The leakage current is given by $I_{GSS} = V_1/R_1$. The circuit must be electrostatically shielded. Care must also be taken that measurement is not falsified by leakage currents that may be caused by the circuit layout.

1.7.5 Input capacitance C_{iss}



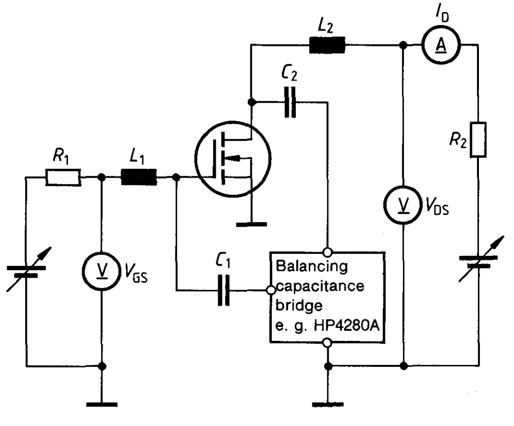
Schematic circuit diagram to measure input capacitance C_{iss} using a bridge without dc passage. The capacitors C_1 and C_2 must form a short circuit at the measuring frequency. The inductor L decouples the dc supply.

1.7.6 Output capacitance C_{oss}



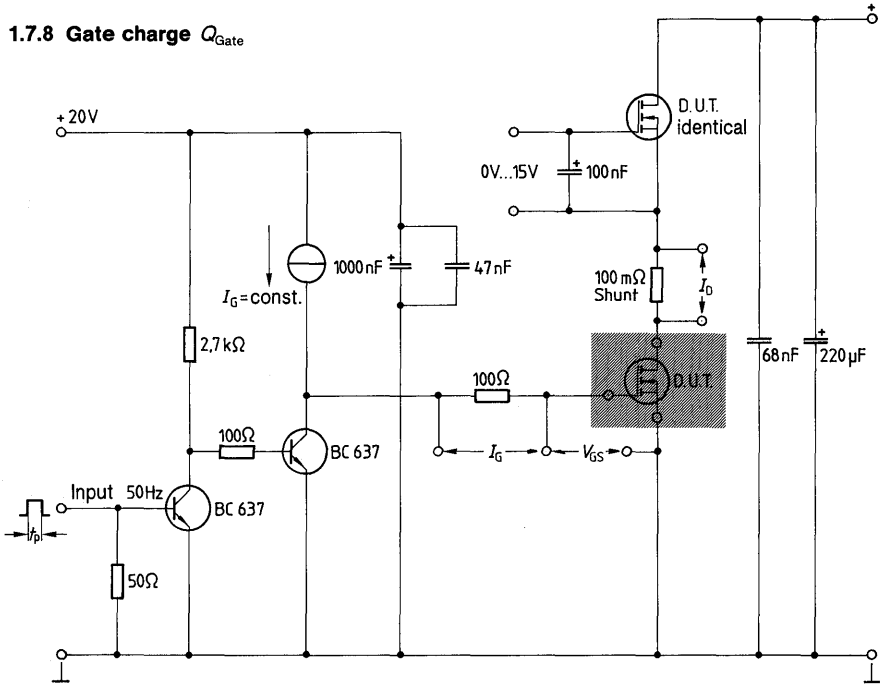
Schematic circuit diagram to measure the output capacitance C_{oss} when using a bridge without dc passage. The capacitors C_1, C_2 and C_3 must form a short circuit at the measuring frequency. The inductor L decouples the dc supply.

1.7.7 Reverse transfer capacitance C_{rss}



Schematic circuit diagram to measure the reverse transfer capacitance C_{rss} when using a bridge without dc passage. The capacitors C_1 and C_2 must form a short circuit at the measuring frequency. The inductors L_1 and L_2 decouple the dc supply.

1.7.8 Gate charge Q_{Gate}



Basic circuit diagram for the measurement of the gate charge.

1.8 Thermal resistance values

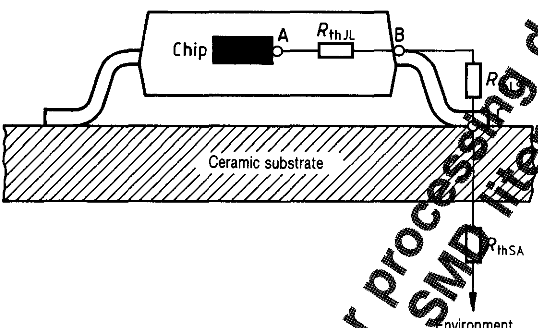
1.8.1 Small signal transistors

The heat dissipation of small signal transistors for surface mounting (SMD) depends on the material and thickness of the PC board and of the conductor paths (inherent heating), as well as on the packing density (external heating). Hence, inherent and external heating determine the junction temperature, and thus the permissible thermal stress of SMDs.
The values for thermal resistance given in the data sheets should only be used for rough estimations of the junction temperature T_j, since they were measured under certain laboratory conditions, where no regard was paid to specific applications.

Thermal resistance

The thermal resistance R_{thJA} can be calculated by:

$$R_{th\,JA} = R_{th\,JL} + R_{th\,LS} + R_{th\,SA}$$



$R_{th\,JL}$ = Thermal resistance between junction and terminals of the component

$R_{th\,LS}$ = Thermal resistance between terminals and soldering surfaces of the substrate

$R_{th\,SA}$ = Thermal resistance between substrate and environment, e.g. air or cooling area

The **internal thermal resistance** $R_{th\,JL}$ is determined by the constructional design of the component and can therefore be exactly specified, whereas the **external thermal resistance,** being the sum of $R_{th\,LS} + R_{th\,SA}$, depends on the individual application.

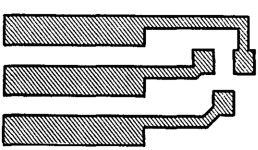
For processing details see SMD literature list

Total power dissipation

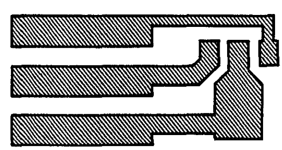
SMDs are grouped according to their max. permissible power dissipation P_D

Thermal resistance	Package SOT 23	Package SOT 89
$R_{th\,JL}$	280 K/W	20 K/W
$R_{th\,LS}$	30 K/W	15 K/W
$R_{th\,SA}$	65 K/W	90 K/W
$R_{th\,JA}$[1])	375 K/W	125 K/W

In order to achieve a reduction in the thermal resistance, the metal surface for the collector connection is enlarged. This is particularly effective with epoxy circuit boards, which have poor thermal conduction.



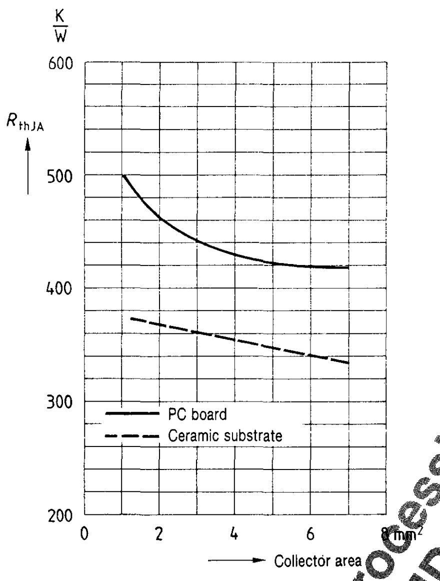
SOT 23 collector area



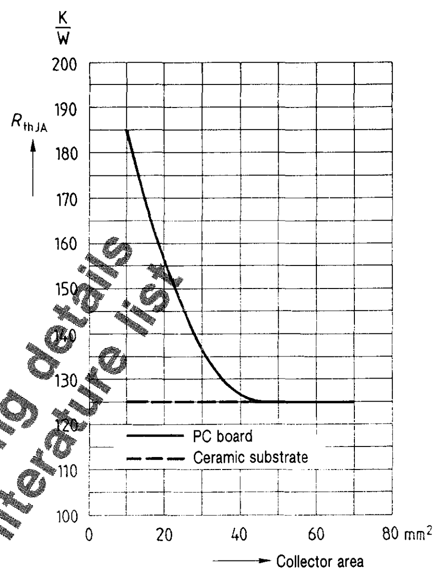
SOT 89 collector area

[1]) For each component group the data shows a typical value, which refers to a common substrate 15 mm × 16.7 mm × 0.7 mm.

Thermal resistance for package SOT 23



Thermal resistance for package SOT 89



For processing details see SMD literature list

Generally, these specifications suffice to determine the junction temperature T_j.
The determination of the junction temperature via the temperature dependence of the diode path is more exact, but is, however, extremely complicated.
Nevertheless, if it becomes necessary to determine the junction temperature T_j exactly, then the temperature T_L of the component connections has to be measured. T_j can then be calculated by:

$$T_j = T_L + R_{th\,JL} \times P_D$$

Methods for measuring the temperature at component connections

- **Measuring with thermocouple element** (e.g. Thermocoax)
  For this method a miniature coated thermocouple element with low thermal capacitance is used. The element, which is coated with a heat-conducting paste, is pressed against the connection with the collector. There is hardly any influence on the device under measurement and deviations do not exceed a few percent.

- **Measuring with temperature indicators** (e.g. thermopaper)
  Temperature indicators do not cause heat dissipation and thus allow an almost exact determination of temperature. A certain number of deviations can only result from the rough grade indication of the temperature indicators. This method is quite easy and provides sufficient accuracy. It is particularly suitable for measurement on PC boards.

1.8.2 Power transistors

For better thermal conductivity the power transistors are mounted on heatsinks. The thermal resistance of the chip through the heat sink to the ambient air is to be calculated. The following approximation formula applies:

$R_{th\,JA} = R_{th\,JC} + R_{th\,CA}$

The thermal resistance of the heat sink $R_{th\,CA}$ is calculated according to the following approximative equation (flat plate cooling fins – not applicable for heat sink with profile):

$$R_{th\,CA} = \frac{3{,}3}{\sqrt{\lambda\,d}}\,C^{\,0{,}25} + \frac{650}{A}\,C$$

d thickness of the heat sink in mm
A area of the heat sink in cm^2
C correction factor for position and surface of heat sink

Thermal conductance λ of the heat sink

Material	Thermal conductance λ
Aluminum	2.1 W/K cm
Copper	3.8 W/K cm
Brass	1.1 W/K cm
Steel	0.46 W/K cm

Correction factor

Position	Surface shiny	blackened
vertical	0.85	0.43
horizontal	1	0.5

This formula applies to approximately square-shaped heat sinks if the transistor, mounted in the center of the heat sink, represents the only heat source on that heat sink. The values of the constants and correction factor hold true in static air up to an ambient temperature of approx. 45 °C, if no heat radiating components are in the vicinity.

Thermal resistance R_{th} of a mica washer

Case	Thickness of the dry washer 50 µm	75 µm	Washer, greased on both sides, reduces the resistance by:
TO 202	8.0 K/W	10.0 K/W	4.0 K/W
TO 204 (TO 3)	1.25 K/W	1.5 K/W	0.9 K/W
TO 218 (TOP 3)	1.5 K/W	2.0 K/W	0.8 K/W
TO 220	1.5 K/W	2.0 K/W	0.8 K/W

Insulating washers produce better thermal resistance than do mica washers.

AQL values and definitions of defectives

Explanations

AQL (acceptable quality level) agreements specify the sampling conditions for the incoming inspection of consignments (conformance test). AQL values in conjunction with the standard sampling inspection plans determine the acceptance or rejection of delivery lots. The size and maximum permissible number of defectives is based on DIN 40 080 (identical with MIL Standard 105 D and IEC 410), single sampling plan for normal inspection, inspection level II. The sampling instructions of this standard are such that a delivery lot will most probably be accepted (> 90%) if the defect percentage is equal to or less than the specified AQL value. Generally, the average defect percentage of the products we deliver is far below the AQL value.

Definitions of defectives

A component is considered defective if it does not comply with the characteristics specified in the data sheet or in an agreed upon delivery specification. Defectives can be divided into inoperatives, which generally exclude a functional application of the component, and defectives of less significance.

Inoperatives are:

- open or short circuit,
- broken component, package, terminals or encapsulation,
- missing or incorrect marking,
- incorrect identification of terminals,
- intermixing with other component types,
- alternating orientation in a packaging tube or tape.

The remaining defectives can be divided into:

- electrical defectives (maximum ratings exceeded),
- mechanical defectives, e.g. dimensions not adhered to, package damaged, illegible marking, bent leads.

Grouping into major defects and minor defects according to DIN 40 080 has been purposely avoided here because these terms are defined primarily on the basis of applications and not specifications. In contrast to this the defective classes that we use – for which AQL values are given below – are clearly outlined by the specification and the mentioned inoperatives.

AQL values

The AQL values valid for the different product families are comprised in the following table:

Defectives	AQL values
Inoperatives (mechanical and electrical)	0.1
Σ electrical defectives	0.4
Σ mechanical defectives	0.4

Incoming inspection

If the user wants to carry out an incoming inspection, the use of a sampling inspection plan is recommended. The test method that is applied must be agreed upon between the user and the supplier.

AQL = Acceptable Quality Level.

The following information is necessary for judging any claims that may arise: test circuit, sample size, number of defective items found, sample of evidence, packing list.

Sampling plan for normal inspection
in accordance with DIN 40080 or ABC-Std. 105 D, inspection level II

Lot size	Sample size	AQL value										
		0,065	0,10	0,15	0,25	0,40	0,65	1,0	1,5	2,5	4,0	6,5
		A R	A R	A R	A R	A R	A R	A R	A R	A R	A R	A R
2 to 8	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1
9 to 15	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑
16 to 25	5	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓
26 to 50	8	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2
51 to 90	13	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3
91 to 150	20	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4
151 to 280	32	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6
281 to 500	50	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8
501 to 1200	80	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11
1201 to 3200	125	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15
3201 to 10000	200	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22
10001 to 35000	315	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑
35001 to 150000	500	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑
150001 to 500000	800	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑
500001 and more	1250	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑

A ≙ Acceptance number, i.e. maximum number of defectives in a sample up to which a lot is accepted.
R ± Rejection number, i.e. the number of defectives which must be found in a sample as a minimum for rejection of the lot.

Other conditions
As the combination "Acceptance 0/Rejection 1" is not particularly clear, the next largest sample should be taken.

Additional information
Stating AQL values is no assurance of characteristics in a legal sense. The agreement of sampling inspections and AQL values does not prevent the customer from carrying out more extensive tests in incoming inspection and claiming replacements for individual defective components under the terms of sale. Any further liability, especially as regards the consequences of component defects, cannot be recognized.

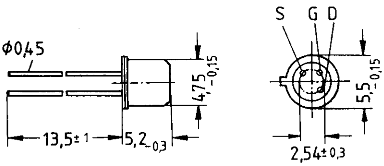
Note: Siemens is prepared to make agreements on PPM values with large-scale customers.

Package Outlines
Mounting Instructions

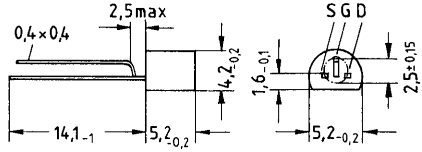
Package Outlines

Small signal transistors

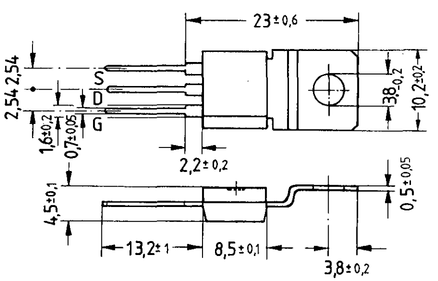
TO 18



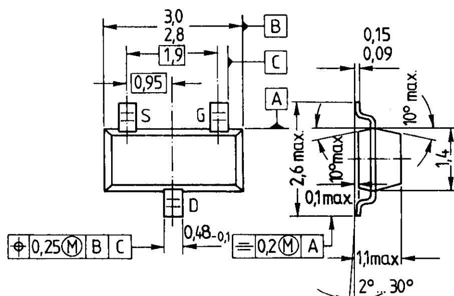
TO 92



TO 202



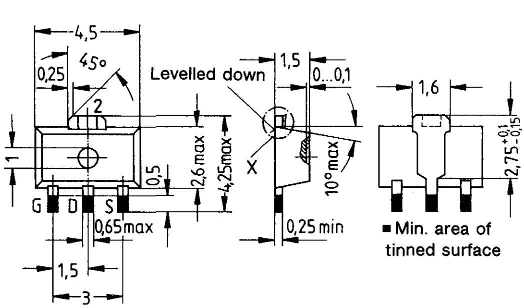
SOT 23



For CAD workstations applies:

Length	Width	Height
2,9 ± 0,1	1,3 ± 0,1	1,1

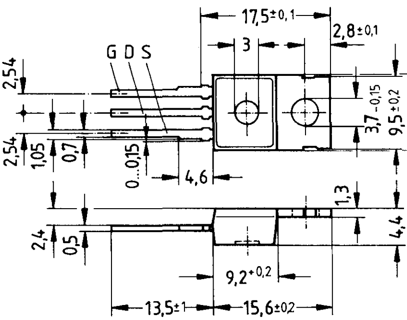
SOT 89



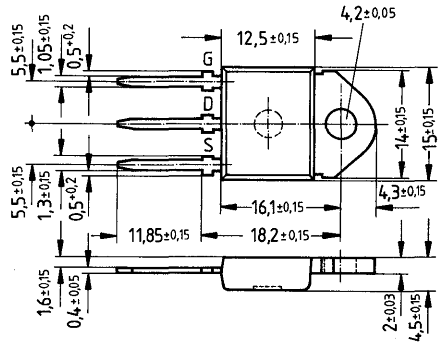
Dimensions in mm

Power transistors

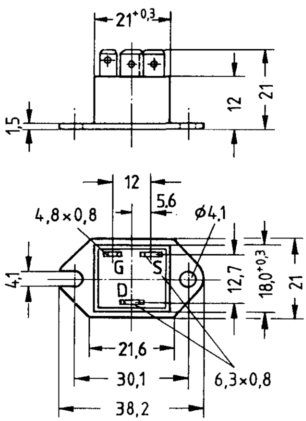
TO 220



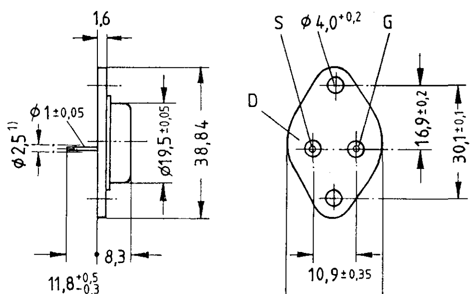
TO 218



TO 238



TO 3



1) Max. bending area

Dimensions in mm

1. Small signal transistors

In contrast to leaded SIPMOS small signal transistors two delivery methods can be used for SMDs:

- bulk
- tape

1.1 Bulk

The simplest and least expensive form of delivery of small signal transistors for surface mounting is in bulk. In contrast to leaded components the method of packaging permits use with automatic machines, because the terminals cannot bend or interlock. With the use of suitable equipment, the components are brought to the assembly machine in the correct position. With this type of packing a large quantity of components can be placed ready at the machine if required. The feeding of the components can take place in-line, without any interruption of the assembly process.

1.1.1 Bulk packaging quantities

Type	Quantity	Mode of delivery
BSS 84 BSS 87 BSS 123 BSS 131 BSS 138	2000 pieces	antistatic container

1.2 Tape (according to DIN IEC 286-3)

A frequently used form of packaging for SMDs is tape packaging. The major benefit of the tape method is that it permits non-interchangeable keeping and meets the requirements of most assembly machines. Cardboard and blister tapes are available tape forms.

The blister tape has preformed compartments corresponding to the component size, which are covered with fixing tape. Blister tapes consist either of plastic material or of plastic-clad aluminum foil. The advantages of the aluminum foil are i.a. its high dimensional stability and its protection against electrostatic charge. For this reason we only use aluminum tapes for packaging our discrete semiconductors.

The tapes are standardized worldwide according to DIN IEC 286-3. It is therefore ensured that the tapes may be used on all automatic machines. At present the tape width is mainly 8 or 12 mm. Other tape widths are currently being prepared.

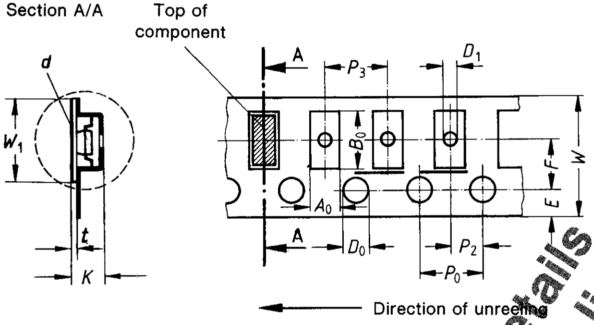
- **8 mm tape** for package SOT 23
- **12 mm tape** for package SOT 89

1.2.1 Tape packaging units

Reel dimension	Package SOT 23	SOT 89
18 cm	3 000 pieces	1 000 pieces
33 cm	10 000 pieces	2 500 pieces

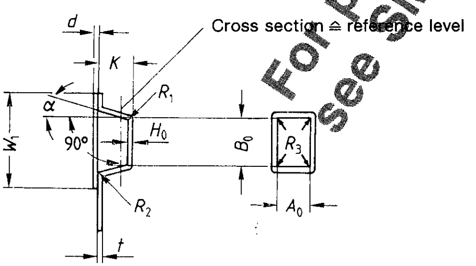
For processing details see SMD literature list

1.2.2 Blister tape



For processing details
see SMD literature list

Component compartment



1.2.3 Table of dimensions for blister tapes

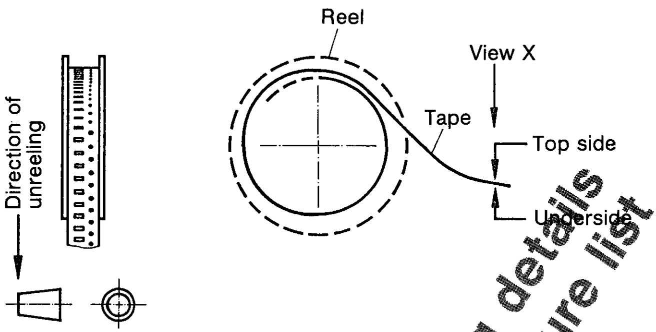
The table contains only dimensions which are important for taping the components.

Designation	Symbol	Dimensions (mm)		Notes
		SOT 23	SOT 89	
Tape width	W	8 ± 0.3	12 ± 0.3	–
Carrier tape thickness	t	0.3 max	0.3 max	–
Pitch of sprocket holes	P_0	4 ± 0.1	4 ± 0.1	Cumulative pitch error + 0.2 mm/10 pitches
Diameter of sprocket holes	D_0	1.5 + 0.2	1.5 + 0.1	–
Distance of sprocket holes	E	1.75 ± 0.1	1.75 ± 0.1	–
Distance of components	F	3.5 ± 0.05	5.5 ± 0.05	Center hole to center compartment
	P_2	2 ± 0.05	2 ± 0.05	
Distance compartment to compartment	P_3	4	8	Every two pitches (SOT 89)
Compartment	K	2.5 max	4.5 max	Exact dimensions are given with component dimensions
	α	15° max	15° max	
	R_1, R_2	0.5 max	0.5 max	
	H_0	$0.3^{+0.1}_{-0.05}$	$0.3^{+0.1}_{-0.05}$	Between inner side of the compartment bottom and the reference level for measuring A_0, B_0
	A_0 B_0	The tolerances are chosen such that the components can change their orientation only within permissible tolerances, but can easily be removed from the tape.		
Hole in compartment	D_1	1 + 0.2	1.5 + 0.2	Tolerance to the center of the sprocket hole: ± 0.1 mm
Width of fixing tape	W_1 d	5.5 typ 0.1 max	9.5 typ 0.1 max	The fixing tape shall not cover the sprocket holes, nor protrude beyond the carrier tape so that the max. tape width will not be exceeded.
Max. device tilt in compartment	–	15° max	15° max	
Minimum bending radius	R	25 min	25 min	Minimum bending radius of tape

For processing details see SMD literature list

1.2.4 Polarity and orientation of taped components

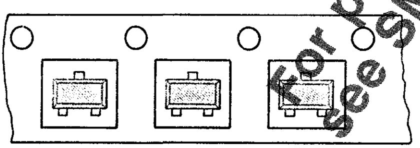
All polarized components are oriented in one direction. The mounting side is oriented to the underside of the component compartment. The underside is defined as the invisible side of the tape.



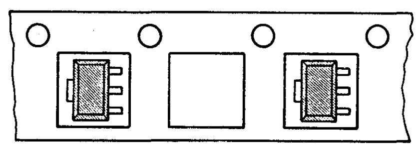
For processing details see SMD literature list

View X (Top side)

SOT 23 package



SOT 89 package



1.2.5 Fixing of components

Components are prevented from falling out of the component compartment by a transparent fixing tape.

1.2.6 Storage of tapes

A storage temperature of 40 + 5 °C at a relative humidity of ≤95 % is permissible up to a maximum of 240 h.

1.2.7 Break force of tape

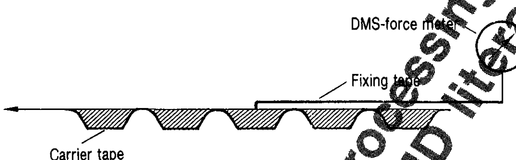
The maximum break force of the tape in the direction of unreeling is ≥ 10 N.

1.2.8 Peel force of fixing tape

During peel-off the angle between the fixing tape and the direction of unreeling is 180 °C. The peel force of the fixing tape ranges from 0.2 N to 1.0 N.

1.2.9 Break force of fixing tape

The minimum break force of the fixing tape is 10 N.



For processing details see SMD literature list

1.2.10 Peel speed of fixing tape

The fixing tape can be peeled off at a rate of 5 mm/s to 20 mm/s.

1.2.11 Reel packaging

Component tapes are wound onto reels as shown in the illustration below and are then suitable for automatic assembly.
Currently available:

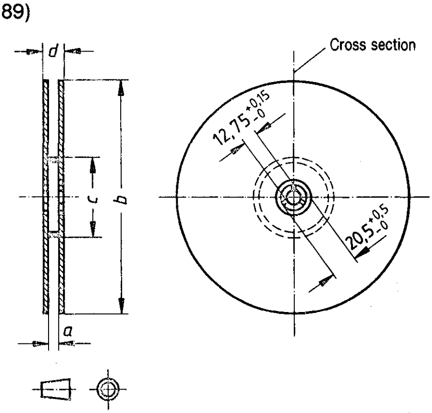
- Tape width = 8 mm (SOT 23) and 12 mm (SOT 89)
- Reel size = 18 cm and 33 cm

The reels are delivered in a protective wrapping.

Reel dimensions (mm)

Dimension	SOT 23	SOT 89	SOT 23	SOT 89
a	8,4 + 1,5	12,4 + 1,5	8,4 + 1,5	12,4 + 1,5
b	180 max	180 max	330 max	330 max
c	60 min	60 min	100 min	100 min
d	14,4 max	18,4 max	14,4 max	18,4 max

Dimensions in mm



1.2.12 Reel labeling

Each reel is labeled with manufacturer, type, series number, and date.

1.2.13 Missing components

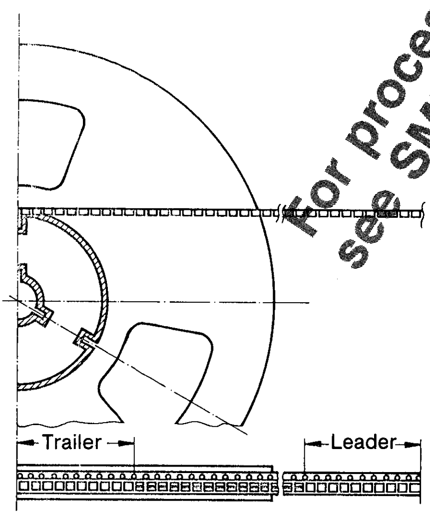
A maximum of two consecutive components may be missing, provided that this gap is followed by six components. The number of empty places shall not exceed 0.25 % of the total number of components per reel. Other agreements are possible upon request.

1.2.14 Leader and trailer

Carrier tape with fixing tape, without components.

Tape leader	**Tape trailer**
min. 400 mm (100 pitches)	min. 300 mm (75 pitches)

For processing details see SMD literature list



1.2.15 ESD

SMDs are delivered in tape protected from static. Care should be taken in processing that the tape reel is electrically connected to the automatic assembly machine and that the machine is grounded. This tape procedure conforms to the standard IEC/T 640.

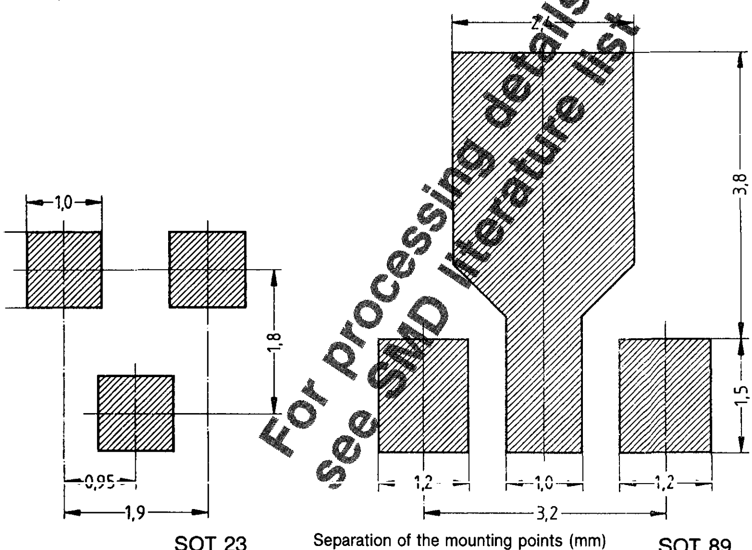
ESD ≙ **E**lectrostatically **S**ensitive **D**evices

1.3 PCB layout

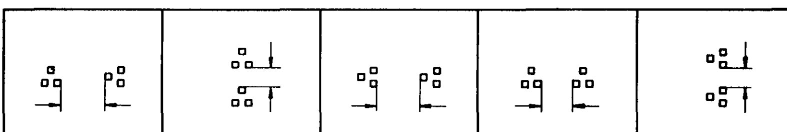
When using surface mounted devices, the PCB layout has to be accommodated to this new technology. This demand should be fulfilled not only to better utilize the packing density but also to meet the requirements resulting from the new placement and processing system. Some factors influencing the PCB layout are:

- Distance between conductor paths
- Component tolerances
- Distance between components
- Misalignment of component and conductor path

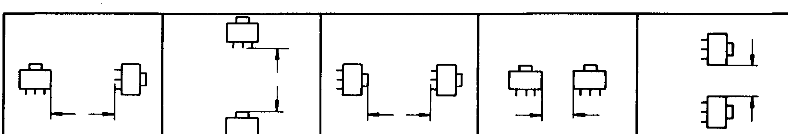
Recommended minimum solder pad dimensions (mm)



Separation of the mounting points (mm)
Direction of solder wave



SOT 23	1,5	0,6	1,5	1	0,6



SOT 89	2	2	2	1	1

2 Power transistors

2.1 Mounting instructions

The transistors may be mounted in any position.
If it is necessary to bend the leads, this should be done in a bending device. If it is necessary to bend the leads by hand, the lead must be held with pliers between the bending point and the header. Please avoid notches and repeated bending of the leads. For insulated mounting of transistors in the cases TO 202, TO 204, TO 218, TO 220, note the increased thermal resistance between transistor and heat sink.

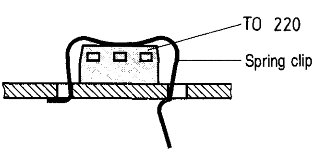
Mounting parts

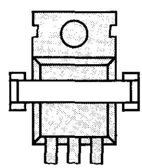
The mounting parts shown in the following are not covered by the Components Group's product line. Please contact the respective manufacturers.

2.1.1 Mounting procedures

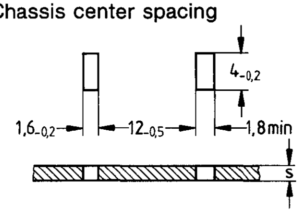
Plastic package TO 220

Non-insulated construction with spring clip



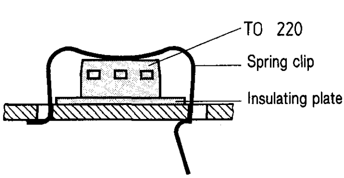


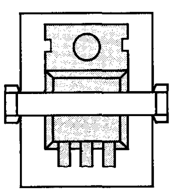
Chassis center spacing



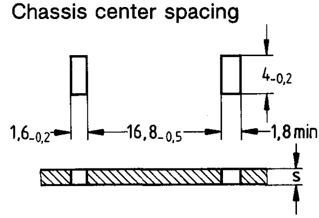
Chassis thickness s = 1 to 2 mm
Contact pressure F = 100 to 250 N

Insulated construction with spring clip





Chassis center spacing

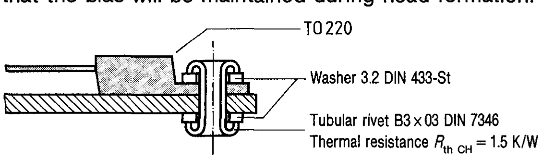


Chassis thickness s = 1 to 2.5 mm
Contact pressure F = 100 to 250 N

Dimensions in mm

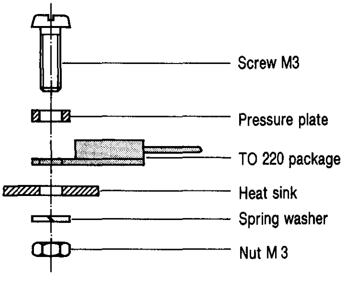
Non-insulated construction with rivets

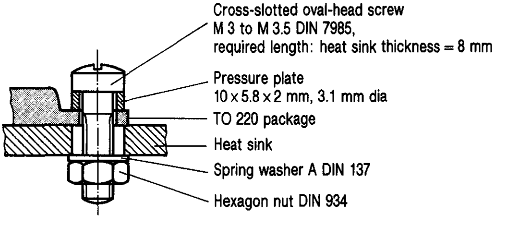
The prefabricated rivet head must always be located at the terminal side, and at least one planar washer (in accordance with DIN 433) has to be provided at the snaphead side as well as one at the heat sink side. During riveting, it has to be observed that the parts will not be deformed and that the bias will be maintained during head formation.



Non-insulated construction by screw mounting

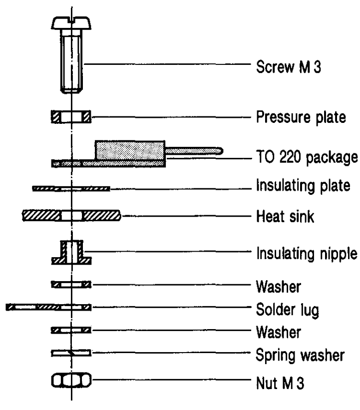
- Heat sinks or mounting plates made of aluminum must have a thickness of at least 2 mm; with copper the minimum value is 1.2 mm. Smaller thickness will cause heat sink deformation which is impermissible for the heat transition.
- The mounting hole in the mounting plate has to be leveled down; the maximum diameter is 3.7 mm. Countersinking may not show a diameter larger than 4 mm.
- The screw head should not be located directly on the terminal, but over the pressure plate to distribute the force properly.
- The nut must always be at the mounting plate side and should be secured by a spring washer (DIN 137).
- Screw tools must not touch the plastic package. Therefore, cross-slotted screws are preferred.
- The recommended mounting torque for M 3 and M 3.5 screws is 60 Ncm with the screw material 5.8. This results in a mounting force of max. 1600 N.
  Compared with 60 Ncm, applying a max. torque of 80 Ncm to such screws will not improve the thermal contact resistance to a large extent.

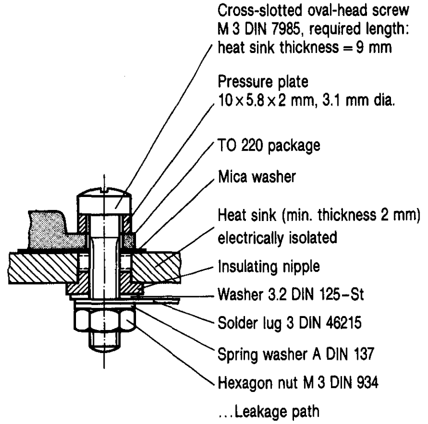




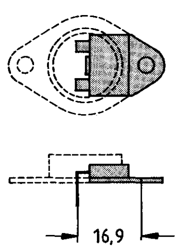
Insulated construction by screw mounting

- This construction permits a maximum leakage path of 1.0 mm. That corresponds to insulation group Ao according to VDE 0110 for 250 V ac (rms).
- The hole diameter in the heat sink may be between 3.8 mm and 5.5 mm. The hole has to be leveled down.
- With the maximum diameter, the contact surface must be flat up to the hole edge.
- During assembly, particularly when passing the screw through the mica washer, it has to be observed that this mica washer will not be damaged.
- Screw tools must not touch the plastic package; therefore, cross-slotted screws are preferred.
- The mounting torque should not exceed 60 Ncm with the insulated construction.

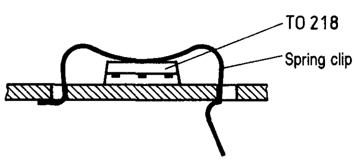


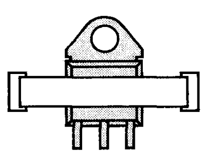


Plastic package TO 218 (TOP 3)
Screw mounting of a TO 218 package instead of a metal case TO 3

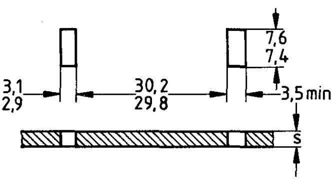


Non-insulated construction with spring clip





Chassis center spacing

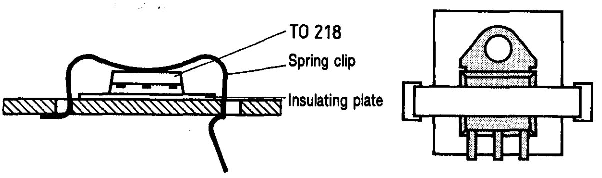


Chassis thickness s = 1,9 to 2,1 mm
Contact pressure F = 100 to 250 N

Dimensions in mm

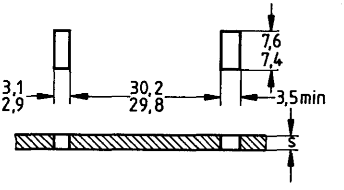
Mounting Instructions

Insulated construction with spring clip



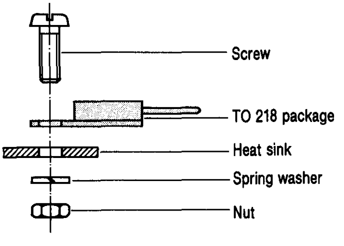
Chassis thickness $s =$ 1,9 to 2,1 mm
Contact pressure $F =$ 100 to 250 N

Chassis center spacing

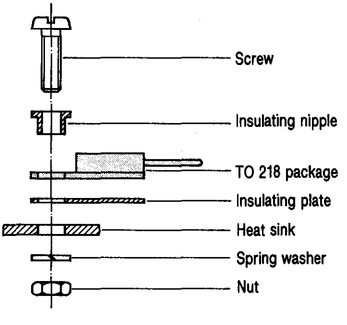


Dimensions in mm

Non-insulated construction by screw mounting

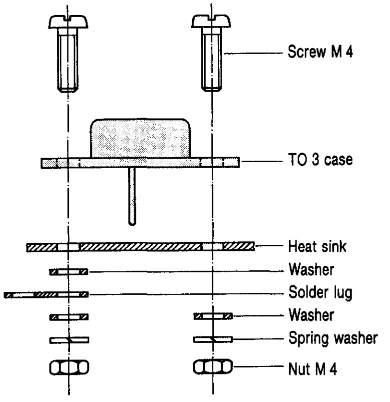


Insulated construction by screw mounting

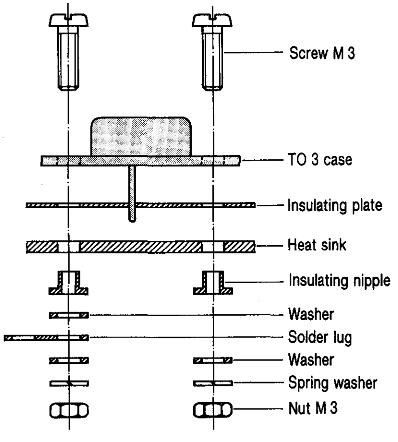


Metal case TO 3

Non-insulated construction by screw mounting

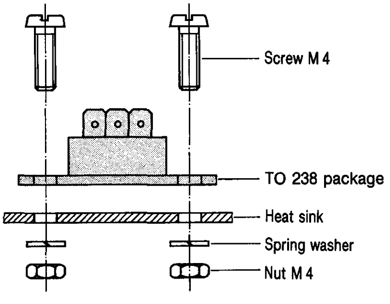


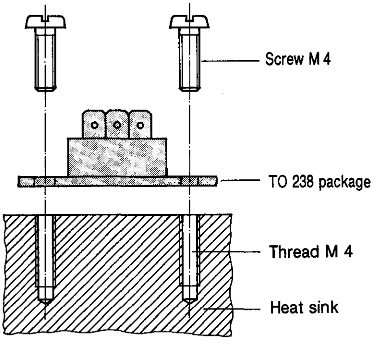
Insulated construction by screw mounting



Plastic package TO 238 (insulated version)

Directly insulated construction (to base plate)





1. Soldering instructions

Every semiconductor is extremely sensitive to the exceeding of its maximum permissible chip temperature. When soldering semiconductors, care must be taken that the components will not be thermally overloaded. The chip temperature may not exceed 200 °C during soldering (max. 1 minute). The leads must not be subject to high mechanical stress during soldering.
The requirements of the solderability tests according to DIN IEC 68-2-20 are satisfied.

1.1 Small signal transistors

1.1.1 Soldering data for the plastic packages TO 202, TO 92

Soldering temperature	Lead length 0.5 mm	Lead length 1.5 mm	Lead length 5 mm
245 °C	4.0 s	5.0 s	10.0 s
260 °C	3.0 s	5.0 s	5.0 s
300 °C[1])	2.5 s	3.0 s	5.0 s

For processing details see SMD literature list

1.1.2 Soldering data for the metal cases TO 18

Soldering temperature	Lead length 0.5 mm	Lead length 1.5 mm	Lead length 5 mm
245 °C	5.0 s	6.0 s	13.0 s
260 °C	3.5 s	4.0 s	10.0 s
300 °C[1])	3.0 s	3.5 s	8.0 s

1.1.3 Surface mounted devices (SMD) SOT 23, SOT 89

Small signal transistors SOT 23 and SOT 89 packages are intended for surface mounting. The following soldering instructions apply to substrates with conductor paths and resistors having an Sn-Pb surface. During soldering, the substrate may not be subjected to high mechanical stress caused by temperature, temperature cycles, or fixing parts.

SMD = Surface Mounted Device

1.1.3.1 Glueing

SMDs must be fixed to the PCB with adhesive before the solder process. The adhesive must fulfil many criteria, such as:

- Adequate bonding
- Short hardening time and low hardening temperature
- Uniform viscosity to ensure easy coating
- No chemical reactions upon hardening in order not to deteriorate component and PC board
- Straightforward exchange of components in case of repair
- Non-toxic, if possible, odorless and solvent-free
- Good thermal conductivity

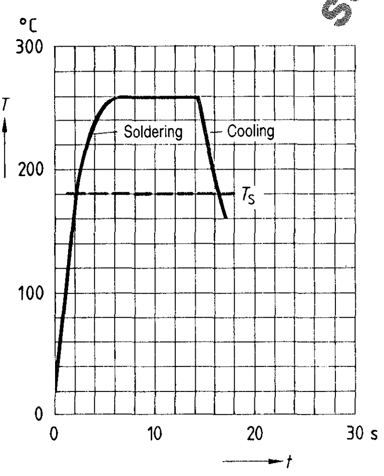
1.1.3.2 Soldering technology

Soldering technology plays a significant role, as good electrical joints are required without the occurrence of short circuits. The choice of the soldering method largely depends on the design of the PC board (single, double-clad, multilayer board etc.), on the supplied components and the production facilities.
In addition to hand soldering, which should only be used for repair purposes, there are mechanical soldering methods such as bath soldering (wave, drag and dip baths) and reflow soldering.

Wave soldering

Wave soldering is the soldering method which is at present applied in most cases. With a maximum bath temperature of 260 °C the soldering time should not exceed 8 s.
The flux is applied in front of the wave with a fluxer.

Max. perm. SMD temperature stress
(soldering without preheating)



T_s = Melting point of the solder

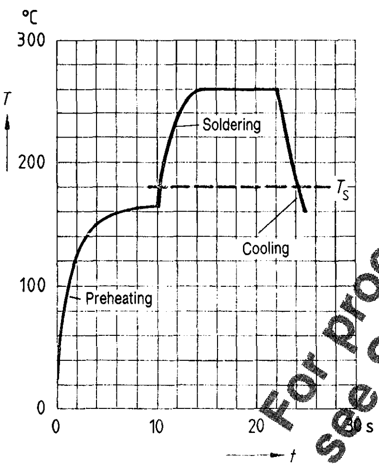
For processing details
see SMD literature list

Reflow soldering

For reflow soldering the required quantity of solder for the connection is applied to the mounting pad e.g. in the form of solder paste. After the SMD has been placed, the connection is made by one of the following methods:

- Vapor phase soldering
- Hot gas soldering
- Heated collet soldering
- Infrared soldering

Max. perm. SMD temperature stress (soldering with preheating)



For processing details see SMD literature list

Iron soldering

Soldering with a temperature controlled miniature soldering iron should only be undertaken in exceptional cases (repair), as it is not only uneconomic, but also involves the danger of damaging the component and the circuit board.

1.1.3.3 Soldering flux

- The soldering flux used for wave soldering is not subject to changes, i.e. use of collophony (F-SW 32 in acc. with DIN 8511).
- If solder pastes are used, however, most of them contain aggressive fluxes, the residues of which must absolutely be removed by cleaning.

1.1.3.4 PCB cleaning

- Cleaning in solvents is permitted at approx. 70 °C to 80 °C for about 15 seconds. Detailed information is available upon request.
- Ultrasonic cleaning (double half-wave operation)
  Ultrasonic cleaning is less advisable; should it, however, be used, the following has to be taken into account:

Cleaning agent:	Isopropanol, Freon
Bath temperature:	approx. 30 °C
Duration of cleaning:	max. 30 s
Ultrasonic frequency:	40 kHz
Ultrasonic changing pressure:	approx. 0.5 bar

1.2 Power transistors

1.2.1 Soldering data for the metal case TO 204 (TO 3)

Soldering temperature	Lead length 2 mm	Lead length 5 mm
245 °C	15 s	20 s
260 °C	12 s	15 s
300 °C[1])	10 s	15 s

1.2.2 Soldering data for the plastic packages TO 202, TO 218, TO 220

Soldering temperature	Lead length 1.6 mm	Lead length 5 mm
245 °C	7 s	10 s
260 °C	7 s	7 s
300 °C[1])	4 s	7 s

1.3 Maintenance

As they are electrical components without moveable parts, transistors are generally maintenance-free. The insulation path, however, is neither protected against splashing and dripping, nor against dust. In order that the insulation and the heat dissipation of the transistors will not be impeded, transistors and heat sinks should be cleaned from time to time.

[1]) The values apply to iron soldering. The lead length is measured from the soldering point.

For processing details see SMD literature list

Small Signal Transistors

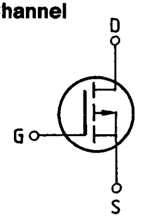
BSS 84 . . .
BSS 100

BSS 101 . . .
BSS 138

Main ratings

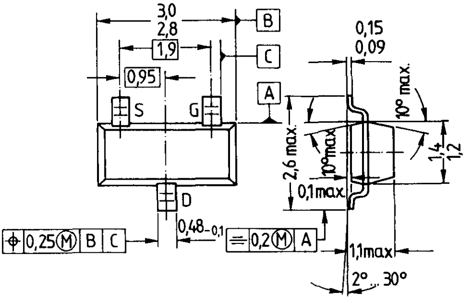
Drain-source voltage V_{DS} = **–50 V**
Continuous drain current I_D = **–130 mA**
Drain-source on-resistance $R_{DS(on)}$ = **10 Ω**

P-Channel



Description SIPMOS, P-channel, enhancement mode
Case Plastic package 23 A 3 in accordance with DIN 41 869 or SOT 23 in accordance with JEDEC.
Approx. weight 0,02 g

Type	Marking	Ordering code for versions in bulk	Ordering code for version on 8 mm tape
BSS 84	SP	Q62702-S393	Q62702-S568



Dimensions in mm

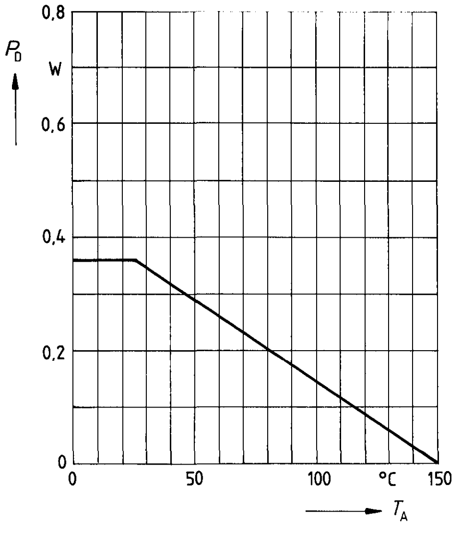
Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	–50	V	
Drain-gate voltage	V_{DGR}	–50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	–130	mA	T_A = 55 °C
Pulsed drain current	I_{Dpuls}	–520	mA	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	0,36	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 … +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\,JA}$	≤350	K/W	
Chip-substrate reverse side for package mounted on alumina 15 mm × 16.7 mm × 0.7 mm	$R_{th\,JSR}$	≤285	K/W	

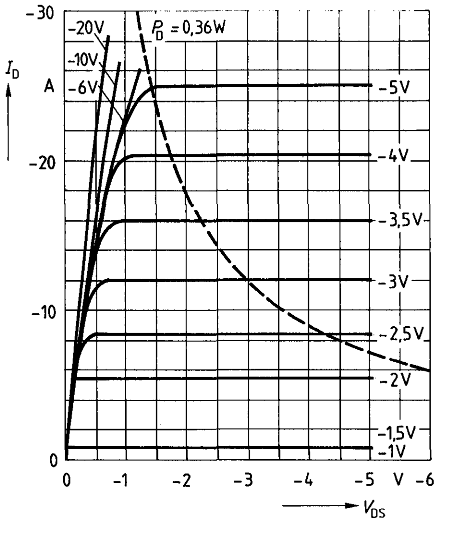
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	−50	–	–	V	V_{GS} = 0V I_D = −0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	−0,8	−1,5	−2,0		V_{DS} = V_{GS} I_D = −1mA
Zero gate voltage drain current	I_{DSS}	– –	−1 −2	−15 −60	µA	T_j = 25 °C T_j = 125 °C V_{DS} = − 50V V_{GS} = 0V
		–	–	−100	nA	T_j = 25 °C V_{DS} = −25V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	−1	−10	nA	V_{GS} = −20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	6	10	Ω	V_{GS} = − 5V I_D = −100mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,05	0,07	–	S	V_{DS} = − 25V I_D = −100mA
Input capacitance	C_{iss}	–	40	–	pF	V_{GS} = 0V V_{DS} = −25V f = 1MHz
Output capacitance	C_{oss}	–	15	–		
Reverse transfer capacitance	C_{rss}	–	6	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = −30V I_D = − 0,27A V_{GS} = − 5V R_{GS} = 50Ω
	t_r	–	10	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	18	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	−0,13	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	−0,52		
Diode forward on-voltage	V_{SD}	–	−1	−1,2	V	I_F = −0,26A V_{GS} = 0V

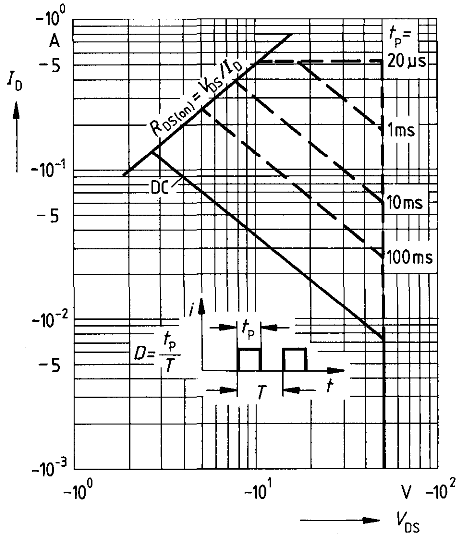
Power dissipation $P_D = f(T_A)$



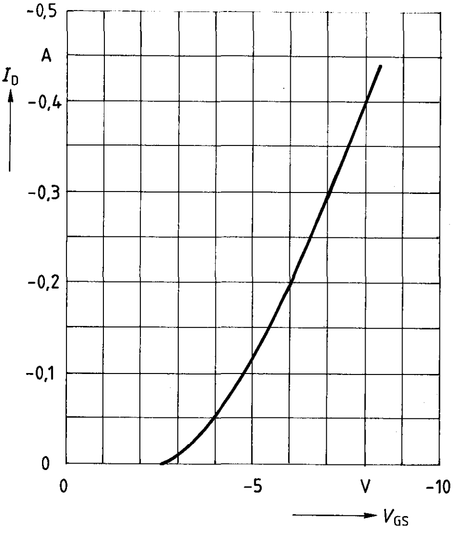
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25$ °C



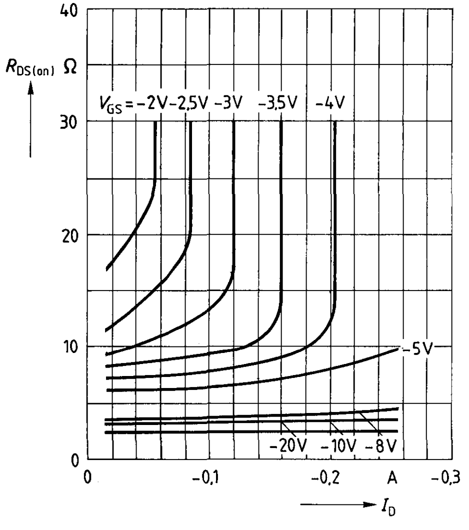
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25$ °C



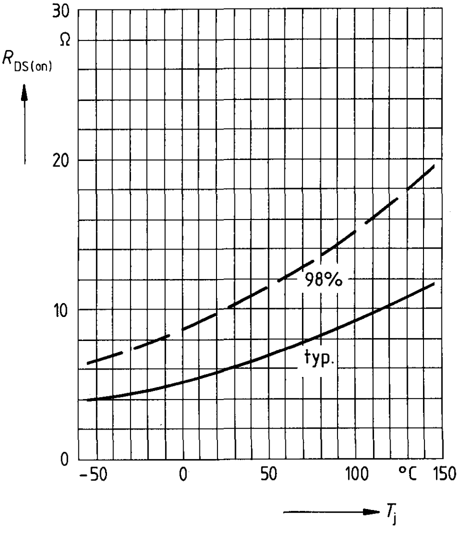
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = -25$V, $T_j = 25$ °C



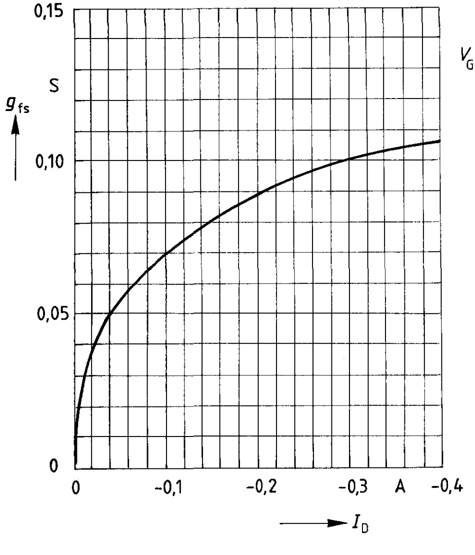
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



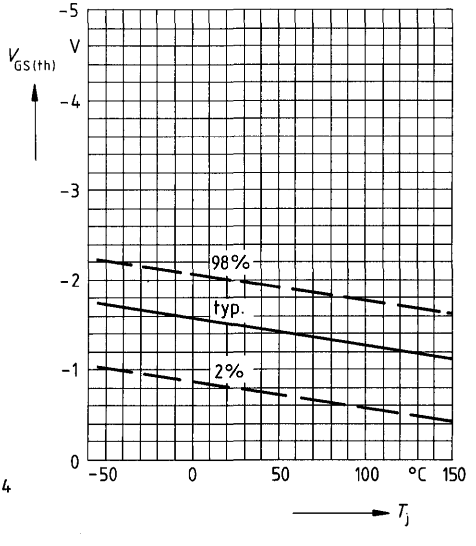
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = -10A$, $V_{GS} = -10V$
(spread)



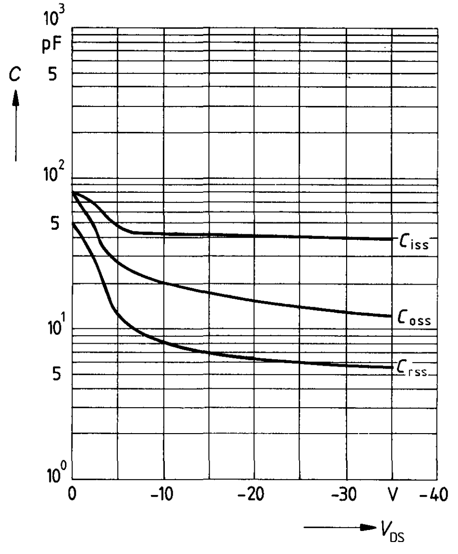
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = -25V$, $T_j = 25\,°C$



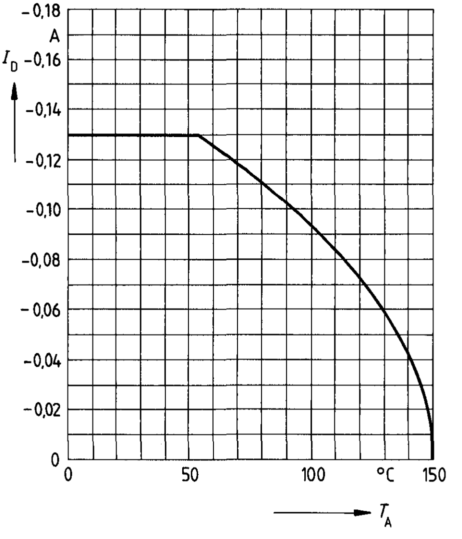
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = -1mA$
(spread)



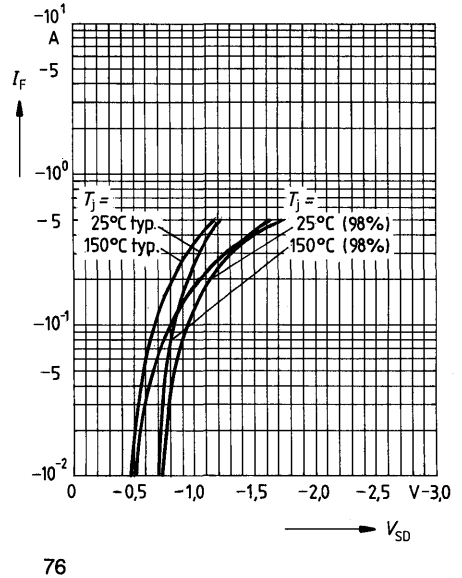
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq -5\text{V}$



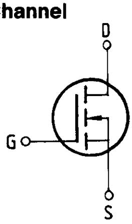
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

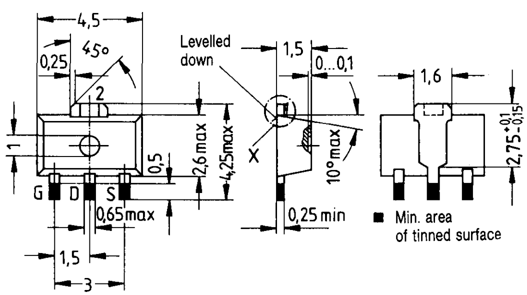
Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 280 mA**
Drain-source on-resistance $R_{DS(on)}$ **= 6,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package SOT 89 in accordance with JEDEC.
Approx. weight 0,1 g

Type	Marking	Ordering code for versions in bulk	Ordering code for version on 12 mm tape
S BSS 87	KA	Q62702-S453	Q62702-S506



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,28	A	T_A = 25 °C
Pulsed drain current	I_{Dpuls}	1,1	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	± 20	V	Aperiodic
Max. power dissipation	P_D	1	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip-substrate reverse side for package mounted on alumina 15 mm × 16.7 mm × 0.7 mm	$R_{th\ JA}$	≤ 125	K/W	

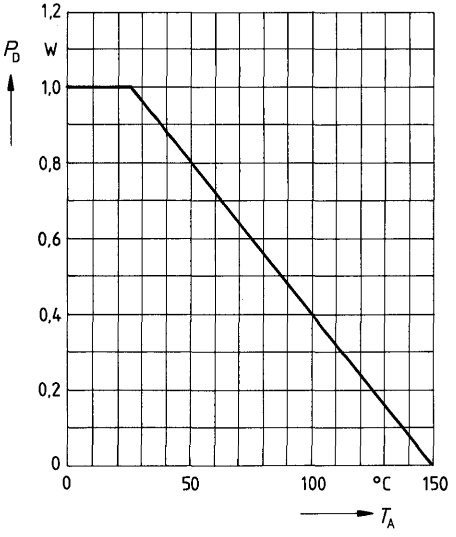
S Preferred Type

Electrical characteristics

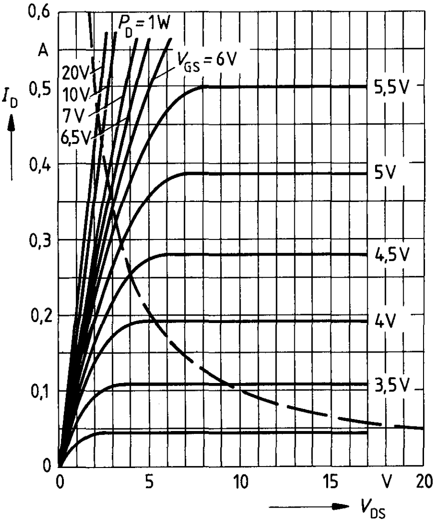
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	0,8	2,2	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	4 8	60 200	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
		–	–	200	nA	T_j = 25 °C V_{DS} = 60V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100		V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS(on)}$	–	5,5	6,0	Ω	V_{GS} = 10V I_D = 0,4A
Dynamic ratings						
Forward transconductance	g_{fs}	0,14	0,2	–	S	V_{DS} = 25V I_D = 0,4A
Input capacitance	C_{iss}	–	110	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	20	–		
Reverse transfer capacitance	C_{rss}	–	5	–		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 0,28A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	70	90		
	t_f	–	40	55		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,28	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	1,1		
Diode forward on-voltage	V_{SD}	–	1,0	1,4	V	I_F = 0,56A V_{GS} = 0V, T_j = 25 °C

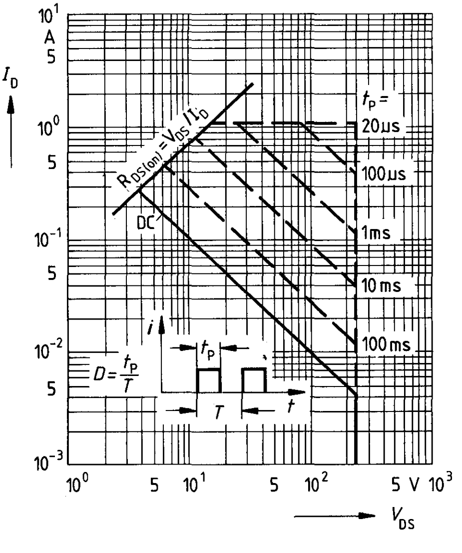
Power dissipation $P_D = f(T_A)$



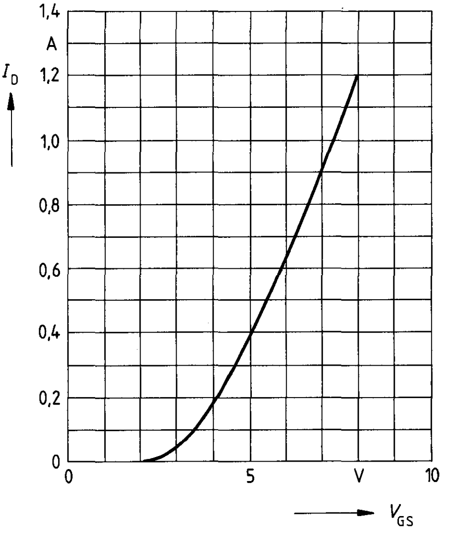
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



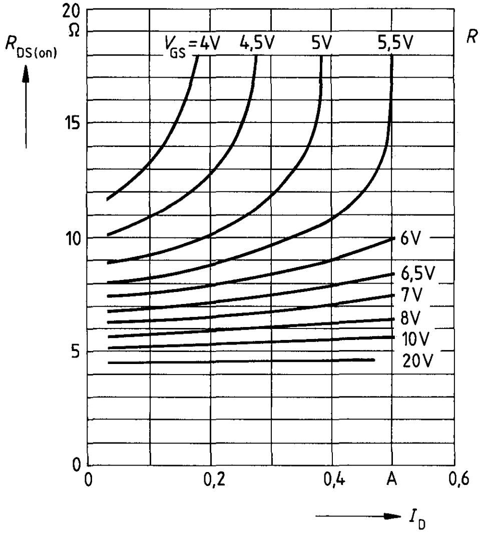
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



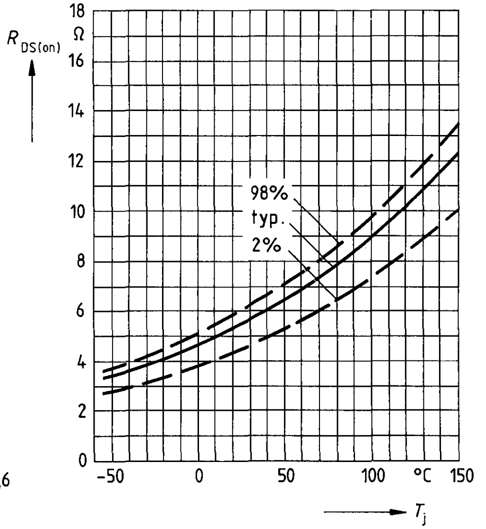
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



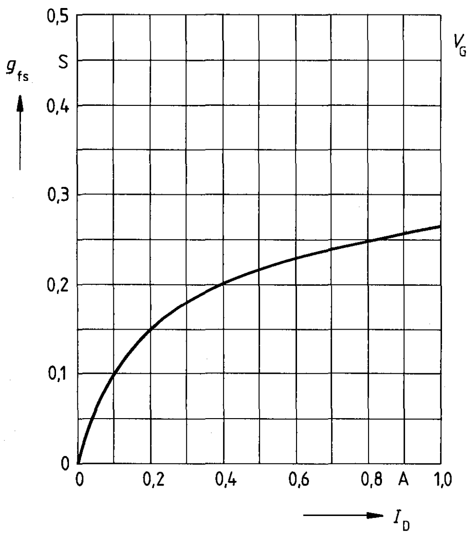
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



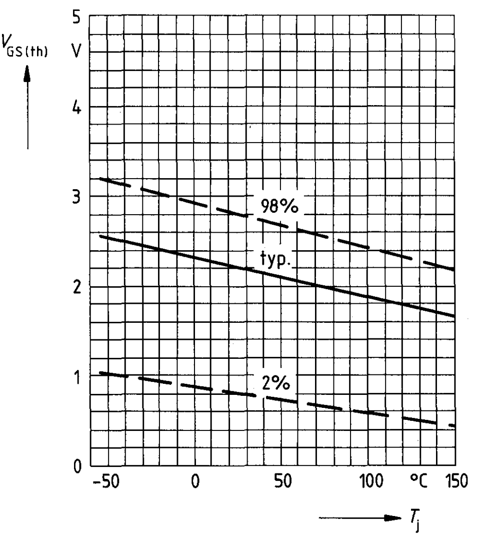
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 0.4A, V_{GS} = 10V
(spread)



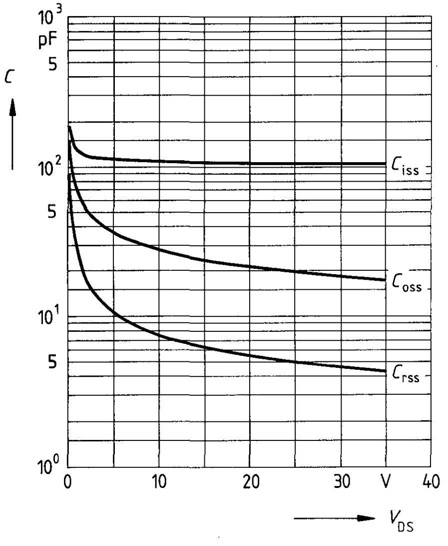
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



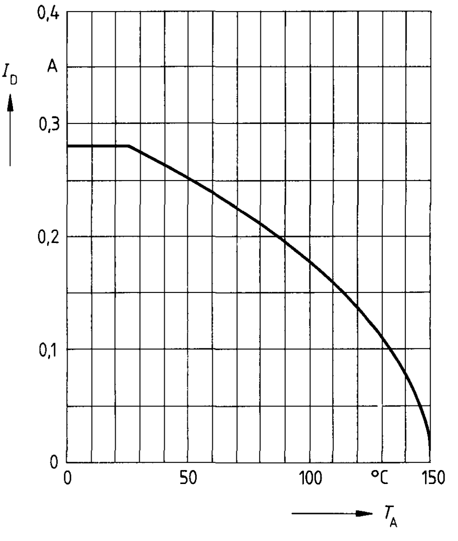
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



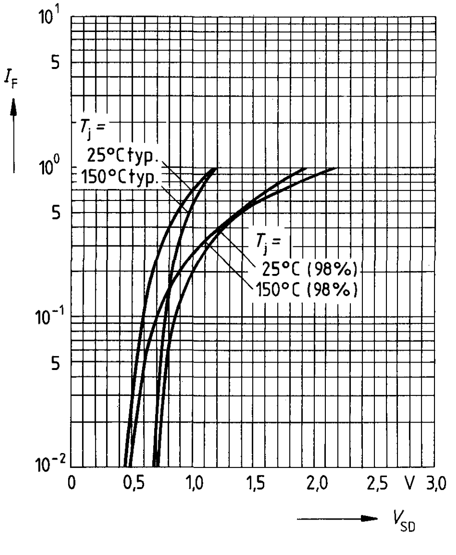
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 10\text{V}$



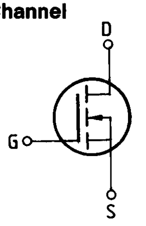
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

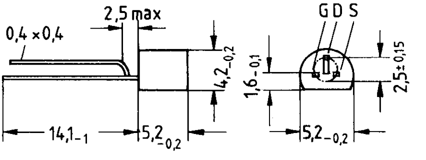
Drain-source voltage V_{DS} **= 230 V**
Continuous drain current I_D **= 250 mA**
Drain-source on-resistance $R_{DS(on)}$ **= 8 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 10 A 3 in accordance with DIN 41 868 or TO 92 in accordance with JEDEC.
Approx. weight 0,2 g

Type	Ordering code
S BSS 88	Q62702-S454



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	230	V	
Drain-gate voltage	V_{DGR}	230	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,25	A	T_A = 25 °C
Pulsed drain current	I_{Dpuls}	1,0	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	1,0	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\,JA}$	≤125	K/W	

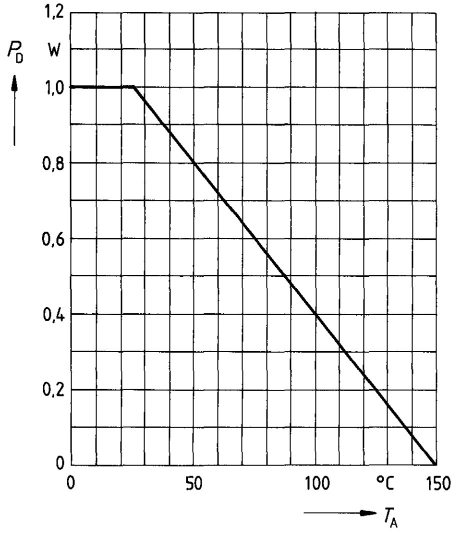
 S Preferred Type

Electrical characteristics

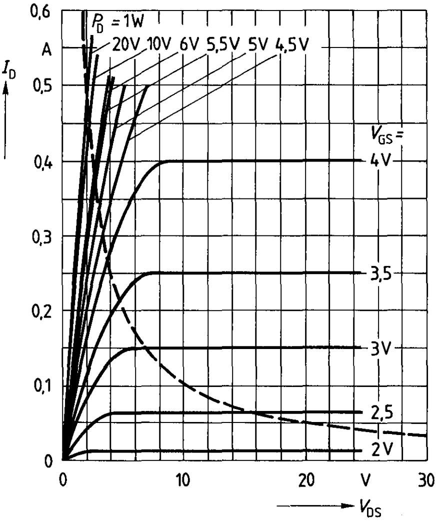
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	230	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,4	0,8	1,2	V	V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	1 10	20 200	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 230V V_{GS} = 0V
		–	–	100	nA	T_j = 25 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	–	15	Ω	V_{GS} = 1,8V I_D = 14mA
		–	5	8	Ω	V_{GS} = 5V I_D = 0,15A
Dynamic ratings						
Forward transconductance	g_{fs}	0,14	0,2	–	S	V_{DS} = 25V I_D = 0,15A
Input capacitance	C_{iss}	–	110	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	20	–	pF	
Reverse transfer capacitance	C_{rss}	–	5	–	pF	
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	–	ns	V_{CC} = 30V I_D = 0,28A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	–	ns	
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	–	ns	
	t_f	–	40	–	ns	
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,25	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	1,0	A	
Diode forward on-voltage	V_{SD}	–	1,0	1,4	V	I_F = 0,5A V_{GS} = 0V

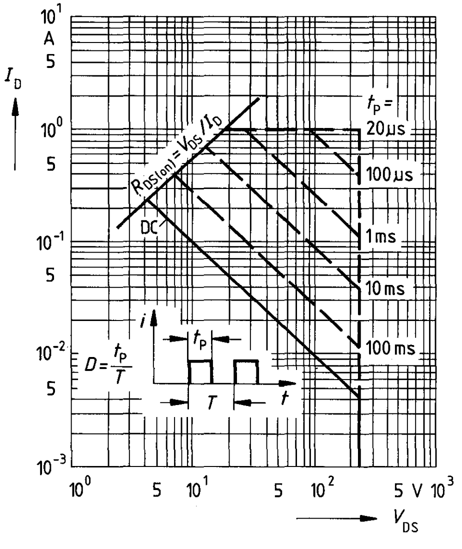
Power dissipation $P_D = f(T_A)$



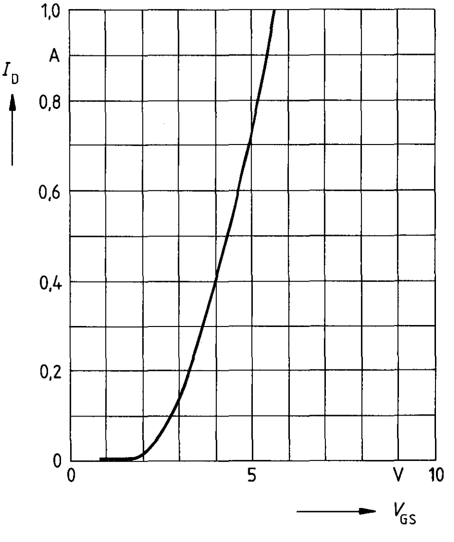
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



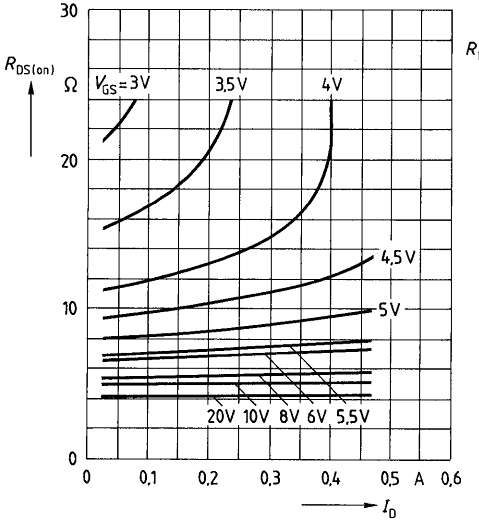
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



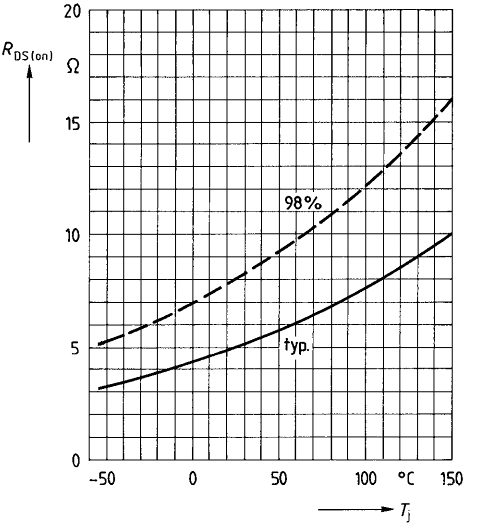
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



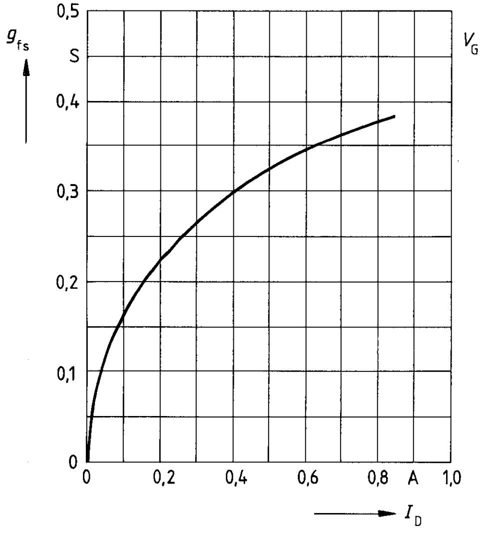
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



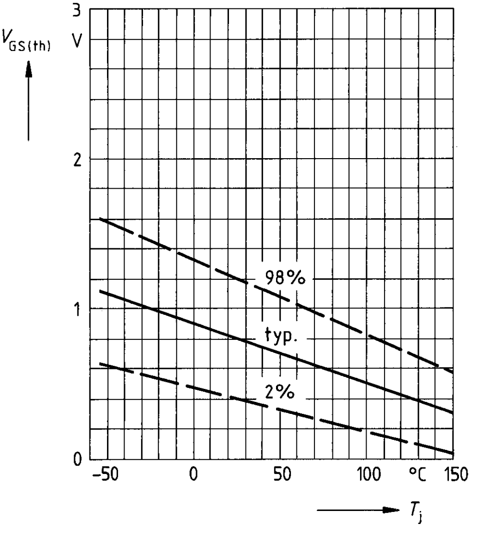
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 0.15A, V_{GS} = 5V
(spread)



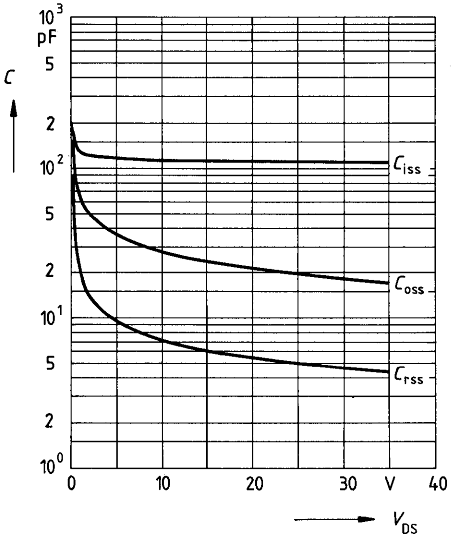
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 μs pulse test,
V_{DS} = 25V, T_j = 25 °C



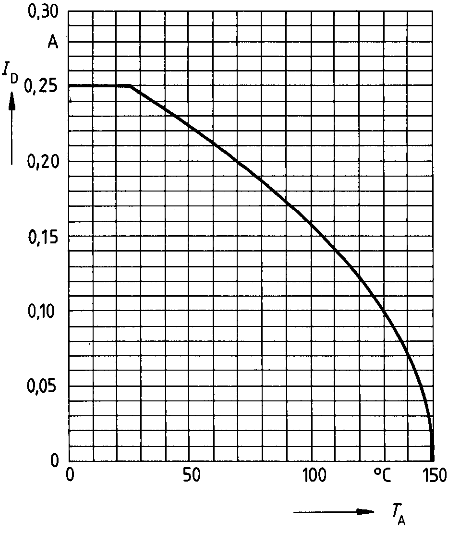
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



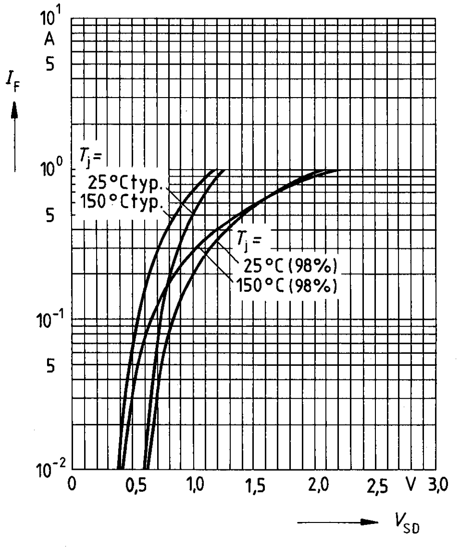
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 5\text{V}$



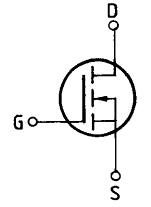
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

N-Channel

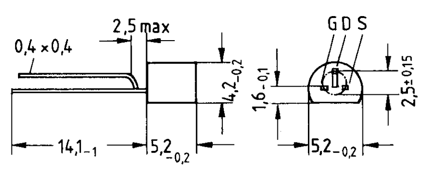
Drain-source voltage	V_{DS}	**= 200 V**
Continuous drain current	I_D	**= 300 mA**
Drain-source on-resistance	$R_{DS(on)}$	**= 6,0 Ω**



Description SIPMOS, N-channel, enhancement mode

Case Plastic package 10 A 3 in accordance with DIN 41 868 or TO 92 in accordance with JEDEC.
Approx. weight 0,2 g

Type	Ordering code
S BSS 89	Q62702-S455



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,3	A	T_A = 25 °C
Pulsed drain current	I_{Dpuls}	1,2	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	1,0	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\,JA}$	≤125	K/W	

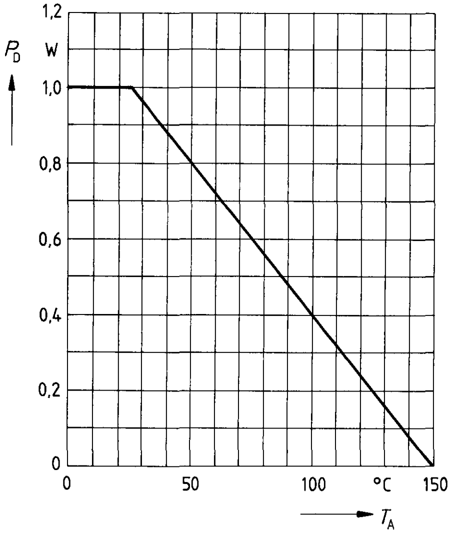
S Preferred Type

Electrical characteristics

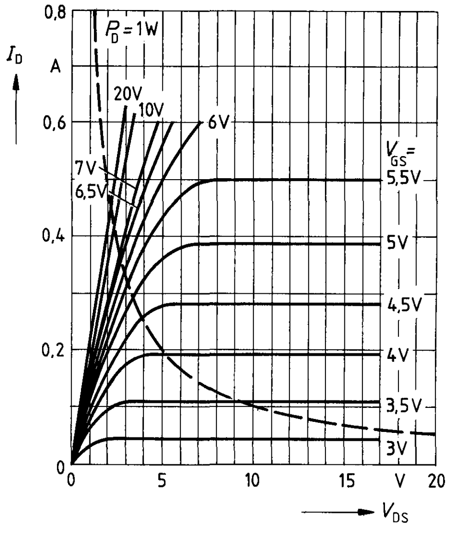
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2,2	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	4 8	60 200	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
		–	–	200	nA	T_j = 25 °C V_{DS} = 60V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100		V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	5,5	6,0	Ω	V_{GS} = 10V I_D = 0,4A
Dynamic ratings						
Forward transconductance	g_{fs}	0,14	0,2	–	S	V_{DS} = 25V I_D = 0,4A
Input capacitance	C_{iss}	–	110	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	20	–		
Reverse transfer capacitance	C_{rss}	–	5	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 0,28A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	40	55		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,3	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	1,2		
Diode forward on-voltage	V_{SD}	–	1,0	1,4	V	I_F = 0,6A V_{GS} = 0V, T_j = 25 °C

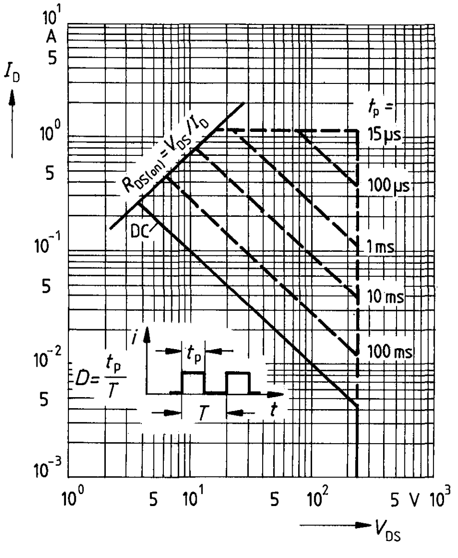
Power dissipation $P_D = f(T_A)$



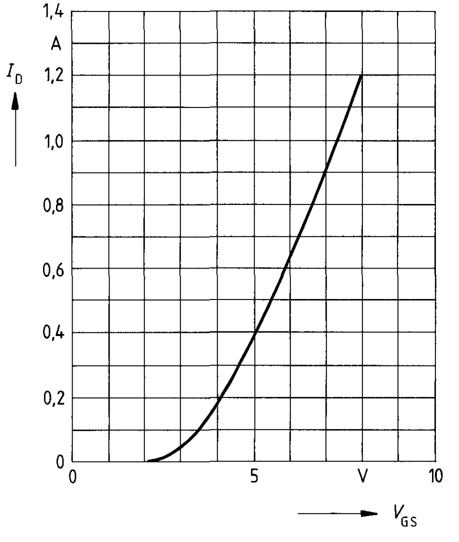
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



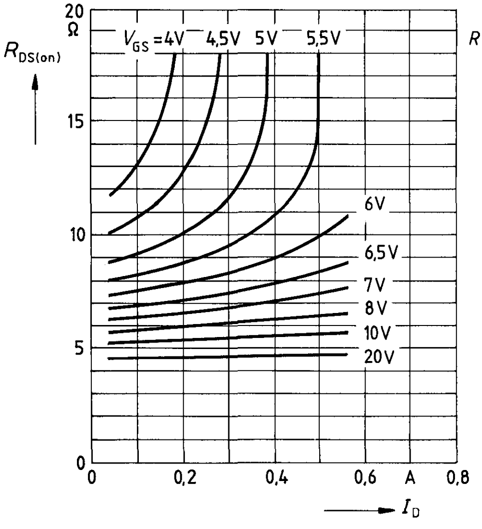
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



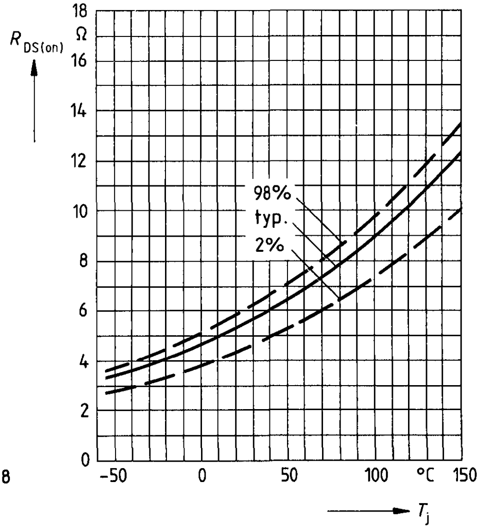
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



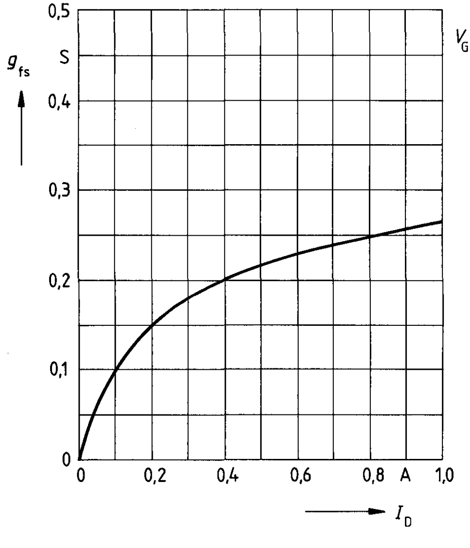
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



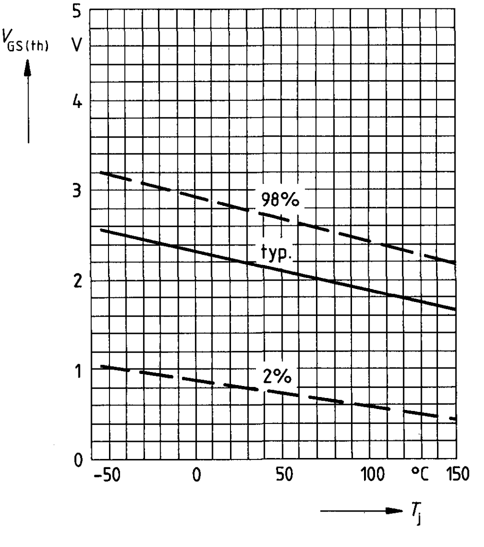
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 0.4A, V_{GS} = 10V
(spread)



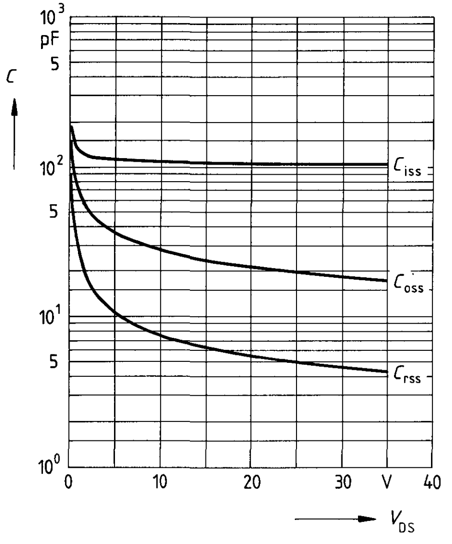
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



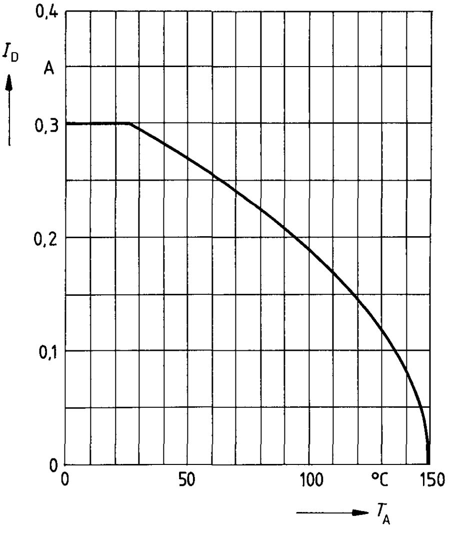
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



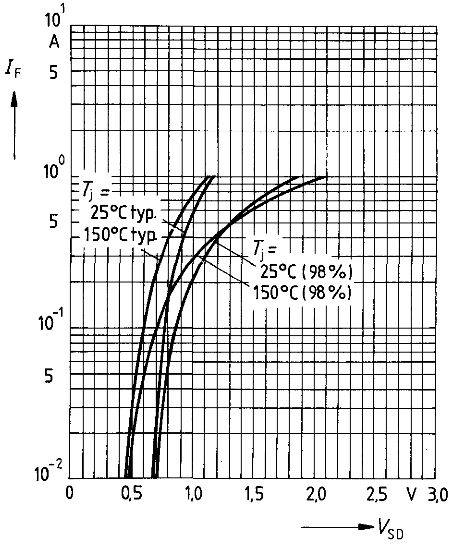
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \leq 10\text{V}$

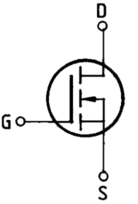


Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu\text{s}$
(spread)



Main ratings

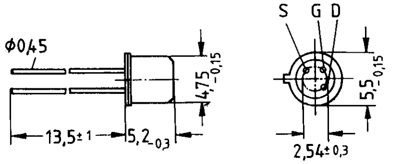
N-Channel



Drain-source voltage V_{DS} = **200 V**
Continuous drain current I_D = **350 mA**
Drain-source on-resistance $R_{DS(on)}$ = **6,0 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package 18 A 3 in accordance with DIN 41 876 or TO 18 in accordance with JEDEC.
Approx. weight 0,3 g

Type	Ordering code
BSS 91	Q62702-S457



Dimensions in mm

Maximum ratings

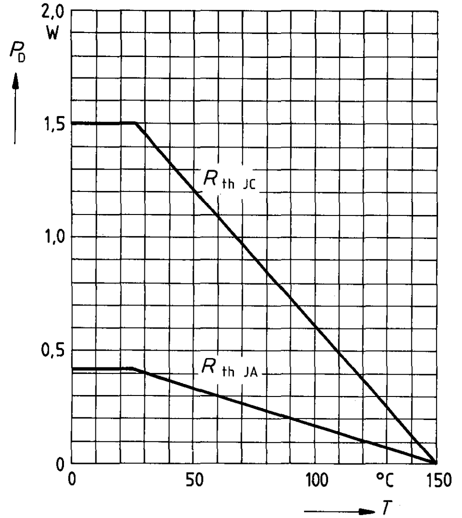
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,35	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	1,4	A	T_C = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	1,5	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤83	K/W	
Chip – ambient	$R_{th\ JA}$	≤300	K/W	

Electrical characteristics

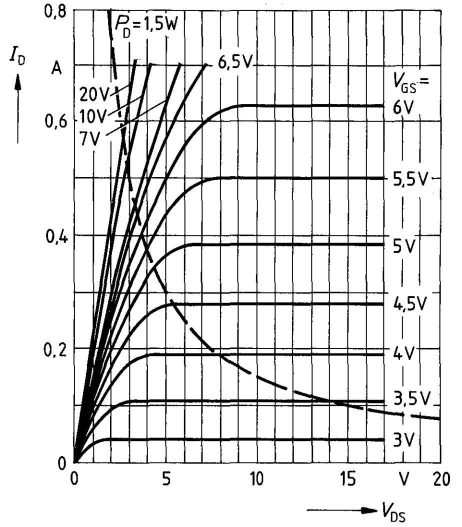
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V, I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2,2	2,8		V_{DS} = V_{GS}, I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	4 8	60 200	μA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
		–	–	200	nA	T_j = 25 °C, V_{DS} = 60V, V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100		V_{GS} = 20V, V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	5,5	6,0	Ω	V_{GS} = 10V, I_D = 0,4A
Dynamic ratings						
Forward transconductance	g_{fs}	0,14	0,2	–	S	V_{DS} = 25V, I_D = 0,4A
Input capacitance	C_{iss}	–	110	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	20	–		
Reverse transfer capacitance	C_{rss}	–	5	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 0,28A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	40	55		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,35	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	1,4		
Diode forward on-voltage	V_{SD}	–	1,0	1,4	V	I_F = 0,7A V_{GS} = 0V, T_j = 25 °C

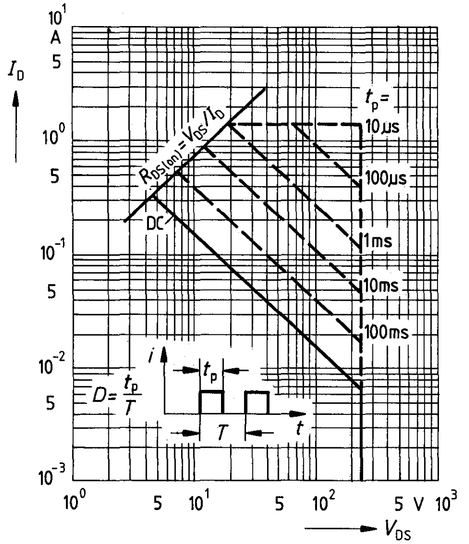
Power dissipation $P_D = f(T)$



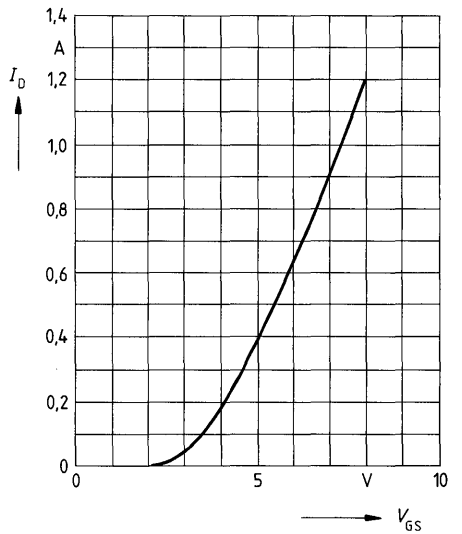
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



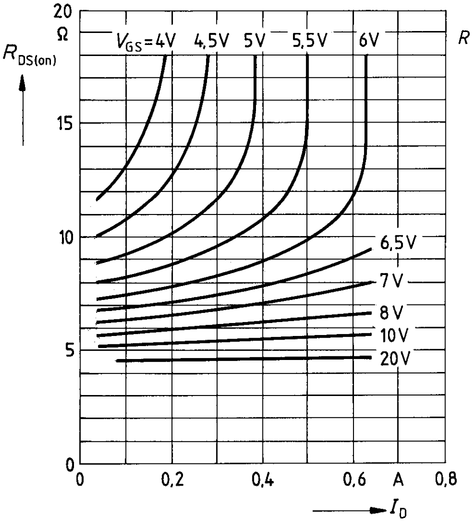
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



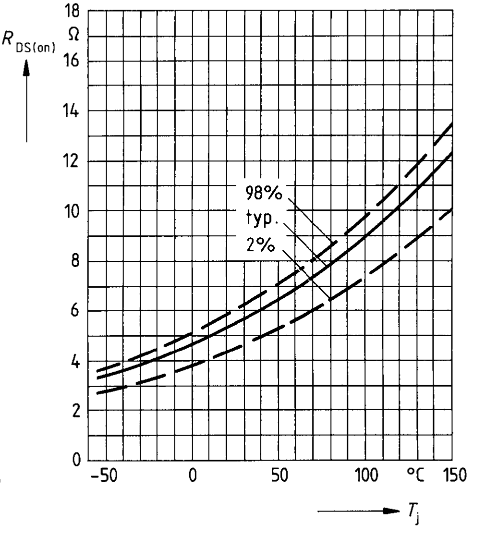
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



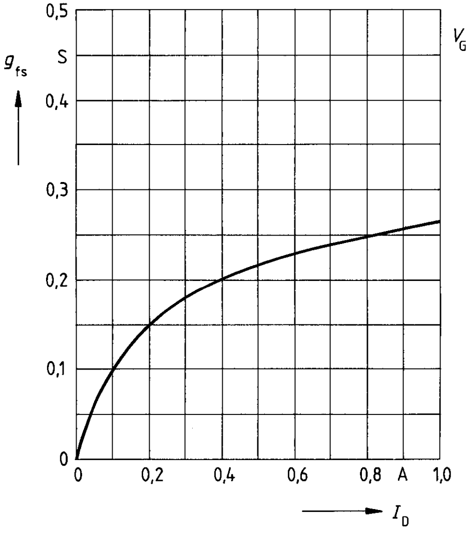
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



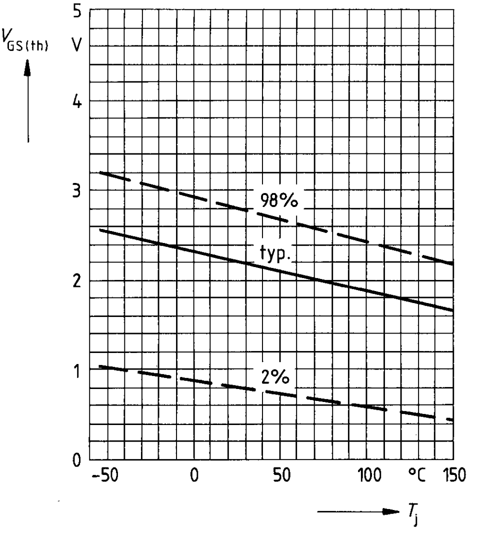
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 0.4A$, $V_{GS} = 10V$
(spread)



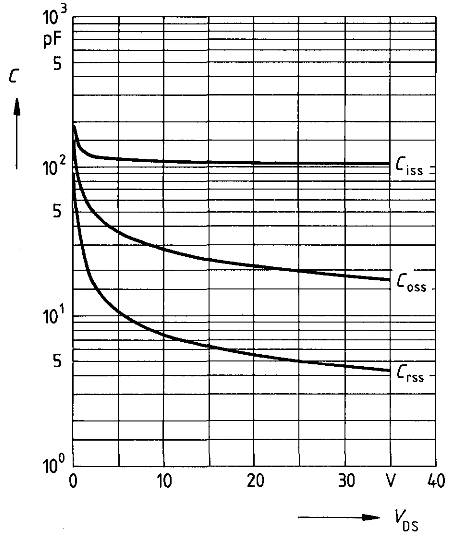
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



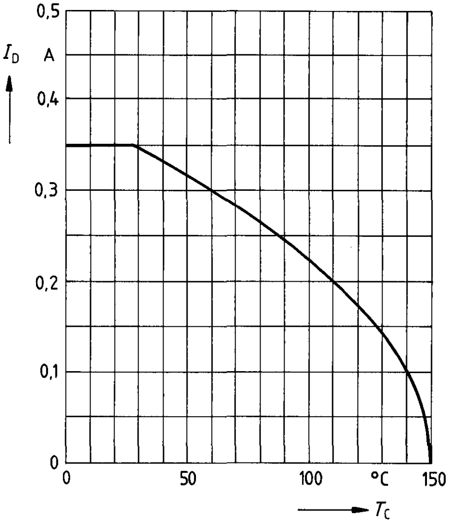
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



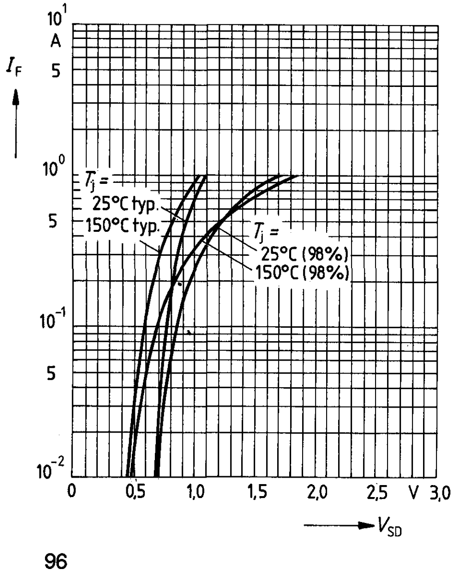
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \leq 10\text{V}$

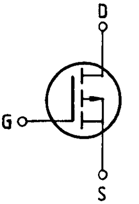


Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

P-Channel

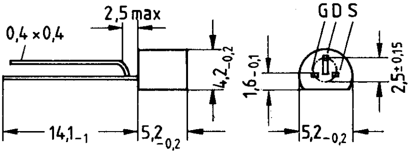


Drain-source voltage	V_{DS}	=	**– 200 V**
Continuous drain current	I_D	=	**– 150 mA**
Drain-source on-resistance	$R_{DS(on)}$	=	**20 Ω**

Description SIPMOS, P-channel, enhancement mode

Case Plastic package 10 A 3 in accordance with DIN 41 868 or TO 92 in accordance with JEDEC.
Approx. weight 0,2 g

Type	Ordering code
S BSS 92	Q62702-S458



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	– 200	V	
Drain-gate voltage	V_{DGR}	– 200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	– 0,15	A	T_A = 25 °C
Pulsed drain current	I_{Dpuls}	– 0,6	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	± 20	V	Aperiodic
Max. power dissipation	P_D	1	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\ JA}$	≤ 125	K/W	

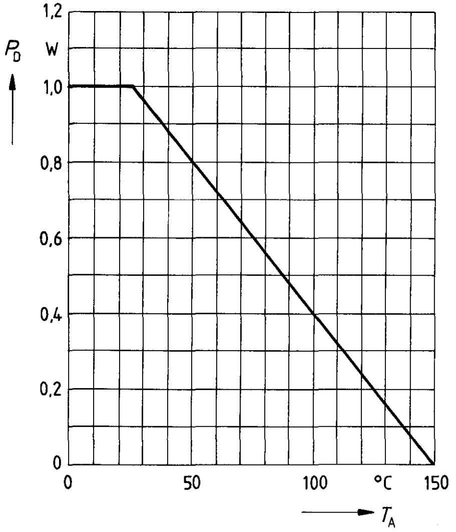
S Preferred Type

Electrical characteristics

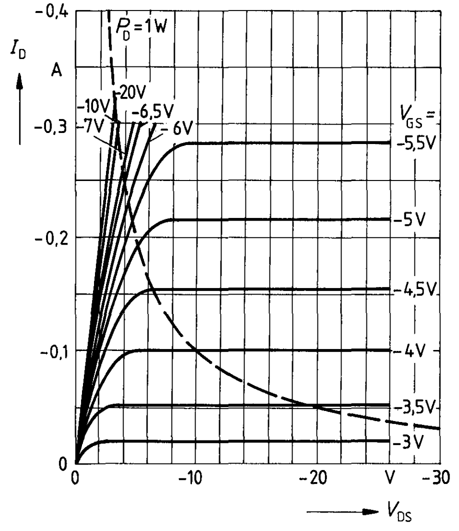
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	– 200	–	–	V	V_{GS} = 0V I_D = – 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	– 0,8	– 2,4	– 2,8		V_{DS} = V_{GS} I_D = – 1mA
Zero gate voltage drain current	I_{DSS}	–	– 4 – 8	– 60 – 200	µA	T_j = 25 °C T_j = 125 °C V_{DS} = – 200V V_{GS} = 0V
		–	–	– 0,2	µA	T_j = 25 °C V_{DS} = – 60V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	– 10	– 100		V_{GS} = – 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	11	20	Ω	V_{GS} = – 10V I_D = – 100mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,06	0,10	–	S	V_{DS} = – 25V I_D = – 100mA
Input capacitance	C_{iss}	–	170	–	pF	V_{GS} = 0V V_{DS} = – 25V f = 1MHz
Output capacitance	C_{oss}	–	20	–		
Reverse transfer capacitance	C_{rss}	–	6	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = – 30V I_D = – 0,25A V_{GS} = – 10V R_{GS} = 50Ω
	t_r	–	10	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	20	–		
	t_f	–	30	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	– 0,15	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	– 0,6		
Diode forward on-voltage	V_{SD}	–	– 0,9	– 1,2	V	I_F = – 0,3A V_{GS} = 0V

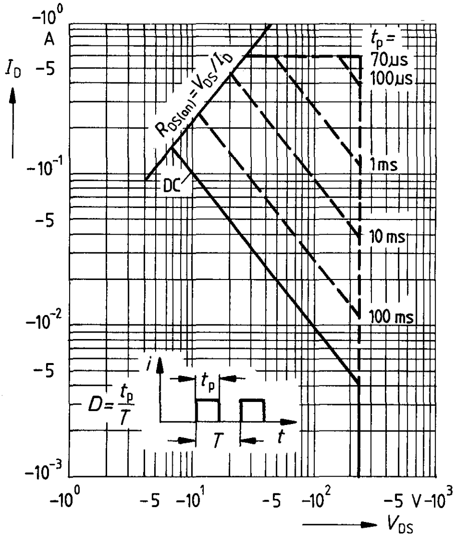
Power dissipation $P_D = f(T_A)$



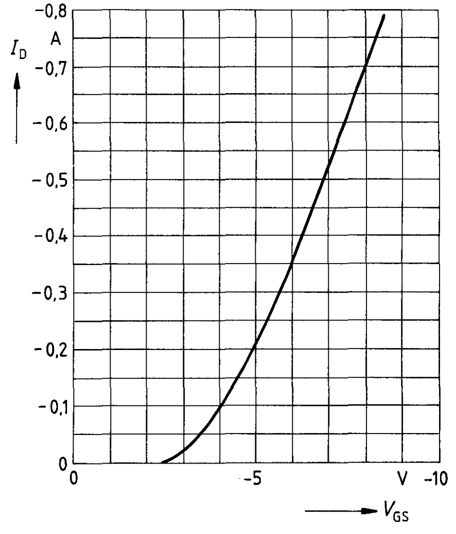
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



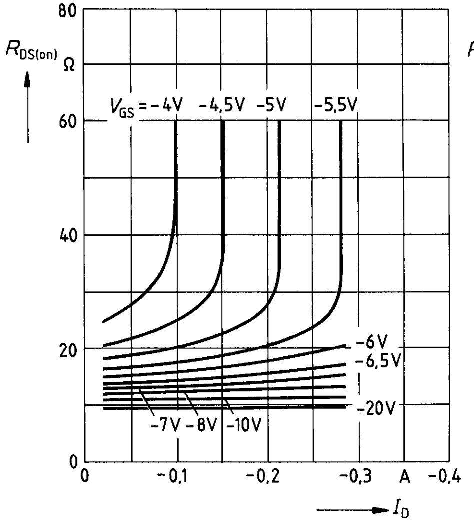
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



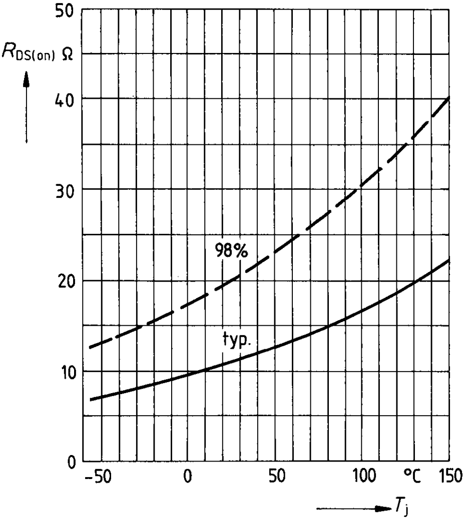
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = -25V$, $T_j = 25\,°C$



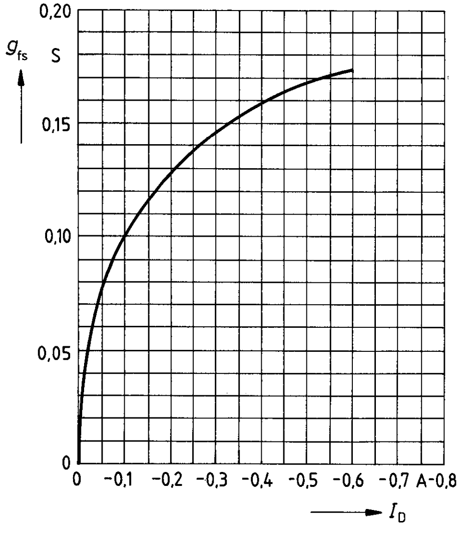
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



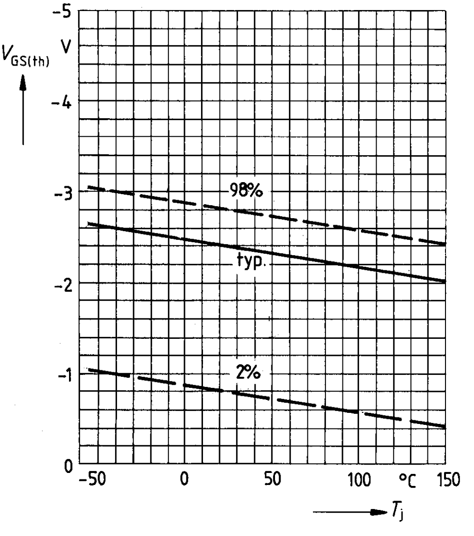
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = -100mA$, $V_{GS} = -10V$
(spread)



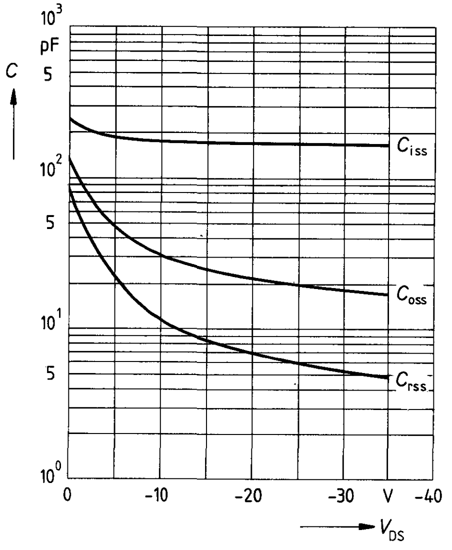
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = -25V$, $T_j = 25\,°C$



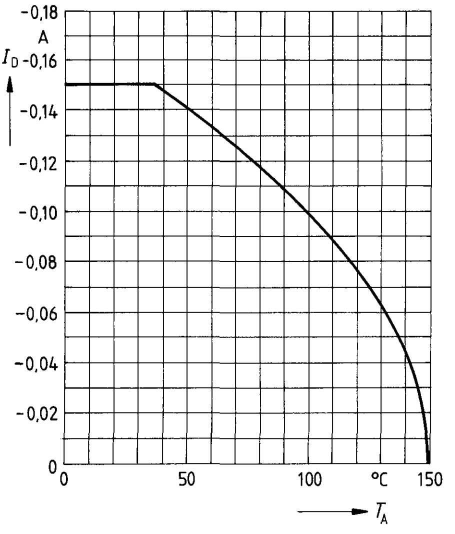
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = -1mA$
(spread)



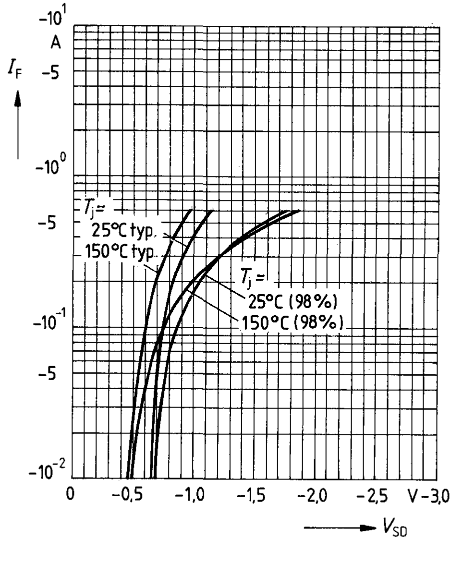
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq -10\text{V}$



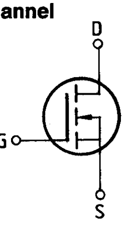
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu\text{s}$
(spread)



Main ratings

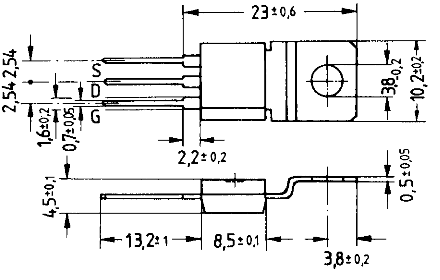
Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 800 mA**
Drain-source on-resistance $R_{DS(on)}$ **= 6,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 202 in accordance with JEDEC.
Approx. weight 1,8 g

Type	Ordering code
S BSS 95	Q62702-S461



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,8	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	3,2	A	T_C = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	8,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤15	K/W	
Chip – ambient	$R_{th\,JA}$	≤65	K/W	

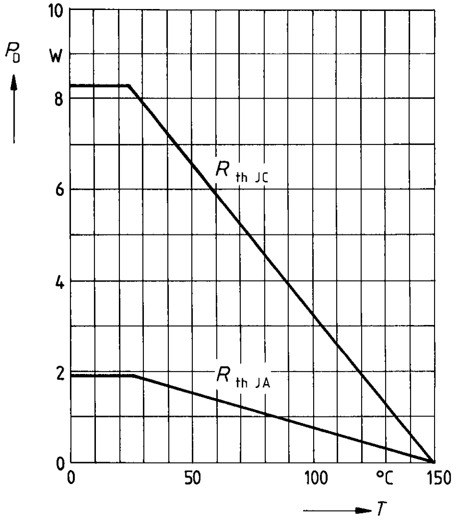
 S Preferred Type

Electrical characteristics

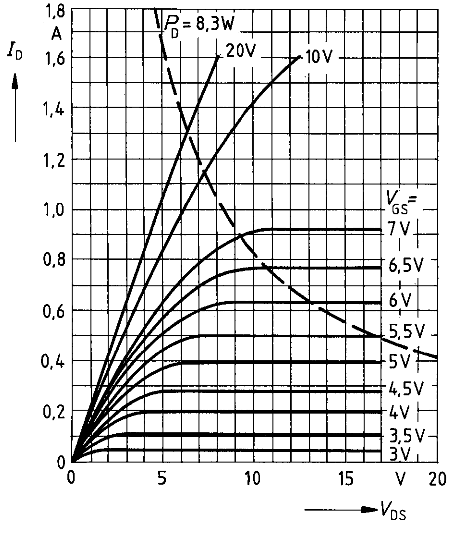
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2,2	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	4 8	60 200	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
		–	–	200	nA	T_j = 25 °C V_{DS} = 60V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100		V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	5,5	6,0	Ω	V_{GS} = 10V I_D = 0,4A
Dynamic ratings						
Forward transconductance	g_{fs}	0,14	0,2	–	S	V_{DS} = 25V I_D = 0,4A
Input capacitance	C_{iss}	–	110	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	20	–		
Reverse transfer capacitance	C_{rss}	–	5	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 0,28A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	40	55		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,8	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	3,2		
Diode forward on-voltage	V_{SD}	–	1,4	1,8	V	I_F = 1,6A V_{GS} = 0V, T_j = 25 °C

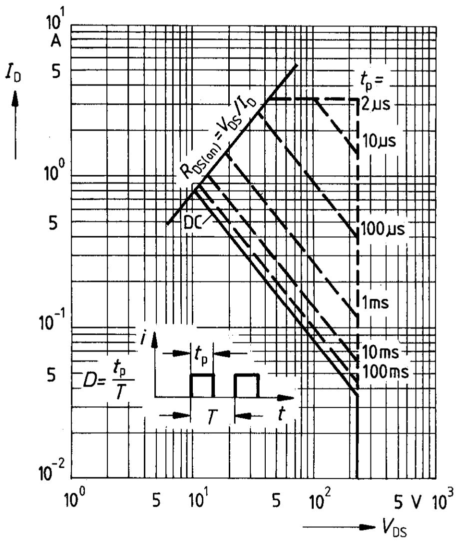
Power dissipation $P_D = f(T)$



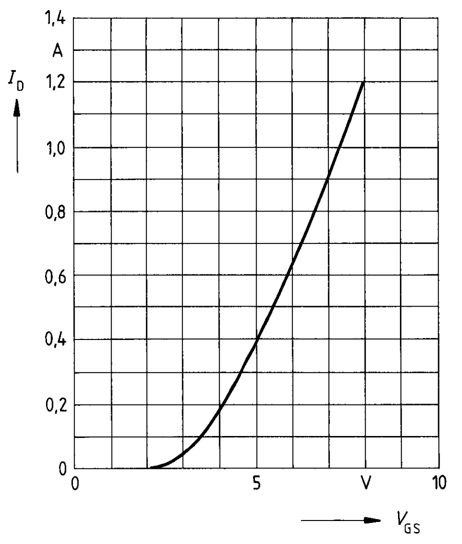
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



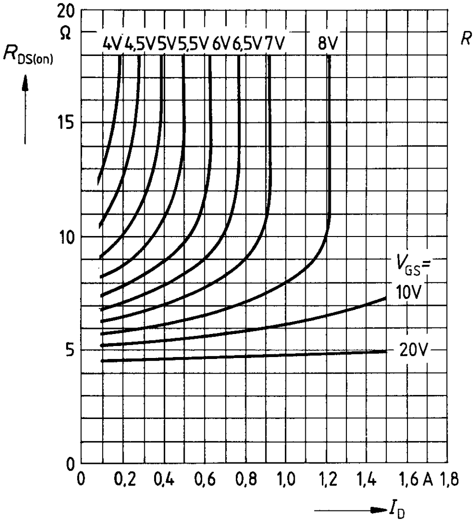
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



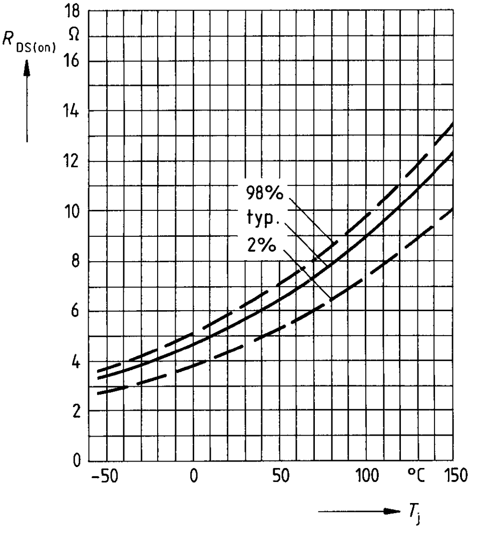
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



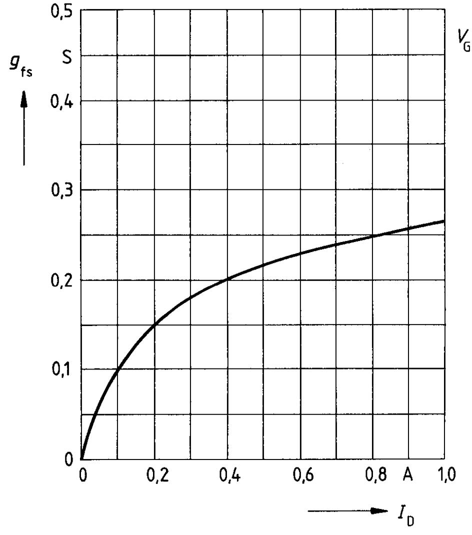
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



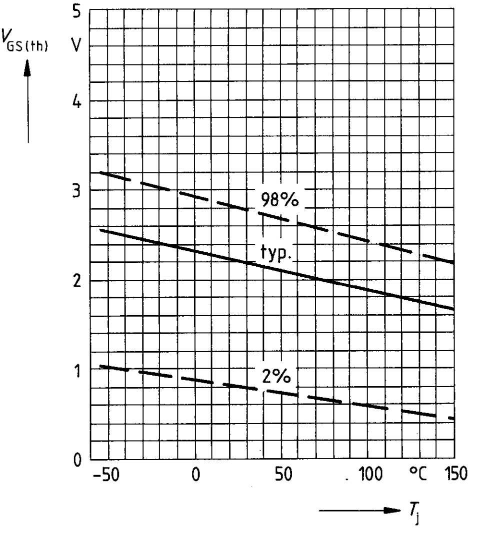
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 0.4A$, $V_{GS} = 10V$
(spread)



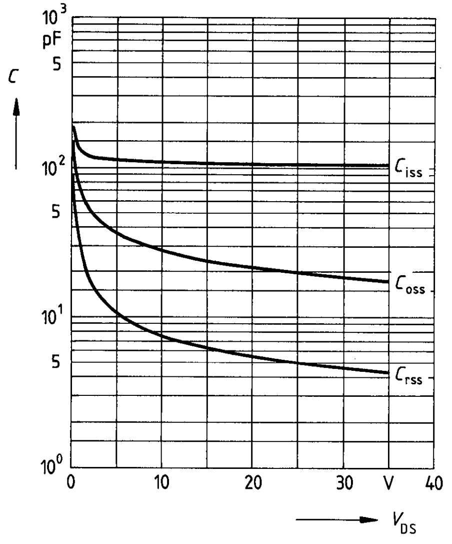
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



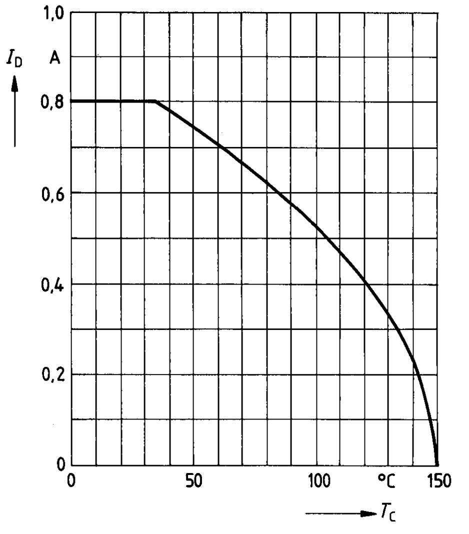
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



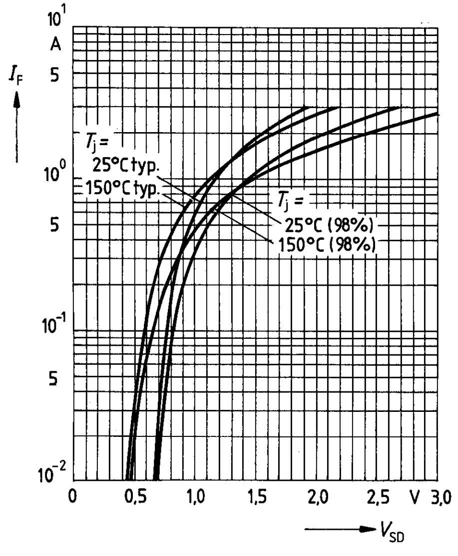
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



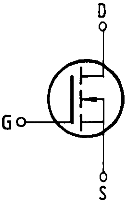
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

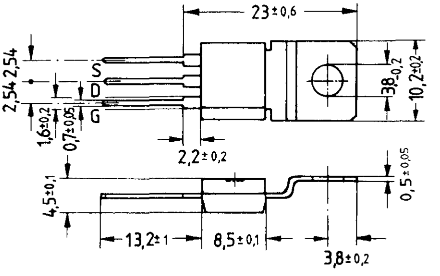
Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 1500 mA**
Drain-source on-resistance $R_{DS(on)}$ **= 2,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 202 in accordance with JEDEC.
Approx. weight 1.8 g

Type	Ordering code
S BSS 97	Q62702-S463



Dimensions in mm

Maximum ratings

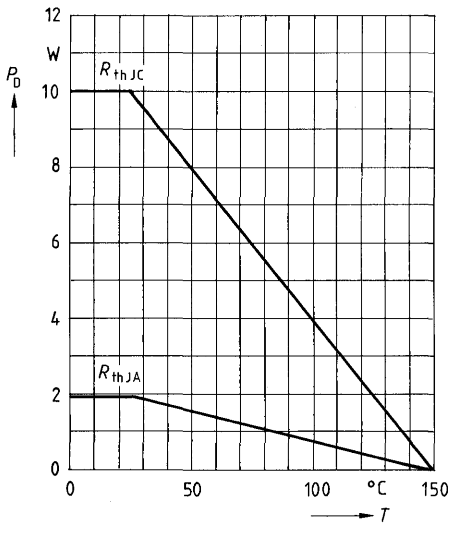
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	1,5	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	6,0	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	1,0	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤12,5	K/W	
Chip – ambient	$R_{th\,JA}$	≤65	K/W	

S Preferred Type

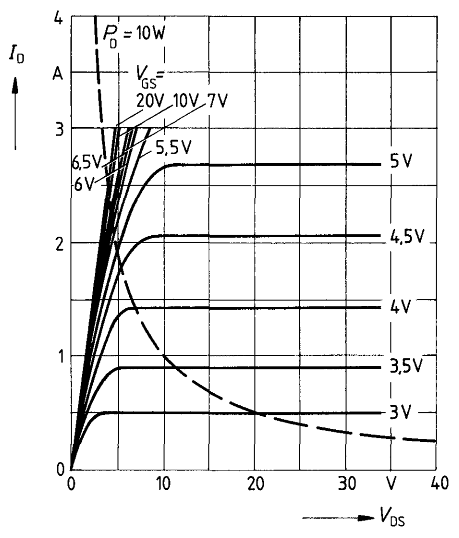
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2,2	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	4 8	60 200	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
		–	–	200	nA	T_j = 25 °C V_{DS} = 60V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100		V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	1,6	2,0	Ω	V_{GS} = 10V I_D = 0,75A
Dynamic ratings						
Forward transconductance	g_{fs}	0,5	1	–	S	V_{DS} = 25V I_D = 0,75A
Input capacitance	C_{iss}	–	400	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	60	–		
Reverse transfer capacitance	C_{rss}	–	30	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 0,29A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	40	55		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	1,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	6,0		
Diode forward on-voltage	V_{SD}	–	1,4	1,8	V	I_F = 3A V_{GS} = 0V, T_j = 25 °C

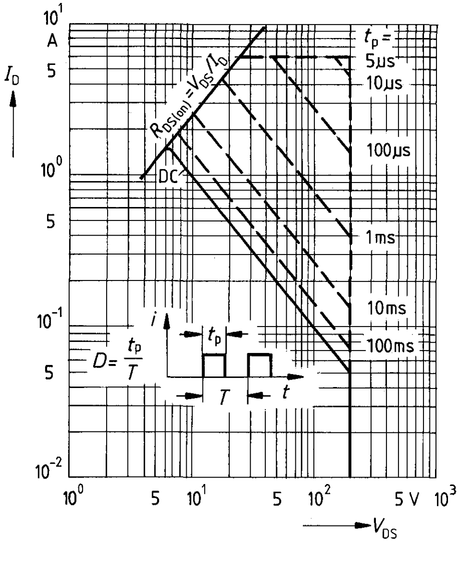
Power dissipation $P_D = f(T)$



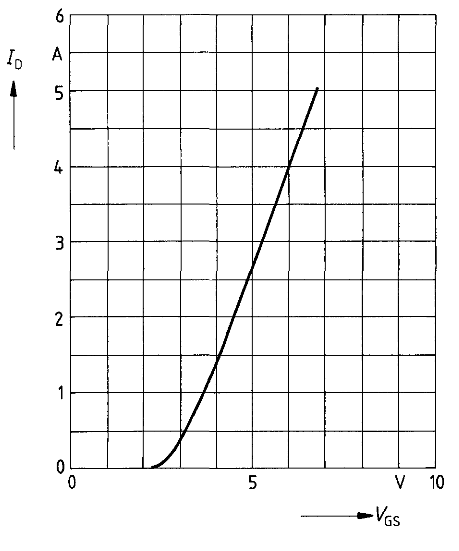
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



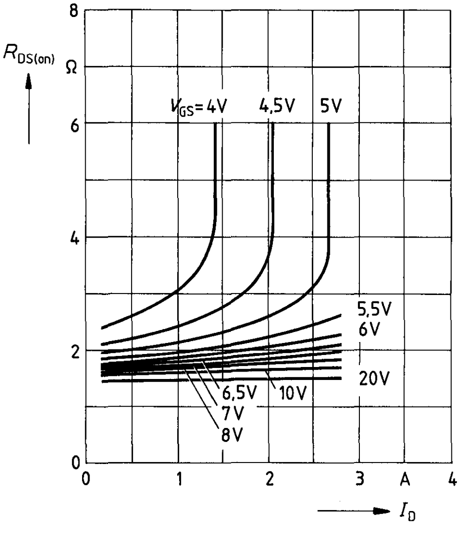
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



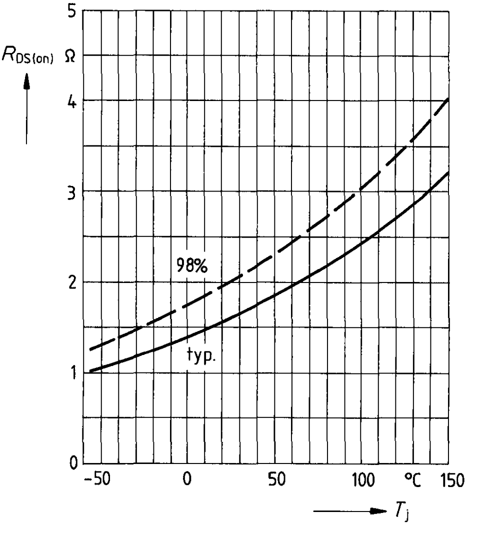
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



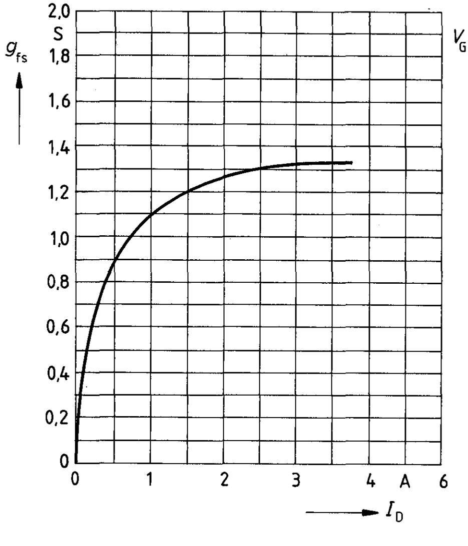
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



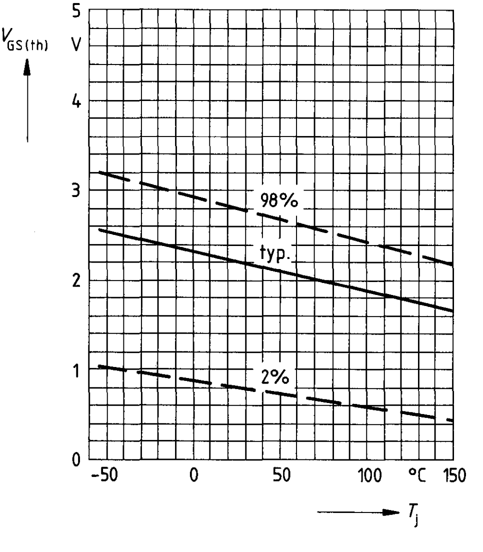
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 0.75A, V_{GS} = 10V
(spread)



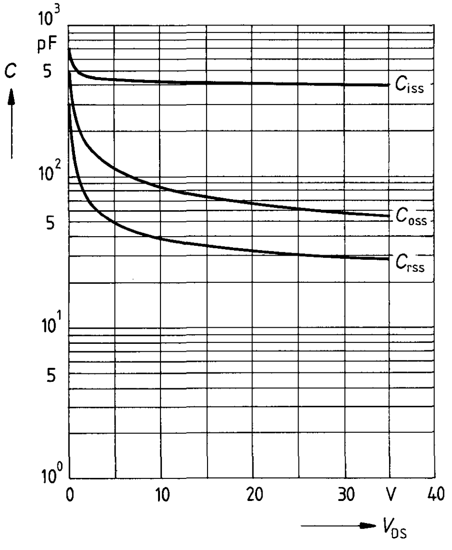
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



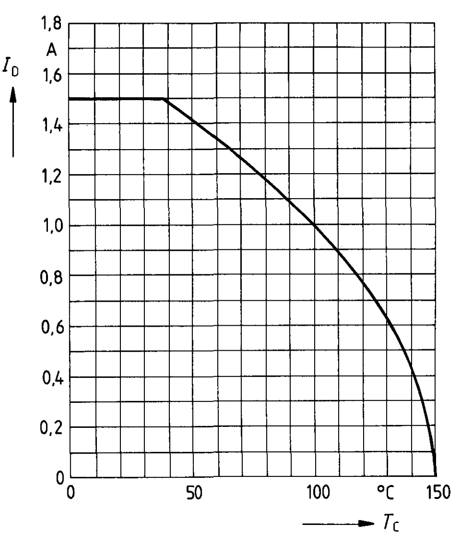
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



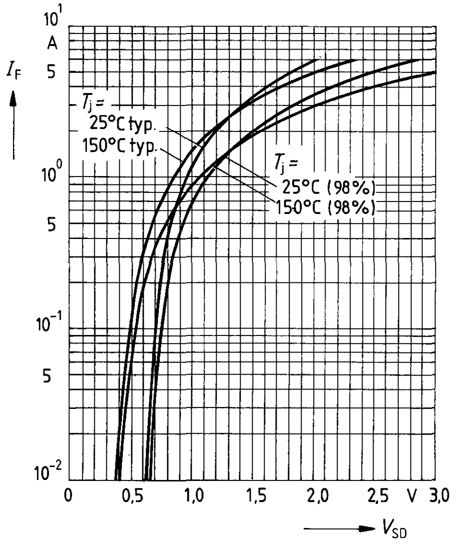
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



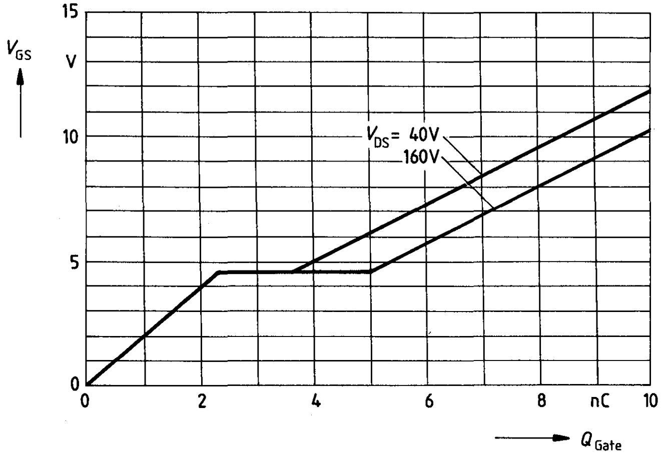
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



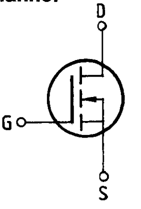
Typical gate charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 2{,}25A$



Main ratings

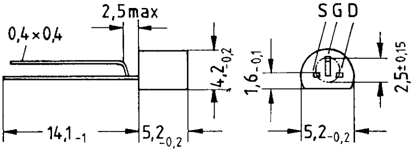
Drain-source voltage V_{DS} = **50 V**
Continuous drain current I_D = **300 mA**
Drain-source on-resistance $R_{DS(on)}$ = **3,5 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 10 A3 in accordance with DIN 41 868
or TO 92 in accordance with JEDEC.
Approx. weight 0.2 g

Type	Ordering code
S BSS 98	Q62702-S464



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,3	A	T_A = 25 °C
Pulsed drain current	I_{Dpuls}	1,2	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	0,63	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\,JA}$	≤200	K/W	

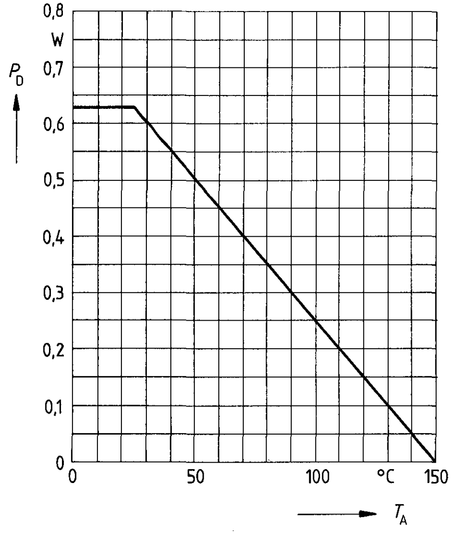
S Preferred Type

Electrical characteristics

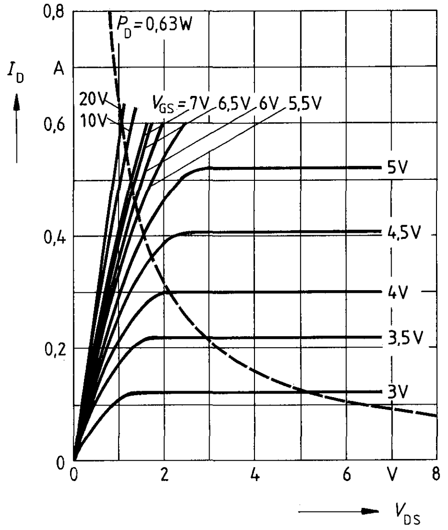
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	50	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	0,5	1,0	1,5		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	0,05 –	0,5 5	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
		–	–	100	nA	T_j = 25 °C V_{DS} = 30V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100		V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS(on)}$	–	2,0	3,5	Ω	V_{GS} = 5V I_D = 0,3mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,12	0,2	–	S	V_{DS} = 25V I_D = 0,3A
Input capacitance	C_{iss}	–	40	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	12	–		
Reverse transfer capacitance	C_{rss}	–	5	–		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	8	–	ns	V_{CC} = 30V I_D = 0,29A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	8	–		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	16	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,3	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	1,2		
Diode forward on-voltage	V_{SD}	–	1,1	1,4	V	I_F = 0,6A V_{GS} = 0V

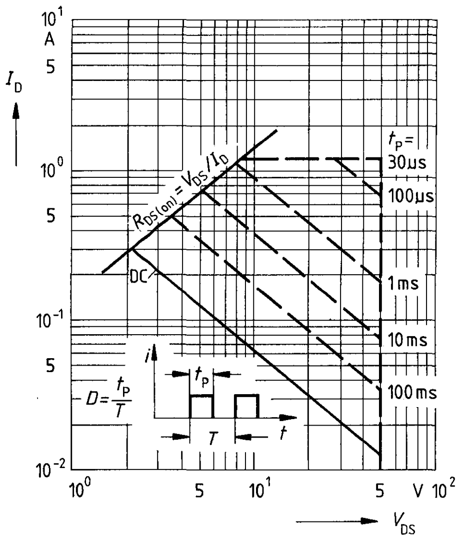
Power dissipation $P_D = f(T_A)$



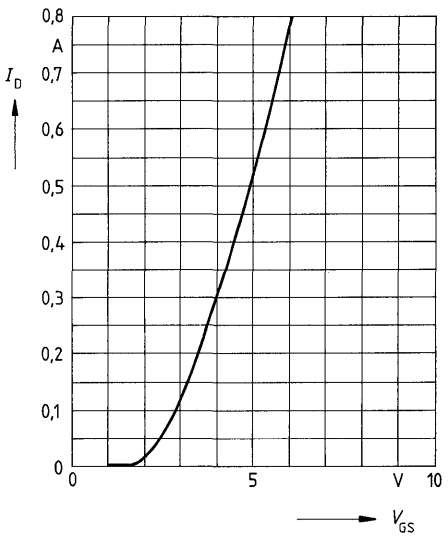
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



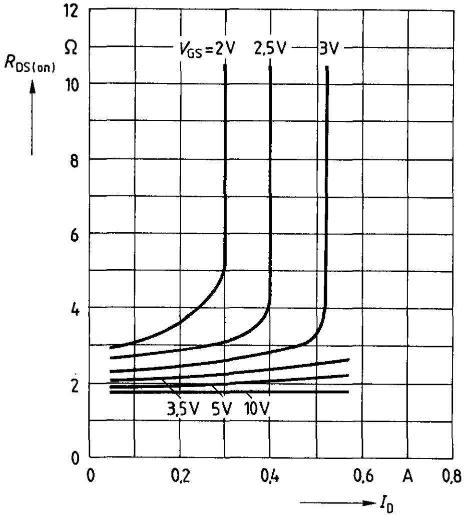
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



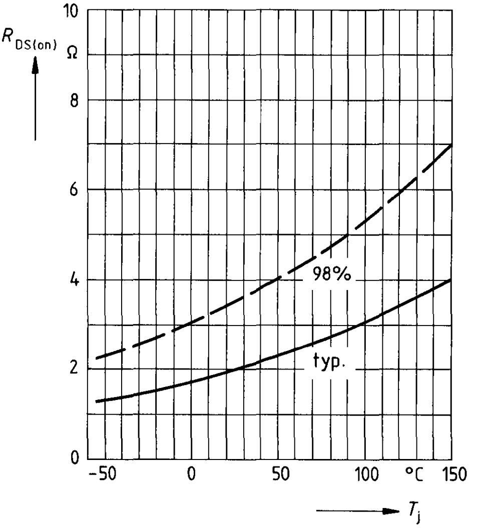
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



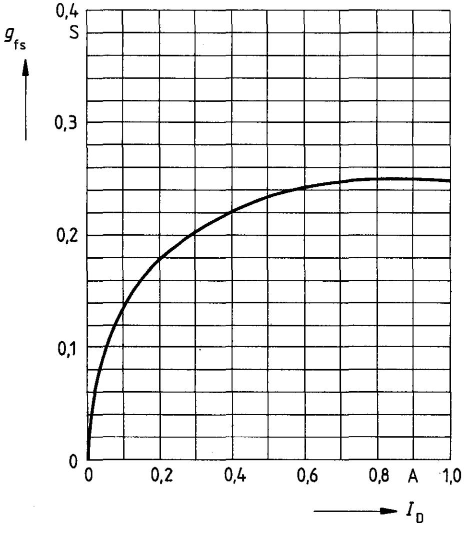
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



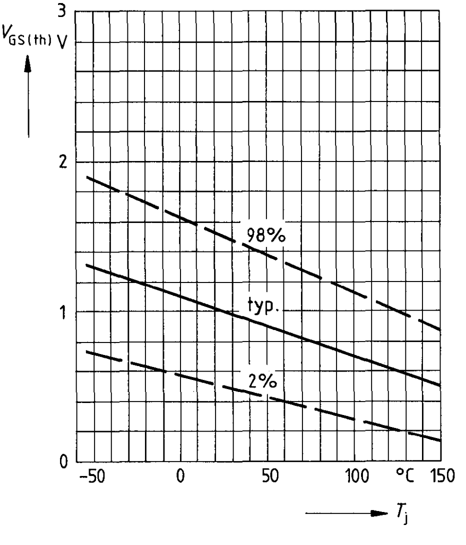
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 0.3A$, $V_{GS} = 10V$
(spread)



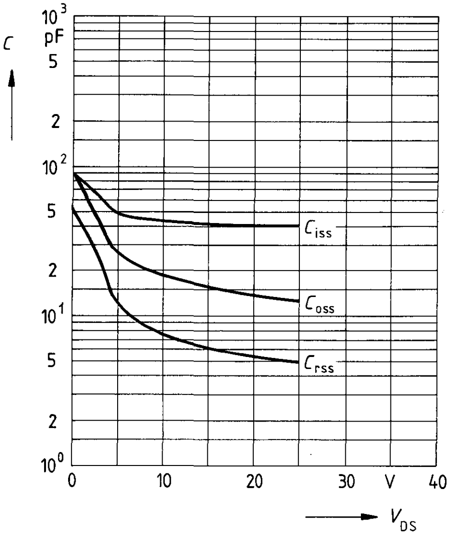
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



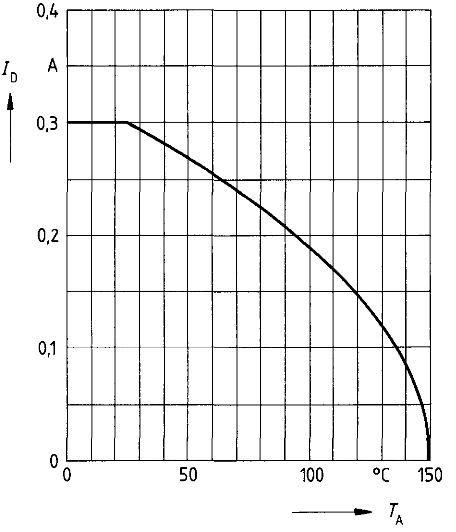
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



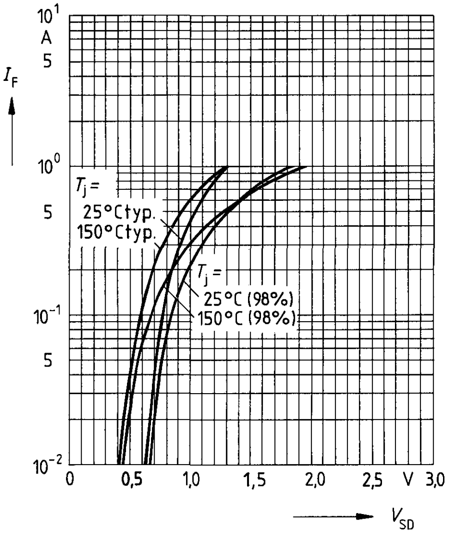
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 5V$



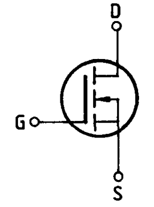
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

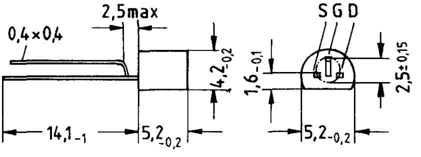
Drain-source voltage V_{DS} **= 100 V**
Continuous drain current I_D **= 250 mA**
Drain-source on-resistance $R_{DS(on)}$ **= 6,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 10 A3 in accordance with DIN 41 868 or TO 92 in accordance with JEDEC.
Approx. weight 0.2 g

Type	Ordering code
BSS 100	Q62702-S483



Dimensions in mm

Maximum ratings

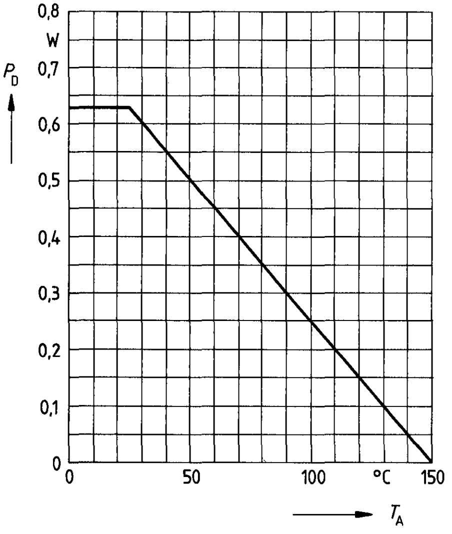
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,25	A	T_A = 25 °C
Pulsed drain current	I_{Dpuls}	1,0	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	0,63	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\,JA}$	≤200	K/W	

Electrical characteristics

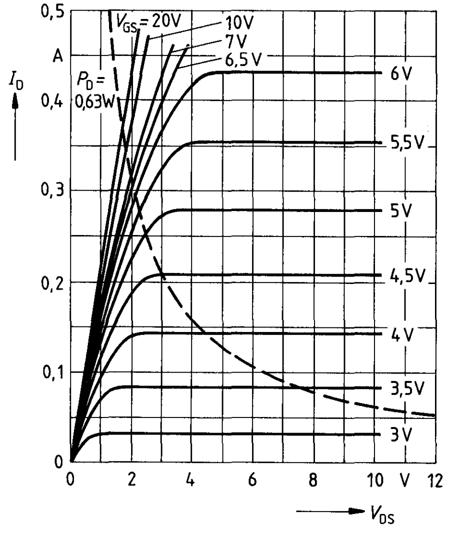
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2,2	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	1 2	15 60	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
		–	–	10	nA	T_j = 25 °C V_{DS} = 60V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	1	10		V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	5,0	6,0	Ω	V_{GS} = 10V I_D = 0,12A
Dynamic ratings						
Forward transconductance	g_{fs}	0,08	0,12	–	S	V_{DS} = 25V I_D = 0,12A
Input capacitance	C_{iss}	–	20	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	9,0	–		
Reverse transfer capacitance	C_{rss}	–	4,0	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = 30V I_D = 0,28A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	10	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	15	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,25	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	1,0		
Diode forward on-voltage	V_{SD}	–	1,1	1,3	V	I_F = 0,5A V_{GS} = 0V, T_j = 25 °C

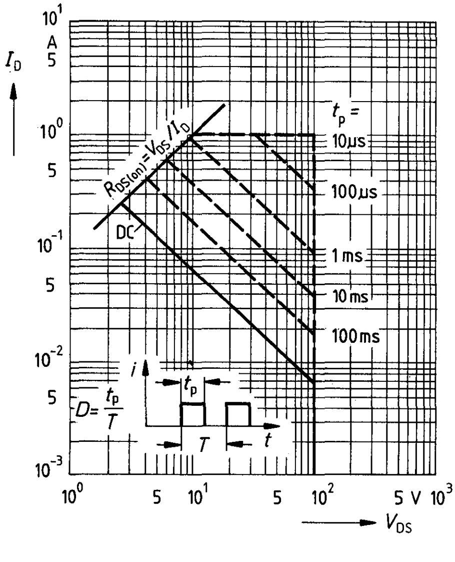
Power dissipation $P_D = f(T_A)$



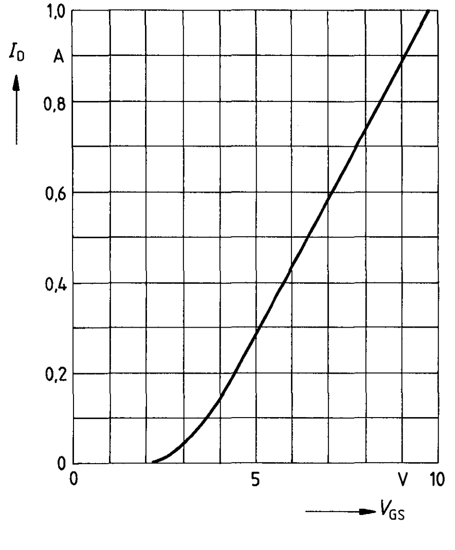
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



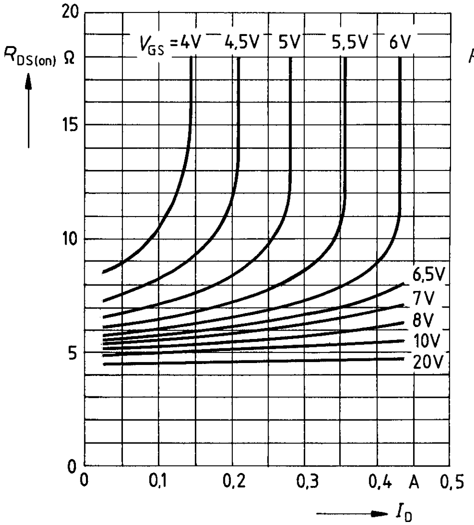
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



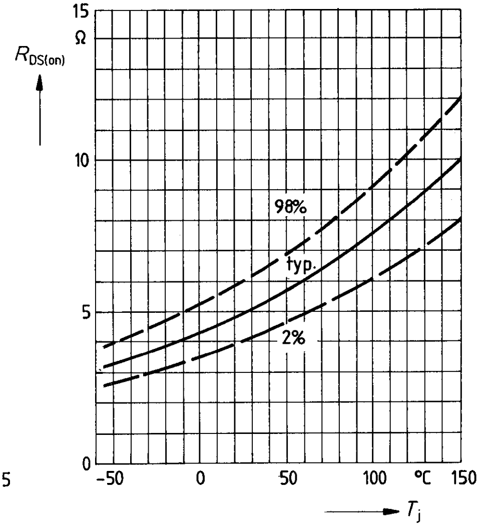
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



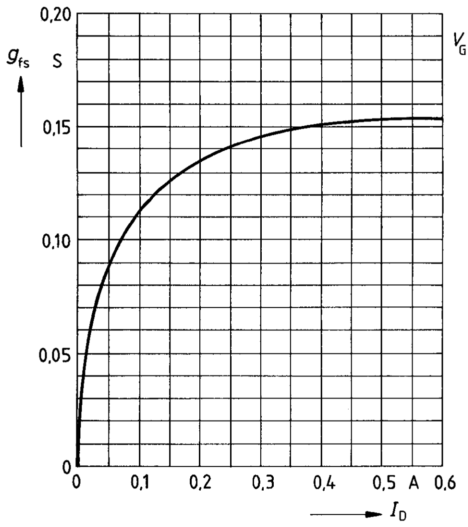
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



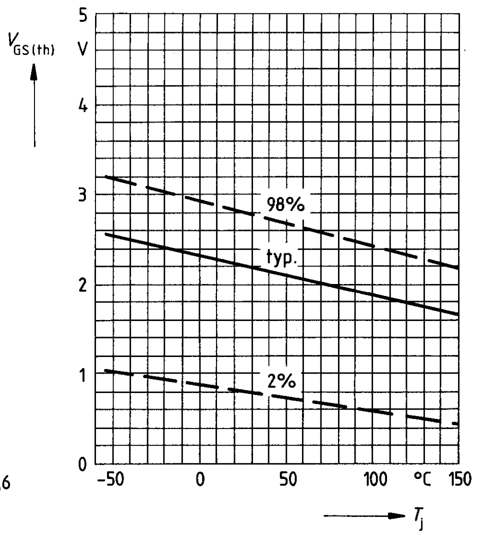
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 0.12A, V_{GS} = 10V
(spread)



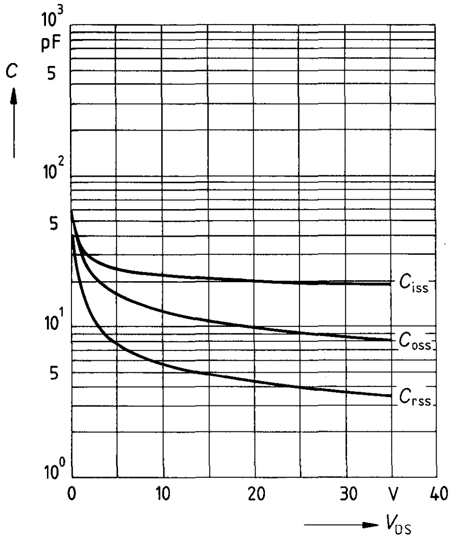
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



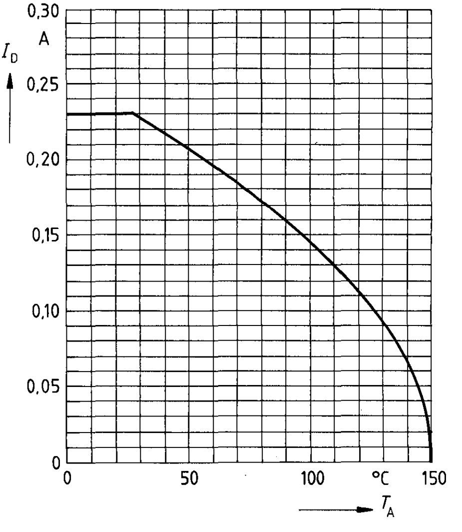
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



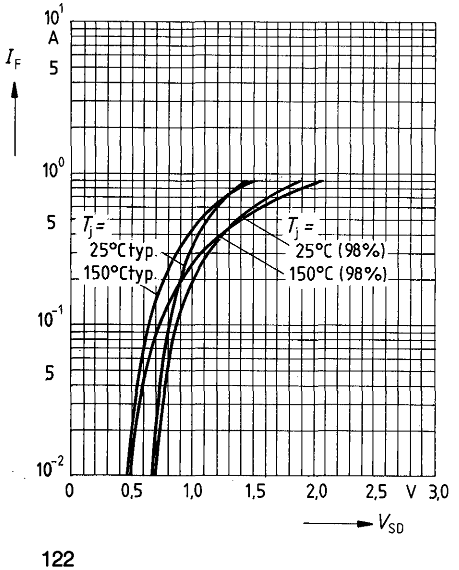
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 10V$

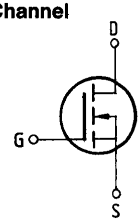


Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

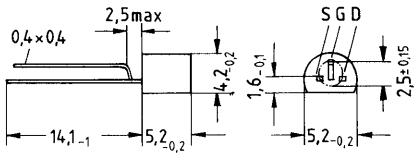
N-Channel



Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 160 mA**
Drain-source on-resistance $R_{DS(on)}$ **= 12 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package 10 A 3 in accordance with DIN 41 868
or TO 92 in accordance with JEDEC.
Approx. weight 0.2 g

Type	Ordering code
S BSS 101	Q62702-S484



Dimensions in mm

Maximum ratings

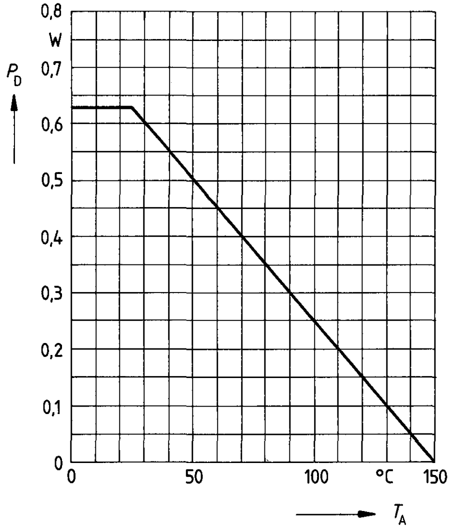
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,16	A	T_A = 25 °C
Pulsed drain current	I_{Dpuls}	0,64	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	0,63	W	T_A = 25 °C
Operating and storage	T_j	–55 ... +150		
temperature range	T_{stg}	E	°C	
DIN humidity category		55/150/56	–	DIN 40 040
IEC climatic category				DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\,JA}$	≤200	K/W	

S Preferred Type

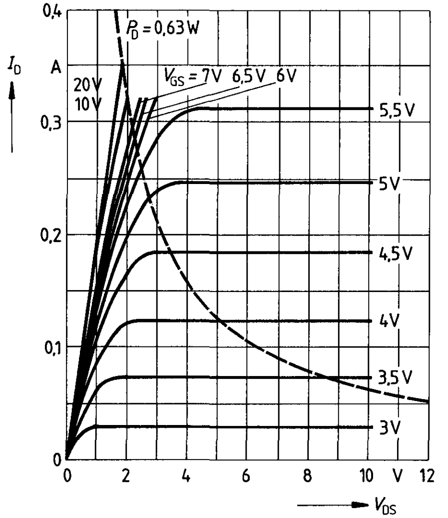
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2,2	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	1 2	15 60	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
		–	–	30	nA	T_j = 25 °C V_{DS} = 130V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	1	10		V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	11	12	Ω	V_{GS} = 10V I_D = 80mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,06	0,07	–	S	V_{DS} = 25V I_D = 80mA
Input capacitance	C_{iss}	–	20	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	6	–		
Reverse transfer capacitance	C_{rss}	–	2,5	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = 30V I_D = 0,27A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	10	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	15	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,16	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	0,64		
Diode forward on-voltage	V_{SD}	–	1,0	1,2	V	I_F = 0,32A V_{GS} = 0V, T_j = 25 °C

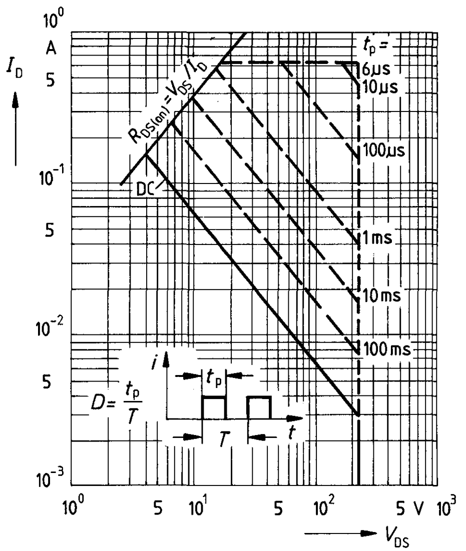
Power dissipation $P_D = f(T_A)$



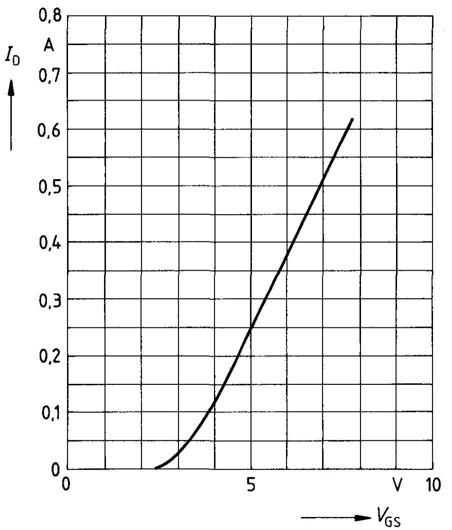
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



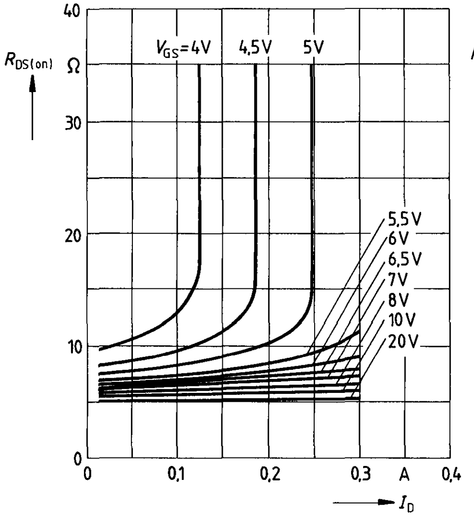
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



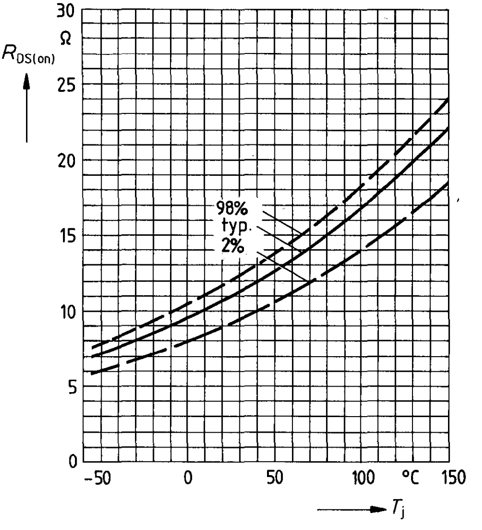
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



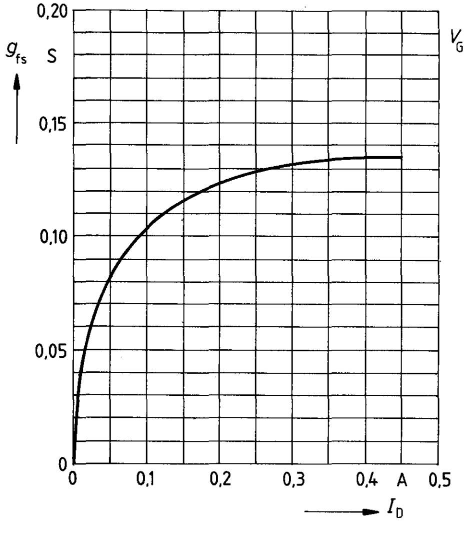
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



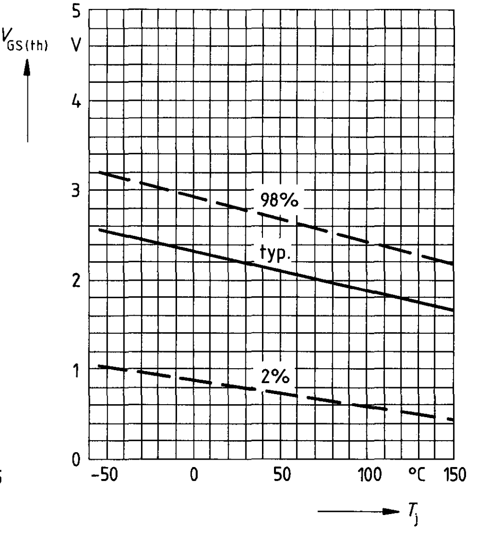
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 80mA, V_{GS} = 10V
(spread)



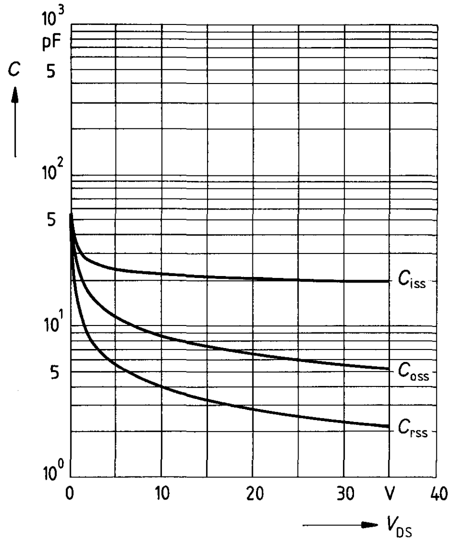
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



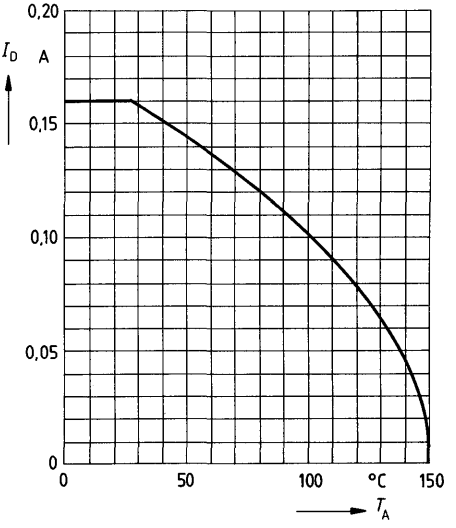
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



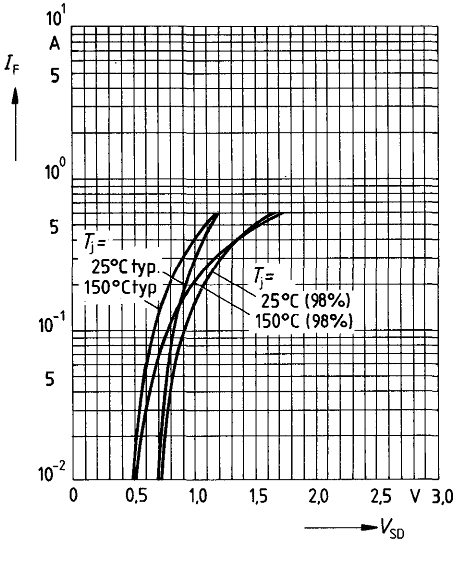
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 10V$



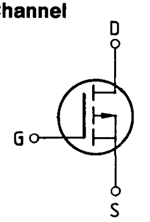
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

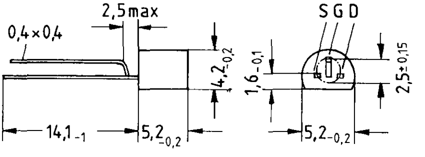
Drain-source voltage V_{DS} = **– 50 V**
Continuous drain current I_D = **– 170 mA**
Drain-source on-resistance $R_{DS(on)}$ = **10 Ω**

P-Channel



Description SIPMOS, P-channel, enhancement mode
Case Plastic package 10 A 3 in accordance with DIN 41 868 or TO 92 in accordance with JEDEC.
Approx. weight 0.2 g

Type	Ordering code
S BSS 110	Q62702-S489



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	– 50	V	
Drain-gate voltage	V_{DGR}	– 50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	– 0,17	A	T_A = 35 °C
Pulsed drain current	I_{Dpuls}	– 0,68	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	± 20	V	Aperiodic
Max. power dissipation	P_D	0,63	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\ JA}$	≤ 200	K/W	

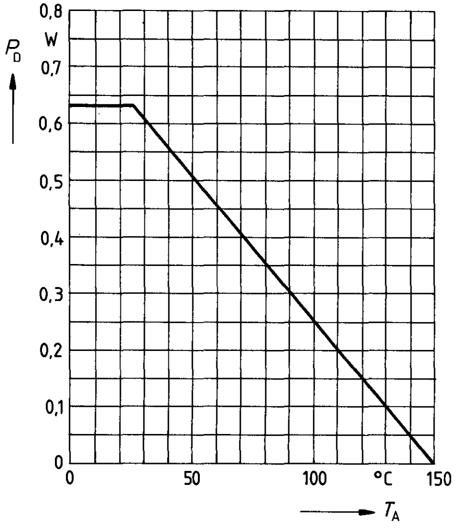
 S Preferred Type

Electrical characteristics

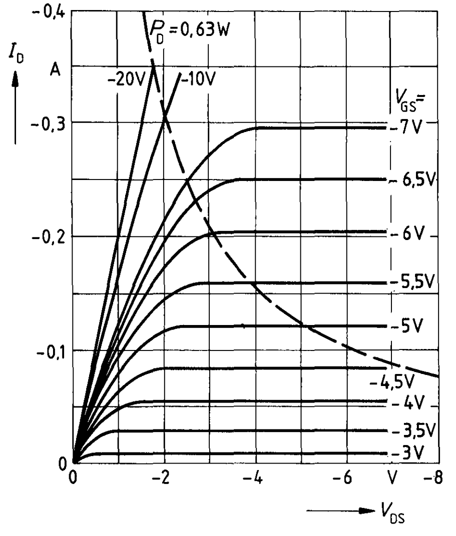
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	–50	–	–	V	V_{GS} = 0V I_D = –0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	–0,8	–2,4	–2,8		V_{DS} = V_{GS} I_D = –1,0mA
Zero gate voltage drain current	I_{DSS}	– –	–1 –2	–15 –60	µA	T_j = 25 °C T_j = 125 °C V_{DS} = – 50V V_{GS} = 0V
		–	–	–0,1		T_j = 25 °C V_{DS} = –25V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	–1	–10	nA	V_{GS} = –20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	6	10	Ω	V_{GS} = –10V I_D = – 0,1A
Dynamic ratings						
Forward transconductance	g_{fs}	0,05	0,07	–	S	V_{DS} = –25V I_D = – 0,1A
Input capacitance	C_{iss}	–	40	–	pF	V_{GS} = 0V V_{DS} = –25V f = 1MHz
Output capacitance	C_{oss}	–	15	–		
Reverse transfer capacitance	C_{rss}	–	6	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = –30V I_D = – 0,27A V_{GS} = –10V R_{GS} = 50Ω
	t_r	–	10	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	18	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	–0,17	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	–0,68		
Diode forward on-voltage	V_{SD}	–	–1	–1,2	V	I_F = –0,34A V_{GS} = 0V, T_j = 25 °C

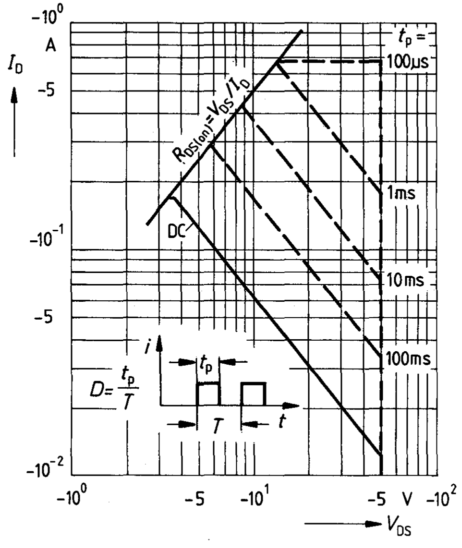
Power dissipation $P_D = f(T_A)$



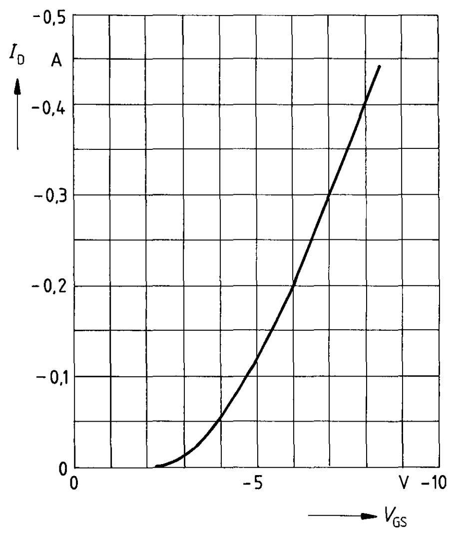
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 μs pulse test,
$T_j = 25\,°C$



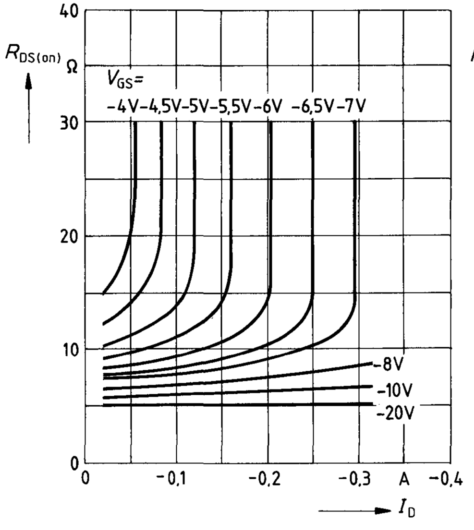
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



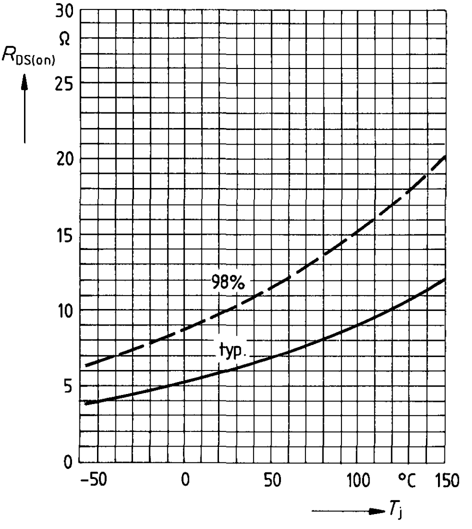
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 μs pulse test,
$V_{DS} = -25V$, $T_j = 25\,°C$



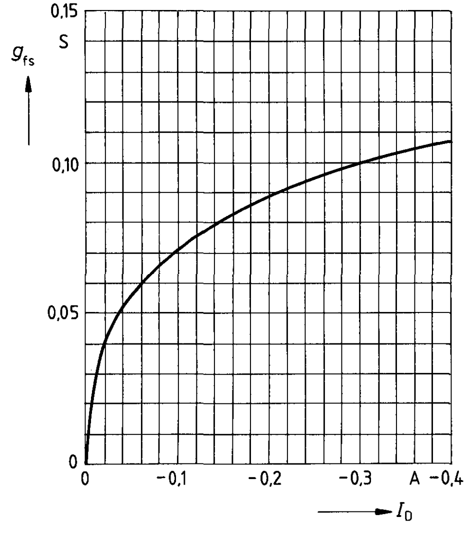
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



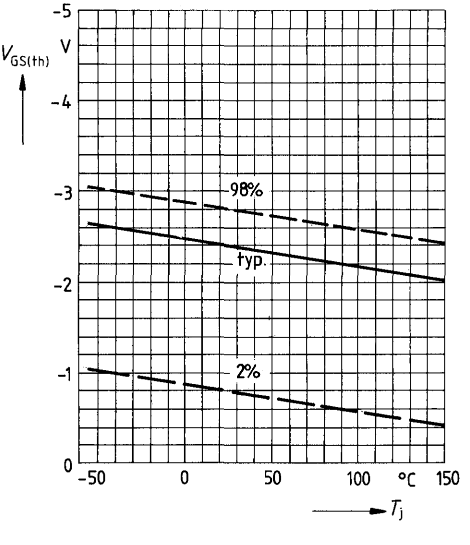
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = -0.1$A, $V_{GS} = -10$V
(spread)



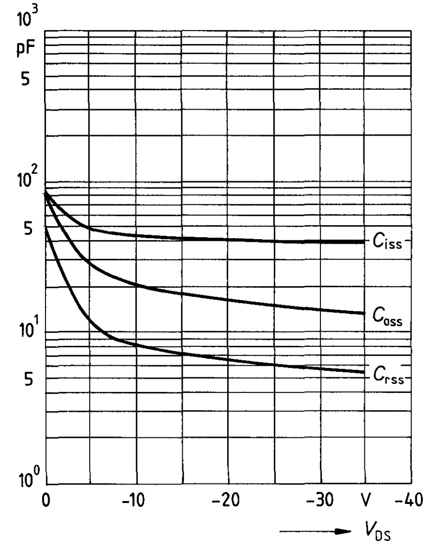
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = -25$V, $T_j = 25\,°C$



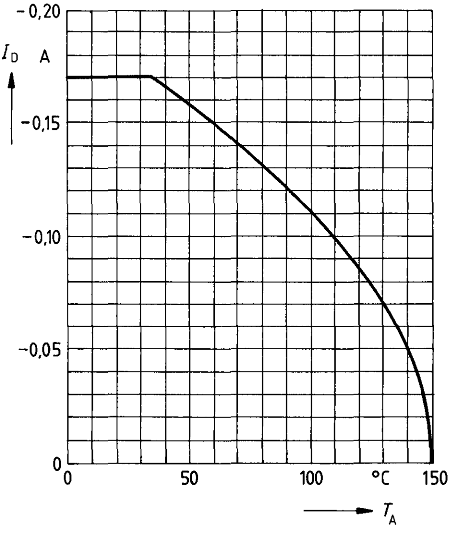
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = -1$mA
(spread)



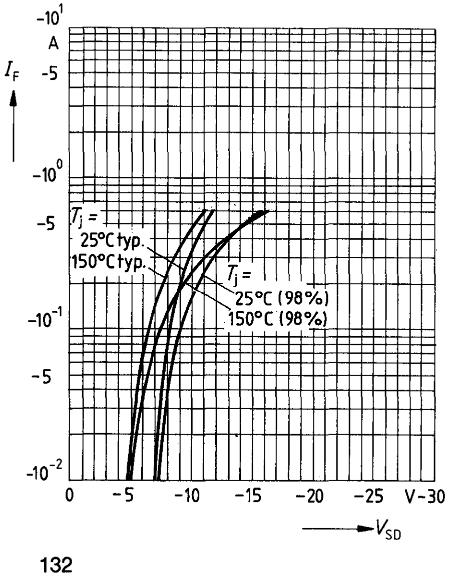
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq -10\text{V}$

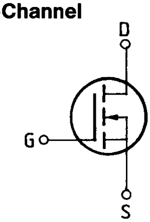


Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

N-Channel

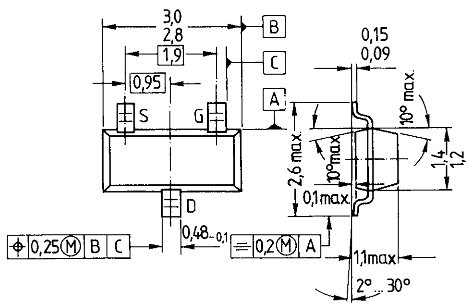


Drain-source voltage	V_{DS}	**= 100 V**
Continuous drain current	I_D	**= 170 mA**
Drain-source on-resistance	$R_{DS(on)}$	**= 6 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 23 A 3 in accordance with DIN 41 869 or SOT 23 in accordance with JEDEC.
Approx. weight 0,02 g

Type	Marking	Ordering code for versions in bulk	Ordering code for versions on 8 mm tape
S BSS 123	SA	Q62702-S507	Q62702-S512



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,17	A	T_A = 50 °C
Pulsed drain current	I_{Dpuls}	0,68	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	0,36	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\,JA}$	≤350	K/W	
Chip-substrate reverse side for package mounted on alumina 15 mm × 16.7 mm × 0.7 mm	$R_{th\,JSR}$	≤285	K/W	

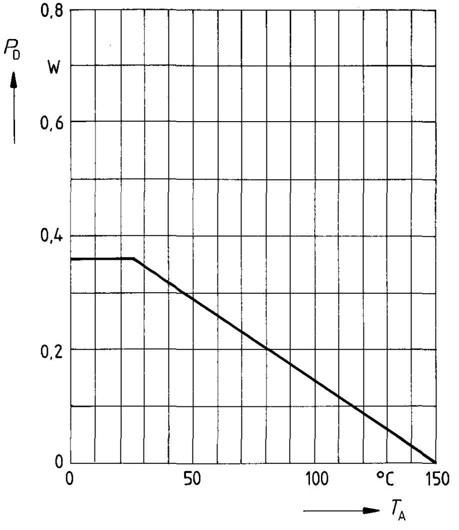
S Preferred Type

Electrical characteristics

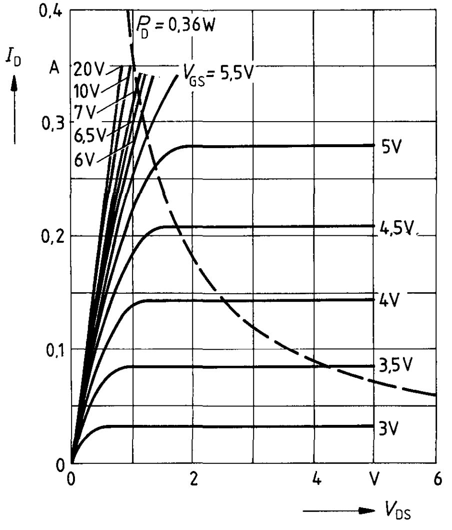
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2,2	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	1 2	15 60	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
		–	–	10	nA	T_j = 25 °C V_{DS} = 20V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	50		V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	5,0	6,0	Ω	V_{GS} = 10V I_D = 100mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,08	0,12	–	S	V_{DS} = 25V I_D = 100mA
Input capacitance	C_{iss}	–	20	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	9	–		
Reverse transfer capacitance	C_{rss}	–	4	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = 30V I_D = 0,28A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	10	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	15	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,17	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	0,68		
Diode forward on-voltage	V_{SD}	–	1,1	1,3	V	I_F = 0,34A V_{GS} = 0V, T_j = 25 °C

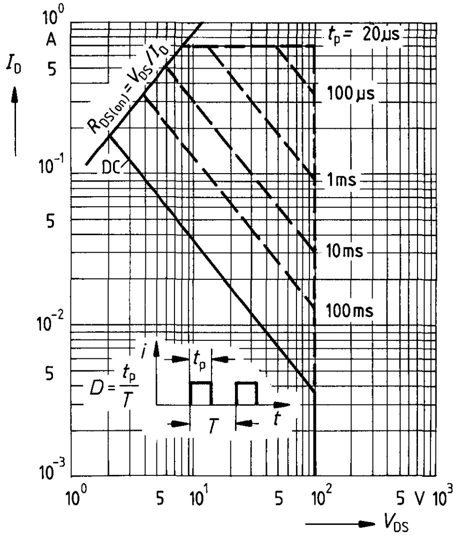
Power dissipation $P_D = f(T_A)$



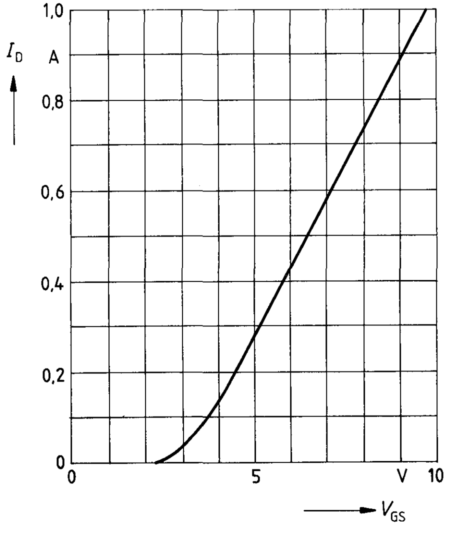
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



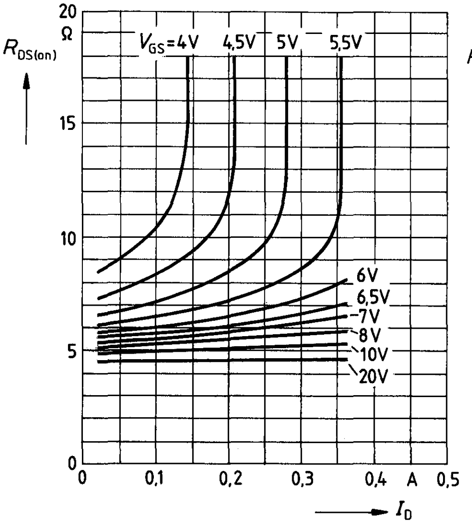
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



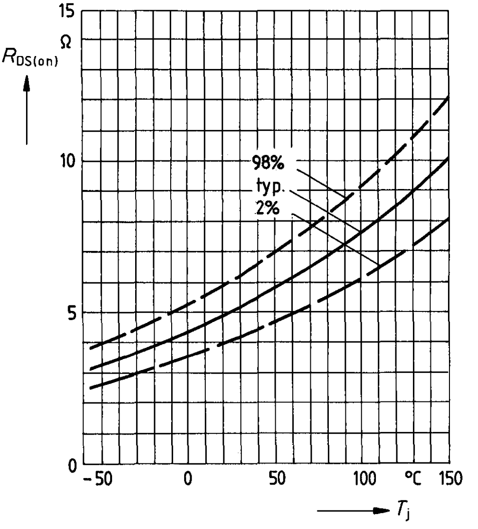
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



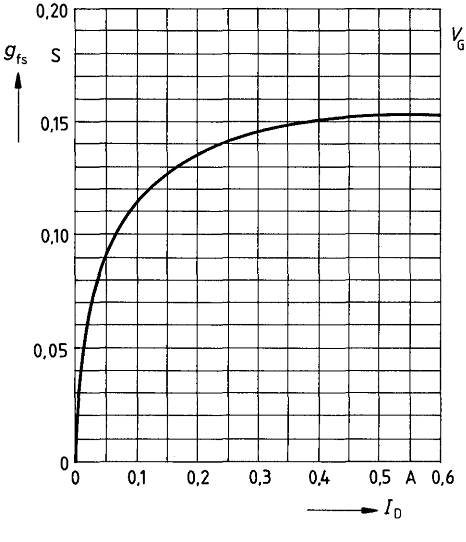
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



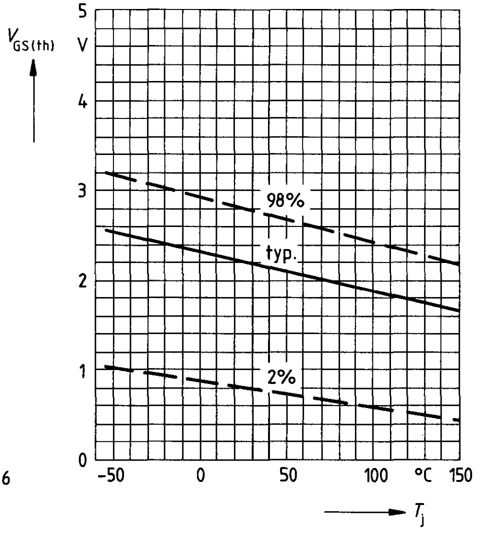
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 100mA, V_{GS} = 10V
(spread)



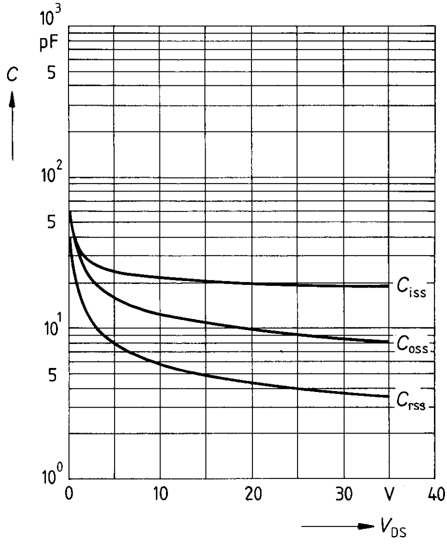
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



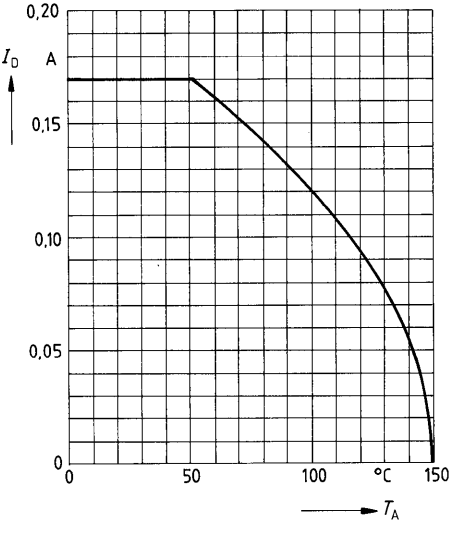
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



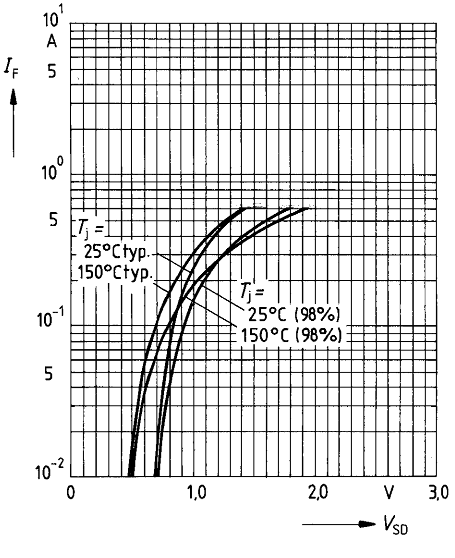
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 10\text{V}$

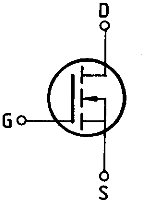


Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

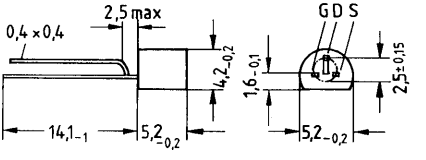
N-Channel



Drain-source voltage V_{DS} = **600 V**
Continuous drain current I_D = **100 mA**
Drain-source on-resistance $R_{DS(on)}$ = **40 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package 10 A 3 in accordance with DIN 41 868
or TO 92 in accordance with JEDEC.
Approx. weight 0.2 g

Type	Ordering code
BSS 125	Q62702-S505



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	600	V	
Drain-gate voltage	V_{DGR}	600	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,10	A	T_A = 35 °C
Pulsed drain current	I_{Dpuls}	0,40	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	1,0	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

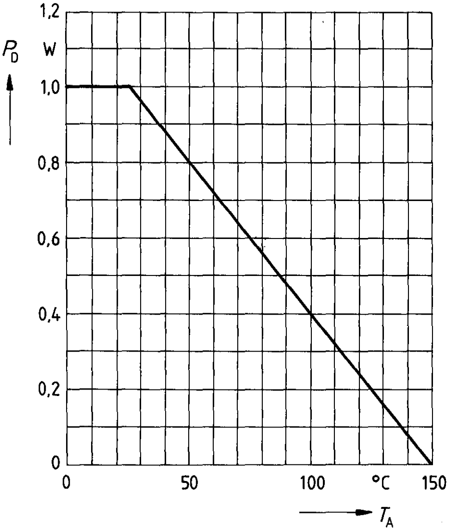
Description	Symbols	Ratings	Units	Conditions
Chip – ambient	$R_{th JA}$	≤125	K/W	

Electrical characteristics

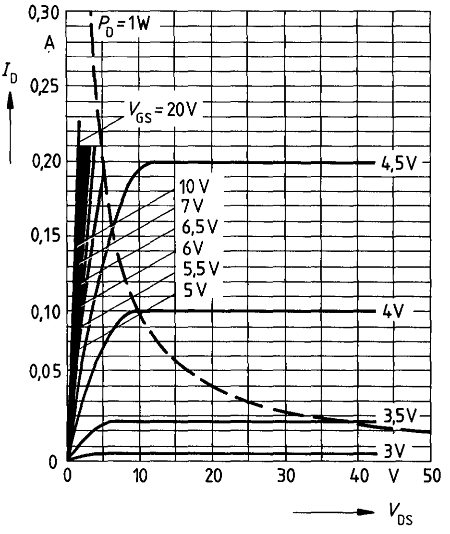
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	600	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	4 8	60 200	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 600V V_{GS} = 0V
		–	–	1,0	µA	T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	1	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	18	40	Ω	V_{GS} = 10V I_D = 60mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,06	0,14	–	S	V_{DS} = 25V I_D = 60mA
Input capacitance	C_{ies}	–	75	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{DSS}	–	10	–		
Reverse transfer capacitance	C_{TSG}	–	4	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = 30V I_D = 0,21A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	10	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	15	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,1	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	0,4		
Diode forward on-voltage	V_{SD}	–	0,8	1,3	V	I_F = 0,2A V_{GS} = 0V, T_j = 25 °C

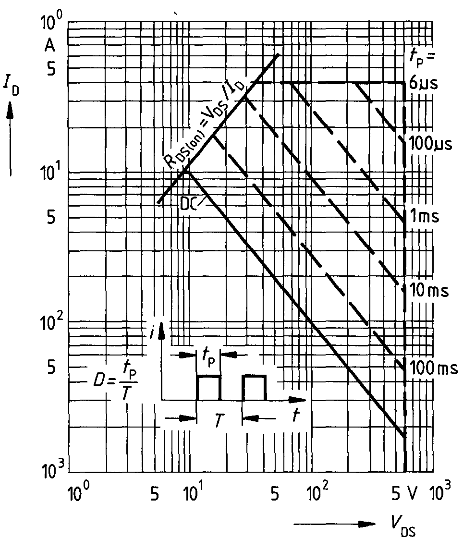
Power dissipation $P_D = f(T_A)$



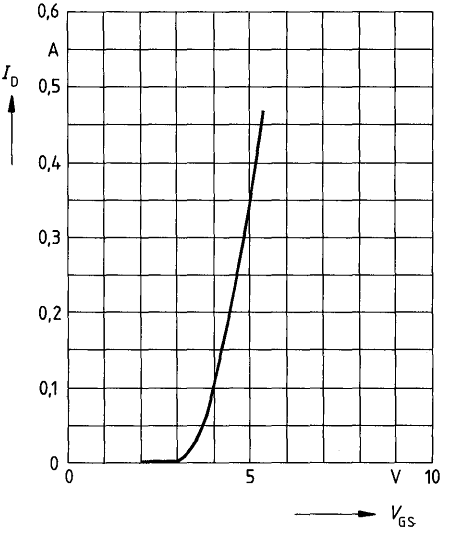
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



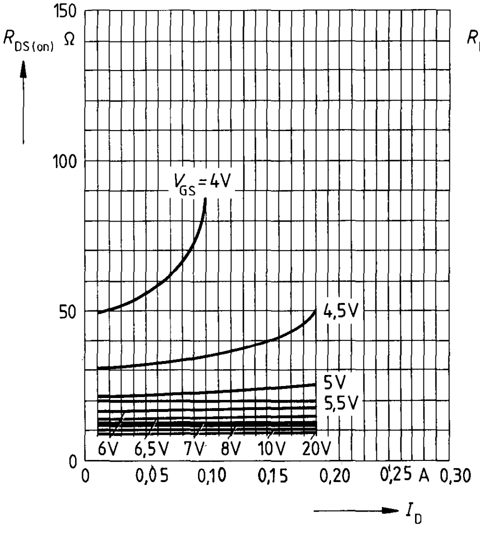
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



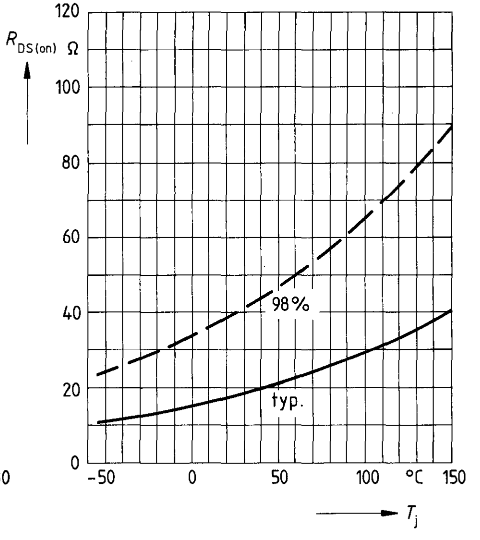
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



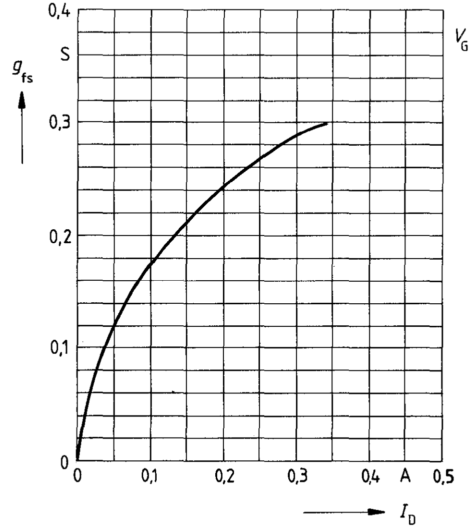
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



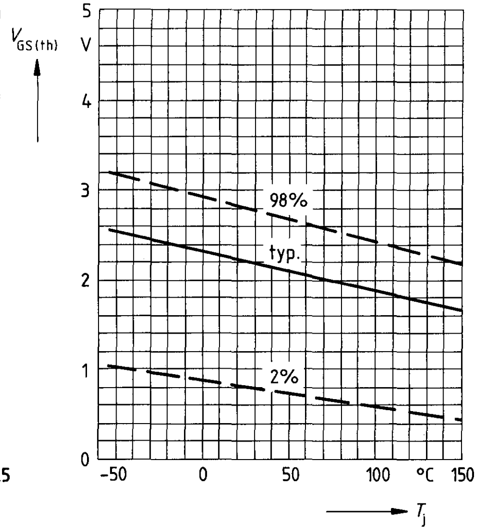
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 0.06A, V_{GS} = 10V
(spread)



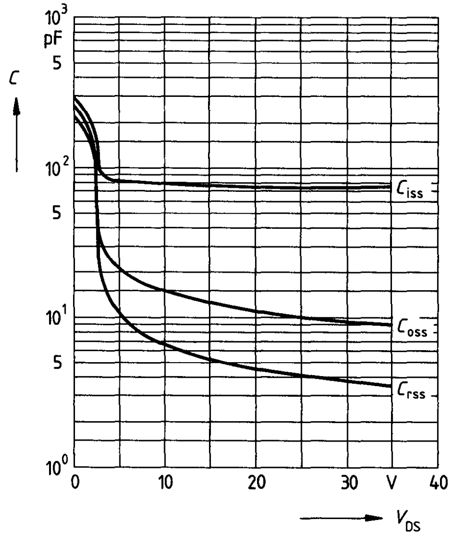
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



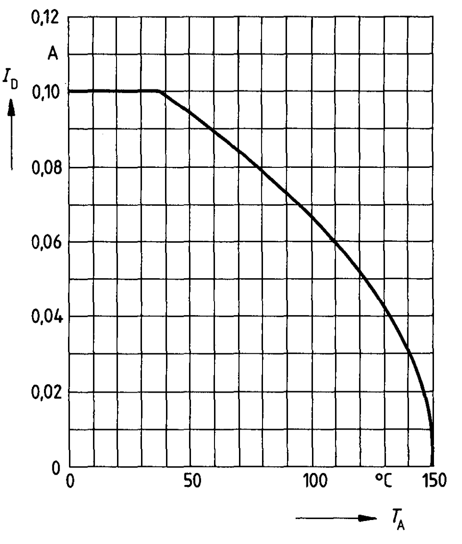
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



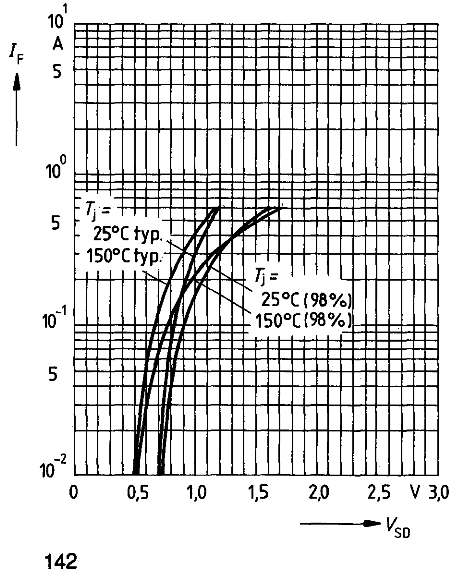
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 10V$

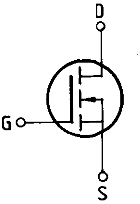


Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

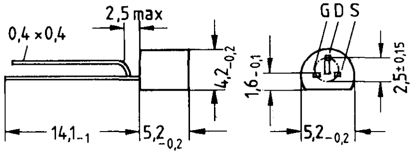
N-Channel



Drain-source voltage V_{DS} **= 230 V**
Continuous drain current I_D **= 150 mA**
Drain-source on-resistance $R_{DS(on)}$ **= 20 Ω**

Description SIPMOS, N-channel, depletion mode
Case Plastic package 10 A 3 in accordance with DIN 41 868
or TO 92 in accordance with JEDEC.
Approx. weight 0.2 g

Type	Ordering code
BSS 129	Q62702-S510



Dimensions in mm

Maximum ratings

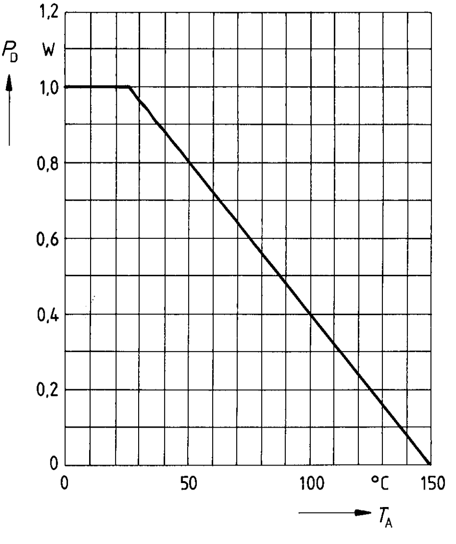
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	230	V	
Drain-gate voltage	V_{DGR}	230	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	0,15	A	T_A = 35 °C
Pulsed drain current	I_{Dpuls}	0,6	A	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	1	W	T_A = 25 °C
Operating and storage	T_j			
temperature range	T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\ JA}$	≤125	K/W	

Electrical characteristics

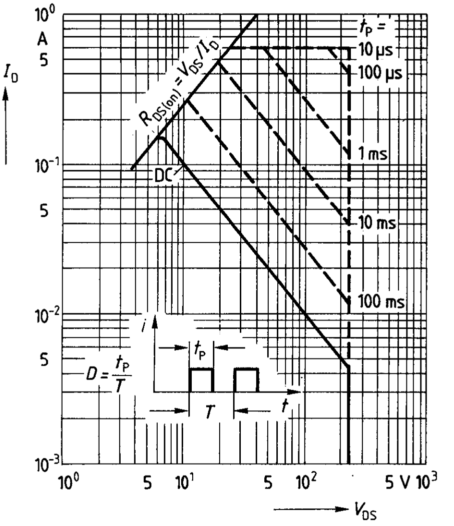
(at $T_j = 25\,°C$ unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	230	–	–	V	V_{GS} = –3V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	–	–1	–0,7		V_{DS} = 3V I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	– –	100 200	nA µA	T_j = 25 °C T_j = 125 °C V_{DS} = 230V V_{GS} = –3V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	–	20	Ω	V_{GS} = 0V I_D = 14mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,14	0,2	–	S	V_{DS} = 25V I_D = 0,25A
Input capacitance	C_{iss}	–	110	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	20	–		
Reverse transfer capacitance	C_{rss}	–	5	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = 30V I_D = 0,25A V_{GS} = –2V… +5V R_{GS} = 50Ω
	t_r	–	15	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	80	–		
	t_f	–	150	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,15	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	1,0		
Diode forward on-voltage	V_{SD}	–	1,0	1,4	V	I_F = 0,3A V_{GS} = 0V

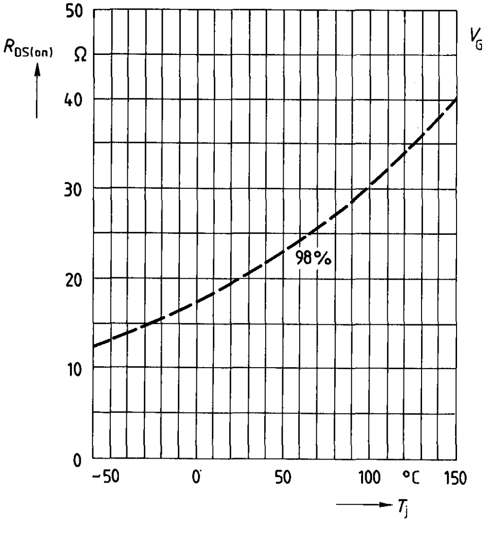
Power dissipation $P_D = f(T_A)$



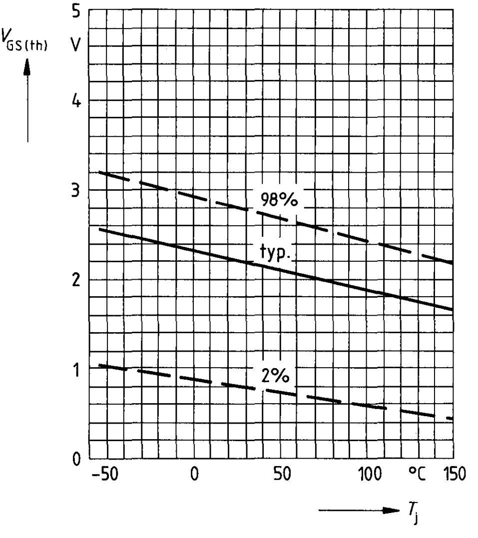
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25°C$



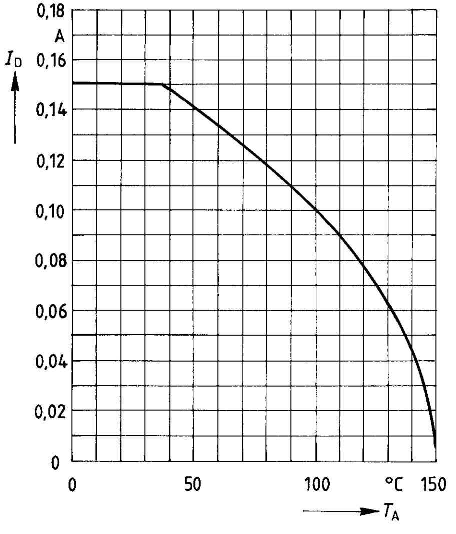
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 4.2A$, $V_{GS} = 10V$
(spread)



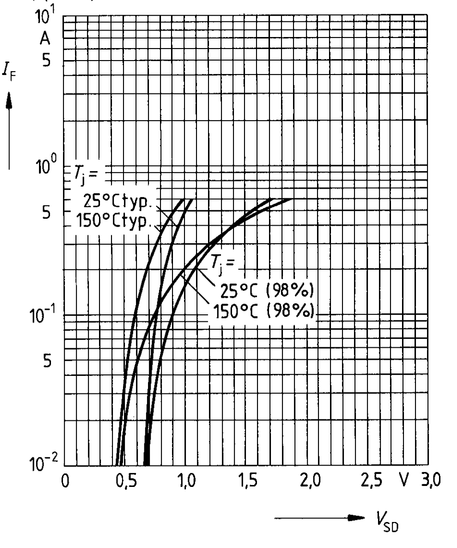
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 10V$

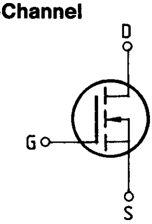


Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, t_p = 80 µs
(spread)



Main ratings

N-Channel

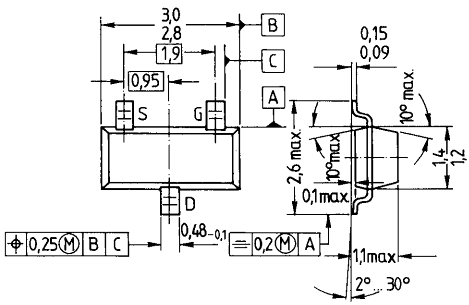


Drain-source voltage	V_{DS}	**= 240 V**
Continuous drain current	I_D	**= 100 mA**
Drain-source on-resistance	$R_{DS(on)}$	**= 16 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 23 A 3 in accordance with DIN 41 869 or SOT 23 in accordance with JEDEC.
Approx. weight 0,02 g

Type	Marking	Ordering code for versions in bulk	Ordering code for versions on 8 mm tape
BSS 131	SR	Q62702-S554	Q62702-S565



Dimensions in mm

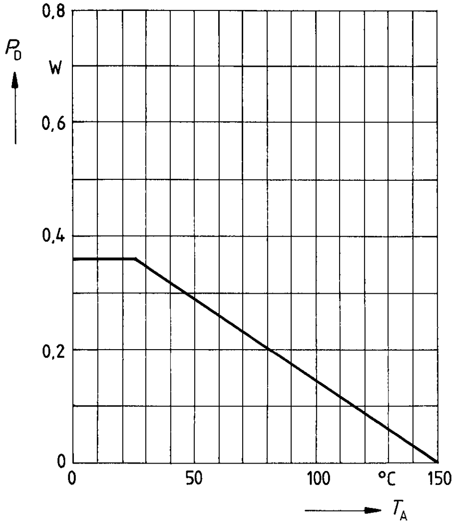
Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	240	V	
Drain-gate voltage	V_{DGR}	240	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	100	mA	T_A = 35 °C
Pulsed drain current	I_{Dpuls}	400	mA	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	0,36	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\ JA}$	≤350	K/W	
Chip-substrate reverse side for package mounted on alumina 15 mm × 16.7 mm × 0.7 mm	$R_{th\ JSR}$	≤285	K/W	

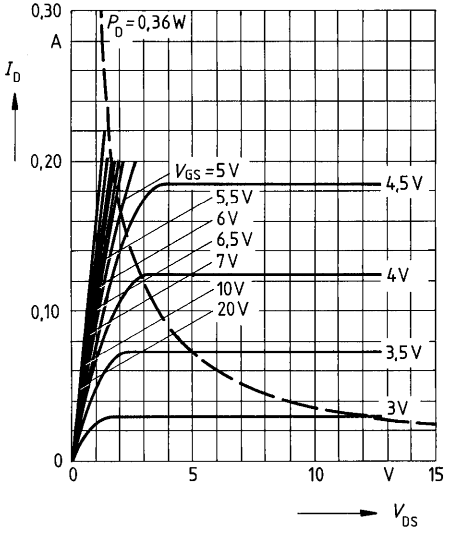
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	240	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,8	2,0	2,8		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	1 2	15 60	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 240V V_{GS} = 0V
		–	–	30	nA	T_j = 25 °C V_{DS} = 130V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	1	10	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	14	16	Ω	V_{GS} = 10V I_D = 100mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,06	0,10	–	S	V_{DS} = 25V I_D = 100mA
Input capacitance	C_{iss}	–	20	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	6	–		
Reverse transfer capacitance	C_{rss}	–	2,5	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	10	–	ns	V_{CC} = 30V I_D = 0,26A V_{GS} = 5V R_{GS} = 50Ω
	t_r	–	10	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	15	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,1	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	0,4		
Diode forward on-voltage	V_{SD}	–	1,1	1,2	V	I_F = 0,2A V_{GS} = 0V

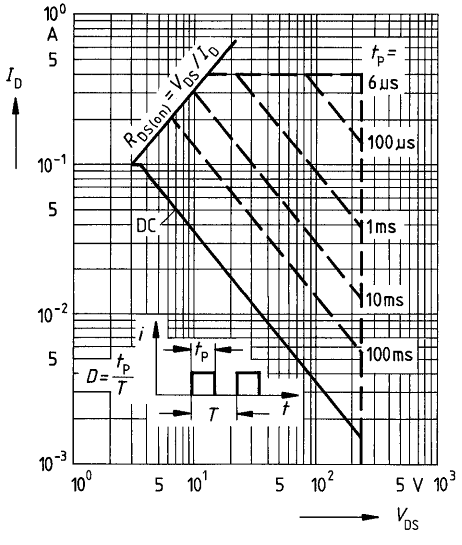
Power dissipation $P_D = f(T_A)$



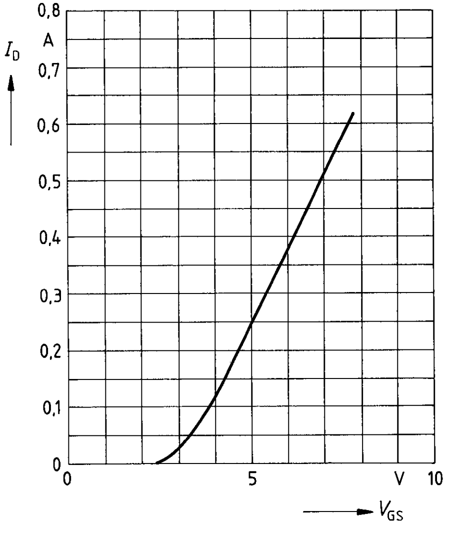
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



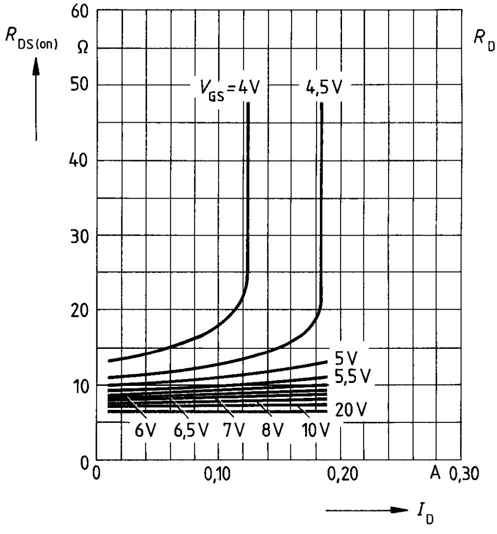
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



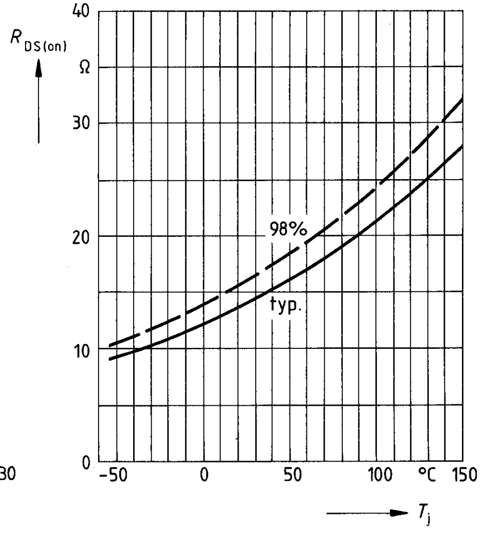
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



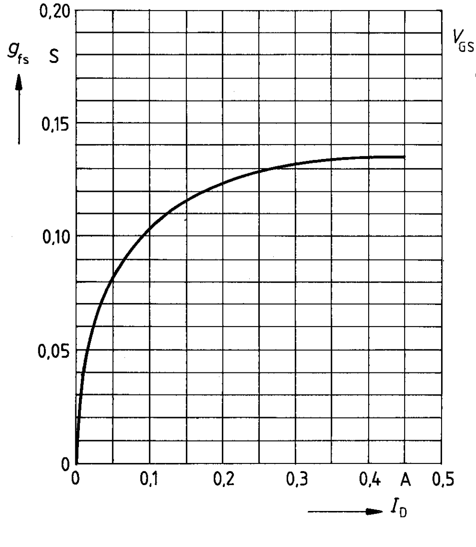
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



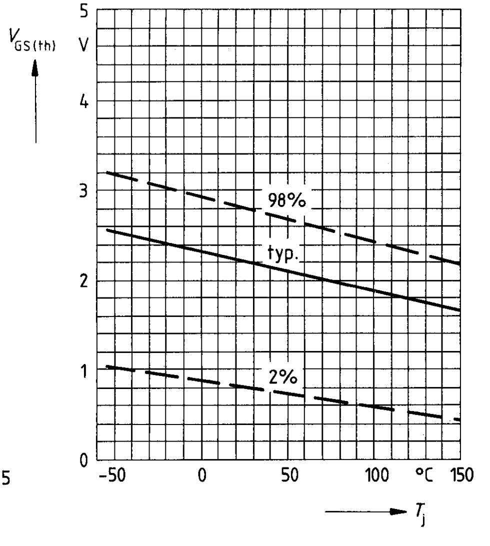
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 0.1A$, $V_{GS} = 10V$
(spread)



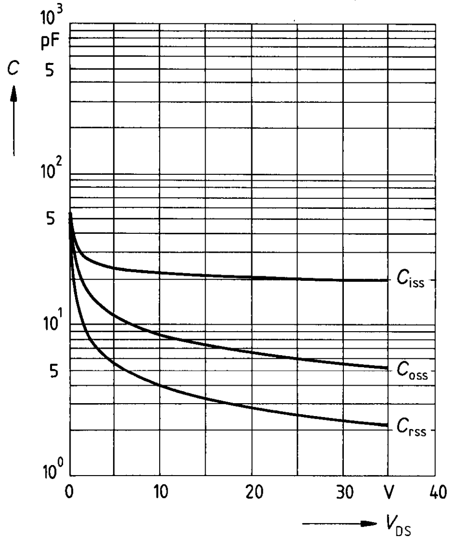
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



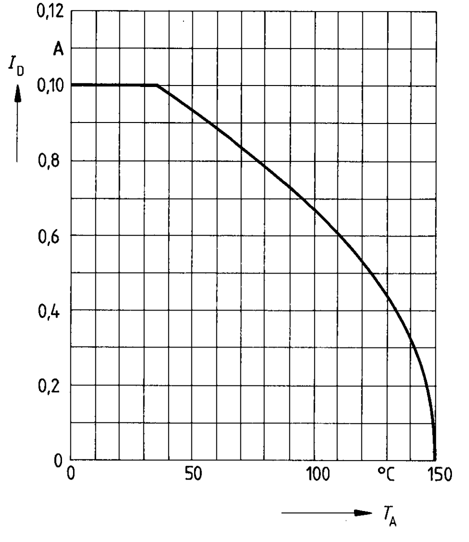
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



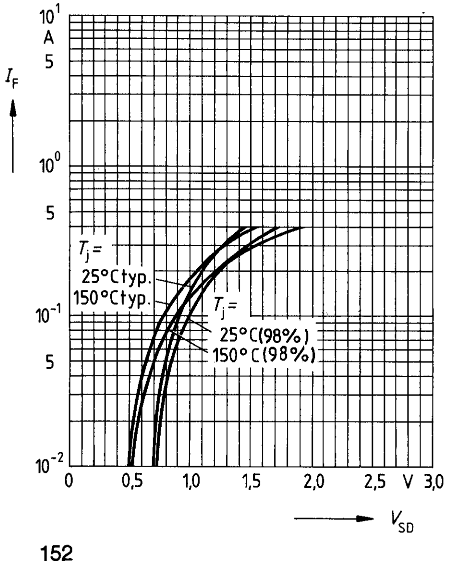
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 10V$



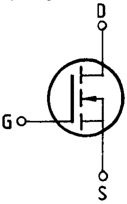
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Main ratings

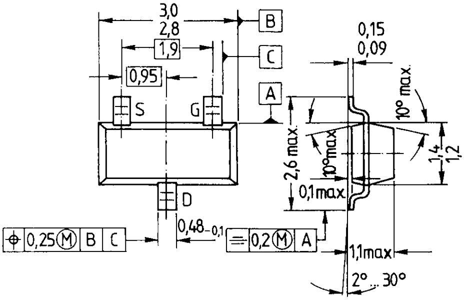
Drain-source voltage V_{DS} **= 50 V**
Continuous drain current I_D **= 200 mA**
Drain-source on-resistance $R_{DS(on)}$ **= 3,5 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 23 A 3 in accordance with DIN 41 869 or SOT 23 in accordance with JEDEC.
Approx. weight 0,02 g

Type	Marking	Ordering code for versions in bulk	Ordering code for versions on 8 mm tape
BSS 138	SS	Q62702-S558	Q62702-S566



Dimensions in mm

Maximum ratings

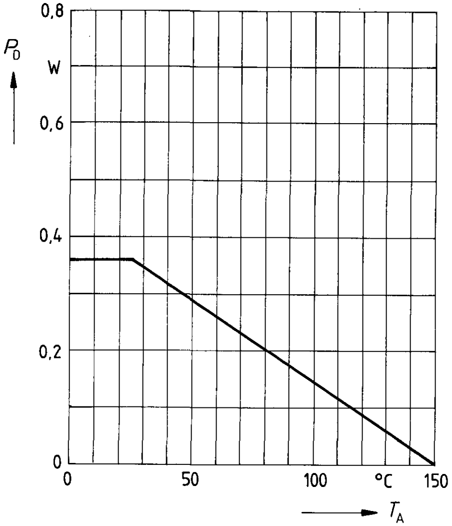
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	200	mA	T_A = 50 °C
Pulsed drain current	I_{Dpuls}	800	mA	T_A = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Aperiodic
Max. power dissipation	P_D	0,36	W	T_A = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – ambient	$R_{th\ JA}$	≤350	K/W	
Chip-substrate reverse side for package mounted on alumina 15 mm × 16.7 mm × 0.7 mm	$R_{th\ JSR}$	≤285	K/W	

Electrical characteristics

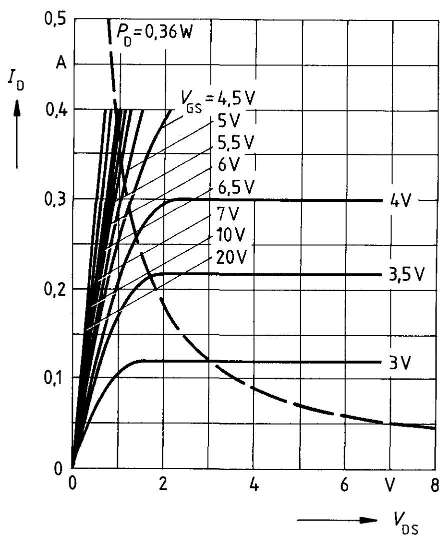
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	0,5	1,0	1,5		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	– –	0,5 5,0	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
		–	–	100	nA	T_j = 25 °C V_{DS} = 25V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-state resistance	$R_{DS\,(on)}$	–	2,0	3,5	Ω	V_{GS} = 5V I_D = 200mA
Dynamic ratings						
Forward transconductance	g_{fs}	0,12	0,2	–	S	V_{DS} = 25V I_D = 200mA
Input capacitance	C_{iss}	–	40	–	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	12	–		
Reverse transfer capacitance	C_{rss}	–	5	–		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	8	–	ns	V_{CC} = 30V I_D = 290mA V_{GS} = 5V R_{GS} = 50Ω
	t_r	–	8	–		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	16	–		
	t_f	–	25	–		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	0,2	A	T_A = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	0,8		
Diode forward on-voltage	V_{SD}	–	1,1	1,4	V	I_F = 0,4A V_{GS} = 0V

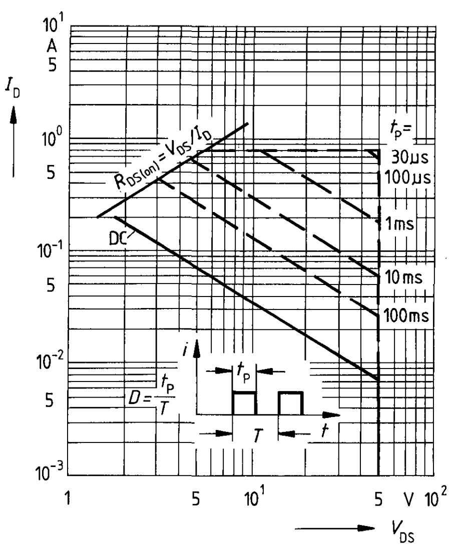
Power dissipation $P_D = f(T_A)$



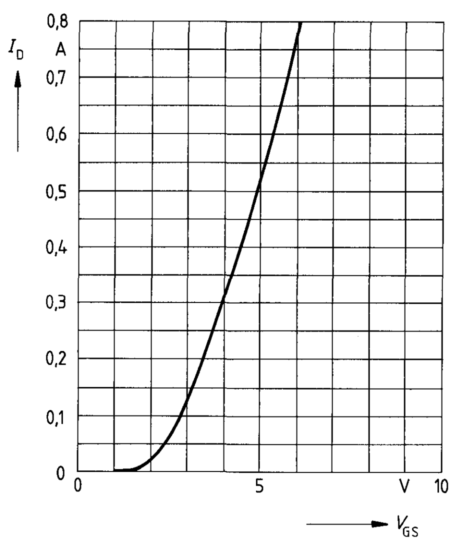
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



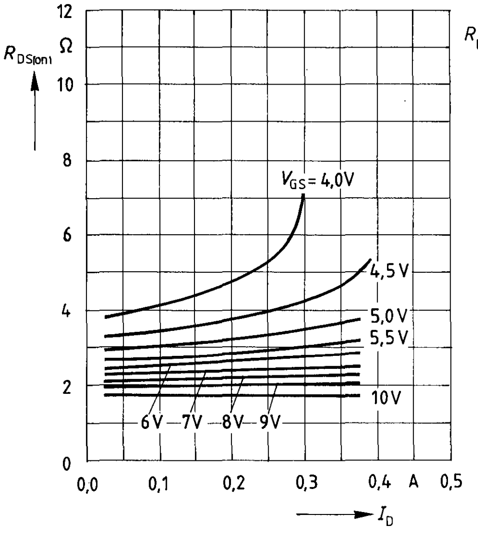
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



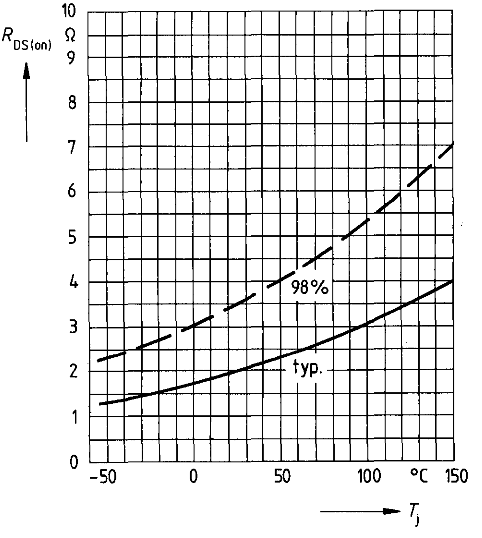
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



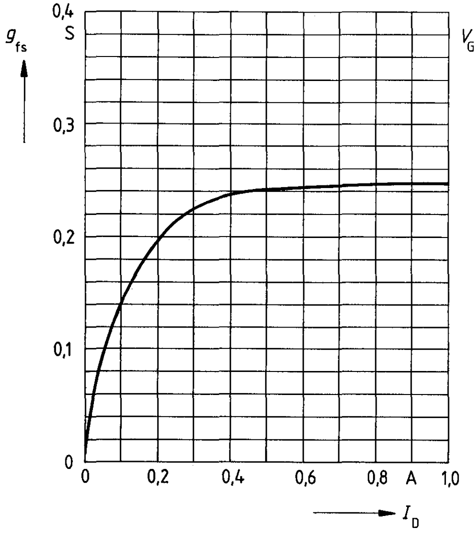
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



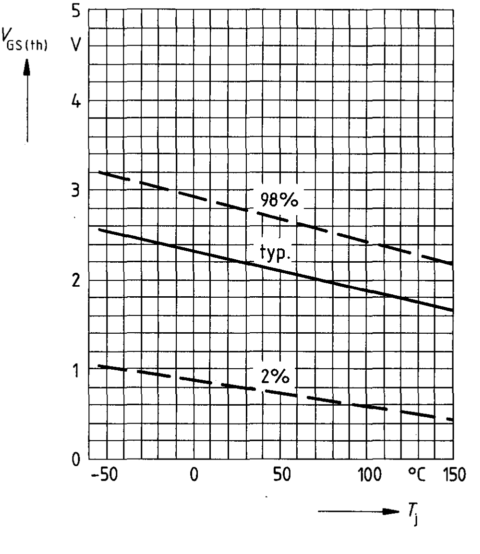
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 0.2A$, $V_{GS} = 5V$
(spread)



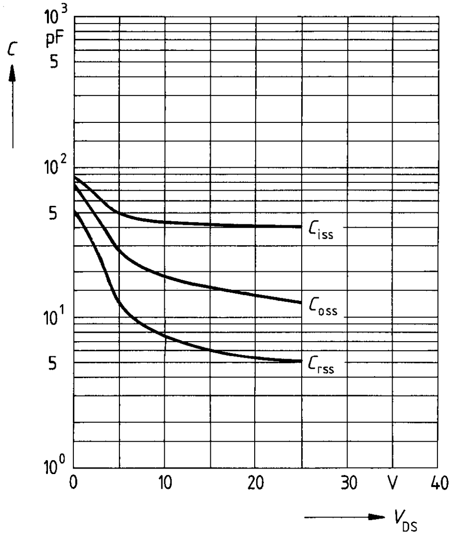
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



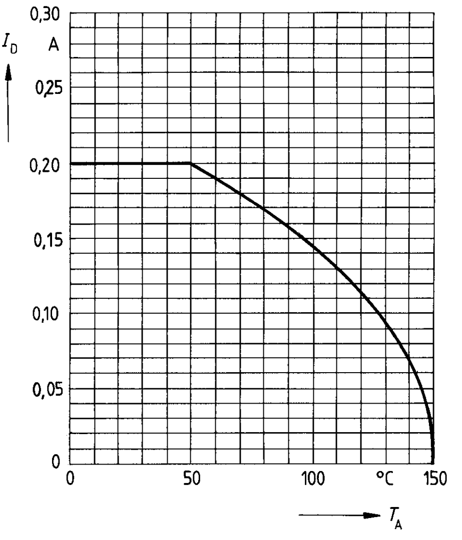
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



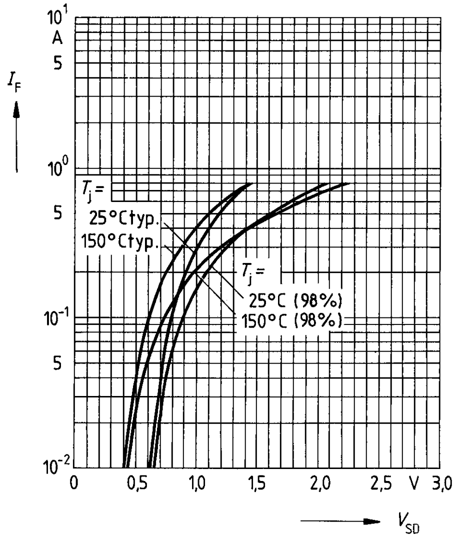
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



Continuous drain current $I_D = f(T_A)$
parameter: $V_{GS} \geq 5V$



Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Power Transistors

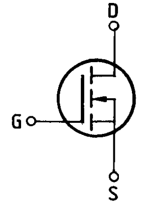
BUZ 10 . . .
BUZ 78

BUZ 80 . . .
BUZ 385

Main ratings

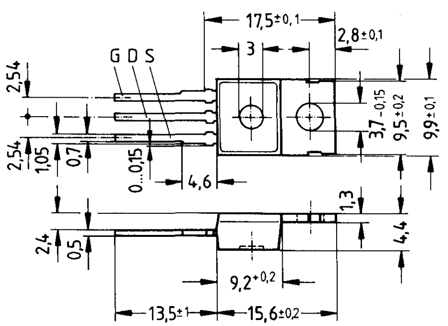
Drain-source voltage V_{DS} **= 50 V**
Continuous drain current I_D **= 20 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,08 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
BUZ 10	C67078-A1300-A2



Dimensions in mm

Maximum ratings

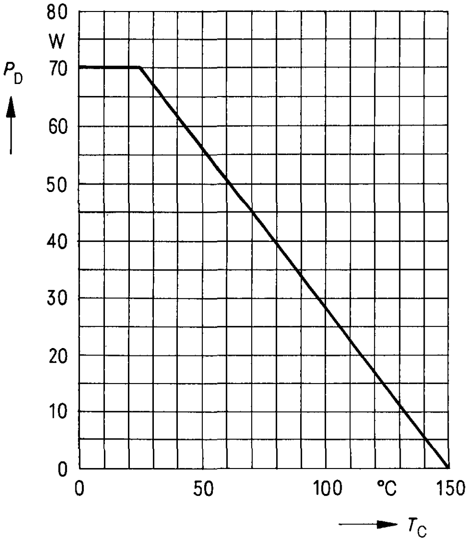
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	20	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	80	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	70	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,78	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

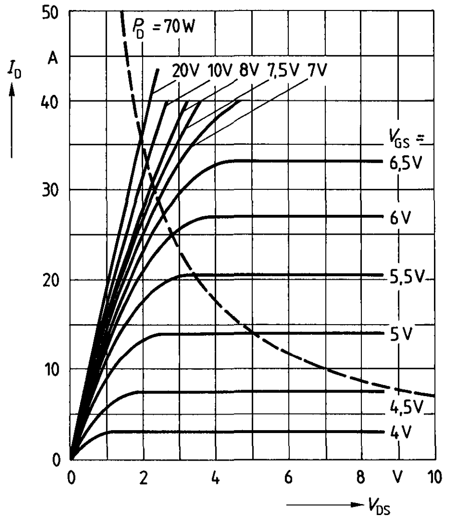
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	μA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,06	0,08	Ω	V_{GS} = 10V I_D = 13A
Dynamic ratings						
Forward transconductance	g_{fs}	8,0	13,0	–	S	V_{DS} = 25V I_D = 13A
Input capacitance	C_{iss}	–	940	1250	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	500	750		
Reverse transfer capacitance	C_{rss}	–	180	270		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	25	40	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	60	90		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	100	130		
	t_f	–	75	95		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	20	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	80		
Diode forward on-voltage	V_{SD}	–	1,2	1,5	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	150	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/μs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,0	–	μC	

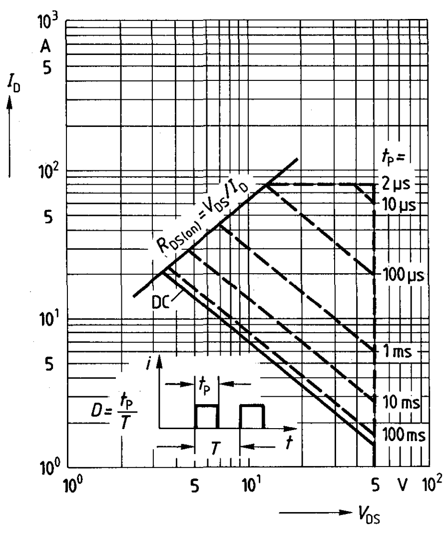
Power dissipation $P_D = f(T_C)$



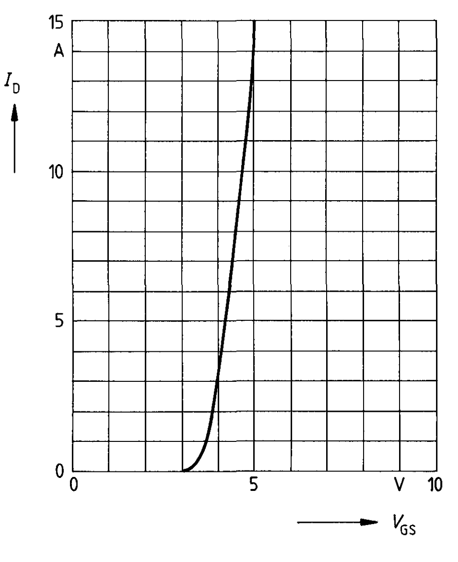
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



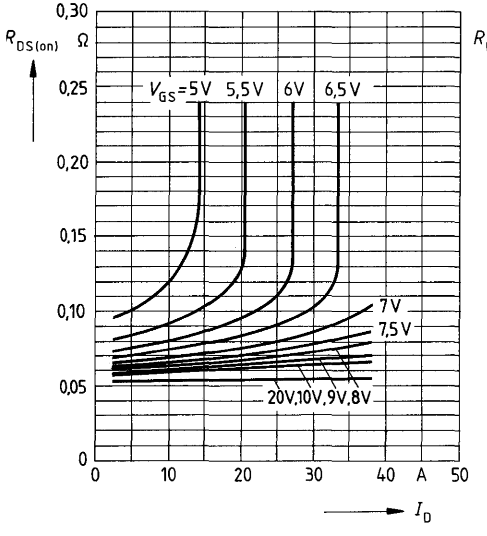
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



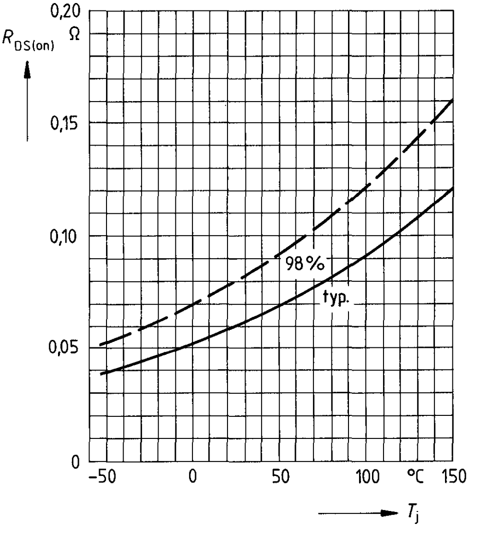
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



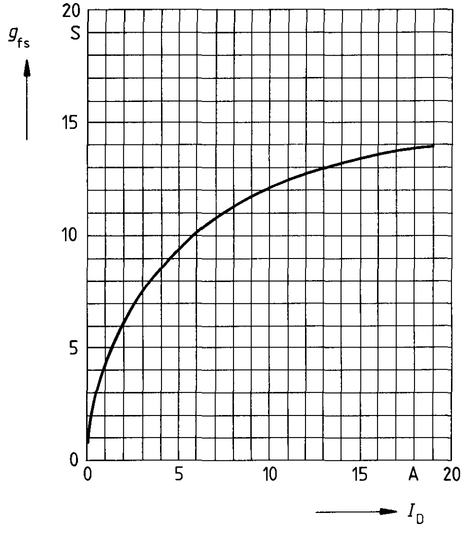
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



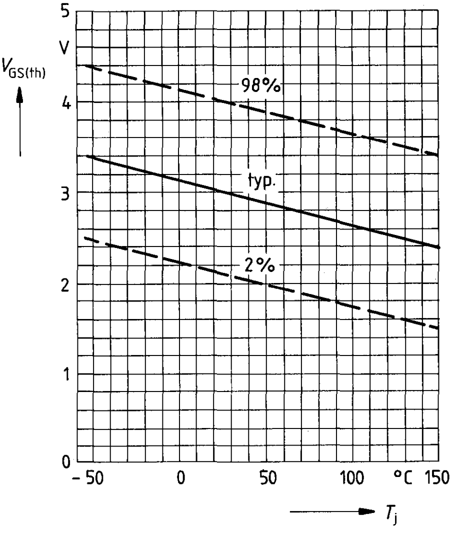
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 13A, V_{GS} = 10V
(spread)



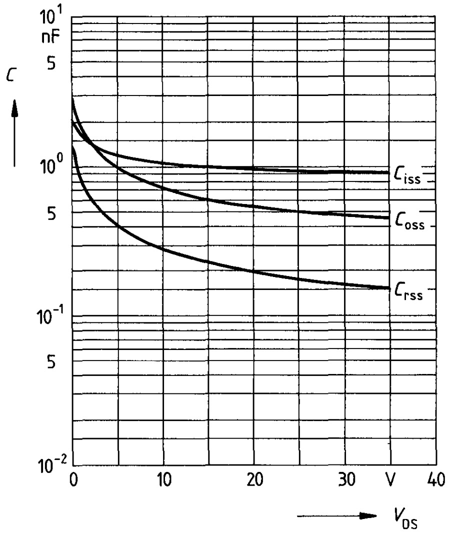
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



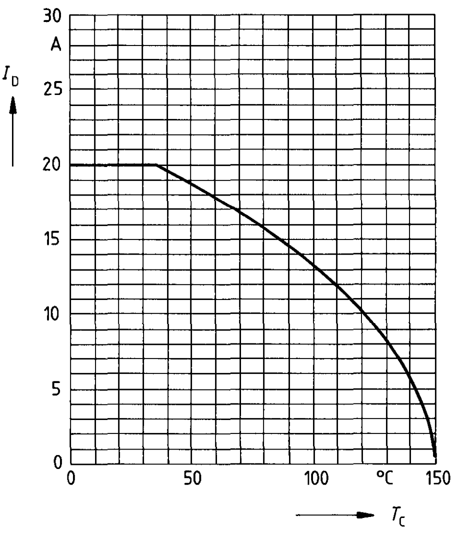
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



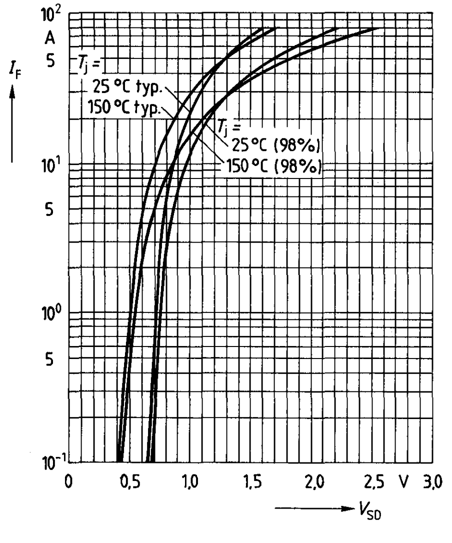
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



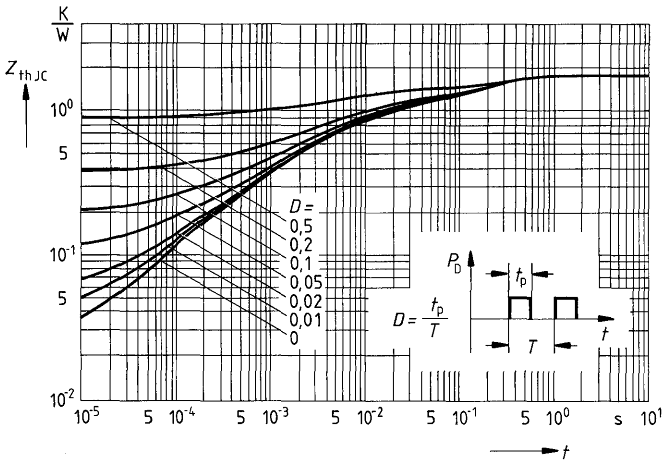
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



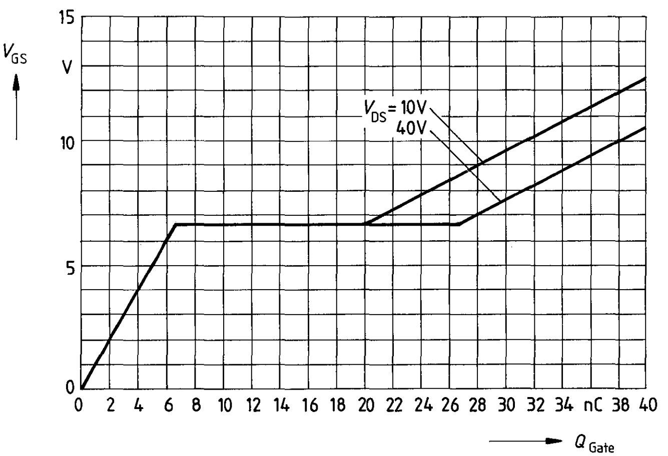
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

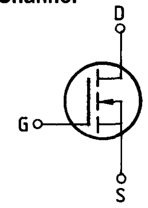


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 30A$



Main ratings

N-Channel

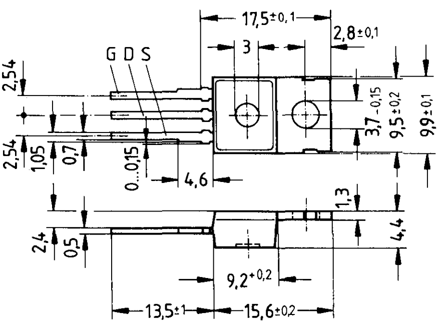


Drain-source voltage	V_{DS}	**= 50 V**
Continuous drain current	I_D	**= 30 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,04 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 11	C67078-A1301-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	30	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	120	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

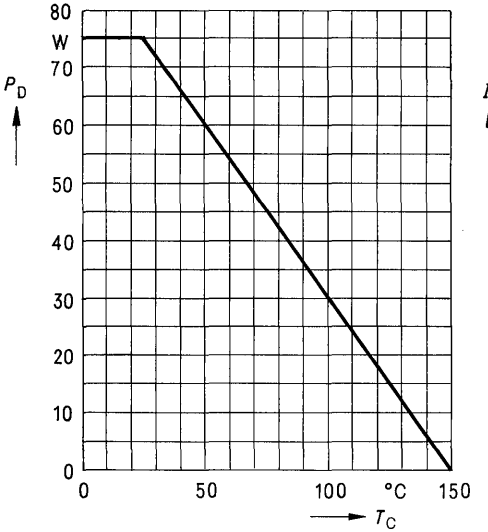
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

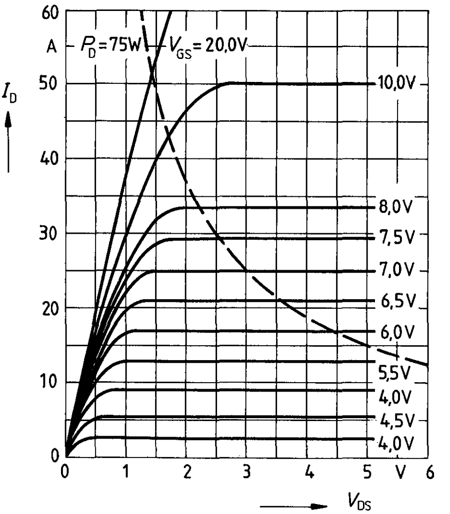
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,03	0,04	Ω	V_{GS} = 10V I_D = 15A
Dynamic ratings						
Forward transconductance	g_{fs}	4,0	8,0	–	S	V_{DS} = 25V I_D = 15A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	750	1100		
Reverse transfer capacitance	C_{rss}	–	250	400		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	70	110		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	180	230		
	t_f	–	130	170		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	30	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	120		
Diode forward on-voltage	V_{SD}	–	1,7	2,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,25	–	µC	

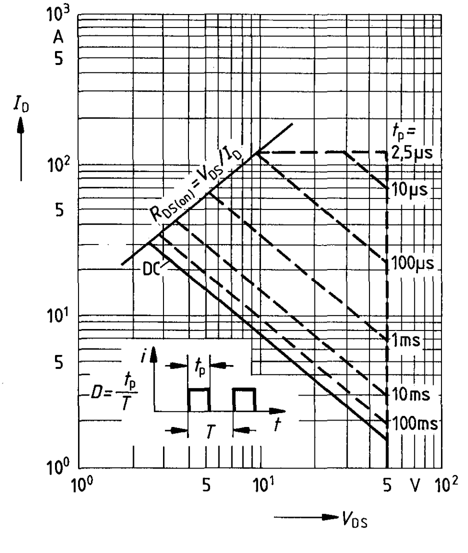
Power dissipation $P_D = f(T_C)$



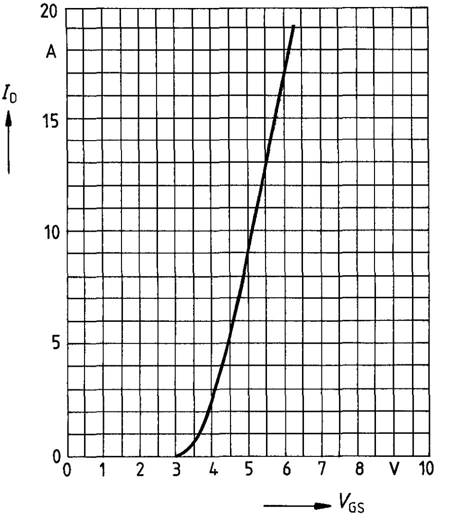
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



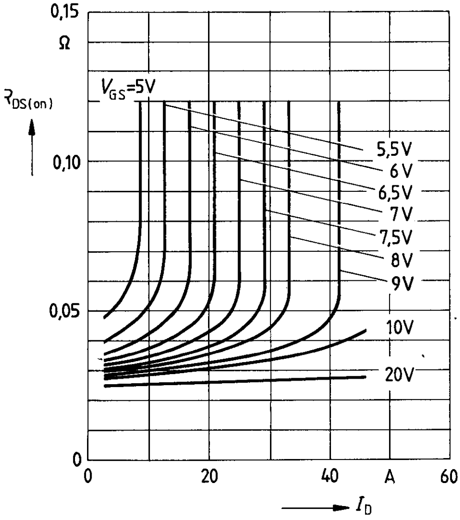
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



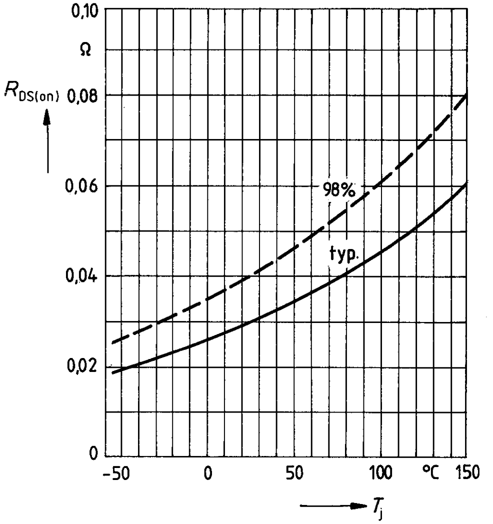
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



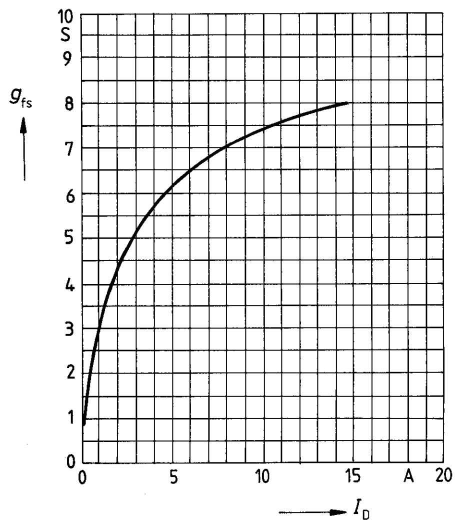
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



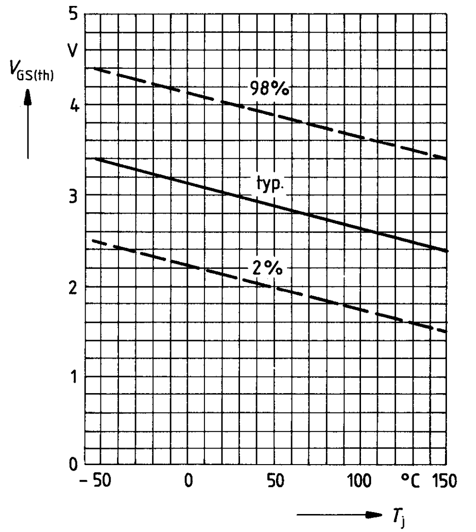
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 15A$, $V_{GS} = 10V$
(spread)



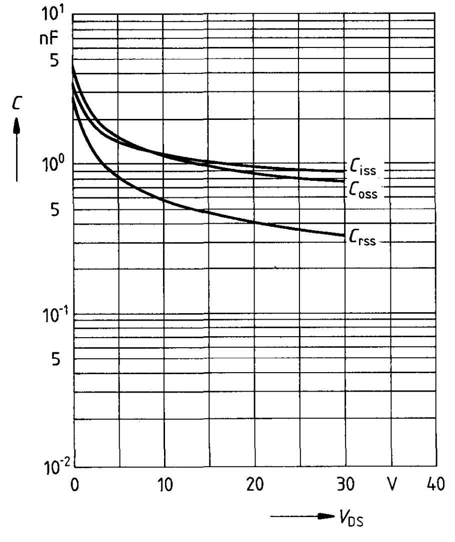
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 μs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



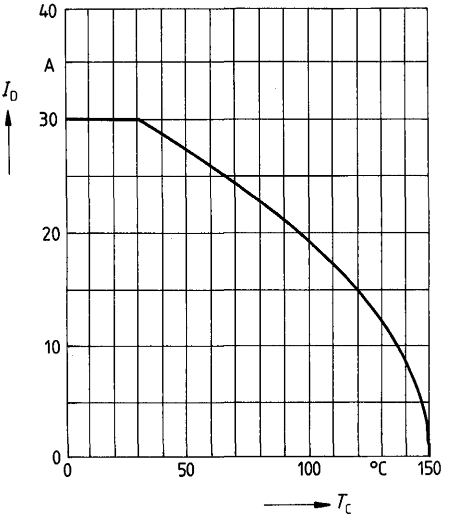
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



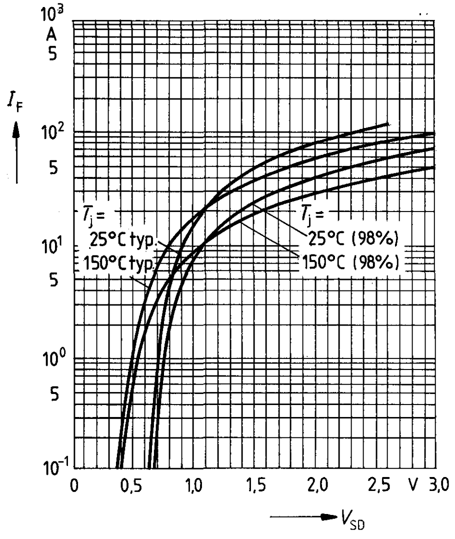
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



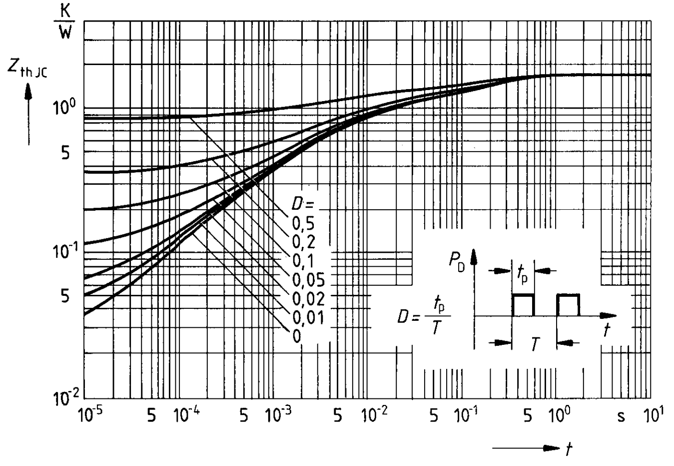
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



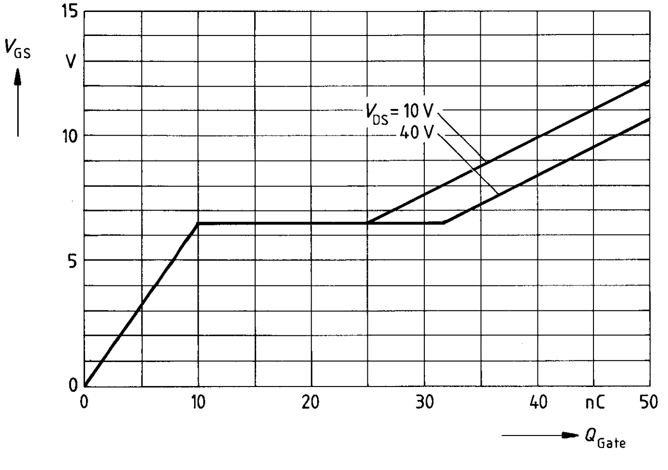
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



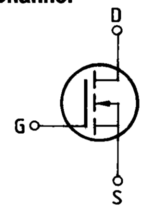
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 45A$



Main ratings

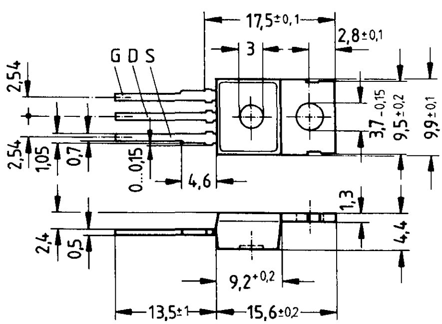
Drain-source voltage V_{DS} **= 50 V**
Continuous drain current I_D **= 25 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,06 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 11 A	C67078-A1301-A3



Dimensions in mm

Maximum ratings

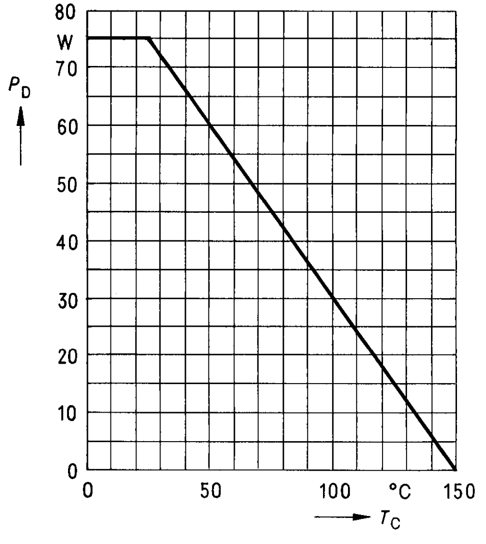
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	25	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	100	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\ JA}$	≤75	K/W	

 S Preferred Type

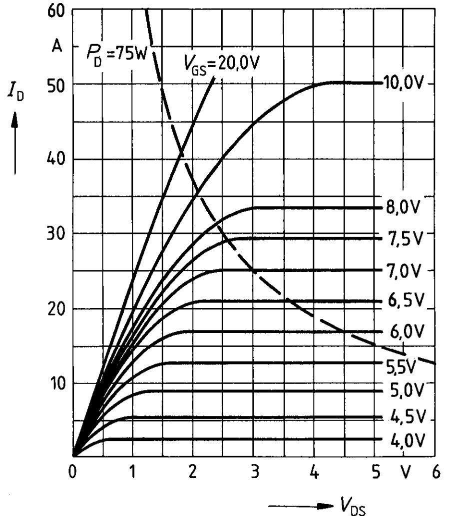
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,05	0,06	Ω	V_{GS} = 10V I_D = 15A
Dynamic ratings						
Forward transconductance	g_{fs}	4,0	8,0	–	S	V_{DS} = 25V I_D = 15A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	750	1100		
Reverse transfer capacitance	C_{rss}	–	250	400		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	70	110		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	180	230		
	t_f	–	130	170		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	25	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	100		
Diode forward on-voltage	V_{SD}	–	1,6	2,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,25	–	µC	

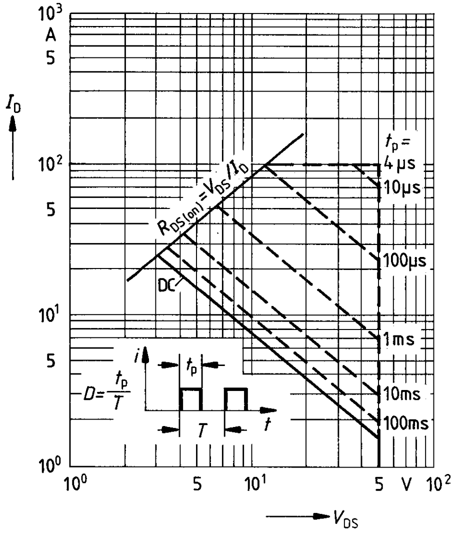
Power dissipation $P_D = f(T_C)$



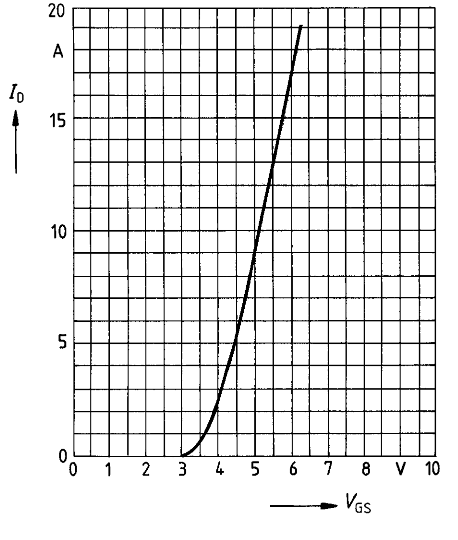
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



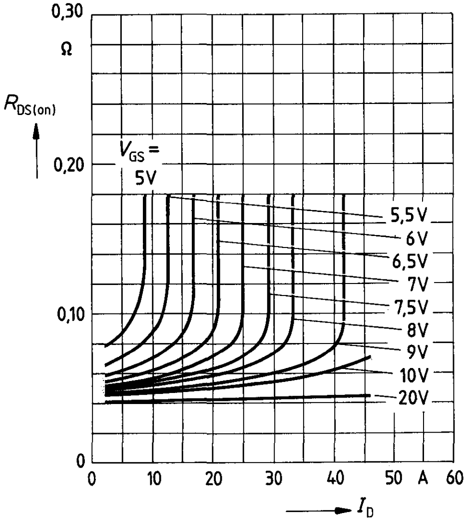
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



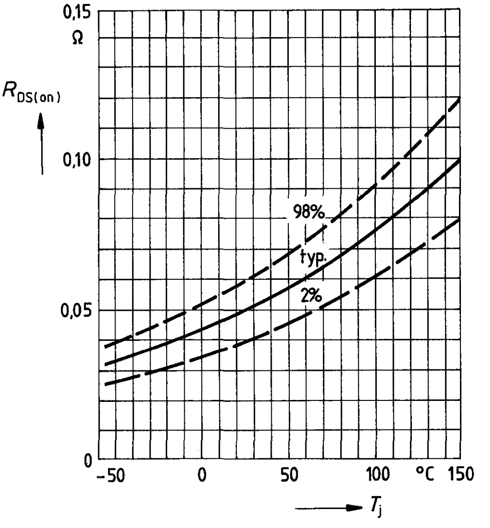
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



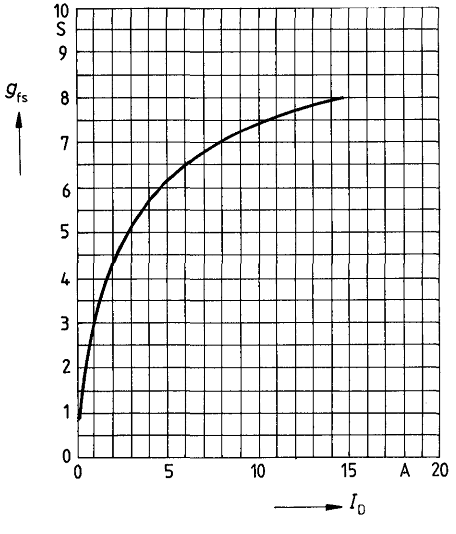
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



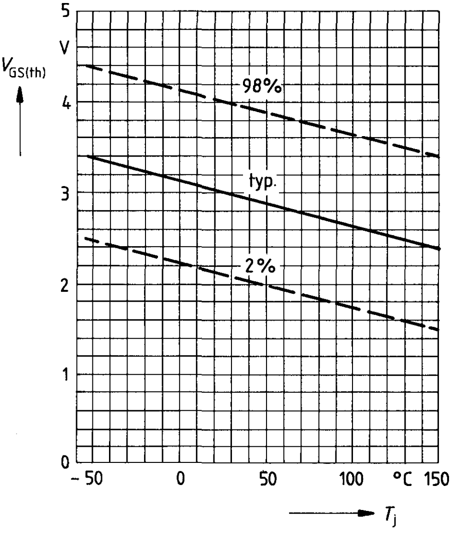
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 15A$, $V_{GS} = 10V$
(spread)



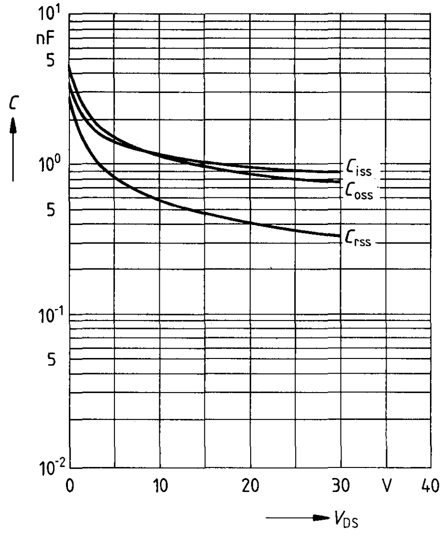
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



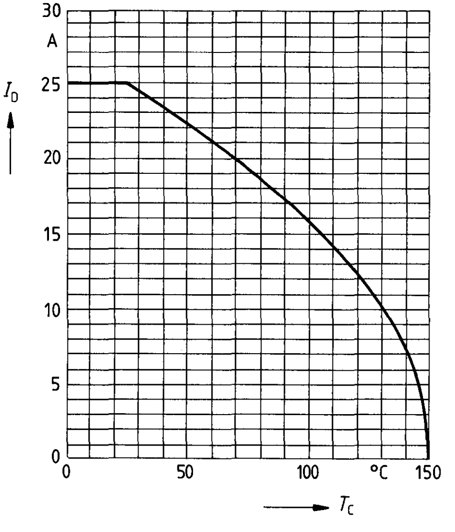
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



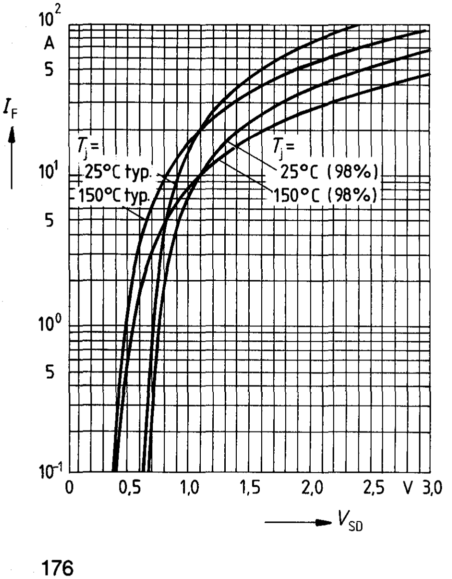
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



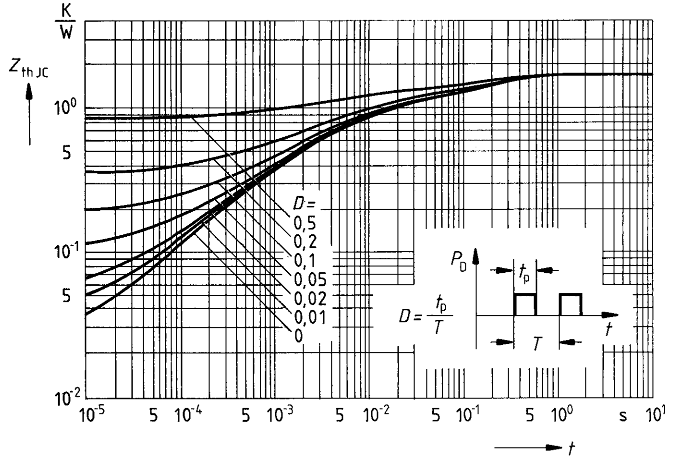
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



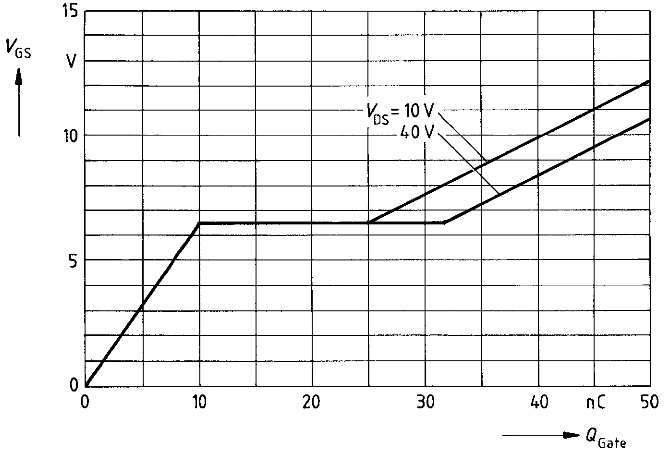
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



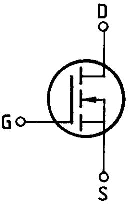
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 45A$



Main ratings

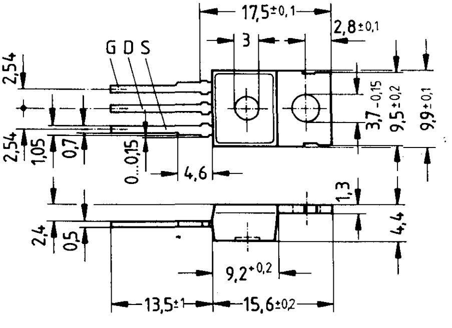
Drain-source voltage V_{DS} **= 50 V**
Continuous drain current I_D **= 30 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,04 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
BUZ 11 S 2	C67078-A1301-A5



Dimensions in mm

Maximum ratings

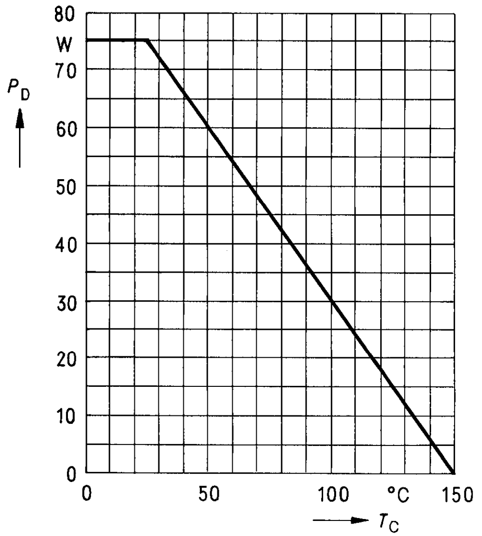
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	30	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	120	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\ JA}$	≤75	K/W	

Electrical characteristics

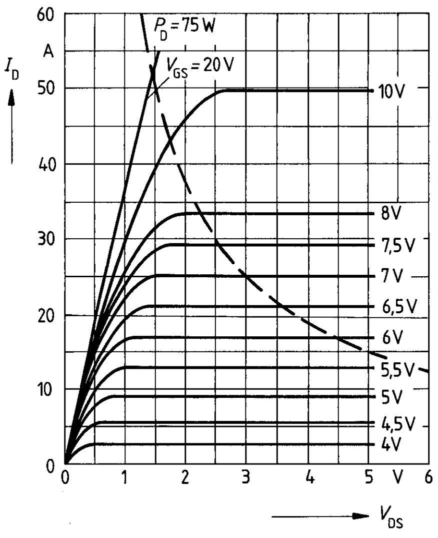
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,03	0,04	Ω	V_{GS} = 10V I_D = 15A
Dynamic ratings						
Forward transconductance	g_{fs}	4,0	8,0	–	S	V_{DS} = 25V I_D = 15A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	750	1100		
Reverse transfer capacitance	C_{rss}	–	250	400		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	70	110		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	180	230		
	t_f	–	130	170		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	30	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	120		
Diode forward on-voltage	V_{SD}	–	1,7	2,6	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,25	–	µC	

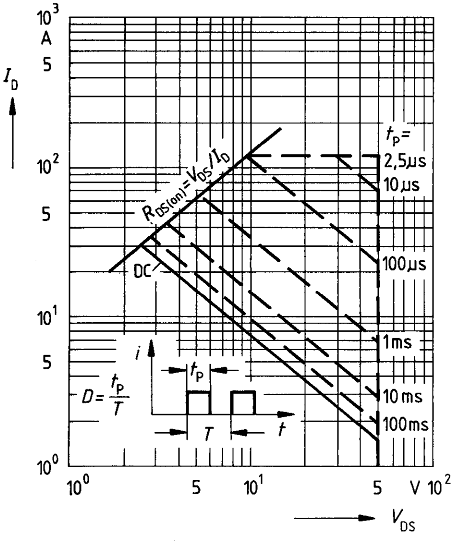
Power dissipation $P_D = f(T_C)$



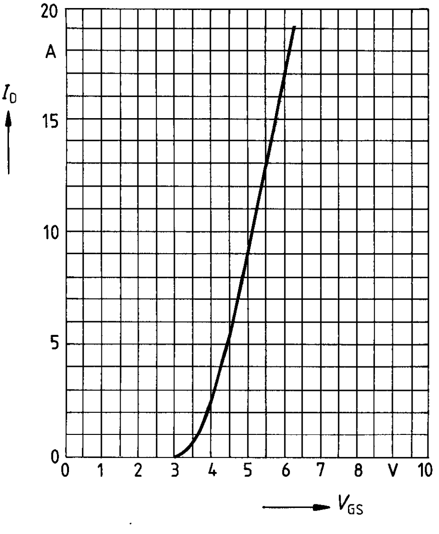
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



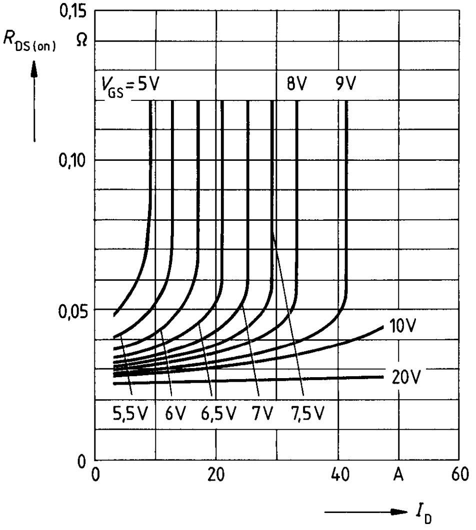
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



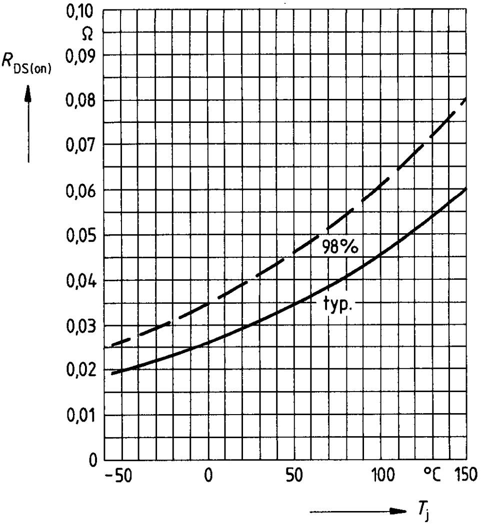
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



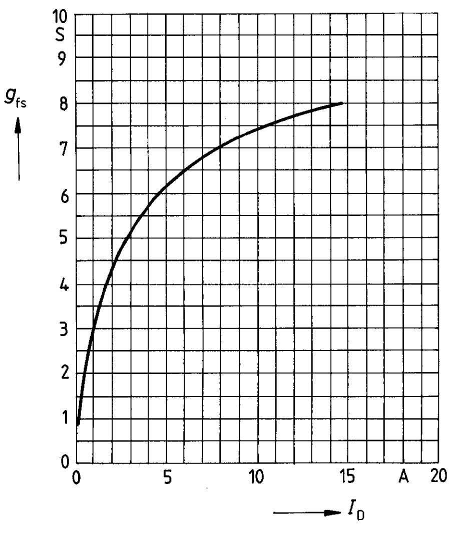
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



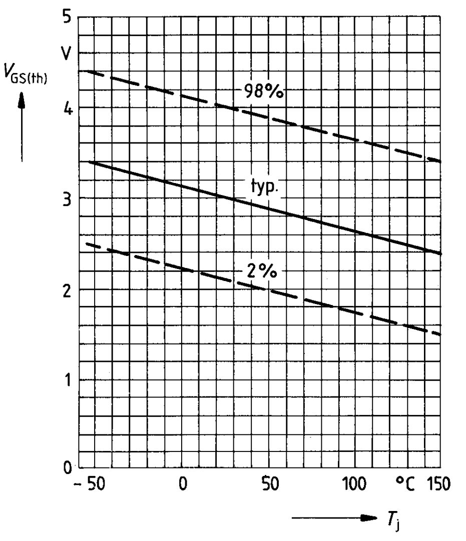
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 15A, V_{GS} = 10V
(spread)



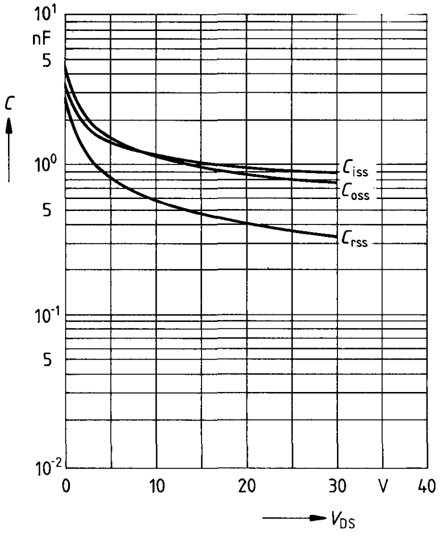
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



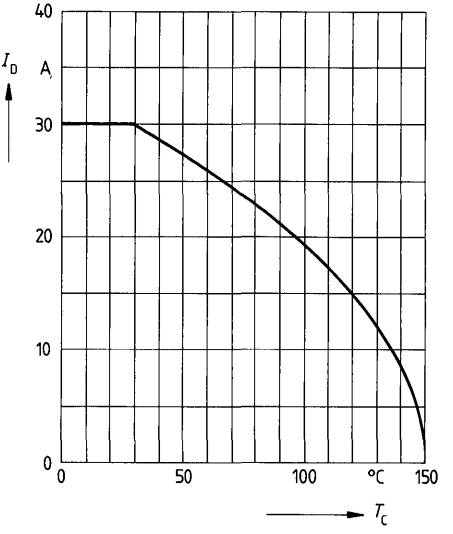
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



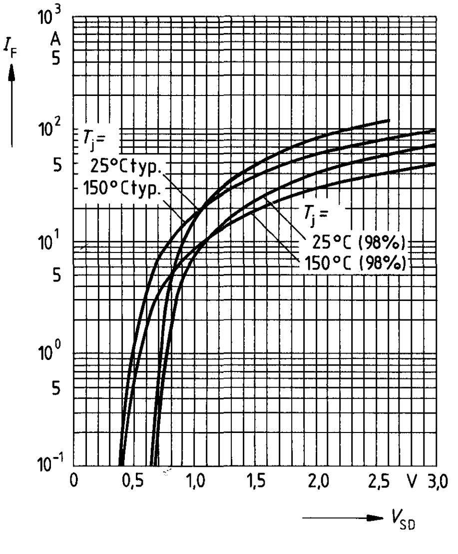
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



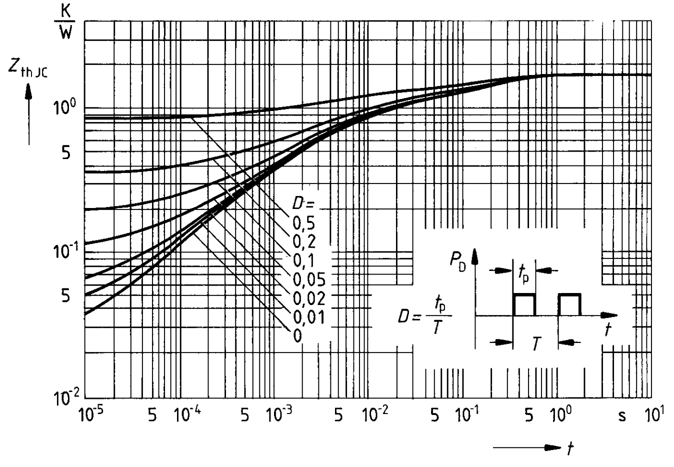
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



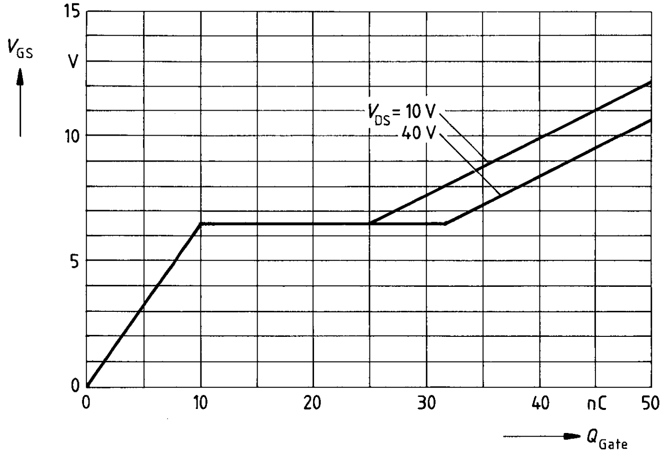
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

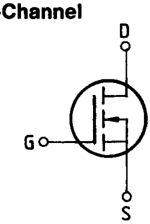


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 45A$



Main ratings

N-Channel

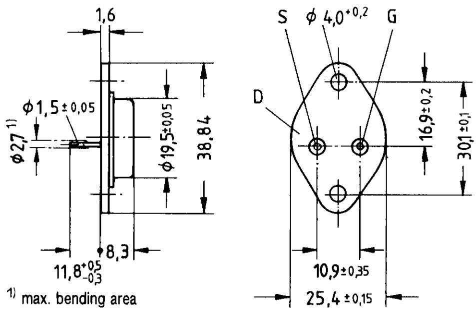


Drain-source voltage	V_{DS}	=	**50 V**
Continuous drain current	I_D	=	**39 A**
Drain-source on-resistance	$R_{DS(on)}$	=	**0,04 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AE (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 14	C67078-A1000-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	39	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	155	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	− 55 ... + 150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\ JC}$	≤ 1,0	K/W
Chip – ambient	$R_{th\ JA}$	≤ 35	K/W

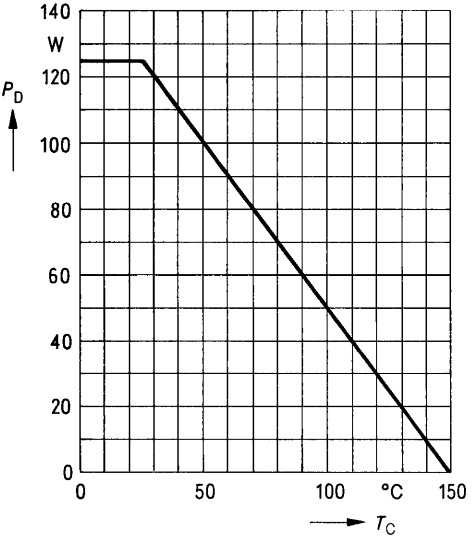
S Preferred Type

Electrical characteristics

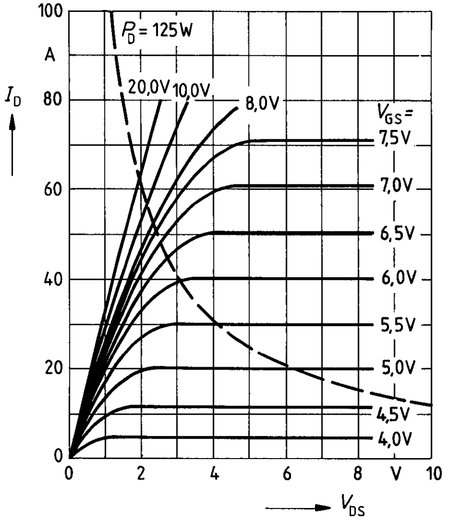
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	65	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,035	0,04	Ω	V_{GS} = 10V I_D = 22A
Dynamic ratings						
Forward transconductance	g_{fs}	7,0	18,0	–	S	V_{DS} = 25V I_D = 22A
Input capacitance	C_{iss}	–	1600	2100	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	1300	2000		
Reverse transfer capacitance	C_{rss}	–	500	800		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	110	170		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	250	330		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	39	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	155		
Diode forward on-voltage	V_{SD}	–	1,5	2,2	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	150	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,0	–	µC	

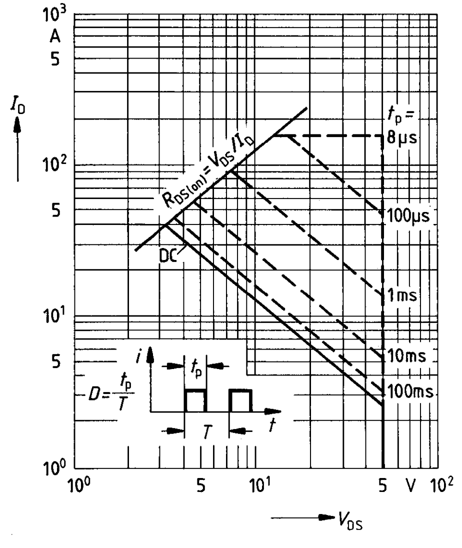
Power dissipation $P_D = f(T_C)$



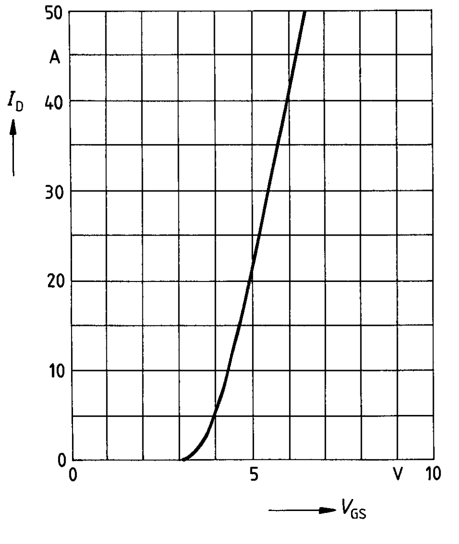
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



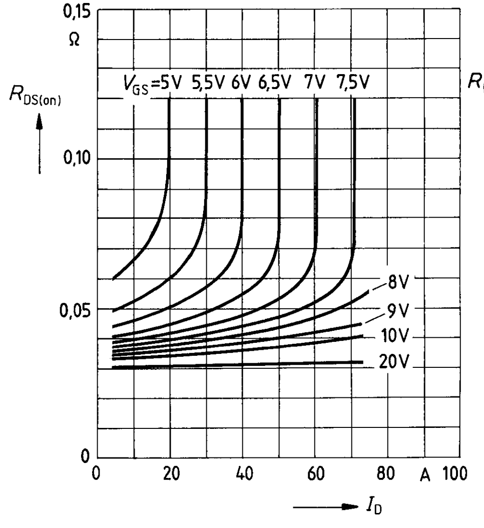
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



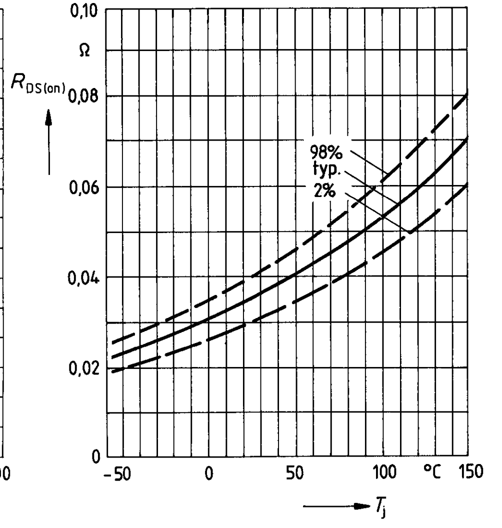
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



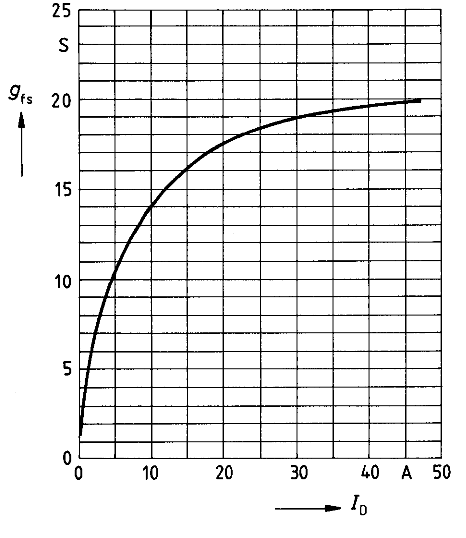
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



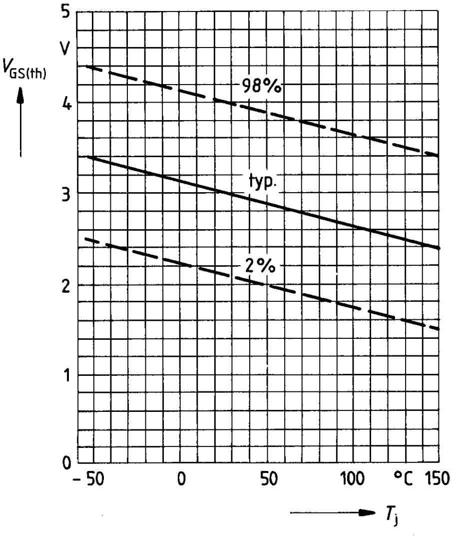
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 22A$, $V_{GS} = 10V$
(spread)



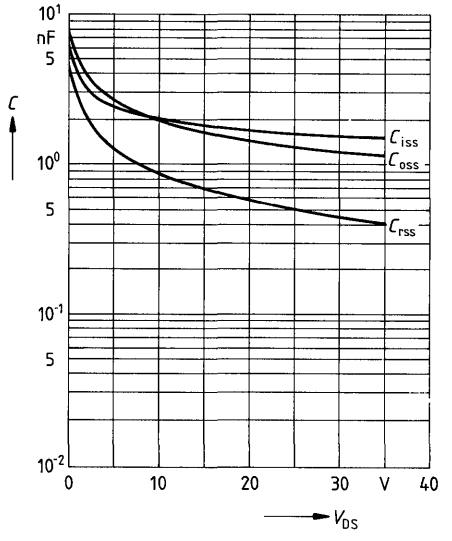
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



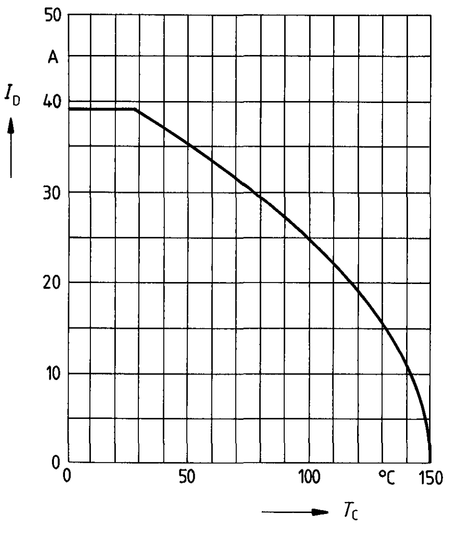
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



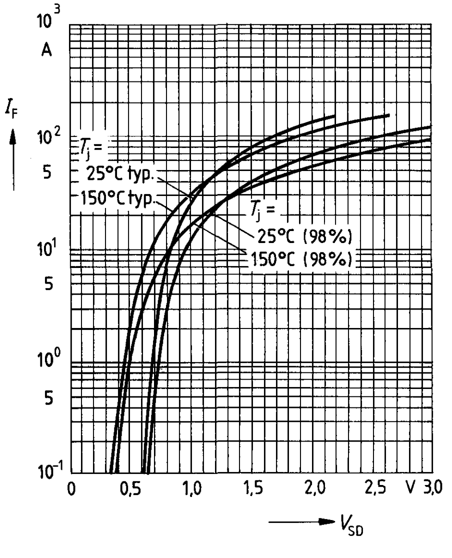
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



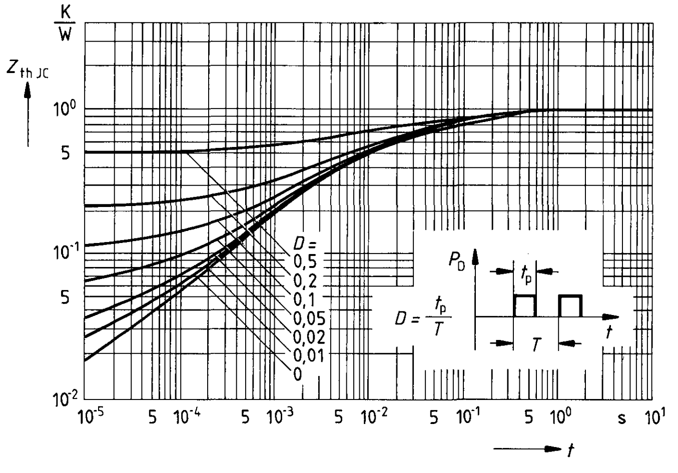
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



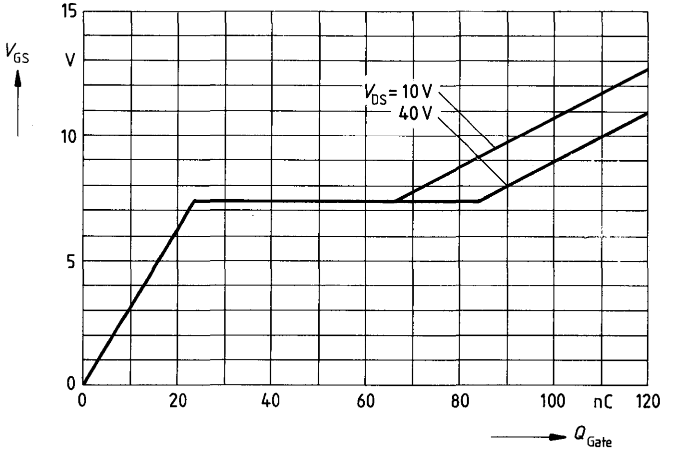
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu\text{s}$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



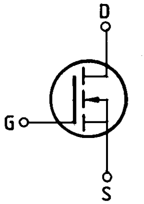
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 67{,}5A$



Main ratings

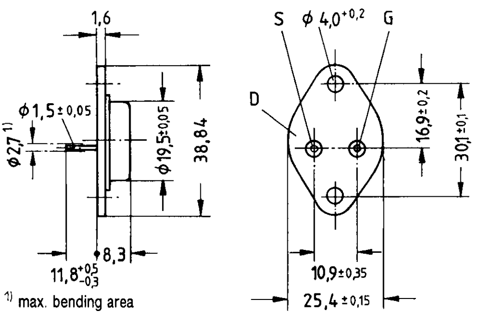
Drain-source voltage V_{DS} = **50 V**
Continuous drain current I_D = **45 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,03 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AE (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
BUZ 15	C67078-A1001-A2



Dimensions in mm

Maximum ratings

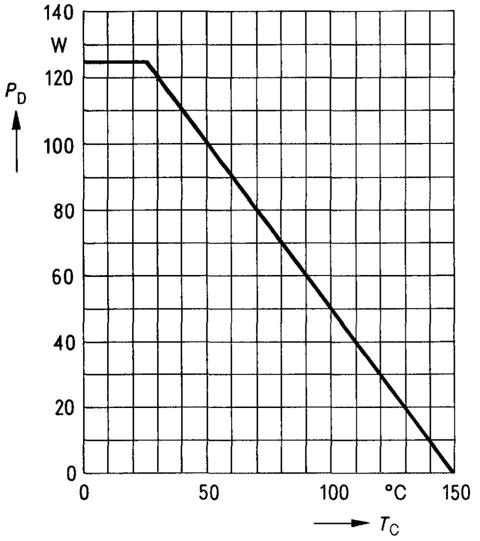
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	45	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	180	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤1,0	K/W	
Chip – ambient	$R_{th JA}$	≤35	K/W	

Electrical characteristics

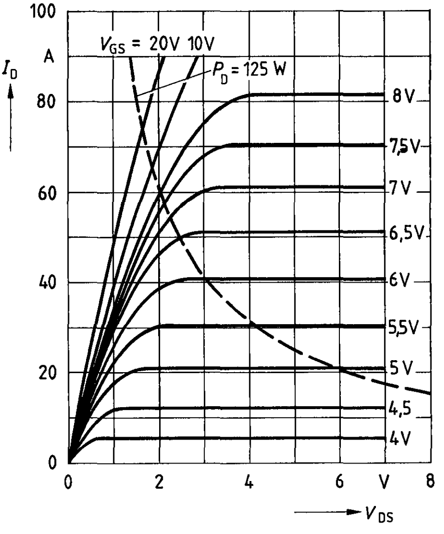
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	65	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,025	0,03	Ω	V_{GS} = 10V I_D = 22A
Dynamic ratings						
Forward transconductance	g_{fs}	7,0	18,0	–	S	V_{DS} = 25V I_D = 22A
Input capacitance	C_{iss}	–	1600	2100	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	1300	2000		
Reverse transfer capacitance	C_{rss}	–	500	800		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	110	170		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	250	330		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	45	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	180		
Diode forward on-voltage	V_{SD}	–	1,6	2,4	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	150	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,0	–	µC	

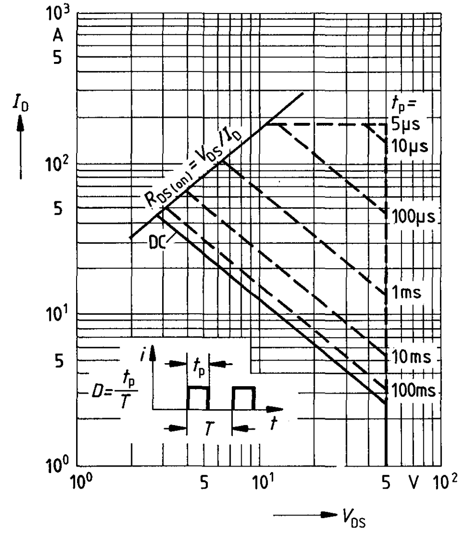
Power dissipation $P_D = f(T_C)$



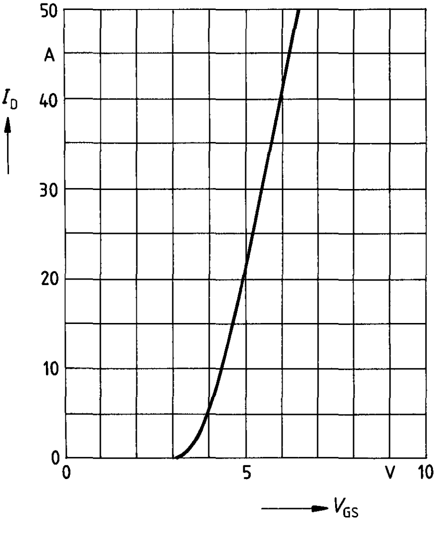
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



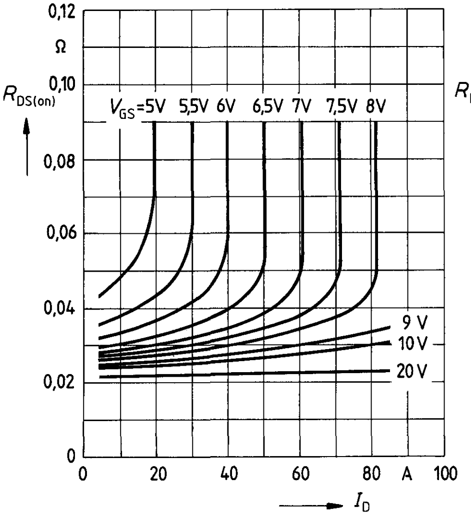
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



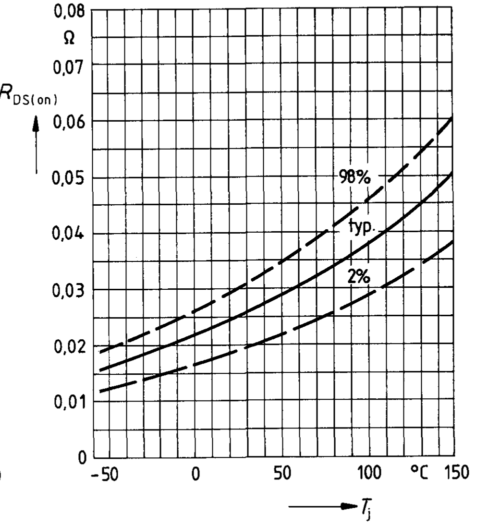
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



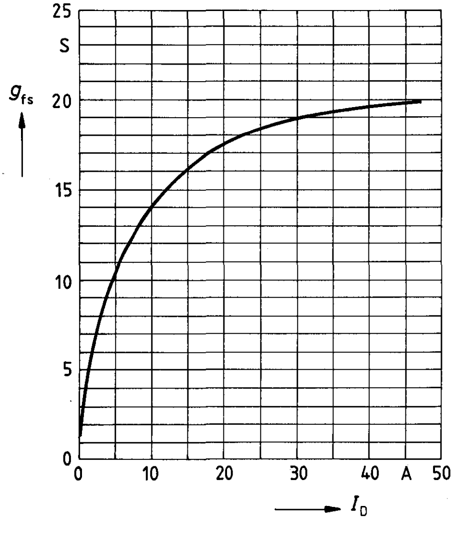
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



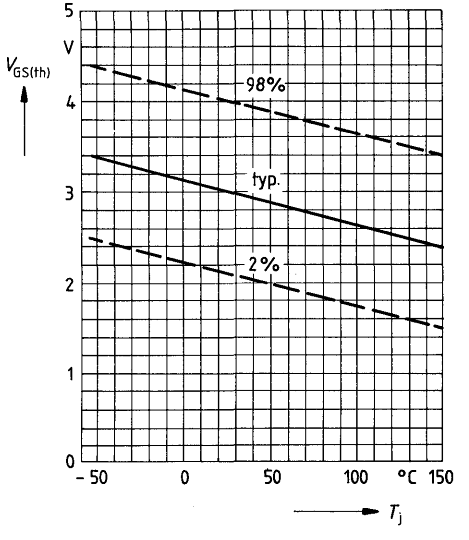
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 22A, V_{GS} = 10V
(spread)



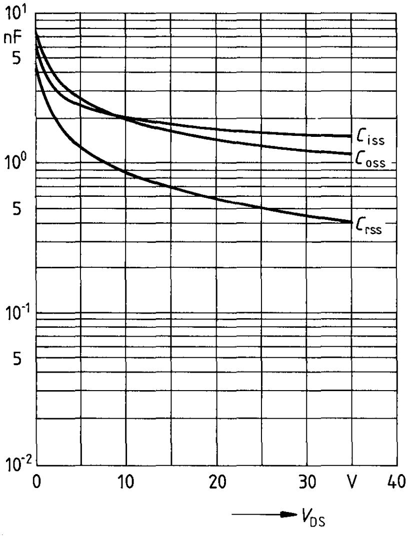
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



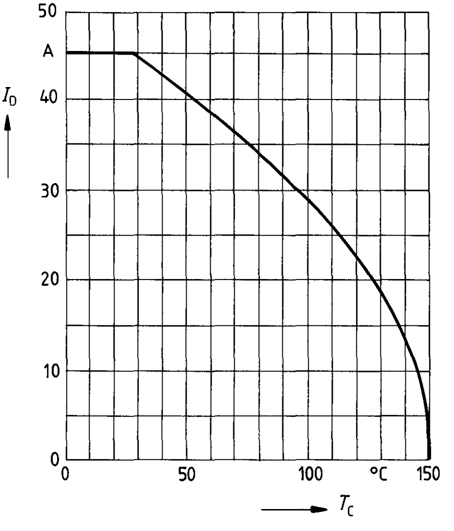
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



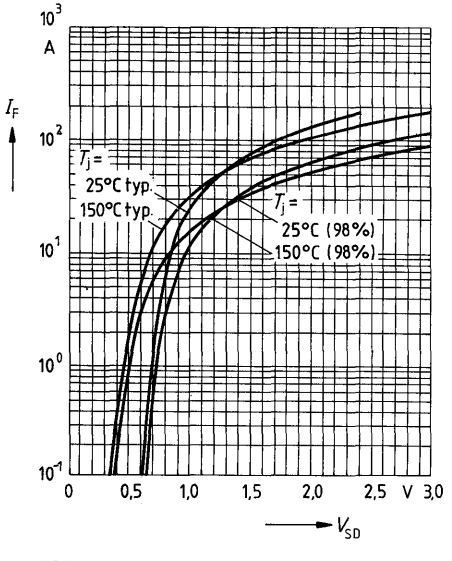
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



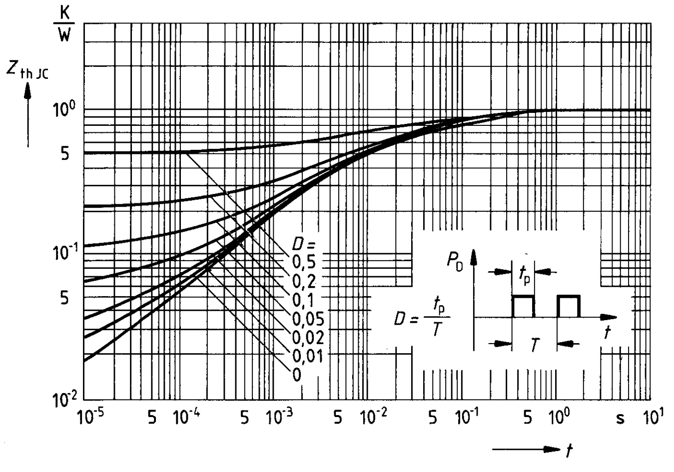
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



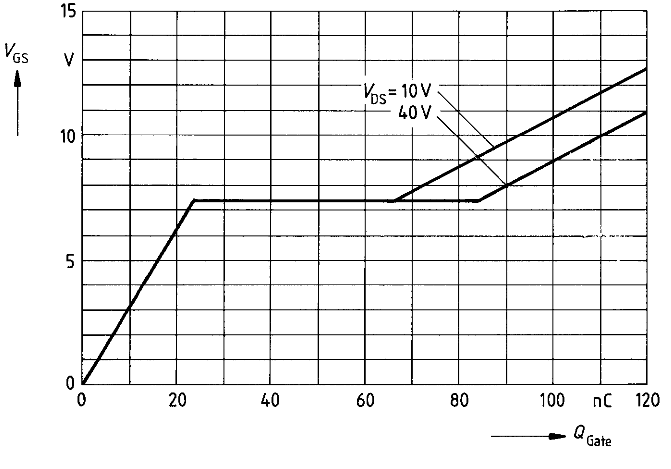
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



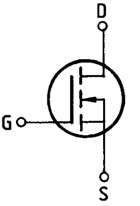
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 67{,}5A$



Main ratings

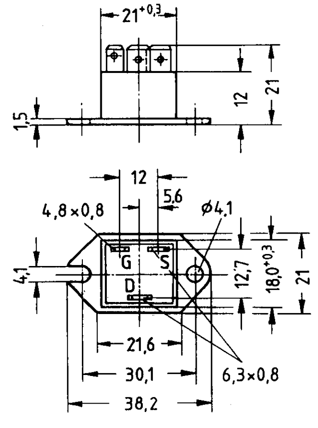
Drain-source voltage V_{DS} **= 50 V**
Continuous drain current I_D **= 32 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,04 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 17	C67078-A1600-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	32	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	125	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40… +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤1,5	K/W	

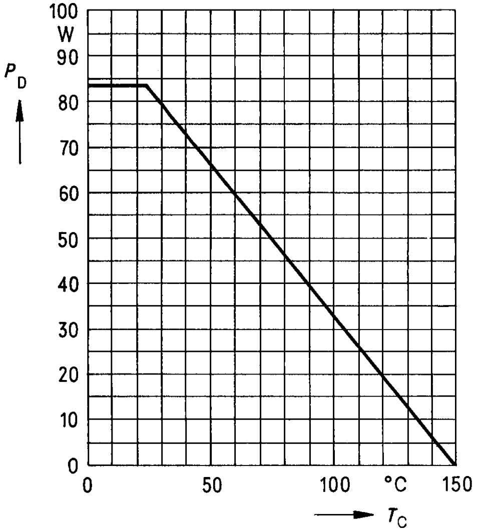
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

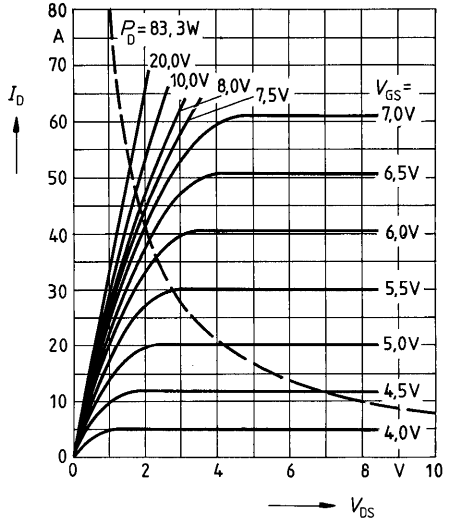
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	65	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,035	0,04	Ω	V_{GS} = 10V I_D = 22A
Dynamic ratings						
Forward transconductance	g_{fs}	7,0	18,0	–	S	V_{DS} = 25V I_D = 22A
Input capacitance	C_{iss}	–	1600	2100	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	1300	2000		
Reverse transfer capacitance	C_{rss}	–	500	800		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	110	170		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	250	330		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	32	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	125		
Diode forward on-voltage	V_{SD}	–	1,4	2,0	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	150	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,0	–	µC	

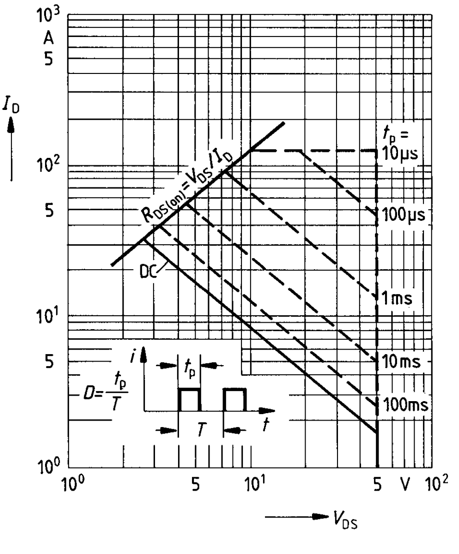
Power dissipation $P_D = f(T_C)$



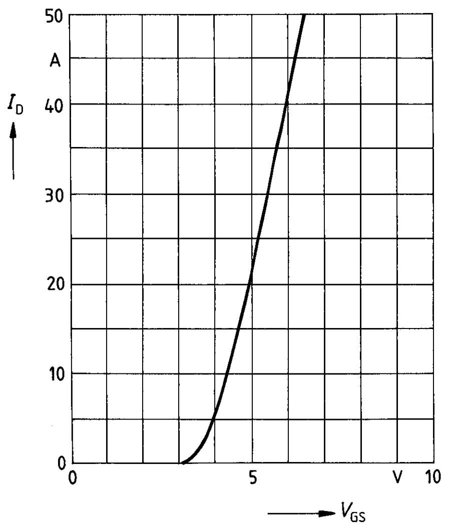
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



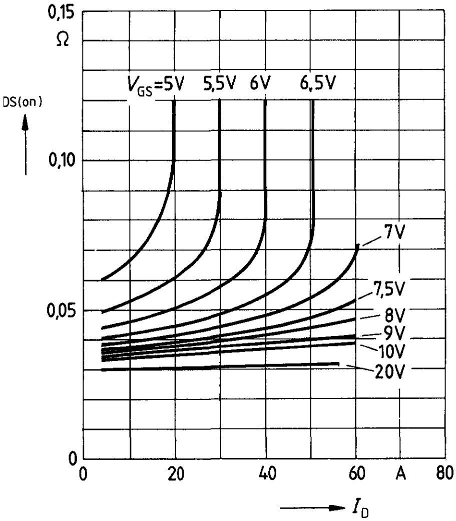
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



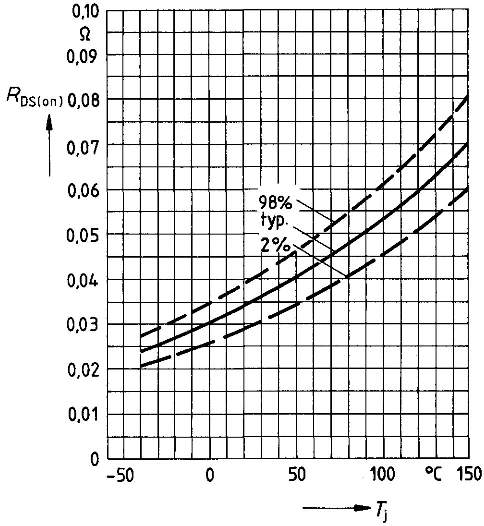
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



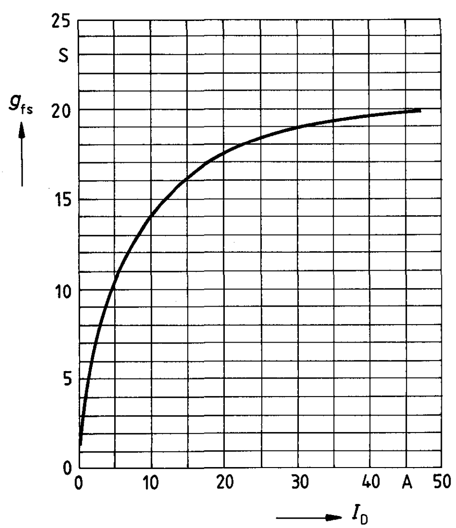
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



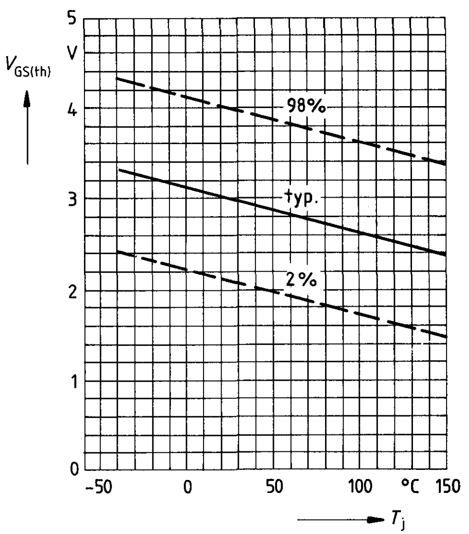
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 22A, V_{GS} = 10V
(spread)



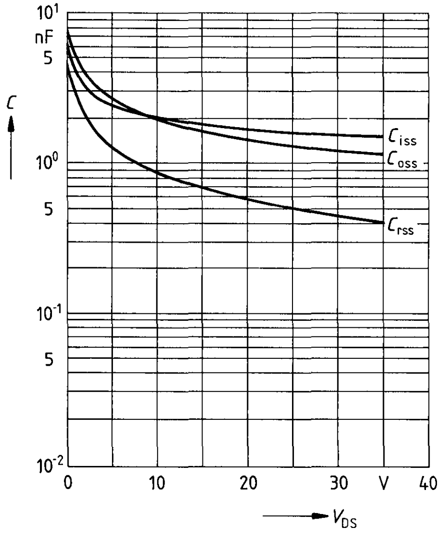
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



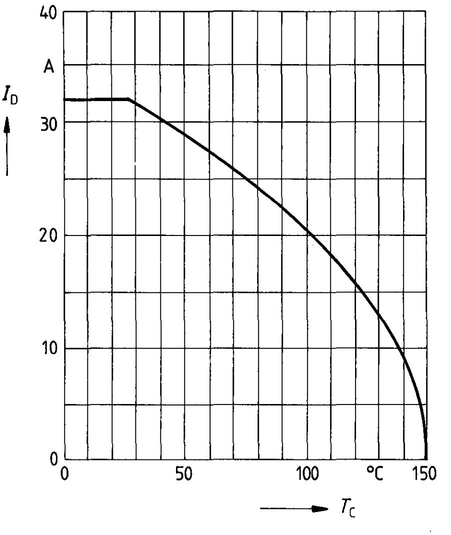
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



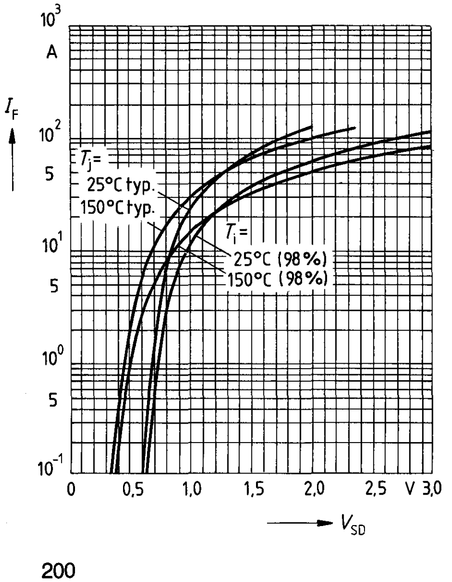
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



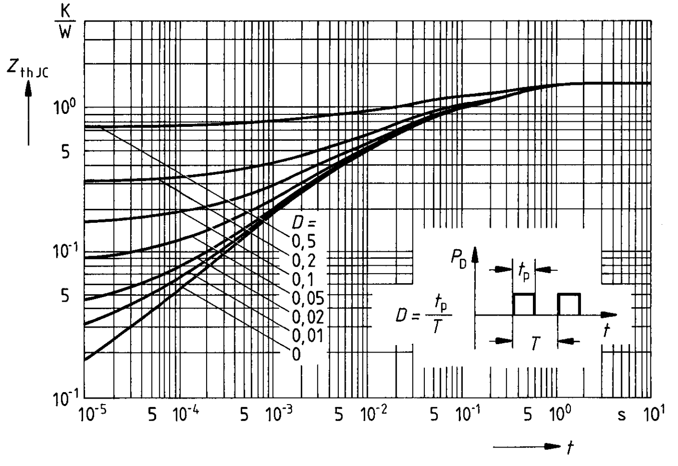
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



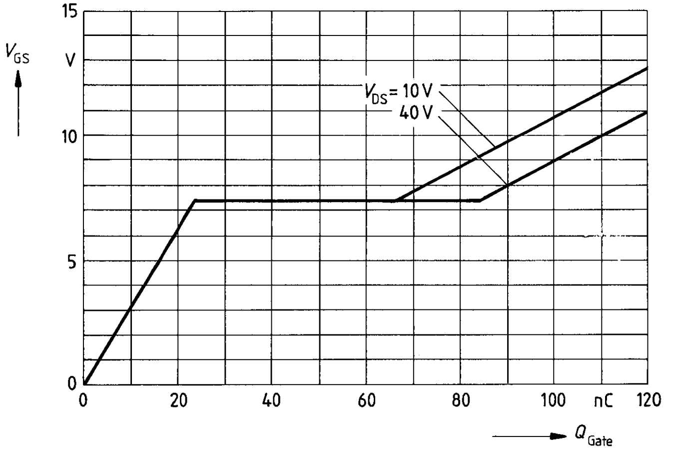
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

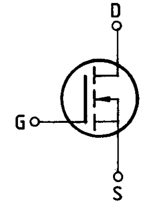


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 67{,}5A$



Main ratings

N-Channel

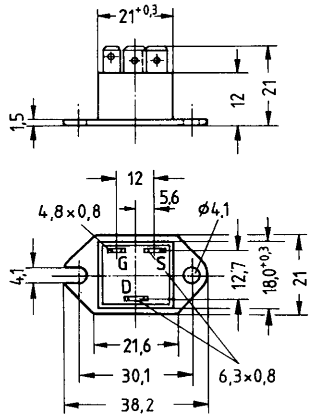


Drain-source voltage	V_{DS}	**= 50 V**
Continuous drain current	I_D	**= 37 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,03 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
S BUZ 18	C67078-A1601-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	37	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	145	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40… +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,5	K/W	

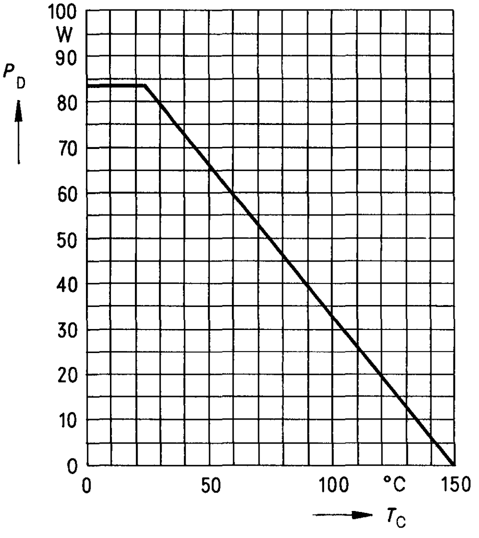
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

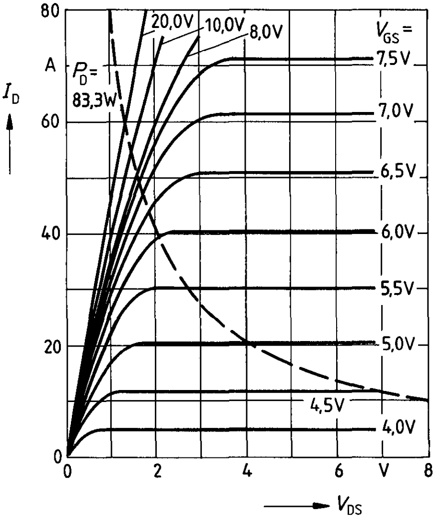
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	550	65	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,025	0,03	Ω	V_{GS} = 10V I_D = 22A
Dynamic ratings						
Forward transconductance	g_{fs}	7,0	18,0	–	S	V_{DS} = 25V I_D = 22A
Input capacitance	C_{iss}	–	1600	2100	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	1300	2000		
Reverse transfer capacitance	C_{rss}	–	500	800		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	110	170		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	250	330		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	37	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	145		
Diode forward on-voltage	V_{SD}	–	1,5	2,2	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	150	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,0	–	µC	

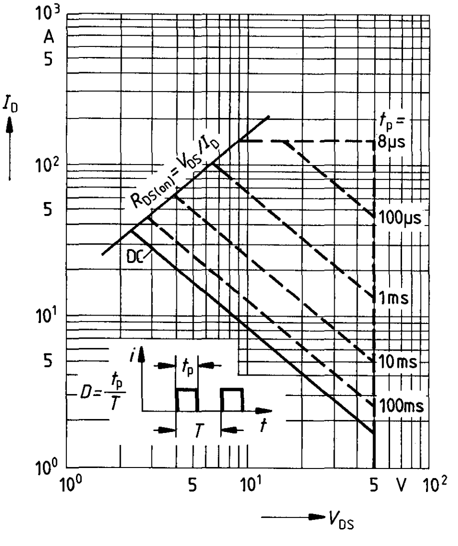
Power dissipation $P_D = f(T_C)$



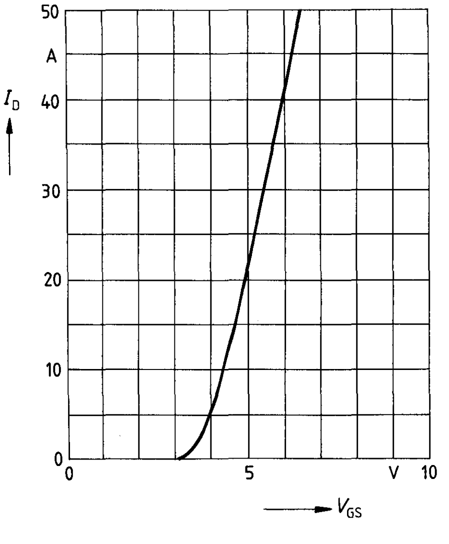
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



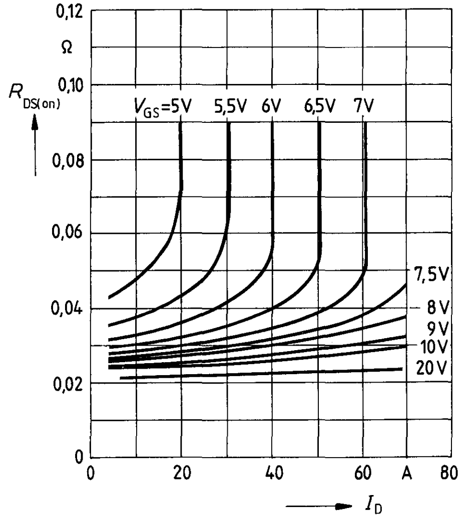
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



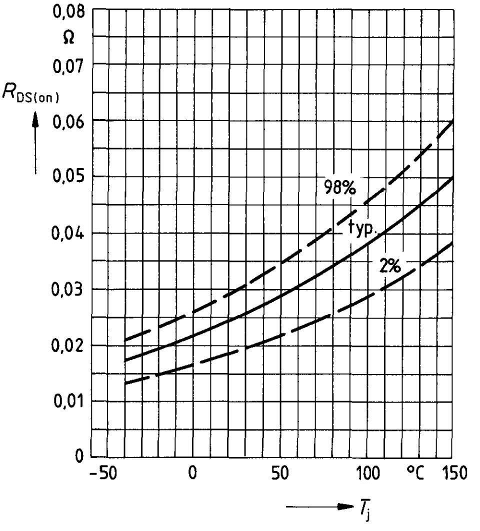
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



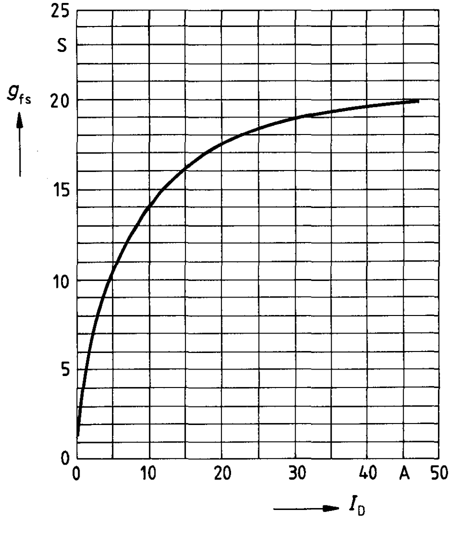
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



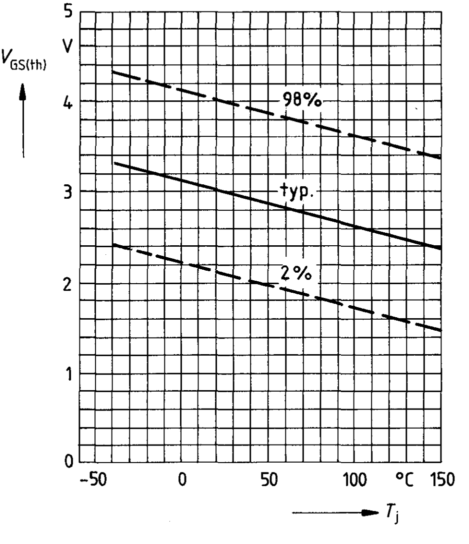
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 22A$, $V_{GS} = 10V$
(spread)



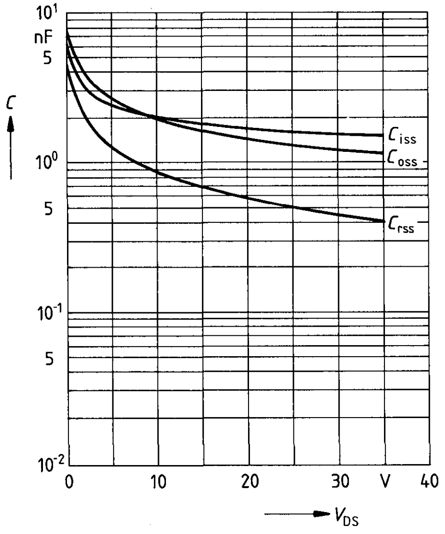
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



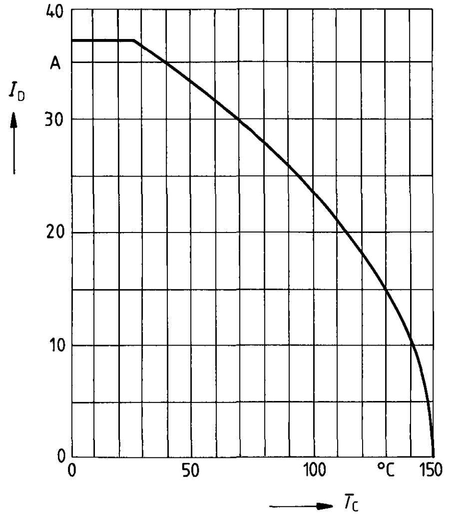
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



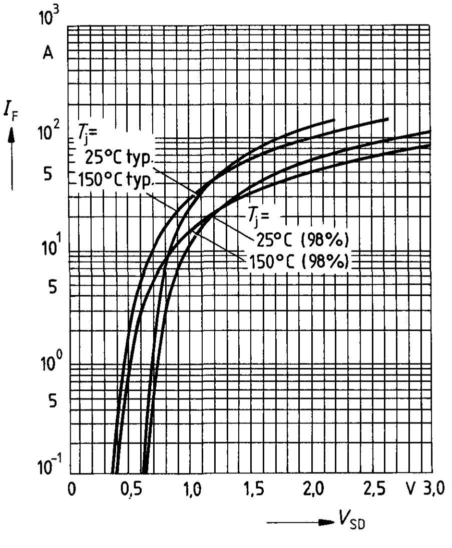
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



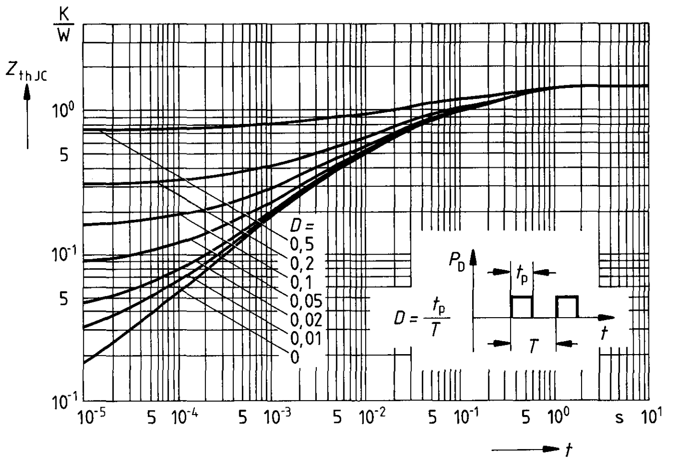
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



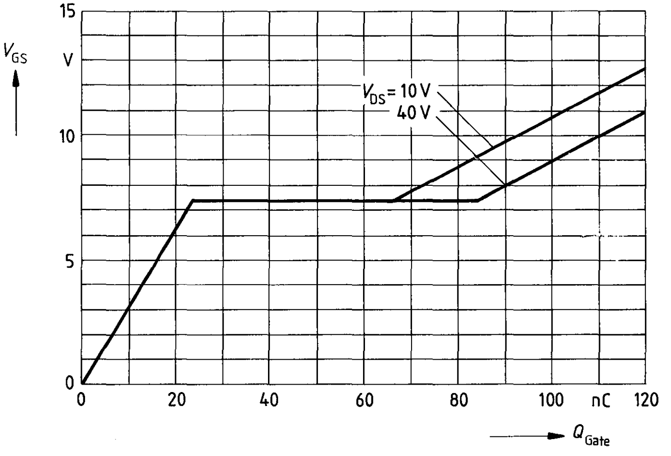
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu\text{s}$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



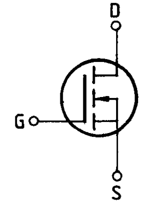
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 67{,}5A$



Main ratings

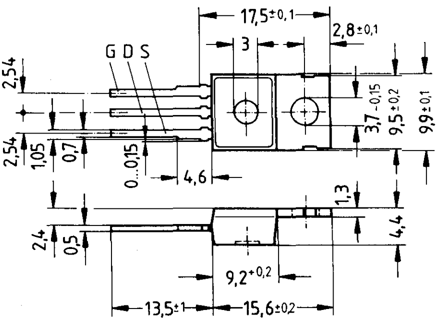
Drain-source voltage V_{DS} **= 100 V**
Continuous drain current I_D **= 12 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,2 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 20	C67078-A1302-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	12	A	T_C = 55 °C
Pulsed drain current	I_{Dpuls}	48	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

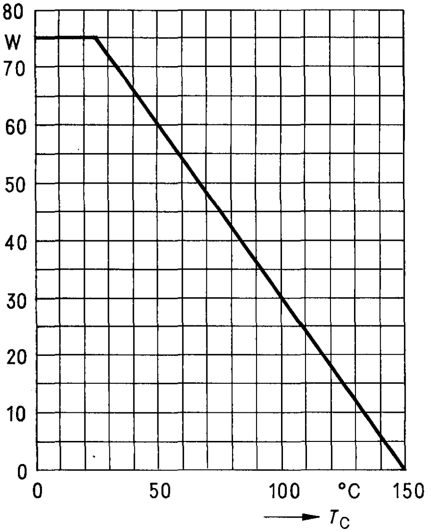
 S Preferred Type

Electrical characteristics

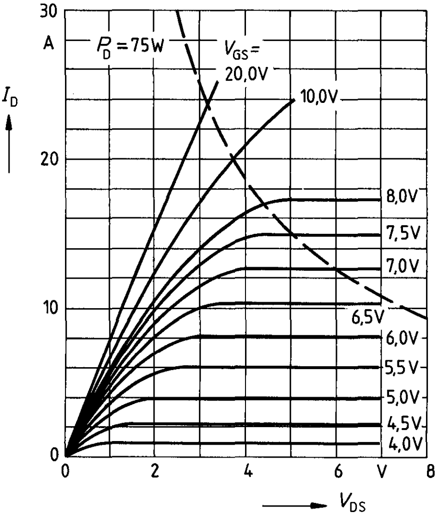
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,15	0,2	Ω	V_{GS} = 10V I_D = 6A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	4,0	–	S	V_{DS} = 25V I_D = 6A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	300	500		
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	50	75		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	12	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	48		
Diode forward on-voltage	V_{SD}	–	1,4	1,8	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,6	–	µC	

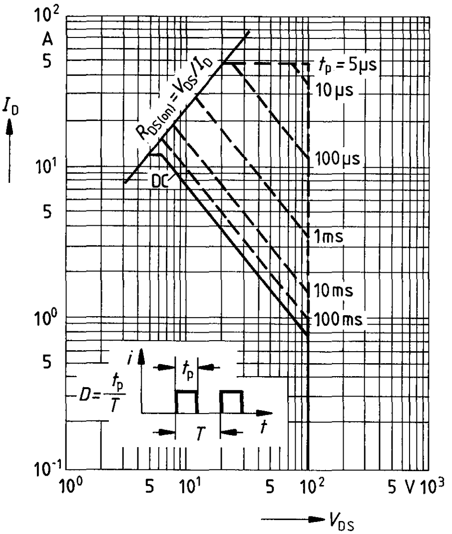
Power dissipation $P_D = f(T_C)$



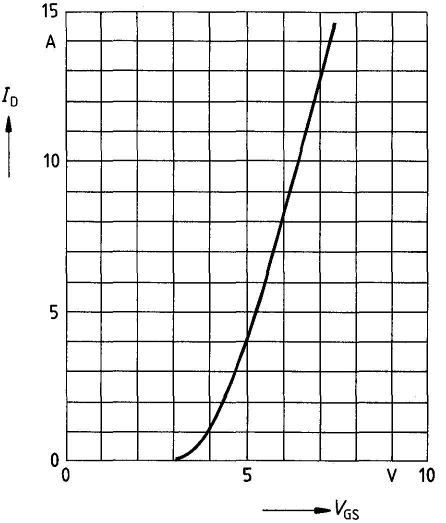
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



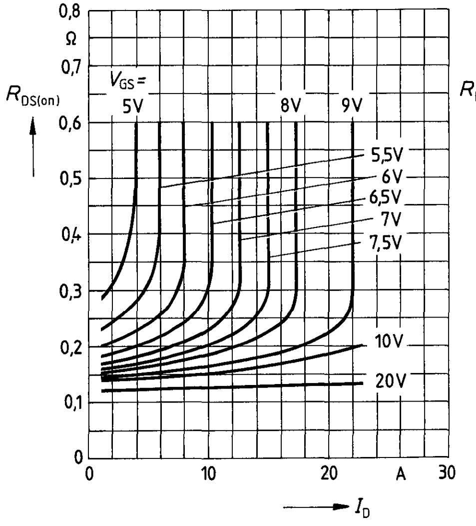
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



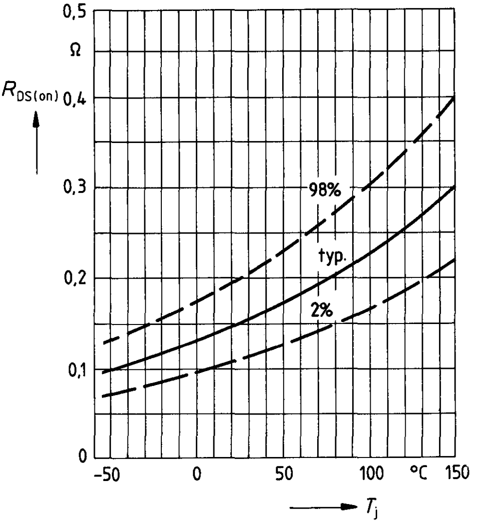
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



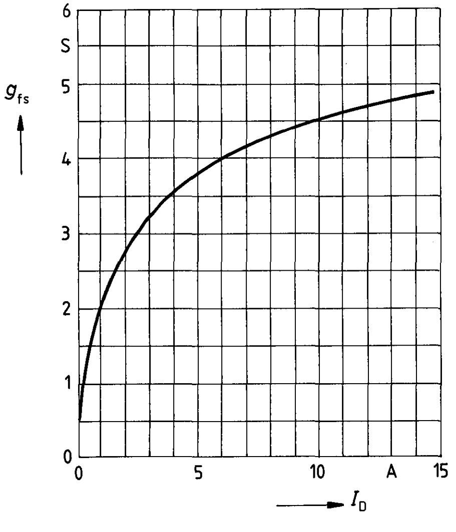
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



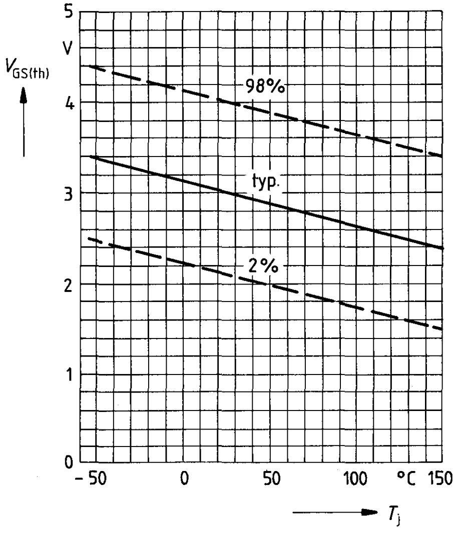
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 6A, V_{GS} = 10V
(spread)



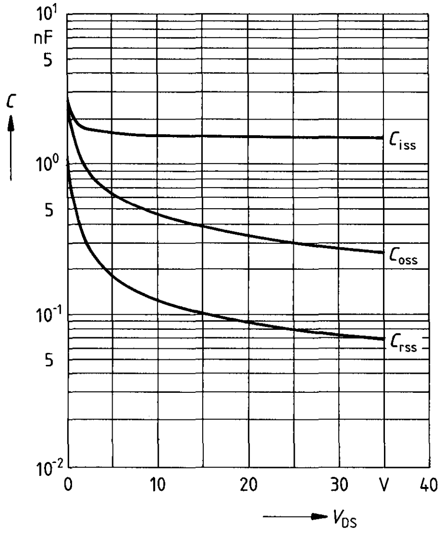
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



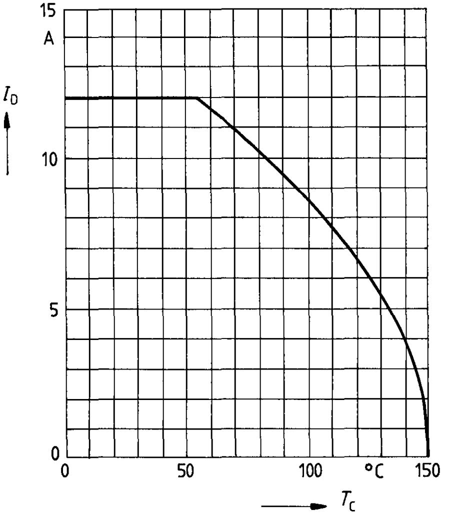
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



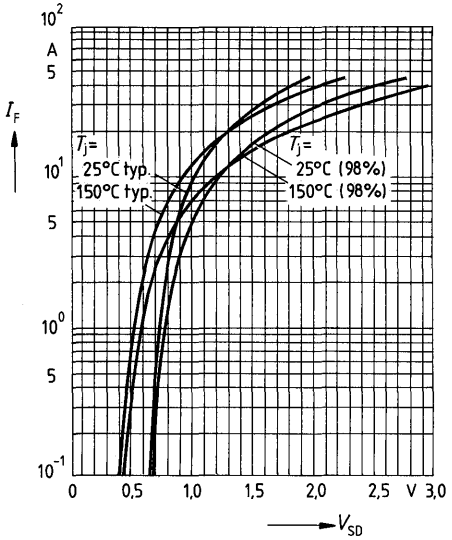
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



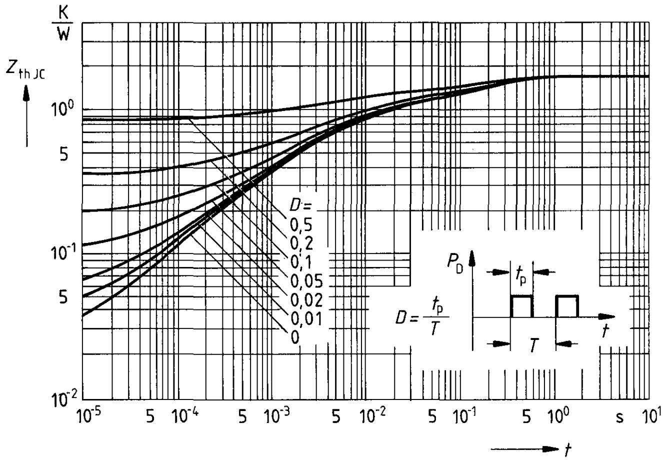
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



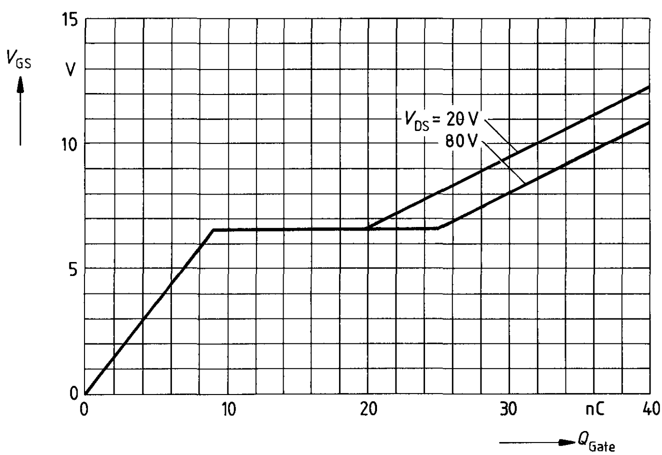
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



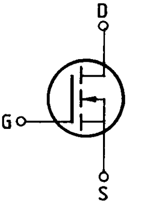
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 18A$



Main ratings

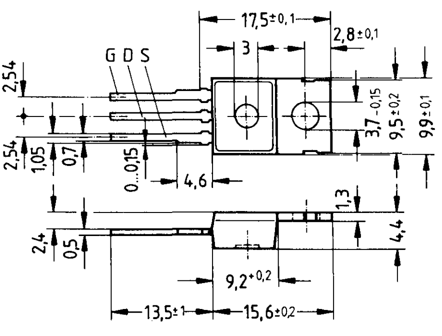
Drain-source voltage V_{DS} **= 100 V**
Continuous drain current I_D **= 19 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,1 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 21	C67078-A1308-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	19	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	75	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

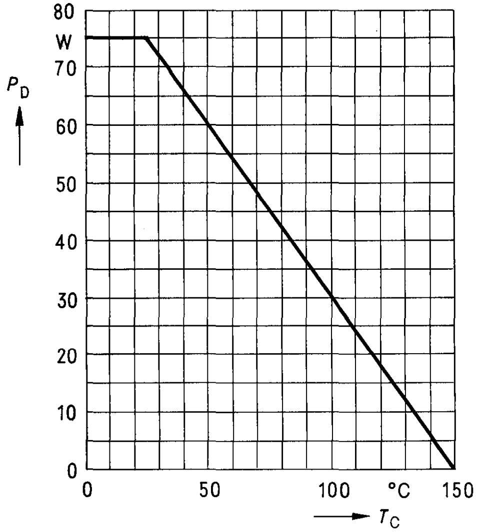
 S Preferred Type

Electrical characteristics

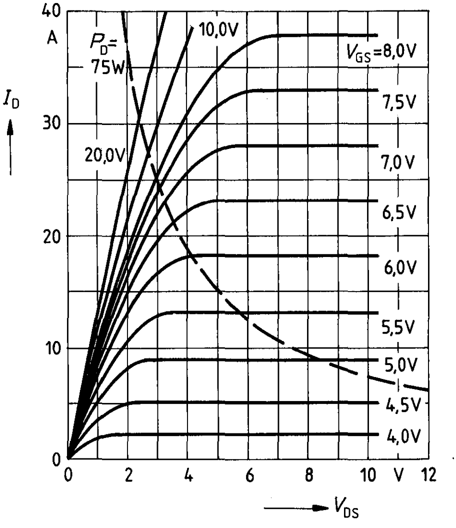
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,09	0,1	Ω	V_{GS} = 10V I_D = 9A
Dynamic ratings						
Forward transconductance	g_{fs}	4,0	8,0	–	S	V_{DS} = 25V I_D = 9A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	450	700		
Reverse transfer capacitance	C_{rss}	–	150	240		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	50	75		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	170	220		
	t_f	–	80	110		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	19	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	75		
Diode forward on-voltage	V_{SD}	–	1,5	2,1	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,25	–	µC	

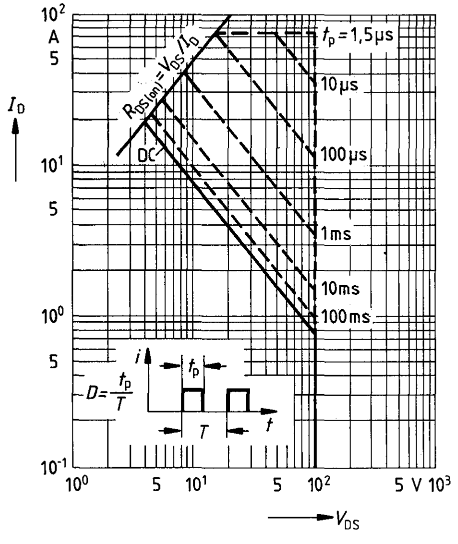
Power dissipation $P_D = f(T_C)$



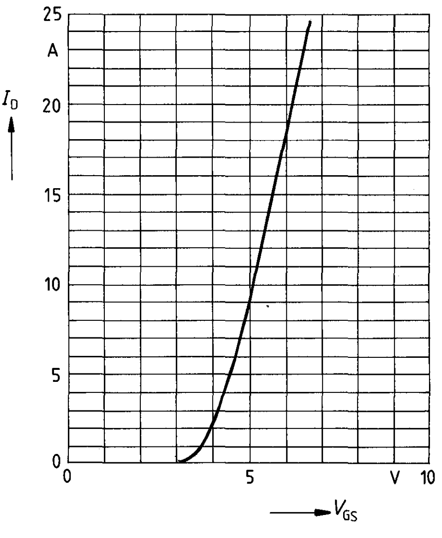
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



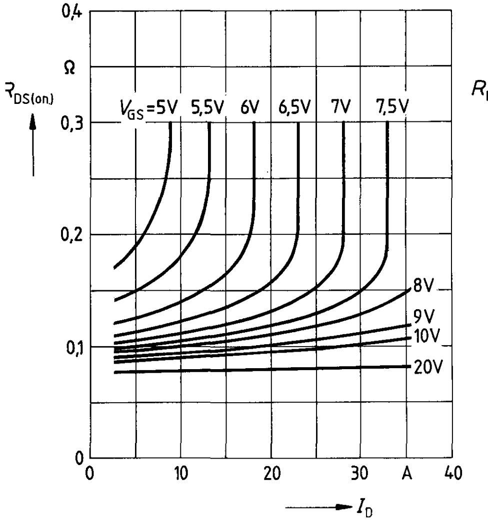
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



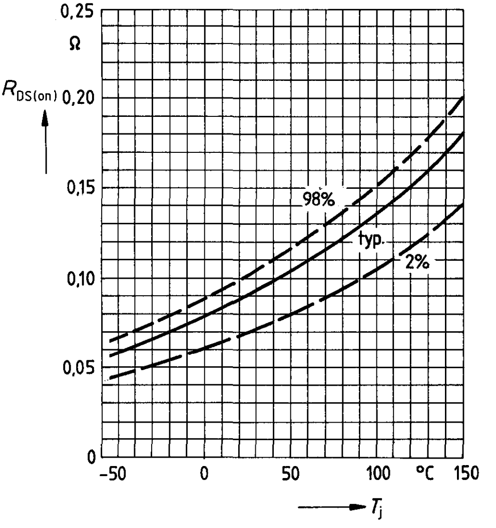
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



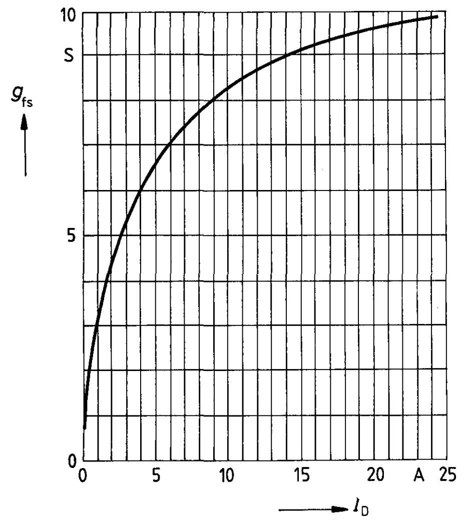
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



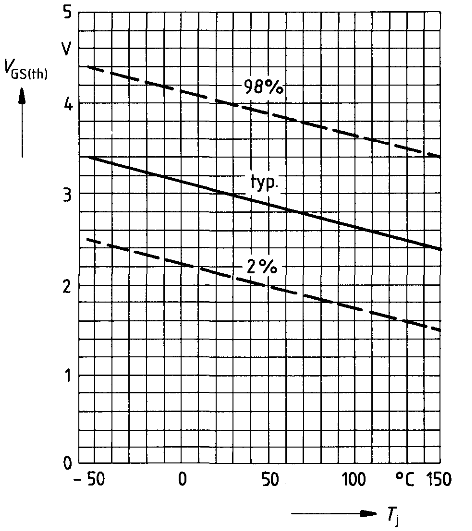
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 9A$, $V_{GS} = 10V$
(spread)



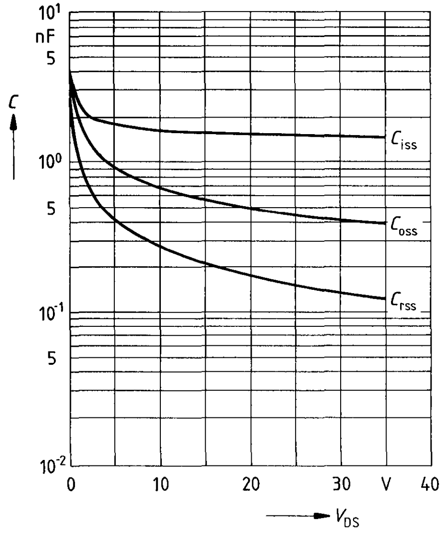
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 μs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



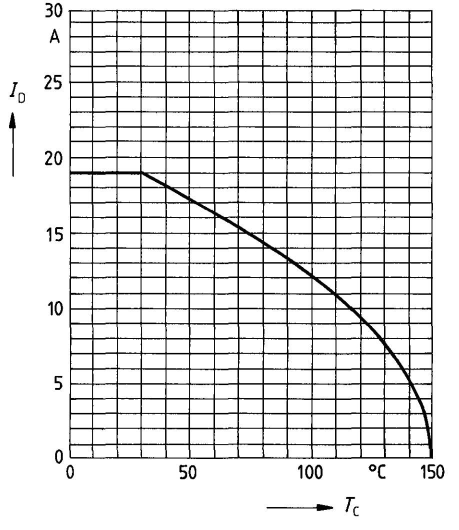
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



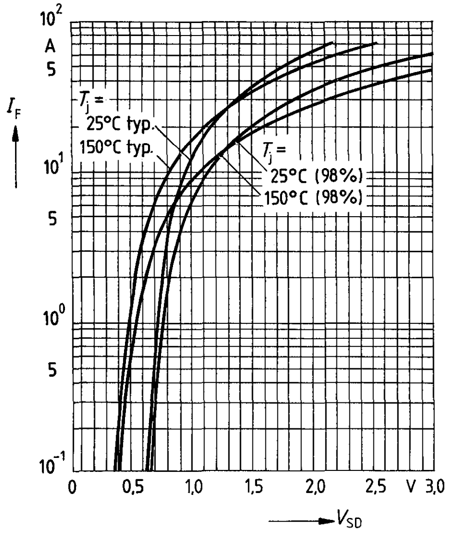
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



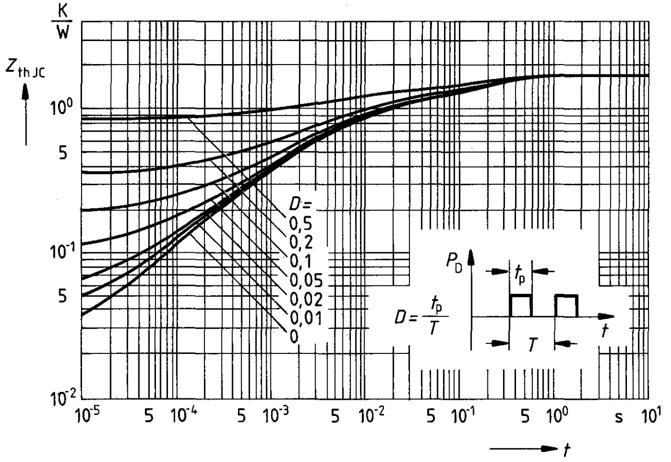
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



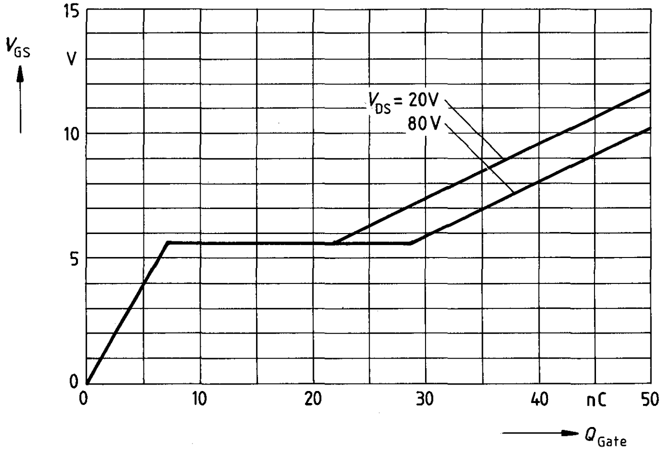
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

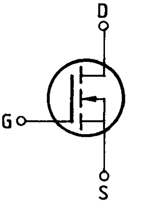


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 21A$



Main ratings

N-Channel

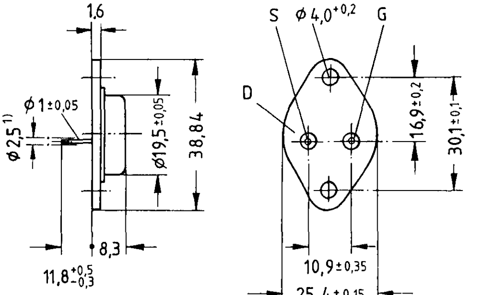


Drain-source voltage	V_{DS}	**= 100 V**
Continuous drain current	I_D	**= 10 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,2 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Metal case 3A2 in accordance with DIN 41872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 23	C67078-A1002-A2



1) max. bending area

Dimensions in mm

Maximum ratings

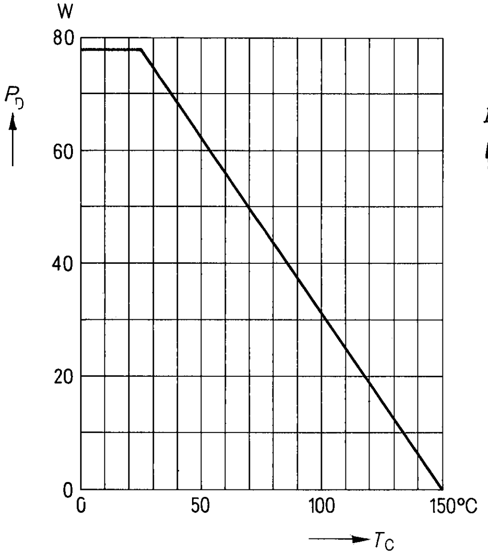
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	10	A	T_C = 85 °C
Pulsed drain current	I_{Dpuls}	40	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,6	K/W	
Chip – ambient	$R_{th\ JA}$	≤35	K/W	

Electrical characteristics

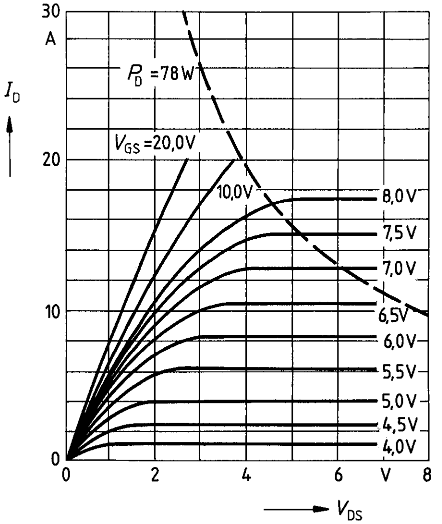
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,15	0,2	Ω	V_{GS} = 10V I_D = 6A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	4,0	–	S	V_{DS} = 25V I_D = 6A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	300	500		
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	50	75		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	10	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	40		
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,6	–	µC	

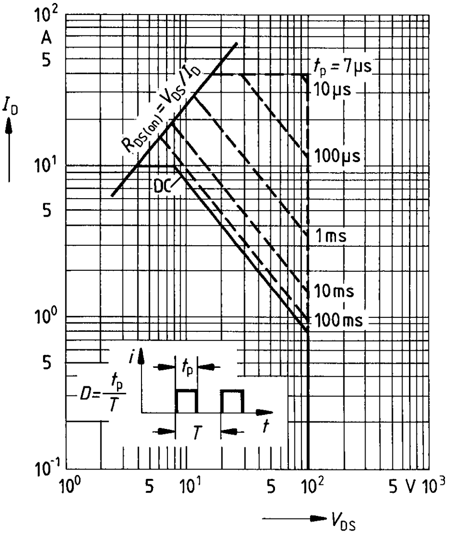
Power dissipation $P_D = f(T_C)$



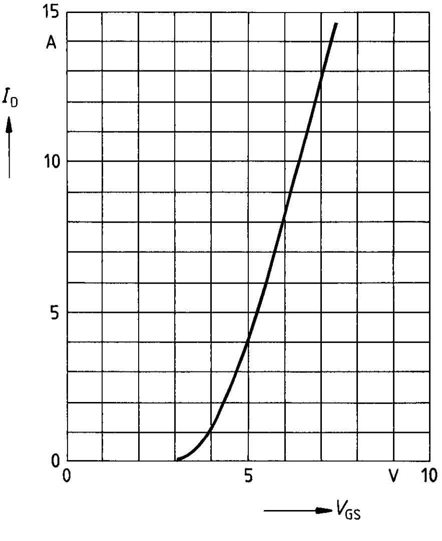
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



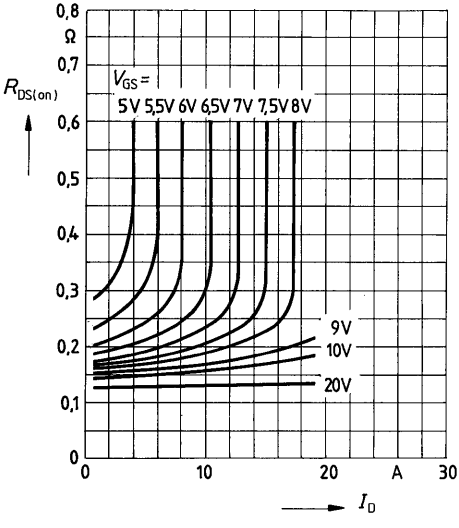
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



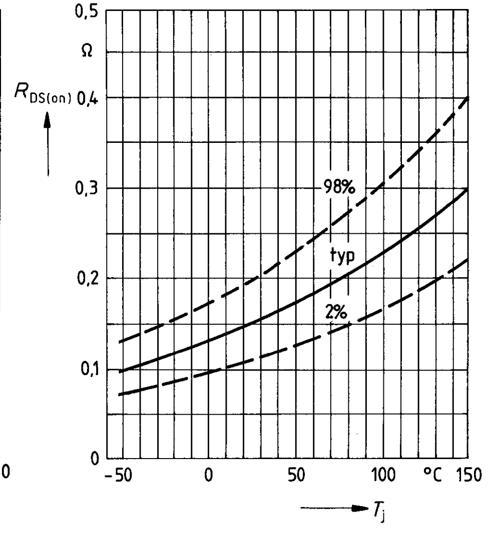
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



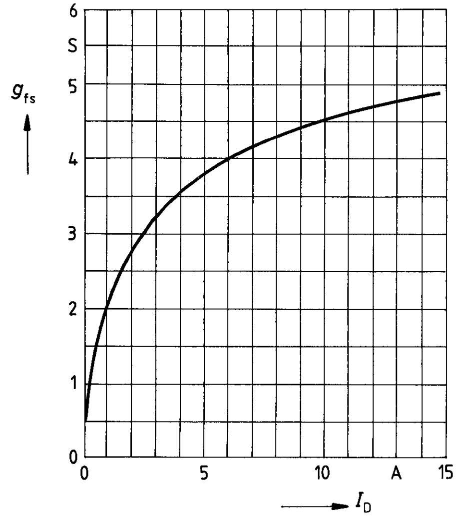
Typical drain-source on-state resistance
$R_{DS\,(on)} = f\,(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



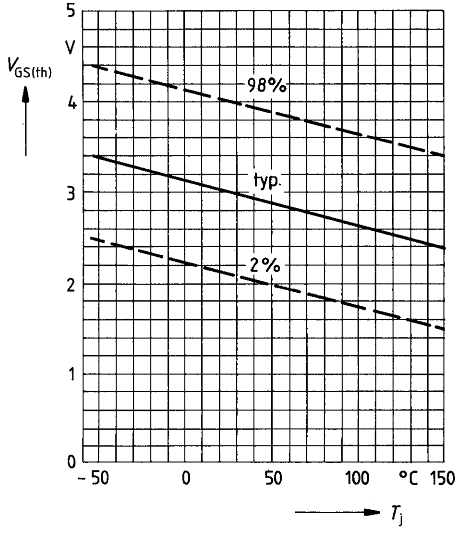
Drain-source on-state resistance
$R_{DS\,(on)} = f\,(T_j)$
parameter: I_D = 6A, V_{GS} = 10V
(spread)



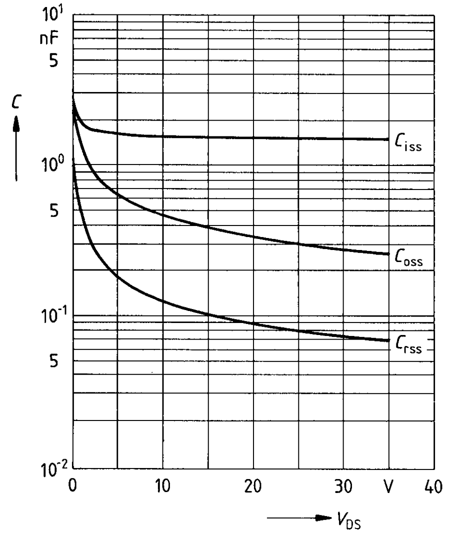
Typical transconductance $g_{fs} = f\,(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



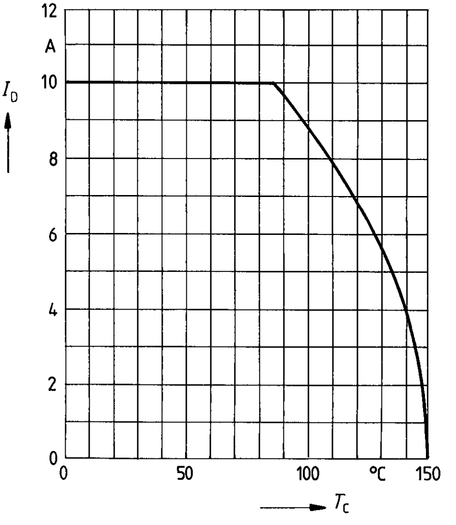
Gate threshold voltage $V_{GS(th)} = f\,(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



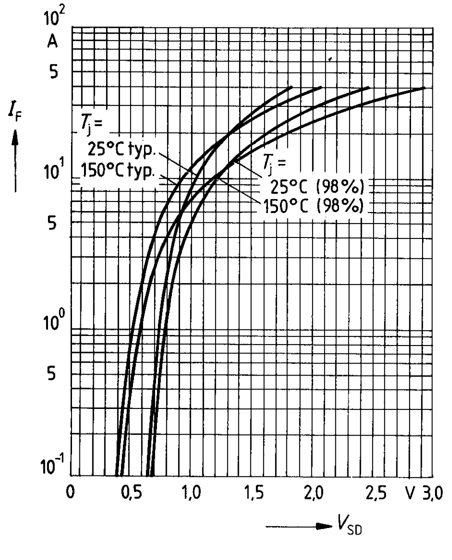
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



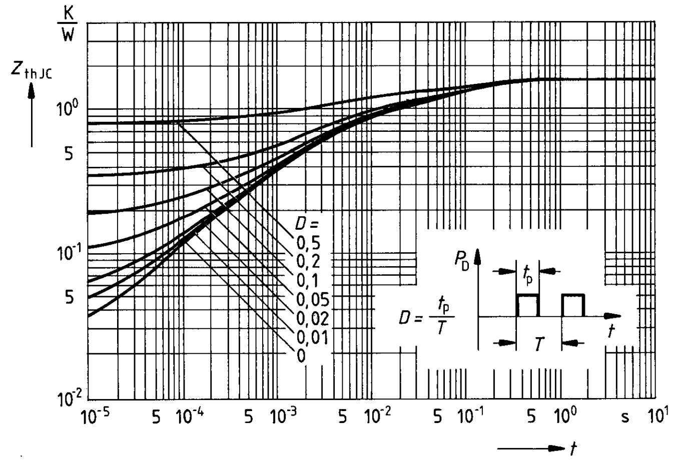
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



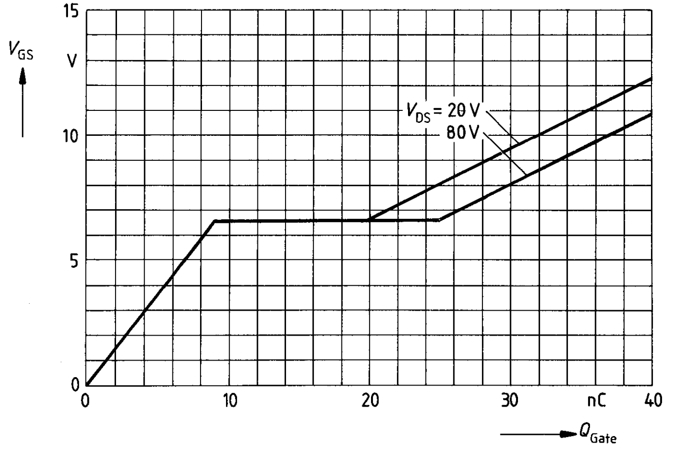
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu\text{s}$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



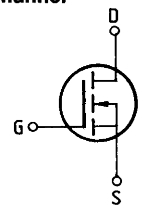
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 18A$



Main ratings

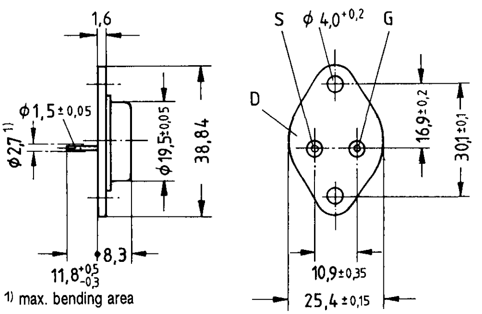
Drain-source voltage V_{DS} **= 100 V**
Continuous drain current I_D **= 32 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,06 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AE (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 24	C67078-A1003-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	32	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	125	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

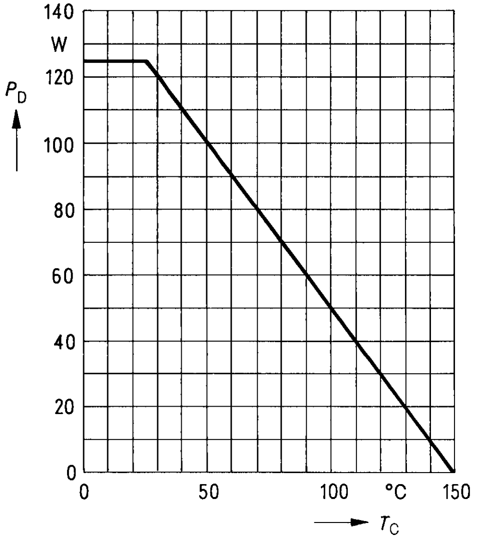
 S Preferred Type

Electrical characteristics

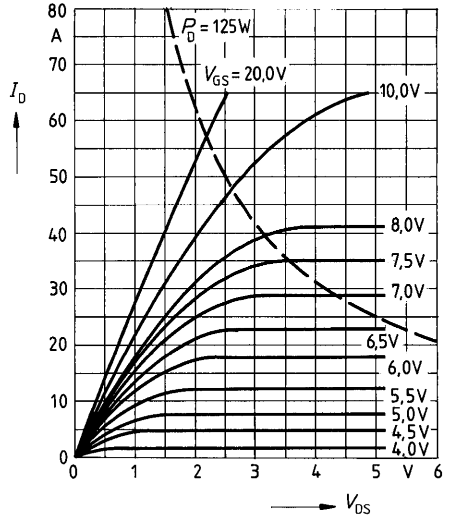
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,045	0,06	Ω	V_{GS} = 10V I_D = 16A
Dynamic ratings						
Forward transconductance	g_{fs}	6,0	10,0	–	S	V_{DS} = 25V I_D = 16A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	800	1200		
Reverse transfer capacitance	C_{rss}	–	300	500		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	170	220		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	32	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	125		
Diode forward on-voltage	V_{SD}	–	1,5	2,0	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,6	–	µC	

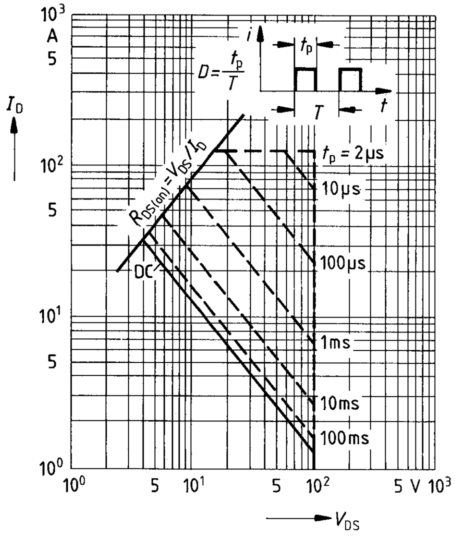
Power dissipation $P_D = f(T_C)$



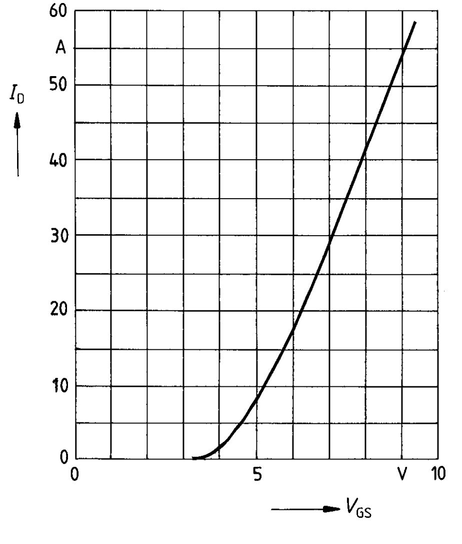
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



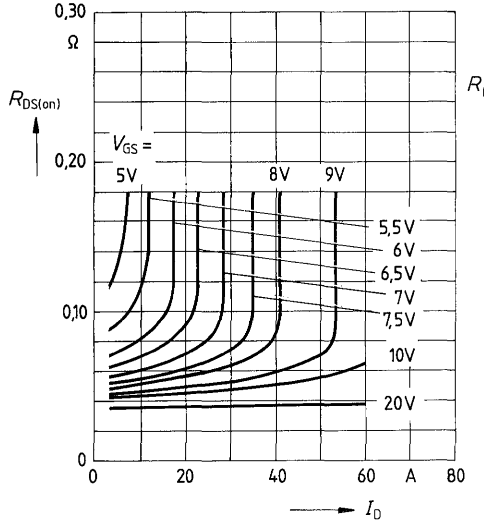
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



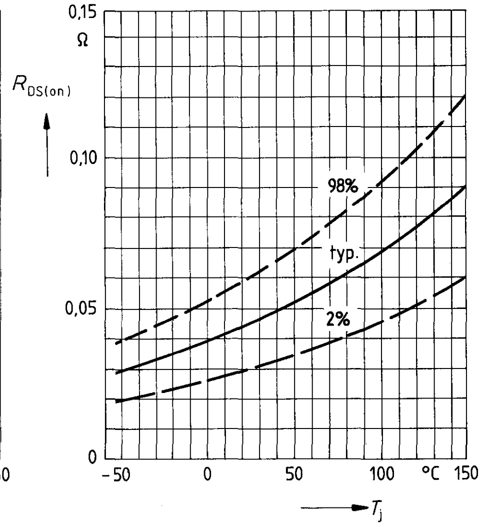
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



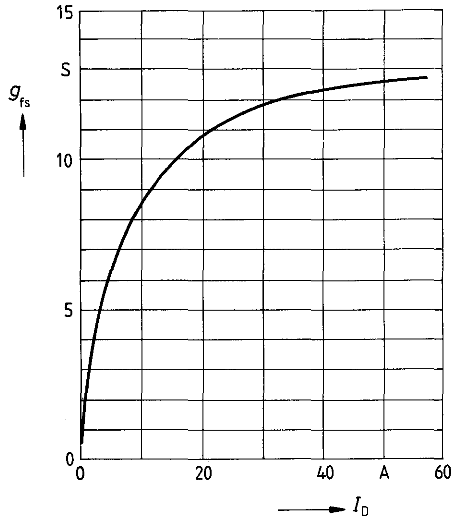
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



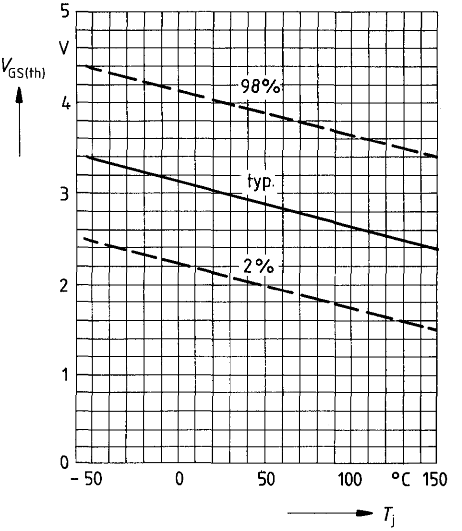
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 16A$, $V_{GS} = 10V$
(spread)



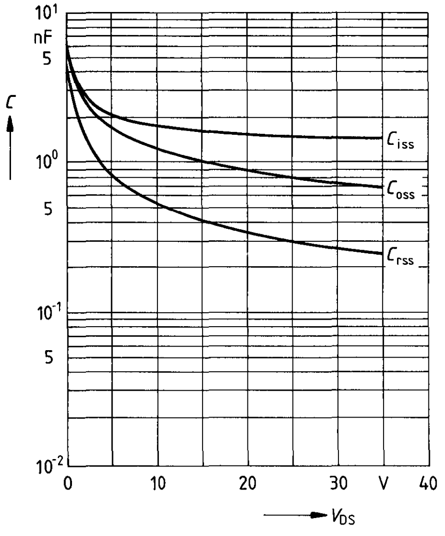
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



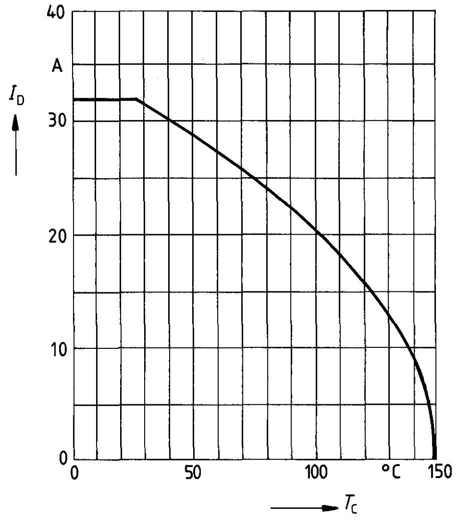
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



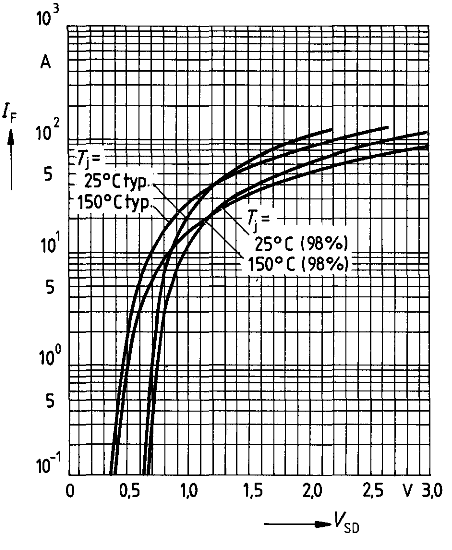
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



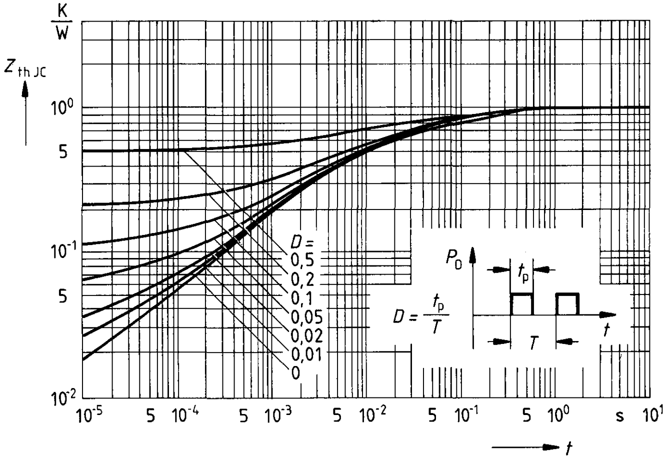
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



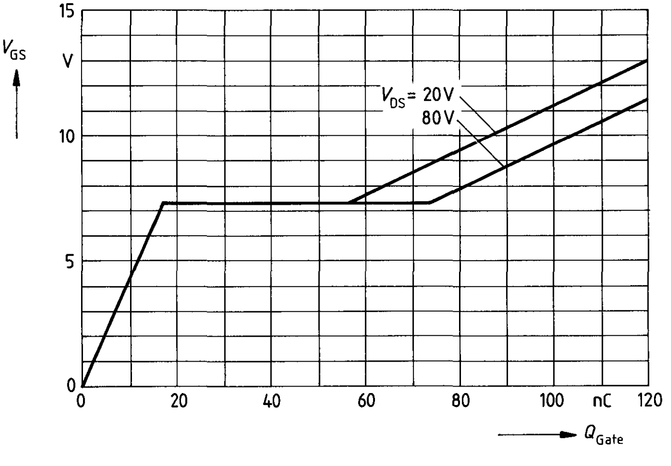
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



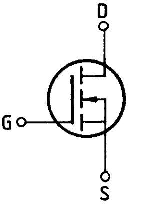
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 48A$



Main ratings

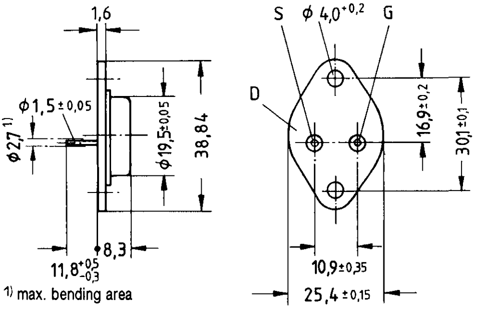
Drain-source voltage V_{DS} = **100 V**
Continuous drain current I_D = **19 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,1 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3A2 in accordance with DIN 41872, or TO 204 AE (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 25	C67078-A1011-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	19	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	75	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,6	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

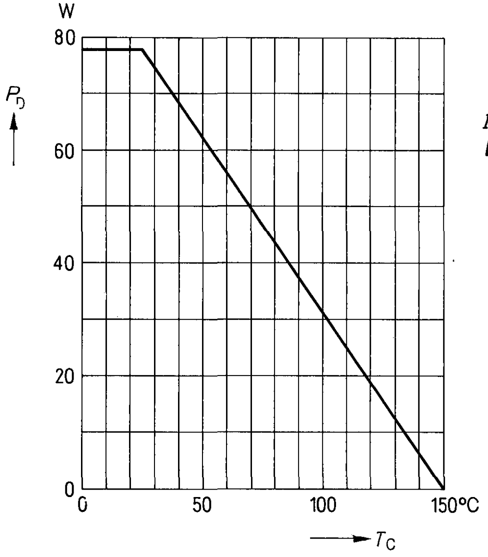
 S Preferred Type

Electrical characteristics

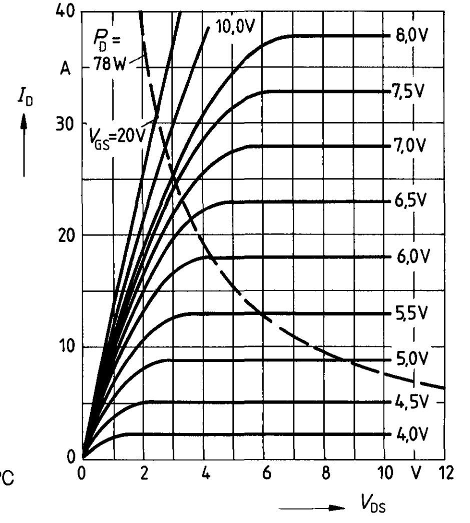
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,09	0,1	Ω	V_{GS} = 10V I_D = 9A
Dynamic ratings						
Forward transconductance	g_{fs}	4,0	8,0	–	S	V_{DS} = 25V I_D = 9A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	450	700		
Reverse transfer capacitance	C_{rss}	–	150	240		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	50	75		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	170	220		
	t_f	–	80	110		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	19	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	75		
Diode forward on-voltage	V_{SD}	–	1,5	2,1	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,25	–	µC	

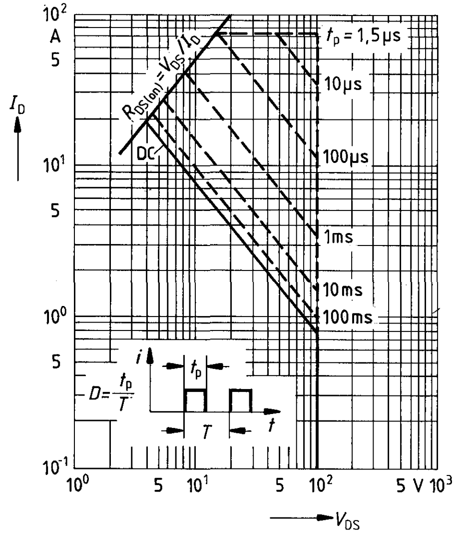
Power dissipation $P_D = f(T_C)$



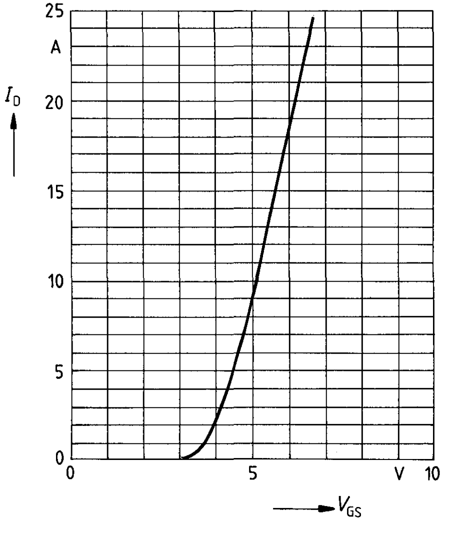
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



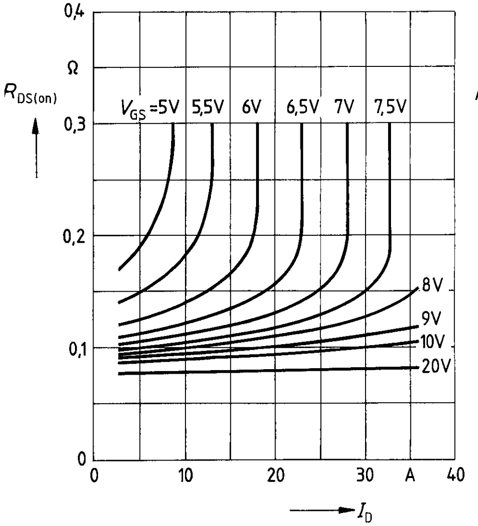
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



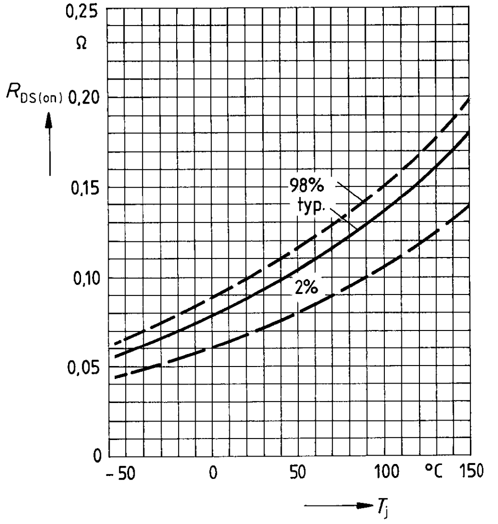
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



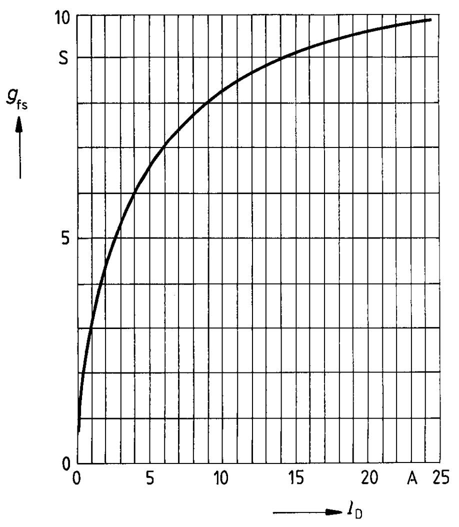
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



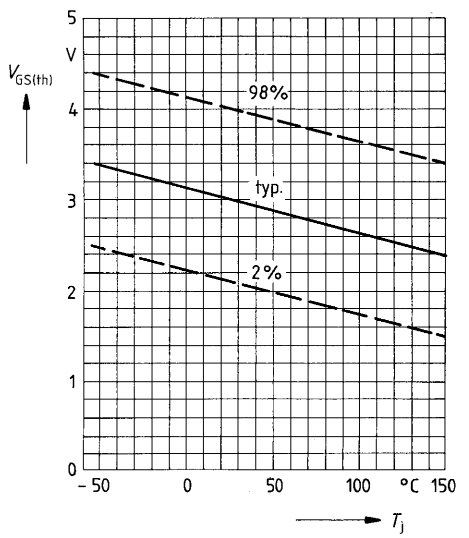
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 9A$, $V_{GS} = 10V$
(spread)



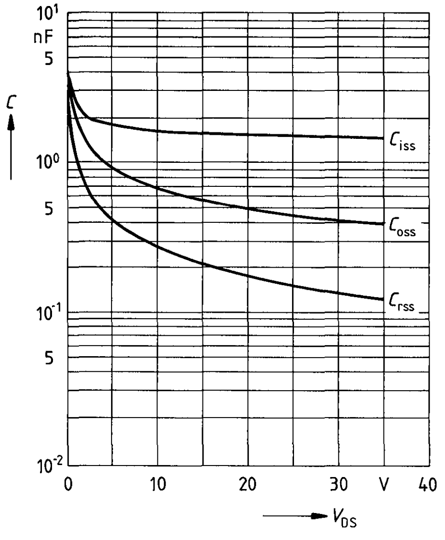
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



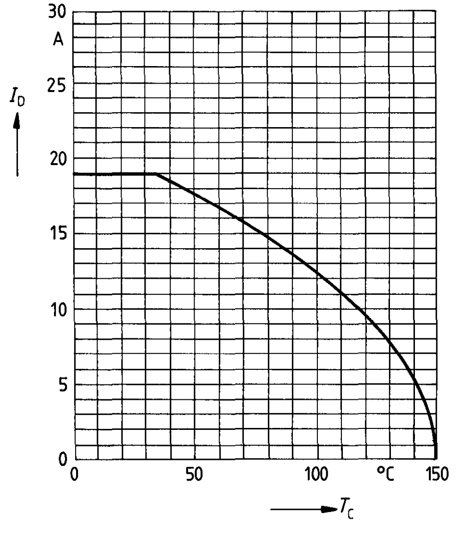
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



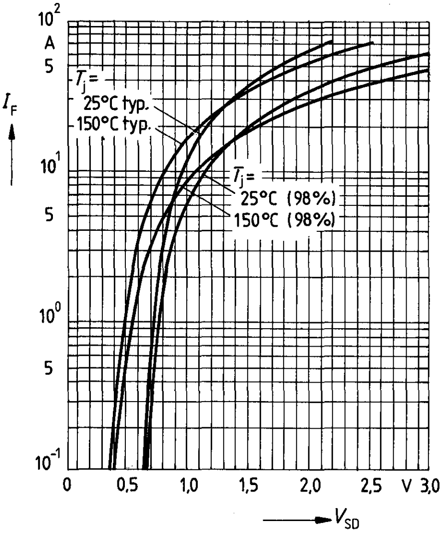
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



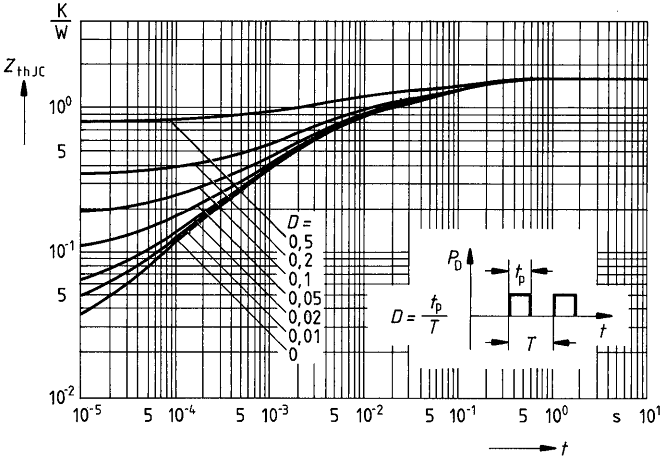
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



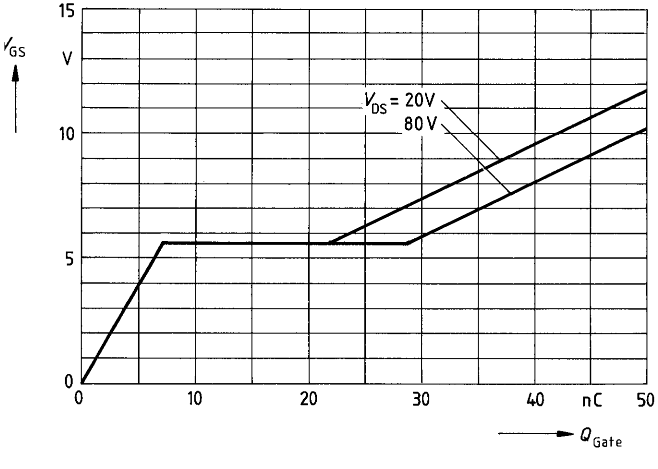
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

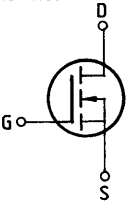


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 28{,}5A$



Main ratings

N-Channel

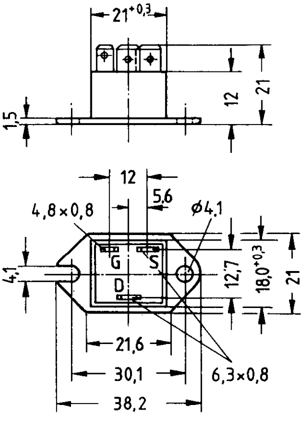


Drain-source voltage	V_{DS}	**= 100 V**
Continuous drain current	I_D	**= 26 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,06 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
S BUZ 27	C67078-A1602-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	26	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	100	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 … +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,5	K/W	

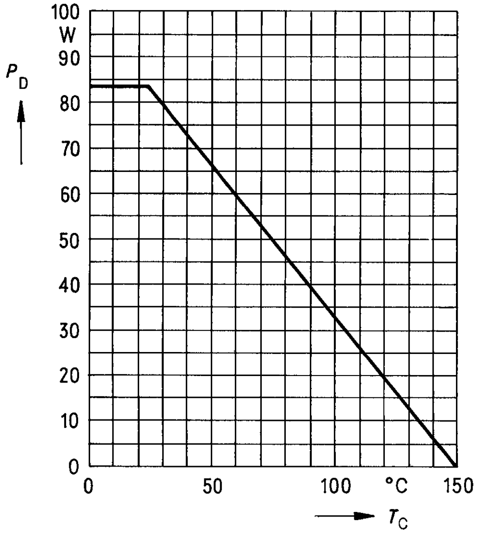
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

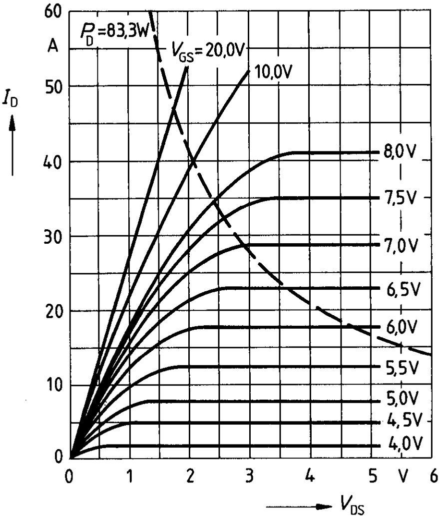
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,045	0,06	Ω	V_{GS} = 10V I_D = 16A
Dynamic ratings						
Forward transconductance	g_{fs}	6,0	10,0	–	S	V_{DS} = 25V I_D = 16A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	800	1200		
Reverse transfer capacitance	C_{rss}	–	300	500		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	170	220		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	26	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	100		
Diode forward on-voltage	V_{SD}	–	1,4	1,8	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,6	–	µC	

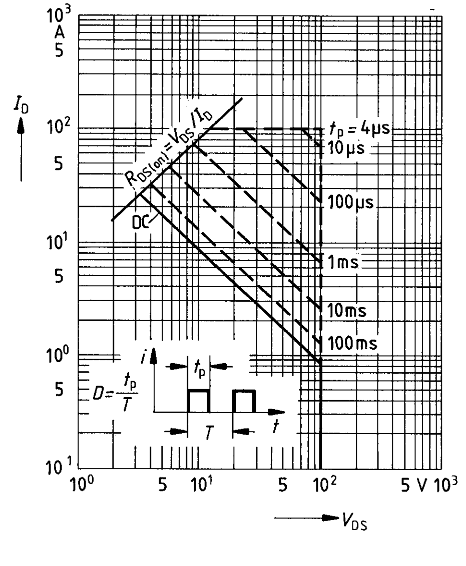
Power dissipation $P_D = f(T_C)$



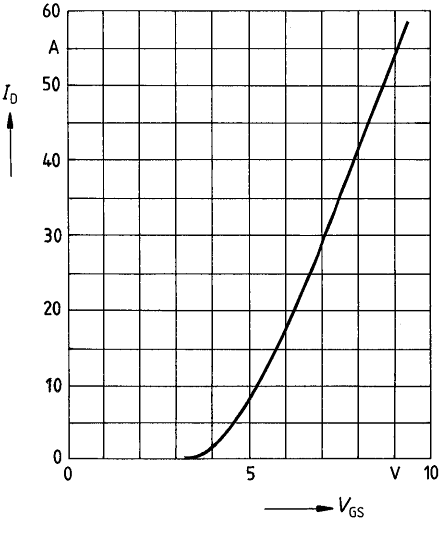
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



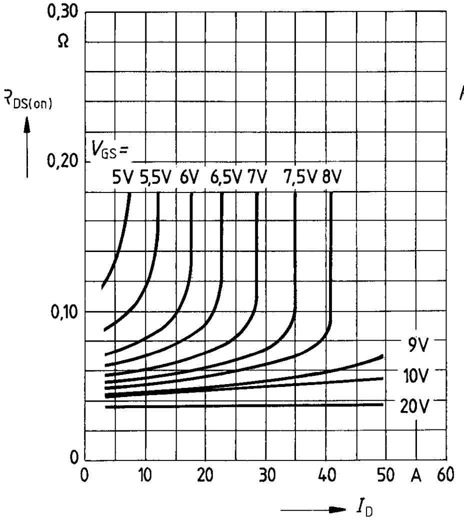
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



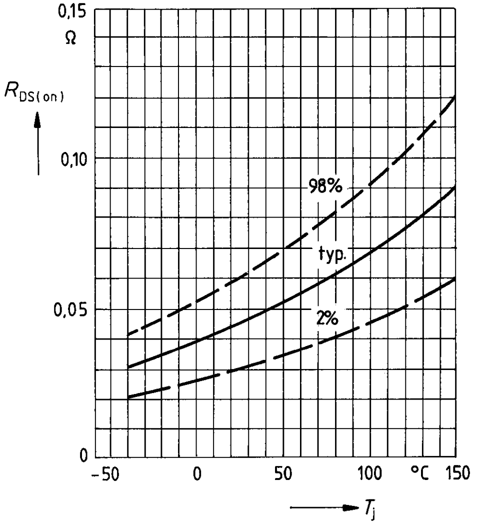
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



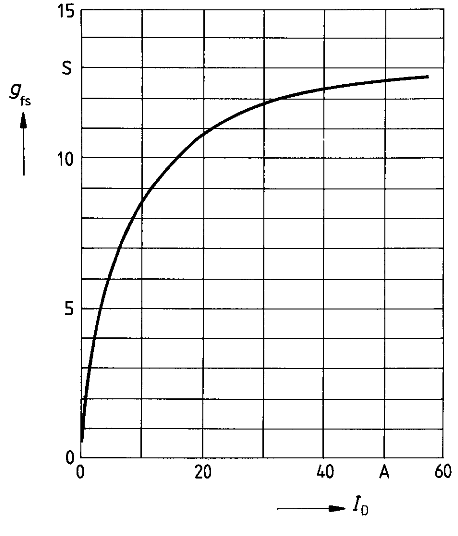
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



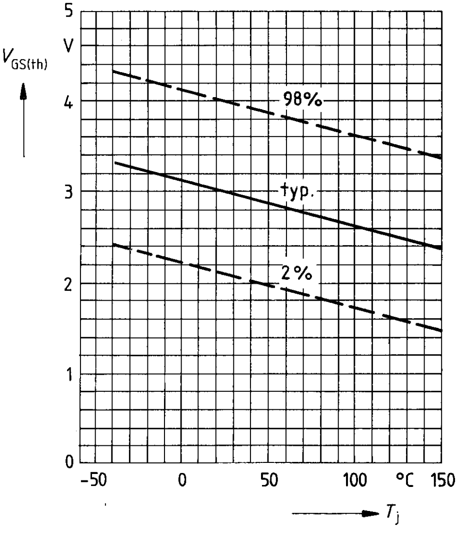
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 16A, V_{GS} = 10V
(spread)



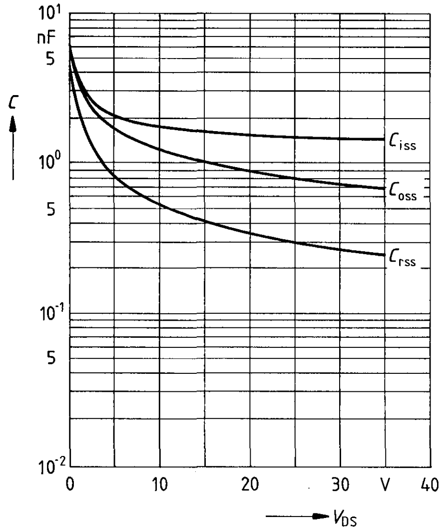
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



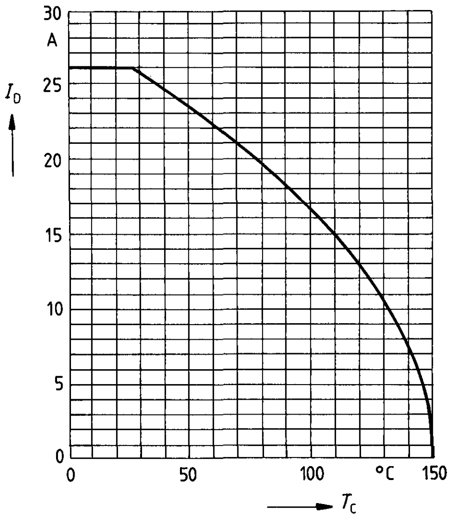
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



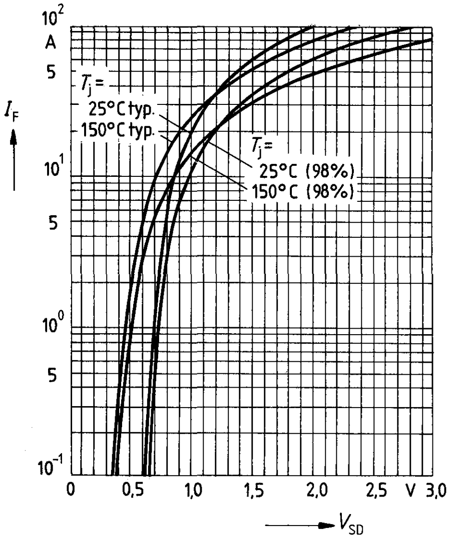
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



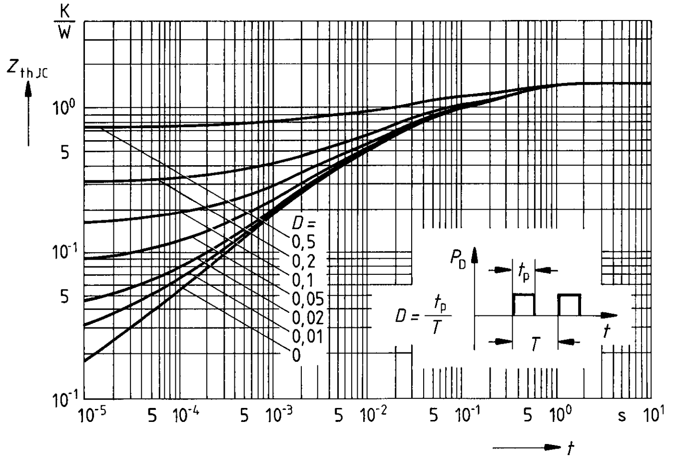
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



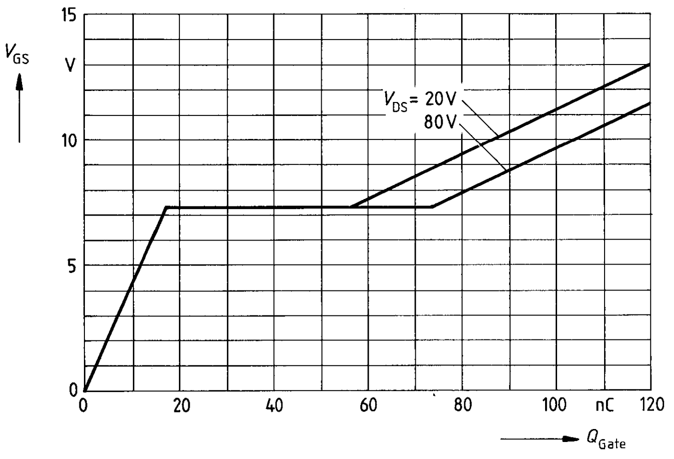
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

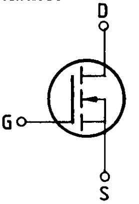


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 48A$



Main ratings

N-Channel



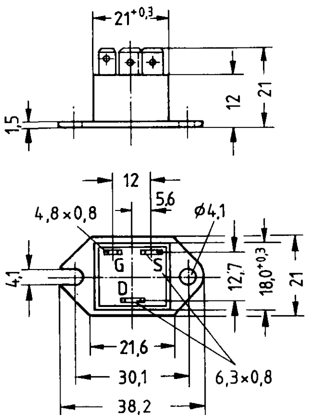
Drain-source voltage	V_{DS}	**= 100 V**
Continuous drain current	I_D	**= 18 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,1 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 28	C67078-A1608-A2

Not for new design



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	18	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	70	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	70	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 … +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\,JC}$	≤1,78	K/W

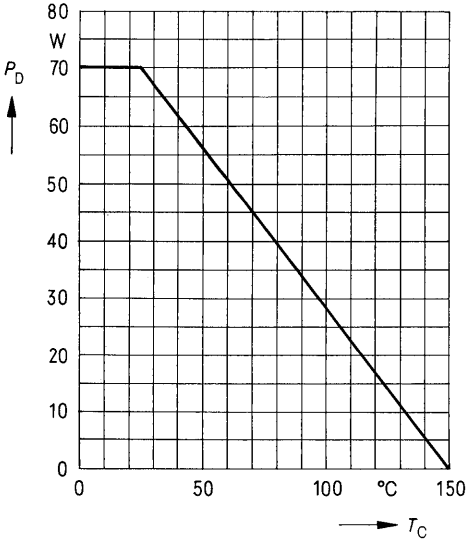
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

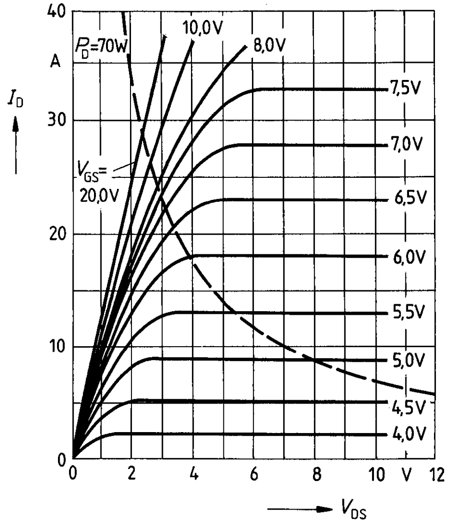
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	μA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	0,09	0,1	Ω	V_{GS} = 10V I_D = 9A
Dynamic ratings						
Forward transconductance	g_{fs}	4,0	8,0	–	S	V_{DS} = 25V I_D = 9A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	450	700		
Reverse transfer capacitance	C_{rss}	–	150	240		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	50	75		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	170	220		
	t_f	–	80	110		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	18	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	70		
Diode forward on-voltage	V_{SD}	–	1,4	2,0	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/μs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,25	–	μC	

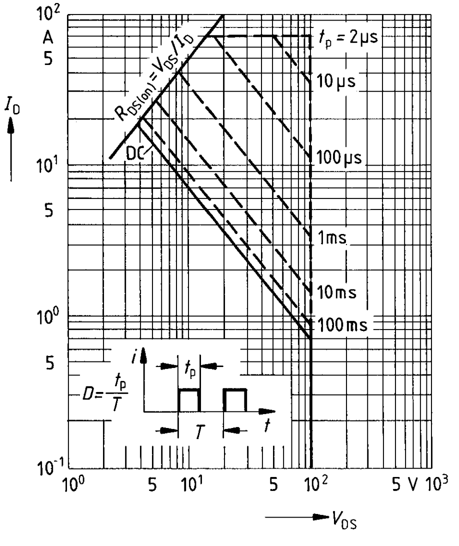
Power dissipation $P_D = f(T_C)$



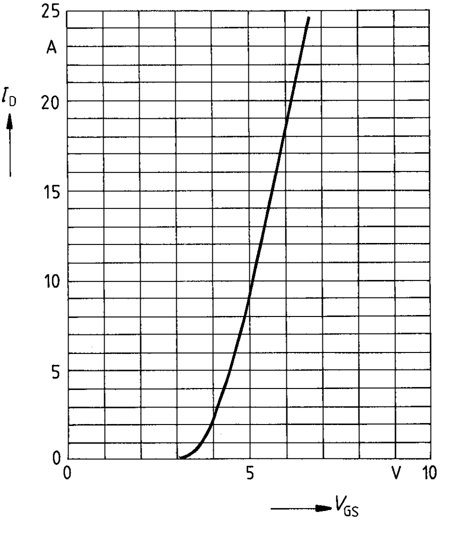
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



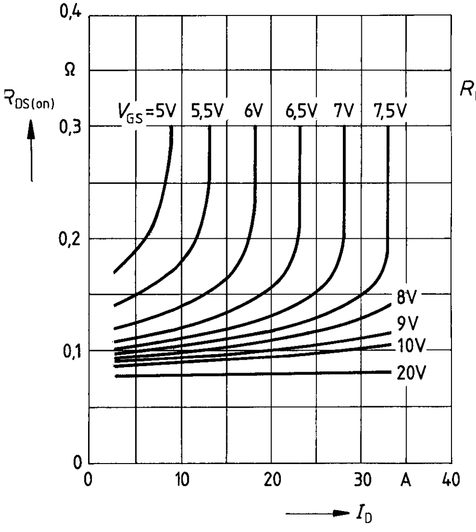
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



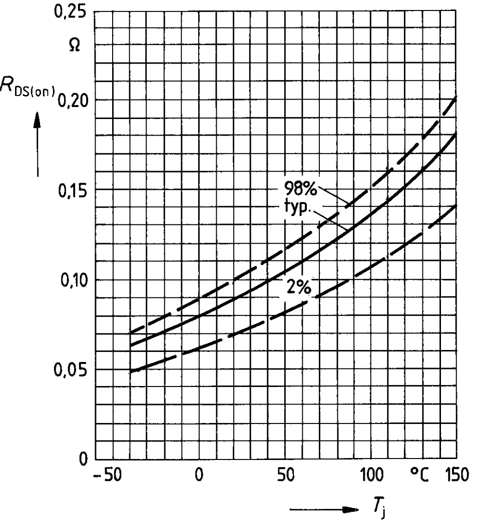
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



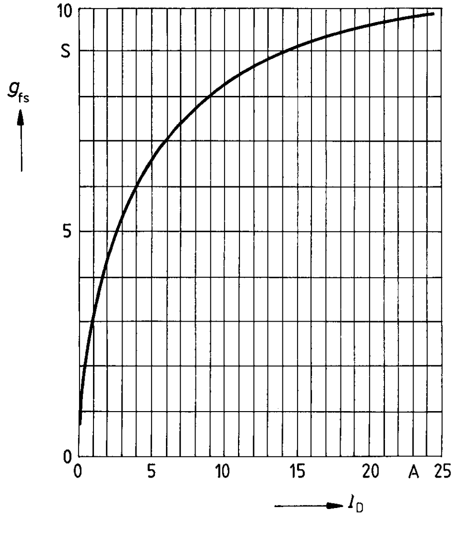
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



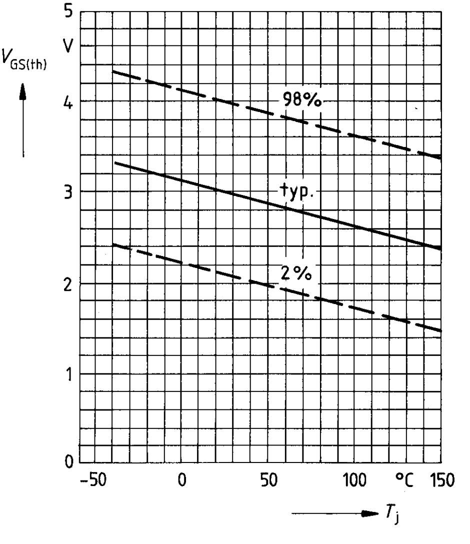
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 9A$, $V_{GS} = 10V$
(spread)



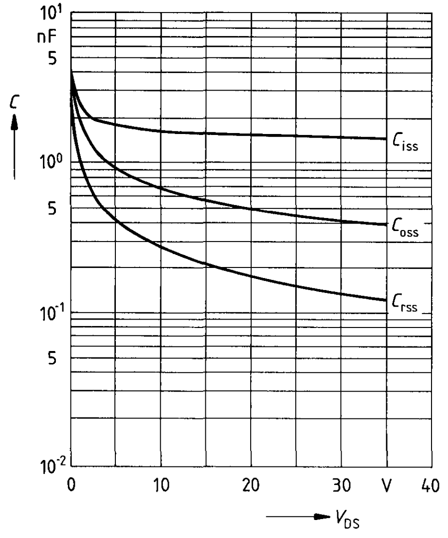
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



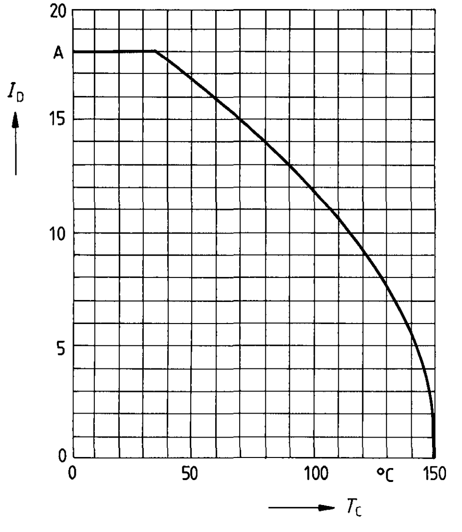
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



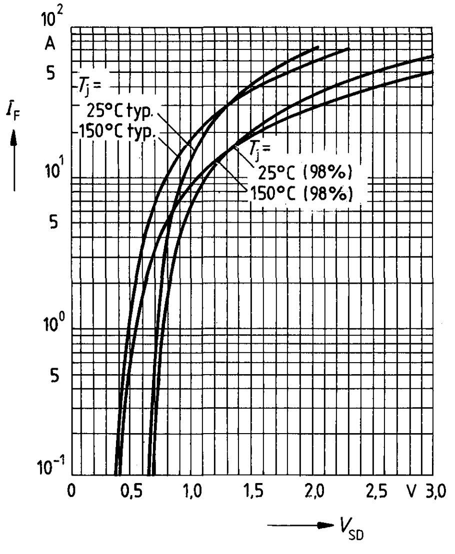
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, f = 1MHz



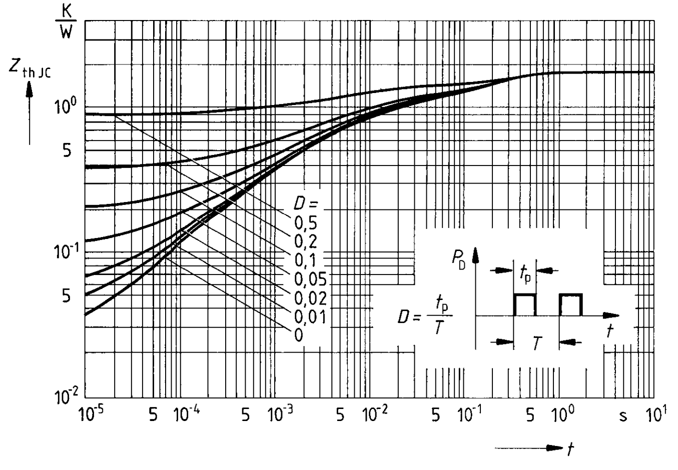
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



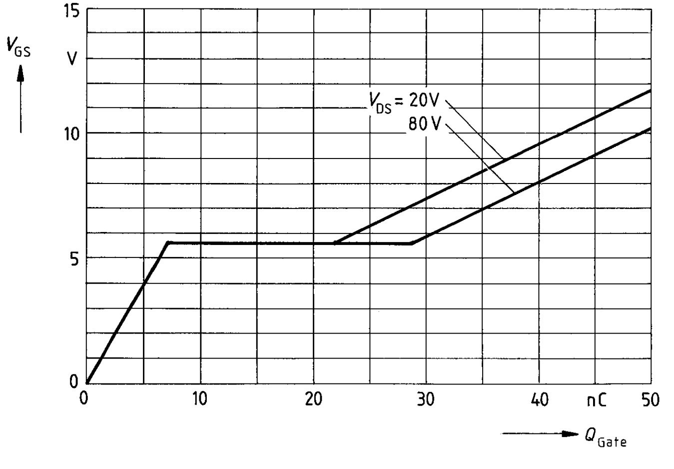
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, t_p = 80 µs
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



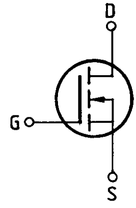
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 28{,}5A$



Main ratings

Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 12,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,2 Ω**

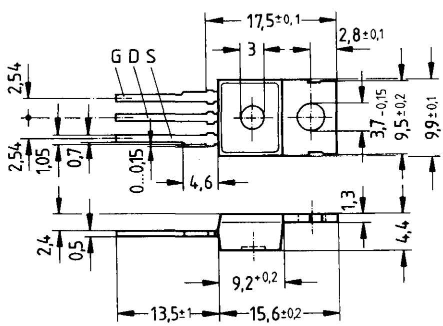
N-Channel



Description SIPMOS, N-channel, enhancement mode

Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 31	C67078-A1304-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	12,5	A	T_C = 45 °C
Pulsed drain current	I_{Dpuls}	50	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

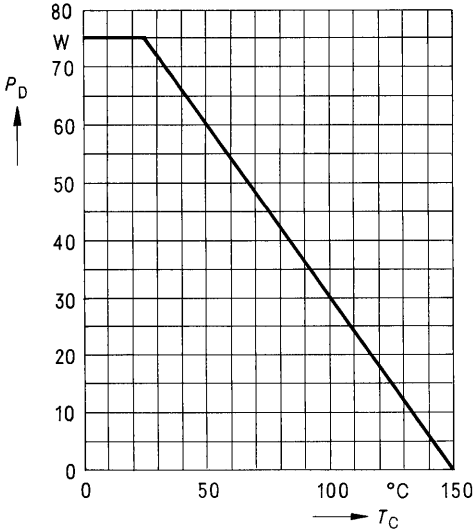
 S Preferred Type

Electrical characteristics

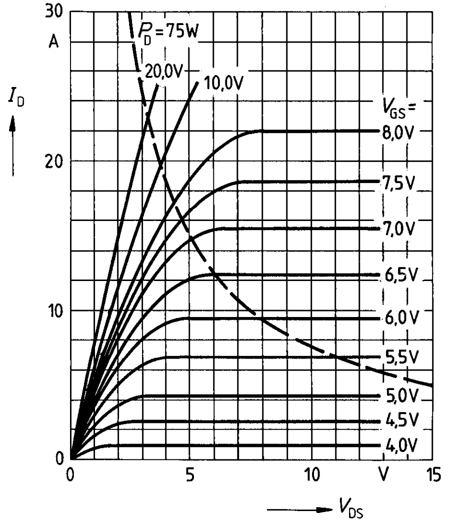
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,17	0,2	Ω	V_{GS} = 10V I_D = 7A
Dynamic ratings						
Forward transconductance	g_{fs}	3,0	5,0	–	S	V_{DS} = 25V I_D = 7A
Input capacitance	C_{iss}	–	900	1400	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	300	500		
Reverse transfer capacitance	C_{rss}	–	140	250		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	170	220		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	12,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	50		
Diode forward on-voltage	V_{SD}	–	1,4	1,8	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	400	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

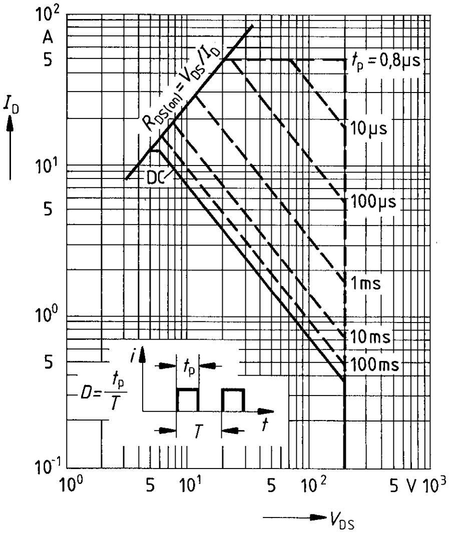
Power dissipation $P_D = f(T_C)$



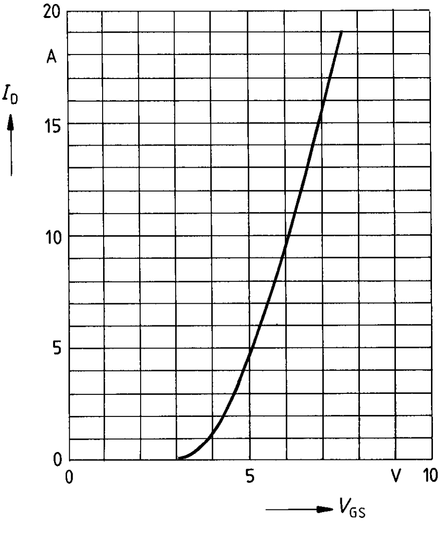
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 μs pulse test,
$T_j = 25\,°C$



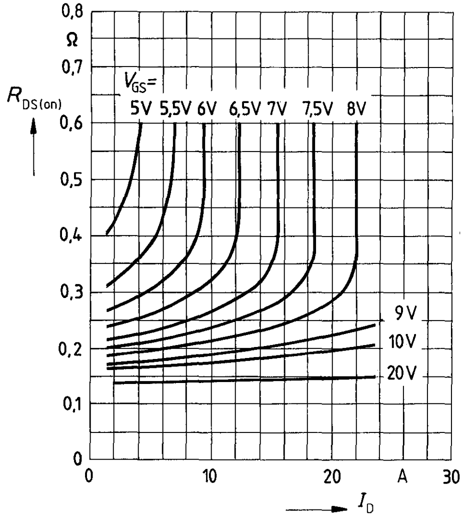
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



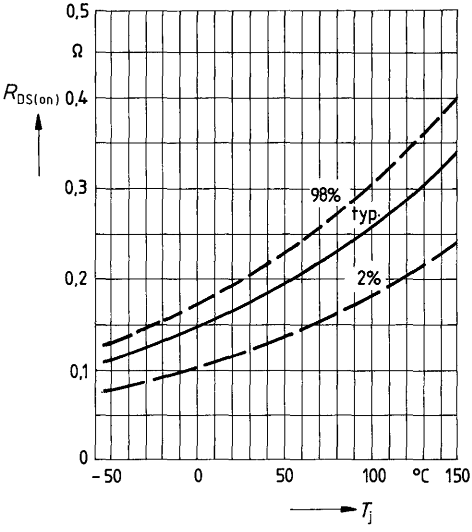
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 μs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



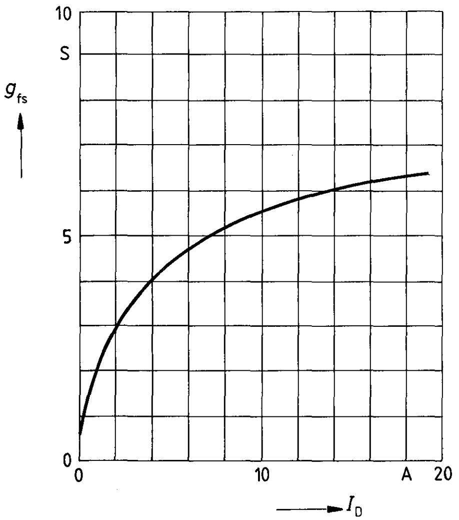
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



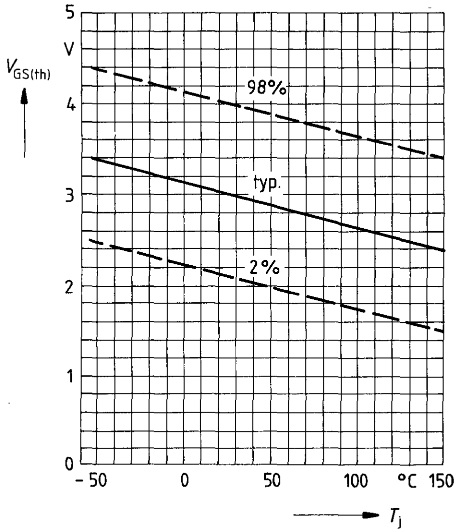
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 7A$, $V_{GS} = 10V$
(spread)



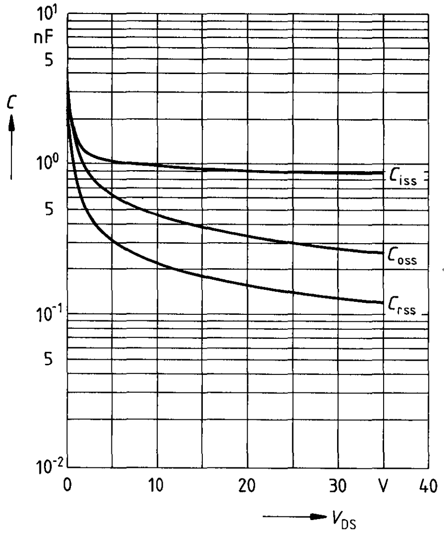
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



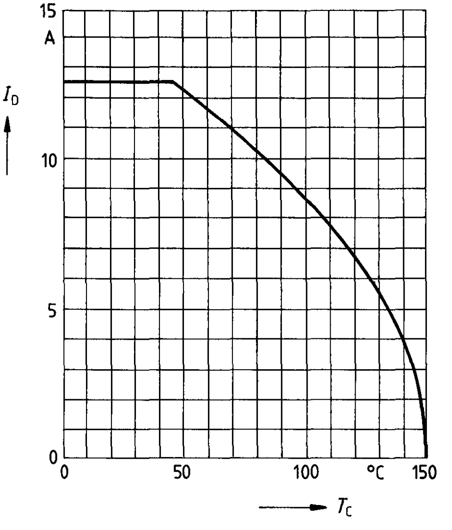
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



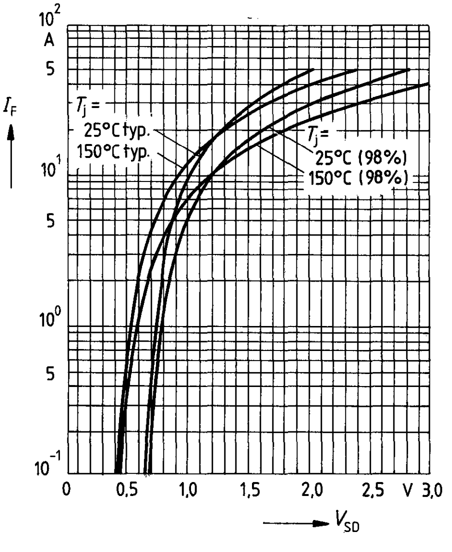
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



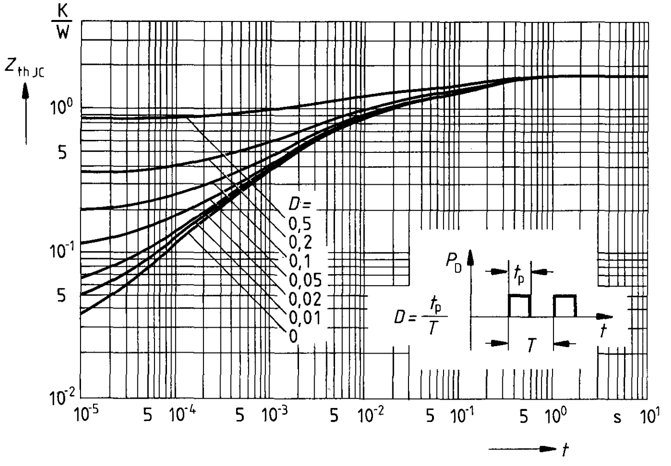
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



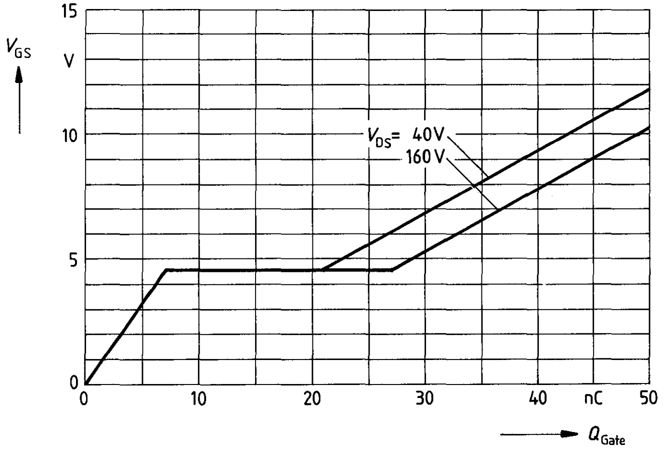
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



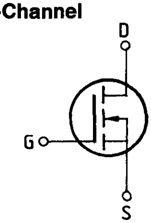
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls}$ = 18,8A



Main ratings

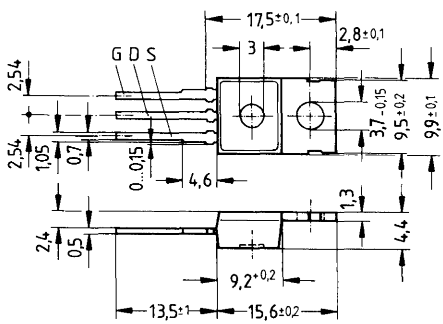
Drain-source voltage V_{DS} = **200 V**
Continuous drain current I_D = **9,5 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,4 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
S BUZ 32	C67078-A1310-A2



Dimensions in mm

Maximum ratings

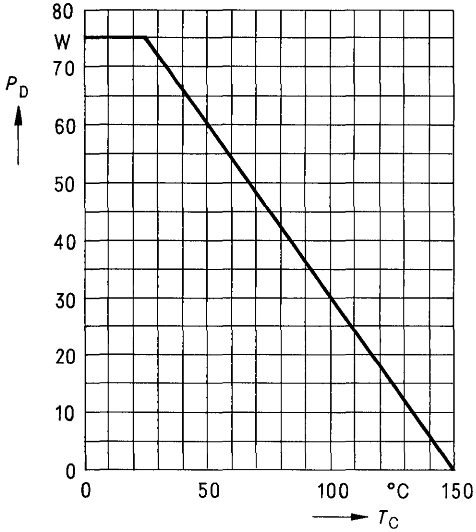
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	9,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	38	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j, T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

 S Preferred Type

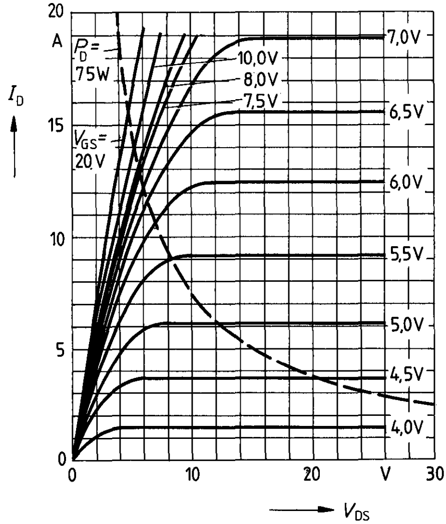
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	0,35	0,4	Ω	V_{GS} = 10V I_D = 4,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,2	5,0	–	S	V_{DS} = 25V I_D = 4,5A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400		
Reverse transfer capacitance	C_{rss}	–	70	120		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	9,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	38		
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	400	–	ns	T_j = 25 °C
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V

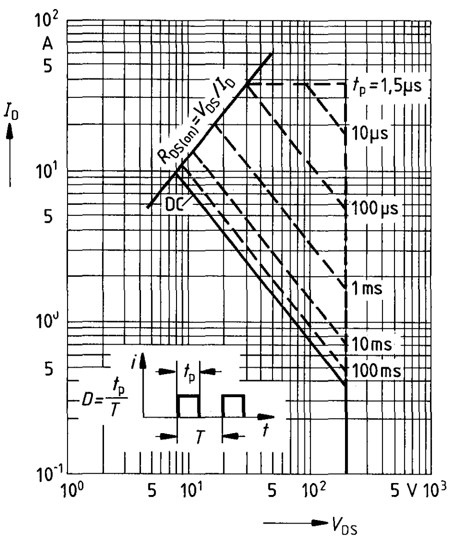
Power dissipation $P_D = f(T_C)$



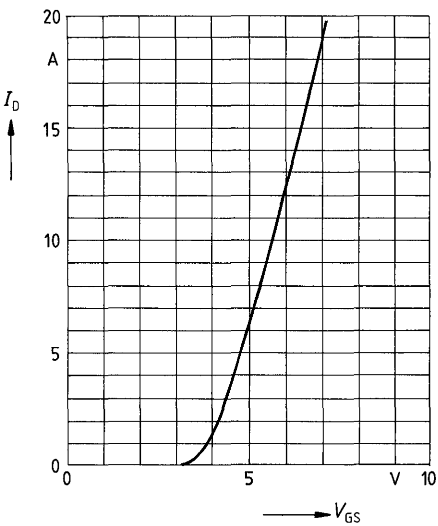
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



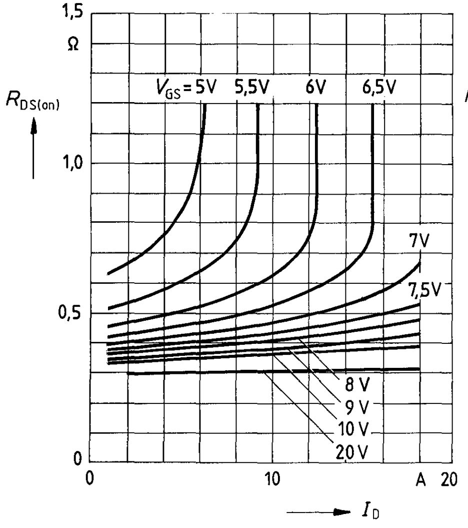
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



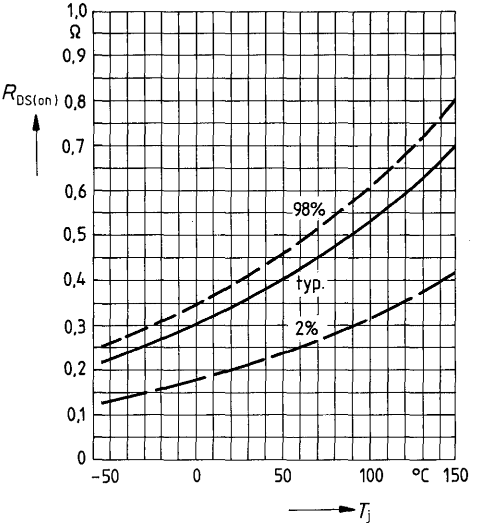
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



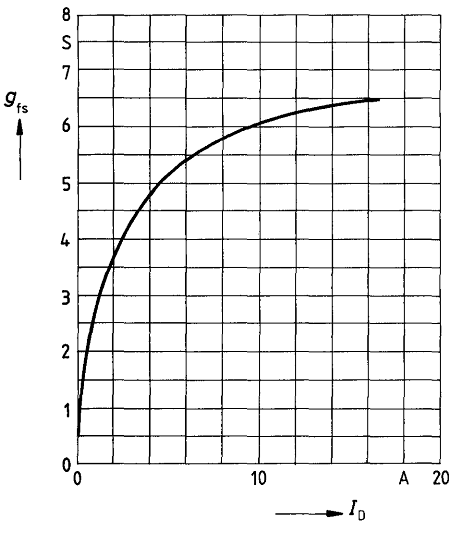
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



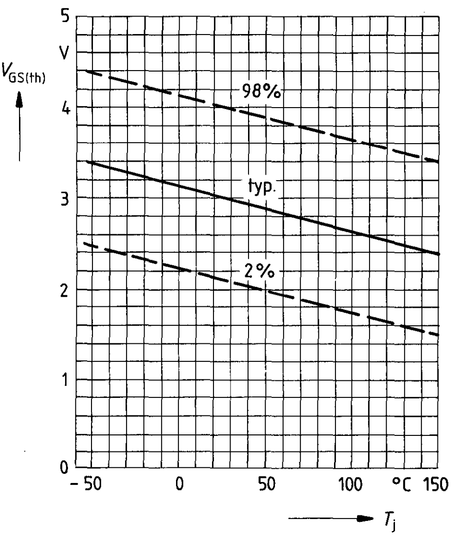
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 4,5A, V_{GS} = 10V
(spread)



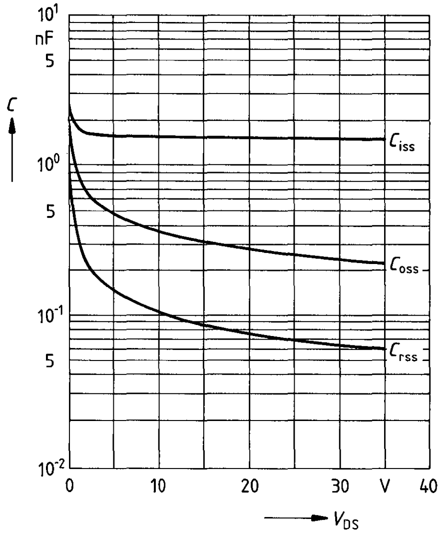
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



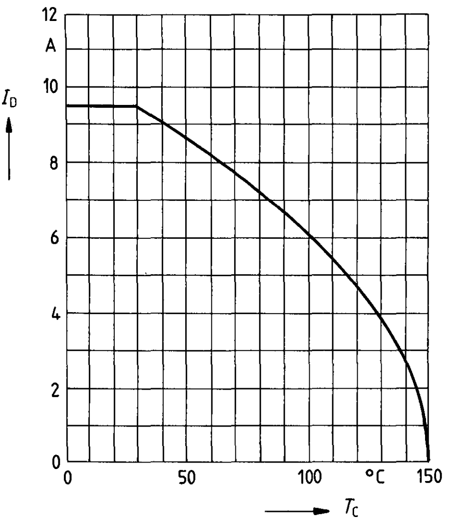
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



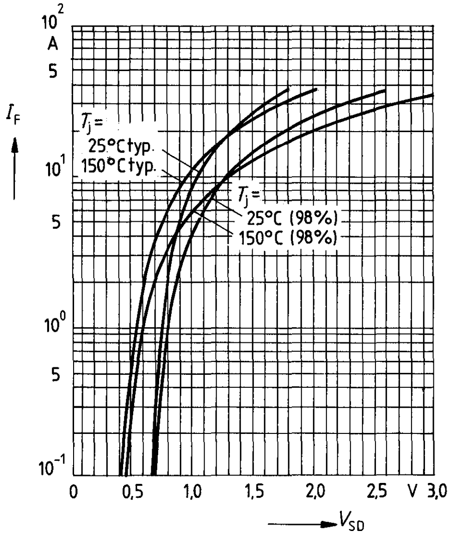
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



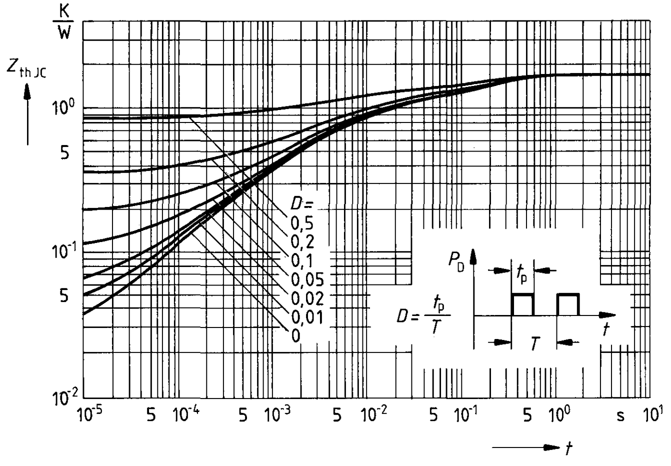
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



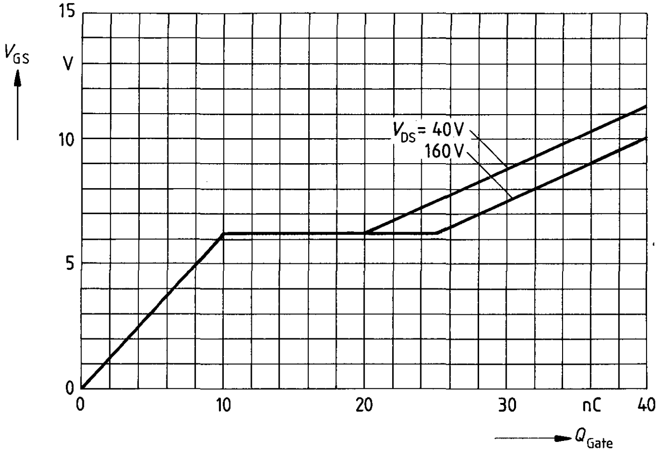
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



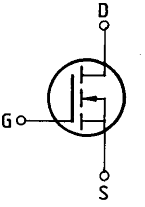
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14{,}3A$



Main ratings

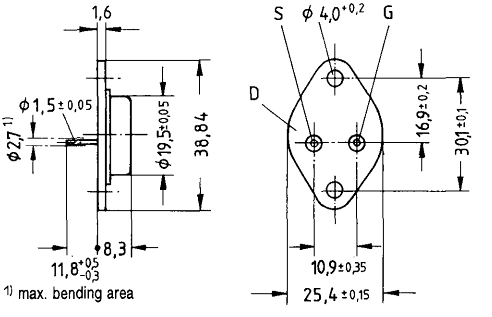
Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 14 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,2 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AE (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 34	C67078-A1005-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	14	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	56	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 … + 150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤ 1,6	K/W	
Chip – ambient	$R_{th\ JA}$	≤ 35	K/W	

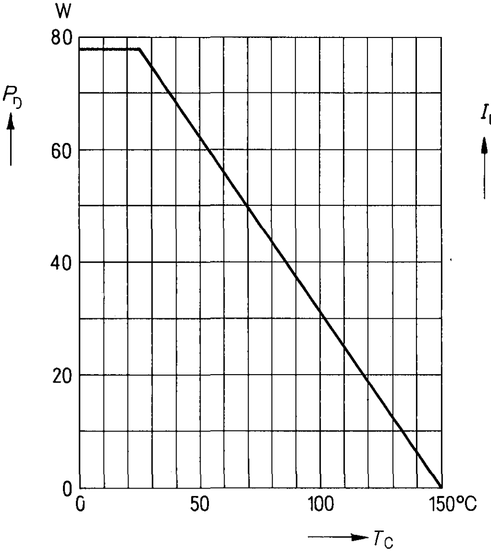
 S Preferred Type

Electrical characteristics

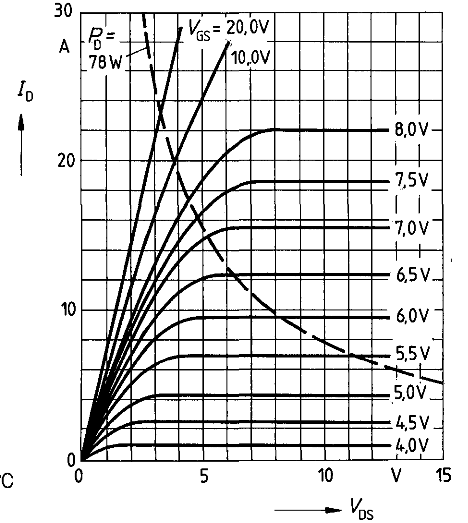
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,17	0,2	Ω	V_{GS} = 10V I_D = 7A
Dynamic ratings						
Forward transconductance	g_{fs}	3,0	5,0	–	S	V_{DS} = 25V I_D = 7A
Input capacitance	C_{iss}	–	900	1400	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	300	500		
Reverse transfer capacitance	C_{rss}	–	140	250		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	170	220		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	14	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	56		
Diode forward on-voltage	V_{SD}	–	1,5	1,9	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	400	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

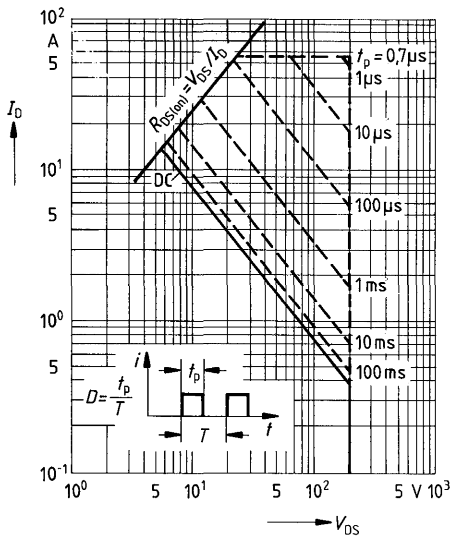
Power dissipation $P_D = f(T_C)$



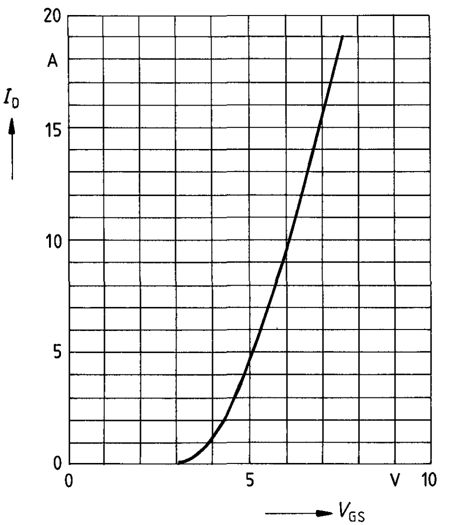
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



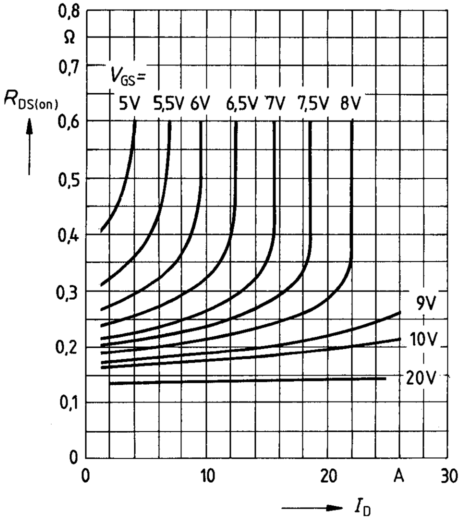
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



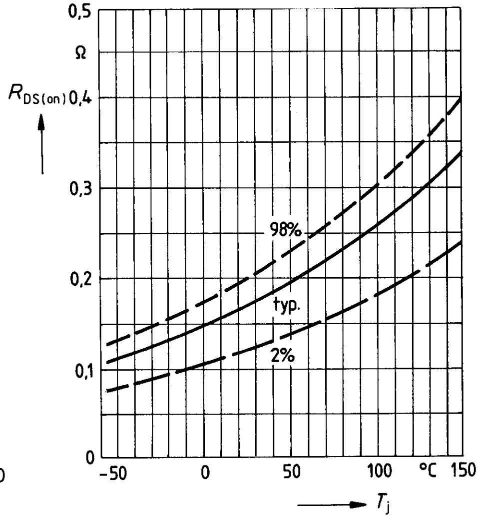
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



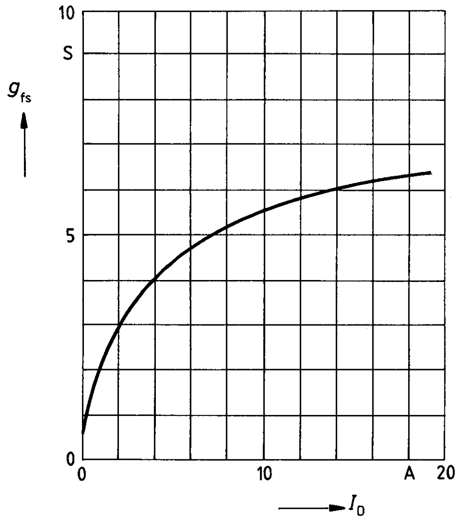
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



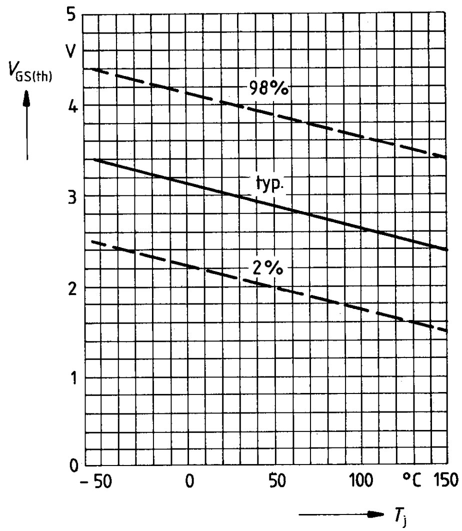
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 7A, V_{GS} = 10V
(spread)



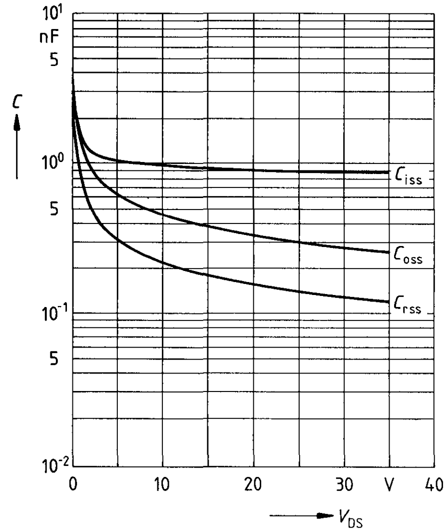
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



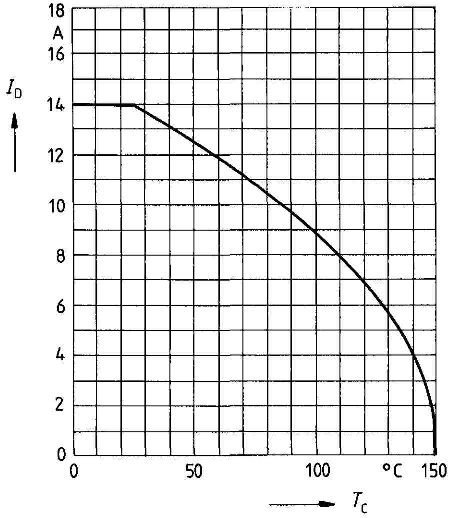
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



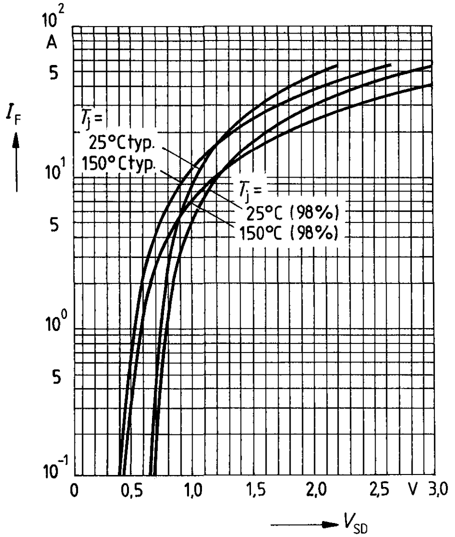
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



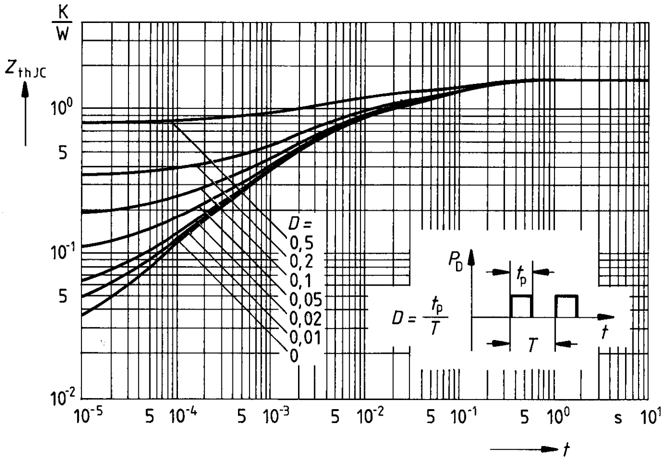
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



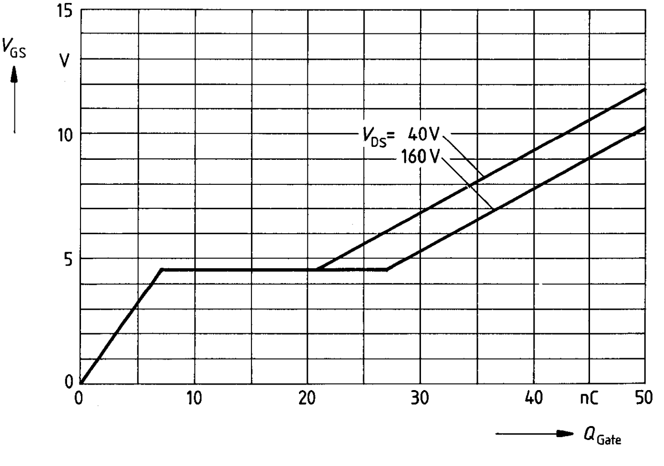
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



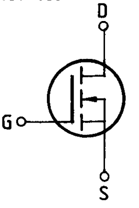
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 18{,}8A$



Main ratings

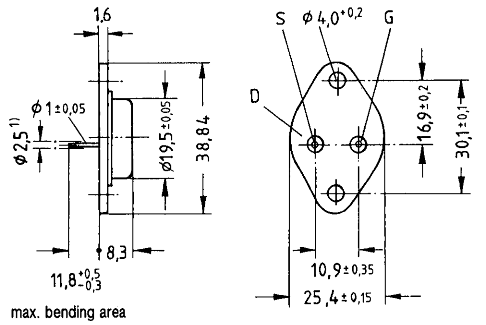
Drain-source voltage V_{DS} = **200 V**
Continuous drain current I_D = **9,9 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,4 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 35	C67078-A1014-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	9,9	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	39	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,6	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

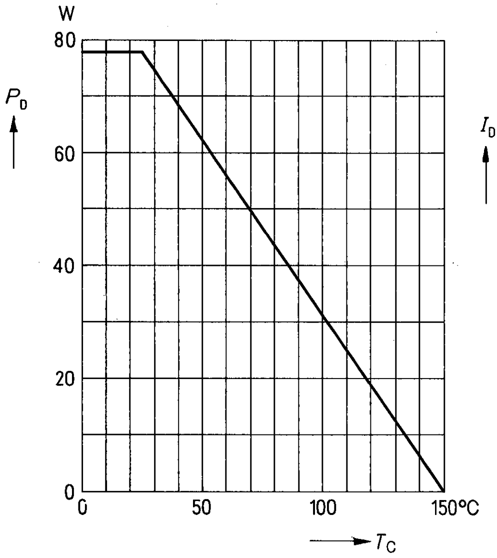
 S Preferred Type

Electrical characteristics

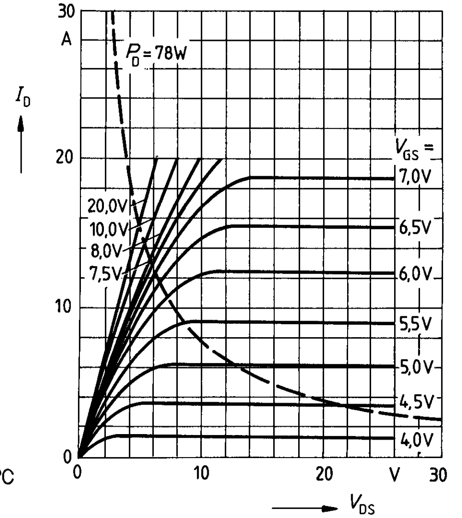
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,35	0,4	Ω	V_{GS} = 10V I_D = 4,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,2	5,0	–	S	V_{DS} = 25V I_D = 4,5A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400		
Reverse transfer capacitance	C_{rss}	–	70	120		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	9,9	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	39		
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	400	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

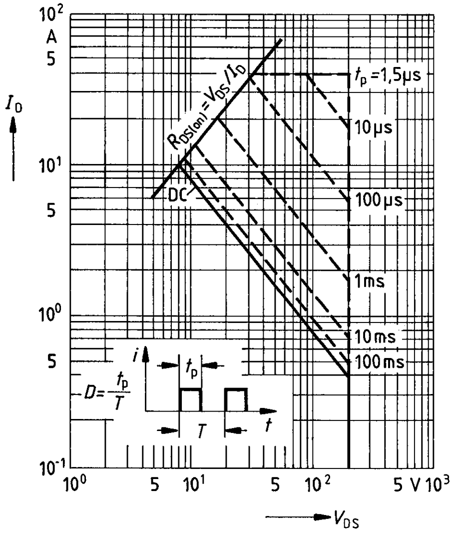
Power dissipation $P_D = f(T_C)$



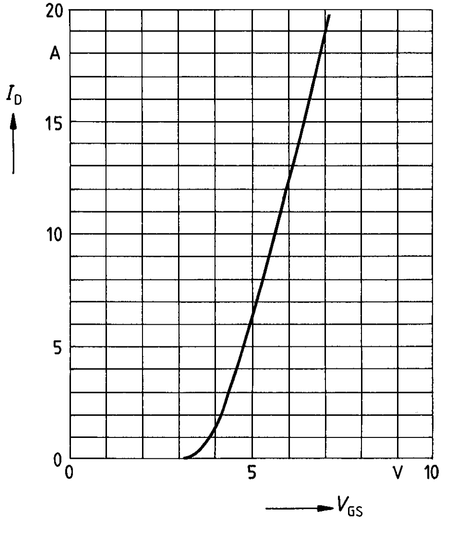
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



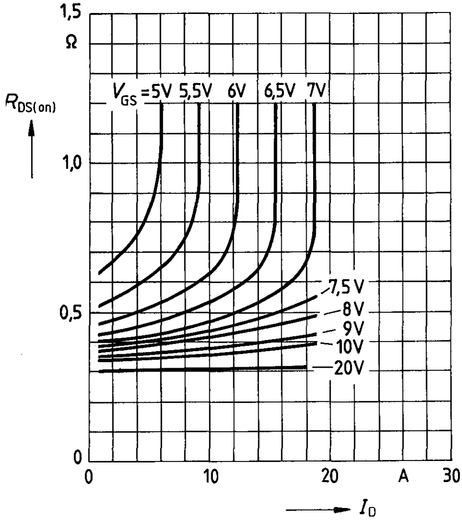
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



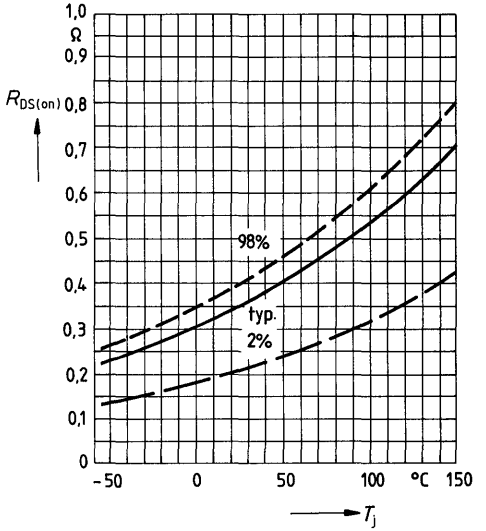
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



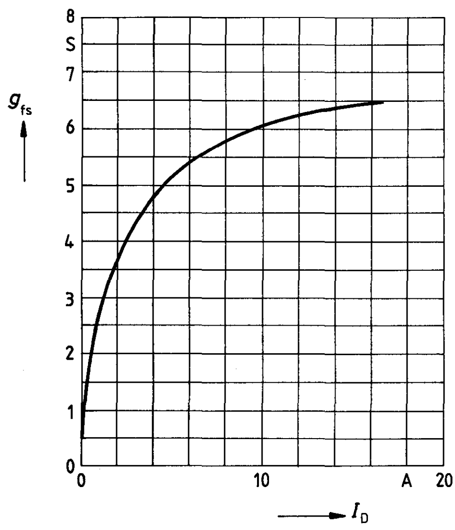
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



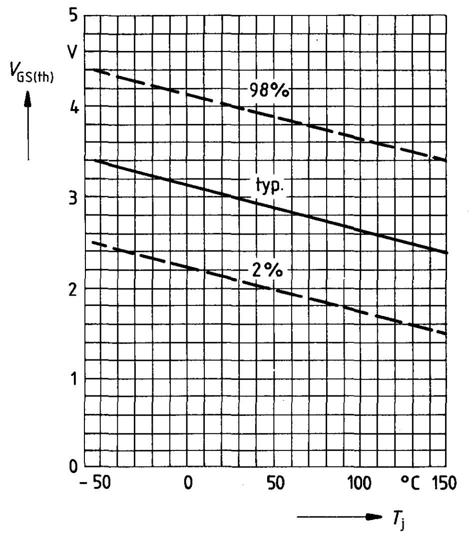
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 4{,}5A$, $V_{GS} = 10V$
(spread)



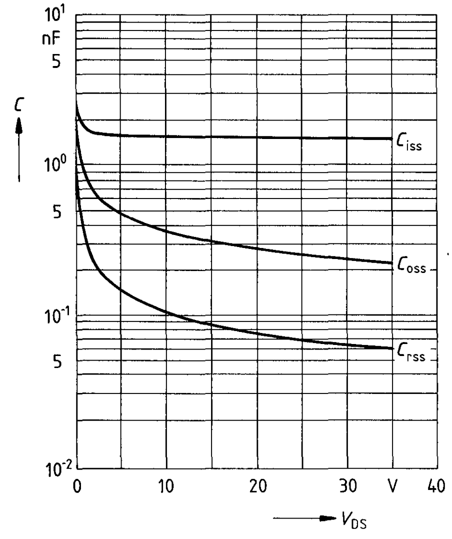
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



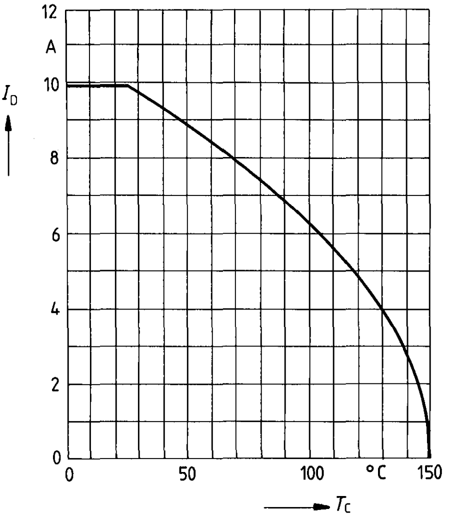
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



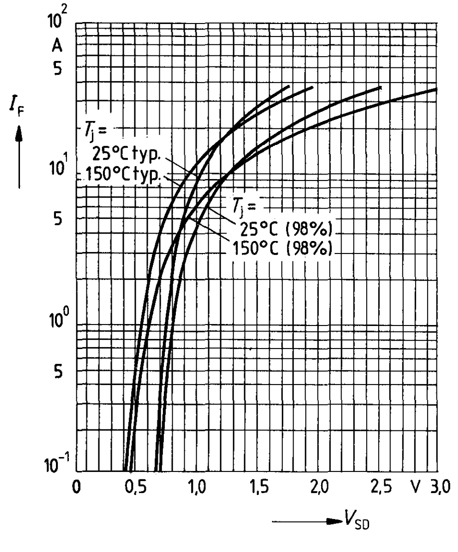
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



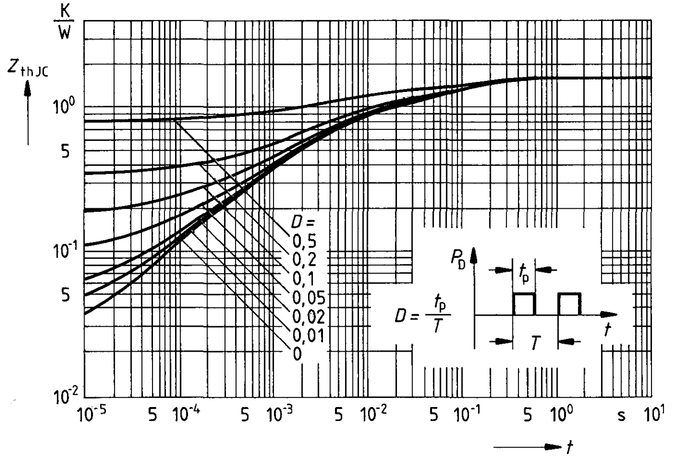
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



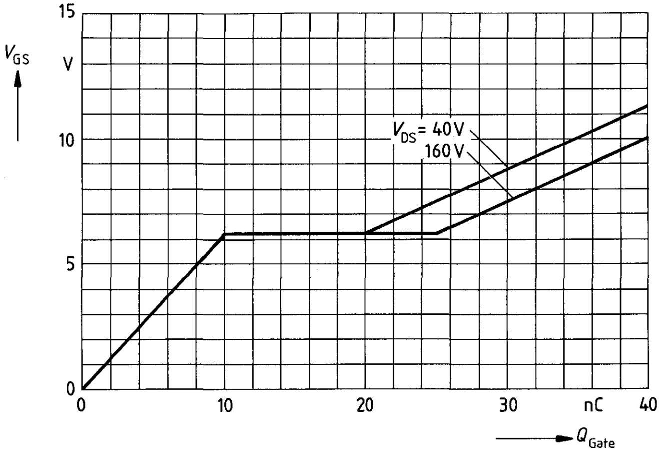
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



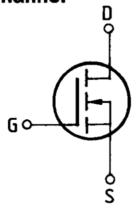
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14{,}3A$



Main ratings

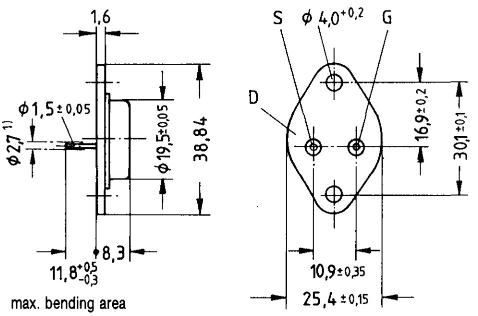
Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 22 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,12 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AE (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 36	C67078-A1018-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	22	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	85	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

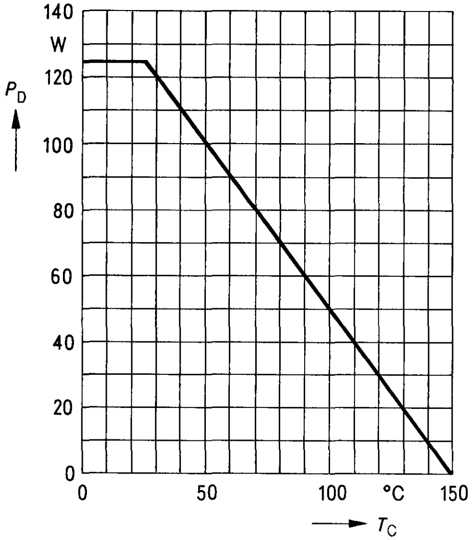
 S Preferred Type

Electrical characteristics

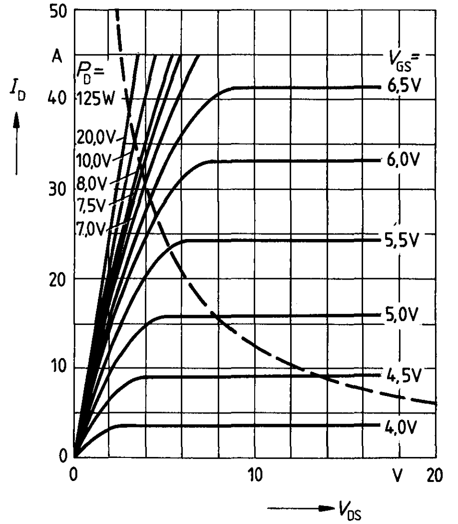
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,09	0,12	Ω	V_{GS} = 10V I_D = 11A
Dynamic ratings						
Forward transconductance	g_{fs}	9,0	13,0	–	S	V_{DS} = 25V I_D = 11A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	500	800		
Reverse transfer capacitance	C_{rss}	–	200	350		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	70	110		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	120	160		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	22	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	85		
Diode forward on-voltage	V_{SD}	–	1,2	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	400	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

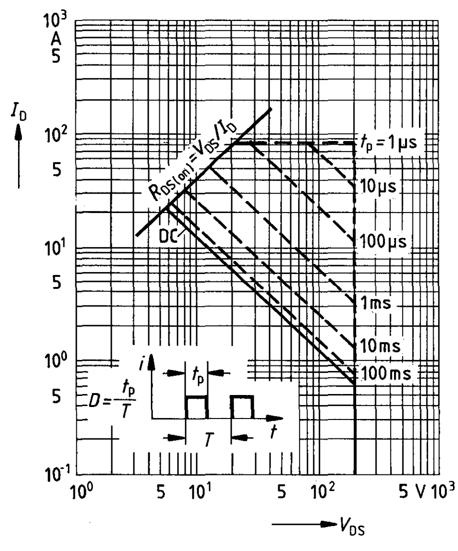
Power dissipation $P_D = f(T_C)$



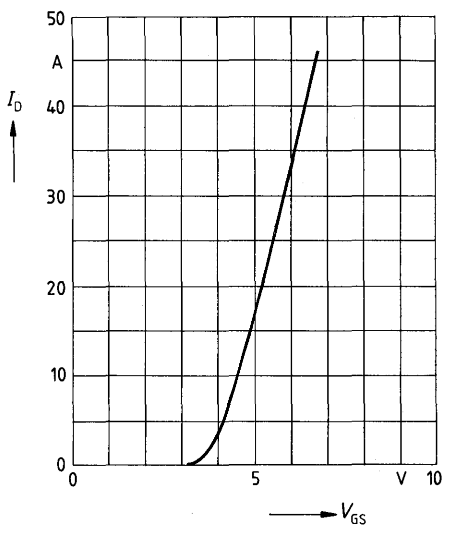
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



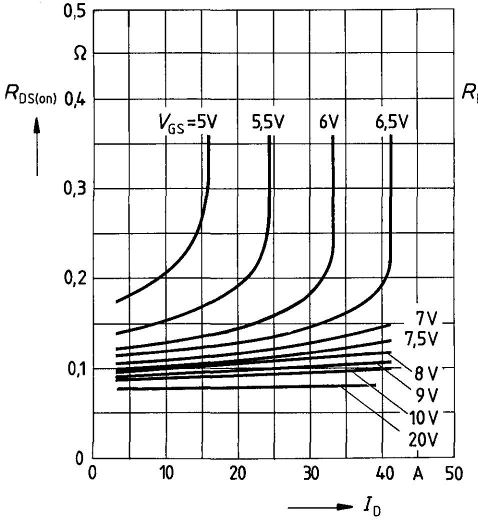
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



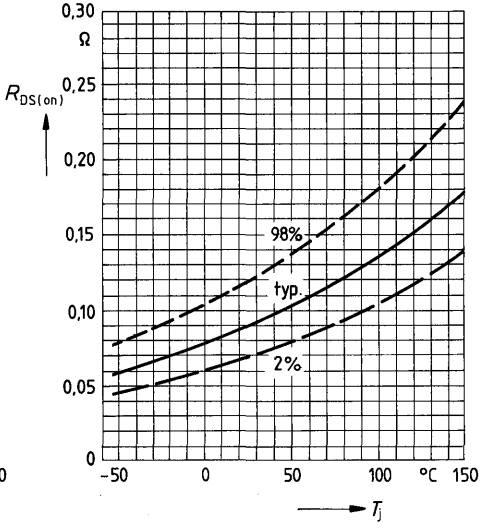
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\,V$, $T_j = 25\,°C$



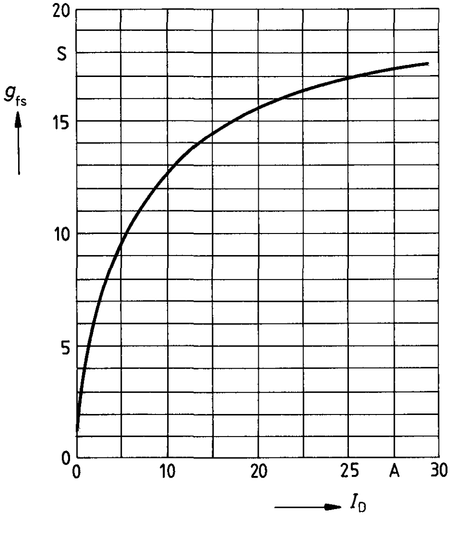
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



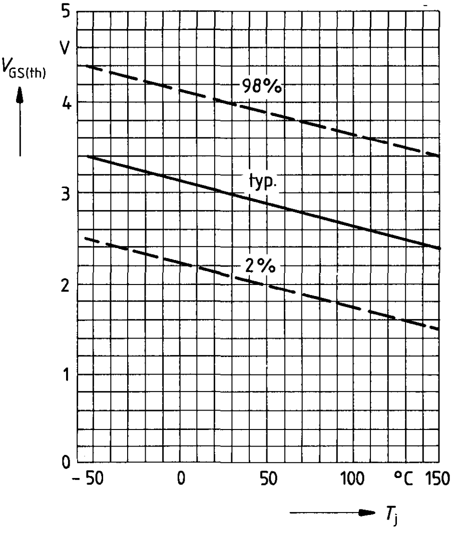
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 11A$, $V_{GS} = 10V$
(spread)



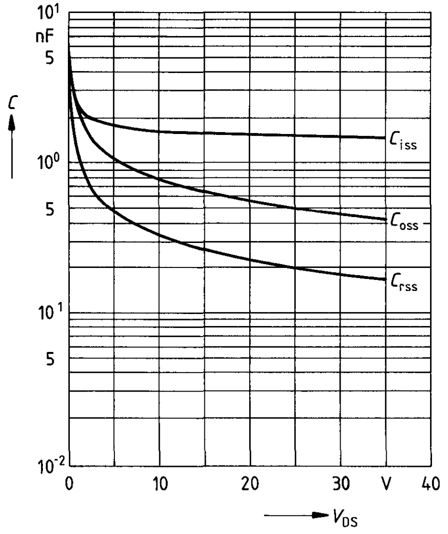
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



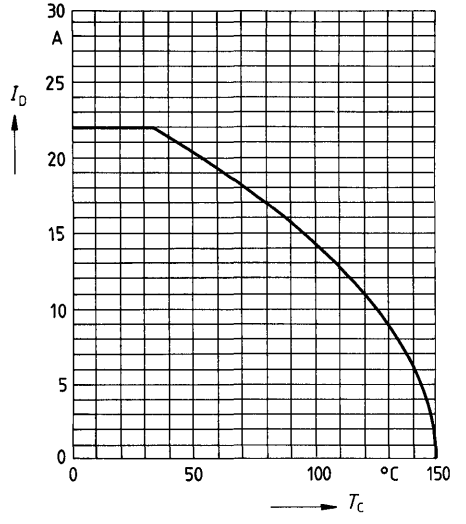
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



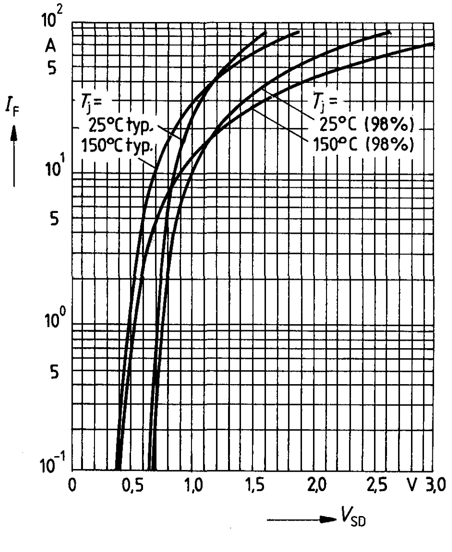
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



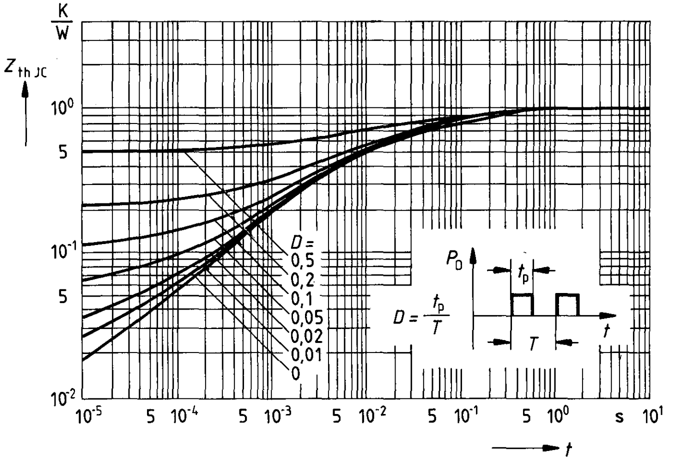
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



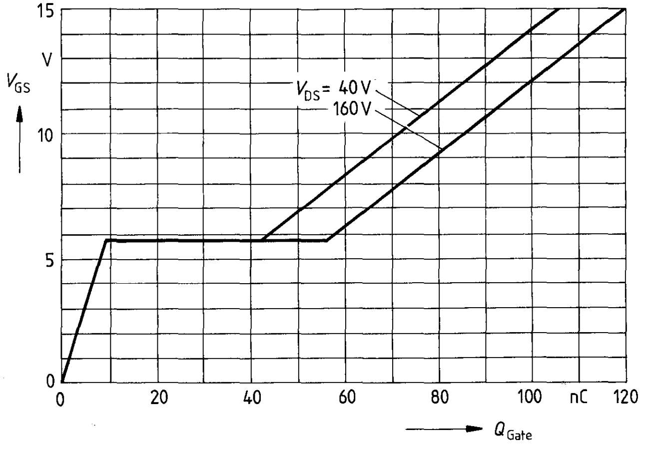
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



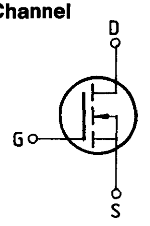
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 33A$



Main ratings

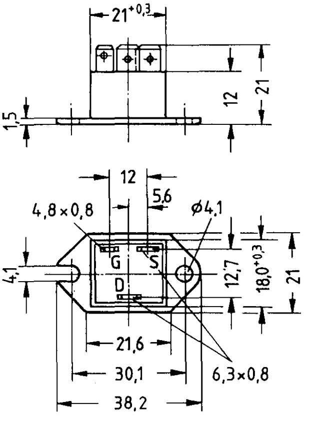
Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 13 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,2 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 37	C67078-A1603-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	13	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	52	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	70	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–40 … +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤1,78	K/W	

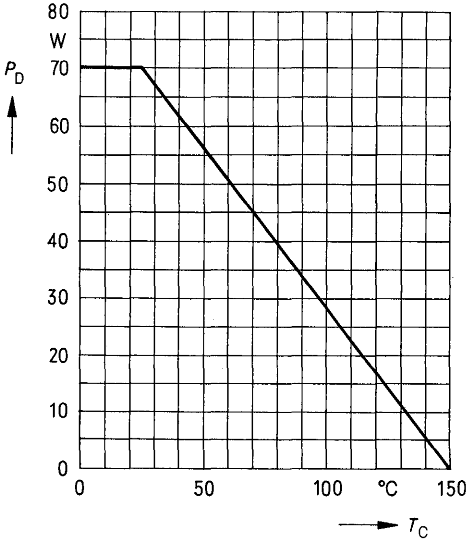
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

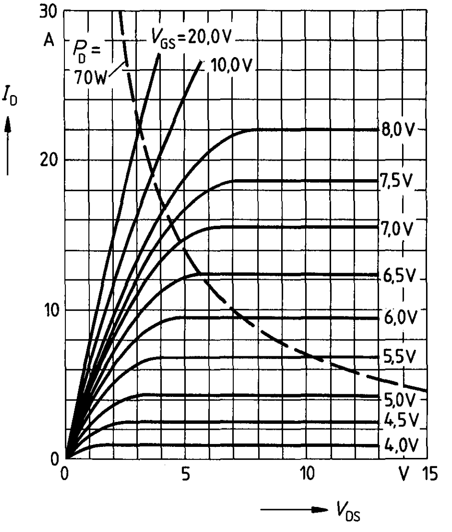
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,17	0,2	Ω	V_{GS} = 10V I_D = 7A
Dynamic ratings						
Forward transconductance	g_{fs}	3,0	5,0	–	S	V_{DS} = 25V I_D = 7A
Input capacitance	C_{iss}	–	900	1400	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	300	500		
Reverse transfer capacitance	C_{rss}	–	140	250		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	170	220		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	13	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	52		
Diode forward on-voltage	V_{SD}	–	1,4	1,8	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	400	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

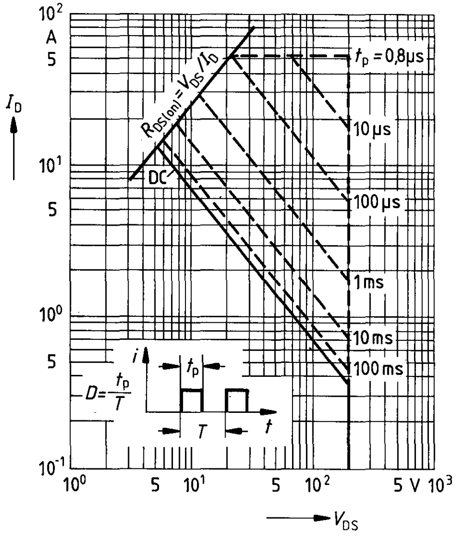
Power dissipation $P_D = f(T_C)$



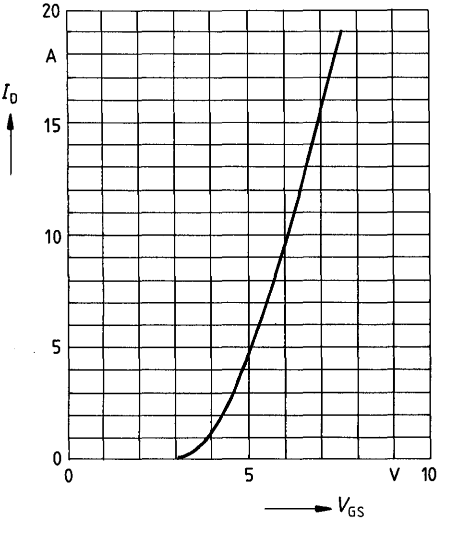
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



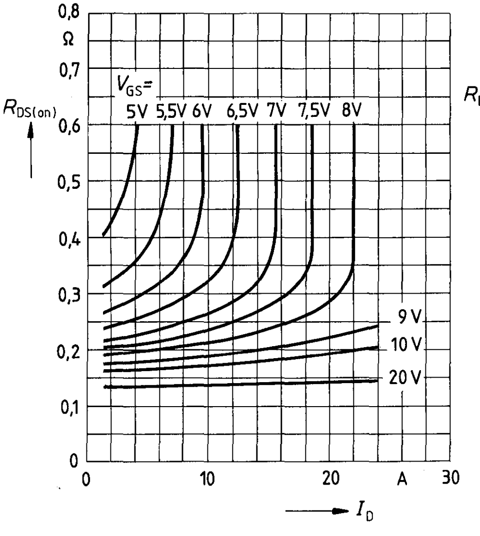
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



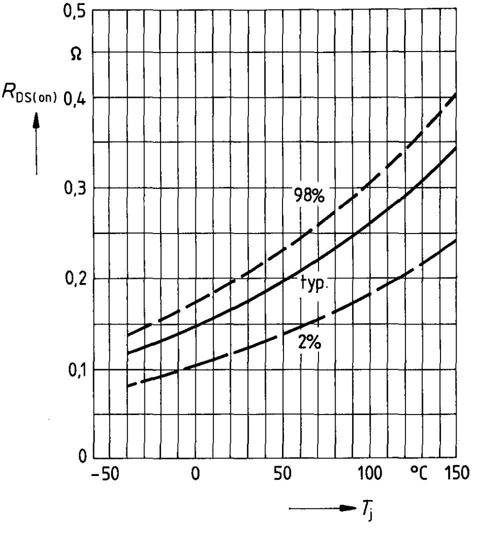
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



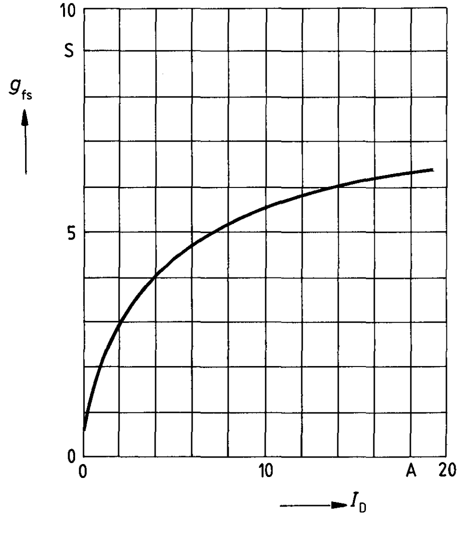
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



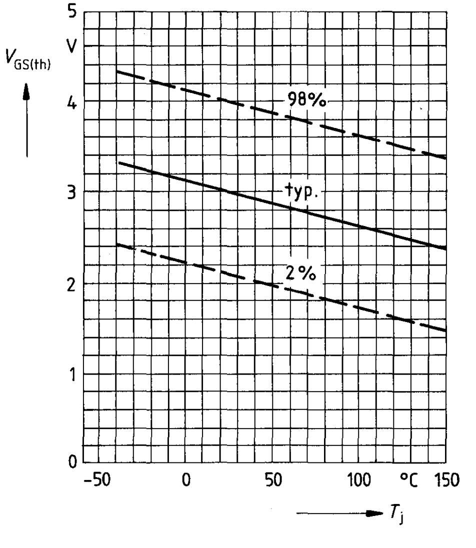
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 11A$, $V_{GS} = 10V$
(spread)



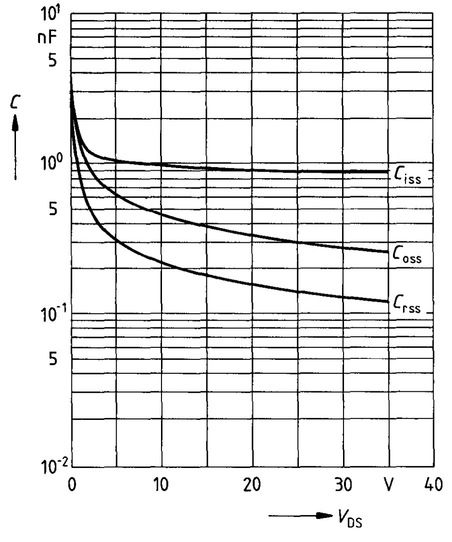
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



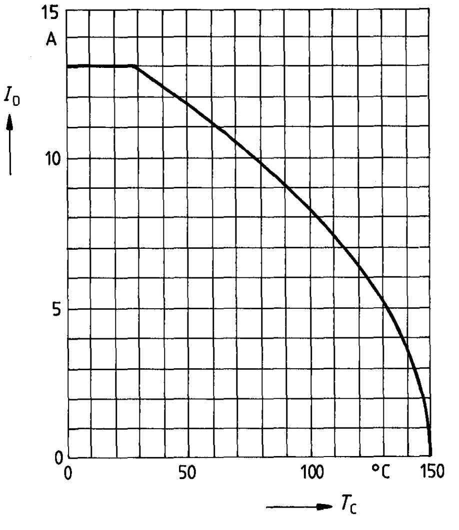
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



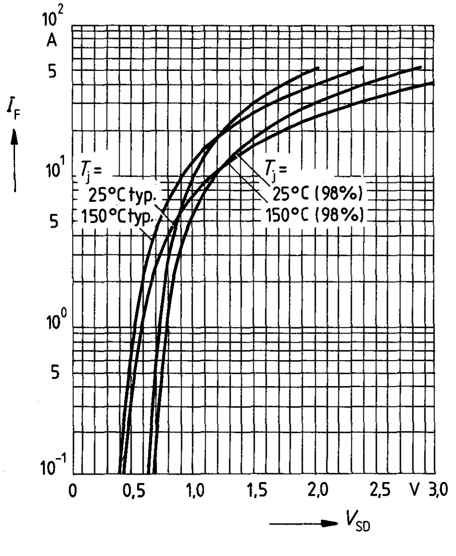
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



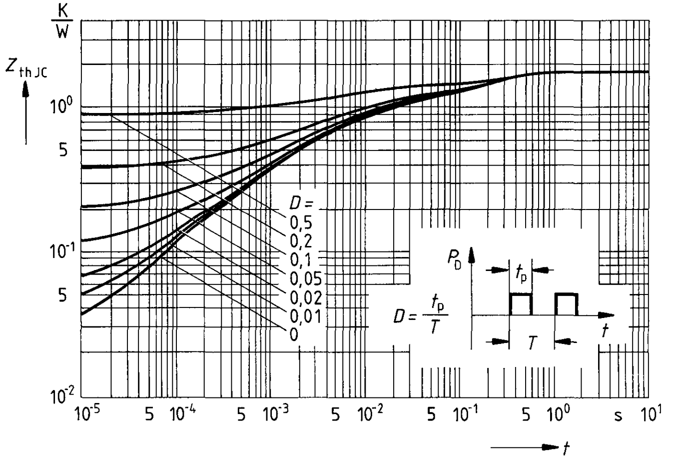
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



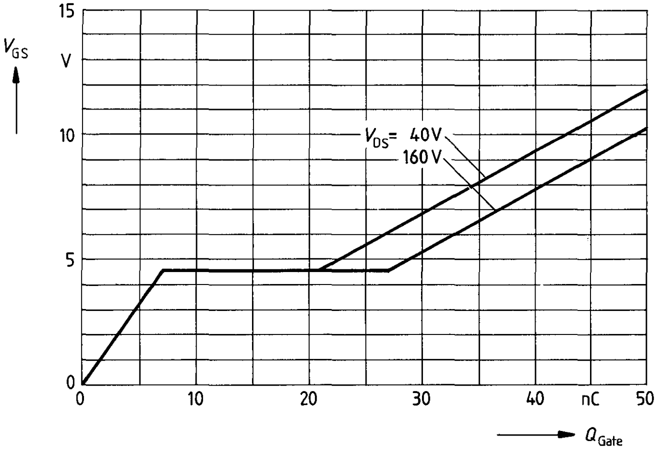
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

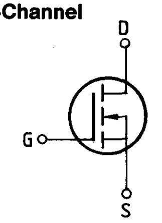


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 18{,}8A$



Main ratings

N-Channel

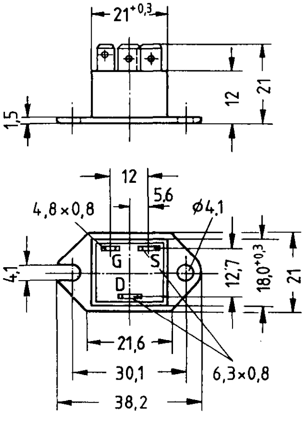


Drain-source voltage	V_{DS}	**= 200 V**
Continuous drain current	I_D	**= 18 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,12 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
S BUZ 38	C67078-A1611-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	18	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	70	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage	T_j			
temperature range	T_{stg}	−40 … +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,5	K/W	

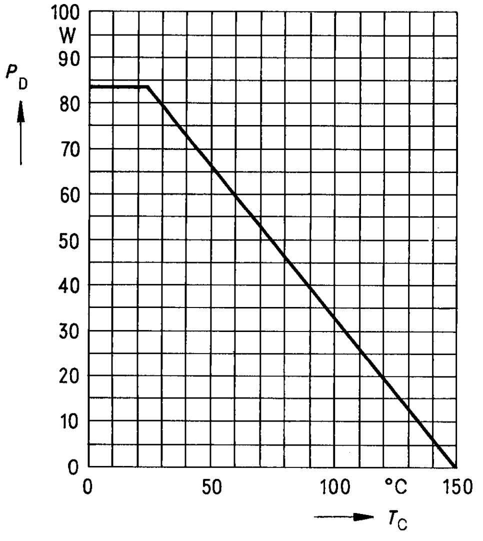
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

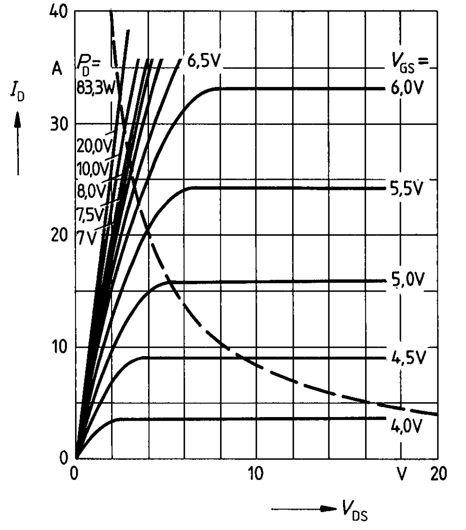
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,09	0,12	Ω	V_{GS} = 10V I_D = 11A
Dynamic ratings						
Forward transconductance	g_{fs}	9,0	13,0	–	S	V_{DS} = 25V I_D = 11A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	500	800		
Reverse transfer capacitance	C_{rss}	–	200	350		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	70	110		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	120	160		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	18	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	70		
Diode forward on-voltage	V_{SD}	–	1,15	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	400	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

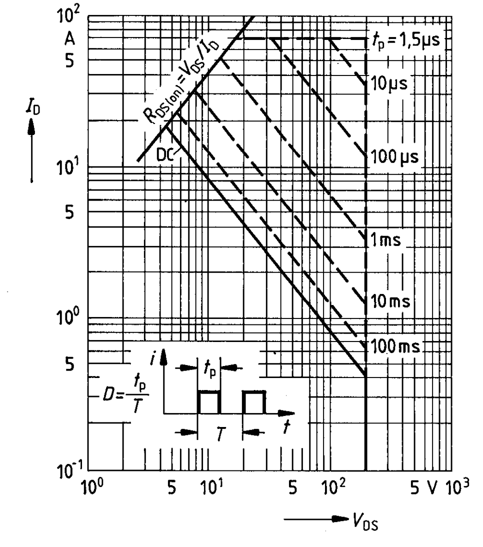
Power dissipation $P_D = f(T_C)$



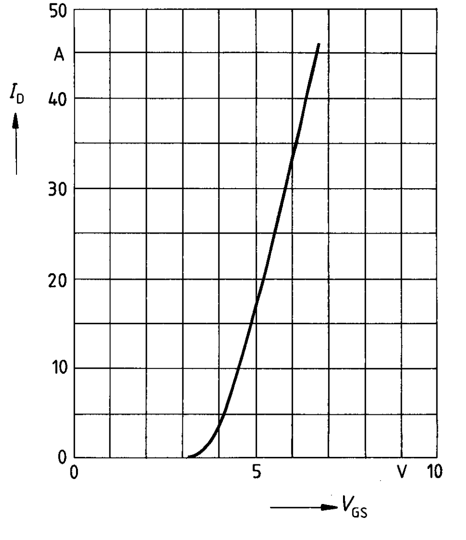
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



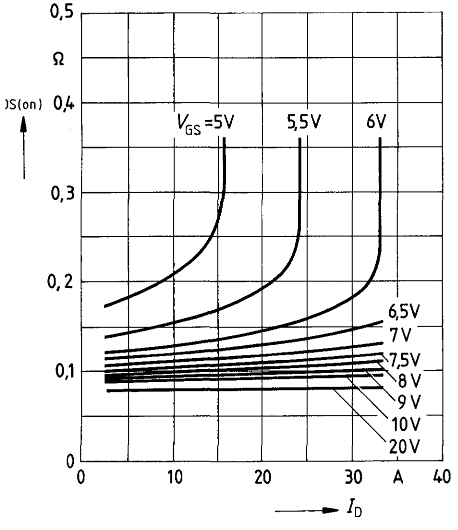
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



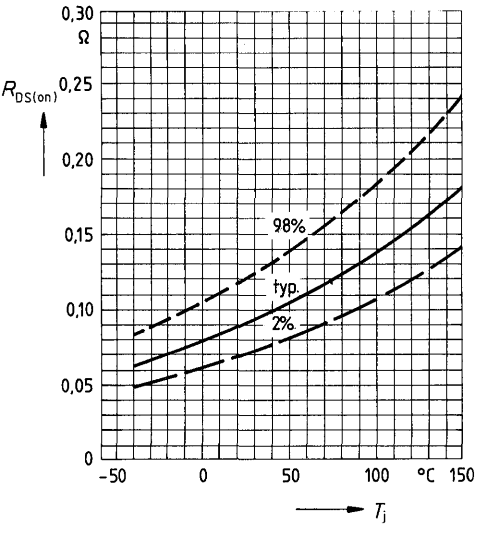
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



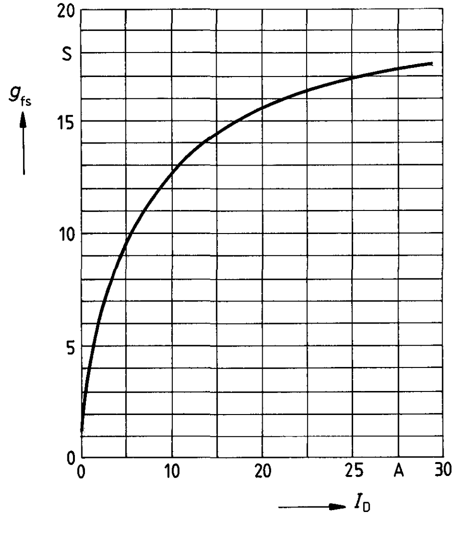
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



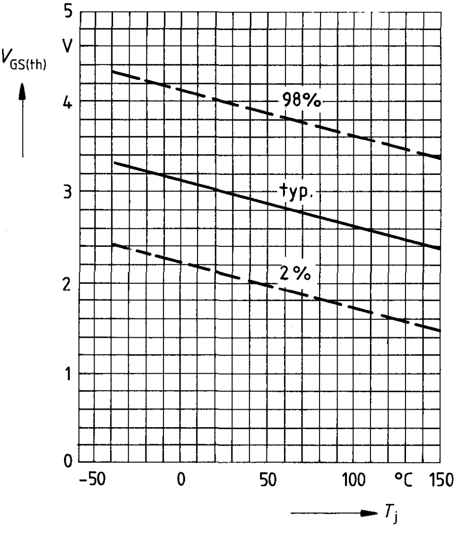
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 11A, V_{GS} = 10V
(spread)



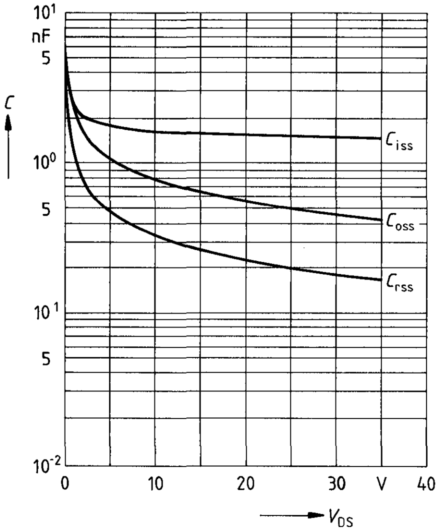
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



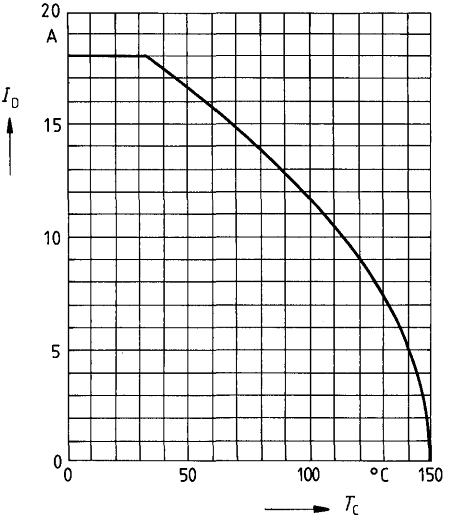
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



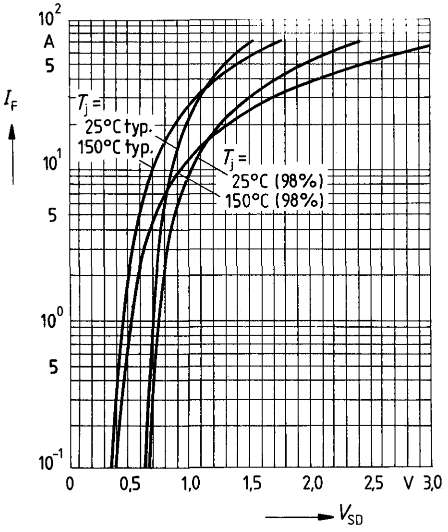
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



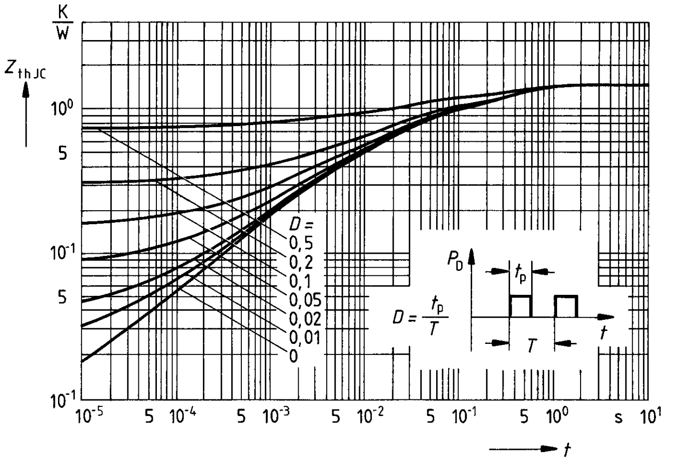
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



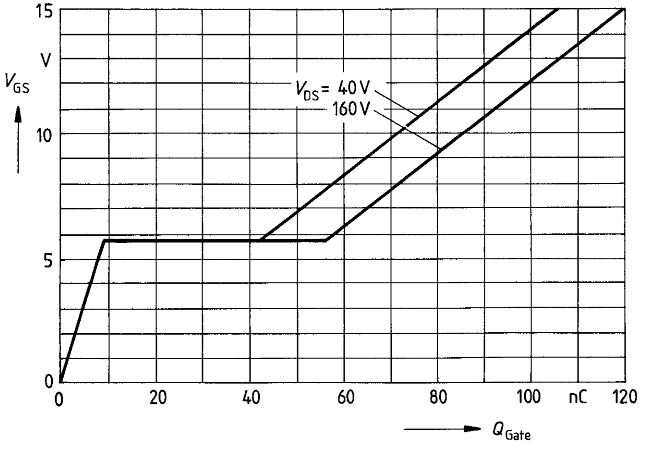
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

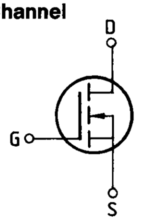


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 33A$



Main ratings

N-Channel

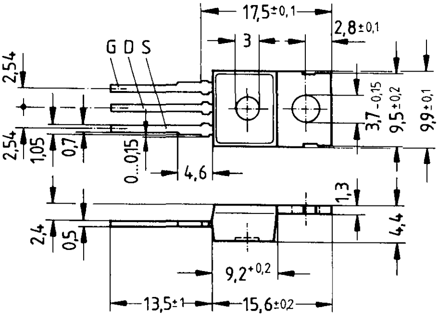


Drain-source voltage	V_{DS}	**= 500 V**
Continuous drain current	I_D	**= 4,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 1,5 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 41 A	C67078-A1306-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,5	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	18	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

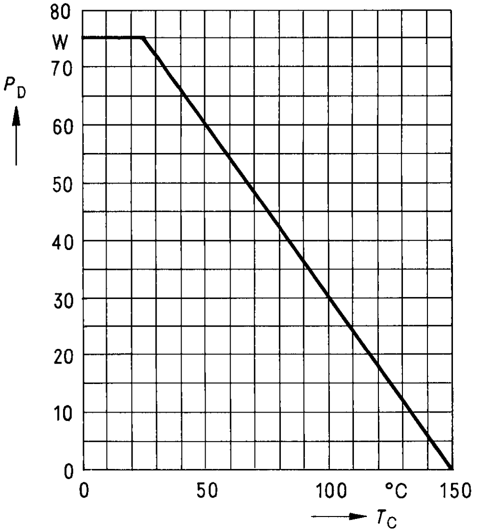
S Preferred Type

Electrical characteristics

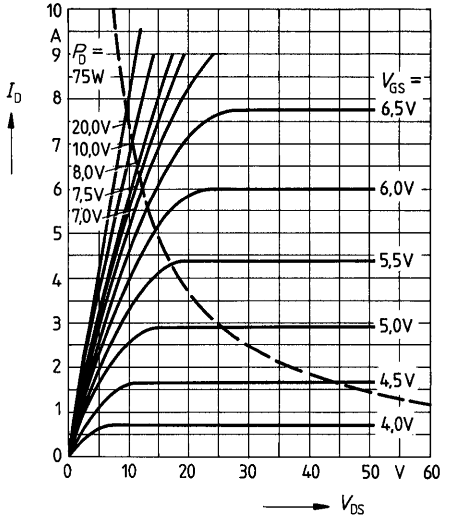
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,4	1,5	Ω	V_{GS} = 10V I_D = 2,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	110	170		
Reverse transfer capacitance	C_{rss}	–	40	70		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	18		
Diode forward on-voltage	V_{SD}	–	1,1	1,5	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

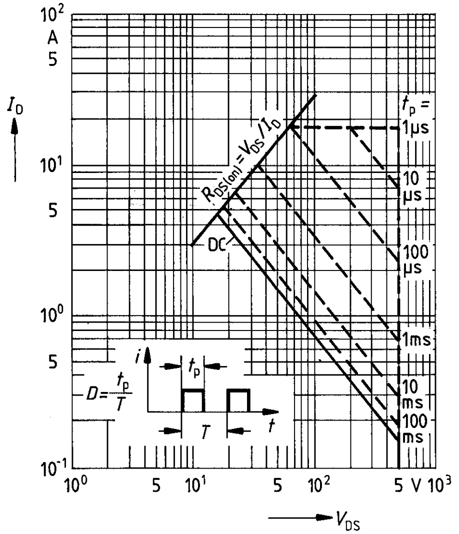
Power dissipation $P_D = f(T_C)$



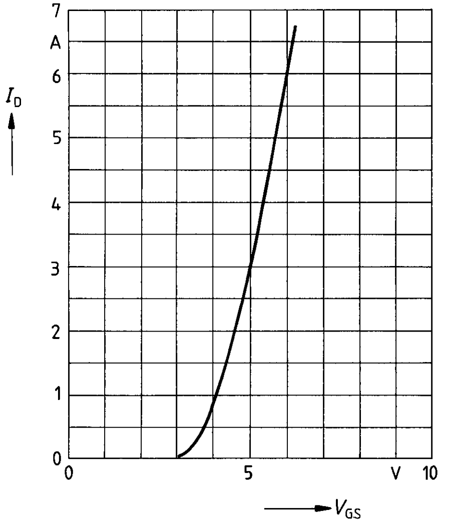
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



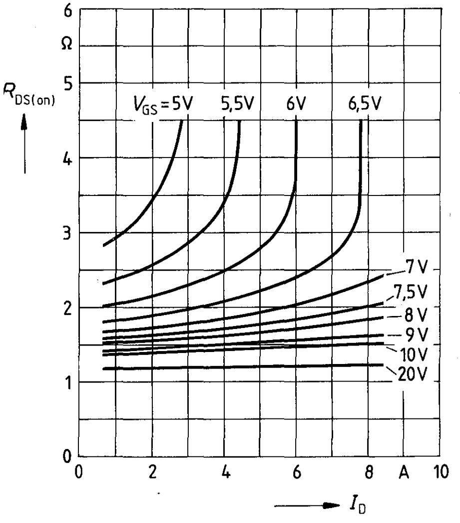
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



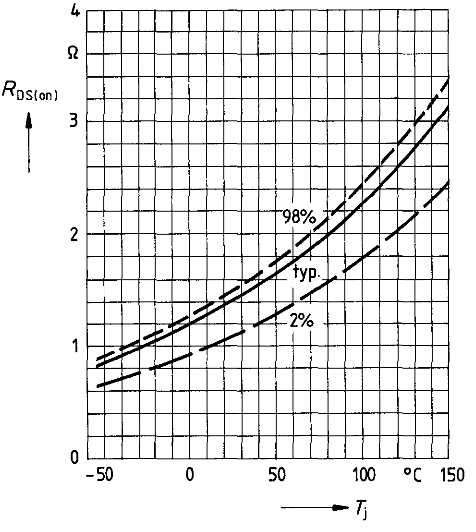
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



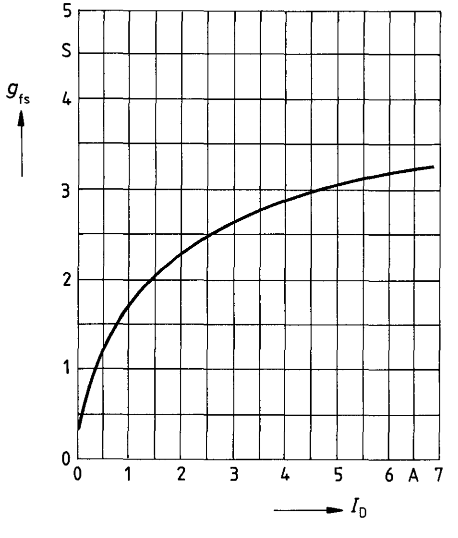
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



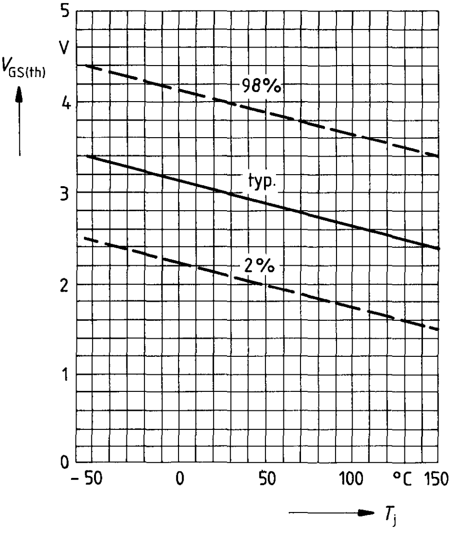
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 2,5A, V_{GS} = 10V
(spread)



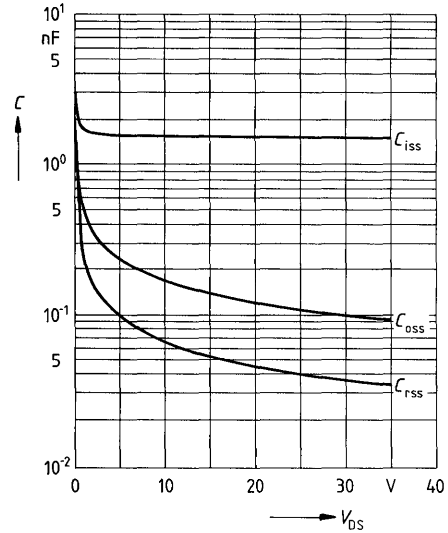
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



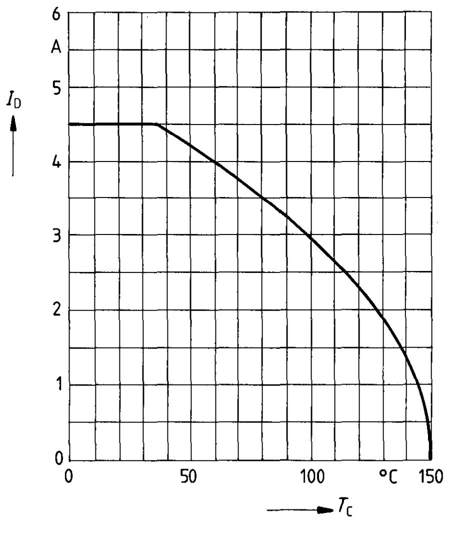
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



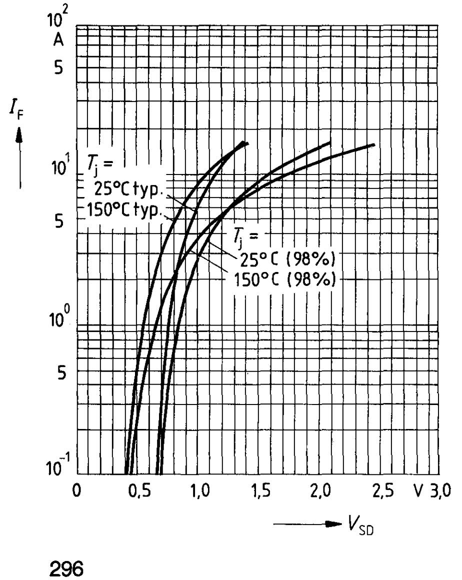
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



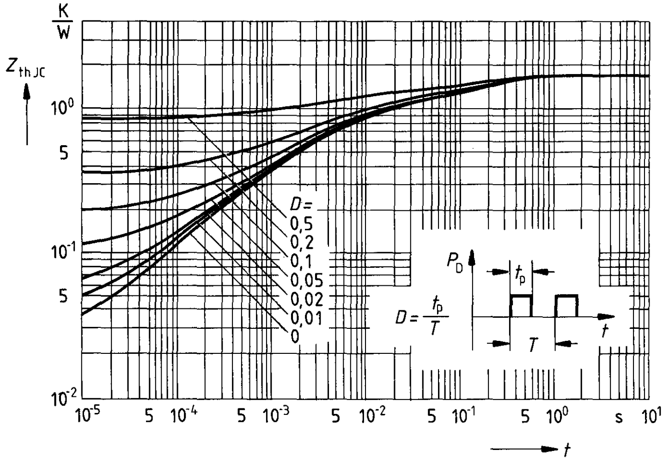
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



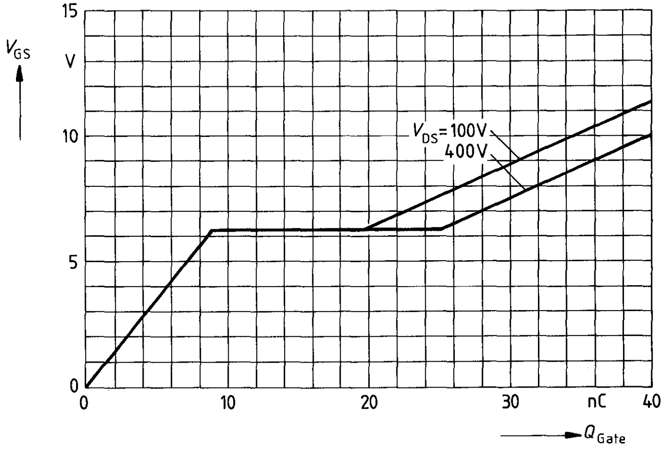
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



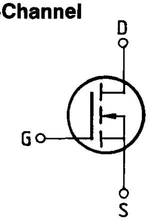
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 6{,}8A$



Main ratings

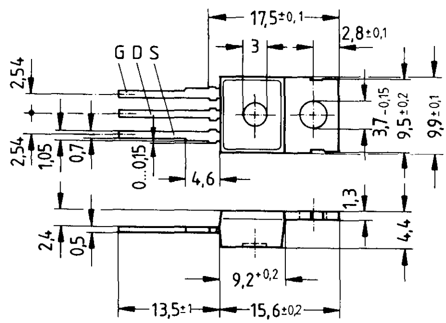
Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 4,0 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 42	C67078-A1311-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,0	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	16	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

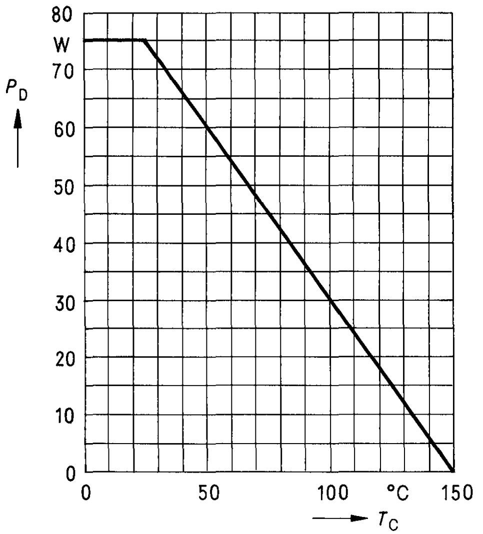
 S Preferred Type

Electrical characteristics

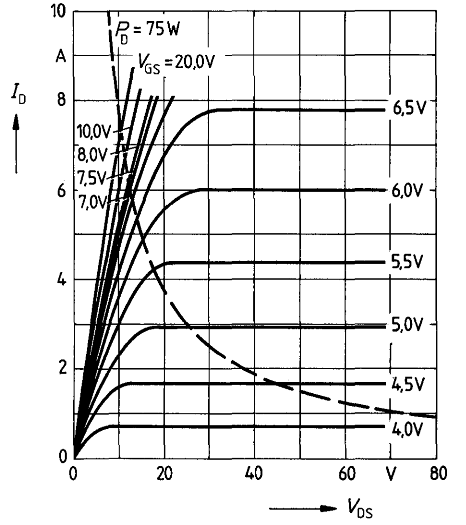
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	1,6	2,0	Ω	V_{GS} = 10V I_D = 2,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	110	170		
Reverse transfer capacitance	C_{rss}	–	40	70		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	110	140		
	t_f	–	50	65		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	16		
Diode forward on-voltage	V_{SD}	–	1,1	1,5	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

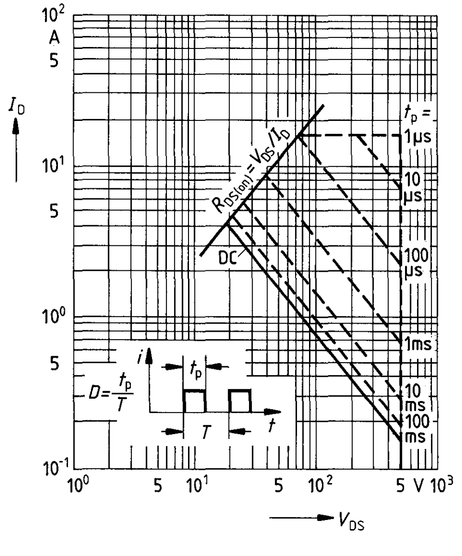
Power dissipation $P_D = f(T_C)$



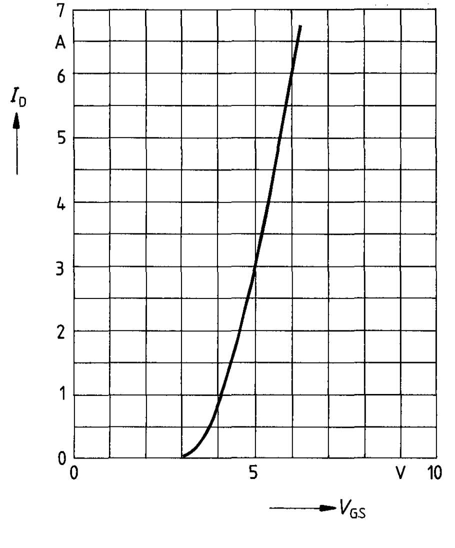
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



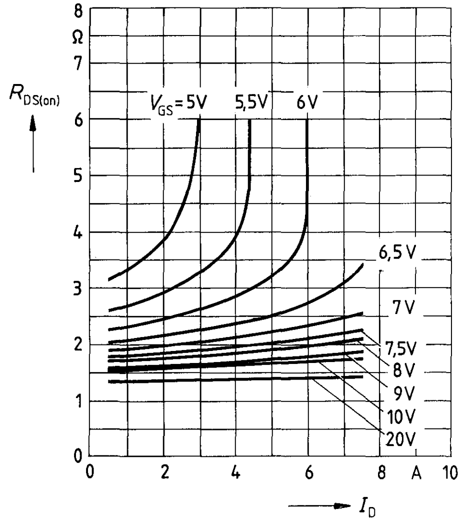
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



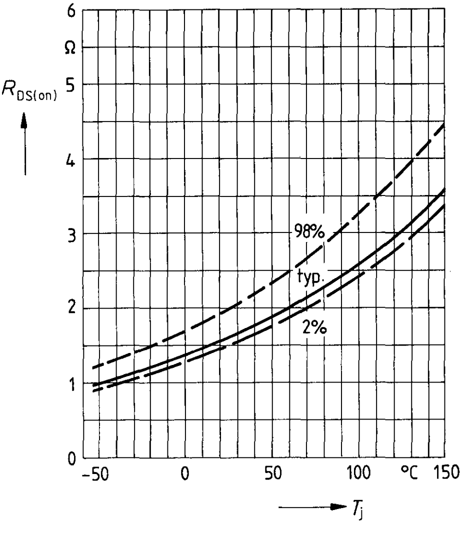
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



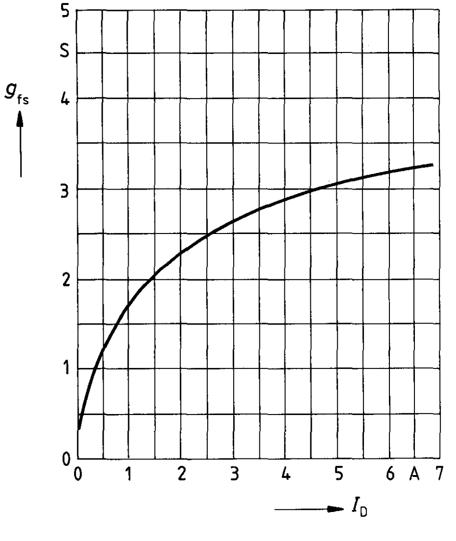
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



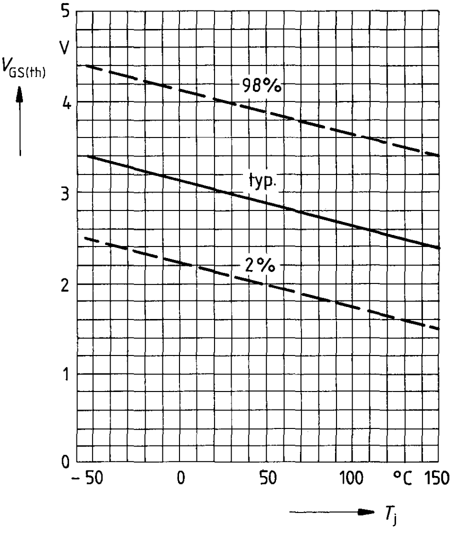
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 2{,}5A$, $V_{GS} = 10V$
(spread)



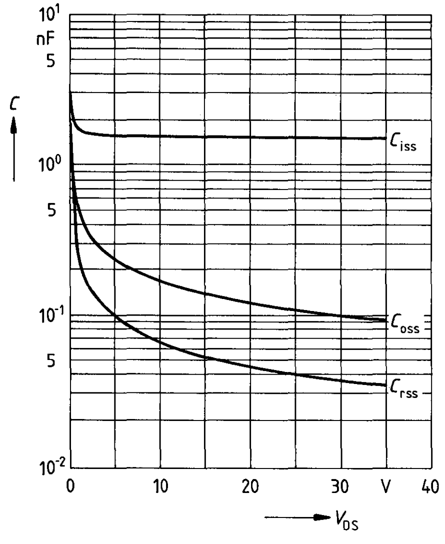
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



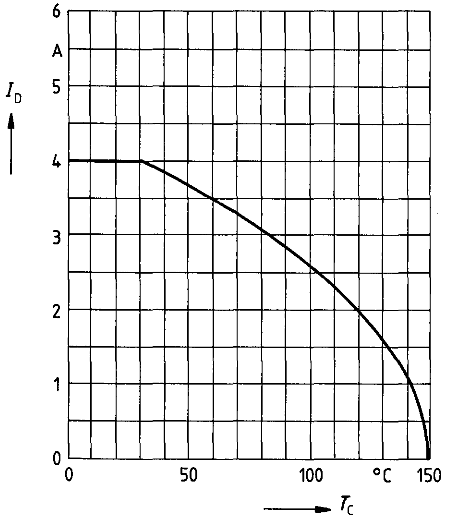
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



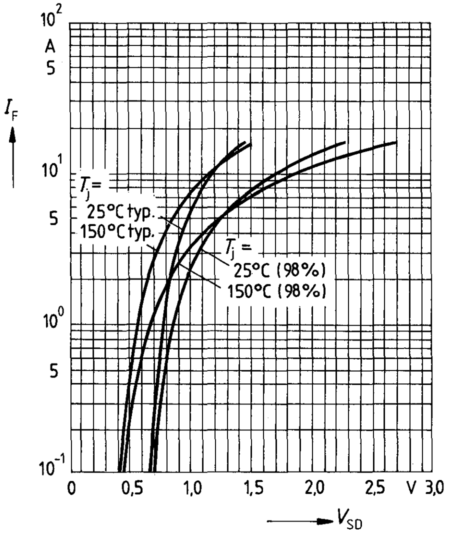
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



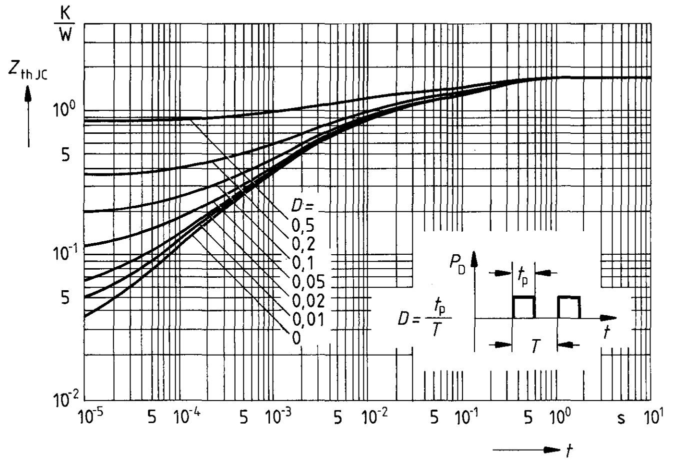
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



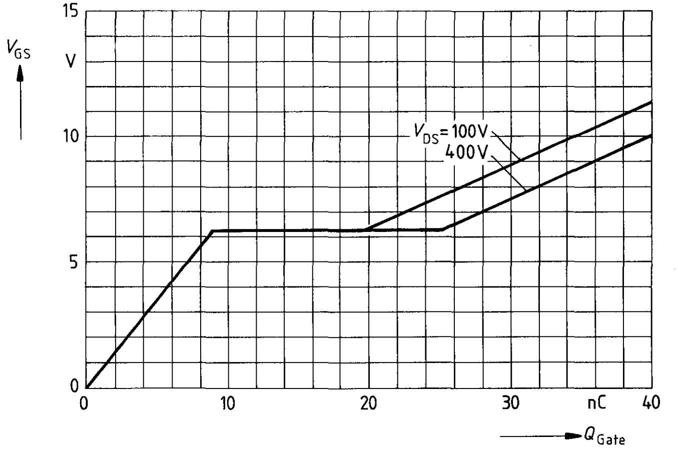
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



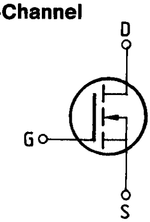
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 6{,}8A$



Main ratings

Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 4,8 A**
Drain-source on-resistance $R_{DS(on)}$ **= 1,5 Ω**

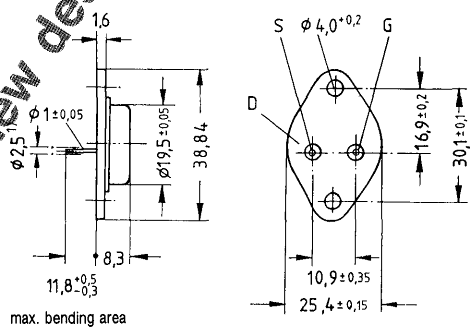
N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 44 A	C67078-A1007-A3

Not for new design



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,8	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	19	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,6	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

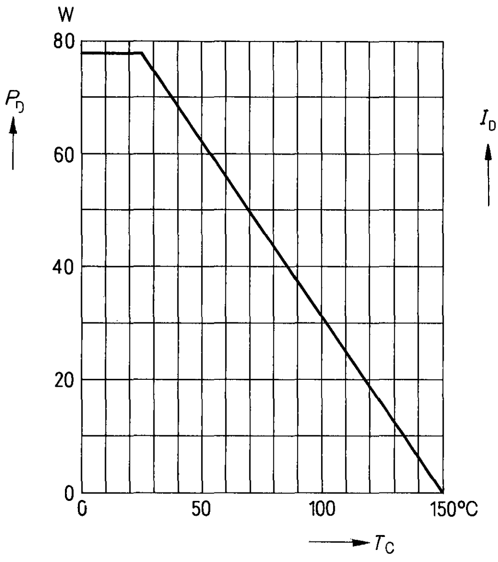
 S Preferred Type

Electrical characteristics

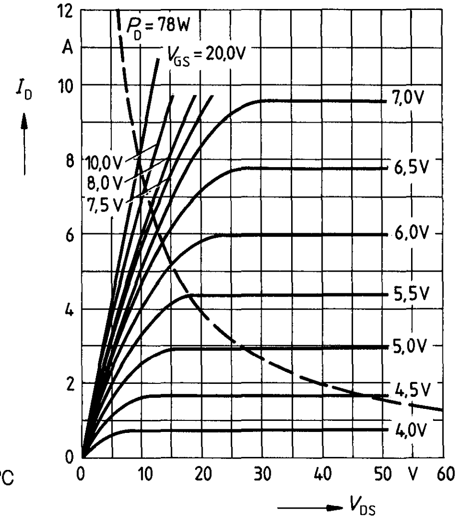
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,4	1,5	Ω	V_{GS} = 10V I_D = 2,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1500	2000	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	110	170		
Reverse transfer capacitance	C_{rss}	–	40	70		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,8	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	19		
Diode forward on-voltage	V_{SD}	–	1,15	1,5	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{IF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6,0	–	µC	

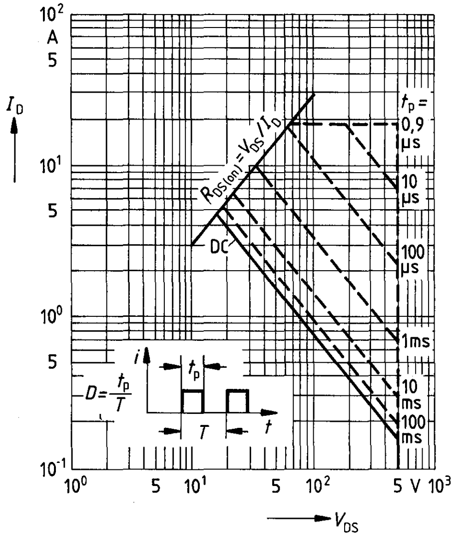
Power dissipation $P_D = f(T_C)$



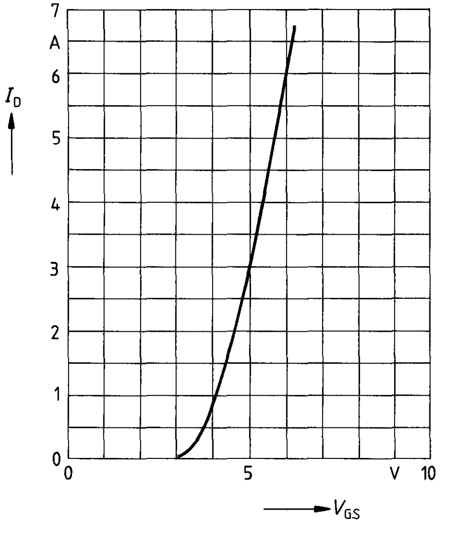
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



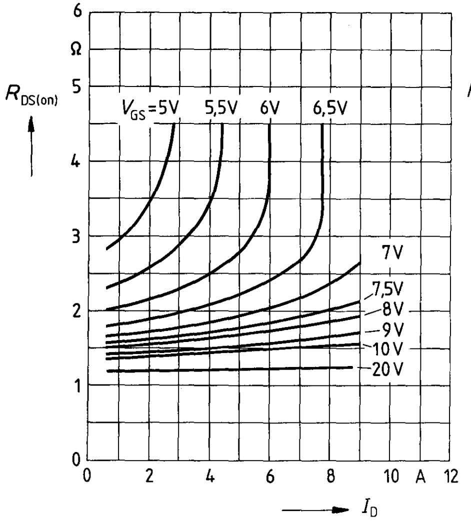
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



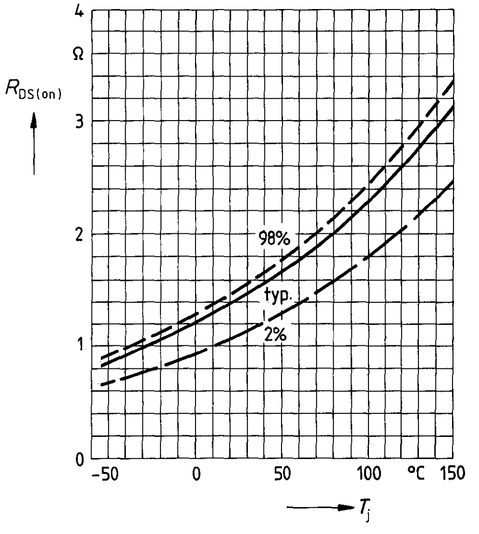
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



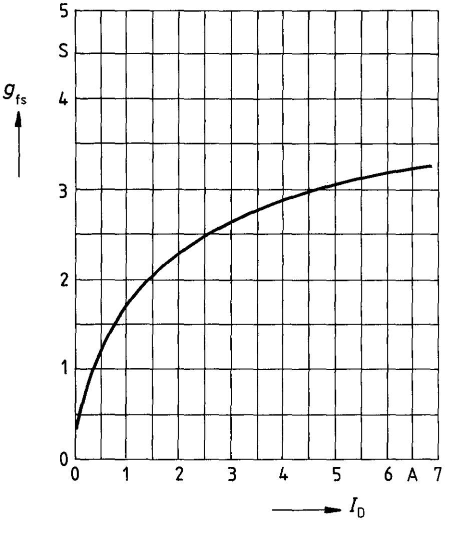
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



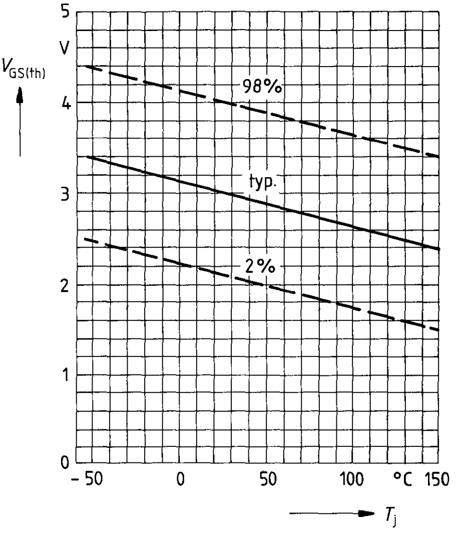
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 2{,}5A$, $V_{GS} = 10V$
(spread)



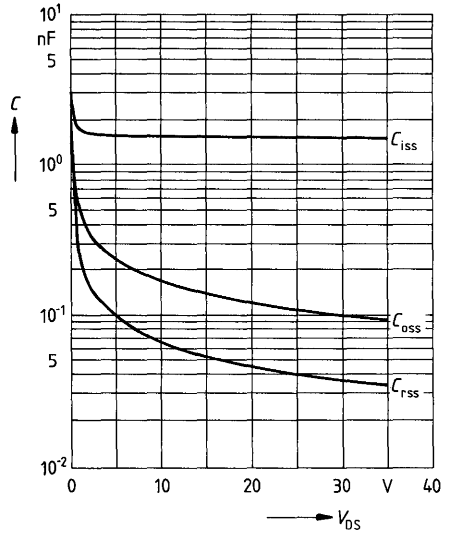
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



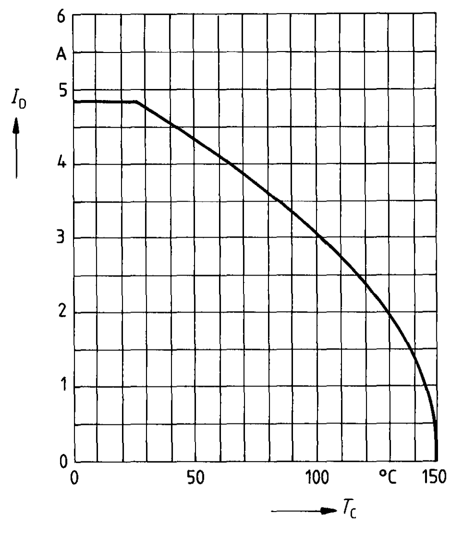
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



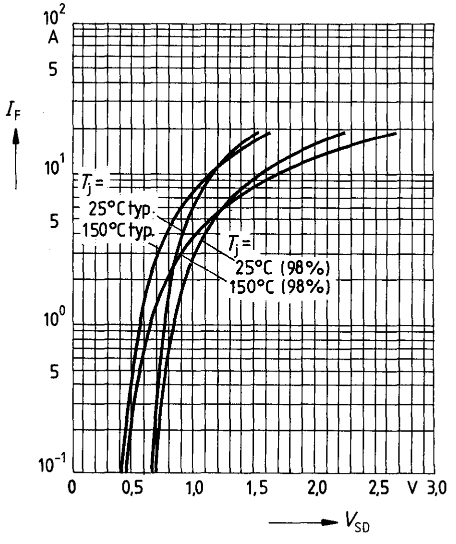
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1 MHz$



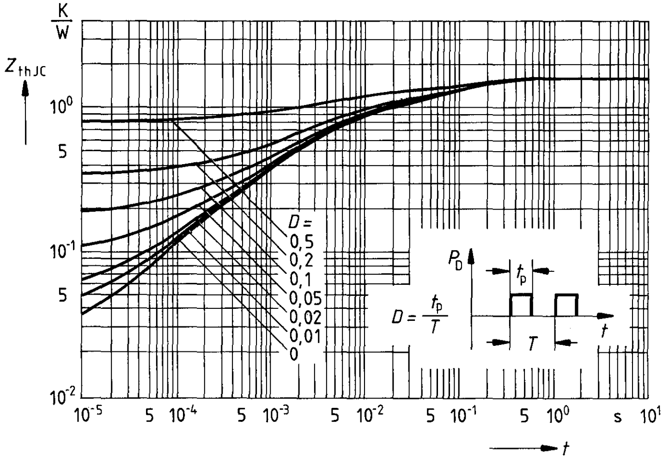
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



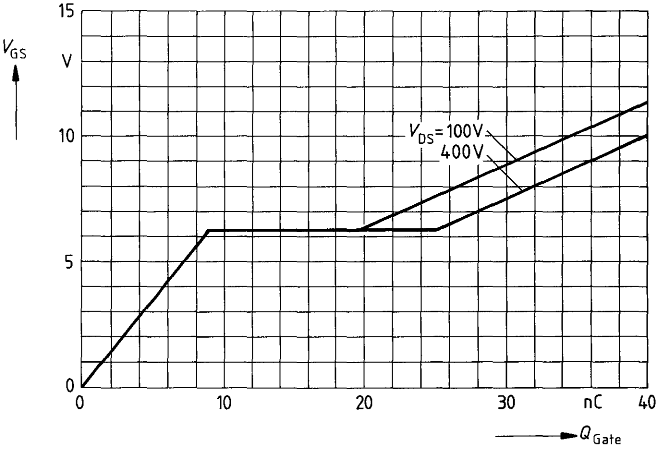
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



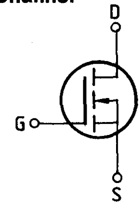
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 6{,}8A$



Main ratings

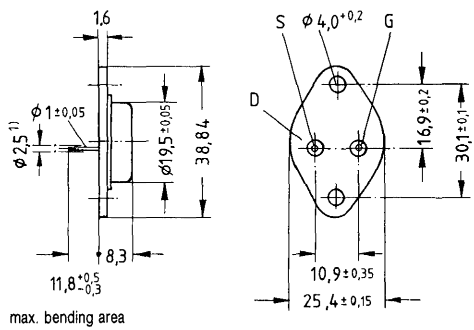
Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 9,6 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,6 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3A2 in accordance with DIN 41872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 45	C67078-A1008-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	9,6	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	38	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

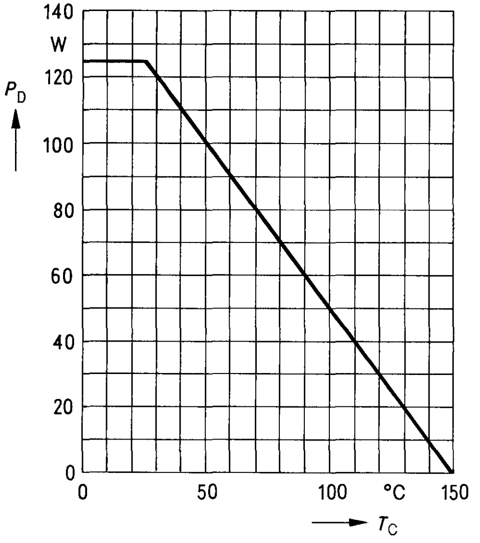
 S Preferred Type

Electrical characteristics

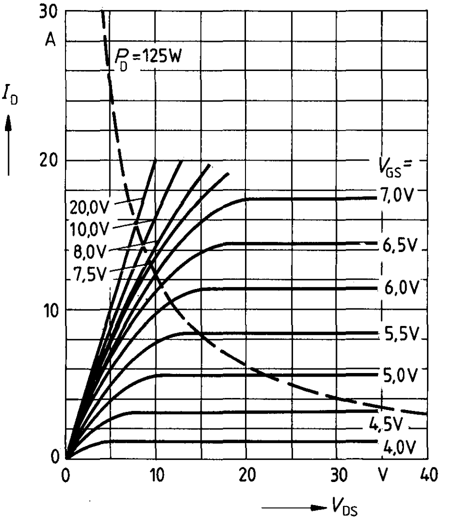
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,55	0,6	Ω	V_{GS} = 10V I_D = 5,0A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	5,0	–	S	V_{DS} = 25V I_D = 5,0A
Input capacitance	C_{iss}	–	3800	4900	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400		
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	9,6	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	38		
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

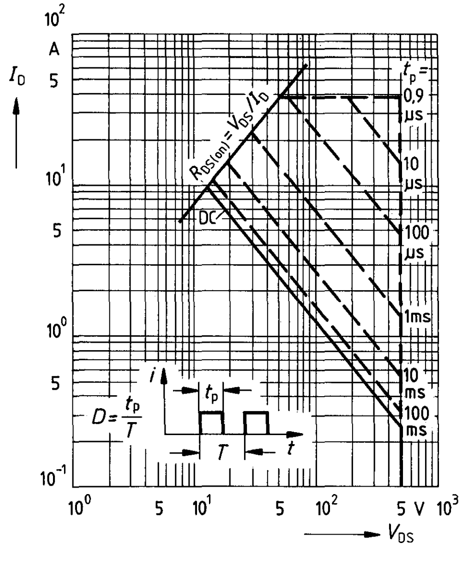
Power dissipation $P_D = f(T_C)$



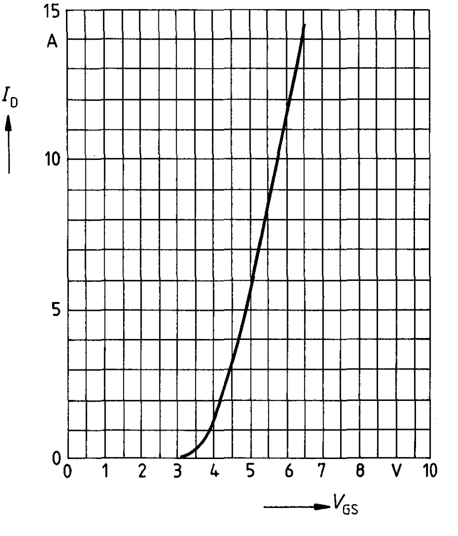
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



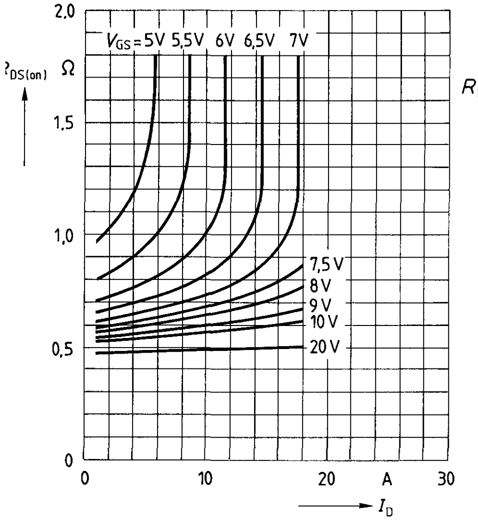
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



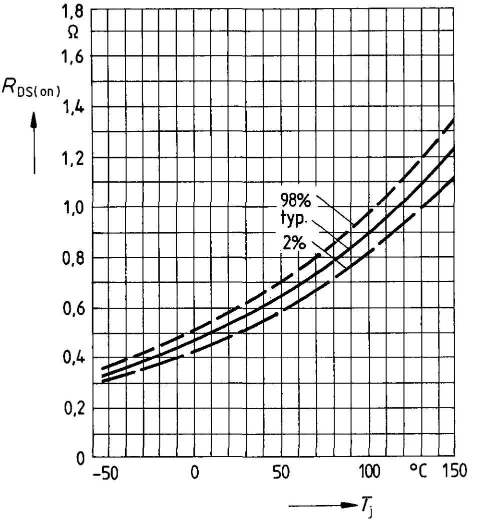
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



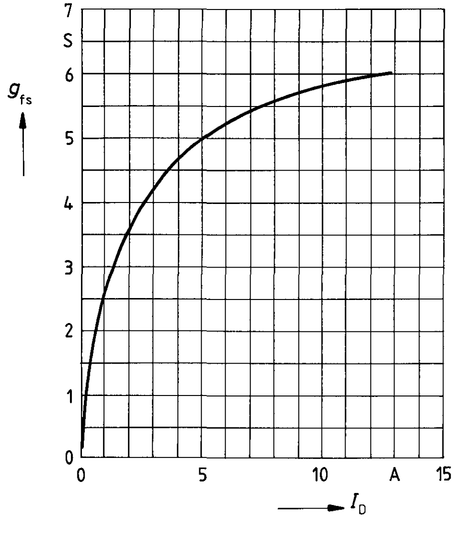
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



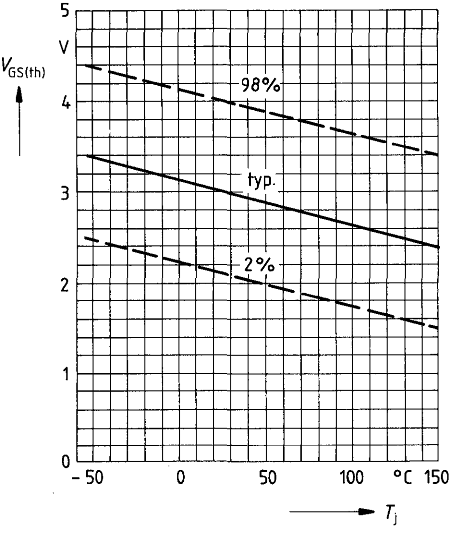
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 5A$, $V_{GS} = 10V$
(spread)



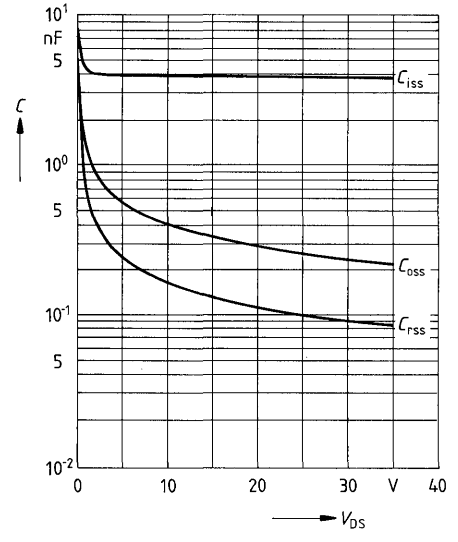
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



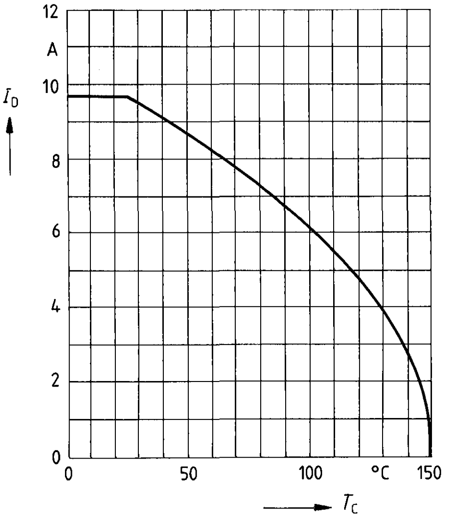
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



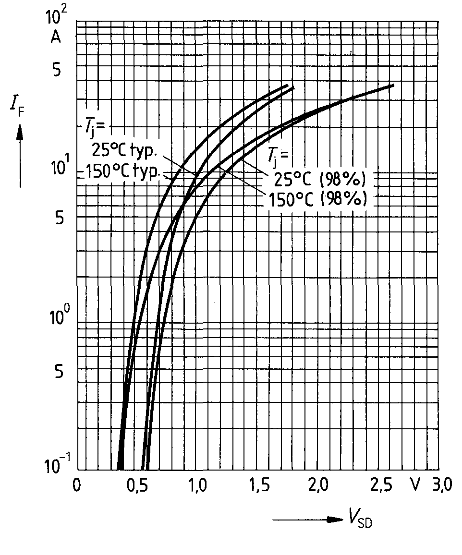
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



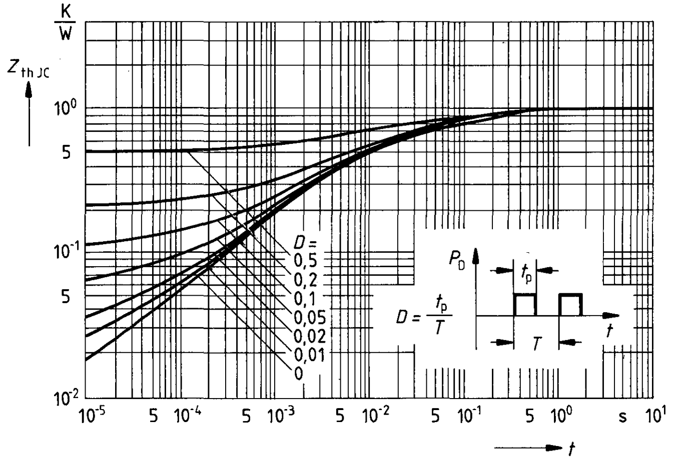
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



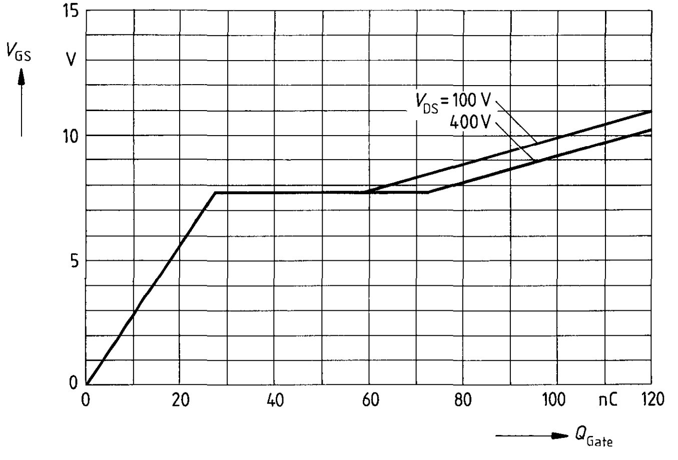
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



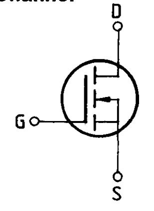
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14{,}4A$



Main ratings

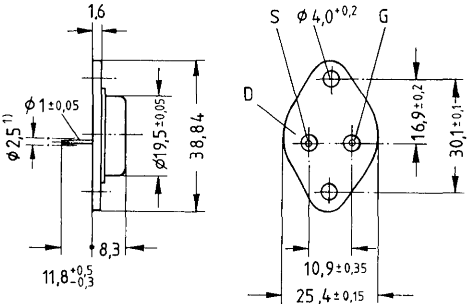
Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 8,3 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,8 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 45 A	C67078-A1008-A3



1) max. bending area

Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	8,3	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	33	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

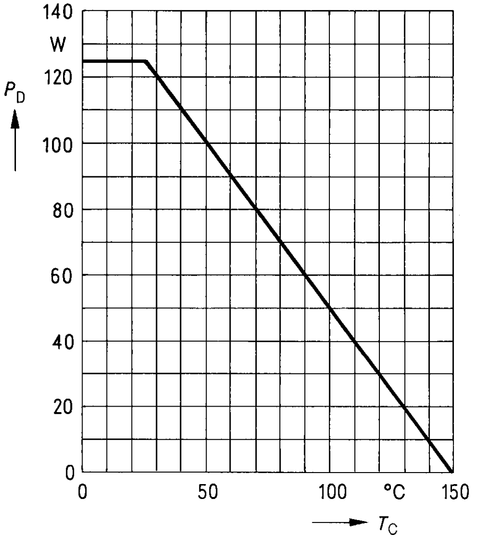
 S Preferred Type

Electrical characteristics

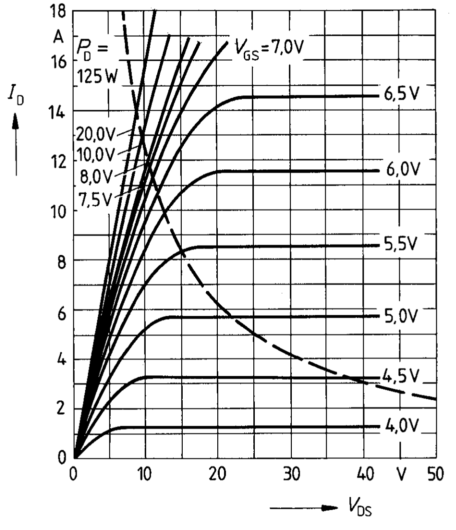
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	0,7	0,8	Ω	V_{GS} = 10V I_D = 5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	5,0	–	S	V_{DS} = 25V I_D = 5A
Input capacitance	C_{iss}	–	3800	4900	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400		
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	8,3	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	33		
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

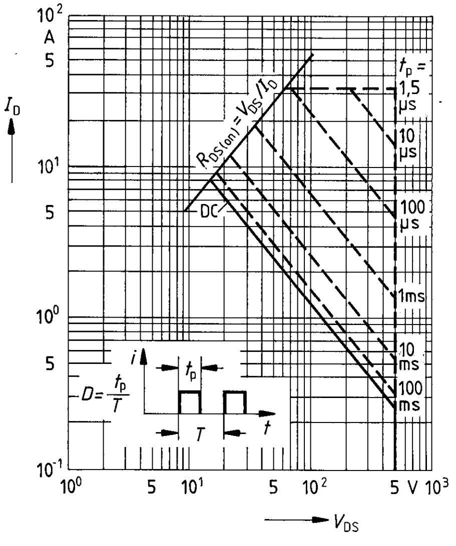
Power dissipation $P_D = f(T_C)$



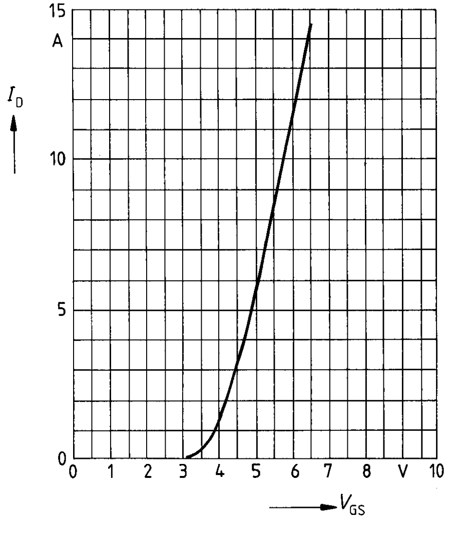
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



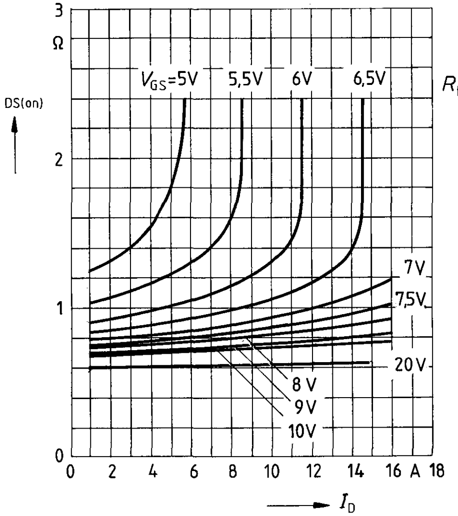
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



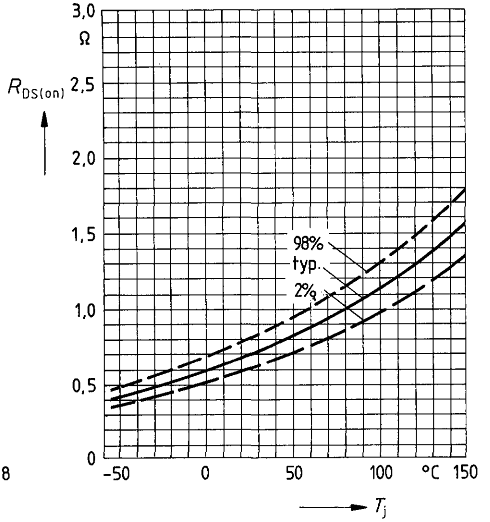
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



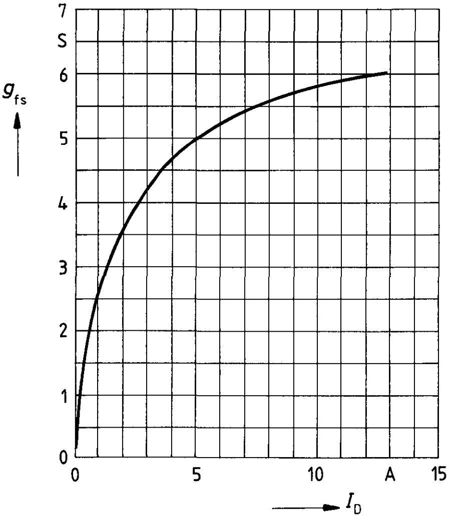
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



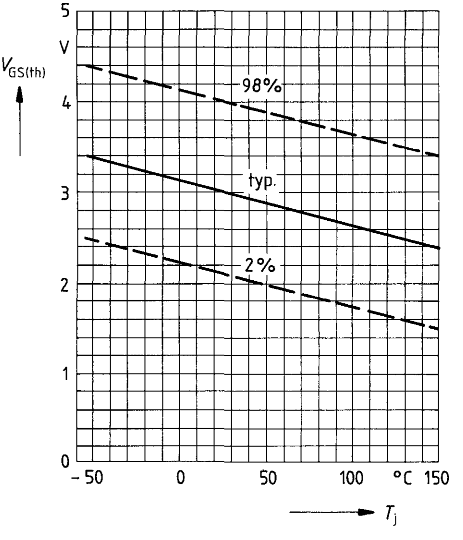
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 5A, V_{GS} = 10V
(spread)



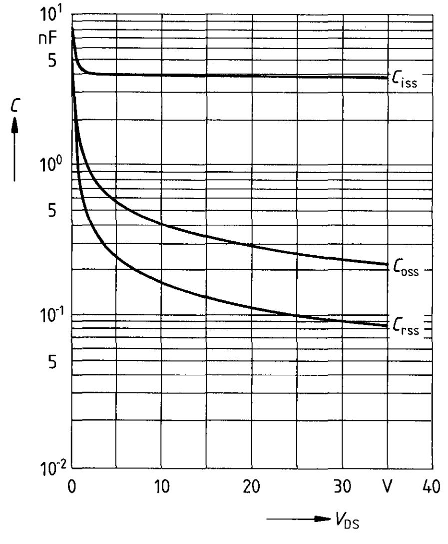
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



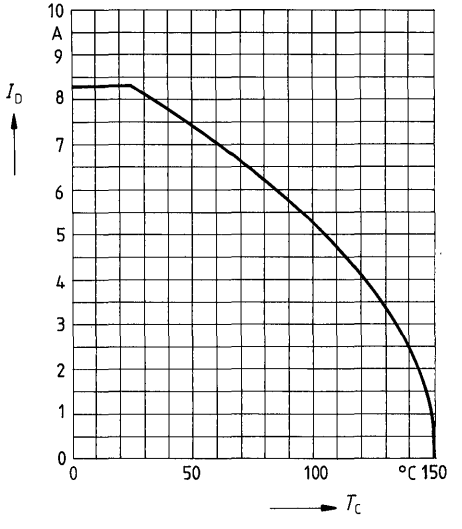
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



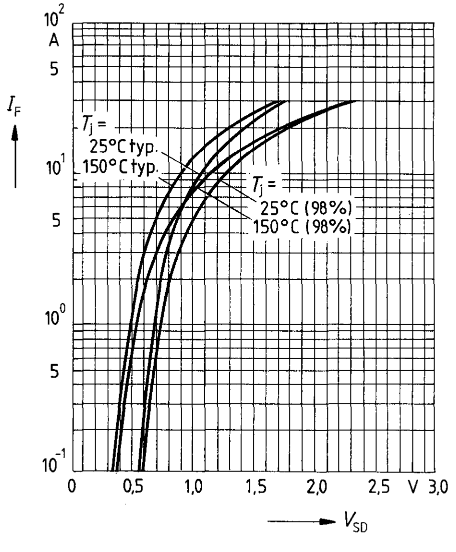
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



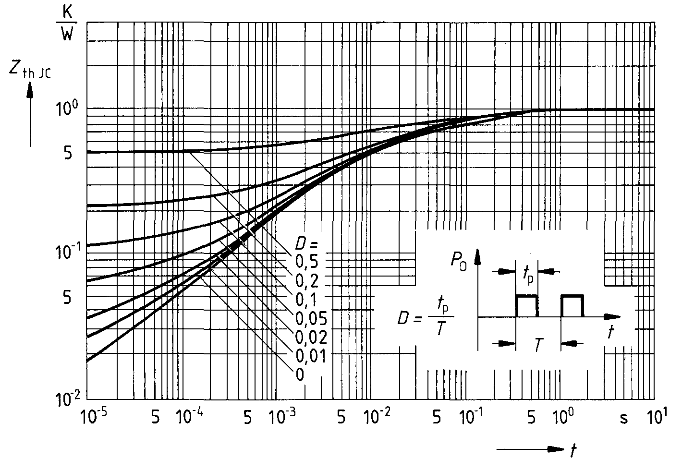
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



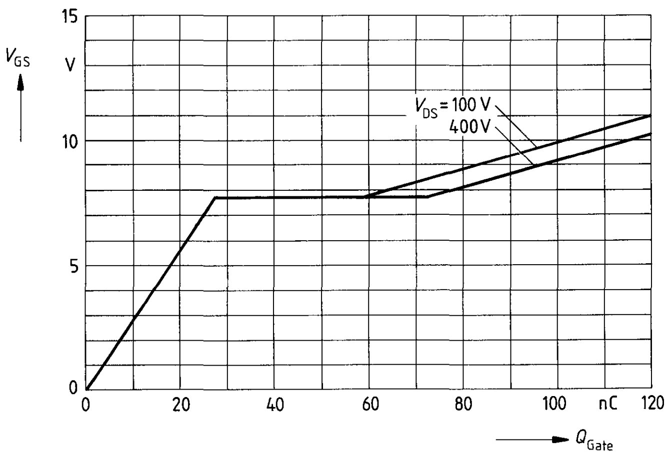
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



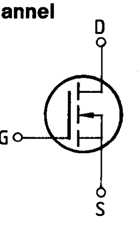
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14{,}4A$



Main ratings

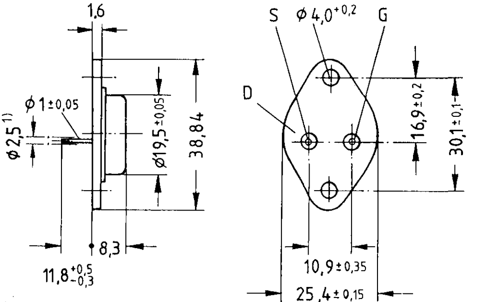
Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 10 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,5 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3A2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
BUZ 45 B	C67078-A1008-A4



1) max. bending area

Dimensions in mm

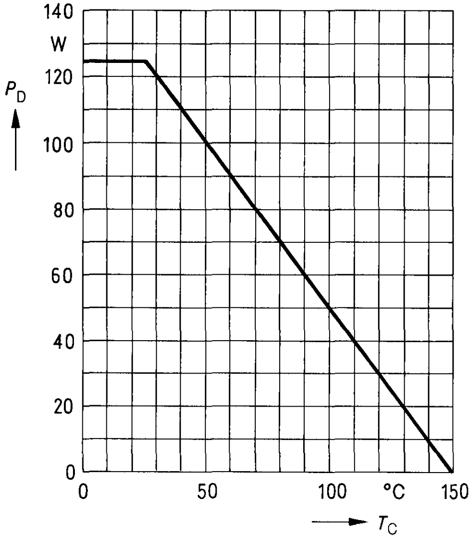
Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	10	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	40	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

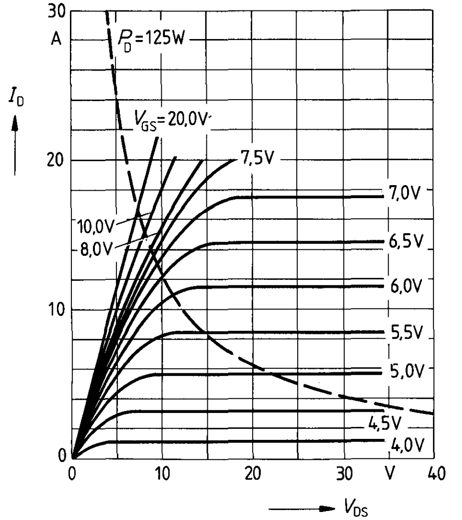
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,49	0,50	Ω	V_{GS} = 10V I_D = 5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	5,0	–	S	V_{DS} = 25V I_D = 5A
Input capacitance	C_{iss}	–	3800	4900	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400		
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	10	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	40		
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

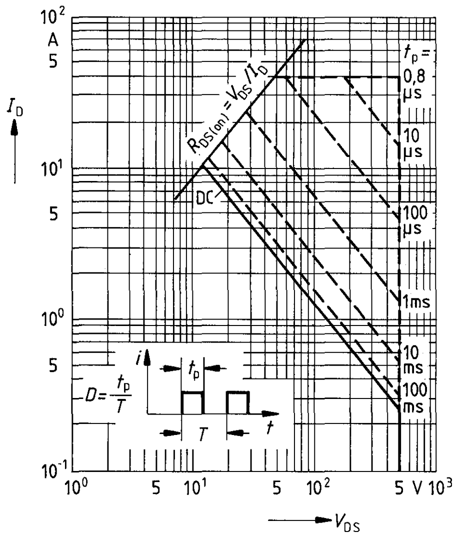
Power dissipation $P_D = f(T_C)$



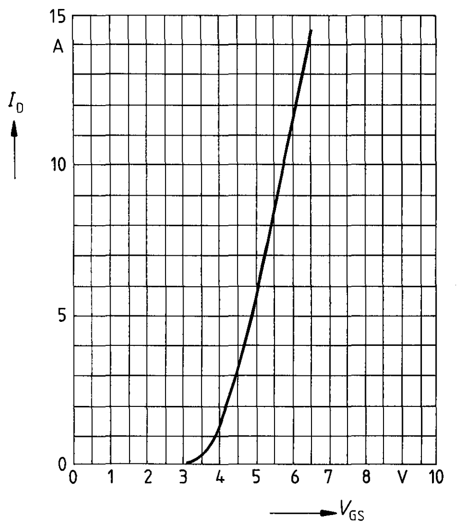
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



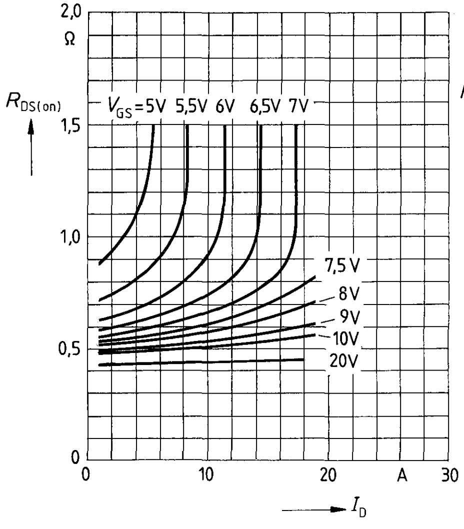
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



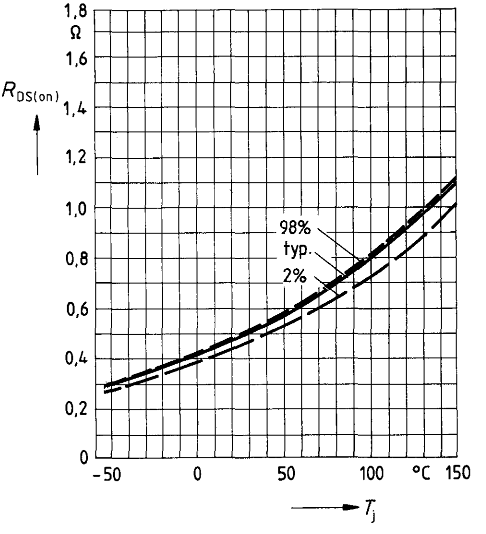
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



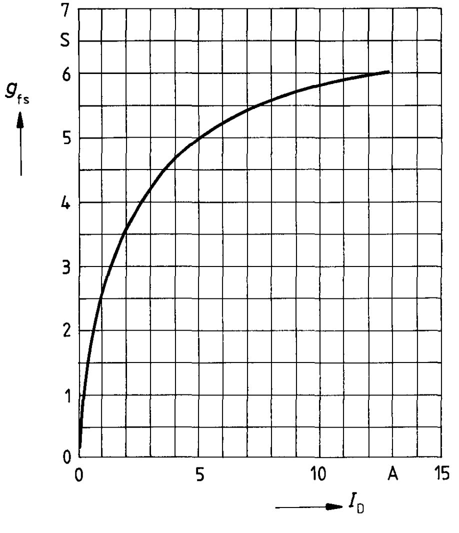
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



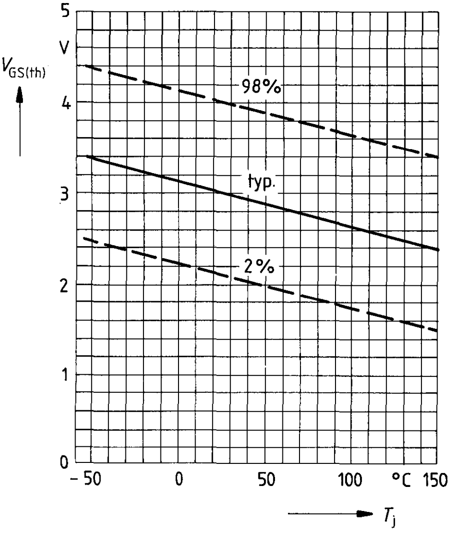
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 5A$, $V_{GS} = 10V$
(spread)



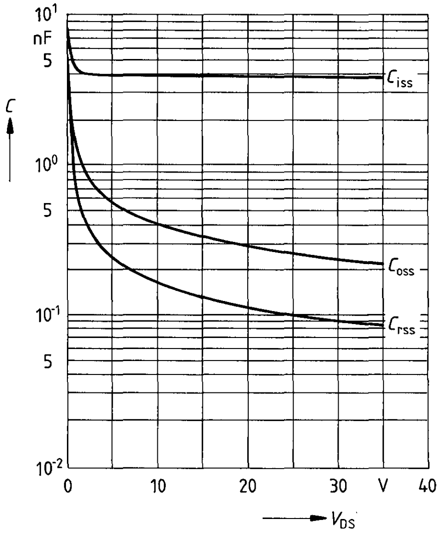
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



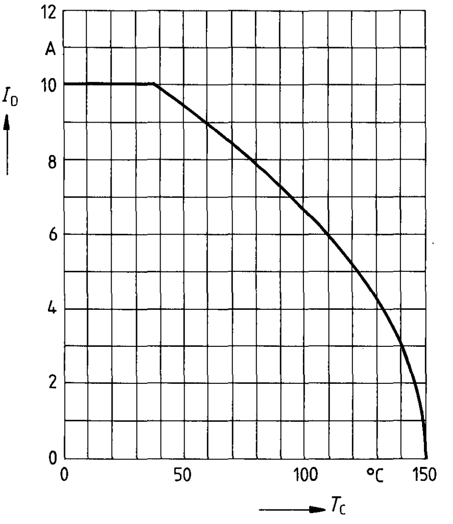
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



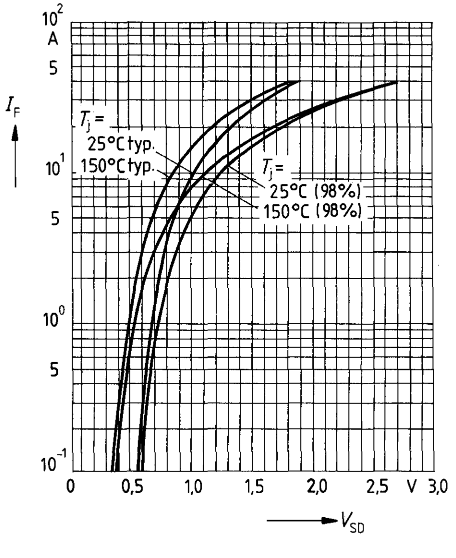
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



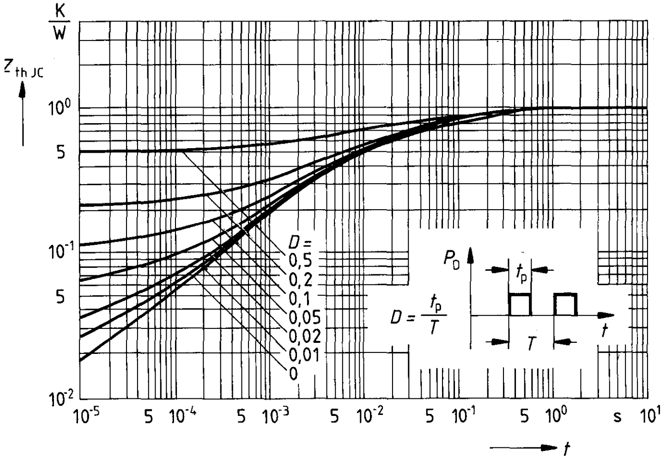
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



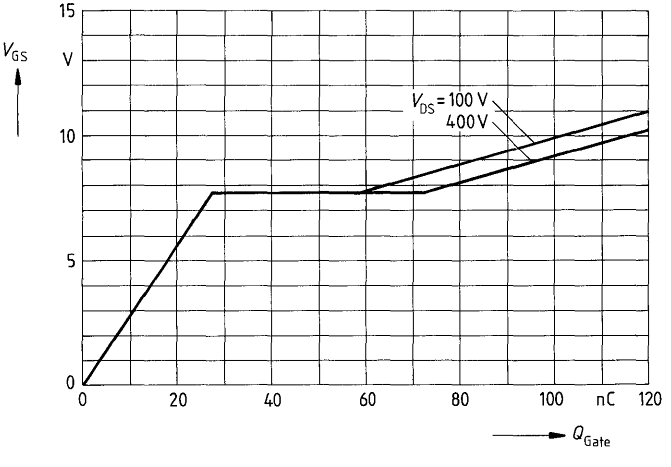
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



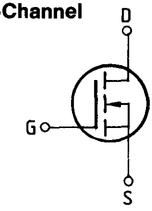
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14{,}4A$



Main ratings

Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 3,9 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,0 Ω**

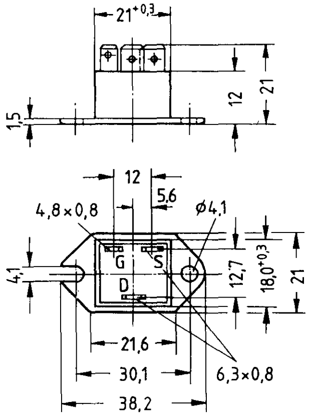
N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 47 A	C67078-A1604-A2

Not for new design



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	3,9	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	15	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	70	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–40 ... +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,78	K/W	

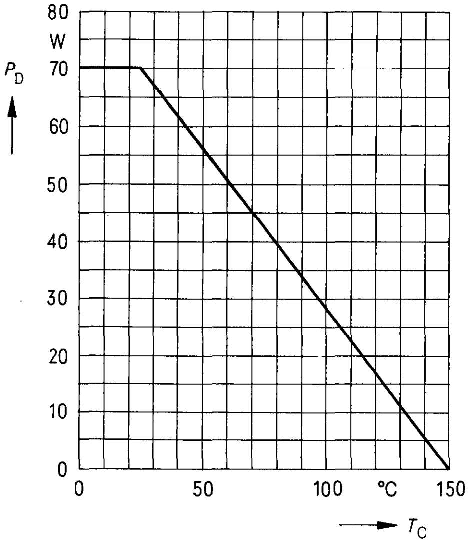
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

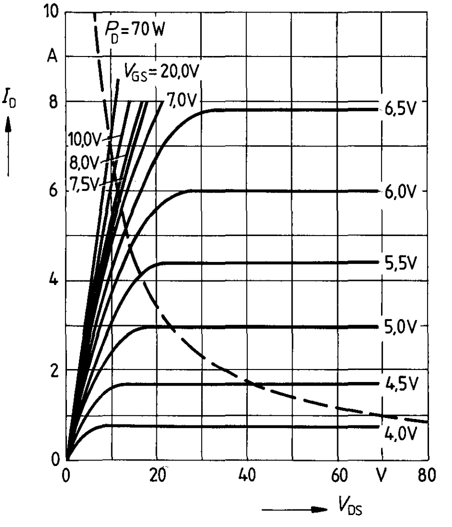
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	μA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	1,6	2,0	Ω	V_{GS} = 10V I_D = 2,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	110	170	pF	
Reverse transfer capacitance	C_{rss}	–	40	70		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	110	140		
	t_f	–	50	65		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	3,9	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	15		
Diode forward on-voltage	V_{SD}	–	1,1	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1,2	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/μs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6	–	μC	

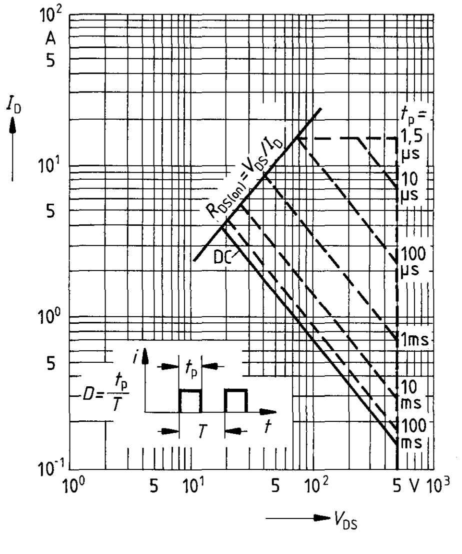
Power dissipation $P_D = f(T_C)$



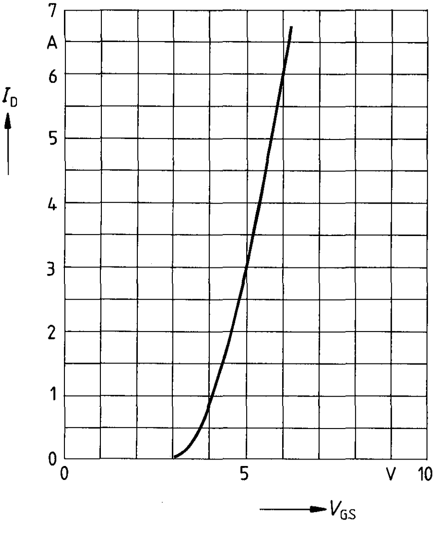
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



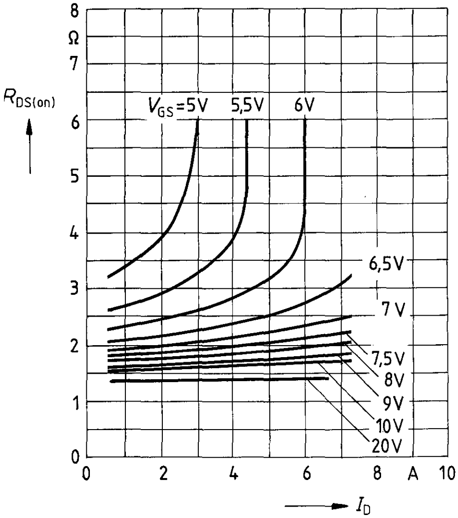
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



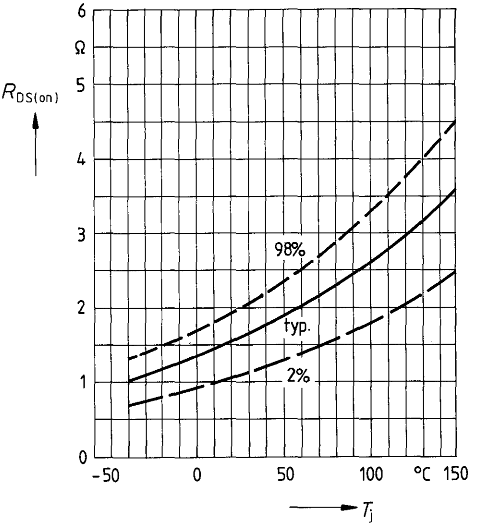
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



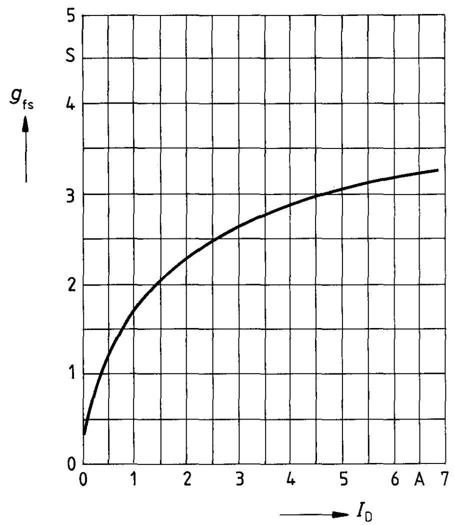
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



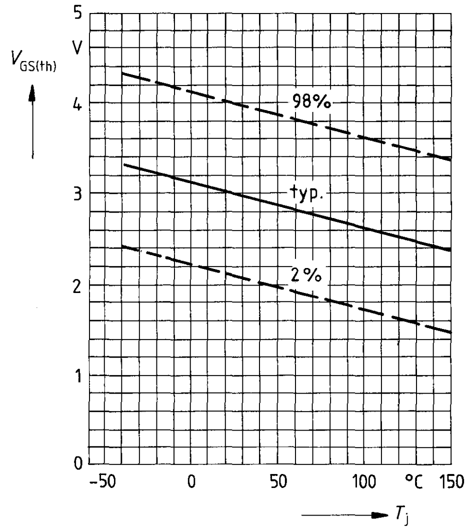
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 2,5A, V_{GS} = 10V
(spread)



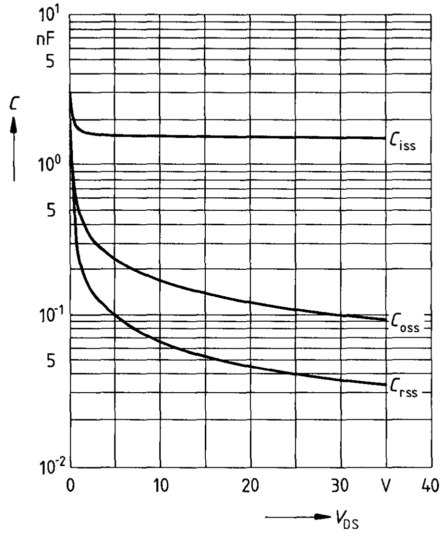
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



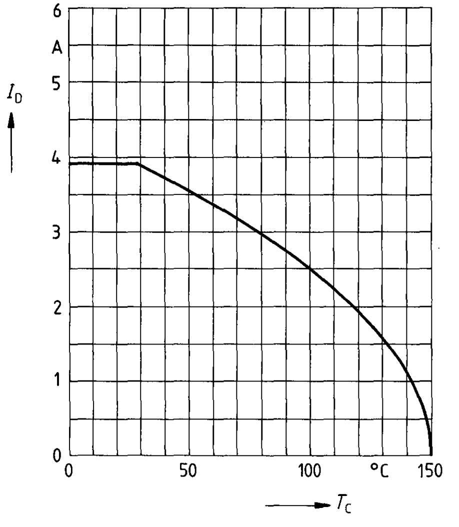
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



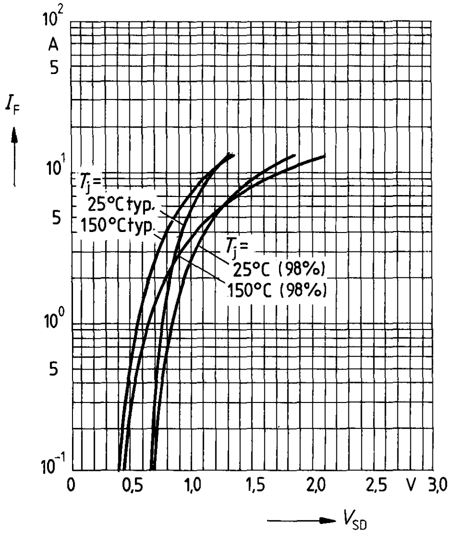
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



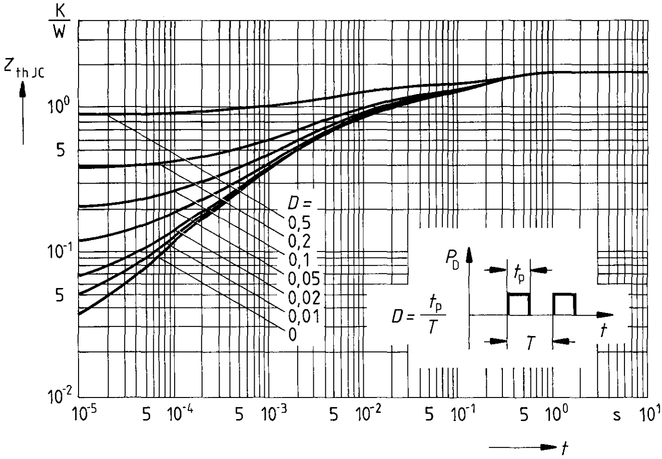
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



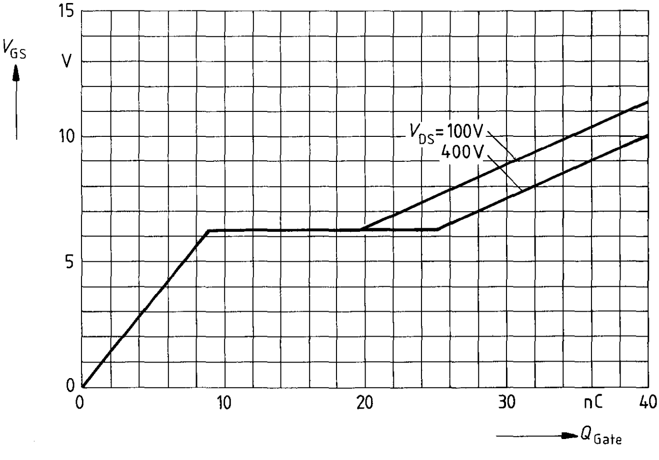
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



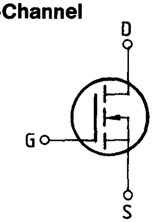
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 6{,}8A$



Main ratings

Drain-source voltage	V_{DS}	= **500 V**
Continuous drain current	I_D	= **7,8 A**
Drain-source on-resistance	$R_{DS(on)}$	= **0,6 Ω**

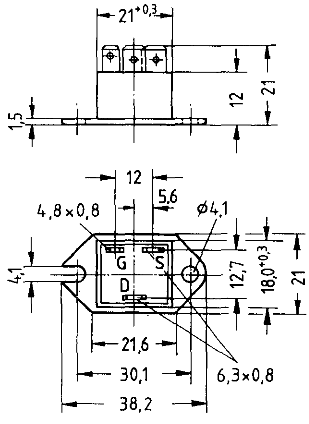
N-Channel



Description SIPMOS, N-channel, enhancement mode

Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
S BUZ 48	C67078-A1605-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	7,8	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	31	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 ... +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤1,5	K/W	

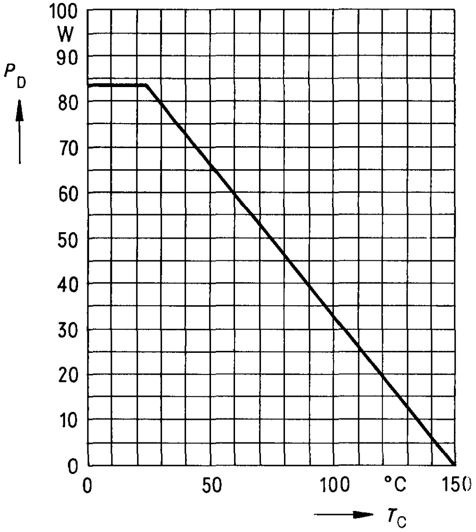
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

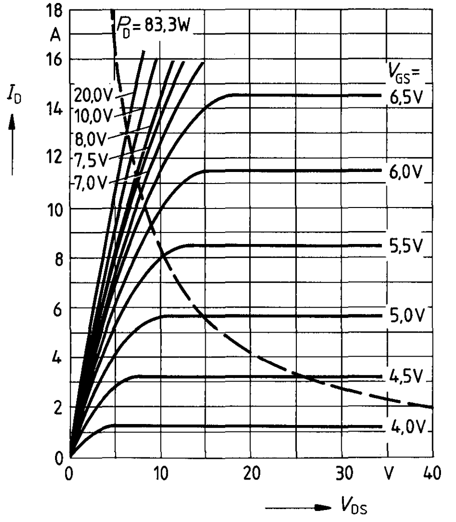
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,55	0,6	Ω	V_{GS} = 10V I_D = 5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	5,0	–	S	V_{DS} = 25V I_D = 5A
Input capacitance	C_{iss}	–	3800	4900	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400		
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} (t_{on} = $t_{d\,(on)}$ + t_r)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} (t_{off} = $t_{d\,(off)}$ + t_f)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	7,8	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	31		
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

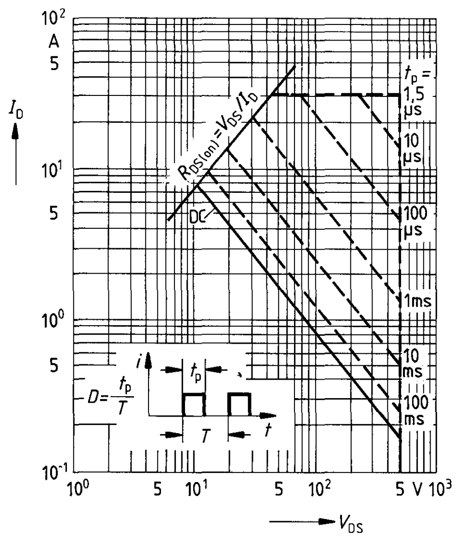
Power dissipation $P_D = f(T_C)$



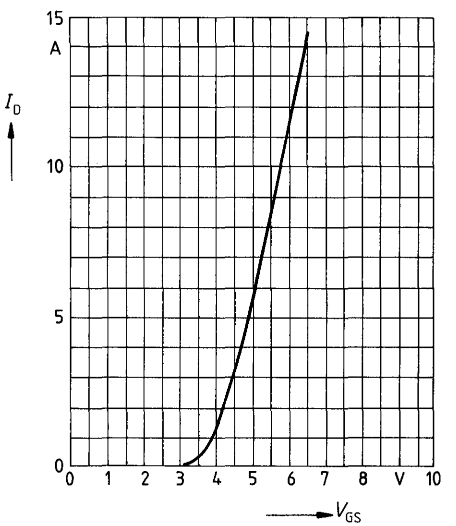
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



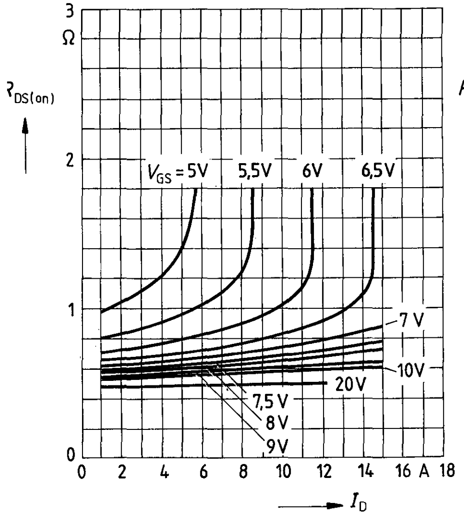
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



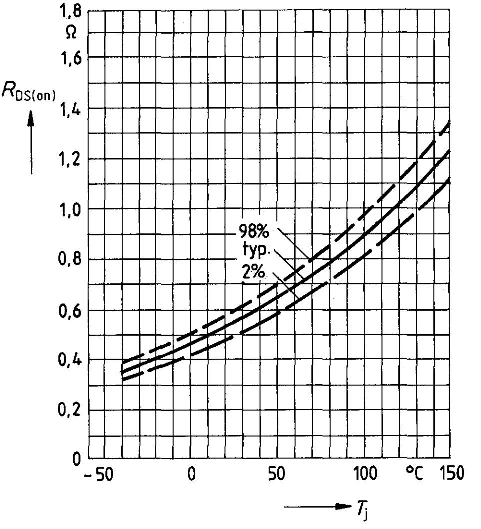
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\text{V}$, $T_j = 25\,°C$



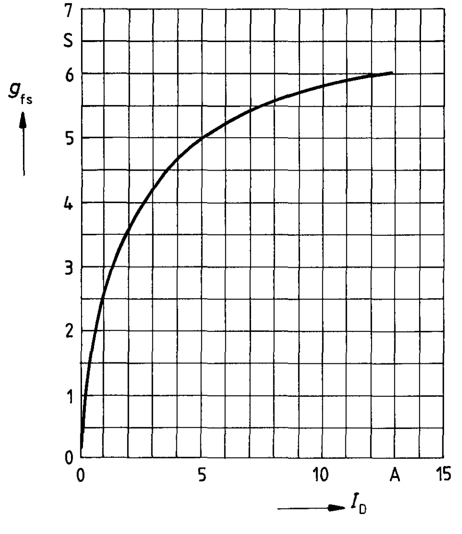
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



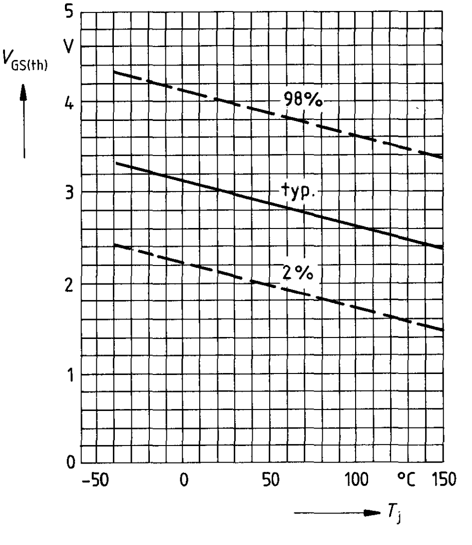
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 5,5A, V_{GS} = 10V
(spread)



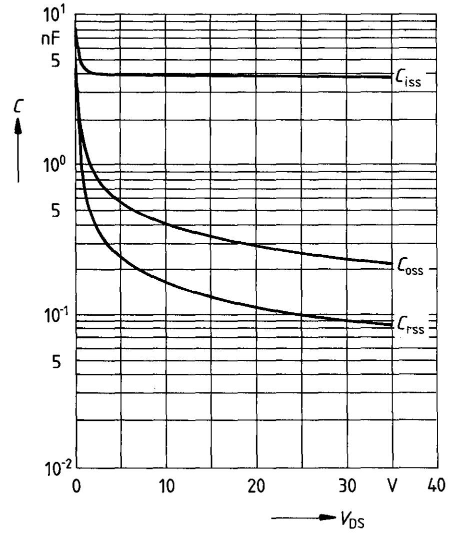
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



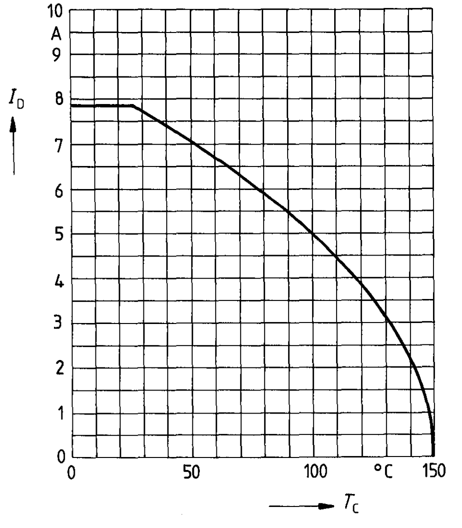
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



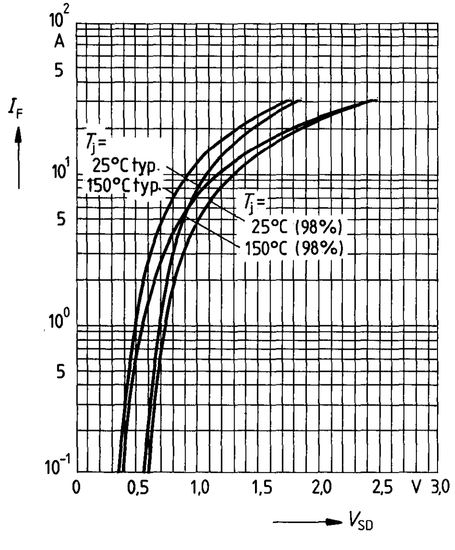
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



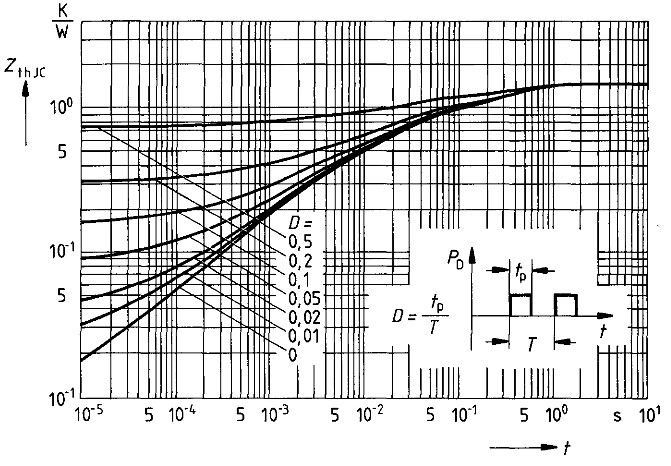
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



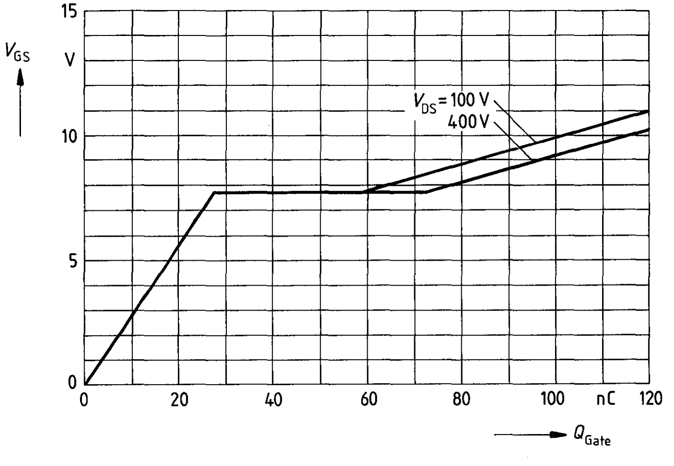
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p/T$

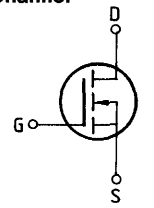


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14{,}4A$



Main ratings

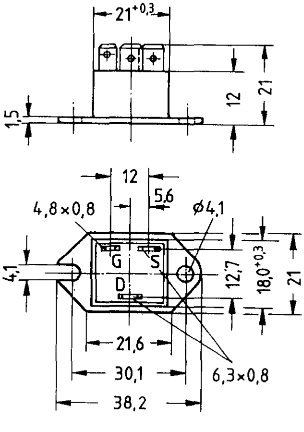
N-Channel



Drain-source voltage V_{DS} = **500 V**
Continuous drain current I_D = **6,8 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,8 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 48 A	C67078-A1605-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	6,8	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	27	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 ... +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\,JC}$	≤1,5	K/W	

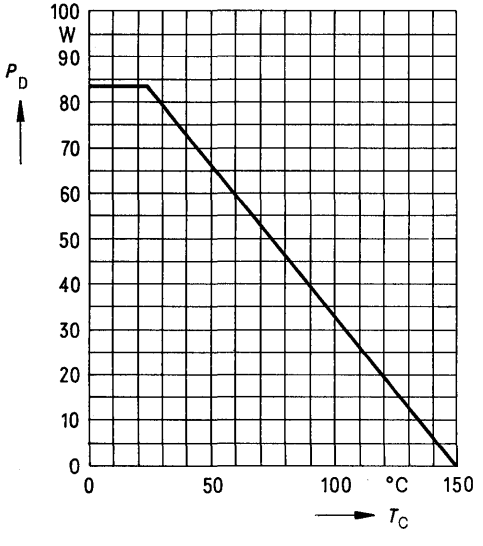
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

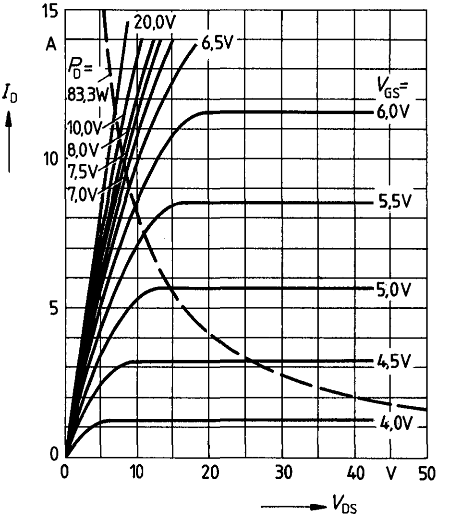
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,7	0,8	Ω	V_{GS} = 10V I_D = 5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	5,0	–	S	V_{DS} = 25V I_D = 5A
Input capacitance	C_{iss}	–	3800	4900	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400		
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} (t_{on} = $t_{d\,(on)}$ + t_r)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} (t_{off} = $t_{d\,(off)}$ + t_f)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	6,8	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	27		
Diode forward on-voltage	V_{SD}	–	1,3	1,55	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

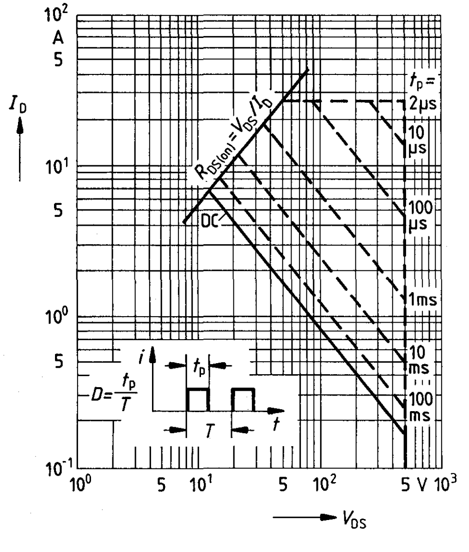
Power dissipation $P_D = f(T_C)$



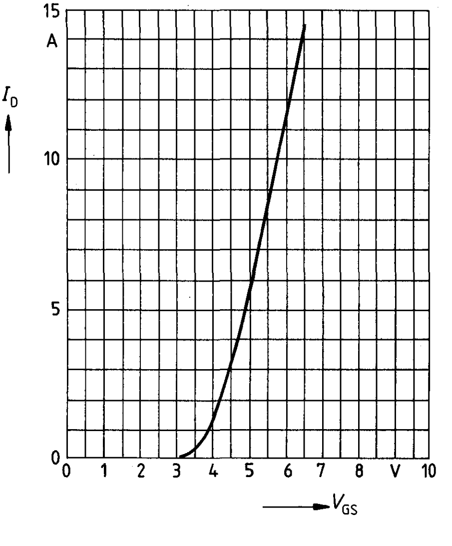
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



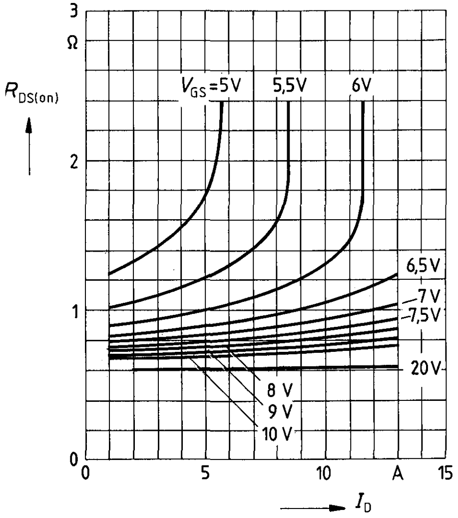
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



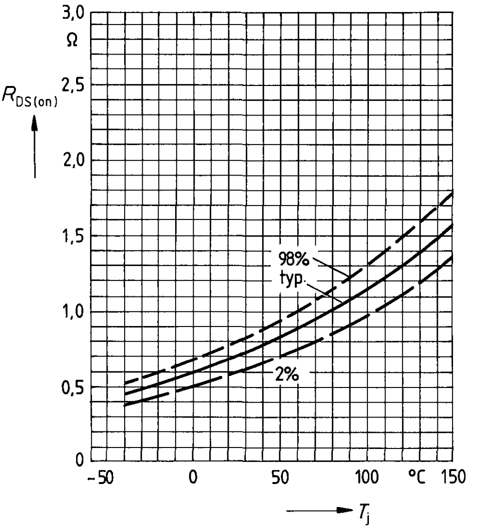
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



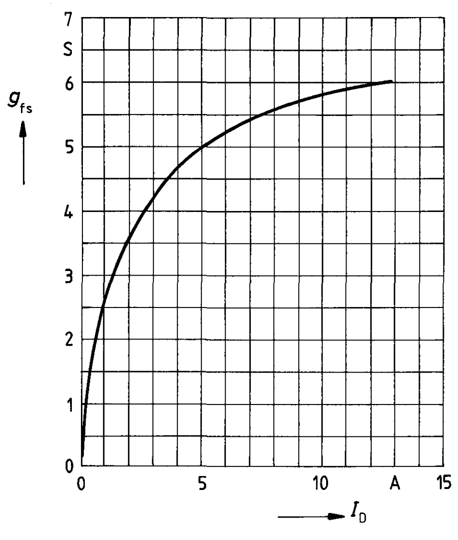
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



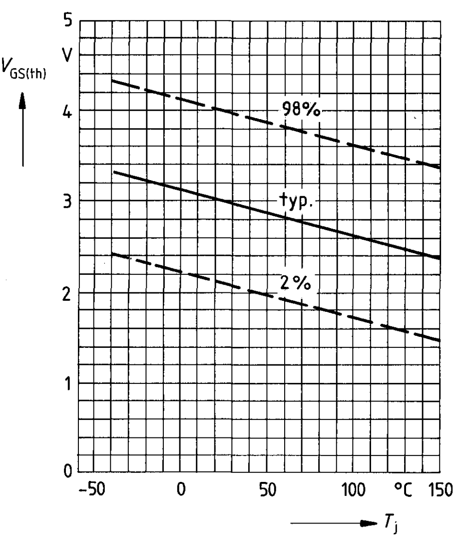
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 5A$, $V_{GS} = 10V$
(spread)



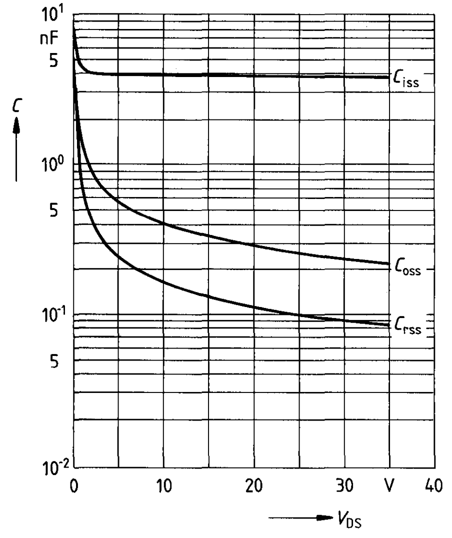
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



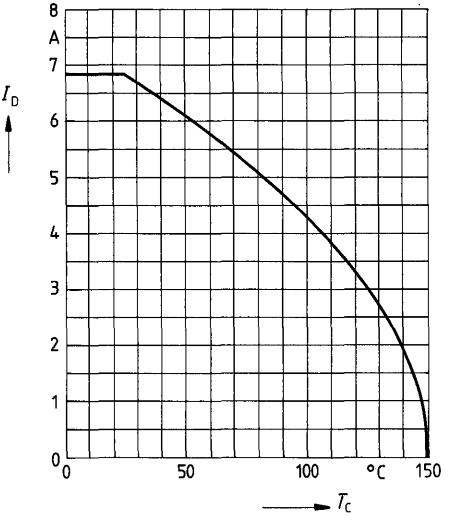
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



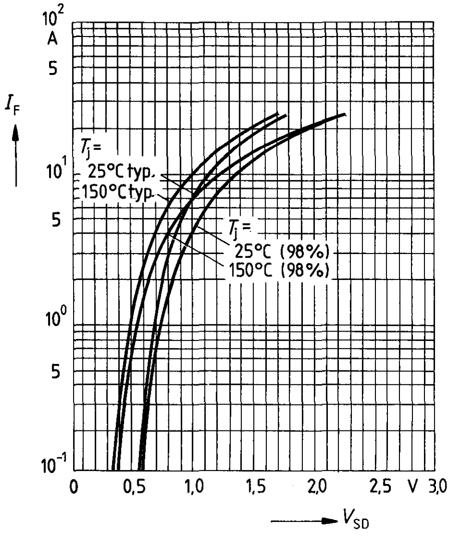
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



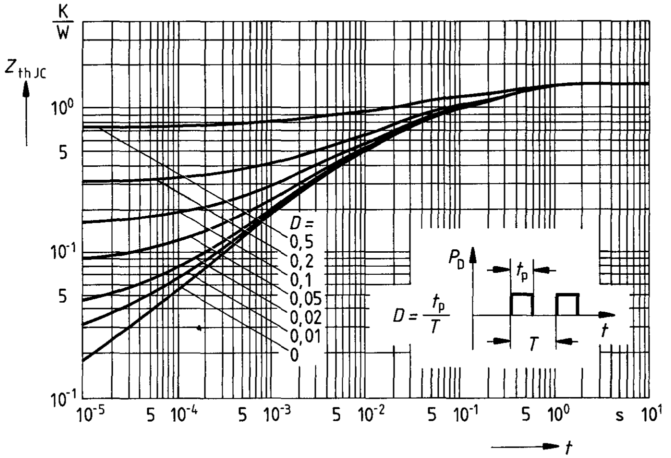
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



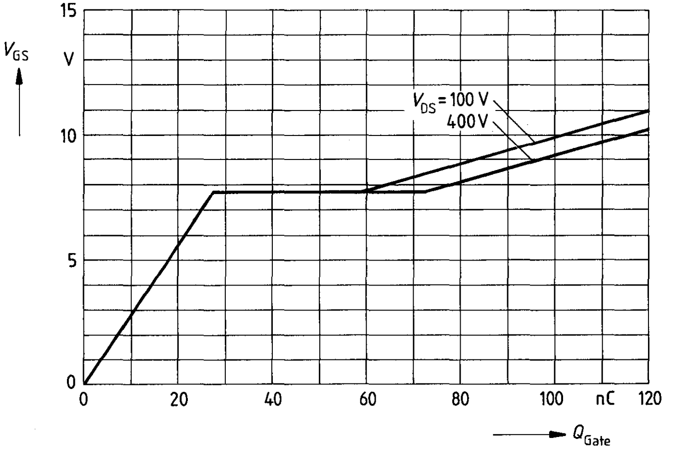
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



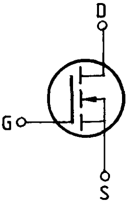
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14{,}4A$



Main ratings

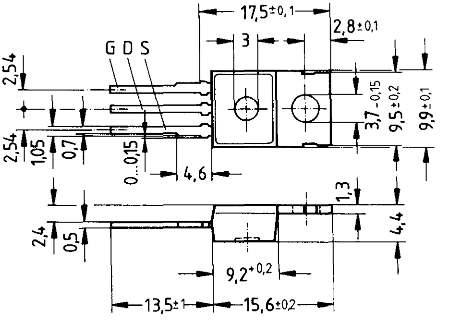
Drain-source voltage V_{DS} **= 1000 V**
Continuous drain current I_D **= 2,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 5,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 50 A	C67078-A1307-A3



Dimensions in mm

Maximum ratings

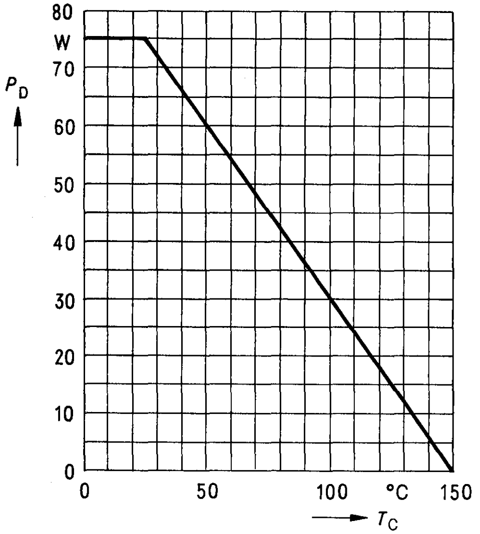
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	10	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

 S Preferred Type

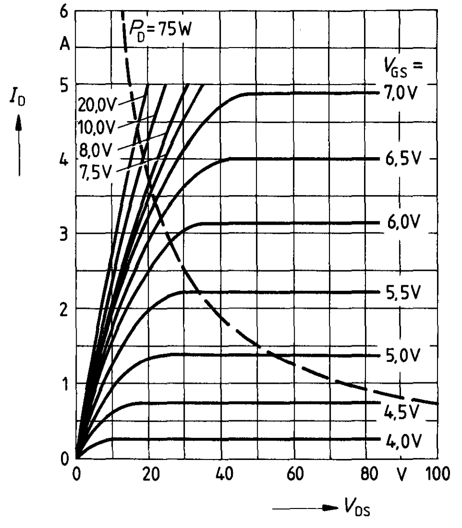
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	4,5	5,0	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	0,7	1,5	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	1600	2100	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	70	120		
Reverse transfer capacitance	C_{rss}	–	30	50		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	10		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	15	–	µC	

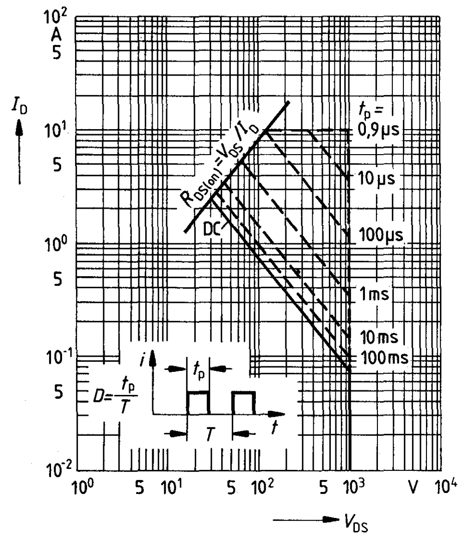
Power dissipation $P_D = f(T_C)$



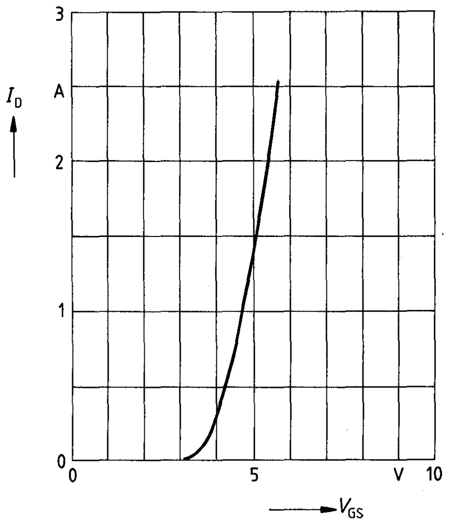
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25°C$



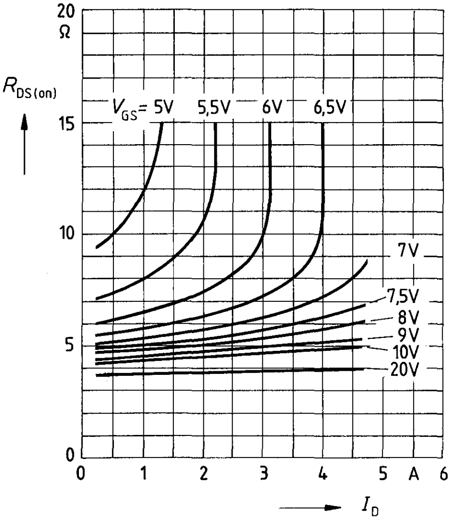
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25°C$



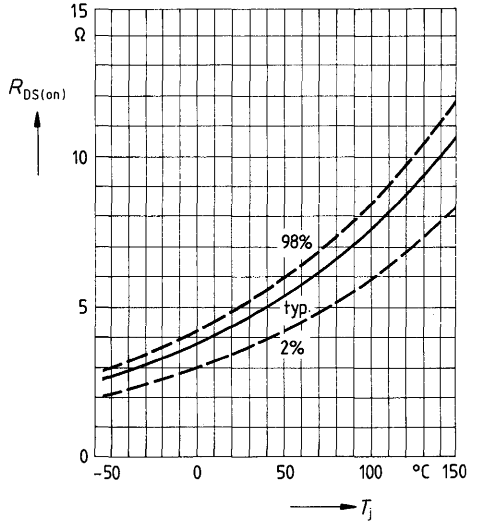
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25°C$



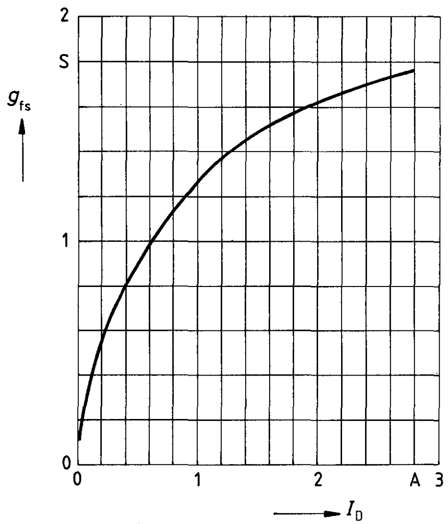
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



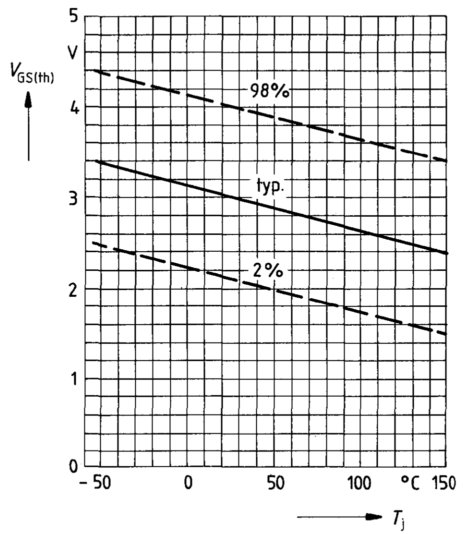
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 1,5A, V_{GS} = 10V
(spread)



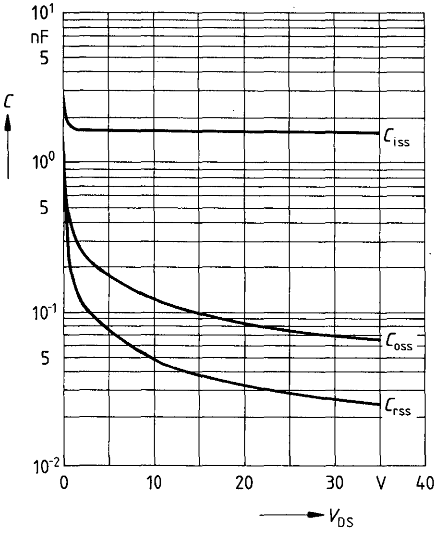
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



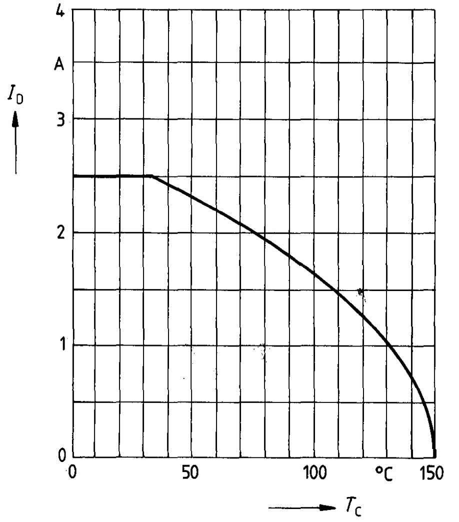
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



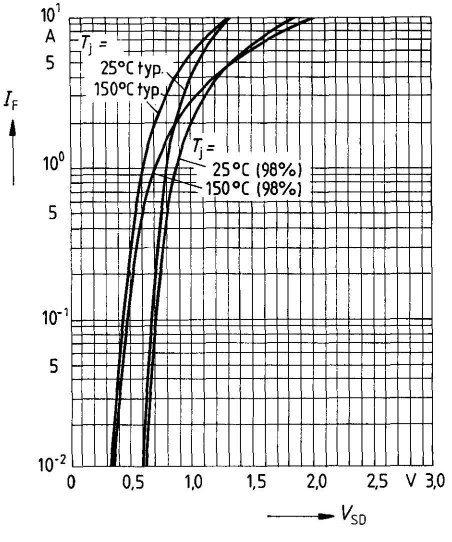
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



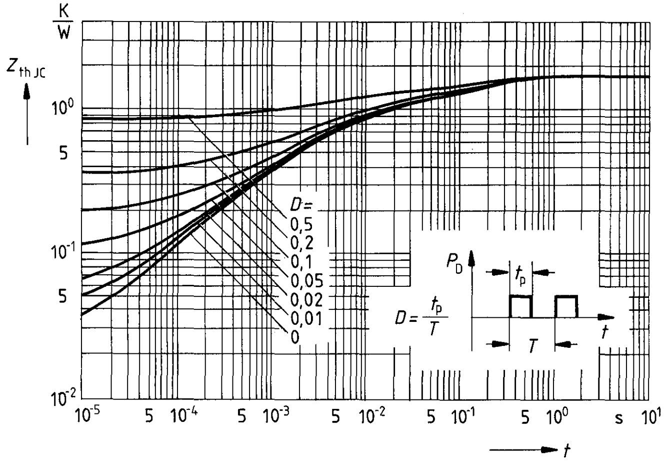
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



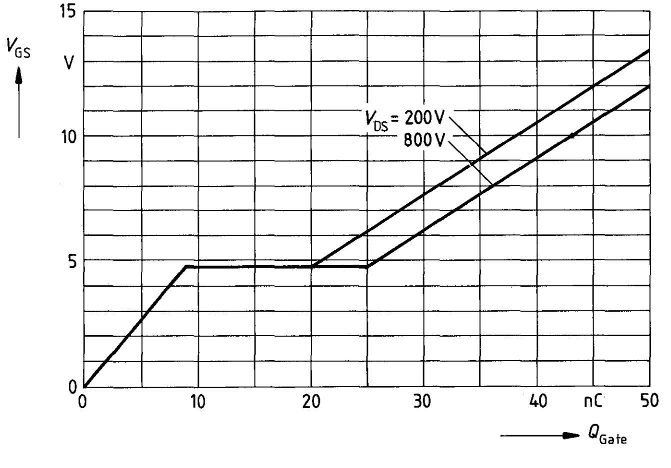
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



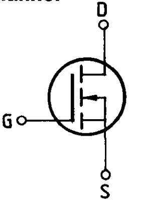
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 3{,}75A$



Main ratings

Drain-source voltage V_{DS} = **1000 V**
Continuous drain current I_D = **2 A**
Drain-source on-resistance $R_{DS(on)}$ = **8,0 Ω**

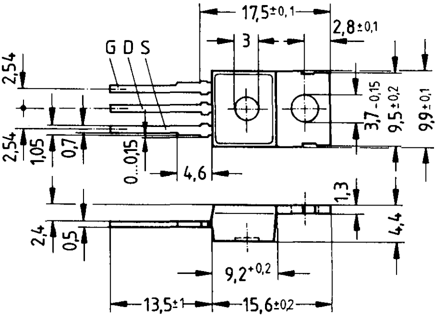
N-Channel



Description SIPMOS, N-channel, enhancement mode

Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
S BUZ 50 B	C67078-A1307-A4



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	8	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

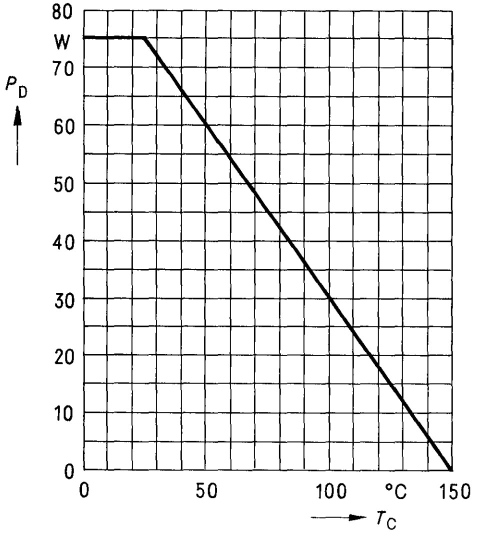
 S Preferred Type

Electrical characteristics

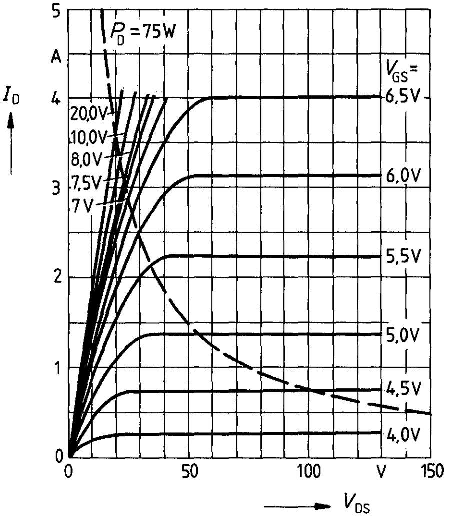
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	6,5	8,0	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	0,7	1,5	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	1600	2100	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	70	120		
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 1,7A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	8		
Diode forward on-voltage	V_{SD}	–	1,05	1,30	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{IF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	15	–	µC	

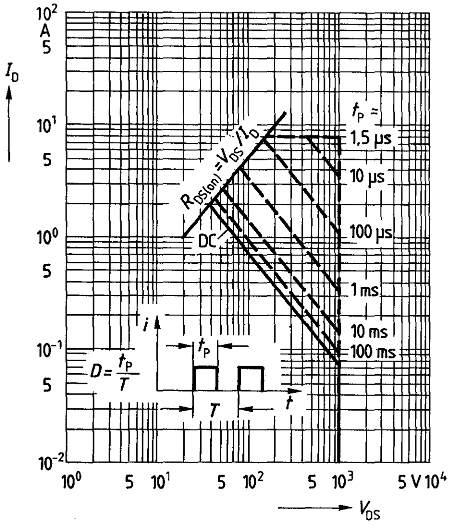
Power dissipation $P_D = f(T_C)$



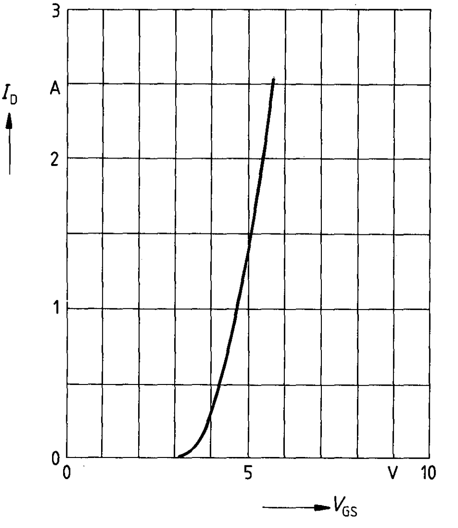
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



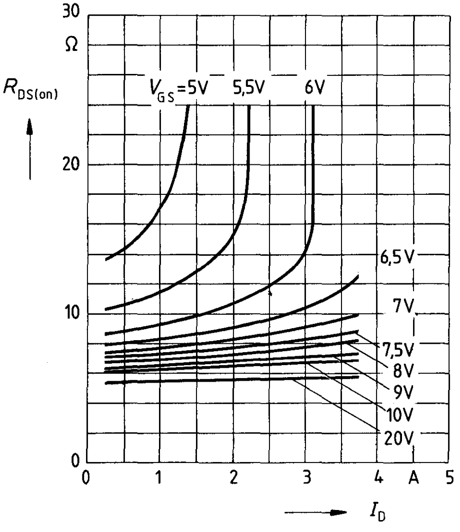
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



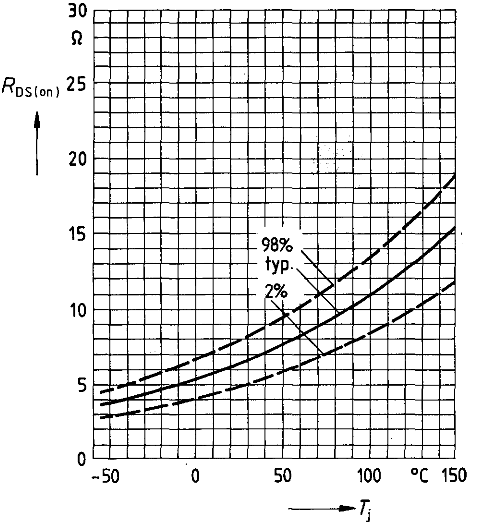
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\text{V}$, $T_j = 25\,°C$



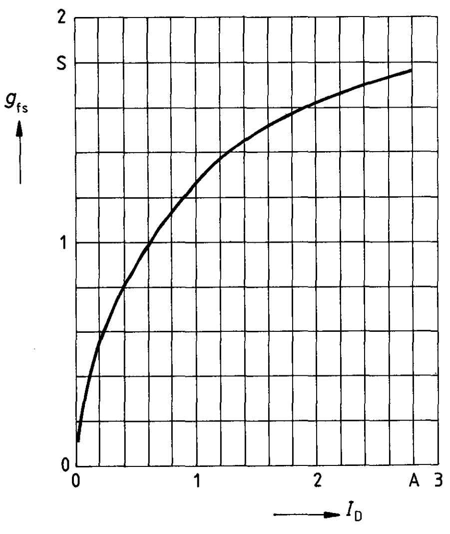
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



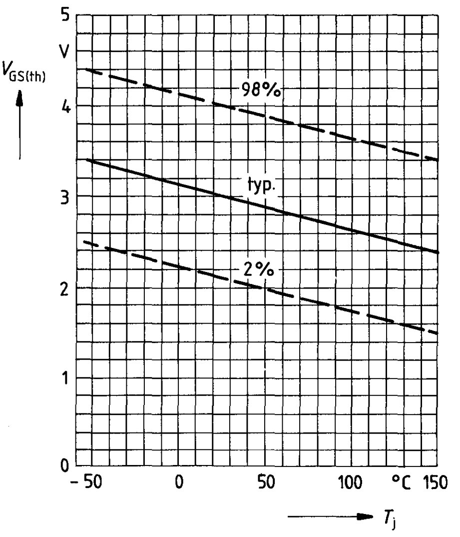
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 2{,}5A$, $V_{GS} = 10V$
(spread)



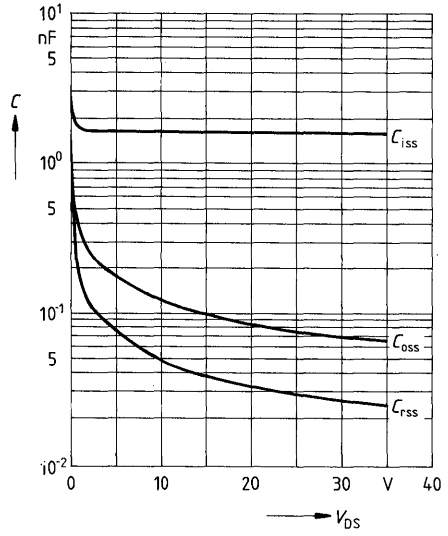
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



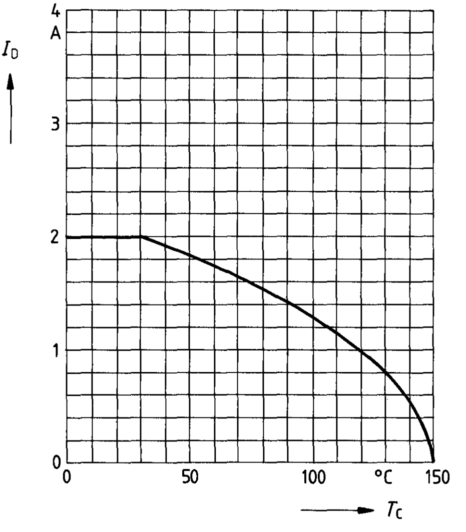
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



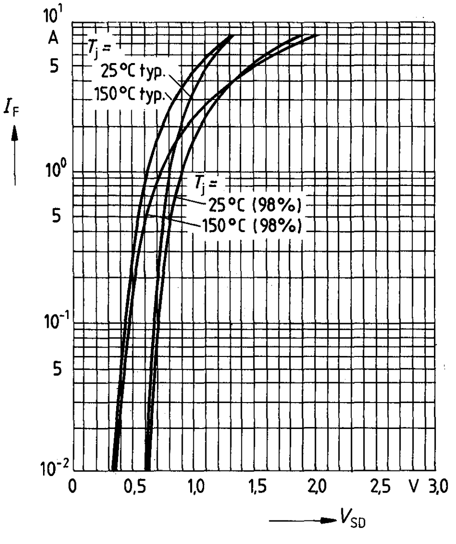
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



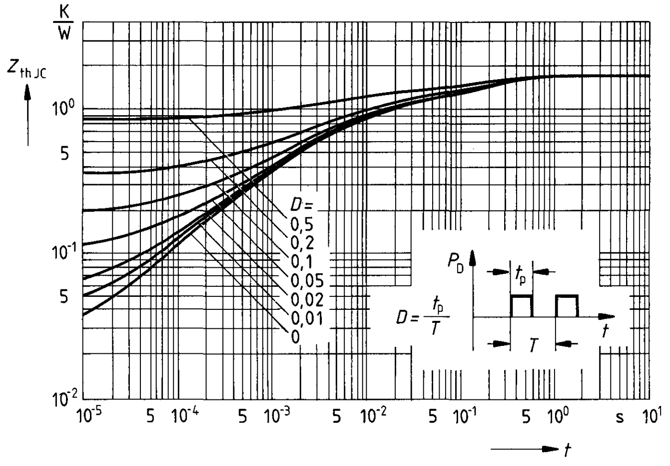
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



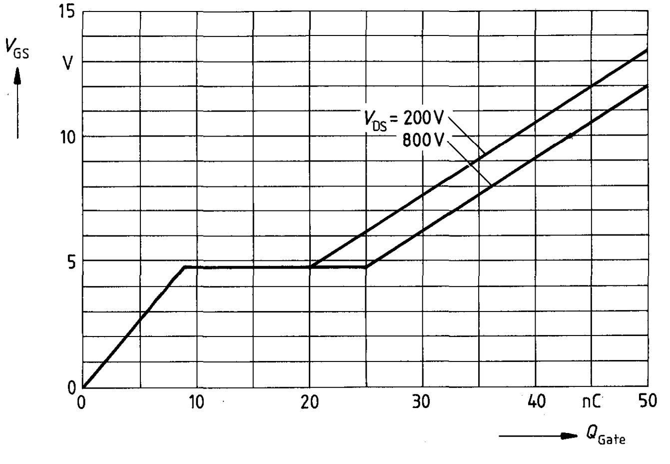
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

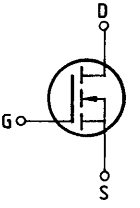


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 3{,}75A$



Main ratings

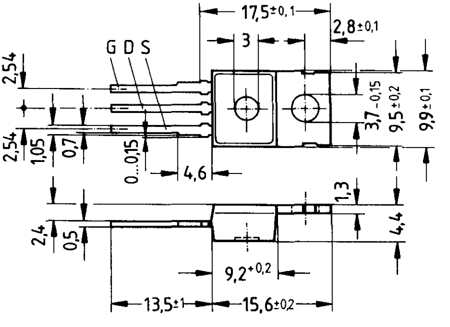
N-Channel



Drain-source voltage V_{DS} = **1000 V**
Continuous drain current I_D = **2,3 A**
Drain-source on-resistance $R_{DS(on)}$ = **6,0 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
BUZ 50 C	C67078-A1307-A5



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,3	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	9,0	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

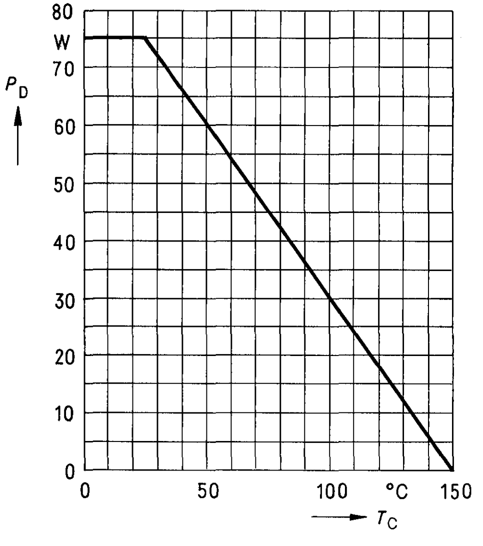
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

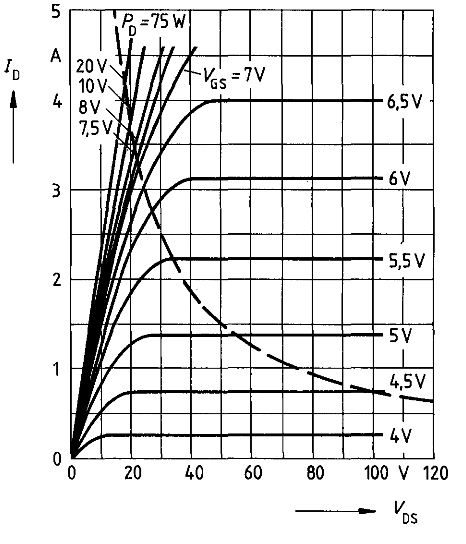
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	5,0	6,0	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	0,7	1,5	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	70	120	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} (t_{on} = $t_{d\,(on)}$ + t_r)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 1,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} (t_{off} = $t_{d\,(off)}$ + t_f)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,3	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	9,0		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	15	–	µC	

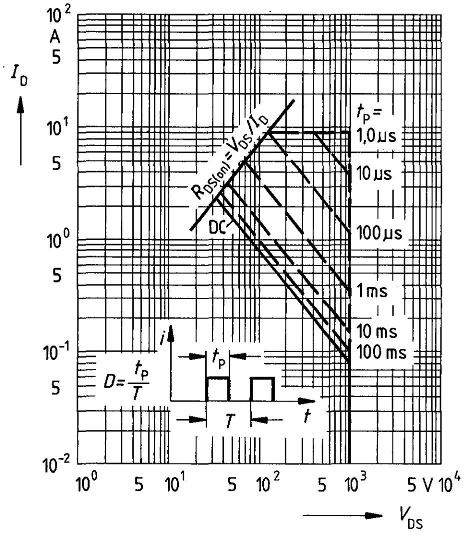
Power dissipation $P_D = f(T_C)$



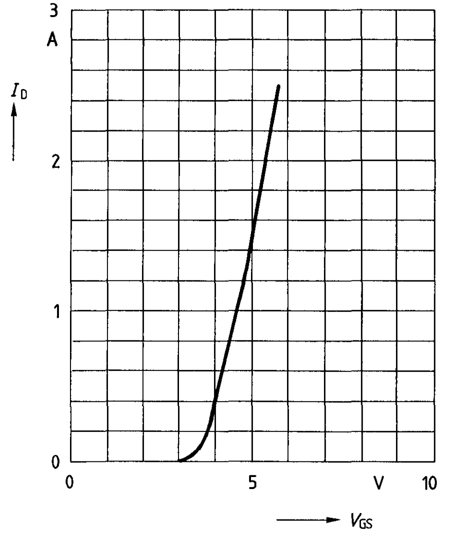
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



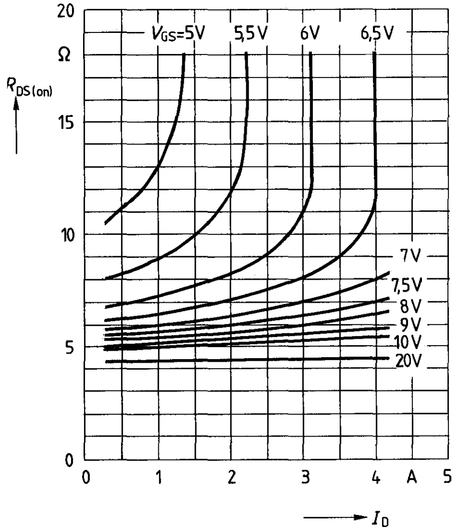
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



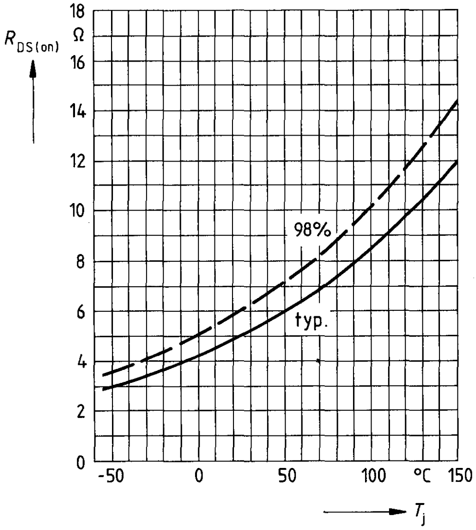
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25$V, $T_j = 25\,°C$



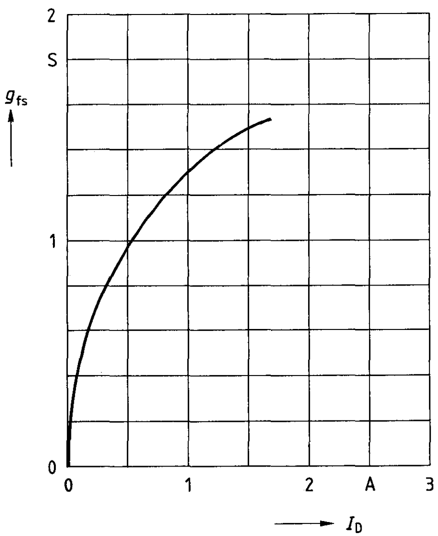
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



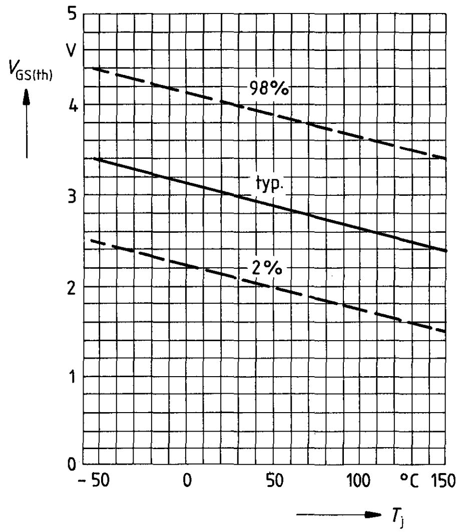
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 1,5A, V_{GS} = 10V
(spread)



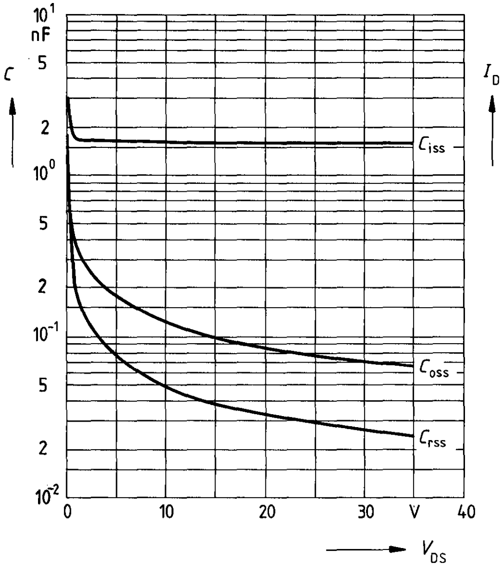
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



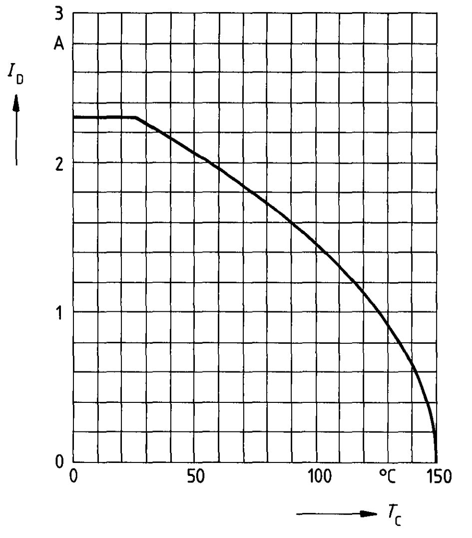
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



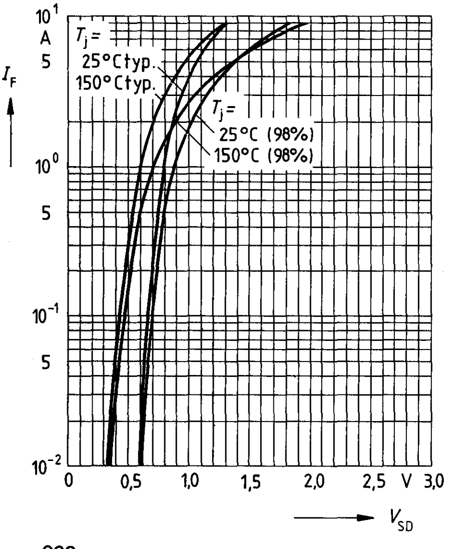
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



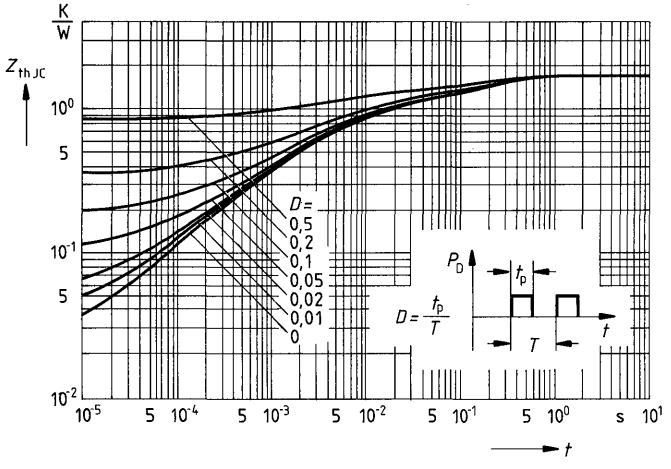
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



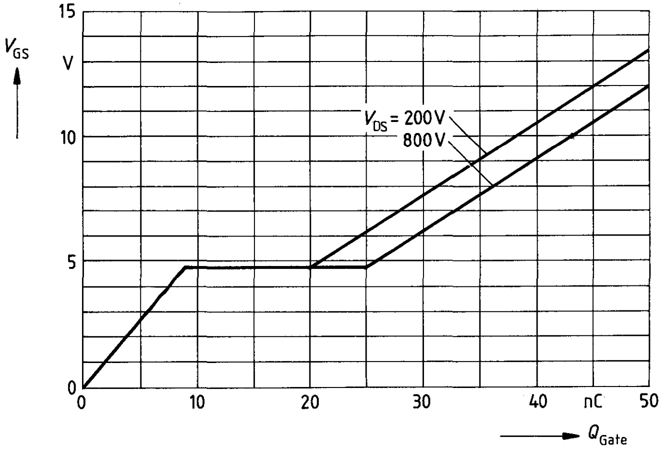
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

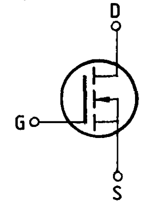


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 3{,}75A$



Main ratings

N-Channel

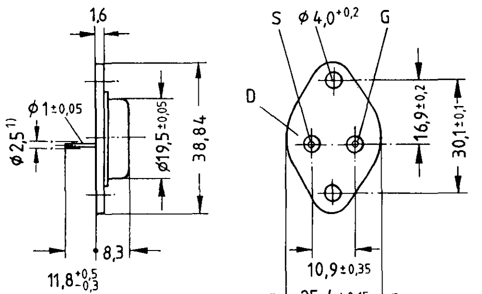


Drain-source voltage	V_{DS}	**= 1000 V**
Continuous drain current	I_D	**= 2,6 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 5,0 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Metal case 3A2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 53 A	C67078-A1009-A3



1) max. bending area

Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,6	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	10	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,6	K/W	
Chip – ambient	$R_{th\ JA}$	≤35	K/W	

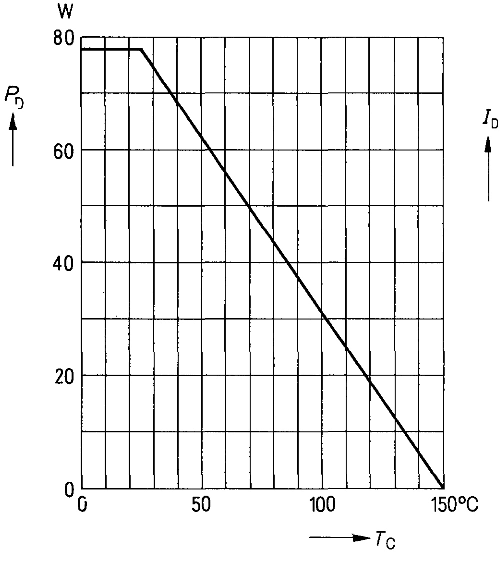
 S Preferred Type

Electrical characteristics

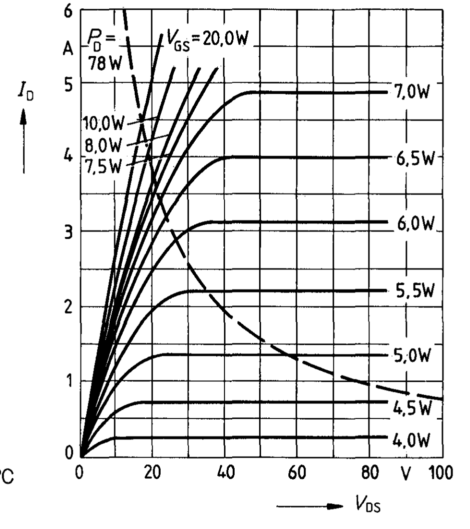
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	4,5	5,0	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	0,7	1,5	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	70	120	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,6	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	10		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	15	–	µC	

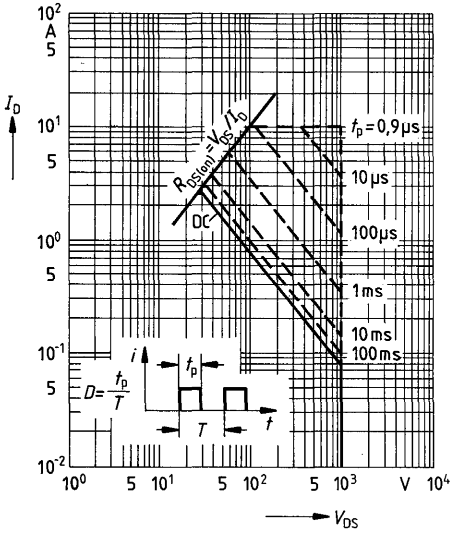
Power dissipation $P_D = f(T_C)$



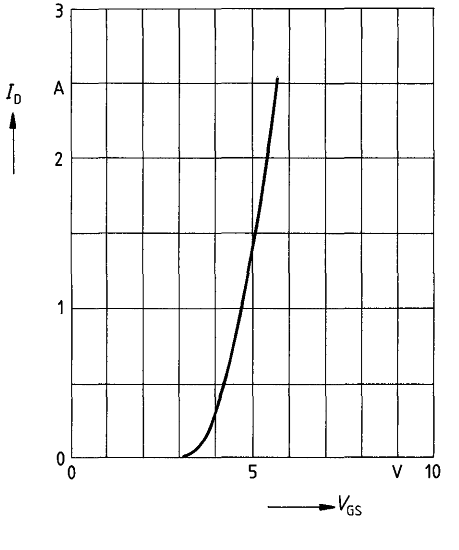
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



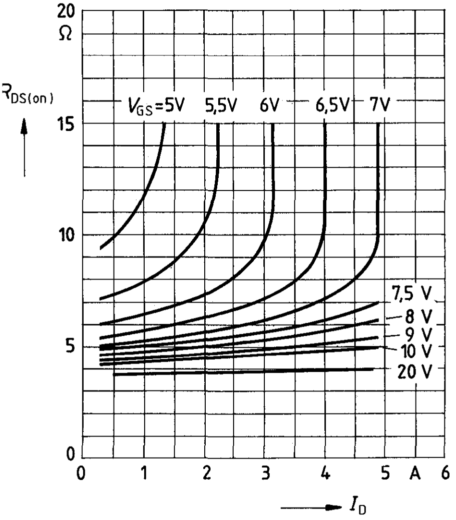
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



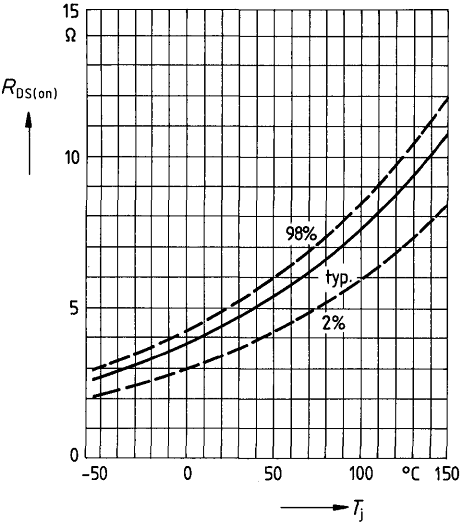
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



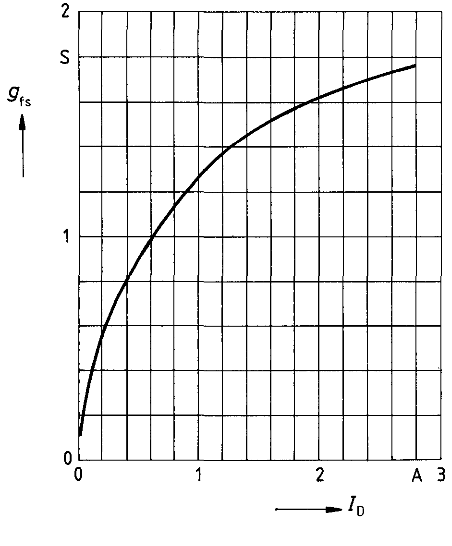
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



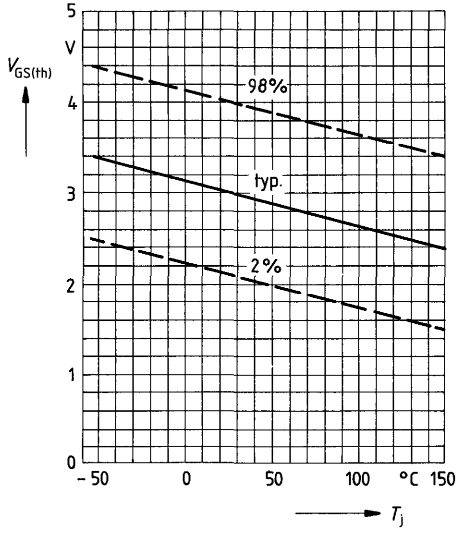
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 1{,}5A$, $V_{GS} = 10V$
(spread)



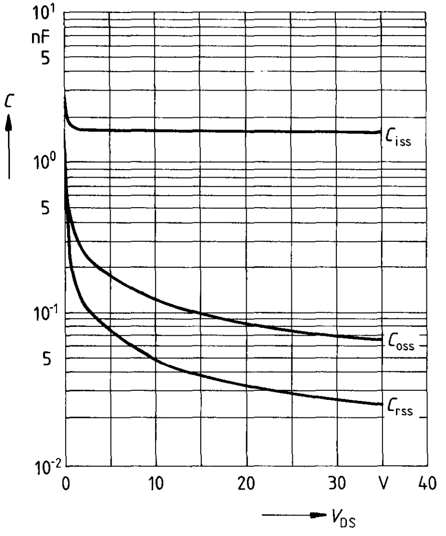
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



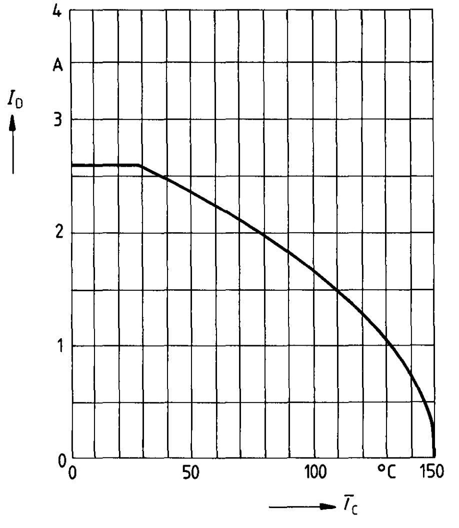
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



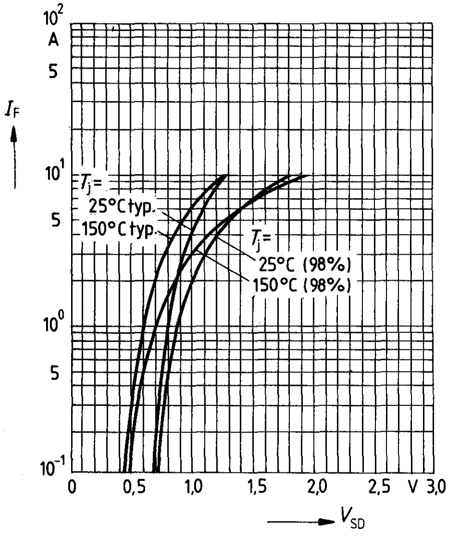
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



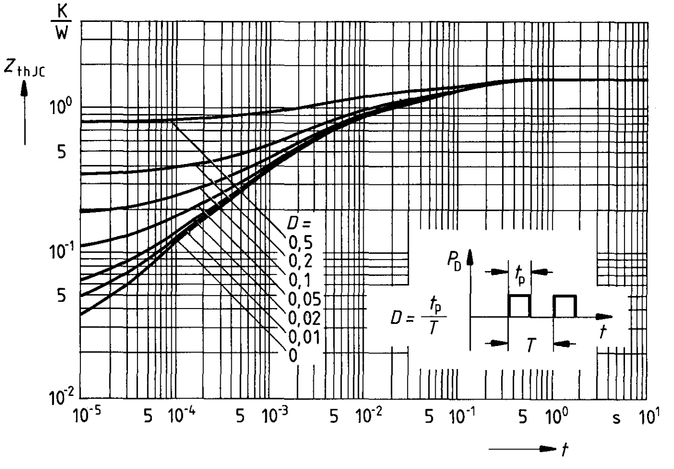
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



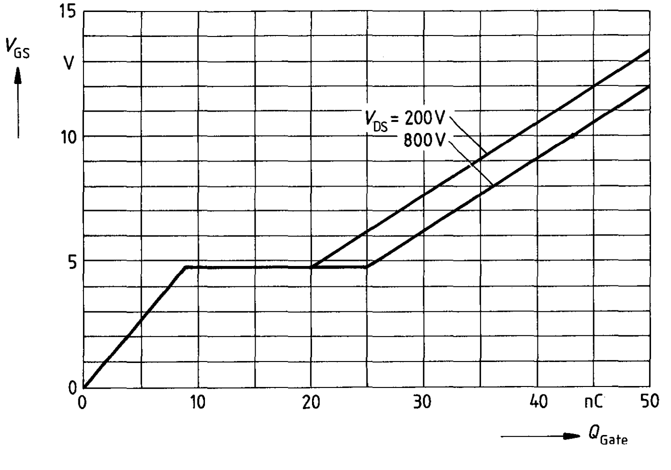
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



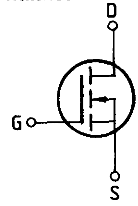
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 3{,}75A$



Main ratings

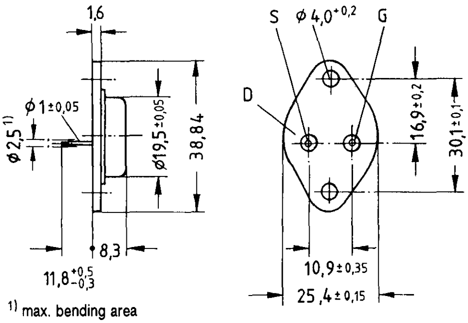
Drain-source voltage V_{DS} **= 1000 V**
Continuous drain current I_D **= 2,3 A**
Drain-source on-resistance $R_{DS(on)}$ **= 6 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
BUZ 53 C	C67078-A1009-A5



Dimensions in mm

Maximum ratings

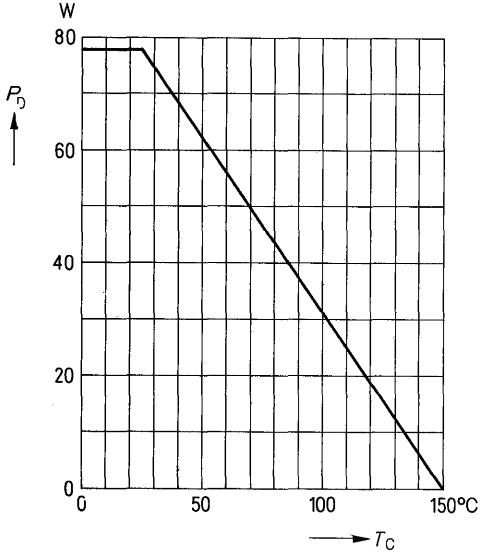
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,3	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	9,0	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤ 1,6	K/W	
Chip – ambient	$R_{th\ JA}$	≤ 35	K/W	

Electrical characteristics

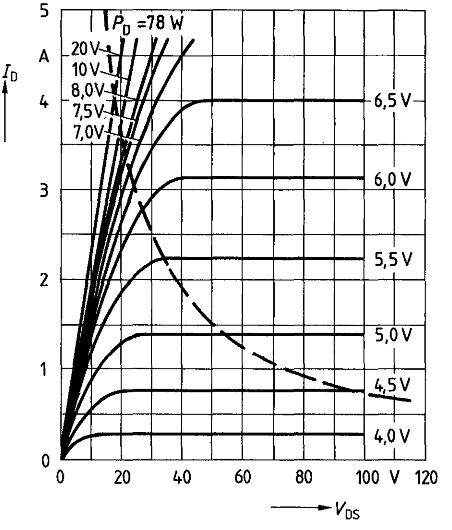
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	5,0	6,0	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	0,7	1,5	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	70	120	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 1,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,3	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	9,0		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	15	–	µC	

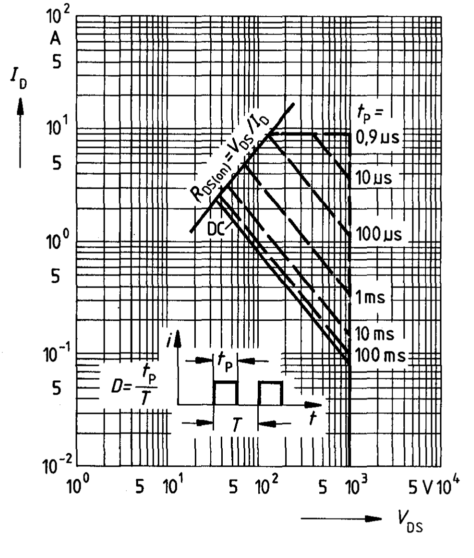
Power dissipation $P_D = f(T_C)$



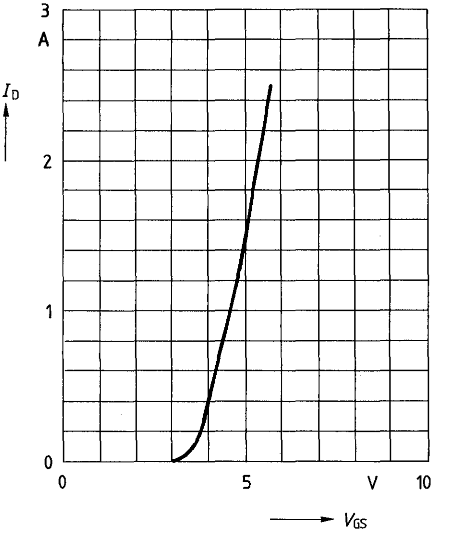
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



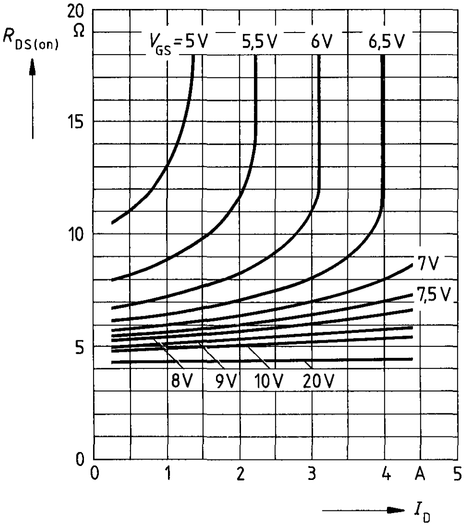
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



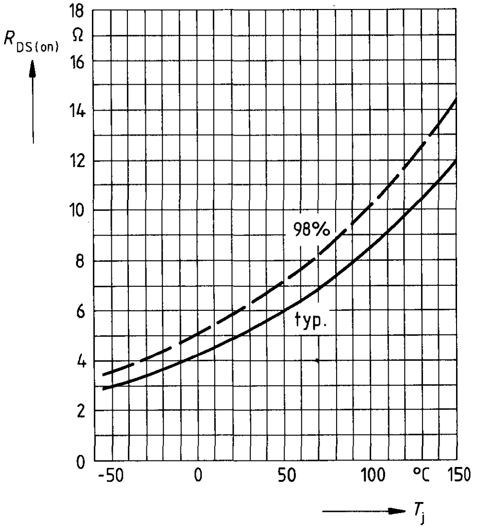
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



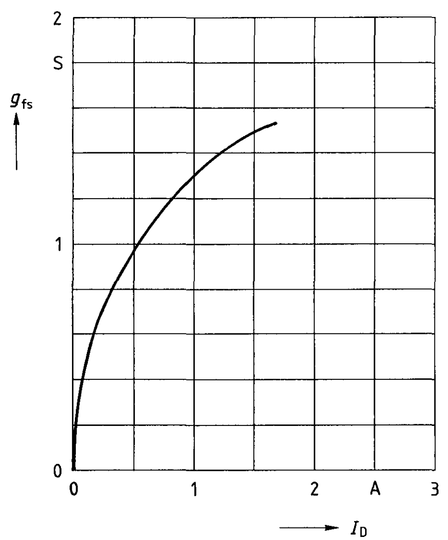
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



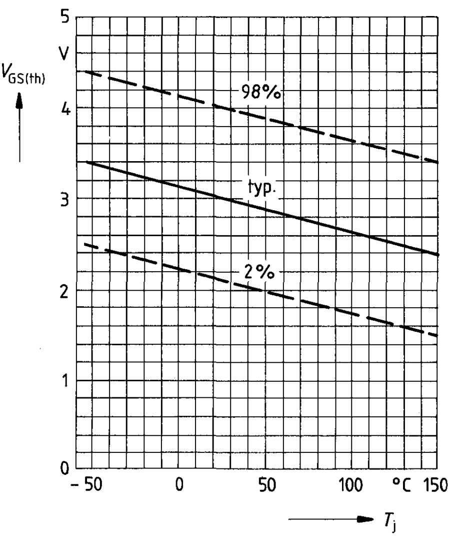
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 1,5A, V_{GS} = 10V
(spread)



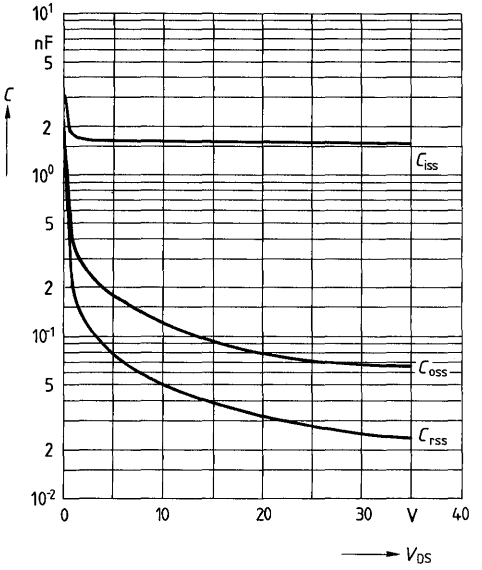
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



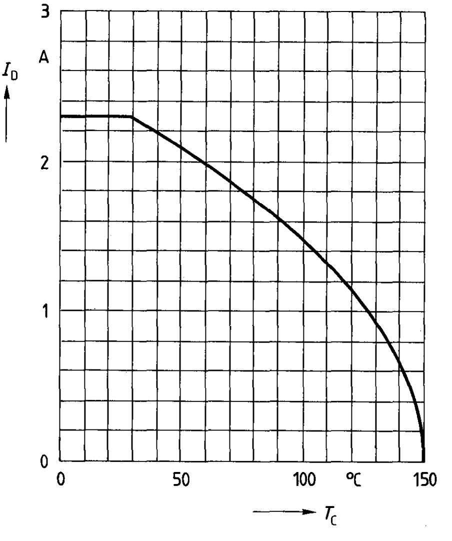
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



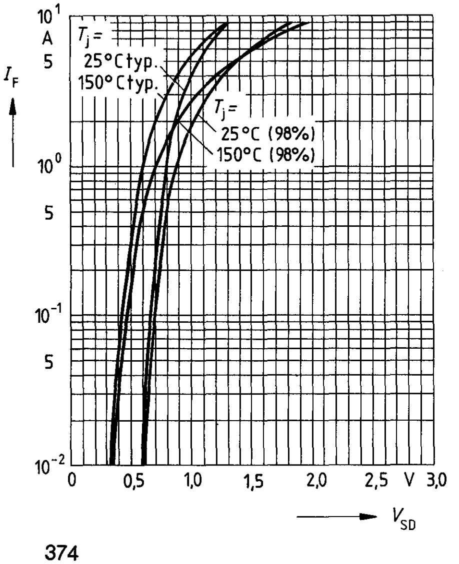
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



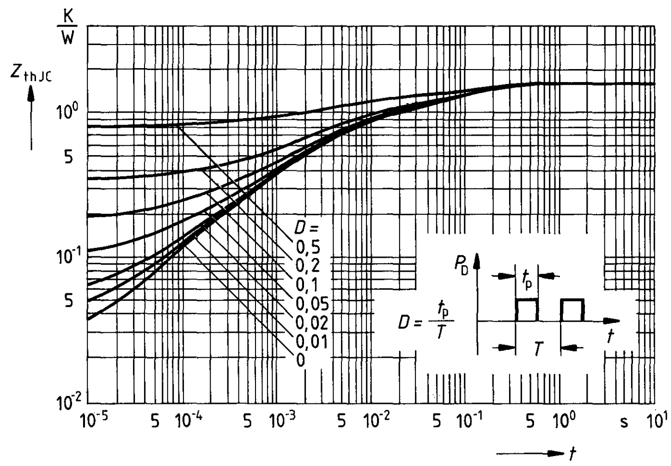
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



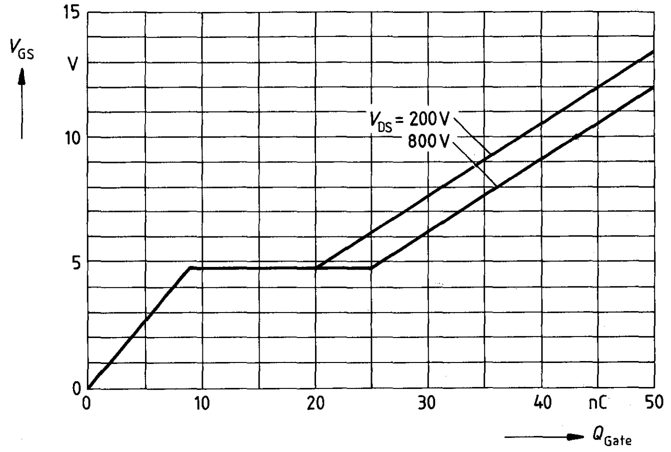
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



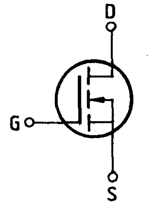
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 3{,}75A$



Main ratings

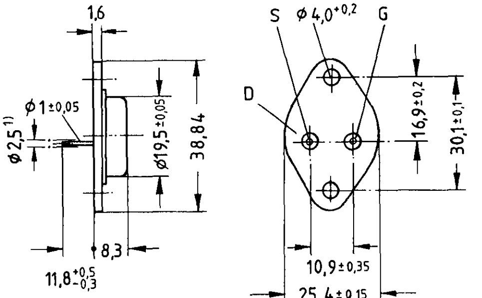
Drain-source voltage V_{DS} = **1000 V**
Continuous drain current I_D = **5,1 A**
Drain-source on-resistance $R_{DS(on)}$ = **2,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3A2 in accordance with DIN 41872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 54	C67078-A1010-A2



1) max. bending area

Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,1	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	20	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j, T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

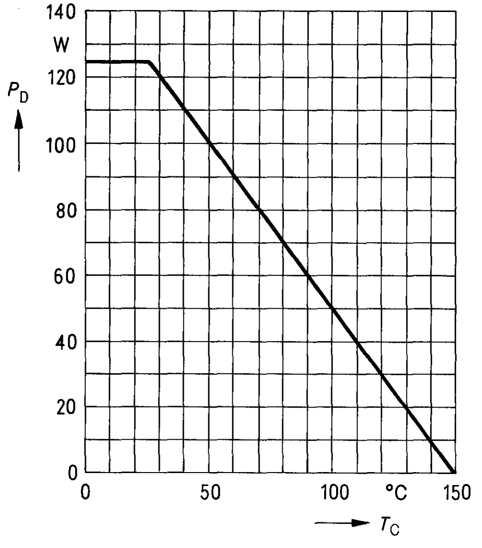
 S Preferred Type

Electrical characteristics

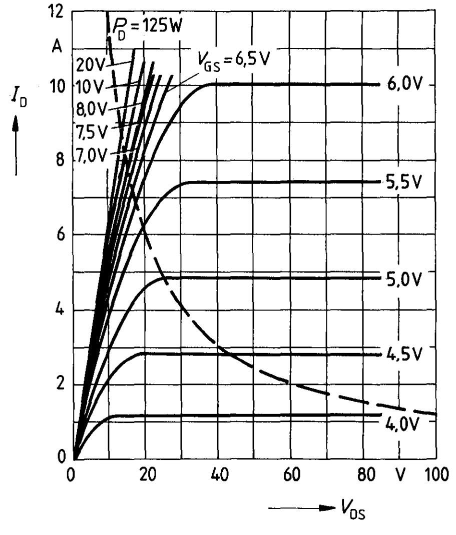
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	1,7	2,0	Ω	V_{GS} = 10V I_D = 2,6A
Dynamic ratings						
Forward transconductance	g_{fs}	1,4	3,5	–	S	V_{DS} = 25V I_D = 2,6A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	300	pF	
Reverse transfer capacitance	C_{rss}	–	70	120		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,1	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	20		
Diode forward on-voltage	V_{SD}	–	1,15	1,4	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	30	–	µC	

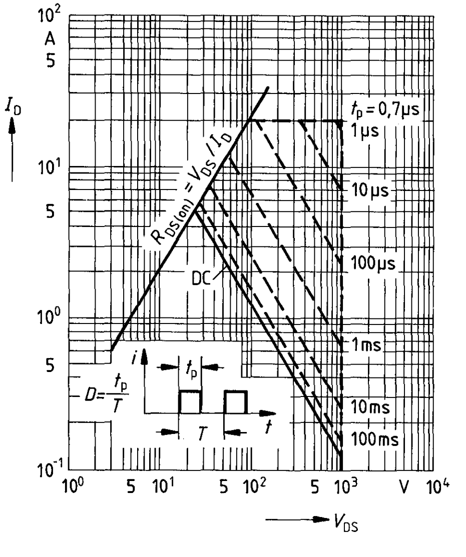
Power dissipation $P_D = f(T_C)$



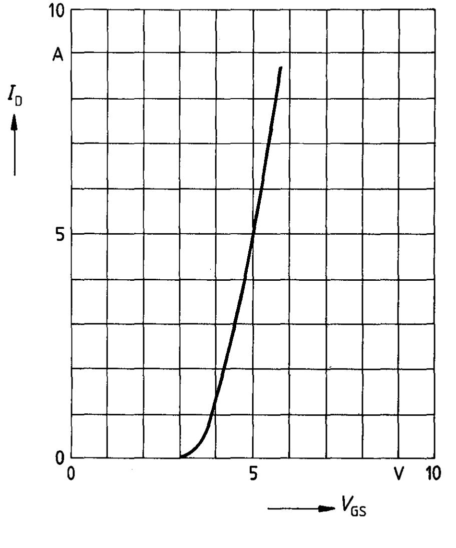
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



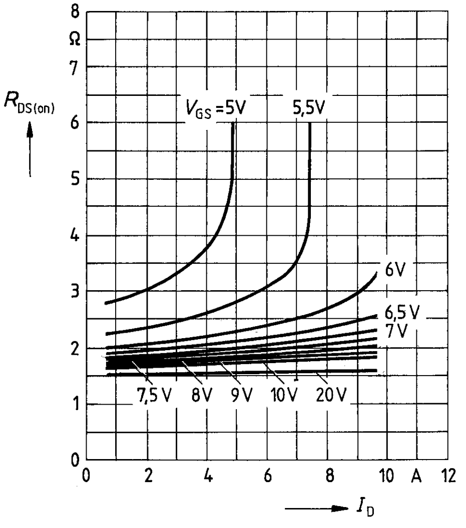
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



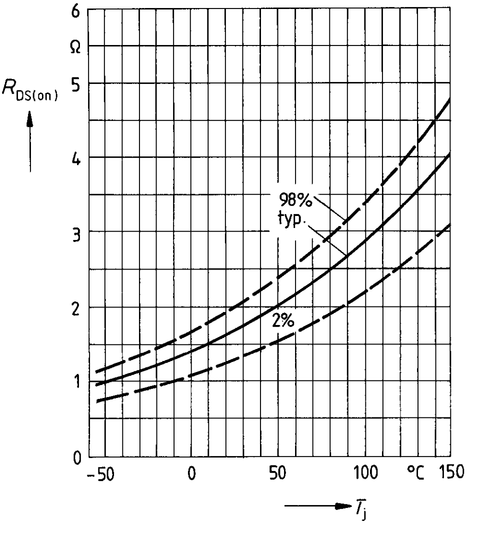
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



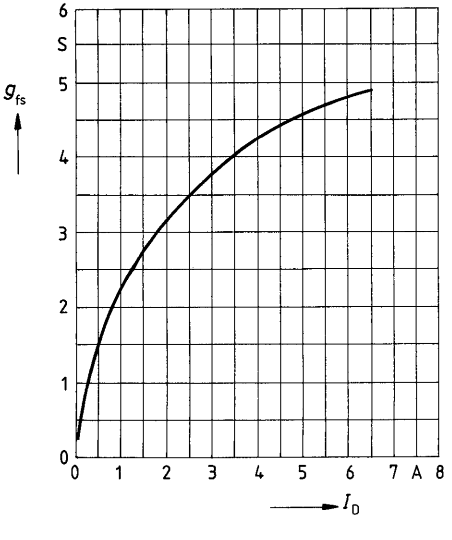
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



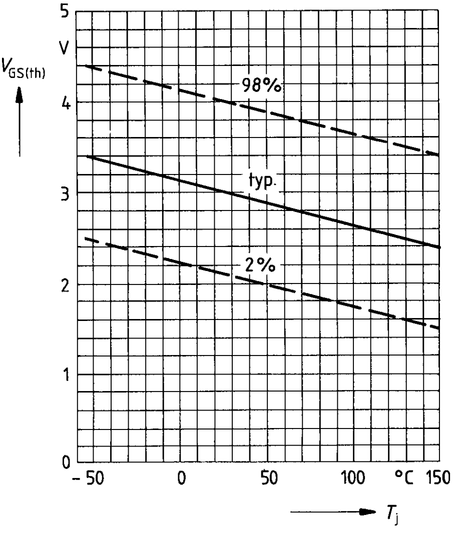
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 2,6A, V_{GS} = 10V
(spread)



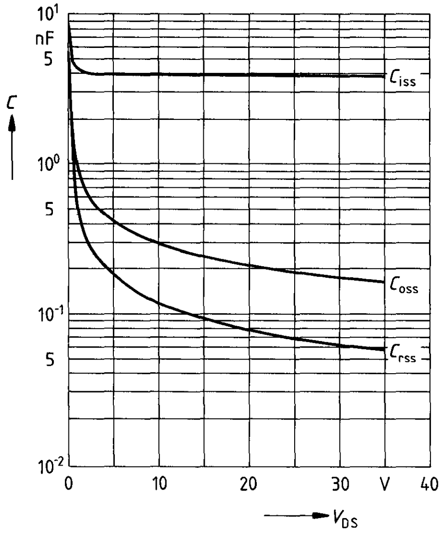
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



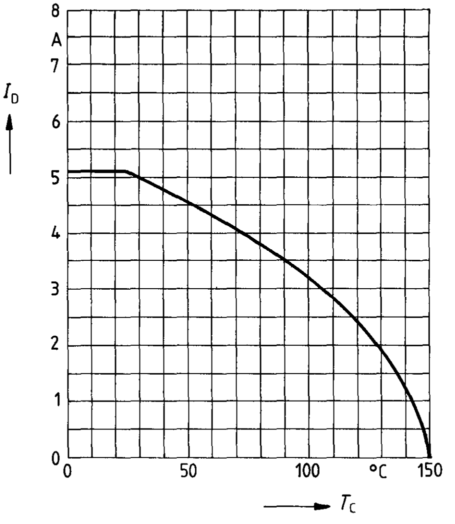
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



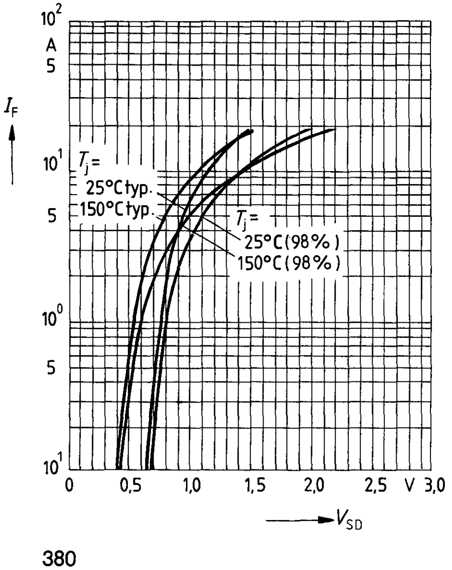
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



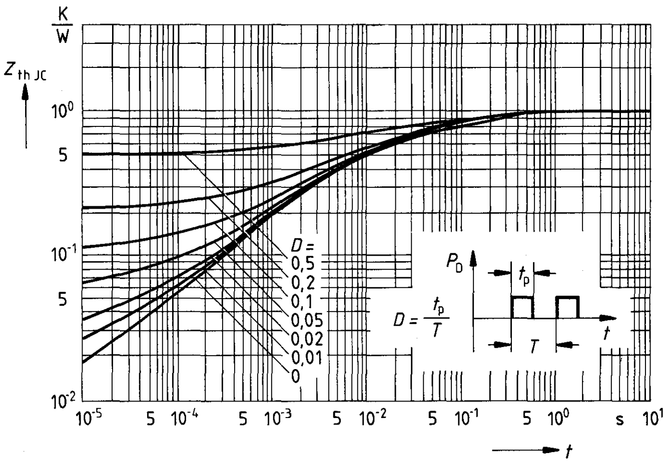
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



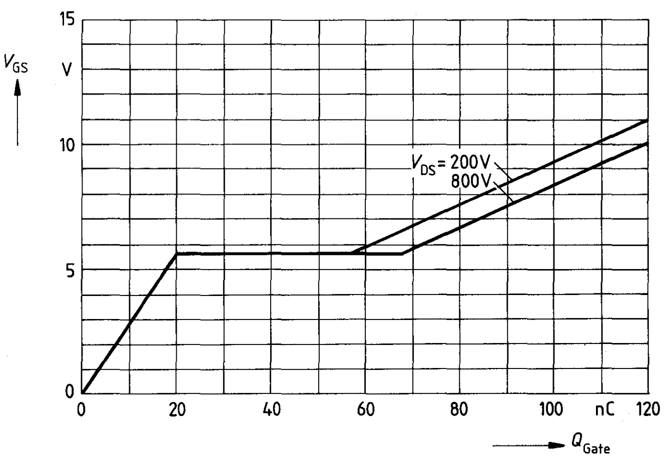
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



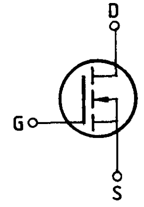
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 8.0$A



Main ratings

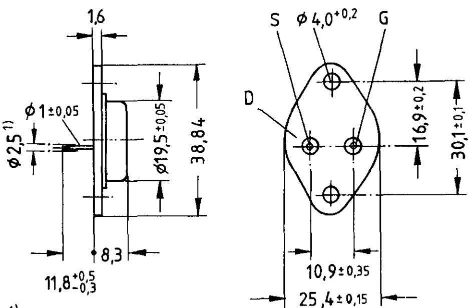
Drain-source voltage V_{DS} **= 1000 V**
Continuous drain current I_D **= 4,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,6 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 54 A	C67078-A1010-A3



1) max. bending area

Dimensions in mm

Maximum ratings

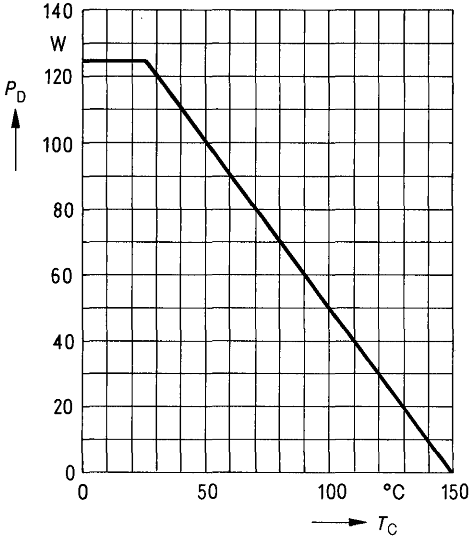
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	18	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤ 35	K/W	

 S Preferred Type

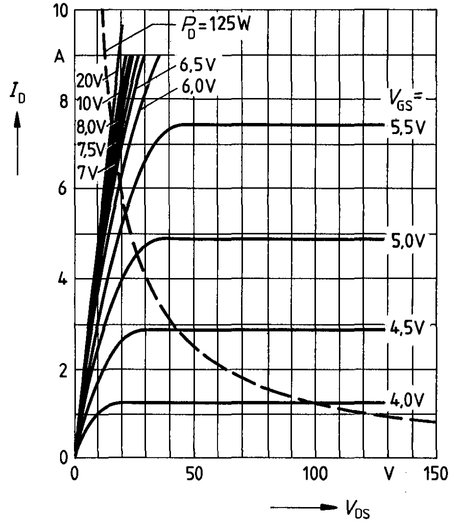
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	2,3	2,6	Ω	V_{GS} = 10V I_D = 2,6A
Dynamic ratings						
Forward transconductance	g_{fs}	1,4	3,5	–	S	V_{DS} = 25V I_D = 2,6A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	300	pF	
Reverse transfer capacitance	C_{rss}	–	60	90		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,4A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	18		
Diode forward on-voltage	V_{SD}	–	1,5	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	30	–	µC	

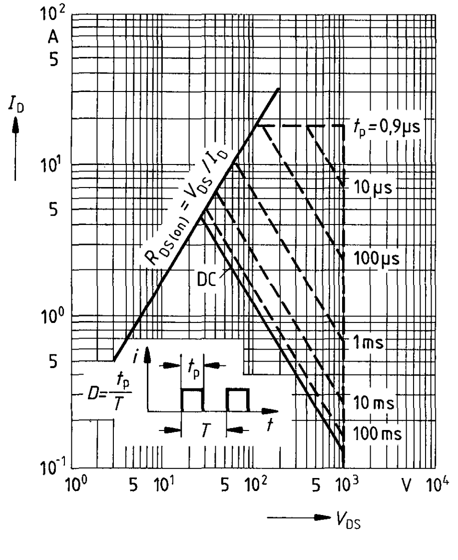
Power dissipation $P_D = f(T_C)$



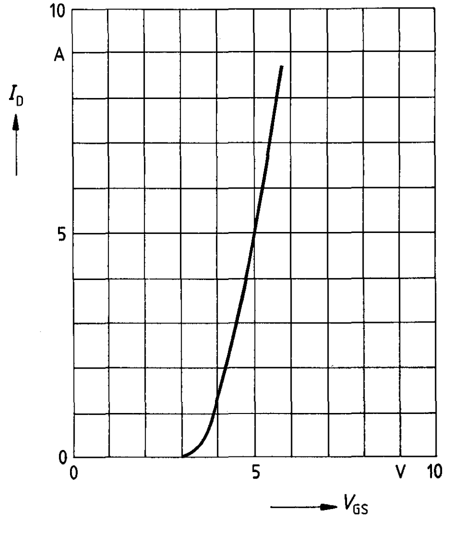
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



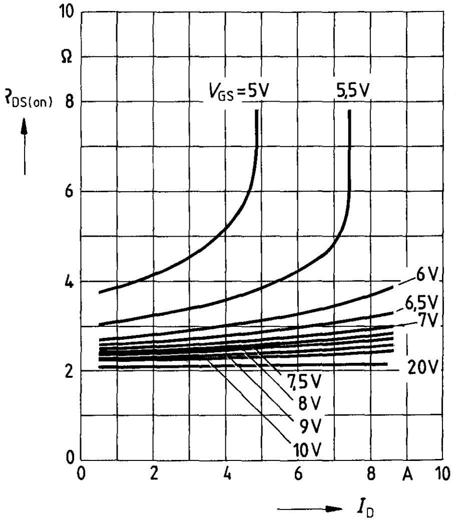
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



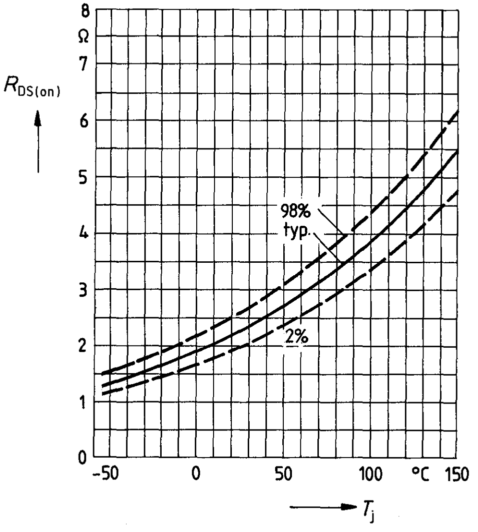
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



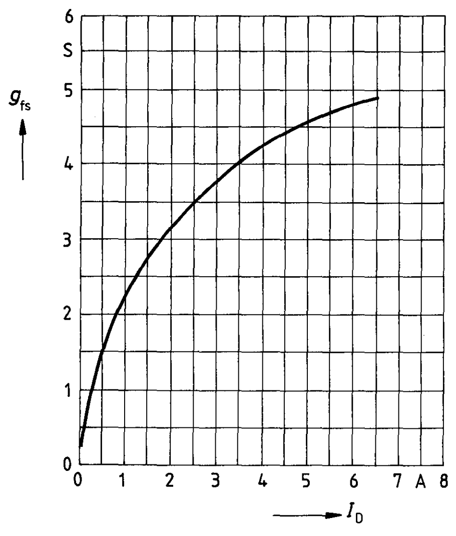
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



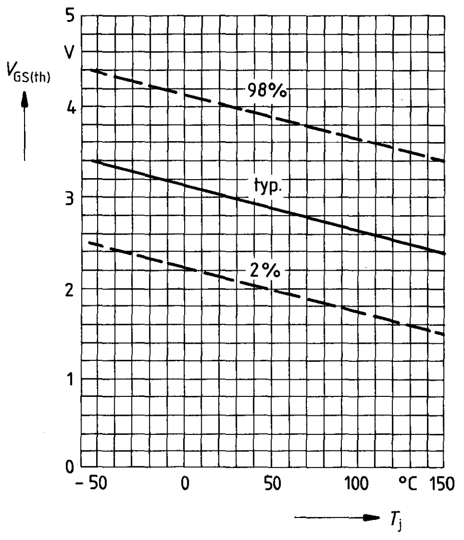
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 2{,}6A$, $V_{GS} = 10V$
(spread)



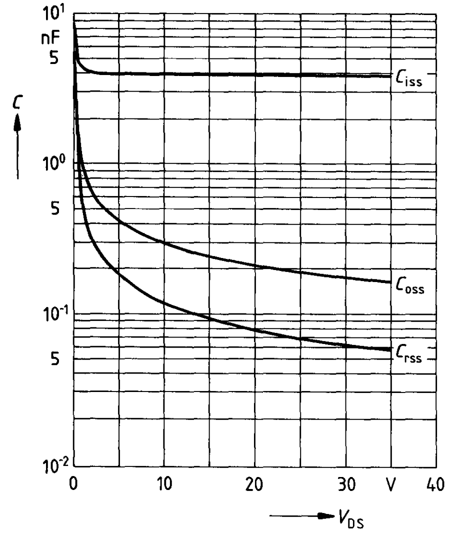
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



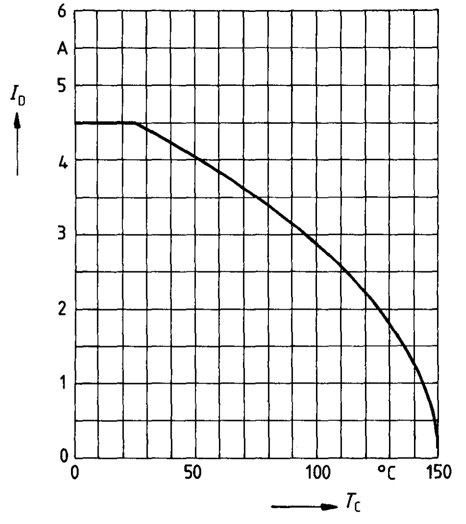
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



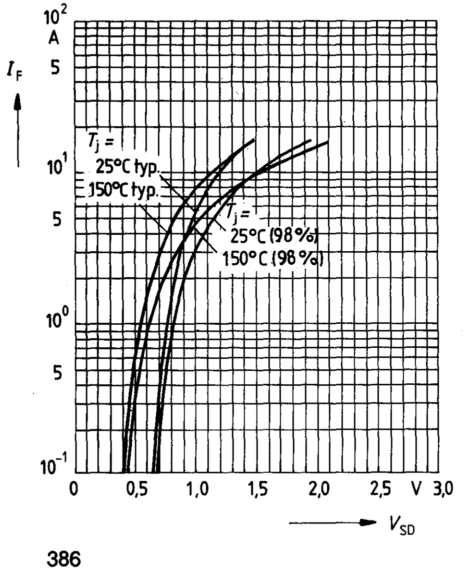
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



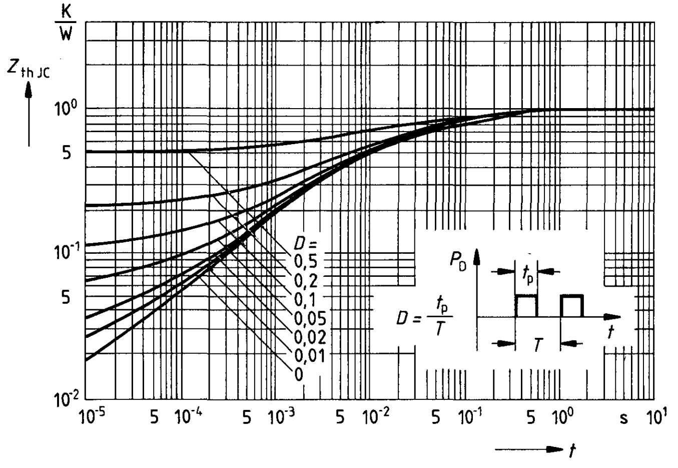
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



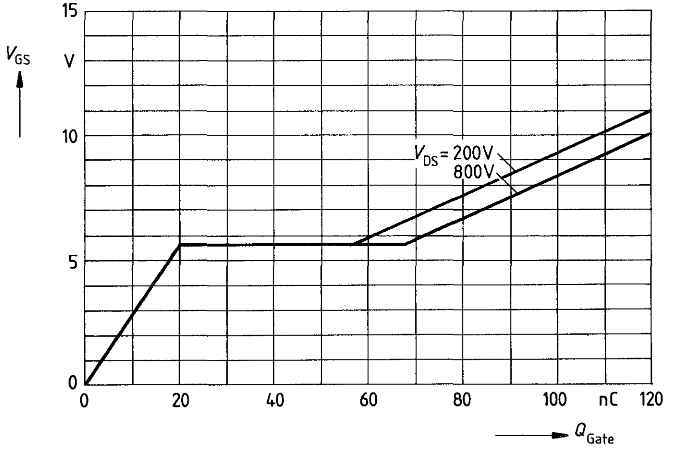
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



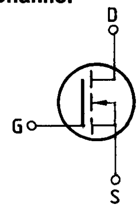
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 8A$



Main ratings

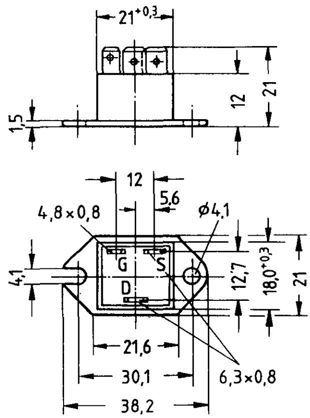
Drain-source voltage V_{DS} **= 1000 V**
Continuous drain current I_D **= 4,2 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
S BUZ 58	C67078-A1607-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,2	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	17	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 ... +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,5	K/W	

[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

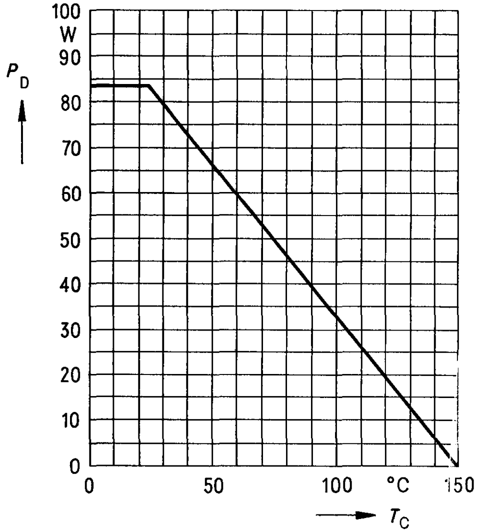
 S Preferred Type

Electrical characteristics

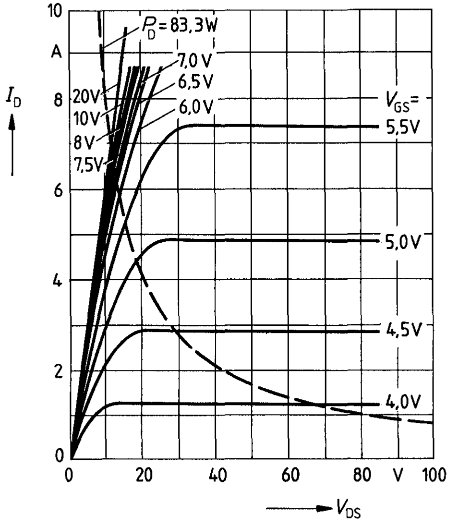
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,7	2,0	Ω	V_{GS} = 10V I_D = 2,6A
Dynamic ratings						
Forward transconductance	g_{fs}	1,4	3,5	–	S	V_{DS} = 25V I_D = 2,6A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	300	pF	
Reverse transfer capacitance	C_{rss}	–	70	120		
Turn-on time t_{on} (t_{on} = $t_{d\,(on)}$ + t_r)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} (t_{off} = $t_{d\,(off)}$ + t_f)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,2	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	17		
Diode forward on-voltage	V_{SD}	–	1,1	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25°C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	30	–	µC	

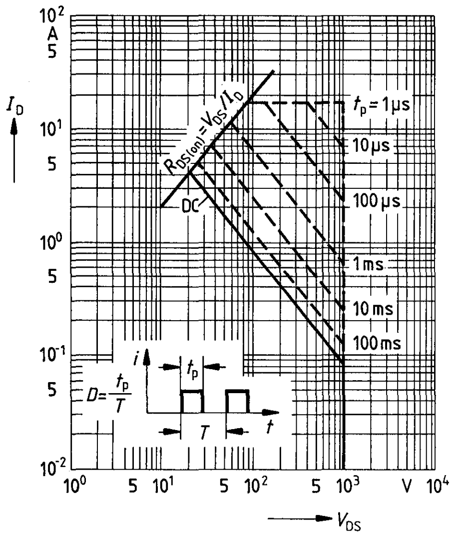
Power dissipation $P_D = f(T_C)$



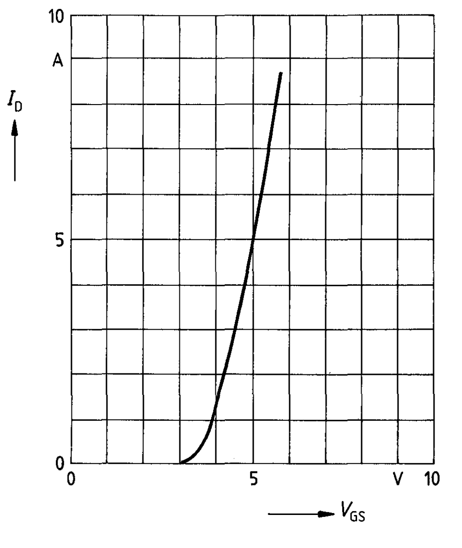
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



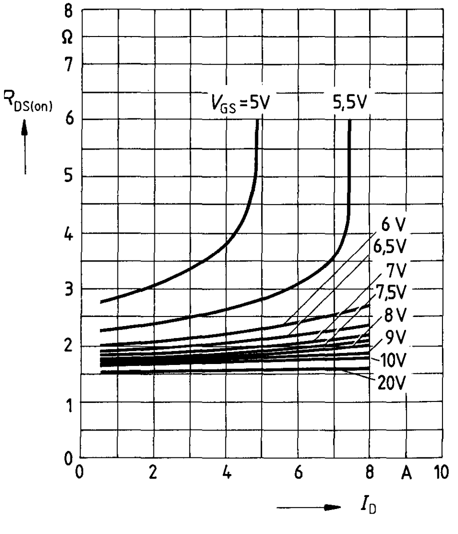
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



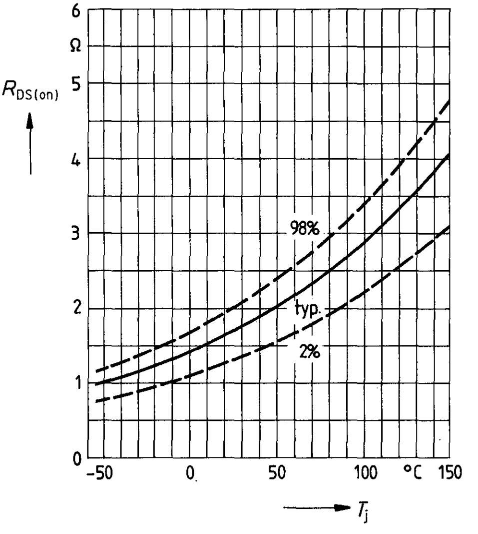
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



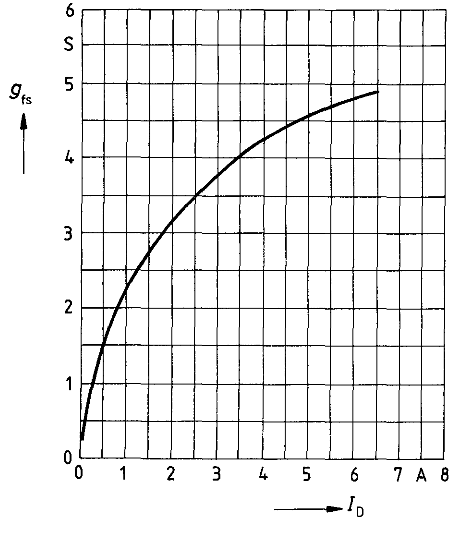
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



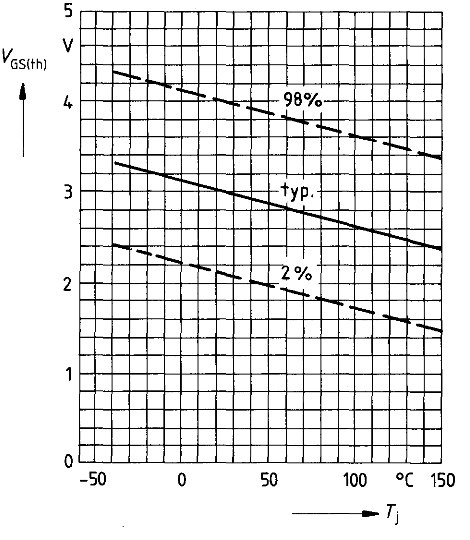
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 2,6A, V_{GS} = 10V
(spread)



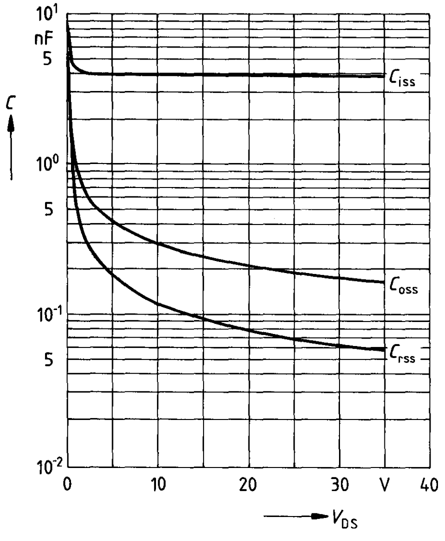
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



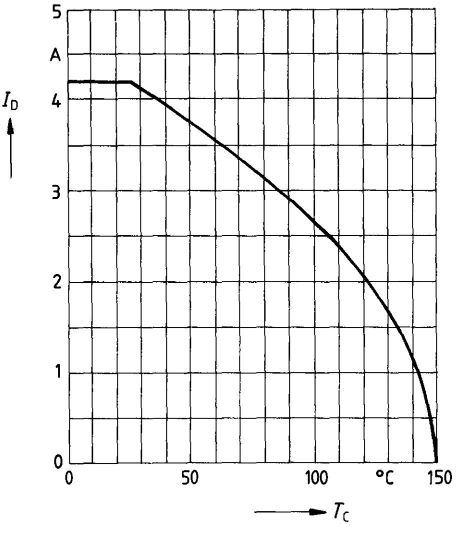
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



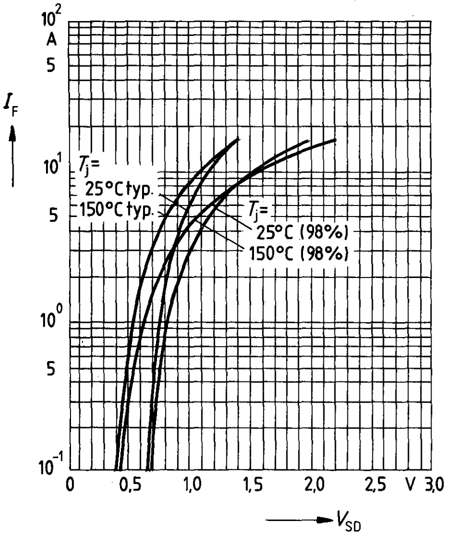
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



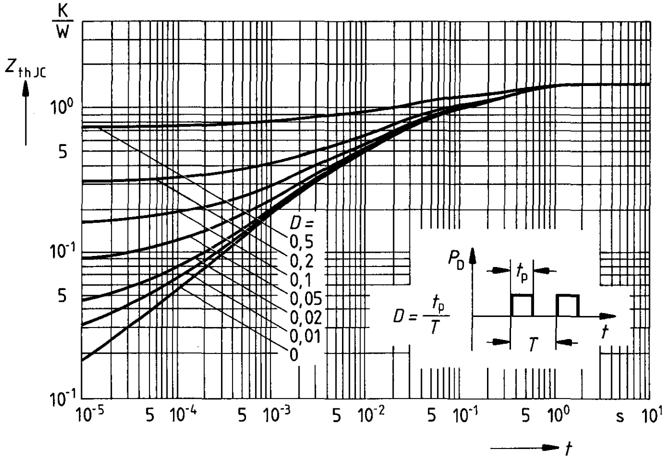
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



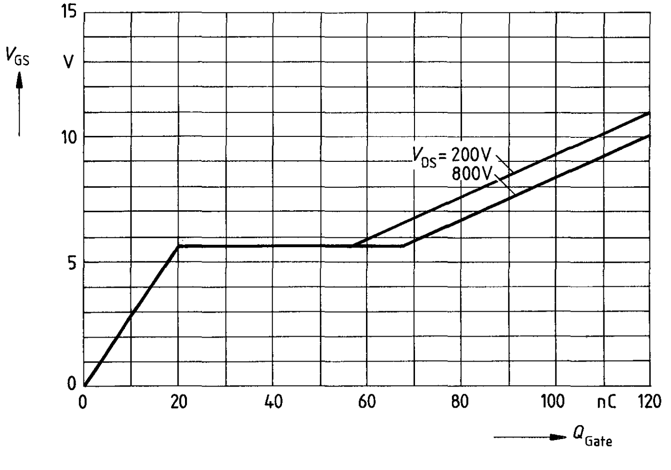
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



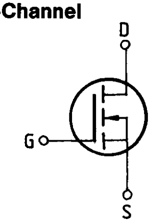
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 8.0A$



Main ratings

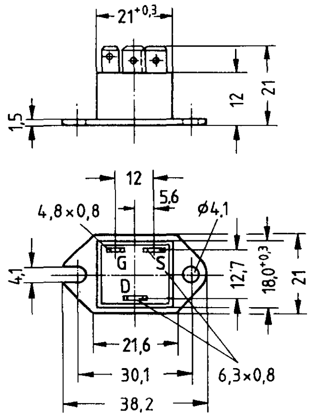
Drain-source voltage V_{DS} **= 1000 V**
Continuous drain current I_D **= 3,6 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,6 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 58 A	C67078-A1607-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	3,6	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	14	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40… +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	R_{thJC}	≤1,5	K/W	

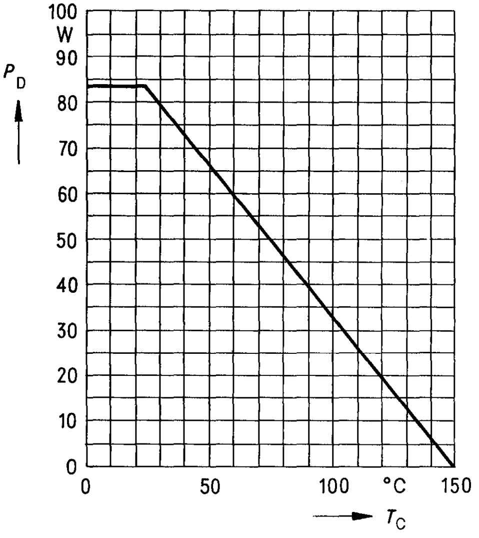
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

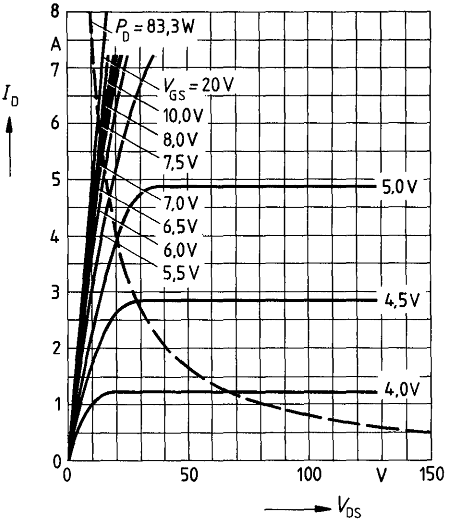
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	2,3	2,6	Ω	V_{GS} = 10V I_D = 2,6A
Dynamic ratings						
Forward transconductance	g_{fs}	1,4	3,5	–	S	V_{DS} = 25V I_D = 2,6A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	300	pF	
Reverse transfer capacitance	C_{rss}	–	70	120		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,4A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	3,6	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	14		
Diode forward on-voltage	V_{SD}	–	1,1	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	30	–	µC	

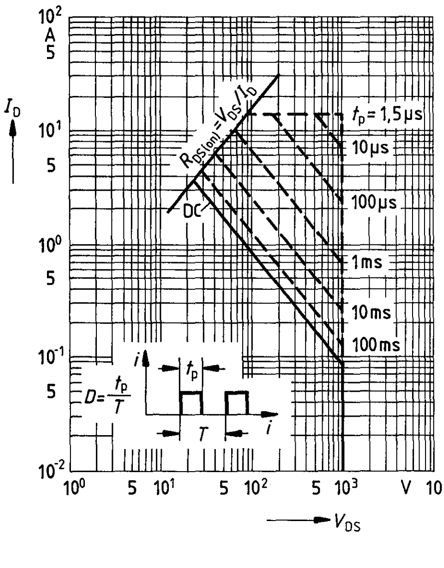
Power dissipation $P_D = f(T_C)$



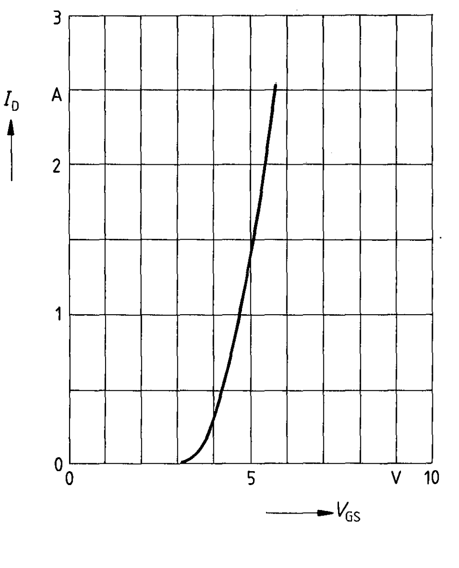
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



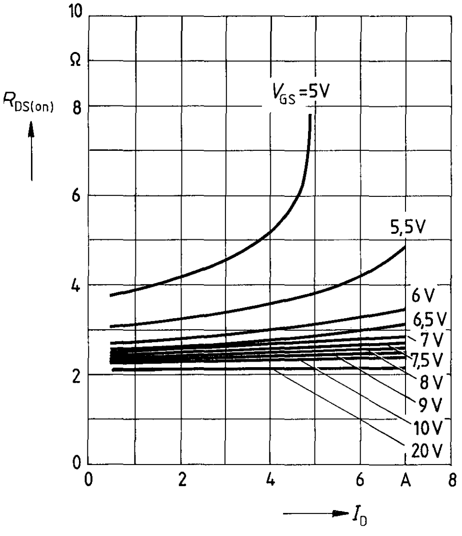
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



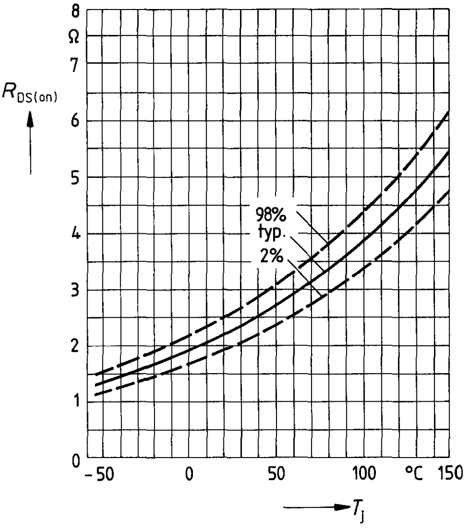
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



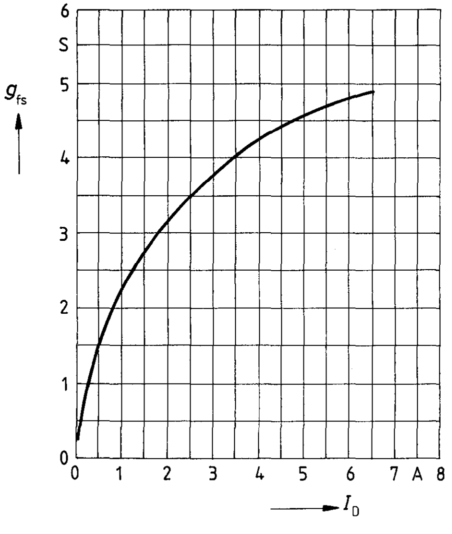
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



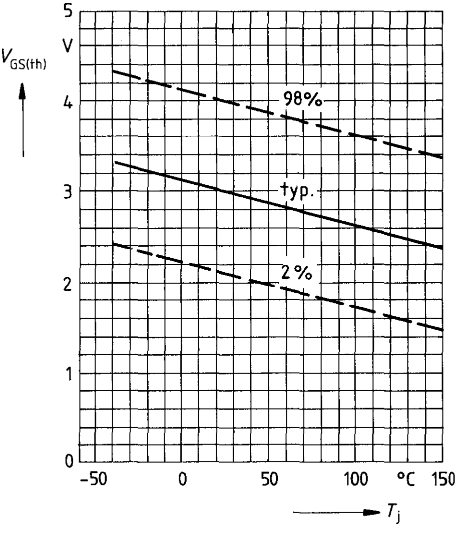
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 2{,}6A$, $V_{GS} = 10V$
(spread)



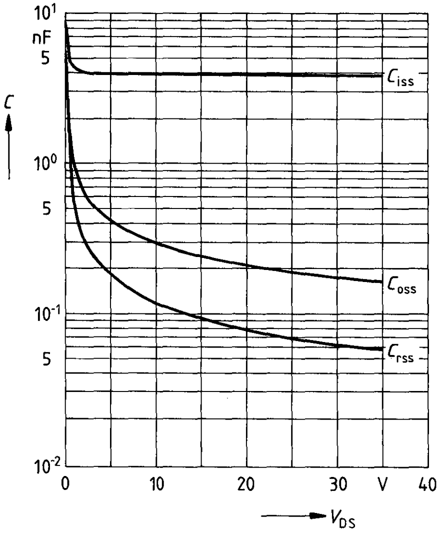
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



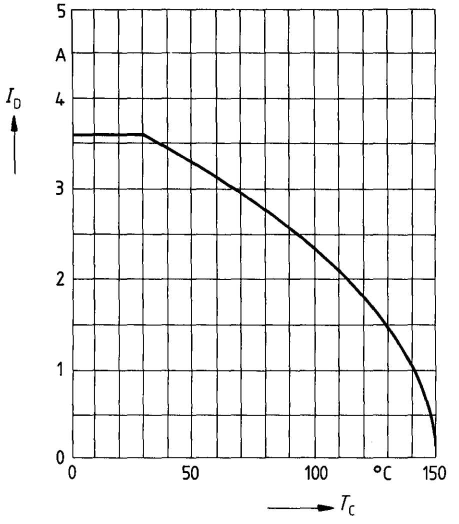
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



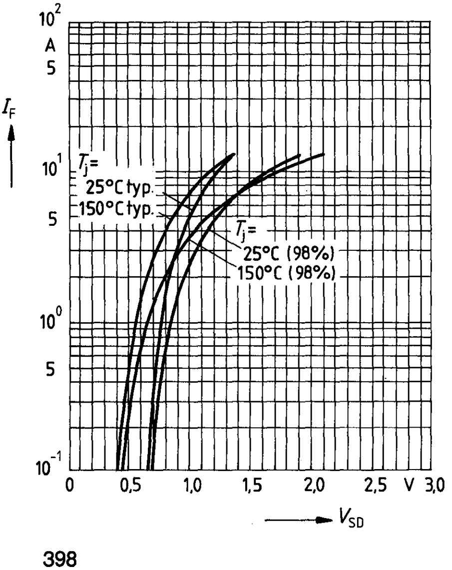
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



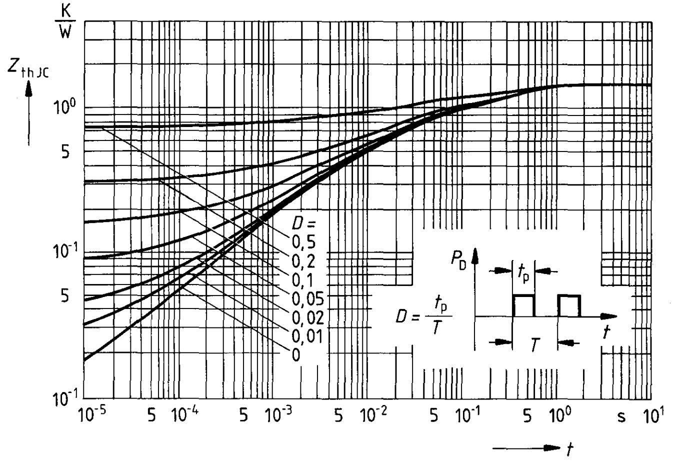
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



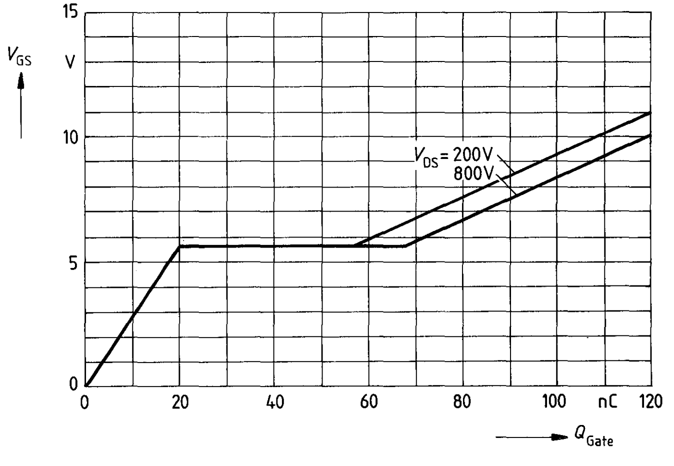
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

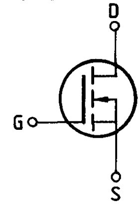


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 8A$



Main ratings

N-Channel

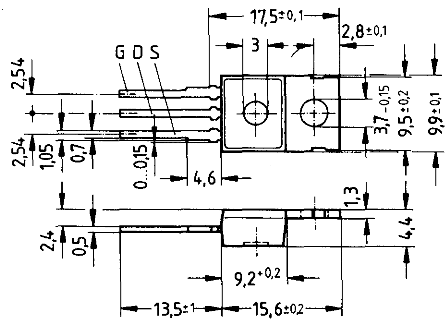


Drain-source voltage	V_{DS}	**= 400 V**
Continuous drain current	I_D	**= 5,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 1,0 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
S BUZ 60	C67078-A1312-A2



Dimensions in mm

Maximum ratings

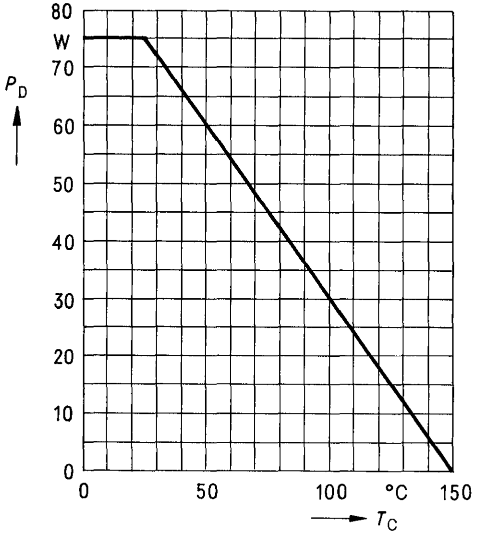
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,5	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	22	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

 S Preferred Type

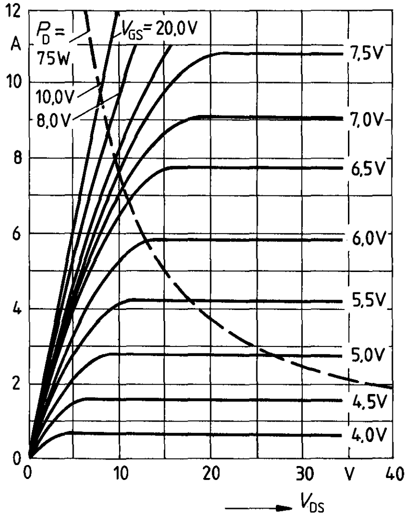
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,9	1,0	Ω	V_{GS} = 10V I_D = 2,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,7	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	120	180	pF	
Reverse transfer capacitance	C_{rss}	–	35	60		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,7A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	22		
Diode forward on-voltage	V_{SD}	–	1,15	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	5	–	µC	

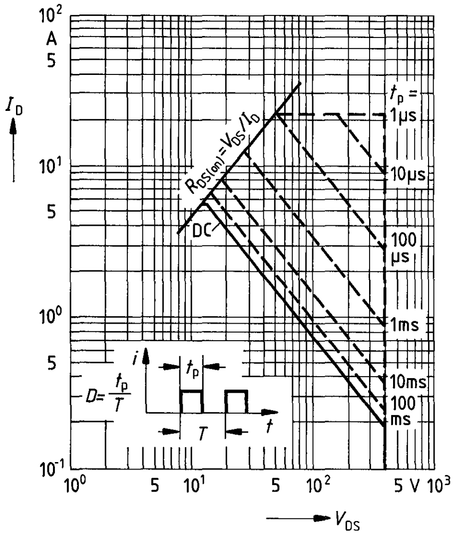
Power dissipation $P_D = f(T_C)$



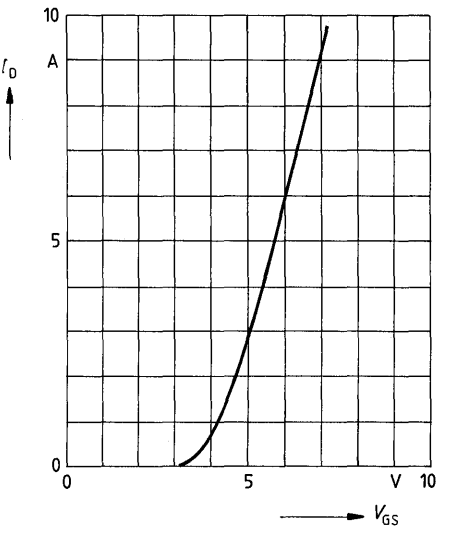
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



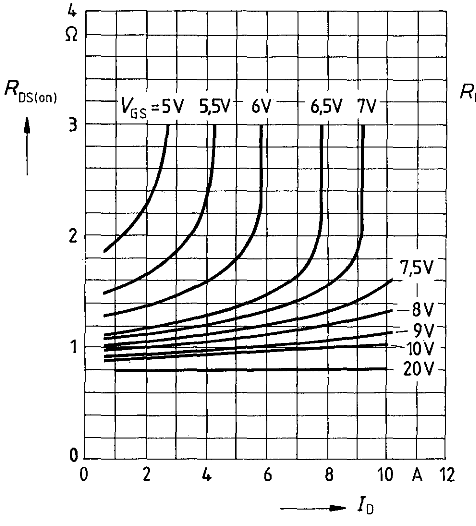
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



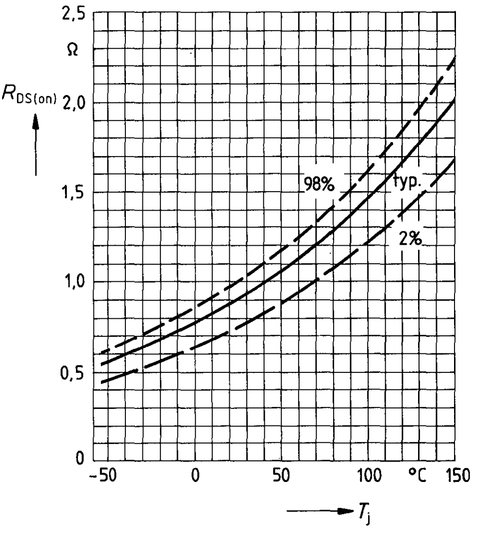
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



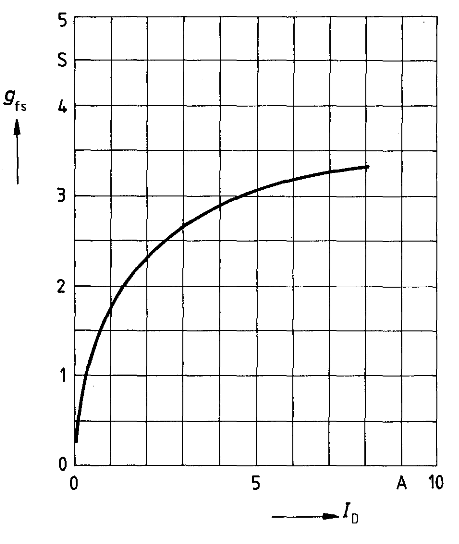
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



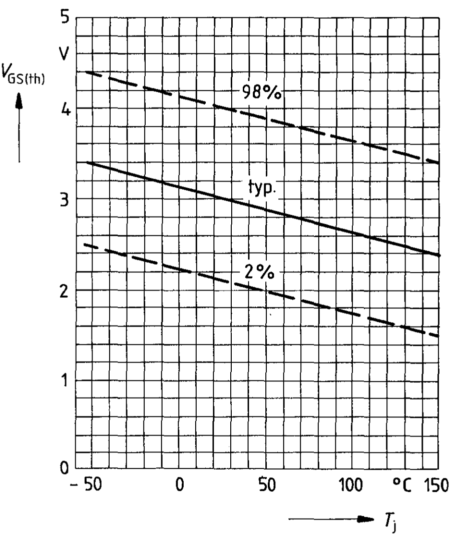
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 2{,}5A$, $V_{GS} = 10V$
(spread)



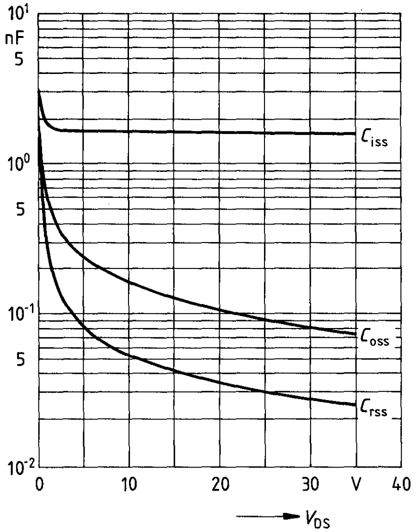
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



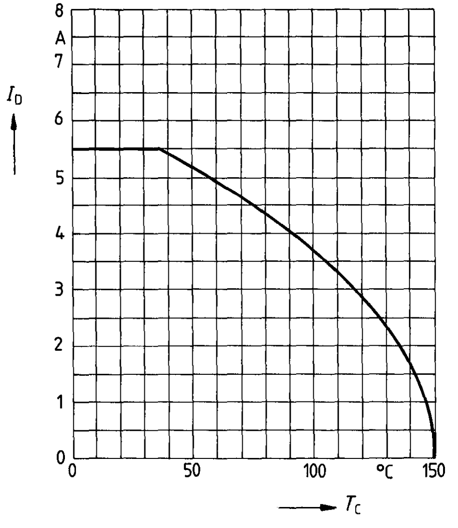
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



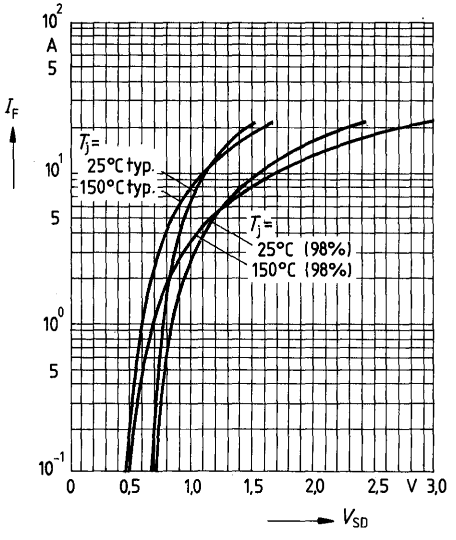
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



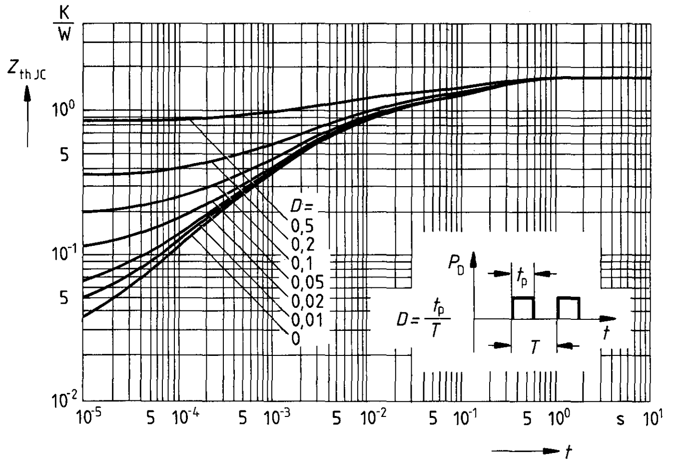
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



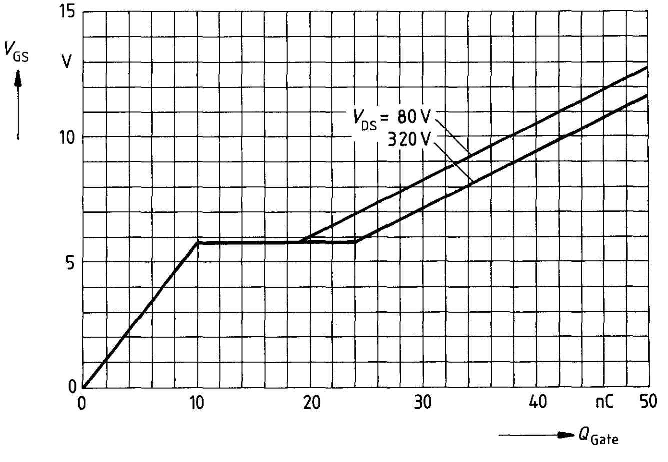
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



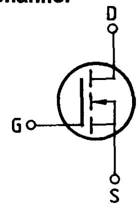
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 8{,}3A$



Main ratings

Drain-source voltage V_{DS} **= 400 V**
Continuous drain current I_D **= 4,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 1,5 Ω**

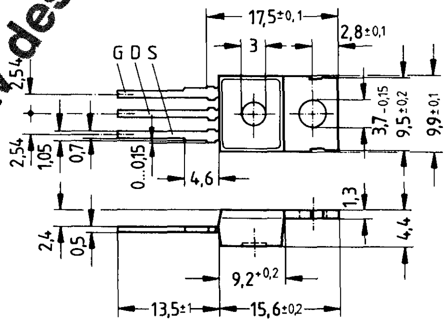
N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 60 B	C67078-A1312-A4

Not for new design



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,5	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	18	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤1,67	K/W	
Chip – ambient	$R_{th JA}$	≤75	K/W	

 S Preferred Type

Electrical characteristics

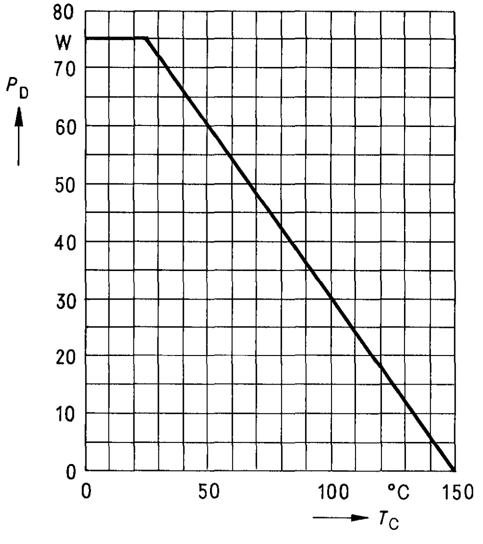
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,2	1,5	Ω	V_{GS} = 10V I_D = 2,5A

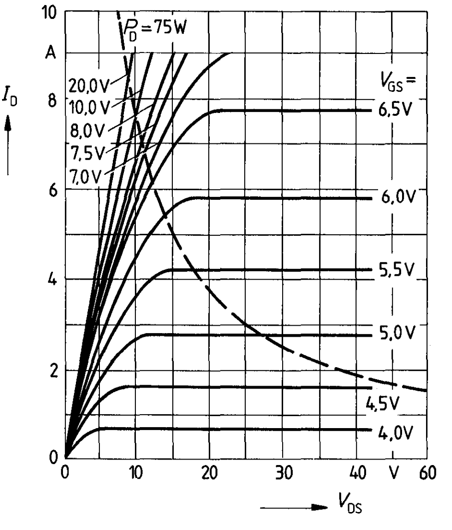
Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Dynamic ratings						
Forward transconductance	g_{fs}	1,7	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	120	180	pF	
Reverse transfer capacitance	C_{rss}	–	35	60		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Reverse diode						
Continuous reverse drain current	I_{DR}	–	1,7	4,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	18		
Diode forward on-voltage	V_{SD}	–	1,15	1,50	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	5	–	µC	

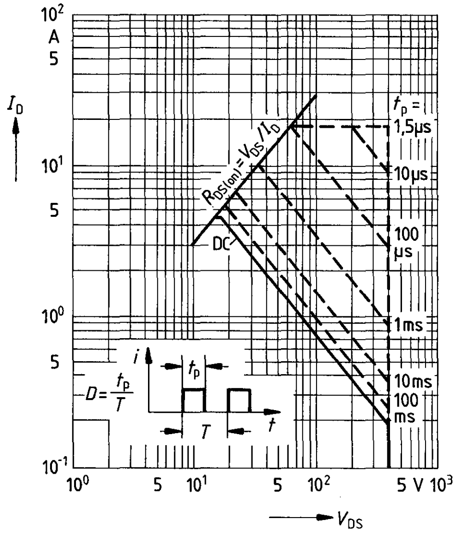
Power dissipation $P_D = f(T_C)$



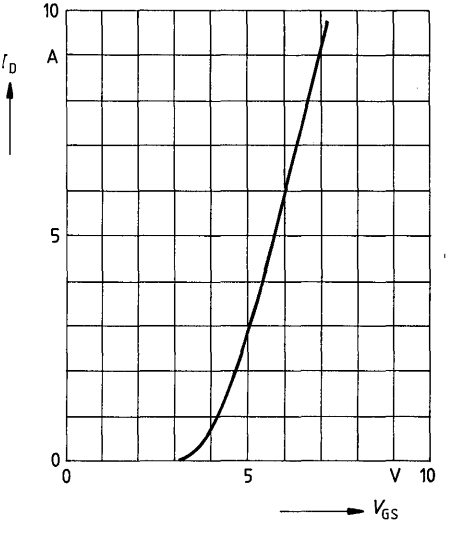
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



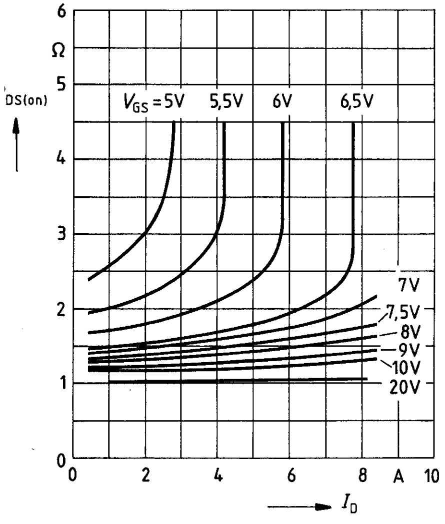
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



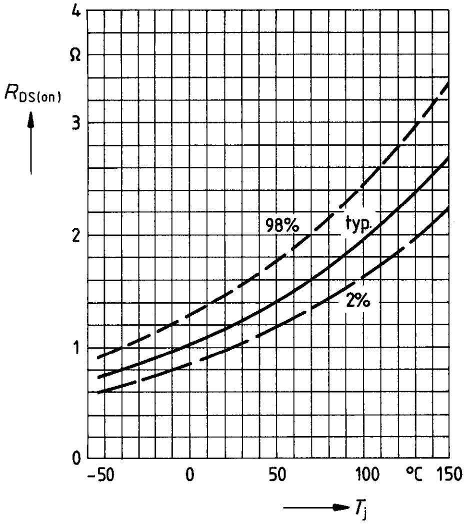
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



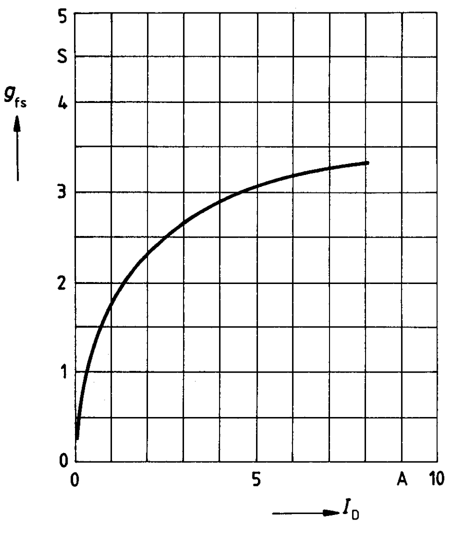
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



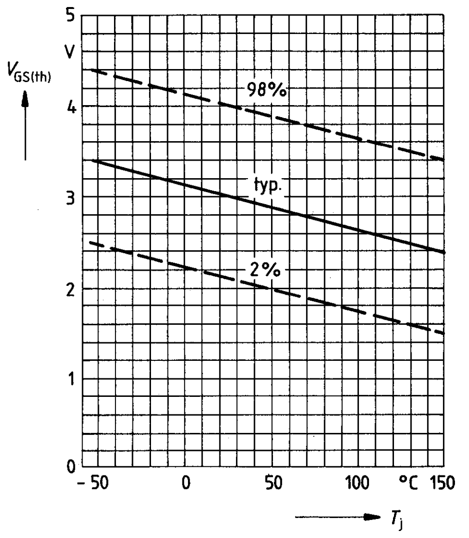
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 2,5A, V_{GS} = 10V
(spread)



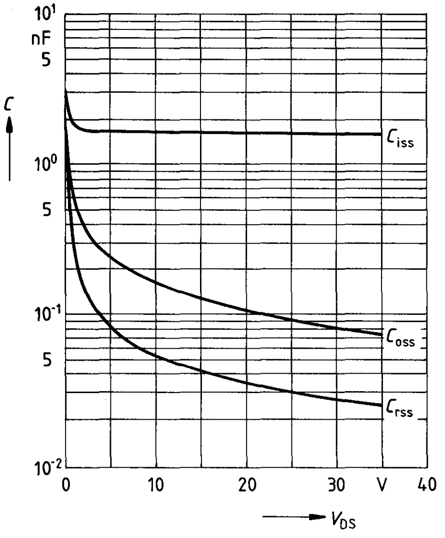
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



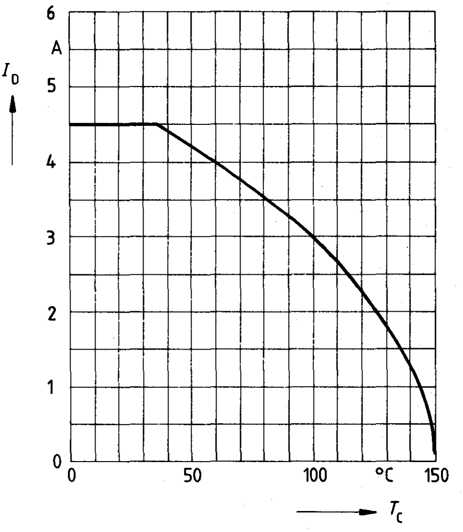
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



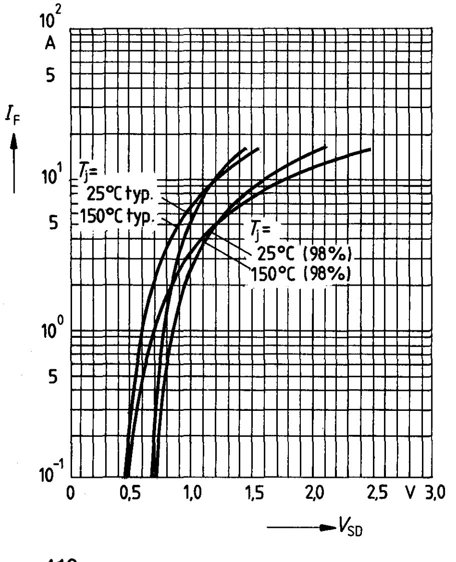
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



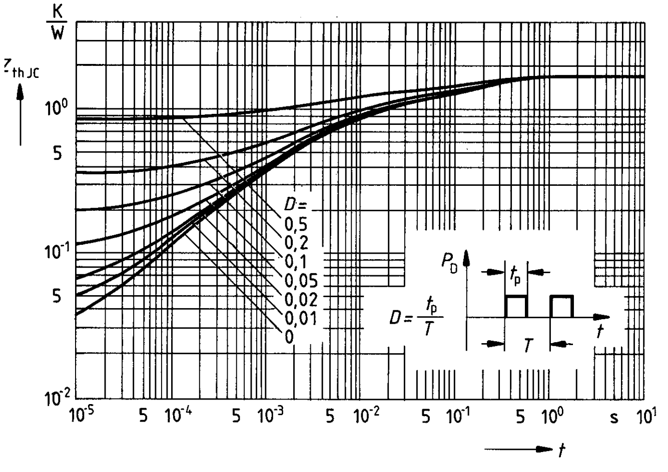
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



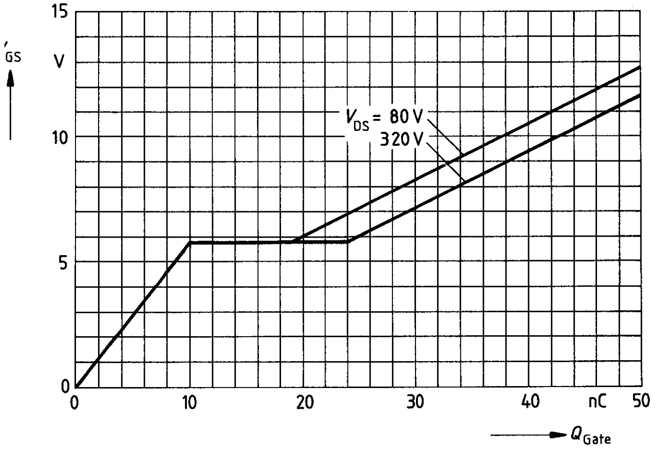
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



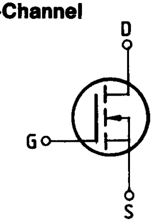
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 8{,}3A$



Main ratings

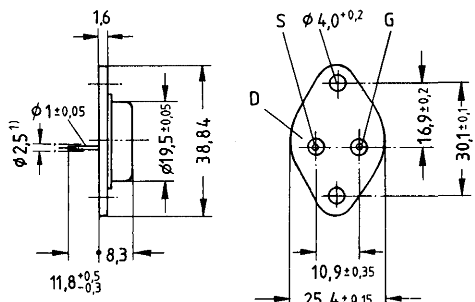
Drain-source voltage V_{DS} **= 400 V**
Continuous drain current I_D **= 5,9 A**
Drain-source on-resistance $R_{DS(on)}$ **= 1,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 63	C67078-A1016-A2



1) max. bending area

Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,9	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	23	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 … +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,6	K/W	
Chip – ambient	$R_{th\ JA}$	≤35	K/W	

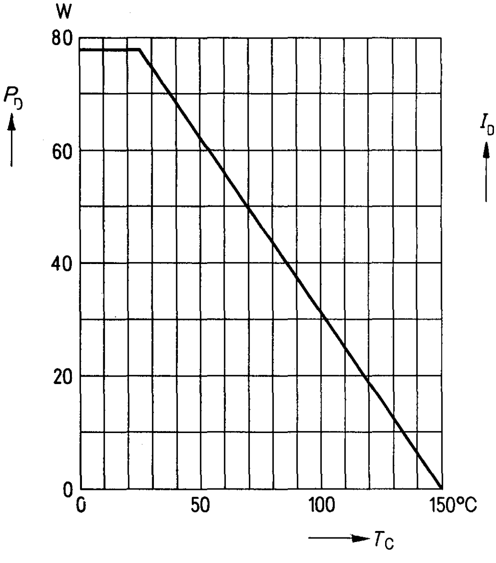
 S Preferred Type

Electrical characteristics

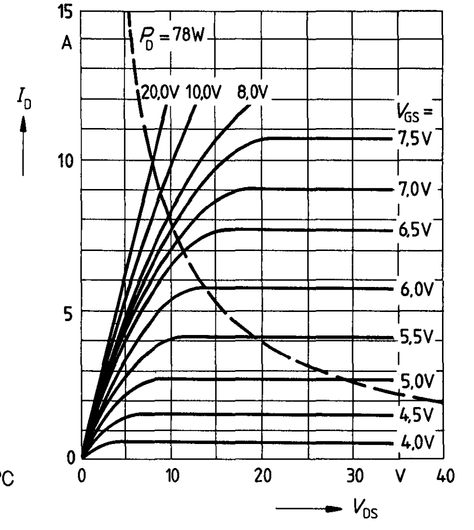
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,9	1,0	Ω	V_{GS} = 10V I_D = 2,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,7	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	120	180	pF	
Reverse transfer capacitance	C_{rss}	–	35	60		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,7A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,9	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	23		
Diode forward on-voltage	V_{SD}	–	1,2	1,65	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	5	–	µC	

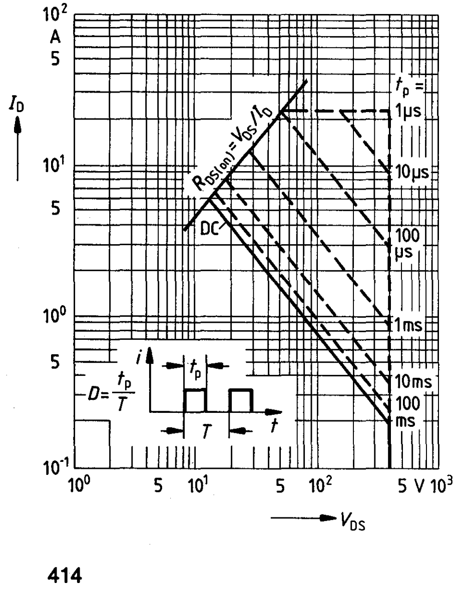
Power dissipation $P_D = f(T_C)$



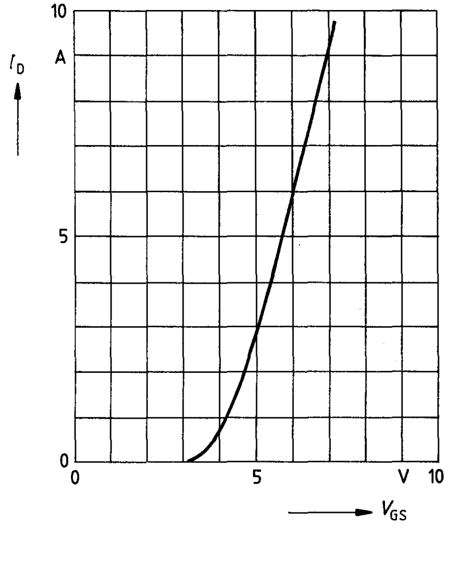
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



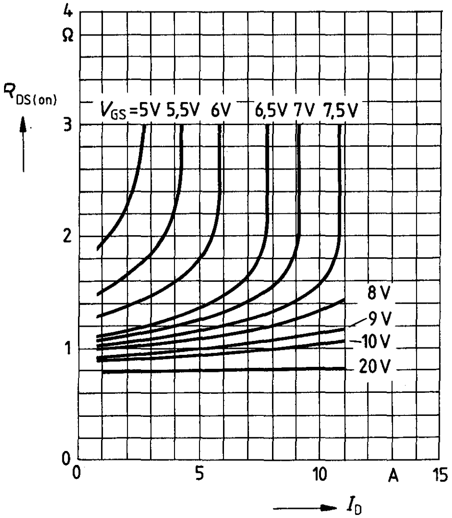
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



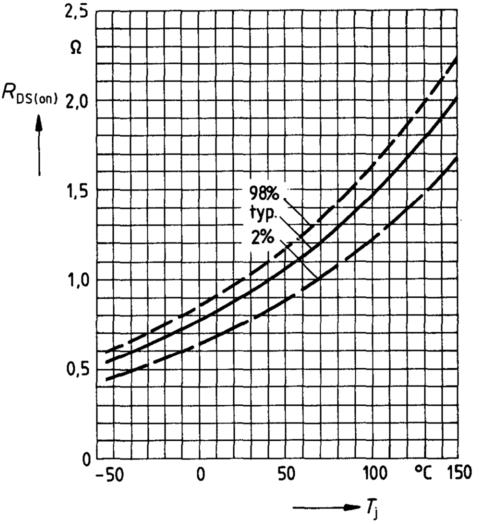
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



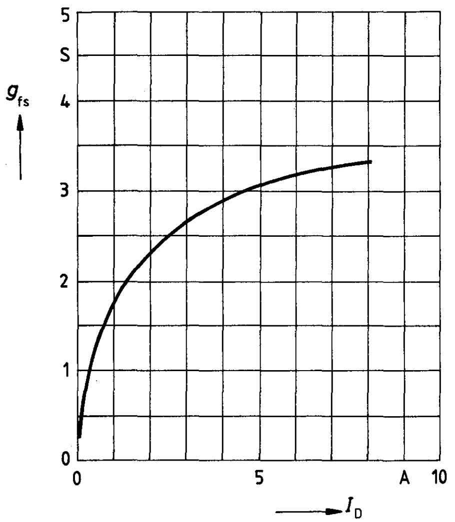
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



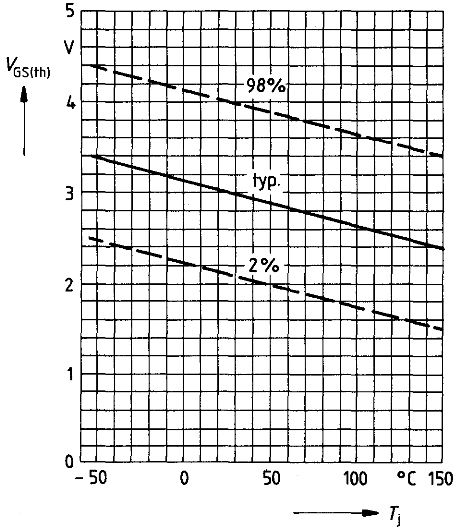
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 2,5A, V_{GS} = 10V
(spread)



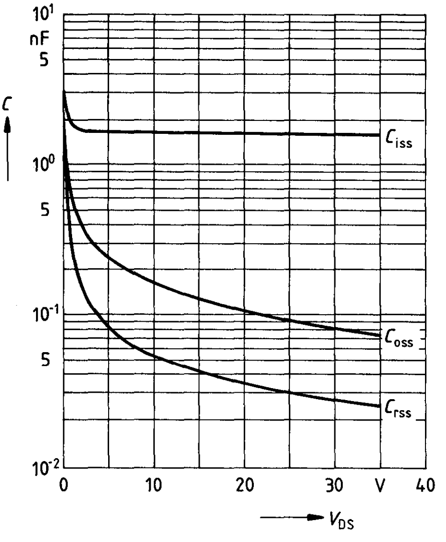
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



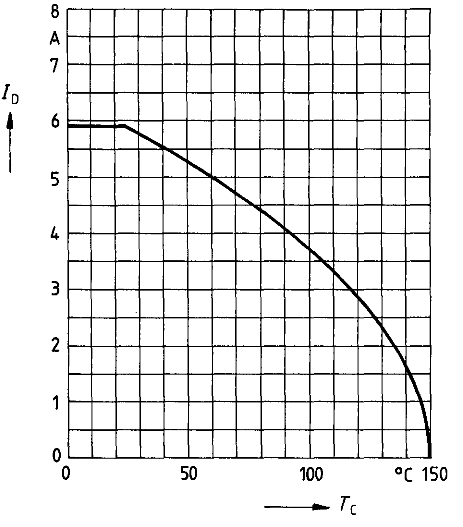
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



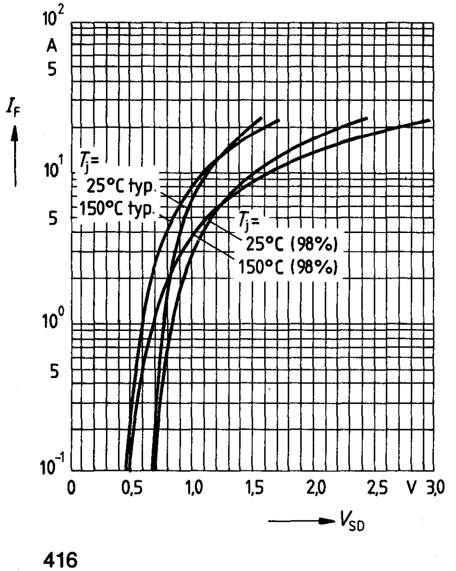
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



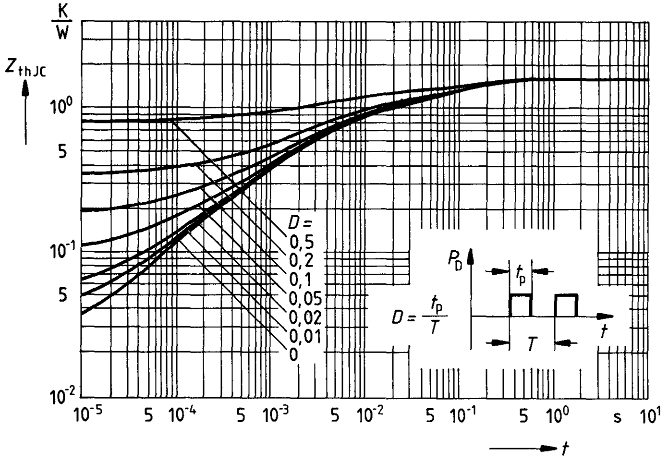
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



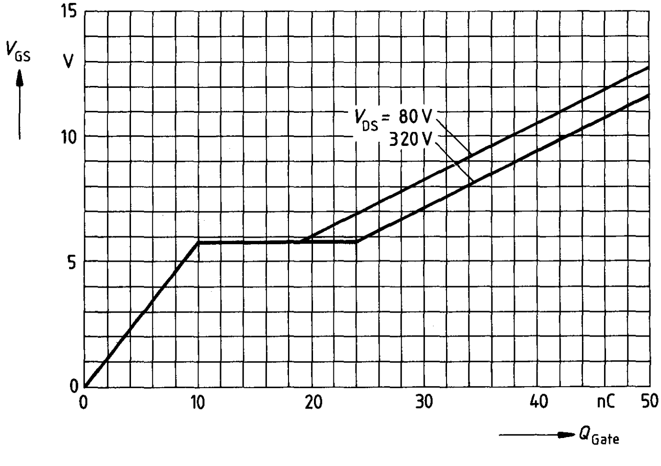
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



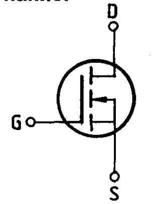
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 8{,}3A$



Main ratings

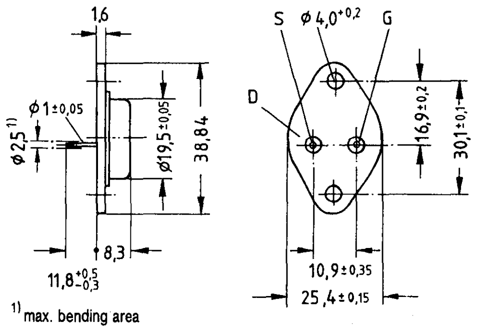
Drain-source voltage V_{DS} = **400 V**
Continuous drain current I_D = **11,5 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,4 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 64	C67078-A1017-A2



Dimensions in mm

Maximum ratings

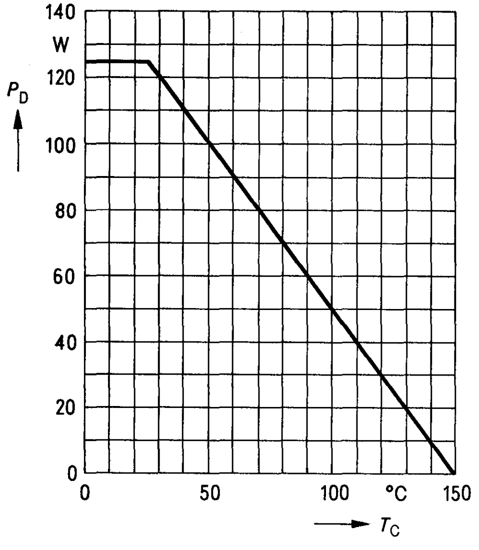
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	11,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	46	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤35	K/W	

Electrical characteristics

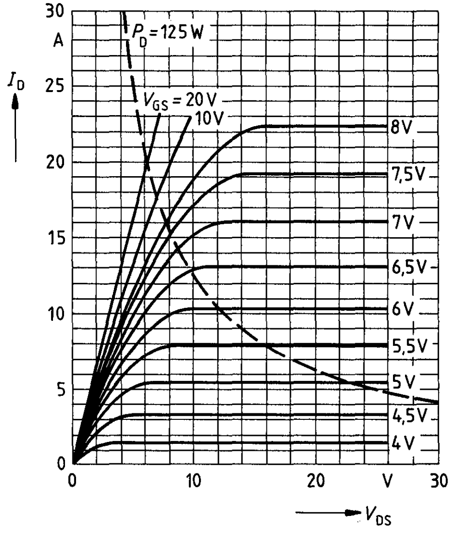
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	0,35	0,40	Ω	V_{GS} = 10V I_D = 5,5A
Dynamic ratings						
Forward transconductance	g_{fs}	3,3	4,5	–	S	V_{DS} = 25V I_D = 5,5A
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	300	500	pF	
Reverse transfer capacitance	C_{rss}	–	120	200		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	11,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	46		
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1000	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	10	–	µC	

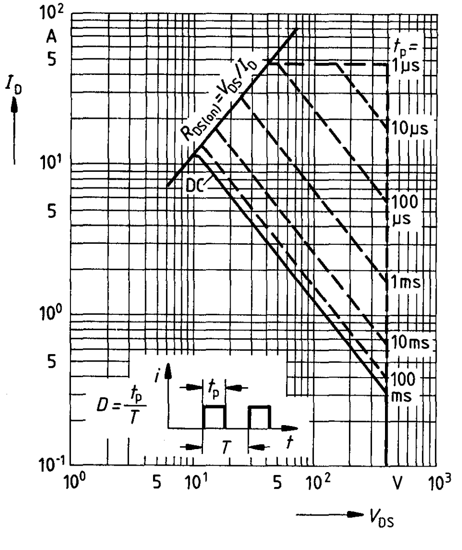
Power dissipation $P_D = f(T_C)$



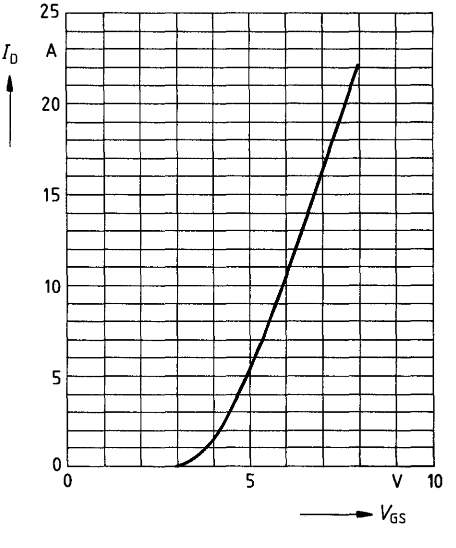
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



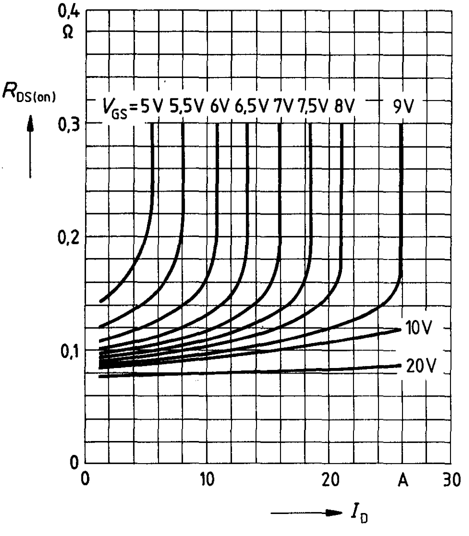
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



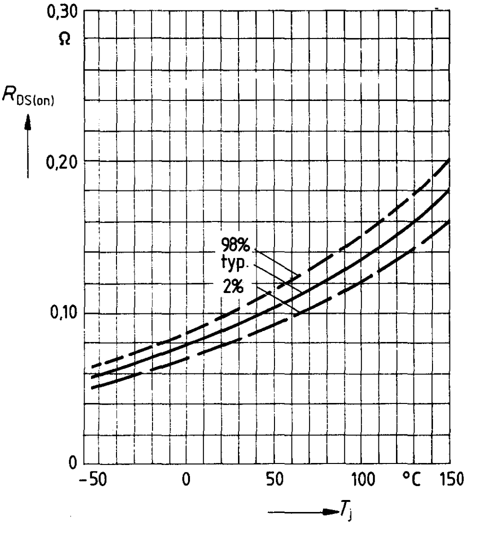
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



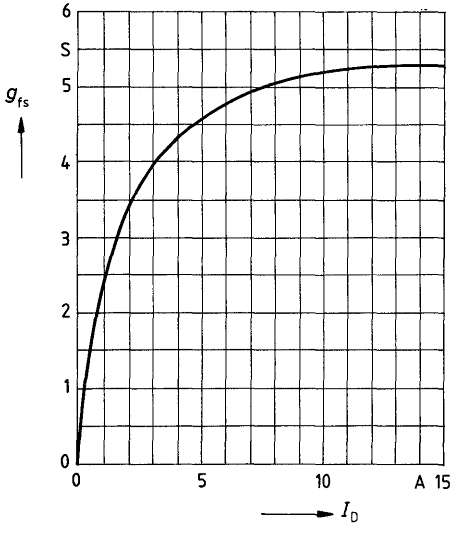
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



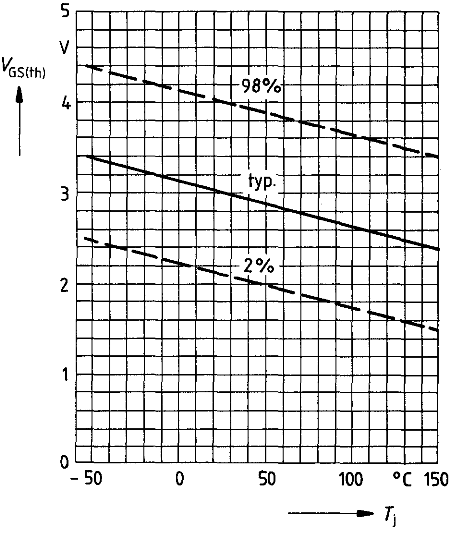
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 9A, V_{GS} = 10V
(spread)



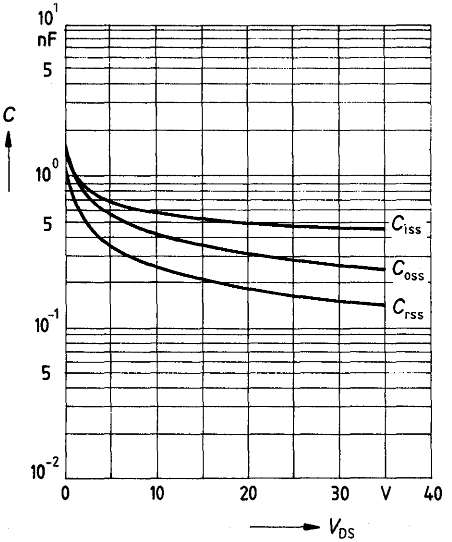
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



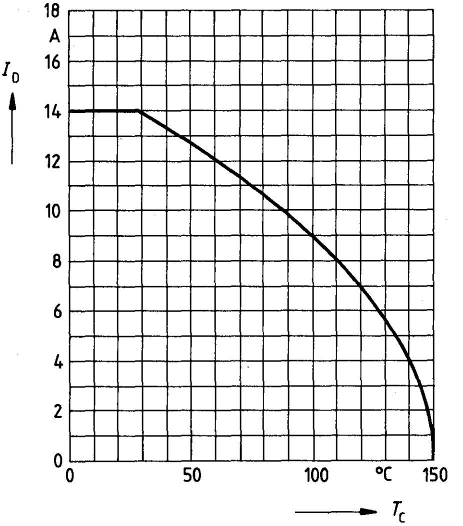
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



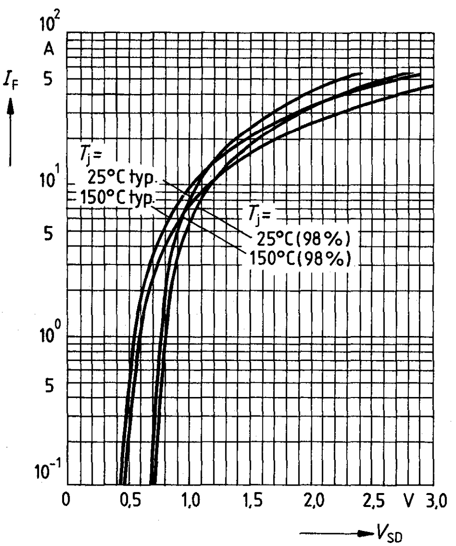
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



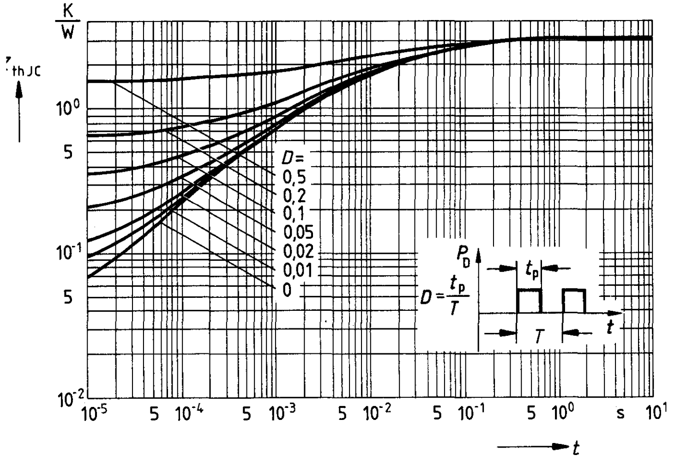
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



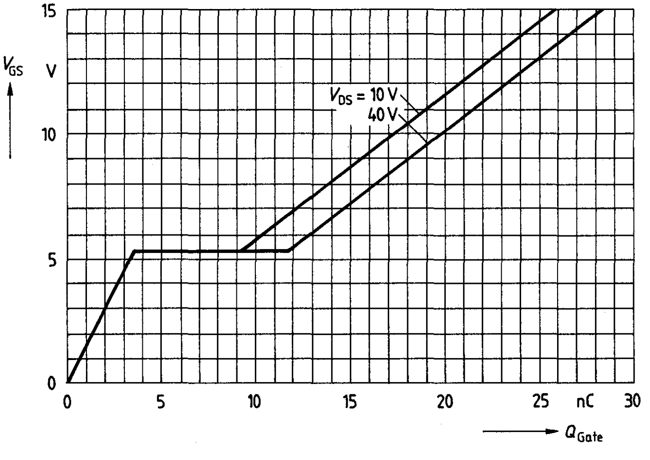
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

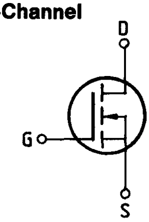


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 18A$



Main ratings

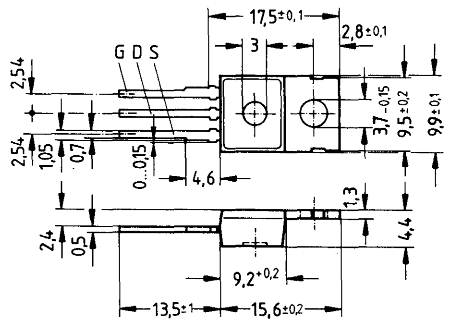
N-Channel



Drain-source voltage V_{DS} **= 50 V**
Continuous drain current I_D **= 13 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,12 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 71 A	C67078-A1316-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	13	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	48	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th JC}$	≤3,1	K/W	
Chip – ambient	$R_{th JA}$	≤75	K/W	

Electrical characteristics

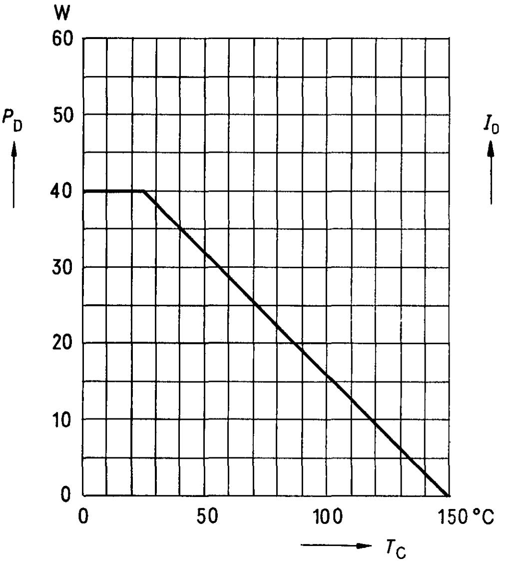
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,11	0,12	Ω	V_{GS} = 10V I_D = 9A

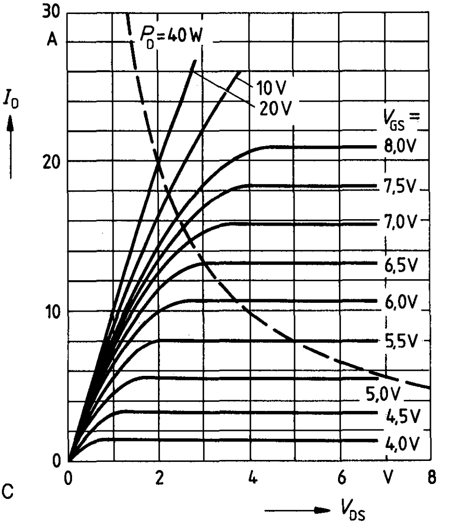
Description	Symbol	min.	typ.	max.	Unit	Conditions
Dynamic ratings						
Forward transconductance	g_{fs}	3,0	5,2	–	S	V_{DS} = 25V I_D = 9A
Input capacitance	C_{iss}	–	480	650	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	280	450		
Reverse transfer capacitance	C_{rss}	–	160	280		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	20	30	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	55	85		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	80	110		

Description	Symbol	min.	typ.	max.	Unit	Conditions
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	13	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	52		
Diode forward on-voltage	V_{SD}	–	1,6	2,2	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	120	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,15	–	µC	

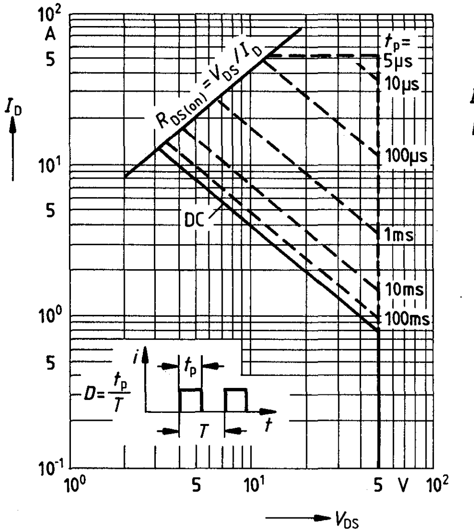
Power dissipation $P_D = f(T_C)$



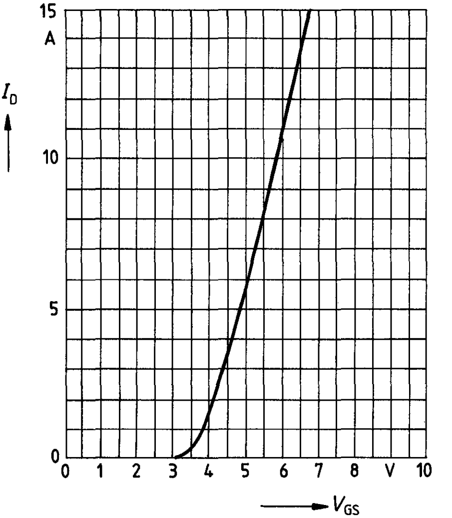
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



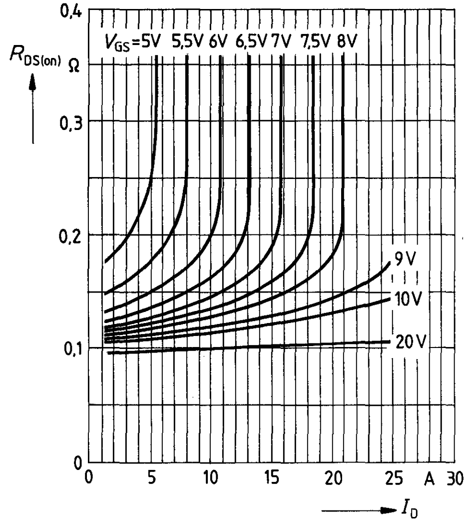
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



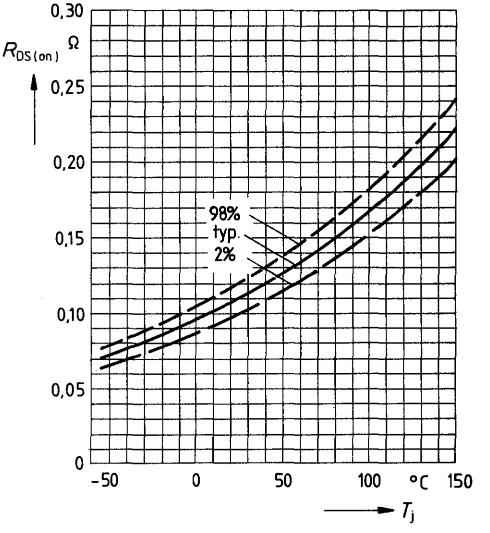
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



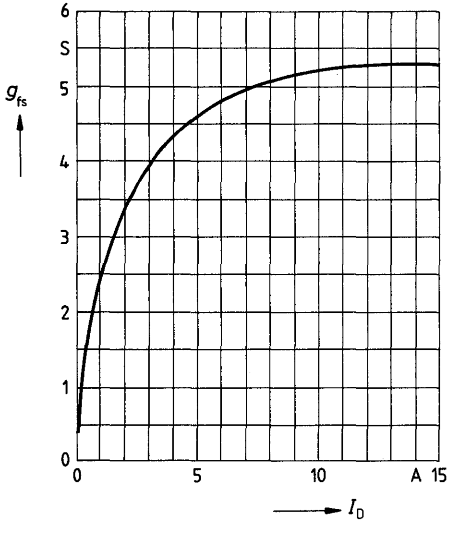
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



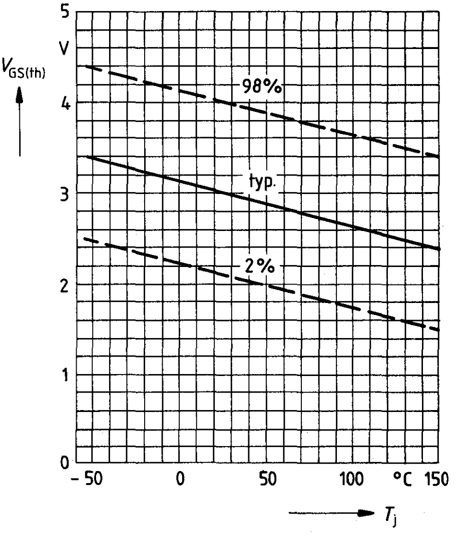
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 9A, V_{GS} = 10V
(spread)



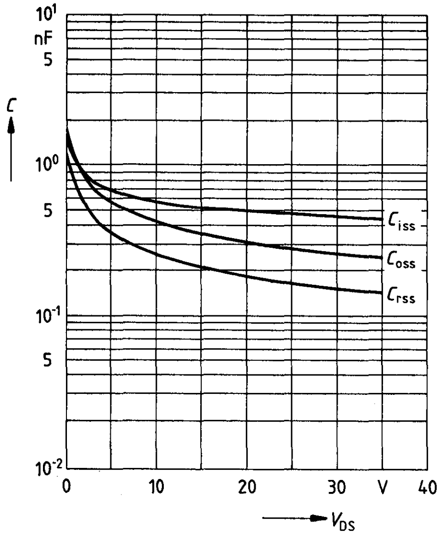
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



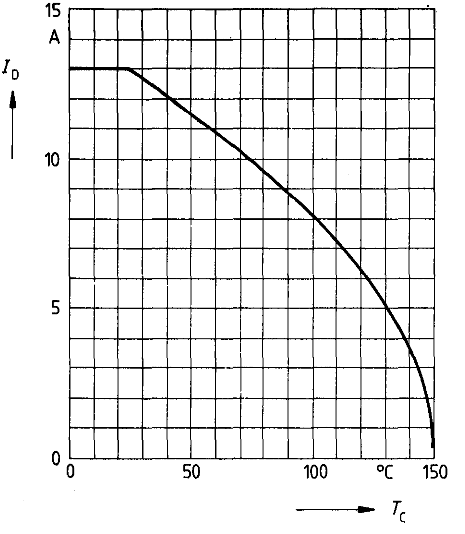
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



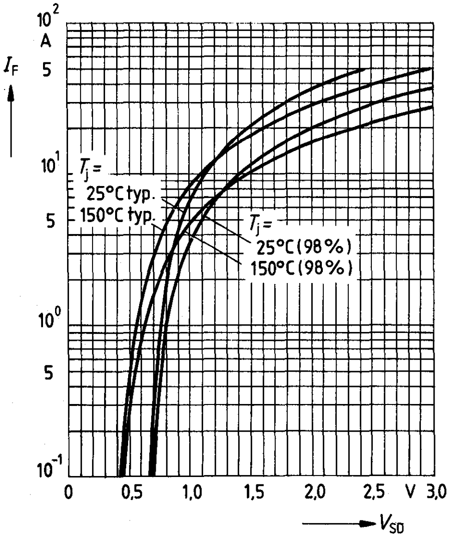
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



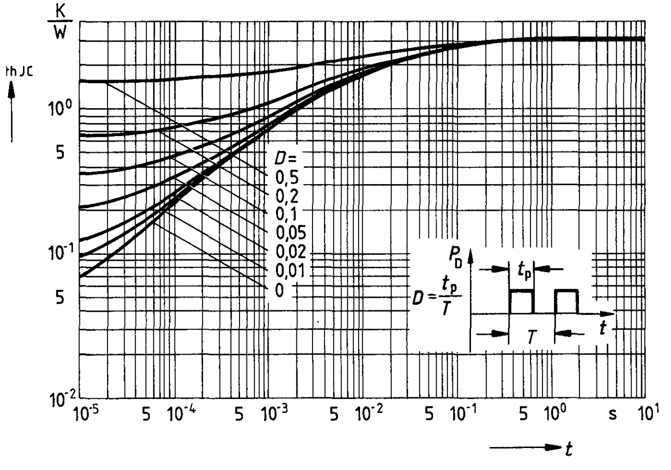
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



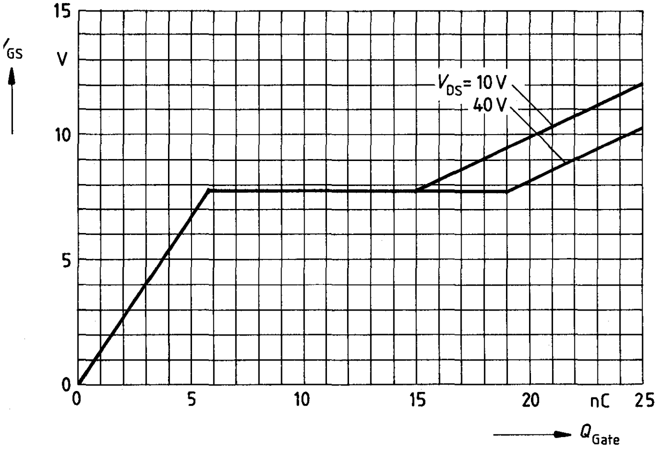
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

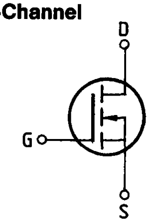


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 18A$



Main ratings

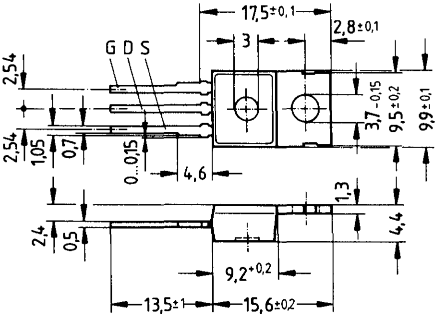
N-Channel



Drain-source voltage V_{DS} **= 50 V**
Continuous drain current I_D **= 14 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,1 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
BUZ 71 L	C67078-A1316-A5



Dimensions in mm

Maximum ratings

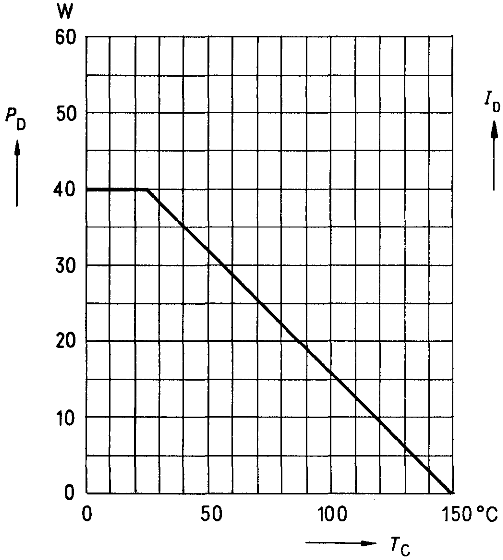
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	14	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	56	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±10	V	
Gate source peak voltage	V_{gs}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

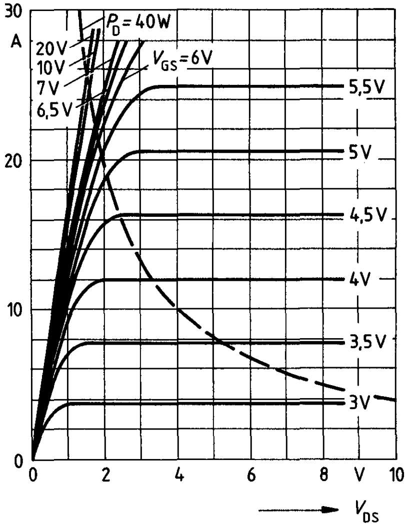
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	1,5	2,0	2,5		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,06	0,1	Ω	V_{GS} = 5V I_D = 9A
Dynamic ratings						
Forward transconductance	g_{fs}	5,0	9,0	–	S	V_{DS} = 25V I_D = 9A
Input capacitance	C_{iss}	–	620	825	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	280	450		
Reverse transfer capacitance	C_{rss}	–	95	160		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	25	ns	V_{CC} = 30V I_D = 3A V_{GS} = 5V R_{GS} = 50Ω
	t_r	–	30	45		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	90	115		
	t_f	–	50	70		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	14	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	56		
Diode forward on-voltage	V_{SD}	–	1,3	1,8	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	120	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,15	–	µC	

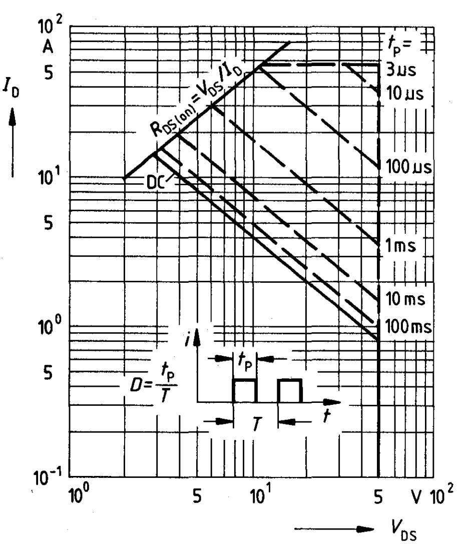
Power dissipation $P_D = f(T_C)$



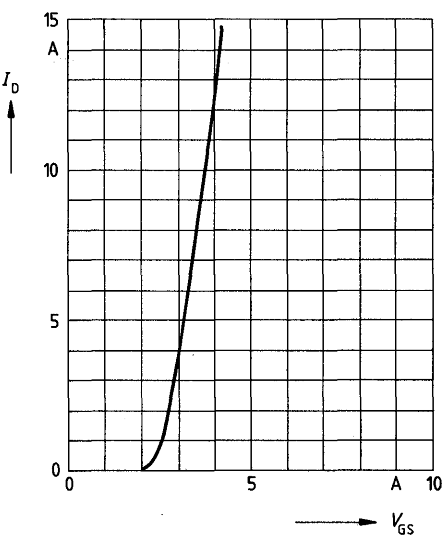
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



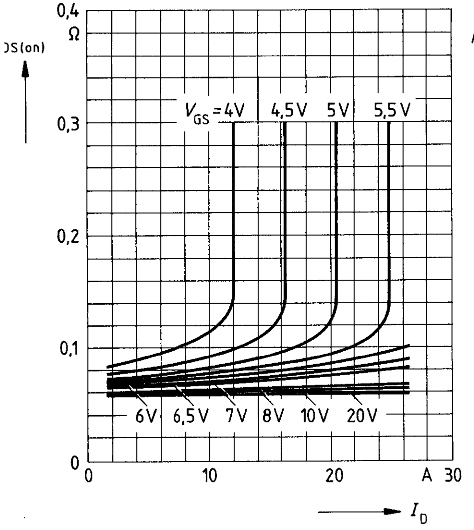
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



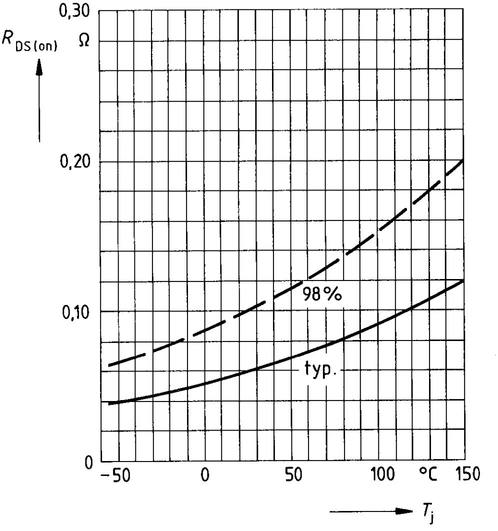
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



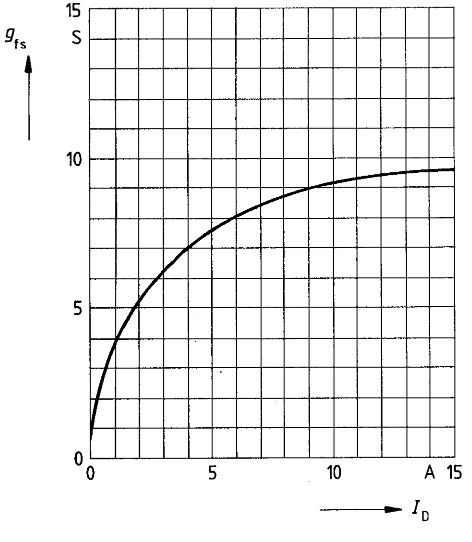
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



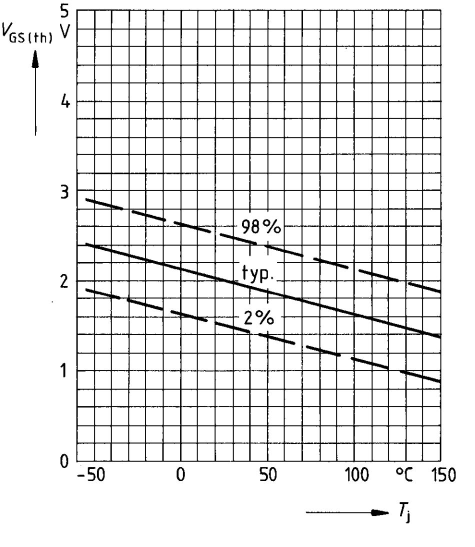
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 9A, V_{GS} = 5V
(spread)



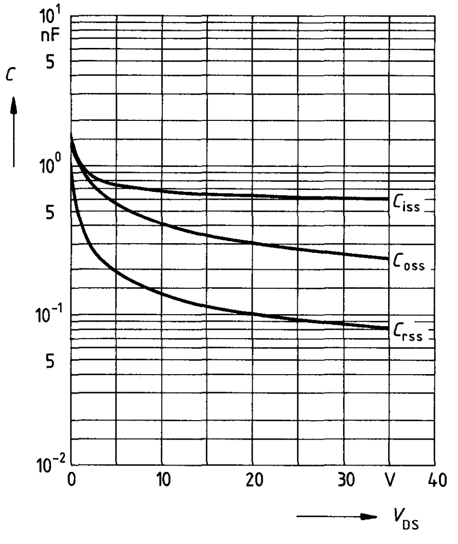
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



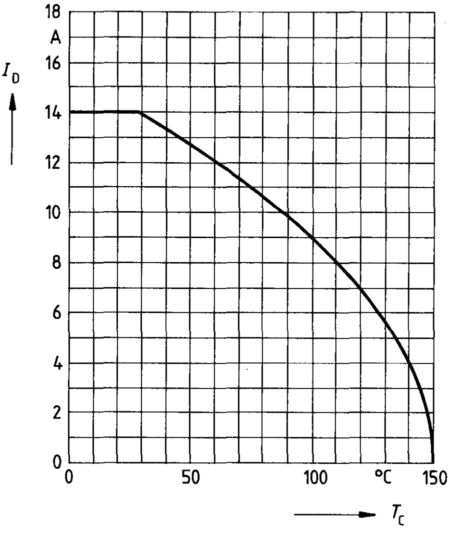
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



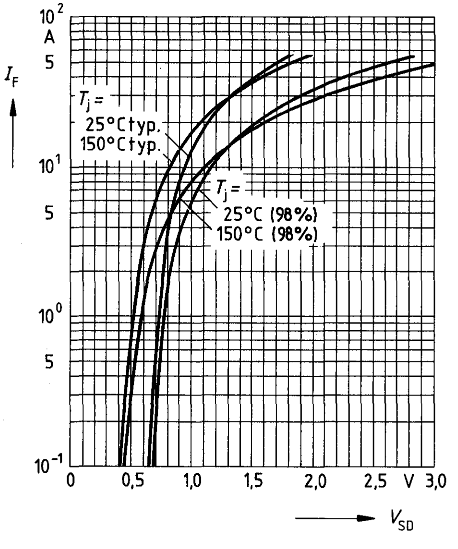
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



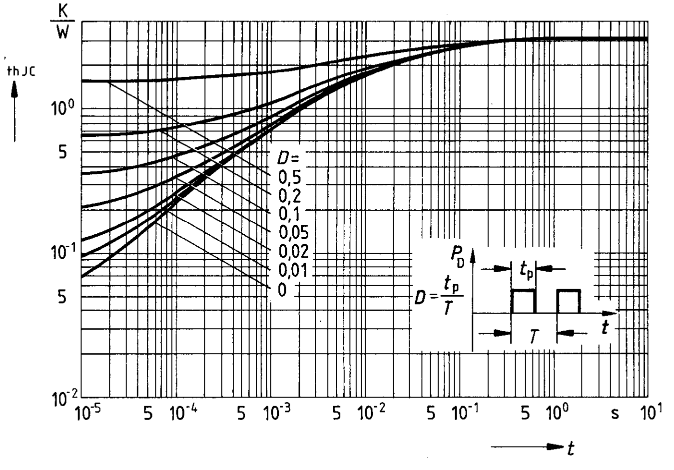
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



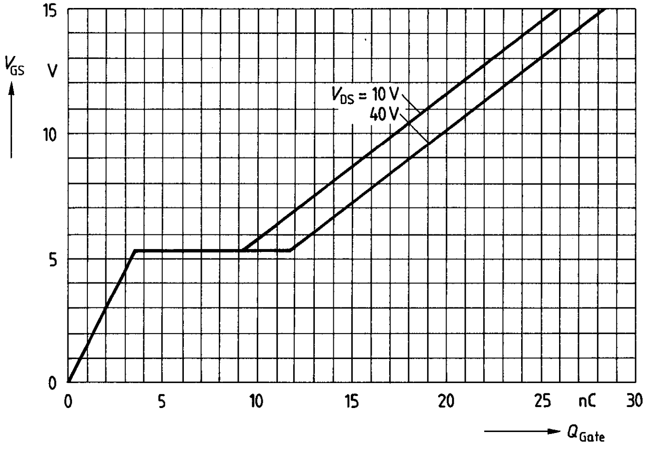
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



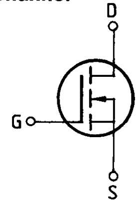
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 18A$



Main ratings

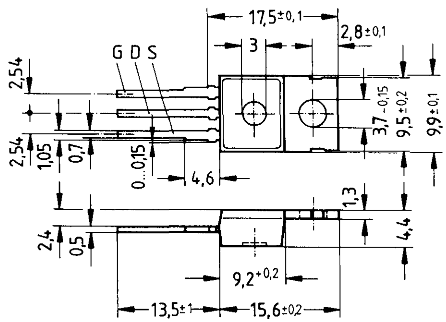
Drain-source voltage V_{DS} **= 100 V**
Continuous drain current I_D **= 10 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,2 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
▣ BUZ 72	C67078-A1313-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	10	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	40	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

 ▣ Preferred Type

Electrical characteristics

(at T_j = 25 °C unless otherwise specified)

Static ratings

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,17	0,2	Ω	V_{GS} = 10V I_D = 5A

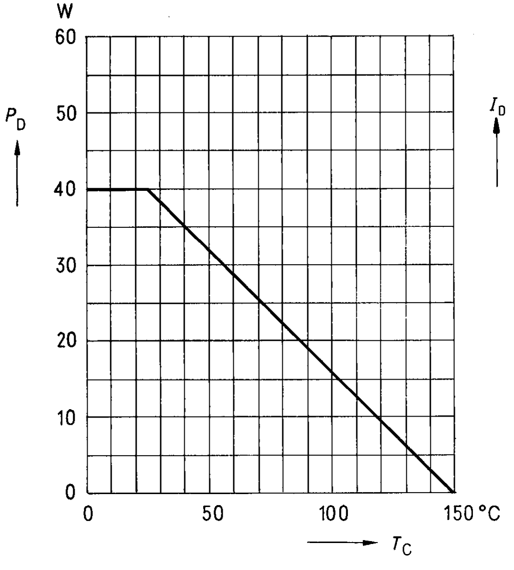
Dynamic ratings

Description	Symbol	min.	typ.	max.	Unit	Conditions
Forward transconductance	g_{fs}	2,7	3,8	–	S	V_{DS} = 25V I_D = 5A
Input capacitance	C_{iss}	–	450	600	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	150	240		
Reverse transfer capacitance	C_{rss}	–	80	130		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	20	30	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	45	70		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	55	70		

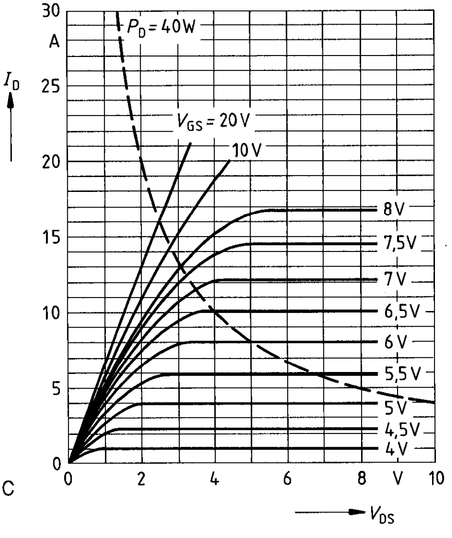
Reverse diode

Description	Symbol	min.	typ.	max.	Unit	Conditions
Continuous reverse drain current	I_{DR}	–	–	10	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	40		
Diode forward on-voltage	V_{SD}	–	1,55	2,1	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	170	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	0,30	–	µC	

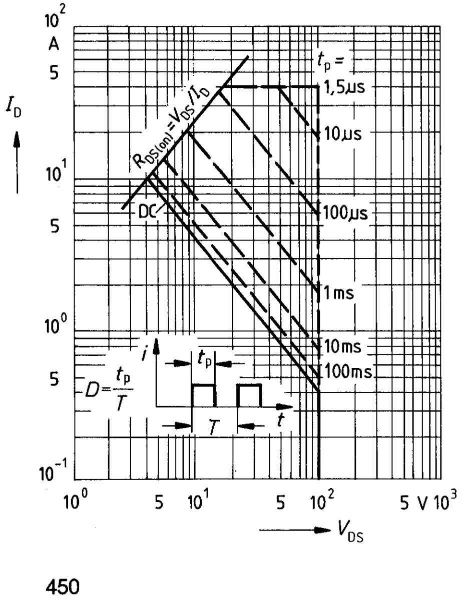
Power dissipation $P_D = f(T_C)$



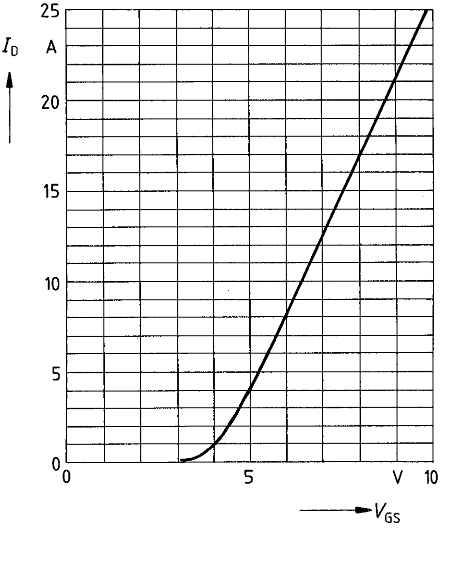
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25°C$



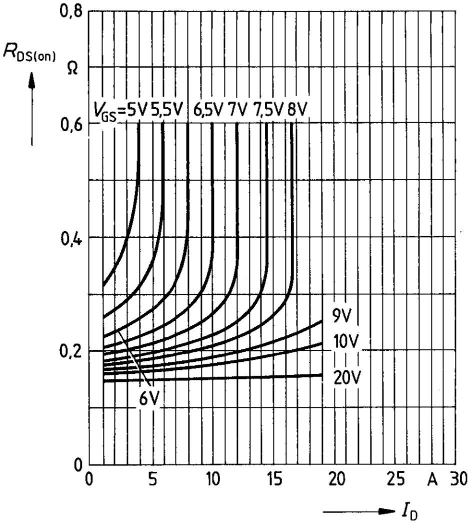
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25°C$



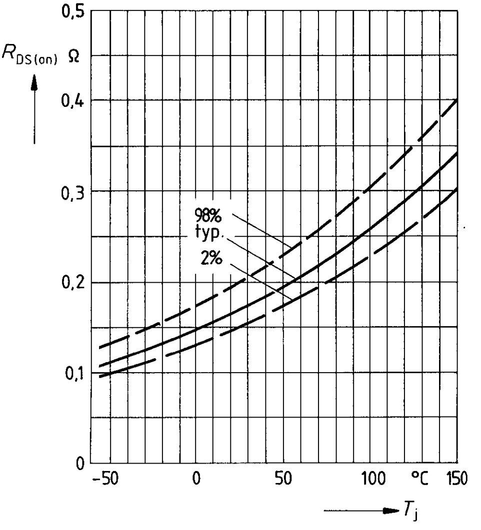
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25°C$



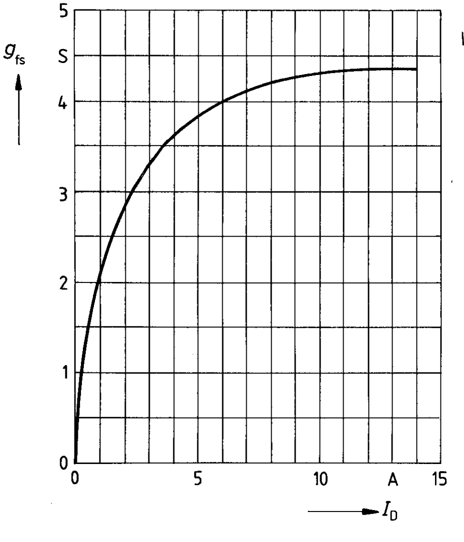
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



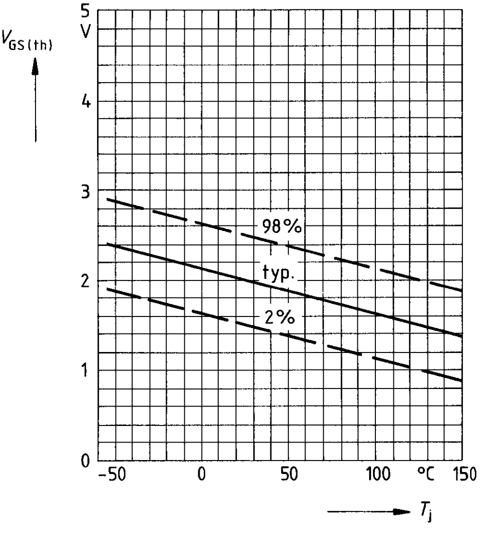
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 5A, V_{GS} = 10V
(spread)



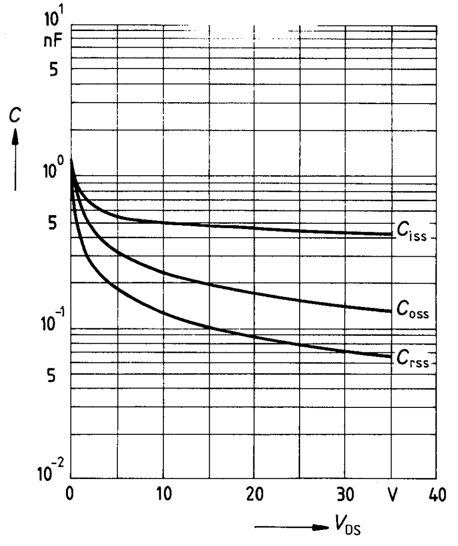
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



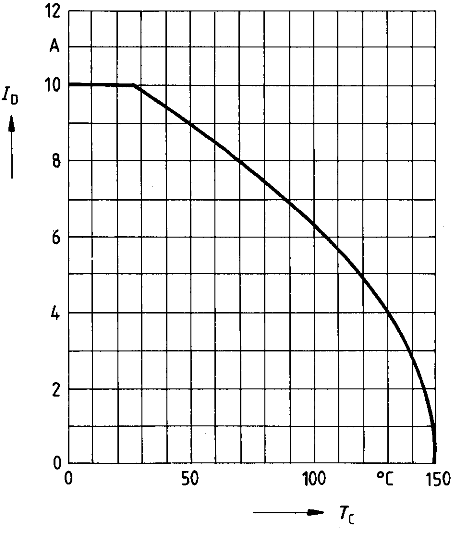
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



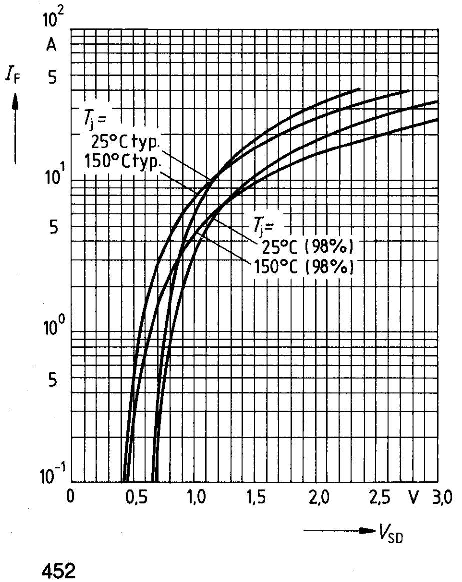
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



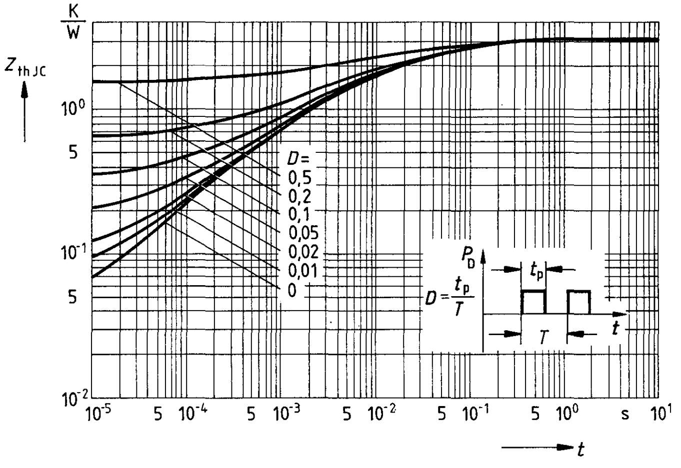
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



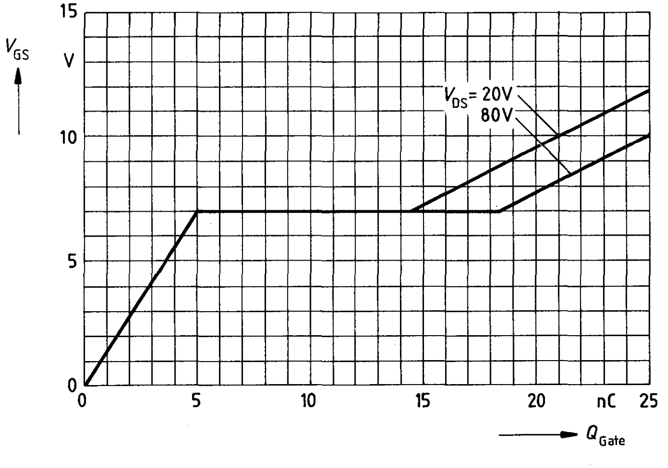
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

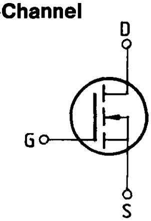


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14A$



Main ratings

N-Channel

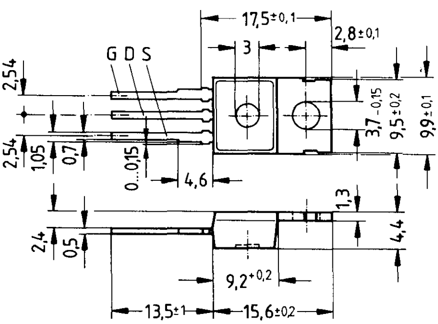


Drain-source voltage	V_{DS}	**= 100 V**
Continuous drain current	I_D	**= 9 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,25 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 72 A	C67078-A1313-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	9	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	36	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

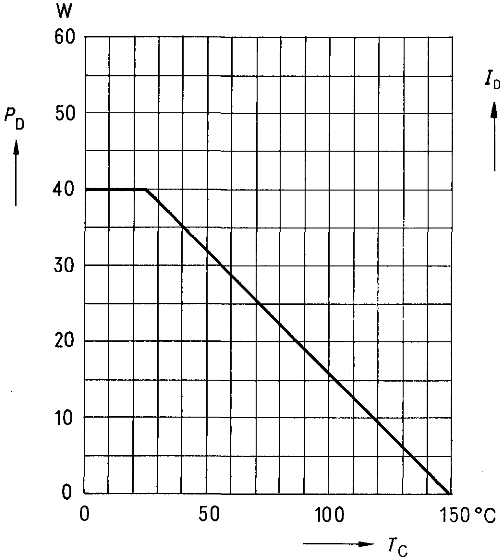
 S Preferred Type

Electrical characteristics

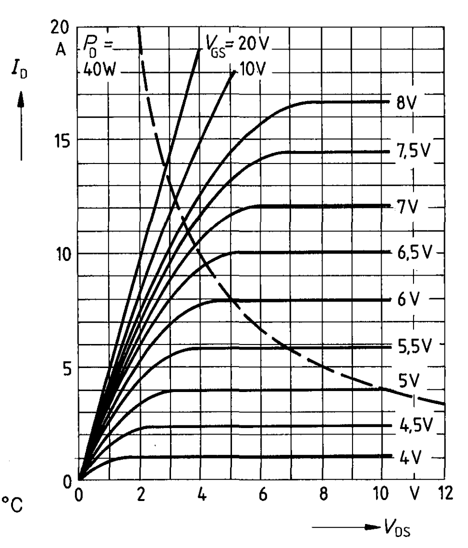
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,23	0,25	Ω	V_{GS} = 10V I_D = 5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	3,8	–	S	V_{DS} = 25V I_D = 5A
Input capacitance	C_{iss}	–	450	600	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	150	240		
Reverse transfer capacitance	C_{rss}	–	80	130		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	20	30	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	45	70		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	55	70		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	9,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	36		
Diode forward on-voltage	V_{SD}	–	1,5	2,0	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	170	–	ns	T_j = 25 °C
Reverse recovery charge	Q_{rr}	–	0,30	–	µC	I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V

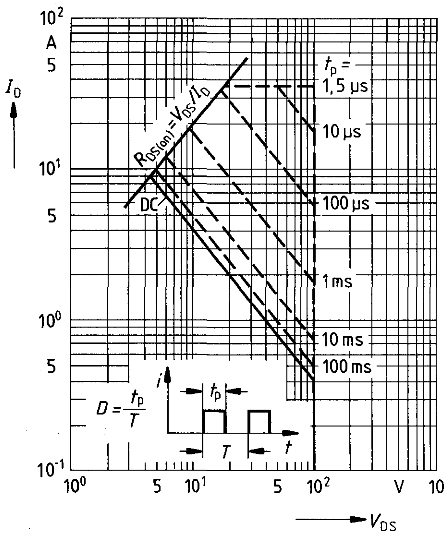
Power dissipation $P_D = f(T_C)$



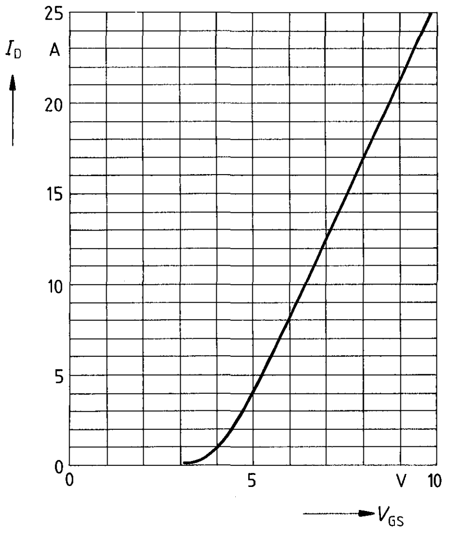
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



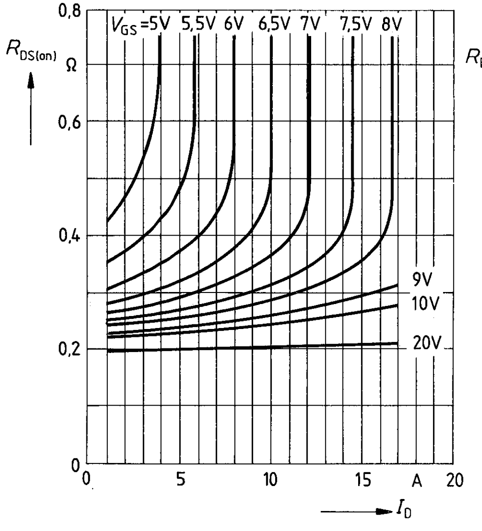
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



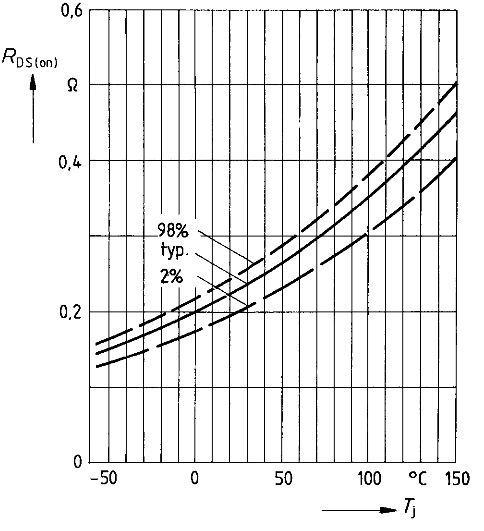
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



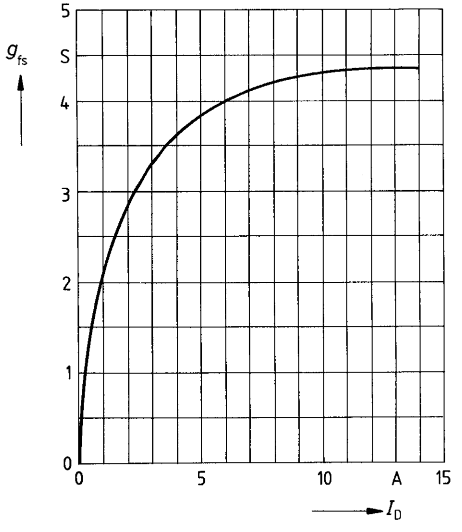
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



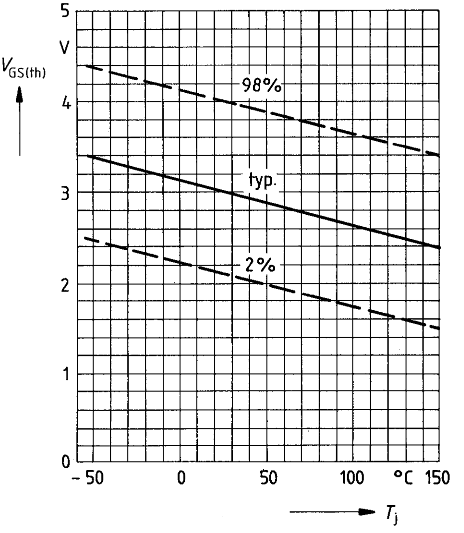
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 5A, V_{GS} = 10V
(spread)



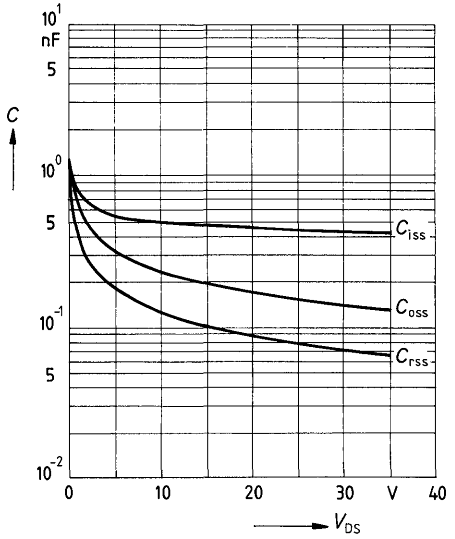
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



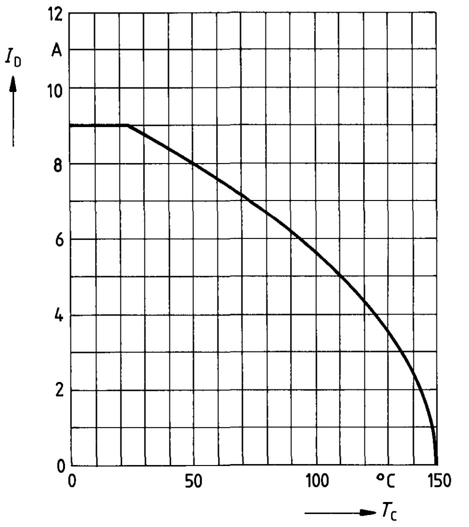
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



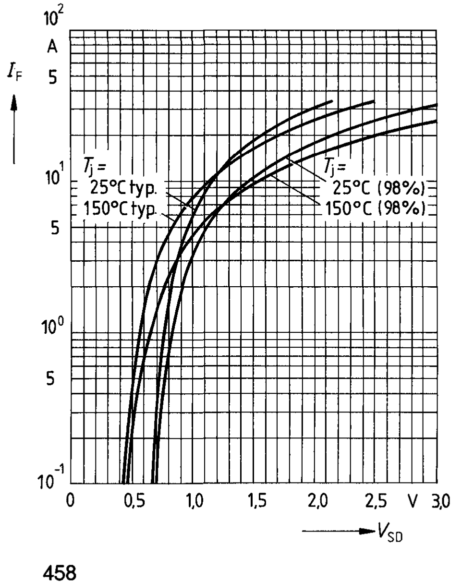
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



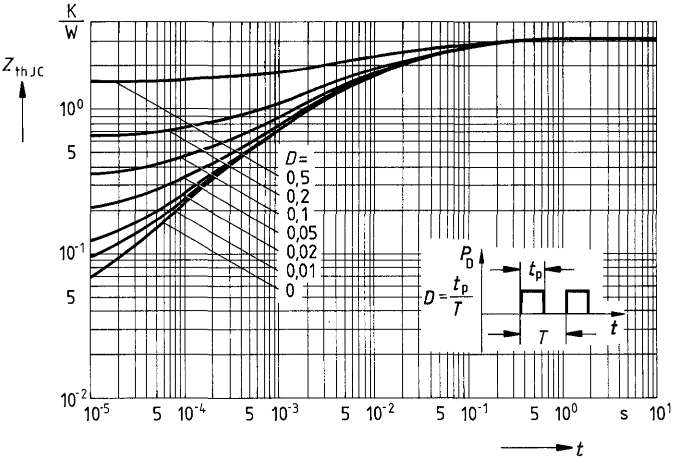
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



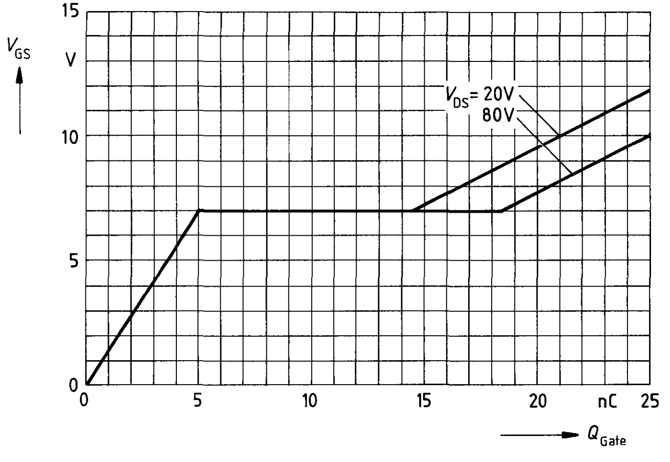
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

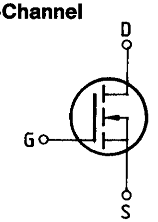


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14A$



Main ratings

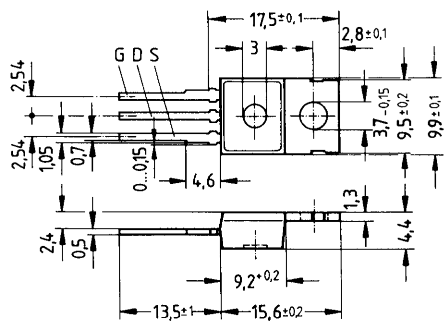
N-Channel



Drain-source voltage V_{DS} = **200 V**
Continuous drain current I_D = **7 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,4 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 73	C67078-A1317-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	7	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	28	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

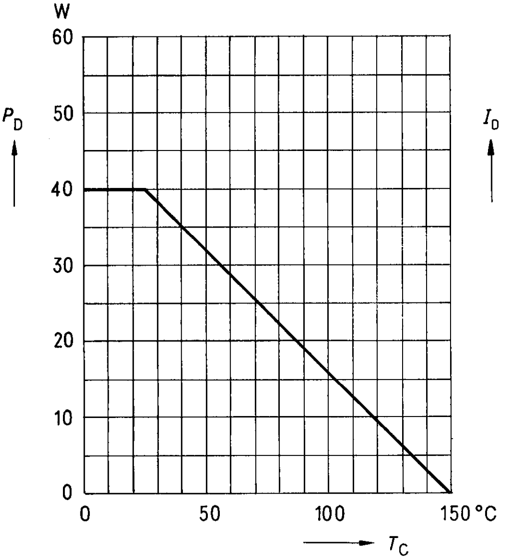
 S Preferred Type

Electrical characteristics

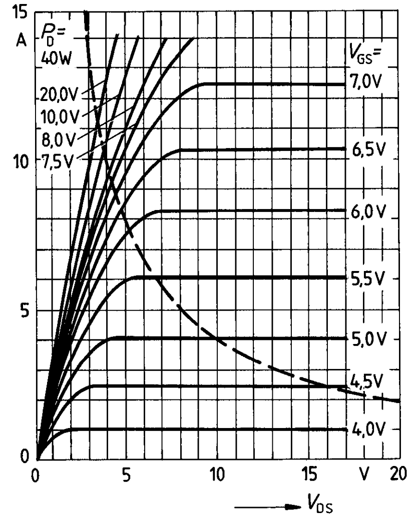
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	0,35	0,4	Ω	V_{GS} = 10V I_D = 3,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,2	3,5	–	S	V_{DS} = 25V I_D = 3,5A
Input capacitance	C_{iss}	–	450	600	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	100	160		
Reverse transfer capacitance	C_{rss}	–	50	80		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	70	90		
	t_f	–	40	55		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	7,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	28		
Diode forward on-voltage	V_{SD}	–	1,4	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C
Reverse recovery charge	Q_{rr}	–	0,6	–	µC	I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V

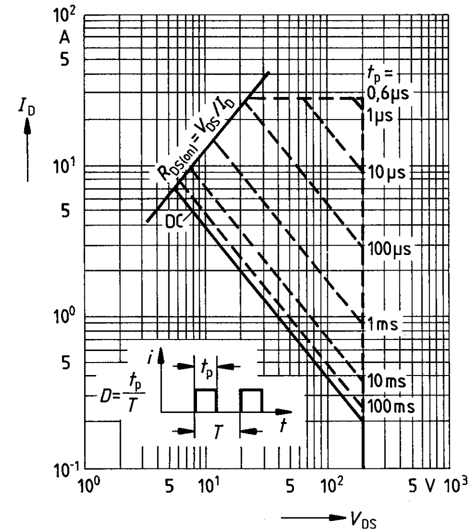
Power dissipation $P_D = f(T_C)$



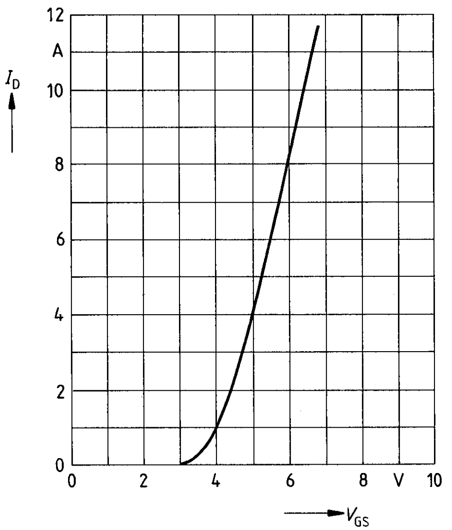
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



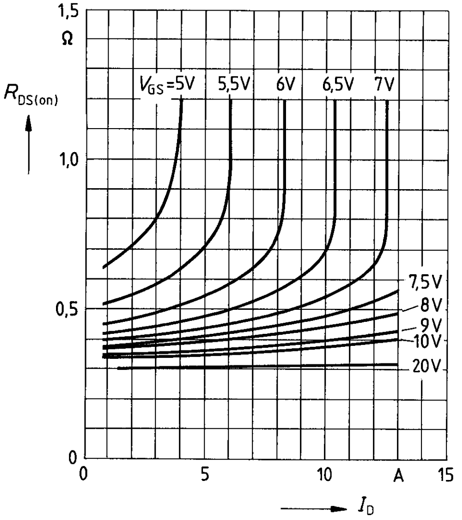
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



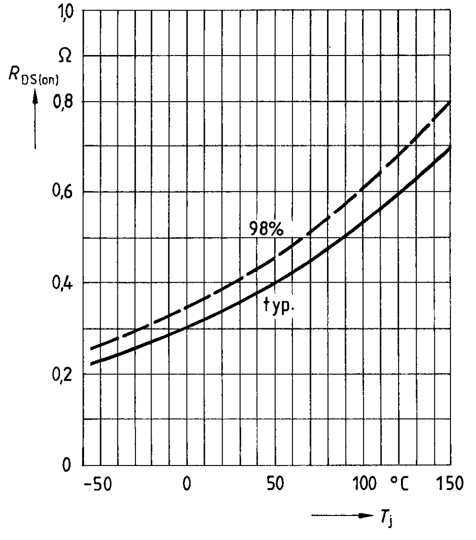
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



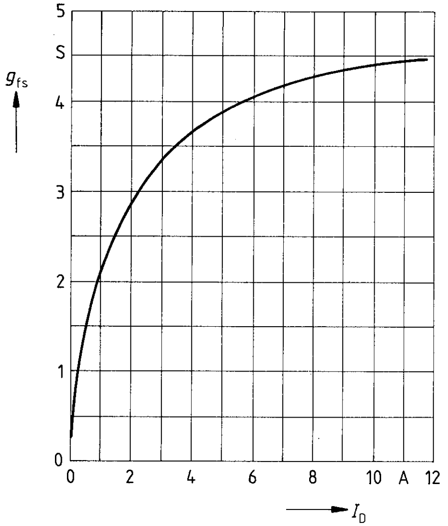
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



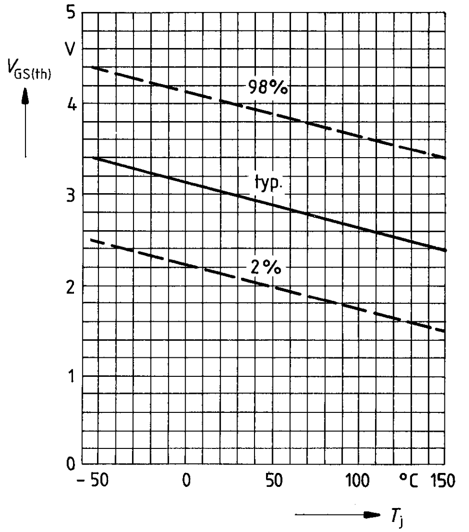
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 3{,}5A$, $V_{GS} = 10V$
(spread)



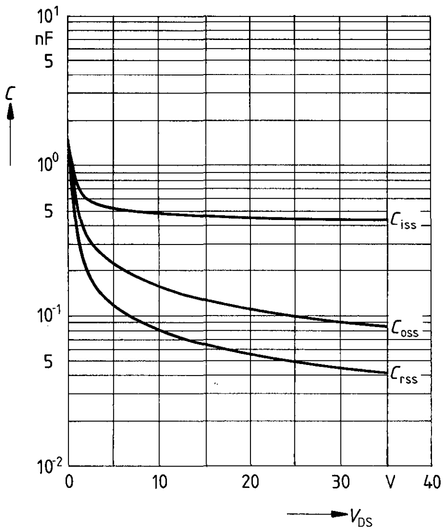
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



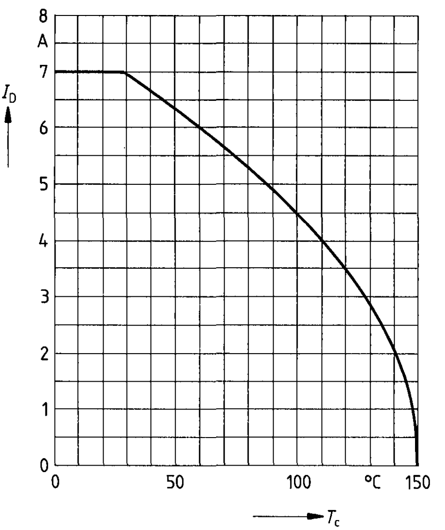
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



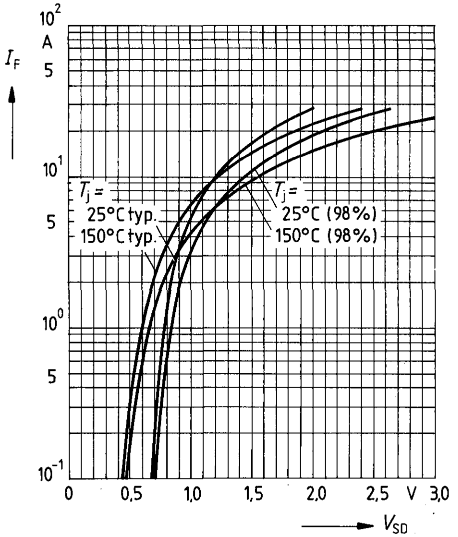
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



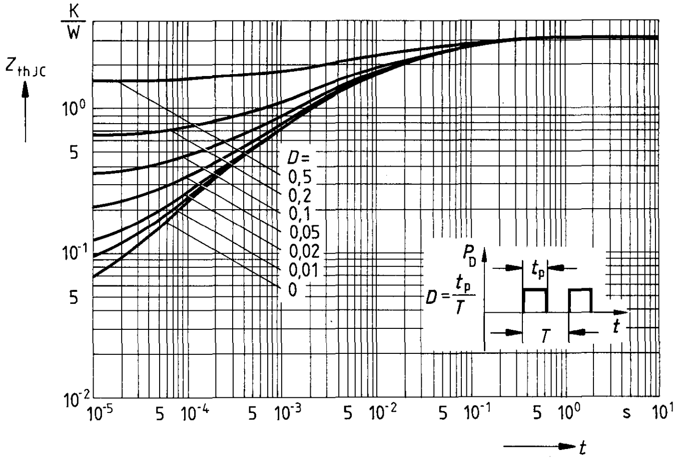
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



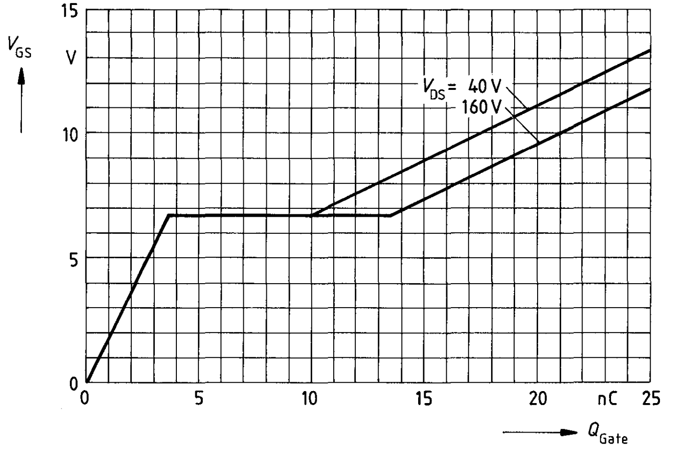
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



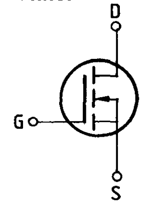
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 10{,}5A$



Main ratings

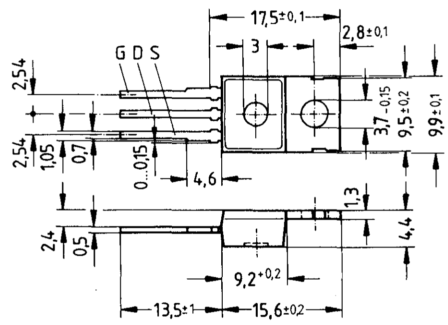
Drain-source voltage V_{DS} **= 200 V**
Continuous drain current I_D **= 5,8 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,6 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 73 A	C67078-A1317-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,8	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	23	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

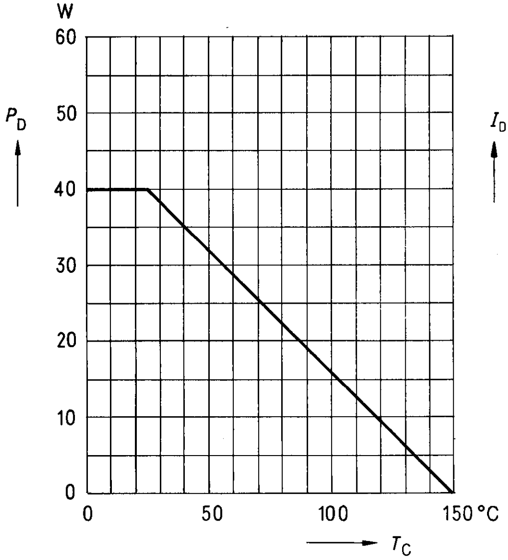
 S Preferred Type

Electrical characteristics

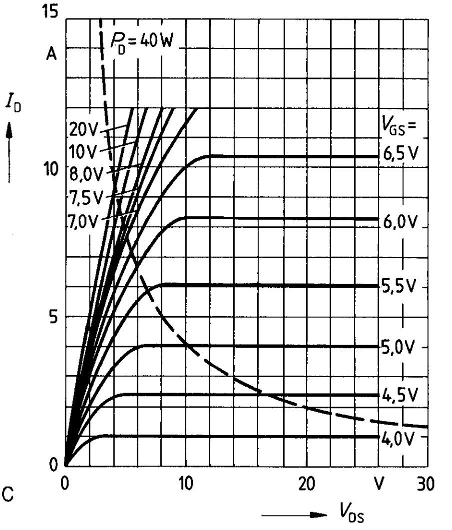
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,5	0,6	Ω	V_{GS} = 10V I_D = 3,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,2	3,5	–	S	V_{DS} = 25V I_D = 3,5A
Input capacitance	C_{iss}	–	450	600	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	100	160		
Reverse transfer capacitance	C_{rss}	–	50	80		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	40	55		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,8	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	23		
Diode forward on-voltage	V_{SD}	–	1,4	1,7	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	0,6	–	µC	

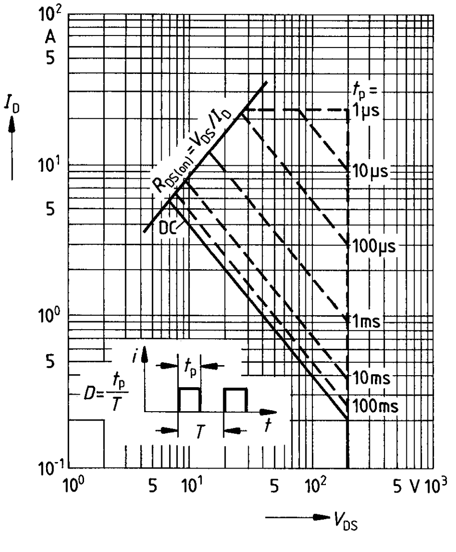
Power dissipation $P_D = f(T_C)$



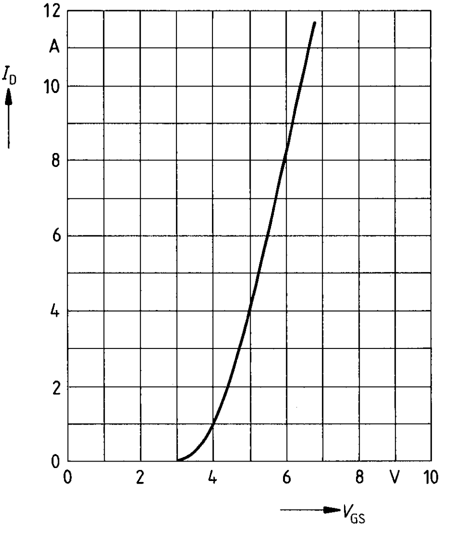
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



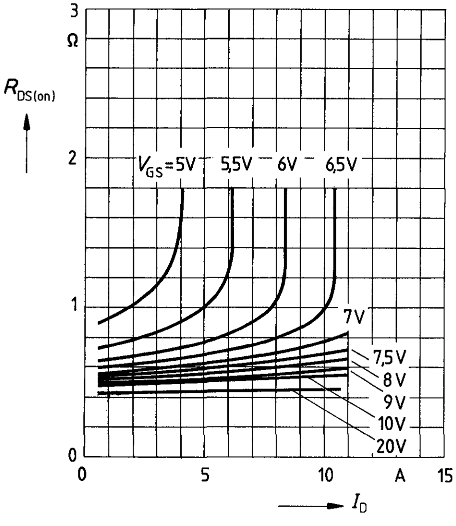
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



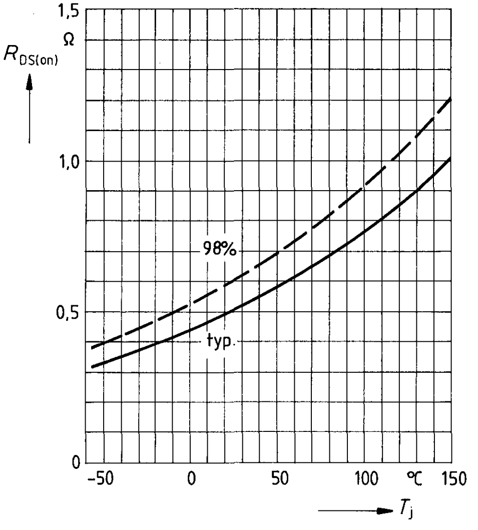
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



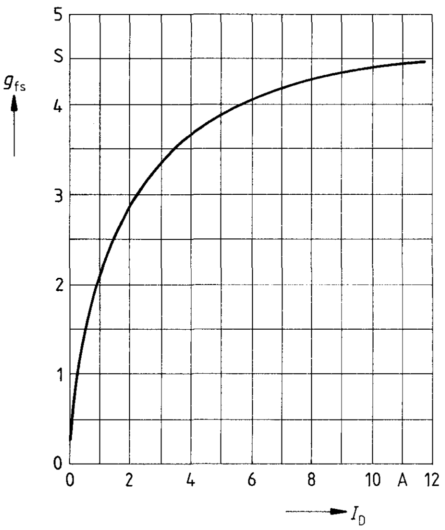
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



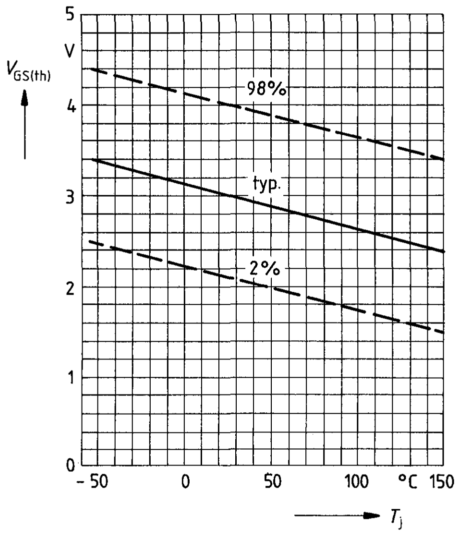
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 3{,}5A$, $V_{GS} = 10V$
(spread)



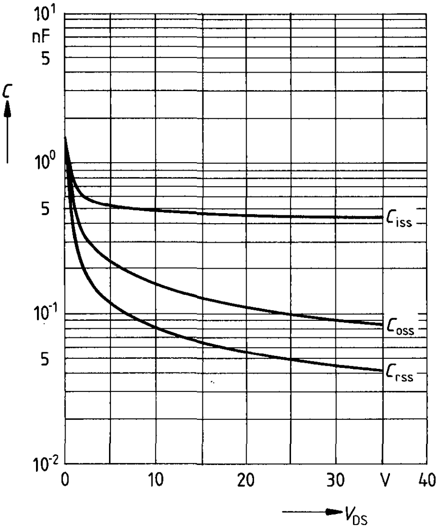
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



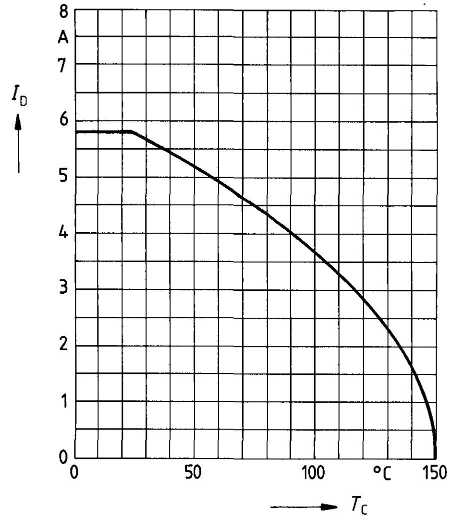
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



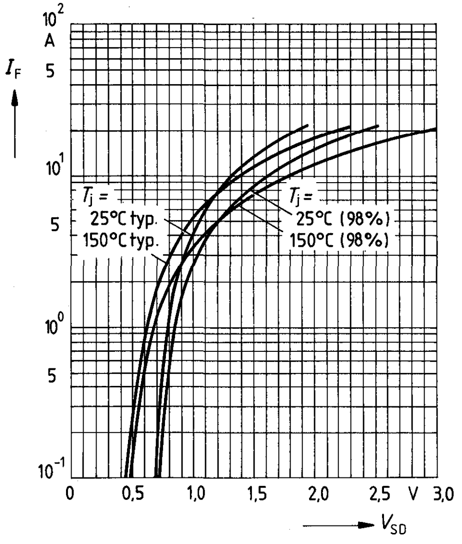
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



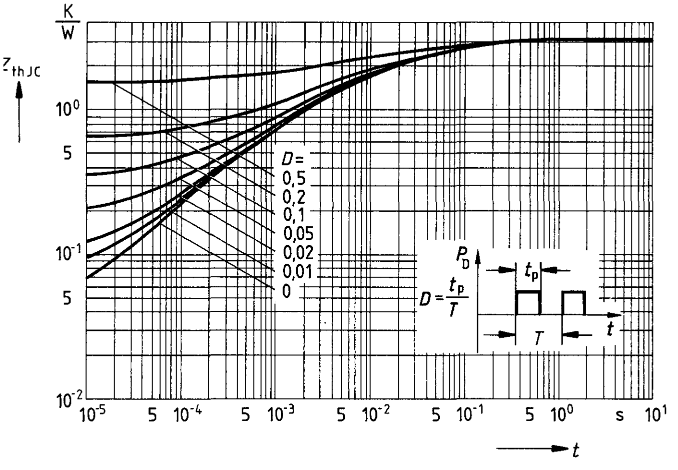
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



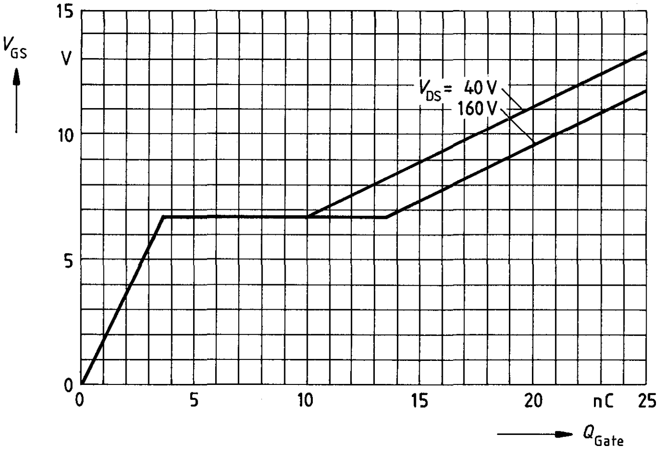
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



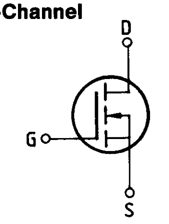
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 10{,}5A$



Main ratings

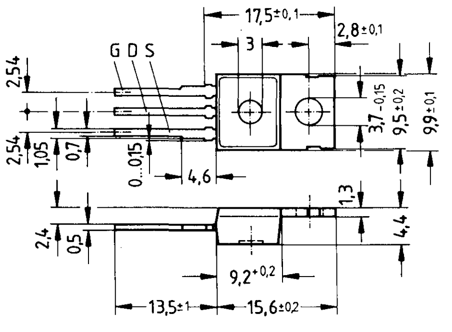
Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 2,4 A**
Drain-source on-resistance $R_{DS(on)}$ **= 3,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 74	C67078-A1314-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,4	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	9,5	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

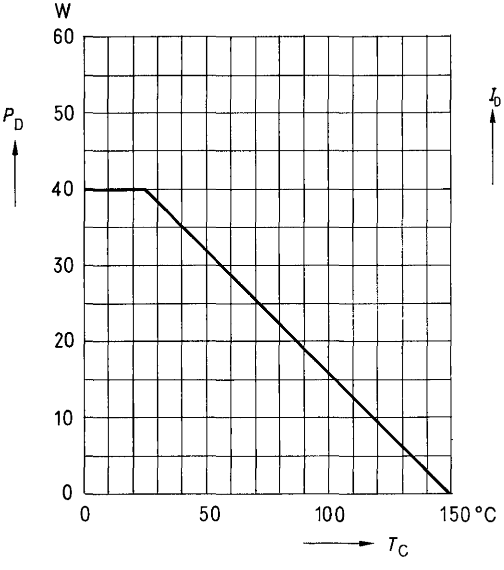
 S Preferred Type

Electrical characteristics

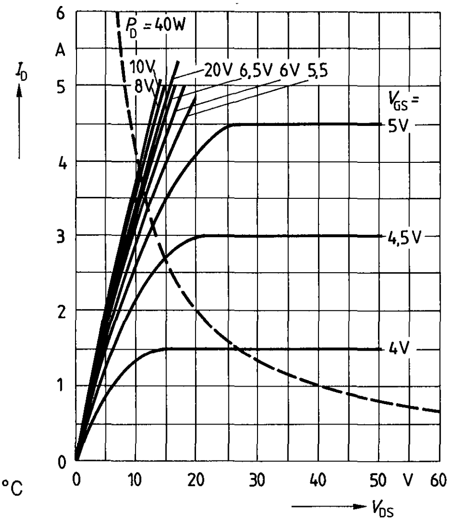
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	2,6	3,0	Ω	V_{GS} = 10V I_D = 1,2A
Dynamic ratings						
Forward transconductance	g_{fs}	1,9	2,5	–	S	V_{DS} = 25V I_D = 1,2A
Input capacitance	C_{iss}	–	300	500	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	50	80		
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 2,3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	50	65		
	t_f	–	30	40		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,4	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	9,5		
Diode forward on-voltage	V_{SD}	–	1,0	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	350	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	3,5	–	µC	

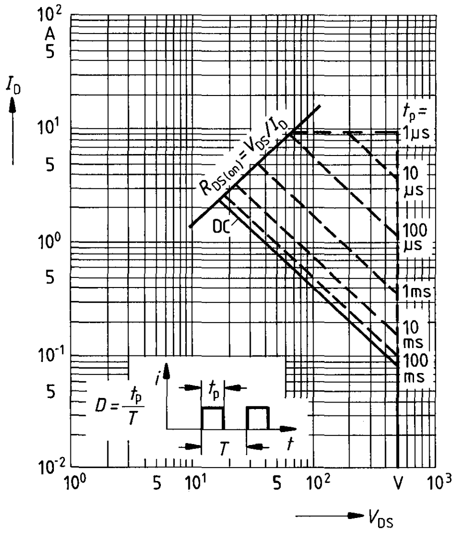
Power dissipation $P_D = f(T_C)$



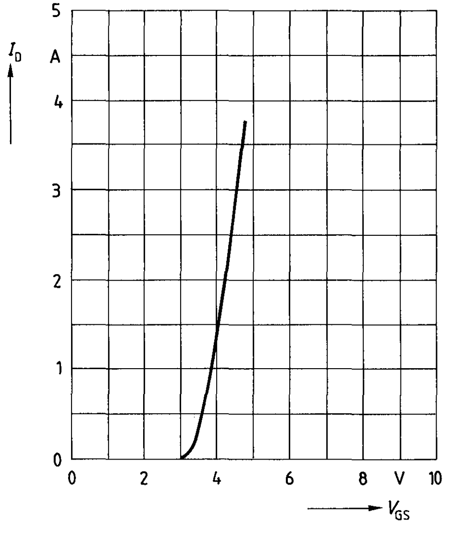
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



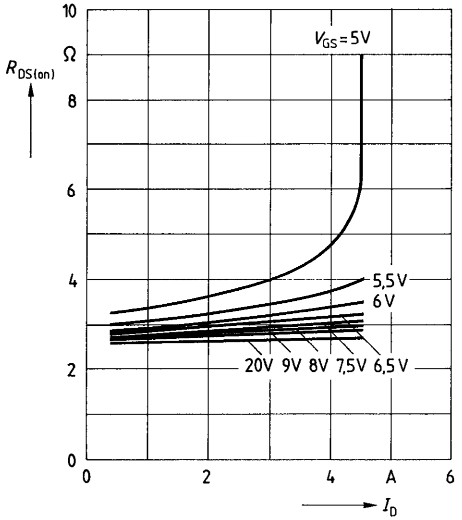
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



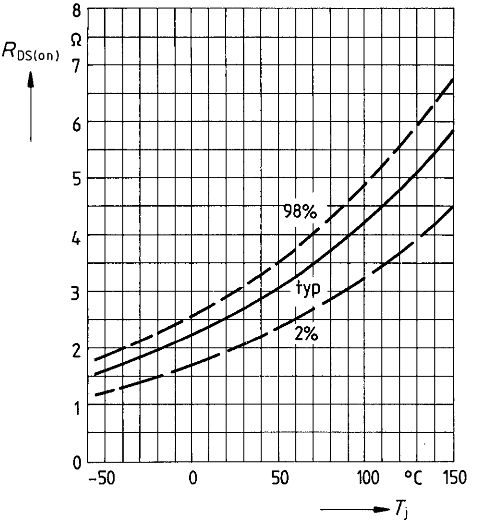
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



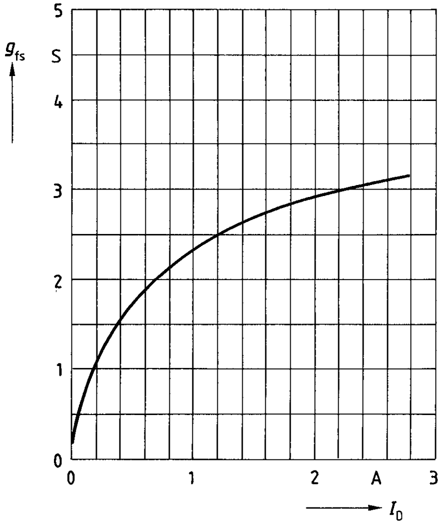
Typical drain-source on-state resistance
$R_{DS\ (on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



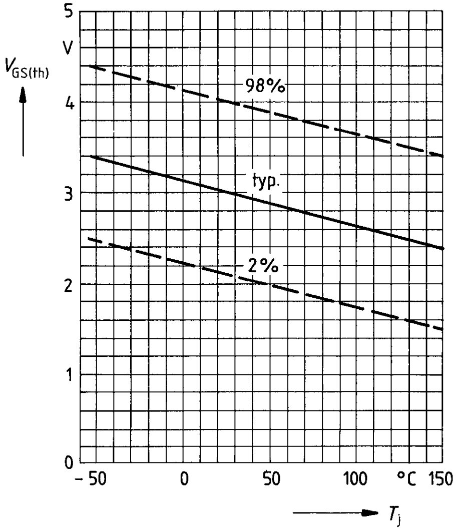
Drain-source on-state resistance
$R_{DS\ (on)} = f(T_j)$
parameter: $I_D = 1{,}2A$, $V_{GS} = 10V$
(spread)



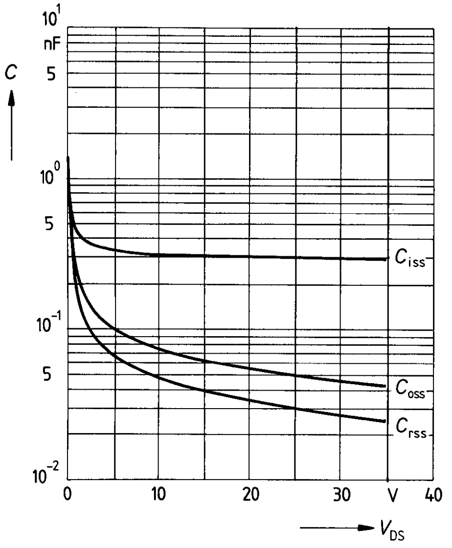
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



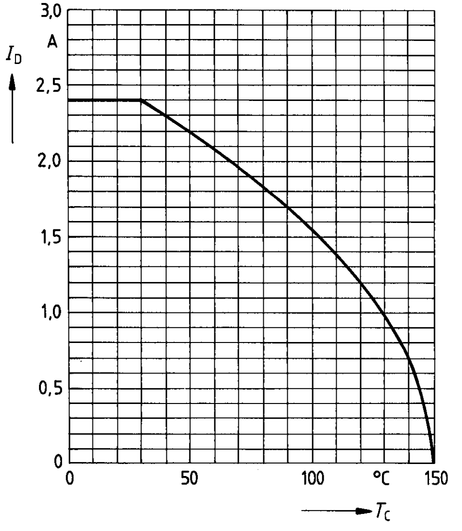
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



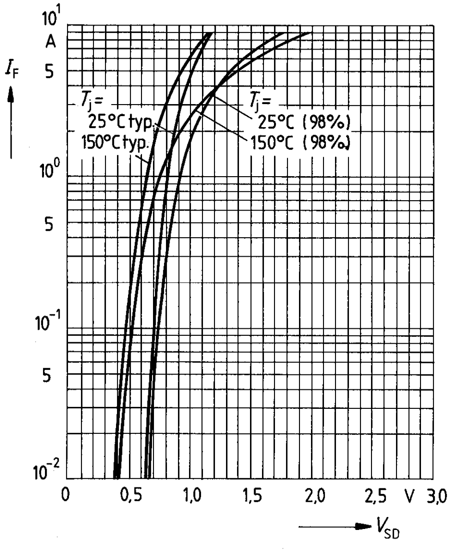
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



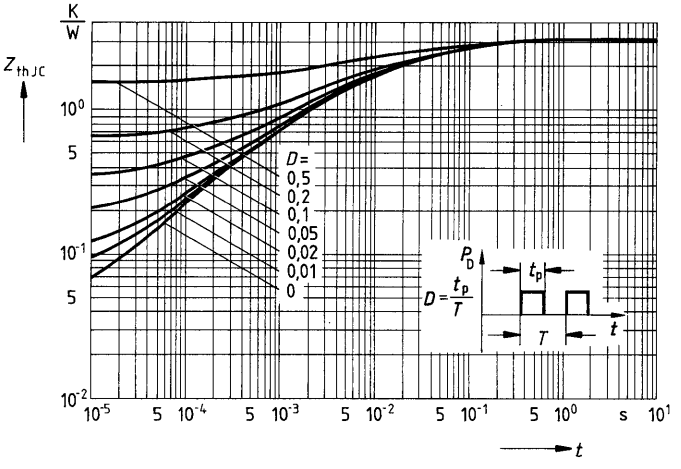
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



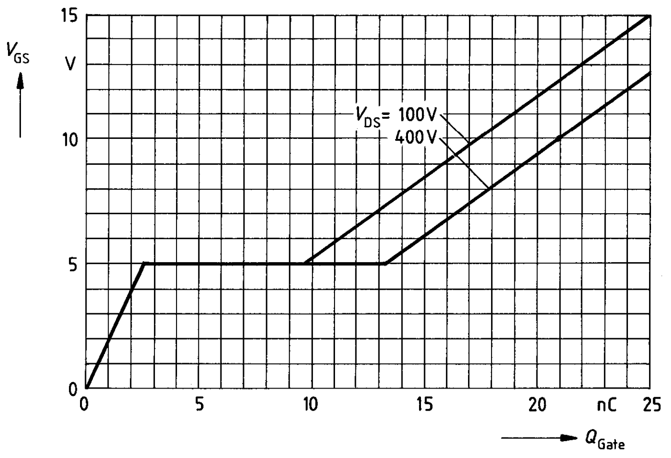
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

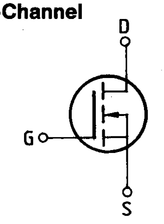


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 3{,}6A$



Main ratings

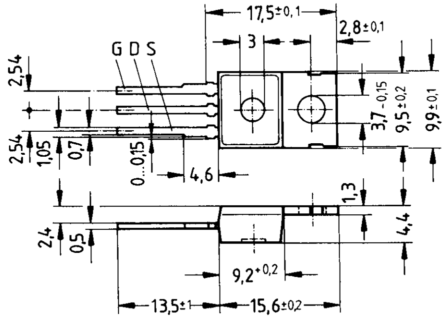
N-Channel



Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 2 A**
Drain-source on-resistance $R_{DS(on)}$ **= 4,0 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 74 A	C67078-A1314-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2	A	T_C = 40 °C
Pulsed drain current	I_{Dpuls}	8	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

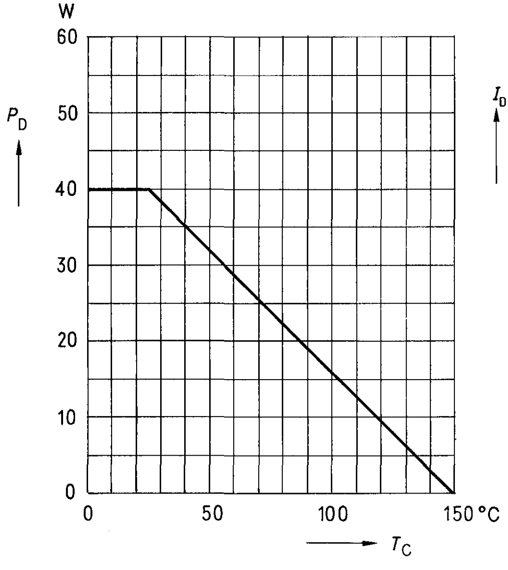
 S Preferred Type

Electrical characteristics

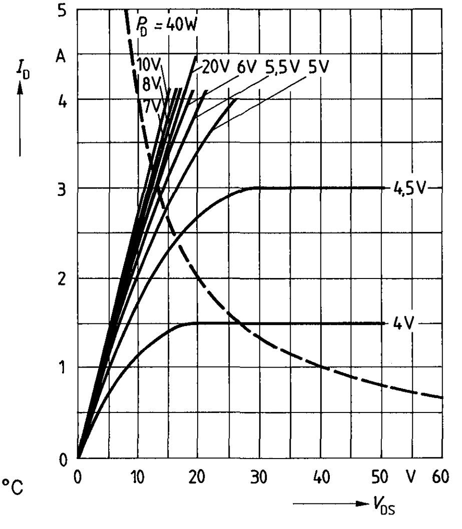
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	3,6	4,0	Ω	V_{GS} = 10V I_D = 1,2A
Dynamic ratings						
Forward transconductance	g_{fs}	1,9	2,5	–	S	V_{DS} = 25V I_D = 1,2A
Input capacitance	C_{iss}	–	300	500	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	50	80		
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} (t_{on} = $t_{d\,(on)}$ + t_r)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 2,1A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} (t_{off} = $t_{d\,(off)}$ + t_f)	$t_{d\,(off)}$	–	50	65		
	t_f	–	30	40		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	8,0		
Diode forward on-voltage	V_{SD}	–	1,0	1,3	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	350	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	3,5	–	µC	

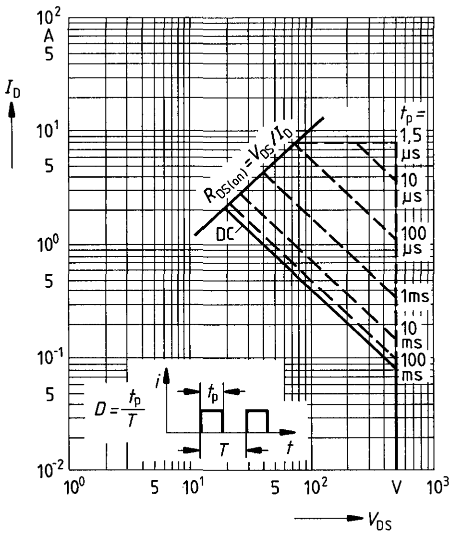
Power dissipation $P_D = f(T_C)$



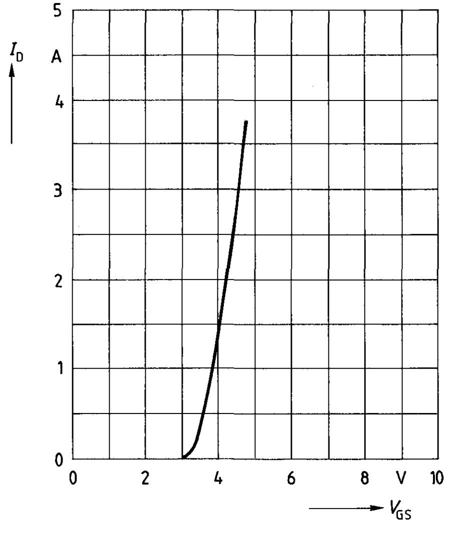
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



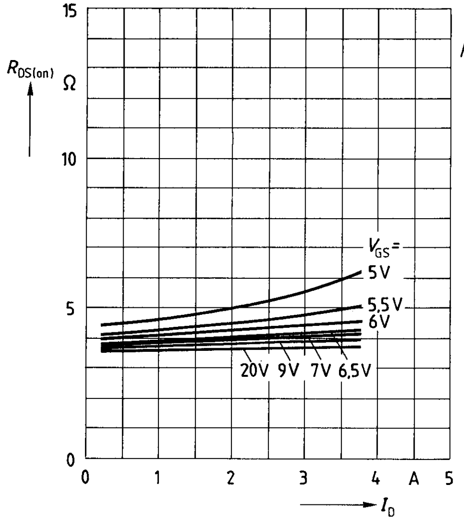
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



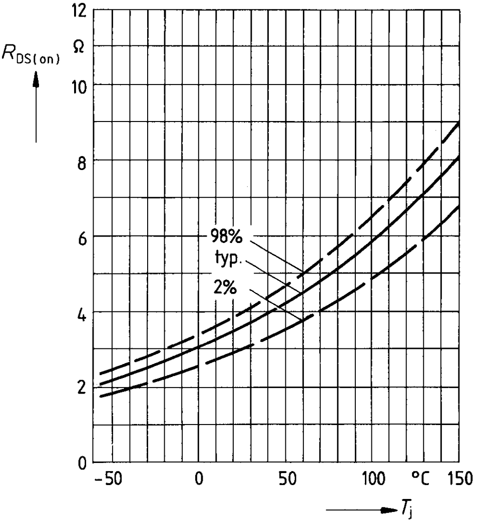
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



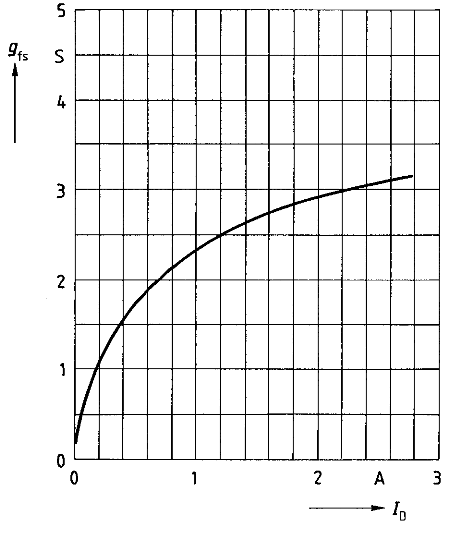
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



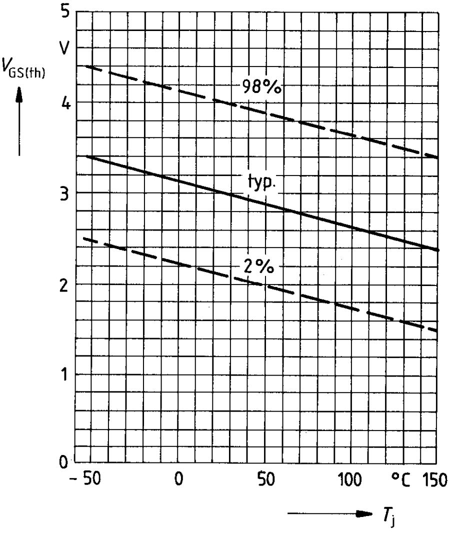
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 1{,}2A$, $V_{GS} = 10V$
(spread)



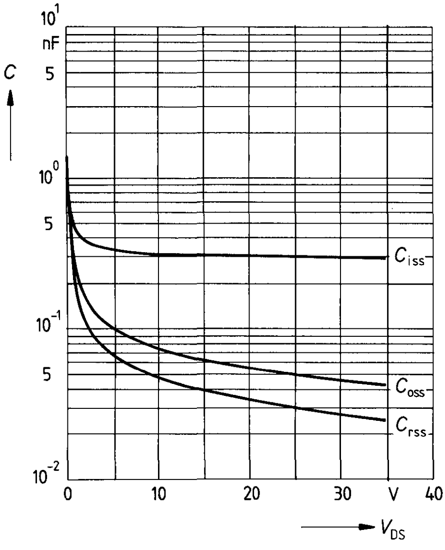
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



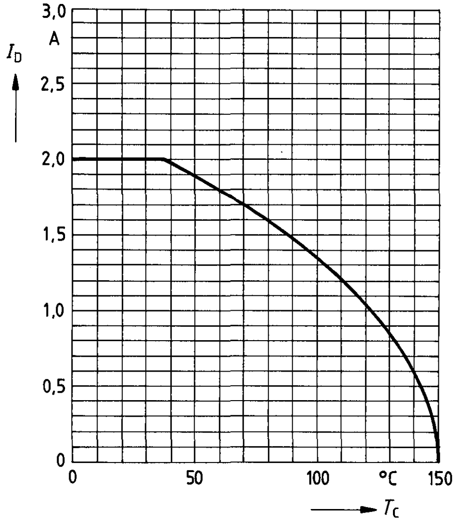
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



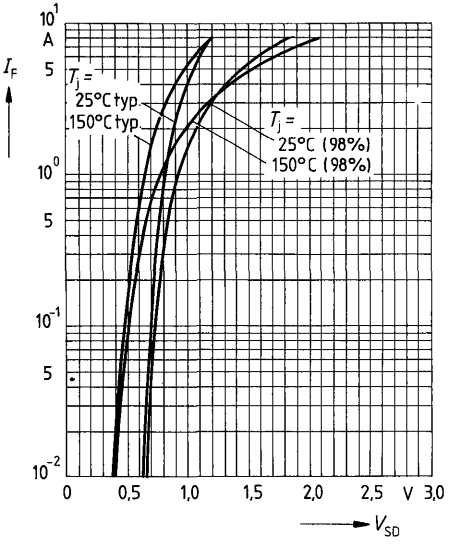
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



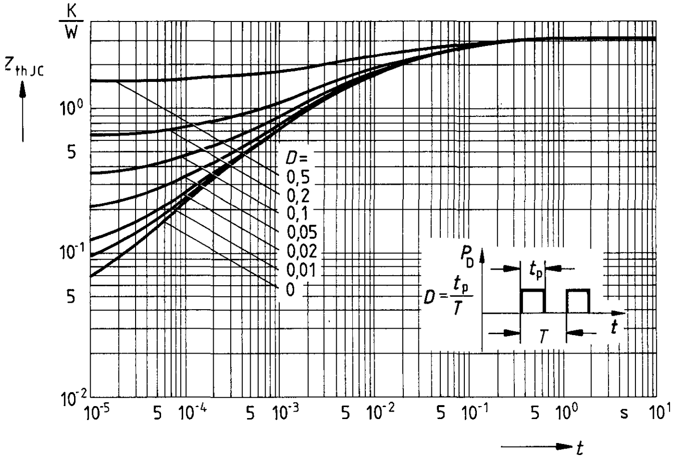
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



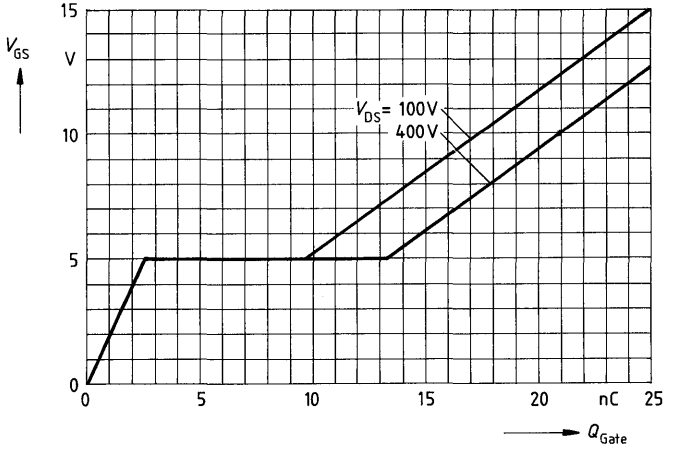
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



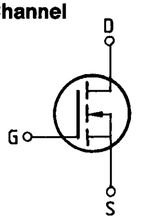
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 3{,}6A$



Main ratings

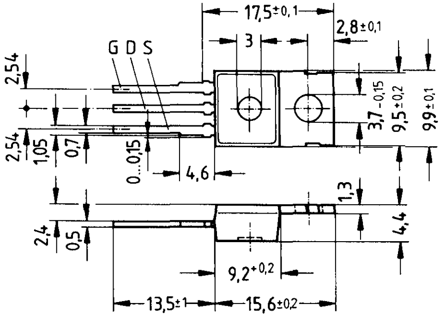
Drain-source voltage V_{DS} **= 400 V**
Continuous drain current I_D **= 3 A**
Drain-source on-resistance $R_{DS(on)}$ **= 1,8 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
S BUZ 76	C67078-A1315-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	3	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	12	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

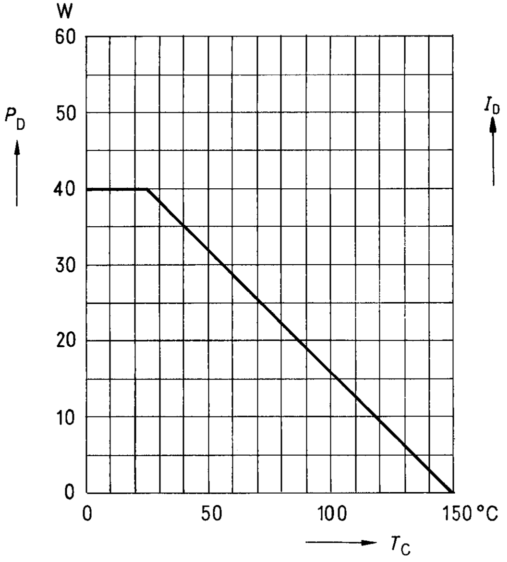
 S Preferred Type

Electrical characteristics

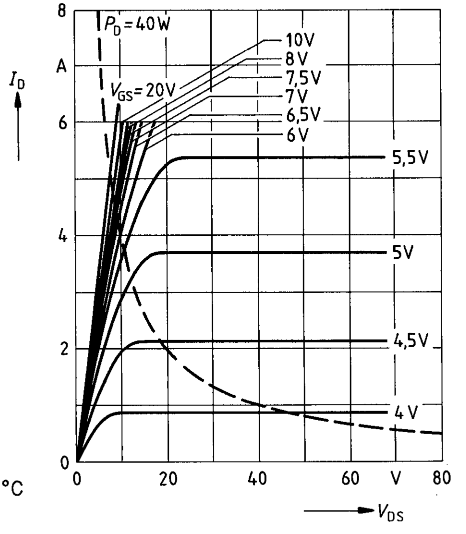
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,65	1,8	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,1	2,5	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	300	500	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	50	80		
Reverse transfer capacitance	C_{rss}	–	35	60		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	50	65		
	t_f	–	30	40		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	3,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	12		
Diode forward on-voltage	V_{SD}	–	1,1	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	300	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	2,5	–	µC	

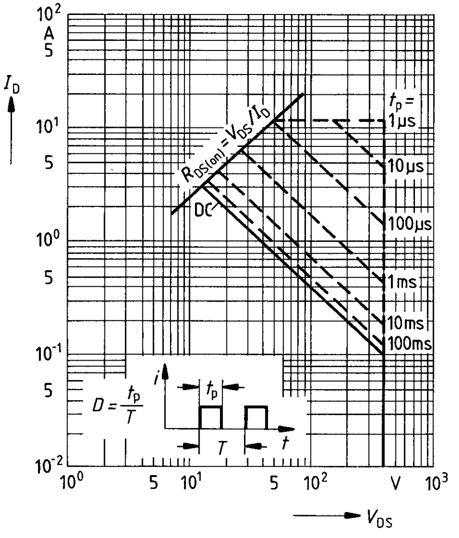
Power dissipation $P_D = f(T_C)$



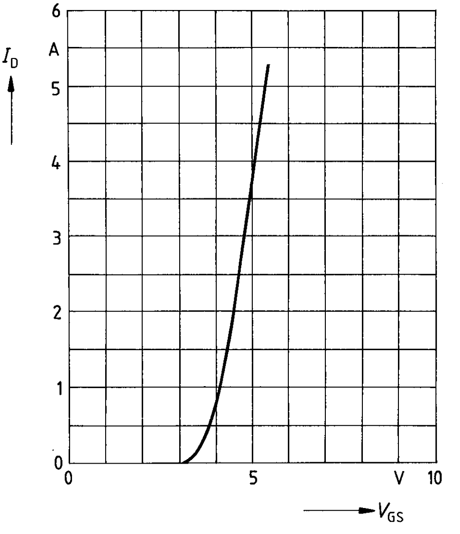
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



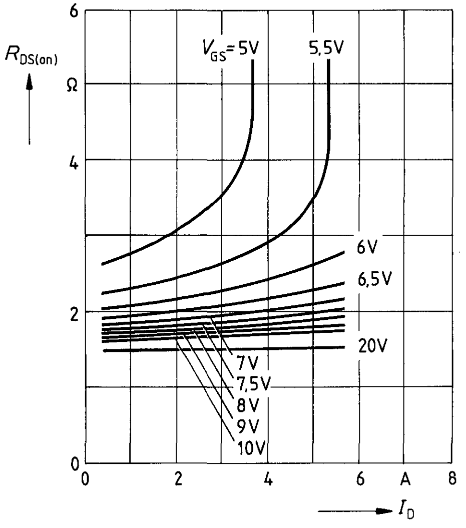
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



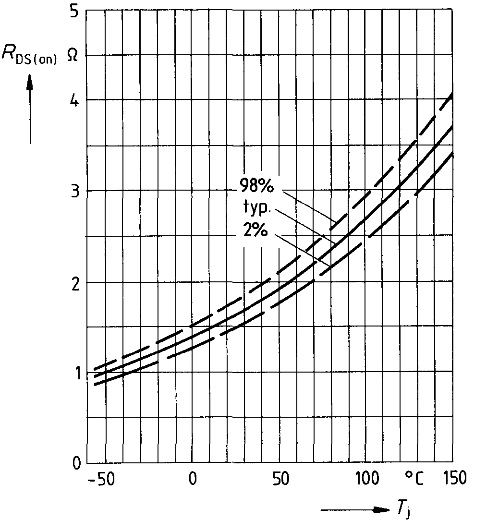
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



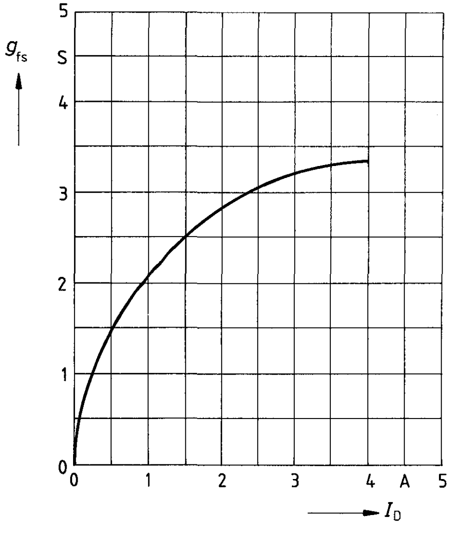
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



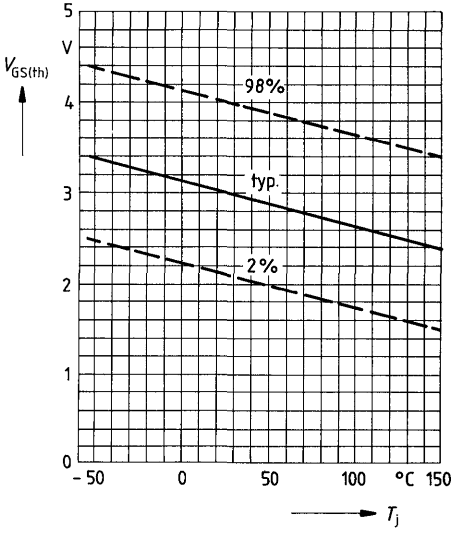
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 1,5A, V_{GS} = 10V
(spread)



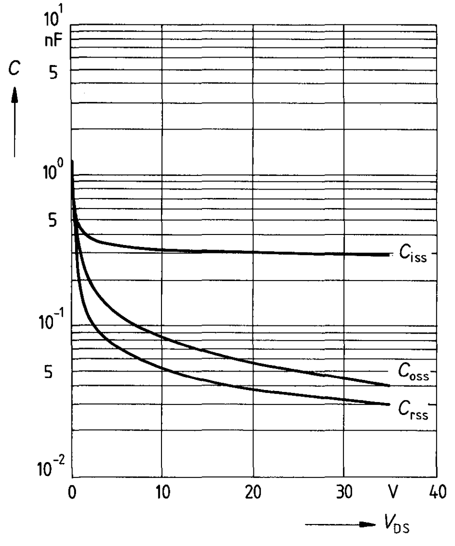
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



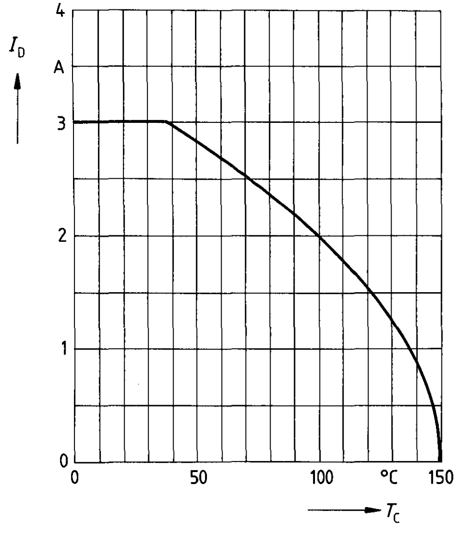
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



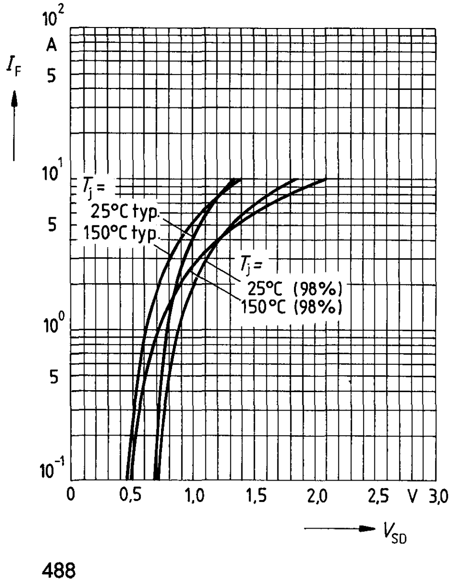
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



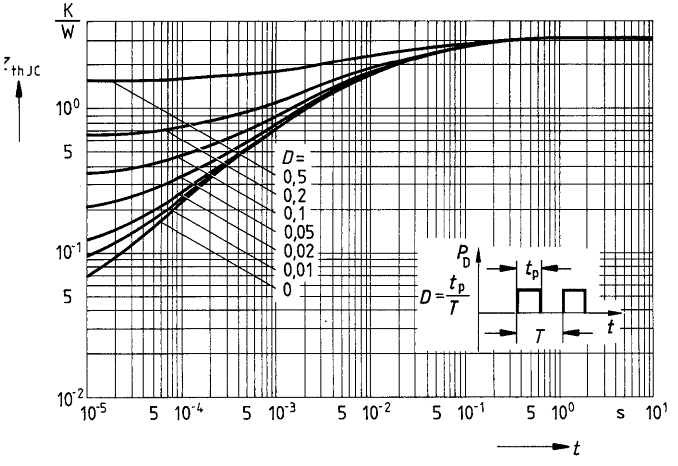
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



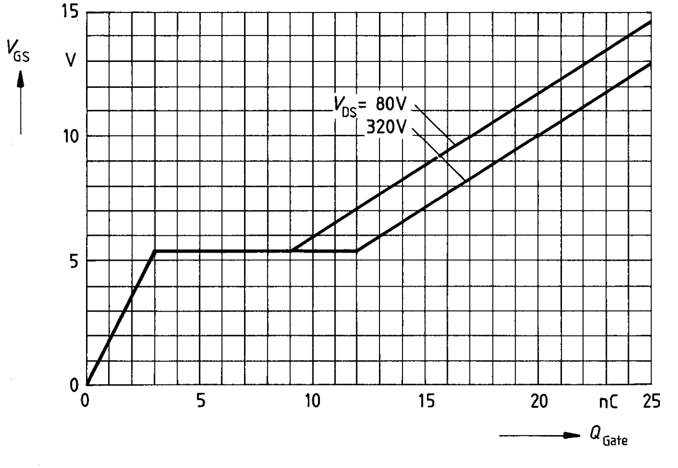
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



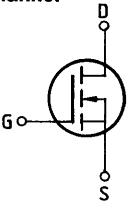
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 4{,}5A$



Main ratings

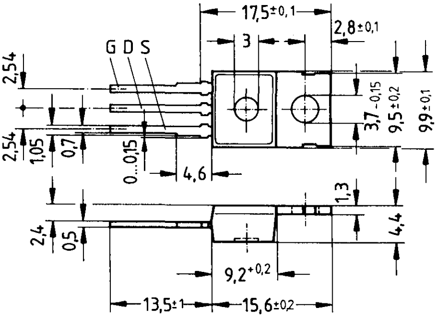
N-Channel

Drain-source voltage V_{DS} **= 400 V**
Continuous drain current I_D **= 2,6 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,5 Ω**



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
S BUZ 76 A	C67078-A1315-A3



Dimensions in mm

Maximum ratings

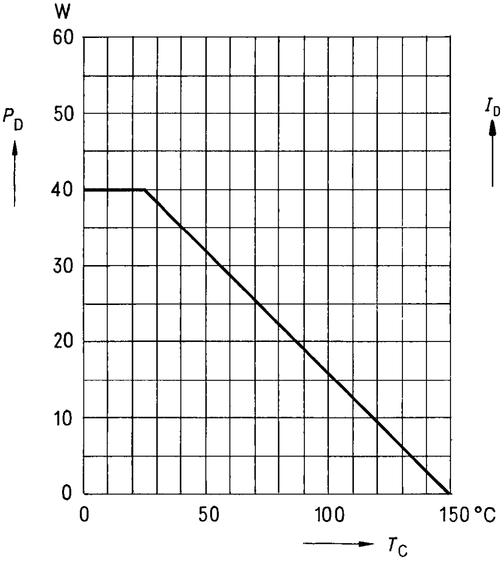
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,6	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	10	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤ 3,1	K/W	
Chip – ambient	$R_{th JA}$	≤ 75	K/W	

 S Preferred Type

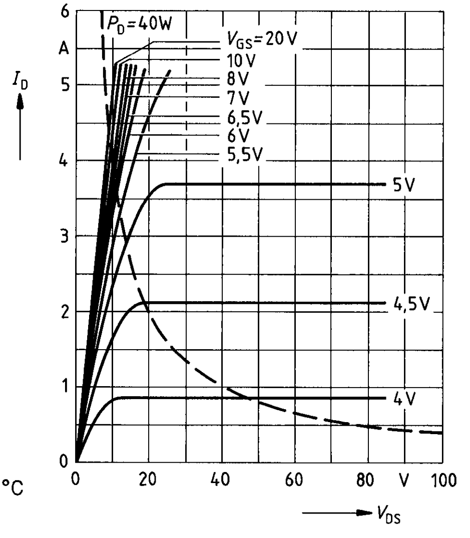
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	2,2	2,5	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,1	2,5	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	300	500	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	50	80		
Reverse transfer capacitance	C_{rss}	–	35	60		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 2,4A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	50	65		
	t_f	–	30	40		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,6	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	10		
Diode forward on-voltage	V_{SD}	–	1,1	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	300	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	2,5	–	µC	

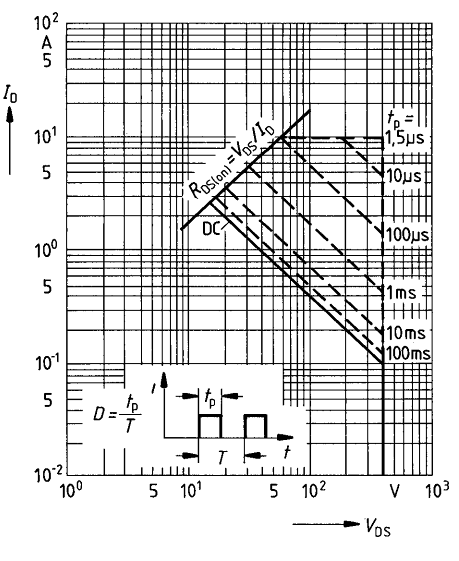
Power dissipation $P_D = f(T_C)$



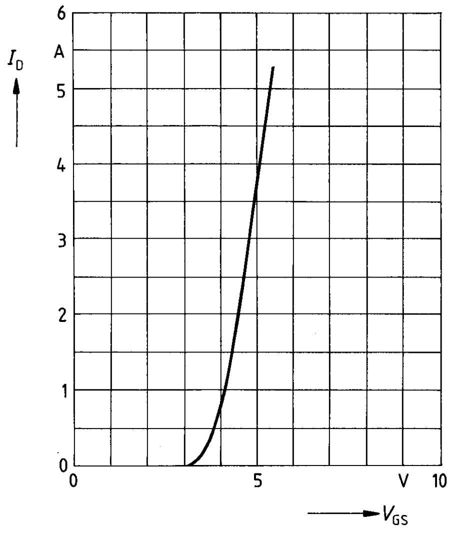
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



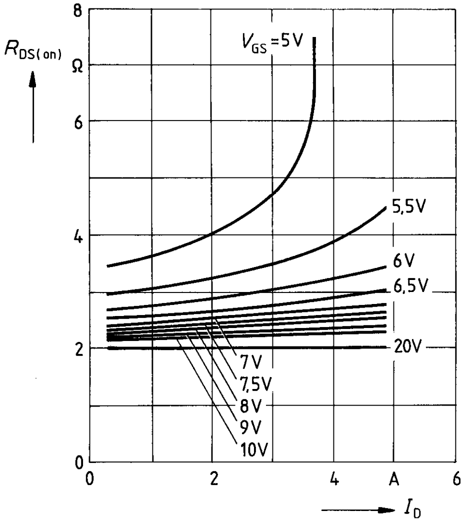
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



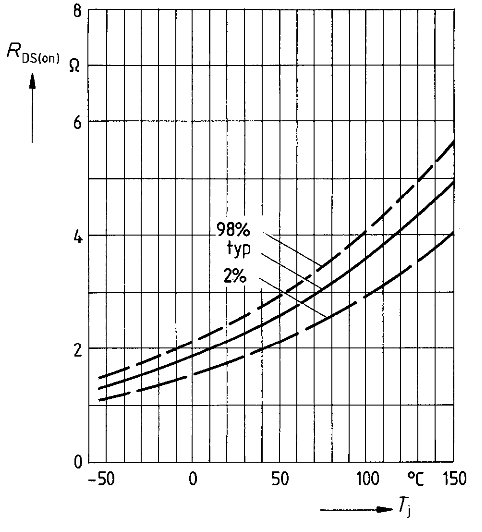
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\text{V}$, $T_j = 25\,°C$



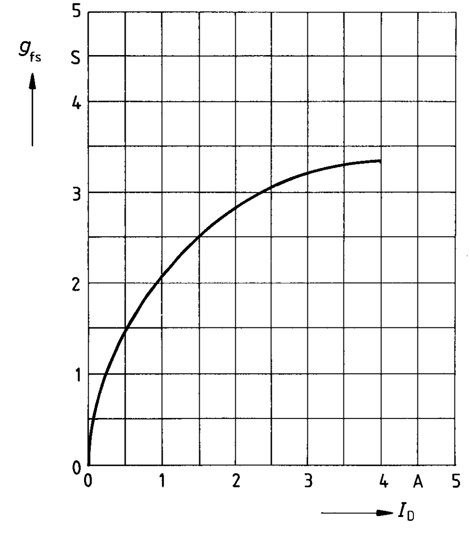
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



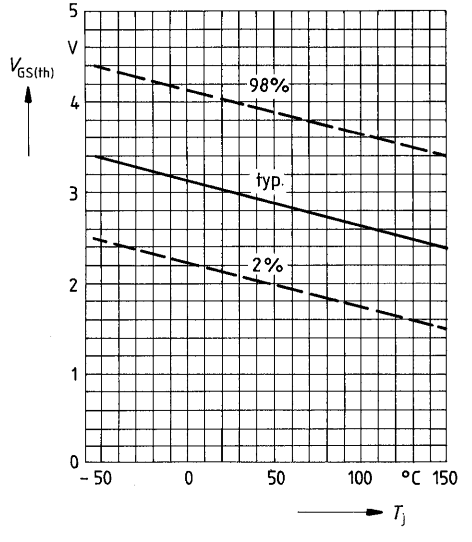
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 1,5A, V_{GS} = 10V
(spread)



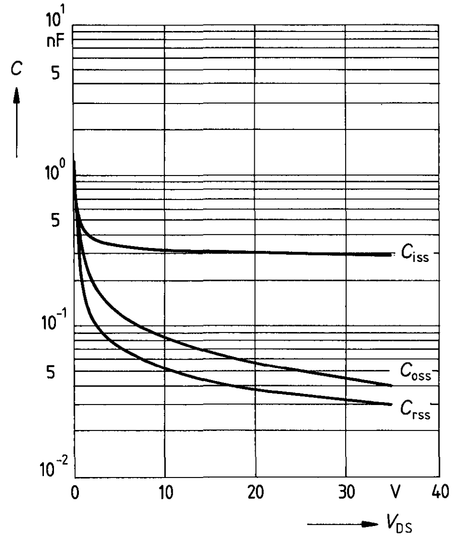
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



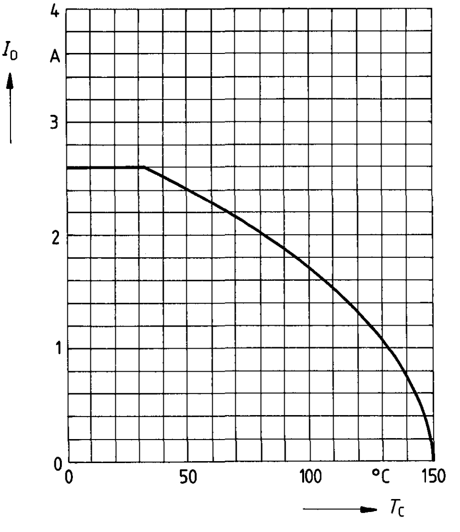
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



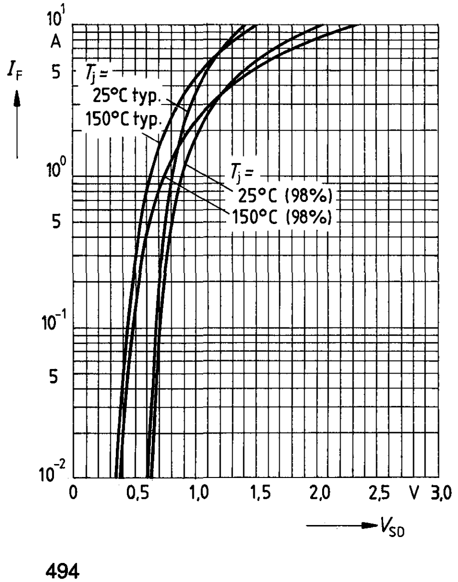
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



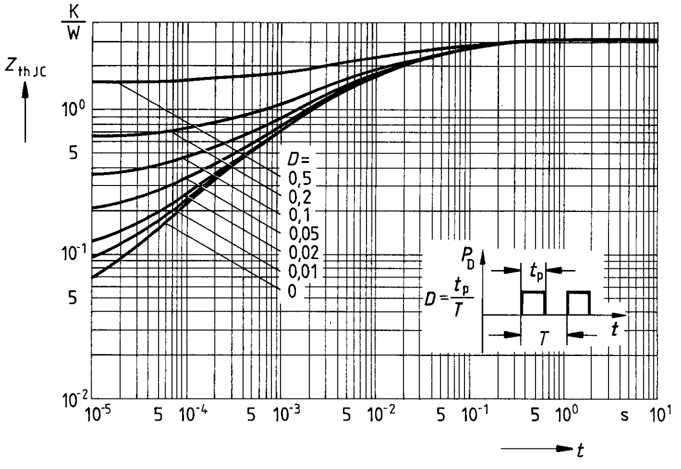
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



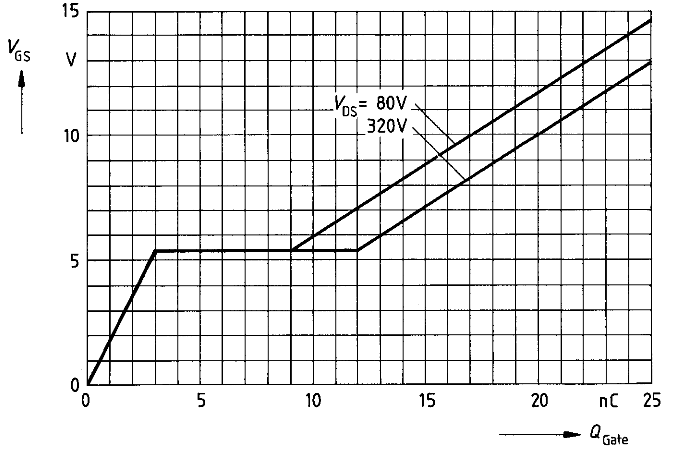
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



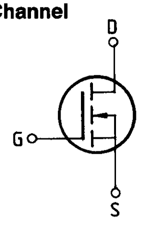
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 4{,}5A$



Main ratings

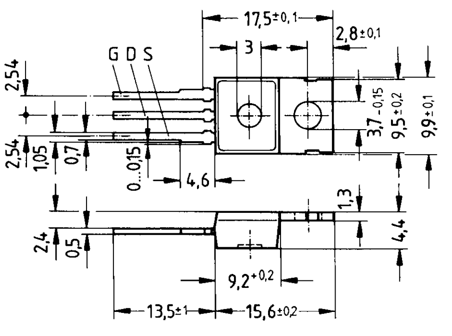
Drain-source voltage V_{DS} **= 800 V**
Continuous drain current I_D **= 1,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 8,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
BUZ 78	C67078-A1318-A2



Dimensions in mm

Maximum ratings

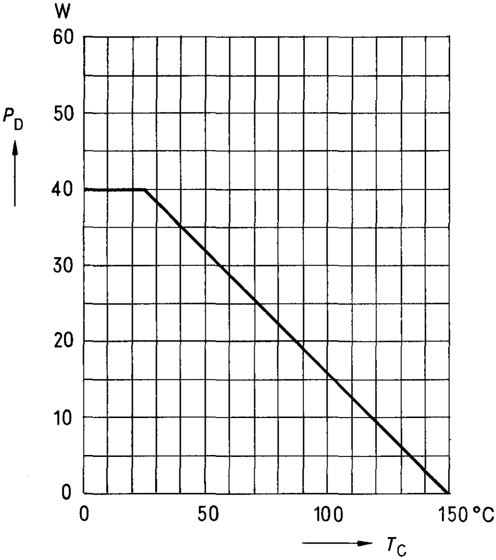
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	1,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	6,0	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

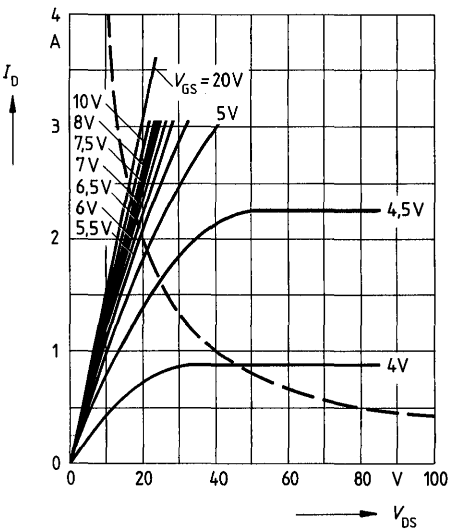
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	μA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	7,0	8,0	Ω	V_{GS} = 10V I_D = 1,0A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	2,3	–	S	V_{DS} = 25V I_D = 1,0A
Input capacitance	C_{iss}	–	450	750	pF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	42	70		
Reverse transfer capacitance	C_{rss}	–	15	30		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = 30V I_D = 1,7A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	25	40		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	50	65		
	t_f	–	30	40		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	1,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	6,0		
Diode forward on-voltage	V_{SD}	–	1,0	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	230	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/μs V_R = 100V
Reverse recovery charge	Q_{rr}	–	1,9	–	μC	

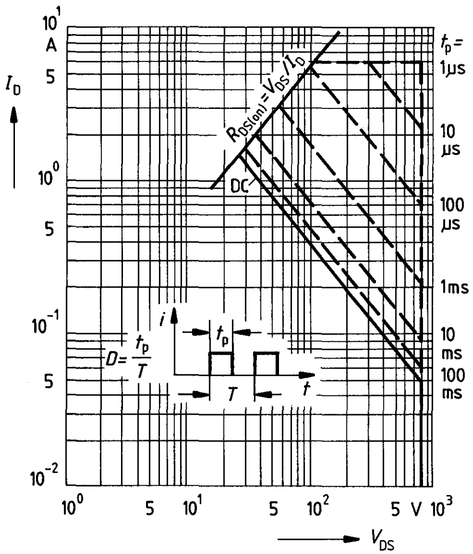
Power dissipation $P_D = f(T_C)$



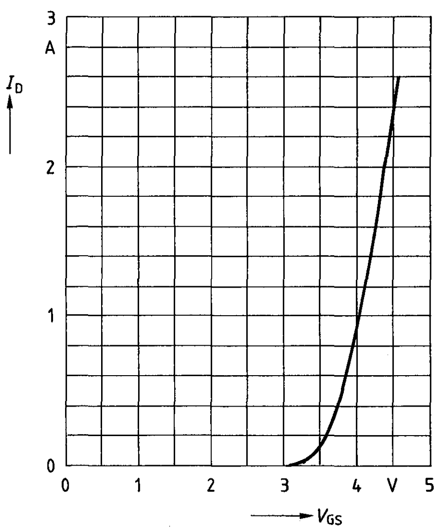
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 μs pulse test,
$T_j = 25\,°C$



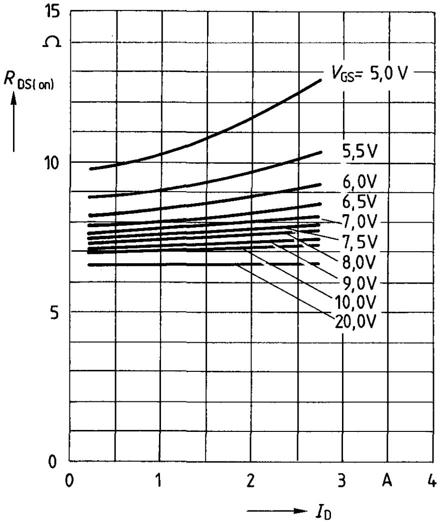
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



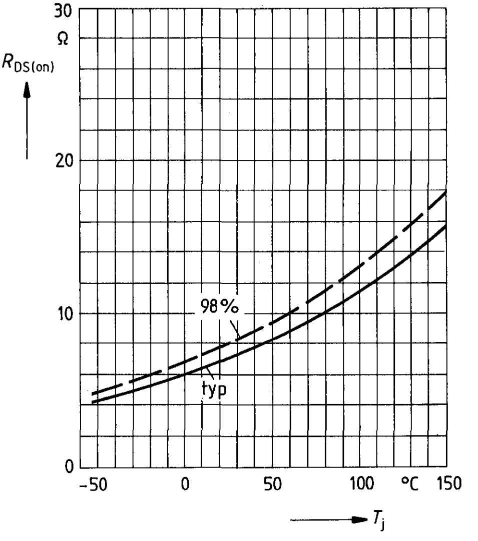
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 μs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



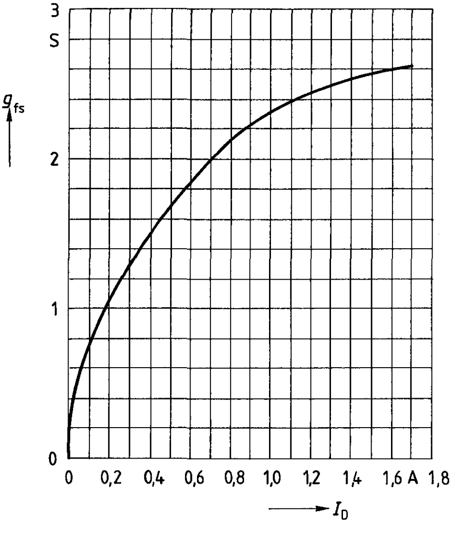
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



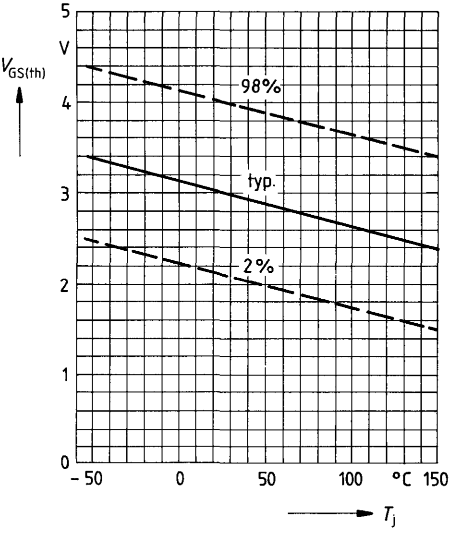
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 1,5A, V_{GS} = 10V
(spread)



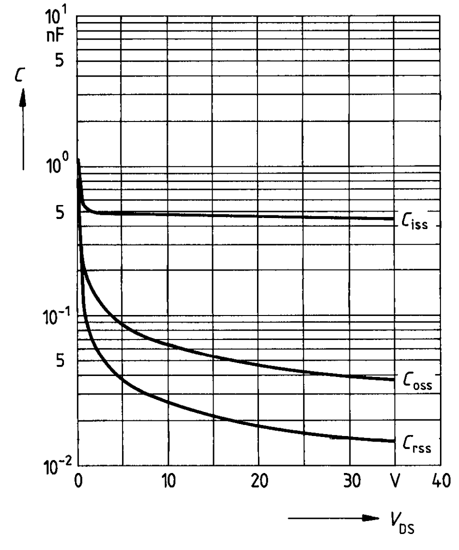
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



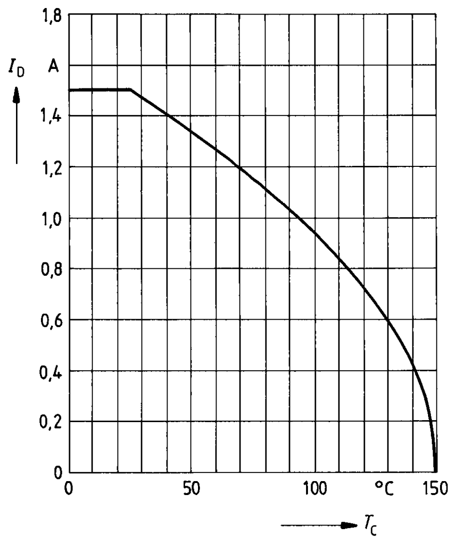
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



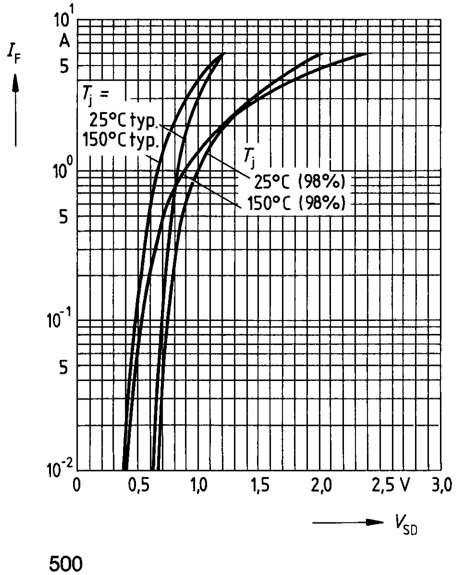
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



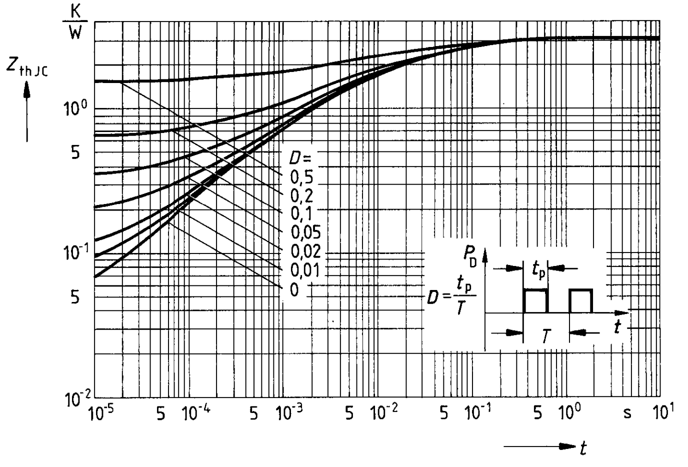
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



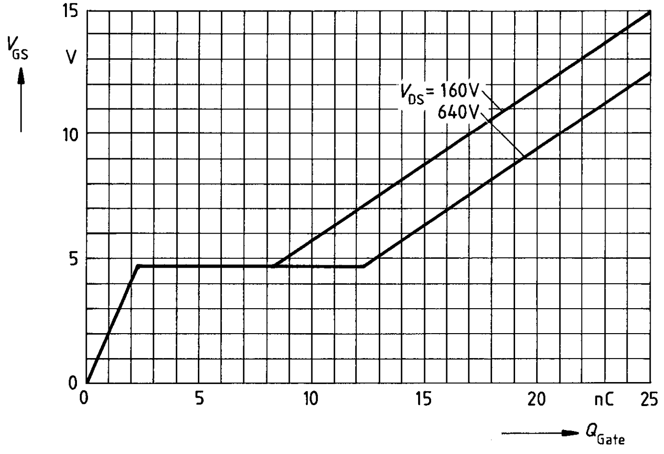
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



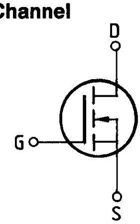
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 2{,}25A$



Main ratings

Drain-source voltage	V_{DS}	**= 800 V**
Continuous drain current	I_D	**= 2,6 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 4,0 Ω**

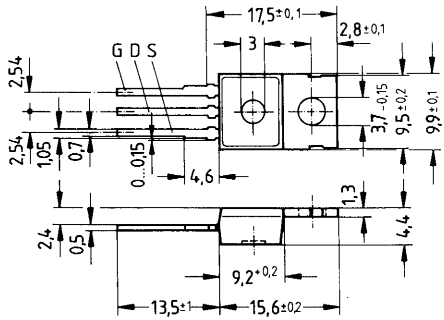
N-Channel



Description SIPMOS, N-channel, enhancement mode

Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 80	C67078-A1309-A2



Dimensions in mm

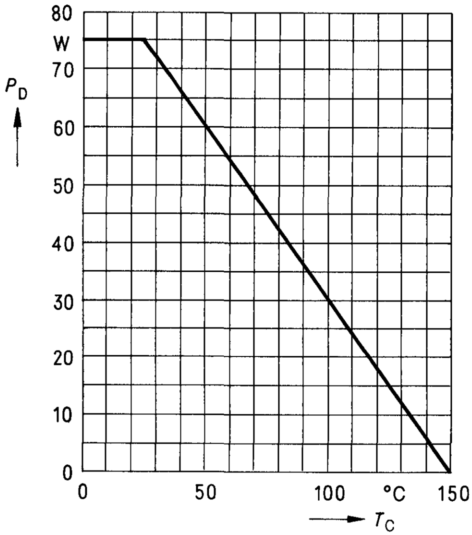
Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,6	A	T_C = 50 °C
Pulsed drain current	I_{Dpuls}	10	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤ 1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤ 75	K/W	

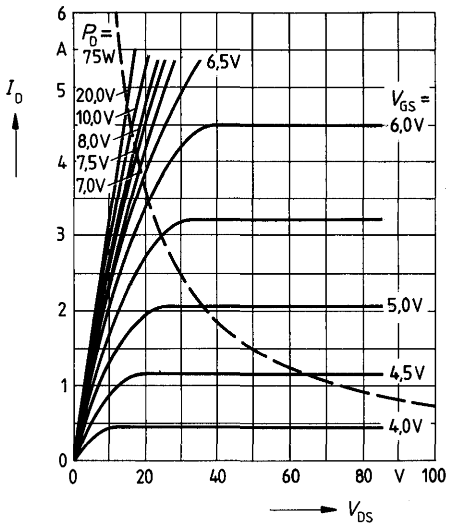
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	3,5	4,0	Ω	V_{GS} = 10V I_D = 1,7A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	1,8	–	S	V_{DS} = 25V I_D = 1,7A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	90	150	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,1A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,6	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	10		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

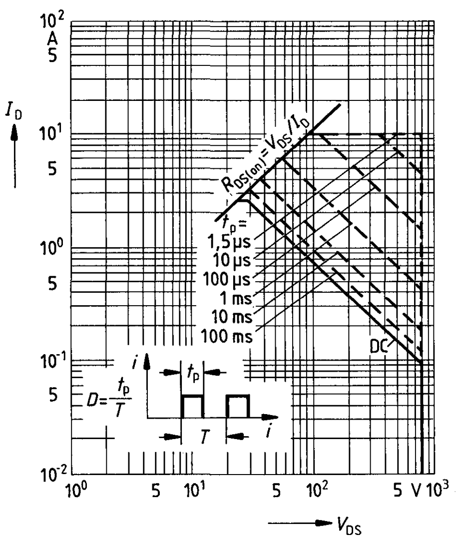
Power dissipation $P_D = f(T_C)$



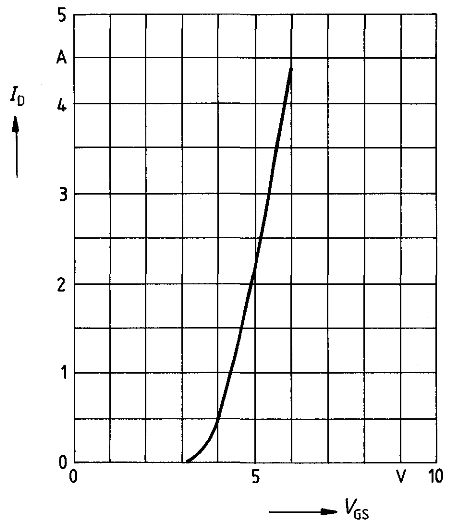
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25$ °C



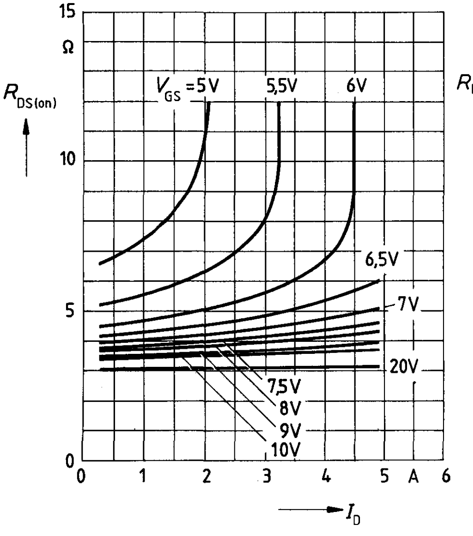
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25$ °C



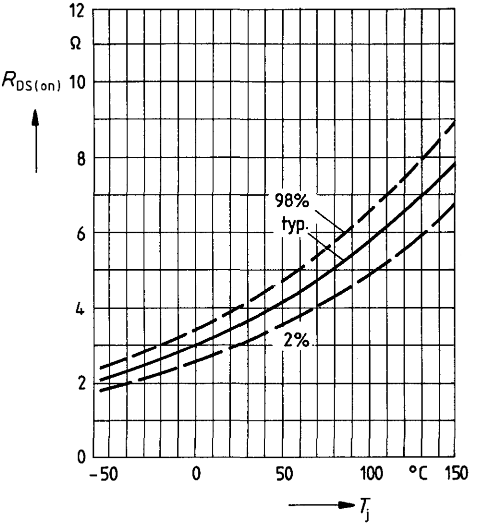
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25$V, $T_j = 25$ °C



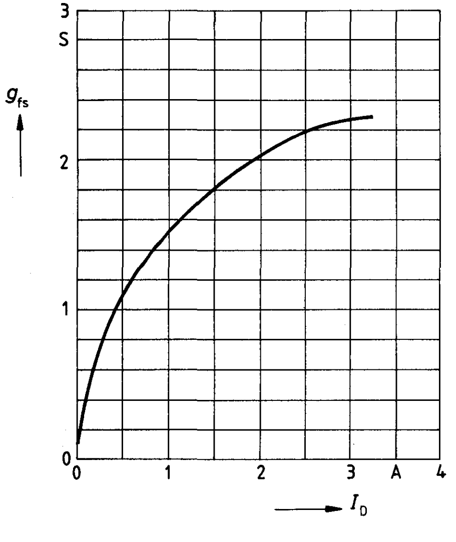
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



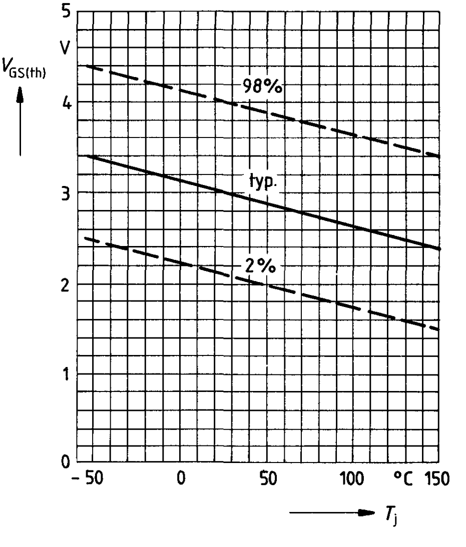
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 1{,}7\,A$, $V_{GS} = 10\,V$
(spread)



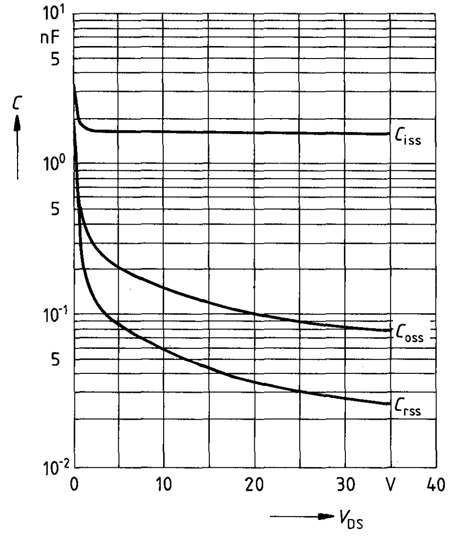
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25\,V$, $T_j = 25\,°C$



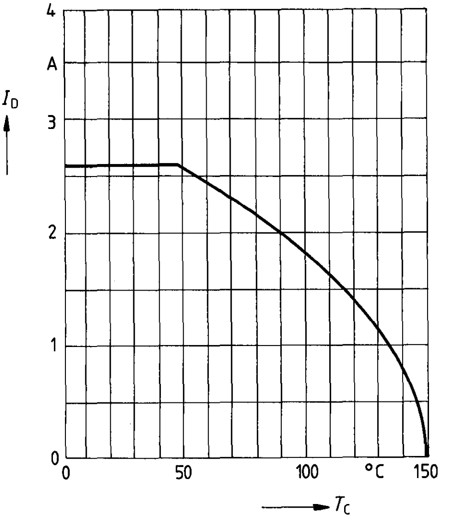
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1\,mA$
(spread)



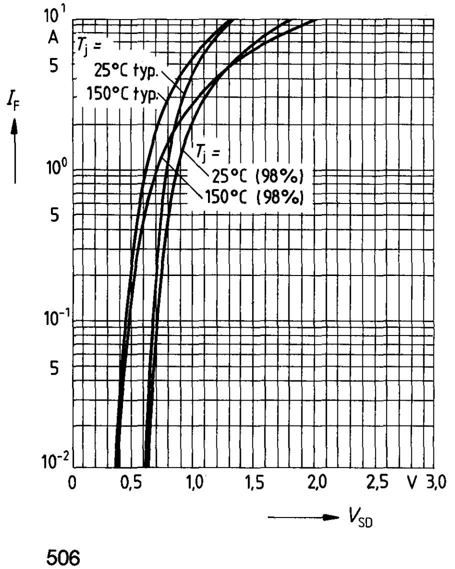
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



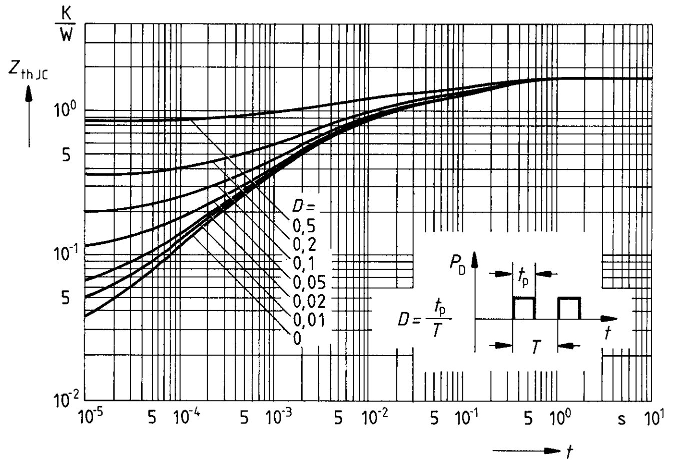
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



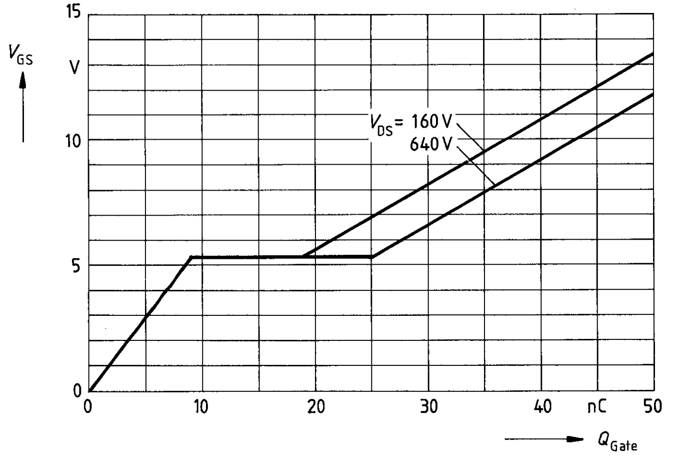
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



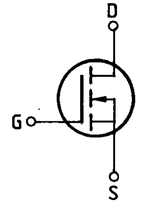
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 5A$



Main ratings

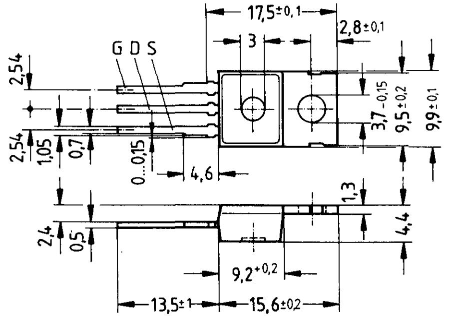
Drain-source voltage V_{DS} = **800 V**
Continuous drain current I_D = **3 A**
Drain-source on-resistance $R_{DS(on)}$ = **3 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 80 A	C67078-A1309-A3



Dimensions in mm

Maximum ratings

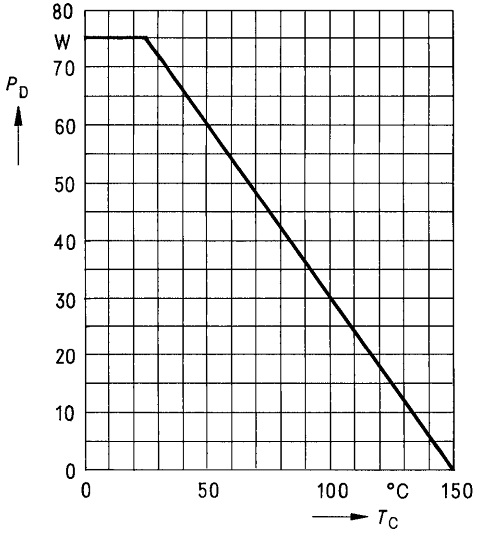
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	3	A	T_C = 50 °C
Pulsed drain current	I_{Dpuls}	12	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

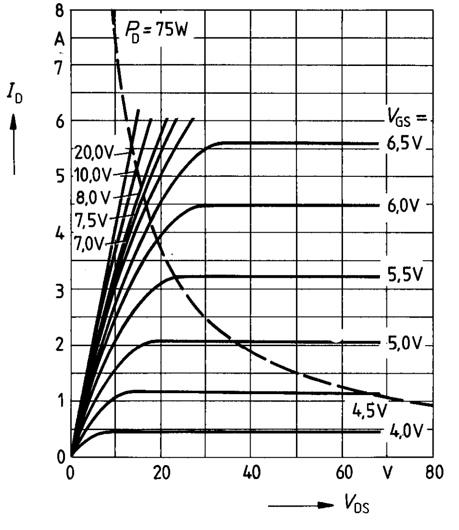
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	2,7	3,0	Ω	V_{GS} = 10V I_D = 1,7A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	1,8	–	S	V_{DS} = 25V I_D = 1,7A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	90	150	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	3,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	12		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

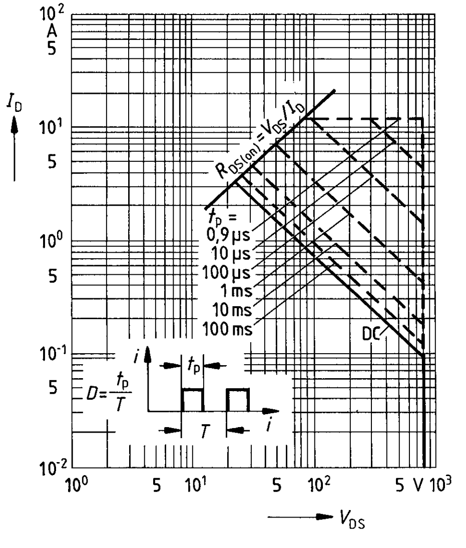
Power dissipation $P_D = f(T_C)$



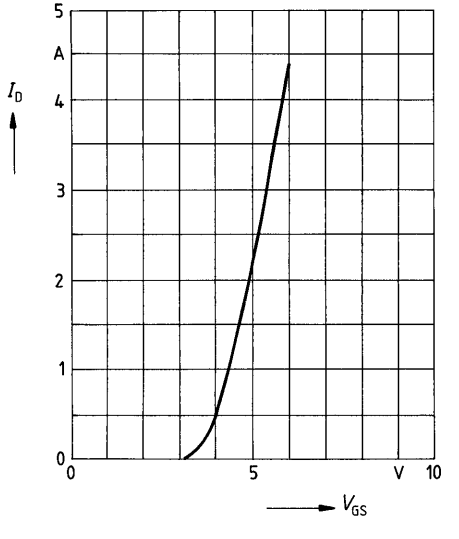
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



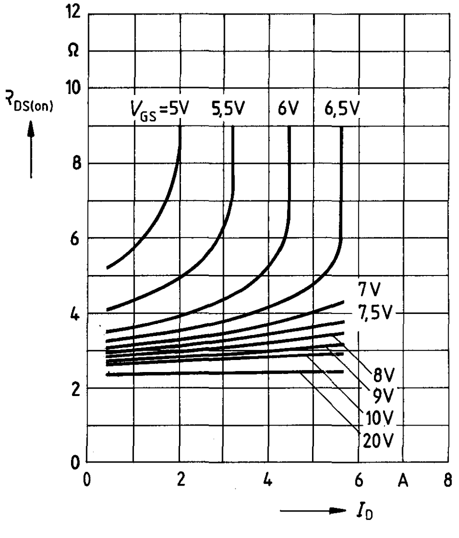
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



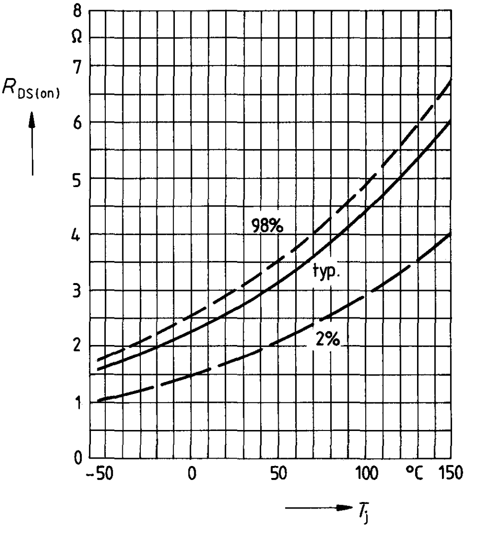
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



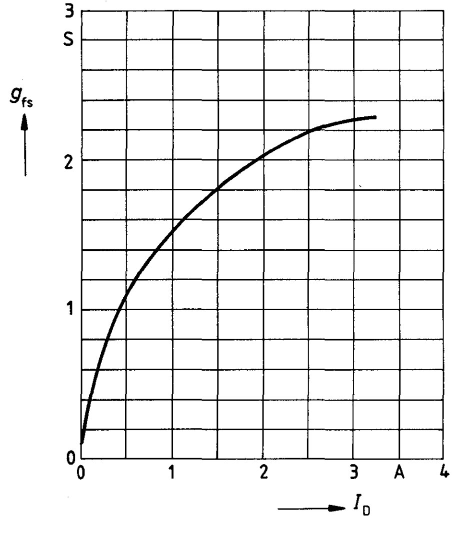
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



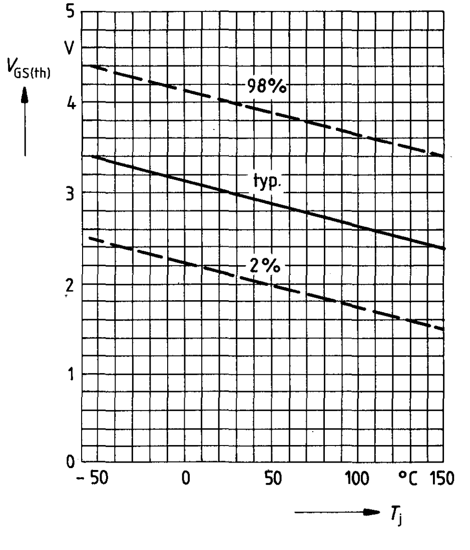
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 1{,}7A$, $V_{GS} = 10V$
(spread)



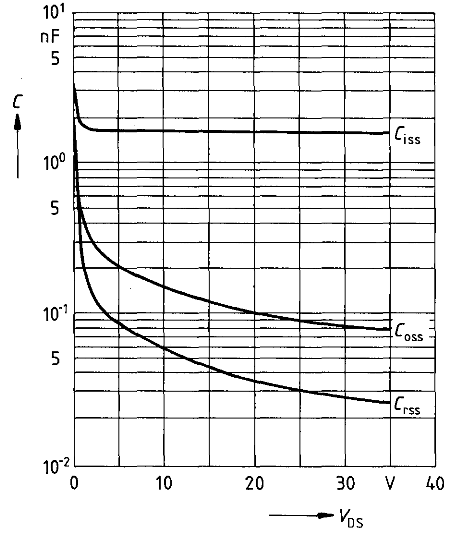
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



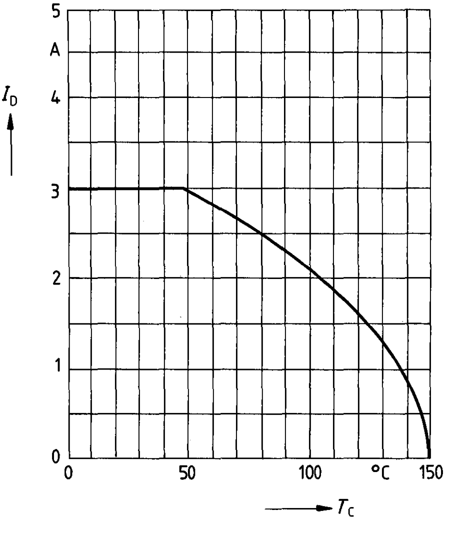
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



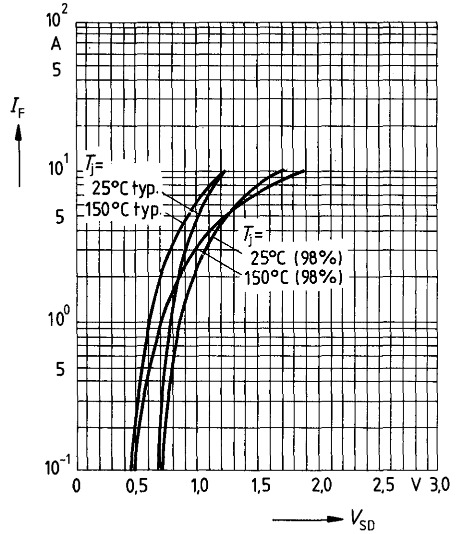
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



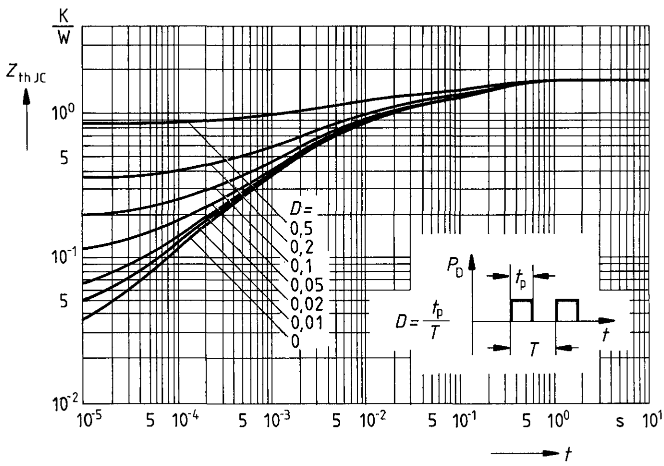
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



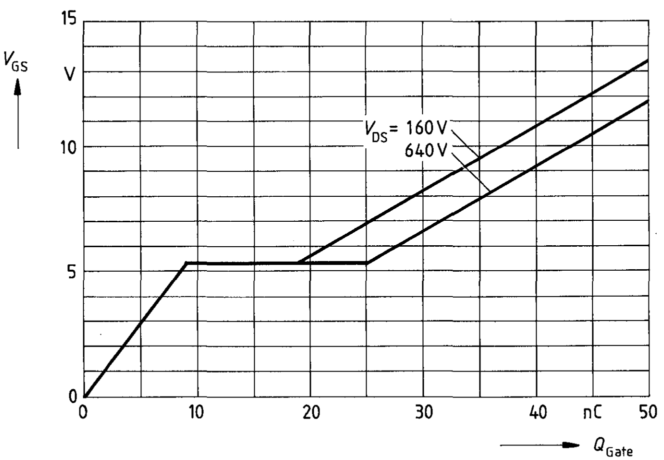
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

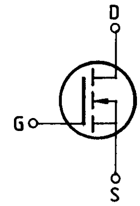


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 5A$



Main ratings

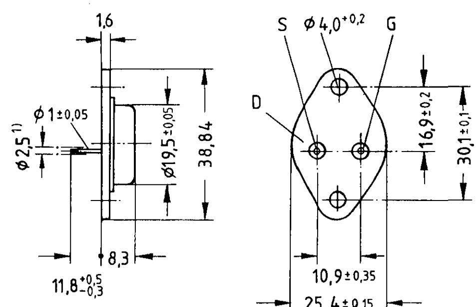
N-Channel



Drain-source voltage	V_{DS}	**= 800 V**
Continuous drain current	I_D	**= 2,9 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 4,0 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 83	C67078-A1012-A2



1) max. bending area

Dimensions in mm

Maximum ratings

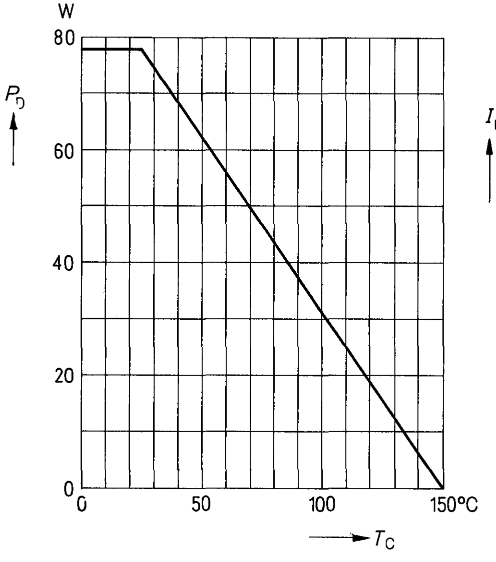
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,9 A	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	11	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,6	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

Electrical characteristics

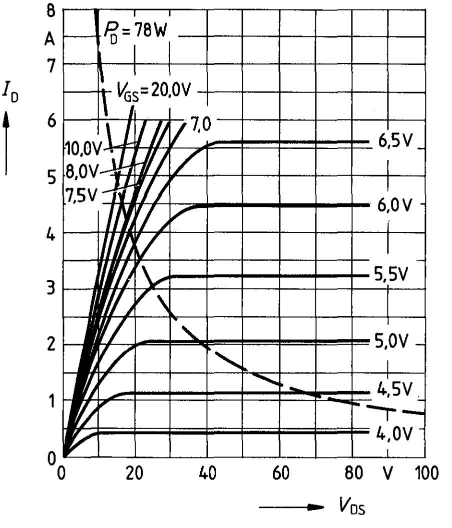
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	3,5	4,0	Ω	V_{GS} = 10V I_D = 1,7A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	1,8	–	S	V_{DS} = 25V I_D = 1,7A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	90	150	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,1A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,9	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	11		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

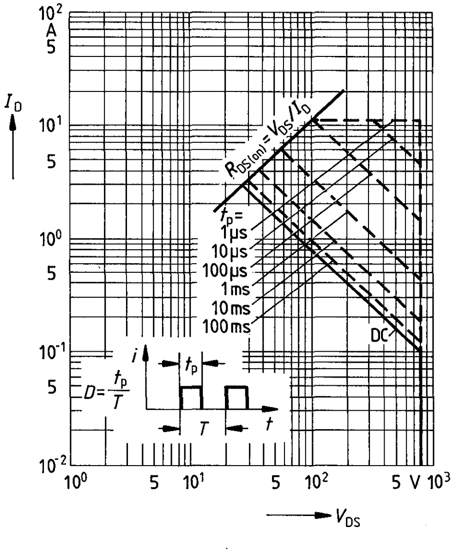
Power dissipation $P_D = f(T_C)$



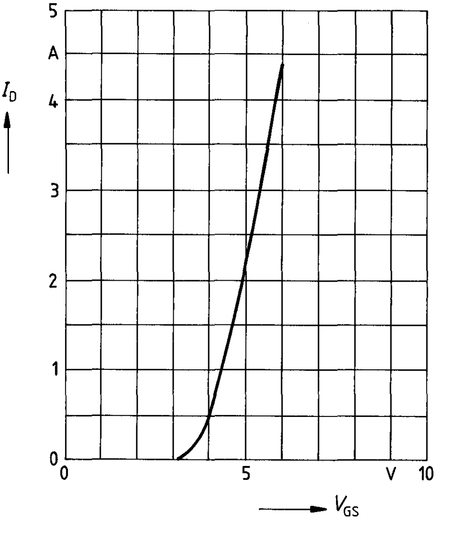
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



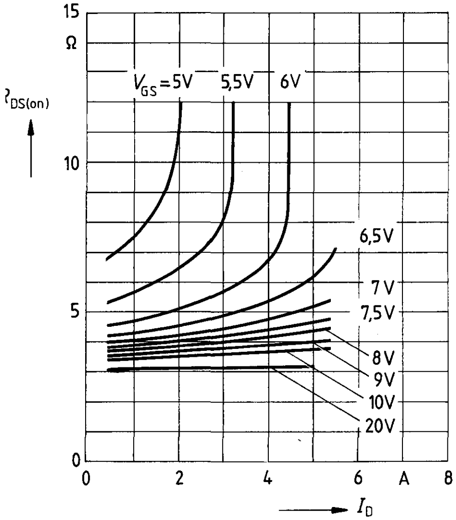
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



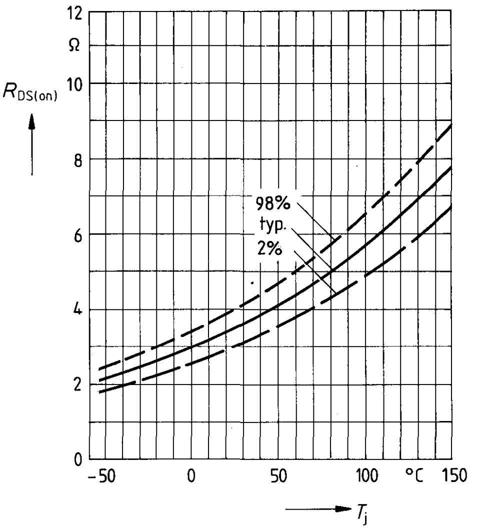
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



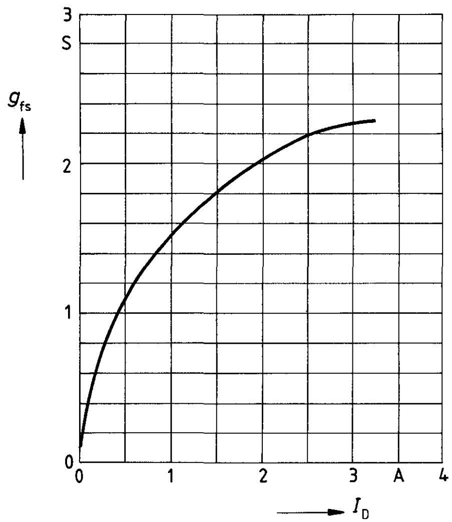
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



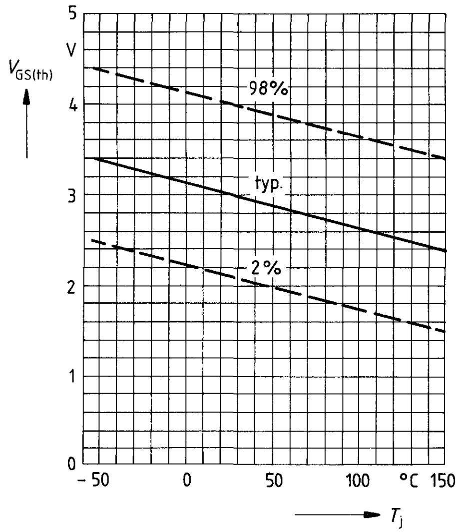
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 1{,}7A$, $V_{GS} = 10V$
(spread)



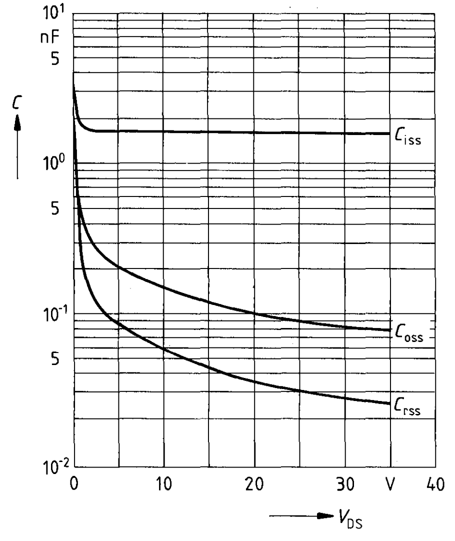
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



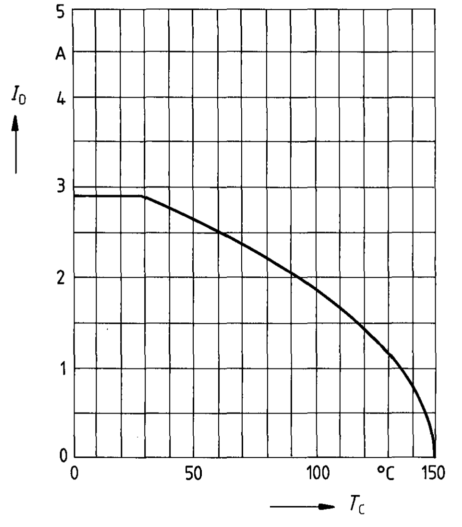
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



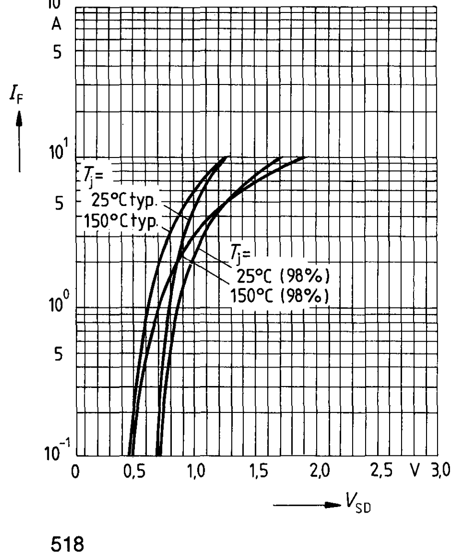
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



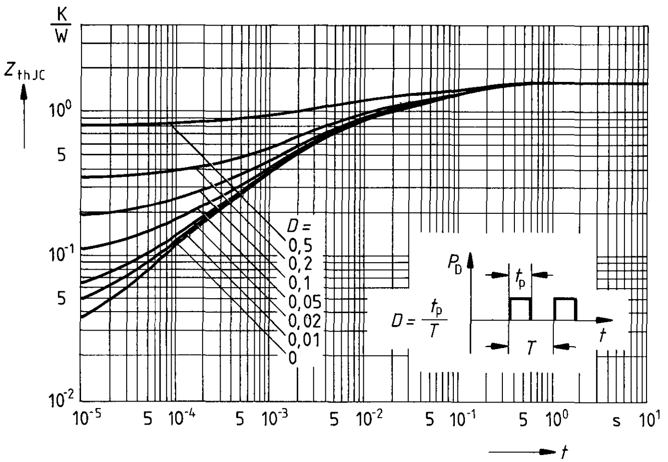
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



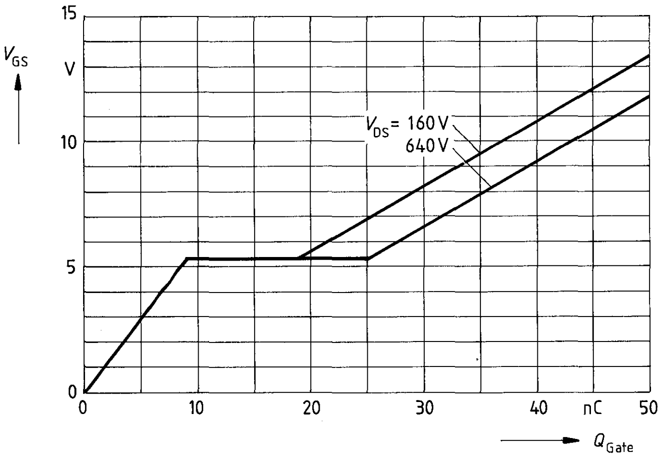
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu\text{s}$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



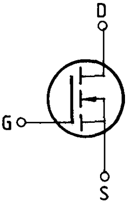
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 5A$



Main ratings

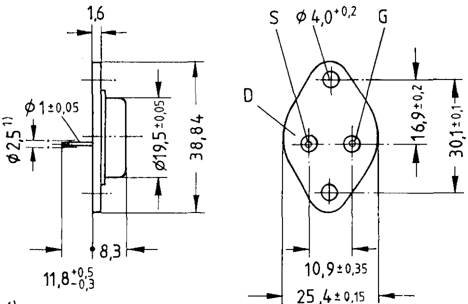
Drain-source voltage V_{DS} **= 800 V**
Continuous drain current I_D **= 3,4 A**
Drain-source on-resistance $R_{DS(on)}$ **= 3,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 83 A	C67078-A1012-A3



[1] max. bending area

Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	3,4	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	11	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	78	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,6	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

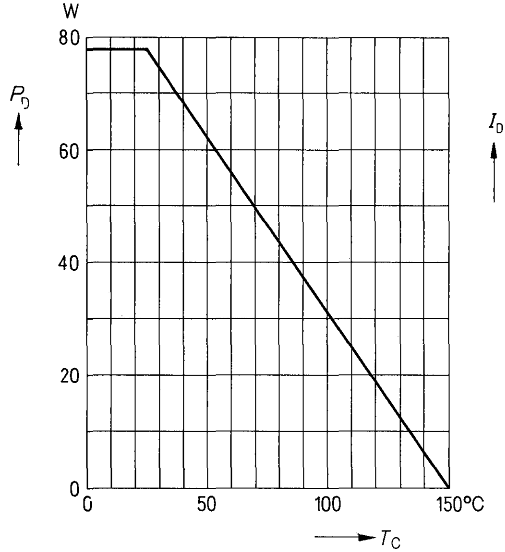
 S Preferred Type

Electrical characteristics

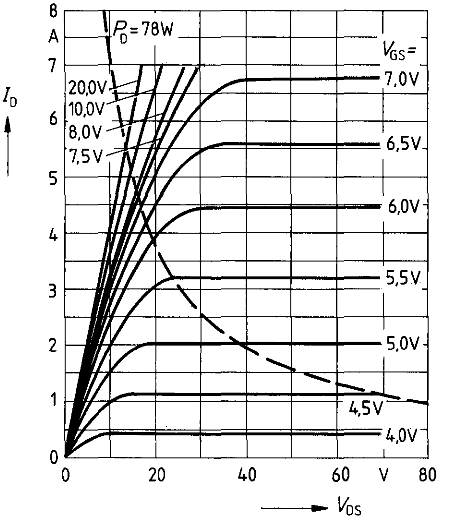
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	2,7	3,0	Ω	V_{GS} = 10V I_D = 1,7A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	1,8	–	S	V_{DS} = 25V I_D = 1,7A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	90	150	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	3,4	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	13		
Diode forward on-voltage	V_{SD}	–	1,1	1,35	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

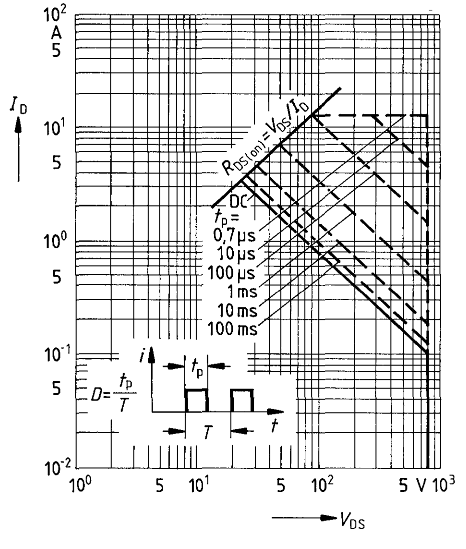
Power dissipation $P_D = f(T_C)$



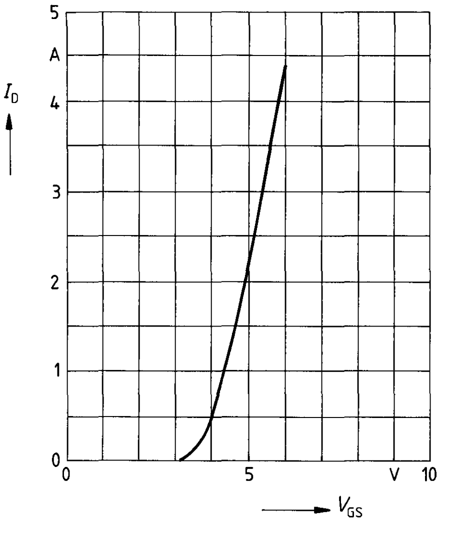
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



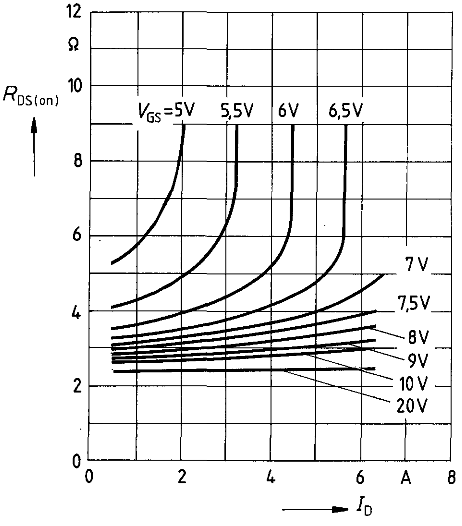
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



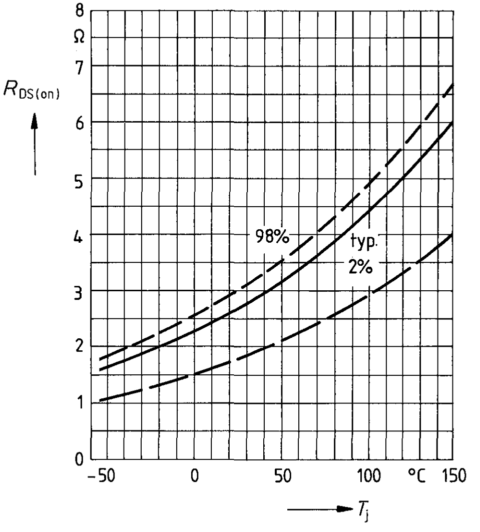
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



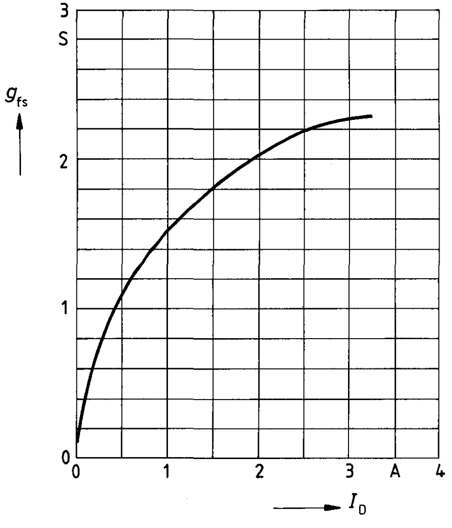
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



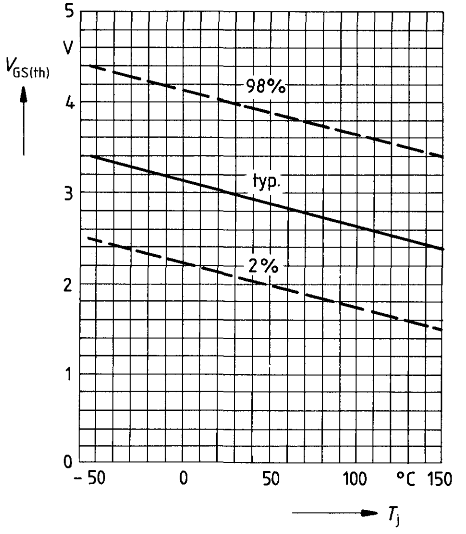
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 1{,}7A$, $V_{GS} = 10V$
(spread)



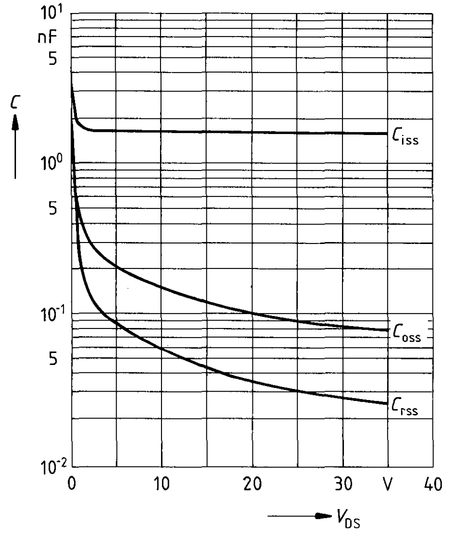
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



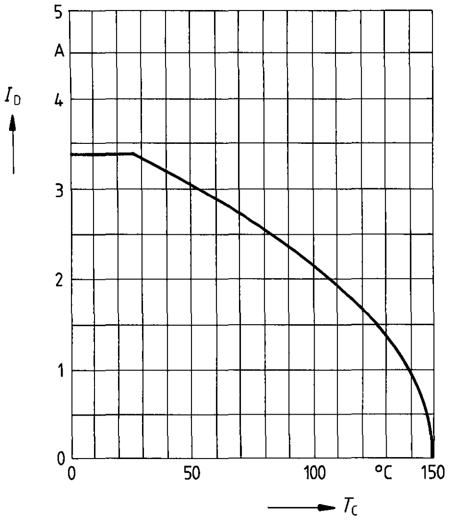
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



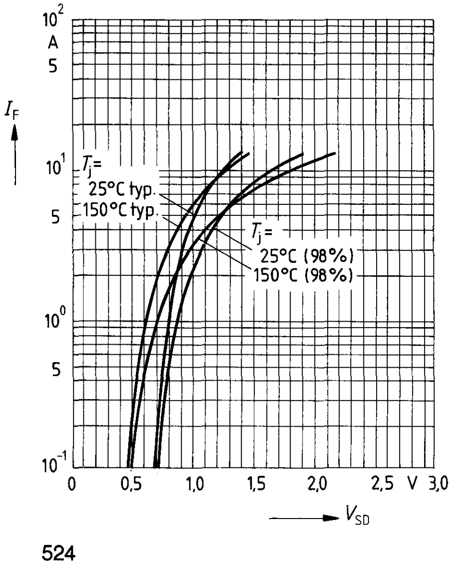
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



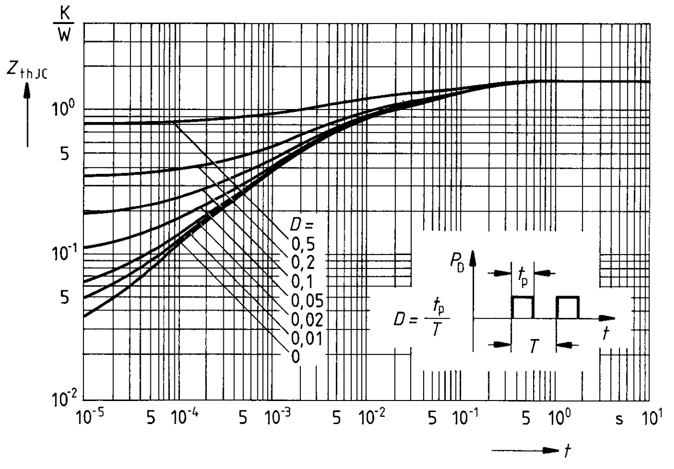
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



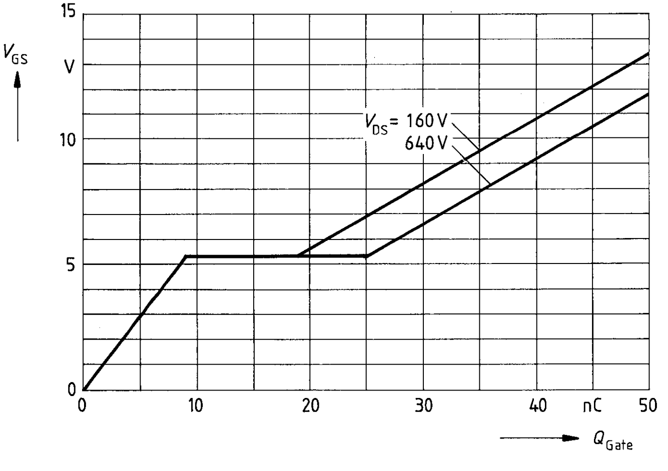
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



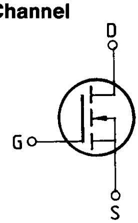
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 5A$



Main ratings

Drain-source voltage	V_{DS}	**= 800 V**
Continuous drain current	I_D	**= 5,3 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 2,0 Ω**

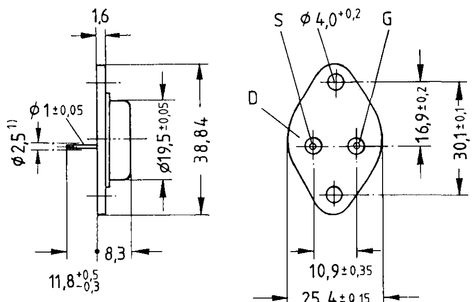
N-Channel



Description SIPMOS, N-channel, enhancement mode

Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 84	C67078-A1013-A2



1) max. bending area

Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,3	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	21	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

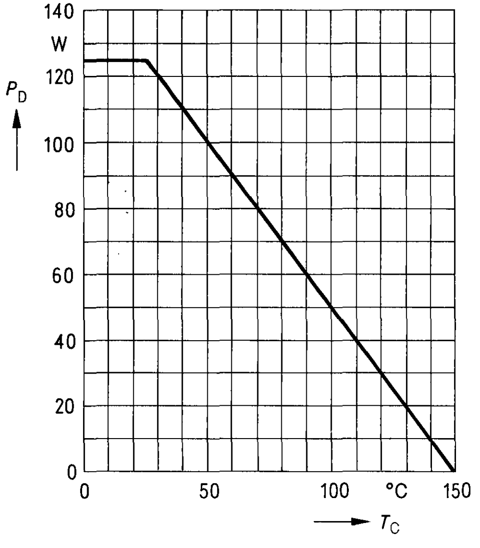
 S Preferred Type

Electrical characteristics

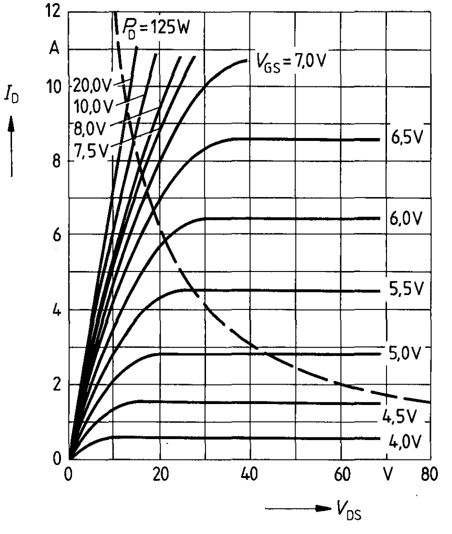
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,6	2,0	Ω	V_{GS} = 10V I_D = 3A
Dynamic ratings						
Forward transconductance	g_{fs}	1,8	3,0	–	S	V_{DS} = 25V I_D = 3A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	200	350	pF	
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,3	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	21		
Diode forward on-voltage	V_{SD}	–	1,0	1,45	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	25	–	µC	

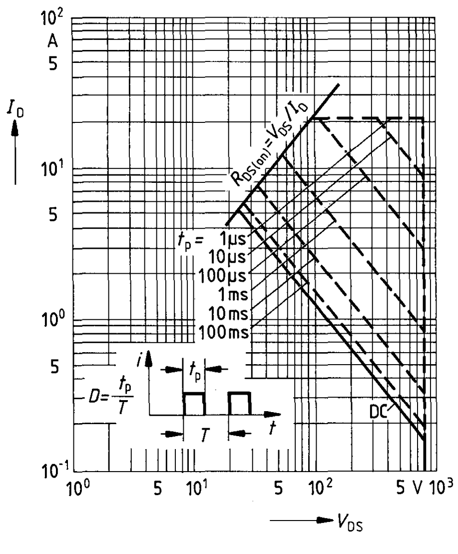
Power dissipation $P_D = f(T_C)$



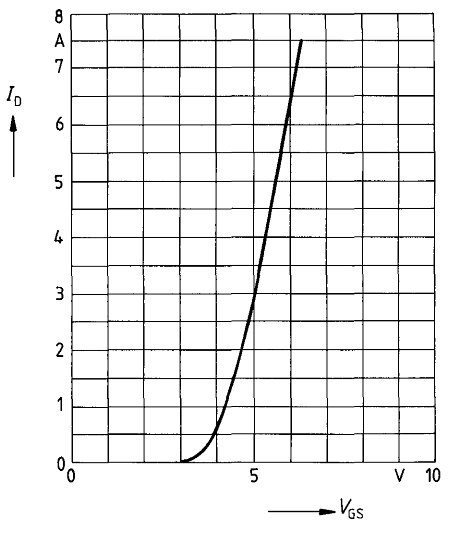
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



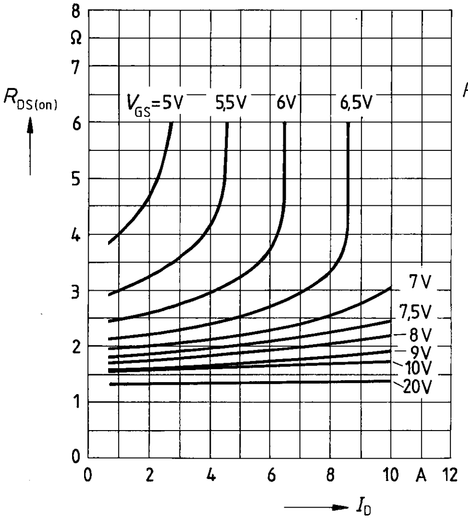
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



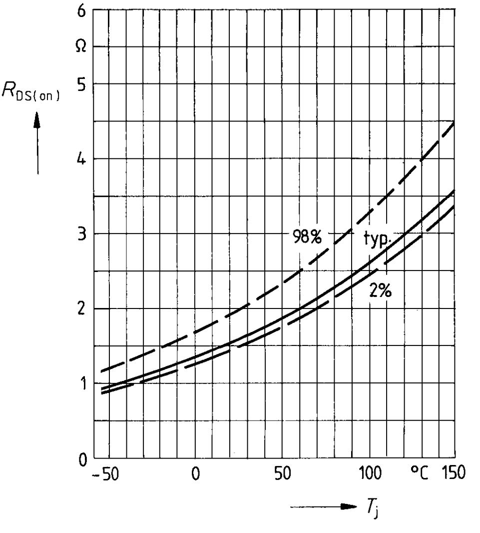
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



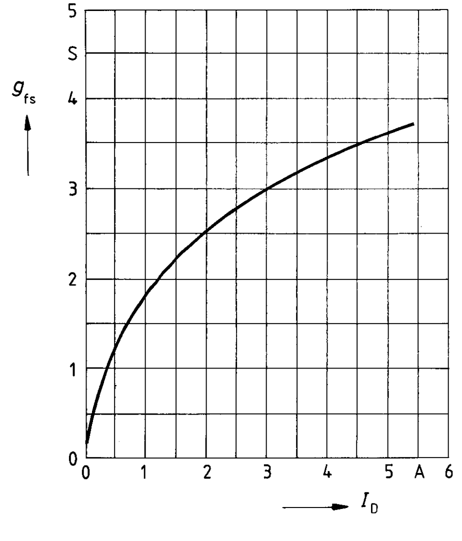
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25°C$



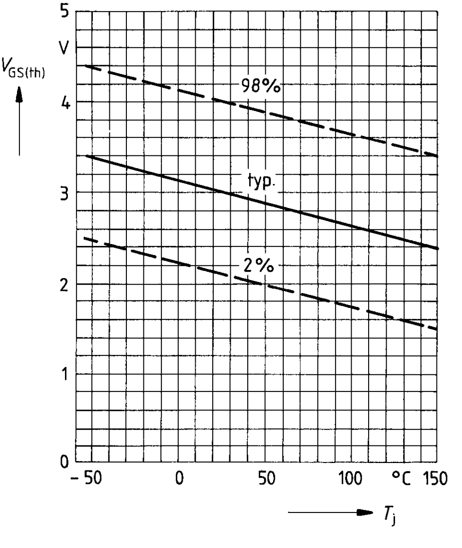
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 3A$, $V_{GS} = 10V$
(spread)



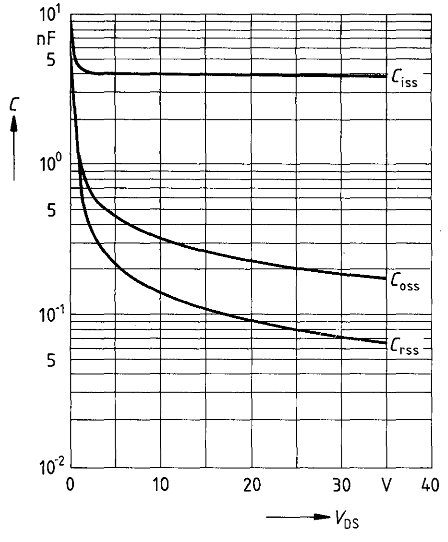
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25°C$



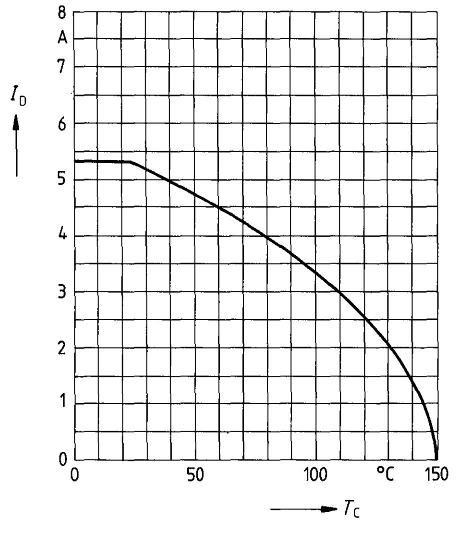
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



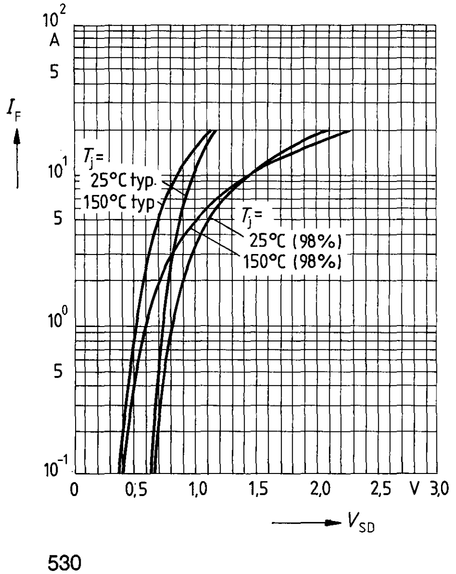
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



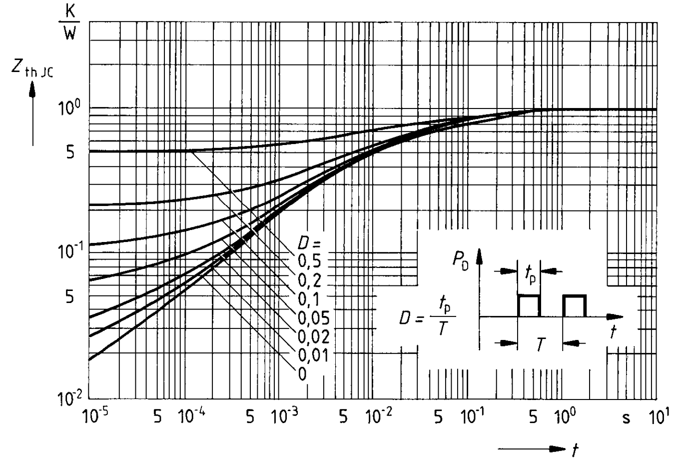
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



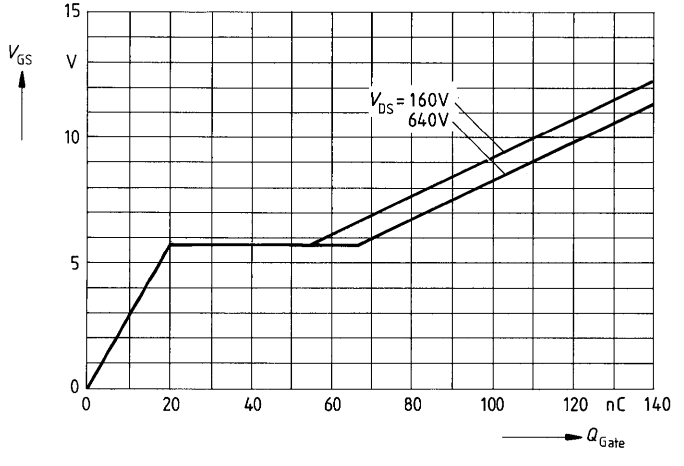
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



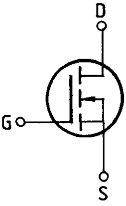
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 9A$



Main ratings

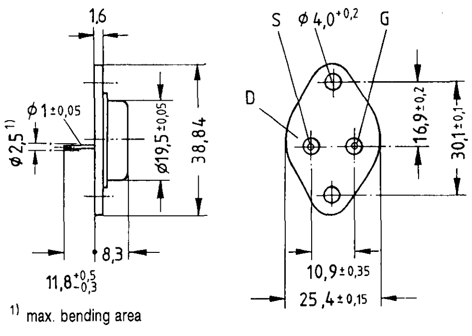
Drain-source voltage V_{DS} = 800 V
Continuous drain current I_D = 6 A
Drain-source on-resistance $R_{DS(on)}$ = 1,5 Ω

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 84 A	C67078-A1013-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	6	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	24	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤35	K/W	

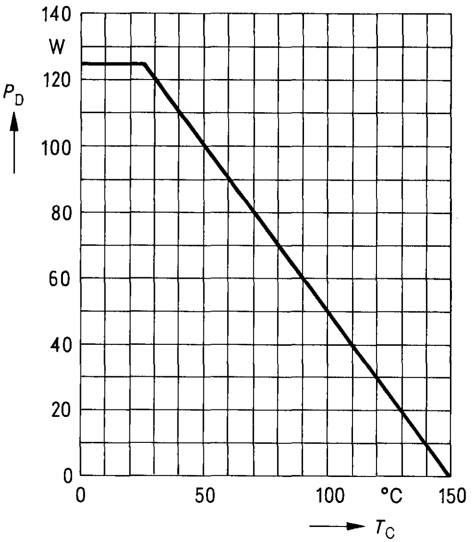
 S Preferred Type

Electrical characteristics

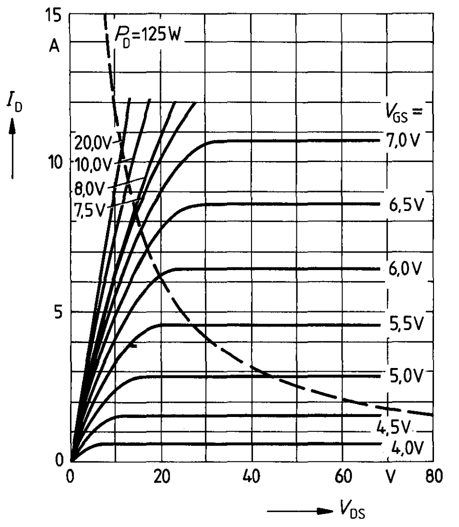
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,3	1,5	Ω	V_{GS} = 10V I_D = 3A
Dynamic ratings						
Forward transconductance	g_{fs}	1,8	3,0	–	S	V_{DS} = 25V I_D = 3A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	200	350	pF	
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	6,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	24		
Diode forward on-voltage	V_{SD}	–	1,1	1,5	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	25	–	µC	

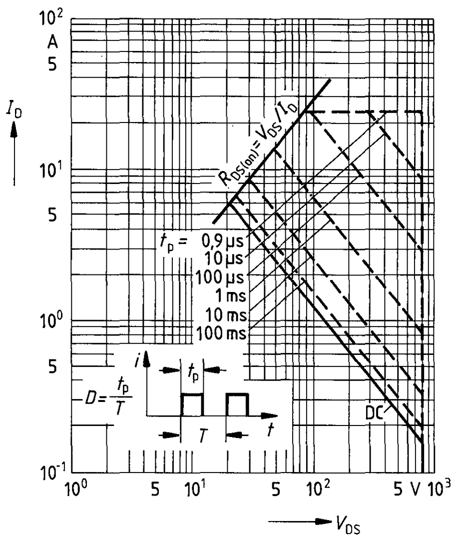
Power dissipation $P_D = f(T_C)$



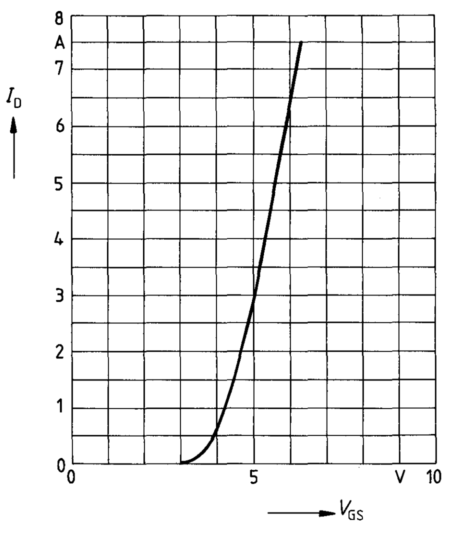
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



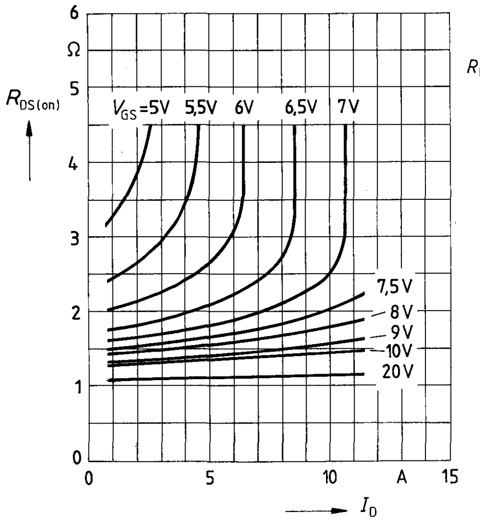
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



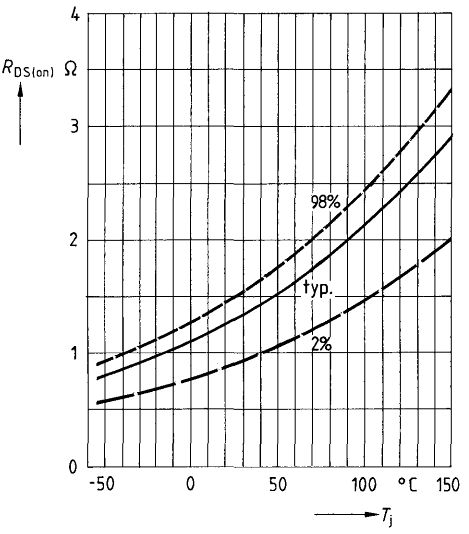
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



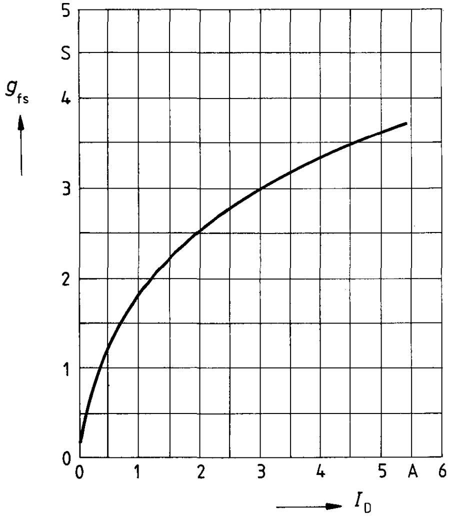
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



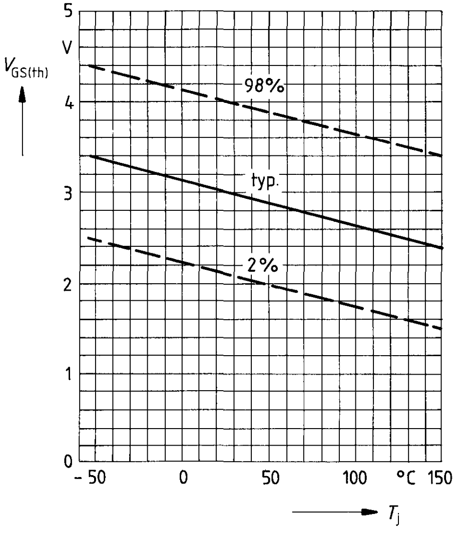
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 3A$, $V_{GS} = 10V$
(spread)



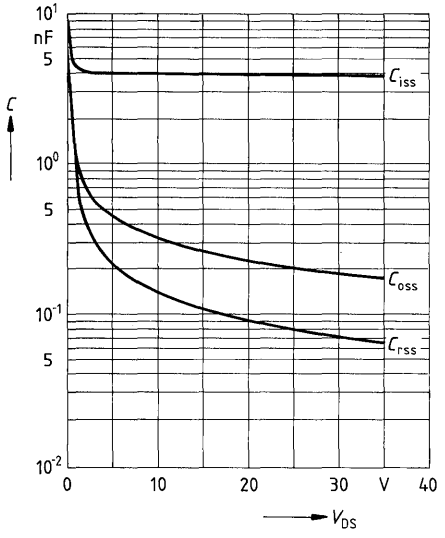
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



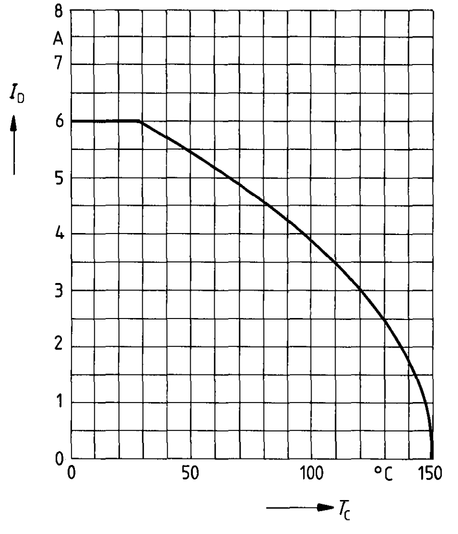
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



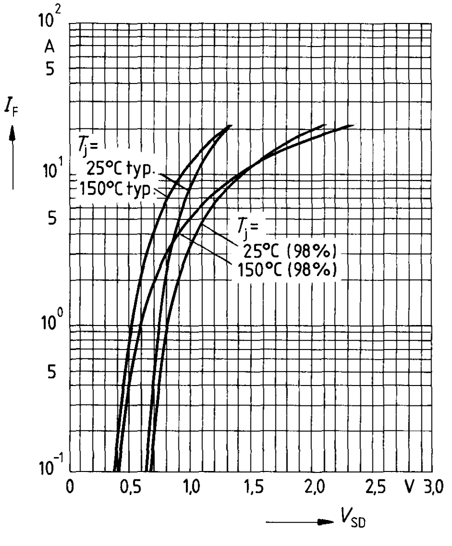
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



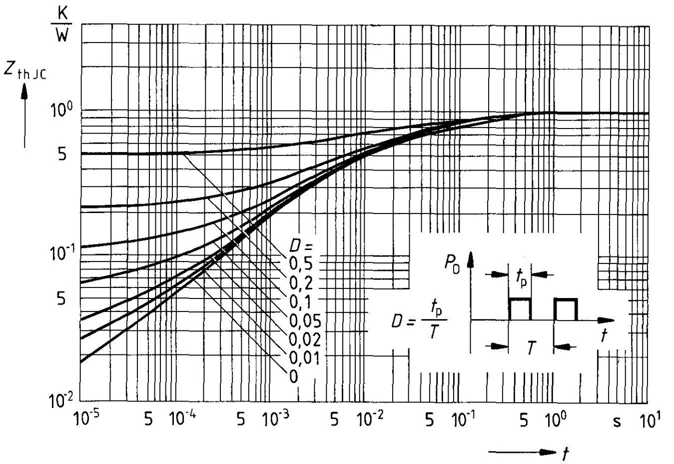
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



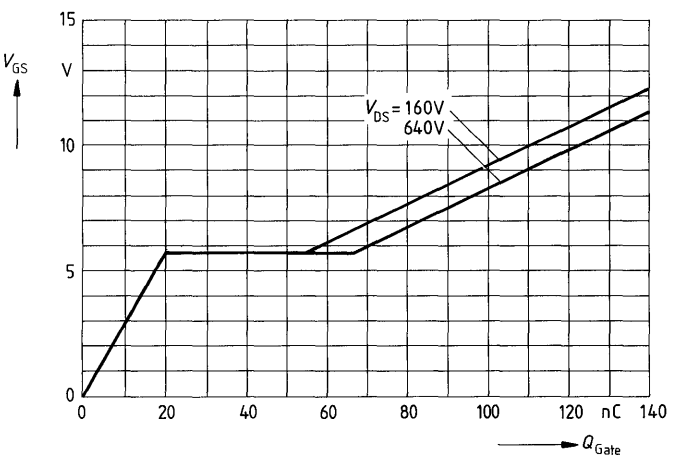
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

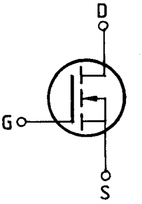


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 9A$



Main ratings

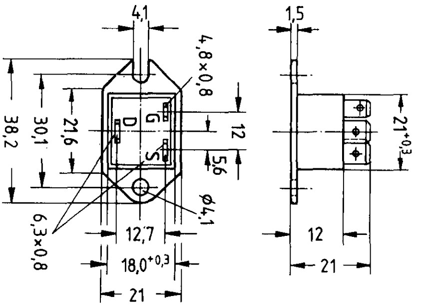
N-Channel



Drain-source voltage V_{DS} = **800 V**
Continuous drain current I_D = **4,3 A**
Drain-source on-resistance $R_{DS(on)}$ = **2,0 Ω**

Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 88	C67078-A1609-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,3	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	17	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 ... +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,5	K/W	

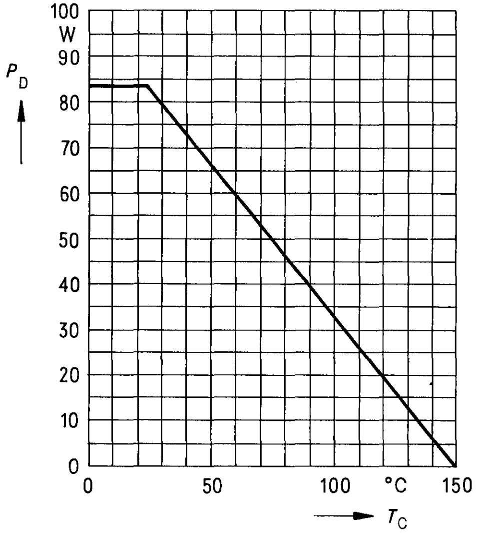
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

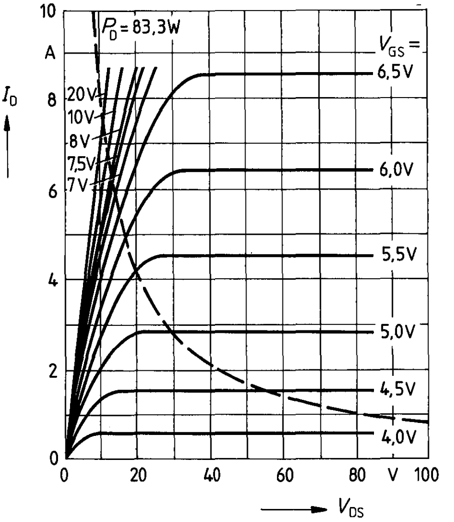
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	1,7	2,0	Ω	V_{GS} = 10V I_D = 3A
Dynamic ratings						
Forward transconductance	g_{fs}	1,8	3,0	–	S	V_{DS} = 25V I_D = 3A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	200	350	pF	
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,3	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	17		
Diode forward on-voltage	V_{SD}	–	1,1	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	25	–	µC	

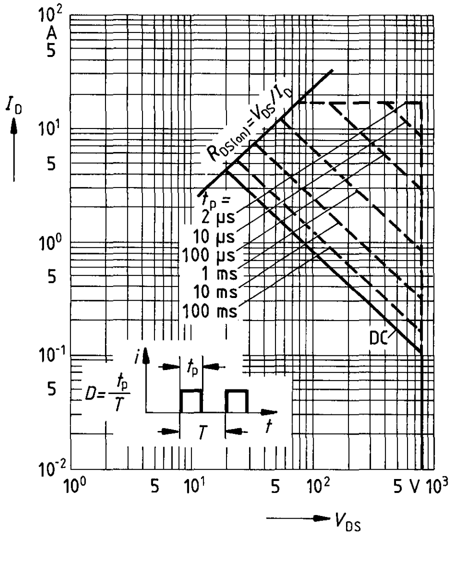
Power dissipation $P_D = f(T_C)$



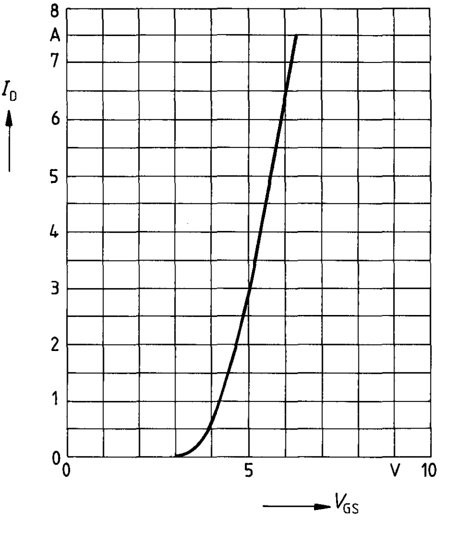
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



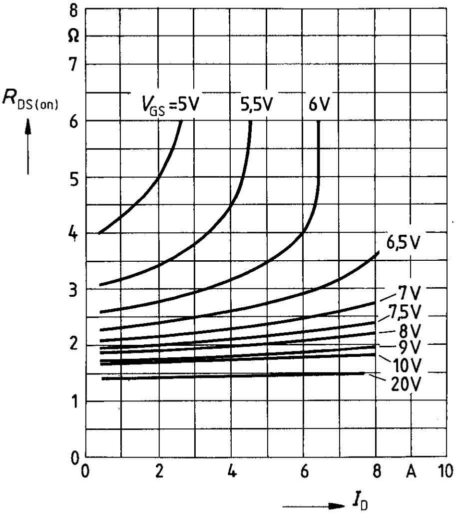
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



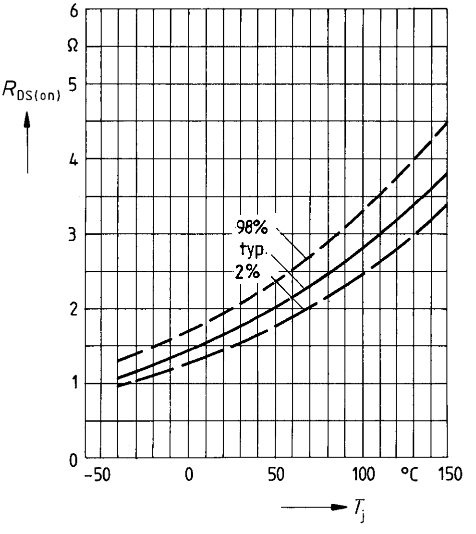
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



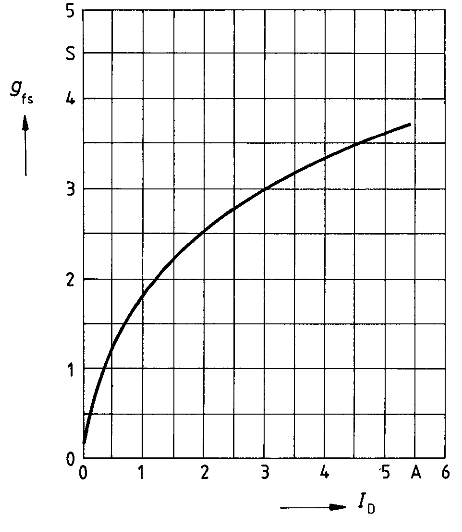
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



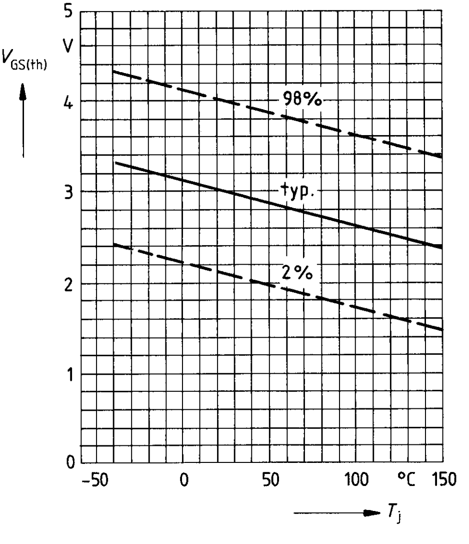
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 3A$, $V_{GS} = 10V$
(spread)



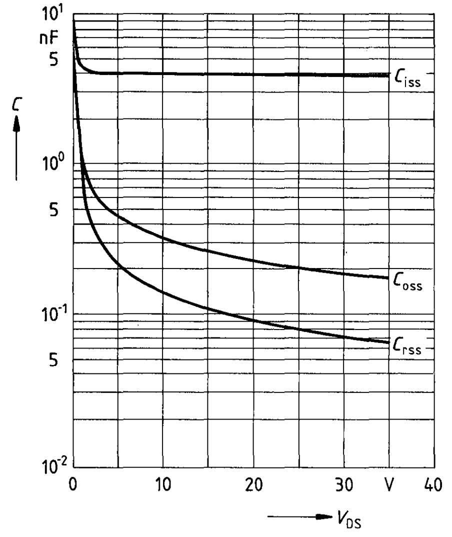
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



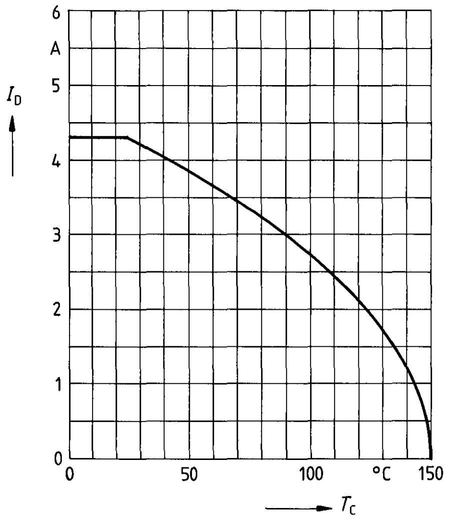
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



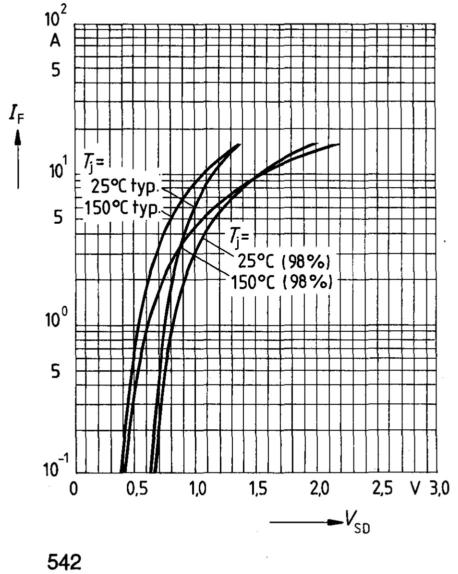
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



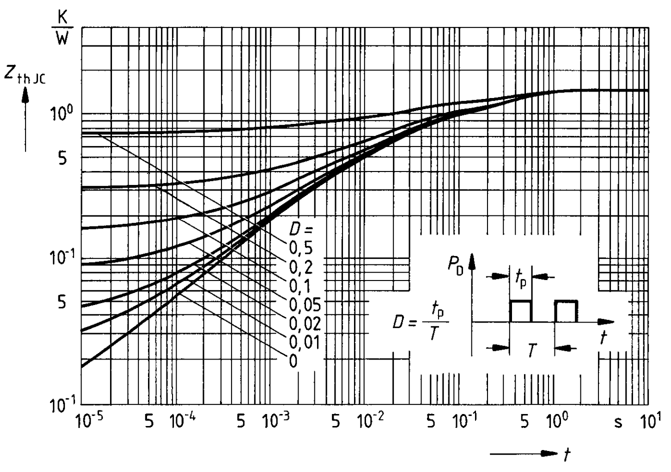
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



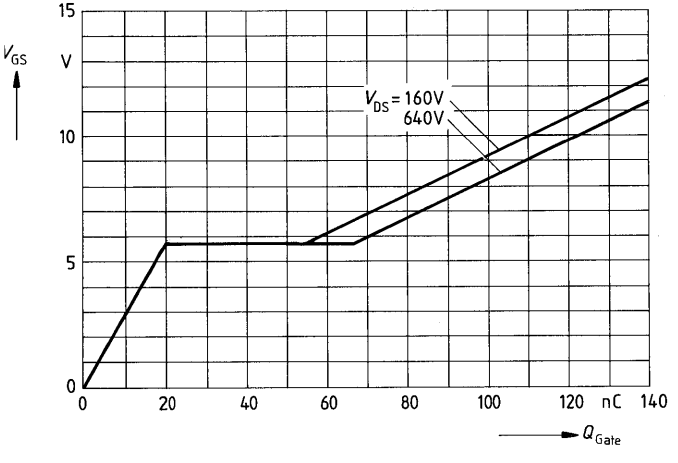
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



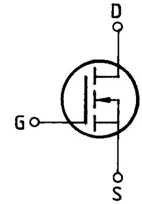
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 9A$



Main ratings

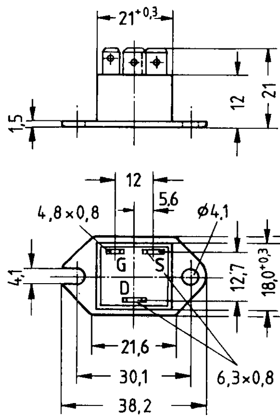
Drain-source voltage V_{DS} = **800 V**
Continuous drain current I_D = **5 A**
Drain-source on-resistance $R_{DS(on)}$ = **1,5 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
S BUZ 88 A	C67078-A1609-A3



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	20	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 … +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\,JC}$	≤1,5	K/W	

[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

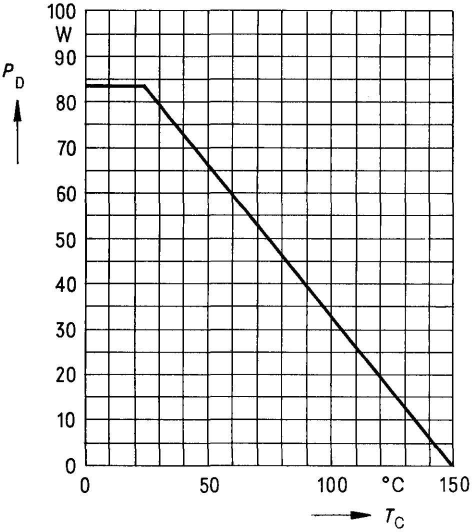
 S Preferred Type

Electrical characteristics

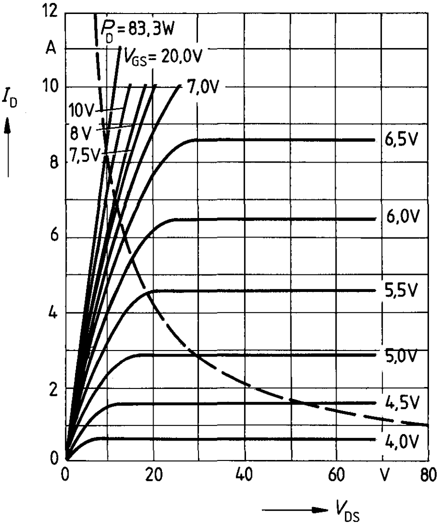
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	1,3	1,5	Ω	V_{GS} = 10V I_D = 3A
Dynamic ratings						
Forward transconductance	g_{fs}	1,8	3,0	–	S	V_{DS} = 25V I_D = 3A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	200	350	pF	
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	20		
Diode forward on-voltage	V_{SD}	–	1,1	1,45	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	25	–	µC	

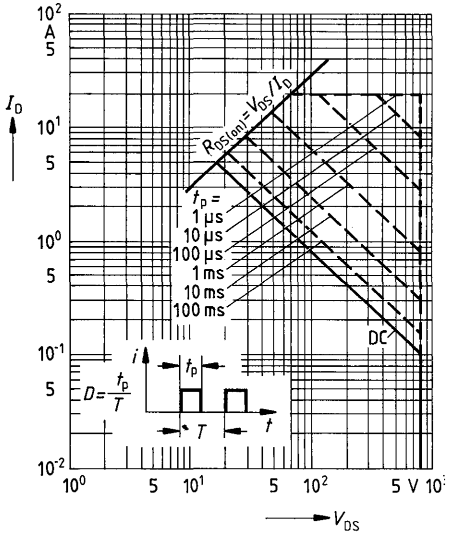
Power dissipation $P_D = f(T_C)$



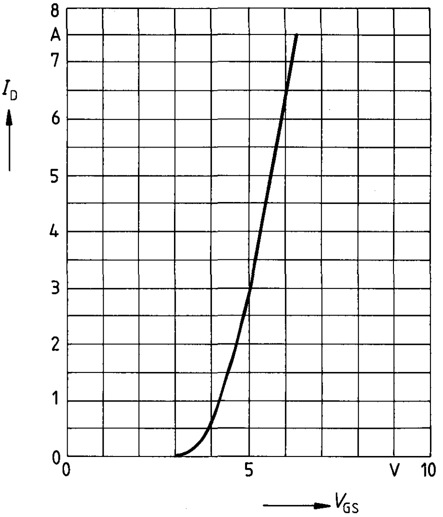
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



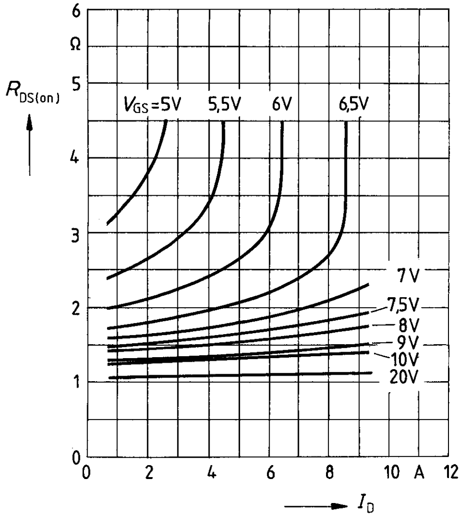
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



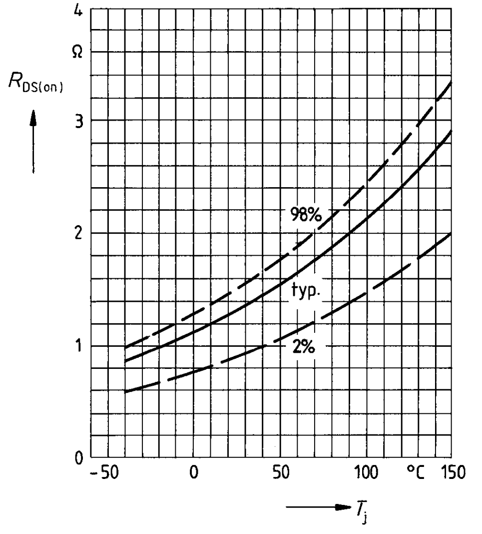
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



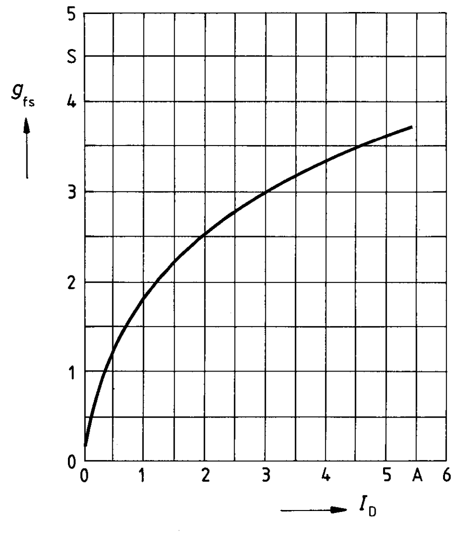
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



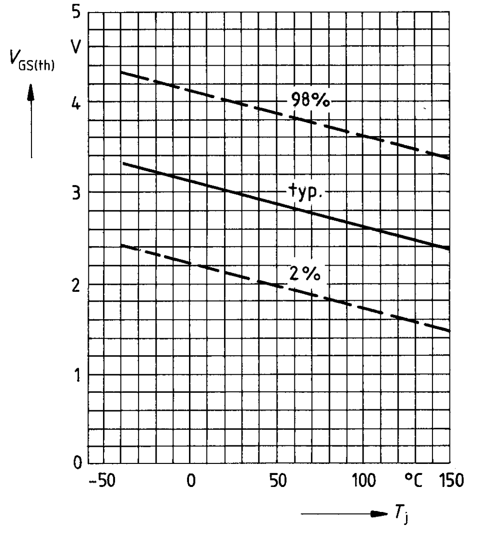
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 3A$, $V_{GS} = 10V$
(spread)



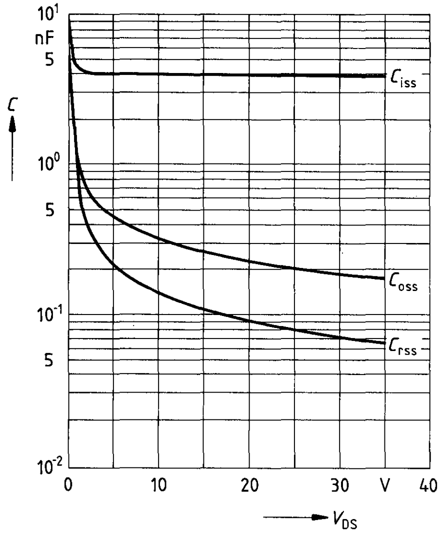
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



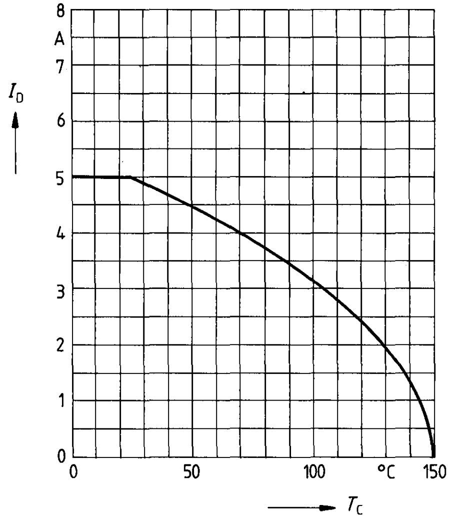
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



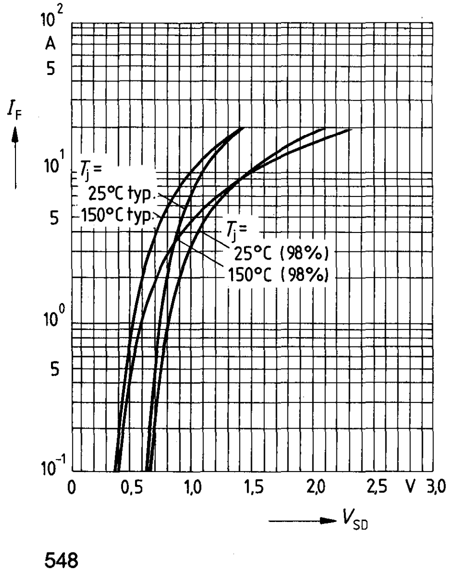
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



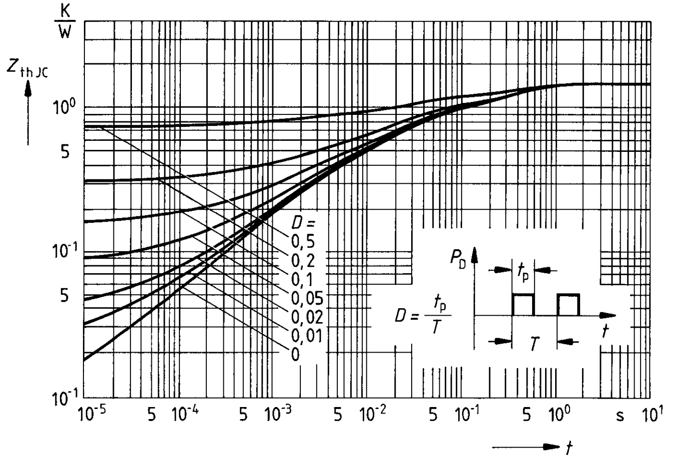
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



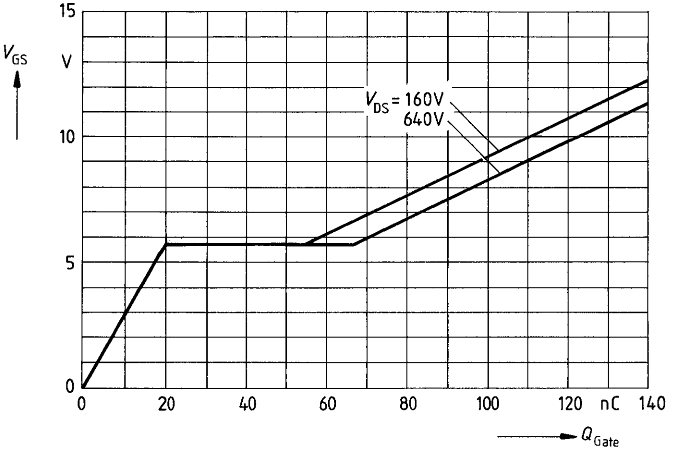
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



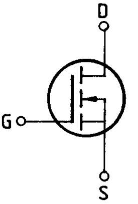
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 9A$



Main ratings

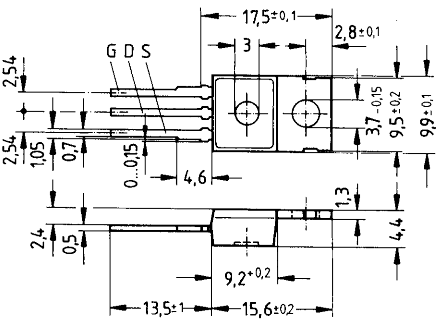
Drain-source voltage V_{DS} **= 600 V**
Continuous drain current I_D **= 4,0 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
Ⓢ BUZ 90	C67078-A1321-A2



Dimensions in mm

Maximum ratings

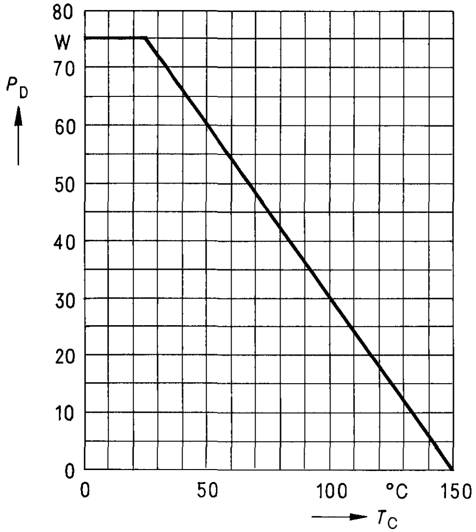
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	600	V	
Drain-gate voltage	V_{DGR}	600	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,0	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	16	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

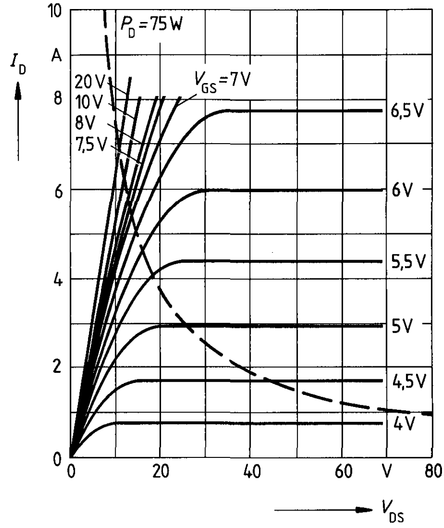
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	600	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 600V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,8	2,0	Ω	V_{GS} = 10V I_D = 2,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	110	170	pF	
Reverse transfer capacitance	C_{rss}	–	40	70		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	60		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	16		
Diode forward on-voltage	V_{SD}	–	0,95	1,2	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1,2	–	µs	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6	–	µC	

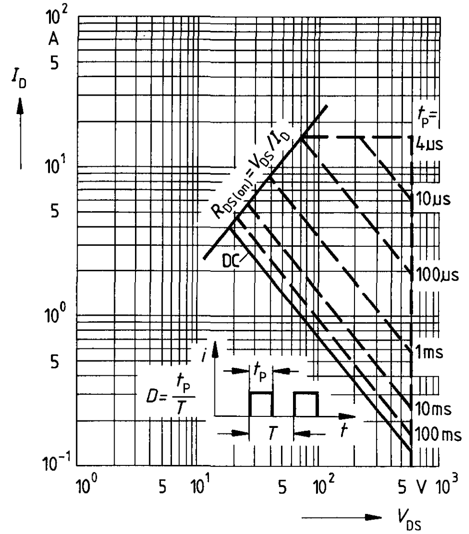
Power dissipation $P_D = f(T_C)$



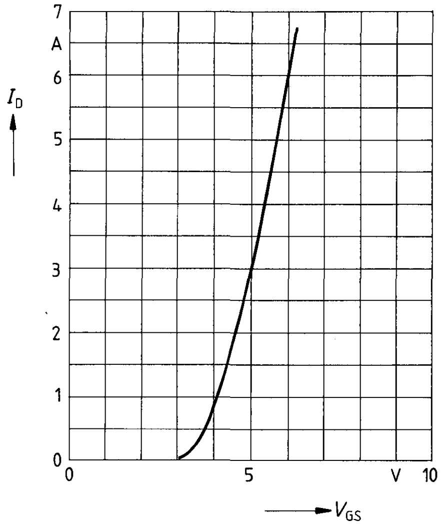
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



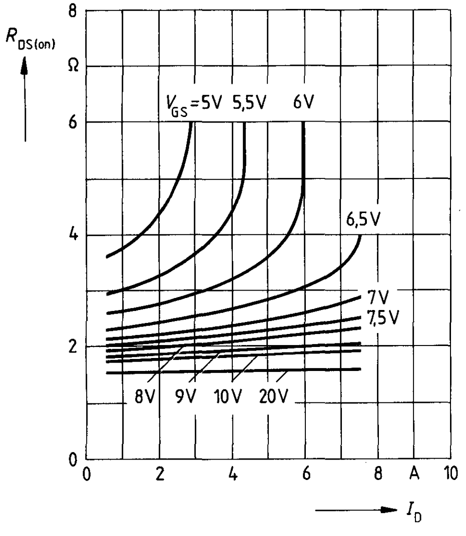
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



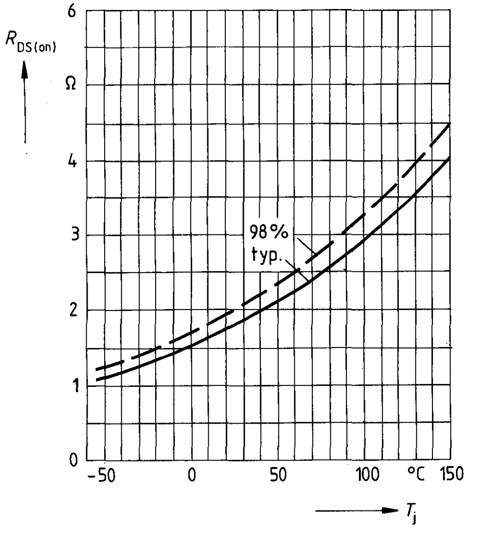
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



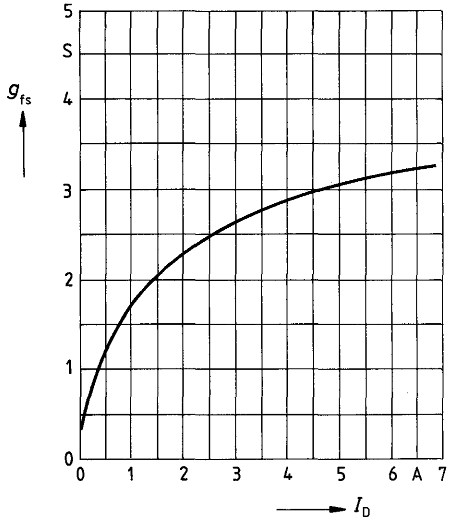
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



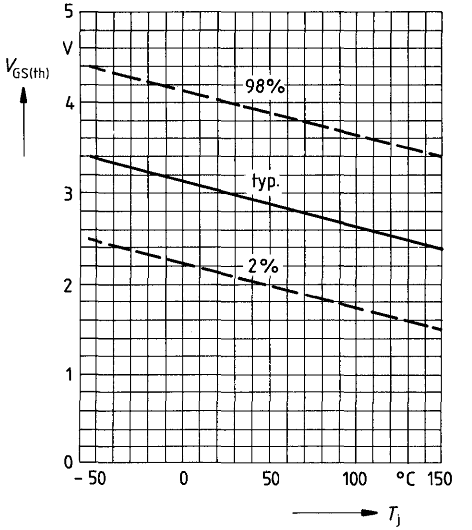
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 2,5A, V_{GS} = 10V
(spread)



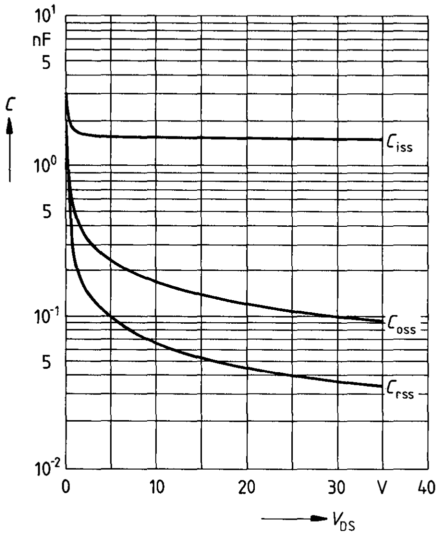
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



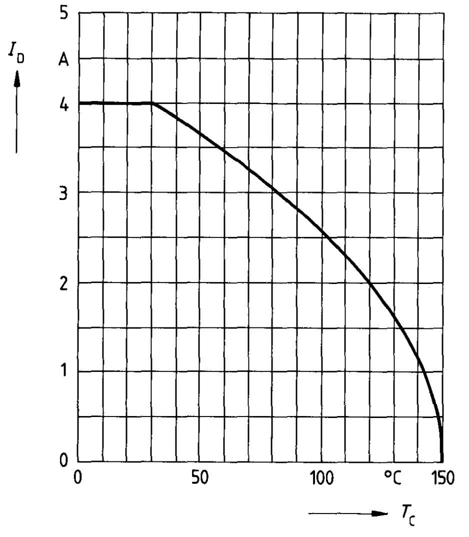
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



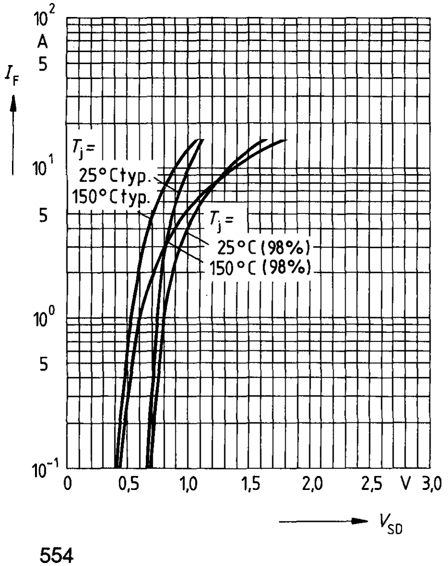
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



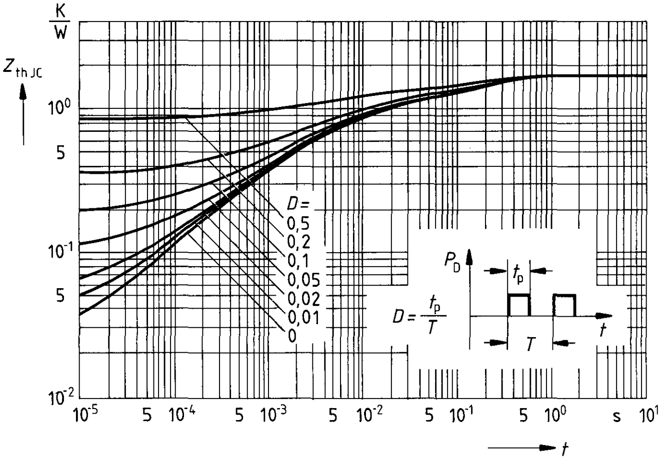
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



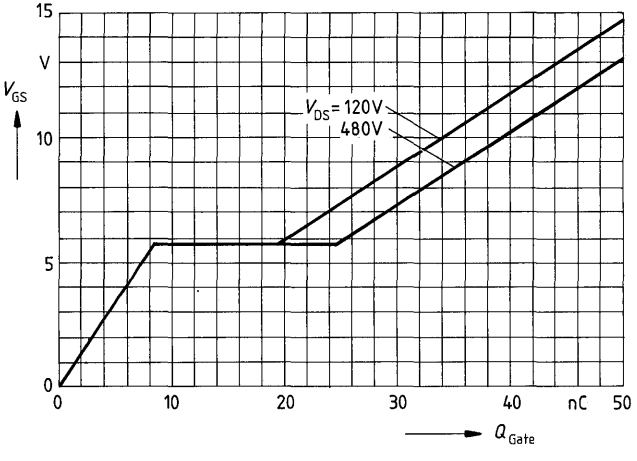
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

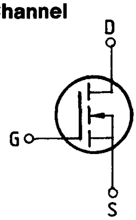


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 39{,}9A$



Main ratings

N-Channel

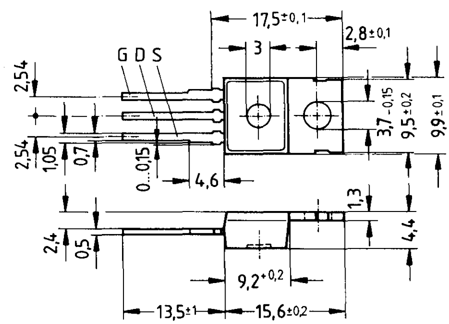


Drain-source voltage	V_{DS}	**= 600 V**
Continuous drain current	I_D	**= 3,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 2,5 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
S BUZ 90 A	C67078-A1321-A3



Dimensions in mm

Maximum ratings

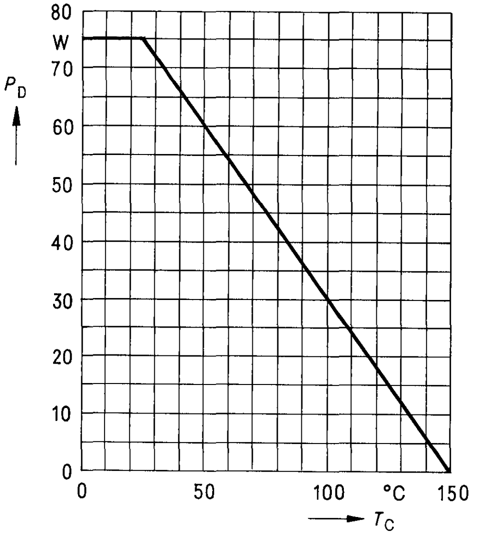
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	600	V	
Drain-gate voltage	V_{DGR}	600	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	3,5	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	14	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j, T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

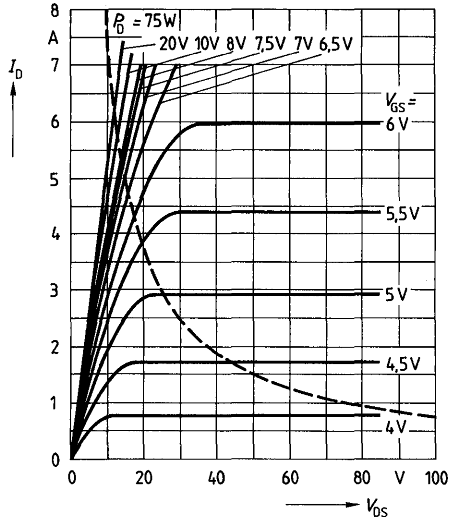
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 600V V_{GS} = 2,5V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	2,2	2,5	Ω	V_{GS} = 10V I_D = 2,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,5	–	S	V_{DS} = 25V I_D = 2,5A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	110	170	pF	
Reverse transfer capacitance	C_{rss}	–	40	70		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,4A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	110	140		
	t_f	–	50	65		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	3,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	14		
Diode forward on-voltage	V_{SD}	–	1,1	1,5	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1,2	–	µs	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6	–	µC	

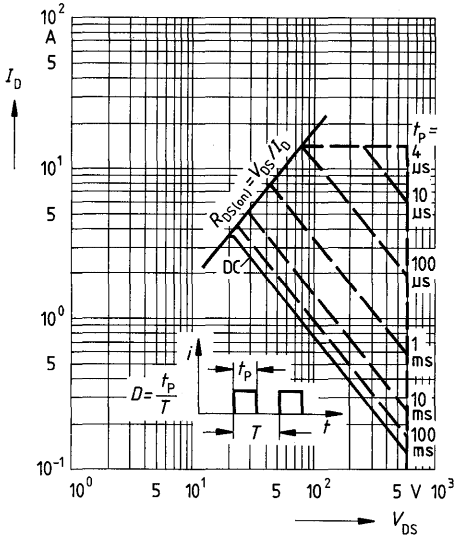
Power dissipation $P_D = f(T_C)$



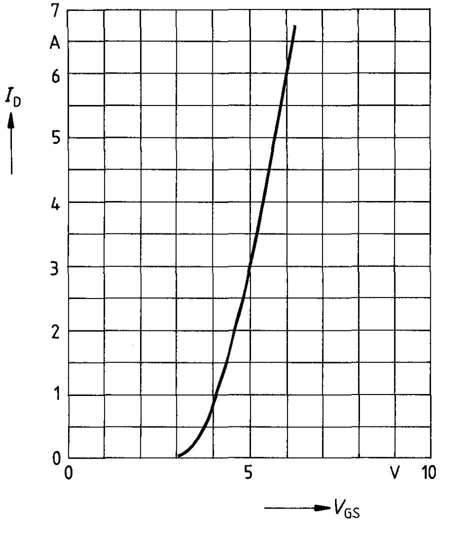
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 μs pulse test,
$T_j = 25\,°C$



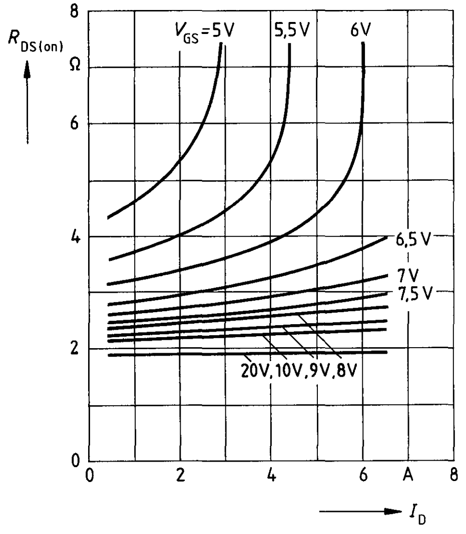
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



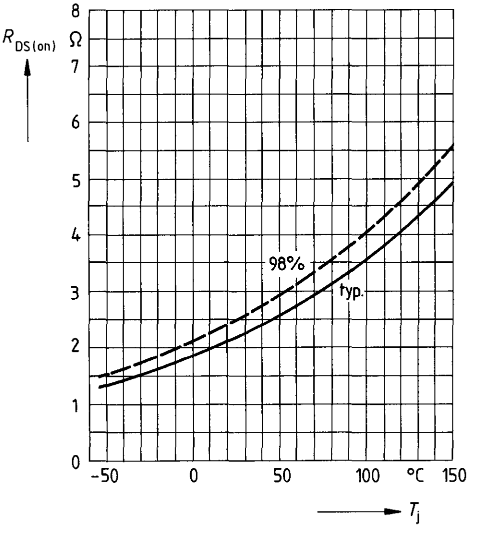
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 μs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



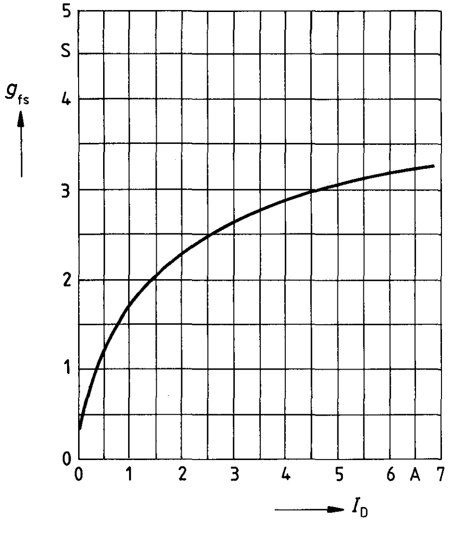
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



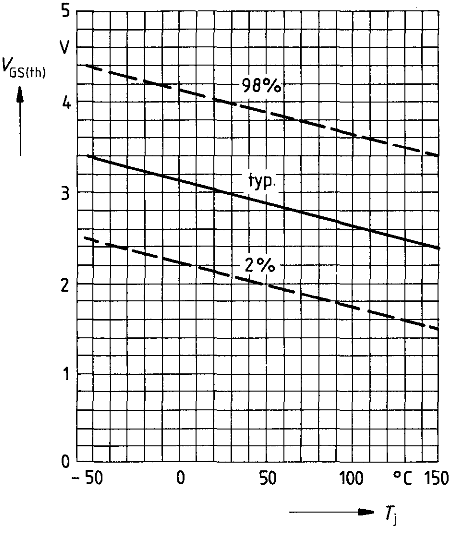
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 2{,}5A$, $V_{GS} = 10V$
(spread)



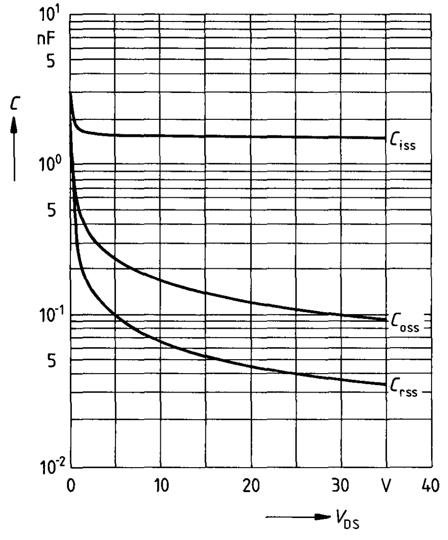
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



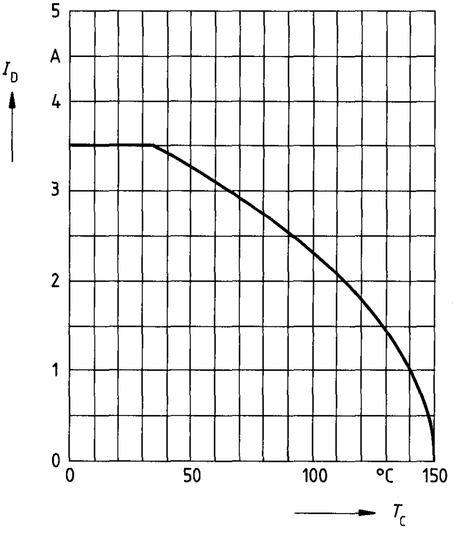
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



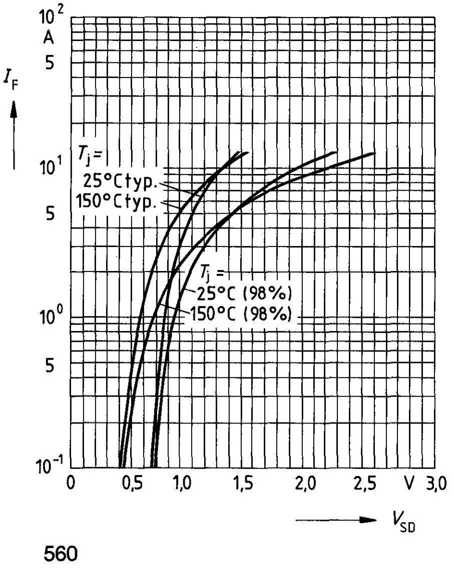
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



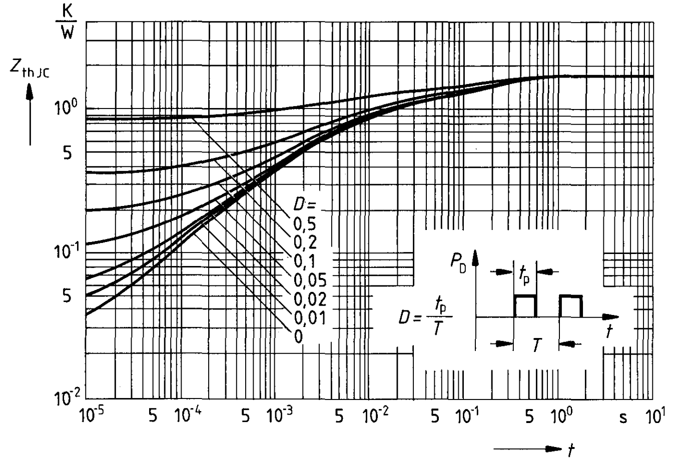
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



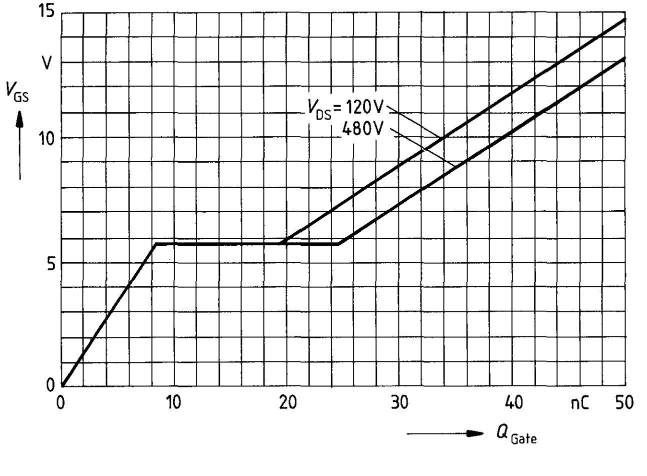
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

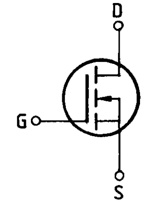


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 39{,}9A$



Main ratings

N-Channel

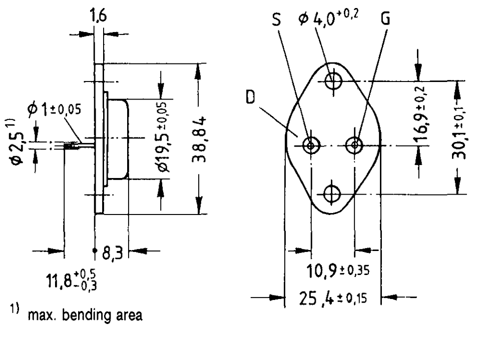


Drain-source voltage	V_{DS}	**= 600 V**
Continuous drain current	I_D	**= 7,8 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,9 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 94	C67078-A1019-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	600	V	
Drain-gate voltage	V_{DGR}	600	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	7,8	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	31	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\ JC}$	≤ 1,0	K/W
Chip – ambient	$R_{th\ JA}$	≤ 35	K/W

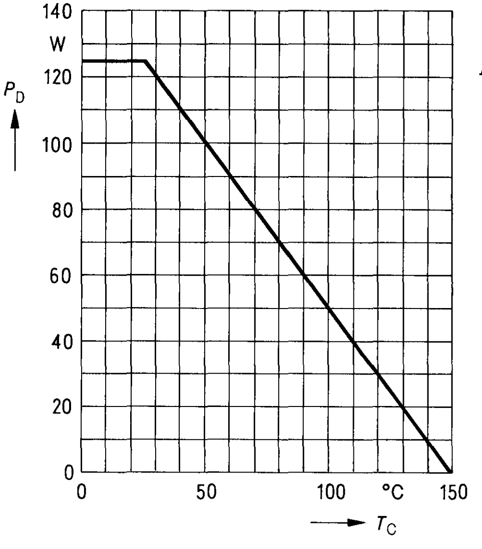
 S Preferred Type

Electrical characteristics

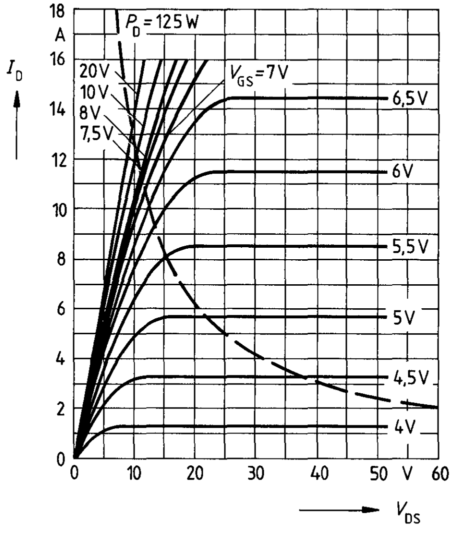
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	600	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 600V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,8	0,9	Ω	V_{GS} = 10V I_D = 5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	4,0	–	S	V_{DS} = 25V I_D = 5A
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400	pF	
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	7,8	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	31		
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1,2	–	µs	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

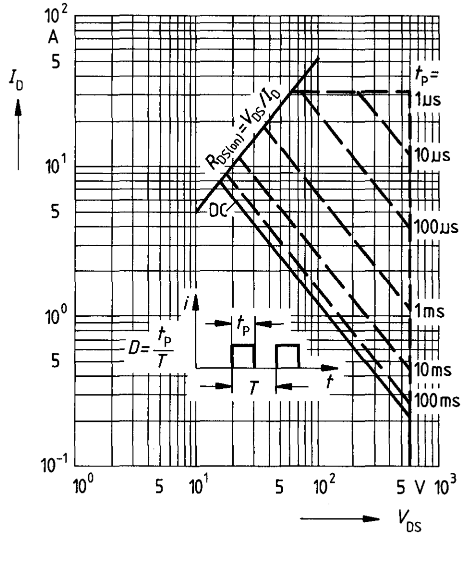
Power dissipation $P_D = f(T_C)$



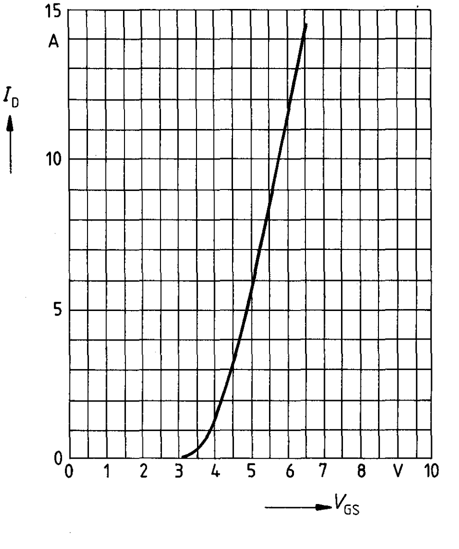
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



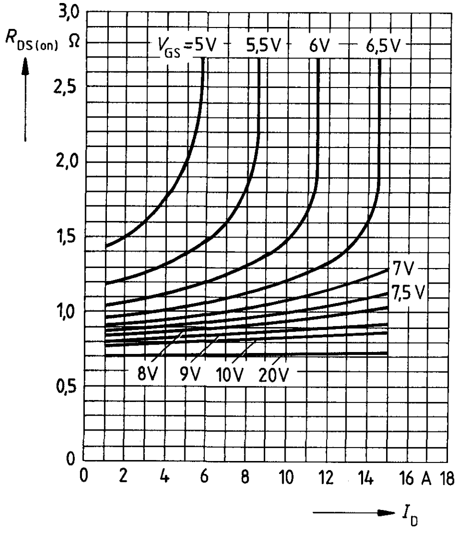
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



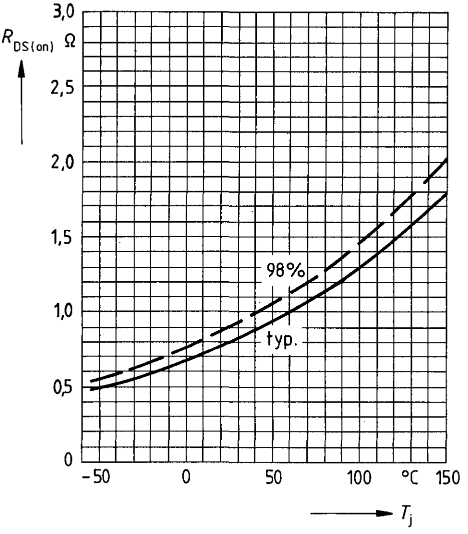
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



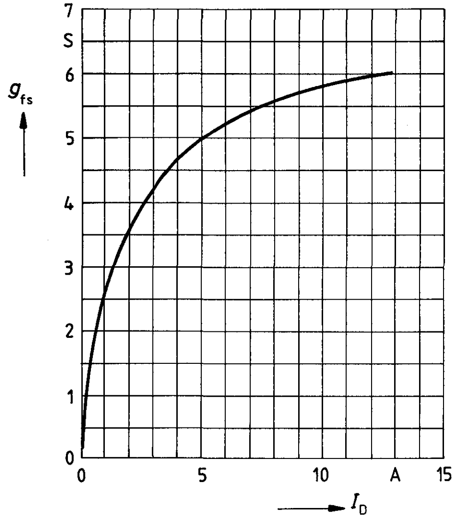
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



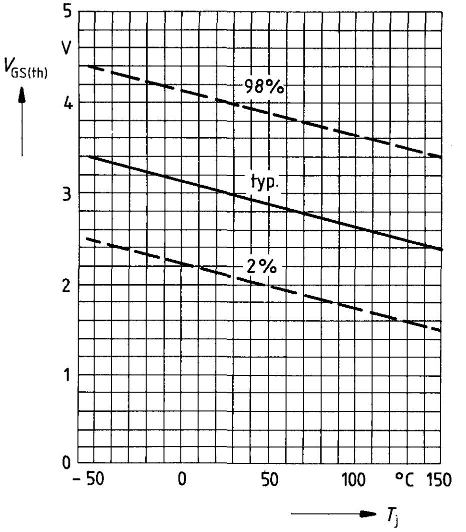
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 5A$, $V_{GS} = 10V$
(spread)



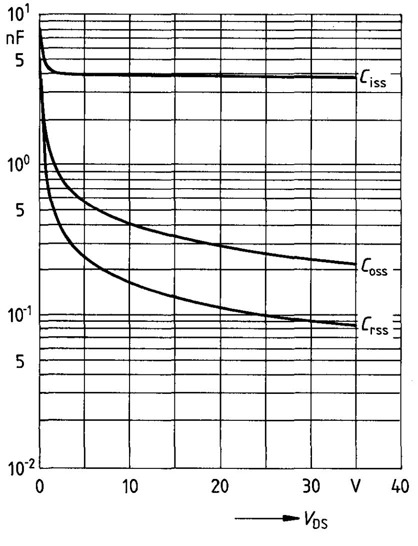
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



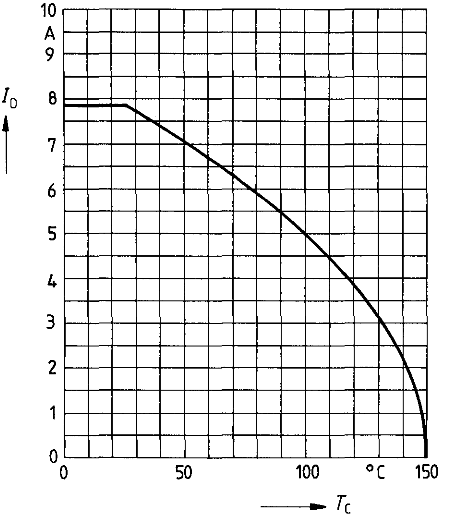
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



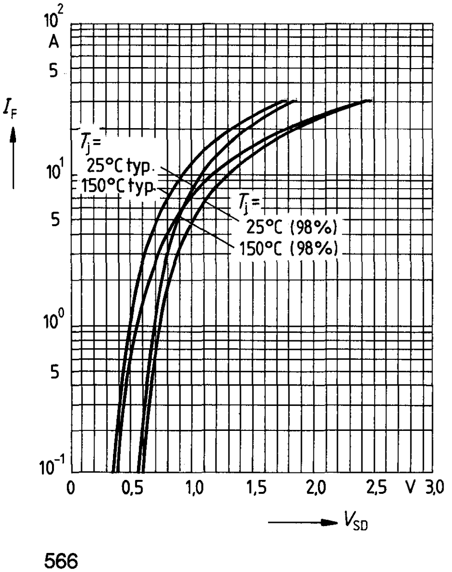
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



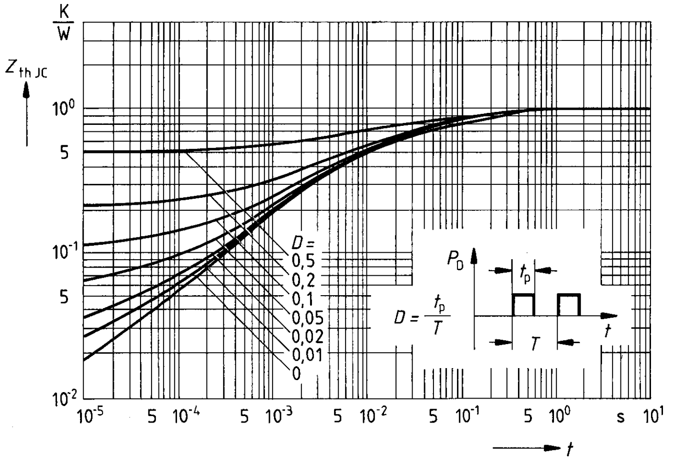
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



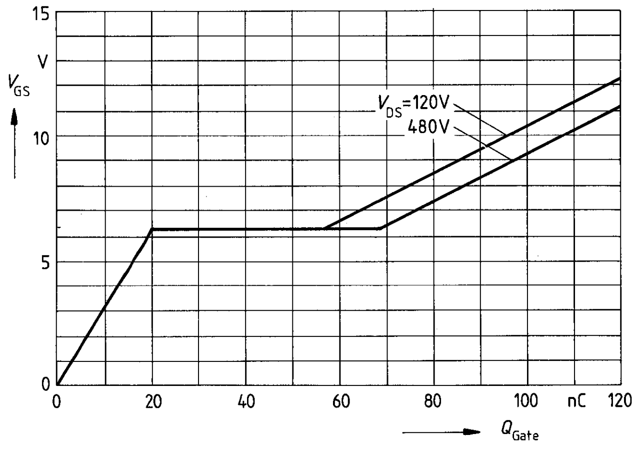
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



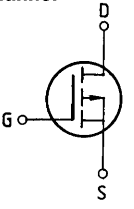
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 11{,}7A$



Main ratings

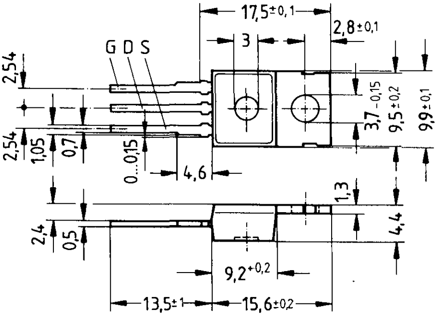
Drain-source voltage V_{DS} **= −50 V**
Continuous drain current I_D **= −7,0 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,4 Ω**

P-Channel



Description SIPMOS, P-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Typ	Bestellnummer
BUZ 171	C67078-A1450-A2



Dimensions in mm

Maximum ratings

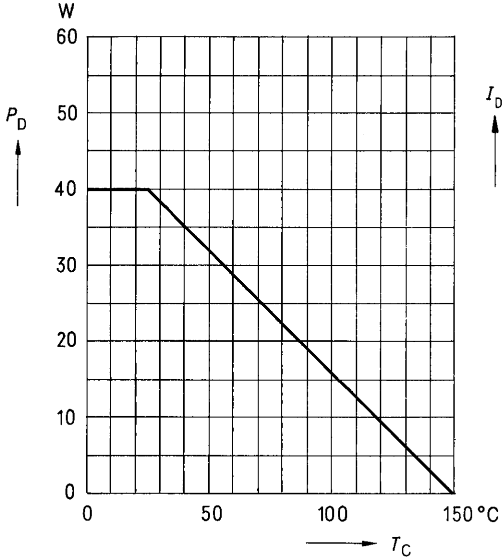
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	−50	V	
Drain-gate voltage	V_{DGR}	−50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	−7	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	−28	A	T_C = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Not periodical
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

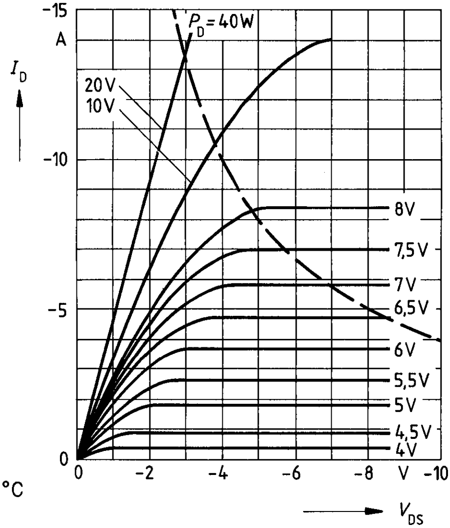
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	−50	–	–	V	V_{GS} = 0V I_D = −0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	−2,1	−3,0	−4,0		V_{DS} = V_{GS} I_D = −1mA
Zero gate voltage drain current	I_{DSS}	– –	−20 −100	−250 −1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = −50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	−10	−100	nA	V_{GS} = −10V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,3	0,4	Ω	V_{GS} = −10V I_D = −4,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,2	–	S	V_{DS} = −25V I_D = −4,5A
Input capacitance	C_{iss}	–	900	1200	pF	V_{GS} = 0V V_{DS} = −25V f = 1MHz
Output capacitance	C_{oss}	–	320	500		
Reverse transfer capacitance	C_{rss}	–	130	230		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	20	30	ns	V_{CC} = −30V I_D = −2,9A V_{GS} = −10V R_{GS} = 50Ω
	t_r	–	60	95		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	55	75		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	−7,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	−28		
Diode forward on-voltage	V_{SD}	–	−2,0	−2,8	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	90	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = −30V
Reverse recovery charge	Q_{rr}	–	0,23	–	µC	

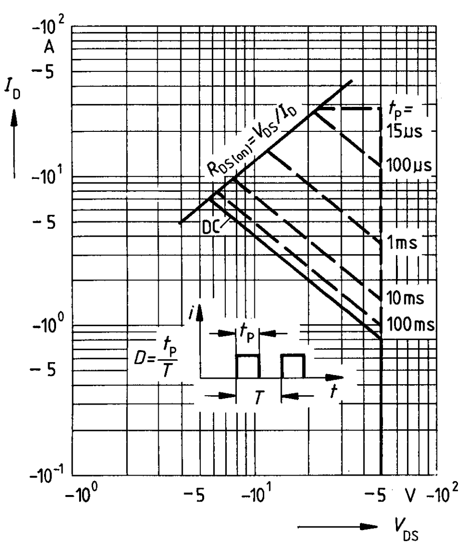
Power dissipation $P_D = f(T_C)$



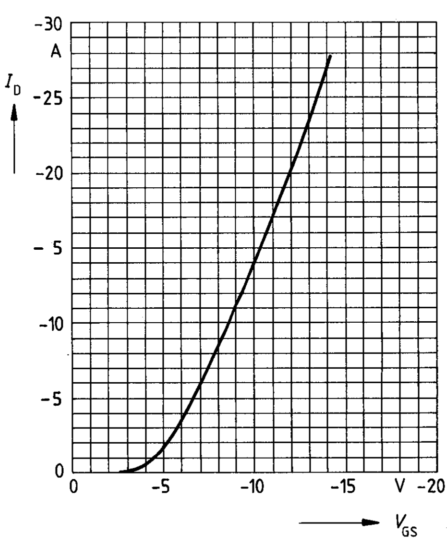
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



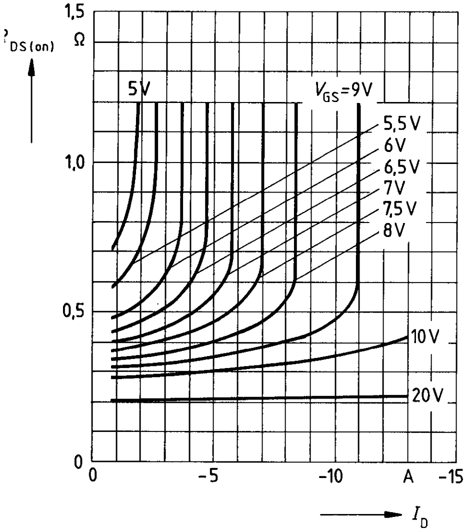
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



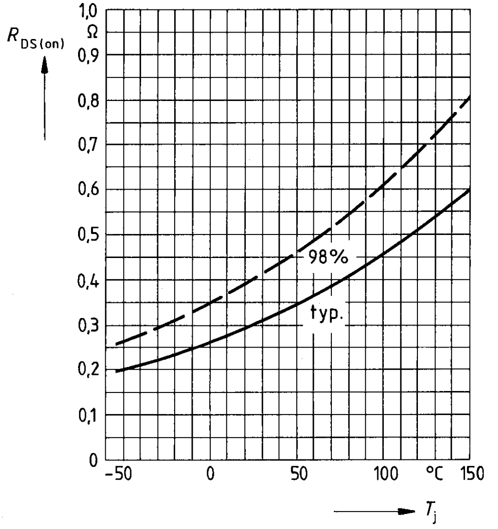
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



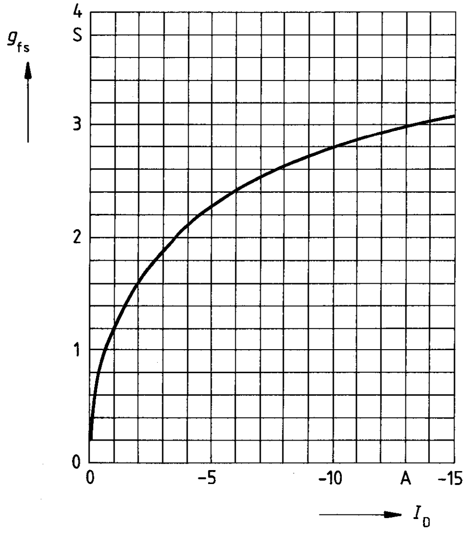
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



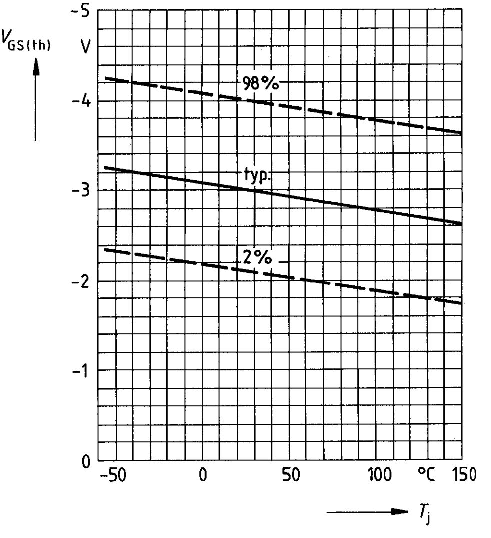
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = -4{,}5A$, $V_{GS} = -10V$
(spread)



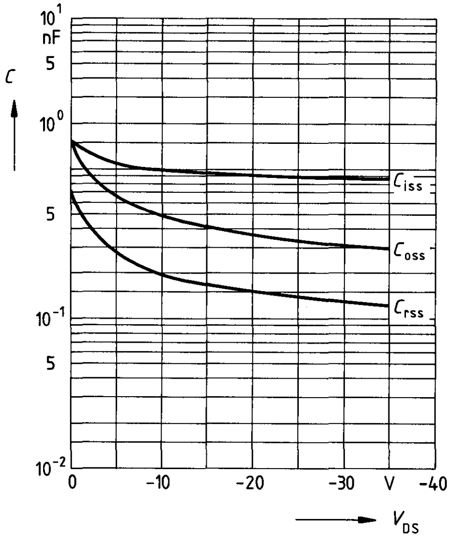
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = -25V$, $T_j = 25\,°C$



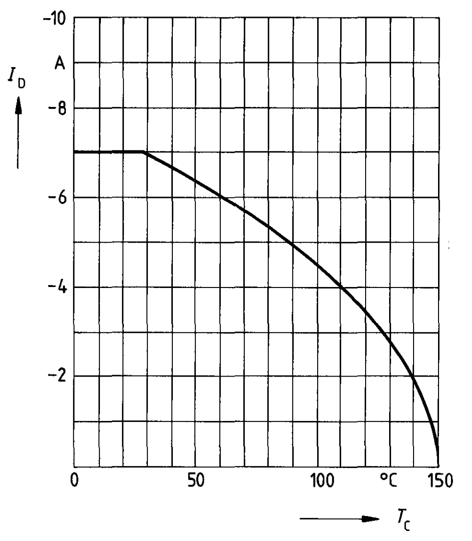
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = -1mA$
(spread)



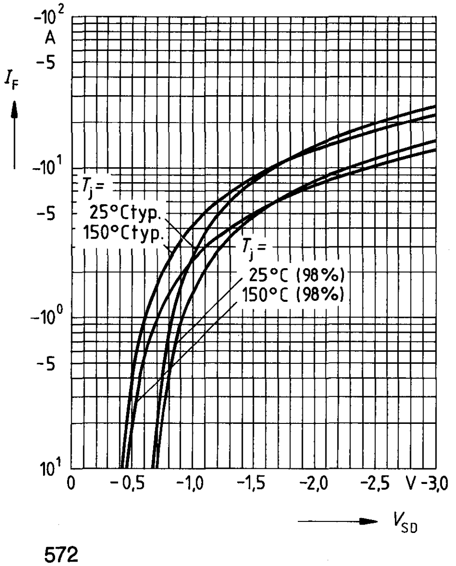
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



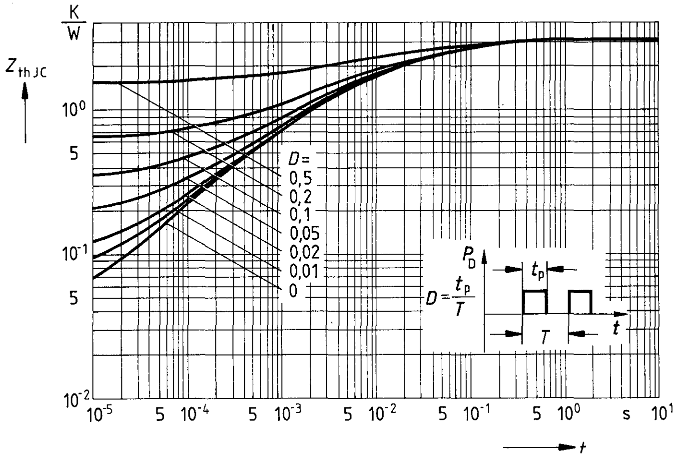
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq -10V$



Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



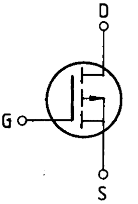
Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



Main ratings

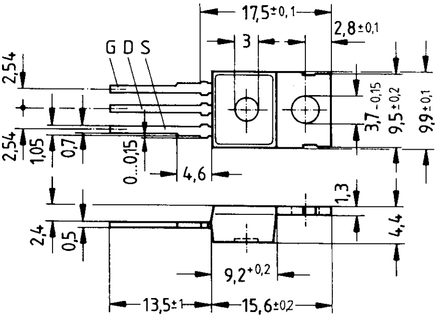
Drain-source voltage V_{DS} **= −100 V**
Continuous drain current I_D **= −5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,8 Ω**

P-Channel



Description SIPMOS, P-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
BUZ 172	C67078-A1451-A2



Dimensions in mm

Maximum ratings

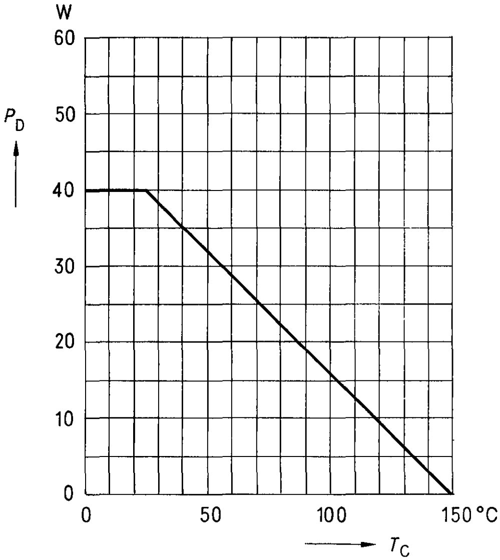
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	−100	V	
Drain-gate voltage	V_{DGR}	−100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	−5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	−20	A	T_C = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Not periodical
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤3,1	K/W	
Chip – ambient	$R_{th JA}$	≤75	K/W	

Electrical characteristics

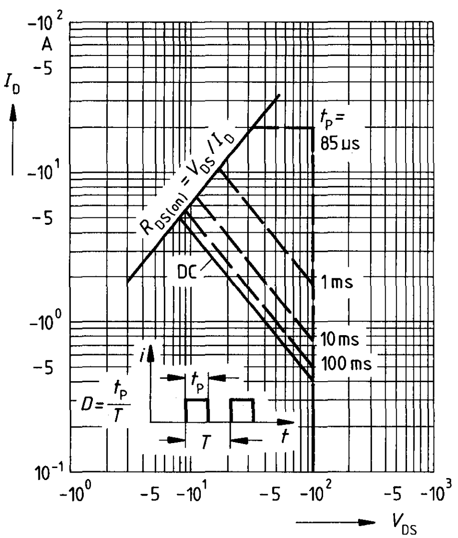
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	−100	–	–	V	V_{GS} = 0V I_D = −0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	−2,1	−3,0	−4,0		V_{DS} = V_{GS} I_D = −1mA
Zero gate voltage drain current	I_{DSS}	– –	−20 −100	−250 −1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = −100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	−10	−100	nA	V_{GS} = −10V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	–	0,8	Ω	V_{GS} = −10V I_D = −3,2A
Dynamic ratings						
Forward transconductance	g_{fs}	0,9	1,1	–	S	V_{DS} = −25V I_D = −3,2A
Input capacitance	C_{iss}	–	1000	–	pF	V_{GS} = 0V V_{DS} = −25V f = 1MHz
Output capacitance	C_{oss}	–	120	–		
Reverse transfer capacitance	C_{rss}	–	60	–		
Turn-on time t_{on} (t_{on} = $t_{d\,(on)}$ + t_r)	$t_{d\,(on)}$	–	15	20	ns	V_{CC} = −30V I_D = −2,8A V_{GS} = −5V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} (t_{off} = $t_{d\,(off)}$ + t_f)	$t_{d\,(off)}$	–	70	90		
	t_f	–	40	55		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	−5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	−20		
Diode forward on-voltage	V_{SD}	–	–	−1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = −30V
Reverse recovery charge	Q_{rr}	–	0,75	–	µC	

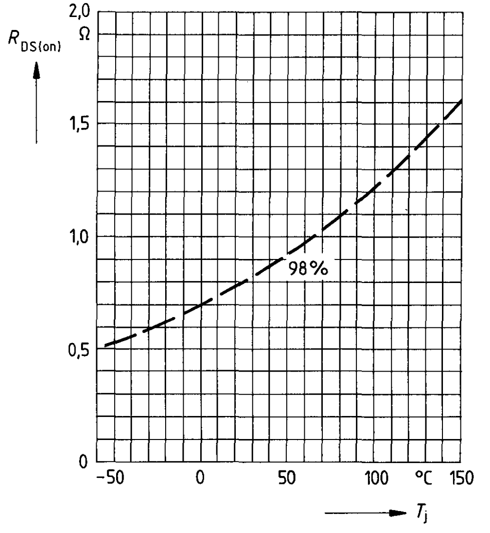
Power dissipation $P_D = f(T_C)$



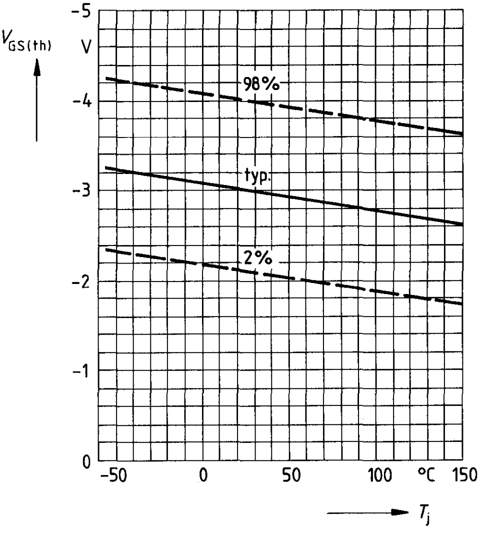
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



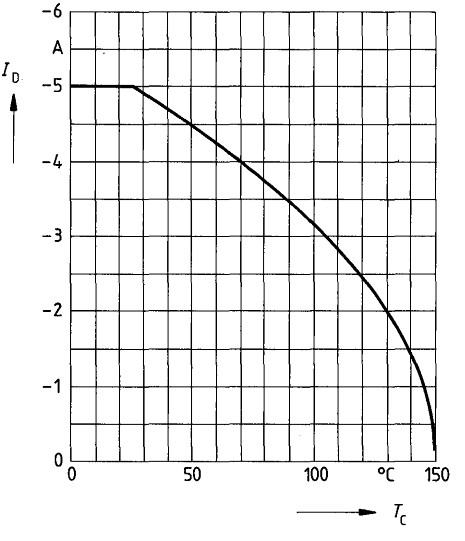
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = -3{,}2A$, $V_{GS} = -10V$
(spread)



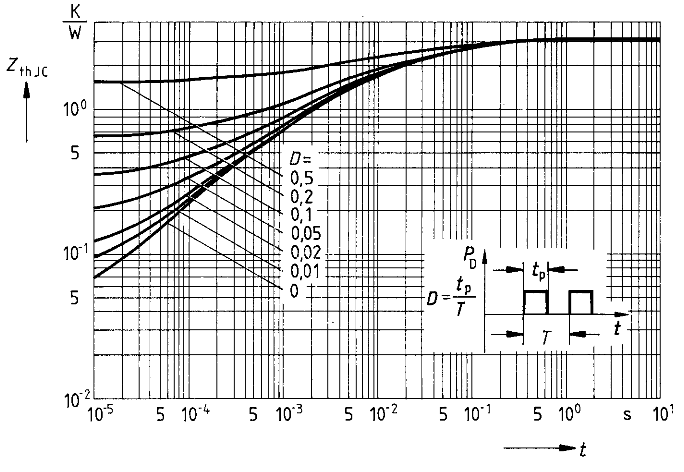
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = -1mA$
(spread)



Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq -10V$

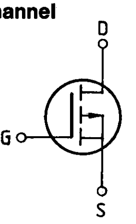


Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



Main ratings

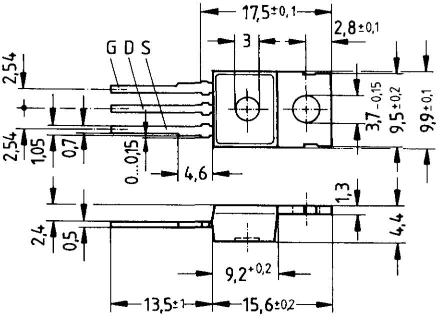
P-Channel



Drain-source voltage V_{DS} = −200 V
Continuous drain current I_D = −3 A
Drain-source on-resistance $R_{DS(on)}$ = 2 Ω

Description SIPMOS, P-channel, enhancement mode
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
BUZ 173	C67078-A1452-A2



Dimensions in mm

Maximum ratings

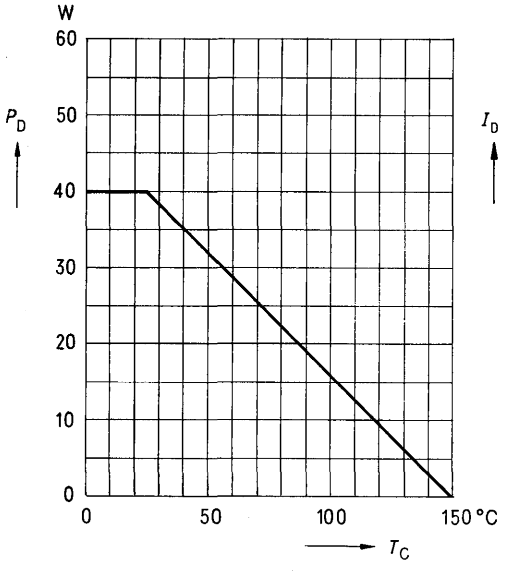
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	−200	V	
Drain-gate voltage	V_{DGR}	−200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	−3	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	−12	A	T_C = 25 °C
Gate-source peak voltage	V_{gs}	±20	V	Not periodical
Max. power dissipation	P_D	40	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤3,1	K/W	
Chip – ambient	$R_{th\ JA}$	≤75	K/W	

Electrical characteristics

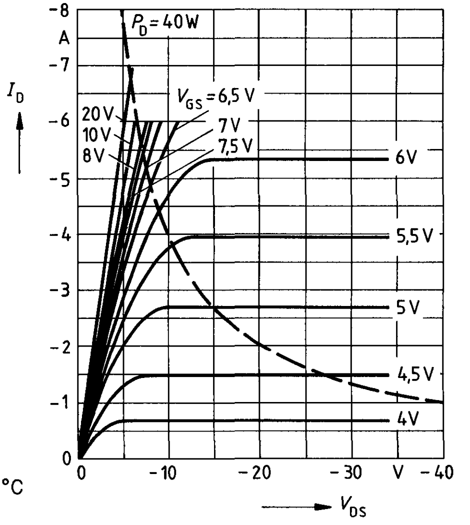
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics			Unit	Conditions
		min.	typ.	max.		
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	–200	–	–	V	V_{GS} = 0V I_D = –0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	–2,1	–3,0	–4,0		V_{DS} = V_{GS} I_D = –1mA
Zero gate voltage drain current	I_{DSS}	– –	–20 –100	–250 –1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = –200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	–10	–100	nA	V_{GS} = –10V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,0	2,0	Ω	V_{GS} = –10V I_D = –2A
Dynamic ratings						
Forward transconductance	g_{fs}	1,1	2,1	–	S	V_{DS} = –25V I_D = –2A
Input capacitance	C_{iss}	–	1000	1300	pF	V_{GS} = 0V V_{DS} = –25V f = 1MHz
Output capacitance	C_{oss}	–	130	200		
Reverse transfer capacitance	C_{rss}	–	45	80		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	20	30	ns	V_{CC} = –30V I_D = –2,5A V_{GS} = –5V R_{GS} = 50Ω
	t_r	–	60	95		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	70	90		
	t_f	–	55	75		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	–3	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	–12		
Diode forward on-voltage	V_{SD}	–	–1	–1,3	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = –100V
Reverse recovery charge	Q_{rr}	–	0,75	–	µC	

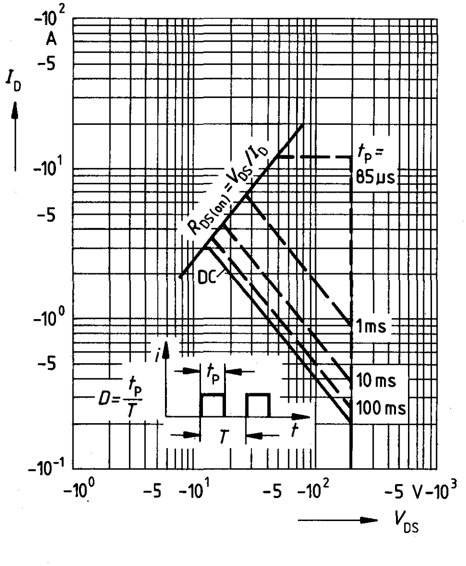
Power dissipation $P_D = f(T_C)$



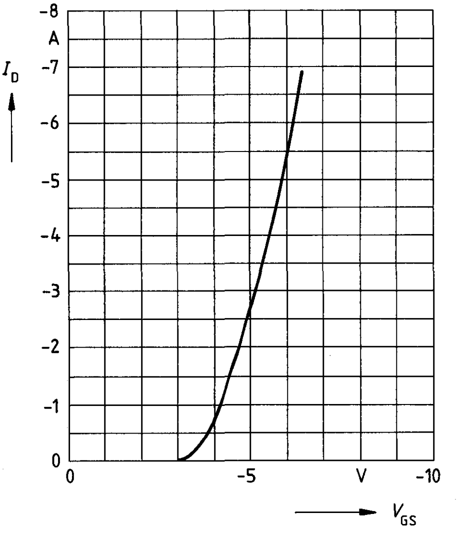
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



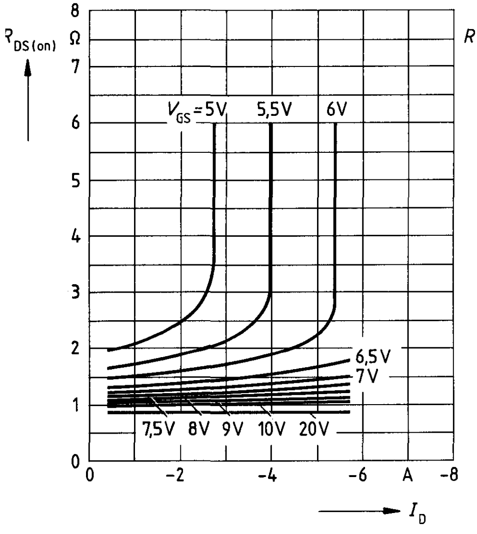
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



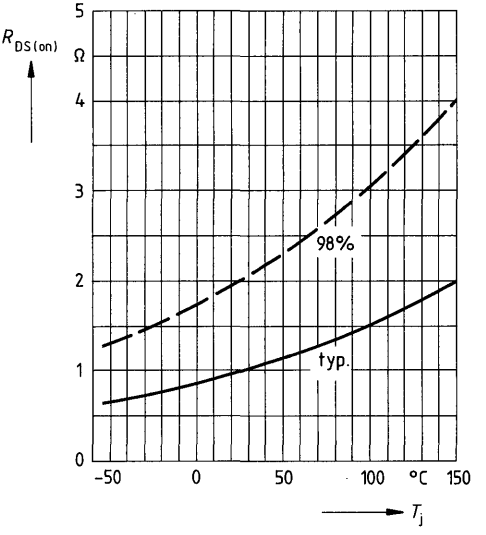
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = -25\,V$, $T_j = 25\,°C$



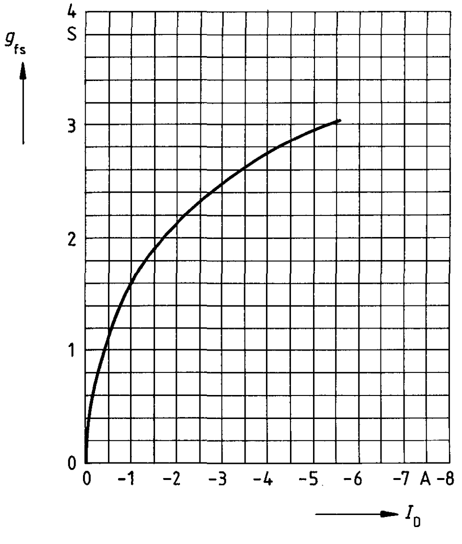
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



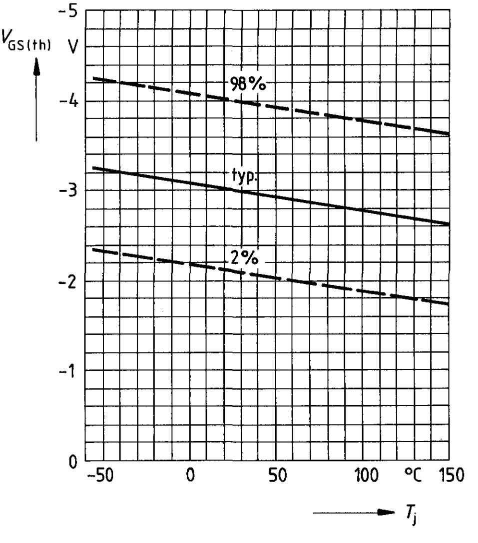
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = −2A, V_{GS} = −10V
(spread)



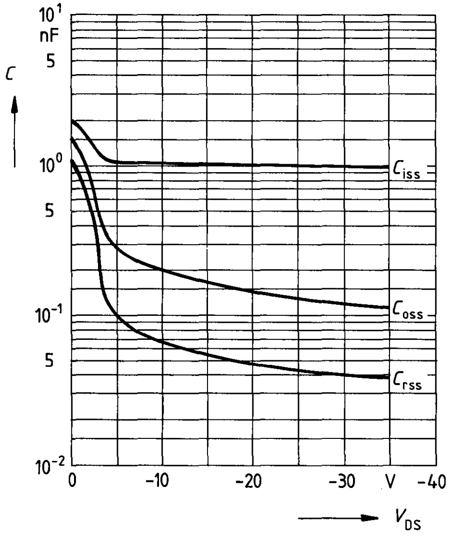
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = −25V, T_j = 25 °C



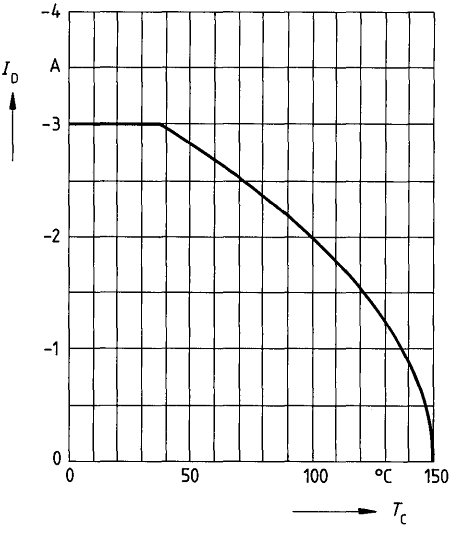
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = −1mA
(spread)



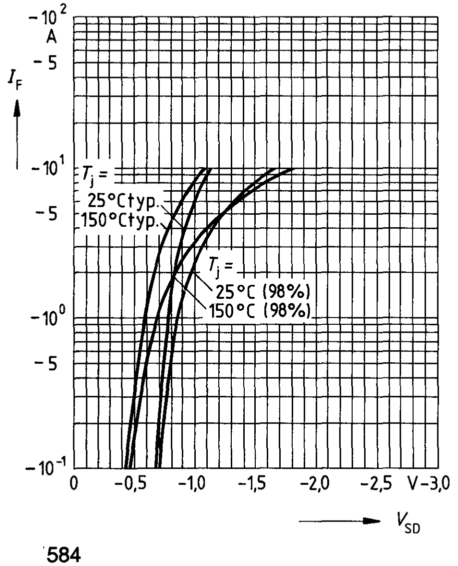
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



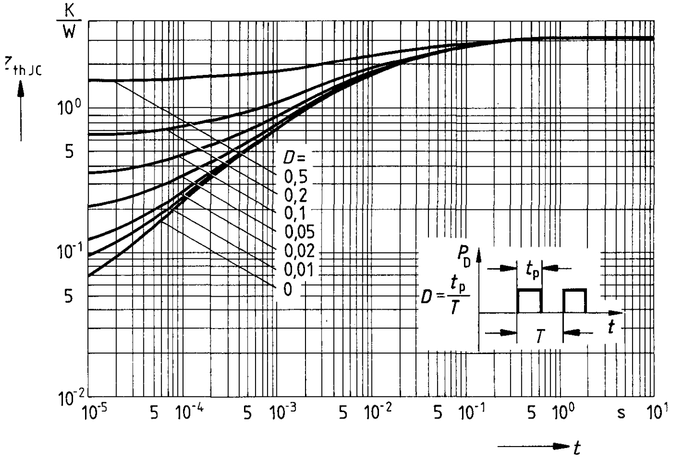
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq -10\text{V}$



Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



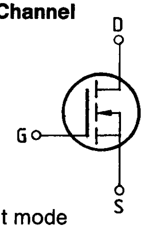
Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



Main ratings

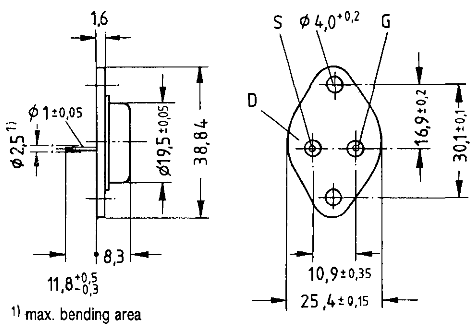
Drain-source voltage V_{DS} **= 400 V**
Continuous drain current I_D **= 12,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,4 Ω**

N-Channel



Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode
Case Metal case 3 A 2 in accordance with DIN 41872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
BUZ 201	C67078-A1101-A2



Dimensions in mm

Maximum ratings

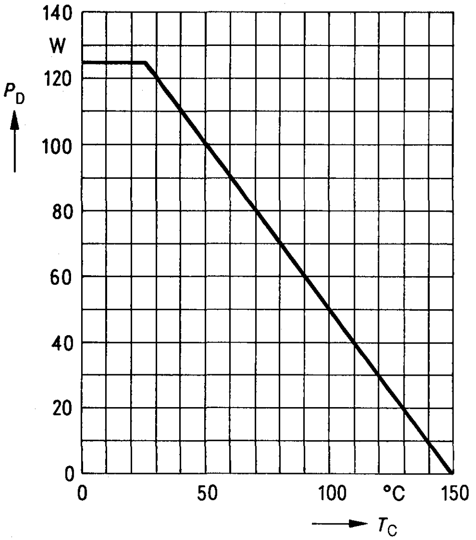
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	12,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	50	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	− 55 ... + 150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤ 35	K/W	

Electrical characteristics

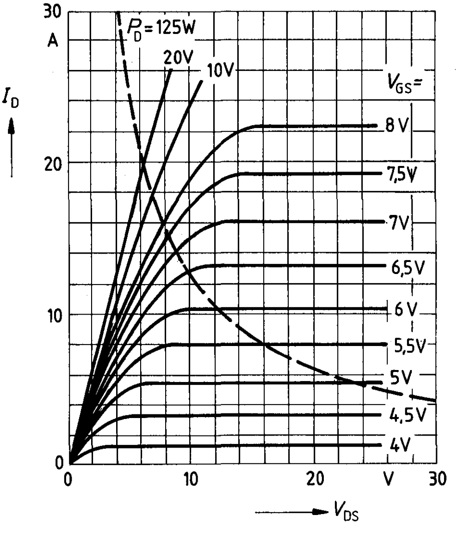
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,35	0,40	Ω	V_{GS} = 10V I_D = 8A	
Dynamic ratings							
Forward transconductance	g_{fs}	3,3	5,2	–	S	V_{DS} = 25V I_D = 8A	
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	300	500	pF		
Reverse transfer capacitance	C_{rss}	–	120	200			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	80	120			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	12,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	50			
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	$I_F = I_{DR}$ di_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reverse recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

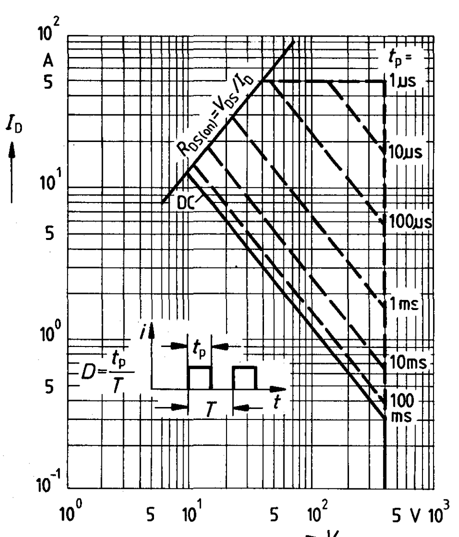
Power dissipation $P_D = f(T_C)$



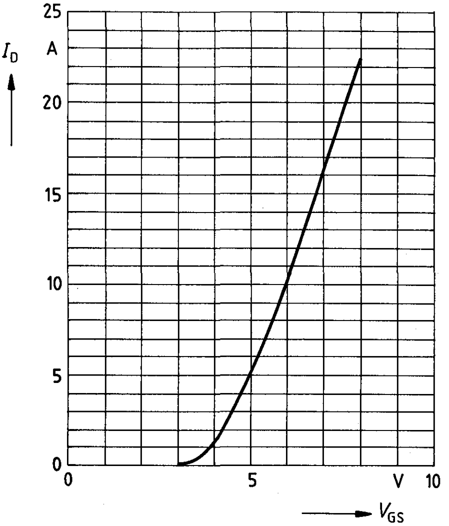
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



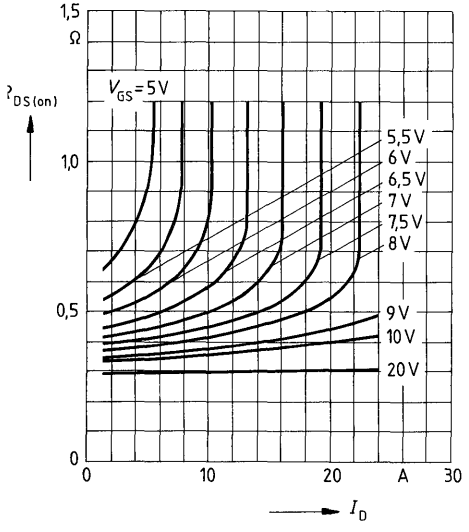
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



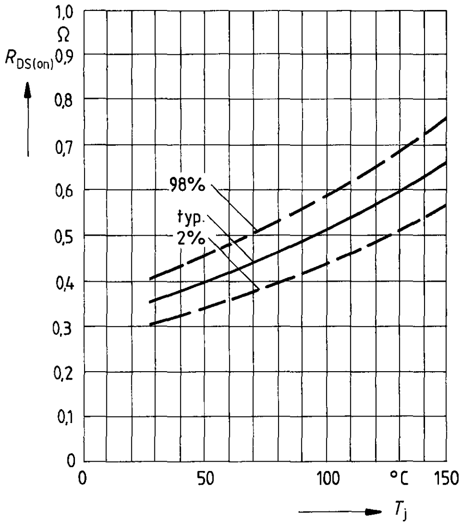
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



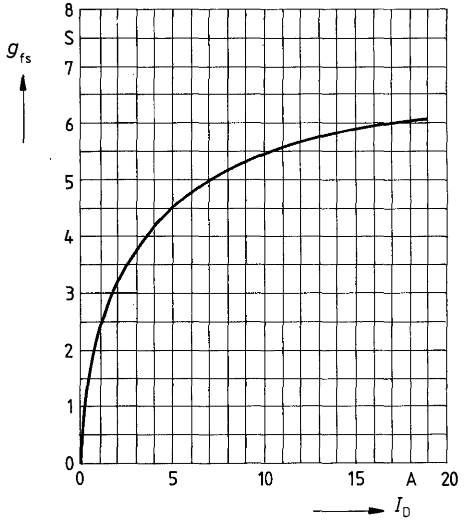
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



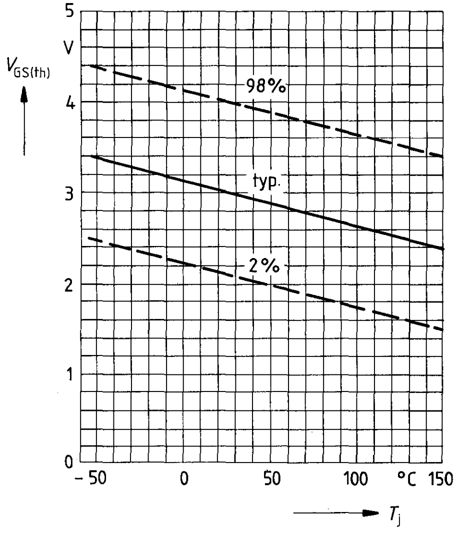
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 4{,}2A$, $V_{GS} = 10V$
(spread)



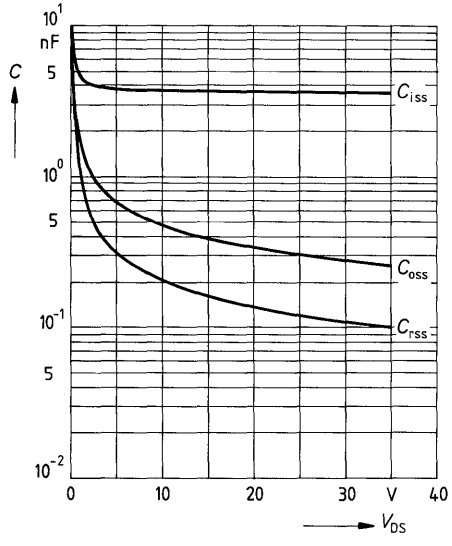
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



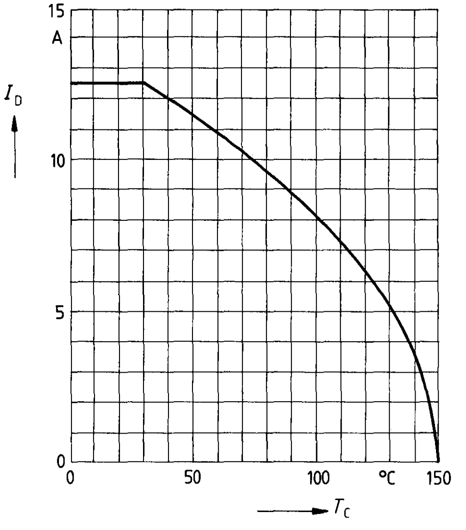
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



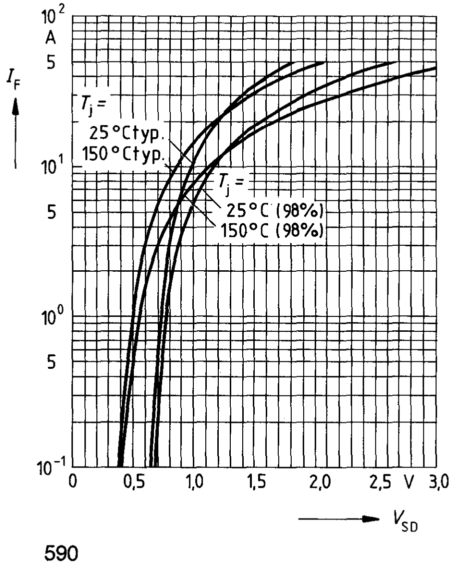
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



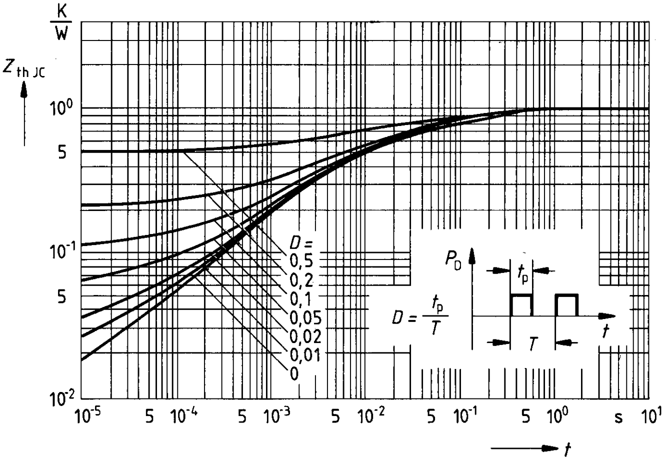
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



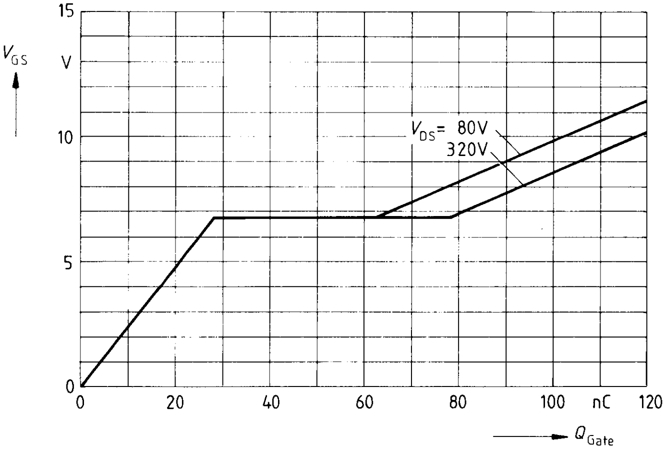
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

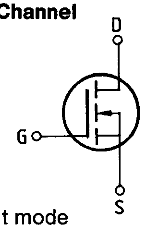


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 17{,}3A$



Main ratings

N-Channel

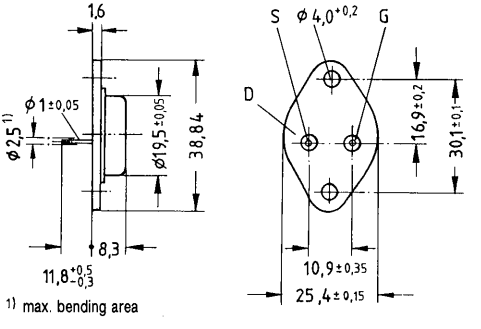


Drain-source voltage	V_{DS}	**= 400 V**
Continuous drain current	I_D	**= 11,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,5 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Metal case 3 A 2 in accordance with DIN 41 872,
or TO 204 AA (TO 3) in accordance with JEDEC.
Approx. weight 12 g

Type	Ordering code
BUZ 202	C67078-A1107-A2



Dimensions in mm

Maximum ratings

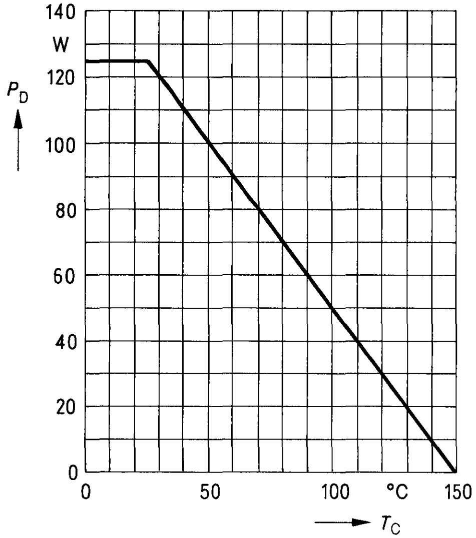
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	11,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	46	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage	T_j			
temperature range	T_{stg}	– 55 … + 150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤ 35	K/W	

Electrical characteristics

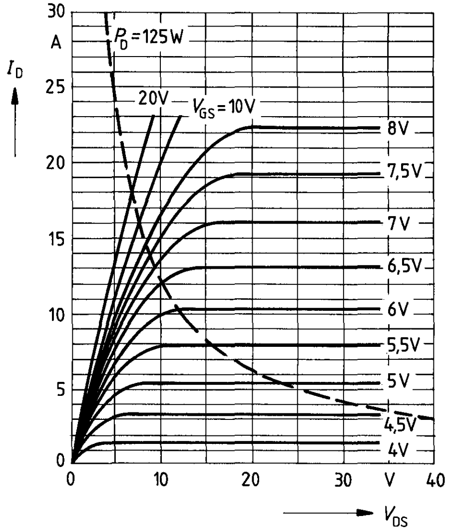
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,45	0,5	Ω	V_{GS} = 10V I_D = 8A	
Dynamic ratings							
Forward transconductance	g_{fs}	3,3	5,2	–	S	V_{DS} = 25V I_D = 8A	
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	300	500	pF		
Reverse transfer capacitance	C_{rss}	–	120	200			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	80	120			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	11,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	46			
Diode forward on-voltage	V_{SD}	–	1,4	1,9	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	$I_F = I_{DR}$ di_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

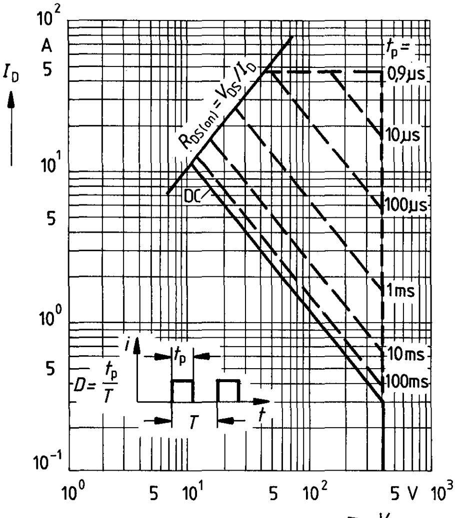
Power dissipation $P_D = f(T_C)$



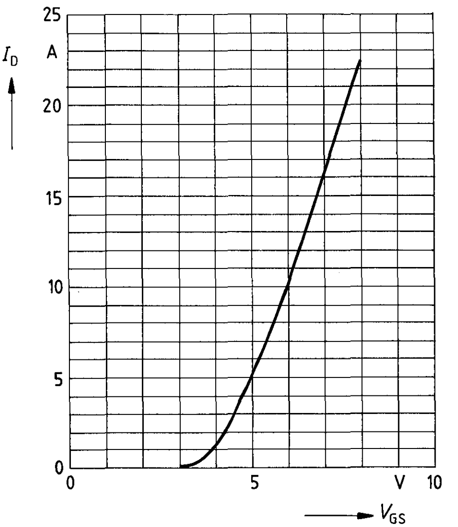
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



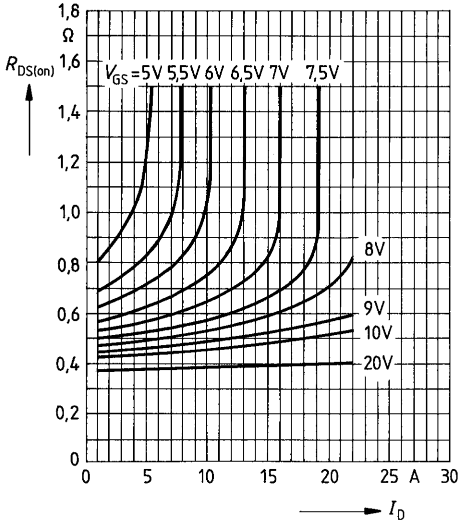
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



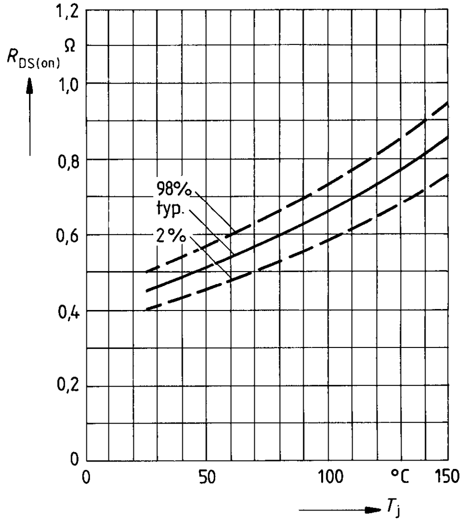
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



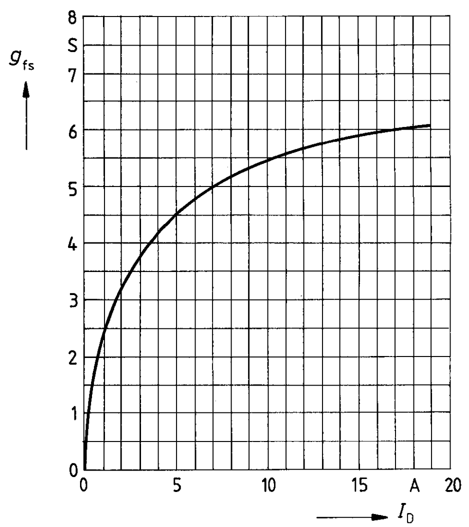
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



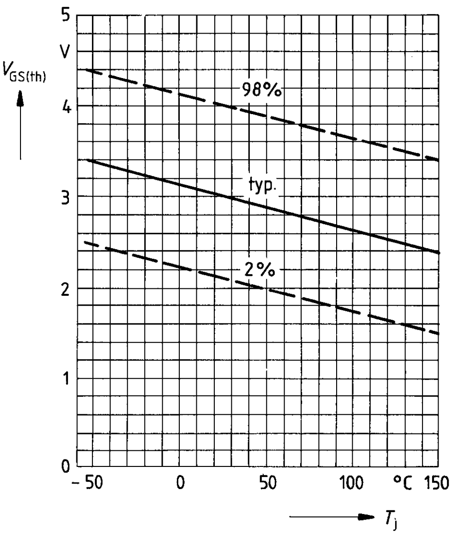
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 8A$, $V_{GS} = 10V$
(spread)



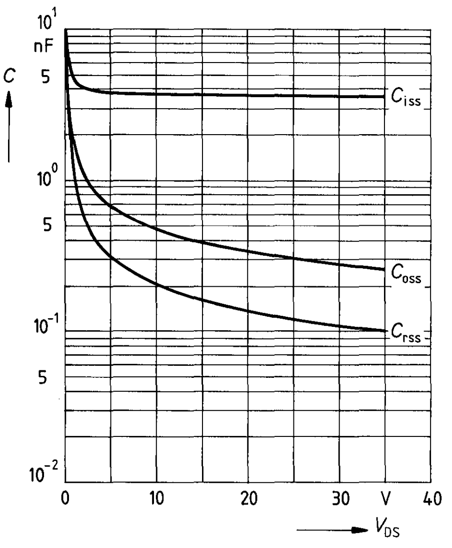
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



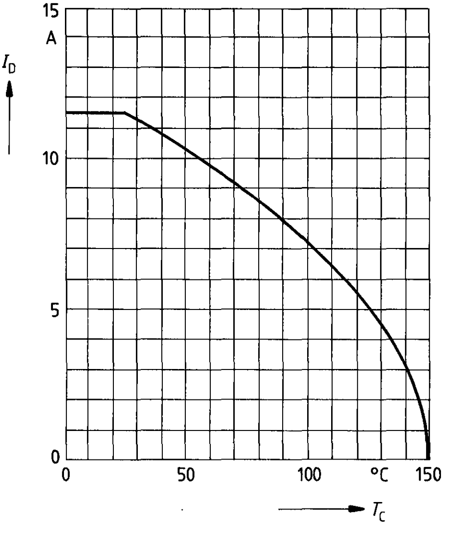
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



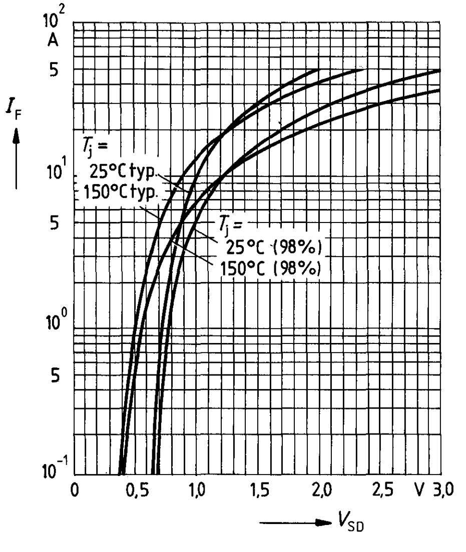
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



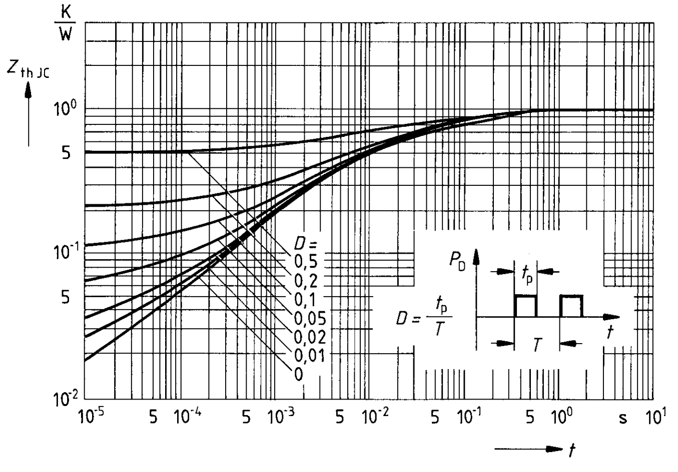
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



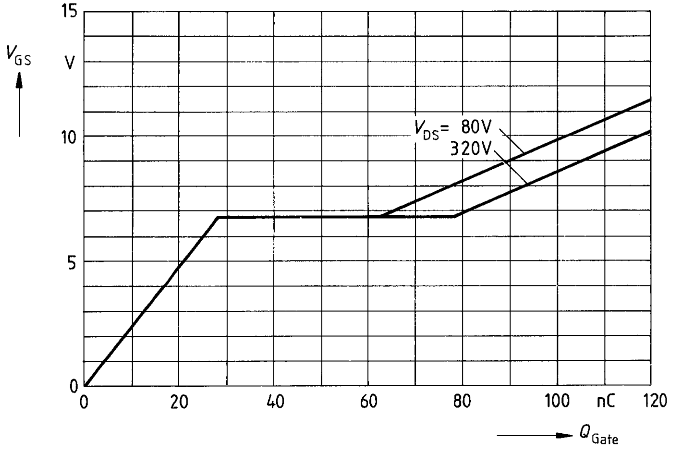
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



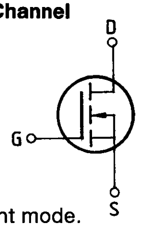
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 17{,}3\text{A}$



Main ratings

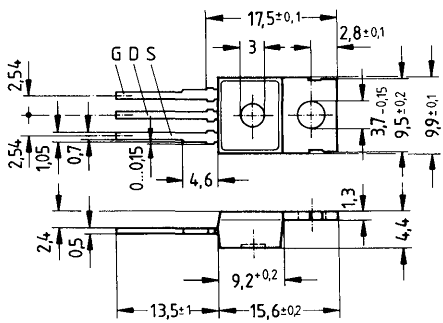
Drain-source voltage V_{DS} **= 400 V**
Continuous drain current I_D **= 6,0 A**
Drain-source on-resistance $R_{DS(on)}$ **= 1,0 Ω**

N-Channel



Description FREDFET with fast-recovery reverse diode, N-channel, enhancement mode.
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
BUZ 205	C67078-A1401-A2



Dimensions in mm

Maximum ratings

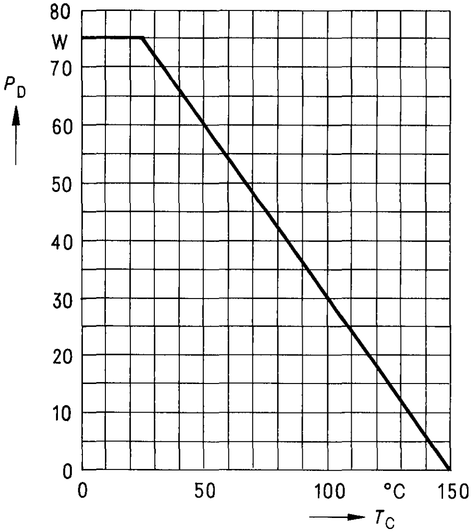
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	6,0	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	24	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage	T_j			
temperature range	T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤75	K/W	

Electrical characteristics

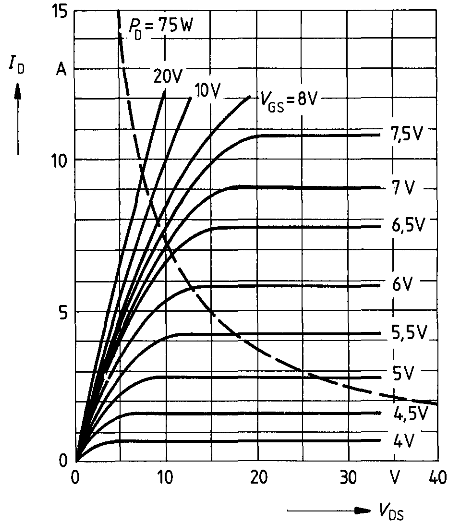
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,9	1,0	Ω	V_{GS} = 10V I_D = 4A
Dynamic ratings						
Forward transconductance	g_{fs}	1,7	2,9	–	S	V_{DS} = 25V I_D = 4A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	120	180	pF	
Reverse transfer capacitance	C_{rss}	–	35	60		
Turn-on time t_{on} (t_{on} = $t_{d\,(on)}$ + t_r)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,7A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} (t_{off} = $t_{d\,(off)}$ + t_f)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	6,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	24		
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; I_F = I_{DR}, di_F/dt = 100A/µs, V_R = 100V
		–	220	300		= 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C
		–	2,6	5,0		= 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		= 150 °C

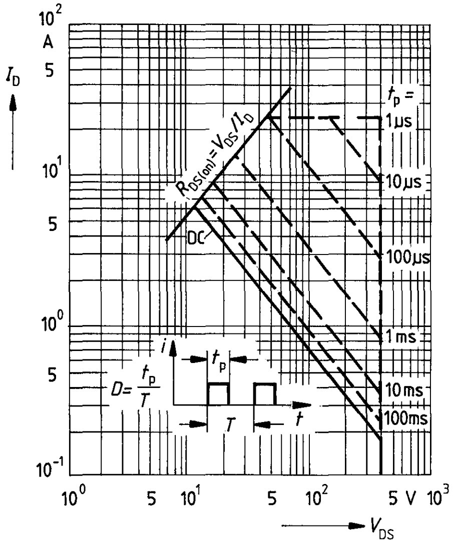
Power dissipation $P_D = f(T_C)$



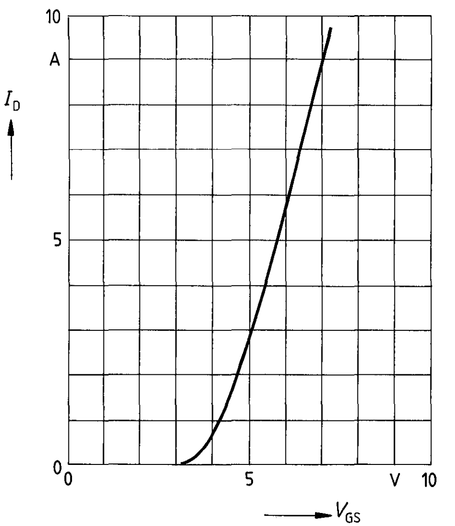
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



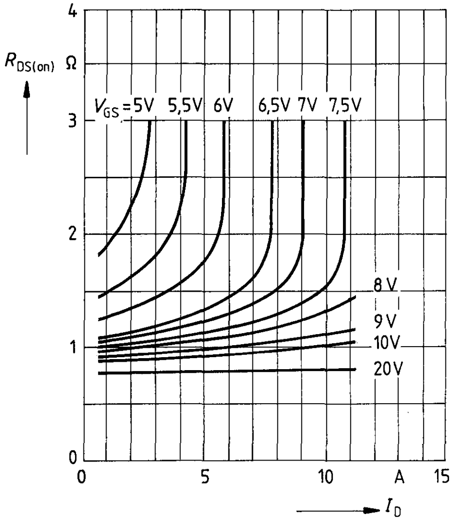
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



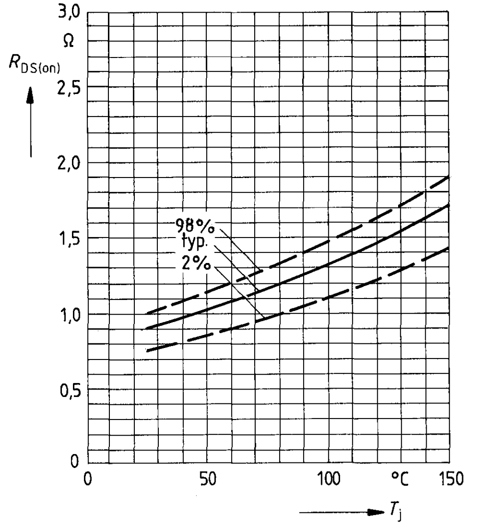
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



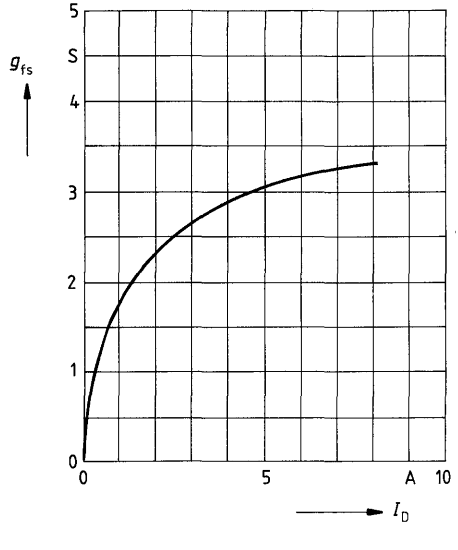
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



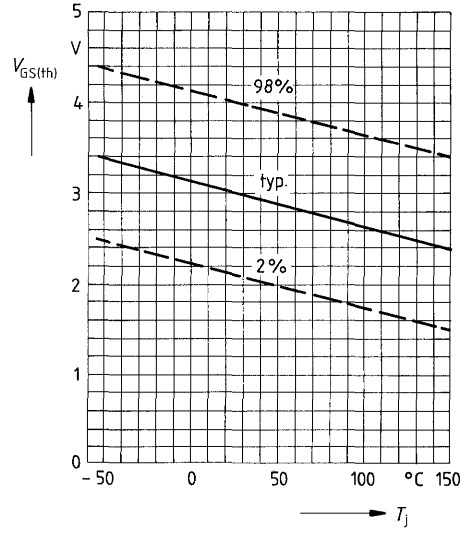
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 4A, V_{GS} = 10V
(spread)



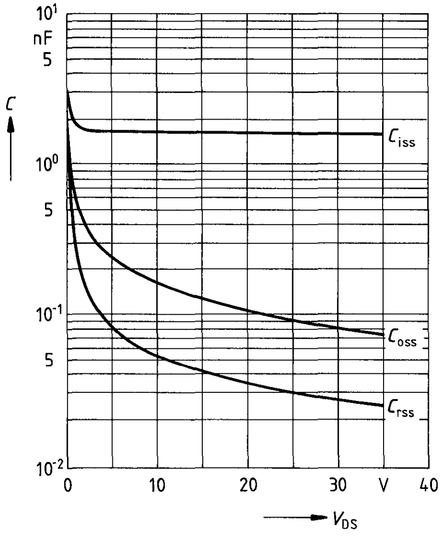
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



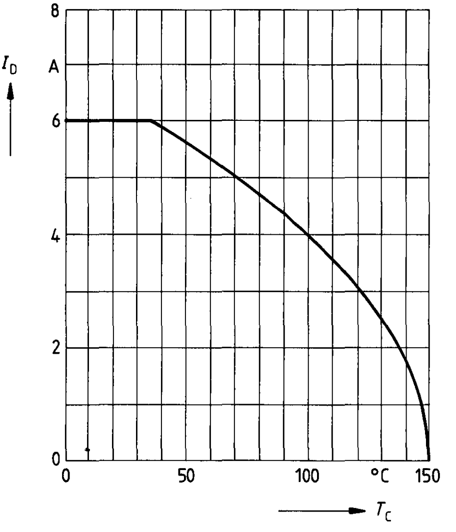
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



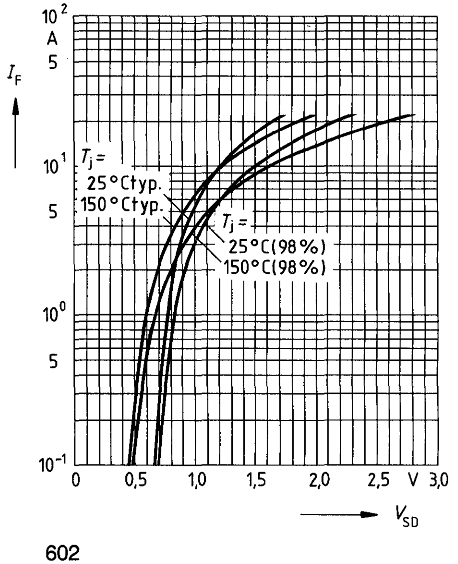
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f =$ 1MHz



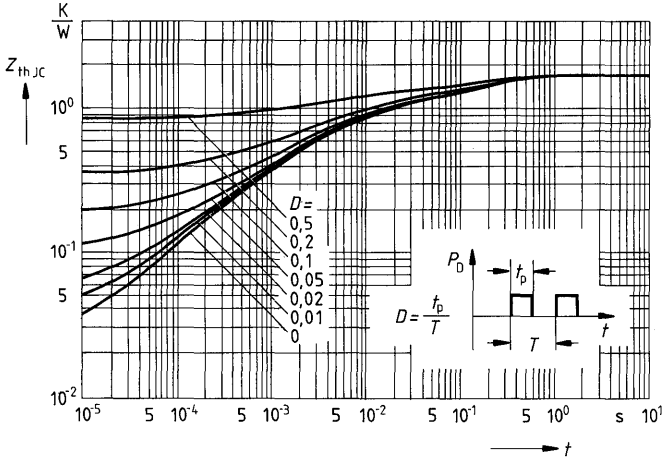
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq$ 10V



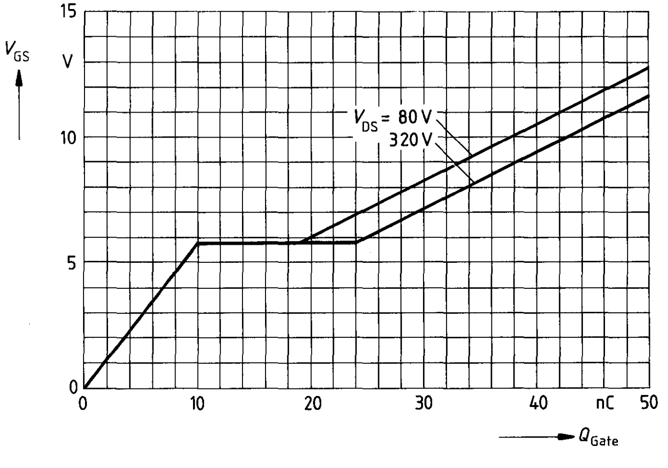
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, t_p = 80 µs
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



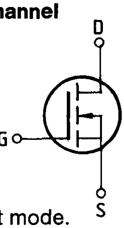
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 8{,}3A$



Main ratings

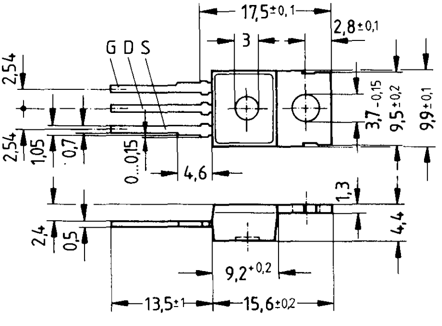
Drain-source voltage V_{DS} **= 400 V**
Continuous drain current I_D **= 5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 1,5 Ω**

N-Channel



Description FREDFET with fast-recovery reverse diode, N-channel, enhancement mode.
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
BUZ 206	C67078-A1403-A2



Dimensions in mm

Maximum ratings

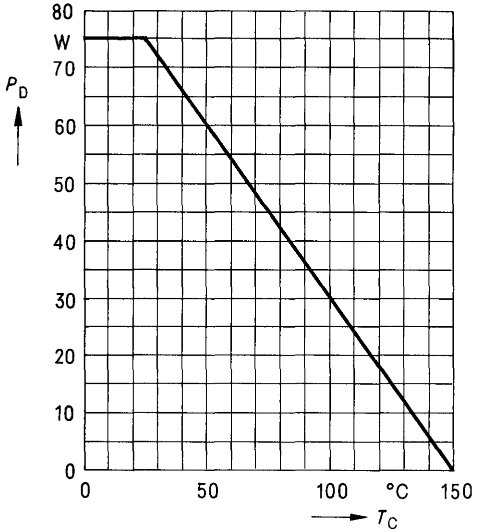
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	20	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤ 1,67	K/W	
Chip – ambient	$R_{th\ JA}$	≤ 75	K/W	

Electrical characteristics

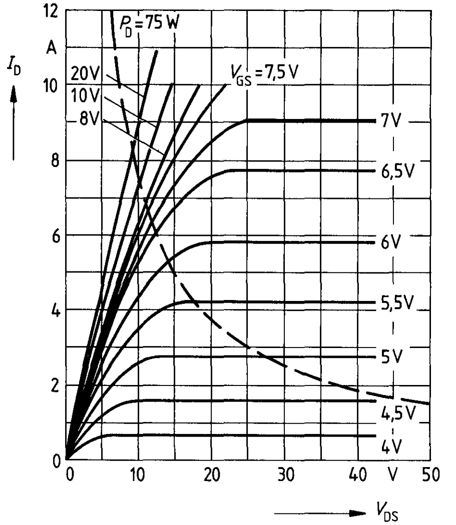
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,3	1,5	Ω	V_{GS} = 10V I_D = 4A
Dynamic ratings						
Forward transconductance	g_{fs}	1,7	2,9	–	S	V_{DS} = 25V I_D = 4A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	120	180	pF	
Reverse transfer capacitance	C_{rss}	–	35	60		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	20		
Diode forward on-voltage	V_{SD}	–	1,4	1,8	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; $I_F = I_{DR}$, di_F/dt = 100A/µs, V_R = 100V
		–	220	300		T_j = 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C
		–	2,6	5,0		T_j = 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		T_j = 150 °C

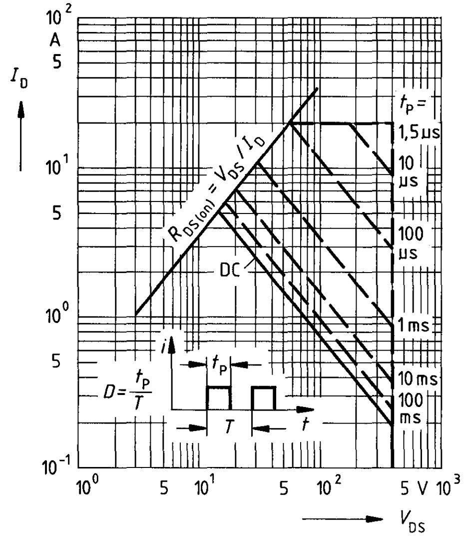
Power dissipation $P_D = f(T_C)$



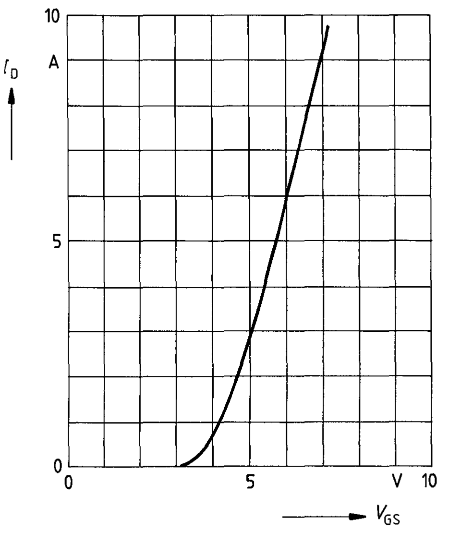
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



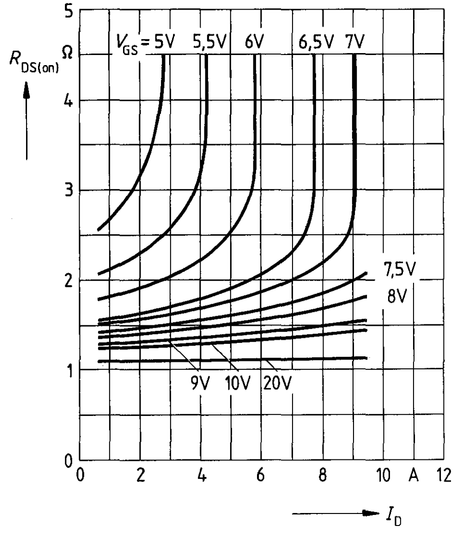
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



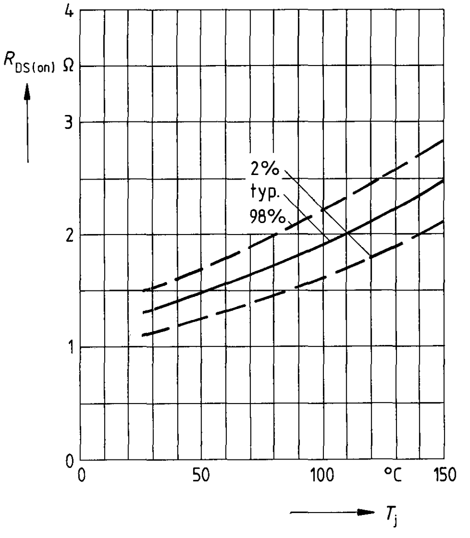
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



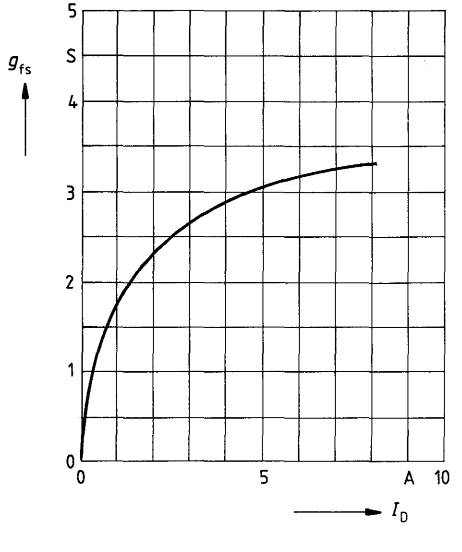
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



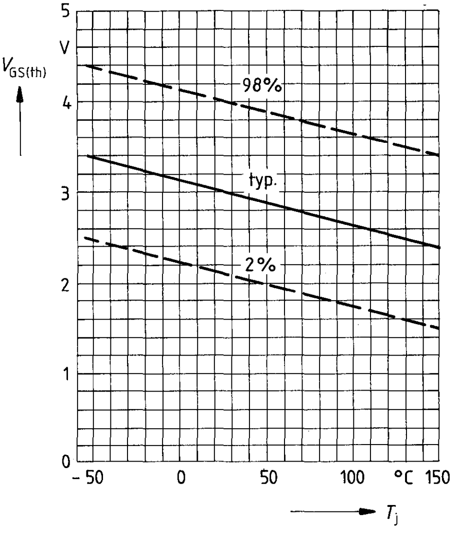
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 4A, V_{GS} = 10V
(spread)



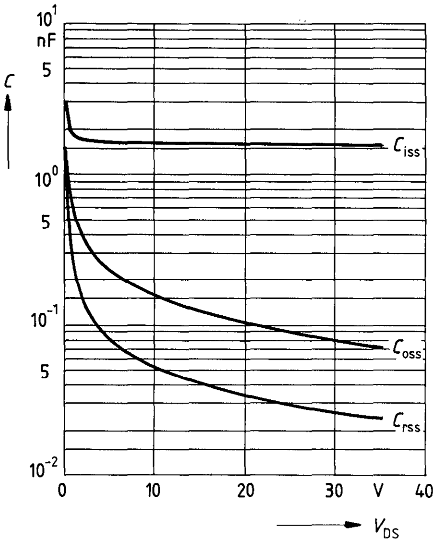
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



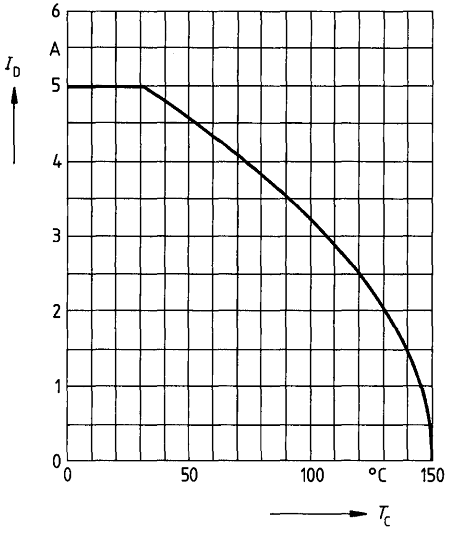
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



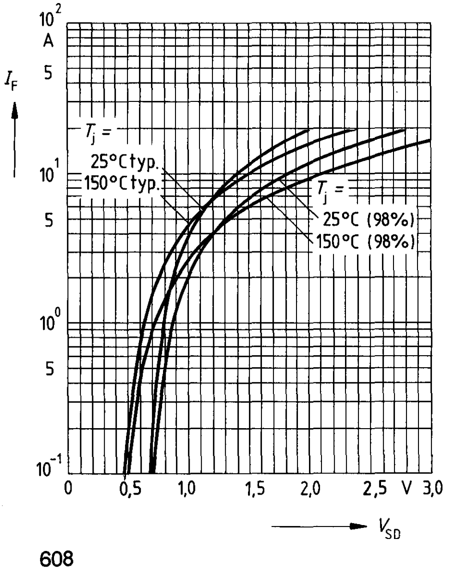
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



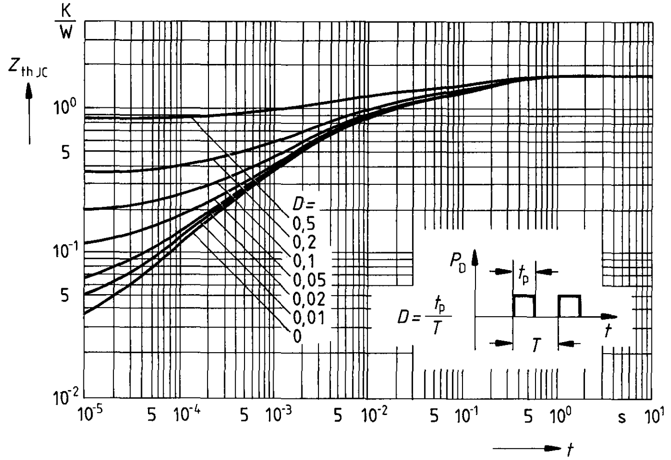
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



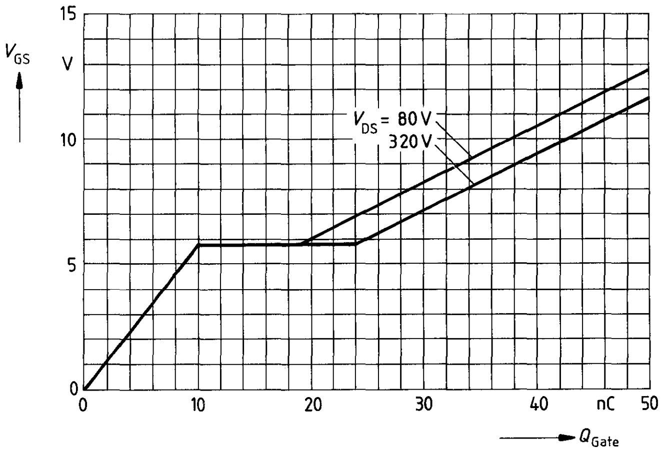
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

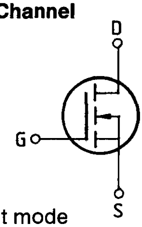


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 8{,}3\text{A}$



Main ratings

N-Channel

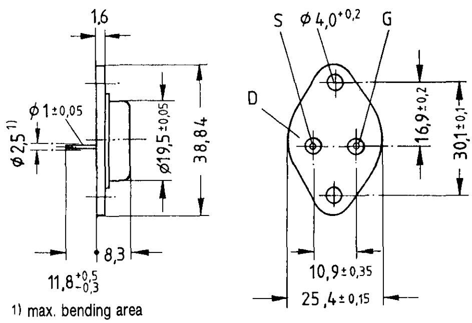


Drain-source voltage	V_{DS}	**= 500 V**
Continuous drain current	I_D	**= 10,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,6 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Metal case 3A2 in accordance with DIN 41872,
or TO 204 AA (TO 3) in accordance with JEDEC.
Approx. weight 12 g

Type	Ordering code
S BUZ 210	C67078-A1102-A2



Dimensions in mm

Maximum ratings

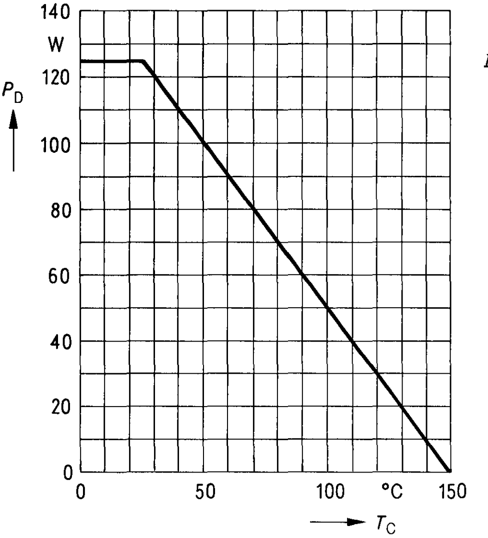
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	10,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	42	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤ 35	K/W	

Electrical characteristics

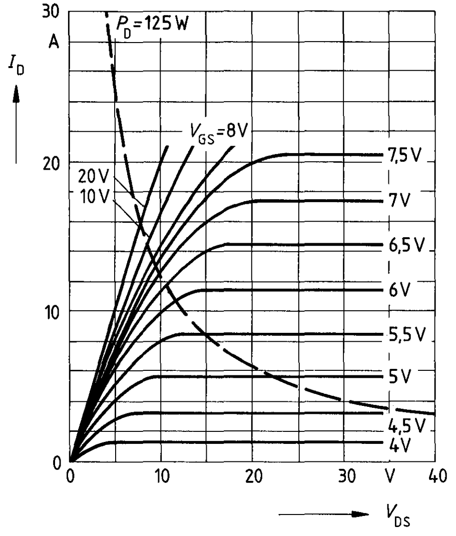
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,55	0,6	Ω	V_{GS} = 10V I_D = 6,5A	
Dynamic ratings							
Forward transconductance	g_{fs}	2,7	5,3	–	S	V_{DS} = 25V I_D = 6,5A	
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	250	400	pF		
Reverse transfer capacitance	C_{rss}	–	100	170			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	80	120			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	10,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	42			
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	$I_F = I_{DR}$ di_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

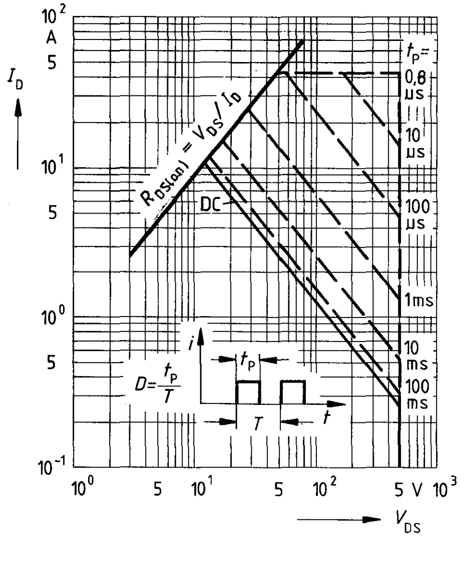
Power dissipation $P_D = f(T_C)$



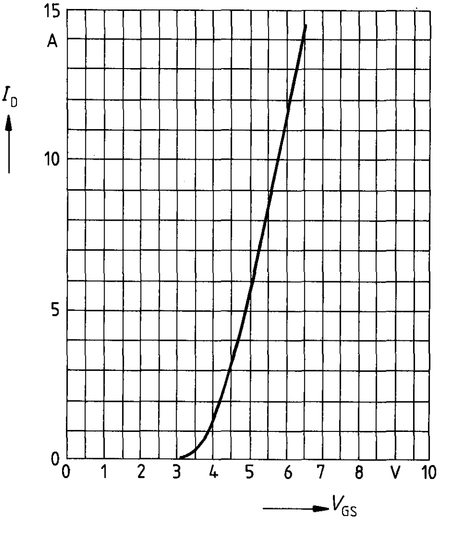
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



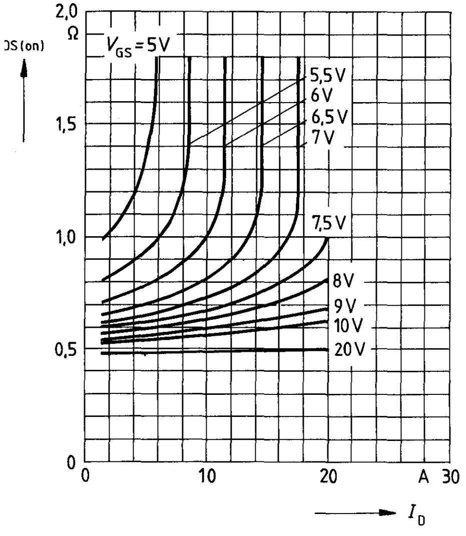
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



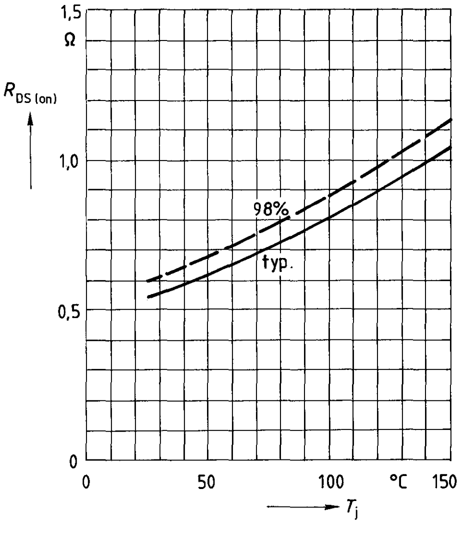
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



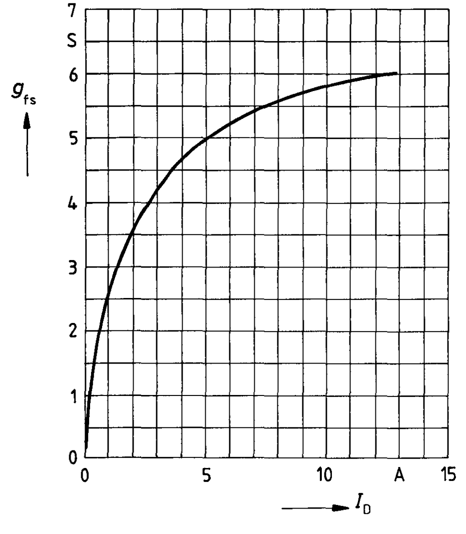
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



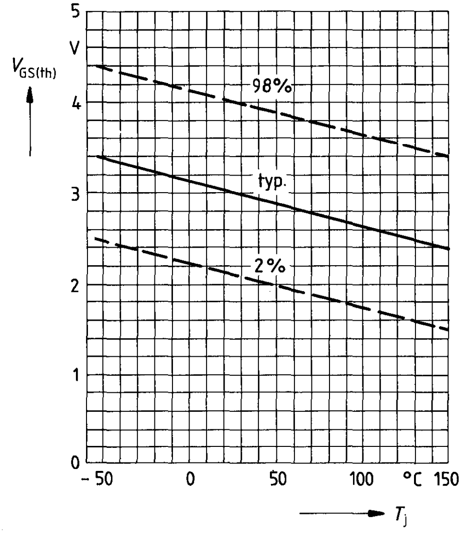
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 6{,}5A$, $V_{GS} = 10V$
(spread)



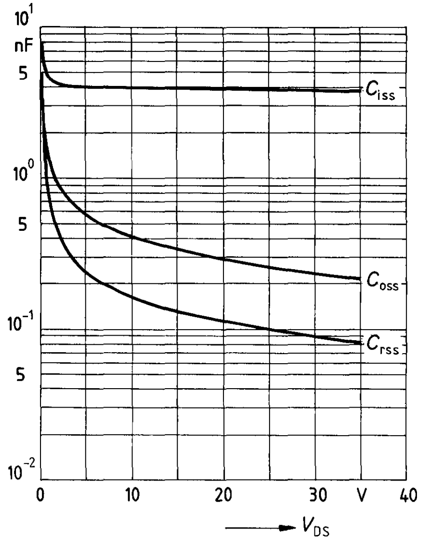
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



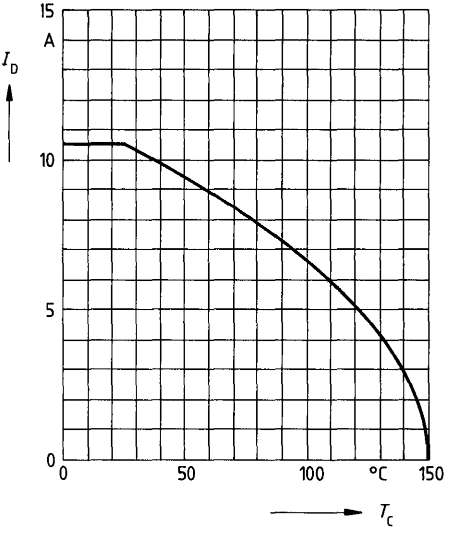
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



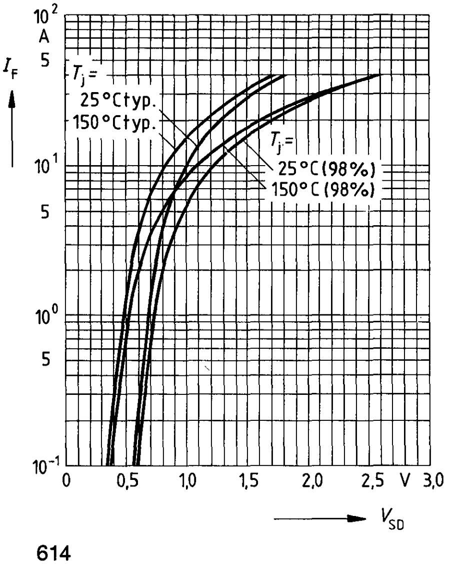
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



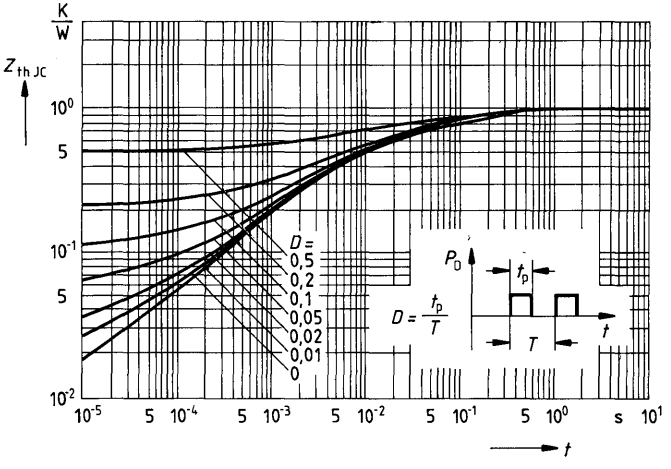
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



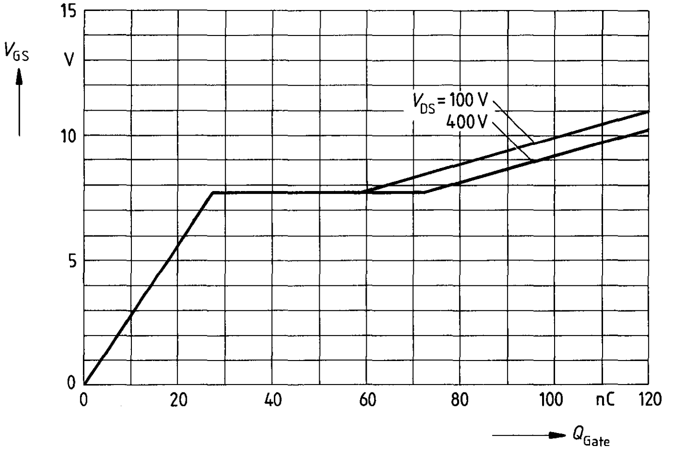
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

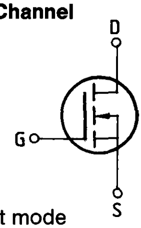


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14{,}4$A



Main ratings

N-Channel

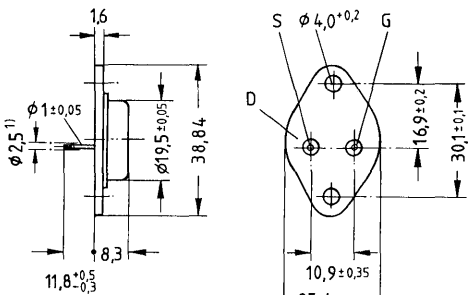


Drain-source voltage	V_{DS}	=	**500 V**
Continuous drain current	I_D	=	**9 A**
Drain-source on-resistance	$R_{DS(on)}$	=	**0,8 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
S BUZ 211	C67078-A1100-A2



1) max. bending area

Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	9	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	36	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\,JC}$	≤ 1,0	K/W
Chip – ambient	$R_{th\,JA}$	≤ 35	K/W

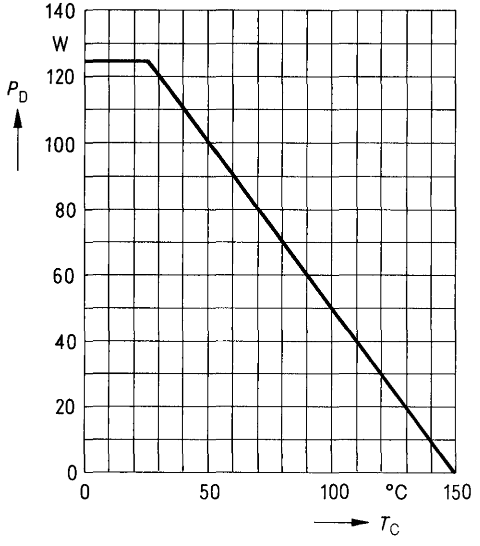
 S Preferred Type

Electrical characteristics

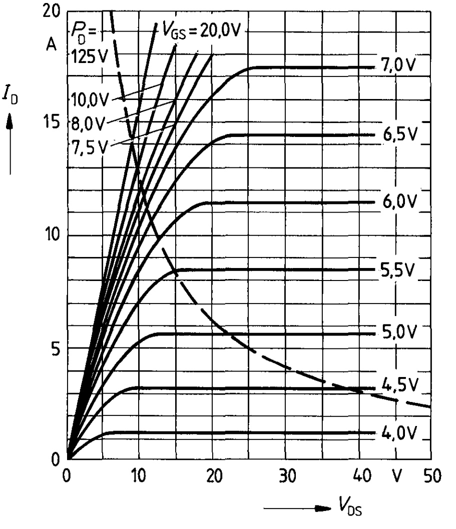
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics			Unit	Conditions
		min.	typ.	max.		
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,7	0,8	Ω	V_{GS} = 10V I_D = 6,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	5,3	–	S	V_{DS} = 25V I_D = 6,5A
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400	pF	
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	9	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	36		
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; I_F = I_{DR}, di_F/dt = 100A/µs, V_R = 100V
		–	220	300		T_j = 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C; I_F = I_{DR}, di_F/dt = 100A/µs, V_R = 100V
		–	2,6	5,0		T_j = 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		T_j = 150 °C

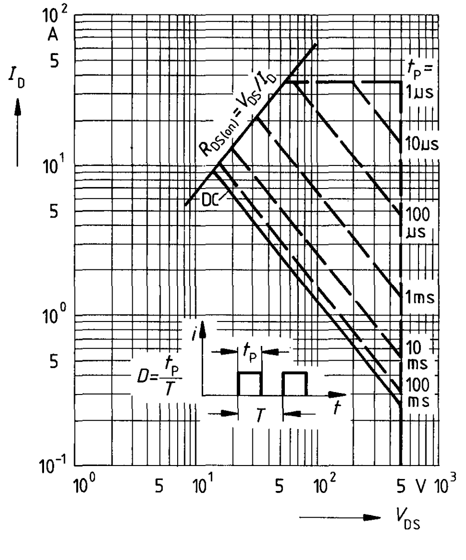
Power dissipation $P_D = f(T_C)$



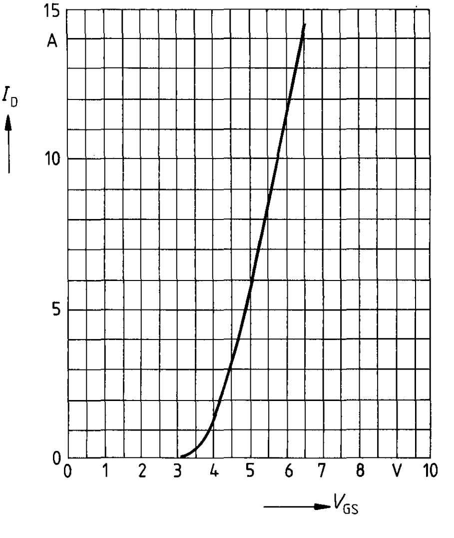
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



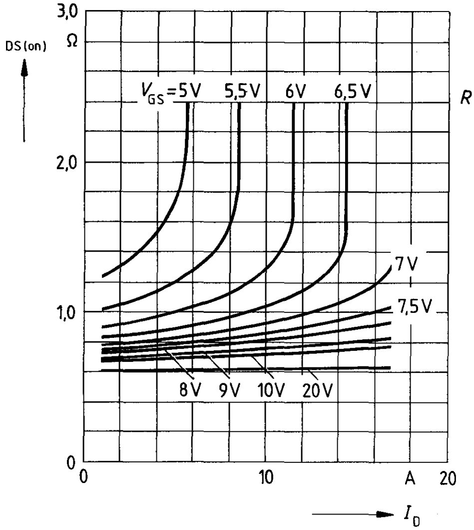
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



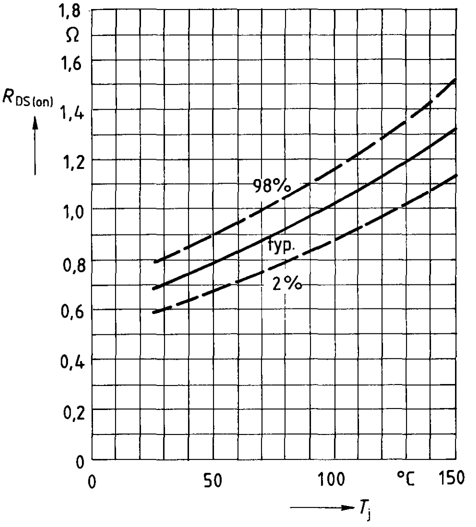
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



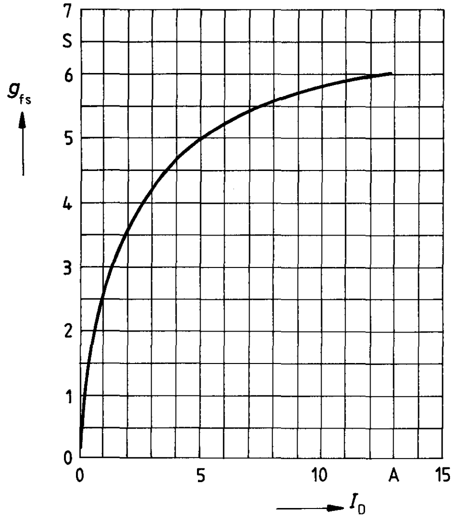
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



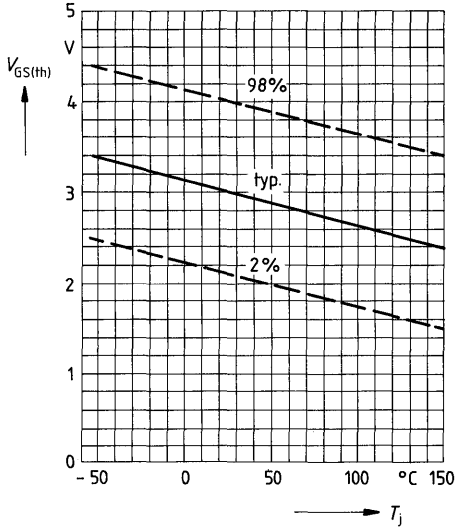
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 6,5A, V_{GS} = 10V
(spread)



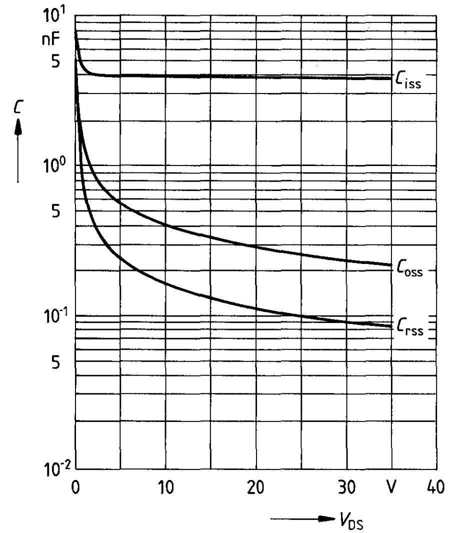
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



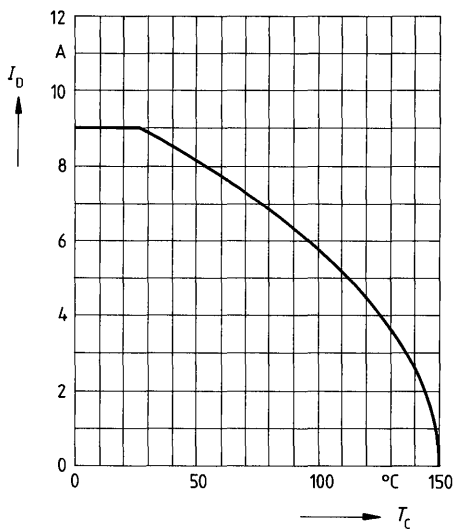
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



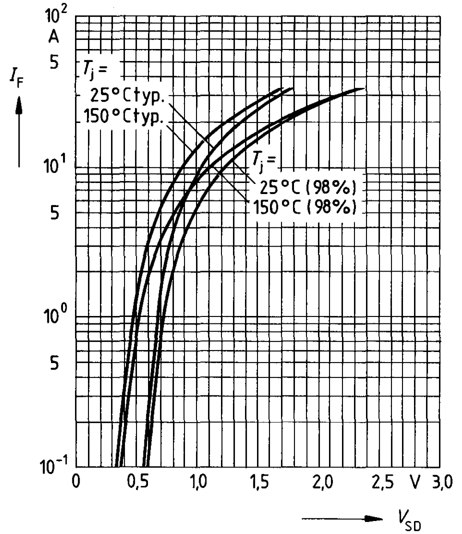
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



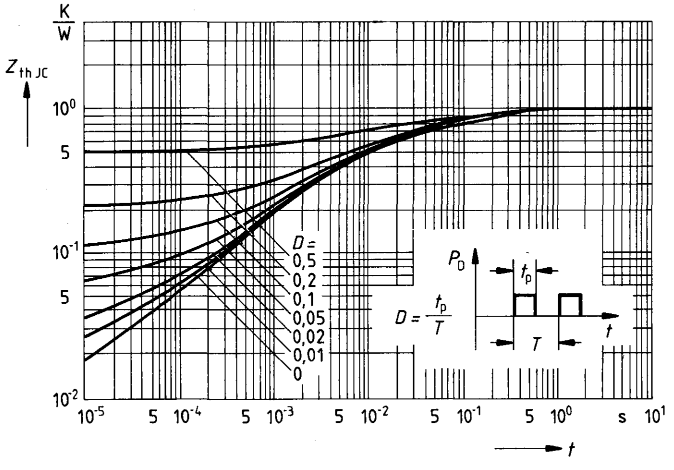
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



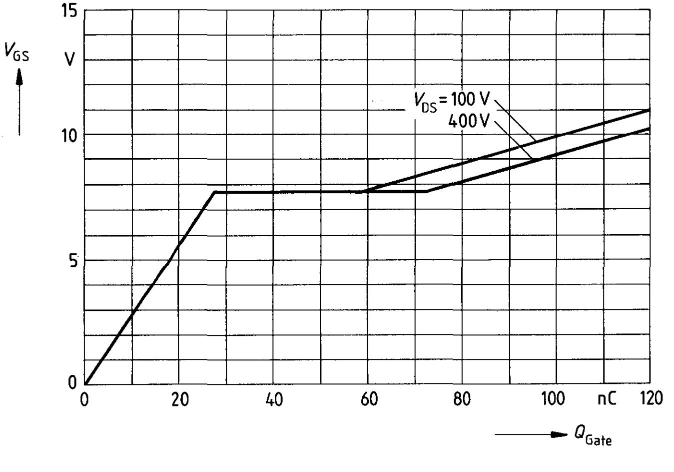
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



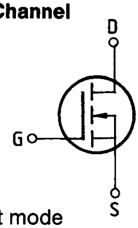
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14{,}4A$



Main ratings

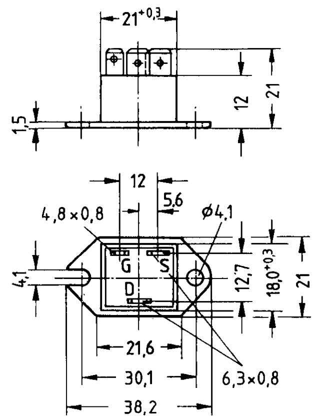
Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 8,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,6 Ω**

N-Channel



Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 213	C67078-A1700-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	8,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	34	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 … +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1])	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\ JC}$	≤1,5	K/W	

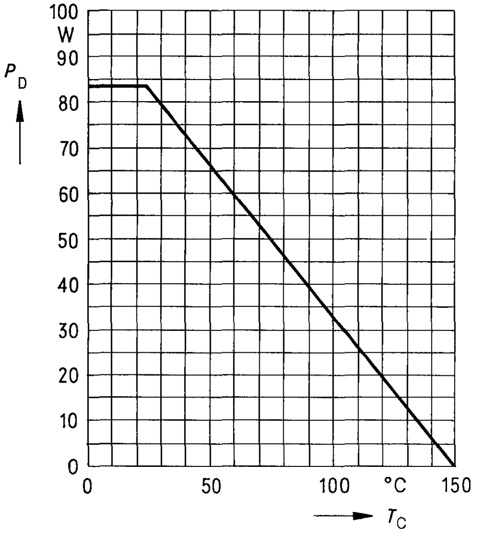
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

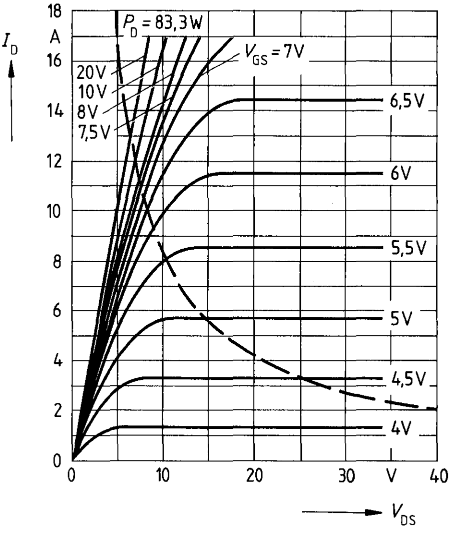
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS(on)}$	–	0,55	0,6	Ω	V_{GS} = 10V I_D = 5,5A	
Dynamic ratings							
Forward transconductance	g_{fs}	2,7	5,3	–	S	V_{DS} = 25V I_D = 5,5A	
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	250	400	pF		
Reverse transfer capacitance	C_{rss}	–	100	170			
Turn-on time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	80	120			
Turn-off time t_{off} (t_{off} = $t_{d(off)}$ + t_f)	$t_{d(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	8,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	34			
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	I_F = I_{DR} di_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

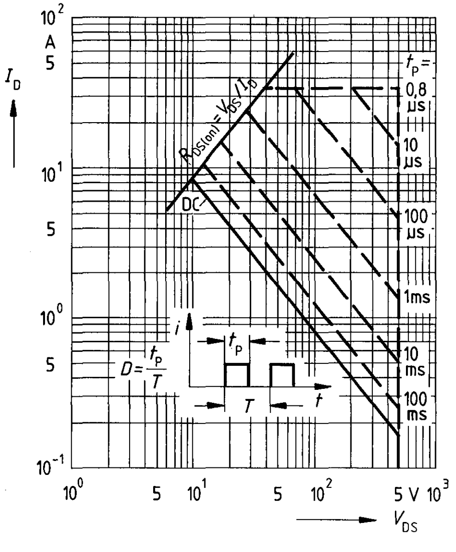
Power dissipation $P_D = f(T_C)$



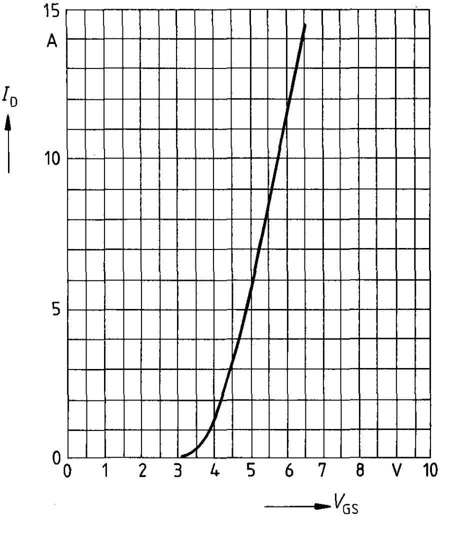
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



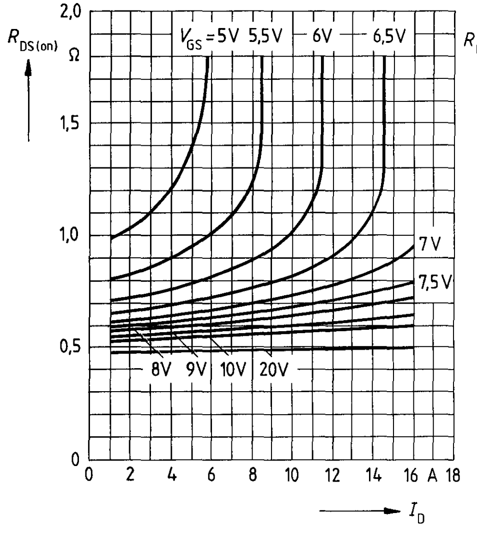
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



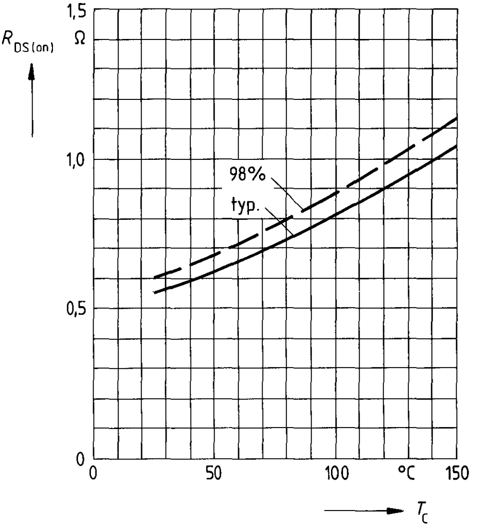
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



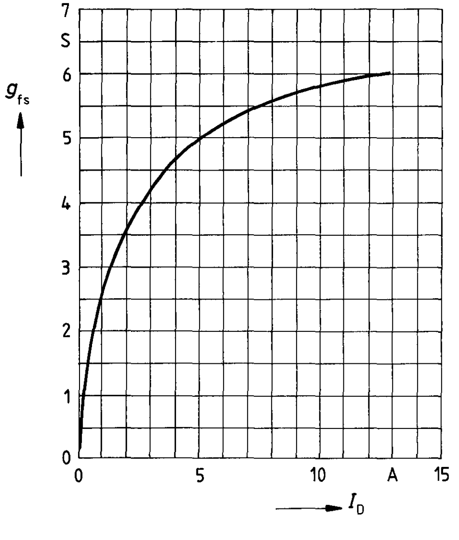
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



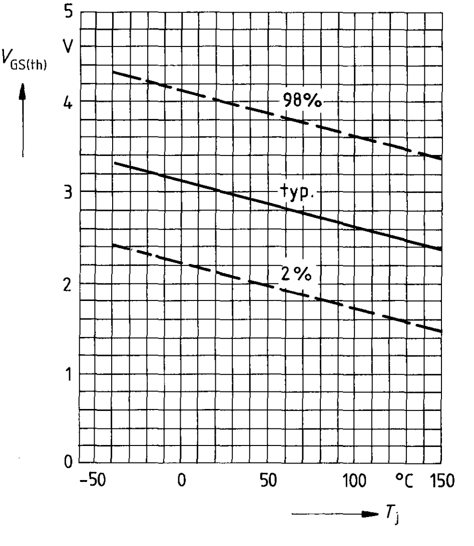
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 5,5A, V_{GS} = 10V
(spread)



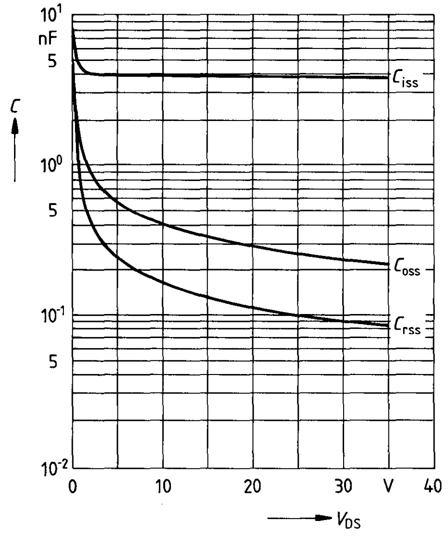
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



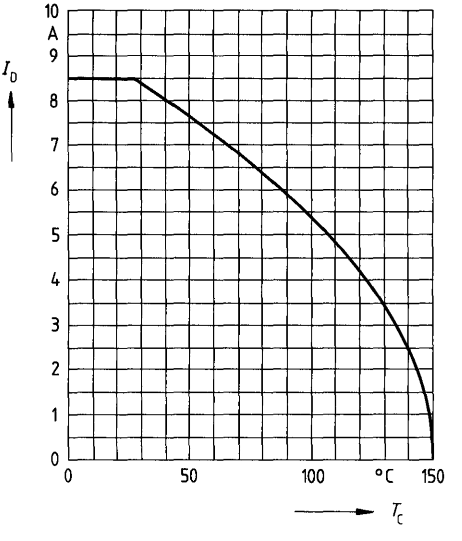
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



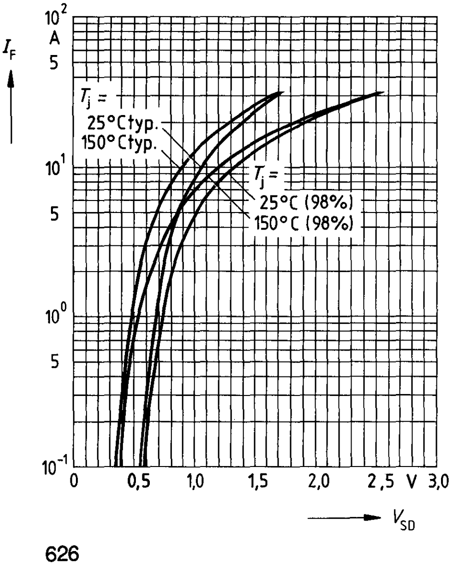
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



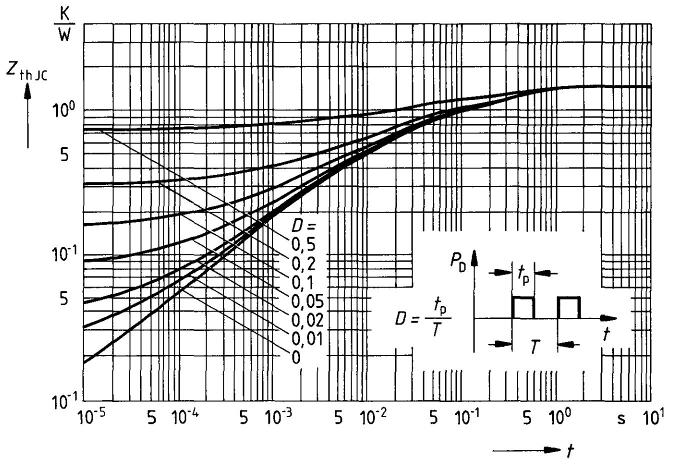
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



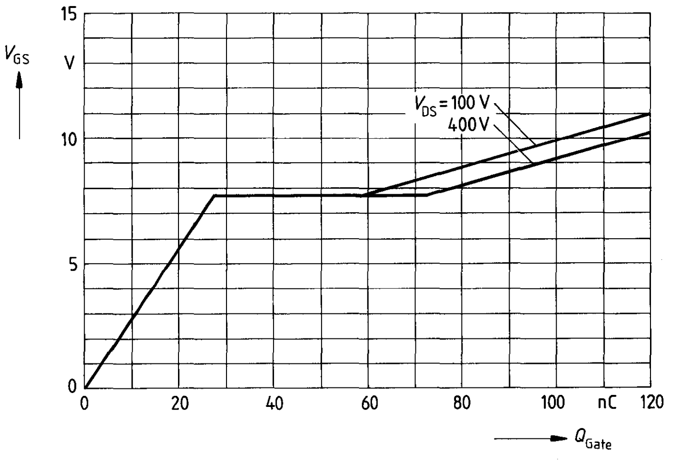
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

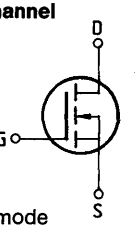


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14{,}4A$



Main ratings

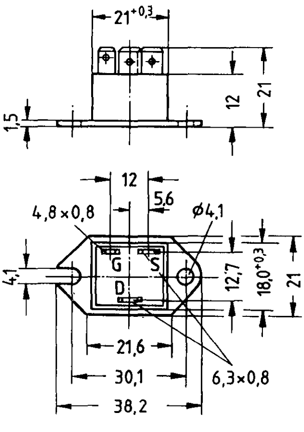
N-Channel



Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 7 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,8 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode
Case Plastic package TO 238 AA with insulated metal base plate in accordance with JEDEC, compatible with TO 3; AMP plug-in connections.
Approx. weight 21 g

Type	Ordering code
BUZ 214	C67078-A1701-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	7	A	T_C = 40 °C
Pulsed drain current	I_{Dpuls}	28	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	83,3	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−40 … +150	°C	
Isolation test voltage	V_{is}	3500	Vdc[1]	t = 1 min
DIN humidity category		F	–	DIN 40040
IEC climatic category		40/150/56		DIN IEC 68-1

Thermal resistance

Chip – case	$R_{th\,JC}$	≤1,5	K/W	

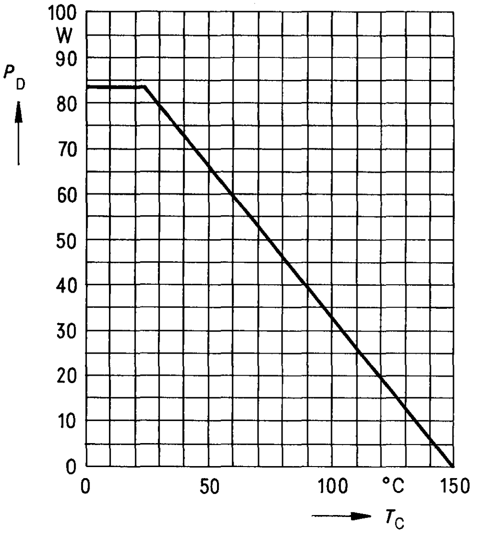
[1]) Isolation test voltage between drain and base plate referred to standard climate 23/50 in accordance with DIN 50014.

Electrical characteristics

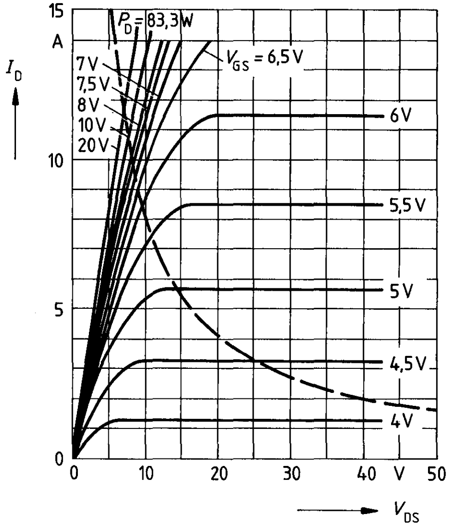
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	μA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,7	0,8	Ω	V_{GS} = 10V I_D = 5,5A	
Dynamic ratings							
Forward transconductance	g_{fs}	2,7	5,3	–	S	V_{DS} = 25V I_D = 5,5A	
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	250	400	pF		
Reverse transfer capacitance	C_{rss}	–	100	170			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	80	120			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	7	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	28			
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	$I_F = I_{DR}$ di_F/dt = 100A/μs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	μC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

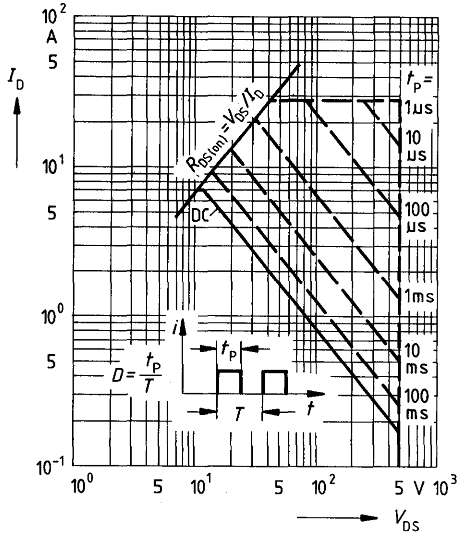
Power dissipation $P_D = f(T_C)$



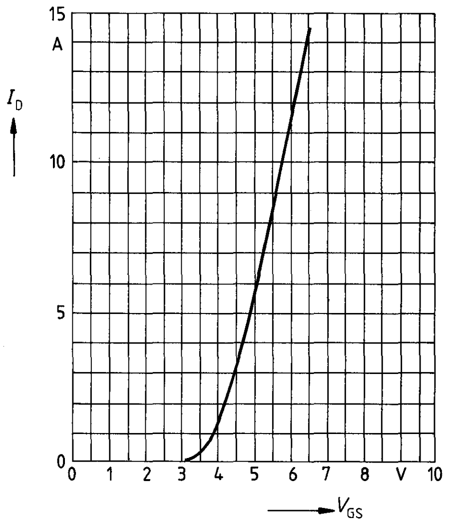
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



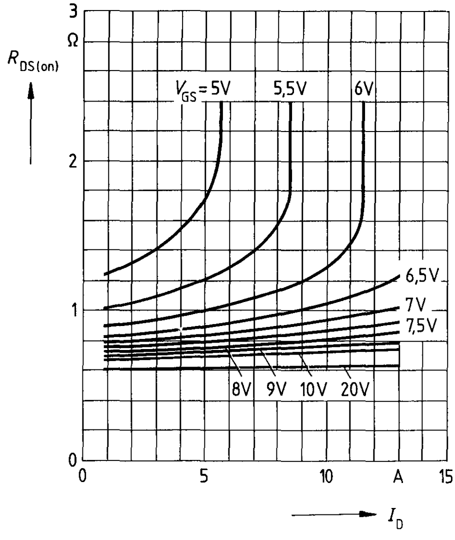
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



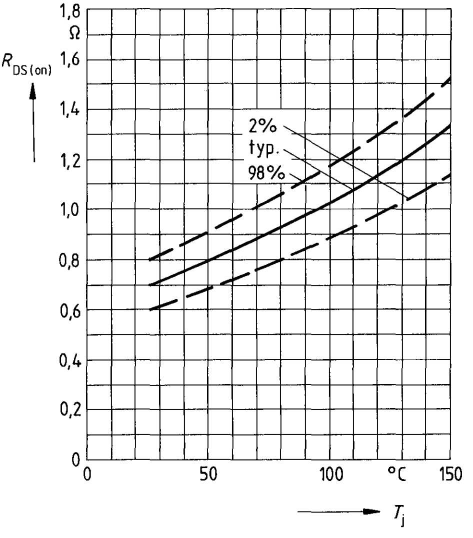
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25$ V, $T_j = 25\,°C$



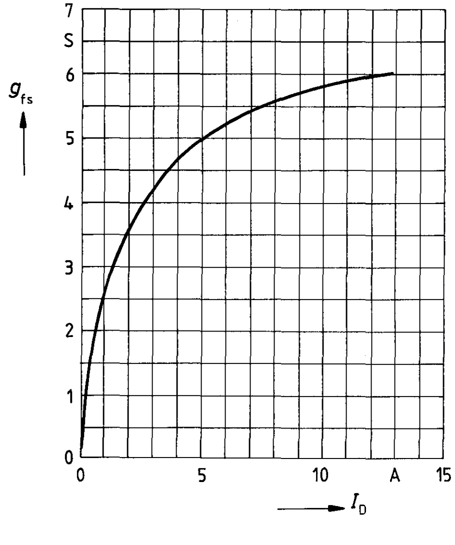
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



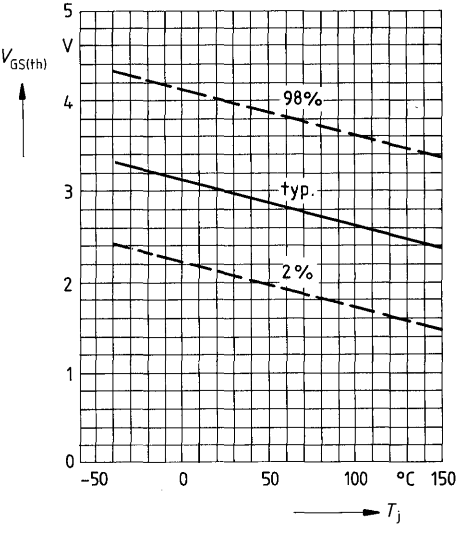
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 5{,}5A$, $V_{GS} = 10V$
(spread)



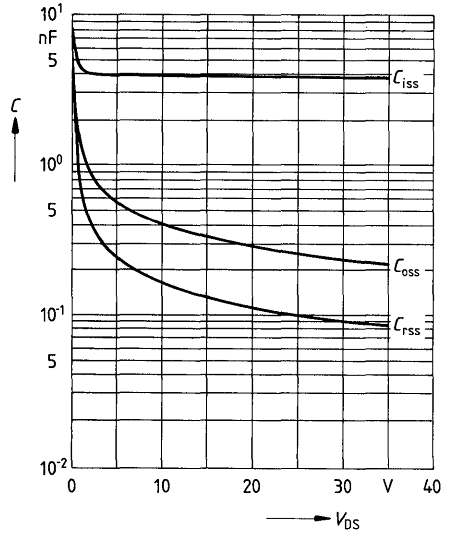
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



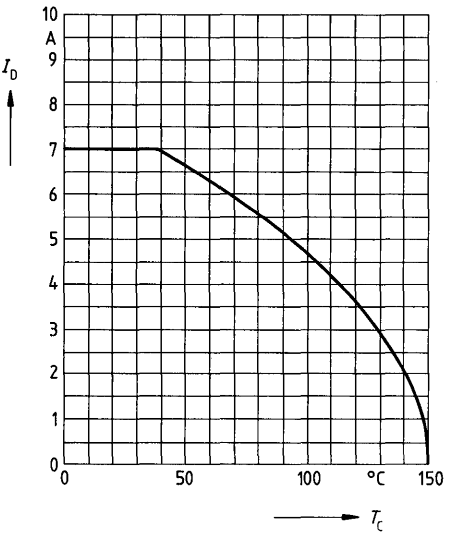
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



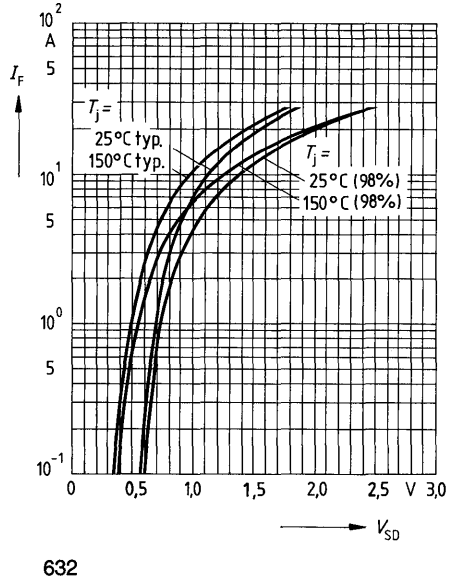
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



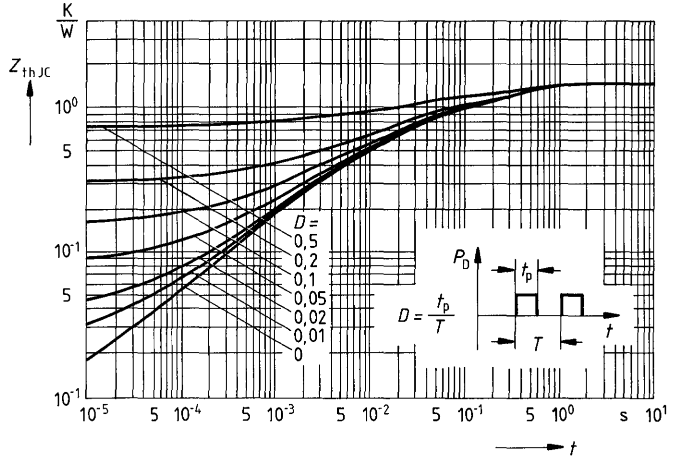
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



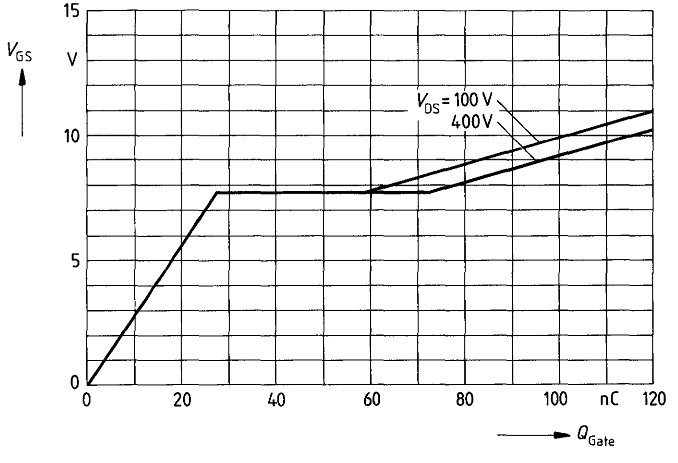
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



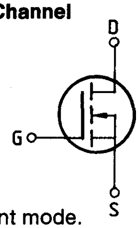
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14{,}4A$



Main ratings

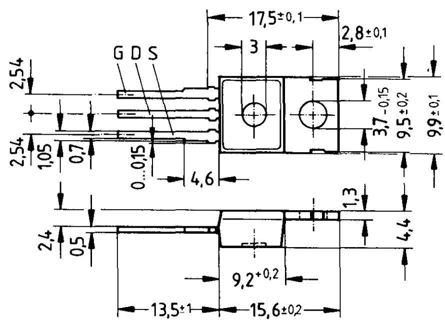
Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 5,0 A**
Drain-source on-resistance $R_{DS(on)}$ **= 1,5 Ω**

N-Channel



Description FREDFET with fast-recovery reverse diode, N-channel, enhancement mode.
Case Plastic package 14 A 3 in accordance with DIN 41 869,
or TO 220 AB in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 2 g

Type	Ordering code
BUZ 215	C67078-A1400-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,0	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	20	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	− 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

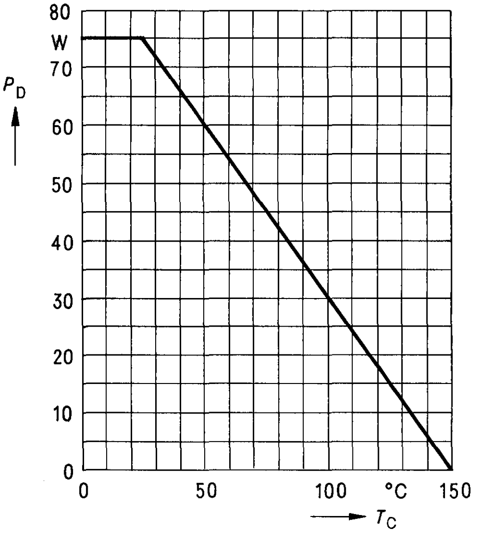
Chip – case	$R_{th\,JC}$	≤ 1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤ 75	K/W	

Electrical characteristics

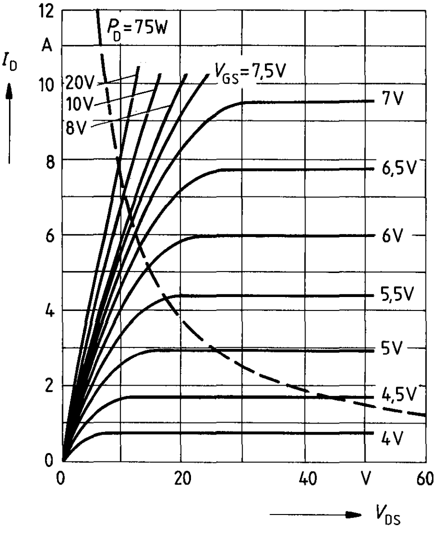
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,4	1,5	Ω	V_{GS} = 10V I_D = 3,2A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,7	–	S	V_{DS} = 25V I_D = 3,2A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	110	170	pF	
Reverse transfer capacitance	C_{rss}	–	40	70		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	20		
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; $I_F = I_{DR}$, di_F/dt = 100A/µs, V_R = 100V
		–	220	300		= 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C
		–	2,6	5,0		= 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		= 150 °C

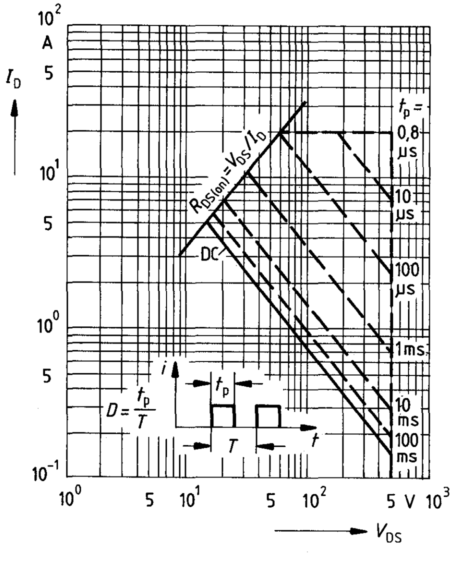
Power dissipation $P_D = f(T_C)$



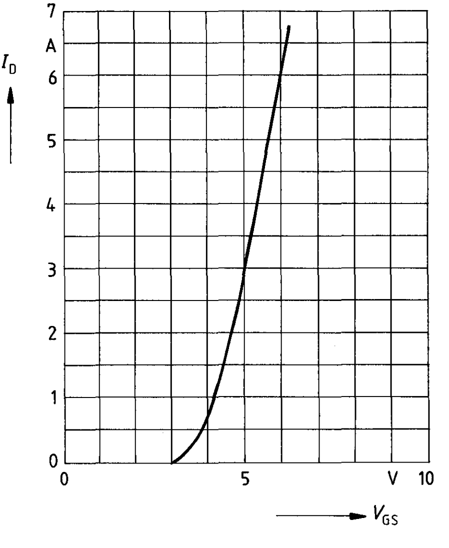
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



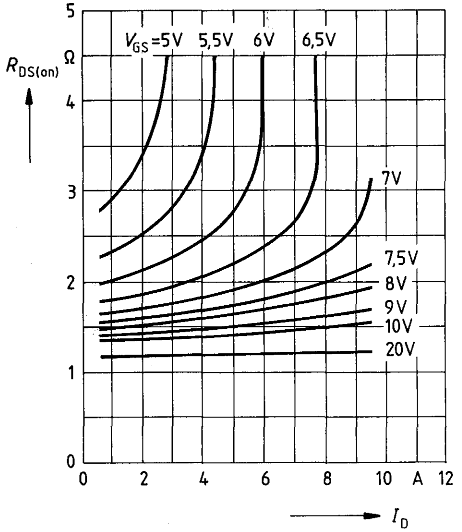
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



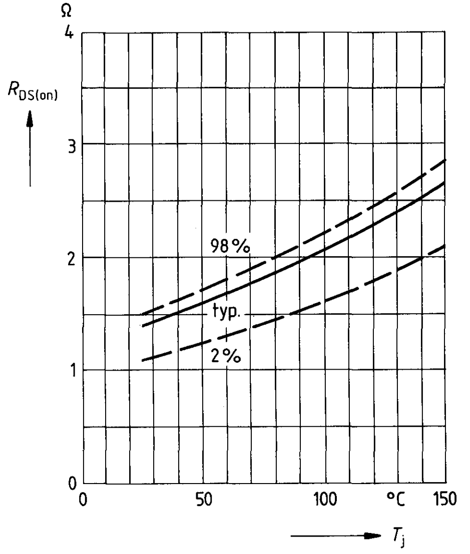
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



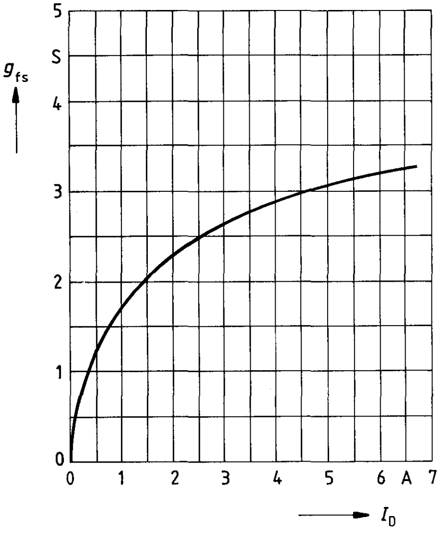
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



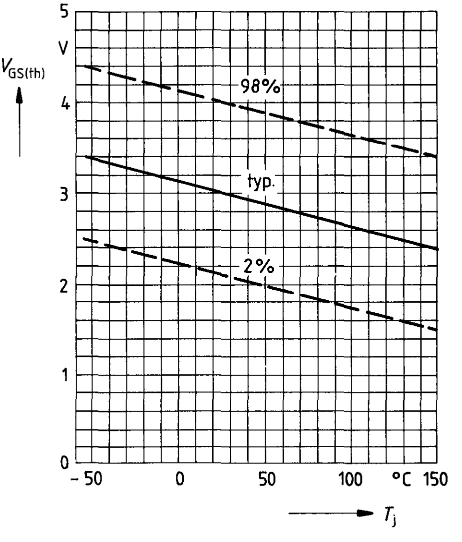
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 3{,}2A$, $V_{GS} = 10V$
(spread)



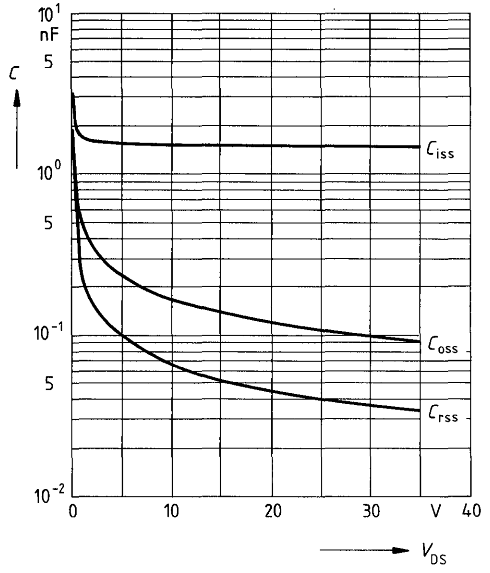
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



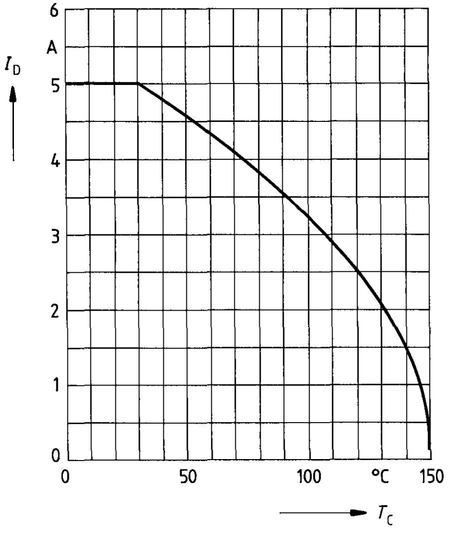
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



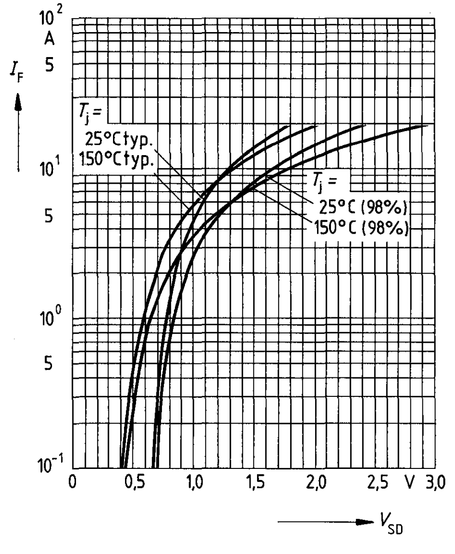
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



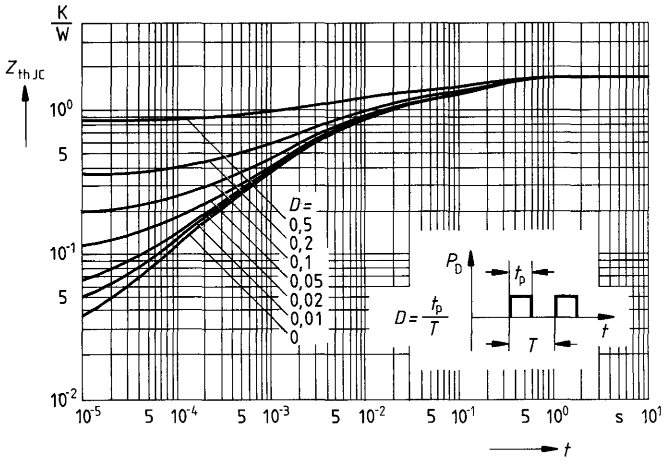
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



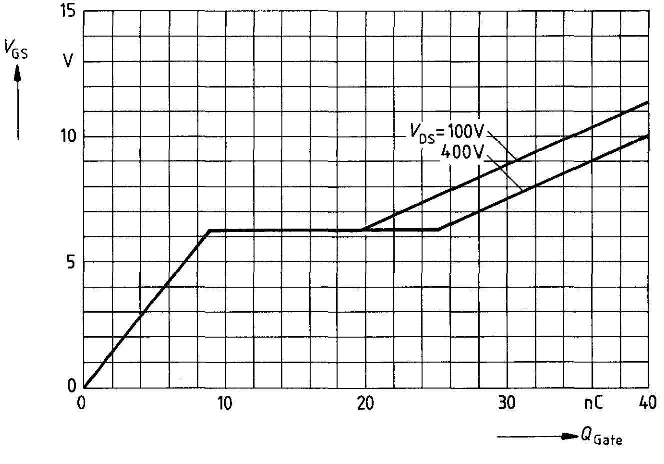
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



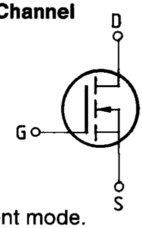
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 6{,}8A$



Main ratings

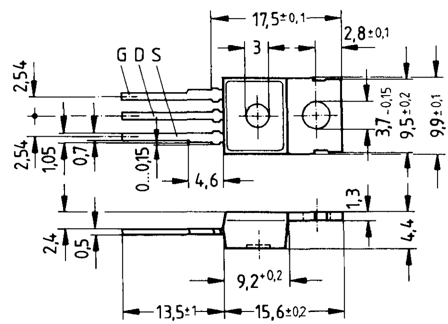
Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 4,4 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2 Ω**

N-Channel



Description FREDFET with fast-recovery reverse diode, N-channel, enhancement mode.
Case Plastic package 14 A 3 in accordance with DIN 41 869, or TO 220 AB in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 2 g

Type	Ordering code
BUZ 216	C67078-A1402-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,4	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	17	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

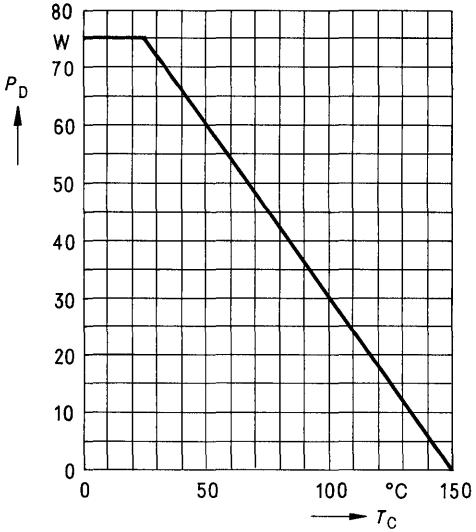
Chip – case	$R_{th JC}$	≤1,67	K/W	
Chip – ambient	$R_{th JA}$	≤75	K/W	

Electrical characteristics

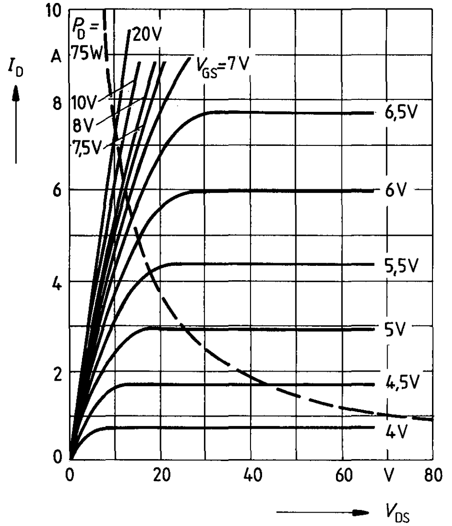
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,7	2,0	Ω	V_{GS} = 10V I_D = 3,2A
Dynamic ratings						
Forward transconductance	g_{fs}	1,5	2,7	–	S	V_{DS} = 25V I_D = 3,2A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	110	170	pF	
Reverse transfer capacitance	C_{rss}	–	40	70		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	50	65		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,4	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	17		
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; $I_F = I_{DR}$, di_F/dt = 100A/µs, V_R = 100V
		–	–	–		= 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C
		–	–	–		= 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		= 150 °C

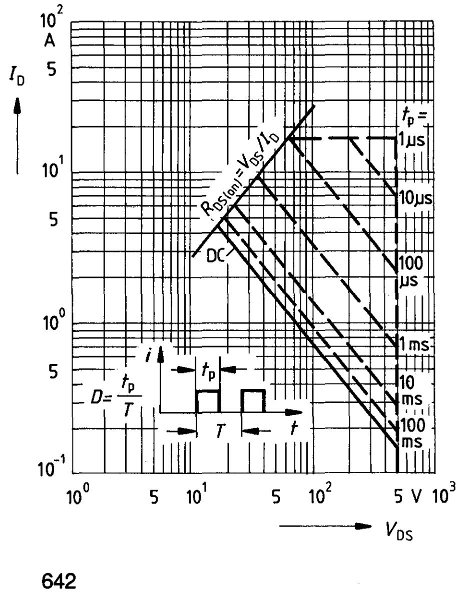
Power dissipation $P_D = f(T_C)$



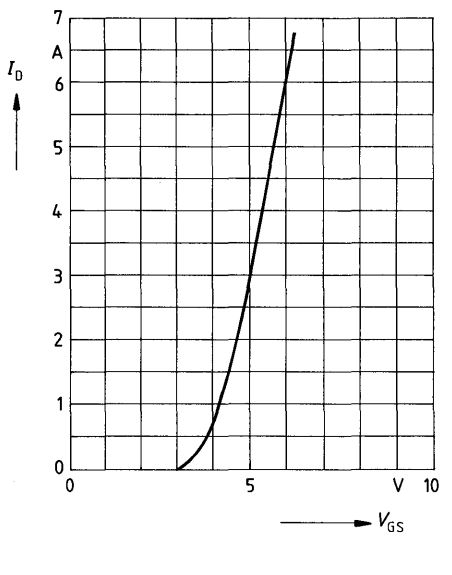
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



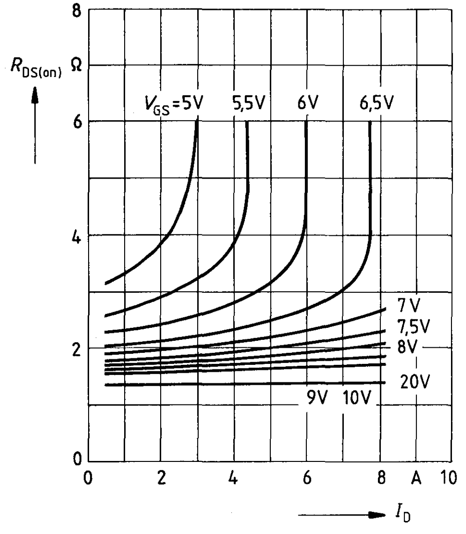
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



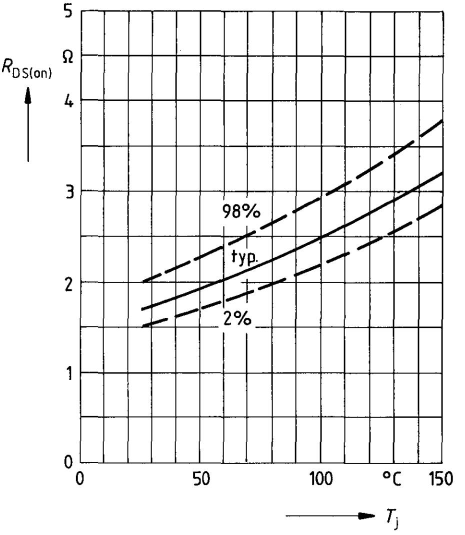
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



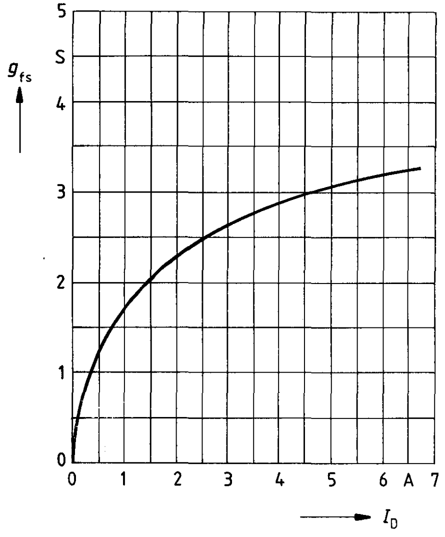
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



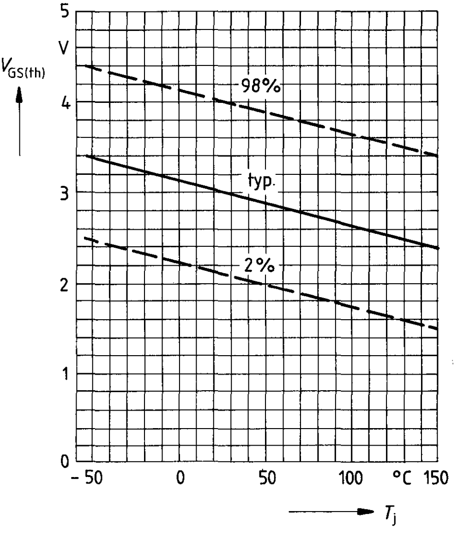
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 3{,}2A$, $V_{GS} = 10V$
(spread)



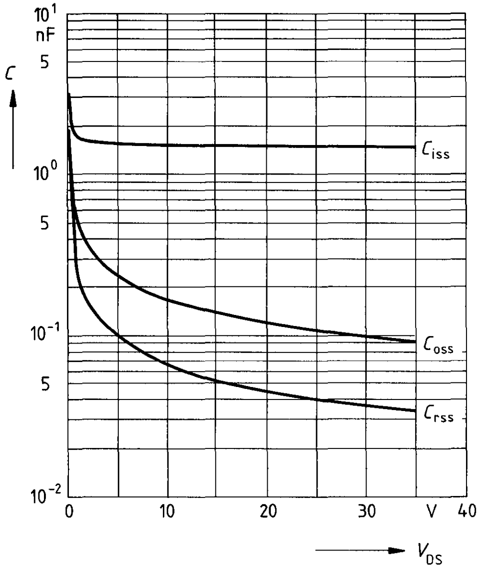
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



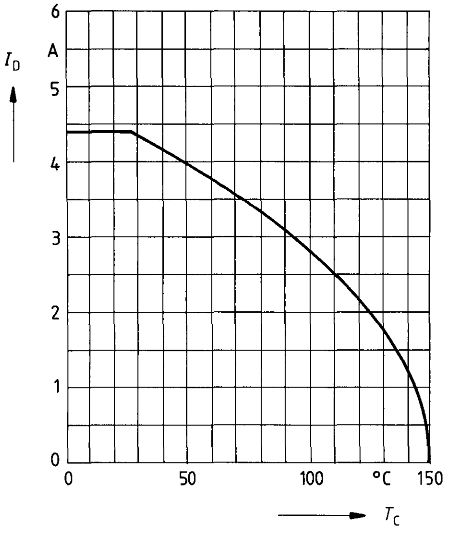
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



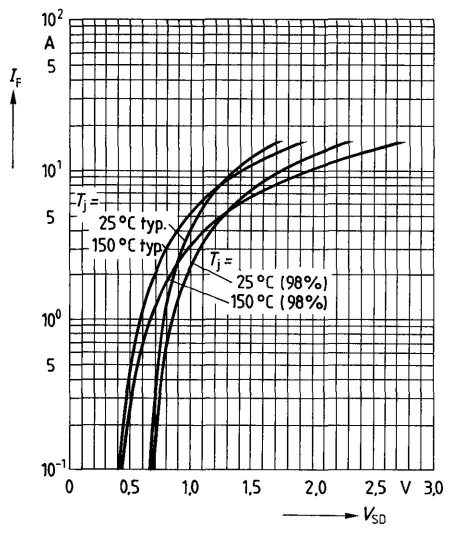
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



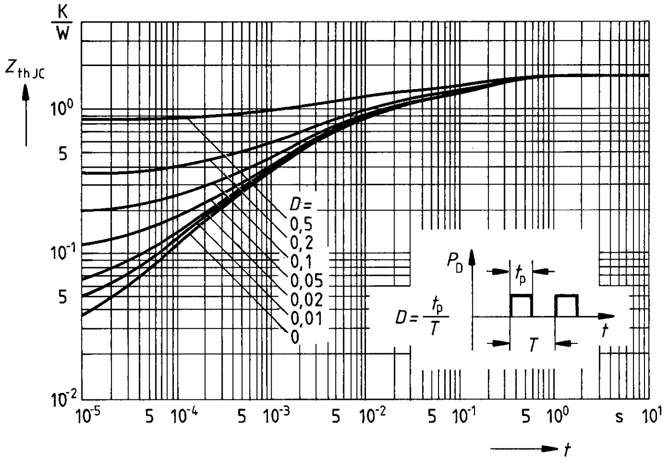
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



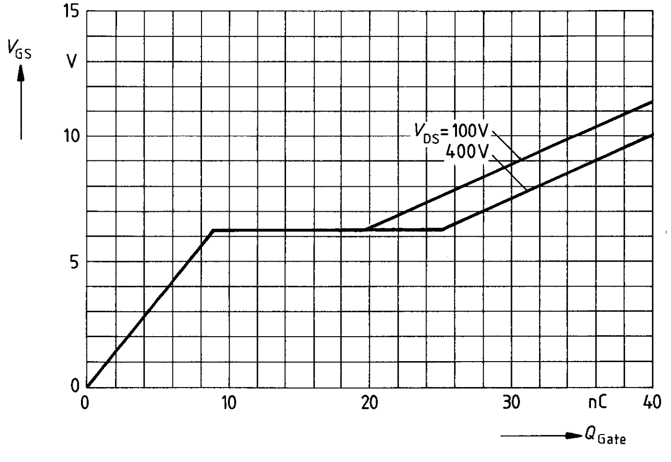
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

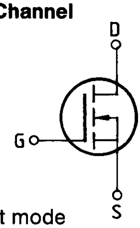


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 6{,}8A$



Main ratings

N-Channel



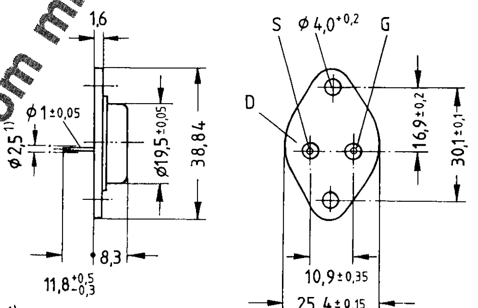
Drain-source voltage	V_{DS}	**= 800 V**
Continuous drain current	I_D	**= 6,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 1,5 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Metal case 3 A 2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
BUZ 220	C67078-A1103-A2

Available from mid 1987



1) max: bending area

Dimensions in mm

Maximum ratings

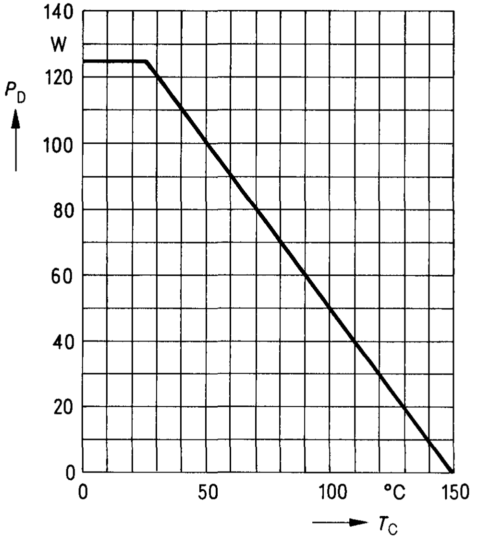
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	6,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	26	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

Electrical characteristics

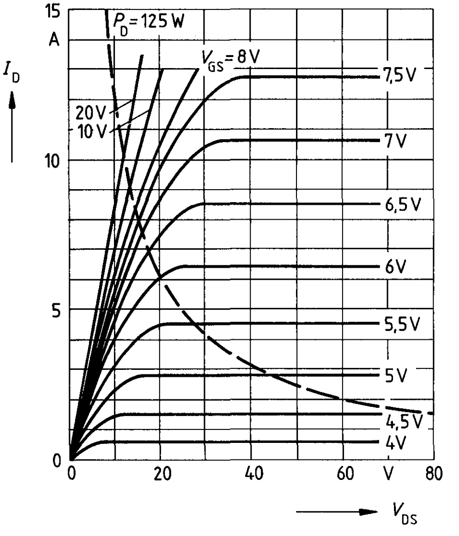
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,4	1,5	Ω	V_{GS} = 10V I_D = 4,2A	
Dynamic ratings							
Forward transconductance	g_{fs}	1,8	3,4	–	S	V_{DS} = 25V I_D = 4,2A	
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	200	350	pF		
Reverse transfer capacitance	C_{rss}	–	80	140			
Turn-on time t_{on} (t_{on} = $t_{d\,(on)}$ + t_r)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	90	140			
Turn-off time t_{off} (t_{off} = $t_{d\,(off)}$ + t_f)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	6,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	26			
Diode forward on-voltage	V_{SD}	–	1,15	1,6	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	I_F = I_{DR} di_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

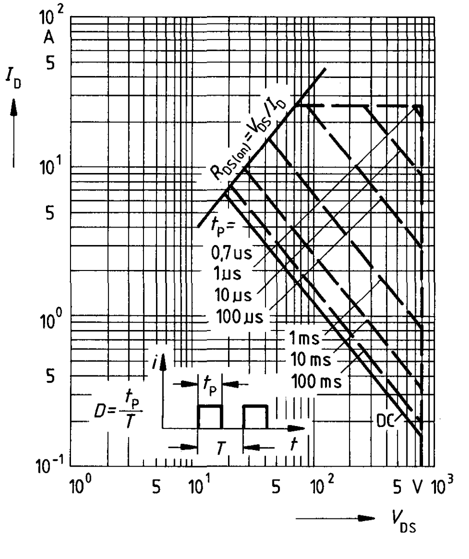
Power dissipation $P_D = f(T_C)$



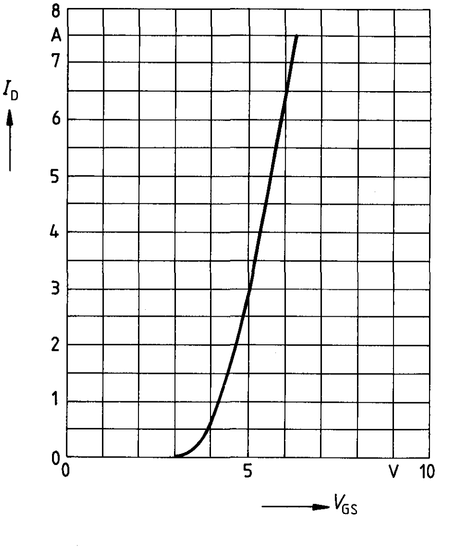
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



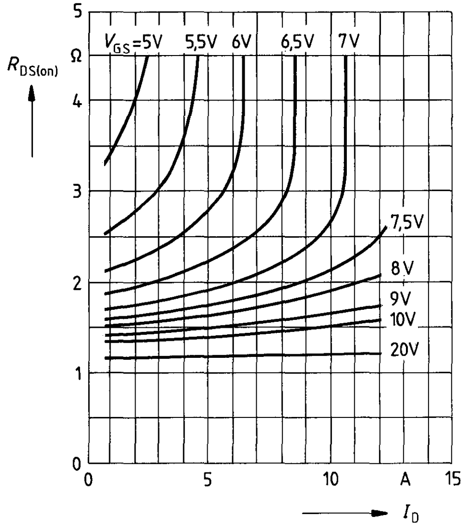
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



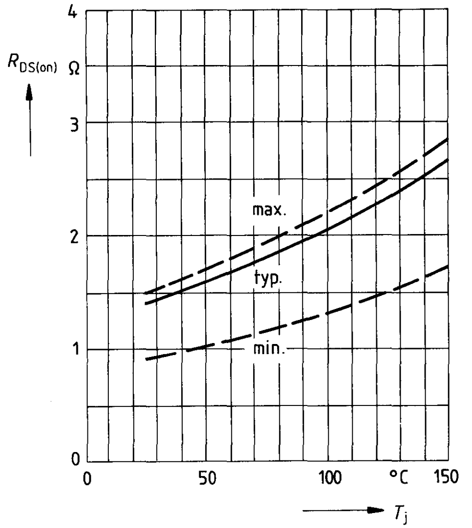
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\,V$, $T_j = 25\,°C$



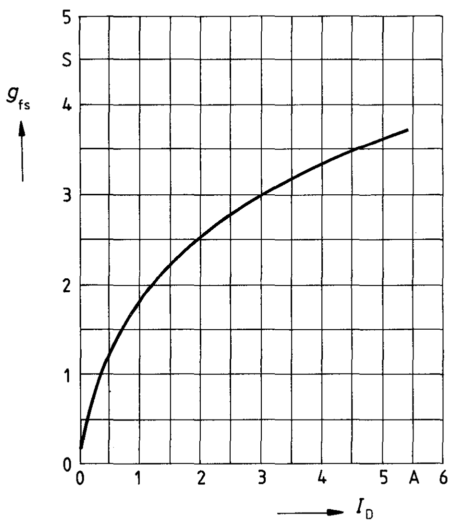
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



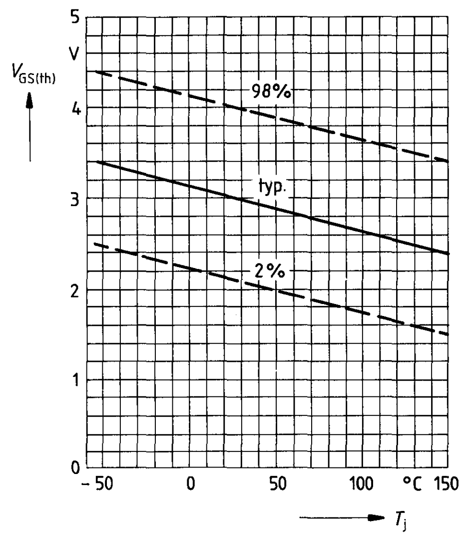
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 4,2A, V_{GS} = 10V
(spread)



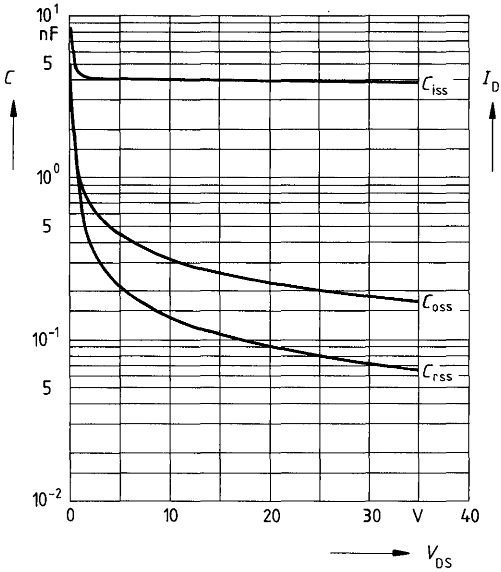
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



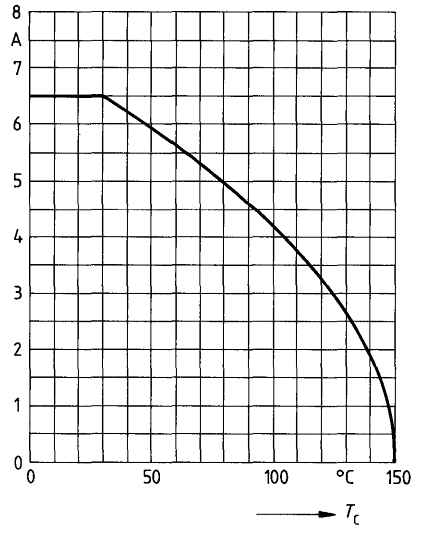
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



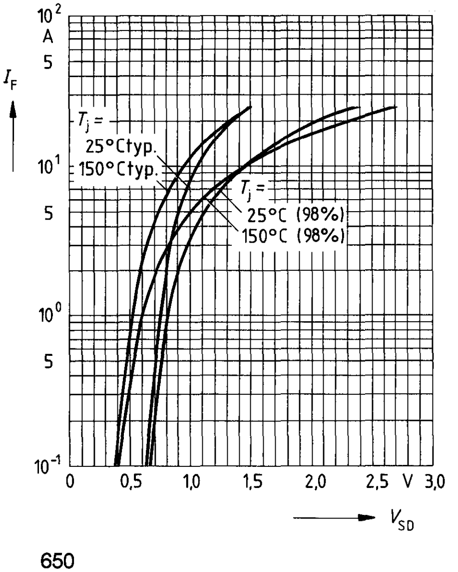
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



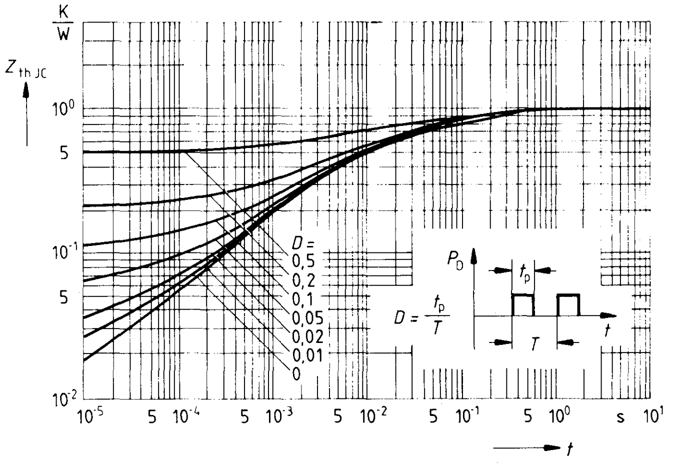
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



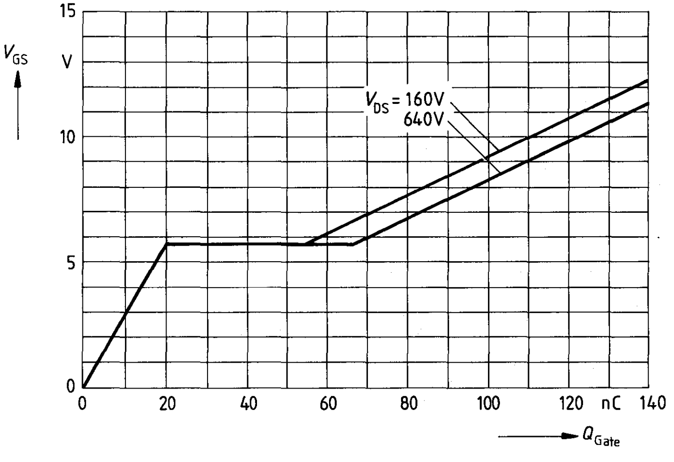
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



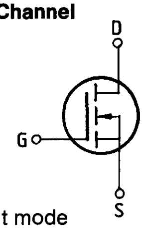
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 9A$



Main ratings

Drain-source voltage V_{DS} **= 800 V**
Continuous drain current I_D **= 5,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2 Ω**

N-Channel



Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

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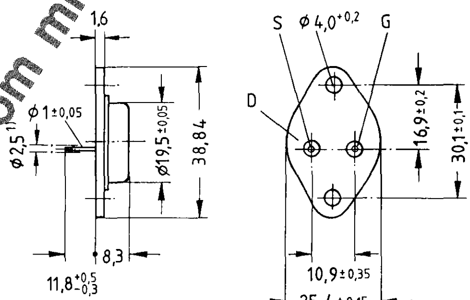
or TO 204 AA (TO 3) in accordance with JEDEC.
Approx. weight 12 g

Available from mid 1987

Type	Ordering code
BUZ 221	C67078-A1104-A2



1) max. bending area

Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,5	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	22	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	− 55 ... + 150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

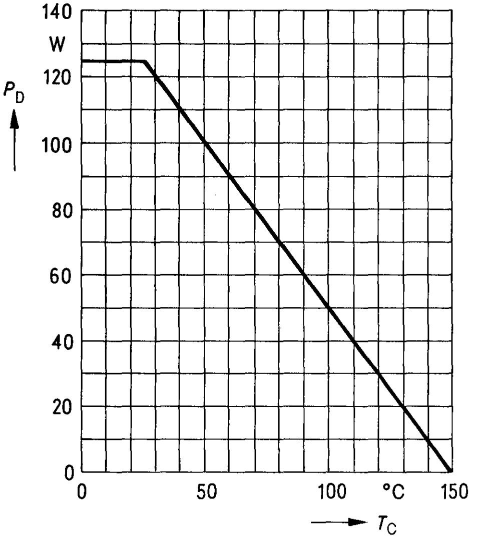
Chip – case	$R_{th\ JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤ 35	K/W	

Electrical characteristics

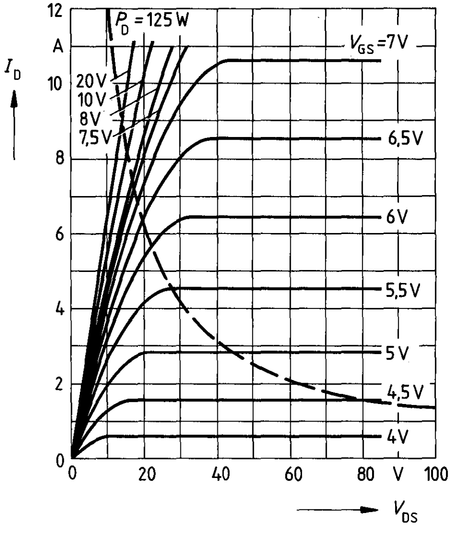
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,8	2,0	Ω	V_{GS} = 10V I_D = 4,2A
Dynamic ratings						
Forward transconductance	g_{fs}	1,8	3,4	–	S	V_{DS} = 25V I_D = 4,2A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	200	350	pF	
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	22		
Diode forward on-voltage	V_{SD}	–	1,1	1,55	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; $I_F = I_{DR}$, di_F/dt = 100A/µs, V_R = 100V
		–	220	300		= 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C
		–	2,6	5,0		= 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		= 150 °C

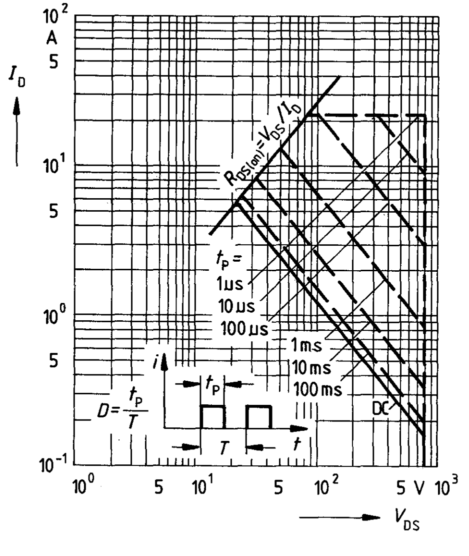
Power dissipation $P_D = f(T_C)$



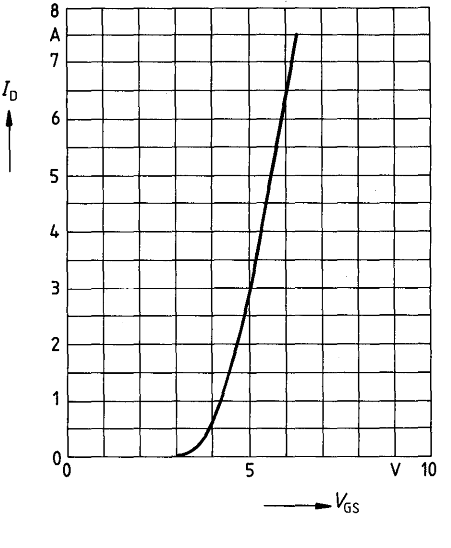
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



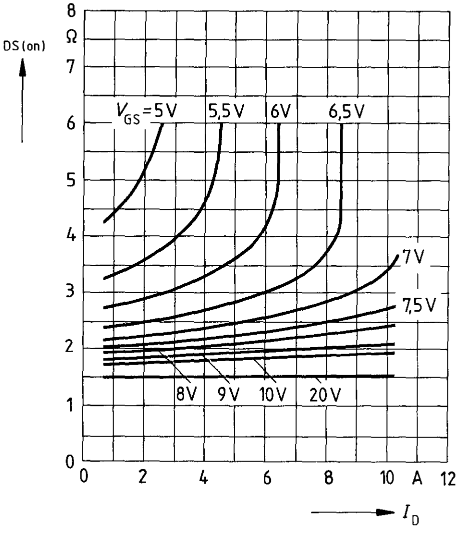
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



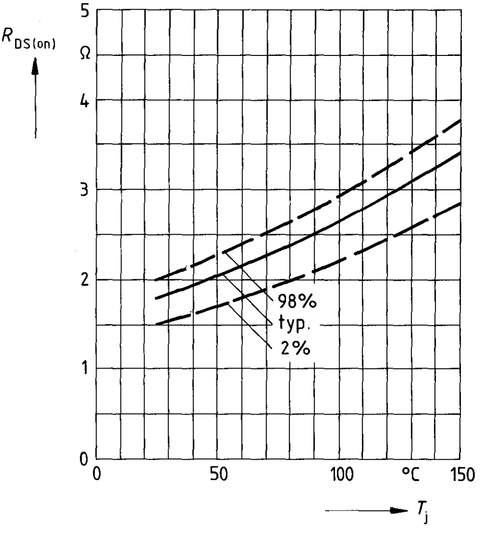
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



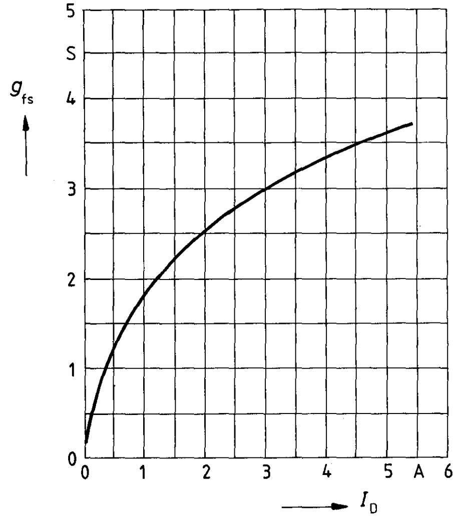
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



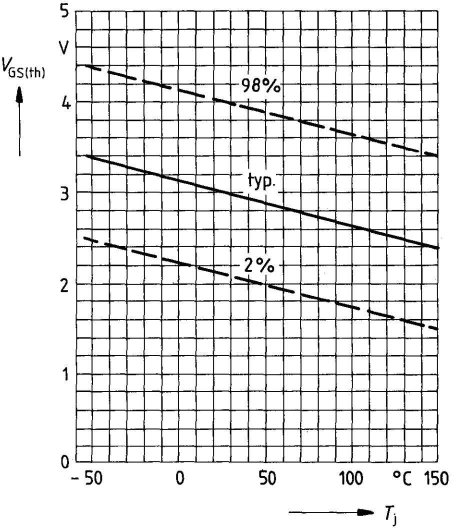
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 4{,}2A$, $V_{GS} = 10V$
(spread)



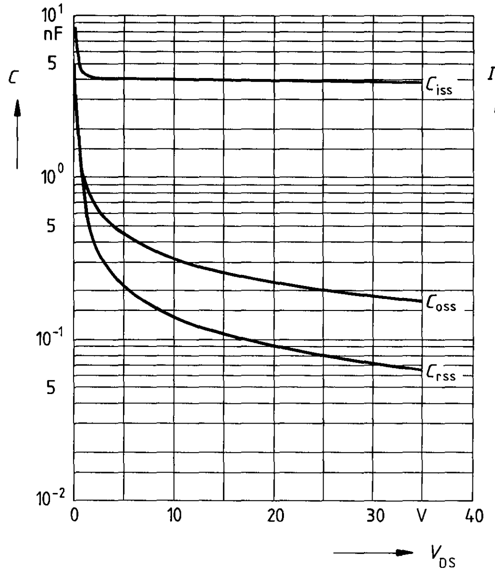
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



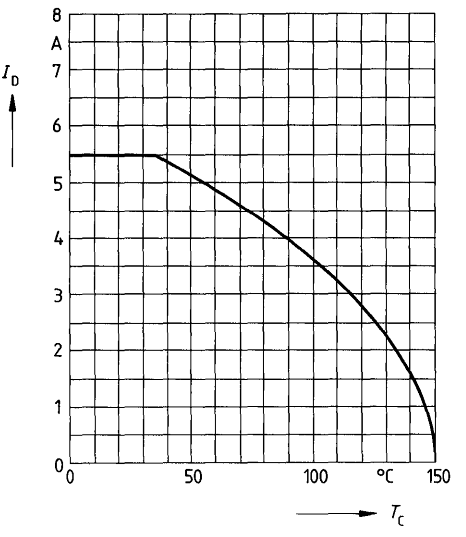
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



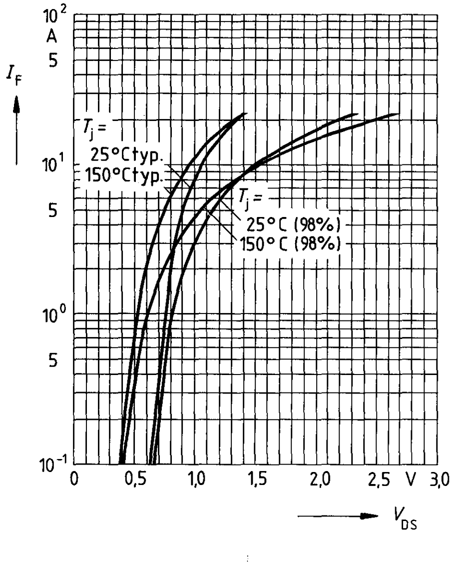
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



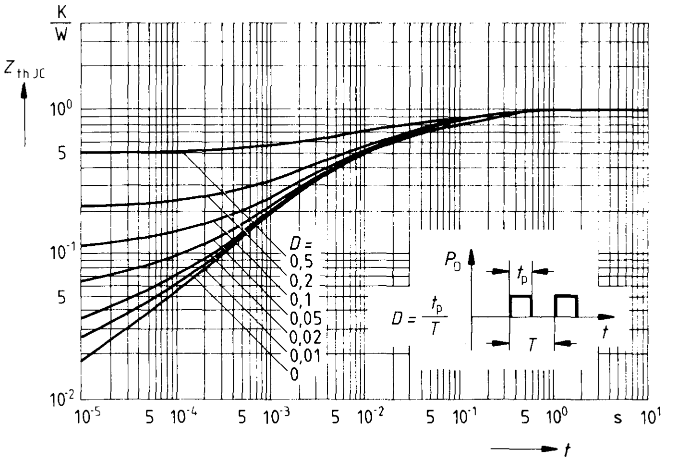
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



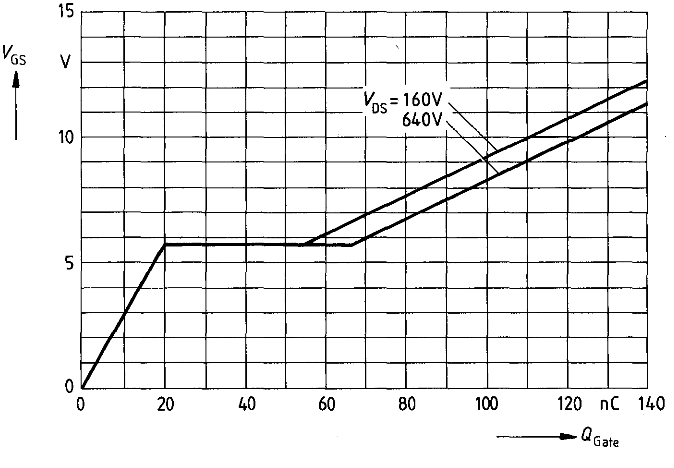
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

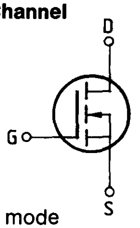


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 9A$



Main ratings

N-Channel



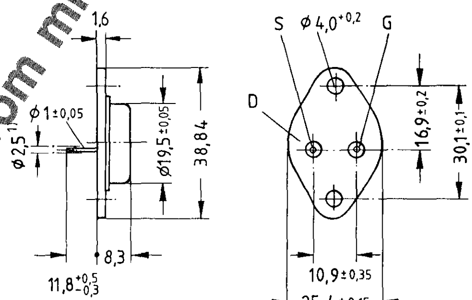
Drain-source voltage	V_{DS}	**= 1000 V**
Continuous drain current	I_D	**= 5,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 2 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Metal case 3 A 2 in accordance with DIN 41 872,
or TO 204 AA (TO 3) in accordance with JEDEC.
Approx. weight 12 g

Type	Ordering code
BUZ 230	C67078-A1105-A2

Available from mid 1987



1) max. bending area

Dimensions in mm

Maximum ratings

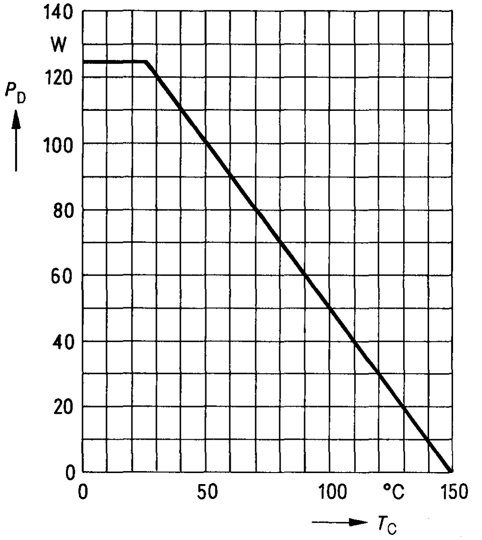
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	22	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		C	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤1,0	K/W	
Chip – ambient	$R_{th JA}$	≤35	K/W	

Electrical characteristics

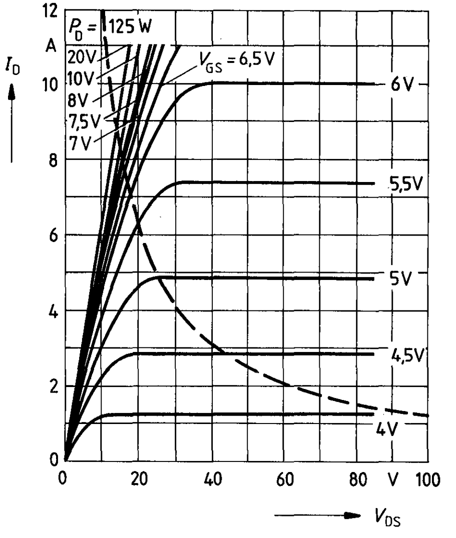
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,7	2,0	Ω	V_{GS} = 10V I_D = 3,5A	
Dynamic ratings							
Forward transconductance	g_{fs}	1,4	4,0	–	S	V_{DS} = 25V I_D = 3,5A	
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	180	300	pF		
Reverse transfer capacitance	C_{rss}	–	70	120			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	90	140			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	5,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	22			
Diode forward on-voltage	V_{SD}	–	1,25	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	I_F = I_{DR} di_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

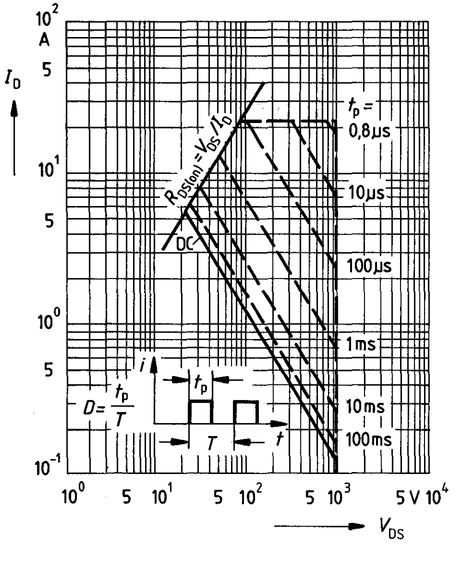
Power dissipation $P_D = f(T_C)$



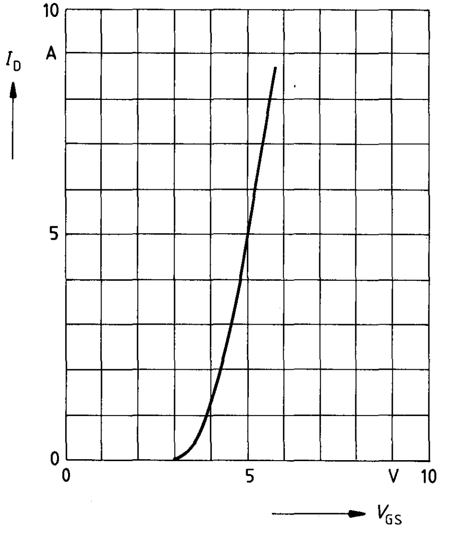
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



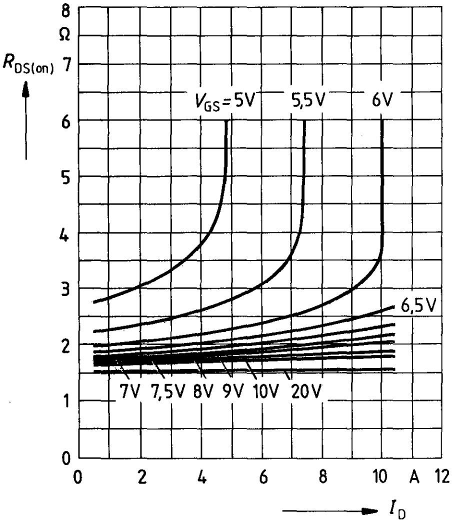
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



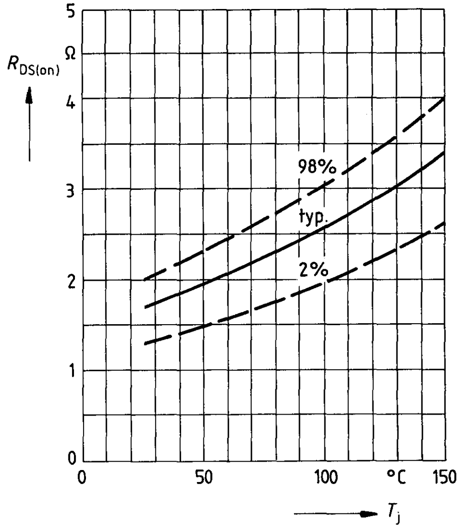
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



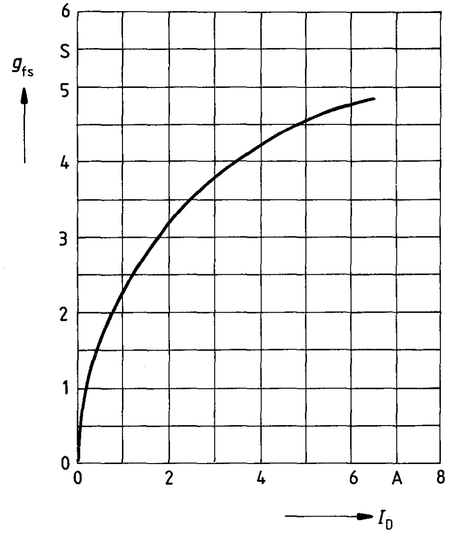
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



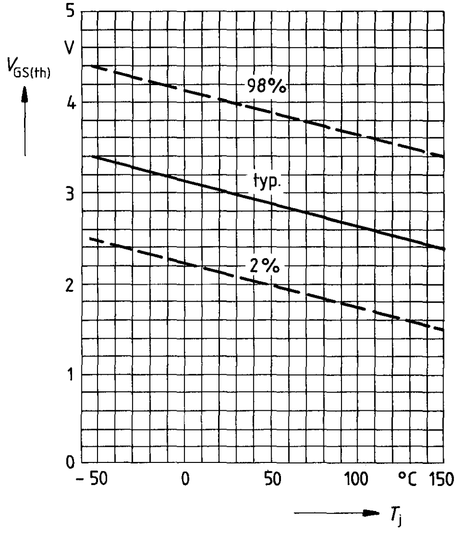
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 3{,}5A$, $V_{GS} = 10V$
(spread)



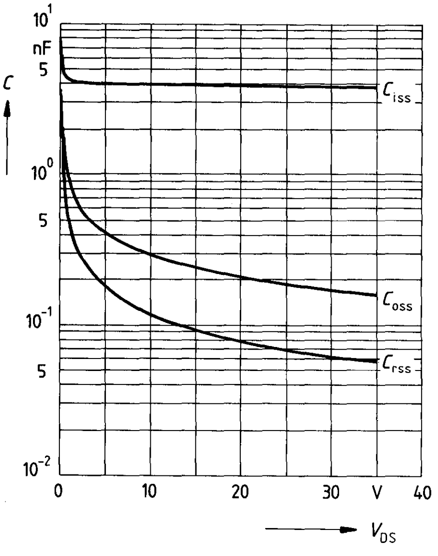
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



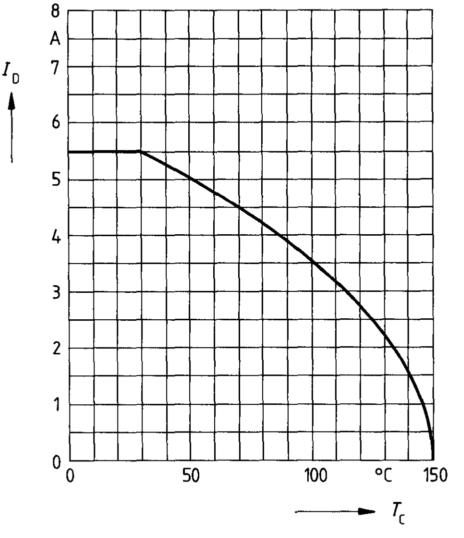
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



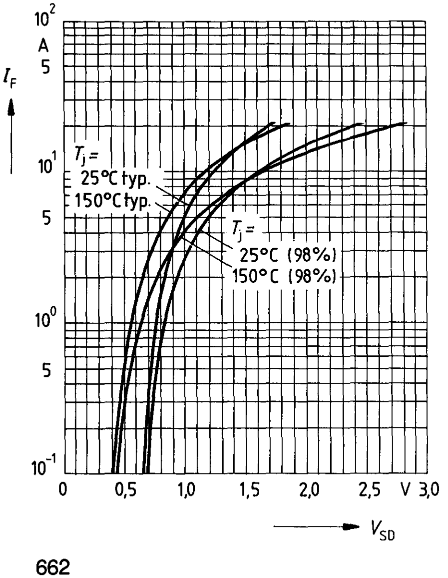
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



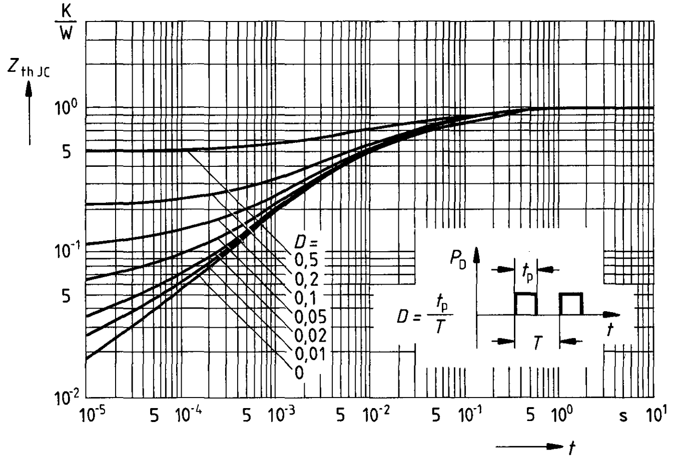
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



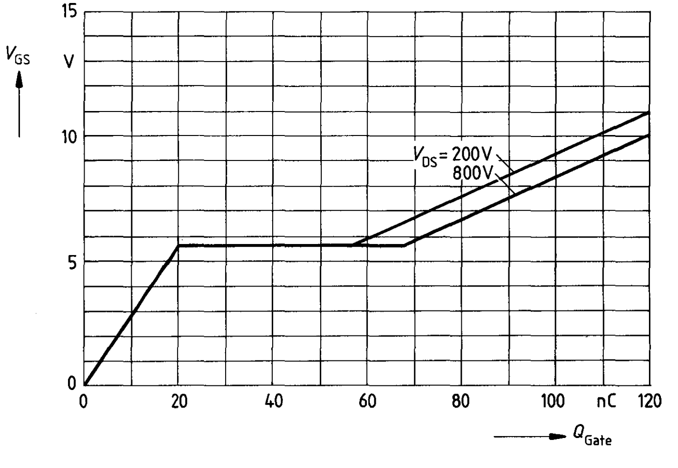
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

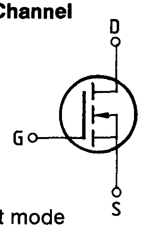


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 8A$



Main ratings

N-Channel



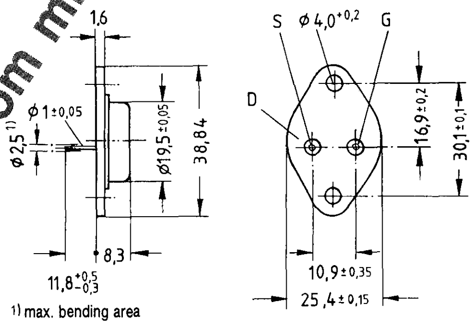
Drain-source voltage	V_{DS}	**= 1000 V**
Continuous drain current	I_D	**= 4,9 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 2,6 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Metal case 3A2 in accordance with DIN 41 872, or TO 204 AA (TO 3) in accordance with JEDEC. Approx. weight 12 g

Type	Ordering code
BUZ 231	C67078-A1106-A2

Available from mid 1987



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,9	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	19	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55… +150	°C	
DIN humidity category		C	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

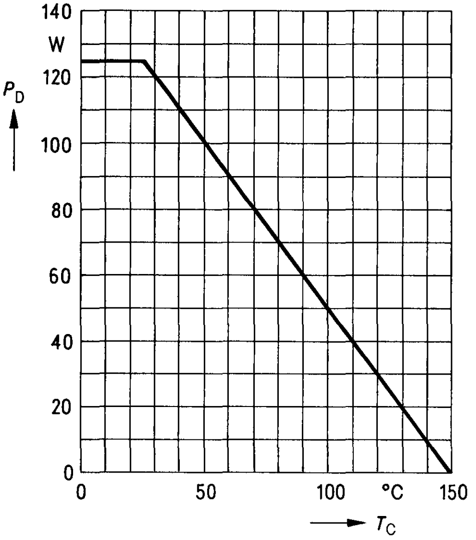
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤35	K/W	

Electrical characteristics

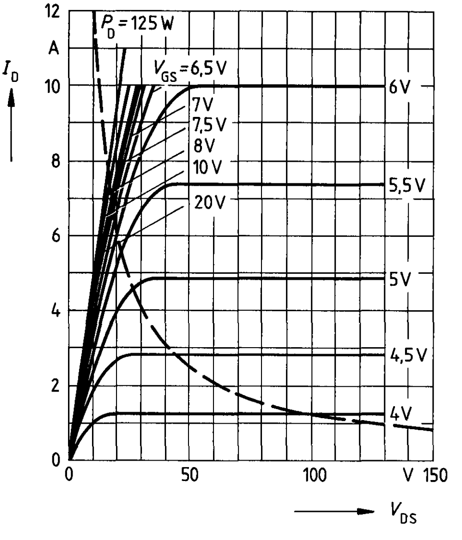
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	2,3	2,6	Ω	V_{GS} = 10V I_D = 3,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,4	4,0	–	S	V_{DS} = 25V I_D = 3,5A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	300	pF	
Reverse transfer capacitance	C_{rss}	–	70	120		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,4A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	110	140		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,9	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	19		
Diode forward on-voltage	V_{SD}	–	1,25	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; $I_F = I_{DR}$, di_F/dt = 100A/µs, V_R = 100V
		–	220	300		= 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C
		–	2,6	5,0		= 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		= 150 °C

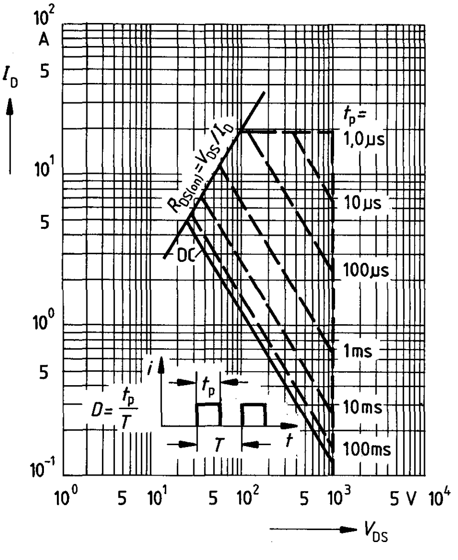
Power dissipation $P_D = f(T_C)$



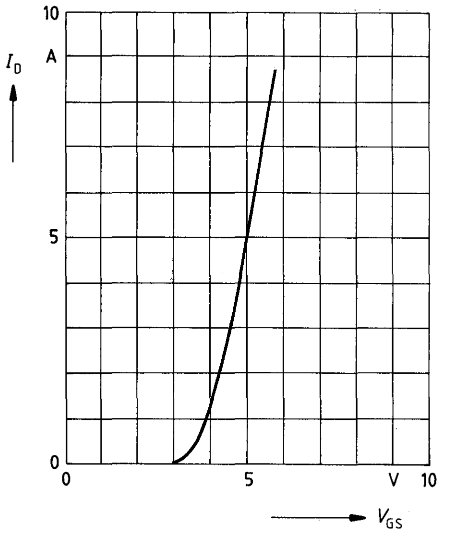
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



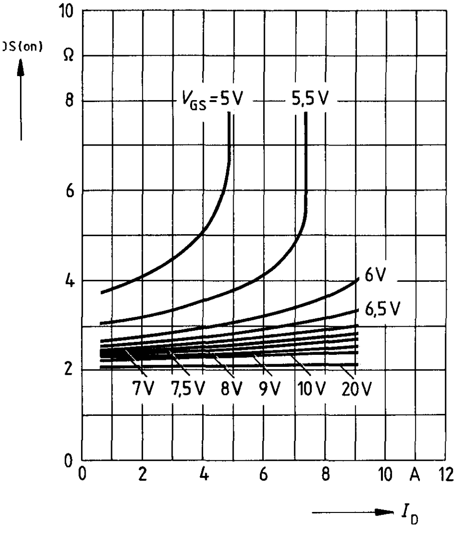
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



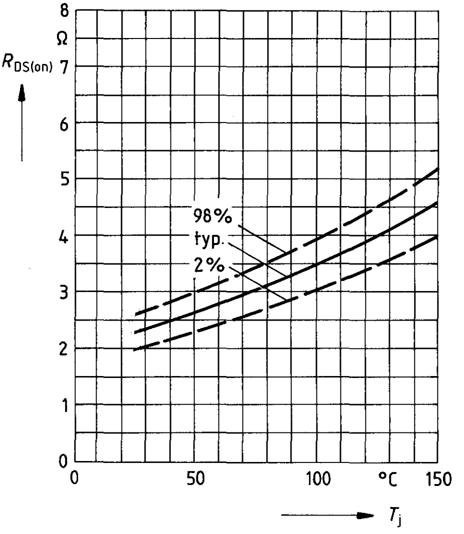
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



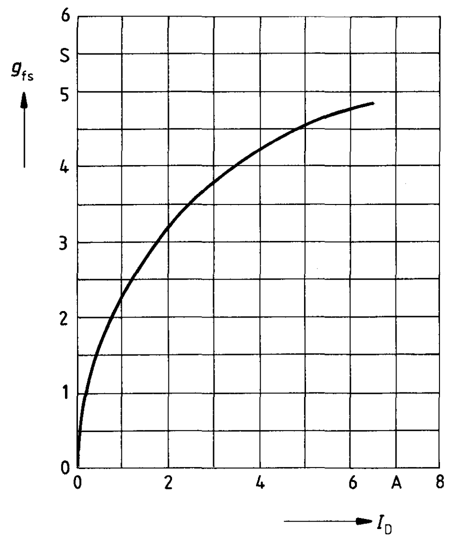
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



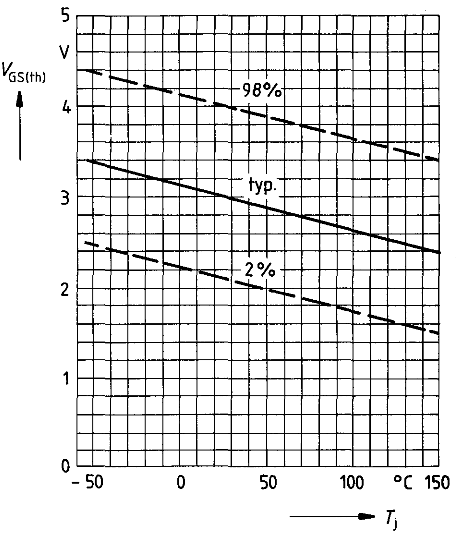
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 3,5A, V_{GS} = 10V
(spread)



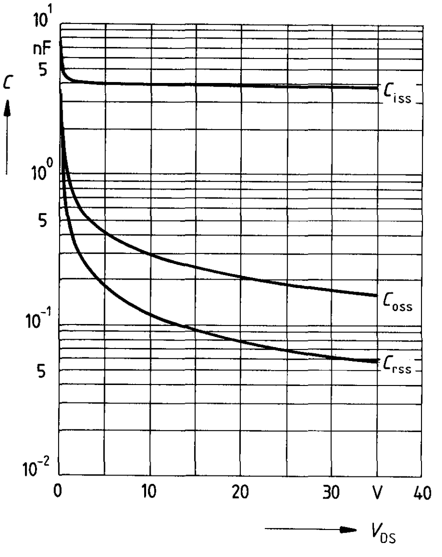
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



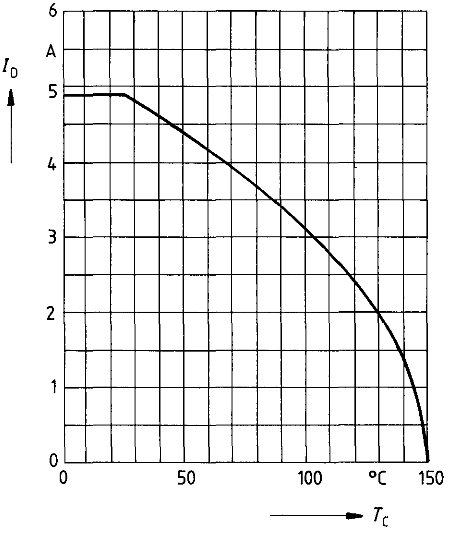
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



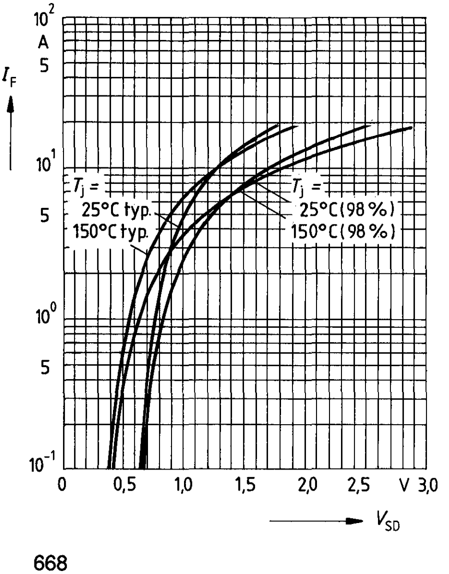
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



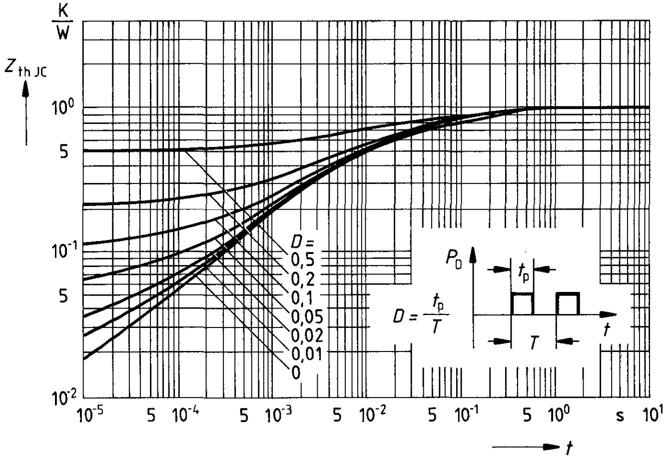
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



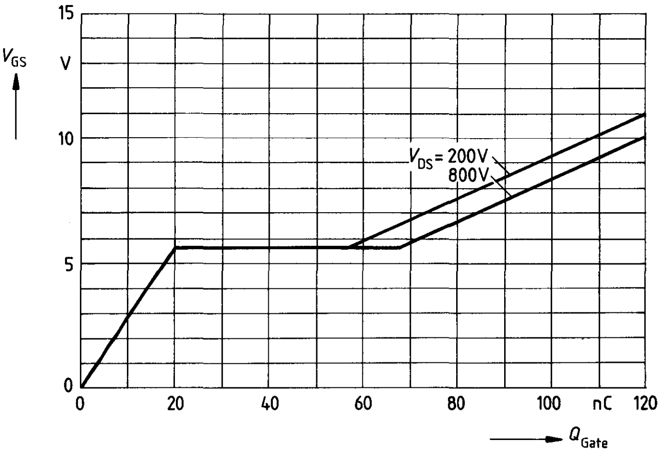
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

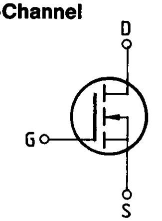


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 8A$



Main ratings

N-Channel

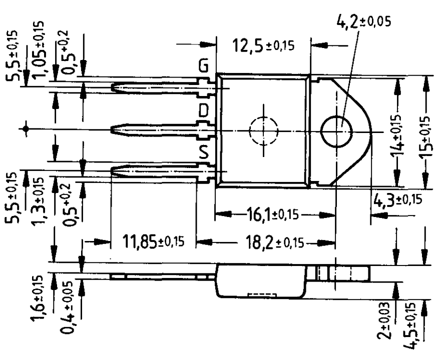


Drain-source voltage	V_{DS}	**= 800 V**
Continuous drain current	I_D	**= 3 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 3 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41869 or TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 307	C67078-A3100-A2



Dimensions in mm

Maximum ratings

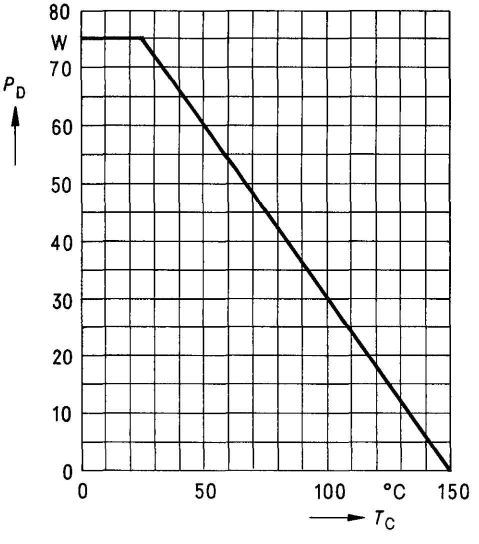
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	3,0	A	T_C = 50 °C
Pulsed drain current	I_{Dpuls}	12	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

 S Preferred Type

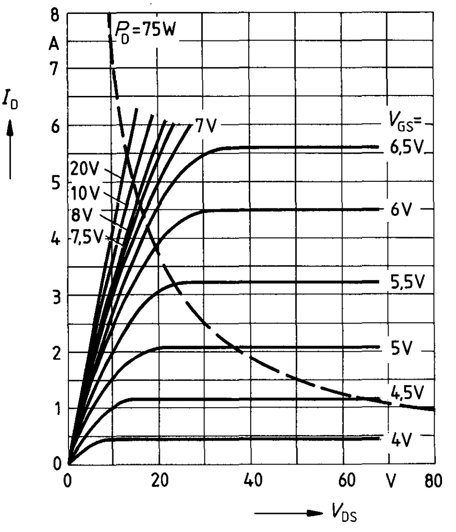
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	2,7	3,0	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	1,8	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	90	150	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	3,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	12		
Diode forward on-voltage	V_{SD}	–	1,05	1,30	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

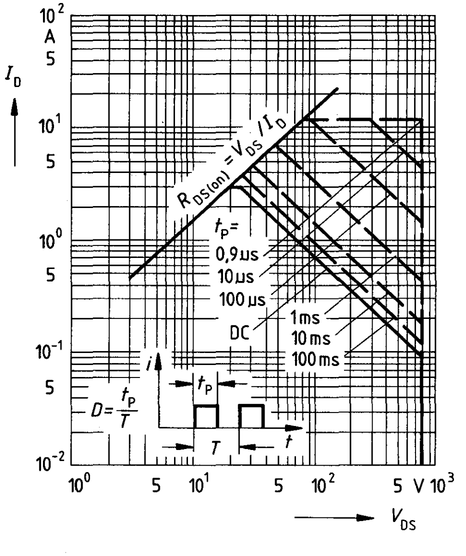
Power dissipation $P_D = f(T_C)$



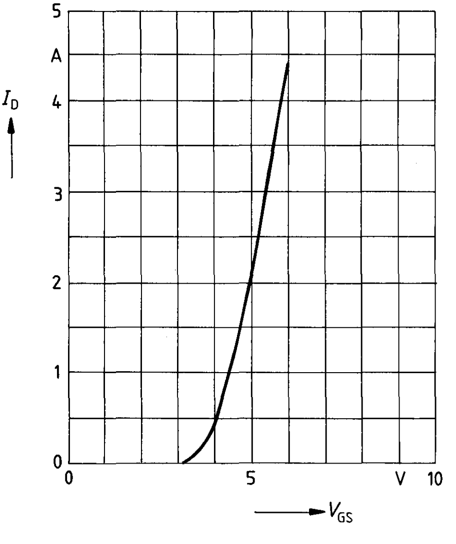
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



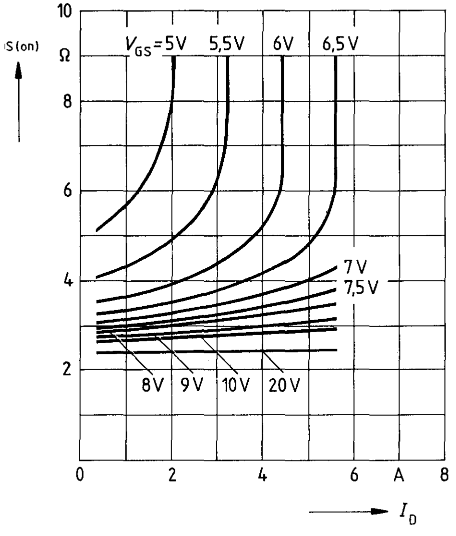
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



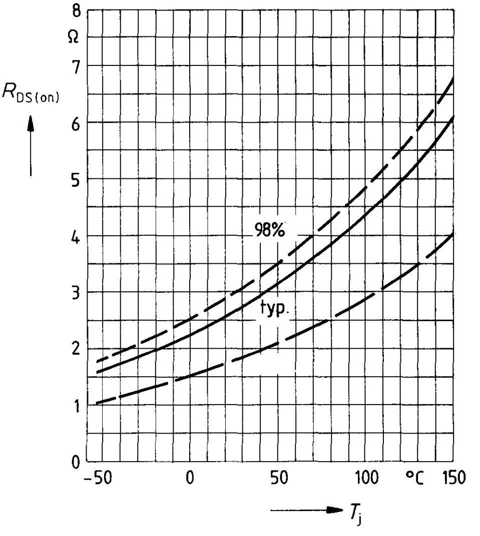
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



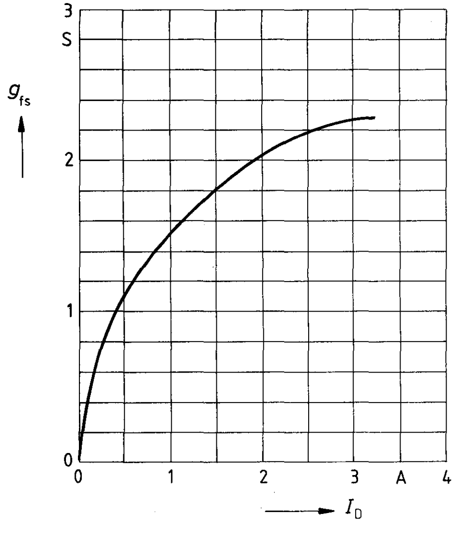
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



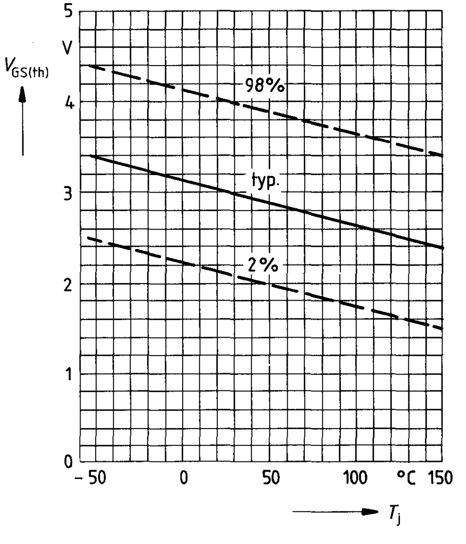
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 1{,}5A$, $V_{GS} = 10V$
(spread)



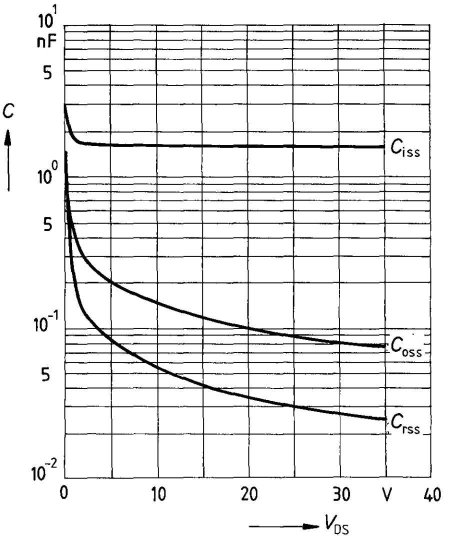
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



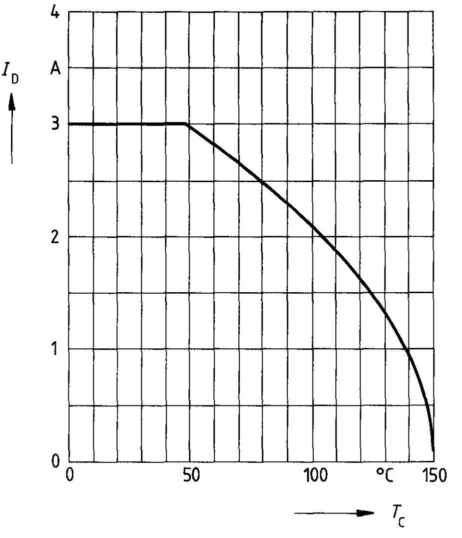
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



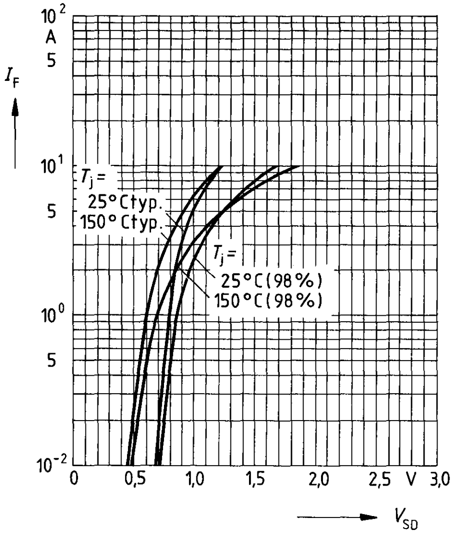
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



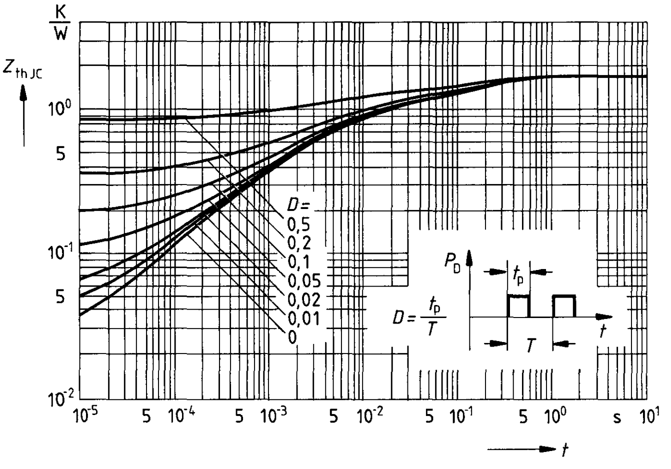
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



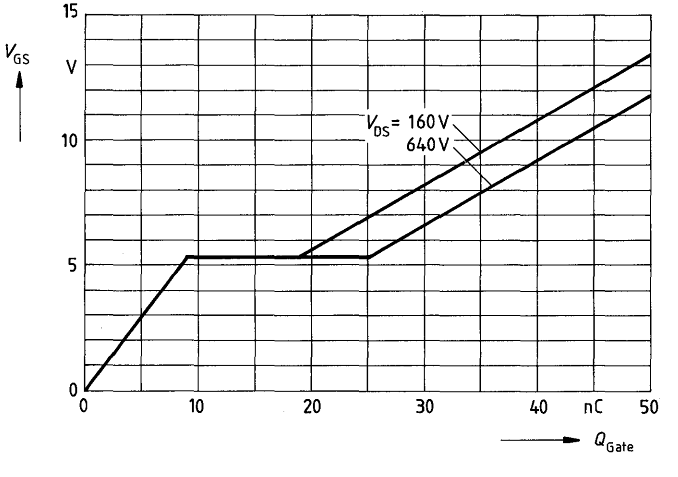
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



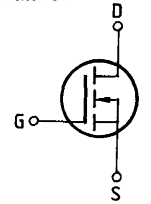
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 5A$



Main ratings

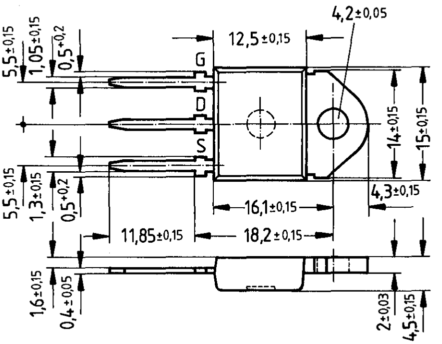
Drain-source voltage V_{DS} **= 800 V**
Continuous drain current I_D **= 2,6 A**
Drain-source on-resistance $R_{DS(on)}$ **= 4,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
Ⓢ BUZ 308	C67078-A3109-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,6	A	T_C = 50 °C
Pulsed drain current	I_{Dpuls}	10	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\ JA}$	≤45	K/W	

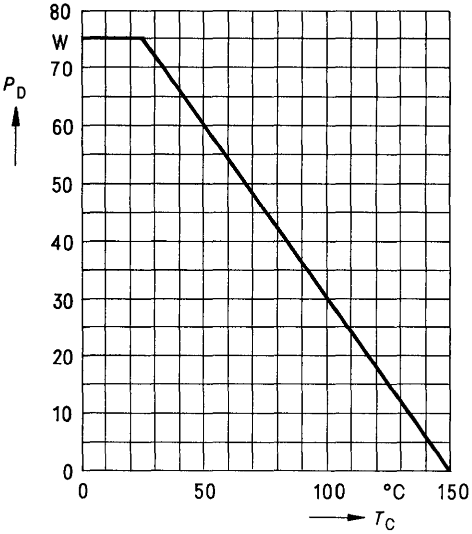
Ⓢ Preferred Type

Electrical characteristics

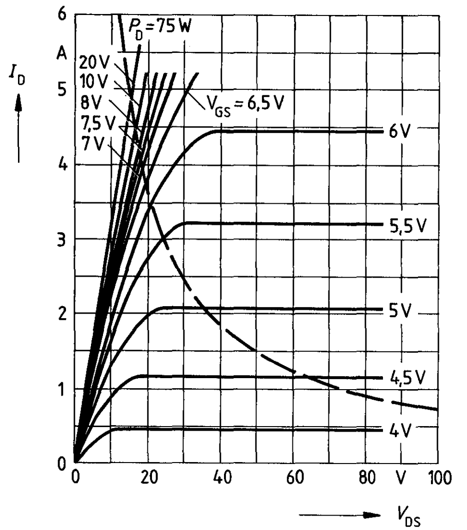
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	3,5	4,0	Ω	V_{GS} = 10V I_D = 1,5A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	1,8	–	S	V_{DS} = 25V I_D = 1,5A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	90	150	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,1A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,6	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	10		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1800	–	ns	T_j = 25 °C
Reverse recovery charge	Q_{rr}	–	12	–	µC	I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V

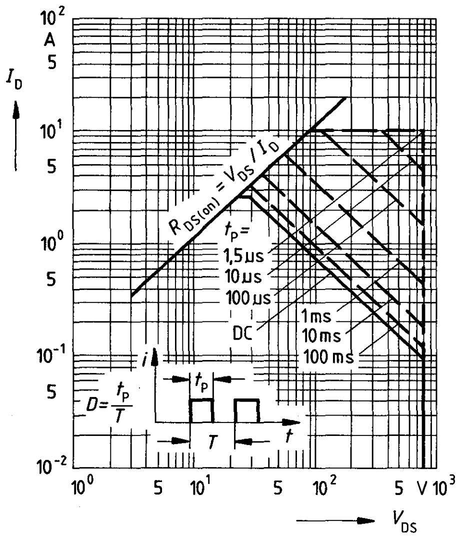
Power dissipation $P_D = f(T_C)$



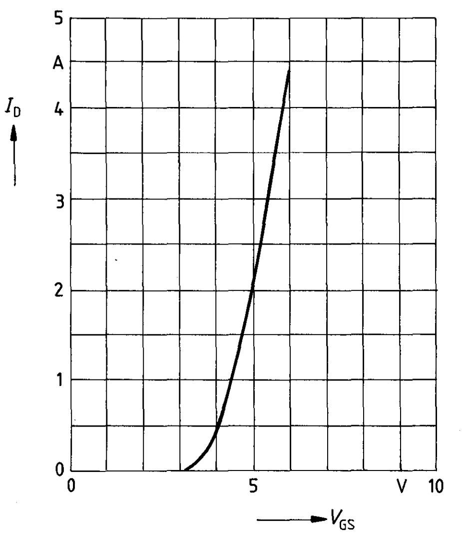
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



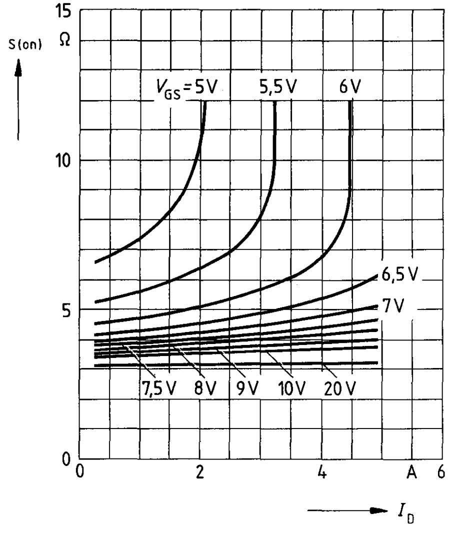
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



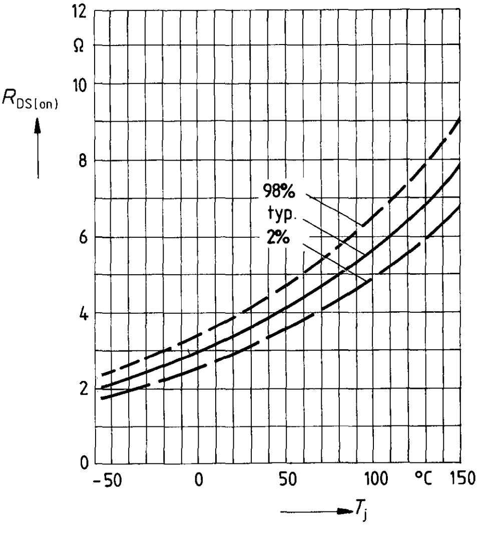
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\,V$, $T_j = 25\,°C$



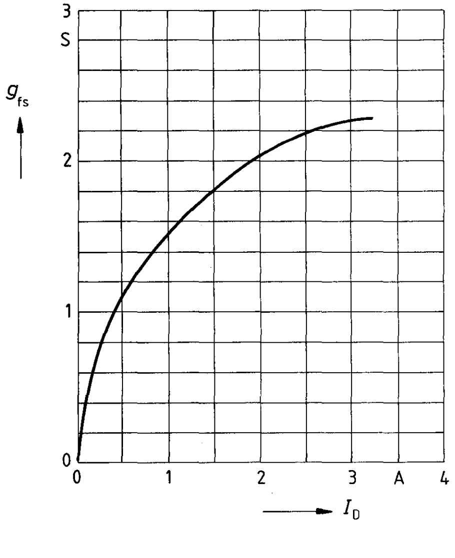
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



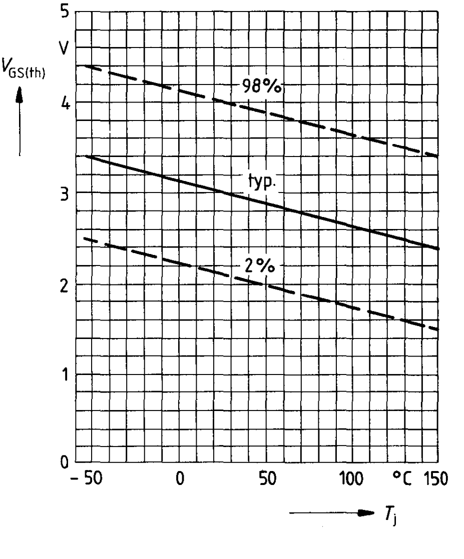
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 1{,}5A$, $V_{GS} = 10V$
(spread)



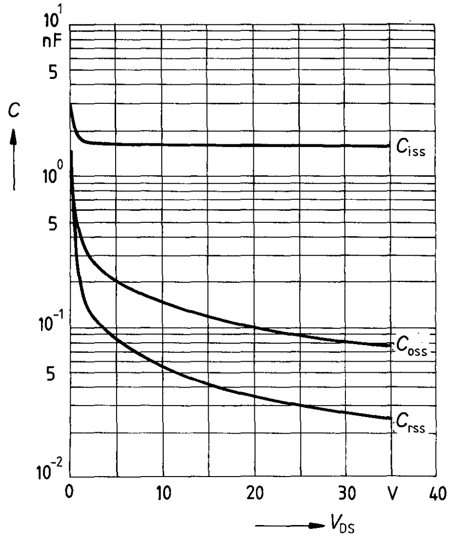
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



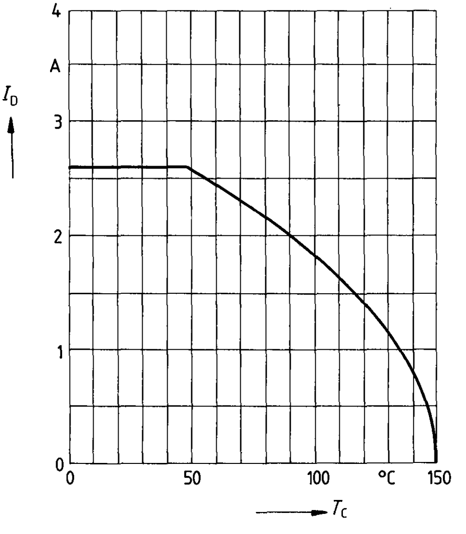
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



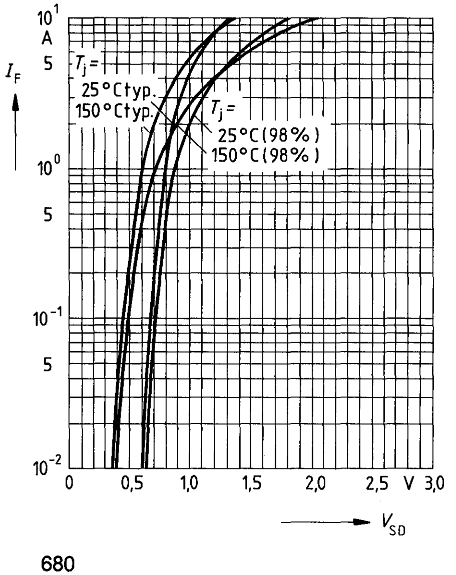
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



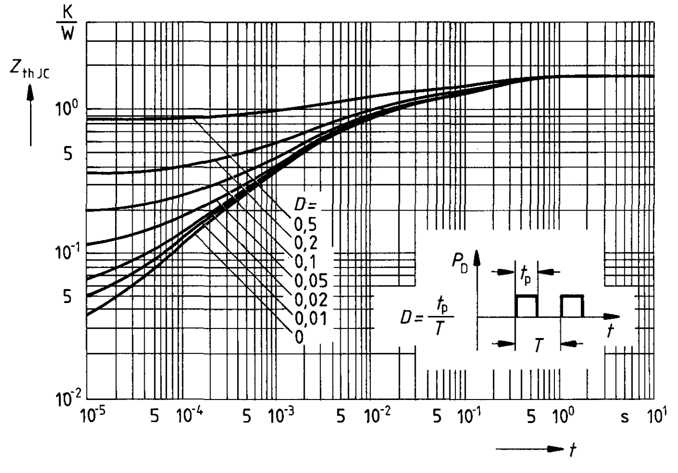
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



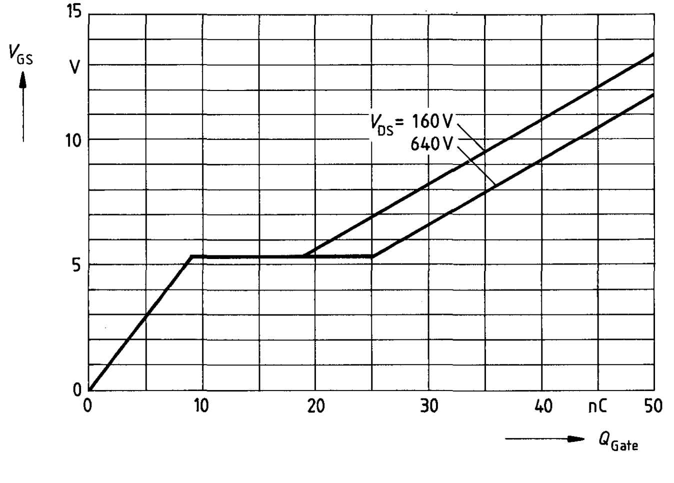
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



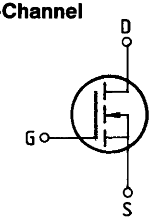
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 5A$



Main ratings

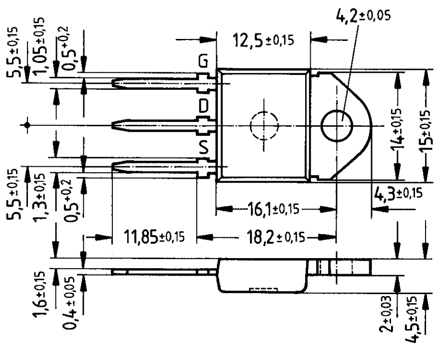
Drain-source voltage V_{DS} **= 1000 V**
Continuous drain current I_D **= 2,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 5,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 310	C67078-A3101-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	10	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

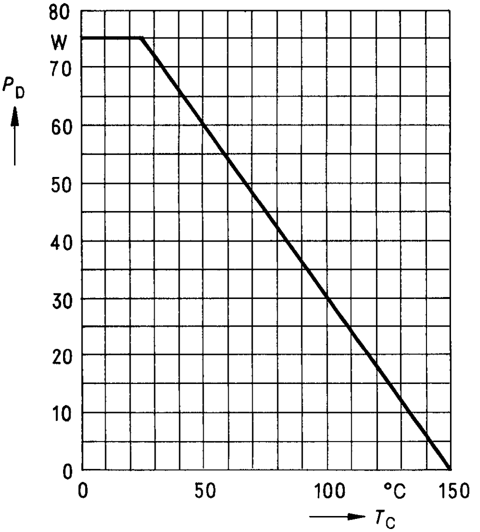
 S Preferred Type

Electrical characteristics

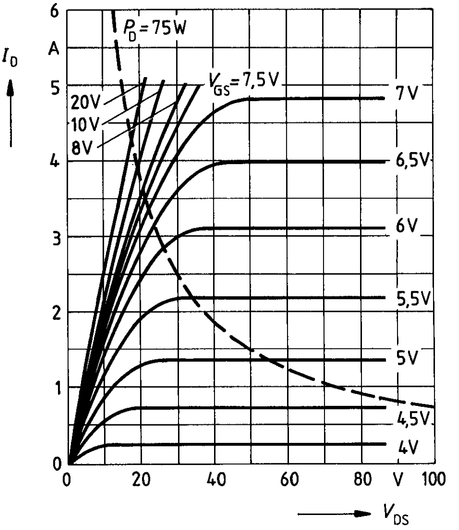
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	4,5	5,0	Ω	V_{GS} = 10V I_D = 1,6A
Dynamic ratings						
Forward transconductance	g_{fs}	0,7	1,5	–	S	V_{DS} = 25V I_D = 1,6A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	70	120	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	10		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2,0	–	µs	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	15	–	µC	

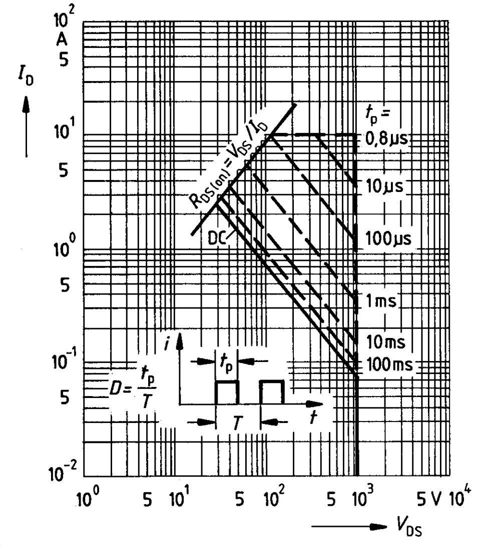
Power dissipation $P_D = f(T_C)$



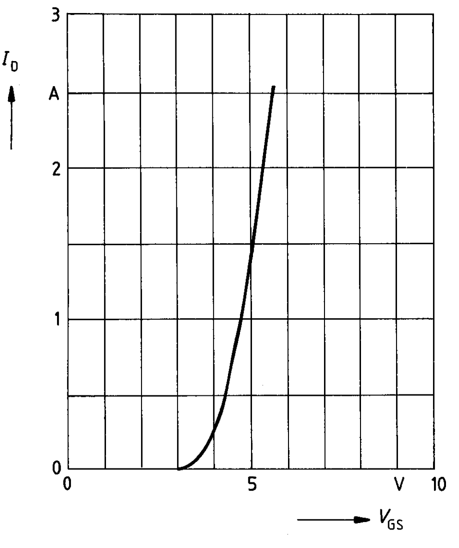
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



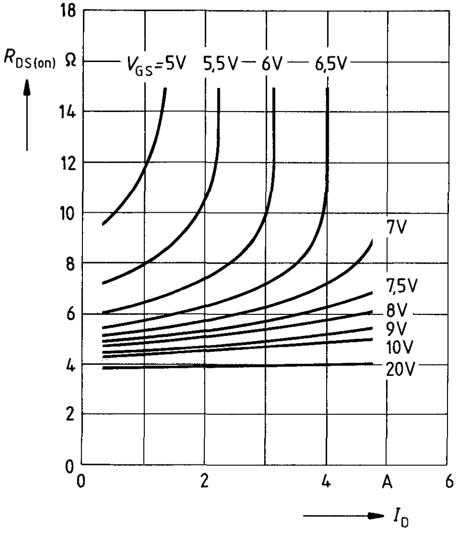
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



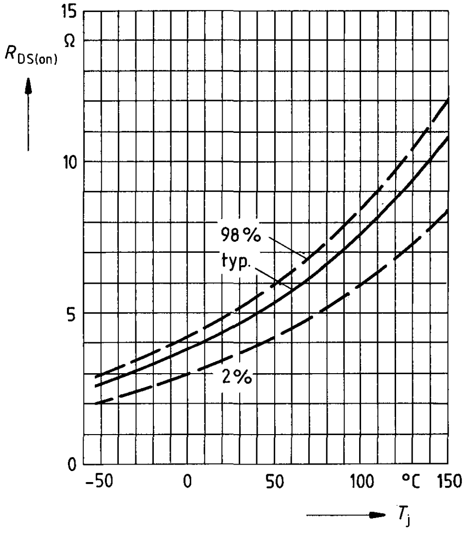
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



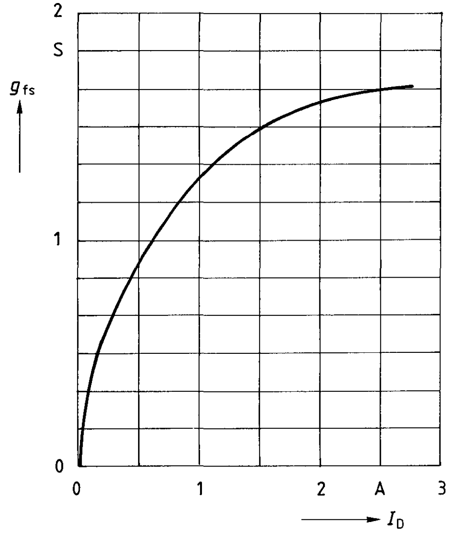
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



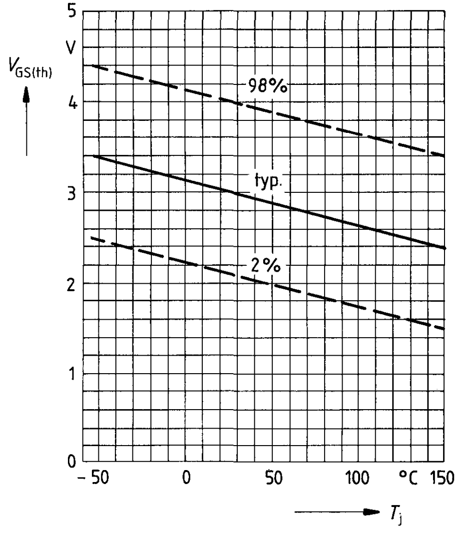
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 1,6A, V_{GS} = 10V
(spread)



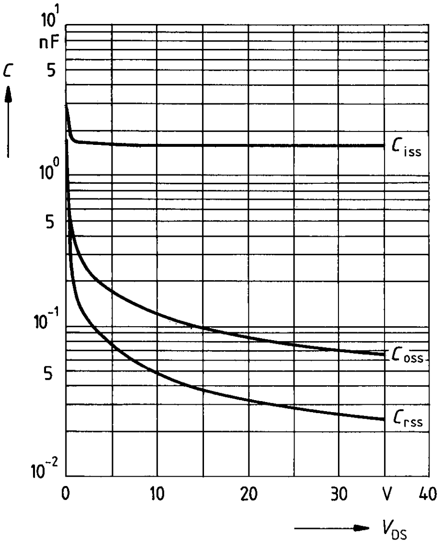
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



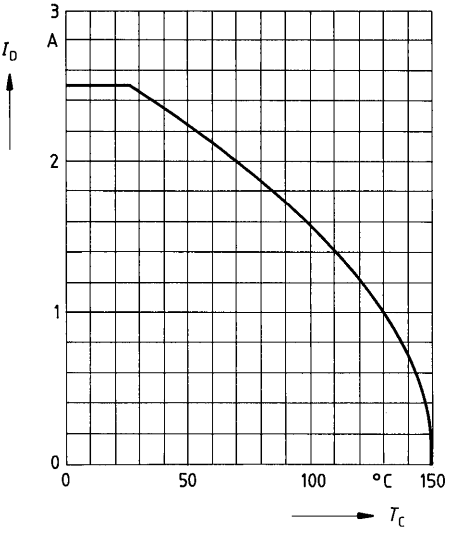
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



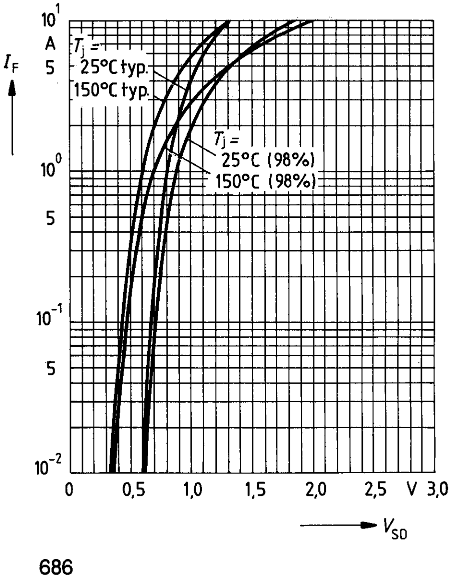
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



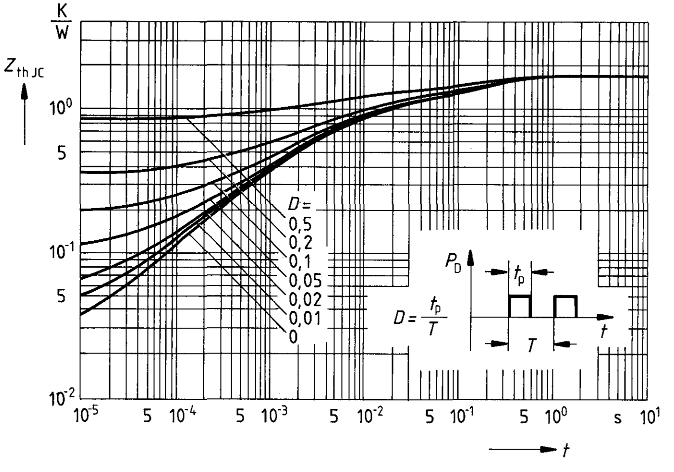
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



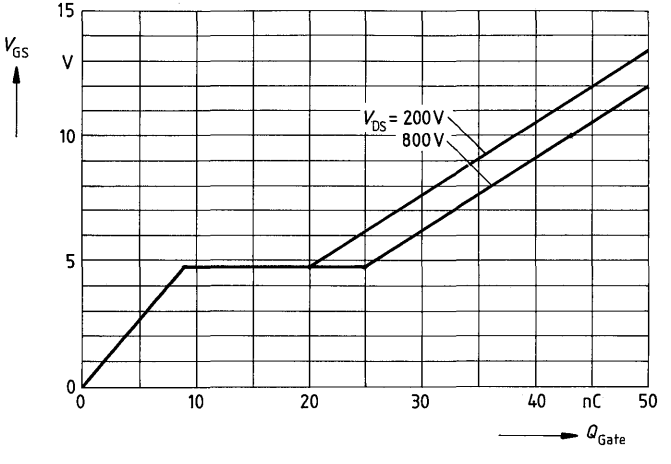
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

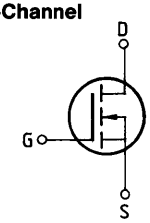


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 3{,}75A$



Main ratings

N-Channel

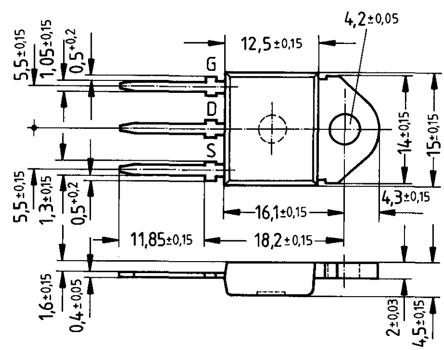


Drain-source voltage	V_{DS}	**= 1000 V**
Continuous drain current	I_D	**= 2,3 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 6,0 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
Ⓢ BUZ 311	C67078-A3102-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,3	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	9,0	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

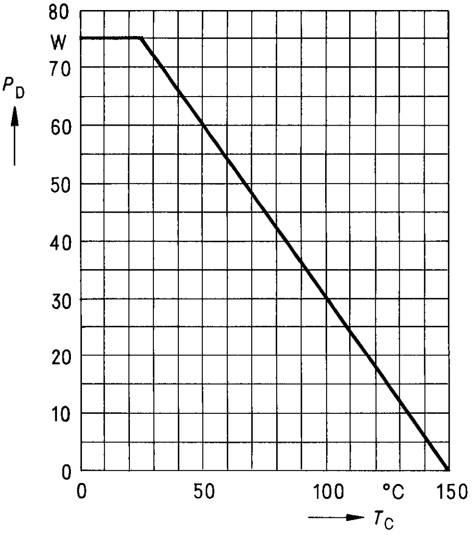
 Ⓢ Preferred Type

Electrical characteristics

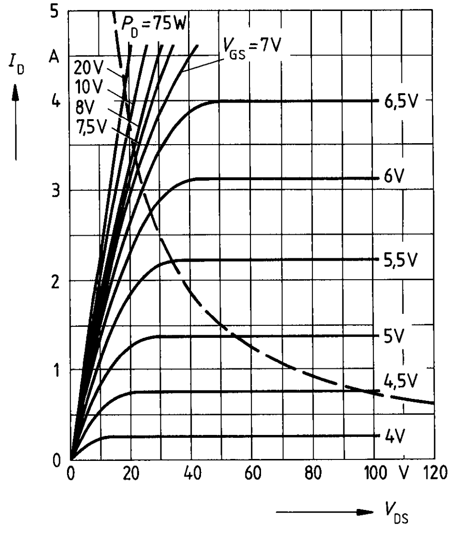
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	5,0	6,0	Ω	V_{GS} = 10V I_D = 1,6A
Dynamic ratings						
Forward transconductance	g_{fs}	0,7	1,5	–	S	V_{DS} = 25V I_D = 1,6A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	70	120	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 1,7A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	40	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	110	140		
	t_f	–	60	80		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,3	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	9,0		
Diode forward on-voltage	V_{SD}	–	1,05	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2,0	–	µs	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	15	–	µC	

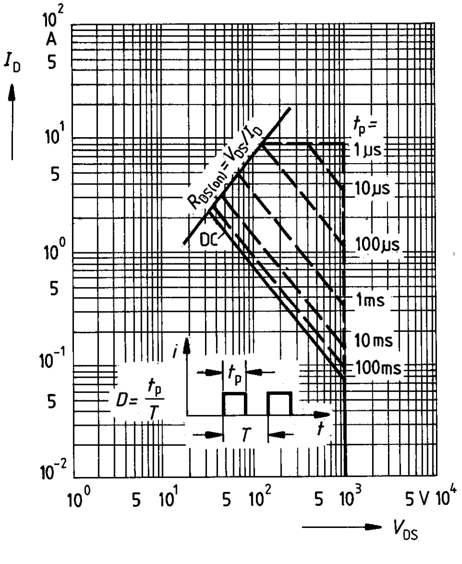
Power dissipation $P_D = f(T_C)$



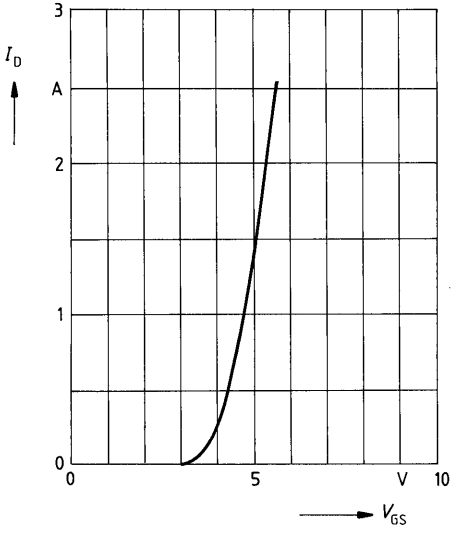
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



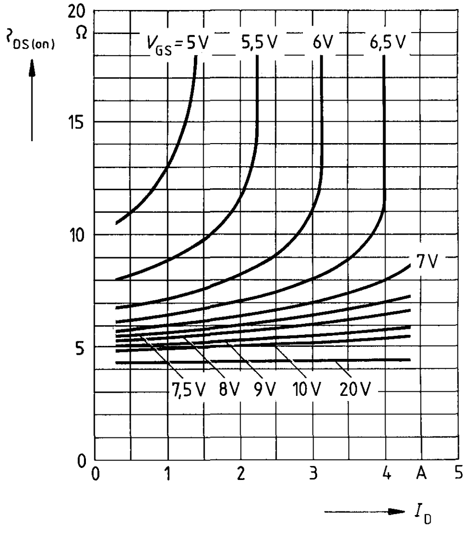
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



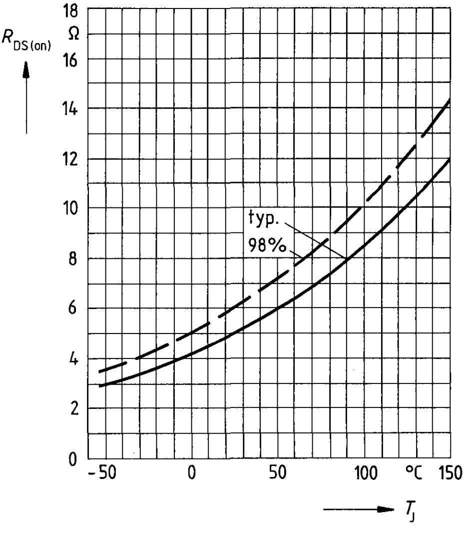
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



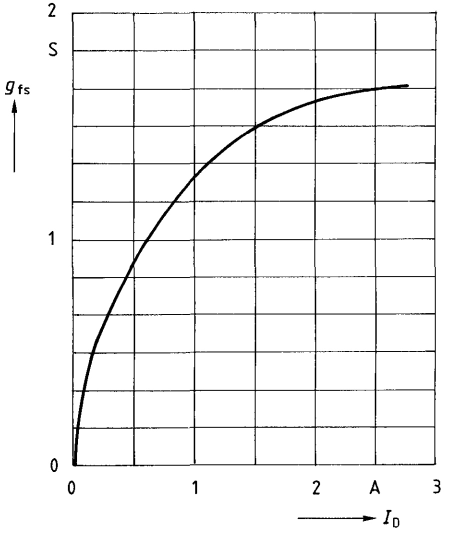
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



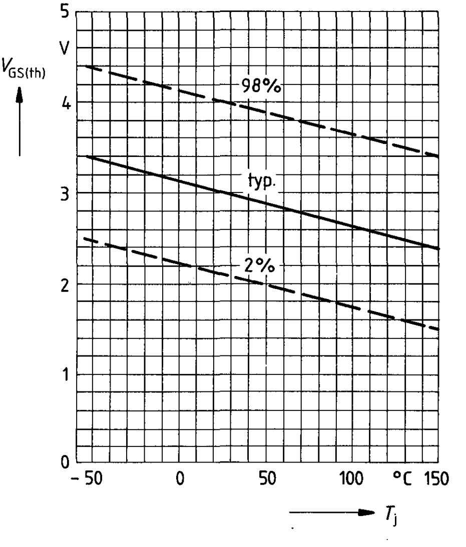
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 1,6A, V_{GS} = 10V
(spread)



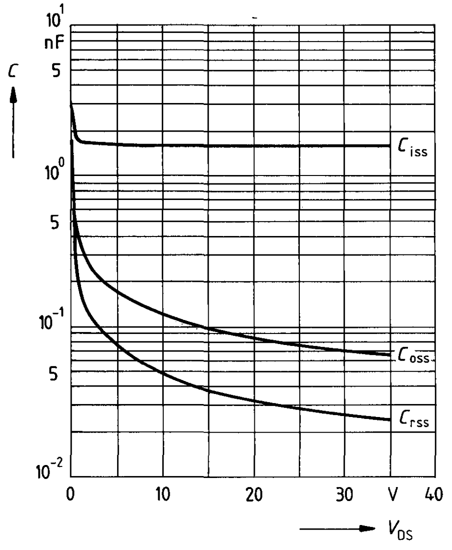
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



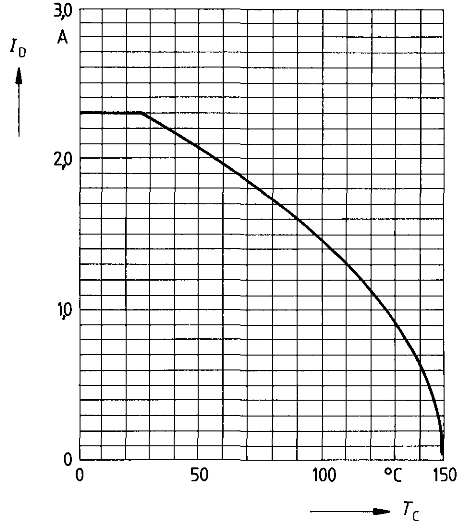
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



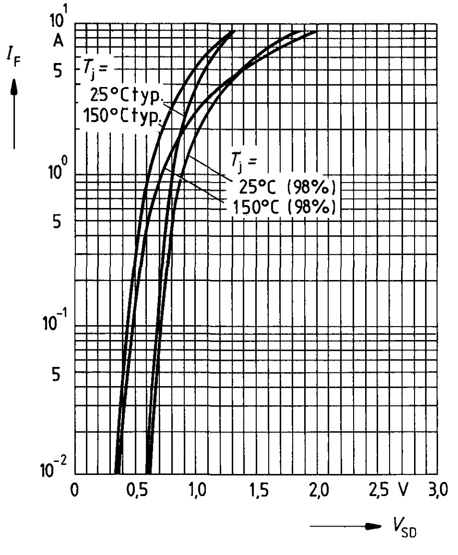
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



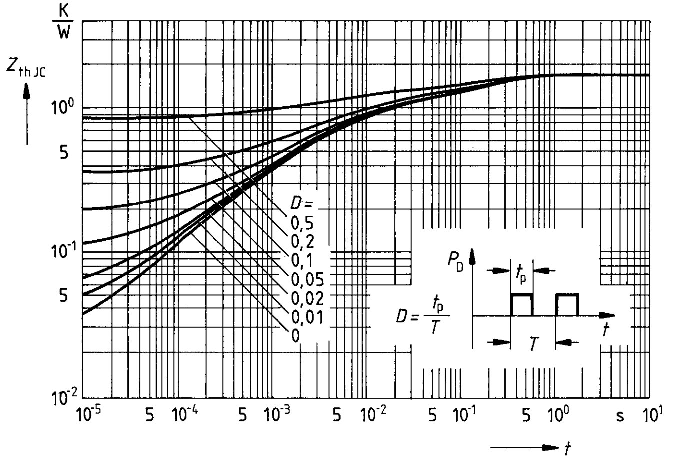
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



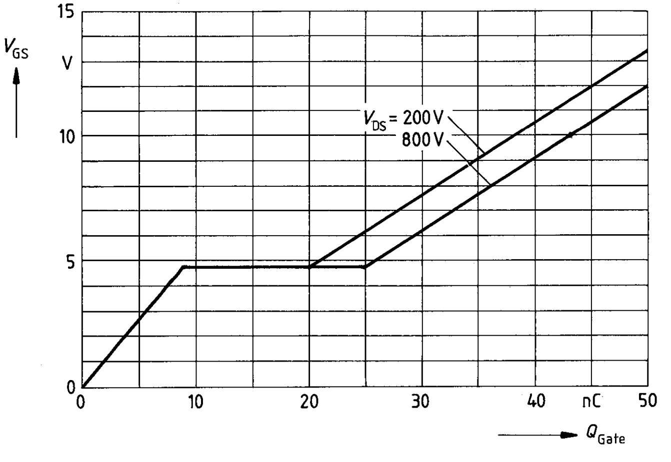
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



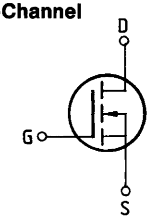
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 3{,}75A$



Main ratings

N-Channel

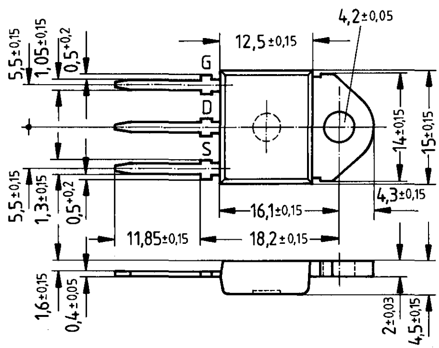
Drain-source voltage	V_{DS}	=	**400 V**
Continuous drain current	I_D	=	**10,5 A**
Drain-source on-resistance	$R_{DS(on)}$	=	**0,5 Ω**



Description SIPMOS, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 326	C67078-A3112-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	10,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	42	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

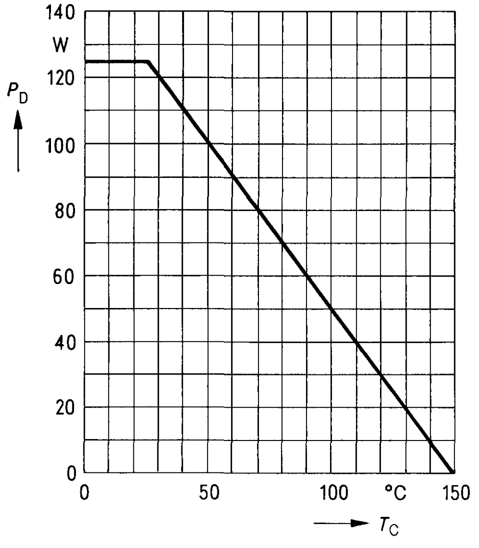
 S Preferred Type

Electrical characteristics

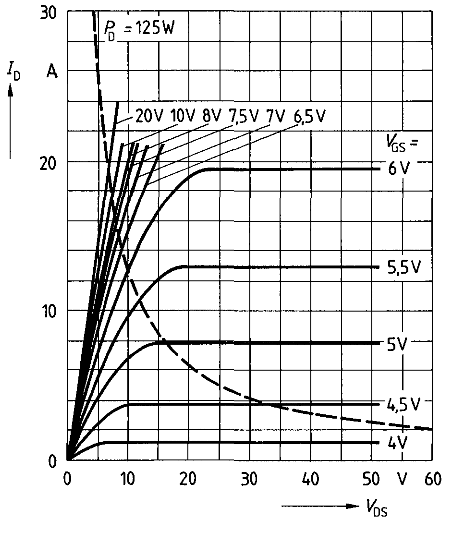
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,4	0,5	Ω	V_{GS} = 10V I_D = 6,0A
Dynamic ratings						
Forward transconductance	g_{fs}	5,0	8,0	–	S	V_{DS} = 25V I_D = 6,0A
Input capacitance	C_{iss}	–	1,35	1,75	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	200	320	pF	
Reverse transfer capacitance	C_{rss}	–	90	150		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	25	40	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	45	70		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	250	310		
	t_f	–	75	90		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	10,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	42		
Diode forward on-voltage	V_{SD}	–	1,0	1,5	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	–	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	–	–	µC	

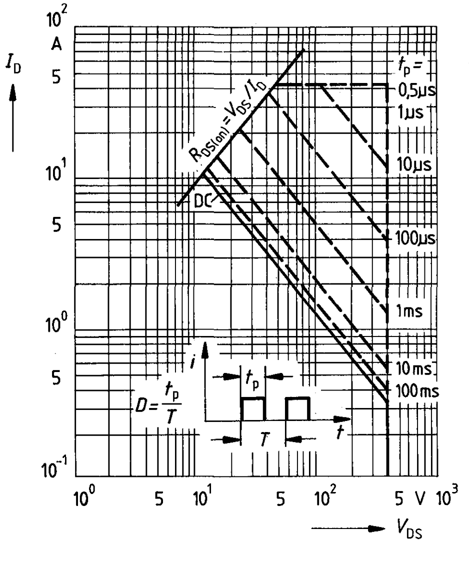
Power dissipation $P_D = f(T_C)$



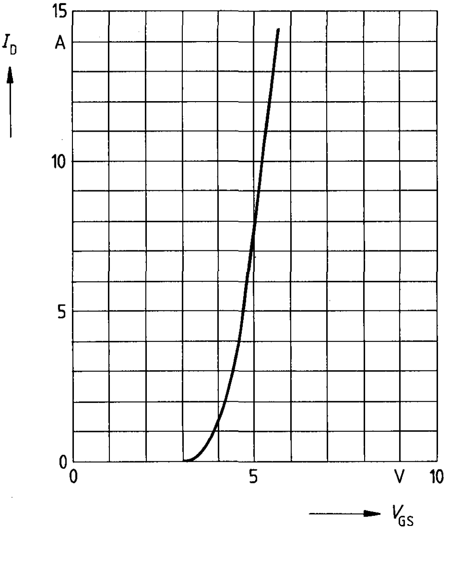
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



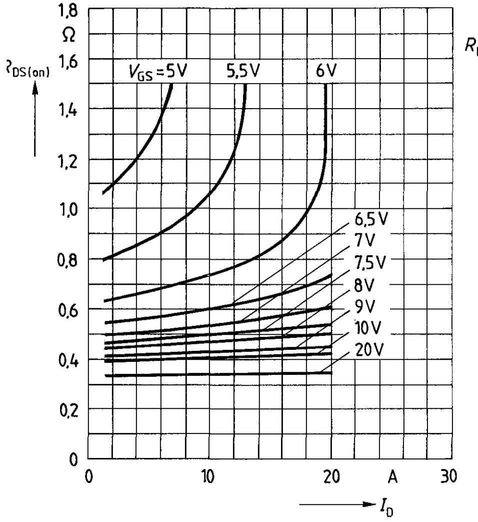
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



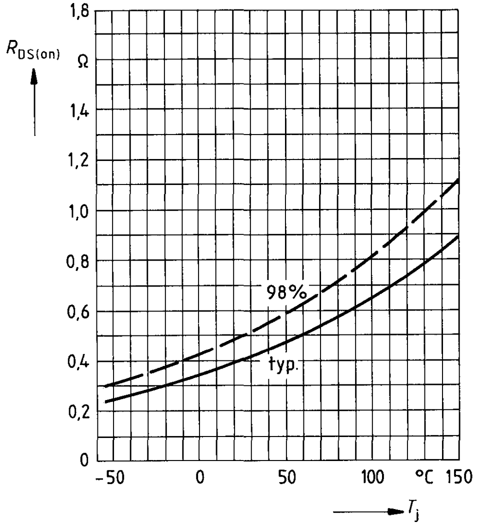
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



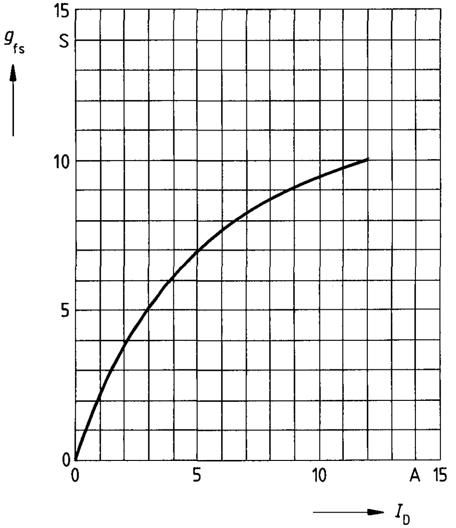
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



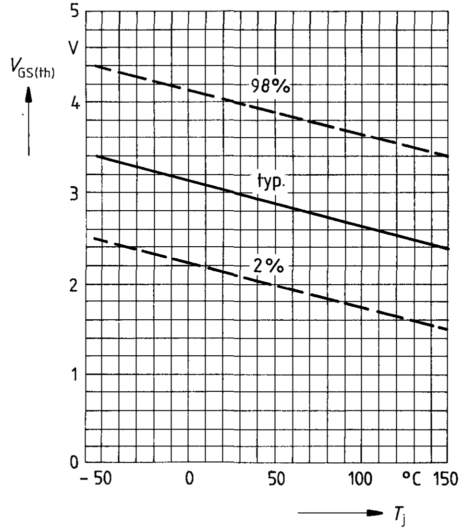
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 6A$, $V_{GS} = 10V$
(spread)



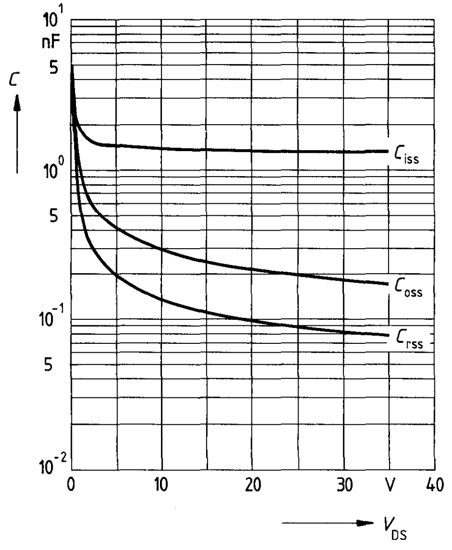
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



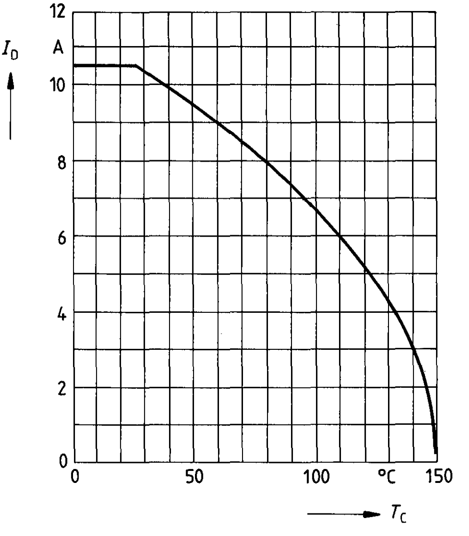
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



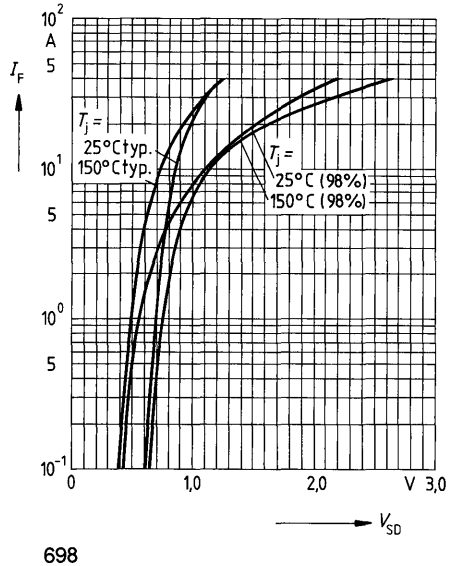
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



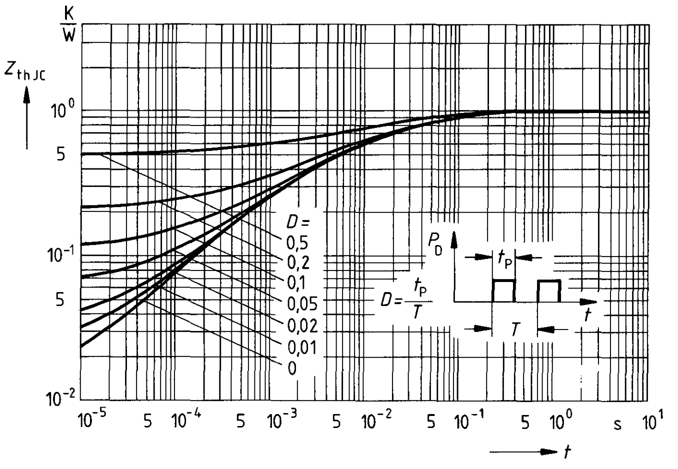
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



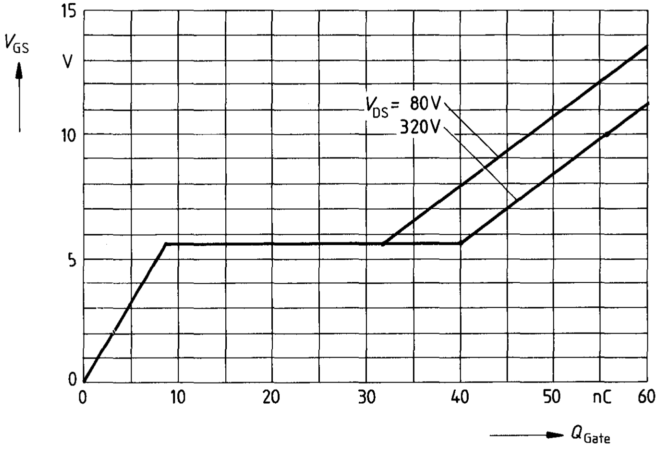
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



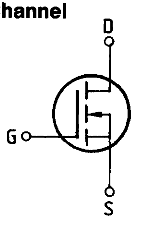
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14{,}3A$



Main ratings

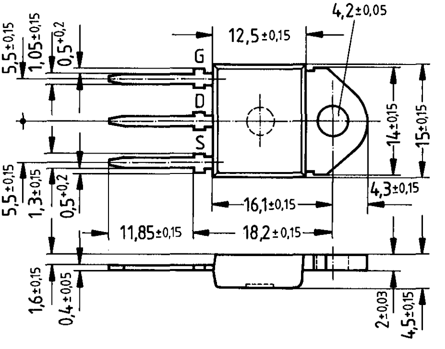
Drain-source voltage V_{DS} = 500 V
Continuous drain current I_D = 9,5 A
Drain-source on-resistance $R_{DS(on)}$ = 0,6 Ω

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 330	C67078-A3105-A2



Dimensions in mm

Maximum ratings

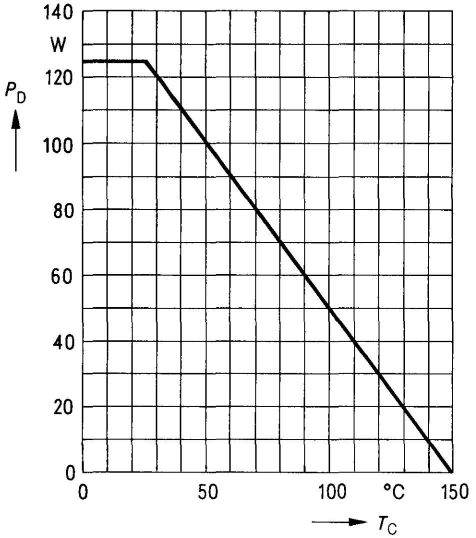
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	9,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	38	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

Electrical characteristics

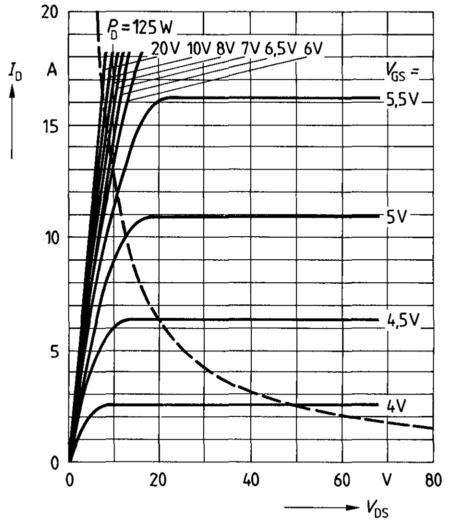
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,5	0,6	Ω	V_{GS} = 10V I_D = 6,0A
Dynamic ratings						
Forward transconductance	g_{fs}	5,0	8,0	–	S	V_{DS} = 25V I_D = 6,0A
Input capacitance	C_{iss}	–	1,35	1,80	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	270	pF	
Reverse transfer capacitance	C_{rss}	–	80	120		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	25	40	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	45	70		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	250	310		
	t_f	–	75	90		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	9,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	38		
Diode forward on-voltage	V_{SD}	–	1,0	1,4	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	–	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	–	–	µC	

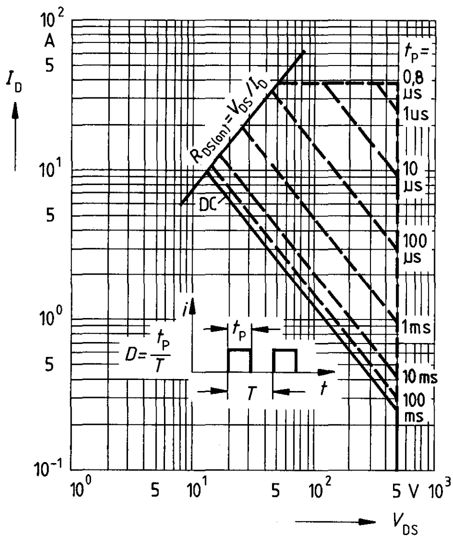
Power dissipation $P_D = f(T_C)$



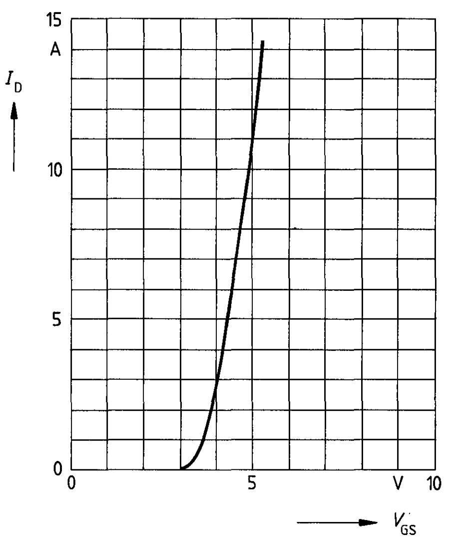
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



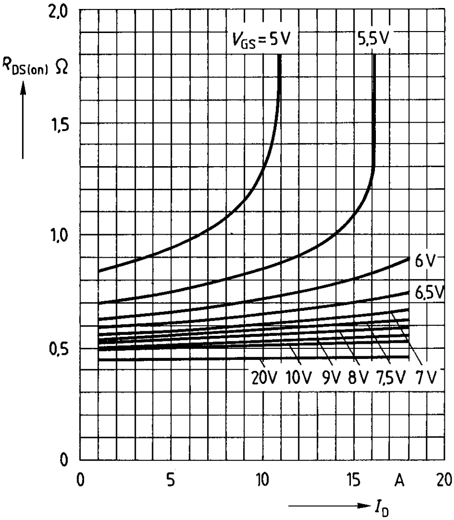
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



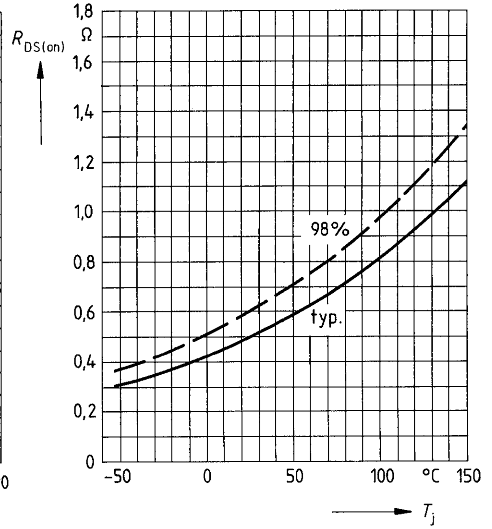
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



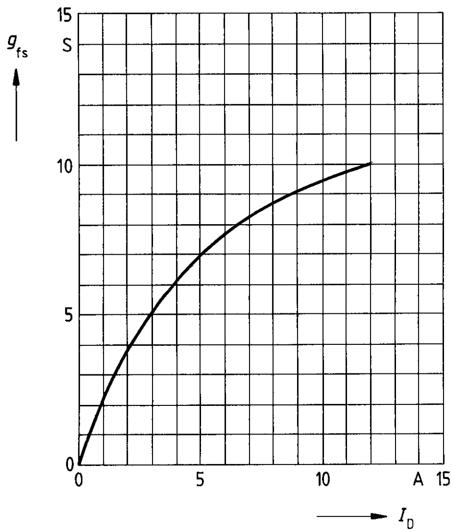
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



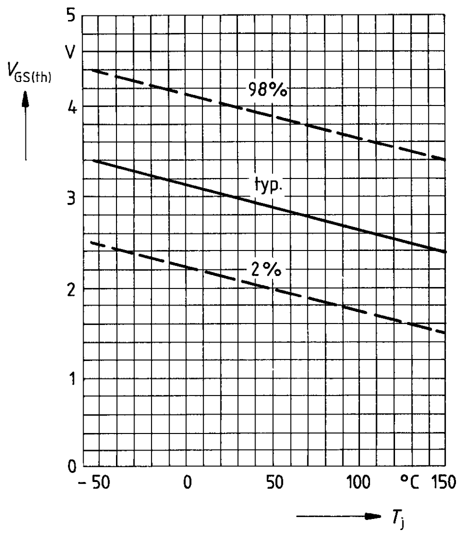
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 6,0A, V_{GS} = 10V
(spread)



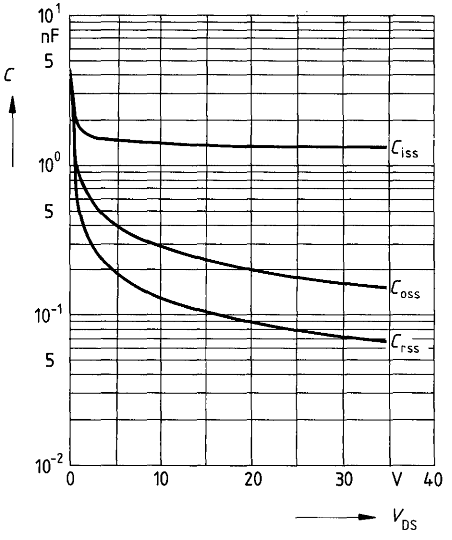
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



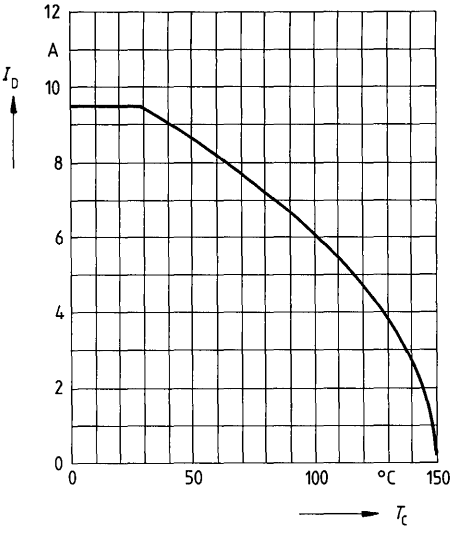
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



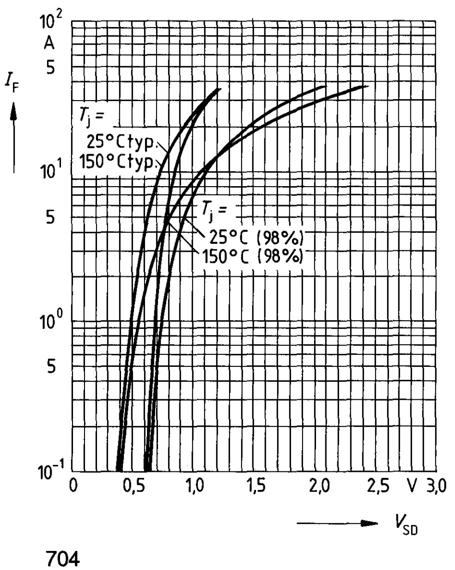
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



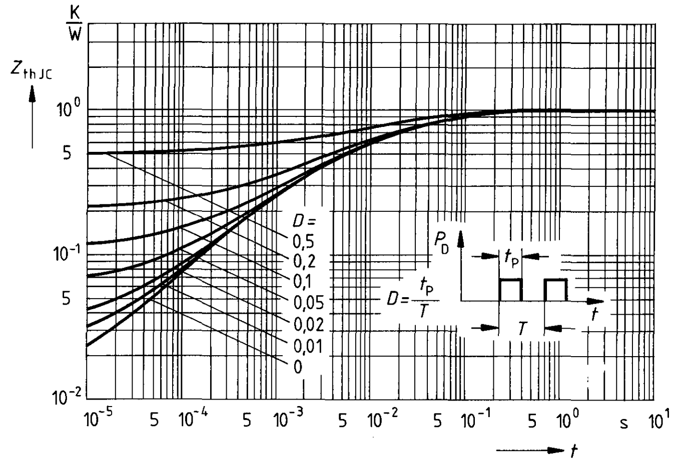
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



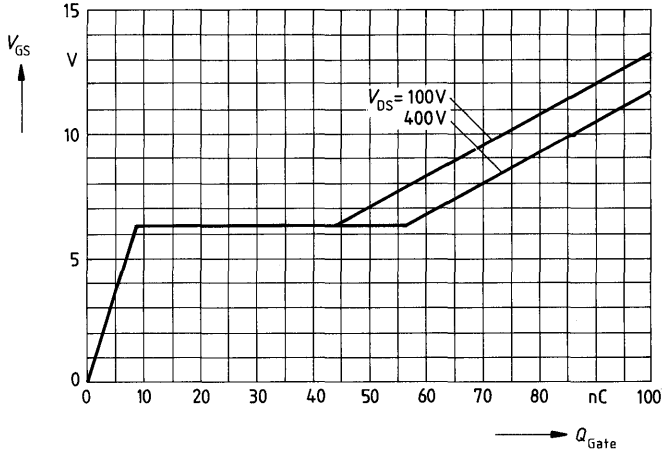
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



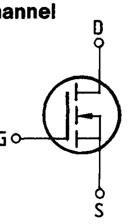
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 12{,}8A$



Main ratings

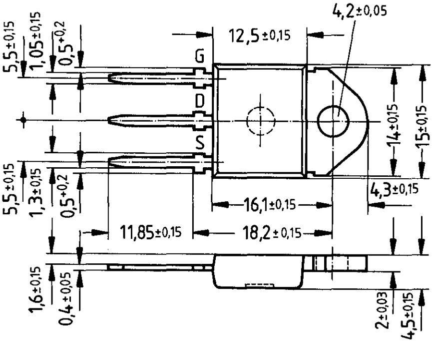
Drain-source voltage V_{DS} = **500 V**
Continuous drain current I_D = **8 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,8 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 331	C67078-A3119-A2



Dimensions in mm

Maximum ratings

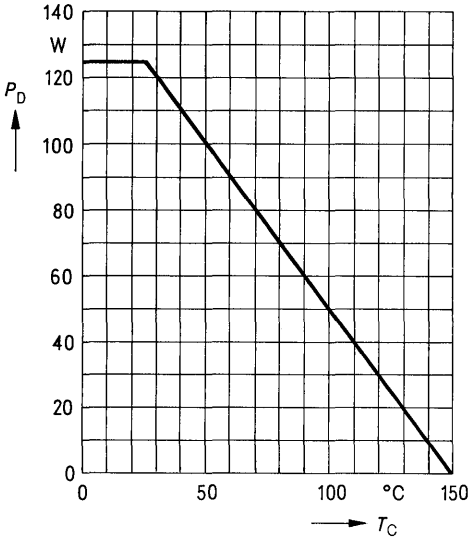
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	8	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	32	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤45	K/W	

Electrical characteristics

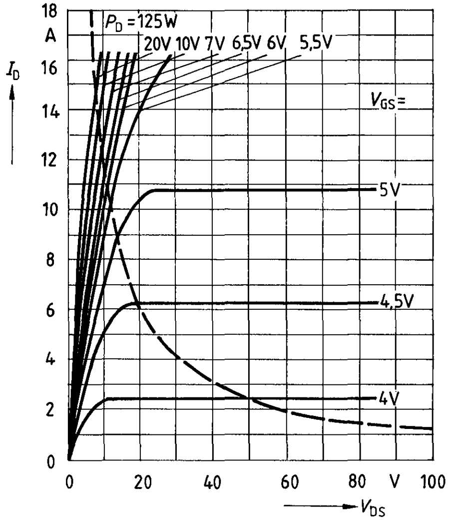
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	0,7	0,8	Ω	V_{GS} = 10V I_D = 6,0A
Dynamic ratings						
Forward transconductance	g_{fs}	5,0	8,0	–	S	V_{DS} = 25V I_D = 6,0A
Input capacitance	C_{iss}	–	1,35	1,80	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	270	pF	
Reverse transfer capacitance	C_{rss}	–	80	120		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	25	40	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	45	70		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	250	310		
	t_f	–	75	90		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	8	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	32		
Diode forward on-voltage	V_{SD}	–	1,0	1,4	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	–	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	–	–	µC	

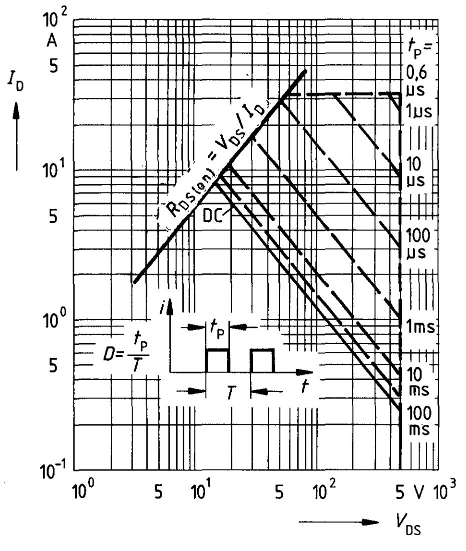
Power dissipation $P_D = f(T_C)$



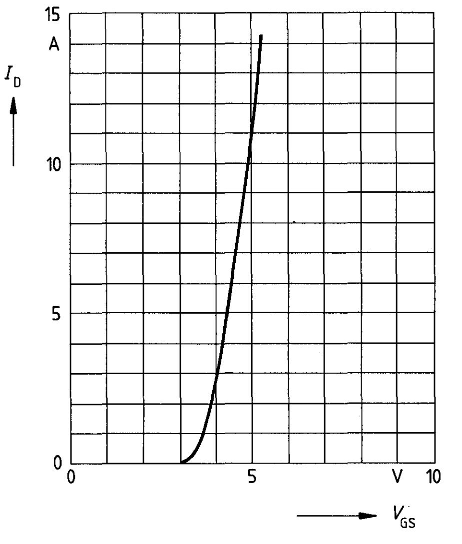
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



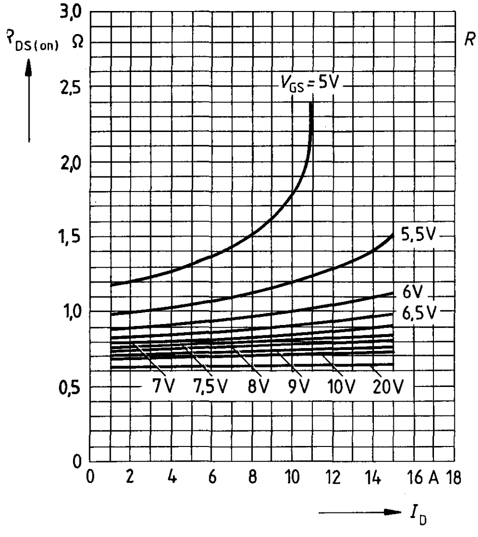
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



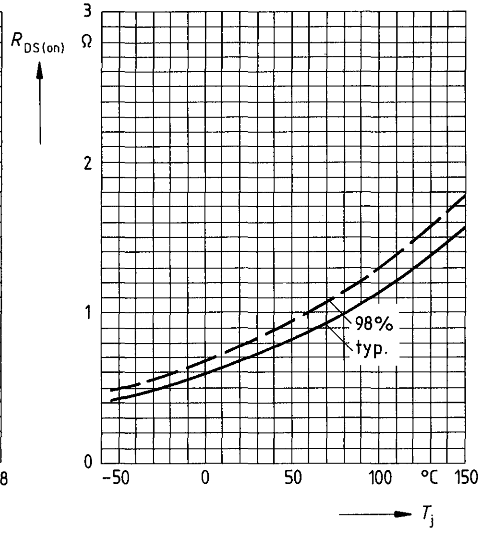
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



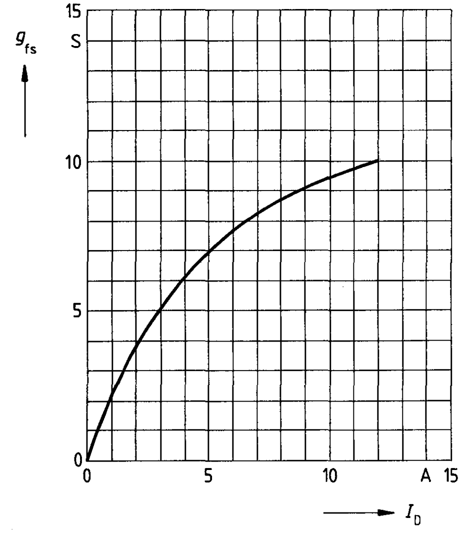
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



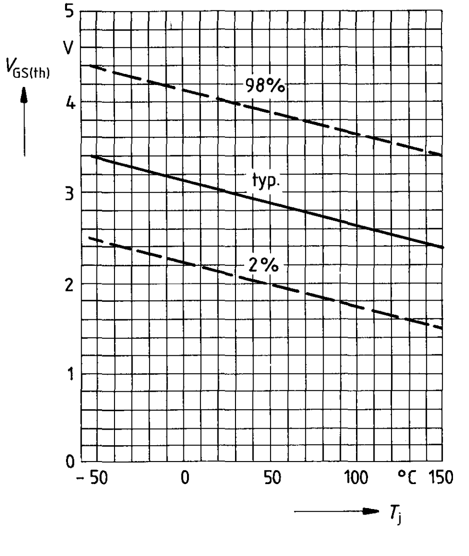
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 6,0A, V_{GS} = 10V
(spread)



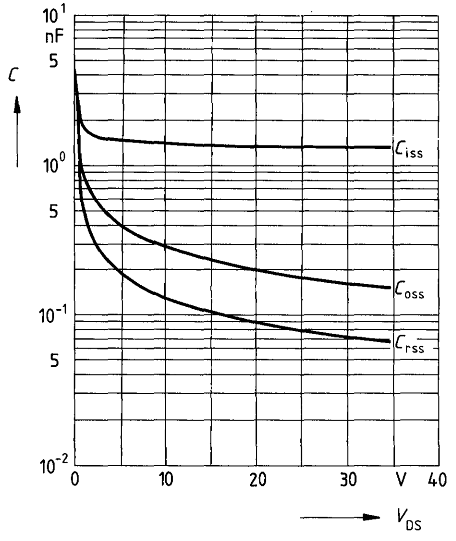
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



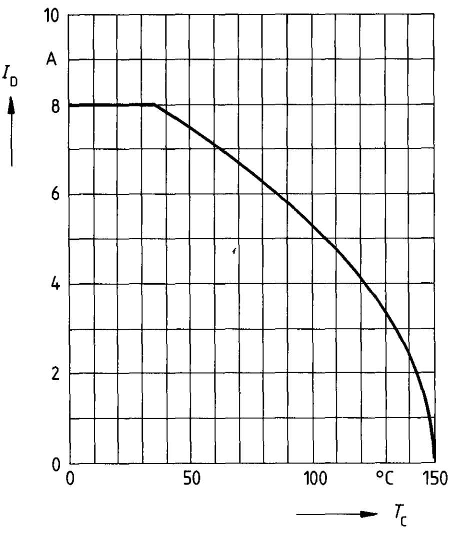
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



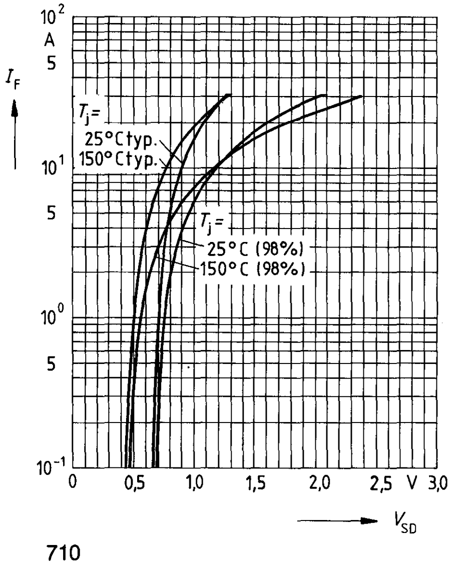
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



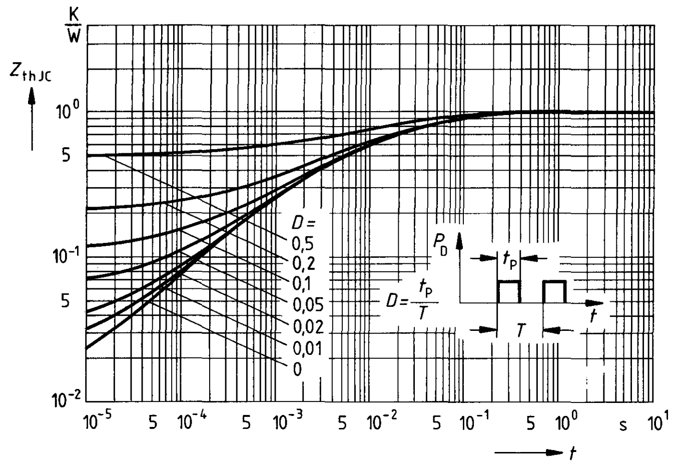
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



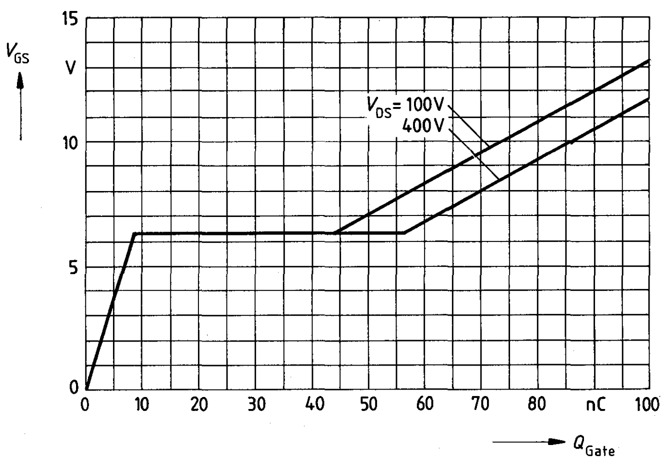
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

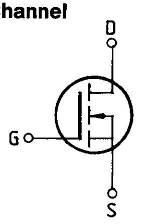


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 12{,}8A$



Main ratings

N-Channel

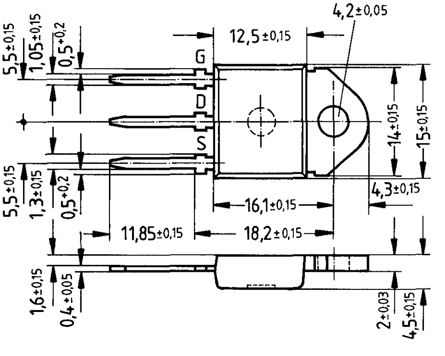


Drain-source voltage	V_{DS}	**= 50 V**
Continuous drain current	I_D	**= 40 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,03 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 347	C67078-A3115-A2



Dimensions in mm

Maximum ratings

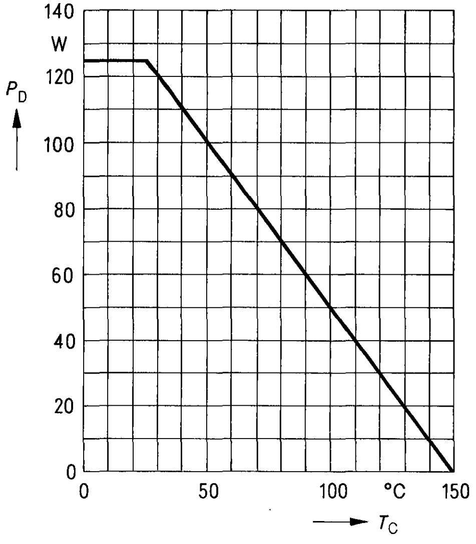
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	40	A	T_C = 55 °C
Pulsed drain current	I_{Dpuls}	160	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤ 45	K/W	

Electrical characteristics

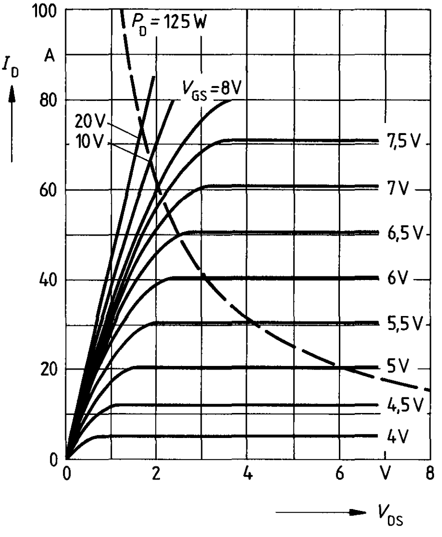
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	50	65	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,025	0,03	Ω	V_{GS} = 10V I_D = 28A
Dynamic ratings						
Forward transconductance	g_{fs}	7,0	18,0	–	S	V_{DS} = 25V I_D = 28A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	1300	2000	pF	
Reverse transfer capacitance	C_{rss}	–	500	800		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	110	170		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	250	330		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	40	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	160		
Diode forward on-voltage	V_{SD}	–	1,6	1,95	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	150	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,0	–	µC	

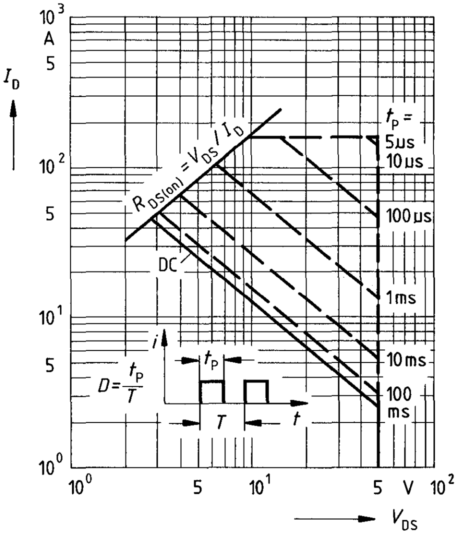
Power dissipation $P_D = f(T_C)$



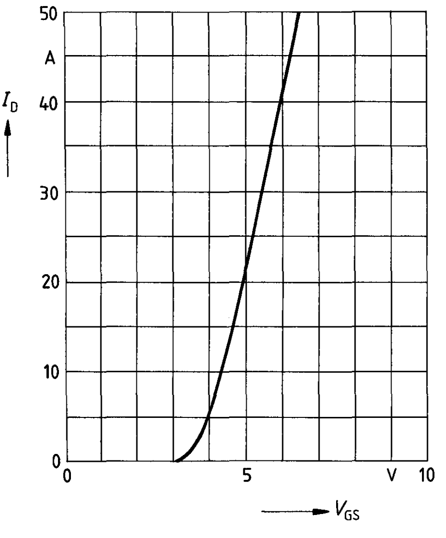
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



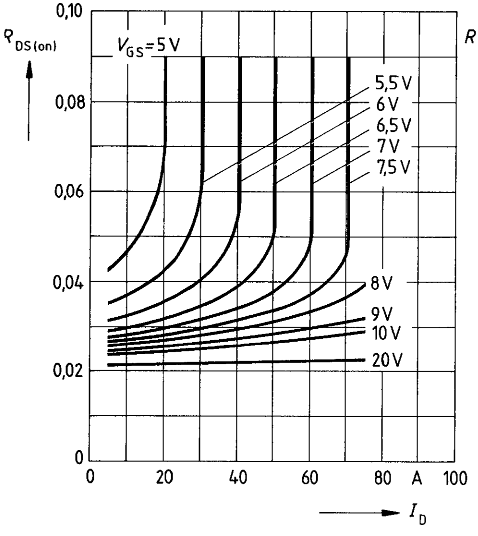
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



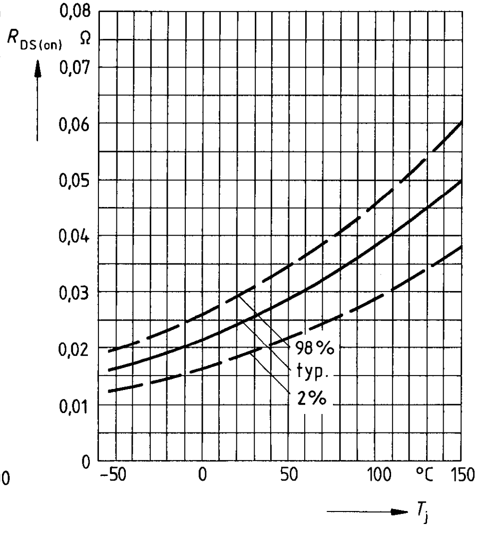
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\,V$, $T_j = 25\,°C$



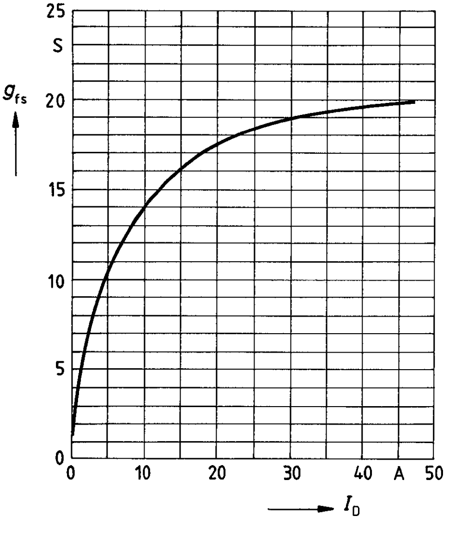
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



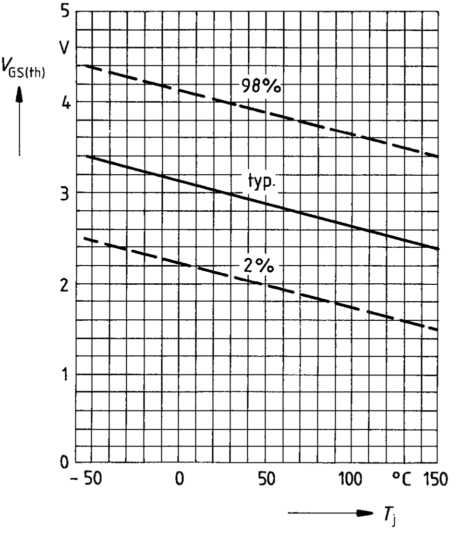
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 28A, V_{GS} = 10V
(spread)



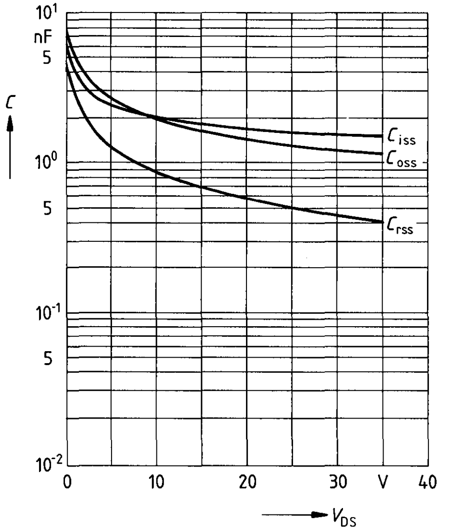
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



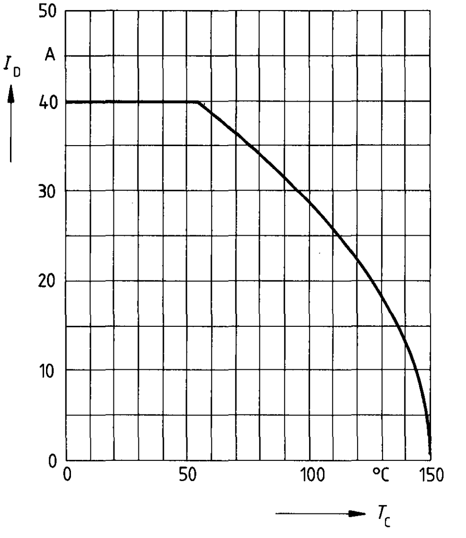
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



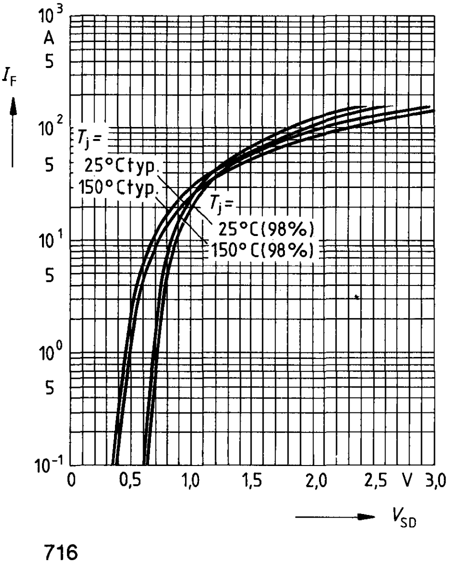
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



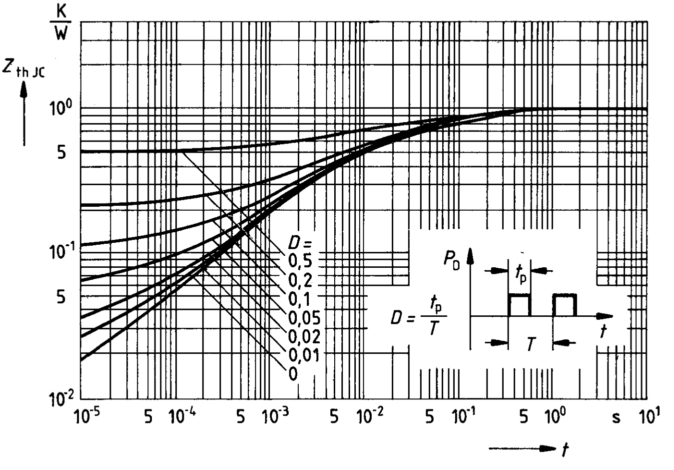
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



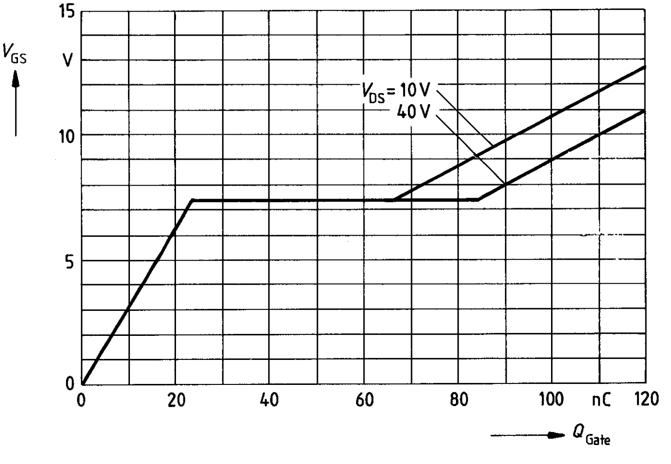
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu\text{s}$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



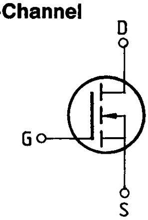
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 67{,}5A$



Main ratings

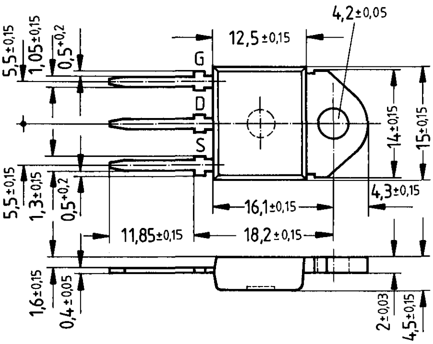
Drain-source voltage V_{DS} **= 50 V**
Continuous drain current I_D **= 39 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,04 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 348	C67078-A3116-A2



Dimensions in mm

Maximum ratings

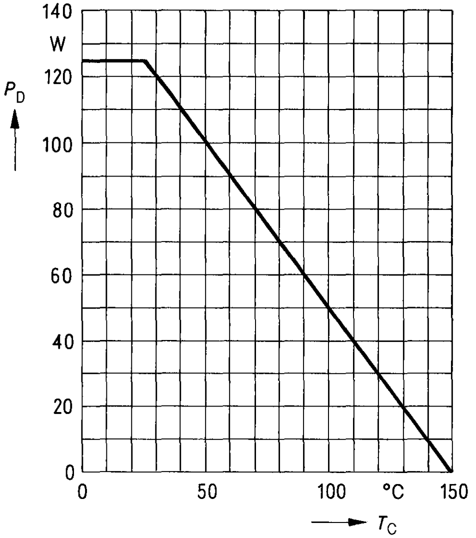
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	50	V	
Drain-gate voltage	V_{DGR}	50	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	39	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	156	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤1,0	K/W	
Chip – ambient	$R_{th JA}$	≤45	K/W	

Electrical characteristics

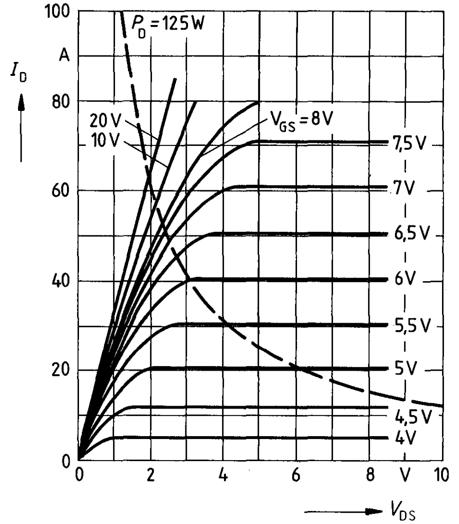
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	50	65	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 50V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	0,035	0,04	Ω	V_{GS} = 10V I_D = 28A
Dynamic ratings						
Forward transconductance	g_{fs}	7,0	18,0	–	S	V_{DS} = 25V I_D = 28A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	1300	2000	pF	
Reverse transfer capacitance	C_{rss}	–	500	800		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	110	170		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	250	330		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	39	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	156		
Diode forward on-voltage	V_{SD}	–	1,6	1,95	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	150	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,0	–	µC	

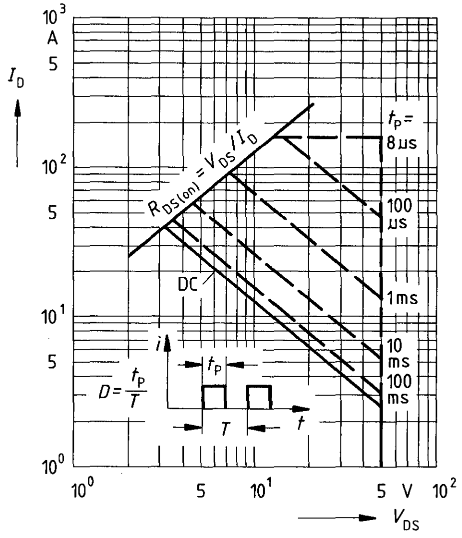
Power dissipation $P_D = f(T_C)$



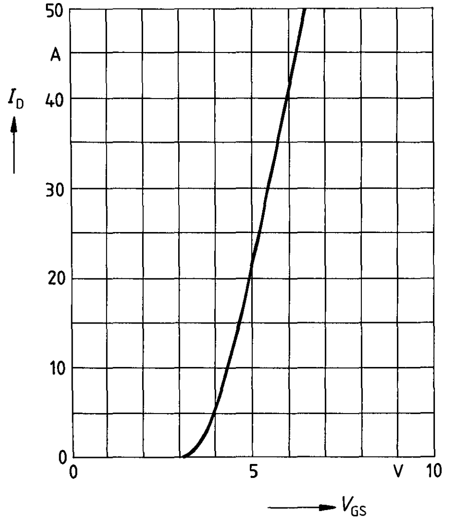
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



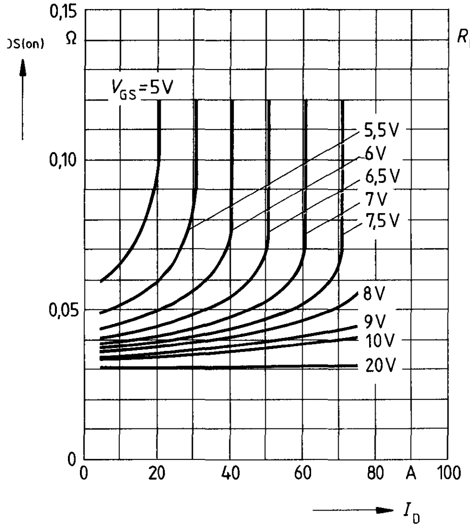
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



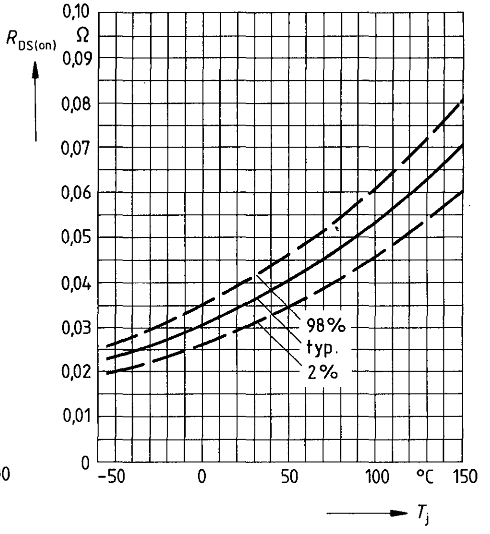
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



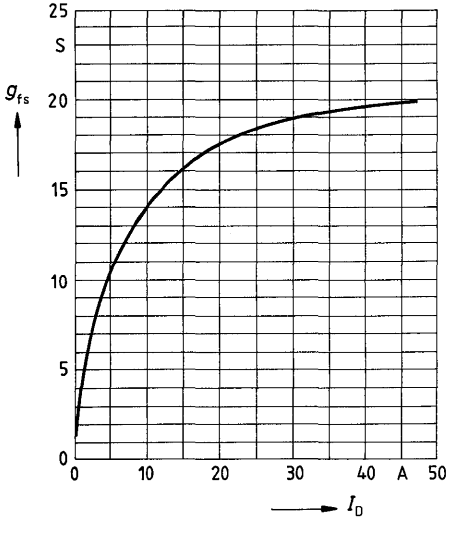
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



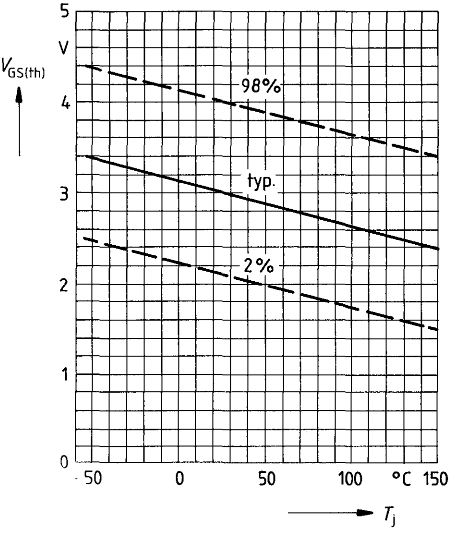
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 28A, V_{GS} = 10V
(spread)



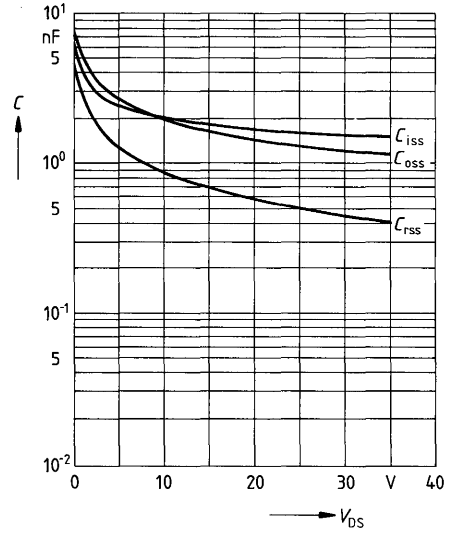
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



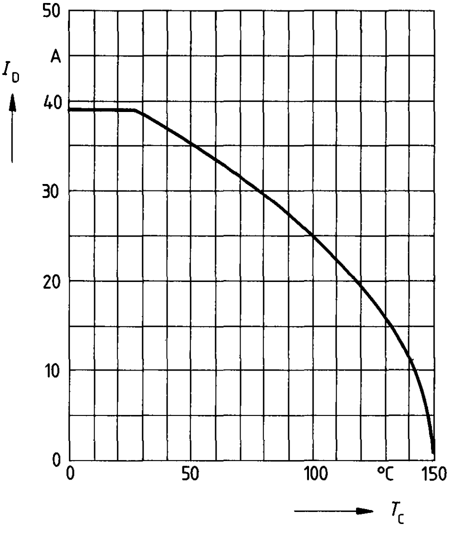
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



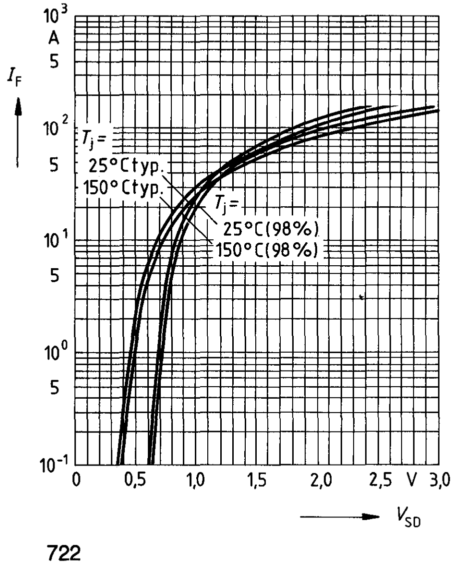
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



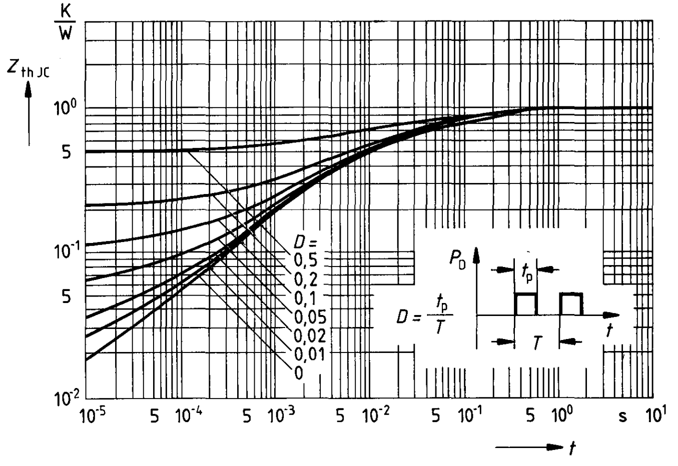
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



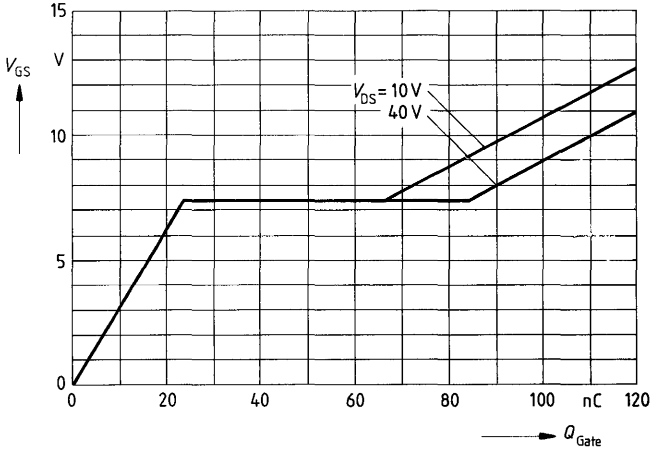
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



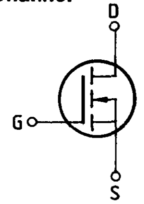
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 67{,}5A$



Main ratings

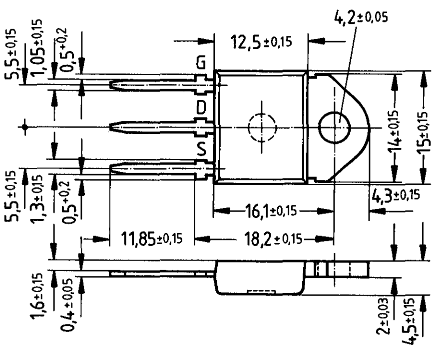
Drain-source voltage V_{DS} **= 100 V**
Continuous drain current I_D **= 32 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,06 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 349	C67078-A3113-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	100	V	
Drain-gate voltage	V_{DGR}	100	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	32	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	125	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 … + 150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

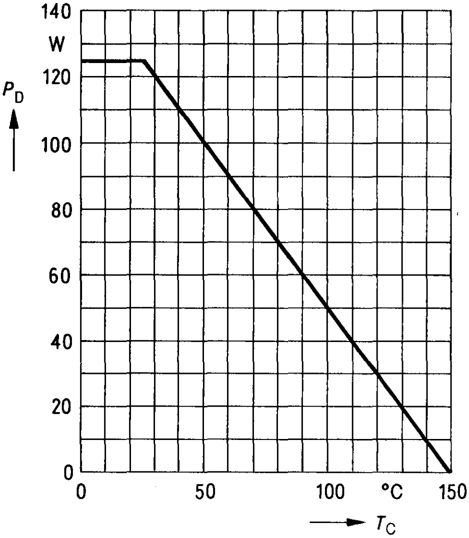
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

Electrical characteristics

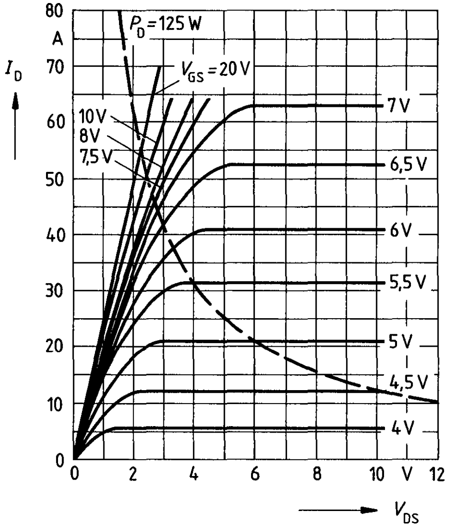
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	100	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 100V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,045	0,06	Ω	V_{GS} = 10V I_D = 21A
Dynamic ratings						
Forward transconductance	g_{fs}	6,0	18,0	–	S	V_{DS} = 25V I_D = 21A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	800	1200	pF	
Reverse transfer capacitance	C_{rss}	–	300	500		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	170	220		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	32	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	125		
Diode forward on-voltage	V_{SD}	–	1,5	2,0	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 30V
Reverse recovery charge	Q_{rr}	–	1,6	–	µC	

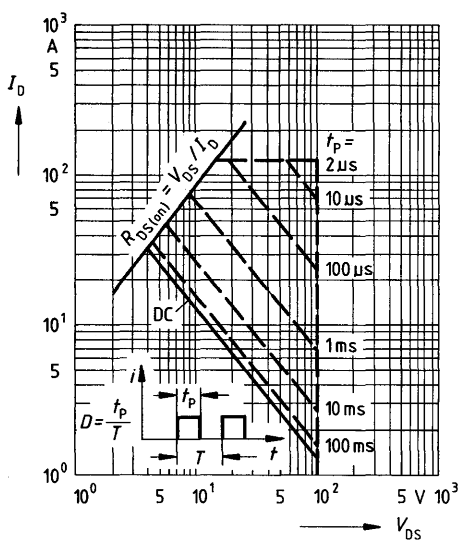
Power dissipation $P_D = f(T_C)$



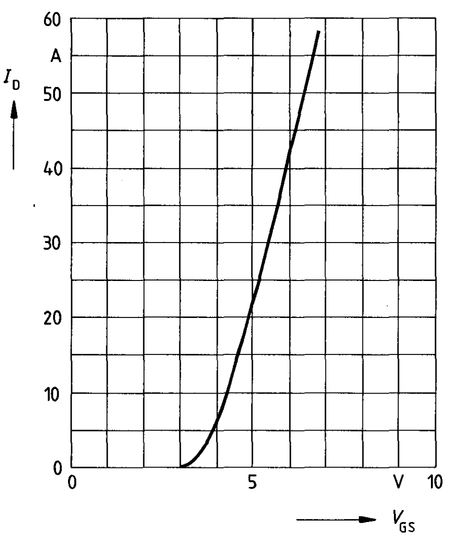
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
T_j = 25 °C



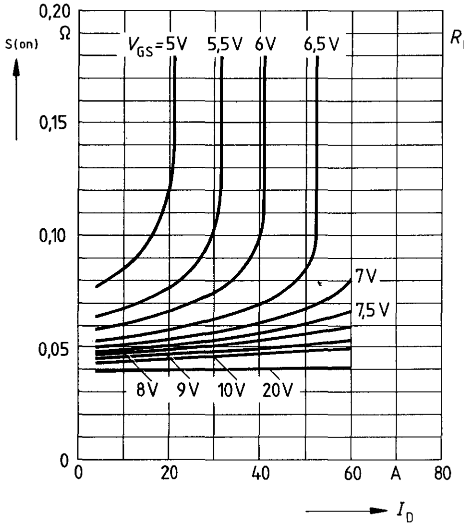
Safe operating area $I_D = f(V_{DS})$
parameter: D = 0.01, T_C = 25 °C



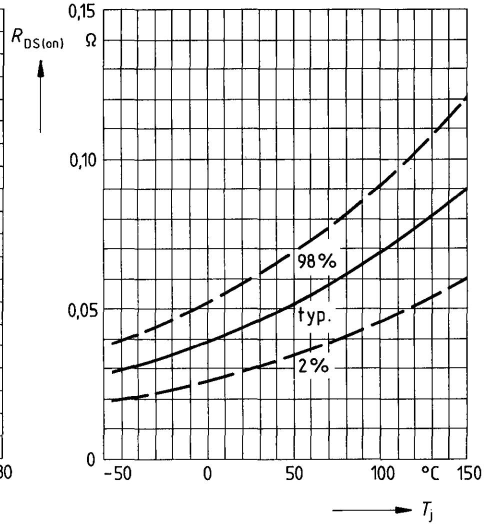
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



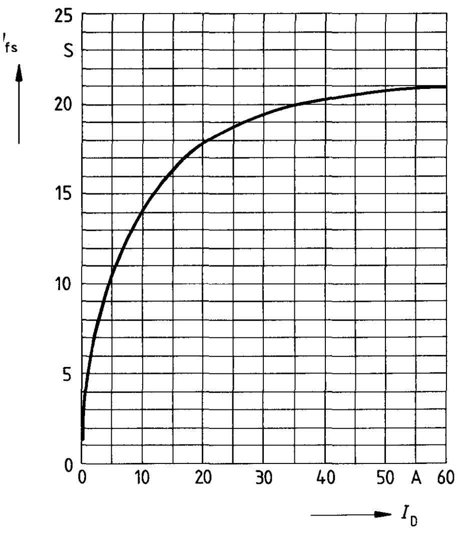
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



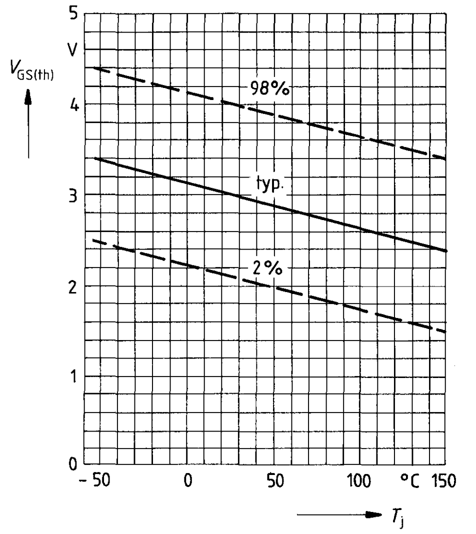
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 21A$, $V_{GS} = 10V$
(spread)



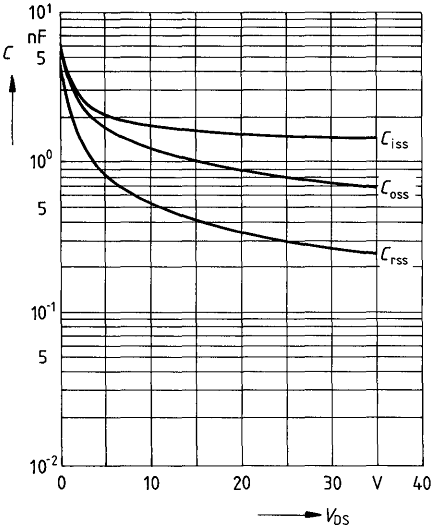
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



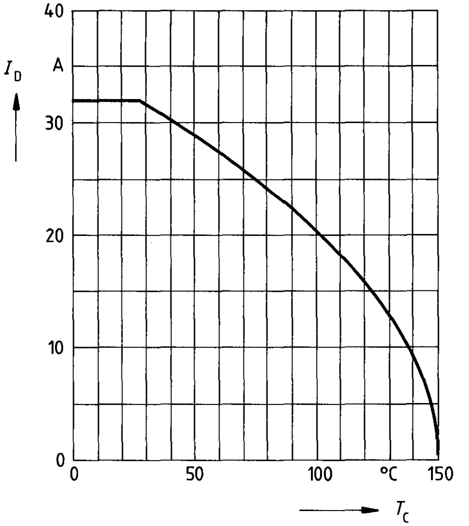
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



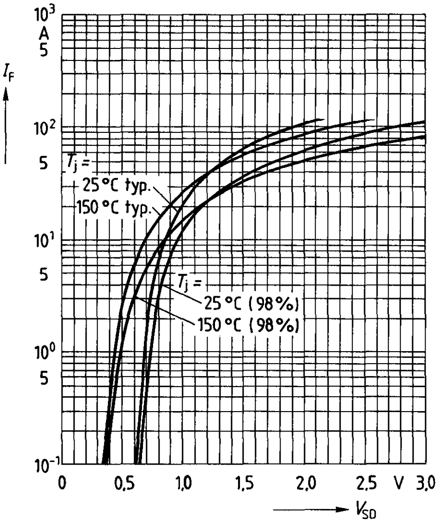
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



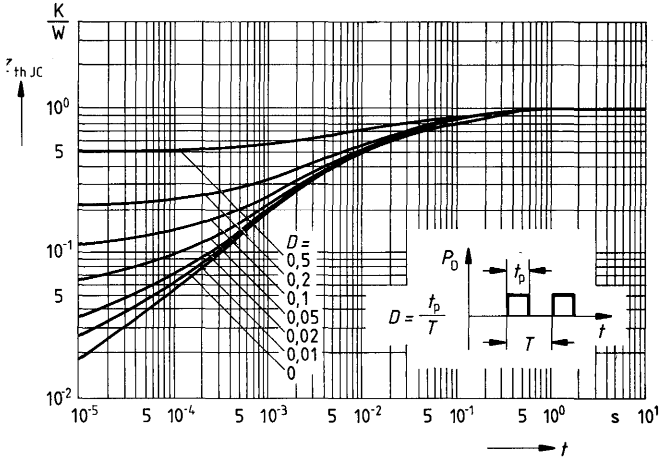
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



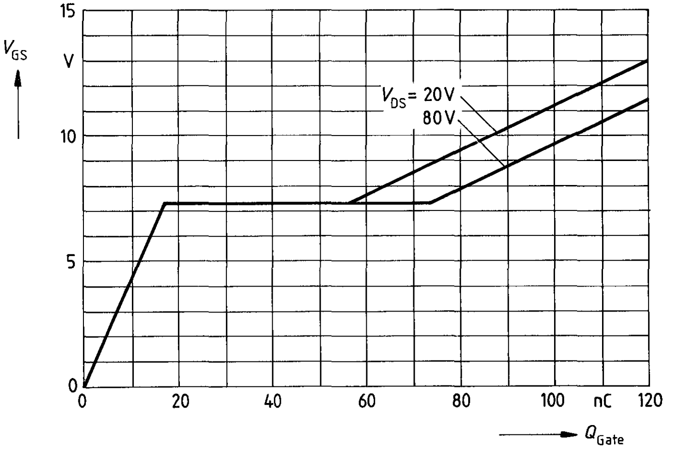
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

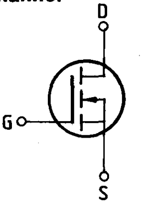


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 48A$



Main ratings

N-Channel

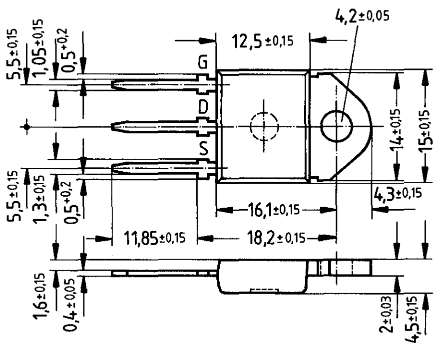


Drain-source voltage	V_{DS}	**= 200 V**
Continuous drain current	I_D	**= 22 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,12 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 350	C67078-A3317-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	200	V	
Drain-gate voltage	V_{DGR}	200	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	22	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	85	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

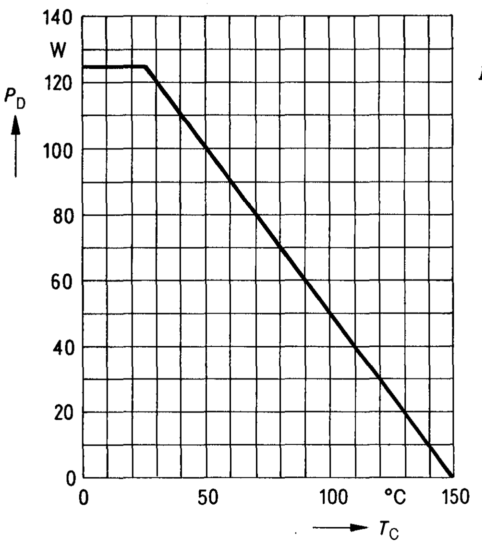
Chip – case	$R_{th\,JC}$	≤1,0	K/W
Chip – ambient	$R_{th\,JA}$	≤45	K/W

Electrical characteristics

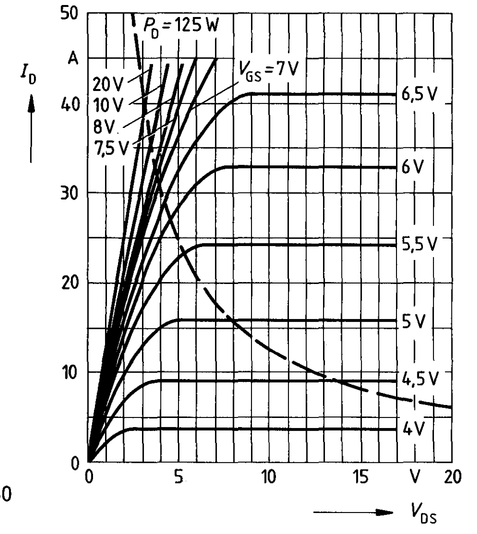
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	200	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 200V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,09	0,12	Ω	V_{GS} = 10V I_D = 11A
Dynamic ratings						
Forward transconductance	g_{fs}	9,0	13,0	–	S	V_{DS} = 25V I_D = 11A
Input capacitance	C_{iss}	–	1,5	2,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	500	800	pF	
Reverse transfer capacitance	C_{rss}	–	200	350		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	70	110		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	120	160		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	22	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	85		
Diode forward on-voltage	V_{SD}	–	1,2	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	400	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	6	–	µC	

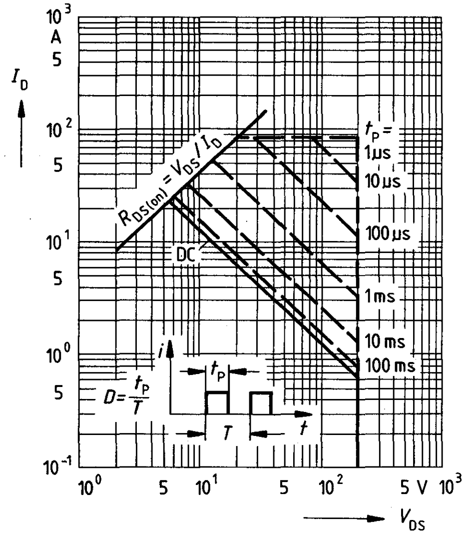
Power dissipation $P_D = f(T_C)$



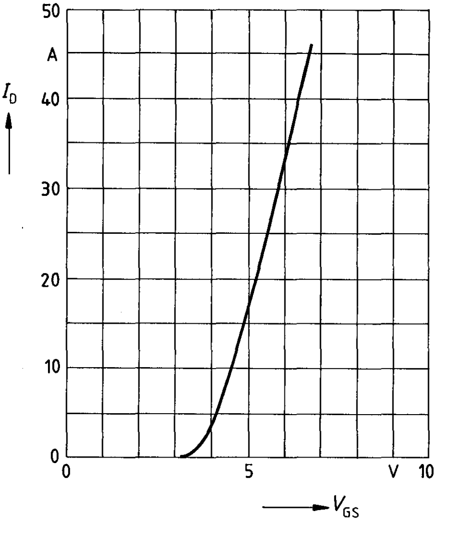
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



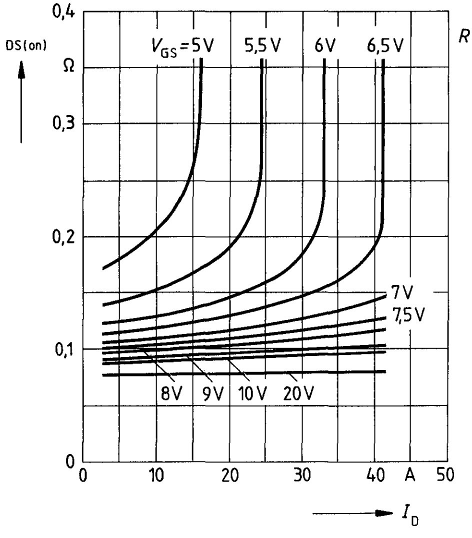
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



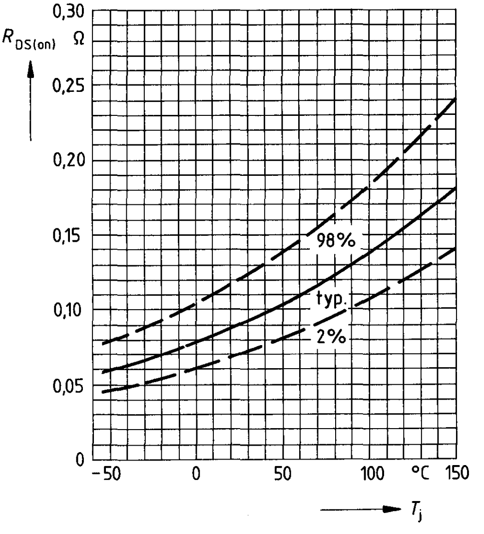
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25$V, $T_j = 25\,°C$



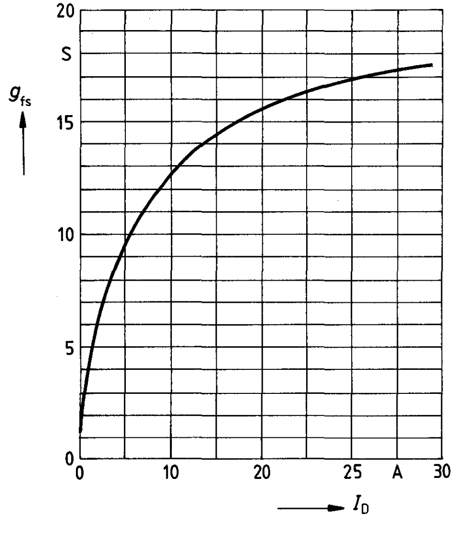
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



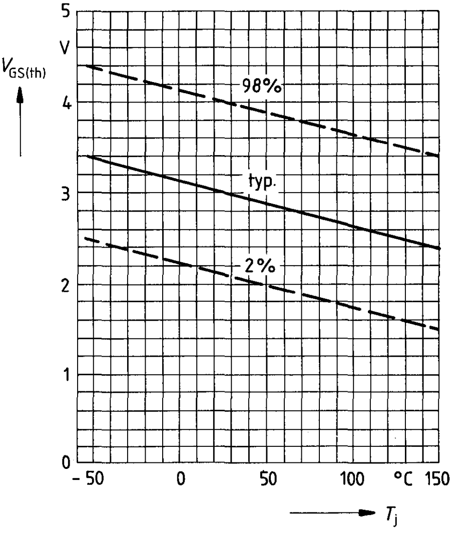
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 11A$, $V_{GS} = 10V$
(spread)



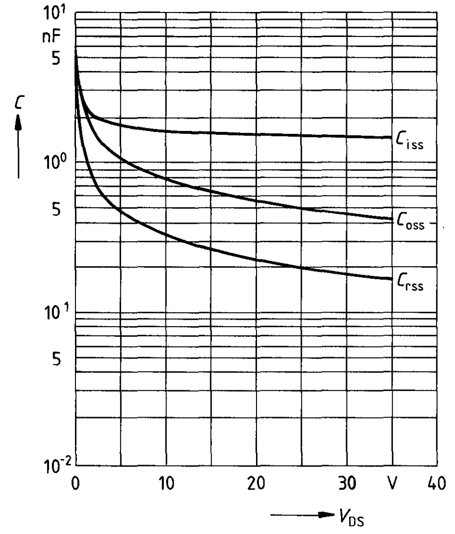
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



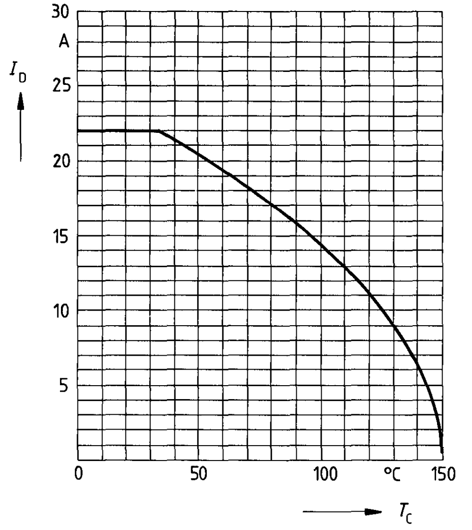
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



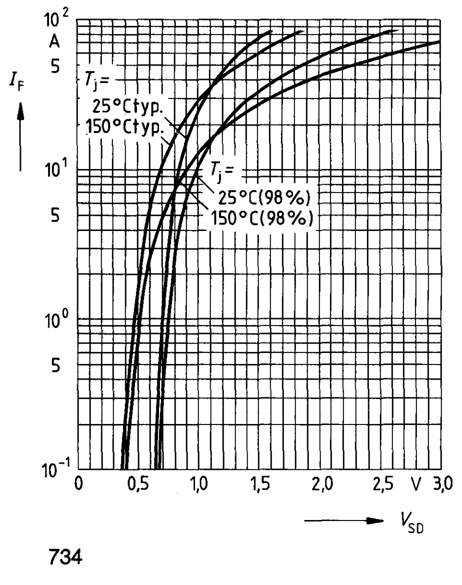
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1$MHz



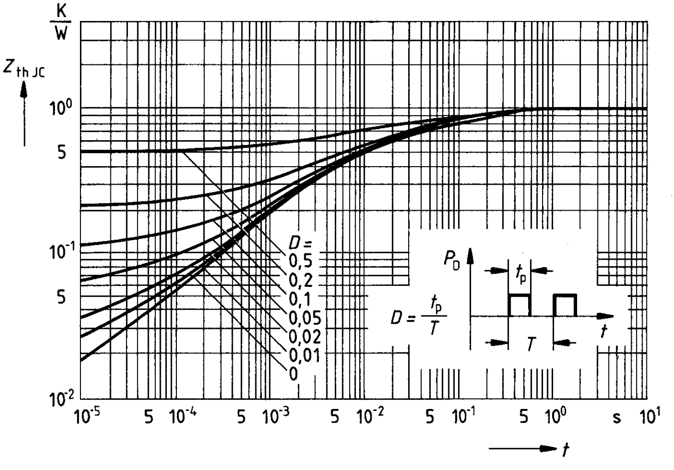
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10$V



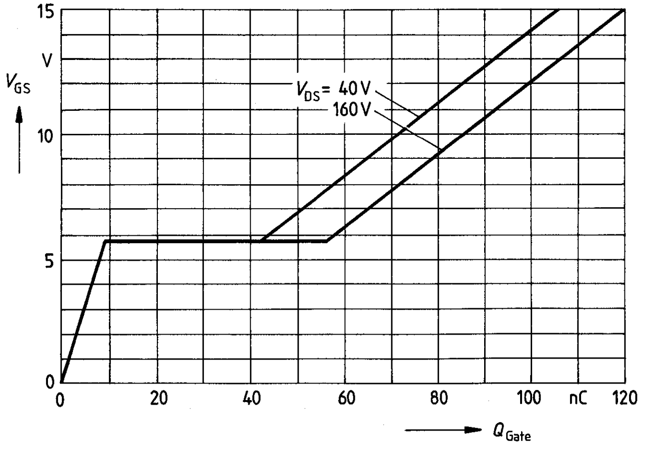
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

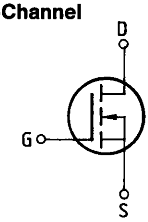


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 33A$



Main ratings

N-Channel

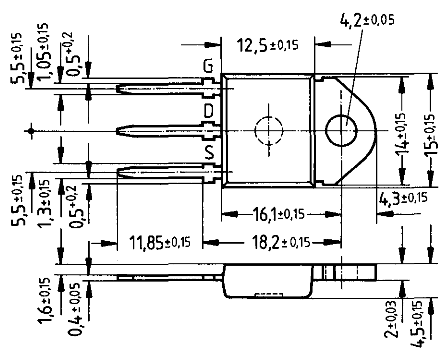


Drain-source voltage	V_{DS}	**= 400 V**
Continuous drain current	I_D	**= 11,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,4 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 351	C67078-A3103-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	11,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	46	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

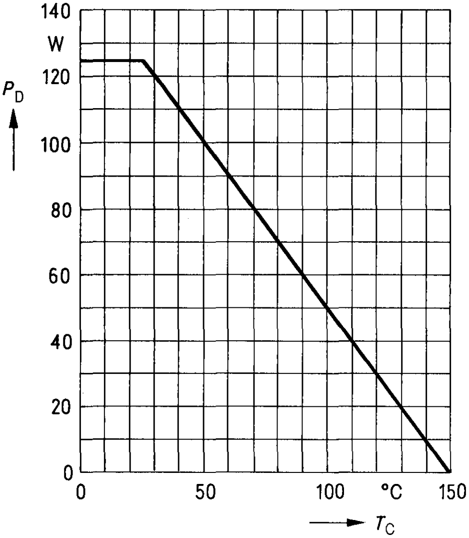
 S Preferred Type

Electrical characteristics

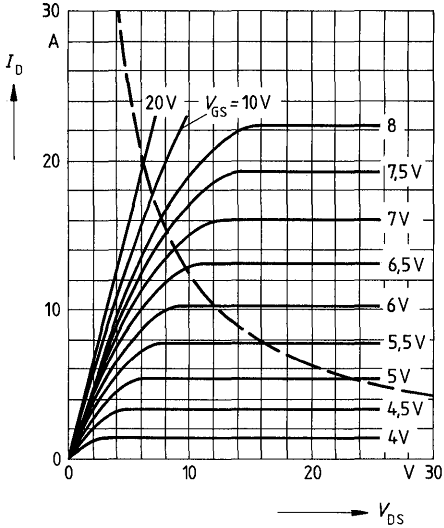
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,35	0,4	Ω	V_{GS} = 10V I_D = 5,5A
Dynamic ratings						
Forward transconductance	g_{fs}	3,3	4,5	–	S	V_{DS} = 25V I_D = 5,5A
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	300	500	pF	
Reverse transfer capacitance	C_{rss}	–	120	200		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	11,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	46		
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1,0	–	µs	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	10	–	µC	

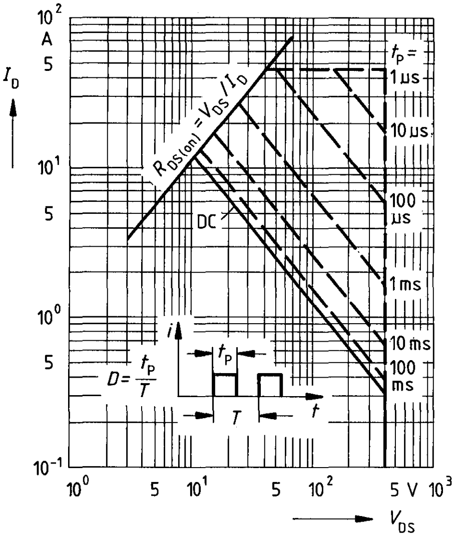
Power dissipation $P_D = f(T_C)$



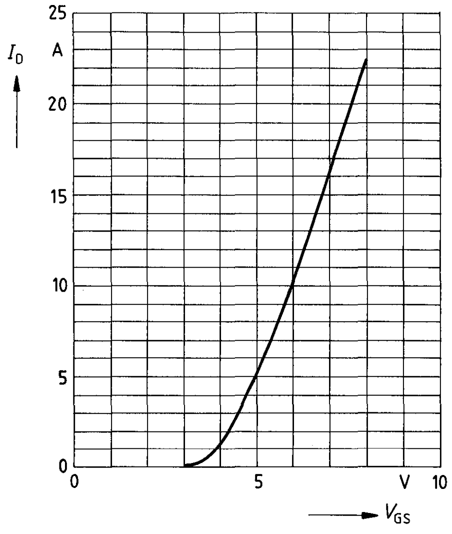
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



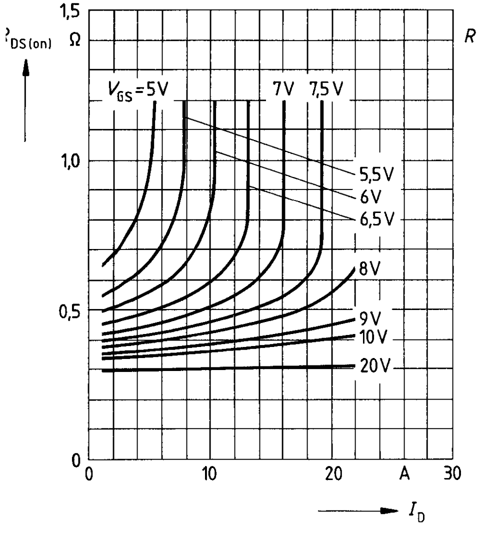
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



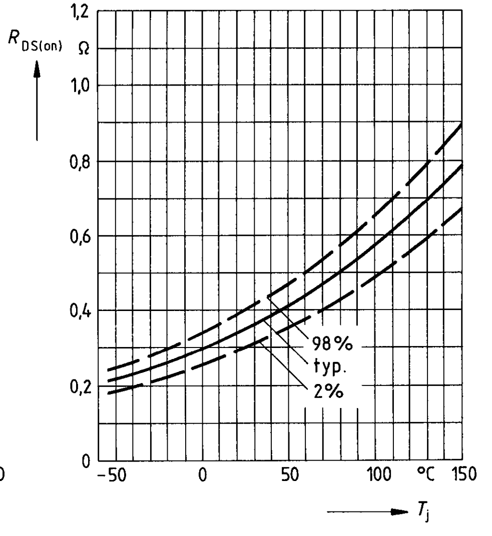
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



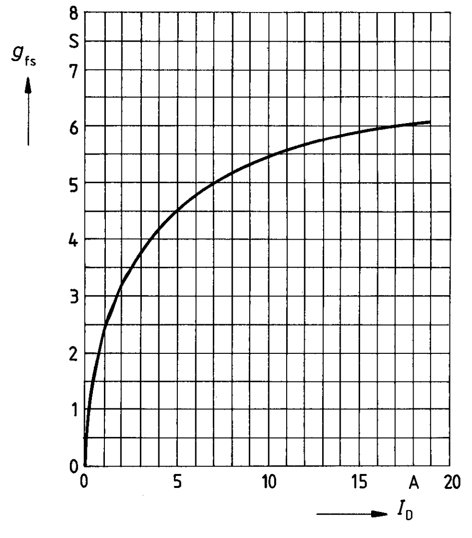
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



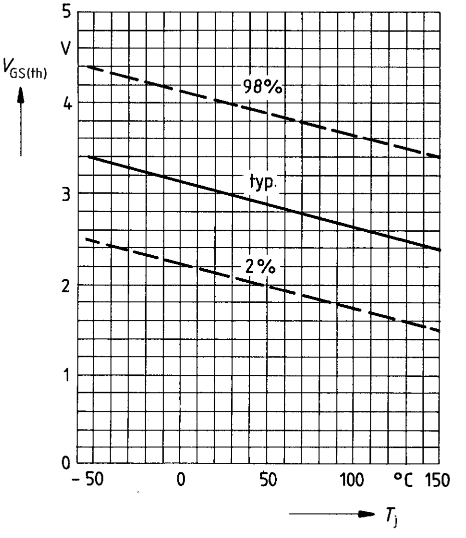
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 5,5A, V_{GS} = 10V
(spread)



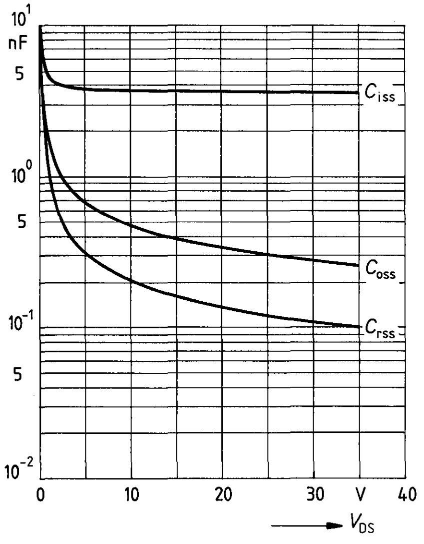
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



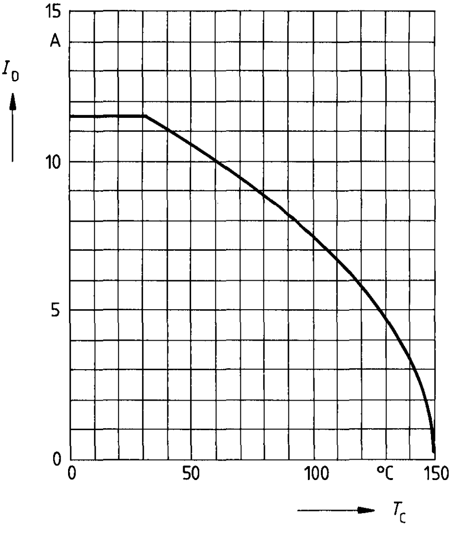
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



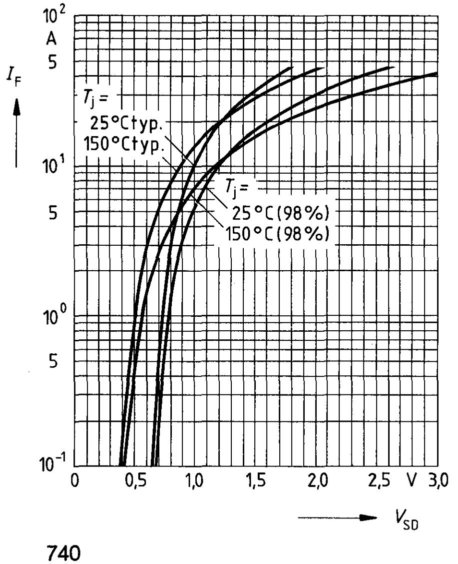
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



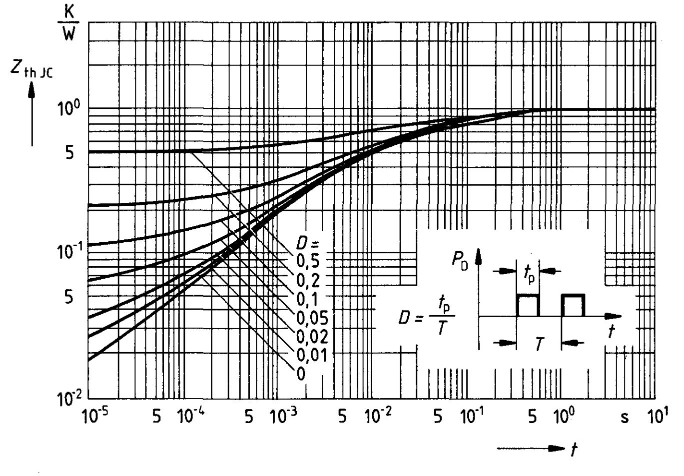
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



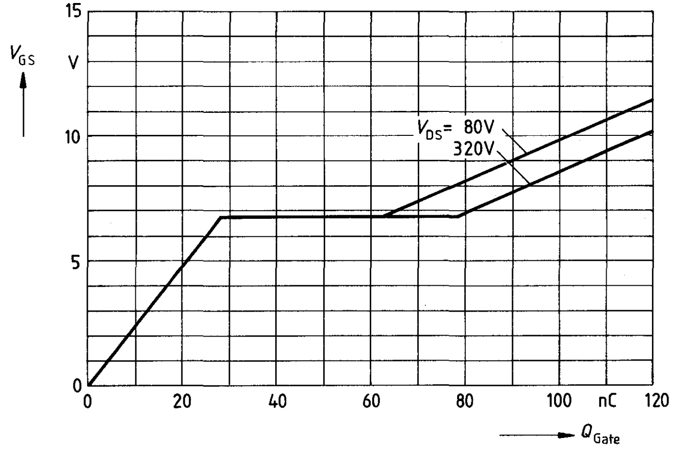
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu\text{s}$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



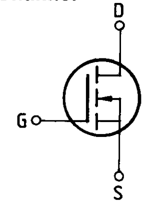
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 17{,}3A$



Main ratings

Drain-source voltage V_{DS} **= 500 V**
Continuous drain current I_D **= 9,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,6 Ω**

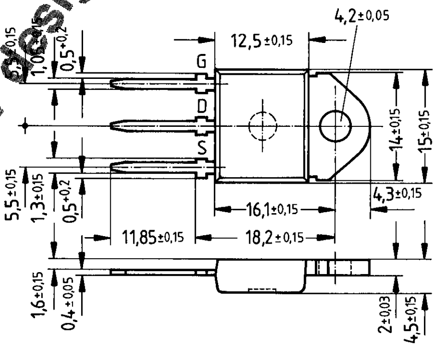
N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 353	C67078-A3104-A2

Not for new design



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	9,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	38	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

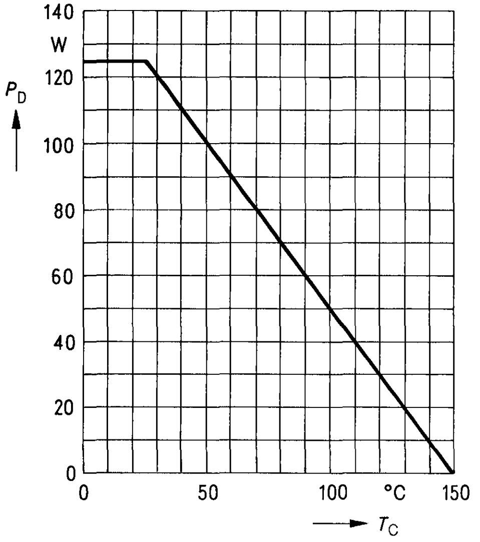
 S Preferred Type

Electrical characteristics

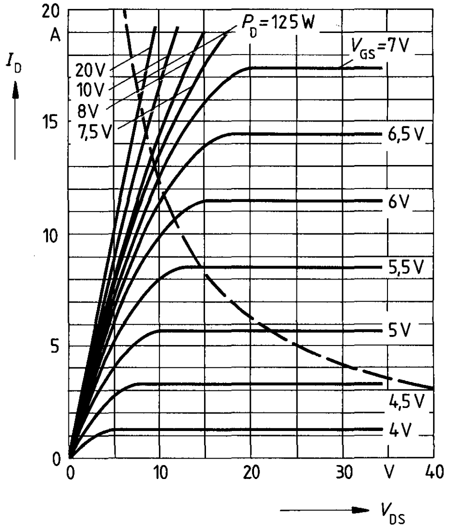
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,55	0,6	Ω	V_{GS} = 10V I_D = 5,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	5,0	–	S	V_{DS} = 25V I_D = 5,5A
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400	pF	
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	9,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	38		
Diode forward on-voltage	V_{SD}	–	1,3	1,7	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1,2	–	µs	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

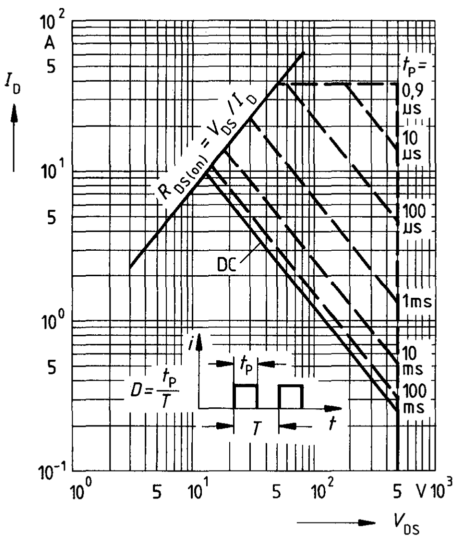
Power dissipation $P_D = f(T_C)$



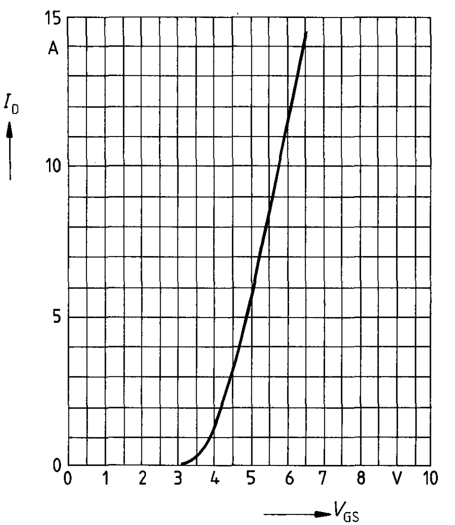
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



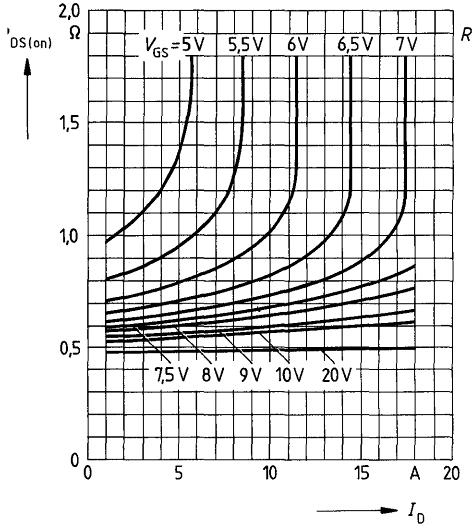
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



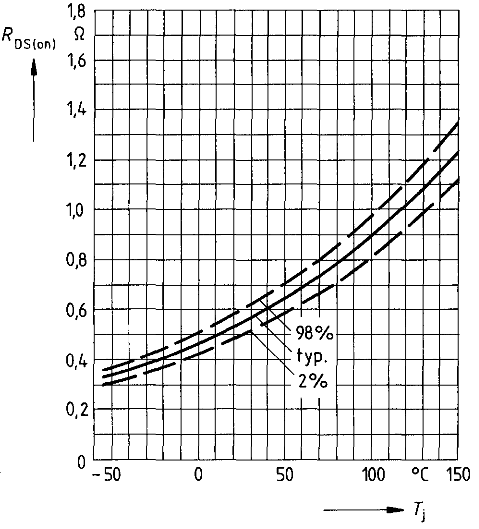
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



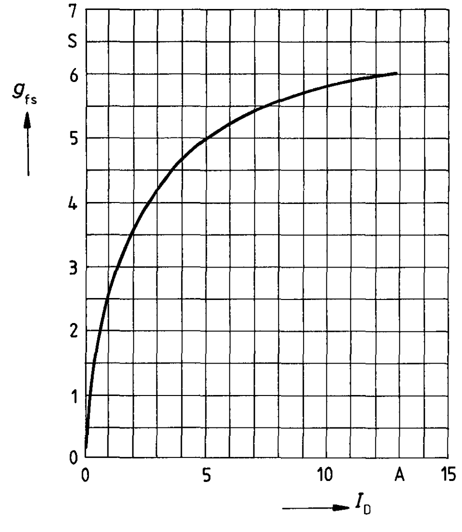
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



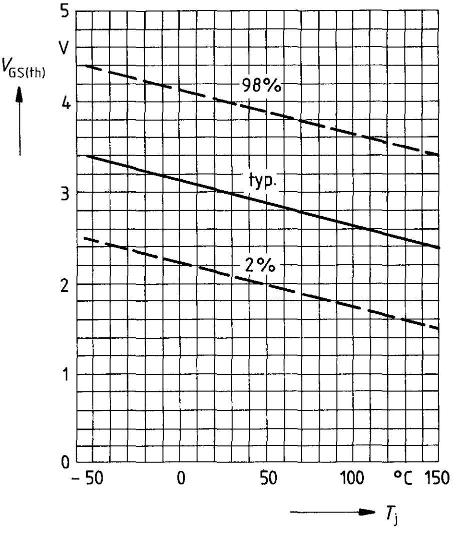
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 5{,}5A$, $V_{GS} = 10V$
(spread)



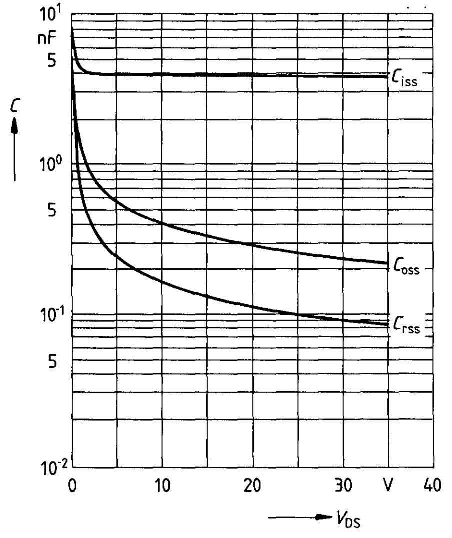
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



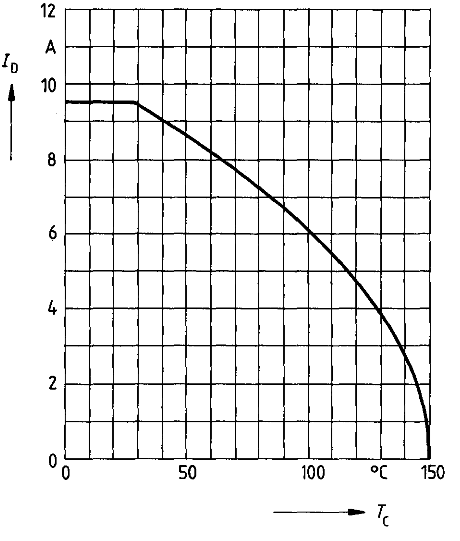
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



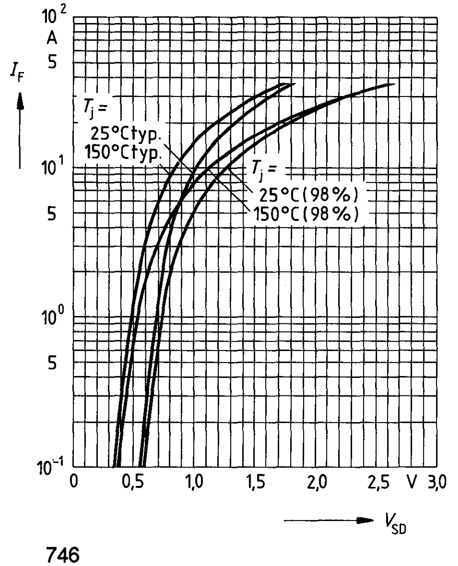
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



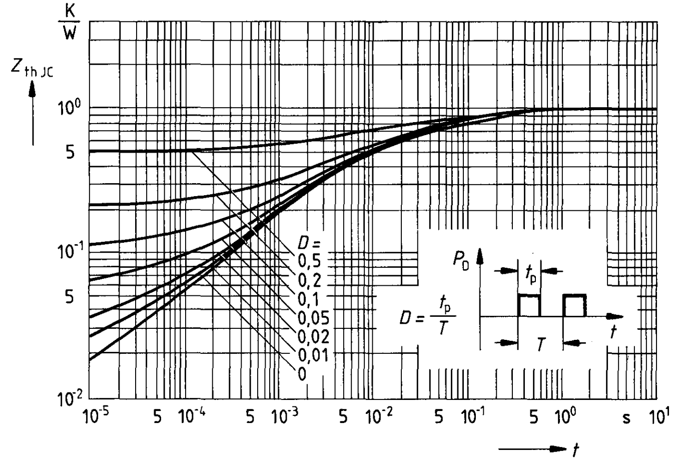
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



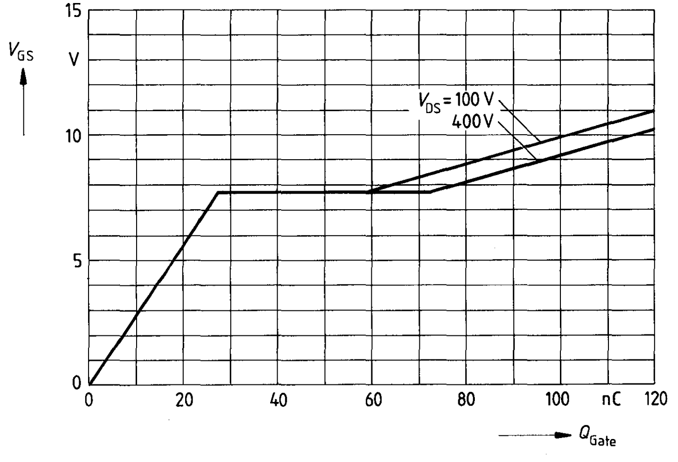
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p/T$

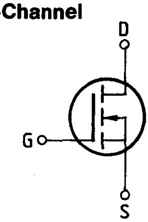


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14{,}4A$



Main ratings

N-Channel



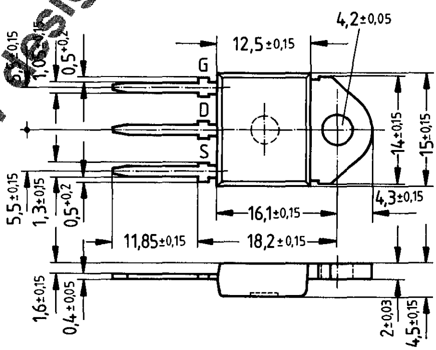
Drain-source voltage	V_{DS}	**= 500 V**
Continuous drain current	I_D	**= 8 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,8 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or TO 218 AA (TOP 3) in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 4,5 g

Type	Ordering code
Ⓢ BUZ 354	C67078-A3106-A2

Not for new design



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	8	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	32	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

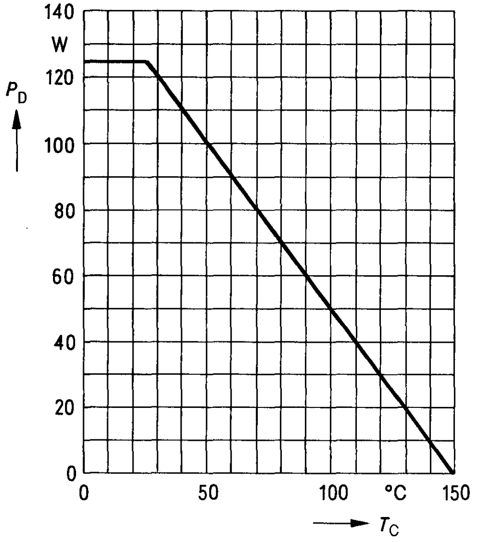
 Ⓢ Preferred Type

Electrical characteristics

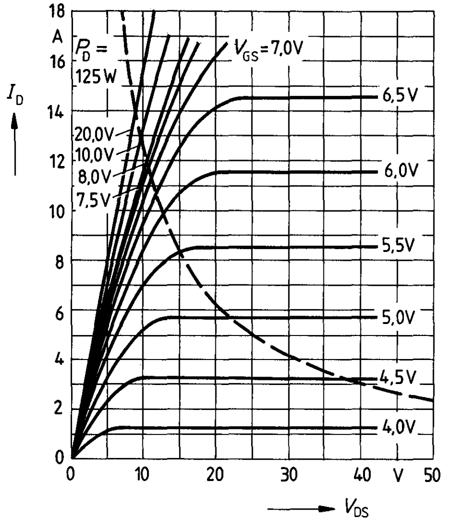
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,7	0,8	Ω	V_{GS} = 10V I_D = 5,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	5,0	–	S	V_{DS} = 25V I_D = 5,5A
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400	pF	
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	8,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	32		
Diode forward on-voltage	V_{SD}	–	1,3	1,6	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1200	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	12	–	µC	

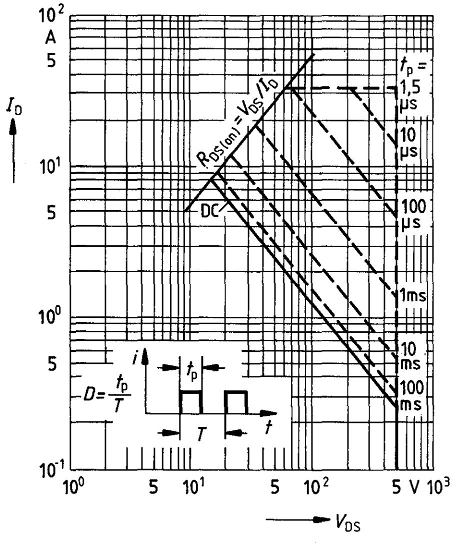
Power dissipation $P_D = f(T_C)$



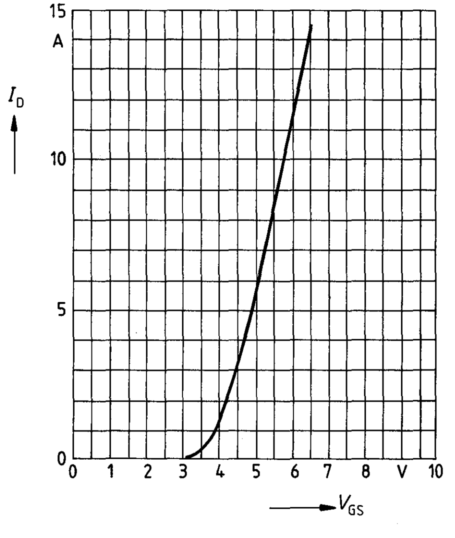
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25°C$



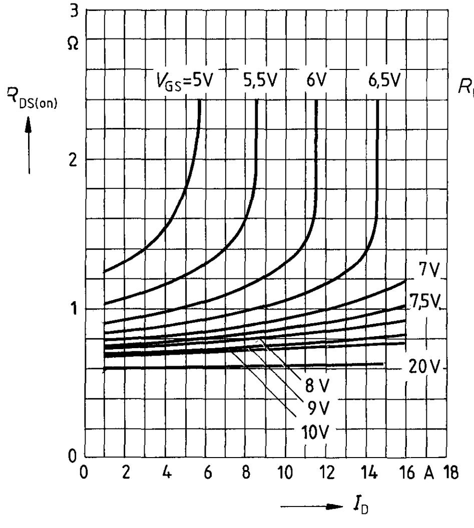
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25°C$



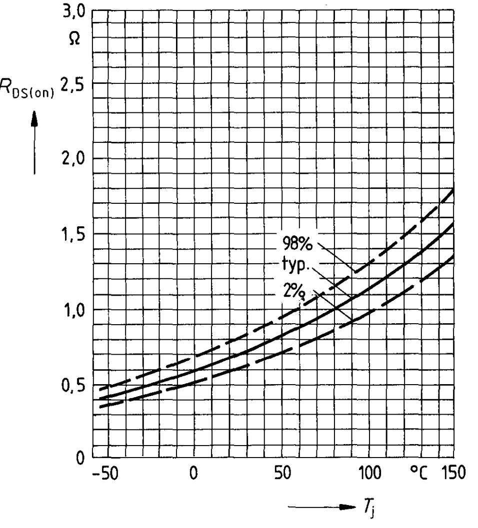
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25°C$



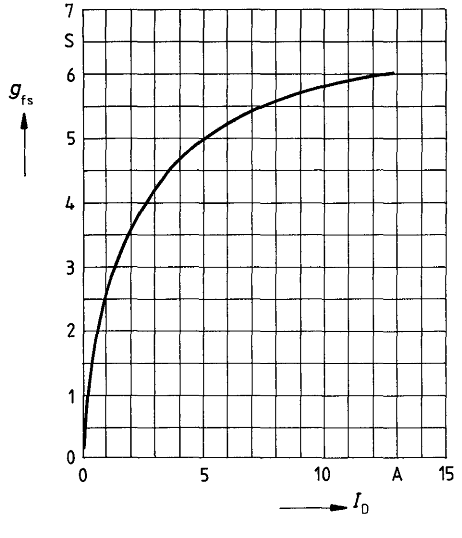
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



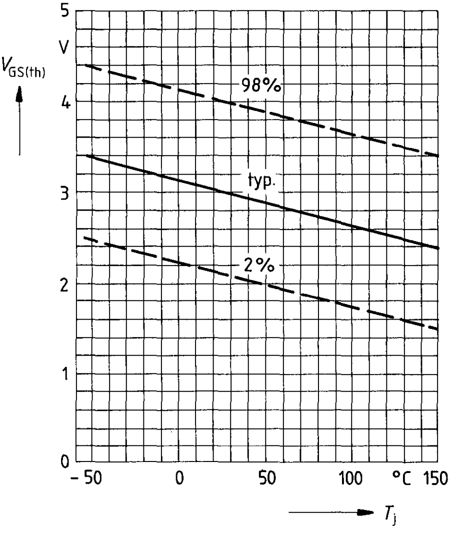
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 5{,}5A$, $V_{GS} = 10V$
(spread)



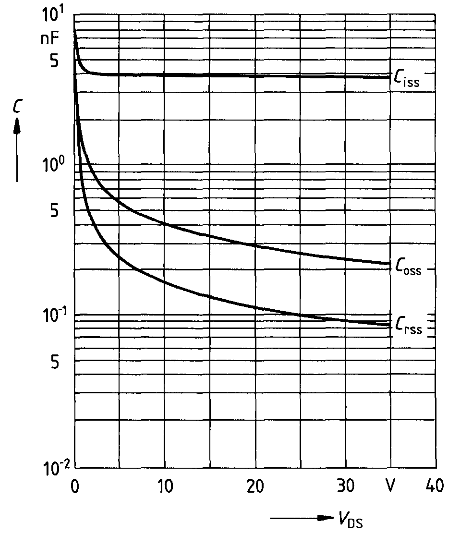
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



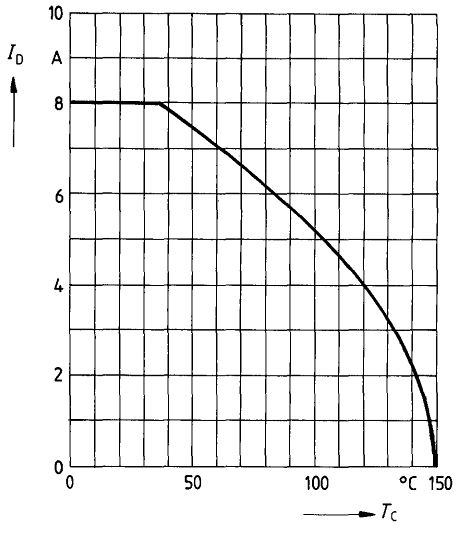
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



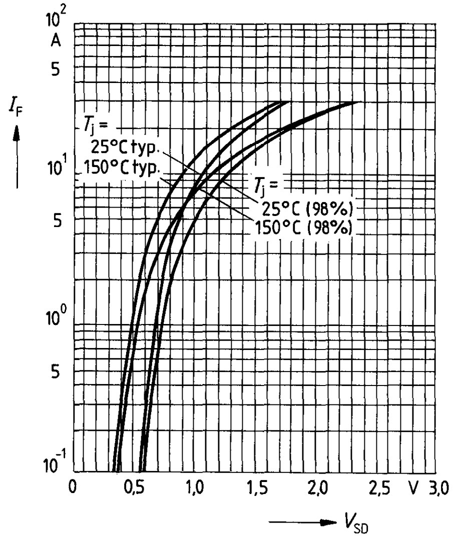
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



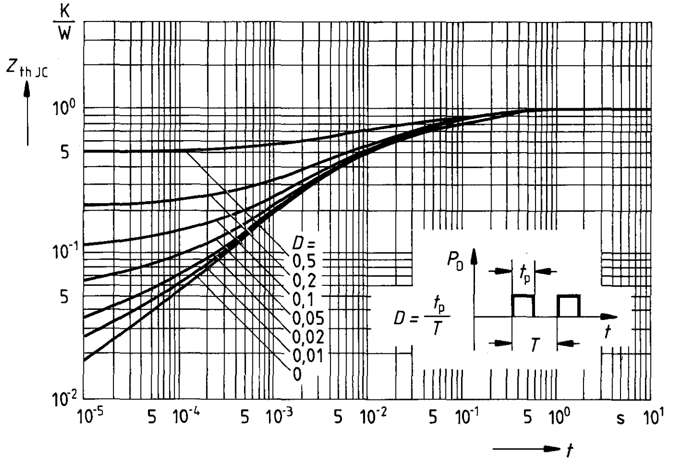
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



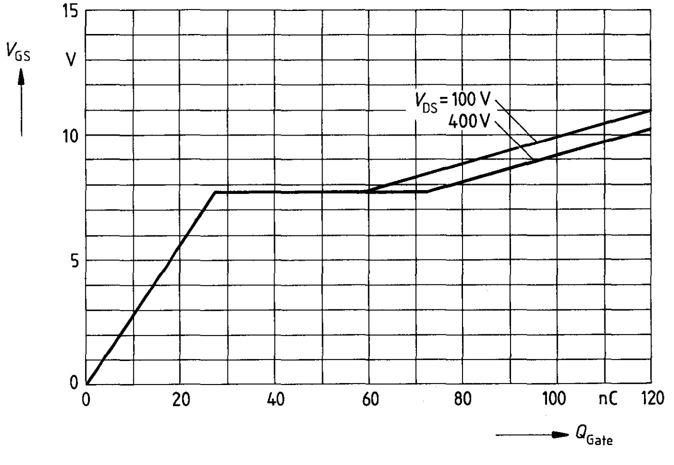
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



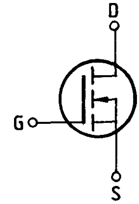
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 14{,}4A$



Main ratings

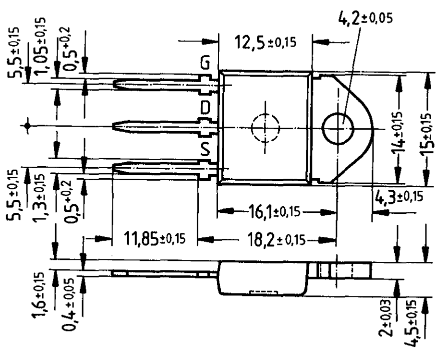
Drain-source voltage V_{DS} = **800 V**
Continuous drain current I_D = **6,0 A**
Drain-source on-resistance $R_{DS(on)}$ = **1,5 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 355	C67078-A3107-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	6	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	24	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage	T_j			
temperature range	T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

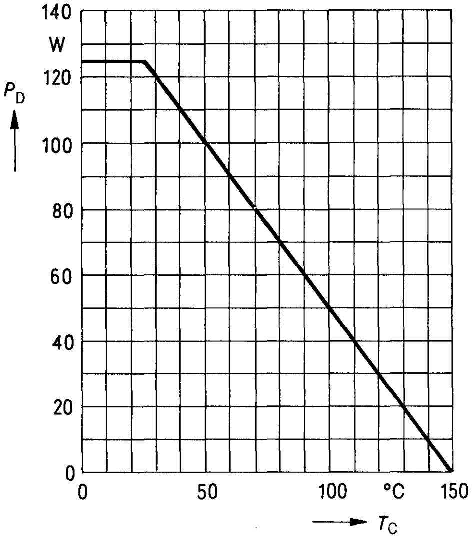
 S Preferred Type

Electrical characteristics

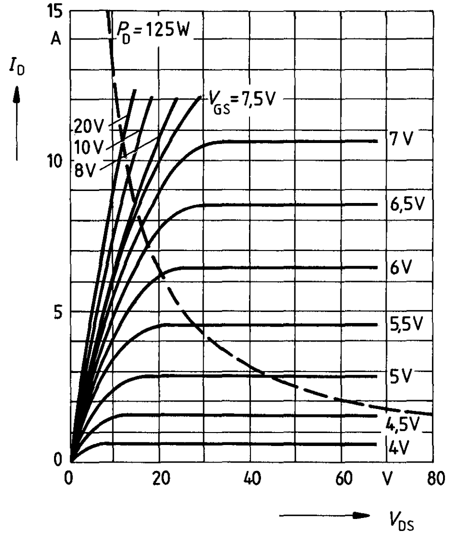
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,3	1,5	Ω	V_{GS} = 10V I_D = 3,8A
Dynamic ratings						
Forward transconductance	g_{fs}	1,8	3,3	–	S	V_{DS} = 25V I_D = 3,8A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	200	350	pF	
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,6A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	6,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	24		
Diode forward on-voltage	V_{SD}	–	1,1	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1,8	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	25	–	µC	

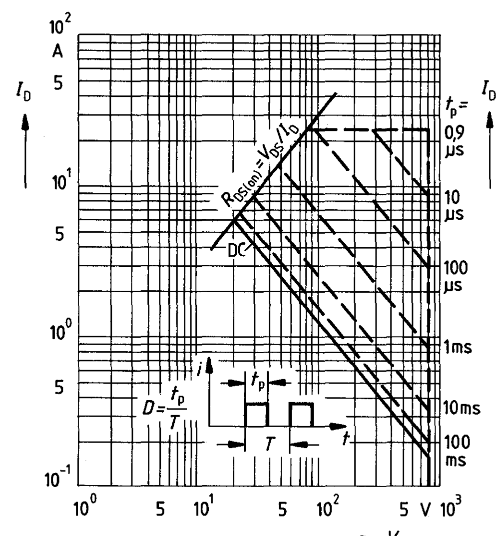
Power dissipation $P_D = f(T_C)$



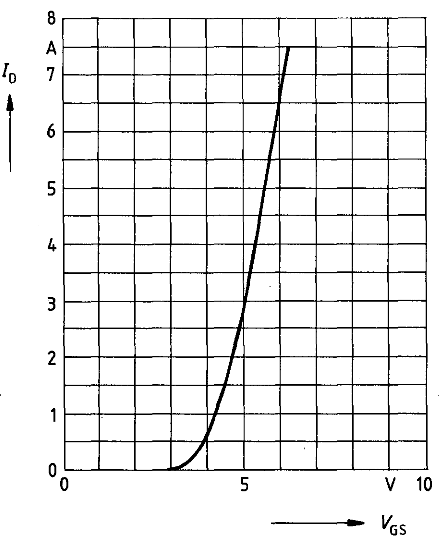
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



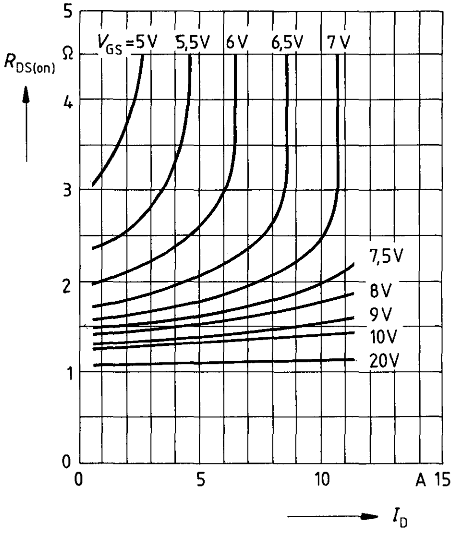
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



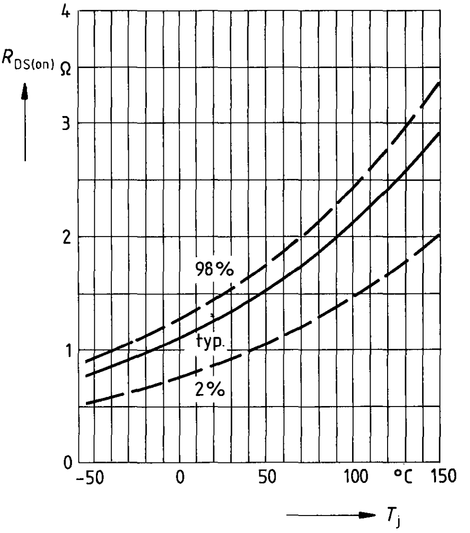
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



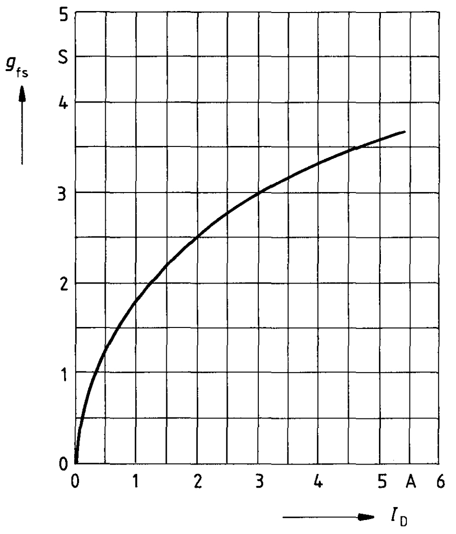
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



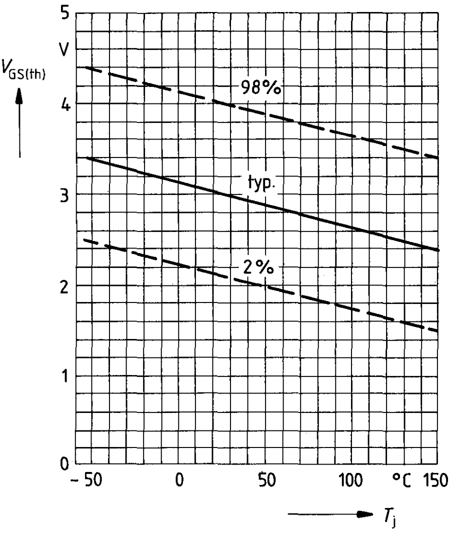
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 4,2A, V_{GS} = 10V
(spread)



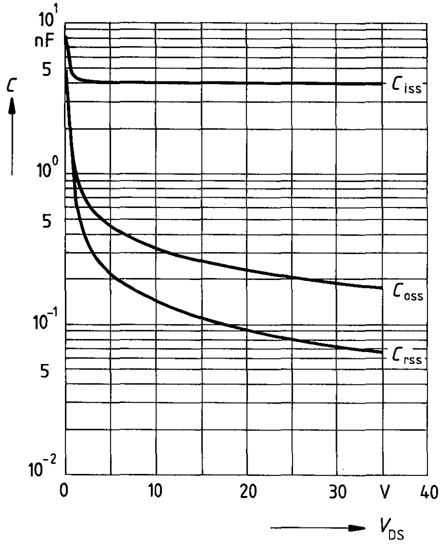
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



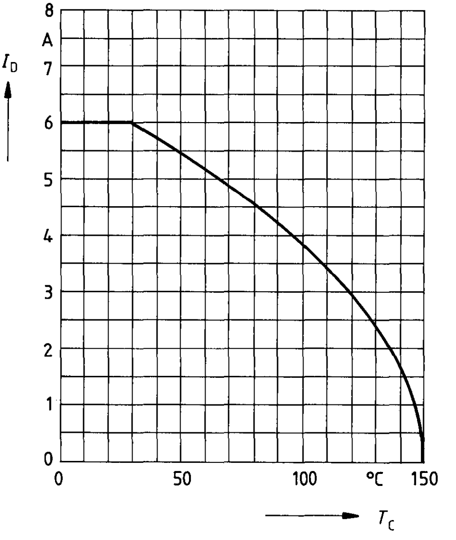
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



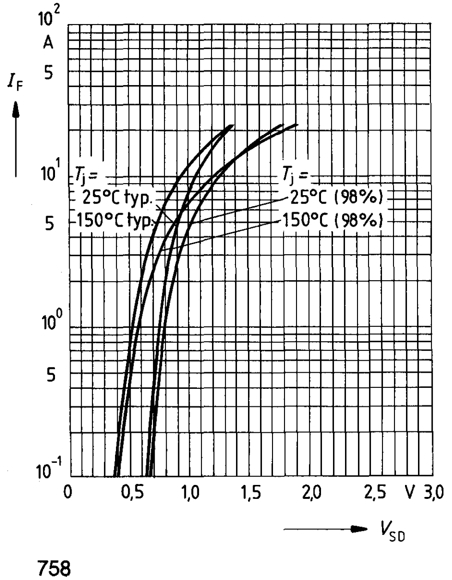
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



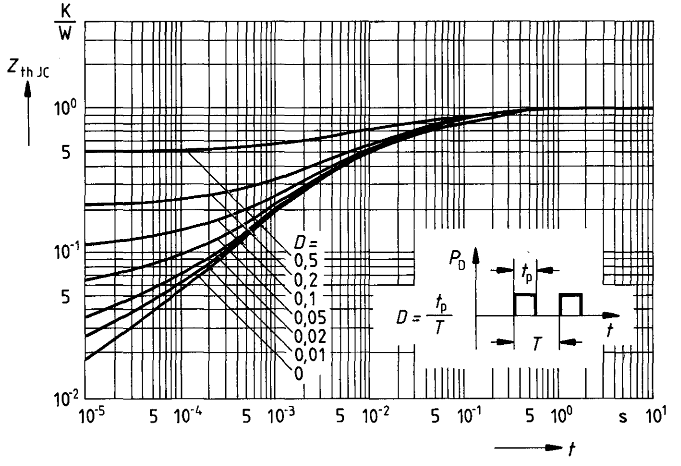
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



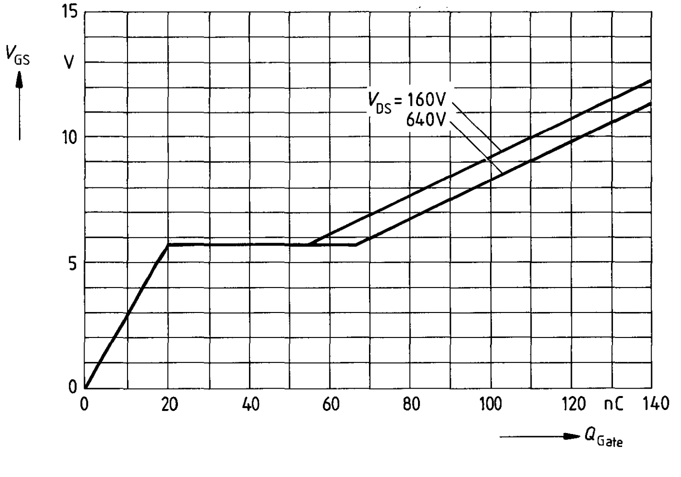
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



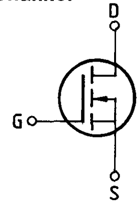
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 9A$



Main ratings

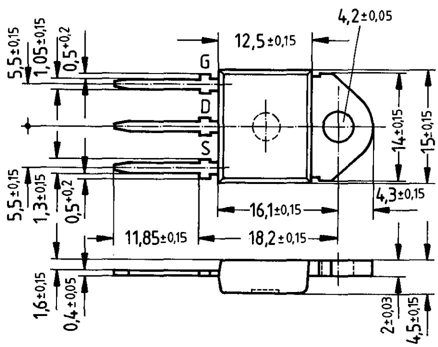
Drain-source voltage V_{DS} **= 800 V**
Continuous drain current I_D **= 5,0 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 356	C67078-A3108-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,0	A	T_C = 35 °C
Pulsed drain current	I_{Dpuls}	21	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 … + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤ 45	K/W	

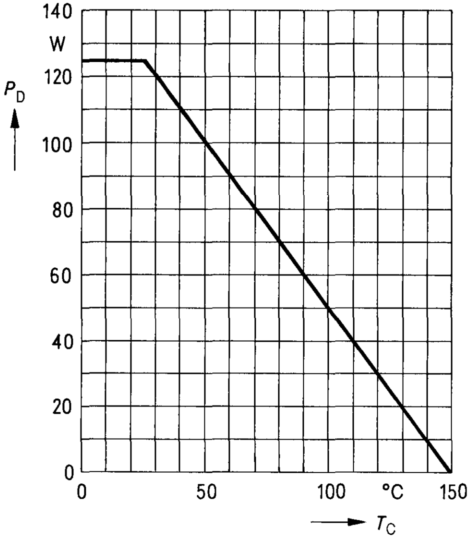
 S Preferred Type

Electrical characteristics

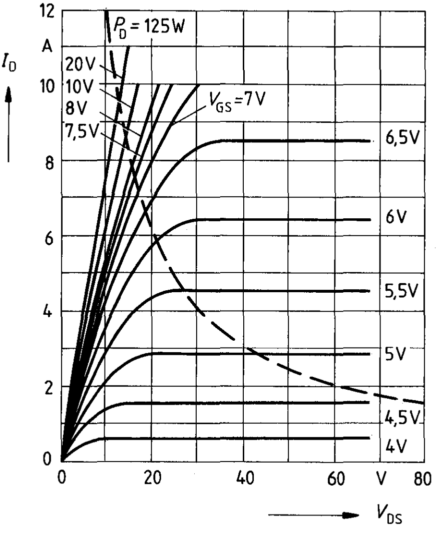
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	1,6	2,0	Ω	V_{GS} = 10V I_D = 3,8A
Dynamic ratings						
Forward transconductance	g_{fs}	1,8	3,3	–	S	V_{DS} = 25V I_D = 3,8A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	200	350	pF	
Reverse transfer capacitance	C_{rss}	–	80	140		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	20		
Diode forward on-voltage	V_{SD}	–	1,0	1,3	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	1,8	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	25	–	µC	

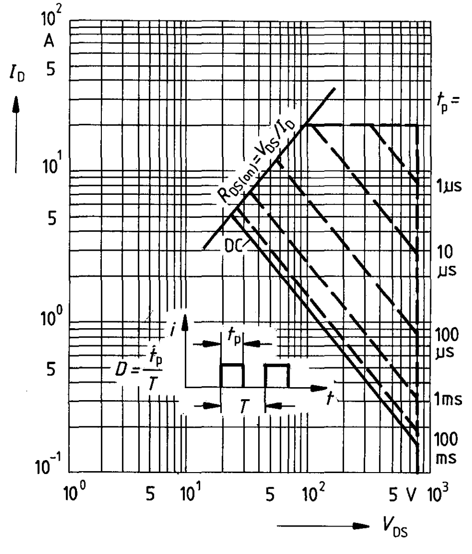
Power dissipation $P_D = f(T_C)$



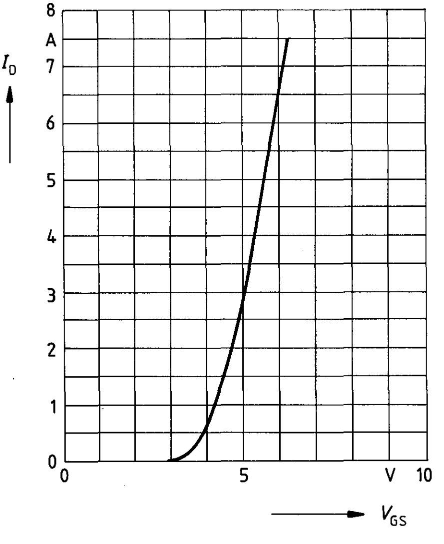
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



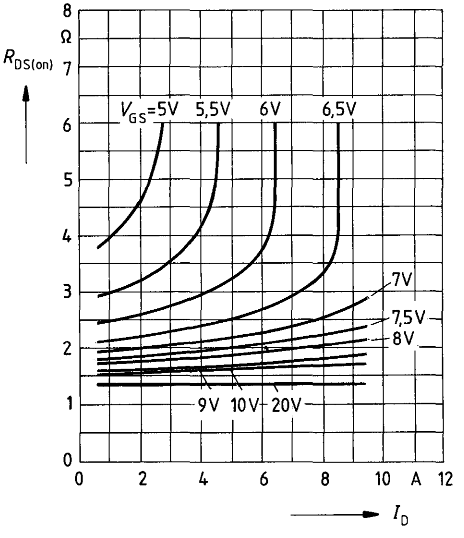
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



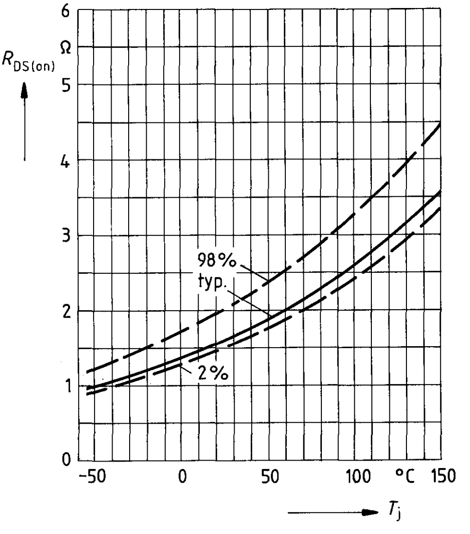
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



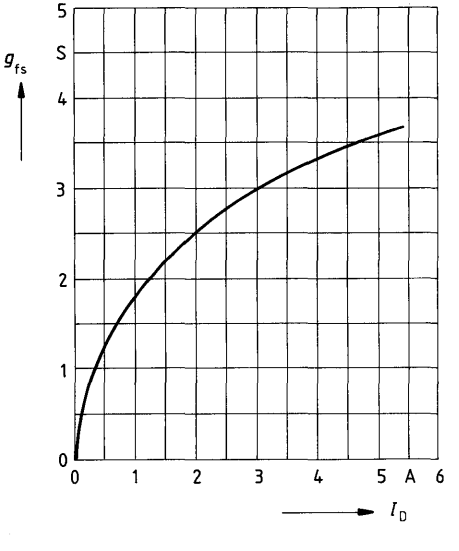
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



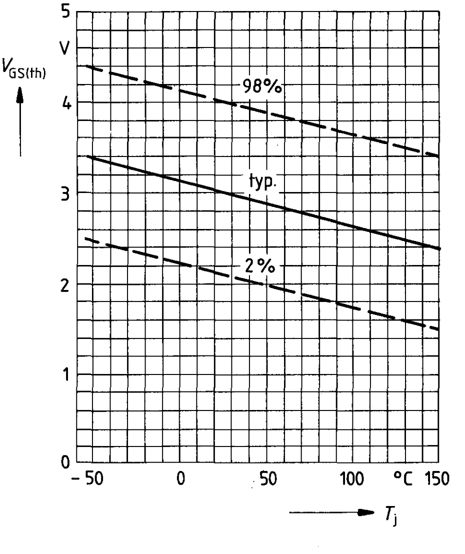
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 3,8A, V_{GS} = 10V
(spread)



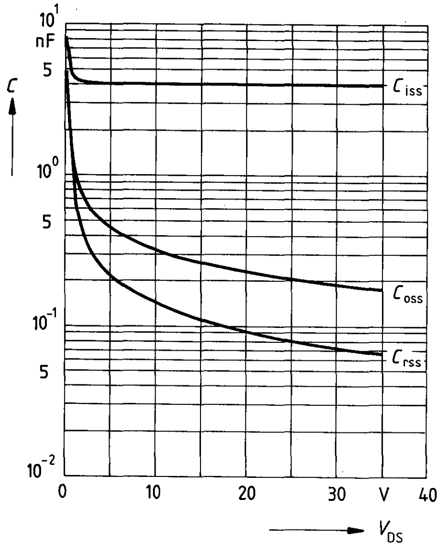
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



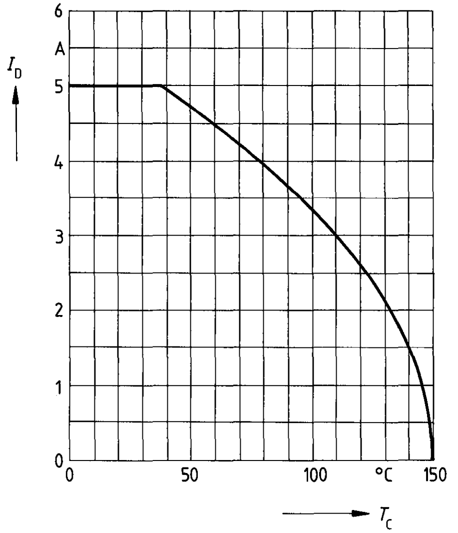
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



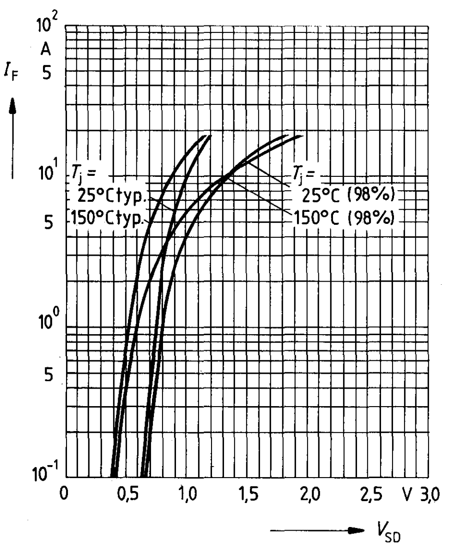
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



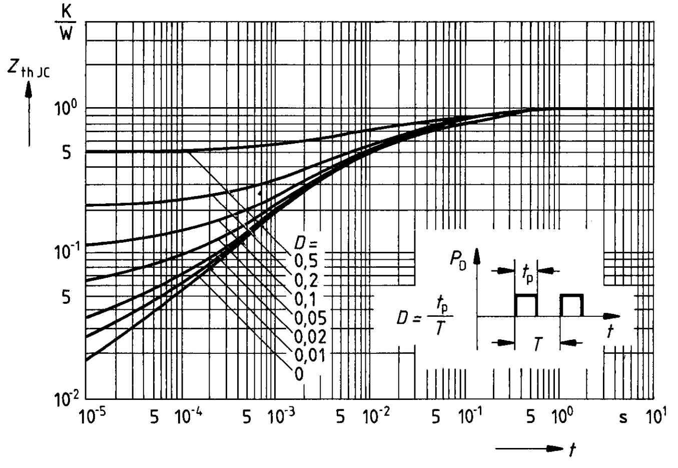
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



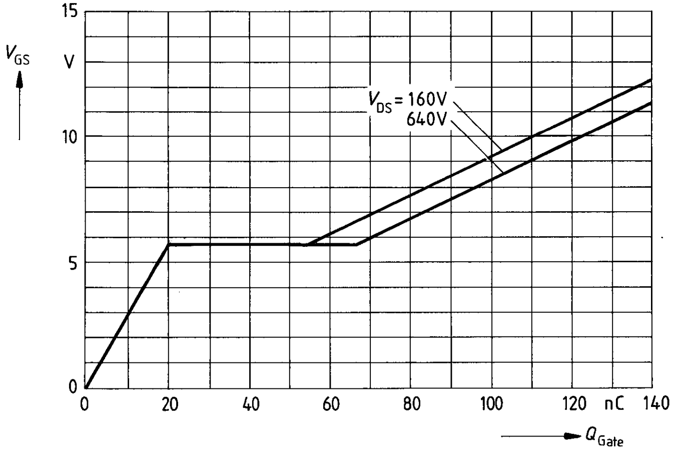
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



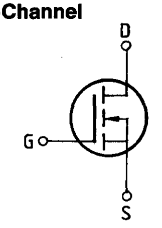
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 9A$



Main ratings

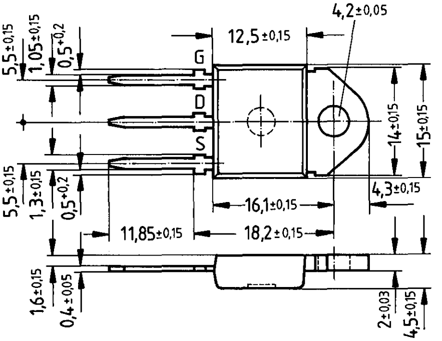
Drain-source voltage V_{DS} **= 1000 V**
Continuous drain current I_D **= 5,0 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,0 Ω**

N-Channel



Description SIPMOS, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 357	C67078-A3110-A2



Dimensions in mm

Maximum ratings

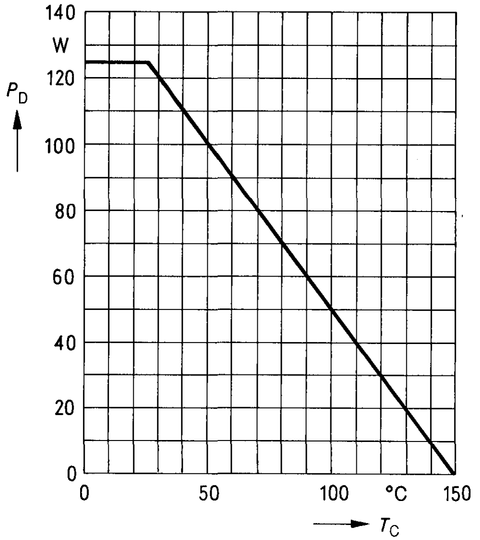
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,0	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	20	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤1,0	K/W	
Chip – ambient	$R_{th JA}$	≤45	K/W	

 S Preferred Type

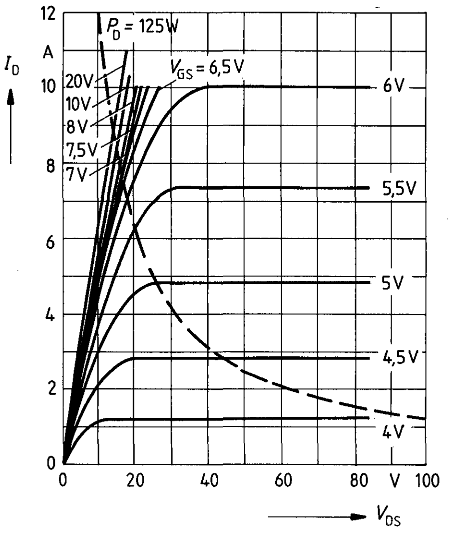
Electrical characteristics
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,7	2,0	Ω	V_{GS} = 10V I_D = 3,2A
Dynamic ratings						
Forward transconductance	g_{fs}	1,4	3,8	–	S	V_{DS} = 25V I_D = 3,2A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	300	pF	
Reverse transfer capacitance	C_{rss}	–	70	120		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	5,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	20		
Diode forward on-voltage	V_{SD}	–	1,0	1,3	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2,0	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	30	–	µC	

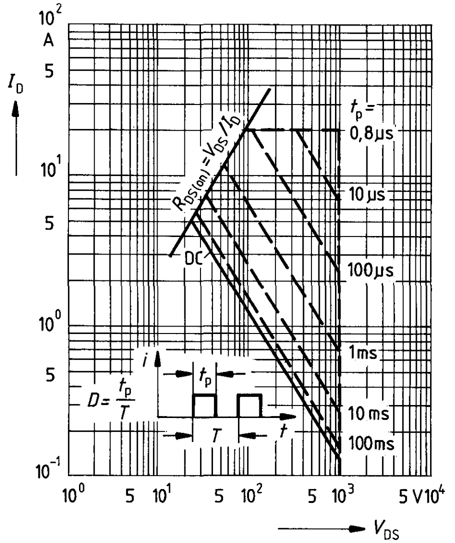
Power dissipation $P_D = f(T_C)$



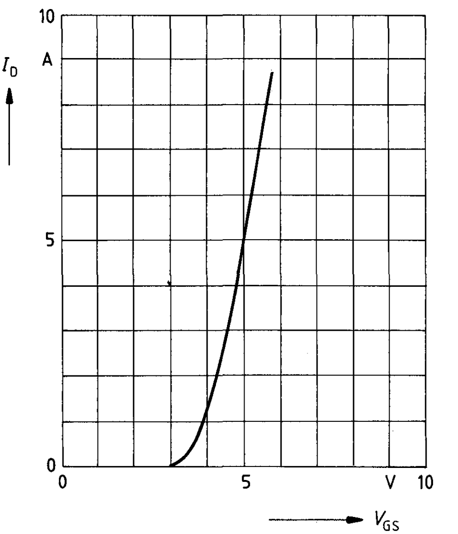
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



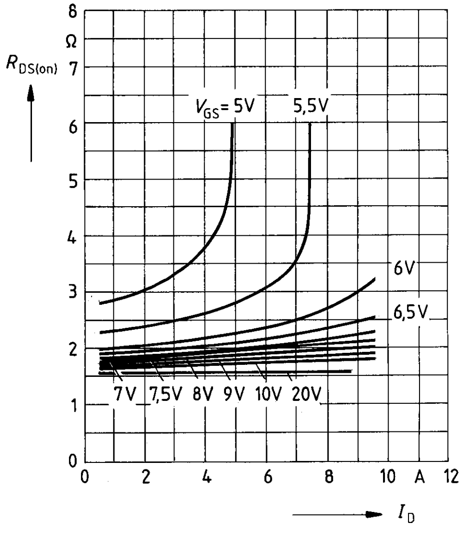
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



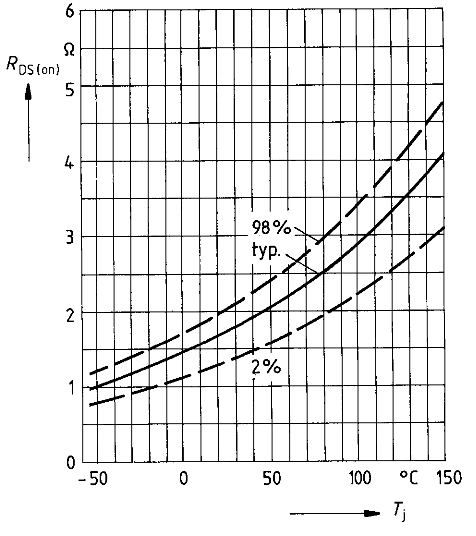
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



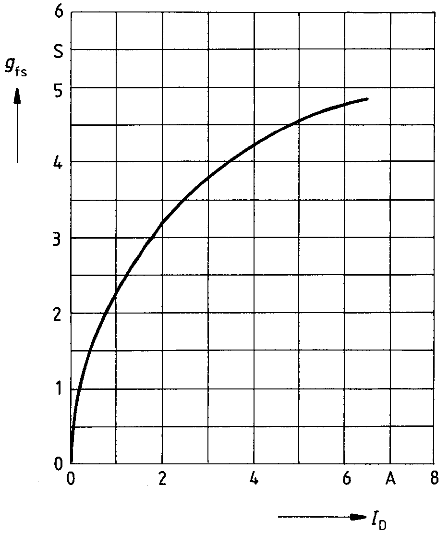
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



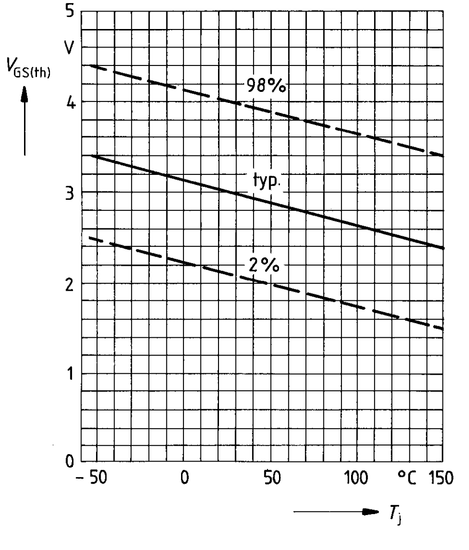
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 3,2A, V_{GS} = 10V
(spread)



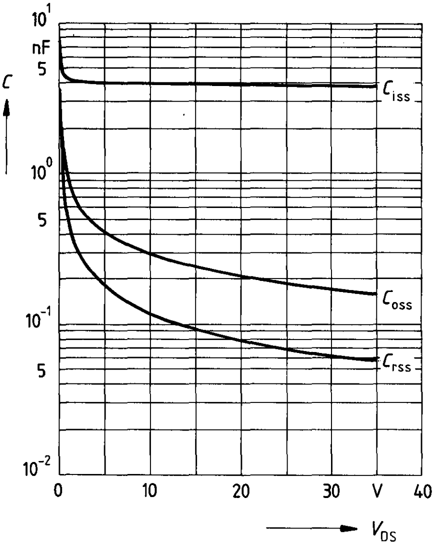
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



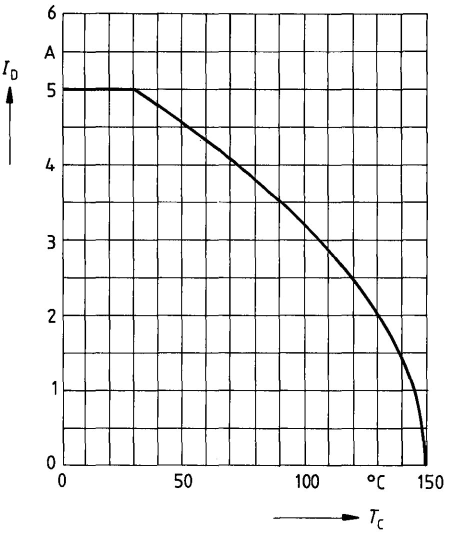
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



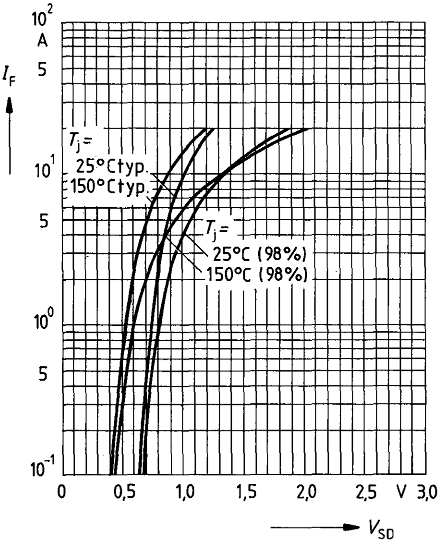
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



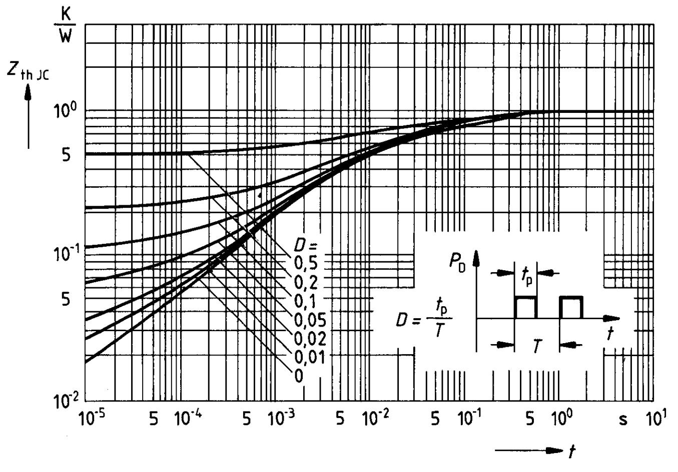
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



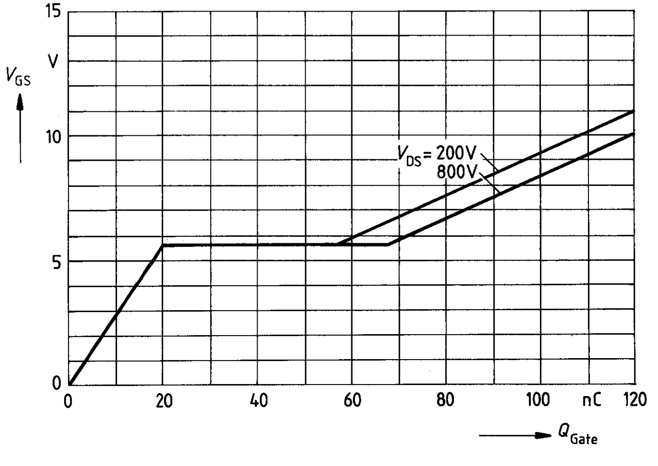
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

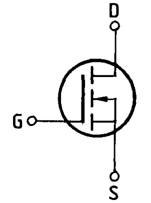


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 8A$



Main ratings

N-Channel

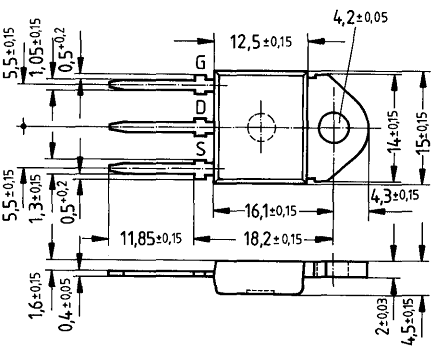


Drain-source voltage	V_{DS}	**= 1000 V**
Continuous drain current	I_D	**= 4,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 2,6 Ω**

Description SIPMOS, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
S BUZ 358	C67078-A3111-A2



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	18	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

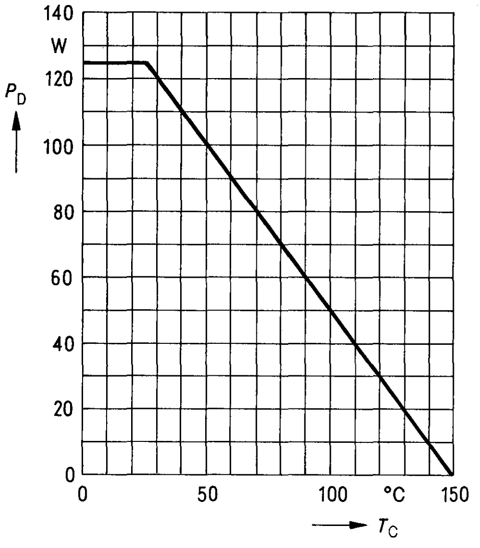
S Preferred Type

Electrical characteristics

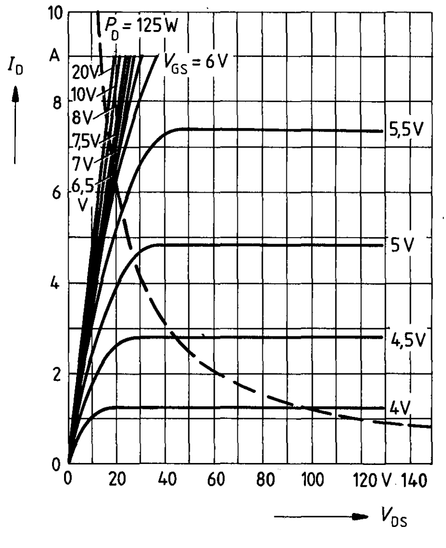
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	2,3	2,6	Ω	V_{GS} = 10V I_D = 3,2A
Dynamic ratings						
Forward transconductance	g_{fs}	1,4	3,8	–	S	V_{DS} = 25V I_D = 3,2A
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	180	300	pF	
Reverse transfer capacitance	C_{rss}	–	70	120		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,4A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	90	140		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Reverse diode						
Continuous reverse drain current	I_{DR}	–	–	4,5	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	18		
Diode forward on-voltage	V_{SD}	–	1,0	1,3	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	2,0	–	ns	T_j = 25 °C I_F = I_{DR} $d_{iF/dt}$ = 100A/µs V_R = 100V
Reverse recovery charge	Q_{rr}	–	30	–	µC	

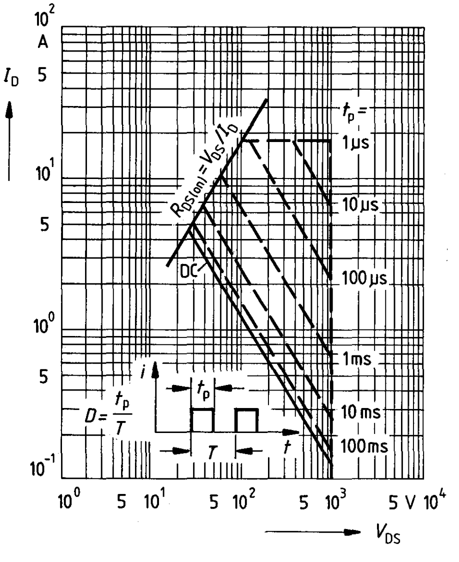
Power dissipation $P_D = f(T_C)$



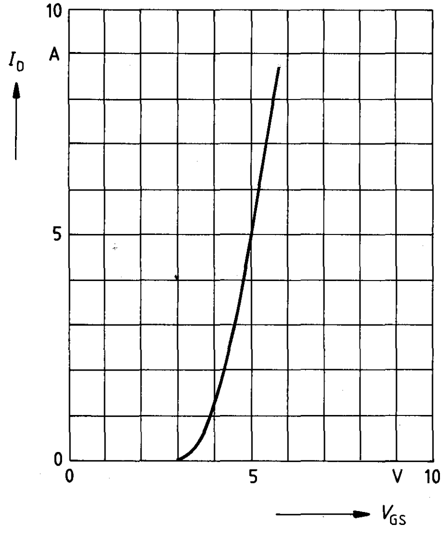
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



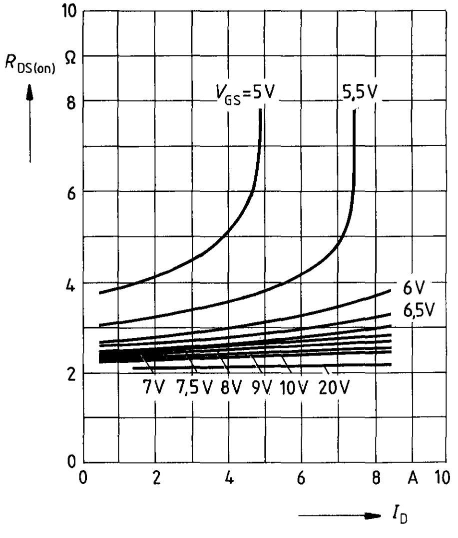
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



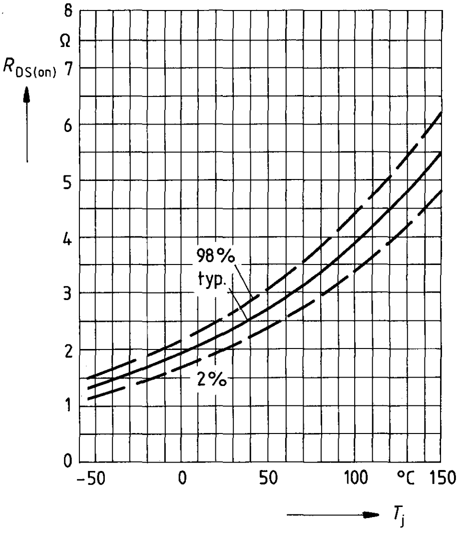
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\text{V}$, $T_j = 25\,°C$



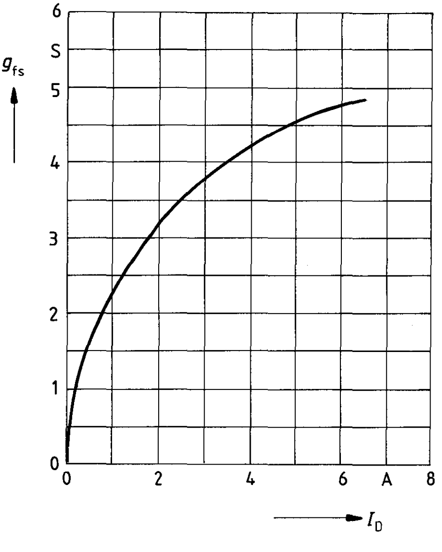
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; T_j = 25 °C



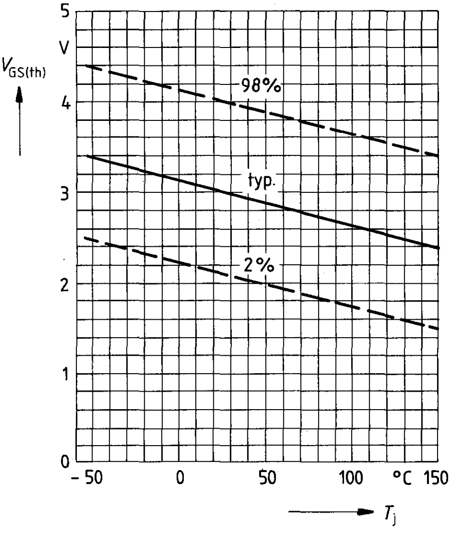
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 3,2A, V_{GS} = 10V
(spread)



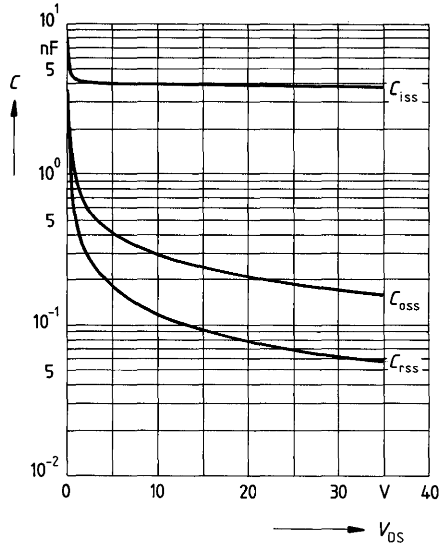
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, T_j = 25 °C



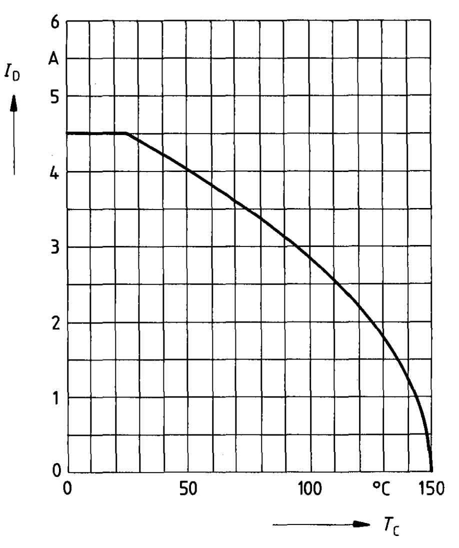
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



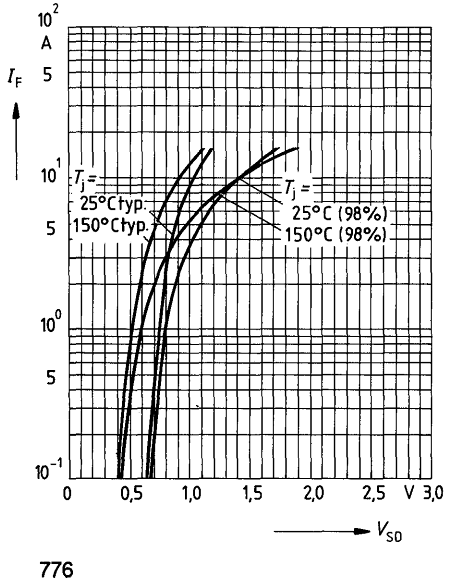
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



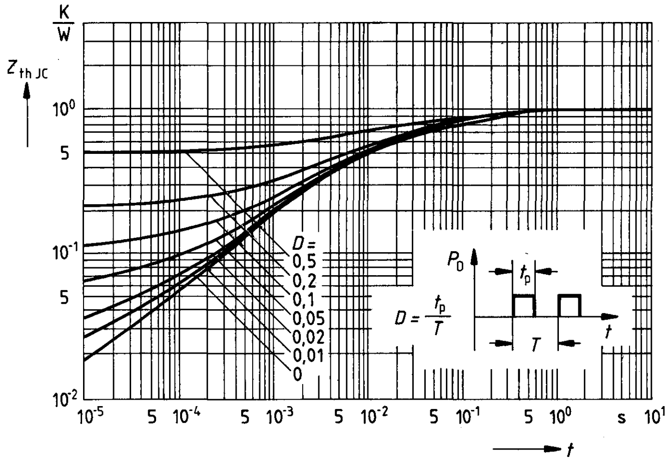
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



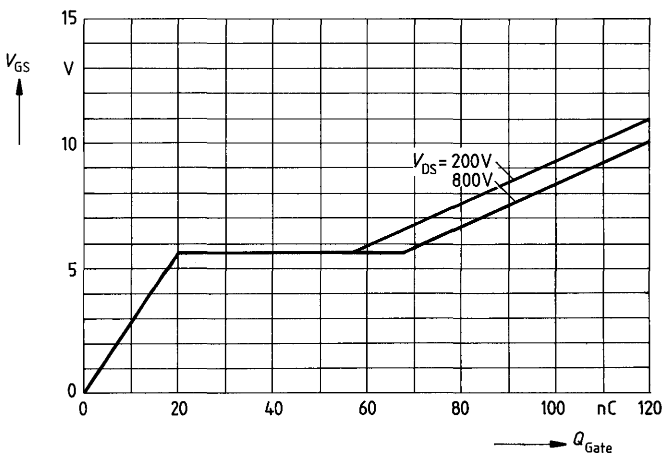
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

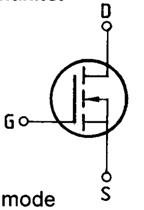


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 8A$



Main ratings

N-Channel

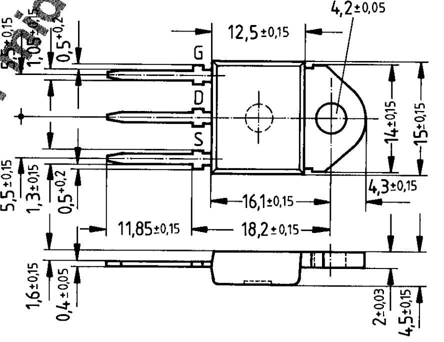


Drain-source voltage	V_{DS}	=	**800 V**
Continuous drain current	I_D	=	**3,6 A**
Drain-source on-resistance	$R_{DS(on)}$	=	**3,0 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 360	C67078-A3204-A2



Dimensions in mm

Maximum ratings

Description	**Symbols**	**Ratings**	**Units**	**Conditions**
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	3,6	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	14	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

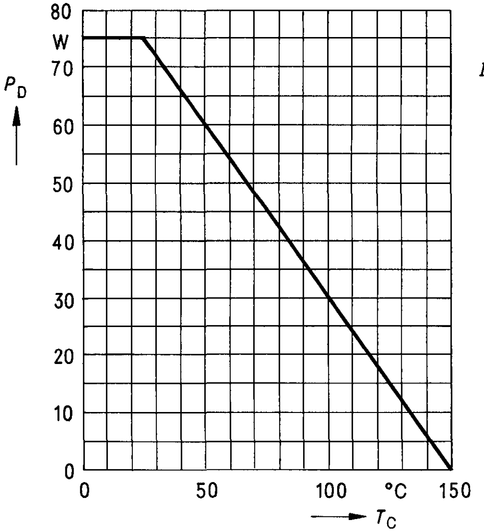
Chip – case	$R_{th\,JC}$	≤1,67	K/W
Chip – ambient	$R_{th\,JA}$	≤45	K/W

Electrical characteristics

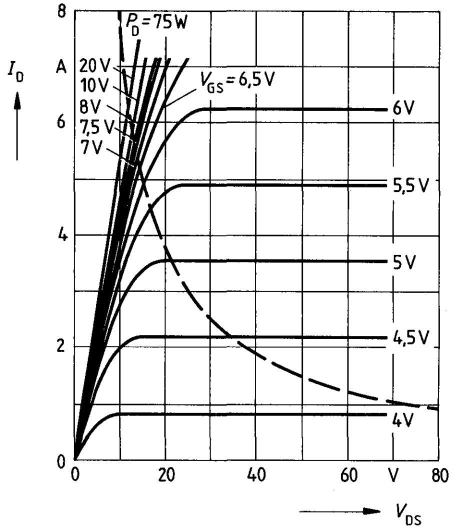
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	μA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS(on)}$	–	2,0	3,0	Ω	V_{GS} = 10V I_D = 2,3A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	2,4	–	S	V_{DS} = 25V I_D = 2,3A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	90	150	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d(on)} + t_r$)	$t_{d(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,3A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	50	60		
Turn-off time t_{off} ($t_{off} = t_{d(off)} + t_f$)	$t_{d(off)}$	–	100	140		
	t_f	–	60	80		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	3,6	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	14		
Diode forward on-voltage	V_{SD}	–	1,15	1,5	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; $I_F = I_{DR}$, di_F/dt = 100A/μs, V_R = 100V
		–	220	300		= 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	μC	T_j = 25 °C
		–	2,6	5,0		= 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		= 150 °C

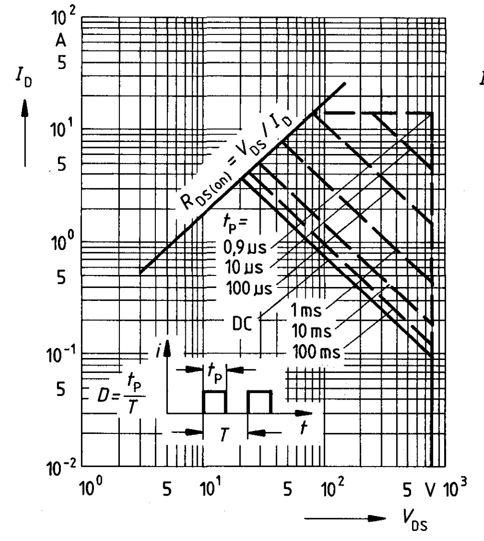
Power dissipation $P_D = f(T_C)$



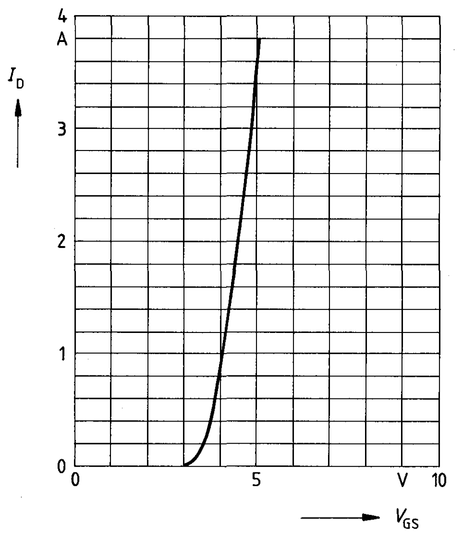
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25°C$



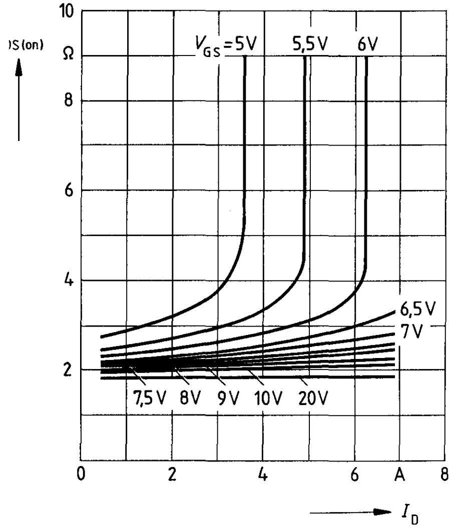
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25°C$



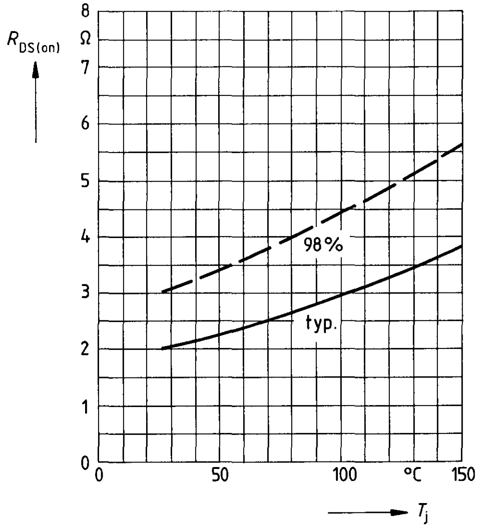
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25°C$



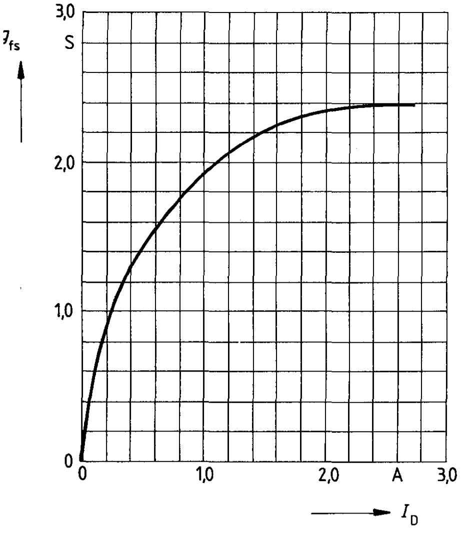
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



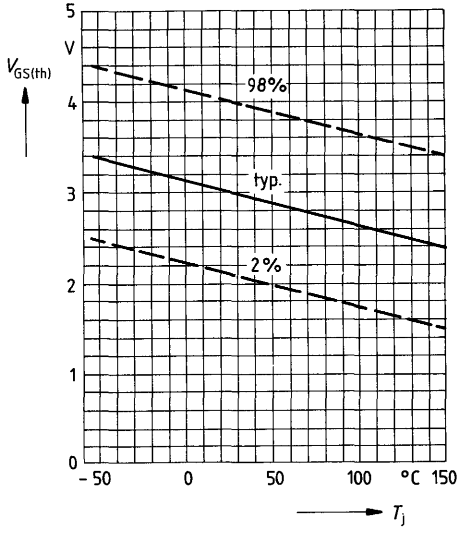
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 2{,}3A$, $V_{GS} = 10V$
(spread)



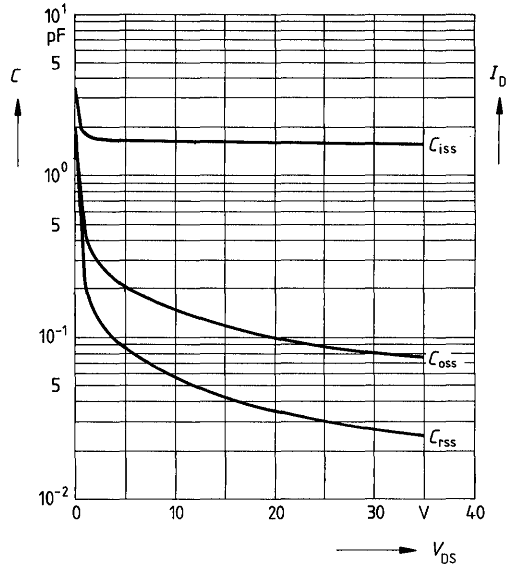
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



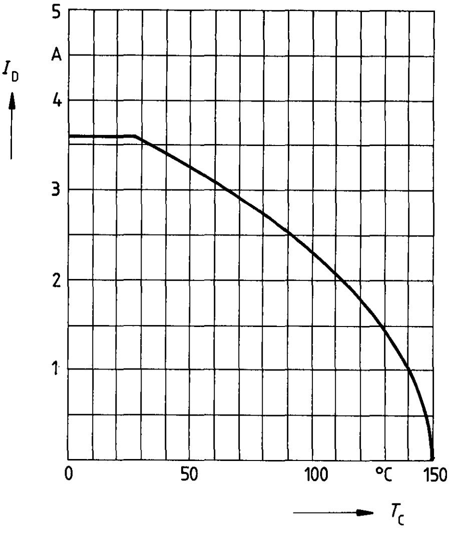
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



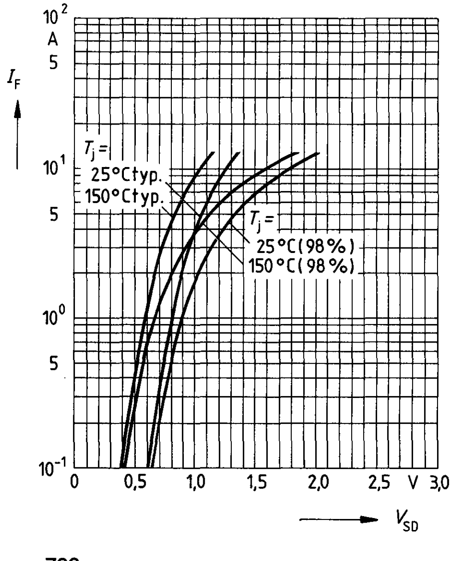
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



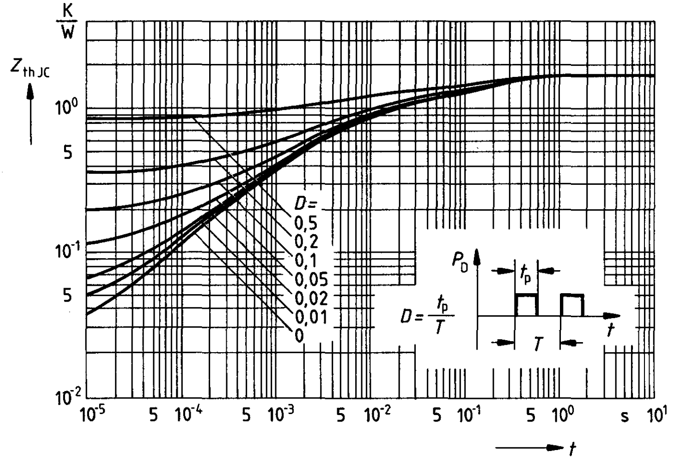
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



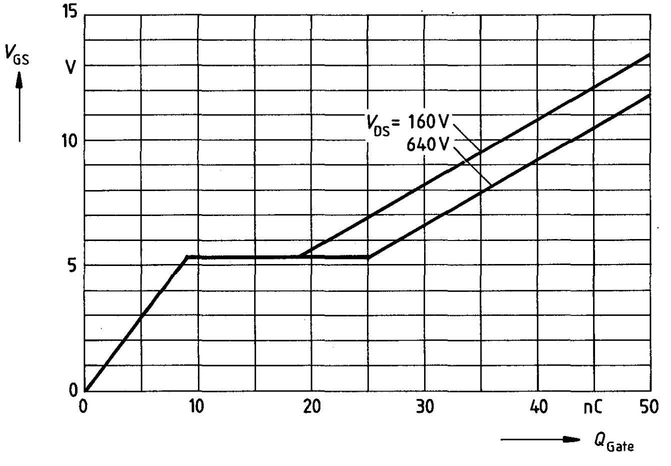
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



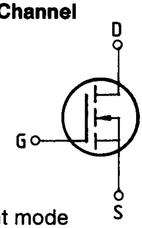
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 5A$



Main ratings

Drain-source voltage V_{DS} **= 800 V**
Continuous drain current I_D **= 2,9 A**
Drain-source on-resistance $R_{DS(on)}$ **4,5 Ω**

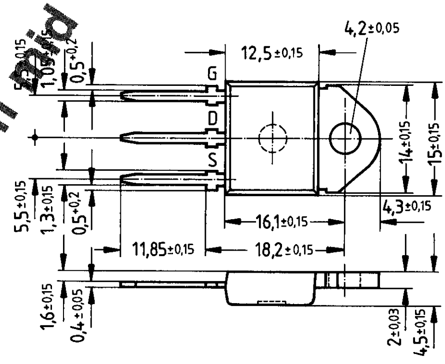
N-Channel



Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 361	C67078-A3200-A2

Available from mid 1987



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	800	V	
Drain-gate voltage	V_{DGR}	800	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	2,9	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	11,5	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	75	W	T_C = 25 °C
Operating and storage	T_j			
temperature range	T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

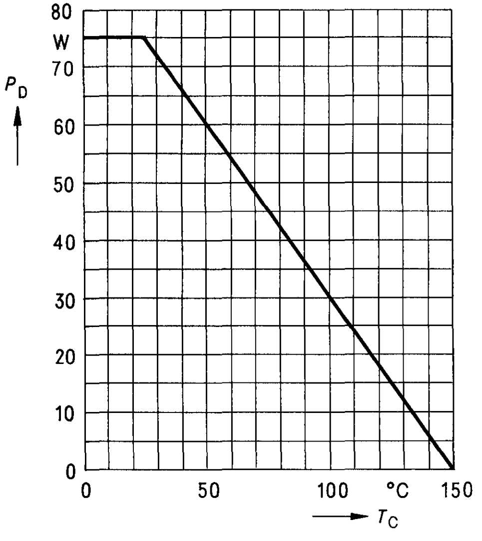
Chip – case	$R_{th\,JC}$	≤1,67	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

Electrical characteristics

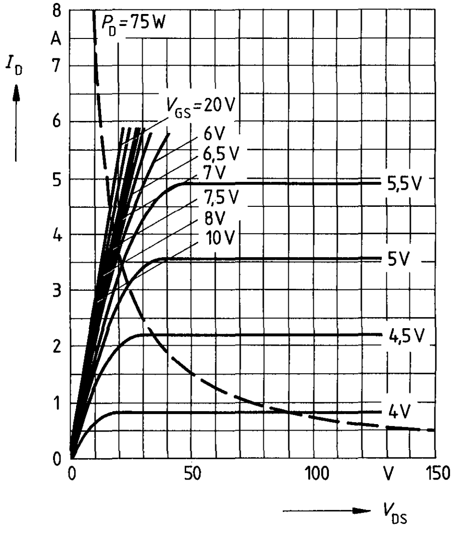
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	800	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 800V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	4,0	4,5	Ω	V_{GS} = 10V I_D = 2,3A
Dynamic ratings						
Forward transconductance	g_{fs}	1,0	2,4	–	S	V_{DS} = 25V I_D = 2,3A
Input capacitance	C_{iss}	–	1,6	2,1	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	90	150	pF	
Reverse transfer capacitance	C_{rss}	–	30	55		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	30	45	ns	V_{CC} = 30V I_D = 2,1A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	50	60		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	100	140		
	t_f	–	60	80		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	2,9	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	11,5		
Diode forward on-voltage	V_{SD}	–	1,15	1,50	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; $I_F = I_{DR}$, di_F/dt = 100A/µs, V_R = 100V
		–	220	300		T_j = 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C
		–	2,6	5,0		T_j = 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		T_j = 150 °C

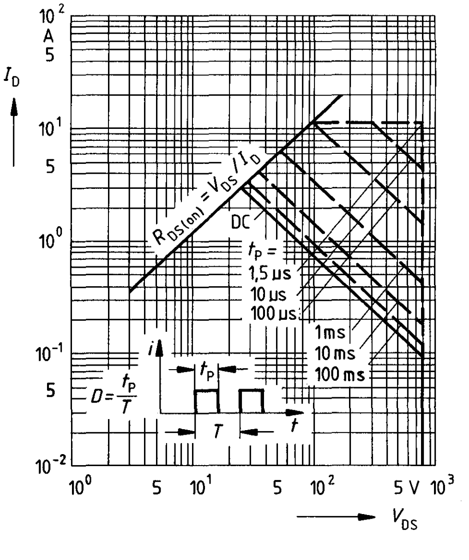
Power dissipation $P_D = f(T_C)$



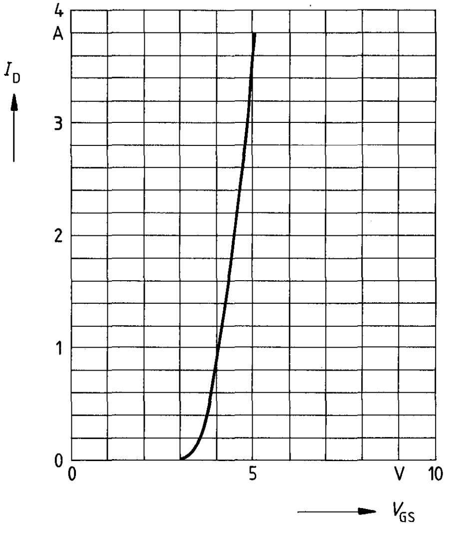
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



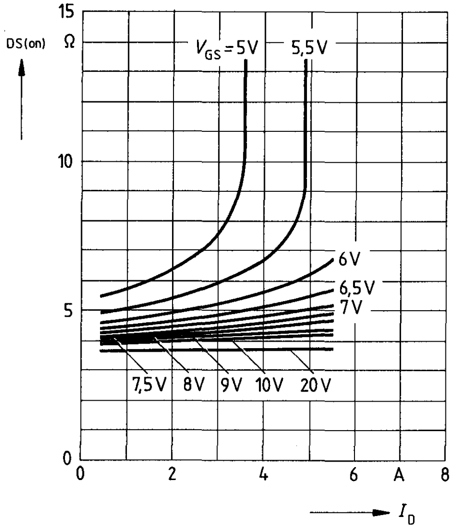
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



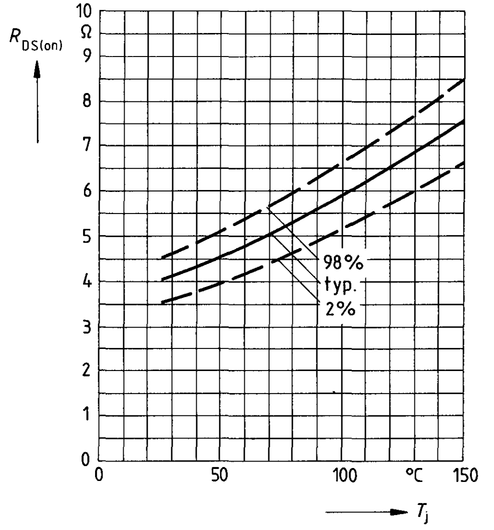
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



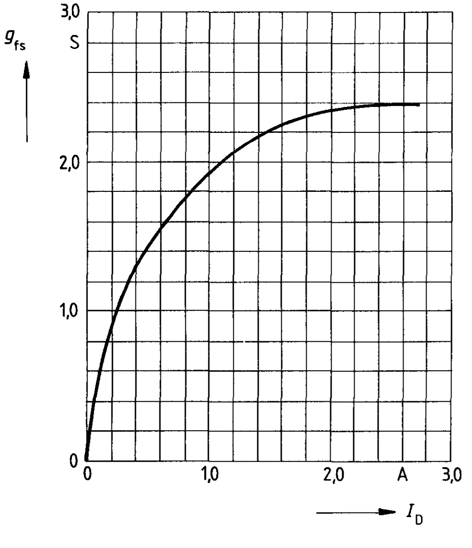
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



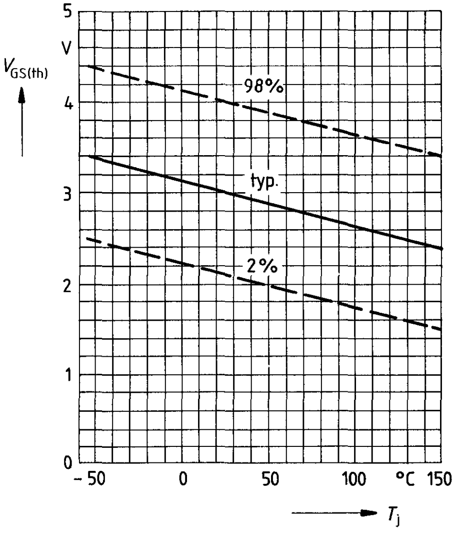
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 2,3A, V_{GS} = 10V
(spread)



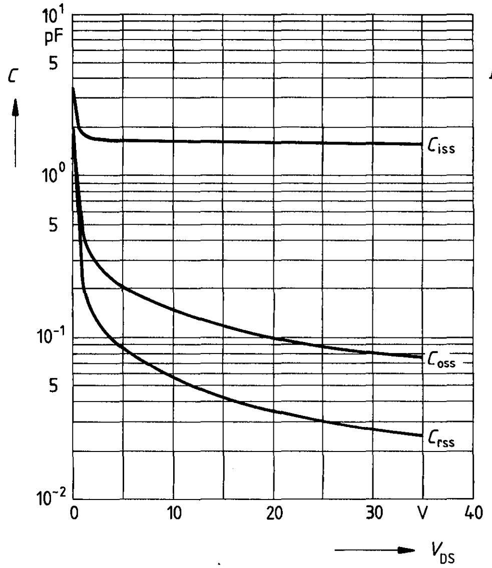
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



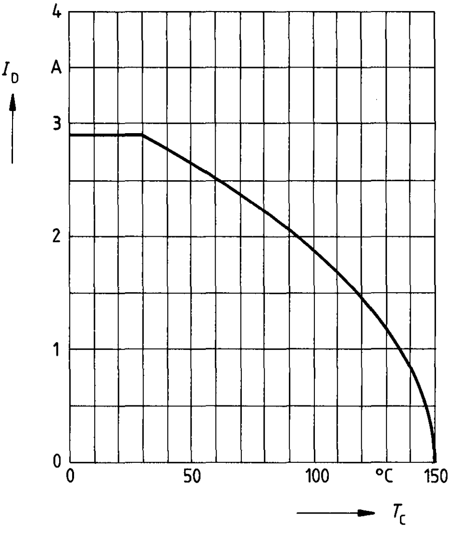
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



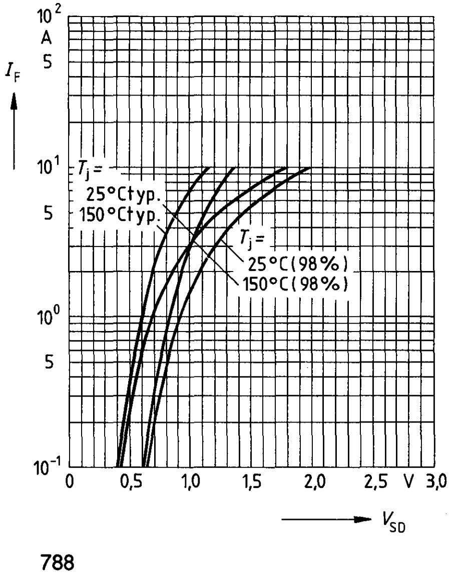
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



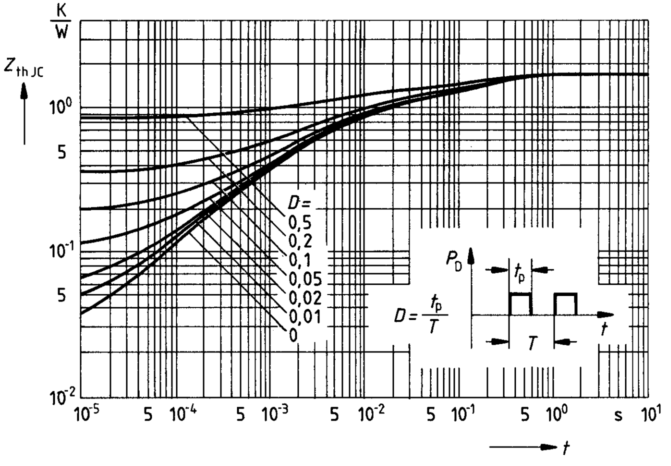
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



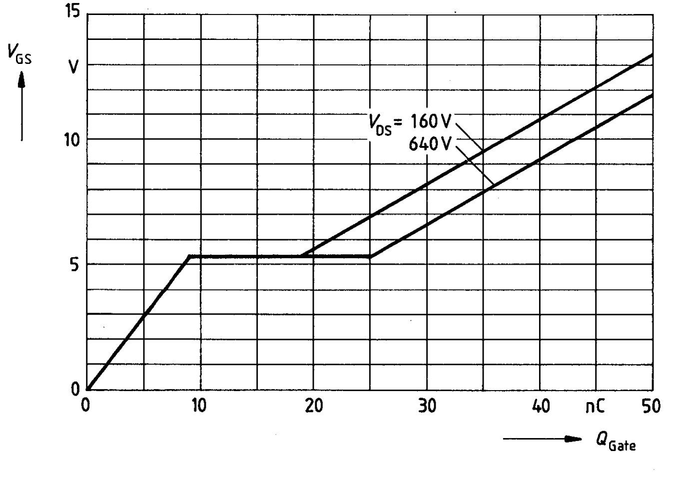
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



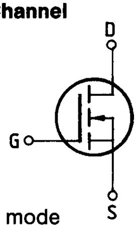
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 5A$



Main ratings

Drain-source voltage V_{DS} **= 1000 V**
Continuous drain current I_D **= 5,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 2,0 Ω**

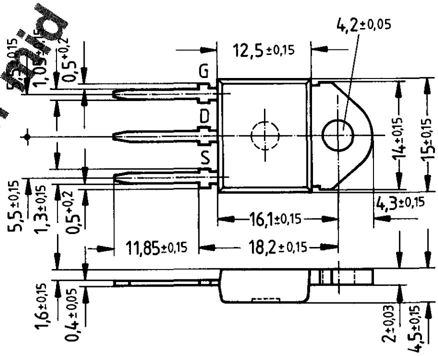
N-Channel



Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 380	C67078-A3205-A2

Available from Mid 1987



Dimensions in mm

Maximum ratings

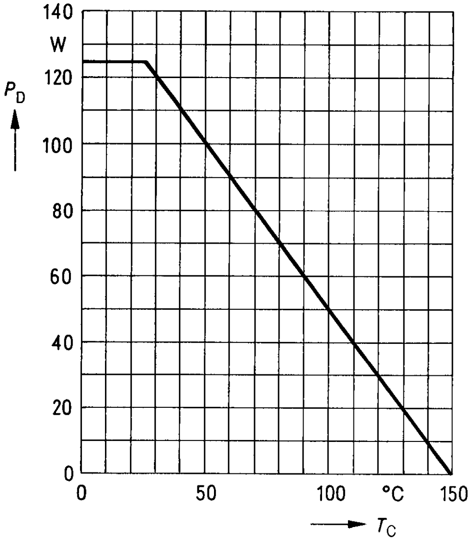
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	5,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	22	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j, T_{stg}	−55 … +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\,JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\,JA}$	≤45	K/W	

Electrical characteristics

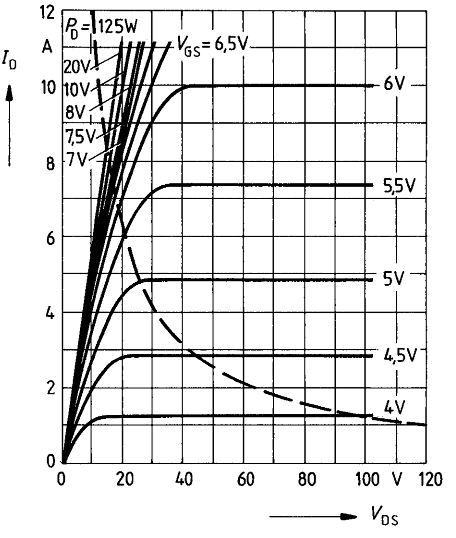
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	1,7	2,0	Ω	V_{GS} = 10V I_D = 3,5A	
Dynamic ratings							
Forward transconductance	g_{fs}	1,4	4,0	–	S	V_{DS} = 25V I_D = 3,5A	
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	180	300	pF		
Reverse transfer capacitance	C_{rss}	–	70	120			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,5A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	90	140			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	5,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	22			
Diode forward on-voltage	V_{SD}	–	1,35	1,60	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	I_F = I_{DR} di_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

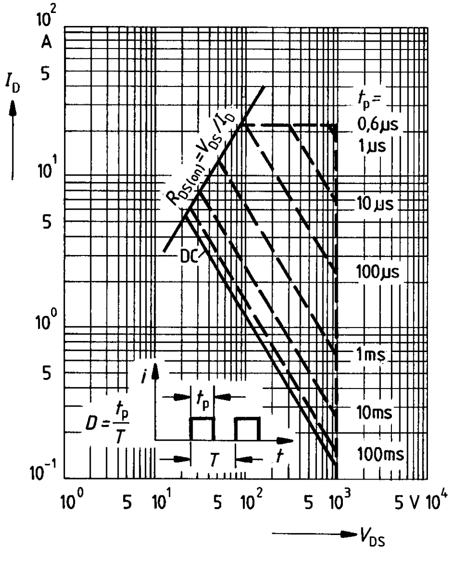
Power dissipation $P_D = f(T_C)$



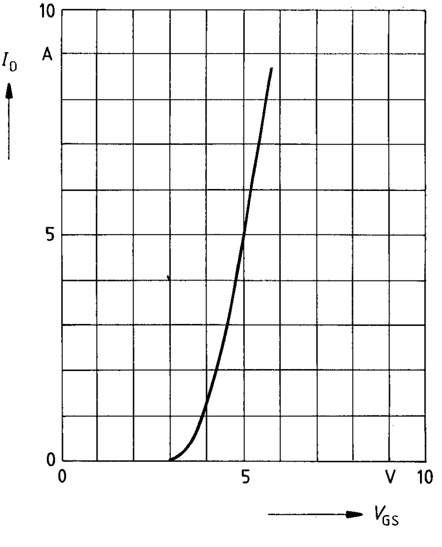
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



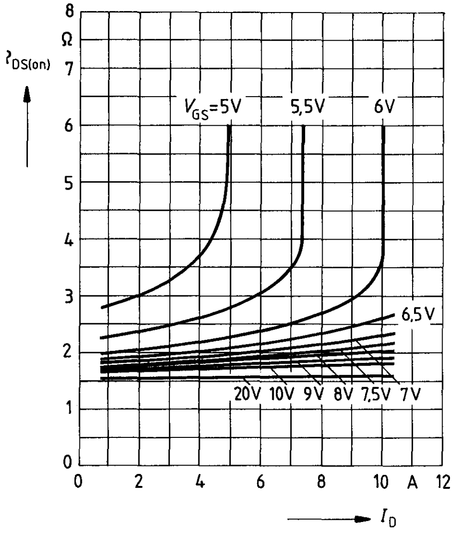
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



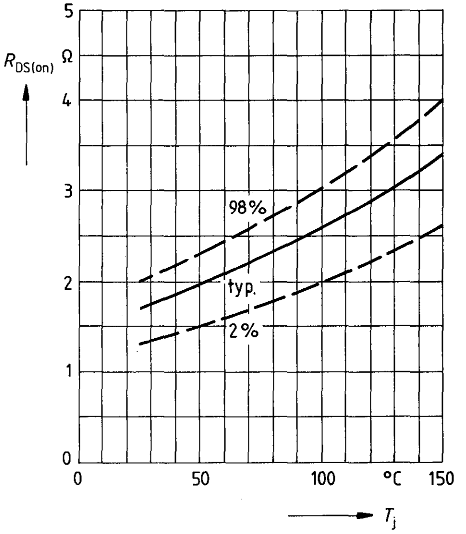
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



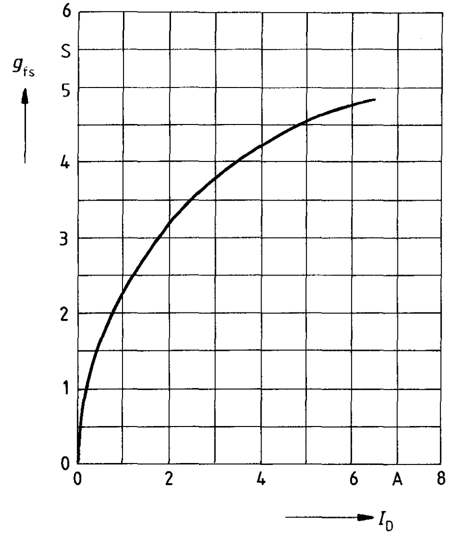
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



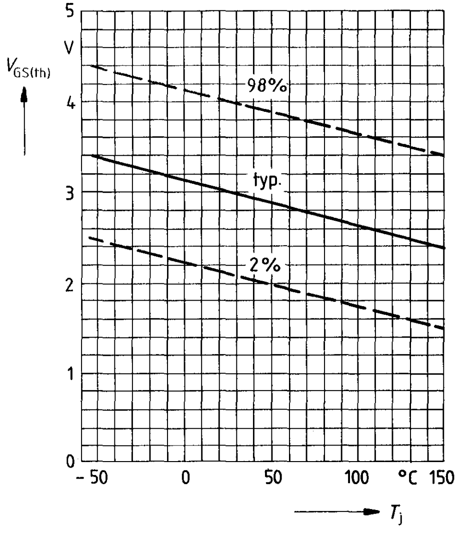
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 3{,}5A$, $V_{GS} = 10V$
(spread)



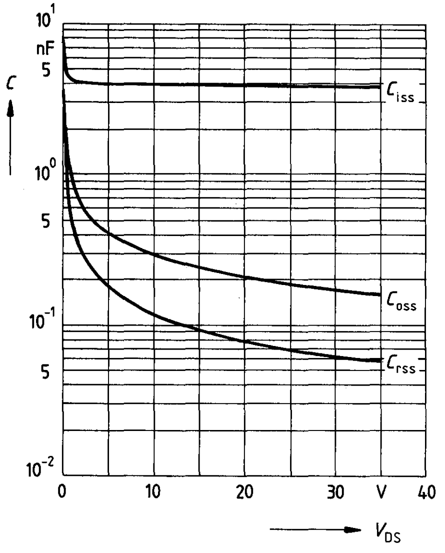
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



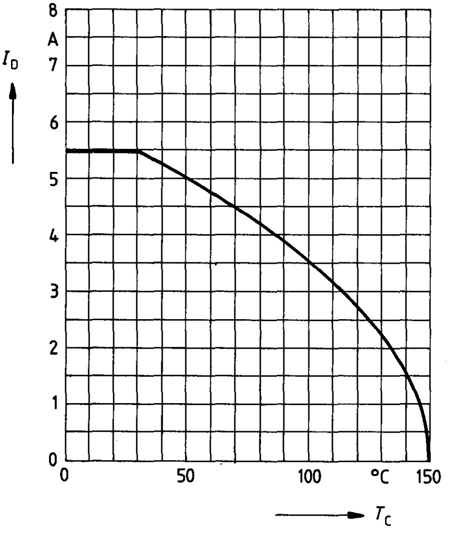
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



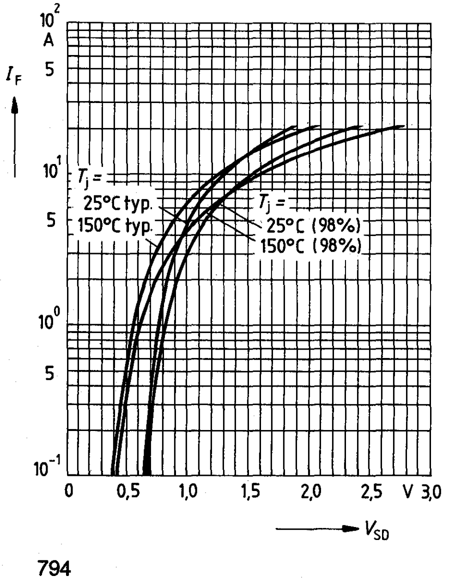
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



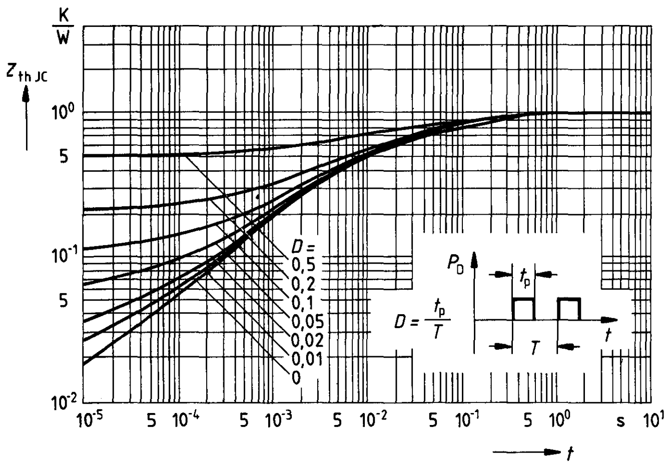
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



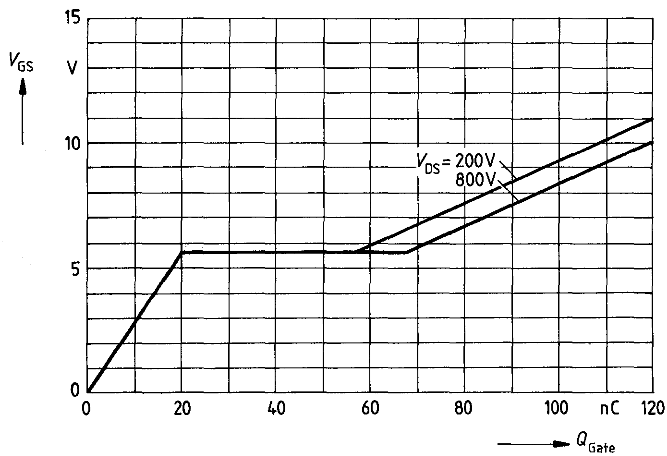
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

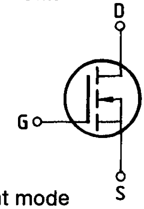


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 8A$



Main ratings

N-Channel



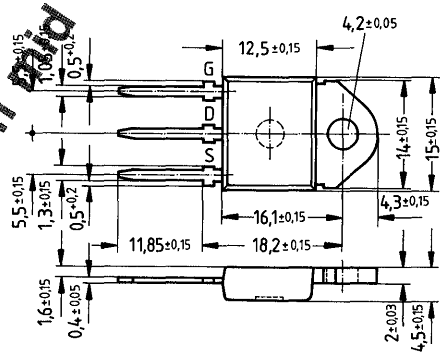
Drain-source voltage V_{DS} = **1000 V**
Continuous drain current I_D = **4,9 A**
Drain-source on-resistance $R_{DS(on)}$ = **2,6 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 381	C67078-A3206-A2

Available from mid 1987



Dimensions in mm

Maximum ratings

Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	1000	V	
Drain-gate voltage	V_{DGR}	1000	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	4,9	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	19	A	T_C = 25 °C
Gate-source voltage	V_{GS}	± 20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1

Thermal resistance

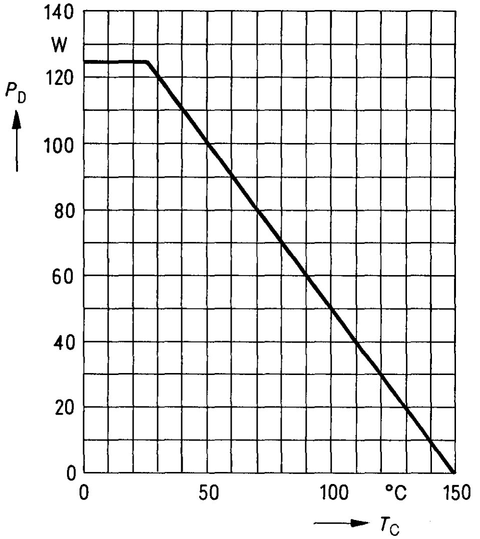
Chip – case	$R_{th\ JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤ 45	K/W	

Electrical characteristics

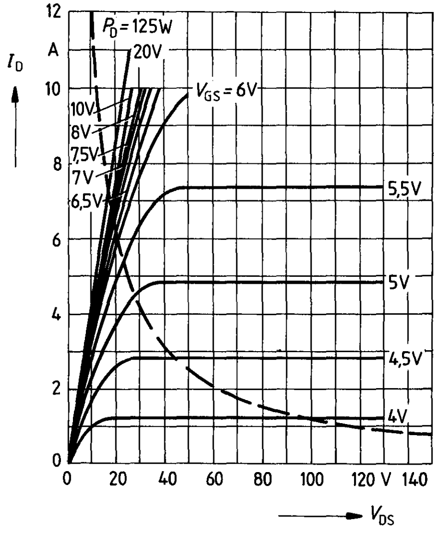
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	1000	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 1000V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	2,3	2,6	Ω	V_{GS} = 10V I_D = 3,5A	
Dynamic ratings							
Forward transconductance	g_{fs}	1,4	4,0	–	S	V_{DS} = 25V I_D = 3,5A	
Input capacitance	C_{iss}	–	3,9	5,0	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	180	300	pF		
Reverse transfer capacitance	C_{rss}	–	70	120			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	60	90	ns	V_{CC} = 30V I_D = 2,4A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	90	140			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	4,9	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	19			
Diode forward on-voltage	V_{SD}	–	1,35	1,60	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	–	250	ns	T_j = 25 °C	$I_F = I_{DR}$ di_F/dt = 100A/µs V_R = 100V
		–	–	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	–	1,2	µC	T_j = 25 °C	
		–	–	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

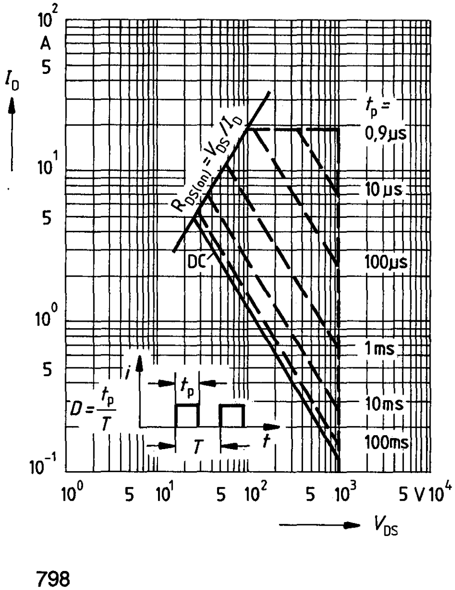
Power dissipation $P_D = f(T_C)$



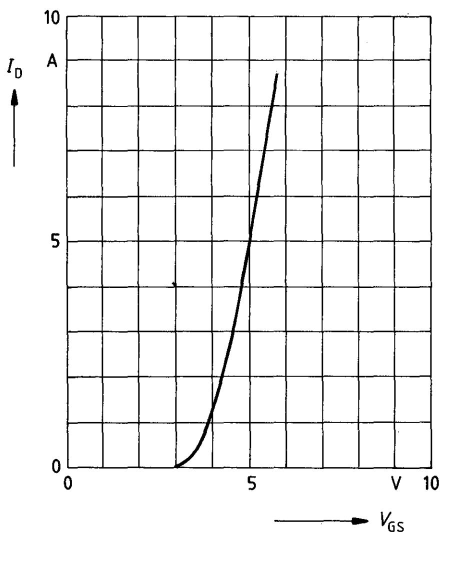
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



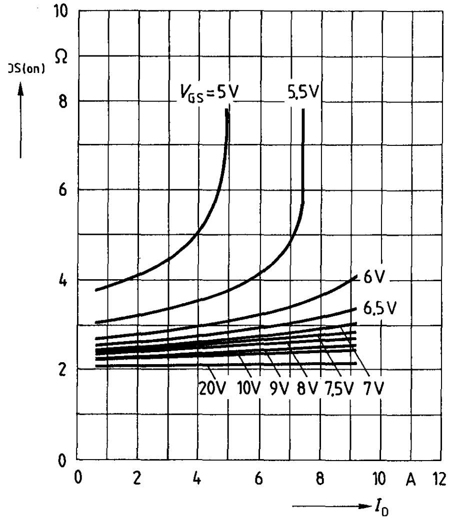
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



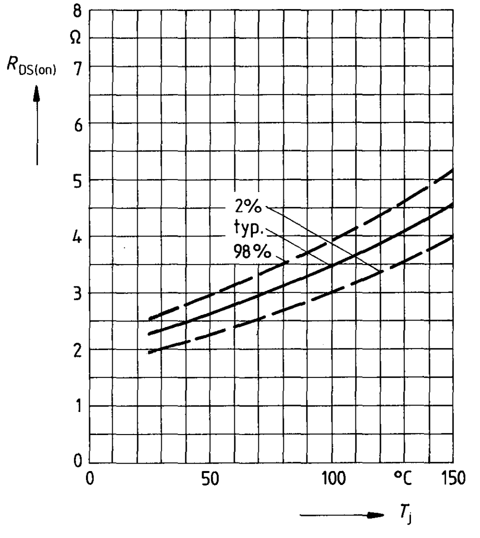
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25\text{V}$, $T_j = 25\,°C$



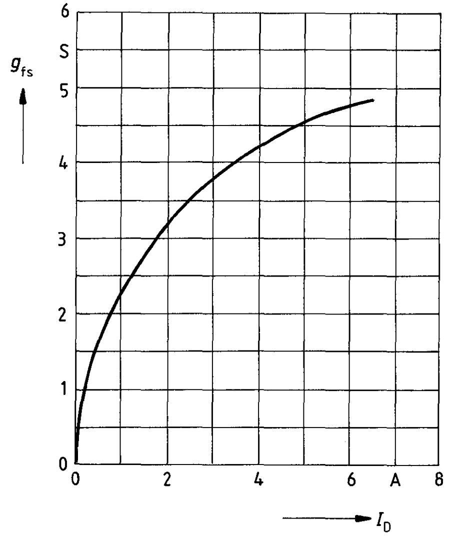
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



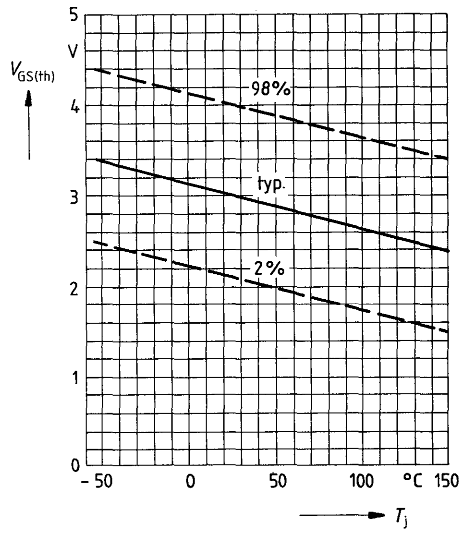
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: I_D = 3,5A, V_{GS} = 10V
(spread)



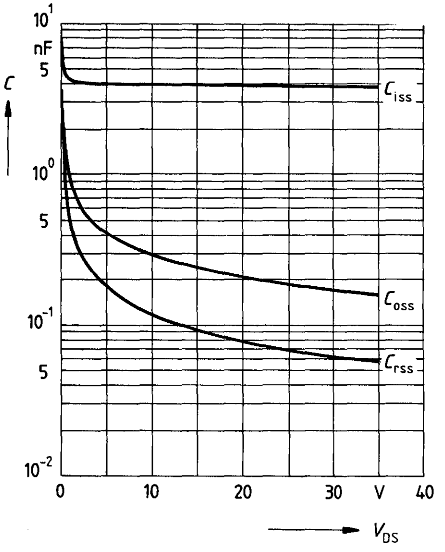
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



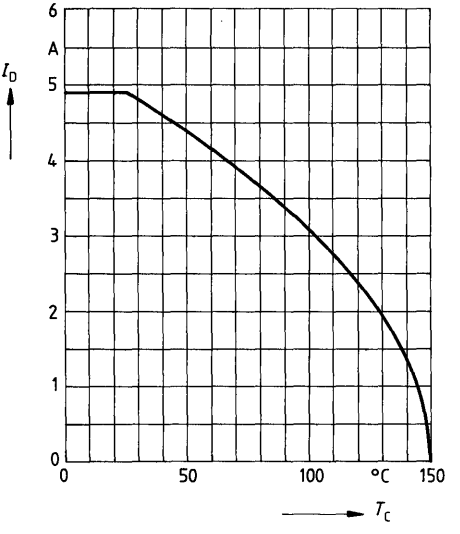
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



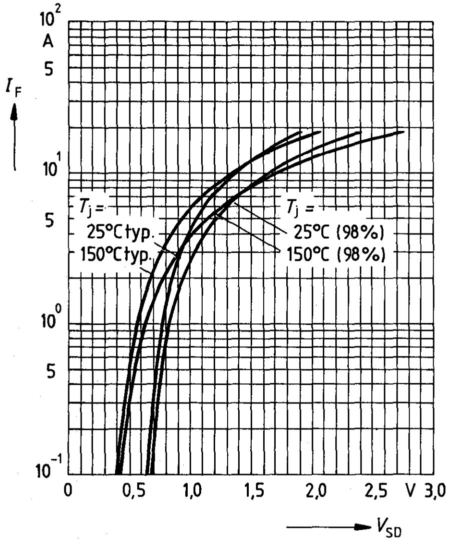
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



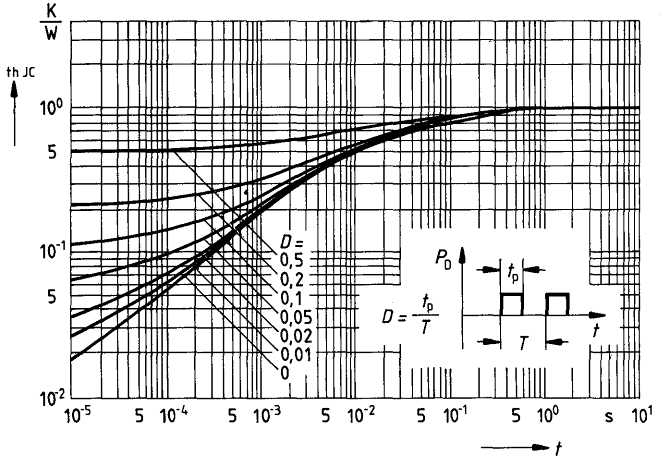
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



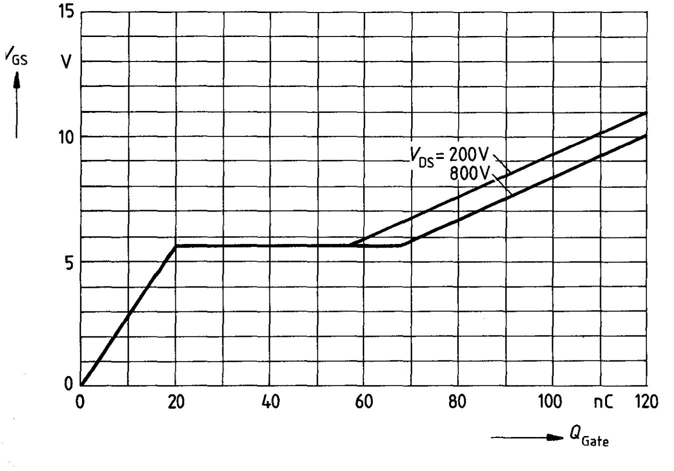
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



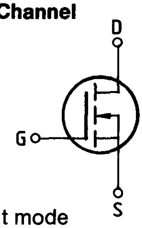
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 8A$



Main ratings

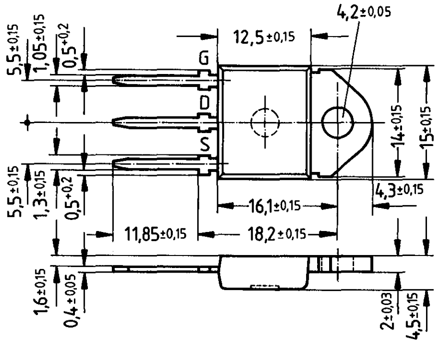
Drain-source voltage V_{DS} **= 400 V**
Continuous drain current I_D **= 12,5 A**
Drain-source on-resistance $R_{DS(on)}$ **= 0,4 Ω**

N-Channel



Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 382	C67078-A3207-A2



Dimensions in mm

Maximum ratings

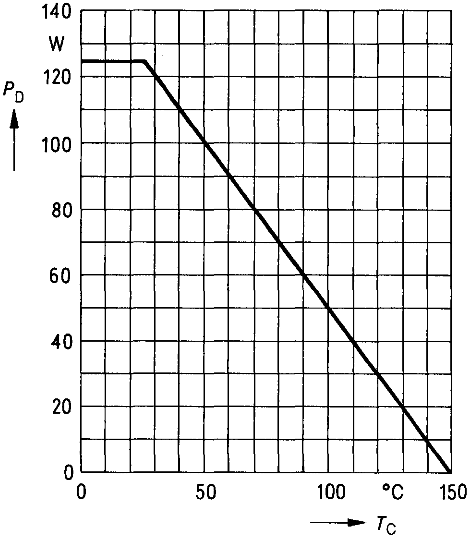
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	12,5	A	T_C = 30 °C
Pulsed drain current	I_{Dpuls}	50	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	−55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤45	K/W	

Electrical characteristics

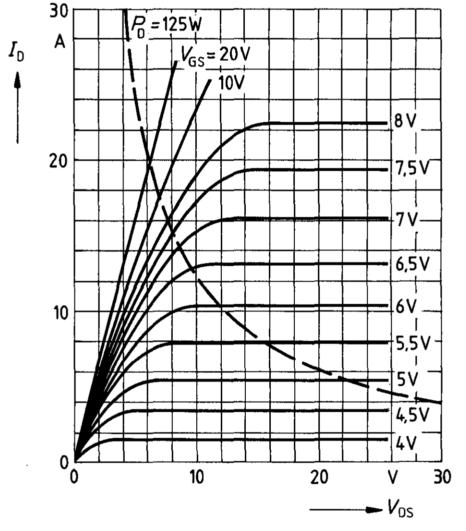
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,35	0,4	Ω	V_{GS} = 10V I_D = 8A	
Dynamic ratings							
Forward transconductance	g_{fs}	3,3	5,2	–	S	V_{DS} = 25V I_D = 8A	
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	300	500	pF		
Reverse transfer capacitance	C_{rss}	–	120	200			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	80	120			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	12,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	50			
Diode forward on-voltage	V_{SD}	–	1,4	1,9	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	I_F = I_{DR} di_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

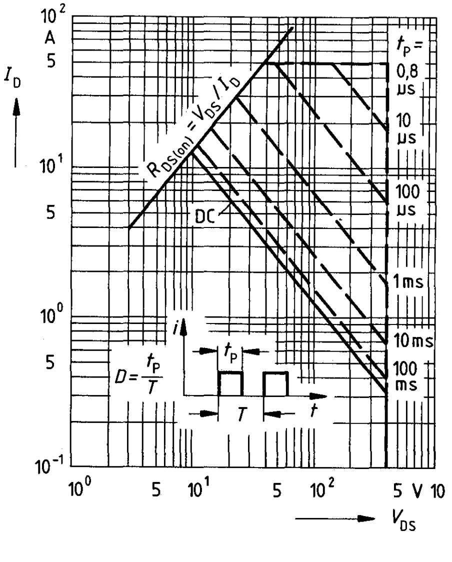
Power dissipation $P_D = f(T_C)$



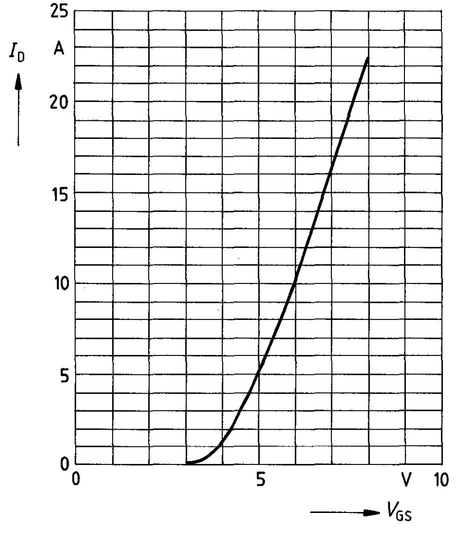
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



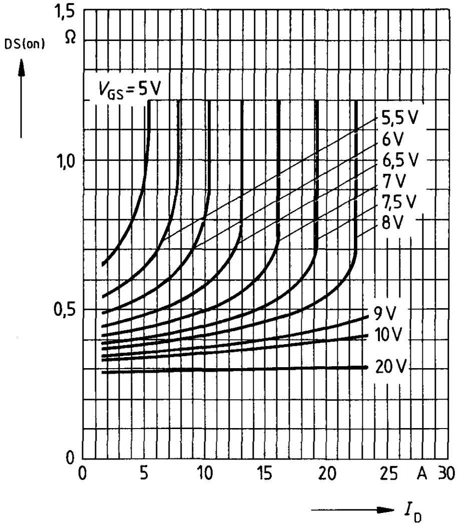
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



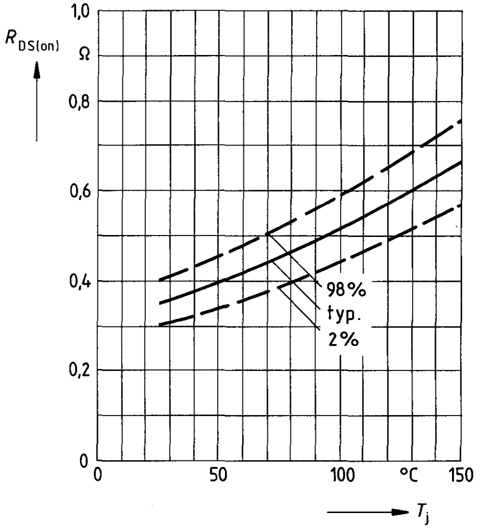
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



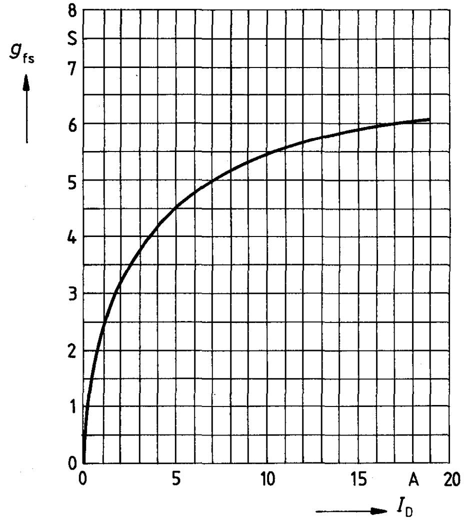
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



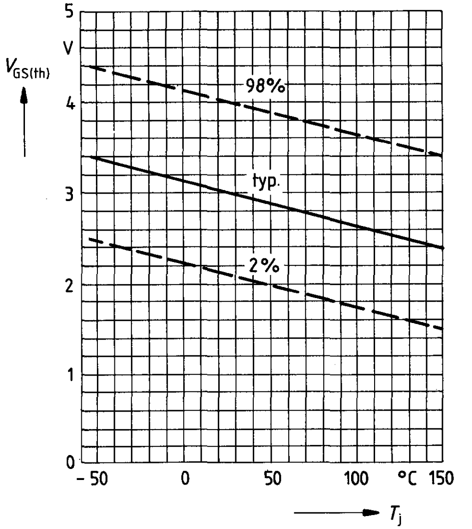
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 8A$, $V_{GS} = 10V$
(spread)



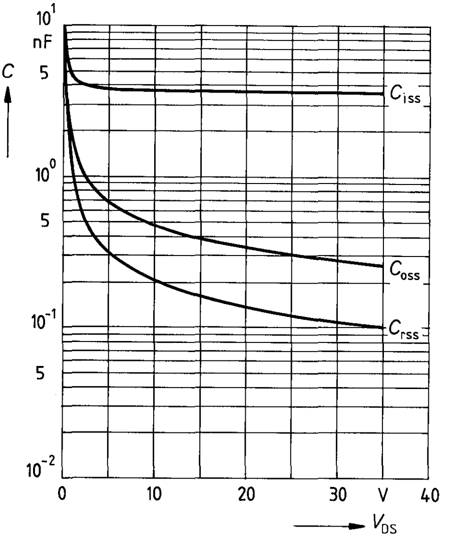
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



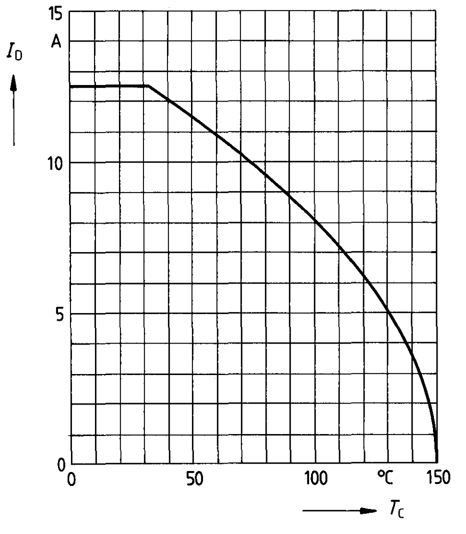
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



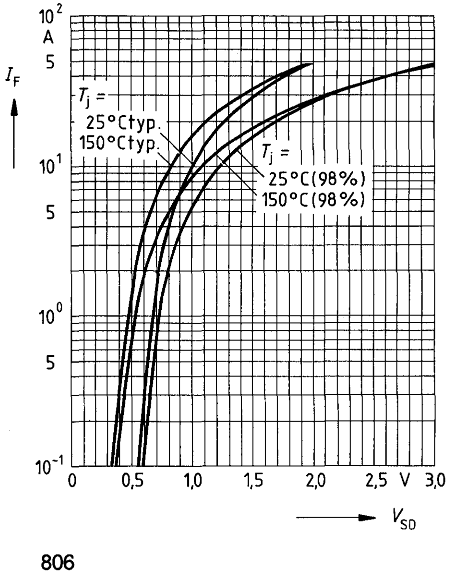
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1MHz$



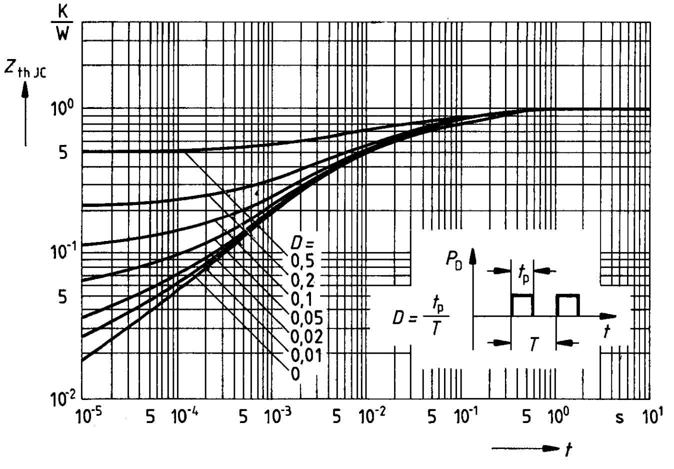
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



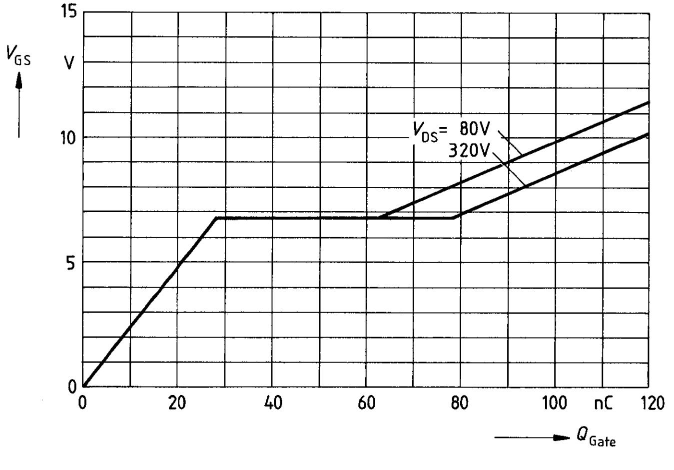
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



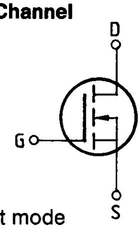
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\ puls} = 17{,}3A$



Main ratings

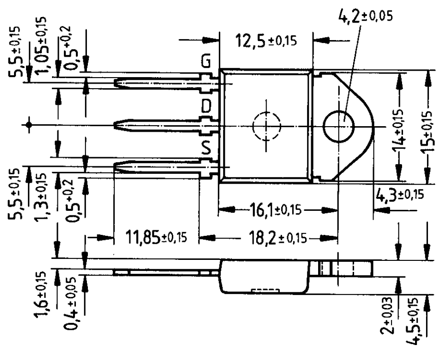
Drain-source voltage V_{DS} = **400 V**
Continuous drain current I_D = **11,5 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,5 Ω**

N-Channel



Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 383	C67078-A3308-A2



Dimensions in mm

Maximum ratings

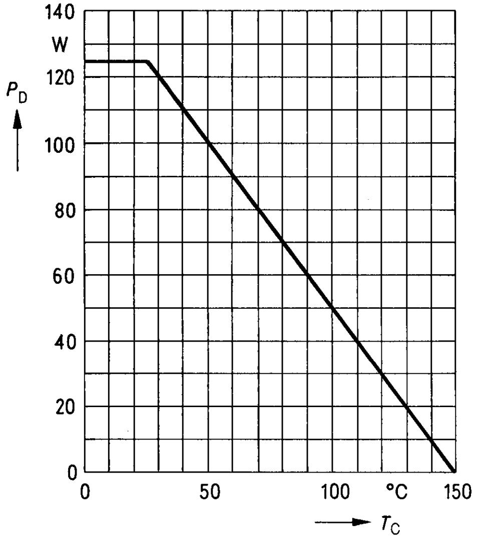
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	400	V	
Drain-gate voltage	V_{DGR}	400	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	11,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	46	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40 040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th JA}$	≤ 45	K/W	

Electrical characteristics

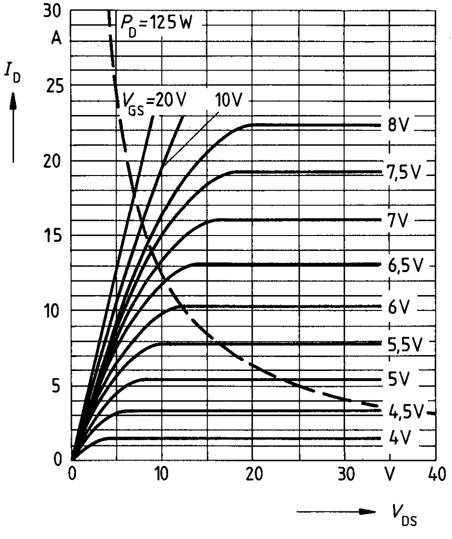
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	400	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 400V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,45	0,5	Ω	V_{GS} = 10V I_D = 7,5A	
Dynamic ratings							
Forward transconductance	g_{fs}	3,3	5,2	–	S	V_{DS} = 25V I_D = 7,5A	
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	300	500	pF		
Reverse transfer capacitance	C_{rss}	–	120	200			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,9A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	80	120			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	11,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	46			
Diode forward on-voltage	V_{SD}	–	1,4	1,9	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	I_F = I_{DR} dI_F/dt = 100A/µs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

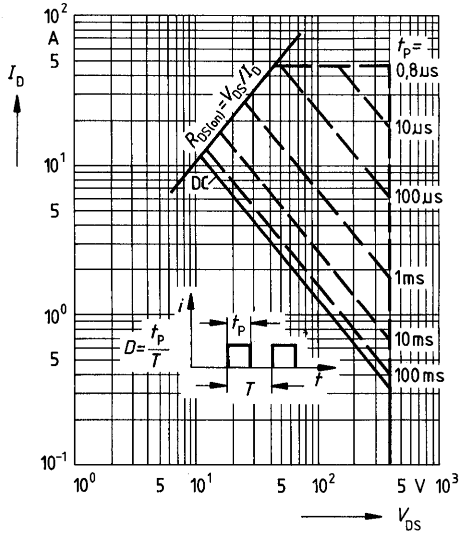
Power dissipation $P_D = f(T_C)$



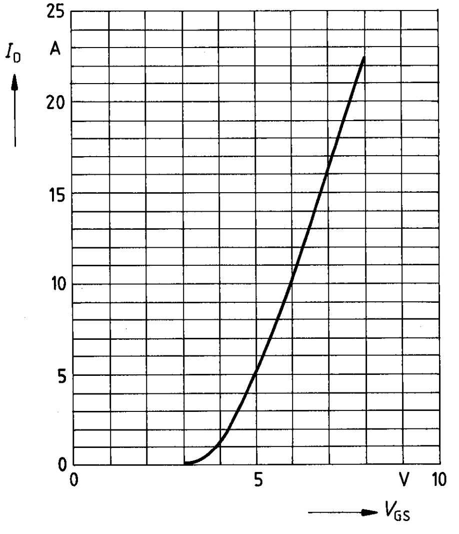
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



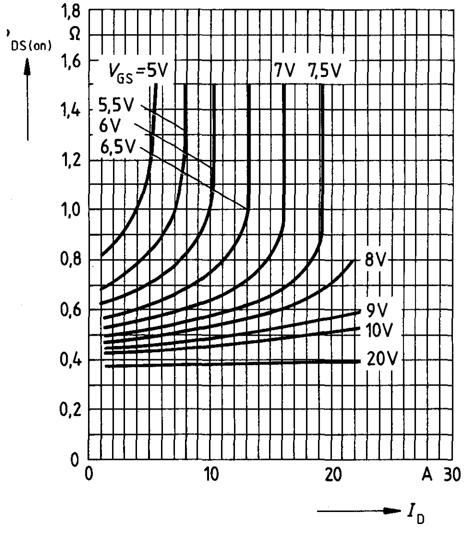
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



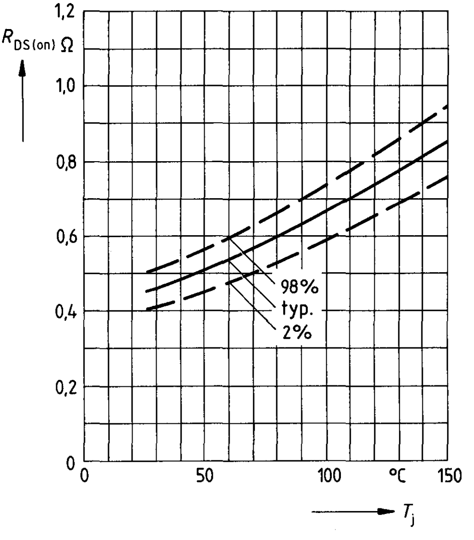
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



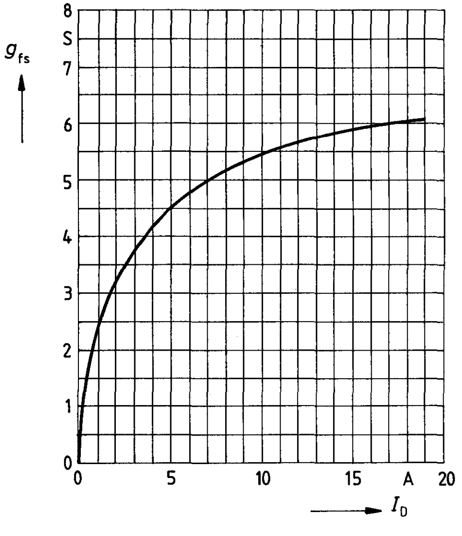
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



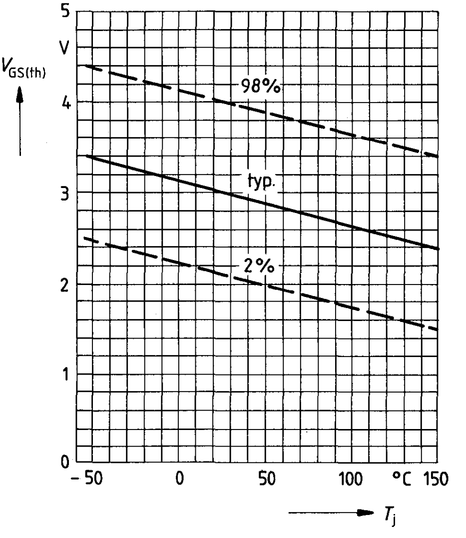
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: I_D = 7,5A, V_{GS} = 10V
(spread)



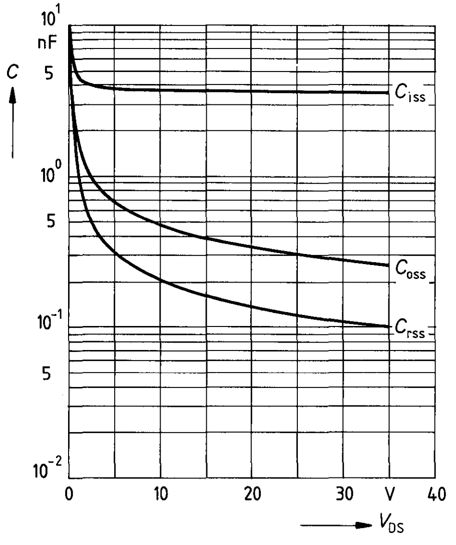
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
V_{DS} = 25V, $T_j = 25\,°C$



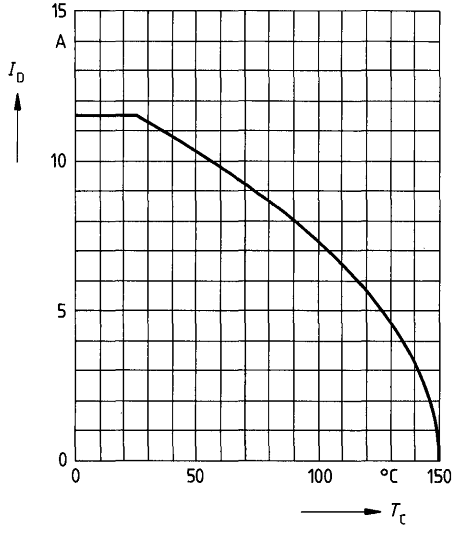
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, I_D = 1mA
(spread)



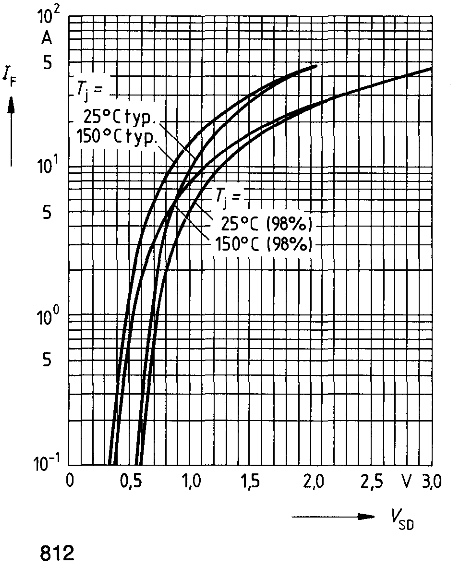
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



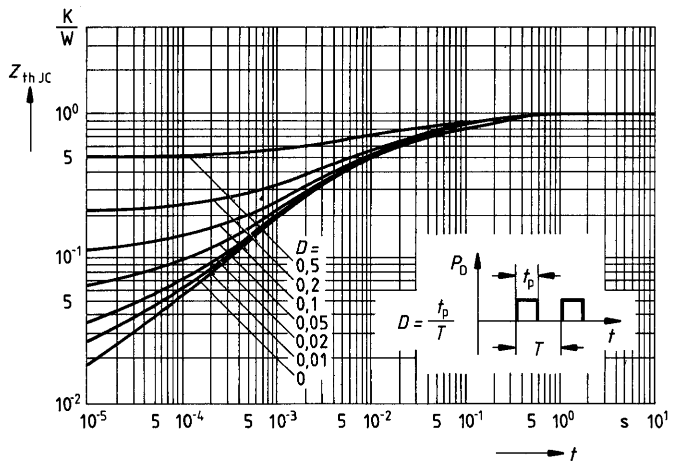
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10\text{V}$



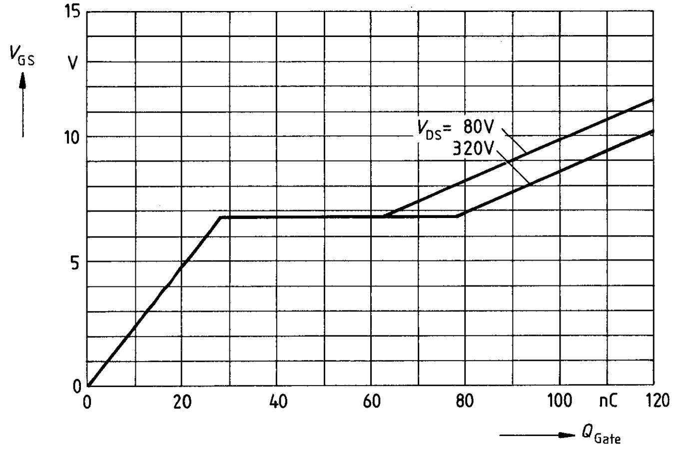
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$

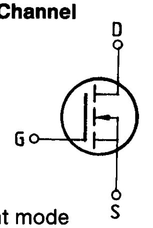


Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 17{,}3A$



Main ratings

N-Channel

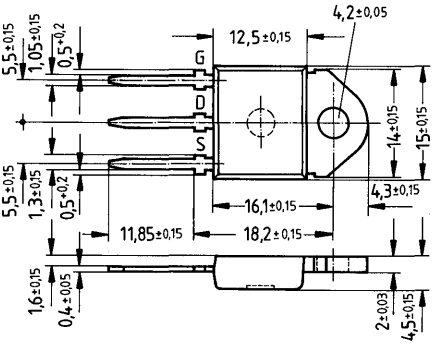


Drain-source voltage	V_{DS}	**= 500 V**
Continuous drain current	I_D	**= 10,5 A**
Drain-source on-resistance	$R_{DS(on)}$	**= 0,6 Ω**

Description FREDET with fast-recovery reverse diode, N-channel, enhancement mode

Case Plastic package 15 in accordance with DIN 41 869 or TO 218 AA (TOP 3) in accordance with JEDEC. The drain terminal is conductively connected to the mounting flange. Approx. weight 4,5 g

Type	Ordering code
BUZ 384	C67078-A3206-A2



Dimensions in mm

Maximum ratings

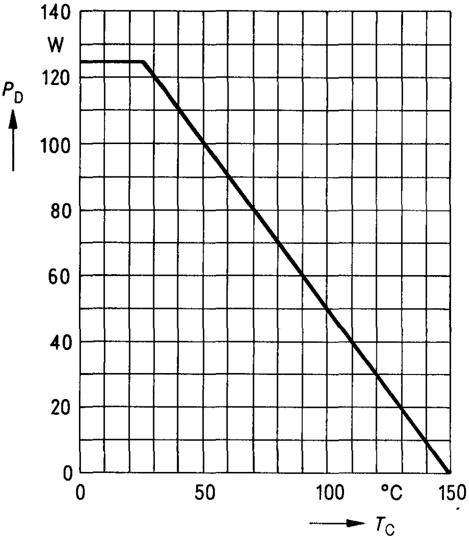
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	10,5	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	42	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	–55 ... +150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤45	K/W	

Electrical characteristics

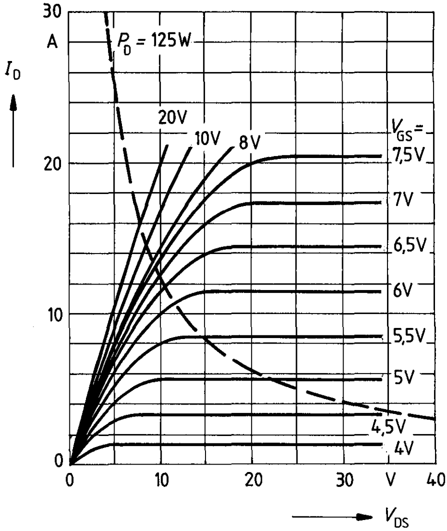
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions	
Static ratings							
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA	
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA	
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	μA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V	
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V	
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,55	0,6	Ω	V_{GS} = 10V I_D = 6,6A	
Dynamic ratings							
Forward transconductance	g_{fs}	2,7	5,4	–	S	V_{DS} = 25V I_D = 6,6A	
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz	
Output capacitance	C_{oss}	–	250	400	pF		
Reverse transfer capacitance	C_{rss}	–	100	170			
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω	
	t_r	–	80	120			
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430			
	t_f	–	110	140			
Fast-recovery reverse diode							
Continuous reverse drain current	I_{DR}	–	–	10,5	A	T_C = 25 °C	
Pulsed reverse drain current	I_{DRM}	–	–	42			
Diode forward on-voltage	V_{SD}	–	1,5	1,9	V	I_F = 2× I_{DR} V_{GS} = 0V, T_j = 25 °C	
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C	$I_F = I_{DR}$ di_F/dt = 100A/μs V_R = 100V
		–	220	300		= 150 °C	
Reserve recovery charge	Q_{rr}	–	0,65	1,2	μC	T_j = 25 °C	
		–	2,6	5,0		= 150 °C	
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C	
		–	15	–		= 150 °C	

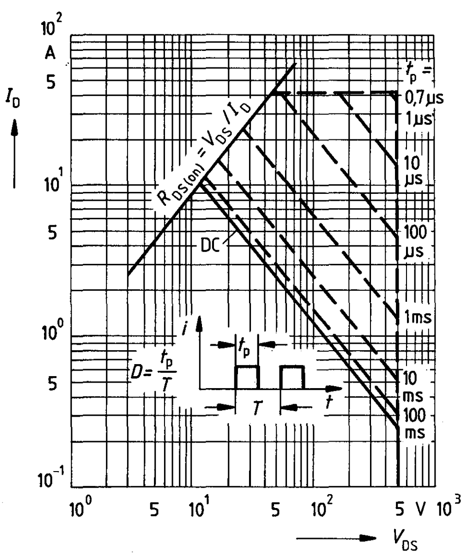
Power dissipation $P_D = f(T_C)$



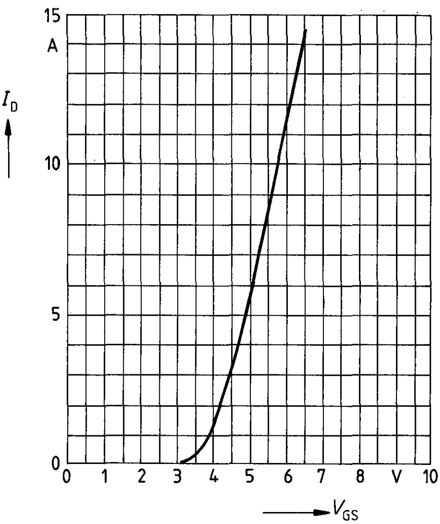
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



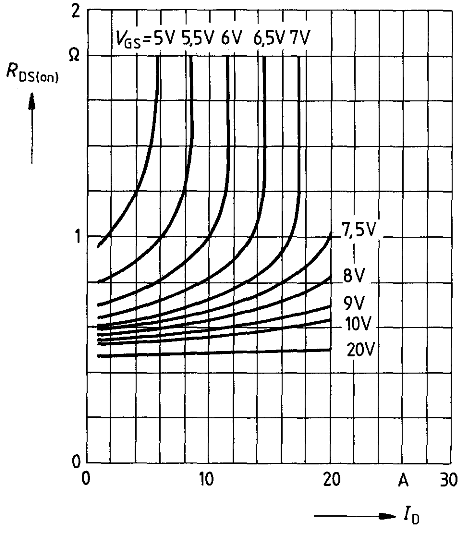
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



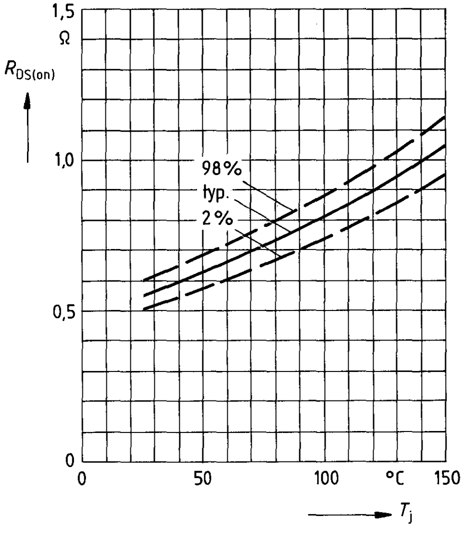
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



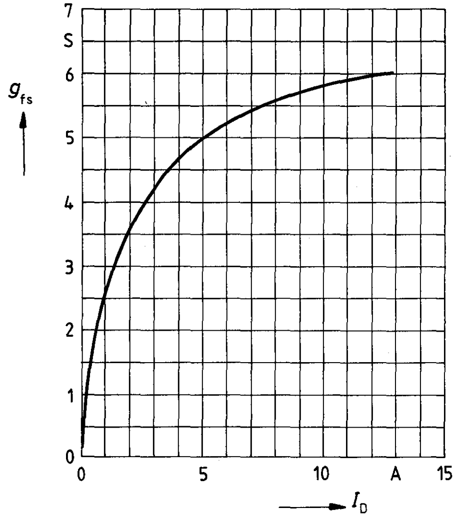
Typical drain-source on-state resistance
$R_{DS(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25°C$



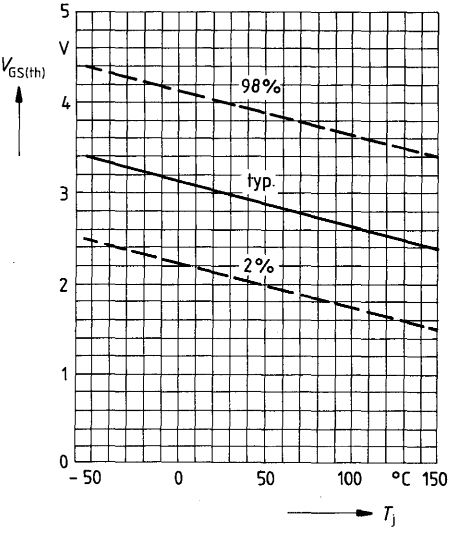
Drain-source on-state resistance
$R_{DS(on)} = f(T_j)$
parameter: $I_D = 6{,}5A$, $V_{GS} = 10V$
(spread)



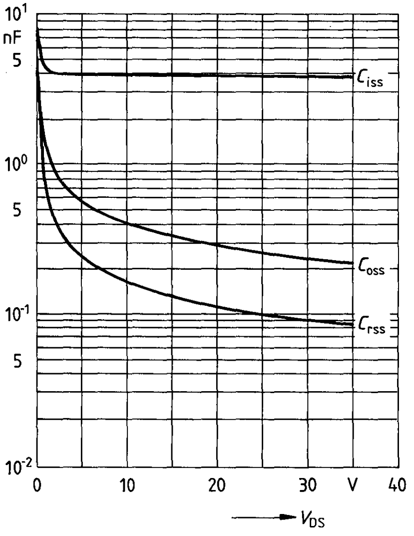
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 μs pulse test,
$V_{DS} = 25V$, $T_j = 25°C$



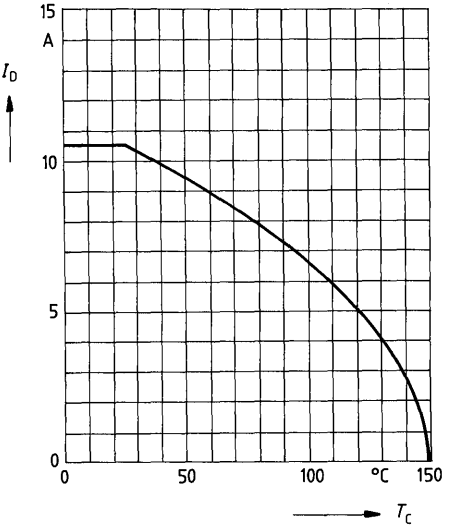
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



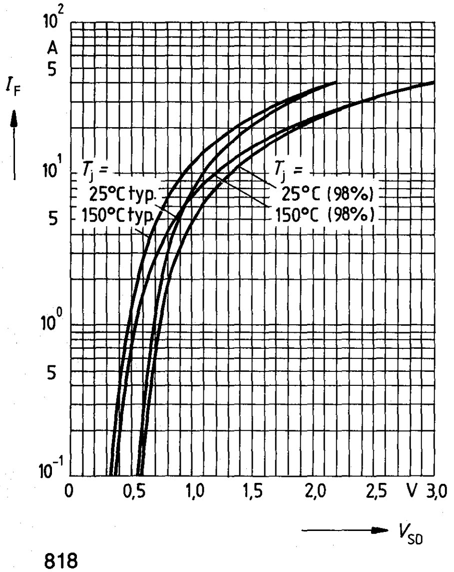
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



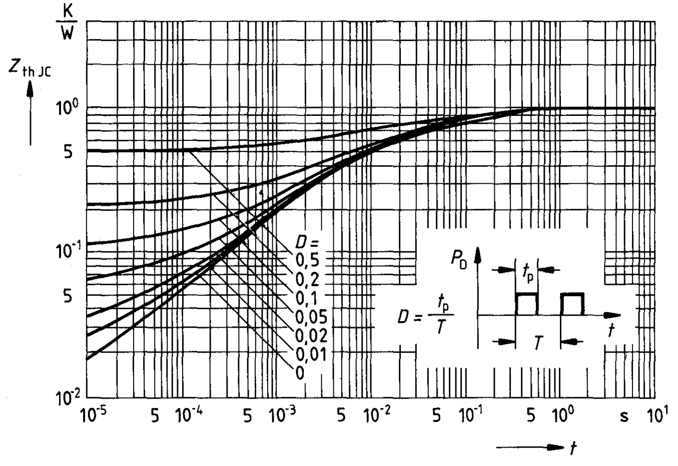
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



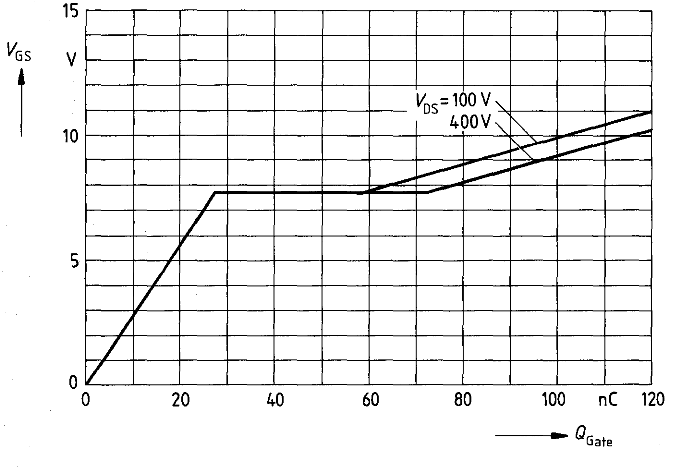
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80$ µs
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



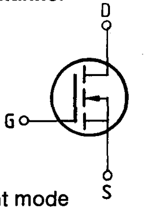
Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14{,}4\text{A}$



Main ratings

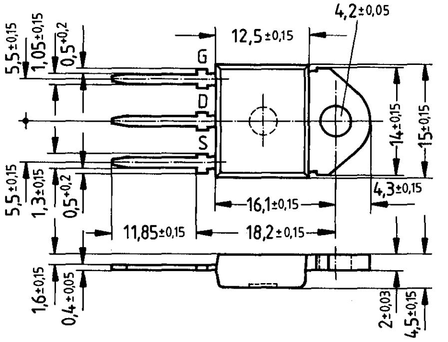
Drain-source voltage V_{DS} = **500 V**
Continuous drain current I_D = **9 A**
Drain-source on-resistance $R_{DS(on)}$ = **0,8 Ω**

N-Channel



Description FREDFET with fast-recovery reverse diode, N-channel, enhancement mode
Case Plastic package 15 in accordance with DIN 41 869 or
TO 218 AA (TOP 3) in accordance with JEDEC.
The drain terminal is conductively connected to the mounting flange.
Approx. weight 4,5 g

Type	Ordering code
BUZ 385	C67078-A3210-A2



Dimensions in mm

Maximum ratings

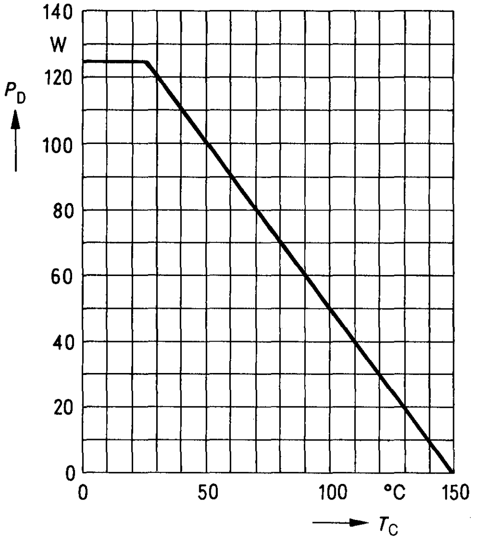
Description	Symbols	Ratings	Units	Conditions
Drain-source voltage	V_{DS}	500	V	
Drain-gate voltage	V_{DGR}	500	V	R_{GS} = 20 kΩ
Continuous drain current	I_D	9	A	T_C = 25 °C
Pulsed drain current	I_{Dpuls}	36	A	T_C = 25 °C
Gate-source voltage	V_{GS}	±20	V	
Max. power dissipation	P_D	125	W	T_C = 25 °C
Operating and storage temperature range	T_j T_{stg}	– 55 ... + 150	°C	
DIN humidity category		E	–	DIN 40040
IEC climatic category		55/150/56		DIN IEC 68-1
Thermal resistance				
Chip – case	$R_{th\ JC}$	≤ 1,0	K/W	
Chip – ambient	$R_{th\ JA}$	≤ 45	K/W	

Electrical characteristics

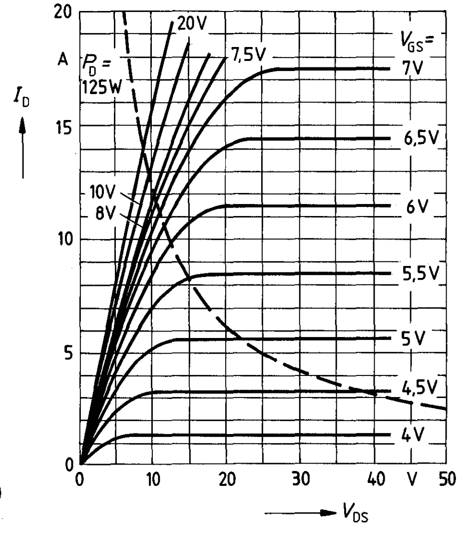
(at T_j = 25 °C unless otherwise specified)

Description	Symbol	Characteristics min.	typ.	max.	Unit	Conditions
Static ratings						
Drain-source breakdown voltage	$V_{(BR)\,DSS}$	500	–	–	V	V_{GS} = 0V I_D = 0,25mA
Gate threshold voltage	$V_{GS\,(th)}$	2,1	3,0	4,0		V_{DS} = V_{GS} I_D = 1mA
Zero gate voltage drain current	I_{DSS}	– –	20 100	250 1000	µA	T_j = 25 °C T_j = 125 °C V_{DS} = 500V V_{GS} = 0V
Gate-source leakage current	I_{GSS}	–	10	100	nA	V_{GS} = 20V V_{DS} = 0V
Drain-source on-resistance	$R_{DS\,(on)}$	–	0,7	0,8	Ω	V_{GS} = 10V I_D = 6,5A
Dynamic ratings						
Forward transconductance	g_{fs}	2,7	6,6	–	S	V_{DS} = 25V I_D = 6,5A
Input capacitance	C_{iss}	–	3,8	4,9	nF	V_{GS} = 0V V_{DS} = 25V f = 1MHz
Output capacitance	C_{oss}	–	250	400	pF	
Reverse transfer capacitance	C_{rss}	–	100	170		
Turn-on time t_{on} ($t_{on} = t_{d\,(on)} + t_r$)	$t_{d\,(on)}$	–	50	75	ns	V_{CC} = 30V I_D = 2,8A V_{GS} = 10V R_{GS} = 50Ω
	t_r	–	80	120		
Turn-off time t_{off} ($t_{off} = t_{d\,(off)} + t_f$)	$t_{d\,(off)}$	–	330	430		
	t_f	–	110	140		
Fast-recovery reverse diode						
Continuous reverse drain current	I_{DR}	–	–	9,0	A	T_C = 25 °C
Pulsed reverse drain current	I_{DRM}	–	–	36		
Diode forward on-voltage	V_{SD}	–	1,5	1,9	V	I_F = 2 × I_{DR} V_{GS} = 0V, T_j = 25 °C
Reverse recovery time	t_{rr}	–	180	250	ns	T_j = 25 °C; $I_F = I_{DR}$, di_F/dt = 100A/µs, V_R = 100V
		–	220	300		T_j = 150 °C
Reserve recovery charge	Q_{rr}	–	0,65	1,2	µC	T_j = 25 °C
		–	2,6	5,0		T_j = 150 °C
Repetitive peak reverse current	I_{RRM}	–	–	–	A	T_j = 25 °C
		–	15	–		T_j = 150 °C

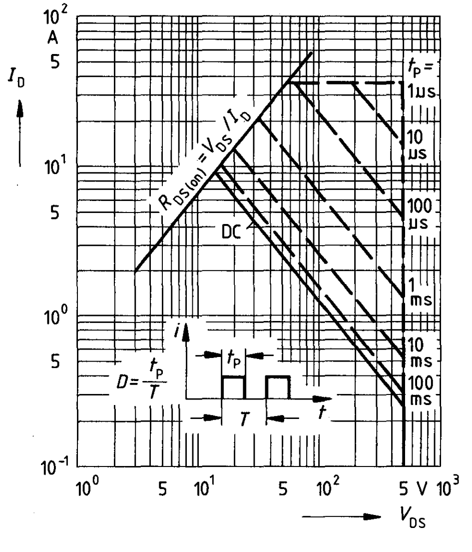
Power dissipation $P_D = f(T_C)$



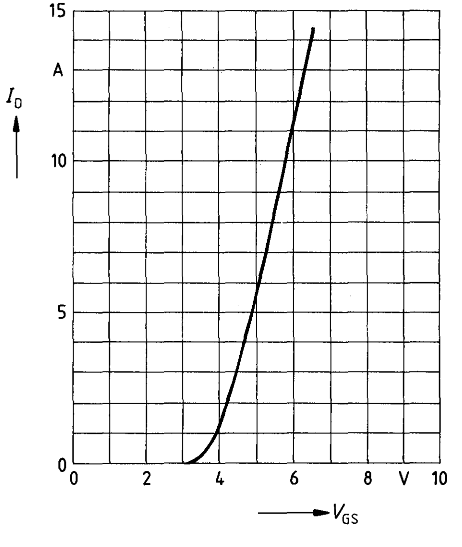
Typical output characteristics $I_D = f(V_{DS})$
parameter: 80 µs pulse test,
$T_j = 25\,°C$



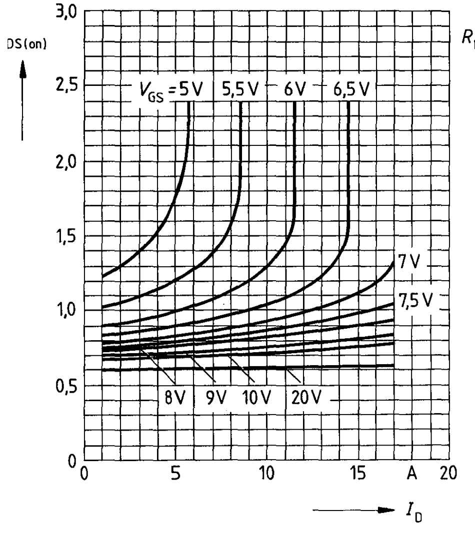
Safe operating area $I_D = f(V_{DS})$
parameter: $D = 0.01$, $T_C = 25\,°C$



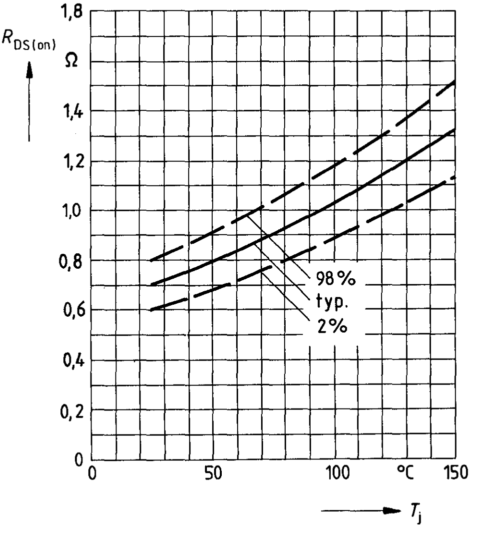
Typical transfer characteristic $I_D = f(V_{GS})$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



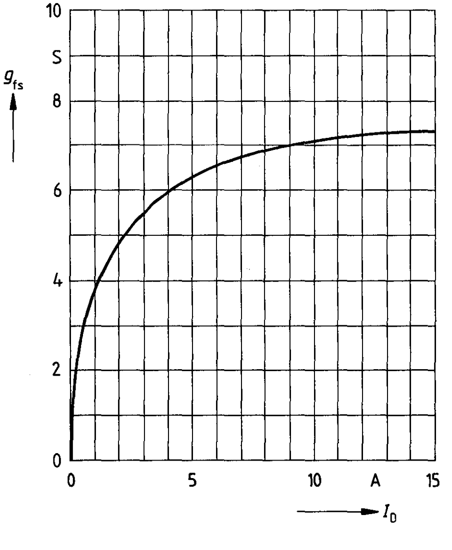
Typical drain-source on-state resistance
$R_{DS\,(on)} = f(I_D)$
parameter: V_{GS}; $T_j = 25\,°C$



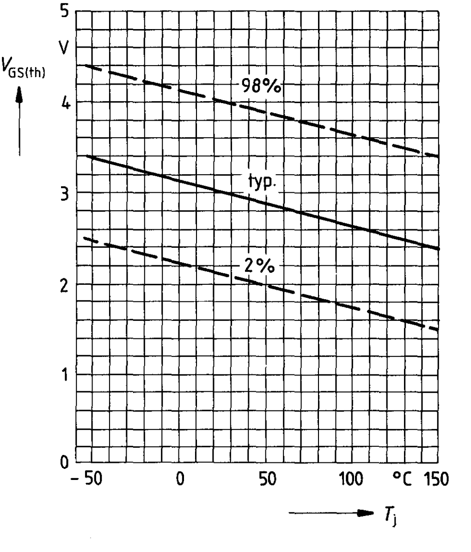
Drain-source on-state resistance
$R_{DS\,(on)} = f(T_j)$
parameter: $I_D = 6{,}5A$, $V_{GS} = 10V$
(spread)



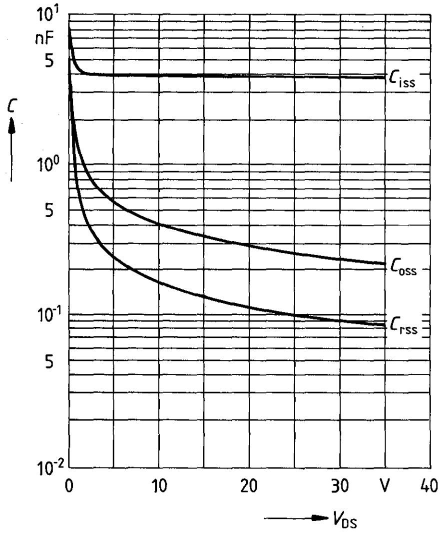
Typical transconductance $g_{fs} = f(I_D)$
parameter: 80 µs pulse test,
$V_{DS} = 25V$, $T_j = 25\,°C$



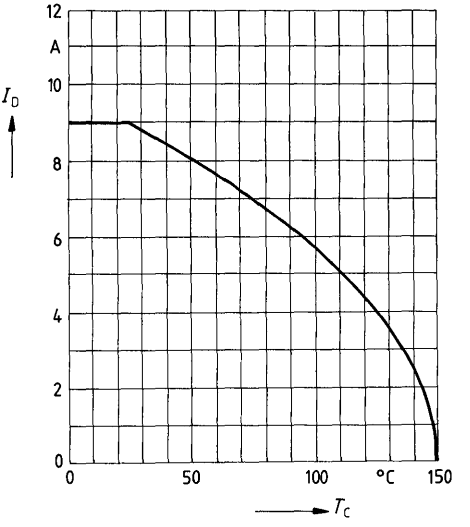
Gate threshold voltage $V_{GS(th)} = f(T_j)$
parameter: $V_{DS} = V_{GS}$, $I_D = 1mA$
(spread)



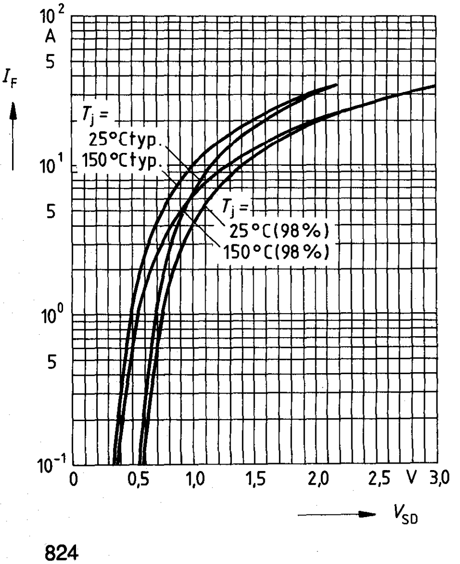
Typical capacitances $C = f(V_{DS})$
parameter: $V_{GS} = 0$, $f = 1\text{MHz}$



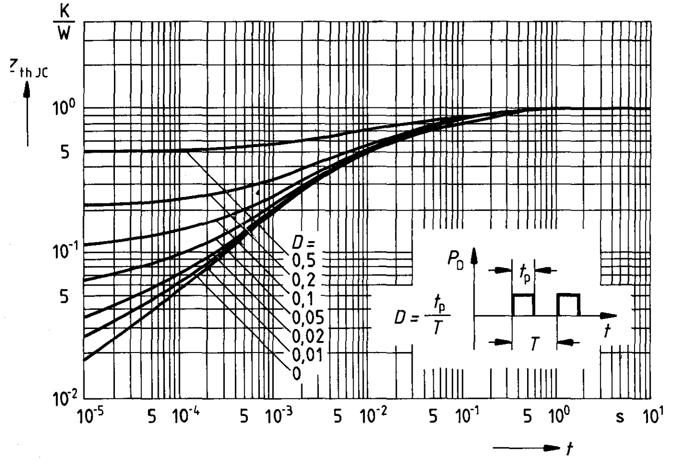
Continuous drain current $I_D = f(T_C)$
parameter: $V_{GS} \geq 10V$



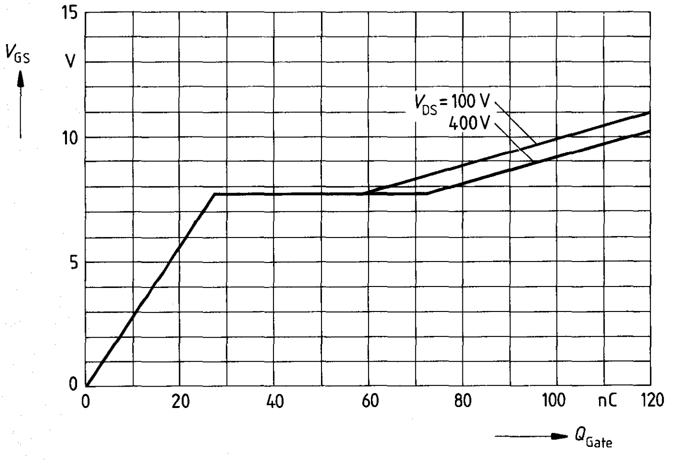
Forward characteristic of reverse diode
$I_F = f(V_{SD})$
parameter: T_j, $t_p = 80\ \mu s$
(spread)



Transient thermal impedance $Z_{thJC} = f(t)$
parameter: $D = t_p / T$



Typical gate-charge $V_{GS} = f(Q_{Gate})$
parameter: $I_{D\,puls} = 14{,}4A$



AC Switch SITAC

BRT 11 . . .
BRT 12

The new SITAC® AC switch (**S**iemens **I**solated **T**riac **AC** switch) in SIPMOS® technology provides a convenient, interface between microprocessor electronics and power electronics with no feedback between power and microprocessor electronics. A current of 2 mA is sufficient in the input IR emitting diode to directly switch loads up to 66 W in the 220 V line. Furthermore, all triacs and thyristors on the market requiring a trigger current up to 3 A can be safely switched. For applications requiring electrical isolation from line voltage the SITAC is preferred as replacement for existing optocouplers because neither auxiliary voltage nor driver transistors are necessary on the power side.
The SITAC is available in a DIP 6 plastic package with or without zero voltage switch (with – BRT 22, without – BRT 11, BRT 12). With built-in zero voltage switch the SITAC is used in AC and three phase current switches whereas regulating units and line current converters use the other version.
Special note should be taken of the SITAC's high critical rates of voltage and current rise of $di/dt_{cr} = 10$ A/µs and $dv/dt_{cr} = 10\,000$ V/µs.

Principle of the SITAC AC switch
The SITAC consists of such familiar components as a GaAs-IR diode (IRED) in the drive section and a photodetector and two back-to-back SCRs on the load side. This provides an electrical isolation of control and power circuits, i. e. one obtains an AC switch activated by infrared radiation. When operated as a simple AC switch, the built-in monolithic zero voltage switch, provides interference-free switching at the line waveform zero crossing (BRT 22).
The high permissible rate of voltage rise of 10 kV/µs can only be attained because the opto-activated SIPMOS triac consists of two back-to-back connected thyristors. Fig. 1b shows the three chips of the SITAC – two power chips and one IRED all housed in a DIP 6 package.

Comparison with other drive methods
Fig. 2 shows the additional expenditure required for other drive methods using optocouplers, trigger transformers or piezo trigger couplers. Compared with these, the SITAC offers a more economical solution (bottom of Fig. 2). Direct microcomputer drive of power components is facilitated by an adequate sensitivity and matching logic level of the SITAC (active microcomputer output = L state; i. e. current flows through the IRED and switches on the SITAC).

SITAC used between microcomputer and AC load (220 V/66 W)
Fig. 3a shows a microcomputer interface consisting of conventional components and Fig. 3b a SITAC circuit.
As steep voltage edges ($dv/dt_{cr} = 10\,000$ V/µs) are permitted at the load the protective *RC* network is omitted. A comparison of circuits shows the considerable cut in required components.

Semiconductor switches to replace mechanical switches
In AC and three phase equipment for higher current or higher switching frequencies, an AC or three phase switch with back-to-back thyristors seems to be more favorable than mechanical switches or power contactors because of
- no moving parts, so maintenance-free and wear-proof (no arcing when switching on or off),
- convenient remote control,
- fast, noiseless operation.

SITAC® is a registered trade mark of Siemens AG

The SITAC as a driver module for power thyristors
In this case the load shall not be switched by the SITAC but serves as a drive device or drive component for powerful thyristors in AC or three phase current switches.
A SITAC and a THYODUL® thyristor module can together form **one** AC switch. AC switch (W 1) and three phase switch (W 3) control AC loads from 5 to 69 kW.

AC switch with thyristors
The AC switch controls thyristors in a way that the load is switched at the instant of the line waveform zero crossing. In this operating mode the thyristor conducts during the whole AC halfwave.
The conductive state can only be interrupted for periods of one or more complete AC halfwaves.
The thyristors are made conductive by triggering at the AC zero crossing. As the gate trigger current flows for only a short time the amount of drive power required is very small.
The SITAC with BRT 22 zero voltage switch in a DIP 6 package triggers the thyristor.
The BRT 22 is designed for a permissible positive or negative repetitive peak off-state voltage of 600 V and an rms on-state current of 0.3 A.
The DC voltage isolation between control and load circuit is 5.3 kV with a leakage path of 8.2 mm.
The interaction of a SITAC and a fully driven THYODUL MTT 40A 06N line commutated module is clearly shown in Fig. 4.
When applying a 5 V DC voltage to the SITAC control circuit the triac is switched.
The gate trigger delay time is 80 μs at 10 V line voltage, followed by a period of 40 μs during which a gate current of 120 mA is supplied to the power thyristor. This (after a total of 120 μs) switches the thyristor and thus the line voltage to the load.
A load of 15 kW AC is switched at a 220 V line voltage with the THYODUL MTT 40A 06N.

Three phase switch with thyristor
For a performance of greater than 5 kW three phase switches are used. Three of the single phase AC switches as described are inserted in the line supply leads. They form the six-pulse, three phase switch shown in Fig. 5. Its mode of operation largely corresponds to that of the AC switch. There are two types of three phase switches:
Switch mode A: The three pairs of thyristors are inserted between the load and neutral conductor Mp.
Switch mode B: The three pairs of thyristors are inserted between the load and phase conductors R, S, T. Each type is intended for a particular kind of application. The three phase load can be connected either to the phase conductors R, S, T or to the neutral conductor Mp, as shown in Fig. 5.
As far as the voltages of the semiconductors are concerned (THYODUL and SITAC) it is, however, most important to establish whether or not the transformer's neutral point is connected to the load.
With the neutral conductor connected and operating, each of the three AC switches operates independently and thyristor voltage class 08 is sufficient, i. e. V_{RRM} and. V_{DRM} of 800 V.
The THYODUL 3 × MTT 40A 08N allows three phase power of 17 to 69 kW depending on the thermal resistance of the heat sink.

Solid state relay, SSR
One important SITAC application is in electronic load switching relays with AC output.
These semiconductor relays are produced in large quantities and are available on the market as modules.

An aluminum plate, onto which a triac or thyristors are mounted separately, provides heat sinking for the power semiconductors.
This metal baseplate can also be used for mounting the SSR on cooling surfaces, e.g. the chassis.
Single-pole SSRs are employed to switch AC loads and they link logic outputs to load current circuits. Switching functions are taken over exclusively by electronic components.
Control and switching circuits are electrically isolated via an optocoupler. The relays are directly driven with 3 to 30 V DC voltage and a power of only a few milliwatt.
They switch on electronically at a zero crossing of the AC voltage and switch off at a point below the triac's holding current.
Triacs and thyristors switch AC voltages of up to 380 V at the load. In this application the SITAC with its zero voltage switch replaces about 12 individual components.
Fewer components cut the size of circuit boards and number of solder joints and increase the life in operation.
Fig. 6a shows a semiconductor relay using discrete components. A semiconductor relay using a triac (600 V/10 A) and the SITAC as driver is shown in Fig. 6b.
The SITAC can be used in a semiconductor relay with either DC input (3 to 30 V DC) or AC input (90 to 250 V AC).

Voltage and current curves of SITAC and THYODUL power thyristor at 10 A load current

Curve 1:	SITAC output voltage (between pins 4 and 6)	V_{Tc}	5 V/Div.
Curve 2:	Power thyristor gate current	I_{ThG}	50 mA/Div.
Curve 3:	Anode – cathode voltage at power thyristor	$V_{ThA\text{-}K}$	5 V/Div.

The SITAC has the following features:

- Fully IC compatible
  The SITAC's high input sensitivity allows its use with CMOS, MOS and bipolar ICs in positive and negative logic. Anode and cathode of the IRED in the SITAC can be freely connected. One side of the diode is connected to the IC output and the other via a series resistor to the supply voltage so that the required input current flows through the IRED in the forward direction with the IC input at L-level. As driver outputs of, say a microprocessor, switch to L-level to initialize further functions (active = low), the IRED conducts in this case and the SITAC is switched on. Additional inverter stages are not necessary.
- High input sensitivity
  2 mA (input current class H)
  5 mA (input current class M)
- High insulation test voltage 5300 V DC between control and load circuit for safe 220 V line operation.
- Wide application range:
  High critical rate of rise of off-state voltage and on-state current of 10000 V/µs and 10 A/µs (T_j = + 25 °C) allow wide application and provide sufficient protection of the SITAC against steep voltage and current edges with fast switching line-commutated loads as well as against possible external interference (e.g. when suddenly applying line voltage or with line interference voltages). Hence *RC* networks at the output are not required.
- Almost interference-free switching with internal zero voltage switch (BRT 22).

Final remarks

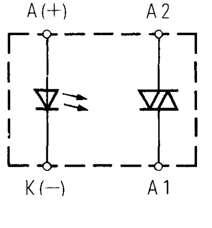
For drive circuits operating between μC electronics and power electronics at the line voltage, a triac such as the SITAC, is a very suitable coupling device with minimum circuitry required. Input and output are electrically isolated by means of an optocoupler. As the SITAC in DIP 6 plastic package offers considerable circuit simplification and cost reduction it will certainly make its mark in the field of power electronics.

Fig. 1 Internal SITAC configuration.

a Principle of IR emitting diode in the input circuit and opto-coupled triac in the output circuit.

b Functions of the three chips inside. The IRED chip is electrically isolated from the other two. Both chips of the output circuits contain each a thyristor and drive electronic devices, i. e. photodetector, amplifying circuits and zero voltage switch (BRT 22). When the individual thyristors are connected back-to-back they function as a triac at the output

a



b

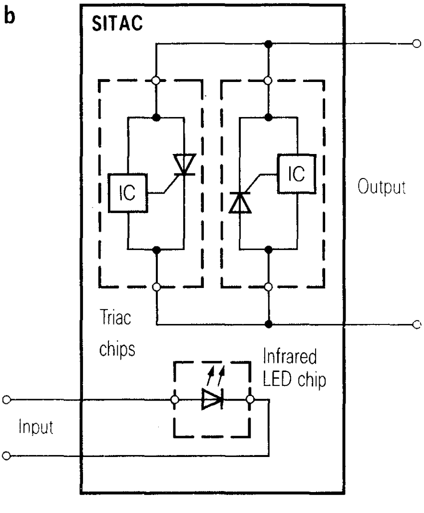


Fig. 2 Various interface circuits between microcomputer and power electronics. Compared with conventional electrically isolated drive methods the SITAC requires the fewest components (bottom circuit)

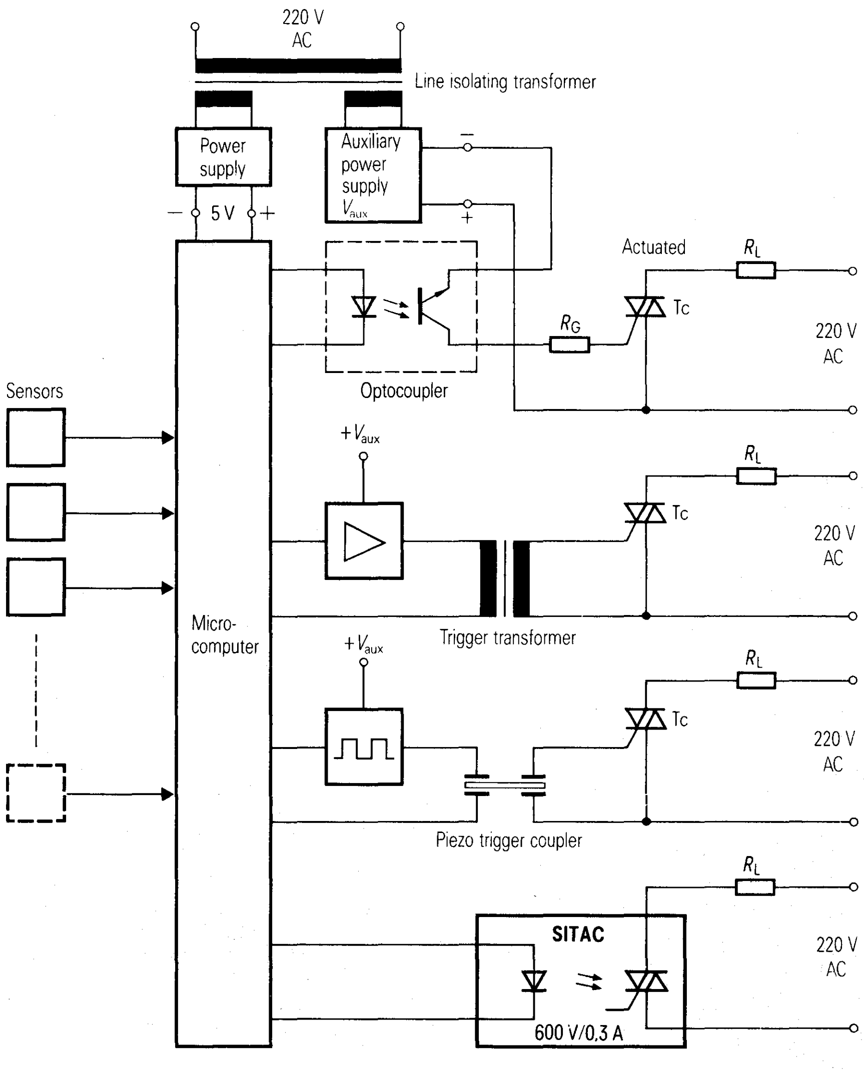


Fig. 3 Conventional μC interface circuit with discrete components and optocoupler (a) as well as μC interface circuit with the SITAC (b)

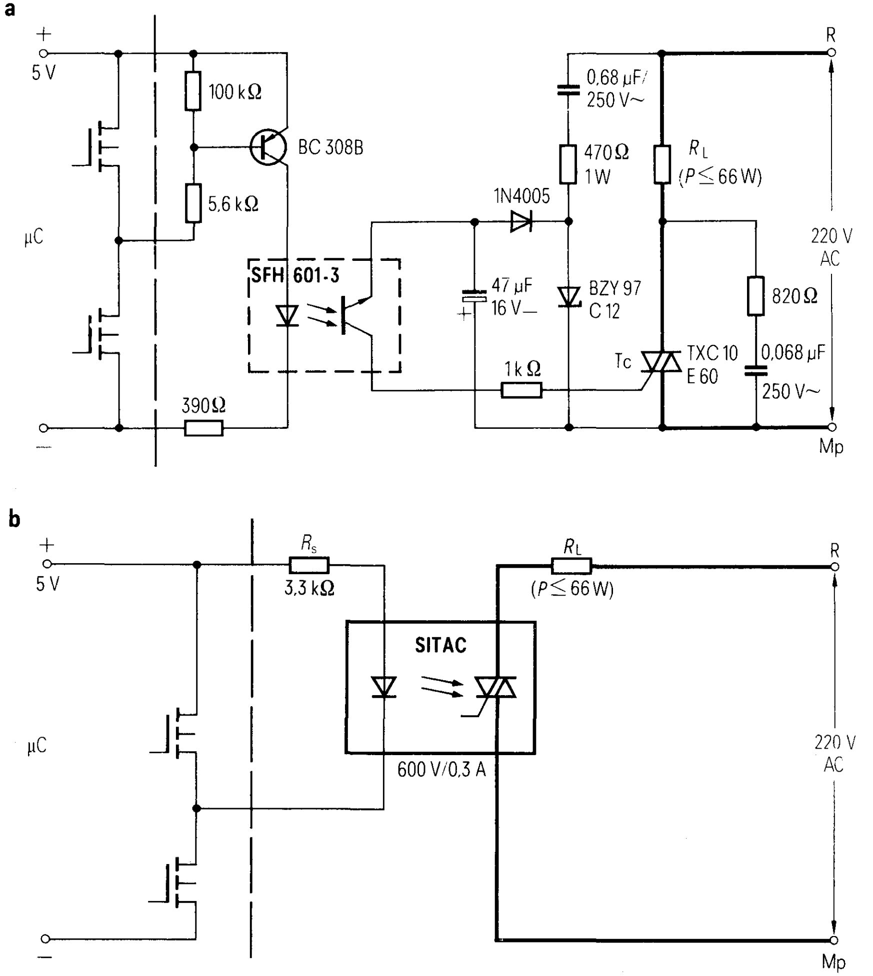
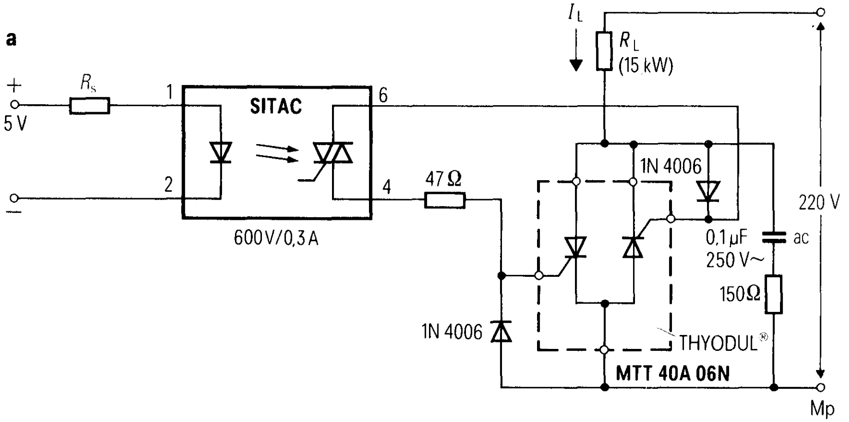


Fig. 4 The SITAC used as a driver for a THYODUL MTT 40A 06N line thyristor module (a) and voltage and current curves (b)

a



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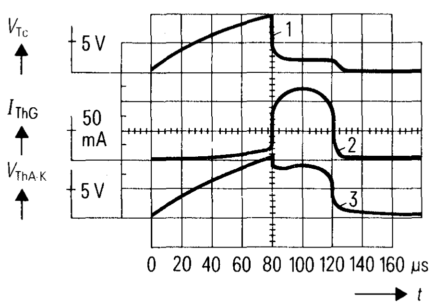


Fig. 5 Circuit of six-pulsed, three-phase current switch using SITAC drivers

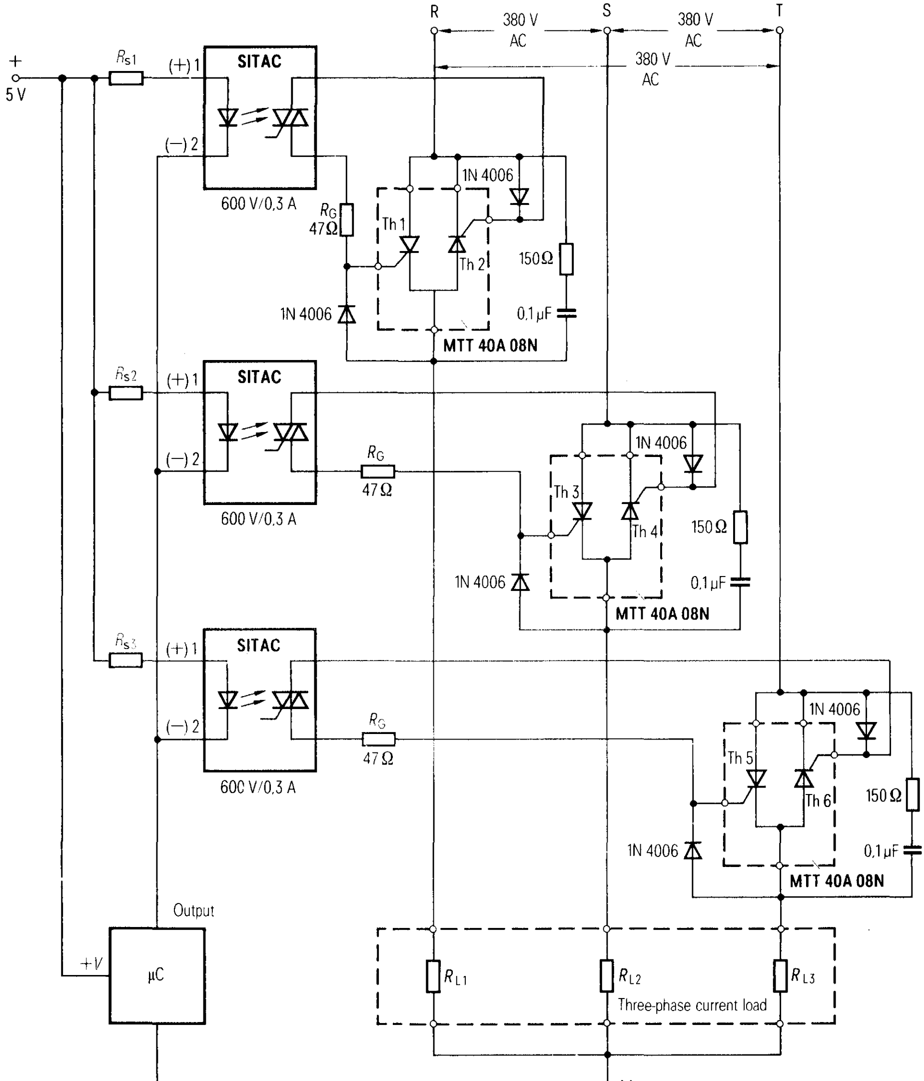
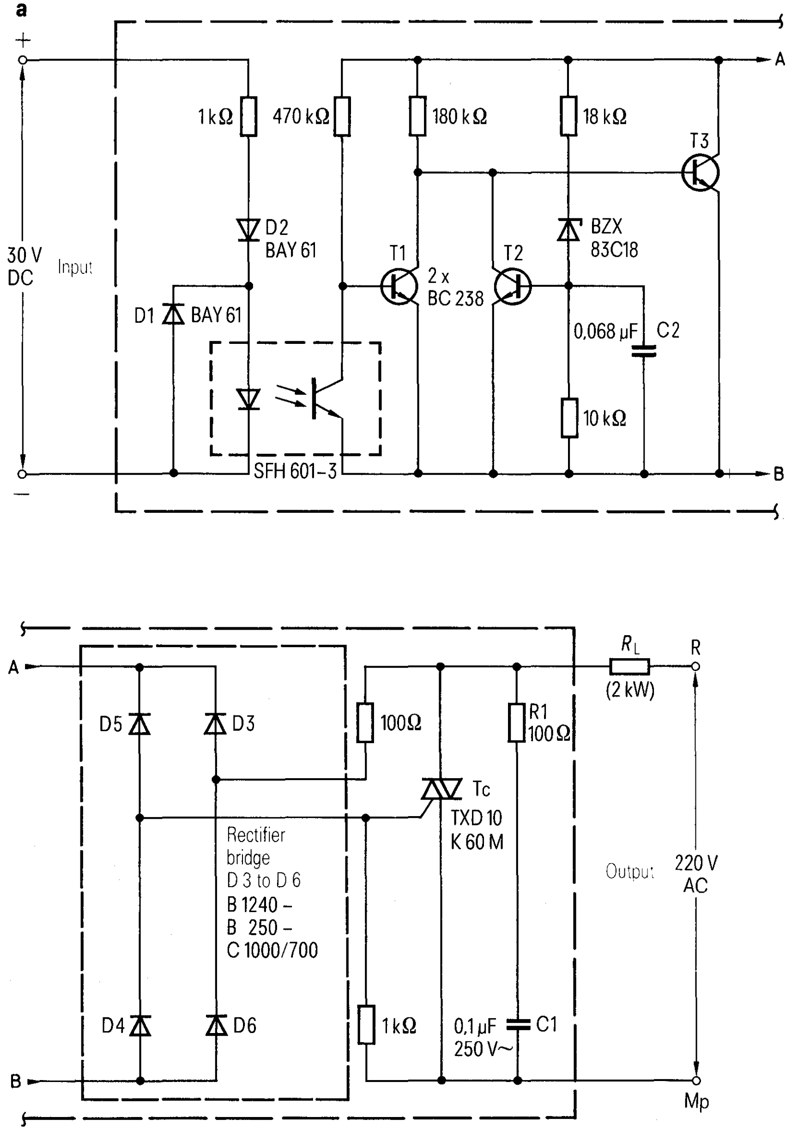


Fig. 6 Conventional design of a Solid State Relay (SSR) with discrete components (a) and simplified structure of an SSR using a SITAC (b)

a



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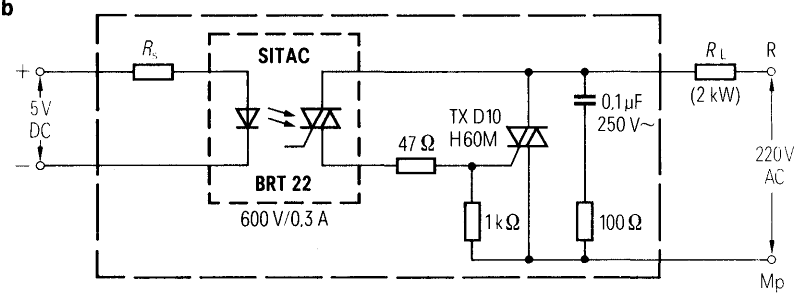
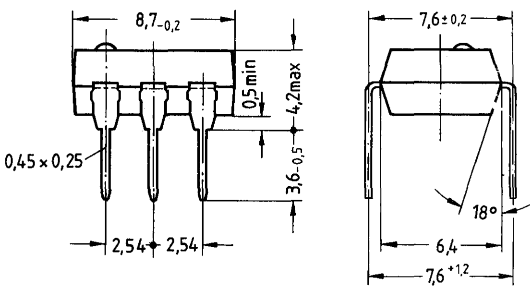

+
5 V
DC
−
R_S
SITAC
BRT 22
600 V/0,3 A
47 Ω
TX D10
H60M
1 kΩ
0,1 µF
250 V~
100 Ω
R_L
(2 kW)
R
220 V
AC
Mp

Application General-purpose switch for alternating current; dc decoupling between input and output circuit.

Description SIPMOS AC switch with GaAs infrared diode and monolithic IC.

Case Plastic package 20A6 in accordance with DIN 41 866 or DIP6 in accordance with JEDEC
Approx. weight 0.6 g



Type	Ordering code
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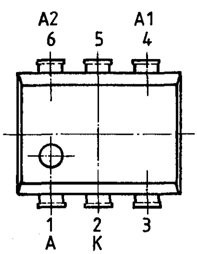
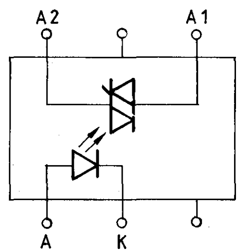
BRT 11 M	C67079-A1000-A10



Dimensions in mm

Output circuit



Input circuit

Output circuit:
4: anode 1
5: undefined, potential A1/A2
6: anode 2

Input circuit:
1: LED, anode (+)
2: LED, cathode (–)
3: n. c.

AC switch ratings
at T_j = 25 °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Operating temperature range	T_j	– 40 . . . + 100 °C
Storage temperature range	T_{stg}	– 40 . . . + 150 °C
Max. power dissipation	P_{tot}	525 mW
Isolation test voltage (t = 1 min)	V_{is}	5300 Vdc
Surface leakage path (input/output circuit)	–	≥ 8,2 mm
Humidity category (DIN 40040)	–	F

Characteristics

Capacitance: Input/output	C	max. 2 pF

Output circuit ratings
at T_j = 25 °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Peak off-state or reverse voltage	V_{DRM}, V_{RRM}	400 V
RMS on-state current, (T_A = 25 °C)	I_{TRMS}	300 mA
Single cycle surge current (50 Hz)	I_{TSM}	3 A
Total power dissipation	P_{tot}	500 mW

Characteristics
(in both directions, unless otherwise specified)

Designation	Symbols	min.	typ.	max.	Unit	Conditions
Critical rate of rise of off-state voltage	dv/dt_{cr}	10000	–	–	V/µs	T_j = 25 °C; V_{DRM}, V_{RRM} = 267 V
		–	2000	–	V/µs	T_j = 80 °C; V_{DRM}, V_{RRM} = 267 V
Critical rate of rise of on-state current	di/dt_{cr}	10	–	–	A/µs	
Max. on-state voltage	V_T	–	–	2,3	V	I_T = 300 mA
Reverse current	I_R	–	–	100	µA	T_j = 100 °C; V_{DRM}, V_{RRM} = 400 V
Max. holding current	I_H	–	0,1	1,0	mA	
Thermal resistance, junction-ambient	$R_{th\,JA}$	–	–	150	K/W	

Input circuit ratings
at T_j = 25 °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Reverse voltage	V_R	6 V
Forward current	I_F	20 mA
Surge forward current ($t \leq 10$ µs)	I_{FSM}	1,5 A
Total power dissipation	P_{tot}	25 mW

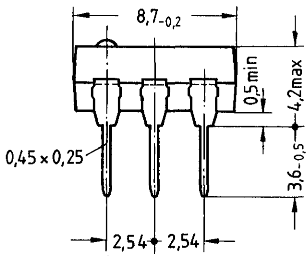
Characteristics

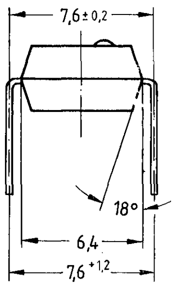
Designation	Symbols	min.	typ.	max.	Unit	Conditions
Gate trigger voltage range	$V_{A1/A2}$	10	–	–	V	$I_F = I_{FT}$
Forward current (LED)	I_{FT}					
Type H		–	–	2,0	mA	
Type M		–	–	5,0	mA	
Forward voltage	V_F	–	–	1,5	V	I_F = 10 mA
Reverse current	I_R	–	–	10	µA	V_R = 6 V
Thermal resistance, junction-ambient	$R_{th\,JA}$	–	–	3000	K/W	

Application General-purpose switch for alternating current; dc decoupling between input and output circuit.

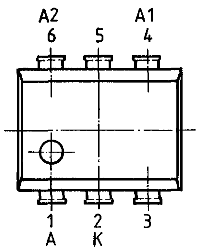
Description SIPMOS AC switch with GaAs infrared diode and monolithic IC.

Case Plastic package 20A6 in accordance with DIN 41 866 or DIP6 in accordance with JEDEC
Approx. weight 0.6 g



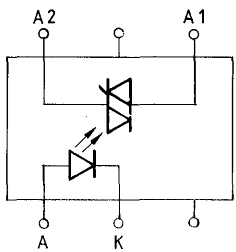


Type	Ordering code
BRT 12 H	C67079-A1001-A6
BRT 12 M	C67079-A1001-A10



Dimensions in mm

Output circuit



Input circuit

Output circuit:
4: anode 1
5: undefined, potential A1/A2
6: anode 2

Input circuit:
1: LED, anode (+)
2: LED, cathode (−)
3: n. c.

AC switch ratings

at T_j = 25 °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Operating temperature range	T_j	−40 ... + 100 °C
Storage temperature range	T_{stg}	−40 ... + 150 °C
Max. power dissipation	P_{tot}	525 mW
Isolation test voltage (t = 1 min)	V_{is}	5300 Vdc
Surface leakage path (input/output circuit)	–	≥ 8,2 mm
Humidity category (DIN 40040)	–	F

Characteristics

Capacitance: Input/output	C	max. 2 pF

Output circuit ratings
at $T_j = 25\ °C$ (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Peak off-state or reverse voltage	V_{DRM}, V_{RRM}	600 V
RMS on-state current ($T_A = 25\ °C$)	I_{TRMS}	300 mA
Single cycle surge current (50 Hz)	I_{TSM}	3 A
Total power dissipation	P_{tot}	500 mW

Characteristics
(in both directions, unless otherwise specified)

Designation	Symbols	min.	typ.	max.	Unit	Conditions
Critical rate of rise of off-state voltage	dv/dt_{cr}	10000	–	–	V/µs	$T_j = 25\ °C$ } V_{DRM}, $V_{RRM} = 400$ V
		–	2000	–	V/µs	$T_j = 80\ °C$ } V_{DRM}, $V_{RRM} = 400$ V
Critical rate of rise of on-state current	di/dt_{cr}	10	–	–	A/µs	
Max.on-state voltage	V_T	–	–	2,3	V	$I_T = 300$ mA
Reverse current	I_R	–	–	100	µA	$T_j = 100\ °C$; V_{DRM}, $V_{RRM} = 600$ V
Max. holding current	I_H	–	0,1	1,0	mA	
Thermal resistance, junction-ambient	$R_{th\ JA}$	–	–	150	K/W	

Input circuit ratings
at $T_j = 25\ °C$ (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Reverse voltage	V_R	6 V
Forward current	I_F	20 mA
Surge forward current ($t \leq 10$ µs)	I_{FSM}	1,5 A
Total power dissipation	P_{tot}	25 mW

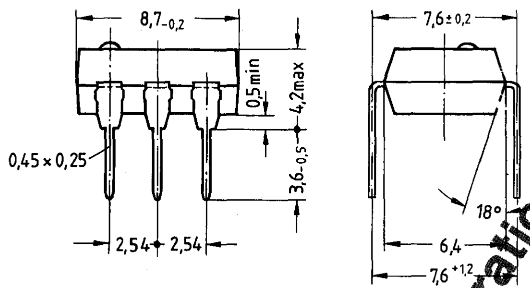
Characteristics

Designation	Symbols	min.	typ.	max.	Unit	Conditions
Gate trigger voltage range	$V_{A1/A2}$	10	–	–	V	$I_F = I_{FT}$
Forward current (LED)	I_{FT}					
Type H		–	–	2,0	mA	
Type M		–	–	5,0	mA	
Forward voltage	V_F	–	–	1,5	V	$I_F = 10$ mA
Reverse current	I_R	–	–	10	µA	$V_R = 6$ V
Thermal resistance, junction-ambient	$R_{th\ JA}$	–	–	3000	K/W	

Application General-purpose switch for alternating current; dc decoupling between input and output circuit.

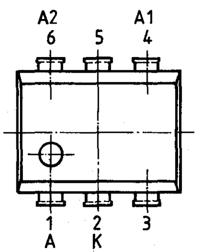
Description SIPMOS AC switch with GaAs infrared diode and monolithic IC.

Case Plastic package 20A6 in accordance with DIN 41866 or DIP6 in accordance with JEDEC
Approx. weight 0.6 g



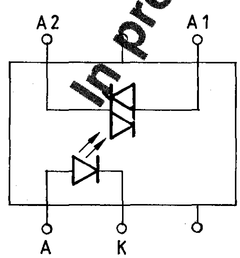
In preparation

Type	Ordering code
BRT 21 H	C67079-A1020-A6
BRT 21 M	C67079-A1020-A10



Dimensions in mm

Output circuit



Input circuit

Output circuit:
4: anode 1
5: undefined, potential A1/A2
6: anode 2

Input circuit:
1: LED, anode (+)
2: LED, cathode (–)
3: n. c.

AC switch ratings
at T_j = 25 °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Operating temperature range	T_j	– 40 . . . + 100 °C
Storage temperature range	T_{stg}	– 40 . . . + 150 °C
Max. power dissipation	P_{tot}	525 mW
Isolation test voltage (t = 1 min)	V_{is}	5300 Vdc
Surface leakage path (input/output circuit)	–	≥ 8,2 mm
Humidity category (DIN 40040)	–	F

Characteristics

Capacitance: Input/output	C	max. 2 pF

Output circuit ratings
at $T_j = 25$ °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Peak off-state or reverse voltage	V_{DRM}, V_{RRM}	400 V
RMS on-state current ($T_A = 25$ °C)	I_{TRMS}	300 mA
Single cycle surge current (50 Hz)	I_{TSM}	3 A
Total power dissipation	P_{tot}	500 mW

Characteristics
(in both directions, unless otherwise specified)

Designation	Symbols	min.	typ.	max.	Unit	Conditions
Critical rate of rise of off-state voltage	dv/dt_{cr}	10000	–	–	V/µs	$T_j = 25$ °C; V_{DRM}, $V_{RRM} = 267$ V
		–	2000	–	V/µs	$T_j = 80$ °C; V_{DRM}, $V_{RRM} = 267$ V
Critical rate of rise of on-state current	di/dt_{cr}	10	–	–	A/µs	
Max.on-state voltage	V_T	–	–	2,3	V	$I_T = 300$ mA
Reverse current	I_R	–	–	100	µA	$T_j = 100$ °C; V_{DRM}, $V_{RRM} = 400$ V
Max. holding current	I_H	–	0,1	1,0	mA	
Thermal resistance, junction-ambient	$R_{th\,JA}$	–	–	150	K/W	

In preparation

Input circuit ratings
at $T_j = 25$ °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Reverse voltage	V_R	6 V
Forward current	I_F	20 mA
Surge forward current ($t \leq 10$ µs)	I_{FSM}	1,5 A
Total power dissipation	P_{tot}	25 mW

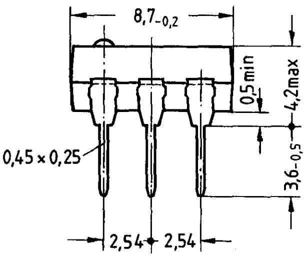
Characteristics

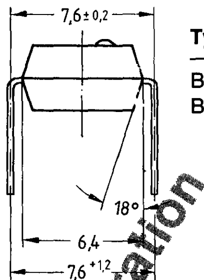
Designation	Symbols	min.	typ.	max.	Unit	Conditions
Gate trigger voltage range	$V_{A1/A2}$	–	10	–	V	$I_F = I_{FT}$
Forward current (LED)	I_{FT}					
Type H		–	–	2,0	mA	
Type M		–	–	5,0	mA	
Forward voltage	V_F	–	–	1,5	V	$I_F = 10$ mA
Reverse current	I_R	–	–	10	µA	$V_R = 6$ V
Thermal resistance, junction-ambient	$R_{th\,JA}$	–	–	3000	K/W	

Application General-purpose switch for alternating current; dc decoupling between input and output circuit.

Description SIPMOS AC switch with GaAs infrared diode and monolithic IC.

Case Plastic package 20A6 in accordance with DIN 41866 or DIP6 in accordance with JEDEC
Approx. weight 0.6 g

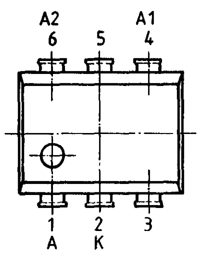


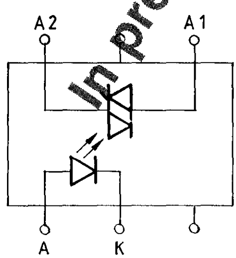


Type	Ordering code
BRT 22 H	C67079-A1021-A6
BRT 22 M	C67079-A1021-A10

In preparation

Output circuit





Dimensions in mm

Input circuit

Output circuit:
4: anode 1
5: undefined, potential A1/A2
6: anode 2

Input circuit:
1: LED, anode (+)
2: LED, cathode (–)
3: n. c.

AC switch ratings
at T_j = 25 °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Operating temperature range	T_j	–40 . . . + 100 °C
Storage temperature range	T_{stg}	–40 . . . + 150 °C
Max. power dissipation	P_{tot}	525 mW
Isolation test voltage (t = 1 min)	V_{is}	5300 Vdc
Surface leakage path (input/output circuit)	–	≥ 8,2 mm
Humidity category (DIN 40040)	–	F

Characteristics

Capacitance: Input/output	C	max. 2 pF

Output circuit ratings
at T_j = 25 °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Peak off-state or reverse voltage	V_{DRM}, V_{RRM}	600 V
RMS on-state current (T_A = 25 °C)	I_{TRMS}	300 mA
Single cycle surge current (50 Hz)	I_{TSM}	3 A
Total power dissipation	P_{tot}	500 mW

Characteristics
(in both directions, unless otherwise specified)

Designation	Symbols	min.	typ.	max.	Unit	Conditions
Critical rate of rise of off-state voltage	dv/dt_{cr}	10000	–	–	V/µs	T_j = 25 °C; V_{DRM}, V_{RRM} = 400 V
		–	2000	–	V/µs	T_j = 80 °C; V_{DRM}, V_{RRM} = 400 V
Critical rate of rise of on-state current	di/dt_{cr}	10	–	–	A/µs	
Max.on-state voltage	V_T	–	–	2,3	V	I_T = 300 mA
Reverse current	I_R	–	–	100	µA	T_j = 100 °C; V_{DRM}, V_{RRM} = 600 V
Max. holding current	I_H	–	0,1	1,0	mA	
Thermal resistance, junction-ambient	$R_{th\,JA}$	–	–	150	K/W	

In preparation

Input circuit ratings
at T_j = 25 °C (unless otherwise specified)

Maximum ratings

Designation	Symbols	Ratings
Reverse voltage	V_R	6 V
Forward current	I_F	20 mA
Surge forward current ($t \leq 10$ µs)	I_{FSM}	1,5 A
Total power dissipation	P_{tot}	25 mW

Characteristics

Designation	Symbols	min.	typ.	max.	Unit	Conditions
Gate trigger voltage range	$V_{A1/A2}$	–	10	–	V	$I_F = I_{FT}$
Forward current (LED)	I_{FT}					
Type H		–	–	2,0	mA	
Type M		–	–	5,0	mA	
Forward voltage	V_F	–	–	1,5	V	I_F = 10 mA
Reverse current	I_R	–	–	10	µA	V_R = 6 V
Thermal resistance, junction-ambient	$R_{th\,JA}$	–	–	3000	K/W	

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