Silicon Systems Communication Products 1991 Data Book

INTEGRATED CIRCUITS FOR

COMMUNICATION PRODUCTS

1991 Data Book

silicon systems®

Table of Contents

Advanced and Preliminary Information
In this data book the following conventions are used in designating a data sheet "Advanced" or "Preliminary."

Advance Information–
Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Preliminary Data–
Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Product Index

DISCONTINUED PARTS LIST

The following parts are no longer supplied or supported by Silicon Systems. Please note alternate sources.

Part #	Alternate Source	No Alternate Source
22100	RCA	SSI 291 (use SSI K-Series)
22101/102	RCA	SSI 213 (use SSI 73M3522)
22106	RCA	SSI 263A (SC02)
SSI 32C452A	SSI 32C452	SSI 169 (SC01)
SSI 32D536	SSI 32D5362	SSI 32D450A
SSI 32D537	SSI 32D5371/2	SSI 32P542
6020 & 60XX	Plessey Semiconductor	SSI 73M3522
any 60 number	(516) 543-0200	SSI 78P8050
(A/D, D/A convertors)		SSI 78P8060

Numerical Index

Silicon Systems' Communication Products Capabilities

Silicon Systems offers a broad line of standard integrated circuits aimed at providing cost effective system solutions for many mixed signal communications equipment problems. For those manufacturers that have special mixed signal requirements we offer custom or customized integrated circuit capability. The heart of Silicon Systems' efforts in the communications market is the continuous expansion of circuit technology. Our pioneering work with CMOS switched capacitor filters enabled us to develop the first integrated DTMF receiver which led to our industry standard DTMF family. This CMOS switched capacitor technology has been used in many non-DTMF filtering functions of other Silicon Systems integrated circuits, most notably, our family of modem products.

The pioneering continues as our mixed signal technology expansion has led us to develop DSP techniques to supplement traditional analog signal processing techniques. The SSI 73K224 V.22bis modem is one example of how the use of this DSP technology has been used with analog signalling processing to optimize die size so that a single IC modem solution was possible. Our highly integrated system solutions demonstrate not only technological leadership in our own semiconductor field but also the ability to anticipate the growing needs of the fast-paced communications marketplace.

Here are a few examples of custom and standard ICs that demonstrate our broad communications IC capabilities.

CMOS

Integrated Circuit Function	Application
DTMF Receiver	Decodes Touch-Tone® Telephone Signals
One-chip Modems	Data Transmission
Error Control and Compression	Data Transmission
Remote Transmitter	Telephone Ans. Machine
Modem AFE	V.32 Data Transmission
Analog Crosspoint Switch	PBX's
Video Processor	Infrared Video System
16 Channel Switching Matrix	Bank Comm. Systems
Digital Loop Detector	Traffic Signal Control
ΣΔ Convertor Plus DSP and Control AFE	High Speed Data Transmission
DSP Based Filter	Programmable Filters
Satellite Descrambler	CATV Receiver
Modem AFE	19.2 Kbit/s Data Transmission
DSP-based Telemetry	Watt Hour Meter

BIPOLAR

Integrated Circuit Function	Application
Audio System Receiver	Telephone Answering Machine
VHF/UHF Gain Mixer	Radio Receiver
Digital Receiver	Remote Control
PCM Encoder/Decoder	Telecom System
Digital Correlator/Integrator	Radio Telescope
DS-1 Line Interface	T1 Channel Banks Multiplexers
LAN Transceiver	IEEE 802.3 Ethernet LAN
Modem AFE	1200 bit/s Data Transmission
DS-3 Line Interface	T3 Sonet

PROCESSES

Three **bipolar** processes are used to optimize cost/performance. Key features include polysilicon emitter structures, base and collector plugs, double metal, f_T from 3 to 7.5 GHz and metal-nitride-poly capacitors.

There are also three **CMOS** processes in production for cost/performance optimization. Key features include poly-poly capacitors, poly resistors, operating voltages from 5 to 12 volt, double poly and double metal.

PRODUCT QUALITY

Silicon Systems' quality goals will be given the highest priority in the 90s. The mission to achieve total customer satisfaction through quality excellence forms the basis of The Silicon Systems Master Quality Plan. The Quality Mission further sets its sites on products to have fewer than 1 ppm defective by the end of the decade through an ongoing process of specified continuous improvement in every phase of its operation.

CUSTOMER SERVICE

Silicon Systems provides individualized service for every customer. Our Customer Service Department is dedicated to responsive service and is staffed with personnel trained to consider our customers' needs as their most urgent requirement. Product quality and service are both viewed as cornerstones for Silicon Systems' continued growth.

Communication IC Selector Guide

Silicon Systems Device Number	Operating Modes 212A	V.22, V.21	V.22bis	Features	Power Supply (V)	Available Packages
K-SERIES SINGLE CHIP MODEM FAMILY						
SSI 73K212	✗			300, 1200 bit/s, Bell 212A/103 compatible	12	28, 22 DIP, 28 PLCC
SSI 73K212L	✗			Low power 73K212, 40 mW, +5V single supply	5	28, 22 DIP, 28 PLCC
SSI 73K212U	✗			73K212 with integral 16C450 UART	5	40 DIP
SSI 73K221		✗		600, 1200 bit/s, CCITT V.22/V.21 compatible	12	28, 22 DIP, 28 PLCC
SSI 73K221L		✗		Low power 73K221, 40 mW, +5V single supply	5	28, 22 DIP, 28 PLCC
SSI 73K221U		✗		73K221 with integral 16C450 UART	5	40 DIP
SSI 73K222	✗	✗		300, 600, 1200 bit/s Bell 212/103, CCITT V.22/V.21	12	28, 22 DIP, 28 PLCC
SSI 73K222L	✗	✗		Low power 73K222, 40 mW, +5V single supply	5	28, 22 DIP, 28 PLCC
SSI 73K222U	✗	✗		73K222 with integral 16C450 UART	5	40 DIP
SSI 73K224	✗	✗	✗	300, 1200, 2400 bit/s, V.22bis, V.22, V.21 Bell 212/103 compatible	12	28, 44 PLCC
SSI 73K224L	✗	✗	✗	Low power 73K224, 100mW,+5V single supply	5	28, 44 PLCC
SSI 73K302L	✗			0-1200 bit/s		
SSI 73K321L				0-1200 bit/s, V.23, V.21 modes	5	28, 22 DIP, 28 PLCC
SSI 73K322L		✗		73K221 w/ V.23 mode (European applications)	5	28, 22 DIP, 28 PLCC
SSI 73K324L		✗	✗	300, 1200, 2400 bit/s, V.22bis, V.22, V.21 w/ V.23 mode (European applications)		
MODEM PROTOCOL & BUS INTERFACE PRODUCTS						
SSI 73D2180	✗	✗		1200 bit/s low power "AT" modem device set for integral applications	5	40 DIP, 44 PLCC
SSI 73D2240	✗	✗	✗	2400 bit/s low power "AT" modem device set	5	28, 40 DIP, 32, 44 PLCC
SSI 73D2404	✗	✗	✗	2400 bit/s "AT" modem device set	±5	28, 40 DIP, 28, 44 PLCC
SSI 73M450				16C450 pin compatible UART	5	40 DIP, 44 PLCC
SSI 73M450F				Fast version of SSI 73M450 UART	5	40 DIP, 44 PLCC
SSI 73M1450				28-pin version of SSI 73M450	5	28 DIP, 28 PLCC
SSI 73M2450				Adds µPRST function to SSI 73M1450	5	28 DIP, 28 PLCC
SSI 73M550				16C550 pin compatible UART	5	40 DIP, 44 PLCC
SSI 73M550F				Fast version of SSI 73M550 UART	5	40 DIP, 44 PLCC
SSI 73M1550				28-pin version of SSI 73M550	5	28 DIP, 28 PLCC
SSI 73M2550				Adds µPRST function to SSI 73M1550	5	28 DIP, 28 PLCC

Silicon Systems Device Number	Circuit Function	Features	Power Supply	Available Packages
SPECIAL MODEM PRODUCTS				
SSI 73M214	2400 bit/s Modem Filter	V.22bis/V.22/V.21, Bell 212/103 modes	±5V	28 DIP, 28 PLCC
SSI 73M223	1200 bit/s Modem	Compact HDX V.23 modem	5V	16 DIP
SSI 73M3522	1200 bit/s Modem Filter	High performance filter for V.22/212A modes	±5V	16 DIP
TONE SIGNALLING PRODUCTS				
SSI 75T201	Integrated DTMF Receiver	Binary of 2-of-8 output	12V	22 DIP
SSI 75T202	Int. DTMF Receiver	Low power, binary output	5V	18 DIP
SSI 75T203	Int. DTMF Receiver	Early detect, binary output	5V	18 DIP
SSI 75T204	Int. DTMF Receiver	Low power, binary output	5V	14 DIP, 16 SO
SSI 75T2089	Int. DTMF Transceiver	Generator & receiver, µP interface	5V	22 DIP
SSI 75T2090	Int. DTMF Transceiver	Like 75T2089 w/ call progress detect	5V	22 DIP
SSI 75T2091	Int. DTMF Transceiver	Like 75T2090 w/ early detect	5V	28 DIP, 28 PLCC
SSI 75T957	Int. DTMF Receiver	Early detect, dial tone reject	5V	22 DIP, 24 SO
SSI 75T980	Imprecise Call Progress Det.	Energy detect in 305-640 Hz band, Teltone	5V	8 DIP
SSI 75T981	Precise Call Progress Det.	Det. 350, 400, 440, 480 Hz, Teltone 2nd source	5V	22 DIP
SSI 75T982	Precise Call Progress Det.	Det. 350, 440, 480, 620 Hz, Teltone 2nd source	5V	22 DIP
TELEPHONY / DIGITAL TELECOM				
SSI 78P233	DS-1 Line Interface	T1 clock data recovery, transmit equalization	5V	24 DIP, SDIP, SO
SSI 78P234	2048 kbit/s PCM Interface	Receive clock & data recovery, transmit drivers	5V	20 DIP, SO
SSI 78A093A/B	12x8x1 Crosspoint Switch	Low ON resistance, two versions	5-12V	40 DIP, 44 PLCC
SSI 78A207	Integrated MF Receiver	Detects central office toll signals	5V	20 DIP
SSI 78A400	4-Wire Loopback	2713 Hz detector, failsafe timeouts	±5V	16 DIP, 18 SO
SSI 78A420	4-Wire Loopback	As above w/ gain/loss block	±5V	22 DIP

Section

1

K-SERIES MODEM FAMILY

Silicon Systems K-Series Family of One-Chip Modems

Silicon Systems is a leader in the design and manufacturing of CMOS VLSI modems, and has been providing innovative solutions to the communication industry for more than ten years. Currently, Silicon Systems offers the most extensive line of one-chip modem ICs available, with high-performance, cost-effective designs suitable for a wide range of applications. Silicon Systems' fully compatible modem IC family has redefined the modem IC as a universal component which can be easily integrated into any system. Designs can be upgraded to meet different standards and speeds by simply substituting one K-Series IC for another. Using a K-Series family modem IC in your application eliminates product obsolesence, and minimizes development costs.

The Silicon Systems modem IC family consists of four basic products:

1. The SSI 73K222, a multi-mode device which combines both Bell 212A/103 and V.22/V.21 capability in one chip, with operating modes at 0 - 30, 600 and 1200 bit/s.

2. The SSI 73K222U which combines the functionality of the 73K222 with the industry standard 16C450 UART.

3. The SSI 73K224, a major technological breakthrough which provides 2400 bit/s V.22bis operation in addition to V.22/V.21 and Bell 212A/103 modes in a single IC.

4. The SSI 73K322 provides CCITT V.22/V.21 plus V.23 Videotex modes.

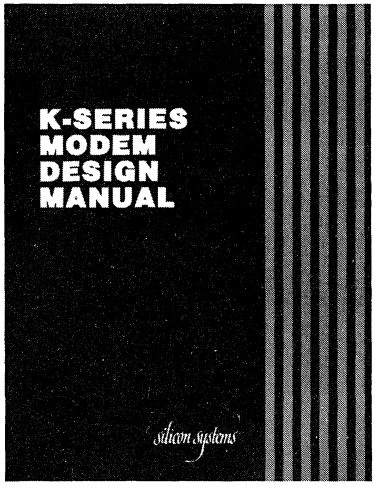
New additions to Silicon Systems' modem IC family extend the available operating modes and provide features which greatly simplify integral modem design. The SSI 73K324 offers V.22bis, V.22/V.21 and V.23 operating modes on one chip. These products dramatically reduce external circuitry required for dedicated integral modem designs.

Silicon Systems' one-chip modem IC products represent technical achievements unmatched in the industry. An advanced Digital Signal Processor resides on the same chip with sophisticated analog circuitry in the SSI 73K224 and SSI 73K324 products. "U" versions of the K-Series devices integrate an industry standard UART with full modem capability on a single chip. In addition, an innovative bus structure makes a separate controller unnecessary in dedicated integral designs. All K-Series devices are available in low-power versions. This feature allows optimal performance with single +5V supply operation and is unique to Silicon Systems' products.

Silicon Systems' single-chip modem IC family is designed to be the most effective solution for a wide variety of modem applications. The products provide for a full range of communications standards and speeds up to 2400 bit/s. Moreover, features can be extended to include additional modes and higher operating speeds without impacting existing designs. Take advantage of these capabilities. Design for tomorrow's needs today by using Silicon Systems' K-Series modem IC family.

K-Series Modem Design Manual

The Silicon Systems K-Series Modem Design Manual contains a large body of application literature for the K-Series family of single chip modem products. This manual is intended as a tutorial for those users who may be designing with modems for the first time, and also as a helpful guide for more experienced modem designers.



The K-Series Modem Design Manual is available through our worldwide network of representatives and distributors.

SSI 73K212/K212L
Bell 212A/103
Single-Chip Modem

1

July, 1990

DESCRIPTION

The SSI 73K212 is a highly integrated single-chip modem IC which provides the functions needed to construct a typical Bell 212A full–duplex modem. Using an advanced CMOS process that integrates analog, digital and switched–capacitor filter functions on a single substrate, the SSI 73K212 offers excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K212L low power version of the SSI 73K212 provides identical performance and features, but operates from a single +5 volt supply with substantially lower power consumption.

The SSI 73K212 includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes and a DTMF dialer. This device supports all Bell 212A modes of operation allowing both synchronous and asychronous communications.

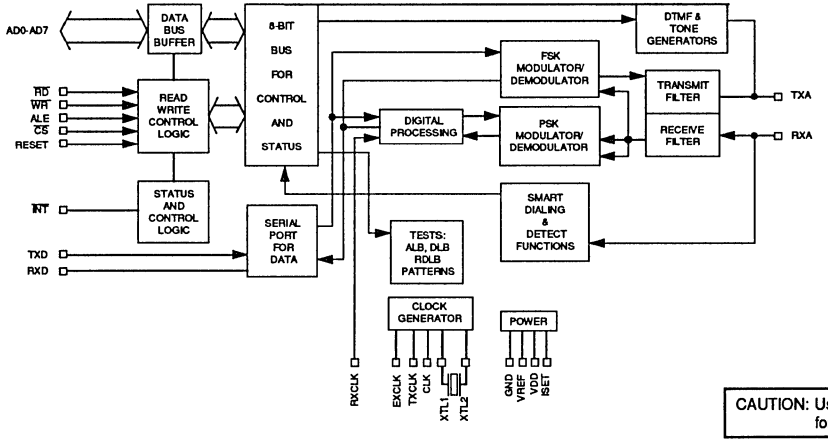
Test features such as analog loop, digital loop, and remote digital loopback are provided. Internal pattern generators are also included for self-testing. The SSI73K212 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors

(Continued)

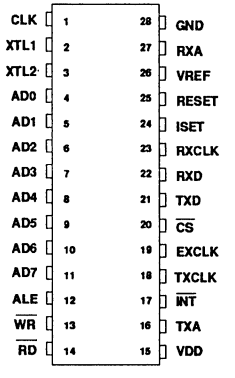
FEATURES

- **One-chip Bell 212A and 103 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel (28-pin DIP) microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone and long loop detectors**
- **DTMF generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **Space efficient 22- or 28-pin DIP packages**
- **CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V**
- **Single +5 volt (73K212L) or +12 volt (73K212) versions**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

(80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K212 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bps data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level convertor for a typical system. The SSI 73K212 is part of SSi's K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K212 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data within a 0.01% rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bit/s ± .01% (± .01% is the required synchronous data rate accuracy).

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least $2 \cdot N + 3$ bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K212 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K212 uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In the Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and

space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 mode.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K212 control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal, (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (73K212) or 5V ±10% (73K212L). Bypass with .1 and 22 µF capacitors to ground.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low during the falling edge of ALE on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K212 internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K212 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K212 that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K212 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200 bit/s +1%, -2.5%.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. Consult crystal manufacturer for proper valves. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. In parallel mode the address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K212 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1	DTMF0
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	0	0						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
				0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1	DTMF0
		RXD PIN 0=NORMAL 1=TRI STATE		0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			
ID REGISTER ID	110	ID BIT 1	ID BIT 0	ID					
		00X 73K212 or 73K322 01X 73K221 or 73K302L 10X 73K222 110 73K224 111 73K324L							

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 stop or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used, must be written as "0."

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrier at the TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency on reset.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4	Bypass Scrambler	0	Selects normal operation. DPSK transmit data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	LONG LOOP	0	Indicates normal received signal.
		1	Indicates low received signal.
D1	CALL PROGRESS DETECT	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.
D2	ANSWER TONE DETECT	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone. The device must be in originate mode for detection of answer tone.
D3	CARRIER DETECT	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	UNSCRAM-BLED MARK	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	RECEIVE DATA		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	TRANSMIT DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high (with Transmit Enable, CR0-D1). TX DTMF overrides all other transmit functions.
D5	TRANSMIT ANSWER TONE	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.
D7	RXD OUTPUT CONTROL	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal, weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID					

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212(L) or 73K322L
		0 1 X	SSI 73K221(L) or 73K302L
		1 0 X	SSI 73K222(L)
		1 1 0	SSI 73K224L
		1 1 1	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(External to GND)	0.1			µF
VDD Bypass capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

ELECTRICAL SPECIFICATIONS (Continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX=1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATION (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to + 85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10.0	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low-Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High-Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, DPSK mode	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
- 10 dB loss in the Transmit path to the line.
- 9 dB gain in the Receive path from the line.

5V Version
- 0 dB loss in the Transmit path to the line.
- 2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATION (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	In FSK mode	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
TXA pin Output Impedance			200	300	Ω
Output load	TXA pin; FSK Single Tone out for THD = -50 db in .3 to 3.4 KHz	10		 50	KΩ pF
Spurious Freq. Comp.	Frequency = 76.8 KHz			-39	dBm0
	Frequency = 153.6 KHz			-45	dBm0
Clock Noise	TXA pin; 76.8 KHz				
5V Version (73K212L)				1.0	mVrms
12V Version (73K212)				2.0	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATION (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

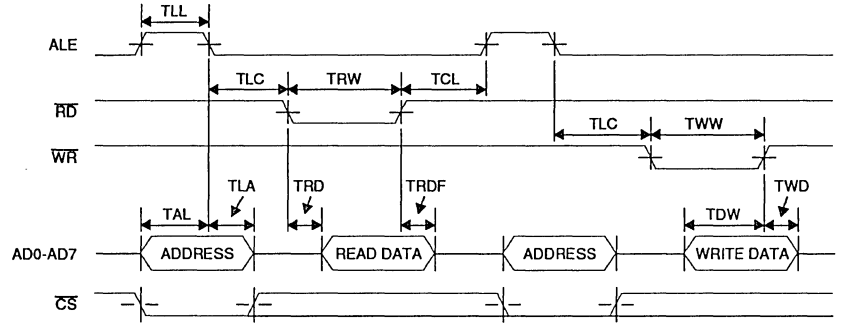
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE low	20			ns
TLC	ALE low to $\overline{RD}/\overline{WR}$ low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE high	10			ns
TRD	Data out from $\overline{RD}$ low	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ high	0		80	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000*	ns
TDW	Data setup before $\overline{WR}$ high	150			ns
TWD	Data hold after $\overline{WR}$ high	20			ns
TCKD	Data out after EXCLK low			200	ns
TCKW	$\overline{WR}$ after EXCLK low	150			ns
TDCK	Data setup before EXCLK low	150			ns
TAC	Address setup before control**	50			ns
TCA	Address hold after control**	50			ns
TWH	Data Hold after EXCLK	20			ns

* Maximum time applies to parallel version only.

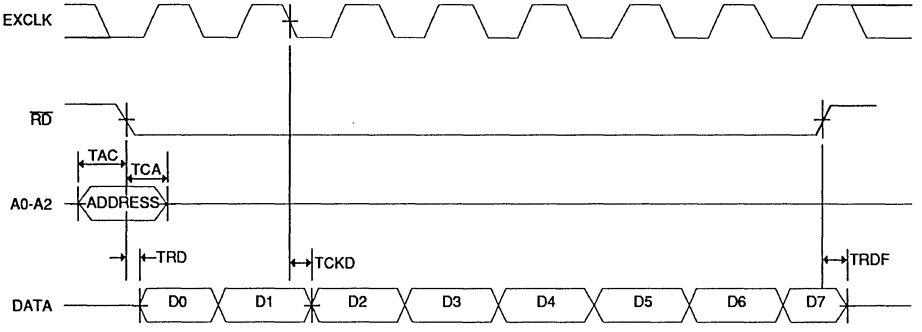
** Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

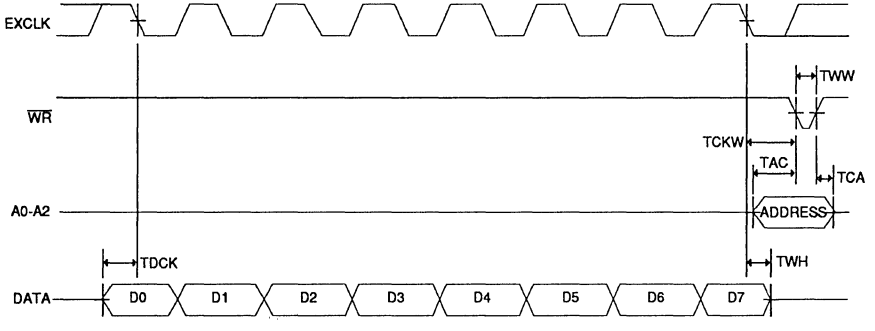
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

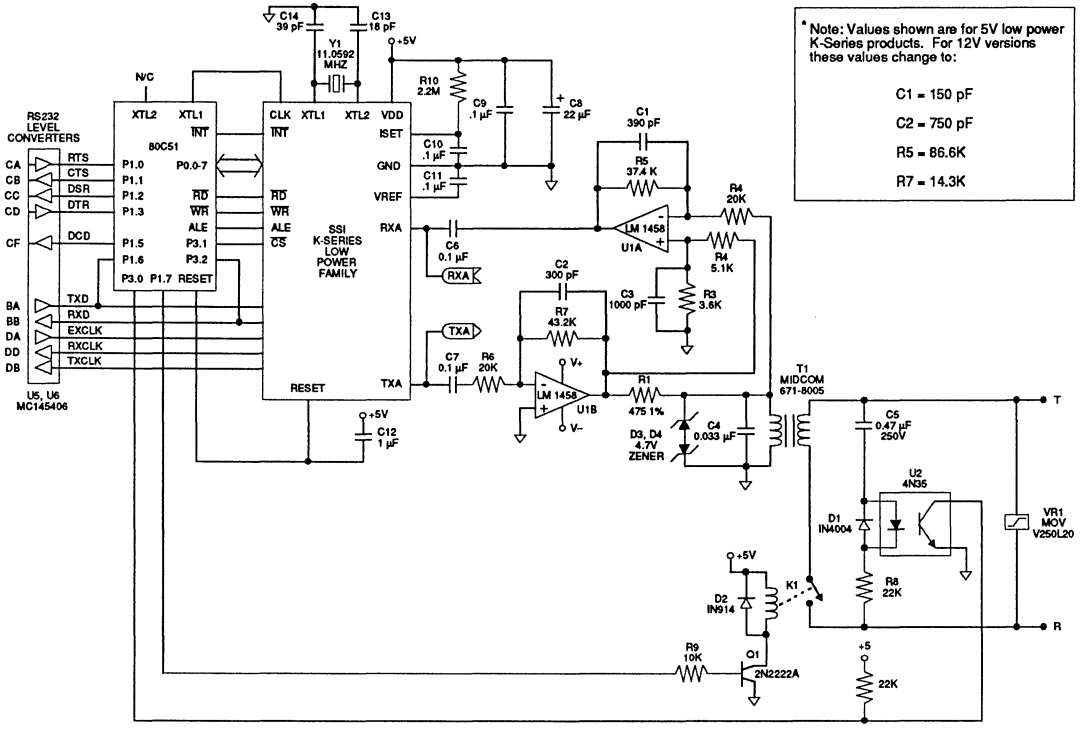


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

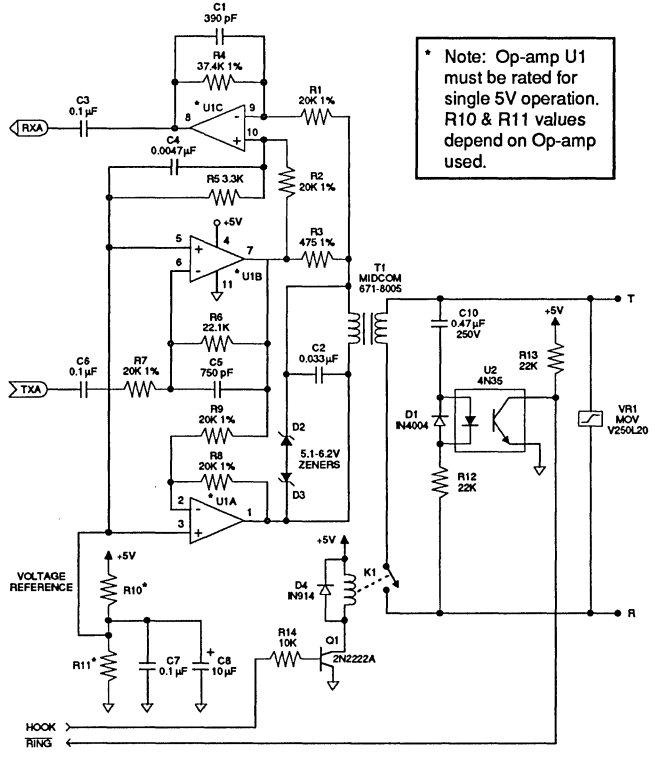


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

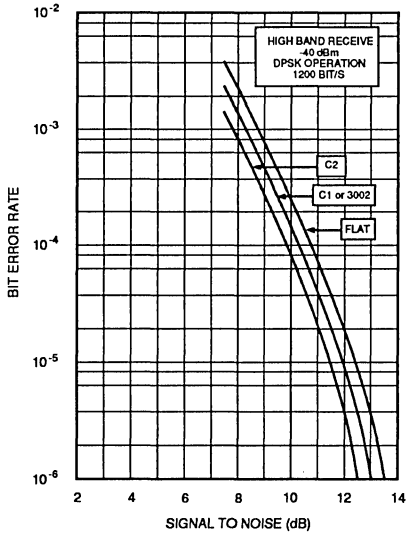
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

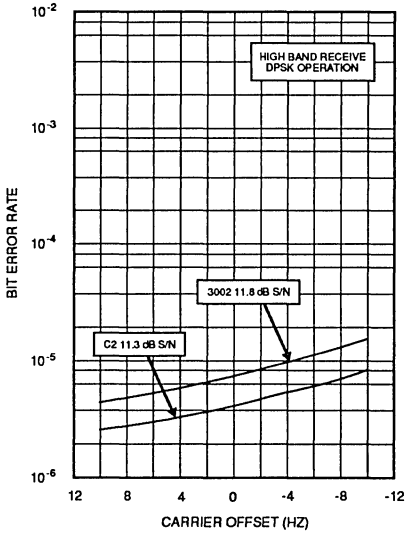
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

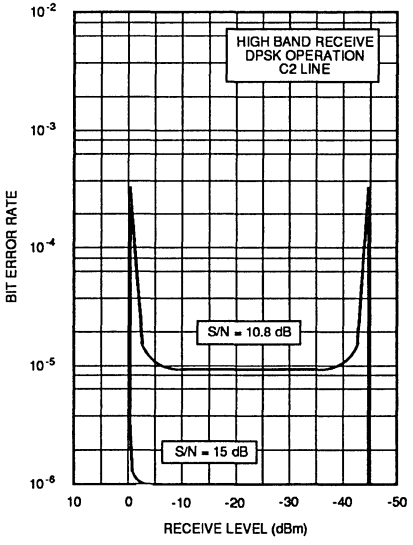
SSI 73K212, 73K212L
BER vs SIGNAL TO NOISE



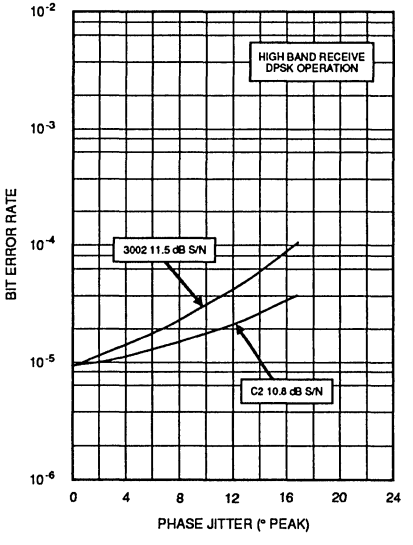
SSI 73K212, 73K212L
BER vs CARRIER OFFSET



*SSI 73K212, 73K212L
BER vs RECEIVE LEVEL



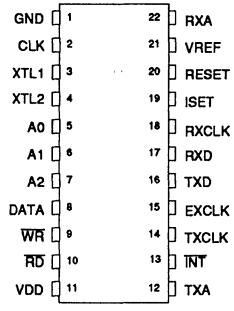
*SSI 73K212, 73K212L
BER vs PHASE JITTER



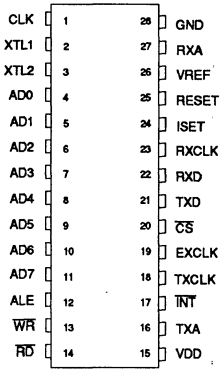
* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

SSI 73K212/K212L
Bell 212A/103
Single-Chip Modem

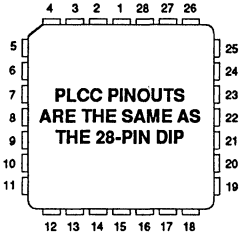
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K212 with Parallel Bus Interface		
28-pin 12 volt supply		
Plastic Dual-In-Line	SSI 73K212 – IP	73K212 – IP
Plastic Leaded Chip Carrier	SSI 73K212 – IH	73K212 – IH
28-pin 5 volt supply		
Plastic Dual-In-Line	SSI 73K212L – IP	73K212 – IP
Plastic Leaded Chip Carrier	SSI 73K212L – IH	73K212L – IH
SSI 73K212 with Serial Interface		
22-pin 12 volt supply		
Plastic Dual-In-Line	SSI 73K212S – IP	73K212S – IP
22-pin 5 volt supply		
Plastic Dual-In-Line	SSI 73K212SL – IP	73K212S – IP
Ceramic Dual-In-Line	SSI 73K212SL – IC	73K212SL – IC

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 73K221/K221L
CCITT V.22, V.21
Single-Chip Modem

1

July, 1990

DESCRIPTION

The SSI 73K221 is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation over dial-up lines. The SSI 73K221 is an enhancement of the SSI 73K212 single-chip modem with performance characteristics suitable for European and Asian telephone systems. The SSI 73K221 produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows V.21 for 300 Hz FSK operation. The SSI 73K221 integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K221L, low power version of the SSI 73K221 provides identical performance and features, but operates from a single +5 volt supply with substantially lower power consumption.

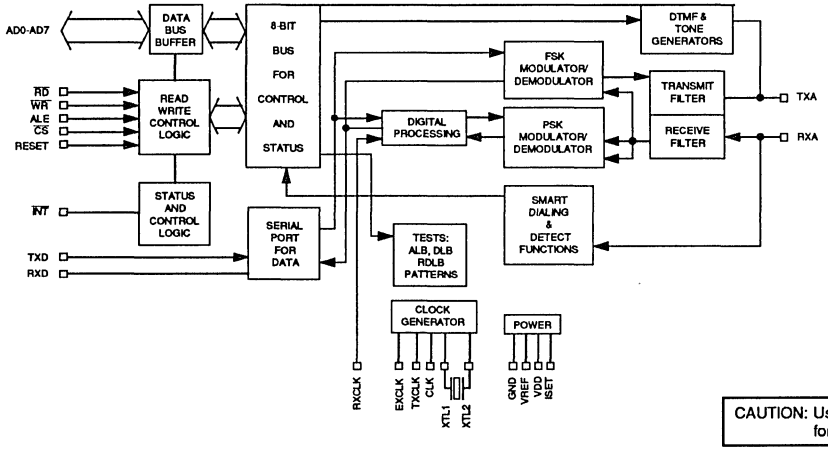
The SSI 73K221 includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer and 550 or 1800 Hz guard tone. This device supports V.22 (except mode v) and V. 21 modes of operation,

(Continued)

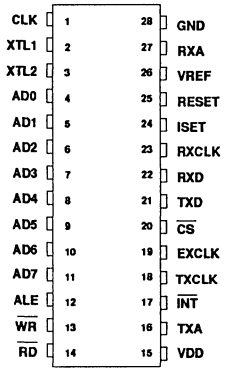
FEATURES

- **One-chip CCITT V.22 and V.21 standard compatible modem data pump**
- **Full-duplex Operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel (28-pin DIP) microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2100 Hz), and long loop detectors**
- **DTMF, and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **Space efficient 22- or 28-pin DIP packages**
- **CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V**
- **Single +5 volt (73K221L) or +12 volt (73K221) versions**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

allowing both synchronous and asynchronous communications. The SSI 73K221 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or alternatively via the serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K221 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K221 is part of SSi's K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K221 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, - 2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± .01%.

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNC/SYNC converter is bypassed when synchronous mode is selected and data is transmitted at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K221 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or

ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K221 uses a phase locked loop coherent demodulation technique for optimum performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the V.21 mode.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, optionselect and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K221 control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out the remaining seven bits of the selected address LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the addressed register on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark signal is also detected when the received data out of the DPSK demodulator before the descrambler has been mark for 165.5 ms ± 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all conditions except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (or 5V ±10%). Bypass with .1 and 22 µF capacitors to ground.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal control registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state $\overline{CS}$ is a latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K221 internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this pin informs the SSI 73K221 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K221 that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K221 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to the TXD pin. Alternately used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data at RXD. RXCLK will be valid as long as a carrier is present in DPSK synchronous modes.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in DPSK synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied to this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring an 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

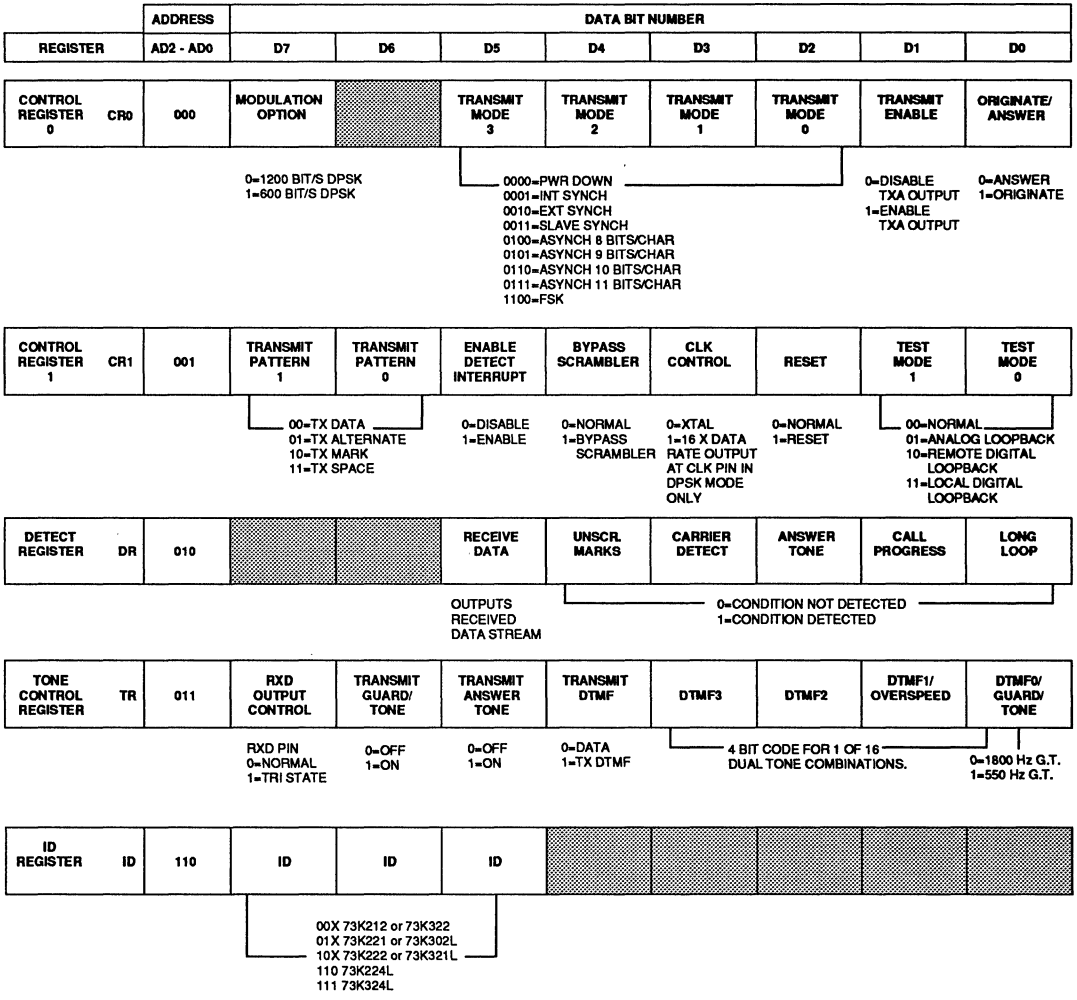
Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. In parallel mode AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K221 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output driver used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	0	1						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band,receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to allow Answer Tone and DTMF transmission.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ±0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 stop bit).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a "0."

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	DPSK mode at 1200 bit/s.
		1 0 X	DPSK mode at 600 bit/s. X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as determined by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Detect	0	No answer tone detected.
		1	Indicates detection of 2100 Hz answer tone. The device must be in originate mode for detection of answer tone.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the received channel.
D4	Unscrambled Mark	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. This may be used in the V.22 connect sequence or for requesting a remote modem to configure itself for remote digital loopback. A valid indication means that unscrambled marks have been received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Guard Tone	D6 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X 1 X	Transmit DTMF tones.
		X 0 0	Transmits 1800 Hz guard tone.
		X 0 1	Transmits 550 Hz guard tone.
D1	DTMF 1/	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 or 600 bit/s +1.0% - 2.5%
		0 1	Asynchronous DPSK 1200 or 600 bit/s +2.3% -2.5%.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:
D4	Transmit DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions. Modem must be in DPSK mode during DTMF transmission.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	TX Guard (Transmit Guard Tone)	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin becomes a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID					

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212(L) or 73K322L
		0 1 X	SSI 73K221(L) or 73K302L
		1 0 X	SSI 73K222(L) or 73K321L
		1 1 0	SSI 73K224L
		1 1 1	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

ELECTRICAL SPECIFICATIONS (Continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator (Modem must be in DPSK mode to meet specifications)					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Group, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Group, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Group to Low-Group	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
- 10 dB loss in the Transmit path to the line.
- 9 dB gain in the Receive path from the line.

5V Version
- 0 dB loss in the Transmit path to the line.
- 2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	In FSK mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single	10			KΩ
	Tone out for THD = -50 db in .3 to 3.4 KHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 KHz			-39	dBm0
	Frequency = 153.6 KHz			-45	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin; 76.8 KHz				
5V Version (73K221L)				1.0	mVrms
12V Version (73K221)				2	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change		40	100	ms
Recovered Clock					
Capture Range		-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

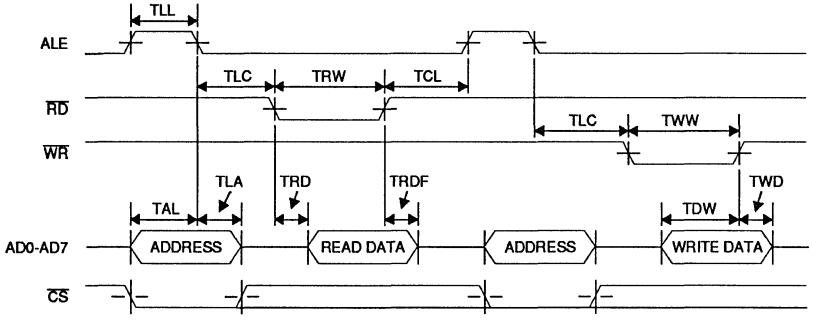
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE low	20			ns
TLC	ALE low to $\overline{RD}/\overline{WR}$ low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE high	10			ns
TRD	Data out from $\overline{RD}$ low	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ high	0		80	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000*	ns
TDW	Data setup before $\overline{WR}$ high	150			ns
TWD	Data hold after $\overline{WR}$ high	20			ns
TCKD	Data out after EXCLK low			200	ns
TCKW	$\overline{WR}$ after EXCLK low	150			ns
TDCK	Data setup before EXCLK low	150			ns
TAC	Address setup before control**	50			ns
TCA	Address hold after control**	50			ns
TWH	Data hold after EXCLK	150			ns

* Maximum time applies to parallel version only.

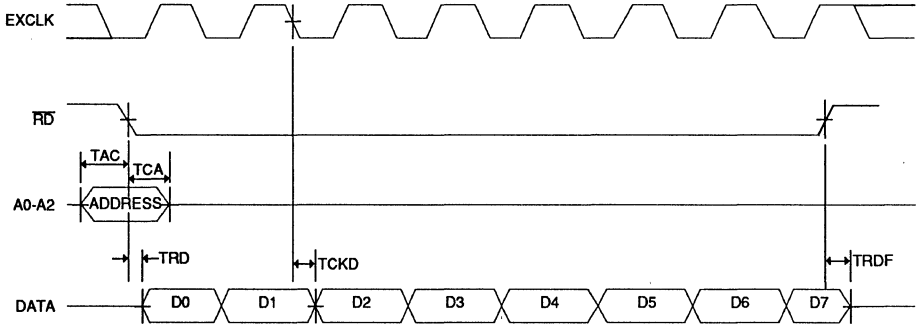
** Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

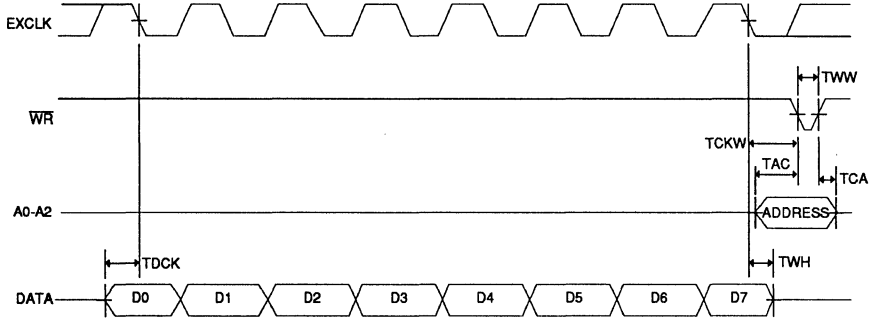
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

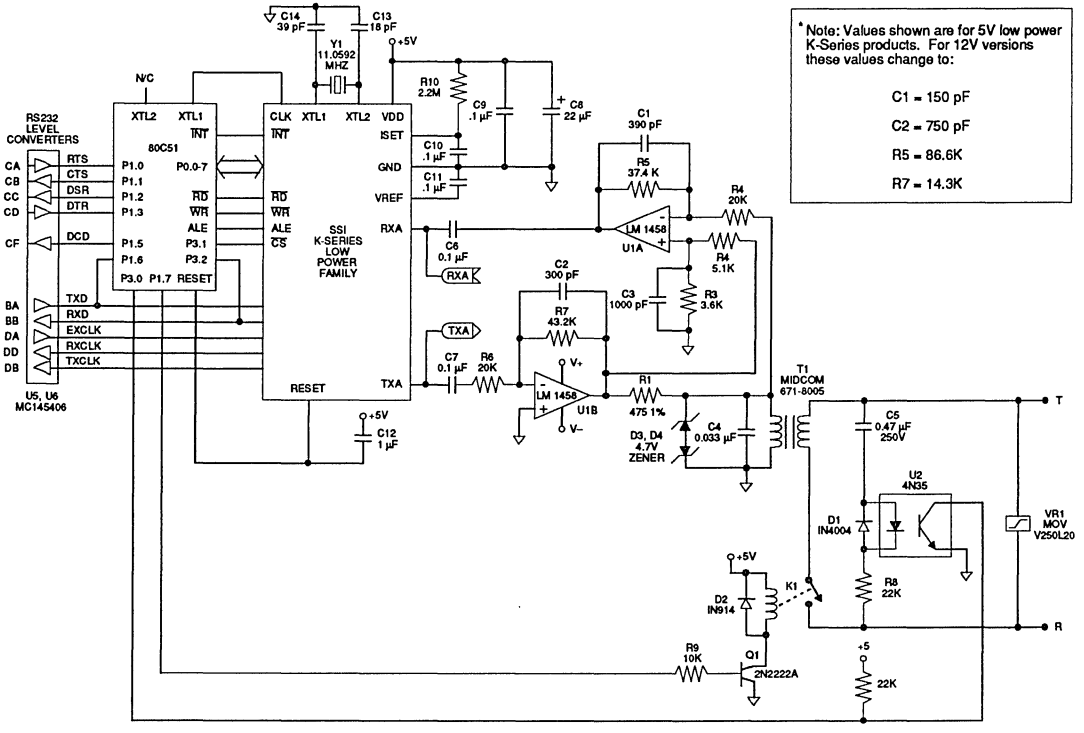


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

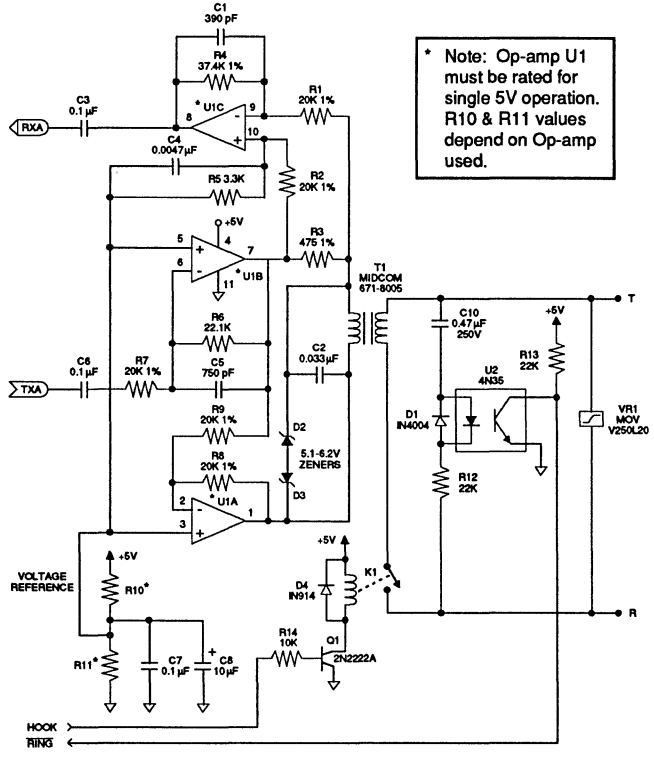


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

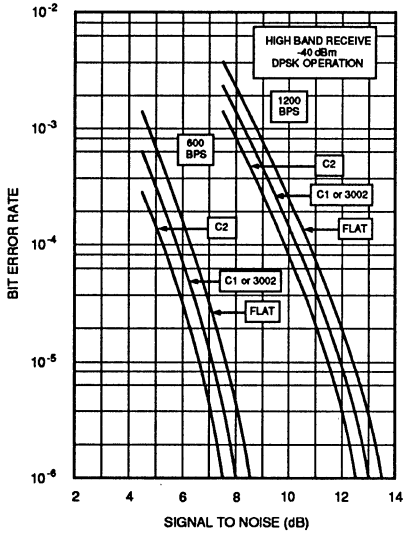
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

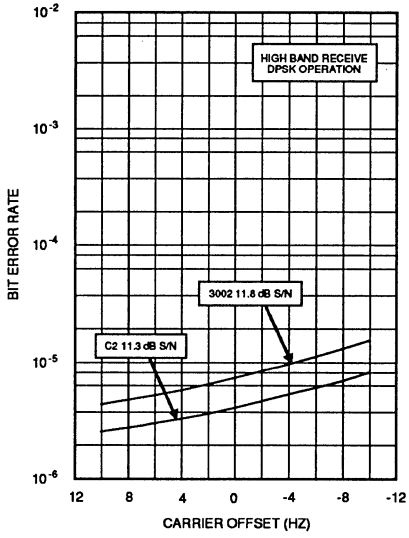
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

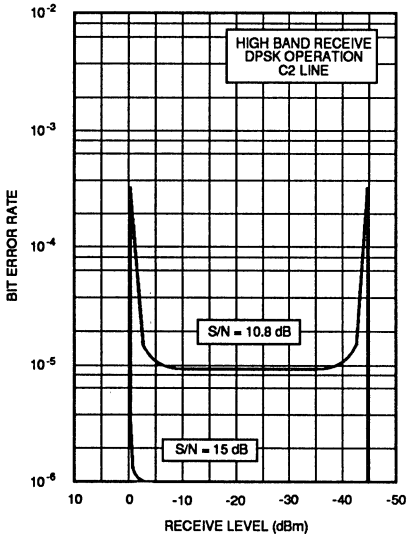
*SSI 73K221, 73K221L
BER vs SIGNAL TO NOISE



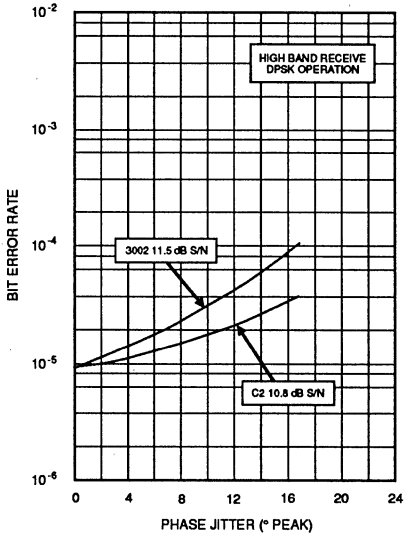
*SSI 73K221, 73K221L
BER vs CARRIER OFFSET



*SSI 73K221, 73K221L
BER vs RECEIVE LEVEL



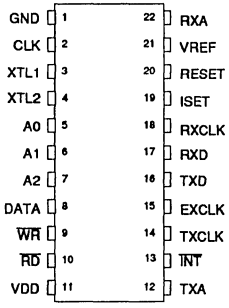
*SSI 73K221, 73K221L
BER vs PHASE JITTER



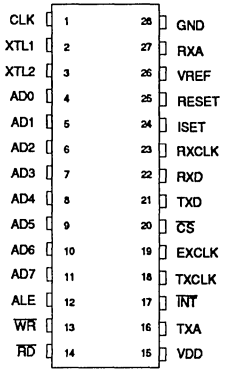
* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

PACKAGE PIN DESIGNATIONS

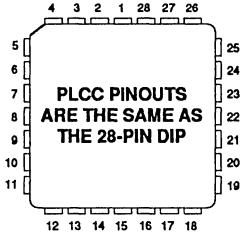
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K221 with Parallel Bus Interface		
28-pin 12 volt supply		
Plastic Dual-In-Line	SSI 73K221 – IP	73K221 – IP
Plastic Leaded Chip Carrier	SSI 73K221 – IH	73K221 – IH
28-pin 5 volt supply		
Plastic Dual-In-Line	SSI 73K221L – IP	73K221L – IP
Plastic Leaded Chip Carrier	SSI 73K221L – IH	73K221L – IH
SSI 73K212 with Serial Interface		
22-pin 12 volt supply		
Plastic Dual-In-Line	SSI 73K221S – IP	73K221S – IP
22-pin 5 volt supply		
Plastic Dual-In-Line	SSI 73K221SL – IP	73K221S – IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 73K222/K222L
V.22, V.21, Bell 212A Single-Chip Modem

1

July, 1990

DESCRIPTION

The SSI 73K222 is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22, V.21 and Bell 212A compatible modem, capable of 1200 bit/s full–duplex operation over dial-up lines. The SSI 73K222 is an enhancement of the SSI 73K212 single-chip modem which adds V.22 and V.21 modes to the Bell 212A and 103 operation of the SSI 73K212. In Bell 212A mode, the SSI 73K222 provides the normal Bell 212A and 103 functions and employs a 2225 Hz answer tone. The SSI 73K222 in V.22 mode produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows 600 bit/s V.22 or 0-300 bit/s V.21 operation. The SSI 73K222 integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K222L, low power version of the SSI 73K222 provides identical performance and features, but operates from a single +5 volt supply with substantially lower power consumption.

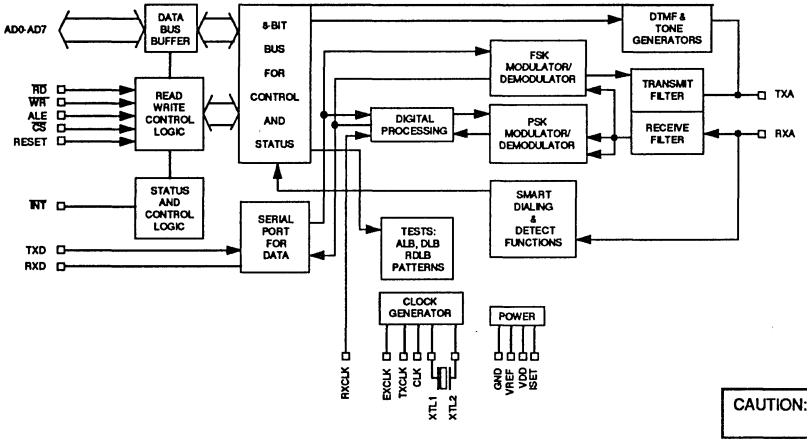
The SSI 73K222 includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor and a tone generator capable of

(Continued)

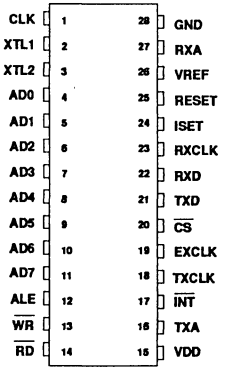
FEATURES

- **One-chip CCITT V.22, V.21, Bell 212A and 103 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel (28-pin DIP) microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation including V.22 extended overspeed**
- **Call progress, carrier, precise answer tone (2100 or 2225 Hz), and long loop detectors**
- **DTMF, and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **Space efficient 22- or 28-pin DIP packages**
- **CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V**
- **Single +5 volt (73K222L) or +12 volt (73K222) versions**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

tone required for European applications. This device supports V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and asynchronous communications. Test features such as analog loop, digital loop, and remote digital loopback are supported. Internal pattern generators are also included for self-testing. The SSI 73K222 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K222 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K222 is part of Silicon Systems' K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K222 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data within a ±0.01% rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± 0.01% (± 0.01% is required synchronous data rate accuracy).

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K222 modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire

telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K222 uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space), or 1650 and 1850Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 or V.21 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K222 control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the addressed register occurs on the rising edge of $\overline{WR}$. This interface mode is also supported in the 28-pin packages. See serial control interface pin description.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (73K222) or 5V ±10% (73K222L). Bypass with .1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to ground.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K222 internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K222 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K222 that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K222 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

DTE USER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. In parallel mode the address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K222 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANS TONE
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID					

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

REGISTER	ADDRESS AD2 - AD0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK 0=BELL 103 FSK 1=V.21 FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER/ TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			0=2225 Hz A.T. 1800 Hz G.T. 1=2100 Hz A.T. 500 Hz G.T.
ID REGISTER ID	110	ID	ID	ID					
		00X=73K212(L) or 73K322L 01X=73K221(L) or 73K302L 10X=73K222(L) 110=73K224 111=73K324L							

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band,receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to allow Answer Tone and DTMF Transmiission.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a "0."

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	DPSK mode at 1200 bit/s.
		1 0 X	DPSK mode at 600 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK CCITT V.21 mode.
			X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Detect	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in originate mode for detection of answer tone. For CCITT answer tone detection, bit D0 of the Tone Register must be set to a 1.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the receive channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 0 0 0	Detects 2225 Hz in originate mode.
		X 1 0 0	Transmits 2225 Hz in answer mode (Bell).
		X 0 0 1	Detects 2100 Hz in originate mode.
		X 1 0 1	Transmits 2100 Hz in answer mode (CCITT).
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK +1.0% -2.5%.
		0 1	Asynchronous DPSK +2.3% -2.5%.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

D4	Transmit DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown.
		0 0 X	Disables answer tone generator.
		1 0 0	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.
		1 0 1	Likewise a 2100 Hz answer tone will be transmitted.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 1	ID 0	ID					

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212(L) or 73K322L
		0 1 X	SSI 73K221(L) or 73K302L
		1 0 X	SSI 73K222(L)
		1 1 0	SSI 73K224L
		1 1 1	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

ELECTRICAL SPECIFICATIONS (Continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10.0	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, DPSK Mode	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
- 10 dB loss in the Transmit path to the line.
- 9 dB gain in the Receive path from the line.

5V Version
- 0 dB loss in the Transmit path to the line.
- 2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect	DPSK or FSK				
Threshold	receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	In FSK mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single	10			KΩ
	Tone out for THD = -50 db in .3 to 3.4 KHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 KHz			-39	dBm0
	Frequency = 153.6 KHz			-45	dBm0
TXA pin Output Impedance			200	300	Ω
Clock Noise	TXA pin; 76.8 KHz				
5V Version (73K222L)				1.0	mVrms
12V Version (73K222)				2.0	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATIONS (Continued)

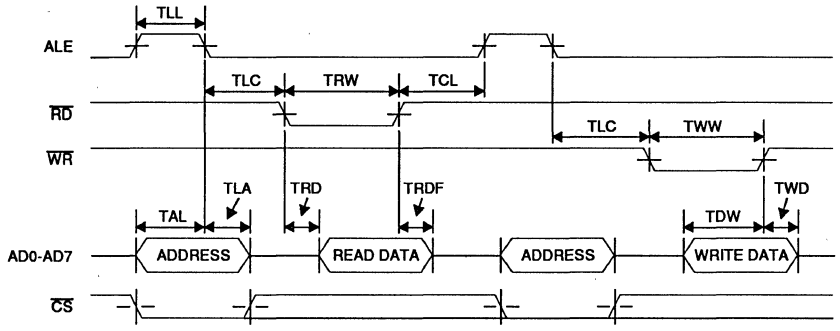
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 Hz				
	1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}/\overline{WR}$ Low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		200	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

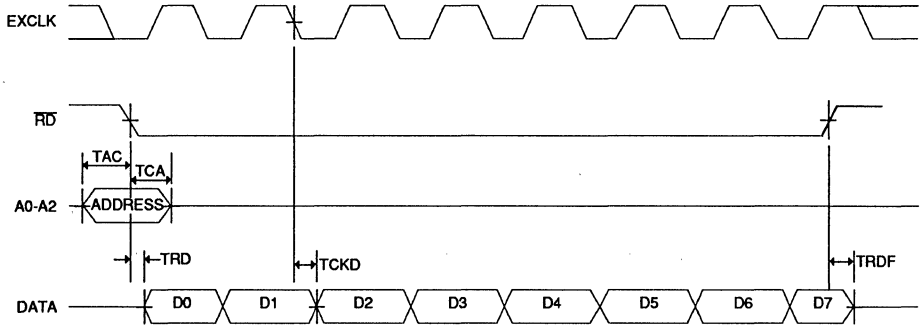
* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

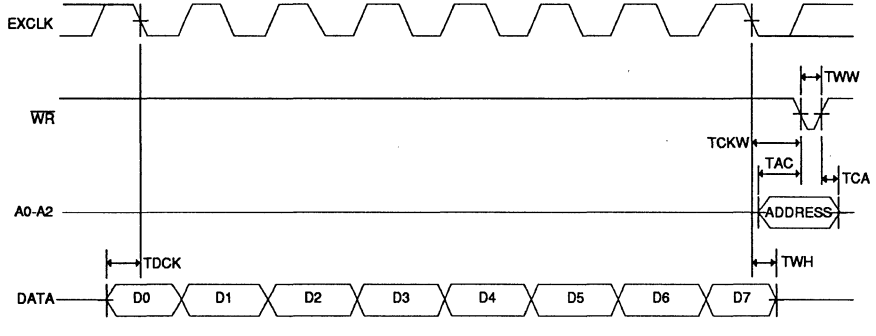
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

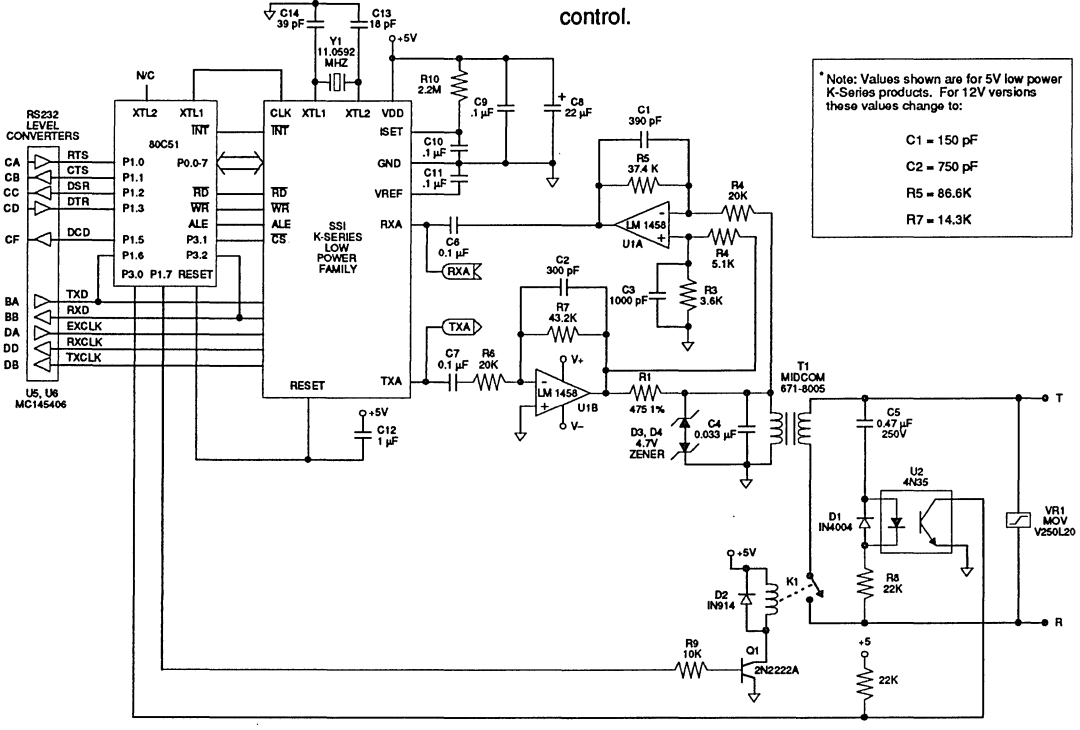


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

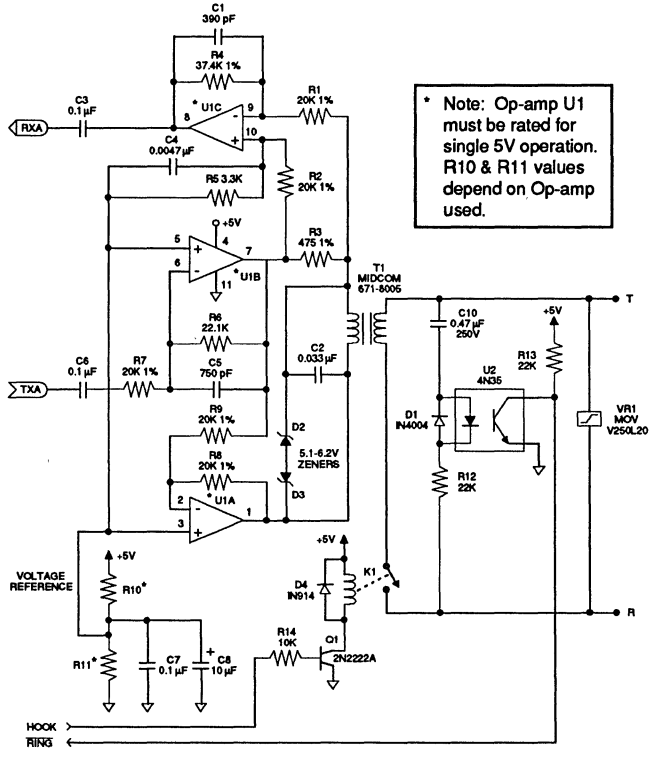


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

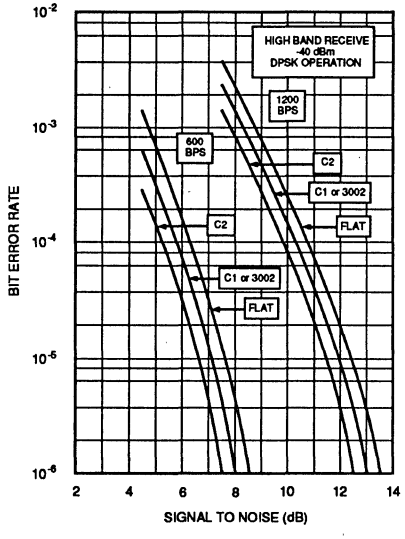
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

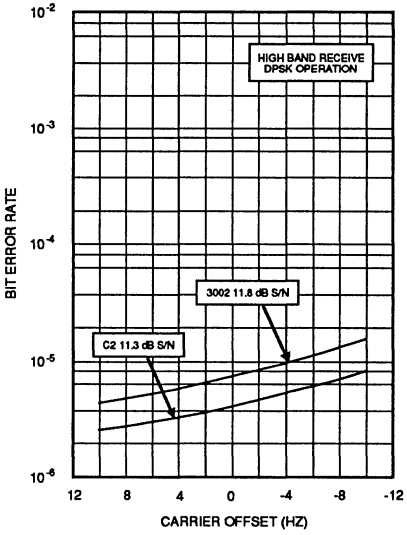
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

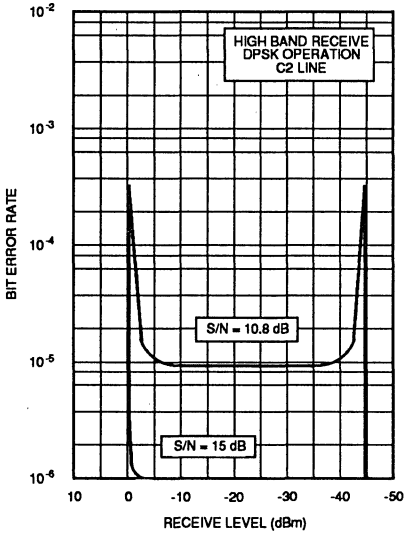
*SSI 73K222, 73K222L
BER vs SIGNAL TO NOISE



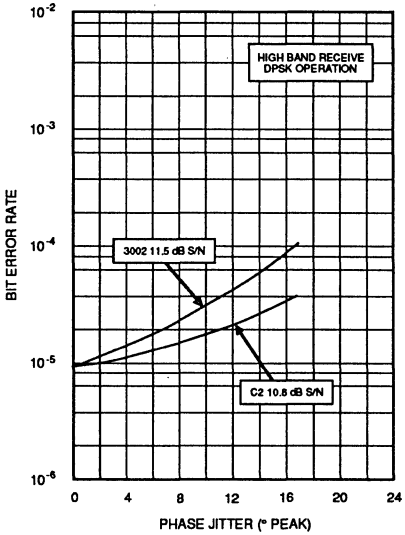
*SSI 73K222, 73K222L
BER vs CARRIER OFFSET



*SSI 73K222, 73K222L
BER vs RECEIVE LEVEL



*SSI 73K222, 73K222L
BER vs PHASE JITTER

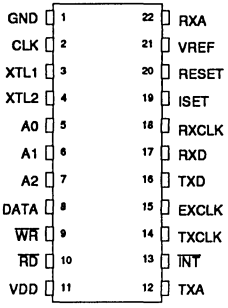


* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

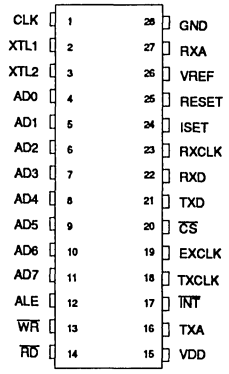
SSI 73K222/K222L
V.22, V.21, Bell 212A
Single-Chip Modem

1

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



400-Mil
22-Pin DIP



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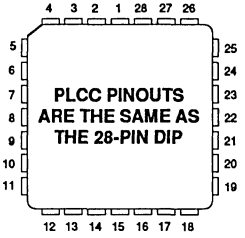
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K222 with Parallel Bus Interface		
28-Pin 12 Volt Supply		
Plastic Dual-In-Line	SSI 73K222 – IP	73K222 – IP
Plastic Leaded Chip Carrier	SSI 73K222 – IH	73K222 – IH
28-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K222L – IP	73K222L – IP
Plastic Leaded Chip Carrier	SSI 73K222L – IH	73K222L – IH
SSI 73K222 with Serial Interface		
22-Pin 12 Volt Supply		
Plastic Dual-In-Line	SSI 73K222S – IP	73K222S – IP
22-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K222SL – IP	73K222SL – IP
Ceramic Dual-In-Line	SSI 73K222SL – IC	73K222SL – IC

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 73K222U
Single-Chip Modem with UART

1

July, 1990

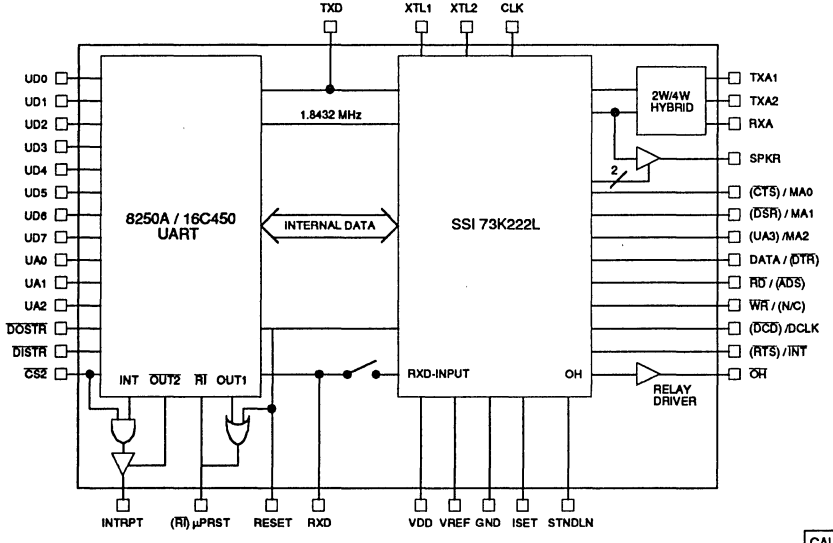
DESCRIPTION

The SSI 73K222U is a compact, high-performance modem which includes a 8250A/16C450 compatible UART with the 1200 bit/s modem function on a single chip. Based on the SSI 73K222L 5-volt low power CMOS modem IC, the SSI 73K222U is the perfect modem/UART component for integral modem applications. It is ideal for applications such as portable terminals and laptop computers. The SSI 73K222U is the first fully featured modem IC which can function as an intelligent modem in integral applications without requiring a separate dedicated microcontroller. It provides for data communication at 1200, 600, and 300 bit/s in a multi-mode manner that allows operation compatible with both Bell 212A/103 and CCITT V.22/V.21 standards. The digital interface section contains a high speed version of the industrystandard 8250A/16C450 UART, commonly used in personal computer products. A unique feature of the SSI 73K222U is that the UART section can be used without the modem function, providing an additional asynchronous port at no added cost. The SSI 73K222U is designed in CMOS technology and operates from a single +5V supply. Available packaging includes 40-pin DIP or 44-pin PLCC for surface mount applications.

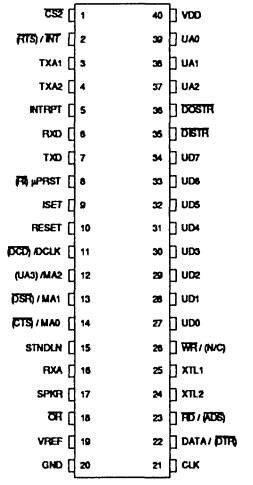
FEATURES

- **Modem/UART combination optimized for integral bus applications**
- **Includes features of SSI 73K222L single-chip modem**
- **Fully compatible 16C450/8250 UART with 8250B or 8250A selectable interrupt emulation**
- **High speed UART will interface directly with high clock rate bus with no wait states**
- **Compatible with SSI 73K212U (Bell 212A/103) and SSI 73K221U (CCITT V.22/V.21) family members**
- **Single-port mode allows full modem and UART control from CPU bus, with no dedicated microprocessor required**
- **Dual-port mode suits conventional designs using local microprocessor for transparent modem operation**
- **Complete modem functions for 1200 bit/s (Bell 212A, V.22) and 0-300 bit/s (Bell 103, V.21)**
- **Includes DTMF generator, carrier, call-progress and precise answer-tone detectors for intelligent dialing capability**
- **On chip 2-wire/4-wire hybrid driver and off-hook relay buffer**
- **Speaker output with four-level software driven volume control**
- **Low power CMOS (40 mW) with power down mode (15 mW)**
- **Operates from single +5V supply**

BLOCK DIAGRAM



PIN DIAGRAM



Parentheses indicate single-port mode.

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73K222U
Single-Chip Modem with UART

FUNCTIONAL DESCRIPTION

The SSI 73K222U integrates an industry standard 8250/16C450 UART function with the modem capability provided by the SSI 73K222L single chip modem IC. The SSI 73K222U is designed specifically for integral microprocessor bus intelligent modem products. These designs typically require the standard 8250 or higher speed 16450 UART to perform parallel-to-serial and serial-to-parallel conversion process necessary to interface a parallel bus with the inherently serial modem function. The SSI 73K222U provides a highly integrated design which can eliminate multiple components in any integral bus modem application, and is ideal for internal PC modem applications.

The SSI 73K222U includes two possible operating modes. In the dual-port mode, the device is suitable for conventional plug-in modem card designs which use a separate local microprocessor for command interpretation and control of the modem function. In this mode, a dedicated microcontroller communicates with the SSI 73K222U using a separate serial command port. In the single-port mode the main CPU can control both the UART and modem function using the parallel data bus. This allows very efficient modem design with no local microprocessor required for dedicated applications such as laptop PC's or specialized terminals.

To make designs more space efficient, the SSI 73K222U includes the 2-wire to 4-wire hybrid drivers, off-hook relay driver, and an audio monitor output with software volume control for audible call progress monitoring. As an added feature the UART function can be used independent of the modem function, providing an added asynchronous port in a typical PC application with no additional circuitry required.

UART FUNCTION (16C450)

The UART section of the SSI 73K222U is completely compatible with the industry standard 16C450 and the 8250 UART devices. The bus interface is identical to the 16450, except that only a single polarity for the control signals is supported. The register contents and addresses are also the same as the 16C450. To insure compatibility with all existing releases of the 8250 UART design, external circuitry normally used in PC applications to emulate 8250B or 8250A interrupt operation has been included on the SSI 73K222U. A select line is then provided to enable the desired interrupt operation. The UART used in the SSI 73K222U can be used with faster bus read and write cycles than a conventional 16C450 UART. This allows it to interface directly with higher clock rate microprocessors with no need for external circuitry to generate wait states.

The primary function of the UART is to perform parallel-to-serial conversion on data received from the CPU and serial-to-parallel conversion on data received from the internal modem or an external device. The UART can program the number of bits per character, parity bit generation and checking, and the number of stop bits. The UART also provides break generation and detection, detection of error conditions, and reporting of status at any time. A prioritized maskable interrupt is also provided.

The UART block has a progammable baud rate generator which divides an internal 1.8432 MHz clock to generate a clock at 16 x the data rate. The data rate for the transmit and receive sections must be the same. For DPSK modulation, the data rate must be 1200 Hz or 600 Hz. For FSK modulation, the data rate must be 300 Hz or less. The baud generator can create a clock that supports digital transfer at up to 115.2 KHz. The output of the baud generator can be made available at the CLK pin under program control.

MODEM FUNCTION (SSI 73K222L)

The modem section of the SSI 73K222U provides all necessary analog functions required to create a single chip Bell 212A/103 and CCITT V.22/V.21 modem, controlled by the system CPU or a local dedicated microprocessor. Asynchronous 1200 bit/s DPSK (Bell 212A and V.22) and 300 baud FSK (Bell 103 and V.21) modes are supported.

The modem portion acts as a peripheral to the microprocessor. In both modes of operation, control information is stored in register memory at specific address locations. In the single-port mode, the modem section can be controlled through the 16C450 interface, with no external microcontroller required. The primary analog blocks are the DPSK modulator/demodulator, the FSK modulator/demodulator, the high and low band filters, the AGC, the special detect circuitry, and the DTMF tone generator. The analog functions are performed with switched capacitor technology.

PSK MODULATOR / DEMODULATOR

The SSI 73K222U modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the band limited 2-wire PSTN line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. The demodulator decodes either a 1200 Hz carrier (originate carrier) or a 2400 Hz carrier (answer carrier). The SSI 73K222U uses a phase-locked-loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225Hz and 2025 Hz (answer mark and space) are used. V.21 mode uses 980 Hz and 1180 Hz (originate, mark and space) or 1650 Hz and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the band limited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping, and provides a total dynamic range of >45 dB.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone, and weak received signal (long loop condition). An unscrambled mark signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 mS ±13.5 mS. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all monitored conditions except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to a 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from a 0 to a 1.

TEST FEATURES

Test features such as analog loopback (ALB), remote digital loopback, local digital loopback, and internal pattern generators are also included.

LINE INTERFACE

The line interface of the SSI 73K222U consists of a two-to-four wire hybrid, and an off-hook relay driver.

The two-to-four wire converter has a differential transmit output and requires only a line transformer and an external impedance matching resistor. Four-wire operation is also available by simply using either of the transmit output signals.

The relay driver output of the SSI 73K222U is an open drain signal capable of sinking 20 mA, which can control a line closure relay used to take the line off hook and to perform pulse dialing.

AUDIO MONITOR

An audio monitor output is provided which has a software programmable volume control. Its output is the received signal. The audio monitor output can directly drive a high impedance load, but an external power amplifier is necessary to drive a low-impedance

PIN DESCRIPTION

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V Supply ±10%, bypass with a .1 and a 22µF capacitor to GND
GND	20	22	I	System Ground
VREF	19	21	O	VREF is an internally generated reference voltage which is externally bypassed by a .1µF capacitor to the system ground.
ISET	9	11	I	The analog current is set by connecting this pin to VDD through a 2MΩ resistor. ISET should be bypassed to GND. Alternatively, an internal bias can be selected by connecting ISET to GND, which will result in a larger worst-case supply current due to the tolerance of on-chip resistors. Bypass with .1µF capacitor if resistor is used.
XTL1 XTL2	25 24	27 26	I I	These pins are connections for the internal crystal oscillator requiring an 11.0592 MHz crystal (9216Hz x 1200). XTAL2 can also be TTL driven from an external clock.
CLK	21	23	O	Output Clock. This pin is selectable under processor control to be either the crystal frequency (which might be used as a processor clock) or the output of the baud generator.
RESET	10	12	I	Reset. An active signal (high) on this pin will put the chip into an inactive state. The control register bits (except the Receiver Buffer, Transmitter Holding, and Divisor latches) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on reset using a 0.1µF capacitor connected to the 5V supply.
STNDLN	15	17	I	Single-port mode select (active high). In a single-port system there is no local microprocessor and all the modem control is done through the 16C450 parallel bus interface. The local microprocessor interface is replaced with UART control signals which allow the device to function as a digital UART as well as modem.

PIN DESCRIPTION (continued)

UART INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
UA0-UA2 UA3	37-39 12	41-43 14	I I	UART Address. These pins determine which of the UART registers is being selected during a read or write on the UART data bus. The contents of the DLAB bit in the UART's Line Control Register also control which register is referenced. In single-port mode, UA0-UA3 are latched when $\overline{ADS}$ goes high. In dual-port, only UA0-UA2 are used.
UD0-UD7	27-34	30-37	I/O	(3 state) UART Data. Data or control information to the UART registers is carried over these lines.
$\overline{DISTR}$	35	38	I	Data Input Strobe. A low on this pin requests a read of the internal UART registers. Data is output on the D0-D7 lines if $\overline{DISTR}$ and $\overline{CS2}$ are active.
$\overline{DOSTR}$	36	39	I	Data Output Strobe. A low on this pin requests a write of the internal UART registers. Data on the D0-D7 lines are latched on the rising edge of $\overline{DOSTR}$. Data is only written if both $\overline{DOSTR}$ and $\overline{CS2}$ are active.
$\overline{CS2}$	1	2	I	Chip Select. A low on this pin allows a read or write to the UART registers to occur. In single port mode, $\overline{CS2}$ is latched on $\overline{ADS}$.
INTRPT	5	7	O	(3 state) UART Interrupt. This signal indicates that an interrupt condition on the UART side has occurred. If the Enable 8250A interrupt bit in the interrupt Enable Register is 0 the interrupt is gated by the $\overline{DISTR}$ signal to provide compatibility with the 8250B. The output can be put in a high impedance state with the OUT2 register bit in the Modem Control Register. In single-port mode, INTRPT also becomes valid when a modem interrupt signal is generated by the modem section's Detect Register.
RXD	6	8	I/O	Function is determined by STNDLN pin and bit 7, Tone Control Register:

STNDLN	D7	
0	0	RXD outputs data received by modem.
1	0	RXD is electrically an input but signal is ignored.
X	1	RXD is a serial input to UART.

PIN DESCRIPTION (continued)

UART INTERFACE (continued)

<table>
<tr><td>TXD</td><td>7</td><td>9</td><td>O</td><td colspan="3">Function is determined by STNDLN pin and bit 7, Tone Control Register:</td></tr>
<tr><td rowspan="4"></td><td rowspan="4"></td><td rowspan="4"></td><td rowspan="4"></td><td>STNDLN</td><td>D7</td><td></td></tr>
<tr><td>0</td><td>0</td><td>TXD is a serial output of UART.</td></tr>
<tr><td>1</td><td>0</td><td>TXD is forced to a mark.</td></tr>
<tr><td>X</td><td>1</td><td>TXD is a serial output of UART.</td></tr>
</table>

ANALOG / LINE INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
TXA1 TXA2	3 4	4 5	O O	(differential) Transmitted Analog. These pins provide the analog output signals to be transmitted to the phone line. The drivers will differentially drive the impedance of the line transformer and the line matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal.
RXA	16	18	I	Received Analog. This pin inputs analog information that is being received by the two-to-four wire hybrid. This input can also be taken directly from an external hybrid.
SPKR	17	19	O	Speaker Output. This pin outputs the received signal through a programmable attenuator stage, which can be used for volume control and disabling the speaker.
$\overline{OH}$	18	20	O	Off-hook relay driver. This signal is an open drain output capable of sinking 20mA and is used for controlling a relay. The output is the complement of the $\overline{OH}$ register bit in CR3.

PIN DESCRIPTION (continued)

UART CONTROL INTERFACE (STNDLN = 1)

(See Figure 1: Single-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{ADS}$	23	25	I	Address Strobe. $\overline{ADS}$ is used to latch address and chip select to simplify interfacing to a multiplexed Address/Data Bus. UA0-UA3 and $\overline{CS2}$ are latched when the $\overline{ADS}$ signal goes high.
UA3	12	14	I	UART Address Bit 3. UA3 is used in single-port mode to address the modem registers from the 16C450 interface. If UA3 is 0, the normal 16C450 registers are addressed by UA0-UA2 and if UA3 is 1, the modem registers are addressed. UA3 is latched when $\overline{ADS}$ goes high.
$\overline{CTS}$	14	16	I	Clear to Send. This pin is the complement of CTS bit in the Modem Status Register. The signal is used in modem handshake control to signify that communications have been established and that data can be transmitted.
$\overline{DSR}$	13	15	I	Data Set Ready. This pin is the complement of DSR bit in the Modem Status Register. The signal is used in modem handshake to signify that the modem is ready to establish communications.
$\overline{DCD}$	11	13	I	Data Carrier Detect. This pin is the complement of DCD bit in the Modem Status Register. The signal is used in modem control handshake to signify that the modem is receiving a carrier.
$\overline{DTR}$	22	24	O	Data Terminal Ready. The $\overline{DTR}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 is available to communicate.
$\overline{RTS}$	2	3	O	Request to Send. The $\overline{RTS}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 has data to transmit.
$\overline{RI}$	8	10	I	Ring Indicator. This Indicates that a telephone ringing signal is being received. This pin is the complement of the RI bit in the Modem Status Register.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE (STNDLN = 0)

(See Figure 2: Dual-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	12-14	14-16	I	Modem Address Control. These lines carry register addresses for the modem registers and should be valid throughout any read or write operation.
DATA	22	24	I/O	Serial Control Data. Serial control data to be read/written is clocked in/out on the falling edge of the DCLK pin. The direction of data transfer is controlled by the state of the $\overline{RD}$ pin. If the $\overline{RD}$ pin is active (low) the DATA line is an output. Conversely, if the $\overline{RD}$ pin is inactive (high) the DATA line is an input.
$\overline{RD}$	23	25	I	Read. A low on this input informs the SSI 73K222U that control data or status information is being read by the processor from a modem register.
$\overline{WR}$	26	28	I	Write. A low on this input informs the SSI 73K222U that control data or status information is available for writing into a modem register. The procedure for writing is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.
DCLK	11	13	I	Data Clock. The falling edge of this clock is used to strobe control data for the modem registers in or out on the DATA pin. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$. The falling edge of the $\overline{RD}$ signal must continue for eight cycles of DCLK in order to read all eight bits of the reference register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{INT}$	2	3	O	(with weak pull-up) Modem Interrupt. This output signal is used to inform the modem processor that a change in a modem detect flag has occurred. The processor must then read the Modem Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the Modem Detect Register or does a full reset.
µPRST*	8	10	O	Microprocessor Reset. This output signal is used to provide a hardware reset to the microprocessor. This signal is high if the RESET pin is high or the MCR bit D3 (OUT1) bit is set.
* NOTE: The µPRST pin is an upgraded function which was not included in the initial definition of the SSI 73K222U.				

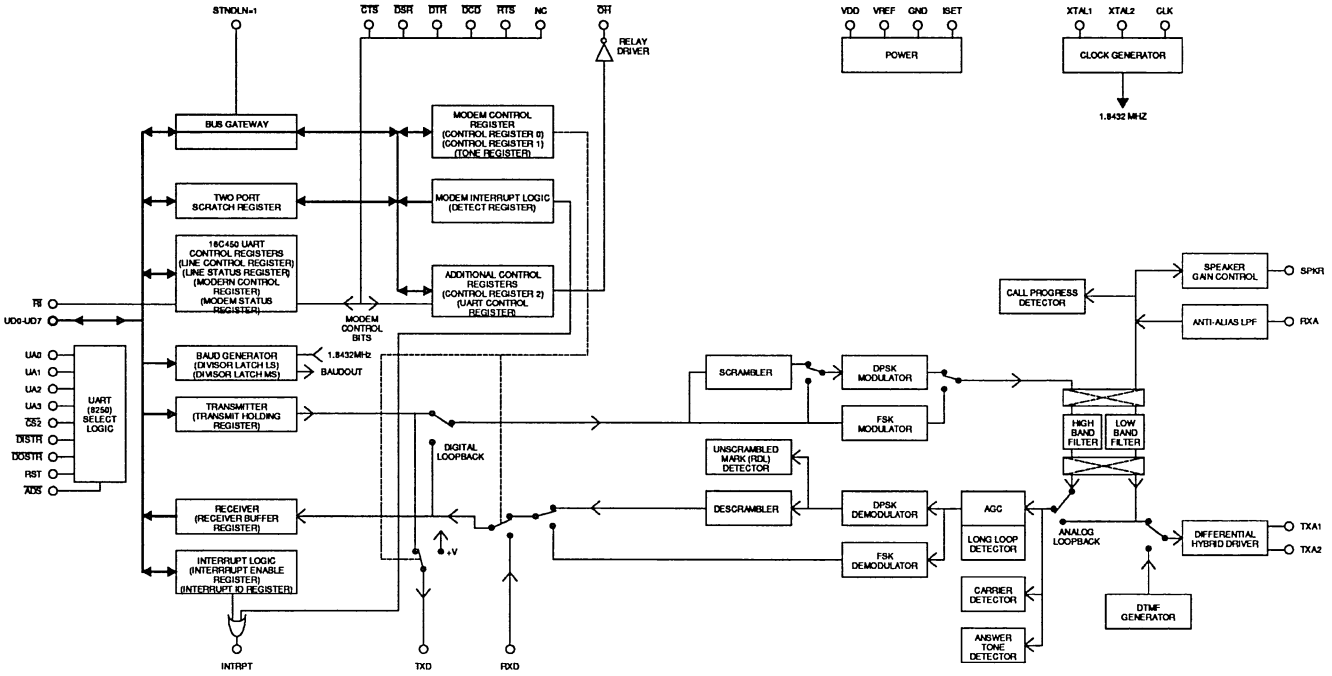


FIGURE 1:
Single-Port Mode

In the single-port mode, the SSI 73K222U is designed to be accessed only by the main CPU using the same parallel bus utilized for data transfer. This mode is enabled when the STNDLN pin is at a logic "1". In the single port mode, internal registers are accessed by the main CPU to configure both the UART section and the modem function, eliminating the need for a separate microcontroller. In this mode, multiplexed pins provide the $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{DED}$ and $\overline{RI}$ signals normally associated with the UART function. A separate pin, $\overline{ADS}$, is used for bus control.

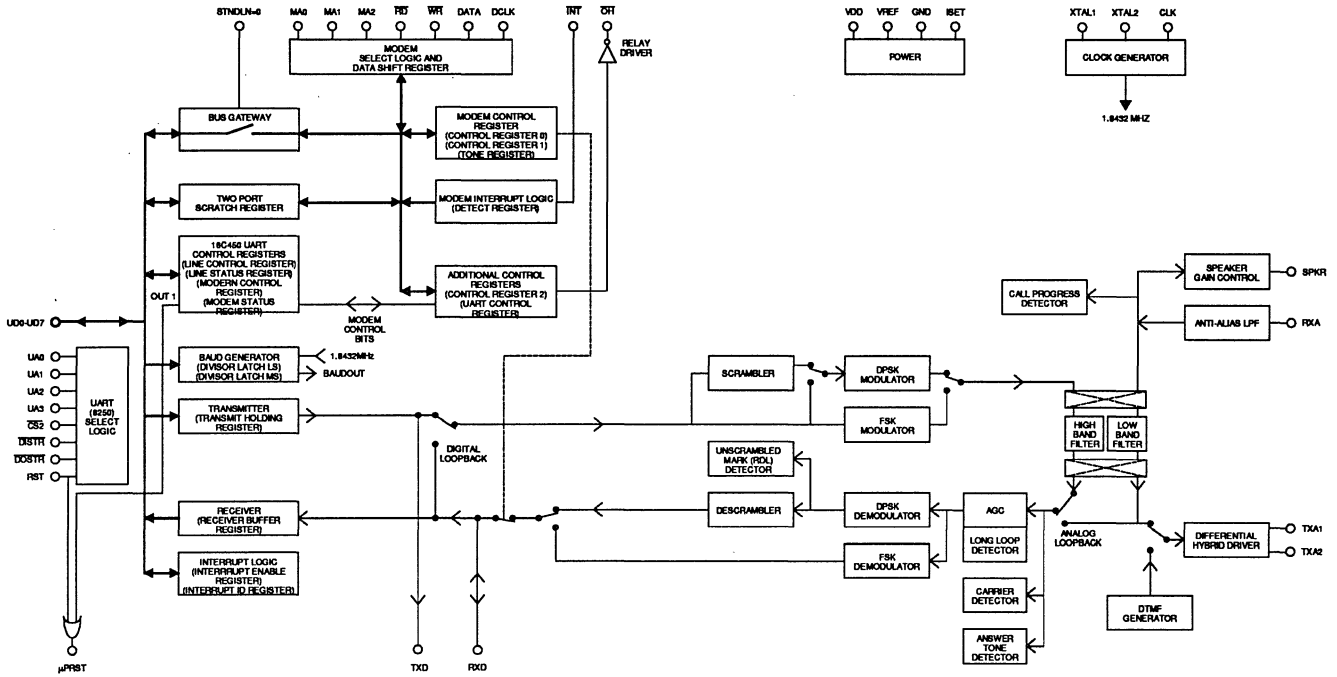


FIGURE 2:
Dual-Port Mode

The dual-port mode allows use of a dedicated microprocessor for control of the modem function, and is enabled when the STNDLN pin = "0". This mode is useful for conventional plug-in card modem designs where it is necessary to make the modem function transparent to the main CPU. In this mode, the SSI 73K222U's multiplexed pins form the serial command bus used to communicate with the external microprocessor. The $\overline{RI}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, and $\overline{DCD}$ logic functions must then be implemented using ports from the dedicated microprocessor.

The serial control interface allows access to the control and status registers via a serial command port. In this mode the MA0, MA1, and MA2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of DCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of DCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

UART CONTROL REGISTER OVERVIEW

REGISTER		UART ADDRESS UA3-UA0*	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	0001 DLAB = 0	0	0	0	ENABLE 8250A/ 16C450 INTERRUPT	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	0010	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	0011	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	0100	0	0	0	LOOP	ENABLE INTERRUPT (OUT2 IN 16C450)	µPRST (OUT1 IN 16C450)	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	0101	0	TRANSMIT SHIFT REG. EMPTY (TSRE)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	0110	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	0111	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	0000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	0001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

* In single-port mode (STNDLN pin = 1), all four address lines UA3-UA0 are used to address the UART Control Registers.

* In dual-port mode (STNDLN pin = 0), only three address lines UA2-UA0 are used to address the UART Control Registers; the UA3 pin becomes the MA2 pin in this mode.

MODEM CONTROL REGISTER OVERVIEW

REGISTER		ADDRESS STNDLN 0 MA2-MA0	ADDRESS STNDLN 1 UA3-UA0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0	CR0	000	1000	MODULATION OPTION	0	MODULATION MODE	POWER ON	CHARACTER SIZE 1 (READ ONLY)	CHARACTER SIZE 0 (READ ONLY)	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1	CR1	001	1001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLE	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	1010	DEVICE SIGNATURE 1	DEVICE SIGNATURE 0	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	ANSWER TONE DETECT	CALL PROGRESS DETECT	LONG LOOP DETECT
TONE CONTROL REGISTER	TONE	011	1011	RXD/TXD CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0 GUARD/ANS. TONE
CONTROL REGISTER 2	CR2	100	1100	RESERVED FOR FUTURE USE							
CONTROL REGISTER 3	CR3	101	1101	SPEAKER VOLUME 1	SPEAKER VOLUME 0	OFF-HOOK	X	X	X	X	X
SCRATCH REGISTER	SCR	110	1110	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UART CONTROL REGISTER	UCR	111	1111	TXCLK (READ ONLY)	X	REQUEST TO SEND (RTS) (READ ONLY)	DATA TERM. READY (DTR) (READ ONLY)	RING INDICATOR (RI)	DATA CARRIER DETECT (DCD)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)

UART REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 0**	**UA3 - UA0 = 0000, DLAB = 0**

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 0**	**UA3 - UA0 = 0000, DLAB = 0**

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 001, DLAB = 0**	**UA3 - UA0 = 0001, DLAB = 0**

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt, when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt, when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Register Interrupt when set to interrupt logic 1.
D4	8250A/16450	1/0	Set for compatibility with 8250A/16C450 UARTS. Reset this bit to disable the gating of the INTRPT interrupt line with the $\overline{\text{DISTR}}$ signal which is needed for 8250B compatibility.
D5 - D7	Not Used	0	These three bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY) **UART SECTION**

STNDLN: **0** **1**

ADDRESS: **UA2 - UA0 = 010** **UA3 - UA0 = 0010**

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired priortized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 011 UA3 - UA0 = 0011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Word Length Select 0			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable	1		This bit is the Parity Enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select	1 or 0		This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's are transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's are transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued)

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Stick Parity	1 or 0		This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		Output of modem is set to a spacing state. When the modem is transmitting DPSK data if the Set Break bit is held for one full character (start, data, parity, stop) the break will be extended to 2 N + 3 space bits (where N = # data bits + parity bit + 1 start + 1 stop). Any data bits generated during this time will be ignored. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TSRE = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 100**	**UA3 - UA0 = 0100**

The MCR register controls the interface with the modem. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers. In single-port mode, bits D1 and D0 are available inverted at the $\overline{RTS}$ and $\overline{DTR}$ pins.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	µPRST* (OUT1 in 16C450)	1	In single-port mode inactive unless loop = 1, then functions as below (D4). In dual-port mode the µPRST pin is the logical OR of this bit and the RESET pin.
D3	Enable Interrupt (OUT2 in 16C450)	0	Sets INTRPT pin to high impedance if STNDLN = 1.
		1	INTRPT output enabled.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART portion of the SSI 73K222U. When bit D4 is set to logic 1, the following occurs: 1. TXD is forced to mark, RXD is ignored. 2. The output of the Transmitter is looped to the Receiver. 3. The four modem control inputs to the UART ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are ignored and the UART signals $\overline{RTS}$, $\overline{DTR}$, Enable Interrupt, and µPRST are forced inactive. 4. The UART signals RTS, DTR, Enable Interrupt, and µPRST are internally connected to the four control signals CTS, DSR, DCD and RI respectively. Note that the Modem Status Register Interrupts are now controlled by the lower four bits of the Modem Control Register. The interrupts are still controlled by the Interrupt Enable Register.
D5 - D7		0	These bits are permanently set to logic 0.

* Note: The µPRST bit has an upgraded function which was not included in the initial definition of the SSI 73K222U.

LINE STATUS REGISTER (LSR) UART SECTION

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 101**	**UA3 - UA0 = 0101**

This register provides status information to the CPU concerning the data transfer.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Data Ready is reset to 0 by reading the data in the Receiver Buffer Register or by writing a 0 into it from the processor.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. The bit is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. A framing error will not occur in DPSK receive from the modem due to the fact that missing stop bits are reinserted.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop) or for two full data words when receiving in DPSK mode from the modem. The BI bit is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) indicates that the Transmitter is ready to accept a new character for transmission. The THRE bit is reset when the CPU loads a character into the Transmit Holding Register.
D6	TSRE	1	The Transmit Shift Empty (TSRE) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty.
D7		0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 110**	**UA3 - UA0 = 0110**

This register provides the current state of the control signals from the modem. In addition, four bits provide change information. The CTS, DSR, DCD, and RI signals come from the UART Control Register if STNDLN = 0 and from the $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$ pins (inverted) if STNDLN = 1. This register is READ ONLY. The delta bits indicate whether the inputs have changed since the last time the Modem Status Register has been read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, µPRST, and Enable Interrupt in the Modem Control Register respectively.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DCTS	1	This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	This bit is the Trailing Edge of the Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed state.
D3	DDCD	1	This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to µPRST in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to Enable Interrupt in the MCR.

UART SECTION

SCRATCH REGISTER (SCR)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 111**	**UA3 - UA0 = 0111**

The Scratch Register is a dual port register which can be simultaneously accessed through both the UART bus and the modem bus.This provides the possibility for the modem controller to communicate directly with the central CPU. Note that if both processors write the Scratch Register, the data stored will be from whichever processor last wrote the register.

DIVISOR LATCH (Least significant byte) (DLL)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 1**	**UA3 - UA0 = 0000, DLAB = 1**

DIVISOR LATCH (Most significant byte) (DLM)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 001, DLAB = 1**	**UA3 - UA0 = 0001, DLAB = 1**

DIVISOR LATCH VALUE VS. DATA RATE

The Divisor Latch is two 8-bit write only registers which control the rate of the programmable baud generator. The programmable baud generator generates an output clock by dividing an internal 1.8432MHz clock by the value stored in the divisor latch. This output clock has a value of 16X the data rate at which the modem will operate. This output clock is available at pin 21 under the control of bit 3 (D3) of the Modem Control Register 1. Upon loading either of the Divisor Latches the 16-bit device counter is immediately loaded, preventing long counts on initial load. The following table shows divisor values for common data rates.

DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED	DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED
50 [1]	2304		4800	24	
75 [1]	1536		7200	16	
110 [1]	1047		9600	12	
134.5 [1]	857	0.058	19200	6	
159 [1]	768		38400	3	
300 [1]	384		56000	2	2.86
600 [2]	192		1. Data Rate valid for FSK transmission.		
1200 [2]	96		2. Data Rate valid for halfspeed DPSK transmission.		
1800	64				
2000	58	0.69	3. Data Rate valid for normal 1200BPS DPSK transmission.		
2400	48				
3600	32				

MODEM REGISTER BIT DESCRIPTIONS

CONTROL REGISTER (CR0)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 000 UA3 - UA0 = 1000

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Answer/Originate	0		Selects Answer Mode (transmit in high band, receive in low band).
		1		Selects Originate Mode (transmit in low band, receive in high band).
D1	Transmit Enable	0		Disables transmit output at TXA.
		1		Enables transmit output at TXA. NOTE: Answer tone and DTMF TX control require Transmit Enable. If Transmit Enable is on, call progress and answer tone detector interrupts are masked.
D2, D3	Character Size 0, 1			These bits are read only. These bits represent the character size. The character size is determined by the UART Line Control Register and includes data, parity (if used), one start bit, and one stop bit.
		D3	D2	Character length
		0	0	8-bit character
		0	1	9-bit character
		1	0	10-bit character
		1	1	11-bit character
D4	Power ON			This bit controls the power down mode of the SSI 73K222U, the analog, and most digital portions of the chip. The digital interface is active during power down.
		0		Power down mode.
		1		Normal operation.
D5	Modulation Mode	0		DPSK
		1		FSK
D6	Reserved	0		Must be written as zero.
D7	Modulation Option	0		DPSK: 1200 bit/s
		1		600 bit/s
		0		FSK: 103 mode
		1		V.21 mode

CONTROL REGISTER (CR1)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 001 UA3 - UA0 = 1001

MODEM SECTION

BIT NO.	NAME	CONDITION		DESCRIPTION
D0, D1	Test Mode	D1	D0	
		0	0	Selects normal operating mode.
		0	1	Analog Loopback Mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the Transmitter. To squelch the TXA pin, transmit enable bit must be forced low.
		1	0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data in TXD is ignored.
		1	1	Selects half-duplex. Internally performs a logical AND of TXD and RXD to send to the UART receiver. Both transmit and receive characters will occur at the Receiver Buffer Register.
D2	Reset	0		Selects normal operation.
		1		Resets modem to power down state. All Control Register bits (CR0, CR1, TONE) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0		CLK pin output is selected to be an 11.0592 MHz crystal echo output.
		1		CLK pin output is selected to be 16 x the Data Rate set by the UART divisor latch.
D4	Bypass Scrambler	0		Selects normal operation. DPSK data is passed through scrambler.
		1		Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path.

CONTROL REGISTER (CR1) (Continued)

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Enable Detect Interrupt	0		Disables interrupts generated by Detect Register bits D1 - D4 at INT pin in dual-port mode, or at INTRPT pin in single-port mode. All interrupts normally disabled in power down modes.
		1		Enables interrupts generated by Detect Register bits D1 - D4 at $\overline{INT}$ pin in dual-port mode, or at INTRPT pin in single-port mode. An interrupt will be generated with a change in status of DR bits D1 - D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode. The interrupt is reset when the DR register is read.
D6, D7	Transmit Pattern	D7	D6	
		0	0	Selects normal data transmission as controlled by the state of the TXD pin.
		0	1	Selects an alternating mark/space transmit pattern for modem testing.
		1	0	Selects a constant mark transmit pattern.
		1	1	Selects a constant space transmit pattern.

DETECT REGISTER (DR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 010 UA3 - UA0 = 1010

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Long Loop	0		Indicates normal received signal.
		1		Indicates low received signal level (< -38 dBm).
D1	Call Progress Detect	0		No call progress tone detected.
		1		Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.
D2	Answer Tone Received	0		No answer tone detected.
		1		Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in Originate Mode for detection of answer tone for normal operation. For CCITT answer tone detection, bit D0 of the Tone Register must be set.
D3	Carrier Detect	0		No carrier detected in the receive channel.
		1		Carrier has been detected in the receive channel.
D4	Unscrambled Marks	0		No unscrambled mark detected.
		1		Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 13.5 ms.
D5	Receive Data			Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Device Signature 0, 1	D7	D6	Product Identified
		0	0	SSI 73K212U
		0	1	SSI 73K221U
		1	0	SSI 73K222U

TONE CONTROL REGISTER (TONE)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 011 UA3 - UA0 = 1011

The Tone Control Register contains information on the tones that are transmitted. Tones are transmitted only if the Transmit Enable bit is set. The priority of the transmit tones are: 1) DTMF, 2) Answer, 3) FSK, 4) Guard.

BIT NO.	NAME	CONDITION				DESCRIPTION
D0	DTMF 0 / Answer/ Guard Tone	D6	D5	D4	D0	D0 interacts with bits D6, D5, and D4 as shown:
		X	X	1	X	Transmit DTMF tones.
		X	1	0	0	Select 2225Hz answer tone (Bell).
		X	1	0	1	Select 2100Hz answer tone (CCITT).
		1	0	0	0	Select 1800Hz guard tone.
		1	0	0	1	Select 550Hz guard tone.
D0, D1, D2, D3	DTMF	Table below				Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below.

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE CONTROL REGISTER (TONE) (Continued)

D4	TX DTMF (Transmit DTMF)	0		Disable DTMF.
		1		Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer Tone)	D5	D0	D5 interacts with bit D0 as shown.
		0	X	Disables answer tone generator.
		1	0	Enables answer tone generator. A 2225Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode.
		1	1	Enables a 2100Hz answer tone generator, with operation same as above.
D6	TX Guard (Transmit Guard Tone)	0		Disables guard tone generator.
		1		Enables guard tone generator. (See D0 for selection of guard tones).
D7	RXD/TXD Control	STNDLN	D7	Function is dependant on status of STNDLN pin.
		0	0	RXD is output data received by modem, TXD is serial output of UART.
		1	0	RXD is electrically an input, but the signal is ignored, TXD is forced to a mark.
		X	1	RXD is serial input to UART, TXD is serial output of UART.

CONTROL REGISTER (CR3)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 101 UA3 - UA0 = 1101

BIT NO.	NAME	CONDITION		DESCRIPTION
D0 - D4	Not Used			Not presently used.
D5	Off Hook	0		Relay driver open.
		1		Open drain driver pulling low.
D6, D7	Speaker Volume 0, 1	D7	D6	Speaker volume control status.
		0	0	Speaker off
		0	1	-24dB
		1	0	-12dB
		1	1	0dB

SCRATCH REGISTER (SCR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 110 UA3 - UA0 = 1110

The Scratch Register is a dual-port register which can be accessed either through the UART bus or the modem bus. It can be used for a communication path outside the data stream.

UART CONTROL REGISTER (UCR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 111 UA3 - UA0 = 1111

The UART Control Register contains the handshaking signals necessary for the microprocessor to communicate with the central CPU through the UART.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	CTS	1	In dual-port mode, CTS, DSR, DCD and RI are writeable locations which can be read through the 16C450 port in the Modem Status Register.
D1	DSR	1	
D2	DCD	1	In the single-port mode, D0 - D3 are ignored and the information for the Modem Status Register comes directly from the external pins.
D3	RI	1	
D4	DTR	1	
D5	RTS	1	DTR and RTS are read only versions of the same register bits in the Modem Contol Register.
D6	Not Used		
D7	TXCLK	Clock	TXCLK is the clock that the UART puts out with TXD. The falling edge of TXCLK is coincident with the transitions of data on TXD. TXCLK can also be used for the microprocessor to send synchronous data independent of the UART by forcing data patterns using CR1 bits 6 and 7 before the rising edge of TXCLK.
NOTE: Control Register 2 (CR2) is reserved for future products and is disabled.			

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

TA = -40°C to 85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD +0.3	V
NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD, Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		85	°C
External Component (Refer to application drawing for placement.)					
VREF Bypass Capacitor [1]	(VREF to GND)	0.1			µF
Bias Setting Resistor [1]	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor [1]	ISET pin to GND	0.1			µF
VDD Bypass Capacitor [1]	(VDD to GND)	0.1			µF
XTL1 Load Capacitor	From pin to GND			40	pF
XTL2 Load Capacitor	From pin to GND			20	pF
Input Clock Variation	(11.0592 MHz)	-0.01		+0.01	%
Hybrid Loading					
R1	See Figure 3		600		Ω
R2			600		Ω
C	TXA Hybrid Loading		0.033		µF

1. Optional for minimum worst case current consumption.
2. Minimum for optimized system layout; may require higher values for noisy environments.

DC ELECTRICAL CHARACTERISTICS
TA = -40°C to +85 °C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
IDD, Supply Current					
IDDA, Active	ISET Resistor = 2MΩ		8	12	mA
IDDA, Active	ISET = GND		8	15	mA
IDD1, Power-Down	CLK = 11.0592MHz		3	4	mA
IDD2, Power-Down	CLK = 19.200KHz		2	3	mA
Digital Inputs					
Input High Current IIH	VI = VDD			100	µA
Input Low Current IIL	VI = 0	-200			µA
Input Low Voltage VIL				0.8	V
Input High Voltage VIH	Except RESET & XTL1	2.0			V
Input High Voltage VIH	RESET & XTL1	3.0			V
Pull Down Current RESET PIN		5		30	µA
Input Capacitance				10	pF
Digital Outputs					
Output High Voltage VOH	IOUT = - 1 mA	2.4		VDD	V
VOL UD0-UD7 and INTRPT	IOUT = 3.2 mA			0.4	V
VOL other outputs	IOUT = 1.6 mA			0.4	V
CLK Output VOL	IOUT = 3.2 mA			0.6	V
OH Output VOL	IOUT = 20 mA			1.0	V
OH Output VOL	IOUT = 10 mA			0.5	V
Offstate Current INTRPT pin	VO = 0V	-20		20	µA
Capacitance					
Inputs	Input Capacitance			10	pF
CLK	Maximum capacitive load to pin			15	pF
Analog Pins					
RXA Input Resistance			200		KΩ
RXA Input Capacitance				25	pF

DYNAMIC CHARACTERISTICS AND TIMING
TA = -40°C to +85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	ANS TONE 2225 or 2100 Hz	-11	-10.0	-9	dBm0
	DPSK TX Scrambled Marks	-11	-10.0	-9	dBm0
	FSK Dotting Pattern	-11	-10.0	-9	dBm0
FSK Tone Error	Bell 103 or V.21			±5	Hz
DTMF Generator					
Freq. Accuracy		-.25		.25	%
Output Amplitude	Low Band, not in V.21 mode	-10	-9	-8	dBm0
Output Amplitude	High Band, not in V.21 mode	-8	-7	-6	dBm0
Long Loop Detect	DPSK or FSK	-40		-32	dBm0
Demodulator Dynamic Range	DPSK or FSK		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600Hz Band	-39		0	dBm0
Reject Level	2-Tones in 350-600Hz Band			-46	dBm0
Delay Time	-70dBm0 to -30dBm0 Step	27		80	ms
Hold Time	-30dBm0 to -70dBm0 Step	27		80	ms
Hysteresis		2			dB
Carrier Detect	DPSK or FSK Receive				
Threshold	Data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	15		45	ms
Hysteresis		2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 Step	10		24	ms
Answer Tone Detector					
Detect Level Threshold	In FSK mode	-49.5		-42	dBm0
Delay Time	-70dBm0 to -30dBm0 STEP	20		45	ms
Hold Time	-30dBm0 to -70dBm0 STEP	10		30	ms
Detect Frequency Range		-2.5		+2.5	%

1. All units in dBm0 are measured at the line input to the transformer. The interface circuit inserts an 8 dB loss in the transmit path (TXA1 - TXA2 to line), and a 3dB loss in the receive path (line to RXA).

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
Speaker Output					
Gain Error		-1		+1	dB
Output Swing SPKR	10K||50pF LOAD 5% THD	2.75			VP
Carrier VCO					
Capture Range	Originate or Answer	-10		10	Hz
Capture Time	-10Hz to +10Hz Carrier Frequency change assumed		40	100	ms
Recovered Clock					
Capture Range	% of Center Frequency	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin.		30	50	ms
Guard Tone Generator					
Tone Accuracy	550 or 1800Hz	-20		+20	Hz
Tone Level	550HZ	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800HZ	-7.0	-6.0	-5.0	dB
Harmonic Distortion	700 to 2900HZ			-60	dB

SERIAL BUS INTERFACE (See Figure 4)
The following times are for CL = 100pF.

PARAMETER		MIN	NOM	MAX	UNIT
TRD	Data out from Read	0		140	ns
TCKD	Data out after Clock			200	ns
TRDF	Data Float after Read	0		200	ns
TRCK	Clock High after Read	200			ns
TWW	Write Width	140		10000	ns
TDCK	Data Setup Before Clock	150			ns
TCKH	Data Hold after Clock	20			ns
TCKW	Write after Clock	150			ns
TACR	Address setup before Control [1]	50			ns
TCAR	Address Hold after Control [1]	50			ns
TACW	Address setup before Write	50			ns
TCAW	Address Hold after Write	50			ns

1. Control is later of falling edge of RD or DCLK.

PARALLEL BUS INTERFACE (See Figure 5) The following times are for Cl = 100pF.

PARAMETER		MIN	MAX	MIN	MAX	UNIT
		Dual-Port Mode		Single-Port Mode		
RC	Read Cycle = TAD + TRC	240		340		ns
TDIW	DISTR Width	80		80		ns
TDDD	Delay DISTR to Data (read time)		80		80	ns
THZ	DISTR to Floating Data Delay	0	50	0	50	ns
TRA	Address Hold after DISTR	20		20		ns
TRCS	Chip select hold after DISTR	20		20		ns
TAR	DISTR Delay after Address	20		20		ns
TCSR	DISTR Delay after Chip Select	20		20		ns
WC	Write Cycle = TAW + TDOW + TWC	140		140		ns
TDOW	DOSTR Width	80		80		ns
TDS	Data Setup	30		50		ns
TDH	Data Hold	20		20		ns
TWA	Address Hold after DOSTR	20		20		ns
TWCS	Chip select hold after DOSTR	20		20		ns
TAW	DOSTR delay after Address	20		20		ns
TCSW	DOSTR delay after Chip Select	20		20		ns
TADS	Address Strobe Width			40		ns
TAS	Address Setup Time			30		ns
TAH	Address Hold Time			0		ns
TCS	Chip Select Setup Time			30		ns
TCH	Chip Select Hold Time			0		ns
TRC	Read Cycle Delay	40		40		ns
TWC	Write Cycle Delay	40		40		ns
TAD	Address to Read Data	200		300		ns

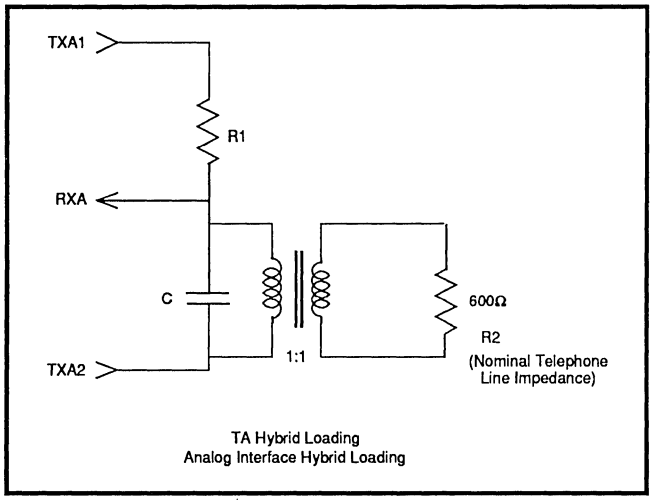


FIGURE 3: TXA Hybrid Loading Analog Interface Hybrid Loading

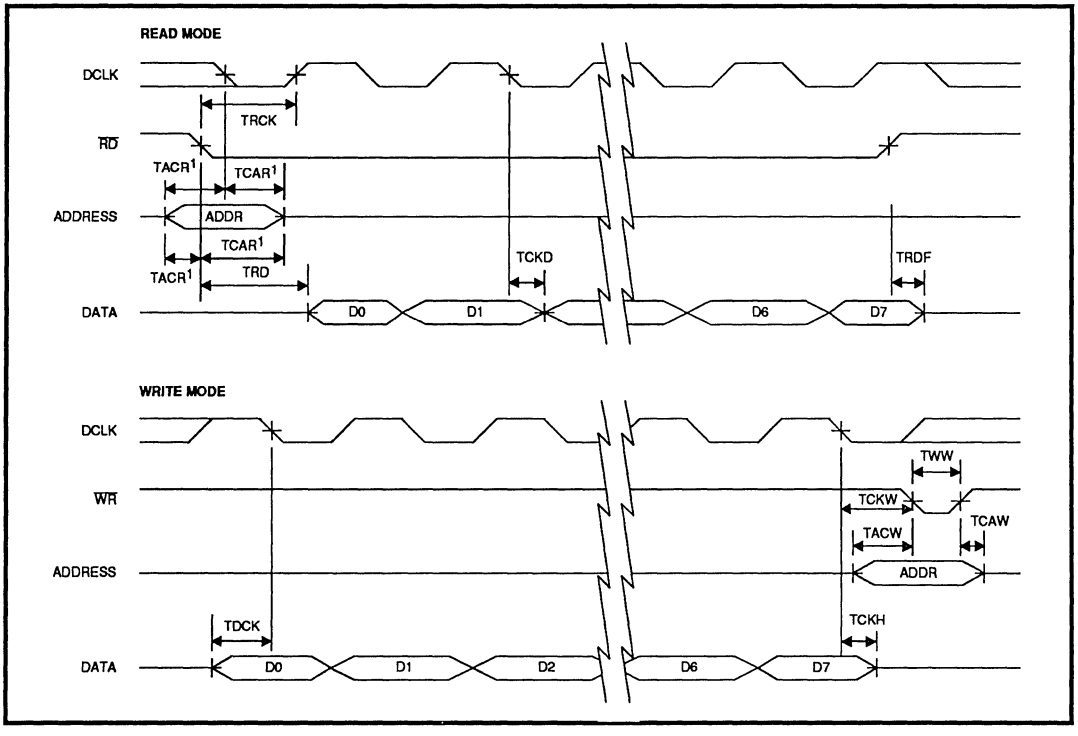


FIGURE 4: Modem Serial Bus Timing

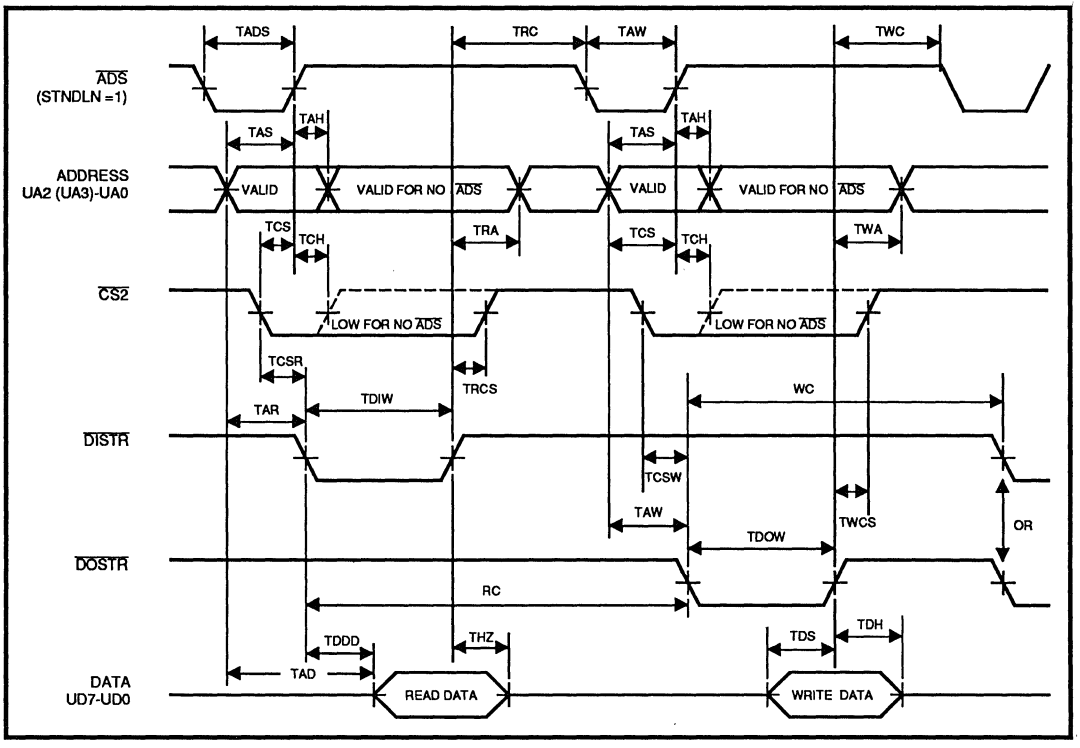


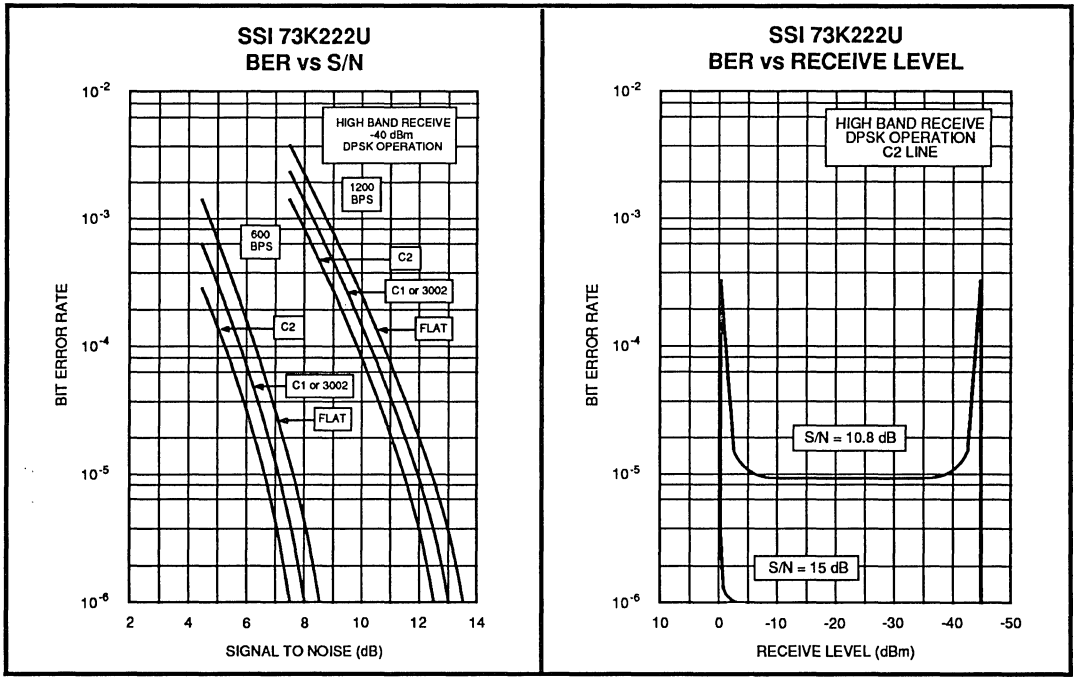
FIGURE 5: UART Bus Timing

TYPICAL PERFORMANCE CHARACTERISTICS

The SSI 73K222U was designed using an integrated analog/digital architecture that offers optimum performance over a wide range of line conditions. The SSI 73K222U utilizes the circuit design proven in SSI's 73K222L one-chip modem, with added enhancements which extend low signal level performance and increase immunity to spurious noise typically encountered in integral bus applications. The SSI 73K222U provides excellent immunity to the types of disturbances present with usage of the dial-up telephone network. The following curves show representative Bit Error Rate performance under various line conditions.

BER vs S/N

This test measures the ability of the modem to function with minimum errors when operating over noisy lines. Since some noise is generated by even the best dial-up lines, the modem must operate with as low a S/N ratio as possible. Optimum performance is shown by curves that are closest to the zero axis. A narrow spread between curves for the four line conditions indicates minimal variation in performance when operating over a range of line qualities and is typical of high performance adaptive equalization receivers. High band receive data is typically better than low band due to the inherent design of PSK modems.

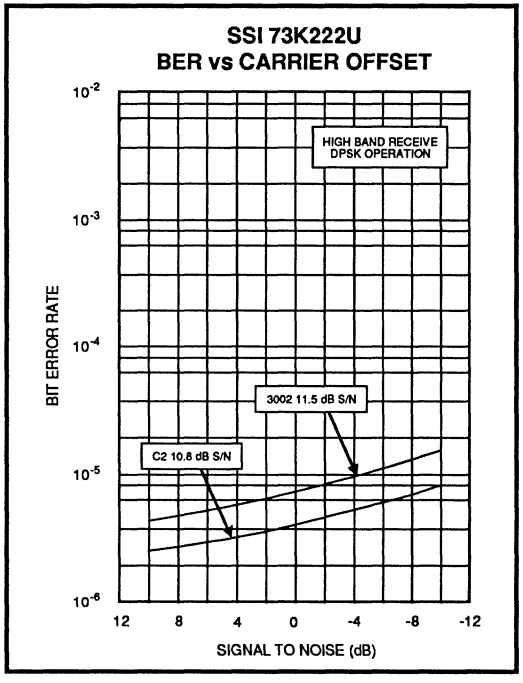


BER vs Receive Level

This measures the dynamic range of the modem. As signal levels vary widely over dial-up lines, the widest dynamic range possible is desirable. The minimum Bell specification calls for 36dB of dynamic range. S/N ratios were held constant at the indicated values while receive level was lowered from very high to very low signal levels. The "width of the bowl" of these curves taken at the 10^{-4} BER point is a measure of the dynamic range.

BER vs Carrier Offset

This parameter indicates how the modem performance is impacted by frequency shifts encountered in normal PSTN operation. Flat curves show no performance degradation from frequency offsets. The SSI K-Series devices use a 2nd order carrier tracking phase-locked-loop, which is insensitive to carrier offsets in excess of 10Hz. The Bell network specifications allow as much as 7Hz offset, and the CCITT specifications require modems to operate with 7Hz of offset.



APPLICATION

The SSI 73K222U includes additional circuitry to greatly simplify integral modem designs in either of two different configurations. The single-port mode represents the most efficient implementation for an integral modem. Figure 9 shows a typical schematic using this mode. In this configuration, the SSI 73K222U transfers data and commands through the single parallel port. All modem control is provided by the main CPU, eliminating the need for an external microcontroller and supporting components. The SSI 73K222U is unique in that access to both the UART and modem sections is possible through the UART port. Also shown is a separate serial port, which can be used independent of the modem function when the modem section is inactive. Figure 10 shows a more conventional integral modem design, in which a local microprocessor handles modem supervision, allowing the modem function to be transparent to the main processor. Inclusion of the hybrid drivers, audio volume control, and off hook relay driver reduces component count for a highly efficient design. In either mode of operation, the SSI 73K222U's ability to operate from a single +5 volt power supply eliminates the need for additional supply voltages and keeps power usage to a minimum.

(See Figure 9 & 10: Typical Integral Applications Single and Dual-Port Modes.)

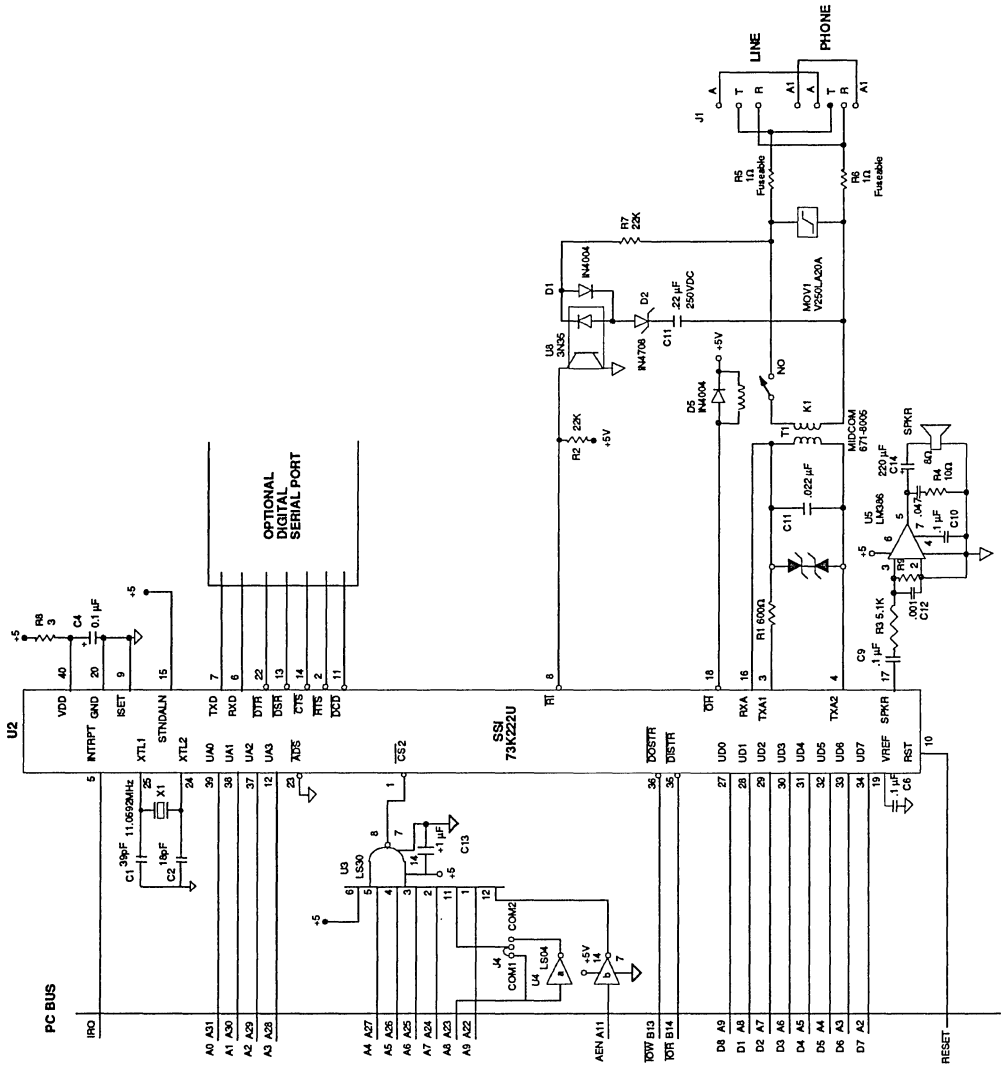


FIGURE 9:
73K22U Typical Integral Application
Single-Port Mode

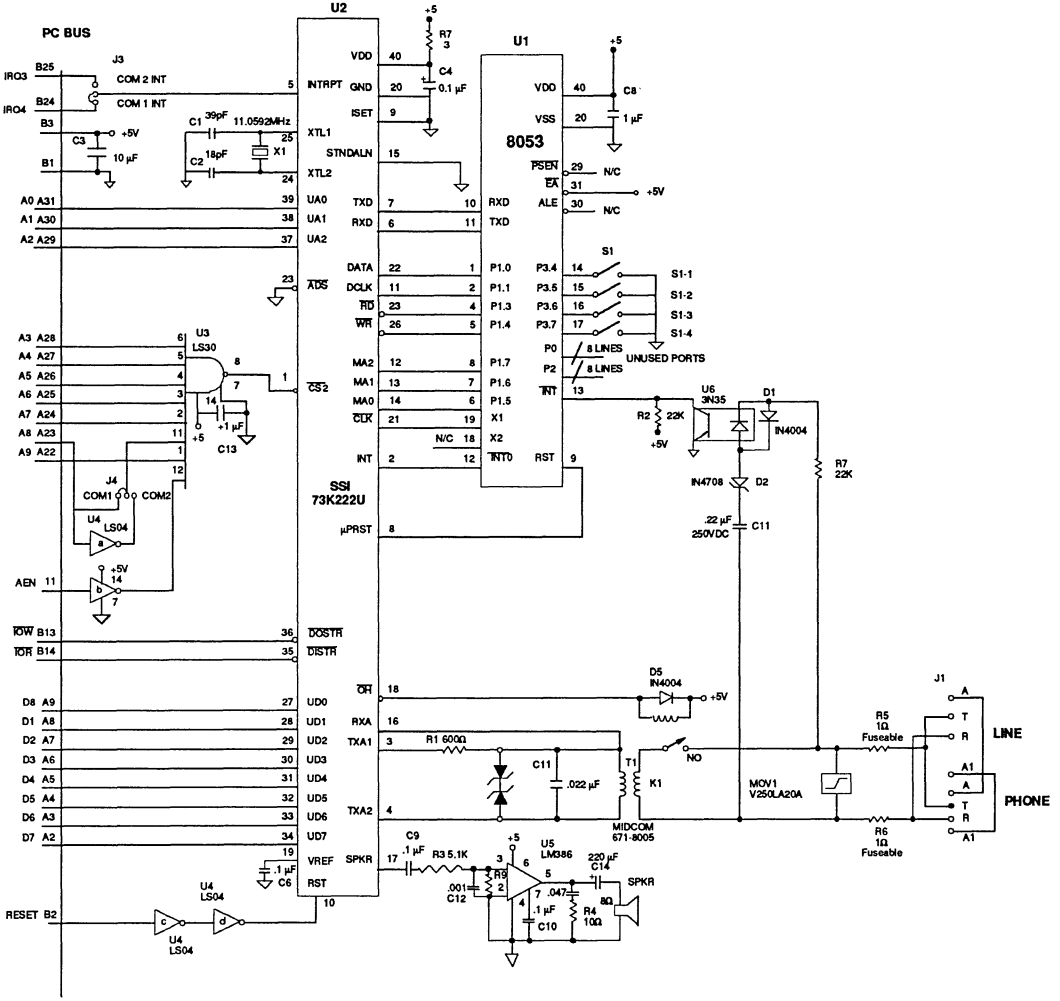
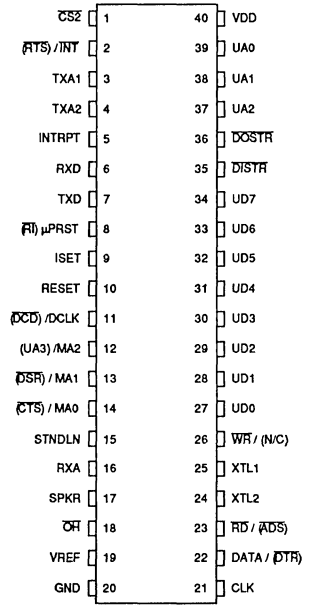


FIGURE 10:
73K22U Typical Integral Application
Dual-Port Mode

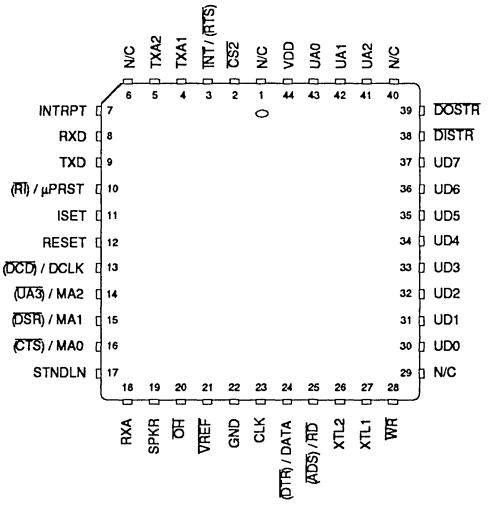
PACKAGE PIN DESIGNATIONS

(TOP VIEW)



600-Mil
40-Pin DIP

Parentheses indicate single-port mode.



44-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K222U		
40-Pin Plastic Dual-In-Line	SSI 73K222U – IP	73K222U – IP
44-Pin Plastic Leaded Chip Carrier	SSI 73K222U – IH	73K222U – IH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 731-5457

Notes:

SSI 73K224L
V.22 bis/V.22/V.21, Bell 212A/103 Single-Chip Modem

1

July, 1990

DESCRIPTION

The SSI 73K224L is a highly integrated single-chip modem IC which provides the functions needed to construct a V.22 bis compatible modem, capable of 2400 bit/s full-duplex operation over dial-up lines. The SSI 73K224L offers excellent performance and a high level of functional integration in a single 28-pin DIP. This device supports V.22 bis, V.22, V.21, Bell 212A and Bell 103 modes of operation, allowing both synchronous and asynchronous communication. The SSI 73K224L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular single-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications normally occur through a separate serial port. The SSI 73K224L is pin and software compatible with the SSI 73K212L and SSI 73K222L single-chip modem ICs, allowing system upgrades with a single component change.

The SSI 73K224L operates from a single +5 volt supply for low power consumption.

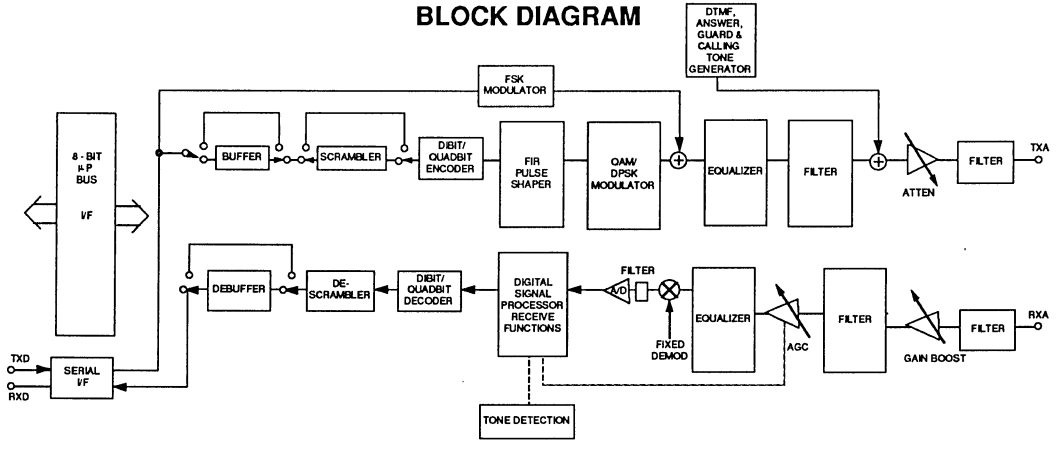
The SSI 73K224L is ideal for use in either free-standing or integral system modem products where full-duplex

(Continued)

FEATURES

- One-chip multi-mode V.22 bis/V.22/V.21 and Bell 212A/103 compatible modem data pump
- FSK (300 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding
- Pin and software compatible with other SSI K-Series 1-chip modems
- Interfaces directly with standard microprocessors (8048, 80C51 typical)
- Parallel microprocessor bus (28-pin DIP, 32- and 44-pin PLCC) for control
- Selectable asynch/synch with internal buffer/de-buffer and scrambler/descrambler functions
- All synchronous and asynchronous operating modes (internal, external, slave)
- Adaptive equalization for optimum performance over all lines
- Programmable transmit attenuation (16 dB, 1 dB steps), selectable receive boost (+12 dB)
- Call progress, carrier, answer tone, unscrambled mark, S1, and signal quality monitors
- DTMF, answer and guard tone generators
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit, S1 pattern
- CMOS technology for low power consumption (125 mW @ 5V) with power-down mode (30 mW @ 5V)
- TTL and CMOS compatible inputs and outputs

BLOCK DIAGRAM



DESCRIPTION (Continued)

2400 bit/s data communications over the 2–wire switched telephone network is desired. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability.

The SSI 73K224L is designed to be a complete V.22 bis compatible modem on a chip. The complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. Many functions were included to simplify implementation of typical modem designs. In addition to the basic 2400 bit/s QAM, 600/1200 bit/s DPSK and 300 bit/s FSK modulator/demodulator sections, the device also includes SYNCH/ASYNCH converters, scrambler/descrambler, call progress tone detect, DTMF tone generator capabilities and handshake pattern detectors. V.22 bis, V.22, V.21 and Bell 212A/103 modes are supported (synchronous and asynchronous) and test modes are provided for diagnostics. Most functions are selectable as options and logical defaults are provided.

OPERATION

QAM MODULATOR/DEMODULATOR

The SSI 73K224L encodes incoming data into quad-bits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K224L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). Adaptive equalization is also used in DPSK modes for optimum operation with varying line conditions.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) are used when this mode is selected. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communication with asynchronous terminals which may communicate at 600,1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01%. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where quad-bit/di-bit

encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking, FSK, and synchronous operation as selected. The device recognizes a break signal and handles it in accordance with Bell 212A specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted at the same rate as it is input.

PARALLEL BUS INTERFACE

Seven 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Five control registers are read/write memory. The detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and the TX DTMF mode bit previously loaded into the tone register. Transmission of DTMF tones is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	32-PIN	44-PIN	TYPE	DESCRIPTION
GND	28	32	44	I	System Ground.
VDD	15	17	23	I	Power supply input, 5V -5% +10%. Bypass with .1 µF and 22 µF capacitors to GND.
VREF	26	30	42	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	27	36	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

NAME	28-PIN	32-PIN	44-PIN	TYPE	DESCRIPTION
ALE	12	14	20	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	4, 6-12	4,9-15	I/O	Address/data bus. These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	20	23	32	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	1	1	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	19	25	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	16	22	I	Read. A low requests a read of the SSI 73K224L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	28	37	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	13	15	21	I	Write. A low on this informs the SSI 73K224L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active (low).
Note:	The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.				

DTE USER INTERFACE

NAME	28-PIN	32-PIN	44-PIN	TYPE	DESCRIPTION
EXCLK	19	22	31	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	26	35	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be active as long as a carrier is present.
RXD	22	25	34	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	20	26	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	24	33	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (2400/1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

NAME	28-PIN	32-PIN	44-PIN	TYPE	DESCRIPTION
RXA	27	32	43	I	Received modulated analog signal input from the phone line.
TXA	16	18	24	O	Transmit analog output to the phone line.
XTL1 XTL2	2 3	2 3	2 3	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

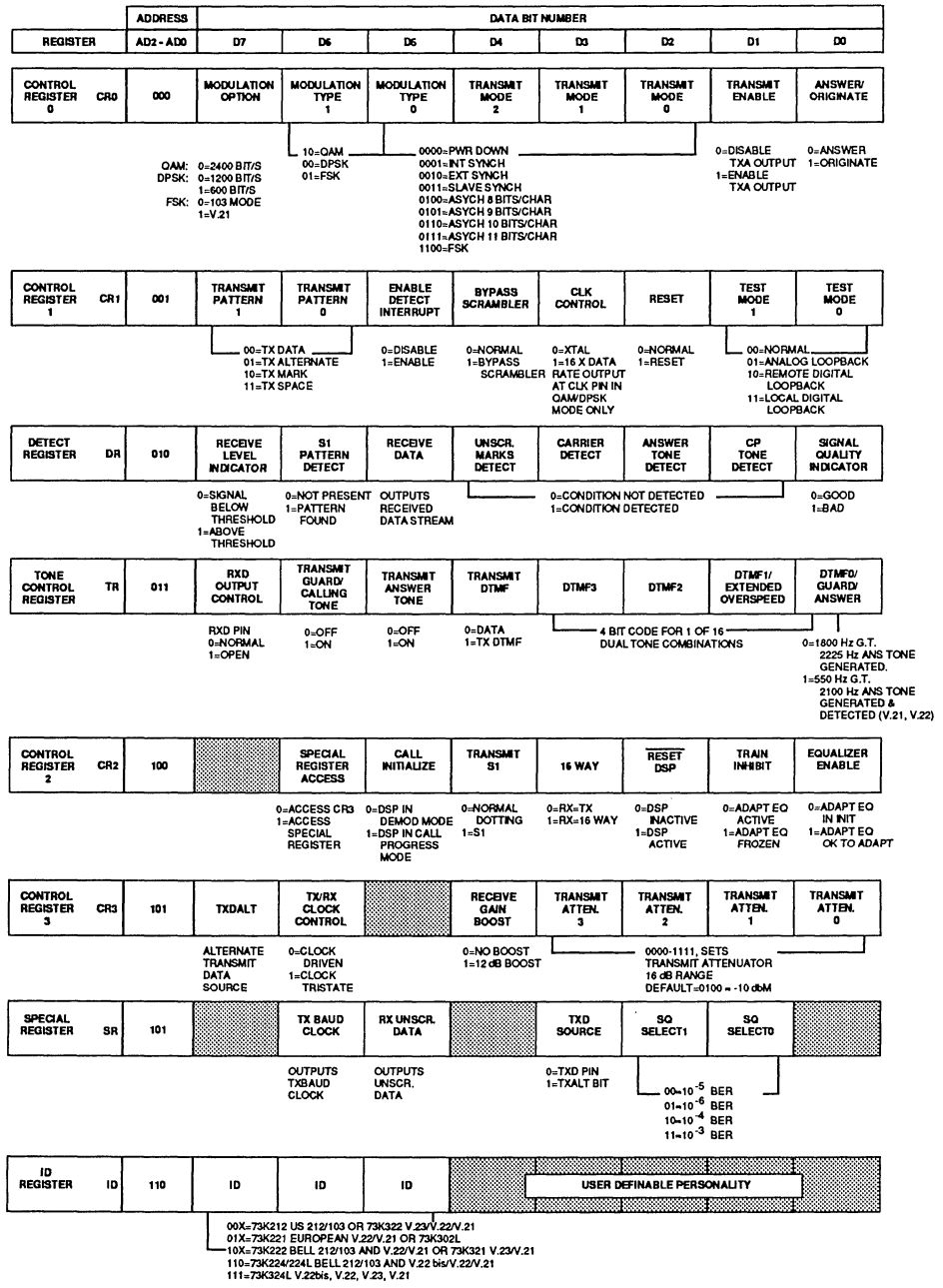
Seven 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K224L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ EXTENDED OVERSPEED	DTMF0/GUARD/ ANSWER
CONTROL REGISTER 2 CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3 CR3	101	TXDALT	TX/RX CLOCK CONTROL	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
SPECIAL REGISTER SR	101		TX BAUD CLOCK	RX UNSCR. DATA		TXD SOURCE	SQ SELECT 1	SQ SELECT 0	
ID REGISTER ID	110	1	1	1	USER DEFINABLE PERSONALITY				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone or DTMF.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	0	QAM selects 2400 bps. DPSK selects 1200 bps. FSK selects 103 mode.
		1	DPSK selects 600 bps. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	Clock Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK/ QAM modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONE DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Signal Quality	0	Indicates normal received signal.
		1	Indicates low received signal quality (above average error rate).
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONE DETECT	CALL PROG.	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Received	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone in Bell mode (TR bit D0=0) or 2100 Hz if in CCITT mode (TR bit D0=1). The device must be in originate mode for detection of answer tone.
D3		0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0	No S1 pattern being received.
		1	S1 pattern detected. Should be time qualified by software. S1 pattern is defined as a double di-bit (001100..) unscrambled 1200 bit/s DPSK signal. Pattern must be aligned with baud clock to be detected.
D7	Receive Level	0	Received signal level below threshold, (≈ -21 dBm0);can use receive gain boost (+12 dB).
		1	Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 1 0 0	Select Bell mode answer tone. Interacts with DR bit D2 and TR bit D5.
(Continued)		X 1 0 1	Select CCITT mode answer tone. Interacts with DR bit D2 and TR bit D5.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Extended Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM or DPSK +1.0% -2.5%.
		0 1	Asynchronous QAM or DPSK +2.3% -2.5%.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336
*	1 0 1 1	941 1209
#	1 1 0 0	941 1477
A	1 1 0 1	697 1633
B	1 1 1 0	770 1633
C	1 1 1 1	852 1633
D	0 0 0 0	941 1633

D4	TX DTMF (Transmit DTMF)	0	Disable DTMF.
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown. Also interacts with DR bit D2 in originate mode. See Detect Register description.
		0 0 X	Disables answer tone generator.
		1 0 0	In answer mode, a Bell 2225 Hz tone is transmitted continuously when the Transmit Enable bit is set.
		1 0 1	Likewise, a CCITT 2100 Hz answer tone is transmitted.
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator. (See D0 for selection of guard tones.)
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This signal is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.

CONTROL REGISTER 2 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Transmit	0	The transmitter when placed in QAM alternating mark/space mode transmits 0101..... scrambled or not dependent on the bypass scrambler bit.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the various mode bits.
		1	The DSP decodes both answer tone and call progress tones.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the SPECIAL REGISTER. See the SPECIAL REGISTER for details.
D7	Not used at this time	0	Only write zero to this bit.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	0	0	0	RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Sets the attenuation level of the transmitted signal in 1dB steps. The default (D3-D0=0100) is for a transmit level of -10 dBm0 at the line with the recommended hybrid transmit gain. The total range is 16 dB.
D4	Receive Gain Boost	0	12 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D7, D6, D5	Not used at this time	0	Only write zeros to these bits.

SPECIAL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
SR 101		TXBAUD CLOCK	RXUN-DSCR DATA		TXD SOURCE	SIGNAL QUALITY LEVEL SELECT1	SIGNAL QUALITY LEVEL SELECT0	

BIT NO.	NAME	DESCRIPTION
D7, D4, D0		NOT USED AT THIS TIME. Only write ZEROs to these bits.
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.
D5	RXUNDSCR DATA	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.
D3	TXD SOURCE	This bit selects the transmit data source; either the TXD pin if ZERO or the TXDALT if this bit is a ONE. The TRANSMIT PATTERN bits D7 and D6 in CR1 override either of these sources.
D2, D1	SIGNAL QUALITY LEVEL SELECT	The signal quality indicator is a logical ONE when the signal received is not acceptable for low error rate reception. It is determined by the value of the Mean Squared Error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a ONE constantly. The SQI bit and threshold selection are valid for QAM and DPSK only.

D2	D1	THRESHOLD VALUE	UNITS
0	0	10^{-5}	BER (default)
0	1	10^{-6}	BER
1	0	10^{-4}	BER
1	1	10^{-3}	BER

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a ONE and addressing CR3. This register provides functions to the 73K224L user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a ZERO.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID	ID 2	ID 1	ID 0	USER DEFINABLE PERSONALITY				

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5 110	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212(L) or 73K322L
		0 1 X	SSI 73K221(L) or 73K302L
		1 0 X	SSI 73K222(L)
		1 1 0	SSI 73K224L
		1 1 1	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.75	5	5.5	V
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(VDD to GND)	0.1			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
XTL1 Load Capacitance	Depends on crystal requirements			40	pF
XTL2 Load Capacitance	Depends on crystal requirements			20	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		55	°C

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 55°C, VDD =recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
	ISET Resistor = 2 MΩ				
IDD1, Active			25	27	mA
IDD2, Idle			3	5	mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VIH MAX			100	µA
IIL, Input Low Current	VI = VIL MIN	-200			µA
Reset Pull-down Current	Reset = VDD	5		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
VOL, CLK Output	IOUT = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-5		-50	µA
Capacitance					
Maximum Capacitive Load					
CLK	Maximum permitted load			15	pF
Input Capacitance	All Digital Inputs			10	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +55°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks ATT=0100 (default)	-11.5	-10.0	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-.31		+.05	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
Output Distortion	All products through BPF			-45	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD	-5		+5	%
2100 Hz Answer Tone Generator					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21	-11.5	-10	-9	dBm0
Output Distortion	All products though BPF			-40	dB
NOTE: Parameters expressed in dBm0 refer to the following definition: 0 dB loss in the Transmit path to the line. 2 dB gain in the Receive path from the line. Refer to the Basic Box Modem diagram in the Applications section for the DAA design.					
DTMF Generator	Not in V.21				
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band, ATT = 0100, DPSK Mode	-10		-8	dBm0
Output Amplitude	High Band, ATT = 0100, DPSK Mode	-8		-6	dBm0
Twist	High-Band to Low-Band, DPSK Mode	1.0	2.0	3.0	dB
Receiver Dynamic Range	Refer to Performance Curves	-48		-3.0	dBm0
Call Progress Detector	In Call Init mode				
Detect Level	460 Hz test signal	-34		0	dBm0
Reject Level				-50	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			25	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
DTMF Generator						
Freq. Accuracy			-.25		+.25	%
Output Amplitude		Low Band ATT = 0100	-10		-8	dBm0
Output Amplitude		High Band ATT = 0100	-8		-6	dBm0
Twist		High-Band to Low-Band	1.0	2.0	3.0	dB
Receiver Dynamic Range		Refer to Performance Curves	-48		-3	dBm0
Carrier Detect						
Threshold		FSK	-51		-38	dBm0
		QAM/DPSK receive data	-49		-42	dBm0
Hysteresis		All Modes	2			
Delay Time	DPSK	-70 dBm0 to -6 dBm0	15	20	25	ms
		-70 dBm0 to -40 dBm0	10	20	25	ms
	QAM	-70 dBm0 to -6 dBm0	25	30	35	ms
		-70 dBm0 to -40 dBm0	25	33	41	ms
Hold Time	DPSK	-6 dBm0 to -70 dBm0	15	22	28	ms
		-40 dBm0 to -70 dBm0	10	15	20	ms
	QAM	-6 dBm0 to -70 dBm0	54	60	66	ms
		-40 dBm0 to -70 dBm0	21	26	31	ms
Answer Tone Detectors						
Detect Level			-48		-43	dBm0
Detect Time		Call Init Mode for signals from	7		37	ms
Hold Time		-6 to -40 dBm0, 2100 or 2225 Hz	10		48	ms
Detect Time		Demod Mode for signals from	4		26	ms
Hold Time		-6 to -40 dBm0, 2100 or 2225 Hz	11		43	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Pattern Detectors	DPSK Mode				
S1 Pattern					
Delay Time	For signals from -6 to -40 dBm0,	5		65	ms
Hold Time	-6 to -40 dBm0, Demod Mode	5		45	ms
Unscrambled Mark					
Delay Time	For signals from -6 to -40	5		38	ms
Hold Time	Demod or call Init Mode	5		47	ms
Receive Level Indicator					
Detect On				19	dBm0
Valid after Carrier Detect		10			ms
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output load	TXA pin; FSK Single	10			KΩ
	Tone out for THD = -50 dB in .3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy	4 kHz, Guard Tones off			-35	dBm0
	10 kHz, Guard Tones off			55	dBm0
	12 kHz, Guard Tones off			65	dBm0
Anti Alias Low Pass Filter					
Out of Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Level at RXA pin with receive Boost Enabled				
	Scrambled data at 2400 bit/s in opposite band			-14	dBm
	Sinusoids out of band			-9	dBm
Transmit Attenuator					
Range of gain	Default ATT=0100 (0 dBm0)	+4		-11	dB
Step Accuracy		-0.15		+0.15	dB
Output Impedance			200	300	Ω
Clock Noise					
	TXA pin; 153.6 kHz			1.5	mVrms
Carrier Offset					
Capture Range	Originate or Answer		±7	±10	Hz

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

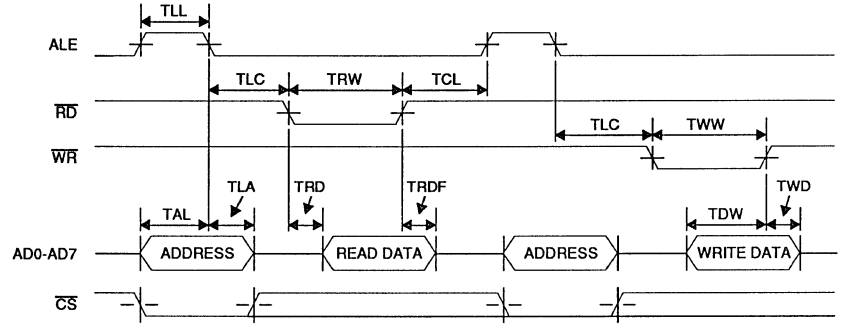
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Recovered Clock					
Capture Range	% of frequency originate or answer	-.024		+.024	%
Guard Tone Generator					
Tone Accuracy	550 Hz			+1.18	%
	1800 Hz	-0.7			
Tone Level	550 Hz	-5.0	-3.5	-2.0	dB
(Below QAM/DPSK Output)	1800 Hz	-8.0	-6.5	-5.0	dB
Harmonic Distortion	550 Hz			-60	dB
(700 to 2900 Hz)	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}/\overline{WR}$ Low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		200	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000*	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control**	50			ns
TCA	Address hold after control**	50			ns
TWH	Data Hold after EXCLK	20			ns

* Maximum time applies to parallel version only.

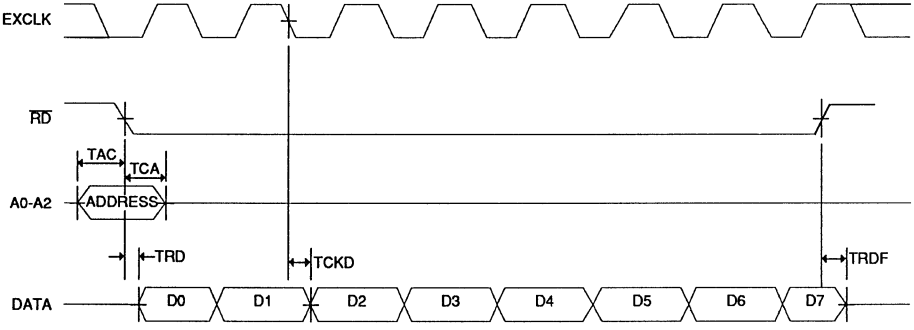
** Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

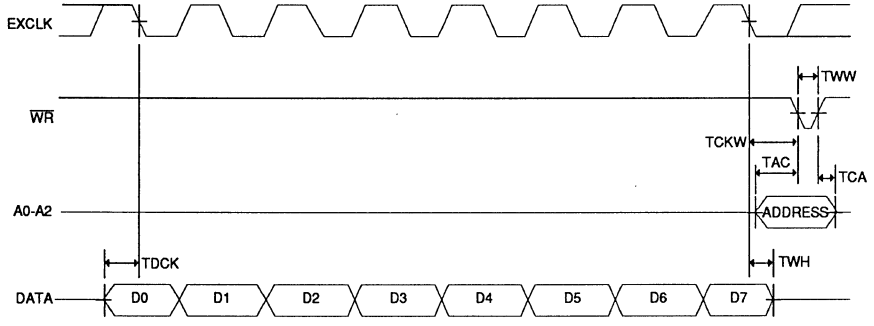
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

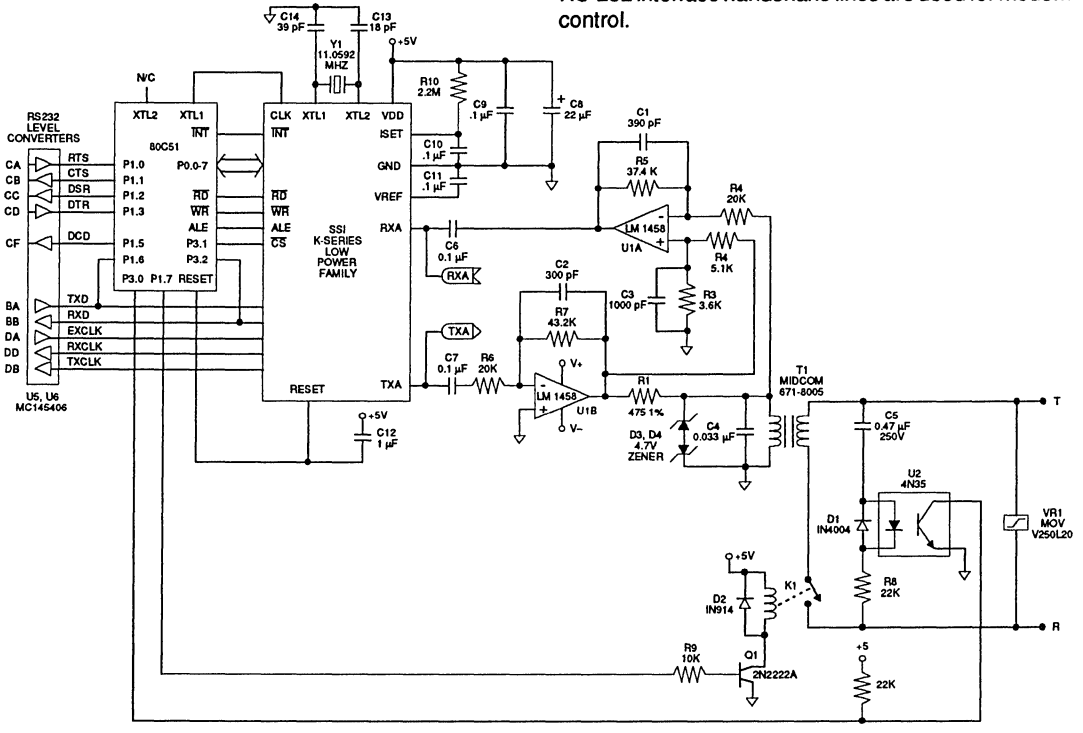


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

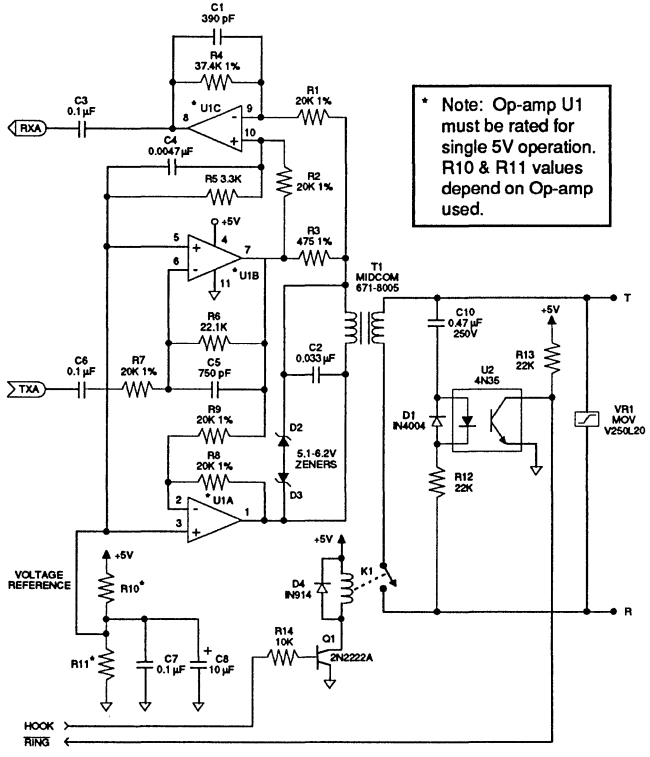


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

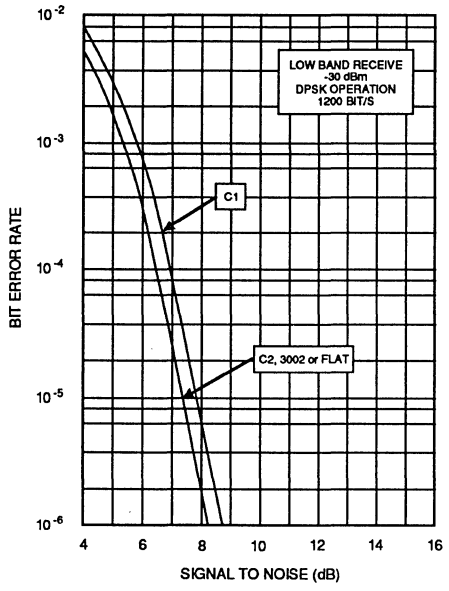
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

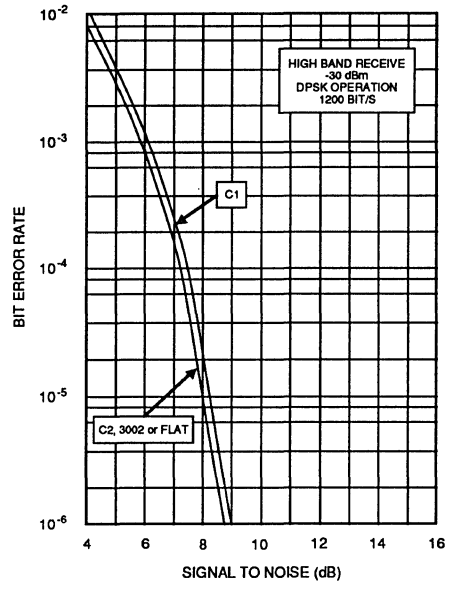
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

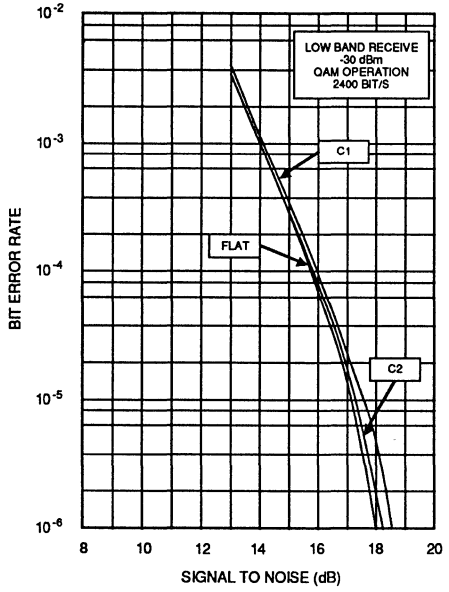
SSI 73K224L BER vs S/N-DPSK LOW



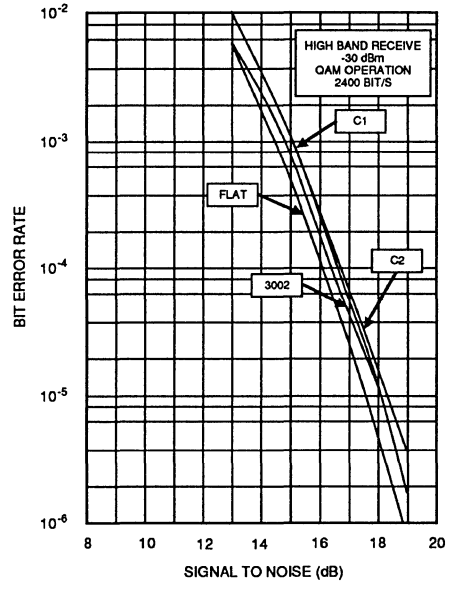
SSI 73K224L BER vs S/N-DPSK HIGH



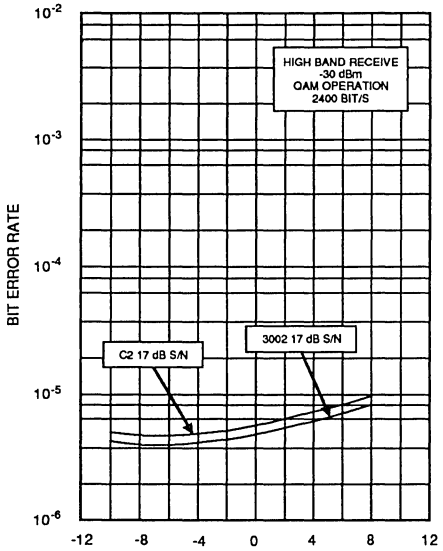
SSI 73K224L BER vs S/N-QAM-LOW



SSI 73K224L BER vs S/N-QAM-HIGH

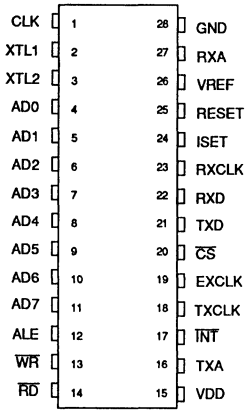


SSI 73K224L BER vs CARRIER OFFSET

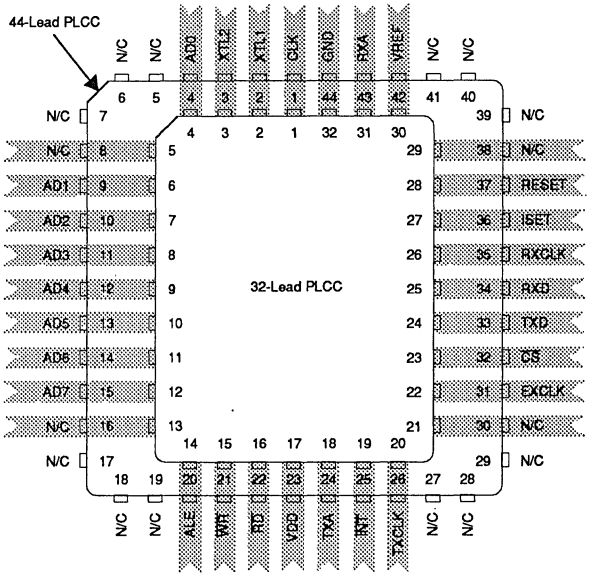


SSI 73K224L
V.22 bis/V.22/V.21, Bell 212A/103
Single-Chip Modem

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



600-Mil
28-Pin DIP



32, 44-Lead PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K224L with Parallel Bus Interface		
28-Pin Plastic Dual-In-Line	SSI 73K224L – CP	73K224L – CP
32-Pin Plastic Leaded Chip Carrier	SSI 73K224L – 32CH	73K224L – 32CH
44-Pin Plastic Leaded Chip Carrier	SSI 73K224L – CH	73K224L – CH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 731-5457

SSI 73K302L
Bell 212A, 103, 202 Single-Chip Modem
Preliminary Data

July, 1990

1

DESCRIPTION

The SSI 73K302L is a highly integrated single-chip modem IC which provides the functions needed to construct a Bell 202, 212A and 103 compatible modem. The SSI 73K302L is an enhancement of the SSI 73K212L single-chip modem with Bell 202 mode features added. The 73K302L is capable of 1200 or 0-300 bit/s full-duplex operation over dial-up lines. 4-wire full-duplex capability and a low speed back channel are also provided in Bell 202 mode. The SSI 73K302L recognizes and generates a 900 Hz soft carrier turn-off tone, and allows 103 for 300 bit/s FSK operation. The SSI 73K302L integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28 or 22–pin DIP configuration. The SSI 73K302L operates from a single +5 volt supply with very low power consumption.

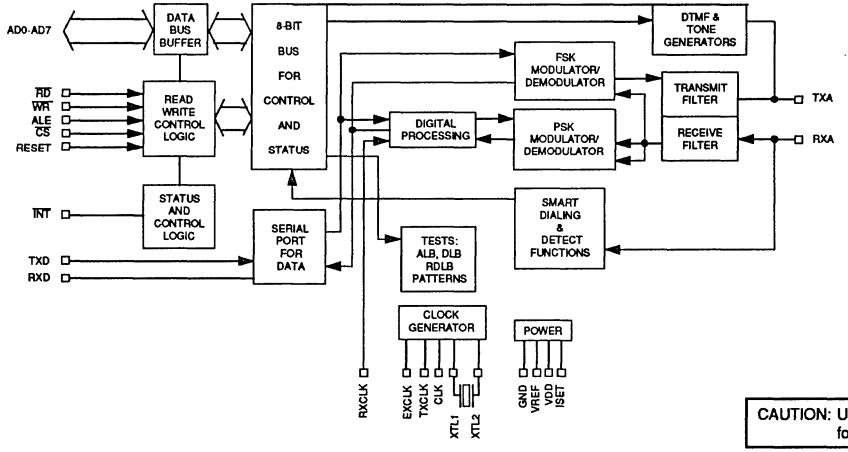
The SSI 73K302L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a tone generator capable of producing DTMF, answer, and 900 Hz soft carrier turn-off tone. This device supports Bell 202, 212A and 103 modes of operation, allowing both

(Continued)

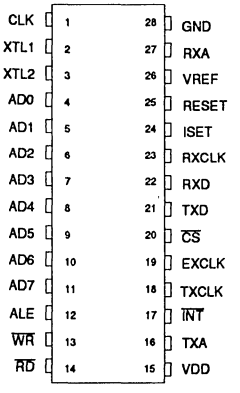
FEATURES

- **One-chip Bell 212A, 103 and 202S/T standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK), 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-150 bit/s back channel**
- **Full-duplex 4-wire operation in Bell 202 mode**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel microprocessor bus (28-pin DIP) for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2225 Hz), soft carrier turn-off (SCT), and FSK mark detectors**
- **DTMF, answer, and SCT tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Space efficient 22 or 28-pin DIP packages**
- **CMOS technology for low power consumption using 35 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

synchronous and asynchronous communications. The SSI 73K302L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K302L is ideal for use in either free standing or integral system modem products where multi-standard data communications is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a modem controller, and RS232 level converter for a typical system.

Tri-mode capability in one-chip allows full-duplex Bell 212 and 103 operation or assymetrical Bell 202S operation over the 2-wire switched telephone network. 202T mode full-duplex operation at 1200 bit/s is also possible when operating on 4-wire leased lines.

A soft carrier turn-off feature facilitates fast line turn around when using the 202S mode for half-duplex applications.

The SSI 73K302L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K302L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 bit/s +1.0%, 2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bit/s ± .01% (± .01% is the required synchronous data rate accuracy).

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The ASYNC/ASYNC converter will reinsert any deleted stop bits and output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The Bell 212A standard defines synchronous operation at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73K302L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using

either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K302L uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. Bell 103 mode uses 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space). Bell 202 mode uses 1200 and 2200 Hz for the main channel and 387 and 487 Hz for the back channel. The modulation rate of the back channel is up to 150 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the 103 or 202 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available in the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K302L control and status registers via a serial command port. In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brough low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 900 Hz soft carrier turn-off tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect lower quality call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

SOFT CARRIER TURN-OFF TONE GENERATOR

The soft carrier turn-off tone generator will output a 900 Hz tone. When activated in Bell 202 main channel transmit mode, the output signal will shift to 900 Hz, maintaining phase continuity during the transition.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with .1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K302L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K302L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K302L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K302L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous DPSK transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In Bell 202 mode a clock which is 16 x 1200 baud data rate is output.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In Bell 202 mode the output is a 16 x 1200 baud clock.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

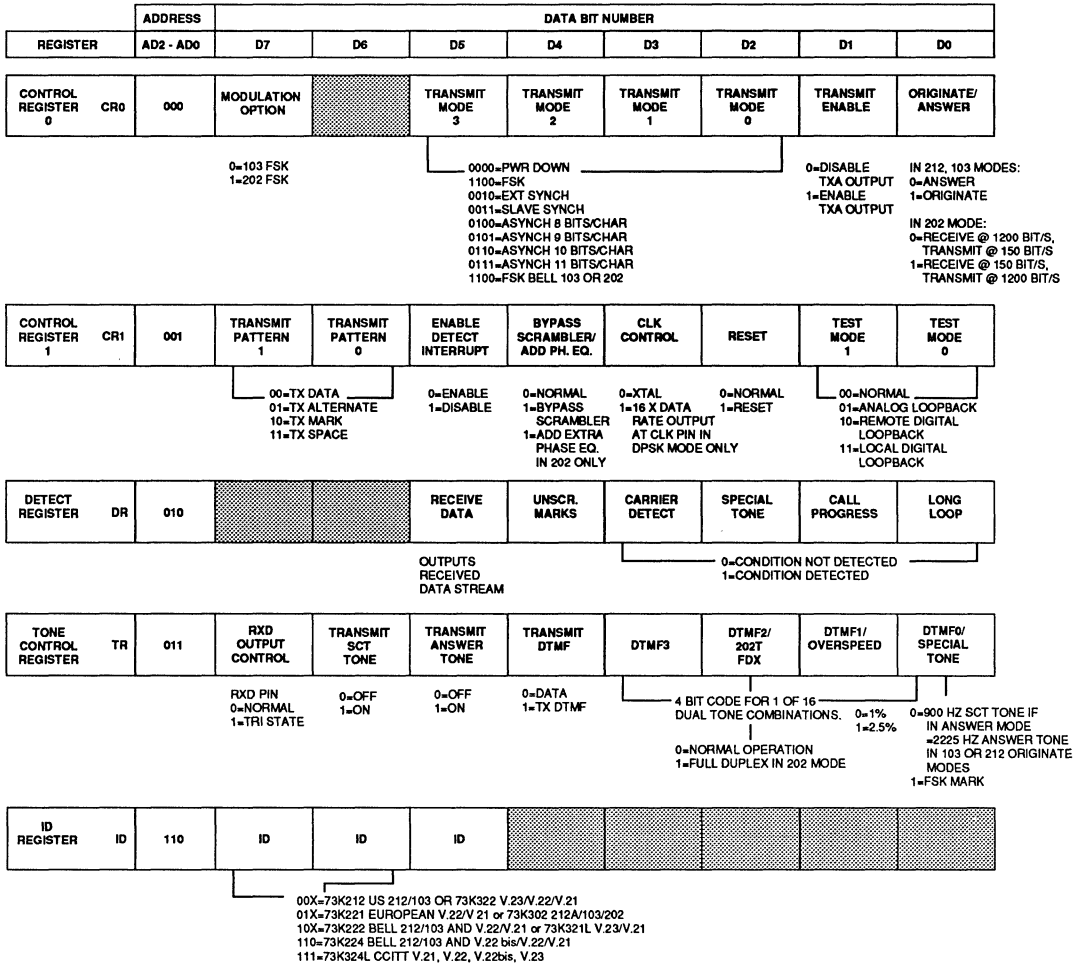
Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K302L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. 202	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF/ 202T FDX	DTMF1/ OVERSPEED	DTMF0/ SPEC. TONE/ ANSWER TONE/ SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	0	1						

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in Bell 202 mode, receive at 1200 bit/s and transmit at 150 bit/s).
		1	Selects originate mode (transmit in low band,receive in high band or in Bell 202 mode, receive at 150 bit/s and transmit at 1200 bit/s).
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects 103 or 202 FSK operation.

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		X 0 X	DPSK asynchronous mode at 1200 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK Bell 202 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low. Not supported in FDX202 mode.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4*	Bypass Scrambler/ Add Phase Equalization	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path. In Bell 202 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

* D4 should always be set to 1 when receiving 1200 bit/s data and to 0 when transmitting 1200 bit/s data in 202 mode.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2225 Hz answer tone if D0 of TR=0 and the device is in Bell 103 or 212A originate mode.
			(2) Soft carrier turn-off tone if D0 of TR=0 and the device is in Bell 202 answer mode.
			(3) an FSK mark in the mode the device is set to receive if D0 of TR is set to 1.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	(DPSK only) Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 202 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Special Tone Detect/Select	D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		0 1 X	Transmit DTMF tones.
		0 0 0	2225 Hz answer tone will be detected in D2 of DR if originate mode is selected in CR0.
			900 Hz SCT tone will be detected in D2 of DR if Bell 202 answer mode is selected in CR0.
		X 0 1	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		1 0 0	2225 Hz answer tone will be generated when in answer mode and transmit enable is selected in CR0.
		1 0 1	2100 Hz answer tone will be generated when in answer mode and transmit enable is selected in CR0.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 bit/s +1.0% -2.5%.
		0 1	Asynchronous DPSK 1200 bit/s +2.3% -2.5%.
D2	DTMF2/202T FDX	0	Enables 202 half-duplex operation if D4=0
		1	Enables 202 full-duplex operation if D4=0
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209
8	1 0 0 0	852 1336
9	1 0 0 1	852 1477
0	1 0 1 0	941 1336

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 202T FDX	DTMF 1/ OVER-SPEED	DTMF 0/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH * 1 0 1 1 941 1209 # 1 1 0 0 941 1477 A 1 1 0 1 697 1633 B 1 1 1 0 770 1633 C 1 1 1 1 852 1633 D 0 0 0 0 941 1633
D4	Transmit DTMF	0	Disable DTMF.
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. To transmit answer tone, the device must be in answer mode.
D6	Transmit SCT Tone	0	Disables SCT tone generator.
		1	Transmit SCT tone in Bell 202 mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

Notes for Tone Register use:

1. To detect SCT tone, 202 answer mode must be selected. To transmit SCT tone, 202 originate mode must be selected.
2. For answer tone detection, 103 or 212 originate mode must be active. To transmit answer tone, the 73K302 must be in 103 or 212 answer mode.
3. After completion of DTMF dialing, bit D2 should be reset unless 202 full-duplex mode is selected.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID					

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212 or 73K322L
		0 1 X	SSI 73K221 or 73K302L
		1 0 X	SSI 73K222 or 73K321L
		1 1 0	SSI 73K224L
		1 1 1	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temp.		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTL1, 2 Load Capacitors	Depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
DPSK Modulator					
Carrier Suppression	Measured at TXA	45			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Soft Carrier Turnoff Tone		-11.9	-10.9	-9.9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
DTMF Generator	Must not be in 202 mode				
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude, Low group	DPSK mode	-10	-9	-8	dBm0
Output Amplitude, High group	DPSK mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	With Sinusoid	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

Note: Parameters expressed in dBm0 refer to the following definition:

5V Version:
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	20		40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time					
Bell 103		8		20	ms
Bell 212A		15		32	ms
Bell 202 Forward Channel		6		12	ms
Bell 202 Back Channel		25		40	ms
Hold Time					
Bell 103		6		20	ms
Bell 212A		10		24	ms
Bell 202 Forward Channel		3		8	ms
Bell 202 Back Channel		10		25	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-49		-42	dBm0
Delay Time					
Answer tone		10		25	ms
900 Hz SCT tone	Preceded by valid carrier*	4		10	ms
202 Main Channel Mark		10		25	ms
202 Back Channel Mark		20		65	ms
1270 or 2225 Hz marks		10		25	ms

* If SCT duration >4ms, it is guaranteed to detect.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors (Continued)					
Hold Time					
Answer tone		4		15	ms
900 Hz SCT tone		1		10	ms
202 Main Channel Mark		3		10	ms
202 Back Channel Mark		10		25	ms
1270 or 2225 Hz marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10			kΩ
				50	pF
Out of Band Energy	Frequency >12 kHz in all modes See Transmit Energy Spectrum			-60	dBm0
Output Impedance	TXA pin		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in 202 main channel		0.1	0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change		40	100	ms
DPSK Recovered Clock					
Capture Range	% of data rate (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms
Tone Generator					
Tone Accuracy	DTMF or FSK tones	-5		+5	Hz
Tone Level	For DTMF, must not be in 202 mode	-1		+1	dB

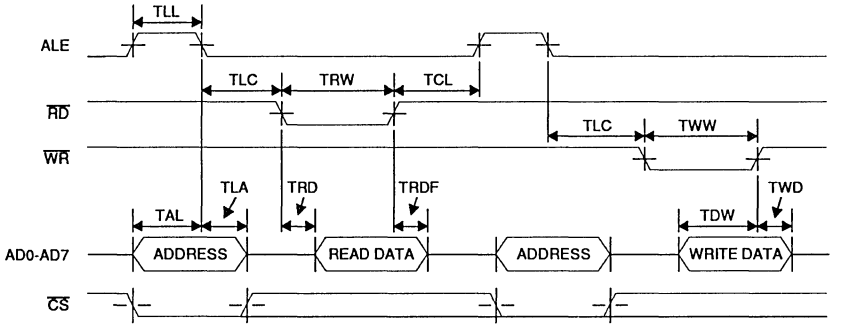
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}/\overline{WR}$ Low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		200	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

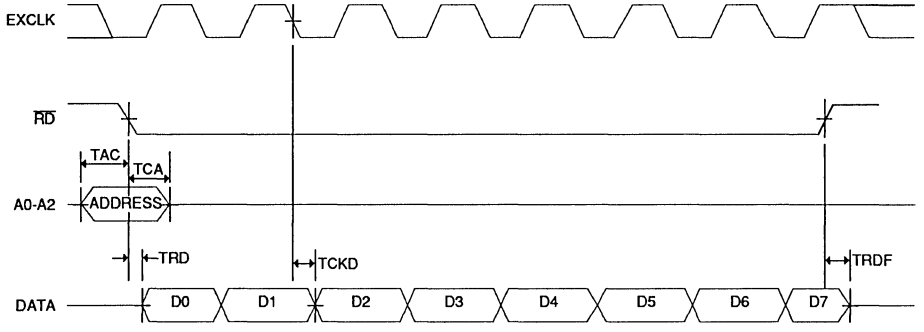
* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

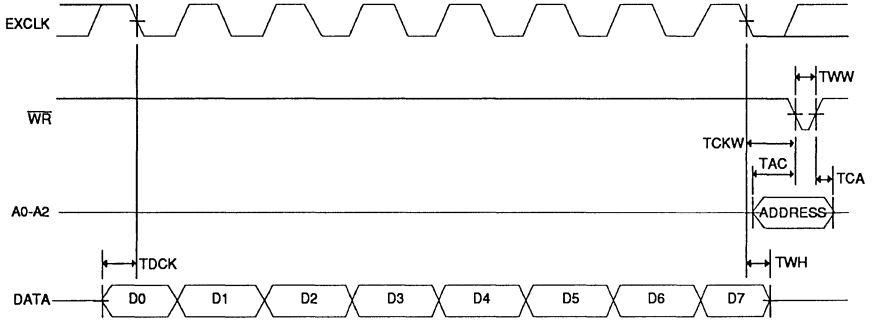
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

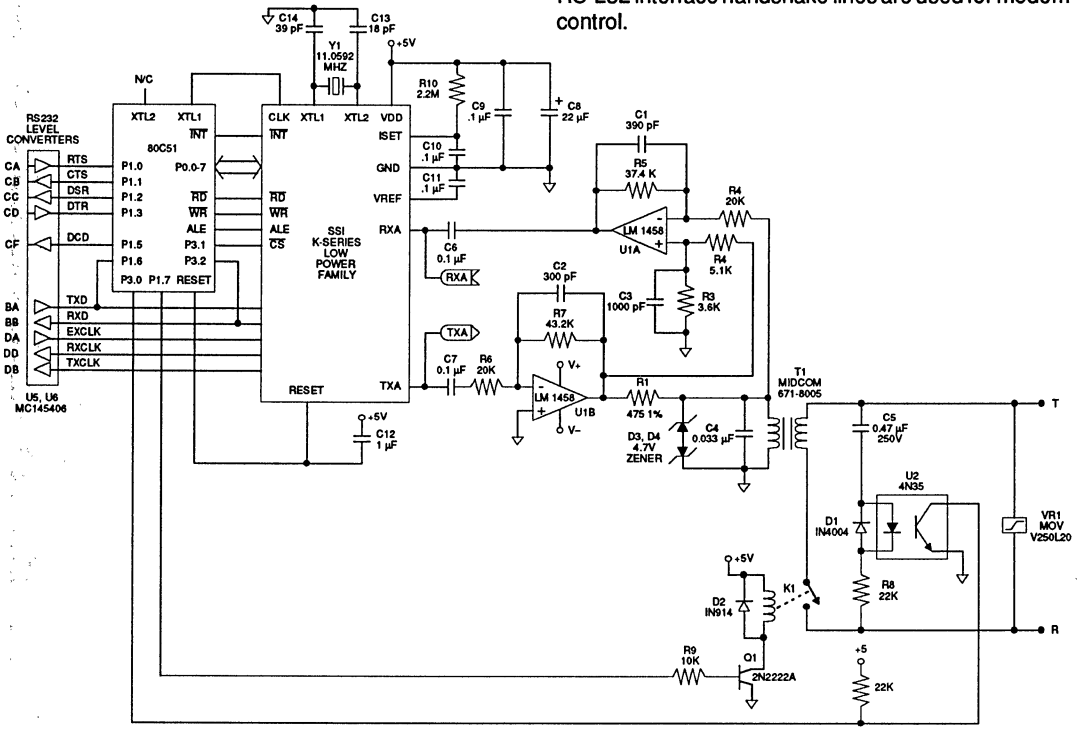


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

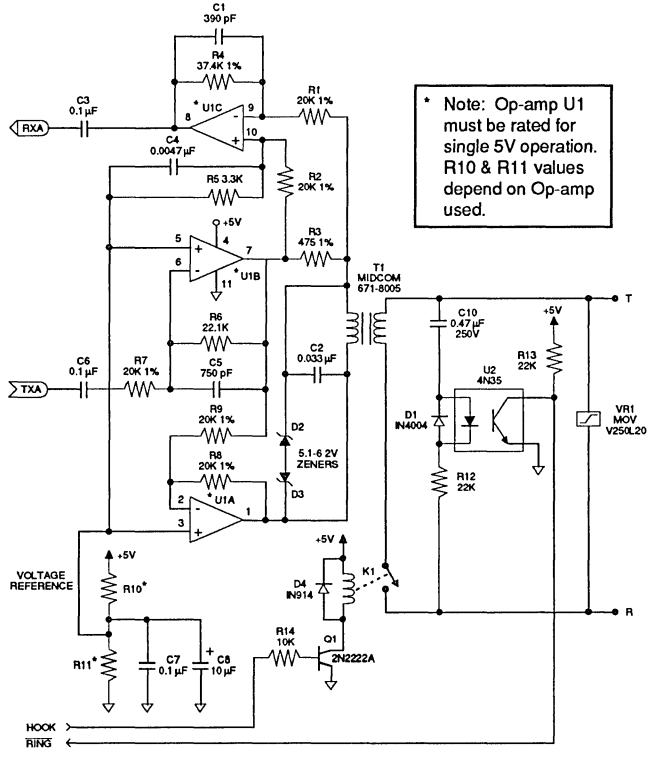


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

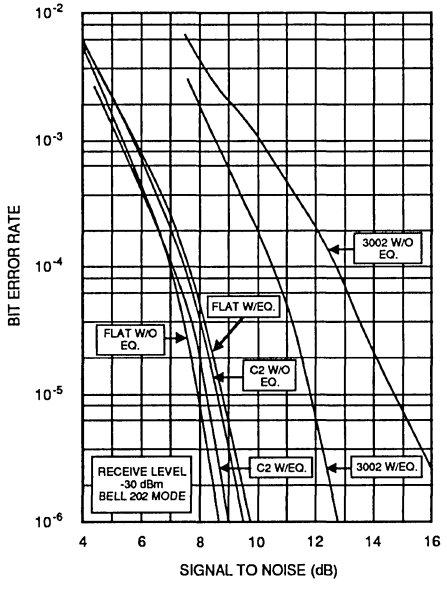
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

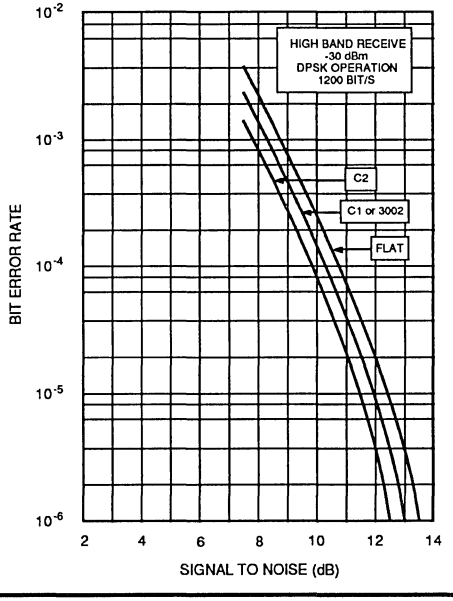
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

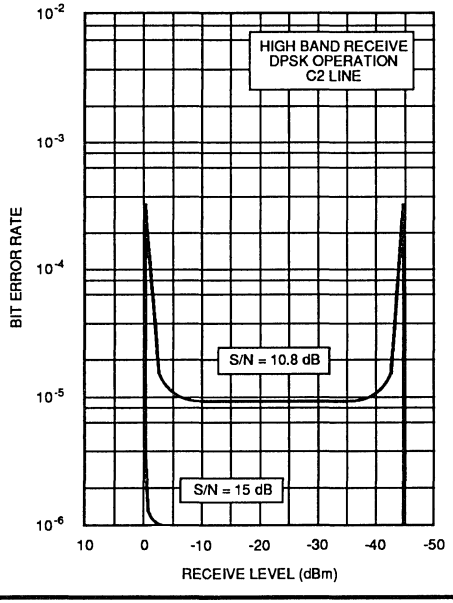
SSI 73K302L
BER vs S/N



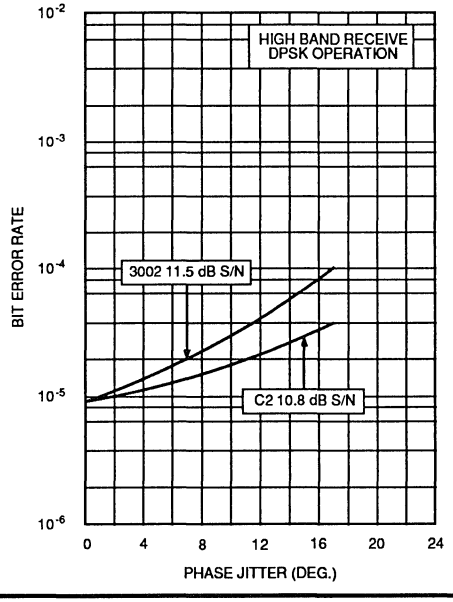
SSI 73K302L
BER vs S/N

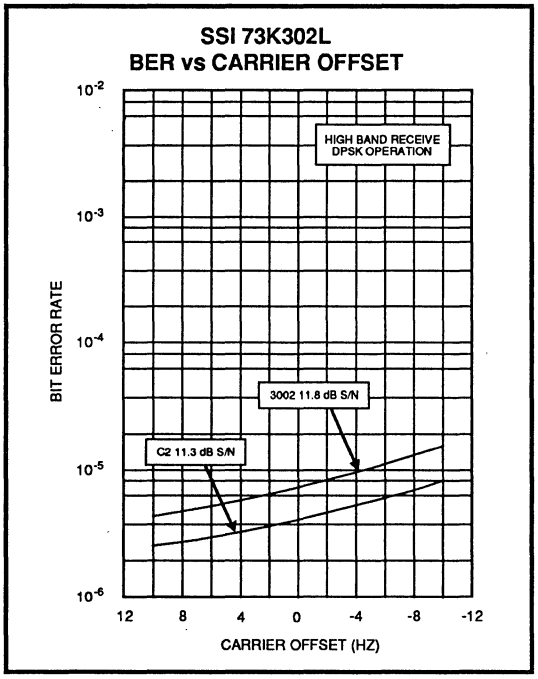


SSI 73K302L
BER vs RECEIVE LEVEL



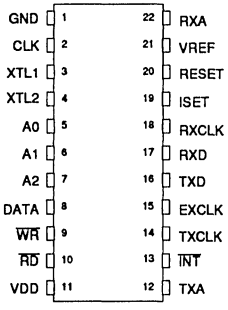
SSI 73K302L
BER vs PHASE JITTER



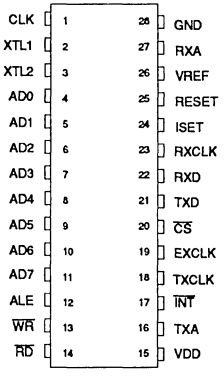

SSI 73K302L
BER vs CARRIER OFFSET
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.8 dB S/N
C2 11.3 dB S/N
BIT ERROR RATE
10-2
10-3
10-4
10-5
10-6
12
8
4
0
-4
-8
-12
CARRIER OFFSET (HZ)

PACKAGE PIN DESIGNATIONS

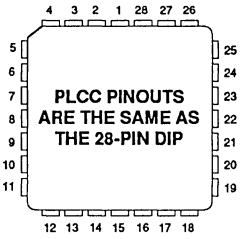
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K302L with Parallel Bus Interface 28-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K302L - IP	73K302L - IP
Plastic Leaded Chip Carrier	SSI 73K302L - IH	73K302L - IH
SSI 73K302L with Serial Interface 22-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K302SL - IP	73K302SL - IP

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 73K321L
CCITT V.23, V.21 Single-Chip Modem

Preliminary Data

July, 1990

1

DESCRIPTION

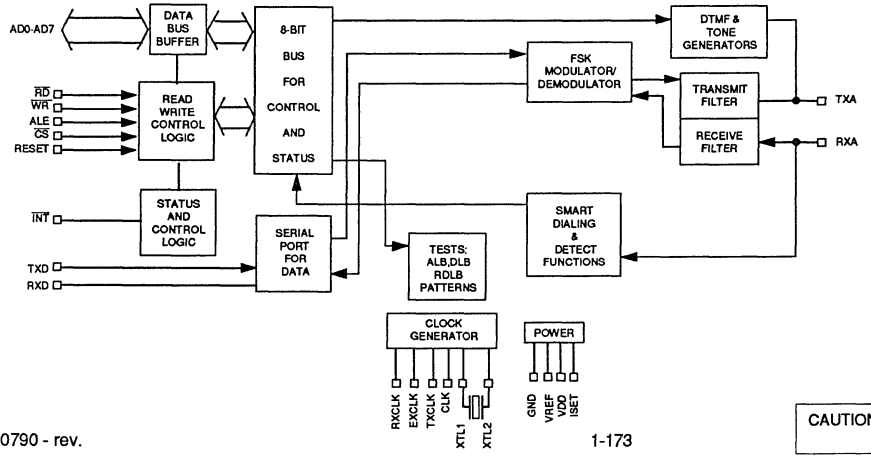
The SSI 73K321L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23 and V.21 compatible modem, capable of 0-300 bit/s full-duplex or 0-1200 bit/s half-duplex operation over dial-up telephone lines. The 73K321L provides 1200 bit/s operation in V.23 mode and 300 bit/s in V.21 mode. The SSI 73K321L also can both detect and generate the 2100 Hz answer tone needed for call initiation. The SSI 73K321L integrates analog, digital, and switched-capacitor array functions on a single substrate,offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K321L operates from a single +5 volt supply with very low power consumption.

The SSI 73K321L includes the FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling tones. The SSI 73K321L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only. (Continued)

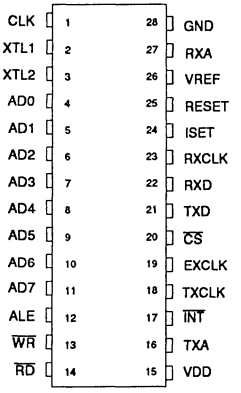
FEATURES

- **One-chip CCITT V.23 and V.21 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (V.21) or 0-1200 bit/s (V.23) forward channel with or without 0–75 bits/s back channel**
- **Full Duplex 0-1200 bit/s (V.23) in 4-wire mode**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel microprocessor bus (28-pin DIP) for control**
- **Serial port for data transfer**
- **Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FS mark detectors**
- **DTMF generator**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **Space efficient 22- or 28-pin DIP packages**
- **CMOS technology for low power consumption using 30 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 73K321L is ideal for either free standing or integral system modem applications where multi-standard data communications over the 2-wire switched telephone network is desired. Typical uses include videotex terminals, low-cost integral modems and built-in diagnostics for office automation or industrial control systems. The 73K321L's high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability in these applications. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K321L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available with the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K321L control and status registers via a serial command port. In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after RD is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone-pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low during the falling edge of ALE on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K321L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal high on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K321L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K321L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K321L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. Used for serial control interface to clock control data in or out of the 73K321L.
RXCLK	23	18	O	Receive Clock. A clock which is 16 x 1200 or 16 x 300 baud data rate is output in either V.23 or V.21, respectively.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. TXCLK is always active. In V.23 or V.21 mode the output is either a 16 x 1200 baud clock or 16 x 300 baud clock, respectively.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In asynchronous modes (1200 or 300 baud) no clocking is necessary.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

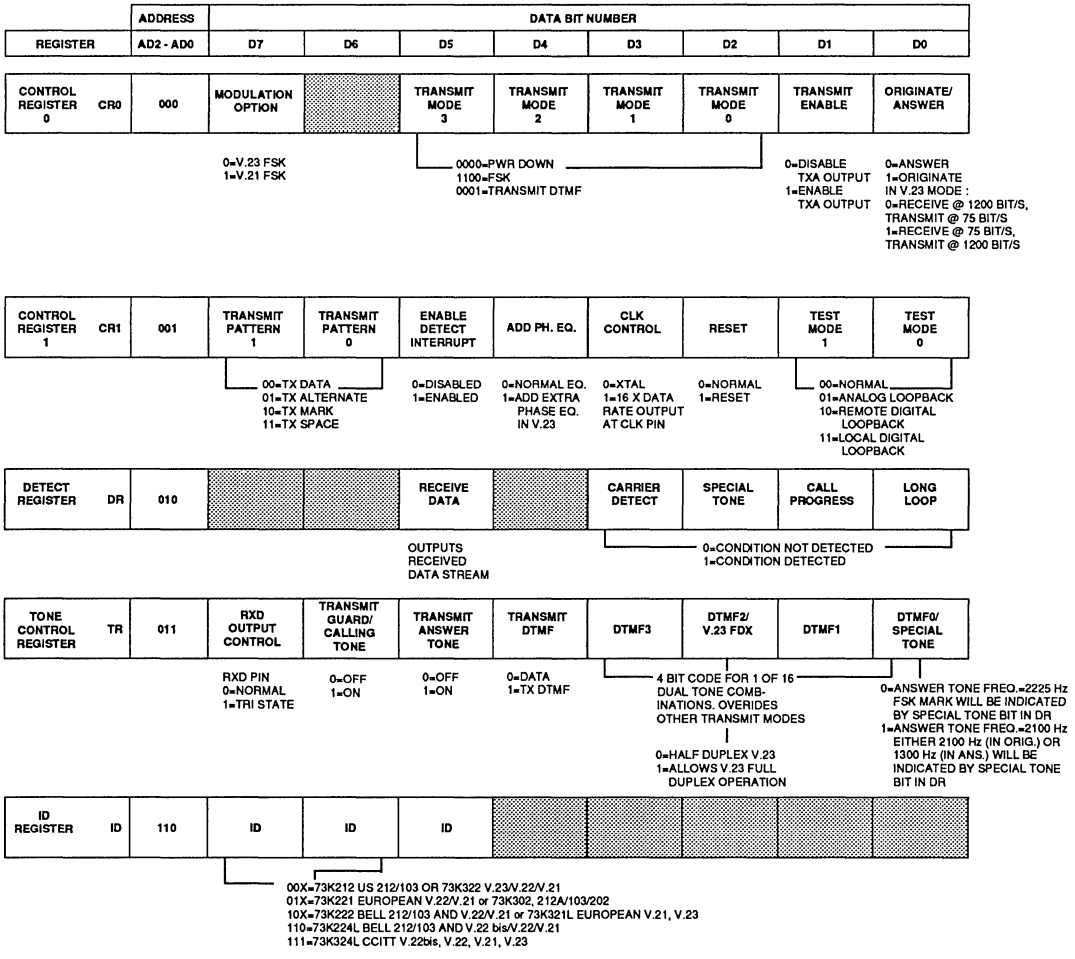
Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K321L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1	DTMF0/ ANSWER/SPEC. TONE SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID					

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2		TX DTMF	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in V.23 mode, receive at 1200 bit/s and transmit at 75 bit/s).
		1	Selects originate mode (transmit in low band,receive in high band or in V.23 mode, receive at 75 bit/s and transmit at 1200 bit/s). If in V.23 and D2 of TR=1, selects V.23 full duplex operation in 4-wire configuration.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 1	Transmit DTMF
D2		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		1 1 0 0	Selects FSK operation.
D6	Unused	0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		0 1 1	FSK CCITT V.23 mode.
		1 1 1	FSK CCITT V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16x the data rate. (16 x 75 or 300 or 1200 Hz.)
D4	Add Ph. Eq.	0	Selects normal equalization.
		1	In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D3. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA		CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21 or V.23 answer mode.
			(3) an FSK mark for the mode the device is set to receive in if D0 of TR = 0.
			NOTE: Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unused		Not used in the 73K321L.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0/ ANS. TONE/ SPECIAL TONE/ SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer Tone/ Special Tone/ Detect/Select	D6 D5 D4 D0	D0 interacts with bits D6, D5, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21 or V.23 answer mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz answer tone in answer mode.
		X 1 0 1	Transmit 2100 Hz answer tone in answer mode.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW	TONES HIGH
1	0 0 0 1	697	1209
2	0 0 1 0	697	1336
3	0 0 1 1	697	1477
4	0 1 0 0	770	1209
5	0 1 0 1	770	1336
6	0 1 1 0	770	1477
7	0 1 1 1	852	1209
8	1 0 0 0	852	1336
9	1 0 0 1	852	1477
0	1 0 1 0	941	1336

TONE REGISTER (Continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (Cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH
			* 1 0 1 1 941 1209
			# 1 1 0 0 941 1477
			A 1 1 0 1 697 1633
			B 1 1 1 0 770 1633
			C 1 1 1 1 852 1633
			D 0 0 0 0 941 1633
D4	Transmit DTMF	0	Disabled DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode.
D6	Transmit Calling Tone	0	Disables calling tone generator.
		1	Transmit calling tone in either mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID					

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212(L) or 73K322L
		0 1 X	SSI 73K221(L) or 73K302L
		1 0 X	SSI 73K222(L) or 73K321L
		1 1 0	SSI 73K224L
		1 1 1	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
NOTE: Parameters expressed in dBm0 refer to the following definition: 0 dB loss in the Transmit path to the line. 2 dB gain in the Receive path from the line. Refer to the Basic Box Modem diagram in the Applications section for the DAA design.					
DTMF Generator					
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude	Low Band, CR0 bit D2=1	-10	-9	-8	dBm0
Output Amplitude	High Band, CR0 bit D2=1	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, as above	1.0	2.0	3.0	dB
Long Loop Detect	Not valid for V.23 back channel	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		43		dB
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	Single Tone	-48		-43	dBm0
Delay Time					
V.21		10		20	ms
V.23 Forward Channel		6		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		6		20	ms
V.23 Forward Channel		3		8	ms
V.23 Back Channel		10		25	ms
Hysteresis		2			dB

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step				
2100 Hz answer tone		10		25	ms
1300 Hz calling tone		10		25	ms
390 Hz V.23 back channel mark		20		65	ms
980 or 1650 Hz V.21 marks		10		25	ms
Hold Time	-30 dBm0 to -70 dBm0 Step				
2100 Hz answer tone		4		15	ms
1300 Hz calling tone		3		10	ms
390 Hz V.23 back channel mark		10		25	ms
980 or 1650 Hz V.21 marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in .3 to 3.4 kHz	10		 50	kΩ pF
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin, TXA Enabled		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in V.23 main channel		0.1	0.4	mVrms

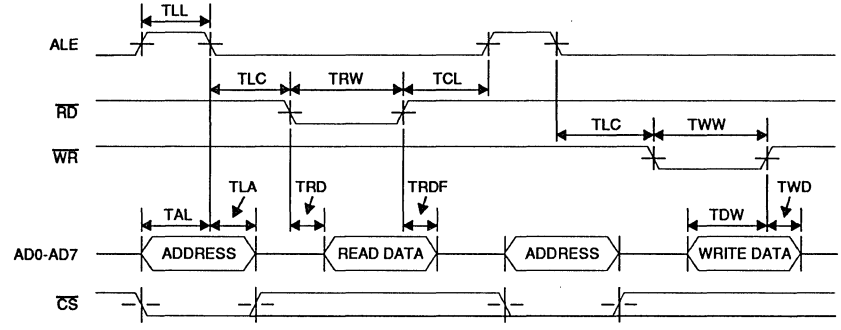
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}/\overline{WR}$ Low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		200	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

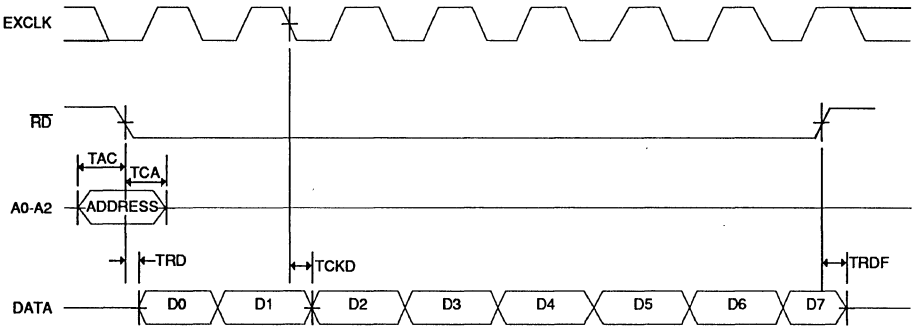
* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

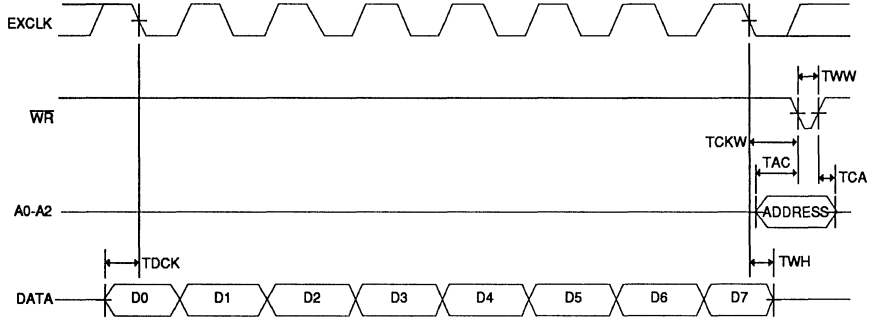
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

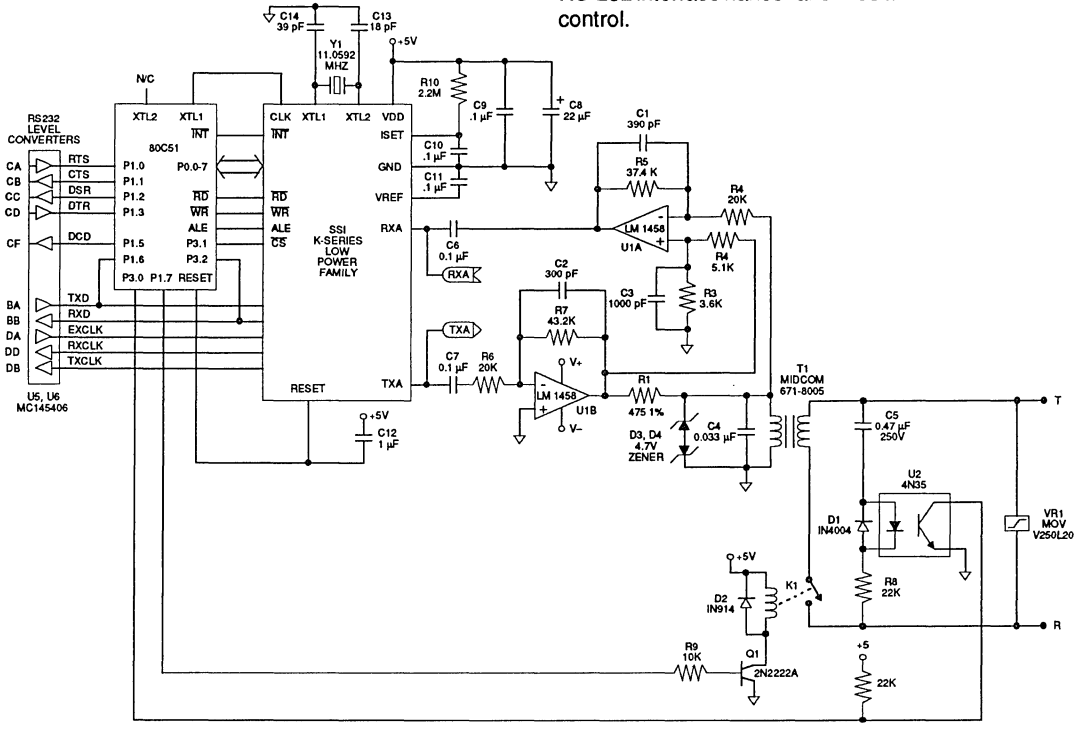


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

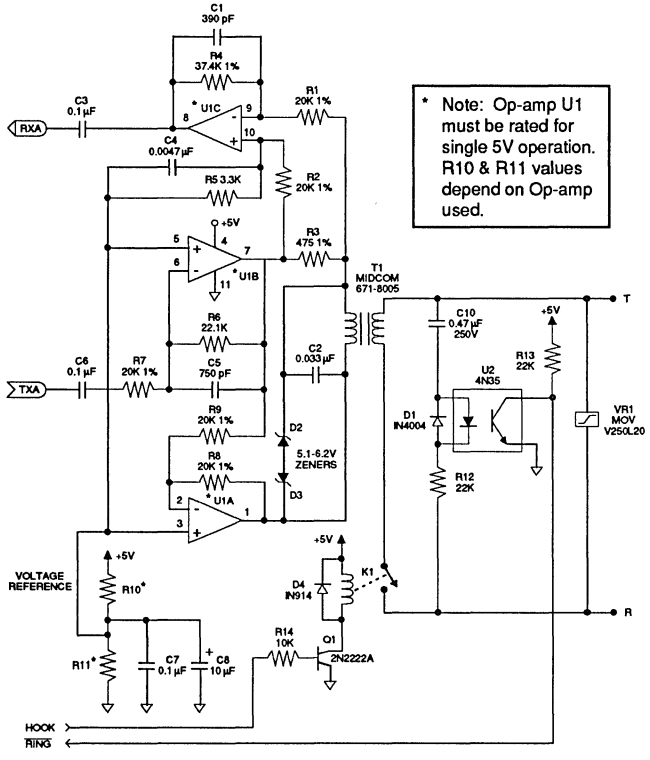


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

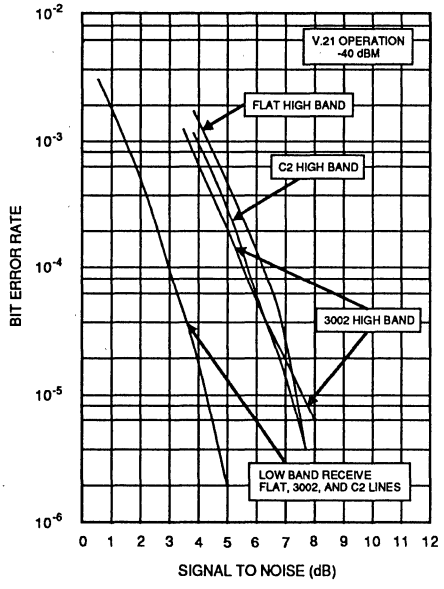
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

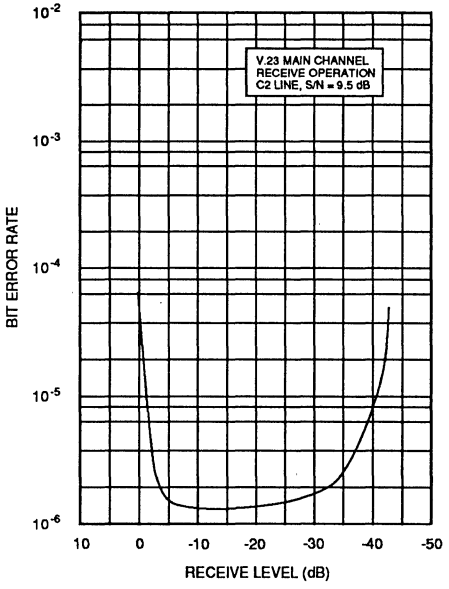
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

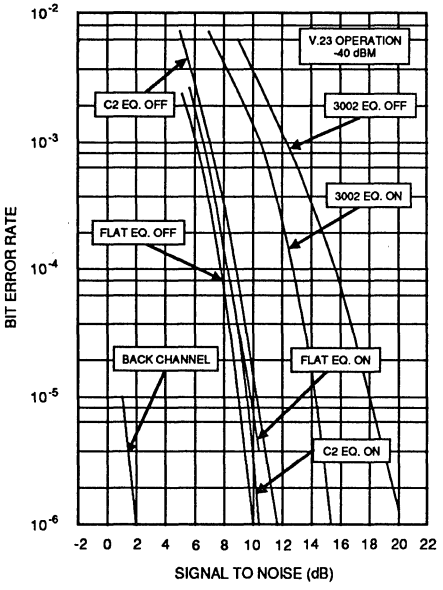
SSI 73K321L
BER vs SIGNAL TO NOISE



***SSI 73K321L**
BER vs RECEIVE LEVEL (V.23)



***SSI 73K321L**
BER vs S/N (V.23 ONLY)**

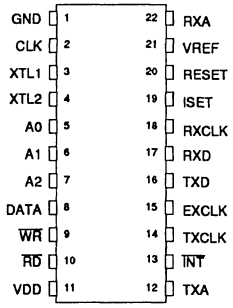


* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

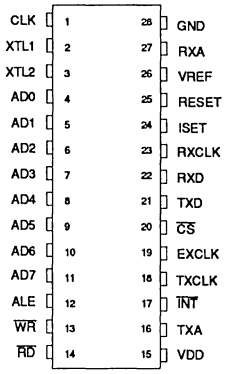
** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

PACKAGE PIN DESIGNATIONS

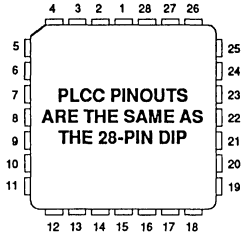
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K321L with Parallel Bus Interface		
28-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K321L - IP	73K321L - IP
Plastic Leaded Chip Carrier	SSI 73K321L - IH	73K321L - IH
SSI 73K321L with Serial Interface		
22-Pin 5 Volt Supply	SSI 73K321SL - IP	73K321SL - IP
Plastic Dual-In-Line	SSI 73K321SL - IC	73K321SL - IC

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 73K322L
CCITT V.23, V.22, V.21 Single-Chip Modem

1

July, 1990

DESCRIPTION

The SSI 73K322L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23, V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation or 0-1200 bit/s half-duplex operation with or without the back channel over dial-up lines. The SSI 73K322L is an enhancement of the SSI 73K221L single-chip modem with performance characteristics suitable for European and Asian telephone systems. The SSI 73K322L produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and supports V.21 for 300 Hz FSK operation. It also operates in V.23, 1200 bit/s FSK mode. The SSI 73K322L integrates analog, digital, and switched-capacitor array functions on a single substrate,offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K322L operates from a single +5 volt supply with very low power consumption.

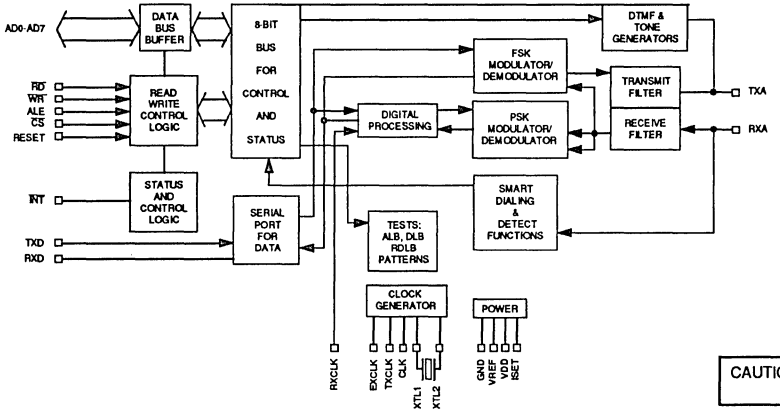
The SSI 73K322L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling and 550 or 1800 Hz guard tone. This device supports V.23, V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and

(Continued)

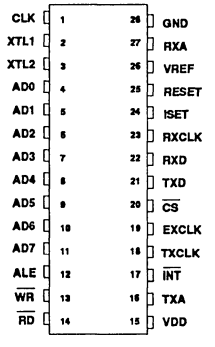
FEATURES

- One-chip CCITT V.23, V.22 and V.21 standard compatible modem data pump
- Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-75 bit/s back channel
- Interfaces directly with standard microprocessors (8048, 80C51 typical)
- Serial (22-pin DIP) or parallel microprocessor bus (28-pin DIP) for control
- Serial port for data transfer
- Both synchronous and asynchronous modes of operation
- Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FSK mark detectors
- DTMF and 550 or 1800 Hz guard tone generators
- Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns
- Precise automatic gain control allows 45 dB dynamic range
- Space efficient 22- or 28-pin DIP packages
- CMOS technology for low power consumption using 30 mW @ 5V from a single power supply

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

asynchronous communications. The SSI 73K322L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K322L is ideal for use in either free standing or integral system modem products where multi-standard data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K322L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K322L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± .01% (± .01% is the crystal tolerance).

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The ASYNC/ASYNC converter will reinsert any deleted stop bits and output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73K322L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K322L uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the V.21 or V.23 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K322L control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with .1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K322L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K322L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous DPSK transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.

RS-232 INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x1200 or 16 x 300 Hz baud data rate is output, respectively.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200 or 16 x 300 Hz baud clock, respectively.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

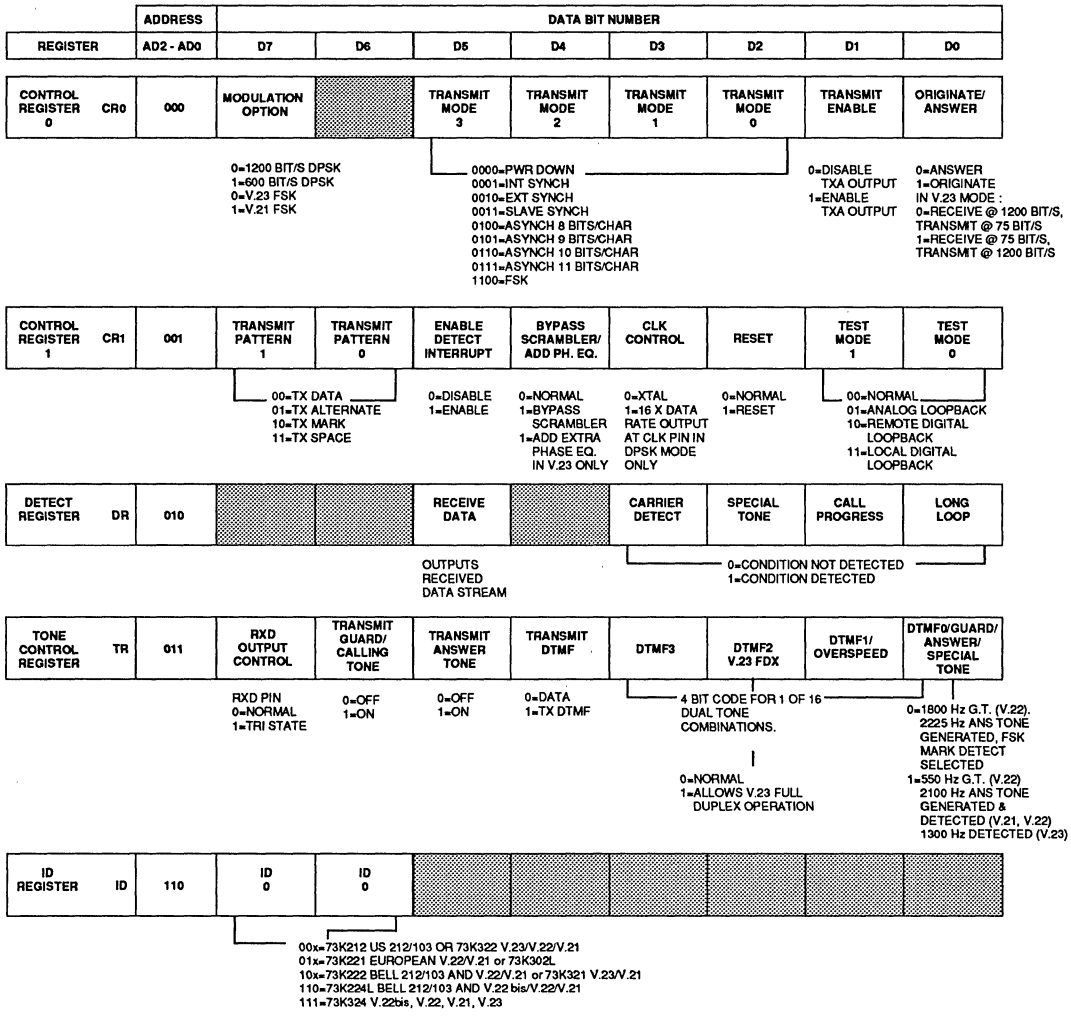
Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K322L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/SPEC. TONE SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID					

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s).
		1	Selects originate mode (transmit in low band,receive in high band or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s).
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	PSK asynchronous mode at 1200 bit/s.
		1 0 X	PSK asynchronous mode at 600 bit/s.
		0 1 1	FSK CCITT V.23 mode.
		1 1 1	FSK CCITT V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4	Bypass Scrambler/ Add Phase Equalization	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path. In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect	0	Disables interrupt at $\overline{INT}$ pin.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 or V.22 originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21, or V.22 answer mode.
			(3) an FSK mark in the mode the device is set to receive.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ SP. TONE/ SELECT

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0	D6 D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
	Guard Tone/ Answer Tone	1 X 0 0	Select 1800 Hz guard tone if in V.22 and answer mode in CR0.
	Special Tone/ Detect/Select	1 X 0 1	Select 550 Hz guard tone if in V.22 and answer mode in CR0.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 or V.22 originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21, or V.22 answer mode is selected in CR0.
		X 0 0 0	Transmit 2225 Hz Answer Tone
		X 1 0 1	Transmit 2100 Hz Answer Tone
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 or 600 bit/s +1.0% -2.5%.
		0 1	Asynchronous DPSK 1200 or 600 bit/s +2.3% -2.5%.
D2	DTMF 2/ V.23 FDX	0	Half-duplex asymetric operation in V.23 mode.
		1	Full-duplex (4-wire) operation in V.23 mode.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0 (Cont.)			KEYBOARD EQUIVALENT / DTMF CODE D3 D2 D1 D0 / TONES LOW HIGH
			8 — 1 0 0 0 — 852 1336
			9 — 1 0 0 1 — 852 1477
			0 — 1 0 1 0 — 941 1336
			* — 1 0 1 1 — 941 1209
			# — 1 1 0 0 — 941 1477
			A — 1 1 0 1 — 697 1633
			B — 1 1 1 0 — 770 1633
			C — 1 1 1 1 — 852 1633
			D — 0 0 0 0 — 941 1633
D4	Transmit DTMF	0	Disable DTMF.
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode. To transmit answer tone, the device must be in DPSK answer mode.
D6	TX Guard or Calling Tone	0	Disables guard/calling tone generator.
		1	Transmit guard tone if in V.22 and answering; otherwise transmit calling tone, in any other mode including V.23 mode.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID					

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212(L) or 73K322L
		0 1 X	SSI 73K221(L) or 73K302L
		1 0 X	SSI 73K222(L) or 73K321L
		1 1 0	SSI 73K224L
		1 1 1	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temp.		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal characteristics	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
DPSK Modulator					
Carrier Suppression	Measured at TXA	45			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
DTMF Generator					
Freq. Accuracy	Must be in V.22 mode	-.25		+.25	%
Output Amplitude	Low Band, V.22 mode	-10	-9	-8	dBm0
Output Amplitude	High Band, V.22 mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, V.22 mode	1.0	2.0	3.0	dB
Long Loop Detect	With Sinusoid	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

Note: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-48		-43	dBm0
Delay Time					
V.21		10		20	ms
V.22		15		32	ms
V.23 Forward Channel		6		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		6		20	ms
V.22		10		24	ms
V.23 Forward Channel		3		8	ms
V.23 Back Channel		10		25	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time					
2100 Hz answer tone		10		25	ms
1300 Hz calling tone		10		25	ms
390 Hz V.23 back channel mark		20		65	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors (Continued)					
980 or 1650 Hz V.21 marks		10		25	ms
Hold Time					
2100 Hz answer tone		4		15	ms
1300 Hz calling tone		3		10	ms
390 Hz V.23 back channel mark		10		25	ms
980 or 1650 Hz V.21 marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10		 50	kΩ pF
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin, TXA enabled		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in V.23 main channel		0.1	0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

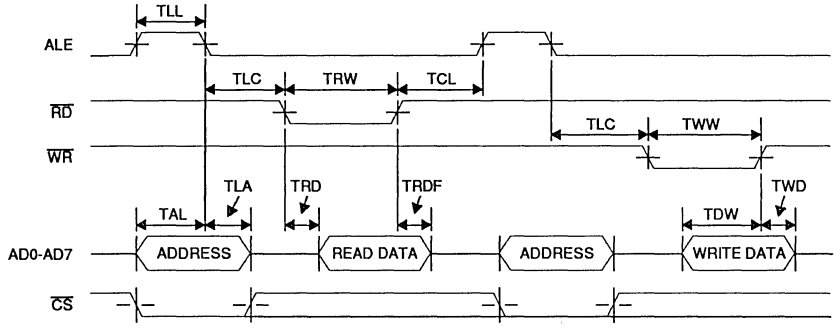
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion 700 to 2900 Hz	550 Hz			-50	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}/\overline{WR}$ Low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		200	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

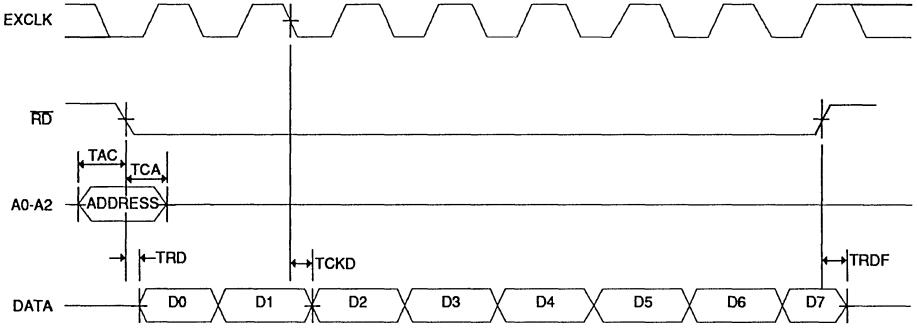
* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

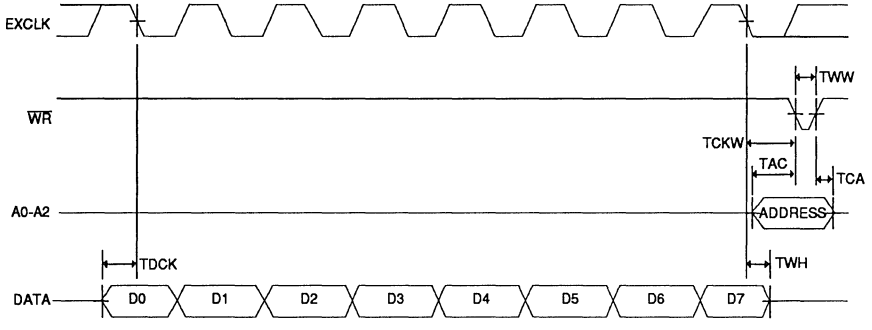
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

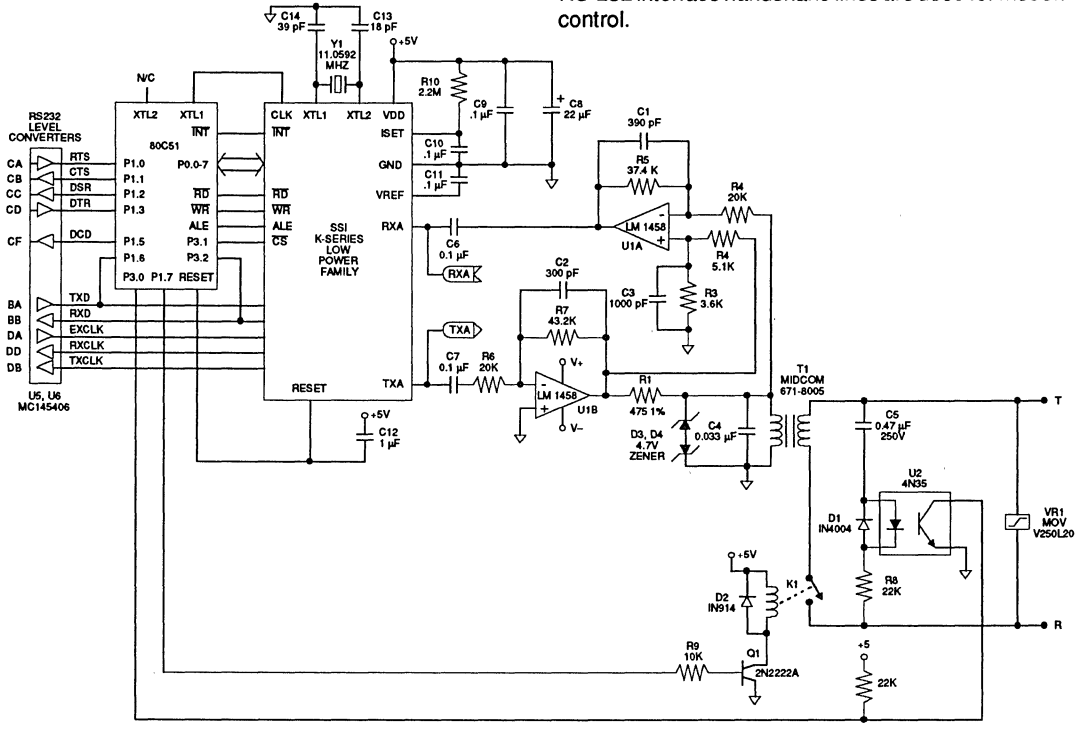


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

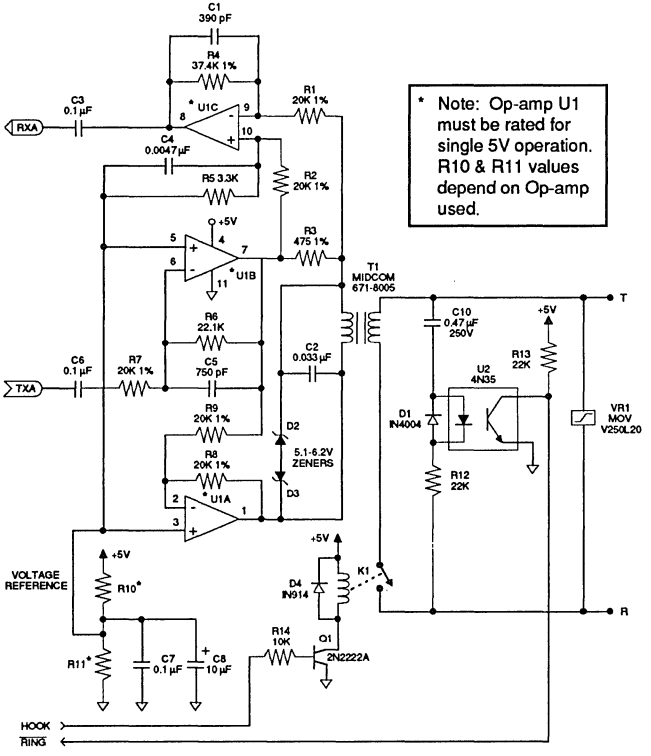


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

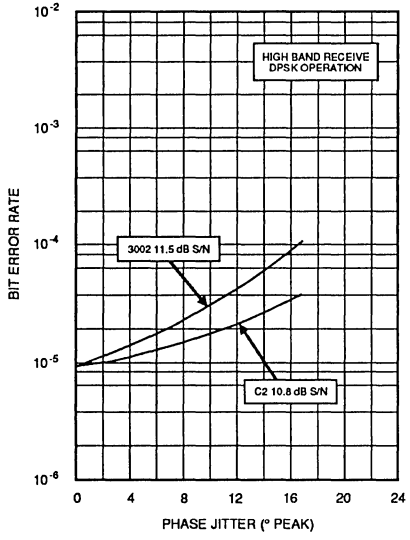
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

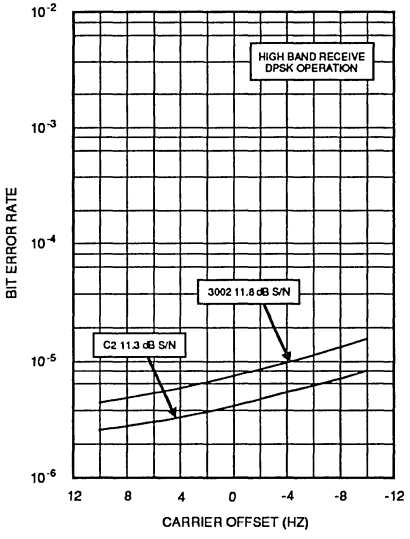
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

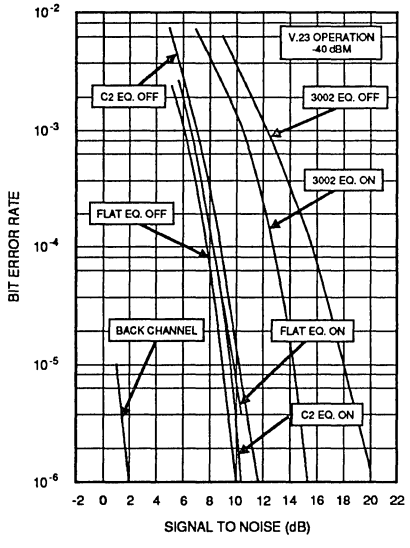
*SSI 73K322L
BER vs PHASE JITTER



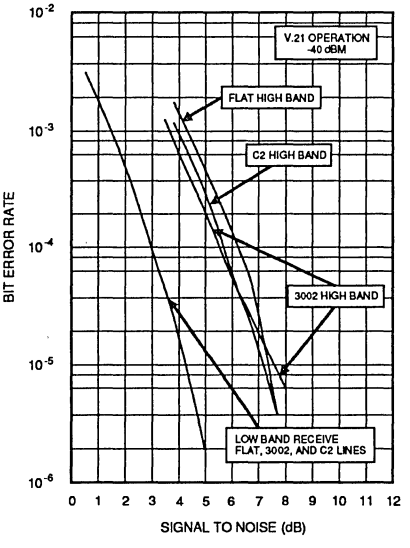
SSI 73K322L
BER vs CARRIER OFFSET



*SSI 73K322L
BER vs S/N (V.23 ONLY)**



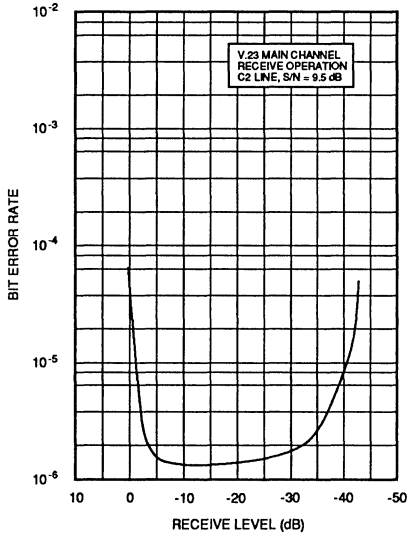
SSI 73K322L
BER vs SIGNAL TO NOISE



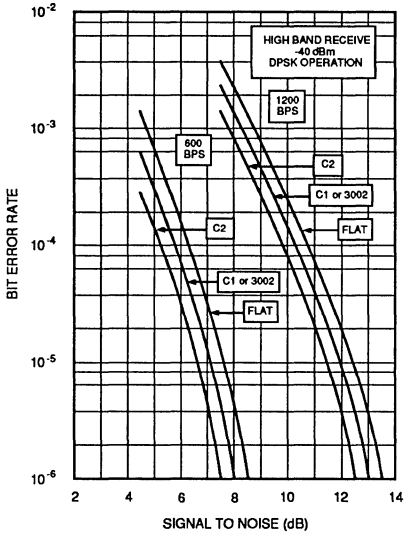
* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

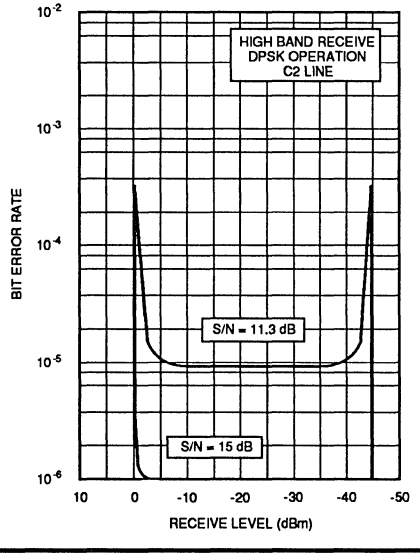
*SSI 73K322
BER vs RECEVE LEVEL (V.23)



*SSI 73K322L
BER vs SIGNAL TO NOISE



*SSI 73K322
BER vs RECEVE LEVEL



* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

SSI 73K322L
CCITT V.23, V.22, V.21
Single-Chip Modem

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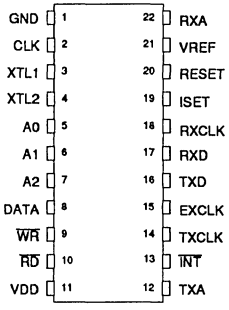
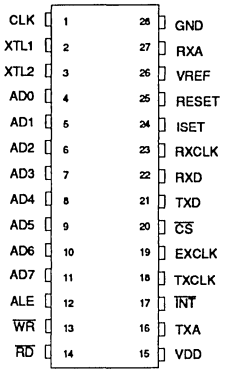
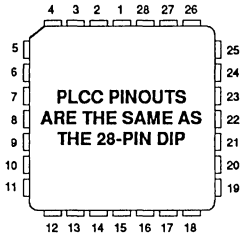
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Lead
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K322L with Parallel Bus Interface		
28-Pin 5 Volt Supply		
Plastic Dual-In-Line	SSI 73K322L - IP	73K322L - IP
Plastic Leaded Chip Carrier	SSI 73K322L - IH	73K322L - IH
SSI 73K322L with Serial Interface		
22-Pin 5 Volt Supply	SSI 73K322SL - IP	73K322SL - IP
Plastic Dual-In-Line	SSI 73K322SL - IC	73K322SL - IC

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 73K324L
CCITT V.22bis, V.22, V.21, V.23 Single-Chip Modem

Advance Information

July, 1990

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DESCRIPTION

The SSI 73K324L is a highly integrated single-chip modem IC which provides the functions needed to design a quad-mode CCITT compatible modem capable of operation over dial-up lines. The SSI 73K324L adds V.23 capability to the CCITT modes of SSI's 73K224 one-chip modem, allowing a one-chip implementation in designs intended for European markets which require this added modulation mode. The SSI 73K324L offers excellent performance and a high level of functional integration in a single 28-pin DIP. The device supports V.22bis, V.22, V.21, and V.23 operating modes, allowing both synchronous and asynchronous operation as defined by the appropriate standard.

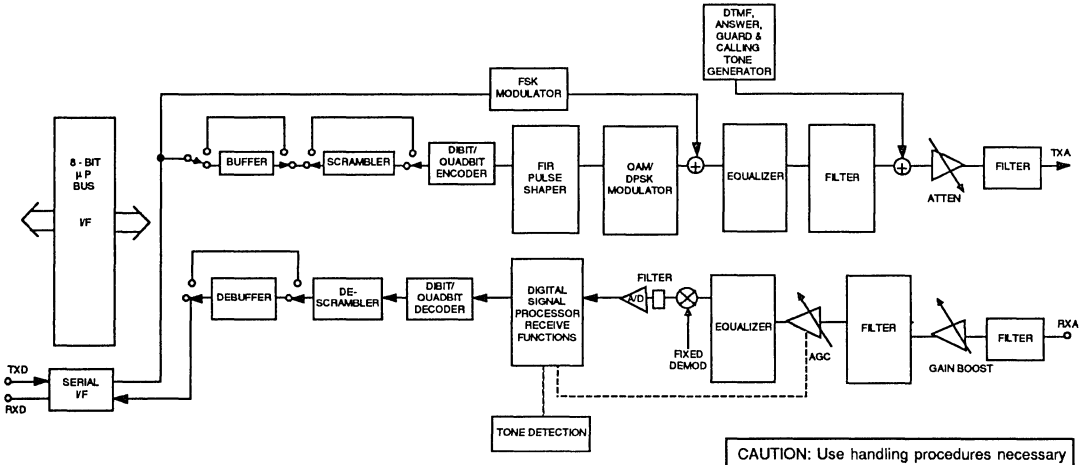
The SSI 73K324L is designed to appear to the Systems Engineer as a microprocessor peripheral, and will easily interface with popular one-chip microcontrollers (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus. An optional serial control bus is also available for applications not requiring a parallel interface. Data communications occurs through a separate serial port.

(Continued)

FEATURES

- **One-chip multi-mode CCITT V.22bis, V.22, V.21, V.23 compatible modem data pump**
- **FSK (75, 300/1200 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Pin and software compatible with other SSI K-Series family one-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Selectable asynch/synch with internal buffer/debuffer and scrambler/descrambler functions**
- **All synchronous (internal, external, slave) and asynchronous operating modes**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (15 dB, 1 dB steps), and selectable receive boost (+12 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, SCT (900 Hz) calling tone (1300 Hz) and signal quality monitors**
- **DTMF, answer, calling, SCT and guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space and Alternating bit patterns**
- **CMOS technology for low power consumption**
- **4-wire full duplex operation in all modes**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 73K324L offers full hardware and software compatibility with other products in Silicon Systems' K-Series family of single-chip modems, allowing system upgrades with a single component change. The SSI 73K324L is ideal for use in free-standing or integral system modem products where full-duplex 2400 bit/s operation with alternate mode capability is required. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converters for a typical system.

The SSI 73K324L is designed to provide a complete V.22bis, V.22, V.21, and V.23 compatible modem on a chip. Many functions were included to simplify implementation in typical modem designs. In addition to the basic 2400 bit/s QAM, 1200/600 bit/s DPSK and 1200/300/75 bit/s FSK modulator/demodulator sections, the device also includes synch/asynch buffering, DTMF, guard, and calling tone generator capabilities. Handshake pattern detectors simplify control of connect sequences, and precise tone detectors allow accurate detection of call progress, answer back, and calling tones. All operating modes defined by the incorporated standards are included, and test modes are provided for simplified diagnostics. Most functions are selectable as options, and logical defaults are provided when override modes are activated. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus for control and status monitoring. Data communications takes place through a separate serial port. Data may also be sent and received through the control registers. This simplifies designs requiring speed buffering, error control and compression.

FUNCTIONAL DESCRIPTION

QAM MODULATOR/DEMODULATOR

The SSI 73K324L encodes incoming data into quadbits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K324L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K324L use a phase locked loop coherent demodulation technique that offers excellent performance. Adaptive equalization is also used in DPSK modes for optimium operation with varying lines.

FSK MODULATOR/DEMODULATOR

The FSK modulator/demodulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 frequencies of 980 and 1180 Hz (originate mark and space), or 1650 and 1850 Hz (answer mark and space) are used in V.21 mode. V. 23 mode uses 1300 and 2100 Hz for the main channel or 390 and 450 Hz for the back channel. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and to provide compromise delay equalization as well as rejection of out-of-band signals. The transmit signal filtering corresponds to a $\sqrt{75\%}$ raised cosine frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communciation with asynchronous terminals which may transfer data at 600, 1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01%. When transmitting in this mode the serial data on the TxD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where di-bit or quad-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking, FSK, and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be recognized in accordance with the appropriate standard and passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter has an extended overspeed mode which allows selection of an output speed range of either +1% or +2.3%. In the extended overspeed mode, some stop bits are output at 7/8 the normal width.

Similar to the transmit side, both the SYNC/ASYNC rate converter and the data descrambler are bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

PARALLEL BUS INTERFACE

Seven 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Five contol registers are read/write. The status detect and ID register are read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K324 control and status registers via a serial command port. In this mode the A0, A1, and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected addresss location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consectuive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

TONE GENERATOR

The tone generator will output one of 16 standard dual tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Guard, answer, SCT and calling tones are also provided by this section.

FULL DUPLEX OPERATION

Four wire full duplex operation is allowed in all modes. This feature allows transmission and reception in the same band for four wire applications only.

PIN DESCRIPTION

POWER

NAME	28-PIN	32-PIN	TYPE	DESCRIPTION
GND	28	32	I	System Ground.
VDD	15	17	I	Power supply input, 5V ±10%. Bypass with .1 and 22 µF capacitors to GND.
VREF	26	30	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	27	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

NAME	28-PIN	32-PIN	TYPE	DESCRIPTION
ALE	12	14	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	4, 6-12	I/O	Address/data bus. These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{CS}$	20	23	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	1	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	19	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	16	I	Read. A low requests a read of the SSI 73K324L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	28	I	Reset. An active signal high on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{WR}$	13	15	I	Write. A low on this informs the SSI 73K324L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are low.
Note:	The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.			

RS-232 INTERFACE

NAME	28-PIN	32-PIN	TYPE	DESCRIPTION
EXCLK	19	22	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	26	O	Receive Clock Tristate. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x 1200/75 or 16 x 300 Hz data rate is output, respectively.
RXD	22	25	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	20	O	Transmit ClockTristate. This signal is used in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200/75 or 16 x 300 Hz clock, respectively.
TXD	21	24	I	Transmit Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (2400/1200/600 bit/s or 300 baud) no clocking is necessary. DPSK/QAM data must be +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE

RXA	27	32	I	Received modulated analog signal input from the phone line.
TXA	16	18	O	Transmit analog output to the phone line.
XTL1 XTL2	2 3	2 3	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

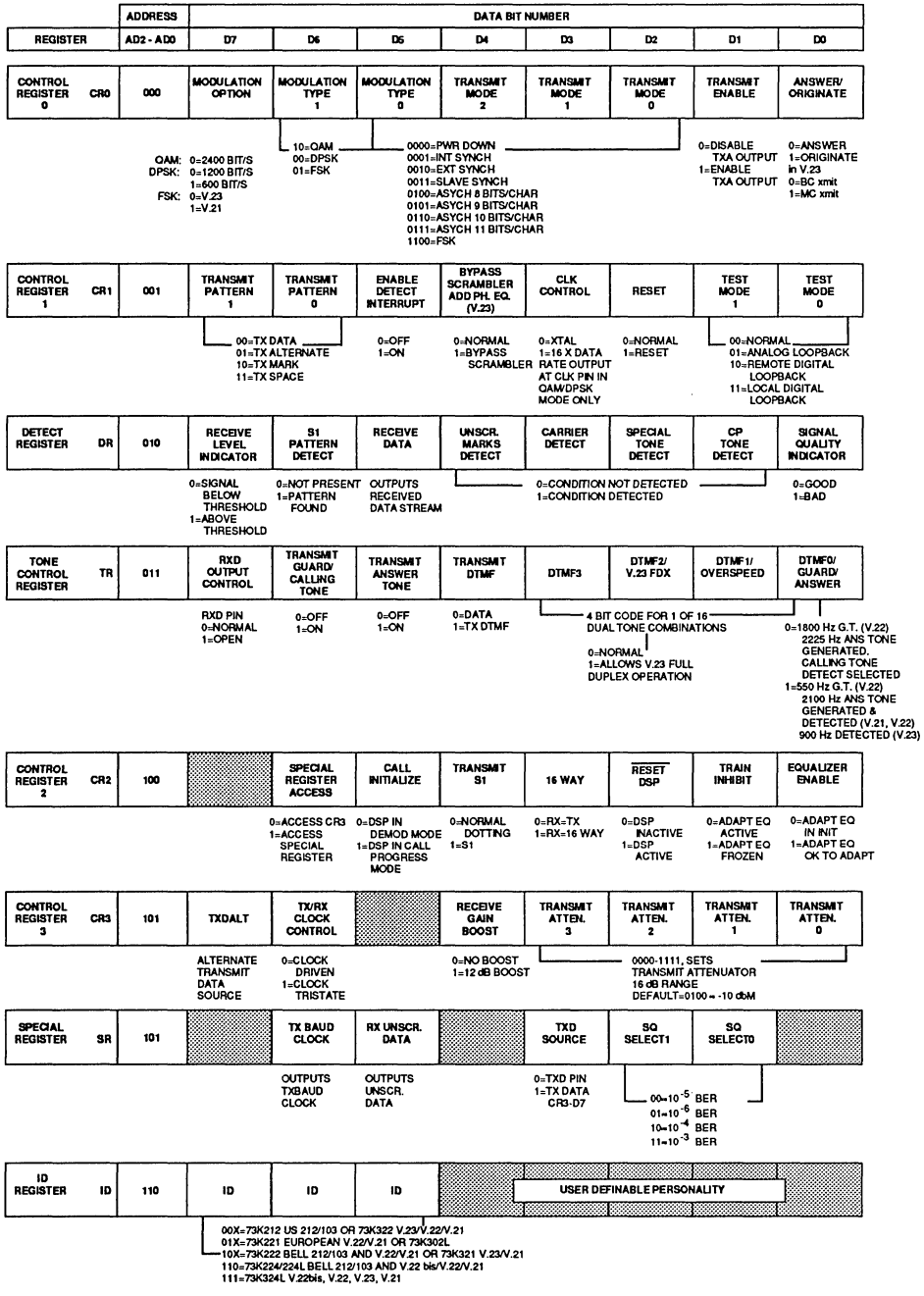
Seven 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K324L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 4 WIRE FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/ CALLING/SCT
CONTROL REGISTER 2 CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3 CR3	101	TXDALT	TX/RX CLOCK CONTROL	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
SPECIAL REGISTER SR	101		TX BAUD CLOCK	RX UNSCR. DATA		TXD SOURCE	SQ SELECT 1	SQ SELECT 0	
ID REGISTER ID	110	1	1	1	USER DEFINABLE PERSONALITY				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE



CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s.)
		1	Selects originate mode (transmit in low band, receive in high band or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s.)
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone, DTMF, or Carrier.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.

CONTROL REGISTER 0 (Continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK
D7	Modulation Option	0	QAM selects 2400 bit/s. DPSK selects 1200 bit/s. FSK selects V.23 mode.
		1	DPSK selects 600 bit/s. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB/ ADD PH.EQ	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate output at CLK pin in all modes.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB/ ADD PH.EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler/ Add Ph. Eq.	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path. In the V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupts will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION			DESCRIPTION
D0	Signal Quality Indicator	0			Indicates normal received signal.
		1			Indicates low received signal quality (above average error rate). Interacts with special Register SQ bits D1, D0.
D1	Call Progress Detect	0			No call progress tone detected.
		1			Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0			Condition not detected
		1			Condition detected
		CR0 D0	TR D0	CR2 D5	
		1	0	1	2225 Hz ±10 Hz answer tone detected in V.22bis, V.22, V.21 modes.
		1	1	1	2100 Hz ±1% answer tone detected in V.22bis, V.22, V.21 modes.
		1	X	0	2225 ± 1% or 2100 Hz ±10 Hz Answer tone detected in V.22bis, V.22, V.21 modes.
		0	0	1	1300 Hz calling tone detected in V.22 bis, V.22, V.21, V.23 modes.
		0	1	0	900 Hz SCT tone detected in V.23 mode.
D3	Carrier Detect	0			No carrier detected in the receive channel.
		1			Indicated carrier has been detected in the received channel. Should be time qualified by software.
D4	Unscr. Mark Detect	0			No unscrambled mark bring received.
		1			Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data				Continuously outputs the received data stream.
					This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0			No S1 pattern being received.
		1			S1 pattern detected. Should be time qualified by software. S1 is an unscrambled double dibit (11001100...) sent in DPSK mode.
D7	Receive Level Indicator	0			Received signal level below threshold, (≈ -19 dBm0);can use receive gain boost (+12 dB.)
		1			Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ CALLING/SCT TONE/SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Guard Tone/ Answer Tone/ Calling/SCT/ Tone/ Detect/Select	D6 D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
		1 X 0 0	Select 1800 Hz guard tone if in V.22bis or V.22 and answer mode in CR0.
		1 X 0 1	Select 550 Hz guard tone if in V.22bis or V.22 and answer mode in CR0.
		X 0 0 0	2225 Hz answer tone will be detected in D2 of DR or if V.21, V.22, or V.22bis originate mode is selected in D0.
		X 0 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 or V.22 originate mode is selected in CR0.
		0 0 0 0	1300 Hz calling tone will be detected in D2 of DR if V.21, V.22, V.22bis or V.23 answer mode is selected in CR0 and CR2 bit D5 = 1.
		X 0 0 0	Transmit 2225 Hz Answer Tone. Must be in DPSK answer mode.
		X 1 0 0	Transmit 2100 Hz Answer Tone. Must be in DPSK answer mode.
		X 0 0 1	900 Hz SCT (soft carrier turnoff) tone detected in V.23 1200 bit/s receive mode. (CR0 bit D0 = 0).
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM/DPSK +1% -2.5%.
		0 1	Asynchronous QAM/DPSK, 2400, 1200 or 600 bit/s +2.3% -2.5%.
D2	DTMF 2/ FDX	D4 D2	
		0 0	Selects 2-wire full-duplex or half-duplex.
		0 1	Selects 4-wire full-duplex in the mode selected by CR0 D7-D5, D0

Note: DTMF0 - DTMF2 should be set an appropriate state after DTMF dialing to avoid inadvertant unintended operation.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ FDX	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ CALLING/SCT TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ FDX	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ CALLING/SCT TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Transmit DTMF	0	Disabled DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	Transmit Answer Tone	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2100 Hz or 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode. To transmit answer tone, the device must be in DPSK answer mode.
D6	Transmit Guard, Soft Carrier Turnoff or Calling Tone	0	Disables guard/calling SCT tone generator.
		1	Transmit guard tone if in V.22 bis, V.22 and answering; or transmit Calling Tone if Orig and not V.23; or transmit SCT if Orig and in V.23.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This signal is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.
D4	Transmit S1	0	The transmitter when placed in QAM alternating mark/space mode transmits 0101..... scrambled or not dependent on the bypass scrambler bit.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the various mode bits. Answer tone bandwidth 2100 Hz ±10 Hz, 2225 Hz ±1%.
		1	The DSP decodes both answer tone and call progress tones. 2100 Hz answer tone ±1%, 2225 Hz ±10 Hz.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the SPECIAL REGISTER. See the SPECIAL REGISTER for details.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	TXDALT	TX/RX CLOCK CONTROL	0	RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Sets the attenuation level of the transmitted signal in 1dB steps. The default (D3-D0=0100) is for a transmit level of -10 dBm0 at the line with the recommended hybrid transmit gain. The total range is 16 dB.
D4	Receive Gain Boost	0	12 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D5	Not Used		Not used. Only write zeros this location.
D6	RX/TX Clock Control		RX/TX Clock Tristate control. Controls output state of TXCLK and RXCLK.
		0	Outputs driven
		1	Outputs in Tristate mode
D7	TXDALT	N/A	Alternate TX data source. See Special Register.

SPECIAL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
SR 101		TXBAUD CLOCK	RXUN-DSCR DATA		TXD SOURCE	SIGNAL QUALITY LEVEL SELECT1	SIGNAL QUALITY LEVEL SELECT0	

BIT NO.	NAME	DESCRIPTION
D7, D4, D0		NOT USED AT THIS TIME. Only write ZEROs to these bits.
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.
D5	RXUNDSCR DATA	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.

SPECIAL REGISTER (Continued)

BIT NO.	NAME	DESCRIPTION	
D3	TXD SOURCE	This bit selects the transmit data source; either the TXD pin if ZERO or the TXDALT if this bit is a ONE. The TRANSMIT PATTERN bits D7 and D6 in CR1 override either of these sources.	
D2, D1	SIGNAL QUALITY LEVEL SELECT	The signal quality indicator is a logical ONE when the signal received is not acceptable for low error rate reception. It is determined by the value of the Mean Squared Error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a ONE constantly. The SQI bit and threshold selection are valid for QAM and DPSK only.	
	D2 D1	**THRESHOLD VALUE**	**UNITS**
	0 0	10^{-5}	BER (default)
	0 1	10^{-6}	BER
	1 0	10^{-4}	BER
	1 1	10^{-3}	BER

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a ONE and addressing CR3. This register provides functions to the 73K324L user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a ZERO.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 2	ID 1	ID 0					

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5	Device Identification Signature	D7 D6 D5	Indicates Device:
		0 0 X	SSI 73K212(L) or 73K322L
		0 1 X	SSI 73K221(L) or 73K302L
		1 0 X	SSI 73K222(L)
		1 1 0	SSI 73K224L
		1 1 1	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(VDD to GND)	0.1			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
XTL1 Load Capacitance	Depends on crystal requirements			40	pF
XTL2 Load Capacitance	Depends on crystal requirements			20	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		55	°C

DC ELECTRICAL CHARACTERISTICS
(TA = -40°C to 70°C, VDD =recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
	ISET Resistor = 2 MΩ				
IDD1, Active			25	27	mA
IDD2, Idle			3		mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VIH MAX			100	µA
IIL, Input Low Current	VI = VIL MIN	-200			µA
Reset Pull-down Current	Reset = VDD	5		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
VOL, CLK Output	IOUT = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-5		-50	µA
Capacitance					
Maximum Capacitive Load					
CLK				15	pF
Input Capacitance	All Digital Inputs			10	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks ATT=0100 (default)	-11.5	-10.0	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-.31		+.05	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
Output Distortion	All products through BPF			-45	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±10		%
Jitter	Transmit Dotting Pattern in ALB @ RXD		±10		%
2100 Hz Answer Tone Generator					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21 or V.23 Mode	-11.5	-10	-9	dBm0
Output Distortion	All products though BPF			-40	dB
NOTE: Parameters expressed in dBm0 refer to the following definition: 0 dB loss in the Transmit path to the line. 2 dB gain in the Receive path from the line. Refer to the Basic Box Modem diagram in the Applications section for the DAA design.					
DTMF Generator	Not in V.21 or V.23 mode				
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band, ATT = 0100	-10		-8	dBm0
Output Amplitude	High Band, ATT = 0100	-8		-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Receiver Dynamic Range	Refer to Performance Curves	-48		-3.0	dBm0
Call Progress Detector	In Call Init mode				
Detect Level	460 Hz test signal	-34		0	dBm0
Reject Level				-40	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			25	ms
Hysteresis		2			dB

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect						
Threshold		QAM/DPSK or FSK receive data	-48		-43	dBm0
Hysteresis		All Modes	2			dB
Delay Time	FSK, DPSK or QAM	-70 dBm0 to -6 dBm0	10		30	ms
Hold Time	FSK, DPSK or QAM	-6 dBm0 to -70 dBm0	10		65	ms
Special Tone Detectors						
Detect Level		See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time						
2225 or 2100 Hz answer tone		See detect register for detect bandwidth	10		45	ms
1300 Hz calling tone		Tone Accuracy ±0.5%	10		45	ms
900 Hz SCT V.23 main channel		Tone Accuracy ±5 Hz	10		45	ms
Hold Time						
2100 Hz answer tone		See detect register for detect bandwidth	10		45	ms
1300 Hz calling tone		Tone Accuracy ±0.5%	10		45	ms
900 Hz SCT V.23 main channel Mark		Tone Accuracy ±5 Hz	10		45	ms
Hysteresis			2			dB
Pattern Detectors		DPSK Mode				
S1 Pattern						
Delay Time		For signals from -6 to -40 dBm0,	10		45	ms
Hold Time		Demod Mode	10		45	ms
Unscrambled Mark						
Delay Time		For signals from -6 to -40	10		45	ms
Hold Time		Demod or call Init Mode	10		45	ms
Receive Level Indicator						
Detect On					-19	dBm0
Valid after Carrier Detect			10			ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output Load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 dB in .3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy	4 kHz, Guard Tones off			-35	dBm0
	10 kHz, Guard Tones off			-55	dBm0
	12 kHz, Guard Tones off			-65	dBm0
Anti Alias Low Pass Filter					
Maximum allowed Out-of-Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Level at RXA pin with receive Boost Enabled				
	Scrambled data at 2400 bit/s in opposite band			-14	dBm
	Sinusoids out of band			-9	dBm
Transmit Attenuator					
Range of Gain	Relative to -10 dBm0	+4		-11	dB
Step Accuracy		-0.15		+0.15	dB
Clock Noise	TXA pin; 153.6 kHz		1.5		mV rms
Carrier Offset					
Capture Range	Originate or Answer	-10	±7	+10	Hz
Recovered Clock					
Capture Range	% of data rate originate or answer	-.024		+.024	%
Guard Tone Generator					
Tone Accuracy	550 Hz			+1.18	%
	1800 Hz	-0.7			%
Tone Level	550 Hz	-5.0	-3.0	-2.0	dB
(Below QAM/DPSK Output)	1800 Hz	-8.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
(700 to 2900 Hz)	1800 Hz			-60	dB

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

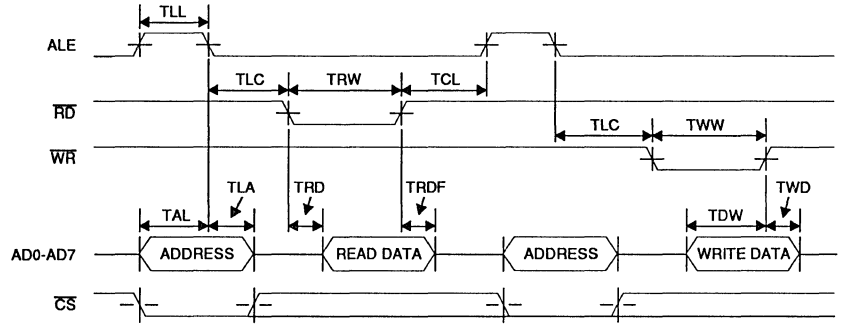
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}/\overline{WR}$ Low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		200	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000*	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control**	50			ns
TCA	Address hold after control**	50			ns
TWH	Data Hold after EXCLK	20			

* Maximum time applies to parallel version only.

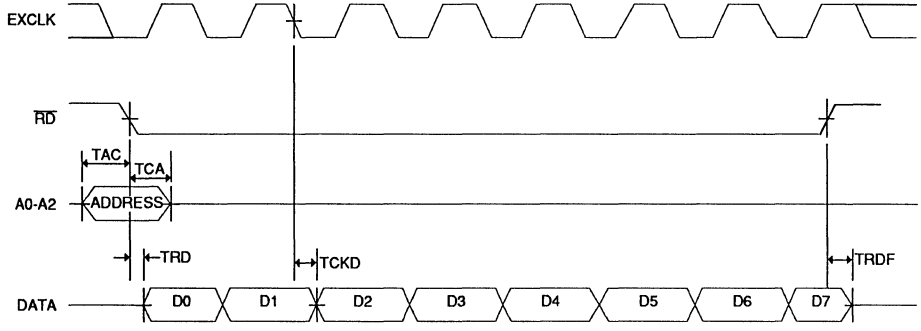
** Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

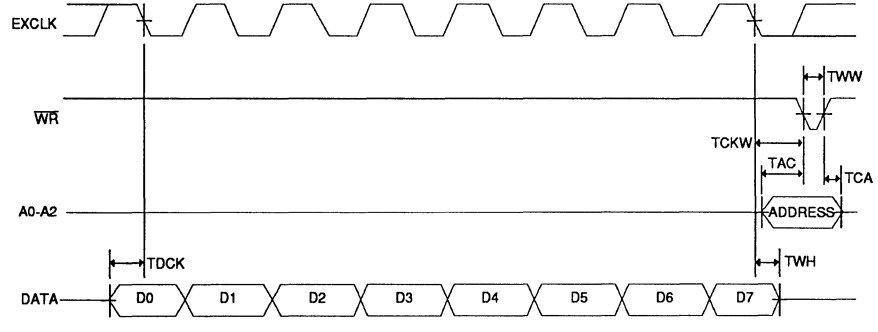
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

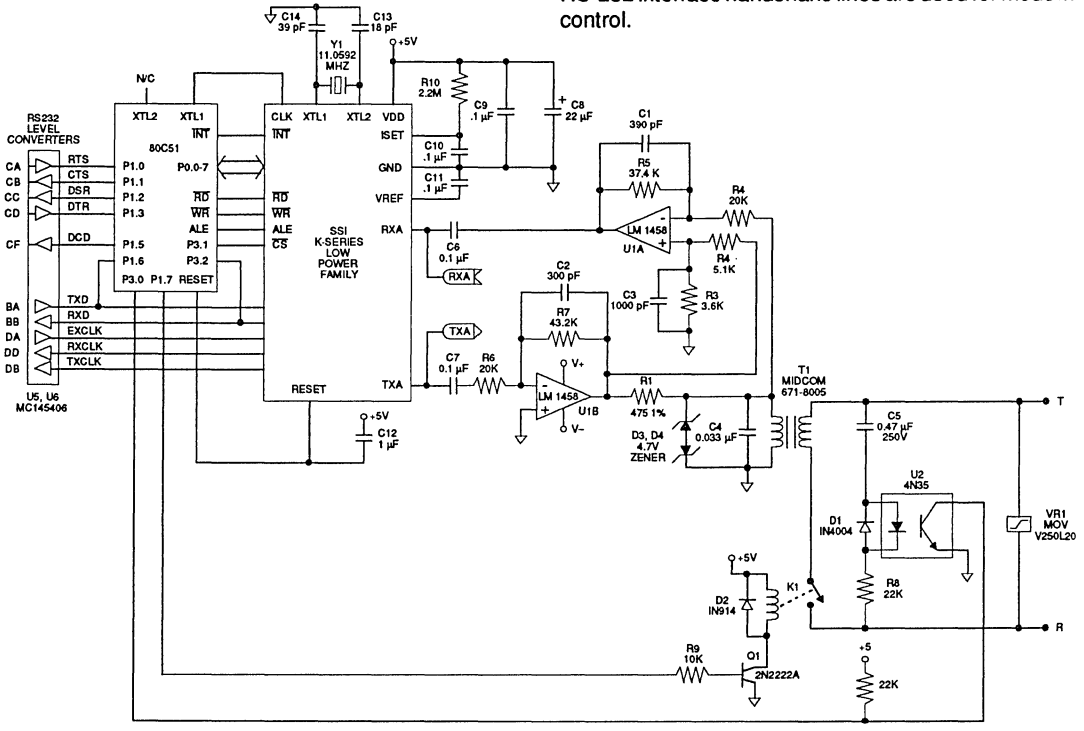


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.

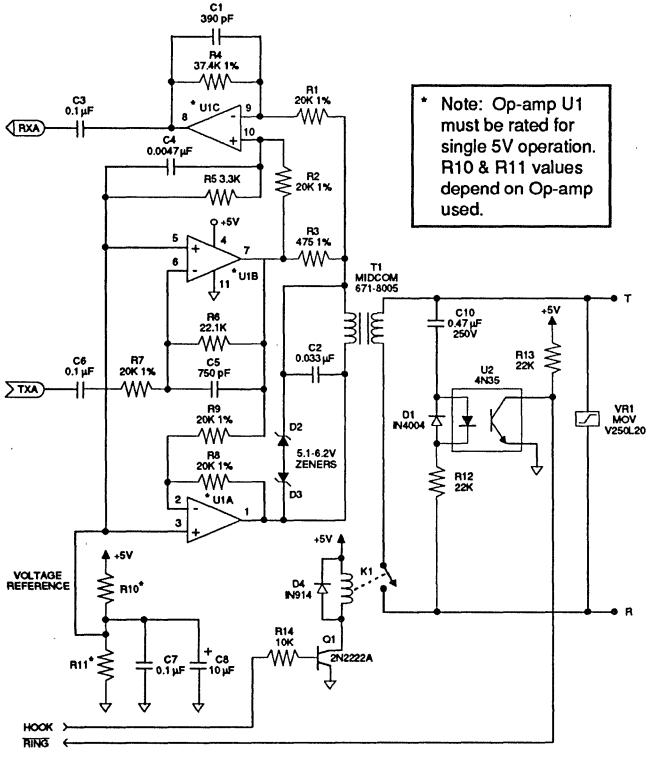


FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

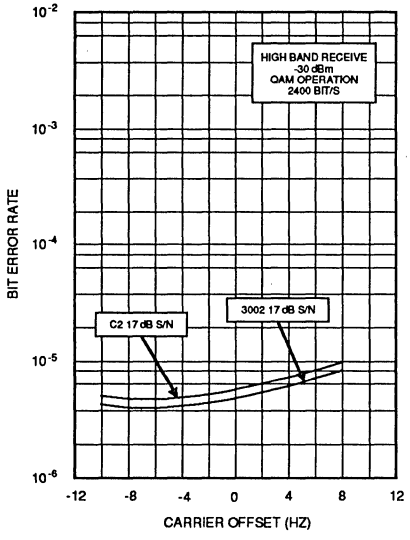
BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

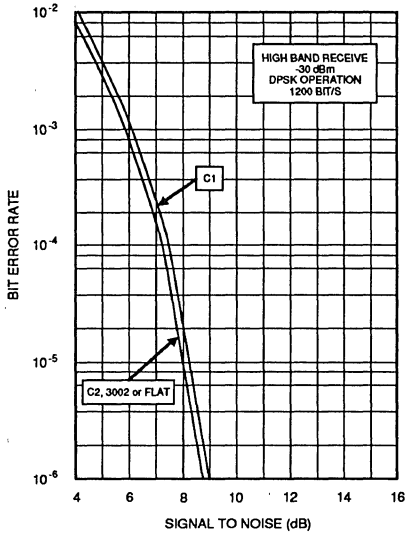
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

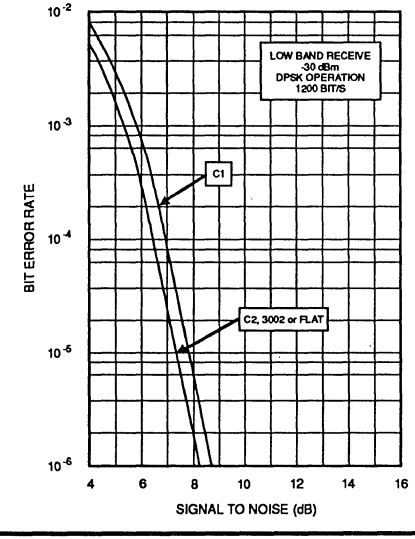
SSI 73K324L BER vs CARRIER OFFSET
PRELIMINARY



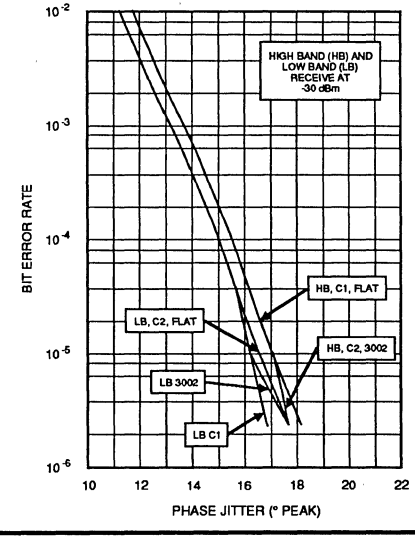
SSI 73K324L BER vs S/N
PRELIMINARY



SSI 73K324L BER vs S/N
PRELIMINARY

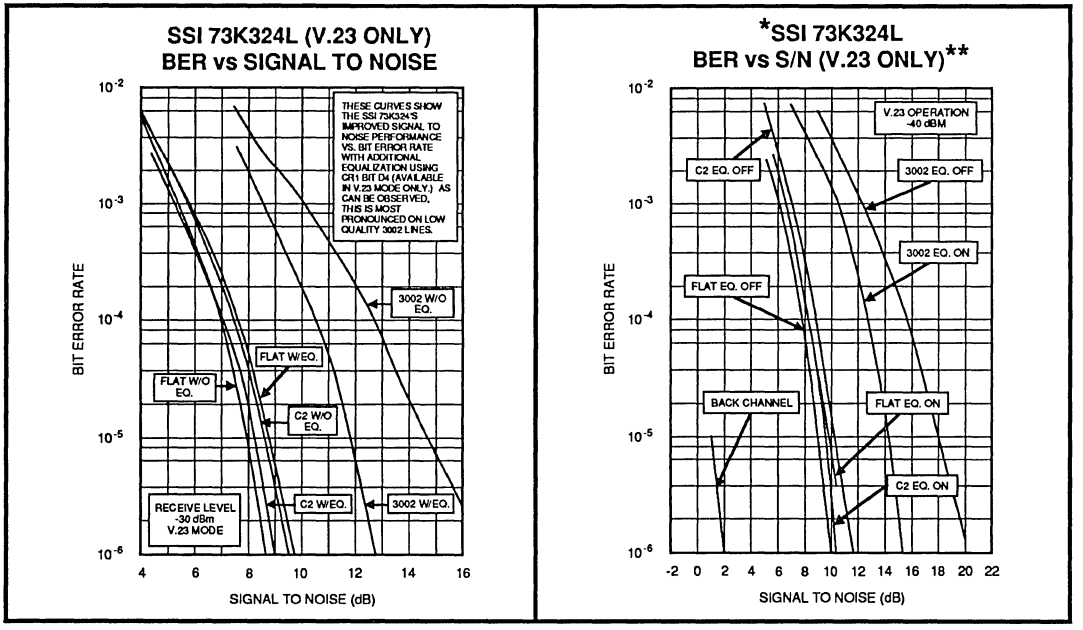


SSI 73K324L BER vs QAM



* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

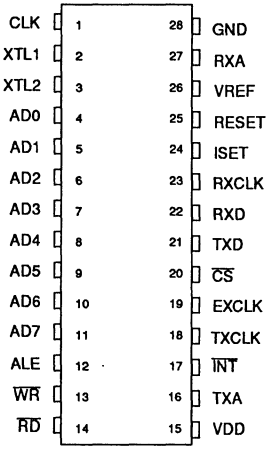


* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

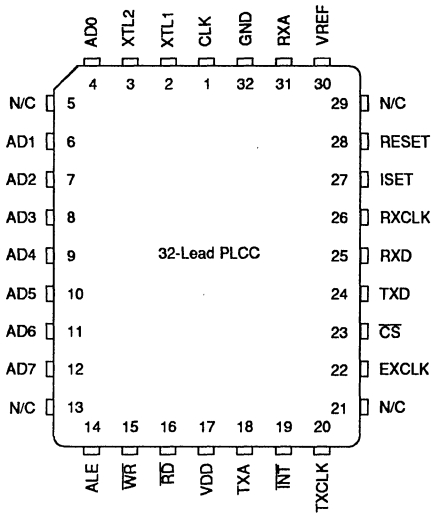
** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

SSI 73K324L
CCITT V.22bis, V.22, V.21, V.23
Single-Chip Modem

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



600-Mil
28-Pin DIP



32-Lead PLCC

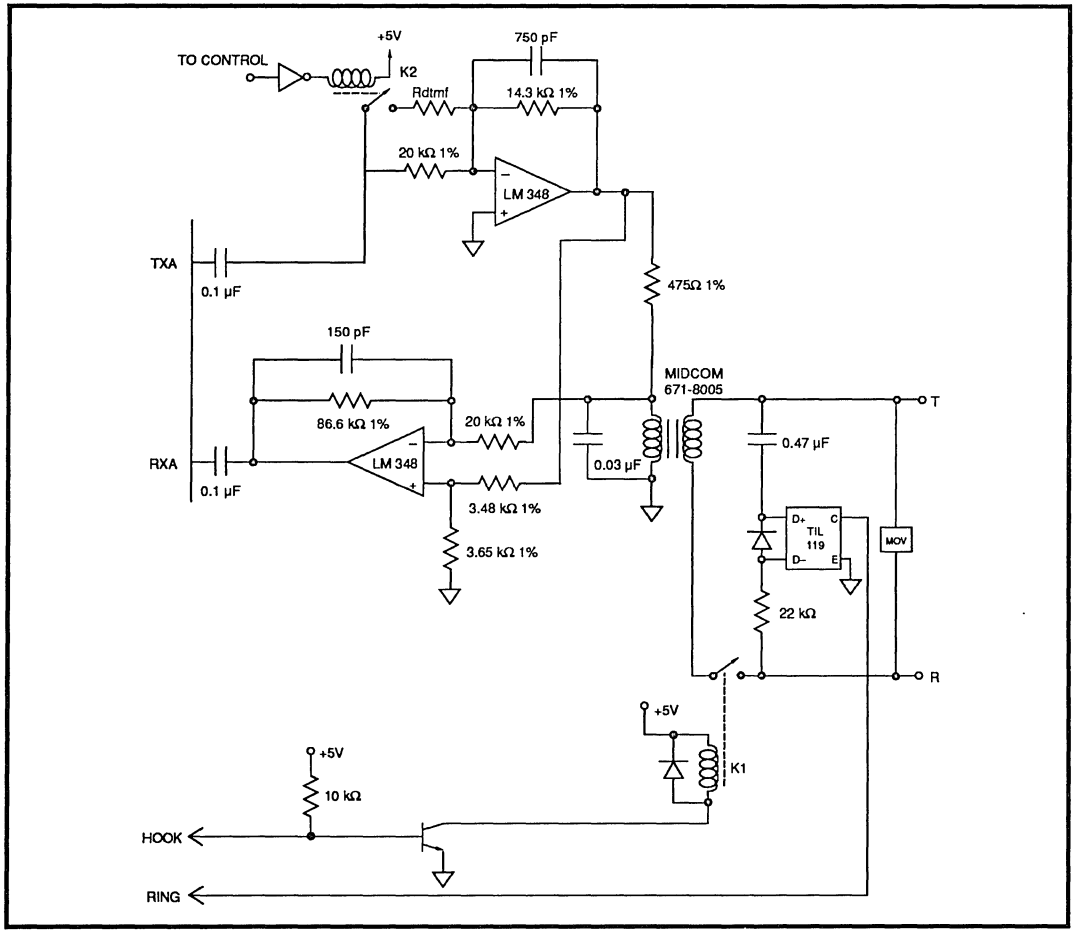
Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Setting DTMF Levels for 1200 Bit/s K-Series Modems

Some applications of the K-series modems without output level adjustment may require setting the DTMF transmit level to something other than the normally transmitted level. This level is nominally about 5 dB higher than during data transmission. If the data is transmitted at -10 dBm, the DTMF levels will be at about -5 dBm, which is adequate in most applications.

The simplest way to change the relative levels of DTMF tones and data is to change the transmit gain during dialing. This can be accomplished as shown below. In this example, it is assumed that the DTMF tones are to be transmitted at a higher level than normal. Closing relay K2 will increase the gain of the transmit op-amp and allow a higher DTMF tone level during dialing. If it is desired to decrease the DTMF level, the relay can be open for dialing and closed for data. The value of the shunt resistor, Rdtmf, will be relatively large compared to the resistor R1, therefore the precision of Rdtmf is not as critical as R1. This means an analog switch or similar device could be used instead of a relay, with the on resistance of the switch not seriously affecting the tolerance of the gain setting.



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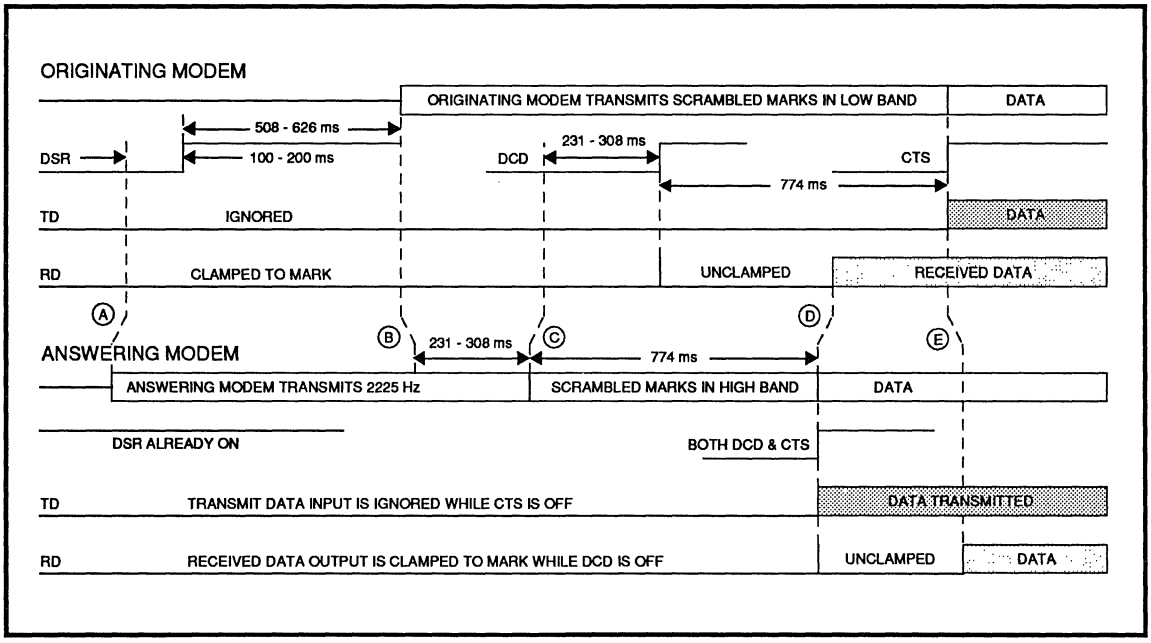
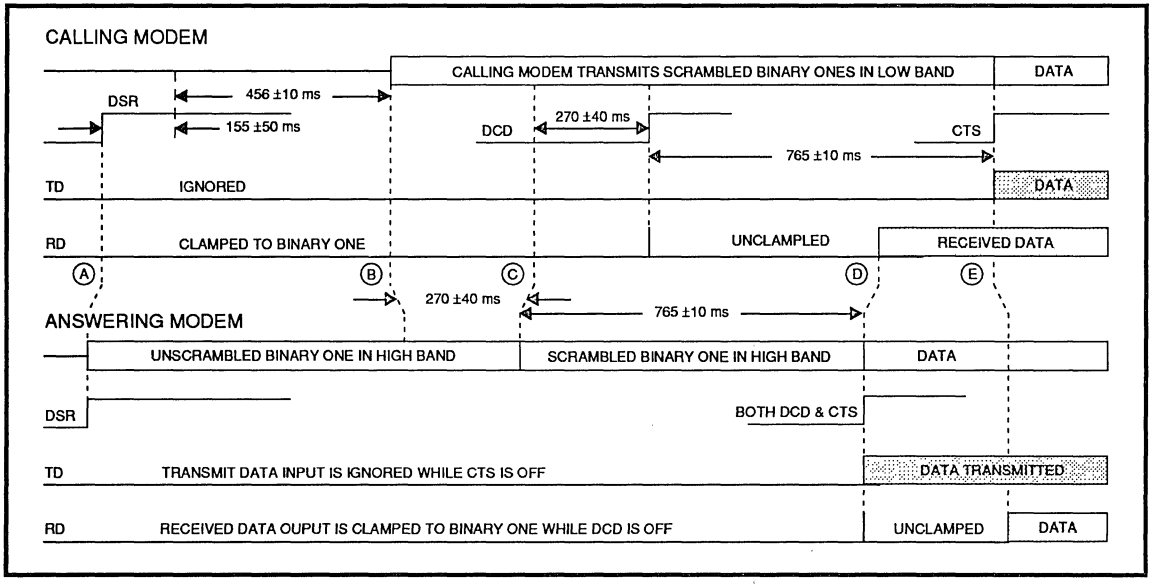
APPLICATION NOTE

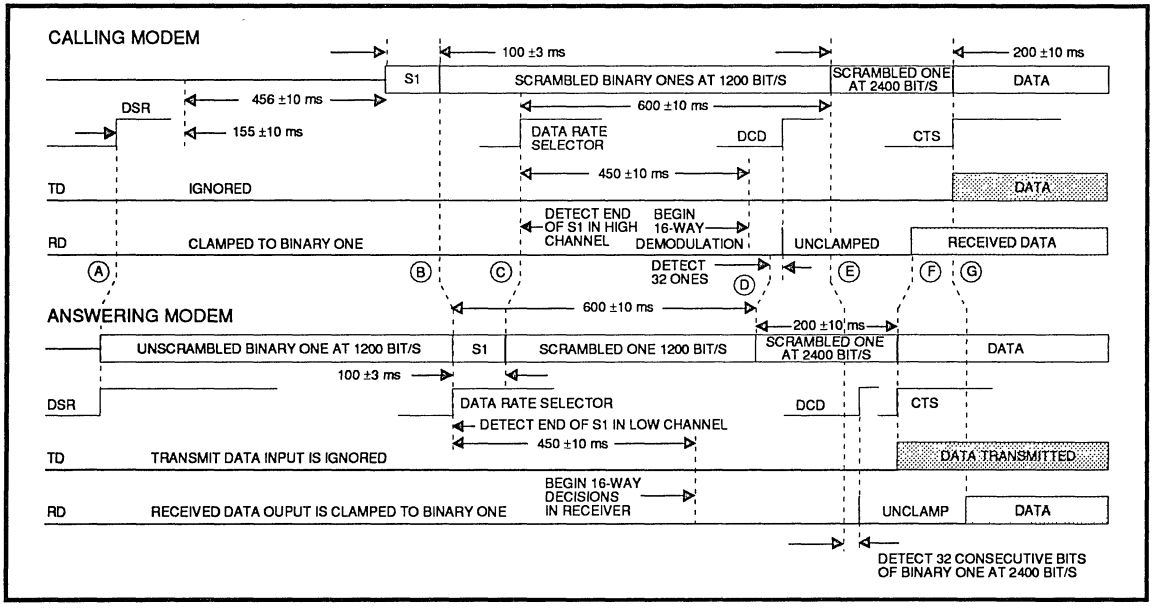
SSI 73K212A High Speed Connect Sequence



V.22


CALLING MODEM
CALLING MODEM TRANSMITS SCRAMBLED BINARY ONES IN LOW BAND
DATA
DSR
456 ±10 ms
155 ±50 ms
DCD
270 ±40 ms
CTS
765 ±10 ms
TD
IGNORED
DATA
RD
CLAMPED TO BINARY ONE
UNCLAMPLED
RECEIVED DATA
A
B
C
D
E
270 ±40 ms
765 ±10 ms
ANSWERING MODEM
UNSCRAMBLED BINARY ONE IN HIGH BAND
SCRAMBLED BINARY ONE IN HIGH BAND
DATA
DSR
BOTH DCD & CTS
TD
TRANSMIT DATA INPUT IS IGNORED WHILE CTS IS OFF
DATA TRANSMITTED
RD
RECEIVED DATA OUPUT IS CLAMPED TO BINARY ONE WHILE DCD IS OFF
UNCLAMPED
DATA

V.22bis


CALLING MODEM
100 ±3 ms
200 ±10 ms
S1
SCRAMBLED BINARY ONES AT 1200 BIT/S
SCRAMBLED ONE AT 2400 BIT/S
DATA
DSR
456 ±10 ms
600 ±10 ms
155 ±10 ms
DATA RATE SELECTOR
DCD
CTS
450 ±10 ms
TD
IGNORED
DATA
DETECT END OF S1 IN HIGH CHANNEL
BEGIN 16-WAY DEMODULATION
RD
CLAMPED TO BINARY ONE
UNCLAMPED
RECEIVED DATA
DETECT 32 ONES
A
B
C
D
E
F
G
ANSWERING MODEM
600 ±10 ms
200 ±10 ms
UNSCRAMBLED BINARY ONE AT 1200 BIT/S
S1
SCRAMBLED ONE 1200 BIT/S
SCRAMBLED ONE AT 2400 BIT/S
DATA
100 ±3 ms
DSR
DATA RATE SELECTOR
DCD
CTS
DETECT END OF S1 IN LOW CHANNEL
450 ±10 ms
TD
TRANSMIT DATA INPUT IS IGNORED
DATA TRANSMITTED
BEGIN 16-WAY DECISIONS IN RECEIVER
RD
RECEIVED DATA OUPUT IS CLAMPED TO BINARY ONE
UNCLAMP
DATA
DETECT 32 CONSECUTIVE BITS OF BINARY ONE AT 2400 BIT/S

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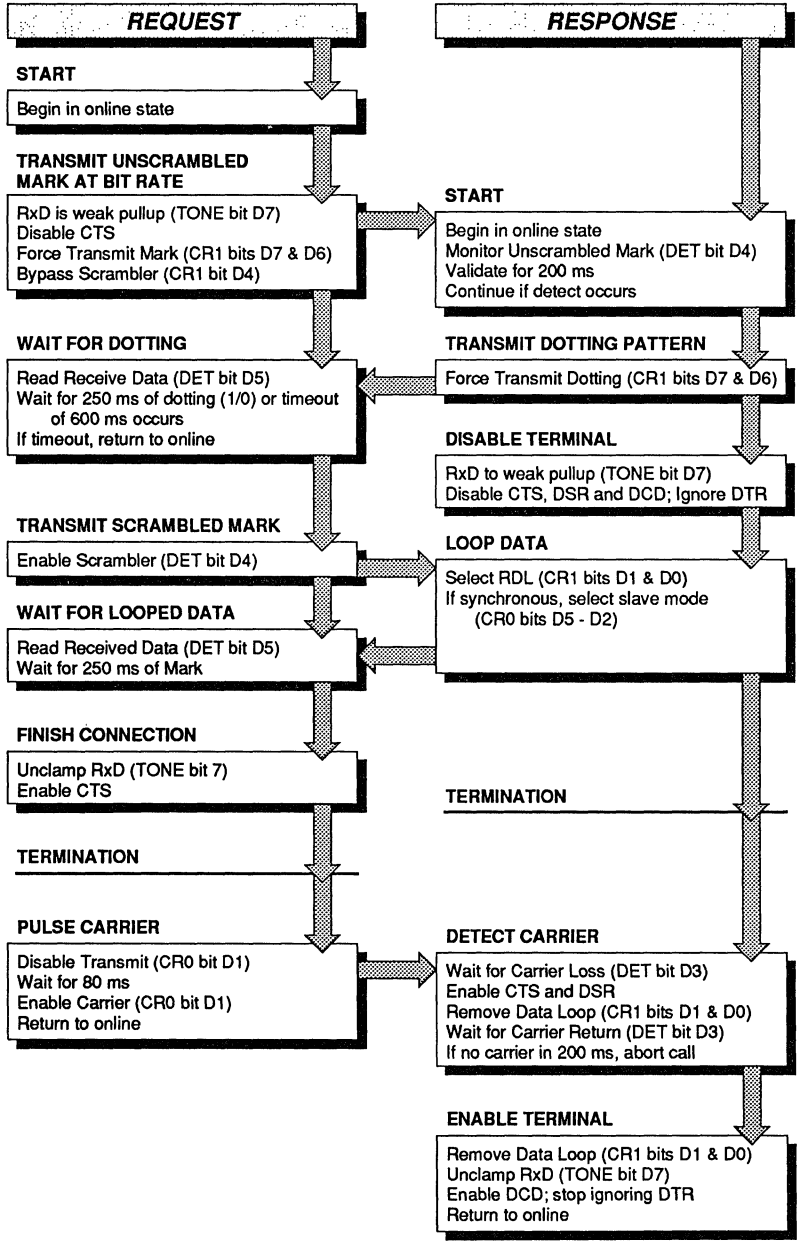
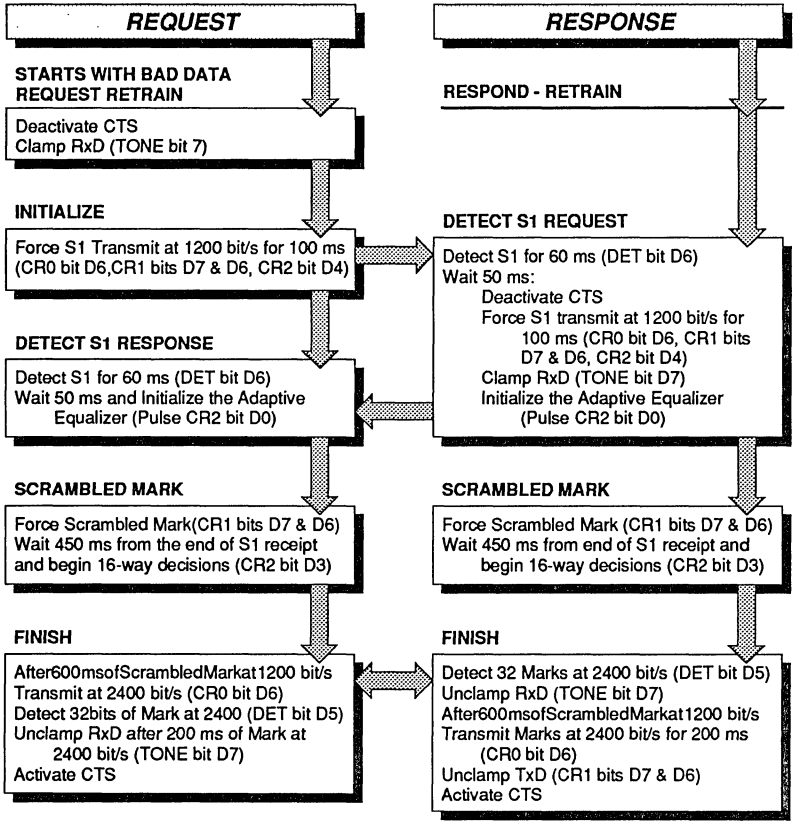
APPLICATION NOTE

Remote Loop Handshake Sequence




REQUEST
RESPONSE
STARTS WITH BAD DATA
REQUEST RETRAIN
Deactivate CTS
Clamp RxD (TONE bit 7)
RESPOND - RETRAIN
INITIALIZE
Force S1 Transmit at 1200 bit/s for 100 ms
(CR0 bit D6,CR1 bits D7 & D6, CR2 bit D4)
DETECT S1 REQUEST
Detect S1 for 60 ms (DET bit D6)
Wait 50 ms:
Deactivate CTS
Force S1 transmit at 1200 bit/s for
100 ms (CR0 bit D6, CR1 bits
D7 & D6, CR2 bit D4)
Clamp RxD (TONE bit D7)
Initialize the Adaptive Equalizer
(Pulse CR2 bit D0)
DETECT S1 RESPONSE
Detect S1 for 60 ms (DET bit D6)
Wait 50 ms and Initialize the Adaptive
Equalizer (Pulse CR2 bit D0)
SCRAMBLED MARK
Force Scrambled Mark(CR1 bits D7 & D6)
Wait 450 ms from the end of S1 receipt
and begin 16-way decisions (CR2 bit D3)
SCRAMBLED MARK
Force Scrambled Mark (CR1 bits D7 & D6)
Wait 450 ms from end of S1 receipt and
begin 16-way decisions (CR2 bit D3)
FINISH
After600msofScrambledMarkat1200 bit/s
Transmit at 2400 bit/s (CR0 bit D6)
Detect 32bits of Mark at 2400 (DET bit D5)
Unclamp RxD after 200 ms of Mark at
2400 bit/s (TONE bit D7)
Activate CTS
FINISH
Detect 32 Marks at 2400 bit/s (DET bit D5)
Unclamp RxD (TONE bit D7)
After600msofScrambledMarkat1200 bit/s
Transmit Marks at 2400 bit/s for 200 ms
(CR0 bit D6)
Unclamp TxD (CR1 bits D7 & D6)
Activate CTS

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APPLICATION NOTE

SSI 73K212 & 73K222 Originate Handshake Sequence

(RXD is in tri-state mode, TONE bit D7≤1)

DIAL
1. Go off hook
2. Bring out of power down mode (CR0 bits D5-D2)
3. Set DTMF tone (Tone bits D4-D0)
4. Turn on transmitter (Set CR0 bit D1)
5. Wait DTMF on time
6. Turn off transmitter (Clear CR0 bit D1)
7. Wait DTMF off time
8. Repeat 3-7 for all digits

WAIT FOR CARRIER
1. Start S7 (Wait for carrier) timeout
2. Set to Bell 103 originate mode (Set CR0 bits D5-D0 to 110001)
3. Wait for carrier detect bit (DR bit D3) to come on
4. Start sliding window counter (Wait through possible 2100 Hz answer tone period)
5. Qualify RXD mark* for 150 ms (DR bit D5) to detect answer modem (Carrier detect bit must also be on)
6. Raise DSR

FSK
1. Wait 100-200 ms
2. Raise DCD, start 755-774 ms timer; wait 426-446 ms, send FSK marks (Set CR1 bits D7 & D6 to 10, set CR0 bit D1)
3. At end of 755-774 ms timer period (started in #2 above); raise CTS, unclamp RXD & TXD from marking (clear TONE bit D7; clear CR1 bits D7 & D6)

DPSK
1. Wait 456 (V.22) or 508-626 ms (212A), switch to DPSK
2. Send scrambled marks (Set CR1 bits D7 & D6 to 10)
3. Qualify scrambled marks from answer modem for 150 ms
4. Wait for 231-302 ms of scrambled marks, raise DCD
5. Enable RXD (Tone bit D7)
6. Wait 774 ms, raise CTS, enable TXD (Clear CR1 bits D7 & D6)

*This may be either answer tone from a Bell modem or unscrambled marks from a V.22 modem

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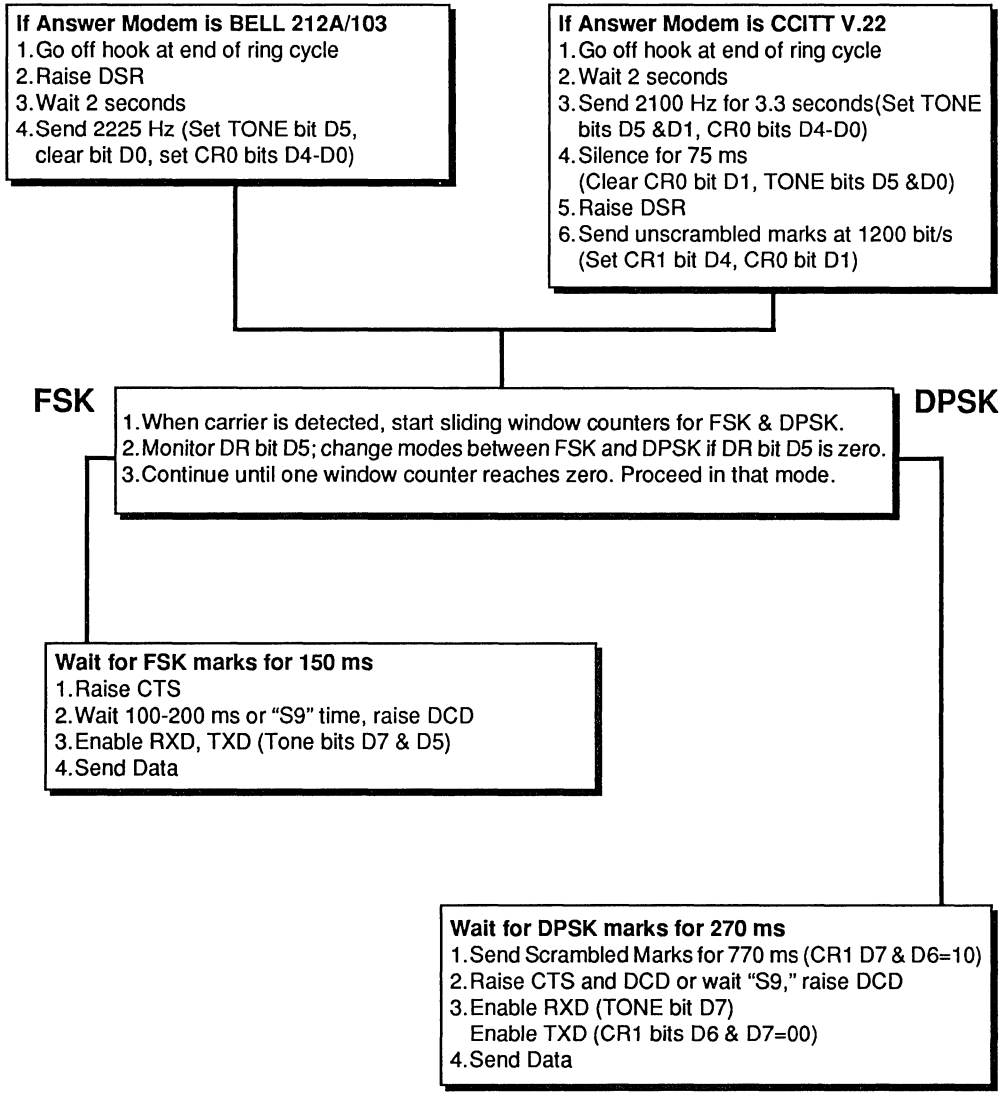
APPLICATION NOTE

SSI 73K212 & 73K222 Answer Handshake Sequence

1

(RXD is in tri-state mode, TONE bit D7=1)



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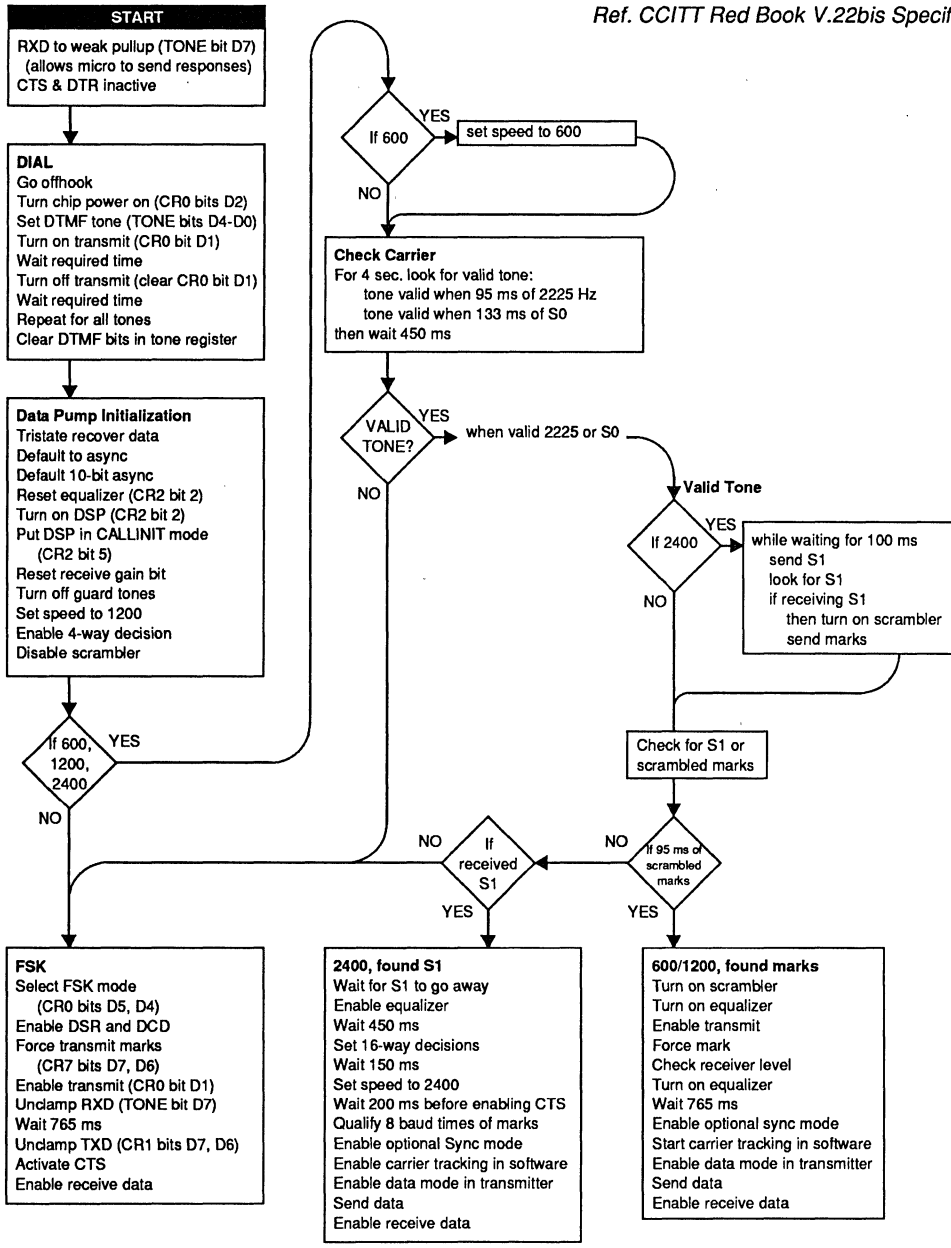
APPLICATION NOTE

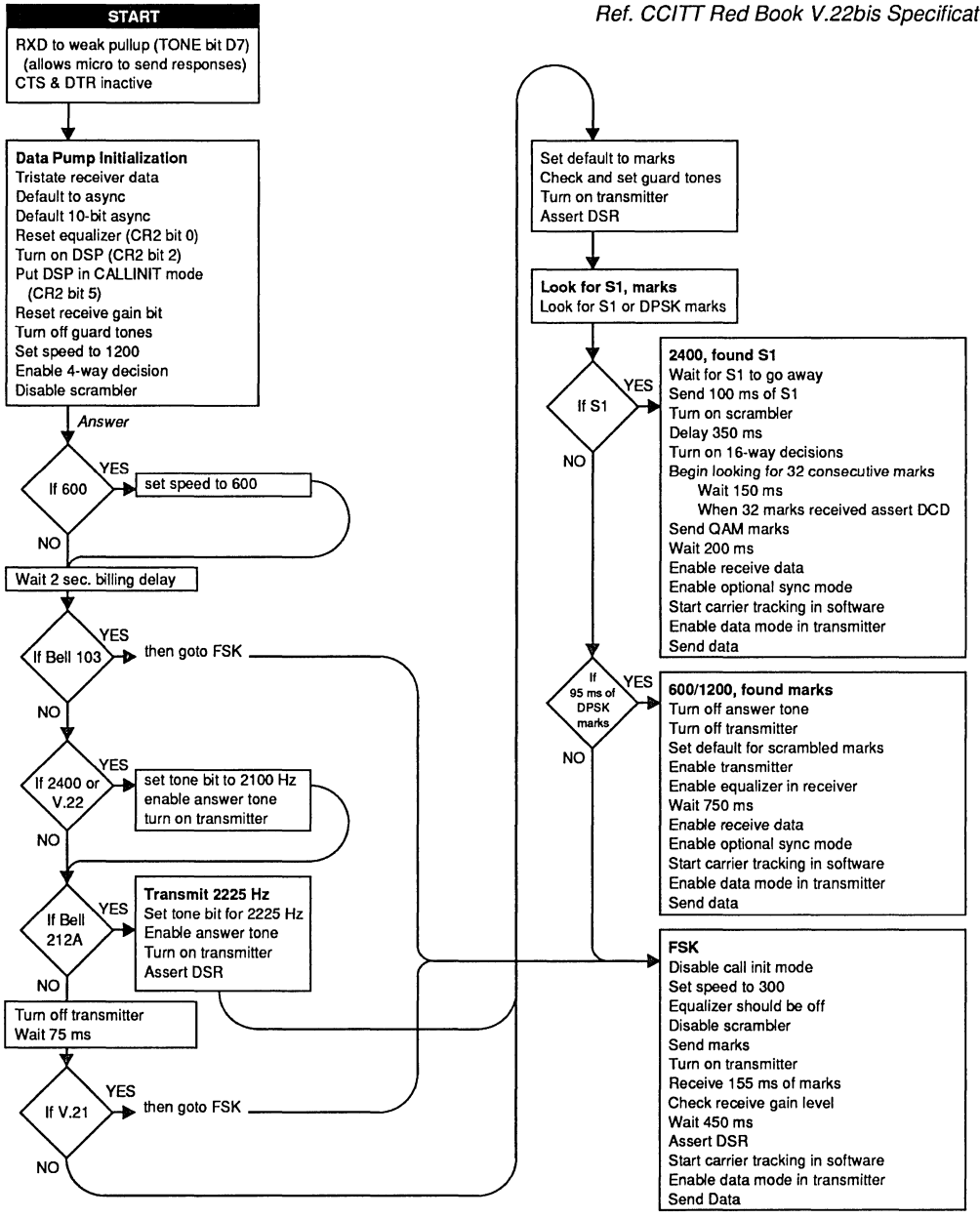
SSI 73K224 Originate Handshake Sequence

Ref. CCITT Red Book V.22bis Specification



SSI 73K224 Answer Handshake Sequence

Ref. CCITT Red Book V.22bis Specification



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APPLICATION NOTE

Performance Testing
Silicon Systems K-Series Single-Chip Modem Family

Why Modem Performance Is Important

In today's world of expanding communications, the modem has become an essential element in providing data communications capability for such applications as personal computers, lap-top PCs, and hand-held portable terminals. To fit the requirements of these systems, the modem must become more compact even as it becomes more complex. As more modem functions are integrated onto a single chip, it is the modem IC that becomes the key to designing small footprint modems that integrate well into today's computer applications.

Trying to compare competitive modem ICs by analyzing published technical specifications can be misleading. No meaningful comparisons can be made, because data sheets provide little useful performance information. Products that appear functionally competitive can vary widely in datacom performance.

Hidden differences in modem architecture can have a profound effect on overall modem operation. Where one modem IC might perform well within a real-world operating environment, another seemingly comparable IC might perform just marginally. So ultimately what the designer needs is a way to realistically compare modem ICs by their ability to perform, error-free, under real-world operating conditions.

The Real World of Telecommunications

Telephone lines vary. In different geographical areas, factors such as age, technology, and upkeep of equipment all contribute to variations in the physical operating environment. The physical mechanics of call-routing introduce other uncertainties, since call-routing can be completely random in a typical dial-up connection due to the automatic routing techniques being used.

Also, differences in the switching and multiplexing methods used in different locations, as well as differences in the conductive medium (copper-wire or fiber-optics), all add to the mix, making it difficult to design a modem that will perform well in a manner that is transparent to all of these factors.

These equipment and routing factors that adversely affect data communications create performance aberrations that are known collectively as line impairments. These line impairments cause the real-world side-effects that define the actual environment in which the modem, and the modem IC, must survive and perform.

Line Impairments

Generally, line impairments can be classified into four categories: line noise, signal-level variations, phase distortion, and carrier offset.

Line Noise

Line noise is the most common impairment to efficient datacommunications and can manifest itself in many ways. Ambient noise, for example, can be caused by copper line conductors. Wideband noise can be generated by hybrid repeater amplifiers in the network. Crosstalk from adjacent lines can sometimes couple into the connection and add to noise on the line.

Generally, noise impairments occur within the 300 to 3000 Hz voiceband, since other frequencies are attenuated by repeaters or filters on the line. The specific quality that enables a modem IC to operate error-free in a noisy line environment can be found in its design architecture, which reflects the functional efficiency of both its components and its circuit layout.

Signal-Level Variations

High signal-level is one impairment in this category. This stronger-than-normal signal can occur when an unusually efficient connection is made, as when routed through a PBX or when the transmitter and receiver are within close proximity to one another. A maximum level for normal operation on a dial-up line might be -10 dBm. An abnormally high level might approach 0 dBm.

Low signal-levels result from high line-resistance or from long, circuitous call-routing paths. The lowest signal level expected on a dial-up line is -45 dBm. The ability of the modem to handle abnormally high or low signal-levels is defined by its dynamic range.

Gain hits are short, quick changes in the receive signal's amplitude. The phenomenon can be caused by trunk-line switching activity or by sudden changes in line impedance, both of which can cause a breakdown in data-transfer integrity. Gain hits can be offset by fast-tracking capability within the AGC circuitry of the modem IC.

Phase Distortion

These impairments include phase jitter, phase hits, and group/envelope delay. Phase jitter is a periodic shift in the phase of the received carrier, which can be caused by variations in the line characteristics or by imperfections in the transmitting modem. Phase hits are more instantaneous in nature. They are characterized by significant changes in phase in the received carrier and are caused by ongoing switching action in the dial-up network. Group delay (envelope delay) results from reactive line-impedance characteristics that induce phase shifts in the frequencies present in the received signal. The modem must correct for group-delay distortion. Failure to do so can result in a phenomenon known as intersymbol interference. This occurs when frequency elements from one signal-modulation period overlap those of another, making it difficult to detect the original phase-encoded information in the signal, thus introducing data errors.

Carrier Offset

This impairment refers to a shift in frequency between the transmitted signal and the received signal. The condition is often introduced during long-distance call routing, where frequency-division multiplexing combines lower-frequency voiceband signals into a higher frequency signal. This phenomenon can be offset by the modem's phase-lock-loop tracking capabilities.

How Modems Can Be Compared For Performance

In order to compare modem ICs realistically, the design engineer needs to test each device under conditions that reflect real-life telephone line conditions. To achieve this, a test environment must be set up to simulate a set of actual line characteristics that conform to specifications defined by Bell System published standards. The engineer can then subject each test modem to artificially induced impairments under each of these line-standard conditions and compare the specific performance of competitive modems. A range of line conditions must be used to show how the modem will operate over the random variety of lines that might be encountered in typical operation.

Line Standards

Characteristics for dial-up telephone lines are not commonly specified, but leased lines are conditioned lines for which linear-distortion characteristics, including frequency-response and envelope-distortion parameters, are guaranteed by the telephone company. The Bell System line standards define four premium line conditions that operate with characteristics similar to those found in dial-up lines. These lines, which allow for modem performance testing over a wide range of representative conditions, include the following:

The 3002 Line is the lowest quality leased line and represents the poorest environment for accurate data communications. Allowable amplitude variation is 15 dB over the voiceband range. Envelope delay can vary as much as 1750 microseconds over the 800 to 2600 Hz range.

The C1 Line is conditioned to a greater extent than the 3002 line and can be considered to represent the average in dial-up line characteristics. Amplitude variation over the frequency band of interest is limited to 8 dB. Allowable envelope delay is the same as for the 3002 line.

The C2 Line represents an intermediate-quality line for modem testing. Frequency response is limited to 8 dB amplitude variation. Envelope delay is improved to not more than 500 microseconds over a 1000 to 2600 Hz range.

The C4 Line represents the best line conditions to be expected in a dial-up telephone environment. Optimum modem performance would be expected using this standard. Group delay or attenuation is negligible. Frequency response is limited to 8 dB. Envelope delay distortion is held to less than 300 microseconds over a 1000 to 2600 Hz range.

The Testing Method

To qualify modem ICs for performance, the test method must be uniformly applied. A test unit is used to simulate each of the Bell System line standards and to generate the environmentally representative line impairments. A typical test set-up includes a line simulator, a personal computer, an RMS voltmeter, and a reference modem to test against. Control of the test parameters is handled by the PC connected to the test fixture through a GPIB data bus. The PC sets up and controls the line simulator, monitors the results, and accumulates the error count for each iteration.

Two modem ICs are compared in a typical test sequence. The modem IC to be tested is connected to the modem testing equipment via a breadboard evaluation fixture and is fed a continuous data stream for testing. The tester monitors the data received from the test modem and the data bit-errors are counted and plotted to signify the ratio between the number of bits transmitted compared to the number of transmission error-bits. This results in a statistical bit-error rate (BER).

The test method calls for a large sample of data errors to be simulated for each device, under each line condition. Multiple data points are taken for each test for each device. Test message data is transmitted in a

random, broad-range pattern. Each data point results from the transmission of a million data bits and a complete test sequence on a single modem IC could represent 100 hours of test time before a realistic error sampling might be realized.

The SSI K-Series Modem ICs

Silicon Systems' K-Series family of modem ICs use an integrated analog/digital design philosophy for enhanced high-performance operation, which virtually eliminates data-error-related modem failures. These pin and function-compatible family products comply with the full range of relevant worldwide operating standards for data transfer speeds ranging from 300 to 2400 bit/s. The SSI 73K224L, the industry's first 2400 bit/s single-chip modem for both US and European standards, features adaptive equalization, which further enhances performance by giving the modem the ability to adapt automatically to varying line conditions.

The K-Series modem ICs are used in the sample test curves presented with this document as a base against which competitive performance information can be compared.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

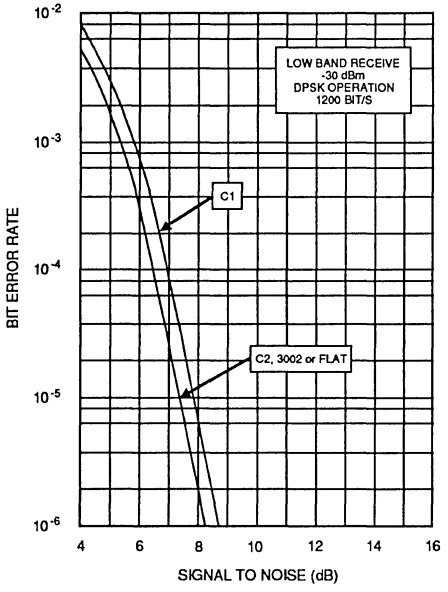
BER vs. Phase Jitter

DPSK and QAM modulation is sensitive to phase jitter. Modems using these techniques need to be as tolerant as possible of phase jitter on the line. In this test, relatively flat curves indicate minimal degradation of performance when phase jitter is encountered on the line.

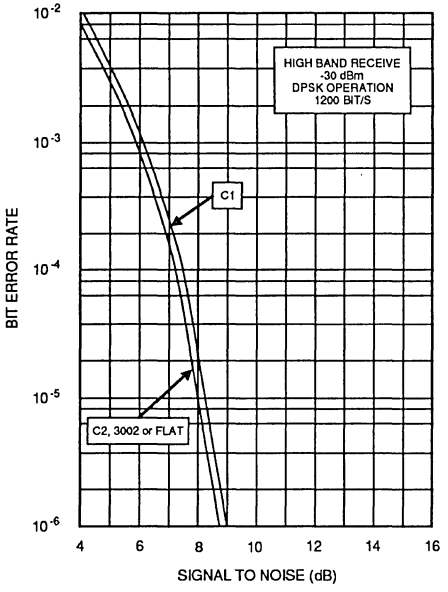
BER vs. Carrier Offset

This parameter indicates how the modem's performance is affected by the shifts in carrier frequency encountered in normal public telephone network operation. Flat curves are an indication that there is no performance degradation from frequency offsets. The SSI K-Series modem ICs use a second-order, carrier-tracking phase-lock-loop that is insensitive to carrier offsets in excess of 10 Hz. Both the Bell and European/Japanese CCITT specifications allow as much as 7 Hz offset.

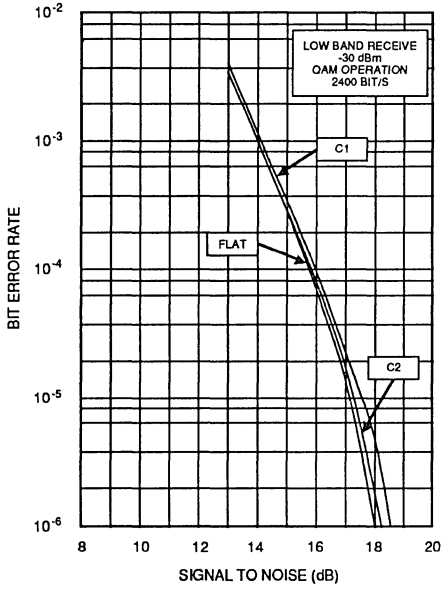
SSI 73K224L
BER vs. Signal to Noise



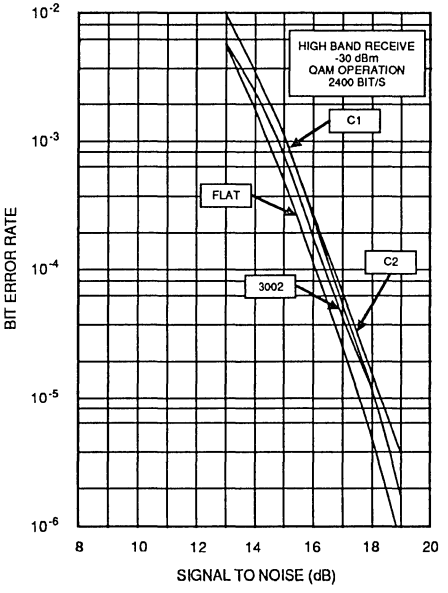
SSI 73K224L
BER vs. Signal to Noise

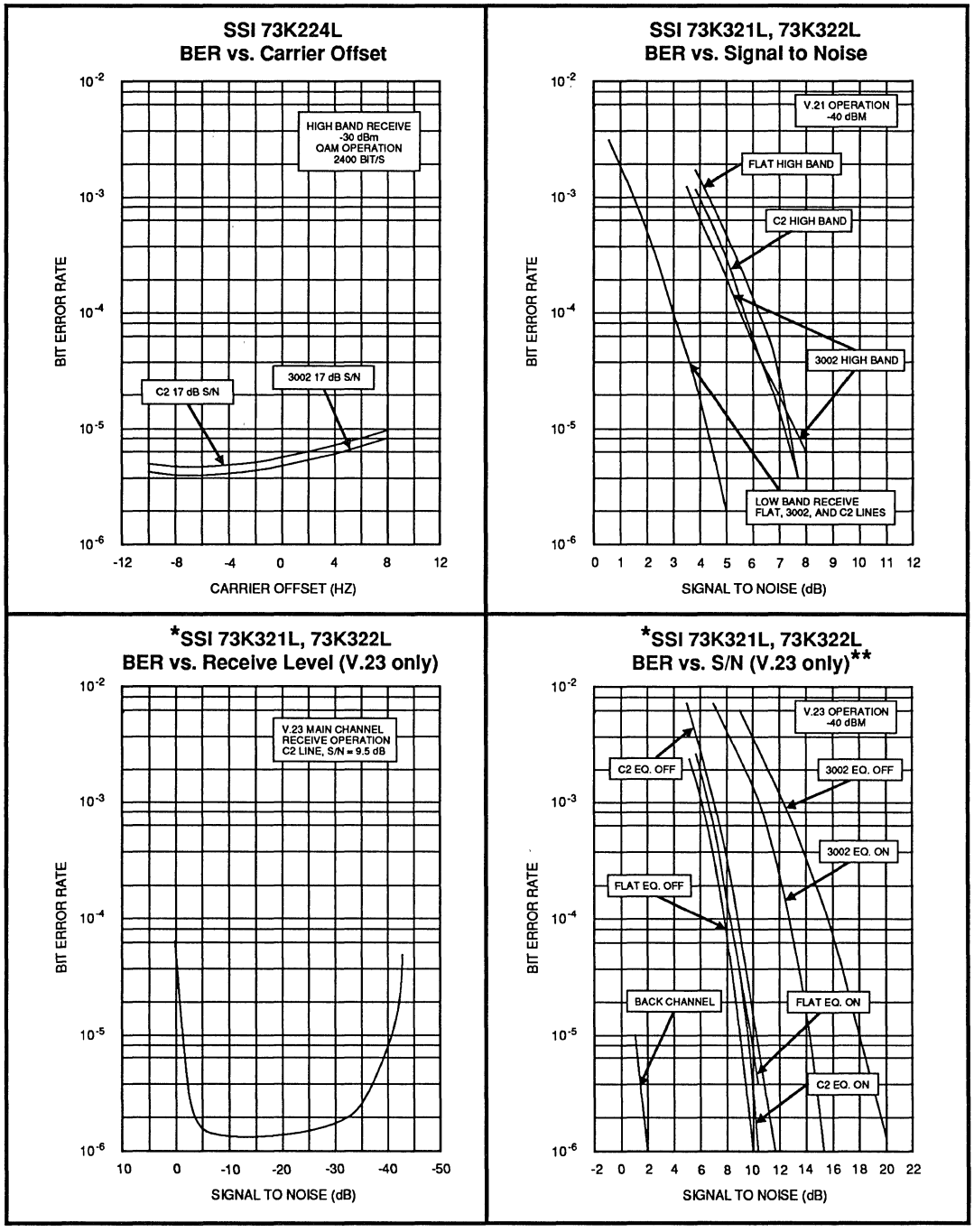


SSI 73K224L
BER vs. QAM-LOW



SSI 73K224L
BER vs. QAM-HIGH

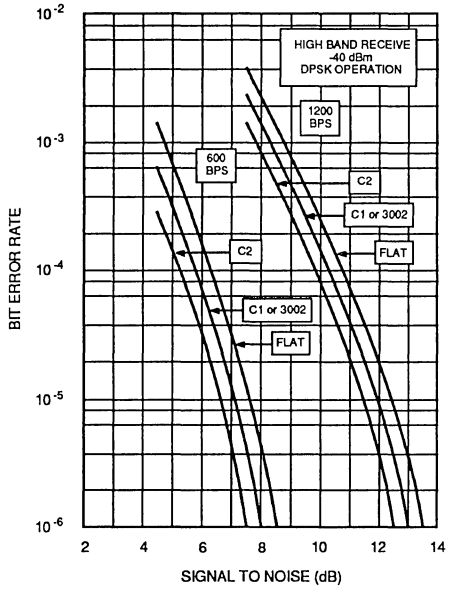




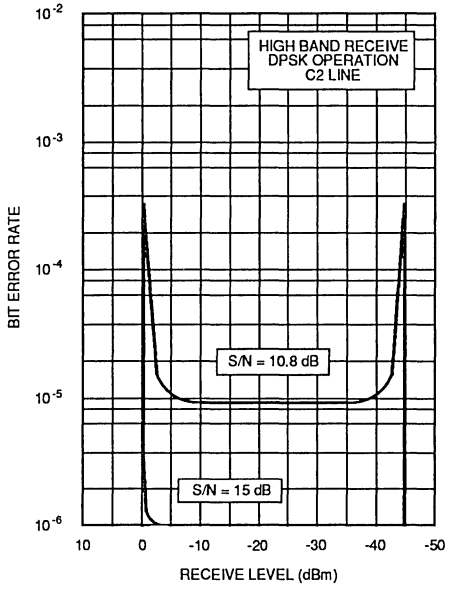
* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

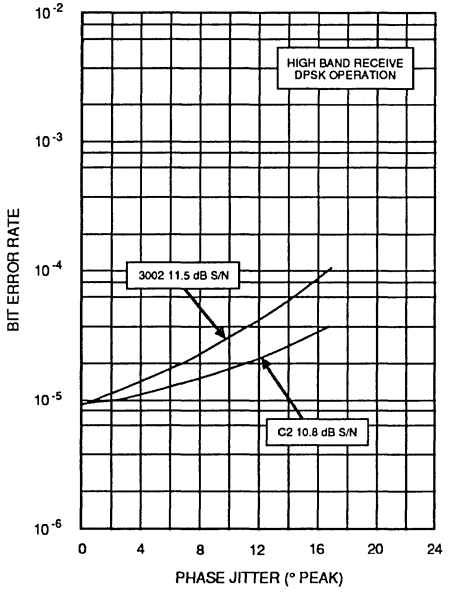
*SSI 73K322L BER vs. Signal to Noise



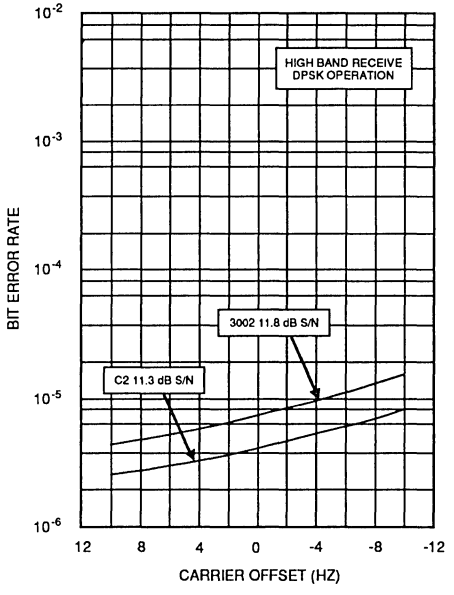
*SSI 73K322L BER vs. Receive Level



*SSI 73K322L BER vs. Phase Jitter



*SSI 73K322L BER vs. Carrier Offset



* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

silicon systems®

APPLICATION NOTE

Troubleshooting the Modem Design

Excerpt from the Silicon Systems ***K-Series Modem Design Manual***

Possible Causes of a Totally Dead System

It is always particularly depressing when you power-up a new design for the first time and absolutely nothing happens. However, this is often the easiest type of fault to find. We will try to think of a few things that could cause this problem (apart from the obvious, like the plug falling out of the wall socket).

The K-Series Modem IC is Stuck in the Reset State

You will generally get very little cooperation from a K–Series modem IC while it is in the power-down state. It enters this state when a reset operation is performed, either by writing to the Reset bit (bit 2) in Control Register 1 or by taking the RESET input pin to logic ONE. Make sure that your firmware is bringing the part out of this state by writing something other than all ZEROs to bits 5 to 2 in Control Register 0. Also, make sure that this happens after the RESET pin has been returned to logic ZERO. A capacitor from this pin to VDD can hold the part in the reset state for many seconds. Attempts to program the part during this time will not take effect. For products with a DSP, check that the RESET DSP bit (CR2 bit D2) is also written with ONE when appropriate.

Crystal Oscillator Fails to Start

If a complete crystal oscillator is used to directly drive the K-Series modem, any starting problem should be addressed to the manufacturer of that device. If the internal oscillator is used with a crystal, there may be situations in which it will not start. Check the values of the capacitors from XTL1 and XTL2 to ground. If these are too high in value, 40 pF or above, the oscillator may not start. Such large values are not recommended and should not be necessary if the crystal is correctly specified. Also ensure that the circuit board is designed to minimize stray inductance and capacitance in the area of the oscillator. The crystal and both capacitors should be placed as close as possible to the XTL pins of the K-Series modem IC and connected by direct traces. The ground connection of the capacitors should be via wide traces to the digital grounding system. It is also possible that the oscillator will not start or will be slow to start if the risetime of the power supply voltage is very long. The starting properties are helped by the asymmetry in the load capacitor values, the capacitor at XTL1 should be about twice as large as that at XTL2.

Clock to Microcontroller Isn't Getting Through

Using the K-Series modem ICs on-chip clock oscillator to generate timing for the entire system is very efficient from the point of view of component count and EMI generation. However, note that the CLK output of the modem chip is specified only to drive TTL compatible inputs. Many common microcontrollers require clock inputs that rise closer to the supply voltage for logic ONE. We have seen applications which use the CLK pin to drive these inputs without problem, however, the low-power (5V supply) parts may give a lower logic ONE level than is necessary at elevated temperature. We recommend that you use a TTL to CMOS level converting buffer between the CLK pin and the controller clock input in 5V systems. A pull-up resistor to the 5V supply is not effective in increasing the logic high voltage. In some cases capacitive coupling to a CMOS input is also effective if the controller clock input is properly biased.

Connect Handshake Fails

If your system seems to be working well but cannot get into the situation of exchanging data with another modem, it is likely that you have a problem in the connect handshake. It is better to examine handshake problems using a "known good" modem at the remote end rather than another of your own systems. This helps isolate problems if more than one are present. Use a modem from an established and reputable manufacturer, as discounted generic modems may not conform fully to established specifications. Depending on the modulation mode, there may be many or few opportunities to fail so we can only offer general pointers to problems we have encountered in the past. It is very helpful to build extra diagnostic code into the handshake to diagnose unexpected conditions.

If things never start, check that the initial set-up of the chip is correct. The chip must be taken out of power-down before it will do anything and in DSP-based chips the DSP must have been reset after any previous call and then taken out of the reset state. (A DSP–based part cannot be used in a non-DSP socket without many such changes to the controller code; watch this when upgrading a 73K222 system to use a 73K224L.) If in CALLINIT mode the answer tone is not detected, check that you have selected the desired answer tone frequency by programming in the Tone Register. The selectivity of the answer tone detector is quite high, so verify that your answering modem is generating a frequency within the specifications of the modulation standard. You should be able to verify the operation of your various signal detectors with breakpoints in the controller code. If these do not fire at the appropriate point, the handshake is likely to hang-up or get out of step with the other modem. Be especially careful with the S1 detector, if this is failing you may get connections at 1200 bit/s which were supposed to be at 2400 bit/s. With DSP-based chips in QAM or DPSK modes, make sure that you are enabling the adaptive equalizer at the appropriate time. Enabling it too early, when the received signal is unsuitable for training, and too late, when there is too little time left before the gear shift to 2400 bit/s, can both give connect problems. Finally, make sure the crystal oscillator frequency is in specification as a gross error here can cause failure of the handshake.

Errors Committed Immediately After Handshake, With Later Improvement

We have seen situations in which a K-Series modem makes many data errors during the first few seconds of a connection, but then shapes up and performs normally thereafter. This is generally due to some problem in equalizer training in a DSP-based chip. The equalizer must be held in the initial state (bit 0 of CR2 = ZERO) up to the point in the handshake when scrambled DPSK binary ONES first appear at the receiver. It must then be released promptly (bit 0 of CR2 = ONE) and allowed to adapt so that it is fully trained before the gear shift to 2400 bit/s and the transition to data mode occurs. Enabling the equalizer too early will cause it to train on an unsuitable unscrambled signal. Because it adapts more rapidly immediately after being enabled, it may take a long time to recover from a bad solution when the correct receiver signal arrives. Enabling the equalizer too late reduces the time available for training before the received data is relied upon to be correct. If you have to put the equalizer back into the initialized state after a period of training, make sure that Equalizer Enable (bit 0 of CR2) stays at ZERO for at least 2 ms. It is better to have the Receiver Gain Boost bit dealt with before the equalizer is enabled, otherwise transients caused by changing this bit may upset the equalizer solution.

Errors Experienced at High Receive Signal Levels

If the error rate gets worse at high receive signal levels, you should look for some source of clipping in the receive path. Injecting a signal of known level at the line coupling transformer and looking at the RXA pin with an oscilloscope should enable you to isolate any problem in the line interface. Look for excessive gain in the receiver buffer amplifier or other causes of clipping at this point such as badly chosen op-amps for single 5V supply operation. If the signal at RXA looks good and you are using a DSP-based modem chip, it is possible that the controller is incorrectly inserting the 12 dB receiver gain boost even if the Receive Level bit in the Detect Register is set. Note that early data sheets for the 73K224L gave this bit the wrong sense, i.e., ONE for low level. Only set Receive Gain Boost if this bit is ZERO.

Errors Experienced at Low Receive Signal Levels

There can be many causes of data errors at low receive signal levels, almost all associated with the presence of some level of interference or noise in the receive path. If you are performing tests over the telephone network, make sure that the error rate you are experiencing is not to be expected from the background noise level on the line. It is best to use a line simulator or a direct connection through an attenuator if looking for system noise problems. The capacitor across the feedback resistor of the receiver buffer amplifier is important to attenuate out-of-band noise at the modem chip receiver input.

Distortion in the telephone line interface can be located by injecting low-level signals into the line terminals and examining the signal at the RXA pin with a spectrum analyzer. Look for crossover distortion in the receiver buffer amplifier. This can arise from a poorly chosen op–amp type, such as the LM324 which makes a transition from class A to class AB operation at low signal levels and is not suitable for this application. We have found LM348 and LM1458 type op-amps to be free from this problem. It is also possible for the line coupling transformer to introduce harmonic distortion, particularly when a large D.C. holding current is flowing.

In the absence of significant distortion, look for a high noise level at the RXA pin. Another symptom of this problem, apart from data errors, is that the Carrier Detect bit (bit 3 in DR) comes on or blinks when no signal is applied to the modem receiver. The system may also fail to disconnect at the end of a call. If this is

your experience don't confine your search to the normal carrier bandwidth because the modem chip will also be susceptible to higher frequencies. Op-amps may be noisy or may self-oscillate at low level due to poor layout. If the op-amps themselves are not causing the noise, it may be due to poor circuit layout or grounding. If, finally, nothing suspicious is visible at the RXA pin then the noise must be getting into the receive signal inside the modem IC. This can be from the power supply and bias pins or from signals routed under the chip. Check the connections to GND, VDD, VREF and ISET pins for component values and placement and routing of decoupling components. You are more likely to have problems with supply noise if you are using a switching power supply. Look also for fast digital signals routed under the modem IC; these should be re–routed and a ground plane placed under the chip. Serious interference pickup problems can be created by two crystal oscillators producing beat frequencies in-band to the modem. We strongly recommend using one master crystal in the system. Check the gain in the receive path from the line terminals and, in DSP-based parts, the state of the Receive Gain Boost bit set by the controller. If either of these are incorrect, then noise in the chip will appear more significant compared to the signal.

The transmitter of the modem can be a source of noise in the receiver. It should not generate signals that are in–band to the receiver, but this can happen if either the buffer amplifier or the line transformer are causing harmonic distortion. This will be most noticeable in call mode, when the low band transmit signal has harmonics in the high band filter of the receiver. For 5V only systems, the choice of op-amps in the buffer amplifier and their D.C. bias point is crucial to obtaining a sufficient voltage swing without distortion. Because of its internal operation, a small amount of switching noise is present at the TXA pin. The capacitor across the buffer amplifier feedback resistor is important to prevent this signal from reaching the receiver. It is difficult to obtain good rejection of the transmit signal at the receiver for all practical line conditions, but you should check that your four-wire to two-wire hybrid circuit is operating correctly. For most terminations, the transmit signal at the RXA pin minus the receive buffer gain should be 6 dB below the level at the line.

Modem Works in Loopback but Fails to Connect or Makes Errors in Bursts with Some Other Modems

If anything appears "flaky" about the modem operation it is a good idea to check the oscillator frequency with a counter capable of resolving to at least ten parts per million. Using an oscilloscope is of no use whatsoever. Many systems that use crystal oscillators are not very particular about the exact frequency; this is not so of modems. Measure the frequency at the CLK pin and verify that it is between 11.0581 MHz and 11.0603 MHz. Do not measure at the XTL1 or XTL2 pins as the probe capacitance will alter the frequency of oscillation. Some causes of out–of–specification readings are: a) the wrong crystal frequency entirely, b) a series-resonant crystal, or c) a parallel-resonant crystal unmatched to the circuit capacitance.

Problems Unique to FSK Modes

The SSI 73K224L does not permit answer tone detection in FSK modes, so ensure that a mode other than FSK is selected before attempting to detect answer tones.

Section

MODEM PROTOCOL & BUS INTERFACE

2

SSI 73D2180
Bell 212A/103, CCITT V.22, V.21 Modem Device Set

July, 1990

2

DESCRIPTION

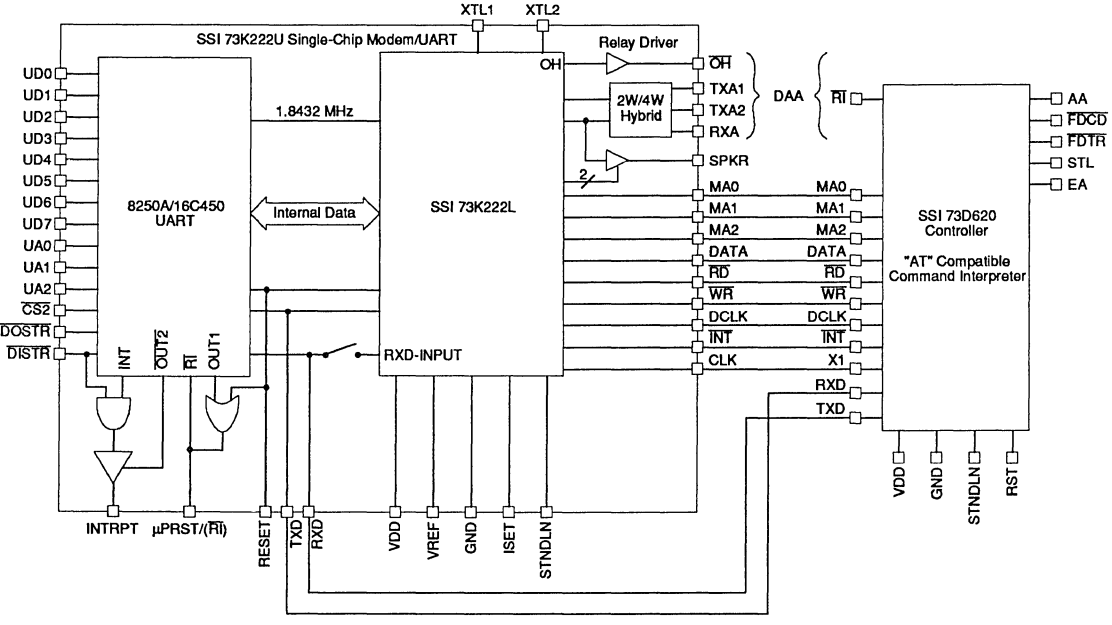
The SSI 73D2180 consists of two CMOS integrated circuits which provide the data pump functions and command interpretation required to construct a high performance 1200 bit/s full-duplex intelligent modem. The 73D2180 includes operating modes compatible with CCITT V.22, V.21, Bell 212A, and 103 data-communications standards. Using advanced processes that include analog and switched capacitor filter techniques, the SSI 73D2180 offers excellent performance and a high level of functional integration in a compact two-chip set. The 73D2180 provides a Hayes "AT" compatible command interpreter, a 16C450 compatible UART and an enhanced version of Silicon Systems' 73K222L single-chip modem.

The 73D2180 is ideal for use in integral system modem products where full-duplex 1200 bit/s data-communications over the 2-wire public service telephone network is desired.

FEATURES

- **Multi-mode CCITT V.22/V.21 & Bell 212A/103 compatible device set for intelligent modem designs**
- **Full duplex operation at 0-300 and 1200 bit/s**
- **Includes high-level "AT" command interpreter compatible with 1200 bit/s industry standard products**
- **Complete complement of "AT" modem features**
- **Selectable automatic speed detect, handshake and autobaud functions**
- **Dynamic range from 0 to -45dBm**
- **Call progress, carrier and answer tone detectors provide intelligent dialing functions**
- **DTMF and CCITT guard tone generators**
- **Test modes available - ALB, DL, RDL for complete test capability**
- **Space efficient 40-pin DIPs or 44-pin PLCCs**
- **Low power consumption (115 mW using +5V)**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

OPERATION

The SSI 73D2180 is a complete Bell 212A/103 and V.22/V.21 intelligent modem contained in two IC's. The device set forms the basis for a high performance integral modem product with self-contained command interpreter and a 16C450 compatible UART.

The 73D2180 chip set is composed of the SSI 73K222U single-chip modem/UART and the SSI 73D620 controller chip. The 73K222U is a single-chip modem integrated on the same die with a 16C450 compatible UART. The 73K222U interfaces with the main CPU via a parallel demultiplexed bus. Commands and data are passed to the chip set over this port and are serialized by the on-board UART. The 73D620 controller chip hosts an "AT" compatible command interpreter. This controller monitors the internal serial bus of the 73K222U (UART output) for user commands which it interprets and executes. The 73D620 controller communicates with the 73K222U modem/UART via a serial port. Refer to the block diagram on Page 1 and to the 73K222U Modem/UART Data Sheet for further details.

The SSI 73K222U provides the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guard tones. This device supports the V.22, V.21 and Bell 212A/103 operating modes.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the 73D2180 modulates the 1200 bit/s incoming data into dibits represented by four possible signal points as specified by CCITT recommendation V.22 and Bell 212A. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator reverses this procedure and recovers the data and data clock from the incoming signal.

FSK MODULATOR/DEMODULATOR

The FSK transmitter frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) or the V.21 standard frequencies of 980 and 1180 Hz (originate mark and space) and 1650 and 1850 Hz (answer mark and space) are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A bandsplit filter is included to shape the amplitude and phase response of the transmit signal to a square root 75% raised cosine and provide rejection of out-of-band signals in the receive channel.

AUTOMATIC HANDSHAKE

The SSI 73D2180 will automatically perform a complete handshake as defined by the CCITT V.22, V.21 and Bell 212A/103 standards to connect with a remote modem. The 73D2180 automatically determines the speed and operating mode and adjusts its operation to correspond to that of an originating modem when answering a call.

TEST MODES

The SSI 73D2180 allows use of Analog Loopback, Digital Loopback and Remote Digital Loopback test modes. Full test mode capability allows testing of the modem and interface functions from the local terminal using the appropriate control commands, or remotely using the RDL function.

"AT" COMMAND INTERPRETER

The SSI 73D620 controller includes an AT command interpreter which is compatible with the Hayes 1200 Smartmodem™ command set. Functions and features included with intelligent modems are provided by the 73D620 controller including auto-dial/auto-answer, handshake with auto-fallback, and selectable pulse or DTMF dialing sequences.

The 73D620 is also compatible with other SSI modem/UART family members and can be used interchangably with these products. Modes not available will be automatically disabled by the 73D620 controller in this case.

PIN DESCRIPTION - SSI 73D620 CONTROLLER

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V supply ±10%. Bypass with a 0.1 µF capacitor to ground.
GND	20	22	I	Digital ground
X1	19	21	I	11.0592 MHz clock input from the 73K222U.
RST	9	10	I	Reset Input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits power-on reset using a 0.1 µF capacitor to the 5V supply.
STNDLN	13	15	I	Stand alone. Tie low for proper operation as a command interpreter. Tie high to disable device.
EA	31	35	I	Tie to VDD.
AA	28	31	I	Auto Answer at power-up. Tie high to enable auto answer on power-up feature. Controller will automatically answer a ring as specified in the S11 register. Tie low to disable auto answer on power-up.
$\overline{\text{FDCD}}$	14	16	I	Force on data carrier detect. Tie low to permanently force on data carrier detect indication to controller. Tie high or leave floating to allow carrier detection from telephone line.
$\overline{\text{FDTR}}$	15	17	I	Force on data terminal ready. Tie low to permanently force on the data terminal ready indication to the controller. Tie high or leave floating to allow data terminal ready indication to be obtained from the 73K222U register.
STL	16	18	I	Switched telephone lines. Tie high or leave floating if operating with the public switched telephone network lines. Tie low if operating with leased lines.
$\overline{\text{RI}}$	17	19	I	Ring indication. Input to the controller from the telephone ring isolation circuit.

PIN DESCRIPTION - SSI 73D620 CONTROLLER (Continued)

MODEM INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	6-8	7-9	O	See SSI 73K222U pin description
DATA	1	2	I/O	See SSI 73K222U pin description
$\overline{RD}$	4	5	O	See SSI 73K222U pin description
$\overline{WR}$	5	6	O	See SSI 73K222U pin description
DCLK	2	3	O	See SSI 73K222U pin description
INT	12	14	O	See SSI 73K222U pin description
RXD	10	11	I	See SSI 73K222U pin description
TXD	11	13	I	See SSI 73K222U pin description

Note: Unused 73D620 controller pins are active, but not used for this application. These pins should be left floating.

PIN DESCRIPTION - SSI 73K222U

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V Supply ±10%, bypass with a 0.1 and a 22 µF capacitor to GND.
GND	20	22	I	Ground. Connect to analog ground.
VREF	19	21	O	VREF is an internally generated reference voltage which is externally bypassed by a 0.1 µF capacitor to the system ground.
ISET	9	11	I	The analog current is set by connecting this pin to VDD through a 2MΩ resistor. ISET should be bypassed to GND. Alternatively, an internal bias can be selected by connecting ISET to GND, which will result in a larger worst-case supply current due to the low tolerance of on-chip resistors. Bypass with .1µF capacitor if resistor is used.
XTL1, XTL2	25 24	27 26	I I	These pins are inputs for the internal crystal oscillator requiring an 11.0592 MHz crystal. XTL2 can also be driven from an external clock.
CLK	21	23	O	Output Clock. This pin provides an 11.0592 MHz clock to drive the 73D620 controller.

GENERAL (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
RESET	10	12	I	Reset. An active signal (high) on this pin will put the chip into an inactive state. The control register bits (except the Receiver Buffer, Transmitter Holding, and Divisor latches) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on reset using a 0.1µF capacitor connected to the 5V supply.
STNDLN	15	17	I	Tie low to enable the dual-port mode of the chip. This is required in order to operate properly with the 73D620.

UART INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
UA0-UA2	37-39	41-43	I	UART Address. These pins determine which of the UART registers is being selected during a read or write on the UART data bus. The contents of the DLAB bit in the UART's Line Control Register also control which register is referenced. See the SSI 73K222U data sheet.
UD0-UD7	27-34	30-37	I/O	UART Data. Data or control information to the UART registers is carried over these lines.
$\overline{\text{DISTR}}$	35	38	I	Data Input Strobe. A low on this pin requests a read of the internal UART registers. Data is output on the D0-D7 lines if $\overline{\text{DISTR}}$ and $\overline{\text{CS2}}$ are active.
$\overline{\text{DOSTR}}$	36	39	I	Data Output Strobe. A low on this pin requests a write of the internal UART registers. Data on the D0-D7 lines are latched on the rising edge of $\overline{\text{DOSTR}}$. Data is only written if both $\overline{\text{DOSTR}}$ and $\overline{\text{CS2}}$ are active.
$\overline{\text{CS2}}$	1	2	I	Chip Select. A low on this pin allows a read or write to the UART registers to occur.
INTRPT	5	7	O	UART Interrupt. This signal indicates that an interrupt condition from the UART has occurred. If the Enable 8250A interrupt bit in the interrupt Enable Register is 0 the interrupt is gated by the $\overline{\text{DISTR}}$ signal to provide compatibility with the 8250B. The output can be put in a high impedance state with the OUT2 register bit in the Modem Control Register. See the SSI 73K222U data sheet.

PIN DESCRIPTION - SSI 73K222U (Continued)

ANALOG / LINE INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
TXA1, TXA2	3 4	4 5	O O	Transmitted Analog (differential). These pins provide the analog output signals to be transmitted to the phone line. The drivers will differentially drive the impedance of the line transformer and the impedance matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal; in such a case, TXA2 should be left floating.
RXA	16	18	I	Received Analog. This pin inputs analog signals from the line transformer to the two-to-four wire hybrid. This input can also be taken directly from an external hybrid.
SPKR	17	19	O	Speaker Output. This pin outputs the received signal through a programmable attenuator stage, which controls volume or disables the speaker.
$\overline{OH}$	18	20	O	Off-hook relay driver. This signal is an open drain output capable of sinking 20mA and is used for controlling a hook relay.

MICROPROCESSOR INTERFACE (STNDLN = 0)

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	12-14	14-16	I	Modem Address Control. These lines carry register addresses for the modem registers and are valid throughout any read or write operation.
DATA	22	24	I/O	Serial Control Data. Serial control data to be read/written is clocked in/out on the falling edge of the DCLK pin. The direction of data transfer is controlled by the state of the $\overline{RD}$ pin. If the $\overline{RD}$ pin is active (low) the DATA line is an output. Conversely, if the $\overline{RD}$ pin is inactive (high) the DATA line is an input.
$\overline{RD}$	23	25	I	Read. A low on this input informs the SSI 73K222U that control data or status information is being read by the processor from a modem register.
$\overline{WR}$	26	28	I	Write. A low on this input informs the SSI 73K222U that control data or status information is available for writing into a modem register. The procedure for writing is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

MICROPROCESSOR INTERFACE (STNDLN = 0)

NAME	DIP	PLCC	TYPE	DESCRIPTION
DCLK	11	13	I	Data Clock. The falling edge of this clock is used to strobe control data for the modem registers in or out on the DATA pin. The procedure for a WRITE is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$. The falling edge of the $\overline{RD}$ signal must continue for eight cycles of DCLK in order to read all eight bits of the reference register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{INT}$	2	3	O	Modem Interrupt (with weak pull-up). This output signal is used to inform the 73D620 controller that a change in a modem detect flag has occurred. The controller then reads the Modem Detect Register to determine which detect triggered the interrupt. $\overline{INT}$ stays active until the controller reads the Modem Detect Register or does a full reset.
µPRST	8	10	O	Microprocessor Reset. This output signal is used to provide a hardware reset to the controller. This signal is high if the RESET pin is high or the MCR bit D3 (OUT1) bit is set. See the SSI 73K222U data sheet.
RXD	6	8	O	RXD outputs data received by modem from telephone line. This data is monitored by the 73D620 controller.
TXD	7	9	O	TXD is serial output of UART. This data is monitored by the 73D620 controller which checks for and executes the "AT" commands downloaded from the computer's CPU.

"AT" COMMANDS SUPPORTED
(Note: s=string; n=decimal, 0-255; x=Boolean, 0/1=false/true)

COMMAND	OPTIONS	DEFAULT
A/	Repeats last command line	N/A
A	Answer	N/A
Bx	BELL/CCITT = 1/0*	1
Ds	Dial string specified by s	No string
Ex	Command echo, 0/1 = off/on	1
Hn	Hook status, 0/1 = on/off	N/A
In	ID code, 0/1/2/3/4 (see Table 5)	N/A
Ln	Speaker volume, (0)1/2/3 = lo/med/hi	2
Mn	Speaker, 0/1/2/ = control (see Table 3)	1
On	Online, 0/1/2/ = on-line/on-line with remote digital loopback (see Table 4)	N/A
P	Pulse dial	Pulse
Qx	Quiet result, 0/1 = 1-quiet	0
R	Reverse originate	N/A
Sn=n	Set S register (see Table 2)	N/A
Sn?	Return value in register n (see Table 2)	N/A
T	Touch tone dial	Pulse
Vx	Verbose result, 0/1 = off/on	1
Xn	Result code, 0/1/2/3/4 (see Table 1)	4
Yx	Enable long space disconnect, 1 = enable	0
Z	Restore all default settings	N/A

*B0 command (CCITT mode) is operational only when using K-series modem/UARTs that include CCITT modes.

Dial string arguments:

, = delay	@ = silent answer	! = flash
; = return to command	W = wait for tone	R=reverse mode

TABLE 1: Result Codes

Xn	VOCAL/NUMERIC RESULT CODE
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6

TABLE 2: S Registers Supported

NUMBER	FUNCTION	UNITS	DEFAULT
S0	Answer on ring	No. of rings	000[1]
S1	Ring counter	No. of rings up to 8	000
S2	Escape code	ASCII CHR$( )	043
S3	Carriage return	ASCII CHR$( )	013
S4	Line feed	ASCII CHR$( )	010
S5	Back space	ASCII CHR$( )	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds	006
S10	Carrier drop out	100 milliseconds	007
S11	DTMF tone duration	1 millisecond	070
S12	Escape guard time	20 milliseconds	050
S13	Bit mapped register		N/A
S14	Bit mapped register	Decimal 0-255	Hex 6A
S15	Bit mapped register		N/A
S16	Test register	Decimal #	000

[1]Valid for AA pin tied low.

DIP SWITCH FUNCTIONS SUPPORTED
(DIP switches are only read on power-up.)

PIN	FUNCTION	SETTINGS (Suggested default underlined)
$\overline{\text{FDTR}}$	Force DTR on	Tie high or float: DTR signal controls modem
		Tie low: DTR always on
STL	Operate with switched telephone lines	Tie high or float: Switched telephone lines
		Tie low: Leased lines
$\overline{\text{FDCD}}$	Force DCD on	Tie high or float: RS-232 DCD line follows carrier
		Tie low: DCD line always on

TABLE 3: Speaker Modes

Mn	SPEAKER MODE
M0	Speaker off
M1	Speaker on during connect only
M2	Speaker on always

TABLE 4: O Modes

On	ONLINE/RETRAIN MODE
O0	Return online
O1	Return online
O2	Return online with remote digital loopback enabled

TABLE 5: ID Codes

In	CODE
I 0	Product code (139)
I 1	ROM checksum
I 2	Checksum test
I 3	Product revision
I 4	Software copyright

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

TA = 0°C to 70°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD +0.3	V

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD, Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		0		70	°C
External Component [3]					
VREF Bypass Capacitor [2]	(External to GND)	0.1			µF
Bias Setting Resistor [1]	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor [2]	ISET pin to GND	0.1			µF
VDD Bypass Capacitor [2]	(External to GND)	0.1			µF
Input Clock Variation	(11.0592 MHz)	-0.01		+0.01	%

Note 1: Optional for minimum worst case current consumption.

Note 2: Minimum for optimized system layout; may require higher values for noisy environments.

Note 3: Refer to application drawing for placement.

DC CHARACTERISTICS
TA = 0°C to +70°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
IDD, Supply Current						
73K222U IDDA, Active		ISET Resistor = 2 MΩ		8	12	mA
73K222U IDDA, Active		ISET = GND		8	15	mA
73K222U IDD1, Power-Down		CLK = 11.0592 MHz		3	4	mA
73K222U IDD2, Power-Down		CLK = 19.200 kHz		2	3	mA
73D620L IDDA, Active			11	15	19	mA
Digital Inputs						
Input High Current	IIH	VI = VDD			100	µA
Input Low Current	IIL	VI = 0	-200			µA
Input Low Voltage	VIL				0.8	V
Input High Voltage	VIH	Except RESET & XTL 1	2.0			V
Input High Voltage	VIH	RESET & XTL 1	3.0			V
Pull Down Current		RESET pin	5		30	µA
Input Capacitance					10	pF
Digital Outputs						
Output High Voltage	VOH	IOUT = - 1 mA	2.4		VDD	V
VOL UD0-UD7 and INTRPT		IOUT = 3.2 mA			.4	V
VOL other outputs		IOUT = 1.6 mA			.4	V
CLK Output	VOL	IOUT = 3.2 mA			0.6	V
OH Output	VOL	IOUT = 20 mA			1.0	V
OH Output	VOL	IOUT = 10 mA			0.5	V
Offstate Current INTRPT pin		VO = 0V	-20		20	µA
Analog Pins						
RXA Input Resistance				200		kΩ
RXA Input Capacitance					25	pF

DYNAMIC CHARACTERISTICS AND TIMING
TA = 0°C to +70°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	ANS TONE 2225 or 2100 Hz	-11	-10.0	-9	dBm0[1]
	DPSK TX Scrambled Marks	-11	-10.0	-9	dBm0
	FSK Dotting Pattern	-11	-10.0	-9	dBm0
FSK Tone Error	Bell 103 or V.21			±5	Hz
DTMF Generator					
Freq. Accuracy		-.25		.25	%
Output Amplitude	Low Band	-10	-9	-8	dBm0
Output Amplitude	High Band	-8	-7	-6	dBm0
Long Loop Detect	DPSK or FSK	-40		-32	dBm0
Demodulator Dynamic Range	DPSK or FSK		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600Hz Band	-39		0	dBm0
Reject Level	2-Tones in 350-600Hz Band			-46	dBm0
Delay Time	-70dBm0 to -30dBm0 Step	27		80	ms
Hold Time	-30dBm0 to -70dBm0 Step	27		80	ms
Hysteresis		2			dB
Carrier Detect	DPSK or FSK Receive				
Threshold	Data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	15		45	ms
Hysteresis		2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 Step	10		24	ms

Note 1: All units in dBm0 are measured at the line side to the transformer. The interface circuit inserts an 8dB loss in the transmit path (TXA1 - TXA2 to line), and a 3dB loss in the receive path (line to RXA).

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
Answer Tone Detector					
Detect Level Threshold	In FSK mode	-49.5		-42	dBm0
Delay Time	-70dBm0 to -30dBm0 STEP	20		45	ms
Hold Time	-30dBm0 to -70dBm0 STEP	10		30	ms
Detect Frequency Range		-2.5		+2.5	%
Hybrid Loading					
R1	See Figure 1		600		Ω
R2	Nominal telephone line load		600		Ω
C	TXA Hybrid Loading	.02		.033	µF
Speaker Output					
Gain Error		-1		+1	dB
Output Swing SPKR	10K||50pF LOAD 5% THD	2.75			VPP
Carrier VCO					
Capture Range	Originate or Answer	-10		10	Hz
Capture Time	-10Hz to +10Hz Carrier Frequency change assumed		40	100	ms
Recovered Clock					
Capture Range	% of Center Frequency	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin.		30	50	ms
Guard Tone Generator					
Tone Accuracy	550 or 1800Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	700 to 2900 Hz			-60	dB
Capacitance					
Inputs	All digital inputs			10	pF
XTL1, XTL2 load capacitors	Per crystal manufacturer's recommendations		30		pF
CLK	Maximum capacitive load			15	pF

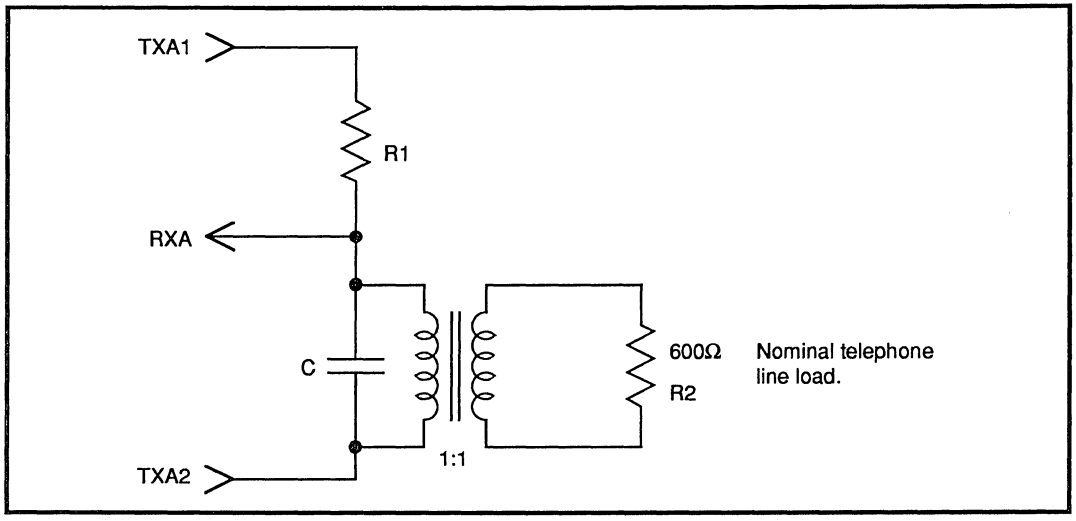


FIGURE 1: TXA Hybrid Loading Analog Interface Hybrid Loading

SERIAL BUS INTERFACE (See Figure 2)
The following times are for CL = 100pF.

PARAMETER		MIN	NOM	MAX	UNIT
TRD	Data out from Read	0		140	ns
TCKD	Data out after Clock			200	ns
TRDF	Data Float after Read	0		200	ns
TRCK	Clock High after Read	200			ns
TWW	Write Width	140		25000	ns
TDCK	Data Setup Before Clock	150			ns
TCKD	Data Hold after Clock	20			ns
TCKW	Write after Clock	150			ns
TACR	Address setup before Control[1]	50			ns
TCAR	Address Hold after Control [1]	50			ns
TACW	Address setup before Write	50			ns
TCAW	Address Hold after Write	50			ns

Note 1: Control is later of falling edge of RD or DCLK.

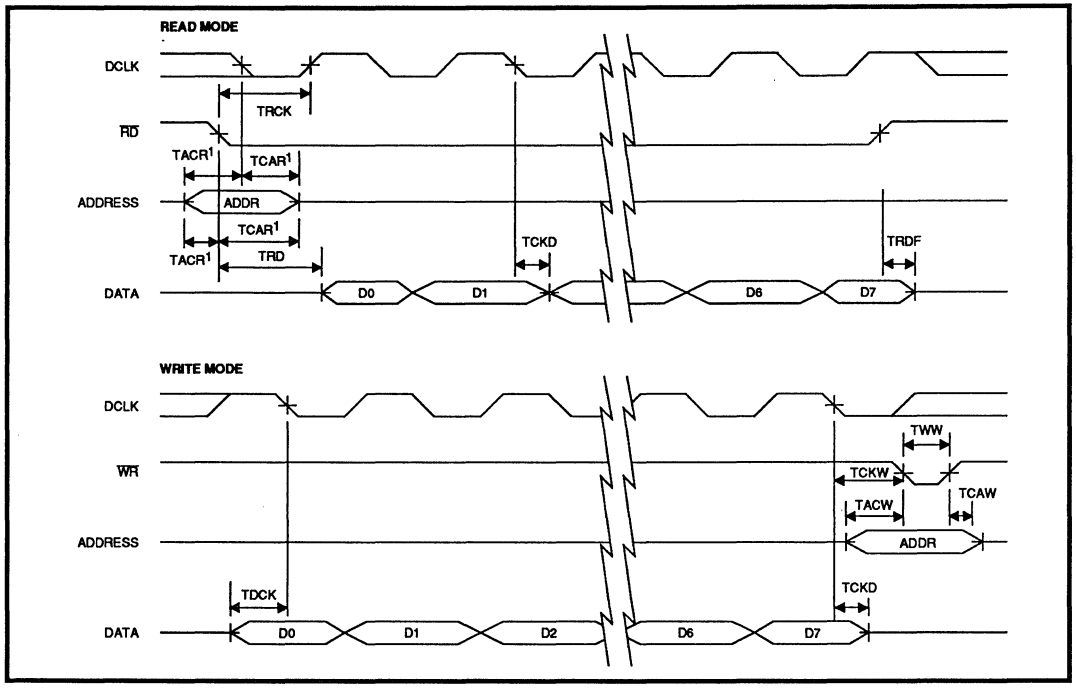


FIGURE 2: Modem Serial Bus Timing

PARALLEL BUS INTERFACE (See Figure 3) The following times are for Cl = 100pF.

PARAMETER		MIN	MAX	UNIT
RC	Read Cycle = TAD + TRC	240		ns
TDIW	DISTR Width	80		ns
TDDD	Delay DISTR to Data (read time)		80	ns
THZ	DISTR to Floating Data Delay	0	50	ns
TRA	Address Hold after DISTR	20		ns
TRCS	Chip select hold after DISTR	20		ns
TAR	DISTR Delay after Address	20		ns
TCSR	DISTR Delay after Chip Select	20		ns
WC	Write Cycle = TAW + TDOW + TWC	140		ns
TDOW	DOSTR Width	80		ns
TDS	Data Setup	30		ns
TDH	Data Hold	20		ns

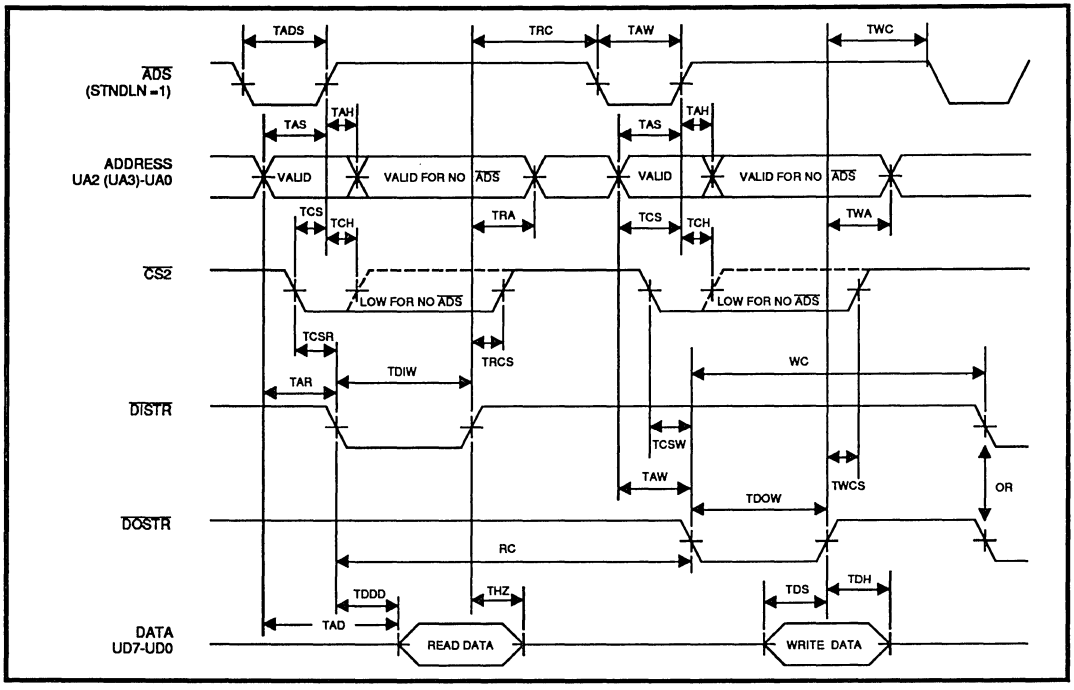


FIGURE 3: UART Bus Timing

PARALLEL BUS INTERFACE (Continued)

PARAMETER		MIN	MAX	UNIT
TWA	Address Hold after DOSTR	20		ns
TWCS	Chip select hold after DOSTR	20		ns
TAW	DOSTR delay after Address	20		ns
TCSW	DOSTR delay after Chip Select	20		ns
TADS	Address Strobe Width			ns
TAS	Address Setup Time			ns
TAH	Address Hold Time			ns
TCS	Chip Select Setup Time			ns
TCH	Chip Select Hold Time			ns
TRC	Read Cycle Delay	40		ns
TWC	Write Cycle Delay	40		ns
TAD	Address to Read Data	200		ns

TYPICAL PERFORMANCE CHARACTERISTICS

The SSI 73K222U was designed using an integrated analog/digital architecture that offers optimum performance over a wide range of line conditions. The SSI 73K222U utilizes the circuit design proven in SSI's 73K222L one-chip modem, with added enhancements which extend low signal level performance and increase immunity to spurious noise typically encountered in integral bus applications. The SSI 73K222U provides excellent immunity to the types of disturbances present with usage of the dial-up telephone network. The following curves show representative Bit Error Rate performance under various line conditions. (See Figures 4, 5 and 6 Performance Curves)

BER vs S/N

This test measures the ability of the modem to function with minimum errors when operating over noisy lines. Since some noise is generated by even the best dial-up lines, the modem must operate with as low a S/N ratio as possible. Optimum performance is shown by curves that are closest to the zero axis. A narrow spread between curves for the four line conditions indicates minimal variation in performance when operating over a range of line qualities and is typical of high performance adaptive equalization receivers. High band receive data is typically better than low band due to the inherent design of PSK modems.

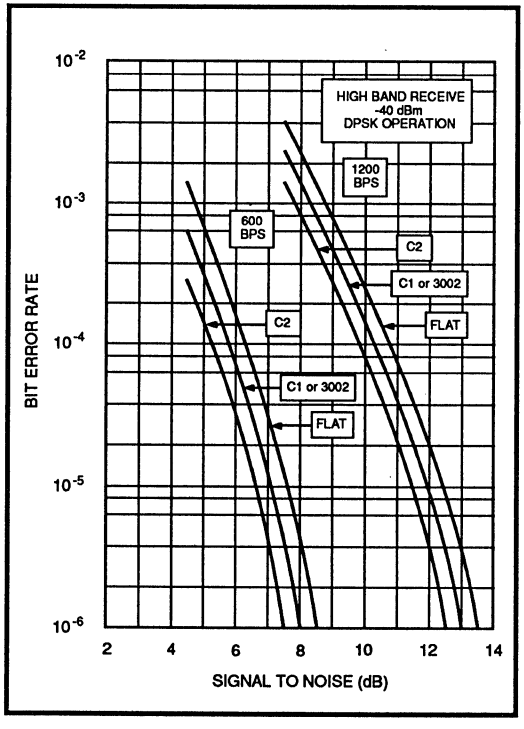


FIGURE 4: SSI 73K222U Typical BER vs. S/N

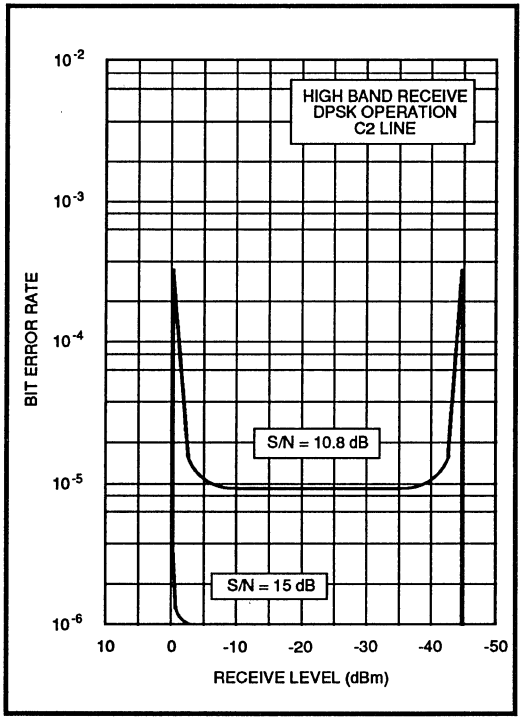


FIGURE 5: SSI 73K222U Typical BER vs. Receive Level

BER vs Receive Level

This measures the dynamic range of the modem. As signal levels vary widely over dial-up lines, the widest dynamic range possible is desirable. The minimum Bell specification calls for 36dB of dynamic range. S/N ratios were held constant at the indicated values while receive level was lowered from very high to very low signal levels. The "width of the bowl" of these curves taken at the 10^{-3} BER point is a measure of the dynamic range.

BER vs Carrier Offset

This parameter indicates how the modem performance is impacted by frequency shifts encountered in normal PSTN operation. Flat curves show no performance degradation from frequency offsets. The SSI K-Series devices use a 2nd order carrier tracking phase-locked-loop, which is insensitive to carrier offsets in excess of 10Hz. The Bell network specifications allow as much as 7Hz offset, and the CCITT specifications require modems to operate with 7Hz of offset.

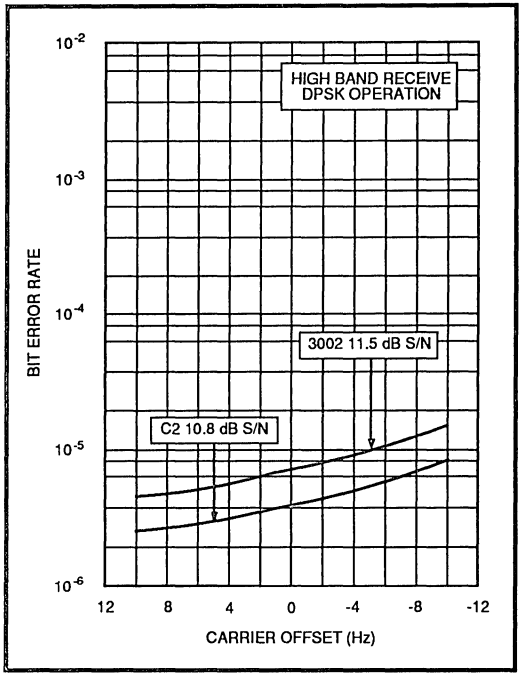


FIGURE 6: SSI 73K222U Typical BER vs. Carrier Offset

APPLICATIONS INFORMATION

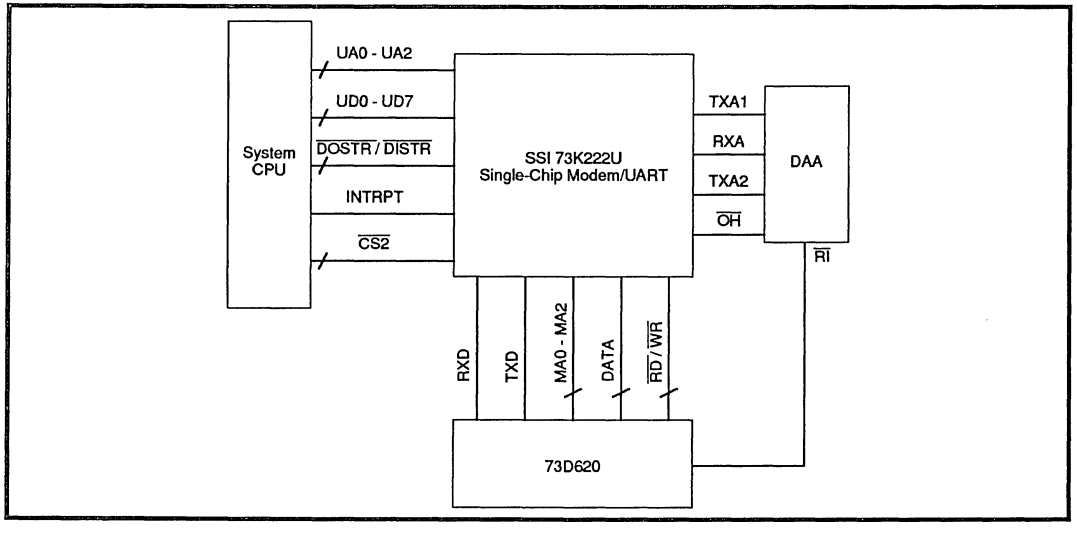


FIGURE 7: Typical Block Diagram for an Internal Modem Utilizing the SSI 73D2180 Chip-Set

APPLICATIONS INFORMATION (Continued)

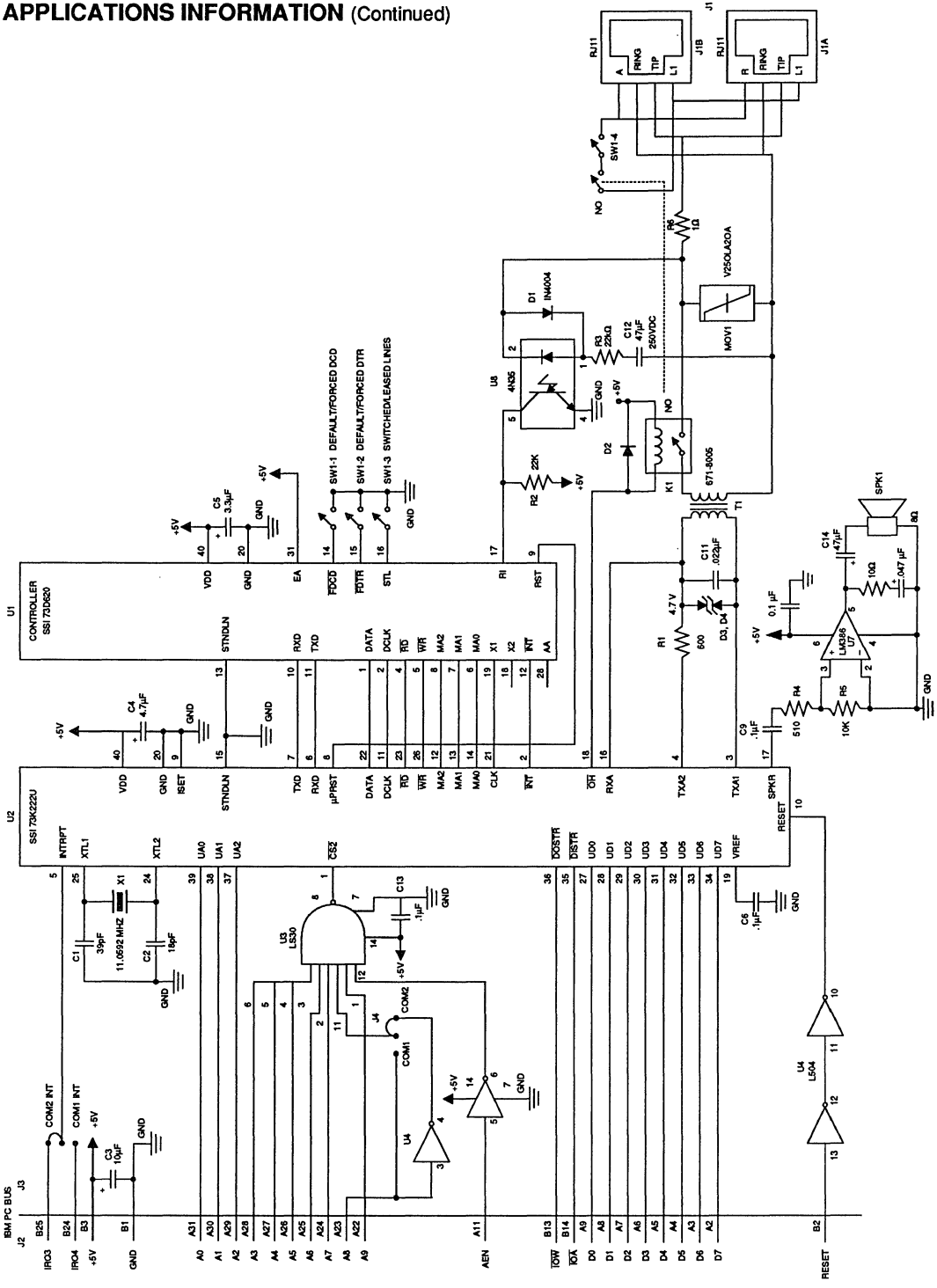
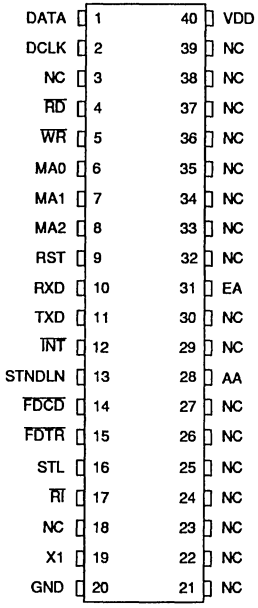
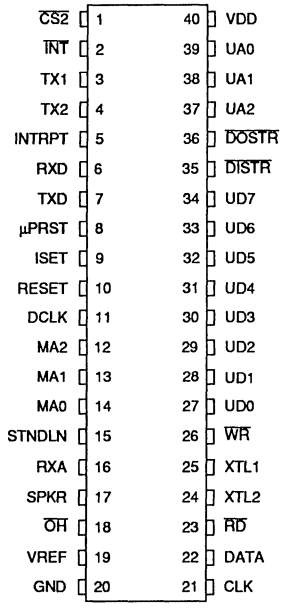


FIGURE 8: Typical Internal Modem Schematic Using the SSI 73D2180 Chip-Set

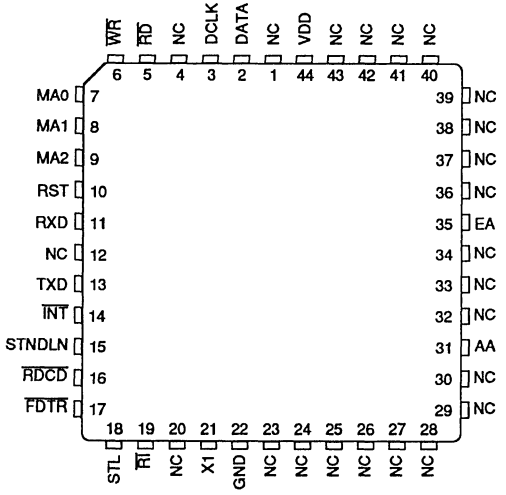
PACKAGE PIN DESIGNATIONS



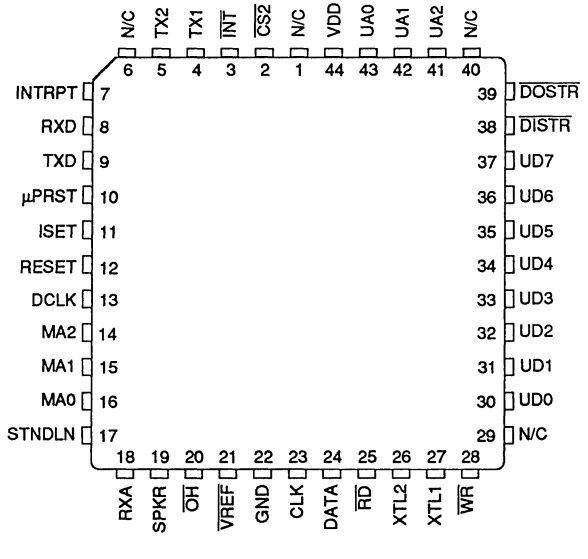
SSI 73D620 40-pin DIP



SSI 73K222U 40-pin DIP



SSI 73D620 44-pin PLCC



SSI 73K222U 44-pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73D2180 Chip-set Two 40-pin DIP packages	SSI 73D2180L-CP	73K222U-IP 73D620L-CP
SSI 73D2180 Chip-set Two 44-pin PLCC packages	SSI 73D2180L-CH	73K222U-IH 73D620L-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

SSI 73D2240
V.22bis 2400 Bit/s Modem Device Set
Advance Information

July, 1990

2

DESCRIPTION

The SSI 73D2240 is a set of two ICs that provide the data pump functions needed to design a high-performance, low-power 2400 bit/s intelligent modem for use in dial-up telephone network applications. The 73D2240 consists of the SSI 73K224L 1-chip multi-mode modem along with the SSI 73D600, a companion supervisory controller that provides a complete "AT" command and feature set compatible with industry standard products.

The 73D2240 includes operating modes compatible with CCITT V.22bis, V.22, and V.21, as well as Bell 212A and 103 data communications standards. Using advanced CMOS processes that integrate analog, digital signal processing and switched capacitor filter functions on the same chip, the SSI 73D2240 offers excellent performance, full modem features and the lowest power consumption available in a compact 2-chip set.

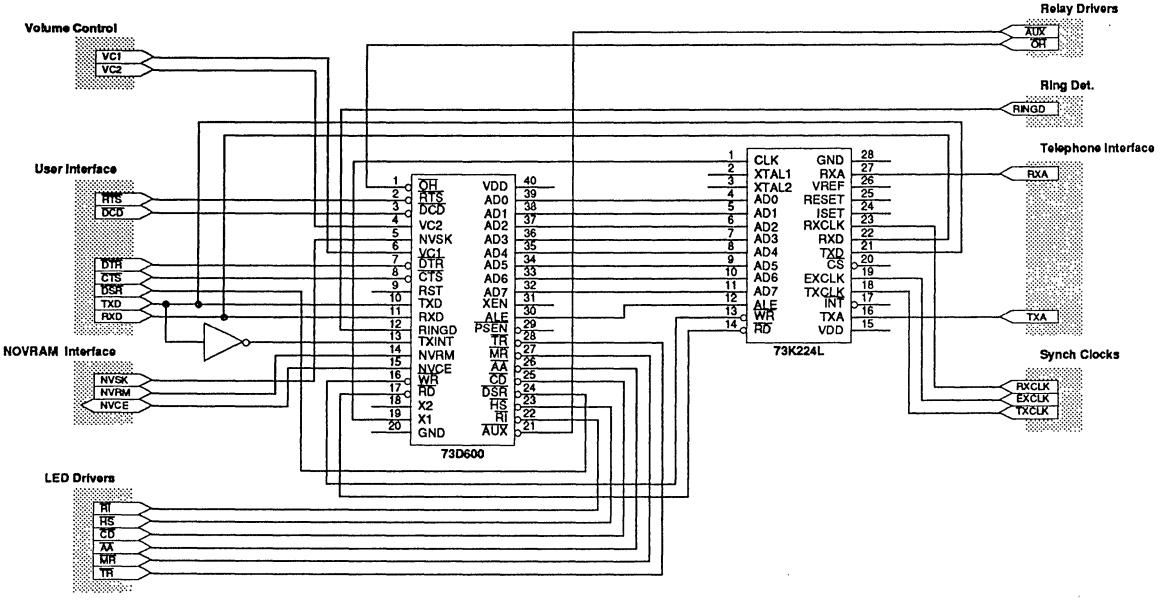
(Continued)

FEATURES

- **Multi-mode V.22bis/V.22/V.21 & Bell 212A/103 compatible device set for intelligent modem designs**
- **Full duplex operation at 0-300, 1200 and 2400 bit/s with all synch & asynch operating modes**
- **Includes high-level "AT" command interpreter compatible with 2400 bit/s industry standard products**
- **73K600 Controller Compatible with other K-series products**
- **Complete complement of "AT" modem features**
- **Selectable automatic speed detect, handshake and autobaud functions**
- **Supports external non-volatile memory to store user configurations**
- **Adaptive equalization for optimum performance over all lines**
- **Dynamic range from -3 to -45 dBm**

(Continued)

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The 73D2240 can be used in free-standing and integral modem designs where full-duplex 2400 bit/s operation is required. Single 5V supply operation with extremely low power draw make it ideal for battery powered terminals, lap-top PCs and other power sensitive applications.

FEATURES (Continued)

- **Call progress, carrier and answer tone detectors provide intelligent dialing functions**
- **DTMF and CCITT guard tone generators**
- **Test modes available - ALB, DL, RDL for complete test capability**
- **Space efficient 28- and 40-pin DIPs**
- **All CMOS technology for low power consumption (< 600mW using ±5V)**

OPERATION

The SSI 73D2240 is a complete V.22bis intelligent modem contained in two CMOS ICs. The device set forms the basis for a high performance stand-alone modem product with self-contained command interpreter, indicator LEDs, and interface lines for an RS-232 serial port. Both data and commands are passed over the serial port as in conventional intelligent modem designs.

The SSI 73D2240 provides the QAM, PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guard tones. This device supports the V.22bis, V.22, V.21 and Bell 212A/103 operating modes, both synchronous and asynchronous. The 73D2240 is designed to provide functions needed for an intelligent modem and includes auto-dial/auto-answer, handshake with auto-fallback, and selectable pulse or DTMF dialing sequences to simplify these designs.

The SSI 73D2240 consists of two devices. The SSI 73K224L is an analog processor and DSP that perform the filtering, timing adjustment, level detection and modulation/demodulation functions. The SSI 73D600 is a command processor that provides supervisory control and command interpretation. The SSI 73D600 is also compatible with the SSI 73K212, 221 and 222 K–series modem ICs.

QAM MODULATOR/DEMODULATOR

The SSI 73D2240 scrambles and encodes the 2400 bit/s incoming data into quad bits represented by 16 possible signal points as specified by CCITT recommendation V.22 bis. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator reverses this procedure and recovers a data clock from the incoming signal. Adaptive equalization corrects for different line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the 73D2240 modulates the 1200 bit/s incoming data using a subset of the QAM signal points as specified by CCITT recommendation V.22bis, V.22 and Bell 212A. The DPSK demodulator is similar to the QAM demodulator.

FSK MODULATOR/DEMODULATOR

The FSK transmitter frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) or the V.21 standard frequencies of 980 and 1180 Hz (originate mark and space) and 1650 and 1850 Hz (answer mark and space) are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A bandsplit filter is included to shape the amplitude and phase response of the transmit signal to a square root 75% raised cosine and provide rejection of out-of-band signals in the receive channel.

ASYNCHRONOUS MODES

The character asynchronous modes are used for communication between asynchronous terminals which may vary the data rate from +1.5% to -2.3%. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to

output the data within 0.01%. The signal is routed to a data scrambler (following the CCITT V.22bis algorithm) and into the modulator. The 73D2240 recognizes a break signal and handles it in accordance with specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits. An incoming break signal will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODES

Synchronous operation is possible only with the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. External synchronous mode is provided for a user supplied clock accurate to ±0.01%. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data at the RXD output is clocked out on the rising edge of RXCLK. The async/synch converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as is input. The RXCLK, TXCLK and EXCLK are for synchronous modes only.

AUTOMATIC HANDSHAKE

The SSI 73D2240 will automatically perform a complete handshake as defined by the V.22bis, V.22 and Bell 212A/103 standards to connect with a remote modem. The 73D2240 automatically determines the speed and operating mode and adjusts its operation to correspond to that of an answering modem when originating a call.

TEST MODES

The SSI 73D2240 allows use of Analog Loopback, Digital Loopback and Remote Digital Loopback test modes. Full test mode capability allows testing of the modem and interface functions from the local terminal using the appropriate control commands, or remotely using the RDL function.

ADAPTIVE EQUALIZATION WITH AUTO-RETRAIN

The SSI 73D2240 uses adaptive equalization which automatically compensates for varying line characteristics by adjusting taps on a multi-tap FIR filter. Optimum performance is obtained with this technique over a wide range of line conditions. When the line quality deteriorates to a specified level the 73D2240 can automatically initiate a retrain of the equalizer to reestablish data communications without the need to go through a complete handshake sequence.

"AT" COMMAND INTERPRETER

The SSI 73D2240 includes an AT command interpreter which is compatible with the Hayes 2400 Smartmodem™ command set. Functions and features included with intelligent modems are provided by the 73D2240 command interpreter. The 73D600 controller may also be used with the 73K212, K221, and K222. It will function with these parts in the modes supported by the device. It will still support the Hayes Smartmodem™ 2400 commands even though operation at 2400 bit/s will not be permitted. The controller reads the device signature of the modem IC installed to determine which modes should be allowed.

NON-VOLATILE MEMORY

The SSI 73D2240 supports connection to an external non-volatile memory (National 9346 or equivalent) to store dial strings and the current AT command configuration. If NOVRAM is not present, the factory default configuration is automatically used, but dial string storage is not permitted.

SPEED/PROTOCOL COMPATIBILITY GUIDE

Calling a:			73D2240 originating as:				
			Bell		CCITT		
			300	1200	300	1200	2400
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400[1]	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22bis)	300	1200	-	1200	2400
Called from a:			**73D2240 answering as:**				
			Bell		**CCITT**		
			300	**1200**	**300**	**1200**	**2400**
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22bis)	300	1200	-	1200	2400

[1] A Bell 2400 is a V.22bis using a 2225 Hz answer tone without unscrambled marks.

"AT" COMMANDS SUPPORTED
(Note: s=string; n=decimal, 0-255; x=Boolean, 0/1=false/true)

COMMAND	OPTIONS	DEFAULT
A/	Repeats last command line	N/A
A	Answer	N/A
Bx	BELL/CCITT = 1/0 answer tone @1200 (N/A @2400)	1
DS = n	Dial string specified by n, n = 0-3	n = 0
Ex	Command echo, 0/1 = off/on	1
Hn	Hook status, 0/1 = on/off	N/A
In	ID code, 0/1/2 (see Table 8)	N/A
Ln	Speaker volume, (0)1/2/3 = lo/med/hi	2
Mn	Speaker, 0/1/2/3 = control (see Table 3)	1
On	Online, 0/1/2/3 = online/retrain/no retrain (see Table 4)	N/A
P	Pulse dial	Pulse
Qx	Quiet result, 0/1 = 1-quiet	0
R	Reverse originate	N/A
Sn=n	Set S register (see Table 2)	N/A
Sn?	Return value in register n (see Table 2)	N/A
T	Touch tone dial	Pulse
Vx	Verbose result, 0/1 = off/on	1
Xn	Result code, 0/1/2/3/4 (see Table 1)	4
Yx	Enable long space disconnect, 1 = enable	0
Zx	Restore from Non-Volatile Memory, x = 0 or 1	N/A
&Cx	Carrier detect override, 0/1 = on/normal	0
&Dn	DTR mode, 0/1/2/3 (see Table 5)	0
&F	Restore to factory configuration	N/A
&Gn	CCITT guard tone, 0/1/2 = off/1800/550	0
&Jx	Auxiliary relay control	0
&Mn	Async/Sync mode, 0/1/2/3 (see Table 6)	0

"AT" COMMANDS SUPPORTED (Continued)

COMMAND	OPTIONS	DEFAULT
&Px	Pulse dial mode, 0/1=U.S./U.K.	0
&Qx	Same as &M	N/A
&Rx	Enable RTS/CTS	0
&Sx	DSR override, 0/1=U.S./U.K.	0
&Tn	Test mode (see Table 7)	N/A
&V	View active configuration and user profiles	N/A
&Wx	Write current configuration to NVRAM x = 0 or 1	0
&Xn	Sync Tx clock mode, 0/1/2=int/ext/slave	0
&Yx	Designate default user profile Z0 or Z1	N/A
&Zn = s	Store a telephone number n = 0-3	N/A

Factory configuration[1]:
B1 E1 F1 L2 M1 P Q0 V1 X4 Y0 &C0 &D0 &G0 &J0 &M0 &P0 &R0 &S0 &T4 &X0

Dial string arguments:
, = delay @ = silent answer ! = flash
; = return to command s = dial stored number W = wait for tone R=reverse mode

TABLE 1: Result Codes

Xn	VOCAL/NUMERIC RESULT CODE
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6

TABLE 2: S Registers Supported

Sn	FUNCTION	UNITS	DEFAULT
S0[2]	Answer on ring	No. of rings	000
S1	Ring counter	No. of rings up to 8	000
S2	Escape code	ASCII CHR$( )	043
S3	Carriage return	ASCII CHR$( )	013

[1] If the NOVRAM has not been initialized it may be necessary to Power down/Power up and type AT&F&W<cr> to properly initialize modem state.
[2] Stored in NVRAM with &W command

TABLE 2: S Registers Supported (Continued)

NUMBER	FUNCTION	UNITS	DEFAULT
S4	Line feed	ASCII CHR$( )	010
S5	Back space	ASCII CHR$( )	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds	006
S10	Carrier drop out	100 milliseconds	014
S11	DTMF tone duration	1 millisecond	070
S12	Escape guard time	20 milliseconds	050
S13	Unused		N/A
*S14[2]	Bit mapped register	Decimal 0-255	170
S15	Unused		N/A
S16	Test register	Decimal #	000
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[2]	Bit mapped register	Decimal 0-255	000
*S22[2]	Bit mapped register	Decimal 0-255	118
*S23[2]	Bit mapped register	Decimal 0-255	007
S24	Unused		N/A
S25[2]	DTR delay	10 milliseconds	005
S26[2]	CTS delay	10 milliseconds	001
*S27[2]	Bit mapped register	Decimal 0-255	064

* The bit mapped register functions are equivalent to normal "AT" command modem registers. They are not needed for evaluation of the 73D2240 capabilities.

Asynchronous character formats supported:
[Number of data bits, parity (even/odd/none), number of stop bits]

1200/2400 bit/s: 7N2, 7E1, 7O1, 8N1

300 bit/s: 7N2, 7E1, 7O1, 8N1

[2] Stored in NVRAM with &W command

TABLE 3: Speaker Modes

Mn	SPEAKER MODE
M0	Speaker off
M1	Speaker on during connect only
M2	Speaker on always
M3	Speaker on during call progress

TABLE 4: O Modes

On	ONLINE/RETRAIN MODE
O0	Return online
O1	Return online with retrain
O2	Enable automatic retrain (default)
O3	Disable automatic retrain

TABLE 5: DTR Modes

&Dn	DTR MODE
&D0	Ignore DTR
&D1	Go to command state if ON to OFF detected
&D2	Go to command state and disable auto-answer if ON to OFF detected
&D3	Initialize modem with NVRAM if ON to OFF detected

TABLE 6: Synchronous Modes

&Mn	SYNCHRONOUS MODE
&M0	Asynchronous
&M1	Sync mode entered upon completion of connect sequence
&M2	Dial stored number on OFF to ON transition of DTR and go online
&M3	Manual dial using DTR as talk data switch

TABLE 7: Test Modes

&Tn	TEST MODE
&T0	End/Abort test
&T1	Initiate local analog loopback (L3)
&T3	Initiate local digital loopback
&T4	Permit remote digital loopback (L2)
&T5	Prohibit remote digital loopback
&T6	Initiate remote digital loopback (L2)
&T7	Initiate RDL with self-test and error detector
&T8	Initiate ALB with self-test and error detector

TABLE 8: ID Codes

In	CODE
I 0	Product code (249)
I 1	ROM checksum
I 2	Checksum test
I 3	Product revision
I 4	Software copyright

HARDWARE INTERFACE

POWER SUPPLIES AND CLOCKS

LABEL	I/O	PIN CONNECTION		DESCRIPTION
		73M224L	73D600	
VDD	I	15	40	Positive supply (+5V)
VDD	I	28		System ground
GND	I	28		Digital ground
X1	I		19	Clock input 11.0592 MHz
CLK	O	18		Clock output 11.0592 MHz
RST	I	25	9	Reset (10 µF & 8.2k)

DAA INTERFACE

RxA	I	27		Receive analog from DAA
TxA	O	16		Transmit analog to DAA
VC1	O		6	Audio volume control
VC2	O		4	Audio volume control
RINGD	I		12	From ring indicator
$\overline{OH}$	O		1	Off hook relay control
$\overline{AUX}$	O		21	Auxiliary relay control

RS-232/V.24 INTERFACE

$\overline{RI}$	O		22	Ring indicator output
$\overline{HS}$	O		23	Indicates high speed
TXD	I	21	10	Digital data from terminal
RXD	O	22	11	Digital receive data
$\overline{DCD}$	O		3	Data carrier detect
$\overline{DSR}$	O		24	Data set ready
EXCLK	I	19		External Tx sync clock input
RXCLK	O	23		Receive clock ouptut
TXCLK	O	18		Transmit clock output
$\overline{CTS}$	O		8	Clear to send
$\overline{RTS}$	I		2	Request to send
$\overline{DTR}$	I		7	Indicates DTE available

HARDWARE INTERFACE (Continued)

LED DISPLAY SIGNAL SOURCE

LABEL	I/O	PIN CONNECTION 73D600	DESCRIPTION
TR	LED	28	Data terminal ready (Active Low)
SD	LED	11	Transmit data (Mark = High)
RD	LED	10	Receive data (Mark = High)
CD	LED	25	Data carrier detect (Active Low)
HS	LED	23	High speed indicator (Active Low)
MR	LED	27	Modem ready/test in progress (Active Low)
AA	LED	26	Auto answer indicator (Active Low)
OH	LED	1	Off hook indicator (Active Low)

NVRAM INTERFACE 73D600

NVCE	O	15	NVCE
NVRM	I/O	14	NVRM
NVSK	I	5	NVSK

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
VDD Supply Voltage	73K224L	14	V
	73D600	7	V
Storage Temperature		-65 to 150	°C
Soldering Temperature (10 sec.)		260	°C
Applied Voltage		-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.			

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(VDD to GND)	0.1			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF

RECOMMENDED OPERATING CONDITIONS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Components - 73D600					
VDD Bypass Capacitor	VDD to GND	1			µF
XTL1, 2 Load Capacitors	Typical, depends on crystal	15		40	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		70	°C

DC ELECTRICAL CHARACTERISTICS

*(TA = -40°C to 70°C, VDD =recommended range unless otherwise noted.)

VDD Supply Voltage					
73D600, 73K224L		4.5	5	5.5	V
IDD, Supply Current	**CLK = 11.0592 MHz**				
73K224L	ISET Resistor = 2 MΩ				
IDD1, Active			25	27	mA
IDD2, Idle	CLK = 11.0592 MHz		3		mA
73K600					
IDD1, Active				16	mA
IDD2, Idle				3.7	mA
Digital Inputs 73K224L					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VIH MAX			100	µA
IIL, Input Low Current	VI = VIL MIN	-200			µA
Reset Pull-down Current	Reset = VDD	5		50	µA
Digital Outputs 73K224L					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
VOL, CLK Output	IOUT = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-5		-50	µA
Capacitance 73K224L					
Inputs	Input capacitance, all Digital Input pins			10	pF
CLK	Maximum Capacitive Load			15	pF

* Although marked as a commercial temperature range part (0-70°C) the 73K224L operates to -40°C as with industrial temperature range rated devices.

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Digital Inputs 73K600					
VIL, Input Low Voltage		0		.2VDD-.1	V
VIH, Input High Voltage					
Reset, X1		.7 VDD		VDD	V
All Other Pins		.2 VDD +.9		VDD	V
IIL, Low Input Current	Vin = 0.45 V			-50	µA
ITL, Logic 1 to 0 Transition Current	Vin = 2.0V			-500	µA
Digital Outputs 73K600					
VOH Output High Voltage					
All Ports Except ALE, AD0-7	IOH = -80 µA	2.4			V
AD0-7, ALE	IOH = -400 µA	2.4			
VOL Output Low Voltage					
All Ports Except ALE, AD0-7	IOL = 1.6 µA			0.45	V
AD0-7, ALE	IOL = 3.2 µA			0.45	V
Reset Pull Down Resistor		40		125	kΩ

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +70°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11.5	-10.0	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.31		+0.05	%
Transmit Level	Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
Output Distortion	All products through BPF			-45	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD	-5		+5	%
2100 Hz Answer Tone Generator					
Output Amplitude		-11.5	-10	-9	dBm0
Output Distortion	All products though BPF			-40	dB

NOTE: Parameters expressed in dBm0 refer to the following definition:
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.
Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
DTMF Generator						
Freq. Accuracy			-0.25		+0.25	%
Output Amplitude			-10		-8	dBm0
Output Amplitude			-8		-6	dBm0
Twist		High-Band to Low-Band	1.0	2.0	3.0	dB
Receiver Dynamic Range		Refer to Performance Curves	-48		-3	dBm0
Call Progress Detector		In Call Init mode				
Detect Level		460 Hz test signal	-34		0	dBm0
Reject Level					-40	dBm0
Delay Time		-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time		-30 dBm0 to -70 dBm0 STEP			25	ms
Hysteresis			2			dB
Carrier Detect						
Threshold		QAM/DPSK or FSK receive data	-48		-43	dBm0
Hysteresis		All Modes	2			dB
Delay Time	DPSK	-70 dBm0 to -6 dBm0	15	20	25	ms
		-70 dBm0 to -40 dBm0	15	20	25	ms
	QAM	-70 dBm0 to -60 dBm0	25	30	35	ms
		-70 dBm0 to -40 dBm0	25	33	41	ms
Hold Time	DPSK	-6 dBm0 to -70 dBm0	15	22	28	ms
		-40 dBm0 to -70 dBm0	10	15	20	ms
	QAM	-6 dBm0 to -70 dBm0	44	50	56	ms
		-40 dBm0 to -70 dBm0	21	26	31	ms
Answer Tone Detectors		Call Init Mode				
Detect Level			-48		-43	dBm0
Detect Time		For signals from	7		37	ms
Hold Time		-6 to -40 dBm0, 2100 or 2225 Hz	10		48	ms
Detect Time		Demod Mode for signals from	4		26	ms
Hold Time		-6 to -40 dBm0, 2100 or 2225 Hz	11		43	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Pattern Detectors	DPSK Mode				
S1 Pattern					
Delay Time	For signals from -6 to -40 dBm0,	15		32	ms
Hold Time	Demod Mode	4		21	ms
Unscrambled Mark					
Delay Time	For signals from -6 to -40,	16		38	ms
Hold Time	Demod or call Init Mode	13		47	ms
Receive Level Indicator					
Detect On				-20	dBm0
Valid after Carrier Detect		10			ms
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 dB in 0.3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy	4 kHz, Guard Tones off			-35	dBm0
	10 kHz, Guard Tones off			-60	dBm0
	12 kHz, Guard Tones off			-70	dBm0
Anti Alias Low Pass Filter	(Frequency kHz)				
Out of Band Signal Energy (Defines Hybrid Trans-	Level at RXA pin with receive Boost Enabled				
Hybrid loss requirements)	Scrambled data at 2400 bit/s in opposite band			-14	dBm
	Sinusoids out of band			-9	dBm
Clock Noise	TXA pin; 153.6 kHz				
73K224L				1.5	mVrms
Carrier Offset					
Capture Range	Originate or Answer		±7	±10	Hz

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Recovered Clock					
Capture Range	% of frequency originate or answer	-.024		+.024	%
Guard Tone Generator					
Tone Accuracy	550 Hz			+1.18	%
	1800 Hz	-0.7			
Tone Level	550 Hz	-5.0	-3.0	-2.0	dB
(Below QAM/DPSK Output)	1800 Hz	-8.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
(700 to 2900 Hz)	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE	30			ns
TLA	$\overline{CS}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{RD}/\overline{WR}$ control	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to Latch	10			ns
TRD	Data out from $\overline{RD}$	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after READ	0		200	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns

1: Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

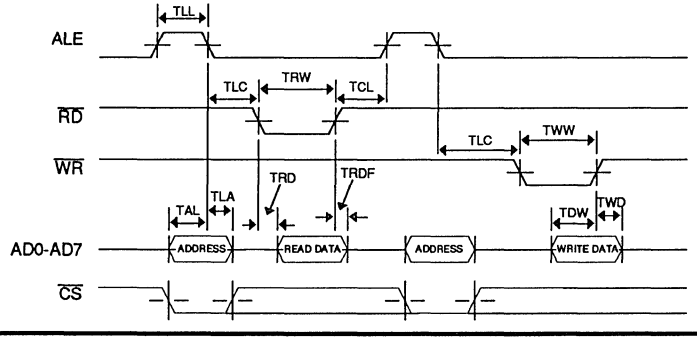


FIGURE 1: Bus Timing Diagram (Parallel Version)

PERFORMANCE DATA

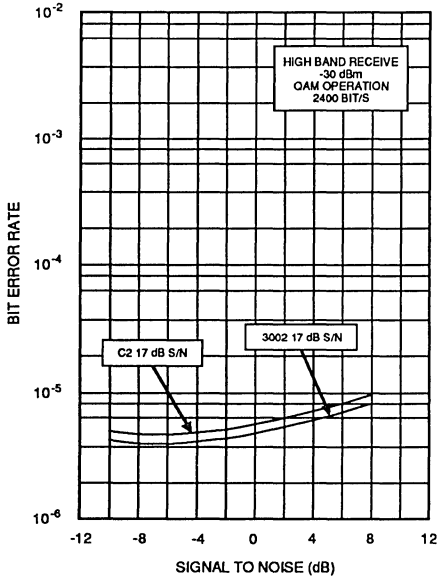
(This performance data was taken using an AEA tester and the 73D2402 MEU board.)

TYPICAL BER PERFORMANCE

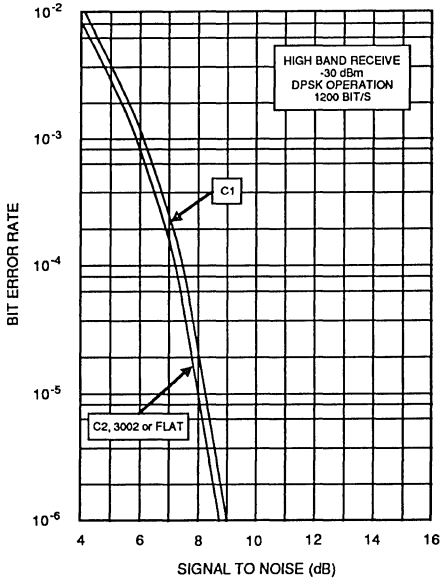
(-20dBm receive level 10-5 BER)

PARAMETER - RECEIVE BAND C-WEIGHTED	MINIMUM SNR REQUIRED
2400 bit/s Originate	17 dB SNR
2400 bit/s Answer	18.5 dB SNR
1200 bit/s Originate	8.0 dB SNR
1200 bit/s Answer	8.5 dB SNR
0-300 bit/s Originate	8.0 dB SNR
0-300 bit/s Answer	8.0 dB SNR

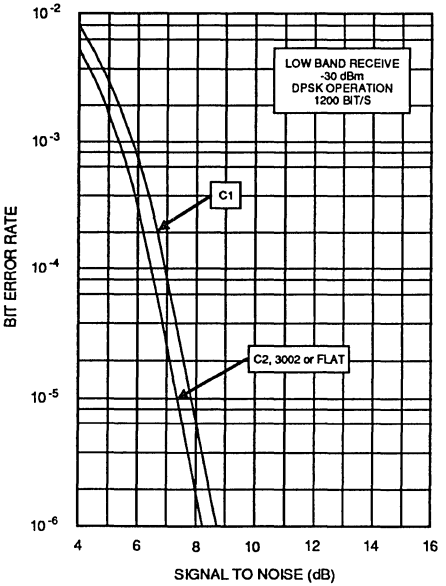
SSI 73K224L BER vs CARRIER OFFSET
PRELIMINARY



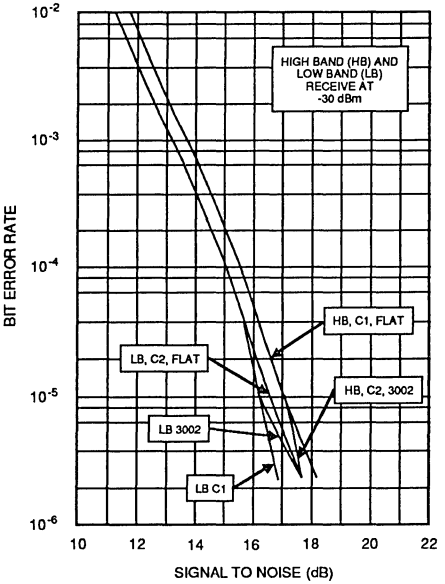
SSI 73K224L BER vs S/N
PRELIMINARY



SSI 73K224L BER vs S/N
PRELIMINARY



SSI 73K224L BER vs QAM



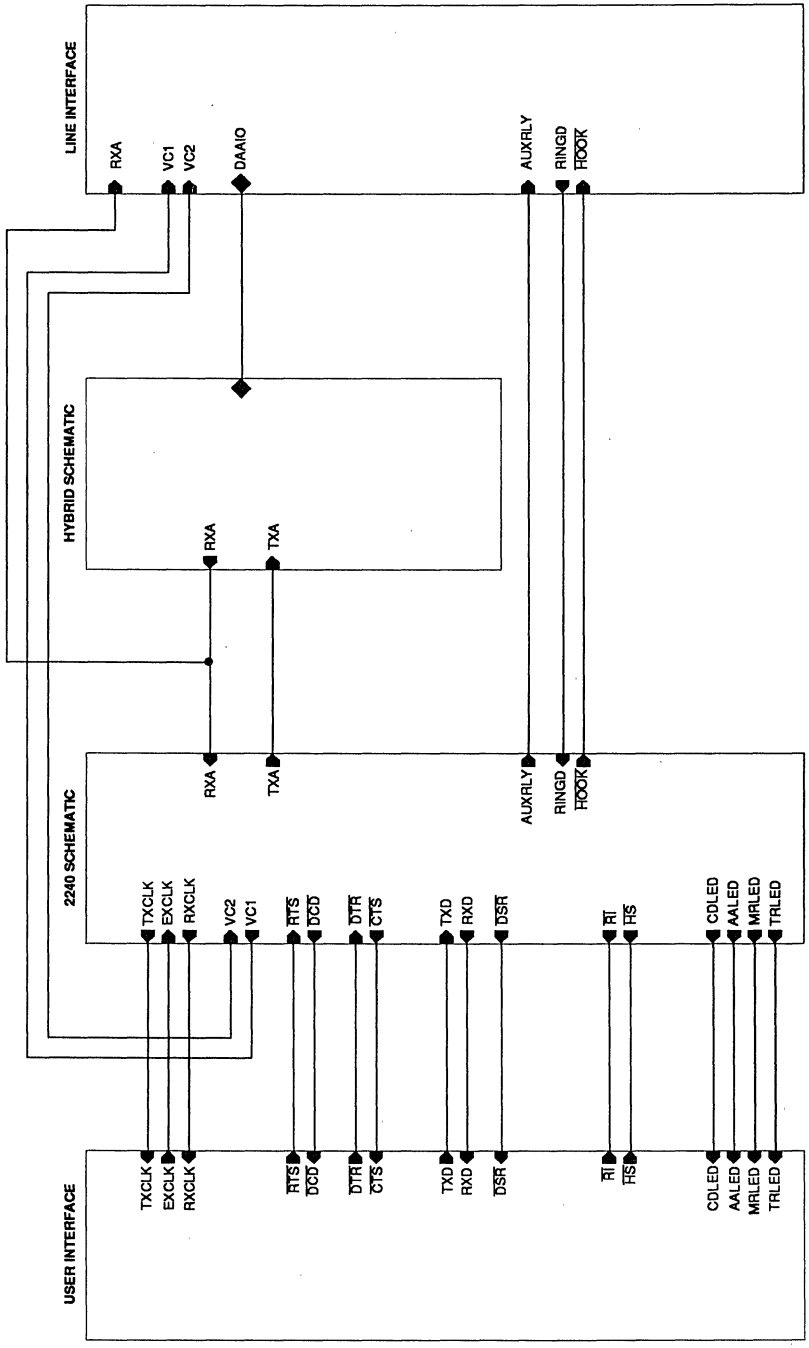


FIGURE 2: SSI 73D2240 Box Modem Block Diagram

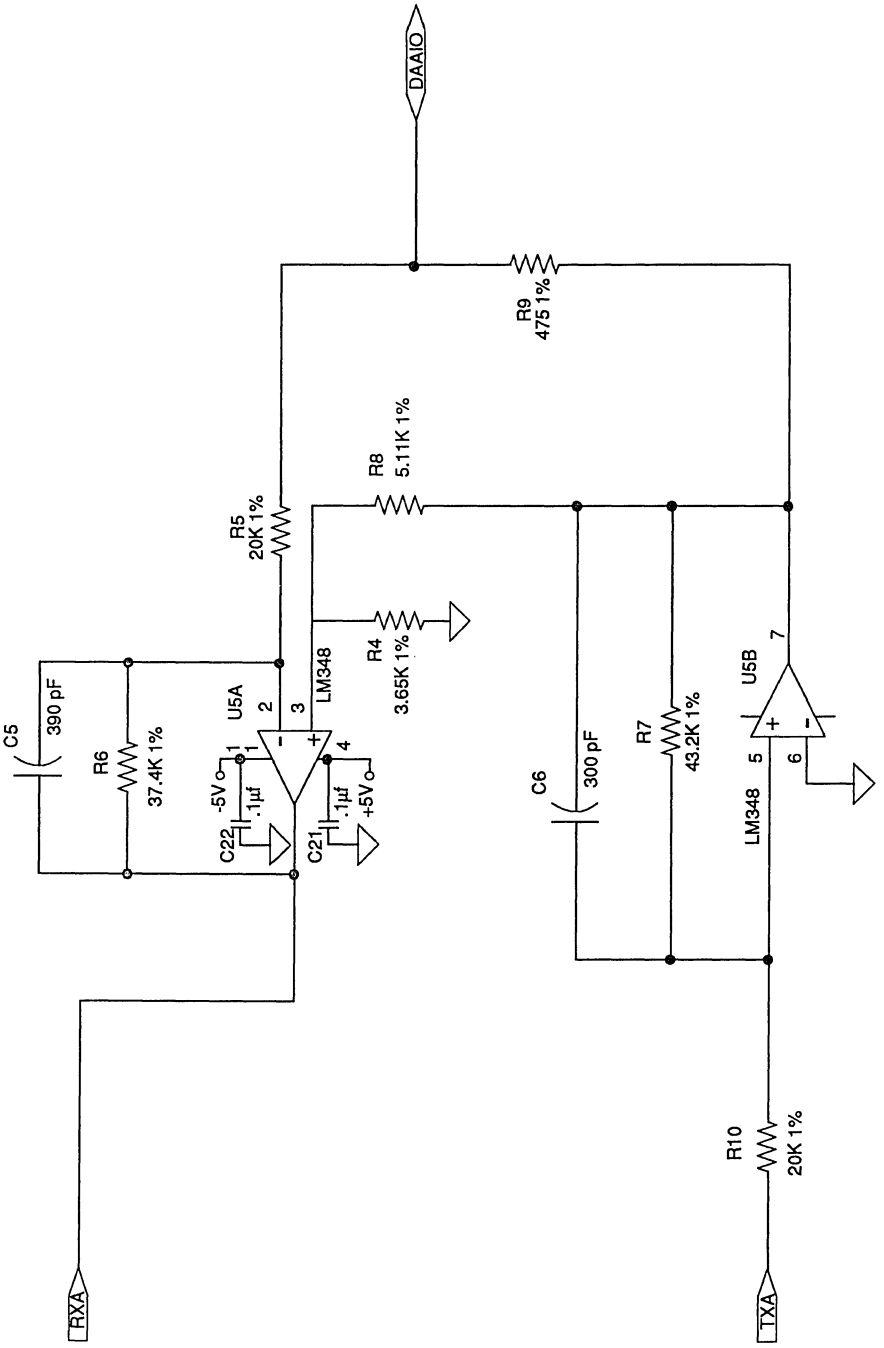


FIGURE 3: SSI 73D2240 Hybrid

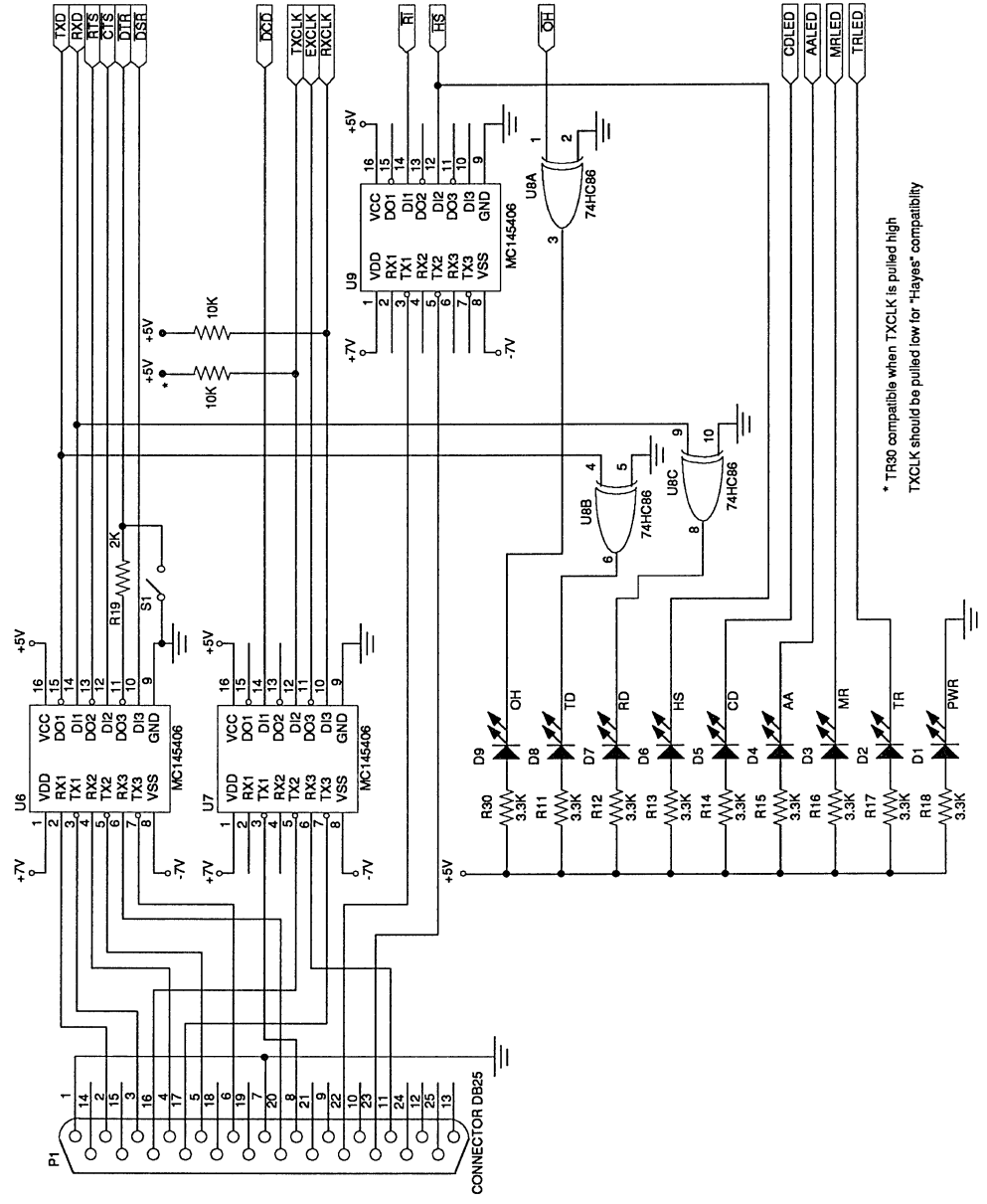


FIGURE 4: 73D2240 User Interface

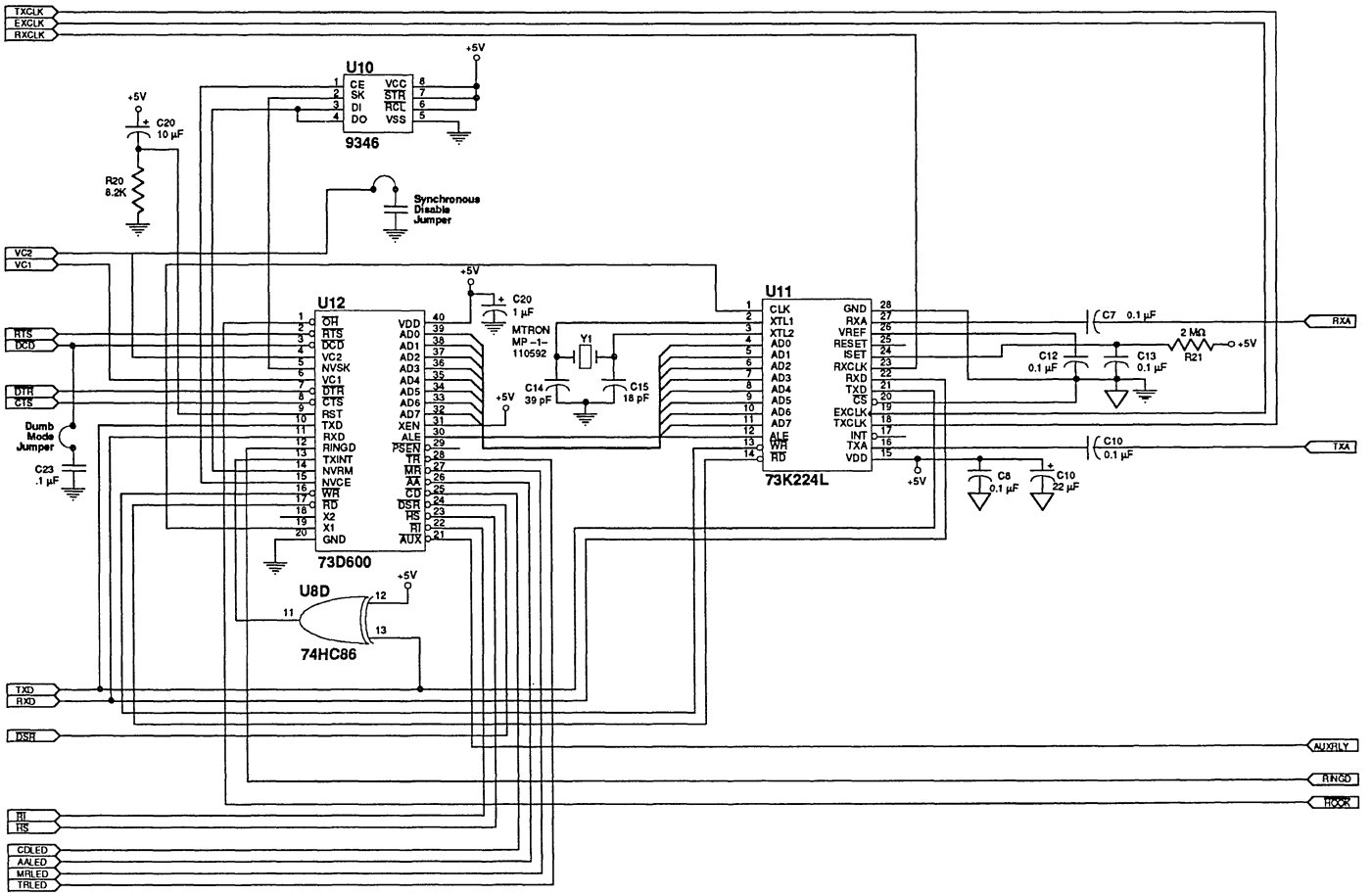


FIGURE 5: 73D2240 Interconnect

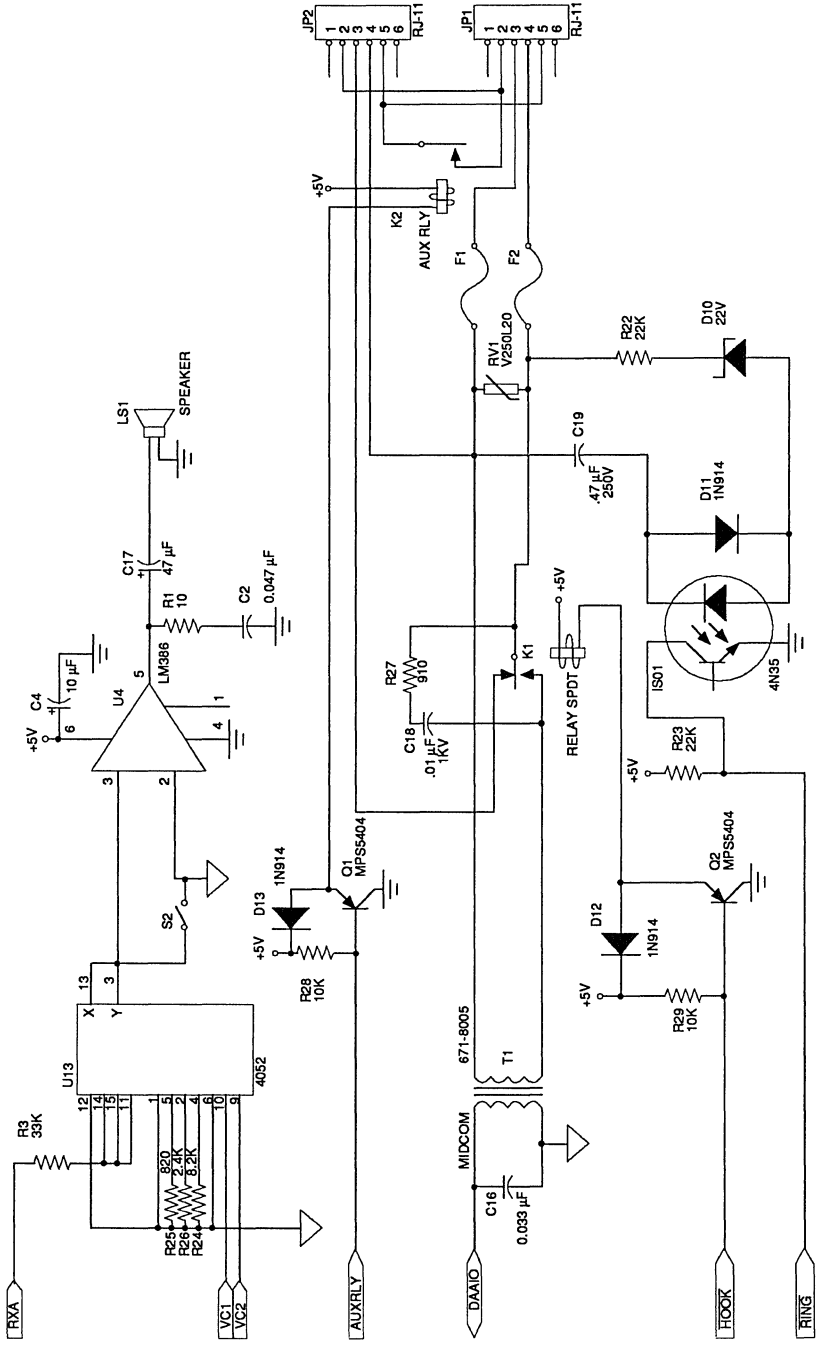
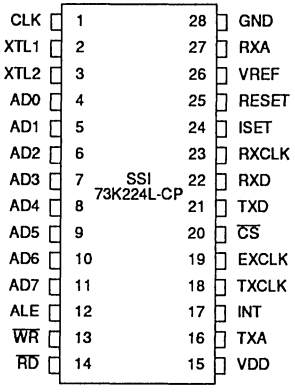
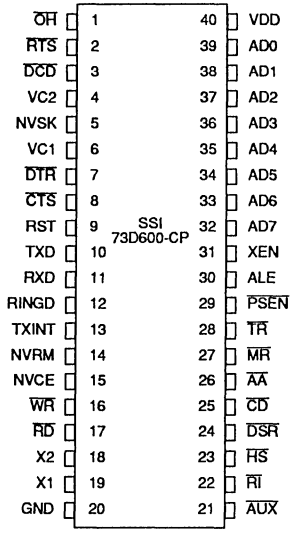


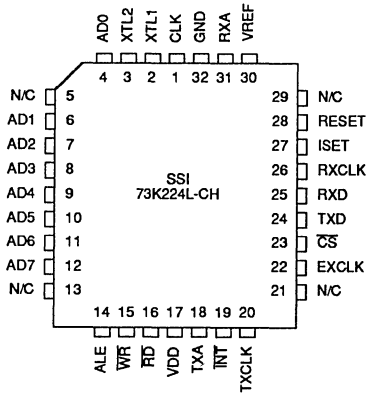
FIGURE 6: 73D2240 Line Interface

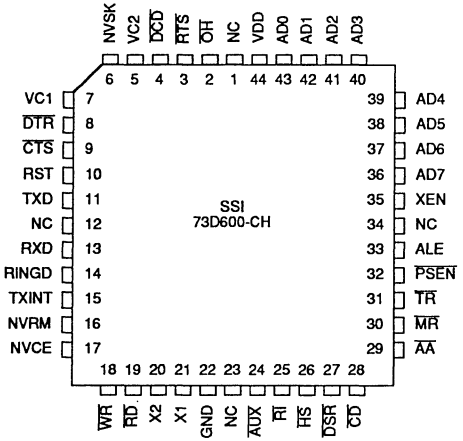
PIN DIAGRAMS - Top View





SSI 73K2240-CP
28- and 40-Pin DIP





SSI 73K2240-CH
32- and 44-Pin PLCC

SSI 73D2240
V.22bis 2400 Bit/s
Modem Device Set

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

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SSI 73D2404
V.22bis 2400 Bit/s Modem Device Set

June, 1990

2

DESCRIPTION

The SSI 73D2404 consists of three CMOS integrated circuits which together provide the data pump functions required to construct a high performance 2400 bit/s full-duplex intelligent modem for use over the dial-up telephone network. The 73D2404 includes operating modes compatible with CCITT V.22bis, V.22, V.21, as well as Bell 212A and 103 data-communications standards. Using advanced CMOS processes that include analog, digital signal processing and switched capacitor filter techniques, the SSI 73D2404 offers excellent performance and a high level of functional integration in a compact three-chip set available in DIP or surface mount packages.

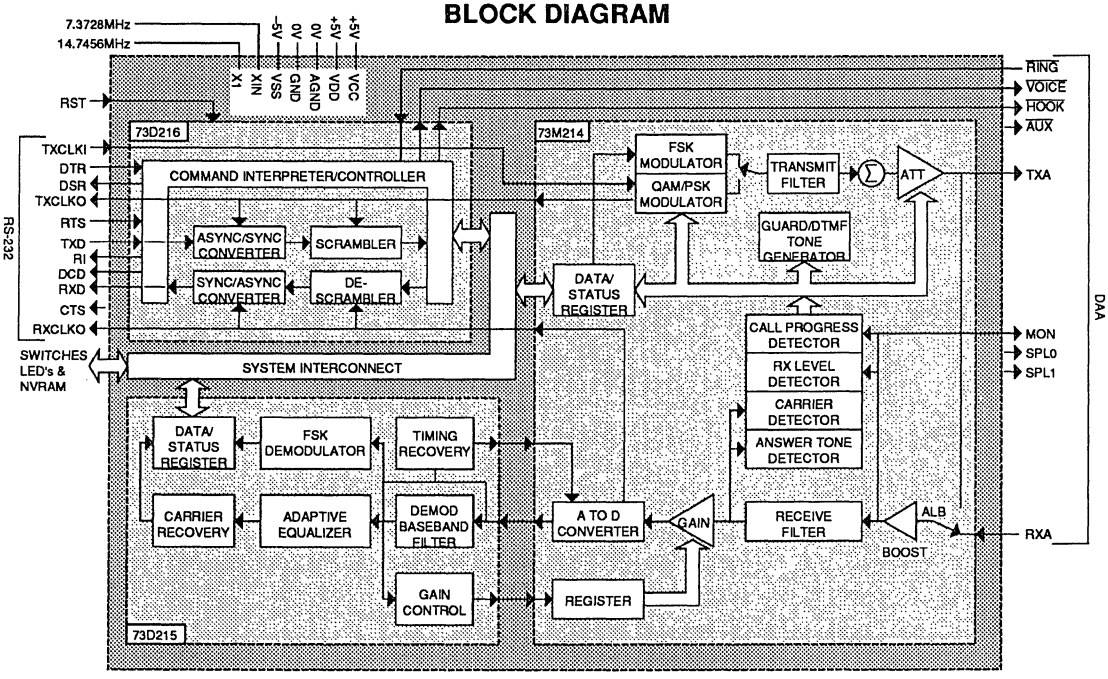
The 73D2404 is ideal for use in both free-standing or integral system modem products where full-duplex 2400 bit/s data-communications over the 2-wire public service telephone network is desired.

FEATURES

- **Multi-mode V.22bis/V.22/V.21 & Bell 212A/103 compatible device set for intelligent modem designs**
- **Full duplex operation at 0-300, 1200 and 2400 bit/s with with both synch & asynch operating modes**
- **Includes high-level "AT" command interpreter compatible with 2400 bit/s industry standard products**
- **Complete complement of "AT" modem features**
- **Selectable automatic speed detect, handshake and autobaud functions**
- **Supports external non-volatile memory to store user configurations**
- **Adaptive equalization for optimum performance over all lines**
- **Dynamic range from 0 to -45dBm**
- **Call progress, carrier and answer tone detectors provide intelligent dialing functions**

(Continued)

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FEATURES (Continued)

- **DTMF and CCITT guard tone generators**
- **Test modes available - ALB, DL, RDL for complete test capability**
- **All CMOS technology for low power consumption**

OPERATION

The SSI 73D2404 is a complete V.22bis intelligent modem contained in three CMOS IC's. The device set forms the basis for a high performance stand-alone modem product with self-contained command interpreter, indicator LED's, default switches and interface lines for an RS-232 serial port. Both data and commands are passed over the serial port as in conventional intelligent modem designs.

The SSI 73D2404 provides the QAM, PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guard tones. This device supports the V.22bis, V.22, V.21 and Bell 212A/103 operating modes, both synchronous and asynchronous. The 73D2404 is designed to provide functions needed for an intelligent modem and includes auto-dial/auto-answer, handshake with auto-fallback, and selectable pulse or DTMF dialing sequences to simplify these designs.

The SSI 73D2404 consists of three devices. The SSI 73M214 is an analog processor that performs the filtering, timing adjustment, level detection and modulation functions. The 73D215 is the receiver digital signal processor. The 73D216 is a command processor that provides supervisory control and command interpretation.

QAM MODULATOR/DEMODULATOR

The SSI 73D2404 scrambles and encodes the 2400 bit/s incoming data into quad bits represented by 16 possible signal points as specified by CCITT recommendation V.22bis. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator reverses this procedure and recovers a data clock from the incoming signal. Adaptive equalization corrects for different line conditions by automatically changing filter parameters to compensate for line characteristics.

PSK MODULATOR/DEMODULATOR

In PSK mode the 73D2404 modulates the 1200 bit/s incoming data using a subset of the QAM signal points as specified by CCITT recommendation V.22bis, V.22 and Bell 212A. The PSK demodulator is similar to the QAM demodulator.

FSK MODULATOR/DEMODULATOR

The FSK transmitter frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) or the V.21 standard frequencies of 980 and 1180 Hz (originate mark and space) and 1650 and 1850 Hz (answer mark and space) are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A bandsplit filter is included to shape the amplitude and phase response of the transmit signal to a square root 75% raised cosine and provide rejection of out-of-band signals in the receive channel.

ASYNCHRONOUS MODES

The asynchronous mode is used for communication between asynchronous terminals which may vary the data rate from +1.5% to -1.5%. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal whose data rate is accurate to 0.01%. The signal is routed to a data scrambler (following the CCITT V.22bis algorithm) and into the modulator. The 73D2404 recognizes a break signal and handles it in accordance with BELL 212A specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits. An incoming break signal will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODES

Synchronous operation is possible only with the QAM or PSK mode. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the falling edge of TXCLK. Receive data at the RXD output is clocked out on the rising edge of RXCLK. The async/synch converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as is input.

AUTOMATIC HANDSHAKE

The SSI 73D2404 will automatically perform a complete handshake as defined by the V.22bis, V.22 and Bell 212A/103 standards to connect with a remote modem. The 73D2404 automatically determines the speed and operating mode and adjusts its operation to correspond to that of an answering modem when originating a call.

TEST MODES

The SSI 73D2404 allows use of Analog Loopback, Digital Loopback and Remote Digital Loopback test modes. Full test mode capability allows testing of the modem and interface functions from the local terminal using the appropriate control commands, or remotely using the RDL function.

ADAPTIVE EQUALIZATION WITH AUTO-RETRAIN

The SSI 73D2404 uses adaptive equalization which automatically compensates for varying line characteristics by adjusting taps on a multi-tap FIR filter. Optimum performance is obtained with this technique over a wide range of line conditions. When the line quality deteriorates to a specified level the 73D2404 can automatically initiate a retrain of the equalizer to re-establish data communications without the need to go through a complete handshake sequence.

"AT" COMMAND INTERPRETER

The SSI 73D2404 includes an AT command interpreter which is compatible with the Hayes 2400 Smartmodem™ command set. Functions and features included with intelligent modems are provided by the 73D2404 command interpreter.

NON-VOLATILE MEMORY

The SSI 73D2404 supports connection to an external non-volatile memory (ie. Xicor X2444) to store a dial string and the current AT command configuration.

SPEED/PROTOCOL COMPATIBILITY GUIDE

Calling a:			73D2404 originating as:				
			Bell		CCITT		
			300	1200	300	1200	2400
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400[1]	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22bis)	300	1200	-	1200	2400
Called from a:			**73D2404 answering as:**				
			Bell		**CCITT**		
			300	**1200**	**300**	**1200**	**2400**
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22bis)	300	1200	-	1200	2400

[1] A Bell 2400 is a V.22bis using a 2225 Hz answer tone without unscrambled marks.

HARDWARE INTERFACE

POWER SUPPLIES AND CLOCKS

LABEL	I/O	PIN CONNECTION			DESCRIPTION
		73M214	73D215	73D216	
VDD	I			40	Positive supply (analog +5V)
VCC	I	28	28		Positive supply (digital +5V)
VSS	I	14			Negative supply (analog -5V)
AGND	I	26			Analog ground
GND	I	15	14	20	Digital ground
X1	I			19	Clock input 14.7456 MHz
XIN	I	18			Clock input 7.3728 MHz
RST	I			9	Reset (10 µF & 8.2k)

DAA INTERFACE

RXA	I	27			Receive analog from DAA
TXA	O	20			Transmit analog to DAA
MON	O	25			Audio monitor
SPL0	O			B.4*	Audio volume control
SPL1	O			B.5*	Audio volume control
$\overline{\text{RING}}$	I			5	From ring indicator
$\overline{\text{HOOK}}$	O			6	Off hook relay control
AUXR	O			B.7*	Auxiliary relay control

RS-232/V.24 INTERFACE

RI	O			3	Ring indicator output
RATE	O			B.3*	Indicates high speed
TXD	I			10	Digital data from terminal
RXD	O			11	Digital receive data
DCD	O			2	Data carrier detect
DSR	O			4	Data set ready
EXCLK	I	22			External Tx sync clock input
RXCLK	O	24		8	Receive clock ouptut
TXCLK	O	23		15	Transmit clock output
CTS	O			B.6*	Clear to send
RTS	I			B.6*	Request to send
DTR	I			B.7*	Indicates DTE available

* Available with expanded I/O

HARDWARE INTERFACE (Continued)

LED DISPLAY

LABEL	I/O	PIN CONNECTION 73M214	73D215	73D216	DESCRIPTION
$\overline{WR}$	O	4	24	16	Write strobe (active low)
TR	LED	Performed externally			Data terminal ready
SD	LED			10	Transmit data
RD	LED			11	Receive data
CD	LED			2	Data carrier detect
HS	LED			B.3*	High speed indicator
MR	LED			B.2*	Modem ready/test in progress
AA	LED			B.1*	Auto answer indicator
OH	LED			B.0*	Off hook indicator

DEFAULT SWITCHES

$\overline{IOEN}$	O			26	LED/switch enable (active low)
$\overline{RD}$	O	3	25	17	Read strobe (active low)
SW2-1	SW	Performed externally			Force DTR
SW2-2	SW			B.5*	Disable "AT" recognition ("Dumb" mode)
SW2-3	SW	Performed externally			Force DCD

NVRAM INTERFACE

NVRCE	O			14	NVRAM CE (active high)
TXD	I/O			10	NVRAM DI/DO
RXD	I			11	NVRAM SK

* Available with expanded I/O

HARDWARE INTERFACE (Continued)

LABEL	I/O *	PIN CONNECTION 73M214	73D215	73D216	DESCRIPTION
DEVICE SET INTERCONNECT (Refer to Figure 7 & 8.)					
VPP	I		1		+5V
INT	I		17		+5V
$\overline{EA}$	I			31	+5V
EXADCC	I	19			0V
$\overline{DACK}$	I		2		+5V
CLK	S	16	15		7.3728 MHz
RXINT	S		5	13	RX Interrupt
$\overline{TXINT}$	S	21		12	TX Interrupt
RST	S		16	1	
FSK	S		4	7	
$\overline{RD}$	S	3	25	17	
$\overline{WR}$	S	4	24	16	
A15	S	2		28	
A8	S		27	21	
D0	I/O	5	6	39	Data Bus 0
D1	I/O	6	7	38	Data Bus 1
D2	I/O	7	8	37	Data Bus 2
D3	I/O	8	9	36	Data Bus 3
D4	I/O		10	35	Data Bus 4
D5	I/O		11	34	Data Bus 5
D6	I/O		12	33	Data Bus 6
D7	I/O		13	32	Data Bus 7
SIN	S	10	22		
SOUT	S	11	21		
SIRQ	S	9	23		
SCK	S	13	18		
$\overline{SEN}$	S	12	19,20		

* "S" refers to system interconnect

"AT" COMMANDS SUPPORTED
(Note: s=string; n=decimal, 0-255; x=boolean, 0/1=false/true)

COMMAND	OPTIONS	DEFAULT
A/	Repeats last command line	N/A
A	Answer	N/A
Bx	BELL/CCITT = 1/0 answer tone @1200 (N/A @2400)	1
Ds	Dial string specified by s	No string
Ex	Command echo, 0/1 = off/on	1
Hn	Hook status, 0/1 = on/off	N/A
In	ID code, 0/1/2/3/4 (see Table 8)	N/A
Kn	SSi test	N/A
Ln	Speaker volume, (0)1/2/3 = lo/med/hi	2
Mn	Speaker, 0/1/2/3 = control (see Table 3)	1
On	Online, 0/1/2/3 = on-line/retrain/no retrain (see Table 4)	N/A
P	Pulse dial	Pulse
Qx	Quiet result, 0/1 = 1-quiet	0
R	Reverse originate	N/A
Sn=n	Set S register (see Table 2)	N/A
Sn?	Return value in register n (see Table 2)	N/A
T	Touch tone dial	Pulse
Ux	User help screen, Sreg, dial string, data format	N/A
Vx	Verbose result, 0/1 = off/on	1
Xn	Result code, 0/1/2/3/4 (see Table 1)	4
Yx	Enable long space disconnect, 1 = enable	0
Z	Restore from Non-Volatile Memory	N/A
&Cx	Carrier detect override, 0/1 = on/normal	0
&Dn	DTR mode, 0/1/2/3 (see Table 5)	0
&F	Restore to factory configuration	N/A
&Gn	CCITT guard tone, 0/1/2 = off/1800/550	0
&Jx	Auxiliary relay control	0
&Mn	Async/Sync mode, 0/1/2/3 (see Table 6)	0

"AT" COMMANDS SUPPORTED (Continued)

COMMAND	OPTIONS	DEFAULT
&Rx	Enable RTS/CTS	0
&Sx	DSR override, 0/1=on/normal	0
&Tn	Test mode (see Table 7)	N/A
&Px	Pulse dial mode, 0/1=U.S./U.K.	0
&W	Write current configuration to NVRAM	N/A
&Xn	Sync Tx clock mode, 0/1/2=int/ext/slave	0
&Zs	Store a telephone number=string	N/A

Factory configuration[1]:
B1 E1 F1 L2 M1 P Q0 V1 X4 Y0 &C0 &D0 &G0 &J0 &M0 &P0 &R0 &S0 &T4 &X0

Dial string arguments:
, = delay @ = silent answer ! = flash
; = return to command s = dial stored number W = wait for tone R=reverse mode

[1]If the NovRAM has not been initialized it may be necessary to type AT&F&W<cr> to properly initialize modem state.

TABLE 1: Result Codes

Xn	VOCAL/NUMERIC RESULT CODE
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNCET (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6

TABLE 2: S Registers Supported

NUMBER	FUNCTION	UNITS	DEFAULT
S0[1]	Answer on ring	No. of rings	000
S1	Ring counter	No. of rings up to 8	000
S2	Escape code	ASCII CHR	043
S3	Carriage return	ASCII CHR	013

[1]Stored in NVRAM with &W command

TABLE 2: S Registers Supported (Continued)

NUMBER	FUNCTION	UNITS	DEFAULT
S4	Line feed	ASCII CHR	010
S5	Back space	ASCII CHR	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds	006
S10	Carrier drop out	100 milliseconds	014
S11	DTMF tone duration	1 millisecond	070
S12	Escape guard time	20 milliseconds	050
S13	Unused		N/A
*S14[1]	Bit mapped register	Decimal 0-255	170
S15	Unused		N/A
S16	Test register	Decimal #	000
S17	SSI Special test register	Decimal 0-255	096
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[1]	Bit mapped register	Decimal 0-255	000
*S22[1]	Bit mapped register	Decimal 0-255	118
*S23[1]	Bit mapped register	Decimal 0-255	007
S24	Unused		N/A
S25[1]	DTR delay	10 milliseconds	005
S26[1]	CTS delay	10 milliseconds	001
*S27[1]	Bit mapped register	Decimal 0-255	064

*The bit mapped register functions are equivalent to normal "AT" command modem registers. They are not needed for evaluation of the 73D2404 capabilities.

Asynchronous character formats supported:
[Number of data bits, parity (even/odd/none), number of stop bits]

1200/2400 bit/s: 7N2, 7E1, 7O1, 8N1

300 bit/s: 7N2, 7E1, 7O1, 8N1, 8E1, 8O1

[1]Stored in NVRAM with &W command

TABLE 3: Speaker Modes

Mn	SPEAKER MODE
M0	Speaker off
M1	Speaker on during connect only
M2	Speaker on always
M3	Speaker on during call progress

TABLE 4: O Modes

On	ONLINE/RETRAIN MODE
O0	Return online
O1	Return online with retrain
O2	Enable automatic retrain (default)
O3	Disable automatic retrain

TABLE 5: DTR Modes

&Dn	DTR MODE
&D0	Ignore DTR
&D1	Go to command state if ON to OFF detected
&D2	Go to command state and disable auto-answer if ON to OFF detected
&D3	Initialize modem with NVRAM if ON to OFF detected

TABLE 6: Synchronous Modes

&Mn	SYNCHRONOUS MODE
&M0	Asynchronous
&M1	Sync mode entered upon completion of connect sequence
&M2	Dial stored number on OFF to ON transition of DTR and go online
&M3	Manual dial using DTR as talk data switch

TABLE 7: Test Modes

&Tn	TEST MODE
&T0	End/Abort test
&T1	Initiate local analog loopback (L3)
&T3	Initiate local digital loopback
&T4	Permit remote digital loopback (L2)
&T5	Prohibit remote digital loopback
&T6	Initiate remote digital loopback (L2)
&T7	Initiate RDL with self-test and error detector
&T8	Initiate ALB with self-test and error detector

TABLE 8: ID Codes

In	CODE
I 0	Product code (249)
I 1	ROM checksum
I 2	Checksum test
I 3	Product revision
I 4	Software copyright

DIP SWITCH FUNCTIONS SUPPORTED
(DIP switches are only read on power-up if NovRAM is not present.)

SWITCH	FUNCTION	SETTINGS (Suggested default underlined)
SW2-1	DTR override	off = DTR signal controls modem
		on = DTR always on
SW2-2	"AT" command set recognition	off = Normal operation
		on = "AT" command recognition disabled ("dumb" mode)
SW2-3	Carrier detect override	off = RS-232 CD line toggles (&C1)
		on = CD line always on (&C0)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Ta, Ambient Temperature		0		70	°C
VCC & VDD, Supply Voltage	73M214, 73D215, 73D216	4.25		5.25	V
VSS, Supply Voltage	73M214	-4.25		-5.25	V
VDD, VSS Bypass Capacitors		10+0.1			µF
CLK Load Capacitance				25	pF
Digital Load Capacitance				50	pF
TxA, MON Loading				See Note	
Input Clock Frequency (X1)			14.7456		MHz
Input Clock Variation (X1, XIN)	XIN must be X1 div. by 2	-0.01		0.01	%

Note: 10 KΩ in parallel with 50 pF

INPUT CLOCK TIMING (See Figure 1.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
TCLCX		20			ns
TCLCX2		54		82	ns
TCHCX		20			ns
TCHCX2		54		82	ns
TR, TF				15	ns
TCHCH		0		20	ns

INTERFACE TIMING (This information is provided to assist in the connection of external circuitry to the data bus. Refer to application circuit in Figure 9.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
LED Write Timing (See Figure 2.)						
TWLWH	$\overline{WR}$ pulse width		307			ns
TAVWL	Address valid to $\overline{WR}$ low		141			ns
TQVWH	Data valid to $\overline{WR}$ high		370			ns
TQVWX	Data valid to $\overline{WR}$ transition		27			ns
TWHDX	Data hold after $\overline{WR}$		86			ns
Switch Read Timing (See Figure 3.)						
TRLRH	$\overline{RD}$ pulse width		307			ns
TAVRL	Address valid to $\overline{RD}$ low		141			ns
TRLDV	$\overline{RD}$ low to data valid				174	ns
TRHDX	Data hold after $\overline{RD}$		0			ns

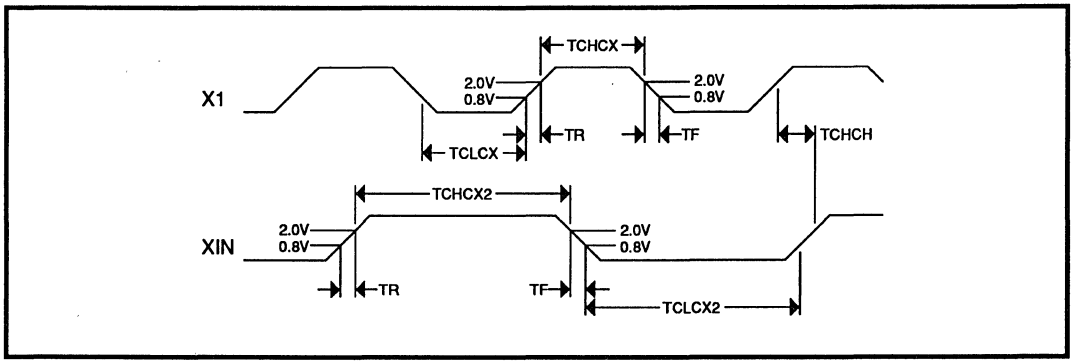


FIGURE 1: Input Clock Timing

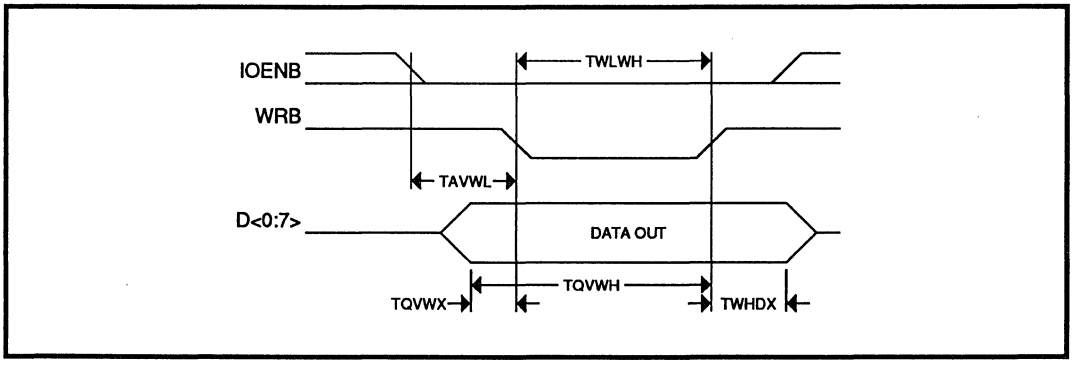


FIGURE 2: LED Write Timing

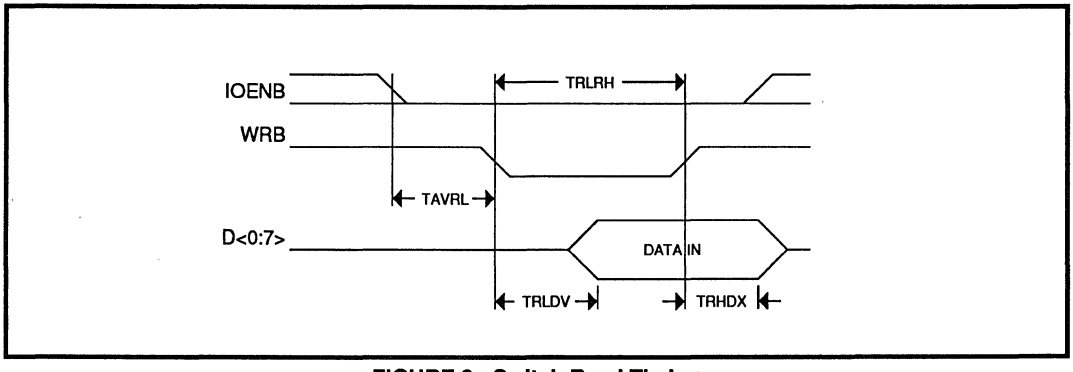


FIGURE 3: Switch Read Timing

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
IDD	Supply Current				100	mA
ISS					25	mA
VIL	Input Low Voltage		0		0.8	V
VIH	Input High Voltage		2.0		VDD	V
IIH	Input High Current	Except $\overline{CS}$ which has a pullup of 20 kΩ			-20 10	µA µA
IIL	Input Low Current	Except TxCLKI, EXADC which have pullup of 20 kΩ			-20	µA
	Digital Input Capacitance				10	pF
VOH	Output High Voltage	Iout = -.4 mA	2.4			V
VOL	Output Low Voltage	Iout = 1.6 mA			0.4	V
RXA	Input Resistance		100k			Ω
RXA	Input Capacitance				25	pF

TRANSMITTER SPECIFICATIONS

TRANSMITTER POWER

Values given are measured at the line connection point and assume that the DAA shown in Figure 8 is used with a 600Ω load.

TRANSMITTER POWER	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Transmitter Power	With or without CCITT tones	-9.8		-8.2	dBm
CCITT Guard Tone	550	-14.8		-12.8	dBm
	1800	-16.0		-14.0	dBm
FSK Transmitter Power	103/V.21	-10.0		-8.0	dBm
Answer Tone Power		-10.0		-8.0	dBm
DTMF Transmitter Power	High band tones	-7.0		-5.0	dBm
	Low band tones	-9.0		-7.0	dBm
	Twist	-3.0		-1.0	dB

TRANSMITTER FREQUENCY
(All tones are digitally derived from the clock input and have the input clock frequency tolerance.)

TRANSMITTER FREQUENCY		CONDITIONS		MIN	NOM	MAX	UNITS
QAM/DPSK Carrier Frequencies		Originate			1200.0		Hz
		Answer			2400.0		Hz
FSK Tone Frequencies							
103	Originate	Space	1070		1066.7		Hz
		Mark	1270		1269.4		Hz
	Answer	Space	2025		2021.1		Hz
		Mark	2225		2226.1		Hz
V.21	Originate	Space	1180		1181.6		Hz
		Mark	980		978.3		Hz
	Answer	Space	1850		1850.0		Hz
		Mark	1650		1651.6		Hz
Special Tone Frequencies							
Answer Tone			2100		2104.1		Hz
CCITT Guard Tones			550		556.5		Hz
			1800		1786.0		Hz
DTMF Dialing Tone Frequencies							
Low Group		Columns	697		698.2		Hz
			770		771.9		Hz
			852		853.3		Hz
			941		942.3		Hz
High Group		Rows	1209		1209.5		Hz
			1336		1335.7		Hz
			1477		1476.9		Hz
			1663		1634.0		Hz

TRANSMITTER DISTORTION

TRANSMITTER DISTORTION	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Carrier Suppresion	Measured at TxA	35			dB
CCITT Guard Tone Distortion	800-1600 Hz band			-60	dB
	0-10 kHz band			-45	dB
Answer Tone Distortion	800-1600 Hz band			-60	dB
	0-10 kHz band			-40	dB
FSK Output Bias Distortion	Transmit dotting 300 bit/s	-6		6	%
FSK Opposite Band Distortion				-60	dB
DTMF Tone Distortion	700-2900 Hz band			-29	dB

RECEIVER SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier VCO					
Capture Range	Carrier offset	-10		10	Hz
Carrier Jitter	50-65 Hz			30	Degrees
Data Clock Recovery Capture Range	From system clock div. by 24576 (600 Hz symbol clock)	-.025		+.025	%
Data Delay Time	RxA to RxD	30		75	ms
Retrain Request Threshold	If enabled	10-3		10-2	BER
Carrier Detect					
Threshold		-48		-43	dBm
Hysteresis		2			dB
Answer Tone Detect	2100/2225 Hz				
Threshold		-48		-43	dBm
Hysteresis		2			dB
Call Progress Detect	350-650 Hz dual tone				
Threshold		-40		-30	dBm
Hysteresis		2			dB

PERFORMANCE DATA

(This performance data was taken using an AEA tester and the 73D2404 MEU board.)

BER PERFORMANCE

(-20dBm receive level 10-5 BER)

PARAMETER	MINIMUM SNR REQUIRED
2400 bit/s Originate	16.5 dB SNR
2400 bit/s Answer	16.0 dB SNR
1200 bit/s Originate	9.0 dB SNR
1200 bit/s Answer	8.0 dB SNR
0-300 bit/s Originate	9.0 dB SNR
0-300 bit/s Answer	7.5 dB SNR

DYNAMIC RANGE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
2400 bit/s Originate	10-5 BER @ 17dB SNR	-45		0	dBm
2400 bit/s Answer	10-5 BER @ 17dB SNR	-45		0	dBm
1200 bit/s Originate	10-5 BER @ 12dB SNR	-45		0	dBm
1200 bit/s Answer	10-5 BER @ 12dB SNR	-45		0	dBm
0-300 bit/s Originate	10-5 BER @ 12dB SNR	-45		0	dBm
0-300 bit/s Answer	10-5 BER @ 12dB SNR	-45		0	dBm

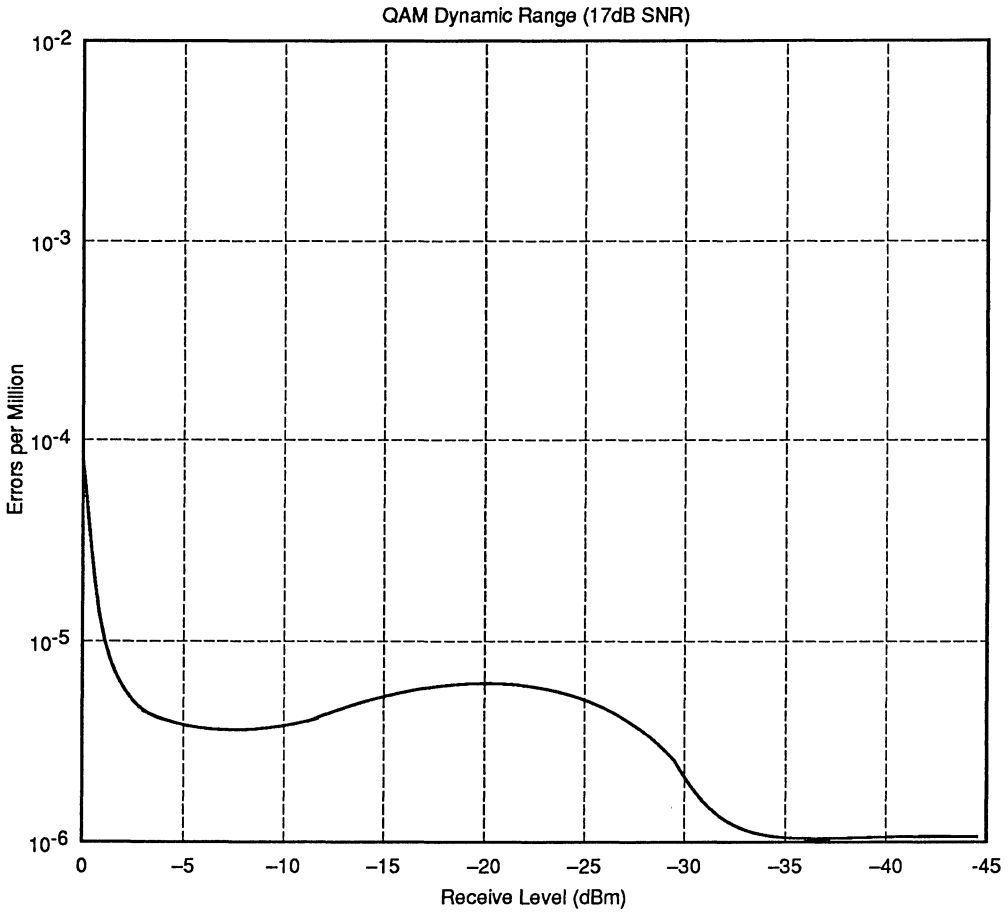


FIGURE 4: QAM Dynamic Range

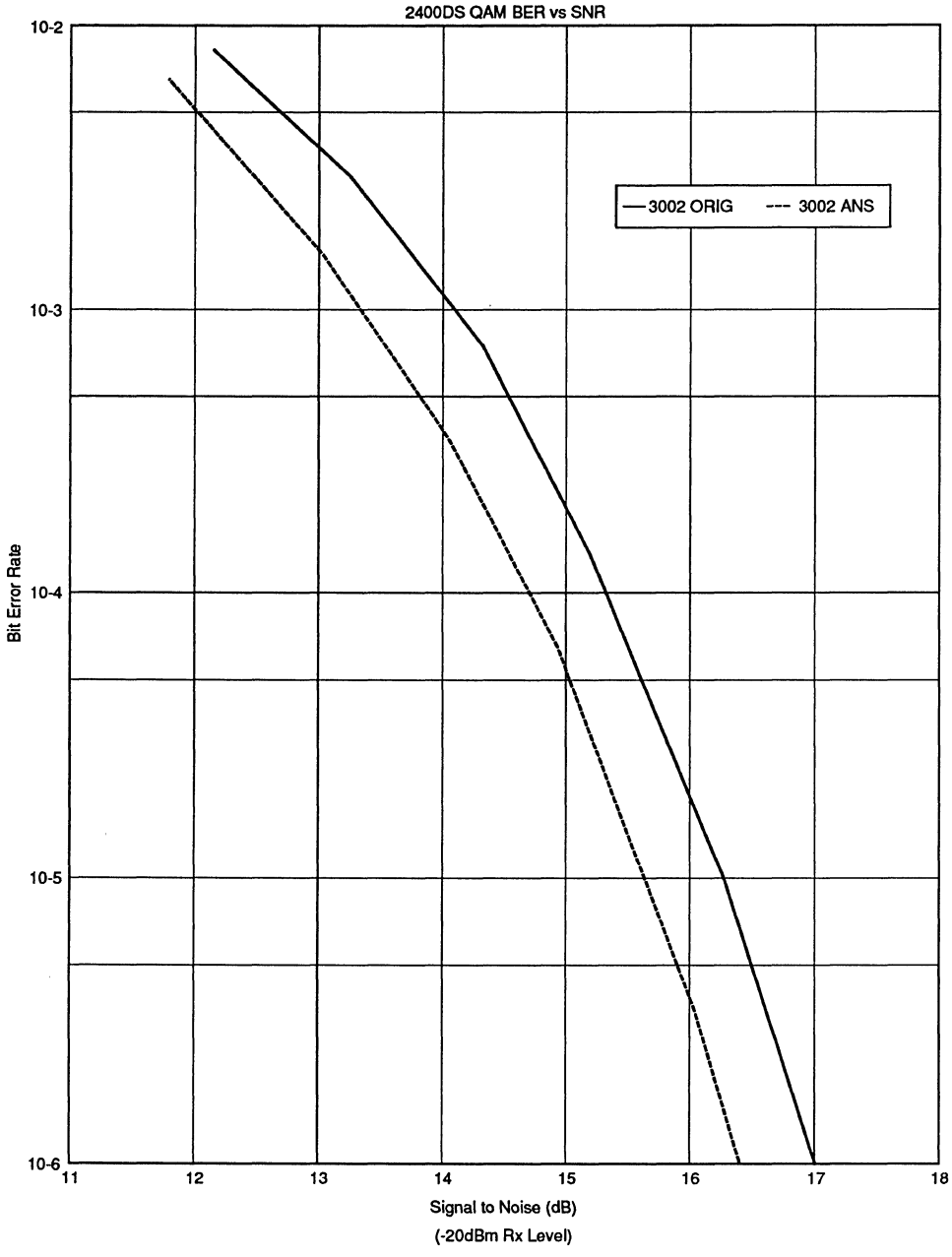


FIGURE 5: BER vs. SNR

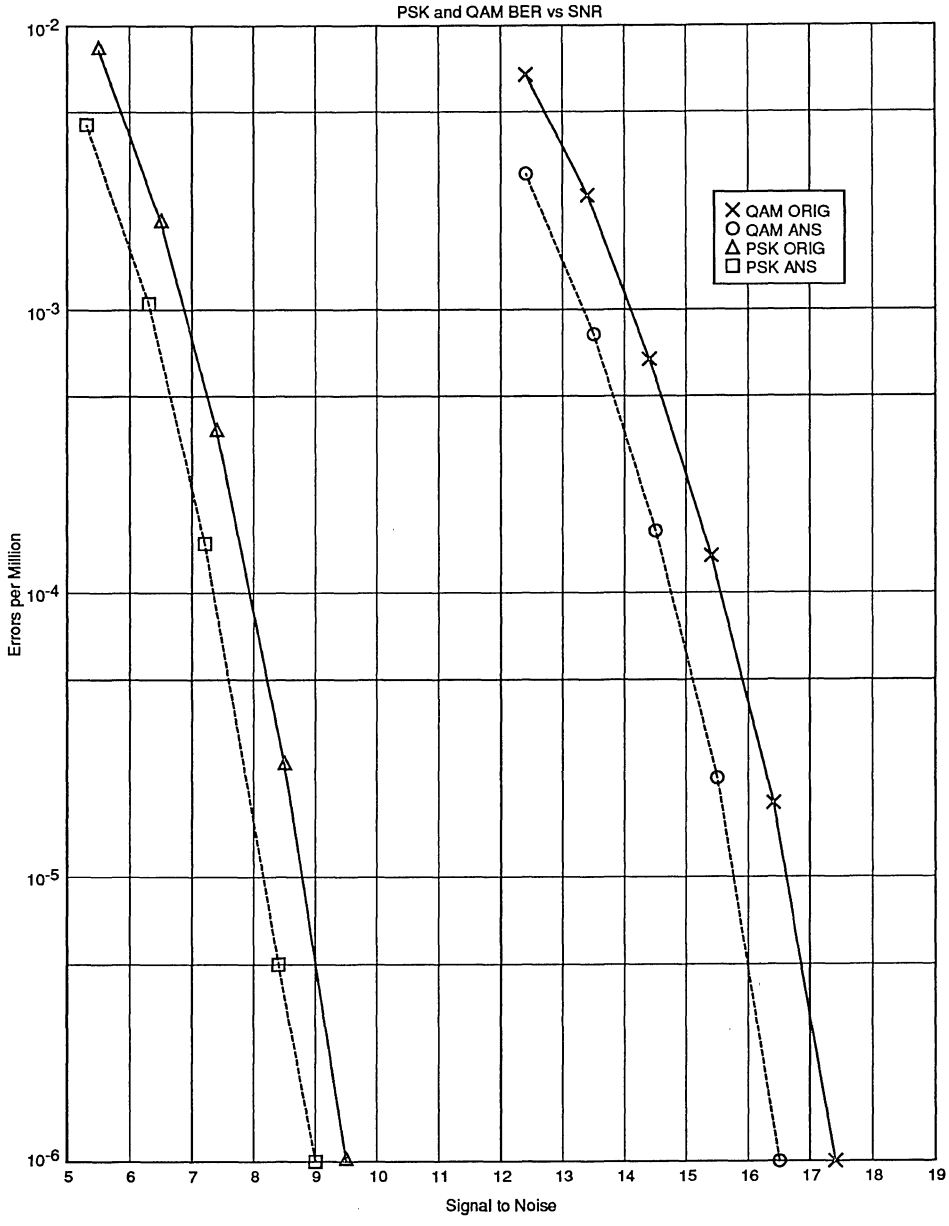


FIGURE 6: QAM and PSK BER vs. SNR with -20dBm Receive Level

APPLICATION INFORMATION

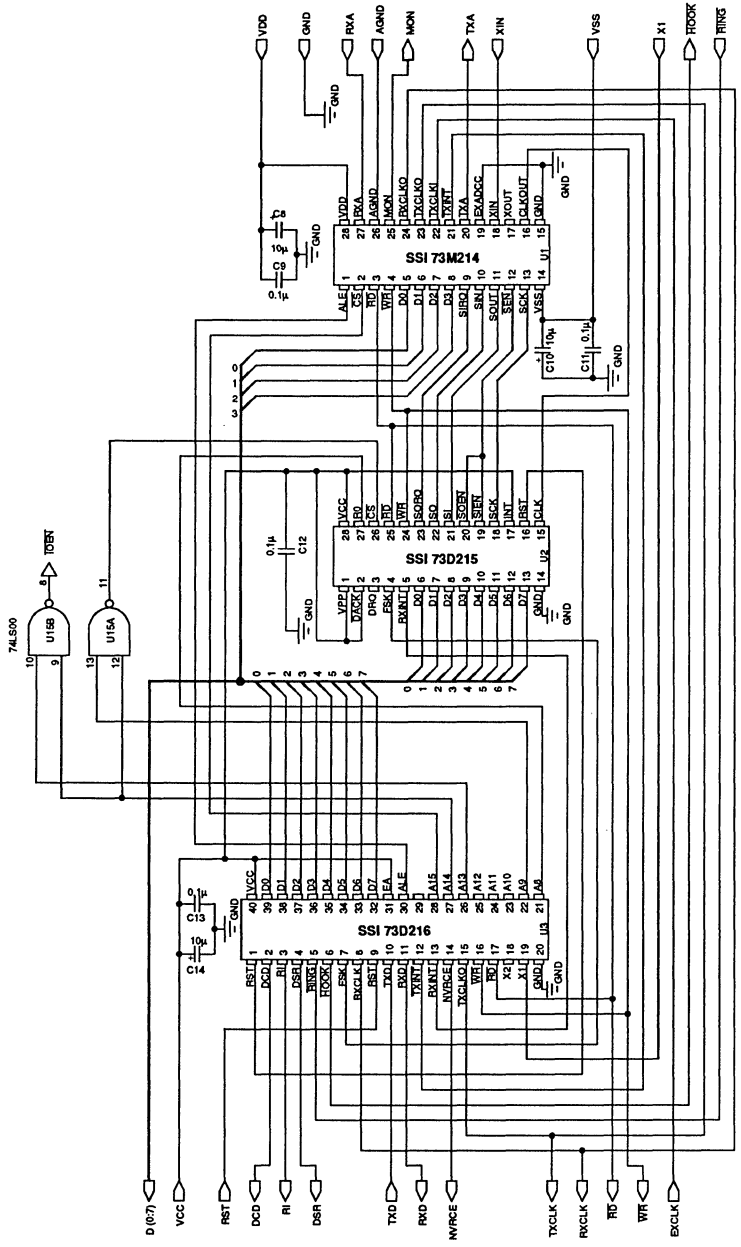


FIGURE 7: SSI 73D2404 System Interconnect

APPLICATION INFORMATION (Continued)

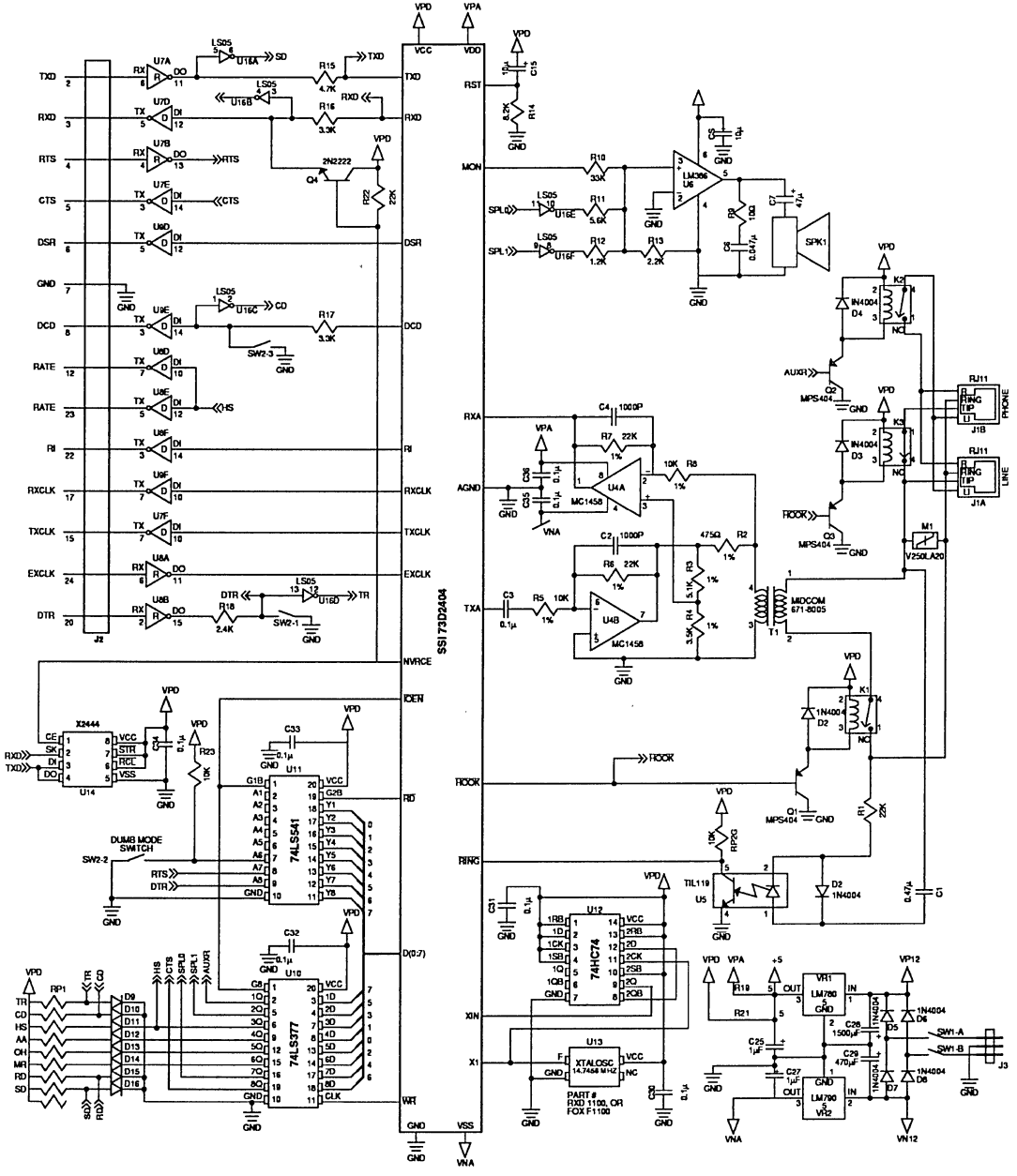
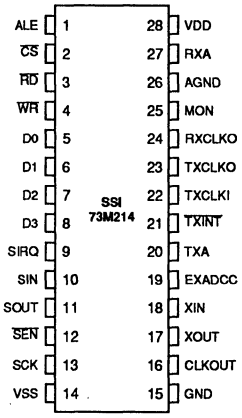
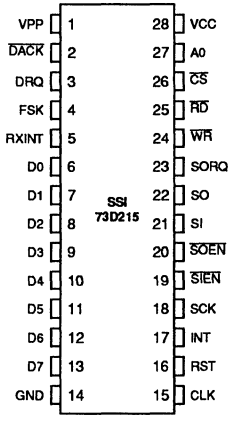


FIGURE 8: Sample Application Circuit

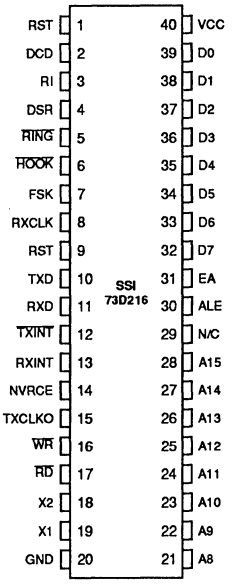
PACKAGE PIN DESIGNATIONS (TOP VIEW)



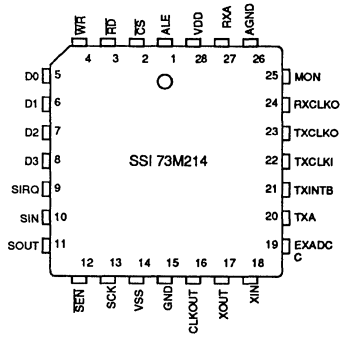
SSI 73M214
28-PIN DIP, CERDIP



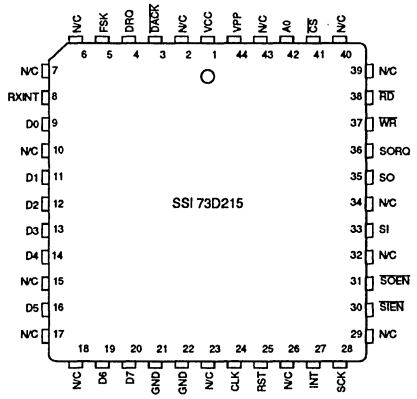
SSI 73D215
28-PIN DIP



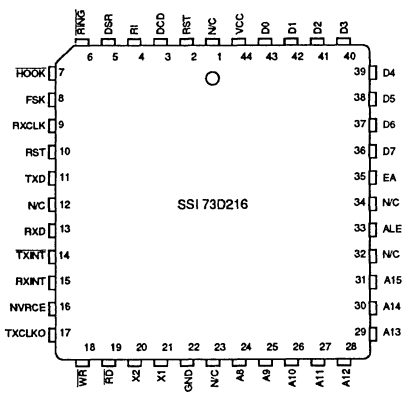
SSI 73D216
40-PIN DIP



SSI 73M214
28-PIN PLCC



SSI 73D215
44-PIN PLCC



SSI 73D216
44-PIN PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73D2404 Dual-In-Line Package	SSI 73D2404-CP	
28-pin Plastic DIP		73M214-IP
28-pin Plastic DIP		73D215-CP
40-pin Plastic DIP		73D216-CP
SSI 73D2404 Surface Mount Package	SSI 73D2404-CH	
28-pin Plastic Leaded Chip Carrier		73M214-IH
44-pin Plastic Leaded Chip Carrier		73D215-CH
44-pin Plastic Leaded Chip Carrier		73D216-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

Notes:

SSI 73D2407
MNP5 Controller and Modem Device Set
Advance Information

July, 1990

2

DESCRIPTION

The SSI 73D2407 consists of four CMOS integrated circuits which together provide the data pump functions required to construct a high performance 2400 bit/s full-duplex intelligent modem for use over the dial-up telephone network. The SSI 73D2407 includes operating modes compatible with CCITT V.22 bis, V.22, V.21, as well as Bell 212A and 103 data-communications standards. Using advanced CMOS processes that include analog, digital signal processing and switched capacitor filter techniques, the SSI 73D2407 offers excellent performance and a high level of functional integration in a compact four-chip set available in DIP or surface-mount packages.

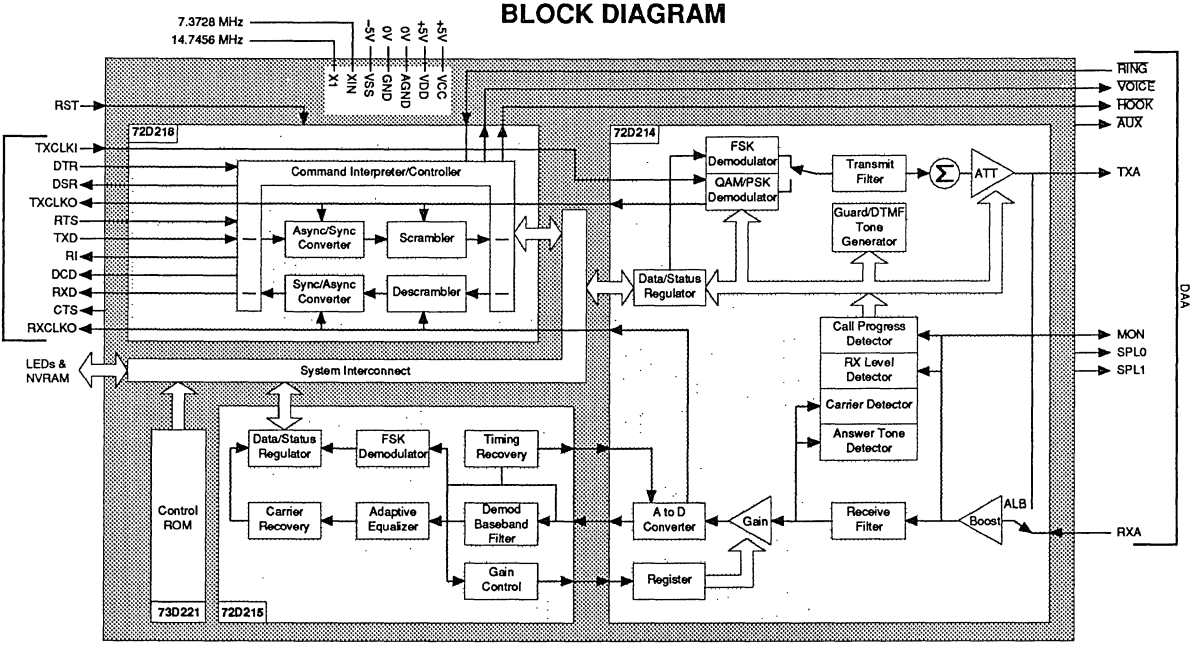
The SSI 73D2407 is ideal for use in both free-standing or integral system modem products where full-duplex 2400 bit/s data-communications over the 2-wire public service telephone network is desired.

FEATURES

- **Multi-mode V.22bis/V.22/V.21 & Bell 212A/103 compatible device set for intelligent modem designs**
- **Full duplex operation at 0-300, 1200 and 2400 bit/s with both sync & async operating modes**
- **Includes Microcom Networking Protocol (MNP) levels 4 and 5**
- **Includes high-level "AT" command interpreter compatible with 2400 bit/s industry standard products**
- **Supports external non-volatile memory to store user configurations**
- **Adaptive equalization for optimum performance over all lines**
- **Dynamic range from 0 to -45 dBm**
- **Call progress, carrier and answer tone detectors provide intelligent dialing functions**

(Continued)

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FEATURES (Continued)

- **DTMF and CCITT guard tone generators**
- **Test modes available – ALB, DL, RDL for complete test capability**
- **All CMOS for low power consumption**

OPERATION

The SSI 73D2407 is a complete V.22bis intelligent modem consisting of four CMOS ICs. The device set forms the basis for a high performance stand-alone modem product with self-contained command interpreter, indicator LEDs, default switches and interface lines for an RS-232 serial port. Both data and commands are passed over the serial port as in conventional intelligent modem designs. Error control of MNP4 and data compression are included.

The SSI 73D2407 provides the QAM, PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guard tones. This device supports the V.22 bis, V.22, V.21 and Bell 212A/103 operating modes, both synchronous and asynchronous. The SSI 73D2407 is designed to provide functions needed for an intelligent modem and includes auto-dial/auto-answer, handshake with auto-fallback, and selectable pulse or DTMF dialing sequences to simplify these designs.

The SSI 73D2407 consists of four devices. The SSI 73M214 is an analog processor that performs the filtering, timing adjustment, level detection and modulation functions. The SSI 73D215 is the receiver digital signal processor. The SSI 73D218 is a command processor that provides supervisory control and command interpretation. A SSI 73D221 ROM for code storage completes the package.

QAM MODULATOR/DEMODULATOR

The SSI 73D2407 scrambles and encodes the 2400 bit/s incoming data into quad bits represented by 16 possible signal points as specified by CCITT recommendation V.22 bis. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator recovers a data clock from the incoming signal and reverses this procedure. Adaptive equalization corrects for different line conditions by automatically changing filter parameters to compensate for line characteristics.

PSK MODULATOR/DEMODULATOR

In PSK mode the SSI 73D2407 modulates the 1200 bit/s incoming data using a subset of the QAM signal points as specified by CCITT recommendation V.22bis, V.22 and Bell 212A. The PSK demodulator is similar to the QAM demodulator.

FSK MODULATOR/DEMODULATOR

The FSK transmitter frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark & space) and 2225 and 2025 Hz (answer mark & space) or the V.21 standard frequencies of 980 and 1180 Hz (originate mark and space) and 1650 and 1850 Hz (answer mark and space) are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The data may be any value up to 300 bit/s.

PASSBAND FILTERS AND EQUALIZERS

A bandsplit filter is included to shape the amplitude and phase response of the transmit signal to a square root of 75% raised cosine and provide rejection of out-of-band signals in the receive channel.

ASYNCHRONOUS MODES

The asynchronous mode is used for communication between asynchronous terminals which may vary the data rate from +1.5% to –1.5% from the nominal 1200 or 2400 value. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal whose data rate is accurate to 0.01%. The signal is routed to a data scrambler (following the CCITT V.22 bis algorithm) and into the modulator. The SSI 73D2407 recognizes a break signal and handles it in accordance with BELL 212A specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits. An incoming break signal will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODES

Synchronous operation is possible with the PSK or QAM modes at 1200 or 2400 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the falling edge of TXCLK. Receive data at the RXD output is clocked out on the rising edge of RXCLK. The async/synch converter is bypassed when synchronous mode is selected.

AUTOMATIC HANDSHAKE

The SSI 73D2407 will automatically perform a complete handshake as defined by the V.22 bis, V.22 and Bell 212A/103 standards to connect with a remote modem. The SSI 73D2407 automatically determines the speed and operating mode and adjusts its operation to correspond to that of an answering modem when originating a call.

TEST MODES

The SSI 73D2407 allows use of Analog Loopback, Digital Loopback and Remote Digital Loopback test modes. Full test mode capability allows testing of the modem and interface functions from the local terminal using the analog loopback command, or remotely using the RDL command. The digital loopback command must be entered at the remote modem.

ADAPTIVE EQUALIZATION WITH AUTO-RETRAIN

The SSI 73D2407 uses adaptive equalization which automatically compensates for varying line characteristics by adjusting taps on a multi-tap FIR filter. Optimum performance is obtained with this technique over a wide range of line conditions. When the line quality deteriorates to a specified level the SSI 73D2407 can automatically initiate a retrain of the equalizer to re-establish data communications without the need to go through a complete handshake sequence.

"AT" COMMAND INTERPRETER

The SSI 73D2407 includes an AT command interpreter which is compatible with the Hayes 2400 Smartmodem™ command set. Functions and features included with intelligent modems are provided by the SSI 73D2407 command interpreter.

NON-VOLATILE MEMORY

The SSI 73D2407 supports connection to an external non-volatile memory (i.e., 93C46) to store a dial string and the current AT command configuration.

MICROCOM NETWORKING PROTOCOL

Error control features of the Microcom Networking Protocol (MNP) Level 4 and data compression Level 5 are available through AT commands. Throughput increases of up to 20% are available with MNP4 and 200% with MNP5. In either case, data passed is error-free.

SPEED/PROTOCOL COMPATIBILITY GUIDE

Calling a:		73D2407 Originating as:				
		Bell		CCITT		
		300	1200	300	1200	2400
Bell	300 (103)	300	300	-	-	300
	1200 (212)	300	1200	-	1200	1200
	2400[1] (224)	300	1200	-	1200	2400
CCITT	300 (V.21)	-	-	300	-	-
	1200 (V.22)	300	1200	-	1200	1200
	2400 (V.22bis)	300	1200	-	1200	2400
Called from a:		**73D2407 Answering as:**				
		Bell		CCITT		
		300	1200	300	1200	2400
Bell	300 (103)	300	300	-	-	300
	1200 (212)	300	1200	-	1200	1200
	2400 (224)	300	1200	-	1200	2400
CCITT	300 (V.21)	-	-	300	-	-
	1200 (V.22)	300	1200	-	1200	1200
	2400 (V.22bis)	300	1200	-	1200	2400

[1]Bell 2400 is the same as V.22bis using a 2225 Hz answer tone without unscrambled marks.

HARDWARE INTERFACE

POWER SUPPLIES AND CLOCKS

LABEL	I/O	PIN CONNECTION					DESCRIPTION
		73M214	73D215	73D218	73D221 DIP	73D221 SMT	
VDD	I			40			Positive supply (analog +5V)
VCC	I	28	28		28	32	Positive supply (digital +5V)
VSS	I	14					Negative supply (analog -5V)
AGND	I	26					Analog ground
GND	I	15	14	20	14	16	Digital ground
X1	I			19			Clock input 14.7456 MHz
XIN	I	18					Clock input 7.3728 MHz
RST	I			9			Reset (10 µF & 8.2 kΩ)

DAA INTERFACE

RXA	I	27					Receive analog from DAA
TXA	O	20					Transmit analog to DAA
MON	O	25					Audio monitor
SPL0	O			B.4*			Audio volume control
SPL1	O			B.5*			Audio volume control
$\overline{\text{RING}}$	I			5			From ring indicator
$\overline{\text{HOOK}}$	O			6			Off hook relay control
AUXR	O			B.7*			Auxiliary relay control

RS-232/V.24 INTERFACE

RI	O			3			Ring indicator output
RATE	O			B.3*			Indicates high speed
TXD	I			10			Digital data from terminal
RXD	O			11			Digital receive data
DCD	O			2			Data carrier detect
DSR	O			4			Data set ready
EXCLK	I	22					External Tx sync clock input
RXCLK	O	24		8			Receive clock ouptut
TXCLK	O	23		15			Transmit clock output
CTS	O			B.6*			Clear to send
RTS	I			B.6*			Request to send
DTR	I			B.7*			Indicates DTE available

* Available with expanded I/O

HARDWARE INTERFACE (Continued)

LED DISPLAY

LABEL	I/O	PIN CONNECTION					DESCRIPTION
		73M214	73D215	73D218	73D221 DIP	73D221 SMT	
$\overline{WR}$	O	4	24	16			Write strobe (active low)
TR	LED	Performed externally					Data terminal ready
SD	LED			1			Transmit data
RD	LED			11			Receive data
CD	LED			2			Data carrier detect
HS	LED			B.3*			High speed indicator
MR	LED			B.2*			Modem ready/test in progress
AA	LED			B.1*			Auto answer indicator
OH	LED			B.0*			Off hook indicator

NVRAM INTERFACE

NVRCE	O			14			NVRAM CE (active high)
TXD	I/O			10			NVRAM DI/DO
RXD	I			11			NVRAM SK

* Available with expanded I/O

DEVICE SET INTERCONNECT

LABEL	I/O*	PIN CONNECTION					DESCRIPTION
		73M214	73D215	73D218	73D221 DIP	73D221 SMT	
VPP	I		1		1	2	+5V
INT	I		17				+5V
$\overline{EA}$	I			31			+5V
EXADCC	I	19					0V
$\overline{DACK}$	I		2				+5V
CLK	S	16	15				7.3728 MHz
$\overline{RXINT}$	S		5	13			RX Interrupt
$\overline{TXINT}$	S	21		12			TX Interrupt
RST	S		16				
FSK	S		4	7			
$\overline{RD}$	S	3	25	17	22	25	
$\overline{WR}$	S	4	24	16			

DEVICE SET INTERCONNECT (Continued)

LABEL	I/O*	PIN CONNECTION					DESCRIPTION
		73M214	73D215	73D218	73D221 DIP	73D221 SMT	
D0	I/O	5	6	39	11	13	Data Bus 0
D1	I/O	6	7	38	12	14	Data Bus 1
D2	I/O	7	8	37	13	15	Data Bus 2
D3	I/O	8	9	36	15	18	Data Bus 3
D4	I/O		10	35	16	19	Data Bus 4
D5	I/O		11	34	17	20	Data Bus 5
D6	I/O		12	33	18	21	Data Bus 6
D7	I/O		13	32	19	22	Data Bus 7
SIN	S	10	22				
SOUT	S	11	21				
SIRQ	S	9	23				
SCK	S	13	18				
$\overline{SEN}$	S	12	19, 20				
A0	S				10	11	Address Bus 0
A1	S				9	10	Address Bus 1
A2	S				8	9	Address Bus 2
A3	S				7	8	Address Bus 3
A4	S				6	7	Address Bus 4
A5	S				5	6	Address Bus 5
A6	S				4	5	Address Bus 6
A7	S				3	4	Address Bus 7
A8 (AH0)	S		27	21	25	29	Address Bus 8
A9 (AH1)	S				24	28	Address Bus 9
A10(AH2)	S				21	24	Address Bus 10
A11 (AH3)	S				23	27	Address Bus 11
A12 (AH4)	S				2	3	Address Bus 12
A13 (AH5)	S				26	30	Address Bus 13
A14 (AH6)	S			7	27	31	Address Bus 14
A15 (AH7)	S						Address Bus 15
$\overline{CE}$	I				20	23	GND

* "S" Refers to system interconnect.

AT COMMAND SUMMARY*

Command	Description
AT	command prefix – precedes command line
<CR>	carriage return character – terminates command line
A	go into answer mode; attempt to go to on-line state
A/	re-execute previous command line; not preceded by AT nor followed by <CR>
B0	select CCITT V.22 standard for 1200 bit/s communication
B1	***select Bell 212A standard for 1200 bit/s communication***
D	dial number that follows; attempt to go to on-line state, originate mode
DS=n	dial stored number in location "n" (0-3)
E0	Disable character echo in command state
E1	***Enable character echo in command state***
H0	go on hook (hang up)
H1	go off hook; operate auxiliary relay
I0	request product indentification code
I1	perform checksum on firmware ROM; return checksum
I2	perform checksum on firmware ROM; returns OK or ERROR result codes
L0 or L1	low speaker volume
L2	***medium speaker volume***
L3	high speaker volume
M0	speaker off
M1	***speaker on until carrier detected***
M2	speaker always on
M3	speaker on until carrier detected, except during dialing
O0	go to on-line state
O1	go to on-line state and initiate equalizer retrain at 2400 bit/s
Q0	***modem returns result codes***
Q1	modem does not return result codes
Sr	set pointer to register "r"
Sr=n	set register "r" to value "n"
Sr?	display value stored in register "r"
V0	display result codes in numeric form
V1	***display result codes in verbose form (as words)***
X0	enable features represented by result codes 0-4
X1	enable features represented by result codes 0-5, 10-12
X2	enable features represented by result codes 0-6, 10-12
X3	enable features represented by result codes 0-5, 7, 10-12
X4	***enable features represented by result codes 0-7, 10-12***
Y0	***disable long space disconnect***
Y1	enable long space disconnect
Z0	reset modem
&C0	***assume data carrier always present***
&C1	track presence of data carrier
&D0	***ignore DTR signal***
&D1	assume command state when an on-to-off transition of DTR occurs
&D2	hang up and assume command state when an on-to-off transition of DTR occurs
&D3	reset when an on-to-off transition of DTR occurs
&F	recall factory settings as active configuration
&G0	***no guard tone***
&G1	550 Hz guard tone
&G2	1800 Hz guard tone
&J0	***RJ-11/RJ-41S/RJ-45S telco jack***
&J1	RJ-12/RJ-13 telco jack
&M0	***asynchronous mode***
&M1	synchronous mode 1
&M2	synchronous mode 2
&M3	synchronous mode 3
&T0	terminate test in progress
&T1	initiate local analog loopback
&T3	initiate local digital loopback
&T4	***grant request from remote modem for RDL***
&T5	deny request from remote modem for RDL
&T6	initiate remote digital loopback
&T7	initiate remote digital loopback with self test
&T8	initiate local analog loopback with self test
&V	view active configuration, user profiles, and stored numbers
&W0	save storable parameters of active configuration
&X0	***modem provides transmit clock signal***
&X1	data terminal provides transmit clock signal
&X2	receive carrier provides transmit clock signal
&Zn=x	store phone number "x" in location "n" (0-3)

MNP COMMANDS

Command	Description
%A	Auto-Reliable fallback character
%C	compression control
\A	maximum block size
\G	modem port flow control
\J	rate adjust
\K	break control
\N	operating mode
\O	originate Reliable Link
\Q	flow control
\T	inactivity timer
\U	accept Reliable Link
\V	result code form
\X	XON/XOFF pass-through
\Y	switch to Reliable mode
\Z	switch to Normal mode

Note: ***Italicized*** parameters indicate default settings. If a parameter (0, 1, etc.) is not specified, the modem assumes the 0 parameter.

* Hayes Standard AT Command Set as implemented in Hayes Smartmodem 2400

Dial string arguments:

, = delay	@ = silent answer	! = flash	
; = return to command	s = dial stored number	W = wait for tone	R=reverse mode

If the NovRAM has not been initialized it may be necessary to Power down/Power up and type *AT&F&W<cr>* to properly initialize modem state.

TABLE 1: Result Codes

Xn	VERBOSE/TERSE RESULT CODES
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6, NO ANSWER/8

TABLE 2: S Registers Supported

Sn	FUNCTION	UNITS	DEFAULT
S0[1]	Answer on ring	No. of rings on which to answer	000[2]
S1	Ring counter	No. of rings accumulated	000
S2	Escape code	ASCII CHR Decimal 0-127	043
S3	Carriage return	ASCII CHR Decimal 0-127	013
S4	Line feed	ASCII CHR Decimal 0-127	010
S5	Back space	ASCII CHR	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds (0.1 sec)	006
S10	Carrier drop out	100 milliseconds (0.1 sec)	014
S11	DTMF tone duration	1 millisecond (0.001 sec)	070
S12	Escape guard time	20 milliseconds (0.05 sec)	050
S13	Unused		N/A
*S14[1]	Bit mapped register	Decimal 0-255	170

1 Stored in NVRAM with &W command.
2 Modem will not answer until value is changed to 1 or greater.

TABLE 2: S Registers Supported (Continued)

NUMBER	FUNCTION	UNITS	DEFAULT
S15	Unused		N/A
S16	Test register	Decimal #	000
S17	SSi Special test register	Decimal 0-255	096
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[1]	Bitmapped register	Decimal 0-255	000
*S22[1]	Bitmapped register	Decimal 0-255	118
*S23[1]	Bitmapped register	Decimal 0-255	007
S24	Unused		N/A
S25[1]	DTR delay	10 milliseconds (0.01 sec)	005
S26[1]	CTS delay	10 milliseconds (0.01 sec)	001
*S27[1]	Bitmapped register	Decimal 0-255	064
S37	Desired Modem Line Speed	Decimal 0-3	000

* The bitmapped register functions are equivalent to normal "AT" command modem registers. They are not needed for evaluation of the 73D2407 capabilities.

Asynchronous character formats supported:
[Number of data bits, parity (even/odd/none), number of stop bits]

1200/2400 bit/s: 7N2, 7E1, 7O1, 8N1

300 bit/s: 7N2, 7E1, 7O1, 8N1, 8E1, 8O1

[1] Stored in NVRAM with &W command

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
T_A, Ambient Temperature		0		70	°C
V_{CC} & V_{DD}, Supply Voltage	73M214, 73D215, 73D218, 73D221	4.75		5.25	V
V_{SS}, Supply Voltage	73M214	–4.25		–5.25	V
V_{DD}, V_{SS} Bypass Capacitors		10+0.1			µF
CLK Load Capacitance				25	pF
Digital Load Capacitance				50	pF
TXA, MON Loading				See Note	
Input Clock Frequency (X1)			14.7456		MHz
Input Clock Variation (X1, XIN)	XIN must be X1 ÷ 2	–0.01		0.01	%

Note: 10 kΩ in parallel with 50 pF

INPUT CLOCK TIMING (See Figure 1.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
TCLCX		20			ns
TCLCX2		54		82	ns
TCHCX		20			ns
TCHCX2		54		82	ns
TR, TF				15	ns
TCHCH		0		20	ns

INTERFACE TIMING

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
LED Write Timing (See Figure 2.)						
TWLWH	$\overline{WR}$ pulse width		307			ns
TAVWL	Address valid to $\overline{WR}$ low		141			ns
TQVWH	Data valid to $\overline{WR}$ high		370			ns
TQVWX	Data valid to $\overline{WR}$ transition		27			ns
TWHDX	Data hold after $\overline{WR}$		86			ns

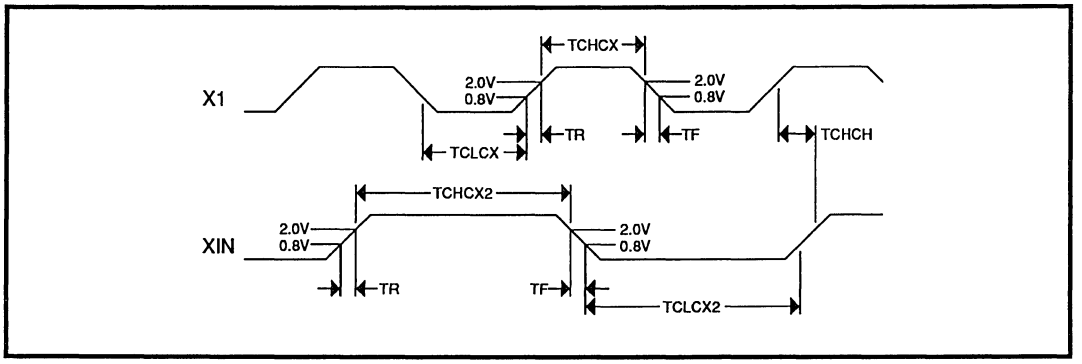


FIGURE 1: Input Clock Timing

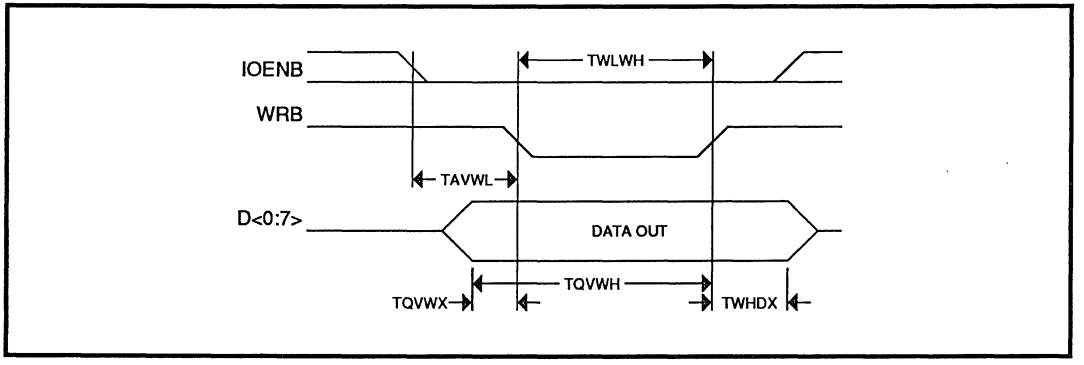


FIGURE 2: LED Write Timing

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
I_{DD}	Supply Current				130	mA
I_{SS}					25	mA
V_{IL}	Input Low Voltage		0		0.8	V
V_{IH}	Input High Voltage		2.0		VDD	V
I_{IH}	Input High Current	Except $\overline{CS}$ which has a pulldown of 20 kΩ			10	µA
I_{IL}	Input Low Current	Except TXCLKI, EXADCC which have pullups of 20 kΩ			-20	µA
	Digital Input Capacitance				10	pF
V_{OH}	Output High Voltage	Iout = -.4 mA	2.4			V
V_{OL}	Output Low Voltage	Iout = 1.6 mA			0.4	V
RXA	Input Resistance		100			kΩ
RXA	Input Capacitance				25	pF

TRANSMITTER SPECIFICATIONS

TRANSMITTER POWER

(Values given are measured at the line connection point and assume that the DAA shown in our application literature is used with a 600 Ω load.)

TRANSMITTER POWER	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Transmitter Power	With or without CCITT tones	–9.8		–8.2	dBm
CCITT Guard Tone	550	–14.8		–12.8	dBm
	1800	–16.0		–14.0	dBm
FSK Transmitter Power	103/V.21	–10.0		–8.0	dBm
Answer Tone Power		–10.0		–8.0	dBm
DTMF Transmitter Power	High Band Tones	–7.0		–5.0	dBm
	Low Band Tones	–9.0		–7.0	dBm
	Twist	–3.0		–1.0	dB

TRANSMITTER FREQUENCY
(All tones are digitally derived from the clock input and have the input clock frequency tolerance.)

TRANSMITTER FREQUENCY		CONDITIONS		MIN	NOM	MAX	UNITS
QAM/DPSK Carrier Frequencies		Originate			1200.0		Hz
		Answer			2400.0		Hz
FSK Tone Frequencies							
103	Originate	Space	1070		1066.7		Hz
		Mark	1270		1269.4		Hz
	Answer	Space	2025		2021.1		Hz
		Mark	2225		2226.1		Hz
V.21	Originate	Space	1180		1181.6		Hz
		Mark	980		978.3		Hz
	Answer	Space	1850		1850.0		Hz
		Mark	1650		1651.6		Hz
Special Tone Frequencies							
Answer Tone			2100		2104.1		Hz
CCITT Guard Tones			550		556.5		Hz
			1800		1786.0		Hz
DTMF Dialing Tone Frequencies							
Low Group		Columns	697		698.2		Hz
			770		771.9		Hz
			852		853.3		Hz
			941		942.3		Hz
High Group		Rows	1209		1209.5		Hz
			1336		1335.7		Hz
			1477		1476.9		Hz
			1663		1634.0		Hz

TRANSMITTER DISTORTION

TRANSMITTER DISTORTION	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Carrier Suppresion	Measured at TXA	35			dB
CCITT Guard Tone Distortion	800-1600 Hz band			–60	dB
	0-10 kHz band			–45	dB
Answer Tone Distortion	800-1600 Hz band			–60	dB
	0-10 kHz band			–40	dB
FSK Output Bias Distortion	Transmit dotting 300 bit/s	–6		6	%
FSK Opposite Band Distortion				–60	dB
DTMF Tone Distortion	700-2900 Hz band			–29	dB

RECEIVER SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier VCO					
Capture Range	Carrier offset	–10		10	Hz
Carrier Phase Jitter	50-65 Hz			30	Degrees
Data Clock Recovery Capture Range	From system clock ÷ 24576 (600 Hz symbol clock)	-.025		+.025	%
Data Delay Time	RXA to RXD	30		75	ms
Retrain Request Threshold	If enabled	10-3		10-2	BER
Carrier Detect					
Threshold		–48		–43	dBm
Hysteresis		2			dB
Answer Tone Detect	2100/2225 Hz				
Threshold		–48		–43	dBm
Hysteresis		2			dB
Call Progress Detect	350-650 Hz dual tone				
Threshold		–40		–30	dBm
Hysteresis		2			dB

PERFORMANCE DATA

(This performance data was taken using an AEA tester and the SSI 73D2404 MEU board.)

BER PERFORMANCE

(–20 dBm receive level, 10^{-5} BER)

PARAMETER	MINIMUM SNR REQUIRED
2400 bit/s Originate	16.5 dB SNR
2400 bit/s Answer	16.0 dB SNR
1200 bit/s Originate	9.0 dB SNR
1200 bit/s Answer	8.0 dB SNR
0-300 bit/s Originate	9.0 dB SNR
0-300 bit/s Answer	7.5 dB SNR

DYNAMIC RANGE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
2400 bit/s Originate	10^{-5} BER @ 17dB SNR	–45		0	dBm
2400 bit/s Answer	10^{-5} BER @ 17dB SNR	–45		0	dBm
1200 bit/s Originate	10^{-5} BER @ 12dB SNR	–45		0	dBm
1200 bit/s Answer	10^{-5} BER @ 12dB SNR	–45		0	dBm
0-300 bit/s Originate	10^{-5} BER @ 12dB SNR	–45		0	dBm
0-300 bit/s Answer	10^{-5} BER @ 12dB SNR	–45		0	dBm

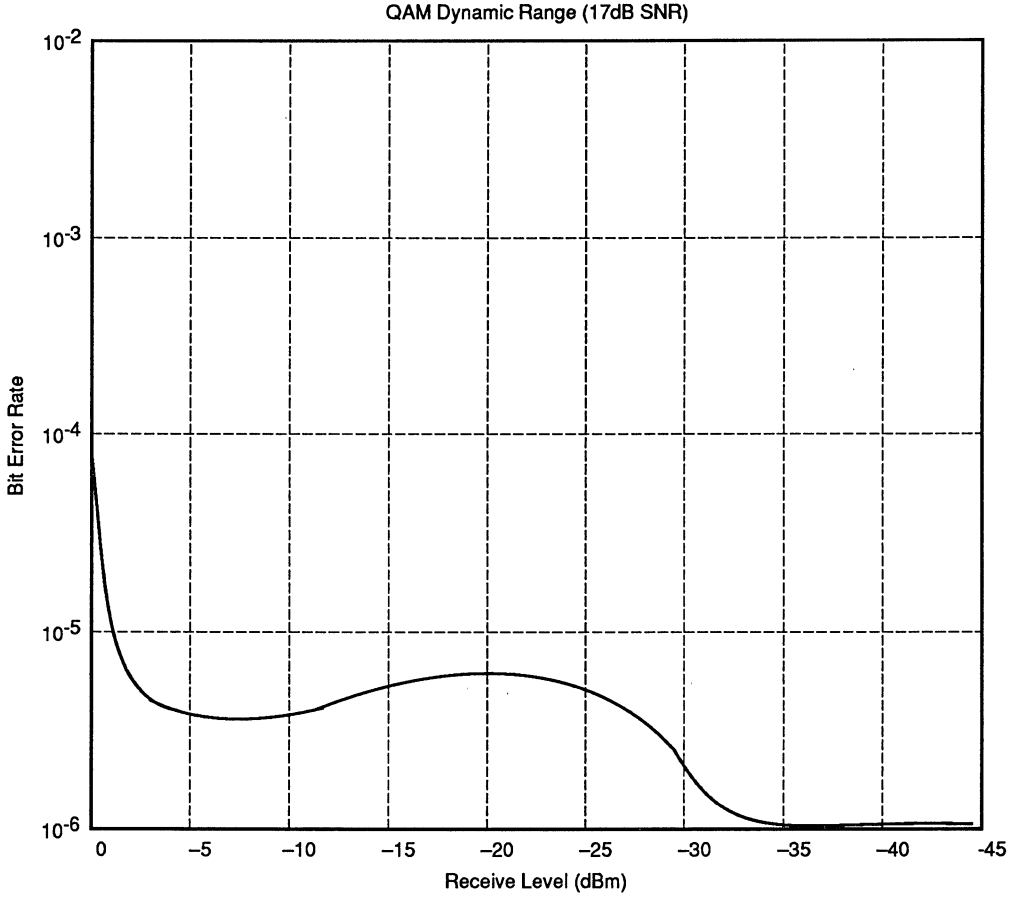


FIGURE 4: QAM Dynamic Range

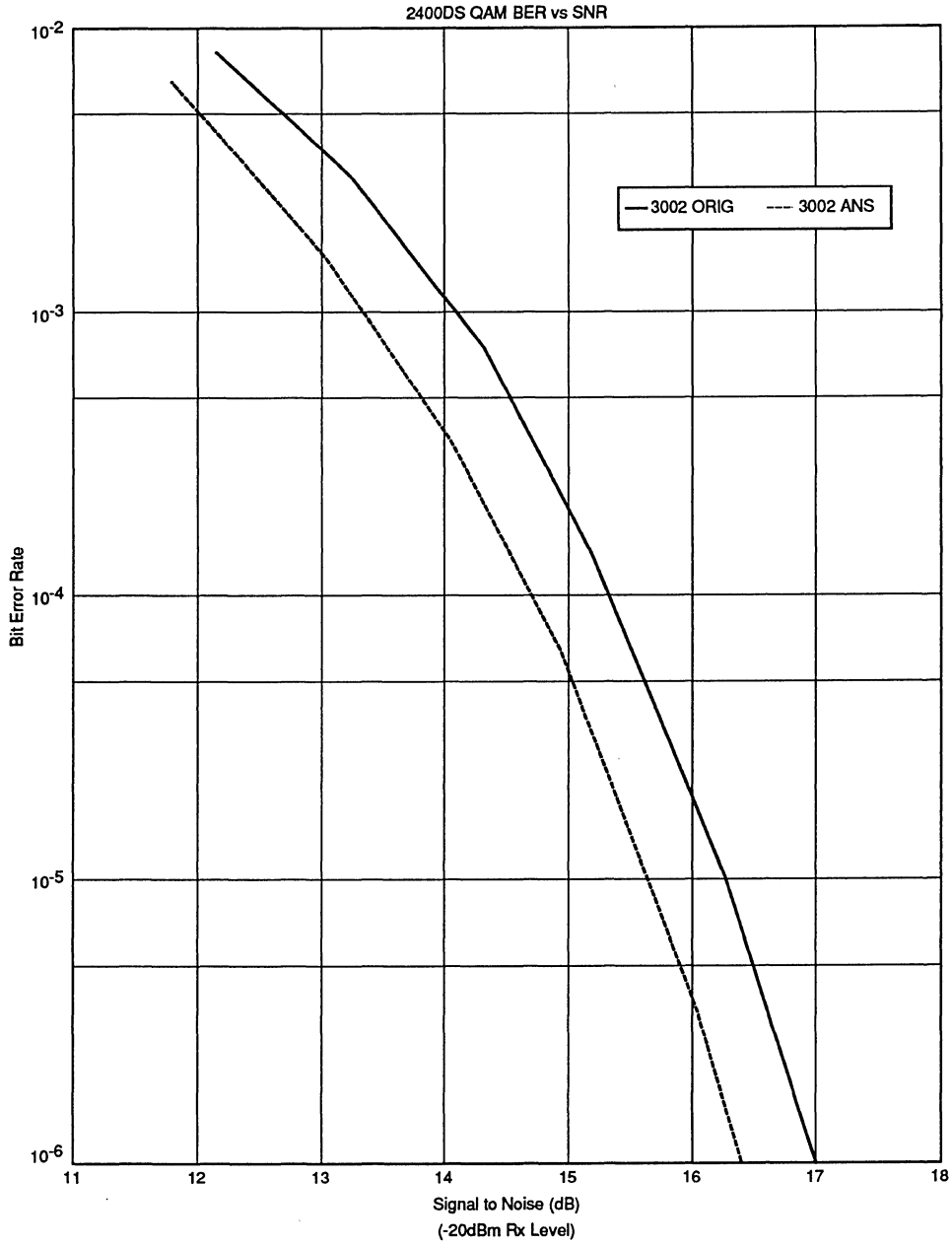


FIGURE 5: BER vs. SNR

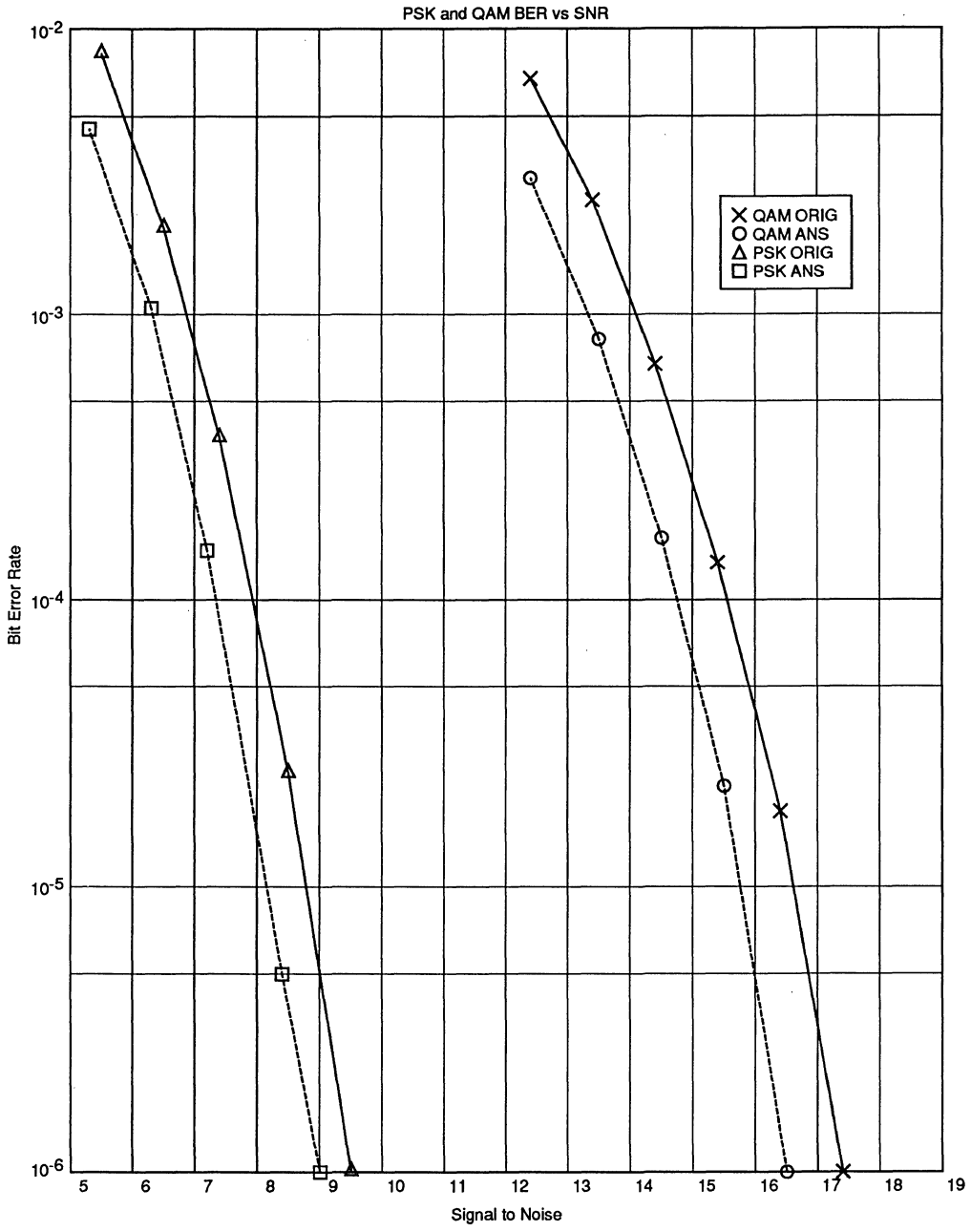
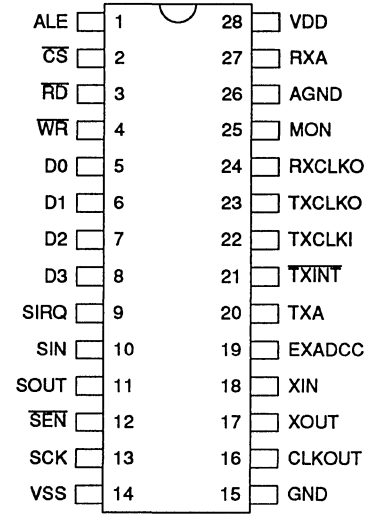
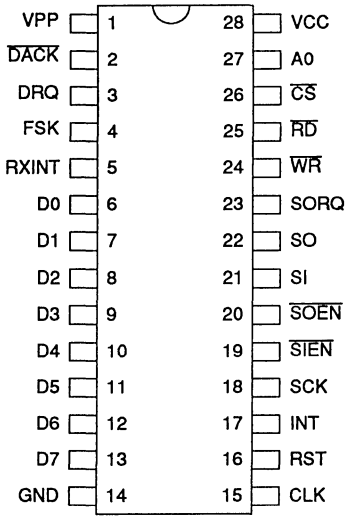


FIGURE 6: QAM and PSK BER vs. SNR with -20 dBm Receive Level

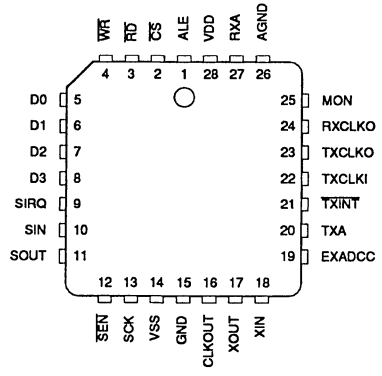
PACKAGE PIN DESIGNATIONS (TOP VIEW)



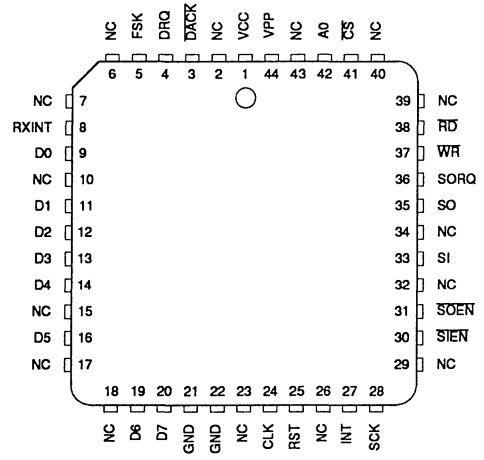
SSI 73M214
28-PIN DIP



SSI 73D215
28-PIN DIP



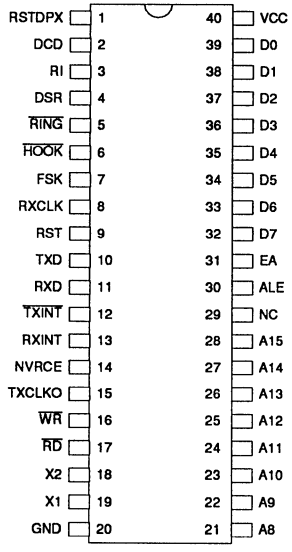
SSI 73M214
28-PIN PLCC



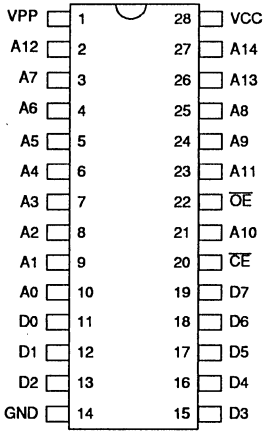
SSI 73D215
44-PIN PLCC

SSI 73D2407
MNP5 Controller and Modem Device Set

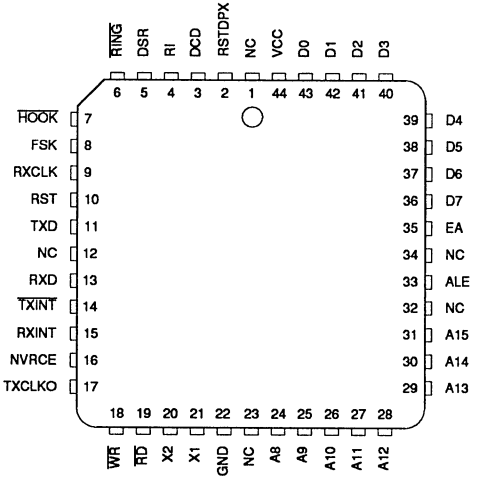
PACKAGE PIN DESIGNATIONS (TOP VIEW)



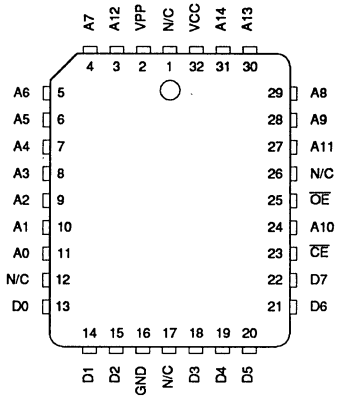
SSI 73D218
40-PIN DIP



SSI 73D221
28-PIN DIP



SSI 73D218
44-PIN PLCC



SSI 73D221
32-PIN PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

Notes:

SSI 73D2417
MNP5 Datacom/FAX Modem Device Set
Preliminary Data

July, 1990

2

DESCRIPTION

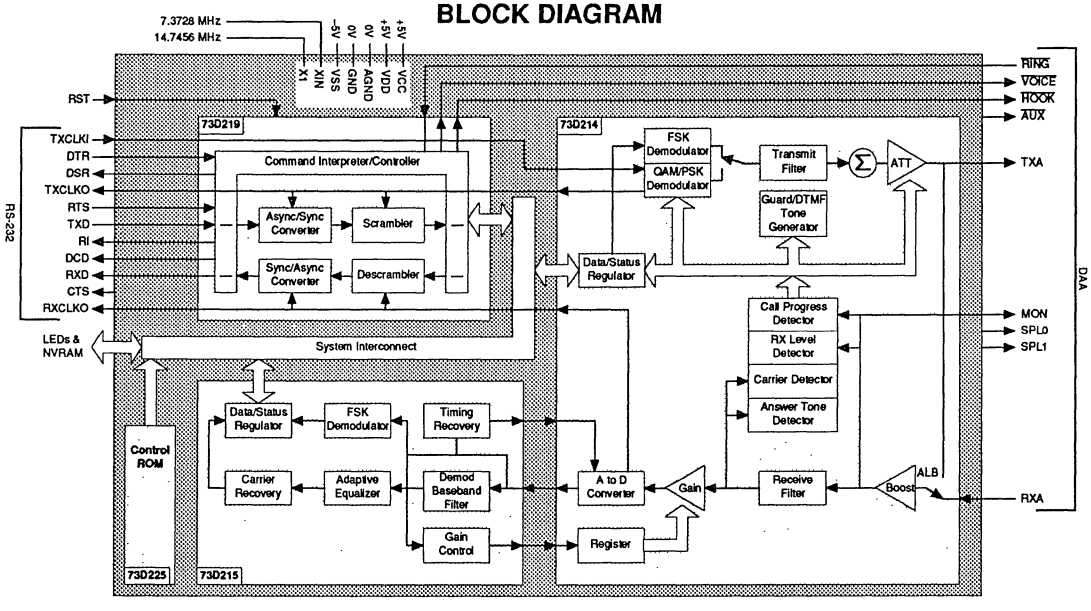
The SSI 73D2417 is a 4-chip CMOS device set that combines 2400 bit/s smart modem functions, including MNP 5, with FAX transmit capability. The 73D2417 includes operating modes compatible with V.22bis, V.22, V.21, and Bell 212A/103 communications standards. The 73D2417 also complies with V.27 ter FAX standards for transmit only FAX operation at 4800 and 2400 bit/s. All user interface and modem protocol is included in the 73D2417 to provide a turnkey modem/FAX design. In datacom mode, the 73D2417 command interpreter provides an AT command set compatible with industry standard software. MNP 5 capability can also be used during data communication to provide error free data transfer and compression, increasing the effective data throughput. In FAX mode, the 73D2417 provides a send only FAX function, operating at speeds of 4800 or 2400 bit/s, that can transmit to conventional FAX machines. The 73D2417 includes a subset of the industry standard AT user interface commands as defined by EIA/TIA, and is compatible

(continued)

FEATURES

- **2400 bit/s data communication, MNP5, and FAX capability combined in one product**
- **Multimode V.22bis/V.22/V.21, and Bell 212A/103 data com**
- **Microcom Networking Protocol (MNP) level 4 and 5 error control and data compression**
- **V.27ter FAX transmit capability at 4800/2400 bit/s rates for text, ASCII, or graphic files**
- **Standard 2400 bit/s AT and TIA/EIA Class 2 (FAX AT) command sets and features for software compatibility**
- **Supports external NVRAM for nonvolatile storage of user setup configurations**
- **Compact DIP or PLCC packages for surface mount designs**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

with existing terminal software. The SSI 73D2417 is designed to provide an economical, high performance solution for applications needing both datacom and FAX capability. Its high level of performance and integrated features make it ideal for use in personal computer, portable terminal, and laptop FAX applications which communicate using the dialup telephone network.

OPERATION

The SSI 73D2417 is a complete datacom/FAX capable "smart" modem with MNP5 functions included in four CMOS ICs. The device set forms the basis for a high performance stand alone modem/FAX product with self contained AT command interpreter and features, RS232 or UART interface lines, and expansion for NVRAM for storage of default parameters.

MNP5 error control and data compression is included in datacom modes, and an EIA/TIA industry standard AT user interface is provided in FAX mode for compatibility with conventional software.

The SSI 73D2417 provides the QAM, PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guard tones. This device supports the V.22bis, V.22, V.21 and Bell 212A/103 operating modes, both synchronous and asynchronous. The SSI 73D2417 is designed to provide functions needed for an intelligent modem and includes auto-dial/auto-answer, handshake with auto-fallback, and selectable pulse or DTMF dialing sequences to simplify these designs.

The SSI 73D2417 consists of four devices. The SSI 73M214 is an analog processor that performs the filtering, timing adjustment, level detection and modulation functions. The SSI 73D215 is the receiver digital signal processor. The SSI 73D219 is a command processor that provides supervisory control and command interpretation. A SSI 73D225 ROM provides storage for internal control software.

QAM MODULATOR/DEMODULATOR

The SSI 73D2417 scrambles and encodes the 2400 bit/s incoming data into quad bits represented by 16 possible signal points as specified by CCITT recommendation V.22bis. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator recovers a data clock from the incoming signal and reverses this procedure. Adaptive equalization corrects for different line conditions by automatically changing filter parameters to compensate for line characteristics.

PSK MODULATOR/DEMODULATOR

In PSK mode the SSI 73D2417 modulates the 1200 bit/s incoming data using a subset of the QAM signal points as specified by CCITT recommendation V.22bis, V.22 and Bell 212A. For FAX operation, the modulator conforms to V.27 ter signal point locations. The PSK demodulator is similar to the QAM demodulator.

FSK MODULATOR/DEMODULATOR

The FSK transmitter frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark & space) and 2225 and 2025 Hz (answer mark & space) or the V.21 standard frequencies of 980 and 1180 Hz (originate mark and space) and 1650 and 1850 Hz (answer mark and space) are used when this mode is selected. Demodulation involves detecting the receive frequencies and decoding them into the appropriate binary value. The speed rate may be any up to 300 bit/s.

PASSBAND FILTERS AND EQUALIZERS

A bandsplit filter is included to shape the amplitude and phase response of the transmit signal to a square root of 75% raised cosine and provide rejection of out-of-band signals in the receive channel.

ASYNCHRONOUS MODES

The asynchronous mode is used for communication between asynchronous terminals which may vary the data rate from +1.5% to -2.3% from the nominal 1200 or 2400 value. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal whose data rate is accurate to 0.01%. The signal is routed to a data scrambler (following the CCITT V.22bis algorithm) and

into the modulator. The SSI 73D2417 recognizes a break signal and handles it in accordance with BELL 212A specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits. An incoming break signal will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODES

Synchronous operation is possible with the PSK or QAM mode at 1200 or 2400 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the falling edge of TXCLK. Receive data at the RXD output is clocked out on the rising edge of RXCLK. The async/synch converter is bypassed when synchronous mode is selected.

AUTOMATIC HANDSHAKE

The SSI 73D2417 will automatically perform a complete handshake as defined by the V.22bis, V.22 and Bell 212A/103 standards to connect with a remote modem. The SSI 73D2417 automatically determines the speed and operating mode and adjusts its operation to correspond to that of an answering modem when originating a call.

TEST MODES

The SSI 73D2417 allows use of Analog Loopback, Digital Loopback and Remote Digital Loopback test modes. Full test mode capability allows testing of the modem and interface functions from the local terminal using the analog loopback command, or remotely using the RDL command. The digital loopback command must be entered at the remote modem.

ADAPTIVE EQUALIZATION WITH AUTO-RETRAIN

The SSI 73D2417 uses adaptive equalization which automatically compensates for varying line characteristics by adjusting taps on a multi-tap FIR filter. Optimum performance is obtained with this technique over a wide range of line conditions. When the line quality deteriorates to a specified level the SSI 73D2417 can automatically initiate a retrain of the equalizer to re-establish data communications without the need to go through a complete handshake sequence.

AT COMMAND INTERPRETER

The SSI 73D2417 includes an AT command interpreter which is compatible with the Hayes 2400 Smartmodem™ command set. Functions and features included with intelligent modems are provided by the SSI 73D2417 command interpreter.

NON-VOLATILE MEMORY

The SSI 73D2417 supports connection to an external non-volatile memory (i.e., 93C46) to store a dial string and the current AT command configuration.

MICROCOM NETWORKING PROTOCOL

Error control features of the Microcom Networking Protocol (MNP) Level 4 and data compression Level 5 are available through AT commands. Throughput increases of up to 20% are available with MNP4 and 200% with MNP5. In either case, data passed is error-free.

FAX TRANSMIT CAPABILITY

The 73D219 Controller, when operating in FAX mode, sends data to a digital-to-analog converter, the output of which is converted from a current to a voltage and filtered to emulate the output of a V.27 FAX modulator. This, in conjunction with the 300 bit/s capability of the basic modem, provides the hardware necessary to communicate with a FAX machine at 2400 or 4800 bit/s. Firmware necessary to dial a FAX call, determine the capabilities of the remote receiver and pass the FAX traffic is included.

SPEED/PROTOCOL COMPATIBILITY GUIDE

Calling a:			73D2417 Originating as:				
			Bell		CCITT		
			300	1200	300	1200	2400
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400[1]	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22bis)	300	1200	-	1200	2400
Called from a:			**73D2417 Answering as:**				
			Bell		CCITT		
			300	1200	300	1200	2400
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22bis)	300	1200	-	1200	2400

[1] Bell 2400 is the same as V.22bis using a 2225 Hz answer tone without unscrambled marks.

HARDWARE INTERFACE

DEVICE SET INTERCONNECT

LABEL	I/O*	PIN CONNECTION					DESCRIPTION
		73M214	73D215	73D218	73D221 DIP	73D221 SMT	
VPP	I		1		1	2	+5V
INT	I		17				+5V
$\overline{EA}$	I			31			+5V
EXADCC	I	19					GND
$\overline{DACK}$	I		2				+5V
CLK	S	16	15				7.3728 MHz
$\overline{RXINT}$	S		5	13			Rx Interrupt
$\overline{TXINT}$	S	21		12			Tx Interrupt
RST	S		16	1			
FSK	S		4	7			
$\overline{RD}$	S	3	25	17	22	25	
$\overline{WR}$	S	4	24	16			
D0	I/O	5	6	39	11	13	Data Bus 0
D1	I/O	6	7	38	12	14	Data Bus 1
D2	I/O	7	8	37	13	15	Data Bus 2
D3	I/O	8	9	36	15	18	Data Bus 3
D4	I/O		10	35	16	19	Data Bus 4
D5	I/O		11	34	17	20	Data Bus 5
D6	I/O		12	33	18	21	Data Bus 6
D7	I/O		13	32	19	22	Data Bus 7
SIN	S	10	22				
SOUT	S	11	21				
SIRQ	S	9	23				
SCK	S	13	18				
$\overline{SEN}$	S	12	19,20				
A0	S				10	11	Address Bus 0
A1	S				9	10	Address Bus 1
A2	S				8	9	Address Bus 2
A3	S				7	8	Address Bus 3
A4	S				6	7	Address Bus 4
A5	S				5	6	Address Bus 5
A6	S				4	5	Address Bus 6
A7	S				3	4	Address Bus 7
A8 (AH0)	S		27	21	25	29	Address Bus 8

* "S" refers to System Interconnect

HARDWARE INTERFACE (Continued)

DEVICE SET INTERCONNECT

LABEL	I/O	PIN CONNECTION					DESCRIPTION
		73M214	73D215	73D218	73D221 DIP	73D221 SMT	
A9 (AH1)	S				24	28	Address Bus 9
A10 (AH2)	S				21	24	Address Bus 10
A11 (AH3)	S				23	27	Address Bus 11
A12 (AH4)	S				2	3	Address Bus 12
A13 (AH5)	S				26	30	Address Bus 13
A14 (AH6)	S				27	31	Address Bus 14
A15 (AH7)	S						Address Bus 15
$\overline{CE}$	I				20	23	0V
ALE	S	1		30			
DSP/$\overline{CS}$	S		26				
$\overline{PSEN}$	S			29	22		Program Store Enable
$\overline{CE}$					20		GND

NVRAM INTERFACE

NVRCE	I			14			NVRAM CE (active high)
TXD	I/O			10			NVRAM DI/DO
RXD	I			11			NVRAM SK

POWER SUPPLIES AND CLOCKS

LABEL	I/O	PIN CONNECTION					DESCRIPTION
		73M214	73D215	73D218	73D225 DIP	73D225 SMT	
VDD	I			40			Positive supply (analog +5V)
VCC	I	28	28		28		Positive supply (digital +5V)
VSS	I	14					Negative supply (analog -5V)
AGND	I	26					Analog ground
GND	I	15	14	20	14	16	Digital ground
X1	I			19			XTAL input 14.7456 MHz
X2	O			18			XTAL output 14.7456 MHz
XIN	I	18					Clock input 7.3728 MHz
RST	I			9			Reset (10 µF & 8.2 kΩ)
Vpp			1				+5V

HARDWARE INTERFACE (Continued)

DAA INTERFACE

LABEL	I/O	PIN CONNECTION					DESCRIPTION
		73M214	73D215	73D218	73D225 DIP	73D225 SMT	
RXA	I	27					Receive analog from DAA
TXA	O	20					Transmit analog to DAA
MON	O	25					Audio monitor
$\overline{\text{HOOK}}$	O			8			Off hook relay control

RS-232/V.24 INTERFACE

$\overline{\text{RI}}$	O			3			Ring indicator output
TXD	I			10			Digital data from terminal
RXD	O			11			Digital receive data
DCD	O			2			Data carrier detect
DSR	O						Data set ready
TXCLK1	I	22					External Tx sync clock input
RXCLK	O	24		15			Receive clock ouptut
TXCLK	O	23		15			Transmit clock output
CTS	O			5			Clear to send
RTS	I			1			Request to send
DTR	I			4			Indicates DTE available

AT COMMAND SUMMARY*

Command	Description
AT	command prefix – precedes command line
<CR>	carriage return character – terminates command line
A	go into answer mode; attempt to go to on-line state
A/	re-execute previous command line; not preceded by AT nor followed by <CR>
B0	select CCITT V.22 standard for 1200 Bit/s communication
B1	***select Bell 212A standard for 1200 Bit/s communication***
D	dial number that follows; attempt to go to on-line state, originate mode
DS=n	dial stored number in location "n" (0-3)
E0	Disable character echo in command state
E1	***Enable character echo in command state***
H0	go on hook (hang up)
H1	go off hook; operate auxiliary relay
I0	request product indentification code
I1	perform checksum on firmware ROM; return checksum
I2	perform checksum on firmware ROM; returns OK or ERROR result codes
L0 or L1	low speaker volume
L2	***medium speaker volume***
L3	high speaker volume
M0	speaker off
M1	***speaker on until carrier detected***
M2	speaker always on
M3	speaker on until carrier detected, except during dialing
O0	go to on-line state
O1	go to on-line state and initiate equalizer retrain at 2400 Bit/s
Q0	***modem returns result codes***
Q1	modem does not return result codes
Sr	set pointer to register "r"
Sr=n	set register "r" to value "n"
Sr?	display value stored in register "r"
V0	display result codes in numeric form
V1	***display result codes in verbose form (as words)***
X0	enable features represented by result codes 0-4
X1	enable features represented by result codes 0-5, 10-12
X2	enable features represented by result codes 0-6, 10-12
X3	enable features represented by result codes 0-5, 7, 10-12
X4	***enable features represented by result codes 0-7, 10-12***
Y0	***disable long space disconnect***
Y1	enable long space disconnect
Z0	reset modem
&C0	***assume data carrier always present***
&C1	track presence of data carrier
&D0	***ignore DTR signal***
&D1	assume command state when an on-to-off transition of DTR occurs
&D2	hang up and assume command state when an on-to-off transition of DTR occurs
&D3	reset when an on-to-off transition of DTR occurs
&F	recall factory settings as active configuration
&G0	***no guard tone***
&G1	550 Hz guard tone
&G2	1800 Hz guard tone
&J0	***RJ-11/RJ-41S/RJ-45S telco jack***
&J1	RJ-12/RJ-13 telco jack
&M0	***asynchronous mode***
&M1	synchronous mode 1
&M2	synchronous mode 2
&M3	synchronous mode 3
&T0	terminate test in progress
&T1	initiate local analog loopback
&T3	initiate local digital loopback
&T4	***grant request from remote modem for RDL***
&T5	deny request from remote modem for RDL
&T6	initiate remote digital loopback
&T7	initiate remote digital loopback with self test
&T8	initiate local analog loopback with self test
&V	view active configuration, user profiles, and stored numbers
&W0	save storable parameters of active configuration
&X0	***modem provides transmit clock signal***
&X1	data terminal provides transmit clock signal
&X2	receive carrier provides transmit clock signal
&Zn=x	store phone number "x" in location "n" (0-3)

MNP COMMANDS

Command	Description
%A	Auto-Reliable fallback character
%C	compression control
\A	maximum block size
\G	modem port flow control
\J	rate adjust
\K	break control
\N	operating mode
\O	originate Reliable Link
\Q	flow control
\T	inactivity timer
\U	accept Reliable Link
\V	result code form
\X	XON/XOFF pass-through
\Y	switch to Reliable mode
\Z	switch to Normal mode

Note: ***Italicized*** parameters indicate default settings. If a parameter (0, 1, etc.) is not specified, the modem assumes the 0 parameter.

* Hayes Standard AT Command Set as implemented in Hayes Smartmodem 2400

AT COMMAND SUMMARY

TRANSMIT FAX COMMANDS

Command	Description
#F0	Return to normal modem mode
#F1	Enter FAX mode at DTE speed of 19200 bit/s
#M0	Speaker always off
#M1	Speaker off after connect message
#M2	Speaker always on
#M3	Speaker off during dial
#Pn	number of pages to send (n=1 to 255)
#R0	send with normal resolution
#R1	send with fine resolution

All extended commands have a # prefix after the AT. Extended commands have only one alpha character followed by a numeric value in the range of 0 to 255; the value 0 may be omitted. Once FAX mode is entered, commands are accepted at a fixed rate of 19200 bit/s and FAX mode will remain active until one of the following occurs:

1. The host software issues a #F command to return to modem command mode.
2. A call disconnect frame is received.
3. The host software issues an abort by dropping DTR.

The &D2 command must be issued for a DTR controlled abort. FAX mode assumes XON/XOFF or CTS flow control in data mode.

DIAL STRING ARGUMENTS

Argument	Description
,	Delay
;	Return to Command Mode After Dialing
@	Wait For Silent Answer
S	Dial Stored Number
!	Hook Flash
W	Wait for Dial Tone
R	Reverse Mode

TABLE 1: Result Codes

Xn	VERBOSE/TERSE RESULT CODES
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6, NO ANSWER/8

TABLE 2: S Registers Supported

Sn	FUNCTION	UNITS	DEFAULT
S0[1]	Answer on ring	No. of rings on which to answer	000[2]
S1	Ring counter	No. of rings accumulated	000
S2	Escape code	ASCII CHR Decimal 0-127	043
S3	Carriage return	ASCII CHR Decimal 0-127	013
S4	Line feed	ASCII CHR Decimal 0-127	010
S5	Back space	ASCII CHR Decimal 0-127	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds (0.1 sec)	006
S10	Carrier drop out	100 milliseconds (0.1 sec)	014
S11	DTMF tone duration	1 millisecond (0.001 sec)	070
S12	Escape guard time	20 milliseconds (0.05 sec)	050
S13	Unused		N/A
*S14[1]	Bit mapped register	Decimal 0-255	170

[1] Stored in NVRAM with &W command.
[2] Modem will not answer until value is changed to 1 or greater.
[3] If the NovRAM has not been initialized it may be necessary to type AT&F&W <cr> to set initial modem state.

TABLE 2: S Registers Supported (Continued)

NUMBER	FUNCTION	UNITS	DEFAULT
S15	Unused		N/A
S16	Test register	Decimal #	000
S17	SSi Special test register	Decimal 0-255	096
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[1]	Bit mapped register	Decimal 0-255	000
*S22[1]	Bit mapped register	Decimal 0-255	118
*S23[1]	Bit mapped register	Decimal 0-255	007
S24	Unused		N/A
S25[1]	DTR delay	10 milliseconds (0.01 sec)	005
S26[1]	CTS delay	10 milliseconds (0.01 sec)	001
*S27[1]	Bit mapped register	Decimal 0-255	064
S37	Desired Modem Line Speed	Decimal 0-3	000

* The bit mapped register functions are equivalent to normal "AT" command modem registers. They are not needed for evaluation of the 73D2417 capabilities.

Asynchronous character formats supported:
[Number of data bits, parity (even/odd/none), number of stop bits]

1200/2400 Bit/s: 7N2, 7E1, 7O1, 8N1

300 Bit/s: 7N2, 7E1, 7O1, 8N1, 8E1, 8O1

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
T_A, Ambient Temperature		0		70	°C
V_{CC} & V_{DD}, Supply Voltage	73M214, 73D215, 73D219, 73D225	4.75		5.25	V
V_{SS}, Supply Voltage	73M214	–4.25		–5.25	V
V_{DD}, V_{SS} Bypass Capacitors		10+0.1			µF
CLK Load Capacitance				25	pF
Digital Load Capacitance				50	pF
TXA, MON Loading				See Note	
Input Clock Frequency (X1)			14.7456		MHz
Input Clock Variation (X1, XIN)	XIN must be X1 ÷ 2	–0.01		0.01	%

Note: 10 kΩ in parallel with 50 pF

INPUT CLOCK TIMING (See Figure 1.)

TCLCX		20			ns
TCLCX2		54		82	ns
TCHCX		20			ns
TCHCX2		54		82	ns
TR, TF				15	ns
TCHCH		0		20	ns

INTERFACE TIMING

LED Write Timing (See Figure 2.)

TWLWH	$\overline{WR}$ pulse width		307			ns
TAVWL	Address valid to $\overline{WR}$ low		141			ns
TQVWH	Data valid to $\overline{WR}$ high		370			ns
TQVWX	Data valid to $\overline{WR}$ transition		27			ns
TWHDX	Data hold after $\overline{WR}$		86			ns

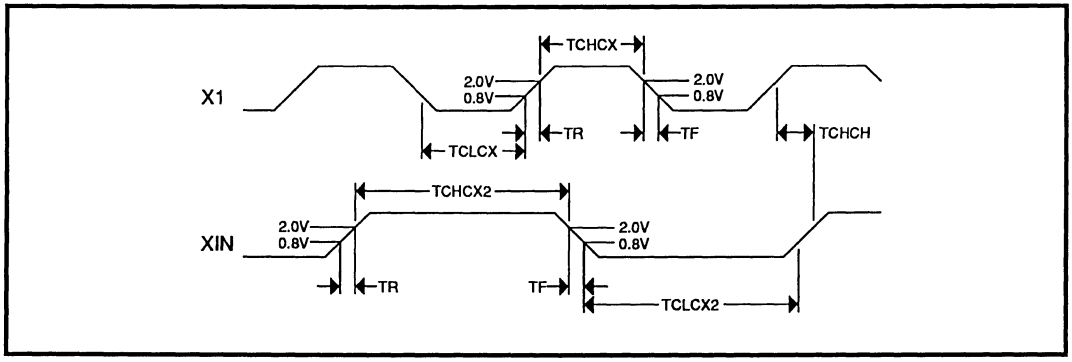


FIGURE 1: Input Clock Timing

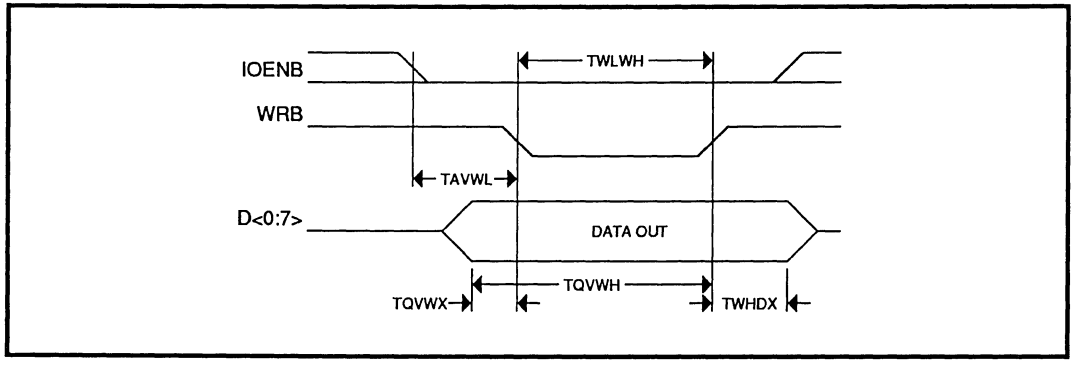


FIGURE 2: LED Write Timing

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
I_{DD}	Supply Current				130	mA
I_{SS}					25	mA
VIL	Input Low Voltage		0		0.8	V
VOH	Input High Voltage		2.0		VDD	V
I_{IH}	Input High Current	Except $\overline{CS}$ which has a pulldown of 20 kΩ			10	µA
I_{IL}	Input Low Current	Except TXCLKI, EXADCC which have pullups of 20 kΩ			-20	µA
	Digital Input Capacitance				10	pF
V_{OH}	Output High Voltage	Iout = -.4 mA	2.4			V
V_{OL}	Output Low Voltage	Iout = 1.6 mA			0.4	V
RXA	Input Resistance		100			kΩ
RXA	Input Capacitance				25	pF

TRANSMITTER SPECIFICATIONS

TRANSMITTER POWER

Values given are mearsured at the line connection point and assume that the DAA shown in our application literature is used with a 600Ω load.

TRANSMITTER POWER	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Transmitter Power	With or without CCITT tones	–9.8		–8.2	dBm
CCITT Guard Tone	550	–14.8		–12.8	dBm
	1800	–16.0		–14.0	dBm
FSK Transmitter Power	103/V.21	–10.0		–8.0	dBm
Answer Tone Power		–10.0		–8.0	dBm
DTMF Transmitter Power	High band tones	–7.0		–5.0	dBm
	Low band tones	–9.0		–7.0	dBm
	Twist	–3.0		–1.0	dB

TRANSMITTER FREQUENCY
(All tones are digitally derived from the clock input and have the input clock frequency tolerance.)

TRANSMITTER FREQUENCY		CONDITIONS		MIN	NOM	MAX	UNITS
QAM/DPSK Carrier Frequencies		Originate			1200.0		Hz
		Answer			2400.0		Hz
FSK Tone Frequencies							
103	Originate	Space	1070		1066.7		Hz
		Mark	1270		1269.4		Hz
	Answer	Space	2025		2021.1		Hz
		Mark	2225		2226.1		Hz
V.21	Originate	Space	1180		1181.6		Hz
		Mark	980		978.3		Hz
	Answer	Space	1850		1850.0		Hz
		Mark	1650		1651.6		Hz
Special Tone Frequencies							
Answer Tone			2100		2104.1		Hz
CCITT Guard Tones			550		556.5		Hz
			1800		1786.0		Hz
DTMF Dialing Tone Frequencies							
Low Group		Columns	697		698.2		Hz
			770		771.9		Hz
			852		853.3		Hz
			941		942.3		Hz
High Group		Rows	1209		1209.5		Hz
			1336		1335.7		Hz
			1477		1476.9		Hz
			1663		1634.0		Hz

TRANSMITTER DISTORTION

TRANSMITTER DISTORTION	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Carrier Suppresion	Measured at TXA	35			dB
CCITT Guard Tone Distortion	800-1600 Hz band			–60	dB
	0-10 kHz band			–45	dB
Answer Tone Distortion	800-1600 Hz band			–60	dB
	0-10 kHz band			–40	dB
FSK Output Bias Distortion	Transmit dotting 300 bit/s	–6		6	%
FSK Opposite Band Distortion				–60	dB
DTMF Tone Distortion	700-2900 Hz band			–29	dB

RECEIVER SPECIFICATIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier VCO					
Capture Range	Carrier offset	–10		10	Hz
Carrier Phase Jitter	50-65 Hz			30	Degrees
Data Clock Recovery Capture Range	From system clock + 24576 (600 Hz symbol clock)	-.025		+.025	%
Data Delay Time	RXA to RXD	30		75	ms
Retrain Request Threshold	If enabled	10^{-3}		10^{-2}	BER
Carrier Detect					
Threshold		–48		–43	dBm
Hysteresis		2			dB
Answer Tone Detect	2100/2225 Hz				
Threshold		–48		–43	dBm
Hysteresis		2			dB
Call Progress Detect	350-650 Hz dual tone				
Threshold		–40		–30	dBm
Hysteresis		2			dB

PERFORMANCE DATA

(This performance data was taken using an AEA tester and a Silicon Systems evaluation modem.)

BER PERFORMANCE

(–20dBm receive level 10^{-5} BER)

PARAMETER	MINIMUM SNR REQUIRED
2400 Bit/s Originate	16.5 dB SNR
2400 Bit/s Answer	16.0 dB SNR
1200 Bit/s Originate	9.0 dB SNR
1200 Bit/s Answer	8.0 dB SNR
0-300 Bit/s Originate	9.0 dB SNR
0-300 Bit/s Answer	7.5 dB SNR

DYNAMIC RANGE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
2400 Bit/s Originate	10^{-5} BER @ 17dB SNR	–45		0	dBm
2400 Bit/s Answer	10^{-5} BER @ 17dB SNR	–45		0	dBm
1200 Bit/s Originate	10^{-5} BER @ 12dB SNR	–45		0	dBm
1200 Bit/s Answer	10^{-5} BER @ 12dB SNR	–45		0	dBm
0-300 Bit/s Originate	10^{-5} BER @ 12dB SNR	–45		0	dBm
0-300 Bit/s Answer	10^{-5} BER @ 12dB SNR	–45		0	dBm

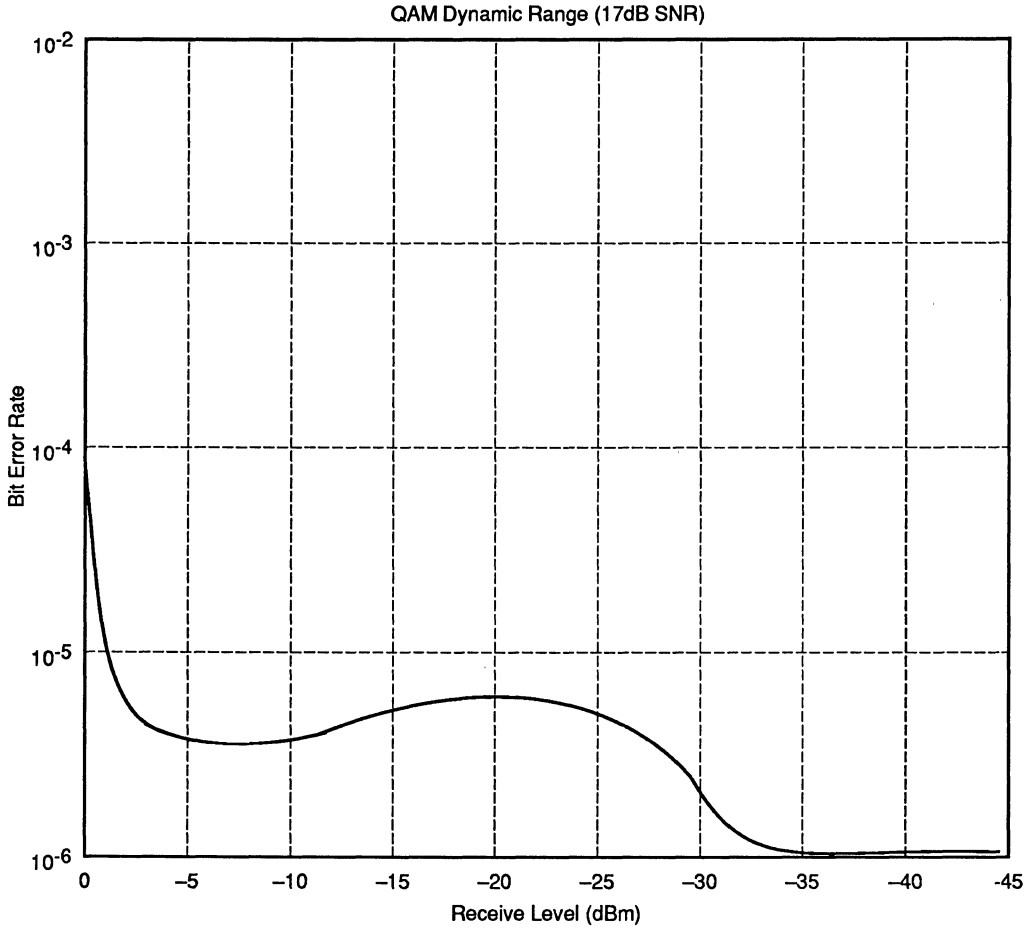


FIGURE 4: QAM Dynamic Range

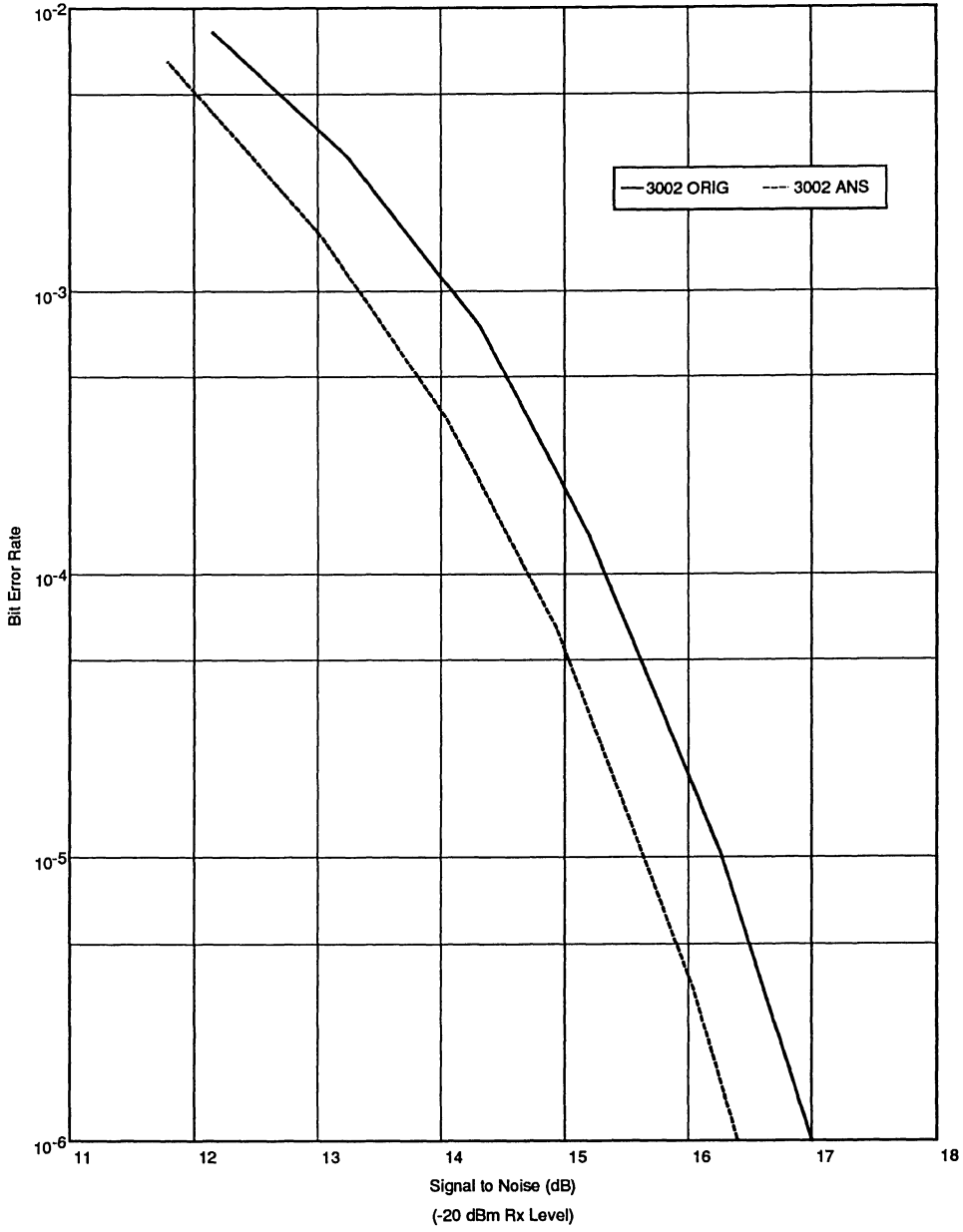


FIGURE 5: BER vs. SNR

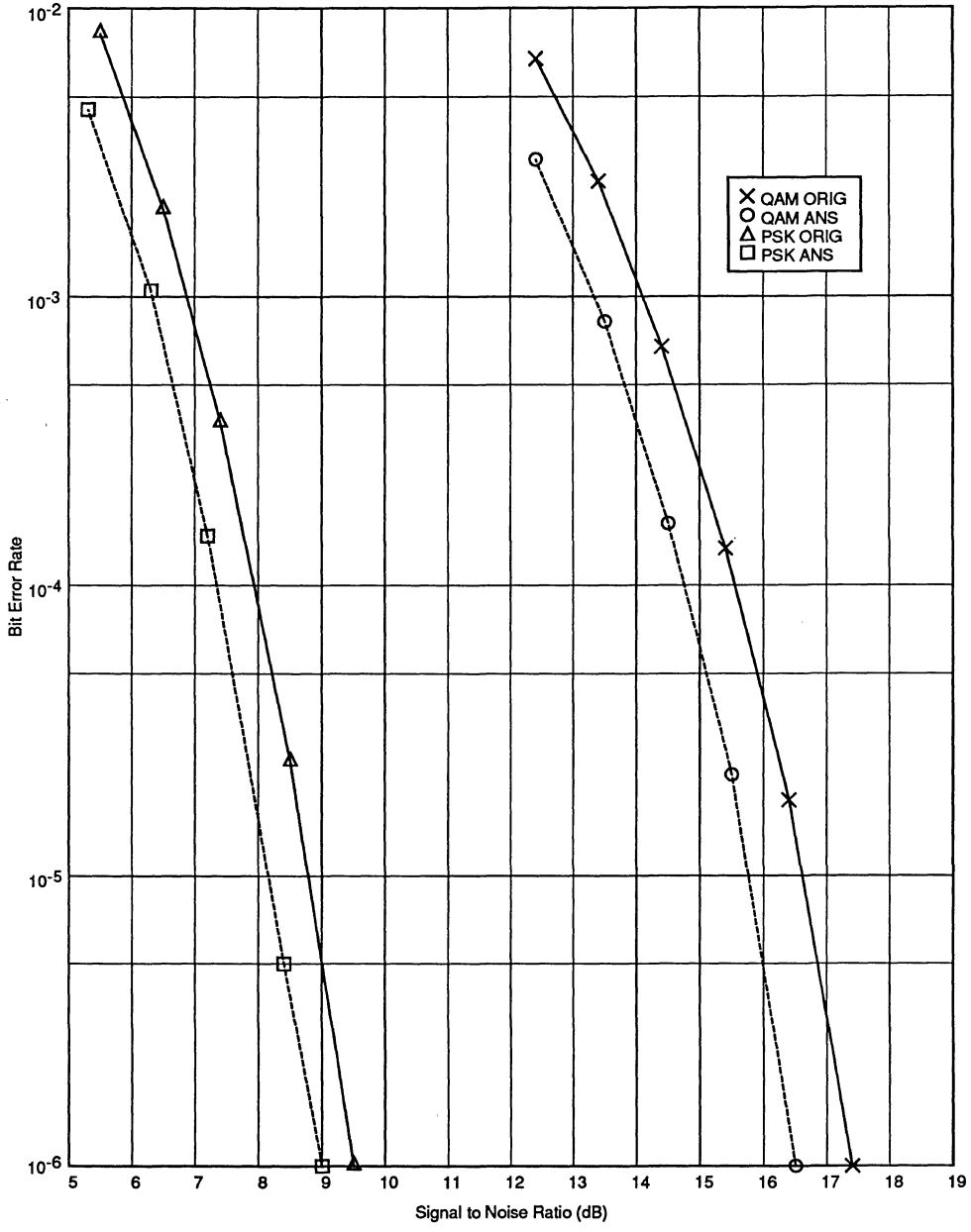


FIGURE 6: QAM and PSK BER vs. SNR with -20dBm Receive Level

APPLICATIONS INFORMATION

The SSI 73D2417 includes features and commands that are needed to design a full featured "smart" modem with industry standard AT commands and functions, including MNP5.

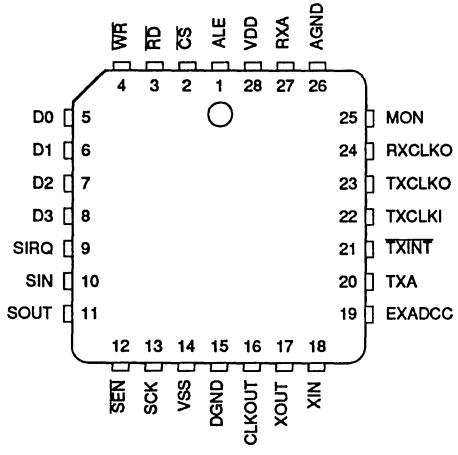
Control software needed for modem management, AT user interface, and FAX transmit mode is included within the device set. A complete basic modem requires the addition of an RS232 or UART interface, an appropriate telephone line interface, and circuitry for clock generation and address decode logic. Optional features that are provided for in the SSI 73D2417 and that may be included in a full featured modem design include: Nonvolatile memory for storage of setup parameters, a speaker and amplifier for audible monitoring of call activity, and LEDs for display of modem status.

The FAX transmit mode additionally requires a low cost D/A converter and band shaping filter to provide a V.27ter conformant transmit waveform. For data communication modes, the SSI 73D2417 employs an AT command set user interface that is compatible with existing modem products and software. With this interface, the user can directly control a modem using simple AT commands. As an option, communications software programs such as Smartcom™ may be used to provide a menu driven interface and additional features that make the modem easier to use.

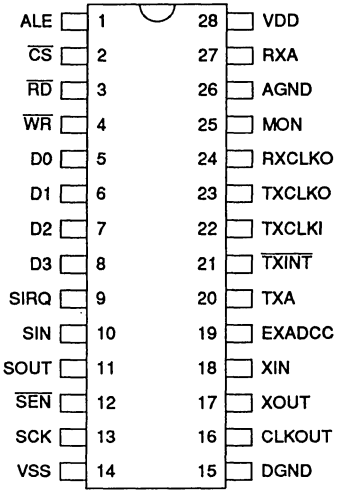
A FAX operating sequence is similar to, but more complex than that required for data communication, as the FAX operation adds an additional format conversion step which must be implemented by external communications software. A compatible communications software package, in conjunction with the SSI 73D2417 will provide full transmit FAX capability. Sources for datacom software that currently support this standard are listed below:

1. Bit FAX available from Bit Software
   (408) 263-2197
2. QuickLink II FAX available from
   Smith Micro Software
   (714) 964-0412

PACKAGE PIN DESIGNATIONS (Top View)



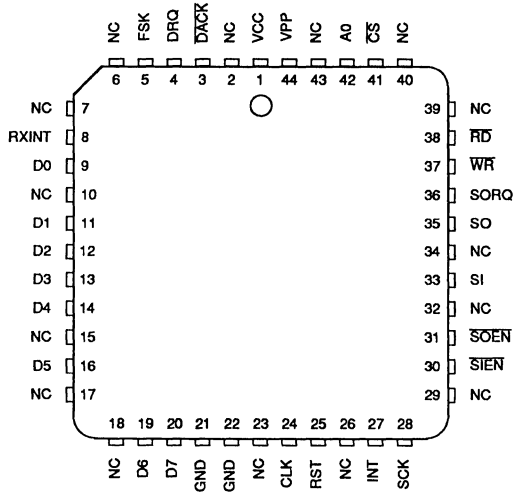
SSI 73M214
28-Pin PLCC



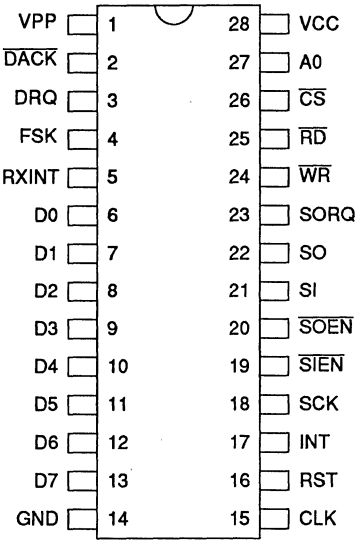
SSI 73M214
28-Pin DIP

SSI 73D2417
MNP5 Datacom/FAX
Modem Device Set

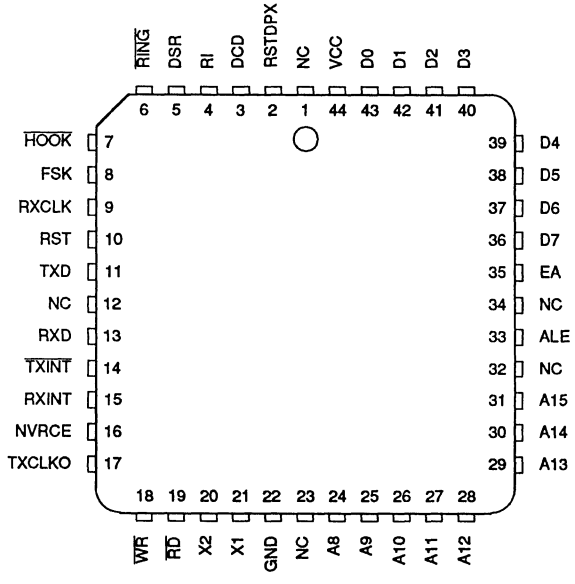
PACKAGE PIN DESIGNATIONS (Top View)



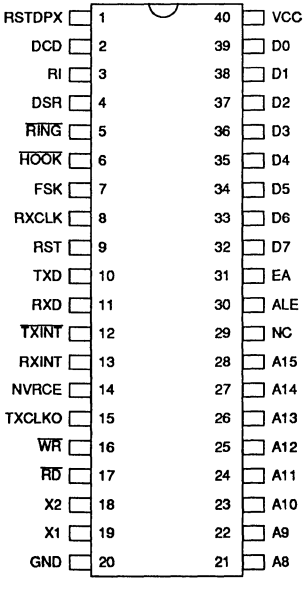
SSI 73M215
44-Pin PLCC



SSI 73M215
28-Pin DIP

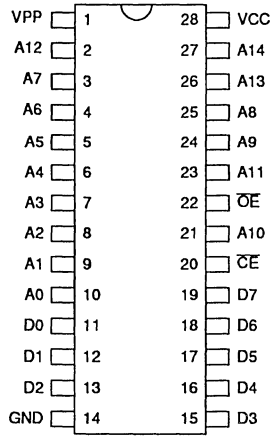


SSI 73M219
44-Pin PLCC

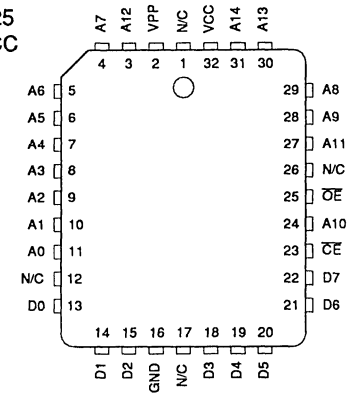


SSI 73M219
40-Pin DIP

SSI 73M225
28-Pin DIP



SSI 73M225
32-Pin PLCC



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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73D2417 Dual-In-Line Package	SSI 73D2417-CP	
28-pin Plastic DIP		73M214-IP
28-pin Plastic DIP		73D215-CP
40-pin Plastic DIP		73D219-CP
28-pin Plastic DIP		73D225-CP
SSI 73D2417 Surface Mount Package	SSI 73D2417-CH	
28-pin Plastic Leaded Chip Carrier		73M214-IH
44-pin Plastic Leaded Chip Carrier		73D215-CH
44-pin Plastic Leaded Chip Carrier		73D219-CH
32-pin Plastic Leaded Chip Carrier		73D225-CP

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

Notes:

SSI 73D2420/2421
CCITT V.42/V.42bis Protocol and Controller IC Set

Advance Information

June, 1990

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DESCRIPTION

The SSI 73D2420/2421 is an integrated circuit set which contains Silicon Systems' 73D680 controller, 73D681 K-Series interface, and 73D682 ROM. The IC set provides CCITT V.42 error-control and CCITT V.42bis data compression, Lap-B error-control, Asynchronous Framing Technique (AFT) error-control, adaptive data compression, automatic feature negotiation, flow control, automatic speed buffering and Hayes® AutoSync, when connected to an SSI 73K224 2400 bit/s multi-mode modem IC. Other K-Series modem ICs can be used, but the SSI 73K224 provides the highest level of connectivity. This IC set allows the user to build modems with advanced features not available from other semiconductor manufacturers. These advanced features are the same technology used by Hayes in their V-series® system products.

This Hayes technology is the same used by Hayes in their V-series products to implement the advanced features of these products. Silicon Systems is offering this integrated circuit set only to licensees of the Hayes Patent License Agreement.

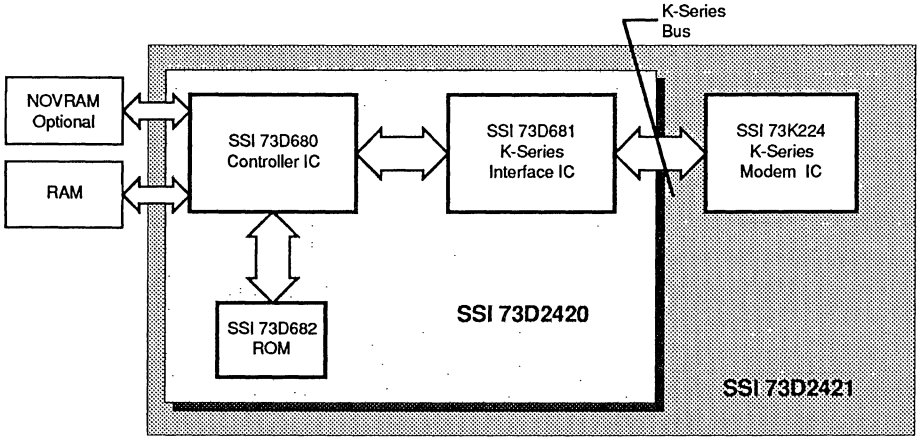
Hayes and V-series are registered trademarks, and Smartmodem 2400 is a trademark, of Hayes Microcomputer Products, Inc.

FEATURES

- **Supports CCITT V.22bis, V.22, V.21, and U.S. Modem Standards 212A and 103**
- **Full compliance with CCITT V.42, both LAP-M and the alternate Microcom Networking Protocol (MNP®) 4**
- **Supports CCITT V.42bis and MNP Level 5**
- **Hayes standard AT Command Set as implemented in Hayes V-series Smartmodem 2400™ V.42**
- **Hayes V-series features:**
  - **Lap-B error-control**
  - **Automatic Feature Negotiation**
  - **Adaptive Data Compression***
  - **AutoSync**
  - **Flow Control**
  - **Automatic Speed Buffering**
  - **Asynchronous Framing Technique (AFT)**
- **Power Down (Stand-By) Mode**

* Indicates Hayes patented technology. In addition to these patents, other patents concerning Hayes developed technology are pending.

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73D2420/2421
CCITT V.42/V.42bis Protocol and Controller IC Set

FUNCTIONAL DESCRIPTION

ERROR-CONTROL

The SSI 73D2420/2421 operates in full compliance with CCITT V.42, the international standard for point-to-point modem error-control, adopted in November 1988. LAP-M (Link Access Procedure for Modems), the Primary Protocol, and Annex A, the Alternate Protocol, provide backward compatibility with MNP®. Classes 2 through 4 are included. LAP-B (Link Access Procedure Balanced), the CCITT standard used by packet switched networks is also included. Lap-B was adapted by Hayes for use in modem point-to-point error-control for connectivity to all Hayes V-series system products.

DATA COMPRESSION*

The SSI 73D2420/2421 supports CCITT V.42bis, the international compression standard which provides compression capabilities up to 4:1, for use by modems incorporating the V.42 LAP-M error-control standard. The IC set provides a migration path to CCITT V.42bis data compression by supporting backward compatibility with Hayes adaptive data compression and MNP 5, each of which provide up to 2:1 compression.

AUTOMATIC FEATURE NEGOTIATION

Eliminates the need for user configuration for connection between dissimilar types of modems. Automatic Feature Negotiation occurs following the modulation handshake and provides the best possible connection. The range of features negotiated can be controlled by S-Register settings and include protocol type, compression, and parameters specific to the protocols.

DATA FLOW CONTROL

In error-control mode, the modem's buffers must hold incoming data until accurate transmission is verified. This process requires flow control to prevent possible data loss resulting from buffer overflow. Three types of flow control are used: RTS/CTS (hardware-based), XON/XOFF, and Transparent Flow Control (both character-based).

AUTOMATIC SPEED BUFFERING (ASB)

ASB permits computer equipment to transmit data to and from the modem at a constant rate regardless of the type or speed of the modem-to-modem connection.

ASYNCHRONOUS FRAMING TECHNIQUE

Hayes-developed framing technique which provides synchronous-like transmission across an asynchronous link. Synchronous protocols assemble data in frames prior to transmission and disassemble the frames on arrival.

HAYES AUTOSYNC*

The Hayes AutoSync capability provides synchronous communications to the remote modem, while using an asynchronous interface to the local DTE. Hayes AutoSync supports Binary Synchronous (BSC) and High-Level Data Link Control (HDLC) protocols by providing functions such as FCS generation and checking that are used by those protocols. The Hayes Synchronous Driver (HSD) supports this technology on IBM® PC and compatible computers, and is available to developers.

IC SET DESCRIPTION

SSI 73D680 Controller IC

The Hayes V-series protocol processor is a CMOS VLSI chip integrating Z80 CPU, a four-channel Counter Timer (CTC), dual port Parallel I/O (PIO), and dual channel Serial I/O (SIO), together with about 1200 logic gates. All functions are included on a single piece of silicon packaged in a 100-pin gull wing flat pack.

SSI 73D681 K-Series Interface IC

This chip takes commands from the 73D680 Controller and converts them to a form useful to the 73K224 modem chip. Responses from the modem are accumulated and interpreted by the interface and passed back to the controller.

SSI 73D682 ROM

This is a high performance, 1,048,576-bit Electrically Programmable Read Only Memory chip. It's organized as 128 K-words of 8 bits each, and provides code storage for the 73D680.

SSI 73K224 K-Series Modem IC

This chip is included in the SSI 73D2421 IC set and distinguishes it from the SSI 73D2420. Please refer to the SSI 73K224 stand-alone data sheet.

AT COMMAND SUMMARY*

Command	Description
AT	command prefix - precedes command line
<CR>	carriage return character - terminates command line
A	go into answer mode; attempt to go to on-line state
A/	re-execute previous command line; not preceded by AT nor followed by <CR>
B0	select CCITT V.22 standard for 1200 bit/s communication
B1	***select Bell 212A standard for 1200 bit/s communication***
B15	***select CCITT V.21 standard for 110/300 bit/s communication***
B16	***select Bell 103 standard for 110/300 bit/s communication***
D	go into originate mode; dial number that follows; attempt to go to on-line state
E0	Disable character echo in command state
E1	***Enable character echo in command state***
H0	go on hook (hang up)
H1	go off hook; operate auxiliary relay
I0	request product indentification code
I1	perform checksum on firmware ROM; return checksum
I2	perform checksum on firmware ROM; returns OK or ERROR result codes
L0 or L1	low speaker volume
L2	***medium speaker volume***
L3	high speaker volume
M0	speaker off
M1	***speaker on until carrier detected***
M2	speaker always on
M3	speaker on until carrier detected, except during dialing
N0	require modem to handshake at DCE speed selected with S37
N1	***permit modem to handshake at any DCE speed permitted by S37***
O0	go to on-line state
O1	go to on-line state and initiate equalizer retrain at 2400 bit/s
Q0	***modem returns result codes***
Q1	modem does not return result codes
Q2	modem returns result codes in originate mode; does not return result codes in answer mode
Sr	set pointer to register "r"
Sr=n	set register "r" to value "n"
Sr?	display value stored in register "r"
V0	display result codes in numeric form
V1	***display result codes in verbose form (as words)***
W0	***negotiation progress result codes not returned***
W1	negotiation progress result codes returned
X0	enable features represented by result codes 0-4
X1	enable features represented by result codes 0-5, 10-12
X2	enable features represented by result codes 0-6, 10-12
X3	enable features represented by result codes 0-5, 7, 10-12
X4	***enable features represented by result codes 0-7, 10-12***
Y0	***disable long space disconnect***
Y1	enable long space disconnect
Z0	reset modem and recall user profile 0
Z1	reset modem and recall user profile 1

Command	Description
&C0	***assume data carrier always present***
&C1	track presence of data carrier
&C2	data carrier support for UNIX
&D0	***ignore DTR signal***
&D1	assume command state when an on-to-off transition of DTR occurs
&D2	hang up and assume command state when an on-to-off transition of DTR occurs
&D3	reset when an on-to-off transition of DTR occurs
&D4	reset and enter low power mode when DTR is low
&F	recall factory settings as active configuration
&G0	***no guard tone***
&G1	550 Hz guard tone
&G2	1800 Hz guard tone
&J0	***RJ-11/RJ-41S/RJ-45S telco jack***
&J1	RJ-12/RJ-13 telco jack
&K0	local flow-control disabled
&K3	***RTS/CTS***
&K4	XON/XOFF
&K5	transparent XON/XOFF
&Q0	asynchronous mode
&Q1	synchronous mode 1
&Q2	synchronous mode 2
&Q3	synchronous mode 3
&Q4	synchronous mode 4
&Q5	***error-control mode***
&Q6	automatic speed buffering (ASB)
	Note: *&Mn* may be used in place of all *&Qn* options except *&Q4*, *&Q5*, and *&Q6*
&R0	***track CTS according to RTS***
&R1	ignore RTS; always assume presence of CTS
&S0	***assume presence of DSR signal***
&S1	track presence of DSR signal
&T0	terminate test in progress
&T1	initiate local analog loopback
&T3	initiate local digital loopback
&T4	***grant request from remote modem for RDL***
&T5	deny request from remote modem for RDL
&T6	initiate remote digital loopback
&T7	initiate remote digital loopback with self test
&T8	initiate local analog loopback with self test
&V	view active configuration, user profiles, and stored numbers
&W0	save storable parameters of active configuration as profile 0
&W1	save storable parameters of active configuration as profile 1
&X0	***modem provides transmit clock signal***
&X1	data terminal provides transmit clock signal
&X2	receive carrier provides transmit clock signal
&Y0	***recall user profile 0 on power-up***
&Y1	recall user profile 1 on power-up
&Zn=x	store phone number "x" in location "n" (0-3)

(Continued)

* Hayes Standard AT Command Set as implemented in Hayes V-Series Smartmodem 2400 V.42

AT COMMAND SUMMARY (continued)

The AT commands and the associated conditions described below may also affect the modem configuration and operation. These commands issued with parameters other than those specified will generate the ERROR result code.

C1	***enable transmit carrier switching***
F1	***disable on-line state character echo***

S-REGISTER SUMMARY

Register	Range	Description
S0	0-255 rings	select ring to answer on
S1	0-255 rings	ring count (incremented with each ring)
S2	0-127 ASCII	define escape sequence character
S3	0-127 ASCII	define carriage return character
S4	0-127 ASCII	define line feed character
S5	0-32, 127 ASCII	define back space character
S6	2-255 sec.	select wait time before blind dialing
S7	1-255 sec.	select wait time for carrier/dial tone
S8	0-255 sec.	select duration of comma dial modifier
S9	1-255 1/10 sec.	select carrier detect response time
S10	1-255 1/10 sec.	select time between carrier loss/hang up
S11	50-255 msec.	define duration/spacing of tones
S12	0-255 1/50 sec.	define escape frequency guard time
S18	0-255 sec.	select test timer
S25	0-255 1/100 sec.*	select DTR change detect time
S26	0-255 1/100 sec.	select RTS to CTS delay
S36	0, 1, 3, 4, 5, 7	select negotiation failure treatment
S37	0-3, 5, 6	select desired DCE line speed
S38	0-255 sec.	select delay before forced hang up
S46	0-3, 136, 138	protocol selection
S48	0, 7, 128	feature negotiation action
S49	1-249	buffer lower limit ASB (&Q6)
S50	2-250	buffer lower limit ASB (&Q6)
S82	3, 7, 128	break handling
S86	0-14	connection failure cause code
S89	0-255	0 = no power down
S95	bit mapped	compression result code

* When the modem is configured for synchronous operation, and until on-line, units of S25 are measured in whole seconds rather than 1/100 sec.

DIAL MODIFIERS

Modifier	Description
0-9 * # A B C D	digits/characters for dialing
P	pulse dial (factory setting)
T	tone dial
,	delay processing of next character
!	hookflash
@	wait for quiet answer
W	wait for dial tone
;	return to command state after dialing
R	reverse mode (to call an originate-only modem)
S=n	dial stored number in location "n" (n=0...3)

RESULT CODES SUMMARY

#	Word	Description
0	OK	command executed
1	CONNECT	connection at 0-300 bit/s or higher if Xo selected
2	RING	ring signal detected
3	NO CARRIER	carrier signal not detected, or lost
4	ERROR	invalid command, checksum, error in command line, or command line exceeds 255 characters
5	CONNECT 1200	connection at 1200 bit/s
6	NO DIALTONE	no dial tone detected
7	BUSY	busy signal detected
8	NO ANSWER	the @ dial modifier failed to detect quiet answer
10	CONNECT 2400	connection at 2400 bit/s
11	CONNECT 4800	connection at 4800 bit/s
12	CONNECT 9600	connection at 9600 bit/s
14	CONNECT 19200	connection at 19200 bit/s
40	CARRIER 300	carrier detected at 300 bit/s
46	CARRIER 1200	carrier detected at 1200 bit/s
47	CARRIER 2400	carrier detected at 2400 bit/s
70	PROTOCOL: NONE	asynchronous mode
71	PROTOCOL: ERROR-CONTROL/LAP-B	error-control mode with LAP-B protocol
73	PROTOCOL: ERROR-CONTROL/AFT	error-control mode with AFT
77	PROTOCOL: LAP-M	V.42 LAP-M
79	PROTOCOL: LAP-M/AFT	V.42 LAP-M with AFT
80	PROTOCOL: ALT	alternate protocol

Notes: ***Italicized*** parameters indicate default settings. If a parameter (0, 1, etc.) is not specified, the modem assumes the 0 parameter.

* Indicates Hayes patented technology (in addition to these patents, other patents concerning Hayes developed technology are pending).

SSI 73D680

The SSI 73D680 Hayes V-series protocol processor is a CMOS VLSI chip integrating Z80 CPU, a four channel Counter Timer (CTC), dual port Parallel I/O (PIO), and dual channel Serial I/O (SIO), together with about 1200 logic gates. All functions are included on a single piece of silicon packaged in a 100-pin gull wing flat pack.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
OSCIN, OSCOUT	I O	Crystal The OSCIN and OSCOUT pins provide the interface for either an external crystal or a CMOS compatible clock. Frequency of the crystal or external clock source is 11.0592 MHz±0.01%. If an external CMOS clock is applied, the OSCOUT pin should be left unterminated. The external clock may be connected directly to the OSCIN pin.
MA0-MA8	O	Multiplexed Address Bus MA0-MA8 are output pins which provide multiplexed address signals from the Z80 CPU and bank switch logic. Under most circumstances the lower 8 bits of the Z80 CPU's address, A0-A7, will be placed on pins MA0-MA7. MA8 will typically source XA17 from the bank select logic. When a memory access to a valid DRAM address is made, these lines will be switched to provide high order address lines A8-A12, and the bank switched lines XA13-XA16, respectively. Switching occurs shortly after the beginning of the second T-State of the memory cycle. These signals are intended to provide a multiplexed address bus for direct interface to external Dynamic RAM. These signals also are used as low order address signals for interfacing external memory and I/O devices.
A8-A15	O	High Order Address Bus The A8-A15 output pins source the most significant 8 bits of the processor address directly from the Z80 CPU. These signals are to be used for interfacing external memory and "extended" I/O devices.
XA13-XA17	O	Bank Switched Address Bus XA13-XA17 are output pins which provide bank switched address signals directly from the bank switched multiplexer logic. These signals are to be used for interfacing external non-multiplexed memory devices.
D0-D7	I/O	Data Bus Signals D0-D7 provide a common 8-bit bidirectional data bus used for all memory and I/O data transactions.
$\overline{RD}$	O	Read Strobe The $\overline{RD}$ signal indicates when the Z80 CPU is requesting read data from a memory or an I/O device. This signal should be used by addressed memory or I/O devices to gate data onto the data bus.
$\overline{WR}$	O	Write Strobe The $\overline{WR}$ signal indicates when the Z80 CPU has placed valid data on the 8-bit data bus for storage by the addressed memory or I/O device.
$\overline{MREQ}$	O	Memory Request The $\overline{MREQ}$ signal indicates when the Z80 CPU address bus holds a valid memory address for either a memory read or memory write transaction.

SSI 73D680 PIN DESCRIPTION, Continued

NAME	TYPE	DESCRIPTION
$\overline{IORQ}$	O	Input/Output Request The $\overline{IORQ}$ signal indicates when the Z80 CPU address bus holds a valid memory address for either an I/O read or I/O write cycle. This signal is also used in conjunction with an active low $\overline{M1}$ signal during a Mode 2 interrupt acknowledge cycle to indicate to the interrupting device that its interrupt vector should be placed on the data bus.
$\overline{M1}$	O	Machine Cycle One The $\overline{M1}$ signal when active together with $\overline{MREQ}$ indicates that the current machine cycle is an opcode fetch. The $\overline{M1}$ signal when active together with $\overline{IORQ}$ indicates an interrupt acknowledge cycle.
$\overline{NMI}$	I	Non-Maskable Interrupt The $\overline{NMI}$ signal is a negative edge triggered interrupt input used to force the Z80 CPU to restart at location 0066H. $\overline{NMI}$ is recognized at the end of the current instruction and has a higher priority than $\overline{INT}$. This signal is pulled high internally via an on-chip 20K pullup cell.
$\overline{INT}$	I	Interrupt Request The $\overline{INT}$ signal is an open drain interrupt request line which is shared by both on-chip I/O resources and external interrupt sources. This signal is wired-OR and is pulled high internally via an on-chip 20K pullup cell. The Z80 CPU will respond to an active interrupt signal at the end of the current instruction if the internal software controlled interrupt enable flip-flop is enabled.
$\overline{RESET}$	I	Reset The $\overline{RESET}$ input signal is used to initialize the Z80 CPU, SIO, CTC and all programmable registers contained on board the chip. The $\overline{RESET}$ input is Schmitt-triggered and is internally latched and extended for 256 system clock cycles after the externally applied signal goes inactive.
$\overline{ZRESET}$	O	Z80 System Reset The $\overline{ZRESET}$ signal is an output signal intended to be used as an active low reset signal for external peripherals to the chip. $\overline{ZRESET}$ will be driven low whenever the $\overline{RESET}$ returns high. $\overline{ZRESET}$ may also be activated by a low to high transition of the signal on the PIOA_0 pin if such detection has been enabled via programming of an internal reset enable control register bit.
CLK	O	Clock The CLK signal provides a divide by two output of the OSCIN clock input frequency. This signal provides a single phase timing reference which matches the internal Z80 system clock. This signal is to be used by external peripherals requiring access to the Z80 system clock reference.
$\overline{CSROM}$	O	Chip Select ROM The $\overline{CSROM}$ signal indicates when the Z80 CPU is performing a memory transaction to a memory location over the 0 to 32K Z80 physical address range. This signal is intended to be used as the chip select strobe for an external ROM device.
$\overline{CSRAM}$	O	Chip Select RAM The $\overline{CSRAM}$ signal indicates when the Z80 CPU is performing a memory read cycle to a memory location over the 32K to 64K Z80 physical address range. This signal is intended to be used as the output enable strobe for external DRAM devices and is used to instruct such devices to gate data onto the Z80 data bus. Additionally, an internal register can be programmed to allow $\overline{CSRAM}$ to occur during a memory read cycle to any address over the entire 64K physical address range.

NAME	TYPE	DESCRIPTION
$\overline{CSIO1}$	O	Chip Select IO1 The $\overline{CSIO1}$ signal indicates when the Z80 CPU is performing a read or write transaction to an external device mapped over the Z80 I/O address range of 2C-2F (hex). This signal is not qualified by $\overline{IORQ}$ and is intended to be used with I/O mapped devices which require chip select to become active before the write or read strobe. The $\overline{IRD}$ and $\overline{IWR}$ signals provide the suitable $\overline{IORQ}$ qualification for such devices.
$\overline{CSIO2}$	O	Chip Select IO2 The $\overline{CSIO2}$ signal indicates when the Z80 CPU is performing an I/O transaction to an external device mapped over the Z80 I/O address range of 40-5F (hex). This signal is intended to be used as the chip select strobe for an external I/O device and is internally qualified by $\overline{IORQ}$.
$\overline{CSEE}$	O	Chip Select EEPROM The $\overline{CSEE}$ signal indicates when the Z80 CPU is performing an I/O transaction to an external device mapped over the Z80 I/O address range of 60-7F (hex). This signal is intended to be used as the chip select strobe for the external I/O device and is internally qualified by $\overline{IORQ}$.
$\overline{CSIO3}$	O	Chip Select IO3 The $\overline{CSIO3}$ signal indicates when the Z80 CPU is performing an I/O transaction cycle to an external device mapped over the Z80 I/O address range of 80-9F (hex). This signal is intended to be used as the chip select strobe for an external I/O device and is internally qualified by $\overline{IORQ}$.
$\overline{RAS}$	O	Row Address Strobe The $\overline{RAS}$ signal is intended to be used as the row address strobe when used in conjunction with external DRAM devices. The first falling edge of $\overline{RAS}$ during a memory cycle instructs the DRAM devices to latch the current value present on the MA0-MA8 address lines. $\overline{RAS}$ timing is also designed to activate the internal refresh counter of the DRAM during all opcode fetch cycles.
$\overline{CAS}$	O	Column Address Strobe The $\overline{CAS}$ signal is intended to be used as the column address strobe when used in conjunction with external DRAM devices. The first falling edge of $\overline{CAS}$ during a memory cycle instructs the DRAM devices to latch the current value present on the MA0-MA8 address lines.
$\overline{WEEE}$	O	Write Enable EEPROM The $\overline{WEEE}$ signal indicates that the Z80 CPU data bus holds valid data to be stored into an I/O device mapped over the address range of 60-7F (hex). This signal is intended to be used as the write strobe for an external device enabled with the $\overline{CSEE}$ signal.
$\overline{IRD}$	O	I/O Read Strobe The $\overline{IRD}$ signal indicates when the Z80 CPU is requesting read data from an I/O device. This signal should be used by addressed I/O devices to gate data onto the data bus. The $\overline{IRD}$ signal is qualified by both active $\overline{IORQ}$ and $\overline{RD}$ from the Z80 CPU.
$\overline{IWR}$	O	I/O Write Strobe The $\overline{IWR}$ signal indicates when the Z80 CPU has placed valid data on the 8-bit data bus for storage by the addressed I/O device. This signal is qualified by both active $\overline{IORQ}$ and $\overline{WR}$ from the Z80.

SSI 73D680 PIN DESCRIPTION, Continued

NAME	TYPE	DESCRIPTION
TXD_DTE	I	Transmit Data DTE The TXD_DTE signal is the serial transmit data input for the built-in data terminal interface implemented on the A-channel of the internal SIO. Signal polarity is high for mark and low for space.
RXD_DTE	O	Receive Data DTE The RXD_DTE signal is the serial receive data output for the built-in data terminal interface implemented on the A-channel of the internal SIO. Signal polarity is high for mark and low for space.
TXD_MOD	O	Transmit Data MOD The TXD_MOD signal is the serial transmit data output for the built-in modem $\overline{DCE}$ interface implemented on the B-channel of the internal SIO. Signal polarity is high for mark and low for space.
RXD_MOD	I	Receive Data MOD The RXD_MOD signal is the serial receive data input for the built-in modem $\overline{DCE}$ interface implemented on the B-channel of the internal SIO. Signal polarity is high for mark and low for space.
$\overline{TXC\_IN}$	I	Transmit Clock Input The $\overline{TXC\_IN}$ signal accepts signal element timing information for synchronous serial data transmitted on the TXD_MOD serial data output signal. The low to high transition indicates the center of each signal element on TXD_MOD.
$\overline{RXC\_IN}$	I	Receive Clock Input The $\overline{RXC\_IN}$ signal accepts signal element timing information for synchronous serial data received on the RXD_MOD serial data input signal. The low to high transition indicates the center of each signal element on RXD_MOD.
$\overline{TXC\_OUT}$	O	Transmit Clock Output The $\overline{TXC\_OUT}$ signal provides signal element timing information for synchronous serial data received on the TXD_DTE serial data input signal. The low to high transition indicates the center of each signal element on TXD_DTE.
$\overline{RXC\_OUT}$	O	Receive Clock Output The $\overline{RXC\_OUT}$ signal provides signal element timing information for synchronous serial data transmitted on the RXD_DTE serial data output signal. The low to high transition indicates the center of each signal element on RXD_DTE.
$\overline{XTC\_IN}$	I	Transmit Clock Input The $\overline{XTC\_IN}$ signal accepts signal element timing information for synchronous serial data received on the TXD_DTE serial data input signal for modes where the data terminal must supply the transmit clock. The low to high transition indicates the center of each signal element on TXD_DTE.
PORT1_0 - PORT1_7	O	Output Port PORT1_0 - PORT1_7 provide an eight-bit wide general purpose fixed output port. All eight outputs are derived from a common on chip I/O accessed register with readback capability.

NAME	TYPE	DESCRIPTION
PIOA_0	I	PIOA Bit 0 PIOA_0 is the least significant I/O line provided from the A-channel of the internal PIO. This signal is user programmable as either an input or output and may be used for general purpose I/O applications. When configured as an input, this signal can also be programmed to generate a system reset upon receipt of a low to high transition.
PIOA_1	I	PIOA Bit 1 PIOA_1 is an I/O line provided from the A-channel of the internal PIO. When configured as an input, this signal may also be programmed to generate interrupts via the DCDA external status interrupt line on the A-channel of the internal SIO. Interrupts generated in this manner are transition sensitive.
PIOA_2	O	PIOA Bit 2 PIOA_2 is an I/O line provided from the A-channel of the internal PIO.
PIOA_3	O	PIOA Bit 3 PIOA_3 is an I/O line provided from the A-channel of the internal PIO.
PIOA_4	O	PIOA Bit 4 PIOA_4 is an I/O line provided from the A-channel of the internal PIO.
PIOA_5	I	PIOA Bit 5 PIOA_5 is an I/O line provided from the A-channel of the internal PIO. When configured as an input, this signal may also be programmed to generate interrupts via the $\overline{CTS}$ external status interrupt line on the B-channel of the internal SIO. Interrupts generated in this manner are transition sensitive.
PIOA_6	I	PIOA Bit 6 PIOA_6 is an I/O line provided for the A-channel of the internal PIO.
PIOA_7	I	PIOA Bit 7 PIOA_7 is the most significant I/O line provided from the A-channel of the internal PIO.
PIOB_0-1 PIOB_2-5 PIOB_6-7	I O I	PIOB_0-PIOB_7 provide an eight-bit wide general purpose I/O port. All eight lines are derived from the B-channel of the internal PIO and can individually be programmed as either an input or output. PIOB lines 6 and 7, when programmed as inputs, are internally pulled high via on-chip 20K pullup cells to facilitate their use as jumper strap inputs.
$\overline{INTDCD}$	I/O	Interrupt DCD $\overline{INTDCD}$ is a general purpose input signal which is gated to the $\overline{DCD}$ external status line on the B-channel of the SIO. This signal can also be programmed to generate transition sensitive interrupts via the SIO or act as the master IEI daisy chain interrupt enable input.
$\overline{SYNCA}$	I/O	SYNCA SIO Channel A $\overline{SYNCA}$ can be defined as either an input or output based on the configuration of SIO channel A. This signal is directly connected to the $\overline{SYNCA}$ line of the SIO. This signal may either be pulled high or left open in the final application circuit.
$\overline{ITC1}$-$\overline{ITC3}$	I	Internal Test Control $\overline{ITC1}$-$\overline{ITC3}$ are internal test control lines required to verify proper functionality of internal chip circuitry. These signals should be tied low in the final application circuit.

SSI 73D680 PIN DESCRIPTION, Continued

NAME	TYPE	DESCRIPTION
TEN	I	Internal Test Control TEN is the internal test enable control line required to verify proper functionality of internal chip circuitry. This signal should be tied low in the final application circuit.
VDD	I	+5 Volt Power Input Four VDD power input leads are provided by this chip package. These signals should be connected to a +5 Volt power supply with a tolerance rating of ±5% or better.
VSS	I	Power Return Input Four VSS power return leads are provided by this chip package. These signals should be connected to the ground return line of the +5 Volt power supply. These pins provide the ground reference for all signals on the chip.

ABSOLUTE MAXIMUM RATINGS

Power Supply (V_{DD}) .....–0.3V to 7.0V
Input Voltage (Vi) .....–0.3V to V_{DD} + 0.3V
Input Current (Ii) .....20 mA
Soldering Temperature .....260°C for 10 sec
Storage Temperature (Tstg) .....–40°C to 125°C

GENERAL REQUIREMENTS

Power Supply Range .....5V ±5%
Operating Temperature Range .....0-70°C
Operating Humidity Range ... 10-90% noncondensing

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC CHARACTERISTICS, TTL Level Input Buffer (Ta = 0°C - 70°C; V_{DD} = 5.0V ± 5%)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP(3)	MAX	UNIT
V_{IL}	Input Low Voltage	except $\overline{RESET}$	–0.3		0.8	V
V_{IH}	Input High Voltage	except $\overline{RESET}$	2.2		V_{DD}	V
V_{ILT}	Min. Low Going Input Threshold Voltage for $\overline{RESET}$		0.9			V
V_{IHT}	Max. High Going Input Threshold Voltage for $\overline{RESET}$				3.6	V
V_H	Input Hysterysis Voltage		0.4		2.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.4	V
V_{OH1}	Output High Voltage	I_{OH} = –1.6 mA	2.4			V
V_{OH2}	Output High Voltage	I_{OH} = –250 µA	V_{DD} – 0.8			V
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$			±10	µA
I_{LOZ}	3-State Output Leakage Current in Float	$V_{SS} + 0.4 \le V_{IN} \le V_{DD}$			±10	µA
I_{DD}	Power Supply Current	V_{CC} = 5V, fCLK = 8 MHz $V_{IH} = V_{DD} - 0.2V$, V_{IL} = 0.2V			80	mA

AC CHARACTERISTICS (VCC = 5.0V ±5%, Ta = 25°C, Load = 100 pF for all signals except $\overline{RAS}$ = 30 pF)

NO.	SYMBOL	PARAMETER	MIN	MAX	UNIT
1	TcC	System Clock Cycle Time	125	DC	ns
2	TwCh	System Clock Pulse Width (high)	55	DC	ns
3	TwCl	System Clock Pulse Width (low)	55	DC	ns
4	TfC	System Clock Fall Time		10	ns
5	TrC	System Clock Rise Time		10	ns
6	TdCrADR	Clock to Address Valid Delay		80	ns
7	TdA	Address Valid to $\overline{MREQ}$ Delay	20		ns
8	TdCfMREQf	Clock to Falling $\overline{MREQ}$ Delay		58	ns
9	TdCrMREQr	Clock to Rising $\overline{MREQ}$ Delay		58	ns
10	TwMREQh	$\overline{MREQ}$ Pulse Width (high)	45		ns
11	TwMREQl	$\overline{MREQ}$ Pulse Width (low)	100		ns
12	TdCfMREQr	Clock to Rising $\overline{MREQ}$ Delay		58	ns
13	TdCfRDf	Clock to Falling $\overline{RD}$ Delay		70	ns
14	TdCrRDr	Clock to Rising $\overline{RD}$ Delay		60	ns
15	TdCrM1f	Clock to Falling $\overline{M1}$ Delay		70	ns
16	TdCrM1r	Clock to Rising $\overline{M1}$ Delay		70	ns
17	TdCrDz	Clock to Data Float Delay		70	ns
18	TsDCr	Data Setup Time to Clock	30		ns
19	ThDRDr	Data Hold Time to $\overline{RD}$ Rising	0		ns
20	TdMAR	Row Address to $\overline{RAS}$ Delay	5		ns
21	ThMAR	Row Address Hold Time from $\overline{RAS}$ (Note 1)	15		ns
22	TdCfRASf	Clock to Falling $\overline{RAS}$ Delay		70	ns
23	Tw1RASl	$\overline{RAS}$ First Pulse Width (low)	120		ns
24	TwRASh	$\overline{RAS}$ Pulse Width (high)	105		ns
25	Tw2RASl	$\overline{RAS}$ Second Pulse Width (low)	120		ns
26	TdCrRASr	Clock to Rising $\overline{RAS}$ Delay		30	ns
27	TdRASCAS	$\overline{RAS}$ to $\overline{CAS}$ Delay (Note 2)	30		ns
28	TdMACCAS	Column Address to $\overline{CAS}$ Delay	5		ns
29	TdCASfCr	$\overline{CAS}$ Falling to Rising Clock of T3 (Note 2)	120		ns
30	TdCrCASr	Clock Rising to $\overline{CAS}$ Rising Delay		30	ns
31	TdCSRAMf	Clock to $\overline{CSRAM}$ Falling Delay		80	ns
32	TdCSRAMr	Clock to $\overline{CSRAM}$ Rising Delay		70	ns

Note:
1. To meet this specification when fCLK = 8 MHz, the EXTEND mode must be enabled to delay $\overline{CAS}$ and the MA0-8 address multiplexer by a quarter system clock cycle or (8) must occur within 45 ns after the falling edge of the clock during the T1 state time.
2. These timing specifications are valid for either setting of the EXTEND timing control signal.

AC CHARACTERISTICS, Continued

(VCC = 5.0V ±5%, Ta = 25°C, Load = 100 pF for all signals except $\overline{RAS}$ = 30 pF)

NO.	SYMBOL	PARAMETER		MIN	MAX	UNIT
33	TdCSROMf	Clock to $\overline{CSROM}$ Falling Delay			70	ns
34	TdCSROMr	Clock to $\overline{CSROM}$ Rising Delay			70	ns
35	TdCrXA	Clock to XAddress Valid Delay			95	ns
36	TdXA	XAddress Valid to $\overline{MREQ}$ Delay		5		ns
37	ThXA	XAddress Hold after $\overline{MREQ}$		10		ns
38	ThMAC	Column Address Hold after $\overline{MREQ}$		0		ns
39	TwMREQh4	$\overline{MREQ}$ Pulse Width (high) (Note 3)		110		ns
40	TwMREQl4	$\overline{MREQ}$ Pulse Width (low) (Note 3)		160		ns
41	ThMAR4	Row Address Hold Time from $\overline{RAS}$ (Note 3)		20		ns
42	Tw1RASl4	$\overline{RAS}$ First Pulse Width (low) (Note 3)		200		ns
43	TwRASh4	$\overline{RAS}$ Pulse Width (high) (Note 3)		110		ns
44	Tw2RASl4	$\overline{RAS}$ Second Pulse Width (low) (Note 3)		160		ns
45	TdCASfCr4	$\overline{CAS}$ Falling to Rising Clock of T3 (Note 3)		110		ns
46	TdMREQrAh	$\overline{MREQ}$ Rising to Address Hold Time		20		ns
47	TdCfRDr	Clock to $\overline{RD}$ Rising Delay			60	ns
48	TdDCf	Data Setup Time to Clock during M2, M3, M4 or M5 cycles		30		ns
49	TdCfWRf	Clock to $\overline{WR}$ Falling Delay			60	ns
50	TwWR	$\overline{WR}$ Pulse Width (low)		100		ns
51	TdCfWRr	Clock to Rising $\overline{WR}$ Delay			60	ns
52	TdCfD	Clock to Write Data Valid			115	ns
53	TdDWRf	Write Data Valid prior to $\overline{WR}$		5		ns
54	TdDWRr	Write Data Hold Delay after $\overline{WR}$		15		ns
55	TdMREQrMA	Column Address Hold after $\overline{MREQ}$		0		ns
56	TdCfRASr	Clock to $\overline{RAS}$ Rising Delay			70	ns
57	TdCASfCf	$\overline{CAS}$ Falling to	Early $\overline{CAS}$	110		ns
		Falling T3 Clock	Extended $\overline{CAS}$	100		ns
58	TdCSRAMr2	Clock to $\overline{CSRAM}$ Rising Delay			70	ns
59	TdCSROMr2	Clock to $\overline{CSROM}$ Rising Delay			70	ns
60	Td1ORQrAh	$\overline{IORQ}$ to Address Hold Time		20		ns
61	TsAIORQf	Address Setup to $\overline{IORQ}$ Falling		75		ns
62	TdCrMA	Clock to MAddress Delay			100	ns

Note:

3. These specifications only apply when fCLK is ≤ 4 MHz. Operation above 4 MHz requires the enabling of the Op-Code Fetch Wait State generator circuitry.

SSI 73D680

NO.	SYMBOL	PARAMETER	MIN	MAX	UNIT
63	TsMAIORQf	MAddress Setup to $\overline{IORQ}$ Falling	55		ns
64	ThIORQrMA	$\overline{IORQ}$ to MAddress Hold Time	20		ns
65	TdCrIORQf	Clock to $\overline{IORQ}$ Falling Delay		55	ns
66	TdCfIORQr	Clock to $\overline{IORQ}$ Rising Delay		60	ns
67	TdCrRDf	Clock to $\overline{RD}$ Falling Delay		60	ns
68	TdCfRDr	Clock to $\overline{RD}$ Rising Delay		60	ns
69	TdCrIRDf	Clock to $\overline{IRD}$ Falling Delay		70	ns
70	TdCIRDr	Clock to $\overline{IRD}$ Rising Delay		70	ns
71	TsDCf	Data Setup to Clock during T3	30		ns
72	TdCrWRf	Clock to $\overline{WR}$ Falling Delay		55	ns
73	TdCfWRr	Clock to $\overline{WR}$ Rising Delay		60	ns
74	ThWRrD	Data Hold Time after $\overline{WR}$ Rising	15		ns
75	TdCfIWRf	Clock to $\overline{IWR}$ Falling Delay		20	ns
76	TwIWR	$\overline{IWR}$ Pulse Width (low)	170		ns
77	TdCrIWRr	Clock to $\overline{IWR}$ Rising Delay		25	ns
78	TdCfWEEEf	Clock to $\overline{WEEE}$ FallingDelay		30	ns
79	TwWEEE	$\overline{WEEE}$ Pulse Width (low)	170		ns
80	TdCrWEEEr	Clock to $\overline{WEEE}$ Rising Delay		35	ns
81	TdDWRfIO	Data Stable prior to $\overline{WR}$ Falling	55		ns
82	TdDWRr	Data Hold Time after $\overline{WR}$	15		ns
83	TdCrCSEEf	Clock to $\overline{CSEE}$ Falling Delay		70	ns
84	TdCfCSEEr	Clock to $\overline{CSEE}$ Rising Delay		75	ns
85	TdCrCSFEf	Clock to $\overline{CSFE}$ Falling Delay		70	ns
86	TdCfCSFEr	Clock to $\overline{CSFE}$ Rising Delay		75	ns
87	TdCrCSGAf	Clock to $\overline{CSGE}$ Falling Delay		70	ns
88	TdCfCSGAr	Clock to $\overline{CSGE}$ Rising Delay		75	ns
89	TdCCSDEDf	Clock to $\overline{CSDED}$ Falling Delay		100	ns
90	TdICSDEDr	$\overline{IORQ}$ Rising to $\overline{CSDED}$ Rising Delay	20		ns
91	ThDWRr	Data Hold Time after $\overline{IWR}$	60		ns
92	ThDWEEEr	Data Hold Time after $\overline{WEEE}$	60		ns
93	TdCSDEDfI	$\overline{CSDED}$ Falling to $\overline{IORQ}$ Delay	30		ns
94	TdCfRASr	Clock to $\overline{RAS}$ Rising Delay		70	ns

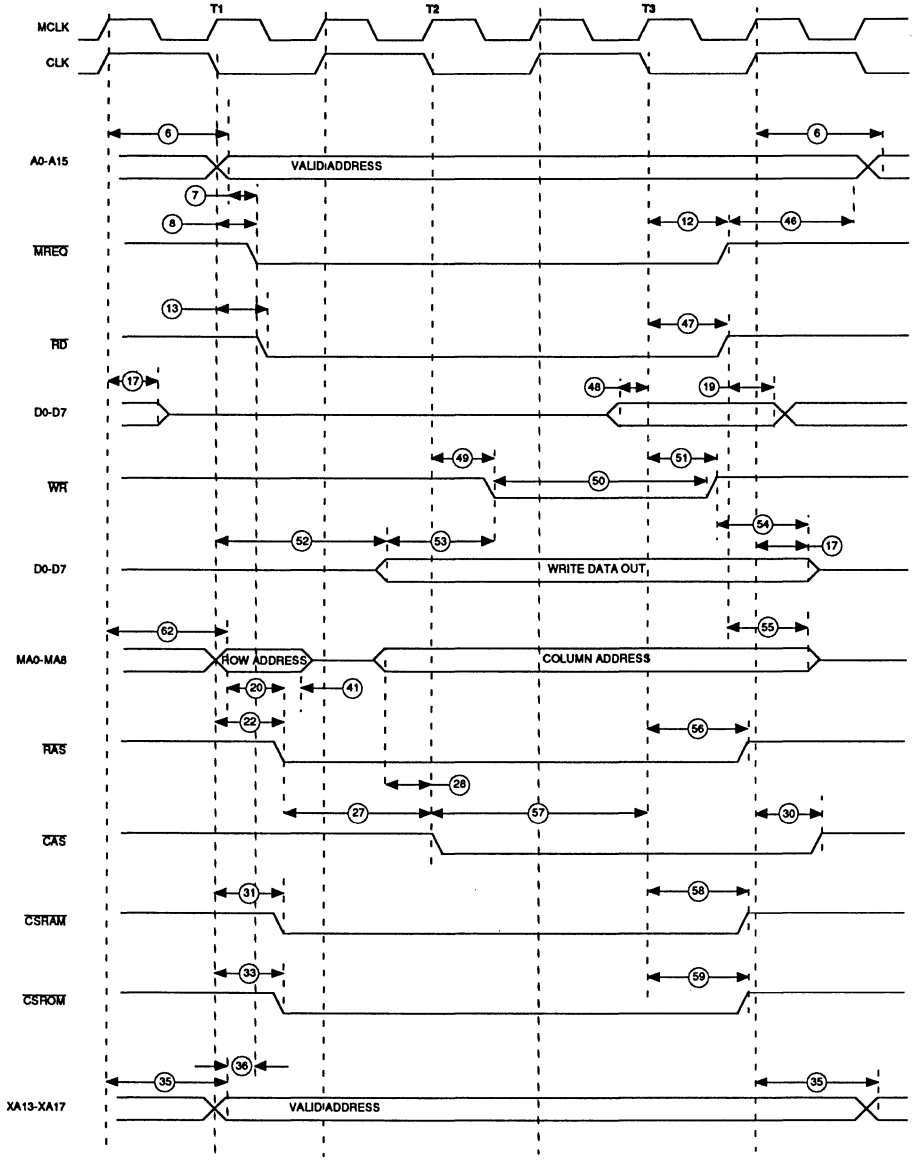


FIGURE 1: Z80 CPU Memory Read/Write Timing

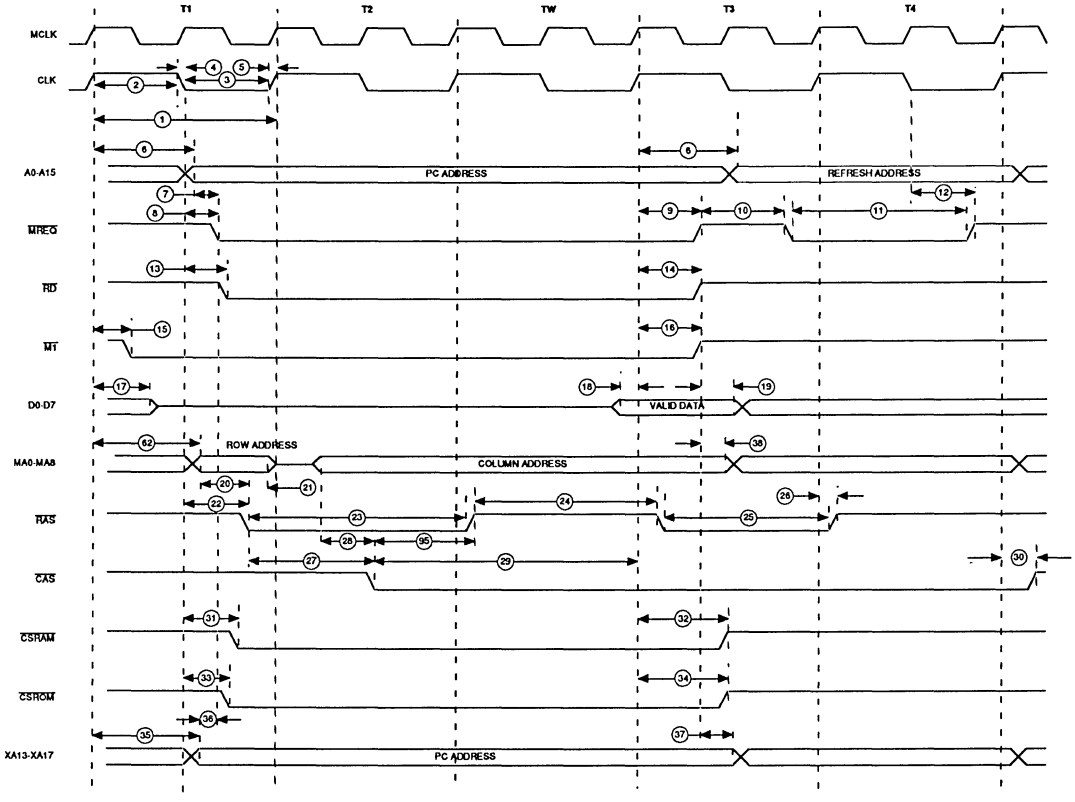


FIGURE 2: Z80 CPU Opcode Fetch Timing – Wait State Mode Enabled

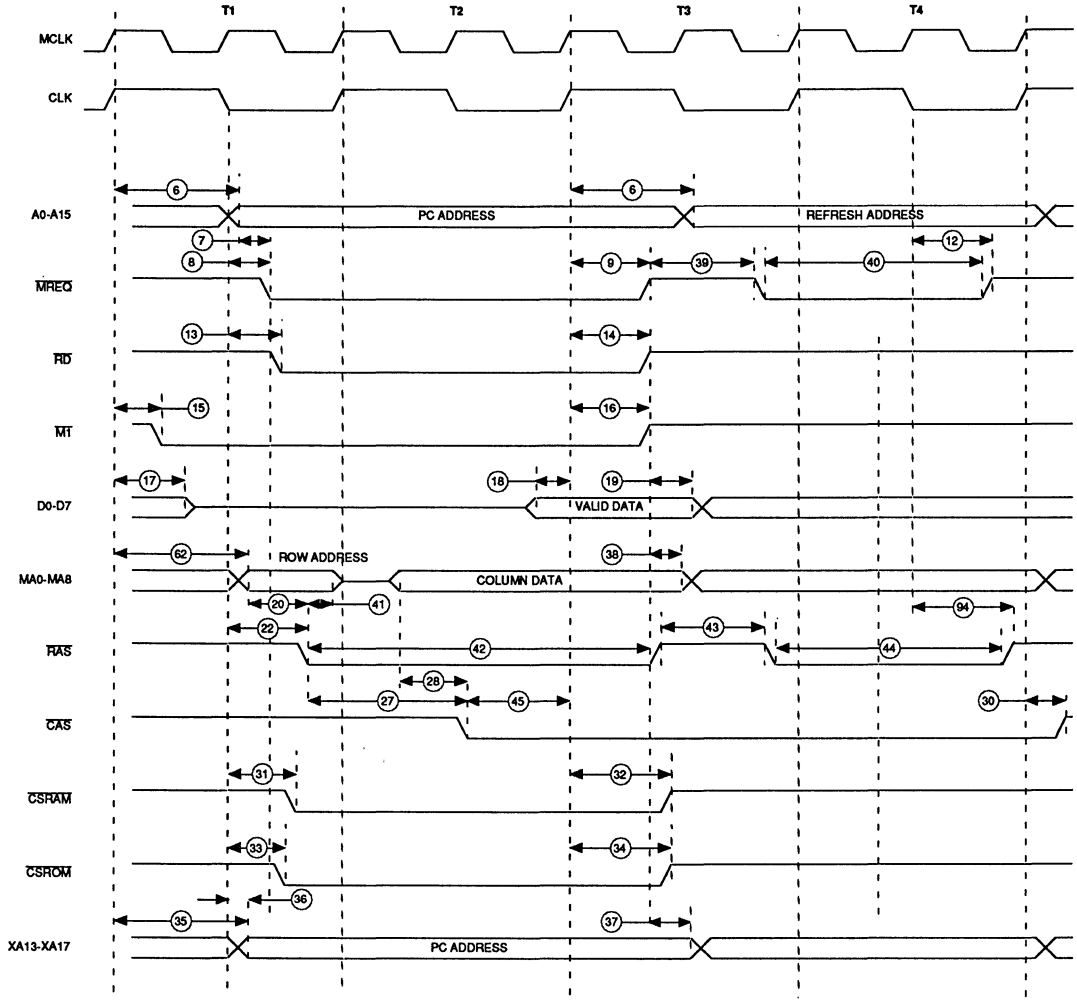


FIGURE 3: Z80 CPU Opcode Fetch Timing – No Wait State

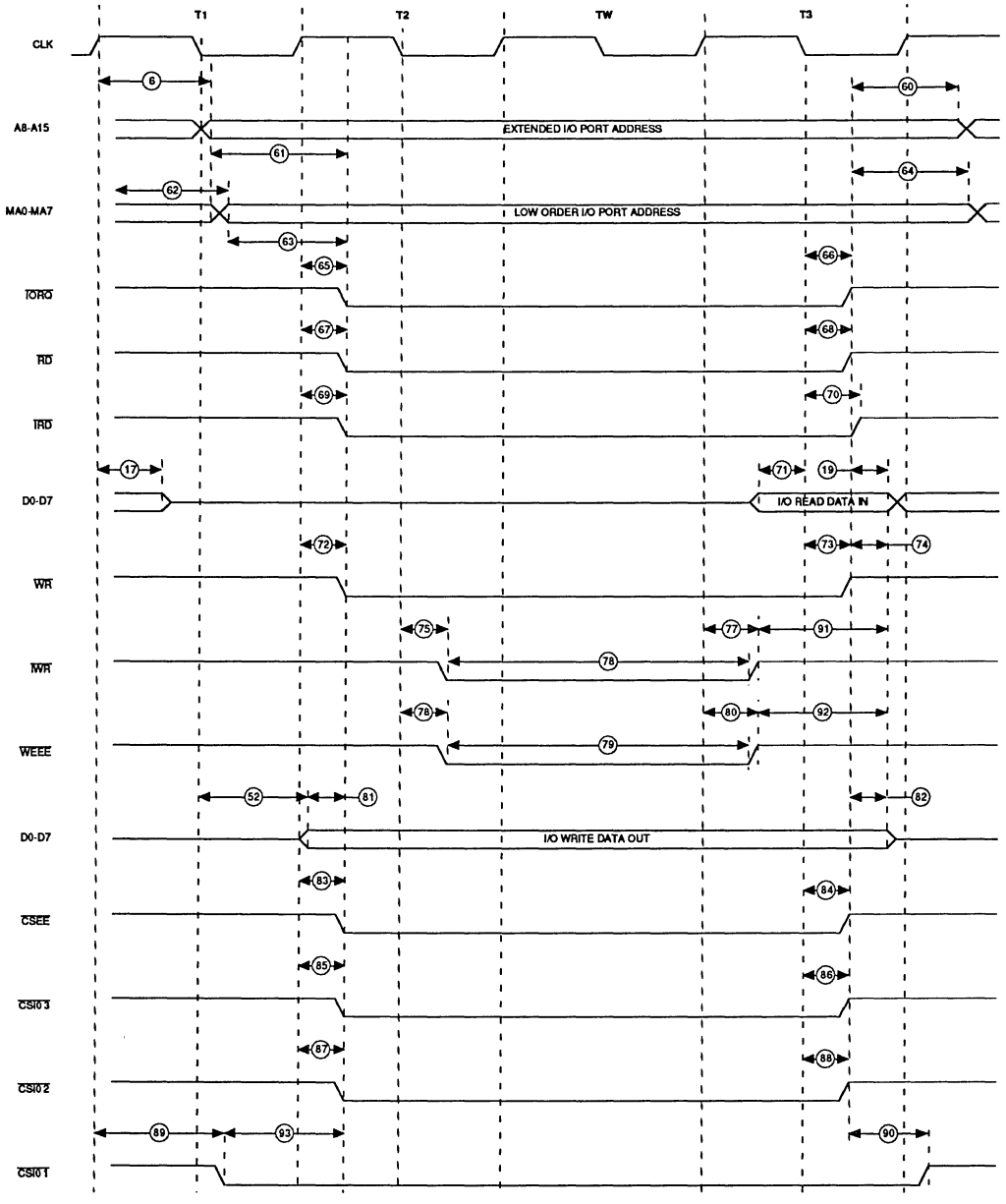


FIGURE 4: Z80 Input/Output Timing

SSI 73D681

The SSI 73D681 Interface Chip takes commands from the SSI 73D680 Controller and converts them to a form useful to the SSI 73K224 modem chip. Responses from the modem are accumulated and interpreted by the interface and passed back to the Controller.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
TEST2	O	For Silicon Systems use only. Do not connect.
$\overline{\text{DTR}}$	I	Powers up chip when power saving mode is enabled. This signal must be low for at least 100 ms for power-up to occur.
TEST3	O	For Silicon Systems use only. Do not connect.
TEST4	O	For Silicon Systems use only. Do not connect.
CCMD	I	Command input for isochronous data from the host processor.
CINT	O	Interrupt pin to the host processor. This pin may be as either an interrupt out pin or as a detector pin. The function of this pin is controlled by the host processor.
MACK	O	Clock for data transfers from SSI 73D681 to the host processor.
MRSP	O	Isochronous data from SSI 73D681 that is transferred to the host processor.
RST	I	Reset in, active high.
RXD	I	Serial Asynchronous Command Port: receive data pin for asynchronous commands. This pin is used for testing and evaluation only.
TXD	O	Serial Asynchronous Command Port: transmit data pin for asynchronous commands. This pin is used for evaluation of the data pump.
SPL0	O	Speaker – Volume Command port. LSB
SPL1	O	Speaker – Volume Command port. MSB
$\overline{\text{HOOK}}$	O	Hook drive relay, active low.
$\overline{\text{RESET}}$	O	Reset active low to host processor.
RESET	O	Reset active high to RAM. This pin is assigned to a circuit that protects the RAM during power-up.

PIN DESCRIPTION, Continued

NAME	TYPE	DESCRIPTION
$\overline{\text{RELAY}}$	O	Aux drive relay active low.
DAASEL	I	DAA type select 373/Other. This pin is an input. It should be connected low while reset is asserted by SSI 73D681. This pin is only used as input while reset is asserted. This pin is used as an output during internal Silicon Systems testing. This pin displays detector bits.
$\overline{\text{UARTEN}}$	O	UART Enable. This pin is asserted low when the UART should be turned on for data after power saving mode is exited.
$\overline{\text{PSEN}}$	O	Do not connect.
$\overline{\text{RD}}$	O	Read active low to Silicon Systems "K" Family Data Pump.
$\overline{\text{WR}}$	O	Write active low to Silicon Systems "K" Family Data Pump.
ALE	O	Address Strobe to "K" Family Data Pump.
AD0	I/O	Data line D0 to Data Pump.
AD1	I/O	Data line D1 to Data Pump.
AD2	I/O	Data line D2 to Data Pump.
AD3	I/O	Data line D3 to Data Pump.
AD4	I/O	Data line D4 to Data Pump.
AD5	I/O	Data line D5 to Data Pump.
AD6	I/O	Data line D6 to Data Pump.
AD7	I/O	Data line D7 to Data Pump.
CLKIN	I	11.0592 MHz clock in.
CLKOUT	O	11.0592 MHz clock out.
$\overline{\text{STR}}$	I	Host Processor command data block.
CMD1	I	First command bit from Host Processor.
RXCLK	I	RXCLK from data pump.
RI	I	Ring indicate from DAA.
$\overline{\text{EA}}$	I	Internal test pin.
VCC	I	Digital five volts power input.
VSS	O	Digital ground.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias .....0°C to +70°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin to V_{SS} .....–0.5V to V_{CC} +0.5V
Voltage on V_{CC} to V_{SS} .....–0.5V to +6.5V
Maximum I_{OL} per I/O pin .....15 mA
Power Dissipation.....1.0W*

*This value is based on the maximum allowable die temperature and the thermal resistance to the package.

Notice: Stresses listed above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Notice: Specifications contained within the following tables are subject to change.

DC READ CHARACTERISTICS (Ta = 0°C to 70°C; V_{CC} = 5V ± 20%; V_{SS} = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP(3)	MAX	UNIT
V_{IL}	Input Low Voltage (Except $\overline{EA}$)		–0.5		0.2 V_{CC} – 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		–0.5		0.2 V_{CC} – 0.3	V
V_{IH}	Input High Voltage (Except CLKIN, RST)		0.2 V_{CC} + 0.9		V_{CC} + 0.5	V
V_{IH1}	Input High Voltage (CLKIN, RST)		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)				0.45	V
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA			0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	I_{OH} = –60 µA, V_{CC} = 5V ±10%	2.4			V
		I_{OH} = –25 µA	0.75 V_{CC}			V
		I_{OH} = –10 µA	0.9 V_{CC}			V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.45V			–50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V_{IN} = 2.0V			–650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}			±10	µA
CIO	Pin Capacitance	Test Freq. = 1 MHz, Ta = 25°C			10	pF
I_{CC}	Power Supply Current Active Mode, 12 MHz (4) Idle Mode, 12 MHz (4) Power Down Mode			 11 1.7 5	 20 5 50	 mA mA µA

Port 0 = pins 32-39
Port 1 = pins 1-8
Port 2 = pins 21-28
Port 3 = pins 10-17

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SSI 73D682

The SSI 73D682 is a high performance, 1,048,576-bit Electrically Programmable Read Only Memory. It's organized as 128 K-words of 8 bits each, and provides code storage for the SSI 73D680 Controller.

Key Features Include:

- **High Performance CMOS**
  - 120 ns Access Time
  - 50 mA Active Power
- **Simplified Upgrade Path**
  - V_{PP} and PGM are "Don't Care" During Normal Read Operation
- **EPI Processing**
  - Latch-up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 32-pin Dip
  - 32-pin Chip PLCC
- **Compatible with JEDEC 27C010 EPROMs**

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +125°C
Voltages on any Pin with Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground ..... −0.6V to +7V
ESD Protection ..... >2000V

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
A0-A16	I	Addresses
CE	I	Chip Enable
OE	I	Output Enable
O0-O7	O	Outputs
PGM	I	Program
XX		Don't Care (During Read)

ELECTRICAL CHARACTERISTICS

TIMING

PARAMETER	SSI 73D682
Address Access Time (max)	120 ns
Chip Select Time (max)	120 ns
Output Enable Time (max)	35 ns

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Comm.	0°C to +70°C	+5V	±5% / ±10%

DC READ CHARACTERISTICS (Over operating range with $V_{PP} = V_{CC}$)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –400 µA	2.4		V
I_{SB}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, F = 5 MHz		50	mA
I_{PP}	V_{PP} Supply Current (1)	$V_{PP} = V_{CC}$		10	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} – 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	–10	10	µA

AC READ CHARACTERISTICS (Over operating range with $V_{PP} = V_{CC}$)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{ACC}	Address to Output Delay		120	ns
t_{CE}	$\overline{CE}$ to Output Delay		120	ns
t_{OE}	$\overline{OE}$ to Output Delay		35	ns
t_{DF}	Output Disable to Output Float (2)		35	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurred first (2)	0		ns

Notes:

1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 - O_7 unloaded.
2. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.

MODE SELECTION

The mode of operation of the SSI 73D682 are listed below. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A_9 for device signature.

MODE		PINS							
		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X (1)	X	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP} (2)	6.0V	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP} (2)	6.0V	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP} (2)	5.0V	High Z
Signature	Manufacturer (3)	V_{IL}	V_{IL}	X	V_H (2)	V_{IL}	X	5.0V	YY H (4)
	Device (3)	V_{IL}	V_{IL}	X	V_H (2)	V_{IH}	X	5.0V	ZZ H (5)

Notes:
1. X can be V_{IL} or V_{IH}
2. $V_H = V_{PP} = 12.75 \pm 0.25V$
3. A_1–A_8, A_{10}–$A_{16} = V_{IL}$
4. YY represents the manufacturer code
5. ZZ represents the device code

PROGRAMMING INFORMATION

DC CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current ($V_{IN} = V_{CC}$ or GND)	I_{LI}	–10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE} = \overline{PGM} = V_{IL}$)	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	–0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = –400 µA)	V_{OH}	3.5		V

Notes:
1. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
2. V_{PP} must not be greater than 14V including overshoot. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5V to 12.75V or vice-versa.
3. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (Ta = 25 ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
$\overline{CE}$ High to $\overline{OE}$ High	t_{COH}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid from Out Enable	t_{OE}			55	ns
V_{PP} Setup Time / $\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

CAPACITANCE (2) Ta = 25°C, f = 1 MHz

PARAMETER	CONDITIONS	SYMBOL	TYP (1)	MAX	UNITS
Input Capacitance	V_{IN} = 0V	C_{IN}	4	6	pF
Output Capacitance	V_{OUT} = 0V	C_{OUT}	8	12	pF
V_{PP} Capacitance	V_{PP} = 0V	C_{VPP}	18	25	pF

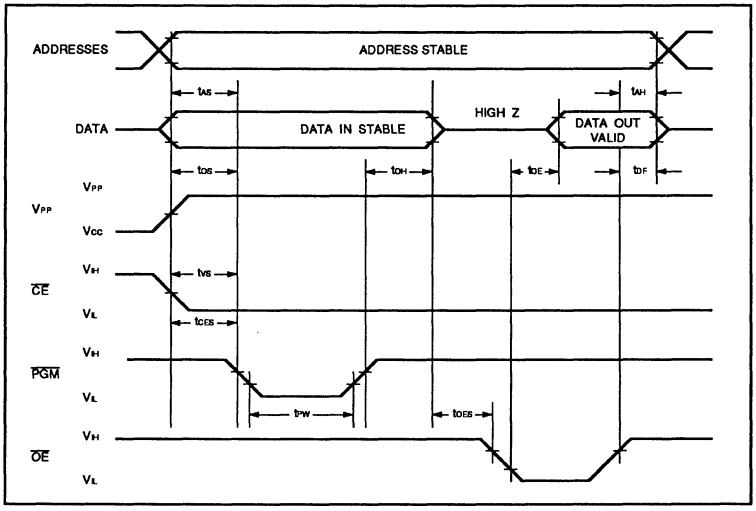


FIGURE 5: Programming Waveforms

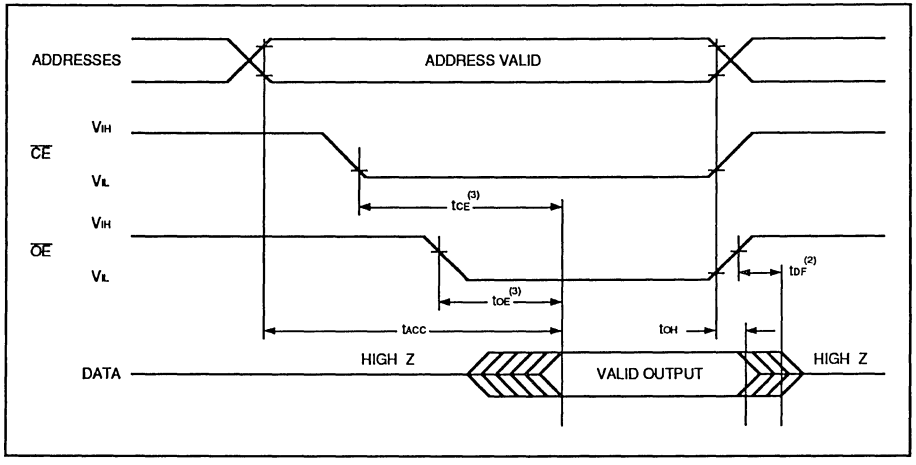


FIGURE 6: AC Waveforms

Notes:
1. Typical values are for Ta = 25°C and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE}-t_{CE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}

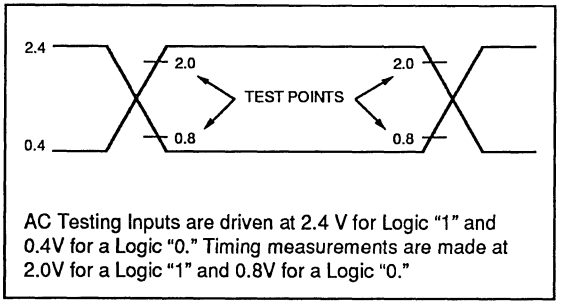


FIGURE 7: AC Testing I/O Waveform

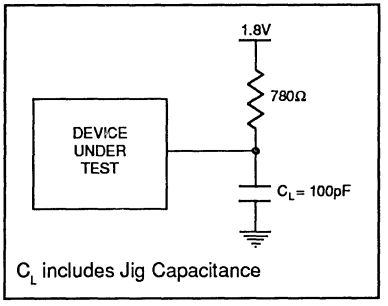
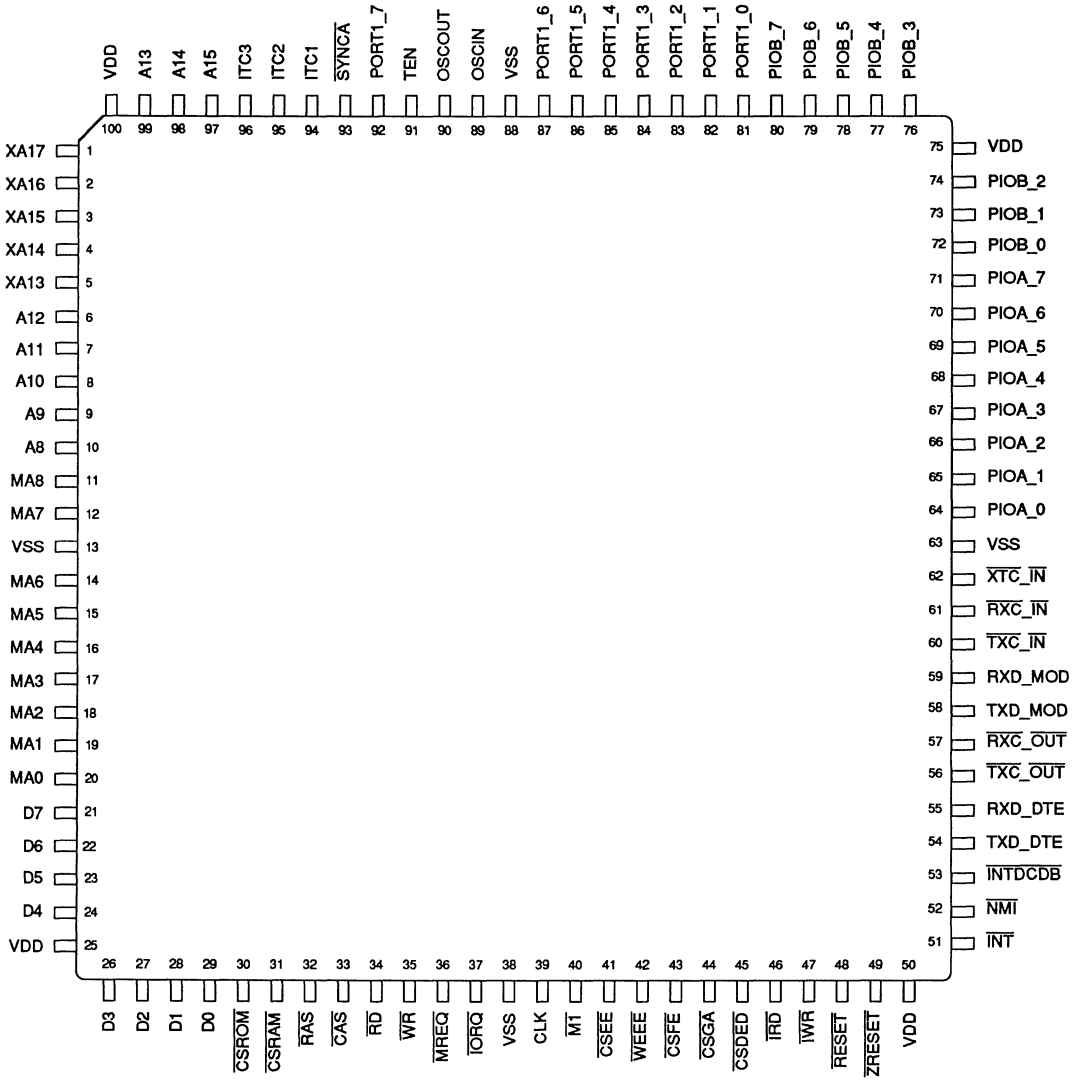


FIGURE 8: Testing Load Circuit

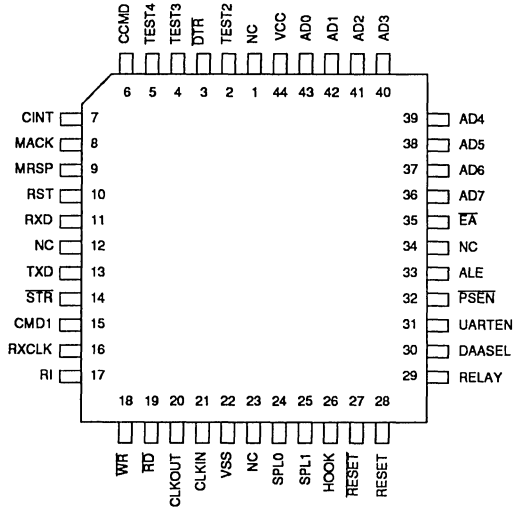
PIN DIAGRAMS- Top View



SSI 73D680 Controller Pin Diagram

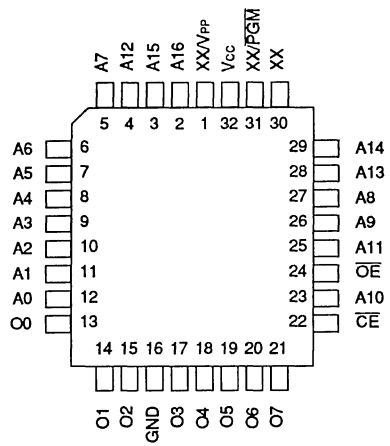
100-pin Flat Pack

PIN DIAGRAMS - Top View



SSI 73D681

44-pin PLCC Surface Mount



SSI 73D682

32-pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

Notes:

SSI 73D2291/2292
FAX Modem Device Set with TIA/EIA User Interface

Advance Information

July, 1990

2

DESCRIPTION

The SSI 73D2291 is a CMOS device set that allows half-duplex transmit and receive G3 facsimile data communication over the dial-up telephone network. The 73D2291 conforms to CCITT V.29 and V.27ter standards as defined for FAX operation, and it includes an EIA/TIA industry standard AT user interface for high level control of FAX functions. The AT command set provided by the 73D2291's user interface simplifies control of the FAX modes, and insures compatibility with existing personal computer applications software designed for FAX communications.

The 73D2291 employs the same control architecture used in Silicon Systems 1-chip modem products, and is compatible with these devices. 2400 bit/s datacom modes can be incorporated into the product by addition of the SSI 73K224L 1-chip modem (73D2292 product). Other Silicon Systems 1-chip modems may be used to provide alternate datacom modes. The SSI 73D2291's built in AT command interpreter can control both the FAX and datacom modes, eliminating the need for separate controllers and additional components.

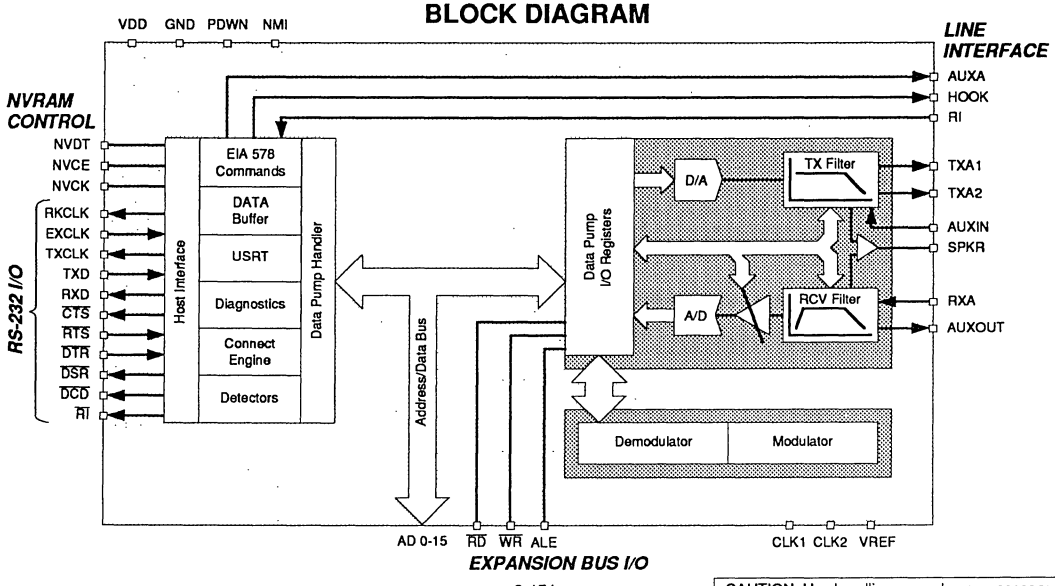
The high level of performance, integrated features, and industry standard user interface provided by the

(Continued)

FEATURES

- **Full G3 facsimile modes including V.21 ch. 2, V.27ter, and V.29**
- **9600, 7200, 4800 bit/s (V.29), 4800, 2400 bit/s (V.27ter), and 300 bit/s (V.21) operation with T.4 and T.30 compatibility**
- **Includes EIA/TIA industry standard (AT) user interface and command interpreter for FAX transmission and reception**
- **Compatible with existing Silicon Systems products for, 1-chip addition of datacom modes**
- **Upgrades to 14.4 kbit/s operation with future Silicon Systems products**
- **Adaptive equalization plus selectable compromise equalizer**
- **Automatically adapts to terminal speeds of 300 to 19.2 kbit/s, with flow control**
- **Includes HDLC framing to facilitate T.30 FAX handshake protocol**
- **Low power operation (450 mW) from a single +5V supply**
- **PLCC packages for surface mount designs**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

73D2291 make it easy to design both FAX and datacom capability into one product. It is ideal for use in personal computer, portable terminal, and Laptop FAX/datacom applications which communicate using existing telephone lines.

OPERATION

The SSI 73D2291 is designed for applications that require half-duplex 9600 bit/s operation over the GSTN. This product is optimized for personal computer-based FAX and related applications which combine both FAX and datacom into a single product. The SSI 73D2291 includes full group 3 FAX modes, along with an industry standard EIA/TIA user interface, providing an AT command interpreter with special commands for control of FAX functions. The 73D2291 provides for simple expansion to include 2400 bit/s datacom modes by adding the SSI 73K224L 1-chip modem, or other Silicon Systems modem products for alternate modes such as V.23 operation, if desired. The SSI 73D2292 is a version of the SSI 73D2291 configured for, and including the SSI 73K224L to provide full FAX and datacom. The SSI 73D2291's AT command interpreter controls the datacom function in this case, eliminating the need for additional circuitry. Other features such as DTMF dialing and detection, call progress detection, and diagnostics are included and may be controlled using selected AT commands.

A complete FAX/datacom modem using the 73D2291/2292 in a PC environment requires only the addition of the phone line interface, a UART, and driver routines or a commercial software program for the PC to handle FAX management, file transfer, and graphics conversion. The SSI 73D2291 is one member in a family of new Silicon Systems products for high speed modem applications. These products allow interchangeable upgrades to higher speeds or alternate modes, while retaining compatibility with existing Silicon Systems 1-chip modem products.

HOST INTERFACE

The EIA 578 standard for PC FAX operation provides for communication of commands and data over a serial RS-232 port. The SSI 73D2291 provides an asynchronous interface and appropriate control signals conforming to this standard to allow data and command transfer between the DTE and DCE.

COMMAND PROCESSOR

The 73D2291/2292's AT command processor (CP) automatically determines the communications speed, character length, and parity of the DTE, and adjusts its operation accordingly, using an autobaud technique. The CP interprets EIA standard "AT" commands, as well as conventional and extended "AT" commands for data communications, and provides appropriate control for both FAX and data modes, eliminating the need for additional circuitry. Other features such as DTMF dialing and detection, call progress detection, and diagnostics are included and may be controlled using selected AT commands. The command processor can also be expanded with external memory to allow integration of popular protocols such as V.42bis for error control and compression used in conjunction with data communications modes.

DATA BUFFER

The CP will autobaud over a range of 110 bit/s to 19.2 kbit/s and can use either hardware flow control (RTS/CTS) or software flow control (XON/XOFF) at high speeds if required making use of an internal 32 byte buffer. Autobaud speed must be at least 20% higher than the data transfer rate of the selected modulation technique for proper operation.

USRT

The SSI 73D2291/2292 can transmit and receive HDLC frames in data modes as needed to support the Group 3 FAX T.30 protocol. In transmit modes the USRT takes data out of the buffer, computes a Frame Check Sum (FCS), does zero insertion, and appends flags. The USRT also filters the data stream from the DTE removing all character pairs beginning with the ASCII <DLE> character (hex $10). In addition, the USRT recognizes the pattern <DLE> <ETX> (hex $10, hex $03) as the stream terminator. The USRT recognizes the pattern <DLE> <DLE> and will reinsert a single <DLE> character in its place. In receive modes, it reverses the process by detecting flags, deleting inserted zeros, and checking FCS for errors which are then reported to the DTE. The USRT also filters the data stream to the DTE and inserts an extra <DLE> (ASCII hex $10) character ahead of <DLE> data.

DATA PUMP

The 73D2291/2292 data pump consists of three sections, the AFE, the DSP, and the CP, as shown in the block diagram. The AFE provides signal conditioning and data acquisition for the DSP, which performs modulation and demodulation under control of the CP. The AFE provides A/D and D/A conversion, scrambler/descrambler functions, timing generation and recovery, and filtering. The DSP section modulates and demodulates data, transmits and detects DTMF and other call progress tones, and provides pattern detection needed to complete the initial call connect sequence. In a data mode transmit operation, the CP receives 8-bit characters, strips start and stop bits, and rate buffers the data with flow control. If HDLC is enabled, the data is formatted as HDLC frames. The DP then extracts data from the buffer for transmission. In a receive operation, the DP processes data received from the phone line. If HDLC is enabled, frames are detected, and data is deposited into the buffer. The buffered data is then formatted into characters by the CP, and transmitted to the DTE.

COMMAND INTERPRETER

The 73D2291/2292 includes an integral command interpreter with the ability to recognize and take action on 3 categories of commands. For conventional data modes, a basic, and an enhanced "AT" command set is included for use with data modem speeds up to 2400 bit/s. An EIA 578 compatible set of "AT" commands is also provided by the 73D2291/2292 for FAX operation. EIA standard commands are similar to data modem "AT" commands, but are preceded by a "+F" character, to distinguish them from basic and extended "AT" commands. In addition to these three groups of commands, special Silicon Systems commands are included that add extra diagnostic and control features to the 73D2291/2292 when operating in FAX mode.

COMMUNICATIONS MODES AND COMPATIBILITY

MODE	SPEED	BAUD RATE	CARRIER (Hz)	MOD. METHOD	APPLICATION
V.29	9600	2400	1700	QAM	FAX G3
	7200	2400	1700	QAM	FAX fallback
	4800	2400	1700	QAM	FAX fallback
V.27ter	4800	1600	1800	DPSK	FAX fallback
	2400	1200	1800	DPSK	FAX fallback
V.21 CH2	300	300	1650/1850	FSK	FAX handshake
V.22bis*	2400	600	2400,1200	QAM	FDX data com
V.22*	1200	600	2400,1200	DPSK	FDX data com
Bell 212A*	1200	600	2400,1200	DPSK	FDX data com
Bell 103*	300	300	2025,2225	FSK	FDX data com
V.21*	300	300	1650/1850 980/1180	FSK	FDX data com

* SSI 73D2292 only

COMPATIBILITY FOR DATA COMMUNICATIONS MODES (SSI 73D2292 only)

Calling a:		73D2292 originating as:				
		Bell		CCITT		
		300	**1200**	**300**	**1200**	**2400**
Bell	300 (103)	300	300	-	-	300
	1200 (212)	300	1200	-	1200	1200
	2400* (224)	300	1200	-	1200	2400
CCITT	300 (V.21)	-	-	300	-	-
	1200 (V.22)	300	1200	-	1200	1200
	2400 (V.22bis)	300	1200	-	1200	2400
Called from a:		**73D2292 answering as:**				
		Bell		CCITT		
		300	**1200**	**300**	**1200**	**2400**
Bell	300 (103)	300	300	-	-	300
	1200 (212)	300	1200	-	1200	1200
	2400 (224)	300	1200	-	1200	2400
CCITT	300 (V.21)	-	-	300	-	-
	1200 (V.22)	300	1200	-	1200	1200
	2400 (V.22bis)	300	1200	-	1200	2400

* A Bell 2400 is a V.22bis using a 2225 Hz answer tone without unscrambled marks.

PIN DESCRIPTION

235 PINS

48-PIN	44-PIN	NAME	DESCRIPTION
36	33	VPA	+5 Analog
37	34	VPD	+5 Digital
13	13	GNA	Analog Ground
12	12	GND	Digital Ground
41	38	CKI	Clock Input (11.0592 MHz)
22	21	RXA	Receive Input
26	24	TX1	Transmitter Output
25	23	TX2	Transmitter Output
24		N/C	No Connect
27	25	AXI	Auxilliary Input
21	20	AXO	Auxilliary Output
23	22	MON	Speaker Output
11	11	CS	Chip Select
14	14	$\overline{CS}$	Chip Select
15	15	$\overline{WR}$	Write Enable

PIN DESCRIPTION (Continued)

73M235 PINS

48-PIN	44-PIN	NAME	DESCRIPTION
16	16	$\overline{RD}$	Read Enable
17	17	ALE	Address Latch Enable
18	18	$\overline{IT}$	Interrupt Request
20	19	NMI	Non Maskable Interrupt
19		N/C	No Connect
6		N/C	No Connect
2-10	3-10	AD0-AD7	Address/Data
	46	43	SO0 Serial Output 0
45	42	SO1	Serial Output 1
1	2	SI0	Serial Input 1
48	1	SI1	Serial Input 1
42	39	SCK	Serial Clock
43	40	TFS	Transmit Frame Sync
44	41	RFS	Receive Frame Sync
47	44	SAK	Serial Acknowledge
39	36	RCK	Receive Bit Clock Output
35	32	TCK	Transmit Bit Clock Output
40	37	XCK	External Bit Clock Input
38	35	RXD	Receive Data
34	31	TXD	Transmit Data
33	30	$\overline{TX}$	Transmit Data (inverted)
28	26	RI	Ring Detect
29	27	HOOK	Hook Relay Control
30		N/C	No Connect
31	28	DRST	DSP Reset
32	29	PWDN	Power Down Output

PIN DESCRIPTION (Continued)

73D640 PIN

40-PIN	44-PIN	NAME	DESCRIPTION
30	34	VCC	+5V
10	1,12,18,29	VSS	Ground
40	44	PA2	Peripheral Address
1	2	PA1	Peripheral Address
2	3	PA0	Peripheral Address
4	5	$\overline{RS}$	Reset
5	6	$\overline{INT}$	Interrupt
6	7	CLK	Clock/4 Output
7	8	X1	Crystal
8	9	CKI/X2	Clock Input/Crystal
9	10	$\overline{BIO}$	Polling Input
	11	N/C	No Connect
3	4	MC	Code Select
27	31	$\overline{PM}$	Code Select
26	30	D0	Data Bus
25	28	D1	Data Bus
24	27	D2	Data Bus
23	26	D3	Data Bus
22	25	D4	Data Bus
21	24	D5	Data Bus
20	23	D6	Data Bus
19	22	D7	Data Bus
11	13	D8	Data Bus
12	14	D9	Data Bus
13	15	D10	Data Bus
14	16	D11	Data Bus
15	17	D12	Data Bus
16	19	D13	Data Bus
17	20	D14	Data Bus
18	21	D15	Data Bus
32	36	$\overline{RD}$	Read Enable
31	35	$\overline{WR}$	Write Enable
28	32	SAK	Serial Acknowledge
29	33	SI0	Serial Input 0
33	37	SI1	Serial Input 1
34	38	SCK	Serial Clock
35	39	SO0	Serial Output 0
36	40	SO1	Serial Output 1
37	41	FR	Frame Output
38	42	TFS	Transmit Frame Sync
39	43	RFS	Receive Frame Sync

PIN DESCRIPTION (Continued)

73D641 PIN

40-PIN	44-PIN	NAME	DESCRIPTION
	1	N/C	No Connect
1	2	$\overline{DSR}$	Modem Ready
2	3	$\overline{DTR}$/NVCK	Terminal Ready
3	4	NVCE	EEProm Enable
4	5	$\overline{RI}$	Ring Indicate
5	6	$\overline{DCD}$	Carrier Detect
6	7	$\overline{CTS}$	Transmit Flow Control
7	8	$\overline{RTS}$/NVDT	Receive Flow Control
8	9	AUXR	A/A1 Relay Control
9	10	$\overline{RST}$	Reset
10	11	TXD	Transmit Data
	12	N/C	
11	13	RXD	Receive Data
12	14	INT0	"A" Search Interrupt
13	15	INT1	AFE Interrupt
14	16	RXC	Receive Bit Clock
15	17	TXC	Transmit Bit Clock
16	18	$\overline{WR}$	Write Enable
17	19	$\overline{RD}$	Read Enable
18	20	X2	11.0592/22.184 MHz Input
19	21	X1	
20	22	VSS	Ground
	23	N/C	
21-28	24-32	A8-A15	Address Bus
29	32	$\overline{PSEN}$	External ROM Enable
30	33	ALE	Address Latch Enable
	34	N/C	
31	35	EA	External ROM Select
32-39	36-43	AD7-AD0	Address/Data Bus
40	44	VDD	+5V Power

EIA-578 STANDARD "AT" COMMANDS FOR FAX OPERATION

COMMAND	DESCRIPTION/OPTIONS
+FCLASS=n	Sets class of operation for: n = 0 (FAX modem in Data mode). Responds OK if FAX modem, Error if data only modem n = 1 Enables Class 1 commands n = 2 (Reserved)
+FCLASS?	Queries current setting
+FCLASS=?	Reports all possible modes
+FTS=nnn	Stops transmitting, then transmits nnn/100 seconds of silence. After nnn/100 seconds, responds with OK, or executes next command on command line.
+FRS=nnn	Wait for nnn/100 seconds of silence. Responds with OK, or executes next command on command line.
+FTH=nnn	Transmit HDLC frame using modulation nnn. Responds with CONNECT, enters data mode, then begins transmitting HDLC flags. Characters received will be transmitted in HDLC frames. Data overrun will result in closing frames, and occurs if the second byte of the frame is 0 x C8(T.30 final frame byte). In this case the response will be OK, otherwise the modem will respond CONNECT and begin the next frame.
+FRH=nnn	Receive HDLC frame using modulation nnn. Modem responds with CONNECT if flags are detected. If no carrier is detected the modem responds NO CARRIER. If another carrier is detected the modem responds +FCERROR (+F4). The end of data is indicated by <DLE><ETX> from modem. The 2 bytes preceding the end of frame will be the FCS. Following the end of frame the modem will respond OK or ERROR indicating the status of the FCS.
+FTM=nnn	Transmit using modulation nnn. Will respond CONNECT after completion of the training sequence. Data mode will be terminated if a character other than NUL (oxoo) is the last character transmitted when underrun occurs, or a <DLE><ETX> is encountered.
+FRM=nnn	Receive using modulation nnn. Will respond CONNECT after completion of the training sequence. Will respond +FCERROR(+F4) if another modulation type is detected. Sends data followed by <DLE><ETX> ok.
+ACU?	Query EIA command capability. Modem responds OK if available.
+CNG=<Hz>	Enable selected Transmit calling tone of Hz frequency.
+MFR?	Query manufacturer name. Responds with manufacturer's name.
+MDL?	Query product model. Responds with MFG. product model.
+Rad(ix)=n	Set base for numeric results as shown: 0 = Decimal 1 = Hex 2 = Binary
+REV?	Query component revision number. Responds with individual component device numbers and revision in form "Device.rev"

Modulation codes for above commands:

nnn = Code	*Speed*
3	300
24	2400
48	4800
72	7200
96	9600
120	12000 (reserved)
144	14400 (reserved)

Note: The host must protect <DLE> characters in the data with another <DLE>, and strip extra <DLE> on reception.

SILICON SYSTEMS EXTENDED COMMANDS

COMMAND	DESCRIPTION/OPTIONS
%ATT=nn	Sets transmit attenuator for value of nn = 0 to 15 dB.
%DAA=n	Selects DAA configuration for RJ11 (n=0) or RJ45 (n=1).
%EQU=n	Configures link and cable equalizers in RX and TX directions. The preceding 3 commands are issued only once for initialization of NVRAM. If NVRAM is not present, then default values are used.
%ERASE	Erases NVRAM to allow reconfiguration of hardware parameters.
%DACa= pnnnb%	Displays diagnostic information as follows when in diagnostic mode: *Value* — *Action* a = X or Y — Selects D/A address X or Y p = A (AFE), D (DSP), R (RAM), U (controller) — Selects source for data nnn = Hex # 000—FFF — Selects memory location b = H/L — Selects high or low memory byte
%DEBUG=n	Enables diagnostic modes and updates as follows: *"n" Value* *Action* 0 Disable diagnostic (default) 1 Enable diagnostic display at interrupt rate 2 Enable diagnostic display update every 10 ms
%DUMP= pnnnb	Dumps RAM location nnn of selected device to serial port. Command is aborted by expiration of S18 test timer or receipt of %DUMP command. Parameters are same as for %DAC command.
%BITa= pnnn.b	Display RAM bit b of location nnn for selected device p to test bit a. Bit a is the $\overline{RI}$ pin. Bit b is $\overline{DSR}$. Default addresses are RI and DSR.
%PDWN=nnn	Sets automatic power down mode for nnn as shown below. The modem will be awakened by either a negative edge from $\overline{RING}$, or a NMI transition (normally caused by UART write access decode or TXD input). *"n" Value* *Action* 0 immediately enters powerdown 1-254 enters powerdown after nnn sec. of inactivity (only if on hook and not in test modes) 255 will not enter power down (default)

BASIC "AT" COMMAND SET*

COMMAND & DESCRIPTION

A — Answer call
In FAX Mode:
1. *Modem goes off hook*
2. *Waits billing delay*
3. *Optionally reports CNG presence (1100 Hz)*
4. *Sends 3 seconds of CED tone (2100 Hz)*
5. *Begins V.21 HDLC preamble (1 sec. of flags)*

A/ — Repeat last command

D*s* — Dial using Dial string "s"
In FAX Mode:
1. *Modem goes off hook*
2. *Optionally searches for dial tone*
3. *Dials number (processing embedded dial mods.)*
4. *Optionally generates CNG (1100 Hz)*
5. *Optionally reports presence of CED (2100 Hz)*
6. *Reports CONNECT when V.21 HDLC flags are detected*

Dial Modifiers

Modifier	*Description*
0-9 * #	digits/characters for dialing
A B C D	
P	pulse dial (factory setting)
T	tone dial
,	delay processing of next character
!	hookflash
@	wait for quiet answer
W	wait for dial tone
;	return to command state after dialing
R	reverse mode (to call an originate-only modem)
S=n	dial stored number in location "n" (n = 0...3)

E[0|1] — Command local echo
E0 Disabled
E1 Enabled

H[0|1] — Hook relay control
H0 Go on hook (hang up)
H1 Go off hook

I*n* — Identify
I0 Product code
I1 ROM check sum
I2 Check ROM check sum

L*n* — Speaker volume
L0,1 Low
L2 Medium
L3 High

M*n* — Speaker mode
M0 Speaker off
M1 Speaker on during connect only
M2 Speaker always on
M3 Speaker on during call progress

P — Pulse dial

Q*n* — Quiet mode, enables command responses
Q0 Responses enabled
Q1 Responses disabled

S*n* — S registers
S*n=nnn* set "S" register to value
S*n*? query current "S" register value

T — Tone dial

V[0|1] — Verbose command responses
V0 Enable terse numeric response
V1 Enable verbose responses

Z*n* — Reset to configuration *n* in EEPROM

EXTENDED "AT" COMMAND SET**

COMMAND & DESCRIPTION

&C[0|1] — DCD modes
&C0 DCD always on
&C1 DCD follows carrier detect

&D*n* — DTR modes
&D0 Ignore DTR
&D1 Go to command state if ON-to-OFF detected
&D2 Go to command state and disable autoanswer if ON-to-OFF detected
&D3 Initialize modem with EEPROM if ON-to-OFF detected

&F — Factory configuration. Restores modem to factory settings.

&J[0|1] — Auxilliary relay control
&J0 AUXR off
&J1 AUXR follows HOOK

&M*n* — Synchronous modes
&M0 Asynchronous
&M1 Sync mode entered upon completion of dial
&M2 Dial stored number on OFF-to-ON transition of DTR and go on-line
&M3 Manual dial using DTR as Talk/Data switch

&P[0|1] — Pulse dial make/break ratio
&P0 US 39%/61%
&P1 UK/HK 33%/67%

&S*n* — DSR modes
&S0 DSR always on
&S1 DSR normal

&T*n* — Test modes (TBD)

&V — Display current configuration

&W*n* — Write configuration to EEPROM

&Y*n* — Select power up EEPROM configuration

&Z*n=s* — Store telephone number "s" in EEPROM location "n"

Notes: ***Italicized*** parameters indicate default settings.
If a parameter (0, 1, etc.) is not specified, the modem assumes the 0 parameter.

* Basic AT commands consist of a single letter optionally followed by a numeric argument. The numeric argument can be 1 or 0 indicating a TRUE or FALSE condition. No argument means "0." The numeric argument can also be a decimal number in the range 0-255.

** Extended AT commands are preceded by an ampersand.

S-REGISTER SUMMARY

Reg.	Description	Range:Default
S0	select ring to answer on	0-255 rings:0
S1	ring count (incremented with each ring)	0-255 rings
S2	define escape sequence character	0-127 ASCII:43
S3	define carriage return character	0-127 ASCII:13
S4	define line feed character	0-127 ASCII:10
S5	define back space character	0-32, 127 ASCII:8
S6	select wait time before blind dialing	2-255 sec.:10
S7	select wait time for carrier/dial tone	1-255 sec.:30
S8	select duration of comma dial modifier	0-255 sec.:2
S9	select carrier detect response time	1-255 1/10 sec.:6
S10	select time between carrier loss/hang up	1-255 1/10 sec.:14
S11	define duration/spacing of tones	50-255 ms:70
S12	define escape frequency guard time	0-255 1/50 sec.:50
S14	bit mapped options Bit 1 - En Command Echo :1 Bit 2 - Qn Quiet :0 Bit 3 - Vn Verbose Results :1 Bit 5 - Tone (0), Pulse (1) Dial :0 Bit 7 - Answer (0), Originate (1) :1	
S16	modem test options Bit 0 - &T1 Analog Loopback :0 Bit 2 - &T3 Local Digital Loopback :0 Bit 6 - &T8 ALB with self test :0	
S18	modem test timer	0-255 sec.:0
S21	modem test options Bit 0 - &Jn Auxilliary Relay :0 Bit 3, 4 - DTR Modes 00 - &D0 01 - &D1 10 - &D2 11 - &D3 Bit 5 - &Cn DCD :0 Bit 6 - &Sn DSR :0	

Reg.	Description	Range:Default
S22	bit mapped options Bit 0, 1 - Speaker Volume 00 - res. 01 - L1 10 - L2 11 - L3 Bit 2, 3 - Speaker Modes 00 - M0 01 - M1 10 - M2 11 - M3 Bit 4, 5, 6 - Call Progress 000 - X0 001 - res. 010 - res. 011 - res. 100 - X1 101 - X2 110 - X3 111 - X4 Bit 7 - &Pn Pulse Type	
S23	bit mapped options Bit 0, 1 - Speaker Volume 00 - res. 01 - L1 10 - L2 11 - L3 Bit 2, 3 - Speaker Modes 00 - M0 01 - M1 10 - M2 11 - M3 Bit 4, 5, 6 - Call Progress 000 - X0 001 - res. 010 - res. 011 - res. 100 - X1 101 - X2 110 - X3 111 - X4 Bit 7 - &Pn Pulse Type	
S25	detect DTR change timer	0-255 1/100 sec.:5
S27	bit mapped options Bit 0, 1 - Sync Mode 00 - &M0 01 - &M1 10 - &M2 11 - &M3 Bit 4, 5 - Sync Mode 00 - &X0 01 - &X1 10 - &X2 11 - &X3	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITION	MIN	NOM	MAX	UNITS
Ambient Temperature, Ta		0		70	°C
Supply Voltage, VCC, VDD		4.75		5.25	V
Input Low Voltage, VIL		0		0.8	V
Input High Voltage, VIH		2.0		VDD	V
Output Low Current				1.6	mA
Output High Current		-0.4			mA
Digital Load Capacitance				50	pF
Input Clock Frequency, X2 XTL2, CKI			22.1184 11.0592		MHz
Input Clock Variation, X1, XIN	XIN must be (X1) ÷ 2	-0.01		0.01	%

DC ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
IDD	Supply Current				110	mA
IIH	Input High Current				10	µA
IIL	Input Low Current		-10			µA
	Digital Input Capacitance				10	pF
VOH	Output High Voltage	Iout = -0.4 mA	2.4			V
VOL	Output Low Voltage	Iout = 1.6 mA			0.4	V
RXA	Input Resistance		100			kΩ
RXA	Input Capacitance				25	pF

APPLICATIONS INFORMATION

The SSI 73D2291/2292 includes features and commands that are needed to design a full featured FAX/Datacom modem with industry standard "AT" commands and functions. All control software needed for modem control, AT user interface, and FAX modes are included within the device set. A complete basic modem requires the addition of an RS-232 or UART interface, and an appropriate telephone line interface. PC resident software then performs the T.4 FAX compression/decompression and format manipulation for proper screen display or print-out. Software can be customized for specific applications, or commercial software packages can be used that support FAX operation using the EIA 578 interface.

Optional features that are provided for in the 73D2291/2922 and that may be included in a full-featured modem design include: Non-volatile memory for storage of set-up parameters; a speaker and amplifier for audible monitoring of call activity; and LEDs for display of modem status.

For data communication modes, the SSI 73D2292 employs an AT command set user interface that is compatible with existing modem products and software. With this interface, the user can directly control a modem using simple AT commands, or commercially available communications software programs such as Smartcom™ may be used to provide a menu driven interface and additional features that make the modem easier to use.

The FAX operating sequence is similar to, but more complex than that required for data communication, as the FAX operation adds the additional format conversion and file compression steps to normal data transfer. The industry standard EIA/TIA "AT" user interface included in the 73D2291/2922 provides a high level user interface to the FAX modem function. FAX data pump control, format conversion, and compression must be implemented by external communications software. A compatible communications software package, in conjunction with the 73D2291/2292 will provide full FAX capability. The industry standard user interface provided in the 73D2291/2292 is expected to be widely supported in the future by popular commercial software programs.

SAMPLE T.30 FAX HANDSHAKE SESSION

The following table is a sample FAX connect session using the EIA 578 defined "AT" commands incorporated in the SSI 73D2291/2292. All transmissions take place at 19.2 kbit/s using 8-bit characters and no parity setting. Verbose result codes are shown for clarity. Binary data formatted as characters is shown as <DATA>.

EXAMPLE: Single Page FAX Transmission Without Any Reported Problems

DTE Commands	DCE Responses	Local DCE Action	Remote DCE Action	Notes
AT+FCLASS=1	OK	set to Class 1		
ATDT5846161	CONNECT <NSF Frame> <DLE><ETX> OK	1) Dials 2) Enters V.21 HDLC Receive 3) Detects HDLC Flags	1) Answers 2) Sends CED 3) Sends HDLC Flags Sends NSF Frame	AT+FRH=3 implied by dialing +FCLASS=1
AT+FRH=3	CONNECT <CSI Frame> <DLE><ETX> OK	Detect Flags	Sends CSI	Frame Status
AT+FRH=3	CONNECT <DIS Frame> <DLE><ETX> OK	Detect Flags	1) Sends DIS 2) Drops Carrier 3) Receives Flags	
AT+FRH=3	NO CARRIER	Detects loss of Carrier		
AT+FTH=3 <TSI Frame> <DLE><ETX> <DCS Frame> <DLE><ETX>	CONNECT CONNECT OK	Send Flags 1) Sends Frame 2) Appends FCS 3) Appends Flag 1) Sends Frame 2) Appends FCS 3) Appends Flag 4) Drops Carrier	Receives TSI Receives DCS	Final Frame
AT+FTS=8	OK	waits 80ms		
AT+FTM=96 <TCF Frame> <DLE><ETX>	CONNECT OK	Transmits V.29 (9600) Drops Carrier	 Receives and Checks TCF	

EXAMPLE: Single Page FAX Transmission Without Any Reported Problems (continued)

DTE Commands	DCE Responses	Local DCE Action	Remote DCE Action	Notes
AT+FRH=3	CONNECT <CFR Frame> <DLE><ETX> OK	Detects Flags	1) Sends CFR 2) Drops Carrier	Frame Status
AT+FRH=3	NO CARRIER	Detects loss of Carrier		
AT+FTM=96 <page data> <DLE><ETX>	CONNECT OK	Transmits V.29 Drops carrier	Receives page data	
AT+FTH=3 <EOP Frame> <DLE><ETX>	CONNECT OK	Sends Flags 1) Sends Frame 2) Appends FCS 3) Appends Flag 4) Drops Carrier	Receives EOP	Final Frame
AT+FRH=3	CONNECT <MCF Frame> <DLE><ETX> OK	Detects Flags	Sends MCF Drops Carrier	Frame Status
AT+FRH=3	NO CARRIER	Detects loss of Carrier		
AT+FTH=3 <DCN Frame> <DLE><ETX>	CONNECT OK	Sends Flags 1) Sends Frame 2) Appends FCS 3) Appends Flag 4) Drops Carrier	Receives DCN Hangs up	Final Frame
ATH0	OK	Hangs up		

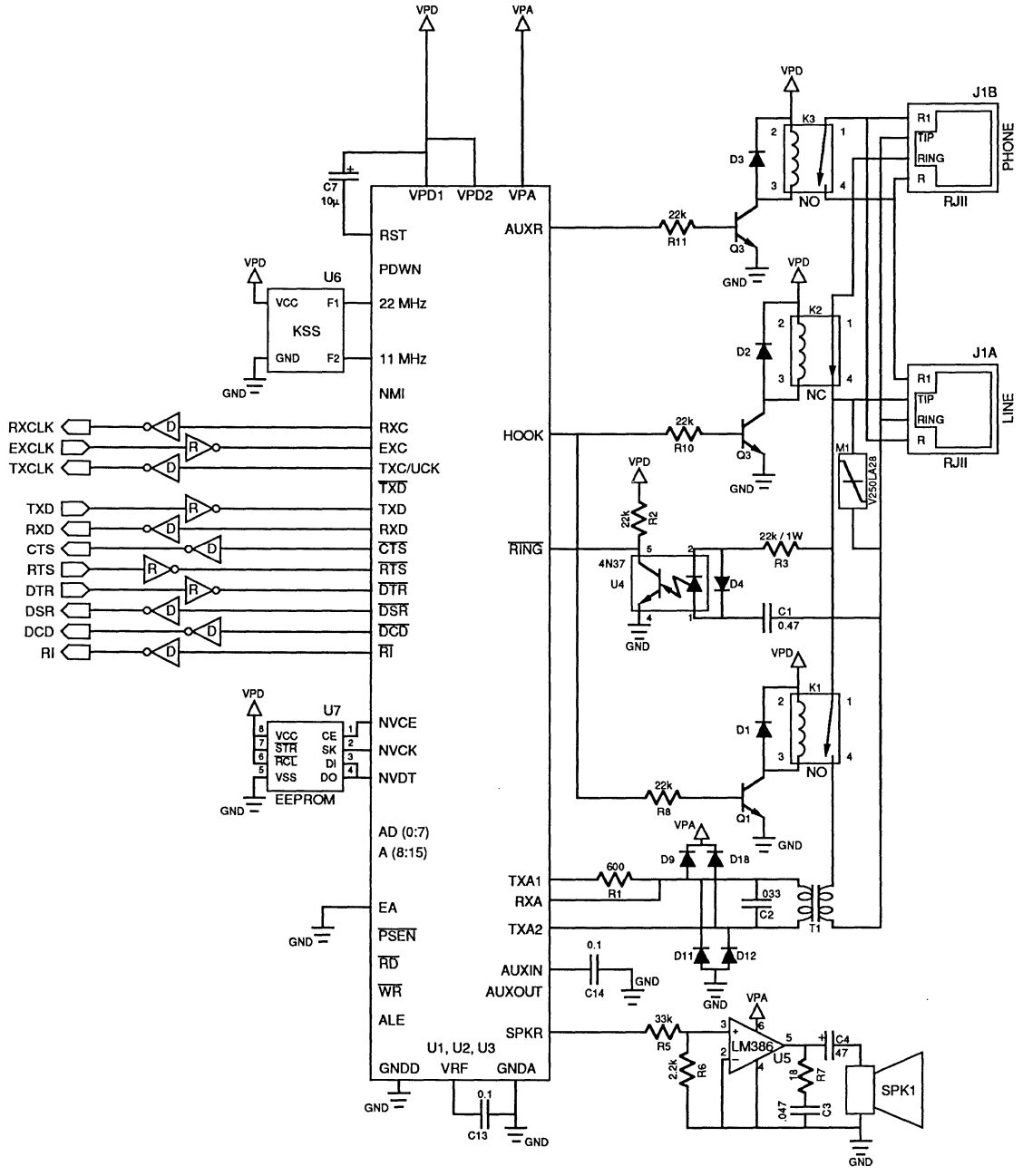
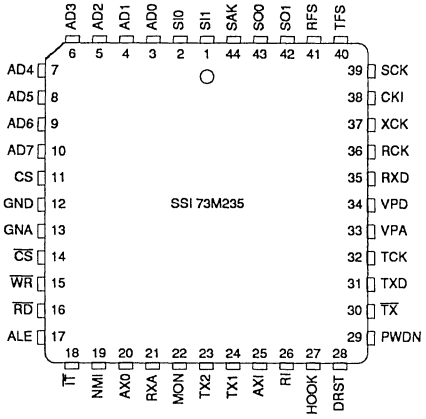
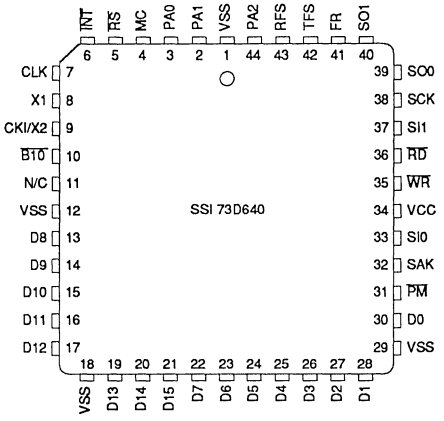


FIGURE 2: SSI 73D2291 Typical Application - FAX Modem

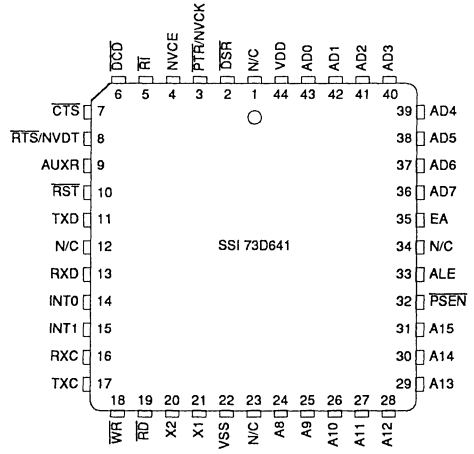
PACKAGE PIN DESCRIPTIONS (TOP VIEW)



44-Pin PLCC



44-Pin PLCC



44-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 73D2331/2332
V.17 FAX Modem Device Set with EIA 578 User Interface

Advance Information

July, 1990

2

DESCRIPTION

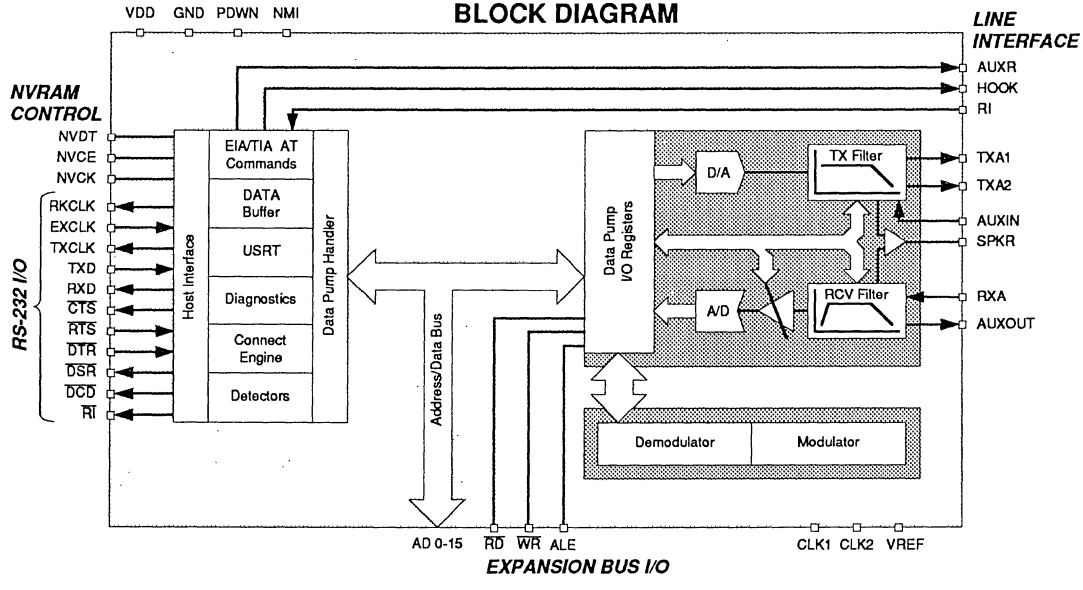
The SSI 73D2331 is a CMOS device set that allows 14.4 kbit/s transmit and receive facsimile data communication over the dial-up telephone network. The 73D2331 conforms to CCITT V.17, V.29 and V.27ter standards as defined for FAX operation, and it includes an EIA 578 industry standard "AT" user interface for high level control of FAX functions in Personal Computers, or similar applications. The "AT" command set provided by the 73D2331's user interface simplifies control of the FAX modes, and insures compatibility with personal computer applications software designed for FAX communications.

The 73D2331 employs the same control architecture used in Silicon Systems' 1-chip modem products, and is compatible with these devices. 2400 bit/s data communications modes can be incorporated into the product by the addition of the SSI 73K224L 1-chip modem (73D2332 product.) Other Silicon Systems 1-chip modems may also be used to provide alternate data communications modes. (continued)

FEATURES

- **High speed G3 facsimile modes including V.21 ch.2, V.27ter, V.17, and V.29**
- **14,400 bit/s (V.17), 9600, 7200, 4800 bit/s (V.29), 4800, 2400 bit/s (V.27ter), and 300 bit/s (V.21) operation**
- **Includes EIA 578 industry standard ("AT") user interface and command interpreter**
- **Compatible with existing Silicon Systems products for easy upgrades**
- **Trellis encoding forward error correction with fast training capability in V.17 modes at speeds of 14,400, 1200, 9600, and 7200 bit/s**
- **Automatically adapts to terminal speeds of 300 to 19,200 bit/s, with flow control**
- **Includes HDLC framing to facilitate T.30 FAX handshake protocol**
- **Low power CMOS design operates from a single +5V supply**
- **Compact DIP or PLCC packages for surface-mount designs**

BLOCK DIAGRAM



DESCRIPTION (Continued)

The 73D2331's built-in AT command interpreter can control both the FAX and data communications modes, eliminating the need for separate controllers and additional components.

The high level of performance, integrated features, and industry standard user interface provided by the 73D2331 make it easy to design both FAX and data communications capability into one product. It is ideal for use in personal computer, portable terminal, and Lap-top FAX/data communications applications which communicate using existing telephone lines.

OPERATION

The SSI 73D2331 is designed for applications that require high speed operation at 14,400 bit/s over the General Switched Telephone Network (GSTN). This product is optimized for Personal Computer-based FAX and related applications which combine both FAX and data communications into a single product. The 73D2331 includes the new V.17 high performance FAX mode using Trellis encoding, for speeds of 14,400, 12000, 9600, and 7200 bit/s. Full group 3 FAX modes, and an industry standard EIA 578 user interface are also included, providing an "AT" command interpreter with special commands for control of FAX functions. The 73D2331 provides for simple expansion to include 2400 bit/s data communications modes by adding SSI's 73K224L 1-chip modem, or other Silicon Systems modem products for special modes of operation. The 73D2332 is a version of the 73D2331 configured for, and including the 73K224L to provide full FAX and data communications capability.

A complete FAX/data communications modem using the 73D2331/2 in a PC environment requires only the addition of the phone line interface, a UART, and driver routines or a commercial software program for the PC to handle FAX management, file transfer, and graphics conversion. The 73D2331 is one member in a family of new Silicon Systems products for high speed data communications applications. These products allow interchangeable upgrades to different speeds or alternate modes, while retaining compatibility with existing Silicon Systems 1-chip modem products.

HOST INTERFACE

The EIA 578 standard for PCFAX operation provides for communication of commands and data over a serial RS-232 port. The SSI 73D2331 provides an asynchronous interface and appropriate control signals conforming to this standard to allow data and command transfer between the DTE and DCE.

COMMAND PROCESSOR

The 73D2331/2's AT command processor (CP) automatically determines the communications speed, character length, and parity of the DTE, and adjusts its operation accordingly, using an autobaud technique. The CP interprets EIA standard "AT" commands, as well as conventional and extended "AT" commands for data communications, and provides appropriate control for both FAX and data modes, eliminating the need for additional circuitry. Other features such as DTMF dialing and detection, call progress detection, and diagnostics are includes and may be controlled using selected AT commands. The command processor can also be expanded with external memory to allow integration of popular protocols such as V.42bis for error control and compression used in conjunction with data communications modes.

DATA BUFFER

The CP will autobaud over a range of 110 bit/s to 19,200 bit/s and can use either hardware flow control (RTS/CTS) or software flow control (XON/XOFF) at high speeds, if required, making use of an internal 32 byte buffer. Optional RAM may be added to extend buffer size, if needed. Autobaud speed must be at least 20% higher than the data transfer rate of the selected modulation technique for proper operation.

USRT

The SSI 73D2331/2 can transmit and receive HDLC frames in data modes as needed to support the Group 3 FAX T.30 protocol for completion of handshake. In transmit modes the USRT takes data out of the buffer, computes a Frame Check Sum (FCS), does zero insertion, and appends flags. The USRT also filters the data stream from the DTE removing all character pairs beginning with the ASCII <DLE> character (hex $10>). In addition the USRT recognizes the pattern <DLE> <ETX> (hex $10, hex $03) as the stream terminator. The USRT also recognizes the pattern <DLE><DLE> and reinsert a single <DLE> character in its place. In receive modes, it reverses the process by detecting flags, deleting inserted zeros, and checking FCS for errors which are then reported to the DTE. In addition, the USRT filters the data stream to the DTE and inserts an extra <DLE> (ASCII hex $10) character ahead of <DLE> data.

DATA PUMP

The 73D2331/2 data pump consists of three sections, the AFE, the DSP, and the CP, as shown in the block diagram. The AFE provides signal conditioning and data acquisition for the DSP, which performs modulation and demodulation under control of the CP. The AFE provides A/D and D/A conversion, scrambler/descrambler functions, timing generation and recovery, and filtering. The DSP section

DATA PUMP (Continued)

modulates and demodulates data, transmits and detects DTMF and other call progress tones, and provides pattern detection needed to complete the initial call connect sequence. In a data mode transmit operation, the CP receives 8 bit characters, strips start and stop bits, and rate buffers the data with flow control. If HDLC is enabled, the data is formatted as HDLC frames. The DP then extracts data from the buffer for transmission. In a receive operation, the DP processes data received from the phone line. If HDLC is enabled, frames are detected, and data is deposited into the buffer. The buffered data is then formatted into characters by the CP, and transmitted to the DTE.

COMMAND INTERPRETER

The 73D2331/2332 includes an integral command interpreter with the ability to recognize and take action on 3 categories of commands. For conventional data modes, a basic, and an enhanced "AT" command set is included for use with data modem speeds up to 2400 bit/s. An EIA 578 compatible set of "AT" commands is also provided by the 73D2291/2292 for FAX operation. EIA standard commands are similar to data modem "AT" commands, but are preceded by a "+" character, to distinguish them from basic and extended "AT" commands. In addition to these three groups of commands, special Silicon Systems commands are included that add extra diagnostic and control features to the 73D2331/2332 when operating in FAX mode.

APPLICATIONS INFORMATION

The SSI 73D2331/2332 includes features and commands that are needed to design a full featured FAX/Datacom modem with industry standard "AT" commands and functions. All control software needed for modem control, AT user interface, and FAX modes are included within the device set. A complete basic modem requires the addition of an RS-232 or UART interface, and an appropriate telephone line interface. PC resident software then performs the T.4 FAX compression/decompression and format manipulation for proper screen display or print-out. Software can be customized for specific applications, or commercial software packages can be used that support FAX operation using the EIA 578 interface.

Optional features that are provided for in the 73D2331/2332 and that may be included in a full-featured modem design include: non-volatile memory for storage of set-up parameters; a speaker and amplifier for audible monitoring of call activity; and LEDs for display of modem status. For data communication modes, the 73D2332 employs an AT command set user interface that is compatible with existing modem products and software. With this interface, the user can directly control a modem using simple AT commands, or commercially available communications software programs such as Smartcom™ may be used to provide a menu driven interface and additional features that make the modem easier to use.

COMMUNICATIONS MODES AND COMPATIBILITY

MODE	SPEED	BAUD RATE	CARRIER (Hz)	MOD. METHOD	APPLICATION
V.17	14,400	2400		Trellis	V.17 FAX
V.29	9600	2400	1700	QAM	FAX G3
	7200	2400	1700	QAM	FAX fallback
	4800	2400	1700	QAM	FAX fallback
V.27ter	4800	1600	1800	DPSK	FAX fallback
	2400	1200	1800	DPSK	FAX fallback
V.21	300	300	1650, 1850	FSK	FAX handshake
V.23	1200	1200	1300, 2100	FSK	Videotex
(73D2332 only)					
V.22bis	2400	600	2400, 1200	QAM	FDX data com
V.22	1200	600	2400, 1200	DPSK	FDX data com
Bell 212A	1200	600	2400, 1200	DPSK	FDX data com
Bell 103	300	300	FSK	FSK	FDX data com
V.21	300	300	FSK	FSK	FDX data com

COMPATIBILITY FOR DATA COMMUNICATIONS MODES (SSI 73D2332 only)

		73D2331 originating as:				
		Bell		CCITT		
Calling a:		300	1200	300	1200	2400
Bell	300 (103)	300	300	-	-	300
	1200 (212)	300	1200	-	1200	1200
	2400* (224)	300	1200	-	1200	2400
CCITT	300 (V.21)	-	-	300	-	-
	1200 (V.22)	300	1200	-	1200	1200
	2400 (V.22bis)	300	1200	-	1200	2400
		73D2332 answering as:				
		Bell		CCITT		
Called from a:		300	1200	300	1200	2400
Bell	300 (103)	300	300	-	-	300
	1200 (212)	300	1200	-	1200	1200
	2400 (224)	300	1200	-	1200	2400
CCITT	300 (V.21)	-	-	300	-	-
	1200 (V.22)	300	1200	-	1200	1200
	2400 (V.22bis)	300	1200	-	1200	2400

* A Bell 2400 is a V.22bis using a 2225 Hz answer tone without unscrambled marks.

APPLICATIONS INFORMATION (Continued)

The FAX operating sequence is similar to, but more complex than that required for data communication, as the FAX operation adds the additional format conversion and file compression steps to normal data transfer. The industry standard EIA "AT" user interface included in the 73D2331/2332 provides a high level control interface for the FAX modem function. FAX data pump control, format conversion, and compression must be implemented by external communications software. A compatible communications software package, in conjunction with the 73D2331/2332 will provide full FAX capability. The industry standard user interface provided in the 73D2331/2332 is expected to be widely supported in the future by popular commercial software programs.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 73M376
Integrated Line Interface

Preliminary Data

July, 1990

2

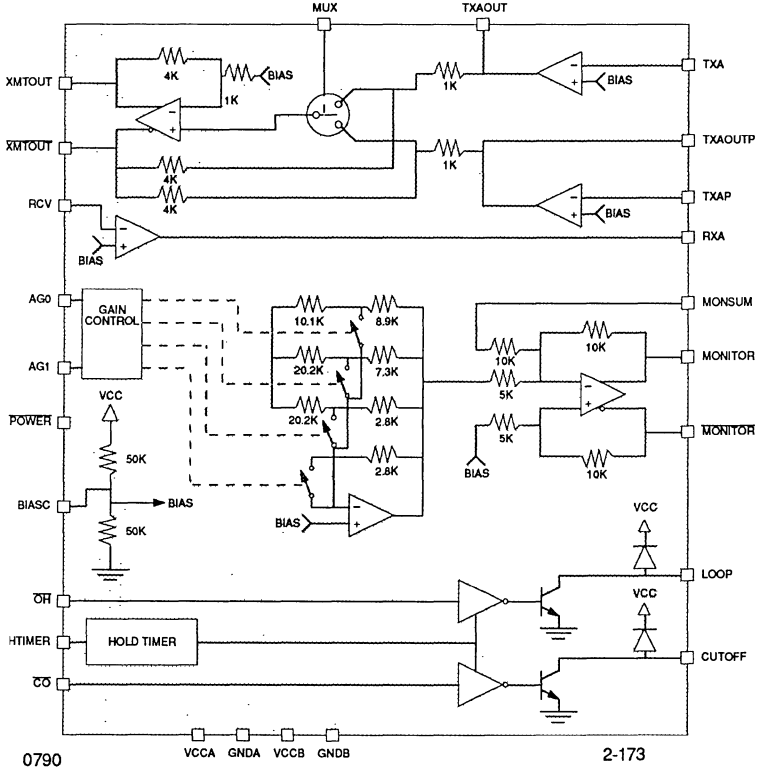
DESCRIPTION

The SSI 73M376 K-Series Integrated Line Interface Unit(LIU) enables the modem to make direct connections to the Public SwitchedTelephone Network. This single chip data access arrangement integrates all external active (line side) components required in K-series modem designs. The SSI 73M376 operates from a single 5 volt supply ideally suited for low power portable applications. Along with the transmit and receive function, it provides transmit and receive amplifiers, programmable audio monitor, and relay drivers. In the transmit path it has provision for level programmable gain path as well as a normal gain path which can be switched via a TTL input. The 73M376 comes in a 28-lead PLCC package.

FEATURES

- **One-Chip data access arrangement**
- **Compatible with all SSI K-Series Modem Products**
- **On-board receive and transmit paths. Transmit has level protected programmability**
- **On-board differential speaker driver with four step variable gain**
- **On-board relay driver with power conserving hold state**
- **Low power (85 mW) with power down mode (25 mW) when on-hook**
- **Operates from a single +5V supply**

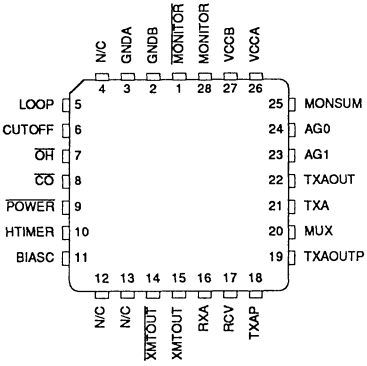
BLOCK DIAGRAM



0790

2-173

PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The transmit output uses a differential drive to allow undistorted signals to be sent with a single 5 volt supply. Each output supplies half the drive signal to the transformer thus increasing the available output amplitude by 100%. Two dedicated transmit op-amps are supplied with the outputs and minus inputs brought out so that external resistors and capacitors can be connected facilitating gain setting and filtering. The TTL input, MUX, switches the output of the op-amps to the differential driver. If the MUX input is pulled high, or left floating, the TXA op-amp is selected. If the MUX input is pulled low the TXAP op-amp is selected.

The receive input, RCV, is the minus input of a dedicated op-amp where external resistors and capacitors can be connected facilitating gain setting and filtering. The bias, or plus, input for all the dedicated op-amps are connected to a VCC/2 bias point which allows for maximum swing between the supply rails. The VCC/2 bias point is brought out to an external pin, BIASC, where a compensation capacitor can be connected for power supply noise filtering.

The audio monitor gain stage has the RXA output as its input and has four gain settings; off or squelch, low, medium, and high. The output of the gain cell is fed to a summer where a signal can be summed in through the MONSUM pin. The audio amp differential output can drive an 8Ω speaker with up to 400 mW rms of power. A capacitor needs to be in series with the speaker so no DC current will flow.

On board relay drivers can directly drive the loop and cutoff relays. The TTL input $\overline{OH}$ (Off Hook) controls the loop relay driver. The TTL input $\overline{CO}$ (Cut Off) controls the cutoff relay driver. A timer, which uses an external timing capacitor connected to the HTIMER pin, is available to set a delay after relay energizing before the driver will go into its hold state. A negative transition on $\overline{OH}$ or $\overline{CO}$ starts the timer. When the timer has expired, both relay drivers will go into the hold state. While the timer is timing the relay drivers are in their full energizing state. If $\overline{OH}$ is low and $\overline{CO}$ goes low before the timer expires, or vice versa, then the timer will reset and start timing again.

The TTL input $\overline{POWER}$ controls the power down state. When $\overline{POWER}$ is low the part is powered up and when it is high, it is in its power down state.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCCA	I	Analog power supply input.
VCCB	I	Digital power supply input.
GNDA	I	Analog ground pin.
GNDB	I	Digital ground pin.
TXA	I	Negative input to transmit op-amp.
TXAOUT	O	Transmit amplifier output.
TXAP	I	Minus level programmed transmit op-amp input.
TXAOUTP	O	Level programmed transmit amplifier output.
MUX	O	Transmit amplifier outputs mux control (TTL).
XMTOUT	O	Transmit output.
$\overline{XMTOUT}$	O	Transmit output (inverted).
RCV	I	Negative input to receive amplifier.
RXA	O	Receive amplifier output.
MONITOR	O	Positive audio amplified output.
$\overline{MONITOR}$	O	Negative audio amplified output.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
MONSUM	I	Monitor summing input.
AG0	I	Bit1 (TTL) input to set audio gain.
AG1	I	Bit2 (TTL) input to set audio gain.
BIASC	I	VCC/2 bias compensation point.
$\overline{OH}$	I	Off hook TTL compatible input. Controls the loop relay
$\overline{CO}$	I	Cut off TTL compatible input. Controls the cutoff relay.
HTIMER	I	Relay hold timing control pin.
LOOP	O	Loop relay drive output.
CUTOFF	O	Cutoff relay drive output.
$\overline{POWER}$	I	Power Down TTL compatible input. Controls power down mode

ELECTRICAL SPECIFICATIONS

ABSOULUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
VCC Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	300	°C

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified 4.50V < Vcc < 5.50V and 0°C < T(ambient) < 70°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC SUPPLY VOLTAGE					
+5V	$\overline{POWER}$ low Outputs unloaded			17.0	mA
+5V	$\overline{POWER}$ high			5.0	mA
Junction Temperature	Relay drivers in hold state driving maximum current. MONITOR, $\overline{MONITOR}$ driving 8Ω speaker to max rms power			135	°C

DIGITAL PINS
(TTL compatible inputs: AG0, AG1, $\overline{OH}$, $\overline{CO}$, MUX, $\overline{POWER}$ pins)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Input low voltage	(VIL)	-0.3		0.8	V
Input high voltage	(VOH)	2.0		VCC+0.3	V
Input low current	VIL = 0.4 V	0.0		-0.4	mA
Input high current	VIH = 2.4 V			100	µA

TRANSMIT AND RECEIVE SECTION

Transmit Gain Single ended into Differential	$\frac{(XMTOUT - \overline{XMTOUT})}{TXAOUT}$ MUX=High	11.5		12.5	dB
Transmit Gain Single ended into Differential	$\frac{(XMTOUT - \overline{XMTOUT})}{TXAOUTP}$ MUX=Low	11.5		12.5	dB
XMTOUT, $\overline{XMTOUT}$ Differential Output Impedance				30	Ω
Transmit THD	7V p-p differential From TXA or TXAP to XMTOUT-$\overline{XMTOUT}$ with Op-Amp gain=0dB @ 4 kHz Zload = 600 Ω speaker driver off			-56	dB
Max. Capacitive differential load XMTOUT, $\overline{XMTOUT}$				300	pF
RCV, TXA, TXAP input impedance			1		MΩ
RCV, TXA, TXAP input offset voltage	RCV - VCC/2 TXA - VCC/2 TXAP - VCC/2		10		mV
RCV, TXA, TXAP input bias current	Vin = VCC/2			500	nA
Receive THD	From receive Op-Amp input to RXA with Op-Amp gain=8dB 4 kHz speaker driver off			-56	dB
Max. Capacitive load, TXAOUT, TXAOUTP, RXA				150	pF
Transmit and Receive Op-Amps Unity Gain Bandwidth			500		kHz
BIASC impedance V_{BIASC}=VCC/2		18K		32K	Ω

MONITOR OUTPUT CIRCUIT

(All of the measurements are made with an 8Ω load, tied from MONITOR to $\overline{\text{MONITOR}}$, AC coupled through a 20 µF capacitor.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Gain	From RXA to Monitor outputs (MONITOR-$\overline{\text{MONITOR}}$)/RXA AG0=Low, AG1=Low			-60	dB
	AG0=High, AG1=Low	-12		-10	dB
	AG0=Low, AG1=High	-4		-2	dB
	AG0=High, AG1=High	4		6	dB
Max Output Swing	THD < -20 dB MONITOR-$\overline{\text{MONITOR}}$	3.5			Vpp
MONSUM gain	$\frac{\text{MONITOR} - \overline{\text{MONITOR}}}{\text{MONSUM}}$	-2		0	dB
Max input at MONSUM				3.5	Vpp
MONITOR output offset	MONITOR-$\overline{\text{MONITOR}}$ AG0=Low, AG1=Low		5		mV
MONITOR output offset	MONITOR-$\overline{\text{MONITOR}}$ AG0=High, AG1=High		10		mV
MONSUM input impedance		8K			Ω

RELAY DRIVER OUTPUTS

Peak pull in current	-25 °C < T(ambient) < 85 °C at Vol=0.8 V	35			mA
Hold voltage	After hold timer has timed out	25%		40%	Vcc
Hold voltage delay	t=CHTIMER • 750K for 0.01 µF<CHTIMER<0.47 µF			±45	%

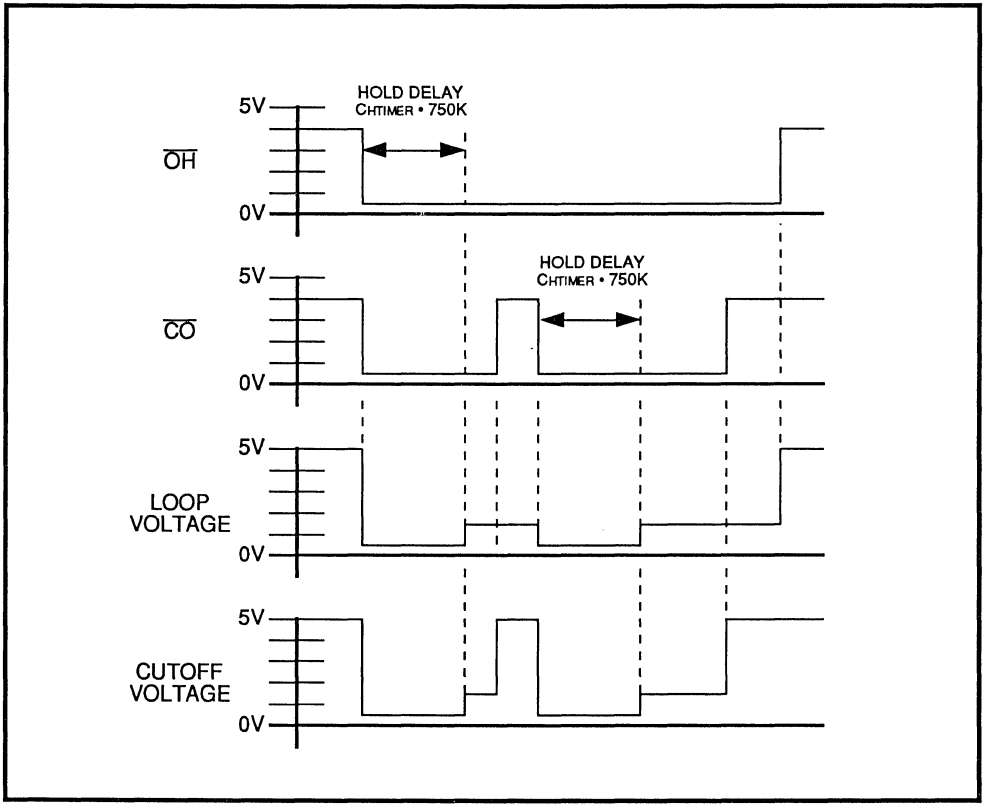


FIGURE 1: Relay Hold and Power Down Timing Diagrams

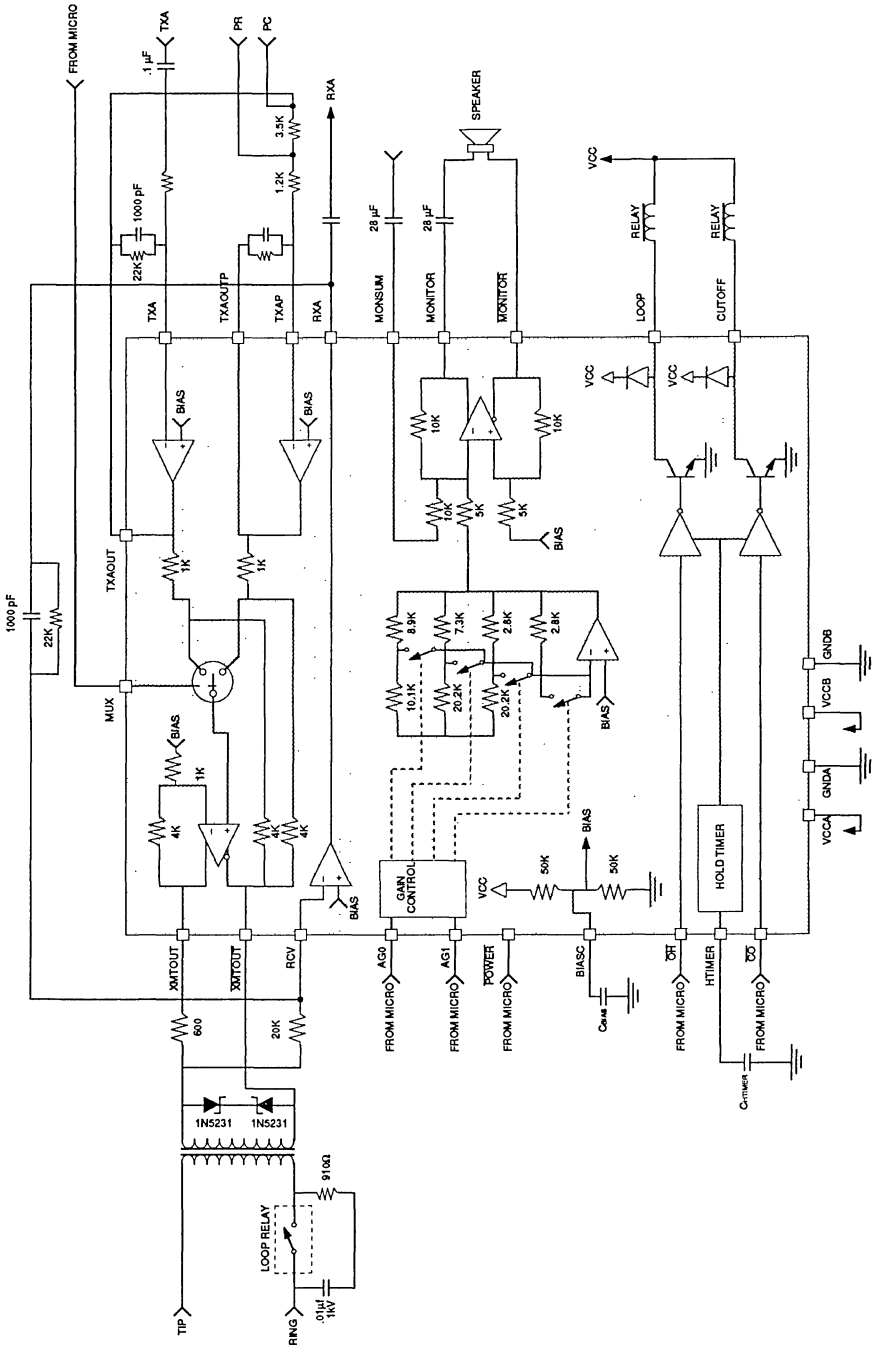
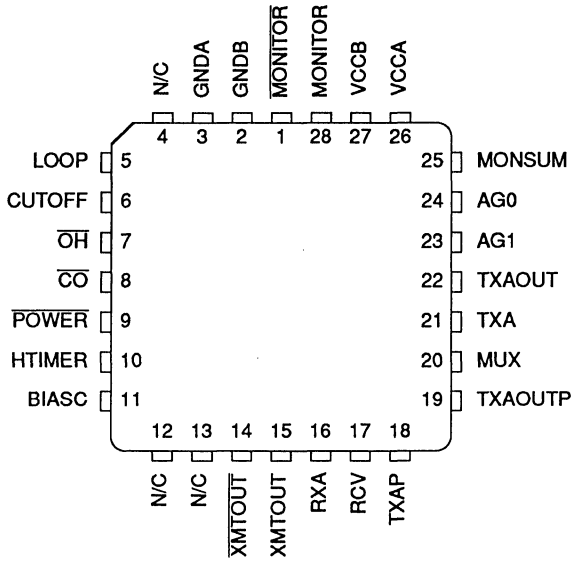


FIGURE 2: System Configuration

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73M376		
28-Pin PLCC	SSI 73M376-CH	73M376-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

SSI 73M450/450F
Universal Asynchronous Receiver/Transmitter

July, 1990

2

DESCRIPTION

The SSI 73M450 is a Universal Asynchronous Receiver/Transmitter (UART) circuit which is pin- and function-compatible with industry-standard 16C450-type UARTs. It is primarily used in the interface between the serial data port and the parallel peripheral bus in 8-bit microprocessor systems. The 73M450F is a fast version of the UART that does not require wait states for operation with newer, higher-speed processors. Both versions are designed in CMOS for low-power quiescent operation. The 73M450 and 73M450F require only a single 5-volt supply and are available in either a 40-pin DIP or 44-pin PLCC package.

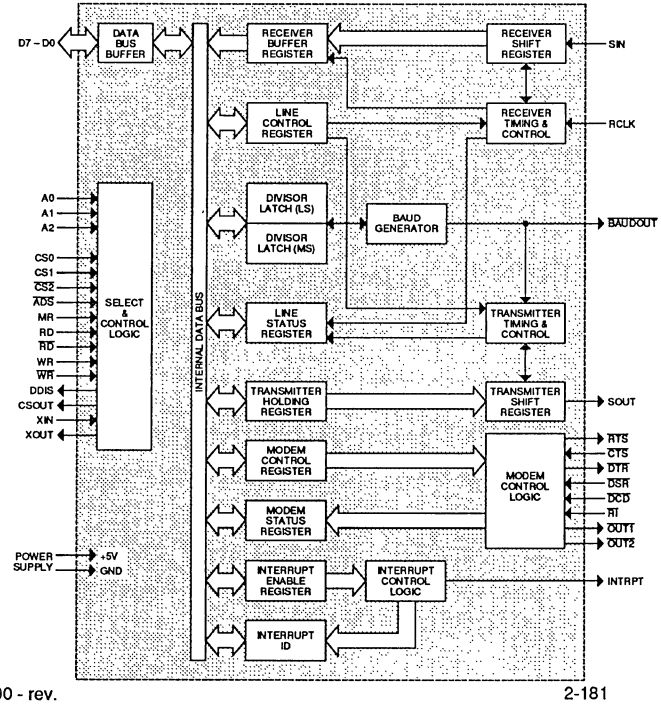
FEATURES

- **Compatible with industry-standard UARTs**
- **High-speed version for zero wait-state operation with higher-speed busses**

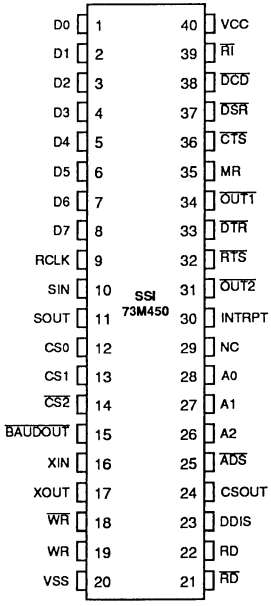
FEATURES (Continued)

- **Fully CMOS for low-power quiescent operation**
- **High drive current for directly driving large loads**
- **Full double buffering**
- **Independent control of transmit, receive, line status and data set interrupts**
- **Contains modem control function including $\overline{CTS}$, $\overline{TRS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{RI}$ and $\overline{DCD}$**
- **Programmable serial interface characteristics include:**
  - **5, 6, 7 or 8-bit characters**
  - **even, odd or no-parity bit generation and detection**
  - **1, 1 1/2 or 2 stop-bit generation**
  - **baud rate generation (dc to 56K baud)**
- **Full status reporting capabilities**
- **Available in 40-pin DIP or 44-pin PLCC**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

BUS INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{ADS}$	25	28	I	Address Strobe: The rising edge of this signal is used for latching the Register Address and Chip Select inputs, thus facilitating interface to a multiplexed Address/Data bus. If not required, $\overline{ADS}$ should be tied permanently low.
CS0, CS1, $\overline{CS2}$	12-14	14-16	I	Chip Select: The UART is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Chip selection is complete when the decoded chip select signal is latched with an active (low) $\overline{ADS}$ input. This enables communication between the UART and the CPU.
A0-2	28-26	31-29	I	Register Select Address: These pins determine which of the UART registers is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit in the UART's Line Control Register (see Table 1) also controls which register is referenced.
RD, $\overline{RD}$	22,21	25,24	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling RD high or $\overline{RD}$ low while the chip is selected. Since only one input is required for a read, tie either RD permanently low or $\overline{RD}$ permanently high if not used.
WR, $\overline{WR}$	19, 18,	21, 20	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling WR high or $\overline{WR}$ low while the chip is selected. Since only one input is required for a write, tie either WR permanently low or $\overline{WR}$ permanently high if not used.
D0-7	1-8	2-9	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data, control words and status information are transferred via this bus.
CSOUT	24	27	O	Chip Select Out: When high, indicates that the chip has been selected by active CS0, CS1 and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic "1." CSOUT goes low when the chip is deselected.
DDIS	23	26	O	Driver Disable: Goes low when the CPU is reading data from the UART. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and UART on the D0-D7 Data Bus) at all times, except when the CPU is reading data.

BUS INTERFACE (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
INTRPT	30	33	O	Interrupt: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

DATA I/O

NAME	DIP	PLCC	TYPE	DESCRIPTION
SIN	10	11	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	11	13	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{RTS}$	32	36	O	Request To Send: This output is programmed by bit 1 of the Modem Control Register and is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{CTS}$	36	40	I	Clear To Send: A modem status input whose condition corresponds to the complement of the CTS bit (bit 4) of the Modem Status Register. When $\overline{CTS}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{DTR}$	33	37	O	Data Terminal Ready: This output is programmed by bit 0 of the Modem Control Register, and is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{DSR}$	37	41	I	Data Set Ready: A modem status input whose condition corresponds to the complement of the DSR bit (bit 5) of the Modem Status Register. When $\overline{DSR}$ is low, it indicates that the modem is ready to establish communications.

MODEM CONTROL (Continued)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{DCD}$	38	42	I	Data Carrier Detect: A modem status input whose condition corresponds to the complement of the DCD bit (bit 7) of the Modem Status Register. When $\overline{DCD}$ is low, it indicates that the modem is receiving a carrier.
$\overline{RI}$	39	43	I	Ring Indicator: A modem status input whose condition corresponds to the complement of the RI bit (bit 6) of the Modem Status Register. When $\overline{RI}$ is low, it indicates that a telephone ringing signal is being received.
$\overline{OUT1}$ $\overline{OUT2}$	34 31	38 35	O O	Output 1, 2: User designated outputs that can be set to an active low by setting bit 2 ($\overline{OUT1}$) or bit 3 ($\overline{OUT2}$) of the Modem Control Register high. These output signals are set high upon Master Reset or during loop mode operation.

GENERAL & CLOCKS

NAME	DIP	PLCC	TYPE	DESCRIPTION
VCC	40	44	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to VSS.
VSS	20	22	I	System Ground.
MR	35	39	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$ and $\overline{DTR}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger.
XIN, XOUT	16,17	18,19	I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source.
RCLK	9	10	I	Receiver Clock: This input is the 16X baud rate clock for the receiver section of the chip.
$\overline{BAUDOUT}$	15	17	O	Baud Generator Output: 16X clock signal for the transmitter section of the UART, equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. May also be used for the receiver section by tying this output to the RCLK input of the chip.
NC	29	1,12 23, 34	-	No Connection: These pins have no internal connection and may be left floating.

TABLE 1: Control Register Address Table

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	Modem Control
X	1	0	1	Line Status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

TABLE 2: UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1 & 2 are low; bits 3-7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High

CONTROL REGISTER OVERVIEW

REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER							
			D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB = 0	0	0	0	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB = X	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	011 DLAB = X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB = X	0	0	0	LOOP	OUT2	OUT1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB = X	0	TRANSMIT-TER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB = X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB = X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

BIT	NAME	COND.	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Interrupt when set to logic 1.
D4 - D7	Not Used	0	These three bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND.	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	N/A
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND.		DESCRIPTION
D0	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND.		DESCRIPTION
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		This is the Break Control bit. When set to a logic 1, the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit 6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - UA0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers.

BIT	NAME	COND.	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	OUT1	1	This bit controls the Output 1 ($\overline{OUT1}$) signal, which is an auxiliary user-designated output. When bit 2 is set to a logic 1, the $\overline{OUT1}$ output is forced to a logic 0. When bit 2 is reset to a logic 0, the $\overline{OUT1}$ output is forced to a logic 1.
D3	OUT2	0	This bit controls the Output 2 ($\overline{OUT2}$) signal, which is an auxiliary user-designated output. When bit 3 is set to a logic 1, the $\overline{OUT2}$ output is forced to a logic 0. When bit 3 is reset to a logic 0, $\overline{OUT2}$ output is forced to a logic 1.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected; the four Modem Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four Modem Control inputs, and the Modem Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D7		0	These bits are permanently set to logic 0.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits 1-4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND.	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading the data in the Receiver Buffer Register.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Regsiter into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character.
D7	-	0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition, four bits provide change information. Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register respectively.

BIT	NAME	COND.	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit indicates that the $\overline{RI}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 4 MHz) and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)/(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

Note: The maximum operating frequency of the Baud Generator is 4 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56K Baud.

TABLE 3: Baud Rates Using 1.8432 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 4: Baud Rates Using 3.072 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

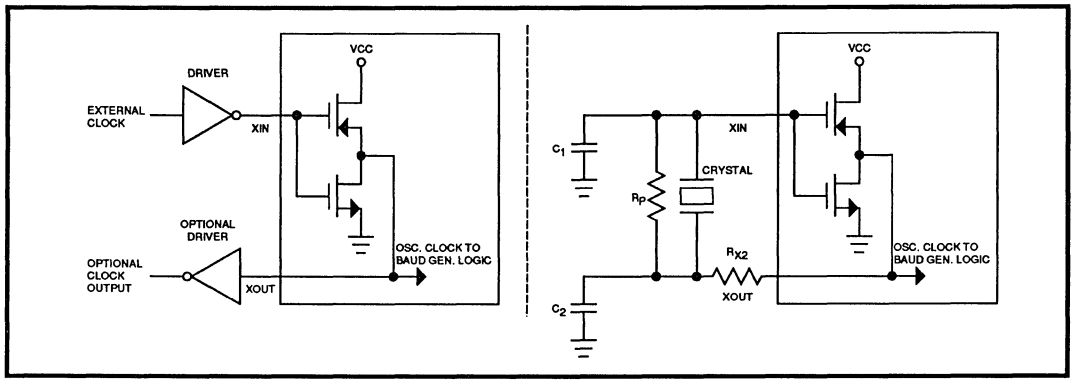


FIGURE 1: Typical Clock Circuits

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
1.8 - 3.1 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF

ABSOLUTE MAXIMUM RATINGS

(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+14V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to Vcc + 0.3

DC CHARACTERISTICS
(TA = –40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		Vcc	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = 5.0 mA on all outputs except XOUT	2.4			V
ICC	Average Power Supply	See Note 1		5	10	mA
	Current	See Note 2			50	µA
IIL	Input Leakage	VCC=5.25V, VSS=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 KHz.
Note 2: VCC = 5.5V, TA = –40°C; No output load; CMOS-level inputs, XIN = Vcc

CAPACITANCE
(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2	Clock Input Capacitance			15	20	pF
CXTAL1	Clock Output Capacitance			20	30	pF
CI	Input Capacitance			6	10	pF
CO	Output Capacitance			10	20	pF

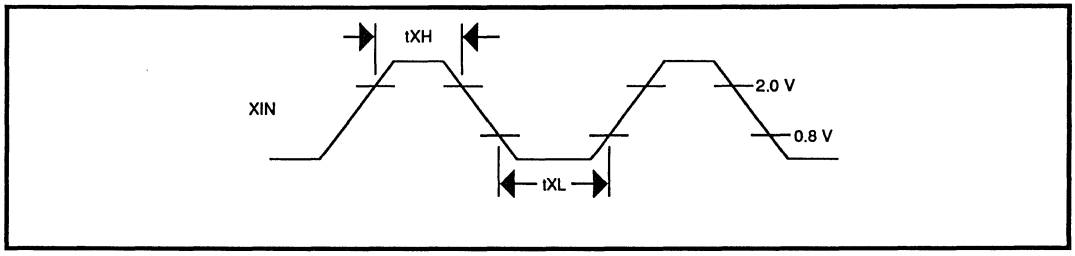
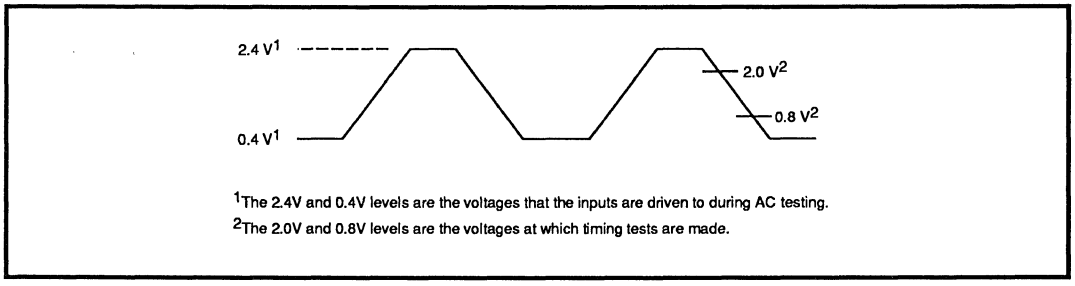


FIGURE 2: External Clock Input* (4 MHz Maximum)



[1]The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
[2]The 2.0V and 0.8V levels are the voltages at which timing tests are made.

FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5.)

PARAMETER		CONDITIONS	73M450		73M450F		UNITS
			MIN	MAX	MIN	MAX	
tADS	Address Strobe Width		60		50		ns
tAS	Address Setup Time		60		30		ns
tAH	Address Hold Time		0		0		ns
tCS	Chip Select Setup Time		60		30		ns
tCH	Chip Select Hold Time		0		0		ns
tCSC	Chip Select Output Delay from Select	100 pF load See Note 3		100		80	ns
tCSR	RD, $\overline{RD}$ Delay from Chip Select	See Note 3	50		30		ns
tAR	RD, $\overline{RD}$ Delay from Address	See Note 3	60		30		ns

READ & WRITE CYCLE (Continued)

PARAMETER		CONDITIONS	73M450		73M450F		UNITS
			MIN	MAX	MIN	MAX	
tRD	RD, $\overline{RD}$ Strobe Width		125		80		ns
tRC	Read Cycle Delay		175		50		ns
tAD	Address to Read Data	73M450F only		NA		160	ns
RC	Read Cycle	See Note 1	360		210		ns
tRDD	RD, $\overline{RD}$ to Driver Disable Delay	100 pF load See Note 2		60		50	ns
tRVD	Delay from RD, $\overline{RD}$ to Data	100 pF load		125		80	ns
tHZ	RD, $\overline{RD}$ to Floating Data Delay	100 pF load See Note 2	0	100	0	60	ns
tRA	Address Hold Time from RD, $\overline{RD}$	See Note 3	20		20		ns
tRCS	Chip Select Hold Time from RD, $\overline{RD}$	See Note 3	20		20		ns
tCSW	WR, $\overline{WR}$ Delay from Select	See Note 3	50		30		ns
tAW	WR, $\overline{WR}$ Delay from Address	See Note 3	60		30		ns
tWR	WR, $\overline{WR}$ Strobe Width		100		80		ns
tWC	Write Cycle Delay		200		50		ns
WC	Write Cycle=tAW+tWR+tWC		360		160		ns
tDS	Data Setup Time		40		30		ns
tDH	Data Hold Time		40		30		ns
tWA	Address Hold Time from WR, $\overline{WR}$	See Note 3	20		20		ns
tWCS	Chip Select Hold time from WR, $\overline{WR}$	See Note 3	20		20		ns
tMRW	Master Reset Pulse Width		5		1		µs
tXH	Duration of Clock High Pulse	External Clock (4 MHz max.)	100		100		ns
tXL	Duration of Clock Low Pulse	External Clock (4 MHz max.)	100		100		ns

Note 1: RC = tAR + tRD + tRC for 73M450
RC = tAD + tRC for 73M450F
Note 2: Charge and discharge time is determined by VOL, VOH and the external loading.
Note 3: Applicable only when $\overline{ADS}$ is tied low.

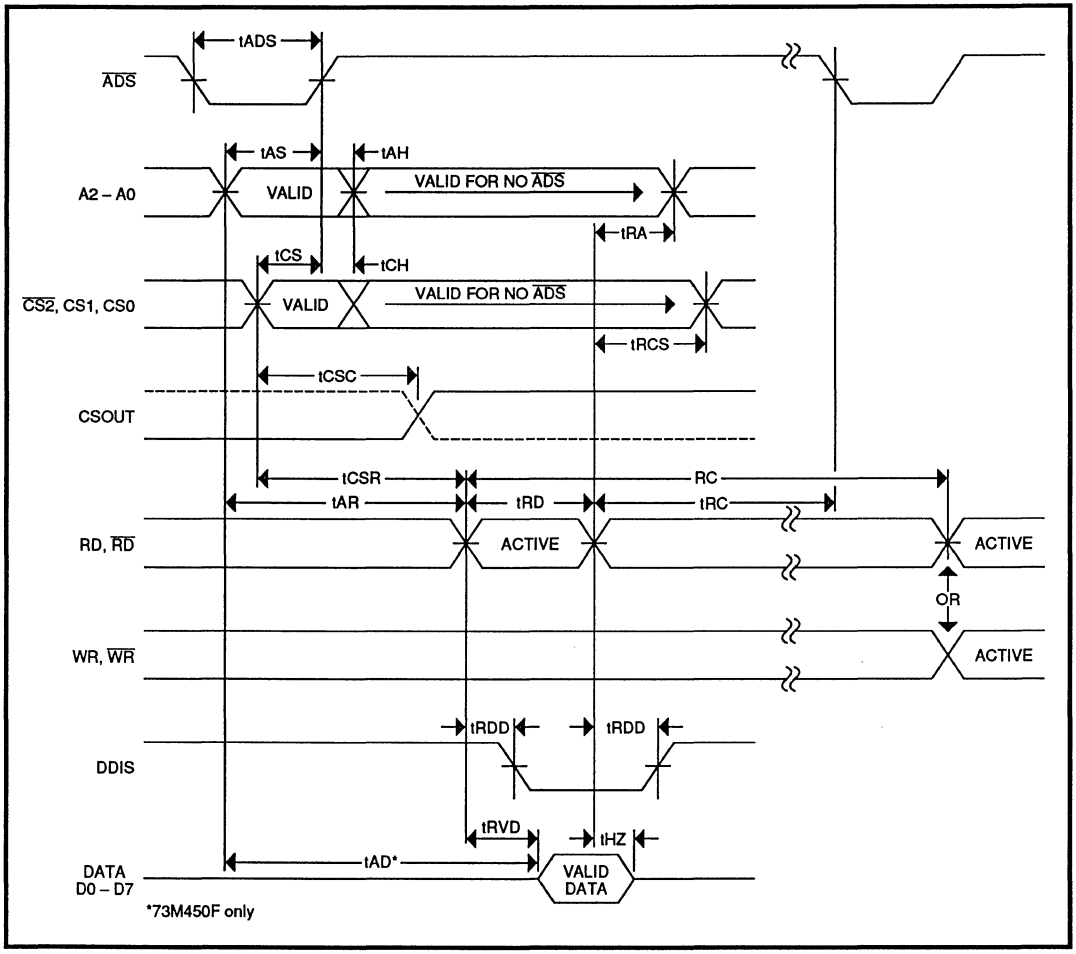


FIGURE 4: Read Cycle Timing

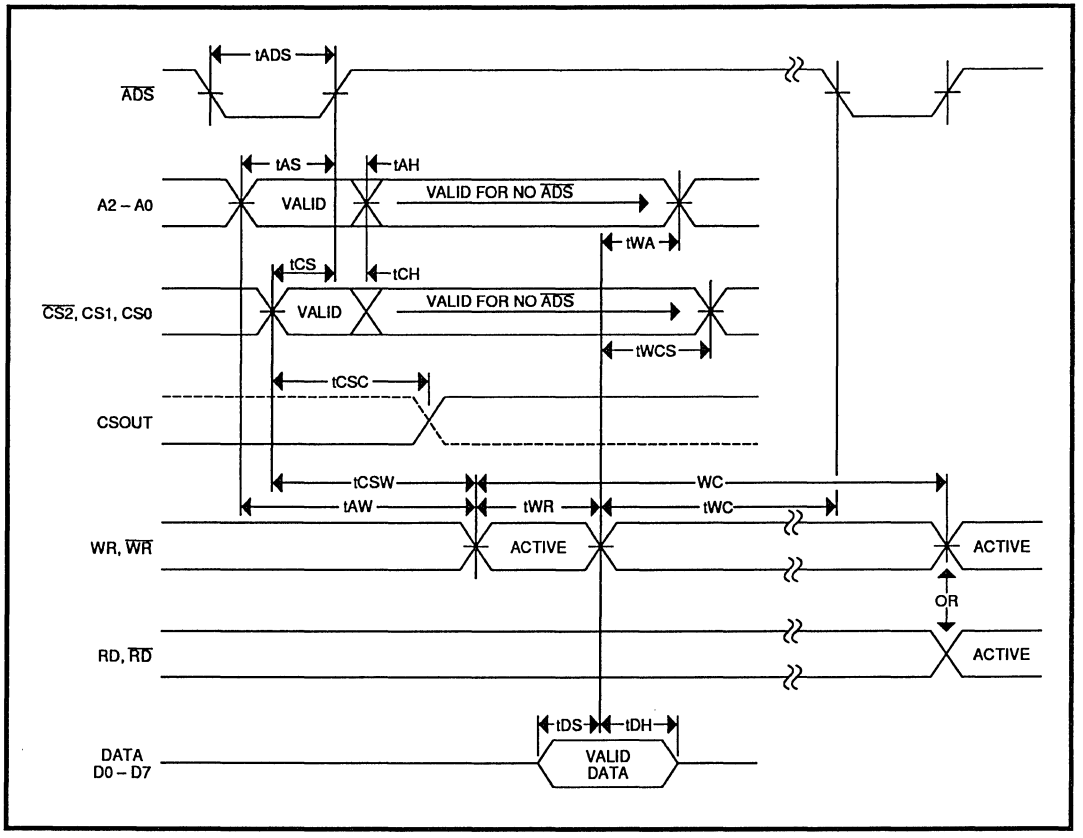


FIGURE 5: Write Cycle Timing

AC CHARACTERISTICS (Continued)

TRANSMITTER (Refer to Figure 6.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from rising edge of WR, $\overline{WR}$ (WR THR)to Reset Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		24	40	BAUDOUT cycles
tSI	Delay from Initial Write to Interrupt		16	32	BAUDOUT cycles
tSTI	Delay from Stop to Interrupt (THRE)		8	8	BAUDOUT cycles
tIR	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF load		250	ns

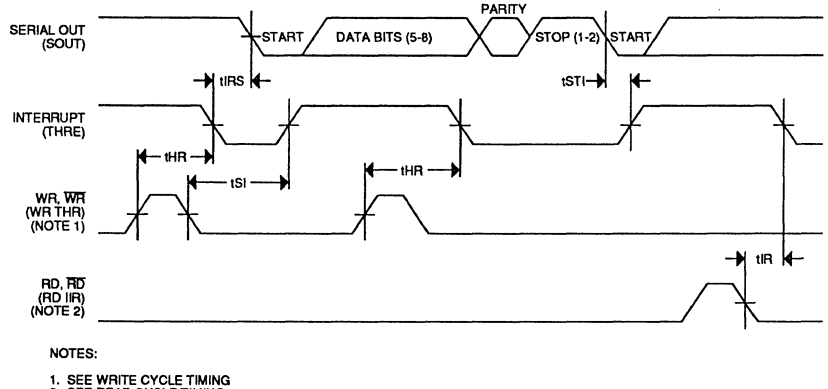


FIGURE 6: Transmitter Timing

AC CHARACTERISTICS (Continued)

MODEM CONTROL (Refer to Figure 7.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from WR, $\overline{WR}$ (WR MCR) to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Reset Interrupt from RD, $\overline{RD}$ (RS MSR)	100 pF load		250	ns

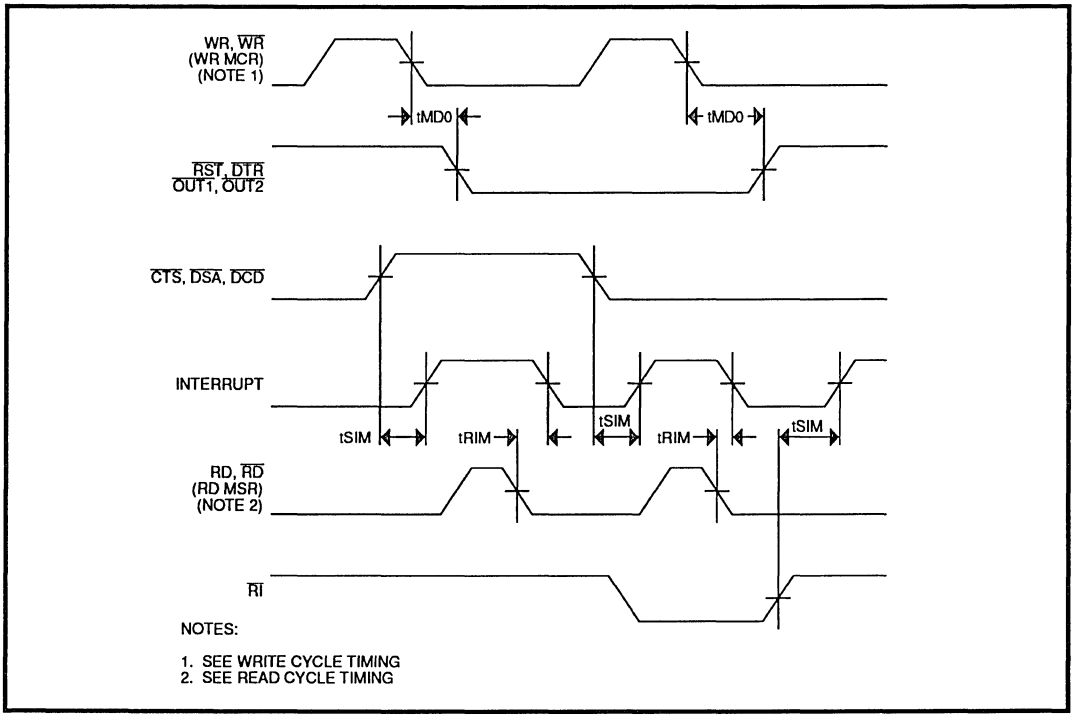


FIGURE 7: Modem Controls Timing

AC CHARACTERISTICS (Continued)

BAUD GENERATOR (Refer to Figure 8.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
N	Baud Divisor		1	2^{16}-1	
tBLD	Baud Output Negative Edge Delay	100 pF load		125	ns
tBHD	Baud Output Positive Edge Delay	100 pF load		125	ns
tLW	Baud Output Down Time	fX=2 MHz, div. by 2, 100 pF load	425		ns
tHW	Baud Output Up Time	fX=3 MHz, div. by 3, 100 pF load	250		ns

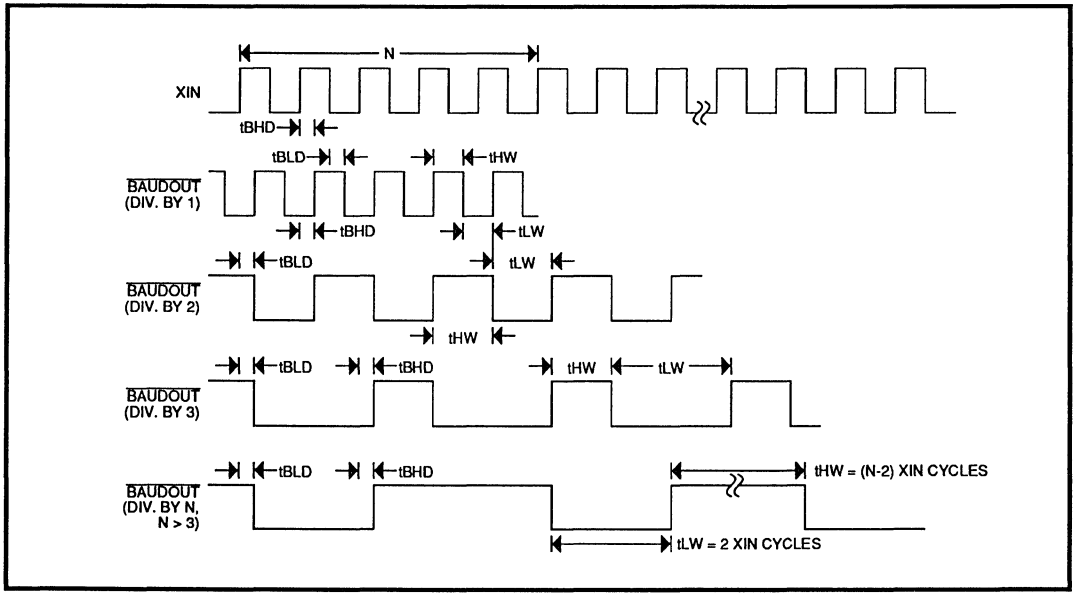


FIGURE 8: $\overline{\text{BAUDOUT}}$ Timing

AC CHARACTERISTICS (Continued)

RECEIVER (Refer to Figure 9.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt	RCLK=tXH & tXL		1	RCLK cycles
tRINT	Delay from RD, $\overline{RD}$ (RD RBR/RDLSR) to Reset Interrupt	100 pF load		1	µs

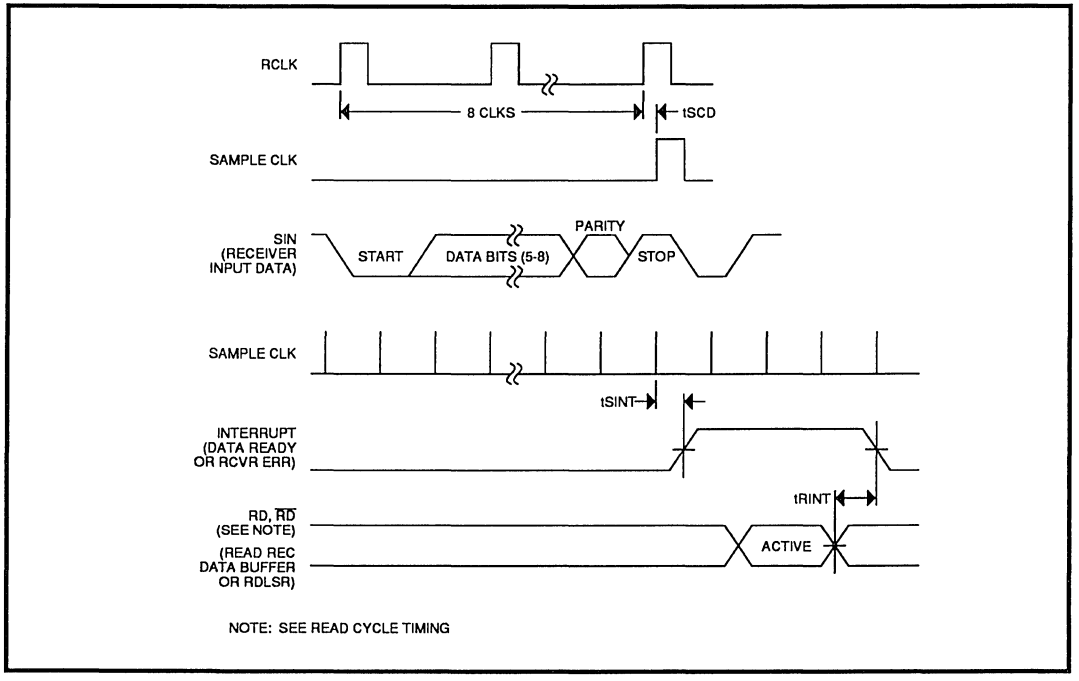


FIGURE 9: Receiver Timing

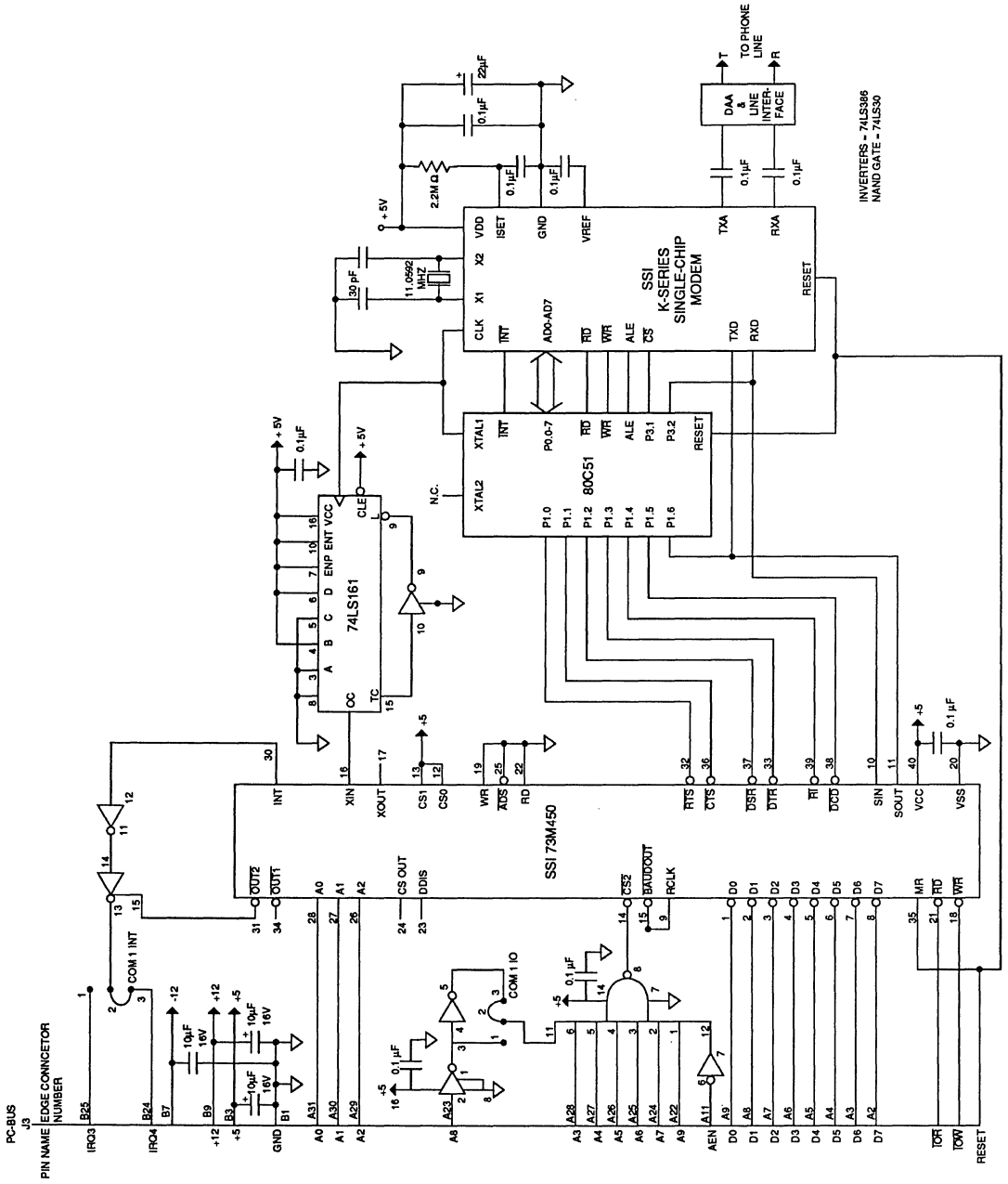
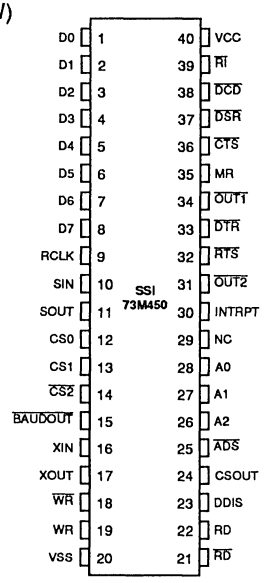


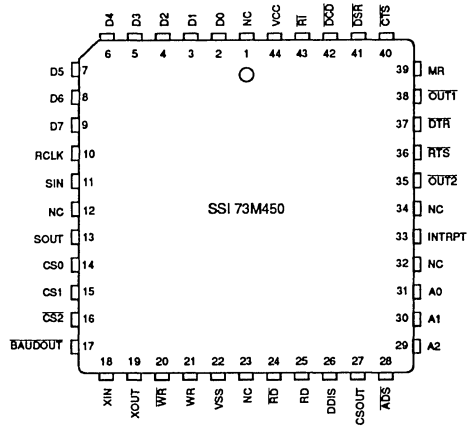
FIGURE 10: Typical Application showing Modem Interface to PC-Bus via SSI 73M450 UART

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



40 - Pin DIP



44 - Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 73M450	40-pin PDIP	SSI 73M450-IP	73M450-IP
	44-pin PLCC	SSI 73M450-IH	73M450-IH
SSI 73M450F	40-pin PDIP	SSI 73M450F-IP	73M450F-IP
	44-pin PLCC	SSI 73M450F-IH	73M450F-IH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

Notes:

SSI 73M450L/450LF
Universal Asynchronous Receiver/Transmitter

June, 1989

2

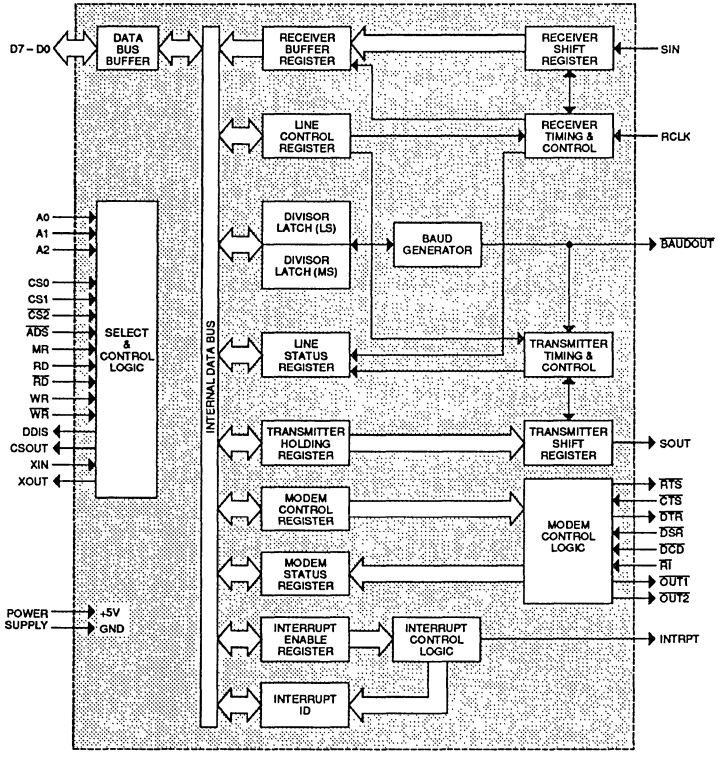
DESCRIPTION

The SSI 73M450L is an enhanced version of the SSI 73M450 Universal Asynchronous Receiver/ Transmitter (UART). The enhancement allows the chip to be placed into low-power operation by shutting off the crystal oscillator. The SSI 73M450LF is a fast version of the chip. Both versions require a single 5V supply, and are available in 40-pin DIP and 44-pin PLCC.

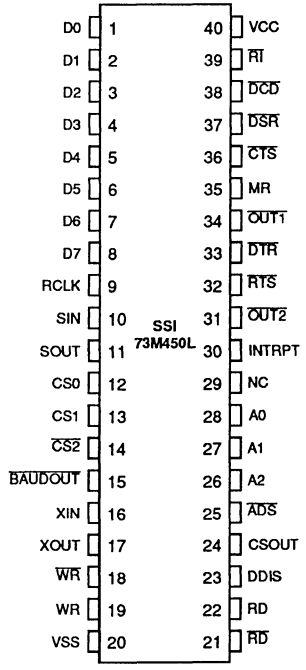
FEATURES

- **Pin and register compatible with the SSI 73M450/450F**
- **Bit programmable oscillator disable provides a shut-down mode while retaining memory**
- **High drive current for directly driving large loads**
- **Available in 40-pin DIP and 44-pin PLCC**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CONTROL REGISTER OVERVIEW

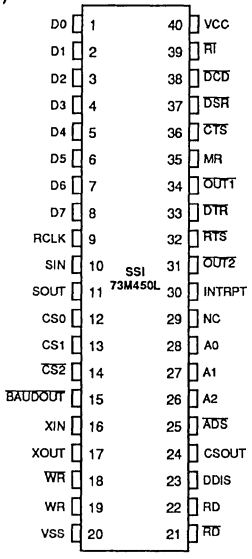
REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB = 0	0	0	SSI MODE	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB = X	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	011 DLAB = X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB = X	OSC OFF	0	0	LOOP	OUT2	OUT1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DR)
LINE STATUS REGISTER	LSR	101 DLAB = X	0	TRANSMIT-TER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY (THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB = X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB = X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

POWER SHUT-DOWN OPERATION

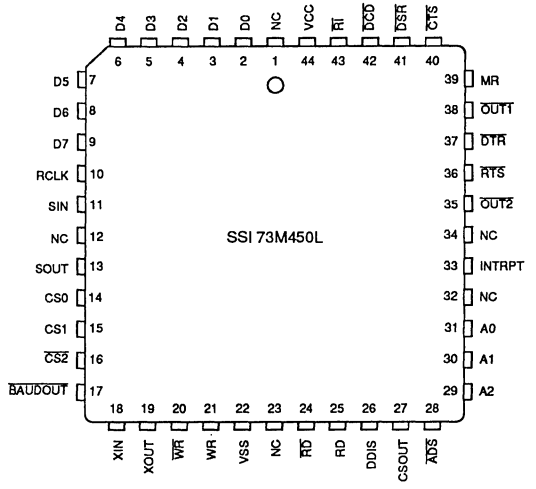
The oscillator of the SSI 73M450L/450LF is placed into power shut-down by setting bits D5 of the Interrupt Enable Register (IER) and D7 of the Modem Control Register (MCR) to a "1." During shut-down, the contents of all registers are retained. Resetting bit D7 of the MCR returns the chip to normal operation.

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



40 - Pin DIP



44 - Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 73M450L	40-pin PDIP	SSI 73M450L-IP	73M450L-IP
	44-pin PLCC	SSI 73M450L-IH	73M450L-IH
SSI 73M450LF	40-pin PDIP	SSI 73M450LF-IP	73M450LF-IP
	44-pin PLCC	SSI 73M450LF-IH	73M450LF-IH

Notes:

SSI 73M550
SSI 73M1550/2550
UART with FIFOs

August, 1990

2

DESCRIPTION

The SSI 73M550 is a Universal Asynchronous Receiver/Transmitter (UART) with receive and transmit FIFO buffers. The 16-byte FIFO registers are active during the FIFO mode, allowing the UART to reduce CPU overhead and accomodate Direct Memory Access (DMA) transfers. This mode is supported by interrupt functions and selectable interrupt trigger levels in both the RCVR and TXMR FIFO.

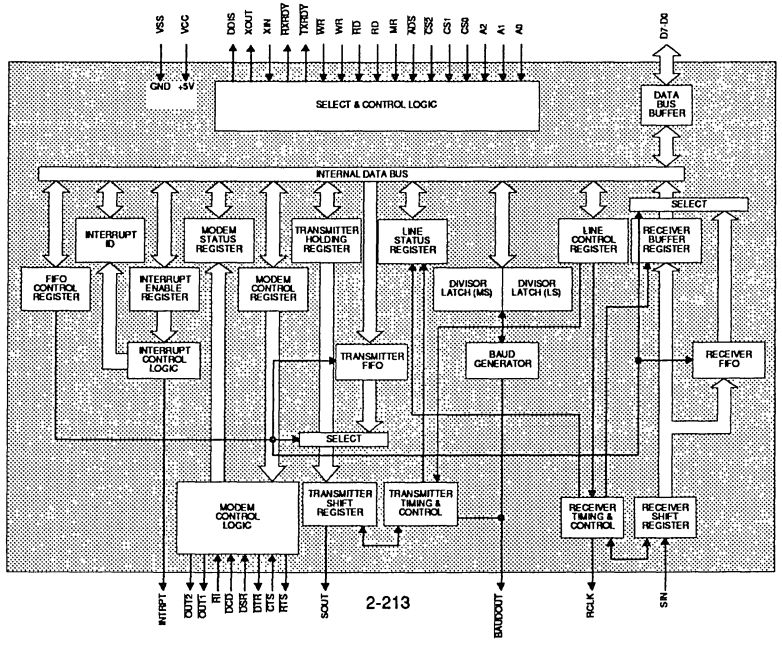
The 73M550 is functionally identical to the SSI 73M450 in the CHARACTER mode. Pins 24 (CSOUT) and 29 (NC) of the 73M450 have been replaced by $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$, respectively, on the 73M550. The chip is automatically put into the CHARACTER mode upon power-up, and subsequent mode changes are accomplished via software control.

The 73M1550 and 73M2550 are 28-pin versions of the 73M550. The difference between these versions is that 73M2550 adds a µPRST pin at the expense of the XOUT pin. See Figure 17 on page 32 for detail. All versions are available in DIP or PLCC and require a single 5V supply.

FEATURES

- **16 bytes of receive and transmit FIFO buffering available in FIFO mode reduces CPU overhead**
- **Supports DMA transfers with $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ pins**
- **Backwards-compatible with the 73M450 in CHARACTER mode**
- **Oscillator disable allows a static low-power state**
- **Bit-programmable high impedance state of INTRPT pin**
- **High drive current for directly driving large loads**
- **Full double buffering**
- **Independent control transmit, receive, line status and data set interrupts**
- **Contains modem control functions including $\overline{\text{CTS}}$, $\overline{\text{TRS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$ and $\overline{\text{DCD}}$**
- **Full status reporting capabilities**
- **Available in 40-pin DIP, 44-pin PLCC, 28-pin DIP and PLCC**
- **CMOS design for low-power operation**

BLOCK DIAGRAM



PIN DESCRIPTION

BUS INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{ADS}$	I	Address Strobe: The rising edge of this signal is used for latching the Register Address and Chip Select inputs, thus facilitating interface to a multiplexed Address/Data bus. $\overline{ADS}$ is also required when register address signals (A2, A1, A0) are not stable for the duration of the read or write cycle. If not required, $\overline{ADS}$ should be tied permanently low.
CS0, CS1, $\overline{CS2}$	I	Chip Select: The UART is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Chip selection is complete when the decoded chip select signal is latched with the rising edge of an active (low) $\overline{ADS}$ input. This enables communication between the UART and the CPU. If $\overline{ADS}$ is permanently low, then chip select should be stabilized for the duration of the tCSW parameter.
A0-A2	I	Register Select Address: These pins determine which of the UART registers is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit in the UART's Line Control Register (see Table 1) also controls which register is referenced.
RD, $\overline{RD}$	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling RD high or $\overline{RD}$ low while the chip is selected. Since only one input is required for a read, tie either RD permanently low or $\overline{RD}$ permanently high if not used.
WR, $\overline{WR}$	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling WR high or $\overline{WR}$ low while the chip is selected. Since only one input is required for a write, tie either WR permanently low or $\overline{WR}$ permanently high if not used.
D0-D7	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data control words and status information are transferred via this bus.
$\overline{TXRDY}$	I/O	Transmitter Ready Signal for DMA Transfer: Remains low as long as XMIT FIFO is not completely full. In FIFO mode, DMA transfer modes 0 and 1 are allowed. In the character mode, only DMA transfer mode 0 is allowed. DMA mode 0 supports single DMA transfer mode between CPU bus cycles. DMA mode 1 supports multiple DMA transfers until the XMIT FIFO has been filled.
$\overline{RXRDY}$	O	Receiver Ready Signal for DMA Transfer: Remains low until RCVR FIFO has been emptied. In FIFO mode DMA transfer modes 0 and 1 are allowed. In the character mode only DMA mode 0 is allowed. DMA mode 0 supports single DMA transfer made between CPU bus cycles. DMA mode 1 supports multiple DMA transfers until the RCVR FIFO has been emptied.
DDIS	O	Driver Disable: Goes low when the CPU is reading data from the UART. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and UART on the D0-D7 Data Bus) at all times, except when the CPU is reading data.

BUS INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
INTRPT	O	Interrupt: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag, Received Data Available; Timeout (FIFO mode only); Transmitter Holding Register Empty and Modem Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

DATA I/O

NAME	TYPE	DESCRIPTION
SIN	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

NAME	TYPE	DESCRIPTION
$\overline{RTS}$	O	Request To Send: This output is programmed by $\overline{RTS}$ bit (D1) of the Modem Control Register and represents the compliment of that bit. I is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{CTS}$	I	Clear To Send: A modem status input whose condition corresponds to the complement of the CTS bit (D4) of the Modem Status Register. When $\overline{CTS}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{DTR}$	O	Data Terminal Ready: This output is programmed by DTR bit (D0) of the Modem Control Register, and represents the compliment of that bit. It is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{DSR}$	I	Data Set Ready: A modem status input whose condition is complimented and reflected in the DSR bit (D5) of the Modem Status Register. When $\overline{DSR}$ is low, it indicates that the modem is ready to establish communications.
$\overline{DCD}$	I	Data Carrier Detect: A modem status input whose condition is complemented and reflected in the DCD bit (D7) of the Modem Status Register. When $\overline{DCD}$ is low, it indicates that the modem is receiving a carrier.
$\overline{RI}$	I	Ring Indicator: A modem status input whose condition is complimented and reflected in the RI bit (D6) of the Modem Status Register. When $\overline{RI}$ is low, it indicates that a telephone ringing signal is being received.
$\overline{OUT1}$ $\overline{OUT2}$	O O	Output 1, 2: User designated outputs that can be set to an active low by setting bit 2 ($\overline{OUT1}$) or bit 3 ($\overline{OUT2}$) of the Modem Control Register high. These output signals are set high upon Master Reset or during loop mode operation.

GENERAL & CLOCKS

NAME	TYPE	DESCRIPTION
VCC	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to VSS.
VSS	I	System Ground
MR	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$ and $\overline{DTR}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger. See Table 2.
XIN, XOUT	I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source.
RCLK	I	Receiver Clock: This input is the 16X baud rate clock for the receiver section of the chip.
$\overline{BAUDOUT}$	O	Baud Generator Output: 16X clock signal for the transmitter section of the UART. The clock is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. May also be used for the receiver section by tying this output to the RCLK input of the chip.
N/C	-	No Connection: These pins have no internal connection and may be left floating.

28-PIN VERSION, SPECIAL PINS

NAME	I/O	DESCRIPTION
INTRPT	O	Interrupt: In the 28-pin versions of this chip, the INTRPT pin can be forced into a high impedance state by resetting to 0 the OUT2 bit (D3) of the Modem Control Register. INTRPT pin operation is enabled by setting the OUT2 bit to 1.
XIN, XOUT	I/O	External System Clock: The XOUT pin is not available on the 73M2550 and therefore must be driven by an external clock connected to the XIN pin.
µPRST	O	Microprocessor Reset: This output signal is used to provide a hardware reset to a local controller. This pin becomes active high when the MR pin is pulled high or the OUT1 bit (D2) of the Modem Control Register is set to 1. The µPRST function is available only on the 73M2550.

TABLE 1: Control Register Address Table

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control
X	1	0	0	Modem Control
X	1	0	1	Line Status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

TABLE 2: UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 & 5 forced and 4, 6 & 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1, 2, 3, 6 & 7 are low; bits 4 & 5 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low (bits 5, 6 & 7 permanent)
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High
FIFO Control Register	Master Reset	All bits low
RCVR FIFO	MR/FCR1 and FCR0/ΔFCR0	All bits low
XMIT FIFO	MR/FCR2 and FCR0/ΔFCR0	All bits low

CONTROL REGISTER OVERVIEW

REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB=0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB=0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB=0	0	0	ENABLE SSI MODE (NOTE 1)	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB=X	FIFOs ENABLED (NOTE 1)	FIFOs ENABLED (NOTE 1)	SSI MODE RXRDY FOR DMA	SSI MODE TXRDY FOR DMA	INTERRUPT ID BIT 2 (NOTE 1)	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
FIFO CONTROL REGISTER (WRITE ONLY)	FCR	010 DLAB=X	RCVR TRIGGER (MSB)	RCVR TRIGGER (LSB)	SSI MODE XMIT TRIGGER (MSB)	SSI MODE XMIT TRIGGER (LSB)	DMA MODE SELECT	XMIT FIFO RESET	RCVR FIFO RESET	FIFO ENABLE
LINE CONTROL REGISTER	LCR	001 DLAB=X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB=X	SSI MODE OSC OFF	0	0	LOOP	OUT 2	OUT 1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB=X	ERROR IN RCVR FIFO (NOTE 1)	TRANS-MITTER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB=X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB=X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLL	000 DLAB=1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB=1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

NOTE 1: THESE BITS ARE RESET TO 0 IN THE 73M450 MODE (Character Mode)

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the five types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

The chip's SSi mode can be activated by setting bit D5. Once in the SSi mode, the chip can be placed in a power shut-down state by setting bit D7 in the Modem Control Register.

BIT	NAME	COND	DESCRIPTION
D0	Received Data	1	When set to logic 1 this bit enables the Received Data Available Interrupt, and timeout interrupts in FIFO mode.
D1	Transmitter Holding Register Empty	1	When set to logic 1 this bit enables the Transmitter Holding Register Empty Interrupt.
D2	Receiver Line Status Interrupt	1	When set to logic 1 this bit enables the Receiver Line Status Interrupt.
D3	Modem Status	1	When set to logic 1 this bit enables the Modem Status Interrupt.
D4	Not Used	0	This bit are is always logic 0.
D5	SSI Mode	1	When set to logic 1, this bit enables the SSi Mode. In the SSi Mode the oscillator can be turned off via bit D7 in the Modem Control Register, and the XMIT THRE interrupt trigger set via bits D4 & D5 of the FIFO Control Register.
D6-D7	Not used	0	These two bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions and also allows for DMA transfer operations in a polled FIFO manner under the SSi mode. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a prioritized interrupt or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2 D3	Interrupt ID bits 0, 1, 2	See table Page 10	These three bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table. Bit D3 is reset to 0 when FIFO mode is disabled.
D4	SSI mode TXRDY for DMA	1	This bit function is available only when SSi mode is enabled (bit D5 in IER is set). This bit is the compliment of $\overline{\text{TXRDY}}$ pin and is used to support DMA transfers in a polled environment. A logic 1 indicates transmitter is less than full and is ready for DMA transfer.
		0	A logic 0 indicates transmitter is full and not ready for DMA transfer. Also when SSI mode is disabled this bit will be reset to 0.
D5	SSI mode RXRDY for DMA	1	This bit function is available only when SSi mode is enabled (bit D5 in IER is set). This bit is the compliment of $\overline{\text{RXRDY}}$ pin and is used to support DMA transfers in a polled environment. A logic 1 indicates receiver is not empty and is ready for DMA transfer.
		0	A logic 0 indicates receiver is empty and not ready for DMA transfer. Also when SSi mode is disabled this bit will be reset to 0.
D6, D7	FIFOs enabled	1	These two bits are set to logic 1 when bit D0 in FCR is set to 1 (FIFO mode enabled).
		0	These two bits are reset to logic 0 when bit D0 in FCR is reset to 0 (FIFO mode disabled).

INTERRUPT PRIORITY TABLE

D3	D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	0	1	–	None	None	N/A
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Receive Data Available	Receive Data Available or RCVR FIFO trigger level reached	Reading the Receiver Buffer Register or the RCVR FIFO drops below trigger level
1	1	0	0	Second	Character Timeout Indicator	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time	Reading the Receiver Buffer Register
00	1	0	Third	Transmit Holding	Transmit Holding Register Register Empty	Empty or below XMIT FIFO trigger level	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register or XMIT FIFO trigger level reached
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the Modem Status Register

FIFO CONTROL REGISTER (FCR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 010

This is a write only register at the same location as the IIR read only Register. This register is used to enable the FIFOs, clear the FIFOs, set the XMIT and RCVR FIFO trigger level, and select the type of DMA signalling.

BIT	NAME	COND	DESCRIPTION
D0	FIFO Enable	1	Setting this bit to logic 1 enables both XMIT and RCVR FIFOs. This bit must be written as 1 when other FCR bits are written to or they will not be programmed.
		0	Resetting this bit to logic 0 disables the FIFO mode (enables the 73M450 mode) and clears data in both FIFOs when changing from FIFO mode to 73M450 mode and vice versa, data is automatically cleared from FIFOs.
D1	RCVR FIFO Reset	1	Setting this bit to logic 1 clears all data in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The logic 1 written into this bit is self clearing.
D2	XMIT FIFO Reset	1	Setting this bit to logic 1 clears all data in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The logic 1 written into this bit is self clearing.

FIFO CONTROL REGISTER (FCR) (WRITE ONLY) (Continued)

BIT	NAME	COND	DESCRIPTION
D3	DMA Mode Select	1	Setting this bit to logic 1 will enable DMA mode 1. In this mode pins $\overline{TXRDY}$ and $\overline{RXRDY}$ and bits D4 and D5 in IIR, support multiple DMA transfers.
		0	Resetting this bit to logic 0 will enable DMA mode 0. In this mode, pins $\overline{TXRDY}$ and $\overline{RXRDY}$ and bits D4 and D5 in IIR support single DMA transfers.
D5, D4	SSI Mode XMIT Trigger (MSB, LSB)	0/1	These two bits are active in the SSi mode only. The value written into D5 and D4 determine the XMIT FIFO trigger level as described in table below. The THRE interrupt will occur if the XMIT FIFO is below the trigger level and will reset when the XMIT FIFO is filled to trigger level.
D7, D6	RCVR Trigger (MSB, LSB)	0/1	The value written into D7 and D6 determining the RCVR FIFO trigger level as described in table below. The received data available interrupt will occur if the RCVR FIFO is filled to or above the trigger level and will reset when the RCVR FIFO drops below the trigger level.

D5	D4	XMIT FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

D7	D6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND		DESCRIPTION
D0/D1	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit D2 is a logic 0, one stop bit is generated in the transmitted data. If bit D2 is a logic 1 when a 5-bit word length is selected via bits D0 and D1, one-and-a-half stop bits are generated. If bit D2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit D3 is a logic 1 and bit D4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit D3 is a logic 1 and bit D4 is a logic 1 an even number of logic 1's is transmitted or checked.
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit D3 is a logic 1 and bit D5 is a logic 1 the parity bit is transmitted and checked by the receiver as a logic 0 if bit D4 is a logic 1 or as a logic 1 if bit D4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND	DESCRIPTION
D6	Set Break	1	This is the Break Control bit. It causes a break condition to be sent to the receiving UART. When set to a logic 1 the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit D6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1	The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - A0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device.

BIT	NAME	COND	DESCRIPTION
D0	DTR	0/1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1 the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0 the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	0/1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1 the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0 the $\overline{RTS}$ output is forced to a logic 1.
D2	OUT1	0/1	This bit controls the Output 1 ($\overline{OUT1}$) signal, an auxiliary user-designated output. When bit D2 is set to a logic 1, $\overline{OUT1}$ is forced to a logic 0. When bit D2 is reset to a logic 0, $\overline{OUT1}$ is forced to a logic 1. On the SSI 73M2550 only, this bit controls the µPRST output. When bit D2 is set to a logic 1, the µPRST output is forced to a logic 1. When bit D2 is reset to logic 0, µPRST is forced to logic 0.
D3	OUT2	0/1	This bit controls the Output 2 ($\overline{OUT2}$) signal, an auxiliary user-designated output. When bit D3 is set to a logic 1, $\overline{OUT2}$ forced to a logic 0. When bit D3 is reset to a logic 0, $\overline{OUT2}$ output is forced to a logic 1. On the 28-pin versions, this bit controls the INTRPT pin. When bit D3 is set to a logic 1, the INTRPT output is enabled. When bit D3 is reset to logic 0, the INTRPT pin is forced into a high impedance state.

MODEM CONTROL REGISTER (MCR) (Continued)

BIT	NAME	COND	DESCRIPTION
D4	LOOP	0/1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected; the four Modem Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four Modem Control inputs, and the Modem Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D6		0	These bits are permanently set to logic 0.
D7	SSi Mode Osc. off	1	This bit is active in the SSi Mode only. When D7 is set the UART oscillator is tunred off placing the UART in a power shutdown state. All UART memory is retained during power shutdown.
		0	Resetting this bit enable the oscillator and powers up the UART.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits D1-D4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND	DESCRIPTION
D0	DR	0/1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading all data in the Receiver Buffer Register FIFO.
D1	OE	0/1	The Overrun Error (OE) bit is set when data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register. In FIFO mode if data continues to fill the FIFO beyond the trigger level an overrun error will occur only after the FIFO is full and the next character has been completely received in (Continued)

LINE STATUS REGISTER (LSR) (Continued)

BIT	NAME	COND	DESCRIPTION
D1	OE	0/1	the shift register. OE is indicated to the CPU as soon as it occurs. The character in the shift register is overwritten but it is not transferred to the FIFO.
D2	PE	0/1	The Parity Error (PE) bit is set when the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register. In FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples the following start bit twice and then takes in the data that follows.
D4	BI	1	The Break Interrupt (BI) bit is set when a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register. In the FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking (high) state and receives the next valid start bit.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Register into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is filled below the trigger level and will reset when the FIFO is filled to the trigger level.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character. In the FIFO mode this bit is set whenever the XMIT FIFO and the transmitter shift register are both empty.
D7	Error in Rcvr FIFO	0	In the character mode this bit is reset to 0. In the FIFO mode this bit is set when there is at least one parity error, framing error or break indication in the FIFO. This bit is reset when the CPU reads the Line Status Register if there are no subsequent errors in the FIFO.
Note:	Bits D1-D4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.		

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition four bits provide change information. Whenever bit D0, D1, D2 or D3 is set to logic 1 a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register, respectively.

BIT	NAME	COND	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit is set when the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit is set when the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit is set when the $\overline{RI}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 8 MHz) and dividing it by any divisor from 2 to 2^{16}-1. 4 MHz is the highest input clock frequency recommended when the divisor = 1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)/(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3, 4 and 5 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz, 3.072 MHz, and 8 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

TABLE 3: Baud Rates using 1.8432 MHZ Crystal

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

TABLE 4: Baud Rates using 3.072 MHZ Crystal

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344

TABLE 5: Baud Rates using 8 MHZ Crystal

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR D0 = 1, IER D0 = 1) RCVR interrupts will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached and like the interrupt it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.

D. The data ready bit (LSRD0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:
   - at least one character is in the FIFO
   - the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
   - the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCRD0 = 1, IERD1 = 1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt occurs when the XMIT FIFO is below the trigger level. It is cleared as soon as the transmitter holding register is written to and reaches the trigger level or the IIR is read. If the SSi mode is disabled (IER D5 = 0) then the XMIT FIFO trigger level is set to 1 byte.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenver the folowing occurs: THRE =1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR D0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO MODE OPERATION

With FCR D0 = 1 resetting IER D0, IER D1, IER D2, IER D3 or all to zero puts the UART in the FIFO polled mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation. In this mode the users program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR D0 will be set as long as there is one byte in the RCVR FIFO

LSR D1 to LSR D4 will specify which error(s) has occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER D2 = 0

LSR D5 will indicate when the XMIT FIFO is empty.

LSR D6 will indicate that both the XMIT FIFO and shift register are empty.

LSR D7 will indicate whether there are any errors in the RVCR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

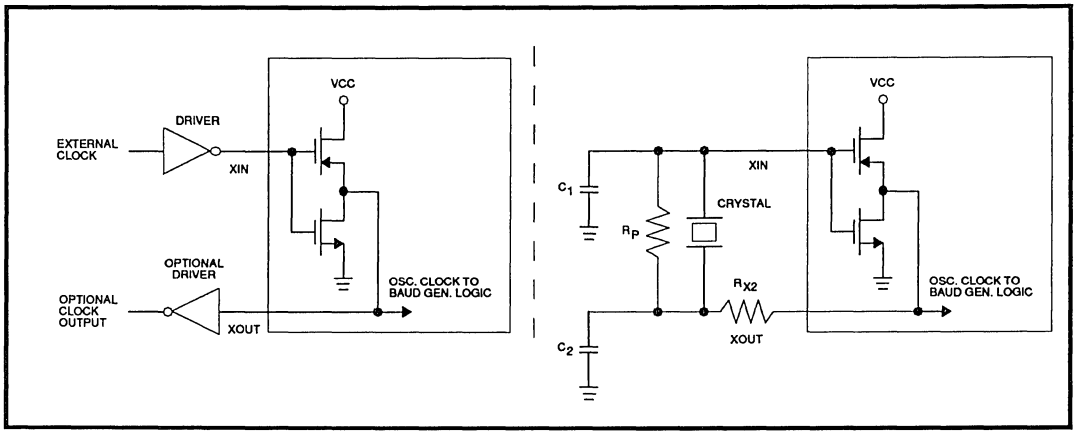


FIGURE 1: Typical Clock Circuits

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
1.8 - 8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+14V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to Vcc + 0.3

DC CHARACTERISTICS
(TA = –40°C to +85°C, VCC = 5V ± 10%, Vss = 0V, unless otherwise noted; positive current is defined as entering the chip.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		Vcc	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = -5.0 mA on all outputs except XOUT	2.4			V
ICC	Average Power Supply	See Note 1		5	10	mA
	Current	See Note 2			50	µA
IIL	Input Leakage	VCC=5.25V, VSS=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 kHz.

Note 2: VCC = 5.5V, TA = –40°C; No output load; CMOS-level inputs, oscillator disabled

CAPACITANCE
(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2	Clock Input Capacitance			15	20	pF
CXTAL1	Clock Output Capacitance			20	30	pF
CI	Input Capacitance			6	10	pF
CO	Output Capacitance			10	20	pF

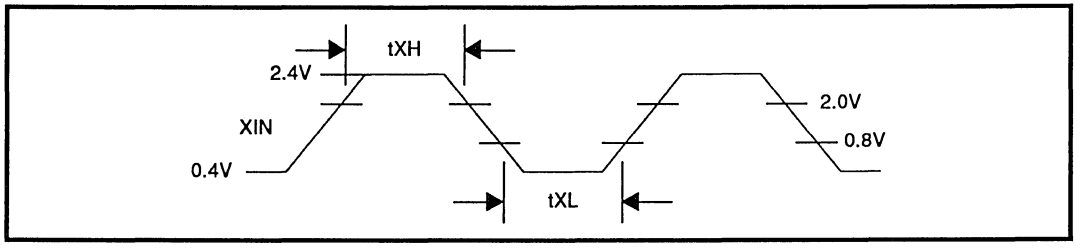


FIGURE 2: External Clock Input* (8 MHz Maximum)

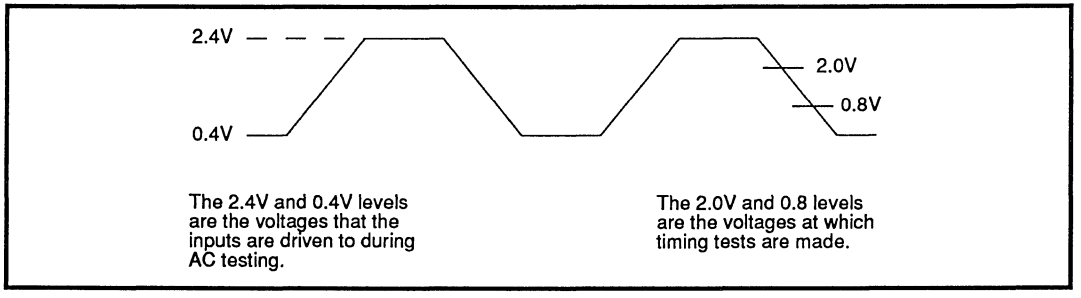


FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5.)

PARAMETER		CONDITIONS	73M550		UNITS
			MIN	MAX	
tADS	Address Strobe Width		60		ns
tAS	Address Setup Time		60		ns
tAH	Address Hold Time		0		ns
tCS	Chip Select Setup Time		60		ns
tCH	Chip Select Hold Time		0		ns
tCSR	RD, $\overline{RD}$ Delay from Chip Select	See Note 3	30		ns
tAR	RD, $\overline{RD}$ Delay from Address	See Note 3	30		ns
tRD	RD, $\overline{RD}$ Strobe Width		125		ns
tRC	Read Cycle Delay		125		ns

READ & WRITE CYCLE (Continued)

PARAMETER		CONDITIONS	73M550		UNITS
			MIN	MAX	
RC	Read Cycle	See Notes 1 & 4	280		ns
tRDD	RD, $\overline{RD}$ to Driver Disable Delay	100 pF load See Note 2		60	ns
tRVD	Delay from RD, $\overline{RD}$ to Data	100 pF load		125	ns
tHZ	RD, $\overline{RD}$ to Floating Data Delay	100 pF load See Note 2	0	100	ns
tRA	Address Hold Time from RD, $\overline{RD}$	See Note 3	20		ns
tRCS	Chip Select Hold Time from RD, $\overline{RD}$	See Note 3	20		ns
tCSW	WR, $\overline{WR}$ Delay from Select	See Note 3	30		ns
tAW	WR, $\overline{WR}$ Delay from Address	See Note 3	30		ns
tWR	WR, $\overline{WR}$ Strobe Width		100		ns
tWC	Write Cycle Delay		150		ns
WC	Write Cycle=tAW+tWR+tWC		280		ns
tDS	Data Setup Time		30		ns
tDH	Data Hold Time		30		ns
tWA	Address Hold Time from WR, $\overline{WR}$	See Note 3	20		ns
tWCS	Chip Select Hold time from WR, $\overline{WR}$	See Note 3	20		ns
tMRW	Master Reset Pulse Width		5		µs
tXH	Duration of Clock High Pulse	External Clock (8 MHz max.)	55		ns
tXL	Duration of Clock Low Pulse	External Clock (8 MHz max.)	55		ns

Note 1: RC = tAR + tRD + tRC for 73M550

Note 2: Charge and discharge time is determined by VOL, VOH and the external loading.

Note 3: Applicable only when $\overline{ADS}$ is tied low.

Note 4: In FIFO mode R = 425 ns (minimum) between reads of the RCVR FIFO and the status registers (interrupt identification register or line status register).

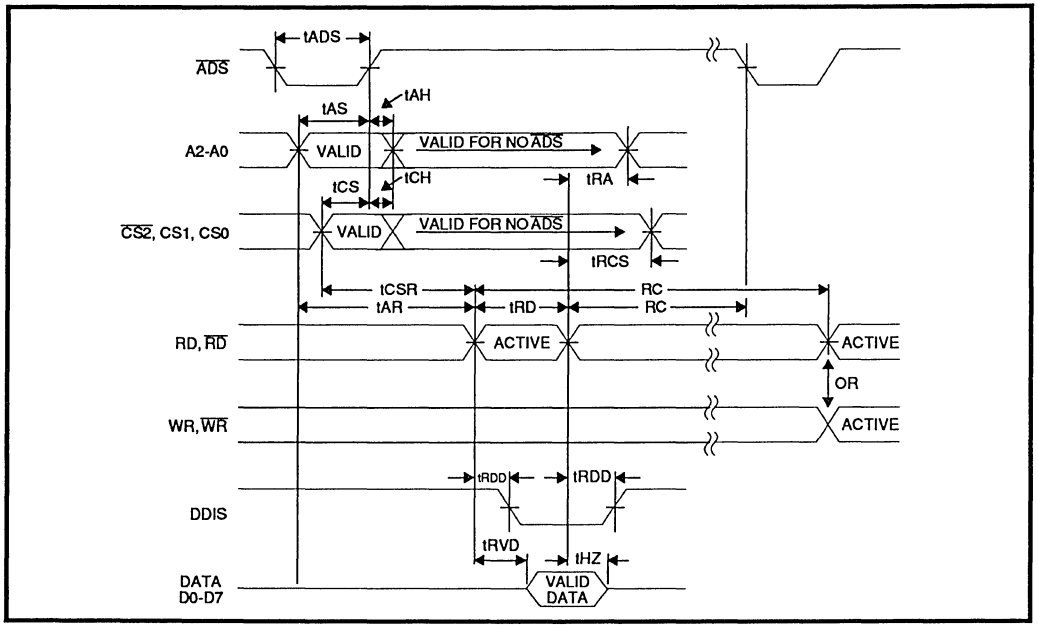


FIGURE 4: Read Cycle Timing

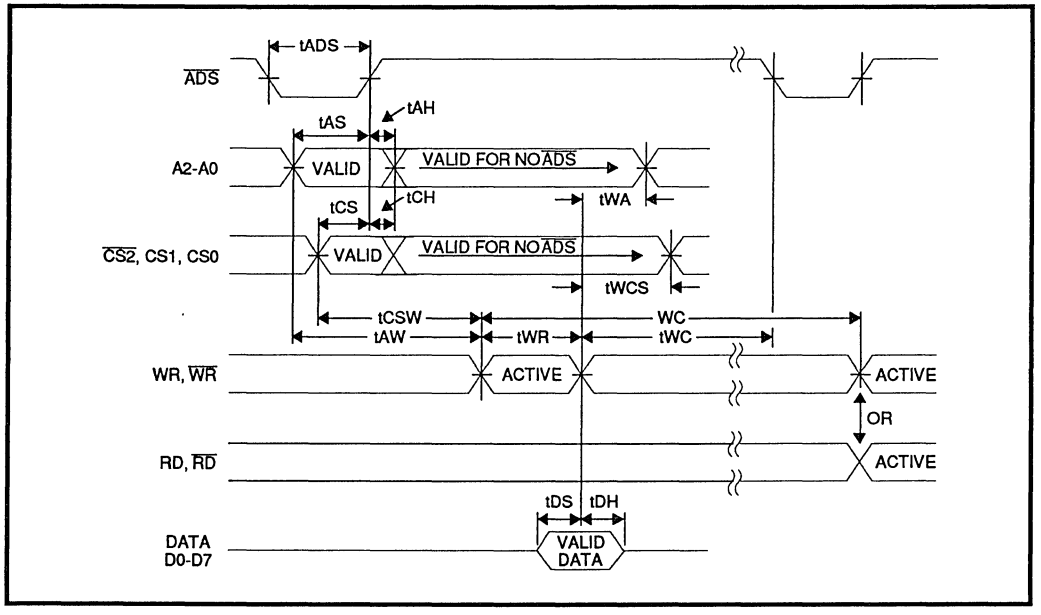
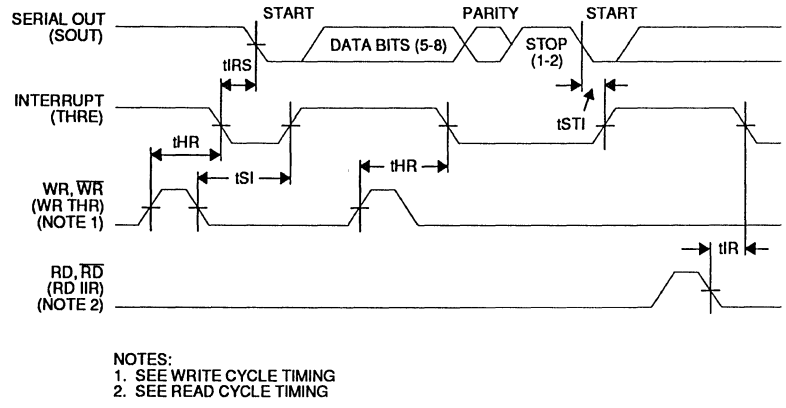


FIGURE 5: Write Cycle Timing

TRANSMITTER (Refer to Figure 6)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from rising edge of WR, $\overline{WR}$ (WR THR)to Reset Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		8	24	BAUDOUT cycles
tSI	Delay from Initial Write to Interrupt	See Note 1	16	24	BAUDOUT cycles
tSTI	Delay from Stop to Interrupt (THRE)	See Note 1	8	8	BAUDOUT cycles
tIR	Delay from RD, $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF load		250	ns
tSXA	Delay from Start to $\overline{TXRDY}$ active	100 pF load		8	BAUDOUT cycles
tWXI	Delay from Write to $\overline{TXRDY}$ inactive	100 pF load		195	ns
Note:	This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active (see FIFO Interrupt mode operation).				



NOTES:
1. SEE WRITE CYCLE TIMING
2. SEE READ CYCLE TIMING

FIGURE 6: Transmitter Timing

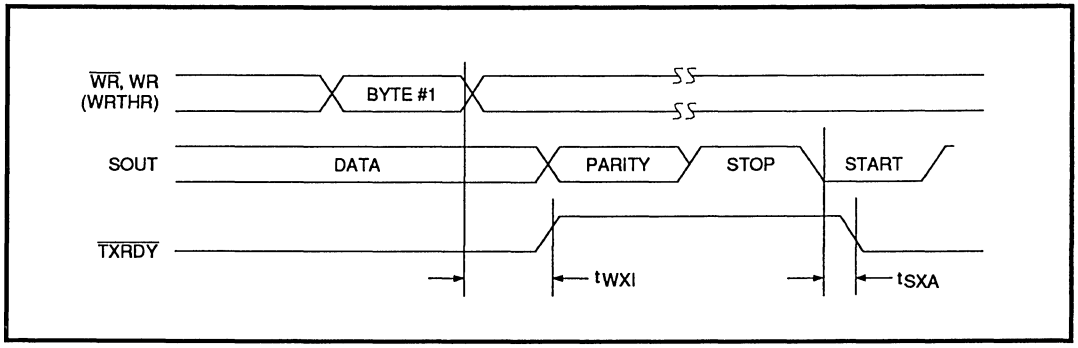


FIGURE 7: Transmitter Ready (Pin 24) FCR D0 = 0 or FCR D0 = 1 and FCR D3 = 0 (Mode 0)

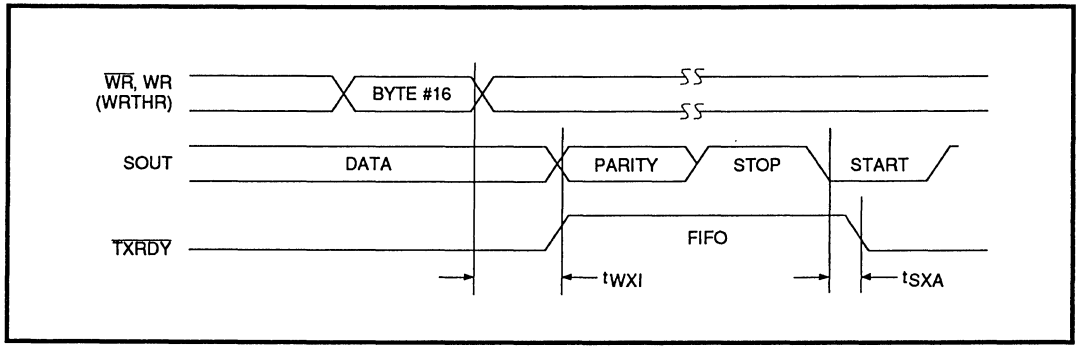
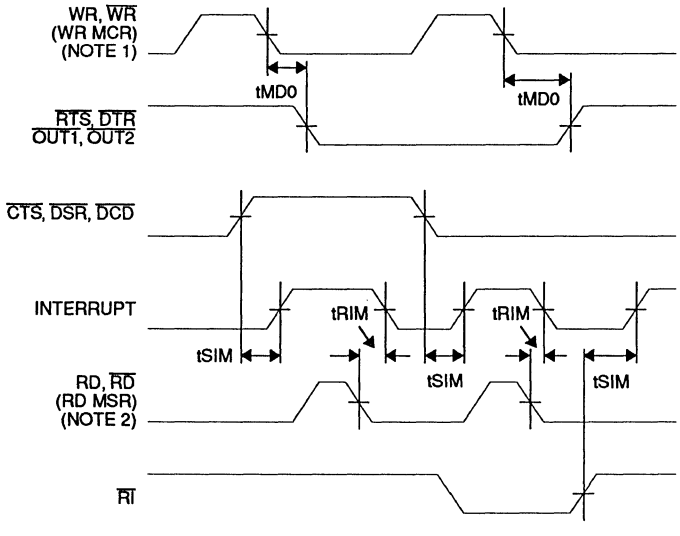


FIGURE 8: Transmitter Ready (Pin 24) FCR D0 = 1 and FCR D3 =1 (Mode 1)

MODEM CONTROL (Refer to Figure 9)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from WR, $\overline{WR}$ (WR MCR) to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)	100 pF load		250	ns



NOTES:
1. SEE WRITE CYCLE TIMING
2. SEE READ CYCLE TIMING

FIGURE 9: Modem Controls Timing

BAUD GENERATOR (Refer to Figure 10)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
N	Baud Divisor		1	2^{16}-1	
tBLD	Baud Output Negative Edge Delay	100 pF load		125	ns
tBHD	Baud Output Positive Edge Delay	100 pF load		125	ns
tLW	Baud Output Down Time	fX=8 MHz, div. by 2, 100 pF load	100		ns
tHW	Baud Output Up Time	fX=8 MHz, div. by 2, 100 pF load	75		ns

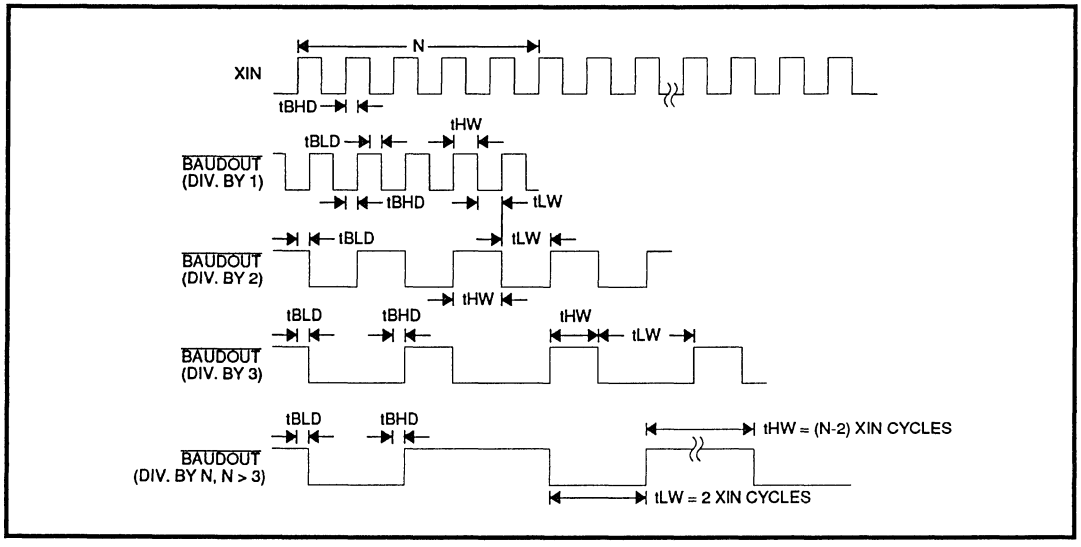
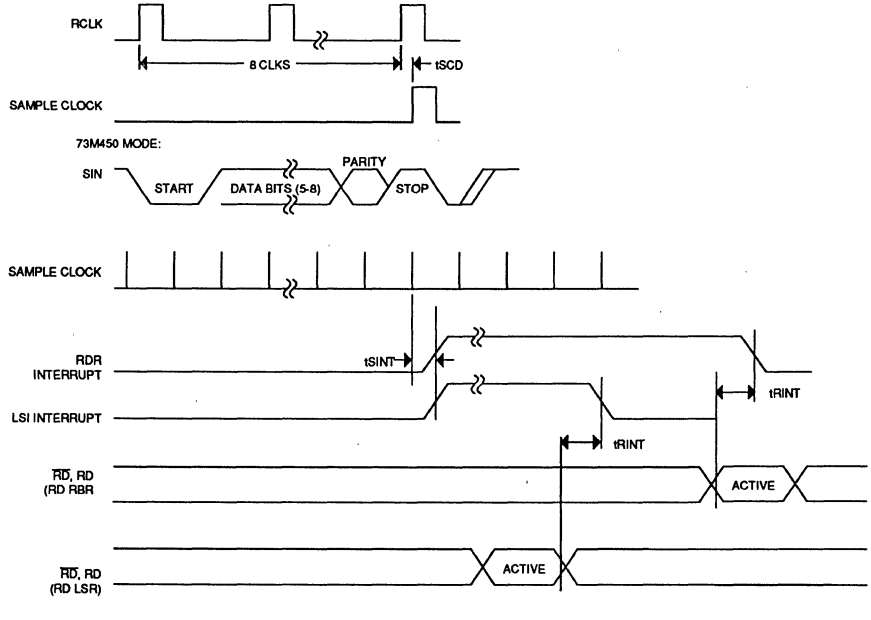


FIGURE 10: $\overline{\text{BAUDOUT}}$ Timing

RECEIVER (Refer to Figure 11)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt	RCLK=tXH & tXL See Note 1		1	RCLK cycles
tRINT	Delay from RD, $\overline{RD}$ (RD RBR/RD LSR) to Reset Interrupt	100 pF load		1	µs

Note 1: In the FIFO mode (FCR D0 = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RD RBR goes inactive. Timeout interrupt is delayed 8 RCLKs.



NOTE: SEE READ CYCLE TIMING

FIGURE 11: Receiver Timing

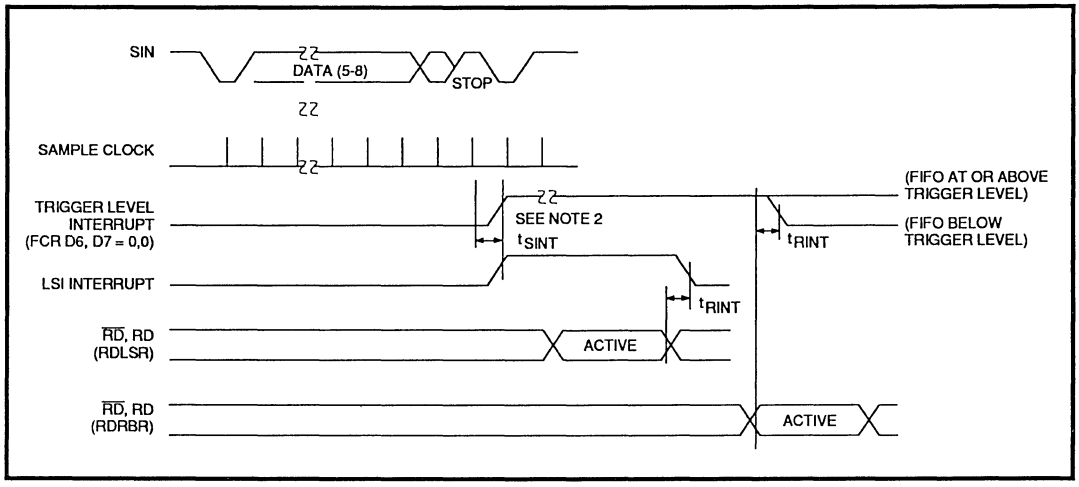


FIGURE 12: RCVR FIFO First Byte (This sets RBR)

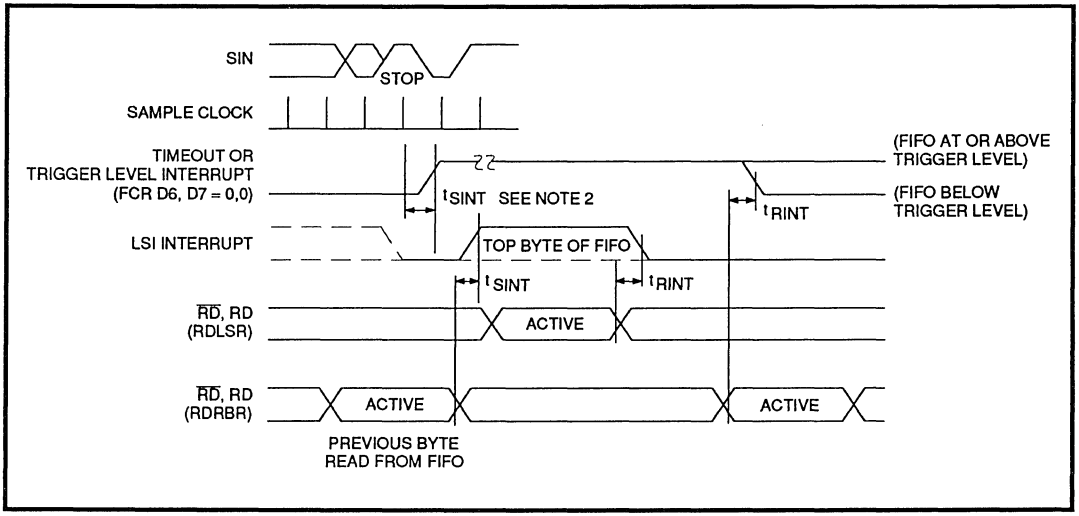


FIGURE 13: RCVR FIFO Bytes Other Than the First Byte (RBR is already set)

Note 1: This is the reading of the last byte in the FIFO

Note 2: If FCR D0 = 1, then tSINT = 3 RCLKs. For a timeout interrupt, tSINT = 8RCLKs.

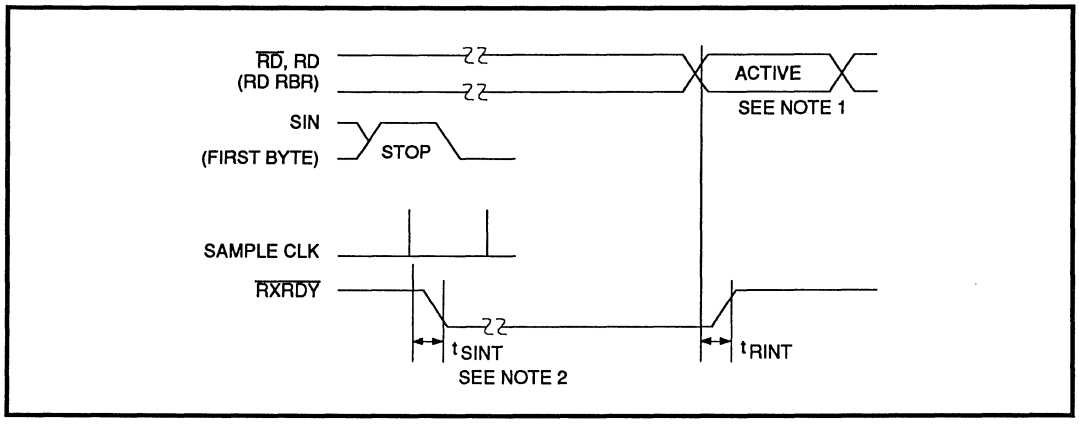


FIGURE 14: Receiver Ready (Pin 29) FCR D0 = 0 or FCR D0 = 1 and FCR D3 = 0 (Mode 0)

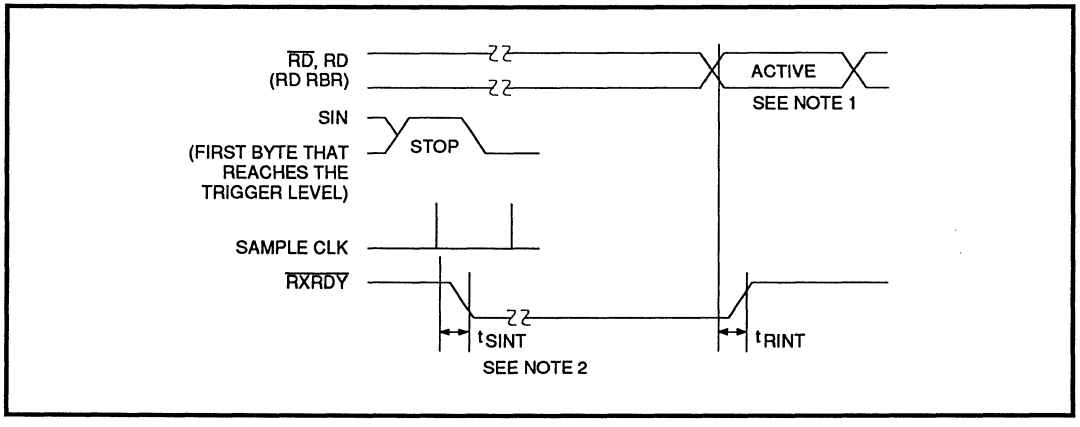


FIGURE 15: Receiver Ready (Pin 29) FCR D0 = 1 and FCR D3 = 1 (Mode 1)

Note 1: This is the reading of the last byte in the FIFO

Note 2: If FCR D0 = 1, then tSINT = 3 RCLKs. For a timeout interrupt, tSINT = 8RCLKs.

APPLICATIONS INFORMATION

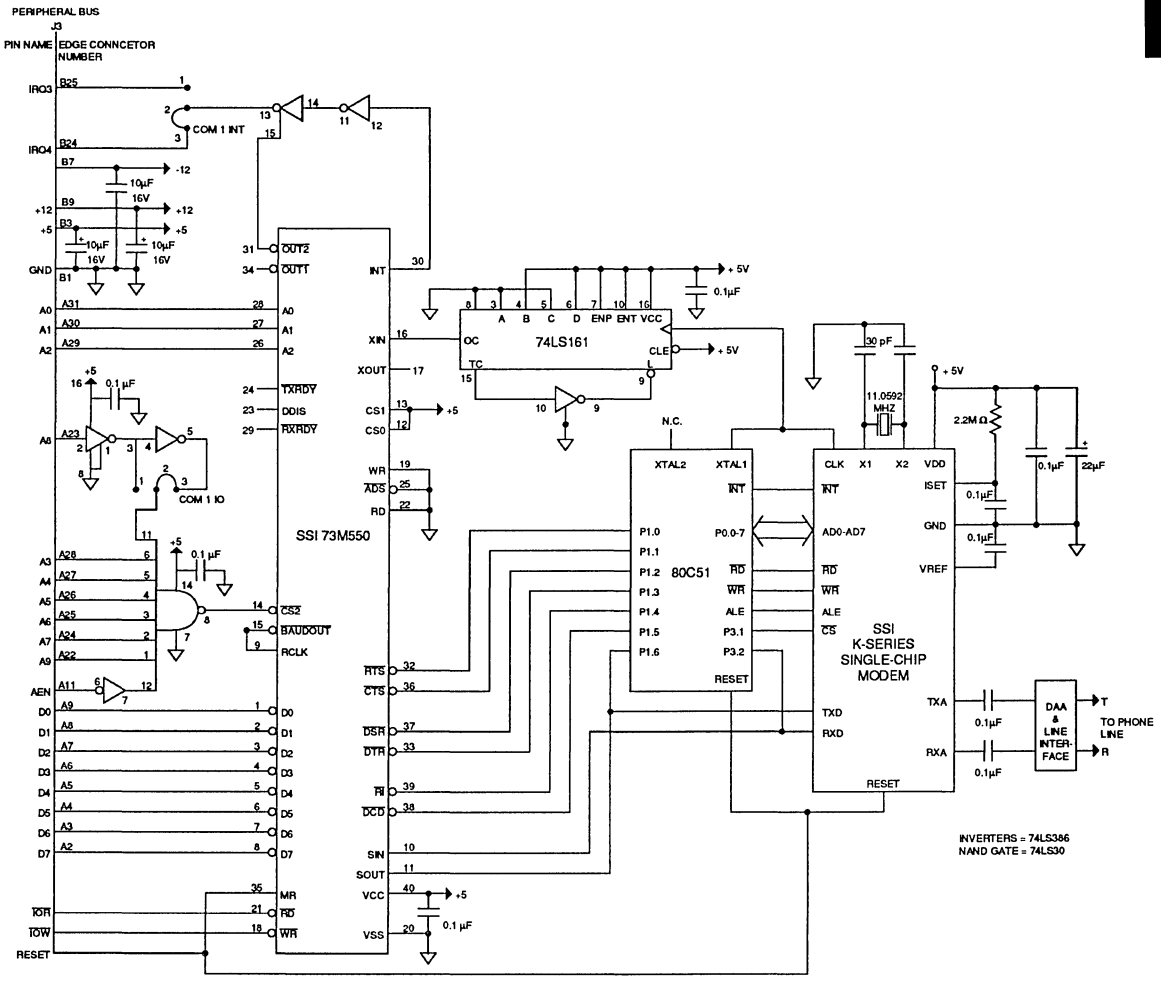
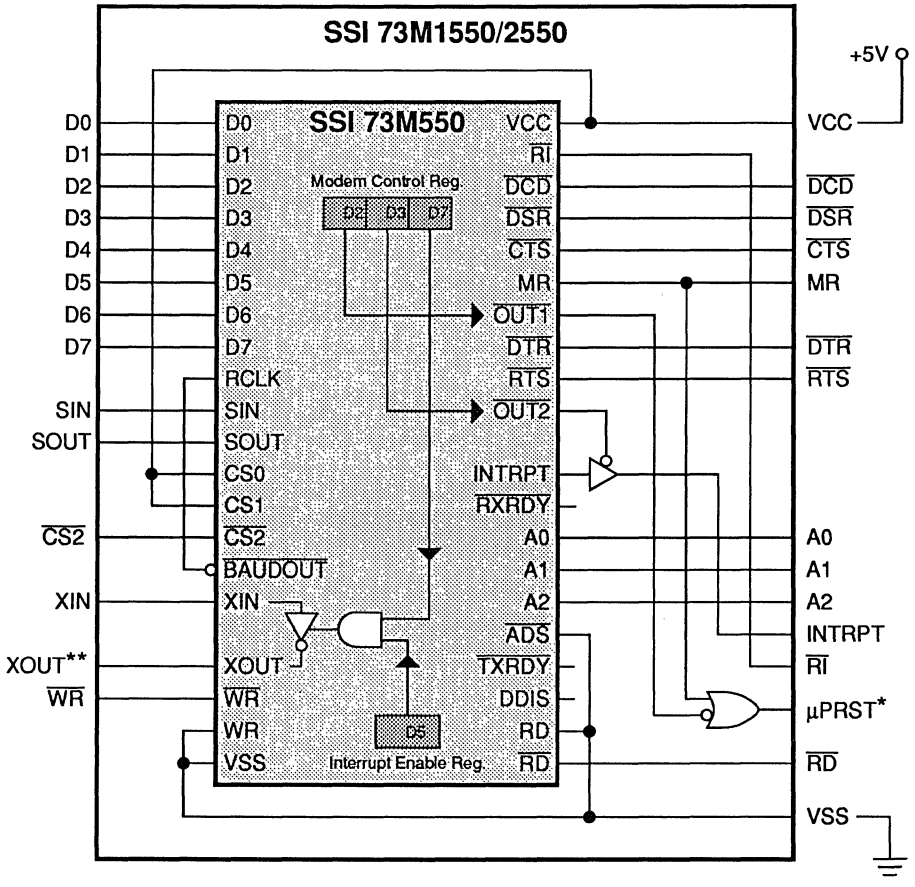


FIGURE 16: Typical Application Showing Modem Interface to Peripheral-Bus via SSI 73M550 UART

APPLICATIONS INFORMATION (Continued)

28-PIN VERSION

The 73M550 is available in two 28-pin configurations: SSI 73M1550 and SSI 73M2550. The relation between these two products and the 40-pin version is shown in the accompanying diagram. Note that the only difference between the 73M1550 and 73M2550 is that the 73M2550 adds the µPRST pin at the expense of the XOUT pin.

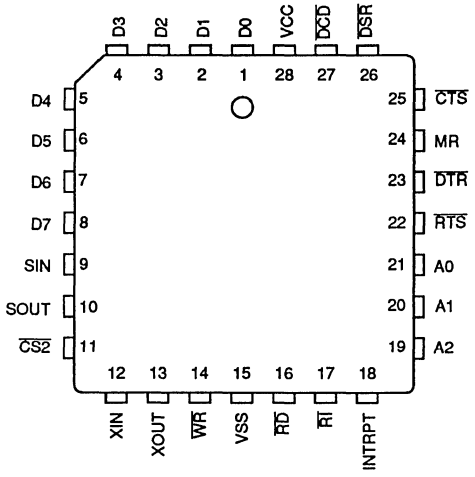


*SSI 73M2550 only.
**SSI 73M1550 only.

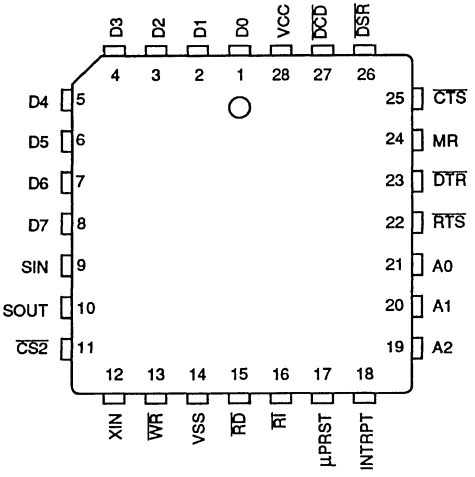
FIGURE 17: Adapter Diagram Showing Internal Connections and Bond-outs from 40-pin to 28-pin Packages

2

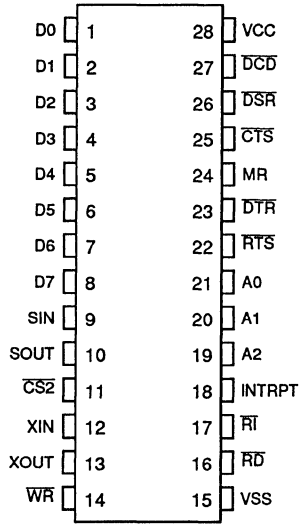
PACKAGE PIN DESIGNATIONS
(Top View)



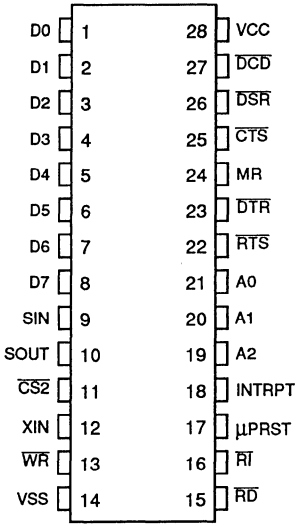
SSI 73M1550 UART
28-PIN PLCC



SSI 73M2550 UART
28-PIN PLCC



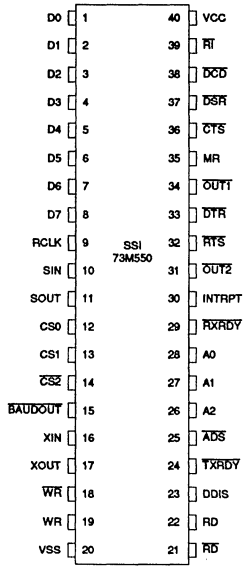
SSI 73M1550 UART
28-PIN DIP



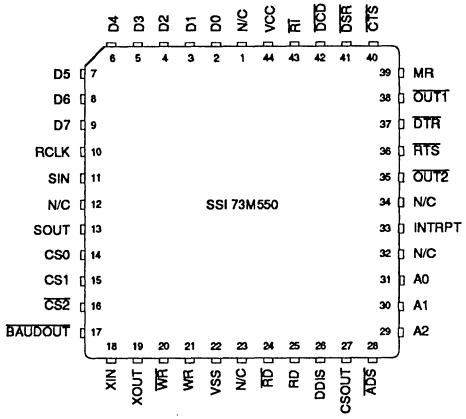
SSI 73M2550 UART
28-PIN DIP

SSI 73M550
SSI 73M1550/2550
UART with FIFOs

PACKAGE PIN DESIGNATIONS (Continued)
(Top View)



SSI 73M550 40-Pin DIP



SSI 73M550 44-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 73M550	40-pin PDIP	SSI 73M550-IP	73M550-IP
	44-pin PLCC	SSI 73M550-IH	73M550-IH
SSI 73M1550	28-pin PDIP	SSI 73M1550-IP	73M1550-IP
	28-pin PLCC	SSI 73M1550-IH	73M1550-IH
SSI 73M2550	28-pin PDIP	SSI 73M2550-IP	73M2550-IP
	28-pin PLCC	SSI 73M2550-IH	73M2550-IH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

SSI 73M1450/2450
Universal Asynchronous Receiver/Transmitter

July, 1990

2

DESCRIPTION

The SSI 73M1450 and 73M2450 are 28-pin UART ICs. These devices provide the majority of functions performed by the 40-pin SSI 73M450 UART (16C450 compatible), and include additional features. By eliminating redundant pins and minor functions, the 73M1450/2450 retain major compatibility with the 73M450 while reducing the device from a 40-pin package to a 28-pin package. The 73M1450/2450 are primarily used in the interface between a serial data port and the parallel peripheral bus in microprocessor systems.

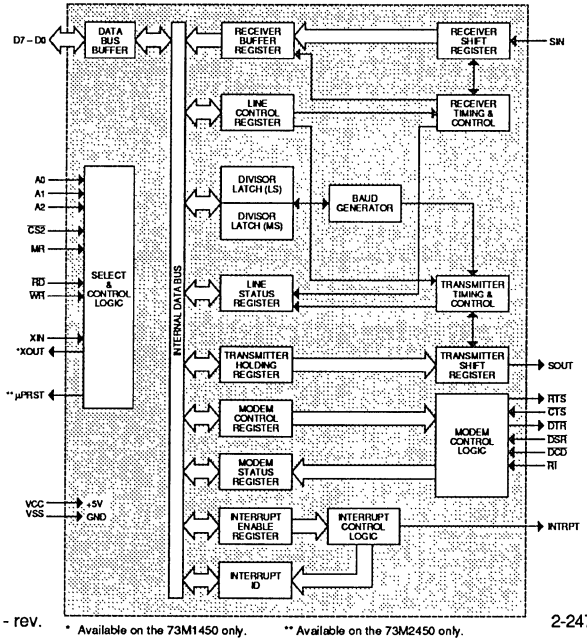
The 73M1450/2450 provide enhanced functions not found in the 73M450 UART. These functions include a bit-programmable oscillator disable for power conservation, a bit-programmable high impedance state on the INTRPT pin, and mPRST pin available on the 73M2450 for resetting external hardware.

(Continued)

FEATURES

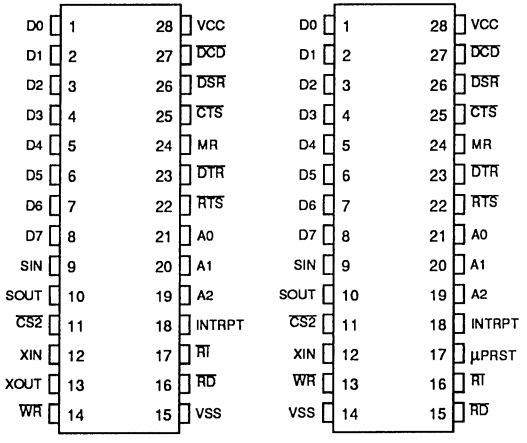
- **Compact, 28-pin DIP or PLCC package types**
- **Bit programmable oscillator disable provides a shut-down mode while retaining memory**
- **Bit programmable high impedance state of INTRPT pin**
- **mPRST pin for external hardware reset (73M2450)**
- **High drive current for directly driving large loads**
- **Full CMOS design for low-power, quiescent operation**
- **Available in two versions:**
  - **73M1450 features XIN & XOUT pins for crystal connection**
  - **73M2450 features XIN pin for external clock input, and mPRST pin for external hardware reset**

BLOCK DIAGRAM



* Available on the 73M1450 only. ** Available on the 73M2450 only.

PIN DIAGRAM



73M1450
28-Pin DIP

73M2450
28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The 73M1450/2450 eliminates the following pins from a 73M450 UART in order to achieve the smaller, 28-pin package configuration: RCLK, CS0, CS1, $\overline{\text{BAUDOUT}}$, $\overline{\text{OUT1}}$, RD, DDIS, CSOUT, $\overline{\text{ADS}}$, $\overline{\text{OUT2}}$, and WR. The 73M1450 and 73M2450 differ in one feature only: the 73M1450 retains the XIN and XOUT pins found in the 73M450 for connection to the external crystal, the 73M2450 replaces the XOUT pin with a µPRST pin used for resetting external hardware. The 73M2450 is then driven with an external clock input at the XIN pin.

PIN DESCRIPTION

BUS INTERFACE

NAME	73M1450	73M2450	TYPE	DESCRIPTION
$\overline{\text{CS2}}$	11	11	I	Chip Select: The UART is selected when $\overline{\text{CS2}}$ is low. This enables communication between the UART and the CPU.
A0-2	21-19	21-19	I	Register Select Address: These pins determine which UART register is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit (D7) in the Line Control Register (see Table 1) also controls which register is referenced.
$\overline{\text{RD}}$	16	15	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling $\overline{\text{RD}}$ low while the chip is selected.
$\overline{\text{WR}}$	14	13	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling $\overline{\text{WR}}$ low while the chip is selected.
D0-7	1-8	1-8	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data, control words and status information are transferred via this bus.
INTRPT	18	18	O	Interrupt (three-state): Goes high whenever any one of the following interrupt types occurs: Received Data, Transmitter Holding Register Empty, Receiver Line Status, and Modem Status. These interrupt types must be enabled via the IER for the INTRPT pin to become active. The INTRPT pin is reset low upon the appropriate interrupt service or a master reset operation. The INTRPT pin operation is enabled by setting the OUT2 bit (D3) in the Modem Control Register. When the OUT2 bit (D3) is reset to zero, the INTRPT pin is forced into a high impedance state.

DATA I/O

NAME	73M1450	73M2450	TYPE	DESCRIPTION
SIN	9	9	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	10	10	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

NAME	73M1450	73M2450	TYPE	DESCRIPTION
$\overline{RTS}$	22	22	O	Request To Send: This output is programmed by RTS bit (D1) of the Modem Control Register and represents the compliment of that bit. It is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{CTS}$	25	25	I	Clear To Send: A modem status input whose condition is complimented and reflected in the CTS bit (D4) of the Modem Status Register. When $\overline{CTS}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{DTR}$	23	23	O	Data Terminal Ready: This output is programmed by DTR bit (D0) of the Modem Control Register, and represents the compliment of that bit. It is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{DSR}$	26	26	I	Data Set Ready: A modem status input whose condition is complimented and reflected in the DSR bit (D5) of the Modem Status Register. When $\overline{DSR}$ is low, it indicates that the modem is ready to establish communications.
$\overline{DCD}$	27	27	I	Data Carrier Detect: A modem status input whose condition is complimented and reflected in the DCD bit (D7) of the Modem Status Register. When $\overline{DCD}$ is low, it indicates that the modem is receiving a carrier.
$\overline{RI}$	17	16	I	Ring Indicator: A modem status input whose condition is complimented and reflected in the RI bit (D6) of the Modem Status Register. When $\overline{RI}$ is low, it indicates that a telephone ringing signal is being received.

GENERAL & CLOCKS

NAME	73M1450	73M2450	TYPE	DESCRIPTION
VCC	28	28	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to GND.
VSS	15	14	I	System Ground.
MR	24	24	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{RTS}$ and $\overline{DTR}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger.
XIN XOUT	12 13	12 N/A	I/O I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source. The XOUT pin is not available on the 73M2450 which requires an external clock connected to the XIN pin.
µPRST	N/A	17	O	Microprocessor Reset: This output signal is used to provide a hardware reset to a local controller. This pin becomes active high when the MR pin is pulled high or OUT1 bit (D2) of the Modem Control Register is set. The µPRST function is available with the 73M2450 device only.

TABLE 1: CONTROL REGISTER ADDRESS TABLE

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read), Transmitter Holding Reg. (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read only)
X	0	1	1	Line Control Register
X	1	0	0	Modem Control Register
X	1	0	1	Line Status Register
X	1	1	0	Modem Status Register
X	1	1	1	Scratch Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

TABLE 2: UART RESET FUNCTIONS

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1 & 2 are low; bits 3-7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
µPRST	Master Reset/set OUT1 bit	High during active Master Reset/OUT1 bit; low afterwards

CONTROL REGISTER OVERVIEW

REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER							
			D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB = 0	0	0	SSI MODE	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB = X	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	011 DLAB = X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB = X	OSC OFF	0	0	LOOP	OUT2 (INTRPT ENABLE)	OUT1 (μPRST CNTRL)	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB = X	0	TRANSMIT-TER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB = X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB = X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. This register also allows access to the chip's special SSI mode which contains the oscillator disable function. It is possible to totally disable the interrupt system by resetting bits D0 through D3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

The chip's SSI mode can be activated by setting bit D5. Once in the SSI mode, the chip can be placed in a power shut-down state by setting bit D7 in the Modem Control Register.

BIT	NAME	COND.	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Interrupt when set to logic 1.
D4	Not used	0	Always logic 0.
D5	SSI Mode	0	Disables chip's SSI Mode; normal operation.
		1	Enables chip's SSI mode. In this mode, chip can be placed into power shut-down by setting bit D7 in modem control register.
D6-D7	Not used	0	Always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND.	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit D0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit D0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	N/A
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND.		DESCRIPTION
D0	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit D2 is a logic 0, one stop bit is generated in the transmitted data. If bit D2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit D2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit D3 is a logic 1 and bit D4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit D3 is a logic 1 and bit D4 is a logic 1, an even number of logic 1's is transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND.		DESCRIPTION
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit D3 is a logic 1 and bit D5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit D4 is a logic 1 or as a logic 1 if bit D4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		This is the Break Control bit. When set to a logic 1, the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit D6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - A0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers.

BIT	NAME	COND.	DESCRIPTION
D0	DTR	0/1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit D0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit D0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	0/1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit D1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit D1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	OUT1 (µPRST control)	0/1	This bit controls the µPRST output. When bit D2 is set to a logic 1, the µPRST output is forced to a logic 1. When bit D2 is reset to logic 0, the µPRST is forced to logic 0.
D3	OUT2 (INTRPT enable)	0/1	This bit controls the INTRPT output. When bit D3 is set to logic 1, the INTRPT output is enabled. When bit D3 is reset to logic 0, the INTRPT output is forced into a high impedance state.
D4	LOOP	0/1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit D4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected; the three modem control output pins ($\overline{DTR}$, $\overline{RTS}$ and µPRST) are forced to their inactive state; the four modem control register bits DTR, RTS, OUT1 and OUT2 are mapped to the modem status register bits CTS, DSR, RI and DCD, respectively. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D6		0	These bits are permanently set to logic 0.
D7	OSC OFF	0/1	This bit is available only in the SSI mode. Resetting this bit allows normal operation. Setting this bit places the chip in a power shut-down mode.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits 1-4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND.	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading the data in the Receiver Buffer Register.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Regsiter into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character.
D7	-	0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition, four bits provide change information. Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register respectively.

BIT	NAME	COND.	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit indicates that the $\overline{RI}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit D4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit D4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit D4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit D4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 4 MHz) and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)÷(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

TABLE 3: BAUD RATES USING 1.8432 MHZ CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 4: BAUD RATES USING 3.072 MHZ CRYSTAL

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-

ABSOLUTE MAXIMUM RATINGS
(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+14V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to V_{DD} + 0.3

DC CHARACTERISTICS
(TA = –40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		V_{CC}	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		V_{DD}	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = 5.0 mA on all outputs except XOUT	2.4			V
IDD	Power Supply Current	See Note 1		5	10	mA
IDD	Power Supply Current	See Note 2			50	µA
IIL	Input Leakage	VCC=5.25V, GND=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 KHz.

Note 2: VCC = 5.5V, TA = -45°C; No output load; CMOS level inputs; Oscillator disabled or XIN = VCC

CAPACITANCE
(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2 Clock Input Capacitance			15	20	pF
CXTAL1 Clock Output Capacitance			20	30	pF
CI Input Capacitance			6	10	pF
CO Output Capacitance			10	20	pF

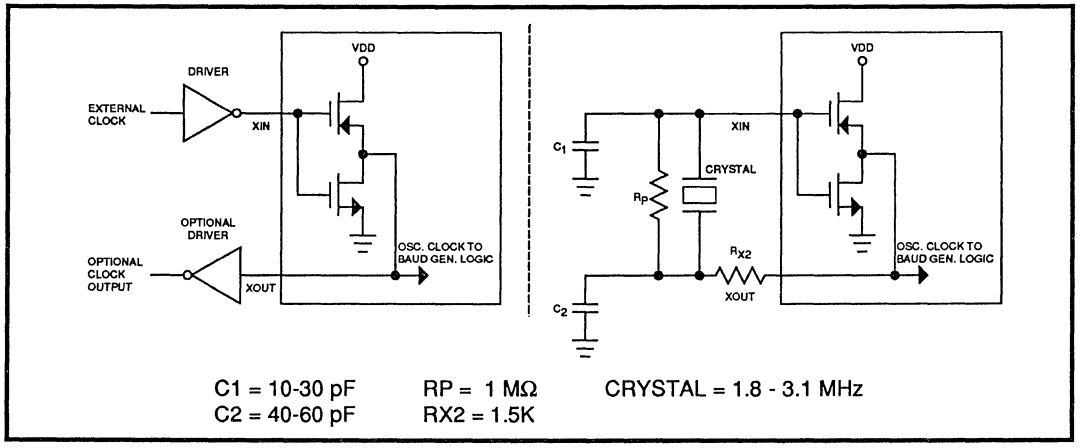


FIGURE 1: Typical Clock Circuits

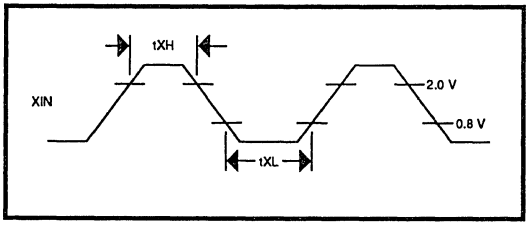


FIGURE 2: External Clock Input*
(4 MHz Maximum)

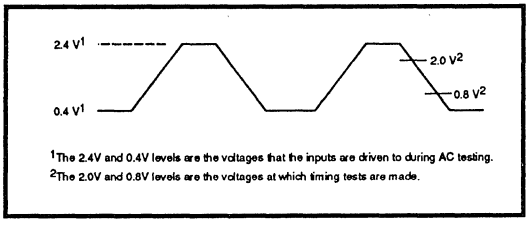


FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tCSR	$\overline{RD}$ Delay from Chip Select		50		ns
tAR	$\overline{RD}$ Delay from Address		60		ns
tRD	$\overline{RD}$ Strobe Width		125		ns
tRC	Read Cycle Delay		175		ns
RC	Read Cycle	See Note 1	360		ns
tRVD	Delay from $\overline{RD}$ to Data	100 pF load		125	ns
tHZ	$\overline{RD}$ to Floating Data Delay	100 pF load See Note 2	0	100	ns
tRA	Address Hold Time from $\overline{RD}$		20		ns
tRCS	Chip Select Hold Time from $\overline{RD}$		20		ns
tCSW	$\overline{WR}$ Delay from Select		50		ns
tAW	$\overline{WR}$ Delay from Address		60		ns
tWR	$\overline{WR}$ Strobe Width		100		ns
tWC	Write Cycle Delay		200		ns
WC	Write Cycle=tAW+tWR+tWC		360		ns
tDS	Data Setup Time		40		ns
tDH	Data Hold Time		40		ns
tWA	Address Hold Time from $\overline{WR}$		20		ns
tWCS	Chip Select Hold time from $\overline{WR}$		20		ns
tMRW	Master Reset Pulse Width		5		µs
tXH	Duration of Clock High Pulse	External Clock (4 MHz max.)	100		ns
tXL	Duration of Clock Low Pulse	External Clock (4 MHz max.)	100		ns

Note 1: RC = tAR + tRD + tRC
Note 2: Charge and discharge time is determined by VOL, VOH and the external loading.

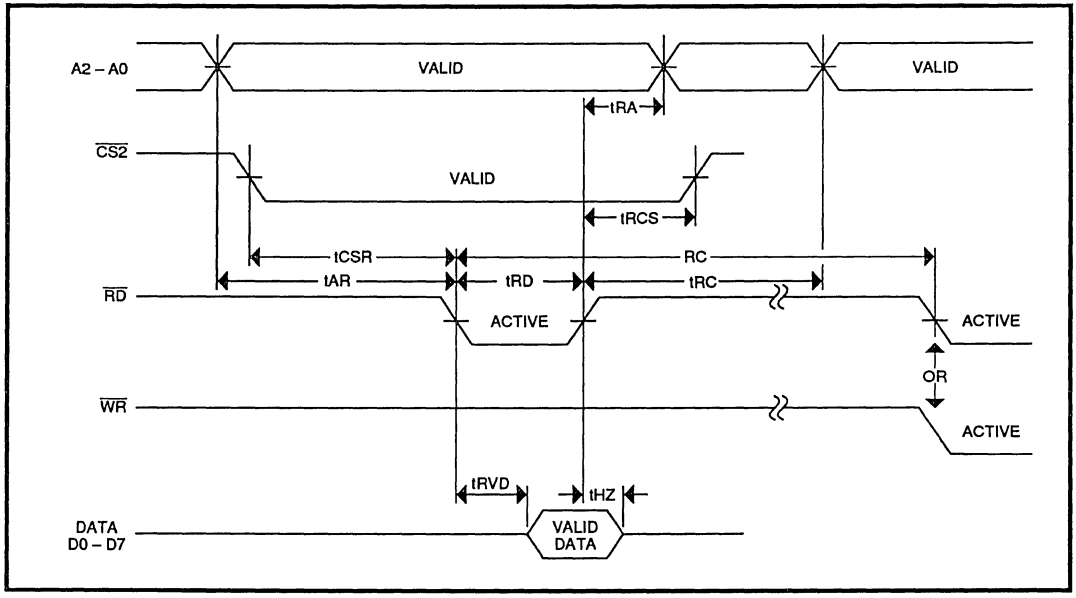


FIGURE 4: Read Cycle Timing

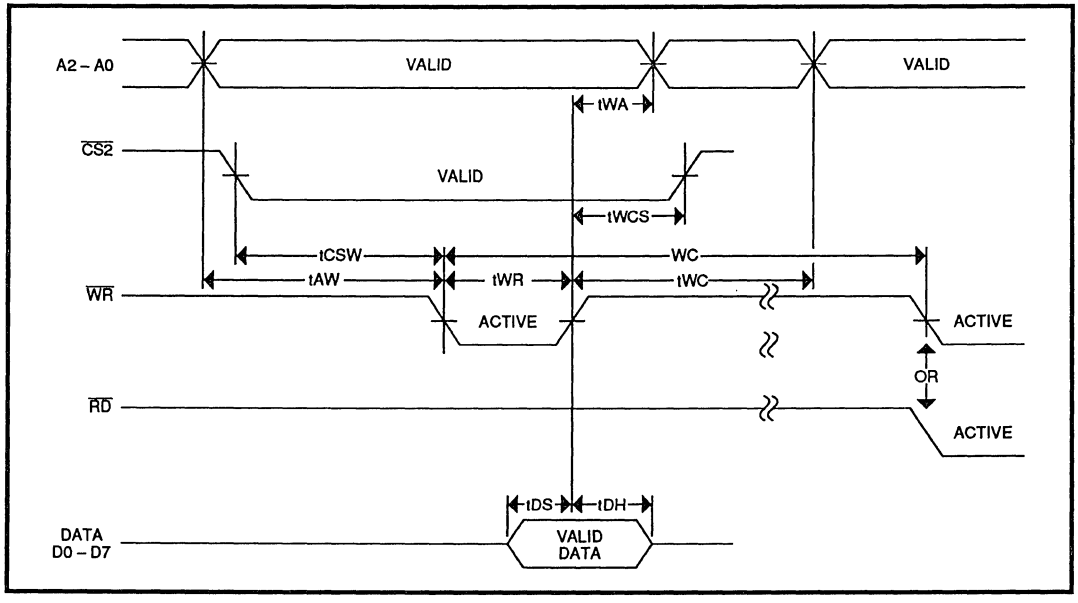


FIGURE 5: Write Cycle Timing

AC CHARACTERISTICS (Continued)

TRANSMITTER (Refer to Figure 6.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from falling edge of $\overline{WR}$ (WR THR)to Reset Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		24	40	BAUD CLK cycles
tSI	Delay from Initial Write to Interrupt		16	32	BAUD CLK cycles
tSTI	Delay from Stop to Interrupt (THRE)		8	8	BAUD CLK cycles
tIR	Delay from $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)	100 pF load		250	ns

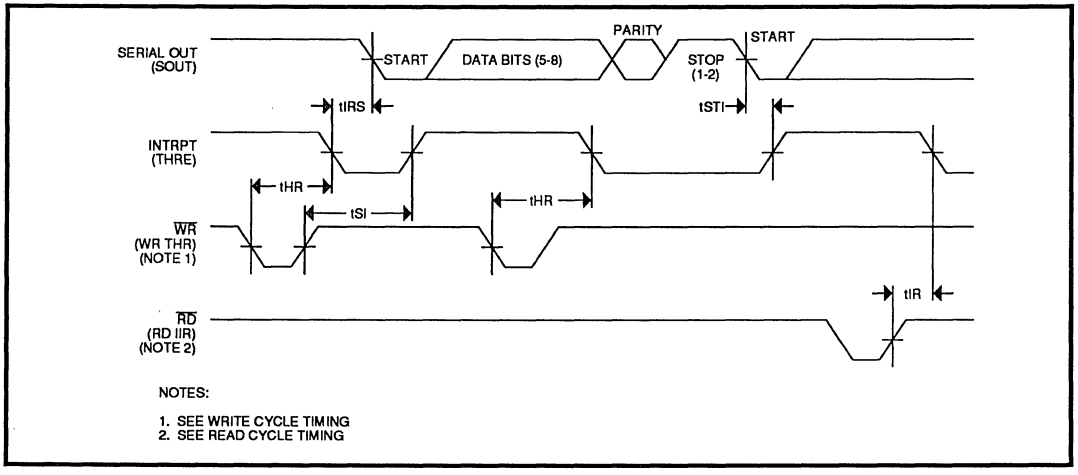


FIGURE 6: Transmitter Timing

AC CHARACTERISTICS (Continued)

MODEM CONTROL (Refer to Figure 7.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from $\overline{WR}$ (WR MCR) to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Reset Interrupt from $\overline{RD}$ (RS MSR)	100 pF load		250	ns

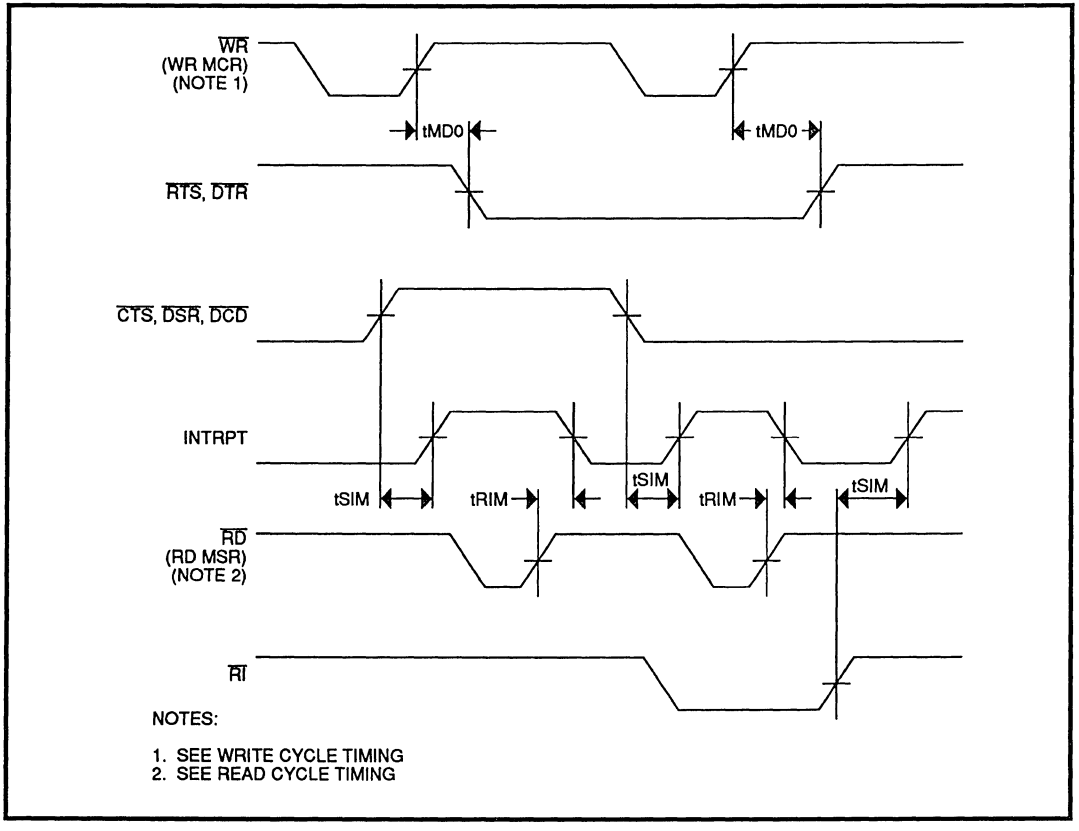


FIGURE 7: Modem Controls Timing

AC CHARACTERISTICS (Continued)

RECEIVER (Refer to Figure 8.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt			1	BAUD CLK cycles
tRINT	Delay from $\overline{RD}$ (RD RBR/RDLSR) to Reset Interrupt	100 pF load		1	µs

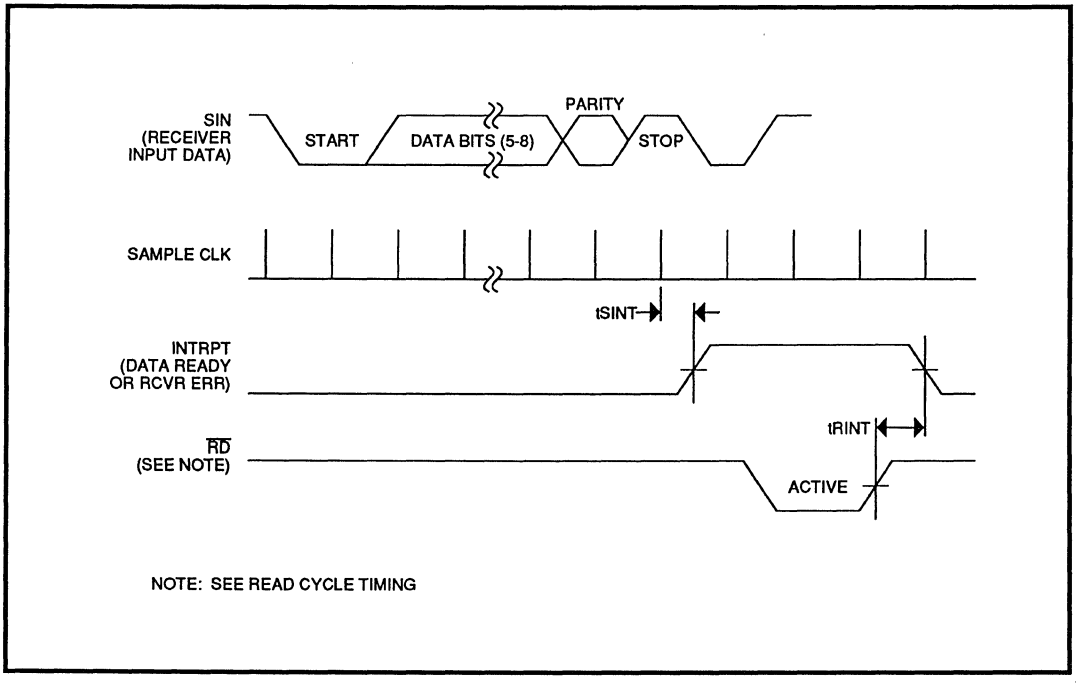


FIGURE 8: Receiver Timing

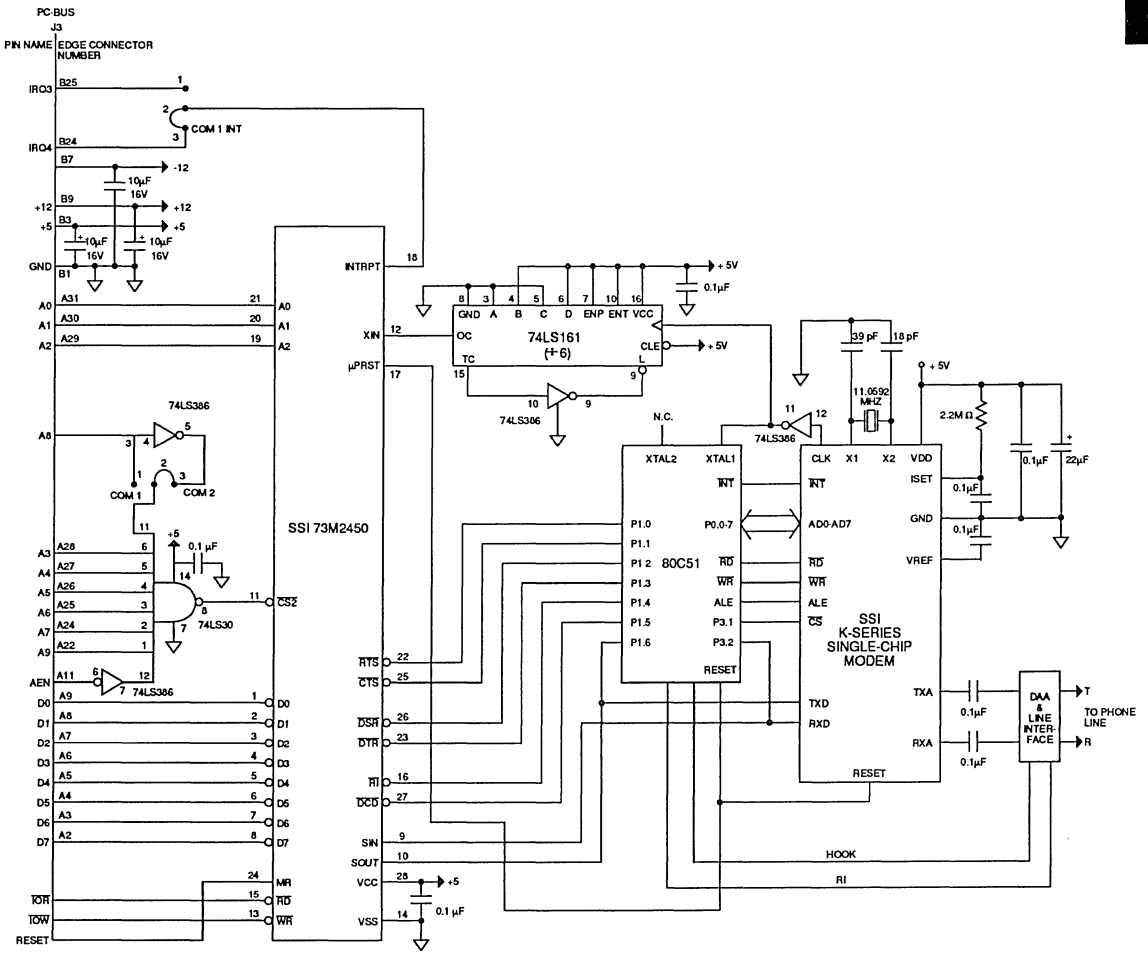
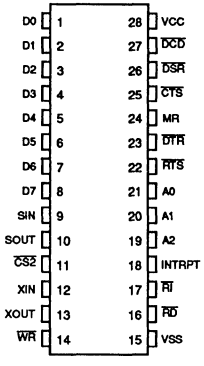


FIGURE 9: Typical Application Showing Modem Interface to PC-Bus via SSI 73M2450 UART

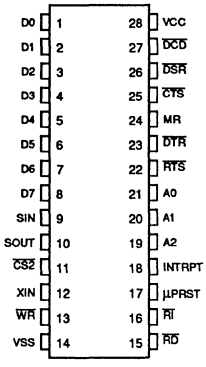
SSI 73M1450/2450
Universal Asynchronous Receiver/Transmitter

PACKAGE PIN DESIGNATIONS

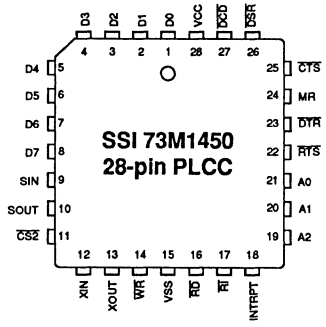
(TOP VIEW)

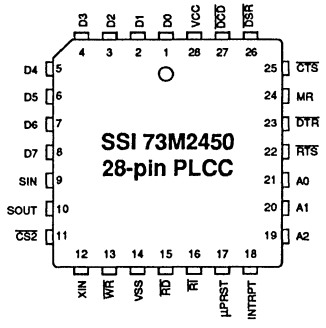


SSI 73M1450 28-pin DIP



SSI 73M2450 28-pin DIP





ORDERING INFORMATION

PART DESCRIPTION		ORDER NO.	PKG. MARK
SSI 73M1450	28-pin PDIP	SSI 73M1450-IP	73M1450-IP
	28-pin PLCC	SSI 73M1450-IH	73M1450-IH
SSI 73M2450	28-pin PDIP	SSI 73M2450-IP	73M2450-IP
	28-pin PLCC	SSI 73M2450-IH	73M2450-IH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

SSI 73M650/1650
Serial Packet Controller

Advance Information

July, 1990

2

DESCRIPTION

The SSI 73M650 Serial Packet Controller (SPC) is a multifunction synchronous/asynchronous communications IC that simplifies synchronous communications interface to a standard PC peripheral bus. The SPC consists of the control and FIFO registers of a 16550A UART combined with one channel of an 8530 SCC. It operates in two basic configurations.

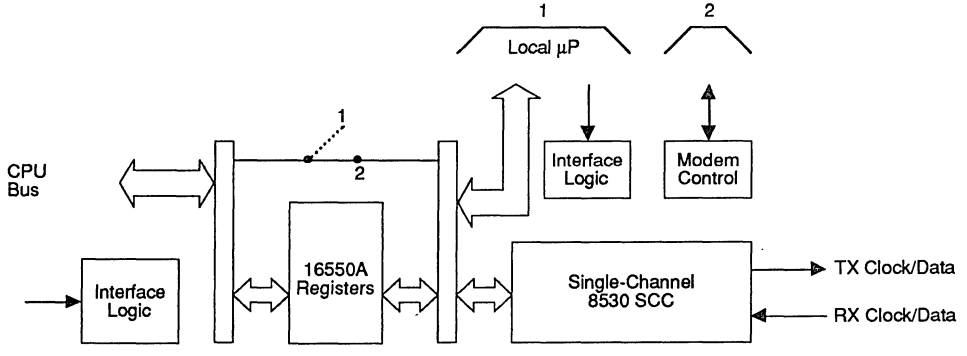
The Dual-Processor configuration has two parallel interface ports, one for connection to a CPU and the other to a local protocol controller. The local controller can then use the SCC block for synchronous or asynchronous protocols.

The Single-Processor configuration can be used in either a Mailbox or Non-mailbox mode. The Mailbox mode uses the same internal configuration as Dual-Processor, but all registers are accessible through only one hardware port. This allows the CPU to replace the function of the local controller while the SPC maintains the standard asynchronous interface. In the Non-mailbox mode, the SPC is simply a 16550A and one channel of an 8530 in the same package. The user may select either the 16550A block or the 8530 block.

FEATURES

- **Register compatibility with 16550A UART**
- **Functional superset of a single channel 8530 SCC**
- **DMA signals available in 44-pin package**
- **NRZ, NRZI, FM and Manchester encode and decode**
- **32-bit CRC for V.42 compatibility**
- **3-byte transmit FIFO for SCC reduces interrupt overhead**
- **External devices can be mapped into PC I/O space**
- **Oscillator disable for low power standby**
- **Clock pre-divide to allow input of higher frequency processor clocks**
- **16-byte UART transmit and receive FIFOs reduce CPU overhead**
- **Space-saving 28-pin version (73M1650)**

BLOCK DIAGRAM



1) Dual Processor Only

2) Single Processor Only

FUNCTIONAL DESCRIPTION

The SSI 73M650 Serial Packet Controller (SPC) simplifies high speed packetized serial communications in the PS/2 or PC bus environment.

FUNCTIONAL BLOCKS

The SPC is configured as two main blocks: the 16550A Main Processor UART Register block which facilitates interface to software packages written for 16450/16550A UARTs, and a Serial Communication Controller block (SCC) which is an enhanced version of one-channel of an 8530.

16550A UART Register Block

The UART Register block is hardware- and register-compatible to a 16550A UART and will run most existing software packages. Additional bits to control power down and other features are available through a special hardware mode called Single-Chip-Select (SINGLECS).

A distinct feature of the 73M650 is the accessibility of all these registers to a second processor through Channel-B in the Dual-Processor configuration. The local processor can then modify these registers and the data FIFOs to perform compression and/or error correction (such as V.42bis) at a very high speed. This is not currently possible using standard products.

The scratchpad register, acting as a Mailbox, allows communication between the CPU and a local processor or microcontroller.

SCC Block

The SCC block implements the operation of one-channel (channel A) of an 8530 SCC. Some improvements in the 73M650 over the 8530 may require modifications to be made to the software currently available for the 8530.

The SCC block performs asynchronous data transfer and packetized synchronous protocols such as Monosync, Bisync, HDLC and SDLC. Included in this block are a baud rate generator, a Digital Phase Locked Loop (DPLL) for clock recovery, and a three-byte FIFO in the SCC transmit and receive path. The SCC block has NRZ, NRZI, FM and Manchester data encoding and supports a 32-bit CRC useful in the V.42bis error correction standard.

The SPC can operate at up to 10 Mbit/s data rate. The crystal rate may be as high as 20 MHz with an internal programmable prescaler.

REGISTER SETS

The SSI 73M650 SPC contains three register sets:

Main Processor UART Registers

This register set is virtually identical to a 16550A register set. In a special hardware mode called Single-Chip-Select (SINGLECS), additional bits are introduced into these registers.

Channel A Registers

This register set is similar to 8530 Channel A registers and controls the asynchronous and synchronous serial port.

Channel B Registers

This register set allows for access by a second processor or software package to the main processor 16550A data. An additional register contains a clock prescaler and oscillator shut down.

PRODUCT CONFIGURATIONS

The SPC is used in either single- or dual-processor environments with different applications as follows:

1. When a local processor is available for high speed packetized applications, the Dual-Processor configuration is selected by tying the SP pin to GND. In this configuration the local processor and the CPU use separate hardware pins to access the SPC. The 16550A and SCC blocks are accessed independently.
2. When no local processor is needed, the SPC is used in the Single-Processor configuration and the SP pin is connected to +5V.

For maximum functionality, the SPC can operate in a unique register access arrangement called Single-Chip-Select (SINGLECS). This is the only operating mode for the 28-pin version (73M1650), and can be selected in 40- and 44-pin versions by tying the $\overline{CS2}$ and $\overline{MCS}$ pins together.

Dual-Processor Configuration

When the SP pin is connected to GND, the SPC is put into the Dual-Processor configuration. In this configuration, the main CPU and local processor use separate address, data and control pins to access the SPC. The 16550A registers are controlled by the CPU. Some of these registers are accessible to a local processor via Channel B through separate pins. The local processor uses Channel A for serial data transfer.

Upon any change in the 16550A register contents and FIFOs status, an interrupt can be generated to notify the local processor that the CPU has accessed the SPC.

Note that in Dual-Processor configuration the Modem Control and Status signals ($\overline{RTS}$, $\overline{CTS}$, etc.) are available to the main CPU via the 16550A registers.

Single-Processor Configuration

When the SP pin is connected to +5V, the SPC operates in the Single-Processor configuration. The CPU has access to all of the registers in the SPC using one data bus (D0-D7), one read strobe ($\overline{RD}$) and one write strobe ($\overline{WR}$). The address and chip select pins may be connected in the following ways:

1. When maximum firmware compatibility to 16550A/8530 operation is desired, the main CPU accesses different registers as follows:
   a. $\overline{CS2}$, A0-A2 to access main port 16550A registers.
   b. $\overline{MCS}$, A/$\overline{B}$, D/$\overline{C}$ to access Channel A and Channel B.
2. When maximum functionality is desired, the $\overline{CS2}$ and $\overline{MCS}$ pins are tied together to take the SPC into the Single-Chip-Select (SINGLECS) mode. In this mode, which is the only operating mode for the 28-pin version (73M1650), new bits are added to the 16550A registers to allow for the following features:
   a. Firmware control of power-down.
   b. Transmit FIFO trigger level control.
   c. DMA TXRDY and RXRDY status bits.
   d. Programmable access to the three register sets using bits 7, 6 of 16550A IER (RSEL0, RSEL1 bits).
   e. Access to an external device by setting both RSEL0 and RSEL1 bits. In this unique application of the 73M650, proper signals to access a multiplexed address/data bus component (ALE, $\overline{MRD}$, $\overline{MWR}$) are generated allowing access to the external device in two cycles. This application greatly simplifies the required hardware for interface of PC bus to a local device.

Mailbox Mode

When the PE bit (bit 7 of Channel B, CCR) is set, the CPU can independently access the 16550A and SCC blocks. The SPC has the same internal set-up as the Dual-Processor configuration, however the hardware access to different registers is through only one data bus. The SCC block is now accessible to the CPU.

This allows the user to develop software drivers for the CPU to access and modify the data transmitted or received by a standard software package. This feature is useful in multi-tasking environments.

An interrupt can be sent to the CPU to invoke the operation of the auxiliary software package whenever data is transferred by the main processor. The auxiliary software package can then read the data FIFOs, modify the data by compression or error correction and transmit the new data using the SCC block.

Non-mailbox Mode

When the PE bit (bit 7 of Channel B, CCR) is cleared, the main CPU can access either the 16550A or SCC block.The SPC effectively behaves as either a 16550A or a single-channel 8530 in the same package, always operating as the block (16550A or 8530) that was last

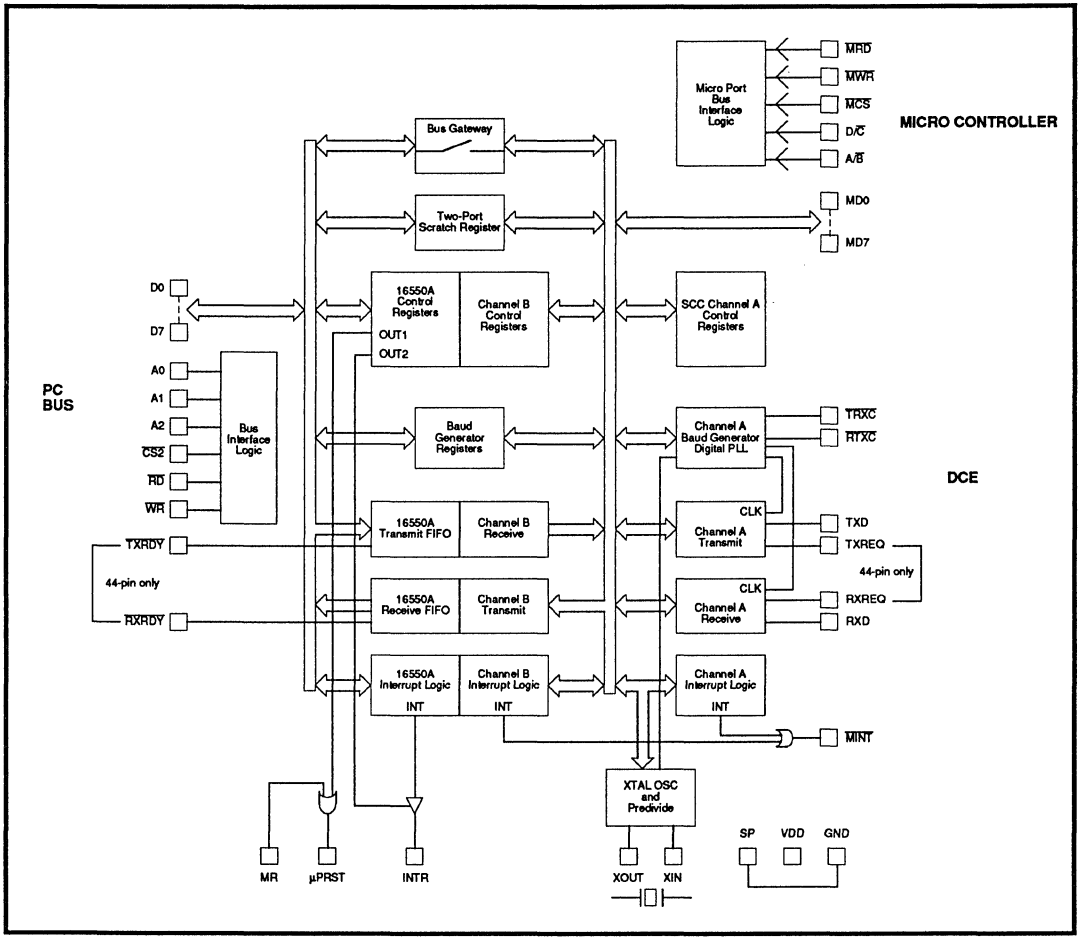


FIGURE 1: Dual-Processor Block Diagram

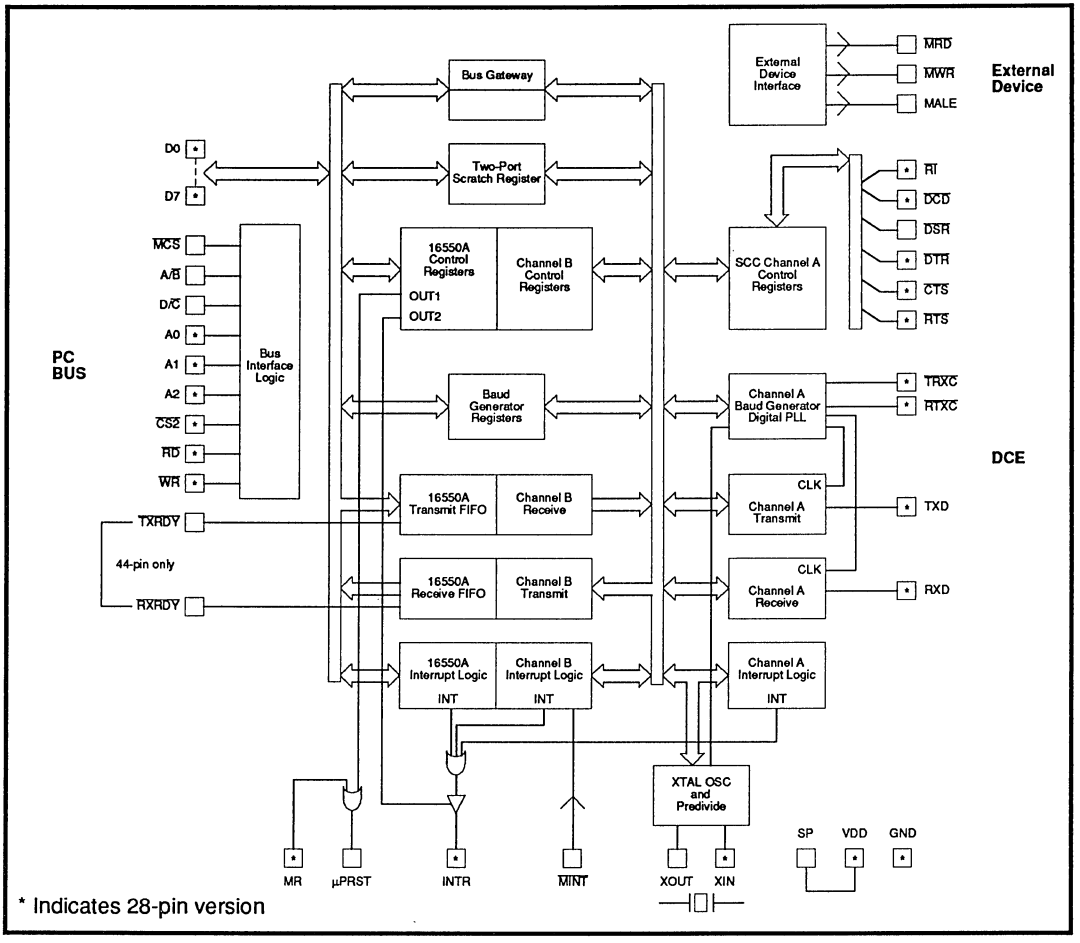


FIGURE 2: Single-Processor Mailbox Mode Block Diagram

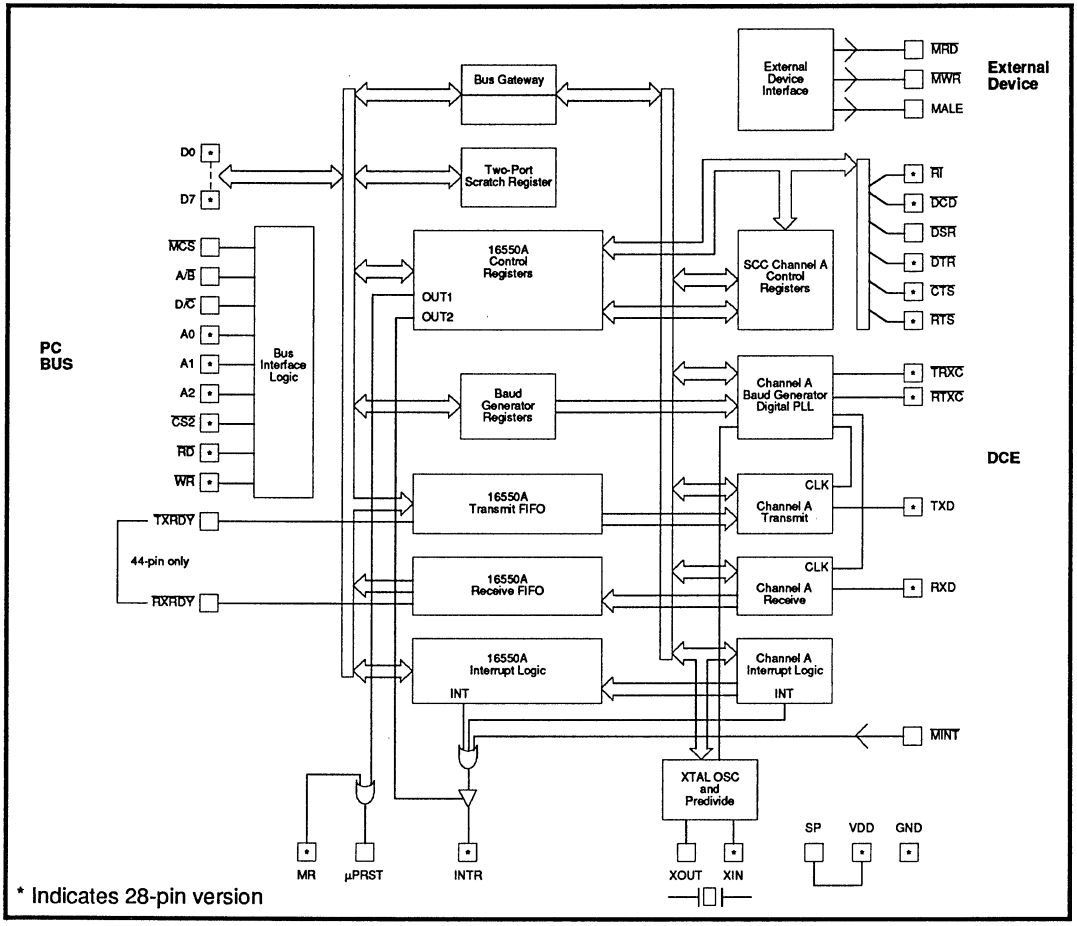


FIGURE 3: Single-Processor Non-Mailbox Mode Block Diagram

PIN DESCRIPTION

Pins marked by * are not available in 28-pin version (73M1650).

NAME	TYPE	DESCRIPTION
VDD	I	+5V Supply, ±10%. Bypass with a .1 µF capacitor.
GND	I	System Digital Ground.
SP *	I	Single-Processor Mode Select. When high, selects Single-Processor mode. When low, selects Dual-Processor mode.
XIN	I	Crystal/Clock Input. When a crystal is used for the time base, it is connected between this pin and XOUT. When an external clock is used, this pin requires a TTL logic level signal at maximum frequency of 20 MHz. By programming the 4-bit prescaler (bits 0, 1, 2, 3 of Channel B CCR), the external clock frequency can be adjusted to supply the required internal clock.
XOUT *	I/O	Crystal output. When a crystal is used for the time base, it is connected between this pin and XIN.
MR	I	Master Reset. When high, internal registers are initialized. This signal should be brought low for the normal operation of the SPC. A high on MR generates a high on the µPRST pin.
µPRST *	O	Local Microprocessor Reset. This signal follows the state of MR signal and is used to reset a local microprocessor. Programming the µPRST bit (bit 2 of 16550A MCR) to a high will also generate an active high signal on this pin.
TXD	O	Serial Transmit Data. The serial data is updated on the rising edge of the internal transmit clock. The source of transmit clock is either an inverted version of the $\overline{\text{TRXC}}$/$\overline{\text{RTXC}}$ pins signal or the output of Baud Rate Generator or the DPLL.
$\overline{\text{TRXC}}$	I/O	Synchronized Clock. The function of this pin is controlled by the TRXCO/I bit (bit 2 of Channel A WR11). If the TRXCO/I bit is set, this pin is an output clock whose rising edge can be used to sample TXD signal . If the TRXCO/I bit is cleared, this pin functions as an input transmit clock. When the source of the transmit clock is selected to be this pin by programming bits 4, 3 of Port-A WR11 to 01, the serial transmit data (TXD) pin is updated on the falling edge of this signal. When other sources of transmit clock are selected, the TXD has no phase relationship to this signal.
RXD	I	Serial Receive Data. Serial data is sampled on the falling edge of the internal receive clock. The source of the receive clock is either an inverted version of the $\overline{\text{TRXC}}$/$\overline{\text{RTXC}}$ pins signal or the output of Baud Rate Generator or the DPLL.

PIN DESCRIPTION (Continued)

Pins marked by * are not available in 28-pin version (73M1650).

NAME	TYPE	DESCRIPTION
$\overline{RTXC}$	I	Synchronized Receive Clock. When an external receive clock source is selected by clearing bits 4, 3 of Channel A WR11, the data on the RXD pin is sampled on the rising edge of this signal. The received clock may also be supplied by the $\overline{TRXC}$ pin, Baud Rate Generator or the DPLL, in which case this pin has no function. In comparison with the 8530, this pin has no accommodation for an external crystal to supply the receive clock.
$\overline{TXRDY}$ *	O	DMA Transmit Request. Available on the 44-pin version only; shows the status of the 16550A transmit FIFO. In the non-FIFO or 16450 mode (bit 0 FCR cleared) or when no DMA is selected (bit 3 FCR cleared), $\overline{TXRDY}$ goes active low when there is no character in the transmit FIFO and returns high when the first character is loaded into the FIFO. In the FIFO mode (bit 0 FCR set) and when DMA is selected (bit 3 FCR set), $\overline{TXRDY}$ goes active low as the transmit FIFO trigger level is reached and goes inactive high when the FIFO is completely full. If the Silicon Systems enhancement mode is not selected (bit 5 IER cleared), $\overline{TXRDY}$ goes active when the FIFO is not full. This is equivalent to a FIFO trigger level of 15.
$\overline{RXRDY}$ *	O	DMA Receive Ready. Available on the 44-pin version only; shows the status of the 16550A receive FIFO. In the non-FIFO or 16450 mode (bit 0 FCR cleared) or when no DMA is selected (bit 3 FCR cleared), this signal goes active low when there is at least one character in the receive FIFO. It returns inactive high when there are no more characters in the receive FIFO. In the FIFO mode (bit 0 FCR set) and DMA operation (bit 3 FCR set), this signal goes active low as the receive FIFO trigger level is reached or timeout is occurred. $\overline{RXRDY}$ returns to the inactive high level when there are no characters in the receive FIFO.
TXREQ *	O	DMA Transmit Request. Available on the 44-pin version only; shows the status of the 8530 three-byte transmit FIFO. TXREQ goes active high when the transmit FIFO is not full. It goes low when the FIFO is completely full.
RXREQ *	O	DMA Receive Request. Available on the 44-pin version only; shows the status of the 8530 three-byte receive FIFO. RXREQ goes active high when data is available in the receive FIFO. It goes inactive low when the receive FIFO is completely empty.

Main processor 16550A port:

Function and timing of these pins are similar to 16550A.

NAME	TYPE	DESCRIPTION
D0-D7	I/O	Data Bus. This bus provides bi-directional communication between the SPC and the main CPU. In Dual-Processor mode, the 16550A registers are accessed by this bus. In the Single-Processor mode; 16550A registers, Channel A and Channel B registers are accessed by this bus.

PIN DESCRIPTION (Continued)

Main processor 16550A port: (Continued)

Function and timing of these pins are similar to 16550A.

Pins marked by * are not available in 28-pin version (73M1650).

NAME	TYPE	DESCRIPTION
A0-A2	I	Register Select Address. These signals determine the address of the 16550A register to be accessed. Eight registers are selected when DLAB bit (bit 7 of 16550A LCR) is low or upon reset. Two additional registers are accessed when DLAB is set high.
$\overline{CS2}$	I	Chip Select, Main port. When low while $\overline{RD}$ or $\overline{WR}$ are low, allows reading or writing of the registers. In the Dual-Processor mode only the 16550A registers are accessed using this pin. In the Single-Processor mode, 16550A port as well as Channel A and Channel B registers are accessed using this pin.
$\overline{RD}$	I	Read Strobe. When low while $\overline{CS2}$ is low, the contents of the register addressed by A0-A2 or A/$\overline{B}$,D/$\overline{C}$ may be read to the D0-D7 data bus.
$\overline{WR}$	I	Write Strobe. When low while $\overline{CS2}$ is low, the contents of the D0-D7 data bus are written to the register selected by A0-A2 or A/$\overline{B}$,D/$\overline{C}$ on the rising edge of this signal. No change is made to the register which is marked to be READ-ONLY.
INTR	I	Interrupt, High-impedance. This pin goes high whenever attention is requested from the main CPU. Clearing the E1 bit (bit 3 of 16550A MCR), places this pin in a high impedance state, allowing multiple ICs to share one CPU interrupt signal.

Channel A and Channel B in Dual-Processor Configuration:

Pins marked by # have a different function in the **Single-Processor** configuration.

NAME	TYPE	DESCRIPTION
MD0-7 *#	I/O	Data Bus, Local Processor: Allows access to Channel A and Channel B. This bus is controlled by the local processor.
A/$\overline{B}$ *	I	Port Select Address: Controlled by the local processor. When high selects Channel A (USART) to transmit and receive data serially. When low allows access of the local processor to the main port (16550A) registers through Channel B.
D/$\overline{C}$ *	I	Command or Data Select Address: When low, a command register within Channel A or Channel B is selected. Command registers are selected in two cycles: the register address is first written into the lower four bits of command register, and the desired data is subsequently written to the selected command register. When high, the serial transmit/receive data is transferred in one cycle.
$\overline{MCS}$ *#	I	Chip Select, Local Processor: In combination with the MRD and MWR; allows access to Channel A and Channel B registers.

PIN DESCRIPTION (Continued)

Channel A and Channel B In Dual-Processor Configuration: (Continued)

Pins marked by * are not available in 28-pin version (73M1650).

Pins marked by # have a different function in the **Single-Processor** configuration.

NAME	TYPE	DESCRIPTION
$\overline{MRD}$ *#	I	Read Strobe, Local Processor. When low while $\overline{MCS}$ is low, the contents of the selected register in Channel A or Channel B is transferred to the data bus. The serial data register (D/$\overline{C}$ high) can be read in one cycle. When reading the command register (D/$\overline{C}$ low), the command register address is determined by bits 0, 1, 2, 3 of WR0. To read a new command register a write cycle to WR0 to change the register address should be done prior to the read cycle.
$\overline{MWR}$ *#	I	Write Strobe, Local Processor. When low while $\overline{MCS}$ is low, contents of the data bus is written into the selected register in Channel A or Channel B if the register is not marked READ-ONLY. Writing into the serial data register (D/$\overline{C}$ high) can be done in one cycle. When writing the command register (D/$\overline{C}$ low), The command register address is determined by bits 0, 1, 2, 3 of WR0. To write to a new command register, a write cycle to change the register address should be done prior to the write cycle.
$\overline{MINT}$ *#	O	Interrupt, Local Processor. When high, notify the local processor that an access is made by the main CPU to the SPC registers or an interrupt has occurred in the SCC.

Channel A and Channel B In Single-Processor Configuration:

Pins marked by * are not available in 28-pin version (73M1650).

Pins marked by # have a different function in the **Dual-Processor** configuration.

NAME	TYPE	DESCRIPTION
A/$\overline{B}$ *	I	Channel Select Address. When high, selects Channel A (USART) to transmit and receive data serially. When low, allows access to the Main Processor (16550A) registers through Channel B. This signal is only used when the $\overline{MCS}$ is low.
D/$\overline{C}$ *	I	Command or Data Address Select. When low, a command register within Channel A or Channel B is selected. Individual registers are selected in two cycles: The address of the register is first written into the lower four bits of the command register then desired data is subsequently read from or written into the command register. When high, the serial transmit/receive data is transferred in one cycle. This signal is only used when the $\overline{MCS}$ is low.

PIN DESCRIPTION (Continued)

Channel A and Channel B In Single-Processor Configuration: (Continued)

Pins marked by * are not available in 28-pin version (73M1650).

Pins marked by # have a different function in the **Dual-Processor** configuration.

NAME	TYPE	DESCRIPTION
$\overline{MCS}$ *#	I	Chip select, Channel A and Channel B. Access to the SPC registers is controlled by this signal and $\overline{CS2}$. When these signals are not tied together and individually controlled, the last block selected (16550A or Channel A/B) controls the operation of the serial port. When this signal is tied to $\overline{CS2}$, The SPC is put into the Single-Chip-Select (SINGLECS) mode and access to the registers is controlled by two bits in the 16550A IER register (RSEL1, RSEL0). Setting RSEL1 bit enables access to an external device in two cycles.In the SINGLECS mode, new bits are introduced in the Main Processor 16550A registers, allowing additional features.
MALE *#	O	External Device ALE. When in the Single-Chip-Select (SINGLECS) mode and RSEL1 bit is set, this signal is used by the external device to latch the address of its registers. MALE is an inverted version of the WRB signal in the first cycle of an external device access. Data is transferred to the external device in the subsequent cycle using the $\overline{MWR}$ or $\overline{MRD}$ signal. When not in the SINGLECS mode, thispin remains high.
$\overline{MWR}$ *#	O	External Device Write Strobe. When in the Single-Chip-Select (SINGLECS) mode and RSEL1 bit is set, this signal follows the $\overline{WR}$ signal issued by the main processor in the second cycle of an external device access. Data present on the main processor data bus (D0-D7) can be written into the external device. When not in SINGLECS mode, this pin remains high.
$\overline{MRD}$ *#	O	External Device Read Strobe. When in the Single-Chip-Select (SINGLECS) mode and RSEL1 bit is set, this signal follows the $\overline{RD}$ signal issued by the main processor in the second cycle of an external device access. Data can be read from the external device to the main processor data bus (D0-D7). When not in the SINGLECS mode, this pin remains high.
$\overline{MINT}$ *#	I	External Device Interrupt. When in the Single-Chip-Select (SINGLECS) mode, a low level on this pin generates an interrupt to the main processor on the INTR pin if enabled by the software. When not in the SINGLECS mode, this pin is ignored.
$\overline{RTS}$ #	O	Request To Send. This signal shows that a DCE (modem) is ready to send the data. It is controlled by the RTS bit (bit 1 of 16550A MCR or bit 1, Port-A WR8). Setting the RTS bit results in a low level on this pin. Clearing the RTS bit would result in this pin going high immediately when the Auto Enable feature is not active. When the Auto Enable feature is active (bit 5, WR3 set), this pin goes high only after RTS bit is cleared and transmitter register is empty.

PIN DESCRIPTION (Continued)

Channel A and Channel B in Single-Processor Configuration: (Continued)

Pins marked by * are not available in 28-pin version (73M1650).

Pins marked by # have a different function in the **Dual-Processor** configuration.

NAME		TYPE	DESCRIPTION
$\overline{CTS}$	#	I	Clear To Send. This signal is used in DCE (modem) handshaking to show that the DCE has established the communication and data may be transferred to DCE. This input is Schmitt triggered and inverted and its status is reflected in the CTS bit (bit 4 of 16550A MSR and bit 5, Channel A RR0). If the Auto Enable feature is active (bit 5, WR3 set), data is automatically transmitted when this pin is low. If the Auto Enable is not selected this pin can be used as a general purpose input. The DCTS bit (bit 0 of 16550A MSR) is set when a change in the $\overline{CTS}$ logic level is detected, and it can generate an interrupt.
$\overline{DTR}$	#	O	Data Terminal Ready. This signal is used in DCE (modem) handshaking to signify that the SPC is ready to communicate. This pin is a complement of DTR bit (bit 0 of 16550A MCR and bit 7, Channel A WR5). This pin can be used as a general purpose output pin.
$\overline{DSR}$	*#	I	Data Set Ready. This signal is used in the DCE (modem) handshaking to indicate that the DCE is ready to communicate. This input is Schmitt triggered and inverted and its status is reflected in the DSR bit (bit 5 of 16550A MSR or bit 5, of Channel A RR10). This pin can be used as a general purpose input pin. Bit DDSR (bit 1 of 16550A MSR) is set when a change in $\overline{DSR}$ logic level is detected, and it can generate an interrupt.
$\overline{DCD}$	*	I	Data Carrier Detect. A DCE (modem) status input indicates that the DCE has detected the carrier signal on the medium (telephone line). This input is Schmitt triggered and inverted and its status is reflected in the DCD bit (bit 7 of 16550A MSR and bit 3, Channel A RR0). If the Auto Enable feature is active (bit 5, Channel A WR3 set), a low level on $\overline{DCD}$ automatically activates the receiver circuity. When the Auto Enable is not selected this pin can be used as a general purpose input pin. Bit DDCD (bit 3 of 16550A MSR) is set when a change in $\overline{DCD}$ level is detected, and it can generate an interrupt.
$\overline{RI}$	#	I	Ring Indicator. A DCE (modem) status input indicating the presence of ringing voltage on the telephone line. This input is Schmitt triggered and inverted and its status is reflected in the RI bit (bit 6 of 16550A MSR and bit 0, Channel A RR10). This input can be used as a general purpose input pin.The TERI bit (bit 2 of 16550A MSR) is set when a high-to-low transition is detected on this pin, and it can generate an interrupt to the main processor.

REGISTER		ADDRESS A2-A0	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
Receiver Buffer Register (Read only)	RBR	0 DLAB = 0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Transmit Holding Register (Write only)	THR	0 DLAB = 0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Interrupt Enable Register	IER	1 DLAB = 0	Register Select 1 (Single CS)	Register Select 0 (Single CS)	SSi Enable (Single CS)	0	Enable Modem Status	Enable Receiver Status	Enable THRE	Enable RDA
Interrupt ID Register (Read only)	IIR	2	FIFOs Enabled	FIFOs Enabled	RxRDY (SSI Enable)	TxRDY (SSi Enable)	Interrupt ID 2	Interrupt ID 1	Interrupt ID 0	Interrupt Pending
FIFO Control Register (Write only)	FCR	2	RCVR Trigger 1	RCVR Trigger 0	XMIT Trigger 1 (SSi Enable)	XMIT Trigger 0 (SSi Enable)	DMA Mode Select	XMIT FIFO Reset	RCVR FIFO Reset	FIFO Enable
Line Control Register	LCR	3	Divisor Latch Access (DLAB)	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop	Word Length Select 1	Word Length Select 0
Modem Control Register	MCR	4 REGSEL=0	0	0	0	Loop	Enable Interrupt	µPRST	RTS	DTR
Line Status Register	LSR	5 REGSEL=0	Error in Receive FIFO	Transmit Empty	Transmit Holding Empty	Break Interrupt (BI)	Framing Error (FE)	Parity Error (PE)	Overrrun Error (OE)	Data Ready (DR)
Modem Status Register	MSR	6 REGSEL=0	DCD	RI	DSR	CTS	Delta DCD (DDCD)	Trailing Edge RI (TERI)	Delta DSR (DDSR)	Delta CTS (DCTS)
Scratch Register	SCR	7 REGSEL=0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (LS)	DLL	0 DLAB = 1	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (MS)	DLM	1 DLAB = 1	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

FIGURE 4: Main Port 16550A UART Registers

REGISTER		ADDRESS UCR (3:0)	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
UART Command Register (Write only)	UCR	D/$\overline{C}$=0 A/$\overline{B}$=0 ONECS =1: D/$\overline{C}$=0 A3=1 RGSEL0=1	0	0	0	0	Register Select 3	Register Select 2	Register Select 1	Register Select 0
Receiver Buffer Register (Read only)	RBR	8 or D/$\overline{C}$=1 A/$\overline{B}$=0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Transmit Holding Register (Write only)	THR	8 or D/$\overline{C}$=1 A/$\overline{B}$=0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Interrupt Enable Register	IER	1	0	0	0	Enable External INT (SP=1)	Enable MCR/SCR Status	Enable Divisor LCR Status	Enable THRE	Enable RDA/OE
Interrupt ID Register (Read only)	IIR	2	0	0	0	0	0	Interrupt ID 2	Interrupt ID 1	Interrupt ID 0
Line Control Register (Read only)	LCR	3	0	Set Break	Stick Parity	Even Parity	Parity Enable	Number Stop	Word Length Select 1	Word Length Select 0
Modem Control Register (Read only)	MCR	4	0	0	0	Loop	0	0	RTS	DTR
Line Status Register	LSR	5	0	0	Transmit Holding Ready (Read only)	Channel B Tx Transmit Break	Channel B Tx Framing Error	Channel B Tx Parity Error	Channel B Rx Overrun Error (Read only)	Channel B Rx Data Ready (Read only)
Modem Status Register (Read/Write)	MSR	6	DCD	RI	DSR	CTS	0	0	0	0
Scratch Register	SCR	7	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (LS) (Read only)	DLL	9	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch (MS) (Read only)	DLM	A	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Configure Control Register	CCR	B	16550A Parallel Enable (SP=1)	0	0	OSC OFF	Divisor Prescale 3	Divisor Prescale 2	Divisor Prescale 1	Divisor Prescale 0

FIGURE 5: Channel B Registers

REGISTER		ADDRESS WR0 (3:0)	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
Command Register	WR0	0	CRC Reset 1	CRC Reset 1	Command Code 2	Command Code 1	Command Code 0	Register Select 2	Register Select 1	Register Select 0
Tx/Rx Interrupt Data Transfer	WR1	1 (WR only)	0	0	0	Receive Interrupt Mode 1	Receive Interrupt Mode 0	Parity Special	Tx Int Enable	External Interrupt Enable
Interrupt Vector Register	WR2 RR2	2 (RD/WR)	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Receive Control	WR3	3 (WR only)	Rx Bits /Char 1	Rx Bits /Char 0	Auto Enable	Enter Hunt Mode	Rx CRC Enable	Address Search Mode (SDLC)	SYNC Char Load Inhibit	Receiver Enable
Tx/Rx Misc. Modes	WR4 RR4	4 (RD/WR)	Clock Rate 1	Clock Rate 0	SYNC Mode 1	SYNC Mode 0	Stop Bits 1	Stop Bits 0	Even Parity	Parity Enable
Transmit Control	WR5 RR5	5 (RD/WR)	DTR	Tx Bits /Char 1	Tx Bits /Char 0	Send Break	Transmit Enable	SDLC/ $\overline{\text{CRC-16}}$	RTS	Tx CRC Enable
SYNC Char or SDLC Address	WR6 RR6	6 (RD/WR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC Char or SDLC Flag	WR7 RR7	7 (RD/WR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Transmit Buffer Register	WR8	8 D/C=1 A/B=1 (WR only)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Master Interrupt Control	WR9 RR9	9 (RD/WR)	Reset Command 1	Reset Command 0	0	Status High	Master Interrupt Enable (MIE)	0	0	Vector Includes Status
Tx/Rx Misc. Control	WR10	10 (WR only)	CRC Preset	Data Encoding 1	Data Encoding 0	Go Active on Poll	Mark Idle	Abort on Overrun	Loop	6 Bit Sync
Clock Mode Control	WR11 RR11	11 (RD/WR)	Manchester Encode Transmit	Receive Clock Source 1	Receive Clock Source 1	Transmit Clock Source 1	Transmit Clock Source 0	TRxC Pin Output	TRxC Output Source 1	TRxC Output Source 0
Lower Byte Baud Generator	WR12 RR12	12 (RD/WR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Upper Byte Baud Generator	WR13 RR13	13 (AD/WR)	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Misc. Control	WR14 RR14	14 (RD/WR)	PLL Command 2	PLL Command 1	PLL Command 0	Local Loopback	Auto Echo	TX CRC-32	Baud Generator Source	Baud Generator Enable
External /Status Interrupt Control	WR15 RR15	15 (RD/WR)	Break/ Abort Interrupt Control	Tx Underrun /EOM Int. En.	CTS Interrupt Enable	Sync/ Hunt Interrupt Enable	DCD Interrupt Enable	DSR Interrupt Enable	Zero Count Interrupt Enable	RI Interrupt Enable

FIGURE 6: SCC Channel A Write Registers

REGISTER		ADDRESS WR0 (3:0)	DATA BIT NUMBER D7	D6	D5	D4	D3	D2	D1	D0
Tx/Rx Buffer/ External Status	RR0	0	Break/ Abort Detect	Transmit Underrun /EOM	CTS	Hunt	DCD	Transmit Buffer Empty	Zero Count	Receive Char. Available
Special Receive Condition Status	RR1	1	End of Frame (SDLC)	CRC/ Framing Error	Receive Overrun Error	Parity/ CAC-32 Error	Bit Remainder 2	Bit Remainder 1	Bit Remainder 0	All Sent
Interrupt Vector Register	RR2	2	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Interrupt Pending Register	RR3	3	0	0	Channel A Receive Interrupt Pending	Channel A Transmit Interrupt Pending	Channel A Ext/Station Interrupt Pending	Channel B Interrupt ID 2	Channel B Interrupt ID 1	Channel B Interrupt ID 0
Receive Data Register	RR8	8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Misc. Status	RR10	10	One Clock Missing	Two Clocks Missing	DSR	Loop Sending	CRC16	CRC32	On Loop	RI

FIGURE 7: SCC Channel A Read Registers

ADDRESS MAPPING: Single Processor Register Maps In Single-Chip-Select Mode

REGSEL1	REGSEL0	A2	A1	A0	A/$\overline{B}$	D/$\overline{C}$	Addressed Register
0	0	000 - 111			X	X	550 Registers as normal
0	1	0	00 - 11		X	X	550 Registers as normal
0	1	1	X	X	0	0	Channel B Control
0	1	1	X	X	0	1	Channel B Data
0	1	1	X	X	1	0	Channel A Control
0	1	1	X	X	1	1	Channel A Data
1	1	X	X	X	X	X	External Device

FIGURE 8: 40 and 44 Pin Versions

REGSEL1	REGSEL0	A2	A1	A0	A/$\overline{B}$	D/$\overline{C}$	Addressed Register
0	0	000 - 111			-	-	550 Registers as normal
0	1	0	00 - 11		-	-	550 Registers as normal
0	1	1	0	0	-	-	Channel A Data
0	1	1	0	1	-	-	Channel A Control
0	1	1	1	0	-	-	Channel B Data
0	1	1	1	1	-	-	Channel B Control

FIGURE 9: 28 Pin Version (73M1650)

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(TA = -40°C to +85°C, VCC = 5V ±10%, unless otherwise noted.)

PARAMETER		CONDITION	MIN	NOM	MAX	UNITS
VILX	Clock Input Low Voltage		-0.5		0.8	V
VIHX	Clock Input High Voltage		2.0		VCC	V
VIL	Input Low Voltage		-0.5		0.8	V
VIH	Input High Voltage		2.0		VCC+.5	V
VOL	Output Low Voltage	IOL = -5 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = 5 mA (except XOUT)	2.4			V
ICC1	Supply Current	See Note 1		5	10	mA
ICC2	Power Down Current	See Note 2			50	µA
IIL	Input Leakage				±10	µA
IOZ	High-Impedance Leakage				±20	µA

Note 1: Outputs unloaded, CMOS level inputs, Xtal = Data Rate = 10 MHz.

Note 2: Outputs unloaded, CMOS level input, Oscillator disabled or XIN = VCC.

ELECTRICAL CHARACTERISTICS (Continued)

AC CHARACTERISTICS

(TA = -40°C to +85°C, VCC = 5V ±10%, unless otherwise noted.)

PARAMETER		NOTES	MIN	NOM	MAX	UNITS
tASC	Address Setup before Control	1, 2, 3, 4	30			ns
tCAH	Address Hold after Control	1, 2, 3, 4	30			ns
tRD	Read strobe width	3	80			ns
tAD	Address to Read Data	1, 5	150			ns
tCC	Control end to Control start	2	100			ns
tWR	Write strobe width	4	80			ns
tDSW	Data Setup before Write	4, 5	30			ns
tDHW	Data Hold after Write	4, 5	30			ns
tWE	$\overline{WR}$ to External write delay	6 SP = 1	40			ns
tRME	$\overline{RD}$ to External read delay	SP = 1	40			ns
tCD	$\overline{TRXC}$ or $\overline{RTXC}$ to TXD delay	1 x mode			40	ns
fOSC	Crystal/external clock frequency				20	MHz
fDPLL	Input clock for DPLL				20	MHz
fDATA	Data bit rate				10	MHz
fDLOOP	Data bit rate in SDLC Loop				5	MHZ

Note 1: Address includes A0-A2, $\overline{CS2}$, A/$\overline{B}$, D/$\overline{C}$ and $\overline{MCS}$.

Note 2: Control includes $\overline{RD}$, $\overline{WR}$, $\overline{MRD}$ and $\overline{MWR}$.

Note 3: Read Strobe includes $\overline{RD}$ and $\overline{MRD}$.

Note 4: Write strobe includes $\overline{WR}$ and $\overline{MWR}$.

Note 5: Data includes D0-D7 and MD0-MD7.

Note 6: External device write pins are MALE and $\overline{MWR}$ which are derived from $\overline{WR}$.

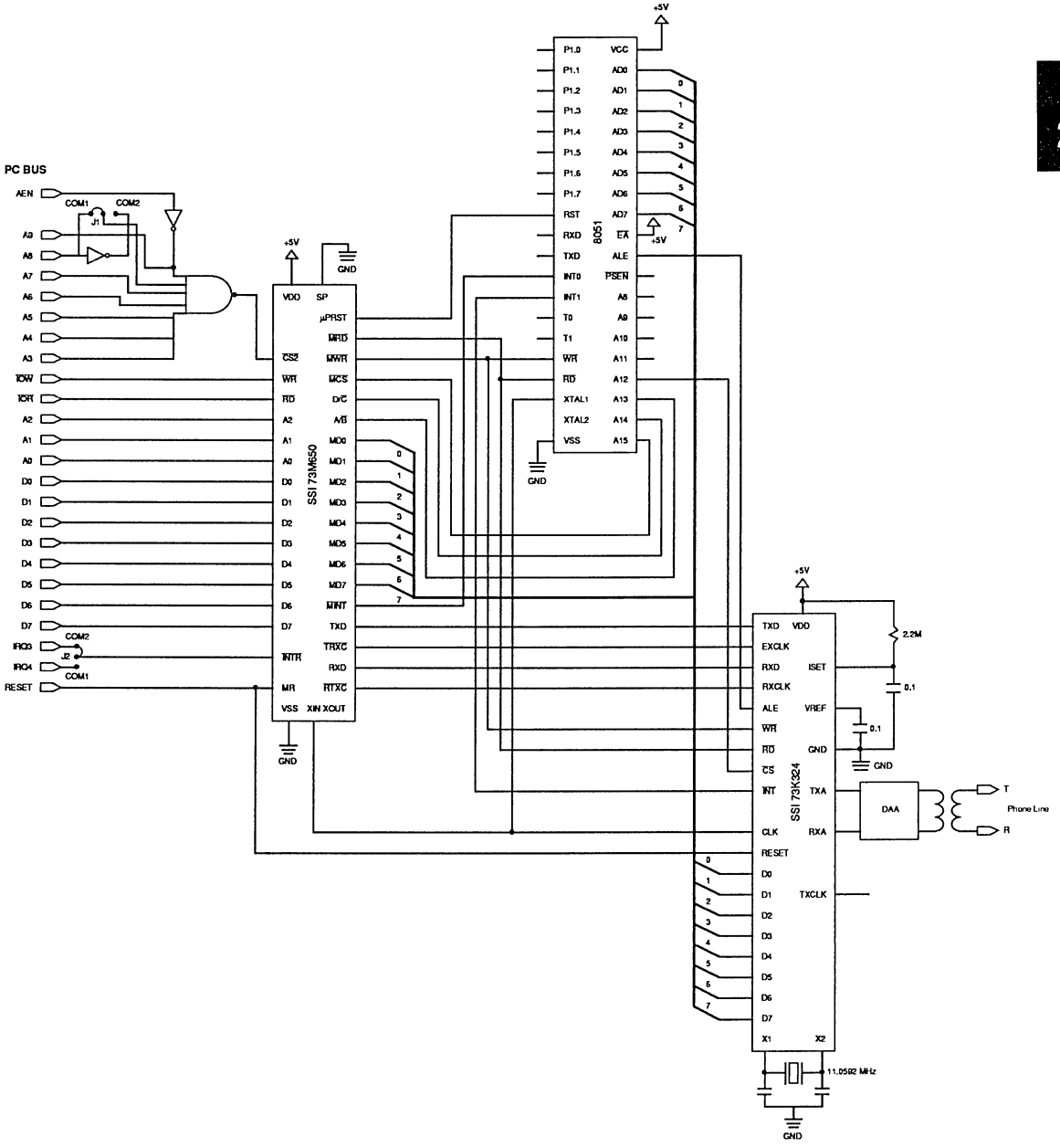


FIGURE 10: Dual-Processor Application Example

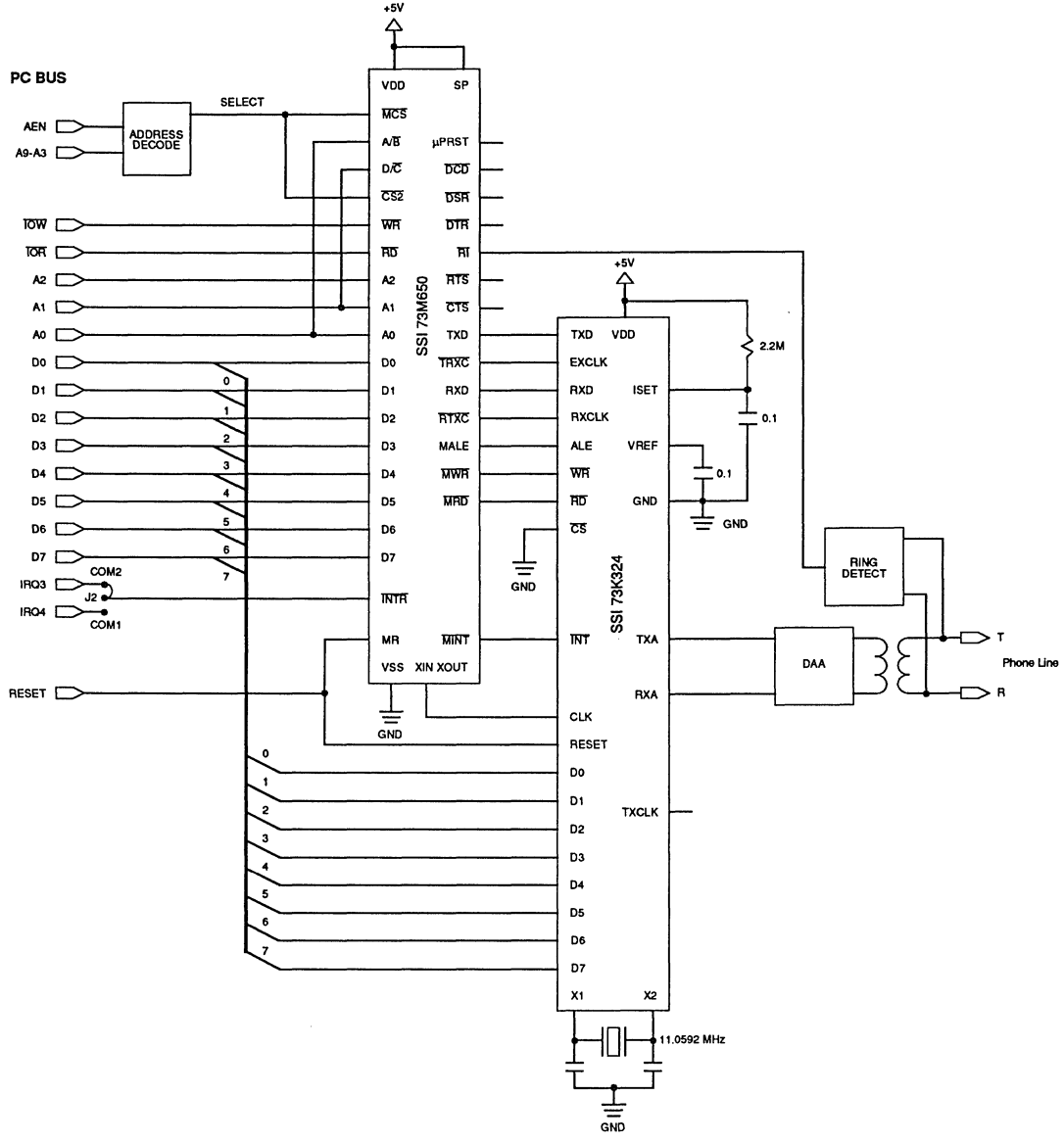


FIGURE 11: Single-Processor Mailbox Mode Application Example

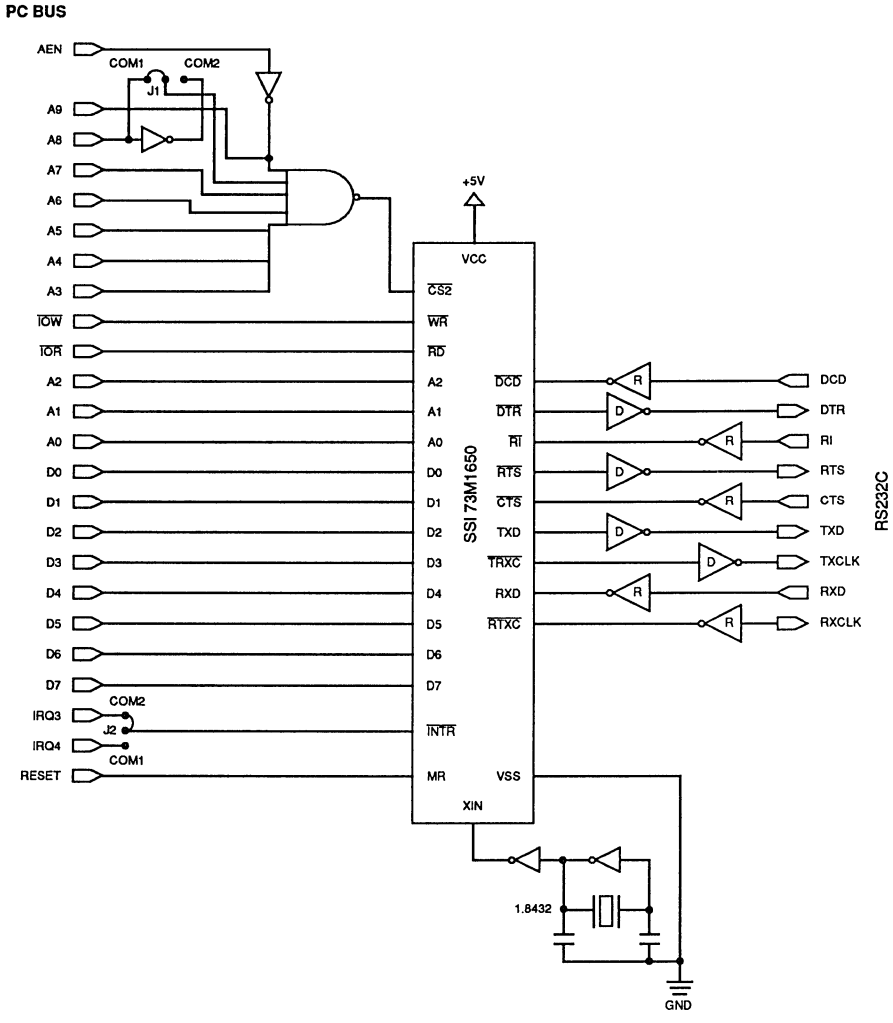
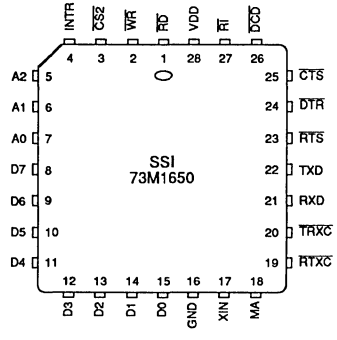


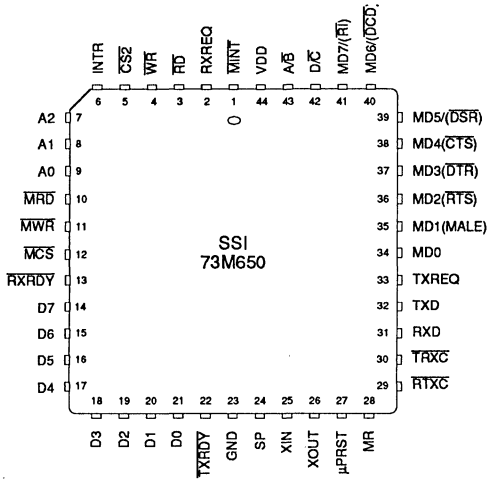
FIGURE 12: Single-Processor Non-Mailbox Mode Application Example

SSI 73M650/1650
Serial Packet Controller

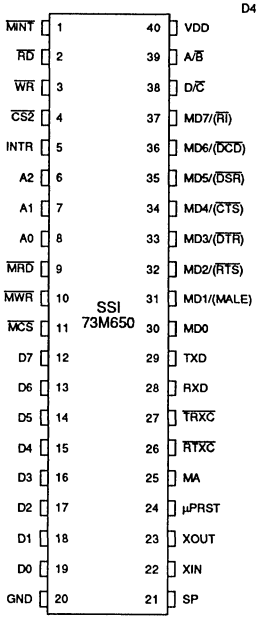
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



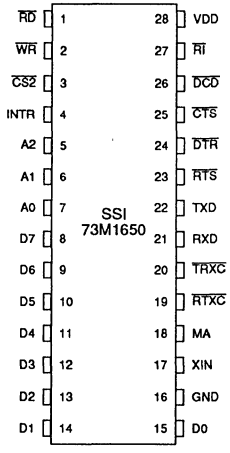
28-pin PLCC



44-pin PLCC



40-pin DIP



28-pin DIP

Serial Packet Controller
Package and Configuration Matrix

	Dual Processor	Single Processor Mailbox	Single Processor Non-mailbox
40/44-pin (73M650)	Yes	Yes	Yes
28-pin (73M1650)	No	Yes	Yes

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Section

SPECIAL MODEM PRODUCTS

3

SSI 73M214
Modem
Analog Front End

June, 1990

DESCRIPTION

The SSI 73M214 is a complete analog front end IC for digital signal processor based V.22bis, V.22, Bell 212A, V.21, and Bell 103 compatible modems.

The 73M214 provides bandsplit filters, compromise equalization, and digitally controlled receive gain and transmit attenuation. An 8-bit A/D convertor is available for receive signal processing, and on-chip modulators provide the QAM, PSK, and FSK transmit signals, making it unnecessary for the DSP to perform the transmit functions. A tone generator is used to produce DTMF, answer, and guard tones while an analog loopback mode allows system testing. Carrier, answer, and call progress tone detection is provided.

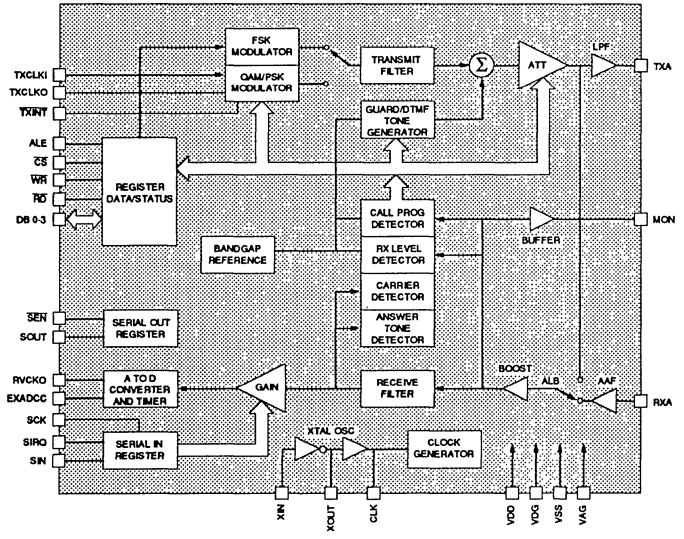
The SSI 73M214 uses two busses to transfer data and control information. A 4-bit address/data multiplexed bus is used for connection to a control microprocessor (8031 typical) which performs the scrambler/descrambler, buffer/debuffer, system control, data, and user interface functions. A serial data bus transfers received digitized data as well as receiver status information to a standard DSP (7720 typical). The DSP also sends the 73M214 receive timing and gain control information over the serial bus. (Continued)

FEATURES

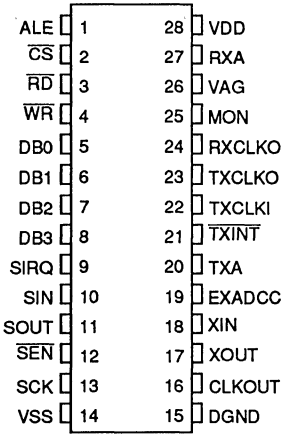
- Analog front end for DSP-based V.22bis modems
- Complete modulators for QAM/DPSK (V.22bis, V.22, Bell 212) and FSK (Bell 103 and V.21)
- Programmable receive gain/transmit attenuation
- 8-bit ADC with reference, sample and hold
- Band split filters with compromise equalization
- Analog loopback test mode
- Serial interface for receive processing
- Parallel interface for transmitter and control
- Timer for transmit synchronization
- Programmable timer for receiver data clock recovery
- Carrier, call progress, and answer tone detectors
- Audio monitor for audible call status
- DTMF, guard tone, and answer tone generation
- Crystal oscillator with output buffer
- Low power CMOS (± 5V at < 250 mW)
- 28-pin plastic DIP or PLCC surface mount package
- Controllable audio monitor

3

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component

DESCRIPTION (Continued)

The SSI 73M214 is ideal for use in self-contained or integral intelligent modem products requiring the benefits of 2400 bit/s full duplex operation while maintaining compatibility with existing standards at speeds down to 300 bit/s. By integrating the majority of the analog functions needed on a single CMOS IC, system complexity and cost is reduced without compromising performance or features.

OPERATION

The SSI 73M214 provides the analog front end processing for a V.22bis/224 2400 bit/s modem. The SSI 73M214 includes band-split filters, fixed U.S. compromise line equalizer, programmable gain/attenuator for receive and transmit functions, FSK/QAM modulators, differential encoder, and an analog to digital converter. The 73M214 interfaces to an external digital signal processor and inexpensive control microprocessor to complete the modem function.

FUNCTIONAL DESCRIPTION

The 73M214 allows selection of 300 bit/s, 600 bit/s, 1200 bit/s, or 2400 bit/s transmission modes. The 73M214 generates the bit rate clocks RVCKO (receive) and TXCKO (transmit) and a baud rate clock $\overline{\text{TXINT}}$. In the synchronous modes, there is a fixed phase relationship between TXCKO and $\overline{\text{TXINT}}$ (refer to figure of Transmit Timing). Each case here assumes that the receive timer is in internal timing mode, otherwise RVCKO is high. Register CR0 selects a mode (there are three synchronous modes and one asynchronous mode). In internal synchronous mode, the SSI 73M214 generates an accurate bit rate clock, TXCKO.This may be used for data transfers from the DTE to the microprocessor. The microprocessor sends the latest quadbit (or dibit), which is latched into the modulator on the falling edge of $\overline{\text{TXINT}}$. Pin TXCKI is ignored in internal synchronous mode. RVCKO is the receiver bit rate clock.

In external synchronous mode the data rate clock from the DTE should be connected to the TXCKI pin. TXCKI is used to generate phase locked clocks TXCKO and $\overline{\text{TXINT}}$ (TXCKI's falling edge synchronously resets an internal counter). RVCKO is the receiver bit rate clock.

RECEIVE PROCESSING

The received signal from the line passes through an anti-alias filter with adjustable gain, then through a band-split filter with selectable compromise line equalization, after which it is amplified by a programmable gain stage. The analog signal is converted to an 8-bit, 2's complement number for the digital signal processor. The ADC output and AGC gain word are transferred serially between the DSP and SSI 73M214. A programmable timer is included for use in the data clock recovery loop. Answer tone, carrier, and imprecise call progress detectors are included for modem smart dialing capability.

TRANSMIT PROCESSING

In QAM (DPSK) mode, the quadbit (dibit) is transfered to the SSI 73M214 where it is differentially encoded and then passed through a baseband filter. The baseband information is modulated up to 1200 Hz or 2400 Hz. A band-split filter shapes the modulator output and provides compromise line equalization. The transmitted spectrum has the recommended square root of 75% raised cosine shaping. Guard tone is added to the signal after the filter, and the programmable attenuator sets the transmit amplitude. Finally, a smoothing filter eliminates out-of-band energy generated by the switched-capacitor filters.

In FSK mode, a programmable tone generator acts as the modulator. The modulator output passes through the band-split and smoothing filters as in the QAM mode.

MICROPROCESSOR INTERFACE

The SSI 73M214 acts as a peripheral to the microprocessor (e.g., Intel 8051, Zilog Z8601, Motorola 6801) on a 4-bit multiplexed address/data bus. Control and status information are stored in registers on the 73M214. Transmit data is also sent from the microprocessor over the bus in 4-bit nibbles.

RECEIVE DSP INTERFACE

The SSI 73M214 interfaces to a digital signal processor over two serial ports.The serial interface is directly compatible with the NEC/OKI 7720 or 77C20. The 73M214 can also be interfaced with parallel bus signal processors using standard LSTTL 7400 series shift registers. The digital sample from the A/D convertor is

sent to the DSP on the serial output port, and the AGC gain value is sent from the DSP to the SSI 73M214 on the serial input port. Both serial ports transfer 16 bits simultaneously under timing control generated by the 73M214.

In slave mode TXCKO and $\overline{\text{TXINT}}$ are phase locked internally to RVCKO (RVCKO's falling edge synchronously resets an internal counter). Pin TXCKI is ignored in slave mode. If the internal receive timer is not being used, slave mode can be implemented by putting the SSI 73M214 in external synchronous mode and externally connecting the recovered receiver bit rate clock to TXCKI.

Asynchronous mode operation is the same as internal synchronous mode, except TXCKO and RVCKO are high.

SERIAL DSP INTERFACE

Serial DSP Interface provides for communication between the DSP and the 73M214. A programmable receive timer block which provides for adjustment of the ADC sampling rate is included on the 73M214. It may be used as part of the data clock recovery loop. The receive timer control bits RvT1 and RvT0 (TR0) select one of four possible ADC modes; off, external timing, internal timing 7200 Hz, or internal timing 9600 Hz. The DSP through serial port SIN (bits 8-9) provides for adjustment to the internal sampling clock rates either 7200 Hz ± 1 µs or 9600 Hz ± 1 µs. The falling edge of $\overline{\text{SEN}}$ corresponds to the following events:

1) The signal on RXA is sampled and an 8-bit analog-to-digital conversion begins.
2) The previous 8-bit ADC sample and the status bits are loaded into a register for serial shifting out of port SOUT to the DSP.
3) The previous gain & timer bits from the DSP are latched into the 214 register and the current DSP serial word is shifted into port SIN.

Serial Output- 16-bit word - bit 0 (LSB) is shifted out first.

BIT #	15 - 12	11	10	9	8	7 - 0
Output Data	Fast C.D.	Slow C.D.	A.T.	CPD	RCV Level	ADC Output

Serial input - 10 bits - bit 0 (LSB) is shifted first.

Bit #	15 - 10	9 - 8	7	6 - 0
Input Data	X	RCV Timer Control	X	Gain Word (Log) MSB-LSB

SERIAL DSP TIMING

The timing diagram for the serial receive processor interface is shown in Figure 3. Signal SIRQ is generated by the NEC/OKI 77C20 and must be high to send SIN data. If it is low during a serial transmission, SOUT remains active but SIN becomes inactive and the 73M214 will continue to use the last gain/timer value. SCK from the 73M214 is the serial shift clock.

QAM/DPSK ENCODER/MODULATOR

The quadbits sent to the 73M214 are differentially encoded according to the CCITT V.22bis specification. The encoded quadbits are then passed through an FIR baseband filter. The baseband signal thus generated is modulated by the carrier at either 1.2 kHz or 2.4 kHz.

FSK MODULATOR

The FSK modulator frequency modulates the data in a continuous phase manner. FSK operation is asynchronous and is determined by the control bits shown:

REGISTER	D3	D2	D1	DCR
CR0	1	1	x	x
CR1	0/1	x	x	1
CR3	0	0	x	0/1
TR0	x	x	1	0
TR1	1/0	1/0	1/0	1/0

TONE GENERATOR

The tone generator will output a dual-tone (DTMF) or a single tone (FSK, answer tone, or guard tone) on the TXA line if the appropriate control bits are enabled. The control bits are found in register TR0 and TR1. The tone is specified by register TR1 - 16 dual-tone combinations and 7 single tones are possible. DTMF has priority over single tones. The tone generator consists of 4 blocks: tone selection and control, two programmable down counters, two three-level six-step square wave generators, and a 3-pole ladder filter with programmable gain and pole setting.

BAND SPLIT FILTERS

The band-split filters provide attenuation for out-of-band noise components and near-end cross talk. The filters also provide some of the root 75% raised cosine shaping for minimum intersymbol interference. Transmit and Receive delay equalization can be bypassed by using the TxEQ and RvF1 bits. The receive filter can be bypassed for direct access to the ADC with the RvF0 bit.

PROGRAMMABLE GAIN STAGE

The programmable gain stage is part of an AGC loop which is controlled by the receive digital signal processor. The gain increased monotonically with increasing gain word. The 7-bit gain setting covers a 48 dB range with 0.375 dB steps. Minimum gain of 0 dB corresponds to 0000000, maximum gain of 48 dB is 1111111.

ADC

The 8-bit analog to digital converter provides a 2's complement representation of the sampled analog voltage. The sample and hold function is incorporated in this switched-capacitor ADC.

TRANSMIT ATTENUATOR

The programmable transmit attenuator allows the control processor to set the transmit power level. If the attenuator control bits are set to 0000, the attenuator acts as a unity gain stage. The attenuation increments by 1 dB per bit.

In addition to the user programmable attenuator, there is an internally controlled attenuator for the QAM/DPSK modulated signal. The attenuation value is determined by the guard tone selected and assures that modulated data plus guardtone gives 0 dBm prior to the transmit attenuator regardless of the guard tone setting.

DETECTORS

The special detect circuitry checks the received analog signal for special conditions. The conditions checked for are the presence of a carrier (i.e., energy in the receive band), the presence of an answer tone (2100 or 2225 Hz), and the presence of a call progress signal.

IMPRECISE CALL PROGRESS DETECTOR

The call progress detector monitors activity on the line. This detector is an imprecise call progress detector- the on/off envelope of the signal is replicated as a 1/0 in the CPD bit of the SR register. The detector consists of a bandpass filter followed by a peak detector. The 3 dB points of the bandpass filter are 350 Hz and 620 Hz. Dial-tone, busy-signal, ringback and reorder are composed of at least one tone in this band.

PRECISE ANSWER TONE DETECTOR

The receive filter output is fed to a highly selective frequency discriminator controlled by the ABT1 and ABT0 bits of the DCR register to detect 2100 and 2225 Hz answer back tones. The frequency discriminator is gated by the output of the carrier detector to provide amplitude discrimination.

CARRIER DETECTOR

The carrier detector detects the presence of a signal in the receive band. When energy is detected the CAR bit of the SR register is set to "1." The detector uses a peak-to-peak amplitude detecting scheme which requires knowledge of the Peak/Rms ratio of the waveform to be detected. This information is obtained from the data rate control register (CR0) bits DR1 and DR0.

DR1	DR0	Carrier Type	Peak/Rms
0	0	None	1.414
0	1	FSK	1.414
1	0	DPSK	2.0
1	1	QAM	2.5

The fast carrier detect is an imprecise carrier detector that is derived from the short term peak-to-peak amplitude in the carrier detector. The detector output will be erratic for small signals with high peak-to-rms values. The fast carrier is output on the FCAR bit of the serial output port.

RECEIVE LEVEL DETECTOR

The receive level detector indicates whether the signal present at RXA is too large to permit the use of the receive gain (RvGE) of 12 dB prior to the band-split filters. When the RvL bit of the SR register - "1," the signal is too large to use the gain.

A fixed, switchable 12 dB gain is provided ahead of the band-split filters to be used when the total received signal (received signal + near-end signal) is more than 12 dB below the maximum allowed input voltage.

OUTPUT SMOOTHING FILTER

The output smoothing filter attenuates out-of-band frequency components that are generated by the switched capacitor filters on the chip.

INPUT ANTI-ALIAS LOW PASS FILTER

The anti-alias low pass filter prevents aliasing of incoming frequency components into the passband of interest.

PIN DESCRIPTION

POWER

NAME	PIN NO.	I/O	DESCRIPTION
VDD	28	I	Positive voltage supply (+5V)
VSS	14	I	Negative voltage supply (-5V)
VAG	26	I	Analog Ground
VDG	15	I	Digital Ground

ANALOG INTERFACE

NAME	PIN NO.	I/O	DESCRIPTION
RXA	27	I	Receive analog input from line.
TXA	20	O	Transmit analog output to line. Modulator output as well as DTMF output uses this pin.
XIN	18	I	Crystal connection, 7.3728 MHz crystal, or externally generated 7.3728 MHz oscillator input.
XOUT	17	O	Crystal connection, 7.3728 MHz crystal.
CLKOUT	16	O	Crystal oscillator output echoed for system use.
MONITOR	25	O	Analog output for call progress tone monitoring. Can be muted (see Control Bits).

MICROPROCESSOR INTERFACE

NAME	PIN NO.	I/O	DESCRIPTION
DB0-DB3	5,6,7,8	I/O	(Bi-directional, 3 state) Address/Data Bus.
$\overline{CS}$	2	I	Chip Select. A low allows a read or write cycle to occur. DB0-DB3 can not be written to or read from if $\overline{CS}$ (latched) is not low. $\overline{CS}$ is latched on the falling edge of ALE.
$\overline{RD}$	3	I	Read. A low requests a read of the 73M214 registers. Data cannot be ouput on DB0-DB3 unless both $\overline{RD}$ and the latched $\overline{CS}$ are low.
$\overline{WR}$	4	I	Write. A low informs the 73M214 that data is available on DB0-DB3 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$ - no data is written unless both $\overline{WR}$ and $\overline{CS}$ are low.
ALE	1	I	Address strobe line for multiplexed addressed/data bus. The falling edge of ALE latches the address on DB0-DB3 and the chip select $\overline{CS}$.

TRANSMIT INTERFACE

NAME	PIN NO.	I/O	DESCRIPTION
TXCKI	22	I	Transmit clock input, used for the external synchronous mode. In external synchronous mode, all clocks for the modulator are synchronized to this bit rate clock.
TXCKO	23	O	Bit rate transmit clock output, provided when the modulator is in a synchronous mode. In FSK, or modulator off modes, this pin is pulled high.
$\overline{\text{TXINT}}$	21	O	Transmit interrupt, active low. Baud rate clock which requests a new quadbit for the modulator. Active in the 1200 or 2400 bit/s modes only. Forced high otherwise.

RECEIVE INTERFACE

NAME	PIN NO.	I/O	DESCRIPTION
RVCKO	24	O	Bit rate receive clock output from receive timer. Output is active in 2400 or 1200 bit/s transmission when the internal timer is used and the modulator is operating in a synchronous mode. Otherwise the output is forced high.
SOUT	11	O	Output serial port - sends ADC/status bits to DSP.
SIN	10	I	Input serial port receive gain and timer bits from DSP.
SIRQ	9	I	Serial input request. SIRQ high signifies that data is available to shift into SIN port - SIRQ low causes SIN port to retain past data and not shift. SIRQ is latched by $\overline{\text{SEN}}$ falling edge. SIRQ does not affect the shifting of the SOUT port.
$\overline{\text{SEN}}$	12	O	Serial enable pin. Enables serial shifting on SOUT and SIN ports. Signal is low for 16 cycles of SCK.
SCK	13	O	Shift clock generated on 73M214 for serial ports SIN and SOUT. Clock rate is 184 kHz and is resychronized to receive timer every $\overline{\text{SEN}}$ falling edge.
EXADCC	19	I	External ADC convert clock input which is required if the internal receive timer is not being used. The rising edge of EXADCC is aligned to an internal 922 kHz clock; it starts an ADC conversion and serial shifting over the SIN and SOUT ports.

REGISTER ADDRESSES

The signals A0, A1, A2, and A3 (DB0-DB3 latched by ALE) are used to address the on chip registers.

FUNCTION	REGISTER	D3	D2	D1	D0	A3-A0
Transmit Control Register	CR0	DR1	DR0	TxM1	TxM0	0000
Interface Control Register	CR1	FBK	RvF1	RvF0	$\overline{\text{TxSQ}}$	0001
Attentuation Control Register	CR2	ATT3	ATT2	ATT1	ATT0	0010
Set-up Control Register	CR3	TST	ALB	RvGE	ORIG	0011
Detect Control Register	DCR	ABT1	ABT0	MONEN	RST	0100
Status Register	SR	CAR	ATD	CPD	RvL	0101
Transmit Tone Control Reg. 0	TR0	RvT1	RvT0	ST	DTMF	0110
Transmit Tone Control Reg. 1	TR1	TRB3	TRB2	TRB1	TRB0	0111
Quadbit Register-QAM/DPSK	QBR	QB3	QB2	QB1	QB0	1000

REGISTER BIT DESCRIPTION

TRANSMIT CONTROL REGISTER				
	D3	D2	D1	D0
CR0	DR1	DR0	TXM1	TXM0

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D1	Transmit Modes (TXM0, TXM1)	D1 D0 0 0	Asynchronous mode: Modulator clocks are derived from crystal. The 73K214 operates in the internal synchronous mode as described below. TXCKO and RVCKO are high in asynchronous mode.
		0 1	Internal synchronous mode: Modulator clocks are derived from crystal. The SSI 73M214 generates an accurate bit rate clock, TXCKO. This may be used for data transfers from the DTE to the microprocessor. The microprocessor scrambles the data and sends the latest quadbit or (dibit) to the modulator as requested by the baud rate clock TXINT. The TXCKI pin is ignored in the internal synchronous mode. If the receive timer is enabled, RVCKO is a bit rate clock. If the receive timer is disabled, RVCKO is high.
		1 0	External synchronous mode: Modulator clocks are synchronized to signal on TXCKI pin. The data rate clock from the DTE should be connected to the TXCKI pin. This clock is internally synchronized to a high speed clock. The synchronized signal is echoed on pin TXCKO and used to generate the quadbit interrupt signal TXINT. RVCKO is as described above.
		1 1	Slave mode: Modulator clocks are synchronized to RVCKO signal. In slave mode with the receive timer enable, RVCKO signal is internally routed to TXCKI. If the receive timer is not being used, slave mode can be implemented by putting the SSI 73K214 in external mode and connecting the recovered bit rate clock to TXCKI.

REGISTER BIT DESCRIPTION (continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D2, D3	Data Rates	D3 D2 0 0	Modulator off: With the modulator off, carrier detect defaults to FSK settings, and the modular output is effectively shortened to ground.
		0 1	Select FSK operating mode. The FSK modulation is performed by programming the tone generator output frequency. Operation is asynchronous, and the transmission mode control bits (CR0 - TXM1, TXM0) are ignored in FSK mode. TXCKO and RVCKO are high.
		1 0	Select DPSK operating mode at 1200 bit/s.
		1 1	Select QAM operating mode at 2400 bit/s.

INTERFACE CONTROL REGISTER				
	D3	D2	D1	D0
CR1	FBK	RvF1	RvF0	$\overline{\text{TxSQ}}$

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Tx squelch ($\overline{\text{TxSQ}}$)	0	Disables transmit output at TXA. Forces TXA output to ground.
		1	Enables transmit output at TXA.
D1	Receive Filter (RvF0)	0	Select normal mode.
		1	Bypass receive filter to allow direct access to ADC.
D2	Receive Filter Equalizer (RvF1)	0	Select normal mode.
		1	Bypass Receive filter delay equalizer.
D3 (FBK)	Fallback		Selects low speed options. (See Table 1.)

REGISTER BIT DESCRIPTION (continued)

Table 1: Rate/Mode Selections

Register bits CR0 - DR1, DR0, TXM1, TXM0 and CR1 - FBK control the data clocks and modular mode. To enable DPSK/QAM modulation, FSK and Answer tones must be disabled. This table assumes the receive timer to be in internal timer mode (if not RVCKO is high) - see register TR0 - RVT1, RVT0.

CR1	CR0				MODULATOR MODE	DATA CLOCKS		
FBK	DR1	DR0	TXM1	TXM0		TXCKO	$\overline{\text{TXINT}}$	RVCKO[1]
x	0	0	0	0	off	1	1	1
x	0	0	0	1	off	1200 Hz	1	1200 Hz
x	0	0	1	0	off	TsCKI	1	1200 Hz
x	0	0	1	1	off	RVCKO	1	1200 Hz
0	0	1	X	X	FSK(103)	1	1	1
1	0	1	X	X	FSK(V.21)	1	1	1
0	1	0	0	0	DPSK	1	600 Hz	1
0	1	0	0	1	DPSK	1200 Hz	600 Hz	1200 Hz
0	1	0	1	0	DPSK	RXCKI	600 Hz	1200 Hz
0	1	0	1	1	DPSK	RVCKO	600 Hz	1200 Hz
1	1	0	0	0	DPSK	1	600 Hz	1
1	1	0	0	1	DPSK	600 Hz	600 Hz	600 Hz
1	1	0	1	0	DPSK	TXCKI	600 Hz	600 Hz
1	1	0	1	1	DPSK	RVCKO	600 Hz	600 Hz
x	1	1	0	0	QAM	1	600 Hz	1
x	1	1	0	1	QAM	2400 Hz	600 Hz	2400 Hz
x	1	1	1	0	QAM	TXCKI	600 Hz	2400 Hz
x	1	1	1	1	QAM	RVCKO	600 Hz	2400 Hz

[1]RVCKO pin is high if receive timer is not in internal mode-register bits TR0; D3, D2.

ATTENUATION CONTROL REGISTER				
	D3	D2	D1	D0
CR2	ATT3	ATT2	ATT1	ATT0

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D1, D2, D3	Transmit Attenuator	D3, D2, D1, D0 0000 to 1111	Sets transmit attenuator which scales modulated data (and guard tone if enabled). Attenuation increments by 1 dB per LSB ATT = 0000 is unity gain, ATT = 1111 is 15 dB of Attenuation.

SET-UP CONTROL REGISTER				
	D3	D2	D1	D0
CR3	TST	ALB	RvGE	ORIG

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Originate/Answer	0	Select answer mode. Answer mode set transmit path for high band modulation and filtering and connects the low band filter on the receive side.
		1	Select originate mode. Originate mode sets the transmit path for low band modulation and filtering connects the high band filter on the receive side.
D1	Receive filter gain (RvGE)	0	Receive path gain = 0 dB
		1	Adds 12 dB of gain in the receive path prior to the band-split filter to enhance dynamic range. Care must be taken to ensure that the level at RXA does not exceed - 12 dBm when RvGE is enabled. The status bit RvL indicates the signal level at the receive band-split filter input. If RvL is low, the Receive filter gain can be safely enabled.
D2	Analog Loopback (ALB)	0	Select normal mode.
		1	Select analog loopback mode. A '1' causes the modulated data to pass through the transmit band-split filter (magnitude & delay section), through the attenuator, through transmit smoothing filter, into the receive anti-alias filter, bypassing the receive band-split filter (magnitude and delay), through the gain stage, into the ADC. The RXA input is floated, and the TXA is grounded. Detectors are active.
D3	Test (TST)	0	Select normal mode.
		1	Silicon Systems test mode. Not for customer use.

DETECT CONTROL REGISTER				
	D3	D2	D1	D0
DCR	ABT1	ABT0	MONEN	RST

The Detect Control Register holds the control for the Special Detect circuits and some miscellaneous functions.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Reset (RST)	0	Normal mode.
		1	Resets all Registers to the 0 state.
D1	Monitor Enable (MONEN)	0	Monitor output disabled.
		1	Enables echoing of the RXA signal on the MON pin.
D2, D3	Answer Back Select (ABT0, ABT1)	D3, D2	Selects which answer back tone or combination of tones will cause the Answer Tone status bit (ATD) to go high, as shown
		00/11	Detect broadband from 2100 to 2225 Hz
		01	Detect only 2225 Hz
		10	Detect only 2100 Hz

STATUS REGISTER				
	D3	D2	D1	D0
SR	CAR	ATD	CPD	RvL

The Status Register holds the special detect circuit outputs and are read-only. These status bits and a "fast" carrier detect bit are sent out on the serial interface.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Receive level indicator (RvL)	0	Signal peak amplitude is small enough to safely allow 12 dB pre-filter gain to be switched in.
		1	Signal amplitude is too large to allow the 12dB gain.
D1	Call progress detect (CPD)	0	No call progress detected.
		1	Energy in call progress band present.
D2	Answer tone detect (ATD)	0	No answer tone detected.
		1	Valid answer back tone present.
D3	Carrier Detect (CAR)	0	No energy in receive band detected.
		1	Valid carrier present.

TRANSMIT TONE CONTROL REGISTER 0				
	D3	D2	D1	D0
TR0	RvT1	RvT0	ST	DTMF

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF enable (DTMF)	0	Disables DTMF.
		1	Activates DTMF. Selects dual tones. Output level is to be 0 dBm when attenuator setting is 0000. All detectors will be operating and should be ignored during DTMF. The tone pairs are determined by TR1 contents.
D1	Single tone enable (ST)	0	Disables single tone transmit.
		1	Selects single tones (FSK, Guard, or Answer). The tone frequency is determined by the bits in register TR1.
D2, D3	Receiver Timer (RvT0, RvT1)	D3, D2	The receive timer (RvT1, RvT0) selects one of four possible sampling rates: off, external timing, internal 7200 Hz, or internal 9600 Hz. The rising edge of an internal sampling clock initiates an analog-to-digital conversion and data transfer to the DSP. In the two internal modes, the sampling clock is generated by an on chip counter which can be controlled by bits 8 and 9 of the serial input word.
		00	$\overline{SEN}$ is forced high. This state can be used for initializing the serial interface to the NEC 7720. ADC is stopped.
		01	External timer EXADCC (synchronized internally) is the sampling clock.
		10	Internal timer, 7200 Hz sampling rate
		11	Internal timer, 9600 Hz sampling rate

TRANSMIT TONE CONTROL REGISTER 1				
	D3	D2	D1	D0
TR1	TRB3	TRB2	TRB1	TRB0

BIT NO.	NAME	CONDITION	DESCRIPTION
D0 to D3	DTMF Mode (TR0 - DTMF = 1)	0000 to 1111	Programs 1 of 16 DTMF tone pairs that will be transmitted when DTMF (TR0) bit is set. Tone Encoding is shown below.

Keyboard Equivalent	Register TR1 D3	D2	D1	DO	Tones (Hz) Low	High
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1209
6	0	1	1	0	770	1477
7	0	1	1	1	852	1336
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

D0 to D3	Single Tone Mode (TR0 - ST = 1)	0000 to 1111	Programs 1 of 11 single tones that will be transmitted when ST (TR0) bit is set. Tone encoding is shown below.

Tone-Type	Register TR1 D3	D2	D1	D0	Tones (Hz)
FSK 103	0	0	0	0	2025
FSK 103	0	0	0	1	2225
FSK 103	0	0	1	0	1070
FSK 103	0	0	1	1	1270
FSK V.21	1	1	0	0	1850
FSK V.21	1	1	0	1	1650
FSK V.21	1	1	1	0	1180
FSK V.21	1	1	1	1	980
Guard	0	1	0	0	1800
Guard	0	1	0	0	550
Answer	1	0	0	0	2225
Answer	1	0	0	1	2100

QUADBIT REGISTER				
	D3	D2	D1	D0
QBR	QB3	QB2	QB1	QB0

The new quadbit for the QAM modulator is written to this register by the transmit microprocessor for every baud. Quadbits are latched into the modulator on the falling edge of TXINT. In 1200 bit/s mode, QB1 is internally forced to 0 and QB0 is forced to 1 so that only a dibit need be written in QB3, QB2. In 600 bit/s mode, QB1, QB0 are forced to 01, and QB3 is duplicated in QB2 so that only one bit need be written in QB3.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D1	Quadbits (QB0, QB1)	D1, D0	The last two quadbits which determine the point within the quadrant in QAM. Forced to 01 in DPSK. Point in quadrant (I)
		0 0	(1,1)
		0 1	(3,1) [DPSK points]
		1 0	(1,3)
		1 1	(3,3)
D2, D3	Quadbits (QB2, QB3)	D3, D2	The first two quadbits as described in the V.22bis spec. (these bits determine the differential quadrant shift). Used as Dibit in DPSK Quadrant shift (I)
		0 0	+90°
		0 1	0°
		1 0	+180°
		1 1	+270°

SERIAL INTERFACE DESCRIPTION

BIT NO.	0 1 2 3 4 5 6	7	8 9	10	11	12	13	14	15
INPUT DATA	LSB ←GAIN WORD→ MSB	X	RCV TIMER CONTROL	X	X	X	X	X	X

BITS	NAME	CONDITION	DESCRIPTION
0-6	GAIN WORD	0000000-1111111	Receive Gain from DSP for programmable Receive Gain stage. Step size is approximately 0.375 dB/bit with 48 dB of range. Transmitted LSB first.

SERIAL INTERFACE DESCRIPTION (continued)

BITS	NAME	CONDITION	DESCRIPTION
7	NONE	X	Not used
8,9	REC. TIMER CONTROL (internal modes only)	8,9	Used for timer control & correction of timing errors in the time base, $\overline{SEN}$, for start of ADC conversion. Sample rate is selected by TR0-RVT1, RVT0. Used only with internal modes.
		0,0	7200 Hz (or 9600 Hz)
		1,1	7200 Hz (or 9600 Hz)
		1,0	7200 Hz - 1 µs (or 9600 Hz - 1 µs)
		0,1	7200 Hz + 1 µs (or 9600 Hz + 1 µs)
10 - 15	NONE	XXXXXX	Not used

BIT NO.	0 1 2 3 4 5 6 7	8	9	10	11	12 13 14 15
OUTPUT DATA	LSB ← ADC 2's → MSB Complement output	RVL	CPD	AT	Slow CD	Fast CD

BITS	NAME	CONDITIONS	DESCRIPTIONS
0-7	ADC OUTPUT	00000000-11111111	2's Complement coded output from 8-bit ADC ±3.75V F.S.
8	RVL (same as SR-RVL)	0	Receive level amplitude is small enough to allow 12 dB pre-filter gain to be used.
		1	Receive level too large for 12 dB gain to be used.
9	CPD (same as Sr-CPD)	0	No call progress energy detected
		1	Call progress energy detected
10	AT (same as SR-ATD)	0	No answer tone detected
		1	Answer tone detected
11	SLOW CD (same as SR-CAR)	0	No carrier detected
		1	Time qualified carrier detected
12 - 15	Fast CD	0	No carrier detected
		1	Carrier detected

ABSOLUTE MAXIMUM RATINGS - Operation above maximum ratings may damage the device

PARAMETER	RATING	UNITS
Supply Voltage VDD	+7.5	V
VSS	-7.5	V
Storage Temperature	-65 to 150	°C
Lead Temperature (10 sec.)	260	°C
Inputs	VSS -0.3 to VDD +0.3	V
TTL Compatible Outputs	-0.3 to VDD +0.3	V
TTL Compatible Outputs	±3	mA
Analog Outputs	VSS -0.3 to VDD +0.3	V
Analog Outputs	±3	mA

Notes: 1. All inputs and outputs are protected from static charge using built-in industry standard protection devices.

2. All outputs are short-circuit protected.

3. All voltages are referenced to GND.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNITS
Positive Supply (VDD)	4.75		5.25	V
Negative Supply (VSS)	-4.75		-5.25	V
Ambient Temperature (TA)	0		70	°C
External Components VDD, VSS Bypass Capacitors (External to ground (VAG))	0.1			µF
External Loads				
Load Capacitance XIN, XOUT	10		50	pF
Load Capacitance CLKOUT			25	pF
Digital Input Capacitance			10	pF
Digital Output Loading			50	pF
Analog Input Capacitance RXA			26	pF
Analog Input Resistance RXA	100			kΩ
Analog Loading, TXA Output (Vout = ±3Vpk)			10k, 50 pF	
Analog Loading, MON Output (Vout = ±3Vpk)			10k, 50 pF	
On-chip pull up/down Resistor pull down: $\overline{CS}$, pull up: TXC KI, EXADCC	20			kΩ
Input Clock variation (7.3728 MHz Input XTAL)	-0.01		+0.01	%

DC ELECTRICAL CHARACTERISTICS

(TA = 0 to 70°C, VDD = 5V, VSS = -5V Unless otherwise noted)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current (IDD)				25	mA
(ISS)				25	mA
Input Low voltage (VIL)				0.8	V
Input High Voltage (VIH)		2.0			V
Input High Current (IIH)	Input voltage = VDD			10	µA
Input Low Current (IIL)	Input Voltage = 0V			-20	µA
High Output Voltage (VOH)	Iout = -0.4 mA	2.4			V
Low Output Voltage (VOL)	Iout = 1.6 mA			0.4	V

DYNAMIC CHARACTERISTICS AND TIMING[1]

(TA = 0 to 70°C. VDD = 5V, VSS = -5V Unless otherwise noted)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Receive Signal Path					
Receive Gain	RvGE = 0 Gain word 0000000 Measured at input of ADC		0.0		dB
Receive Noise	RXA = 0 Boost 0dB Gain word 0000000 0.3 to 3400 kHz bandwidth			775	µVrms
Receive Boost	RvGE = 0	-0.2		0.2	dB
Receive Boost	RvGE = 1	11.8		12.2	dB
Programmable Gain Stage					
Gain Range		0.0		48.0	dB
Step Size		0.275	0.375	0.475	dB
Gain Error				0.2	dB
ADC					
Integral non-linearity				1/2	LSB
Differential non-linearity				1/2	LSB
Total input referred offset		-4		+4	LSB
Input voltage range		-3.75		+3.75	V
Input Anti-alias Low Pass Filter					
Receive Attenuation					
@ 4.0 kHz			-35		dB
@ 10.0 kHz			-60		dB
@ 12.0 kHz			-70		dB
@ 153.6 kHz			-55		dB
@ 921.6 kHz			-40		dB

1) All dBm numbers refer to the signal power on the 2-wire telephone line as may be realized thru an external 2W/4W converter (hybrid). The hybrid gain from the line to the RXA pin should be 0 dB.

DYNAMIC CHARACTERISTICS AND TIMING[1] (continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Precise Answer Tone Detector					
Must Detect Level				-43	dBm
Must Reject Level		-48			dBm
Delay Time		40		200	ms
Hold Time		40		100	ms
Answer Tone Detect					
Frequency Range					
Must Accept	2100 Hz to 2225 Hz	2078		2247	Hz
Must Reject Low	Mode Selected			2000	Hz
Must Reject High	(ABT1, ABT0 = 00 or 11)	2350			Hz
Must Accept	2100 Hz only	2078		2122	Hz
Must Reject Low	Mode Selected			2000	Hz
Must Reject High	(ABT1, ABT0 = 01)	2200			Hz
Must Accept	2225 Hz only	2203		2247	Hz
Must Reject Low	Mode Selected	2350			Hz
Must Reject High	(ABT1, ABT0 = 01)			2125	Hz
Fast Carrier Detector	The following detect levels assume a waveform of the type shown is present in the receive band.				
Must Detect	See Condition Table Below			-43	dBm
Must Reject Level		-48			dBm
Delay Time		0		20	ms
Hold Time		0		20	ms
Slow Carrier Detector	The following detect levels assume a waveform of the type shown is present in the receive band.				
Must Detect Level	See Condition Table Below			-43	dBm
Must Reject Level		-48			dBm
Hysteresis		2			dB
Delay Time		40		205	ms
Hold Time		40		65	ms

CONDITION TABLE

DR1	DR0	CARRIER TYPE	PEAK/RMS
0	0	None[2]	1.414
0	1	FSK	1.414
1	0	DPSK	2.0
1	1	QAM	2.5

2) When the modulator is off, the carrier detector responds to sinusoids as might be found in answer back type tones.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Receive Signal Path					
Imprecise Call Progress Detector					
Must Detect Level	460 Hz Input frequency			-35	dBm
Must Reject Level	460 Hz Input frequency	-45			dBm
Hysteresis	460 Hz Input frequency	2			dB
Delay Time	460 Hz Input frequency	40		200	ms
Hold Time		10		40	ms
Receive Level Indicator (SR-RVL)					
Must Detect Level				1.00	Vpk
Must Reject Level		0.50			Vpk
Hysteresis		2			dB
Delay Time		40		205	ms
Hold Time		40		65	ms
Transmit Signal Path					
Transmit Output	Measured at TXA Attenuator word 0000 Guard tones Off V.52 511 bit data pattern	-0.8		0.8	dBV
QAM/DPSK Encoder/Modulator					
Carrier Suppression	Measured at TXA	50			dB
Modulation Frequency	1200 or 2400 Hz	-0.1		+0.1	%
Transfer Gain Variation	Measured at TXA ATT = 0000	-0.8		+0.8	dB
Transmit Attenuator					
Attenuation Range		0		15	dB
Attenuation Error	Any setting	-0.2		0.2	dB
Modulator output attenuation					
Guard Tones Off		-0.05		0.05	dB
1800 Hz guard tone on		0.9		1.1	dB
550 Hz guard tone on		1.65		1.85	dB
Tone Level	Specified for an attenuator setting of -9 dB (ATT = 1001)				
Guard Tone 550 Hz		-14.8		-12.8	dBm
Guard Tone 1800 Hz	0.4922	-17		-15	dBm
Answer Tone	0.3182	-10		-8	dBm
FSK (103, V.21)	Nom (VPP) 0.777	-10		-8	dBm
DTMF (columns)	0.777	-7		-5	dBm
DTMF (rows)	1.098	-9		-7	dBm
DTMF (twist)	0.872	-3		-1	dB

DYNAMIC CHARACTERISTICS AND TIMING[1] (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Harmonic Distortion	Distortion is specified below in dB relative to the fundamental frequency generated.				
DTMF	(0 - 10 kHz bandwidth)			-29	dB
FSK, V.21				-45	dB
Guard Tone				-31	dB
Answer Tone				-40	dB
Output Smoothing Filter Transmitted energy					
4.0 kHz				-35	dBm
10.0 kHz				-60	dBm
12.0 kHz	Guard tones disabled			-70	dBm
917.6 kHz				-70	dBm
921.6 kHz				-40	dBm
Register Reset	Register Bit DCR - RST resets all register bits to the '0' state. Subsequent µP read/write's should wait until the internal 73K214 reset cycle end.				
RST on	Time from reset bit written (rising edge $\overline{WR}$) until registers reset to '0'		4	10	µs
RST off	Time from reset bit written (rising edge $\overline{WR}$) until next permissible µP register read/write		8	20	µs
Clock Off Reset	The 73K214 will reset all control registers and status bits whenever the 7.3728 MHz clock is not present. This provides a "power on reset" capability which forces all control register bits to '0'.				
Trst	Time from last clock transition to registers reset	2		100	µs
Tact	Time from start of clock to activate state	25		40	clocks

DYNAMIC CHARACTERISTICS AND TIMING[1] (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Microprocessor Bus Interface		The timing necessary for the $\overline{CS}$ signal is the same as for address.				
Intel 8051 µP						
Address Before Latch	TAL	CL = 100 pF	20			ns
Address hold after Latch	TLA		10			ns
Latch to $\overline{RD}/\overline{WR}$ control	TLC		30			ns
$\overline{RD}/\overline{WR}$ to Latch	TCL		30			ns
Data out from $\overline{RD}$	TRD		120			ns
ALE Width	TLL		40			ns
Data float after Read	TRDF		0		80	ns
Read Width	TRW		150		5000	ns
Write Width	TWW		100		5000	ns
Data setup before write	TDW		100			ns
Data hold after write	TWD		25			ns

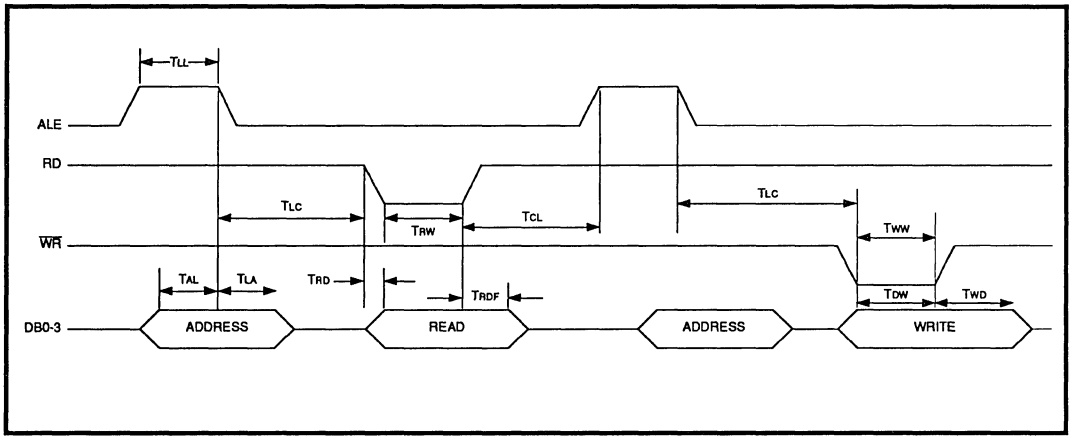


Figure 1: Intel 8051 Bus Timing

DYNAMIC CHARACTERISTICS AND TIMING[1] (continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
Zilog 8601		Zilog interface requires externally inverting ALE and $\overline{RD}$, these pins then assume the functionality of Zilog pins $\overline{AS}$ and $\overline{DS}$ respectively.				
Address before latch	TAL	CL = 100 pF	20			ns
Address hold after latch	TLA		10			ns
Latch to $\overline{DS}$ control	TLC		30			ns
Data out for $\overline{DS}$	TRD		120			ns
$\overline{AS}$ width	TLL		40			ns
Data float after read	TRDF		0		80	ns
Read width	TRW		150		5000	ns
Write width	TWW		100		5000	ns
Data setup before write	TDW		100			ns
Data hold after write	TWD		25			ns
R/$\overline{W}$ hold after $\overline{DS}$	TWH		20			ns

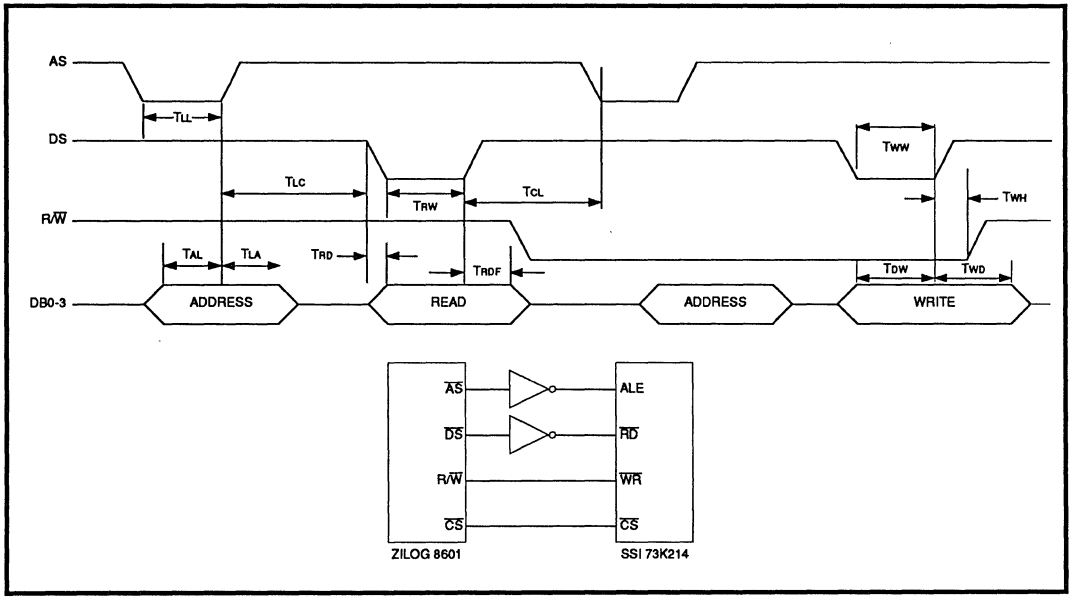


Figure 2: Zilog 8601 Bus Timing

DYNAMIC CHARACTERISTICS AND TIMING[1] (continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
Serial DSP Interface						
SCKK falling to SOUT valid	TDCK				100	ns
$\overline{SEN}$ edge to SCK edge	TSS		400			ns
SIN setup before SCK	TADC		100			ns
SIN hold after SCK	TACD	CL = 50 pF	25			ns
SIRQ setup before $\overline{SEN}$	TSL		100			ns
SIRQ hold after $\overline{SEN}$	TLS		100			ns
SCK width	TPW		800			ns
SCK frequency	FSCK			184		kHz
Receiver Clocking						
RVCKO rising to $\overline{SEN}$ falling	TRS			1.3		µs
EXADCC rising to $\overline{SEN}$ falling	TES		.5	1.1	1.7	µs
$\overline{SEN}$ low pulse width	TS			86		µs
EXADCC frequency	FEXADCC				10.5	kHz
Transmit Timing						
TXCKO rising to $\overline{TXINT}$ falling	TOB		0		500	ns
TXCKI falling to TXCKO rising	TEO[1]		-3	+1	+3	µs
RVCKO falling to TXCKO rising	TRO[2]		-3	+1	+3	µs

1) All dBm numbers refer to the signal power on the 2-wire telephone line as may be realized thru an external 2W/4W converter (hybrid). The hybrid gain from the line to the RXA pin should be 0dB.

2) When the modulator is off, the carrier detector responds to sinusoids as might be found in answer back type tones.

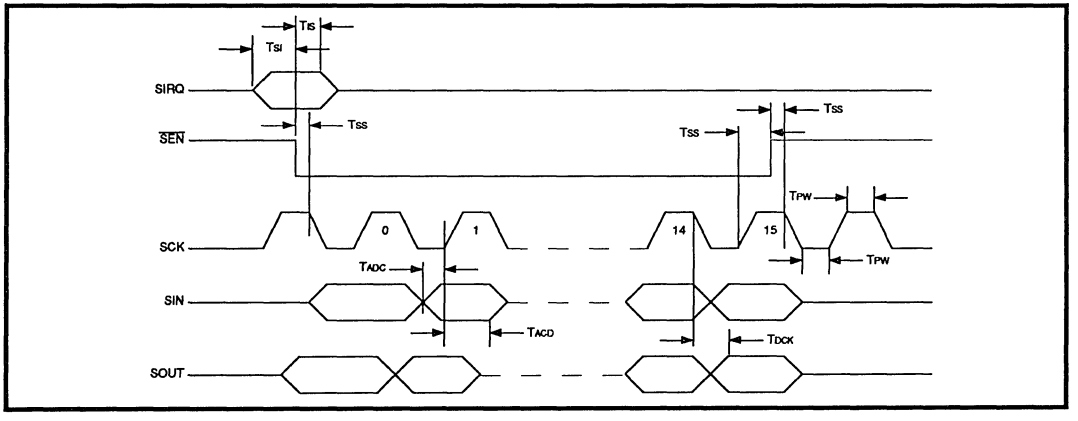


Figure 3: Serial DSP Interface Timing

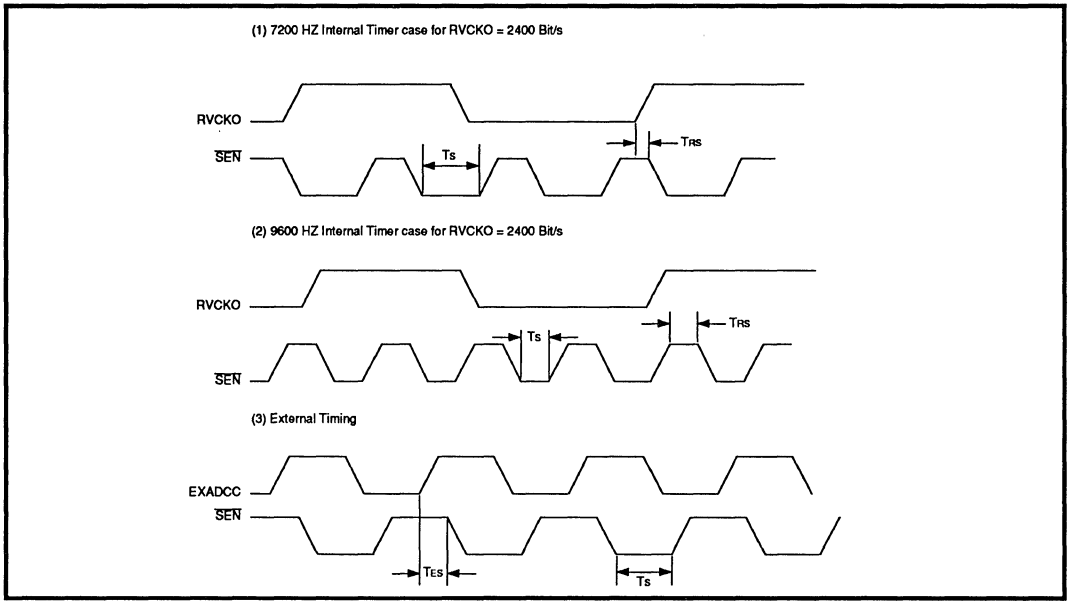


Figure 4: Receive Clocking

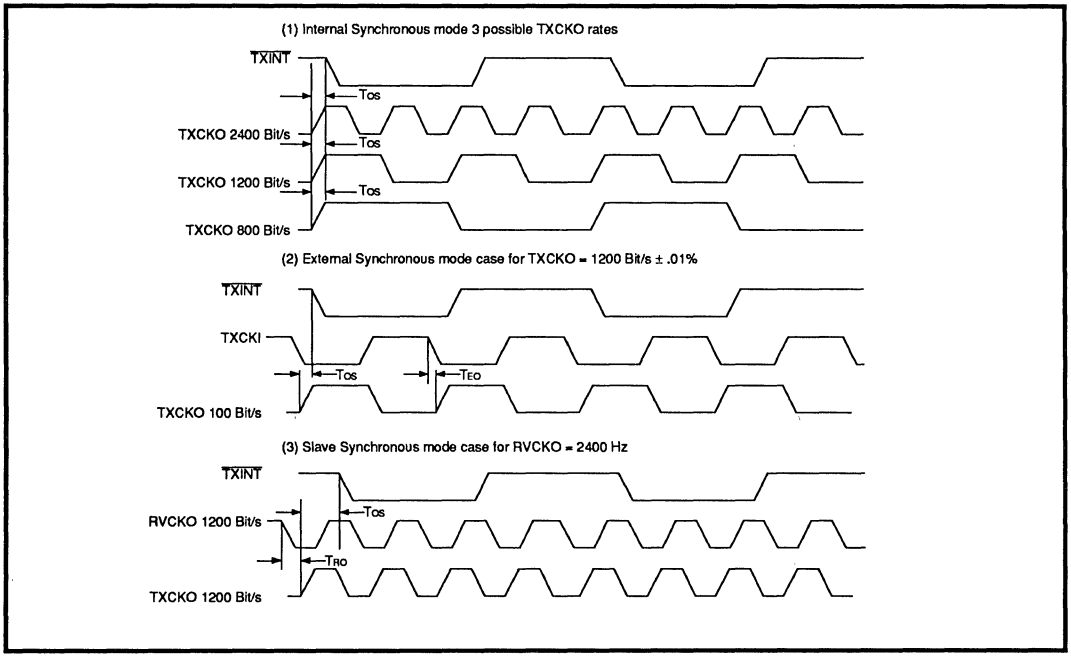


Figure 5: Transmit Timing

APPENDIX A: V.21 Operation

The SSI 73M214 tone generator includes the V.21 tones (980/1180 Hz, 1650/1850 Hz). These tones can be accessed by setting ST-1 in TR0 and writing the appropriate bits in TR1 which select 1070/1270 Hz and 2025/2225 Hz. A difficulty arises because the high band V.21 tones will not pass through the high BPF required for V.22bis. Therefore, when V.21 FSK mode is selected (i.e., DR1, DR0 = 01, FBK = 1 in registers CR0, CR1), the BPFs center frequency and bandwidth are shifted to allow the V.21 signals to pass. Care must be taken in using this feature. Some settling time will be required when the filters shift to (from) FSK. Also, the answer tone detector will not function properly when the filters have been shifted. We recommend shifting the filters after answer tone has been detected.

APPENDIX B: Using the RvT bits to synchronize the NEC 7720

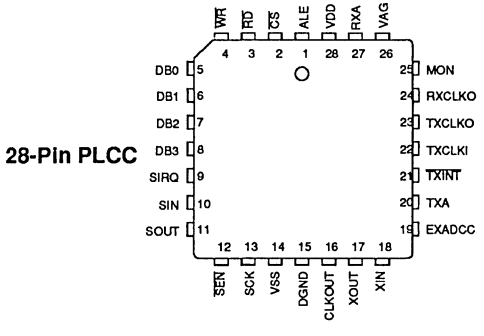
To properly synchronize the serial interface to the 7720, the following procedure may be used after power up:

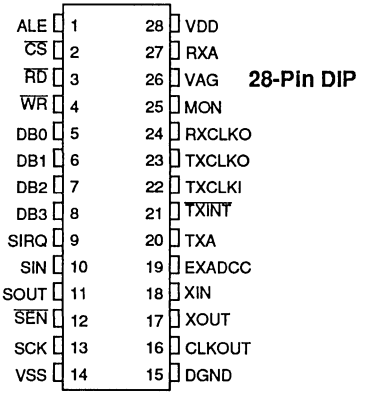
1. RESET the SSI 73M214 (write XXX 1 in Detect Register), this resets all control bits to 0, and therefore sets RvT1 = 0, RvT0 = 0.
2. WAIT 100 ms before changing RvT1, RvT0. This allows all serial clocks to cycle to an idle state. During this 100 ms, SEN will be high, and the 7720 should be reset during that time. (Other control registers may be written during this time.)

3

PACKAGE PIN DESIGNATIONS

(TOP VIEW)





ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 73M214		
Plastic Dual-In-Line	SSI 73M214-IP	73M214-IP
Plastic Leaded Chip Carrier	SSI 73M214-IH	73M214-IH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 73M235
High Speed Multi-mode Modem Analog Front End

Advance Information

July, 1990

DESCRIPTION

The SSI 73M235 is a high performance analog front end for high-speed, multi-mode modem and FAX designs. This device includes programmable filter capability, special tone detectors, and high-resolution A/D and D/A convertors to provide the analog signal conversion required for modem modulation and demodulation functions. The 73M235 also provides programmable clock recovery modes needed to support its defined operating standards. Used in conjunction with a digital signal processor, the 73M235 allows design of full and half-duplex modem products capable of operation at speeds up to 14.4 kbit/s over the conventional telephone network, on either 2- or 4-wire lines.

The SSI 73M235 uses advanced switched-capacitor filtering circuitry to achieve a wide dynamic range with low on-chip noise. To simplify modem designs, it provides a digital bus interface compatible with Silicon Systems' existing modem family, and which allows direct interface with industry standard micro-

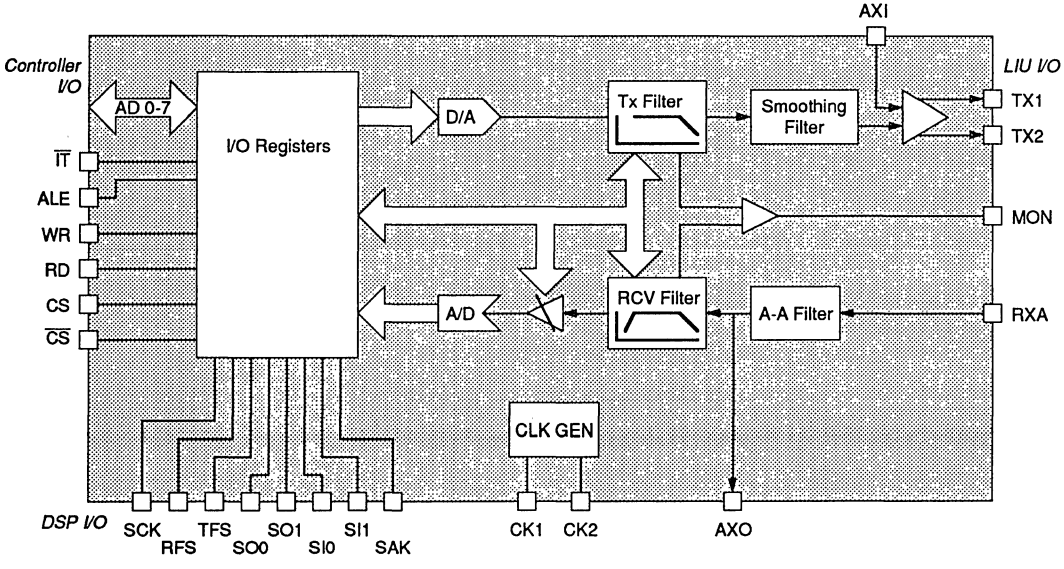
(Continued)

FEATURES

- **High performance modem analog front end for use at speeds up to 14.4 kbit/s, full or half-duplex**
- **Supports V.33, V.29, V.27ter, V.26, Bell 201/208, and fallback modes required in FAX/Data applications**
- **On-chip detectors for fast carrier detect, call progress, and answer tone detection**
- **High accuracy 8-bit A/D and D/A conversion with programmable sample rate**
- **Standard microprocessor and DSP bus interfaces allow direct connection without external hardware**
- **Less than 150 mW power from a single +5V supply with power down capability**
- **Available in 48-pin DIP or 44-pin PLCC packages**

3

BLOCK DIAGRAM



DESCRIPTION (Continued)

processors and serial-bus oriented digital signal processors typically used in modem applications. The digital interface permits data transfer in both serial and parallel modes.

The SSI 73M235 is a low power CMOS integrated circuit which operates from a single +5V power supply, allowing typical power dissipation of less than 150 mW. Packages available are 48-pin DIP or 44-pin PLCC for surface mount applications.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

SSI 73M670
V.32 Multi-mode modem Analog Front End

Advance Information

July, 1990

DESCRIPTION

The SSI 73M670 is a high performance analog front end for multi-mode V.32 high speed modem designs. This device provides programmable band-split and band-limiting filter capability, special tone detectors, and high resolution A/D and D/A convertors needed for analog signal conversion in full-duplex mode systems. Used in conjunction with one or more digital signal processors, the 73M670 allows design of half and full-duplex modem products capable of operation at speeds up to 14.4 kbit/s. On-chip interpolation and decimation filters reduce external circuitry and make it possible to design a full duplex V.32 modem with echo cancellation using the SSI 73M670, one or more DSPs, and a controlling microprocessor.

The SSI 73M670 employs a DSP to implement over-sampled Sigma-Delta A/D conversion. This provides high resolution conversion with relatively low on-chip noise, resulting in an effective dynamic range of 80 dB, and high conversion accuracy.

The SSI 73M670 is a low power CMOS integrated circuit which operates from a single +5V power supply, allowing typical power dissipation of less than 150 mW. Packages available are 64-pin miniDIP, 64-pin QFP, or 68-pin PLCC for surface mount applications.

FEATURES

- **High performance modem analog front end for use at speeds up to 14.4 kbit/s, full or half-duplex**
- **Programmable filter configurations for 8 operating modes**
- **On-chip tone detectors for carrier detect, call progress, and answer tone detection**
- **High accuracy A/D and D/A conversion using Sigma-Delta architecture**
- **Standard microprocessor and DSP bus interfaces**
- **Less than 150 mW power from a single +5V supply**
- **Available in 64-pin miniDIP, 64-pin QFP, or 68-pin PLCC pacakages**

3

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

Section

TONE SIGNALLING PRODUCTS

4

SSI 75T201
Integrated DTMF Receiver

July, 1990

DESCRIPTION

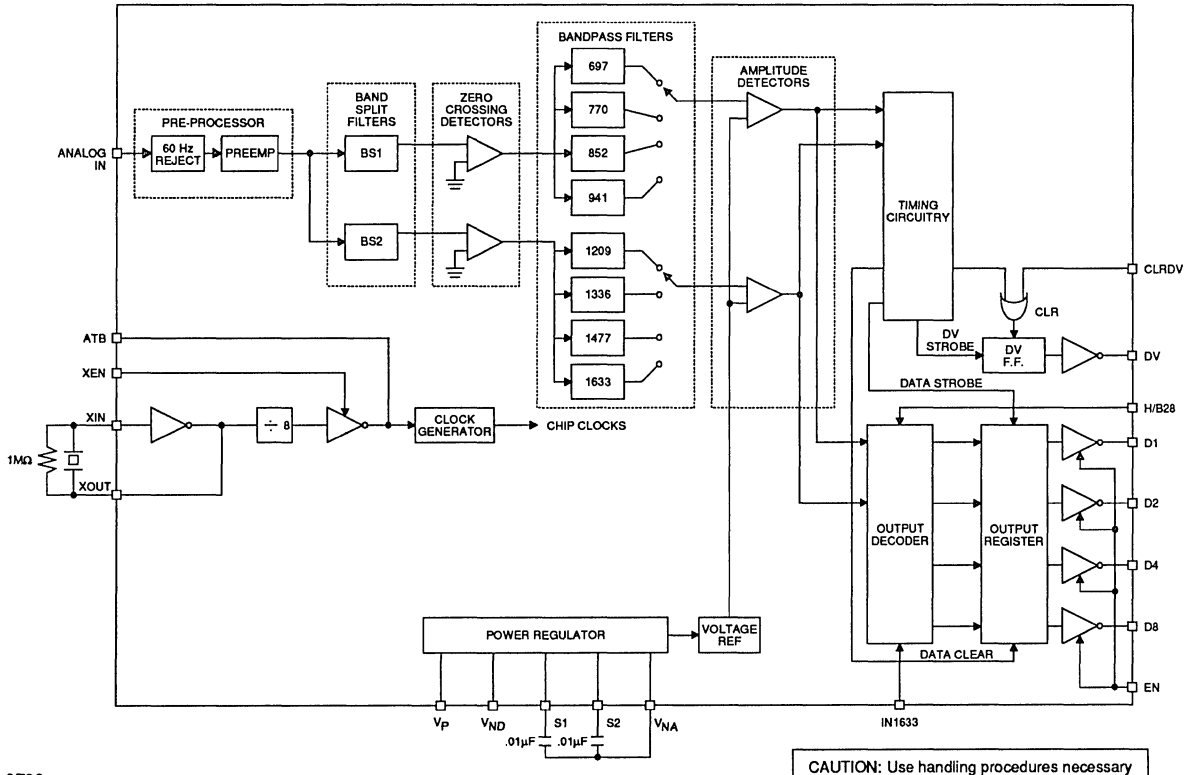
The SSI 75T201 is a complete Dual-Tone Multifrequency (DTMF) receiver detecting a selectable group of 12 or 16 standard digits. No front-end prefiltering is needed. The only external components required are an inexpensive 3.58 MHz television "colorburst" crystal (for frequency reference) and two low-tolerance bypass capacitors. Extremely high system density is made possible by using the clock output of a crystal connected SSI 75T201 receiver to drive the time bases of additional receivers. The SSI 75T201 is a monolithic integrated circuit fabricated with low-power, complementary symmetry MOS (CMOS) processing. It requires only a single low tolerance voltage supply and is packaged in a standard 22-pin DIP. (Continued)

FEATURES

- **Central office quality**
- **NO front-end band-splitting filters required**
- **Single, low-tolerance, 12-volt supply**
- **Detects either 12 or 16 standard DTMF digits**
- **Uses inexpensive 3.579545 MHz crystal for reference**
- **Excellent speech immunity**
- **Output in either 4-bit hexadecimal code or binary coded 2-of-8**
- **22-pin DIP package for high system density**
- **Synchronous or handshake interface**
- **Three-state outputs**

4

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 75T201 employs state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is preprocessed by 60 Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

CRYSTAL OSCILLATOR

The SSI 75T201 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T201's may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Twenty-five devices may run off a single crystal-connected SSI 75T201 as shown in Figure 2.

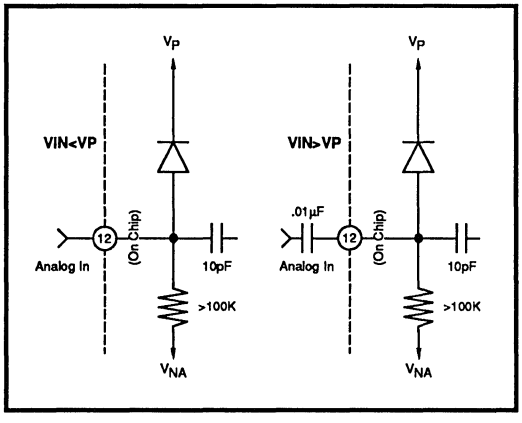


FIGURE 1: Input Coupling

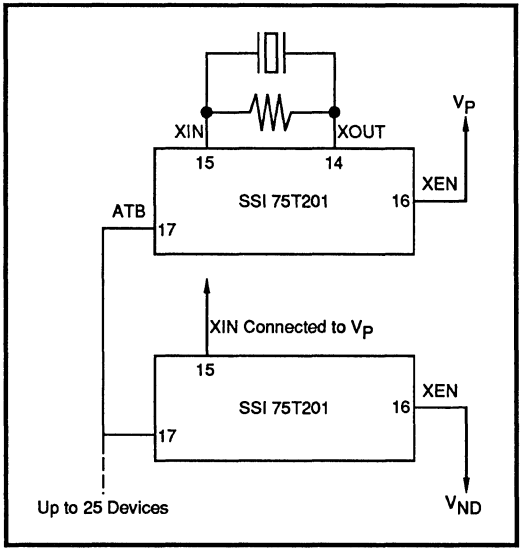


FIGURE 2: Crystal Connections

H/B28

This pin selects the format of the digital output code. When H/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: Output Codes

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633 Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, and D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the H/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever comes first.

INTERNAL BYPASS PINS, S1, S2

In order for the SSI 75T201 DTMF Receiver to function properly, these pins must be bypassed to V_{NA} with 0.01 µF ±20% capacitors.

POWER SUPPLY PINS, V_P, V_{NA}, V_{ND}

The analog (V_{NA}) and digital (V_{ND}) supplies are brought out separately to enhance analog noise immunity on the chip. V_{NA} and V_{ND} should be connected externally as shown in Figure 3.

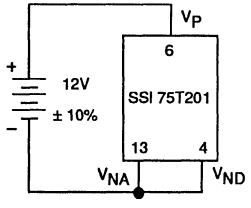


FIGURE 3: 12V System

N/C PINS

These pins have no internal connection and may be left floating.

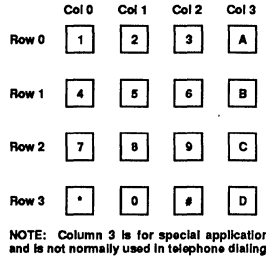


FIGURE 4: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may damage the device. All SSI 75T201 unused inputs must be connected to V_P or V_{ND}, as appropriate.

PARAMETER	RATING	UNIT
DC Supply Voltage - V_P	Referenced to V_{NA}, V_{ND}	+16V
Operating Temperature		-40 to +85°C Ambient
Storage Temperature		-65 to +150°C
Power Dissipation (25°C)		1W
Input Voltage	All inputs except ANALOG IN	(V_P+ 0.5V) to (V_{ND} -0.5V)
ANALOG IN Voltage		(V_P + 0.5V) to (V_P - 22V)
DC Current into any Input		±1.0 mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

(-40°C ≤ Ta ≤ +85°C, V_P - V_{ND} = V_P - V_{NA} = 12V ± 10%)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		± (1.5+2 Hz)	±2.3	±3.0	% of f_O
Amplitude for Detection	each tone	-24		+6	dBm ref. to 600Ω
Minimum Acceptable Twist	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-8		+4	dB
60 Hz Tolerance				2	Vrms
Dial Tone Tolerance	"precise" dial tone			0	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 750 µA load	V_{ND}		V_{ND}+0.5	V
(except XOUT)	"1" level, 750 µA load	V_P-0.5		V_P	V
Digital Inputs	"0" level	V_{ND}		**	V
(except H/B28, XEN)	"1" level	***		V_P	V
Digital Inputs	"0" level	V_{ND}		V_{ND}+1	V
H/B28, XEN	"1" level	V_P-1		V_P	V
Power Supply Noise	wide band			25	mVp-p
Supply Current	Ta = 25°C V_P - V_{NA} = V_P - V_{ND} = 12V±10%		29	50	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P$ - 22	100 kΩ||5 pF			

* dB referenced to lowest amplitude tone
** V_{ND} + 0.3(V_P - V_{ND})
*** V_P - 0.3(V_P - V_{ND})

TIMING CHARACTERISTICS

(-40°C ≤ Ta ≤ +85°C, V_P - V_{ND} = V_P - V_{NA} = 12V ± 10%)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_v	Tone Detection Time		20	25	40	ms
t_{slh}	Data Overlap of DV Rising Edge	CLRDV = V_{ND}, EN = V_P	7			µs
t_p	Pause Detection Time		25	32	40	ms
t_{dv}	Time between end of Tone and Fall of DV		40	45	50	ms

TIMING CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{shl}	Data overlap of DV Falling Edge		4	4.56	4.8	ms
t_{phl}	Prop. Delay: Rise of CLRDV to fall of DV	Cl = 300 pF Measured at 50% points			1	µs
	Output Enable Time	Cl = 300 pF, Rl = 10K Measured from 50% point of Rising Edge of EN to the 50% point of the data output with Rl to opposite rail.			1	µs
	Output Disable Time	Cl = 300 pF, Rl = 1K, ΔV = 1V Measured from 50% point of Falling Edge of EN to time at which output has changed 1V with Rl to opposite rail.			1	µs
	Output 10-90% Transition Time	Cl = 300 pF			1	µs

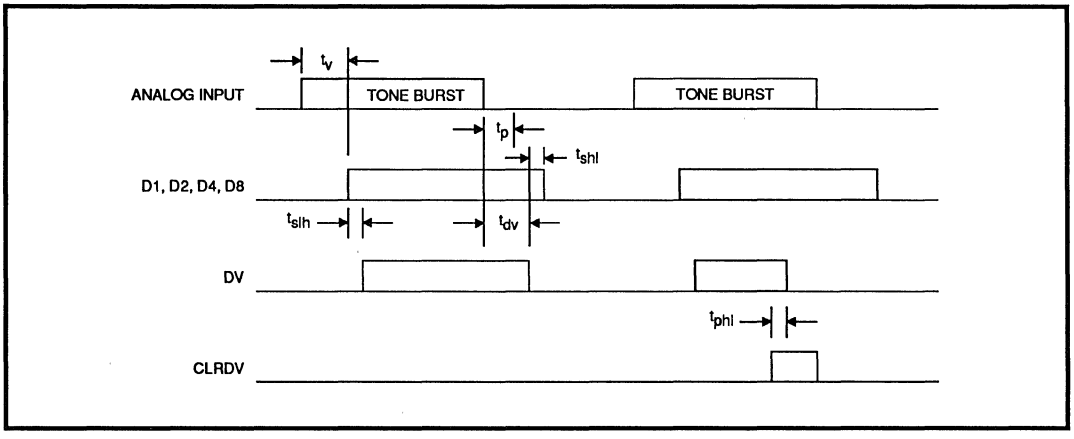


FIGURE 5: Timing Diagram

APPLICATION INFORMATION

TELEPHONE LINE INTERFACE

In applications that use the SSI 75T201 to decode DTMF signals from a phone line, a DAA (Direct Access Arrangement) must be implemented. Equipment intended for connection to the public telephone network must comply with and be registered in accordance with FCC Part 68. For PBX applications refer to EIA Standard RS-464.

Some of the basic guidelines are:

1) Maximum voltage and current ratings of the SSI 75T201 must not be exceeded; this calls for protection from ringing voltage, if applicable, which ranges from 80 to 120 volts RMS over a 20 to 80Hz frequency range.

2) The interface equipment must not breakdown with high-voltage transient tests (including a 2500 volt peak surge) as defined in the applicable document.

3) Phone line termination must be less than 200Ω DC and approximately 600Ω AC (200-3200 Hz).

4) Termination must be capable of sustaining phone line loop current (off-hook condition) which is typically 18 to 120 mA DC.

5) The phone line termination must be electrically balanced with respect to ground.

6) Public phone line termination equipment must be registered in accordance to FCC Part 68 or connected through registered protection circuitry. Registration typically takes about six months.

Figure 6 shows a simplified phone line interface using a 600Ω 1:1 line transformer. Transformers specially designed for phone line coupling are available from many transformer manufacturers.

Figure 7 shows a more featured version of Figure 6. These added options include:

1) A 150-volt surge protector to eliminate high voltage spikes.

2) A Texas Instruments TCM1520A ring detector, optically isolated from the supervisory circuitry.

3) Back-to-back Zener diodes to protect the DTMF (and optional multiplexer Op-Amp) from ringer voltage.

4) Audio multiplexer which allows voice or other audio to be placed on the line (a recorded message, for example) and not interfere with incoming DTMF tone detection.

An integrated voice circuit may also be implemented for line coupling, such as the Texas Instruments TCM1705A, however, this approach is typically more expensive than using a transformer as shown above.

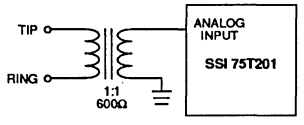


FIGURE 6: Simplified Interface

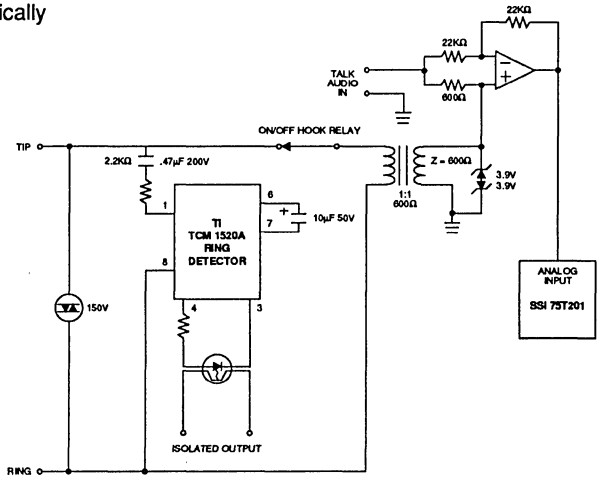
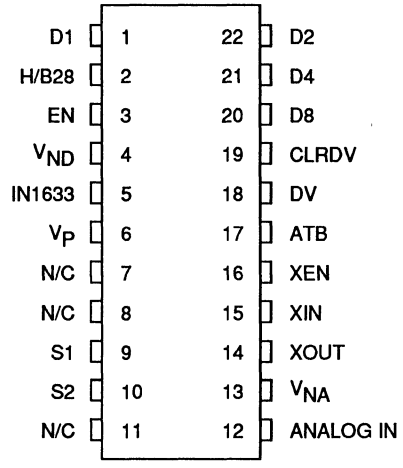


FIGURE 7: Full Featured Interface

SSI 75T201
Integrated
DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



22-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T201 22-Pin Plastic DIP	SSI 75T201 - IP	75T201 - IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 75T202/203
5V Low-Power DTMF Receiver

July, 1990

DESCRIPTION

The SSI 75T202 and 75T203 are complete Dual-Tone Multifrequency (DTMF) receivers detecting a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is made possible by using the clock output of a crystal-connected SSI 75T202 or 75T203 receiver to drive the time bases of additional receivers. Both are monolithic integrated circuits fabricated with low-power, complementary symmetry MOS (CMOS) processing. They require only a single low tolerance voltage supply and are packaged in a standard 18-pin plastic DIP.

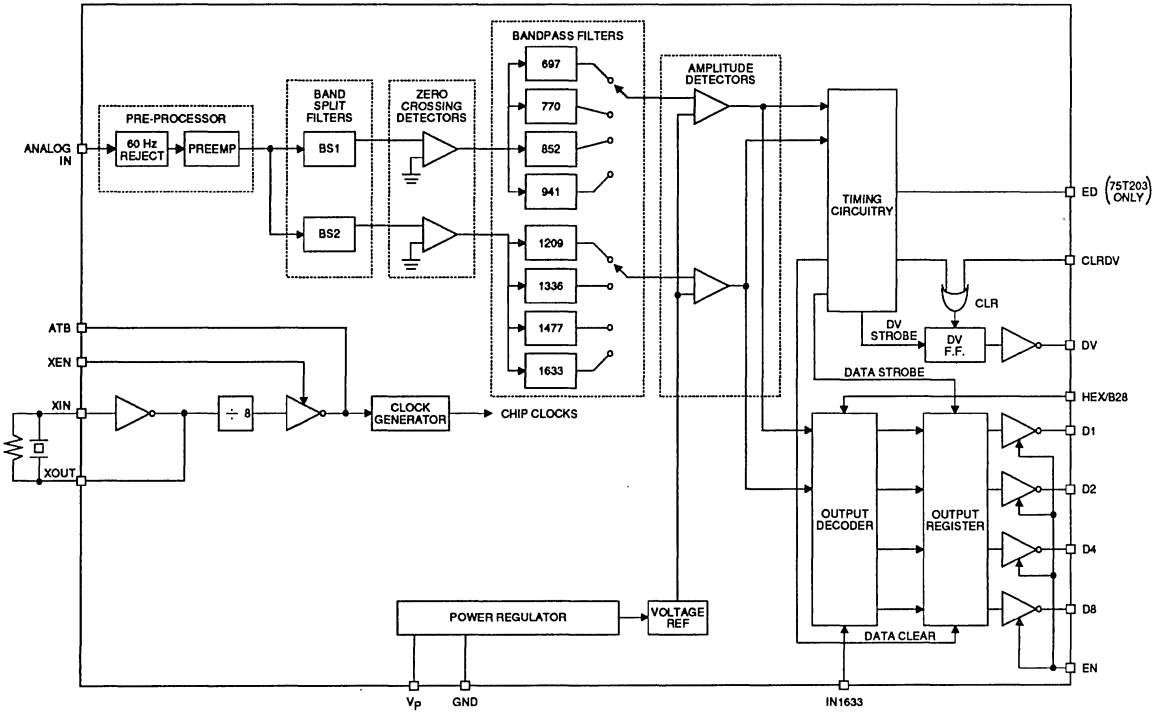
(Continued)

FEATURES

- **Central office quality**
- **NO front-end band-splitting filters required**
- **Single, low-tolerance, 5-volt supply**
- **Detects either 12 or 16 standard DTMF digits**
- **Uses inexpensive 3.579545-MHz crystal for reference**
- **Excellent speech immunity**
- **Output in either 4-bit hexadecimal code or binary coded 2-of-8**
- **18-pin DIP package for high system density**
- **Synchronous or handshake interface**
- **Three-state outputs**
- **Early detect output (SSI 75T203 only)**

4

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 75T202 and 75T203 employ state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semicondutor process. The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

The SSI 75T202 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics less then -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T202 and 75T203 contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T202's (or 75T203's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 75T202 or 75T203 as shown in Figure 2.

HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: Output Codes

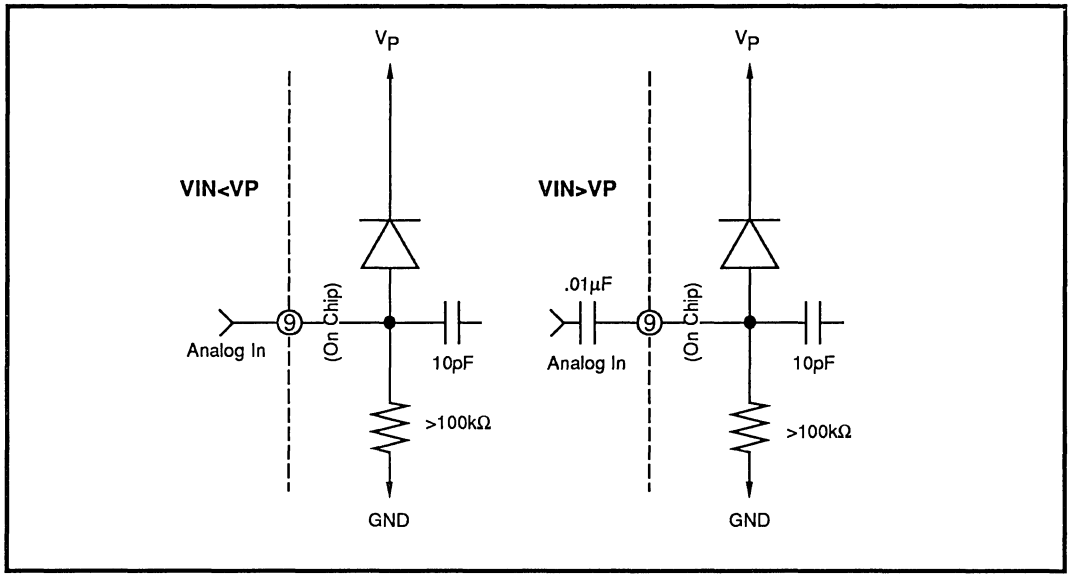


FIGURE 1: Input Coupling

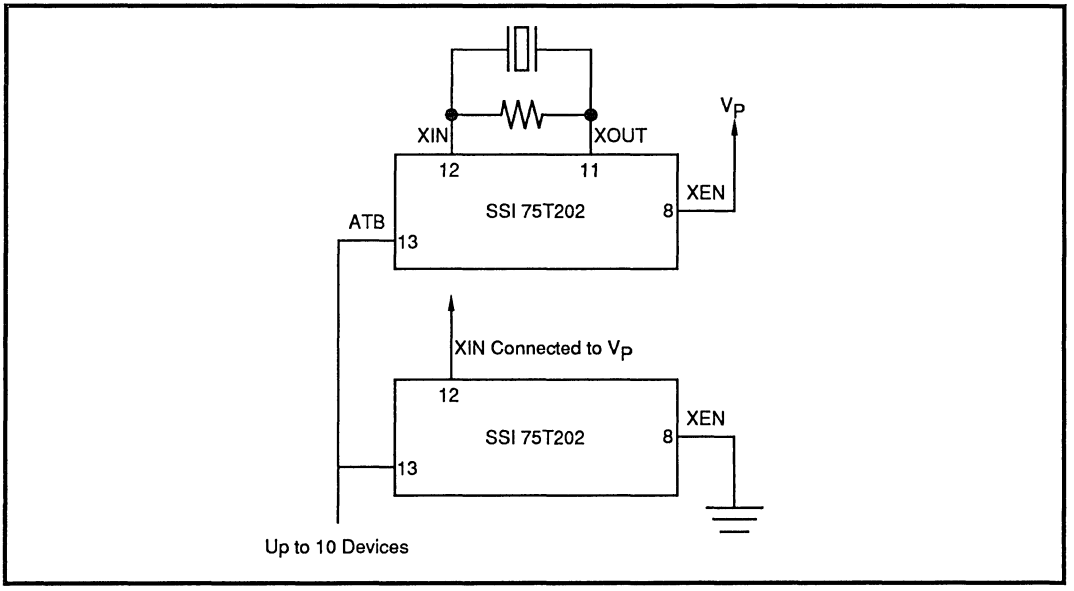


FIGURE 2: Crystal Connections

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier.

ED (SSI 75T203 only)

The ED output goes high as soon as the SSI 75T203 begins to detect a DTMF tone pair and falls when the 75T203 begins to detect a pause. The D1, D2, D4, and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

N/C PINS

These pins have no internal connection and may be left floating.

DTMF DIALING MATRIX

See Figure 3. Please make note that column 3 is for special applications and is not normally used in telephone dialing.

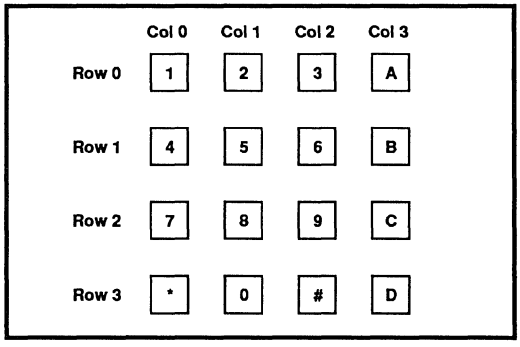


FIGURE 3: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may damage the device. All SSI 75T202/203 unused inputs must be connected to V_P or GND, as appropriate.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P		+7V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		65mW
Input Voltage	All inputs except ANALOG IN	(V_P + .5V) to -.5V
ANALOG IN Voltage		(V_P + .5V) to (V_P - 10V)
DC Current into any Input		±1.0mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

(-40°C ≤ T_A ≤ +85°C, V_P = 5V ± 10%)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	% of fo
Amplitude for Detection	each tone	-32		-2	dBm ref. to 600Ω
Minimum Acceptable Twist	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-10		+10	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 400µA load	0		0.5	V
(except XOUT)	"1" level, 200µA load	V_P-0.5		V_P	V
Digital Inputs	"0" level	0		0.3V_P	V
	"1" level	0.7V_P		V_P	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P$-10	100kΩ||15pF			

* dB referenced to lowest amplitude tone

SSI 75T202/203 TIMING

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON}	Tone Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_{OFF}	Pause Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_D	Detect Time		25	-	46	ms
t_R	Release Time		35	-	50	ms
t_{SU}	Data Setup Time		7	-	-	µs
t_H	Data Hold Time		4.2	-	5.0	ms
t_{CL}	DV Clear Time		-	160	250	ns
t_{PW}	CLRDV Pulse Width		200	-	-	ns
t_{ED}	ED Detect Time		7	-	22	ms
t_{ER}	ED Release Time		2	-	18	ms
	Output Enable Time	C_L = 50pF, R_L = 1kΩ	-	-	200	ns
	Output Disable Time	C_L = 35pF, R_L = 500Ω	-	-	200	ns
	Output Rise Time	C_L = 50pF	-	-	200	ns
	Output Fall Time	C_L = 50pF	-	160	200	ns

SSI 75T202/203 TIMING (Continued)

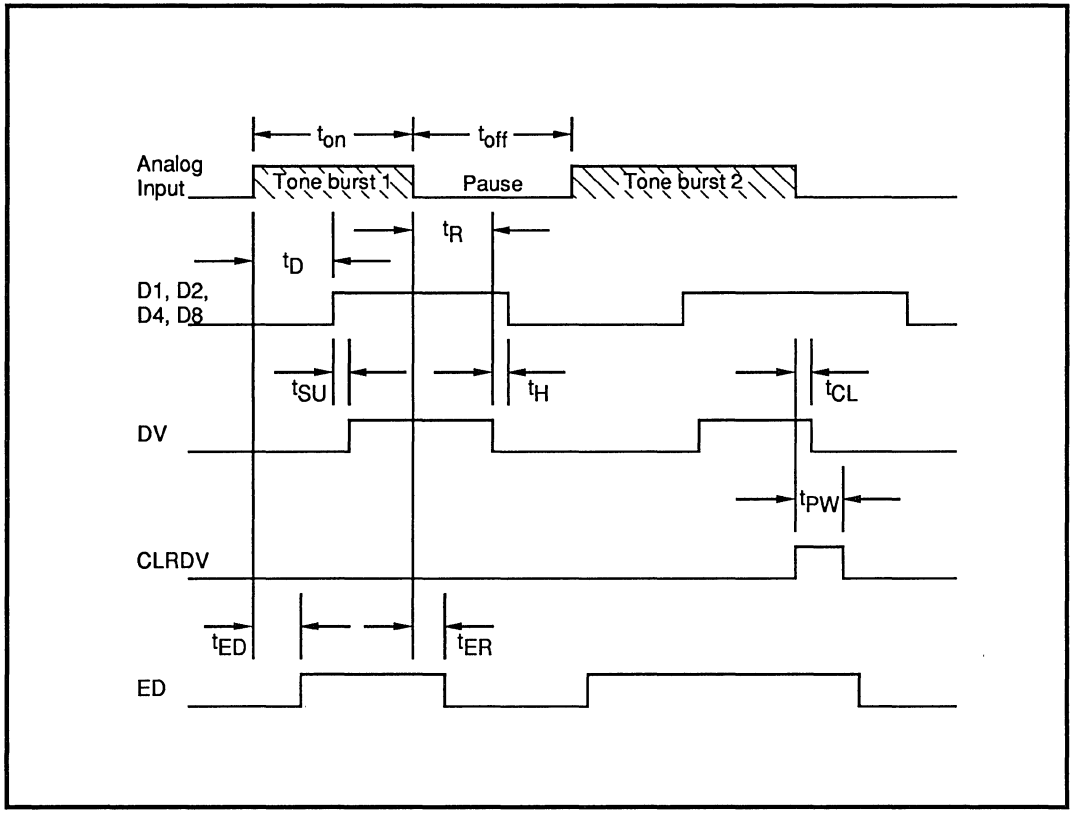
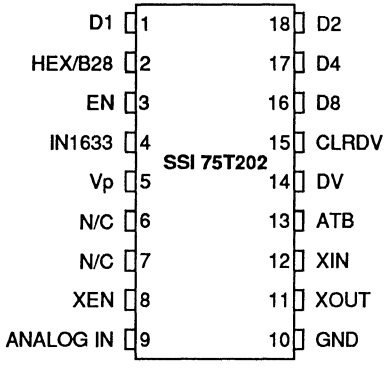


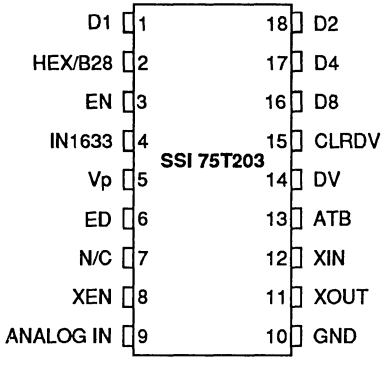
FIGURE 4: Timing Diagram

SSI 75T202/203
5V Low-Power
DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



18 - Pin DIP
SSI 75T202



18 - Pin DIP
SSI 75T203

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T202 18-pin Plastic DIP	SSI 75T202-IP	75T202-IP
SSI 75T203 18-pin Plastic DIP	SSI 75T203-IP	75T203-IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 75T204
5V Low-Power Subscriber DTMF Receiver

July, 1990

DESCRIPTION

The SSI 75T204 is a complete Dual-Tone Multifrequency (DTMF) receiver that detects 16 standard digits. No front-end pre-filtering is needed. The only external components required are an inexpensive 3.58-MHz television "colorburst" crystal for frequency reference and a bias resistor. An Alternate Time Base (ATB) is provided to permit operation of up to 10 SSI 75T204's from a single crystal. The SSI 75T204 employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering, and digital circuitry on the same CMOS chip. The analog input signal is pre-processed by 60-Hz reject and band split filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to

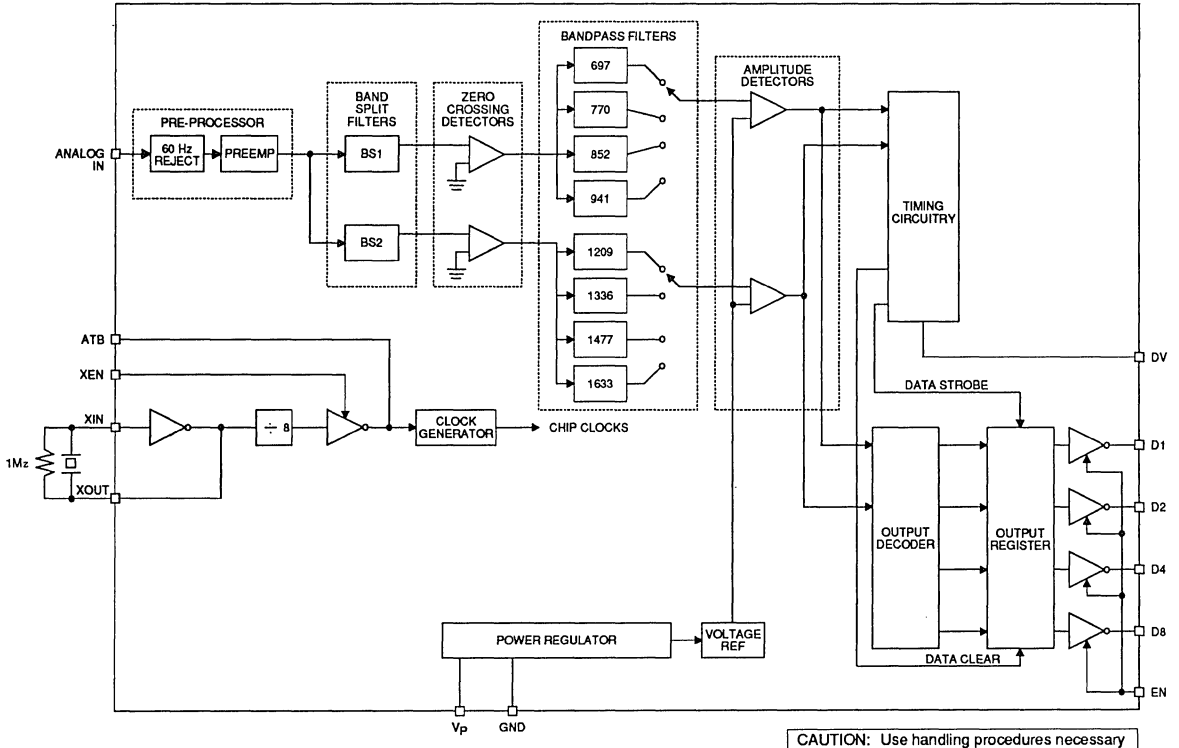
(Continued)

FEATURES

- **Intended for applications with less requirements than the SSI 75T202**
- **14-pin plastic DIP or 16-pin SO package for high system density**
- **NO front-end band-splitting filters required**
- **Single low-tolerance 5-volt supply**
- **Detects all 16 standard DTMF digits.**
- **Uses an inexpensive 3.579545-MHz crystal**
- **Excellent speech immunity**
- **Output in 4-bit hexadecimal code**
- **Three-state outputs for microprocessor interface**

4

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

measure the tone and pause durations and to provide output timing and decoding. The outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

The SSI 75T204 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics less then -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T204 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T204's (or 75T202's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 75T204 (or 75T202) as shown in Figure 2.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. The hexadecimal codes are described in Table 1.

DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs.

N/C PINS

These pins have no internal connection and may be left floating.

	Output Code			
Digit	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

TABLE 1: Output Codes

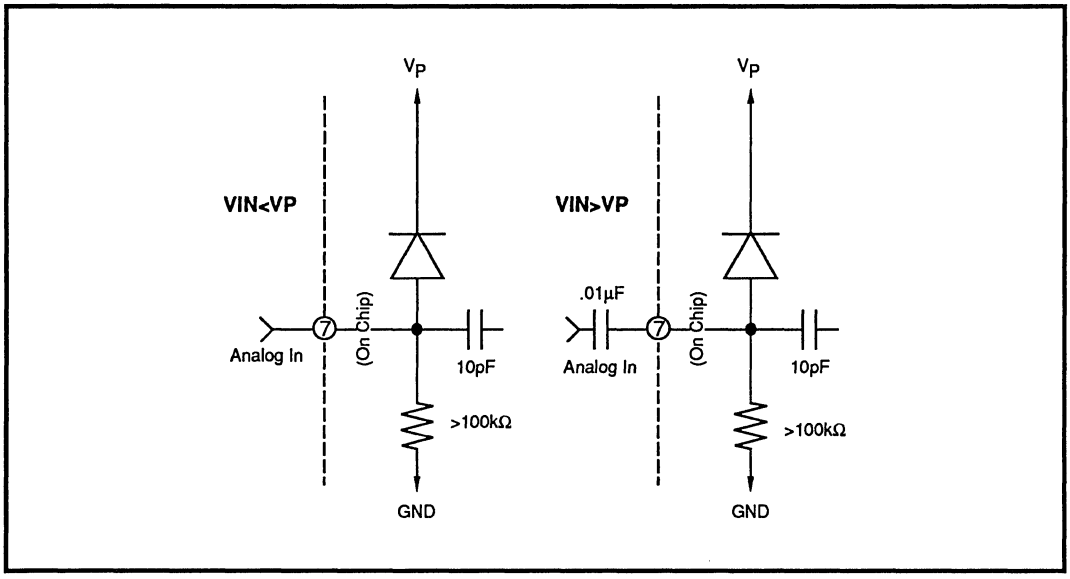


FIGURE 1: Input Coupling

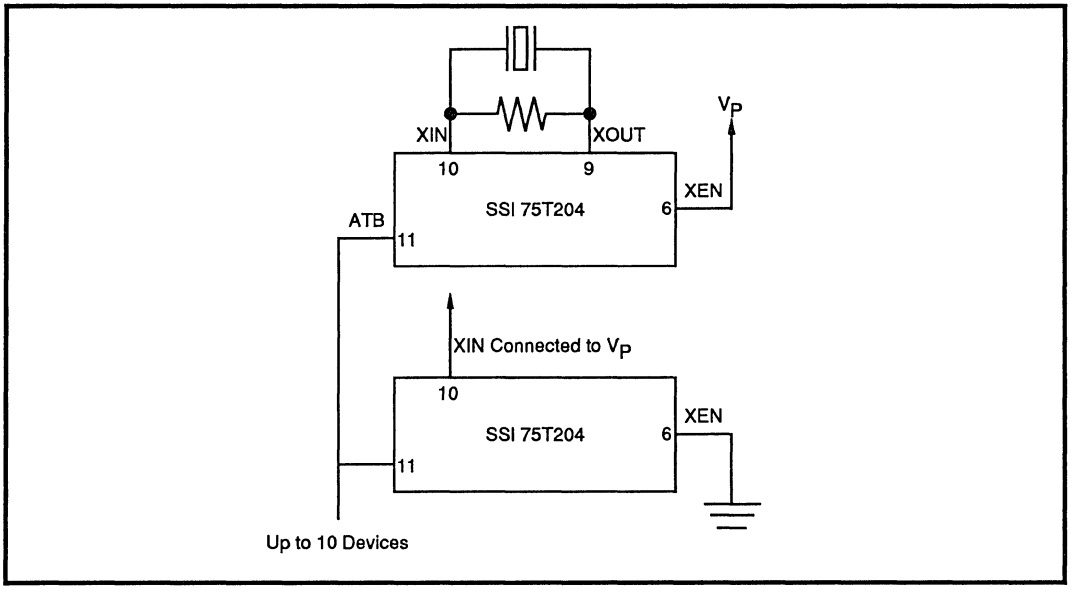


FIGURE 2: Crystal Connections

DTMF DIALING MATRIX

See Figure 3. Please note that column 3 is for special applications and is not normally used in telephone dialing.

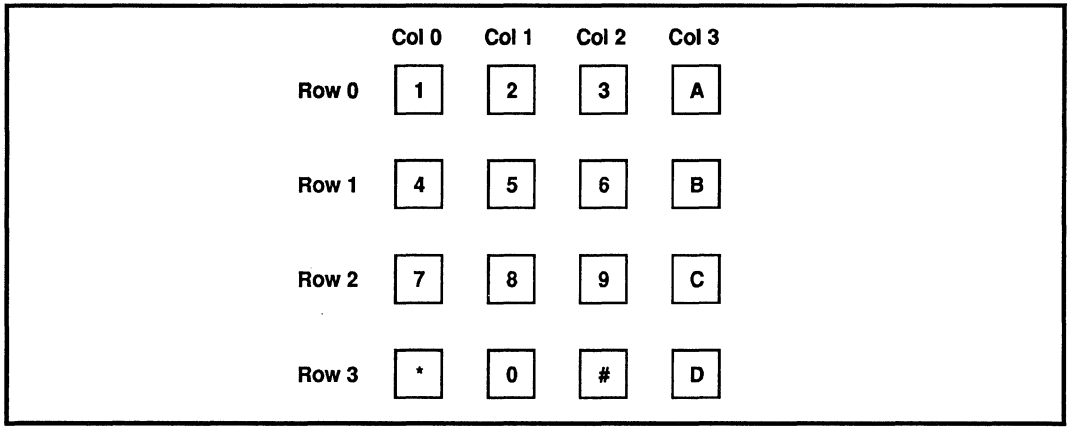


FIGURE 3: DTMF Dialing Matrix

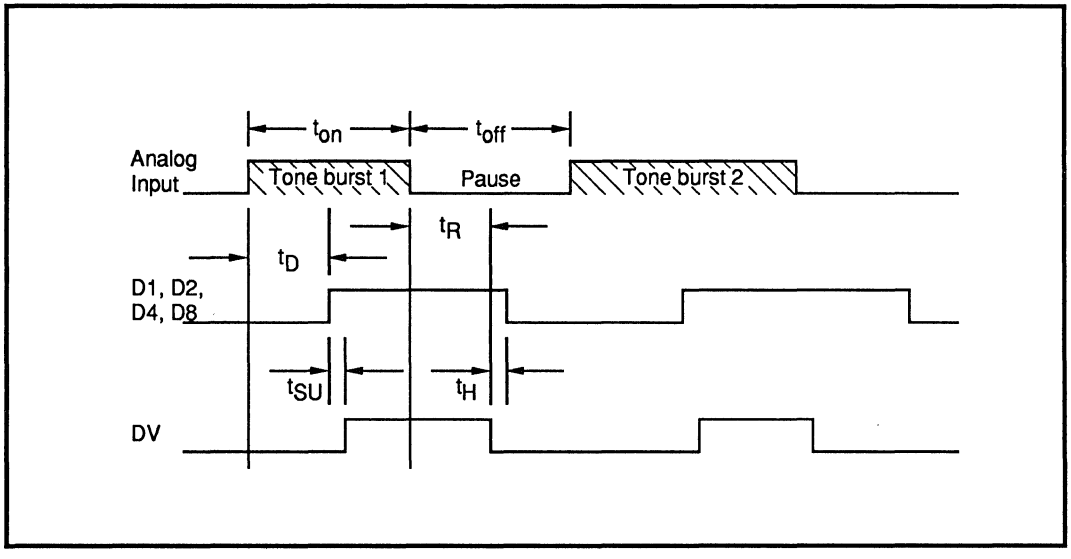


FIGURE 4: Timing Diagram

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

SSI 75T204 TIMING (Refer to Figure 4.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON}	Tone Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_{OFF}	Pause Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_D	Detect Time		25	-	46	ms
t_R	Release Time		35	-	50	ms
t_{SU}	Data Setup Time		7	-	-	µs
t_H	Data Hold Time		4.2	-	5.0	ms
	Output Enable Time	C_L = 50pF, R_L = 1kΩ	-	-	200	ns
	Output Disable Time	C_L = 35pF, R_L = 500Ω	-	-	200	ns
	Output Rise Time	C_L = 50pF	-	-	200	ns
	Output Fall Time	C_L = 50pF	-	-	200	ns

APPLICATION INFORMATION

The SSI 75T204 will tolerate total input RMS noise up to 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the SSI 75T204 unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter shown in Figure 5 may be employed to band limit the incoming signal.

Noise will also be reduced by placing a grounded trace around the XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case leave XOUT floating.

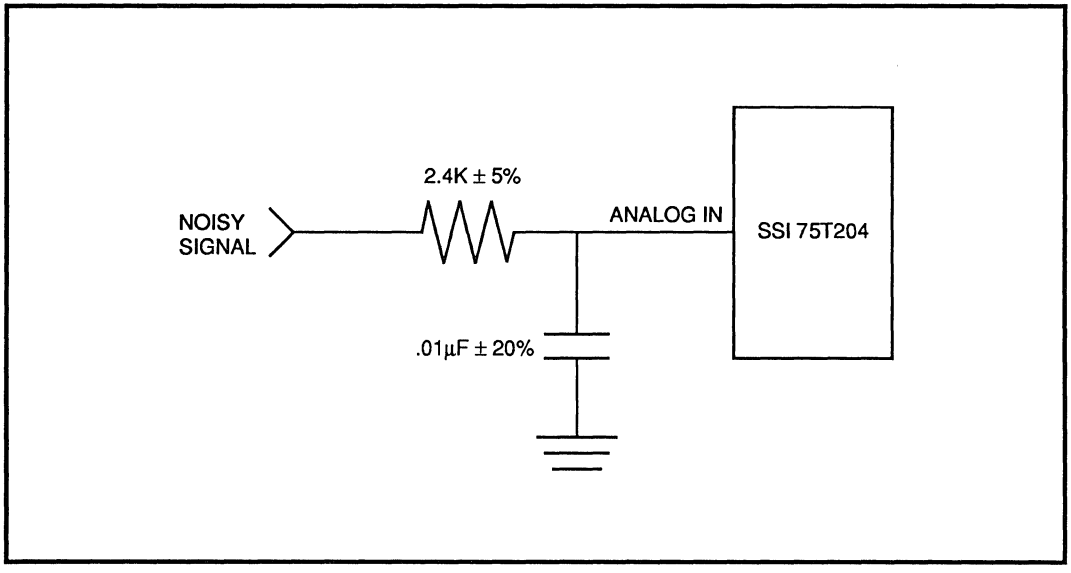


FIGURE 5: RC Filter

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may damage the device. All SSI 75T204 unused inputs must be connected to V_P or GND, as appropriate.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P		+7V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		65mW
Input Voltage	All inputs except ANALOG IN	(V_P + 0.5V) to -0.5V
ANALOG IN Voltage		(V_P + .5V) to (V_P - 10V)
DC Current into any Input		±1.0mA
Lead Temperature	Soldering, 10 sec.	300°C

4

ELECTRICAL CHARACTERISTICS

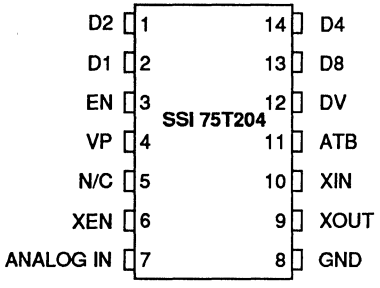
(-40°C ≤ T_A ≤ +85°C, V_P = 5V ± 10%)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	% of fo
Amplitude for Detection	each tone	-32		-2	dBm ref. to 600Ω
Minimum Acceptable Twist	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-10		+10	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 400µA load	0		0.5	V
(except XOUT)	"1" level, 200µA load	V_P-0.5		V_P	V
Digital Inputs	"0" level	0		0.3V_P	V
	"1" level	0.7V_P		V_P	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P$-10	100KΩ||15pF			

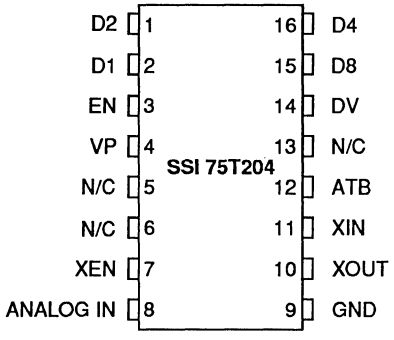
* dB referenced to lowest amplitude tone

SSI 75T204
5V Low-Power
Subscriber DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



14 - Pin DIP



16 - Pin SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T204 14-pin PDIP	SSI 75T204-IP	75T204-IP
SSI 75T204 16-pin SOL	SSI 75T204-IL	75T204-IL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 75T2089
DTMF Transceiver

July, 1990

DESCRIPTION

Silicon Systems' SSI 75T2089 is a complete Dual-Tone Multifrequency (DTMF) Transceiver that can both generate and detect all 16 DTMF tone pairs. The SSI 75T2089 circuit integrates the performance proven SSI 75T202 DTMF receiver with a new DTMF generator circuit.

The DTMF receiver electrical characteristics are identical to the standard SSI 75T202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

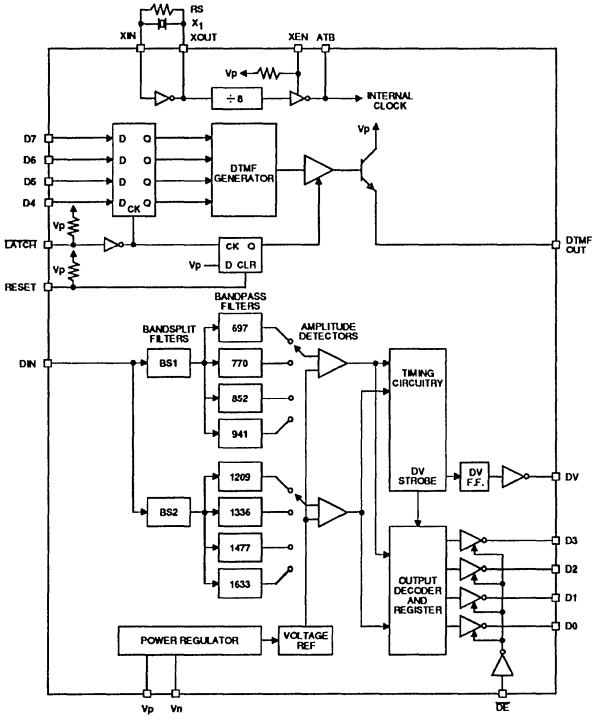
The only external components necessary for the SSI 75T2089 are a 3.58 MHz "colorburst" crystal with a parallel 1MΩ resistor. This provides the time base for digital functions and switched-capacitor filters in the device. No external filtering is required.

FEATURES

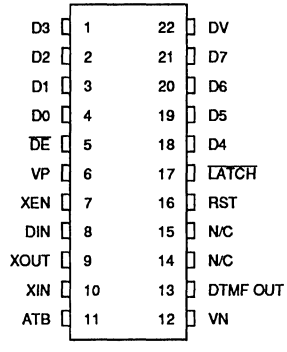
- **DTMF Generator and Receiver on one-chip**
- **22-pin, 400 mil plastic DIP**
- **Low-power 5 volt CMOS**
- **DTMF Receiver exhibits excellent speech immunity**
- **Three-state outputs (4-bit hexadecimal) from DTMF Receiver**
- **AC coupled, internally biased analog input**
- **Latched DTMF Generator inputs**
- **Analog input range from –32 to –2 dBm (ref 600 Ω)**
- **DTMF output typ. –8 dBm (Low Band) and –5.5 dBm (High Band)**
- **Uses inexpensive 3.579545 MHz crystal for reference**
- **Easy interface for microprocessor dialing**

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

RECEIVER

The DTMF Receiver in the SSI 75T2089 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band-splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

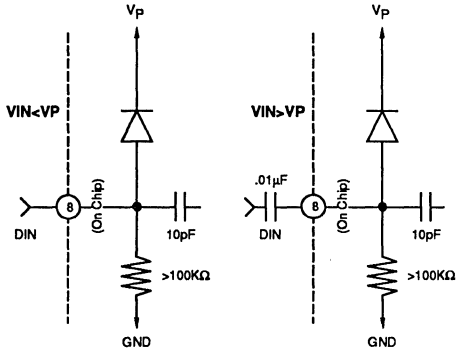


FIGURE 1: Input Coupling

The SSI 75T2089 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T2089 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the SSI 75T2089 depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SSI 75T2089 as shown in Figure 2.

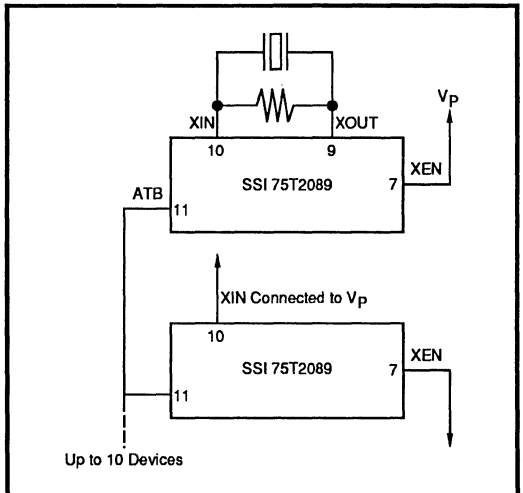


FIGURE 2: Crystal Connections

RECEIVER OUTPUTS AND THE $\overline{DE}$ PIN

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Figure 3 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

Digit In / Out	Hexadecimal Code D7 / D3	D6 / D2	D5 / D1	D4 / D0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

FIGURE 3

GENERATOR

The DTMF generator on the SSI 75T2089 responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{\text{LATCH}}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

DIGITAL INPUTS

The D4, D5, D6, D7, $\overline{\text{LATCH}}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Figure 4 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits

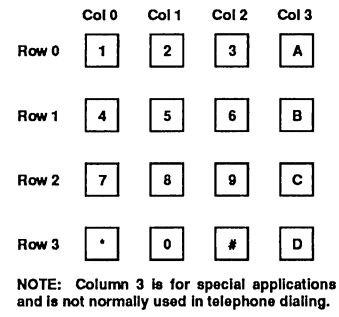


FIGURE 4: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697Hz	Column 0 = 1209Hz
Row 1 = 770Hz	Column 1 = 1336Hz
Row 2 = 852Hz	Column 2 = 1477Hz
Row 3 = 941Hz	Column 3 = 1633Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown in Figure 5.

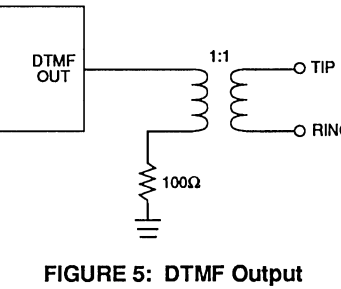


FIGURE 5: DTMF Output

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating above absolute maximum ratings may damage the device.

PARAMETER	RATING	UNIT
DC Supply Voltage (Vp - Vn)	+7	V
Voltage at any Pin (Vn = 0)	-0.3 to Vp + 0.3	V
DIN Voltage	Vp + 0.5 to Vp - 10	V
Current through any Protection Device	±20	mA
Operating Temperature Range	-40 to + 85	°C
Storage Temperature	-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Voltage		4.5		5.5	V
Power Supply Noise (wide band)				10	mV pp
Ambient Temperature		-40		+85	°C
Crystal Frequency (F Nominal = 3.579545MHz)		-0.01		+0.01	%
Crystal Shunt Resistor		0.8		1.2	MΩ
DTMF OUT Load Resistance		100			Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current*			15	30	mA
Power Dissipation				225	mW
Input Voltage High		0.7Vp			V
Input Voltage Low				0.3Vp	V
Input Current High				10	µA
Input Current Low		-10			µA
Output Voltage High	Ioh = -0.2mA	Vp-0.5			V
Output Voltage Low	Iol = +0.4mA			Vn+0.5	V
* with DTMF output disabled					

DTMF RECEIVER: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection		-32		-2	dBm
Twist Tolerance		-10		+10	dB
60Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone			0	dB*
Speech Immunity	MITEL Tape #CM7290		2		hits
Noise Tolerance	MITEL Tape #CM7290			-12	dB*
Input Impedance		100			kΩ
* Referenced to lowest amplitude tone					

DTMF RECEIVER: Timing Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TON	Tone Time for Detect		40			ms
TON	Tone Time for No Detect				20	ms
TOFF	Pause Time for Redetection		40			ms
TOFF	Pause Time for Bridging				20	ms
TD1	Detect Time		25		46	ms
TR1	Release Time		35		50	ms
TSU1	Data Set Up Time		7			µs
THD1	Data Hold Time		4.2		5.0	ms
	Output Enable Time				200	ns
	Output Disable Time				200	ns

DTMF GENERATOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Accuracy		-1.0		+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp - Vn = 5.0V				
Low Band		-9.2		-7.2	dBm
High Band		-6.6		-4.6	dBm
Output Distortion	DC to 50kHz			-20	dB

DTMF GENERATOR: Timing Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TSTART	Start-Up Time				2.5	µs
TSU2	Data Set-Up Time		100			ns
THD2	Data Hold Time		50			ns
TRP	RESET Pulse Width		100			ns
TPW	$\overline{\text{LATCH}}$ Pulse Width		100			ns

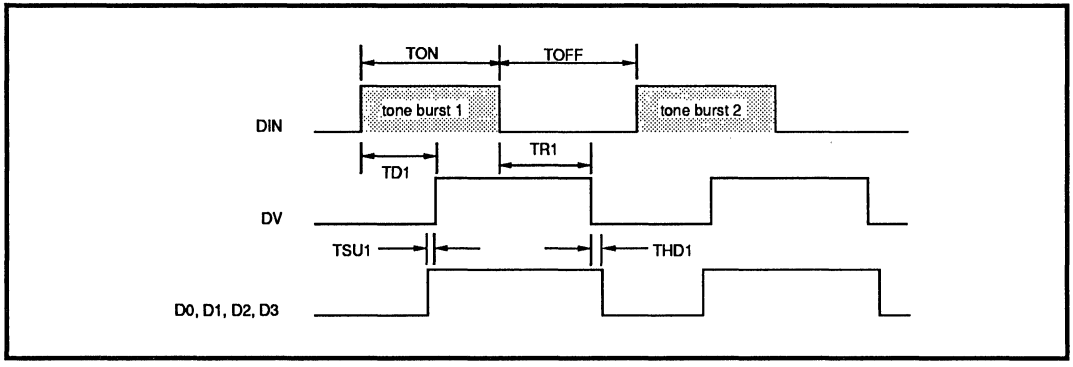


FIGURE 6: DTMF DECODER

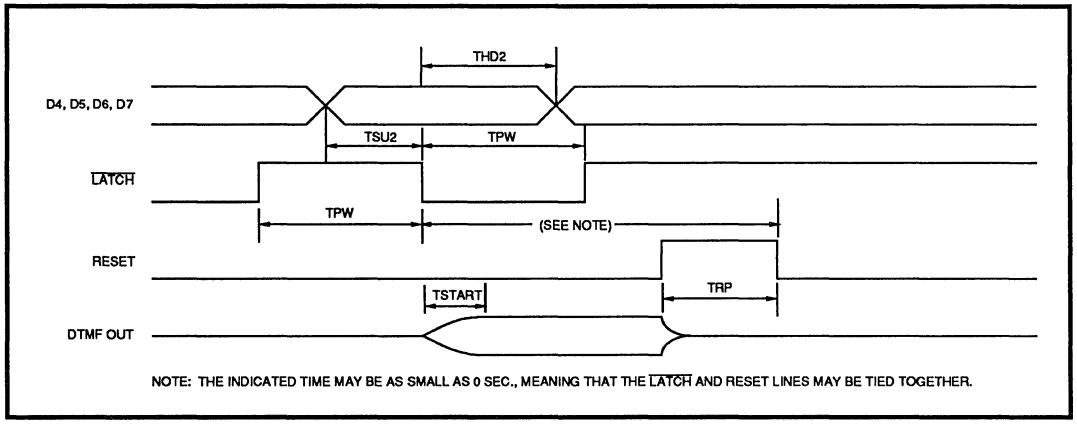
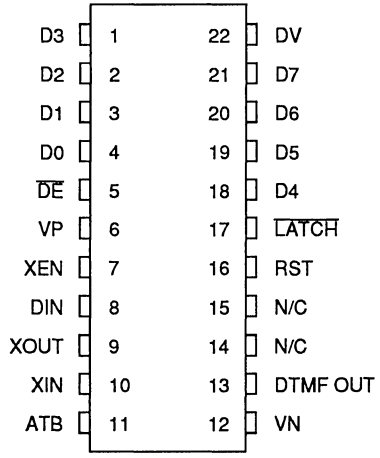


FIGURE 7: DTMF GENERATOR

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



22-Pin DIP

4

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T2089 22-Pin Plastic DIP	SSI 75T2089 - IP	75T2089 - IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 75T2090
DTMF Transceiver and Call Progress Detection

July, 1990

DESCRIPTION

Silicon Systems' SSI 75T2090 is a complete Dual-Tone Multifrequency (DTMF) Transceiver that can both generate and detect all 16 standard Touch-Tone digits. The SSI 75T2090 circuit integrates the performance proven SSI 75T202 DTMF Receiver with a new DTMF generator circuit.

The DTMF Receiver electrical characteristics are identical to the standard SSI 75T202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

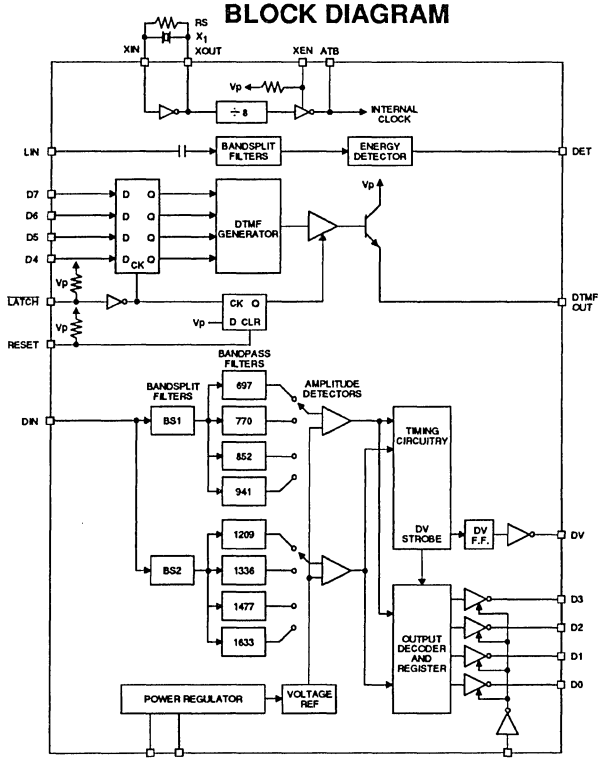
An additional features of the 75T2090 is "imprecise" call progress detector. The detector detects the presence of signals in the 305-640 Hz band. (Continued)

FEATURES

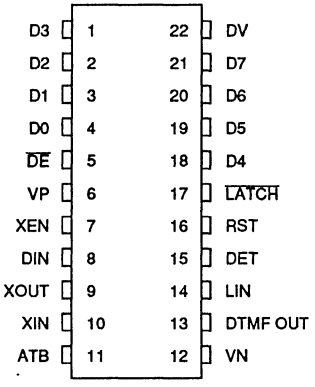
- DTMF Generator and Receiver on one-chip
- 22-pin, 400 mil plastic DIP
- Low-power 5 volt CMOS
- DTMF Receiver exhibits excellent speech immunity
- Three-state outputs (4-bit hexadecimal) from DTMF Receiver
- AC coupled, internally biased analog input
- Latched DTMF Generator inputs
- Analog input range from –32 to –2 dBm (ref 600Ω)
- DTMF output typ. –8 dBm (Low Band) and –5.5 dBm (High Band)
- Uses inexpensive 3.579545 MHz crystal for reference
- Easy interface for microprocessor dialing
- Call progress detection

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The only external components necessary for the SSI 75T2090 are a 3.58 MHz "colorburst" crystal with a parallel 1MΩ resistor. This provides the time base for digital functions and switched-capacitor filters in the device. No external filtering is required.

CIRCUIT OPERATION

RECEIVER

The DTMF Receiver in the SSI 75T2090 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60Hz reject and band-splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

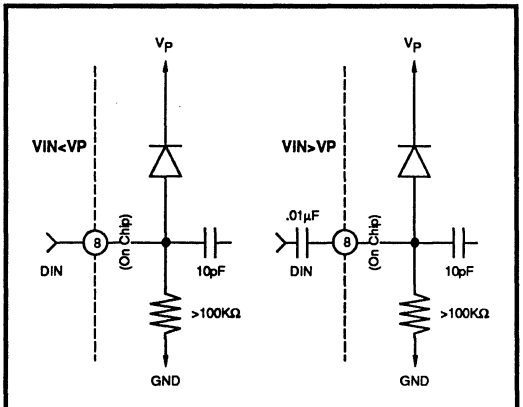


FIGURE 1: Input Coupling

The SSI 75T2090 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T2090 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the SSI 75T2090 depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SSI 75T2090 as shown in Figure 2.

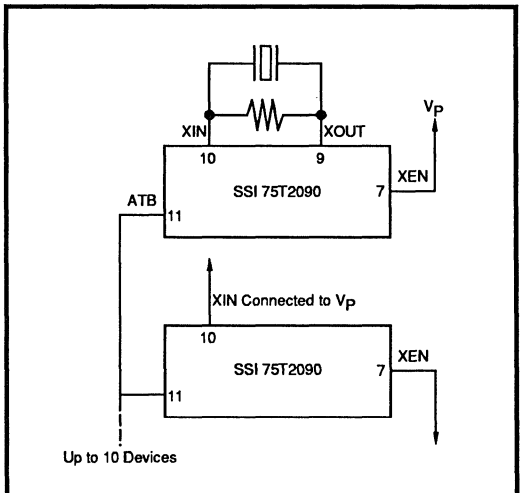


FIGURE 2: Crystal Connections

RECEIVER OUTPUTS AND THE $\overline{DE}$ PIN

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Figure 3 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

	Hexadecimal Code			
Digit In / Out	D7 / D3	D6 / D2	D5 / D1	D4 / D0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

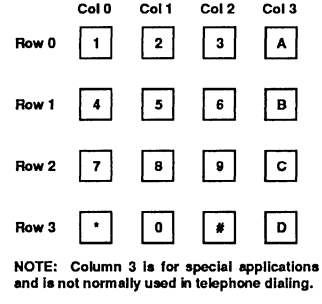
FIGURE 3

GENERATOR

The DTMF generator on the SSI 75T2090 responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{LATCH}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

DIGITAL INPUTS

The D4, D5, D6, D7, $\overline{LATCH}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Figure 4 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits.



NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

FIGURE 4: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697Hz	Column 0 = 1209Hz
Row 1 = 770Hz	Column 1 = 1336Hz
Row 2 = 852Hz	Column 2 = 1477Hz
Row 3 = 941Hz	Column 3 = 1633Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown in Figure 5.

CALL PROGRESS DETECTION

The Call Progress Detector consists of a bandpass filter and an energy detector for turning the on/off cadences into a microprocessor compatible signal.

LIN INPUT

This analog input accepts the call progress signal and should be used in the same manner as the receiver input DIN.

DET OUTPUT

This output is TTL compatible and will be of a frequency corresponding to the various cadences of Call Progress signals such as, on 0.5 sec/off 0.5 sec for a busy tone, on 0.25 sec/off 0.25 sec for a reorder tone and on 0.8-1.2 sec/off 2.7-3.3 sec for an audible ring tone.

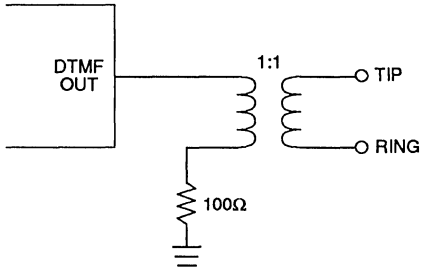


FIGURE 5: DTMF Output

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating above absolute maximum ratings may damage the device.

PARAMETER	RATING	UNIT
DC Supply Voltage (Vp - Vn)	+7	V
Voltage at any Pin (Vn = 0)	-0.3 to Vp + 0.3	V
DIN Voltage	Vp + 0.5 to Vp - 10	V
Current through any Protection Device	±20	mA
Operating Temperature Range	-40 to + 85	°C
Storage Temperature	-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Voltage		4.5		5.5	V
Power Supply Noise (wide band)				10	mV pp
Ambient Temperature		-40		+85	°C
Crystal Frequency (F Nominal = 3.579545MHz)		-0.01		+0.01	%
Crystal Shunt Resistor		0.8		1.2	MΩ
DTMF OUT Load Resistance		100			Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: LIN, DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current*			15	30	mA
Power Dissipation				225	mW
Input Voltage High		0.7Vp			V
Input Voltage Low				0.3Vp	V
Input Current High				10	µA
Input Current Low		-10			µA
Output Voltage High	Ioh = -0.2mA	Vp-0.5			V
Output Voltage Low	Iol = +0.4mA			Vn+0.5	V
* with DTMF output disabled					

DTMF RECEIVER: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection		-32		-2	dBm
Twist Tolerance		-10		+10	dB
60Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone			0	dB*
Speech Immunity	MITEL Tape #CM7290		2		hits
Noise Tolerance	MITEL Tape #CM7290			-12	dB*
Input Impedance		100			kΩ
* Referenced to lowest amplitude tone					

DTMF RECEIVER: Timing Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TON	Tone Time for Detect		40			ms
TON	Tone Time for No Detect				20	ms
TOFF	Pause Time for Redetection		40			ms
TOFF	Pause Time for Bridging				20	ms
TD1	Detect Time		25		46	ms
TR1	Release Time		35		50	ms

DTMF RECEIVER: Timing Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSU1 Data Set Up Time		7			µs
THD1 Data Hold Time		4.2		5.0	ms
Output Enable Time				200	ns
Output Disable Time				200	ns

DTMF GENERATOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Accuracy		-1.0		+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp - Vn = 5.0V				
Low Band		-9.2		-7.2	dBm
High Band		-6.6		-4.6	dBm
Output Distortion	DC to 50kHz			-20	dB

DTMF GENERATOR: Timing Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSTART Start-Up Time				2.5	µs
TSU2 Data Set-Up Time		100			ns
THD2 Data Hold Time		50			ns
TRP RESET Pulse Width		100			ns
TPW $\overline{\text{LATCH}}$ Pulse Width		100			ns

CALL PROGRESS DETECTOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Amplitude for Detection	305Hz-640Hz	-40		0	dBm
Amplitude for No Detecion	305Hz-640Hz			-50	dBm
	f>2200Hz, <160Hz			-25	dBm
Detect Output	Logic 0			.5	V
	Logic 1	4.5			V
"LIN" Input	Max. Voltage	V_{DD}-10		V_{DD}	V
Input Impedance	500Hz	100			kΩ

CALL PROGRESS DETECTOR: Timing Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TON Signal Time for Detect		40			ms
TON Dignal Time for No Detect				10	ms
TOFF Interval Time for Detect		40			ms
TOFF Interval Time fo No Detect				20	ms
TD2 Detect Time				40	ms
TR2 Release Time				40	ms

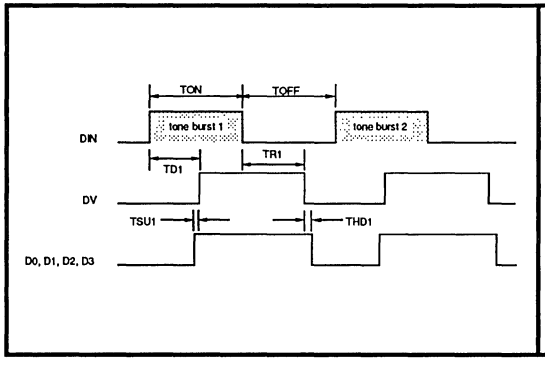


FIGURE 6: DTMF Decoder

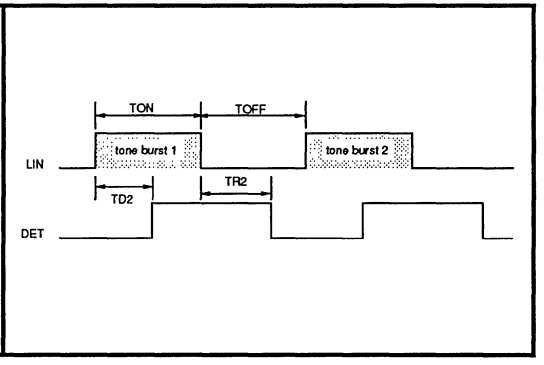


FIGURE 7: Call Progress Detector

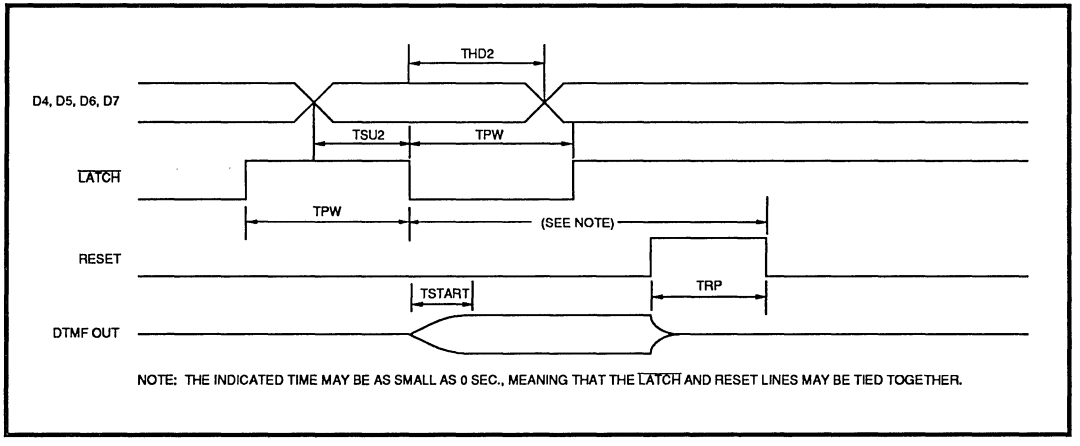
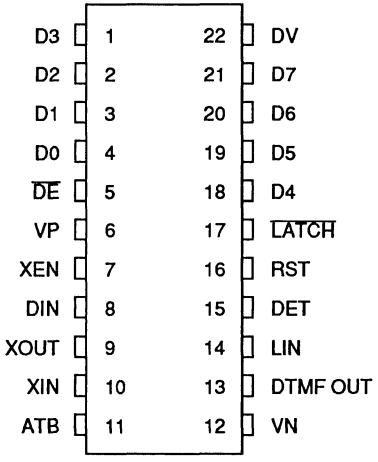


FIGURE 8: DTMF Generator

SSI 75T2090
DTMF Transceiver with Call Progress Detection

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



22-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T2090 22-Pin DIP	SSI 75T2090 - IP	75T2090 - IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 75T2091
DTMF Transceiver with Early Detect & Call Progress Detection

July, 1990

DESCRIPTION

Silicon Systems' SSI 75T2091 is a complete Dual-Tone Multifrequency (DTMF) Transceiver that can both generate and detect all 16 DTMF tone-pairs. The SSI 75T2091 circuit integrates the performance proven SSI 75T203 DTMF receiver with a new DTMF generator circuit.

The DTMF receiver electrical characteristics are identical to the standard SSI 75T203 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

An additional feature of the SSI 75T2091 is "imprecise" call progress detector. The detector detects the presence of signals in the 305-640 Hz band.

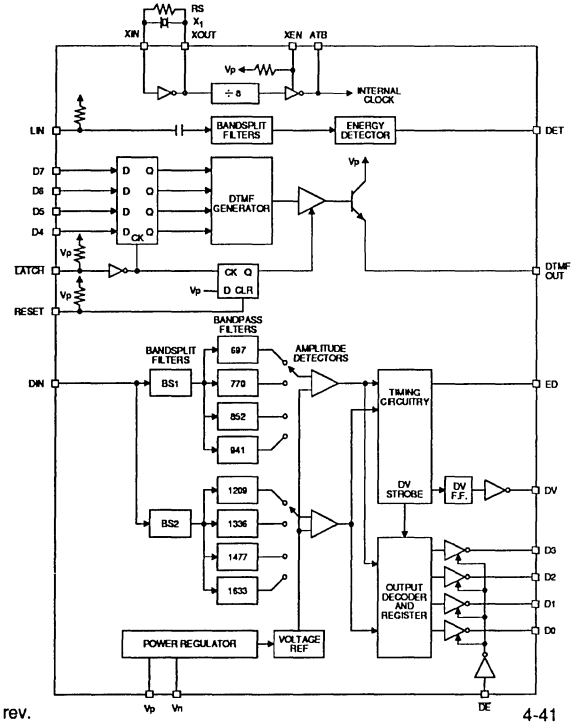
(Continued)

FEATURES

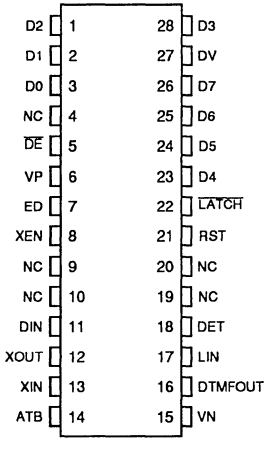
- DTMF Generator and Receiver on one-chip
- Call progress detection
- Early detect output
- DTMF Receiver exhibits excellent speech immunity
- Analog input range from –32 to –2 dBm (ref 600 Ω)
- Three-state outputs (4-bit hexadecimal) from DTMF Receiver
- AC coupled, internally biased analog input
- Latched DTMF Generator inputs
- DTMF output typ. –8 dBm (Low Band) and –5.5 dBm (High Band)
- Easy interface for microprocessor dialing
- Uses inexpensive 3.579545 MHz crystal for reference
- Low-power 5 volt CMOS
- 28-pin DIP or PLCC

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The only external components necessary for the SSI 75T2091 are a 3.58 MHz "colorburst" crystal with a parallel 1MΩ resistor. This provides the time base for digital functions and switched-capacitor filters in the device. No external filtering is required.

CIRCUIT OPERATION

RECEIVER

The DTMF Receiver in the SSI 75T2091 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band-splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

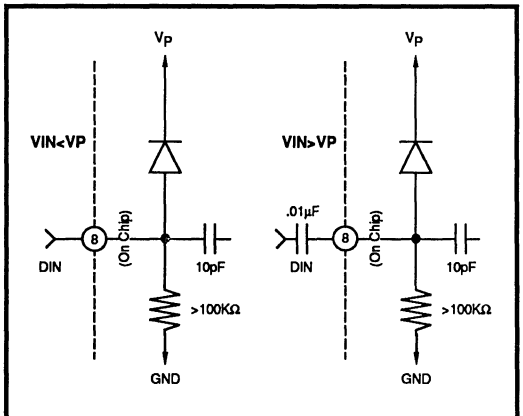


FIGURE 1: Input Coupling

The SSI 75T2091 is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T2091 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the SSI 75T2091 depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock frequency output. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected SSI 75T2091 as shown in Figure 2.

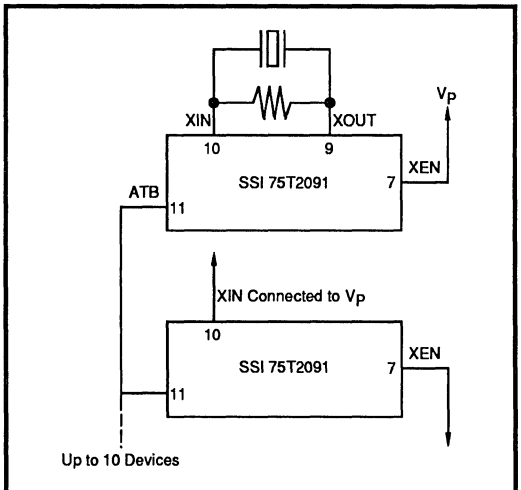


FIGURE 2: Crystal Connections

RECEIVER OUTPUTS AND THE $\overline{DE}$ PIN

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{DE}$ low) and open-circuited (high impedance) when disabled ($\overline{DE}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Figure 3 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

Digit In Out	Hexadecimal Code D7 D3	D6 D2	D5 D1	D4 D0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

FIGURE 3

ED OUTPUT

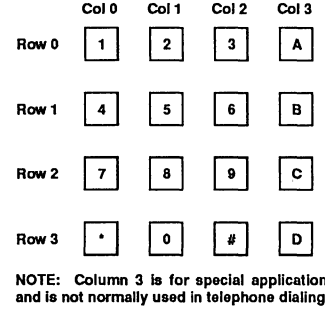
The ED output goes high as soon as the SSI 75T2091 begins to detect a DTMF tone pair and falls when the SSI 75T2091 begins to detect a pause. The D1, D2, D4, and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

GENERATOR

The DTMF generator on the SSI 75T2091 responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{LATCH}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

DIGITAL INPUTS

The D4, D5, D6, D7, $\overline{LATCH}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Figure 4 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits.



NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

FIGURE 4: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697Hz	Column 0 = 1209Hz
Row 1 = 770Hz	Column 1 = 1336Hz
Row 2 = 852Hz	Column 2 = 1477Hz
Row 3 = 941Hz	Column 3 = 1633Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown in Figure 5.

CALL PROGRESS DETECTION

The Call Progress Detector consists of a bandpass filter and an energy detector for turning the on/off cadences into a microprocessor compatible signal.

LIN INPUT

This analog input accepts the call progress signal and should be used in the same manner as the receiver input DIN.

DET OUTPUT

The output is TTL compatible and will be of a frequency corresponding to the various candences of Call Progress signals such as: on 0.5 sec/off 0.5 sec for a busy tone, on 0.25 sec/off 0.25 sec for a reorder tone and on 0.8-1.2 sec/off 2.7-3.3 sec for an audible ring tone.

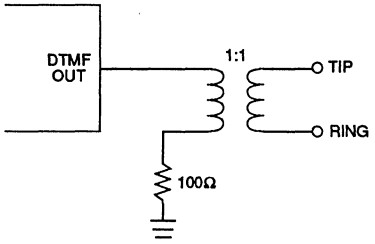


FIGURE 5: DTMF Output

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating above absolute maximum ratings may damage the device.

PARAMETER	RATING	UNIT
DC Supply Voltage (Vp - Vn)	+7	V
Voltage at any Pin (Vn = 0)	-0.3 to Vp + 0.3	V
DIN Voltage	Vp + 0.5 to Vp - 10	V
Current through any Protection Device	±20	mA
Operating Temperature Range	-40 to + 85	°C
Storage Temperature	-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage		4.5		5.5	V
Power Supply Noise (wide band)				10	mV pp
Ambient Temperature		-40		+85	°C
Crystal Frequency (F Nominal = 3.579545MHz)		-0.01		+0.01	%
Crystal Shunt Resistor		0.8		1.2	MΩ
DTMF OUT Load Resistance		100			Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: LIN, DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current*			15	30	mA
Power Dissipation				225	mW
Input Voltage High		0.7Vp			V
Input Voltage Low				0.3Vp	V
Input Current High				10	µA
Input Current Low		-10			µA
Output Voltage High	Ioh = -0.2mA	Vp-0.5			V
Output Voltage Low	Iol = +0.4mA			Vn+0.5	V
* with DTMF output disabled					

DTMF RECEIVER: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection	Each Tone	-32		-2	dBm/tone
Twist Tolerance		-10		+10	dB
60Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone			0	dB*
Speech Immunity	MITEL Tape #CM7290		2		hits
Noise Tolerance	MITEL Tape #CM7290			-12	dB*
Input Impedance		100			KΩ
* Referenced to lowest amplitude tone					

DTMF RECEIVER: Timing Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TON	Tone Time for Detect		40			ms
TON	Tone Time for No Detect				20	ms
TOFF	Pause Time for Redetection		40			ms
TOFF	Pause Time for Bridging				20	ms
TD1	Detect Time		25		46	ms
TR1	Release Time		35		50	ms

DTMF RECEIVER: Timing Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSU1 Data Set Up Time		7			µs
THD1 Data Hold Time		4.2		5.0	ms
TED ED Detect Time		7		22	ms
BER ED Release Time		2		18	ms
Output Enable Time				200	ns
Output Disable Time				200	ns

DTMF GENERATOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Accuracy		-1.0		+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp - Vn = 5.0V				
Low Band		-9.2		-7.2	dBm
High Band		-6.6		-4.6	dBm
Output Distortion	DC to 50kHz			-20	dB

DTMF GENERATOR: Timing Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSTART Start-Up Time				2.5	µs
TSU2 Data Set-Up Time		100			ns
THD2 Data Hold Time		50			ns
TRP RESET Pulse Width		100			ns
TPW $\overline{\text{LATCH}}$ Pulse Width		100			ns

CALL PROGRESS DETECTOR: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Amplitude for Detection	305 Hz-640 Hz	-40		0	dBm
Amplitude for No Detection	305 Hz-640 Hz			-50	dBm
	f>2200 Hz, <160 Hz			-25	dBm
Detect Output	Logic 0			.5	V
	Logic 1	4.5			V
"LIN" Input	Max. Voltage	V_{DD}-10		V_{DD}	V
Input Impedance	500 Hz	100			kΩ

CALL PROGRESS DETECTOR: Electrical Characteristics (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TON	Signal Time for Detect		40			ms
TON	Signal Time for No Detect				10	ms
TOFF	Interval Time for Detect		40			ms
TOFF	Interval Time for No Detect				20	ms
TD2	Detect Time				40	ms
TR2	Release Time				40	ms

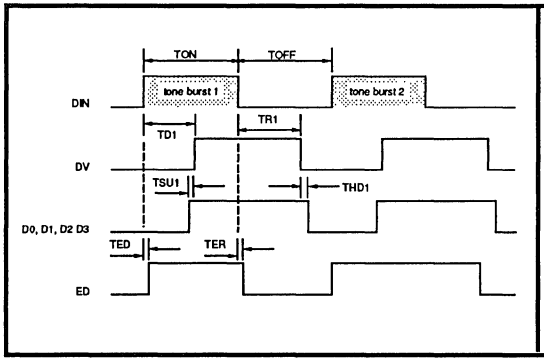


FIGURE 6: DTMF Decoder

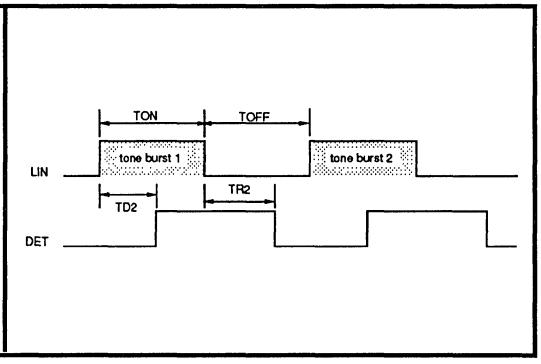


FIGURE 7: Call Progress Detector

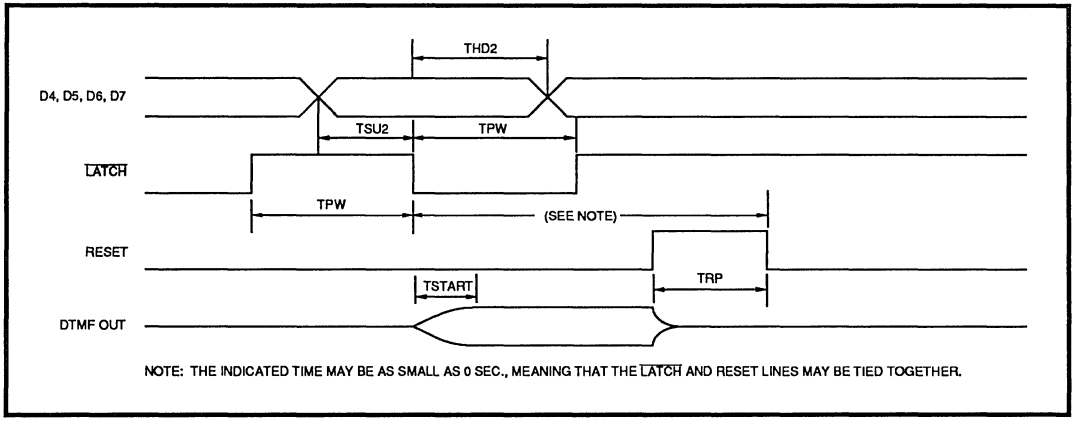
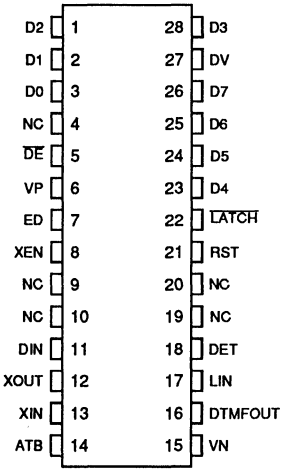


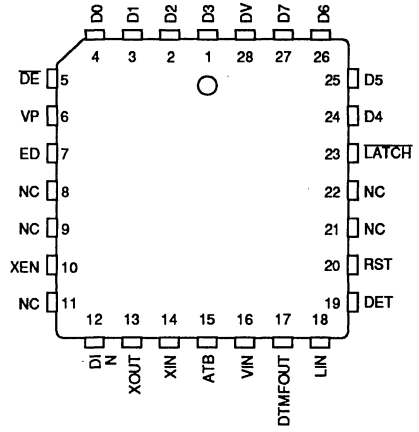
FIGURE 8: DTMF Generator

SSI 75T2091
DTMF Transceiver with Early Detect & Call Progress Detection

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T2091		
28-Pin Plastic DIP	SSI 75T2091 - IP	75T2091 - IP
28-Pin PLCC	SSI 75T2091 - IH	75T2091 - IH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 75T957/957A
DTMF Receiver with Dial Tone Reject Filter

July, 1990

DESCRIPTION

The SSI 75T957/957A combines switched-capacitor and digital frequency measuring techniques to decode Dual-Tone Multifrequency (DTMF) signals to four bit binary data. Dial tone rejection and 60 Hz noise rejection filters are built in. Fabricated as a monolithic integrated circuit using low power CMOS processing, the SSI 75T957/957A is packaged in a 22-pin DIP or 24-pin SO. The SSI 75T957A will operate with a supply range of 5 to 12 volts; the 75T957 is for 5V-only operation. An inexpensive 3.58 MHz television crystal and a resistor are the only external components required. High system density may be achieved by using the clock output of one crystal-connected receiver to drive the time bases of additional receivers.

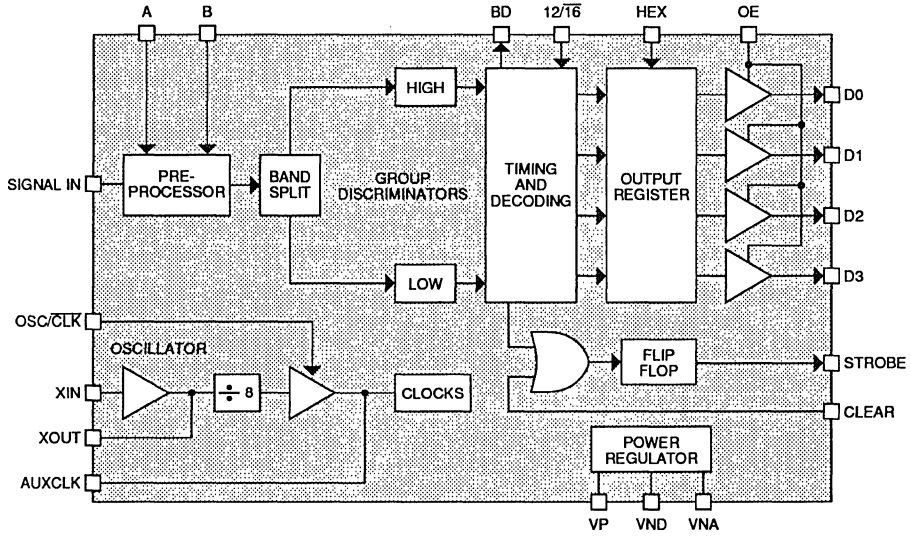
(Continued)

FEATURES

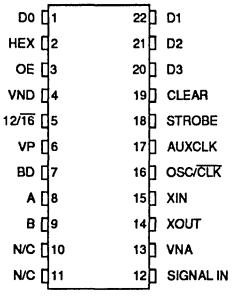
- **Complete DTMF receiver in 22-pin DIP or 24-pin SO**
- **Decodes all 16 DTMF digits**
- **Excellent dial tone and speech immunity**
- **Meets telephone impulse noise immunity standards**
- **Digitally selectable sensitivity to -38 dBm**
- **Selectable 4-bit hexadecimal or binary-coded 2-of-8 output**
- **Fabricated using low-power CMOS technology**
- **Operates at 5V (75T957) or 12V (75T957A)**
- **Second source of Teltone M-957**

4

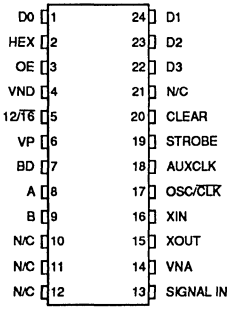
BLOCK DIAGRAM



PIN DIAGRAMS



22-pin DIP



24-pin SO

CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SIGNAL IN input to the SSI 75T957/957A interfaces readily to telephone lines, radio receivers, tape players and other DTMF signal sources. Inputs A and B control sensitivity to a maximum of -38 dBm, while the 12/$\overline{16}$ input determines the signals to be detected. The pre-processing stages of the SSI 75T957/957A filter out dial tone and noise, split the signal into its high frequency group and low frequency group components, and hard limit each component to provide automatic gain control. Four discriminators in each group then detect the individual tones. Post-processing stages of the SSI 75T957/957A time the tone durations and store binary data for outputting as determined by the HEX input. The STROBE output is activated by the presence of valid data in the output register and cleared by the detection of a valid end-of-signal pause or by the CLEAR input. An early signal presence indicator, BD, facilitates applications requiring tone blocking. The data outputs operate with simple logic circuits or microprocessors and are three-state enabled to facilitate bus-oriented architectures.

PIN DESCRIPTION

NAME	22-pin DIP	24-pin SO	TYPE	DESCRIPTION
SIGNAL IN	12	13	I	DTMF input. Timings are shown in Figure 1. Internally biased so that the input signal may be AC coupled. SIGNAL IN also permits DC coupling as long as the input voltage does not exceed the positive supply. Proper coupling is shown in Figure 3. See Table 1 for the frequency pairs associated with each DTMF signal.
12/$\overline{16}$	5	5	I	DTMF signal detection control. When 12/$\overline{16}$ is at logic "1," the SSI 75T957 detects the 12 most commonly used DTMF signals (1 through #). When 12/$\overline{16}$ is at logic "0," the SSI 75T957 detects all 16 DTMF signals (1 through D).
A, B	8, 9	8, 9	I	Binary DTMF signal sensitivity control inputs. A and B select the sensitivity of the SIGNAL IN input to a maximum of -38 dBm.
D3, D2 D1, D0	20, 21 22, 1	22, 23 24, 1	O	Data outputs. When enabled by the OE input, the data outputs provide the code corresponding to the detected digit in the format programmed by the HEX pin. See Table 1. The data outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. Timings are shown in Figure 1.
OE	3	3	I	Output enable. When OE is at logic "1," the data outputs are in the CMOS push/pull state and represent the contents of the output register. When OE is driven to logic "0," the data outputs are forced to the high-impedance or "third" state. Timings are shown in Figure 1.

PIN DESCRIPTION (Continued)

NAME	22-pin DIP	24-pin SO	TYPE	DESCRIPTION
HEX	2	2	I	Binary output format control. When HEX is at logic "1" the output of SSI 75T957 is full, 4-bit binary. When HEX is at logic "0," the output is binary coded 2-of-8. Table 1 shows the output codes.
STROBE	18	19	O	Valid data indication. STROBE goes to logic "1" after a valid tone pair is sensed and decoded at the data outputs. STROBE remains at logic "1" until a valid pause occurs or the CLEAR input is driven to logic "1," whichever is earlier. Once cleared, STROBE will not rise to a logic "1" until a new valid tone (preceded by a valid pause) is detected. Timings are shown in Figure 1.
CLEAR	19	20	I	STROBE control. Driving CLEAR to logic "1" forces the STROBE output to logic "0." When CLEAR is at logic "0," STROBE is forced to logic "0" only when a valid pause is detected. Tie to VNA or VND when not used.
BD	7	7	O	Button down. A logic "1" BD indicates a signal has been detected and is being validated. BD precedes STROBE and data outputs.
XIN, XOUT	15, 14	16, 15	I	Crystal connections. When an auxiliary clock is used, XIN should be tied to logic "1." See Figure 4.
OSC/$\overline{\text{CLK}}$	16	17	I	Time base control. When OSC/$\overline{\text{CLK}}$ is at logic "1," the output of the SSI 75T957's internal oscillator is selected as the time base. When OSC/$\overline{\text{CLK}}$ is at logic "0" and XIN is at logic "1," the AUXCLK input is selected as the time base.
AUXCLK	17	18	O	Auxiliary clock input. When OSC/$\overline{\text{CLK}}$ is at logic "0" and XIN is at logic "1," the AUXCLK input is selected as the SSI 75T957's time base. The auxiliary input must be 3.58 MHz divided by 8 for the SSI 75T957 to operate to specifications. If unused, AUXCLK should be left open.
VNA, VND	13, 4	14, 4	-	Negative analog and digital power supply connections. Separated on the chip for greater system flexibility, VNA and VND should be at equal potential.
VP	6	6	-	Positive power supply connection.
N/C	10, 11	10-12, 21	-	Not connected. These pins have no internal connection and may be left floating.

SSI 75T957/957A TIMING (-40°C ≤ TA ≤ +85°C; 4.5V ≤ VP ≤ 13.2V. Refer to Figure 1.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON}	Tone Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_{OFF}	Pause Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_D	Detect Time		25	-	46	ms
t_R	Release Time		35	-	50	ms
t_{SU}	Data Setup Time		7	-	-	µs
t_H	Data Hold Time		4.2	-	5.0	ms
tcl	Strobe Clear Time		-	160	250	ns
t_{PW}	Clear Pulse Width		200	-	-	ns
t_{BD}	BD Detect Time		7	-	22	ms
t_{BR}	BD Release Time		2	-	18	ms
	Output Enable Time	C_L = 50pF, R_L = 1kΩ	-	200	300	ns
	Output Disable Time	C_L = 35pF, R_L = 500Ω	-	150	200	ns
	Output Rise Time	C_L = 50pF	-	200	300	ns
	Output Fall Time	C_L = 50pF	-	160	250	ns

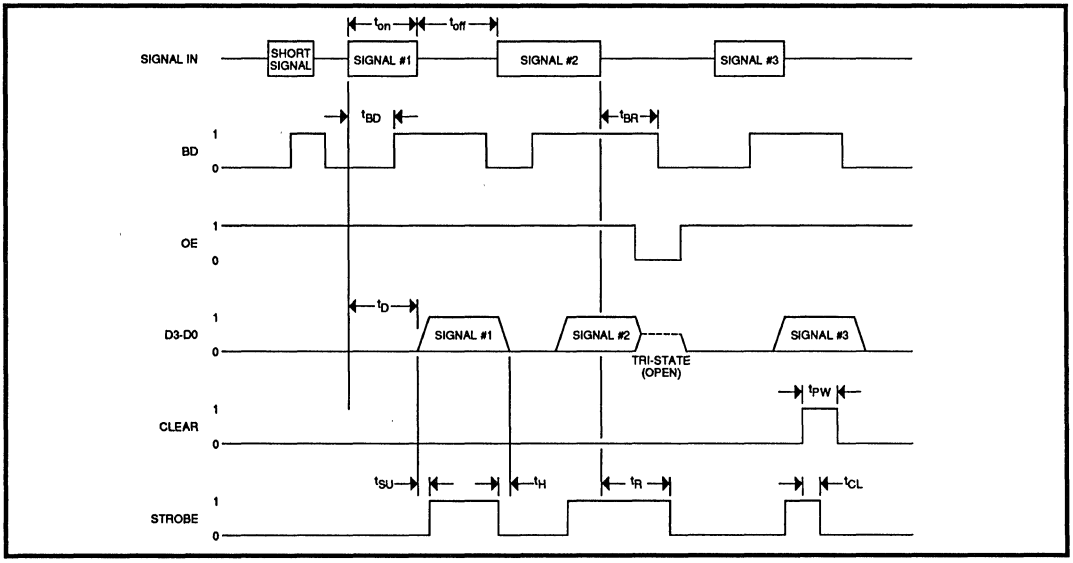


FIGURE 1: Timing Diagram

TABLE 1: DTMF TO BINARY DECODING

DIGIT	LOW-FREQUENCY COMPONENT (Hz)	HIGH-FREQUENCY COMPONENT (Hz)	HEX OUTPUT	BINARY CODED 2-OF-8 OUTPUT
			D3 D2 D1 D0	D3 D2 D1 D0
1	697	1209	0001	0000
2	697	1336	0010	0001
3	697	1477	0011	0010
4	770	1209	0100	0100
5	770	1336	0101	0101
6	770	1477	0110	0110
7	852	1209	0111	1000
8	852	1336	1000	1001
9	852	1477	1001	1010
0	941	1336	1010	1101
*	941	1209	1011	1100
#	941	1477	1100	1110
A	697	1633	1101	0011
B	770	1633	1110	0111
C	852	1633	1111	1011
D	941	1633	0000	1111

Note: The SSI 75T957 detects signals A through D when the 12/$\overline{16}$ input is at logic "0."

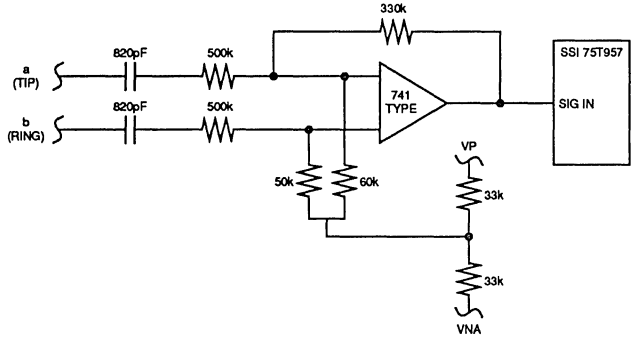
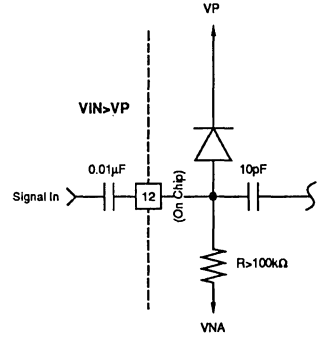


FIGURE 2: Telephone Line Differential Input Interface



NOTE: Coupling capacitor needn't be used when VIN is less than VP.

FIGURE 3: Input Signal Configuration

ABSOLUTE MAXIMUM RATINGS
(Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P	VND=VNA=0V	16.0V
Input Voltage	All inputs except SIGNAL IN	(V_P + 0.5V) to (VND - 0.5V)
SIGNAL IN Voltage		(V_P + 0.5V) to (V_P - 22V)
Storage Temperature		-65° to 150°C
Operating Temperature		-40° to 85°C
Lead Temperature	Soldering, 5 sec.	260°C
Power Dissipation		1W

ELECTRICAL CHARACTERISTICS
(-40°C ≤ T_A ≤ +85°C)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
SIGNAL IN Input Requirements						
Signal Level (per tone) (See Note 1)	V_P=12V	A=0, B=0	-24	-	+6	dBm
		A=1, B=0	-27	-	+3	dBm
		A=0, B=1	-30	-	0	dBm
		A=1, B=1	-	-32	-	dBm
	V_P=5V	A=0, B=0	-32	-	-2	dBm
		A=1, B=0	-35	-	-5	dBm
		A=0, B=1	-38	-	-8	dBm
		A=1, B=1	-	-40	-	dBm
Signal Frequency Deviation with Detection			±(1.5% +2)	±2.5%		Hz
Signal Frequency Deviation without Detection			±3.5%	±3.0%	-	Hz
Twist	See Note 2	-	-	±10	dB	
Gaussian Noise	See Note 3	-	12	A-7	dB	
Dial Tone Level (per tone)	F ≤ 480 Hz; see Note 4		-	-	A+22	dB
Digital Input Requirements (See Note 5)						
Logic 0 Voltage	V_P=12V	0	-	3.6	V	
	V_P=5V	0	-	1.5	V	
Logic 1 Voltage	V_P=12V	8.4	-	12.0	V	
	V_P=5V	3.5	-	5.0	V	

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Digital Output Characteristics (See Note 5)					
Logic 0 Voltage	V_P=12V, Io = 1.0mA	0	-	1.2	V
	V_P=5V, Io = 0.4mA	0	-	0.5	V
Logic 1 Voltage	V_P=12V, Io = -0.5mA	10.8	-	12.0	V
	V_P=5V, Io = -0.2mA	4.5	-	5.0	V
Three-State Leakage		-	-	10.0	µA
Miscellaneous Characteristics					
CMOS Latch-up Voltage	See Note 7	20	-	-	V
SIGNAL IN Input Impedance	F=1kHz||15pF	100k	-	-	Ω
Power Requirements					
Supply Current	V_P=12V	-	20	40	mA
	V_P=5V	-	9	18	mA
Power Dissipation	V_P=12V, see Note 6	-	204	480	mW
(outputs open)	V_P=5V, see Note 6	-	30	90	mW
Power Supply Wide Band Noise	A=0, B=0				
	V_P=12V	-	-	25	mVpp
	V_P=5V	-	-	10	mVpp

Notes:
1. With an ambient temperature of 25°C, the signal duration and signal interval are at minimum, and the signal frequency deviation and twist are at maximum. The unit "dBm" refers to decibels above or below a reference power of one milliwatt into a 600-ohm load. (For example, -24dBm equals 49mVrms.)
2. Twist is defined as the ratio of the level of the high-frequency DTMF component to the level of the low-frequency DTMF component.
3. With an ambient temperature of 25°C, the signal level is at A+5, the signal frequency deviation and twist are at 0, and the signal applied is 50ms off and 50ms on. The A level is the minimum detect level selected.
4. The signal duration and signal interval are at minimum, and the signal frequency deviation and twist are at maximum. The A level is the minimum detect level selected.
5. Logic levels shown are referenced to VND.
6. For an ambient temperature of 25°C.
7. Power supply excursions above this value can cause device damage.

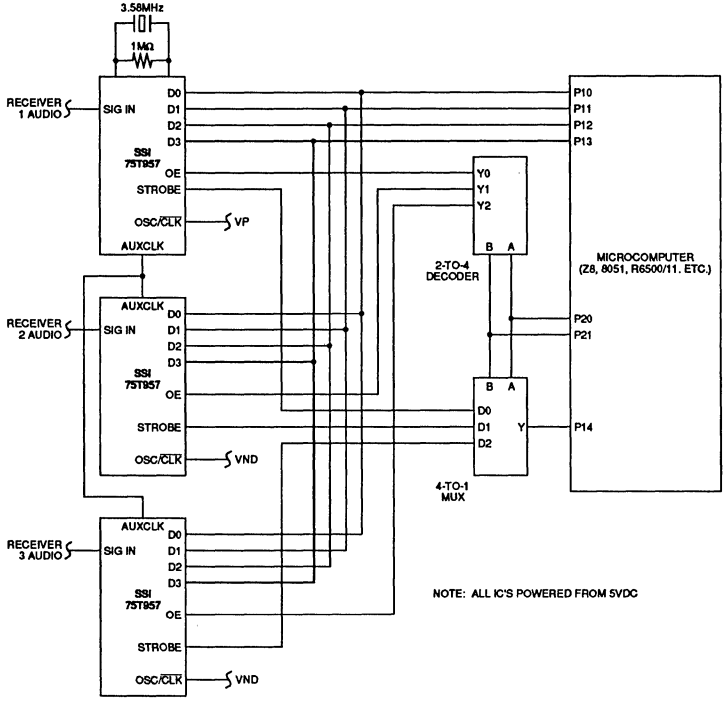


FIGURE 4: Multiple Receiver/Microprocessor Interface

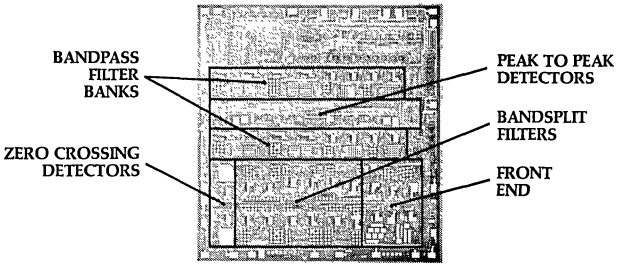
ORDERING INFORMATION

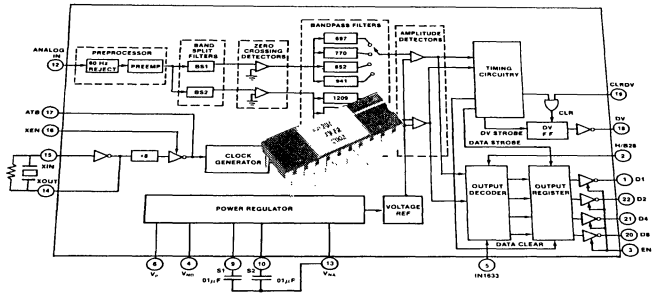
PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T957 22-pin Plastic DIP, 5V-only	SSI 75T957-IP	75T957-IP
SSI 75T957 24-pin SOL, 5V-only	SSI 75T957-IL	75T957-IL
SSI 75T957A 22-pin Plastic DIP, 5-12V operation	SSI 75T957A-IP	75T957A-IP
SSI 75T957A 24-pin SOL, 5-12V operation	SSI 75T957A-IL	75T957A-IL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Application Guide

Monolithic Dual-Tone Multi-Frequency (DTMF) Receivers





4

INTRODUCTION

The Silicon Systems integrated DTMF Receivers and Transceivers are complete Touch-Tone™ detection and generation systems. Each can operate in a stand-alone mode for the majority of telecommunications applications, thereby providing the most economical implementation of DTMF signaling systems possible. Each combines precision active filters and analog circuits with digital control logic on a monolithic CMOS integrated circuit. SSI DTMF chip use is straightforward and the external component requirements are minimal. This application guide describes device operation, performance, system requirements and typical application circuits for the SSI DTMF chips.

HOW THE SILICON SYSTEMS DTMF CIRCUITS WORK

GENERAL DESCRIPTION OF OPERATION

The task of a DTMF Receiver is to detect the presence of a valid DTMF signal on a telephone line or other transmission medium. The presence of a valid DTMF signal indicates a single dialed digit; to generate a valid digit sequence, each DTMF signal must be separated by a valid pause.

Table 1 gives the established Bell system standards for a valid DTMF signal and a valid pause. The SSI DTMF Receivers meet or exceed these standards.

PARAMETER	VALUE
One Low-Group Tone, and	697, 770, 852 or 941 Hz
One High-Group Tone	1209, 1336, 1477 or 1633 Hz
Frequency Tolerance	fo ± (1.5% + 2 Hz)
Amplitude Range	–24 dB ≤ A ≤ 6 dBm @ 600Ω (Dynamic Range 30 dB)
Relative Amplitude (Twist)	$-8\,dB \le \frac{\text{High Group Tone}}{\text{Low Group Tone}} \le +4\,dB$
Duration	40 ms or longer
Inter-tone Pauses	40 ms or longer

Table 1: Bell System Standards

GENERAL DESCRIPTION (Continued)

Similar device architecture is used in all SSI DTMF Receivers. Figure 1 shows the SSI 75T202 Block Diagram. This architecture is implemented in all Silicon Systems single chip receivers, as well as SSi Transceivers. In general terms, the detection scheme is as follows: The input signal is pre-filtered and then split into two bands, each of which contains only one DTMF tone group. The output of each band-split filter is amplified and limited by a zero-crossing detector. The limited signals, in the form of square waves, are passed through tone frequency bandpass filters. Digital logic is then used to provide detector sampling and determine detection validity, to present the digital output data in the correct format, and to provide device timing and control.

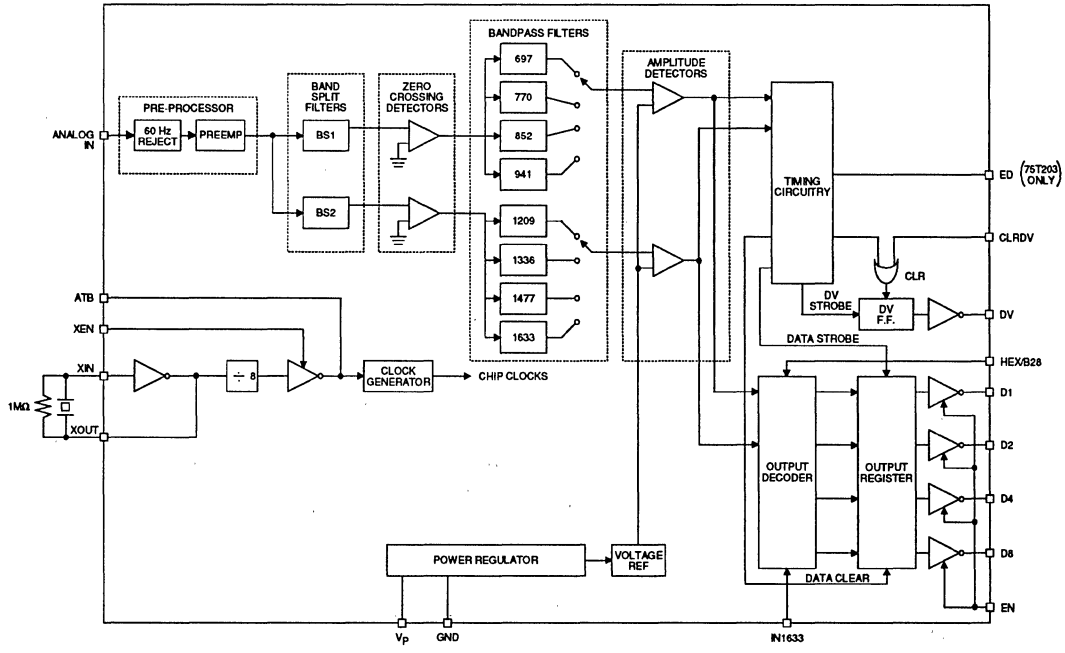


Figure 1: SSI 75T202 Block Diagram

PERFORMANCE CONSTRAINTS

SPEECH IMMUNITY AND NOISE TOLERANCE

The two largest problems confronting a DTMF Receiver are:

1) Distinguishing between valid DTMF tone pairs and other speech or stray signals that contain DTMF tone pair frequencies. This is referred to as Speech Immunity.

2) Detecting valid tone pairs in the presence of noise, which is typically found in the telephone (or other transmission medium) environment. This is referred to as Noise Tolerance.

The SSI DTMF Receivers use several techniques to distinguish between valid tone pairs and other stray signals. These techniques are explained in later sections. Briefly, the techniques are:

1) Pre-filtering of audio signal. Removes supply noise and dial tone from input audio signal and emphasizes the voice frequency domain.

2) Zero-cross detection. Limits the acceptable level of noise during detection of a tone pair. Important for speech rejection.

3) Valid tone pair/pause sampling. Samples the detection filters and checks for consistency before

DETAILED DESCRIPTION OF OPERATION

AUDIO PREPROCESSOR

The Audio Preprocessor is an analog filter that band limits the input analog signal between 500 Hz and 6 kHz. In addition, it emphasizes the 2 kHz to 6 kHz voice region.

Band limiting suppresses power supply and dial tone frequencies, and high frequency noise. The emphasized voice region helps to equalize the audio response since many phone lines tend to roll off at about 1 kHz. In addition, preservation of the upper voice frequencies is important in providing speech immunity.

TONE BAND SPLITTING

After the analog signal is preprocessed, it is then split into two bands, each of which contains only one DTMF tone group. The band-split filters are actually band-stop filters to maintain all frequencies except the *other* tone group; this is done to maintain all analog information to enhance speech immunity but not allow the other tone group to act as interfering noise for the band being detected. These band-stop filters have "floors" that limit the amount of tone pair twist which further enhances speech immunity. See device data sheets for acceptable twist limits.

ZERO-CROSSING DETECTORS

The output of each band-split filter is amplified and limited by a zero-crossing detector (limiter). The function of the zero-crossing detector is to produce a square wave at the prime frequency emanating from the band-split filter. If a pure tone is not present, as in the case of voice or other interfering noise, a rectangular wave with a variable period will result. Proportional to the interference, the limiter output power is spread over a broad frequency range as the zero crossings "dither." When a high level of noise or speech occurs, no single bandpass filter pair will contain significant power long enough to result in a tone detection. On the other hand, when a pure DTMF tone exists with acceptable noise levles, the output of the limiter will not have any significant dither and tone detection will occur. The zero-crossing detector also acts as AGC (Automatic Gain Control) in that the output amplitude is independent of input amplitude; this additionally establishes an acceptable signal-to-noise ratio not dependent on tone amplitude.

BANDPASS FILTERS & AMPLITUDE DETECTORS

The bandpass filters perform tone frequency discrimination. Their responses are tailored so that if the frequency of the limited square wave from the zero-crossing detector is within the tone frequency tolerance, the fitler output will exceed the amplitude detector threshold. The amplitude detectors are interrogated periodically by the digital control circuitry to acertain the presence of only one tone in each band for the required duration. In a similar fashion, valid pauses are measured by the absence of valid tone pairs for the specified time.

TIMING AND LOGIC

During the qualification process, the output decoder gererates the proper digital code for the received DTMF tone pair. After the fidelity and duration of this signal have been verified, the timing circuitry latches this code into the output register and raises the data valid (DV) flag.

The only precision external element needed for the SSI DTMF Receivers is a 3.58 MHz parallel resonant crystal (color-burst frequency) with a .01% tolerance for the on-board oscillator. A 1 MΩ 10% resistor should be connected in parallel with the crystal. This generates the precise clock for the filters and for the logic timing and control of the chip.

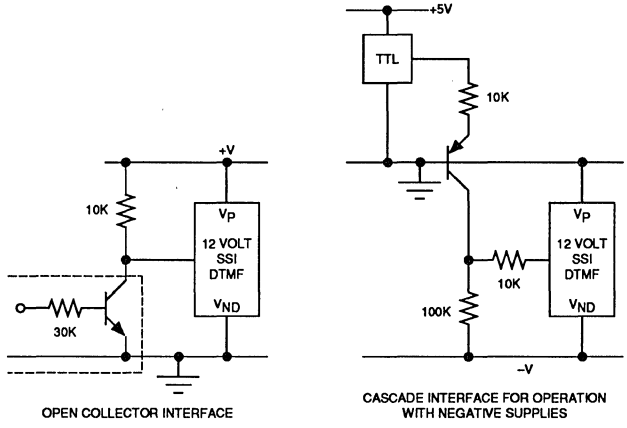


Figure 2: Interface Circuits for Conversion from TTL Output Levels to 12V SSI DTMF Input Levels

CIRCUIT IMPLEMENTATION

Standard CMOS technology is used for the entire circuit. Logic functions use standard low-power circuitry while the analog circuits use precision switched-capacitor-filter technology.

HOW TO USE THE SSI DTMF RECEIVERS

PRECAUTIONS

Although static protection devices are provided on the high-impedance inputs, normal handling precautions observed for CMOS devices should be used.

All CMOS parts are prone to a destructive latch-up mode. This behavior is inherent to these parts due to their physical structure. The latch-up mode can best be described as a low impedance, high current state existing between the power supply connections on a CMOS chip. This is also referred to as triggering of parasitic SCR behavior.

The most common cause of a latch-up mode is operating a CMOS part outside its rated power supply voltage. This over-voltage need not be applied at power supply pins only to cause latch-up. Latch-up can occur when over-voltage is applied at any input or output. For the SSI DTMF Receivers & Transceivers, the pin voltages should be constrained to the range between VN – 0.5V and VP + 0.5V (except the analog input pin whose conditions are discussed below). Clamping diodes should be utilized wherever necessary to ensure that voltage ratings are not exceeded.

Another cause for latch-up is fast dv/dt transients affecting the chip. These transients are encountered in applications that require the connection/disconnection of "live" boards. While these applications are very rare and their implementation is best avoided, it must be mentioned that whenever they are necessary, they present a severe environment for CMOS parts. Care must be taken in such instances to ensure that ground planes and rails are connected first and disconected last. This will go a long way in eliminating voltage transients.

Voltage transients that exist on power lines must also be eliminated. High voltage transients caused by switching of high current devices can trigger latch-up. High frequency decoupling is a requirement for the proper operation of the SSI DTMF devices. A 0.01µF to a 0.1µF ceramic decoupling capacitor should be connected to the power supply pin at the chip.

POWER SUPPLY

Excessive power supply noise should be avoided, and to aid the user in this regard, power supply hook-up options are provided on some devices.

Since the digital circuitry of the devices possess the high noise immunity characteristics of CMOS logic, it is the analog section that is affected most by power supply noise. On those SSI DTMF Receivers that have separate Analog Negative and Digital Negative supply connections (grounds), namely VNA and VND, an unfiltered supply may be used at VND. It is necessary that VND and VNA differ no more than 0.5V.

The analog circuitry of the devices require low power supply noise levels as specified on the device data sheet. The effects of excessive power supply noise are decreased tone amplitude sensitivity and less tone detection frequency bandwidth. Power supply noise can be significantly reduced by decoupling the chip with a 0.1µF

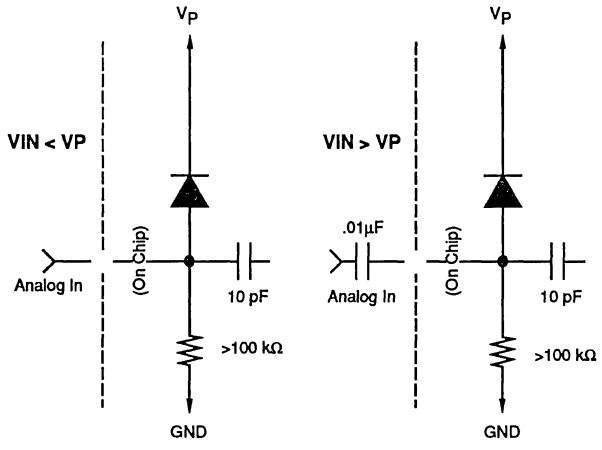


Figure 3: Direct and AC Coupled Configurations

ceramic capacitor. Power supply noise effects will be slightly less if the analog input is referenced to VP. This is normally accomplished by connecting VP to ground and utilizing a negative power supply.

DIGITAL INPUTS

The digital inputs are directly compatible with standard CMOS logic devices powered by VP and VN (or VND). The input logic levels should swing within 30% of VP or VN to insure detection. Any unused input must be tied to VN or VP. Figure 2 shows methods for interfacing TTL outputs to 12V SSI DTMF Receivers.

ANALOG INPUT

The analog input is the signal input pin for the devices, and is specially biased to facilitate its connection to external circuitry, as shown in Figure 3. The signal level at the analog input pin must not exceed the positive supply as stated on the device data sheets. If this condition cannot be guaranteed by the external circuitry, the signal must be AC coupled into the chip with a .01µF ± 20% capacitor.

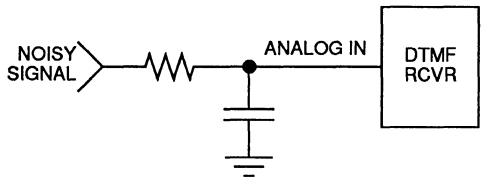
ANALOG INPUT NOISE

The SSI DTMF Receivers will tolerate wide-band input noise of up to 12 dB below the lowest amplitude tone component during detection of a valid tone pair. Any single interference frequency (including tone harmonics) between 1 kHz and 6 kHz should be at least 20 dB below the lowest amplitude tone component. Adherence to these conditions will ensure reliable detection and full tone detection frequency bandwidth. Because of the internal band limiting, noise with frequencies above 8 kHz can remain unfiltered. However, noise near the 56 kHz internal switched-capacitor-filter sampling frequency will be aliased (folded back) into the audio spectrum; noise above 28 kHz therefore should be low-pass filtered with a circuit as shown in Figure 4 using a cut-off frequency (fc) of 6.6 kHz.

A 1 kHz cut-off frequency filter can be used on "normal" phone lines for special applications. When a phone line is particularly noisy, tone pair detection may be unreliable. A 1 kHz low pass filter will remove much of the noise energy but maintain the tone groups; however, a decreased speech immunity will result. This usage should only be considered for applications where speech immunity is not important, such as control paths that carry no speech.

Some DTMF tone pair generators output distorted tones which the SSI DTMF Receivers may not detect reliably (inexpensive extension telephones are an example). Most of the interfering harmonics of these may be removed by the use of a 3 kHz low-pass filter as in Figure 4. Some speech immunity degradation will result. It should be mentioned that when using low-pass filters, a higher cut-off frequency will preserve more of the speech immunity advantages.

The SSI DTMF Receivers provide superior speech immunity and noise rejection. The analog signals are subjected to stringent criteria and rigorous qualification in order to assure that only true DTMF tone pairs are detected and decoded properly. Stray signal and noise with sufficient amplitude will cause a DTMF receiver to disqualify a DTMF tone pair.



F_C (kHZ)	R (kΩ) (±5%)	C (µF) (±20%)
1.0	1.6	0.1
3.1	5.1	.01
6.6	2.4	.01

SUGGESTED COMPONENT VALUES

Figure 4: Filter for Use in Noisy Environments

ANALOG INPUT NOISE (Continued)

Such a condition can be occasionally encountered when using DTMF "beepers." Beepers are normally used to transmit DTMF signals from dial-pulse phones. It has been observed that the non-linearity in the response of carbon microphones in telephone handsets introduces intermodulation products, which actually produce new frequency components. These components happen to fall directly into the useful bandwidths of some of the basic tones that the receiver must detect. Because of the presence of these components (normally referred to as third-tone) with a valid DTMF tone, detection is disabled. To inhibit the more common higher frequency third tones from arriving to the receiver, the circuit shown in Figure 5 is suggested.

TELEPHONE LINE INTERFACE

In applications that use an SSI DTMF Receiver to decode DTMF signals from a phone line, a DAA (Direct Access Arrangement) must be implemented. Equipment intended for connection to the public telephone network must comply with and be registered in accordance to FCC Part 68. For PBX applications refer to EIA Standard RS-464.

Some of the basic guidelines are:

1) Maximum voltage and current ratings of the SSI DTMF Receivers must not be exceeded; this calls for protection from ringing voltage, if applicable, which ranges from 80 to 120V RMS over a 20 to 80 Hz frequency range.
2) The interface equipment must not breakdown with high-voltage transient tests (including a 2500V peak surge) as defined in the applicable document.
3) Phone line termination must be less than 200Ω DC and approximately 600Ω AC (200-3200 Hz).

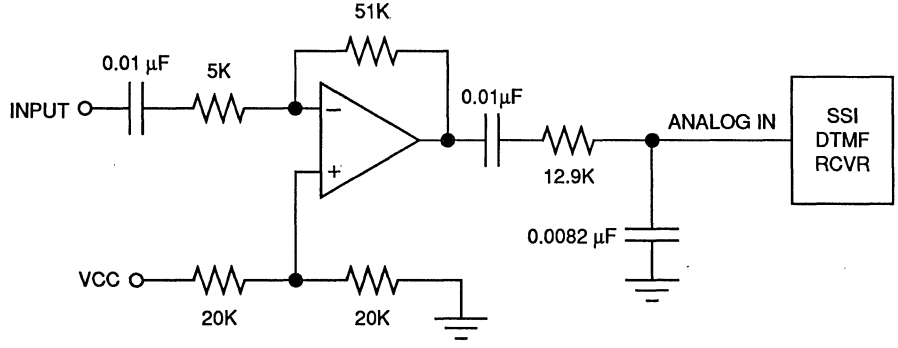


Figure 5: Filter for Use in Environments where a Third Tone Exists

4) Termination must be capable of sustaining phone line lop current (off-hook condition) which is typically 18 to 120 mA DC.
5) The phone line termination must be electrically balanced with respect to ground.
6) Public phone line termination equipment must be registered in accordance to FCC Part 68 or connected through registered protection circuitry. Registration typically takes about six months.

Ready made DAA devices are also available. One source is Cermetek Microelectronics, Sunnyvale, California.

Figure 6 shows a simplified phone line interface using a 600Ω 1:1 line transformer. Transformers specially designed for phone line coupling are available from many transformer manufacturers.
Figure 7 shows a more enhanced version of Figure 6. These added features include:

1) A 150V surge protector to eliminate high voltage spikes.
2) A Texas Instruments TCM 1520A ring detector, optically isolated from the supervisory circuitry.
3) Back-to-back Zener diodes to protect the DTMF (and optional multiplexer Op-Amp) from ringer voltage.

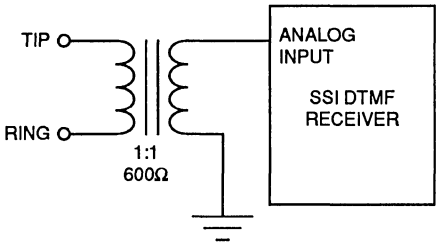


Figure 6: Simplified Phone Line Interface

4) Audio multiplexer which allows voice or other audio to be placed on the line (a recorded message, for example) and not interfere with incoming DTMF tone detection.

An integrated voice circuit may also be implemented for line coupling, such as the Texas Instruments TCM 1705A, however, this approach is typically more expensive than using a transformer as shown below.

4

OUTPUTS

The digital outputs of the SSI DTMF Receivers (except XOUT) swing between VP and VN (or VND) and are fully compatible with standard CMOS logic devices powered

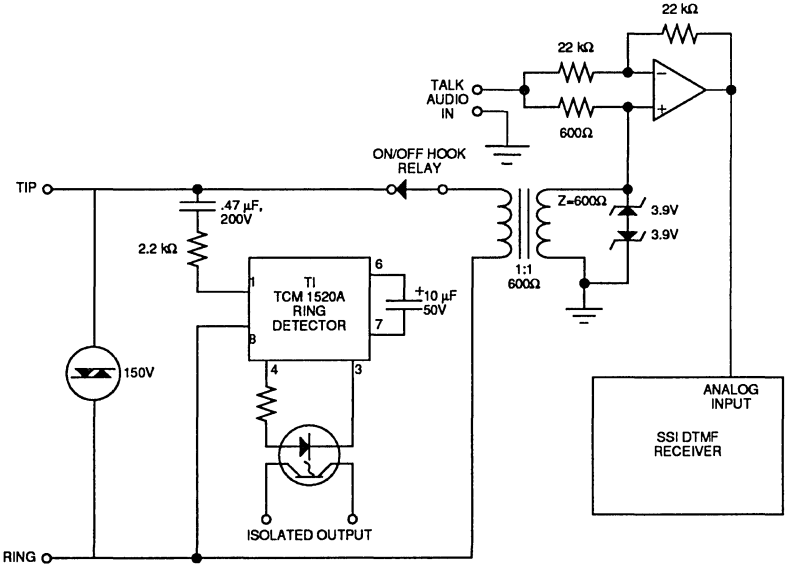


Figure 7: Full Featured Phone Line Interface

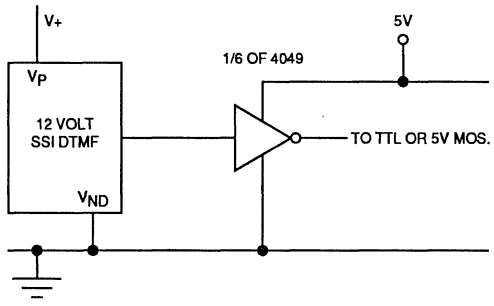


Figure 8: SSI 12V DTMF to TTL Level Interface

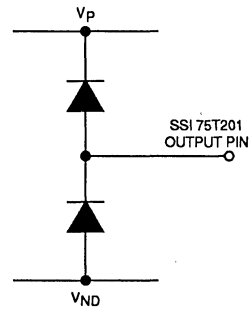


Figure 9: Equivalent Circuit of SSI DTMF Receiver Data Output In High Impedance State

from VP and VN. The 5V DTMF devices will also interface directly to LSTTL. The 12V DTMF devices can interface to TTL or low voltage MOS with the circuit in Figure 8.

Data Outputs D8, D4, D2 and D1 are three-state enabled to facilitate interface to a three-state bus. Figure 9 shows the equivalent circuit for the data outputs in the high impedance state. Care must be taken to prevent either substrate diode in Figure 9 from becoming forward biased or damage may result.

TIMING

Within 40 ms of a valid tone pair appearing at the DTMF Receiver Analog Input, the Data Outputs D8, D4, D2 and D1 will become valid. SSI 75T201 timing and specifications are shown in Figure 10 and Table 2 respectively (refer to the device data sheet for other timing diagrams). Seven microseconds after the data outputs have become valid DV will be raised. DV will remain high and the outputs valid while the valid tone pair remains present. Within 40 ms after the tone pair stops, the DTMF will recognize a valid pause. DV is lowered approximately 45 ms following the end of the tone pair, and the data outputs all set to zero 4.56 ms following Dv going low. DV will strobe at least for the same duration as the received tone pair.

SYSTEM INTERFACE

Provision has been made on the SSI DTMF Receivers for handshake interface with an outside monitoring system. In this mode, the DV strobe is polled by the monitoring system at least once every 40 ms to determine whether a new valid tone pair has been detected. If DV is high, the coded data is stored in the monitoring system and the CLRDV is pulsed high. With some systems operating in the handshake mode, it may be desirable to know when a valid pause has occurred. Ordinarily this would be indicated by the falling edge of DV. However, in the handshake mode, DV is cleared by the monitoring system each time a new valid tone pair is detected and, therefore, cannot be used to determine when a valid pause is detected. The detection of a valid pause in this case may be observed by detecting the clearing of the Data Outputs. Since, in hexadecimal format (the mode normally used with a handshake interface), the all zero state represents a commonly unused tone pair (D), the detection of a valid pause may be detected by connecting a four-input NOR gate to the device outputs and sensing the all zero state.

TIME BASE

The SSI DTMF Receivers contain an on-chip oscillator for a 3.5795 MHz parallel resonant quartz crystal or ceramic resonator. The crystal (or resonator) is placed between XIN and XOUT in parallel with a 1 MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the oscillator, the tone detect band frequency tolerance is proportional to the time base tolerance. The SSI DTMF Receiver frequency response and timing is guaranteed with a time base accuracy of at least ± 0.01%. To obtain this accuracy the CTS Part No. MP036 or Workman Part No. CY1-C or equivalent quartz crystal is recommended. In less critical applications a suitable ceramic resonator may be implemented.

The use of a ceramic resonator requires the addition of two 30 pF ± 10% capacitors; one between XIN and VN (or VND) and the other between XOUT and VN (or VND). Extra caution should be used to avoid stray capacitance on the resonant circuit when using a ceramic resonator instead of a quartz crystal.

When the oscillator is connected as above and XEN is tied high, the ATB (Alternate Time Base) pin delivers a square wave output at one-eighth the oscillator frequency (447.443 kHz nominal). The ATB pin can be converted to a time base input by tying XEN low; ATB can

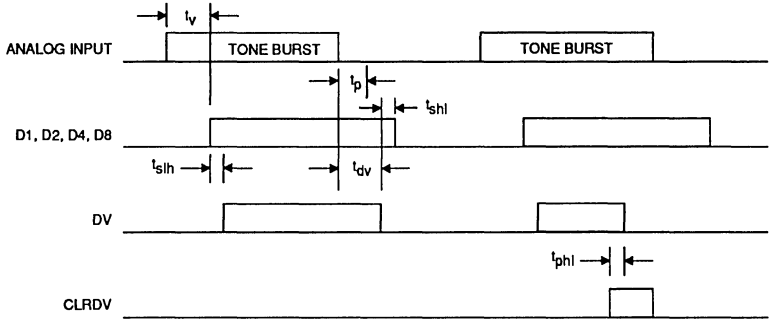


Figure 10: SSI 75T201 Timing Diagram

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
tv	Tone Detection Time		20	25	40	ms
tslh	Data Overlap of DV Rising Edge	CLRDV = VND, EN = VP	7			µs
tp	Pause Detection Time		25	32	40	ms
tdv	Time between end of Tone and Fall of DV		40	45	50	ms
tshl	Data overlap of DV Falling Edge		4	4.56	4.8	ms
tphl	Prop. Delay: Rise of CLRDV to fall of DV	Cl = 300 pF Measured at 50% points			1	µs
	Output Enable Time	Cl = 300 pF, Rl = 10K See Note 1			1	µs
	Output Disable Time	Cl = 300 pF, Rl = 1K ΔV = 1V, See Note 2			1	µs
	Output 10-90% Transition Time	Cl = 300 pF			1	µs

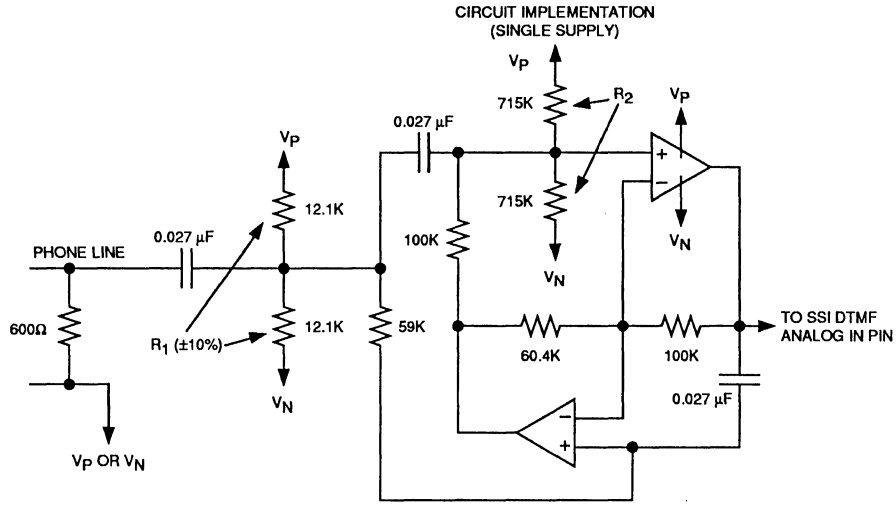
Note 1: Measured from 50% point of Rising Edge of EN to the 50% point of the data output with Rl to opposite rail.

Note 2: Measured from 50% point of Falling Edge of EN to time at which output has changed 1V with Rl to opposite rail.

Table 2: SSI 75T201 Timing Specifications (–40°C ≤ TA ≤ +85°C, VP – VND = VP – VNA = 12V ± 10%)

then be externally driven from another device such as the ATB output of another DTMF. No crystal is required for the ATB input device; XIN must be tied high if unused. Several SSI DTMF Receivers can be driven with a single crystal (refer to device data sheet for fan-out limit).

XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. If a 3.58 MHz clock is needed for more than one device and it is desirable to use only one resonant device, an outside inverter should be used for the time base, buffered by a second inverter or buffer. The buffer output would then drive XIN of the SSI DTMF Receiver as well as the other device(s); XOUT must be left floating and XEN tied high.



Note: All resistors 1%, all caps 5%, unless noted, op-amps: 1/2 LM1458 or equivalent

Figure 11: Dial Tone Reject Filter

DIAL TONE REJECTION

The SSI DTMF Receivers incorporate enough dial tone rejection circuitry to provide dial tone tolerance of up to 0 dB. The SSI 75T957 Receiver has on-board circuitry that provides 22 dB dial tone tolerance. Dial tone tolerance is defined as the total power of precise dial tone (350 Hz and 440 Hz as equal amplitudes) relative to the lowest amplitude tone in a valid tone pair. The filter of Figure 11 may be used for further dial tone rejection. This filter exhibits an elliptic highpass response that provides a minimum of 18 dB rejection at 350 Hz, and 24 dB rejection at 440 Hz so long as the component tolerances indicated are observed. The DTMF on-chip filter rejects 350 Hz at least 6 dB more than 440 Hz. Therefore, employing the filter of Figure 11 yields a dial tone tolerance of +24 dB.

PRINTED CIRCUIT BOARD IMPLEMENTATION

The SSI DTMF Receivers are analog in nature and should be treated as such; circuit noise should be kept to a minimum. To be certain of this, all input and output lines should be kept away from noise sources (high frequency data or clock lines); this is especially true for the Analog Input. Noise in the ground or power supply lines can be avoided by running separate traces to supportive logic circuits or by running thicker (lower resistance) busses. Capacitance power supply bypassing should be performed at the device. Refer to the Power Supply section above.

PERFORMANCE DATA

A portion of the final SSI DTMF Receiver device characterization uses the Mitel CM7290 tone receiver test tape. The evaluation circuit shown in Figure 12 was used to characterize the SSI 75T201. The speed and output level of the tape deck must be adjusted so that the calibration tone at the beginning of the tape is at exactly 1000 Hz and 2V rms.

The Mitel tape tests yield similar results on all of the SSI DTMF Receivers. Test results for the SSI 75T201 are summarized in Table 3. In short, the measured performance data demonstrates that the SSI DTMF Receivers are monolithic realizations of a full "central office quality" DTMF Receiver.

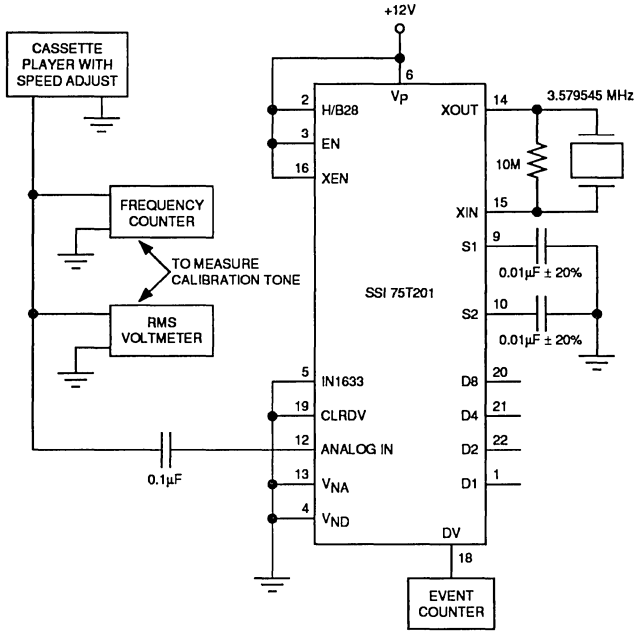


Figure 12: Circuit for Receiver Evaluation

TEST #	RESULTS
2a, b	B.W. = 5.0% of fo
2c, d	B.W. = 5.0% of fo
2e, f	B.W. = 5.3% of fo
2g, h	B.W. = 4.9% of fo
2i, j	B.W. = 5.0% of fo
2k, l	B.W. = 5.3% of fo
2m, n	B.W. = 5.3% of fo
2o, p	B.W. = 4.8% of fo
3	160 decodes
4	Acceptable Amplitude Ratio (Twist) = –19.1 dB to +15.2 dB
5	Dynamic Range = 32.5 dB
6	Guard Time = 23.3 ms
7	100% Successful Decodes at N/S Ratio of –12 dBV
8	2-3 Hits Typical on Talk-Off Test

Table 3: Mitel #CM7290 Tape Test Results for SSI 75T201 (Averaged for 10 parts)

APPLICATIONS

CREATING HEXADECIMAL "0" OUTPUT UPON DIGIT "0" DETECTION

To be consistent with pulse-dialing systems, the SSI DTMF Receivers provide a hexadecimal "10" output upon the detection of a digit "0" tone pair when in the hexadecimal code format. However, some applications may instead require a hexadecimal "0" with a digit "0" detection. The circuit of Figure 13 shows an easy method to recode the hexadecimal outputs to do this using only 4 NOR gates.

Note that this circuit will not give proper code for the " * ", "B", or "C" digits and will cause both digits "D" and "0" to output hexadecimal "0." This circuit should therefore be considered for numeric digits only. The output code format is shown in Table 4.

This circuit is useful for applications that require a display of dialed digits; the digit display usually requires a hexadecimal "0" input for a "0" to be displayed.

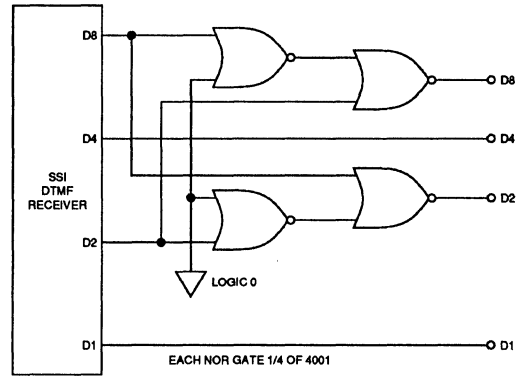


Figure 13: Hex "0" Out with Digit "0" Detect Conversion Circuit

16-CHANNEL REMOTE CONTROL

DTMF signaling provides a simple, reliable means of transmitting information over a 2-wire twisted pair. The complete schematic of a 16-channel remote control is shown in Figure 14. When one of the key pad buttons is depressed, a tone pair is sent over the transmission medium to the SSI DTMF Receiver.

The 4514 raises one of its 16 outputs in response to the 4-bit output code from the DTMF. The output at the 4514 will remain high until the next button is depressed.

Hexadecimal & Fig. 12 Circuit					Hexadecimal				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	1
2	0	0	1	0	2	0	0	1	0
3	0	0	1	1	3	0	0	1	1
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	0	1	1	1
8	1	0	0	0	8	1	0	0	0
9	1	0	0	1	9	1	0	0	1
0	1	0	1	0	0	0	0	0	0
*	1	0	1	1	*	0	0	0	1
#	1	1	0	0	#	1	1	0	0
A	1	1	0	1	A	1	1	0	1
B	1	1	1	0	B	0	1	0	0
C	1	1	1	1	C	0	1	0	1
D	0	0	0	0	D	0	0	0	0

Table 4: Output Code of Figure 13

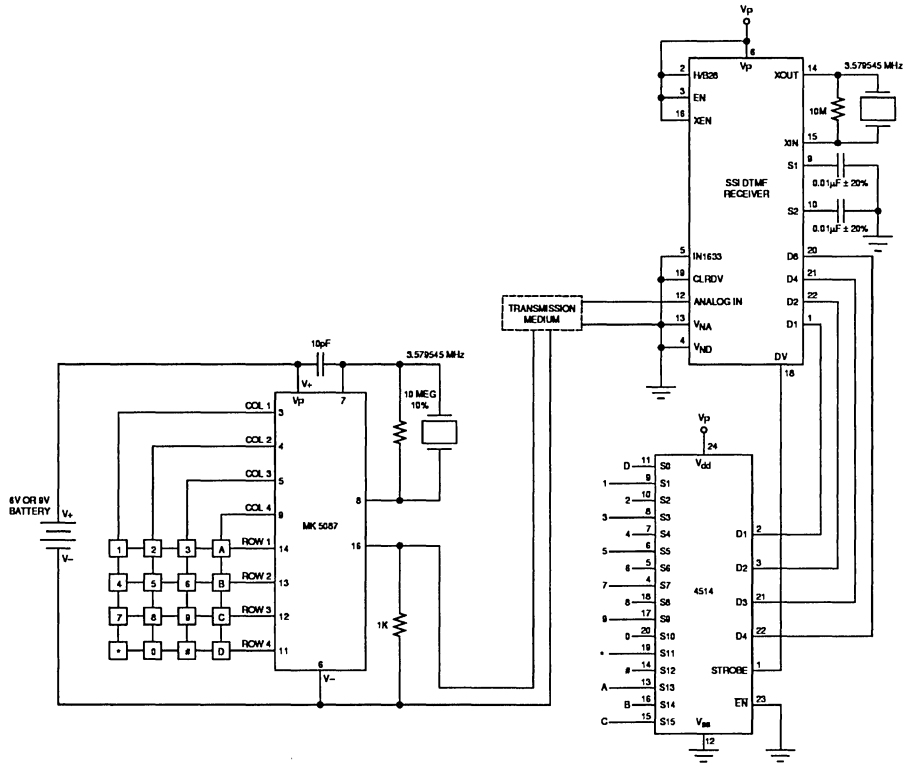


Figure 14: 16-Channel Remote Control

2-0F-8 OUTPUT DECODE

The circuit shown in Figure 15 can be used to convert the binary coded 2-of-8 to the actual 2-of-8 code (or 2-of-7 if detection of 1633 Hz tone is inhibited). The output data will be valid while DV is high. If it is desired to force the eight outputs to zero when a valid tone is not present, DV should be inverted and connected to both E–NOT inputs of the 4555.

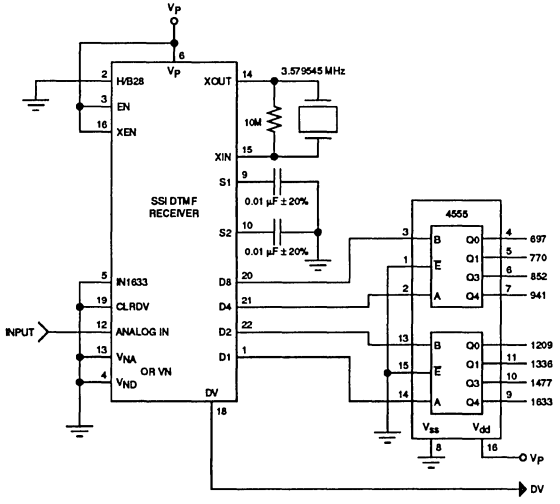


Figure 15: Touch-Tone™ to 2-of-8 Output Converter

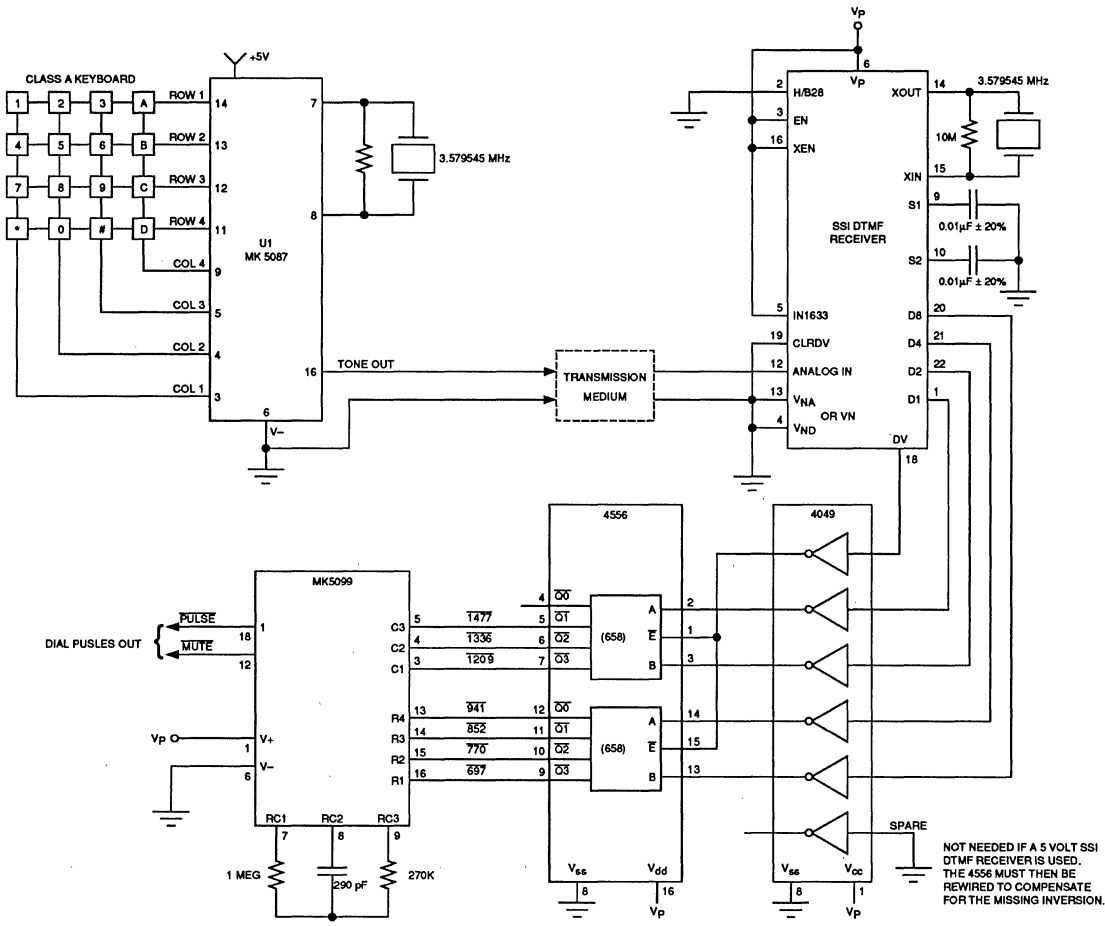


Figure 16: Touch-Tone™ to Rotary Dial Pulse Converter Adding Rotary Dial Pulse Detection Capabilities

DTMF TO ROTARY DIAL PULSE CONVERTER

The 2-of-8 output of Figure 15 can be modified to interface with a pulse dialer as shown in Figure 16. If a 12V DTMF is used the 4049 will translate the 12V outputs to the 5V swings required for the MK5099 pulse dialer.

Figure 17 shows the interface for adding pulse detection and counting to a SSI DTMF Receiver.

The loop detector provides a digital output representing the telephone loop circuit "make" and "break" condition associated with rotary pulse dialing. For the circuit of Figure 17, ground represents a "make" and VP a "break." The loop detector feeds dial pulses to IC-1, a binary counter, and to IC-2A, a re-triggerable "one-shot." When a dial pulse appears the Q1-NOT output of IC-2A immediately goes low, resetting IC-1. The clock input to IC-1 is delayed by R1-C1 so that reset and count input do not overlap. The binary outputs of IC-1 will reflect the pulse count and 0.2 seconds after the last pulse the Q1-NOT output will go high. C3-R3 differentiate this pulse and clock the output latch, IC-3, holding the output pulse until the next digit.

The 0.2 second timeout of IC-2A indicates the end of dial pulsing since even a slow (8 pps) dial would input another pulse every 0.125 seconds. The binary outputs of IC-1 are paralleled with those of the SSI DTMF Receiver

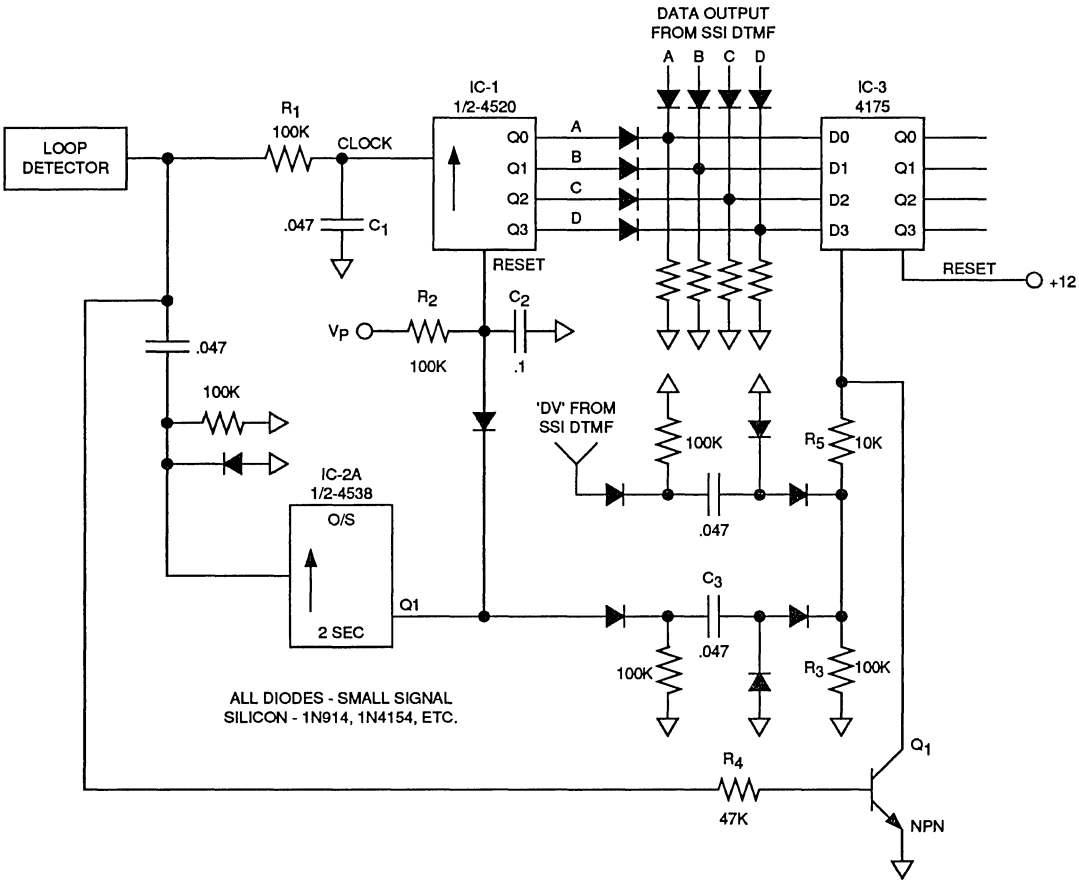


Figure 17: Adding Pulse Detection and Counting to the SSI DTMF Receiver

circuit through diodes to the inputs of IC-3. A pulldown resistor is necessary on each IC-3 input pin. IC-1 must be a binary, not BCD, counter.

With a 4175 for IC-3 the output data is latched until the next valid input, whether from a rotary dial or dual tone instrument. A unique situation exists, however, when going on-hook. The loop detector will output a continuous level of VP which would trigger IC-2A and put a single count into IC-1. A high level from the loop detector also turns on Q1, pulling the clock input of IC-3 to ground. Since the loop detector output will be low at the completion of dialing, all outputs are valid even when the telephone is placed on-hook, an important consideration if output data is recorded.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 75T980
Call Progress Tone Detector

July, 1990

DESCRIPTION

The SSI 75T980 Call Progress Tone Detector circuit allows automatic equipment to monitor tones in dial telephone systems that relate to the routing of calls. Such tones commonly include dial tones, circuits-busy tones, station-busy tones, audible ringing tones and others. By sensing signals in the range of 305 to 640 Hz, the SSI 75T980 does not require the use of precision tones to function. This means that tones which vary with location or call destination can be detected regardless of their exact frequency. The SSI 75T980 is sensitive to signals from 0 dBm to -40 dBm.

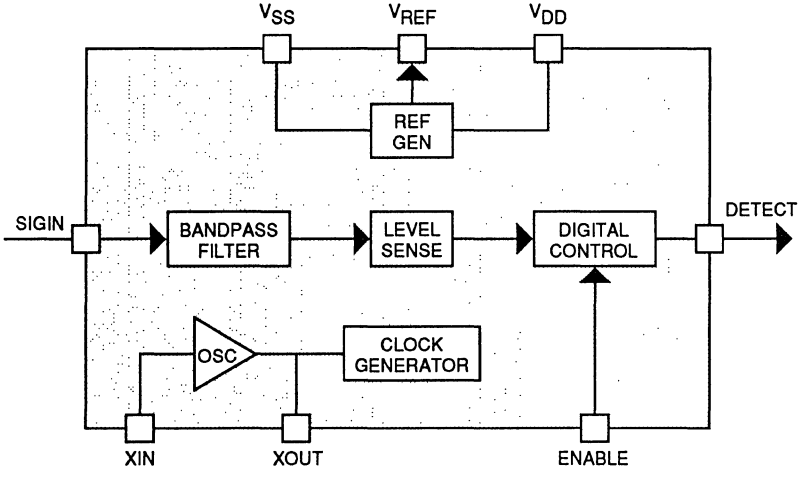
The low power CMOS switched capacitor filters used in the SSI 75T980 derive their accuracy from a 3.58 MHz clock, which in turn may be derived from other devices in the system being designed. The SSI 75T980 is available in a plastic 8-pin DIP and 16-pin SO packages.

FEATURES

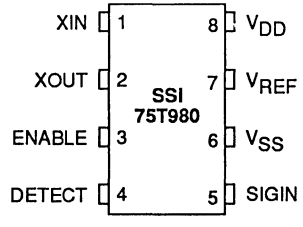
- **Detects tones throughout the telephone progress supervision band (305 to 640 Hz)**
- **Sensitivity to -40 dBm**
- **Dynamic range over 40 dB**
- **40 ms minimum detect (50 ms to output)**
- **Single supply CMOS (low power)**
- **Supply range 4.5 to 5.5 VDC**
- **Uses 3.58 MHz crystal or external clock**
- **8-pin DIP and 16-pin SO packages**
- **Second source of Teltone M-980**

4

BLOCK DIAGRAM



PIN DIAGRAMS



8-pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
SIGIN	I	Accepts analog input signal. See "Electrical Characteristics" for voltage levels, and "Timing Characteristics" for timing.
DETECT	O	Call progress detect output. Goes to logic "1" when signal in 305-460 Hz band is sensed. See "Timing Characteristics."
ENABLE	I	Application of logic "1" on this pin enables the output; logic "0" disables output.
V_{REF}	O	Supplies voltage at half V_{DD} for voltage reference of on-chip op amps.
XIN, XOUT	I	Crystal connections to on-chip oscillator circuit.
V_{DD}	-	Positive power supply connection
V_{SS}	-	Negative power supply connection

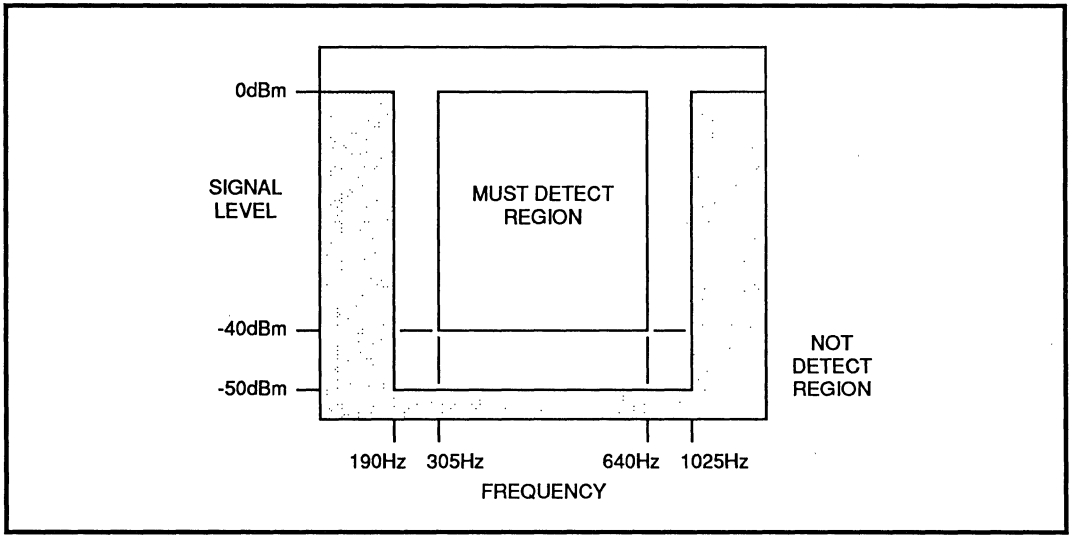


FIGURE 1: Detect and Reject Regions

ABSOLUTE MAXIMUM RATINGS
(Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage	V_{DD}–Vss	16.0V
Input Voltage	All inputs except SIGNAL IN	(V_{DD} + 0.5V) to (Vss – 0.5V)
SIGNAL IN Voltage		(V_{DD} + 0.5V) to (Vss – 22V)
Storage Temperature		–65°C to 150°C
Operating Temperature		0°C to 70°C
Lead Temperature	Soldering, 5 sec.	260°C

4

ELECTRICAL CHARACTERISTICS
(Ta = 25°C, V_{DD} – Vss = 4.5V to 5.5V, dBm is referenced to 600Ω)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current	V_{DD} – Vss = 5V	-	4	10	mA
Signal level for detection	305-640 Hz	–40	-	0	dBm
Signal level for rejection	305-640 Hz	-	-	–50	dBm
	f >1025 Hz, *f* <190 Hz	-	-	0	dBm
DETECT output (Iout = +1mA)	Logic 0	-	-	0.5	V
	Logic 1	4.5	-	-	V
ENABLE, XIN input (Iin=10μA)	Logic 0	Vss	-	Vss+0.2	V
	Logic 1	V_{DD}–0.2	-	V_{DD}	V
XIN duty cycle		40	-	60	%
XIN, XOUT loading		-	-	10	pF
VREF output	Deviation	–2	(V_{DD}+Vss)/2	+2	%
	Resistance	3.25	-	6.75	kΩ
SIGIN input	Maximum voltage	V_{DD}–10	-	V_{DD}	V
	Impedance (500 Hz)	80	-	-	kΩ

TIMING CHARACTERISTICS
(Ta = 25°C, V_{DD} – V_{SS} = 4.5V to 5.5V)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
t_{MD}	Signal duration for detection	305-640 Hz	40	-	ms
t_{ND}	Signal duration for rejection	305-640 Hz	-	20	ms
	Interval duration for detection	Signal dropping from –40 dBm to –50 dBm (t_2)	40	-	ms
		Signal dropping from 0 dBm to –50 dBm (t_1)	90	-	ms
t_D	Detect time		-	50	ms
t_B	Tone dropout bridging		-	20	ms

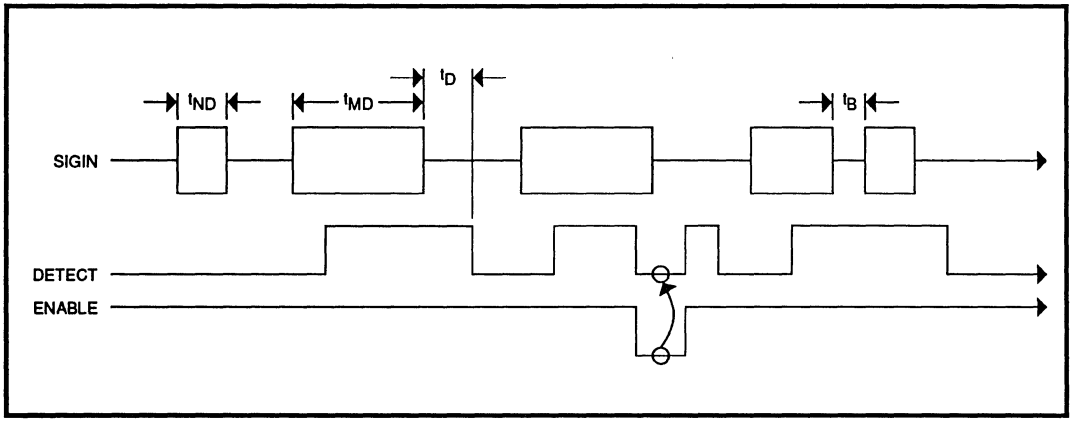


FIGURE 2: Basic Timing

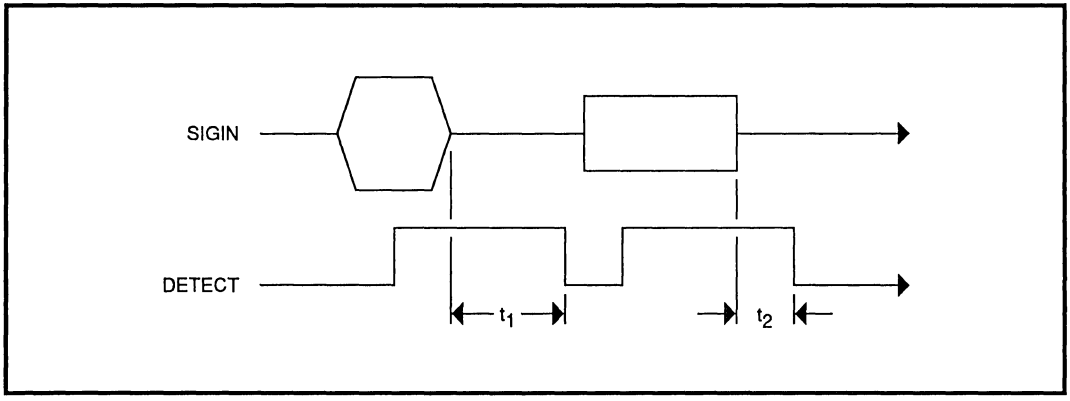


FIGURE 3: Effect of Amplitude on Timing

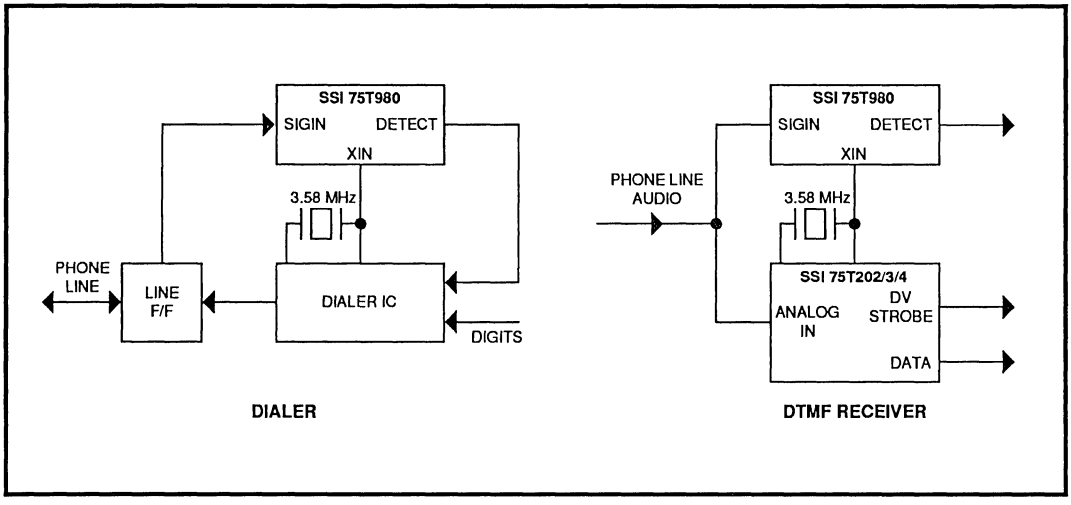
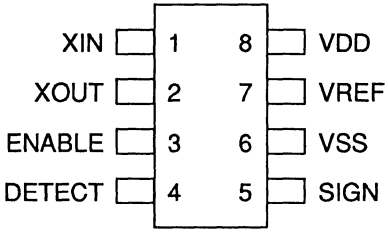


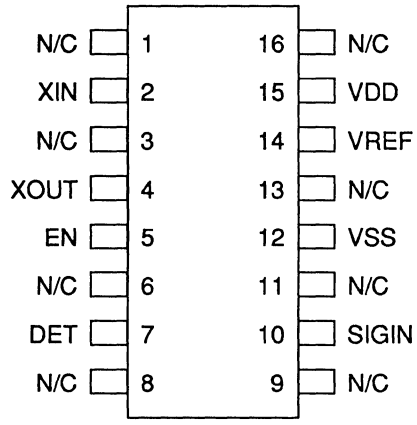
FIGURE 4: Applications Circuits

SSI 75T980
Call Progress
Tone Detector

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



SSI 75T980-CP
8-PIN DIP



SSI 75T980C
16-PIN SO

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T980 8-pin Plastic DIP	SSI 75T980-CP	75T980-CP
SSI 75T980 16-pin SO Package	SSI 75T980-CL	75T980C

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 75T981/982
Precise Call Progress Tone Detector

July, 1990

DESCRIPTION

The SSI 75T981 and SSI 75T982 Precise Call Progress Tone Detector circuits enable automatic monitoring of tones in dial telephone systems for the purpose of routing calls. Built using CMOS switched capacitor technology, each has four independent channels for detecting precise tones in the 305 to 640 Hz range. The outputs of the channels have a response related to the respective tone durations.

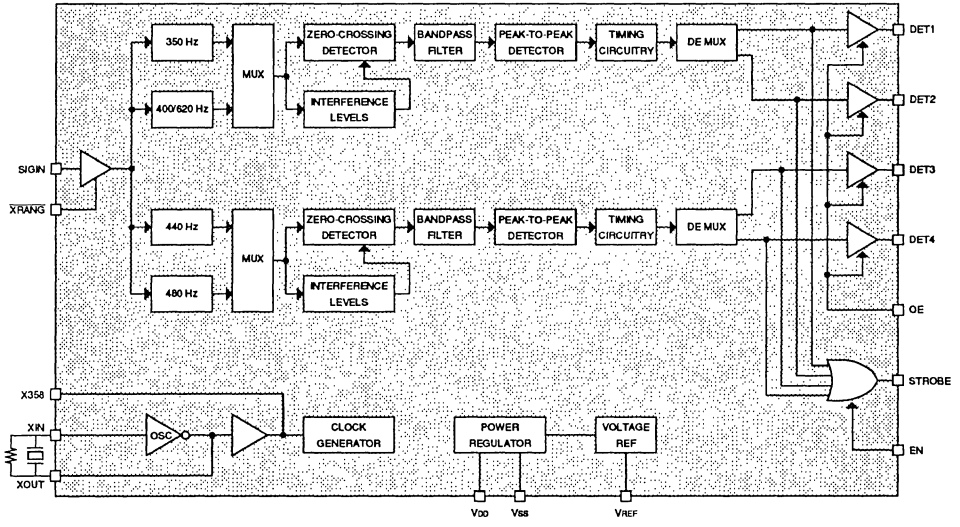
The SSI 75T981 and SSI 75T982 are identical except for the tones detected. The SSI 75T981 will decode 350Hz, 400Hz, 440Hz and 480Hz. The SSI 75T982 will decode 350Hz, 440Hz, 480Hz and 620Hz tones.

FEATURES

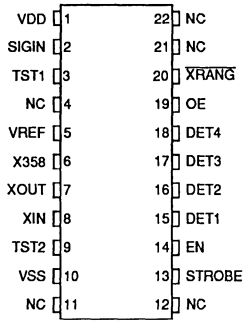
- **Detects & decodes precise tones throughout 305-640 Hz telephone progress band**
- **35 dB dynamic range**
- **Single supply CMOS (low power)**
- **Adjustable gain sensitivity**
- **Supply range 4.75 to 5.5 VDC**
- **Uses 3.58 MHz crystal**
- **Three-state outputs**
- **Standard 22-pin DIP**
- **Second source to Teltone M981 and M982**

4

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The functional block diagram is shown on page 1. Channels 1 and 2, and 3 and 4 are multiplexed, respectively as shown. Each channel starts with a 4-pole band-pass filter that reduces the amplitude of the out-of-band signals. The output of the front-end filter is fed into two circuits, one being a zero-crossing detector which functions as a limiter-AGC, and the other being a circuit that controls the level of the interference floor based on the level of the incoming signal. The output of the ZCD, and energy-limited signal, is fed into a peak-to-peak detector that determines if the precise frequency is present by checking the amplitude of the signal from the back-end filter. Pulses from the peak-to-peak detector, which indicate the presence of the precise tone, are counted to time the duration of the input pulsed-tone. If the criteria of the specifications are met, the appropiate detect output goes to the high state. As shown in the block diagram, all circuitry after the front-end filters is multiplexed. A digital demultiplexer follows the P-P detector to provide the four distinct outputs.

SIGIN

The input signal is applied to the SIGIN pin and is AC-coupled into the front-end filters. The SSI 75T981 and SSI 75T982 can amplify a low level signal by 10 dB when the $\overline{\text{XRANG}}$ pin is held low.

DET OUTPUTS & OE

Outputs DET1-4 are CMOS push-pull when enabled (OE="1") and high impedance when disabled (OE="0"). A "1" on a DET pin indicates that the appropriate valid tone pulse was detected (see Table 1). Detect timing is shown in Figure 1.

STROBE & EN

The STROBE pin is the logical OR of the DETn outputs and will indicate when any one of the four call progress tones has been detected. STROBE is unaffected by OE but goes to a high impedance state when EN="0".

XIN, XOUT & X358

Internal timing and clocks are derived form the 3.58 MHz clock. The SSI 75T981 and SSI 75T982 contain an on-board inverter with sufficient gain to provide oscillation when connected to a low cost "colorburst" crystal. The crystal is connected between XIN and XOUT. A 1MΩ 10% resistor is also connected between these pins. In this mode, X358 is a clock frequency output available to drive other parts requiring the same frequency.

The part will also operate with an external digital clock (duty cycle 40% to 60%).

VREF

Internal analog signal reference voltage. Noise or interference coupled onto this pin may degrade chip functionality.

TST1 & TST2

Manufacturer's special test pins. These pins should be left floating, not grounded.

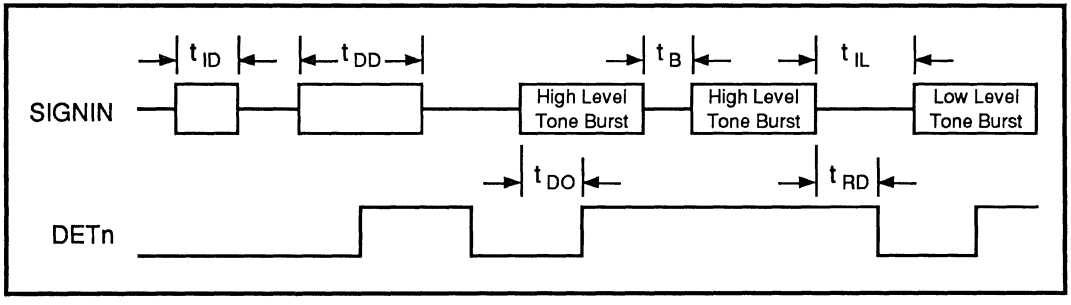


FIGURE 1: Timing Diagram

TIMING CHARACTERISTICS
(Ta = 25°C, V_{DD}-V_{SS} = 4.75V to 5.5V)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
t_{DD}	Signal Duration for Detection	In band, see Electrical Char.	200	-	ms
t_{DO}	Time to Output	In band, see Electrical Char.	-	200	ms
t_B	Bridge Time	In band, see Electrical Char.	-	30	ms
t_{ID}	Signal Duration for Rejection	Noise at SIGIN: –50 dBm, 0.2-3.4 kHz	-	160	ms
t_{RD}	Time to Release	Noise at SIGIN: –50 dBm, 0.2-3.4 kHz	-	200	ms
t_{IL}	Interval Duration for Detection of Both Signals	High to Low; High = 0 dBm, Low = –25 dBm	1	-	sec
t_{EN}	DETn Pin Enable Time, Z to Low or High	C_L = 50 pF, R_L = 100 kΩ	-	450	ns
t_{DS}	DETn pin Disable Time, Low or High to Z	C_L = 50 pF, R_L = 100 kΩ	-	450	ns

4

TABLE 1: Frequency Detection

SIGNAL PRESENT (fo)		DET1	DET2	DET3	DET4	OE	STROBE	EN
75T981	75T982							
350 Hz	350 Hz	1	X	X	X	1	1	1
400 Hz	620 Hz	X	1	X	X	1	1	1
440 Hz	440 Hz	X	X	1	X	1	1	1
480 Hz	480 Hz	X	X	X	1	1	1	1
Other In-Band		0	0	0	0	1	0	1
Any		High Impedance				0	0	0

Note: Out-of-band tones may cause short detect pulses if at sufficient amplitude and pulsed duration.

ELECTRICAL CHARACTERISTICS
(0°C ≤ Ta ≤ 70°C)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
VDD		4.75	5.5	V
Oscillator Frequency Deviation	At XOUT from 3.57959 MHz	–0.01	+0.01	%
Power Supply Noise	0.1 - 5 kHz	-	20	mVpp
Current Drain	VDD=5.5V, Ta = 0°C	-	30	mA
Must Detect Signal				
Frequency Range		–1.0	+1.0	% of *fo*
Level (see Note 2)	$\overline{\text{XRANG}}$=0; In-Band, see Table 1	–35	–10	dBm
	$\overline{\text{XRANG}}$=1; In-Band, see Table 1	–25	0	dBm
Must Reject Signal Level	$\overline{\text{XRANG}}$=0; Noise at SIGIN: -50dBm, 0.2 - 3.4 kHz	-	–60	dBm
	$\overline{\text{XRANG}}$=1; Noise at SIGIN: -50dBm, 0.2 - 3.4 kHz	-	–50	dBm
Level Skew Between Adjacent In-Band Signals for Detection of both	see Note 4	-	6	dB
Steady State Response Must Reject Level	$f < fo - 5\%$ or $f > fo + 5\%$ see Timing Characteristics & Note 3	-	0	dBm
SIGIN Pin				
Voltage Range		VDD - 10	VDD	V
Input Impedance	Resistance; f = 500 Hz	80	-	kΩ
	Capacitance	-	15	pF
Gain	$\overline{\text{XRANG}}$=0	9.9	10.1	dB
$\overline{\text{XRANG}}$ Pin				
VIL		-	0.5	V
VIH		VDD - 2.0	-	V
Pullup Current	$\overline{\text{XRANG}}$=VSS	-	–10	µA
Detect Pins, DETn				
VOL	ISINK = –1mA	-	0.5	V
VOH	ISOURCE = 1mA	VDD - 0.5	-	V
IOZ	VO = VDD, VSS	-	1	µA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
STROBE Pin				
VOL	ISINK = –1 mA	-	0.5	V
VOH	ISOURCE = 1 mA	VDD - 0.5	-	V
OE, EN Pins				
VIL		-	0.5	V
VIH		VDD - 2.0	-	V
Pullup Current	OE, EN = VSS	-	–10	µA
External Clock				
VIL	XOUT Open	-	0.2	V
VIH	XOUT Open	VDD - 0.2	-	V
Duty Cycle	XOUT Open	40	60	%
XIN, XOUT Loading				
Capacitance	Crystal oscillator active	-	10	pF
Resistance	Crystal oscillator active	20	-	MΩ
X358 Pin (CL = 20 pF)				
VOL	ISINK = –10 µA	-	0.2	V
VOH	ISOURCE = 10 µA	VDD - 0.2	-	V
Duty Cycle		40	60	%

Notes:

1. All parameters are specified at VDD = 5 volts and $\overline{\text{XRANG}}$ at a logical "high" state, which implies unity front-end gain. Power levels in dBm are referenced to 600Ω.

2. A post-filter AGC is employed to enhance end-of-tone detection for high-level signals. A drop in amplitude of the input tone may cause an end-of-tone (interval) indication.

3. Large input voltage transients may cause excessive ringing in the highly selective filter, causing spurious detection. The detects are not considered as incorrect circuit operation.

4. Any tone 40 Hz – 1% from fo must adhere to this specification, where fo is defined in Table 1.

ABSOLUTE MAXIMUM RATINGS
(Operation above absolute maximum ratings may damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage	$V_{DD} - V_{SS}$	+7V
Input Voltage	All inputs except SIGIN	V_{SS} – 0.3V to V_{DD} + 0.3V
SIGIN Voltage		V_{DD} – 18V to V_{DD} + 0.3V
Storage Temperature		–65°C to 150°C
Operating Temperature		0°C to 70°C
Lead Temperature	Soldering, 10 sec.	260°C

NORMAL CALL PROGRESS TONES AND SEQUENCE (Refer to Figure 2.)

TONE	FREQUENCY (Hz)	CADENCE
Precision Dial Tone	350 + 440	Continuous
Old Dial Tones	600 + 120 or 133 and other combinations	Continuous
Precision Busy	480 +620	0.5 s on 0.5 s off
Old Busy	600 +120	0.5 s on 0.5 s off
Precision Reorder	480 +620	0.3 s on local 0.2 s off reorder
Old Reorder	600 +120	0.2 s on toll 0.3 s off reorder 0.25 s on toll 0.25 s off local
Precision Audible Ringback	440 +480	2 s on 4 s off
Old Audible Ringback	420 +40 and other combinations	2 s on 4 s off

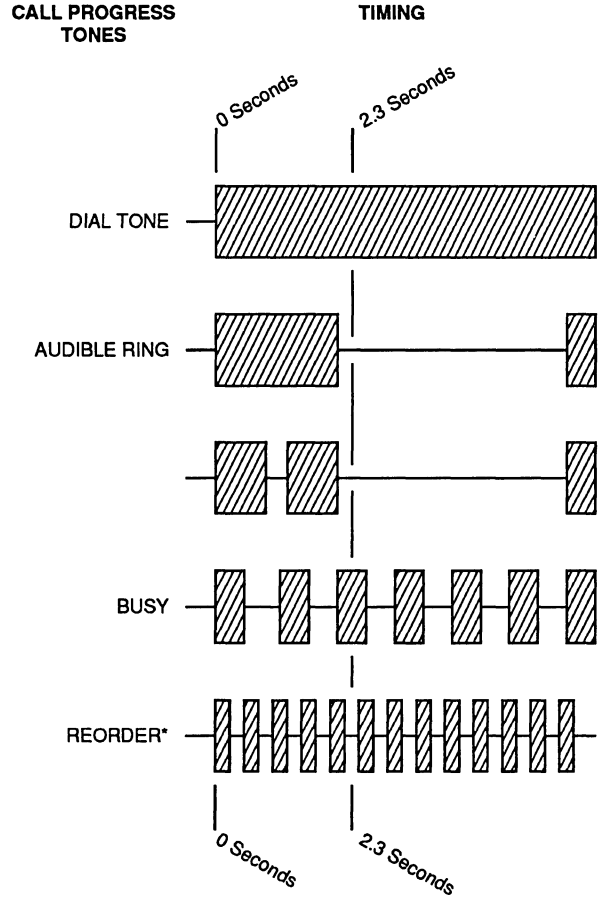
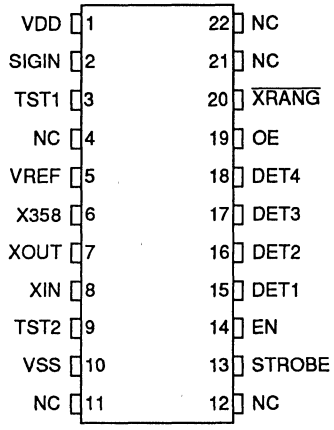


FIGURE 2: Normal Call Progress Tones and Sequence

SSI 75T981/982
Precise Call Progress Tone Detector

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



22 - PIN DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T981 22-Pin Plastic DIP	SSI 75T981-CP	75T981-CP
SSI 75T982 22-Pin Plastic DIP	SSI 75T982-CP	75T982-CP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 731-5457

Section

TELEPHONY/ DIGITAL TELECOM

5

SSI 78A093A/B
CMOS 12x8x1 Crosspoint Switch With Control Memory

July, 1990

DESCRIPTION

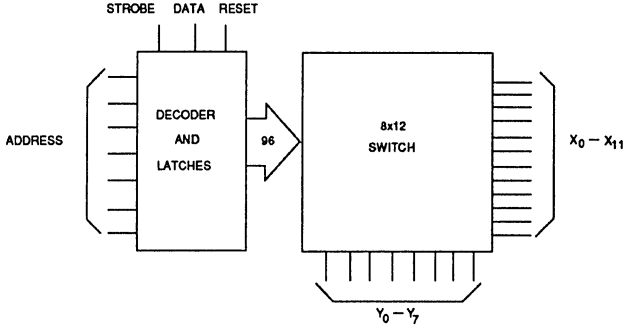
The SSI 78A093 is a 12x8 matrix-array crosspoint-switching IC for telecom-switching and industrial control-routing applications. Standard integrated features include microprocessor-control inputs, line decoder, address latches, and 6 Vp-p analog-signal capability. The product is available with two different power supply configurations: The SSI 78A093A accepts power through the VSS and VDD pins; the SSI 78A093B has an altered pin-out and offers a separate logic ground pin. Both versions offer excellent crosstalk immunity, low feedthrough (–95dB at 1KHz), extra-high isolation between any two switches connected to X0 channel, and less than 1% total distortion at 0 dBm. The X0 channel is optimized for "ON HOLD" use by providing high isolation between switches connected to X0. The SSI 78A093 employs CMOS design technology for low-power operation. Power requirement for both the A and B versions of the SSI 78A093 is 5 to 16 volts. Both versions are packaged in a standard 40-pin plastic DIP or 44-pin PLCC.

FEATURES

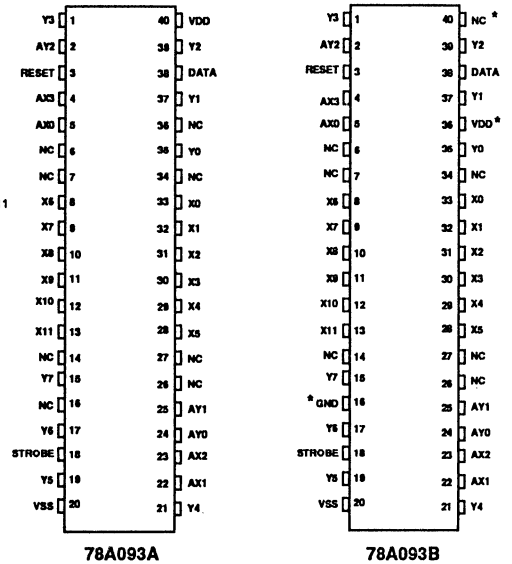
- 96 crosspoint switches in a 12x8 array
- µP-compatible control inputs
- On-chip line demultiplexer
- Low ON resistance: 28 ohms at VDD = 12V typical
- 5 to 16-volt supply operating range
- 6 Vp-p analog signal capability
- Address latches on-chip
- Optimized performance on X0 channel
- Less than 1% total distortion at 0 dBm
- -95 dB feedthrough at 1kHz
- Extra-low crosstalk between any two switches connected to X0
- 78A093B version offers separate logic ground for flexible system design
- Low-power CMOS design
- TTL or CMOS-compatible inputs
- 40-pin plastic DIP or 44-pin PLCC

5

BLOCK DIAGRAM



PIN DIAGRAM



* different pins relative to 78A093A

NOTE: Please see last page for PLCC pinout.

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 78A093A/B
CMOS 12x8x1
Crosspoint Switch
With Control Memory

FUNCTIONAL DESCRIPTION

A functional block diagram of the device is presented in Figure 1. The IC contains a 12x8 matrix of analog switches, each with a latch to maintain its on (closed) or off (open) state. Seven ADDRESS lines, AX0-AX3 and AY0-AY2, are provided to address any one of the 96 switches. The DATA line may be held high to turn the switch on, or low to turn it off. The state of the ADDRESS and DATA lines can be set concurrently or separately. Finally, a positive pulse to the STROBE line initiates the action determined by the ADDRESS and DATA lines. All 96 switches may be turned off by forcing the RESET line high. All control lines (ADDRESS, DATA, STROBE, and RESET) are level sensitive.

The IC has two power supply configurations: the A-version has VDD and VSS power supply pins; the B-version has VDD, VSS and a GND pin. The GND pin is provided as a reference voltage for digital inputs. For proper operation, the positive supply must be at least 4.5 volts above GND.

The switches are designed to provide low resistance connections when turned on. Any Y switches connecting to the X0 channel are optimized to provide lower ON resistance. Furthermore, the X0 channel switches, when turned on, provide maximized isolation between the Y channels when X0 is grounded or connected to a low impedance source.

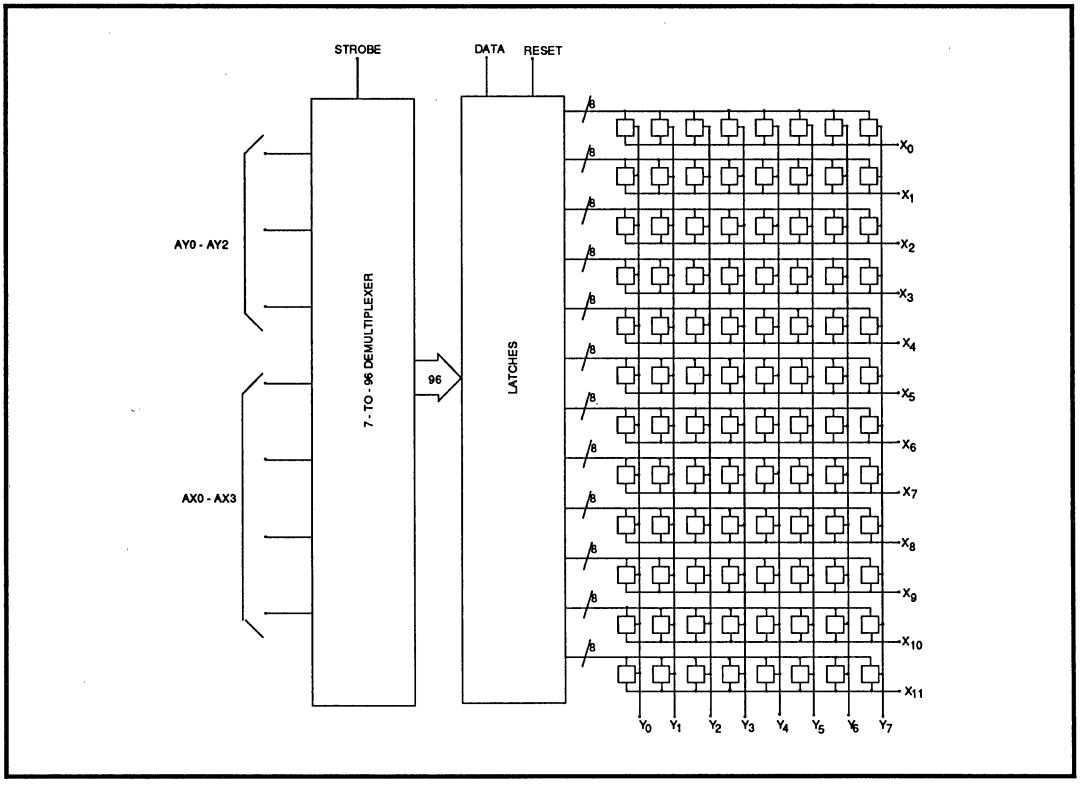


FIGURE: 1

PIN DESCRIPTION

NAME	A-PIN # (DIP)	B-PIN # (DIP)	TYPE	DESCRIPTION
POWER				
VDD	40	36	I	Positive power supply.
VSS	20	20	I	Negative power supply.
GND	-	16	I	Digital signal ground.
ADDRESS				
AX0-AX3	4, 5, 22, 23		I	X address lines. These 4 pins are used to select one of the 12 rows of switches. Refer to the truth table in figure 2, for legal addresses.
AY0-AY2	2, 24, 25		I	Y address lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table in figure 2, for legal addresses.
CONTROL				
DATA	38		I	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
STROBE	18		I	This pin enables whatever action is selected by the address and DATA pins. When the STROBE pin is held low, no switch openings or closing take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin).
RESET	3		I	Master Reset. This pin turns off (opens) all 96 switches. The states of the above control lines are irrelevant. This pin is active high.
DATA				
X0-X11	8-13, 28-33		I/O	Analog Input/Outputs. These pins are connected to the rows of the switch matrix.
Y0-Y7	1, 15, 17, 19, 21, 35, 37, 39		I/O	Analog Input/Outputs. These pins are connected to the columns of the switch matrix.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING	UNIT
VDD with respect to VSS	-0.5 to 17.6	V
GND (B-Version only)	VSS -0.5 to VDD +0.5	V
Storage Temperature	-65 to 150	°C
Control Signals	GND -0.5 to VDD +0.5	V
Analog Signals	7	Vpp
Lead Temperature (soldering, 10 seconds)	300	°C

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
address not allowed 0	1	1	0	0	0	0	no connection
address not allowed 1	1	1	0	0	0	0	no connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0	1	1	1	0	0	0	no connection
1	1	1	1	0	0	0	no connection
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0 - Y1 ↓ X11- Y1
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0 - Y2 ↓ X11- Y2
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0 - Y3 ↓ X11- Y3
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0 - Y4 ↓ X11- Y4
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0 - Y5 ↓ X11- Y5
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0 - Y6 ↓ X11- Y6
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0 - Y7 ↓ X11- Y7

FIGURE 2: Truth Table

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside these limits.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD with respect to VSS		4.5		16.0	V
VDD with respect to GND		4.5		16.0	V
GND with respect to VSS		0		5.5	V
Analog Input Voltages VIN				6	Vpp
Analog Currents				10	mA
Ambient Temperature		0		85	°C

D.C. CHARACTERISTICS

TA = 25°C, VSS = 0V, GND = 0, VDD = 13.2V, RL = 1K, CL = 50pF, UNLESS OTHERWISE NOTED.
Positive current is defined as flowing into the device.

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current IDD				14	20	mA
CROSSPOINT						
ON resistance	X0 channel (X0-Yj)	VIN ≤ 6V		20		Ω
RON	other channels (Xi-Yj)	VIN ≤ 6V		28	45	Ω
ON resistance var.	X0 channel (X0-Yj)			5		Ω
Δ RON	other channels (Xi-Yj)			15	25	Ω
X capacitance	CX	(Switch off)			20	pF
Y capacitance	CY	(Switch off)			30	pF
CONTROL						
Input HIGH voltage	VIH	A-Version B-Version	2.0 GND +2.0			V V
Input LOW voltage	VIL	A-Version B-Version			0.8 GND +0.8	V V
Input leakage	IL		-0.1		0.1	µA

DYNAMIC CHARACTERISTICS AND TIMING

TA = 25°C, VDD = 13.2V, VSS = 0V, GND = 0V, RL = 1K, CL = 50 pF, UNLESS OTHERWISE NOTED. Digital input rise and fall times are 5nS. Output times are defined as the time to rise or fall from 0% to 10% of the full swing (see figure 3).

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
CROSSPOINT						
Propagation Delay		1 Vpp sine wave @ 10 kHz		18	30	ns
Distortion		1 Vpp sine wave		0.2	1.0	%
Feedthrough		10 kHz, any switch off		-90	-80	dB
Yi to Yj isolation on X0 channel		Any two Y channels: Yi, Yj, X0-Yi, X0-Yj are on Xo grounded, Rin = 1K		-90	-60	dB
Crosstalk		1Vp-p sine wave 1 kHz		-97		dB
		1Vp-p sine wave 10 kHz		-92		dB
CONTROL						
Delay: strobe to out	TSZ			60	160	ns
Delay: address to out	TAZ				200	ns
Delay: data to out	TDZ				180	ns
Delay: reset to out	TRZ			100	180	ns
Data setup time	TSU			30		ns
Address setup time	TAS			30		ns
Data hold time	TH			30		ns
Address hold time	TAH			30		ns
Strobe Pulse Width	TST			50		ns
Reset Pulse Width	TRST			50		ns

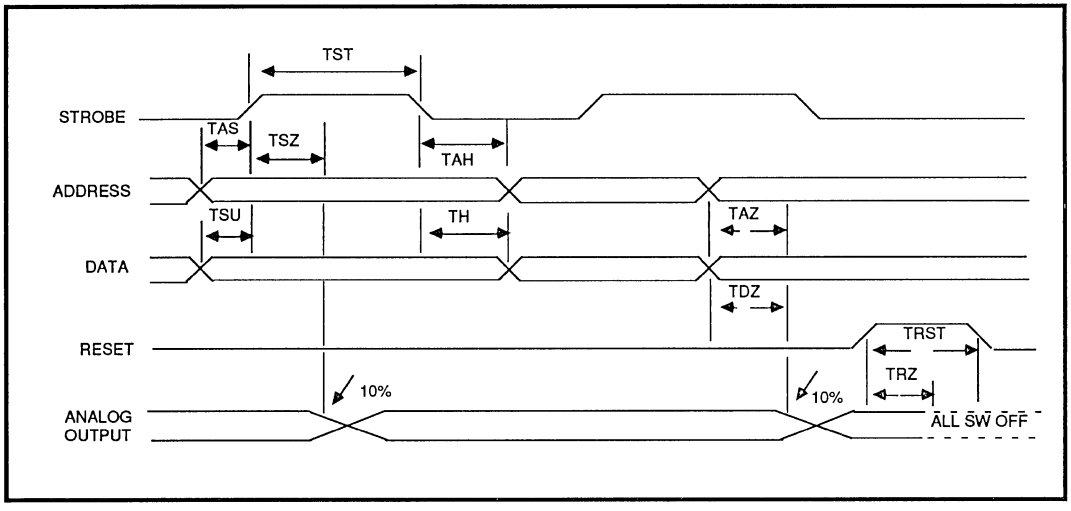


FIGURE 3: Timing Diagram

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APPLICATIONS INFORMATION

Although the SSI 78A093 allows switching 96 possible signal paths, it is not limited to applications of only an 8x12x1 configuration. Figure 4 shows a method of addressing 4 separate 78A093's. In this example, the RESET, DATA, and ADDRESS lines are connected in parallel for the four devices. The logic for lines A, B and STROBE go to a 2-line to 4-line decoder with the STROBE used to both enable and clock the data. This decode (or a wider one) could be easily implemented with a single programmable logic device.

Figure 5 shows a case where both the X and Y lines have been expanded. This may be useful for applications where several different source/destination paths need to be controlled by a single controller. The A and B lines are decoded to select the desired device.

In Figure 6, the Y-lines of all devices are connected in parallel to allow an 8x48x1 switch configuration. The A and B inputs become in effect an extension of the X-address line. This could also be used to make a 32x12x1 matrix by tying the X-lines in parallel with the A and B inputs used as Y-address lines.

Figure 7 shows an application where switches in 2 devices are connected at the same time in a 12x8x2 matrix. This would be useful in applications requiring the switching of differential signals.

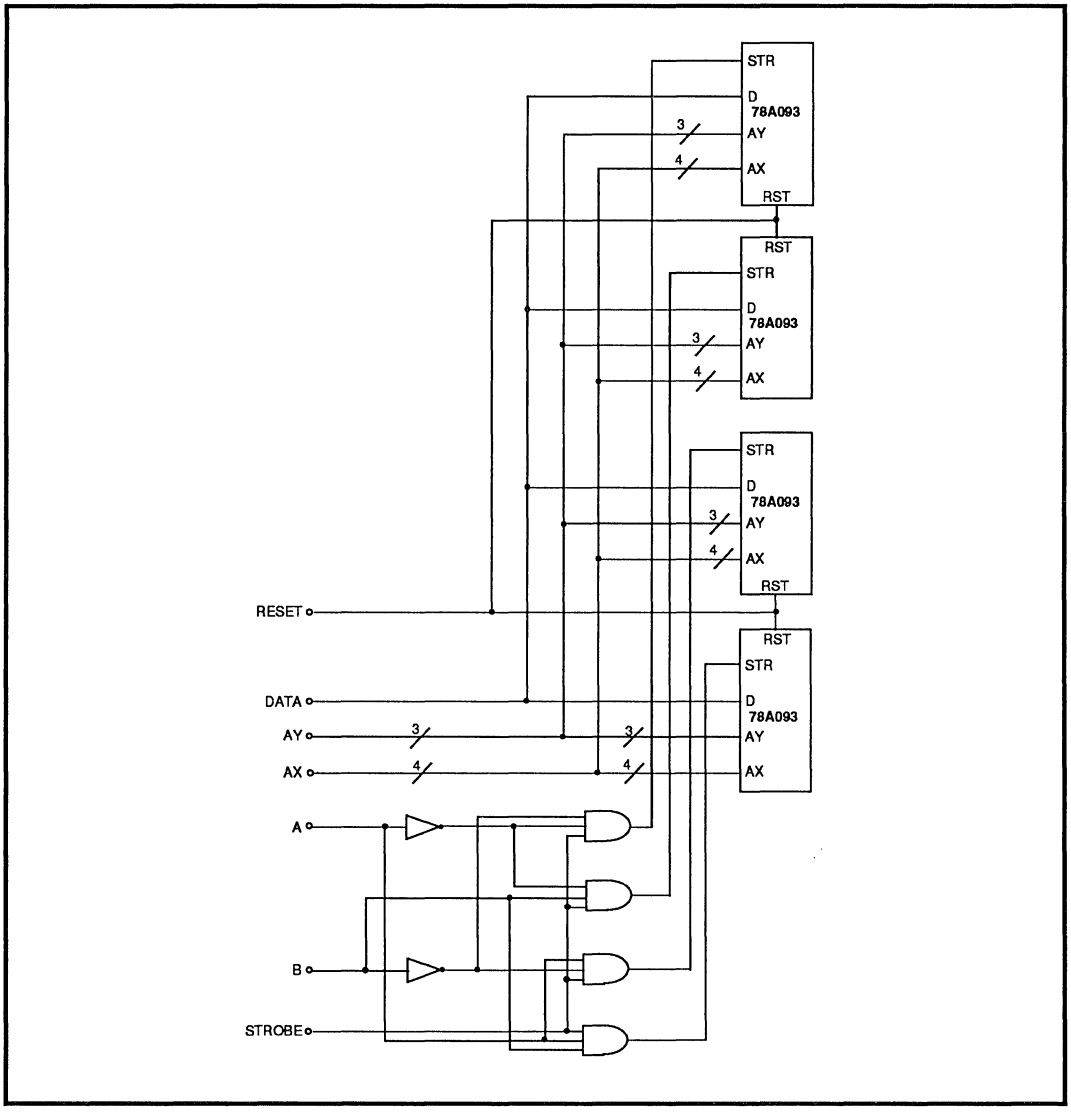


FIGURE 4

FIGURE 5

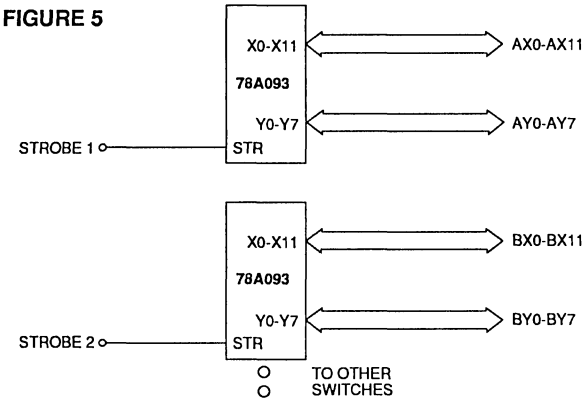


FIGURE 6

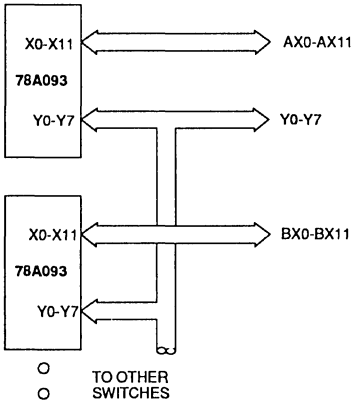
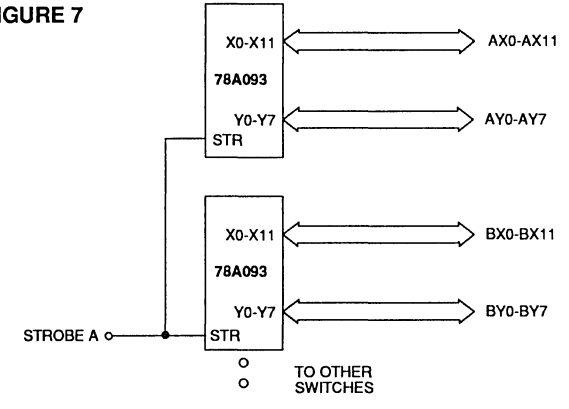


FIGURE 7



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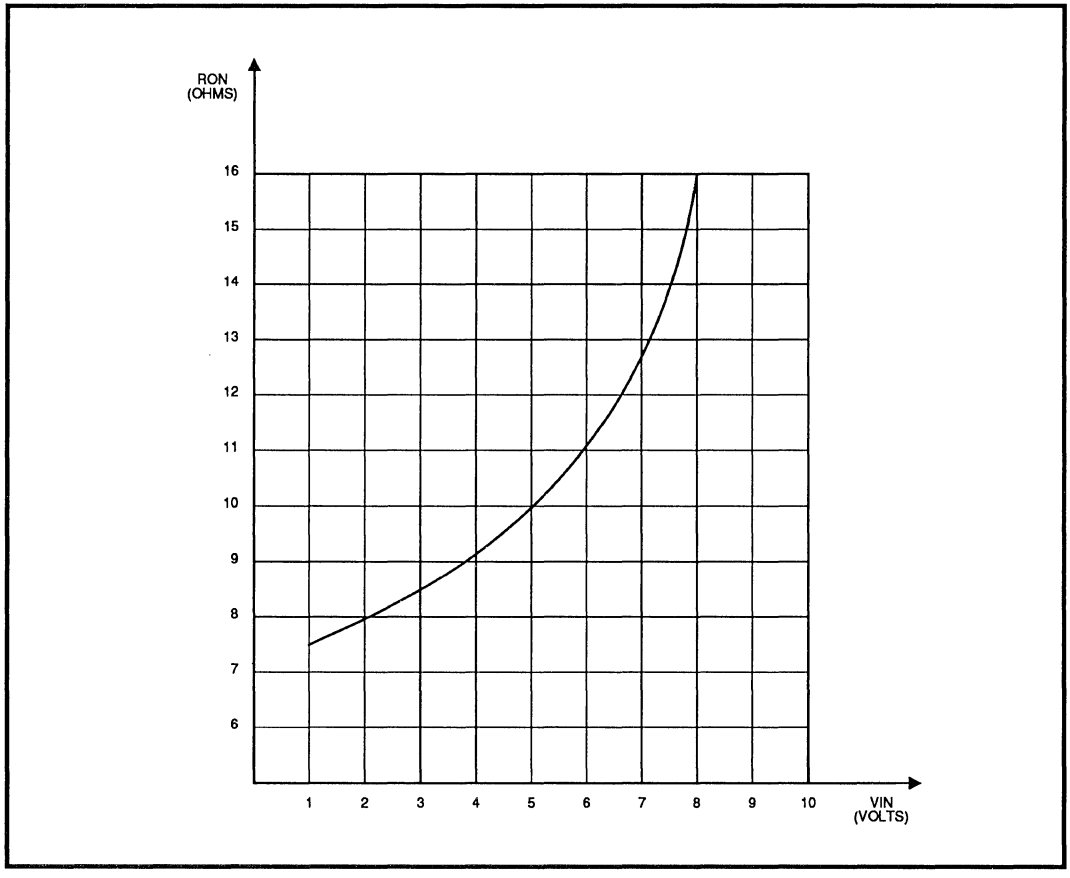


FIGURE 8: X0 - Channel: RON vs. VIN

Figure 8 is valid for all switches connected to the X0 channel only. The graph describes the behavior of the switch resistance RON as a function of the analog signal voltage VIN.

TEST CONDITIONS: VSS = 0V
VDD = 13.2V
RL = 1kΩ (Load Resistance)

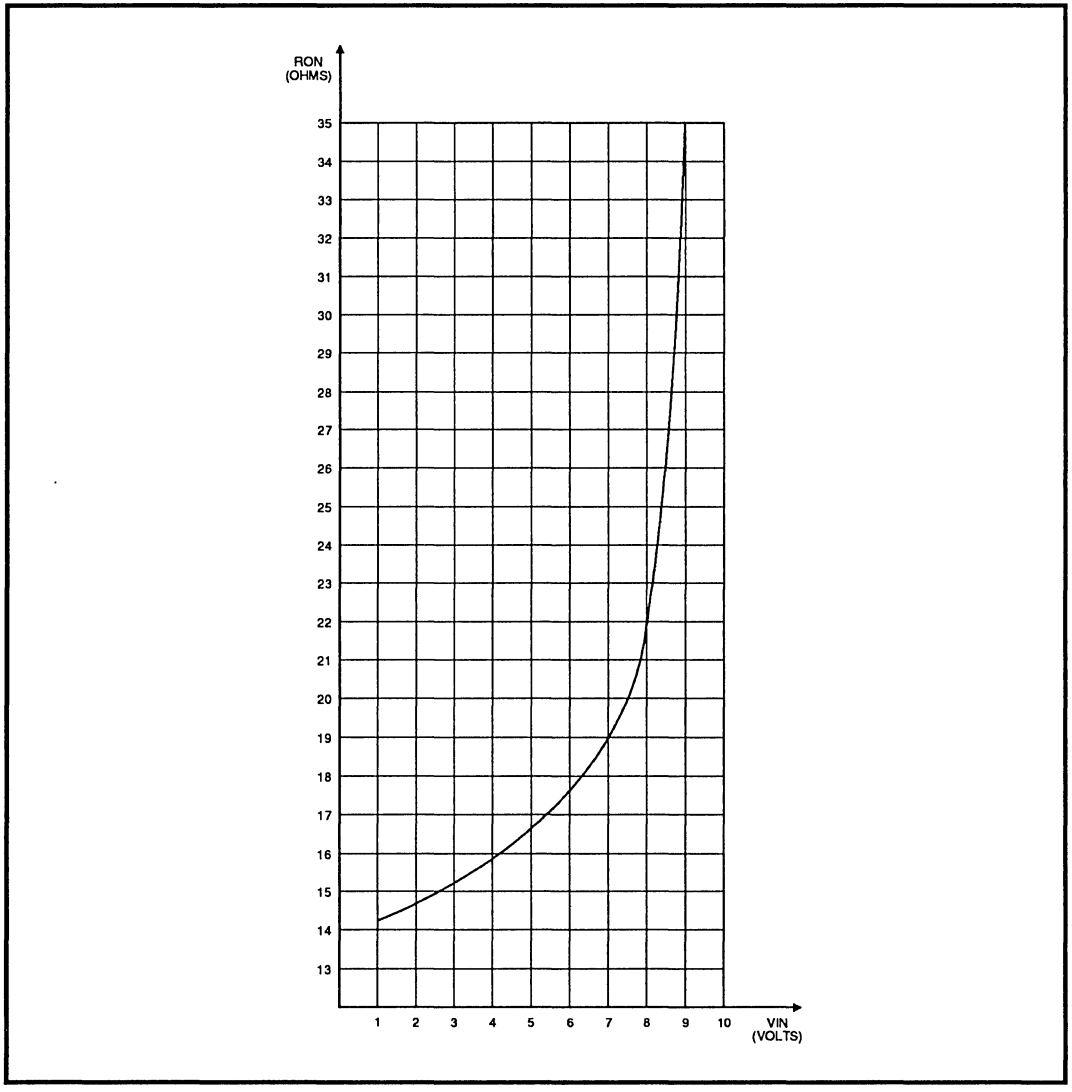


FIGURE 9: X1 - X11 Channel: RON vs. VIN

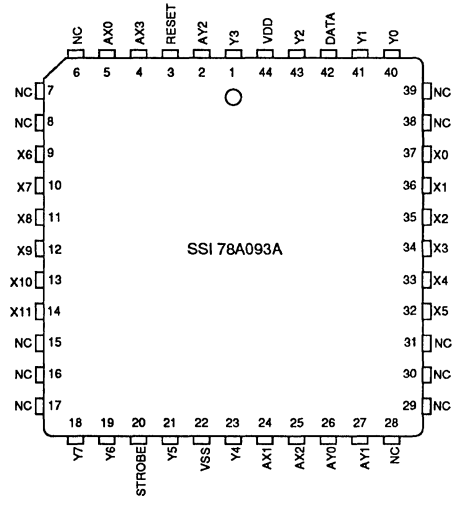
Figure 9 is valid for all switches connected to X1 thru X11 channels. The graph describes the behavior of the switch resistance RON as a function of the analog signal voltage VIN.

TEST CONDITIONS: VSS = 0V
VDD = 13.2V
RL = 1kΩ (Load Resistance)

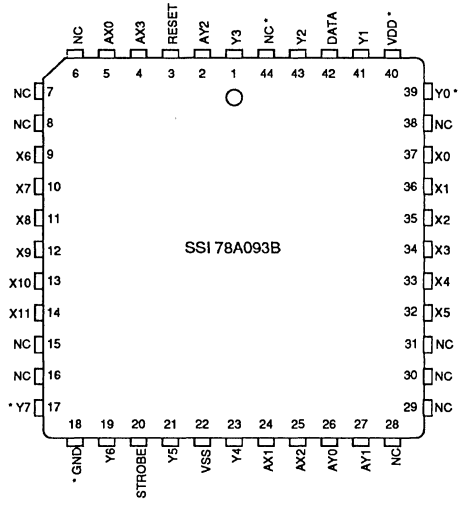
SSI 78A093A/B
CMOS 12x8x1
Crosspoint Switch
With Control Memory

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

Refer to the SSI Data Book for package dimensions.
Please see Page 1 for PDIP pinout.



44 - Pin PLCC
78A093A



44 - Pin PLCC
78A093B

* different pins relative to 78A093A

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78A093, Version A		
Plastic Dual-In-Line	SSI 78A093A-CP	78A093A-CP
PLCC	SSI 78A093A-CH	78A093A-CH
SSI 78A093, Version B		
Plastic Dual-In-Line	SSI 78A093B-CP	78A093B-CP
PLCC	SSI 78A093B-CH	78A093B-CH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 731-5457

SSI 78A207
MFR1 Receiver

July, 1990

DESCRIPTION

The SSI 78A207 is a single-chip, Multi-Frequency (MF) receiver that can detect all 15 tone-pairs, including ST and KP framing tones. This receiver is intended for use in equal access applications and thus meets both Bell and CCITT R1 central office register signalling specifications.

The SSI 78A207 employs state-of-the-art switched capacitor filters in CMOS technology. The receiver consists of a bank of channel-separation bandpass filters followed by zero-crossing detectors and frequency-measurement bandpass filters, an amplitude check circuit, a timer and decoder circuit, and a clock generator. The device does not attempt to identify strings of digits by the KP (key pulse) and ST (stop) tone pairs.

No anti-alias filtering is needed if the input signal is band-limited to 26 KHz. The only external component required is an inexpensive television "color burst" 3.58 MHz crystal.

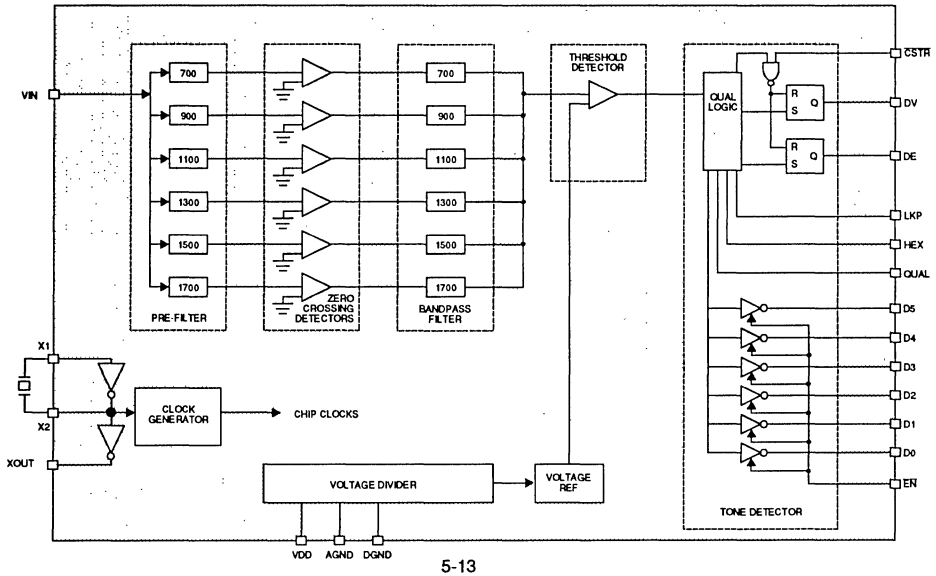
The outputs interface directly with standard CMOS or TTL circuitry and are three-state enabled to facilitate bus-oriented architecture.

FEATURES

- **Meets Bell and CCITT R1 specifications**
- **20-pin plastic DIP**
- **Single low-tolerance 5V supply**
- **Detects all 15 tone-pairs including ST and KP**
- **Long KP capability**
- **Built-in amplitude discrimination**
- **Excellent noise tolerance**
- **Outputs in either "n of 6" or hexadecimal code**
- **Three-state outputs, CMOS-compatible and TTL-compatible**

5

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

VIN

This pin accepts the analog input. It is internally biased to half the supply and is capacitively coupled to the channel separation filters. The input may be DC coupled as long as it does not exceed VDD or drop below GND. Equivalent input circuit is shown below in Figure 1.

CRYSTAL OSCILLATOR

The SSI 78A207 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" crystal. The on-chip clock signals are generated from the oscillator. The crystal is connected between X1 and X2.

XOUT is a 3.58 MHz square wave capable of driving other circuits as long as the capacitive load does not exceed 50 pF. Other devices driven by XOUT should use X1 as the input pin, while X2 should be left floating.

LKP

The KP timer control: When high, the KP detect time is increased. When low, the KP detect time is the same as for other tones.

QUAL

Enables tone pair qualification. When low, the threshold detector outputs are passed to the data outputs (D0-D5) without validation in the format selected by the HEX pin. These outputs, plus strobes DV and DE, are updated once per 2.3 ms frame. Note that the strobes will cycle once per frame (even when the inputs are stable.) As always, data changes only when both strobes are low.

$\overline{\text{CSTR}}$

This input clears both the DV and DE strobes, and is active low. After $\overline{\text{CSTR}}$ is released, the strobes will remain low until a new detect (or error) occurs. The output data is latched by $\overline{\text{CSTR}}$ and will not change while $\overline{\text{CSTR}}$ is low, even in the event that a new detect is qualified internally. (Note that improper use of $\overline{\text{CSTR}}$ may result in missed detects.)

$\overline{\text{EN}}$

The three-state enable control: When low, the D0-D5 outputs are in the low impedance state. In an interrupt oriented microprocessor interface, $\overline{\text{EN}}$ and $\overline{\text{CSTR}}$ will often be tied together to provide automatic reset of the strobes when the output data is enabled.

STROBE PINS - DV AND DE

Valid data is indicated on the DV strobe pin, and data errors are indicated on the DE strobe pin. Whenever a valid 2 of 6 code has been detected, the DV strobe rises. It remains high until the code goes away, or the $\overline{\text{CSTR}}$ line is activated. When an invalid code is detected, e.g., 1 of 6, 3 of 6, etc., the DE strobe remains high until all errors stop, a valid tone pair is detected, or the $\overline{\text{CSTR}}$ line is activated. Once cleared by $\overline{\text{CSTR}}$, DE will not reactivate until a new invalid condition is detected. The DE and DV strobes will never be high simultaneously.

DATA OUTPUT MODES

The digital output format may be either "n of 6" or 4-bit hexadecimal.

For "hex" mode, the HEX pin is pulled high. Outputs D0 to D3 provide a 4-bit code identifying one of the 15 valid tone combinations according to Table1.

The outputs will be cleared to zero when no valid tone pair is present.

For the "n of 6" mode, the HEX pin is pulled low, and each output represents one of the six frequencies as shown below:

FREQUENCY	OUTPUT PIN
700	D0
900	D1
1100	D2
1300	D3
1500	D4
1700	D5

The outputs will be cleared to zero when no valid tone is present.

TABLE 1:

Channels	Tone Pair Freq.	Name	D3	D2	D1	D0
0-1	700, 900	1	0	0	0	1
0-2	700, 1100	2	0	0	1	0
1-2	900, 1100	3	0	0	1	1
0-3	700, 1300	4	0	1	0	0
1-3	900, 1300	5	0	1	0	1
2-3	1100, 1300	6	0	1	1	0
0-4	700, 1500	7	0	1	1	1
1-4	900, 1500	8	1	0	0	0
2-4	1100, 1500	9	1	0	0	1
3-4	1300, 1500	0	1	0	1	0
2-5	1100, 1700	KP	1	0	1	1
4-5	1500, 1700	ST	1	1	0	0
1-5	900, 1700	ST1	1	1	0	1
3-5	1300, 1700	ST2	1	1	1	0
0-5	700, 1700	ST3	1	1	1	1
	any other signal		0	0	0	0
NOTE: In the hex mode, D4 = DE and D5 = DV.						

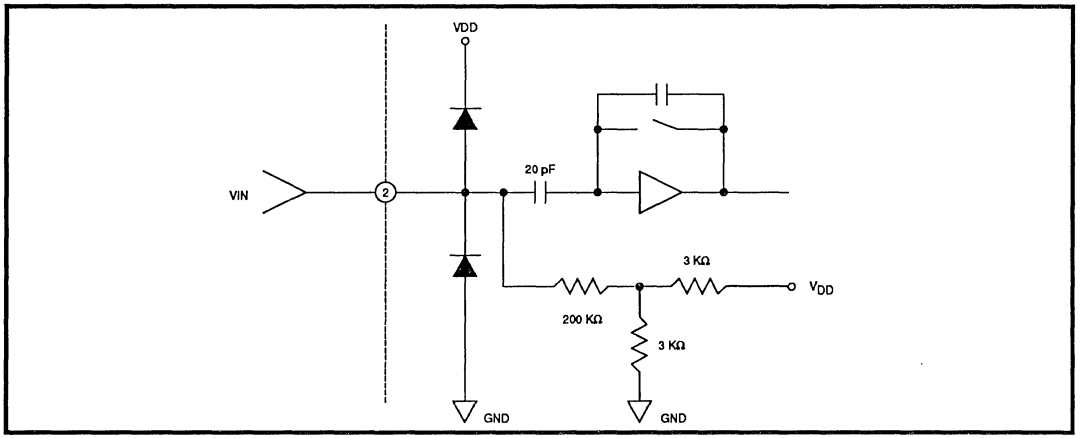


FIGURE 1: VIN Equivalent Input Circuit

TIMING SPECIFICATIONS

	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Ton	Tone Time, KP (LKP = VDD)	detect	55			ms
Ton		reject			30	ms
Ton	Tone Time, KP (LKP = DGND)	detect	30			ms
Ton		reject			10	ms
Ton	Tone Time, All Others	detect	30			ms
Ton		reject			10	ms
Tpse	Pause Time	detect	20			ms
Tbr		reject			10	ms
Tsu	Data Setup Time		6			µs
Th	Data Hold Time		7			µs
Tskew	Tone Skew Tolerance				4	ms
Tstr	Minimum Strobe Pulse Width					
	QUAL High		20			ms
	QUAL Low		2			ms
Tsep	Minimum Strobe Separation					
	QUAL High		20			ms
	QUAL Low		2			ms
Tr	Rise Time DV, DE, D0-D5 10-90%	CL = 20 pF			100	ns
Tf	Fall Time DV, DE, D0-D5 10-90%	CL = 20 pF			100	ns
Tw	$\overline{\text{CSTR}}$ Width		50			ns
Ten	Data Enable Time	CL = 20 pF			100	ns
Tdis	Data Disable Time				100	ns
Trst	Strobe Reset Time	CL = 20 pF			100	ns

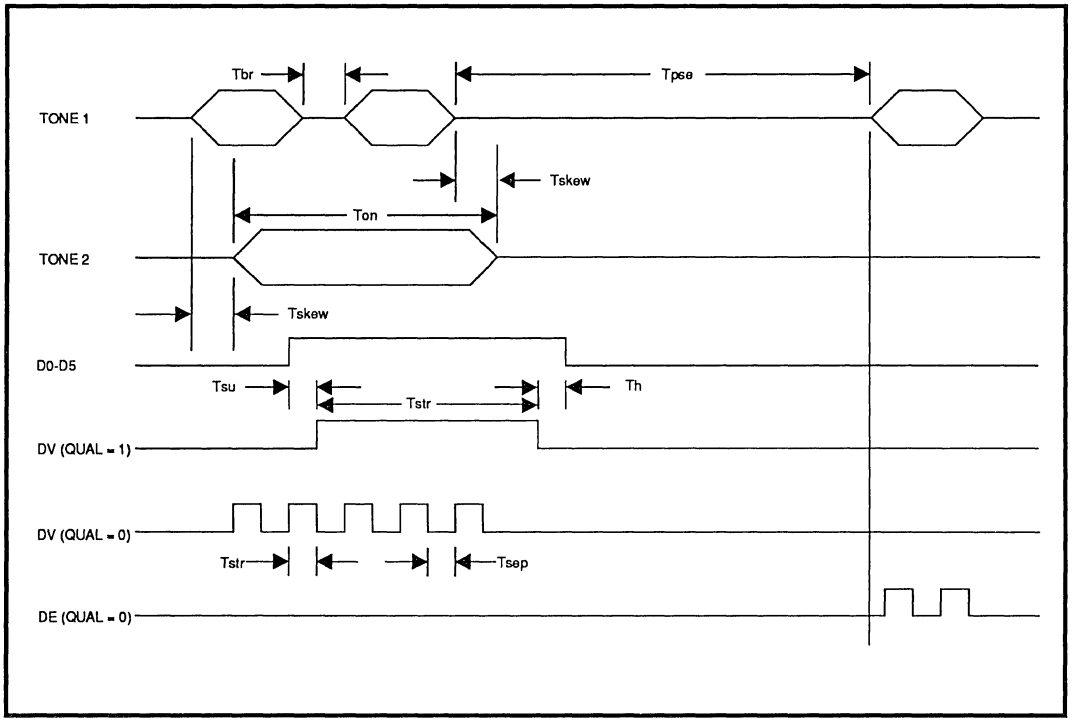


FIGURE 2: SSI 78A207 Timing Diagram

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Operating above absolute maximum ratings may damage the device.)

PARAMETER	RATING	UNIT
DC Supply Voltage V_{DD}	+ 7	V
Operating Temperature	0 to 70 (Ambient)	°C
Storage Temperature	65 to 150	°C
Power Dissipation (25°C) (Derate above TA=25°C @ 6.25 mW/°C)	650	mW
Input Voltage	(V_{DD} + 0.3V) to -0.3	V
DC Current into any input	±10	mA
Lead Temperature (Soldering, 10 sec.)	300	°C

DC ELECTRICAL CHARACTERISTICS (0°C ≤ TA ≥ 70°C, VDD = 5V ± 10%)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Idd	Supply Current				20	mA
Vol	Output Logic 0					
	Iol = 8 mA				0.5	V
	Iol = 1 mA				0.4	V
Voh	Output Logic 1					
	Ioh = -4 mA		VDD-1.0			V
	Ioh = -1 mA		VDD-0.5			V
Vih	Input Logic 1		2.0			V
Voh	Input logic 0				0.8	V
Zin	Analog Input Impedance (Input between VDD and AGND)		$\frac{100K}{30pF}$			Ω
Iin	Digital Input Current (Input between VDD and DGND)		-50		50	µA

AC CHARACTERISTICS (0°C ≤ TA ≥ 70°, VDD = 5V ± 10%)

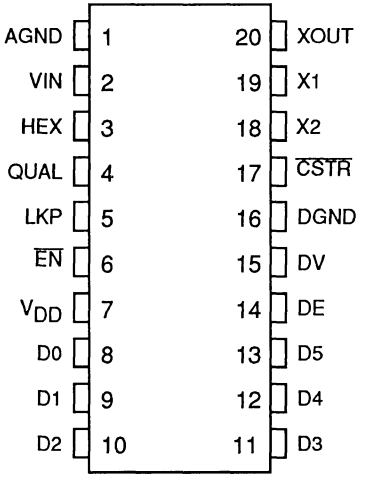
PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
F	Frequency for Detect Tolerance		±(0.015 xFo + 5)			Hz
A	Amplitude for Detect	each tone	-25		0	dBm
			0.123		2.191	Vpp
AN	Amplitude for no Detect				-35	dB
					0.039	Vpp
TW	Twist Tolerance	$TW=\frac{\text{high tone}}{\text{low tone}}$	-6		+6	dB
T3	Third MF Tone Reject Amp	relative to highest amplitude tone	-15			dB
N60	60 HZ Tolerance	not more than one error	81			dBrn
		in 2500 10-digit calls	0.777			Vpp
N180	180 HZ Tolerance	same as above	68			dBrn
			0.174			Vpp
Nn	Noise Tolerance[1]	same as above			-20	dB
NI	Impulse Noise Tolerance[2]	same as above			+12	dB

NOTES: 1. C-message weighted. Measured with respect to highest amplitude tone.

2. With noise tape 201 per PUB 56201. Measured with respect to highest amplitude tone.

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



20 - PIN DIP

5

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78A207 20-Pin Plastic DIP	SSI 78A207-CP	78A207-CP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

Notes:

SSI 78P233
DS-1 Line Interface

July, 1990

DESCRIPTION

The SSI 78P233 DS-1 Line Interface is a bipolar integrated circuit that provides the interface functions necessary to convert DS-1-level signals to TTL-level and conversely. The receiver section accepts alternate-mark-inversion (AMI) encoded line data and provides separated and synchronized data and clock outputs. The transmitter section accepts data and clock and produces AMI pulses of appropriate shape for transmission. A loopback multiplexer is also provided that permits interchange of the signals between the sections.

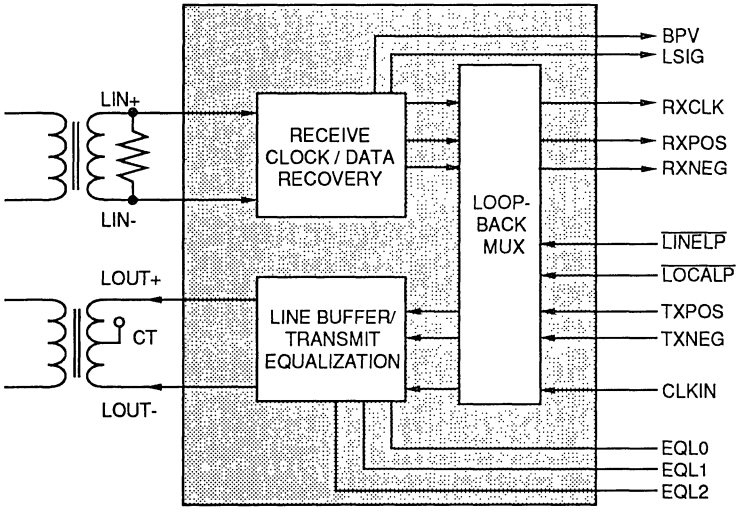
The 78P233 requires a single 5V supply. It is available in three different packages: standard, 600-mil DIP; narrow, 300-mil DIP; small outline (SOIC).

FEATURES

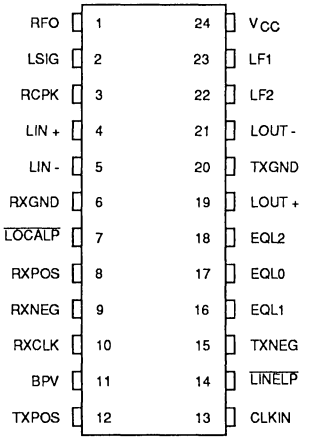
- **Single-chip transmit and receive DS-1 Line Interface**
- **Unique clock recovery circuit, requires no crystals or tuned components**
- **Variable jitter tolerance, adjustable with external components**
- **Pulse-shape transmission conformant with AT&T Compatibility Bulletin 119 specifications**
- **Six different line equalization settings for pulse-shaping at the DSX-1 level**
- **Two alternate transmit settings for 6V-peak pulses**
- **Standard unipolar TTL-level clock & data ports for easy equipment interface**
- **Line-loopback and local-loopback control**
- **Loss-of-signal indication**
- **Bipolar violation detection**

5

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The device consists of receiver and transmitter sections together with a "loopback" means which permits interchange of signals between the sections (See Figure 1).

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. To provide a tracking threshold for amplitude-detecting these pulses, the signal is peak detected and a fixed percentage of the peak value is applied to the comparators which detect individual positive and negative pulses. An external R-C network is required to provide the proper storage of the peak reference value. Should the detected peak value fall below an acceptable level, the Loss of Signal (LSIG) output becomes active. This output may be used as a logical control signal or is able to drive a fault indicator LED directly.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase-locked-oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. Non-precision external components are required, however, to establish the oscillator center frequency and loop bandwidth.

The phase-locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

Additional circuits are provided to detect received bipolar violations. These deviations from the alternate mark inversion format are detected when two or more successive pulses of the same polarity are received. A resultant violation output is in time coincidence with the violating received signal output.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line.

Internal equalizer networks are selected by combinations of the three Equalizer Select inputs so that the waveform at the terminal end of various lengths of cable is as required. Note that the transmitter output pulse widths are determined by the input clock width, so that it must be carefully controlled to provide acceptable outputs.

The transmitter pulse selection logical function is arranged so that the simultaneous occurrence of both positive and negative transmit data inputs inhibits the output driver. Moreover, the driver has a current-limiting feature which protects the circuit in the event of a shorted load or inadvertent shorting of an output to the supply voltage.

LOOPBACK CONTROL SECTION

The loopback control section is essentially a multiplexer which is capable of directing received data and clock to the transmitter section, or directing transmit input data and clock to the receiver outputs. This "looping" is controlled by two active low logic signals, $\overline{\text{LINELP}}$ and $\overline{\text{LOCALP}}$, respectively.

The bipolar violation output is held inactive when the circuits are in the Local Loopback mode.

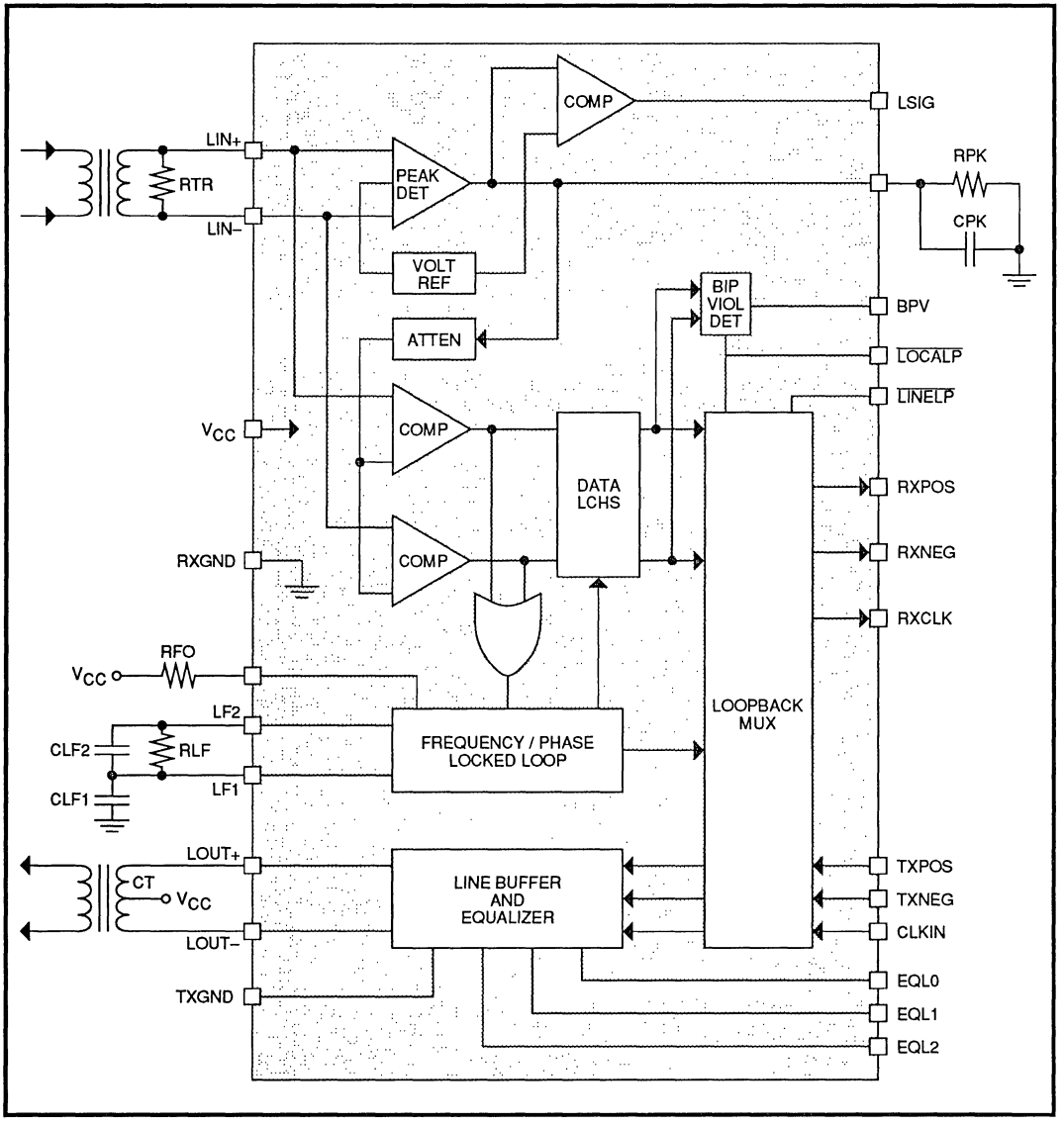


FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

I/O	LABEL	PIN NO.	DESCRIPTION
I	LIN+, LIN-	4, 5	Differential inputs, transformer-coupled from line.
O	RXPOS	8	Unipolar receiver output, active as result of positive pulse at inputs.
O	RXNEG	9	Unipolar receiver output, active as result of negative pulse at inputs.
O	RXCLK	10	Clock pulses recovered from line data.
O	LSIG	2	Loss-of-signal output indicating that input signal is less than threshold value.
O	BPV	11	Bipolar violation output, active as a result of successive pulses at inputs of same polarity.

TRANSMITTER

I	TXPOS	12	Unipolar transmitter data input, active high.
I	TXNEG	15	Unipolar transmitter data input, active high.
I	CLKIN	13	Transmitter clock input. Controls transmit pulse width. Transmit is active when low.
O	LOUT+	19	Output to transformer for positive data pulses.
O	LOUT-	21	Output to transformer for negative data pulses.
I	EQL0 EQL1 EQL2	17 16 18	Line equalizer control signals. Selected according to Table 1 for various cable lengths.

LOOPBACK CONTROL

I	$\overline{\text{LINELP}}$	14	Low level causes receiver recovered data and clock to be connected to the transmitter. Data and clock continue to be present at receiver outputs.
I	$\overline{\text{LOCALP}}$	7	Low level causes transmitter input data and clock to be connected to the receiver outputs. Input data continues to be transmitted.

PIN DESCRIPTION (continued)

EXTERNAL COMPONENT CONNECTION

I/O	LABEL	PIN NO.	DESCRIPTION
I	RFO	1	Resistor connected to Vcc to provide basic center frequency of receiver phase locked loop oscillator.
-	LF1 LF2	23 22	Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
-	RCPK	3	Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

-	Vcc	24	Positive supply terminal for receiver circuits.
-	RXGND	6	Ground terminal for receiver circuits.
-	TXGND	20	Ground terminal for transmitter driver circuits.

5

ABSOLUTE MAXIMUM RATINGS

(T_A = 0°C to 70°C, Vcc = 5V ± 5%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING	UNIT
Vcc, Supply Voltage	-0.5 to +7.0	V
Storage Temperature	-65 to 130	°C
Soldering Temperature (10 sec.)	260	°C
Voltage Applied to Logic Inputs	-0.5 to +7.0	V
Maximum Power Dissipation	800	mW
Junction Operating Temperature	0 to +130	°C
NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ta	Ambient temperature		0		70	°C
Vcc	Power supply voltage		4.75		5.25	V
VIH	High-level input voltage		2.0			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current	LSIG pin only; VO = 1.5V	-7		-13	mA

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor	1% tolerance		6.04		KΩ
RLF	Loop filter resistor			12.0		KΩ
CLF1	Loop filter capacitor			0.022		µF
CLF2	Loop filter capacitor			430.0		pF
RPK	Peak-detector resistor			36.0		KΩ
CPK	Peak-detector capacitor		0.0015	0.015	0.15	µF
	Transmit line transformer	Refer to Table 3		---		---

D. C. ELECTRICAL CHARACTERISTICS
(T_A = 0°C to 70°C, Vcc = 5V ± 5%, unless otherwise specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply current	All outputs open		75	100	mA
IIH	High-level input current	VIH = 2.7V			20	µA
IIL	Low-level input current	VIL = 0.4V			-0.36	mA
VOH	High-level output voltage	IOH = -400 µA	2.7			V
VOL	Low-level output voltage	IOL = 4.0 mA; IOL = 2.0 mA, LSIG pin			0.4	V
RIN	Receiver input resistance		800	1000	1250	Ω

DYNAMIC CHARACTERISTICS AND TIMING, TRANSMITTER
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. Transmit pulse characteristics are obtained using a line transformer which has the characteristics shown in Table 3. Refer to Figure 2.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			648		nsec
TTC	Transmit clock pulse width			324		nsec
TTCNT	Transmit clock negative transition time				10	nsec
TTCPT	Transmit clock positive transition time				10	nsec
TTPDS TTNDS	Transmit data set-up time		15			nsec
TTPDH TTNDH	Transmit data hold time		0			nsec
TTPL	Transmit positive line pulse width	See Note 1	TTC-5		TTC+5	nsec
TTNL	Transmit negative line pulse width	See Note 1	TTPL-5		TTPL+5	nsec
POL	Transmit line pulses power level	See Note 2				
	Transmit line pulses waveshape	See Notes 2 & 3				
Note 1: Measured at transformer with minimum line equalization						
Note 2: Characteristics are in accordance with AT&T Compatibility Bulletin 119, Table 1, and Table 2 or Table 3, for line lengths and equalizer settings as shown in Table 1 of this document.						
Note 3: Characteristics are in accordance with Table 2 for equalizer settings shown therein.						

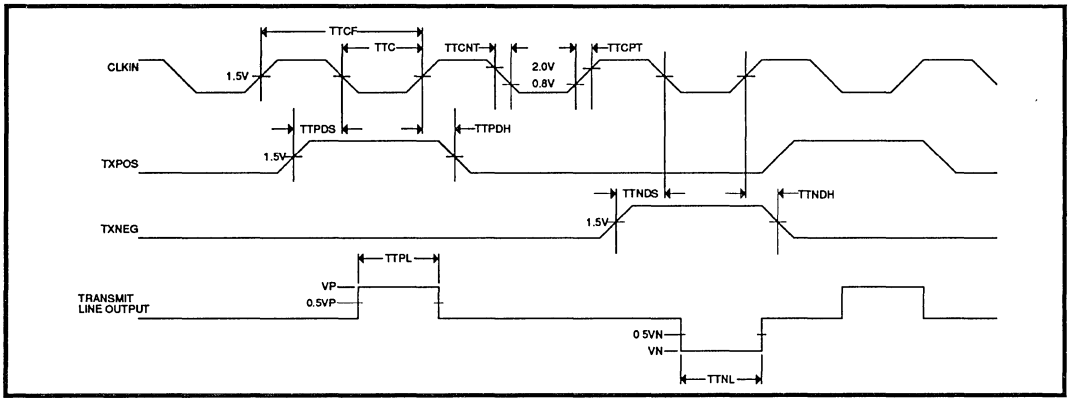


FIGURE 2: Transmit Waveforms

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER
(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. External component values as specified in Recommended Operating Conditions; see Note 1. Refer to Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage		±1.5		±3.7	Vpk
VLOS	Loss-of-signal indicating voltage		±0.5		±1.0	Vpk
TLOS	Loss-of-signal delay time	Timed from removal of input signal; See Note 2	0.7TPK		1.3TPK	sec
VDTH	Receive data detection threshold	Relative to peak amplitude	65		75	%
TSTAB	Receiver stabilization time	After application of input signal			5	msec
TRCF	Receive clock period			648		nsec
TRC	Receive clock pulse width			324		nsec
TRCPT	Receive clock positive transition time	C_L = 15 pF			15	nsec
TRCNT	Receive clock negative transition time	C_L = 15 pF			10	nsec
TRDP TRDN	Positive or negative receive data pulse width			648		nsec
TRDPS TRDNS	Receive data set-up time		290			nsec
TRDPH TRDNH	Receive data hold time		290			nsec
TRBV	Receive bipolar violation pulse width			648		nsec
TRBVS	Receive bipolar violation set-up time		290			nsec
TRBVH	Receive bipolar violation hold time		290			nsec
	Receive input jitter tolerance high frequency	sine, 10 KHz to 100 KHz	±100			nsec
	Receive input jitter tolerance low frequency	sine, 300 Hz or less	±4			µsec

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
KD	Clock Recovery Phase Detector Gain	(All 1's Data Pattern)	66		79	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Control Gain		0.15		0.20	Megrad/ sec. Volt
Note 1: Input signal is transformer coupled, and in accordance with AT&T Compatibility Bulletin 119, Table 1, and Table 2 or Table 3; also, as attenuated by 0 to 655 feet of ABAM* cable.						
Note 2: TPK = RPK x CPK x ln((VIN + 1.2V)/(VLOS + 1.2V))						
* ABAM is the trade name for 22-gauge twisted-pair cable manufactured by AT&T.						

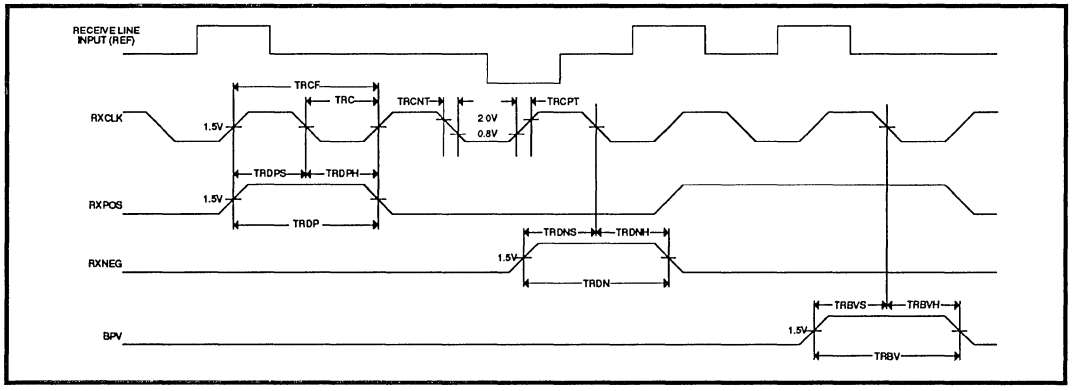


FIGURE 3: Receive Waveforms

TABLE 1: Equalizer Settings for Standard DSX-Level (3V-Peak Nominal) Pulses Versus ABAM Cable Length

CABLE LENGTH IN FEET	EQUALIZER SETTING		
	EQL0	EQL1	EQL2
0 to 50	0	0	0
51 to 131	1	0	0
131 to 262	0	1	0
262 to 393	1	1	0
393 to 524	0	0	1
524 to 655	1	0	1
Note: Equalizer settings may vary slightly at short line lengths.			

TABLE 2: Equalizer Settings for Non-DSX-Level (6V-Peak Nominal) Pulses

PULSE CHARACTERISTICS	EQUALIZER SETTING		
	EQL0	EQL1	EQL2
Rectangular 6.0 ± 0.6V pulse, 10% to 40% trailing edge overshoot	0	1	1
Rectangular 6.0 ± 0.6V pulse, less than 10% trailing edge overshoot	1	1	1
Note: Output waveform at transformer secondary; terminated in 100Ω load.			

TABLE 3: Transmit Line Transformer Characteristics

CHARACTERISTIC	SYMBOL	MIN	NOM	MAX	UNIT
Turns ratio	N		1CT:1		
Primary open circuit inductance	Lp	1.25			mH
Primary leakage inductance	L1			2.0	µH
Primary volt-time product	ET	10			V-µsec
Primary DC resistance	Rp			1.0	Ω
Secondary DC resistance	Rs			1.0	Ω
Effective primary distributed capacitance	C'			15	pF

TABLE 4: Recommended Transmit Line Transformers

MANUFACTURER	PART NO.
AIE Magnetics	318-0765
AT&T	2745 AG
Pan-Mag (Tamura Corporation of America)	PHT-019
Pulse Engineering	PE 64936

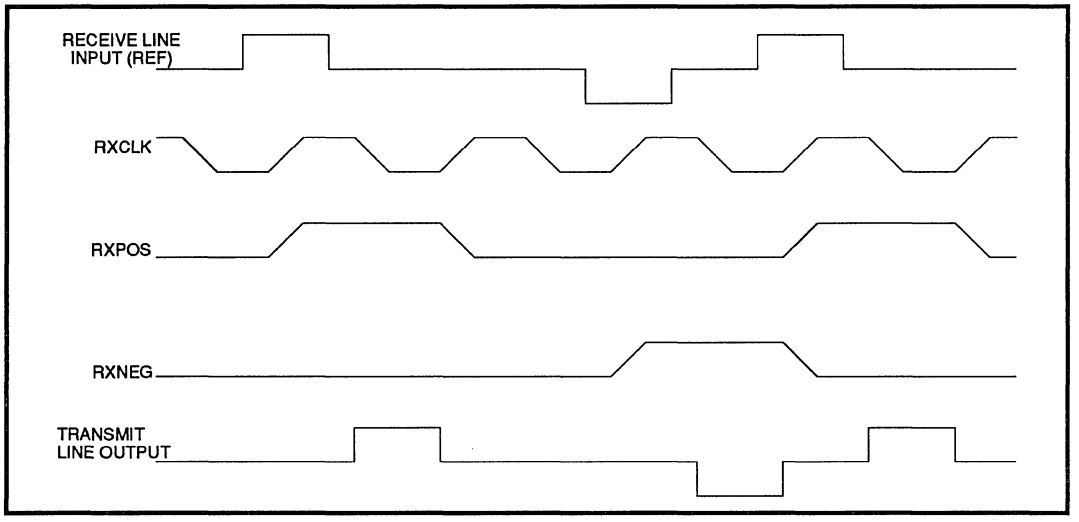


FIGURE 4: Line Loopback Waveforms

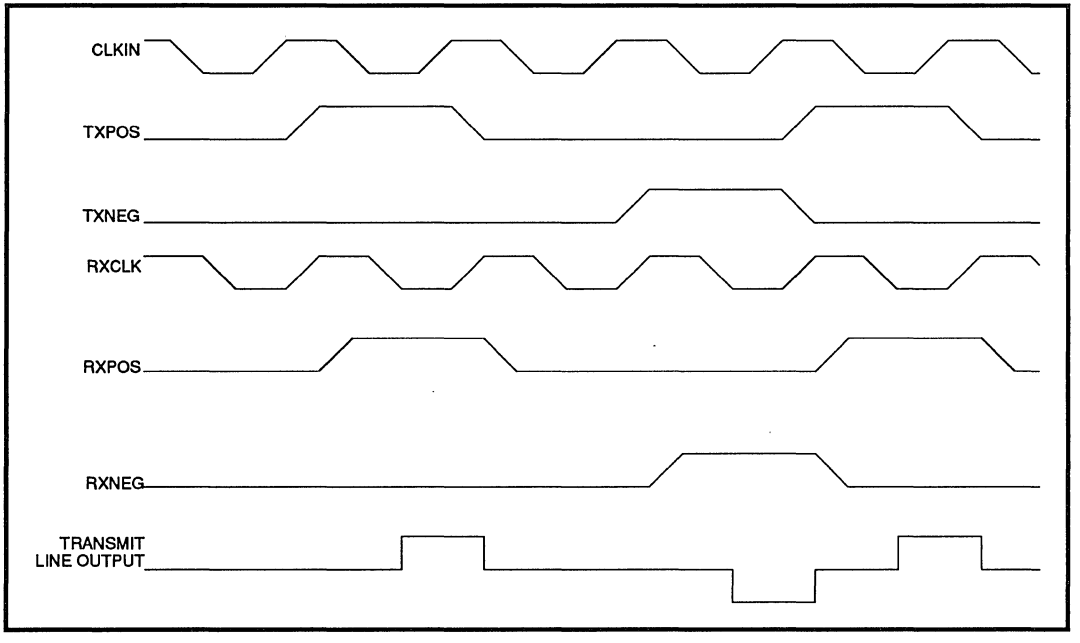
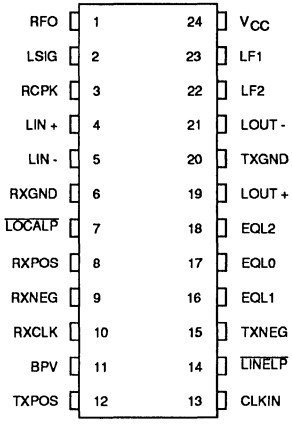


FIGURE 5: Local Loopback Waveforms

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



PIN DIAGRAM FOR ALL PACKAGES

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P233, DS-1 Line Interface - 24-Pin		
Standard Width Plastic DIP (600 mil)	SSI 78P233-CP	78P233-CP
Narrow Width Plastic DIP (300 mil)	SSI 78P233-CS	78P233-CS
Small Outline	SSI 78P233-CL	78P233-CL

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 731-5457

SSI 78P234
2048 KBit/s PCM Interface Unit

July, 1990

DESCRIPTION

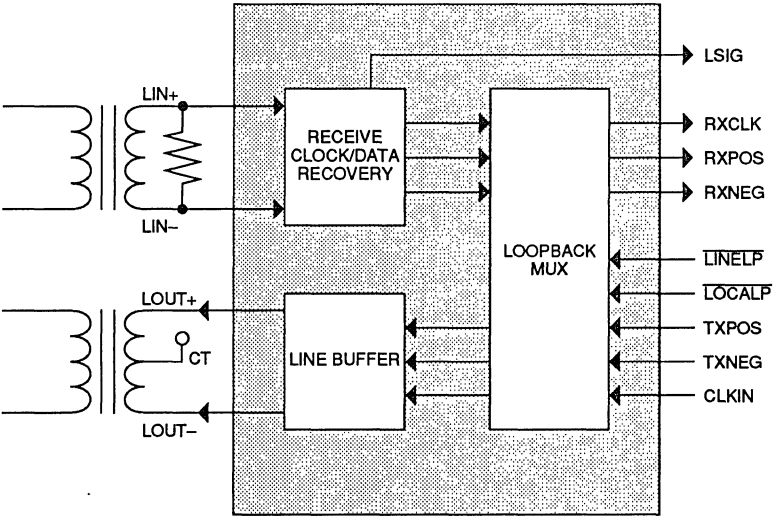
The SSI 78P234 PCM Interface Unit is a bipolar integrated circuit which performs the functions of receiving and transmitting PCM signals in an Alternate-Mark-Inversion (AMI) format. The receiver accepts AMI-format line data and provides separated and synchronized TTL-level data and clock outputs. High-density bipolar three-encoded (HDB3) signals are passed through the chip transparently. The transmitter accepts TTL-level data and clock, typically HDB3-encoded, and produces AMI-format pulses of the appropriate shape for transmission. A loopback multiplexer is also provided that permits interchange of the signals between the sections. The SSI 78P234 requires a single 5V supply, and is available in both 20-pin DIP and small outline (SO) packages.

FEATURES

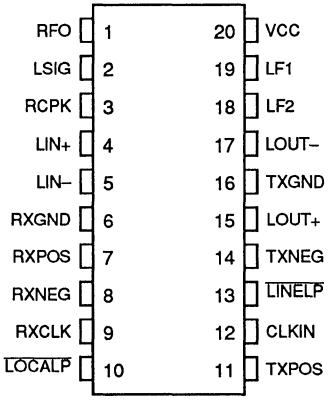
- **High-performance, low-cost solution for 2048 KBit/s PCM interface applications**
- **Both transmit and receive circuitry in a compact, 20-pin package**
- **Compliant with CCITT recommendations G.703 and G.823**
- **Unique clock-recovery circuit, requires no crystals or tuned components**
- **Standard unipolar TTL-level clock and data ports for easy equipment interface**
- **Line-loopback and local-loopback control**
- **Loss-of-signal indication**
- **Available in SO or dual-in-line packages**

5

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The device consists of receiver and transmitter sections together with a "loopback" means which permits interchange of signals between the sections (see Figure 1).

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. To provide a tracking threshold for amplitude-detecting these pulses, the signal is peak detected and a fixed percentage of the peak value is applied to the comparators which detect individual positive and negative pulses. An external R-C network is required to provide the proper storage of the peak reference value. Should the detected peak value fall below an acceptable level, the Loss of Signal (LSIG) output becomes active. This output may be used as a logical control signal or is able to drive a fault indicator LED directly.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase-locked-oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. Non-precision external components are required, however, to establish the oscillator center frequency and loop bandwidth.

The phase-locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line. Note that the transmitter output pulse widths are determined by the input clock width, so that it must be carefully controlled to provide acceptable outputs.

The transmitter pulse selection logical function is arranged so that the simultaneous occurrence of both positive and negative transmit data inputs inhibits the output driver. Moreover, the driver has a current-limiting feature which protects the circuit in the event of a shorted load or inadvertent shorting of an output to the supply voltage.

LOOPBACK CONTROL SECTION

The loopback control section is essentially a multiplexer which is capable of directing received data and clock to the transmitter section, or directing transmit input data and clock to the receiver outputs. This "looping" is controlled by two active low logic signals, $\overline{\text{LINELP}}$ and $\overline{\text{LOCALP}}$, respectively.

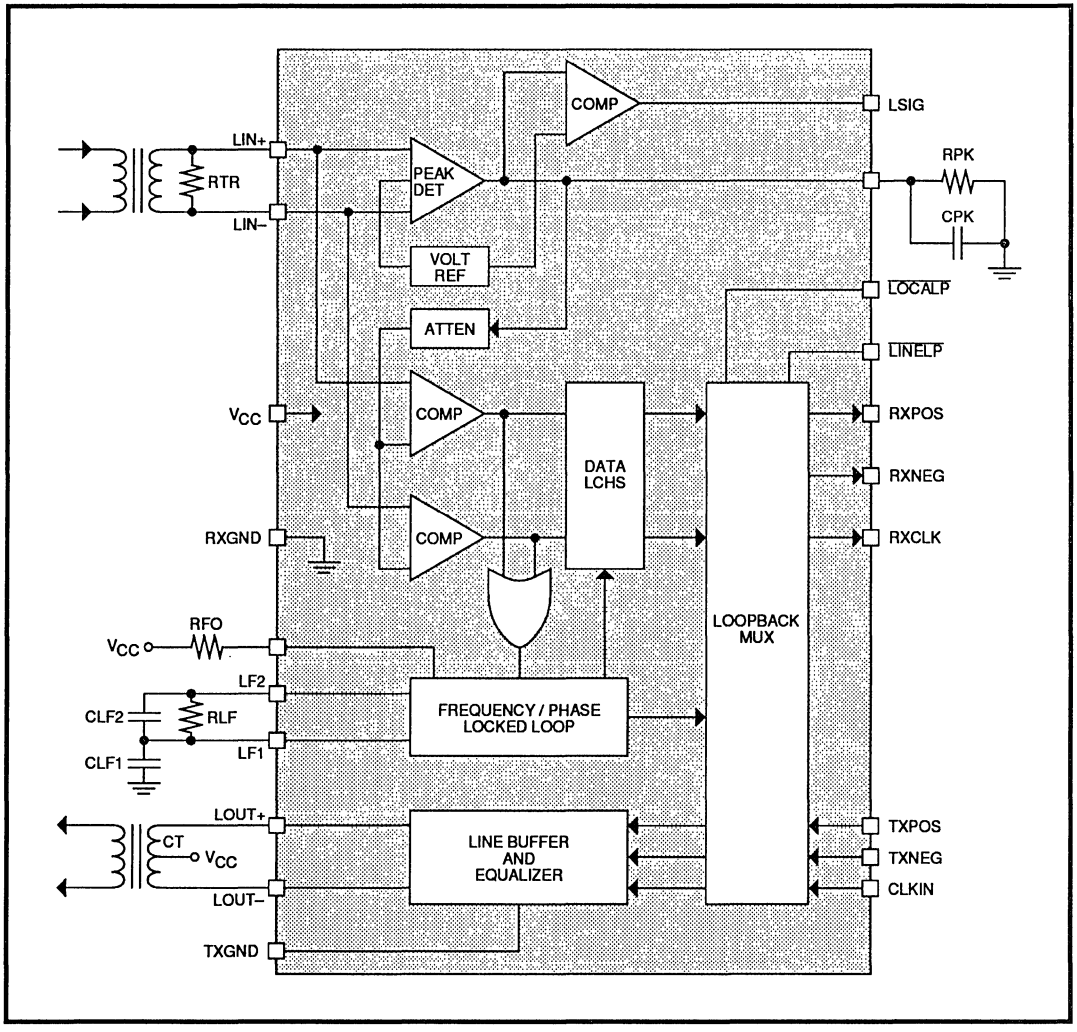


FIGURE 1: SSI 78P234 Functional Diagram

PIN DESCRIPTION

RECEIVER

I/O	LABEL	PIN NO.	DESCRIPTION
I	LIN+, LIN-	4, 5	Differential inputs, transformer-coupled from line.
O	RXPOS	7	Unipolar receiver output, active as result of positive pulse at inputs.
O	RXNEG	8	Unipolar receiver output, active as result of negative pulse at inputs.
O	RXCLK	9	Clock pulses recovered from line data.
O	LSIG	2	Loss-of-signal output indicating that input signal is less than threshold value.

TRANSMITTER

I	TXPOS	11	Unipolar transmitter data input, active high.
I	TXNEG	14	Unipolar transmitter data input, active high.
I	CLKIN	12	Transmitter clock input. Controls transmit pulse width. Transmit is active when low.
O	LOUT+	15	Output to transformer for positive data pulses.
O	LOUT-	17	Output to transformer for negative data pulses.

LOOPBACK CONTROL

I	$\overline{\text{LINELP}}$	13	Low level causes receiver recovered data and clock to be connected to the transmitter. Data and clock continue to be present at receiver outputs.
I	$\overline{\text{LOCALP}}$	10	Low level causes transmitter input data and clock to be connected to the receiver outputs. Input data continues to be transmitted.

PIN DESCRIPTION (Continued)

EXTERNAL COMPONENT CONNECTION

I/O	LABEL	PIN NO.	DESCRIPTION
I	RFO	1	Resistor connected to V_{CC} to provide basic center frequency of receiver phase locked loop oscillator.
-	LF1 LF2	19 18	Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
-	RCPK	3	Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

-	Vcc	20	Positive supply terminal for receiver circuits.
-	RXGND	6	Ground terminal for receiver circuits.
-	TXGND	16	Ground terminal for transmitter driver circuits.

5

ABSOLUTE MAXIMUM RATINGS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING	UNIT
V_{CC}, Supply Voltage	-0.5 to +7.0	V
Storage Temperature	-65 to 130	°C
Soldering Temperature (10 sec.)	260	°C
Voltage Applied to Logic Inputs	-0.5 to +7.0	V
Maximum Power Dissipation	600	mW
Junction Operating Temperature	0 to +130	°C
NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ta	Ambient temperature		0		70	°C
V_{CC}	Power supply voltage		4.75		5.25	V
VIH	High-level input voltage		2.0			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current	LSIG pin only; VO = 1.5V	-7		-13	mA

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor			6.04		KΩ
RLF	Loop filter resistor			10		KΩ
CLF1	Loop filter capacitor			0.015		µF
CLF2	Loop filter capacitor			200		pF
RPK	Peak-detector resistor			36		KΩ
CPK	Peak-detector capacitor		0.0015	0.015	0.15	µF
	Transmit line transformer	Refer to Table 1		---		---

D. C. ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply current	All outputs open			100	mA
IIH	High-level input current	VIH = 2.7V			20	µA
IIL	Low-level input current	VIL = 0.4V			-0.36	mA
VOH	High-level output voltage	IOH = -400µA	2.7			V
VOL	Low-level output voltage	IOL = 4.0mA; IOL = 2.0 mA, LSIG pin			0.4	V
RIN	Receiver input resistance		800		1250	Ω

DYNAMIC CHARACTERISTICS AND TIMING, TRANSMITTER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. Transmit pulse characteristics are obtained using a line transformer which has the characteristics shown in Table 1, and with the appropriate resistive load. Refer to Figure 2.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			488		nsec
TTC	Transmit clock pulse width			244		nsec
TTCNT	Transmit clock negative transition time				10	nsec
TTCPT	Transmit clock positive transition time				10	nsec
TTPDS TTNDS	Transmit data set-up time		15			nsec
TTPDH TTNDH	Transmit data hold time		0			nsec
TTPL	Transmit positive line pulse width	Measured at transformer	TTC-5		TTC+5	nsec
TTNL	Transmit negative line pulse width		TTPL-5		TTPL+5	nsec
	Transmit line pulses waveshape	See Note				

Note: Characteristics are in accordance with Table 6 and Figure 15 of Rec. G.703.

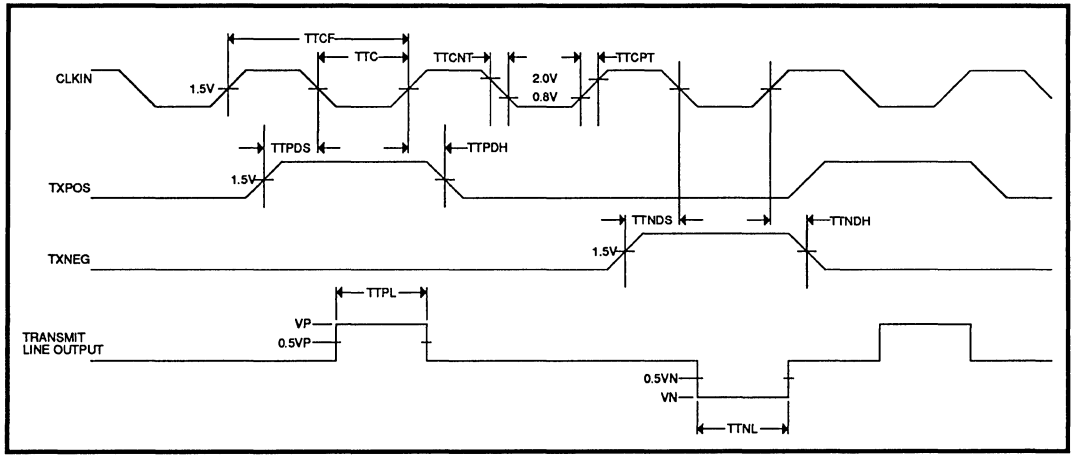


FIGURE 2: Transmit Waveforms

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. External component values as specified in Recommended Operating Conditions; see Note 1. Refer to Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage		±1.2		±3.9	Vpk
VLOS	Loss-of-signal indicating voltage		±0.5		±1.0	Vpk
TLOS	Loss-of-signal delay time	Timed from removal of input signal; See Note 2	0.7TPK		1.3TPK	sec
VDTH	Receive data detection threshold	Relative to peak amplitude	35		45	%
TSTAB	Receiver stabilization time	After application of input signal			5	msec
TRCF	Receive clock period			488		nsec
TRC	Receive clock pulse width			244		nsec
TRCPT	Receive clock positive transition time	C_L = 15pF			15	nsec
TRCNT	Receive clock negative transition time	C_L = 15pF			10	nsec
TRDP TRDN	Positive or negative receive data pulse width			488		nsec
TRDPS TRDNS	Receive data set-up time		210			nsec
TRDPH TRDNH	Receive data hold time		210			nsec
	Receive input jitter tolerance high frequency	sine, 18KHz to 100KHz	±100			nsec
	Receive input jitter tolerance low frequency	sine, 2.4 KHz	±750			nsec
KD	Clock Recovery Phase Detector Gain	(All 1's Data Pattern)	66		79	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Control Gain		0.40		0.55	Megrad/ sec. Volt

Note 1: Input signal is transformer coupled. In accordance with Paragraph 6.3 of Rec. G.703 and Table 2 of Rec. G.823.

Note 2: TPK = RPK x CPK x ln((VIN + 1.2v)/(VLOS + 1.2v))

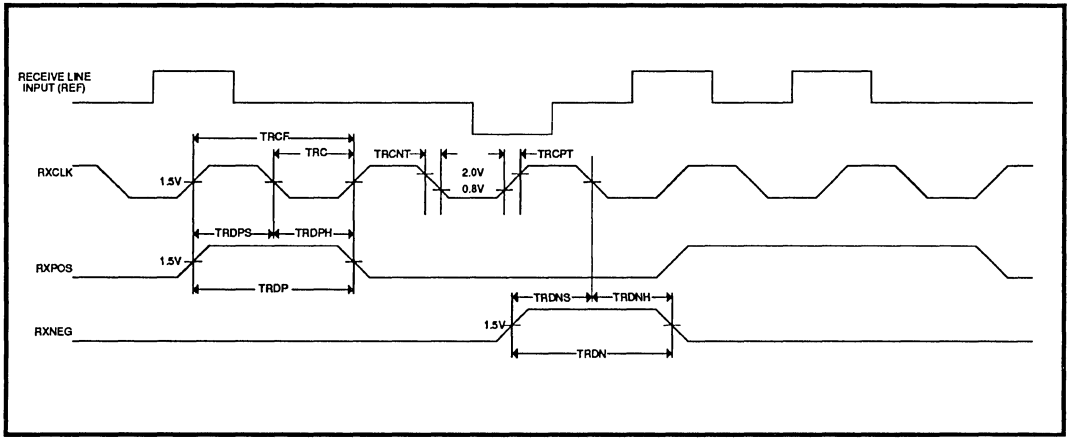


FIGURE 3: Receive Waveforms

5

LINE TRANSFORMERS

The SSI 78P234 is designed to connect to 75Ω coaxial or 120Ω symmetrical pair cabling. The transmitter must meet output pulse characteristics as specified by the CCITT (Table 6 of Rec. G.703) for each of these transmission media. It is important to choose a transformer that meets the specifications shown in Table 1 (below) to assure compliance with these requirements.

CHARACTERISTIC		SYMBOL	MIN	NOM	MAX	UNIT
Turns ratio	75Ω coax	N		2.53CT:1		
	120Ω twisted pair			2CT:1		
Primary open circuit inductance		Lp	3			mH
Primary leakage inductance		L1			4.0	µH
Primary volt-time product		ET	5			V-µsec
Primary DC resistance		Rp			2.5	Ω
Interwinding Capacitance		C_w			25	pF

TABLE 1: Transmit Line Transformer Characteristics

LINE TRANSFORMERS (Continued)

75Ω Coax Connection

Approximate turns ratios for connection to 75Ω coax are: 2.53 CT:1 for the transmitter and 1:1.26 (no CT) for the receiver. Some recommended transformers are listed in Table 2.

RCV/XMIT	TURNS RATIO	PART NUMBER	MANUFACTURER
XMIT	2.53CT:1	PE 64945	Pulse Engineering
XMIT	2.66CT:1	11816	Schott Corporation
RCV	1:1.26	PE 64938	Pulse Engineering

TABLE 2: Recommended Line Transformers for 75Ω Coax Connection

120Ω Symmetrical Pair Connection

Connection to 120Ω symmetrical pair requires a 2CT:1 ratio for the transmitter and 1:1 (no CT) on the receiver. Some recommendations are listed below.

RCV/XMIT	TURNS RATIO	PART NUMBER	MANUFACTURER
XMIT	2CT:1	1323	BH
XMIT	2CT:1	G52J12C	Pan-Mag
XMIT	2CT:1	11815	Schott Corporation
XMIT	1:1:1	PE 64931	Pulse Engineering
RCV	1:1	PE 64935	Pulse Engineering
RCV	1:1:1	G52J111P	Pan-Mag

TABLE 3: Recommended Line Transformers for 120Ω Symmetrical Pair Connection

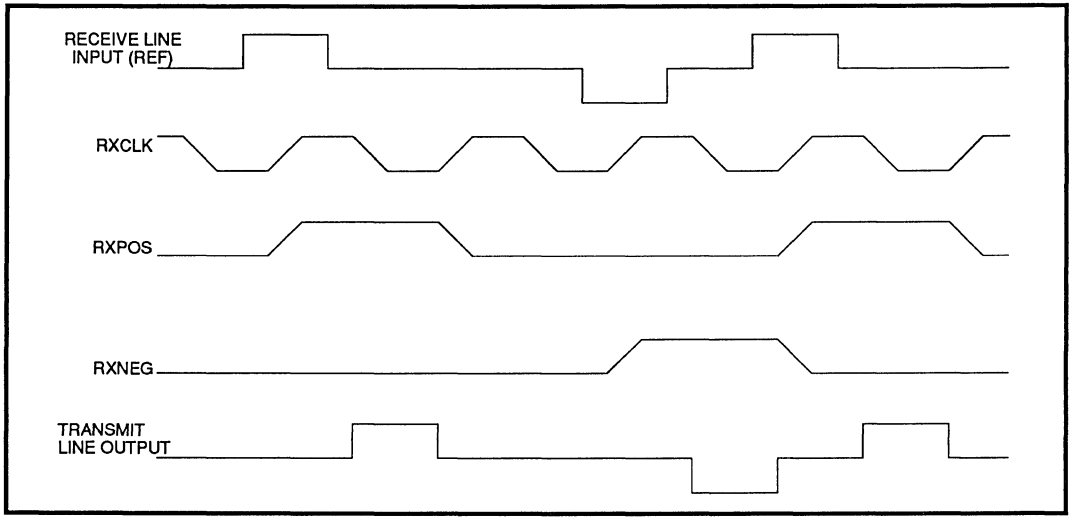


FIGURE 4: Line Loopback Waveforms

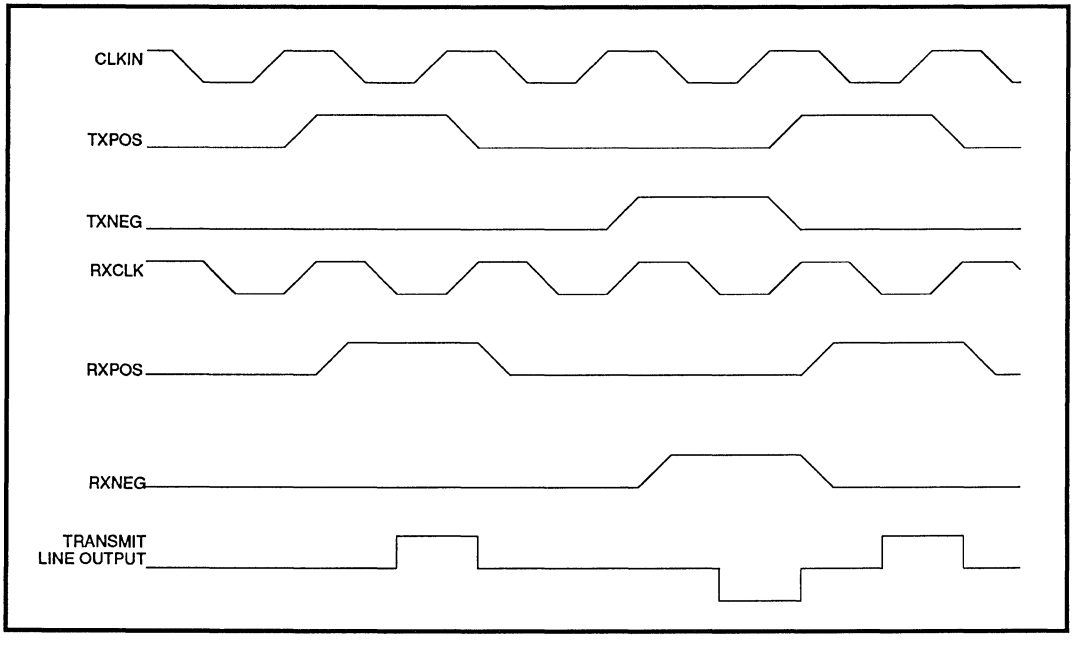
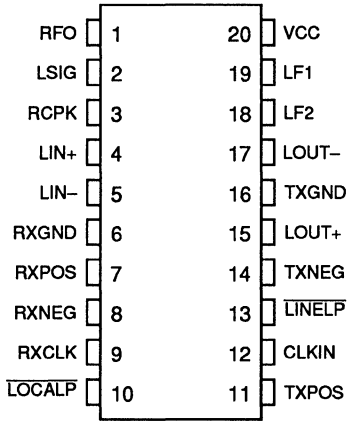


FIGURE 5: Local Loopback Waveforms

SSI 78P234
2048 KBit/s
PCM Interface Unit

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



20-Pin DIP, SO

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
SSI 78P234		
20-Pin Plastic DIP	SSI 78P234-CP	78P234-CP
20-Pin SO	SSI 78P234-CL	78P234-CL

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 731-5457

SSI 78P236
DS-3 Line Interface

Preliminary Data

July, 1990

DESCRIPTION

The SSI 78P236 is a line interface transceiver IC intended for DS-3 (44.736 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, data, and low-level signal detector logical outputs. The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) filter may be selected to attenuate the outgoing pulses for shorter line lengths. The SSI 78P236 requires a 5-volt supply and is available in DIP and surface mount packages.

FEATURES

- **Single chip transmit and receive interface for DS-3 (44.736 Mbit/s) applications**
- **Unique clock recovery circuit, requires no crystals or tuned components**
- **Selectable transmit line buildout to accommodate shorter line lengths**
- **Standard unipolar POS and NEG data and CLK ports**
- **Compliant with AT&T Compatibility Bulletin 119**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **Pin-compatible with SSI 78P2361 and 78P2362**

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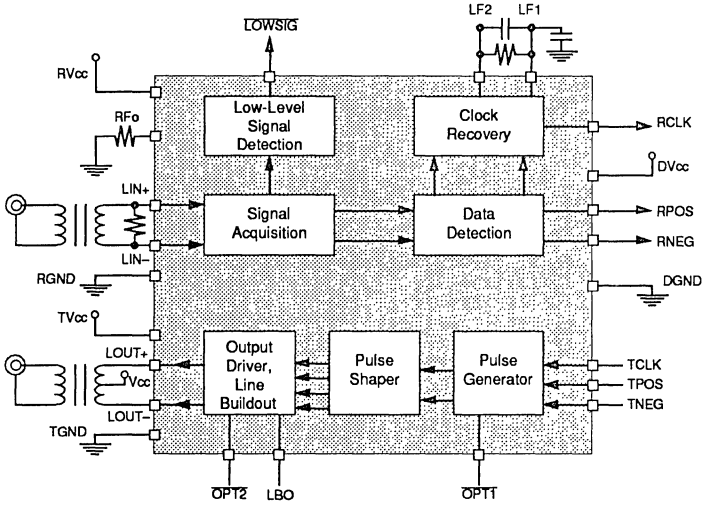
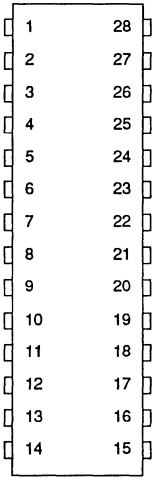
BLOCK DIAGRAM



PIN DIAGRAM



28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78P236 is intended to be used as a DS-3 Line Interface to perform the functions of receiving and transmitting pulse code modulated signals in an alternate mark inversion format. The receiver section accepts encoded line data and provides separated and synchronized data and clock outputs. The transmitter section accepts data and clock and produces alternate mark inversion pulses of the appropriate shape for transmission.

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. The Variable Gain Amplifier is used to adjust the signals applied to the Voltage Comparators to a relatively constant peak amplitude over the range of expected input levels. This is accomplished by means of the Peak Detector and AGC Amplifier wherein the amplified signal peaks are compared with a fixed reference voltage, and the filtered difference applied to the variable gain stage which cause the signal peaks to nearly equal the reference value.

The amplified positive and negative input data pulses are detected by high speed Voltage Comparators. The detection threshold is a fixed percentage of the peak value which is applied as the comparator reference. In this way, even though the input signal amplitude may fall below the minimum value which can be regulated by the variable gain circuits, the proper detection threshold is maintained.

Should the input signal fall below the minimum value which can be regulated, this condition is detected and indicated at the $\overline{\text{LOWSIG}}$ output. A time delay is provided before this output is active so that transient interruptions do not needlessly cause the indication.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits.
A single external resistor is used to establish the oscillator center frequency as well as other timing functions. The response characteristics for the phase locked loop is established by internal means with the provision to added external filter components in parallel.

The phase locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line.

An internal pulse shaper is selected with the LBO logic input so that the waveform at the terminal end of cable lengths less than 225 ft. is as required.

Note that the transmitter output pulse widths are not determined by the input clock width but is set internally.

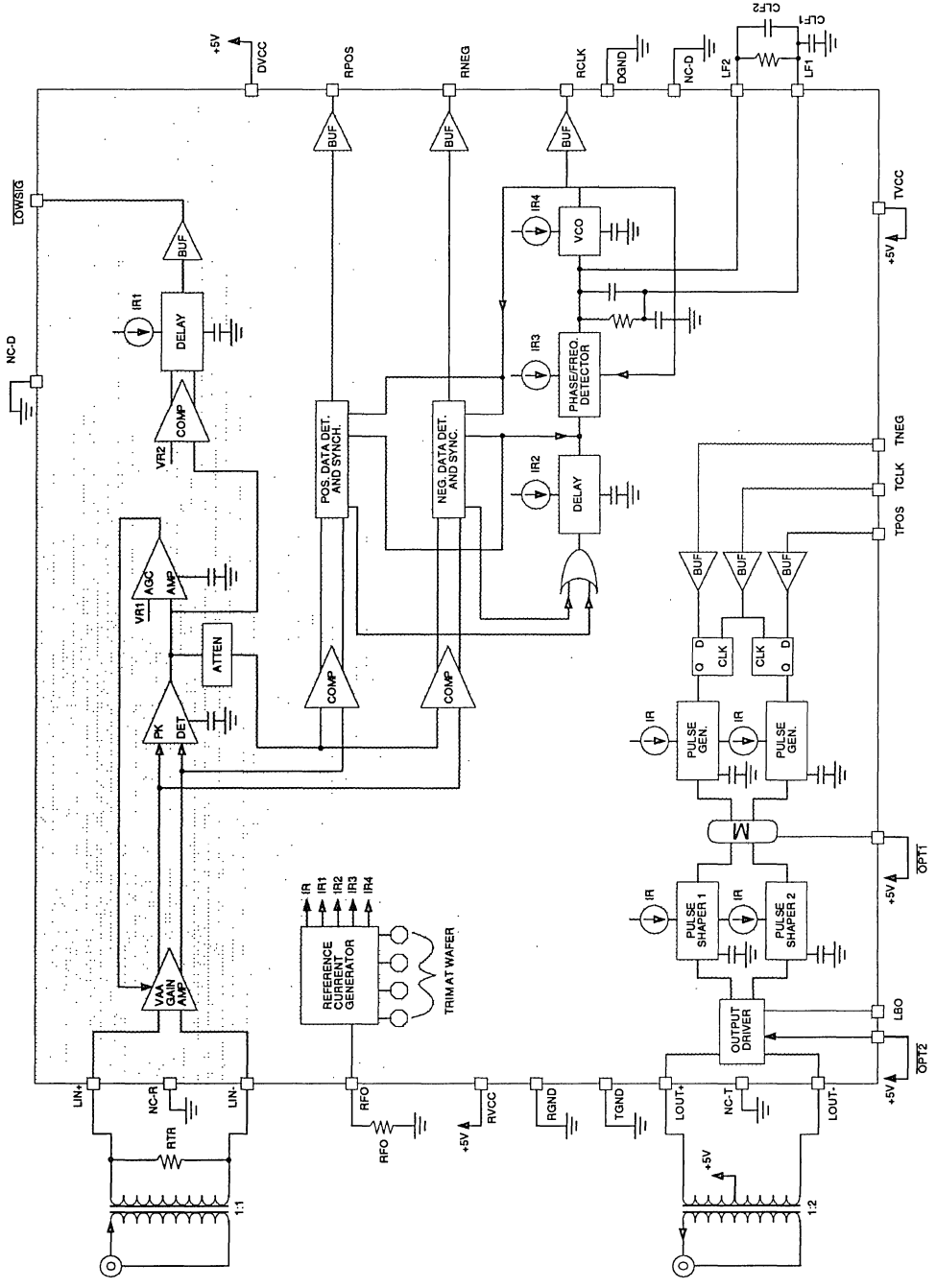


FIGURE 1: Functional Diagram

Note: NC pins should be tied to the ground pin indicated by the trailing letter.

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PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Selected for shorter cable lengths.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude when low.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to RGND to establish bandwidth of phase locked loop.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NC	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin (see figure 1) to minimize pin-to-pin coupling capacitance.

ELECTRICAL CHARACTERISTICS

(TA = 0°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOULUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive 5.0V supply: TVcc, RVcc, DVcc	6.0	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Ambient Operating Temperature, TA	0 to +85	°C
Pin Ratings: LIN+, LIN-, TPOS, TNEG, TCLK, LOUT+, LOUT-, LBO, RFO, LF2, LF1, $\overline{OPT1}$, $\overline{OPT2}$ Pins	-0.3 to Vcc +0.3	V
Pin Ratings: RPOS, RNEG, RCLK, $\overline{LOWSIG}$ Pins	-0.3 to Vcc +0.3	V
	+12	mA

SUPPLY CURRENTS AND POWER

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply Current	Outputs Unloaded, normal operation, transmit and receive all 1's pattern	111	142	174	mA
P	Power Dissipation	Outputs unloaded, TA = 85°C			0.93	W

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor	1% tolerance		5.25		kΩ
RLF	Loop filter resistor			TBD		kΩ
CLF1	Loop filter capacitor			TBD		µF
CLF2	Loop filter capacitor			TBD		pF
	Transmit line transformer			TBD		

ELECTRICAL CHARACTERISTICS (Continued)

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, $\overline{\text{OPT1}}$.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input low voltage		-0.3		1.5	V
VIH	Input high voltage		3.5		Vcc +0.3	V
IIL	Input low current	VIL = 1.5V	-5.0		5.0	µA
IIH	Input high current	VIH = 3.5V	-5.0		5.0	µA
VOL	Output low voltage	IOL = 0.1 mA			1.0	V
VOH	Output high voltage	IOH = -0.1 mA	4.0			V

$\overline{\text{OPT2}}$ CHARACTERISTICS

VIL	Input low voltage	IIL = 0.4 mA			0.5	V
VIH	Input high voltage		2.0			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled in accordance with Table 8 of AT&T Compatibility Bulletin 119.
2. RFO = 5.25 kΩ
3. The circuit is connected as in Figure 1.

VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		50		%
VLOW	Receive data low signal threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input	60		85	mV
VLOWT	Receive data low signal delay	Relative to peak amplitude for 22.37 MHz sinusoidal input		500		ns
TSTAB	Receiver stabilization time	After application of input signal			300	µs
TRCF	Receive clock period			22.35		ns
TRC	Receive clock pulse width			11.18		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns

RECEIVER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRDP TRDN	Positive or negative receive data pulse width			22.35		ns
TRDPS TRDNS	Receive data set-up time		8.7	11.18	13.7	ns
TRDPH TRDNH	Receive data hold time		8.7	11.18	13.7	ns
	Receive input jitter tolerance	sine, 60 kHz	±3.35			ns
	high frequency	to 300 kHz	0.3			UI
	Receive input jitter tolerance	sine, 10 Hz to 2.3 kHz	±55.88			ns
	low frequency		5.0			UI
KD	Clock Recovery Phase Detector Gain	All 1's data pattern KD = .418/RFO	74	80	86	µA/Rad
KO	Clock Recovery Phase Locked Oscillator		16	17	18	Mrad/ sec. -Volt

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TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics TBD.
2. The circuit is connected as in Figure 1.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			22.35		ns
TTC	Transmit clock pulse width			11.18		ns
TTCNT	Transmit clock negative transition time			4.5	6	ns
TTCPT	Transmit clock positive transition time			4.5	6	ns
TTPDS TTNDS	Transmit data set-up time		2.5	11.18		ns
TTPDH TTNDH	Transmit data hold time		2.5	11.18		ns
TTPL	Transmit positive line pulse width	Measured at transformer, LBO = Low	10.62	11.18	12.0	ns

TRANSMITTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTNL	Transmit negative line pulse width	Measured at transformer, LBO = Low	10.62	11.18	12.0	ns
TTEQ	Equalized transmit pulse shape	Measured at transformer, LBO = High		TBD		
	Transmit line pulse waveshape	See Note				

Note: Characteristics are in accordance with paragraph 5.2.2 of AT&T Compatibility Bulletin 119.

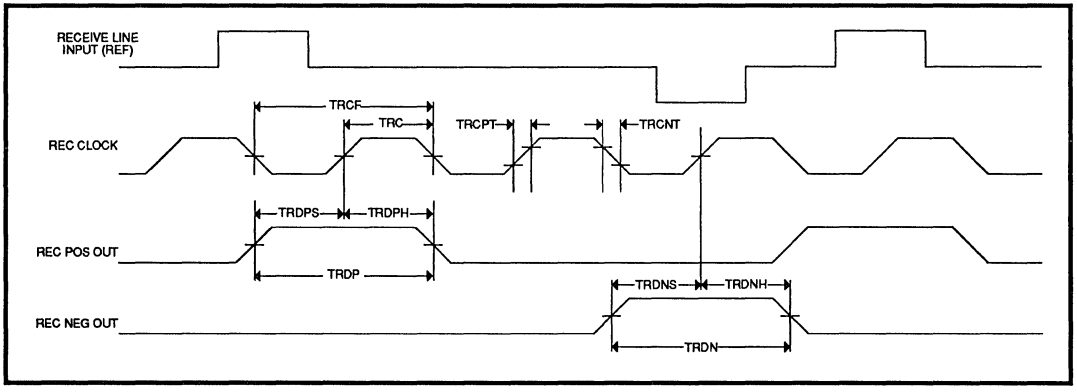


FIGURE 2: Receive Waveforms

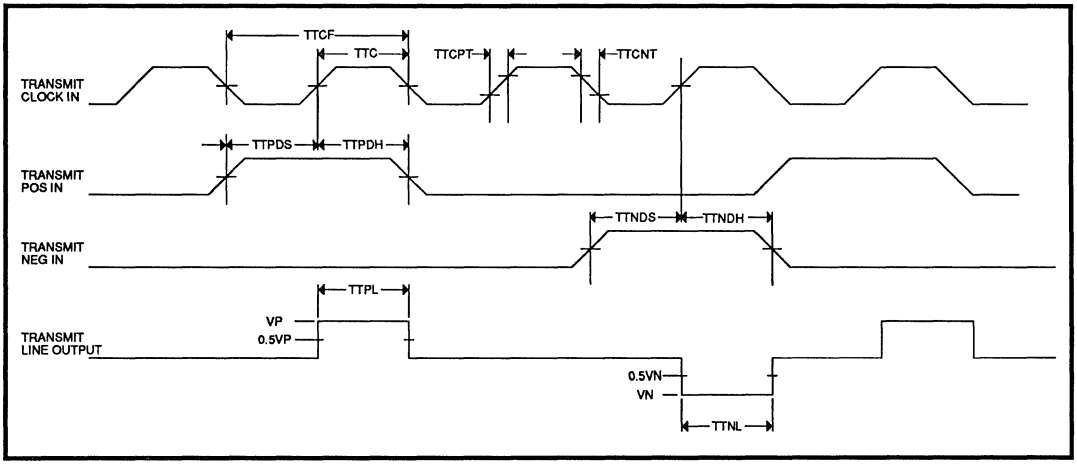
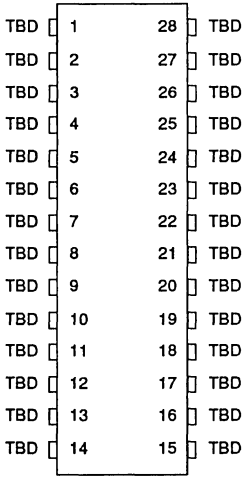


FIGURE 3: Transmit Waveforms

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



28-Pin DIP

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P236, DS-3 Line Interface - 28-pin		
Standard Width Plastic DIP (600 mil)	SSI 78P236-CP	78P236-CP
Surface Mount - TBD		

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX (714) 731-5457

Notes:

SSI 78P2361
STS-1 Line Interface

Advance Information

July, 1990

DESCRIPTION

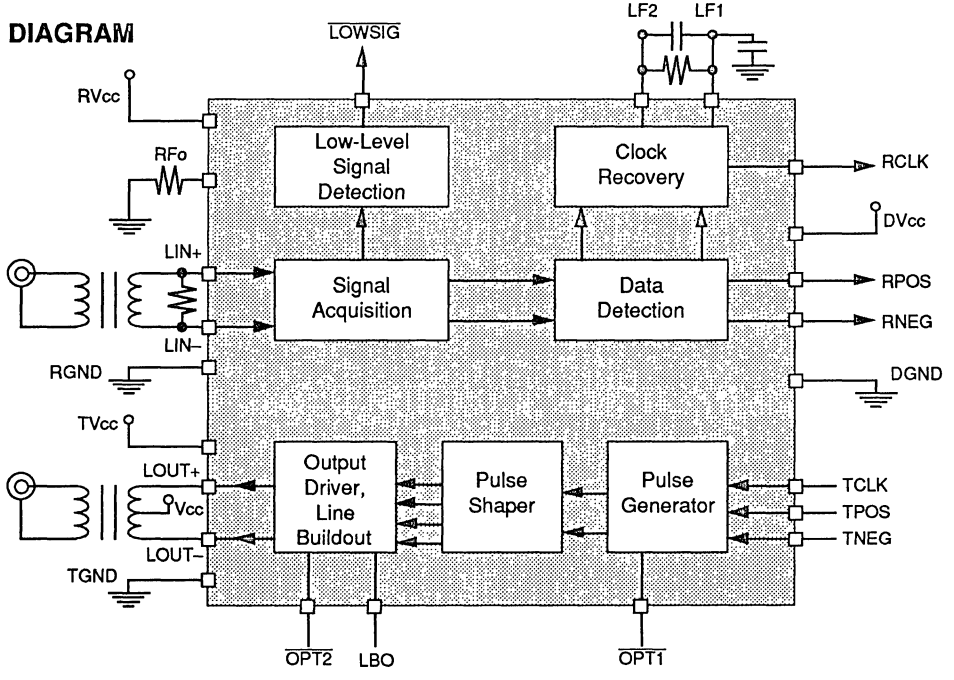
The SSI 78P2361 is a line interface transceiver IC intended for STS-1 (51.84 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, data, and low-level signal detector logical outputs. The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) filter may be selected to attenuate the outgoing pulses for shorter line lengths. The SSI 78P2361 requires a 5-volt supply and is available in DIP and surface mount packages.

FEATURES

- **Single chip transmit and receive interface for STS-1 (51.84 Mbit/s) applications**
- **Unique clock recovery circuit, requires no crystals or tuned components**
- **Selectable transmit line buildout to accommodate shorter line lengths**
- **Standard unipolar POS and NEG data and CLK ports**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **Pin-compatible with SSI 78P236 and 78P2362**

5

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Selected for shorter cable lengths.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude when low.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to RGND to establish bandwidth of phase locked loop.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NC	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin to minimize pin-to-pin coupling capacitance.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

RECEIVER

Input signal is transformer coupled.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		50		%
TSTAB	Receiver stabilization time	After application of input signal			300	µs
TRCF	Receive clock period			19.3		ns
TRC	Receive clock pulse width			9.65		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns
TRDP TRDN	Positive or negative receive data pulse width			19.3		ns
TRDPS TRDNS	Receive data set-up time			9.65		ns
TRDPH TRDNH	Receive data hold time			9.65		ns
	Receive input jitter tolerance high frequency	TBD	TBD			ns
	Receive input jitter tolerance low frequency	TBD	TBD			ns

5

ELECTRICAL CHARACTERISTICS (Continued)

TRANSMITTER

Transmit pulse characteristics are obtained using 0-450 feet of 728A coaxial cable with the appropriate line transformer (to be specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			19.3		ns
TTC	Transmit clock pulse width			9.65		ns
TTCNT	Transmit clock negative transition time			4.5		ns
TTCPT	Transmit clock positive transition time			4.5		ns
TTPDS TTNDS	Transmit data set-up time			9.65		ns
TTPDH TTNDH	Transmit data hold time			9.65		ns
TTPL	Transmit positive line pulse width	Measured at transformer		9.65		ns
TTNL	Transmit negative line pulse width	Measured at transformer		9.65		ns
	Transmit line pulse waveshape			TBD		

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 731-7110, FAX: (714) 731-5457

SSI 78P2362
34.368 Mbit/s Line Interface

Advance Information

July, 1990

DESCRIPTION

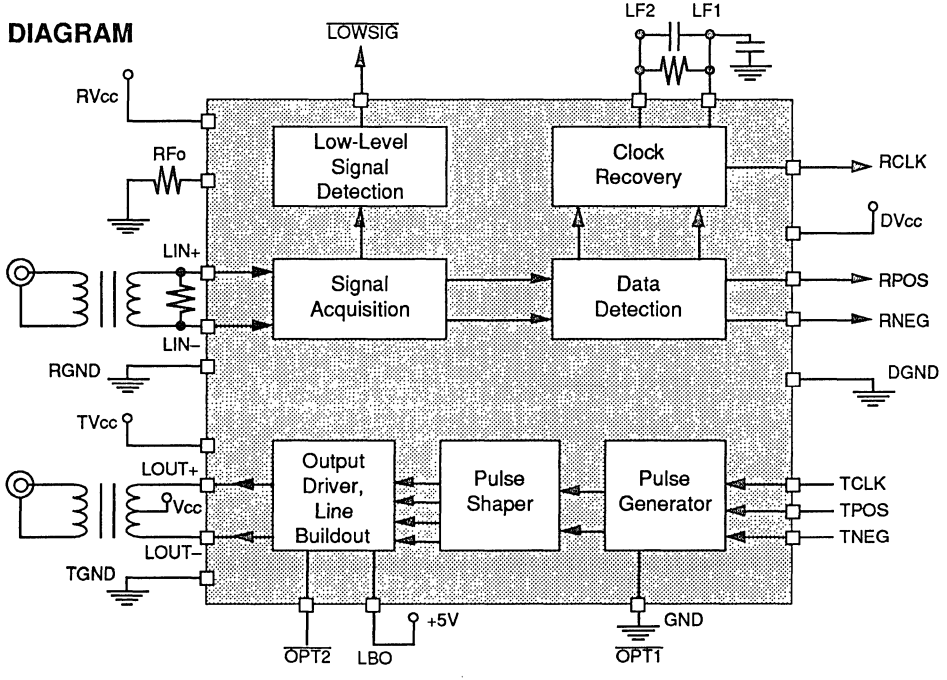
The SSI 78P2362 is a line interface transceiver IC intended for 34.368 Mbit/s applications. The receiver has a very wide dynamic range and is designed to accept HDB3-encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, data, and low-level signal detector logical outputs. The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. The SSI 78P2362 requires a 5-volt supply and is available in DIP and surface mount packages.

FEATURES

- **Single chip transmit and receive interface for 34.368 Mbit/s applications**
- **Unique clock recovery circuit, requires no crystals or tuned components**
- **Standard unipolar POS and NEG data and CLK ports**
- **Compliant with CCITT recommendations G.703 and G.823**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **Pin-compatible with SSI 78P236 and 78P2361**

5

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Attenuates output pulses. Should be tied high for normal CEPT E3 applications
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude. Should be tied low for normal CEPT E3 applications.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to RGND to establish bandwidth of phase locked loop.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NC	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin to minimize pin-to-pin coupling capacitance.

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

RECEIVER

Input signal is transformer coupled.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		50		%
TSTAB	Receiver stabilization time	After application of input signal			300	µs
TRCF	Receive clock period			29.1		ns
TRC	Receive clock pulse width			14.55		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns
TRDP TRDN	Positive or negative receive data pulse width			29.1		ns
TRDPS TRDNS	Receive data set-up time			14.55		ns
TRDPH TRDNH	Receive data hold time			14.55		ns
	Receive input jitter tolerance high frequency	sine, 10 kHz to 800 kHz	±2.18			ns
	Receive input jitter tolerance low frequency	sine, 100 Hz to 1.0 kHz	±21.83			ns

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ELECTRICAL CHARACTERISTICS (Continued)

TRANSMITTER

Transmit pulse characteristics are obtained using a test load of 75Ω with the appropriate line transformer (to be specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			29.1		ns
TTC	Transmit clock pulse width			14.55		ns
TTCNT	Transmit clock negative transition time			4.5		ns
TTCPT	Transmit clock positive transition time			4.5		ns
TTPDS TTNDS	Transmit data set-up time			14.55		ns
TTPDH TTNDH	Transmit data hold time			14.55		ns
TTPL	Transmit positive line pulse width	Measured at transformer		14.55		ns
TTNL	Transmit negative line pulse width	Measured at transformer		14.55		ns
	Transmit line pulse waveshape	See Note		TBD		

Note: Characteristics are in accordance with CCITT recommendation G.703, Figure 17 and Table 8.

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Section

CUSTOM/ SEMICUSTOM CAPABILITIES

6

silicon systems®

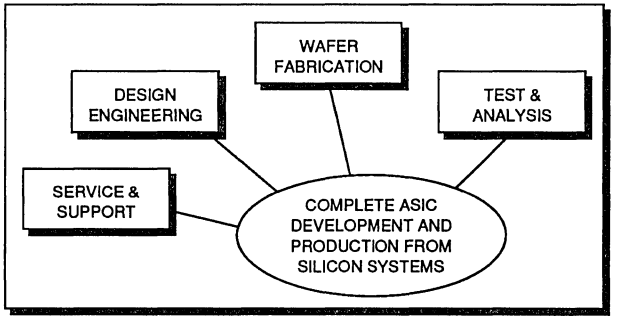
Custom/Semicustom Capabilities

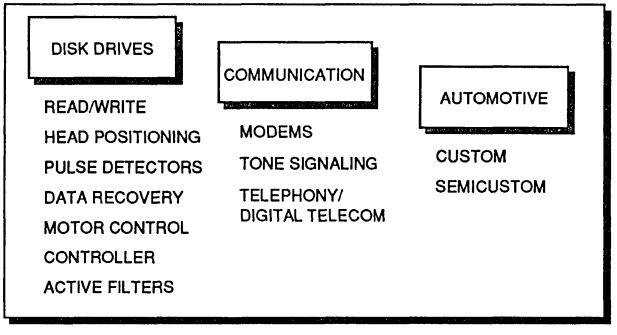
SILICON SYSTEMS LEADS THE WAY DEVELOPING MIXED-SIGNAL CUSTOM/SEMICUSTOM PRODUCTS

Silicon Systems is committed to leadership in the development of high-performance, application-specific, custom/semicustom Mixed-Signal Integrated Circuits (MSICs™).

Silicon Systems offers innovative designs for digital, analog, and mixed analog/digital ICs; a versatile range of CMOS and bipolar processes; quick-turn design methodologies supported by advanced and integrated design automation tools; specialized manufacturing facilities; comprehensive test, quality assurance, and prototype assembly programs; and nearly 20 years of IC design experience. Silicon Systems' efforts pay off by dramatically reducing the time (and cost) it takes to deliver the most optimized custom/semicustom ICs available.

Whether a customer's application falls in Silicon Systems' specialty areas of communications, storage products, automotive, or other areas, Silicon Systems' technical capabilities turn designs around faster and minimize a product's time to market for the competitive advantage.





6

Custom/Semicustom Capabilities

BROAD RANGE OF ANALOG AND DIGITAL DESIGN EXPERIENCE

With a broad base of experience, systems knowledge, and applications expertise, Silicon Systems' designers provide creative IC solutions in both CMOS and bipolar process technologies for analog, digital, and mixed-signal applications.

In CMOS, Silicon Systems has designed digital products ranging from FIFOs to complex hard-disk drive controllers. Combined analog/digital products range from cross-point switches to complete, one-chip 2400 bit/s modems.

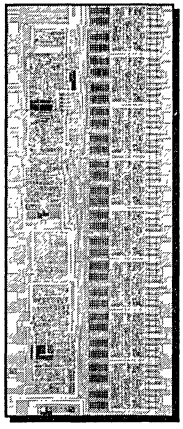
In bipolar, Silicon Systems' design expertise focuses on applications requiring high-speed ECL logic combined with high-performance analog circuitry. Bipolar products range from low-noise amps to very sophisticated data separators that employ patented phase locked loops.

Technique	Application	Silicon Systems Designed Examples
CMOS Signal Processing	For analog continuous time and sampled data (switched-capacitor implementation) and Digital Signal Processing (DSP) applications. Low-power capability also allows inclusion of ROMs, RAMs, and other analog/digital subsystems.	• 73K224 complete single-chip 2400 bit/s modem • C301 single-chip telephone headset amplifier • 14.4 kbit modem • Direct-broadcast satellite descrambler • Motor controllers • Hi-resolution analog data acquisition
Bipolar Signal Processing	For high-performance, low noise, wideband signal acquisition and processing applications. Offers TTL and/or ECL logic interfaces with high current drive.	• Sub 1 nV/sHz HDD R/W amplifiers • AGC, pulse detection amplifiers • High-speed data separators • Wideband transceivers • PLLs (Phase Locked Loops) • Optical signal processing
Digital CMOS	ForASIC controllers, sequencers and data path applications with on-board ROM, RAM, and PLA sub-systems. Offers standard TTL and/or CMOS logic interfaces.	• Hard disk drive controllers • SCSI interface controllers • UARTs • Protocol controllers • Digital signal processors
Digital Bipolar	High-speed logic and interface circuitry. Offers standard logic or custom interfaces.	• Encoders and decoders • High-speed digital transceivers

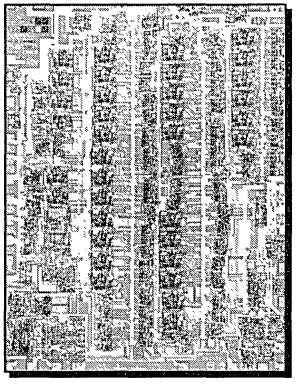
FULL ANALOG AND DIGITAL INTEGRATION ON THE SAME CHIP

Silicon Systems leads its competition in the design of complete systems on a chip which combine complex analog and digital functions. The total system solution approach allows designers to satisfy their application, cost, and performance objectives.

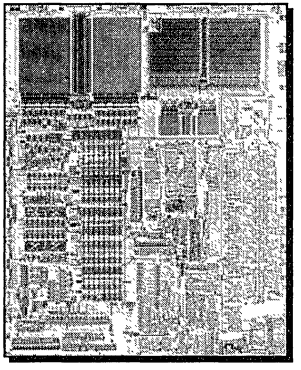
Custom mixed-signal Bipolar low-noise read/write IC



Standard Bipolar mixed-signal, high-performance data separator



Standard product single-chip 2400 bit/s modem with switched capacitor filters and RISC DSP



"DESIGN-FOR-TESTABILITY" AND TEST SUPPORT

Silicon Systems employs design-for-testability methodologies, such as built-in test modes that allow direct testing of internal subsystems. Silicon Systems uses highly specialized equipment, test programs and test procedures for combined analog/digital designs to ensure delivery of high-quality product. To determine product reliability under extreme conditions, products are tested in-house by a wide variety of advanced analog or digital testers including:

- LTX (TS88/DX90) testers
- Trillium Micromaster Plus
- Teradyne A520

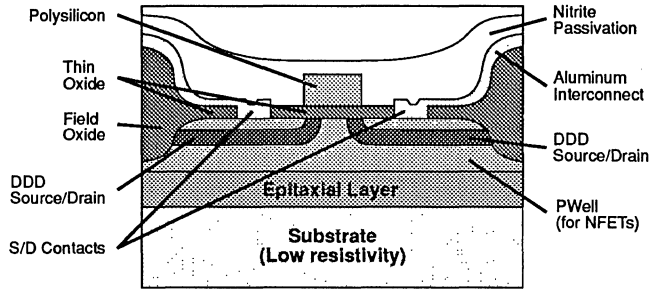
These testers are supported by:

- Automatic handlers (Trigon PLCC, Symtek & Tesec SOIC, and MCT DIP and Delta QFP)
- Burn-in sockets, temperature chambers, Aehr burn-in ovens, and Highly Accelerated Stress Test (HAST)

CMOS PROCESS TECHNOLOGIES

Silicon Systems' mixed signal CMOS processes are used to implement low-power, highly integrated systems solutions.

The two main processes used for new designs are CH (for 12V applications) and CG (for 5V applications). These processes are summarized in the table below. Other production process technologies (such as metal gate) are not utilized for new designs.



CH CMOS PROCESS TRANSISTOR

Process	Type	Application Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches Poly 1	Metal 1	Metal 2	Features
CH	Si-Gate, single metal, dual poly, P Well	12V	18 V	3.6μ	5.8μ	6.4μ	n/a	• DDD S/D structure • Poly-poly capacitors • Low-voltage coefficient • High Ω/□poly resistors • Epi substrate option • Buried Well-ring
CG	Si-Gate, dual metal, dual poly, P Well	5V	7V	1.5μ	3.0μ	4.5μ	6.0μ	• DDD S/D structure • Poly-poly capacitors • Shrinkable to 1.2μ

CMOS PROCESS CHART

The CH process is used for applications requiring a higher (12V) voltage operation. This higher voltage operation is achieved through the use of a DDD (double diffused drain) source/drain structure. This increases the S/D junction grading and thus increases the breakdown voltage and lowers the associated junction capacitance. The CH process also provides low-voltage coefficient, precision poly-poly capacitors. These high quality capacitors support high performance switched-capacitor filtering and data conversion (A/D and D/A) circuits. "Digital" CMOS processes which have been modified to provide poly-diffusion capacitors do not support high performance analog applications such as those possible with poly-poly capacitors. Poly-poly capacitors have much lower voltage coefficients and do not have a large parasitic bottom place capacitor.

Another important feature for analog applications is found on the Silicon Systems CH process, high Ω/□poly resistors. These resistors have a low voltage coefficient which is very important for low distortion, continuous time filters such as in anti-aliasing applications. Typical CMOS processes provide only high value well resistors, which are unacceptable in these applications.

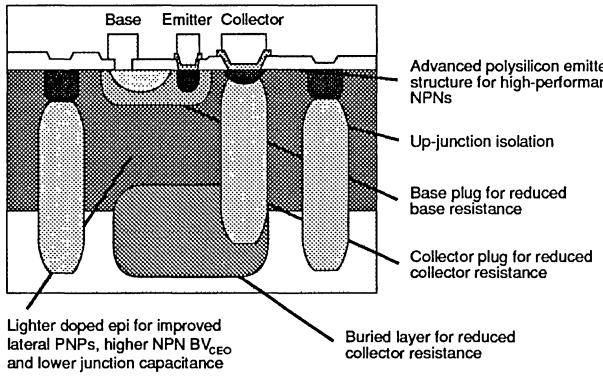
To improve the reliability of your system, Silicon Systems has incorporated a well ring into the CH process. This improves the well tie-down and increases the latchup immunity. In applications with harsh 'environments' (inductive motor drivers, automotive applications...) an epi substrate option is utilized for CH to increase latchup immunity to well over 200 mA.

The CG process is designed to support 5V mixed-signal systems. As the feature size (1.5μ) is significantly reduced over the CH process, much higher levels of system integration are possible. In addition to the much higher level of digital complexity possible, high performance analog circuitry is supported. Just as with the CH process, excellent poly-poly capacitors are available. The CG process is shrinkable to 1.2μ. Both the CH and CG process are proven production processes, thus minimizing your unknowns and risks.

BIPOLAR PROCESS TECHNOLOGIES

Silicon Systems uses its bipolar processes to implement high performance mixed-signal integrated circuits.

The two bipolar processes utilized for new designs are BK (12V) and BN (5V). These processes are summarized in the table below. Other production bipolar processes are not used for new designs.



BK BIPOLAR PROCESS NPN TRANSISTOR

Process	Type	BV_{CEO}	NPN Ft	Emitter Size	M1 Pitch	M2 Pitch	Features
BK	Junction-isolated	12V	2 GHz	2.5μ	9.0μ	14.0μ	• Polysilicon emitters • A1 Schottky diodes • Nitride capacitors • Ion implanted resistors • Up/down junction isolation • Collector/base plugs
BN	Oxide-isolated	6V	8 GHz	2.0μ	4.5μ	8.0μ	• High performance NPNs • PtSi Schotty diodes • Nitride capacitors • Ion implanted resistors • Sidewall oxide isolation • Collector/base plugs

BIPOLAR PROCESS CHART

The BK process is an analog/digital process technology used for applications requiring a higher voltage (12V) operation. Higher voltage operation is achieved through the use of lighter-doped epi, which also improves the performance (current gain and speed) of the lateral PNP transistors. Deep N+ and P+ enhancement layers are provided to reduce the collector series resistance and base resistance, respectively. Up-junction isolation is used to allow a significant reduction in device area as compared to conventional junction isolation methods. Metal-Poly capacitors with a nitride dielectric are provided in BK.

The BN process is a sidewall oxide-isolated bipolar process targeted at applications using 5V power supply. The use of oxide isolation greatly reduces the sidewall parasitic capacitances and allows the fabrication of very small transistors. A minimum size BN transistor consumes 1/5th the area of a minimum size BK transistor. The NPN transistors are available in walled and non-walled configurations with the additional option of recessed collectors to further reduce the base-collector capacitance. Excellent PtSi Schottky diodes are provided as well as nitride/oxide capacitors, dual layer metal, and 100-200 MHz lateral and substrate PNP transistors. The high performance NPN transistors can be used to make sub-nanosecond ECL and CML logic gates as well as high-precision, high-speed analog circuitry. The fine metal pitches and small device sizes produce very dense circuit designs. The intrinsic speed and packing density of this process allow the designer to implement high performance analog/digital systems.

MIXED-SIGNAL ARRAYS

The Mixed-Signal Array (MSA) series has been designed for those applications requiring both analog and digital circuits on a single chip.

Silicon Systems' Mixed-Signal Array program is a hardware and software system for automating integrated circuit design. The arrays are developed with Silicon Systems' Integrated Design Methodology (IDM™), a semicustom design technique for designing high density, high performance mixed-signal (analog and digital) arrays in both Bipolar and CMOS devices.

General Description

The MSA Series is a family of semiconductor arrays designed for efficient implementation of mixed analog/digital circuits. The series consists of seven base arrays ranging in complexity from 24 to 1608 digital gates, 8 to 40 analog cells, and 28 to 66 I/O pads.

Silicon Systems' Mixed-Signal Arrays are prefabricated integrated circuits consisting of tiles surrounded by a periphery of input/output tiles capable of a wide range of system interfaces. The Mixed-Signal Arrays employ a tile architecture which provides a systems designer with an open array of tiles containing unconnected active and passive semiconductor components. The components and tiles are interconnected to build specific electronic functions in combined analog and digital technology through the use of single tiles or tile/component combinations.

In Silicon Systems' integrated CAD/CAE environment, the designer has the option of using the predefined macros provided in the library, or he can use these macros as models for creating macros specific to his own needs. The designer also has the option of storing newly generated or modified macros in a library and reusing them in other designs at a later time.

ADVANTAGES OF MIXED-SIGNAL ARRAYS

The benefits of using arrays are:

- An array can be designed from concept to prototypes in ten to fifteen weeks.
- Manufacturing time is greatly reduced due to the prefabrication of base arrays.
- Arrays are economic. System size and cost are reduced. Power consumption is reduced but performance is generally enhanced.
- Arrays can be reconfigured to fit your unique design requirements.

FEATURES

- CMOS and Bipolar families
- Combines high performance analog and digital circuits on a single chip
- System speeds up to 2 GHz (bipolar)
- Twelve versatile arrays for a variety of applications
- High voltage capability
- ESD protection at each I/O pad
- Full CAE support on Mentor Graphics workstations
- Analog and digital macro library

MIXED-SIGNAL ARRAY	TECHNOLOGY	EQUIVALENT GATES	EQUIVALENT OP AMPS	BONDING PADS
6701	CMOS	1608	40	66
6702	CMOS	280	12	36
6703	CMOS	604	12	42
6704	CMOS	604	12	44
6901	Bipolar	96	24	48
6902	Bipolar	0	8	28
6903	Bipolar	24	26	52
6951	High Performance Bipolar	144	52	64
6952		24	16	40
6953		72	34	56
6954		144	16	56
6955		288	22	72

Silicon Systems Mixed-Signal Array Series

INTEGRATED DESIGN METHODOLOGY—THE IDM™ ADVANTAGE

Silicon Systems has spent almost 10 years developing its Integrated Design Methodology (IDM™). IDM™ consists of an interlocking set of design methods supported by a single Computer-Aided Engineering (CAE) and Computer-Aided Design (CAD) system. As IDM™ supports analog and digital designs in any of Silicon Systems' CMOS and bipolar technologies, it offers the tremendous advantage of flexibility.

COMPARE FULL-CUSTOM TO SEMICUSTOM DESIGN

IDM™ is based on two major design approaches: full-custom and semicustom.

Full-custom design is a "handcrafted" approach used to produce the most compact, high-performance design possible. Two approaches for full-custom physical design are possible: either composite or symbolic. In composite design, every process mask layer is drawn down to the process minimums. This yields the densest, highest-performance designs but is the most time-consuming approach. Symbolic design utilizes correct-by-construction, stick-like, process symbols, such as resistors, capacitors, and wires. Symbolic design is significantly more productive than composite and supports a higher level of circuit verification for greater design accuracy.

Semicustom design is an "automated" approach used to produce the most timely and cost-efficient designs possible. Two approaches are possible: either automatically placed-and-routed library components, including standard cells, or prefabricated array components.

Silicon Systems' analog and digital standard cells are pre-characterized, library-maintained circuits that are automatically placed and routed to generate a layout. The automatic place-and-route software also utilizes macro cell assemblers to route full-custom circuitry. The standard cell approach requires minimal layout effort, leading to lower development cost and a higher first article success rate.

Silicon Systems' mixed-signal arrays are bipolar and CMOS families of integrated circuits which are ninety percent prefabricated. The base arrays utilize a three-tile type core structure each of which is targeted for a specific design application, i.e., analog, digital, and reference. The three tile types forming the array core are separated by interconnect "highways" capable of handling both analog and digital signal busses. The core, in turn, is enclosed by a periphery of predefined I/O functions.

Array customization is achieved by the definition and interconnection of metal and poly-Si or double metal layers. Silicon Systems mixed-signal arrays provide a systems designer with fast prototype cycle times, lower integration costs, and the ability to migrate to either standard cell or custom integration with a minimum perturbation in design production.

CHOOSE THE OPTIMUM DESIGN APPROACH BASED ON TRADE-OFFS

Each IDM™ design approach offers unique cost, time, and performance trade-offs.

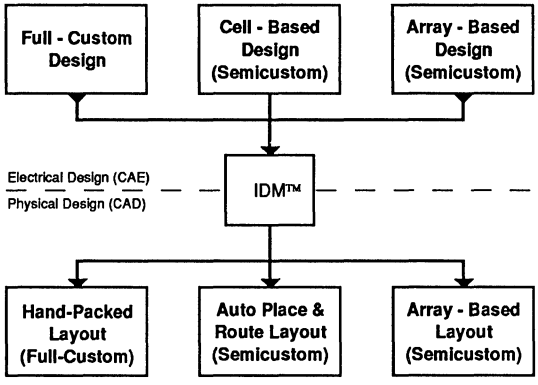
CUSTOM / SEMICUSTOM TRADE-OFFS

	Full - Custom		Semicustom	
	Composite Design	Symbolic Design	Cell-Based Design	Array-based Design
Design Parameters				
Cost (non-recurring expense)	1.0	0.5 - 0.8	0.4 - 0.7	0.2 - 0.4
Time (schedule)	1.0	0.5 - 0.7	0.4 - 0.6	0.2 - 0.4
Production Parameters				
Piece Price (production cost)	1.0	1.2 - 1.4	1.5 - 2.0	2.0 - 2.5
Die Size (silicon area)	1.0	1.1 - 1.2	1.3 - 1.6	1.6 - 2.0

Note: All comparisons are normalized to a composite-level design.

MIX FULL-CUSTOM AND SEMICUSTOM DESIGN ON A SINGLE CHIP

Due to the interlocking nature of Silicon Systems' design approaches, full-custom and semicustom design can be mixed on the electrical and/or physical design of any given IC.

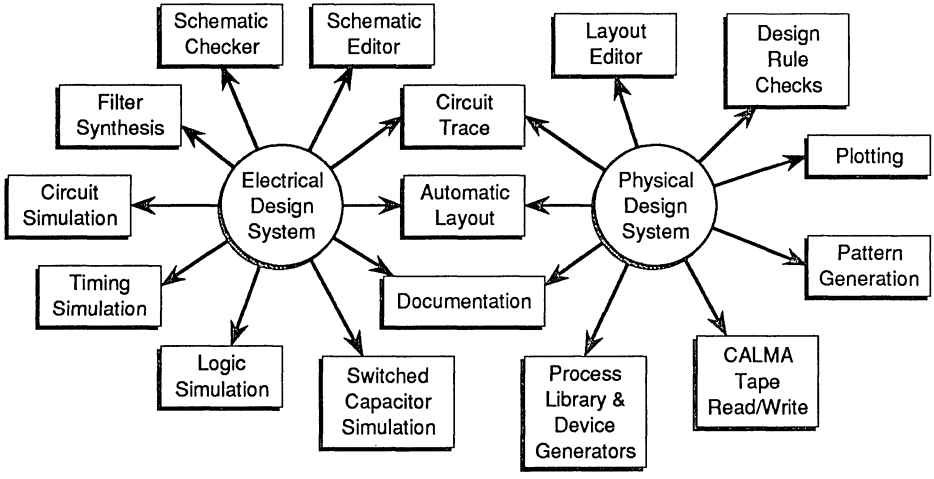


CONVERT SEMICUSTOM DESIGN INTO FULL-CUSTOM DESIGN

With its unique integrated design automation system, Silicon Systems can easily convert a semicustom design into full-custom circuitry. This capability allows Silicon Systems' customers to reduce production costs by converting an area-inefficient semicustom design into a high-performance full-custom design.

SOPHISTICATED DESIGN AUTOMATION TOOLS

The Pegasys™ design automation system, with proprietary and Silicon Systems-enhanced vendor software, addresses both the electrical and physical phases of design.



ELECTRICAL DESIGN

Electrical design is done on Mentor Graphics/Apollo engineering workstations with Silicon Systems-enhanced software that provides schematic capture, simulation, synthesis, and documentation tools. This software is supported by libraries of pre-designed cells and components. Due to our integrated CAE environment, there is no distinction between any schematic capture, simulation, or synthesis capabilities for full- or semicustom design approaches.

ANALOG & DIGITAL SIMULATION

Simulation ensures that we meet the customer's performance specification before converting the design into silicon. Circuit simulation, an important key to Silicon Systems' design methodology, allows us to accurately simulate the performance numbers of our technologies. For circuit simulation, we use Meta-Software's HSPICE™ with a proprietary analog CMOS model that accurately predicts output impedance and other analog parameters over a wide range of operating conditions and device sizes. The HSPICE environment includes a fully hierarchical netlister, a preprocessor called PHSPICE, and a Meta-Software graphic plotter called HSPLOT™. For the analog simulation of switched capacitors, we use Columbia University's SWITCAP™.

For digital simulation, we use a proprietary version of SimuCad's SILOS™ that performs gate and switch-level, zero-delay, functional logic and fault simulation. To analyze delays with a timing-based logic simulation, we use a combination of TSIM™ (developed on Meta-Software's Circuit Path Finder™) and SILOS.

DEVICE MODELING AND CHARACTERIZATION LABORATORY

Highly-accurate circuit simulation models and parameters are developed in Silicon Systems' state-of-the-art Device Modeling and Characterization (DMC) laboratory. With capabilities including precision AC measurement, RS1 statistical analysis, and worst-case modeling, the DMC lab provides complete device model data for our processes.

PHYSICAL DESIGN

Silicon Systems is in the process of converting its physical design system from a proprietary VAX-based system (ALICE) to an enhanced Mentor Graphics/Apollo-based system (ICgraph™). Both systems support a full range of capabilities, including graphical editing, design rule checking (DRC), circuit trace, and pattern generation (PG) in an integrated environment.

With the ALICE system, Silicon Systems pioneered a correct-by-construction device-level design methodology which has proven highly effective in the production of mixed analog/digital chips. Silicon Systems will embody this methodology within the Mentor Graphics-based system.

AUTOMATIC PLACE AND ROUTE SOFTWARE

Silicon Systems' cell-based automatic place-and-route capability, which is based on Cadence's TANCELL™ software, performs physical design far more rapidly than can be done by hand. Extensive proprietary software, developed to complement TANCELL, supports hierarchical routing, parameter passing, library creation and maintenance, and CMOS switched-capacitor analog macro generation directly from full-custom design. A random-logic digital macro assembler is in development. This flexible place-and-route environment supports floor planning, automatic chip construction, and the mix and match of custom cells, standard cells, and compiled cells—all of which are used to reduce design development time.

AUTOMATIC CIRCUIT TRACE AND VERIFICATION SOFTWARE

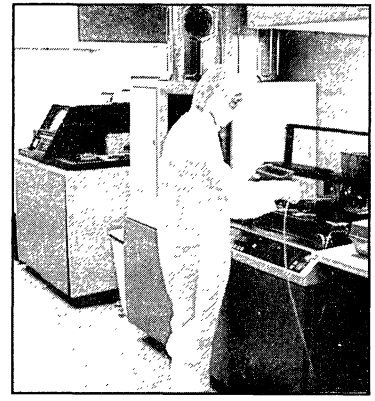
Using a proprietary circuit-trace program called ANITA™, we compare the completed IC layout database automatically to the Mentor schematic database to ensure that the layout implementation matches the schematic design exactly. When this trace program is applied to CMOS and bipolar mixed analog/digital designs, it performs a more detailed trace than is available through commercial layout-versus-schematic (LVS) packages. ANITA allows Silicon Systems to dramatically reduce design errors and minimize the time to product introduction.

DESIGN AUTOMATION BENEFITS

The proprietary Pegasys™ Design Automation system gives Silicon Systems the flexibility to create increasingly complex ASIC designs for our customers while dramatically reducing design schedules, costs, and errors.

MANUFACTURING SUPPORTS CMOS AND BIPOLAR TECHNOLOGIES

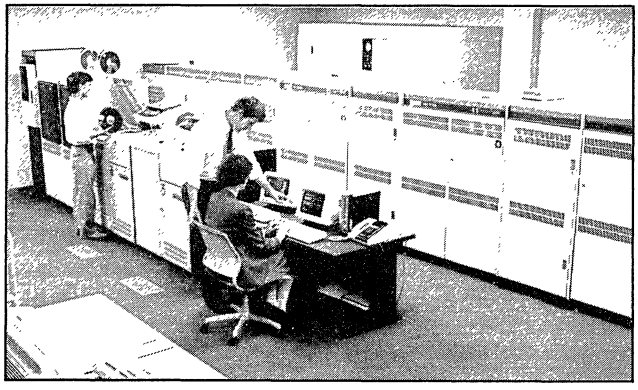
Silicon Systems continually invests in quality and capacity improvements to ensure that the company's wafer fabrication, test, and assembly capabilities meet the latest manufacturing requirements.



Two manufacturing facilities offer specialized capabilities depending on fabrication needs. Both facilities offer high resolution stepper photolithography technology, positive resist, dry plasma etch systems, high current implantation and automatic sputtering.

Fab 1 in Tustin employs bipolar processes including the high-speed BN process. Four-inch wafers are produced, targeted primarily toward the storage products marketplace. Fab 2 in Santa Cruz runs both bipolar and CMOS processes on both four- and six-inch wafers targeted primarily toward the communications and automotive products sector. The newest of the two manufacturing facilities, Fab 2, offers 5x stepper technology, robotics, and a migration towards sub-micron capability.

COMPUTER-AIDED MANUFACTURING WITH PROMIS™ FOR RAPID DELIVERY OF RELIABLE ICs



Committed to Computer-Aided Manufacturing (CAM), Silicon Systems has invested in extensive computer resources. To handle the vast amounts of data required for manufacturing, monitoring, and statistical process control, Silicon Systems uses the Process and Management Information System (PROMIS™). The PROMIS system:

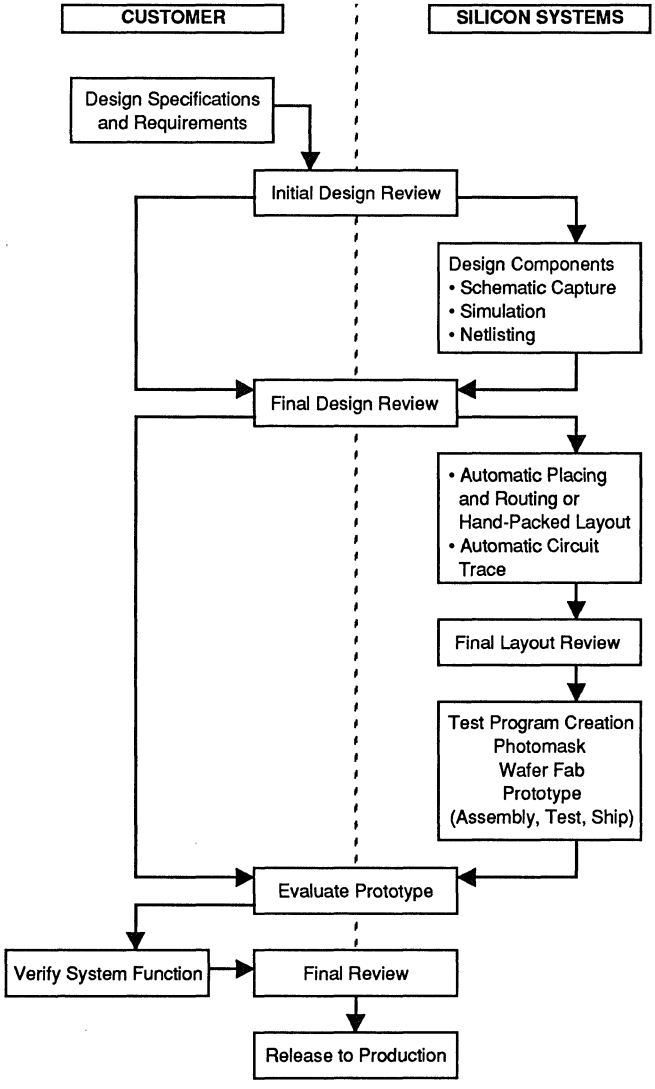
- manages inventory information,
- tracks wafers in process,
- monitors the clean room environment
- performs statistical process control.

PROMIS™ provides computer-controlled (i.e., paperless) facilities, which reduces sources of contamination in the wafer fab clean rooms. Silicon Systems' wafer fab is a class "50" environment with class "10" work surfaces. Cleanliness is maintained through the service chase approach, which channels a minimum of 5 air exchanges per minute. PROMIS allows Silicon Systems to deliver reliable ICs rapidly, thus allowing customers to introduce products to the marketplace on schedule and within budget.

SILICON SYSTEMS WORKS WITH CUSTOMERS TO CREATE THE BEST IC SOLUTION

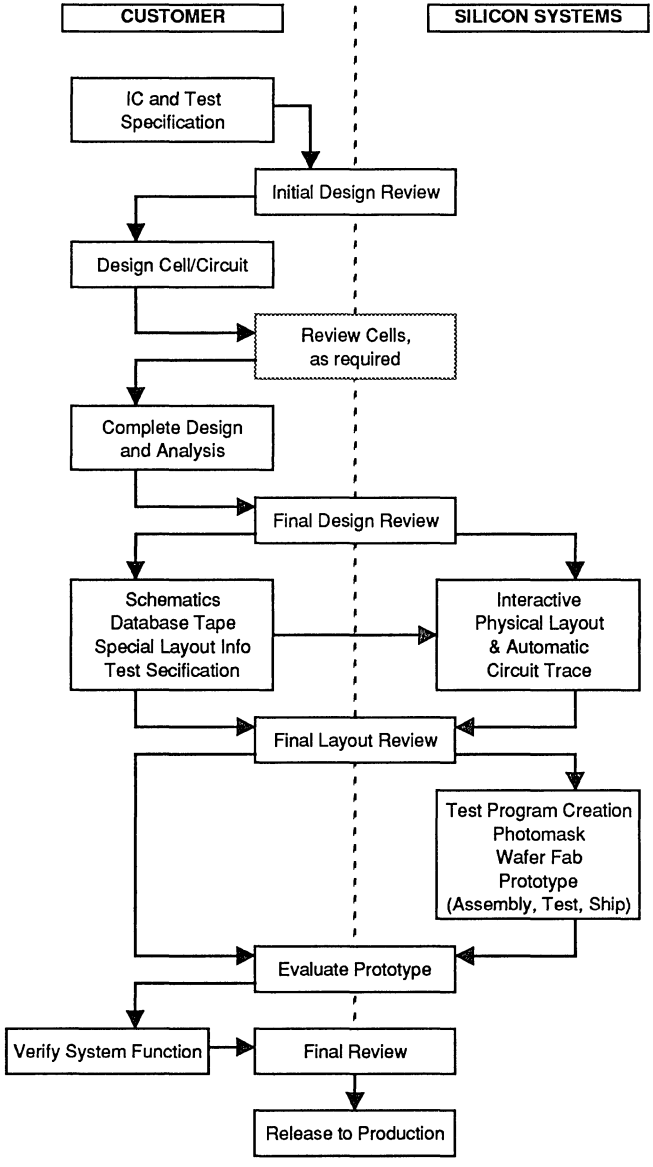
Silicon Systems has five IC design centers located in Tustin, Grass Valley, and Santa Clara, California as well as Tokyo and Singapore. Any of these design centers can accept a functional specification and complete the entire design task using either a full-custom or a cell-based approach.

CUSTOMER INTERFACE FOR FULL-CUSTOM AND CELL-BASED DESIGNS



Or, a customer can complete most of the design, using array technology, and take advantage of Silicon Systems' expertise for physical layout.

CUSTOMER INTERFACE FOR ARRAY-BASED DESIGNS



Notes:

Section

QUALITY ASSURANCE AND RELIABILITY

7

SECTION 1

1.1 INTRODUCTION

Silicon Systems is committed to the goal of customer satisfaction through the on-time delivery of defect free products that meet the customer's expectations and requirements. This statement serves as the corporate quality policy and reflects key elements that are instrumental in attaining true customer satisfaction. This section outlines Silicon Systems' ongoing activities for the control and continual improvement of quality in every aspect of our organization.

Silicon Systems is diligently working to maintain and improve its position as a world-class provider of mixed-signal integrated circuits (MSICs™). Our Corporate Quality Mission describes that commitment: "Achieve Total Customer Satisfaction Through Quality Excellence and Exceed the Goal of 1 ppm by Continuous Improvement."

We realize and practice the concept that quality must be designed and built into our products. In addition, Silicon Systems utilizes rigid inspections and data analysis to evaluate the acceptability and variation existing in incoming materials and performs stringent outgoing quality verification. The manufacturing process flow is encompassed by an effective system of test/inspection checks and in-line monitors which focus on the control and reduction of process variation. These gates and monitors ensure precise adherence to prescribed standards and procedures.

Silicon Systems also incorporates the use of statistical process control techniques into company operations. The control and reduction of the process variation by the use of statistical problem solving techniques, analytical controls and other quantitative methods ensures that Silicon Systems' products maintain the highest levels of quality and reliability. Our Reliability and Quality Assurance organization is committed to working closely with the customer to provide assistance and a continually improving level of product quality.

1.2 RELIABILITY AND QUALITY ASSURANCE

It is the objective of the Reliability and Quality Assurance organization to ensure that proactive quality systems are in place to ensure that Silicon Systems' products will meet or exceed customer requirements and expectations. In addition, the Reliability and Quality Assurance organization works to facilitate the timely implementation of solutions and monitors the effectiveness of corrective actions. These organizational strategies support the continuing enhancement of quality consciousness throughout Silicon Systems, a necessary element in supporting our objective of world-class quality.

To facilitate the close coordination required of the Reliability and Quality function, a combined Reliability and Quality Assurance organization has been established. The R&QA organization structure is pictured in Figure 1. For maximum effectiveness, this organization is headed by a Senior Vice President reporting directly to the President/CEO.

SECTION 2: QUALITY ASSURANCE

2.1 QUALITY OBJECTIVES

While all Silicon Systems employees have direct responsibility for quality in their functions, Quality Assurance has the ultimate responsibility for the reliable performance of our products. This is accomplished through the administration of formal systems which assure Silicon Systems' management, as well as our customers, that products will meet the requirements of customer purchase orders and all other specifications related to design, raw material and thorough completion of the finished product.

Quality Assurance supports and directs the formal qualification of suppliers, material, processes, and products, and the administration of quality systems and production monitors to assure that our products meet Silicon Systems quality standards. Quality Assurance also provides the liaison between

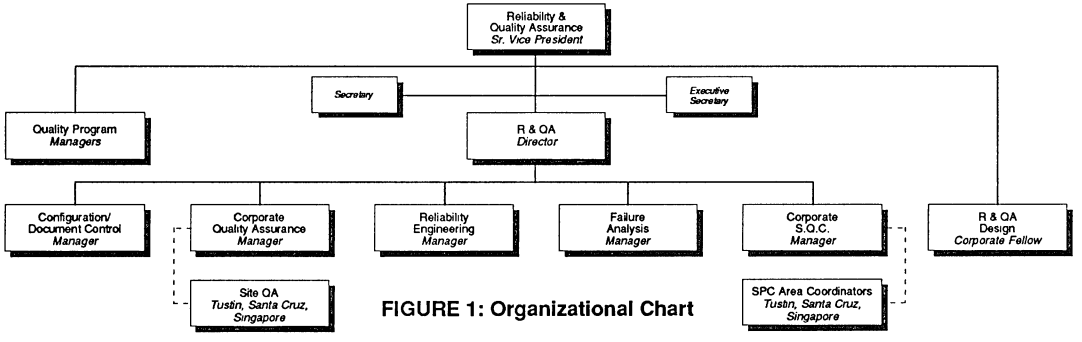


FIGURE 1: Organizational Chart

Silicon Systems and the customer for all product quality related concerns.

It is the practice of Silicon Systems to have the corporate quality and reliability objectives encompass all of its activities. This starts with a strong commitment of support from the corporate level and continues with exceptional customer support long after the product has been shipped.

Silicon Systems emphasizes the belief that quality must be built into all of its products by ensuring that all employees are educated in the quality philosophy of the company. Some of the features built into Silicon Systems Quality Culture include:

1. Structured training programs directed at Wafer Fabrication, Test, and Process Control personnel.
2. Stringent in-process inspection, gates, and monitors.
3. Rigorous evaluation of designs, materials, and processing procedures.
4. Stringent electrical testing (100% and QA AQL/Sample testing).
5. Ongoing reliability monitors and process verifications.
6. Real-time use of statistical process control methodology.
7. Corporate level audits of manufacturing, subcontractors, and suppliers.
8. Timely corrective action system.
9. Control of non-conforming material.

These focused quality methods result in products which deliver superior performance and reliability in the field.

2.2.1 INCOMING INSPECTIONS

Incoming inspection plays a key role in Silicon Systems' quality efforts. Small variations in incoming material can traverse the entire production cycle before being detected much later in the process. By paying strict attention to the monitoring of materials at the earliest possible stage, variation can be reduced, resulting in a stable uniform process.

2.2.2 IN-PROCESS INSPECTIONS

Silicon Systems has established key inspection monitors in such strategic areas as Wafer Fabrication, Wafer Probe, Assembly, and Final Test. These quality monitoring tests are performed in addition to the intermediate and final inspections found in the manufacturing process.

Quality control monitors have been integrated throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediary manufacturing steps. This data is used to document quality trends or long term improvements in the quality of specific operations. A generic description of the product flow and QC inspection points is shown in Figure 2.

2.3 DESIGN FOR QUALITY

Since the foundation of a reliable product is in the design process, the Reliability and Quality Assurance organization utilizes comprehensive reviews of design stages prior to the product's transition to production status. These review stages assure a predictable and effective development cycle. Other important design-related functions include ensuring that process specification revisions are translated into updated design parameters and the translation of manufacturing process capability into design guidelines. This is accomplished through the identification and monitoring of critical process and device parameters. These elements, included in Silicon Systems design for quality effort, support the development of robust design rules which are as insensitive as possible to manufacturing variation. The result is a product that delivers predictable and reliable long term performance.

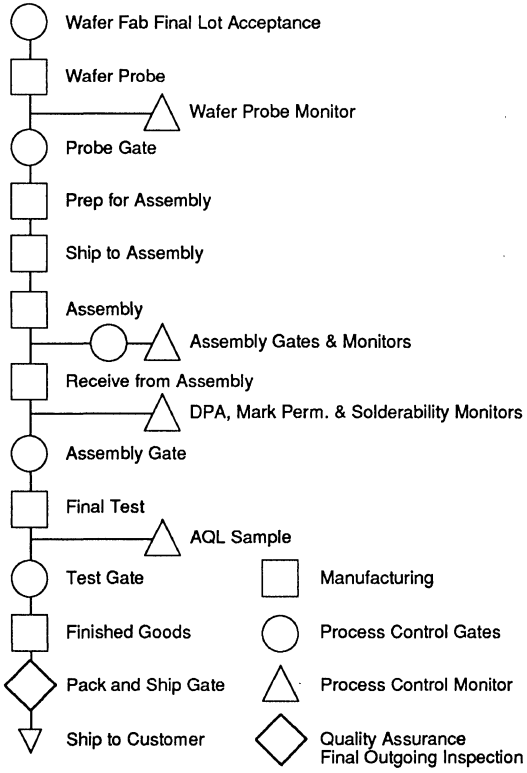


FIGURE 2
Process Control Gates and Monitors

2.4 PPM REDUCTION PROGRAM

The primary purpose of a PPM reduction program is to provide a formalized feedback system in which data from nonconforming products can be used to improve product consistency and reliability. The action portion of this program is accomplished in three stages:

1. Identification of defects by failure mode.
2. Identification of defect causes and initiation of corrective action.
3. Measurement of results and setting of improved goals.

The data summarized from the established PPM program is compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of defective parts per million (PPM). Founded on a statistically valid database of PPM data and an established five-year strategic plan identifying PPM improvement goals, Silicon Systems has progressively achieved excellent quality standards and will continue to improve on PPM standards as set by the industry.

2.5. COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) is used throughout Silicon Systems for the identification, control, collection and dissemination of timely data for logistics control. Silicon Systems also uses this type of computerized system for statistical process control and manufacturing monitoring. PROMIS, the Process Management and Information System, displays approved/controlled recipes, processes, and procedures; tracks work-in-process; reports accurate inventory information; allows continuous recording of facilities data; contains statistical analysis capabilities; and much more. PROMIS allows for a paperless facility, which assists in minimizing contamination of clean room areas.

The PROMIS system has been configured to meet the specific requirements of Silicon Systems.

SECTION 3: RELIABILITY

3.1 RELIABILITY PROGRAM

Silicon Systems has defined various programs that will characterize product reliability levels on a continuous basis. These programs can be categorically described by:

1. Qualifications
2. Production Monitors
3. Evaluations
4. Failure Analysis
5. Data collection and presentation for improvement projects

3.2 QUALIFICATIONS

The application of this program ensures that all new product designs, processes, and packaging configurations meet the absolute maximum ratings of design and the worst case criteria for end use. A large database generated by means of accelerated stress testing results in a high degree of confidence in determining final use performance.

3.3 PRODUCTION MONITORS

This program has been established to randomly select a statistically significant sample of production products for subjection to maximum stress test levels in order to evaluate the useful life of the product in a field use environment.

Table 1 lists reliability methods that are in use at Silicon Systems. This analysis of production monitor at Silicon Systems provides valuable information on possible design/process changes which assure continued improved reliability.

3.4 EVALUATIONS

The evaluation program at Silicon Systems is an ongoing effort that will continue defining standards which address the reliability assessment of the circuit design, process parameters, and package of a new product. This program continuously analyzes updated performance characteristics of product as they undergo improvement projects at Silicon Systems.

3.5 FAILURE ANALYSIS

The failure analysis function is an integral part of the Reliability department at Silicon Systems. Silicon Systems has assembled a high technical and sophisticated failure analysis laboratory and staff. This laboratory provides visual analysis, electrical reject mode analysis, and both destructive and nondestructive data to aid the engineers in developing corrective action for improvement. These test analyses may include metallurgic, optical, chemical, electrical, and SEM with X-ray dispersive analysis as needed.

These conclusive in-house testing and analysis techniques allow Silicon Systems to monitor all aspects of product manufacturing to ensure that the product of highest quality is shipped to our customers.

3.6 DATA COLLECTION AND PRESENTATION FOR IMPROVEMENT PROJECTS

Data collected from each element of the Reliability program is summarized for scope and impact and distributed among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review the performance of our product.

TEST	CONDITIONS	PURPOSE OF EVALUATION
Biased temperature/humidity	85°C/85° %RH	Resistance to high humidity with bias
High temperature operating life (HTOL)	Mil 883C, Method 1005	Resistance to electrical and thermal stress
Highly accelerated stress test (HAST)	SSi Method	Evaluates package integrity
Steam pressure	121°C/15PSI	Resistance to high humidity
Temperature cycling	Mil 883C, Method 1010	Resistance to thermal excursion (air)
Thermal shock	Mil 883C, Method 1011	Resistance to thermal excursion (liquid)
Salt atmosphere	Mil 883C, Method 1009	Resistance to corrosive environment
Constant acceleration	Mil 883C, Method 2001	Resistance to constant acceleration
Mechanical shock	Mil 883C, Method 2002	Resistance to mechanical shocks
Solderability	Mil 883C, Method 2003	Evaluates solderability of leads
Lead integrity	Mil 883C, Method 2004	Evaluates lead integrity before board assembly
Vibration, variable frequency	Mil 883C, Method 2007	Resistance to vibration
Thermal resistance	SSi Method	Evaluates thermal dissipation
Electrostatic damage	Method 3015	Evaluates ESD susceptability
Latch-up	SSi Method	Evaluates latch-up susceptibility
Seal fine and gross leak	Mil Std 883C, Method 1014	Evaluates hermeticity of sealed packages

TABLE 1: Reliability Stress Tests

3.7 RELIABILITY METHODS

The Reliability Program utilizes a number of stress tests that are presently being used to define performance levels of our products. Many of these stress tests are per MIL-STD-883C as shown in Table 3.

3.8 RELIABILITY PREDICTION METHODOLOGY

At Silicon Systems, the Arrhenius model is used to relate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states FR = A exp(-Ea/KT)

Where:

FR = Failure rate

A = Constant

Ea= Activation Energy (eV)

K = Boltzmann's constant 8.62 x 10^{-5} eV/ degree K

T = Absolute temperature (degree K)

SECTION 4: ELECTROSTATIC DISCHARGE PROGRAM

4.1 ESD PREVENTION

Silicon Systems recognizes that procedures for the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity are vital. ESD safe procedures are incorporated throughout all operations which come in contact with these devices. Continuous improvement in the ESD protection levels is being accomplished through the incorporation of increasingly robust protection devices during the circuit design process.

Silicon Systems' quality activity incorporates several protection measures for the control of ESD. Some of the preventive measures include handling of parts at static safe-guarded workstations, the wearing of wrist straps during all handling operation, the use of conductive lab coats in all test areas and areas which handle parts and the packaging of components in conductive or anti-static containers.

Section

PACKAGING/ ORDERING INFORMATION

Silicon Systems
Packaging Index
Ordering Information

*SON is a 150 mil width package.

**SOL is a 300 mil width package.

***SOW is a 400 mil width package.

****SOM is a 300 mil width package, fine pitch.

Package Type	8	10	14	16	18	20	22	24	28	32	34	36	40	44	52	68	100
Plastic DIP																	
300 mil	X		X	X	X	X		S									
400 mil							X										
600 mil								X	X	X			X				
Cerdip																	
300 mil	X		X	X	X	X											
400 mil							X										
600 mil								X	X				X				
Side Braze																	
300 mil	X		X	X	X	X		S									
400 mil							X										
600 mil								X	X				X				
Small Outline																	
150 mil	X		X	X													
300 mil				X		X		X	X		X	X		X			
400 mil										X							
Flatpack		X	X					X	X	X							
Chip Carrier				X		X			X								
Plastic Quad									X	X				X	X	X	
Ceramic Quad									X					X		X	
QFP															X		X

Silicon Systems
Communication Products
Package Types

DEVICE TYPE	PACKAGE TYPE			
	P S* Plastic	H PLCC	N L W Small Outline	QFP Quad Fine Pitch
SSI 73D2180				
73K222U	40	44		
73D620	40	44		
SSI 73D2291/2292				
73M235		44		
73D640		44		
73D631		44		
SSI 73D2404				
73M214	28	28		
73D215	28	44		
73D216	40	44		
SSI 73D2407				
73M214	28	28		
73D215	28	44		
73D218	40	44		
73D221	32	32		
SSI 73D2417				
73M214	28	28		
73M215	28	44		
73D219	40	44		
73D225	32	32		
SSI 73D2240				
73K224L	28	32		
73D600	40	44		
SSI 73D2420/2421				
73D680				100
73D681		44		
73D682		32		
SSI 73K212/212L	22, 28	28		
SSI 73K221/221L	22, 28		28	

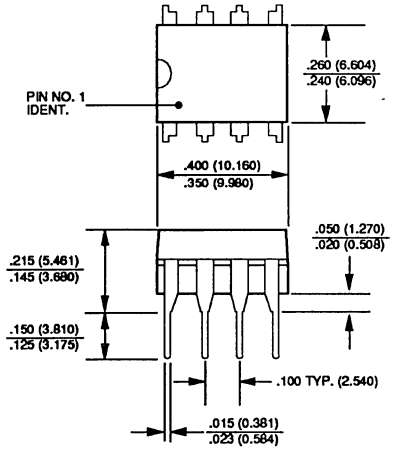
*Narrow

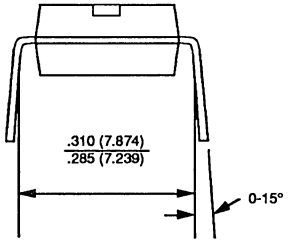
DEVICE TYPE	PACKAGE TYPE			
	P S* Plastic	H PLCC	N L W Small Outline	QFP Quad Fine Pitch
SSI 73K222/222L	22, 28	28		
SSI 73K222U	40	44		
SSI 73K224L	28	32, 44		
SSI 73K302L	22, 28	28		
SSI 73K322L	22, 28	28		
SSI 73K324L	28			
SSI 73M214	28	28		
SSI 73M223	16			
SSI 73M235	48	44		
SSI 73M376		28		
SSI 73M450/450F	40	44		
SSI 73M450L/450LF	40	44		
SSI 73M550	40	44		
SSI 73M650/1650	28, 40	28, 44		
SSI 73M1450/2450	28	28		
SSI 73M1550/2550	28	28		
SSI 75T201	22			
SSI 75T202/203	18			
SSI 75T204	14		16L	
SSI 75T2089/2090	22			
SSI 75T2091	28	28		
SSI 75T957	22		24L	
SSI 75T980	8		16L	
SSI 75T981/982	22			
SSI 78A093A/093B	40	44		
SSI 78A207	20			
SSI 78P233	24, 24S		24L	
SSI 78P234	20		20L	
SSI 78P236	28			
SSI 78P2361	28			
SSI 78P2362	28			

*Narrow

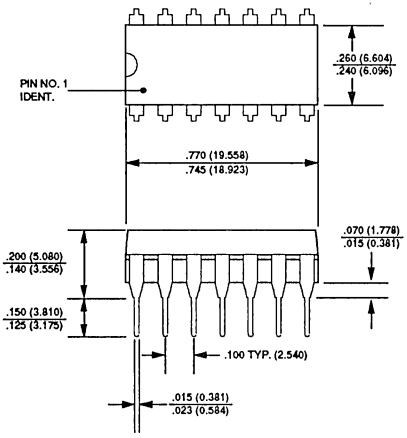
SSI NNA NNNN A AA - N A A
Optional
PRODUCT CATEGORY
32B HDD Interface
32C HDD Controller
32D HDD Data Recovery
32H HDD Head Positioning
32M HDD Motor Speed Controller
32P HDD Pulse Detection
32R HDD Read/Write Amp
34B FDD Interface
34D FDD Data Recovery
34P FDD Pulse Detection
34R FDD Read/Write Amp
35P Tape Drive Pulse Detection
73D Modem Device Set
73K K-Series Modem
73M Modem/Modem Support
75T Tone Signaling
78A Analog Telecom
78P Digital Telecom
DEVICE TYPE 3 or 4 Digits
RELEASE LEVEL (Revision) A through E
NUMBER OF CHANNELS
MODIFIERS
J Burn-In (168 Hours)
K Burn-In (48 Hours)
LJ Low Noise Burn-In (168 Hours)
L Low Power
LN Low Noise
LQ Low Noise, Resistor, Mirror Image
LR Low Noise, Resistor
M Mirror Image
S Serial Version
SL Low Power Serial
R Damping Resistor
RM Resistor, Mirror Image
U On-Chip UART
Cannot use A-E in left position
PACKAGE TYPE
C Side-Brazed Ceramic
D Ceramic Dip
F Flat Pack
G QFP (25 mil. pitch)
H PLCC
P Plastic Dip
T Metal Can
S Plastic, Skinny Dip
N Small Outline, Narrow (150 mil.)
L Small Outline, Large (300 mil.)
W Small Outline, Wide (400 mil.)
M Small Outline, Large (31.6 mil. pitch)
TEMPERATURE RANGE
C Commercial (0 °C to +70 °C)
I Industrial (-40 °C to +85 °C)
M Military (-55 °C to +125 °C)

Package Information

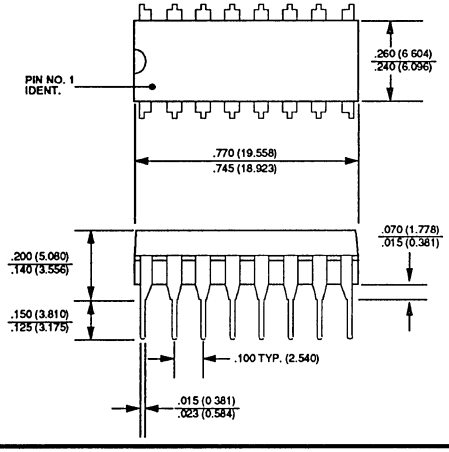


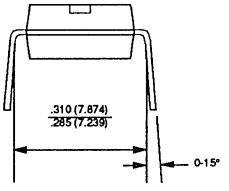


8-Pin Plastic

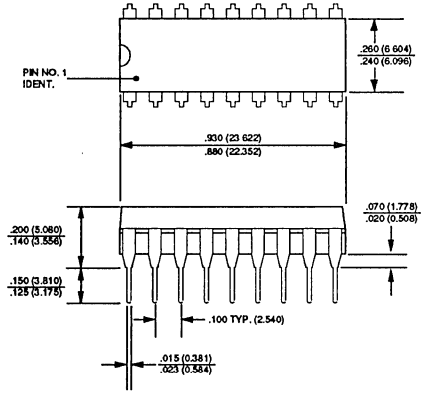


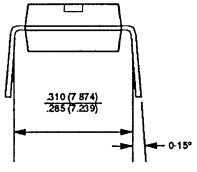
14-Pin Plastic





16-Pin Plastic

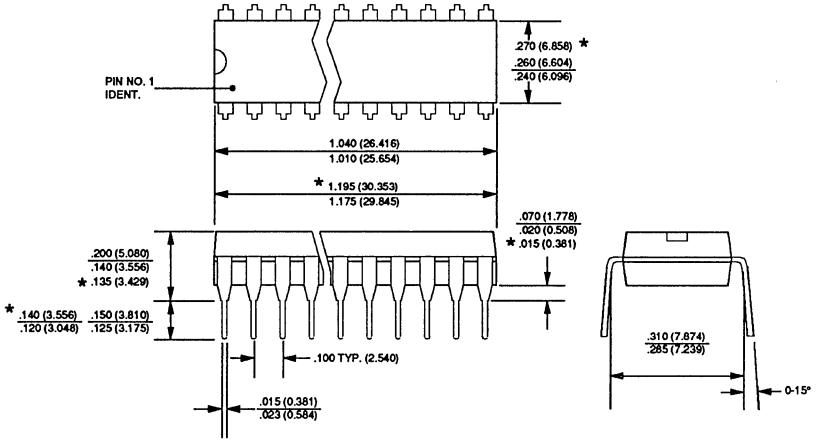




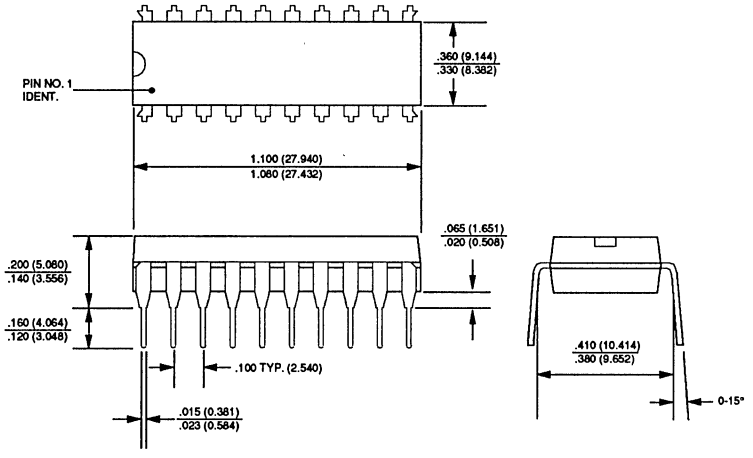
18-Pin Plastic

8

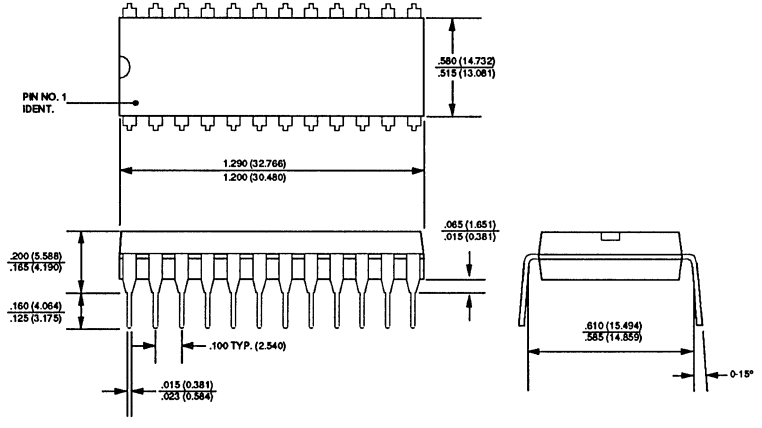
Package Information
(Plastic DIP)



20 Pin Plastic
***24S Pin Plastic**

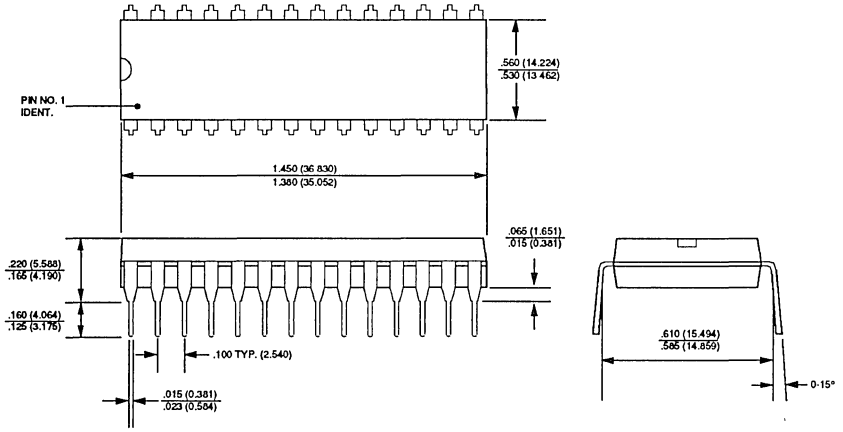


22-Pin Plastic

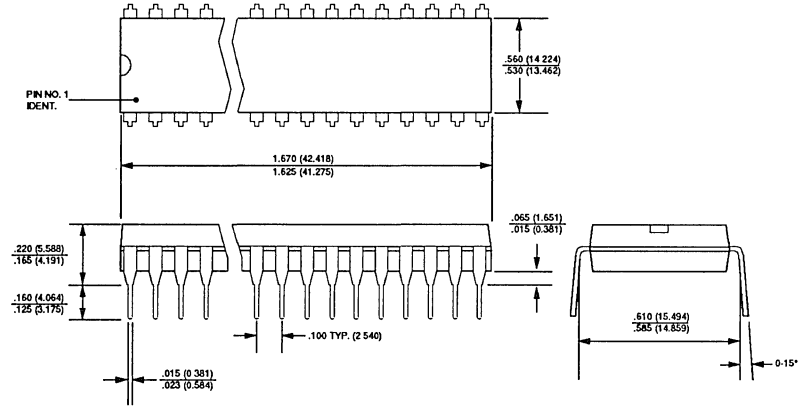


24-Pin Plastic

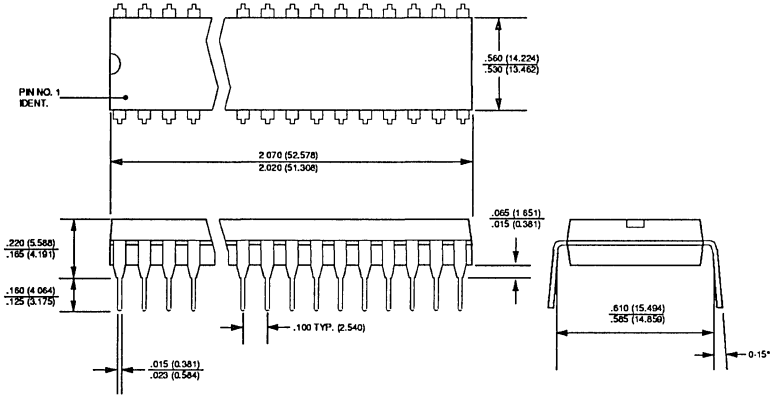
Package Information



28-Pin Plastic



32-Pin Plastic



40-Pin Plastic

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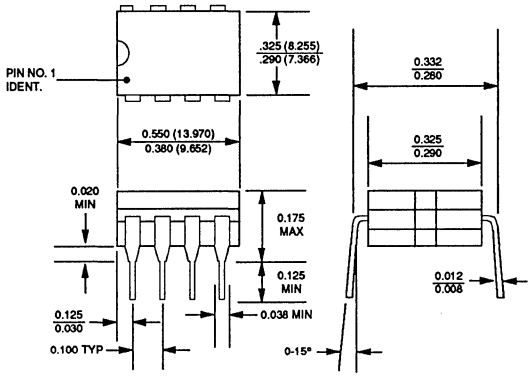
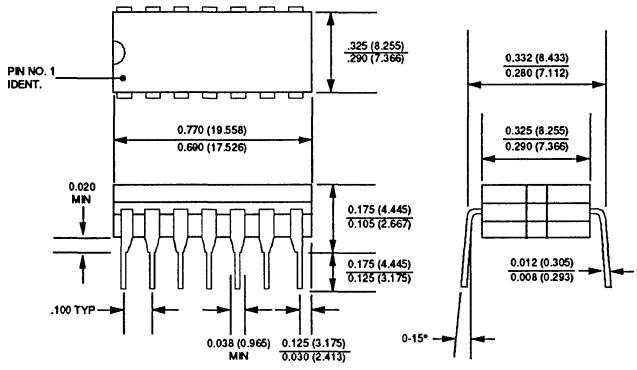
Package Information (Cerdip)



8-Pin Cerdip



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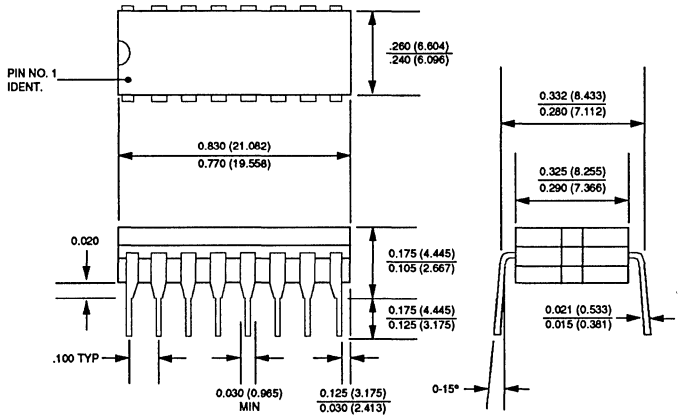
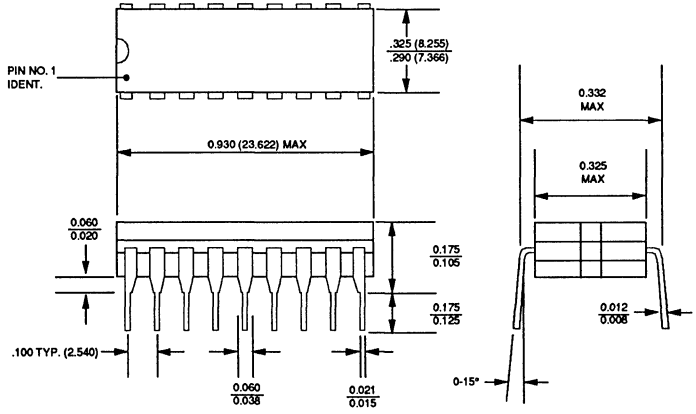
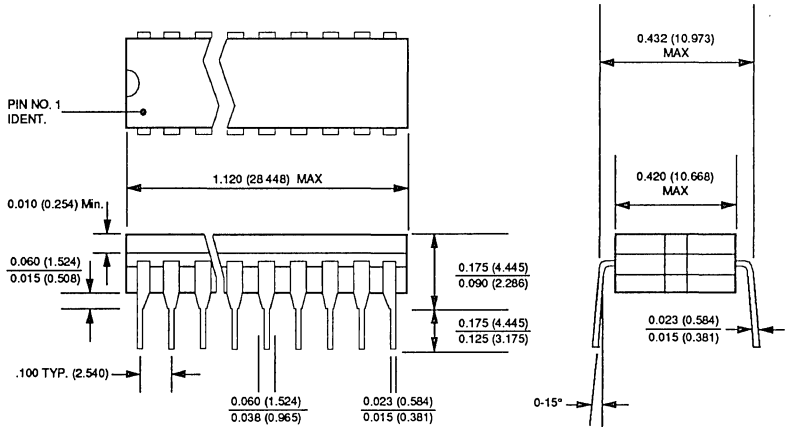


16-Pin Cerdip

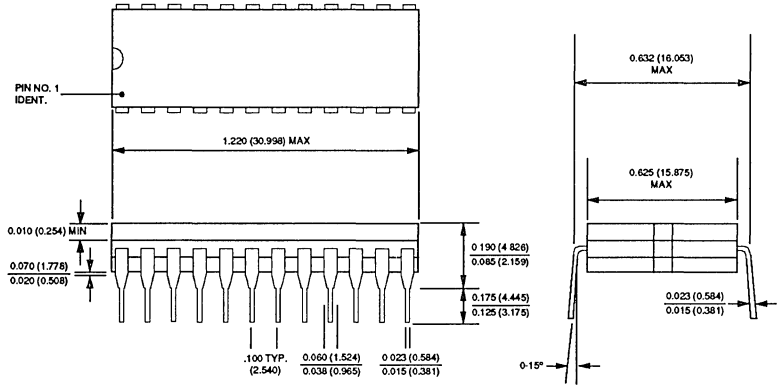


18-Pin Cerdip

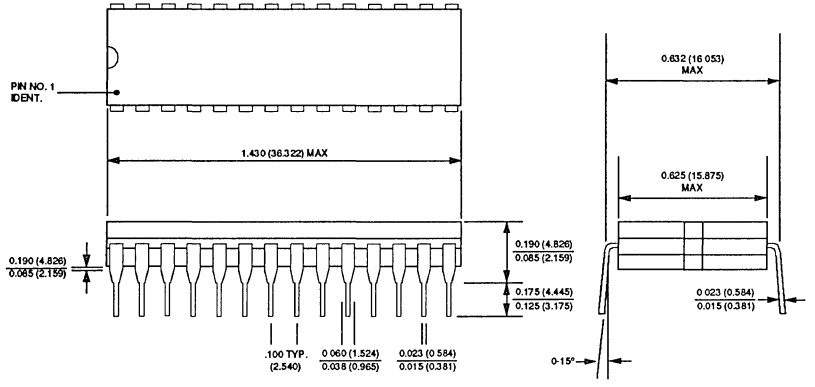
Package Information



22-Pin Cerdip



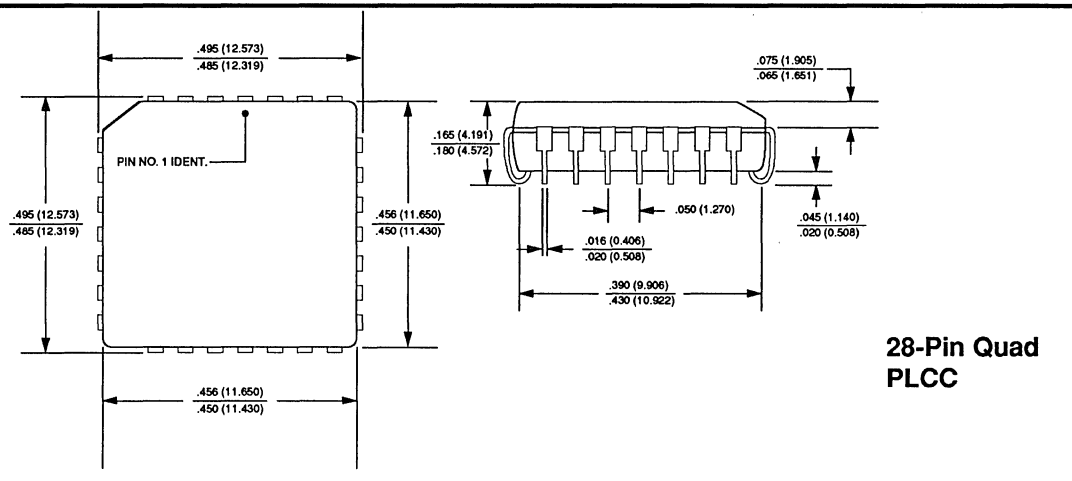
24-Pin Cerdip



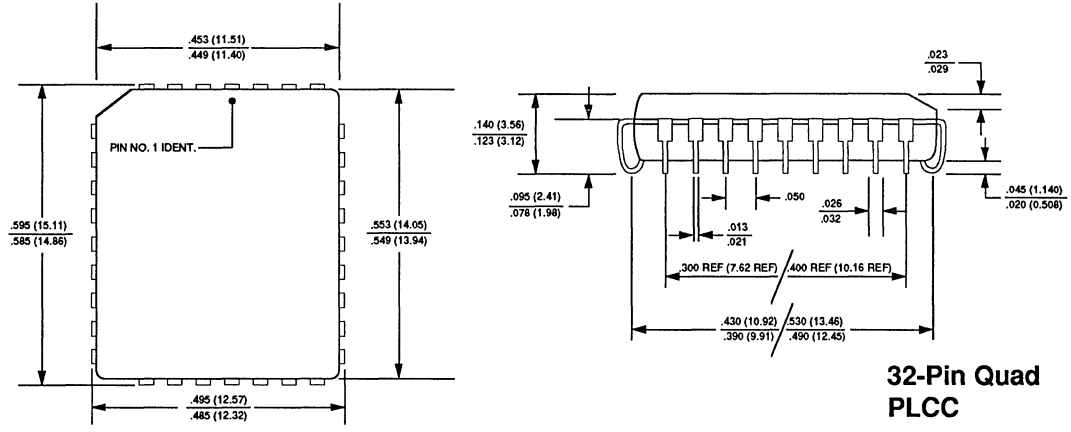
28-Pin Cerdip

8

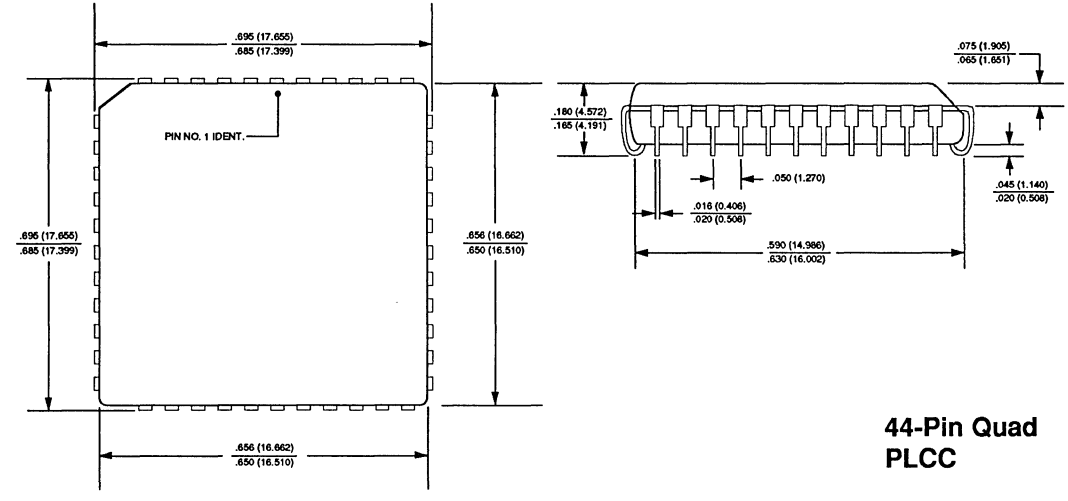
Package Information
PLCC (Quad)



28-Pin Quad PLCC

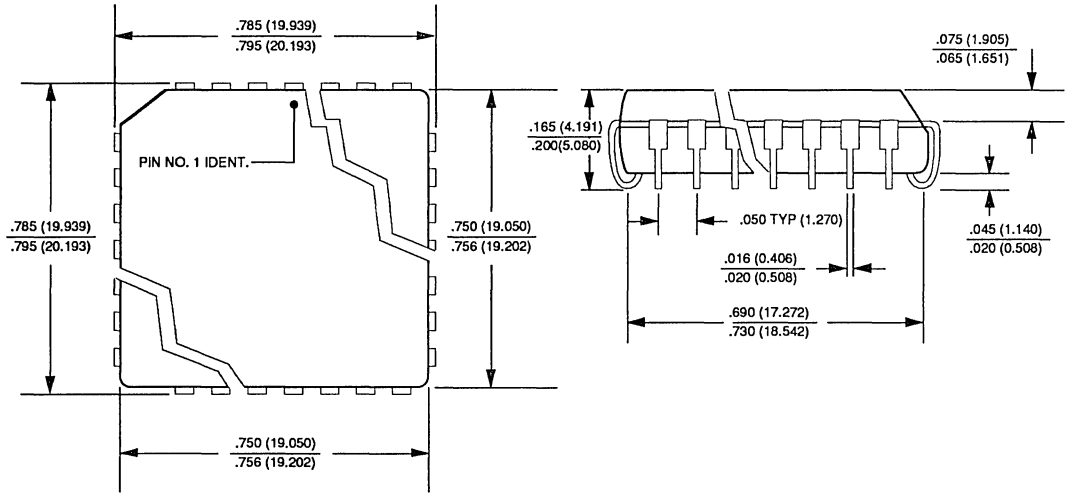


32-Pin Quad PLCC



44-Pin Quad PLCC

Package Information



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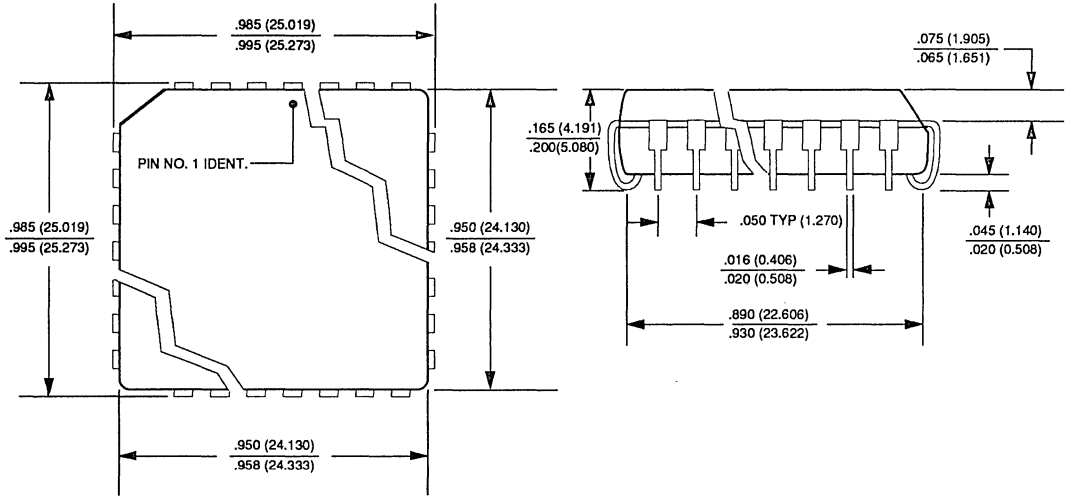
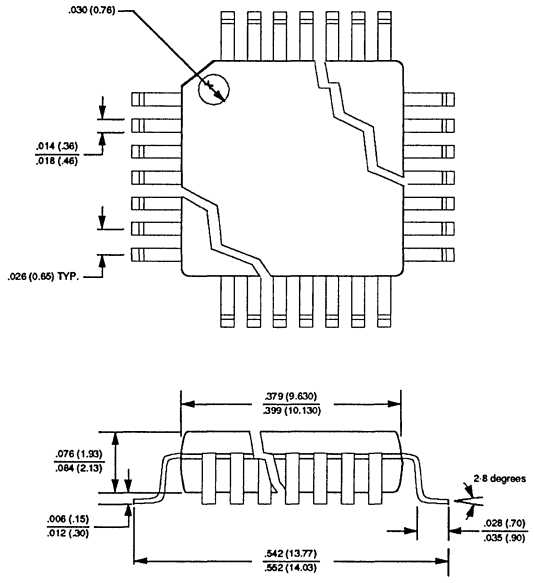


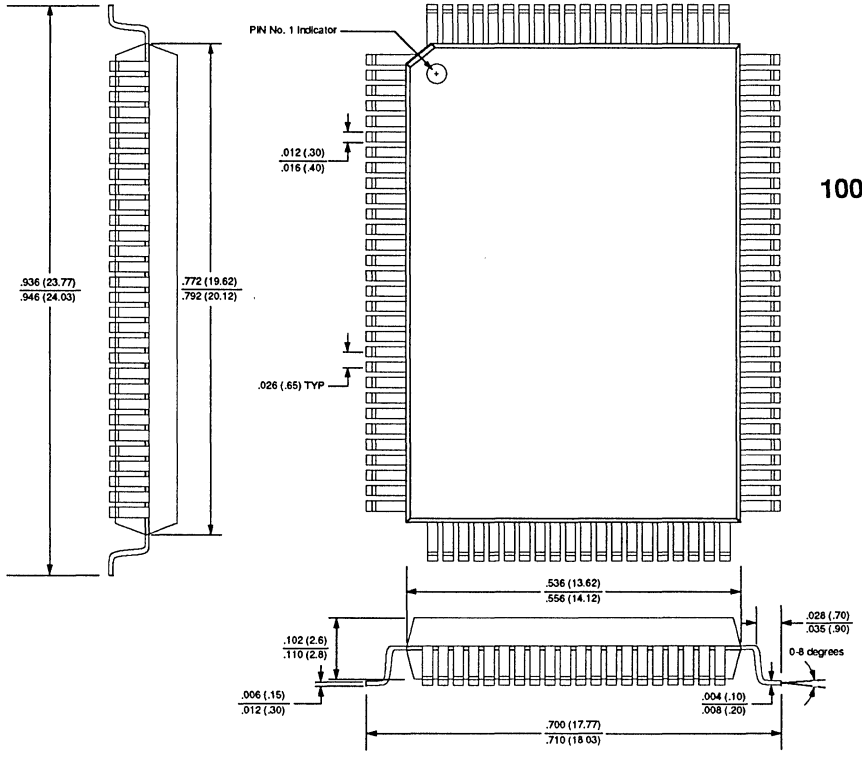
68-Pin Quad PLCC

8

Package Information
Quad (Fine Pitch)

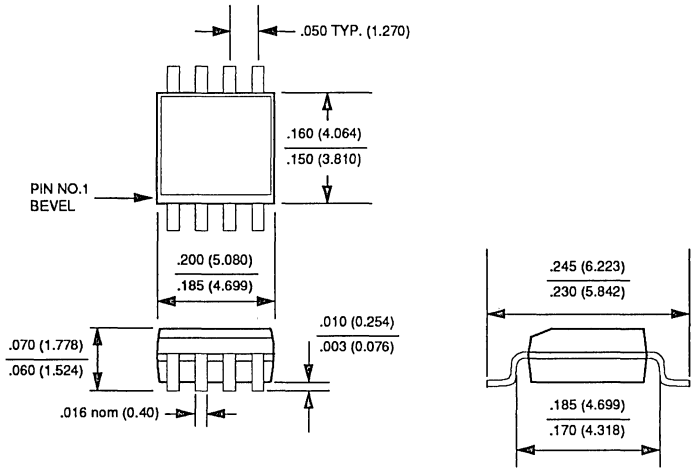


52-Lead Quad Fine Pitch

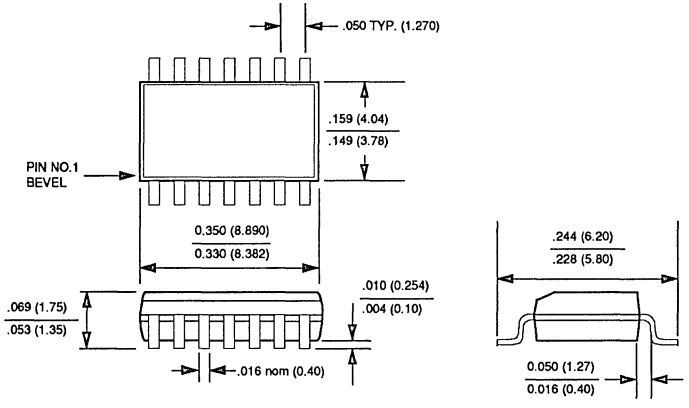


100-Lead Quad Fine Pitch

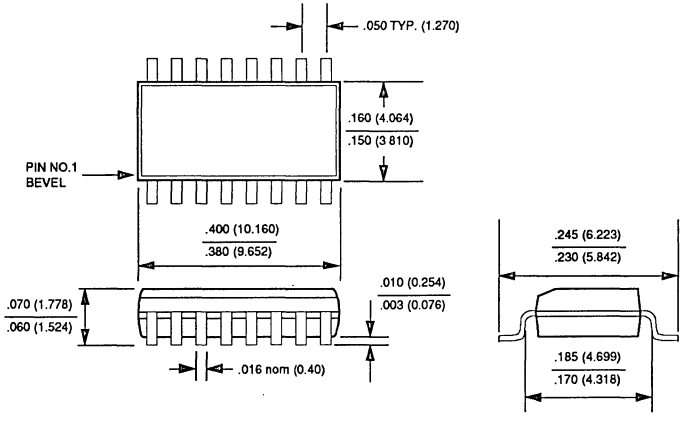
Package Information
(SON)



8-Pin SON



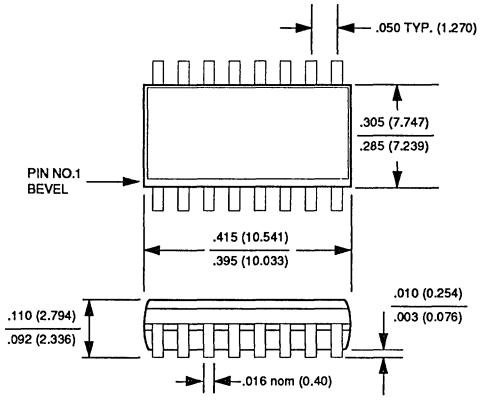
14-Pin SON



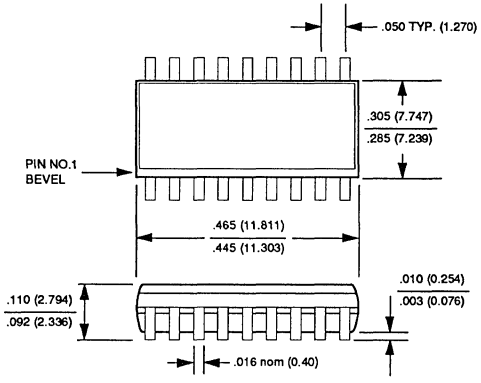
16-Pin SON

8

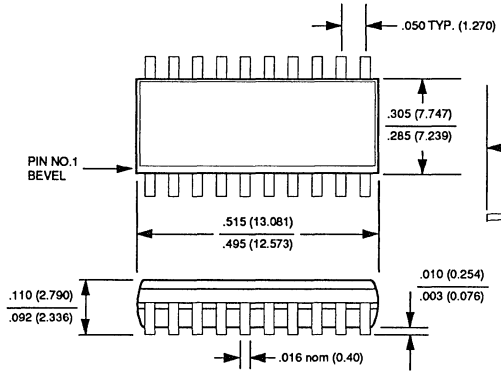
Package Information
(SOL)



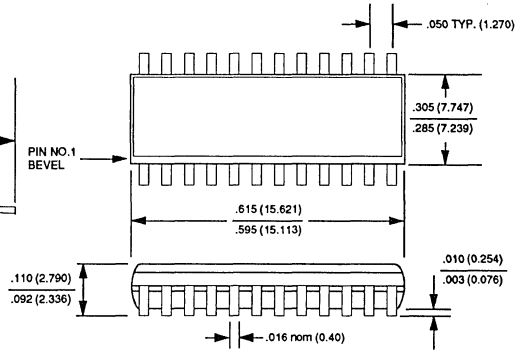
16-Pin SOL



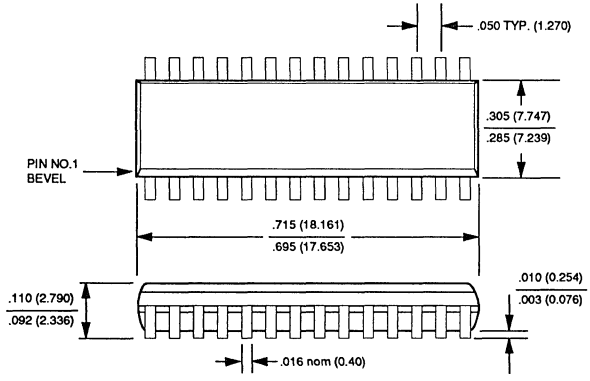
18-Pin SOL



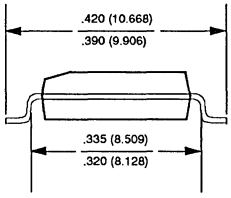
20-Pin SOL



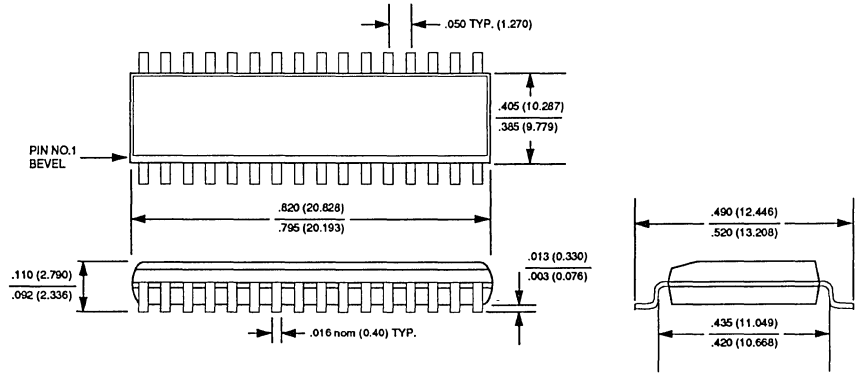
24-Pin SOL



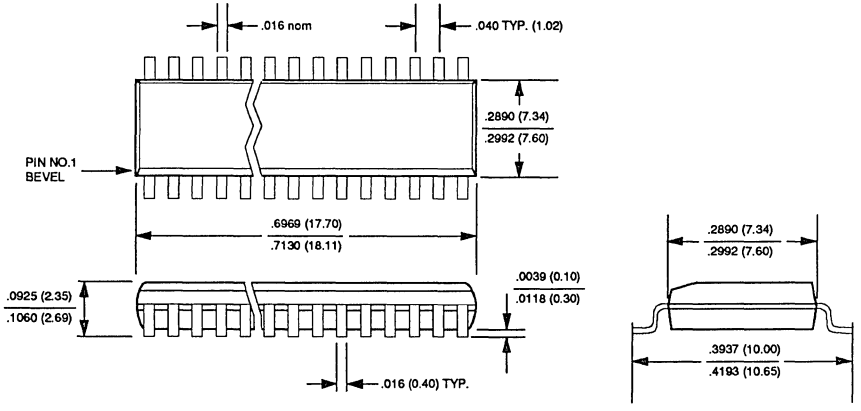
28-Pin SOL



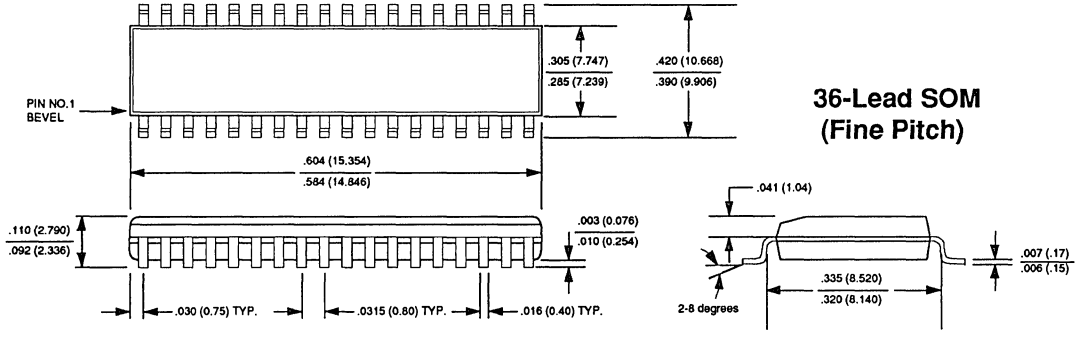
Package Information (SOL/SOM/SOW)



32-Pin SOW



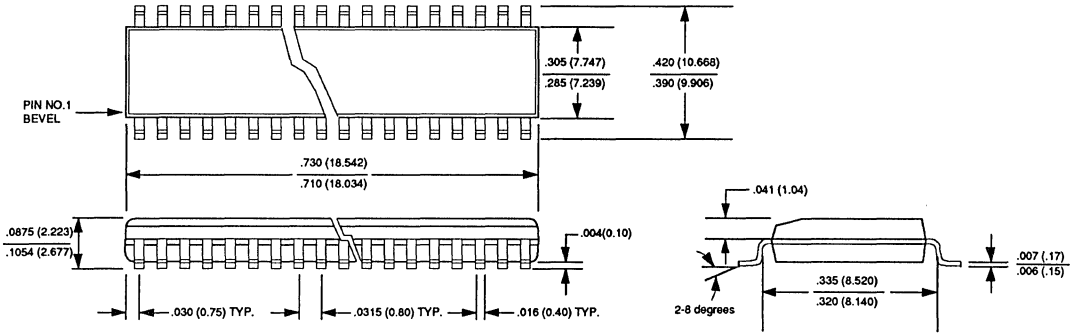
34-Pin SOL



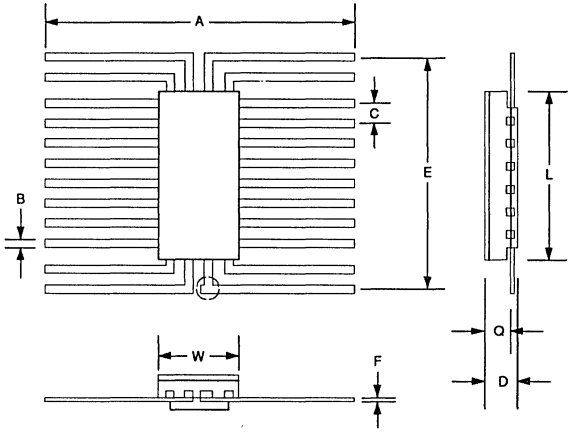
36-Lead SOM (Fine Pitch)

8

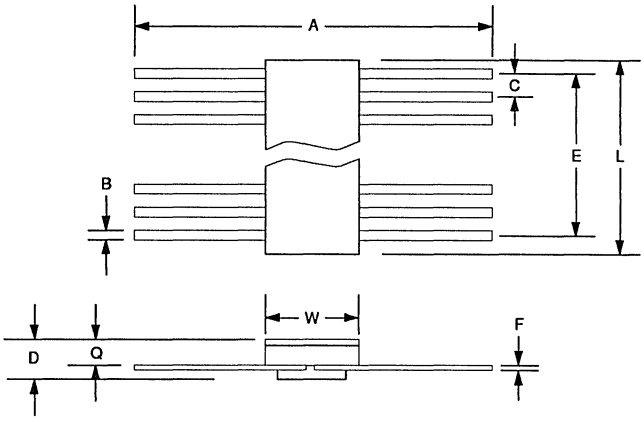
44-Lead SOM
(Fine Pitch)



Package Information
(Flatpack)



Flatpack
24-Leads



Flatpack
10, 28, 32-Leads

Pkg. Type	Lead Cnt.	A	B	C	D	E	F	L	Q	W
F	10	.900	.015 / .019	.045 / .055	.090 max	.200 typ	.004 / .007	.250 / .260	.074 typ	.250 / .260
F	24	.900	.015 / .019	.050 typ	.087 max	.567 typ	.004 / .007	.391 / .405	.075 typ	.264 / .276
F	28	1.150	.015 / .019	.045 / .055	.092 max	.645 / .655	.004 / .007	.712 / .728	.085 / .078	.492 / .508
F	32	1.150	.015 / .019	.045 / .055	.092 max	.745 / .755	.004 / .007	.812 / .828	.085 / .078	.492 / .508

Section

GLOSSARY

9

Glossary

A

ACK - "Acknowledge" character. A transmission control character transmitted by a station as an affirmative response to the station with which a connection has been set up. An acknowledge character may also be used as an accuracy control character.

ACOUSTIC COUPLER - A type of low-speed modem interface frequently used with portable terminals. It sends and receives data using a conventional telephone handset and does not require an electrical connection to the line.

ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION (ADPCM) - An encoding technique, standardized by the CCITT, that allows an analog voice conversation to be carried within a 32K bps digital channel. Three or four bits are used to describe each sample, which represents the difference between two adjacent samples. Sampling is done 8,000 times per second.

ALGORITHM - A prescribed set of well-defined rules for the solution of a problem in a finite number of steps, e.g., A full statement of an arithmetic procedure for evaluating sine x to a stated precision.

AMPLITUDE - Magnitude or size. In waveforms or signals occurring in a data transmission, a complete definition of the waveform can be made if the voltage level is known at all times. In this case, the voltage level is called the amplitude.

AMPLITUDE MODULATION - Method of modifying the amplitude of a sine wave signal in order to encode information.

ANALOG LOOPBACK - A technique used for testing transmission equipment that isolates faults to the analog signal receiving or transmitting circuitry. Basically, where a device, such as a modem, echoes back a received (test) signal that is then compared with the original signal.

ANALOG SIGNAL - Signal in the form of a continuously varying physical quantity such as voltage, which reflects variations in some quantity.

ANSI - American National Standards Institute. A highly active group affiliated with the International Standards Organization (ISO) that prepares and establishes standards for transmission codes (e.g., ASCII), protocols (e.g., ADCCP), media (tape and diskette), and high level languages (e.g., Fortran and Cobol), among other things.

ANSWERBACK - A reply message from a terminal that verifies that the correct terminal has been reached and that it is operational.

APPLICATION LAYER - The top of the seven-layer OSI model, generally regarded as offering an interface to, and largely defined by, the network user; in IBM's SNA, the end-user layer.

ASCII - American Standard Code for Information Interchange. A 7-bit binary code that defines 128 standard characters for use in data communications.

ASYNCHRONOUS - Occurring without a regular or predictable time relationship to a specified event, e.g., The transmission of characters one at a time as they are keyed. Contrast with synchronous.

ASYNCHRONOUS TRANSMISSION - Transmission in which each information character, or sometimes each word or small block, is individually synchronized, usually by the use of start and stop elements. Also called start-stop or character asynchronous transmission.

ATTENUATION - A decrease in the power of a current, voltage, or power of a received signal in transmission between points because of loss through lines, equipment or other transmission devices. Usually measured in decibels.

AUTO-ANSWER - Automatic answering; the capability of a terminal, modem, computer, or a similar device to respond to an incoming call on a dial-up telephone line, and to establish a data connection with a remote device without operator intervention.

AUTOBAUD - The generally used term for automatically detecting the bit rate of a start/stop (character asynchronous) communication format by measuring the length of the start bit of the first character transmitted. Some modems extend this to additionally determine the parity in use by stipulating that the first two characters from the DTE should be "AT". The word autobaud comes from a popular misuse of baud rate to mean the same as bit rate.

AUTODIAL - Automatic dialing; the capability of a terminal, modem, computer, or a similar device to place a call over the switched telephone network, and establish a connection without operator intervention.

AUTOMATIC DIALER, OR AUTODIALER - Device which allows the user to dial preprogrammed numbers simply by pushing a single button.

B

BANDPASS FILTER - A circuit designed to allow a single band of frequencies to pass; neither of the cut-off frequencies can be zero or infinite.

BANDWIDTH - 1) The range of frequencies that can pass over a given circuit. The bandwidth determines the rate at which information can be transmitted through the circuit. The greater the bandwidth, the more information that can be sent through the circuit in a given amount of time. 2) Difference, expressed in hertz (Hz), between the highest and lowest frequencies of a transmission channel.

BASEBAND - Pertaining or referring to a signal in its original form and not changed by modulation. A baseband signal can be analog or digital.

BASEBAND SIGNALING - Transmission of a digital or analog signal at its original frequencies, i.e., a signal in its original form, not changed by modulation; can be an analog or digital signal.

BAUD - A measure of data rate, often misused to denote bits per second. A baud is equal to the number of discrete conditions or signal events per second. There is disagreement over the appropriate use of this word, since at speeds above 2400 bit/s, the baud rate does not always equal the data rate in bits per second.

BELLCORE - Bell Communications Research; organization established by the AT&T divestiture, representing and funded by the BOCs and RBOCs, for the purposes of establishing telephone network standards and interfaces; includes much of former Bell Labs.

BERT - Bit Error Rate Test. A test conducted by transmitting a known, pattern of bits (commonly 63, 511, or 2047 bits in length), comparing the pattern received with the pattern transmitted, and counting the number of bits received in error. Also see bit error rate. Contrast with BLERT.

BINARY CODE - Representation of quantities expressed in the base-2 number system.

BINARY SYNCHRONOUS COMMUNICATIONS - A half-duplex, character-oriented data communications protocol originated by IBM in 1964. It includes control characters and procedures for controlling the establishment of a valid connection and the transfer of data. Also called bisync and BSC. Although still enjoying widespread usage, it is being replaced by IBM's more efficient protocol, SDLC.

BIPOLAR - 1) The predominant signaling method used for digital transmission services, such as DDS and T1, in which the signal carrying the binary value successfully alternates between positive and negative polarities. Zero and one values are represented by the signal amplitude at either polarity, while no-value "spaces" are at zero amplitude. 2) A type of integrated circuit (IC or semiconductor) that uses NPN, PNP, and junction FET's as the primary active devices, as opposed to CMOS, which uses MOS FET's. See Alternate Mark Inversion.

BIT - The smallest unit of information used in data processing. It is a contraction of the words "binary digit."

BIT ERROR RATE (BER) - In data communications testing, the ratio between the total number of bits transmitted in a given message and the number of bits in that message received in error; a measure of the quality of a data transmission.

BITS PER SECOND (BIT/S) - Basic unit of measure for serial data transmission capacity; Kbit/s, or kilobits, for thousands of bits per second; Mbit/s, or megabit/s, for millions of bits per second, etc.

BOC - Bell Operating Company. One of 22 local telephone companies spun off from AT&T as a result of divestiture. The 22 operating companies are divided into seven regions and are held by seven RBHCs (Regional Bell Holding Company).

BROADBAND - Referring or pertaining to an analog circuit that provides more bandwidth than a voice grade telephone line, i.e., a circuit that operates at a frequency of 20 kHz or greater. Broadband channels are used for high-speed voice and data communications, radio and television broadcasting, some local area data networks, and many other services. Also called wideband.

BUFFER - A storage medium or device used for holding one or more blocks of data to compensate for a difference in rate of data flow, or time of occurrence of events, when transmitting data from one device to another.

BUS - 1) Physical transmission path or channel. Typically an electrical connection, with one or more conductors, wherein all attached devices receive all transmissions at the same time. Local network topology, such as used in Ethernet and the token bus, where all network nodes listen to all transmissions, selecting certain ones based on address identification. Involves some type of contention-control mechanism for accessing the bus transmission medium. In data communications, a net-

work topology in which stations are arranged along a linear medium (e.g., a length of cable). 2) In computer architecture, a path over which information travels internally among various components of a system.

BYTE - Group of bits handled as a logical unit; usually 8.

C

CABLE - Assembly of one or more conductors within a protective sheath; constructed to allow the use of conductors separately or in groups.

CALL PROGRESS DETECTION (CPD) - A technique for monitoring the connection status during initiation of a telephone call by detecting presence and/or duty cycle of call progress signaling tones such as dial-tone or busy signals commonly used in the telephone network.

CALL PROGRESS TONES - Audible signals returned to the station user by the switching equipment to indicate the status of a call; dial tones and busy signals are common examples.

CCITT - Comite Consultatif International de Telephonie et de Telegraphie. Telegraph and Telephone Consultive Committee. An advisory committee to the International Telecommunications Union (ITU) whose recommendations covering telephony and telegraphy have international influence among telecommunications engineers, manufacturers, and administrators.

CENTRAL OFFICE (CO) - See Exchange

CHANNEL BANK - Equipment typically used in a telephone central office that performs multiplexing of lower speed, digital channels into a higher speed composite channel. The channel bank also detects and transmits signaling information for each channel, and transmits framing information so that time slots allocated to each channel can be identified by the receiver.

CHANNEL SERVICE UNIT (CSU) - A component of customer premises equipment (CPE) used to terminate a digital circuit, such as DDS or T1 at the customer site; performs certain line-conditioning functions, ensures network compliance per FCC rules and responds to loopback commands from central office; also, ensures proper ones density in transmitted bit stream and performs bipolar violation correction.

CHANNEL, VOICE GRADE - Channel suitable for transmission of speech, analog data, or facsimile, generally with a frequency range of about 300 to 3000 Hz.

CHARACTER - Letter, figure, number, punctuation, or other symbol contained in the message. In data communication, common characters are defined by 7- or 8-bit binary codes, such as ASCII.

CHIP - A commonly used term which refers to an integrated ciruit.

CIRCUIT, TWO-WIRE - A circuit formed by two conductors insulated from each other that can be used as either a one-way or two-way transmission path.

CLOCK - In logic or transmission, repetitive, precisely timed signal used to control a synchronous process.

CMOS - Complementary Metal-Oxide Semiconductor. A type of transistor, typicallly used in low-power integrated circuits.

COAXIAL CABLE - Cable consisting of an outer conductor surrounding an inner conductor, with a layer of insulating material in between. Such cable can carry a much higher bandwidth than a wire pair.

CPE - Customer Premises Equipment

CROSSPOINT - 1) Switching array element in an exchange that can be mechanical or electronic. 2) Two-state semiconductor switching device having a low transmission system impedance in one state and a very high one in the other.

CROSSTALK - Interference or an unwanted signal from one transmission circuit detected on another, usually an adjacent circuit.

CYCLIC REDUNDANCY CHECK (CRC) - A powerful error detection technique. Using a polynomial, a series of two 8-bit block check characters are generated that represent the entire block of data. The block check characters are incorporated into the transmission frame, then checked at the receiving end.

D

DATA COMMUNICATIONS EQUIPMENT (DCE) - Equipment that performs the functions required to connect data terminal equipment (DTE) to the data circuit. In a communications link, equipment that is either part of the network, an access-point to the network, a network node, or equipment at which a network circuit terminates; in the case of an RS-232C connection, the modem is usually regarded as DCE, while the user device is DTE, or data terminal equipment; in a CCITT X.25 connection, the network access and packet-switching node is viewed as the DCE.

DATA LINK - Any serial data communications transmission path, generally between two adjacent nodes or devices and without any intermediate switching nodes.

DATA SET - A synonym for modem used by AT&T and a few other vendors.

DATA SERVICE UNIT (DSU) - A device that replaces a modem on a Digital Data Service (DDS) line. The data service unit regenerates the digital signals for transmission over digital facilities.

DATA TERMINAL EQUIPMENT (DTE) - Equipment which is attached to a network to send or receive data, generally end-user devices, such as terminals and computers, that connect to DCE, which either generate or receive the data carried by the network; in RS-232C connections, designation as either DTE or DCE determines signaling role in handshaking; in a CCITT X.25 interface, the device or equipment that manages the interface at the user premises; see DCE.

dB - Decibel; unit for measuring relative strength of a signal parameter such as power, voltage, etc. The number of decibels is twenty times the logarithm (base 10) of the ratio of the power of two signals, or ratio of the power of one signal to a reference level.

dBm - Decibels relative to one milliwatt.

DDS - 1) Digital Data Service. A digital transmission service supporting speeds up to 56 Kbit/s. 2) Dataphone Digital Service. An AT&T leased line service offering digital transmission at speeds ranging from 2400 to 56 Kbit/s.

DELAY DISTORTION - The change in a signal from the transmitting end to the receiving end resulting from the tendency of some frequency components within a channel to take longer to be propagated than others.

DIAL-UP - The process of, or the equipment or facilities involved in, establishing a temporary connection via the switched telephone network.

DIAL TONE (DT) - Signal sent to an operator or subscriber indicating that the switch is ready to receive dial pulses.

DIGITAL - Referring to communications procedures, techniques, and equipment whereby information is encoded as either binary "1" or "0"; the representation of information in discrete binary form, discontinuous in time, as opposed to the analog representation of information in variable, but continuous, waveforms.

DIGITAL LOOPBACK - A technique for testing the digital processing circuitry of a communications device. It may be initiated locally, or remotely via a telecommunications circuit. The device being tested will echo back a received test message, after first decoding and then re-encoding it, the results of which are compared with the original message.

DIGITAL SIGNAL - Discrete or discontinuous signal; one whose various states are discrete intervals apart.

DIP - Dual-In-Line Package. Method of packaging electronic components for mounting on printed circuit boards.

DISTORTION - The modification of the waveform or shape of a signal caused by outside interference or by imperfections of the transmission system. Most forms of distortion are the result of the characteristics of the transmission system to the different frequency components.

DOTTING, DOUBLE DOTTING, PATTERN - The term "dotting" was coined by Bell to describe a data pattern consisting of alternate marks and spaces. The CCITT uses the full description of "alternating binary ones and zeros" on first needing this idea in a recommendation, but then abbreviate this to "reversals." By extrapolation, "double dotting" has come into use to refer to the data pattern termed "S1" which is used in V.22bis to indicate 2400 bit/s capability. The full description is "unscrambled double dibit 00 and 11 at 1200 bit/s for 100 + 3 ms."

DS-1 - Digital Signal level 1; telephony term describing a digital transmission format in which 24 voice channels are multiplexed into one 1.544 Mbit/s (U.S.) T1 digital channel.

DS-3 - Digital Signal level 3; telephony term describing the 44.736 Mbit/s digital signal carried on a T3 facility.

DTMF - Dualtone Multifrequency (DTMF) - Basis for operation of most push button telephone sets. An in-band signalling technique in which a matrix combination of two frequencies, each from a group of four, are used to transmit numerical address information; it encodes 16 possible combinations of tone pairs using two groups of four tones each. The two groups of four frequencies are 697 Hz, 770 Hz, 852 Hz, and 941 Hz, and 1209 Hz, 1336 Hz, 1477 Hz, and 1633 Hz. DTMF is used primary for call initiation in GSTN telephone applications.

E

ECHO - The distortion created when a transmitted signal is reflected back to the originating station.

ECHO CANCELLER - A devise used to reduce or eliminate echo. It operates by placing a signal that is equal and opposite to the echo signal on the return transmission path.

ECHO SUPPRESSOR - A mechanism used to suppress echoes on long-distance analog connections. The device suppresses the transmission path opposite in direction to the one being used. This feature, although necessary for voice transmission, often interferes with data transmission.

EIA - Electronic Industries Association

EIA INTERFACE, EIA232D, RS 232C - The logical, electrical and physical characteristics of the connection between a DTE and a modem is set out in EIA specification 232D. Previously this has been known as RS232C. The logical characteristics are essentially similar to those specified in CCITT recommendation V.24 and the electrical characteristics to those in V.28.

ELECTROMAGNETIC INTERFERENCE (EMI) - Radiation leakage outside a transmission medium that results mainly from the use of high-frequency wave energy and signal modulation. EMI can be reduced by appropriate shielding.

EMI - See Electromagnetic Interference.

ENVELOPE DELAY - An analog line impairment involving a variation of signal delay with frequency across the data channel bandwidth.

EQUALIZATION - The introduction of components to an analog circuit by a modem to compensate for the attenuation (signal loss) variation and delay distortion with frequency (attenuation equalization) and propagation time variations with frequency (delay equalization). Generally, the higher the transmission rate, the greater the need for equalization.

ERROR - In data communications, any unwanted change in the original contents of a transmission.

ERROR BURST - A concentration of errors within a short period of time as compared with the average incidence of errors. Retransmission is the normal correction procedure in the event of an error burst.

ERROR CONTROL - A process of handling errors, which includes the detection and in some cases, the correction of errors.

EXCHANGE - Assembly of equipment in a communications system that controls the connection of incoming and outgoing lines, and includes the necessary signaling and supervisory functions. Different exchanges, or switches, can be costed to perform different functions, e.g., Local exchange, trunk exchange, etc. See Class of Exchange. Also known as Central Office (U.S. Term).

EXCHANGE, PRIVATE AUTOMATIC BRANCH (PABX) - Private automatic telephone exchange that provides for the switching of calls internally and to and from the public telephone network.

EXCHANGE, PRIVATE BRANCH (PBX) - Private, manually operated telephone exchange that provides private telephone service to an organization and that allows calls to be transmitted to or from the public telephone network.

EXCHANGE AREA - Area containing subscribers served by a local exchange.

F

FILTER - Circuit designed to transmit signals of frequencies within one or more frequency bands and to attenuate signals of other frequencies.

FIRMWARE - Permanent or semi-permanent control coding implemented at a micro-instruction level for an application program, instruction set, operating routine, or similar user-oriented function.

FLOW CONTROL - The use of buffering and other mechanisms, such as controls that turn a device on and off, to prevent data loss during transmission.

FOUR-WIRE CIRCUIT OR CHANNEL - A circuit containing two pairs of wire (or their logical equivalent) for simultaneous (i.e., full-duplex) two-way transmission. Contrast with two-wire channel.

FRAME - 1) A group of bits sent serially over a communications channel; generally a logical transmission unit sent between data-link-layer entities that contain its own control information for addressing and error checking. 2) A piece of equipment in a common carrier office where physical cross connections are made between circuits.

FRAMING - Control procedure used with multiplexed digital channels such as T1 carriers, whereby bits are inserted so the receiver can identify the time slots allocated to each subchannel. Framing bits can also carry alarm signals indicating specific alarm conditions.

FREQUENCY - Rate at which an event occurs, measured in hertz, kilohertz, megahertz, etc.

FREQUENCY BANDS - Frequency bands are defined arbitrarily as follows:

Range (MHz)	Name
0.03-0.3	Low frequency (LF)
0.3-3.0	Medium frequency (MF)
3-30	High frequency (HF)
30-300	Very High frequency (VHF)
300-3000	Ultra high frequency (UHF)
3000-30,000	Super high frequency (SHF) (micro wave)
30,000-300,000	Extremely high frequency (EHF)(millimeterwave)

FSK - Frequency Shift Keying. A method of modulation that uses two different frequencies, usually phase continous, to distinguish between a mark (digital 1) and a space (digital 0) when transmitting on an analog line. Used in modems operating at 1200 bit/s or slower.

FULL-DUPLEX - Pertaining to the capability to send and receive simultaneously.

G

GAIN - Denotes an increase in signal power in transmission from one point to another, usually expressed in dB.

GUARD TONE - In CCITT recommendations V.22 and V.22bis, guard tones may optionally be transmitted along with the data signal from the answering modem. A single frequency of either 1800 or 550 Hz is used and the data signal power must be reduced to keep the overall energy level the same as for transmission without guard tone. The purpose of the guard tone is to prevent the high-band data signal from interfering with the operation of billing apparatus in certain countries.

GSTN - General Switched Telephone Network

H

HALF-DUPLEX - Pertaining to the capability to send and receive but not simultaneously.

HANDSHAKE - An exchange of control sequences between two locations to set up the correct parameters for transmission.

HDLC - High-level Data Link Control. Bit-oriented communication protocol developed by the ISO (International Standards Organization).

HARMONIC DISTORTION - A waveform distortion, usually caused by the nonlinear frequency response of a transmission.

HERTZ (Hz) - A measure of electromagnetic frequency; one hertz is equal to one cycle per second.

HF - High Frequency.

HIGH FREQUENCY (HF) - Portion of the electromagnetic spectrum, typically used in short-wave radio applications. Frequencies in the 3 to 30 MHz range.

Hz - See Hertz.

I

IEEE - Institute of Electrical and Electronics Engineers.

INITIALIZE - To set counters, switches, addresses, or contents of storage to zero or other starting values at the beginning of, or at prescribed points in, the operation of a computer routine.

INTERFACE - A hardware and/or software link between two devices. The interface defines all signal characteristics and other specifications for physical interconnection of the devices.

INTEROFFICE TRUNK - Direct trunk between local central offices (Class 5 offices), or between Class 2, 3, or 4 offices; also called intertoll trunk.

ISO - International Organization for Standardization.

ITU - International Telecommunications Union. The parent organization of the CCITT.

J

JITTER - Slight movement of a transmission signal in time or phase that can introduce errors and loss of synchronization for high-speed synchronous communications. See Phase jitter.

K

KEY PULSING (KP) - Manual method of sending numerical and other signals by the operation of nonlocking pushkeys. Also called Key Sending.

KEY SERVICE UNIT (KSU) - Main operating unit of a key telephone system.

KEY TELEPHONE SYSTEM (KTS) - When more than one telephone line per set is required, pushbutton or key telephone systems offer flexibility and a wide variety of uses, e.g., pickup of several exchange lines, PABX station lines, private lines, and intercommunicating

lines. Features of the system include pickup and holding intercommunications, visual and audible signals, cutoff, exclusion, and signaling.

KP - Key Pulse (signaling unlocking signal). See Key Pulsing.

kHz - Kilohertz, kilocycles per second.

KTU - Key Telephone Unit. See Key Service Unit.

L

LEASED LINE - A line rented exclusively to one customer for voice or data communications; dedicated circuit, typically supplied by the telephone company or transmission authority, that permanently connects two or more user locations and is for the sole use of the subscriber. Such circuits are generally voice grade in capacity and in range of frequencies supported, are typically analog, are used for voice or data, can be point-to-point, or multipoint, and can be enhanced with line conditioning. Also called private line, tie line, or dedicated facility.

LED - Light-Emitting Diode.

LIGHT-EMITTING DIODE (LED) - Semiconductor junction diode that emits radiant energy and is used as a light source for fiber optic communications, particularly for short-haul links.

LIMITED-DISTANCE MODEM - A short-haul modem or line driver that operates over a limited distance. Some limited-distance modems operate at higher speeds than modems that are designed for use over analog telephone facilities, since line conditions can be better controlled.

LINE HIT - A transient disturbance causing a detectable error on a communications line.

LINE-LOADING - The process of installing loading coils in series with each conductor on a transmission line. Usually 88 milliHenry coils installed at 6,000 foot intervals.

LINK - 1) A physical circuit between two points. 2) A logical circuit between two users of a packet switched (or other) network permitting them to communicate (although different physical paths may be used).

LINK LAYER - The logical entity in the OSI model concerned with transmission of data between adjacent network nodes. It is the second layer processing in the OSI model, between the physical and the network layers.

LOADING COILS - An inductance coil installed at regular intervals along a transmission line. Used to improve the quality of voice grade circuits.

LOCAL EXCHANGE - Exchange in which subscribers' lines terminate. The exchange has access to other exchanges and to national trunk networks. Also called local central office, end office.

LOCAL LOOP - The part of a communications circuit between the subscriber's equipment and the equipment in the local exchange.

LOCAL TRUNK - Trunks between local exchanges.

LOSS (TRANSMISSION) - Decrease in energy of signal power in transmission along a circuit due to the resistance or impedance of the circuit or equipment.

M

MARK - The signal (communications channel state) corresponding to a binary one. The marking condition exists when current flows (current-loop channel) or when the voltage is more negative than -3 volts (EIA RS-232 channel).

MATRIX - In switch technology, that portion of the switch architecture where input leads and output leads meet, any pair of which may be connected to establish a through circuit. Also called switching matrix.

Mbit/s - Megabits per second.

MEGAHERTZ (MHz) - A unit of frequency equal to one million cycles per second.

MF - 1) Medium Frequency. 2) Multifrequency. See Dualtone Multifrequency Signaling (DTMF).

MODEM - A contraction of modulate and demodulate; a conversion device installed in pairs at each end of an analog communications line. The modem at the transmitting end modulates digital signals received locally from a computer or terminal; the modem at the receiving end demodulates the incoming signal, converting it back to its original (i.e., digital) format, and passes it to the destination business machine.

MODULATION - The application of information onto a carrier signal by varying one or more of the signal's basic characteristics (frequency, amplitude, or phase); the conversion of a signal from its original (e.g., digital) format to analog format.

MODULATION, PULSE CODE (PCM) - Digital transmission technique that involves sampling of an analog information signal at regular time intervals and coding the measured amplitude value into a series of binary values, which are transmitted by modulation of a pulsed, or intermittent, carrier. A common method of speech digitizing using 8-bit code words, or samples, and a sampling rate of 8 kHz.

Ms - Millisecond. One-thousandth of a second.

MULTIPLEXER - Device that enables more than one signal to be sent simultaneously over one physical channel.

MULTIPLEXING - Division of a transmission facility into two or more channels either by splitting the frequency band transmitted by the channel into narrower bands, each of which is used to constitute a distinct channel (frequency-division multiplex), or by allotting this common channel to several different information channels, one at a time (time-division multiplexing).

MUX - See Multiplexer.

N

NAK - "Negative acknowledge" character. A transmission control character that indicates a block of data was received incorrectly.

NOISE - Undesirable energy in a communications path, which interferes with the reception or processing of a signal.

Ns - Nanosecond; also nsec. One-billionth of a second.

O

OFF HOOK - By analogy with the normal household telephone, a modem is off-hook when it is using the telephone line to make a call. This is similar to raising the telephone handset, or taking it off the hook. Going off-hook is also known as "seizing the line."

ON-HOOK - By analogy with the normal household telephone, a modem is on-hook when it is not using the telephone line. As with a telephone where the handset is on the hook, the line may be used by other equipment to make a call. Going on-hook is also known as "dropping the line."

OSI - Open Systems Interconnection. Referring to the reference model, OSI is a logical structure for network operations standardized within the ISO; a seven-layer network architecture being used for the definition of network protocol standards to enable any OSI-compatible computer or device to communicate with any other OSI-compliant computer or device for a meaningful exchange of information.

OVERFLOW - Excess traffic on a particular route, which is offered to another (alternate) route.

P

PABX - Private Automatic Branch Exchange. See Exchange, Private Automatic Branch (PABX).

PACKET - A group of binary digits including data and call control signals that is switched as a composite whole. The data, call control signals, and error control information are arranged in a specified format.

PBX - Private Branch Exchange. See Exchange, Private Branch.

PHASE JITTER - In telephony, the measurement, in degrees out of phase, that an analog signal deviates from the referenced phase of the main data-carrying signal. Often caused by alternating current components in a telecommunications network; or: a random distortion of signal lengths caused by the rapid fluctuation of the frequency of the transmitted signal. Phase jitter interferes with interpretation of information by changing the timing.

PHASE MODULATION - One of three ways of modifying a sine wave signal to make it carry information. The sine wave or "carrier" has its phase changed in accordance with the information to be transmitted.

PROPAGATION DELAY - The period between the time when a signal is placed on a circuit and when it is recognized and acknowledged at the other end. Propagation delay is of great importance in satellite channels because of the great distances involved.

PROTOCOL - A set of procedures for establishing and controlling communications. Examples include BSC, SDLC, X.25, V.42, V.42bis, MNP, V.22bis handshake, etc.

PSK - Phase Shift Keying. A method of modulation that uses the differences in phase angle between two symbols to encode information. A reference oscillator determines the phase angle change of the incoming signal, which in turn determines which bit or dibit is being transmitted. DPSK (Differential Phase Shift Keying) is a variation of PSK which changes the phase relative to the previous phase.

PULSE CODE MODULATION (PCM) - A method of transmitting information by varying the characteristics of a sequence of pulses, in terms of amplitude, duration, phase, or number. Used to convert an analog signal into a digital bit stream for transmission.

R

REGENERATIVE REPEATER - 1) Repeater utilized in telegraph applications to retime and retransmit the received signal impulses and restore them to their original strength. These repeaters are speed- and code-sensitive and are intended for use with standard telegraph speeds and codes. 2) Repeater used in PCM or digital circuits which detects, retimes, and reconstructs the bits transmitted.

REGENERATOR - Equipment that takes a digital signal that has been distorted by transmission and produces from it a new signal in which the shape, timing, and amplitude of the pulses are that same as those of the original before distortion.

REPEATER - 1) In analog transmission, equipment that receives a pulse train, amplifies it and retimes it for retransmission. 2) In digital transmission, equipment that receives a pulse train, reconstructs it, retimes it, and often then amplifies the signal for retransmission. 3) In fiber optics, a device that decodes a low-power light signal, converts it to electrical energy, and then retransmits it via an LED or laser-generating light source. See also Regenerative Repeater.

REVERSE CHANNEL - A simultaneous low speed data path in the reverse direction over a half-duplex facility. Normally, it is used for positive/negative acknowledgements of previously received data blocks.

RINGER EQUIVALENCE NUMBER - This is a number that the FCC assigns to approved telecom equipment that measures how much load it places on the network during ringing. In the U.S.A., you can connect telephones, modems, FAX machines etc. In parallel to the same telephone line only as long as the sum of their ringer equivalence numbers is less than five. Most countries have a similar regulating system in force, although the methods used to arrive at the number vary widely.

RINGING SIGNAL - Any AC or DC signal transmitted over a line or trunk for the purpose of alerting a party at the distant end of an incoming call. The signal can operate a visual or sound-producing device.

RINGING TONE - Tone received by the calling telephone indicating that the called telephone is being rung. Also called Ringback.

S

SCRAMBLER/DESCRAMBLER - A scrambler function uses a defined method for modifying a data stream, in order to make the altered data stream appear random. A descrambler reverses the effect of the scrambler using the previously defined method to recover the original data stream. Most often used for data encryption, or to avoid transmitting repetitive data patters that can adversely affect data recovery in modems and other data transmission equipment.

SDLC - Synchronous Data Link Control. IBM bit oriented protocol providing for half-duplex transmission; associated with IBM's System Network Architecture (SNA).

SHIELDED PAIR - Two insulated wires in a cable wrapped with metallic braid or foil to prevent interference and provide noise-free transmission.

SIGNAL-TO-NOISE RATIO - The relative power of a signal as compared to the power of noise on a line. As the ratio decreases, it becomes more difficult to distinguish between information and interference.

SIMPLEX - Pertaining to the capability to move in one direction only. Contrast with half-duplex and full-duplex.

SIGNALING - Process by which a caller or equipment on the transmitting end of a line informs a particular party or equipment at the receiving end that a message is to be communicated.

SPACE - Opposite signal condition to a "mark." The signal (communications channnel state) corresponding to a binary zero. In an EIA RS-232 channel, the spacing condition exists when no current flows (current loop channel) or when the voltage is more positive than ±3 volts.

ST - Start (signal to indicate end of outpulsing).

START-STOP (SIGNALING) - Signaling in which each group of code elements corresponding to a character is preceded by a start signal that serves to prepare the receiving mechanism for the reception and registration of character, and is followed by a stop signal that serves to bring the receiving mechanism to rest in preparation for the reception of the next character. Also known as asynchronous transmission.

STOP-BIT - In asynchronous transmission, the quiescent state following the transmission of a character; usually 1-, or 2-bit times long.

STOP ELEMENT - Last bit of a character in asynchronous serial transmission, used to ensure recognition of the next start element.

SUBSCRIBER LINE - Telephone line connecting the exchange to the subscriber's station. Also called (U.S.term) access line and subscriber loop.

SYNCHRONOUS - Having a constant time interval between successive bits, characters, or events. Synchronous transmission doesn't use non-information bits (such as the start and stop bits in asynchronous transmission) to identify the beginning and end or characters, and thus is faster and more efficient than asynchronous transmission. The timing is achieved by transmitting sync characters prior to data or by extracting timing information from the carrier or reference.

SYNCHRONOUS NETWORK - Network in which all the communications links are synchronized to a common clock.

SYNCHRONOUS TRANSMISSION - Transmission process where the information and control characters are sent at regular, clocked intervals so that the sending and receiving terminals are operating continuously in step with each other.

T

T-CARRIER - A time-division multiplexed, digital transmission facility, operating at an aggregate data rate of 1.544 Mbit/s and above. T-carrier is a PCM system using 64 Kbit/s for a voice channel.

T1 - A digital facility used to transmit a DS-1 formatted digital signal at 1.544 Mbit/s; the equivalent of 24 voice channels.

T1C/T2/T3/T4 - Digital carrier facilities used to transmit signals at 3.152M, 6.312M, 44.736M, 274.176 Mbit/s, respectively.

T3 - A digital carrier facility used to transmit a DS-3 formatted digital carrier signal at 44.736 Mbit/s; the equivalent of 672 voice channels.

TOUCH-TONE - An AT&T trademark for dualtone multifrequency signaling equipment. Use of tones simplifies the switching system design and greatly expands the potential for adding features to telephone systems. It also speeds up the dialing operation for a person making a call.

TRANSCEIVER - Device that can transmit and receive traffic.

TRUNK - Transmission paths that are used to interconnect exchanges in the main telephone network, two switching centers, or a switching center and a distribution point, such as a telephone exchange line that terminates in a PABX network.

TTL - Transistor-Transistor Logic. Digital logic family having common electrical characteristics.

TURNAROUND TIME - The time required to reverse the direction of transmission, e.g; to change from receive mode to transmit mode in order to acknowledge on a half-duplex line. When individual blocks are acknowledged, as is required in certain protocols (e.g., IBM BSC) the turnaround time has a major effect on throughput, particularly if the propagation delay is lengthy, such as on a satellite channel.

TWO-WIRE CIRCUIT - Circuit formed of two conductors insulated from each other, providing a send and return path. Signals may pass in one or both directions.

V

VIDEOTEX - An interactive data communications application designed to allow unsophisticated users to converse with remote databases, enter data for transactions, and retrieve textual and graphics information for display on subscriber television sets or low-cost terminals.

VSLI - Very Large Scale Integration.

V SERIES RECOMMENDATIONS - (CCITT V.xx Standards)
Also see Voiceband Modem Standards chart on page 9-12.

V.1 - Definitions of key terms for binary symbol notation, such as binary 0 = space, binary 1 = mark.

V.2 (1) - Specification of power levels for data transmission over telephone line.

V.4 - Definition of the order of bit transmission, the use of a parity bit, and the use of start/stop bits for asynchronous transmission.

V.5 - Specification of data-signaling rates (bit/s) for synchronous transmission in the switched telephone network.

V.6 - Specification of data signaling rates (bit/s) for synchronous transmission on leased telephone circuits.

V.7 - Definitions of other key terms used in the V-series recommendations.

V.10 - Description of an unbalanced physical level interchange circuit (unbalanced means one active wire between transmitter and receiver with ground providing the return).

V.11 - Description of a balanced physical level interchange circuit (balanced means two wires between the transmitter and receiver with both wires' signals constant with respect to Earth).

V.15 - Description of use of acoustic couplers for data transmission.

V.16 - Description of the transmission of ECG (electrocardiogram) signals on the telephone channel.

V.19 - Description of one-way parallel transmission modems using push-button telephone sets.

V.20 - Description of one-way parallel transmission modems, excluding push-button telephone sets.

V.22bis - Operating at 1.2 Kbit/s, encodes two consecutive bit (dibits); the dibits are encoded as a change relative to the previous signal element.

V.22bis - Operating at 2.4 Kbit/s, encodes four consecutive bits (quadbits); the first two bits are encoded relative to the quadrant of the previous signal element, the last two bits are associated with the new quadrant.

V.24 - Definition of the interchange circuit pins between DTEs (data terminal equipment) and DCEs (data circuit-terminating equipment).

V.25 - (2) - Specifications for automatic-answering equipment.

V.25bis - (2) - Specifications for automatic-answering equipment.

V.28 - Description of unbalanced interchange circuits operating below 20 Kbit/s.

V.29 - Operating at 9.6 Kbit/s, encodes four consecutive bits (quadbits); the first bit determines the amplitude, the last three bits use the encoding scheme of V.27.

V.29 - Operating at 4.8 Kbit/s, encodes two consecutive bits (dibits); amplitude is constant and phase changes are the same as V.26.

V.31 - Description of low-speed interchange circuits (up to 75 Bit/s).

V.31bis - Description of low-speed interchange circuits (up to 1.2 Kbit/s).

V.32 - Operating at 9.6 Kbit/s, encodes four consecutive bits (quadbits); the bits are mapped to a QAM signal.

V.32 - Operating at 9.6 Kbit/s with Trellis-coded modulation (TCM), encodes four consecutive bits, two of which are used to generate a fifth bit; the bits are mapped to a QAM signal.

V.32 - Operating at 4.8 Kbit/s, encodes two consecutive bits (dibits), which are mapped to a QAM signal.

V.42 - Defines a method of error control.

V.42bis - Defines a method of data compression.

Note: In the United States, EIA RS-496 specifies these measurements and RS-366 specifies these procedures.

VOICE-GRADE CHANNEL - a channel with a frequency range from 300 to 3000 Hz and suitable for the transmission of speech, data, or facsimile.

W

WORD - A group of bits handled as a logical unit; usually 16.

Voiceband Modem Standards

CCITT Standard	Data Rate (Bit/s)	Full- or Half-Duplex	Channel Separation	Carrier Frequency (Hz)	Modulation Method	Modulation Rate (Baud)	Bits Encoded	Synchronous or Asynchronous	Back Channel	GSTN	Leased Lines	Equalization	Scrambler
V.21	300	Full	Frequency Division	1080, & 1750	Frequency Shift	300	1:1	Either	ND	Yes	No	ND	ND
V.22	1200	Full	Frequency Division	1200, & 2400	Phase Shift	600	2:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed	Yes
V.22	600	Full	Frequency Division	1200, & 2400	Phase Shift	600	1:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed	Yes
V.22bis	2400	Full	Frequency Division	1200, & 2400	Quadrature-Amplitude Modulation	600	4:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed/ Adaptive	Yes
V.22bis	1200	Full	Frequency Division	1200, & 2400	Quadrature-Amplitude Modulation	600	2:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed/ Adaptive	Yes
V.23	600 (1)	Half	N/A	1300, & 1700	Frequency Modulation	600	N/A	Either	Yes	Yes	No	ND	ND
V.23	1200 (1)	Half	N/A	1300, & 2100	Frequency Modulation	1200	N/A	Either	Yes	Yes	No	ND	ND
V.25	2400	Full	4-Wire	1800	Phase Shift	1200	2:1	Synchronous	Yes	No	Point-to-Point Multipoint 4-Wire	ND	ND
V.26bis	2400	Half	N/A	1800	Phase Shift	1200	2:1	Synchronous	Yes	Yes	No	Fixed	ND
V.26bis	1200	Half	N/A	1800	Phase Shift	1200	1:1	Synchronous	Yes	Yes	No	Fixed	ND
V.26ter	2400	Either	Echo Cancellation	1800	Phase Shift	1200	2:1	Either	ND	Yes	Point-to-Point 2-Wire	Either	Yes
V.26ter	1200	Either	Echo Cancellation	1800	Phase Shift	1200	1:1	Either	ND	Yes	Point-to-Point 2-Wire	Either	Yes
V.27	4800	Either	ND (3)	1800	Phase Shift	1600	3:1	Synchronous	Yes	No	Yes (3)	Manual	Yes
V.27bis	4800	Either	4-Wire (4)	1800	Phase Shift	1600	3:1	Synchronous	Yes	No	2-Wire, 4-Wire	Adaptive	Yes
V.27bis	2400	Either	4-Wire (4)	1800	Phase Shift	1200	2:1	Synchronous	Yes	No	2-Wire, 4-Wire	Adaptive	Yes
V.27ter	4800	Half	None	1800	Phase Shift	1800	3:1	Synchronous	Yes	Yes	No	Adaptive	Yes
V.27ter	2400	Half	None	1800	Phase Shift	1200	2:1	Synchronous	Yes	Yes	No	Adaptive	Yes
V.29	9600	Either	4-Wire	1700	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	No	No	Point-to-Point 4-Wire	Adaptive	Yes
V.29	7200	Either	4-Wire	1700	Phase Shift (5)	2400	3:1	Synchronous	ND	No	Point-to-Point 4-Wire	Adaptive	Yes
V.29	4800	Either	4-Wire	1700	Phase Shift (5)	2400	2:1	Synchronous	ND	No	Point-to-Point 4-Wire	Adaptive	Yes
V.32	9600	Full	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32bis	14400	Full (proposed)	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32	9600	Full	Echo Cancellation	1800	Trellis-Coded Modulation	2400	5:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32	4800	Full	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	2:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.33	14400	Half						Synchronous	ND	Yes		Adaptive	Yes
Bell (U.S.) Standard													
103	300	Full	Frequency Division	2225 & 1270(m) 2025 & 1070(s)	Frequency Shift	300	1:1	Either	No	Yes	No	Fixed	No
201	2400	Half	None	1800	Phase Shift	1200	2:1	Synchronous	No	Yes	Point-to-Point 2-Wire	Adaptive	Yes
202	1200	Half	None	1200 & 2200	FSK	1200	1:1	Either	Yes	Yes	Point-to-Point 2-Wire	Fixed	No
208	4800	Half	None	1800	Quadrature-Amplitude Modulation	1600	3:1	Synchronous	No	Yes	Point-to-Point 2-Wire	Adaptive	Yes
212	1200	Full	Frequency Division	1200 & 2400	Phase Shift	600	2:1	Either	No	Yes	No	Fixed	Yes

1. Bit/s not used in specification; rate stated in baud
2. Half-duplex may still use a backward channel
3. Makes no mention of 4-wire (must be assumed)
4. For half-duplex, 2-wire used
5. Amplitude is constant on a relative basis

ND = Not defined (i.e., not specified in the recommendation)

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