INTEGRATED CIRCUITS FOR
COMMUNICATIONS PRODUCTS

• LAN/WAN • PCMCIA • Datacom/FAX Modems • Wireless Communication •

PCM Line Transceivers • Single Chip Modems • DTMF

Bus Interface • Programmable Filters • Integrated Line Interface

• Modem Device Sets • Ethernet Media Access Controllers • UARTs •

1993 DATA BOOK

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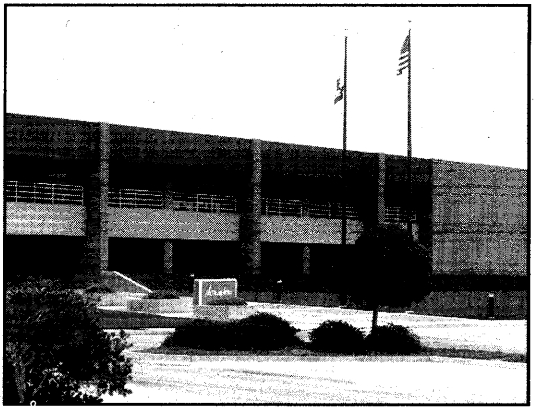
The Company



Silicon Systems' Santa Cruz facility, site of six-inch wafer fabrication line.

Silicon Systems specializes in the design and manufacture of application-specific, mixed-signal integrated circuits (MSICs®). If offers a sophisticated line of custom and standard ICs aimed primarily at the storage, communications and automotive products marketplace.

The company, which is headquartered in California, 30 miles south of Los Angeles, was founded in 1972 as a design center. It soon entered into manufacturing and today has two fabrication sites in California and approximately 2,000 employees worldwide. Additional operations include assembly and test facilities in California and Singapore and design engineering centers in California as well as in Tokyo and Singapore.

Reliability and quality are built into Silicon Systems' products through the use of statistical problem solving techniques, analytical controls, and other quantitative methods. The company is committed to the goal of customer satisfaction through the on-time delivery of defect-free products that meet or exceed the customer's expectations and requirements. This statement reflects the corporate quality mission and contains key elements instrumental in attaining true customer satisfaction. Listed in the back of this publication is a worldwide network of sales representatives and distributors ready to serve you.

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Table of Contents

Target, Advanced and Preliminary Information
In this data book the following conventions are used in designating a data sheet "Target," "Advanced" or "Preliminary":

Target Specification–
The target specification is intended as an initial disclosure of specification goals for the product. Product is in first stages of design cycle.

Advance Information–
Indicates a product still in the design cycle, undergoing testing processes, and any specifications are based on design goals only. Do not use for final design.

Preliminary Data–
Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Index

* Data Sheet available upon request

Numerical Index

*Data Sheet available upon request

Discontinued Parts List

The following parts are no longer supplied or supported by Silicon Systems. Please note alternate sources.

Part #	Alternate Source	Part #	Alternate Source
SSI 32F8000	SSI 32F8001	SSI 75T957	Teltone Corporation
SSI 73D2180	None	SSI 75T981	Teltone Corporation
SSI 73D2404	None	SSI 75T982	Teltone Corporation
SSI 73D2420/2421	None	SSI 78P8050	Rockwell
		SSI 78P8060	Rockwell

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COMMUNICATION PRODUCTS REFERENCE

Device Number	B212 B103	B202	CCITT V.21	CCITT V.23	CCITT V.22	CCITT V.22bis	Description	Power Supply	Available Packages
K-SERIES SINGLE CHIP MODEM FAMILY									
SSI 73K212	✗						Bell 212A/103	+12V	28 DIP, 28 PLCC
SSI 73K212S	✗						73K212 with serial interface only	+12V	22 DIP
SSI 73K212L	✗						Low Power 73K212	+5V	28 DIP, 28 PLCC
SSI 73K212SL	✗						73K212L with serial interface only	+5V	22 DIP
SSI 73K221			✗		✗		CCITT V.22/V.21	+12V	22, 28 DIP, 28 PLCC
SSI 73K221S			✗		✗		73K221 with serial interface only	+12V	22 DIP
SSI 73K221L			✗		✗		Low Power 73K221	+5V	22, 28 DIP, 28 PLCC
SSI 73K221SL			✗		✗		73K221L with serial interface only	+5V	22 DIP
SSI 73K222	✗		✗		✗		Bell 212A/103, CCITT V.22/V.21	+12V	22, 28 DIP, 28 PLC
SSI 73K222S	✗		✗		✗		73K222 with serial interface only	+12V	22 DIP
SSI 73K222L	✗		✗		✗		Low Power 73K222	+5V	22, 28 DIP, 28 PLCC
SSI 73K222SL	✗		✗		✗		73K222L with serial interface only	+5V	22 DIP
SSI 73K222U	✗		✗		✗		73K222L with 16C450 UART	+5V	40 DIP, 44 PLCC
SSI 73K224L	✗		✗		✗	✗	Bell 212A/103, CCITT V.22bis/V.22/V.21	+5V	28 DIP, 28, 32 PLCC, 52 QFP, 64 TQFP
SSI 73K224SL	✗		✗		✗	✗	73K224L with serial interface	+5V	22 DIP
SSI 73K302L	✗	✗					Bell 212A/202/103	+5V	28 DIP, 28 PLCC
SSI 73K302SL	✗	✗					Bell 212A/202/103; serial interface only	+5V	22 DIP
SSI 73K312L	B103	✗	✗	✗			BELL 202/103; CCITT V.21/V.23	+5V	28 DIP, 28 PLCC, 52 QFP, 64 TQFP
SSI 73K321L			✗	✗			CCITT V.23/V.21	+5V	28 DIP, 28 PLCC
SSI 73K321SL			✗	✗			73K321L with serial interface only	+5V	22 DIP
SSI 73K322L			✗	✗	✗		CCITT V.23/V.22/V.21	+5V	28 DIP, 28 PLCC
SSI 73K322SL			✗	✗	✗		73K322L with serial interface only	+5V	22 DIP
SSI 73K324L	B212		✗	✗	✗	✗	CCITT V.22bis/V.22/V.23/V.21	+5V	28 DIP, 28, 32 PLCC 52 QFP, 64 TQFP
MODEM PROTOCOL PRODUCTS/ DEVICE SETS									
SSI 73D2240	✗	✗	✗	✗			Modem Device Set w/ AT (73K224L based design)	+5V	Various DIP & PLCC
SSI 73D2247/Z	✗	✗	✗	✗	✗	✗	Modem Device Set w/ AT, MNP 4&5	+5V	Various DIP & PLCC
SSI 73D2248/2348				✗	✗	✗	Modem Device Set w/ AT, MNP	+5V	Various QFP & TQFP

Notes: The SSI 73D2247 Device Set comes with a Configurable Command Interpreter, and can be ordered with or upgraded to 9600 bit/s send/receive FAX.

Device Number	Circuit Function	Features	Power	Available Packages
SPECIAL MODEM PRODUCTS				
SSI 73M214	2400 bit/s Modem Filter	V.22bis/V.22/V.21, Bell 212/103 modes	±5V	28 DIP, PLCC
SSI 73M223	1200 bit/s Modem IC	Compact HDX V.23 modem	+5V	16 DIP, 16 SOL
SSI 73M376	Integrated Line Interface	The active components of a DAA in a chip used on 73M9001	+5V	28 PLCC, 24 VSOP
ANALOG SIGNALLING AND SWITCHING PRODUCTS				
SSI 75T201	Integrated DTMF Receiver	Binary coded 2-of-8 output	+12V	22 DIP
SSI 75T202	Integrated DTMF Receiver	Low power, binary output	+5V	18 DIP
SSI 75T203	Integrated DTMF Receiver	Early detect, binary output	+5V	18 DIP
SSI 75T204	Integrated DTMF Receiver	Low power, binary output	+5V	14 DIP, 16 SO
SSI 75T2089	Integrated DTMF Transceiver	Generator & receiver, µP interface	+5V	22 DIP
SSI 75T2090	Integrated DTMF Transceiver	Like 75T2089 w/ call progress detect	+5V	22 DIP
SSI 75T2091	Integrated DTMF Transceiver	Like 75T2090 w/ early detect	+5V	28 DIP, PLCC
SSI 75T980	Imprecise Call Progress Detector	Energy detect in 305-640 Hz band, Teltone	+5V	8 DIP
SSI 78A093A/B	12x8x1 Crosspoint Switch	Low ON resistance, two versions	+5, +12V	40 DIP, 44 PLCC
SSI 78A207	Integrated MF Receiver	Detects central office toll signals	+5V	20 DIP
PCM PRODUCTS				
SSI 78P233	DS-1 Line Interface	T1 clock & data recovery, transmit equalization	+5V	24 DIP, SDIP, SO
SSI 78P234	2048 kBit/s PCM Interface	Receive clock & data recovery, transmit drivers	+5V	20 DIP, SO
SSI 78P236	DS-3 Line Interface	T3 clock & data recovery, transmit equalization	+5V	28 DIP
SSI 78P300	T1/E1 Short Haul Transceiver	Receive jitter attenuation	+5V	28 DIP, PLCC
SSI 78P2361	STS-1 Line Interface Transceiver	STS-1 clock & data recovery, transmit equalization	+5V	28 DIP
SSI 78P2362	CEPT E-3 Line Interface Transceiver	E3 clock & data recovery, transmit equalization	+5V	28 DIP
SSI 78P7200	DS-3 Line Interface Transceiver	DS-3 Transceiver w/Receive equalization & higher transmitter drive	+5V	28 DIP
LAN PRODUCTS				
SSI 78Q902	10BaseT MAU Transceiver	Direct interface to twisted pair and AUI	+5V	28 DIP, PLCC
SSI 78Q903	10BaseT Hub Transceiver	Programmable squelch, detect/correct reverse polarity	+5V	24 DIP, 28 PLCC
SSI 78Q8330	802.3 Coax Transceiver	10Base-2 applications	+9V	20 DIP, PLCC, 64 TQFP
SSI 78Q8330A	802.3 Coax Transceiver	10Base-2/10Base-5 applications	+9V	20 DIP, PLCC, 64 TQFP
SSI 78Q8360	Ethernet Controller/ENDEC Combo	Fully integrated MAC ENDEC & AUI	+5V	100 QFP, TQFP
SSI 78Q8370	PCMCIA Ethernet Combo	Highly integrated PCMCIA MAC ENDEC & AUI	+5V	100 QFP, TQFP
BUS INTERFACE PRODUCTS				
SSI 73M450L	16C450 pin compatible UART		+5V	40 DIP, 44 PLCC
SSI 73M1450	28-pin version of SSI 73M450	Full UART in 28-pin package	+5V	28 DIP, PLCC
SSI 73M2450	28-pin version of 73M450	Adds µPRST function	+5V	28 DIP, PLCC
SSI 73M550	16C550 pin compatible UART	Receive and Transmit FIFOs	+5V	40 DIP, 44 PLCC, 48 GT
SSI 73M1550	28-pin version of SSI 73M550	Full UART in 28-pin package	+5V	28 DIP, PLCC
SSI 73M2550	28-pin version of 73M550	Adds µPRST function	+5V	28 DIP, PLCC

Communications ICs at Silicon Systems

Silicon Systems has built its 21-year reputation on the design and manufacture of both custom and standard mixed-signal ICs, or MSICs®.

All communications ICs, to one degree or another, involve mixed-signal design. All input or output real-world, analog signals and digitize them somewhere in between. In fact, the digital signal processing in modem design gave birth to the DSP found in most of today's computers.

Silicon Systems' designers are experts in protocol and signal processing — analog, digital, wired and wireless. But you should know that easily half of our business is in custom design, and all of our ICs are application-specific. We think this gives us an edge in customer-driven engineering.

We can build mixed-signal circuits which conform to almost limitless requirements for partitioning, cost, footprint, performance and power. In other words, we have the tools to do the job exactly the way you want it.

Why not send for a free copy of our *Tool Kit* brochure for a look at what we've developed in the past and what we can develop for you in the future. Bring us your application, and we'll break out the tools.

Section 1

K-SERIES MODEM FAMILY

Silicon Systems' K-Series Family of One-Chip Modems

Silicon Systems is a leader in the design and manufacturing of CMOS VLSI modems. Currently, Silicon Systems offers the most extensive line of one-chip modem ICs available, with high-performance, cost-effective designs suitable for a wide range of applications. Silicon Systems' fully compatible modem IC family has redefined the modem IC as a universal component which can be easily integrated into any system. Designs can be upgraded to meet different standards and speeds by simply substituting one K-Series IC for another. Using a K-Series family modem IC in your application eliminates product obsolesence, and minimizes development costs.

The Silicon Systems modem IC family consists of four basic products:

1. The SSI 73K222L, a multi-mode device which combines both Bell 212A/103 and V.22/V.21 capability in one chip, with operating modes at 0 - 30, 600 and 1200 bit/s.
2. The SSI 73K222U which combines the functionality of the 73K222L with the industry standard 16C450 UART.
3. The SSI 73K224L, a major technological breakthrough which provides 2400 bit/s V.22bis operation in addition to V.22/V.21 and Bell 212A/103 modes in a single IC.
4. The SSI 73K322L provides CCITT V.22/V.21 plus V.23 Videotex modes.

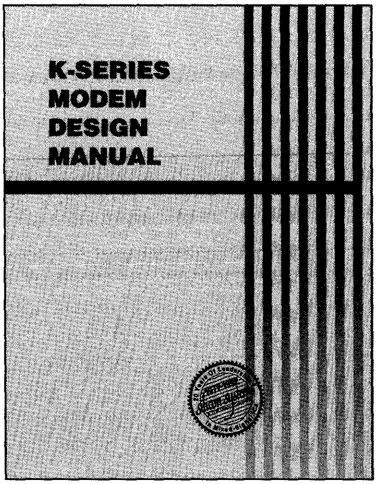
New additions to Silicon Systems' modem IC family extend the available operating modes and provide features which greatly simplify integral modem design. The SSI 73K324L offers V.22bis, V.22/V.21 and V.23 operating modes on one chip. These products dramatically reduce external circuitry required for dedicated integral modem designs.

Silicon Systems' one-chip modem IC products represent technical achievements unmatched in the industry. An advanced Digital Signal Processor resides on the same chip with sophisticated analog circuitry in the SSI 73K224L and SSI 73K324L products. "U" versions of the K-Series devices integrate an industry standard UART with full modem capability on a single chip. In addition, an innovative bus structure makes a separate controller unnecessary in dedicated integral designs. All K-Series devices are available in low-power versions. This feature allows optimal performance with single +5V supply operation and is unique to Silicon Systems' products.

Silicon Systems' single-chip modem IC family is designed to be the most effective solution for a wide variety of modem applications. The products provide for a full range of communications standards and speeds up to 2400 bit/s. Moreover, features can be extended to include additional modes and higher operating speeds without impacting existing designs. Take advantage of these capabilities. Design for tomorrow's needs today by using Silicon Systems' K-Series modem IC family.

K-Series Modem Design Manual

The Silicon Systems K-Series Modem Design Manual contains a large body of application literature for the K-Series family of single chip modem products. This manual is intended as a tutorial for those users who may be designing with modems for the first time, and also as a helpful guide for more experienced modem designers.



The K-Series Modem Design Manual is available through our worldwide network of representatives and distributors.

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SSI 73K212/K212L
Bell 212A/103
Single-Chip Modem

December 1992

DESCRIPTION

The SSI 73K212 is a highly integrated single-chip modem IC which provides the functions needed to construct a typical Bell 212A full–duplex modem. Using an advanced CMOS process that integrates analog, digital and switched–capacitor filter functions on a single substrate, the SSI 73K212 offers excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K212L low power version of the SSI 73K212 provides identical performance and features, but operates from a single +5V supply with substantially lower power consumption.

The SSI 73K212 includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes and a DTMF dialer. This device supports all Bell 212A modes of operation allowing both synchronous and asychronous communications.

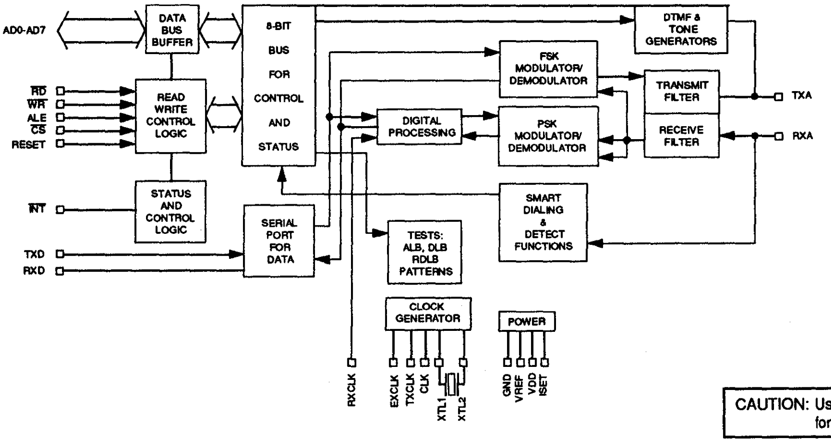
Test features such as analog loop, digital loop, and remote digital loopback are provided. Internal pattern generators are also included for self-testing. The SSI73K212 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors

(Continued)

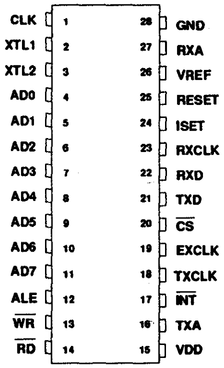
FEATURES

- **One-chip Bell 212A and 103 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone and long loop detectors**
- **DTMF generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V**
- **Single +5V (73K212L) or +12V (73K212) versions**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

(80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K212 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level convertor for a typical system. The SSI 73K212 is part of SSi's K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K212 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data within a 0.01% rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 bit/s +1.0%, - 2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bit/s ± .01% (±.01% is the required synchronous data rate accuracy).

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K212 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K212 uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In the Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 mode.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K212 control and status registers via a serial command port (22-pin version only). In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal, (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (73K212) or 5V 10% (73K212L). Bypass with .1 and 22 µF capacitors to ground.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{\text{CS}}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{\text{CS}}$	20	-	I	Chip select. A low during the falling edge of ALE on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{\text{CS}}$ (latched) is not active. The state of $\overline{\text{CS}}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{\text{INT}}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{\text{INT}}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{\text{RD}}$	14	-	I	Read. A low requests a read of the SSI 73K212 internal registers. Data cannot be output unless both $\overline{\text{RD}}$ and the latched $\overline{\text{CS}}$ are active or low.

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{\text{WR}}$	13	-	I	Write. A low on this informs the SSI 73K212 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{\text{WR}}$. No data is written unless both $\overline{\text{WR}}$ and the latched $\overline{\text{CS}}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{\text{RD}}$ pin. $\overline{\text{RD}}$ low outputs data. $\overline{\text{RD}}$ high inputs data.
$\overline{\text{RD}}$	-	10	I	Read. A low on this input informs the SSI 73K212 that data or status information is being read by the processor. The falling edge of the $\overline{\text{RD}}$ signal will initiate a read from the addressed register. The $\overline{\text{RD}}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{\text{RD}}$ signal is active.
$\overline{\text{WR}}$	-	9	I	Write. A low on this input informs the SSI 73K212 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{\text{WR}}$ low. Data is written on the rising edge of $\overline{\text{WR}}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{\text{CS}}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ controls are used differently.

The Serial Control mode is provided in the parallel control versions by tying ALE high and $\overline{\text{CS}}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200 bit/s +1%, -2.5%.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. Consult crystal manufacturer for proper valves. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. In parallel mode the address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K212 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1	DTMF0
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000			TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
				0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1	DTMF0
		RXD PIN 0=NORMAL 1=TRI STATE		0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			
ID REGISTER 10	110	ID	ID	ID	ID				

00XX=73K212, 322, 321
01XX=73K221, 302
10XX=73K222
1100=73K224
1110=73K324
1101=73K312

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	▨	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit	0	Disables transmit output at TXA.
	Enable	1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
		D5 D4 D3 D2	
D5, D4,D3, D2	Transmit Mode	0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 stop or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used, must be written as "0."

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
		D1 D0	
D1, D0	Test Mode	0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrier at the TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency on reset.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4	Bypass Scrambler	0	Selects normal operation. DPSK transmit data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{\text{INT}}$ pin.
		1	Enables $\overline{\text{INT}}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
		D7 D6	
D7, D6	Transmit Pattern	0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	LONG LOOP	0	Indicates normal received signal.
		1	Indicates low received signal.
D1	CALL PROGRESS DETECT	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.
D2	ANSWER TONE DETECT	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone. The device must be in originate mode for detection of answer tone.
D3	CARRIER DETECT	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	UNSCRAMBLED MARK	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	RECEIVE DATA		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	▨	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW	TONES HIGH
1	0 0 0 1	697	1209
2	0 0 1 0	697	1336
3	0 0 1 1	697	1477
4	0 1 0 0	770	1209
5	0 1 0 1	770	1336
6	0 1 1 0	770	1477
7	0 1 1 1	852	1209
8	1 0 0 0	852	1336
9	1 0 0 1	852	1477
0	1 0 1 0	941	1336
*	1 0 1 1	941	1209
#	1 1 0 0	941	1477
A	1 1 0 1	697	1633
B	1 1 1 0	770	1633
C	1 1 1 1	852	1633
D	0 0 0 0	941	1633

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.		TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	TRANSMIT DTMF	0	Disable DTMF.
		1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high (with Transmit Enable, CR0-D1). TX DTMF overrides all other transmit functions.
D5	TRANSMIT ANSWER TONE	0	Disables answer tone generator.
		1	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.
D7	RXD OUTPUT CONTROL	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal, weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID	ID			

BIT NO.	NAME	CONDITION				DESCRIPTION
		D7	D6	D5	D4	Indicates Device:
D7, D6, D5 D4	Device Identification Signature	0	0	X	X	SSI 73K212(L), 73K321L or 73K322L or 73K321L
		0	1	X	X	SSI 73K221(L) or 73K302L
		1	0	X	X	SSI 73K222(L)
		1	1	0	0	SSI 73K224L
		1	1	1	0	SSI 73K324L
		1	1	0	1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD + 0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(External to GND)	0.1			µF
VDD Bypass capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics; from pin to GND			40	pF
XTL2 Load Capacitor				20	

ELECTRICAL SPECIFICATIONS (Continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 kHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX=1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATION (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to + 85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10.0	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low-Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High-Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, DPSK mode	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
10 dB loss in the Transmit path to the line.
9 dB gain in the Receive path from the line.
5V Version
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATION (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	In FSK mode	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
TXA pin Output Impedance			200	300	Ω
Output load	TXA pin; FSK Single Tone out for THD = -50 db in .3 to 3.4 KHz	10		 50	kΩ pF
Spurious Freq. Comp.	Frequency = 76.8 KHz			-39	dBm0
	Frequency = 153.6 KHz			-45	dBm0
Clock Noise	TXA pin; 76.8 KHz				
5V Version (73K212L)				1.0	mVrms
12V Version (73K212)				2.0	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATION (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

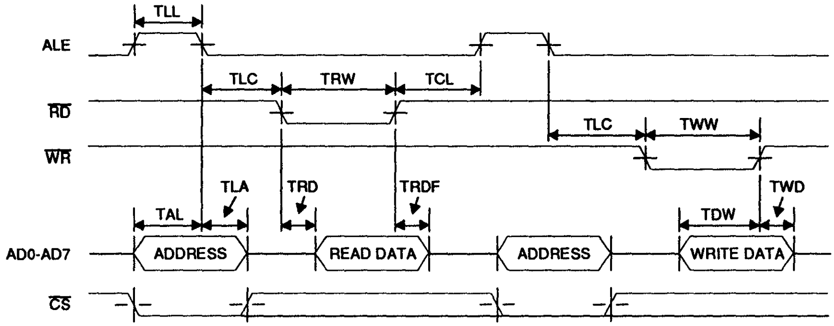
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{\text{CS}}$/Addr. setup before ALE low	30			ns
TLA	$\overline{\text{CS}}$/Addr. hold after ALE low	20			ns
TLC	ALE low to $\overline{\text{RD}}$/$\overline{\text{WR}}$ low	40			ns
TCL	$\overline{\text{RD}}$/$\overline{\text{WR}}$ Control to ALE high	10			ns
TRD	Data out from $\overline{\text{RD}}$ low	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{\text{RD}}$ high	0		80	ns
TRW	$\overline{\text{RD}}$ width	200		25000	ns
TWW	$\overline{\text{WR}}$ width	140		25000*	ns
TDW	Data setup before $\overline{\text{WR}}$ high	150			ns
TWD	Data hold after $\overline{\text{WR}}$ high	20			ns
TCKD	Data out after EXCLK low			200	ns
TCKW	$\overline{\text{WR}}$ after EXCLK low	150			ns
TDCK	Data setup before EXCLK low	150			ns
TAC	Address setup before control**	50			ns
TCA	Address hold after control**	50			ns
TWH	Data Hold after EXCLK	20			ns

* Maximum time applies to parallel version only.

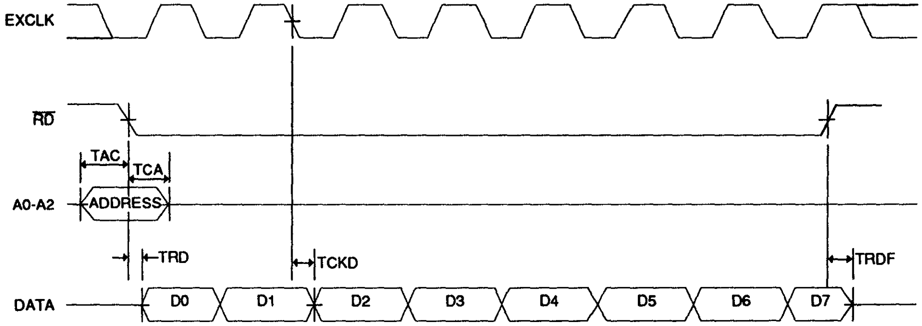
** Control for setup is the falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$.
Control for hold is the falling edge of $\overline{\text{RD}}$ or the rising edge of $\overline{\text{WR}}$.

TIMING DIAGRAMS

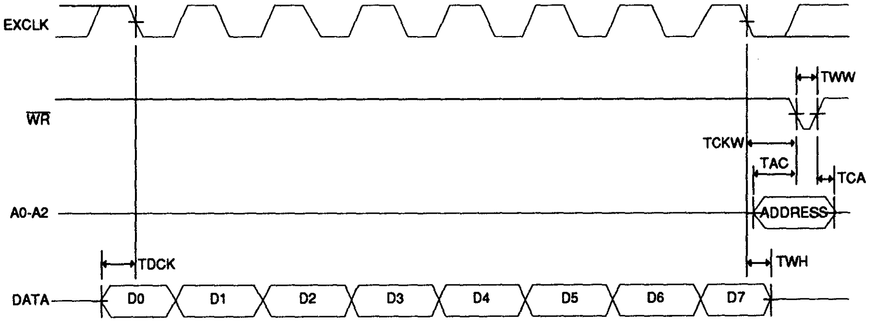
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



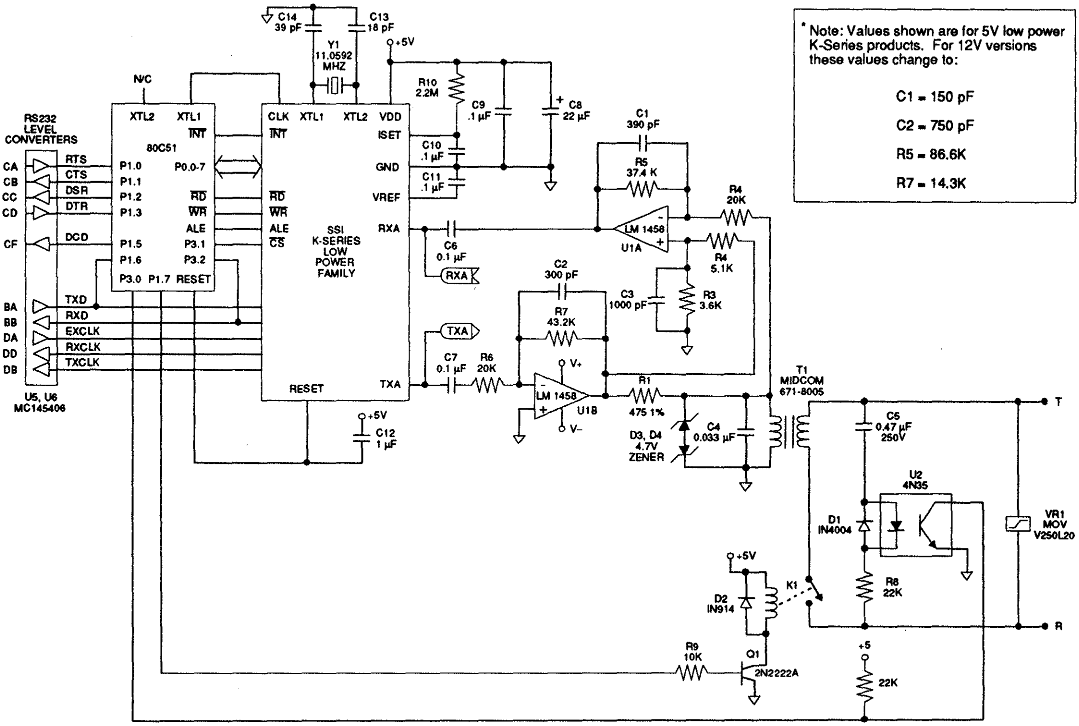
APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.



* Note: Values shown are for 5V low power K-Series products. For 12V versions these values change to:

C1 = 150 pF
C2 = 750 pF
R5 = 86.6K
R7 = 14.3K

FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

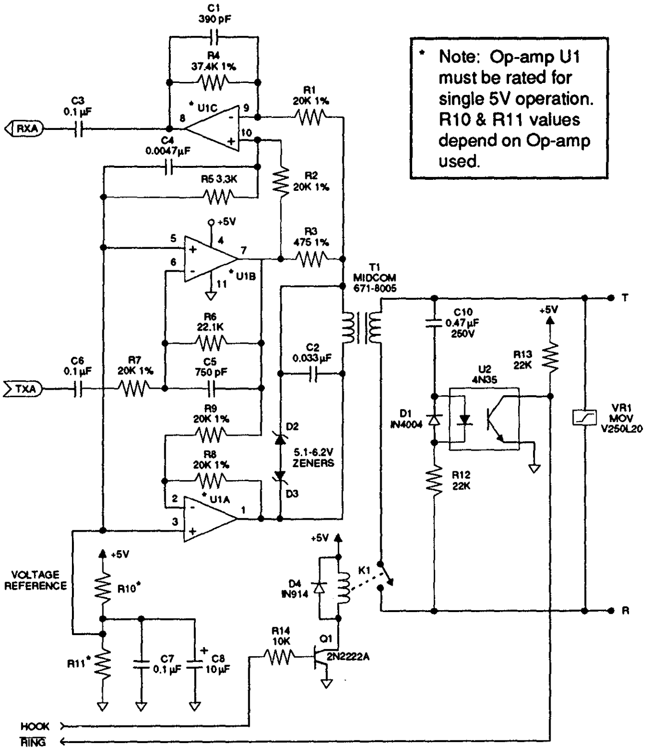
DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K-Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

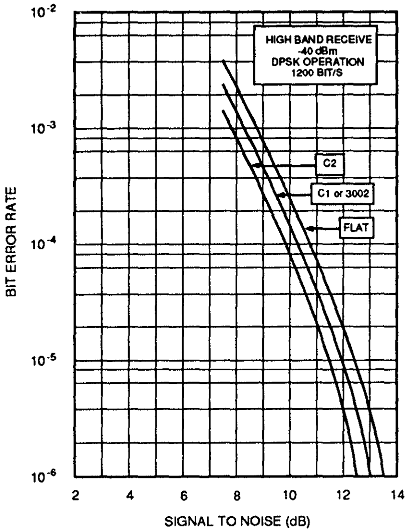
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

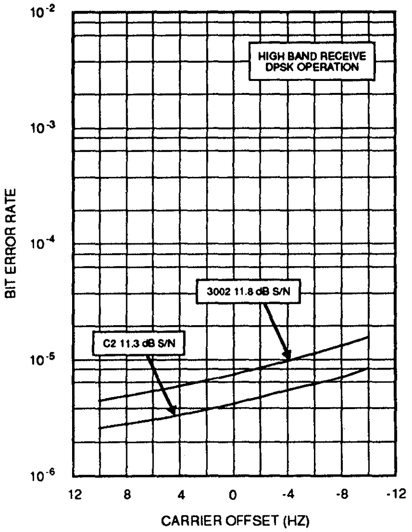
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

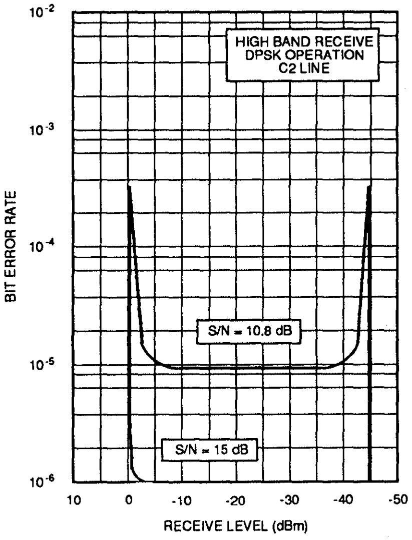
**SSI 73K212, 73K212L
BER vs SIGNAL TO NOISE**



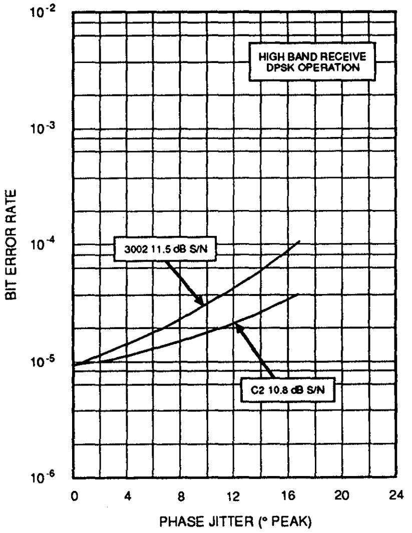
**SSI 73K212, 73K212L
BER vs CARRIER OFFSET**



***SSI 73K212, 73K212L
BER vs RECEIVE LEVEL**



***SSI 73K212, 73K212L
BER vs PHASE JITTER**

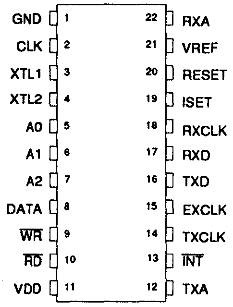


* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

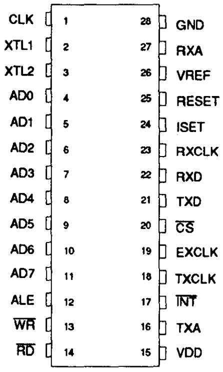
SSI 73K212/K212L
Bell 212A/103
Single-Chip Modem

PACKAGE PIN DESIGNATIONS

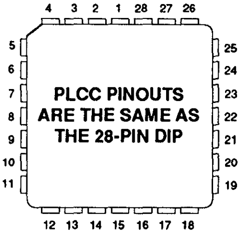
(Top View)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Pin
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K212 with Parallel Bus Interface		
28-pin 12V supply		
Plastic Dual-In-Line	73K212 – IP	73K212 – IP
Plastic Leaded Chip Carrier	73K212 – IH	73K212 – IH
28-pin 5V supply		
Plastic Dual-In-Line	73K212L – IP	73K212L – IP
Plastic Leaded Chip Carrier	73K212L – IH	73K212L – IH
SSI 73K212 with Serial Interface		
22-pin 12V supply		
Plastic Dual-In-Line	73K212S – IP	73K212S – IP
22-pin 5V supply		
Plastic Dual-In-Line	73K212SL – IP	73K212SL – IP
Ceramic Dual-In-Line	73K212SL – IC	73K212SL – IC

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

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A TDK Group Company

SSI 73K221/K221L
CCITT V.22, V.21
Single-Chip Modem

December 1992

DESCRIPTION

The SSI 73K221 is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation over dial-up lines. The SSI 73K221 is an enhancement of the SSI 73K212 single-chip modem with performance characteristics suitable for European and Asian telephone systems. The SSI 73K221 produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows V.21 for 300 Hz FSK operation. The SSI 73K221 integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K221L, low power version of the SSI 73K221 provides identical performance and features, but operates from a single +5 volt supply with substantially lower power consumption.

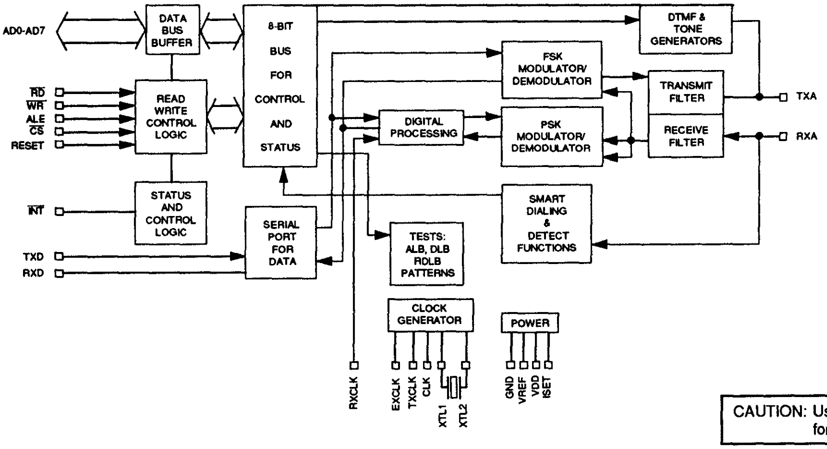
The SSI 73K221 includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer and 550 or 1800 Hz guard tone. This device supports V.22 (except mode v) and V. 21 modes of operation,

(Continued)

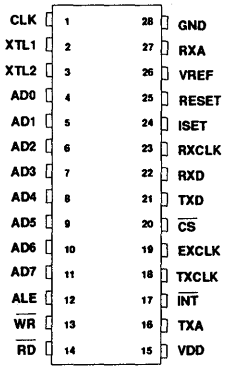
FEATURES

- **One-chip CCITT V.22 and V.21 standard compatible modem data pump**
- **Full-duplex Operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel (28-pin DIP) microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2100 Hz), and long loop detectors**
- **DTMF, and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **Space efficient 22- or 28-pin DIP packages**
- **CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V**
- **Single +5 volt (73K221L) or +12 volt (73K221) versions**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

allowing both synchronous and asynchronous communications. The SSI 73K221 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or alternatively via the serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K221 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K221 is part of Silicon Systems' K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion, The SSI 73K221 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC rate converter. The ASYNC/SYNC rate converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, - 2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± .01%.

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC rate converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC rate converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNC/SYNC converter is bypassed when synchronous mode is selected and data is transmitted at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K221 modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K221 uses a phase locked loop coherent demodulation technique for optimum performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the V.21 mode.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, optionselect and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K221 control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out the remaining seven bits of the selected address LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the addressed register on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark signal is also detected when the received data out of the DPSK demodulator before the descrambler has been mark for 165.5 ms ± 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all conditions except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (or 5V ±10%). Bypass with .1 and 22 µF capacitors to ground.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{\text{CS}}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal control registers.
$\overline{\text{CS}}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{\text{CS}}$ (latched) is not active. The state $\overline{\text{CS}}$ is a latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{\text{INT}}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{\text{INT}}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{\text{RD}}$	14	-	I	Read. A low requests a read of the SSI 73K221 internal registers. Data cannot be output unless both $\overline{\text{RD}}$ and the latched $\overline{\text{CS}}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{\text{WR}}$	13	-	I	Write. A low on this pin informs the SSI 73K221 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{\text{WR}}$. No data is written unless both $\overline{\text{WR}}$ and the latched $\overline{\text{CS}}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{\text{RD}}$ pin. $\overline{\text{RD}}$ low outputs data. $\overline{\text{RD}}$ high inputs data.
$\overline{\text{RD}}$	-	10	I	Read. A low on this input informs the SSI 73K221 that data or status information is being read by the processor. The falling edge of the $\overline{\text{RD}}$ signal will initiate a read from the addressed register. The $\overline{\text{RD}}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{\text{RD}}$ signal is active.
$\overline{\text{WR}}$	-	9	I	Write. A low on this input informs the SSI 73K221 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{\text{WR}}$ low. Data is written on the rising edge of $\overline{\text{WR}}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{\text{CS}}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ controls are used differently.

The Serial Control mode is provided in the parallel control versions by tying ALE high and $\overline{\text{CS}}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to the TXD pin. Alternately used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data at RXD. RXCLK will be valid as long as a carrier is present in DPSK synchronous modes.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in DPSK synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied to this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring an 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. In parallel mode AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K221 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output driver used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	▨	▨	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			0=1800 Hz G.T. 1=550 Hz G.T.
ID REGISTER 10	110	ID	ID	ID	ID	▨	▨	▨	▨

00XX=73K212, 322, 321
01XX=73K221, 302
10XX=73K222
1100=73K224
1110=73K324
1101=73K312

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit	0	Disables transmit output at TXA.
	Enable	1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to allow Answer Tone and DTMF transmission.
		D5 D4 D3 D2	
D5, D4,D3, D2	Transmit Mode	0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 stop bit).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a "0."

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	DPSK mode at 1200 bit/s.
		1 0 X	DPSK mode at 600 bit/s. X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{\text{INT}}$ pin.
		1	Enables $\overline{\text{INT}}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as determined by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Detect	0	No answer tone detected.
		1	Indicates detection of 2100 Hz answer tone. The device must be in originate mode for detection of answer tone.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the received channel.
D4	Unscrambled Mark	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. This may be used in the V.22 connect sequence or for requesting a remote modem to configure itself for remote digital loopback. A valid indication means that unscrambled marks have been received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Guard Tone	D6 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X 1 X	Transmit DTMF tones.
		X 0 0	Transmits 1800 Hz guard tone.
		X 0 1	Transmits 550 Hz guard tone.
D1	DTMF 1/	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 or 600 bit/s +1.0% - 2.5%
		0 1	Asynchronous DPSK 1200 or 600 bit/s +2.3% -2.5%.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

<table>
<tr><th>BIT NO.</th><th>NAME</th><th>CONDITION</th><th>DESCRIPTION</th></tr>
<tr><td>D3, D2, D1, D0</td><td>DTMF 3, 2, 1, 0</td><td>D3 D2 D1 D0
0 0 0 0 -
1 1 1 1</td><td>Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:
<table>
<tr><th>KEYBOARD EQUIVALENT</th><th colspan="4">DTMF CODE</th><th colspan="2">TONES</th></tr>
<tr><th></th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>LOW</th><th>HIGH</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>697</td><td>1209</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>697</td><td>1336</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>697</td><td>1477</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>770</td><td>1209</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td><td>770</td><td>1336</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td><td>770</td><td>1477</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td><td>852</td><td>1209</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>852</td><td>1336</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td><td>852</td><td>1477</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>941</td><td>1336</td></tr>
<tr><td>*</td><td>1</td><td>0</td><td>1</td><td>1</td><td>941</td><td>1209</td></tr>
<tr><td>#</td><td>1</td><td>1</td><td>0</td><td>0</td><td>941</td><td>1477</td></tr>
<tr><td>A</td><td>1</td><td>1</td><td>0</td><td>1</td><td>697</td><td>1633</td></tr>
<tr><td>B</td><td>1</td><td>1</td><td>1</td><td>0</td><td>770</td><td>1633</td></tr>
<tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>852</td><td>1633</td></tr>
<tr><td>D</td><td>0</td><td>0</td><td>0</td><td>0</td><td>941</td><td>1633</td></tr>
</table></td></tr>
<tr><td rowspan="2">D4</td><td rowspan="2">Transmit DTMF</td><td>0</td><td>Disable DTMF.</td></tr>
<tr><td>1</td><td>Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions. Modem must be in DPSK mode during DTMF transmission.</td></tr>
<tr><td rowspan="2">D5</td><td rowspan="2">Transmit Answer Tone</td><td>0</td><td>Disables answer tone generator.</td></tr>
<tr><td>1</td><td>Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.</td></tr>
</table>

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	TX Guard	0	Disables guard tone generator.
	(Transmit Guard Tone)	1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin becomes a high impedance with internal weak pull-up resistor.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID	▨	▨	▨	▨

BIT NO.	NAME	CONDITION	DESCRIPTION
		D7 D6 D5 D4	Indicates Device:
D7, D6, D5 D4	Device Identification Signature	0 0 X X	SSI 73K212(L), 73K321L or 73K322L or 73K321L
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L) or 73K321L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics; from pin to GND			40	pF
XTL2 Load Capacitor				20	

ELECTRICAL SPECIFICATIONS (Continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator (Modem must be in DPSK mode to meet specifications)					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Group, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Group, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Group to Low-Group	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
10 dB loss in the Transmit path to the line.
9 dB gain in the Receive path from the line.
5V Version
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	Not in V.21 mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 db in .3 to 3.4 KHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 kHz			-39	dBm0
	Frequency = 153.6 kHz			-45	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin; 76.8 kHz				
5V Version (73K221L)				1.0	mVrms
12V Version (73K221)				2	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change		40	100	ms
Recovered Clock					
Capture Range		-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

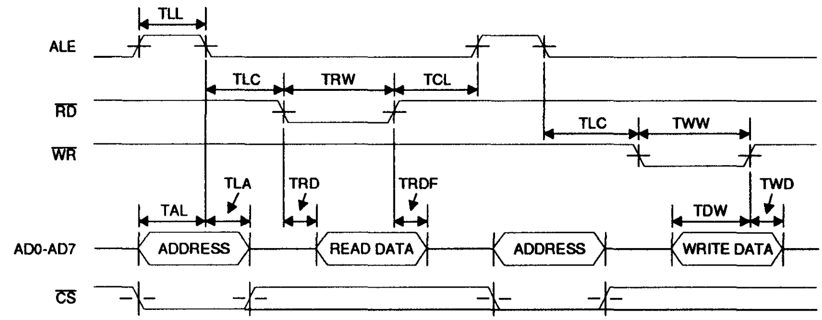
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{\text{CS}}$/Addr. setup before ALE low	30			ns
TLA	$\overline{\text{CS}}$/Addr. hold after ALE low	20			ns
TLC	ALE low to $\overline{\text{RD}}$/$\overline{\text{WR}}$ low	40			ns
TCL	$\overline{\text{RD}}$/$\overline{\text{WR}}$ Control to ALE high	10			ns
TRD	Data out from $\overline{\text{RD}}$ low	0		160	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{\text{RD}}$ high	0		80	ns
TRW	$\overline{\text{RD}}$ width	200		25000	ns
TWW	$\overline{\text{WR}}$ width	140		25000*	ns
TDW	Data setup before $\overline{\text{WR}}$ high	150			ns
TWD	Data hold after $\overline{\text{WR}}$ high	20			ns
TCKD	Data out after EXCLK low			200	ns
TCKW	$\overline{\text{WR}}$ after EXCLK low	150			ns
TDCK	Data setup before EXCLK low	150			ns
TAC	Address setup before control**	50			ns
TCA	Address hold after control**	50			ns
TWH	Data hold after EXCLK	150			ns

* Maximum time applies to parallel version only.

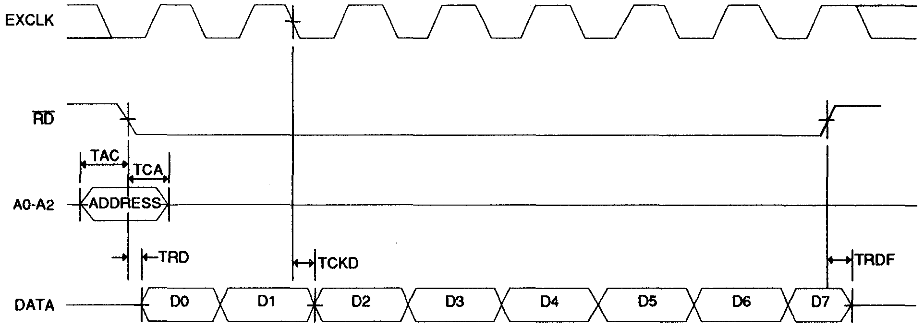
** Control for setup is the falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$.
Control for hold is the falling edge of $\overline{\text{RD}}$ or the rising edge of $\overline{\text{WR}}$.

TIMING DIAGRAMS

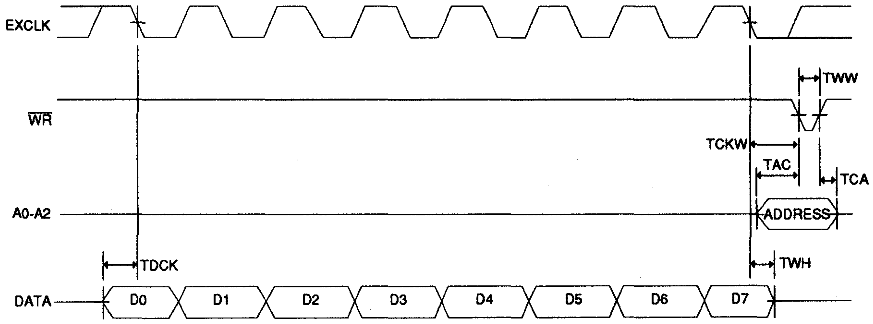
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



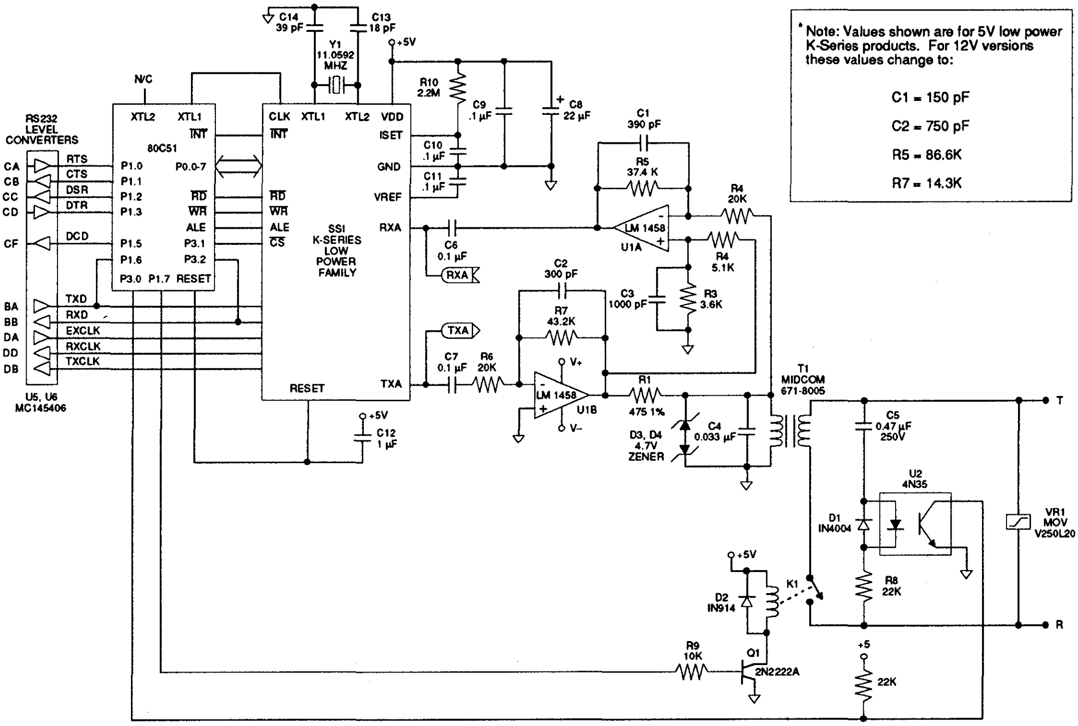
APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.



* Note: Values shown are for 5V low power K-Series products. For 12V versions these values change to:

C1 = 150 pF
C2 = 750 pF
R5 = 86.6K
R7 = 14.3K

FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

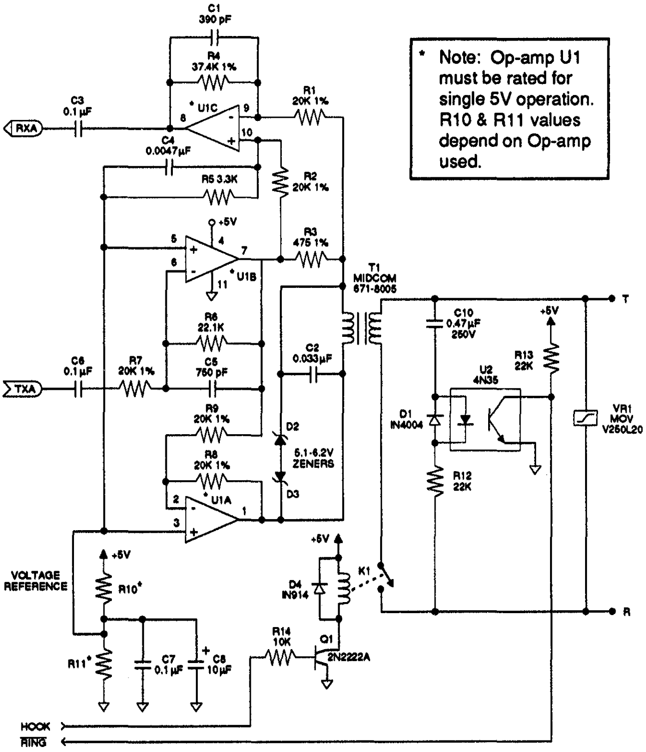
DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 μF electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

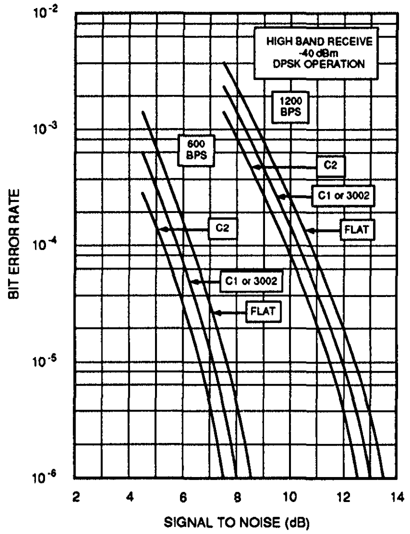
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

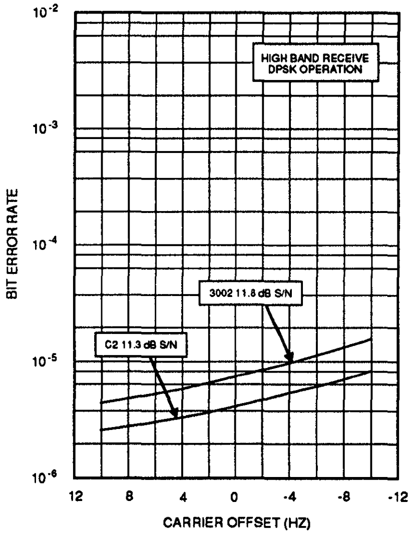
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

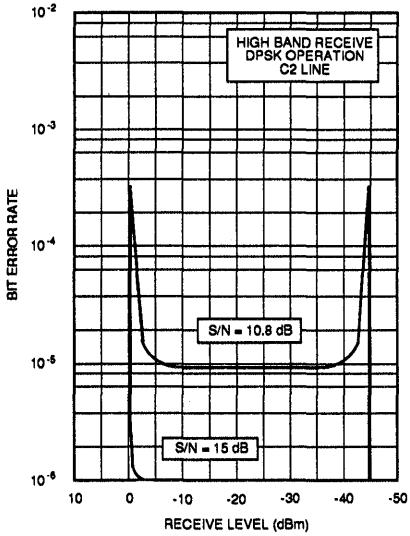
***SSI 73K221, 73K221L**
BER vs SIGNAL TO NOISE



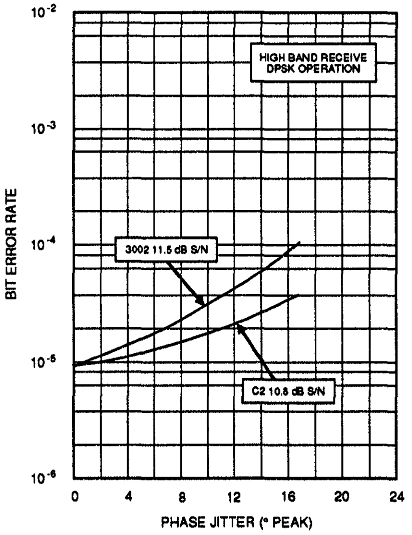
***SSI 73K221, 73K221L**
BER vs CARRIER OFFSET



***SSI 73K221, 73K221L**
BER vs RECEIVE LEVEL



***SSI 73K221, 73K221L**
BER vs PHASE JITTER

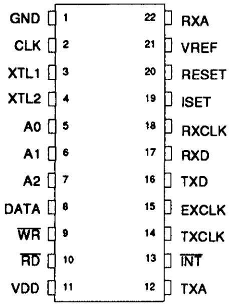


* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

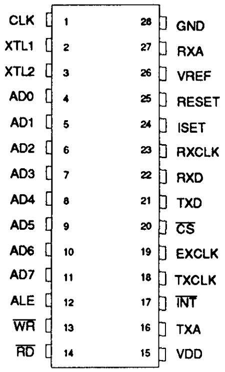
SSI 73K221/K221L
CCITT V.22, V.21
Single-Chip Modem

PACKAGE PIN DESIGNATIONS

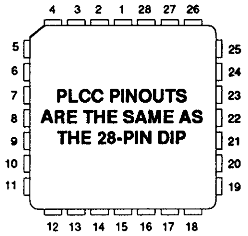
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Pin
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K221 with Parallel Bus Interface		
28-pin 12 volt supply		
Plastic Dual-In-Line	73K221 – IP	73K221 – IP
Plastic Leaded Chip Carrier	73K221 – IH	73K221 – IH
28-pin 5 volt supply		
Plastic Dual-In-Line	73K221L – IP	73K221L – IP
Plastic Leaded Chip Carrier	73K221L – IH	73K221L – IH
SSI 73K212 with Serial Interface		
22-pin 12 volt supply		
Plastic Dual-In-Line	73K221S – IP	73K221S – IP
22-pin 5 volt supply		
Plastic Dual-In-Line	73K221SL – IP	73K221SL – IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714)573-6000, FAX: (714) 573-6914

1292 - rev.

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Notes:

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SSI 73K222/K222L
V.22, V.21, Bell 212A Single-Chip Modem

December 1992

DESCRIPTION

The SSI 73K222 is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.22, V.21 and Bell 212A compatible modem, capable of 1200 bit/s full–duplex operation over dial-up lines. The SSI 73K222 is an enhancement of the SSI 73K212 single-chip modem which adds V.22 and V.21 modes to the Bell 212A and 103 operation of the SSI 73K212. In Bell 212A mode, the SSI 73K222 provides the normal Bell 212A and 103 functions and employs a 2225 Hz answer tone. The SSI 73K222 in V.22 mode produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and allows 600 bit/s V.22 or 0-300 bit/s V.21 operation. The SSI 73K222 integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K222L, low power version of the SSI 73K222 provides identical performance and features, but operates from a single +5V supply with substantially lower power consumption.

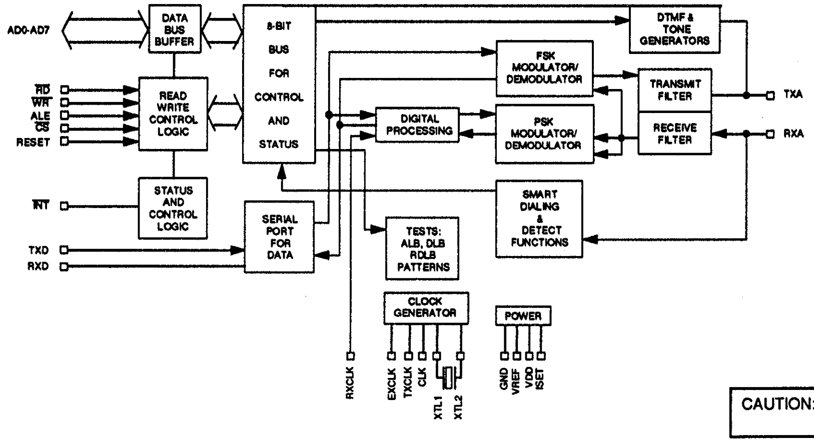
The SSI 73K222 includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor and a tone generator capable of

(Continued)

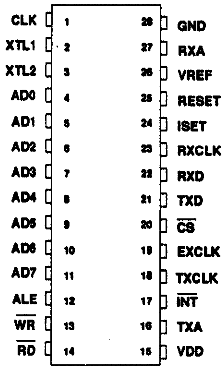
FEATURES

- **One-chip CCITT V.22, V.21, Bell 212A and 103 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK)**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation including V.22 extended overspeed**
- **Call progress, carrier, precise answer tone (2100 or 2225 Hz), and long loop detectors**
- **DTMF, and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 30 mW @ 5V or 180 mW @ 12V**
- **Single +5 volt (73K222L) or +12 volt (73K222) versions**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

tone required for European applications. This device supports V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and asynchronous communications. Test features such as analog loop, digital loop, and remote digital loopback are supported. Internal pattern generators are also included for self-testing. The SSI 73K222 is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K222 is ideal for use in either free standing or integral system modem products where full-duplex 1200 bit/s data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K222 is part of Silicon Systems' K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K222 includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data within a ±0.01% rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± 0.01% (± 0.01% is required synchronous data rate accuracy).

The serial data stream from the ASYNC/SYNC converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. The ASYNC/SYNC converter and the data scrambler are bypassed in all FSK modes. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The SYNC/ASYNC convertor will reinsert any deleted stop bits and transmit output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. The Bell 212A standard defines synchronous operation only at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

The SSI 73K222 modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K222 uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space) are used. V.21 mode uses 980 and 1180 Hz (originate, mark and space), or 1650 and 1850Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are bypassed in the 103 or V.21 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K222 control and status registers via a serial command port (22-pin version only). In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the addressed register occurs on the rising edge of $\overline{WR}$. This interface mode is also supported in the 28-pin packages. See serial control interface pin description.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone and weak received signal (long loop condition). An unscrambled mark request signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 ms ± 6.5 ms minimum. The appropriate detect register bit is set when one of these conditions changes and an interrupt is generated for all purposes except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 12V +10%, -20% (73K222) or 5V±10% (73K222L). Bypass with .1 and 22 μF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 μF capacitor to ground.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 μF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K222 internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{\text{WR}}$	13	-	I	Write. A low on this informs the SSI 73K222 that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{\text{WR}}$. No data is written unless both $\overline{\text{WR}}$ and the latched $\overline{\text{CS}}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{\text{RD}}$ pin. $\overline{\text{RD}}$ low outputs data. $\overline{\text{RD}}$ high inputs data.
$\overline{\text{RD}}$	-	10	I	Read. A low on this input informs the SSI 73K222 that data or status information is being read by the processor. The falling edge of the $\overline{\text{RD}}$ signal will initiate a read from the addressed register. The $\overline{\text{RD}}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{\text{RD}}$ signal is active.
$\overline{\text{WR}}$	-	9	I	Write. A low on this input informs the SSI 73K222 that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{\text{WR}}$ low. Data is written on the rising edge of $\overline{\text{WR}}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{\text{CS}}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ controls are used differently.

The serial control mode is provided in the parallel control versions by tying ALE high and $\overline{\text{CS}}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

DTE USER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data applied to on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Load capacitors should be connected from XTL1 and XTL2 to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. In parallel mode the address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K222 internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANS TONE
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK 0=BELL 103 FSK 1=V.21 FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	▨	▨	RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	ANSWER TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER/ TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.			0=2225 Hz A.T. 1800 Hz G.T. 1=2100 Hz A.T. 500 Hz G.T.
ID REGISTER 10	110	ID	ID	ID	ID	▨	▨	▨	▨
00XX=73K212, 322, 321 01XX=73K221, 302 10XX=73K222 1100=73K224 1110=73K324 1101=73K312									

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band, receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA. Note: TX Enable must be set to 1 to allow Answer Tone and DTMF Transmiission.
		D5 D4 D3 D2	
D5,D4,D3, D2	Transmit Mode	0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects PSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects PSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects PSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects PSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.
D6		0	Not used; must be written as a "0."

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
		D7 D5 D4	Selects:
D7	Modulation Option	0 0 X	DPSK mode at 1200 bit/s.
		1 0 X	DPSK mode at 600 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK CCITT V.21 mode.
			X = Don't care

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
		D1 D0	
D1, D0	Test Mode	0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK data is routed around scrambler in the transmit path.
D5	Enable Detect	0	Disables interrupt at $\overline{\text{INT}}$ pin.
		1	Enables $\overline{\text{INT}}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the 350 to 620 Hz call progress band.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	ANSWER TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Detect	0	No answer tone detected.
		1	Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in originate mode for detection of answer tone. For CCITT answer tone detection, bit D0 of the Tone Register must be set to a 1.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicates carrier has been detected in the receive channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 0 0 0	Detects 2225 Hz in originate mode.
		X 1 0 0	Transmits 2225 Hz in answer mode (Bell).
		X 0 0 1	Detects 2100 Hz in originate mode.
		X 1 0 1	Transmits 2100 Hz in answer mode (CCITT).
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK +1.0% -2.5%.
		0 1	Asynchronous DPSK +2.3% -2.5%.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

<table>
<tr><th>BIT NO.</th><th>NAME</th><th>CONDITION</th><th>DESCRIPTION</th></tr>
<tr><td>D3, D2, D1, D0</td><td>DTMF 3, 2, 1, 0</td><td>D3 D2 D1 D0
0 0 0 0-
1 1 1 1</td><td>Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:
<table>
<tr><th>KEYBOARD EQUIVALENT</th><th>DTMF CODE
D3 D2 D1 D0</th><th>TONES
LOW HIGH</th></tr>
<tr><td>1</td><td>0 0 0 1</td><td>697 1209</td></tr>
<tr><td>2</td><td>0 0 1 0</td><td>697 1336</td></tr>
<tr><td>3</td><td>0 0 1 1</td><td>697 1477</td></tr>
<tr><td>4</td><td>0 1 0 0</td><td>770 1209</td></tr>
<tr><td>5</td><td>0 1 0 1</td><td>770 1336</td></tr>
<tr><td>6</td><td>0 1 1 0</td><td>770 1477</td></tr>
<tr><td>7</td><td>0 1 1 1</td><td>852 1209</td></tr>
<tr><td>8</td><td>1 0 0 0</td><td>852 1336</td></tr>
<tr><td>9</td><td>1 0 0 1</td><td>852 1477</td></tr>
<tr><td>0</td><td>1 0 1 0</td><td>941 1336</td></tr>
<tr><td>*</td><td>1 0 1 1</td><td>941 1209</td></tr>
<tr><td>#</td><td>1 1 0 0</td><td>941 1477</td></tr>
<tr><td>A</td><td>1 1 0 1</td><td>697 1633</td></tr>
<tr><td>B</td><td>1 1 1 0</td><td>770 1633</td></tr>
<tr><td>C</td><td>1 1 1 1</td><td>852 1633</td></tr>
<tr><td>D</td><td>0 0 0 0</td><td>941 1633</td></tr>
</table></td></tr>
<tr><td rowspan="2">D4</td><td rowspan="2">Transmit DTMF</td><td>0</td><td>Disable DTMF.</td></tr>
<tr><td>1</td><td>Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.</td></tr>
<tr><td rowspan="4">D5</td><td rowspan="4">Transmit Answer Tone</td><td>D5 D4 D0</td><td>D5 interacts with bits D4 and D0 as shown.</td></tr>
<tr><td>0 0 X</td><td>Disables answer tone generator.</td></tr>
<tr><td>1 0 0</td><td>Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the Transmit Enable bit is set in CR0. The device must be in answer mode.</td></tr>
<tr><td>1 0 1</td><td>Likewise a 2100 Hz answer tone will be transmitted.</td></tr>
</table>

TONE REGISTER (Continued)

TR 011	D7	D6	D5	D4	D3	D2	D1	D0
	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator (See D0 for selection of guard tones).
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

ID REGISTER

ID 110	D7	D6	D5	D4	D3	D2	D1	D0
	ID	ID	ID	ID				

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212(L), 73K321L or 73K322L or 73K321L
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

ELECTRICAL SPECIFICATIONS (Continued)

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
PSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	TX scrambled marks	-11	-10.0	-9	dBm0
FSK Mod/Demod					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10.0	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±8		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator					
Freq. Accuracy		-.25		+.25	%
Output Amplitude	Low Band, DPSK Mode	-10	-9	-8	dBm0
Output Amplitude	High Band, DPSK Mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, DPSK Mode	1.0	2.0	3.0	dB
Long Loop Detect	DPSK or FSK	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz band	-34		0	dBm0
Reject Level	2-Tones in 350-600 Hz band			-41	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	27		80	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	27		80	ms
Hysteresis		2			dB

Note: Parameters expressed in dBm0 refer to the following definition:

12V Version
10 dB loss in the Transmit path to the line.
9 dB gain in the Receive path from the line.
5V Version
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

ELECTRICAL SPECIFICATIONS (Continued)

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect	DPSK or FSK				
Threshold	receive data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	15		45	ms
Hysteresis	Single tone detected	2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		24	ms
Answer Tone Detector					
Detect Level	Not in V.21 mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Freq. Range		-2.5		+2.5	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 db in .3 to 3.4 KHz			50	pF
Spurious Freq. Comp.	Frequency = 76.8 kHz			-39	dBm0
	Frequency = 153.6 kHz			-45	dBm0
TXA pin Output Impedance			200	300	Ω
Clock Noise	TXA pin; 76.8 KHz				
5V Version (73K222L)				1.0	mVrms
12V Version (73K222)				2.0	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

ELECTRICAL SPECIFICATIONS (Continued)

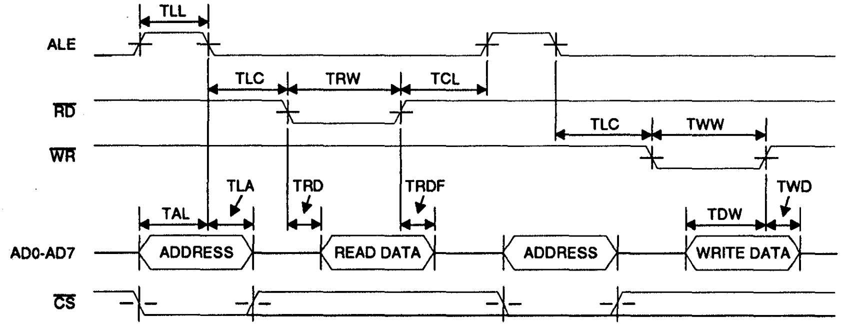
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 Hz				
	1800 Hz	-20		+20	Hz
Tone Level	550 Hz	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion	550 Hz			-50	dB
700 to 2900 Hz	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	60			ns
TRDF	Data float after $\overline{RD}$ High	0		200	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	150			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

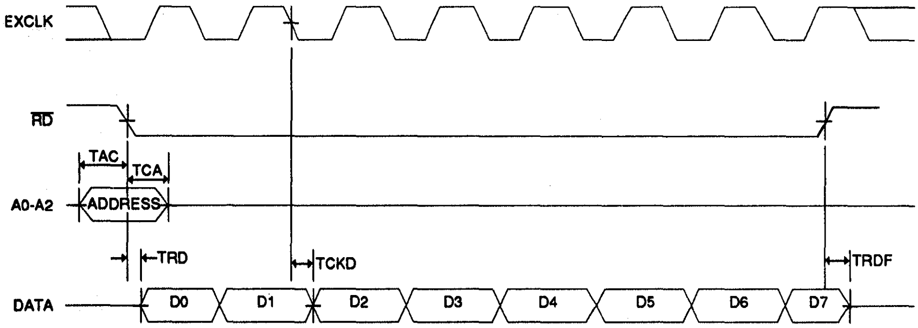
* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

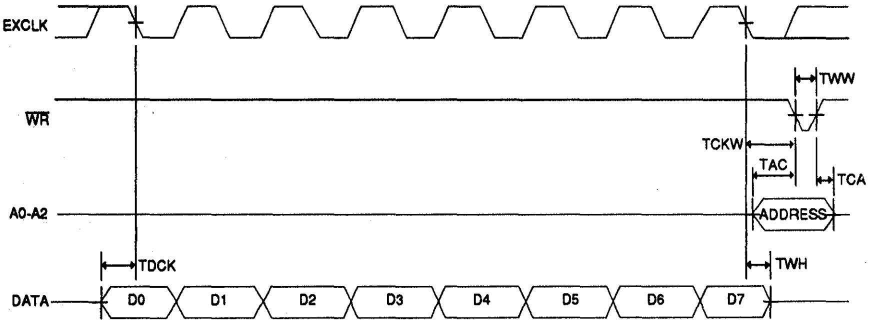
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



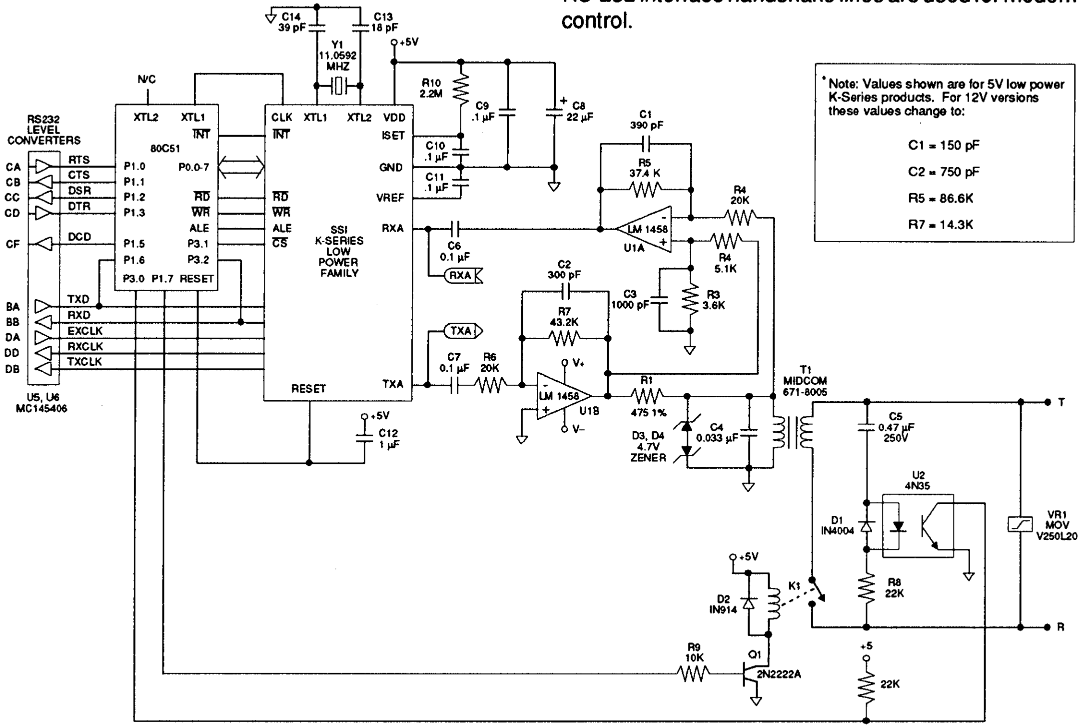
APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.



*Note: Values shown are for 5V low power K-Series products. For 12V versions these values change to:

C1 = 150 pF
C2 = 750 pF
R5 = 86.6K
R7 = 14.3K

FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

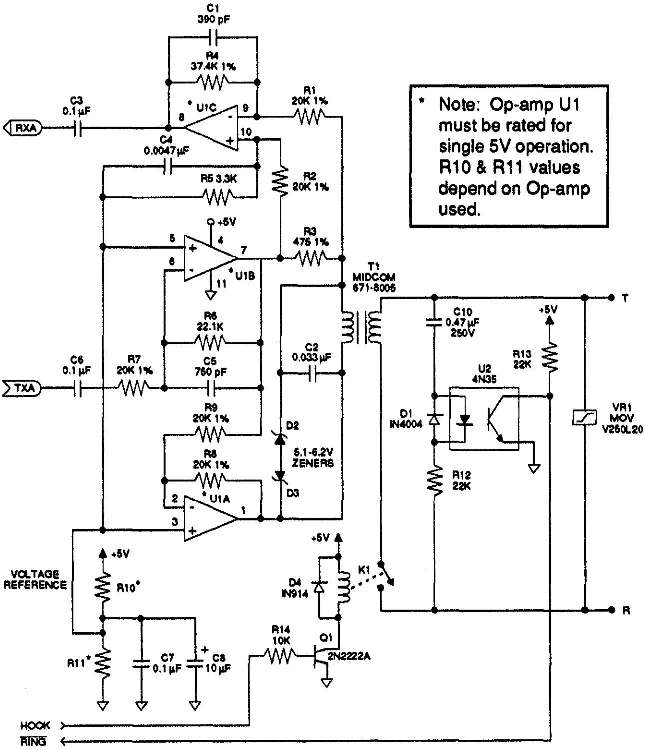
DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

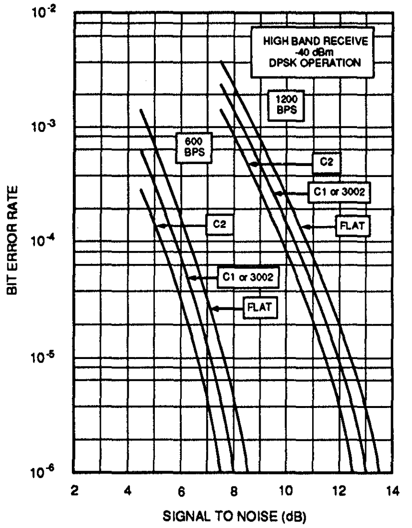
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

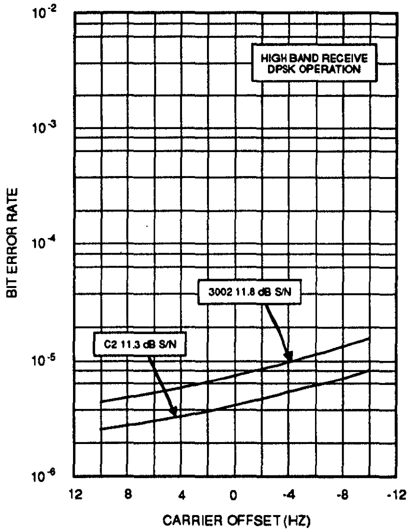
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

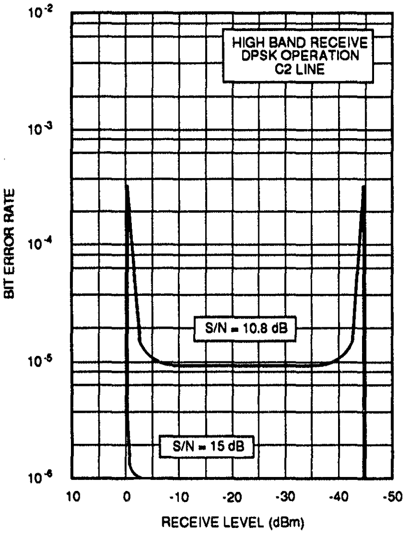
***SSI 73K222, 73K222L
BER vs SIGNALTO NOISE**



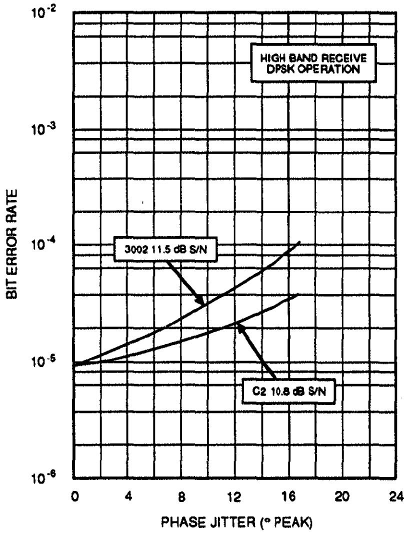
***SSI 73K222, 73K222L
BER vs CARRIER OFFSET**



***SSI 73K222, 73K222L
BER vs RECEIVE LEVEL**



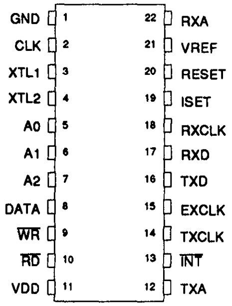
***SSI 73K222, 73K222L
BER vs PHASE JITTER**



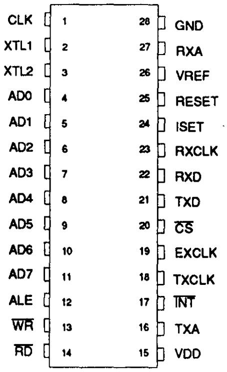
* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

SSI 73K222/K222L
V.22, V.21, Bell 212A
Single-Chip Modem

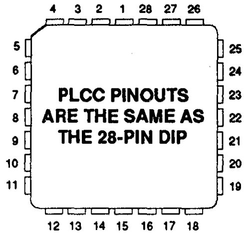
PACKAGE PIN DESIGNATIONS
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Pin
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K222 with Parallel Bus Interface		
28-Pin 12V Supply		
Plastic Dual-In-Line	73K222-IP	73K222-IP
Plastic Leaded Chip Carrier	73K222-IH	73K222-IH
28-Pin 5V Supply		
Plastic Dual-In-Line	73K222L-IP	73K222L-IP
Plastic Leaded Chip Carrier	73K222L-IH	73K222L-IH
SSI 73K222 with Serial Interface		
22-Pin 12V Supply		
Plastic Dual-In-Line	73K222S-IP	73K222S-IP
22-Pin 5V Supply		
Plastic Dual-In-Line	73K222SL-IP	73K222SL-IP
Ceramic Dual-In-Line	73K222SL-IC	73K222SL-IC

Protected by the following Patents (4,691,172) (4,777,453)

Notes:

Silicon Systems®
A TDK Group Company

SSI 73K222U
Single-Chip Modem with UART

December 1992

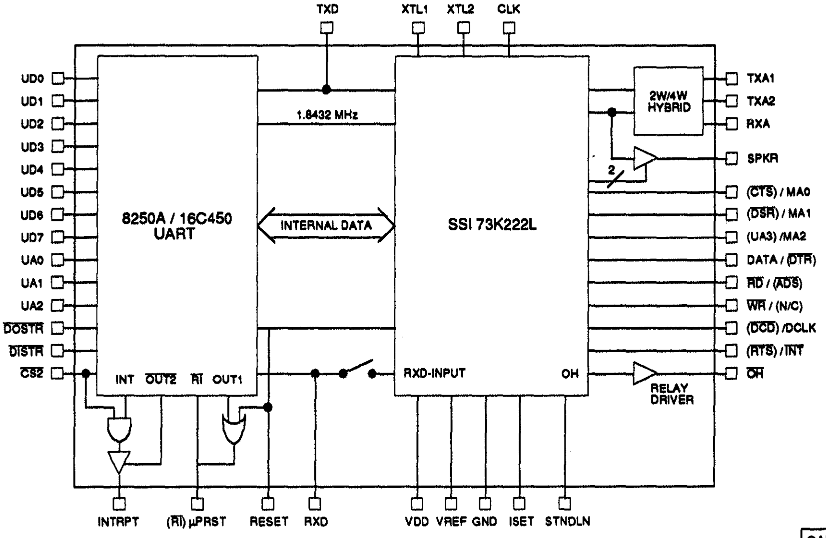
DESCRIPTION

The SSI 73K222U is a compact, high-performance modem which includes a 8250A/16C450 compatible UART with the 1200 bit/s modem function on a single chip. Based on the SSI 73K222L 5V low power CMOS modem IC, the SSI 73K222U is the perfect modem/UART component for integral modem applications. It is ideal for applications such as portable terminals and laptop computers. The SSI 73K222U is the first fully featured modem IC which can function as an intelligent modem in integral applications without requiring a separate dedicated microcontroller. It provides for data communication at 1200, 600, and 300 bit/s in a multi-mode manner that allows operation compatible with both Bell 212A/103 and CCITT V.22/V.21 standards. The digital interface section contains a high speed version of the industry standard 8250A/16C450 UART, commonly used in personal computer products. A unique feature of the SSI 73K222U is that the UART section can be used without the modem function, providing an additional asynchronous port at no added cost. The SSI 73K222U is designed in CMOS technology and operates from a single +5V supply. Available packaging includes 40-pin DIP or 44-pin PLCC for surface mount applications.

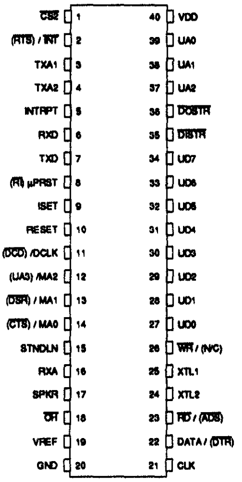
FEATURES

- **Modem/UART combination optimized for integral bus applications**
- **Includes features of SSI 73K222L single-chip modem**
- **Fully compatible 16C450/8250 UART with 8250B or 8250A selectable interrupt emulation**
- **High speed UART will interface directly with high clock rate bus with no wait states**
- **Single-port mode allows full modem and UART control from CPU bus, with no dedicated microprocessor required**
- **Dual-port mode suits conventional designs using local microprocessor for transparent modem operation**
- **Complete modem functions for 1200 bit/s (Bell 212A, V.22) and 0-300 bit/s (Bell 103, V.21)**
- **Includes DTMF generator, carrier, call-progress and precise answer-tone detectors for intelligent dialing capability**
- **On chip 2-wire/4-wire hybrid driver and off-hook relay buffer**
- **Speaker output with four-level software driven volume control**
- **Low power CMOS (40 mW) with power down mode (15 mW)**
- **Operates from single +5V supply**

BLOCK DIAGRAM



PIN DIAGRAM



Parentheses indicate single-port mode.

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73K222U
Single-Chip Modem with UART

FUNCTIONAL DESCRIPTION

The SSI 73K222U integrates an industry standard 8250/16C450 UART function with the modem capability provided by the SSI 73K222L single chip modem IC. The SSI 73K222U is designed specifically for integral microprocessor bus intelligent modem products. These designs typically require the standard 8250 or higher speed 16450 UART to perform parallel-to-serial and serial-to-parallel conversion process necessary to interface a parallel bus with the inherently serial modem function. The SSI 73K222U provides a highly integrated design which can eliminate multiple components in any integral bus modem application, and is ideal for internal PC modem applications.

The SSI 73K222U includes two possible operating modes. In the dual-port mode, the device is suitable for conventional plug-in modem card designs which use a separate local microprocessor for command interpretation and control of the modem function. In this mode, a dedicated microcontroller communicates with the SSI 73K222U using a separate serial command port. In the single-port mode the main CPU can control both the UART and modem function using the parallel data bus.This allows very efficient modem design with no local microprocessor required for dedicated applications such as laptop PC's or specialized terminals.

To make designs more space efficient, the SSI 73K222U includes the 2-wire to 4-wire hybrid drivers, off-hook relay driver, and an audio monitor output with software volume control for audible call progress monitoring. As an added feature the UART function can be used independent of the modem function, providing an added asynchronous port in a typical PC application with no additional circuitry required.

UART FUNCTION (16C450)

The UART section of the SSI 73K222U is completely compatible with the industry standard 16C450 and the 8250 UART devices. The bus interface is identical to the 16450, except that only a single polarity for the control signals is supported. The register contents and addresses are also the same as the 16C450. To insure compatibility with all existing releases of the 8250 UART design, external circuitry normally used in PC applications to emulate 8250B or 8250A interrupt operation has been included on the SSI 73K222U. A select line is then provided to enable the desired interrupt operation. The UART used in the SSI 73K222U can be used with faster bus read and write cycles than a conventional 16C450 UART. This allows it to interface directly with higher clock rate microprocessors with no need for external circuitry to generate wait states.

The primary function of the UART is to perform parallel-to-serial conversion on data received from the CPU and serial-to-parallel conversion on data received from the internal modem or an external device. The UART can program the number of bits per character, parity bit generation and checking, and the number of stop bits. The UART also provides break generation and detection, detection of error conditions, and reporting of status at any time. A prioritized maskable interrupt is also provided.

The UART block has a progammable baud rate generator which divides an internal 1.8432 MHz clock to generate a clock at 16 x the data rate. The data rate for the transmit and receive sections must be the same. For DPSK modulation, the data rate must be 1200 Hz or 600 Hz. For FSK modulation, the data rate must be 300 Hz or less. The baud generator can create a clock that supports digital transfer at up to 115.2 kHz. The output of the baud generator can be made available at the CLK pin under program control.

MODEM FUNCTION (SSI 73K222L)

The modem section of the SSI 73K222U provides all necessary analog functions required to create a single chip Bell 212A/103 and CCITT V.22/V.21 modem, controlled by the system CPU or a local dedicated microprocessor. Asynchronous 1200 bit/s DPSK (Bell 212A and V.22) and 300 baud FSK (Bell 103 and V.21) modes are supported.

The modem portion acts as a peripheral to the microprocessor. In both modes of operation, control information is stored in register memory at specific address locations. In the single-port mode, the modem section can be controlled through the 16C450 interface, with no external microcontroller required. The primary analog blocks are the DPSK modulator/demodulator, the FSK modulator/demodulator, the high and low band filters, the AGC, the special detect circuitry, and the DTMF tone generator. The analog functions are performed with switched capacitor technology.

PSK MODULATOR / DEMODULATOR

The SSI 73K222U modulates a serial bit stream into dibit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A or V.22 standard. The baseband signal is then filtered to reduce intersymbol interference on the band limited 2-wire PSTN line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into dibits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. The demodulator decodes either a 1200 Hz carrier (originate carrier) or a 2400 Hz carrier (answer carrier). The SSI 73K222U uses a phase-locked-loop coherent demodulation technique that offers inherently better performance than typical DPSK demodulators used by other manufacturers.

FSK MODULATOR/DEMODULATOR

The FSK modulator frequency modulates the analog output signal using two discrete frequencies to represent the binary data. In Bell 103, the standard frequencies of 1270 Hz and 1070 Hz (originate mark and space) and 2225Hz and 2025 Hz (answer mark and space) are used. V.21 mode uses 980 Hz and 1180 Hz (originate, mark and space) or 1650 Hz and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit signal and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization is necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the band limited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping, and provides a total dynamic range of >45 dB.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, call-progress tones, answer tone, and weak received signal (long loop condition). An unscrambled mark signal is also detected when the received data out of the DPSK demodulator before the descrambler has been high for 165.5 mS ±13.5 mS. The appropriate status bit is set when one of these conditions changes and an interrupt is generated for all monitored conditions except long loop. The interrupts are disabled (masked) when the enable interrupt bit is set to a 0.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from a 0 to a 1.

TEST FEATURES

Test features such as analog loopback (ALB), remote digital loopback, local digital loopback, and internal pattern generators are also included.

LINE INTERFACE

The line interface of the SSI 73K222U consists of a two-to-four wire hybrid, and an off-hook relay driver.

The two-to-four wire converter has a differential transmit output and requires only a line transformer and an external impedance matching resistor. Four-wire operation is also available by simply using either of the transmit output signals.

The relay driver output of the SSI 73K222U is an open drain signal capable of sinking 20 mA, which can control a line closure relay used to take the line off hook and to perform pulse dialing.

AUDIO MONITOR

An audio monitor output is provided which has a software programmable volume control. Its output is the received signal. The audio monitor output can directly drive a high impedance load, but an external power amplifier is necessary to drive a low-impedance

PIN DESCRIPTION

GENERAL

NAME	DIP	PLCC	TYPE	DESCRIPTION
VDD	40	44	I	+5V Supply ±10%, bypass with a .1 and a 22μF capacitor to GND
GND	20	22	I	System Ground
VREF	19	21	O	VREF is an internally generated reference voltage which is externally bypassed by a .1μF capacitor to the system ground.
ISET	9	11	I	The analog current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND. Alternatively, an internal bias can be selected by connecting ISET to GND, which will result in a larger worst-case supply current due to the tolerance of on-chip resistors. Bypass with .1μF capacitor if resistor is used.
XTL1 XTL2	25 24	27 26	I I	These pins are connections for the internal crystal oscillator requiring an 11.0592 MHz crystal (9216Hz x 1200). XTAL2 can also be TTL driven from an external clock.
CLK	21	23	O	Output Clock. This pin is selectable under processor control to be either the crystal frequency (which might be used as a processor clock) or the output of the baud generator.
RESET	10	12	I	Reset. An active signal (high) on this pin will put the chip into an inactive state. The control register bits (except the Receiver Buffer, Transmitter Holding, and Divisor latches) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull-down resistor permits power-on reset using a 0.1μF capacitor connected to the 5V supply.
STNDLN	15	17	I	Single-port mode select (active high). In a single-port system there is no local microprocessor and all the modem control is done through the 16C450 parallel bus interface. The local microprocessor interface is replaced with UART control signals which allow the device to function as a digital UART as well as modem.

PIN DESCRIPTION (continued)

UART INTERFACE

<table>
<tr><th>NAME</th><th>DIP</th><th>PLCC</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>UA0-UA2
UA3</td><td>37-39
12</td><td>41-43
14</td><td>I
I</td><td>UART Address. These pins determine which of the UART registers is being selected during a read or write on the UART data bus. The contents of the DLAB bit in the UART's Line Control Register also control which register is referenced. In single-port mode, UA0-UA3 are latched when $\overline{\text{ADS}}$ goes high. In dual-port, only UA0-UA2 are used.</td></tr>
<tr><td>UDO-UD7</td><td>27-34</td><td>30-37</td><td>I/O</td><td>(3 state) UART Data. Data or control information to the UART registers is carried over these lines.</td></tr>
<tr><td>$\overline{\text{DISTR}}$</td><td>35</td><td>38</td><td>I</td><td>Data Input Strobe. A low on this pin requests a read of the internal UART registers. Data is output on the D0-D7 lines if $\overline{\text{DISTR}}$ and $\overline{\text{CS2}}$ are active.</td></tr>
<tr><td>$\overline{\text{DOSTR}}$</td><td>36</td><td>39</td><td>I</td><td>Data Output Strobe. A low on this pin requests a write of the internal UART registers. Data on the D0-D7 lines are latched on the rising edge of $\overline{\text{DOSTR}}$. Data is only written if both $\overline{\text{DOSTR}}$ and $\overline{\text{CS2}}$ are active.</td></tr>
<tr><td>$\overline{\text{CS2}}$</td><td>1</td><td>2</td><td>I</td><td>Chip Select. A low on this pin allows a read or write to the UART registers to occur. In single port mode, $\overline{\text{CS2}}$ is latched on $\overline{\text{ADS}}$.</td></tr>
<tr><td>INTRPT</td><td>5</td><td>7</td><td>O</td><td>(3 state) UART Interrupt. This signal indicates that an interrupt condition on the UART side has occurred. If the Enable 8250A interrupt bit in the interrupt Enable Register is 0 the interrupt is gated by the $\overline{\text{DISTR}}$ signal to provide compatibility with the 8250B. The output can be put in a high impedance state with the OUT2 register bit in the Modem Control Register. In single-port mode, INTRPT also becomes valid when a modem interrupt signal is generated by the modem section's Detect Register.</td></tr>
<tr><td>RXD</td><td>6</td><td>8</td><td>I/O</td><td>Function is determined by STNDLN pin and bit 7, Tone Control Register:
<table>
<tr><th>STNDLN</th><th>D7</th><th></th></tr>
<tr><td>0</td><td>0</td><td>RXD outputs data received by modem.</td></tr>
<tr><td>1</td><td>0</td><td>RXD is electrically an input but signal is ignored.</td></tr>
<tr><td>X</td><td>1</td><td>RXD is a serial input to UART.</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTION (continued)

UART INTERFACE (continued)

<table>
<tr><td rowspan="5">TXD</td><td rowspan="5">7</td><td rowspan="5">9</td><td rowspan="5">O</td><td colspan="3">Function is determined by STNDLN pin and bit 7, Tone Control Register:</td></tr>
<tr><td>STNDLN</td><td>D7</td><td></td></tr>
<tr><td>0</td><td>0</td><td>TXD is a serial output of UART.</td></tr>
<tr><td>1</td><td>0</td><td>TXD is forced to a mark.</td></tr>
<tr><td>X</td><td>1</td><td>TXD is a serial output of UART.</td></tr>
</table>

ANALOG / LINE INTERFACE

NAME	DIP	PLCC	TYPE	DESCRIPTION
TXA1 TXA2	3 4	4 5	O O	(differential) Transmitted Analog. These pins provide the analog output signals to be transmitted to the phone line. The drivers will differentially drive the impedance of the line transformer and the line matching resistor. An external hybrid can also be built using TXA1 as a single ended transmit signal.
RXA	16	18	I	Received Analog. This pin inputs analog information that is being received by the two-to-four wire hybrid. This input can also be taken directly from an external hybrid.
SPKR	17	19	O	Speaker Output. This pin outputs the received signal through a programmable attenuator stage, which can be used for volume control and disabling the speaker.
$\overline{OH}$	18	20	O	Off-hook relay driver. This signal is an open drain output capable of sinking 20mA and is used for controlling a relay. The output is the complement of the $\overline{OH}$ register bit in CR3.

PIN DESCRIPTION (continued)

UART CONTROL INTERFACE (STNDLN = 1)
(See Figure 1: Single-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
$\overline{ADS}$	23	25	I	Address Strobe. $\overline{ADS}$ is used to latch address and chip select to simplify interfacing to a multiplexed Address/Data Bus. UA0-UA3 and $\overline{CS2}$ are latched when the $\overline{ADS}$ signal goes high.
UA3	12	14	I	UART Address Bit 3. UA3 is used in single-port mode to address the modem registers from the 16C450 interface. If UA3 is 0, the normal 16C450 registers are addressed by UA0-UA2 and if UA3 is 1, the modem registers are addressed. UA3 is latched when $\overline{ADS}$ goes high.
$\overline{CTS}$	14	16	I	Clear to Send. This pin is the complement of CTS bit in the Modem Status Register. The signal is used in modem handshake control to signify that communications have been established and that data can be transmitted.
$\overline{DSR}$	13	15	I	Data Set Ready.This pin is the complement of DSR bit in the Modem Status Register.The signal is used in modem handshake to signify that the modem is ready to establish communications.
$\overline{DCD}$	11	13	I	Data Carrier Detect. This pin is the complement of DCD bit in the Modem Status Register. The signal is used in modem control handshake to signify that the modem is receiving a carrier.
$\overline{DTR}$	22	24	O	Data Terminal Ready.The $\overline{DTR}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 is available to communicate.
$\overline{RTS}$	2	3	O	Request to Send. The $\overline{RTS}$ output is programmed through a bit in the Modem Control Register. The signal is used in modem handshake to signify that the 16C450 has data to transmit.
$\overline{RI}$	8	10	I	Ring Indicator. This Indicates that a telephone ringing signal is being received. This pin is the complement of the RI bit in the Modem Status Register.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE (STNDLN = 0)

(See Figure 2: Dual-port mode)

NAME	DIP	PLCC	TYPE	DESCRIPTION
MA0-MA2	12-14	14-16	I	Modem Address Control. These lines carry register addresses for the modem registers and should be valid throughout any read or write operation.
DATA	22	24	I/O	Serial Control Data. Serial control data to be read/written is clocked in/out on the falling edge of the DCLK pin. The direction of data transfer is controlled by the state of the $\overline{\text{RD}}$ pin. If the $\overline{\text{RD}}$ pin is active (low) the DATA line is an output. Conversely, if the $\overline{\text{RD}}$ pin is inactive (high) the DATA line is an input.
$\overline{\text{RD}}$	23	25	I	Read. A low on this input informs the SSI 73K222U that control data or status information is being read by the processor from a modem register.
$\overline{\text{WR}}$	26	28	I	Write. A low on this input informs the SSI 73K222U that control data or status information is available for writing into a modem register. The procedure for writing is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{\text{WR}}$ low. Data is written on the rising edge of $\overline{\text{WR}}$.
DCLK	11	13	I	Data Clock. The falling edge of this clock is used to strobe control data for the modem registers in or out on the DATA pin. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive cycles of DCLK and then to pulse $\overline{\text{WR}}$ low. Data is written on the rising edge of $\overline{\text{WR}}$. The falling edge of the $\overline{\text{RD}}$ signal must continue for eight cycles of DCLK in order to read all eight bits of the reference register. Read data is provided LSB first. Data will not be output unless the $\overline{\text{RD}}$ signal is active.
$\overline{\text{INT}}$	2	3	O	(with weak pull-up) Modem Interrupt. This output signal is used to inform the modem processor that a change in a modem detect flag has occurred. The processor must then read the Modem Detect Register to determine which detect triggered the interrupt. $\overline{\text{INT}}$ will stay active until the processor reads the Modem Detect Register or does a full reset.
µPRST*	8	10	O	Microprocessor Reset. This output signal is used to provide a hardware reset to the microprocessor. This signal is high if the RESET pin is high or the MCR bit D3 (OUT1) bit is set.

* NOTE: The µPRST pin is an upgraded function which was not included in the initial definition of the SSI 73K222U.

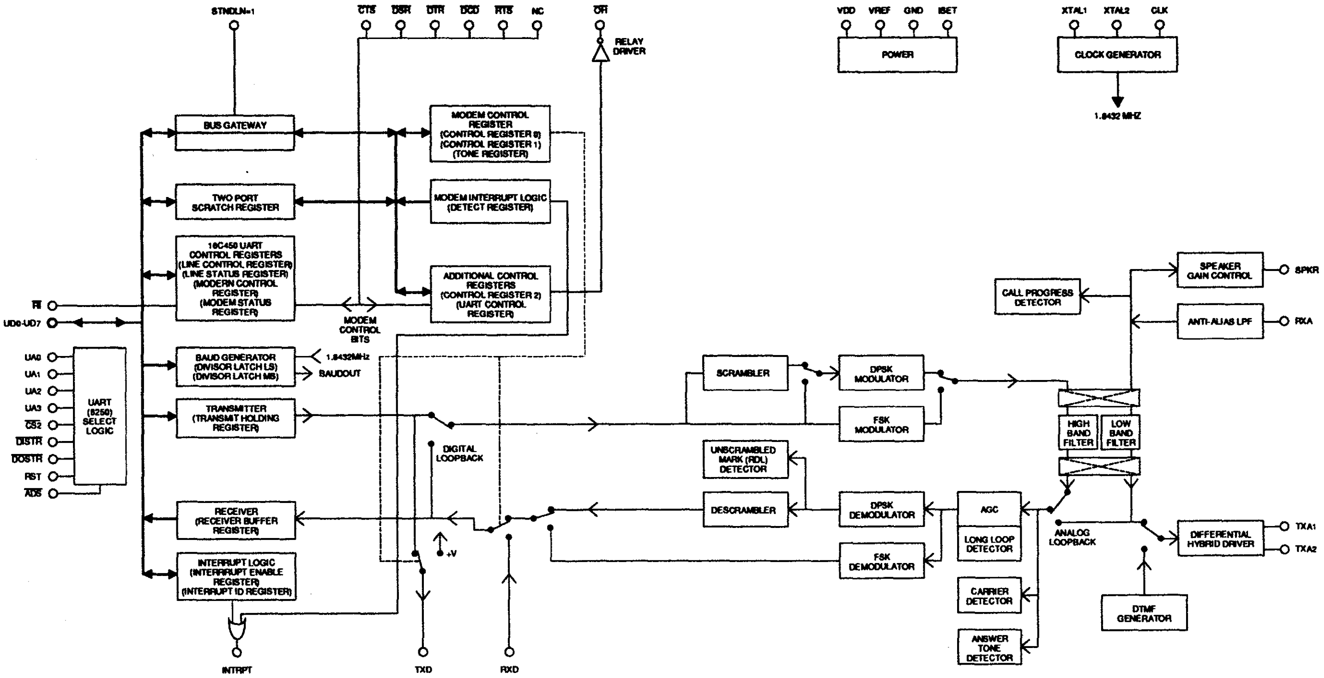


FIGURE 1:
Single-Port Mode

In the single-port mode, the SSI 73K222U is designed to be accessed only by the main CPU using the same parallel bus utilized for data transfer. This mode is enabled when the STNDLN pin is at a logic "1". In the single port mode, internal registers are accessed by the main CPU to configure both the UART section and the modem function, eliminating the need for a separate microcontroller. In this mode, multiplexed pins provide the $\overline{CTS}$, $\overline{DSR}$, $\overline{DTR}$, $\overline{DED}$ and $\overline{RI}$ signals normally associated with the UART function. A separate pin, $\overline{ADS}$, is used for bus control.

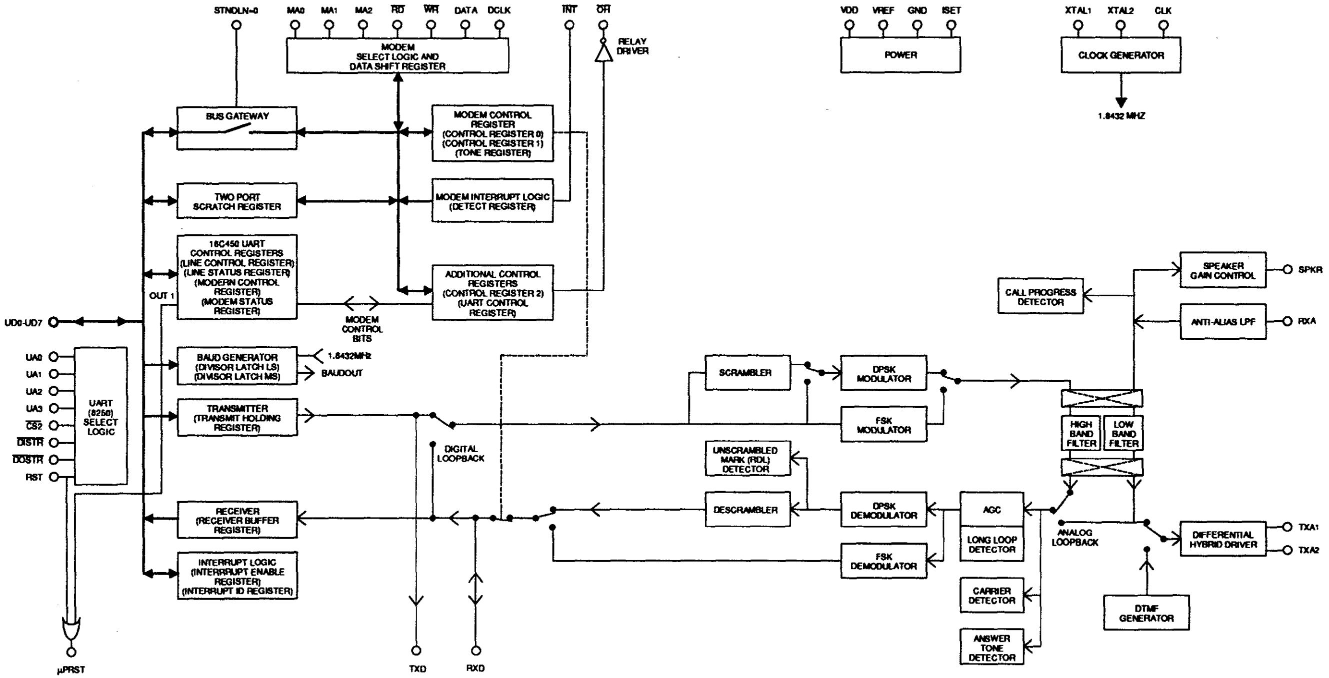


FIGURE 2:
Dual-Port Mode

The dual-port mode allows use of a dedicated microprocessor for control of the modem function, and is enabled when the STNDLN pin = "0". This mode is useful for conventional plug-in card modem designs where it is necessary to make the modem function transparent to the main CPU. In this mode, the SSI 73K222U's multiplexed pins form the serial command bus used to communicate with the external microprocessor. The $\overline{\text{RI}}$, $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DTR}}$, and $\overline{\text{DCD}}$ logic functions must then be implemented using ports from the dedicated microprocessor.

The serial control interface allows access to the control and status registers via a serial command port. In this mode the MA0, MA1, and MA2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ lines. A read operation is initiated when the $\overline{\text{RD}}$ line is taken low. The next eight cycles of DCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of DCLK. $\overline{\text{WR}}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{\text{WR}}$.

UART CONTROL REGISTER OVERVIEW

			DATA BIT NUMBER							
REGISTER		UART ADDRESS UA3-UA0*	D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	0000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	0001 DLAB = 0	0	0	0	ENABLE 8250A/ 16C450 INTERRUPT	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	0010	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	0011	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	0100	0	0	0	LOOP	ENABLE INTERRUPT (OUT2 IN 16C450)	µPRST (OUT1 IN 16C450)	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	0101	0	TRANSMIT SHIFT REG. EMPTY (TSRE)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	0110	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	0111	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	0000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	0001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

* In single-port mode (STNDLN pin = 1), all four address lines UA3-UA0 are used to address the UART Control Registers.

* In dual-port mode (STNDLN pin = 0), only three address lines UA2-UA0 are used to address the UART Control Registers; the UA3 pin becomes the MA2 pin in this mode.

MODEM CONTROL REGISTER OVERVIEW

		ADDRESS		DATA BIT NUMBER							
REGISTER		STNDLN 0	1	D7	D6	D5	D4	D3	D2	D1	D0
		MA2-MA0	UA3-UA0								
CONTROL REGISTER 0	CR0	000	1000	MODULATION OPTION	0	MODULATION MODE	POWER ON	CHARACTER SIZE 1 (READ ONLY)	CHARACTER SIZE 0 (READ ONLY)	TRANSMIT ENABLE	ORIGINATE/ ANSWER
CONTROL REGISTER 1	CR1	001	1001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER	DR	010	1010	DEVICE SIGNATURE 1	DEVICE SIGNATURE 0	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	ANSWER TONE DETECT	CALL PROGRESS DETECT	LONG LOOP DETECT
TONE CONTROL REGISTER	TONE	011	1011	RXD/TXD CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0 GUARD/ANS. TONE
CONTROL REGISTER 2	CR2	100	1100	RESERVED FOR FUTURE USE							
CONTROL REGISTER 3	CR3	101	1101	SPEAKER VOLUME 1	SPEAKER VOLUME 0	OFF-HOOK	X	X	X	X	X
SCRATCH REGISTER	SCR	110	1110	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
UART CONTROL REGISTER	UCR	111	1111	TXCLK (READ ONLY)	X	REQUEST TO SEND (RTS) (READ ONLY)	DATA TERM. READY (DTR) (READ ONLY)	RING INDICATOR (RI)	DATA CARRIER DETECT (DCD)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)

UART REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 0**	**UA3 - UA0 = 0000, DLAB = 0**

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 000, DLAB = 0**	**UA3 - UA0 = 0000, DLAB = 0**

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)

STNDLN:	**0**	**1**
ADDRESS:	**UA2 - UA0 = 001, DLAB = 0**	**UA3 - UA0 = 0001, DLAB = 0**

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding Register Empty	1	This bit enables the Transmitter Holding Register Empty Interrupt, when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt, when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Register Interrupt when set to interrupt logic 1.
D4	8250A/16450	1/0	Set for compatibility with 8250A/16C450 UARTS. Reset this bit to disable the gating of the INTRPT interrupt line with the $\overline{\text{DISTR}}$ signal which is needed for 8250B compatibility.
D5 - D7	Not Used	0	These three bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 010 UA3 - UA0 = 0010

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired priortized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 011 UA3 - UA0 = 0011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Word Length Select 0			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable	1		This bit is the Parity Enable bit. When bit 3 is a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select	1 or 0		This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's are transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's are transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued)

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Stick Parity	1 or 0		This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		Output of modem is set to a spacing state. When the modem is transmitting DPSK data if the Set Break bit is held for one full character (start, data, parity, stop) the break will be extended to 2 N + 3 space bits (where N = # data bits + parity bit + 1 start + 1 stop). Any data bits generated during this time will be ignored. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TSRE = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 100 UA3 - UA0 = 0100

The MCR register controls the interface with the modem. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers. In single-port mode, bits D1 and D0 are available inverted at the $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$ pins.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{\text{DTR}}$) output. When bit 0 is set to a logic 1, the $\overline{\text{DTR}}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{\text{DTR}}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{\text{RTS}}$) output. When bit 1 is set to a logic 1, the $\overline{\text{RTS}}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{\text{RTS}}$ output is forced to a logic 1.
D2	µPRST* (OUT1 in 16C450)	1	In single-port mode inactive unless loop = 1, then functions as below (D4). In dual-port mode the µPRST pin is the logical OR of this bit and the RESET pin.
D3	Enable Interrupt (OUT2 in 16C450)	0	Sets INTRPT pin to high impedance if STNDLN = 1.
		1	INTRPT output enabled.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART portion of the SSI 73K222U. When bit D4 is set to logic 1, the following occurs: 1. TXD is forced to mark, RXD is ignored. 2. The output of the Transmitter is looped to the Receiver. 3. The four modem control inputs to the UART ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, and $\overline{\text{RI}}$) are ignored and the UART signals $\overline{\text{RTS}}$, $\overline{\text{DTR}}$, Enable Interrupt, and µPRST are forced inactive. 4. The UART signals RTS, DTR, Enable Interrupt, and µPRST are internally connected to the four control signals CTS, DSR, DCD and RI respectively. Note that the Modem Status Register Interrupts are now controlled by the lower four bits of the Modem Control Register. The interrupts are still controlled by the Interrupt Enable Register.
D5 - D7		0	These bits are permanently set to logic 0.

* Note: The µPRST bit has an upgraded function which was not included in the initial definition of the SSI 73K222U.

LINE STATUS REGISTER (LSR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 101 UA3 - UA0 = 0101

This register provides status information to the CPU concerning the data transfer.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Data Ready is reset to 0 by reading the data in the Receiver Buffer Register or by writing a 0 into it from the processor.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. The bit is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. A framing error will not occur in DPSK receive from the modem due to the fact that missing stop bits are reinserted.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop) or for two full data words when receiving in DPSK mode from the modem. The BI bit is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) indicates that the Transmitter is ready to accept a new character for transmission. The THRE bit is reset when the CPU loads a character into the Transmit Holding Register.
D6	TSRE	1	The Transmit Shift Empty (TSRE) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty.
D7		0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 110 UA3 - UA0 = 0110

This register provides the current state of the control signals from the modem. In addition, four bits provide change information. The CTS, DSR, DCD, and RI signals come from the UART Control Register if STNDLN = 0 and from the $\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$ and $\overline{\text{RI}}$ pins (inverted) if STNDLN = 1. This register is READ ONLY. The delta bits indicate whether the inputs have changed since the last time the Modem Status Register has been read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, μPRST, and Enable Interrupt in the Modem Control Register respectively.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DCTS	1	This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{\text{CTS}}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{\text{DSR}}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	This bit is the Trailing Edge of the Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{\text{RI}}$ input to the chip has changed state.
D3	DDCD	1	This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{\text{DCD}}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{\text{CTS}}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{\text{DSR}}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{\text{RI}}$) input. If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to μPRST in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{\text{DCD}}$) If STNDLN = 0, this reflects the status of the UART Control Register bit. If bit 4 of the MCR is set to a 1, this bit is equivalent to Enable Interrupt in the MCR.

SCRATCH REGISTER (SCR)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 111 UA3 - UA0 = 0111

The Scratch Register is a dual port register which can be simultaneously accessed through both the UART bus and the modem bus.This provides the possibility for the modem controller to communicate directly with the central CPU. Note that if both processors write the Scratch Register, the data stored will be from whichever processor last wrote the register.

DIVISOR LATCH (Least significant byte) (DLL)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 000, DLAB = 1 UA3 - UA0 = 0000, DLAB = 1

DIVISOR LATCH (Most significant byte) (DLM)
STNDLN: 0 1
ADDRESS: UA2 - UA0 = 001, DLAB = 1 UA3 - UA0 = 0001, DLAB = 1

DIVISOR LATCH VALUE VS. DATA RATE

The Divisor Latch is two 8-bit write only registers which control the rate of the programmable baud generator. The programmable baud generator generates an output clock by dividing an internal 1.8432 MHz clock by the value stored in the divisor latch. This output clock has a value of 16X the data rate at which the modem will operate. This output clock is available at pin 21 under the control of bit 3 (D3) of the Modem Control Register 1. Upon loading either of the Divisor Latches the 16-bit device counter is immediately loaded, preventing long counts on initial load. The following table shows divisor values for common data rates.

DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED	DESIRED DATA RATE	DIVISOR USED FOR 16 x DATA RATE CLOCK	% ERROR GENERATED
50 [1]	2304		4800	24	
75 [1]	1536		7200	16	
110 [1]	1047		9600	12	
134.5 [1]	857	0.058	19200	6	
159 [1]	768		38400	3	
300 [1]	384		56000	2	2.86
600 [2]	192				
1200 [3]	96				
1800	64				
2000	58	0.69			
2400	48				
3600	32				

1. Data Rate valid for FSK transmission.
2. Data Rate valid for halfspeed DPSK transmission.
3. Data Rate valid for normal 1200 BIT/S DPSK transmission.

MODEM REGISTER BIT DESCRIPTIONS

CONTROL REGISTER (CR0)

STNDLN:	**0**	**1**
ADDRESS:	**MA2 - MA0 = 000**	**UA3 - UA0 = 1000**

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Answer/Originate	0		Selects Answer Mode (transmit in high band, receive in low band).
		1		Selects Originate Mode (transmit in low band, receive in high band).
D1	Transmit Enable	0		Disables transmit output at TXA.
		1		Enables transmit output at TXA. NOTE: Answer tone and DTMF TX control require Transmit Enable. If Transmit Enable is on, call progress and answer tone detector interrupts are masked.
D2, D3	Character Size 0, 1			These bits are read only. These bits represent the character size. The character size is determined by the UART Line Control Register and includes data, parity (if used), one start bit, and one stop bit.
		D3	D2	Character length
		0	0	8-bit character
		0	1	9-bit character
		1	0	10-bit character
		1	1	11-bit character
D4	Power ON			This bit controls the power down mode of the SSI 73K222U, the analog, and most digital portions of the chip. The digital interface is active during power down.
		0		Power down mode.
		1		Normal operation.
D5	Modulation Mode	0		DPSK
		1		FSK
D6	Reserved	0		Must be written as zero.
D7	Modulation Option	0		DPSK: 1200 bit/s
		1		600 bit/s
		0		FSK: 103 mode
		1		V.21 mode

CONTROL REGISTER (CR1)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 001 UA3 - UA0 = 1001

BIT NO.	NAME	CONDITION		DESCRIPTION
D0, D1	Test Mode	D1	D0	
		0	0	Selects normal operating mode.
		0	1	Analog Loopback Mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the Transmitter. To squelch the TXA pin, transmit enable bit must be forced low.
		1	0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data in TXD is ignored.
		1	1	Selects half-duplex. Internally performs a logical AND of TXD and RXD to send to the UART receiver. Both transmit and receive characters will occur at the Receiver Buffer Register.
D2	Reset	0		Selects normal operation.
		1		Resets modem to power down state. All Control Register bits (CR0, CR1, TONE) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0		CLK pin output is selected to be an 11.0592 MHz crystal echo output.
		1		CLK pin output is selected to be 16 x the Data Rate set by the UART divisor latch.
D4	Bypass Scrambler	0		Selects normal operation. DPSK data is passed through scrambler.
		1		Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path.

CONTROL REGISTER (CR1) (Continued)

BIT NO.	NAME	CONDITION		DESCRIPTION
D5	Enable Detect Interrupt	0		Disables interrupts generated by Detect Register bits D1 - D4 at INT pin in dual-port mode, or at INTRPT pin in single-port mode. All interrupts normally disabled in power down modes.
		1		Enables interrupts generated by Detect Register bits D1 - D4 at $\overline{INT}$ pin in dual-port mode, or at INTRPT pin in single-port mode. An interrupt will be generated with a change in status of DR bits D1 - D4. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode. The interrupt is reset when the DR register is read.
D6, D7	Transmit Pattern	D7	D6	
		0	0	Selects normal data transmission as controlled by the state of the TXD pin.
		0	1	Selects an alternating mark/space transmit pattern for modem testing.
		1	0	Selects a constant mark transmit pattern.
		1	1	Selects a constant space transmit pattern.

DETECT REGISTER (DR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 010 UA3 - UA0 = 1010

MODEM SECTION

BIT NO.	NAME	CONDITION		DESCRIPTION
D0	Long Loop	0		Indicates normal received signal.
		1		Indicates low received signal level (< -38 dBm).
D1	Call Progress Detect	0		No call progress tone detected.
		1		Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.
D2	Answer Tone Received	0		No answer tone detected.
		1		Indicates detection of 2225 Hz answer tone in Bell mode or 2100 Hz in CCITT mode. The device must be in Originate Mode for detection of answer tone for normal operation. For CCITT answer tone detection, bit D0 of the Tone Register must be set.
D3	Carrier Detect	0		No carrier detected in the receive channel.
		1		Carrier has been detected in the receive channel.
D4	Unscrambled Marks	0		No unscrambled mark detected.
		1		Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 13.5 ms.
D5	Receive Data			Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7	Device Signature 0, 1	D7	D6	Product Identified
		0	0	SSI 73K212U (special order only)
		0	1	SSI 73K221U (special order only)
		1	0	SSI 73K222U

TONE CONTROL REGISTER (TONE)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 011 UA3 - UA0 = 1011

The Tone Control Register contains information on the tones that are transmitted. Tones are transmitted only if the Transmit Enable bit is set. The priority of the transmit tones are: 1) DTMF, 2) Answer, 3) FSK, 4) Guard.

BIT NO.	NAME	CONDITION				DESCRIPTION
D0	DTMF 0 / Answer/ Guard Tone	D6	D5	D4	D0	D0 interacts with bits D6, D5, and D4 as shown:
		X	X	1	X	Transmit DTMF tones.
		X	1	0	0	Select 2225 Hz answer tone (Bell).
		X	1	0	1	Select 2100 Hz answer tone (CCITT).
		1	0	0	0	Select 1800 Hz guard tone.
		1	0	0	1	Select 550 Hz guard tone.
D0, D1, D2, D3	DTMF	Table below				Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below.

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE CONTROL REGISTER (TONE) (Continued)

D4	TX DTMF (Transmit DTMF)	0		Disable DTMF.
		1		Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS (Transmit Answer Tone)	D5	D0	D5 interacts with bit D0 as shown.
		0	X	Disables answer tone generator.
		1	0	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode.
		1	1	Enables a 2100Hz answer tone generator, with operation same as above.
D6	TX Guard (Transmit Guard Tone)	0		Disables guard tone generator.
		1		Enables guard tone generator. (See D0 for selection of guard tones).
D7	RXD/TXD Control	STNDLN	D7	Function is dependant on status of STNDLN pin.
		0	0	RXD is output data received by modem, TXD is serial output of UART.
		1	0	RXD is electrically an input, but the signal is ignored, TXD is forced to a mark.
		X	1	RXD is serial input to UART, TXD is serial output of UART.

CONTROL REGISTER (CR3)

STNDLN:	**0**	**1**
ADDRESS:	**MA2 - MA0 = 101**	**UA3 - UA0 = 1101**

BIT NO.	NAME	CONDITION		DESCRIPTION
D0 - D4	Not Used			Not presently used.
D5	Off Hook	0		Relay driver open.
		1		Open drain driver pulling low.
D6, D7	Speaker Volume 0, 1	D7	D6	Speaker volume control status.
		0	0	Speaker off
		0	1	-24 dB
		1	0	-12 dB
		1	1	0 dB

SCRATCH REGISTER (SCR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 110 UA3 - UA0 = 1110

The Scratch Register is a dual-port register which can be accessed either through the UART bus or the modem bus. It can be used for a communication path outside the data stream.

UART CONTROL REGISTER (UCR)
STNDLN: 0 1
ADDRESS: MA2 - MA0 = 111 UA3 - UA0 = 1111

The UART Control Register contains the handshaking signals necessary for the microprocessor to communicate with the central CPU through the UART.

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	CTS	1	In dual-port mode, CTS, DSR, DCD and RI are writeable locations which can be read through the 16C450 port in the Modem Status Register.
D1	DSR	1	
D2	DCD	1	In the single-port mode, D0 - D3 are ignored and the information for the Modem Status Register comes directly from the external pins.
D3	RI	1	
D4	DTR	1	
D5	RTS	1	DTR and RTS are read only versions of the same register bits in the Modem Contol Register.
D6	Not Used		
D7	TXCLK	Clock	TXCLK is the clock that the UART puts out with TXD. The falling edge of TXCLK is coincident with the transitions of data on TXD. TXCLK can also be used for the microprocessor to send synchronous data independent of the UART by forcing data patterns using CR1 bits 6 and 7 before the rising edge of TXCLK.

NOTE: Control Register 2 (CR2) is reserved for future products and is disabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

TA = -40°C to 85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD +0.3	V

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD, Supply Voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		85	°C
External Component (Refer to application drawing for placement.)					
VREF Bypass Capacitor [2]	(VREF to GND)	0.1			µF
Bias Setting Resistor [1]	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor [2]	ISET pin to GND	0.1			µF
VDD Bypass Capacitor [2]	(VDD to GND)	0.1			µF
XTL1 Load Capacitor	From pin to GND			40	pF
XTL2 Load Capacitor	From pin to GND			20	pF
Input Clock Variation	(11.0592 MHz)	-0.01		+0.01	%
Hybrid Loading					
R1	See Figure 3		600		Ω
R2			600		Ω
C	TXA Hybrid Loading		0.033		µF

1. Optional for minimum worst case current consumption.
2. Minimum for optimized system layout; may require higher values for noisy environments.

DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85 °C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
IDD, Supply Current					
IDDA, Active	ISET Resistor = 2MΩ		8	12	mA
IDDA, Active	ISET = GND		8	15	mA
IDD1, Power-Down	CLK = 11.0592MHz		3	4	mA
IDD2, Power-Down	CLK = 19.200KHz		2	3	mA
Digital Inputs					
Input High Current IIH	VI = VDD			100	µA
Input Low Current IIL	VI = 0	-200			µA
Input Low Voltage VIL				0.8	V
Input High Voltage VIH	Except RESET & XTL1	2.0			V
Input High Voltage VIH	RESET & XTL1	3.0			V
Pull Down Current RESET PIN		5		30	µA
Input Capacitance				10	pF
Digital Outputs					
Output High Voltage VOH	IOUT = - 1 mA	2.4		VDD	V
VOL UD0-UD7 and INTRPT	IOUT = 3.2 mA			0.4	V
VOL other outputs	IOUT = 1.6 mA			0.4	V
CLK Output VOL	IOUT = 3.2 mA			0.6	V
OH Output VOL	IOUT = 20 mA			1.0	V
OH Output VOL	IOUT = 10 mA			0.5	V
Offstate Current INTRPT pin	VO = 0V	-20		20	µA
Capacitance					
Inputs	Input Capacitance			10	pF
CLK	Maximum capacitive load to pin			15	pF
Analog Pins					
RXA Input Resistance			200		KΩ
RXA Input Capacitance				25	pF

DYNAMIC CHARACTERISTICS AND TIMING

TA = -40°C to +85°C, VDD = 5V ± 10%, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
DPSK Modulator					
Carrier Suppression	Measured at TXA	55			dB
Output Amplitude	ANS TONE 2225 or 2100 Hz	-11	-10.0	-9	dBm0
	DPSK TX Scrambled Marks	-11	-10.0	-9	dBm0
	FSK Dotting Pattern	-11	-10.0	-9	dBm0
FSK Tone Error	Bell 103 or V.21			±5	Hz
DTMF Generator					
Freq. Accuracy		-.25		.25	%
Output Amplitude	Low Band, not in V.21 mode	-10	-9	-8	dBm0
Output Amplitude	High Band, not in V.21 mode	-8	-7	-6	dBm0
Long Loop Detect	DPSK or FSK	-40		-32	dBm0
Demodulator Dynamic Range	DPSK or FSK		45		dB
Call Progress Detector					
Detect Level	2-Tones in 350-600 Hz Band	-39		0	dBm0
Reject Level	2-Tones in 350-600 Hz Band			-46	dBm0
Delay Time	-70dBm0 to -30 dBm0 Step	27		80	ms
Hold Time	-30dBm0 to -70 dBm0 Step	27		80	ms
Hysteresis		2			dB
Carrier Detect	DPSK or FSK Receive				
Threshold	Data	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step	15		45	ms
Hysteresis		2	3.0		dB
Hold Time	-30 dBm0 to -70 dBm0 Step	10		24	ms
Answer Tone Detector					
Detect Level Threshold	In FSK mode	-49.5		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		45	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	10		30	ms
Detect Frequency Range		-2.5		+2.5	%

1. All units in dBm0 are measured at the line input to the transformer. The interface circuit inserts an 8 dB loss in the transmit path (TXA1 - TXA2 to line), and a 3dB loss in the receive path (line to RXA).

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
Speaker Output					
Gain Error		-1		+1	dB
Output Swing SPKR	10K||50 pF LOAD 5% THD	2.75			VP
Carrier VCO					
Capture Range	Originate or Answer	-10		10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency change assumed		40	100	ms
Recovered Clock					
Capture Range	% of Center Frequency	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin.		30	50	ms
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level	550 HZ	-4.0	-3.0	-2.0	dB
(Below DPSK Output)	1800 HZ	-7.0	-6.0	-5.0	dB
Harmonic Distortion	700 to 2900 HZ			-60	dB

SERIAL BUS INTERFACE (See Figure 4)
The following times are for CL = 100 pF.

PARAMETER		MIN	NOM	MAX	UNIT
TRD	Data out from Read	0		140	ns
TCKD	Data out after Clock			200	ns
TRDF	Data Float after Read	0		200	ns
TRCK	Clock High after Read	200			ns
TWW	Write Width	140		10000	ns
TDCK	Data Setup Before Clock	150			ns
TCKH	Data Hold after Clock	20			ns
TCKW	Write after Clock	150			ns
TACR	Address setup before Control [1]	50			ns
TCAR	Address Hold after Control [1]	50			ns
TACW	Address setup before Write	50			ns
TCAW	Address Hold after Write	50			ns

1. Control is later of falling edge of RD or DCLK.

PARALLEL BUS INTERFACE (See Figure 5) The following times are for Cl = 100 pF.

PARAMETER		MIN	MAX	MIN	MAX	UNIT
		Dual-Port Mode		Single-Port Mode		
RC	Read Cycle = TAD + TRC	240		340		ns
TDIW	DISTR Width	80		80		ns
TDDD	Delay DISTR to Data (read time)		80		80	ns
THZ**	DISTR to Floating Data Delay	0	50	0	50	ns
TRA	Address Hold after DISTR	20		20		ns
TRCS	Chip select hold after DISTR	20		20		ns
TAR*	DISTR Delay after Address	20		20		ns
TCSR	DISTR Delay after Chip Select	20		20		ns
WC	Write Cycle = TAW + TDOW + TWC	140		140		ns
TDOW	DOSTR Width	80		80		ns
TDS	Data Setup	30		50		ns
TDH**	Data Hold	20		20		ns
TWA	Address Hold after DOSTR	20		20		ns
TWCS	Chip select hold after DOSTR	20		20		ns
TAW*	DOSTR delay after Address	20		20		ns
TCSW	DOSTR delay after Chip Select	20		20		ns
TADS	Address Strobe Width			40		ns
TAS	Address Setup Time			30		ns
TAH	Address Hold Time			0		ns
TCS	Chip Select Setup Time			30		ns
TCH	Chip Select Hold Time			0		ns
TRC	Read Cycle Delay	40		40		ns
TWC	Write Cycle Delay	40		40		ns
TAD	Address to Read Data	200		300		ns

* TAR and TAW are referenced from the falling edge of either $\overline{\text{CS2}}$ or $\overline{\text{DISTR}}$ or $\overline{\text{DOSTR}}$, which ever is later.

** THZ and TDH are referenced from the rising edge of $\overline{\text{CS2}}$ or $\overline{\text{DISTR}}$ or $\overline{\text{DOSTR}}$, which ever is earlier.

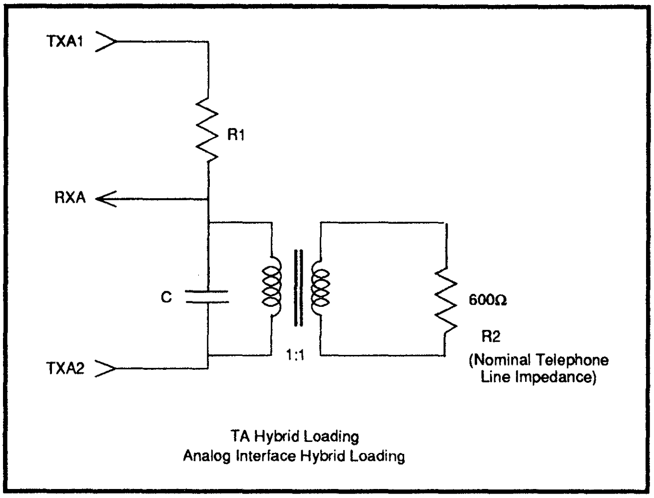


FIGURE 3: TXA Hybrid Loading Analog Interface Hybrid Loading

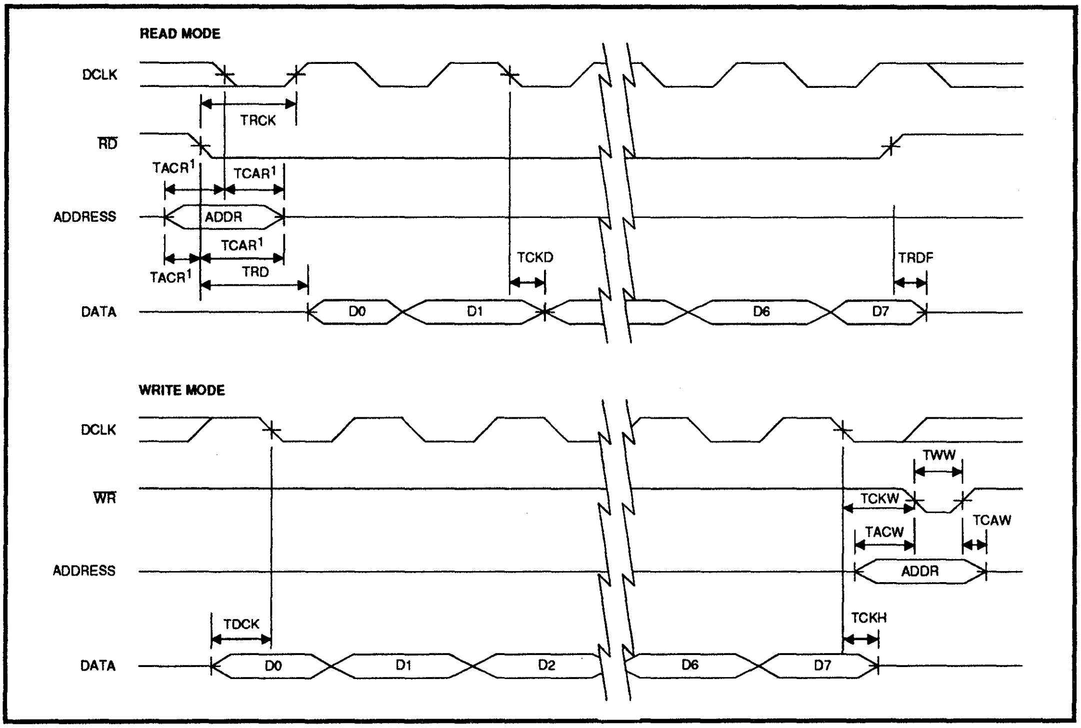


FIGURE 4: Modem Serial Bus Timing

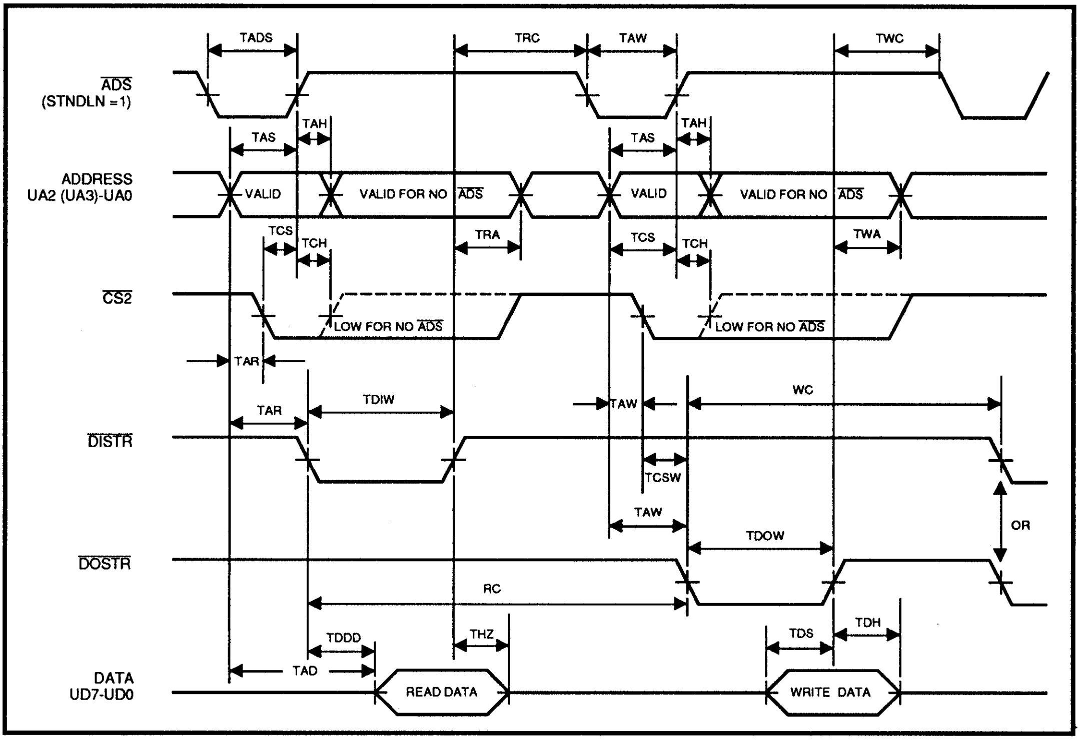


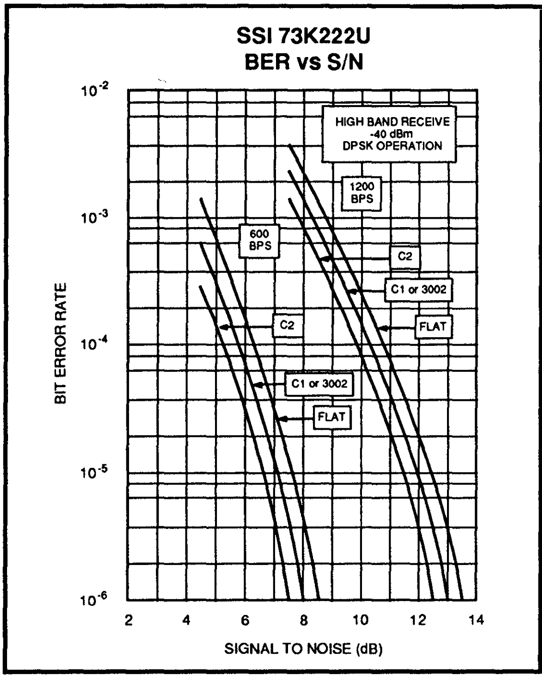
FIGURE 5: UART Bus Timing

TYPICAL PERFORMANCE CHARACTERISTICS

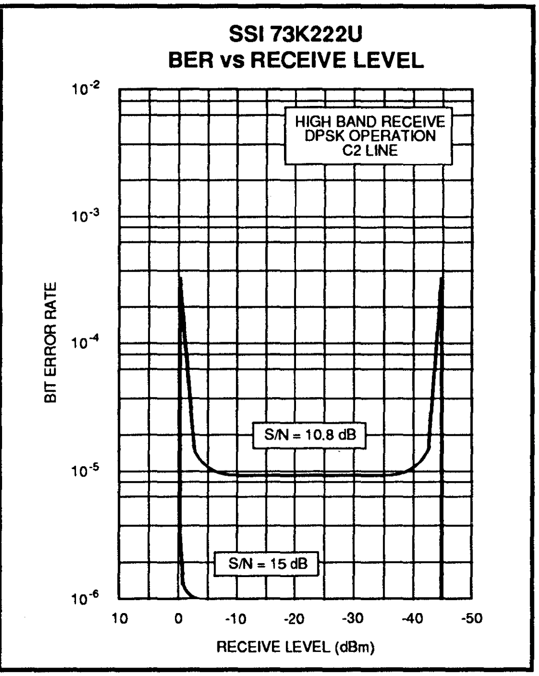
The SSI 73K222U was designed using an integrated analog/digital architecture that offers optimum performance over a wide range of line conditions. The SSI 73K222U utilizes the circuit design proven in SSI's 73K222L one-chip modem, with added enhancements which extend low signal level performance and increase immunity to spurious noise typically encountered in integral bus applications. The SSI 73K222U provides excellent immunity to the types of disturbances present with usage of the dial-up telephone network. The following curves show representative Bit Error Rate performance under various line conditions.

BER vs. S/N

This test measures the ability of the modem to function with minimum errors when operating over noisy lines. Since some noise is generated by even the best dial-up lines, the modem must operate with as low a S/N ratio as possible. Optimum performance is shown by curves that are closest to the zero axis. A narrow spread between curves for the four line conditions indicates minimal variation in performance when operating over a range of line qualities and is typical of high performance adaptive equalization receivers. High band receive data is typically better than low band due to the inherent design of PSK modems.



SSI 73K222U
BER vs S/N



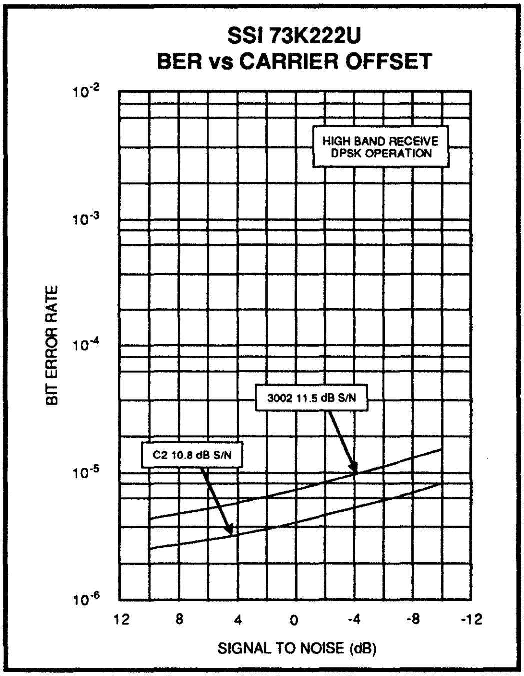
SSI 73K222U
BER vs RECEIVE LEVEL

BER vs. Receive Level

This measures the dynamic range of the modem. As signal levels vary widely over dial-up lines, the widest dynamic range possible is desirable. The minimum Bell specification calls for 36dB of dynamic range. S/N ratios were held constant at the indicated values while receive level was lowered from very high to very low signal levels. The "width of the bowl" of these curves taken at the 10- BER point is a measure of the dynamic range.

BER vs. Carrier Offset

This parameter indicates how the modem performance is impacted by frequency shifts encountered in normal PSTN operation. Flat curves show no performance degradation from frequency offsets. The SSI K-Series devices use a 2nd order carrier tracking phase-locked-loop, which is insensitive to carrier offsets in excess of 10Hz. The Bell network specifications allow as much as 7Hz offset, and the CCITT specifications require modems to operate with 7Hz of offset.



APPLICATION

The SSI 73K222U includes additional circuitry to greatly simplify integral modem designs in either of two different configurations. The single-port mode represents the most efficient implementation for an integral modem. Figure 9 shows a typical schematic using this mode. In this configuration, the SSI 73K222U transfers data and commands through the single parallel port. All modem control is provided by the main CPU, eliminating the need for an external microcontroller and supporting components. The SSI 73K222U is unique in that access to both the UART and modem sections is possible through the UART port. Also shown is a separate serial port, which can be used independent of the modem function when the modem section is inactive. Figure 10 shows a more conventional integral modem design, in which a local microprocessor handles modem supervision, allowing the modem function to be transparent to the main processor. Inclusion of the hybrid drivers, audio volume control, and off hook relay driver reduces component count for a highly efficient design. In either mode of operation, the SSI 73K222U's ability to operate from a single +5 volt power supply eliminates the need for additional supply voltages and keeps power usage to a minimum.

(See Figure 9 & 10: Typical Integral Applications Single and Dual-Port Modes.)

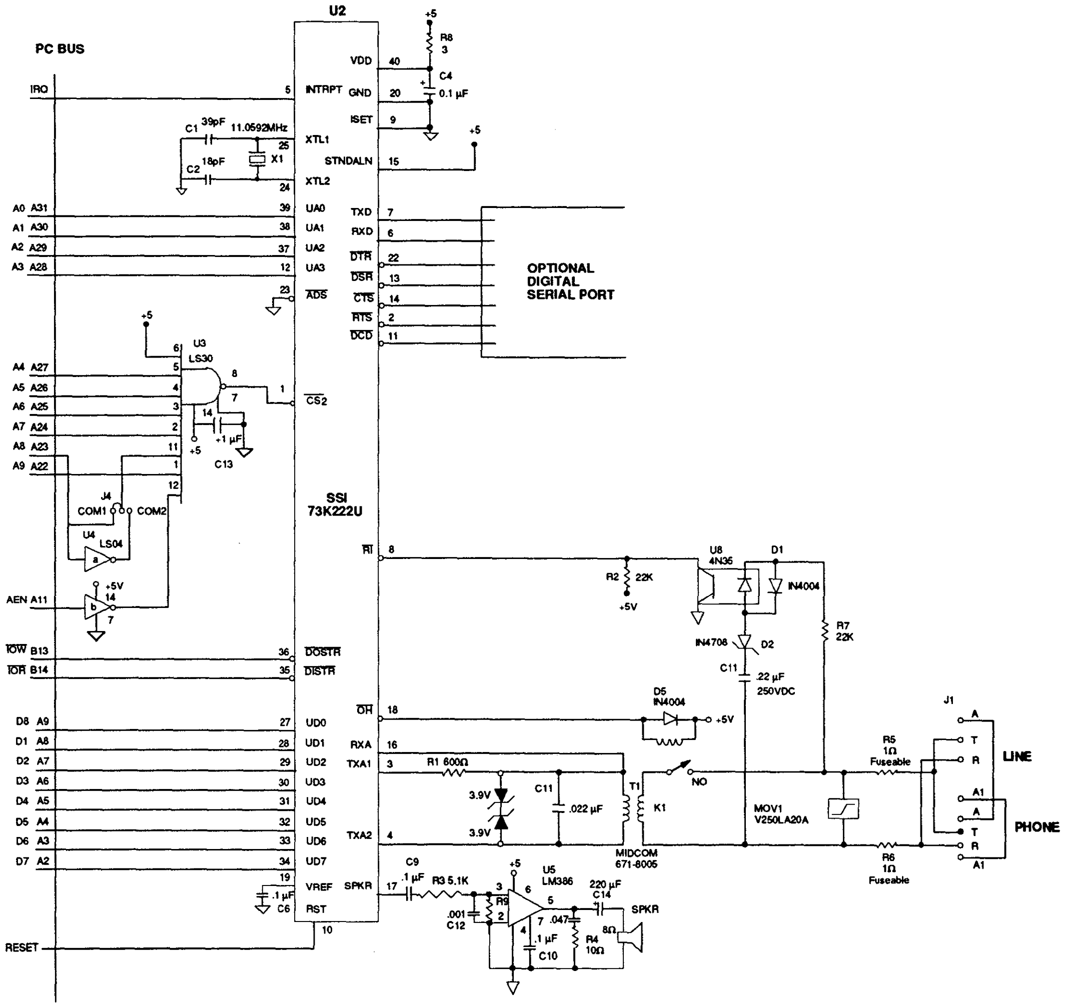


FIGURE 9: 73K22U Typical Integral Application Single-Port Mode

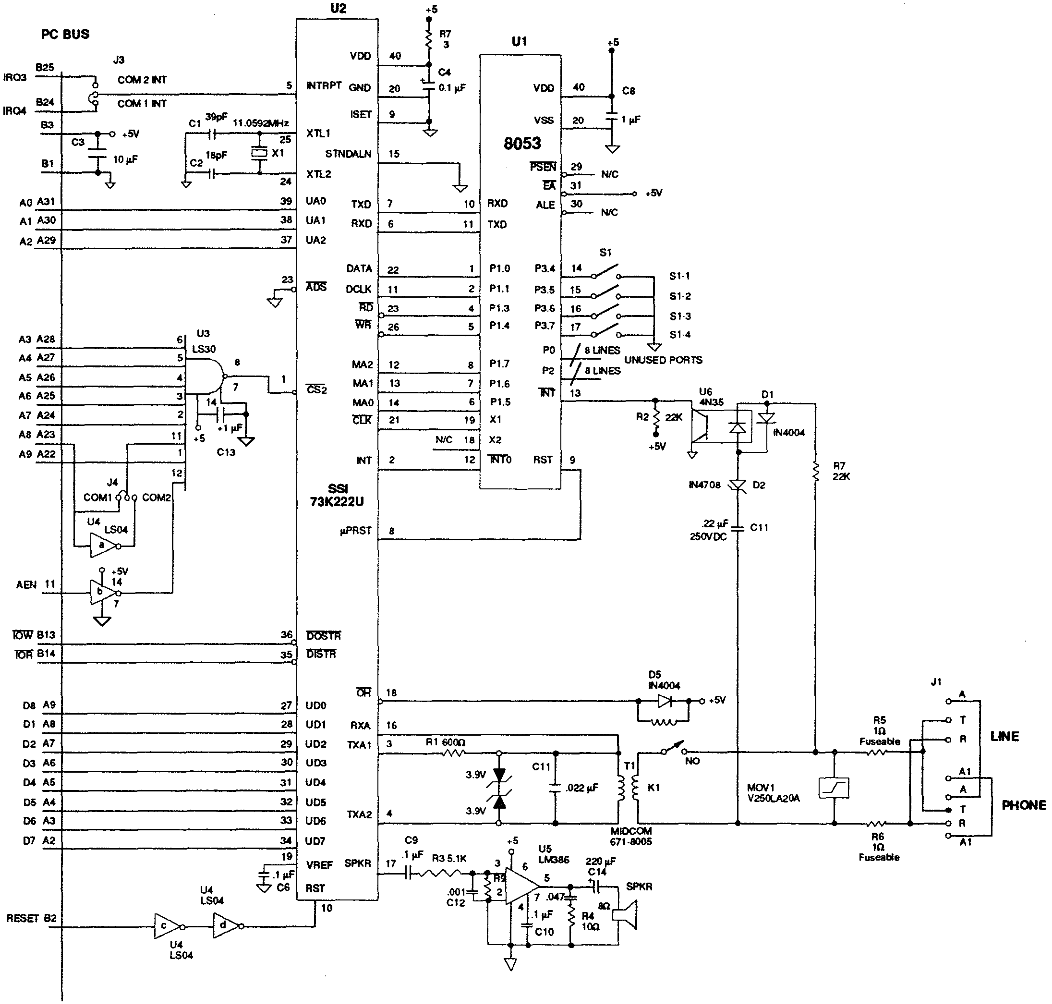
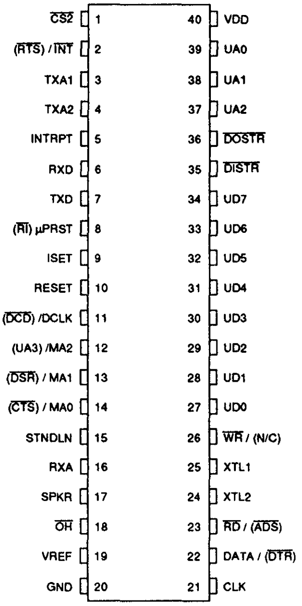


FIGURE 10: 73K22U Typical Integral Application Dual-Port Mode

SSI 73K222U
Single-Chip Modem
with UART

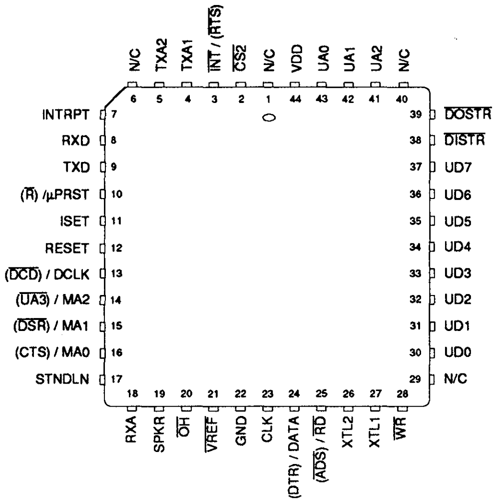
PACKAGE PIN DESIGNATIONS

(Top View)



600-Mil
40-Pin DIP

Parentheses indicate single-port mode.



44-Pin
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K222U		
40-Pin Plastic Dual-In-Line	73K222U-IP	73K222U-IP
44-Pin Plastic Leaded Chip Carrier	73K222U-IH	73K222U-IH

Notes:

silicon systems®
A TDK Group Company

SSI 73K224L
V.22bis/V.22/V.21, Bell 212A/103 Single-Chip Modem

December 1992

DESCRIPTION

The SSI 73K224L is a highly integrated single-chip modem IC which provides the functions needed to construct a V.22bis compatible modem, capable of 2400 bit/s full-duplex operation over dial-up lines. The SSI 73K224L offers excellent performance and a high level of functional integration in a single 28-pin DIP. This device supports V.22bis, V.22, V.21, Bell 212A and Bell 103 modes of operation, allowing both synchronous and asynchronous communication.The SSI 73K224L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular single-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications normally occur through a separate serial port. The SSI 73K224L is pin and software compatible with the SSI 73K212L and SSI 73K222L single-chip modem ICs, allowing system upgrades with a single component change.

The SSI 73K224L operates from a single +5 V supply for low power consumption.

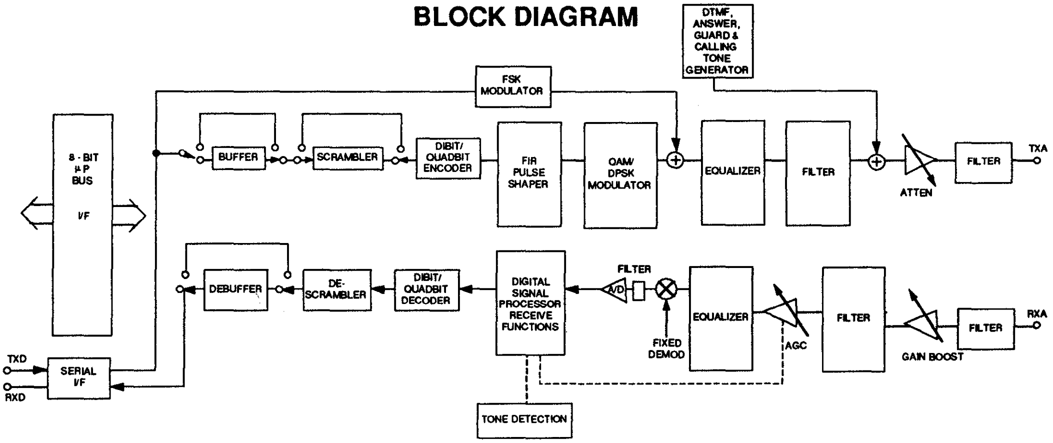
The SSI 73K224L is ideal for use in either free-standing or integral system modem products where full-duplex

(Continued)

FEATURES

- **One-chip multi-mode V.22bis/V.22/V.21 and Bell 212A/103 compatible modem data pump**
- **FSK (300 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Parallel microprocessor bus for control with a wide range of package options**
- **Selectable asynch/synch with internal buffer/ debuffer and scrambler/descrambler functions**
- **All synchronous and asynchronous operating modes (internal, external, slave)**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (16 dB, 1 dB steps), selectable receive boost (+18 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, and signal quality monitors**
- **DTMF, answer and guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit, S1 pattern**
- **CMOS technology for low power consumption (typically 100 mW @ 5V) with power-down mode (15 mW @ 5V)**
- **TTL and CMOS compatible inputs and outputs**

BLOCK DIAGRAM



DESCRIPTION (Continued)

2400 bit/s data communications over the 2–wire switched telephone network is desired. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability.

The SSI 73K224L is designed to be a complete V.22bis compatible modem on a chip. The complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. Many functions were included to simplify implementation of typical modem designs. In addition to the basic 2400 bit/s QAM, 600/1200 bit/s DPSK and 300 bit/s FSK modulator/demodulator sections, the device also includes SYNCH/ASYNCH converters, scrambler/descrambler, call progress tone detect, DTMF tone generator capabilities and handshake pattern detectors. V.22bis, V.22, V.21 and Bell 212A/103 modes are supported (synchronous and asynchronous) and test modes are provided for diagnostics. Most functions are selectable as options and logical defaults are provided.

OPERATION

QAM MODULATOR/DEMODULATOR

The SSI 73K224L encodes incoming data into quad-bits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K224L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation.Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). Adaptive equalization is also used in DPSK modes for optimum operation with varying line conditions.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) are used when this mode is selected. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering corresponds to a 75% square root of raised Cosine frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communication with asynchronous terminals which may communicate at 600,1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01% in DPSK and QAM modes. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where quad-bit/di-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking, and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

Both the SYNC/ASYNC rate converter and the data descrambler are automatically bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted at the same rate as it is input.

PARALLEL BUS INTERFACE

Eight 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Six control registers are read/write memory. The detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

SERIAL CONTROL INTERFACE

The serial command mode allows access to the SSI 73K324 control and status registers via a serial control port. In this mode the A0, A1, and A2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected addresss location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consectuive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

DTMF GENERATOR

The DTMF generator controls the sending of the sixteen standard DTMF tone pairs. The tone pair sent is determined by selecting TRANSMIT DTMF (bit D4) and the 4 DTMF bits (D0-D3) of the TONE register. Transmission of DTMF tones from TXA is gated by the TRANSMIT ENABLE bit of CR0 (bit D1) as with all other analog signals.

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
GND	I	System Ground.
VDD	I	Power supply input, 5V -5% +10%. Bypass with .22 µF and 22 µF capacitors to GND.
VREF	O	An internally generated reference voltage. Bypass with .22 µF capacitor to GND.
ISET	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .22 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{\text{CS}}$.
AD0- AD7	I/O / Tristate	Address/data bus.These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{\text{CS}}$	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{\text{CS}}$ (latched) is not active. $\overline{\text{CS}}$ is latched on the falling edge of ALE.
CLK	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{\text{INT}}$	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{\text{INT}}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{\text{RD}}$	I	Read. A low requests a read of the SSI 73K224L internal registers. Data cannot be output unless both $\overline{\text{RD}}$ and the latched $\overline{\text{CS}}$ are active or low.
RESET	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{\text{WR}}$	I	Write. A low on this informs the SSI 73K224L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{\text{WR}}$. No data is written unless both $\overline{\text{WR}}$ and the latched $\overline{\text{CS}}$ are active (low).

Note: The serial control mode is provided in the parallel versions by tying ALE high and $\overline{\text{CS}}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	TYPE	DESCRIPTION
EXCLK	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	O/Tristate	Receive Clock. Tri-stateable. The falling edge of this clock output is coincident with the transitions in the serial received data output. The rising edge of RXCLK can be used to latch QAM or DPSK valid output data. RXCLK will be active as long as a carrier is present.
RXD	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	O/Tristate	Transmit Clock. Tri-stateable. This signal is used in synchronous transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active.
TXD	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (2400/1200/600 bit/s or 300 baud) no clocking is necessary. DPSK data must be +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	I	Received modulated analog signal input from the phone line.
TXA	O	Transmit analog output to the phone line.
XTL1	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTL2 can also be driven from an external clock.
XTL2	I/O	

PIN DESCRIPTION (continued)

SERIAL MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
A0-A2	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	I	Read. A low on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addresses register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	I	Write. A low on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

REGISTER DESCRIPTIONS

Eight 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K224L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ EXTENDED OVERSPEED	DTMF0/GUARD/ ANSWER
CONTROL REGISTER 2 CR2	100		SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3 CR3	101	TXDALT	TRISTATE TX/RXCLK		RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
SPECIAL REGISTER SR	101		TX BAUD CLOCK	RX UNSCR. DATA		TXD SOURCE	SQ SELECT 1	SQ SELECT 0	
ID REGISTER ID	110	ID	ID	ID	ID	USER DEFINABLE PERSONALITY			

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

SSI 73K224L
V.22bis/V.22/V.21, Bell 212A/103
Single-Chip Modem

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
		QAM: 0=2400 BIT/S DPSK: 0=1200 BIT/S 1=600 BIT/S FSK: 0=103 MODE 1=V.21	10=QAM 00=DPSK 01=FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYCH 8 BITS/CHAR 0101=ASYCH 9 BITS/CHAR 0110=ASYCH 10 BITS/CHAR 0111=ASYCH 11 BITS/CHAR 1X00=FSK			0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN QAM/DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARKS DETECT	CARRIER DETECT	ANSWER TONE DETECT	CP TONE DETECT	SIGNAL QUALITY INDICATOR
		0=SIGNAL BELOW THRESHOLD 1=ABOVE THRESHOLD	0=NOT PRESENT 1=PATTERN FOUND	OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				0=GOOD 1=BAD
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2	DTMF1/ EXTENDED OVERSPEED	DTMF0/ GUARD/ ANSWER
		RXD PIN 0=NORMAL 1=OPEN	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS			0=1800 Hz G.T. 2225 Hz ANS TONE GENERATED. 1=550 Hz G.T. 2100 Hz ANS TONE GENERATED & DETECTED (V.21, V.22)
CONTROL REGISTER 2 CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE
			0=ACCESS CR3 1=ACCESS SPECIAL REGISTER	0=DSP IN DEMOD MODE 1=DSP IN CALL PROGRESS MODE	0=NORMAL DOTTING 1=S1	0=RX=TX 1=RX=16 WAY	0=DSP INACTIVE 1=DSP ACTIVE	0=ADAPT EQ ACTIVE 1=ADAPT EQ FROZEN	0=ADAPT EQ IN INIT 1=ADAPT EQ OK TO ADAPT
CONTROL REGISTER 3 CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
		ALTERNATE TRANSMIT DATA SOURCE	0=NORMAL 1=TRISTATE		0=NO BOOST 1=18 dB BOOST	0000-1111, SETS TRANSMIT ATTENUATOR 16 dB RANGE DEFAULT=0100 ≈ -10 dBm0			
SPECIAL REGISTER SR	101	▨	TX BAUD CLOCK	RX UNSCR. DATA	▨	TXD SOURCE	SQ SELECT1	SQ SELECT0	▨
			OUTPUTS TXBAUD CLOCK	OUTPUTS UNSCR. DATA		0=TXD PIN 1=TXALT BIT	00=10^{-5} BER 01=10^{-6} BER 10=10^{-4} BER 11=10^{-3} BER		
ID REGISTER 10	110	ID	ID	ID	ID	▨	▨	▨	▨

00XX=73K212, 322, 321
01XX=73K221, 302
10XX=73K222
1100=73K224
1110=73K324
1101=73K312

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band).
		1	Selects originate mode (transmit in low band,receive in high band).
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone or DTMF.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 600,1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 600, 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 X 0 0	Selects FSK operation.
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	Modulation Option	0	QAM selects 2400 bit/s. DPSK selects 1200 bit/s. FSK selects 103 mode.
		1	DPSK selects 600 bit/s. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same carrier frequency as the transmitter. To squelch the TXA pin, TRANSMIT ENABLE bit as well as Tone Reg bit D2 must be low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	Clock Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK/ QAM modes only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler	0	Selects normal operation. DPSK and QAM data is passed through scrambler.
		1	Selects Scrambler Bypass. Bypass DPSK and QAM data is routed around scrambler in the transmit path.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{\text{INT}}$ pin. All interrupts are normally disabled in power down mode.
		1	Enables $\overline{\text{INT}}$ output. An interrupt will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONE DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Signal Quality Indicator	0	Indicates normal received signal.
		1	Indicates low received signal quality (above average error rate). Interacts with special register bits D2, D1.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress bandwidth.

DETECT REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARR. DETECT	ANSWER TONE DETECT	CALL PROG.	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	Answer Tone Received	0	No answer tone detected.
		1	In Call Init mode, indicates detection of 2225 Hz answer tone in Bell mode (TR bit D0=0) or 2100 Hz if in CCITT mode (TR bit D0=1). The device must be in originate mode for detection of answer tone. Both answer tones are detected in demod mode.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0	No S1 pattern being received.
		1	S1 pattern detected. Should be time qualified by software. S1 pattern is defined as a double di-bit (001100..) unscrambled 1200 bit/s DPSK signal. Pattern must be aligned with baud clock to be detected.
D7	Receive Level Indicator	0	Received signal level below threshold, (typical ≈ -25 dBm0); can use receive gain boost (+18 dB).
		1	Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		X X 1 X	Transmit DTMF tones.
		X 1 0 0	Select Bell mode answer tone. Interacts with DR bit D2 and TR bit D5.
(Continued)		X 1 0 1	Select CCITT mode answer tone. Interacts with DR bit D2 and TR bit D5.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer/ Guard Tone	D6 D5 D4 D0	D0 interacts with bits D6, D5, and D4 as shown.
		1 0 0 0	Select 1800 Hz guard tone.
		1 0 0 1	Select 550 Hz guard tone.
D1	DTMF 1/ Extended Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM or DPSK +1.0% -2.5%. (normal)
		0 1	Asynchronous QAM or DPSK +2.3% -2.5%. (extended overspeed)
D2	DTMF 2/ 4 WIRE FDX	D4 D2	
		0 0	Selects 2 wire duplex or half duplex
		0 1	D2 selects 4 wire full duplex in the modulation mode selected. The receive path corresponds to the ANS/ ORIG bit CR0 D0 in terms of high or low band selection. The transmitter is in the same band as the receiver, but does not have magnitude filtering or equalization on its signal as in the receive path.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

<table>
<tr><th>BIT NO.</th><th>NAME</th><th>CONDITION</th><th>DESCRIPTION</th></tr>
<tr><td>D3, D2,
D1, D0</td><td>DTMF 3,
2, 1, 0</td><td>D3 D2 D1 D0
0 0 0 0 -
1 1 1 1</td><td>Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:
<table>
<tr><th>KEYBOARD EQUIVALENT</th><th>DTMF CODE
D3 D2 D1 D0</th><th>TONES
LOW HIGH</th></tr>
<tr><td>1</td><td>0 0 0 1</td><td>697 1209</td></tr>
<tr><td>2</td><td>0 0 1 0</td><td>697 1336</td></tr>
<tr><td>3</td><td>0 0 1 1</td><td>697 1477</td></tr>
<tr><td>4</td><td>0 1 0 0</td><td>770 1209</td></tr>
<tr><td>5</td><td>0 1 0 1</td><td>770 1336</td></tr>
<tr><td>6</td><td>0 1 1 0</td><td>770 1477</td></tr>
<tr><td>7</td><td>0 1 1 1</td><td>852 1209</td></tr>
<tr><td>8</td><td>1 0 0 0</td><td>852 1336</td></tr>
<tr><td>9</td><td>1 0 0 1</td><td>852 1477</td></tr>
<tr><td>0</td><td>1 0 1 0</td><td>941 1336</td></tr>
<tr><td>*</td><td>1 0 1 1</td><td>941 1209</td></tr>
<tr><td>#</td><td>1 1 0 0</td><td>941 1477</td></tr>
<tr><td>A</td><td>1 1 0 1</td><td>697 1633</td></tr>
<tr><td>B</td><td>1 1 1 0</td><td>770 1633</td></tr>
<tr><td>C</td><td>1 1 1 1</td><td>852 1633</td></tr>
<tr><td>D</td><td>0 0 0 0</td><td>941 1633</td></tr>
</table></td></tr>
<tr><td>D4</td><td>TX DTMF
(Transmit
DTMF)</td><td>0</td><td>Disable DTMF.</td></tr>
<tr><td></td><td></td><td>1</td><td>Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.</td></tr>
</table>

Note: DTMF0 - DTMF2 should be set to an appropriate state after DTMF dialing to avoid unintended operation.

TONE REGISTER (Continued)

D7	D6	D5	D4	D3	D2	D1	D0	
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 4 WIRE FDX	DTMF 1/ EXTENDED OVER-SPEED	DTMF 0/ ANSWER/ GUARD

BIT NO.	NAME	CONDITION	DESCRIPTION
D5	Transmit Answer Tone	D5 D4 D0	D5 interacts with bits D4 and D0 as shown. Also interacts with DR bit D2 in originate mode. See Detect Register description.
		0 0 X	Disables answer tone generator.
		1 0 0	In answer mode, a Bell 2225 Hz tone is transmitted continuously when the Transmit Enable bit is set.
		1 0 1	Likewise, a CCITT 2100 Hz answer tone is transmitted.
D6	Transmit Guard Tone	0	Disables guard tone generator.
		1	Enables guard tone generator. (See D0 for selection of guard tones.) Bit D4 must be zero.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This bit is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.

CONTROL REGISTER 2 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Transmit S1	0	The transmitter when placed in alternating mark/space mode transmits 0101...... scrambled or not dependent on the bypass scrambler bit.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, and in DPSK or QAM, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the various mode bits. Both answer tones are detected in demod mode concurrently; TR-D0 is ignored.
		1	The DSP decodes unscrambled mark, answer tone and call progress tones.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the SPECIAL REGISTER. See the SPECIAL REGISTER for details.
D7	Not used at this time	0	Only write zero to this bit.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	TXDALT	TRISTATE TX/RXCLK	▨	RECEIVE BOOST ENABLE	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1,D0	Transmit Attenuator	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Sets the attenuation level of the transmitted signal in 1dB steps. The default (D3-D0=0100) is for a transmit level of -10 dBm0 on the line with the recommended hybrid transmit gain. The total range is 16 dB.
D4	Receive Gain Boost	0	18 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D5	Not used at this time	0	Only write zero to this bit.
D6	TRISTATE TXCLK/RXCLK	0	TXCLK and RXCLK are driven.
		1	TXCLK and RXCLK are tristated.
D7	TXDALT	Spec. Reg. Bit D3=1	Alternate TX data source. See Special Register.

SPECIAL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
SR 101	▨	TXBAUD CLOCK	RXUN-DSCR DATA	▨	TXD SOURCE	SIGNAL QUALITY LEVEL SELECT1	SIGNAL QUALITY LEVEL SELECT0	▨

BIT NO.	NAME	DESCRIPTION
D7, D4, D0		NOT USED AT THIS TIME. Only write ZEROs to these bits.
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.
D5	RXUNDSCR DATA	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.
D3	TXD SOURCE	This bit selects the transmit data source; either the TXD pin if ZERO or the TXDALT if this bit is a ONE. The TRANSMIT PATTERN bits D7 and D6 in CR1 override either of these sources.
D2, D1	SIGNAL QUALITY LEVEL SELECT	The signal quality indicator is a logical ZERO when the signal received is acceptable for low error rate reception. It is determined by the value of the Mean Squared Error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a ONE constantly. The SQI bit and threshold selection are valid for QAM and DPSK only and indicates typical error rate.

D2	D1	THRESHOLD VALUE	UNITS
0	0	10^{-5}	BER (default)
0	1	10^{-6}	BER
1	0	10^{-4}	BER
1	1	10^{-3}	BER

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a ONE and addressing CR3. This register provides functions to the 73K224L user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a ZERO.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 3	ID 2	ID 1	ID 0	USER DEFINABLE PERSONALITY			

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5, D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212(L), 73K321L or 73K322L
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 1	SSI 73K312L
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD+0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.22			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.22			µF
VDD Bypass capacitor 1	(VDD to GND)	0.22			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
XTL1 Load Capacitance	Depends on crystal requirements		18	39	pF
XTL2 Load Capacitance	Depends on crystal requirements		18	27	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		85	°C

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
	ISET Resistor = 2 MΩ				
IDD1, Active	Operating with crystal oscillator,		18	25	mA
IDD2, Idle	< 5 pF capacitive load on CLK pin		3	5	mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VDD			100	µA
IIL, Input Low Current	VI = 0V	-200			µA
Reset Pull-down Current	Reset = VDD	2		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
RXD Tri-State Pull-up Curr.	RXD = GND	-2		-50	µA
Capacitance					
Maximum Capacitive Load					
CLK	Maximum permitted load			25	pF
Input Capacitance	All Digital Inputs			10	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks ATT=0100 (default)	-11.5	-10.0	-9	dBm0
FSK Modulator/Demodulator					
Output Freq. Error	CLK = 11.0592 MHz	-.31		+.20	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
TXA Output Distortion	All products through BPF			-45	dB
Output Bias Distortion at RXD	Dotting Pattern measured at RXD Receive Level -20 dBm, SNR 20 dB	-10		+10	%
Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
Sum of Bias Distortion and Output Jitter	Integrated for 5 seconds	-17		+17	%
Answer Tone Generator (2100 or 2225 Hz)					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21	-11.5	-10	-9	dBm0
Output Distortion	Distortion products in receive band			-40	dB
DTMF Generator	Not in V.21				
Freq. Accuracy		-0.03		+0.25	%
Output Amplitude	Low Band, ATT = 0100, DPSK Mode	-10		-8	dBm0
Output Amplitude	High Band, ATT = 0100, DPSK Mode	-8		-6	dBm0
Twist	High-Band to Low-Band, DPSK Mode	1.0	2.0	3.0	dB
Receiver Dynamic Range	Refer to Performance Curves	-43		-3.0	dBm0
Call Progress Detector	In Call Init mode				
Detect Level	460 Hz test signal	-34		0	dBm0
Reject Level				-40	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			25	ms

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect		**Receive Gain = On for lower input level measurements**				
Threshold		All Modes	-48		-43	dBm0
Hysteresis		All Modes	2			
Delay Time	FSK	70 dBm0 to -6 dBm0	25		37	ms
		70 dBm0 to -40 dBm0	25		37	ms
	DPSK	-70 dBm0 to -6 dBm0	7		17	ms
		-70 dBm0 to -40 dBm0	7		17	ms
	QAM	-70 dBm0 to -6 dBm0	25		37	ms
		-70 dBm0 to -40 dBm0	25		37	ms
Hold Time	FSK	-6 dBm0 to -70 dBm0	25		37	ms
		-40 dBm0 to -70 dBm0	15		30	ms
	DPSK	-6 dBm0 to -70 dBm0	20		29	ms
		-40 dBm0 to -70 dBm0	14		21	ms
	QAM	-6 dBm0 to -70 dBm0	25		32	ms
		-40 dBm0 to -70 dBm0	18		28	ms
Answer Tone Detectors		**DPSK Mode**				
Detect Level			-48		-43	dBm0
Detect Time		Call Init Mode, 2100 or 2225 Hz	6		50	ms
Hold Time			6		50	ms
Pattern Detectors		**DPSK Mode**				
S1 Pattern						
Delay Time		For signals from -6 to -40 dBm0,	10		55	ms
Hold Time		-6 to -40 dBm0, Demod Mode	10		45	ms
Unscrambled Mark						
Delay Time		For signals from -6 to -40	10		45	ms
Hold Time		call Init Mode	10		45	ms
Receive Level Indicator						
Detect On			-22		-28	dBm0
Valid after Carrier Detect		DPSK Mode	1	4	7	ms
Output Smoothing Filter						
Output Impedance		TXA pin		200	300	Ω
Output load		TXA pin; FSK Single	10			KΩ
		Tone out for THD = -50 dB in .3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy		4 kHz, Guard Tones off			-35	dBm0
		10 kHz, Guard Tones off			-55	dBm0
		12 kHz, Guard Tones off			-65	dBm0

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Anti Alias Low Pass Filter					
Out of Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Level at RXA pin with receive Boost Enabled				
	Scrambled data at 2400 bit/s in opposite band		-14		dBm
	Sinusoids out of band		-9		dBm
Transmit Attenuator					
Range of Transmit Level	Default ATT=0100 (-10 dBm0) 1111-000	-21		-6	dBm0
Step Accuracy		-0.15		+0.15	dB
Output Impedance			200	300	Ω
Clock Noise					
	TXA pin; 153.6 kHz			1.5	mVrms
Carrier Offset					
Capture Range	Originate or Answer		±5	±7	Hz
Recovered Clock					
Capture Range	% of frequency (originate or answer)	-0.02		+0.02	%
Guard Tone Generator					
Tone Accuracy	550 Hz		+1.2		%
	1800 Hz		-0.8		
Tone Level	550 Hz	-4.5	-3.0	-1.5	dB
(Below QAM/DPSK Output)	1800 Hz	-7.5	-6.1	-4.5	dB
Harmonic Distortion	550 Hz			-50	dB
(700 to 2900 Hz)	1800 Hz			-50	dB
Timing (Refer to Timing Diagrams)					
Parallel Mode					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	10			ns
TLC	ALE Low to $\overline{RD}$/$\overline{WR}$ Low	40			ns
TCL	$\overline{RD}$/$\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low			90	ns
TLL	ALE width	25			ns
TRDF	Data float after $\overline{RD}$ High			40	ns
TRW	$\overline{RD}$ width	70			ns

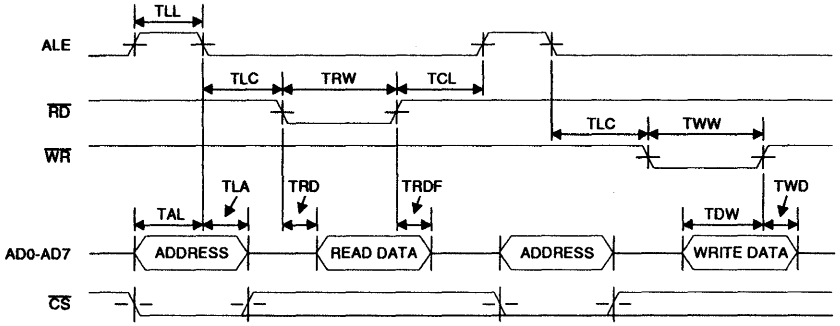
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Parallel Mode (Continued)					
TWW	$\overline{\text{WR}}$ width	70			ns
TDW	Data setup before $\overline{\text{WR}}$ High	70			ns
TWD	Data hold after $\overline{\text{WR}}$ High	20			ns
Serial Mode					
TRCK	Clock High after $\overline{\text{RD}}$ Low	250		T1	ns
TAR	Address setup before $\overline{\text{RD}}$ Low	0			ns
TRA	Address hold after $\overline{\text{RD}}$ Low	350			ns
TRD	$\overline{\text{RD}}$ to Data valid			300	ns
TRDF	Data float after $\overline{\text{RD}}$ High			40	ns
TCKDR	Read Data out after Falling Edge of EXCLK			300	ns
TWW	$\overline{\text{WR}}$ width	350			ns
TAW	Address setup before $\overline{\text{WR}}$ Low	50			ns
TWA	Address hold after Rising Edge of $\overline{\text{WR}}$	50			ns
TCKDW	Write Data hold after Falling Edge of EXCLK	200			ns
TCKW	$\overline{\text{WR}}$ High after Falling Edge of EXCLK	330		T1 + T2	ns
TDCK	Data setup before Falling Edge of EXCLK	50			ns
T1, T2	Minimum Period	500			ns

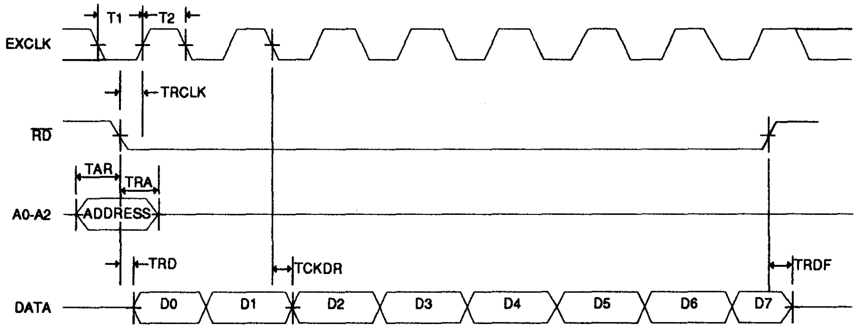
NOTE: T1 and T2 are the low/high periods, respectively, of EXCLK in serial mode.

TIMING DIAGRAMS

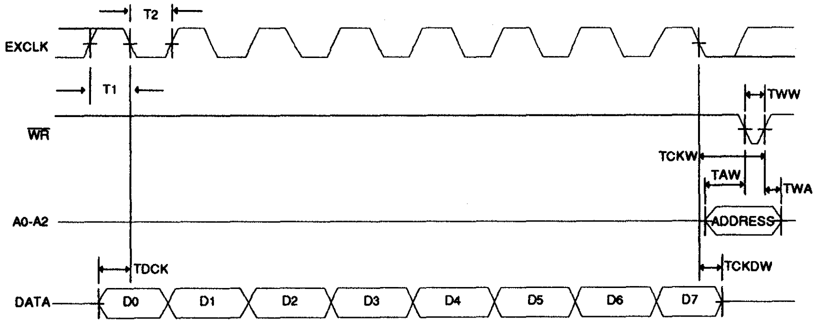
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 V design and one for a single 5 V design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

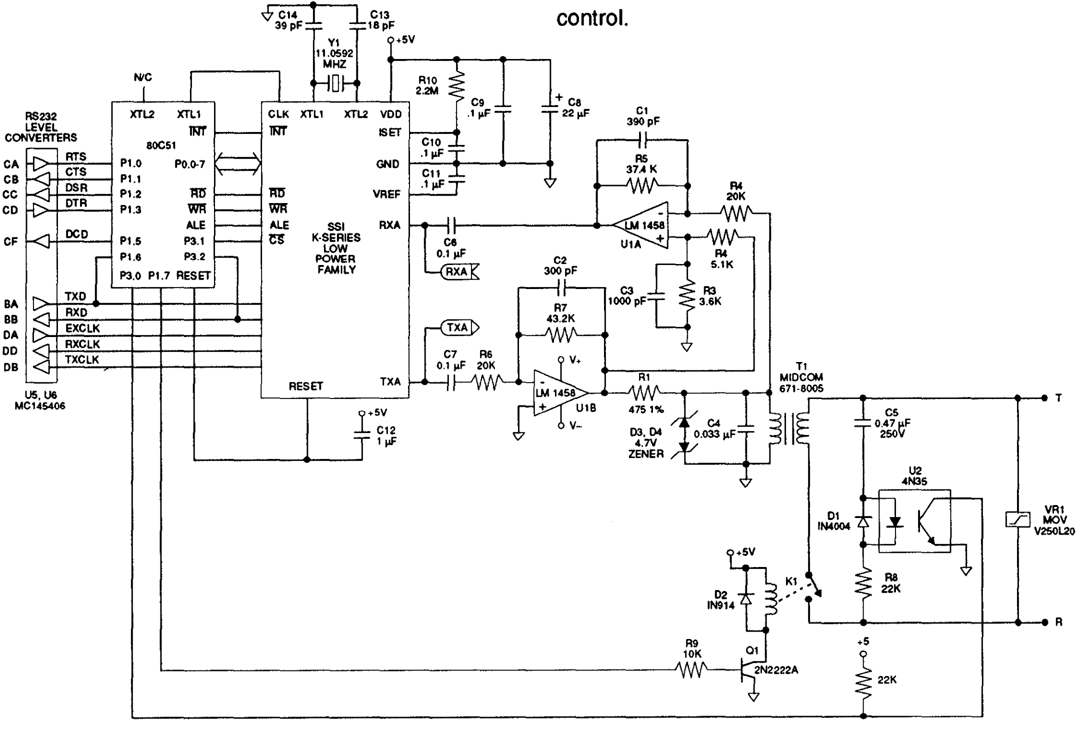


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

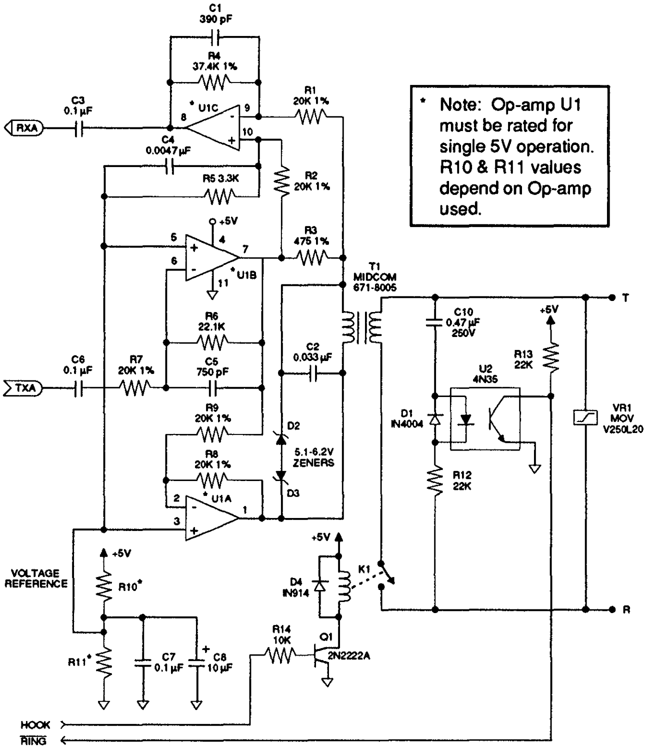
DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.22 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. The ISET resistor and capacitor should be mounted near the ISET pin, away from digital signals. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Hayes SmartModem™ 2400 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

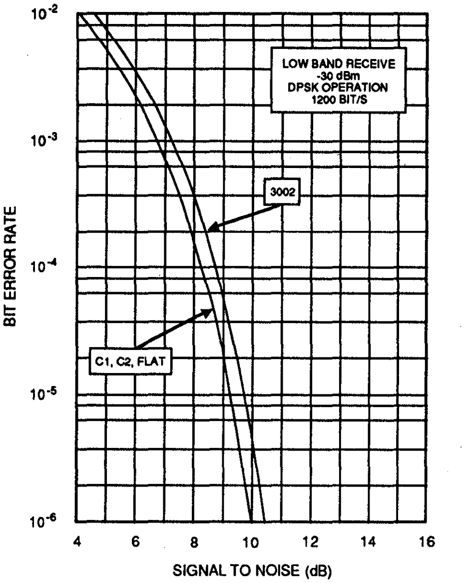
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

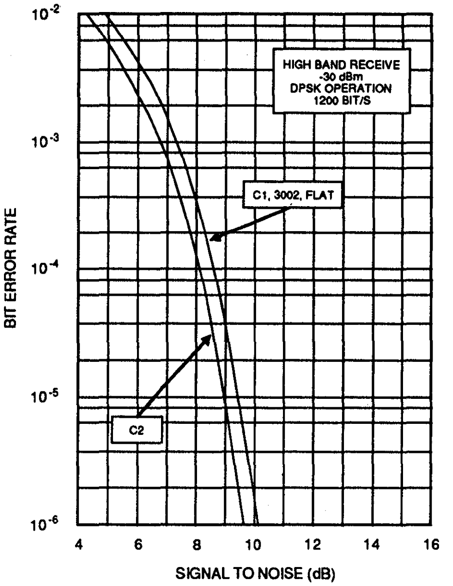
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

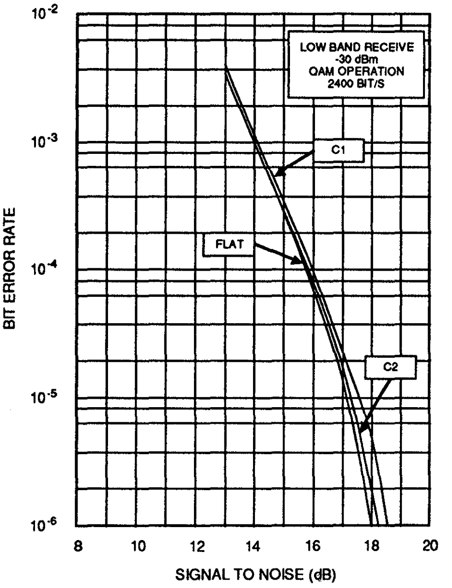
SSI 73K224L BER vs S/N-DPSK LOW BAND



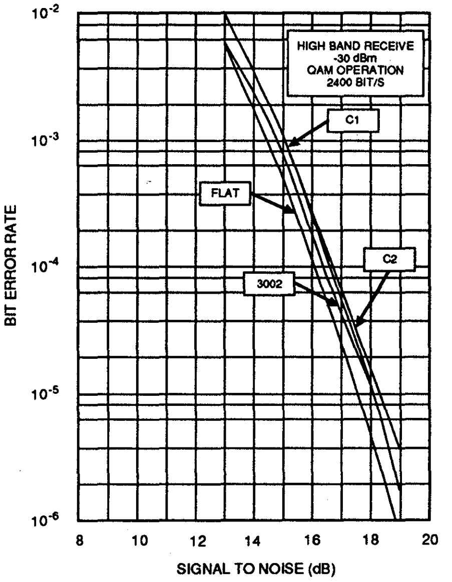
SSI 73K224L BER vs S/N-DPSK HIGH BAND

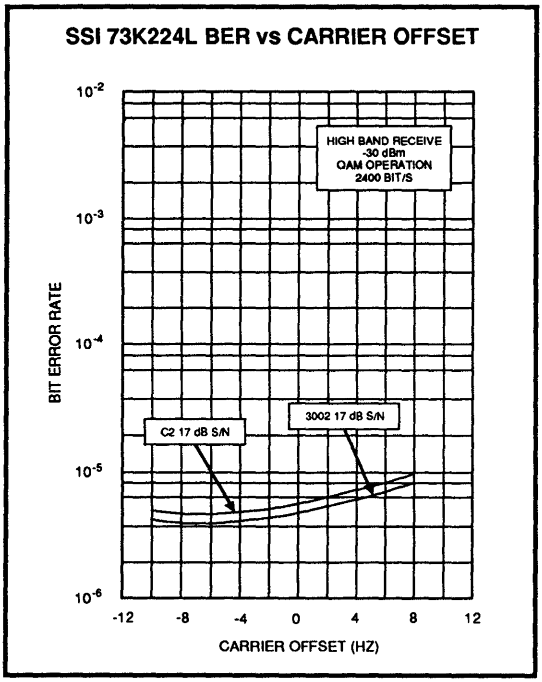


SSI 73K224L
BER vs S/N-QAM-LOW BAND



SSI 73K224L
BER vs S/N-QAM-HIGH BAND

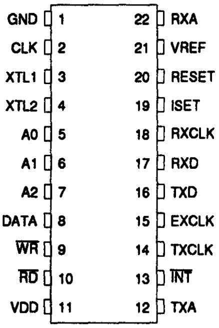



SSI 73K224L BER vs CARRIER OFFSET
HIGH BAND RECEIVE
-30 dBm
QAM OPERATION
2400 BIT/S
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
C2 17 dB S/N
3002 17 dB S/N
-12
-8
-4
0
4
8
12
CARRIER OFFSET (HZ)

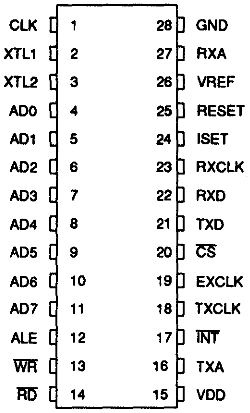
SSI 73K224L
V.22bis/V.22/V.21, Bell 212A/103
Single-Chip Modem

PACKAGE PIN DESIGNATIONS

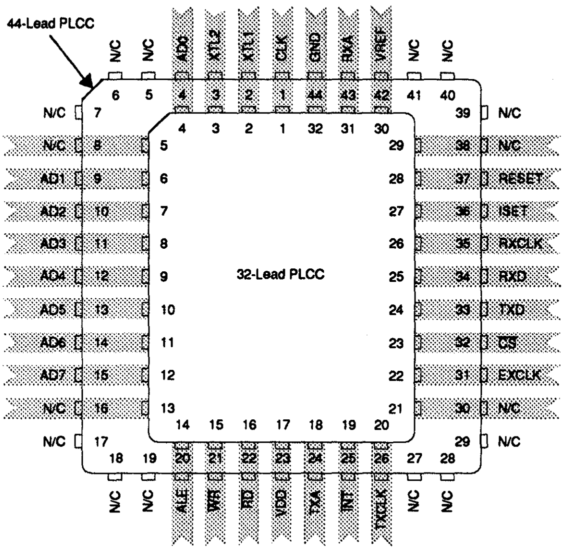
(Top View)



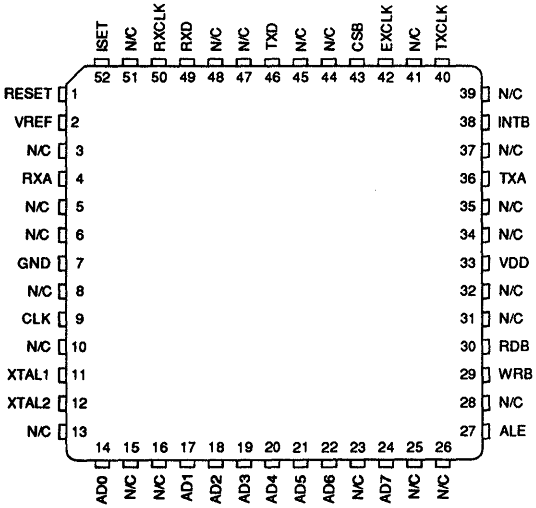
400-Mil
22-Pin DIP



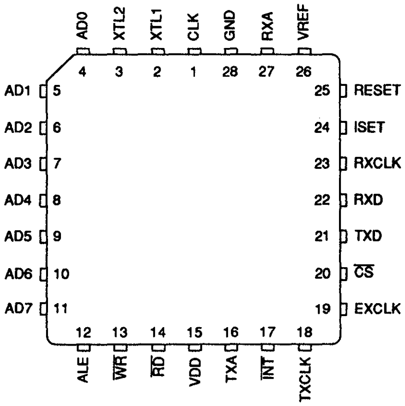
600-Mil
28-Pin DIP



32, 44-Pin PLCC



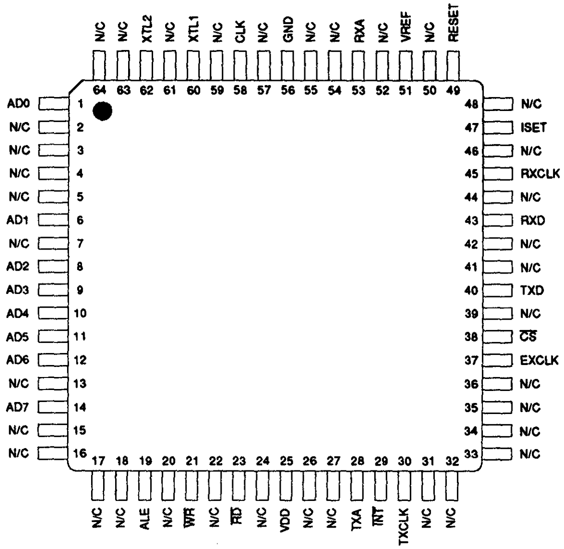
52-Lead QFP



28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73K224L
V.22bis/V.22/V.21, Bell 212A/103
Single-Chip Modem



64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K224L with Serial Bus Interface		
22-Pin Plastic Dual-In-Line	73K224LS-IP	73K224LS-IP
SSI 73K224L with Parallel Bus Interface		
28-Pin Plastic Dual-In-Line	73K224L-IP	73K224L-IP
28-Pin Plastic Leaded Chip Carrier	73K224L-28IH	73K224L-28IH
32-Pin Plastic Leaded Chip Carrier	73K224L-32IH	73K224L-32IH
44-Pin Plastic Leaded Chip Carrier	73K224L-IH	73K224L-IH
52-Lead Quad Flat Pack Package	73K224L-IG	73K224L-IG
64-Lead Thin Quad Flat Pack Package	73K224L-IGT	73K224L-IGT

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914

Protected by the following patents:
(4,777,453), (4,789,995), (4,870,370), (4,847,868), (4,866,739)

Notes:

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A TDK Group Company

SSI 73K302L
Bell 212A, 103, 202 Single-Chip Modem
Preliminary Data

December 1992

DESCRIPTION

The SSI 73K302L is a highly integrated single-chip modem IC which provides the functions needed to construct a Bell 202, 212A and 103 compatible modem. The SSI 73K302L is an enhancement of the SSI 73K212L single-chip modem with Bell 202 mode features added. The 73K302L is capable of 1200 or 0-300 bit/s full-duplex operation over dial-up lines. 4-wire full-duplex capability and a low speed back channel are also provided in Bell 202 mode. The SSI 73K302L recognizes and generates a 900 Hz soft carrier turn-off tone, and allows 103 for 300 bit/s FSK operation. The SSI 73K302L integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28 or 22–pin DIP configuration. The SSI 73K302L operates from a single +5V supply with very low power consumption.

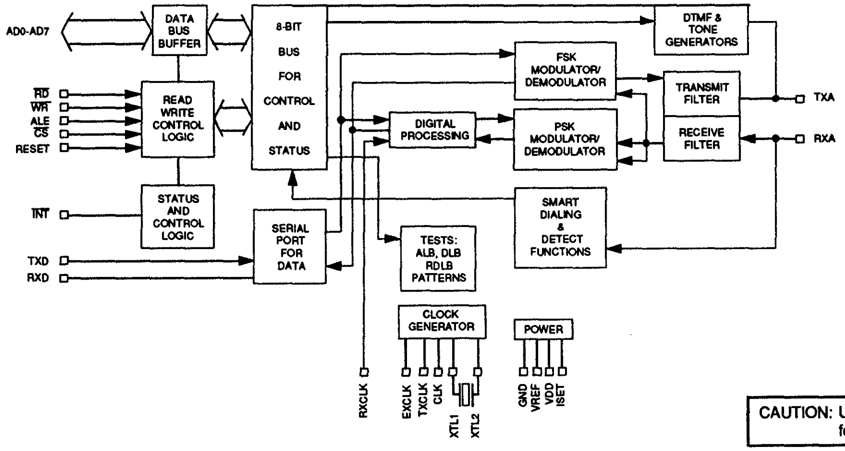
The SSI 73K302L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes, and a tone generator capable of producing DTMF, answer, and 900 Hz soft carrier turn-off tone. This device supports Bell 202, 212A and 103 modes of operation, allowing both

(Continued)

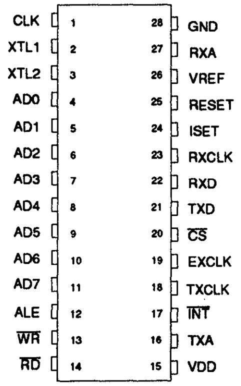
FEATURES

- **One-chip Bell 212A, 103 and 202S/T standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK), 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-150 bit/s back channel**
- **Full-duplex 4-wire operation in Bell 202 mode**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial (22-pin DIP) or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2225 Hz), soft carrier turn-off (SCT), and FSK mark detectors**
- **DTMF, answer, and SCT tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **CMOS technology for low power consumption using 35 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

synchronous and asynchronous communications. The SSI 73K302L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K302L is ideal for use in either free standing or integral system modem products where multi-standard data communications is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a modem controller, and RS232 level converter for a typical system.

Tri-mode capability in one-chip allows full-duplex Bell 212 and 103 operation or assymetrical Bell 202S operation over the 2-wire switched telephone network. 202T mode full-duplex operation at 1200 bit/s is also possible when operating on 4-wire leased lines.

A soft carrier turn-off feature facilitates fast line turn around when using the 202S mode for half-duplex applications.

The SSI 73K302L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K302L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 bit/s +1.0%, 2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 bit/s ± .01% (±.01% is the required synchronous data rate accuracy).

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The ASYNC/ASYNC converter will reinsert any deleted stop bits and output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The Bell 212A standard defines synchronous operation at 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73K302L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K302L uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. Bell 103 mode uses 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space). Bell 202 mode uses 1200 and 2200 Hz for the main channel and 387 and 487 Hz for the back channel. The modulation rate of the back channel is up to 150 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the 103 or 202 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available in the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K302L control and status registers via a serial command port. In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brough low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 900 Hz soft carrier turn-off tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect lower quality call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

SOFT CARRIER TURN-OFF TONE GENERATOR

The soft carrier turn-off tone generator will output a 900 Hz tone. When activated in Bell 202 main channel transmit mode, the output signal will shift to 900 Hz, maintaining phase continuity during the transition.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with .1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK mode only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K302L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{WR}$	13	-	I	Write. A low on this informs the SSI 73K302L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{WR}$. No data is written unless both $\overline{WR}$ and the latched $\overline{CS}$ are active low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	-	10	I	Read. A low on this input informs the SSI 73K302L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	-	9	I	Write. A low on this input informs the SSI 73K302L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

The serial control mode is provided in the parallel control versions by tying ALE high and $\overline{CS}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

PIN DESCRIPTION (Continued)

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used only in synchronous DPSK transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In Bell 202 mode a clock which is 16 x 1200 or 16 x 150 baud data rate is output.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock.This signal is used only in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In Bell 202 mode the output is a 16 x 1200 baud clock or 16 x 150 baud to drive a UART.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K302L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. 202	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF/ 202T FDX	DTMF1/ OVERSPEED	DTMF0/ SPEC. TONE/ ANSWER TONE/ SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	**AD2 - AD0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
CONTROL REGISTER 0 CR0	**000**	**MODULATION OPTION**		**TRANSMIT MODE 3**	**TRANSMIT MODE 2**	**TRANSMIT MODE 1**	**TRANSMIT MODE 0**	**TRANSMIT ENABLE**	**ORIGINATE/ ANSWER**
		0=103 FSK 1=202 FSK		0000=PWR DOWN 1100=FSK 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK BELL 103 OR 202				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	IN 212, 103 MODES: 0=ANSWER 1=ORIGINATE IN 202 MODE: 0=RECEIVE @ 1200 BIT/S, TRANSMIT @ 150 BIT/S 1=RECEIVE @ 150 BIT/S, TRANSMIT @ 1200 BIT/S
CONTROL REGISTER 1 CR1	**001**	**TRANSMIT PATTERN 1**	**TRANSMIT PATTERN 0**	**ENABLE DETECT INTERRUPT**	**BYPASS SCRAMBLER/ ADD PH. EQ.**	**CLK CONTROL**	**RESET**	**TEST MODE 1**	**TEST MODE 0**
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=ENABLE 1=DISABLE	0=NORMAL 1=BYPASS SCRAMBLER 1=ADD EXTRA PHASE EQ. IN 202 ONLY	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	**010**			**RECEIVE DATA**	**UNSCR. MARKS**	**CARRIER DETECT**	**SPECIAL TONE**	**CALL PROGRESS**	**LONG LOOP**
				OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			
TONE CONTROL REGISTER TR	**011**	**RXD OUTPUT CONTROL**	**TRANSMIT SCT TONE**	**TRANSMIT ANSWER TONE**	**TRANSMIT DTMF**	**DTMF3**	**DTMF2/ 202T FDX**	**DTMF1/ OVERSPEED**	**DTMF0/ SPECIAL TONE**
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.	0=NORMAL OPERATION 1=FULL DUPLEX IN 202 MODE	0=1% 1=2.5%	0=900 HZ SCT TONE IF IN ANSWER MODE =2225 HZ ANSWER TONE IN 103 OR 212 ORIGINATE MODES 1=FSK MARK
ID REGISTER 10	**110**	**ID**	**ID**	**ID**	**ID**				
00XX=73K212, 322, 321 01XX=73K221, 302 10XX=73K222 1100=73K224 1110=73K324 1101=73K312									

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in Bell 202 mode, receive at 1200 bit/s and transmit at 150 bit/s).
		1	Selects originate mode (transmit in low band, receive in high band or in Bell 202 mode, receive at 150 bit/s and transmit at 1200 bit/s).
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
		D5 D4 D3 D2	
D5, D4,D3, D2	Transmit Mode	0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects 103 or 202 FSK operation.

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		X 0 X	DPSK asynchronous mode at 1200 bit/s.
		0 1 1	FSK Bell 103 mode.
		1 1 1	FSK Bell 202 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low. Not supported in FDX202 mode.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4*	Bypass Scrambler/ Add Phase Equalization	0	Selects normal operation. DPSK data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path. In Bell 202 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{\text{INT}}$ pin.
		1	Enables $\overline{\text{INT}}$ output. An interrupt will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

* D4 should always be set to 1 when receiving 1200 bit/s data and to 0 when transmitting 1200 bit/s data in 202 mode.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010			RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2225 Hz answer tone if D0 of TR=0 and the device is in Bell 103 or 212A originate mode.
			(2) Soft carrier turn-off tone if D0 of TR=0 and the device is in Bell 202 answer mode.
			(3) an FSK mark in the mode the device is set to receive if D0 of TR is set to 1.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark Detect	0	No unscrambled mark.
		1	(DPSK only) Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 202 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Special Tone Detect/Select	D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
		0 1 X	Transmit DTMF tones.
		0 0 0	2225 Hz answer tone will be detected in D2 of DR if originate mode is selected in CR0.
			900 Hz SCT tone will be detected in D2 of DR if Bell 202 answer mode is selected in CR0.
		X 0 1	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		1 0 0	2225 Hz answer tone will be generated when in answer mode and transmit enable is selected in CR0.
		1 0 1	2100 Hz answer tone will be generated when in answer mode and transmit enable is selected in CR0.
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous DPSK 1200 bit/s +1.0% -2.5%.
		0 1	Asynchronous DPSK 1200 bit/s +2.3% -2.5%.
D2	DTMF2/202T FDX	0	Enables 202 half-duplex operation if D4=0
		1	Enables 202 full-duplex operation if D4=0
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0	
		0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW	TONES HIGH
1	0 0 0 1	697	1209
2	0 0 1 0	697	1336
3	0 0 1 1	697	1477
4	0 1 0 0	770	1209
5	0 1 0 1	770	1336
6	0 1 1 0	770	1477
7	0 1 1 1	852	1209
8	1 0 0 0	852	1336
9	1 0 0 1	852	1477
0	1 0 1 0	941	1336

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT SOFT CARRIER TURN-OFF TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ 202T FDX	DTMF 1/ OVER-SPEED	DTMF 0/ SPECIAL TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION						
D3, D2, D1, D0 (cont.)			KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
			*	1	0	1	1	941	1209
			#	1	1	0	0	941	1477
			A	1	1	0	1	697	1633
			B	1	1	1	0	770	1633
			C	1	1	1	1	852	1633
			D	0	0	0	0	941	1633
D4	Transmit DTMF	0	Disable DTMF.						
		1	Activate DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.						
D5	Transmit Answer Tone	0	Disables answer tone generator.						
		1	Enables answer tone generator. A 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. To transmit answer tone, the device must be in answer mode.						
D6	Transmit SCT Tone	0	Disables SCT tone generator.						
		1	Transmit SCT tone in Bell 202 mode.						
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.						
		1	Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.						

Notes for Tone Register use:

1. To detect SCT tone, 202 answer mode must be selected. To transmit SCT tone, 202 originate mode must be selected.
2. For answer tone detection, 103 or 212 originate mode must be active. To transmit answer tone, the 73K302 must be in 103 or 212 answer mode.
3. After completion of DTMF dialing, bit D2 should be reset unless 202 full-duplex mode is selected.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID				

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212(L), 73K321L or 73K322L or 73K321L
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temp.		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 kHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTL1, 2 Load Capacitors	Depends on crystal	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING
(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
DPSK Modulator					
Carrier Suppression	Measured at TXA	45			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Soft Carrier Turnoff Tone		-11.9	-10.9	-9.9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
DTMF Generator	Must not be in 202 mode				
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude, Low group	DPSK mode	-10	-9	-8	dBm0
Output Amplitude, High group	DPSK mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Long Loop Detect	With Sinusoid	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

Note: Parameters expressed in dBm0 refer to the following definition:

5V Version:
0 dB loss in the Transmit path to the line.
2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP	20		40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP	20		40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-49		-42	dBm0
Delay Time					
Bell 103		8		20	ms
Bell 212A		15		32	ms
Bell 202 Forward Channel		6		12	ms
Bell 202 Back Channel		25		40	ms
Hold Time					
Bell 103		6		20	ms
Bell 212A		10		24	ms
Bell 202 Forward Channel		3		8	ms
Bell 202 Back Channel		10		25	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-49		-42	dBm0
Delay Time					
Answer tone		10		25	ms
900 Hz SCT tone	Preceded by valid carrier*	4		10	ms
202 Main Channel Mark		10		25	ms
202 Back Channel Mark		20		65	ms
1270 or 2225 Hz marks		10		25	ms

* If SCT duration >4ms, it is guaranteed to detect.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors (Continued)					
Hold Time					
Answer tone		4		15	ms
900 Hz SCT tone		1		10	ms
202 Main Channel Mark		3		10	ms
202 Back Channel Mark		10		25	ms
1270 or 2225 Hz marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10			kΩ
				50	pF
Out of Band Energy	Frequency >12 kHz in all modes See Transmit Energy Spectrum			-60	dBm0
Output Impedance	TXA pin		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in 202 main channel		0.1	0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Frequency Change		40	100	ms
DPSK Recovered Clock					
Capture Range	% of data rate (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms
Tone Generator					
Tone Accuracy	DTMF or FSK tones	-5		+5	Hz
Tone Level	For DTMF, must not be in 202 mode	-1		+1	dB

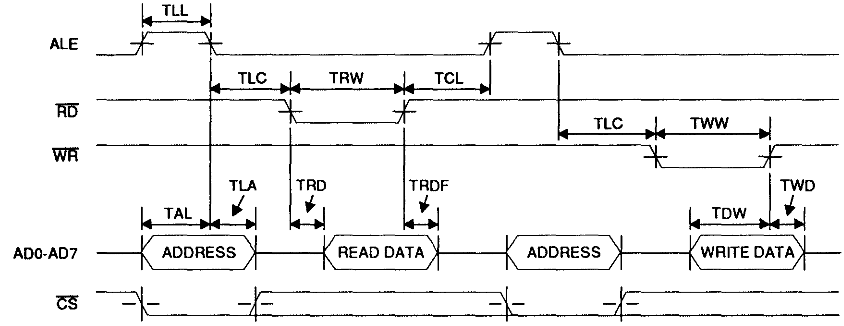
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{CS}$/Addr. setup before ALE Low	25			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{RD}/\overline{WR}$ Low	30			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE High	-5			ns
TRD	Data out from $\overline{RD}$ Low	0		140	ns
TLL	ALE width	30			ns
TRDF	Data float after $\overline{RD}$ High	0		5	ns
TRW	$\overline{RD}$ width	200		25000	ns
TWW	$\overline{WR}$ width	140		25000	ns
TDW	Data setup before $\overline{WR}$ High	40			ns
TWD	Data hold after $\overline{WR}$ High	10			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{WR}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

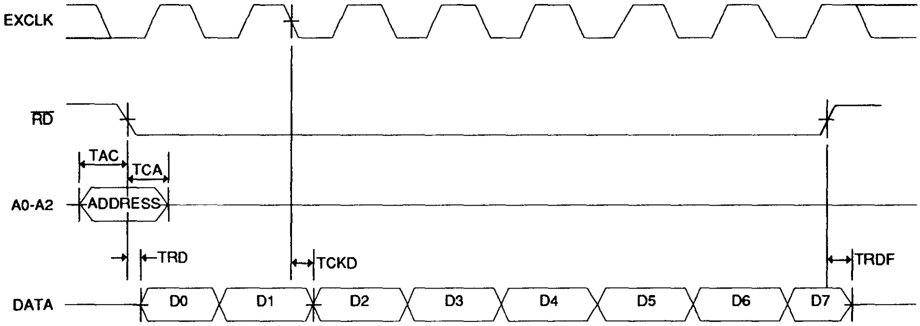
* Control for setup is the falling edge of $\overline{RD}$ or $\overline{WR}$.
Control for hold is the falling edge of $\overline{RD}$ or the rising edge of $\overline{WR}$.

TIMING DIAGRAMS

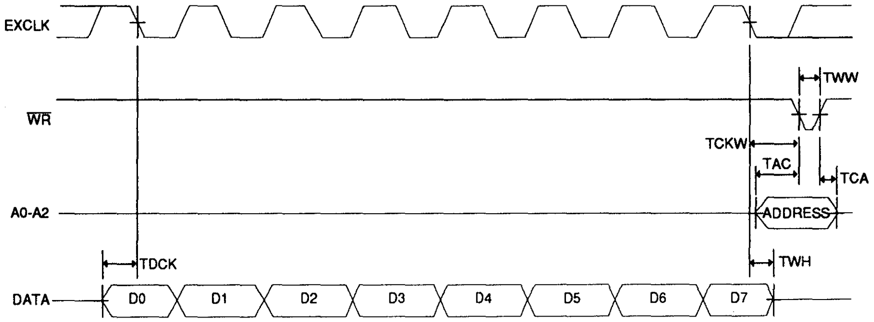
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5V design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

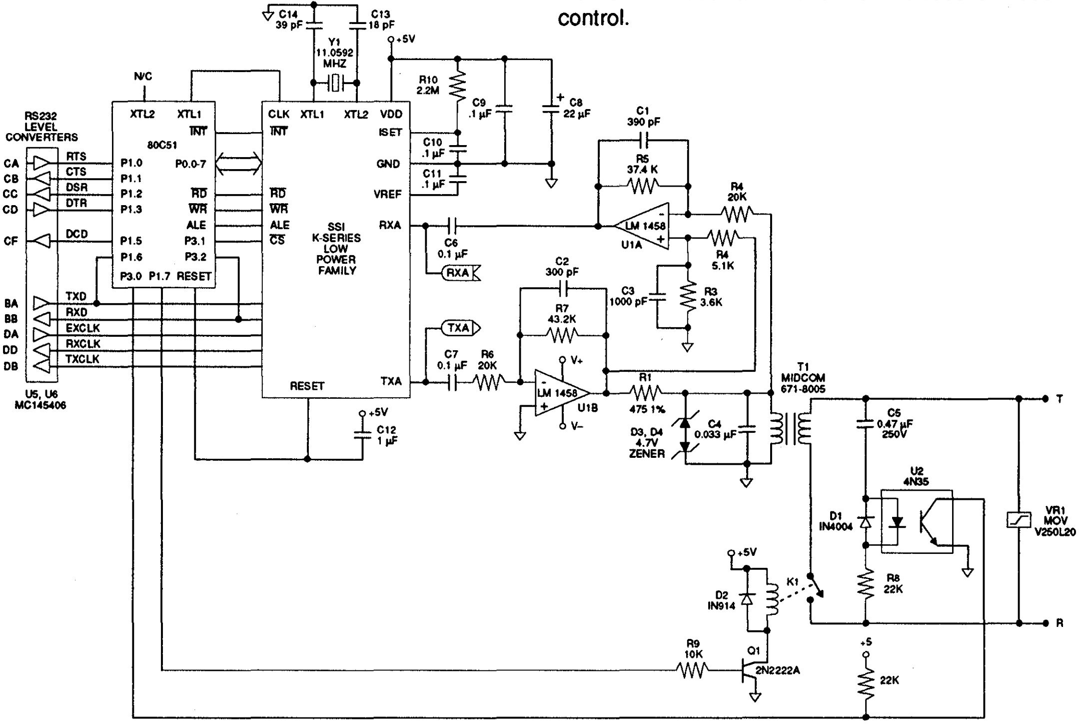


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

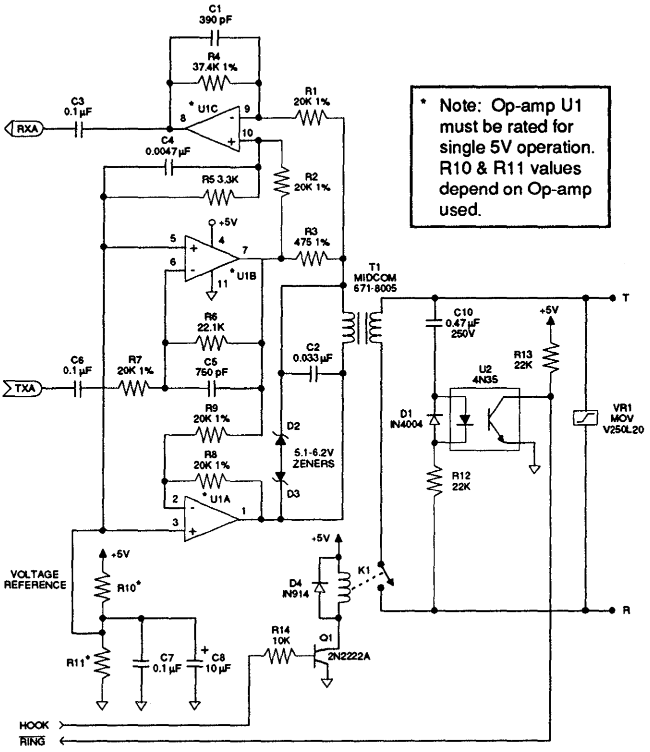
DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V Hybrid Version

SSI 73K302L
Bell 212A, 103, 202
Single-Chip Modem

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

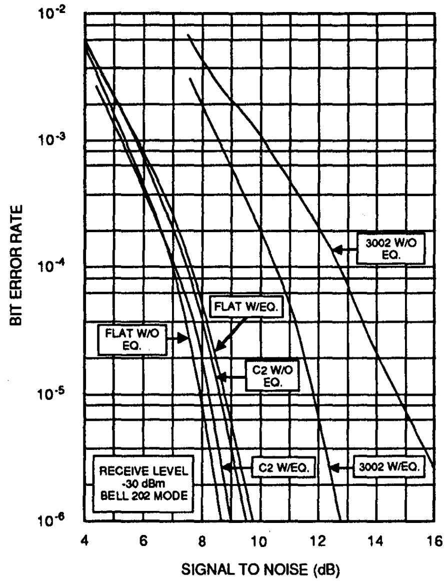
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

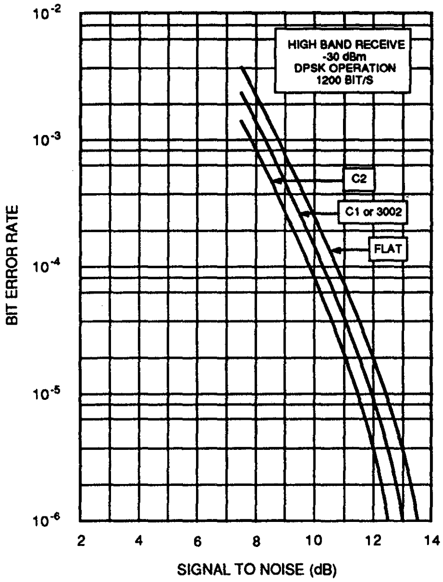
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

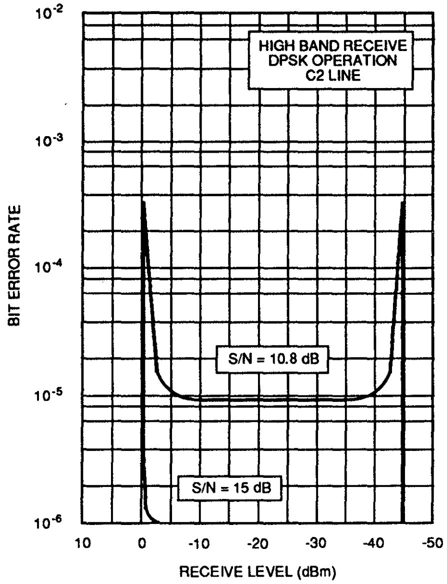
SSI 73K302L
BER vs S/N



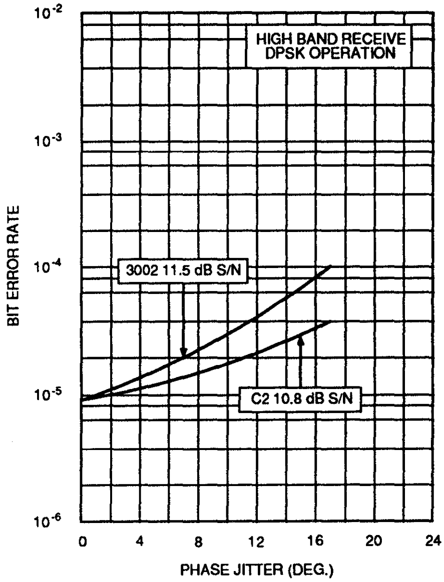
SSI 73K302L
BER vs S/N

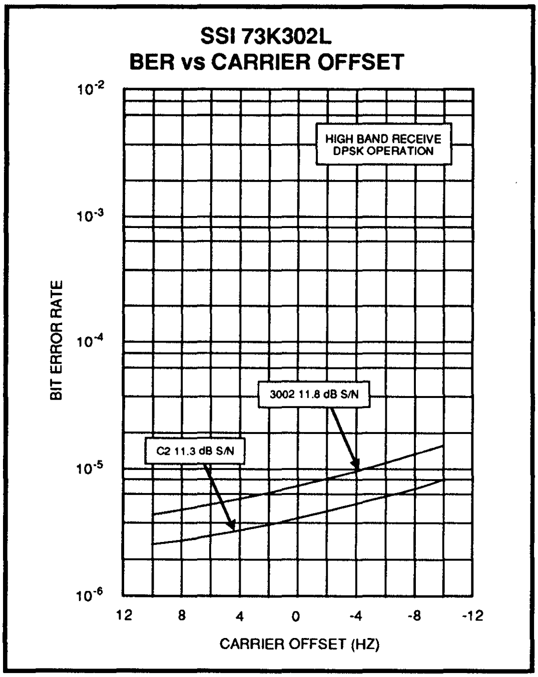


SSI 73K302L
BER vs RECEIVE LEVEL



SSI 73K302L
BER vs PHASE JITTER

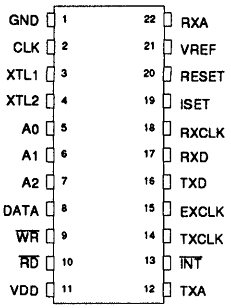



SSI 73K302L
BER vs CARRIER OFFSET
HIGH BAND RECEIVE
DPSK OPERATION
3002 11.8 dB S/N
C2 11.3 dB S/N
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
12
8
4
0
-4
-8
-12
CARRIER OFFSET (HZ)

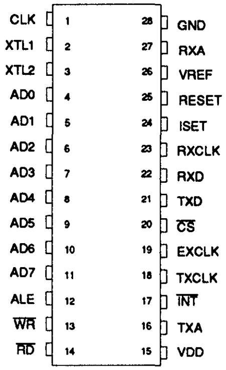
SSI 73K302L
Bell 212A, 103,202
Single-Chip Modem

PACKAGE PIN DESIGNATIONS

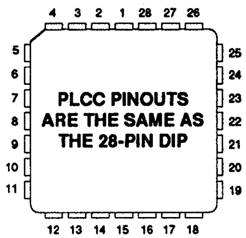
(Top View)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Pin
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K302L with Parallel Bus Interface		
28-Pin Plastic Dual-In-Line	73K302L-IP	73K302L-IP
28-Pin Plastic Leaded Chip Carrier	73K302L-IH	73K302L-IH
SSI 73K302L with Serial Interface		
22-pin Plastic Dual-In-Line	73K302SL-IP	73K302SL-IP

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

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Notes:

silicon systems®
A TDK Group Company

SSI 73K312L
Bell 202, 103 and CCITT V.23, V.21 Single-Chip Modem

Preliminary Data

December 1992

DESCRIPTION

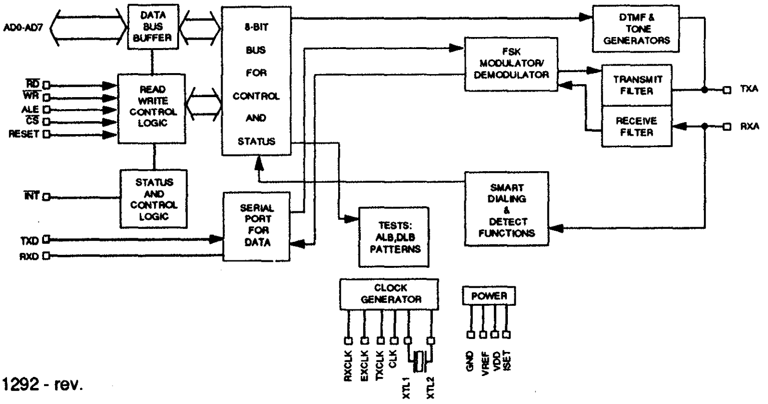
The SSI 73K312L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23, V.21, Bell 202, 103 FSK modem. The 73K312L supports asynchronous 1200 bit/s (600 bit/s at V.23 half speed mode) with or without 75/150 bit/s back channel (75 for V.23 and 150 for Bell 202) and 300 bit/s FSK (V.21 or Bell 103). The SSI 73K312L can also both detect and generate the CCITT and Bell answer tones needed for call initiation. The SSI 73K312L integrates analog, digital, and switched-capacitor array functions on a single substrate, offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP or 28 pin PLCC configuration. The SSI 73K312L operates from a single +5 V supply with very low power consumption.

The SSI 73K312L includes the FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling and 900 Hz soft carrier turnoff tones. The SSI 73K312L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial command bus. An ALE control line simplifies address demultiplexing. Data communications occur through a separate serial port only.

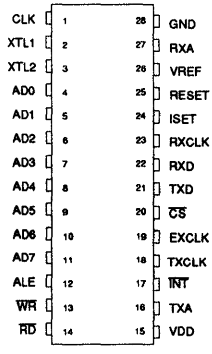
FEATURES

- **Bell 202, 103 and CCITT V.23, V.21 single-chip modem**
- **Full-duplex operation at 0-300 bit/s (V.21 and Bell 103)**
- **V.23 modes 1, 2, (i.e., 0-600 bit/s and 0-1200 bit/s) forward channel with or without 0-75 bit/s back channel**
- **Bell 202 0-1200 bit/s forward channel with or without 0-150 bit/s back channel**
- **Full Duplex 4-wire mode operation in V.23 and Bell 202 modes**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Call progress, carrier, precise answer tone (2100 or 2225 Hz), and precise mark detectors**
- **Precise calling tone and soft carrier turnoff generators/detectors (1300 Hz, 900 Hz)**
- **DTMF generator**
- **Test modes available: ALB, DL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 30 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73K312L
Bell 202, 103 and CCITT V.23, V.21 Single-Chip Modem

OPERATION

The SSI 73K312L is ideal for either free standing or integral system modem applications where multi-standard data communications is desired. Typical uses include videotex terminals, low-cost integral modems and built-in diagnostics for office automation or industrial control systems. The 73K312L's high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability in these applications. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system.

Quad-mode capability in one-chip allows full-duplex V.21 and Bell 103 operation or asymetrical V.23 and Bell 202 operation over the 2-wire switched telephone network. V.23 and 202 mode full-duplex operation at 1200 bit/s is also possible when operating on 4-wire leased lines.

A soft carrier turn-off feature facilitates fast line turn around when using the 202 or V.23 modes for half-duplex applications.

The SSI 73K312L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Bell 103 mode uses 1270 and 1070 Hz (originate, mark and space) or 2225 and 2025 Hz (answer, mark and space). Bell 202 mode uses 1200 and 2200 Hz for the main channel and 387 and 487 Hz for the back channel. The modulation rate of the back channel is up to 150 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A high and low band filter is included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Six 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as memory locations. Three control registers and the tone register are read/write memory. The status detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available with the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K312L control and status registers via a serial command port. In this mode the A0, A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking tones, calling tones and the 900 Hz soft carrier turn-off tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard dual-tones determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected and the transmit enable (CR0 bit D1) is changed from 0 to 1.

SOFT CARRIER TURN-OFF TONE GENERATOR

The soft carrier turn-off tone generator will output a 900 Hz tone. When activated in Bell 202 main channel transmit mode, the output signal will shift to 900 Hz, maintaining phase continuity during the transition.

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
GND	I	System Ground.
VDD	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to ground.
VREF	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to ground.
ISET	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{\text{CS}}$.
AD0-AD7	I/O	Address/data bus. These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{\text{CS}}$	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{\text{CS}}$ (latched) is not active. The state of $\overline{\text{CS}}$ is latched on the falling edge of ALE.
CLK	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or clock depending on the mode: 19.2 kHz (Bell103), 15.36 kHz (V.21, V.23, Bell 202). The pin defaults to the crystal frequency on reset.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{INT}}$	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{\text{INT}}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{\text{RD}}$	I	Read. A low requests a read of the SSI 73K312L internal registers. Data cannot be output unless both $\overline{\text{RD}}$ and the latched $\overline{\text{CS}}$ are active (low).
RESET	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR3) will be reset except for the D2 bit of CR3 which will be set to one to allow nominal transmit power. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a 1 µF capacitor to VDD.
$\overline{\text{WR}}$	I	Write. A low on this informs the SSI 73K312L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{\text{WR}}$. No data is written unless both $\overline{\text{WR}}$ and the latched $\overline{\text{CS}}$ are active (low).

SERIAL MICROPROCESSOR INTERFACE

A0-A2	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{\text{RD}}$ pin. $\overline{\text{RD}}$ low outputs data. $\overline{\text{RD}}$ high inputs data.
$\overline{\text{RD}}$	I	Read. A low on this input informs the SSI 73K312L that data or status information is being read by the processor. The falling edge of the $\overline{\text{RD}}$ signal will initiate a read from the addressed register. The $\overline{\text{RD}}$ signal must continue for seven falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{\text{RD}}$ signal is active.
$\overline{\text{WR}}$	I	Write. A low on this input informs the SSI 73K312L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{\text{WR}}$ low. Data is written on the rising edge of $\overline{\text{WR}}$.

Note: The Serial Control mode is provided in the parallel control versions by floating ALE and $\overline{\text{CS}}$ or tying ALE high and $\overline{\text{CS}}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

The Serial mode data and clock signals are compatible with the serial port mode 0 of the 8051.

RS-232 INTERFACE

NAME	TYPE	DESCRIPTION
EXCLK	I	External Clock. Used for serial control interface to clock control data in or out of the 73K312L.
RXCLK	O	Receive Clock. In V.23 2-wire mode RXCLK equals 16 x 1200 if answering and 16 x 75 if originating. In Bell 202 2-wire mode RXCLK equals 16 x 1200 if answering and 16 x 150 if originating. In V.21 or Bell 103 mode it equals 16 x 300.
RXD	O	Received Digital Data Output. Serial receive data is available on this pin. RXD will output constant marks if no carrier is detected.
TXCLK	O	Transmit Clock. If 1200 bit/s mode is selected, TXCLK equals 16 x1200 if originating and 16 x 75 (V.23) or 16 x 150 (Bell 202) if answering. In V.21 or Bell 103 mode it equals 16 x 300.
TXD	I	Transmit Digital Data Input. Serial data for transmission is input on this pin.

ANALOG INTERFACE AND OSCILLATOR

RXA	I	Received modulated analog signal input from the phone line.
TXA	O	Transmit analog output to the phone line.
XTL1 XTL2	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL1 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The AD0, AD1 and AD2 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K312L internal state. CR3 controls the attenuation of the transmitted signal and enables receive gain boost. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and RX output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	SPEED SELECT		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SPECIAL TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX 202 FDX	DTMF1	DTMF0/ TONE SELECT
CONTROL REGISTER 2 CR2	100				THIS REGISTER LOCATION IS RESERVED FOR USE WITH OTHER K-SERIES FAMILY MEMBERS				
CONTROL REGISTER 3 CR3	101				RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	SPEED SELECT		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=V.23 or BELL 103 1=V.21 or BELL 202		0000=PWR DOWN 1000=BELL 103 or 202 1100=CCITT V.23 or V.21 1110=CCITT V.23 MC HALF SPEED				0=SQUELCH ANALOG 1=ENABLE ANALOG	V.21 AND BELL 103: 0=ANSWER 1=ORIGINATE V.23 AND BELL 202: 0=RECEIVE @ 1200/600 BIT/S TRANSMIT @ 75/150 BIT/S 1=RECEIVE @ 75/150 BIT/S TRANSMIT @ 1200/600 BIT/S
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		IN V.23 or BELL 202 MODE 0=OFF 1=ON	0=NORMAL EQ. 1=ADD EXTRA PHASE EQ. IN SERIES WITH MAIN CHANNEL	0=XTAL 1=19.2 kHz or 15.36 kHz	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT SPECIAL TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX 202 FDX	DTMF1	DTMF0/ TONE SELECT
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=TRANSMITS CALLING TONE IF ORIGINATING IN CCITT MODE. TRANSMITS SCT TONE IF ORIGINATING IN BELL MODE.	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS. IF TRANSMIT DTMF BIT IS SET DTMF = 1	0=NORMAL 1=ALLOWS V.23 or BELL 202 FULL DUPLEX OPERATION		
CONTROL REGISTER 3 CR3	101				RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
					0=NO BOOST 1=12 dB BOOST	0000-1111 SETS TRANSMIT ATTENUATOR 16 dB RANGE DEFAULT=0100=-10dBm			
ID REGISTER 10	110	ID	ID	ID	ID				
00XX=73K212, 322, 321 01XX=73K221, 302 10XX=73K222 1100=73K224 1110=73K324 1101=73K312									

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	SPEED SELECT	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode in V.21 or Bell 103 (transmit in high band, receive in low band, or at 1200/1600 bit/s mode, receive at 1200/600 bit/s and transmit at 75/150 bit/s).
		1	Selects originate mode in V.21 or Bell 103 (transmit in low band, receive in high band) ,or at 1200/600 bit/s mode, receive at 75/150 bit/s and transmit at 1200/600 bit/s. If in V.23/ Bell 202 and D2 of TR=1, selects full duplex operation in 4-wire configuration.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF transmit control require transmit enable.
D5, D4,D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		1 0 0 0	Selects Bell 103 or 202.
		1 1 0 0	Selects CCITT V.23 or V.21.
		1 1 1 0	Selects CCITT V.23 MC Half Speed.
D6	Unused	0	Not used; must be written as a "0."
D7	Modulation Option	0	CCITT V.23 or Bell 103.
		1	CCITT V.21 or Bell 202.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR3 except for D2 bit, Tone) are reset to zero. CR3 bit D2 is set to one. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 19.2 kHz (Bell103) or 15.36 kHz(V.21, V.23, Bell 202).
D4	Add Ph. Eq.	0	Selects normal equalization.
		1	In V.23 or Bell 202 mode, additional phase equalization is added in series with the main channel filters.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{INT}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{INT}$ output. An interrupt will be generated with a change in status of DR bits D1-D3. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	▨	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

<table>
<tr><th>BIT NO.</th><th>NAME</th><th>CONDITION</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="2">D0</td><td rowspan="2">Long Loop</td><td>0</td><td>Indicates normal received signal.</td></tr>
<tr><td>1</td><td>Indicates low received signal level.</td></tr>
<tr><td rowspan="2">D1</td><td rowspan="2">Call Progress Detect</td><td>0</td><td>No call progress tone detected.</td></tr>
<tr><td>1</td><td>Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.</td></tr>
<tr><td rowspan="2">D2</td><td rowspan="2">Special Tone Detect</td><td>0</td><td>No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.</td></tr>
<tr><td>1</td><td>The tone is selected by bits in CR0 and TR.
<table>
<tr><th>Frequency (Hz)</th><th>D0 of TR</th><th>D4 of CR0</th><th>D0 of CR0</th><th>Mode</th></tr>
<tr><td>980</td><td>0</td><td>1</td><td>0</td><td>V.21</td></tr>
<tr><td>1650</td><td>0</td><td>1</td><td>1</td><td>V.21</td></tr>
<tr><td>390</td><td>0</td><td>1</td><td>1</td><td>V.23</td></tr>
<tr><td>1300</td><td>0</td><td>1</td><td>0</td><td>V.23</td></tr>
<tr><td>1300</td><td>1</td><td>1</td><td>0</td><td>V.21 or V.23</td></tr>
<tr><td>2100</td><td>1</td><td>1</td><td>1</td><td>V.21</td></tr>
<tr><td>1270</td><td>1</td><td>0</td><td>0</td><td>103</td></tr>
<tr><td>2225</td><td>1</td><td>0</td><td>1</td><td>103</td></tr>
<tr><td>387</td><td>1</td><td>0</td><td>1</td><td>202</td></tr>
<tr><td>1200</td><td>1</td><td>0</td><td>0</td><td>202</td></tr>
<tr><td>900</td><td>0</td><td>0</td><td>0</td><td>202</td></tr>
<tr><td>2225</td><td>0</td><td>0</td><td>1</td><td>103</td></tr>
</table></td></tr>
<tr><td rowspan="2">D3</td><td rowspan="2">Carrier Detect</td><td>0</td><td>No carrier detected in the receive channel.</td></tr>
<tr><td>1</td><td>Indicated carrier has been detected in the received channel.</td></tr>
<tr><td>D4</td><td>-</td><td>-</td><td>Not used.</td></tr>
<tr><td>D5</td><td>Receive Data</td><td>-</td><td>Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.</td></tr>
<tr><td>D6, D7</td><td>-</td><td>-</td><td>Not used.</td></tr>
</table>

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX 202 FDX	DTMF 1	DTMF 0/ TONE SELECT

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Tone Select		In CCITT mode, the Tone detected in D2 bit of TR is Mark of FSK selected if this bit is 0. 2100 Hz if this bit is 1 and originating, 1300 Hz if this bit is 1 and answering. In Bell mode, the Tone detected in D2 bit of TR is 2225 Hz if this bit is 0 and originating 900 Hz (SCT) if this bit is 0 and answering Mark of FSK selected if this bit is 1.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

TONE REGISTER (Continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D2	V.23/ Bell 202 FDX	0	Normal Operation
		1	Enables V.23 or Bell 202 full-duplex operation if D4=0. A 4-wire configuration is required in this mode.
D4	TX DTMF	0	Disabled DTMF.
	Transmit DTMF	1	Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.
D5	TX ANS	0	Disables answer tone generator.
	(Transmit Answer tone)	1	Enables answer tone generator. A 2100 Hz or 2225 Hz answer tone will be transmitted continuously when the transmit enable bit is set. If TR: D0 = 0, a 2225 Hz tone will be generated. If TR: D0 = 1, a 2100 Hz tone will be generated. The device must be in answer mode.
D6	TX Calling Tone/	0	Disables calling or SCT tone generator.
	SCT (Soft Carrier Turn-Off)Tone	1	Transmit calling tone if originating in CCITT mode. Transmit SCT tone if originating in Bell mode. Transmits neither if answering.
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin.The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 3

				D4	D3	D2	D1	D0
CR3 101				RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
		D3 D2 D1 D0	
D3, D2 D1, D0	Transmit Attenuator	0 0 0 0- 1 1 1 1	Sets the attenuation level of the transmitted signal in 1 dB steps. The default (D3-D0 = 0100) is for a transmit level of -10 dBm0 at the line with the recommended hybrid transmit gain. The total range is 16 dB.
D4	Receive	0	12 dB receive front end boost is not used.
	Gain Boost	1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID 3	ID 2	ID 1	ID 0				

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212(L) or 73K322L or 73K321
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 0	SSI 73K224L
		1 1 0 1	SSI 73K312L
		1 1 1 0	SSI 73K324L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
VDD Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD + 0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5		5.5	V
Digital Pins					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IOH, Output High Current		-0.4			mA
IOL, Output Low Current				1.6	mA
TA, Operating Free-Air Temperature		-40		+85	°C

RECOMMENDED OPERATING CONDITIONS (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Components*					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.9		2.1	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor	(External to GND)	0.1			µF
*Refer to Application section for placement.					

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
IDDA, Active	ISET Resistor = 2 MΩ			10	mA
IDD1, Power-down	CLK = 11.0592 MHz, ISET = GND			3	mA
IDD2, Power-down	CLK = 19.200 KHz, ISET = GND			2	mA
Digital Inputs					
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Digital Outputs					
VOH, Output High Voltage	IO = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = 1.6 mA			0.4	V
Capacitance					
Inputs	Capitance, all Digital Input pins			10	pF
XTL1 Load Capacitor	Depends on crystal		39		pF
XTL2 Load Capacitor	Depends on crystal		15		pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

NOTE: The following parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.38		+0.38	%
Transmit Level	Transmit Dotting Pattern	-11		-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±5		%
Total Output Jitter	Random Input in ALB @ RXD	-15		+15	%
DTMF Generator	**TR bit D4=1, CRO bit D1 = 1**				
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude	Low Band	-10		-8	dBm0
	High Band	-8		-6	dBm0
Twist	High-Band to Low-Band, as above	1.0	2.0	3.0	dB
Long Loop Detect	Not valid for Bell 202 V.23 back channel	-38		-28	dBm0
Dynamic Range			45		dB
Call Progress Detector	**Test signal is a 460 Hz sinusoid**				
Detect Level		-39		0	dBm0
Reject Level				-45	dBm0
Delay Time				35	ms
Hold Time				35	ms
Hysteresis		2			dB
Carrier Detect	**For a sinusoid at freq. = (Mark + Space)/2**				
Threshold		-48		-43	dBm0
Delay Time					
V.21		10	15	20	ms
103		8	15	20	ms
V.23 Main Channel RCV		6	10	12	ms
202 Main Channel RCV		6	8	12	ms
202, V.23 Back Channel		25	30	40	ms
Hold Time					
V.21		6	10	20	ms
103		6	12	20	ms
202, V.23 Main Channel		3	6	8	ms
202, V.23 Back Channel		10	15	25	ms
Hysteresis		2			dB

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-49		-42	dBm0
Delay Time	-70 dBm0 to -30 dBm0 step				
2100 Hz V.21 CCITT Answer Tone		10		25	ms
1300 Hz V.23 Mark		10		25	ms
390 Hz V.23 Back Channel Mark		20		65	ms
980 or 1650 Hz V.21 Marks		10		25	ms
2225 Hz Bell Answer Tone		10		35	ms
900 Hz SCT tone	Assumes that SCT follows data in a phase continuous manner	4		10	ms
1200 Hz Bell 202 Main Channel Mark		10		25	ms
387 Hz Bell 202 Back Channel Mark		20		65	ms
1270 or 2225 Hz Bell 103 Marks		10		30	ms
Hold Time	-30 dBm0 to -70 dBm0 step				
2100 Hz V.21 CCITT Answer Tone		4		15	ms
1300 Hz V.23 Mark		3		10	ms
390 Hz V.23 Back Channel Mark		10		25	ms
980 or 1650 Hz V.21 Marks		5		15	ms
2225 Hz Bell Answer Tone		4		15	ms
900 Hz SCT tone		1		10	ms
1200 Hz Bell 202 Main Channel Mark		3		10	ms
387 Hz Bell 202 Back Channel Mark		10		25	ms
1270 or 2225 Hz Bell 103 Marks		4		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

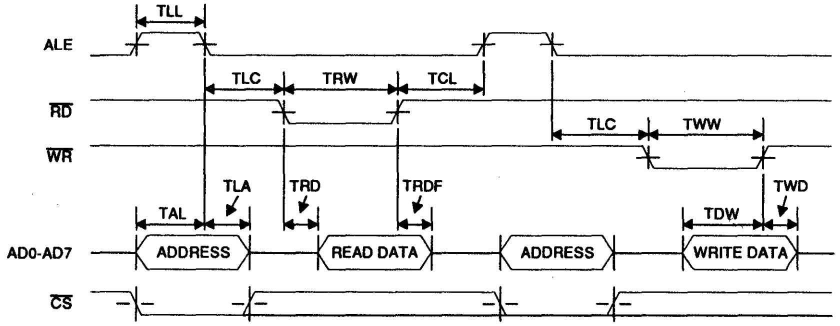
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in .3 to 3.4 kHz	10			kΩ
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin		200	300	Ω
Clock Noise	TXA pin: V.21 @ 61.44 kHz 103 @ 76.8 kHz V.23 or 202 MC @ 122.88 kHz V.23 or 202B @ 15.36 kHz		0.2	0.4	mVrms
Timing (Refer to Timing Diagrams)					
Parallel Mode					
TAL	$\overline{\text{CS}}$/Addr. setup before ALE	25			ns
TLA	$\overline{\text{CS}}$/Addr. hold after latch	20			ns
TLC	Latch to $\overline{\text{RD}}$/$\overline{\text{WR}}$ control	30			ns
TCL	$\overline{\text{RD}}$/$\overline{\text{WR}}$ Control to latch	-5			ns
TRD	Data out from $\overline{\text{RD}}$	0		140	ns
TLL	ALE width	30			ns
TRDF	Data float after READ	0		5	ns
TRW	READ width	200		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	40			ns
TWD	Data hold after WRITE	10			ns
Serial Mode					
TCKDR	Data out after CLK			300	ns
TCKW	WRITE after CLK	200			ns
TDCK	Data setup before CLK	150			ns
TAW	Address setup before control[1]	50			ns
TWA	Address hold after control[1]	50			ns
TWW	Write width	200			ns
TCKDW	Data hold after write	250			ns
TAR	Address setup before control[2]	0			ns
TRA	Address hold after control[2]	400			ns
TRD	Data out from $\overline{\text{RD}}$			350	ns
TRDF	Data float after READ	0		100	ns

[1] Control for setup is the falling edge of $\overline{\text{WR}}$.
Control for hold is the falling edge of $\overline{\text{WR}}$.

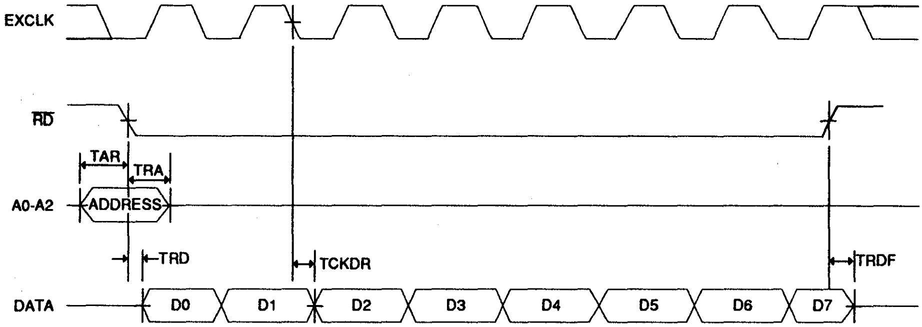
[2] Control for setup is the falling edge of $\overline{\text{RD}}$ or EXCLK.
Control for hold is the falling edge of $\overline{\text{RD}}$ or EXCLK.

TIMING DIAGRAMS

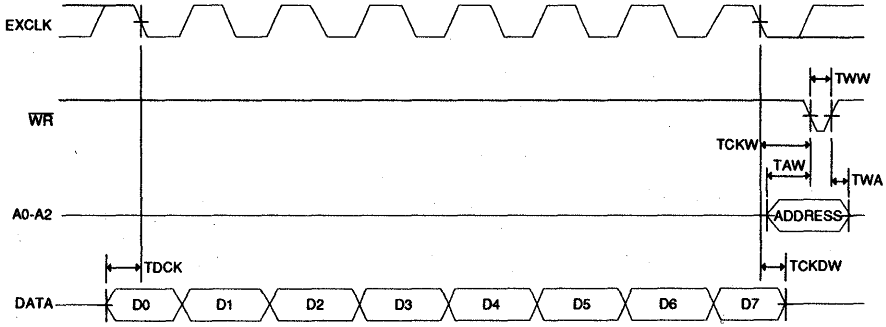
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes. Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, command data to the modem is sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

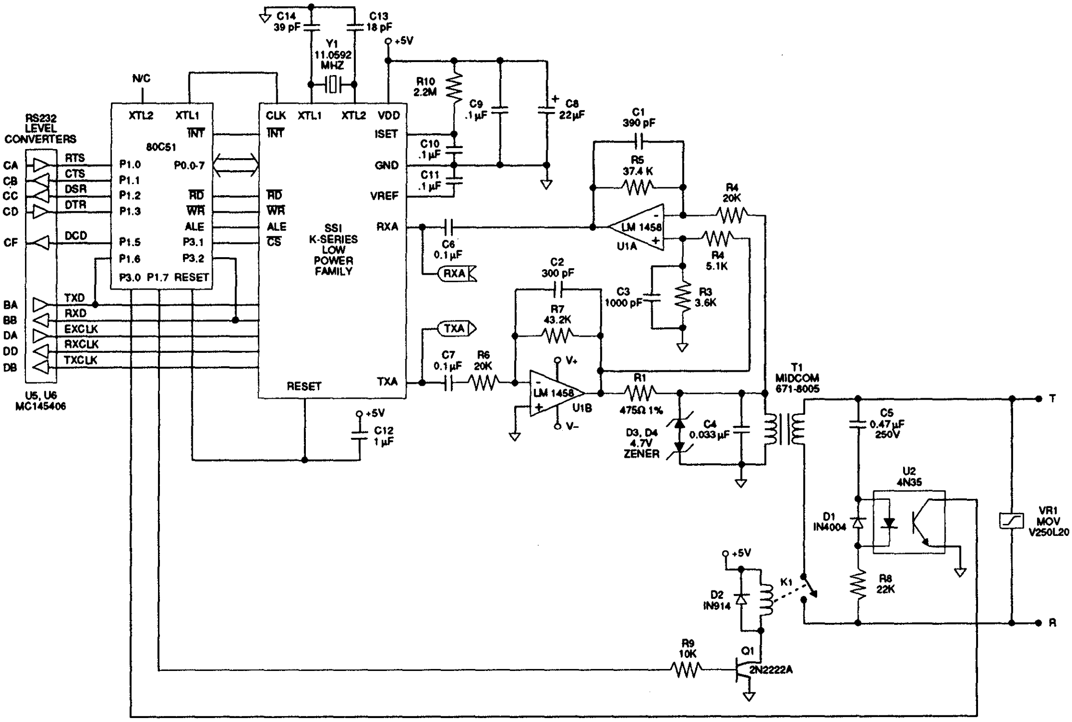


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

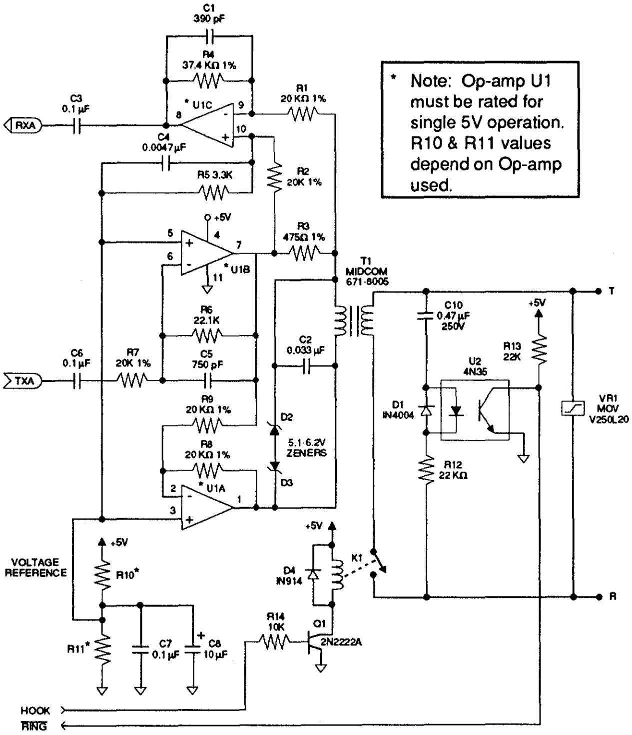
DIRECT ACCESS ARRANGEMENT (DAA)

The DAAs shown are two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply DAA is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. The DAA (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (op-amp C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the summing point of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions on a single IC, accessible from a standard bus interface. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals. Unlike digital logic circuitry, however, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to insure acceptable performance. Using good analog circuit



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V DAA Version

design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

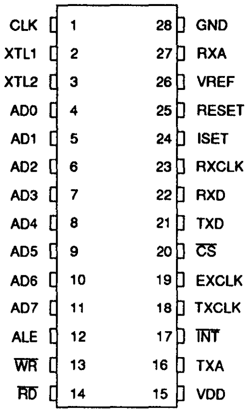
LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and ground is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the DAA and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the analog supplies to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as near to the package as possible.

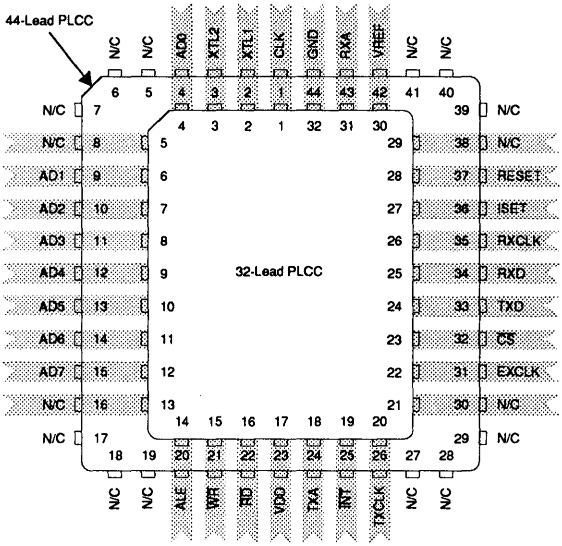
SSI 73K312L
Bell 202, 103 and CCITT V.23, V.21 Single-Chip Modem

PACKAGE PIN DESIGNATIONS

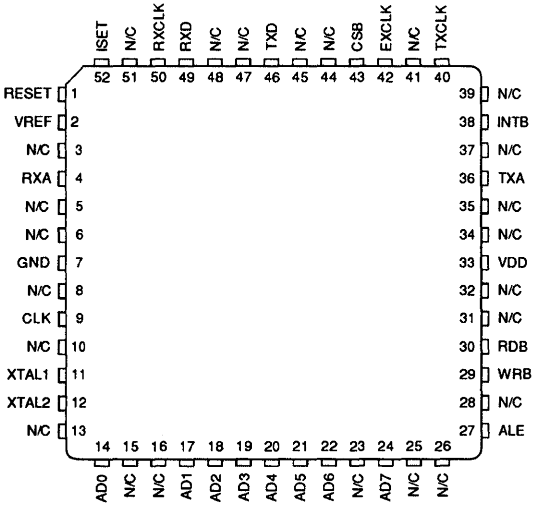
(Top View)



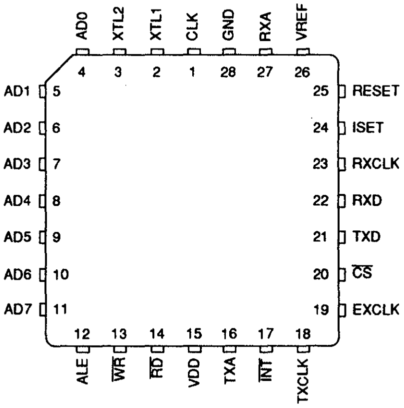
600-Mil
28-Pin DIP



32, 44-Pin PLCC



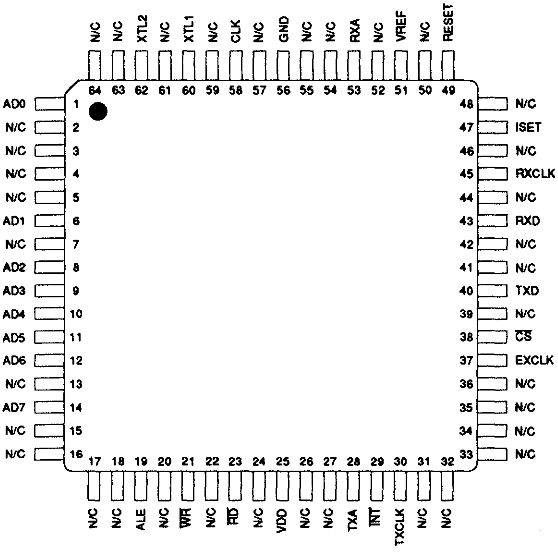
52-Lead QFP



28-Pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73K312L
Bell 202, 103 and CCITT V.23, V.21 Single-Chip Modem



64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K312L with Serial Bus Interface		
SSI 73K312L with Parallel Bus Interface		
28-Pin Plastic Dual-In-Line	73K312L-IP	73K312L-IP
28-Pin Plastic Leaded Chip Carrier	73K312L-28IH	73K312L-28IH
32-Pin Plastic Leaded Chip Carrier	73K312L-32IH	73K312L-32IH
44-Pin Plastic Leaded Chip Carrier	73K312L-IH	73K312L-IH
52-Lead Quad Flat Pack Package	73K312L-IG	73K312L-IG
64-Lead Thin Quad Flat Pack Package	73K312L-IGT	73K312L-IGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

Protected by the following patents: (4,691,172) (4,777,453)

Notes:

silicon systems®
A TDK Group Company

SSI 73K321L
CCITT V.23, V.21
Single-Chip Modem

December 1992

DESCRIPTION

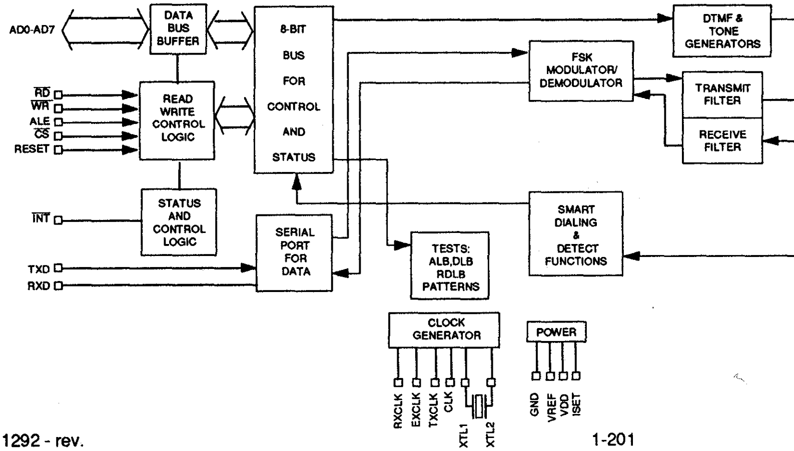
The SSI 73K321L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23 and V.21 compatible modem, capable of 0-300 bit/s full-duplex or 0-1200 bit/s half-duplex operation over dial-up telephone lines. The 73K321L provides 1200 bit/s operation in V.23 mode and 300 bit/s in V.21 mode. The SSI 73K321L also can both detect and generate the 2100 Hz answer tone needed for call initiation. The SSI 73K321L integrates analog, digital, and switched-capacitor array functions on a single substrate,offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K321L operates from a single +5V supply with very low power consumption.

The SSI 73K321L includes the FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling tones. The SSI 73K321L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only. (Continued)

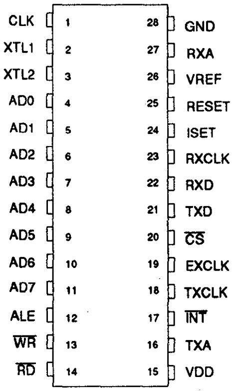
FEATURES

- **One-chip CCITT V.23 and V.21 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (V.21) or 0-1200 bit/s (V.23) forward channel with or without 0–75 bits/s back channel**
- **Full Duplex 0-1200 bit/s (V.23) in 4-wire mode**
- **Pin and software compatible with other SSI K-Series 1-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FS mark detectors**
- **DTMF generator**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **Space efficient 28-pin PLCC package**
- **CMOS technology for low power consumption using 30 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 73K321L is ideal for either free standing or integral system modem applications where multi-standard data communications over the 2-wire switched telephone network is desired. Typical uses include videotex terminals, low-cost integral modems and built-in diagnostics for office automation or industrial control systems. The 73K321L's high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability in these applications. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K321L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters. The parallel bus interface is not available with the 22-pin package.

SERIAL COMMAND INTERFACE

The serial command mode allows access to the SSI 73K321L control and status registers via a serial command port. In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines.' A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after RD is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone-pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Dialing is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with 0.1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with 0.1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a 0.1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{\text{CS}}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{\text{CS}}$	20	-	I	Chip select. A low during the falling edge of ALE on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{\text{CS}}$ (latched) is not active. The state of $\overline{\text{CS}}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is the output of the crystal oscillator frequency only in the SSI 73K321.
$\overline{\text{INT}}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{\text{INT}}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{\text{RD}}$	14	-	I	Read. A low requests a read of the SSI 73K321L internal registers. Data cannot be output unless both $\overline{\text{RD}}$ and the latched $\overline{\text{CS}}$ are active or low.
RESET	25	20	I	Reset. An active high signal high on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PIN DESCRIPTION (Continued)

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{\text{WR}}$	13	-	I	Write. A low on this informs the SSI 73K321L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{\text{WR}}$. No data is written unless both $\overline{\text{WR}}$ and the latched $\overline{\text{CS}}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{\text{RD}}$ pin. $\overline{\text{RD}}$ low outputs data. $\overline{\text{RD}}$ high inputs data.
$\overline{\text{RD}}$	-	10	I	Read. A low on this input informs the SSI 73K321L that data or status information is being read by the processor. The falling edge of the $\overline{\text{RD}}$ signal will initiate a read from the addressed register. The $\overline{\text{RD}}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{\text{RD}}$ signal is active.
$\overline{\text{WR}}$	-	9	I	Write. A low on this input informs the SSI 73K321L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{\text{WR}}$ low. Data is written on the rising edge of $\overline{\text{WR}}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{\text{CS}}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ controls are used differently.

The serial control mode is provided in the 28-pin version by tying ALE high and $\overline{\text{CS}}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. Used for serial control interface to clock control data in or out of the 73K321L.
RXCLK	23	18	O	Receive Clock. A clock which is 16 x 1200, or 16 x 75 in V.23 mode, or 16 x 300 baud data rate is output in V.21.
RXD	22	17	O	Received Digital Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock. TXCLK is always active. In V.23 mode the output is either a 16 x 1200 baud clock or 16 x 75 baud, in V.21 mode the clock is 16 x 300 baud.
TXD	21	16	I	Transmit Digital Data Input. Serial data for transmission is input on this pin. In asynchronous modes (1200 or 300 baud) no clocking is necessary.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the phone line.
TXA	16	12	O	Transmit analog output to the phone line.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K321L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1	DTMF0/ ANSWER/SPEC. TONE SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=V.23 FSK 1=V.21 FSK		0000=PWR DOWN 1100=FSK 0001=TRANSMIT DTMF, CALL PROGRESS DETECTION				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	IN V.21 MODE: 0=ANSWER 1=ORIGINATE IN V.23 MODE : 0=RECEIVE @ 1200 BIT/S, TRANSMIT @ 75 BIT/S 1=RECEIVE @ 75 BIT/S, TRANSMIT @ 1200 BIT/S
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLED 1=ENABLED	0=NORMAL EQ. 1=ADD EXTRA PHASE EQ. IN V.23	0=XTAL 1= NOT SUPPORTED IN THIS DEVICE	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010			RECEIVE DATA		CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1	DTMF0/ SPECIAL TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS. OVERIDES OTHER TRANSMIT MODES	0=HALF DUPLEX V.23 1=ALLOWS V.23 FULL DUPLEX OPERATION		0=ANSWER TONE FREQ.=2225 Hz FSK MARK WILL BE INDICATED BY SPECIAL TONE BIT IN DR 1=ANSWER TONE FREQ.=2100 Hz EITHER 2100 Hz (IN ORIG.) OR 1300 Hz (IN ANS.) WILL BE INDICATED BY SPECIAL TONE BIT IN DR
ID REGISTER 10	110	ID	ID	ID	ID				

00XX=73K212, 322, 321
01XX=73K221, 302
10XX=73K222
1100=73K224
1110=73K324
1101=73K312

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	▨	TX DTMF	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode in V.21 (transmit in high band, receive in low band) or in V.23 mode, receive at 1200 bit/s and transmit at 75 bit/s.
		1	Selects originate mode in V.21 (transmit in low band, receive in high band) or in V.23 mode, receive at 75 bit/s and transmit at 1200 bit/s. If in V.23 and D2 of TR=1, selects V.23 full duplex operation in 4-wire configuration.
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4,D3,	Transmit Mode	D5 D4 D3 D2	
D2		0 0 0 1	Transmit DTMF
D2		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		1 1 0 0	Selects FSK operation.
D6	Unused	0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		0 1 1	FSK CCITT V.23 mode.
		1 1 1	FSK CCITT V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	Program as 0	Not supported in the SSI 73K321.See the TXCLK and RXCLK pin descriptions for 16x the data rate clocks.
D4	Add Ph. Eq.	0	Selects normal equalization.
		1	In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{\text{INT}}$ pin. All interrupts are normally disabled in power down modes.
		1	Enables $\overline{\text{INT}}$ output. An interrupt will be generated with a change in status of DR bits D1-D3. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	▨	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band when CR0 D2 = 1.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21 or V.23 answer mode.
			(3) an FSK mark for the mode the device is set to receive in if D0 of TR = 0.
			NOTE: Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unused		Not used in the 73K321L.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2	DTMF 1	DTMF 0/ ANS. TONE/ SPECIAL TONE/ SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	DTMF 0/ Answer Tone/ Special Tone/ Detect/Select	D6 D5 D4 D0	D0 interacts with bits D6, D5, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21 or V.23 answer mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz answer tone in answer mode.
		X 1 0 1	Transmit 2100 Hz answer tone in answer mode.
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D3 D2 D1 D0 0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW	TONES HIGH
1	0 0 0 1	697	1209
2	0 0 1 0	697	1336
3	0 0 1 1	697	1477
4	0 1 0 0	770	1209
5	0 1 0 1	770	1336
6	0 1 1 0	770	1477
7	0 1 1 1	852	1209
8	1 0 0 0	852	1336
9	1 0 0 1	852	1477
0	1 0 1 0	941	1336

TONE REGISTER (Continued)

<table>
<tr><th>BIT NO.</th><th>NAME</th><th>CONDITION</th><th colspan="7">DESCRIPTION</th></tr>
<tr><td rowspan="7">D3, D2,
D1, D0
(Cont.)</td><td rowspan="7"></td><td rowspan="7"></td><td>KEYBOARD EQUIVALENT</td><td colspan="4">DTMF CODE
D3 D2 D1 D0</td><td colspan="2">TONES
LOW HIGH</td></tr>
<tr><td>*</td><td>1</td><td>0</td><td>1</td><td>1</td><td>941</td><td>1209</td></tr>
<tr><td>#</td><td>1</td><td>1</td><td>0</td><td>0</td><td>941</td><td>1477</td></tr>
<tr><td>A</td><td>1</td><td>1</td><td>0</td><td>1</td><td>697</td><td>1633</td></tr>
<tr><td>B</td><td>1</td><td>1</td><td>1</td><td>0</td><td>770</td><td>1633</td></tr>
<tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>852</td><td>1633</td></tr>
<tr><td>D</td><td>0</td><td>0</td><td>0</td><td>0</td><td>941</td><td>1633</td></tr>
<tr><td rowspan="2">D4</td><td rowspan="2">Transmit DTMF</td><td>0</td><td colspan="7">Disabled DTMF.</td></tr>
<tr><td>1</td><td colspan="7">Activates DTMF. The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.</td></tr>
<tr><td rowspan="2">D5</td><td rowspan="2">Transmit Answer Tone</td><td>0</td><td colspan="7">Disables answer tone generator.</td></tr>
<tr><td>1</td><td colspan="7">Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode.</td></tr>
<tr><td rowspan="2">D6</td><td rowspan="2">Transmit Calling Tone</td><td>0</td><td colspan="7">Disables calling tone generator.</td></tr>
<tr><td>1</td><td colspan="7">Transmit calling tone in either mode.</td></tr>
<tr><td rowspan="2">D7</td><td rowspan="2">RXD Output Control</td><td>0</td><td colspan="7">Enables RXD pin. Receive data will be output on RXD.</td></tr>
<tr><td>1</td><td colspan="7">Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.</td></tr>
</table>

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID	▨	▨	▨	▨

BIT NO.	NAME	CONDITION				DESCRIPTION
		D7	D6	D5	D4	Indicates Device:
D7, D6, D5 D4	Device Identification Signature	0	0	X	X	SSI 73K212(L), 73K321L or 73K322L
		0	1	X	X	SSI 73K221(L) or 73K302L
		1	0	X	X	SSI 73K222(L)
		1	1	0	0	SSI 73K224L
		1	1	1	0	SSI 73K324L
		1	1	0	1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temperature		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 kHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern in ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
NOTE: Parameters expressed in dBm0 refer to the following definition: 0 dB loss in the Transmit path to the line. 2 dB gain in the Receive path from the line. Refer to the Basic Box Modem diagram in the Applications section for the DAA design.					
DTMF Generator					
Freq. Accuracy		-0.25		+0.25	%
Output Amplitude	Low Band, CR0 bit D2=1	-10	-9	-8	dBm0
Output Amplitude	High Band, CR0 bit D2=1	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, as above	1.0	2.0	3.0	dB
Long Loop Detect	Not valid for V.23 back channel	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		43		dB
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	Single Tone	-48		-43	dBm0
Delay Time					
V.21		10		20	ms
V.23 Forward Channel		6		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		6		20	ms
V.23 Forward Channel		3		8	ms
V.23 Back Channel		10		25	ms
Hysteresis		2			dB

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time	-70 dBm0 to -30 dBm0 Step				
2100 Hz answer tone		10		25	ms
1300 Hz calling tone		10		25	ms
390 Hz V.23 back channel mark		20		65	ms
980 or 1650 Hz V.21 marks		10		25	ms
Hold Time	-30 dBm0 to -70 dBm0 Step				
2100 Hz answer tone		4		15	ms
1300 Hz calling tone		3		10	ms
390 Hz V.23 back channel mark		10		25	ms
980 or 1650 Hz V.21 marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in .3 to 3.4 kHz	10		 50	kΩ pF
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin, TXA Enabled		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in V.23 main channel		0.1	0.4	mVrms

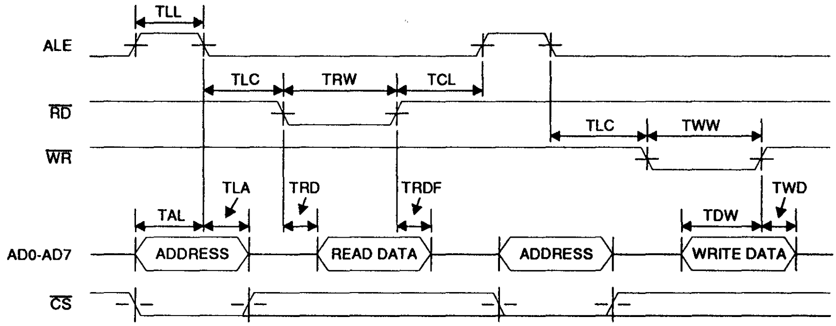
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
TAL	$\overline{\text{CS}}$/Addr. setup before ALE Low	25			ns
TLA	$\overline{\text{CS}}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{\text{RD}}$/$\overline{\text{WR}}$ Low	30			ns
TCL	$\overline{\text{RD}}$/$\overline{\text{WR}}$ Control to ALE High	-5			ns
TRD	Data out from $\overline{\text{RD}}$ Low	0		140	ns
TLL	ALE width	30			ns
TRDF	Data float after $\overline{\text{RD}}$ High	0		5	ns
TRW	$\overline{\text{RD}}$ width	200		25000	ns
TWW	$\overline{\text{WR}}$ width	140		25000	ns
TDW	Data setup before $\overline{\text{WR}}$ High	40			ns
TWD	Data hold after $\overline{\text{WR}}$ High	10			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{\text{WR}}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

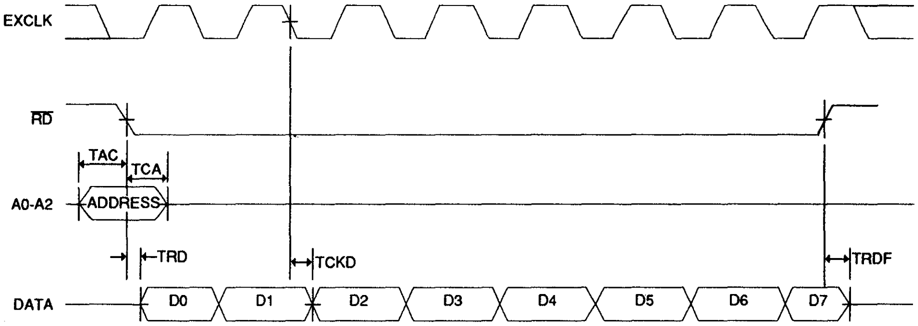
* Control for setup is the falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$.
Control for hold is the falling edge of $\overline{\text{RD}}$ or the rising edge of $\overline{\text{WR}}$.

TIMING DIAGRAMS

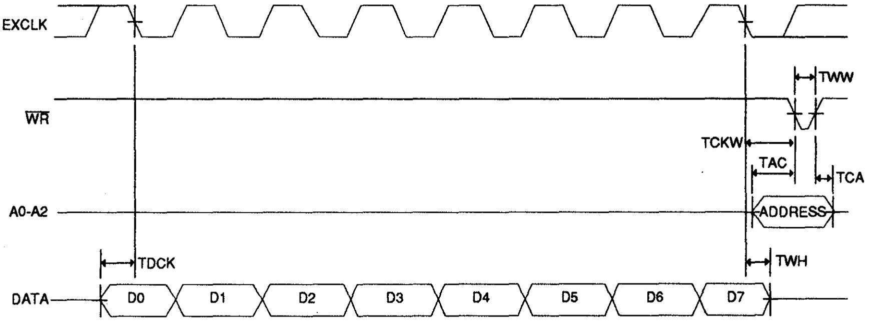
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

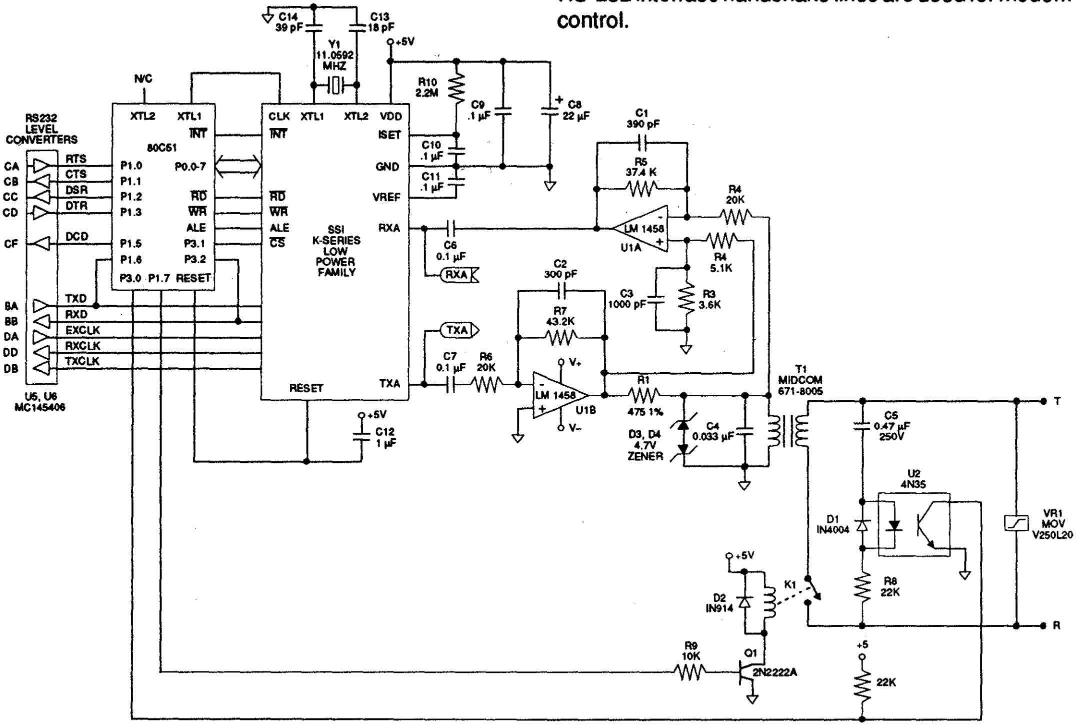


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

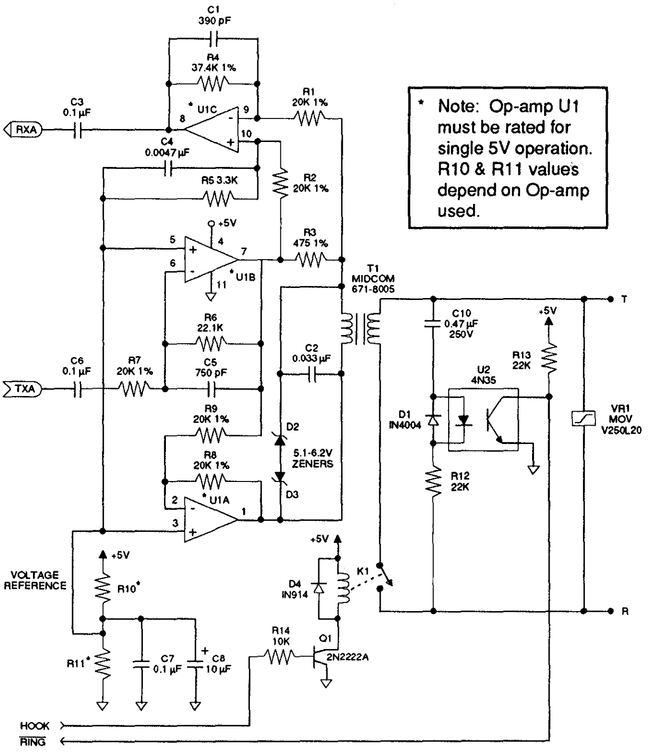
DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5V supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

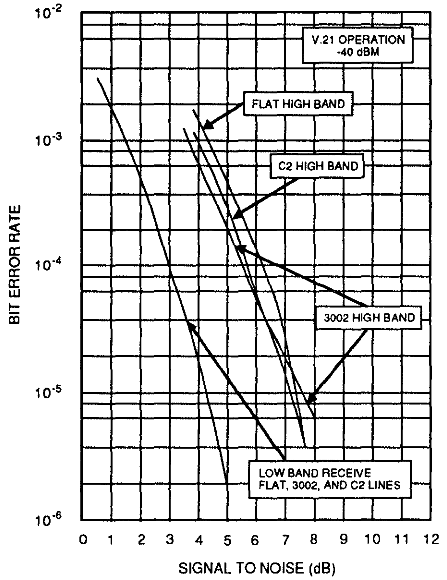
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

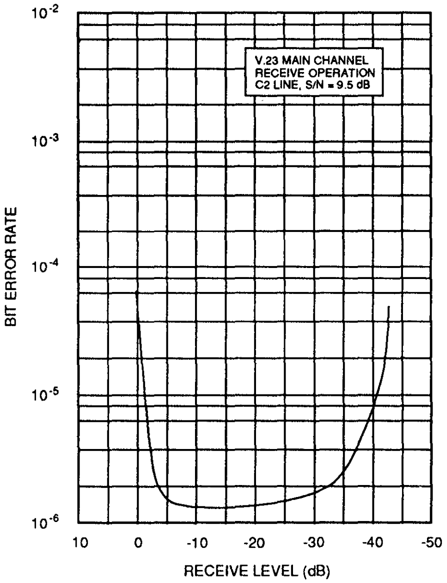
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

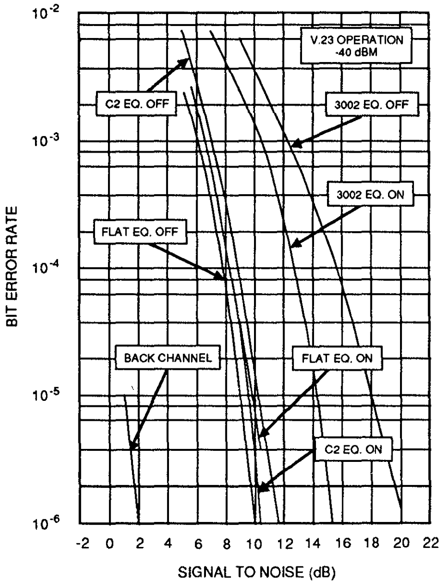
SSI 73K321L
BER vs SIGNAL TO NOISE



***SSI 73K321L**
BER vs RECEIVE LEVEL (V.23)



***SSI 73K321L**
BER vs S/N (V.23 ONLY)**



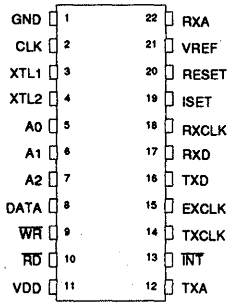
* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

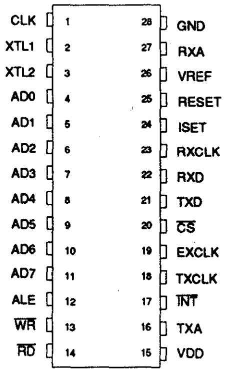
SSI 73K321L
CCITT V.23, V.21
Single-Chip Modem

PACKAGE PIN DESIGNATIONS

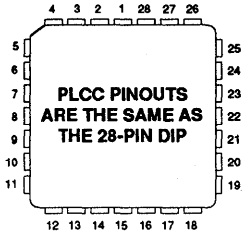
(TOP VIEW)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Pin
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K321L with Parallel Bus Interface 28-Pin 5V Supply Plastic Dual-In-Line	73K321L-IP	73K321L-IP
Plastic Leaded Chip Carrier	73K321L-IH	73K321L-IH
SSI 73K321L with Serial Interface 22-Pin 5V Supply Plastic Dual-In-Line	73K321SL-IP	73K321SL-IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

Protected by the following patents: (4,691,172) (4,777,453)

Notes:

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A TDK Group Company

SSI 73K322L
CCITT V.23, V.22, V.21 Single-Chip Modem

December 1992

DESCRIPTION

The SSI 73K322L is a highly integrated single-chip modem IC which provides the functions needed to construct a CCITT V.23, V.22 and V.21 compatible modem, capable of 1200 or 0-300 bit/s full-duplex operation or 0-1200 bit/s half-duplex operation with or without the back channel over dial-up lines. The SSI 73K322L is an enhancement of the SSI 73K221L single-chip modem with performance characteristics suitable for European and Asian telephone systems. The SSI 73K322L produces either 550 or 1800 Hz guard tone, recognizes and generates a 2100 Hz answer tone, and supports V.21 for 300 Hz FSK operation. It also operates in V.23, 1200 bit/s FSK mode. The SSI 73K322L integrates analog, digital, and switched-capacitor array functions on a single substrate,offering excellent performance and a high level of functional integration in a single 28- or 22-pin DIP configuration. The SSI 73K322L operates from a single +5V supply with very low power consumption.

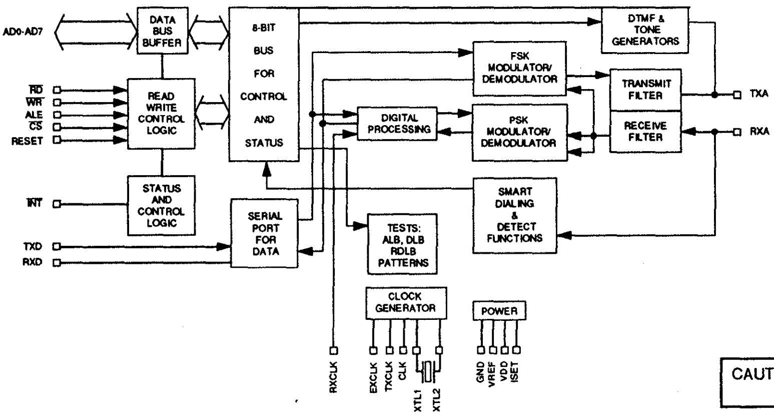
The SSI 73K322L includes the DPSK and FSK modulator/demodulator functions, call progress and handshake tone monitor test modes, and a tone generator capable of producing DTMF, answer, calling and 550 or 1800 Hz guard tone. This device supports V.23, V.22 (except mode v) and V. 21 modes of operation, allowing both synchronous and

(Continued)

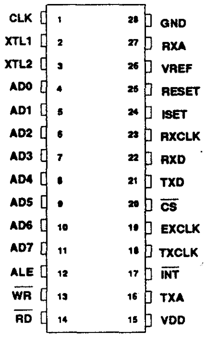
FEATURES

- **One-chip CCITT V.23, V.22 and V.21 standard compatible modem data pump**
- **Full-duplex operation at 0-300 bit/s (FSK) or 600 and 1200 bit/s (DPSK) or 0-1200 bit/s (FSK) forward channel with or without 0-75 bit/s back channel**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial or parallel microprocessor bus for control**
- **Serial port for data transfer**
- **Both synchronous and asynchronous modes of operation**
- **Call progress, carrier, precise answer tone (2100 Hz), calling tone (1300 Hz) and FSK mark detectors**
- **DTMF and 550 or 1800 Hz guard tone generators**
- **Test modes available: ALB, DL, RDL, Mark, Space, Alternating bit patterns**
- **Precise automatic gain control allows 45 dB dynamic range**
- **CMOS technology for low power consumption using 30 mW @ 5V from a single power supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

asynchronous communications. The SSI 73K322L is designed to appear to the systems designer as a microprocessor peripheral, and will easily interface with popular one-chip microprocessors (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus or via an optional serial control bus. An ALE control line simplifies address demultiplexing. Data communications occurs through a separate serial port only.

The SSI 73K322L is ideal for use in either free standing or integral system modem products where multi-standard data communications over the 2-wire switched telephone network is desired. Its high functionality, low power consumption and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converter for a typical system. The SSI 73K322L is part of Silicon Systems K-Series family of pin and function compatible single-chip modem products. These devices allow systems to be configured for higher speeds and Bell or CCITT operation with only a single component change.

OPERATION

ASYNCHRONOUS MODE

Data transmission for the DPSK mode requires that data ultimately be transmitted in a synchronous fashion. The SSI 73K322L includes ASYNC/SYNC and SYNC/ASYNC converters which delete or insert stop bits in order to transmit data at a regular rate. In asynchronous mode the serial data comes from the TXD pin into the ASYNC/SYNC converter. The ASYNC/SYNC converter accepts the data provided on the TXD pin which normally must be 1200 or 600 bit/s +1.0%, -2.5%. The rate converter will then insert or delete stop bits in order to output a signal which is 1200 or 600 bit/s ± .01% (± .01% is the crystal tolerance).

The SYNC/ASYNC converter also has an extended overspeed mode which allows selection of an output overspeed range of either +1% or +2.3%. In the extended overspeed mode, stop bits are output at 7/8 the normal width.

The serial data stream from the transmit buffer or the rate converter is passed through the data scrambler and onto the analog modulator. The data scrambler can be bypassed under processor control when unscrambled data must be transmitted. If serial input data contains a break signal through one character (including start and stop bits) the break will be extended to at least 2 • N + 3 bits long (where N is the number of transmitted bits/character).

Serial data from the demodulator is passed first through the data descrambler and then through the SYNC/ASYNC converter. The ASYNC/ASYNC converter will reinsert any deleted stop bits and output data at an intra-character rate (bit-to-bit timing) of no greater than 1219 bit/s. An incoming break signal (low through two characters) will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODE

The CCITT V.22 standard defines synchronous operation at 600 and 1200 bit/s. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The ASYNCH/SYNCH converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as it is input.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73K322L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the V.22 standards. The base-band signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire telephone line. Transmission occurs using either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K322L uses a phase locked loop coherent demodulation technique for optimum receiver performance.

FSK MODULATOR/DEMODULATOR

The FSK modulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 mode uses 980 and 1180 Hz (originate, mark and space) or 1650 and 1850 Hz (answer, mark and space). V.23 mode uses 1300 and 2100 Hz for the main channel and 390 and 450 Hz for the back channel. The modulation rate of the back channel is up to 75 baud. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the V.21 or V.23 modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and provide compromise delay equalization and rejection of out-of-band signals in the receive channel. Amplitude and phase equalization are necessary to compensate for distortion of the transmission line and to reduce intersymbol interference in the bandlimited receive signal. The transmit signal filtering approximates a 75% square root of raised Cosine frequency response characteristic.

AGC

The automatic gain control maintains a signal level at the input to the demodulators which is constant to within 1 dB. It corrects quickly for increases in signal which would cause clipping and provides a total receiver dynamic range of >45 dB.

PARALLEL BUS INTERFACE

Four 8-bit registers are provided for control, option select and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as four consecutive memory locations. Two control registers and the tone register are read/write memory. The detect register is read only and cannot be modified except by modem response to monitored parameters.

SERIAL COMMAND INTERFACE

The serial command interface allows access to the SSI 73K322L control and status registers via a serial command port (22-pin version only). In this mode the A0 , A1 and A2 lines provide register addresses for data passed through the data pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The first bit is available after $\overline{RD}$ is brought low and the next seven cycles of EXCLK will then transfer out seven bits of the selected address location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consecutive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transferred into the selected register occurs on the rising edge of $\overline{WR}$.

SPECIAL DETECT CIRCUITRY

The special detect circuitry monitors the received analog signal to determine status or presence of carrier, answer tone and weak received signal (long loop condition), special tones such as FSK marking and the 1300 Hz calling tone are also detected. A highly frequency selective call progress detector provides adequate discrimination to accurately detect European call progress signals.

DTMF GENERATOR

The DTMF generator will output one of 16 standard tone pairs determined by a 4-bit binary value and TX DTMF mode bit previously loaded into the tone register. Tone generation is initiated when the DTMF mode is selected using the tone register and the transmit enable (CR0 bit D1) is changed from 0 to 1.

PIN DESCRIPTION

POWER

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
GND	28	1	I	System Ground.
VDD	15	11	I	Power supply input, 5V ±10%. Bypass with .1 and 22 µF capacitors to GND.
VREF	26	21	O	An internally generated reference voltage. Bypass with .1 µF capacitor to GND.
ISET	24	19	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. ISET should be bypassed to GND with a .1 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	12	-	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{CS}$.
AD0-AD7	4-11	-	I/O	Address/data bus. These bidirectional tri-state multiplexed lines carry information to and from the internal registers.
$\overline{CS}$	20	-	I	Chip select. A low on this pin during the falling edge of ALE allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{CS}$ (latched) is not active. The state of $\overline{CS}$ is latched on the falling edge of ALE.
CLK	1	2	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{INT}$	17	13	O	Interrupt. This open drain output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{INT}$ will stay low until the processor reads the detect register or does a full reset.
$\overline{RD}$	14	-	I	Read. A low requests a read of the SSI 73K322L internal registers. Data cannot be output unless both $\overline{RD}$ and the latched $\overline{CS}$ are active or low.
RESET	25	20	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.

PARALLEL MICROPROCESSOR INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
$\overline{\text{WR}}$	13	-	I	Write. A low on this informs the SSI 73K322L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{\text{WR}}$. No data is written unless both $\overline{\text{WR}}$ and the latched $\overline{\text{CS}}$ are low.

SERIAL MICROPROCESSOR INTERFACE

A0-A2	-	5-7	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	-	8	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{\text{RD}}$ pin. $\overline{\text{RD}}$ low outputs data. $\overline{\text{RD}}$ high inputs data.
$\overline{\text{RD}}$	-	10	I	Read. A low on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{\text{RD}}$ signal will initiate a read from the addressed register. The $\overline{\text{RD}}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{\text{RD}}$ signal is active.
$\overline{\text{WR}}$	-	9	I	Write. A low on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{\text{WR}}$ low. Data is written on the rising edge of $\overline{\text{WR}}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{\text{CS}}$ are removed and replaced with the pins; A0, A1, A2, DATA, and an unconnected pin. Also, the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ controls are used differently.

The Serial Control mode is provided in the parallel control versions by tying ALE high and $\overline{\text{CS}}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

DTE USER INTERFACE

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
EXCLK	19	15	I	External Clock. This signal is used only in synchronous DPSK transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous DPSK transmit data available on the TXD pin. Also used for serial control interface.

RS-232 INTERFACE (Continued)

NAME	28-PIN	22-PIN	TYPE	DESCRIPTION
RXCLK	23	18	O	Receive Clock. The falling edge of this clock output is coincident with the transitions in the serial received DPSK data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x1200 (or 16 x 75) or 16 x 300 Hz baud data rate is output, respectively, for driving a UART.
RXD	22	17	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	18	14	O	Transmit Clock.This signal is used only in synchronous DPSK transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is 1200 Hz generated internally. In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200 (or 16 x 75) or 16 x 300 Hz baud clock, respectively for driving a UART.
TXD	21	16	I	Transmit Data Input. Serial data for transmission is applied on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (1200 or 300 baud) no clocking is necessary. DPSK must be 1200/600 bit/s +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE AND OSCILLATOR

RXA	27	22	I	Received modulated analog signal input from the telephone line interface.
TXA	16	12	O	Transmit analog output to the telephone line interface.
XTL1 XTL2	2 3	3 4	I I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal and two load capacitors to Ground. XTL2 can also be driven from an external clock.

REGISTER DESCRIPTIONS

Four 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0 and A1 address lines in serial mode, or the AD0 and AD1 lines in parallel mode. The AD0 and AD1 lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K322L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer and guard tones and RXD output gate used in the modem initial connect sequence. All registers are read/write except for DR which is read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION		TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010			RECEIVE DATA	UNSCR. MARKS	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/SPEC. TONE SELECT
CONTROL REGISTER 2 CR2	100				THESE REGISTER LOCATIONS ARE RESERVED FOR				
CONTROL REGISTER 3 CR3	101				USE WITH OTHER K-SERIES FAMILY MEMBERS				
ID REGISTER ID	110	ID	ID	ID	ID				

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ORIGINATE/ ANSWER
		0=1200 BIT/S DPSK 1=600 BIT/S DPSK 0=V.23 FSK 1=V.21 FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYNCH 8 BITS/CHAR 0101=ASYNCH 9 BITS/CHAR 0110=ASYNCH 10 BITS/CHAR 0111=ASYNCH 11 BITS/CHAR 1100=FSK				0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	IN V.21 OR V.22 MODE: 0=ANSWER 1=ORIGINATE IN V.23 MODE : 0=RECEIVE @ 1200 BIT/S, TRANSMIT @ 75 BIT/S 1=RECEIVE @ 75 BIT/S, TRANSMIT @ 1200 BIT/S
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=DISABLE 1=ENABLE	0=NORMAL 1=BYPASS SCRAMBLER 1=ADD EXTRA PHASE EQ. IN V.23 ONLY	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	▨	▨	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE	CALL PROGRESS	LONG LOOP
				OUTPUTS RECEIVED DATA STREAM		0=CONDITION NOT DETECTED 1=CONDITION DETECTED			
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2 V.23 FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/ SPECIAL TONE
		RXD PIN 0=NORMAL 1=TRI STATE	0=OFF 1=ON	0=OFF 1=ON	0=DATA 1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS.	0=NORMAL 1=ALLOWS V.23 FULL DUPLEX OPERATION		0=1800 Hz G.T. (V.22). 2225 Hz ANS TONE GENERATED, FSK MARK DETECT SELECTED 1=550 Hz G.T. (V.22) 2100 Hz ANS TONE GENERATED & DETECTED (V.21, V.22) 1300 Hz DETECTED (V.23)
ID REGISTER 10	110	ID	ID	ID	ID	▨	▨	▨	▨

00XX=73K212, 322, 321
01XX=73K221, 302
10XX=73K222
1100=73K224
1110=73K324
1101=73K312

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s).
		1	Selects originate mode (transmit in low band, receive in high band or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s).
			Note: This bit works with TR bit D0 to program special tones detected in Tone Register. See detect and tone registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Answer tone and DTMF TX control require TX enable.
D5, D4, D3, D2	Transmit Mode	D5 D4 D3 D2	
		0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 1200 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 1200 Hz ± 0.01% clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects DPSK asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects DPSK asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects DPSK asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects DPSK asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and 1 or 2 stop bits).
		1 1 0 0	Selects FSK operation.

CONTROL REGISTER 0 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	▨	TRANSMIT MODE 3	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D6		0	Not used; must be written as a "0."
D7	Modulation Option	D7 D5 D4	Selects:
		0 0 X	PSK asynchronous mode at 1200 bit/s.
		1 0 X	PSK asynchronous mode at 600 bit/s.
		0 1 1	FSK CCITT V.23 mode.
		1 1 1	FSK CCITT V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same center frequency as the transmitter. To squelch the TXA pin, transmit enable must be forced low.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit carrier from TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, Tone) are reset to zero. The output of the CLK pin will be set to the crystal frequency.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTER.	BYPASS SCRAMB/ ADD PH. EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D3	CLK Control	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate, output at CLK pin in DPSK modes only.
D4	Bypass Scrambler/	0	Selects normal operation. DPSK data is passed through scrambler.
	Add Phase Equalization	1	Selects Scrambler Bypass. DPSK data is routed around scrambler in the transmit path. In V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect	0	Disables interrupt at $\overline{\text{INT}}$ pin.
		1	Enables $\overline{\text{INT}}$ output. An interrupts will be generated with a change in status of DR bits D1-D4. The special tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
D7, D6	Transmit Pattern	D7 D6	
		0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	▨	▨	RECEIVE DATA	UNSCR. MARK	CARR. DETECT	SPECIAL TONE	CALL PROG.	LONG LOOP

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Long Loop	0	Indicates normal received signal.
		1	Indicates low received signal level.
D1	Call Progress Detect	0	No call progress tone detected.
		1	Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0	No special tone detected as programmed by CR0 bit D0 and Tone Register bit D0.
		1	Special tone detected. The detected tone is:
			(1) 2100 Hz answer tone if D0 of TR=1 and the device is in V.21 or V.22 originate mode.
			(2) 1300 Hz calling tone if D0 of TR=1 and the device is in V.21, or V.22 answer mode.
			(3) an FSK mark in the mode the device is set to receive.
			Tolerance on special tones is ±3%.
D3	Carrier Detect	0	No carrier detected in the receive channel.
		1	Indicated carrier has been detected in the received channel.
D4	Unscrambled Mark	0	No unscrambled mark.
		1	Indicates detection of unscrambled marks in the received data. A valid indication requires that unscrambled marks be received for > 165.5 ± 6.5 ms.
D5	Receive Data		Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6, D7			Not used.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ SP. TONE/ SELECT

BIT NO.	NAME	CONDITION	DESCRIPTION
		D6 D5 D4 D0	D0 interacts with bits D6, D4, and CR0 as shown.
D0	DTMF 0	X X 1 X	Transmit DTMF tones.
	Guard Tone/ Answer Tone	1 X 0 0	Select 1800 Hz guard tone if in V.22 and answer mode in CR0.
	Special Tone/ Detect/Select	1 X 0 1	Select 550 Hz guard tone if in V.22 and answer mode in CR0.
		X X 0 0	Mark of an FSK mode selected in CR0 is to be detected in D2 of DR.
		X X 0 1	2100 Hz answer tone will be detected in D2 of DR if V.21 or V.22 originate mode is selected in CR0.
			1300 Hz calling tone will be detected in D2 of DR if V.21, or V.22 answer mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz Answer Tone
		X 1 0 1	Transmit 2100 Hz Answer Tone
		D4 D1	D1 interacts with D4 as shown.
D1	DTMF 1/ Overspeed	0 0	Asynchronous DPSK 1200 or 600 bit/s +1.0% -2.5%.
		0 1	Asynchronous DPSK 1200 or 600 bit/s +2.3% -2.5%.
D2	DTMF 2/ V.23 FDX	0	Half-duplex asymetric operation in V.23 mode.
		1	Full-duplex (4-wire) operation in V.23 mode.
		D3 D2 D1 D0	
D3, D2, D1, D0	DTMF 3, 2, 1, 0	0 0 0 0 - 1 1 1 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) are set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3 D2 D1 D0	TONES LOW HIGH
1	0 0 0 1	697 1209
2	0 0 1 0	697 1336
3	0 0 1 1	697 1477
4	0 1 0 0	770 1209
5	0 1 0 1	770 1336
6	0 1 1 0	770 1477
7	0 1 1 1	852 1209

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ V.23 FDX	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ SPECIAL TONE SEL

<table>
<tr><th>BIT NO.</th><th>NAME</th><th>CONDITION</th><th colspan="7">DESCRIPTION</th></tr>
<tr><td rowspan="11">D3, D2, D1, D0
(Cont.)</td><td rowspan="11"></td><td rowspan="11"></td><td rowspan="2">KEYBOARD EQUIVALENT</td><td colspan="4">DTMF CODE</td><td colspan="2">TONES</td></tr>
<tr><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>LOW</td><td>HIGH</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>852</td><td>1336</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td><td>852</td><td>1477</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>941</td><td>1336</td></tr>
<tr><td>*</td><td>1</td><td>0</td><td>1</td><td>1</td><td>941</td><td>1209</td></tr>
<tr><td>#</td><td>1</td><td>1</td><td>0</td><td>0</td><td>941</td><td>1477</td></tr>
<tr><td>A</td><td>1</td><td>1</td><td>0</td><td>1</td><td>697</td><td>1633</td></tr>
<tr><td>B</td><td>1</td><td>1</td><td>1</td><td>0</td><td>770</td><td>1633</td></tr>
<tr><td>C</td><td>1</td><td>1</td><td>1</td><td>1</td><td>852</td><td>1633</td></tr>
<tr><td>D</td><td>0</td><td>0</td><td>0</td><td>0</td><td>941</td><td>1633</td></tr>
<tr><td rowspan="2">D4</td><td rowspan="2">Transmit DTMF</td><td>0</td><td colspan="7">Disable DTMF.</td></tr>
<tr><td>1</td><td colspan="7">Activate DTMF.The selected DTMF tones are transmitted continuously when this bit is high. TX DTMF overrides all other transmit functions.</td></tr>
<tr><td rowspan="2">D5</td><td rowspan="2">Transmit Answer Tone</td><td>0</td><td colspan="7">Disables answer tone generator.</td></tr>
<tr><td>1</td><td colspan="7">Enables answer tone generator. A 2100 Hz answer tone will be transmitted continuously when the transmit enable bit is set. The device must be in answer mode. To transmit answer tone, the device must be in DPSK answer mode.</td></tr>
<tr><td rowspan="2">D6</td><td rowspan="2">TX Guard or Calling Tone</td><td>0</td><td colspan="7">Disables guard/calling tone generator.</td></tr>
<tr><td>1</td><td colspan="7">Transmit guard tone if in V.22 and answering; otherwise transmit calling tone, in any other mode including V.23 mode.</td></tr>
<tr><td rowspan="2">D7</td><td rowspan="2">RXD Output Control</td><td>0</td><td colspan="7">Enables RXD pin. Receive data will be output on RXD.</td></tr>
<tr><td>1</td><td colspan="7">Disables RXD pin. The RXD pin reverts to a high impedance with internal weak pull-up resistor.</td></tr>
</table>

ID REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
ID 110	ID	ID	ID	ID				

BIT NO.	NAME	CONDITION	DESCRIPTION
		D7 D6 D5 D4	Indicates Device:
D7, D6, D5 D4	Device Identification Signature	0 0 X X	SSI 73K212(L), 73K321L or 73K322L or 73K321L
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
VDD Supply Voltage	14	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Applied Voltage	-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
TA, Operating Free-Air Temp.		-40		+85	°C
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
External Components (Refer to Application section for placement.)					
VREF Bypass Capacitor	(External to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass Capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass Capacitor 1	(External to GND)	0.1			µF
VDD Bypass Capacitor 2	(External to GND)	22			µF
XTL1 Load Capacitor	Depends on crystal characteristics;			40	pF
XTL2 Load Capacitor	from pin to GND			20	

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD = recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	ISET Resistor = 2 MΩ				
IDDA, Active	CLK = 11.0592 MHz		8	12	mA
IDD1, Power-down	CLK = 11.0592 MHz			4	mA
IDD2, Power-down	CLK = 19.200 KHz			3	mA
Digital Inputs					
VIH, Input High Voltage					
Reset, XTL1, XTL2		3.0		VDD	V
All other inputs		2.0		VDD	V
VIL, Input Low Voltage		0		0.8	V
IIH, Input High Current	VI = VIH Max			100	µA
IIL, Input Low Current	VI = VIL Min	-200			µA
Reset Pull-down Current	Reset = VDD	1		50	µA
Input Capacitance	All Digital Input Pins			10	pF
Digital Outputs					
VOH, Output High Voltage	IOH MIN = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO MAX = 1.6 mA			0.4	V
VOL, CLK Output	IO = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-1		-50	µA
CMAX, CLK Output	Maximum Capacitive Load			15	pF
Capacitance					
Inputs	Capacitance, all Digital Input pins			10	pF
XTAL1, 2 Load Capacitors	Depends on crystal characteristics	15		60	pF
CLK	Maximum Capacitive Load			15	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = Recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
DPSK Modulator					
Carrier Suppression	Measured at TXA	45			dB
Output Amplitude	TX scrambled marks	-11	-10	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.35		+0.35	%
Transmit Level	Transmit Dotting Pattern	-11	-10	-9	dBm0
Harmonic Distortion in 700-2900 Hz band	THD in the alternate band DPSK or FSK		-60	-50	dB
Output Bias Distortion	Transmit Dotting Pattern In ALB @ RXD		±3		%
Total Output Jitter	Random Input in ALB @ RXD	-10		+10	%
DTMF Generator					
Freq. Accuracy	Must be in V.22 mode	-.25		+.25	%
Output Amplitude	Low Band, V.22 mode	-10	-9	-8	dBm0
Output Amplitude	High Band, V.22 mode	-8	-7	-6	dBm0
Twist	High-Band to Low-Band, V.22 mode	1.0	2.0	3.0	dB
Long Loop Detect	With Sinusoid	-38		-28	dBm0
Dynamic Range	Refer to Performance Curves		45		dB

Note: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Call Progress Detector					
Detect Level	-3 dB points in 285 and 675 Hz	-38			dBm0
Reject Level	Test signal is a 460 Hz sinusoid			-45	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			40	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			40	ms
Hysteresis		2			dB
Carrier Detect					
Threshold	DPSK or FSK receive data	-48		-43	dBm0
Delay Time					
V.21		10		20	ms
V.22		15		32	ms
V.23 Forward Channel		6		12	ms
V.23 Back Channel		25		40	ms
Hold Time					
V.21		6		20	ms
V.22		10		24	ms
V.23 Forward Channel		3		8	ms
V.23 Back Channel		10		25	ms
Hysteresis		2			dB
Special Tone Detectors					
Detect Level	See definitions for TR bit D0 mode	-48		-43	dBm0
Delay Time					
2100 Hz answer tone		10		25	ms
1300 Hz calling tone		10		25	ms
390 Hz V.23 back channel mark		20		65	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Special Tone Detectors (Continued)					
980 or 1650 Hz V.21 marks		10		25	ms
Hold Time					
2100 Hz answer tone		4		15	ms
1300 Hz calling tone		3		10	ms
390 Hz V.23 back channel mark		10		25	ms
980 or 1650 Hz V.21 marks		5		15	ms
Hysteresis		2			dB
Detect Freq. Range	Any Special Tone	-3		+3	%
Output Smoothing Filter					
Output load	TXA pin; FSK Single Tone out for THD = -50 dB in 0.3 to 3.4 kHz	10		 50	kΩ pF
Out of Band Energy	Frequency >12 kHz in all modes			-60	dBm0
Output Impedance	TXA pin, TXA enabled		20	50	Ω
Clock Noise	TXA pin; 76.8 kHz or 122.88 kHz in V.23 main channel		0.1	0.4	mVrms
Carrier VCO					
Capture Range	Originate or Answer	-10		+10	Hz
Capture Time	-10 Hz to +10 Hz Carrier Freq. Change Assum.		40	100	ms
Recovered Clock					
Capture Range	% of frequency center frequency (center at 1200 Hz)	-625		+625	ppm
Data Delay Time	Analog data in at RXA pin to receive data valid at RXD pin		30	50	ms

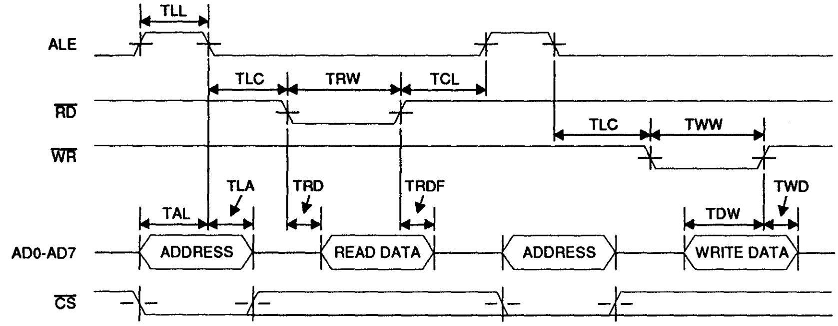
DYNAMIC CHARACTERISTICS AND TIMING (Continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Guard Tone Generator					
Tone Accuracy	550 or 1800 Hz	-20		+20	Hz
Tone Level (Below DPSK Output)	550 Hz	-4.0	-3.0	-2.0	dB
	1800 Hz	-7.0	-6.0	-5.0	dB
Harmonic Distortion 700 to 2900 Hz	550 Hz			-50	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{\text{CS}}$/Addr. setup before ALE Low	25			ns
TLA	$\overline{\text{CS}}$/Addr. hold after ALE Low	20			ns
TLC	ALE Low to $\overline{\text{RD}}$/$\overline{\text{WR}}$ Low	30			ns
TCL	$\overline{\text{RD}}$/$\overline{\text{WR}}$ Control to ALE High	-5			ns
TRD	Data out from $\overline{\text{RD}}$ Low	0		140	ns
TLL	ALE width	30			ns
TRDF	Data float after $\overline{\text{RD}}$ High	0		5	ns
TRW	$\overline{\text{RD}}$ width	200		25000	ns
TWW	$\overline{\text{WR}}$ width	140		25000	ns
TDW	Data setup before $\overline{\text{WR}}$ High	40			ns
TWD	Data hold after $\overline{\text{WR}}$ High	10			ns
TCKD	Data out after EXCLK Low			200	ns
TCKW	$\overline{\text{WR}}$ after EXCLK Low	150			ns
TDCK	Data setup before EXCLK Low	150			ns
TAC	Address setup before control*	50			ns
TCA	Address hold after control*	50			ns
TWH	Data Hold after EXCLK	20			

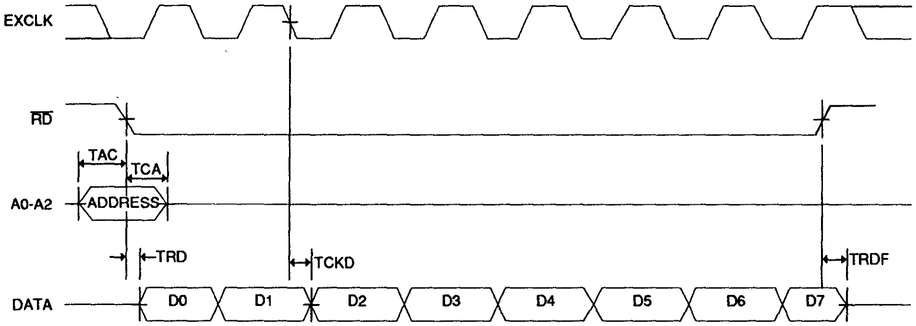
* Control for setup is the falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$.
Control for hold is the falling edge of $\overline{\text{RD}}$ or the rising edge of $\overline{\text{WR}}$.

TIMING DIAGRAMS

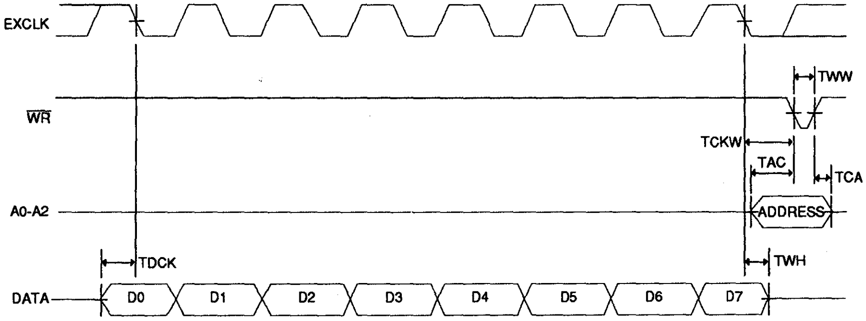
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



SSI 73K322L
CCITT V.23, V.22, V.21
Single-Chip Modem

APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

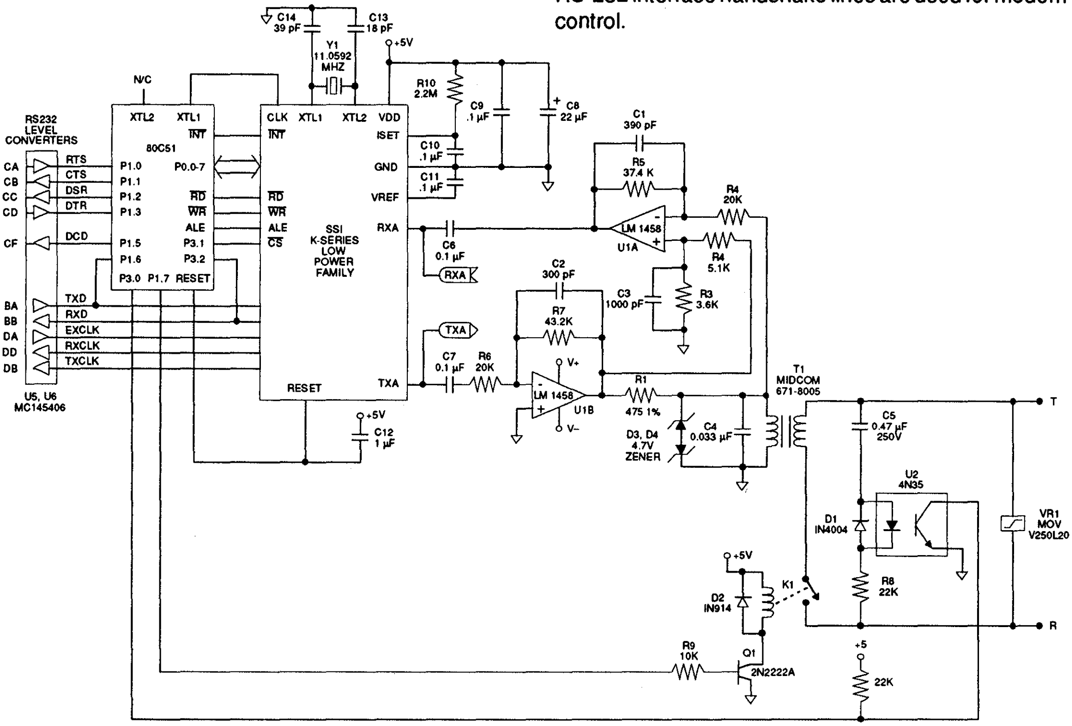


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

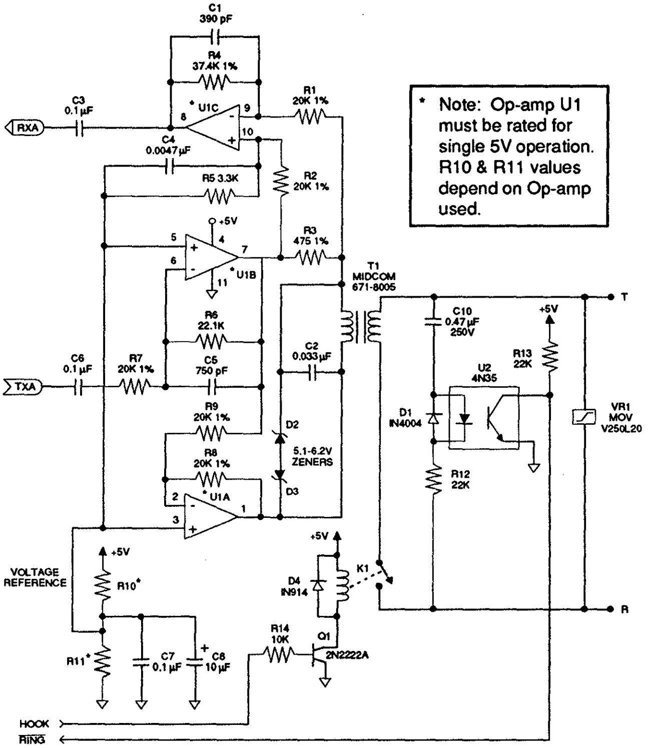
DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V Hybrid Version

SSI 73K322L
CCITT V.23, V.22, V.21
Single-Chip Modem

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

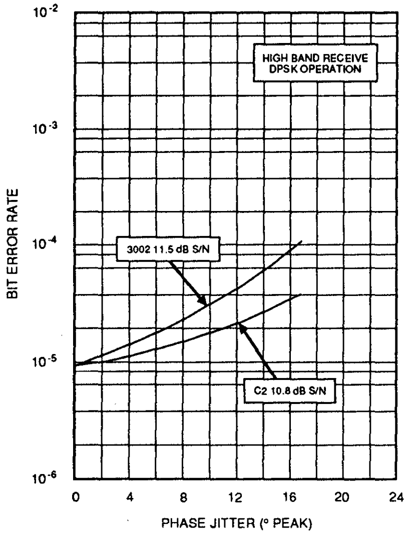
BER vs. S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

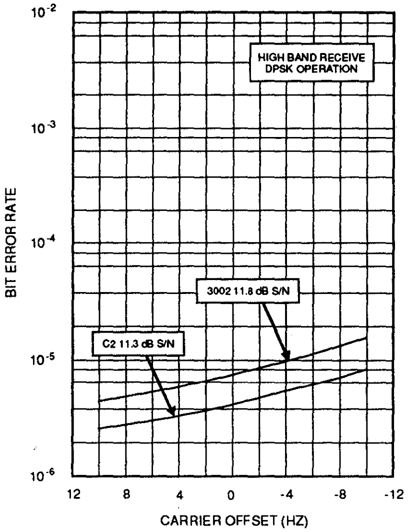
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

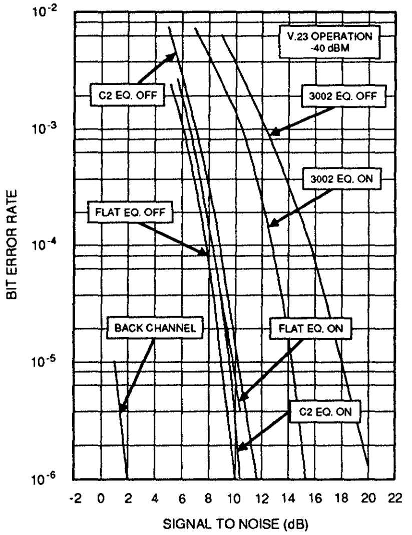
***SSI 73K322L
BER vs PHASE JITTER**



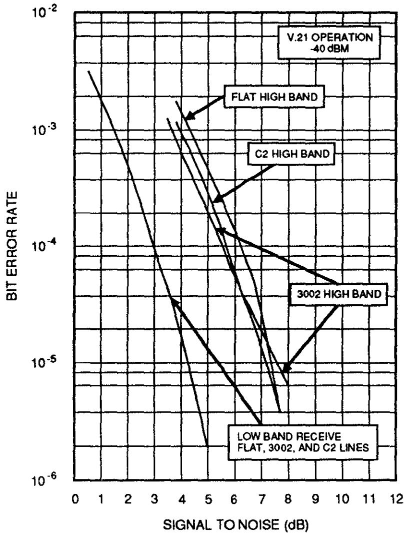
**SSI 73K322L
BER vs CARRIER OFFSET**



***SSI 73K322L
BER vs S/N (V.23 ONLY)****



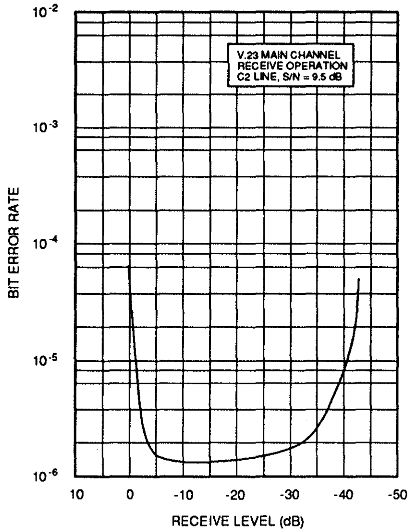
**SSI 73K322L
BER vs SIGNAL TO NOISE**



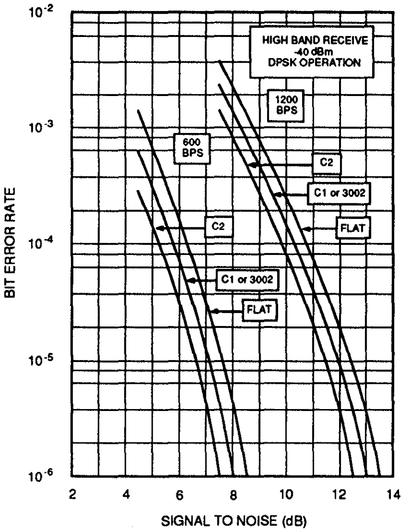
* = “EQ On” Indicates bit CR1 D4 is set for additional phase equalization.

** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

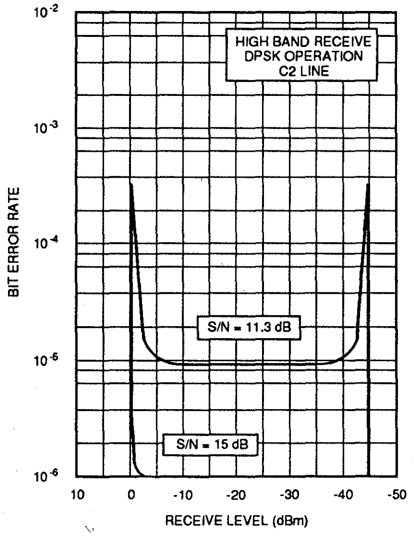
***SSI 73K322**
BER vs RECEVE LEVEL (V.23)



***SSI 73K322L**
BER vs SIGNAL TO NOISE



***SSI 73K322**
BER vs RECEVE LEVEL



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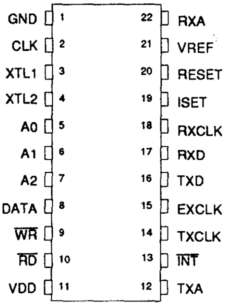
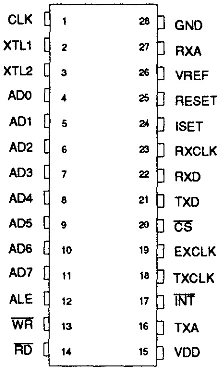
SSI 73K322L
CCITT V.23, V.22, V.21
Single-Chip Modem

PACKAGE PIN DESIGNATIONS

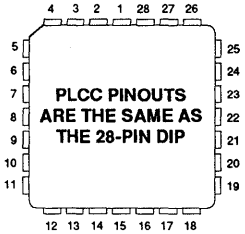
(Top View)



400-Mil
22-Pin DIP



600-Mil
28-Pin DIP



28-Pin
PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K322L with Parallel Bus Interface 28-Pin 5V Supply Plastic Dual-In-Line	73K322L-IP	73K322L-IP
Plastic Leaded Chip Carrier	73K322L-IH	73K322L-IH
SSI 73K322L with Serial Interface 22-Pin 5V Supply Plastic Dual-In-Line	73K322SL-IP	73K322SL-IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

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Notes:

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SSI 73K324L
CCITT V.22bis, V.22, V.21, V.23, Bell 212A Single-Chip Modem

Preliminary Data

December 1992

DESCRIPTION

The SSI 73K324L is a highly integrated single-chip modem IC which provides the functions needed to design a quad-mode CCITT and Bell 212A compatible modem capable of operation over dial-up lines. The SSI 73K324L adds V.23 capability to the CCITT modes of Silicon Systems' 73K224 one-chip modem, allowing a one-chip implementation in designs intended for European markets which require this added modulation mode. The SSI 73K324L offers excellent performance and a high level of functional integration in a single IC. The device supports V.22bis, V.22, Bell 212A, V.21, and V.23 operating modes, allowing both synchronous and asynchronous operation as defined by the appropriate standard.

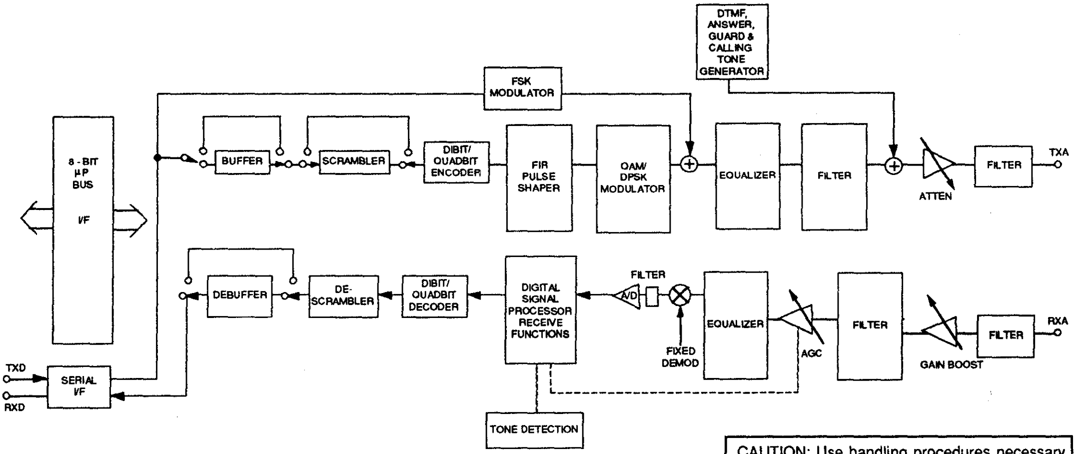
The SSI 73K324L is designed to appear to the Systems Engineer as a microprocessor peripheral, and will easily interface with popular one-chip microcontrollers (80C51 typical) for control of modem functions through its 8-bit multiplexed address/data bus. A serial control bus is available for applications not requiring a parallel interface. An optional package with only the serial control bus is also available. Data communications occurs through a separate serial port.

(Continued)

FEATURES

- **One chip multi-mode CCITT V.22bis, V.22, V.21, V.23 and Bell 212A compatible modem data pump**
- **FSK (75, 300, 1200 bit/s), DPSK (600, 1200 bit/s), or QAM (2400 bit/s) encoding**
- **Pin and software compatible with other SSI K-Series family one-chip modems**
- **Interfaces directly with standard microprocessors (8048, 80C51 typical)**
- **Serial and parallel microprocessor bus for control**
- **Selectable asynch/synch with internal buffer/ debuffer and scrambler/descrambler functions**
- **All synchronous (internal, external, slave) and asynchronous operating modes**
- **Adaptive equalization for optimum performance over all lines**
- **Programmable transmit attenuation (16 dB, 1 dB steps), and selectable receive boost (+18 dB)**
- **Call progress, carrier, answer tone, unscrambled mark, S1, SCT (900 Hz) calling tone (1300 Hz) and signal quality monitors**
- **DTMF, answer, calling, SCT and guard tone generators**
- **Test modes available: ALB, DL, RDL; Mark, Space and Alternating bit pattern generators**
- **CMOS technology for low power consumption**
- **4-wire full duplex operation in all modes**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 73K324L offers full hardware and software compatibility with other products in Silicon Systems' K-Series family of single-chip modems, allowing system upgrades with a single component change. The SSI 73K324L is ideal for use in free-standing or integral system modem products where full-duplex 2400 bit/s operation with alternate mode capability is required. Its high functionality, low power consumption, and efficient packaging simplify design requirements and increase system reliability. A complete modem requires only the addition of the phone line interface, a control microprocessor, and RS-232 level converters for a typical system.

The SSI 73K324L is designed to provide a complete V.22bis, V.22, Bell 212A, V.21, and V.23 compatible modem on a chip. Many functions were included to simplify implementation in typical modem designs. In addition to the basic 2400 bit/s QAM, 1200/600 bit/s DPSK and 1200/300/75 bit/s FSK modulator/demodulator sections, the device also includes synch/asynch buffering, DTMF, answer, soft carrier, guard, and calling tone generator capabilities. Handshake pattern detectors simplify control of connect sequences, and precise tone detectors allow accurate detection of call progress, answer, calling, and soft carrier turn off tones. All operating modes defined by the incorporated standards are included, and test modes are provided. Most functions are selectable as options, and logical defaults are provided. The device can be directly interfaced to a microprocessor via its 8-bit multiplexed address/data bus for control and status monitoring. Data communications takes place through a separate serial port. Data may also be sent and received through the control registers. This simplifies designs requiring speed buffering, error control and compression.

FUNCTIONAL DESCRIPTION

QAM MODULATOR/DEMODULATOR

The SSI 73K324L encodes incoming data into quadbits represented by 16 possible signal points with specific phase and amplitude levels. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited telephone network. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator, although more complex, essentially reverses this procedure while also recovering the data clock from the incoming signal. Adaptive equalization corrects for varying line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

The SSI 73K324L modulates a serial bit stream into di-bit pairs that are represented by four possible phase shifts as prescribed by the Bell 212A/V.22 standards. The baseband signal is then filtered to reduce intersymbol interference on the bandlimited 2-wire PSTN line. Transmission occurs on either a 1200 Hz (originate mode) or 2400 Hz carrier (answer mode). Demodulation is the reverse of the modulation process, with the incoming analog signal eventually decoded into di-bits and converted back to a serial bit stream. The demodulator also recovers the clock which was encoded into the analog signal during modulation. Demodulation occurs using either a 1200 Hz carrier (answer mode or ALB originate mode) or a 2400 Hz carrier (originate mode or ALB answer mode). The SSI 73K324L use a phase locked loop coherent demodulation technique that offers excellent performance. Adaptive equalization is also used in DPSK modes for optimium operation with varying lines.

FSK MODULATOR/DEMODULATOR

The FSK modulator/demodulator produces a frequency modulated analog output signal using two discrete frequencies to represent the binary data. V.21 frequencies of 980 and 1180 Hz (originate mark and space), or 1650 and 1850 Hz (answer mark and space) are used in V.21 mode. V. 23 mode uses 1300 and 2100 Hz for the main channel or 390 and 450 Hz for the back channel. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value. The rate converter and scrambler/descrambler are automatically bypassed in the FSK modes.

PASSBAND FILTERS AND EQUALIZERS

High and low band filters are included to shape the amplitude and phase response of the transmit and receive signals and to provide compromise delay equalization as well as rejection of out-of-band signals. The transmit signal filtering corresponds to a $\sqrt{75\%}$ raised cosine frequency response characteristic.

ASYNCHRONOUS MODE

The asynchronous mode is used for communication with asynchronous terminals which may transfer data at 600, 1200, or 2400 bit/s +1%, -2.5% even though the modem's output is limited to the nominal bit rate ±.01% in DPSK and QAM modes. When transmitting in this mode the serial data on the TxD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal that is the nominal bit rate ±.01%. This signal is then routed to a data scrambler and into the analog modulator where di-bit or quad-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for handshaking and synchronous operation as selected. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal at no greater than the bit rate plus 1%. An incoming break signal (low through two characters) will be recognized and passed through without incorrectly inserting a stop bit.

The SYNC/ASYNC converter has an extended overspeed mode which allows selection of an output speed range of either +1% or +2.3%. In the extended overspeed mode, some stop bits are output at 7/8 the normal width.

Both the SYNC/ASYNC rate converter and the data descrambler are automatically bypassed in the FSK modes.

SYNCHRONOUS MODE

Synchronous operation is possible only in the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a clock and no variation in data transfer rate is allowable. Serial input data appearing at TXD must be valid on the rising edge of TXCLK.

TXCLK is an internally derived 1200 or 2400 Hz signal in internal mode and is connected internally to the RXCLK pin in slave mode. Receive data at the RXD pin is clocked out on the falling edge of RXCLK. The asynch/synch converter is bypassed when synchronous mode is selected and data is transmitted out at essentially the same rate as it is input.

PARALLEL CONTROL INTERFACE

Eight 8-bit registers are provided for control, option select, and status monitoring. These registers are addressed with the AD0, AD1, and AD2 multiplexed address lines (latched by ALE) and appear to a control microprocessor as seven consecutive memory locations. Six contol registers are read/write. The detect and ID registers are read only and cannot be modified except by modem response to monitored parameters.

SERIAL CONTROL INTERFACE

The serial command mode allows access to the SSI 73K324 control and status registers via a serial control port. In this mode the A0, A1, and A2 lines provide register addresses for data passed through the DATA pin under control of the $\overline{RD}$ and $\overline{WR}$ lines. A read operation is initiated when the $\overline{RD}$ line is taken low. The next eight cycles of EXCLK will then transfer out eight bits of the selected addresss location LSB first. A write takes place by shifting in eight bits of data LSB first for eight consectuive cycles of EXCLK. $\overline{WR}$ is then pulsed low and data transfer into the selected register occurs on the rising edge of $\overline{WR}$.

TONE GENERATOR

The DTMF generator controls the sending of the sixteen standard DTMF tone pairs. The tone pair sent is determined by selecting TRANSMIT DTMF (bit D4) and the 4 DTMF bits (D0-D3) of the TONE register. Transmission of DTMF tones from TXA is gated by the TRANSMIT ENABLE bit of CR0 (bit D1) as with all other analog signals.

FULL DUPLEX OPERATION

Four-wire full duplex operation is allowed in all modes. This feature allows transmission and reception in the same band for four wire applications only.

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
GND	I	System Ground.
VDD	I	Power supply input, 5V -5% +10%. Bypass with .22 µF and 22 µF capacitors to GND.
VREF	O	An internally generated reference voltage. Bypass with .22 µF capacitor to GND.
ISET	I	Chip current reference. Sets bias current for op-amps. The chip current is set by connecting this pin to VDD through a 2 MΩ resistor. Iset should be bypassed to GND with a .22 µF capacitor.

PARALLEL MICROPROCESSOR INTERFACE

ALE	I	Address latch enable. The falling edge of ALE latches the address on AD0-AD2 and the chip select on $\overline{\text{CS}}$.
AD0- AD7	I/O / Tristate	Address/data bus.These bidirectional tri-state multi-plexed lines carry information to and from the internal registers.
$\overline{\text{CS}}$	I	Chip select. A low on this pin allows a read cycle or a write cycle to occur. AD0-AD7 will not be driven and no registers will be written if $\overline{\text{CS}}$ (latched) is not active. $\overline{\text{CS}}$ is latched on the falling edge of ALE.
CLK	O	Output clock. This pin is selectable under processor control to be either the crystal frequency (for use as a processor clock) or 16 x the data rate for use as a baud rate clock in QAM/DPSK modes only. The pin defaults to the crystal frequency on reset.
$\overline{\text{INT}}$	O	Interrupt. This open drain weak pullup, output signal is used to inform the processor that a detect flag has occurred. The processor must then read the detect register to determine which detect triggered the interrupt. $\overline{\text{INT}}$ will stay active until the processor reads the detect register or does a full reset.
$\overline{\text{RD}}$	I	Read. A low requests a read of the SSI 73K324L internal registers. Data cannot be output unless both $\overline{\text{RD}}$ and the latched $\overline{\text{CS}}$ are active or low.
RESET	I	Reset. An active high signal on this pin will put the chip into an inactive state. All control register bits (CR0, CR1, CR2, CR3, Tone) will be reset. The output of the CLK pin will be set to the crystal frequency. An internal pull down resistor permits power on reset using a capacitor to VDD.
$\overline{\text{WR}}$	I	Write. A low on this informs the SSI 73K224L that data is available on AD0-AD7 for writing into an internal register. Data is latched on the rising edge of $\overline{\text{WR}}$. No data is written unless both $\overline{\text{WR}}$ and the latched $\overline{\text{CS}}$ are low.

Note: The serial control mode is provided in the parallel versions by tying ALE high and $\overline{\text{CS}}$ low. In this configuration AD7 becomes DATA and AD0, AD1 and AD2 become A0, A1 and A2, respectively.

RS-232 INTERFACE

NAME	TYPE	DESCRIPTION
EXCLK	I	External Clock. This signal is used in synchronous transmission when the external timing option has been selected. In the external timing mode the rising edge of EXCLK is used to strobe synchronous transmit data available on the TXD pin. Also used for serial control interface.
RXCLK	O/Tristate	Receive Clock Tri-statable. The falling edge of this clock output is coincident with the transitions in the serial received DPSK/QAM data output. The rising edge of RXCLK can be used to latch the valid output data. RXCLK will be valid as long as a carrier is present. In V.23 or V.21 mode a clock which is 16 x 1200/75 or 16 x 300 Hz data rate is output, respectively.
RXD	O	Received Data Output. Serial receive data is available on this pin. The data is always valid on the rising edge of RXCLK when in synchronous mode. RXD will output constant marks if no carrier is detected.
TXCLK	O/Tristate	Transmit Clock Tri-statable. This signal is used in synchronous DPSK/QAM transmission to latch serial input data on the TXD pin. Data must be provided so that valid data is available on the rising edge of the TXCLK. The transmit clock is derived from different sources depending upon the synchronization mode selection. In Internal Mode the clock is generated internally (2400 Hz for QAM, 1200 Hz for DPSK or 600 Hz for half-speed DPSK). In External Mode TXCLK is phase locked to the EXCLK pin. In Slave Mode TXCLK is phase locked to the RXCLK pin. TXCLK is always active. In V.23 or V.21 mode the output is a 16 x 1200/75 or 16 x 300 Hz clock, respectively.
TXD	I	Transmit Data Input. Serial data for transmission is input on this pin. In synchronous modes, the data must be valid on the rising edge of the TXCLK clock. In asynchronous modes (2400/1200/600 bit/s, or 75/300 baud) no clocking is necessary. DPSK/QAM data must be +1%, -2.5% or +2.3%, -2.5 % in extended overspeed mode.

ANALOG INTERFACE

RXA	I	Received modulated analog signal input from the phone line.
TXA	O	Transmit analog output to the phone line.
XTL1	I	These pins are for the internal crystal oscillator requiring a 11.0592 MHz parallel mode crystal. Two capacitors from these pins to ground are also required for proper crystal operation. Consult crystal manufacturer for proper values. XTL2 can also be driven from an external clock.
XTL2	I/O	

PIN DESCRIPTION (continued)

SERIAL MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
A0-A2	I	Register Address Selection. These lines carry register addresses and should be valid during any read or write operation.
DATA	I/O	Serial Control Data. Data for a read/write operation is clocked in or out on the falling edge of the EXCLK pin. The direction of data flow is controlled by the $\overline{RD}$ pin. $\overline{RD}$ low outputs data. $\overline{RD}$ high inputs data.
$\overline{RD}$	I	Read. A low on this input informs the SSI 73K322L that data or status information is being read by the processor. The falling edge of the $\overline{RD}$ signal will initiate a read from the addressed register. The $\overline{RD}$ signal must continue for eight falling edges of EXCLK in order to read all eight bits of the referenced register. Read data is provided LSB first. Data will not be output unless the $\overline{RD}$ signal is active.
$\overline{WR}$	I	Write. A low on this input informs the SSI 73K322L that data or status information has been shifted in through the DATA pin and is available for writing to an internal register. The normal procedure for a write is to shift in data LSB first on the DATA pin for eight consecutive falling edges of EXCLK and then to pulse $\overline{WR}$ low. Data is written on the rising edge of $\overline{WR}$.

Note: In the serial, 22-pin version, the pins AD0-AD7, ALE and $\overline{CS}$ are removed and replaced with the pins; A0, A1, A2, DATA, and EXCLK. Also, the $\overline{RD}$ and $\overline{WR}$ controls are used differently.

REGISTER DESCRIPTIONS

Eight 8-bit internal registers are accessible for control and status monitoring. The registers are accessed in read or write operations by addressing the A0, A1 and A2 address lines in serial mode, or the AD0, AD1 and AD2 lines in parallel mode. The address lines are latched by ALE. Register CR0 controls the method by which data is transferred over the phone line. CR1 controls the interface between the microprocessor and the SSI 73K324L internal state. DR is a detect register which provides an indication of monitored modem status conditions. TR, the tone control register, controls the DTMF generator, answer, guard tones, SCT, calling tone, and RXD output gate used in the modem initial connect sequence. CR2 is the primary DSP control interface and CR3 controls transmit attenuation and receive gain adjustments. All registers are read/write except for DR and ID which are read only. Register control and status bits are identified below:

REGISTER BIT SUMMARY

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD - A0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
DETECT REGISTER DR	010	RECEIVE LEVEL	PATTERN S1 DET	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROGRESS DETECT	SIGNAL QUALITY
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD TONE/ SCT/CALLING TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ 4 WIRE FDX	DTMF1/ OVERSPEED	DTMF0/GUARD/ ANSWER/ CALLING/SCT
CONTROL REGISTER 2 CR2	100	0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	RESET DSP	TRAIN INHIBIT	EQUALIZER ENABLE
CONTROL REGISTER 3 CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
SPECIAL REGISTER SR	101		TX BAUD CLOCK	RX UNSCR. DATA		TXD SOURCE	SQ SELECT 1	SQ SELECT 0	
ID REGISTER ID	110	ID	ID	ID	ID	USER DEFINABLE PERSONALITY			

NOTE: When a register containing reserved control bits is written into, the reserved bits must be programmed as 0's.

SSI 73K324L
CCITT V.22bis, V.22, V.21, V.23, Bell 212A
Single-Chip Modem

REGISTER ADDRESS TABLE

	ADDRESS	DATA BIT NUMBER							
REGISTER	AD2 - AD0	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTER 0 CR0	000	MODULATION OPTION	MODULATION TYPE 1	MODULATION TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE
		QAM: 0=2400 BIT/S DPSK: 0=1200 BIT/S 1=600 BIT/S FSK: 0=V.23 1=V.21	10=QAM 00=DPSK 01=FSK		0000=PWR DOWN 0001=INT SYNCH 0010=EXT SYNCH 0011=SLAVE SYNCH 0100=ASYCH 8 BITS/CHAR 0101=ASYCH 9 BITS/CHAR 0110=ASYCH 10 BITS/CHAR 0111=ASYCH 11 BITS/CHAR 1X00=FSK			0=DISABLE TXA OUTPUT 1=ENABLE TXA OUTPUT	0=ANSWER 1=ORIGINATE in V.23 0=BC xmit 1=MC xmit
CONTROL REGISTER 1 CR1	001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INTERRUPT	BYPASS SCRAMBLER/ ADD PH. EQ. (V.23)	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0
		00=TX DATA 01=TX ALTERNATE 10=TX MARK 11=TX SPACE		0=OFF 1=ON	0=NORMAL 1=BYPASS SCRAMBLER	0=XTAL 1=16 X DATA RATE OUTPUT AT CLK PIN IN QAM/DPSK MODE ONLY	0=NORMAL 1=RESET	00=NORMAL 01=ANALOG LOOPBACK 10=REMOTE DIGITAL LOOPBACK 11=LOCAL DIGITAL LOOPBACK	
DETECT REGISTER DR	010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARKS DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CP TONE DETECT	SIGNAL QUALITY INDICATOR
		0=SIGNAL BELOW THRESHOLD 1=ABOVE THRESHOLD	0=NOT PRESENT 1=PATTERN FOUND	OUTPUTS RECEIVED DATA STREAM	0=CONDITION NOT DETECTED 1=CONDITION DETECTED				0=GOOD 1=BAD
TONE CONTROL REGISTER TR	011	RXD OUTPUT CONTROL	TRANSMIT GUARD/ CALLING/ SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF3	DTMF2/ V.23 FDX	DTMF1/ OVERSPEED	DTMF0/ GUARD/ ANSWER/ CALLING/SCT
		RXD PIN 0=NORMAL 1=TRI-STATE	0=OFF 1=ON	0=OFF 1=ON	1=TX DTMF	4 BIT CODE FOR 1 OF 16 DUAL TONE COMBINATIONS	0=NORMAL OPERATION 1=ALLOWS V.23 FULL DUPLEX OPERATION		GUARD: 0 - 1800 HZ 1 - 550 HZ ANSWER: 0 - 2225 HZ 1 - 2100 HZ CALLING: 0 - 1300 HZ SCT: 1 - 900 HZ
CONTROL REGISTER 2 CR2	100	MUST BE 0	SPECIAL REGISTER ACCESS	CALL INITIALIZE	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE
			0=ACCESS CR3 1=ACCESS SPECIAL REGISTER	0=DSP IN DEMOD MODE 1=DSP IN CALL PROGRESS MODE	0=NORMAL DOTTING 1=S1	0=RX=TX 1=RX=16 WAY	0=DSP INACTIVE 1=DSP ACTIVE	0=ADAPT EQ ACTIVE 1=ADAPT EQ FROZEN	0=ADAPT EQ IN INIT 1=ADAPT EQ OK TO ADAPT
CONTROL REGISTER 3 CR3	101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE GAIN BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0
		ALTERNATE TRANSMIT DATA SOURCE	0=CLOCK DRIVEN 1=CLOCK TRISTATE		0=NO BOOST 1=18 dB BOOST	0000-1111, SETS TRANSMIT ATTENUATOR 16 dB RANGE DEFAULT=0100 = -10 dbM0			
SPECIAL REGISTER SR	101	▨	TX BAUD CLOCK	RX UNSCR. DATA	▨	TXD SOURCE	SQ SELECT1	SQ SELECT0	▨
			OUTPUTS TXBAUD CLOCK	OUTPUTS UNSCR. DATA		0=TXD PIN 1=TX DATA CR3-D7	00=10^{-5} BER 01=10^{-6} BER 10=10^{-4} BER 11=10^{-3} BER		
ID REGISTER 10	110	ID	ID	ID	ID	USER DEFINABLE PERSONALITY			

00XX=73K212, 322, 321
01XX=73K221, 302
10XX=73K222
1100=73K224
1110=73K324
1101=73K312

CONTROL REGISTER 0

	D7	D6	D5	D4	D3	D2	D1	D0
CR0 000	MODUL. OPTION	MODUL. TYPE 1	MODUL. TYPE 0	TRANSMIT MODE 2	TRANSMIT MODE 1	TRANSMIT MODE 0	TRANSMIT ENABLE	ANSWER/ ORIGINATE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Answer/ Originate	0	Selects answer mode (transmit in high band, receive in low band or in V.23 HDX mode, receive at 1200 bit/s and transmit at 75 bit/s.)
		1	Selects originate mode (transmit in low band, receive in high band or in V.23 HDX mode, receive at 75 bit/s and transmit at 1200 bit/s.)
			Note: This bit works with Tone Register bits D0 and D6 to program special tones detected in the Detect Register. See Detect and Tone Registers.
D1	Transmit Enable	0	Disables transmit output at TXA.
		1	Enables transmit output at TXA.
			Note: Transmit Enable must be set to 1 to allow activation of Answer Tone, DTMF, or Carrier.
		D5 D4 D3 D2	
D5, D4, D3, D2	Transmit Mode	0 0 0 0	Selects power down mode. All functions disabled except digital interface.
		0 0 0 1	Internal synchronous mode. In this mode TXCLK is an internally derived 600, 1200 or 2400 Hz signal. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data is clocked out of RXD on the falling edge of RXCLK.
		0 0 1 0	External synchronous mode. Operation is identical to internal synchronous, but TXCLK is connected internally to EXCLK pin, and a 600, 1200 or 2400 Hz clock must be supplied externally.
		0 0 1 1	Slave synchronous mode. Same operation as other synchronous modes. TXCLK is connected internally to the RXCLK pin in this mode.
		0 1 0 0	Selects asynchronous mode - 8 bits/character (1 start bit, 6 data bits, 1 stop bit).
		0 1 0 1	Selects asynchronous mode - 9 bits/character (1 start bit, 7 data bits, 1 stop bit).
		0 1 1 0	Selects asynchronous mode - 10 bits/character (1 start bit, 8 data bits, 1 stop bit).
		0 1 1 1	Selects asynchronous mode - 11 bits/character (1 start bit, 8 data bits, Parity and/or 1 or 2 stop bits).
		1 X 0 0	Selects FSK operation.

CONTROL REGISTER 0 (Continued)

BIT NO.	NAME	CONDITION	DESCRIPTION
D6,D5	Modulation Type	D6 D5	
		1 0	QAM
		0 0	DPSK
		0 1	FSK
D7	Modulation Option	0	QAM selects 2400 bit/s. DPSK selects 1200 bit/s. FSK selects V.23 mode.
		1	DPSK selects 600 bit/s. FSK selects V.21 mode.

CONTROL REGISTER 1

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB/ ADD PH.EQ	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D1, D0	Test Mode	D1 D0	
		0 0	Selects normal operating mode.
		0 1	Analog loopback mode. Loops the transmitted analog signal back to the receiver, and causes the receiver to use the same carrier frequency as the transmitter. To squelch the TXA pin, transmit enable bit must be low. Tone Register bit D2 must be zero.
		1 0	Selects remote digital loopback. Received data is looped back to transmit data internally, and RXD is forced to a mark. Data on TXD is ignored.
		1 1	Selects local digital loopback. Internally loops TXD back to RXD and continues to transmit data carrrier at TXA pin.
D2	Reset	0	Selects normal operation.
		1	Resets modem to power down state. All control register bits (CR0, CR1, CR2, CR3 and Tone) are reset to zero except CR3 bit D2. The output of the clock pin will be set to the crystal frequency.
D3	CLK Control (Clock Control)	0	Selects 11.0592 MHz crystal echo output at CLK pin.
		1	Selects 16 X the data rate output at CLK pin in QAM and DPSK only.

CONTROL REGISTER 1 (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
CR1 001	TRANSMIT PATTERN 1	TRANSMIT PATTERN 0	ENABLE DETECT INT.	BYPASS SCRAMB/ ADD PH.EQ.	CLK CONTROL	RESET	TEST MODE 1	TEST MODE 0

BIT NO.	NAME	CONDITION	DESCRIPTION
D4	Bypass Scrambler/ Add Ph. Eq.	0	Selects normal operation. DPSK and QAM data is passed through scrambler.
		1	Selects Scrambler Bypass. DPSK and QAM data is routed around scrambler in the transmit path. In the V.23 mode, additional phase equalization is added to the main channel filters when D4 is set to 1.
D5	Enable Detect Interrupt	0	Disables interrupt at $\overline{\text{INT}}$ pin. All interrupts are normally disabled in power down mode.
		1	Enables $\overline{\text{INT}}$ output. An interrupt will be generated with a change in status of DR bits D1-D4 and D6. The answer tone and call progress detect interrupts are masked when the TX enable bit is set. Carrier detect is masked when TX DTMF is activated. All interrupts will be disabled if the device is in power down mode.
		D7 D6	
D7, D6	Transmit Pattern	0 0	Selects normal data transmission as controlled by the state of the TXD pin.
		0 1	Selects an alternating mark/space transmit pattern for modem testing and handshaking. Also used for S1 pattern generation. See CR2 bit D4.
		1 0	Selects a constant mark transmit pattern.
		1 1	Selects a constant space transmit pattern.

DETECT REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
DR 010	RECEIVE LEVEL INDICATOR	S1 PATTERN DETECT	RECEIVE DATA	UNSCR. MARK DETECT	CARRIER DETECT	SPECIAL TONE DETECT	CALL PROG. DETECT	SIGNAL QUALITY INDICATOR

BIT NO.	NAME	CONDITION			DESCRIPTION
D0	Signal Quality Indicator	0			Indicates normal received signal.
		1			Indicates low received signal quality (above average error rate). Interacts with Special Register SQ bits D2, D1.
D1	Call Progress Detect	0			No call progress tone detected.
		1			Indicates presence of call progress tones. The call progress detection circuitry is activated by energy in the normal 350 to 620 Hz call progress band.
D2	Special Tone Detect	0			Condition not detected
		1			Condition detected
		CR0 D0	TR D0	CR2 D5	
		1	0	1	2225 Hz ±10 Hz answer tone detected in V.22bis, V.22, V.21 modes.
		1	1	1	2100 Hz ±21 Hz answer tone detected in V.22bis, V.22, V.21 modes.
		0	0	1	1300 Hz calling tone detected in V.22 bis, V.22, V.21, V.23 modes.
		0	X	0	900 Hz SCT tone detected in V.23 mode.
		I	X	O	2100 Hz or 2225 Hz answer tone detected in QAM, DPSK, or V.21 Mode.
D3	Carrier Detect	0			No carrier detected in the receive channel.
		1			Indicated carrier has been detected in the received channel. Should be time qualified by software.
D4	Unscr. Mark Detect	0			No unscrambled mark being received.
		1			Indicates detection of unscrambled marks in the received data. Should be time qualified by software.
D5	Receive Data				Continuously outputs the received data stream. This data is the same as that output on the RXD pin, but it is not disabled when RXD is tri-stated.
D6	S1 Pattern Detect	0			No S1 pattern being received.
		1			S1 pattern detected. Should be time qualified by software. S1 is an unscrambled double dibit (11001100...) sent in DPSK 1200 bit/s mode. Generated pattern must be properly aligned to transmitter baud clock to be detected.
D7	Receive Level Indicator	0			Received signal level below threshold, (≈ -25 dBm0);can use receive gain boost (+18 dB.)
		1			Received signal above threshold.

TONE REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ WIRE FDX	DTMF 1/ OVER-SPEED	DTMF 0/ G.T./ANSW./ CALLING/SCT TONE/SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D0, D4, D5, D6	DTMF 0/ Guard Tone/ Answer Tone/ Calling/SCT Tone/ Transmit Select	D6 D5 D4 D0	D0 interacts with bits D6, D5, D4, and CR0 as shown.
		X X 1 X	Transmit DTMF tones (overides all other functions).
		1 0 0 0	Select 1800 Hz guard tone if in V.22bis or V.22 and answer mode in CR0.
		1 0 0 1	Select 550 Hz guard tone if in V.22bis or V.22 and answer mode in CR0.
		Note: Bit D0 also selects the answer tone detected in originate mode, see Detect Register Special Tone Detect (bit D2) for details.	
		1 0 0 0	1300 Hz calling tone will be transmittted if V.21, V.22, V.22bis or V.23 originate mode is selected in CR0.
		X 1 0 0	Transmit 2225 Hz Answer Tone. Must be in DPSK answer mode.
		X 1 0 1	Transmit 2100 Hz Answer Tone. Must be in DPSK answer mode.
		1 0 0 1	900 Hz SCT (soft carrier turnoff) tone transmitted in V.23 75 bit/s receive mode. (CR0 bit D0 = 1).
D1	DTMF 1/ Overspeed	D4 D1	D1 interacts with D4 as shown.
		0 0	Asynchronous QAM/DPSK +1% -2.5%. (Normal).
		0 1	Asynchronous QAM/DPSK, 2400, 1200 or 600 bit/s +2.3% -2.5%. (Extended overspeed).
D2	DTMF 2/ 4 WIRE FDX	D4 D2	
		0 0	Selects 2-wire full-duplex or half-duplex.
		0 1	D2 selects 4 wire full duplex in the modulation mode selected. The receive path corresponds to the ANS/ ORIG bit CR0 D0 in terms of high or low band selection. The transmitter is in the same band as the receiver, but does not have magnitude filtering or equalization on its signal as in the receive path.

Note: DTMF0 - DTMF2 should be set to an appropriate state after DTMF dialing to avoid unintended operation.

TONE REGISTER (Continued)

	D7	D6	D5	D4	D3	D2	D1	D0
TR 011	RXD OUTPUT CONTR.	TRANSMIT GUARD/ CALLING/SCT TONE	TRANSMIT ANSWER TONE	TRANSMIT DTMF	DTMF 3	DTMF 2/ WIRE FDX	DTMF 1/ OVER-SPEED	DTMF 0/ GUARD/ CALLING/SCT TONE SEL

BIT NO.	NAME	CONDITION	DESCRIPTION
D3, D2, D1, D0	DTMF 3, 2, 1, 0	D4 = 1	Programs 1 of 16 DTMF tone pairs that will be transmitted when TX DTMF and TX enable bit (CR0, bit D1) is set. Tone encoding is shown below:

KEYBOARD EQUIVALENT	DTMF CODE D3	D2	D1	D0	TONES LOW	HIGH
1	0	0	0	1	697	1209
2	0	0	1	0	697	1336
3	0	0	1	1	697	1477
4	0	1	0	0	770	1209
5	0	1	0	1	770	1336
6	0	1	1	0	770	1477
7	0	1	1	1	852	1209
8	1	0	0	0	852	1336
9	1	0	0	1	852	1477
0	1	0	1	0	941	1336
*	1	0	1	1	941	1209
#	1	1	0	0	941	1477
A	1	1	0	1	697	1633
B	1	1	1	0	770	1633
C	1	1	1	1	852	1633
D	0	0	0	0	941	1633

BIT NO.	NAME	CONDITION	DESCRIPTION
D7	RXD Output Control	0	Enables RXD pin. Receive data will be output on RXD.
		1	Disables RXD pin.The RXD pin reverts to a high impedance with internal weak pull-up resistor.

CONTROL REGISTER 2

	D7	D6	D5	D4	D3	D2	D1	D0
CR2 100	0	SPEC REG ACCESS	CALL INIT	TRANSMIT S1	16 WAY	$\overline{\text{RESET}}$ DSP	TRAIN INHIBIT	EQUALIZER ENABLE

BIT NO.	NAME	CONDITION	DESCRIPTION
D0	Equalizer Enable	0	The adaptive equalizer is in its initialized state.
		1	The adaptive equalizer is enabled. This bit is used in handshakes to control when the equalizer should calculate its coefficients.
D1	Train Inhibit	0	The adaptive equalizer is active.
		1	The adaptive equalizer coefficients are frozen.
D2	$\overline{\text{RESET DSP}}$	0	The DSP is inactive and all variables are initialized.
		1	The DSP is running based on the mode set by other control bits
D3	16 Way	0	The receiver and transmitter are using the same decision plane (based on the Modulator Control Mode).
		1	The receiver, independent of the transmitter, is forced into a 16 point decision plane. Used for QAM handshaking.
D4	Transmit S1	0	The transmitter when placed in alternating mark/space mode transmits 0101 .... scrambled or not dependent on the bypass scrambler bit and modulation mode.
		1	When this bit is 1 and only when the transmitter is placed in alternating mark/space mode by CR1 bits D7, D6, an unscrambled repetitive double dibit pattern of 00 and 11 at 1200 bit/s (S1) is sent.
D5	Call Init	0	The DSP is setup to do demodulation and pattern detection based on the various mode bits. Both answer tones are detected in Demod Mode concurrently; TR D0 is ignored.
		1	The DSP decodes call progress, calling tones, unscrambled mark, and 2100 Hz and 2225 Hz answer tones.
D6	Special Register Access	0	Normal CR3 access.
		1	Setting this bit and addressing CR3 allows access to the SPECIAL REGISTER. See the SPECIAL REGISTER for details.
D7	N/A	0	Must be 0 for normal operation.

CONTROL REGISTER 3

	D7	D6	D5	D4	D3	D2	D1	D0
CR3 101	TXDALT	TRISTATE TX/RXCLK	0	RECEIVE ENABLE BOOST	TRANSMIT ATTEN. 3	TRANSMIT ATTEN. 2	TRANSMIT ATTEN. 1	TRANSMIT ATTEN. 0

BIT NO.	NAME	CONDITION	DESCRIPTION
		D3 D2 D1 D0	
D3, D2, D1,D0	Transmit Attenuator	0 0 0 0 - 1 1 1 1	Sets the attenuation level of the transmitted signal in 1dB steps. The default (D3-D0=0100) is for a transmit level of -10 dBm0. The total range is 16 dB.
D4	Receive Gain Boost (18 dB)	0	18 dB receive front end boost is not used.
		1	Boost is in the path. This boost does not change reference levels. It is used to extend dynamic range by compensating for internally generated noise when receiving weak signals. The receive level detect signal and knowledge of the hybrid and transmit attenuator setting will determine when boost should be enabled.
D5	Not Used	0	Not used. Only write zeros this location.
D6	Tristate TXCLK/RXCLK	0	TXCLK, RXCLK outputs driven
		1	TXCLK, RXCLK outputs in Tristate mode
D7	TXDALT	Spec. Reg. bit D3=1	Alternate TX data source. See Special Register.

ID REGISTER

SPECIAL REGISTER

	D7	D6	D5	D4	D3	D2	D1	D0
SR 101	▨	TXBAUD CLOCK	RXUN-DSCR DATA	▨	TXD SOURCE	SIGNAL QUALITY LEVEL SELECT1	SIGNAL QUALITY LEVEL SELECT0	▨

BIT NO.	NAME	DESCRIPTION
D7, D4, D0		NOT USED AT THIS TIME. Only write ZEROs to these bits.
D6	TXBAUD CLK	TXBAUD clock is the transmit baud-synchronous clock that can be used to synchronize the input of arbitrary quad/di-bit patterns. The rising edge of TXBAUD signals the latching of a baud-worth of data internally. Synchronous data to be entered via the TXDALT bit, CR3 bit D7, should have data transitions that start 1/2 bit period delayed from the TXBAUD clock edges.
D5	RXUNDSCR DATA	This bit outputs the data received before going to the descrambler. This is useful for sending special unscrambled patterns that can be used for signaling.

SPECIAL REGISTER (Continued)

<table>
<tr><th>BIT NO.</th><th colspan="2">NAME</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>D3</td><td colspan="2">TXD SOURCE</td><td colspan="2">This bit selects the transmit data source; either the TXD pin if ZERO or the TXDALT if this bit is a ONE. The TRANSMIT PATTERN bits D7 and D6 in CR1 override either of these sources.</td></tr>
<tr><td rowspan="6">D2, D1</td><td colspan="2">SIGNAL QUALITY LEVEL SELECT</td><td colspan="2">The signal quality indicator is a logical zero when the signal received is acceptable for low error rate reception. It is determined by the value of the Mean Squared Error (MSE) calculated in the decisioning process when compared to a given threshold. This threshold can be set to four levels of error rate. The SQI bit will be low for good or average connections. As the error rate crosses the threshold setting, the SQI bit will toggle at a 1.66 ms rate. Toggling will continue until the error rate indicates that the data pump has lost convergence and a retrain is required. At that point the SQI bit will be a ONE constantly. The SQI bit and threshold selection are valid for QAM and DPSK only.</td></tr>
<tr><th>D2</th><th>D1</th><th>TYPICAL THRESHOLD VALUE</th><th>UNITS</th></tr>
<tr><td>0</td><td>0</td><td>10^{-5}</td><td>BER (default)</td></tr>
<tr><td>0</td><td>1</td><td>10^{-6}</td><td>BER</td></tr>
<tr><td>1</td><td>0</td><td>10^{-4}</td><td>BER</td></tr>
<tr><td>1</td><td>1</td><td>10^{-3}</td><td>BER</td></tr>
</table>

NOTE: This register is "mapped" and is accessed by setting CR2 bit D6 to a ONE and addressing CR3. This register provides functions to the 73K324L user that are not necessary in normal communications. Bits D7-D4 are read only, while D3-D0 are read/write. To return to normal CR3 access, CR2 bit D6 must be returned to a ZERO.

<table>
<tr><td rowspan="2">ID
110</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td>ID
3</td><td>ID
2</td><td>ID
1</td><td>ID
0</td><td colspan="4">USER DEFINABLE PERSONALITY</td></tr>
</table>

BIT NO.	NAME	CONDITION	DESCRIPTION
D7, D6, D5, D4	Device Identification Signature	D7 D6 D5 D4	Indicates Device:
		0 0 X X	SSI 73K212(L) or 73K322L or 73K321L
		0 1 X X	SSI 73K221(L) or 73K302L
		1 0 X X	SSI 73K222(L)
		1 1 0 0	SSI 73K224L
		1 1 1 0	SSI 73K324L
		1 1 0 1	SSI 73K312L

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
VDD Supply Voltage	7V
Storage Temperature	-65 to 150°C
Soldering Temperature (10 sec.)	260°C
Applied Voltage	-0.3 to VDD+0.3V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply voltage		4.5	5	5.5	V
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.22			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.22			µF
VDD Bypass capacitor 1	(VDD to GND)	0.22			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF
XTL1 Load Capacitance	Depends on crystal requirements		18	39	pF
XTL2 Load Capacitance	Depends on crystal requirements		18	27	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		-40		85	°C

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to 85°C, VDD =recommended range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
IDD, Supply Current	CLK = 11.0592 MHz				
	ISET Resistor = 2 MΩ				
IDD1, Active	Operating with crystal oscillator.		18	25	mA
IDD2, Idle	< 5 pF capacitive load on CLK pin.			5	mA
Digital Inputs					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VDD			100	µA
IIL, Input Low Current	VI = 0V	-200			µA
Reset Pull-down Current	Reset = VDD	-2	-30	-70	µA
Digital Outputs					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
RXD Tri-State Pull-up Curr.	RXD = GND	-2		-50	µA
Capacitance					
Maximum Capacitive Load					
CLK				25	pF
Input Capacitance	All Digital Inputs			10	pF

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks ATT=0100 (default)	-11.5	-10.0	-9	dBm0
FSK Modulator/Demodulator					
Output Freq. Error	CLK = 11.0592 MHz	-.31		+0.20	%
Transmit Level	ATT = 0100 (Default) Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
TXA Output Distortion	All products through BPF			-45	dB
Output Bias Distortion at RXD	Dotting Pattern measured at RXD Receive Level -20 dBm, SNR 20 dB	-10		+10	%
Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
Sum of Bias Distortion and Output Jitter at RXD	Integrated for 5 seconds	-15		+15	%
2100 Hz Answer Tone Generator					
Output Amplitude	ATT = 0100 (Default Level) Not in V.21 or V.23 Mode	-11.5	-10	-9	dBm0
Output Distortion	Distortion products in receive band			-40	dB
DTMF Generator	Not in V.21 or V.23 mode				
Freq. Accuracy		-0.03		+0.25	%
Output Amplitude	Low Band, ATT = 0100	-10		-8	dBm0
Output Amplitude	High Band, ATT = 0100	-8		-6	dBm0
Twist	High-Band to Low-Band	1.0	2.0	3.0	dB
Receiver Dynamic Range	Refer to Performance Curves	-43		-3.0	dBm0
Call Progress Detector	In Call Init mode				
Detect Level	460 Hz input signal	-34		0	dBm0
Reject Level				-40	dBm0
Delay Time	-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time	-30 dBm0 to -70 dBm0 STEP			25	ms
Hysteresis	@ 460 Hz input signal	2			dB

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
Carrier Detect Receive Gain Boost "On" for Lower Input Level Measurements						
Threshold		QAM/DPSK or FSK receive data	-48		-43	dBm0
Hysteresis		All Modes	2			dB
Delay Time	FSK	70 dBm0 to -6 dBm0	25		37	ms
		70 dBm0 to -40 dBm0	25		37	ms
	DPSK	-70 dBm0 to -6 dBm0	7		17	ms
		-70 dBm0 to -40 dBm0	7		17	ms
	QAM	-70 dBm0 to -6 dBm0	25		37	ms
		-70 dBm0 to -40 dBm0	25		37	ms
Hold Time	FSK	-6 dBm0 to -70 dBm0	25		37	ms
		-40 dBm0 to -70 dBm0	15		30	ms
	DPSK	-6 dBm0 to -70 dBm0	20		29	ms
		-40 dBm0 to -70 dBm0	14		21	ms
	QAM	-6 dBm0 to -70 dBm0	25		32	ms
		-40 dBm0 to -70 dBm0	8		28	ms
Special Tone Detectors						
Detect Level		See definitions for D0 of Tone Register	-48		-43	dBm0
Delay and Hold Time						
2225 or 2100 Hz answer tone		Call INIT mode 2225 ± 10 Hz 2100 ± 21 Hz	6		50	ms
1300 Hz calling tone		Tone Accuracy +3, -5%	10		45	ms
900 Hz SCT Receive V.23 main channel		Tone Accuracy ±9 Hz	10		45	ms
Hysteresis			2			dB
Pattern Detectors		DPSK Mode				
S1 Pattern						
Delay Time		For signals from -6 to -40 dBm0,	10		55	ms
Hold Time		Demod Mode	10		45	ms
Unscrambled Mark						
Delay Time		For signals from -6 to -40	10		45	ms
Hold Time		Demod or call Init Mode	10		45	ms
Receive Level Indicator						
Detect On			-22		-28	dBm0
Valid after Carrier Detect		DPSK Mode	1	4	7	ms

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

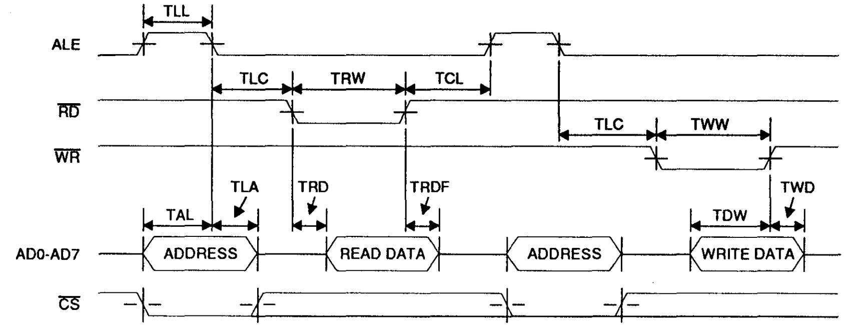
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output Load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 dB in .3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy	4 kHz, Guard Tones off			-35	dBm0
	10 kHz, Guard Tones off			-55	dBm0
	12 kHz, Guard Tones off			-65	dBm0
Anti Alias Low Pass Filter					
Maximum allowed Out-of-Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Scrambled data at 2400 bit/s in opposite band		-14		dBm
	Sinusoids out of band		-9		dBm
Transmit Attenuator					
Range of Transmit Level	Default ATT = 0100 (-10 dBm0) 1111-0000	-21		-6	dBm0
Step Accuracy		-0.15		+0.15	dB
Clock Noise	TXA pin; 153.6 kHz		1.5		mV rms
Carrier Offset					
Capture Range	Originate or Answer	-7	±5	+7	Hz
Recovered Clock					
Capture Range	% of data rate originate or answer	-.02		+.02	%
Guard Tone Generator					
Tone Accuracy	550 Hz		+1.2		%
	1800 Hz		-0.8		%
Tone Level (Below QAM/DPSK Output)	550 Hz	-4.5	-3.0	-1.5	dB
	1800 Hz	-7.5	-6.1	-4.5	dB
Harmonic Distortion (700 to 2900 Hz)	550 or 1800 Hz			-50	dB

DYNAMIC CHARACTERISTICS AND TIMING (Continued)

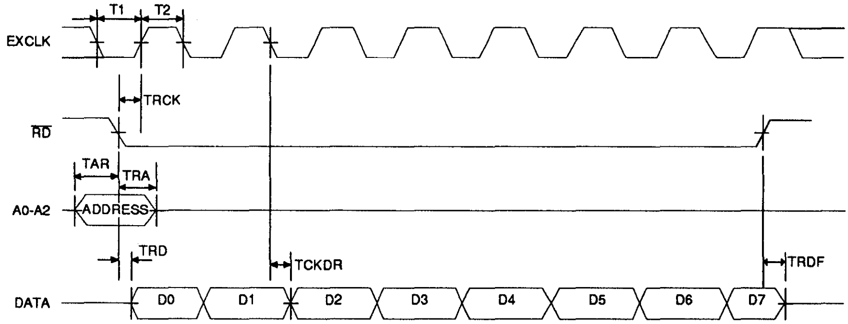
PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Timing (Refer to Timing Diagrams)					
Parallel Mode:					
TAL	$\overline{CS}$/Addr. setup before ALE Low	30			ns
TLA	$\overline{CS}$/Addr. hold after ALE Low	10			ns
TLC	ALE Low to $\overline{RD}/\overline{WR}$ Low	40			ns
TCL	$\overline{RD}/\overline{WR}$ Control to ALE High	10			ns
TRD	Data out from $\overline{RD}$ Low			90	ns
TLL	ALE width	25			ns
TRDF	Data float after $\overline{RD}$ High			40	ns
TRW	$\overline{RD}$ width	70			ns
TWW	$\overline{WR}$ width	70			ns
TDW	Data setup before $\overline{WR}$ High	70			ns
TWD	Data hold after $\overline{WR}$ High	20			ns
Serial Mode:					
TRCK	Clock high after $\overline{RD}$	250		T1	ns
TAR	Address setup before $\overline{RD}$ low	0			ns
TRA	Address hold after $\overline{RD}$ low	350			ns
TRD	$\overline{RD}$ to data valid			110	ns
TRDF	Data float after $\overline{RD}$ high			50	ns
TCKDR	Read data out after falling edge of EXCLK			300	ns
TWW	$\overline{WR}$ width	350			ns
TAW	Address setup before $\overline{WR}$	50			ns
TWA	Address hold after rising edge of $\overline{WR}$	50			ns
TCKDW	Write data hold after falling edge of EXCLK	200			ns
TCKW	$\overline{WR}$ high after falling edge of EXCLK	330		T1& T2	ns
TDCK	Data setup before falling edge of EXCLK	50			ns
T1, T2	Minimum period	500			ns
Note: T1 and T2 are the low/high periods, respectively, of EXCLK in serial mode.					

TIMING DIAGRAMS

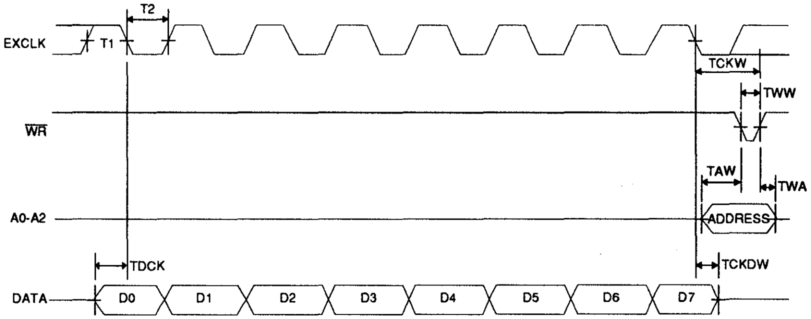
BUS TIMING DIAGRAM (PARALLEL VERSION)



READ TIMING DIAGRAM (SERIAL VERSION)



WRITE TIMING DIAGRAM (SERIAL VERSION)



APPLICATIONS INFORMATION

GENERAL CONSIDERATIONS

Figures 1 and 2 show basic circuit diagrams for K-Series modem integrated circuits. K-Series products are designed to be used in conjunction with a control processor, a UART or RS-232 serial data interface, and a DAA phone line interface to function as a typical intelligent modem. The K-Series ICs interface directly with Intel 8048 and 80C51 microprocessors for control and status monitoring purposes.Two typical DAA arrangements are shown: one for a split ±5 or ±12 volt design and one for a single 5 volt design. These diagrams are for reference only and do not represent production-ready modem designs.

K-Series devices are available with two control interface versions: one for a parallel multiplexed address/data interface, and one for a serial interface. The parallel version is intended for use with 8039/48 or 8031/51 microcontrollers from Intel or many other manufacturers. The serial interface 22-pin version can be used with other microcontrollers or in applications where only a limited number of port lines are available or the application does not lend itself to a multiplexed address/data interface. The parallel versions may also be used in the serial mode, as explained in the data sheet pin description.

In most applications the controller will monitor the serial data for commands from the DTE and the received data for break signals from the far end modem. In this way, commands to the modem are sent over the same line as the transmitted data. In other applications the RS-232 interface handshake lines are used for modem control.

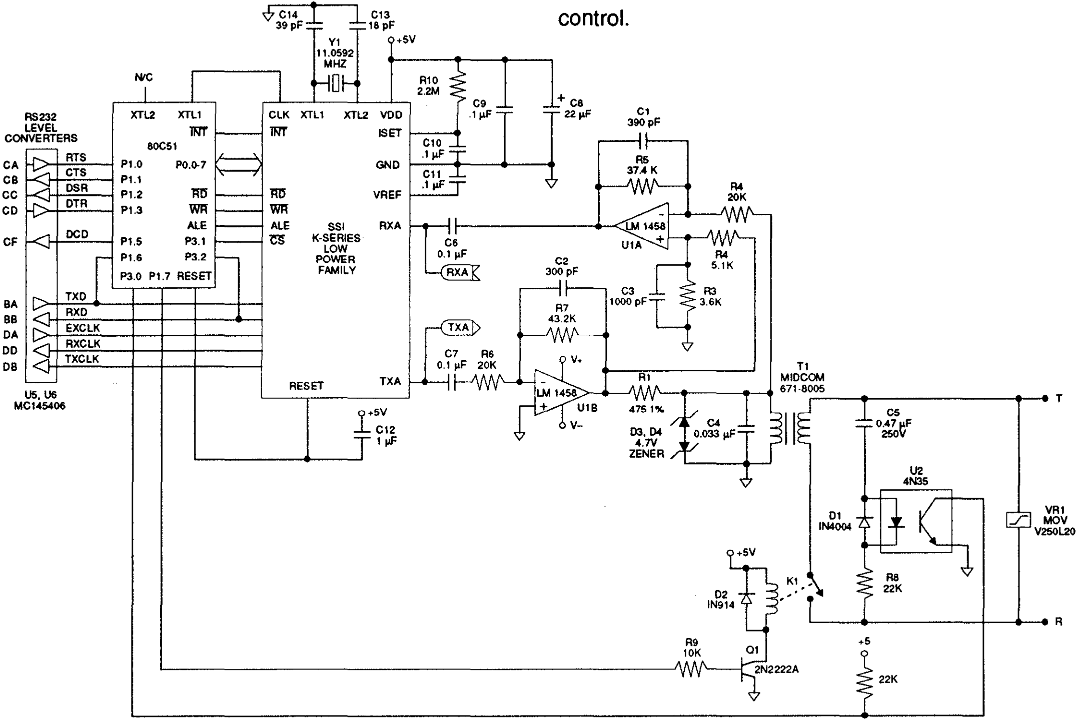


FIGURE 1: Basic Box Modem with Dual-Supply Hybrid

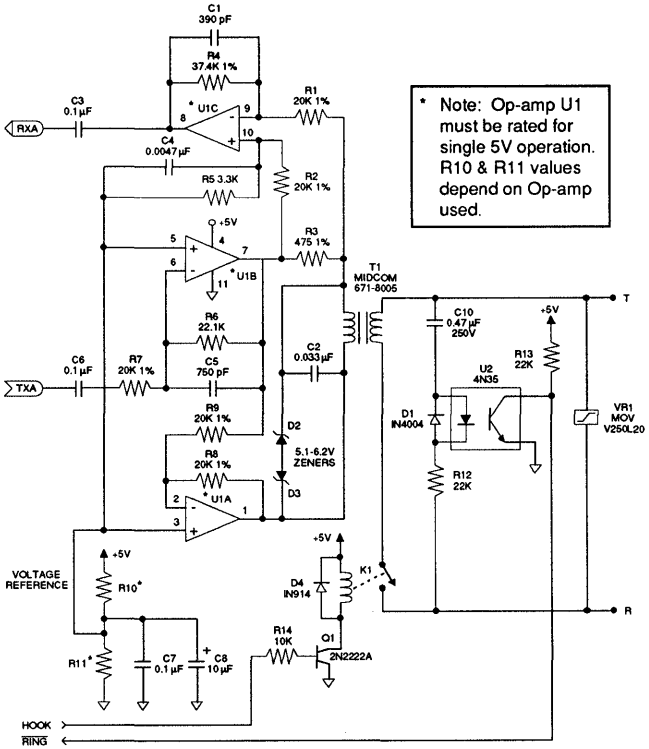
DIRECT ACCESS ARRANGEMENT (DAA)

The telephone line interfaces show two examples of how the "hybrid" may be implemented. The split supply design (Figure 1) is a typical two op-amp hybrid. The receive op-amp serves two purposes. It supplies gain to amplify the receive signal to the proper level for the modem's detectors and demodulator, and it removes the transmitted signal from the receive signal present at the transformer. This is done by supplying a portion of the transmitted signal to the non-inverting input of the receive op-amp at the same amplitude as the signal appearing at the transformer, making the transmit signal common mode.

The single-supply hybrid is more complex than the dual-supply version described above, but its use eliminates the need for a second power supply. This circuit (Figure 2) uses a bridged drive to allow undistorted signals to be sent with a single 5 volt supply. Because DTMF tones utilize a higher amplitude than data, these signals will clip if a single-ended drive approach is used. The bridged driver uses an extra op-amp (U1A) to invert the signal coming from the gain setting op-amp (U1B) before sending it to the other leg of the transformer. Each op-amp then supplies half the drive signal to the transformer. The receive amplifier (U1C) picks off its signal at the junction of the impedance matching resistor and the transformer. Because the bottom leg of the transformer is being driven in one direction by U1A and the resistor is driven in the opposite direction at the same time by U1B, the junction of the transformer and resistor remains relatively constant and the receive signal is unaffected.

DESIGN CONSIDERATIONS

Silicon Systems' 1-chip modem products include all basic modem functions. This makes these devices adaptable for use in a variety of applications, and as easy to control as conventional digital bus peripherals.



* Note: Op-amp U1 must be rated for single 5V operation. R10 & R11 values depend on Op-amp used.

FIGURE 2: Single 5V Hybrid Version

Unlike digital logic circuitry, modem designs must properly contend with precise frequency tolerances and very low level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. Following are additional recommendations which should be taken into consideration when starting new designs.

CRYSTAL OSCILLATOR

The K-Series crystal oscillator requires a parallel mode (antiresonant) crystal which operates at 11.0592 MHz. It is important that this frequency be maintained to within ±0.01% accuracy.

In order for a parallel mode crystal to operate correctly and to specification, it must have a load capacitor connected to the junction of each of the crystal and internal inverter connections, terminated to ground. The values of these capacitors depend primarily on the crystal's characteristics, and to a lesser degree on the internal inverter circuit. The values used affect the accuracy and start up characteristics of the oscillator.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain highest performance in modem designs. The more digital circuitry present on the PC board, the more this attention to noise control is needed. The modem should be treated as a high impedance analog device. A 22 µF electrolytic capacitor in parallel with a 0.22 µF ceramic capacitor between VDD and GND is recommended. Liberal use of ground planes and larger traces on power and ground are also highly favored. High speed digital circuits tend to generate a significant amount of EMI (Electro-Magnetic Interference) which must be minimized in order to meet regulatory agency limitations. To accomplish this, high speed digital devices should be locally bypassed, and the telephone line interface and K-Series device should be located close to each other near the area of the board where the phone line connection is accessed. To avoid problems, power supply and ground traces should be routed separately to the analog and digital functions on the board, and digital signals should not be routed near low level or high impedance analog traces. The analog and digital grounds should only connect at one point near the K-Series device ground pin to avoid ground loops. The K–Series modem IC's should have both high frequency and low frequency bypassing as close to the package as possible. The ISET resistor and bypass capacitor need to be as close to device as possible.

MODEM PERFORMANCE CHARACTERISTICS

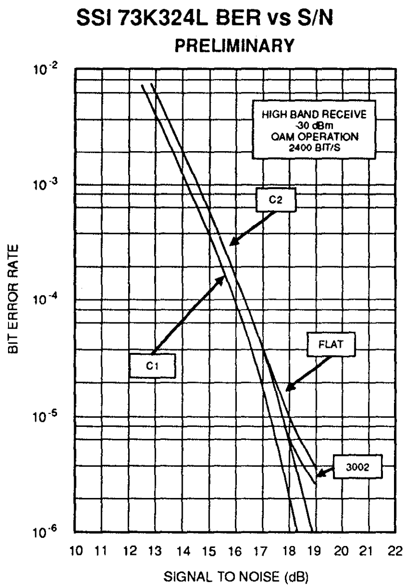
The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Hayes 2400 Smartmodem™ as the reference modem. A 511 pseudo-random-bit pattern was used for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power measurements similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

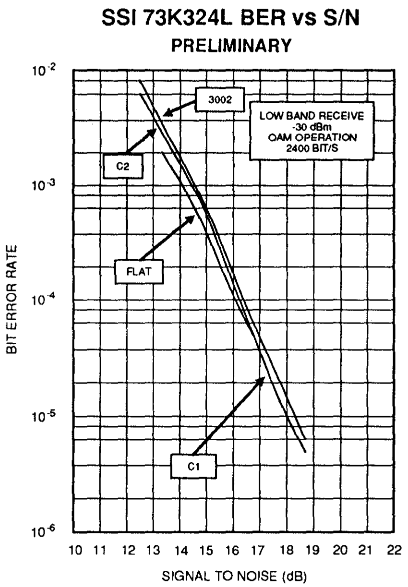
BER vs. S/N

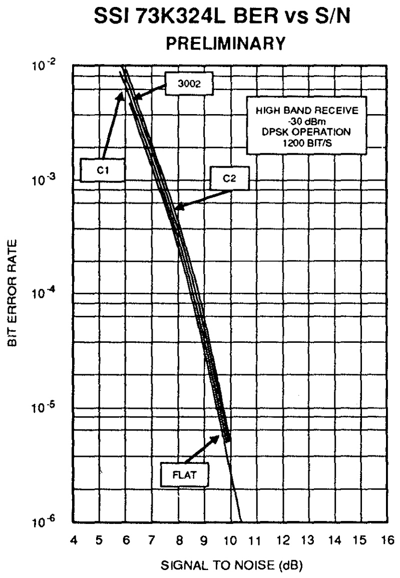
This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically, a modem will exhibit better BER-performance test curves receiving in the low band than in the high band.

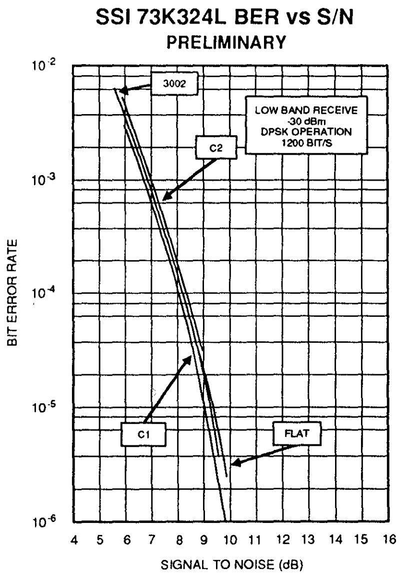
BER vs. Receive Level

This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.


SSI 73K324L BER vs S/N
PRELIMINARY
HIGH BAND RECEIVE
-30 dBm
QAM OPERATION
2400 BIT/S
C2
C1
FLAT
3002
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10 11 12 13 14 15 16 17 18 19 20 21 22
SIGNAL TO NOISE (dB)


SSI 73K324L BER vs S/N
PRELIMINARY
3002
LOW BAND RECEIVE
-30 dBm
QAM OPERATION
2400 BIT/S
C2
FLAT
C1
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10 11 12 13 14 15 16 17 18 19 20 21 22
SIGNAL TO NOISE (dB)


SSI 73K324L BER vs S/N
PRELIMINARY
3002
HIGH BAND RECEIVE
-30 dBm
DPSK OPERATION
1200 BIT/S
C1
C2
FLAT
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
4 5 6 7 8 9 10 11 12 13 14 15 16
SIGNAL TO NOISE (dB)


SSI 73K324L BER vs S/N
PRELIMINARY
3002
LOW BAND RECEIVE
-30 dBm
DPSK OPERATION
1200 BIT/S
C2
C1
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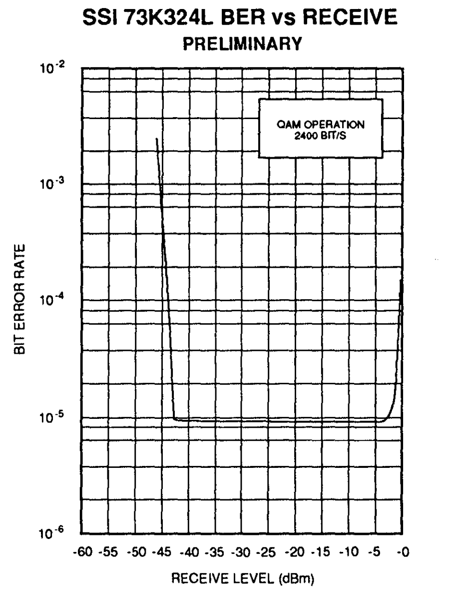
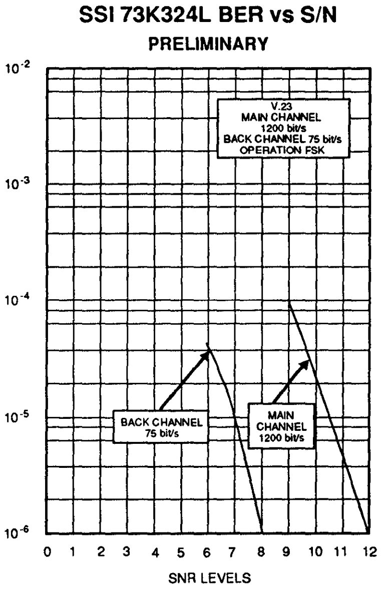
BIT ERROR RATE
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
4 5 6 7 8 9 10 11 12 13 14 15 16
SIGNAL TO NOISE (dB)



SSI 73K324L BER vs RECEIVE

PRELIMINARY



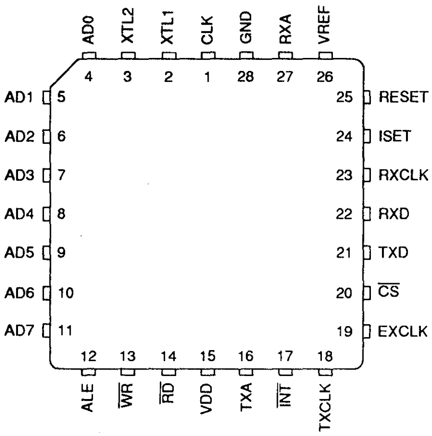
SSI 73K324L BER vs S/N

PRELIMINARY

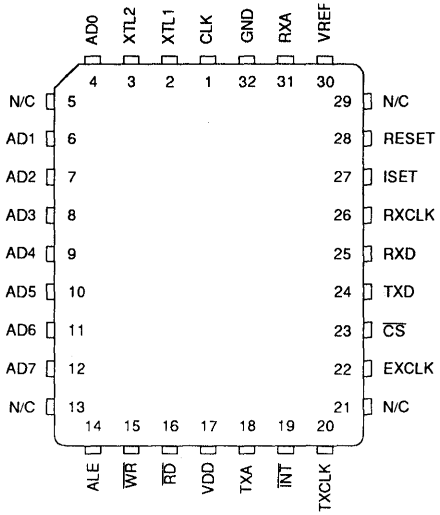
SSI 73K324L
CCITT V.22bis, V.22, V.21, V.23, Bell 212A Single-Chip Modem

PACKAGE PIN DESIGNATIONS

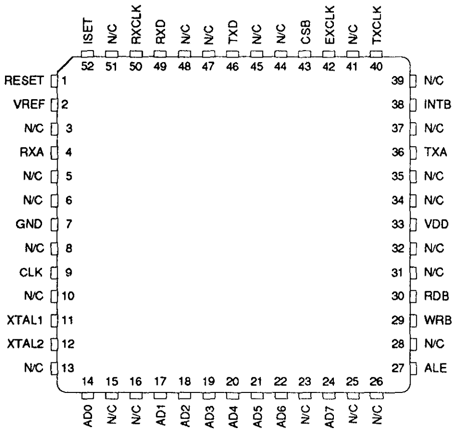
(Top View)



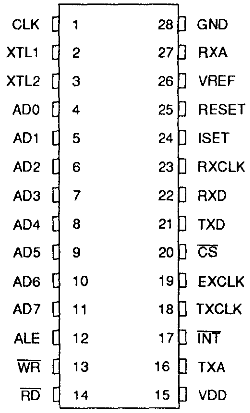
28-Pin PLCC



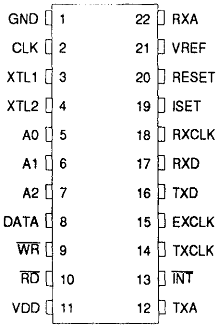
32-Pin PLCC



52-Lead QFP

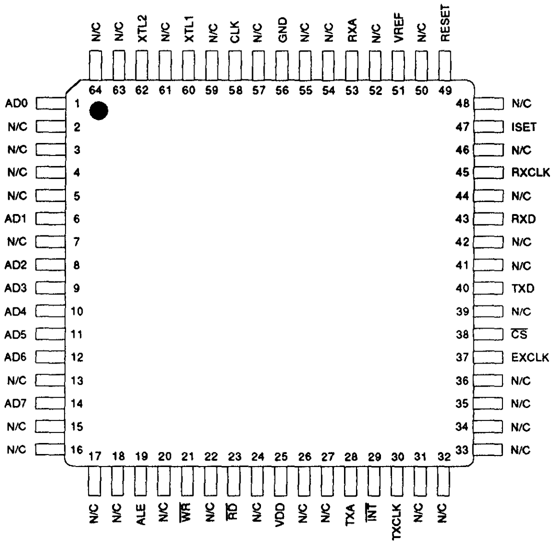


28-Pin DIP



400-Mil
22-Pin DIP

SSI 73K324L
CCITT V.22bis, V.22, V.21, V.23, Bell 212A
Single-Chip Modem



64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73K324L with Serial Bus Interface		
22-Pin Plastic Dual-In-Line	73K324LS-IP	73K324LS-IP
SSI 73K324L with Parallell Bus Interface		
28-Pin Plastic Dual-In-Line	73K324L-IP	73K324L-IP
28-Pin Plastic Leaded Chip Carrier	73K324L-28IH	73K324L-28IH
32-Pin Plastic Leaded Chip Carrier	73K324L-32IH	73K324L-32IH
44-Pin Plastic Leaded Chip Carrier	73K324L-IH	73K324L-IH
52-Pin Quad Flat Pack Package	73K324L-IG	73K324L-IG
64-Lead Thin Quad Flat Pack Package	73K324L-IGT	73K324L-IGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

Protected by the following patents: (4,777,453)
(4,789,995) (4,870,370) (4,847,868) (4,866,739)

Notes:

Section 2

MODEM PROTOCOL & BUS INTERFACE

silicon systems®
A TDK Group Company

SSI 73D2240
V.22bis 2400 Bit/s Modem Device Set

December 1992

DESCRIPTION

The SSI 73D2240 is a set of two ICs that provide the data pump functions needed to design a high-performance, low-power 2400 bit/s intelligent modem for use in dial-up telephone network applications. The SSI 73D2240 consists of the SSI 73K224L 1-chip multi-mode modem along with the SSI 73D600, a companion supervisory controller that provides a complete "AT" command and feature set compatible with industry standard products.

The SSI 73D2240 includes operating modes compatible with CCITT V.22bis, V.22, and V.21, as well as Bell 212A and 103 data communications standards. Using advanced CMOS processes that integrate analog, digital signal processing and switched capacitor filter functions on the same chip, the SSI 73D2240 offers excellent performance, full modem features and the lowest power consumption available in a compact 2-chip set.

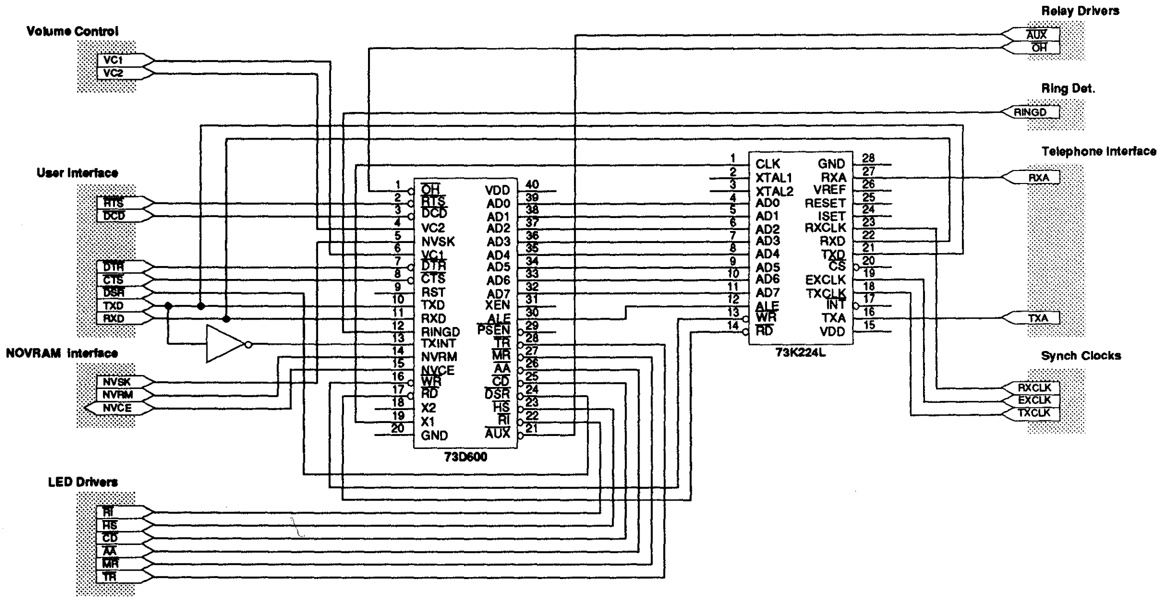
(continued)

FEATURES

- **Multi-mode V.22bis/V.22/V.21 & Bell 212A/103 compatible device set for intelligent modem designs**
- **Full duplex operation at 0-300, 1200 and 2400 bit/s with all synch & asynch operating modes**
- **Includes high-level "AT" command interpreter compatible with 2400 bit/s industry standard products**
- **SSI 73K600 Controller Compatible with other K-series products**
- **Complete complement of "AT" modem features**
- **Selectable automatic speed detect, handshake and autobaud functions**
- **Supports external non-volatile memory to store user configurations**
- **Adaptive equalization for optimum performance over all lines**
- **Dynamic range from -3 to -45 dBm**

(continued)

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

The SSI 73D2240 can be used in free-standing and integral modem designs where full-duplex 2400 bit/s operation is required. Single 5V supply operation with extremely low power draw make it ideal for battery powered terminals, lap-top PCs and other power sensitive applications.

FEATURES (continued)

- **Call progress, carrier and answer tone detectors provide intelligent dialing functions**
- **DTMF and CCITT guard tone generators**
- **Test modes available - ALB, DL, RDL for complete test capability**
- **All CMOS technology for low power consumption (< 600mW using ±5V)**

OPERATION

The SSI 73D2240 is a complete V.22bis intelligent modem contained in two CMOS ICs. The device set forms the basis for a high performance stand-alone modem product with self-contained command interpreter, indicator LEDs, and interface lines for an RS-232 serial port. Both data and commands are passed over the serial port as in conventional intelligent modem designs.

The SSI 73D2240 provides the QAM, PSK and FSK modulator/demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guard tones. This device supports the V.22bis, V.22, V.21 and Bell 212A/103 operating modes, both synchronous and asynchronous. The SSI 73D2240 is designed to provide functions needed for an intelligent modem and includes auto-dial/auto-answer, handshake with auto-fallback, and selectable pulse or DTMF dialing sequences to simplify these designs.

The SSI 73D2240 consists of two devices. The SSI 73K224L is an analog processor and DSP that perform the filtering, timing adjustment, level detection and modulation/demodulation functions. The SSI 73D600 is a command processor that provides supervisory control and command interpretation. The SSI 73D600 is also compatible with the SSI 73K212, 221 and 222 K–series modem ICs.

QAM MODULATOR/DEMODULATOR

The SSI 73D2240 scrambles and encodes the 2400 bit/s incoming data into quad bits represented by 16 possible signal points as specified by CCITT recommendation V.22 bis. The modulator transmits this encoded data using either a 1200 Hz (originate mode) or 2400 Hz (answer mode) carrier. The demodulator reverses this procedure and recovers a data clock from the incoming signal. Adaptive equalization corrects for different line conditions by automatically changing filter parameters to compensate for line characteristics.

DPSK MODULATOR/DEMODULATOR

In DPSK mode the SSI 73D2240 modulates the 1200 bit/s incoming data using a subset of the QAM signal points as specified by CCITT recommendation V.22bis, V.22 and Bell 212A. The DPSK demodulator is similar to the QAM demodulator.

FSK MODULATOR/DEMODULATOR

The FSK transmitter frequency modulates the analog output signal using two discrete frequencies to represent the binary data. The Bell 103 standard frequencies of 1270 and 1070 Hz (originate mark and space) and 2225 and 2025 Hz (answer mark and space) or the V.21 standard frequencies of 980 and 1180 Hz (originate mark and space) and 1650 and 1850 Hz (answer mark and space) are used when this mode is selected. Demodulation involves detecting the received frequencies and decoding them into the appropriate binary value.

PASSBAND FILTERS AND EQUALIZERS

A bandsplit filter is included to shape the amplitude and phase response of the transmit signal to a square root 75% raised cosine and provide rejection of out-of-band signals in the receive channel.

ASYNCHRONOUS MODES

The character asynchronous modes are used for communication between asynchronous terminals which may vary the data rate from +1.5% to -2.3%. When transmitting in this mode the serial data on the TXD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output the data within 0.01%. The signal is routed to a data scrambler (following the CCITT V.22bis algorithm) and into the modulator. The 73D2240 recognizes a break signal and handles it in accordance with specifications. Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits. An incoming break signal will be passed through without incorrectly inserting a stop bit.

SYNCHRONOUS MODES

Synchronous operation is possible only with the QAM or DPSK modes. Operation is similar to that of the asynchronous mode except that data must be synchronized to a provided clock and no variation in data transfer rate is allowable. External synchronous mode is provided for a user supplied clock accurate to ±0.01%. Serial input data appearing at TXD must be valid on the rising edge of TXCLK. Receive data at the RXD output is clocked out on the rising edge of RXCLK. The async/synch converter is bypassed when synchronous mode is selected and data is transmitted out at the same rate as is input. The RXCLK, TXCLK and EXCLK are for synchronous modes only.

AUTOMATIC HANDSHAKE

The SSI 73D2240 will automatically perform a complete handshake as defined by the V.22bis, V.22 and Bell 212A/103 standards to connect with a remote modem. The SSI 73D2240 automatically determines the speed and operating mode and adjusts its operation to correspond to that of an answering modem when originating a call.

TEST MODES

The SSI 73D2240 allows use of Analog Loopback, Digital Loopback and Remote Digital Loopback test modes. Full test mode capability allows testing of the modem and interface functions from the local terminal using the appropriate control commands, or remotely using the RDL function.

ADAPTIVE EQUALIZATION WITH AUTO-RETRAIN

The SSI 73D2240 uses adaptive equalization which automatically compensates for varying line characteristics by adjusting taps on a multi-tap FIR filter. Optimum performance is obtained with this technique over a wide range of line conditions. When the line quality deteriorates to a specified level the SSI 73D2240 can automatically initiate a retrain of the equalizer to re-establish data communications without the need to go through a complete handshake sequence.

"AT" COMMAND INTERPRETER

The SSI 73D2240 includes an AT command interpreter which is compatible with the Hayes 2400 Smartmodem™ command set. Functions and features included with intelligent modems are provided by the SSI 73D2240 command interpreter. The SSI 73D600 controller may also be used with the SSI 73K212, K221, and K222. It will function with these parts in the modes supported by the device. It will still support the Hayes Smartmodem™ 2400 commands even though operation at 2400 bit/s will not be permitted. The controller reads the device signature of the modem IC installed to determine which modes should be allowed.

NON-VOLATILE MEMORY

The SSI 73D2240 supports connection to an external non-volatile memory (National 9346 or equivalent) to store dial strings and the current AT command configuration. If NOVRAM is not present, the factory default configuration is automatically used, but dial string storage is not permitted.

SPEED/PROTOCOL COMPATIBILITY GUIDE

			73D2240 originating as:				
			Bell		CCITT		
Calling a:			300	1200	300	1200	2400
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400[1]	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22bis)	300	1200	-	1200	2400

			73D2240 answering as:				
			Bell		CCITT		
Called from a:			300	1200	300	1200	2400
Bell	300	(103)	300	300	-	-	300
	1200	(212)	300	1200	-	1200	1200
	2400	(224)	300	1200	-	1200	2400
CCITT	300	(V.21)	-	-	300	-	-
	1200	(V.22)	300	1200	-	1200	1200
	2400	(V.22bis)	300	1200	-	1200	2400

[1] A Bell 2400 is a V.22bis using a 2225 Hz answer tone without unscrambled marks.

"AT" COMMANDS SUPPORTED
(Note: s=string; n=decimal, 0-255; x=Boolean, 0/1=false/true)

COMMAND	OPTIONS	DEFAULT
A/	Repeats last command line	N/A
A	Answer	N/A
Bx	BELL/CCITT = 1/0 answer tone @1200 (N/A @2400)	1
DS = n	Dial string specified by n, n = 0-3	n = 0
Ex	Command echo, 0/1 = off/on	1
Hn	Hook status, 0/1 = on/off	N/A
In	ID code, 0/1/2 (see Table 8)	N/A
Ln	Speaker volume, (0)1/2/3 = lo/med/hi	2
Mn	Speaker, 0/1/2/3 = control (see Table 3)	1
On	Online, 0/1/2/3 = online/retrain/no retrain (see Table 4)	N/A
P	Pulse dial	Pulse
Qx	Quiet result, 0/1 = 1-quiet	0
R	Reverse originate	N/A
Sn=n	Set S register (see Table 2)	N/A
Sn?	Return value in register n (see Table 2)	N/A
T	Touch tone dial	Pulse
Vx	Verbose result, 0/1 = off/on	1
Xn	Result code, 0/1/2/3/4 (see Table 1)	4
Yx	Enable long space disconnect, 1 = enable	0
Zx	Restore from Non-Volatile Memory, x = 0 or 1	N/A
&Cx	Carrier detect override, 0/1 = on/normal	0
&Dn	DTR mode, 0/1/2/3 (see Table 5)	0
&F	Restore to factory configuration	N/A
&Gn	CCITT guard tone, 0/1/2 = off/1800/550	0
&Jx	Auxiliary relay control	0
&Mn	Async/Sync mode, 0/1/2/3 (see Table 6)	0

"AT" COMMANDS SUPPORTED (continued)

COMMAND	OPTIONS	DEFAULT
&Px	Pulse dial mode, 0/1=U.S./U.K.	0
&Qx	Same as &M	N/A
&Rx	Enable RTS/CTS	0
&Sx	DSR override, 0/1=U.S./U.K.	0
&Tn	Test mode (see Table 7)	N/A
&V	View active configuration and user profiles	N/A
&Wx	Write current configuration to NVRAM x = 0 or 1	0
&Xn	Sync Tx clock mode, 0/1/2=int/ext/slave	0
&Yx	Designate default user profile Z0 or Z1	N/A
&Zn = s	Store a telephone number n = 0-3	N/A

Factory configuration[1]:
B1 E1 F1 L2 M1 P Q0 V1 X4 Y0 &C0 &D0 &G0 &J0 &M0 &P0 &R0 &S0 &T4 &X0

Dial string arguments:

, = delay	@ = silent answer	! = flash	
; = return to command	s = dial stored number	W = wait for tone	R=reverse mode

TABLE 1: Result Codes

Xn	VOCAL/NUMERIC RESULT CODE
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6

TABLE 2: S Registers Supported

Sn	FUNCTION	UNITS	DEFAULT
S0[2]	Answer on ring	No. of rings	000
S1	Ring counter	No. of rings up to 8	000
S2	Escape code	ASCII CHR$( )	043
S3	Carriage return	ASCII CHR$( )	013

[1] If the NOVRAM has not been initialized it may be necessary to Power down/Power up and type AT&F&W<cr> to properly initialize modem state.

[2] Stored in NVRAM with &W command

TABLE 2: S Registers Supported (continued)

NUMBER	FUNCTION	UNITS	DEFAULT
S4	Line feed	ASCII CHR$( )	010
S5	Back space	ASCII CHR$( )	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds	006
S10	Carrier drop out	100 milliseconds	014
S11	DTMF tone duration	1 millisecond	070
S12	Escape guard time	20 milliseconds	050
S13	Unused		N/A
*S14[2]	Bit mapped register	Decimal 0-255	170
S15	Unused		N/A
S16	Test register	Decimal #	000
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[2]	Bit mapped register	Decimal 0-255	000
*S22[2]	Bit mapped register	Decimal 0-255	118
*S23[2]	Bit mapped register	Decimal 0-255	007
S24	Unused		N/A
S25[2]	DTR delay	10 milliseconds	005
S26[2]	CTS delay	10 milliseconds	001
*S27[2]	Bit mapped register	Decimal 0-255	064

* The bit mapped register functions are equivalent to normal "AT" command modem registers. They are not needed for evaluation of the 73D2240 capabilities.

Asynchronous character formats supported:
[Number of data bits, parity (even/odd/none), number of stop bits]

1200/2400 bit/s: 7N2, 7E1, 7O1, 8N1

300 bit/s: 7N2, 7E1, 7O1, 8N1

[2] Stored in NVRAM with &W command

TABLE 3: Speaker Modes

Mn	SPEAKER MODE
M0	Speaker off
M1	Speaker on during connect only
M2	Speaker on always
M3	Speaker on during call progress

TABLE 4: O Modes

On	ONLINE/RETRAIN MODE
O0	Return online
O1	Return online with retrain
O2	Enable automatic retrain (default)
O3	Disable automatic retrain

TABLE 5: DTR Modes

&Dn	DTR MODE
&D0	Ignore DTR
&D1	Go to command state if ON to OFF detected
&D2	Go to command state and disable auto-answer if ON to OFF detected
&D3	Initialize modem with NVRAM if ON to OFF detected

TABLE 6: Synchronous Modes

&Mn	SYNCHRONOUS MODE
&M0	Asynchronous
&M1	Sync mode entered upon completion of connect sequence
&M2	Dial stored number on OFF to ON transition of DTR and go online
&M3	Manual dial using DTR as talk data switch

TABLE 7: Test Modes

&Tn	TEST MODE
&T0	End/Abort test
&T1	Initiate local analog loopback (L3)
&T3	Initiate local digital loopback
&T4	Permit remote digital loopback (L2)
&T5	Prohibit remote digital loopback
&T6	Initiate remote digital loopback (L2)
&T7	Initiate RDL with self-test and error detector
&T8	Initiate ALB with self-test and error detector

TABLE 8: ID Codes

In	CODE
I 0	Product code (249)
I 1	ROM checksum
I 2	Checksum test
I 3	Product revision
I 4	Software copyright

HARDWARE INTERFACE

POWER SUPPLIES AND CLOCKS

LABEL	I/O	PIN CONNECTION		DESCRIPTION
		73K224L	73D600	
VDD	I	15	40	Positive supply (+5V)
GND	I	28		System ground
GND	I	28		Digital ground
X1	I		19	Clock input 11.0592 MHz
CLK	O	1		Clock output 11.0592 MHz
RST	I	25	9	Reset (10 µF & 8.2k)

DAA INTERFACE

RxA	I	27		Receive analog from DAA
TxA	O	16		Transmit analog to DAA
VC1	O		6	Audio volume control
VC2	O		4	Audio volume control
RINGD	I		12	From ring indicator
$\overline{\text{OH}}$	O		1	Off hook relay control
$\overline{\text{AUX}}$	O		21	Auxiliary relay control

RS-232/V.24 INTERFACE

$\overline{\text{RI}}$	O		22	Ring indicator output
$\overline{\text{HS}}$	O		23	Indicates high speed
TXD	I	21	10	Digital data from terminal
RXD	O	22	11	Digital receive data
$\overline{\text{DCD}}$	O		3	Data carrier detect
$\overline{\text{DSR}}$	O		24	Data set ready
EXCLK	I	19		External Tx sync clock input
RXCLK	O	23		Receive clock ouptut
TXCLK	O	18		Transmit clock output
$\overline{\text{CTS}}$	O		8	Clear to send
$\overline{\text{RTS}}$	I		2	Request to send
$\overline{\text{DTR}}$	I		7	Indicates DTE available

HARDWARE INTERFACE (continued)

LED DISPLAY SIGNAL SOURCE

		PIN CONNECTION	
LABEL	I/O	73D600	DESCRIPTION
TR	LED	28	Data terminal ready (Active Low)
SD	LED	11	Transmit data (Mark = High)
RD	LED	10	Receive data (Mark = High)
CD	LED	25	Data carrier detect (Active Low)
HS	LED	23	High speed indicator (Active Low)
MR	LED	27	Modem ready/test in progress (Active Low)
AA	LED	26	Auto answer indicator (Active Low)
OH	LED	1	Off hook indicator (Active Low)

NVRAM INTERFACE 73D600

NVCE	O	15	NVCE
NVRM	I/O	14	NVRM
NVSK	O	5	NVSK

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
VDD Supply Voltage	73K224L	7	V
	73D600	7	V
Storage Temperature		-65 to 150	°C
Soldering Temperature (10 sec.)		260	°C
Applied Voltage		-0.3 to VDD+0.3	V
Note: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.			

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Components (Refer to Application section for placement.)					
VREF Bypass capacitor	(VREF to GND)	0.1			µF
Bias setting resistor	(Placed between VDD and ISET pins)	1.8	2	2.2	MΩ
ISET Bypass capacitor	(ISET pin to GND)	0.1			µF
VDD Bypass capacitor 1	(VDD to GND)	0.1			µF
VDD Bypass capacitor 2	(VDD to GND)	22			µF

RECOMMENDED OPERATING CONDITIONS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
External Components - 73D600					
VDD Bypass Capacitor	VDD to GND	1			µF
XTL1, 2 Load Capacitors	Typical, depends on crystal	15		40	pF
Clock Variation	(11.0592 MHz) Crystal or external clock	-0.01		+0.01	%
TA, Operating Free-Air Temperature		0		55	°C

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

VDD Supply Voltage					
73D600, 73K224L		4.75	5	5.5	V
IDD, Supply Current	**CLK = 11.0592 MHz**				
73K224L	ISET Resistor = 2 MΩ				
IDD1, Active			25	30	mA
IDD2, Idle	CLK = 11.0592 MHz		3	5	mA
73D600					
IDD1, Active				16	mA
IDD2, Idle				3.7	mA
Digital Inputs 73K224L					
VIL, Input Low Voltage				0.8	V
VIH, Input High Voltage					
All Inputs except Reset XTL1, XTL2		2.0		VDD	V
Reset, XTL1, XTL2		3.0		VDD	V
IIH, Input High Current	VI = VIH MAX			100	µA
IIL, Input Low Current	VI = VIL MIN	-200			µA
Reset Pull-down Current	Reset = VDD	5		50	µA
Digital Outputs 73K224L					
VOH, Output High Voltage	IO = IOH Min IOUT = -0.4 mA	2.4		VDD	V
VOL, Output Low Voltage	IO = IOUT = 1.6 mA			0.4	V
VOL, CLK Output	IOUT = 3.6 mA			0.6	V
RXD Tri-State Pull-up Curr.	RXD = GND	-5		-50	µA
Capacitance 73K224L					
Inputs	Input capacitance, all Digital Input pins			10	pF
CLK	Maximum Capacitive Load			15	pF

DC ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Digital Inputs 73D600					
VIL, Input Low Voltage		0		.2VDD-.1	V
VIH, Input High Voltage					
Reset, X1		.7 VDD		VDD	V
All Other Pins		.2 VDD +.9		VDD	V
IIL, Low Input Current	Vin = 0.45 V			-50	µA
ITL, Logic 1 to 0 Transition Current	Vin = 2.0V			-500	µA
Digital Outputs 73D600					
VOH Output High Voltage					
All Ports Except ALE, AD0-7	IOH = -80 µA	2.4			V
AD0-7, ALE	IOH = -400 µA	2.4			
VOL Output Low Voltage					
All Ports Except ALE, AD0-7	IOL = 1.6 mA			0.45	V
AD0-7, ALE	IOL = 3.2 mA			0.45	V
Reset Pull Down Resistor		40		125	kΩ

DYNAMIC CHARACTERISTICS AND TIMING

(TA = -40°C to +85°C, VDD = recommended range unless otherwise noted.)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
QAM/DPSK Modulator					
Carrier Suppression	Measured at TXA	35			dB
Output Amplitude	TX scrambled marks	-11.5	-10.0	-9	dBm0
FSK Modulator					
Output Freq. Error	CLK = 11.0592 MHz	-0.31		+.20	%
Transmit Level	Transmit Dotting Pattern	-11.5	-10.0	-9	dBm0
Output Distortion	All products through BPF			-45	dB
Sum of Output Bias Distortion and Output Jitter	Transmit Dotting Pattern in ALB @ RXD Bell 103 Originate	-20		+20	%
2100 Hz Answer Tone Generator					
Output Amplitude		-11.5	-10	-9	dBm0
Output Distortion	All products though BPF			-40	dB

NOTE: Parameters expressed in dBm0 refer to the following definition:

0 dB loss in the Transmit path to the line.

2 dB gain in the Receive path from the line.

Refer to the Basic Box Modem diagram in the Applications section for the DAA design.

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNITS
DTMF Generator						
Freq. Accuracy			0.03		+0.25	%
Output Amplitude			-10		-8	dBm0
Output Amplitude			-8		-6	dBm0
Twist		High-Band to Low-Band	1.0	2.0	3.0	dB
Receiver Dynamic Range		Refer to Performance Curves	-43		-3	dBm0
Call Progress Detector		In Call Init mode				
Detect Level		460 Hz test signal	-34		0	dBm0
Reject Level					-50	dBm0
Delay Time		-70 dBm0 to -30 dBm0 STEP			25	ms
Hold Time		-30 dBm0 to -70 dBm0 STEP			25	ms
Hysteresis			2			dB
Carrier Detect						
Threshold		FSK receive data	-51		-40	dBm0
Threshold		QAM/DPSK receive data	-49		-43	dBm0
Hysteresis		All Modes	2			dB
Delay Time	DPSK	-70 dBm0 to -6 dBm0	15	20	25	ms
		-70 dBm0 to -40 dBm0	15	20	25	ms
	QAM	-70 dBm0 to -60 dBm0	25	30	35	ms
		-70 dBm0 to -40 dBm0	25	33	41	ms
Hold Time	DPSK	-6 dBm0 to -70 dBm0	15	22	28	ms
		-40 dBm0 to -70 dBm0	10	15	20	ms
	QAM	-6 dBm0 to -70 dBm0	44	60	66	ms
		-40 dBm0 to -70 dBm0	21	26	31	ms
Answer Tone Detectors		Call Init Mode				
Detect Level			-56		-45	dBm0
Detect Time		For signals from -6 to -40 dBm0, 2100 or 2225 Hz	7		40	ms
Hold Time			10		50	ms
Detect Time		Demod Mode for signals from -6 to -40 dBm0, 2100 or 2225 Hz	4		26	ms
Hold Time			11		43	ms

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Pattern Detectors	DPSK Mode				
S1 Pattern					
Delay Time	For signals from -6 to -40 dBm0,	5		65	ms
Hold Time	Demod Mode	4		45	ms
Unscrambled Mark					
Delay Time	For signals from -6 to -40 dBm0,	5		45	ms
Hold Time	Demod or call Init Mode	5		45	ms
Receive Level Indicator					
Detect On				-21	dBm0
Valid after Carrier Detect		10			ms
Output Smoothing Filter					
Output Impedance	TXA pin		200	300	Ω
Output load	TXA pin; FSK Single	10			kΩ
	Tone out for THD = -50 dB in 0.3 to 3.4 kHz range			50	pF
Maximum Transmitted Energy	4 kHz, Guard Tones off			-35	dBm0
	10 kHz, Guard Tones off			-55	dBm0
	12 kHz, Guard Tones off			-65	dBm0
Anti Alias Low Pass Filter	(Frequency kHz)				
Out of Band Signal Energy (Defines Hybrid Trans-Hybrid loss requirements)	Level at RXA pin with receive Boost Enabled				
	Scrambled data at 2400 bit/s in opposite band			-14	dBm
	Sinusoids out of band			-9	dBm
Clock Noise	TXA pin; 153.6 kHz				
73K224L				1.5	mVrms
Carrier Offset					
Capture Range	Originate or Answer		±7	±10	Hz

DYNAMIC CHARACTERISTICS AND TIMING (continued)

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNITS
Recovered Clock					
Capture Range	% of frequency originate or answer	-.02		+.02	%
Guard Tone Generator					
Tone Accuracy	550 Hz			+1.18	%
	1800 Hz	-0.7			
Tone Level (Below QAM/DPSK Output)	550 Hz	-5.0	-3.0	-2.0	dB
	1800 Hz	-8.0	-6.0	-5.0	dB
Harmonic Distortion (700 to 2900 Hz)	550 Hz			-60	dB
	1800 Hz			-60	dB
Timing (Refer to Timing Diagrams)					
TAL	$\overline{\text{CS}}$/Addr. setup before ALE	30			ns
TLA	$\overline{\text{CS}}$/Addr. Hold after latch	20			ns
TLC	Latch to $\overline{\text{RD}}$/$\overline{\text{WR}}$ control	40			ns
TCL	$\overline{\text{RD}}$/$\overline{\text{WR}}$ Control to Latch	0			ns
TRD	Data out from $\overline{\text{RD}}$	0		160	ns
TLL	ALE width	50			ns
TRDF	Data float after READ	0		5	ns
TRW	READ width	171		25000	ns
TWW	WRITE width	140		25000	ns
TDW	Data setup before WRITE	150			ns
TWD	Data hold after WRITE	20			ns

1: Control for setup is the falling edge of $\overline{\text{RD}}$ or $\overline{\text{WR}}$.
Control for hold is the falling edge of $\overline{\text{RD}}$ or the rising edge of $\overline{\text{WR}}$.

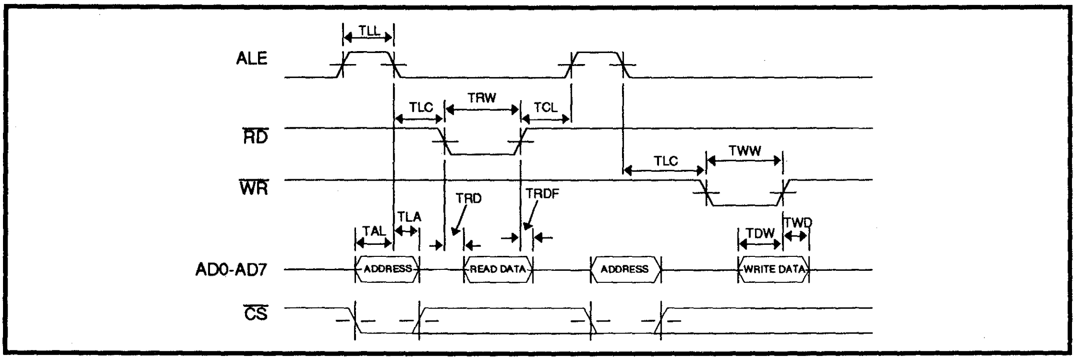


FIGURE 1: Bus Timing Diagram (Parallel Version)

PERFORMANCE DATA

(This performance data was taken using an AEA tester and the 73D2402 MEU board.)

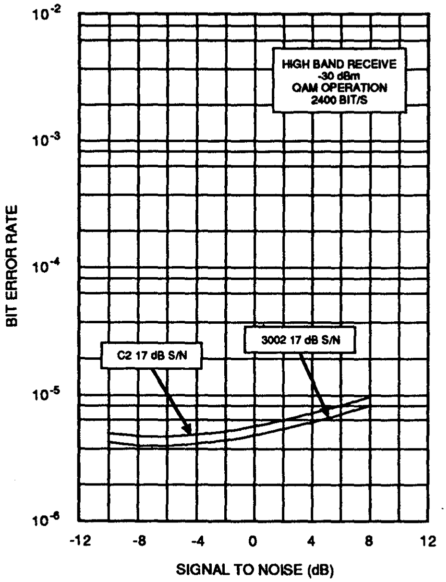
TYPICAL BER PERFORMANCE

(-20dBm receive level 10-5 BER)

PARAMETER - RECEIVE BAND C-WEIGHTED	MINIMUM SNR REQUIRED
2400 bit/s Originate	17 dB SNR
2400 bit/s Answer	18.5 dB SNR
1200 bit/s Originate	8.0 dB SNR
1200 bit/s Answer	8.5 dB SNR
0-300 bit/s Originate	8.0 dB SNR
0-300 bit/s Answer	8.0 dB SNR

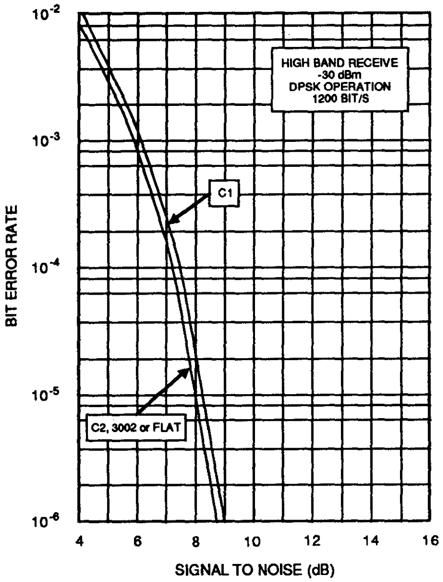
SSI 73K224L BER vs CARRIER OFFSET

PRELIMINARY



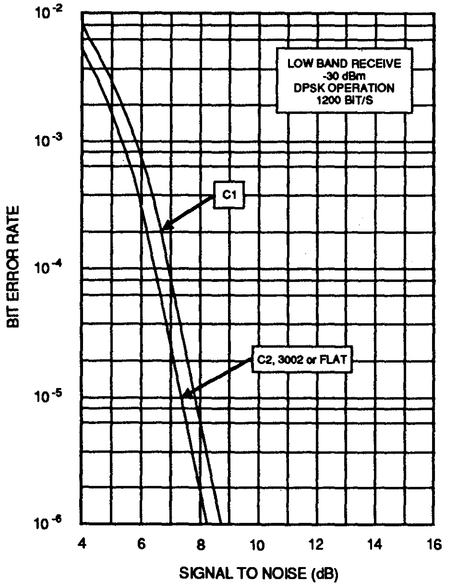
SSI 73K224L BER vs S/N

PRELIMINARY

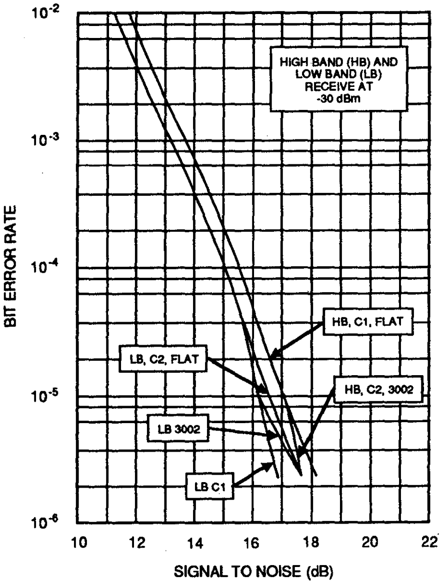


SSI 73K224L BER vs S/N

PRELIMINARY



SSI 73K224L BER vs QAM



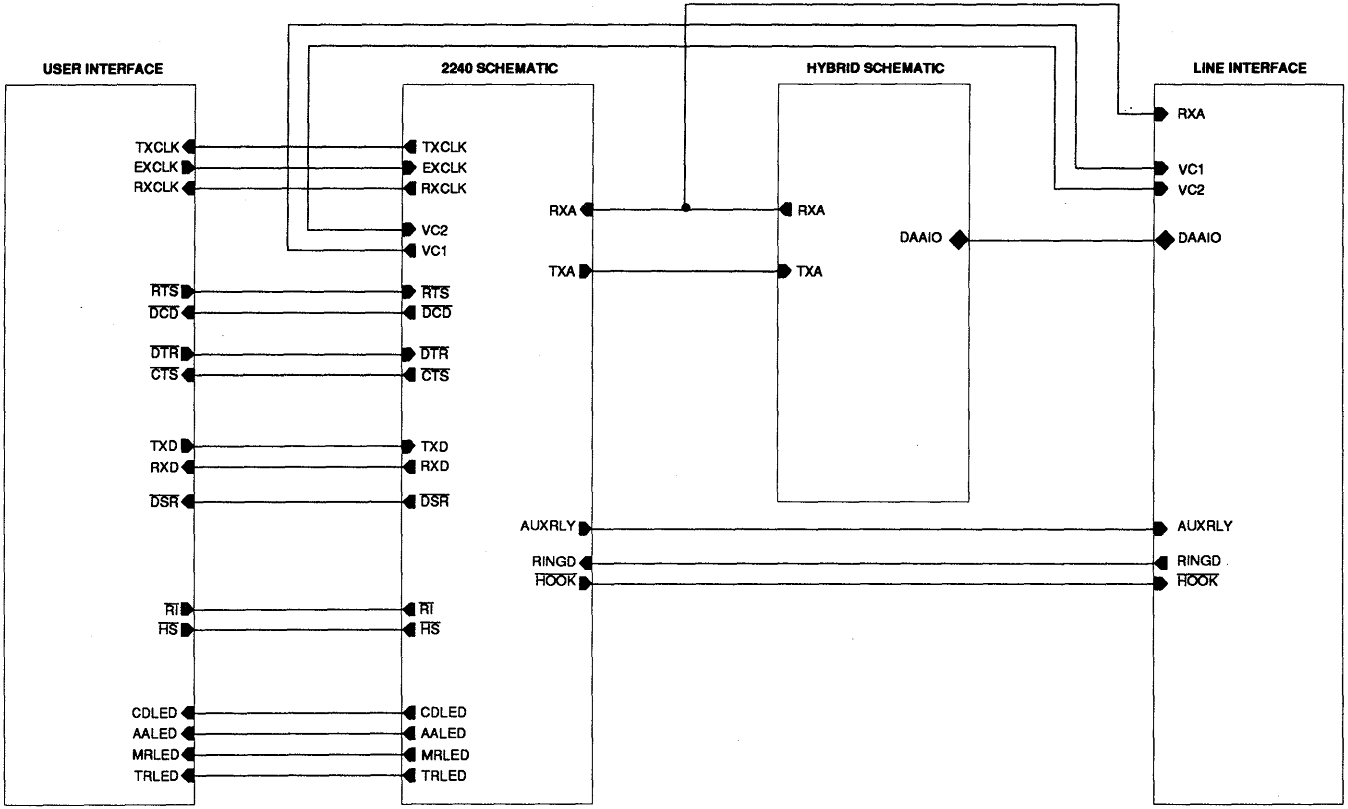


FIGURE 2: SSI 73D2240 Box Modem Block Diagram

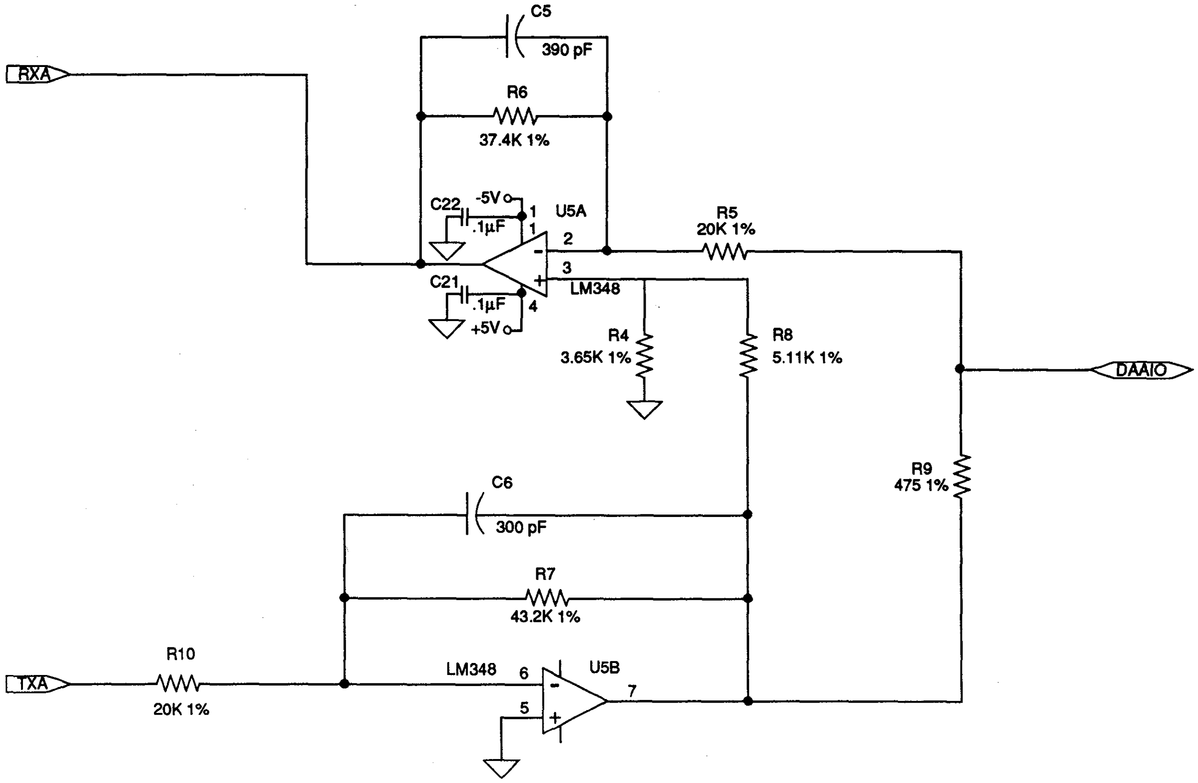


FIGURE 3: SSI 73D2240 Hybrid

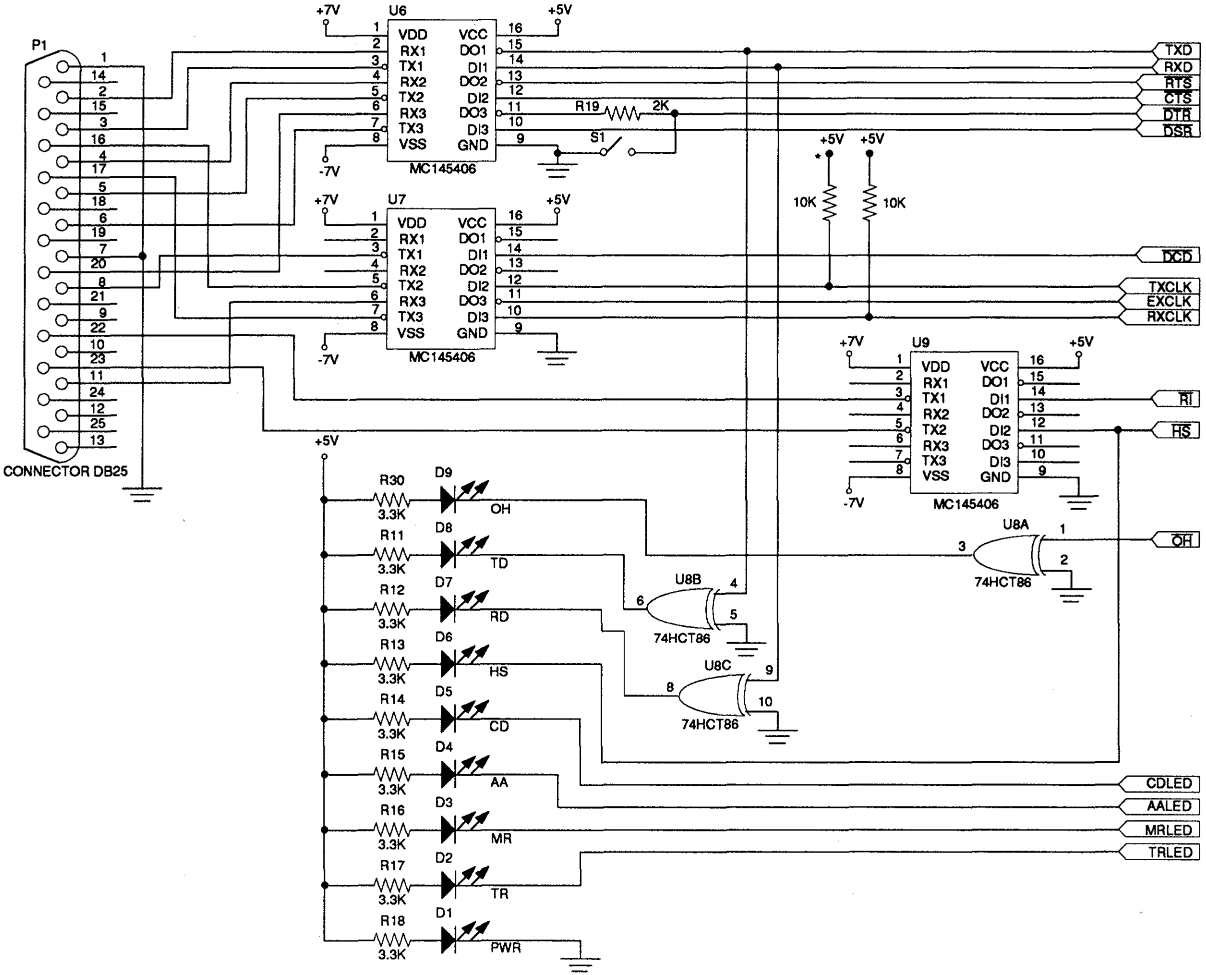


FIGURE 4: 73D2240 User Interface

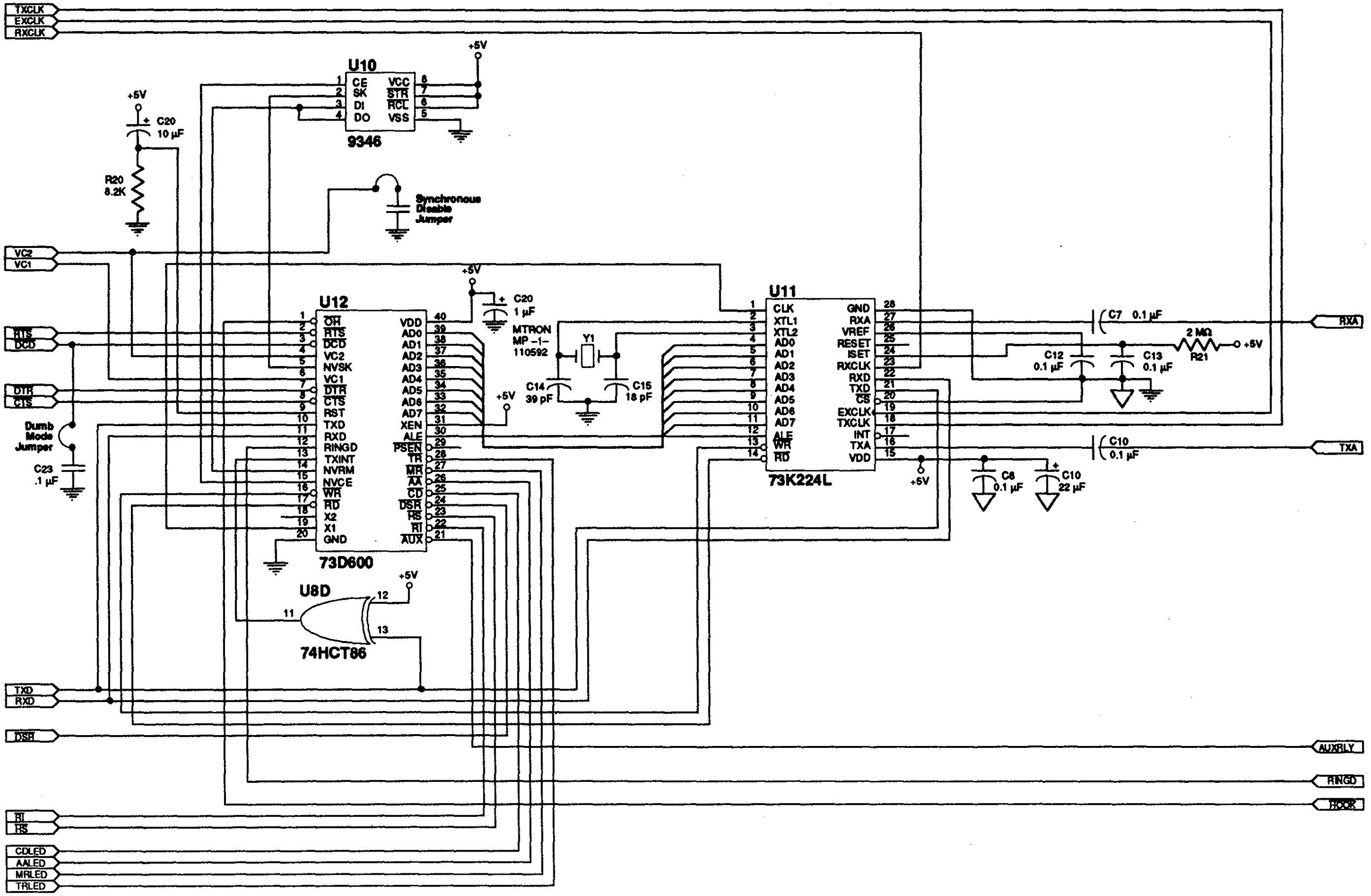


FIGURE 5: 73D2240 Interconnect

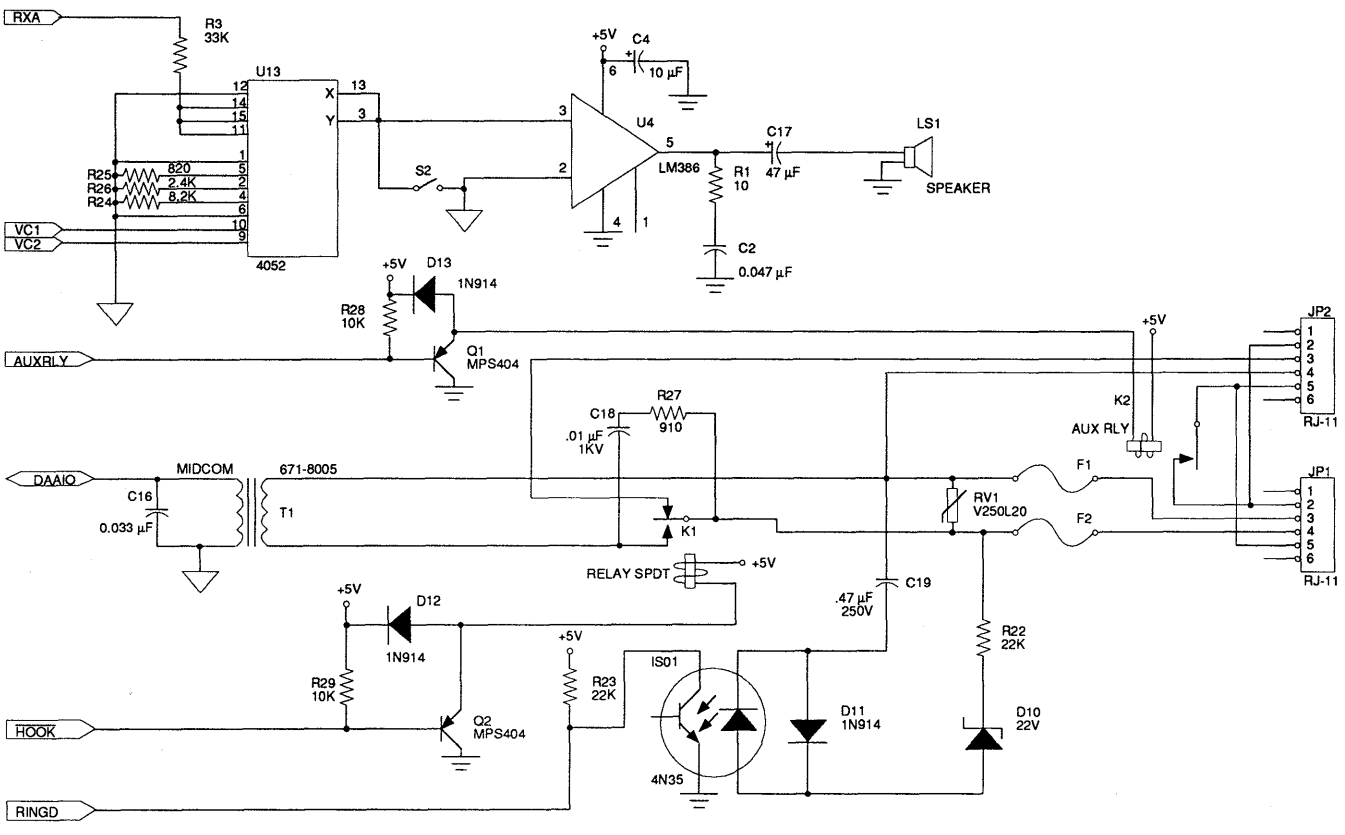
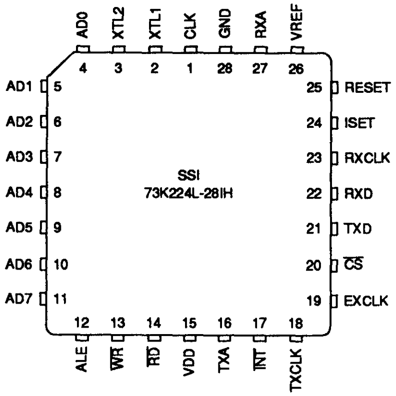


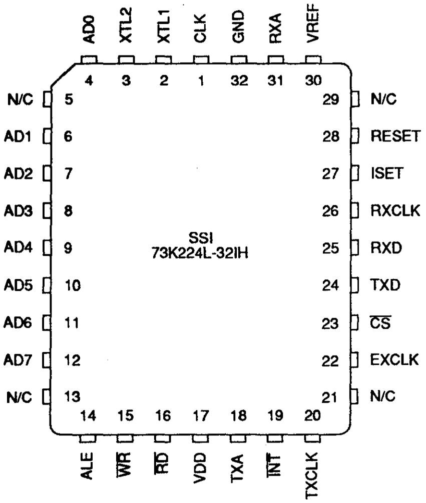
FIGURE 6: 73D2240 Line Interface

PIN DIAGRAMS

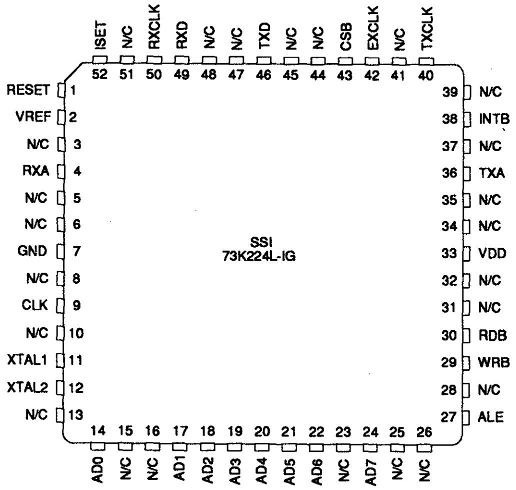
(TOP VIEW)



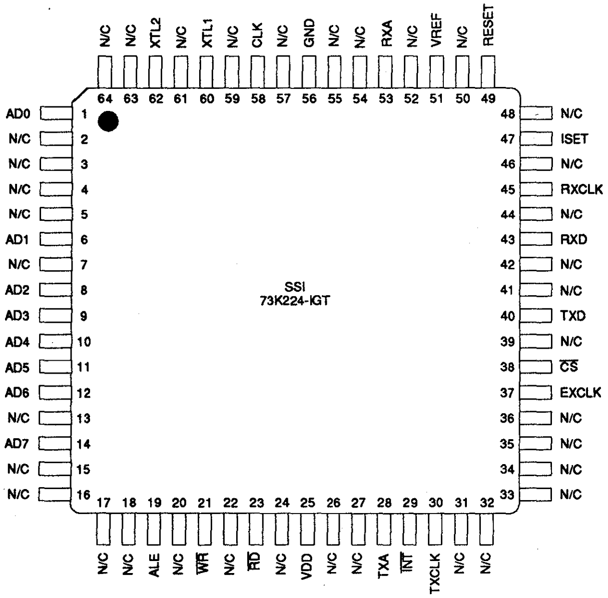
28-Pin PLCC



32-Pin PLCC



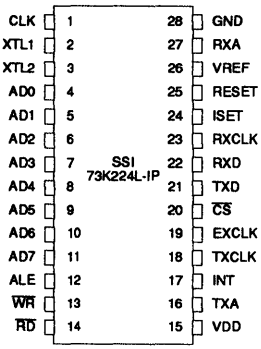
52-Lead PLCC



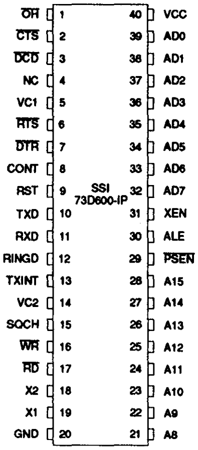
64-Lead TQFP

SSI 73D2240
V.22bis 2400 Bit/s
Modem Device Set

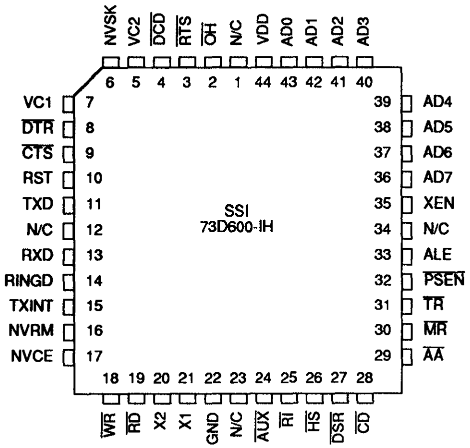
PIN DIAGRAMS
(TOP VIEW)



28-Pin DIP



40-Pin DIP



44-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73D2240 Dual In-Line Package	SSI 73D2240-IP	
28-pin Plastic DIP		73K224L-IP
40-pin Plastic DIP		73D600A-IP
SSI 73D2240 Surface Mount Package	SSI 73D2240-IH	
28-pin Plastic Leaded Chip Carrier		73K224L-28IH
32-pin Plastic Leaded Chip Carrier		73K224L-32IH
44-pin Plastic Leaded Chip Carrier		73D600C-IH
52-Lead Quad Fine Pitch Package		73K224L-IG
64-Lead Thin Quad Flat Pack Package		73K224-IGT

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SSI 73D2247
MNP5, V.42bis Datacom Modem Device Set

January 1993

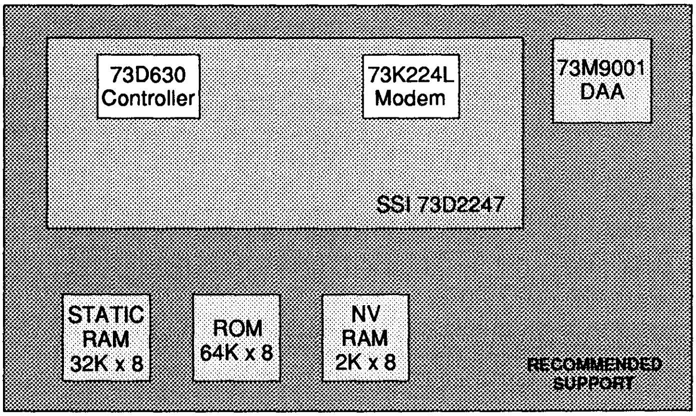
DESCRIPTION

The SSI 73D2247 Chip Set consists of two CMOS integrated circuits which provide the data pump and protocol functions required to implement a high performance 2400 bit/s modem with error control and data compression. The basic modem function is provided by the SSI 73K224L modem chip and is compatible with CCITT V.21, V.22, V.22bis and Bell 103 and 212A protocols. The error control functions are provided by modular software running in the SSI 73D630 controller. Modules are available for MNP4, and V.42. Compression software modules can be can be added to the controller; MNP5 and V.42bis are available. Provisions for customization of the Command Set are provided, forming the basis for an International Modem.

FEATURES

- **Combines Modem and Protocol Controller**
- **Supports 0 - 300, 1200 and 2400 bit/s with both Sync and Async Modes**
- **Modular Software Design Allows Customization**
- **Modem Protocols:**
  - **Bell 103, 212A**
  - **CCITT V.22, V.22bis**
- **Error Control/Compression Protocols Available: MNP4, MNP5, CCITT V.42, V.42bis**
- **Supports Non-volatile Memory to Store User Configurations and Phone Number Blacklists**
- **CMOS Design for Low Power Consumption**

MNP5, V.42bis Datacom Modem Device Set



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73D2247
MNP5, V.42bis Datacom Modem Device Set

FUNCTIONAL DESCRIPTION

The SSI 73D2247 chip set forms the basis for an international modem design incorporating the most advanced error control and compression algorithms. The set consists of two chips, the SSI 73K224L modem and the 73D630 controller. Customization of the controller is one of the features of this chip set; software modules allow the modem vendor to provide a range of features from a standard hardware platform.

The 73K224L provides the QAM, PSK and FSK modulator and demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guardtones. This single-chip modem supports the V.22bis, V.22, V.21 and Bell 103/212A operating protocols in both sync and async modes. Low level functions of the controller provide for automatic detection of DTE speed, auto-dial, auto-answer, handshake with fallback and call progress detection.

A coded version of the 73K224L modem chip is used with the 73D2247 chip set firmware provided by Silicon Systems. Different versions of the controller code can be generated by the modem manufacturer, with "AT" commands only, MNP5 with 8K SRAM, and V.42bis with 32K SRAM as examples.

The 73D630 controller handles both the low level modem functions as well as protocol negotiation and protocol operation. Software modules can be chosen to provide the desired protocols for product customization and differentiation. In addition, the "AT" command set source code will be available for those desiring to provide unique or country dependent features.

QAM Modulator/Demodulator

PSK Modulator/Demodulator

FSK Modulator/Demodulator

Passband Filters and Equalizers

Adaptive Equalization with Retrain

Basic capabilities of the modem are those found in the 73K224L Single-Chip Modem and are listed in the separate 73K224L data sheet.

AUTOMATIC HANDSHAKE

The 73D2247 will automatically perform a complete handshake with a called or calling modem and enter the data transfer mode. After the link between the two modems has been established, the modems may remain in the normal data mode or negotiate a link which has error control and data compression. Commands are provided to inform the modem which action is appropriate.

TEST MODES

The 73D2247 chip set has provisions for three test modes: analog loopback, digital loopback and remote digital loopback. Analog loopback allows data to be sent into the local modem, have it modulated and then demodulated and returned to the local terminal. Digital loopback requires the cooperation of the user at the remote end and allows data to be sent to the remote modem, demodulated, then remodulated and returned to the local end. Remote digital loopback allows the same capability, without the need for a remote operator; signals are sent to the remote modem which perform the switching task that a remote operator would have done.

AT COMMAND INTERPRETER

The SSI 73D2247 includes an AT Command Interpreter which is a superset of the Hayes 2400 Smartmodem™ command set. Common application software will be able to control the modem though this interpreter. Additional commands have been added to provide for control of the MNP and CCITT V.42 modes.

NON-VOLATILE MEMORY

Two modes of operation depend on the use of non-volatile memory: end user configuration storage and telephone number blacklisting. Current hardware provides for a 2K byte memory of which about 400 bytes are used for setup and telephone number storage. The remaining 1600 bytes are avaliable. Memory address space allocated to non-volatile RAM is 8K, so an expansion factor of 4 is available. Alternatively, the address space could be decoded for more hardware functionality.

PROTOCOLS

Microcom Networking Protocol (MNP)

MNP4 is a protocol offering error control while MNP5 offers data compression. Data to be transmitted is broken into blocks of varying sizes, depending on line conditions, and sent to the remote modem along with a 16-bit Cyclic Redundancy Check word. If the algorithm used to derive the CRC word at the transmitter does not produce an identical word when exercised on the received data, a line error is assumed, and the block is repeated. Data compression is obtained by transmitting a short set of characters for a longer redundant set. At the receiver, the short string is replaced with the longer string that it represented, and the data stream is returned to its original state.

CCITT V.42 and V.42bis

The CCITT has ratified a set of protocols which operate in a manner similar to MNP. MNP4 corresponds to V.42 while MNP5 corresponds with V.42bis. Greater efficiency is offered, but the tradeoff is a larger memory space requirement. MNP5 requires an 8K buffer, while V.42bis requires 32K. Data files which show compression ratios approaching 2:1 with MNP5 may show ratios of nearly 4:1 with V.42bis.

ADDITIONAL INFORMATION

The SSI 73D2247 Design Manual completely defines the AT commands, gives a description of the hardware and provides instructions for modifying the code for customization. Please contact your local Silicon Systems sales office or Silicon Systems headquarters in Tustin for a copy of the SSI 73D2247 Design Manual.

AT COMMAND SUMMARY

Command	Description
AT	command prefix – precedes command line
<CR>	carriage return character – terminates command line
A	go into answer mode; attempt to go to on-line state
A/	re-execute previous command line; not preceded by AT nor followed by <CR>
B0	select CCITT V.22 standard for 1200 bit/s communication
B1	***select Bell 212A standard for 1200 bit/s communication***
D	dial number that follows; attempt to go to on-line state, originate mode
DS=n	dial stored number in location "n" (0-3)
E0	Disable character echo in command state
E1	***Enable character echo in command state***
H0	go on hook (hang up)
H1	go off hook; operate auxiliary relay
I0	request product indentification code
I1	perform checksum on firmware ROM; return checksum
I2	perform checksum on firmware ROM; returns OK or ERROR result codes
L0 or L1	low speaker volume
L2	***medium speaker volume***
L3	high speaker volume
M0	speaker off
M1	***speaker on until carrier detected***
M2	speaker always on
M3	speaker on until carrier detected, except during dialing
O0	go to on-line state
O1	go to on-line state and initiate equalizer retrain at 2400 bit/s
Q0	***modem returns result codes***
Q1	modem does not return result codes
Sr	set pointer to register "r"
Sr=n	set register "r" to value "n"
Sr?	display value stored in register "r"
V0	display result codes in numeric form
V1	***display result codes in verbose form (as words)***
W0	***negotiation progress result codes not returned***
W1	negotiation progress result codes returned
X0	enable features represented by result codes 0-4
X1	enable features represented by result codes 0-5, 10-12
X2	enable features represented by result codes 0-6, 10-12
X3	enable features represented by result codes 0-5, 7, 10-12
X4	***enable features represented by result codes 0-7, 10-12***
Y0	***disable long space disconnect***
Y1	enable long space disconnect
Z0	reset modem
&C0	***assume data carrier always present***
&C1	track presence of data carrier
&D0	***ignore DTR signal***
&D1	assume command state when an on-to-off transition of DTR occurs
&D2	hang up and assume command state when an on-to-off transition of DTR occurs
&D3	reset when an on-to-off transition of DTR occurs
&F	recall factory settings as active configuration
&G0	***no guard tone***
&G1	550 Hz guard tone
&G2	1800 Hz guard tone
&K	flow control method
&M0	***asynchronous mode***
&M1	synchronous mode 1
&M2	synchronous mode 2
&M3	synchronous mode 3
&Q5	error control mode
&Q6	automatic speed buffering (ASB)
&T0	terminate test in progress
&T1	initiate local analog loopback
&T3	initiate local digital loopback
&T4	***grant request from remote modem for RDL***
&T5	deny request from remote modem for RDL
&T6	initiate remote digital loopback
&T7	initiate remote digital loopback with self test
&T8	initiate local analog loopback with self test
&V	view active configuration, user profiles, and stored numbers
&W0	save storable parameters of active configuration
&X0	***modem provides transmit clock signal***
&X1	data terminal provides transmit clock signal
&X2	receive carrier provides transmit clock signal
&Zn=x	store phone number "x" in location "n" (0-3)

Dial string arguments:

, = delay	@ = silent answer	! = flash	
; = return to command	s = dial stored number	W = wait for tone	R=reverse mode

If the NovRAM has not been initialized it may be necessary to Power down/Power up and type *AT&F&W<cr>* to properly initialize modem state.

TABLE 1: Result Codes

Xn	VERBOSE/TERSE RESULT CODES
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6, NO ANSWER/8

TABLE 2: S Registers Supported

Sn	FUNCTION	UNITS	DEFAULT
S0[1]	Answer on ring	No. of rings on which to answer	000[2]
S1	Ring counter	No. of rings accumulated	000
S2	Escape code	ASCII CHR Decimal 0-127	043
S3	Carriage return	ASCII CHR Decimal 0-127	013
S4	Line feed	ASCII CHR Decimal 0-127	010
S5	Back space	ASCII CHR	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds (0.1 sec)	006
S10	Carrier drop out	100 milliseconds (0.1 sec)	014
S11	DTMF tone duration	1 millisecond (0.001 sec)	070
S12	Escape guard time	20 milliseconds (0.05 sec)	050
S13	Unused		N/A
*S14[1]	Bit mapped register	Decimal 0-255	170

[1] Stored in NVRAM with &W command.

[2] Modem will not answer until value is changed to 1 or greater.

TABLE 2: S Registers Supported (Continued)

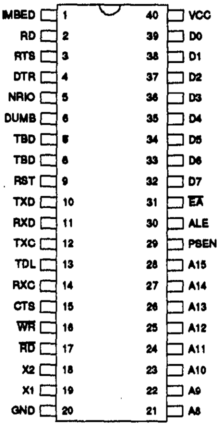
NUMBER	FUNCTION	UNITS	DEFAULT
S15	Unused		N/A
S16	Test register	Decimal #	000
S17	SSi Special test register	Decimal 0-255	096
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[1]	Bitmapped register	Decimal 0-255	000
*S22[1]	Bitmapped register	Decimal 0-255	118
*S23[1]	Bitmapped register	Decimal 0-255	007
S24	Unused		N/A
S25[1]	DTR delay	10 milliseconds (0.01 sec)	005
S26[1]	CTS delay	10 milliseconds (0.01 sec)	001
*S27[1]	Bitmapped register	Decimal 0-255	064
S36	Negotiation failure treatment		5
S37	Desired modem line speed	Decimal 0-9	000
S38	Hang-up timeout		20
S39	Current flow control setting		3
S43	Current DCE speed		0
S46	Protocol/Compression selection		2
S48	Feature negotiation action		7
S49	ASB Buffer low limit	1-249	8
S50	ASB Buffer high limit	2-250	16
S82	Break select register		128
S95	Extended result code bit map		0

* The bitmapped register functions are equivalent to normal "AT" command modem registers.

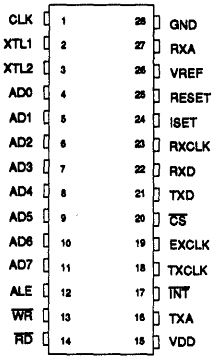
[1] Stored in NVRAM with &W command

SSI 73D2247
MNP5, V.42bis Datacom
Modem Device Set

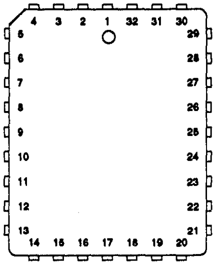
PACKAGE PIN DESIGNATIONS (Top View)



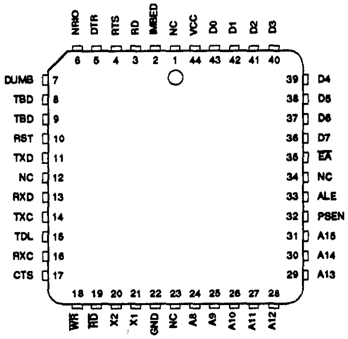
SSI 73D630/631
40-PIN DIP



SSI 73K224
28-PIN DIP



SSI 73K224
32-PIN PLCC



SSI 73D630/631
44-PIN PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK		
		Data Modem	Controller	Fax Modem
AT, MNP2-5, V.42, V.42bis Device Set				
Plastic Dual In-Line	73D2247Z-IP	73K224LZ-IP	11 MHz: 73D630-IP 22 MHz: 73D631-IP	N/A
Plastic Leaded Chip Carrier	73D2247Z-IH	73K224LZ-IH	11 MHz: 73D630-IH 22 MHz: 73D631-IH	N/A
SSI 73D2247 with FAX				
Plastic Dual In-Line	73D2247ZF-IP	73K224LZ-IP	11 MHz: 73D631-IP	Yamaha YTM401D
Plastic Leaded Chip Carrier	73D2247ZF-IH	73K224LZ-IH	11 MHz: 73D631-IH	Yamaha YTM401J

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Notes:

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SSI 73D2247-F
MNP5, V.42bis Datacom and FAX Modem Device Set

January 1993

DESCRIPTION

The SSI 73D2247-F Chip Set consists of two CMOS integrated circuits which provide the data pump and protocol functions required to implement a high performance 2400 bit/s modem with error control and data compression. The basic modem function is provided by the SSI 73K224L modem chip and is compatible with CCITT V.21, V.22, V.22bis and Bell 103 and 212A protocols. The error control functions are provided by modular software running in the SSI 73D630 controller. Modules are available for MNP4, and V.42. Compression software modules can be added to the controller, MNP5 and V.42bis are available.

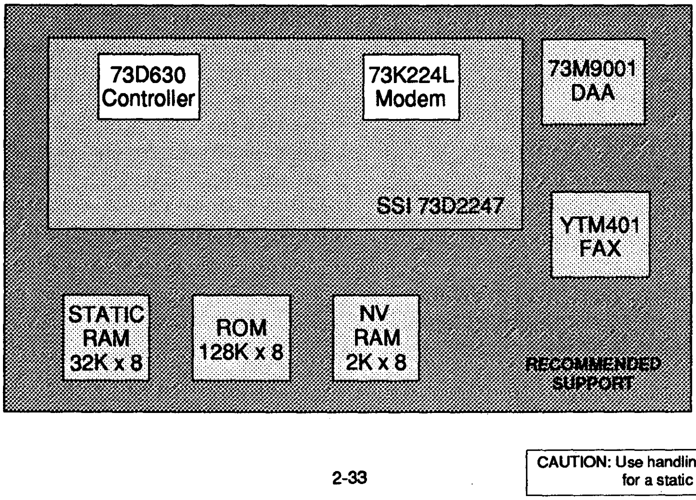
Send and Receive FAX capability is provided by adding a Yamaha YTM401 device. Firmware supporting class 1 FAX commands is provided.

Provisions for customization of the Command Set are provided, forming the basis for an International Modem.

FEATURES

- **Combines Modem and Protocol Controller**
- **Supports 0 - 300, 1200 and 2400 bit/s with both Sync and Async Modes**
- **Modular Software Design Allows Customization**
- **Modem Protocols:**
  - **Bell 103, 212A**
  - **CCITT V.22, V.22bis**
- **Error Control/Compression Protocols Available: MNP4, MNP5, CCITT V.42, V.42bis**
- **Supports Non-volatile Memory to Store User Configurations and Phone Number Blacklists**
- **CMOS Design for Low Power Consumption**
- **Available with MNP5 only: 73D2247/5**
- **Send and Receive FAX Capability**
  - **9600, 7200, 4800, 2400 bit/s**
  - **Firmware Support Provided**

MNP5, V.42bis Datacom and FAX Modem Device Set



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73D2247-F
MNP5, V.42bis Datacom Modem Device Set

FUNCTIONAL DESCRIPTION

The SSI 73D2247-F chip set forms the basis for an international modem design incorporating the most advanced error control and compression algorithms. The set consists of two chips, the SSI 73K224L modem and the SSI 73D630 controller. Customization of the controller is one of the features of this chip set; software modules allow the modem vendor to provide a range of features from a standard hardware platform.

The SSI 73K224L provides the QAM, PSK and FSK modulator and demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guardtones. This single-chip modem supports the Bell 212, V.22 and V.22bis operating protocols in both sync and async modes. V.21 and Bell 103 are supported in async mode. Low level functions of the controller provide for automatic detection of DTE speed, auto-dial, auto-answer, handshake with fallback and call progress detection.

A coded version of the 73K224L modem chip is used with the 73D2247 chip set firmware provided by Silicon Systems. Different versions of the controller code can be generated by the modem manufacturer, with "AT" commands only, MNP5 with 8K SRAM, and V.42bis with 32K SRAM as examples.

The SSI 73D630 controller handles both the low level modem functions as well as protocol negotiation and protocol operation. Software modules can be chosen to provide the desired protocols for product customization and differentiation. In addition, the "AT" command set source code will be available for those desiring to provide unique or country dependent features.

QAM Modulator/Demodulator

PSK Modulator/Demodulator

FSK Modulator/Demodulator

Passband Filters and Equalizers

Adaptive Equalization with Retrain

Basic capabilities of the modem are those found in the SSI 73K224L Single-Chip Modem and are listed in the separate SSI 73K224L data sheet.

AUTOMATIC HANDSHAKE

The SSI 73D2247-F data modem will automatically perform a complete handshake with a called or calling modem and enter the data transfer mode. After the link between the two modems has been established, the modems may remain in the normal data mode or negotiate a link which has error control and data compression. Commands are provided to inform the modem which action is appropriate.

TEST MODES

The SSI 73D2247-F chip set has provisions for three test modes: analog loopback, digital loopback and remote digital loopback. Analog loopback allows data to be sent into the local modem, have it modulated and then demodulated and returned to the local terminal. Digital loopback requires the cooperation of the user at the remote end and allows data to be sent to the remote modem, demodulated, then remodulated and returned to the local end. Remote digital loopback allows the same capability, without the need for a remote operator; signals are sent to the remote modem which perform the switching task that a remote operator would have done.

AT COMMAND INTERPRETER

The SSI 73D2247-F includes an AT Command Interpreter which is a superset of the Hayes 2400 Smartmodem™ command set. Common application software will be able to control the modem though this interpreter. Additional commands have been added to provide for control of the MNP and CCITT V.42 modes.

NON-VOLATILE MEMORY

Two modes of operation depend on the use of non-volatile memory: end user configuration storage and telephone number blacklisting. Current hardware provides for a 2K byte memory of which about 400 bytes are used for setup and telephone number storage. The remaining 1600 bytes are avaliable. Memory address space allocated to non-volatile RAM is 8K, so an expansion factor of 4 is available.

Alternatively, the address space could be decoded for more hardware functionality. Additional support will be provided for an optional serial EPROM (4k bit).

FAX SUPPORT

FAX capability is added to the basic SSI 73D2247 by adding the Yamaha YTM401 data pump chip. In addition to added chip select logic the EEPROM must be upgraded from 64k x 8 to 128k x 8.

PROTOCOLS

Microcom Networking Protocol (MNP)

MNP4 is a protocol offering error control while MNP5 offers data compression. Data to be transmitted is broken into blocks of varying sizes, depending on line conditions, and sent to the remote modem along with a 16-bit Cyclic Redundancy Check word. If the algorithm used to derive the CRC word at the transmitter does not produce an identical word when exercised on the received data, a line error is assumed, and the block is repeated. Data compression is obtained by transmitting a short set of characters for a longer redundant set. At the receiver, the short string is replaced with the longer string that it represented, and the data stream is returned to its original state.

CCITT V.42 and V.42bis

The CCITT has ratified a set of protocols which operate in a manner similar to MNP. MNP4 corresponds to V.42 while MNP5 corresponds with V.42bis. Greater efficiency is offered, but the tradeoff is a larger memory space requirement. MNP5 requires an 8K buffer, while V.42bis requires 32K. Data files which show compression ratios approaching 2:1 with MNP5 may show ratios of nearly 4:1 with V.42bis.

EIA/TIA - 578

EIA - 578 is an ANSI standard covering "Asynchronous Facsimile DCE Control" for Group 3 Facsimile terminals. It consists of "AT" commands similar to a data modem (preceded by a "+F") for data pump control. This insures compatibility with 3rd party personal computer applications DTE software designed for FAX communications.

ADDITIONAL INFORMATION

The SSI 73D2247 Design Manual completely defines the AT commands, gives a description of the hardware and provides instructions for modifying the code for customization. Please contact your local Silicon Systems sales office or Silicon Systems headquarters in Tustin for a copy of the SSI 73D2247 Design Manual.

AT COMMAND SUMMARY

Command	Description
AT	command prefix – precedes command line
<CR>	carriage return character – terminates command line
A	go into answer mode; attempt to go to on-line state
A/	re-execute previous command line; not preceded by AT nor followed by <CR>
B0	select CCITT V.22 standard for 1200 bit/s communication
B1	***select Bell 212A standard for 1200 bit/s communication***
D	dial number that follows; attempt to go to on-line state, originate mode
DS=n	dial stored number in location "n" (0-3)
E0	Disable character echo in command state
E1	***Enable character echo in command state***
H0	go on hook (hang up)
H1	go off hook; operate auxiliary relay
I0	request product indentification code
I1	perform checksum on firmware ROM; return checksum
I2	perform checksum on firmware ROM; returns OK or ERROR result codes
L0 or L1	low speaker volume
L2	***medium speaker volume***
L3	high speaker volume
M0	speaker off
M1	***speaker on until carrier detected***
M2	speaker always on
M3	speaker on until carrier detected, except during dialing
O0	go to on-line state
O1	go to on-line state and initiate equalizer retrain at 2400 bit/s
Q0	***modem returns result codes***
Q1	modem does not return result codes
Sr	set pointer to register "r"
Sr=n	set register "r" to value "n"
Sr?	display value stored in register "r"
V0	display result codes in numeric form
V1	***display result codes in verbose form (as words)***
W0	***negotiation progress result codes not returned***
W1	negotiation progress result codes returned
X0	enable features represented by result codes 0-4
X1	enable features represented by result codes 0-5, 10-12
X2	enable features represented by result codes 0-6, 10-12
X3	enable features represented by result codes 0-5, 7, 10-12
X4	***enable features represented by result codes 0-7, 10-12***
Y0	***disable long space disconnect***
Y1	enable long space disconnect

Command	Description
Z0	reset modem
&C0	***assume data carrier always present***
&C1	track presence of data carrier
&D0	***ignore DTR signal***
&D1	assume command state when an on-to-off transition of DTR occurs
&D2	hang up and assume command state when an on-to-off transition of DTR occurs
&D3	reset when an on-to-off transition of DTR occurs
&F	recall factory settings as active configuration
&G0	***no guard tone***
&G1	550 Hz guard tone
&G2	1800 Hz guard tone
&K	flow control method
&M0	***asynchronous mode***
&M1	synchronous mode 1
&M2	synchronous mode 2
&M3	synchronous mode 3
&Q5	error control mode
&Q6	automatic speed buffering (ASB)
&T0	terminate test in progress
&T1	initiate local analog loopback
&T3	initiate local digital loopback
&T4	***grant request from remote modem for RDL***
&T5	deny request from remote modem for RDL
&T6	initiate remote digital loopback
&T7	initiate remote digital loopback with self test
&T8	initiate local analog loopback with self test
&V	view active configuration, user profiles, and stored numbers
&W0	save storable parameters of active configuration
&X0	***modem provides transmit clock signal***
&X1	data terminal provides transmit clock signal
&X2	receive carrier provides transmit clock signal
&Zn=x	store phone number "x" in location "n" (0-3)

FAX AT COMMAND SUMMARY

Command	Description
+FCLASS = n	Select FAX (1) or Data (0)
+FTS = <TIME>	Transmit silence
+FRS = <TIME>	Detect silence
+FRM = <MOD>	Receive data with <MOD> carrier
+FRH = <MOD>	Receive HDLC data with <MOD> carrier
+FTM = <MOD>	Transmit data with <MOD> carrier
+FTH = <MOD>	Transmit HDLC data w/ <MOD> carrier

Dial string arguments:

, = delay	@ = silent answer	! = flash	
; = return to command	s = dial stored number	W = wait for tone	R=reverse mode

If the NovRAM has not been initialized it may be necessary to Power down/Power up and type *AT&F&W<cr>* to properly initialize modem state.

TABLE 1: Result Codes

Xn	VERBOSE/TERSE RESULT CODES
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6, NO ANSWER/8
FAX only	+FCERROR, +F4

TABLE 2: S Registers Supported

Sn	FUNCTION	UNITS	DEFAULT
S0[1]	Answer on ring	No. of rings on which to answer	000[2]
S1	Ring counter	No. of rings accumulated	000
S2	Escape code	ASCII CHR Decimal 0-127	043
S3	Carriage return	ASCII CHR Decimal 0-127	013
S4	Line feed	ASCII CHR Decimal 0-127	010
S5	Back space	ASCII CHR	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds (0.1 sec)	006
S10	Carrier drop out	100 milliseconds (0.1 sec)	014
S11	DTMF tone duration	1 millisecond (0.001 sec)	070
S12	Escape guard time	20 milliseconds (0.05 sec)	050
S13	Unused		N/A
*S14[1]	Bit mapped register	Decimal 0-255	170

[1] Stored in NVRAM with &W command.

[2] Modem will not answer until value is changed to 1 or greater.

TABLE 2: S Registers Supported (Continued)

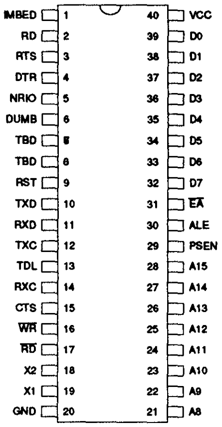
NUMBER	FUNCTION	UNITS	DEFAULT
S15	Unused		N/A
S16	Test register	Decimal #	000
S17	SSi Special test register	Decimal 0-255	096
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[1]	Bitmapped register	Decimal 0-255	000
*S22[1]	Bitmapped register	Decimal 0-255	118
*S23[1]	Bitmapped register	Decimal 0-255	007
S24	Unused		N/A
S25[1]	DTR delay	10 milliseconds (0.01 sec)	005
S26[1]	CTS delay	10 milliseconds (0.01 sec)	001
*S27[1]	Bitmapped register	Decimal 0-255	064
S36	Negotiation failure treatment		5
S37	Desired modem line speed	Decimal 0-9	000
S38	Hang-up timeout		20
S39	Current flow control setting		3
S43	Current DCE speed		0
S46	Protocol/Compression selection		2
S48	Feature negotiation action		7
S49	ASB Buffer low limit	1-249	8
S50	ASB Buffer high limit	2-250	16
S82	Break select register		128
S95	Extended result code bit map		0

* The bitmapped register functions are equivalent to normal "AT" command modem registers.

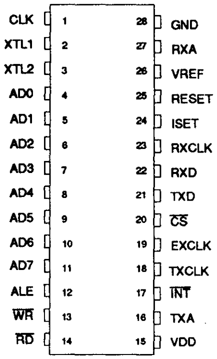
[1] Stored in NVRAM with &W command

SSI 73D2247-F
MNP5, V.42bis Datacom Modem Device Set

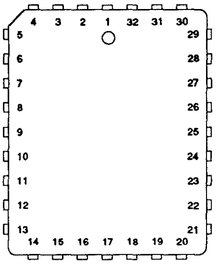
PACKAGE PIN DESIGNATIONS (Top View)



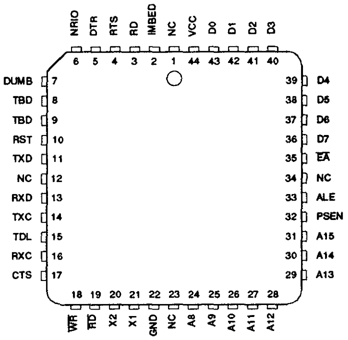
SSI 73D630/631
40-PIN DIP



SSI 73K224
28-PIN DIP



SSI 73K224
32-PIN PLCC



SSI 73D630/631
44-PIN PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK		
		Data Modem	Controller	Fax Modem
AT, MNP2-5, V.42, V.42bis Device Set				
Plastic Dual In-Line	73D2247Z-CP	73K224LZ-CP	11 MHz: 73D630-CP 22 MHz: 73D631-CP	N/A
Plastic Leaded Chip Carrier	73D2247Z-CH	73K224LZ-CH	11 MHz: 73D630-CH 22 MHz: 73D631-CH	N/A
SSI 73D2247 with FAX				
Plastic Dual In-Line	73D2247ZF-CP	73K224LZ-CP	11 MHz: 73D631-CP	Yamaha YTM401D
Plastic Leaded Chip Carrier	73D2247ZF-CH	73K224LZ-CH	11 MHz: 73D631-CH	Yamaha YTM401J

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Notes:

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SSI 73D2248/2348
MNP5, V.42bis Datacom Modem Device Set
Advance Information

January 1993

DESCRIPTION

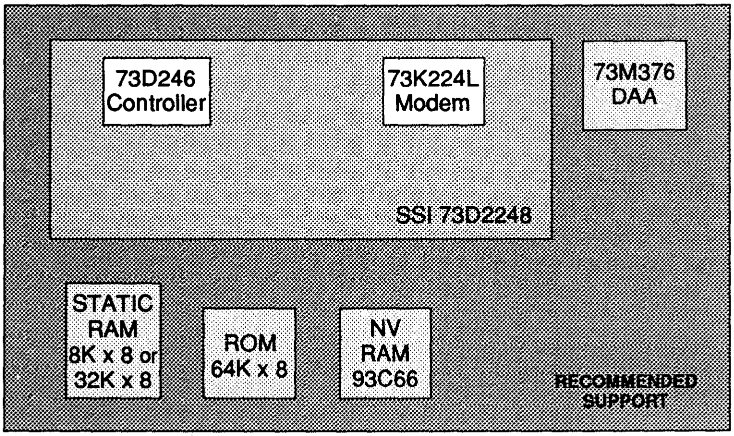
The SSI 73D2248/2348 Chip Sets consists of two CMOS integrated circuits which provide the data pump and protocol functions required to implement a high performance 2400 bit/s modem with error control and data compression. The 73D2248 basic modem function is provided by the SSI 73K224L modem chip and is compatible with CCITT V.21, V.22, V.22bis and Bell 103 and 212A protocols. The error control functions are provided by modular software running in the SSI 73D246 controller. Modules are available for MNP4, and V.42. Compression software modules can be can be added to the controller; MNP5 and V.42bis are available. Provisions for customization of the Command Set are provided, forming the basis for an International Modem.

The 73D2348 differs from the 73D2248 in that it uses the 73K324L instead of the 73K224L for the data pump. The 73K324L replaces the Bell 103 300 baud FSK mode of operation with the CCITT V.23 1200 baud FSK mode. The software is also modified to support V.23. The two products are otherwise identical.

FEATURES

- **Combines Modem and Protocol Controller**
- **Supports 0 - 300, 1200 and 2400 bit/s with both Sync and Async Modes**
- **Modular Software Design Allows Customization**
- **Modem Protocols:**
  - **Bell 103, 212A**
  - **CCITT V.22, V.22bis**
- **Error Control/Compression Protocols Available: MNP4, MNP5, CCITT V.42, V.42bis**
- **Supports Non-volatile Memory to Store User Configurations and Phone Numbers**
- **CMOS Design for Low Power Consumption**
- **TQFP packages available for PCMCIA applications**

MNP5, V.42bis Datacom Modem Device Set



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 73D2248/2348
MNP5, V.42bis Datacom Modem Device Set

FUNCTIONAL DESCRIPTION

The SSI 73D2248/2348 chip set forms the basis for an international modem design incorporating the most advanced error control and compression algorithms. The set consists of two chips, the SSI 73K224L (73K324L) modem and the 73D246 controller. Customization of the controller is one of the features of this chip set; software modules allow the modem vendor to provide a range of features from a standard hardware platform.

The 73K224L (73K324L) provides the QAM, PSK and FSK modulator and demodulator functions, call progress and handshake tone monitors, test modes and a tone generator capable of producing DTMF, answer and CCITT guardtones. This single-chip modem supports the V.22bis, V.22, V.21 and Bell 103/ CCITT V.23/212A operating protocols in both sync and async modes. Low level functions of the controller provide for automatic detection of DTE speed, auto-dial, auto-answer, handshake with fallback and call progress detection.

The 73D246 controller handles both the low level modem functions as well as protocol negotiation and protocol operation. Software modules can be chosen to provide the desired protocols for product customization and differentiation. In addition, the "AT" command set source code will be available for those desiring to provide unique or country dependent features.

Basic capabilities of the modem are those found in the 73K224L (73K324L) Single-Chip Modem and are listed in the separate 73K224L (73K324L) data sheet.

AUTOMATIC HANDSHAKE

The 73D2248/2348 will automatically perform a complete handshake with a called or calling modem and enter the data transfer mode. After the link between the two modems has been established, the modems may remain in the normal data mode or negotiate a link which has error control and data compression. Commands are provided to inform the modem which action is appropriate.

TEST MODES

The 73D2248/2348 chip set has provisions for three test modes: analog loopback, digital loopback and remote digital loopback. Analog loopback allows data to be sent into the local modem, have it modulated and then demodulated and returned to the local terminal. Digital loopback requires the cooperation of the user at the remote end and allows data to be sent to the remote modem, demodulated, then remodulated and returned to the local end. Remote digital loopback allows the same capability, without the need for a remote operator; signals are sent to the remote modem which perform the switching task that a remote operator would have done.

AT COMMAND INTERPRETER

The SSI 73D2248/2348 includes an AT Command Interpreter which is a superset of the Hayes 2400 Smartmodem™ command set. Common application software will be able to control the modem though this interpreter. Additional commands have been added to provide for control of the MNP and CCITT V.42 modes.

NON-VOLATILE MEMORY

A serial NVRAM provides 256 bytes of storage for configuration information and telephone numbers. Current hardware provides for a 2K bit memory of which about 400 bytes are used for setup and telephone number storage. The remaining 1600 bytes are avaliable. Memory address space allocated to non-volatile RAM is 8K, so an expansion factor of 4 is available. Alternatively, the address space could be decoded for more hardware functionality.

PROTOCOLS

Microcom Networking Protocol (MNP)

MNP4 is a protocol offering error control while MNP5 offers data compression. Data to be transmitted is broken into blocks of varying sizes, depending on line conditions, and sent to the remote modem along with a 16-bit Cyclic Redundancy Check word. If the algorithm used to derive the CRC word at the transmitter does not produce an identical word when exercised on the received data, a line error is assumed, and the block is repeated. Data compression is obtained by transmitting a short set of characters for a longer redundant set. At the receiver, the short string is replaced with the longer string that it represented, and the data stream is returned to its original state.

CCITT V.42 and V.42bis

The CCITT has ratified a set of protocols which operate in a manner similar to MNP. MNP4 corresponds to V.42 while MNP5 corresponds with V.42bis. Greater efficiency is offered, but the tradeoff is a larger memory space requirement. MNP5 requires an 8K buffer, while V.42bis requires 32K. Data files which show compression ratios approaching 2:1 with MNP5 may show ratios of nearly 4:1 with V.42bis.

ADDITIONAL INFORMATION

The Silicon Systems Protocol Design Manual defines the AT commands. Please contact your local Silicon Systems sales office or Silicon Systems headquarters in Tustin for a copy of the SSi Protocol Design Manual.

AT COMMAND SUMMARY

Command	Description
AT	command prefix – precedes command line
<CR>	carriage return character – terminates command line
A	go into answer mode; attempt to go to on-line state
A/	re-execute previous command line; not preceded by AT nor followed by <CR>
B0	select CCITT V.22 standard for 1200 bit/s communication
B1	***select Bell 212A standard for 1200 bit/s communication***
D	dial number that follows; attempt to go to on-line state, originate mode
DS=n	dial stored number in location "n" (0-3)
E0	Disable character echo in command state
E1	***Enable character echo in command state***
H0	go on hook (hang up)
H1	go off hook; operate auxiliary relay
I0	request product indentification code
I1	perform checksum on firmware ROM; return checksum
I2	perform checksum on firmware ROM; returns OK or ERROR result codes
L0 or L1	low speaker volume
L2	***medium speaker volume***
L3	high speaker volume
M0	speaker off
M1	***speaker on until carrier detected***
M2	speaker always on
M3	speaker on until carrier detected, except during dialing
O0	go to on-line state
O1	go to on-line state and initiate equalizer retrain at 2400 bit/s
Q0	***modem returns result codes***
Q1	modem does not return result codes
Sr	set pointer to register "r"
Sr=n	set register "r" to value "n"
Sr?	display value stored in register "r"
V0	display result codes in numeric form
V1	***display result codes in verbose form (as words)***
W0	***negotiation progress result codes not returned***
W1	negotiation progress result codes returned
X0	enable features represented by result codes 0-4
X1	enable features represented by result codes 0-5, 10-12
X2	enable features represented by result codes 0-6, 10-12
X3	enable features represented by result codes 0-5, 7, 10-12

Command	Description
X4	***enable features represented by result codes 0-7, 10-12***
Y0	***disable long space disconnect***
Y1	enable long space disconnect
Z0	reset modem
&C0	***assume data carrier always present***
&C1	track presence of data carrier
&D0	***ignore DTR signal***
&D1	assume command state when an on-to-off transition of DTR occurs
&D2	hang up and assume command state when an on-to-off transition of DTR occurs
&D3	reset when an on-to-off transition of DTR occurs
&F	recall factory settings as active configuration
&G0	***no guard tone***
&G1	550 Hz guard tone
&G2	1800 Hz guard tone
&K	flow control method
&M0	***asynchronous mode***
&M1	synchronous mode 1
&M2	synchronous mode 2
&M3	synchronous mode 3
&Q5	error control mode
&Q6	automatic speed buffering (ASB)
&T0	terminate test in progress
&T1	initiate local analog loopback
&T3	initiate local digital loopback
&T4	***grant request from remote modem for RDL***
&T5	deny request from remote modem for RDL
&T6	initiate remote digital loopback
&T7	initiate remote digital loopback with self test
&T8	initiate local analog loopback with self test
&V	view active configuration, user profiles, and stored numbers
&W0	save storable parameters of active configuration
&X0	***modem provides transmit clock signal***
&X1	data terminal provides transmit clock signal
&X2	receive carrier provides transmit clock signal
&Zn=x	store phone number "x" in location "n" (0-3)

Dial string arguments:
, = delay @ = silent answer ! = flash
; = return to command s = dial stored number W = wait for tone R=reverse mode

If the NovRAM has not been initialized it may be necessary to Power down/Power up and type *AT&F&W<cr>* to properly initialize modem state.

TABLE 1: Result Codes

Xn	VERBOSE/TERSE RESULT CODES
X0	OK/0, CONNECT/1, RING/2, NO CARRIER/3, ERROR/4
X1	All functions of X0 + CONNECT (RATE)/1 = 300, 5 = 1200, 10 = 2400
X2	All functions of X1 + NO DIAL TONE/6
X3	All functions of X1 + BUSY/7
X4	All functions of X3 + NO DIAL TONE/6, NO ANSWER/8

TABLE 2: S Registers Supported

Sn	FUNCTION	UNITS	DEFAULT
S0[1]	Answer on ring	No. of rings on which to answer	000[2]
S1	Ring counter	No. of rings accumulated	000
S2	Escape code	ASCII CHR Decimal 0-127	043
S3	Carriage return	ASCII CHR Decimal 0-127	013
S4	Line feed	ASCII CHR Decimal 0-127	010
S5	Back space	ASCII CHR	008
S6	Wait for dial tone	Seconds	002
S7	Wait for carrier	Seconds	030
S8	Pause time	Seconds	002
S9	Carrier valid	100 milliseconds (0.1 sec)	006
S10	Carrier drop out	100 milliseconds (0.1 sec)	014
S11	DTMF tone duration	1 millisecond (0.001 sec)	070
S12	Escape guard time	20 milliseconds (0.05 sec)	050
S13	Unused		N/A
*S14[1]	Bit mapped register	Decimal 0-255	170

[1] Stored in NVRAM with &W command.

[2] Modem will not answer until value is changed to 1 or greater.

TABLE 2: S Registers Supported (Continued)

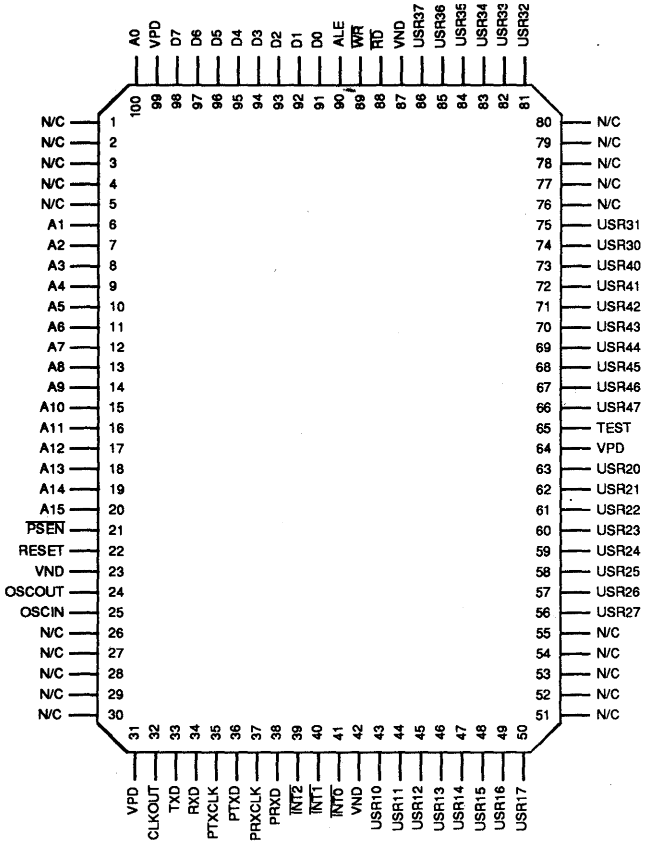
NUMBER	FUNCTION	UNITS	DEFAULT
S15	Unused		N/A
S16	Test register	Decimal #	000
S17	SSi Special test register	Decimal 0-255	096
S18	Test timer	Decimal 0-255	000
S19	Unused		N/A
S20	Unused		N/A
*S21[1]	Bitmapped register	Decimal 0-255	000
*S22[1]	Bitmapped register	Decimal 0-255	118
*S23[1]	Bitmapped register	Decimal 0-255	007
S24	Unused		N/A
S25[1]	DTR delay	10 milliseconds (0.01 sec)	005
S26[1]	CTS delay	10 milliseconds (0.01 sec)	001
*S27[1]	Bitmapped register	Decimal 0-255	064
S36	Negotiation failure treatment		5
S37	Desired modem line speed	Decimal 0-9	000
S38	Hang-up timeout		20
S39	Current flow control setting		3
S43	Current DCE speed		0
S46	Protocol/Compression selection		2
S48	Feature negotiation action		7
S49	ASB Buffer low limit	1-249	8
S50	ASB Buffer high limit	2-250	16
S82	Break select register		128
S95	Extended result code bit map		0

* The bitmapped register functions are equivalent to normal "AT" command modem registers.

[1] Stored in NVRAM with &W command

PACKAGE PIN DESIGNATIONS

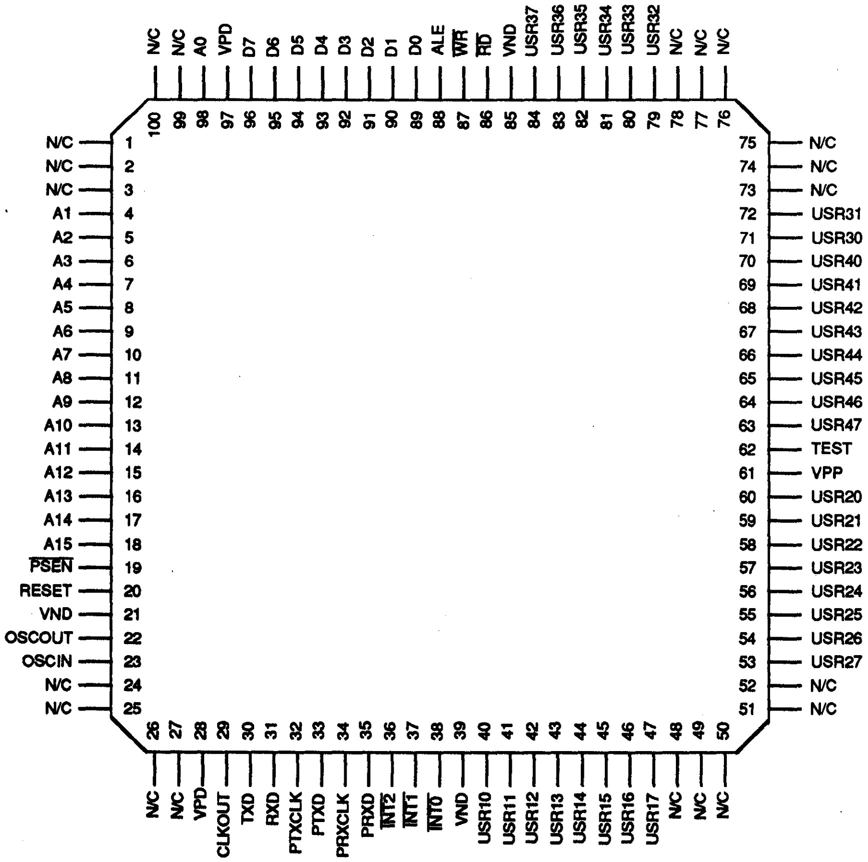
(Top View)



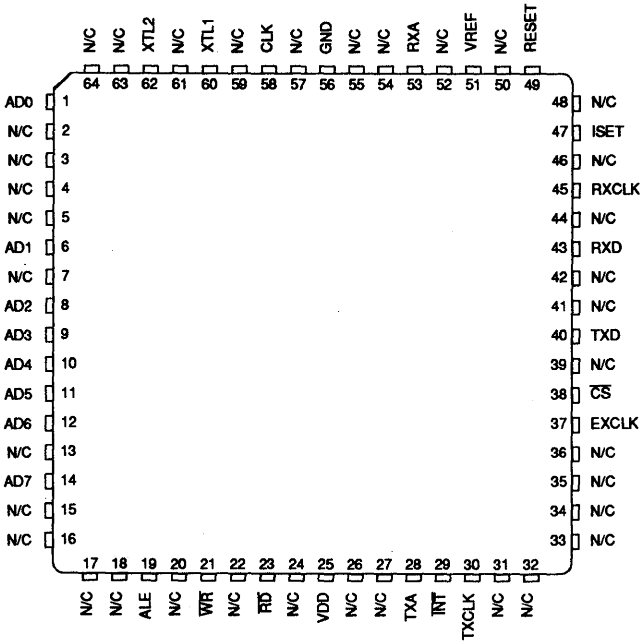
**SSI 73D246
Controller
100-Lead QFP**

PACKAGE PIN DESIGNATIONS

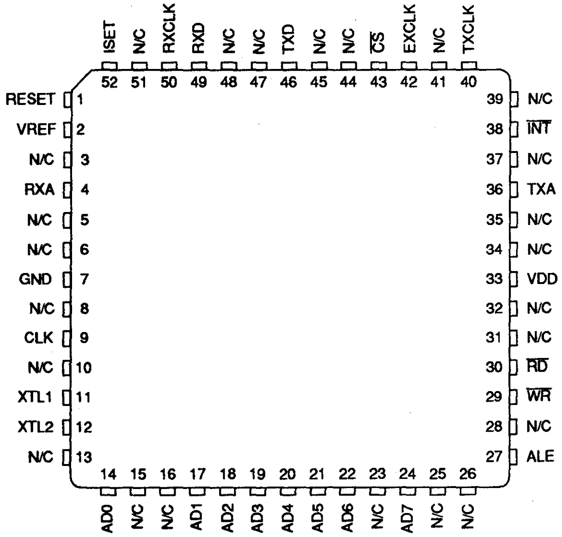
(Top View)



SSI 73D246
Controller
100-Lead TQFP

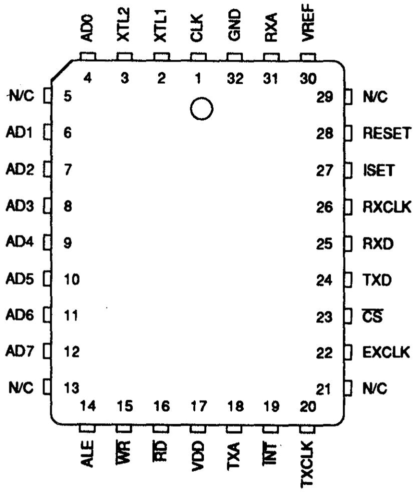


SSI 73K224L
Single Chip Modem
64-Lead TQFP

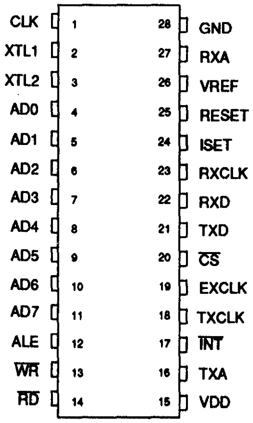


SSI 73K224L
Single Chip Modem
52-Lead QFP

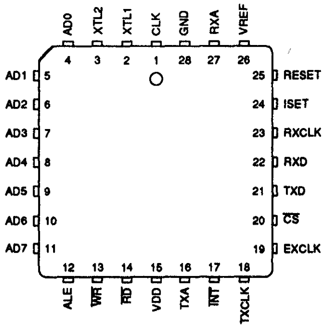
PACKAGE PIN DESIGNATIONS (Top View) (continued)



**SSI 73K224L
Single Chip Modem
32-Pin PLCC**



**SSI 73K224L
Single Chip Modem
28-Pin DIP**



**SSI 73K224L
Single Chip Modem
28-Pin PLCC**

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SSI 73M450L/1450/2450

Universal Asynchronous Receiver/Transmitter

January 1993

DESCRIPTION

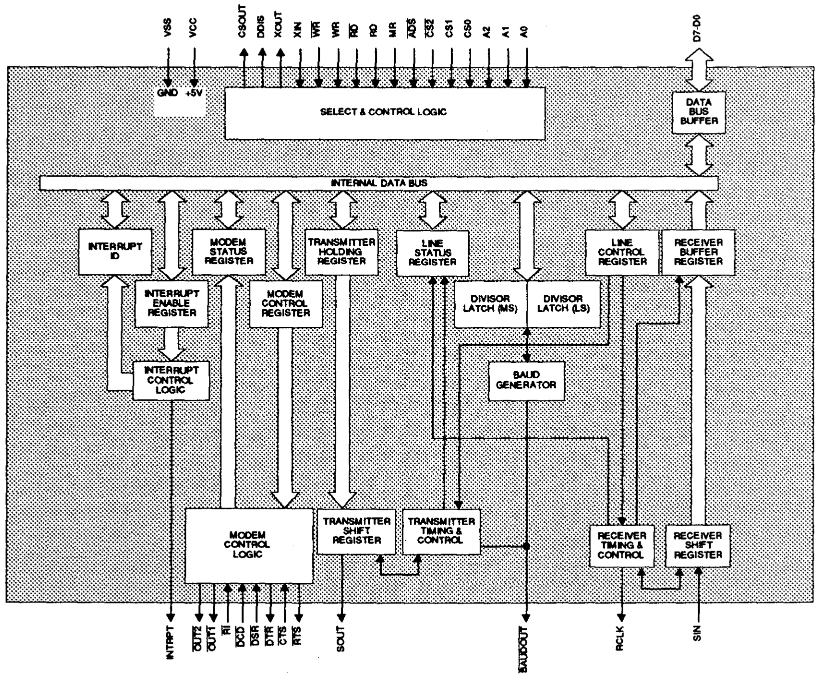
The SSI 73M450L is a Universal Asynchronous Receiver/Transmitter (UART) circuit which is pin- and function-compatible with industry-standard 16C450-type UARTs. It is primarily used in the interface between the serial data port and the parallel peripheral bus in 8-bit microprocessor systems. The SSI 73M450L is available in either a 40-pin DIP or 44-pin PLCC package.

The SSI 73M1450 and SSI 73M2450 are 28-pin versions of the SSI 73M450L. The difference between these versions is that the SSI 73M2450 adds a µPRST pin at the expense of the XOUT pin. See Figure 13 on page 31 for detail. All versions are designed in CMOS for low-power quiescent operation and require a single 5V supply.

FEATURES

- **Compatible with industry standard UARTs**
- **Static CMOS with oscillator shutdown for low-power operation**
- **High drive current allows direct connection to a PC bus**
- **Full double buffering**
- **Independent control of transmit, receive, line status and data set interrupts**
- **Contains modem control function including CTS, RTS, DSR, DTR, RI and DCD**
- **Programmable serial interface characteristics include:**
  - **5, 6, 7 or 8-bit characters**
  - **even, odd or no-parity bit generation and detection**
  - **1, 1 1/2 or 2 stop-bit generation**
  - **baud rate generation (dc to 56K baud)**
- **Full status reporting capabilities**
- **Available in 40-pin DIP, 44-and 28-pin PLCC packages**

BLOCK DIAGRAM



0193 - rev.

PIN DESCRIPTION

BUS INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{\text{ADS}}$	I	Address Strobe: The rising edge of this signal is used for latching the Register Address and Chip Select inputs, thus facilitating interface to a multiplexed Address/Data bus. If not required, $\overline{\text{ADS}}$ should be tied permanently low.
CS0, CS1, $\overline{\text{CS2}}$	I	Chip Select: The UART is selected when CS0 and CS1 are high and $\overline{\text{CS2}}$ is low. Chip selection is complete when the decoded chip select signal is latched with an active (low) $\overline{\text{ADS}}$ input. This enables communication between the UART and the CPU.
A0-2	I	Register Select Address: These pins determine which of the UART registers is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit in the UART's Line Control Register (see Table 1) also controls which register is referenced.
RD, $\overline{\text{RD}}$	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling RD high or $\overline{\text{RD}}$ low while the chip is selected. Since only one input is required for a read, tie either RD permanently low or $\overline{\text{RD}}$ permanently high if not used.
WR, $\overline{\text{WR}}$	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling WR high or $\overline{\text{WR}}$ low while the chip is selected. Since only one input is required for a write, tie either WR permanently low or $\overline{\text{WR}}$ permanently high if not used.
D0-7	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data, control words and status information are transferred via this bus.
CSOUT	O	Chip Select Out: When high, indicates that the chip has been selected by active CS0, CS1 and $\overline{\text{CS2}}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic "1." CSOUT goes low when the chip is deselected.
DDIS	O	Driver Disable: Goes low when the CPU is reading data from the UART. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and UART on the D0-D7 Data Bus) at all times, except when the CPU is reading data.
INTRPT	O	Interrupt: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

DATA I/O

SIN	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

NAME	TYPE	DESCRIPTION
$\overline{\text{RTS}}$	O	Request To Send: This output is programmed by bit 1 of the Modem Control Register and is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{\text{CTS}}$	I	Clear To Send: A modem status input whose condition corresponds to the complement of the CTS bit (bit 4) of the Modem Status Register. When $\overline{\text{CTS}}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{\text{DTR}}$	O	Data Terminal Ready: This output is programmed by bit 0 of the Modem Control Register, and is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{\text{DSR}}$	I	Data Set Ready: A modem status input whose condition corresponds to the complement of the DSR bit (bit 5) of the Modem Status Register. When $\overline{\text{DSR}}$ is low, it indicates that the modem is ready to establish communications.
$\overline{\text{DCD}}$	I	Data Carrier Detect: A modem status input whose condition corresponds to the complement of the DCD bit (bit 7) of the Modem Status Register. When DCD is low, it indicates that the modem is receiving a carrier.
$\overline{\text{RI}}$	I	Ring Indicator: A modem status input whose condition corresponds to the complement of the RI bit (bit 6) of the Modem Status Register. When $\overline{\text{RI}}$ is low, it indicates that a telephone ringing signal is being received.
$\overline{\text{OUT1}}$ $\overline{\text{OUT2}}$	O O	Output 1, 2: User designated outputs that can be set to an active low by setting bit 2 ($\overline{\text{OUT1}}$) or bit 3 ($\overline{\text{OUT2}}$) of the Modem Control Register high. These output signals are set high upon Master Reset or during loop mode operation.

PIN DESCRIPTION (Continued)

GENERAL & CLOCKS

NAME	TYPE	DESCRIPTION
VCC	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to VSS.
VSS	I	System Ground.
MR	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{\text{OUT1}}$, $\overline{\text{OUT2}}$, $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger.
XIN, XOUT	I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source.
RCLK	I	Receiver Clock: This input is the 16X baud rate clock for the receiver section of the chip.
$\overline{\text{BAUDOUT}}$	O	Baud Generator Output: 16X clock signal for the transmitter section of the UART, equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. May also be used for the receiver section by tying this output to the RCLK input of the chip.
NC	-	No Connection: These pins have no internal connection and may be left floating.
INTRPT	O	Interrupt: In the 28-pin versions of this chip, the INTRPT pin can be forced into a high impedance state by resetting to 0 the OUT2 bit (D3) of the Modem Control Register. INTRPT pin operation is enabled by setting the the OUT2 bit to 1.
XIN, XOUT	I/O	External System Clock: The XOUT pin is not available on the SSI 73M2450 and therefore must be driven by an external clock connected to the XIN pin.
µPRST	O	Microprocessor Reset: This output signal is used to provide a hardware reset to a local controller. This pin becomes active high when the MR pin is pulled high or the OUT1 bit (D2) of the Modem Control Register is set to 1. The µPRST function is available only on the SSI 73M2450.

TABLE 1: Control Register Address Table

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	Modem Control
X	1	0	1	Line Status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

TABLE 2: UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1 & 2 are low; bits 3-7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT1}}$	Master Reset	High
µPRST	Master Reset/set OUT1 bit	High during active Master Reset/OUT1 bit; low afterwards

CONTROL REGISTER OVERVIEW

			DATA BIT NUMBER							
REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB = 0	0	0	ENABLE SSI MODE	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB = X	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	011 DLAB = X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB = X	SSI MODE OSC OFF	0	0	LOOP	OUT2	OUT1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB = X	0	TRANSMITTER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB = X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB = X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. This register also allows access to the chip's special SSI mode which contains the oscillator disable function. It is possible to totally disable the interrupt system by resetting bits D0 through D3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

The chip's SSI mode can be activated by setting bit D5. Once in the SSI mode, the chip can be placed in a power shut-down state by setting bit D7 in the Modem Control Register.

BIT	NAME	COND.	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding	1	This bit enables the Transmitter Holding Register
	Register Empty		Empty Interrupt when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Interrupt when set to logic 1.
D4	Not used	0	Always logic 0.
D5	SSI Mode	0	Disables chip's SSI Mode; normal operation.
		1	Enables chip's SSI mode. In this mode, chip can be placed into power shut-down by setting bit D7 in modem control register.
D6-D7	Not used	0	Always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND.	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	N/A
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND.		DESCRIPTION
D0	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND.		DESCRIPTION
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		This is the Break Control bit. When set to a logic 1, the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit 6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - UA0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers.

BIT	NAME	COND.	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{\text{DTR}}$) output. When bit 0 is set to a logic 1, the $\overline{\text{DTR}}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{\text{DTR}}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{\text{RTS}}$) output. When bit 1 is set to a logic 1, the $\overline{\text{RTS}}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{\text{RTS}}$ output is forced to a logic 1.
D2	OUT1	1	This bit controls the Output 1 ($\overline{\text{OUT1}}$) signal, which is an auxiliary user-designated output. When bit 2 is set to a logic 1, the $\overline{\text{OUT1}}$ output is forced to a logic 0. When bit 2 is reset to a logic 0, the $\overline{\text{OUT1}}$ output is forced to a logic 1. On the SSI 73M2450 only, this bit controls the µPRST output. When bit D2 is set to a logic 1, the µPRST output is forced to a logic 1. When bit D2 is reset to logic 0, µPRST is forced to logic 0.
D3	OUT2	0	This bit controls the Output 2 ($\overline{\text{OUT2}}$) signal, which is an auxiliary user-designated output. When bit 3 is set to a logic 1, the $\overline{\text{OUT2}}$ output is forced to a logic 0. When bit 3 is reset to a logic 0, $\overline{\text{OUT2}}$ output is forced to a logic 1. On the 28-pin versions, this bit controls the INTRPT pin. When bit D3 is set to a logic 1, the INTRPT output is enabled. When bit D3 is reset to logic 0, the INTRPT pin is forced into a high impedance state.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{\text{CTS}}$, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$ and $\overline{\text{RI}}$) are disconnected; the four Modem Control outputs ($\overline{\text{DTR}}$, $\overline{\text{RTS}}$, $\overline{\text{OUT1}}$ and $\overline{\text{OUT2}}$) are internally connected to the four Modem Control inputs, and the Modem Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D6		0	These bits are permanently set to logic 0.
D7	SSi Mode Osc. off	1	This bit is active in the SSi Mode only. When D7 is set the UART oscillator is turned off placing the UART in a power shutdown state. All UART memory is retained during power shutdown.
		0	Resetting this bit enable the oscillator and powers up the UART.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits 1-4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND.	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading the data in the Receiver Buffer Register.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Regsiter into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character.
D7	-	0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition, four bits provide change information. Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register respectively.

BIT	NAME	COND.	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit indicates that the $\overline{\text{CTS}}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit indicates that the $\overline{\text{DSR}}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit indicates that the $\overline{\text{RI}}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{\text{DCD}}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{\text{CTS}}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{\text{DSR}}$) input. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{\text{RI}}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{\text{DCD}}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 4 MHz) and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)/(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

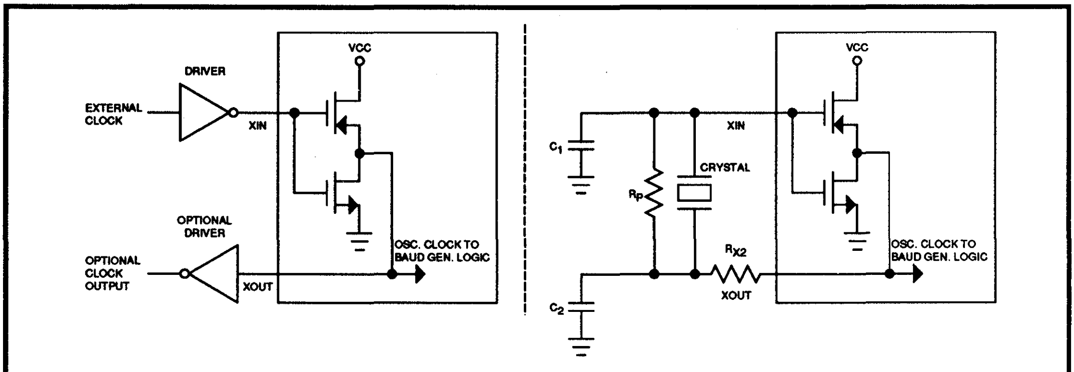
Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

TABLE 3: Baud Rates Using 1.8432 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 4: Baud Rates Using 3.072 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-



NOTE: R_p function is to bias the crystal; RX_2 function is to lower power and reduce crystal overdrive.

FIGURE 1: Typical Clock Circuits

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
1.8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF
4 MHz	1 MΩ	0	10-30 pF	40-60 pF

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+7V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to Vcc + 0.3

DC CHARACTERISTICS

(TA = –40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		Vcc	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = 5.0 mA on all outputs except XOUT	2.4			V
ICC	Average Power Supply Current	See Note 1		5	10	mA
		See Note 2			50	µA
IIL	Input Leakage	VCC=5.25V, VSS=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, $\overline{\text{CTS}}$, $\overline{\text{RI}}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 KHz.

Note 2: VCC = 5.5V, TA = –40°C; No output load; CMOS-level inputs, XIN = Vcc

CAPACITANCE

(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2	Clock Input Capacitance			15	20	pF
CXTAL1	Clock Output Capacitance			20	30	pF
CI	Input Capacitance			6	10	pF
CO	Output Capacitance			10	20	pF

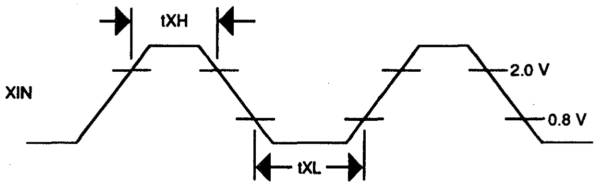
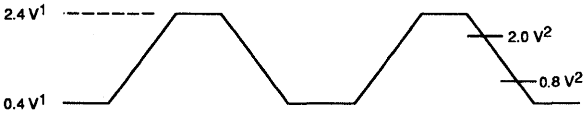


FIGURE 2: External Clock Input* (4 MHz Maximum)



[1] The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.
[2] The 2.0V and 0.8V levels are the voltages at which timing tests are made.

FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ±10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tADS	Address Strobe Width		60		ns
tAS	Address Setup Time		60		ns
tAH	Address Hold Time		0		ns
tCS	Chip Select Setup Time		60		ns
tCH	Chip Select Hold Time		0		ns
tCSC	Chip Select Output Delay from Select	100 pF load See Note 3		100	ns
tAR	READ Delay from Address		60		ns

READ & WRITE CYCLE (Continued)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tRD	READ Strobe Width		125		ns
tRC	Read Cycle Delay		175		ns
RC	Read Cycle	See Note 1	360		ns
tRDD	READ to Driver Disable Delay	100 pF load See Note 2		60	ns
tRVD	Delay from READ to Data	100 pF load		125	ns
tHZ	READ to Floating Data Delay	100 pF load See Note 2	0	100	ns
tRA	Address Hold Time from READ	See Note 3	20		ns
tAW	WRITE Delay from Address	See Note 3	60		ns
tWR	WRITE Strobe Width		100		ns
tWC	Write Cycle Delay		200		ns
WC	Write Cycle=tAW+tWR+tWC		360		ns
tDS	Data Setup Time		40		ns
tDH	Data Hold Time		40		ns
tWA	Address Hold Time from WRITE	See Note 3	20		ns
tMRW	Master Reset Pulse Width		5		µs
tXH	Duration of Clock High Pulse	External Clock (4 MHz max.)	100		ns
tXL	Duration of Clock Low Pulse	External Clock (4 MHz max.)	100		ns

Note 1: RC = tAR + tRD + tRC

Note 2: Charge and discharge time is determined by VOL, VOH and the external loading.

Note 3: Applicable only when $\overline{\text{ADS}}$ is tied low.

READ occurs when both read (RD, $\overline{\text{RD}}$) and chip select (CS0, CS1, $\overline{\text{CS2}}$, latched by $\overline{\text{ADS}}$) are asserted.

WRITE occurs when both write (WR, $\overline{\text{WR}}$) and chip select (CS0, CS1, $\overline{\text{CS2}}$, latched by $\overline{\text{ADS}}$) are asserted.

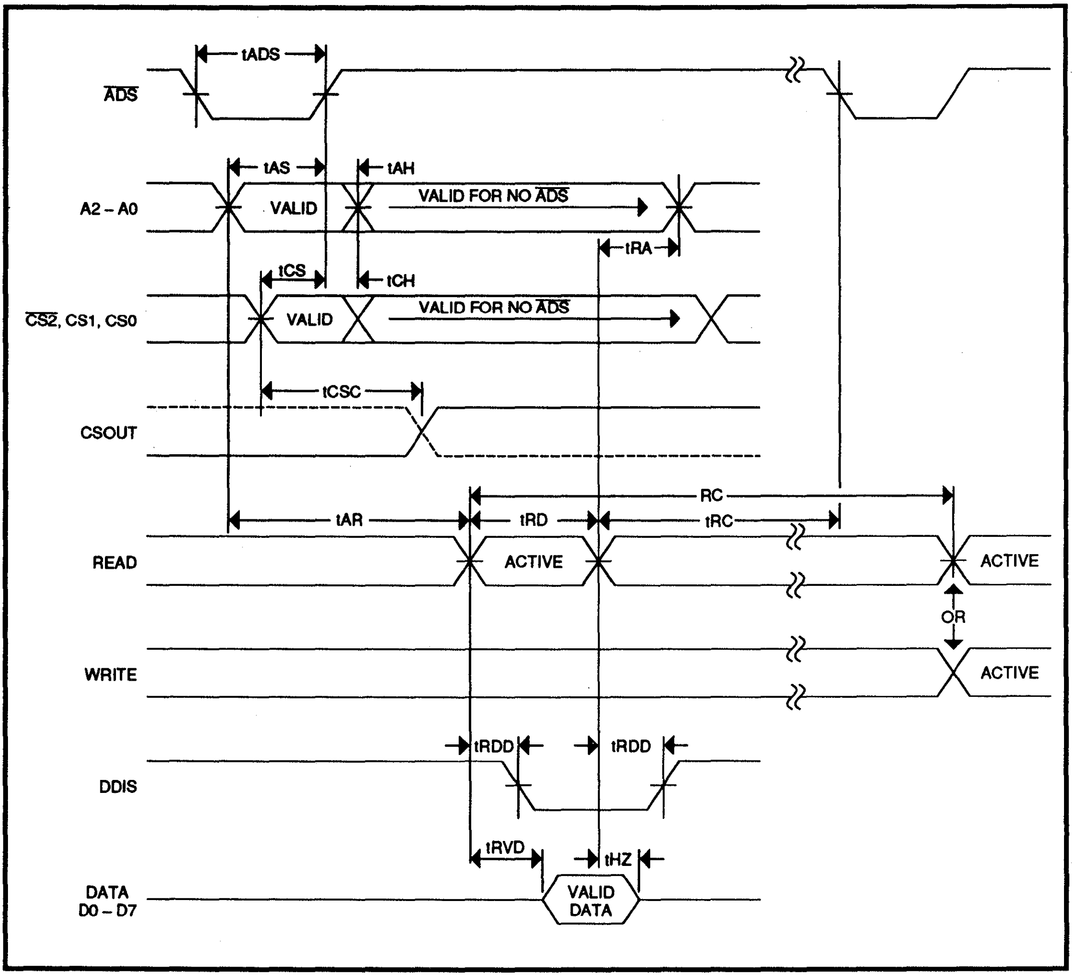


FIGURE 4: Read Cycle Timing

NOTE: READ occurs when both read (RD, $\overline{RD}$) and chip select (CS0, CS1, $\overline{CS2}$, latched by $\overline{ADS}$) are asserted.

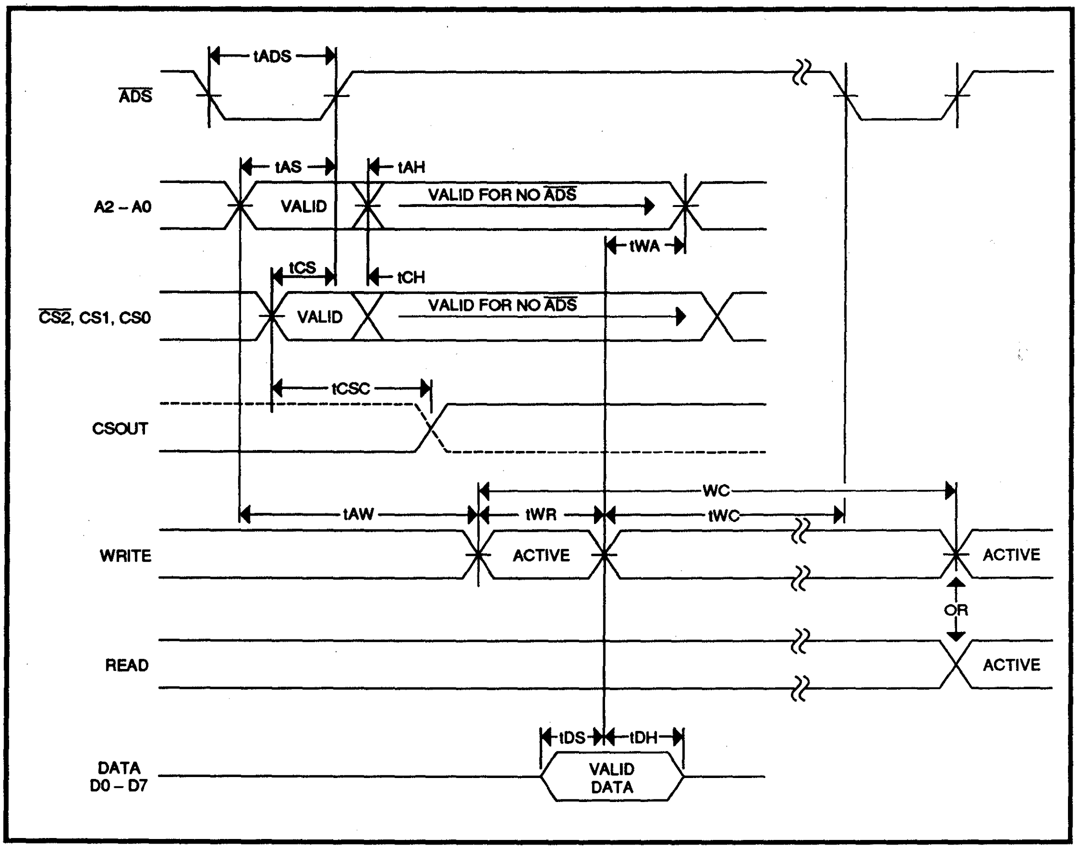


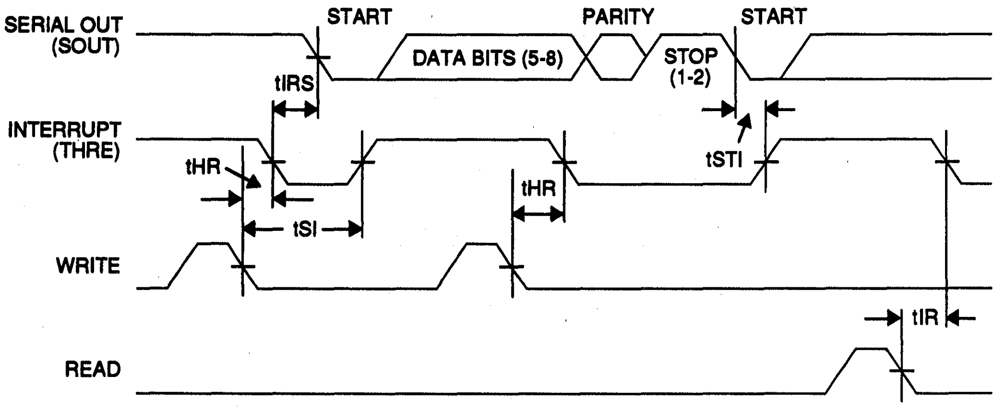
FIGURE 5: Write Cycle Timing

NOTE: WRITE occurs when both write (WR, $\overline{WR}$) and chip select (CS0, CS1, $\overline{CS2}$, latched by $\overline{ADS}$) are asserted.

AC CHARACTERISTICS (Continued)

TRANSMITTER (Refer to Figure 6.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from the end of WRITE to the negation of Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		24	40	BAUDOUT cycles
tSI	Delay from Initial Write to Interrupt		16	32	BAUDOUT cycles
tSTI	Delay from Stop to Interrupt (THRE)		8	8	BAUDOUT cycles
tIR	Delay from the end of READ to the negation of Interrupt	100 pF load		250	ns



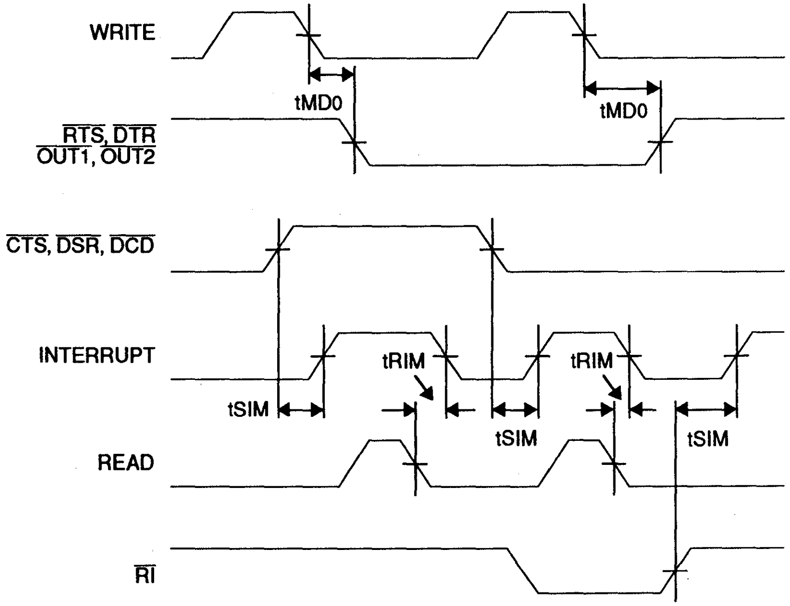
NOTES:
1. SEE WRITE CYCLE TIMING; WRITE IS A PRODUCT OF WR, $\overline{\text{WR}}$ AND CS0, CS1, $\overline{\text{CS2}}$
2. SEE READ CYCLE TIMING; READ IS A PRODUCT OF RD, $\overline{\text{RD}}$ AND CS0, CS1, $\overline{\text{CS2}}$

FIGURE 6: Transmitter Timing

AC CHARACTERISTICS (continued)

MODEM CONTROL (Refer to Figure 7.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from WRITE MCR to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Interrupt negation from READ	100 pF load		250	ns



NOTES:
1. SEE WRITE CYCLE TIMING; READ OCCURS WHEN BOTH READ (RD, $\overline{RD}$) AND CHIP SELECT (CS, CS1, $\overline{CS2}$, LATCHED BY $\overline{ADS}$) ARE ASSERTED.
2. SEE READ CYCLE TIMING; WRITE OCCURS WHEN BOTH WRITE (WR, $\overline{WR}$) AND CHIP SELECT (CS, CS1, $\overline{CS2}$, LATCHED BY $\overline{ADS}$) ARE ASSERTED.

FIGURE 7: Modem Controls Timing

AC CHARACTERISTICS (Continued)

BAUD GENERATOR (Refer to Figure 8.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
N	Baud Divisor		1	2^{16}-1	
tBLD	Baud Output Negative Edge Delay	100 pF load		125	ns
tBHD	Baud Output Positive Edge Delay	100 pF load		125	ns
tLW	Baud Output Down Time	fX=2 MHz, div. by 2, 100 pF load	425		ns
tHW	Baud Output Up Time	fX=3 MHz, div. by 3, 100 pF load	250		ns

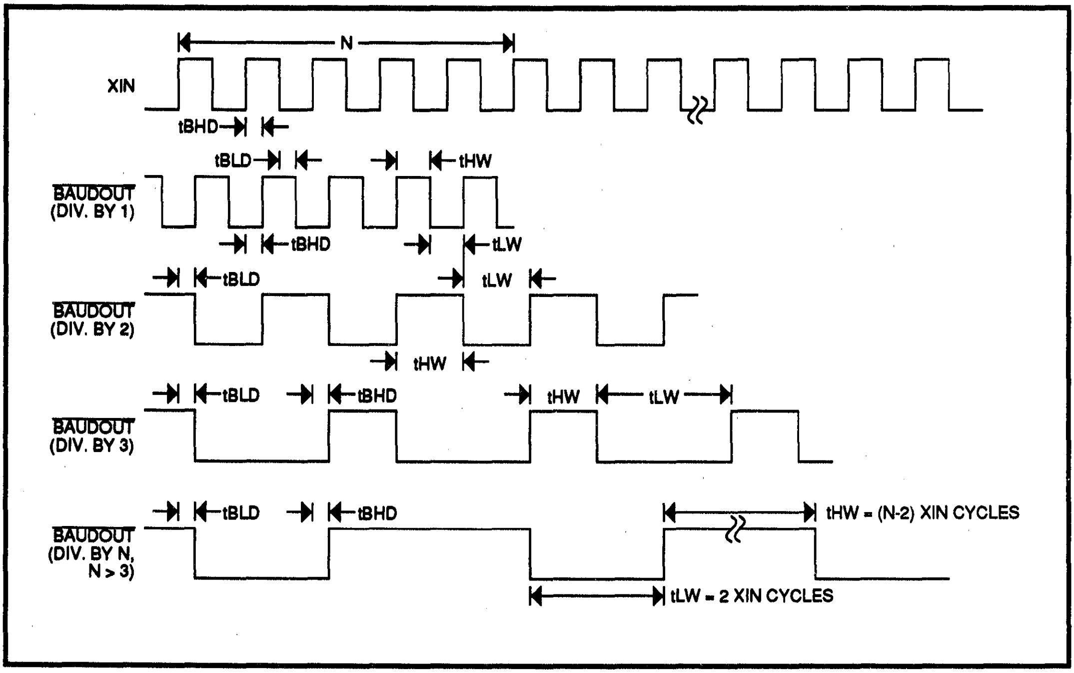
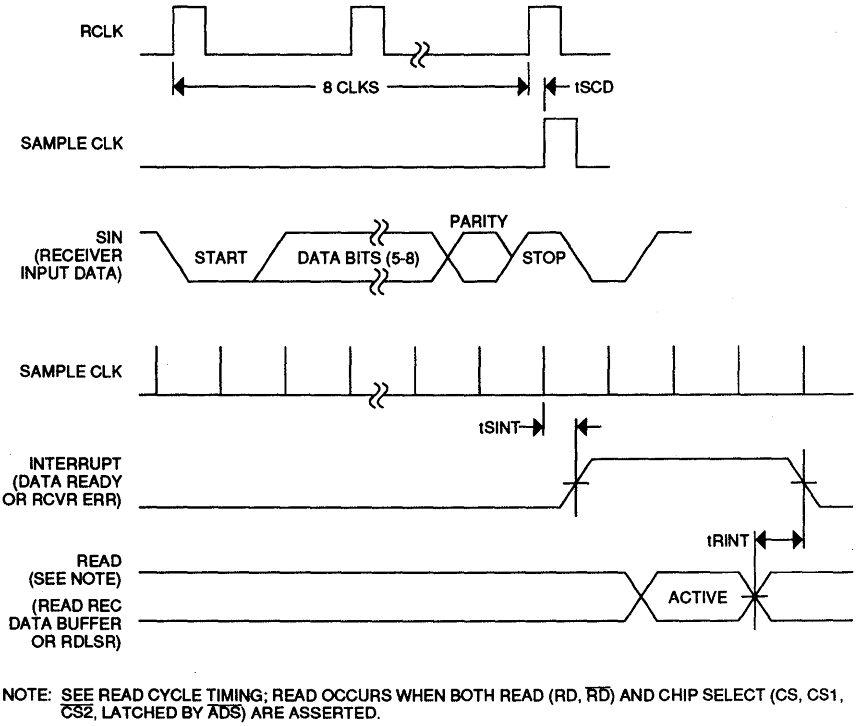


FIGURE 8: $\overline{\text{BAUDOUT}}$ Timing

AC CHARACTERISTICS (Continued)

RECEIVER (Refer to Figure 9.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt	RCLK=tXH & tXL		1	RCLK cycles
tRINT	Delay from READ (READ RBR, READ LSR to Interrupt negation	100 pF load		1	µs



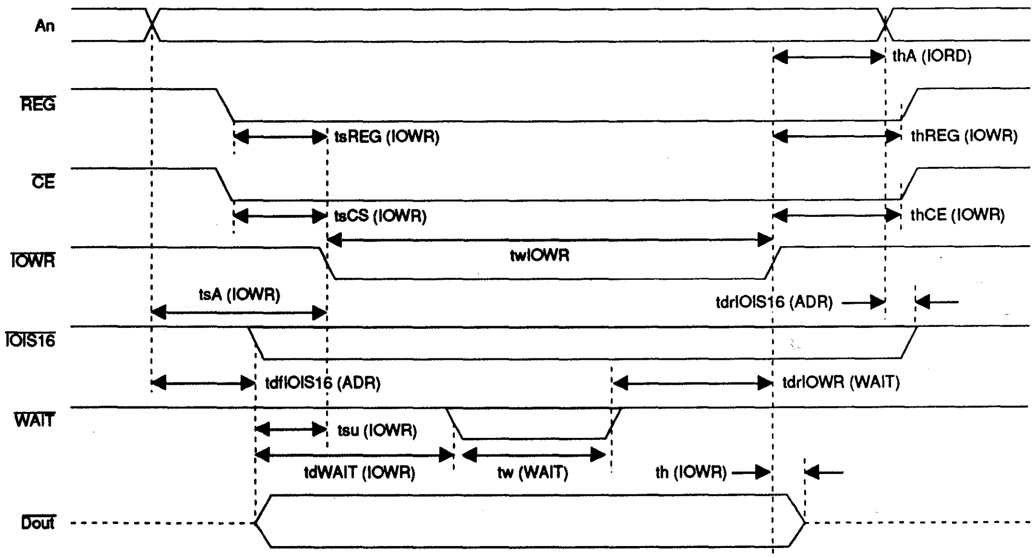
NOTE: SEE READ CYCLE TIMING; READ OCCURS WHEN BOTH READ (RD, $\overline{\text{RD}}$) AND CHIP SELECT (CS, CS1, $\overline{\text{CS2}}$, LATCHED BY $\overline{\text{ADS}}$) ARE ASSERTED.

FIGURE 9: Receiver Timing

SSI 73M450L TIMING COMPARED TO PCMCIA PC CARD STD. - RELEASE 2.0

					SSI 73M450L			
ITEM	**SYMBOL**	**IEEE**	**MIN**	**MAX**	**SSI**	**MIN**	**MAX**	**UNITS**
Data Setup before IOWR	t su (IOWR)	tDVIWL	60		TDS	30		ns
Data Hold following IOWR	t h (IOWR)	tIWHDX	30		TDH	30		ns
IOWR Width Time	t w IOWR	tIWLIWH	165		TWR	80		ns
Address Setup before IOWR	t su A (IOWR)	tAVIWL	70		TAW	30		ns
Address Hold following IOWR	t h A (IOWR)	tIWHAX	20		TWA	20		ns
CE Setup before IOWR	t su CE (IOWR)	tELIWL	5			Any		
CE Hold following IOWR	t h CE (IOWR)	tIWHEH	20			Any		
REG Setup before IOWR	t su REG (IOWR)	tRGLIWL	5					
REG Hold following IOWR	t h REG (IOWR)	tIWHRGH	0					
IOIS16 Delay Falling from Address	t d IOIS16 $(ADR)_1$	tAVISL		35				
IOIS16 Delay Rising from Address	t d IOIS16 $(ADR)_2$	tAVISH		35				
Wait Delay Falling from IOWR	t d WAIT (IOWR)	tIWLWTL		35				
Wait Width Time	t w WAIT	tWLWTH		12,000				
NOTE: The maximum load on WAIT, INPACK and IOIS16 are 1 LSTTL with 50 pF total load.								

TABLE 5: I/O Output (WRITE) Timing Specification for All 5V I/O Cards



All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design

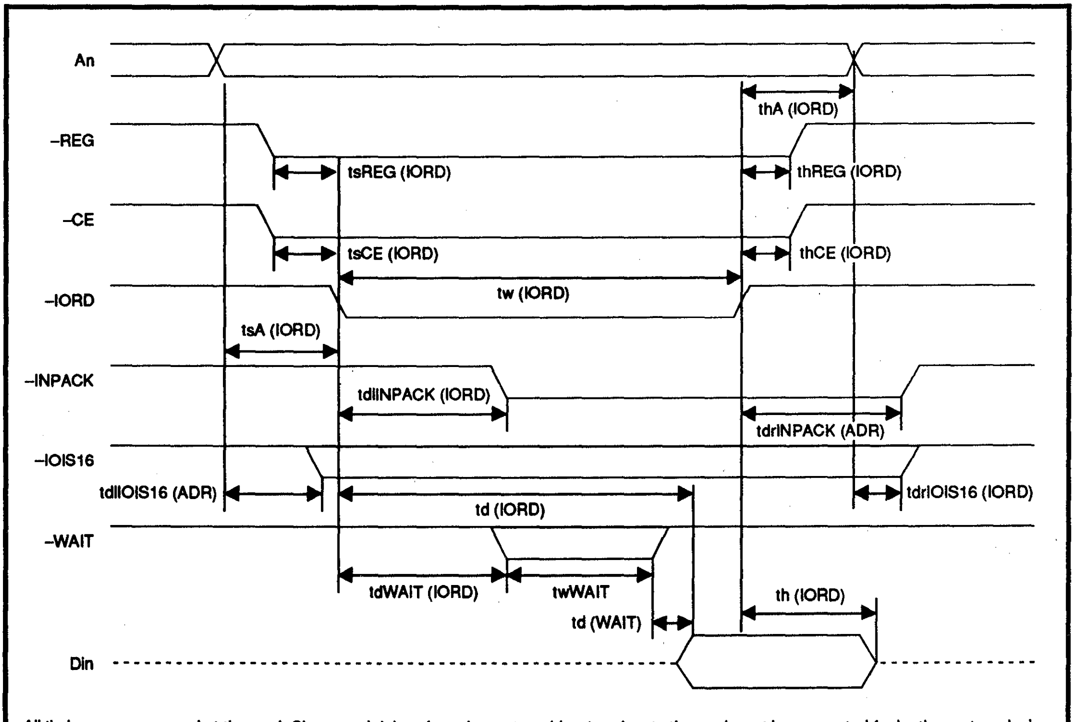
FIGURE 10: I/O Output Timing Specification (WRITE)

SSI 73M450L TIMING COMPARED TO PCMCIA PC CARD STD. - RELEASE 2.0

ITEM	SYMBOL	IEEE	MIN	MAX	SSI 73M450L SSI	SSI 73M450L MIN	SSI 73M450L MAX	SSI 73M450L UNITS
Data Delay after IORD	t d (IORD)	tIGLQV		100	TRVD		80	ns
Data Hold following IORD	t h (IORD)	tIGHQX	0		THZ	0		ns
IORD Width Time	t w IORD	tIGLIGH	165		TRD	80		ns
Address Setup before IORD	t su A (IORD)	tAVIGL	70		TAR	30		ns
Address Hold following IORD	t h A (IORD)	tIGHAX	20		TRA	20		ns
CE Setup before IORD	t su CE (IORD)	tELIGL	5			Any		
CE Hold following IORD	t h CE (IORD)	tIGHEH	20			Any		
REG Setup before IORD	t su REG (IORD)	tRGLIGL	5					
REG Hold following IORD	t h REG (IORD)	tIGHRGH	0					
INPACK Delay Falling from IORD	t d INPACK (IORD)	tGLIAL	0	45				
INPACK Delay Rising from IORD	t d INPACK (IORD)	tIGHIAH		45				
IOIS16 Delay Falling from Address	t d IOIS16 $(ADR)_1$	tAVISL		35				
IOIS16 Delay Rising from Address	t d IOIS16 $(ADR)_2$	tAVISH		35				
Wait Delay Falling from IORD	t d WAIT (IORD)	tIGLWTL		35				
Data Delay from Wait Rising	td(WAIT)	tWTHQV		35				
Wait Width Time	t w WAIT	tWLWTH		12,000				

NOTE: The maximum load on WAIT, INPACK and IOIS16 are 1 LSTTL with 50 pF total load.

TABLE 6: I/O Output (READ) Timing Specification for All 5V I/O Cards



All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design

FIGURE 11: I/O Output Timing Specification (READ)

APPLICATIONS INFORMATION

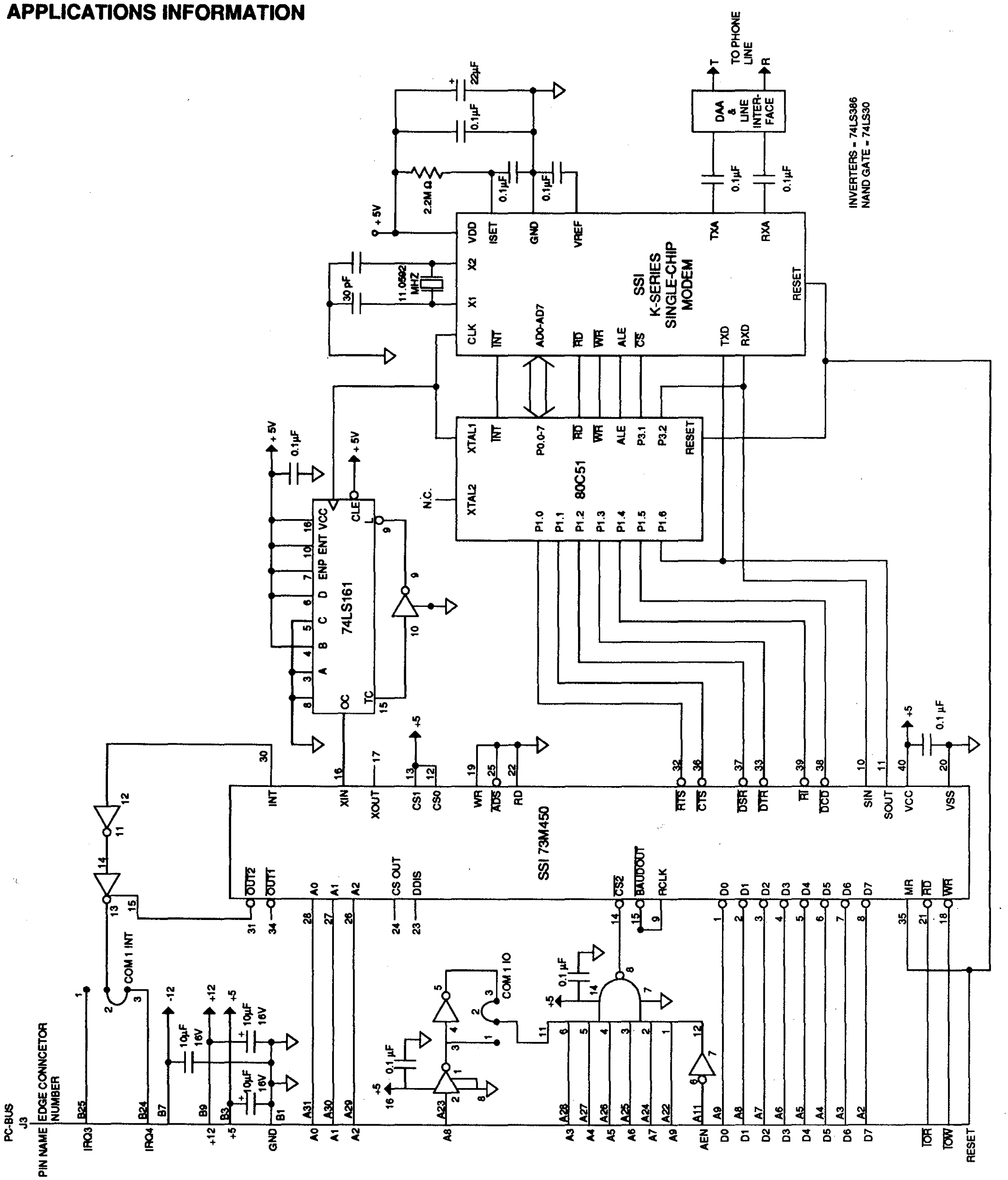
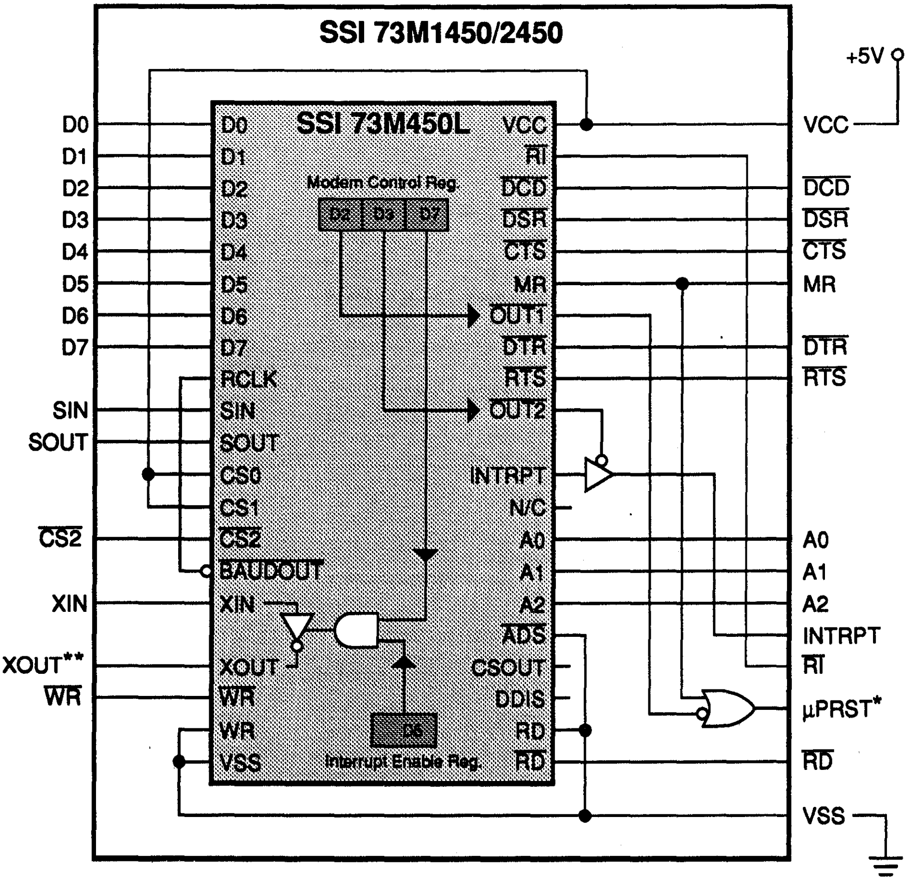


FIGURE 12: Typical Application showing Modem Interface to PC-Bus via SSI 73M450 UART

APPLICATIONS INFORMATION (continued)

28-PIN VERSION

The 73M450L is available in two 28-pin configurations: SSI 73M1450 and SSI 73M2450. The relation between these two products and the 40-pin version is shown in the accompanying diagram. Note that the only difference between the 73M1450 and 73M2450 is that the 73M2450 adds the µPRST pin at the expense of the XOUT pin.



*SSI 73M2450 only.
**SSI 73M1450 only.

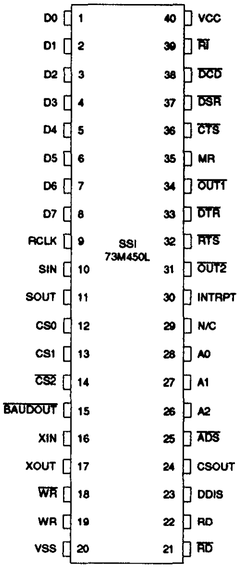
FIGURE 13: Adapter Diagram Showing Internal Connections and Bond-outs from 40-pin to 28-pin Packages

SSI 73M450L/1450/2450
Universal Asynchronous Receiver/Transmitter

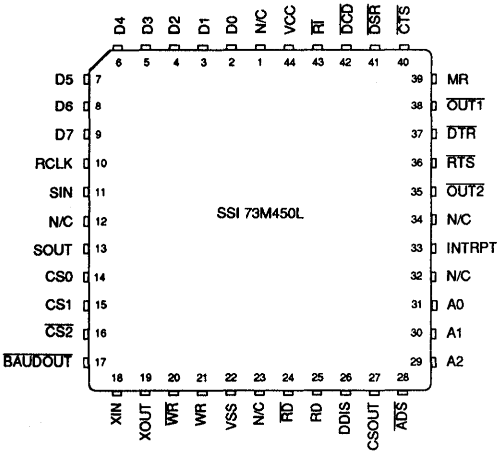
PACKAGE PIN DESIGNATIONS

(Top View)

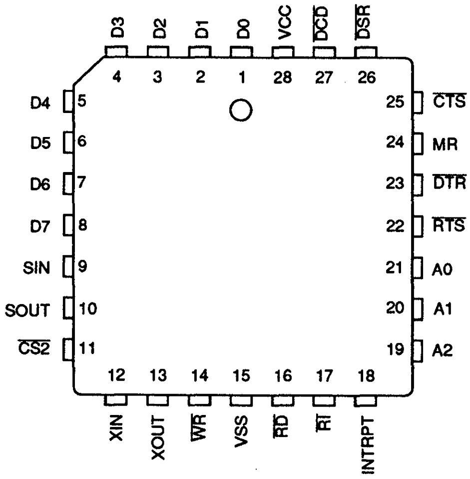
CAUTION: Use handling procedures necessary for a static sensitive component.



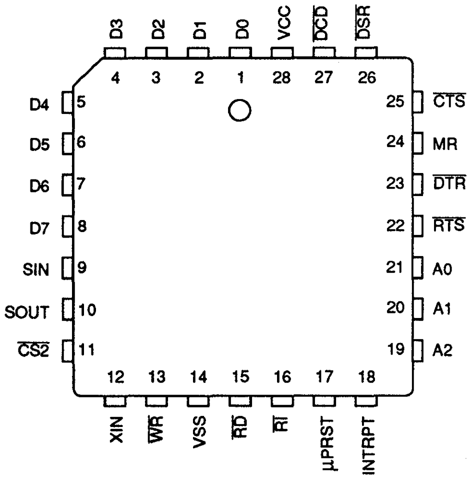
SSI 73M450L 40-Pin DIP



SSI 73M450L 44-Pin PLCC



SSI 73M1450 UART
28-Pin PLCC



SSI 73M2450 UART
28-Pin PLCC

SSI 73M450L/1450/2450
Universal Asynchronous Receiver/Transmitter

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 73M450L	40-pin PDIP	73M450L-IP	73M450-IP
	44-pin PLCC	73M450L-IH	73M450-IH
SSI 73M1450	28-pin PLCC	73M1450-IH	73M1450-IH
SSI 73M2450	28-pin PLCC	73M2450-IH	73M2450-IH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 73M550
SSI 73M1550/2550
UART with FIFOs

January 1993

DESCRIPTION

The SSI 73M550 is a Universal Asynchronous Receiver/Transmitter (UART) with receive and transmit FIFO buffers. The 16-byte FIFO registers are active during the FIFO mode, allowing the UART to reduce CPU overhead and accommodate Direct Memory Access (DMA) transfers. This mode is supported by interrupt functions and selectable interrupt trigger levels in both the RCVR and TXMR FIFO.

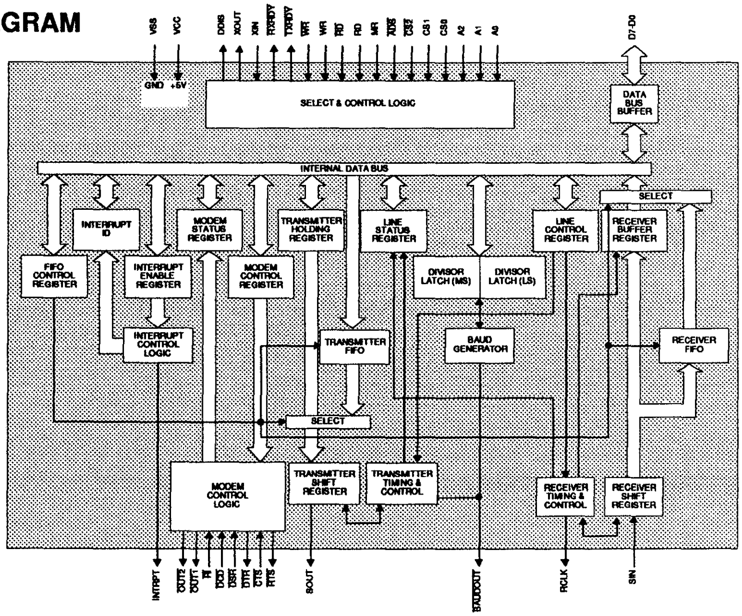
The 73M550 is functionally identical to the SSI 73M450L in the CHARACTER mode. Pins 24 (CSOUT) and 29 (NC) of the 73M450L have been replaced by TXRDY and RXRDY, respectively, on the 73M550. The chip is automatically put into the CHARACTER mode upon power-up, and subsequent mode changes are accomplished via software control.

The 73M1550 and 73M2550 are 28-pin versions of the 73M550. The difference between these versions is that 73M2550 adds a µPRST pin at the expense of the XOUT pin. See Figure 17 on page 32 for detail. These products require a single 5V supply.

FEATURES

- **16 bytes of receive and transmit FIFO buffering available in FIFO mode reduces CPU overhead**
- **Supports DMA transfers with TXRDY and RXRDY pins**
- **High-speed timing for zero wait-state operation is compatible with PCMCIA interface**
- **Oscillator disable allows a static low-power state**
- **Bit-programmable high impedance state of INTRPT pin**
- **High drive current for directly driving large loads**
- **Full double buffering**
- **Independent control transmit, receive, line status and data set interrupts**
- **Contains modem control functions including CTS, RTS, DSR, DTR, RI and DCD**
- **Available in 40-pin DIP, 44-and 28-pin PLCC, 48-lead TQFP (73M550) and 52-lead QFP (73M2550) packages**
- **CMOS design for low-power operation**

BLOCK DIAGRAM



PIN DESCRIPTION

BUS INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{ADS}$	I	Address Strobe: The rising edge of this signal is used for latching the Register Address and Chip Select inputs, thus facilitating interface to a multiplexed Address/Data bus. $\overline{ADS}$ is also required when register address signals (A2, A1, A0) are not stable for the duration of the read or write cycle. If not required, $\overline{ADS}$ should be tied permanently low.
CS0, CS1, $\overline{CS2}$	I	Chip Select: The UART is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Chip selection is complete when the decoded chip select signal is latched with the rising edge of an active (low) $\overline{ADS}$ input. This enables communication between the UART and the CPU. If $\overline{ADS}$ is permanently low, then chip select should be stabilized for the duration of the tCSW parameter.
A0-A2	I	Register Select Address: These pins determine which of the UART registers is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit in the UART's Line Control Register (see Table 1) also controls which register is referenced.
RD, $\overline{RD}$	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling RD high or $\overline{RD}$ low while the chip is selected. Since only one input is required for a read, tie either RD permanently low or $\overline{RD}$ permanently high if not used.
WR, $\overline{WR}$	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling WR high or $\overline{WR}$ low while the chip is selected. Since only one input is required for a write, tie either WR permanently low or $\overline{WR}$ permanently high if not used.
D0-D7	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data control words and status information are transferred via this bus.
$\overline{TXRDY}$	I/O	Transmitter Ready Signal for DMA Transfer: Remains low as long as XMIT FIFO is not completely full. In FIFO mode, DMA transfer modes 0 and 1 are allowed. In the character mode, only DMA transfer mode 0 is allowed. DMA mode 0 supports single DMA transfer mode between CPU bus cycles. DMA mode 1 supports multiple DMA transfers until the XMIT FIFO has been filled.
$\overline{RXRDY}$	O	Receiver Ready Signal for DMA Transfer: Remains low until RCVR FIFO has been emptied. In FIFO mode DMA transfer modes 0 and 1 are allowed. In the character mode only DMA mode 0 is allowed. DMA mode 0 supports single DMA transfer made between CPU bus cycles. DMA mode 1 supports multiple DMA transfers until the RCVR FIFO has been emptied.
DDIS	O	Driver Disable: Goes low when the CPU is reading data from the UART. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and UART on the D0-D7 Data Bus) at all times, except when the CPU is reading data.

BUS INTERFACE (Continued)

NAME	TYPE	DESCRIPTION
INTRPT	O	Interrupt: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag, Received Data Available; Timeout (FIFO mode only); Transmitter Holding Register Empty and Modem Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

DATA I/O

SIN	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

$\overline{\text{RTS}}$	O	Request To Send: This output is programmed by $\overline{\text{RTS}}$ bit (D1) of the Modem Control Register and represents the compliment of that bit. I is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{\text{CTS}}$	I	Clear To Send: A modem status input whose condition corresponds to the complement of the CTS bit (D4) of the Modem Status Register. When $\overline{\text{CTS}}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{\text{DTR}}$	O	Data Terminal Ready: This output is programmed by DTR bit (D0) of the Modem Control Register, and represents the compliment of that bit. It is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{\text{DSR}}$	I	Data Set Ready: A modem status input whose condition is complimented and reflected in the DSR bit (D5) of the Modem Status Register. When $\overline{\text{DSR}}$ is low, it indicates that the modem is ready to establish communications.
$\overline{\text{DCD}}$	I	Data Carrier Detect: A modem status input whose condition is complemented and reflected in the DCD bit (D7) of the Modem Status Register. When $\overline{\text{DCD}}$ is low, it indicates that the modem is receiving a carrier.
$\overline{\text{RI}}$	I	Ring Indicator: A modem status input whose condition is complimented and reflected in the RI bit (D6) of the Modem Status Register. When $\overline{\text{RI}}$ is low, it indicates that a telephone ringing signal is being received.
$\overline{\text{OUT1}}$ $\overline{\text{OUT2}}$	O O	Output 1, 2: User designated outputs that can be set to an active low by setting bit 2 ($\overline{\text{OUT1}}$) or bit 3 ($\overline{\text{OUT2}}$) of the Modem Control Register high. These output signals are set high upon Master Reset or during loop mode operation.

GENERAL & CLOCKS

NAME	TYPE	DESCRIPTION
VCC	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to VSS.
VSS	I	System Ground
MR	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{\text{OUT1}}$, $\overline{\text{OUT2}}$, $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger. See Table 2.
XIN, XOUT	I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source.
RCLK	I	Receiver Clock: This input is the 16X baud rate clock for the receiver section of the chip.
$\overline{\text{BAUDOUT}}$	O	Baud Generator Output: 16X clock signal for the transmitter section of the UART. The clock is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. May also be used for the receiver section by tying this output to the RCLK input of the chip.
N/C	-	No Connection: These pins have no internal connection and may be left floating.

28-PIN VERSION, SPECIAL PINS

INTRPT	O	Interrupt: In the 28-pin versions of this chip, the INTRPT pin can be forced into a high impedance state by resetting to 0 the OUT2 bit (D3) of the Modem Control Register. INTRPT pin operation is enabled by setting the OUT2 bit to 1.
XIN, XOUT	I/O	External System Clock: The XOUT pin is not available on the 73M2550 and therefore must be driven by an external clock connected to the XIN pin.
µPRST	O	Microprocessor Reset: This output signal is used to provide a hardware reset to a local controller. This pin becomes active high when the MR pin is pulled high or the OUT1 bit (D2) of the Modem Control Register is set to 1. The µPRST function is available only on the 73M2550.

TABLE 1: Control Register Address Table

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control
X	1	0	0	Modem Control
X	1	0	1	Line Status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

TABLE 2: UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 & 5 forced and 4, 6 & 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1, 2, 3, 6 & 7 are low; bits 4 & 5 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low (bits 5, 6 & 7 permanent)
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT1}}$	Master Reset	High
FIFO Control Register	Master Reset	All bits low
RCVR FIFO	MR/FCR1 and FCR0/ΔFCR0	All bits low
XMIT FIFO	MR/FCR2 and FCR0/ΔFCR0	All bits low

CONTROL REGISTER OVERVIEW

			DATA BIT NUMBER							
REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB=0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB=0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB=0	0	0	ENABLE SSI MODE (NOTE 1)	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB=X	FIFOs ENABLED (NOTE 1)	FIFOs ENABLED (NOTE 1)	SSI MODE RXRDY FOR DMA	SSI MODE TXRDY FOR DMA	INTERRUPT ID BIT 2 (NOTE 1)	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
FIFO CONTROL REGISTER (WRITE ONLY)	FCR	010 DLAB=X	RCVR TRIGGER (MSB)	RCVR TRIGGER (LSB)	SSI MODE XMIT TRIGGER (MSB)	SSI MODE XMIT TRIGGER (LSB)	DMA MODE SELECT	XMIT FIFO RESET	RCVR FIFO RESET	FIFO ENABLE
LINE CONTROL REGISTER	LCR	011 DLAB=X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB=X	SSI MODE OSC OFF	0	0	LOOP	OUT 2	OUT 1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB=X	ERROR IN RCVR FIFO (NOTE 1)	TRANS-MITTER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB=X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB=X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLL	000 DLAB=1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB=1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

NOTE 1: THESE BITS ARE RESET TO 0 IN THE 73M450 MODE (Character Mode)

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the five types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

The chip's SSi mode can be activated by setting bit D5. Once in the SSi mode, the chip can be placed in a power shut-down state by setting bit D7 in the Modem Control Register.

BIT	NAME	COND	DESCRIPTION
D0	Received Data	1	When set to logic 1 this bit enables the Received Data Available Interrupt, and timeout interrupts in FIFO mode.
D1	Transmitter Holding Register Empty	1	When set to logic 1 this bit enables the Transmitter Holding Register Empty Interrupt.
D2	Receiver Line Status Interrupt	1	When set to logic 1 this bit enables the Receiver Line Status Interrupt.
D3	Modem Status	1	When set to logic 1 this bit enables the Modem Status Interrupt.
D4	Not Used	0	This bit are is always logic 0.
D5	SSI Mode	1	When set to logic 1, this bit enables the SSi Mode. In the SSi Mode the oscillator can be turned off via bit D7 in the Modem Control Register, and the XMIT THRE interrupt trigger set via bits D4 & D5 of the FIFO Control Register.
D6-D7	Not used	0	These two bits are always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions and also allows for DMA transfer operations in a polled FIFO manner under the SSi mode. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a prioritized interrupt or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2 D3	Interrupt ID bits 0, 1, 2	See table Page 10	These three bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table. Bit D3 is reset to 0 when FIFO mode is disabled.
D4	SSI mode TXRDY for DMA	1	This bit function is available only when SSi mode is enabled (bit D5 in IER is set). This bit is the compliment of $\overline{\text{TXRDY}}$ pin and is used to support DMA transfers in a polled environment. A logic 1 indicates transmitter is less than full and is ready for DMA transfer.
		0	A logic 0 indicates transmitter is full and not ready for DMA transfer. Also when SSI mode is disabled this bit will be reset to 0.
D5	SSI mode RXRDY for DMA	1	This bit function is available only when SSi mode is enabled (bit D5 in IER is set). This bit is the compliment of $\overline{\text{RXRDY}}$ pin and is used to support DMA transfers in a polled environment. A logic 1 indicates receiver is not empty and is ready for DMA transfer.
		0	A logic 0 indicates receiver is empty and not ready for DMA transfer. Also when SSi mode is disabled this bit will be reset to 0.
D6, D7	FIFOs enabled	1	These two bits are set to logic 1 when bit D0 in FCR is set to 1 (FIFO mode enabled).
		0	These two bits are reset to logic 0 when bit D0 in FCR is reset to 0 (FIFO mode disabled).

INTERRUPT PRIORITY TABLE

D3	D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	0	1	–	None	None	N/A
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Receive Data Available	Receive Data Available or RCVR FIFO trigger level reached	Reading the Receiver Buffer Register or the RCVR FIFO drops below trigger level
1	1	0	0	Second	Character Timeout Indicator	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty or below XMIT FIFO trigger level	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register or XMIT FIFO trigger level reached
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the Modem Status Register

FIFO CONTROL REGISTER (FCR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 010

This is a write only register at the same location as the IIR read only Register. This register is used to enable the FIFOs, clear the FIFOs, set the XMIT and RCVR FIFO trigger level, and select the type of DMA signalling.

BIT	NAME	COND	DESCRIPTION
D0	FIFO Enable	1	Setting this bit to logic 1 enables both XMIT and RCVR FIFOs. This bit must be written as 1 when other FCR bits are written to or they will not be programmed.
		0	Resetting this bit to logic 0 disables the FIFO mode (enables the 73M450 mode) and clears data in both FIFOs when changing from FIFO mode to 73M450 mode and vice versa, data is automatically cleared from FIFOs.
D1	RCVR FIFO Reset	1	Setting this bit to logic 1 clears all data in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The logic 1 written into this bit is self clearing.
D2	XMIT FIFO Reset	1	Setting this bit to logic 1 clears all data in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The logic 1 written into this bit is self clearing.

FIFO CONTROL REGISTER (FCR) (WRITE ONLY) (Continued)

BIT	NAME	COND	DESCRIPTION
D3	DMA Mode Select	1	Setting this bit to logic 1 will enable DMA mode 1. In this mode pins $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ and bits D4 and D5 in IIR, support multiple DMA transfers.
		0	Resetting this bit to logic 0 will enable DMA mode 0. In this mode, pins $\overline{\text{TXRDY}}$ and $\overline{\text{RXRDY}}$ and bits D4 and D5 in IIR support single DMA transfers.
D5, D4	SSI Mode XMIT Trigger (MSB, LSB)	0/1	These two bits are active in the SSi mode only. The value written into D5 and D4 determine the XMIT FIFO trigger level as described in table below. The THRE interrupt will occur if the XMIT FIFO is below the trigger level and will reset when the XMIT FIFO is filled to trigger level.
D7, D6	RCVR Trigger (MSB, LSB)	0/1	The value written into D7 and D6 determining the RCVR FIFO trigger level as described in table below. The received data available interrupt will occur if the RCVR FIFO is filled to or above the trigger level and will reset when the RCVR FIFO drops below the trigger level.

D5	D4	XMIT FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

D7	D6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND		DESCRIPTION
D0/D1	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit D2 is a logic 0, one stop bit is generated in the transmitted data. If bit D2 is a logic 1 when a 5-bit word length is selected via bits D0 and D1, one-and-a-half stop bits are generated. If bit D2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit D3 is a logic 1 and bit D4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit D3 is a logic 1 and bit D4 is a logic 1 an even number of logic 1's is transmitted or checked.
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit D3 is a logic 1 and bit D5 is a logic 1 the parity bit is transmitted and checked by the receiver as a logic 0 if bit D4 is a logic 1 or as a logic 1 if bit D4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND	DESCRIPTION
D6	Set Break	1	This is the Break Control bit. It causes a break condition to be sent to the receiving UART. When set to a logic 1 the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit D6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1	The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - A0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device.

BIT	NAME	COND	DESCRIPTION
D0	DTR	0/1	This bit controls the Data Terminal Ready ($\overline{\text{DTR}}$) output. When bit 0 is set to a logic 1 the $\overline{\text{DTR}}$ output is forced to a logic 0. When bit 0 is reset to a logic 0 the $\overline{\text{DTR}}$ output is forced to a logic 1.
D1	RTS	0/1	This bit controls the Request to Send ($\overline{\text{RTS}}$) output. When bit 1 is set to a logic 1 the $\overline{\text{RTS}}$ output is forced to a logic 0. When bit 1 is reset to a logic 0 the $\overline{\text{RTS}}$ output is forced to a logic 1.
D2	OUT1	0/1	This bit controls the Output 1 ($\overline{\text{OUT1}}$) signal, an auxiliary user-designated output. When bit D2 is set to a logic 1, $\overline{\text{OUT1}}$ is forced to a logic 0. When bit D2 is reset to a logic 0, $\overline{\text{OUT1}}$ is forced to a logic 1. On the SSI 73M2550 only, this bit controls the µPRST output. When bit D2 is set to a logic 1, the µPRST output is forced to a logic 1. When bit D2 is reset to logic 0, µPRST is forced to logic 0.
D3	OUT2	0/1	This bit controls the Output 2 ($\overline{\text{OUT2}}$) signal, an auxiliary user-designated output. When bit D3 is set to a logic 1, $\overline{\text{OUT2}}$ forced to a logic 0. When bit D3 is reset to a logic 0, $\overline{\text{OUT2}}$ output is forced to a logic 1. On the 28-pin versions, this bit controls the INTRPT pin. When bit D3 is set to a logic 1, the INTRPT output is enabled. When bit D3 is reset to logic 0, the INTRPT pin is forced into a high impedance state.

MODEM CONTROL REGISTER (MCR) (Continued)

BIT	NAME	COND	DESCRIPTION
D4	LOOP	0/1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected; the four Modem Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four Modem Control inputs, and the Modem Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D6		0	These bits are permanently set to logic 0.
D7	SSi Mode Osc. off	1	This bit is active in the SSi Mode only. When D7 is set the UART oscillator is tunred off placing the UART in a power shutdown state. All UART memory is retained during power shutdown.
		0	Resetting this bit enable the oscillator and powers up the UART.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits D1-D4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND	DESCRIPTION
D0	DR	0/1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading all data in the Receiver Buffer Register FIFO.
D1	OE	0/1	The Overrun Error (OE) bit is set when data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register. In FIFO mode if data continues to fill the FIFO beyond the trigger level an overrun error will occur only after the FIFO is full and the next character has been completely received in (Continued)

LINE STATUS REGISTER (LSR) (Continued)

BIT	NAME	COND	DESCRIPTION
D1	OE	0/1	the shift register. OE is indicated to the CPU as soon as it occurs. The character in the shift register is overwritten but it is not transferred to the FIFO.
D2	PE	0/1	The Parity Error (PE) bit is set when the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register. In FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples the following start bit twice and then takes in the data that follows.
D4	BI	1	The Break Interrupt (BI) bit is set when a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register. In the FIFO mode this error is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking (high) state and receives the next valid start bit.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Register into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is filled below the trigger level and will reset when the FIFO is filled to the trigger level.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character. In the FIFO mode this bit is set whenever the XMIT FIFO and the transmitter shift register are both empty.
D7	Error in Rcvr FIFO	0	In the character mode this bit is reset to 0. In the FIFO mode this bit is set when there is at least one parity error, framing error or break indication in the FIFO. This bit is reset when the CPU reads the Line Status Register if there are no subsequent errors in the FIFO.

Note: Bits D1-D4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition four bits provide change information. Whenever bit D0, D1, D2 or D3 is set to logic 1 a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register, respectively.

BIT	NAME	COND	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit is set when the $\overline{\text{CTS}}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit is set when the $\overline{\text{DSR}}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit is set when the $\overline{\text{RI}}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{\text{DCD}}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{\text{CTS}}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{\text{DSR}}$) input. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{\text{RI}}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{\text{DCD}}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 8 MHz) and dividing it by any divisor from 2 to 2^{16}-1. 4 MHz is the highest input clock frequency recommended when the divisor = 1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)/(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3, 4 and 5 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz, 3.072 MHz, and 8 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

TABLE 3: Baud Rates using 1.8432 MHZ Crystal

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

TABLE 4: Baud Rates using 3.072 MHZ Crystal

DESIRED BAUD RATE (BIT RATE CLOCK)	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344

TABLE 5: Baud Rates using 8 MHZ Crystal

FIFO INTERRUPT MODE OPERATION

When the RCVR FIFO and receiver interrupts are enabled (FCR D0 = 1, IER D0 = 1) RCVR interrupts will occur as follows:

A. The receive data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

B. The IIR receive data available indication also occurs when the FIFO trigger level is reached and like the interrupt it is cleared when the FIFO drops below the trigger level.

C. The receiver line status interrupt (IIR = 06), as before, has higher priority than the received data available (IIR = 04) interrupt.

D. The data ready bit (LSRD0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A FIFO timeout interrupt will occur, if the following conditions exist:
   - at least one character is in the FIFO
   - the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).
   - the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with a 12 bit character.

B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCRD0 = 1, IERD1 = 1), XMIT interrupts will occur as follows:

A. The transmitter holding register interrupt occurs when the XMIT FIFO is below the trigger level. It is cleared as soon as the transmitter holding register is written to and reaches the trigger level or the IIR is read. If the SSi mode is disabled (IER D5 = 0) then the XMIT FIFO trigger level is set to 1 byte.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenver the folowing occurs: THRE =1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR D0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO MODE OPERATION

With FCR D0 = 1 resetting IER D0, IER D1, IER D2, IER D3 or all to zero puts the UART in the FIFO polled mode of operation. Since the RCVR and XMITTER are controlled separately either one or both can be in the polled mode of operation. In this mode the users program will check RCVR and XMITTER status via the LSR. As stated previously:

LSR D0 will be set as long as there is one byte in the RCVR FIFO

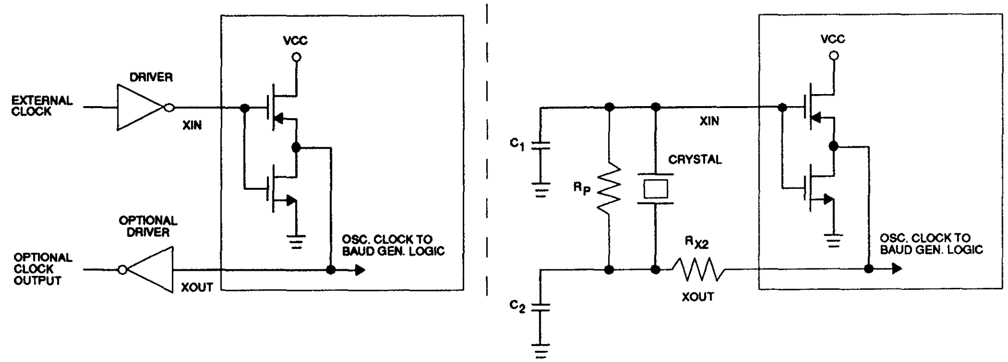
LSR D1 to LSR D4 will specify which error(s) has occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since IER D2 = 0

LSR D5 will indicate when the XMIT FIFO is empty.

LSR D6 will indicate that both the XMIT FIFO and shift register are empty.

LSR D7 will indicate whether there are any errors in the RVCR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.



NOTE: R_p function is to bias the crystal; RX_2 function is to lower power and reduce crystal overdrive.

FIGURE 1: Typical Clock Circuits

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
1.8 - 8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF
8 MHz	1 MΩ	0	10-30 pF	40-60 pF

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+7V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to Vcc + 0.3

DC CHARACTERISTICS

(TA = –40°C to +85°C, VCC = 5V ± 10%, Vss = 0V, unless otherwise noted; positive current is defined as entering the chip.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		Vcc	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = -5.0 mA on all outputs except XOUT	2.4			V
ICC	Average Power Supply	See Note 1		5	10	mA
	Current	See Note 2		50		µA
IIL	Input Leakage	VCC=5.25V, VSS=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{\text{DSR}}$, $\overline{\text{DCD}}$, $\overline{\text{CTS}}$, $\overline{\text{RI}}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 kHz.

Note 2: VCC = 5.5V, TA = –40°C; No output load; CMOS-level inputs, oscillator disabled

CAPACITANCE

(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2	Clock Input Capacitance			15	20	pF
CXTAL1	Clock Output Capacitance			20	30	pF
CI	Input Capacitance			6	10	pF
CO	Output Capacitance			10	20	pF

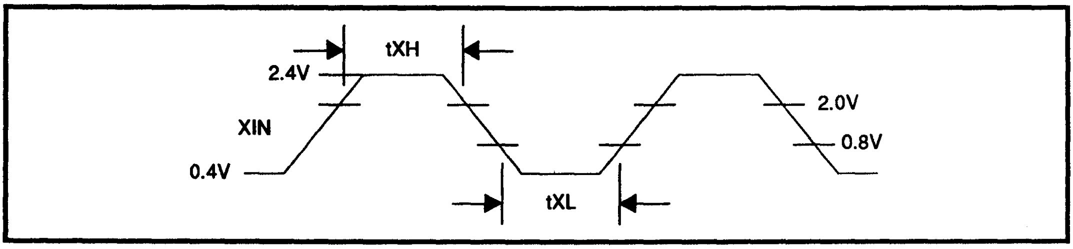
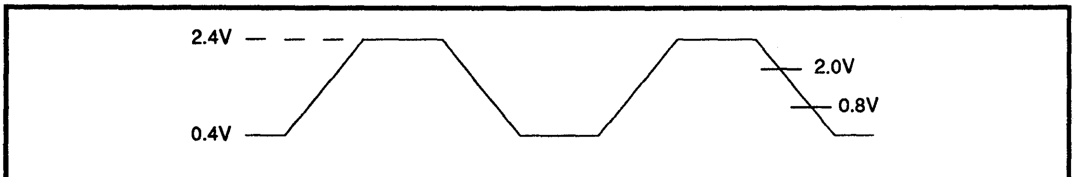


FIGURE 2: External Clock Input* (8 MHz Maximum)



The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

The 2.0V and 0.8 levels are the voltages at which timing tests are made.

FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ±10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5)

PARAMETER		CONDITIONS	73M550 73M1550 73M2550		UNITS
			MIN	MAX	
tADS	Address Strobe Width		50		ns
tAS	Address Setup Time		30		ns
tAH	Address Hold Time		0		ns
tCS	Chip Select Setup Time		30		ns
tCH	Chip Select Hold Time		0		ns
tAR	READ Delay from Address		30		ns

READ & WRITE CYCLE (Continued)

PARAMETER		CONDITIONS	73M550 73M1550 73M2550		UNITS
			MIN	MAX	
tRD	READ Strobe Width		80		ns
tRC	Read Cycle Delay		50		ns
tAD	Address to Read Data			160	ns
RC	Read Cycle	See Note 1 & 4	210		ns
tRDD	READ to Driver Disable Delay	100 pF load See Note 2		50	ns
tRVD	Delay from READ to Data	100 pF load		80	ns
tHZ	READ to Floating Data Delay	100 pF load See Note 2	0	60	ns
tRA	Address Hold Time from READ	See Note 3	20		ns
tAW	WRITE Delay from Address	See Note 3	30		ns
tWR	WRITE Strobe Width		80		ns
tWC	Write Cycle Delay		50		ns
WC	Write Cycle = tAW+tWR+tWC		160		ns
tDS	Data Setup Time		30		ns
tDH	Data Hold Time		30		ns
tWA	Address Hold Time from WRITE	See Note 3	20		ns
tMRW	Master Reset Pulse Width		1		µs
tXH	Duration of Clock High Pulse	External Clock (4 MHz max.)	100		ns
tXL	Duration of Clock Low Pulse	External Clock (4 MHz max.)	100		ns

Note 1: RC = tAD + tRC

Note 2: Charge and discharge time is determined by VOL, VOH and the external loading

Note 3: Applicable only when $\overline{\text{ADS}}$ is tied low

Note 4: In FIFO mode RC = 425 ns (minimum) between reads of the RCVR FIFO and the status registers (interrupt identification register or line status register).

READ occurs when both read (RD, $\overline{\text{RD}}$) and chip select (CS0, CS1, $\overline{\text{CS2}}$, latched by $\overline{\text{ADS}}$) are asserted.

WRITE occurs when both write (WR, $\overline{\text{WR}}$) and chip select (CS0, CS1, $\overline{\text{CS2}}$, latched by $\overline{\text{ADS}}$) are asserted.

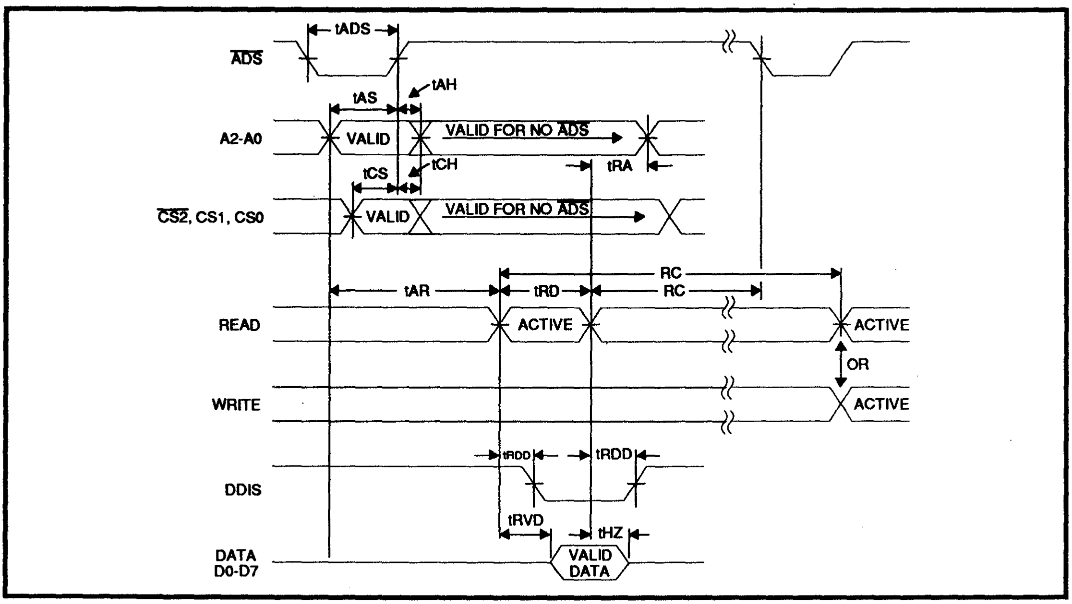


FIGURE 4: Read Cycle Timing

NOTE: READ occurs when both read (RD, $\overline{\text{RD}}$) and chip select (CS0, CS1, $\overline{\text{CS2}}$, latched by $\overline{\text{ADS}}$) are asserted.

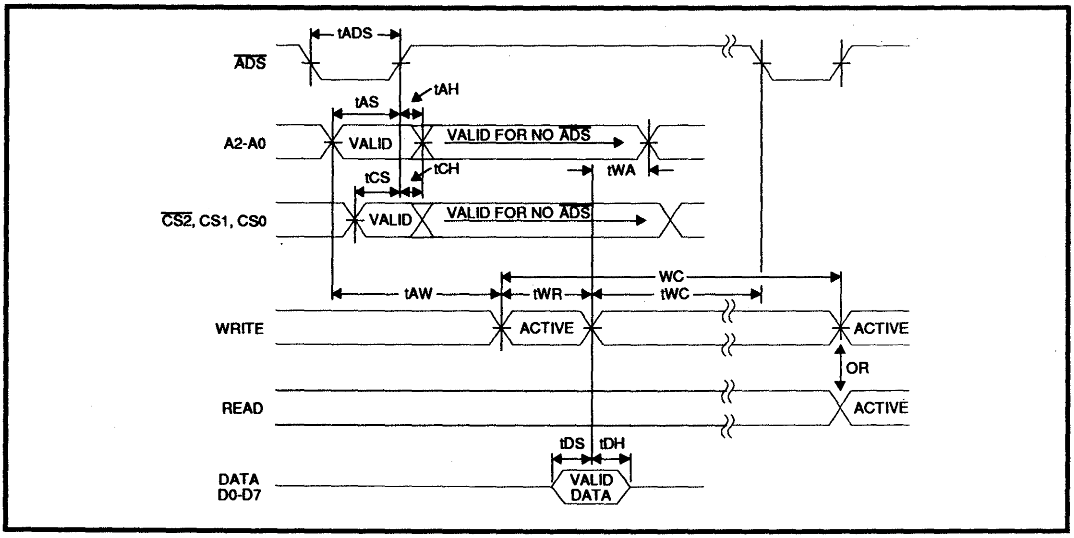


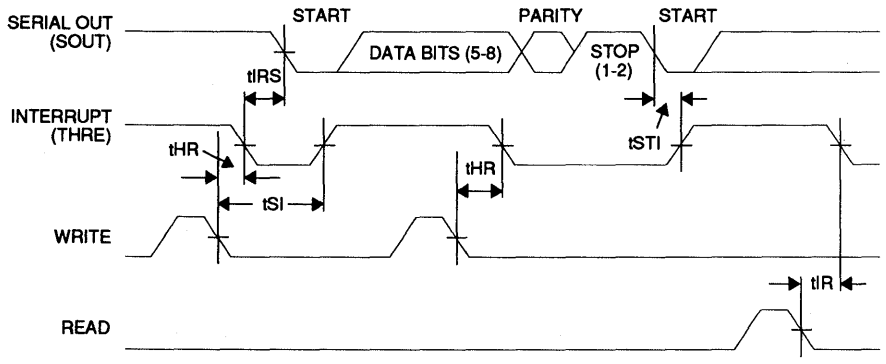
FIGURE 5: Write Cycle Timing

NOTE: WRITE occurs when both write (WR, $\overline{\text{WR}}$) and chip select (CS0, CS1, $\overline{\text{CS2}}$, latched by $\overline{\text{ADS}}$) are asserted.

TRANSMITTER (Refer to Figure 6)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from the end of WRITE to the negation of Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		8	24	BAUDOUT cycles
tSI	Delay from Initial Write to Interrupt	See Note 1	16	24	BAUDOUT cycles
tSTI	Delay from Stop to Interrupt (THRE)	See Note 1	8	8	BAUDOUT cycles
tIR	Delay from the end of READ to the negation of Interrupt	100 pF load		250	ns
tSXA	Delay from Start to $\overline{\text{TXRDY}}$ active	100 pF load		8	BAUDOUT cycles
tWXI	Delay from Write to $\overline{\text{TXRDY}}$ inactive	100 pF load		195	ns

Note: This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active (see FIFO Interrupt mode operation).



NOTES:
1. SEE WRITE CYCLE TIMING; WRITE IS A PRODUCT OF WR, $\overline{\text{WR}}$ AND CS0, CS1, $\overline{\text{CS2}}$
2. SEE READ CYCLE TIMING; READ IS A PRODUCT OF RD, $\overline{\text{RD}}$ AND CS0, CS1, $\overline{\text{CS2}}$

FIGURE 6: Transmitter Timing

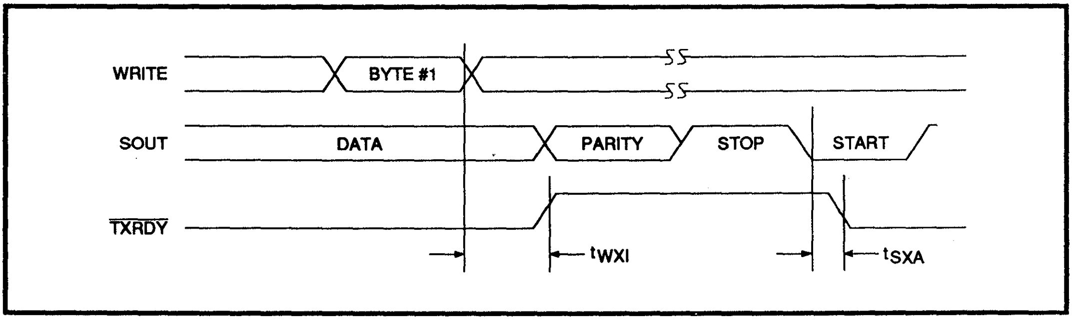


FIGURE 7: Transmitter Ready (Pin 24) FCR D0 = 0 or FCR D0 = 1 and FCR D3 = 0 (Mode 0)

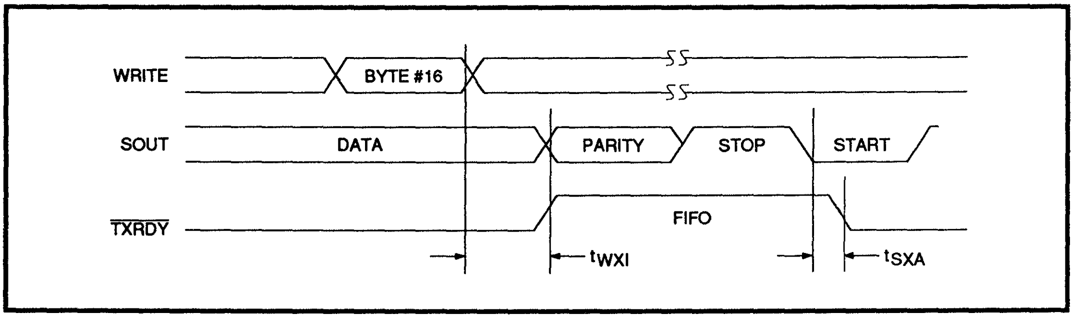
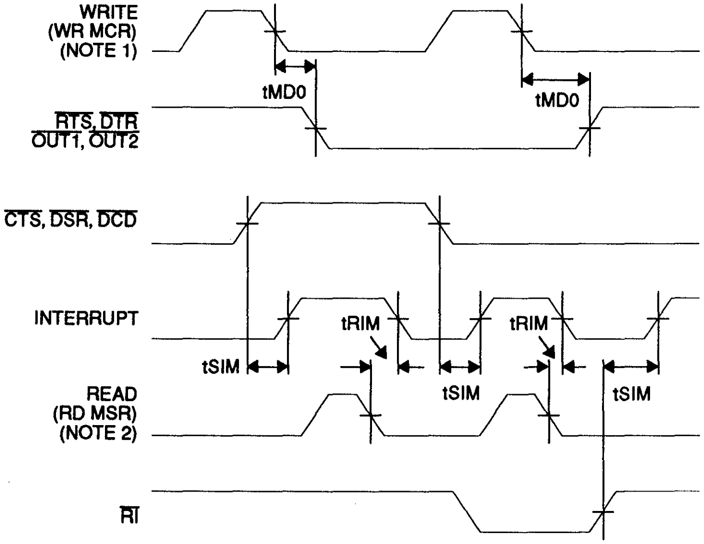


FIGURE 8: Transmitter Ready (Pin 24) FCR D0 = 1 and FCR D3 =1 (Mode 1)

NOTE: WRITE occurs when both write (WR, $\overline{\text{WR}}$) and chip select (CS0, CS1, $\overline{\text{CS2}}$, latched by $\overline{\text{ADS}}$) are asserted.

MODEM CONTROL (Refer to Figure 9)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from WRITE MCR to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Reset Interrupt from RD, $\overline{RD}$ (RD MSR)	100 pF load		250	ns



NOTES:
1. SEE WRITE CYCLE TIMING; READ OCCURS WHEN BOTH READ (RD, $\overline{RD}$) AND CHIP SELECT (CS, CS1, $\overline{CS2}$, LATCHED BY $\overline{ADS}$) ARE ASSERTED.
2. SEE READ CYCLE TIMING; WRITE OCCURS WHEN BOTH WRITE (WR, $\overline{WR}$) AND CHIP SELECT (CS, CS1, $\overline{CS2}$, LATCHED BY $\overline{ADS}$) ARE ASSERTED.

FIGURE 9: Modem Controls Timing

BAUD GENERATOR (Refer to Figure 10)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
N	Baud Divisor		1	2^{16}-1	
tBLD	Baud Output Negative Edge Delay	100 pF load		125	ns
tBHD	Baud Output Positive Edge Delay	100 pF load		125	ns
tLW	Baud Output Down Time	fX=8 MHz, div. by 2, 100 pF load	100		ns
tHW	Baud Output Up Time	fX=8 MHz, div. by 2, 100 pF load	75		ns

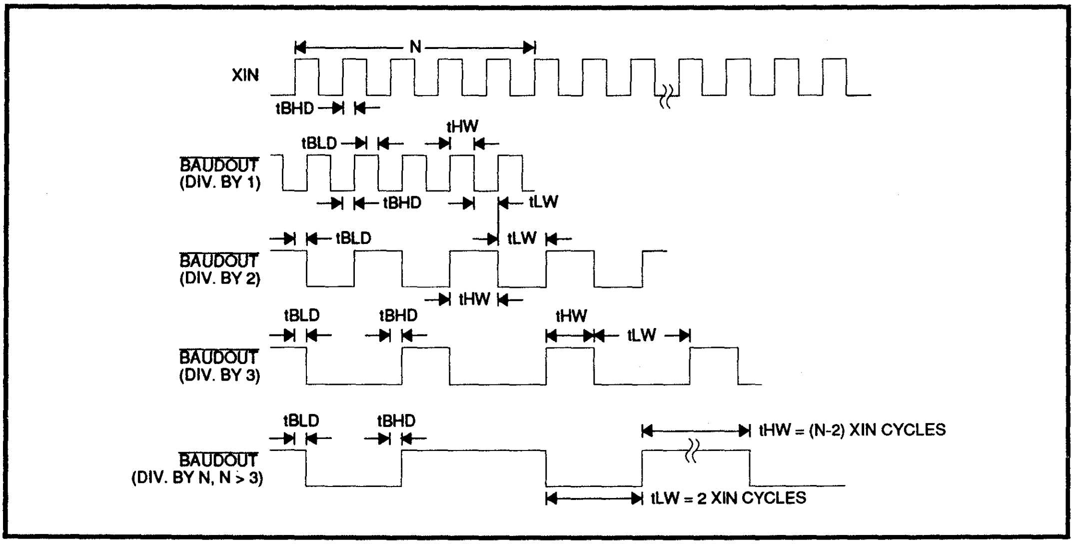
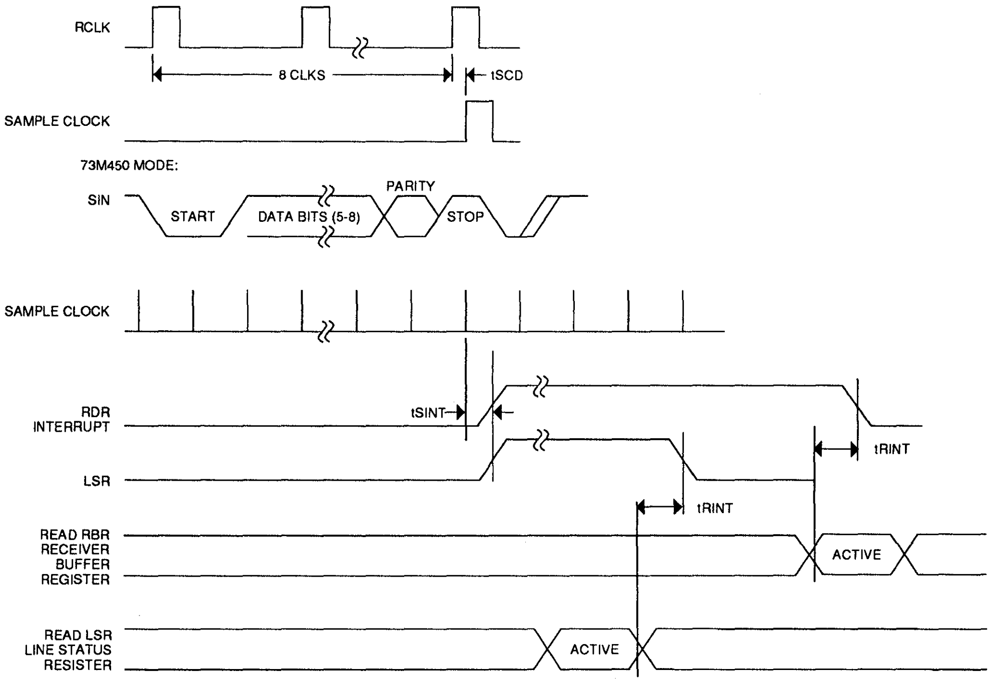


FIGURE 10: $\overline{\text{BAUDOUT}}$ Timing

RECEIVER (Refer to Figure 11)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt	RCLK=tXH & tXL See Note 1		1	RCLK cycles
tRINT	Delay from READ (RD RBR/RD LSR) to Reset Interrupt	100 pF load		1	µs

Note 1: In the FIFO mode (FCR D0 = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RD RBR goes inactive. Timeout interrupt is delayed 8 RCLKs.



NOTE:
1. SEE READ CYCLE TIMING
2. READ OCCURS WHEN BOTH READ (RD, $\overline{RD}$) AND CHIP SELECT (CS, CS1, $\overline{CS2}$, LATCHED BY $\overline{ADS}$) ARE ASSERTED.

FIGURE 11: Receiver Timing

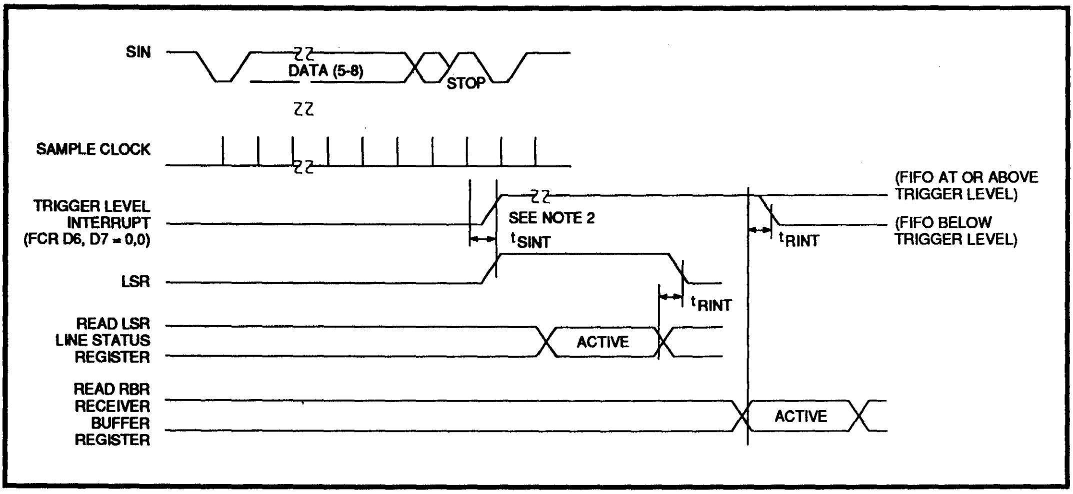


FIGURE 12: RCVR FIFO First Byte (This sets RBR)

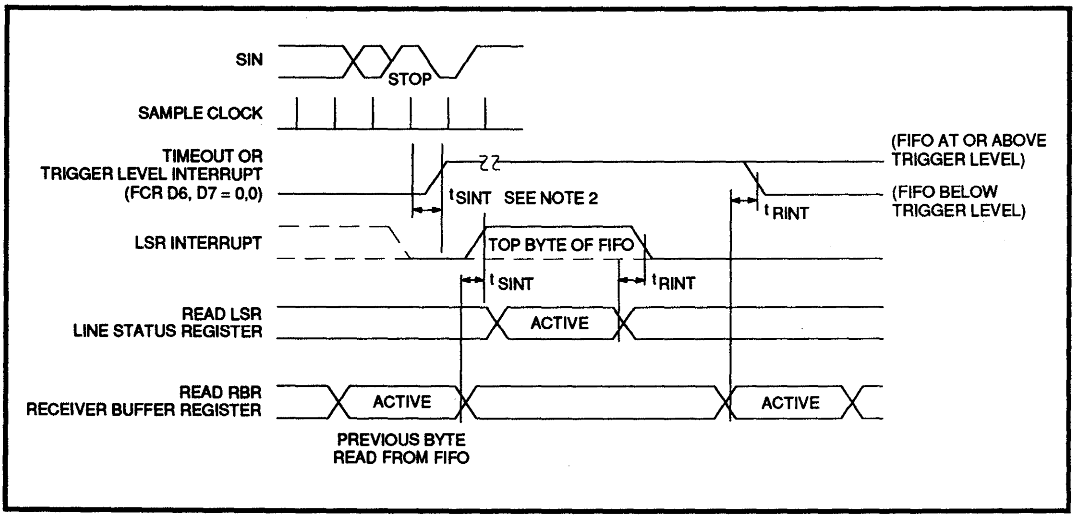


FIGURE 13: RCVR FIFO Bytes Other Than the First Byte (RBR is already set)

Note 1: This is the reading of the last byte in the FIFO

Note 2: If FCR D0 = 1, then tSINT = 3 RCLKs. For a timeout interrupt, tSINT = 8RCLKs.

Note 3: READ occurs when both read (RD, $\overline{RD}$) and chip select (CS0, CS1, $\overline{CS2}$, latched by $\overline{ADS}$) are asserted.

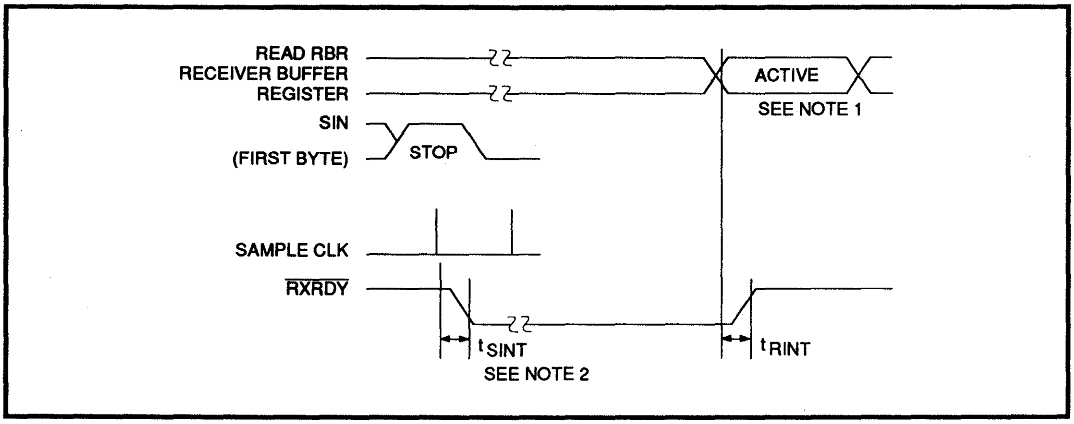


FIGURE 14: Receiver Ready (Pin 29) FCR D0 = 0 or FCR D0 = 1 and FCR D3 = 0 (Mode 0)

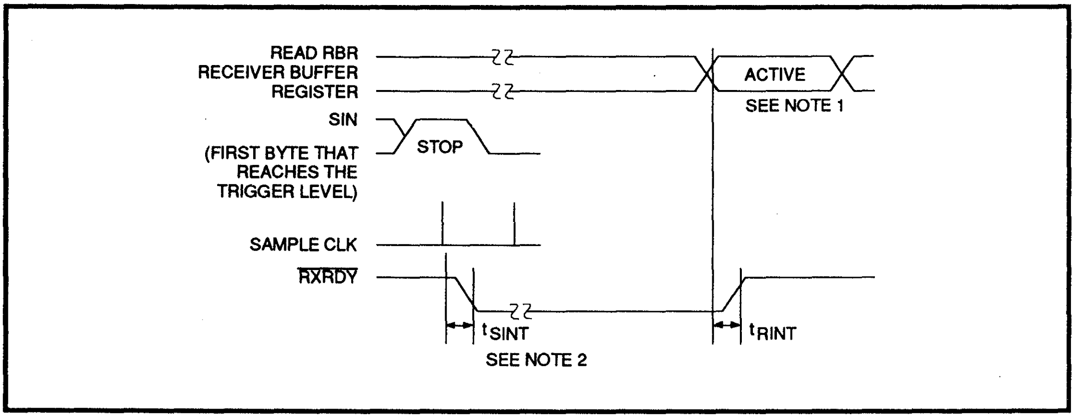


FIGURE 15: Receiver Ready (Pin 29) FCR D0 = 1 and FCR D3 = 1 (Mode 1)

Note 1: This is the reading of the last byte in the FIFO

Note 2: If FCR D0 = 1, then tSINT = 3 RCLKs. For a timeout interrupt, tSINT = 8RCLKs.

Note 3: READ occurs when both read (RD, $\overline{\text{RD}}$) and chip select (CS0, CS1, $\overline{\text{CS2}}$, latched by $\overline{\text{ADS}}$) are asserted.

SSI 73M550 TIMING COMPARED TO PCMCIA PC CARD STANDARD - RELEASE 2.0

					SSI 73M550			
ITEM	**SYMBOL**	**IEEE**	**MIN**	**MAX**	**SSI**	**MIN**	**MAX**	**UNITS**
Data Setup before IOWR	t su (IOWR)	tDVIWL	60		TDS	30		ns
Data Hold following IOWR	t h (IOWR)	tIWHDX	30		TDH	30		ns
IOWR Width Time	t w IOWR	tIWLIWH	165		TWR	80		ns
Address Setup before IOWR	t su A (IOWR)	tAVIWL	70		TAW	30		ns
Address Hold following IOWR	t h A (IOWR)	tIWHAX	20		TWA	20		ns
CE Setup before IOWR	t su CE (IOWR)	tELIWL	5			Any		
CE Hold following IOWR	t h CE (IOWR)	tIWHEH	20			Any		
REG Setup before IOWR	t su REG (IOWR)	tRGLIWL	5					
REG Hold following IOWR	t h REG (IOWR)	tIWHRGH	0					
IOIS16 Delay Falling from Address	t d IOIS16 $(ADR)_1$	tAVISL		35				
IOIS16 Delay Rising from Address	t d IOIS16 $(ADR)_2$	tAVISH		35				
Wait Delay Falling from IOWR	t d WAIT (IOWR)	tIWLWTL		35				
Wait Width Time	t w WAIT	tWLWTH		12,000				
NOTE: The maximum load on WAIT, INPACK and IOIS16 are 1 LSTTL with 50 pF total load.								

TABLE 6: I/O Output (WRITE) Timing Specification for All 5V I/O Cards

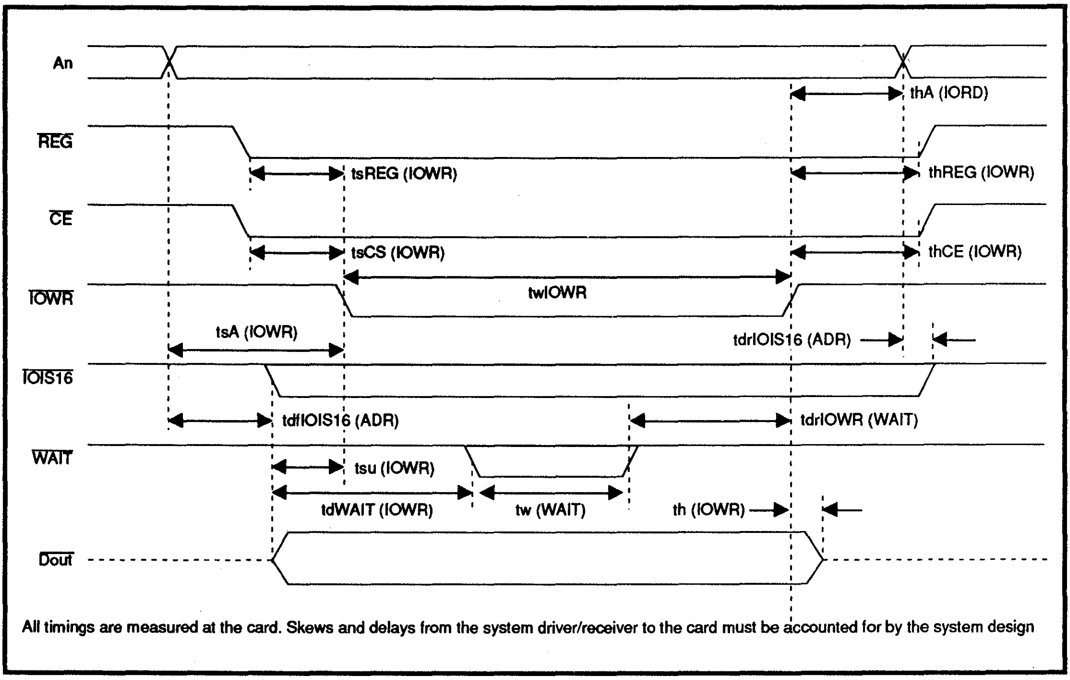


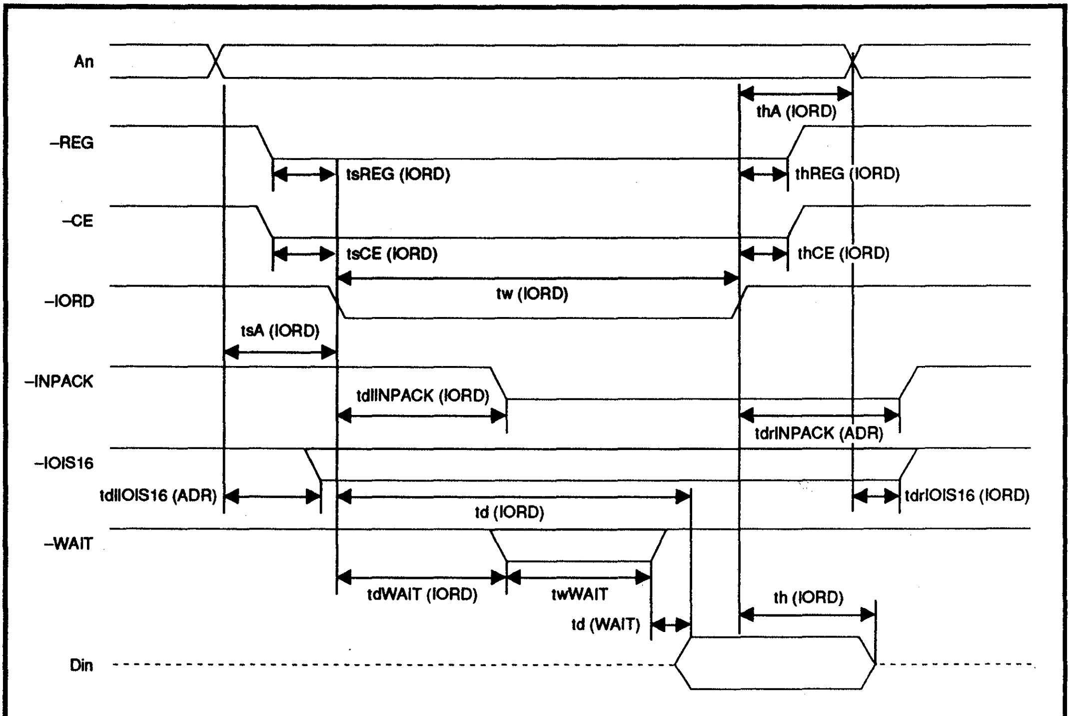
FIGURE 16: I/O Output Timing Specification (WRITE)

SSI 73M550 TIMING COMPARED TO PCMCIA PC CARD STANDARD - RELEASE 2.0

					SSI 73M550			
ITEM	**SYMBOL**	**IEEE**	**MIN**	**MAX**	**SSI**	**MIN**	**MAX**	**UNITS**
Data Delay after IORD	t d (IORD)	tIGLQV		100	TRVD		80	ns
Data Hold following IORD	t h (IORD)	tIGHQX	0		THZ	0		ns
IORD Width Time	t w IORD	tIGLIGH	165		TRD	80		ns
Address Setup before IORD	t su A (IORD)	tAVIGL	70		TAR	30		ns
Address Hold following IORD	t h A (IORD)	tIGHAX	20		TRA	20		ns
CE Setup before IORD	t su CE (IORD)	tELIGL	5			Any		
CE Hold following IORD	t h CE (IORD)	tIGHEH	20			Any		
REG Setup before IORD	t su REG (IORD)	tRGLIGL	5					
REG Hold following IORD	t h REG (IORD)	tIGHRGH	0					
INPACK Delay Falling from IORD	t d INPACK (IORD)	tGLIAL	0	45				
INPACK Delay Rising from IORD	t d INPACK (IORD)	tIGHIAH		45				
IOIS16 Delay Falling from Address	t d IOIS16 (ADR)$_1$	tAVISL		35				
IOIS16 Delay Rising from Address	t d IOIS16 (ADR)$_2$	tAVISH		35				
Wait Delay Falling from IORD	t d WAIT (IORD)	tIGLWTL		35				
Data Delay from Wait Rising	td(WAIT)	tWTHQV		35				
Wait Width Time	t w WAIT	tWLWTH		12,000				

NOTE: The maximum load on WAIT, INPACK and IOIS16 are 1 LSTTL with 50 pF total load.

TABLE 7: I/O Output (READ) Timing Specification for All 5V I/O Cards



All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design

FIGURE 17: I/O Output Timing Specification (READ)

APPLICATIONS INFORMATION

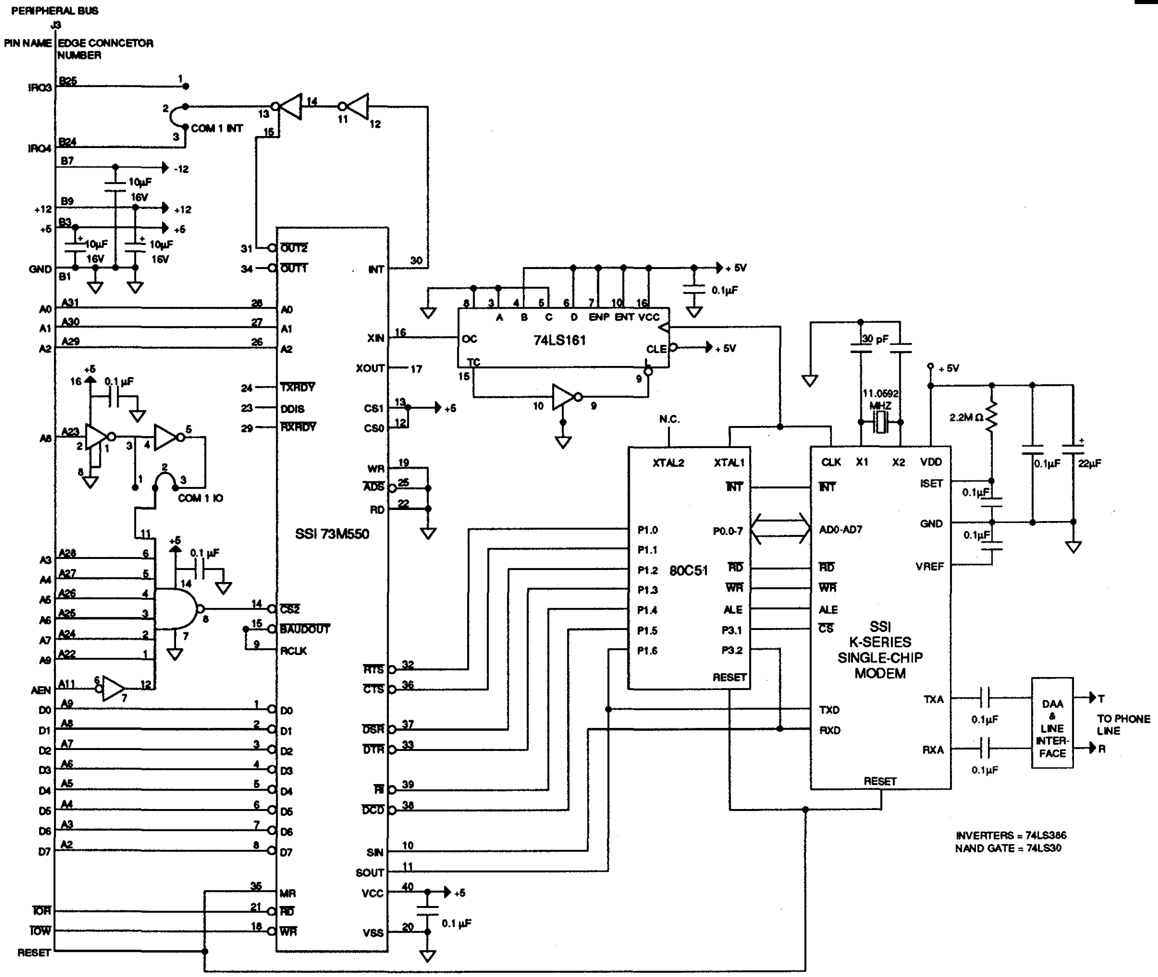
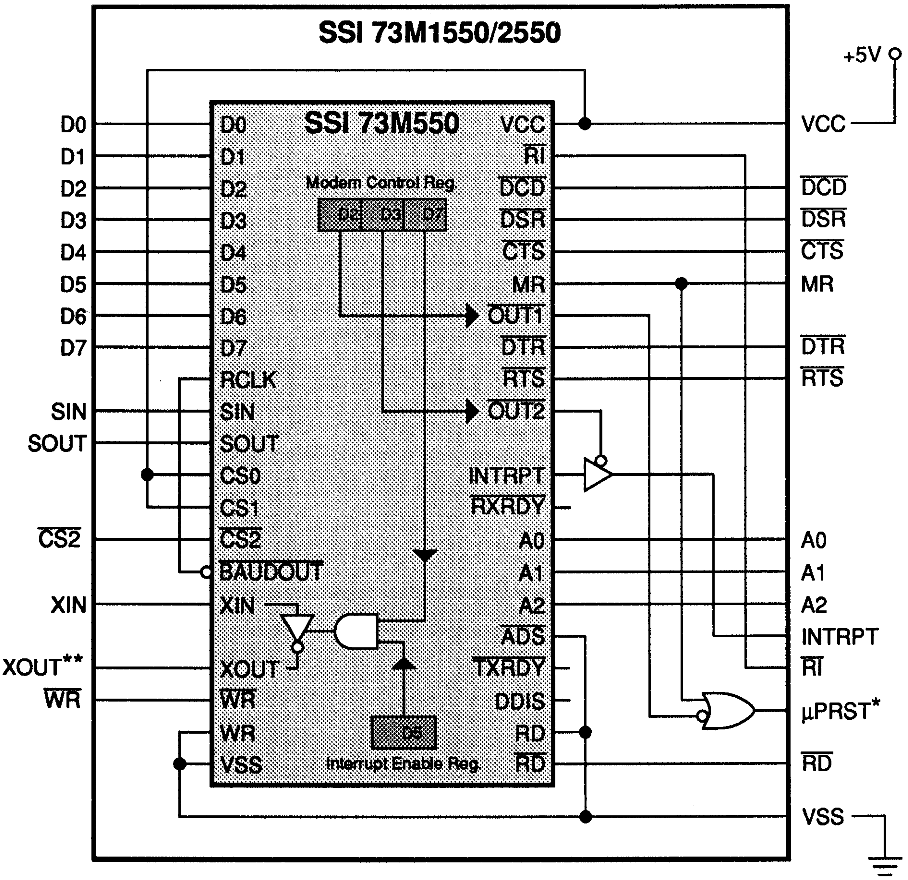


FIGURE 18: Typical Application Showing Modem Interface to Peripheral-Bus via SSI 73M550 UART

APPLICATIONS INFORMATION (Continued)

28-PIN VERSION

The 73M550 is available in two 28-pin configurations: SSI 73M1550 and SSI 73M2550. The relation between these two products and the 40-pin version is shown in the accompanying diagram. Note that the only difference between the 73M1550 and 73M2550 is that the 73M2550 adds the µPRST pin at the expense of the XOUT pin.



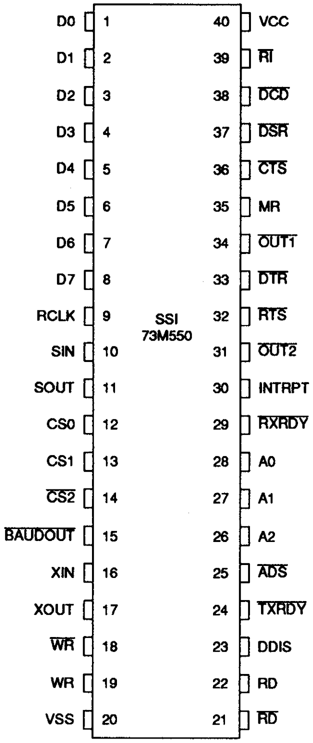
*SSI 73M2550 only.
**SSI 73M1550 only.

FIGURE 19: Adapter Diagram Showing Internal Connections and Bond-outs from 40-pin to 28-pin Packages

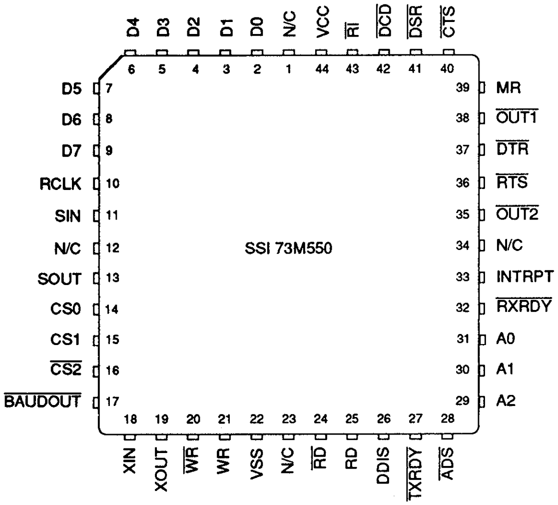
SSI 73M550
SSI 73M1550/2550
UART with FIFOs

PACKAGE PIN DESIGNATIONS

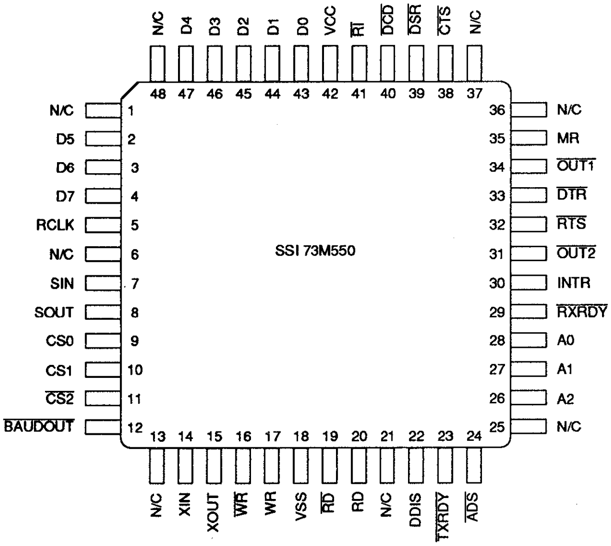
(Top View)



SSI 73M550 40-Pin DIP



SSI 73M550 44-Pin PLCC

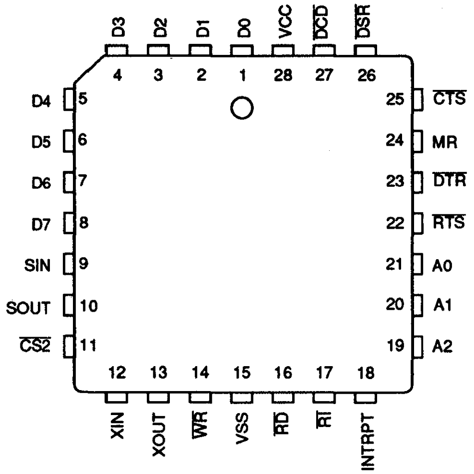


SSI 73M550 48-Lead TQFP

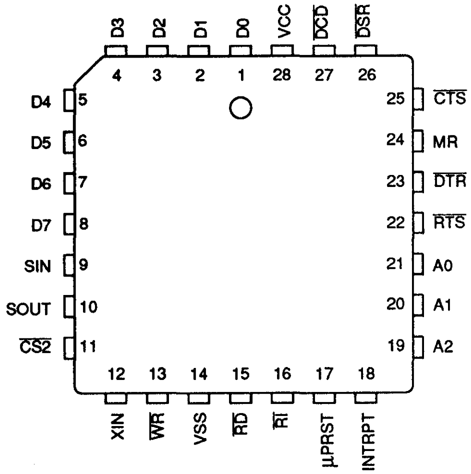
PACKAGE PIN DESIGNATIONS (continued)

(Top View)

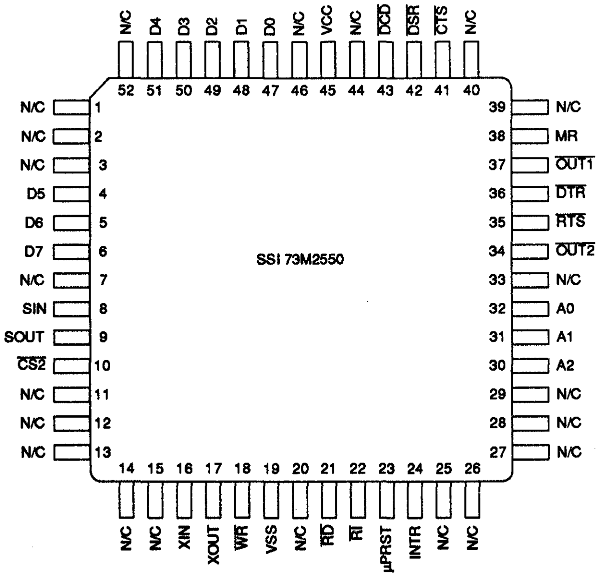
CAUTION: Use handling procedures necessary for a static sensitive component.



SSI 73M1550 UART 28-Pin PLCC



SSI 73M2550 UART 28-Pin PLCC



SSI 73M2550 52-Lead QFP

SSI 73M550
SSI 73M1550/2550
UART with FIFOs

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 73M550	40-pin PDIP	73M550-IP	73M550-IP
	44-pin PLCC	73M550-IH	73M550-IH
	48-lead TQFP	73M550-IGT	73M550-IGT
SSI 73M1550	28-pin PLCC	73M1550-IH	73M1550-IH
SSI 73M2550	28-pin PLCC	73M2550-IH	73M2550-IH
	52-lead QFP	73M2550-IG	73M2550-IG

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Notes:

Section 3

SPECIAL MODEM PRODUCTS

silicon systems®
A TDK Group Company

SSI 73M223
1200 Baud FSK Modem

January 1993

DESCRIPTION

The SSI 73M223 modem device receives and transmits serial and binary data over existing telephone networks using Frequency Shift Keying (FSK). It provides the filtering, modulation, and demodulation to implement a serial, asynchronous data communication channel. The SSI 73M223 employs the CCITT V.23 signaling frequencies of 1302 and 2097 Hz, operating at 1200 baud, and is intended for half duplex operation over a two-line system.

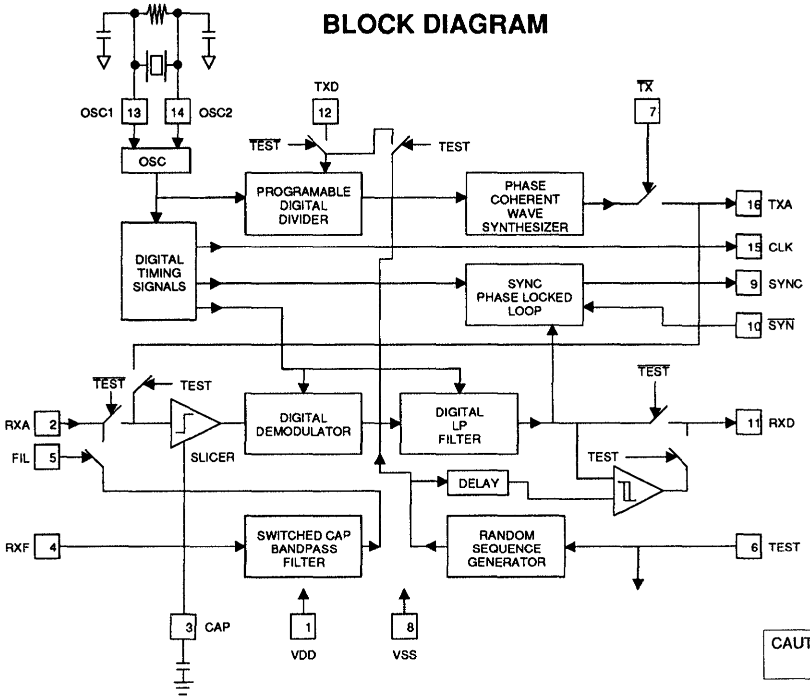
The SSI 73M223 provides a cost-effective alternative to existing modem solutions. It is ideally suited for R.F. data links, credit verification systems, point-of-sale terminals, and remote process control.

CMOS technology ensures small size, low-power consumption and enhanced reliability.

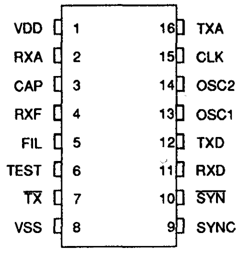
FEATURES

- **Low cost FSK Modem**
- **1200 baud operation**
- **CMOS switched capacitor technology**
- **Built-in self-test feature**
- **On-chip filtering, and Modulation/Demodulation**
- **Uses CCITT V.23 frequencies**
- **On chip crystal oscillator**
- **Low power/High reliability**
- **16-pin plastic package**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 73M223 has four main functional sections: timing, transmit, receive, and test. Each section of the chip will be individually described below.

TIMING

The timing section contains the oscillator (OSC) and random logic which generates digital timing signals used throughout the chip. The time base can be derived from 3.18MHz crystal or an external digital input. The digital timing logic divides the oscillator frequency to give a 1200Hz output than can be used for system timing. The signaling frequencies are 1302Hz for logic "1" and 2097Hz for logic "0". The modem will operate with clock inputs from 330KHz to 3.3MHz. However, the signaling frequencies and the system timing will be different.

TRANSMITTER

The SSI 73M223 transmitter consists of a programmable divider that drives a coherent phase frequency synthesizer. The programmable divider is digitally controlled via the Data Input pin (TXD). The output of the divider clocks a 16 segment phase coherent frequency synthesizer. A sine wave is constructed by eight weighted capacitors which are the inputs to a high pass filter. The synthesized signal is output directly to the transmit pin TXA. The transmit signal can be disabled by using the digital control pin TX.

RECEIVER

The SSI 73M223's receiver is comprised of three sections: the input bandpass filter, the synchronization loop, and the demodulator.

The input bandpass filter is a four pole Butterworth filter, implemented using switched capacitor technology. This filter reduces wideband noise which significantly improves data error rates. The SSI 73M223 can be configured with the bandpass filter in series with the receiver by setting FIL = 1 and inserting the received signal at RXF. The bandpass filter can be deleted from the system by setting FIL = 0 and inputting the received signal through RXA.

The demodulator is used to detect a received mark or space.

The synchronization for sampling the digital output at RXD is derived from a digital phase locked loop. The phase locked loop is clocked at 16 times the bit rate with a maximum lock period of 8 clocks to lock on the data output signal.

SELF TEST MODE

The SSI 73M223 features an autotest mode which provides easy field test capability of the chip's functionality. The modem is placed in the test mode by taking the test pin high. In the test mode the Data Input pin is disconnected and the programmable divider is driven by a pseudo random PN sequence generator and the transmitter's output is connected to the receiver's input. The input data to the programmable divider is delayed by the system delay time and compared to the digital output on sync transitions. If the detected data matches the delayed input data from the PN sequence counter, the SSI 73M223 is properly functioning as indicated by RXD low. A high on the RXD pin indicates a functional problem on the SSI 73M223.

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	VDD	Positive Supply Voltage
2	RXA	Receive Analog Input. Analog input from the telephone network.
3	CAP	Capacitor. Connect a 0.1µF capacitor between Pin 3 and ground (VSS).
4	RXF	Filtered Receive Analog Input
5	FIL	Analog Input Control. A logical 1 selects the filtered input. A logical 0 selects the non-filtered input.
6	TEST	Self-Test Mode Control. Normal operation when a logical 0.A logical 1 places the device into the self-test mode. A low appears at RXD, to indicate a properly functioning device.
7	$\overline{\text{TX}}$	Transmitter Control. A logical 0 selects transmit mode. A logical 1 selects a stand-by condition forcing TXA to VDD/2 VDC.
8	VSS	Ground
9	SYNC	Synchronized Output. Digital output synchronized with the received signal and used to sample the received eye pattern.
10	$\overline{\text{SYN}}$	Sync Disable. A logical 1 input disables the phase locked signal from the received data and locks it to the 1200Hz reference.
11	RXD	Receiver Digital Output
12	TXD	Transmitter Digital Input
13	OSC_1	Crystal Input (3.1872MHz) or External Clock Input
14	OSC_2	Crystal Return
15	CLK	1200Hz Squarewave Output. Can drive up to 10 CMOS loads.
16	TXA	Transmitter Analog Output

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
Power Supply Voltage (VDD-VSS)	14	V
Analog Input Voltage at RXA	- 0.3 to VDD	V
Analog Input Voltage at RXF	- 3 to VDD	V
Digital Input Voltage	VSS - 0.3 to VDD + 0.3	V
Storage Temperature Range	- 65 to + 150	°C
Operating Temperature Range	- 25 to + 70	°C
Lead Temperature (10 secs soldering)	260	°C

ELECTRICAL CHARACTERSITICS

Unless otherwise specified, 4.5 <VDD <13 VDC, VSS = 0 VDC, -25° C <TA

POWER SUPPLY

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
VDD Voltage Supply Range		4.5		13	V
Supply Current	VDD = 5V 25° C		2.0		mA
	VDD = 12V 25° C		5.0		mA
Digital Inputs					
Input Low Voltage VIL		VSS - 0.3		VSS + 1.5	V
Input High Voltage VIH		VDD - 1.5		VDD + 0.3	V
Input Low Current IIL		-1			µA
Input High Current IIH				1	µA
Digital Outputs					
Output Low Voltage VOL	IOL < 1µA			0.05	V
Output High Voltage VOH	IOL < -1µA VDD = 5V	4.95			V
Output Low Current IOL	VOL = 0.4V VDD = 5V	0.5			mA
Output High Current IOH	VOH = 4.5V VDD = 5V	-0.2			mA
Analog Input Level @ RXA	Centered at VDD/2 + 0.5V	0.2		VDD/4	Vpp
Analog Input Level @ RXF	*DC Level between VDD & VSS	0.2		VDD/2	VDC
Error Rate	S/N = 8dB Input @ RXF			5 x 10^{-3}	
Analog Output Level @ TXA	RL ≥ 10K $\overline{TX}$ = 0		VDD/4		Vpp
	$\overline{TX}$ = 1		VDD/2		VDC
Output Frequency @ TXA	XTAL = 3.1872MHz TXD=1		1302		Hz
	TXD=0		2097		Hz
Output Harmonics	2nd to 14th Harmonics		-60	-50	dB
	15th Harmonic			-20	dB
Input Filter (RFX)	*Input = 200 m Vpp to VDD/2 Vpp				
Lower 3dB Corner			760		Hz
Upper 3dB Corner			2625		Hz

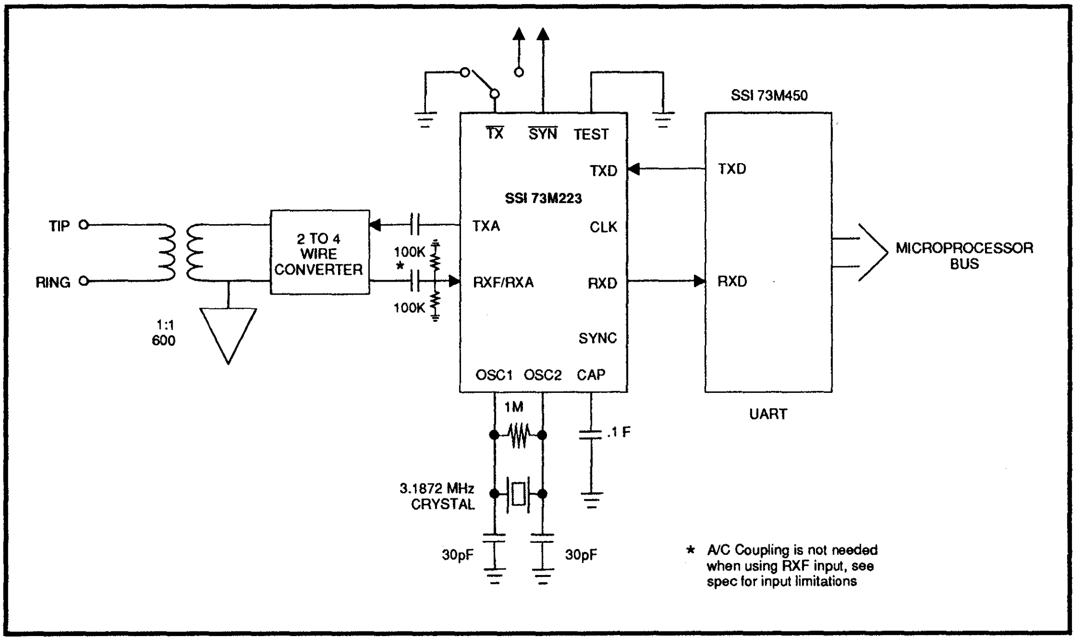
* Note: The SSI 73M223 RXF input is AC coupled internally but the DC value of the input must be between the two supplies VDD & VSS.

APPLICATION INFORMATION

The SSI 73M223 modem chip allows low cost communications in a private network, utilizing twisted pair telephone wires. This chip is the prime choice of those designers who require an efficient, high performance modem solution for dedicated private networks, HDX dial-up and other specialized applications. Such applications include credit verification systems, point-of-sale terminals, remote process control, private data links and acoustic modem designs.

Utilizing a crystal input of 3.1872MHz, the SSI 73M223 is a 1200 Baud, FSK modem. The signaling frequencies generated are 1302Hz for a logic “1” and 2097Hz for a logic “0”. Crystals with frequencies varying between 330KHz to 3.3MHz can be used. The baud rate and signaling frequencies vary linearly with variation in crystal frequency.

A typical implementation on the SSI 73M223 is shown in the figure below. An SSI 73M450 UART receives data to be transmitted from a microprocessor bus. The UART sends the data in a serial format to the SSI 73M223 modem after inserting the necessary start and stop bits. The modem transmits this data to the far end via the TXA pin. The figure depicts a half-duplex operation. Full-duplex operation can be implemented by utilizing separate transmit and receive circuits. A USART can be used instead of a UART if synchronous operation is desired. With synchronous operation, a USART uses the modem’s SYNC signal for timing to sample the received data, and the modem’s CLK signal to send data to be transmitted.

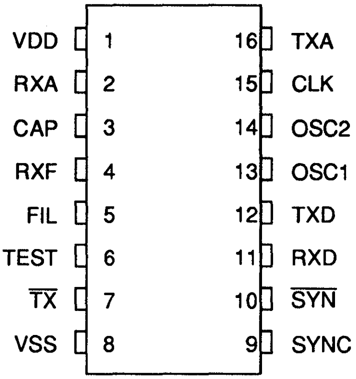


* A/C Coupling is not needed when using RXF input, see spec for input limitations

SSI 73M223 TYPICAL APPLICATION

PACKAGE PIN DESIGNATIONS

(Top View)



16-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73M223 16 Pin Plastic DIP	73M223 - CP	SSI 73M223 - CP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

SSI 73M376
Integrated Line Interface

Preliminary Data

January 1993

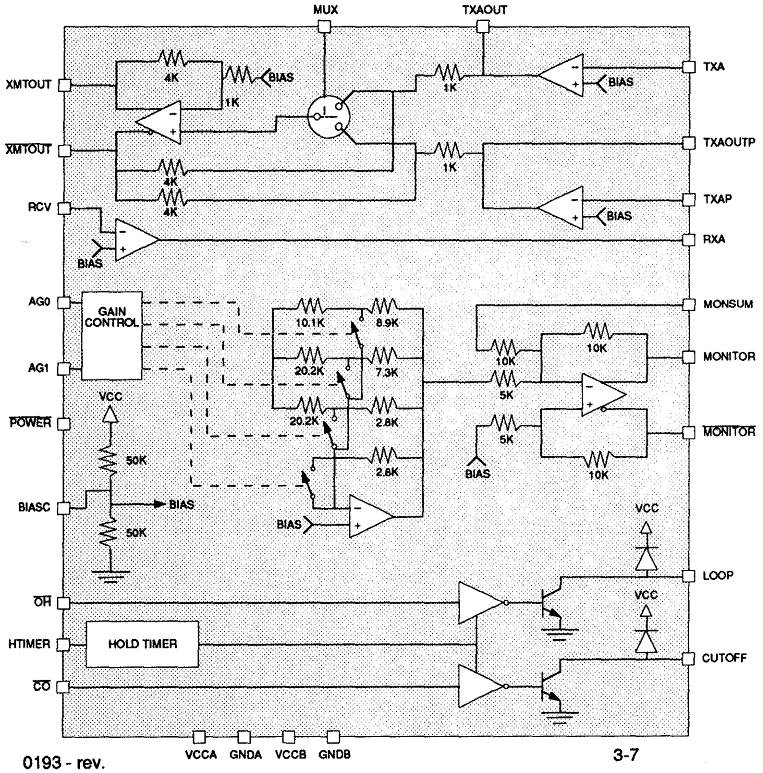
DESCRIPTION

The SSI 73M376 K-Series Integrated Line Interface Unit(LIU) enables the modem to make direct connections to the Public SwitchedTelephone Network. This single chip data access arrangement integrates all external active (line side) components required in K-Series modem designs. The SSI 73M376 operates from a single 5 volt supply ideally suited for low power portable applications. Along with the transmit and receive function, it provides transmit and receive amplifiers, programmable audio monitor, and relay drivers. In the transmit path it has provision for level programmable gain path as well as a normal gain path which can be switched via a TTL input. The 73M376 comes in a 28-lead PLCC package.

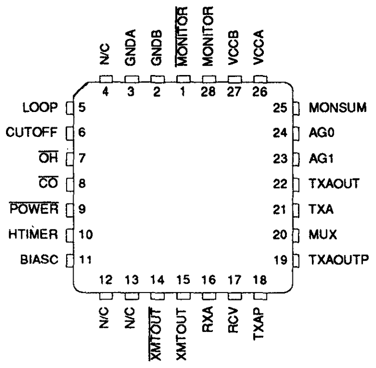
FEATURES

- **One-Chip data access arrangement**
- **Compatible with all SSI K-Series Modem Products**
- **On-board receive and transmit paths. Transmit has level protected programmability**
- **On-board differential speaker driver with four step variable gain**
- **On-board relay driver with power conserving hold state**
- **Low power (85 mW) with power down mode (25 mW) when on-hook**
- **Operates from a single +5V supply**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION:	Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The transmit output uses a differential drive to allow undistorted signals to be sent with a single 5 volt supply. Each output supplies half the drive signal to the transformer thus increasing the available output amplitude by 100%. Two dedicated transmit op-amps are supplied with the outputs and minus inputs brought out so that external resistors and capacitors can be connected facilitating gain setting and filtering. The TTL input, MUX, switches the output of the op-amps to the differential driver. If the MUX input is pulled high, or left floating, the TXA op-amp is selected. If the MUX input is pulled low the TXAP op-amp is selected.

The receive input, RCV, is the minus input of a dedicated op-amp where external resistors and capacitors can be connected facilitating gain setting and filtering. The bias, or plus, input for all the dedicated op-amps are connected to a VCC/2 bias point which allows for maximum swing between the supply rails. The VCC/2 bias point is brought out to an external pin, BIASC, where a compensation capacitor can be connected for power supply noise filtering.

The audio monitor gain stage has the RXA output as its input and has four gain settings; off or squelch, low, medium, and high. The output of the gain cell is fed to a summer where a signal can be summed in through the MONSUM pin. The audio amp differential output can drive an 8Ω speaker with up to 400 mW rms of power. A capacitor needs to be in series with the speaker so no DC current will flow.

On board relay drivers can directly drive the loop and cutoff relays. The TTL input $\overline{\text{OH}}$ (Off Hook) controls the loop relay driver. The TTL input $\overline{\text{CO}}$ (Cut Off) controls the cutoff relay driver. A timer, which uses an external timing capacitor connected to the HTIMER pin, is available to set a delay after relay energizing before the driver will go into its hold state. A negative transition on $\overline{\text{OH}}$ or $\overline{\text{CO}}$ starts the timer. When the timer has expired, both relay drivers will go into the hold state. While the timer is timing the relay drivers are in their full energizing state. If $\overline{\text{OH}}$ is low and $\overline{\text{CO}}$ goes low before the timer expires, or vice versa, then the timer will reset and start timing again.

The TTL input $\overline{\text{POWER}}$ controls the power down state. When $\overline{\text{POWER}}$ is low the part is powered up and when it is high, it is in its power down state.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCCA	I	Analog power supply input.
VCCB	I	Digital power supply input.
GNDA	I	Analog ground pin.
GNDB	I	Digital ground pin.
TXA	I	Negative input to transmit op-amp selected when MUX = 1.
TXAOUT	O	Transmit amplifier output.
TXAP	I	Negative input to alternate transmit op-amp input selected when MUX = 0.
TXAOUTP	O	Level programmed transmit amplifier output.
MUX	I	Transmit amplifier mux control (TTL). 1 selects TXA source 0 slects TXAP source
XMTOUT	O	Transmit output.
$\overline{\text{XMTOUT}}$	O	Transmit output (inverted).
RCV	I	Negative input to receive amplifier.
RXA	O	Receive amplifier output.
MONITOR	O	Positive audio amplified output.
$\overline{\text{MONITOR}}$	O	Negative audio amplified output.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
MONSUM	I	Monitor summing input slected when AG1 and AG0 = 0
AG0	I	Bit1 (TTL) input to set audio gain.
AG1	I	Bit2 (TTL) input to set audio gain.
BIASC	I	VCC/2 bias compensation point.
$\overline{\text{OH}}$	I	Off hook TTL compatible input. Controls the loop relay
$\overline{\text{CO}}$	I	Cut off TTL compatible input. Controls the cutoff relay.
HTIMER	I	Relay hold timing control pin connect to GND if not used.
LOOP	O	Loop relay drive output.
CUTOFF	O	Cutoff relay drive output.
$\overline{\text{POWER}}$	I	Power Down TTL compatible input. Controls power down mode. Low level powers up 73M376.

ELECTRICAL SPECIFICATIONS

ABSOULUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
VCC Supply Voltage	7	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	300	°C

RECOMMENDED OPERATING CONDITIONS

Unless otherwise specified 4.50V < Vcc < 5.50V and 0°C < T(ambient) < 70°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC SUPPLY VOLTAGE					
+5V	$\overline{\text{POWER}}$ low Outputs unloaded			17.0	mA
+5V	$\overline{\text{POWER}}$ high			5.0	mA
Junction Temperature	Relay drivers in hold state driving maximum current. MONITOR, $\overline{\text{MONITOR}}$ driving 8Ω speaker to max rms power			135	°C

DIGITAL PINS

(TTL compatible inputs: AG0, AG1, $\overline{\text{OH}}$, $\overline{\text{CO}}$, MUX, $\overline{\text{POWER}}$ pins)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Input low voltage	(VIL)	-0.3		0.8	V
Input high voltage	(VOH)	2.0		VCC+0.3	V
Input low current	VIL = 0.4 V	0.0		-0.4	mA
Input high current	VIH = 2.4 V			100	µA

TRANSMIT AND RECEIVE SECTION

Transmit Gain Single ended into Differential	$\frac{(\text{XMTOUT} - \overline{\text{XMTOUT}})}{\text{TXAOUT}}$ MUX=High	11.5		12.5	dB
Transmit Gain Single ended into Differential	$\frac{(\text{XMTOUT} - \overline{\text{XMTOUT}})}{\text{TXAOUTP}}$ MUX=Low	11.5		12.5	dB
XMTOUT, $\overline{\text{XMTOUT}}$ Differential Output Impedance				30	Ω
Transmit THD	7V p-p differential From TXA or TXAP to XMTOUT-$\overline{\text{XMTOUT}}$ with Op-Amp gain=0dB @ 1 kHz Zload = 600 Ω speaker driver off			-72	dB
Max. Capacitive differential load XMTOUT, $\overline{\text{XMTOUT}}$				300	pF
RCV, TXA, TXAP input impedance			1		MΩ
RCV, TXA, TXAP input offset voltage	RCV - VCC/2 TXA - VCC/2 TXAP - VCC/2		10		mV
RCV, TXA, TXAP input bias current	Vin = VCC/2			500	nA
Receive THD	From receive Op-Amp input to RXA with Op-Amp gain=8dB 4 kHz speaker driver off			-72	dB
Max. Capacitive load, TXAOUT, TXAOUTP, RXA				150	pF
Transmit and Receive Op-Amps Unity Gain Bandwidth			500		kHz
BIASC impedance V_{BIASC}=VCC/2		18K			Ω

MONITOR OUTPUT CIRCUIT

(All of the measurements are made with an 8Ω load, tied from MONITOR to $\overline{\text{MONITOR}}$, AC coupled through a 20 µF capacitor.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Gain	From RXA to Monitor outputs (MONITOR-$\overline{\text{MONITOR}}$)/RXA AG0=Low, AG1=Low			-60	dB
	AG0=High, AG1=Low	11		15	dB
	AG0=Low, AG1=High	18		23	dB
	AG0=High, AG1=High	27		31	dB
Max Output Swing	THD < -20 dB MONITOR-$\overline{\text{MONITOR}}$	3.5			Vpp
MONSUM gain	$\frac{\text{MONITOR} - \overline{\text{MONITOR}}}{\text{MONSUM}}$	22	25	26	dB
Max input at MONSUM				3.5	Vpp
MONITOR output offset	MONITOR-$\overline{\text{MONITOR}}$ AG0=Low, AG1=Low		5		mV
MONITOR output offset	MONITOR-$\overline{\text{MONITOR}}$ AG0=High, AG1=High		180		mV
MONSUM input impedance		8K			Ω

RELAY DRIVER OUTPUTS

Peak pull in current	-25 °C < T(ambient) < 85 °C at Vol=0.8 V	35			mA
Hold voltage	After hold timer has timed out	25%		40%	Vcc
Hold voltage delay	t=CHTIMER • 750K for 0.01 µF<CHTIMER<0.47 µF			±45	%

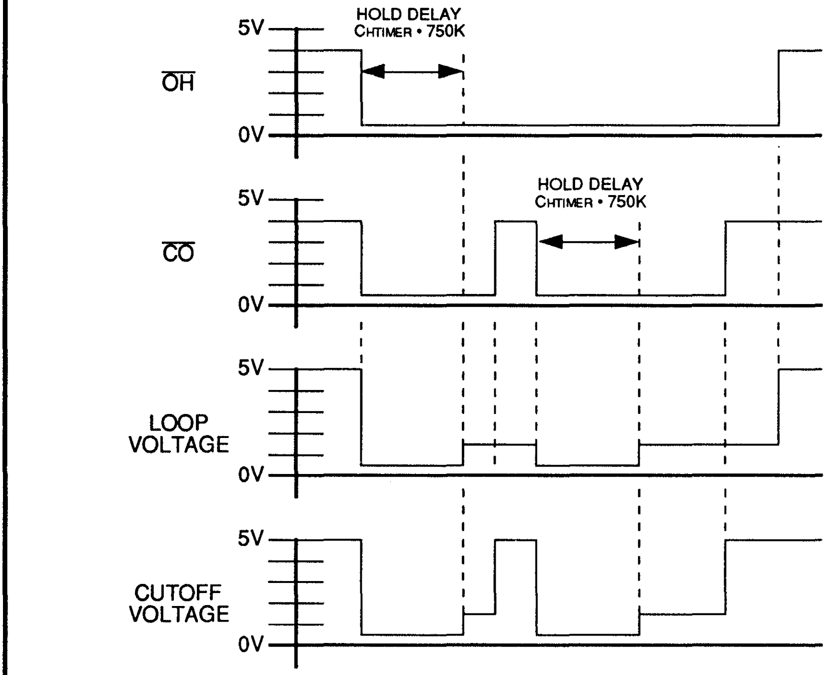


FIGURE 1: Relay Hold and Power Down Timing Diagrams

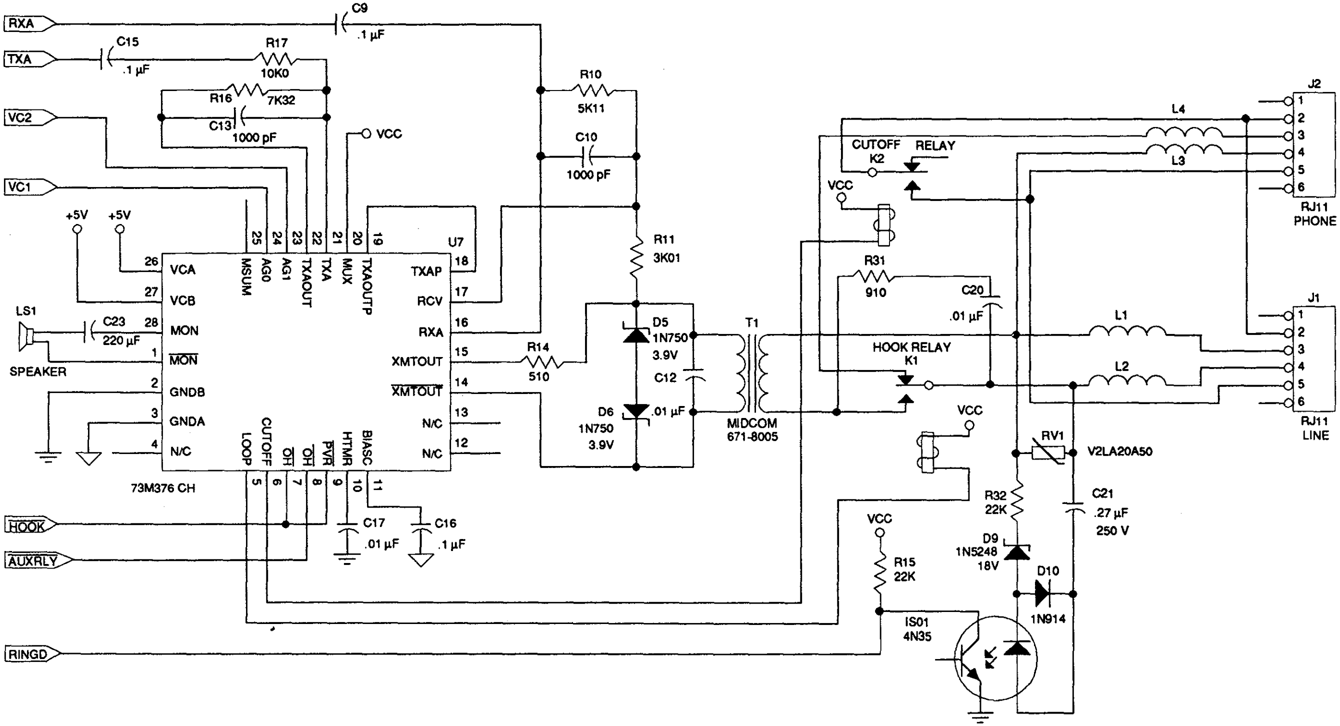
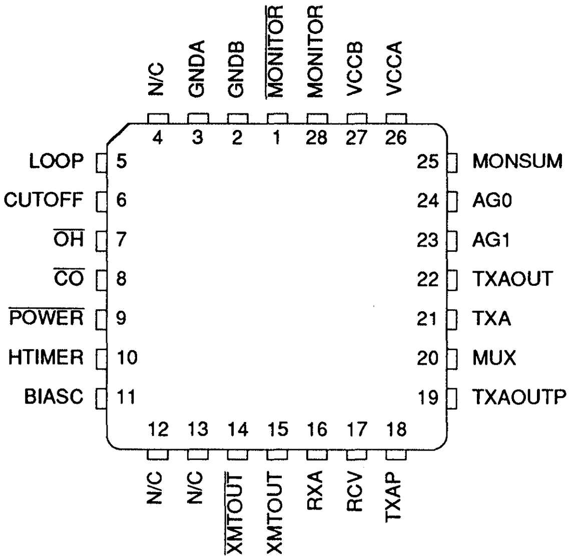


FIGURE 2: SSI 73M376 Based DAA Circuit

SSI 73M376
Integrated Line Interface

PACKAGE PIN DESIGNATIONS
(Top View)



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 73M376 28-Pin PLCC	73M376-CH	73M376-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Section 4

ANALOG SIGNALLING & SWITCHING PRODUCTS

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SSI 75T201
Integrated DTMF Receiver

October 1991

DESCRIPTION

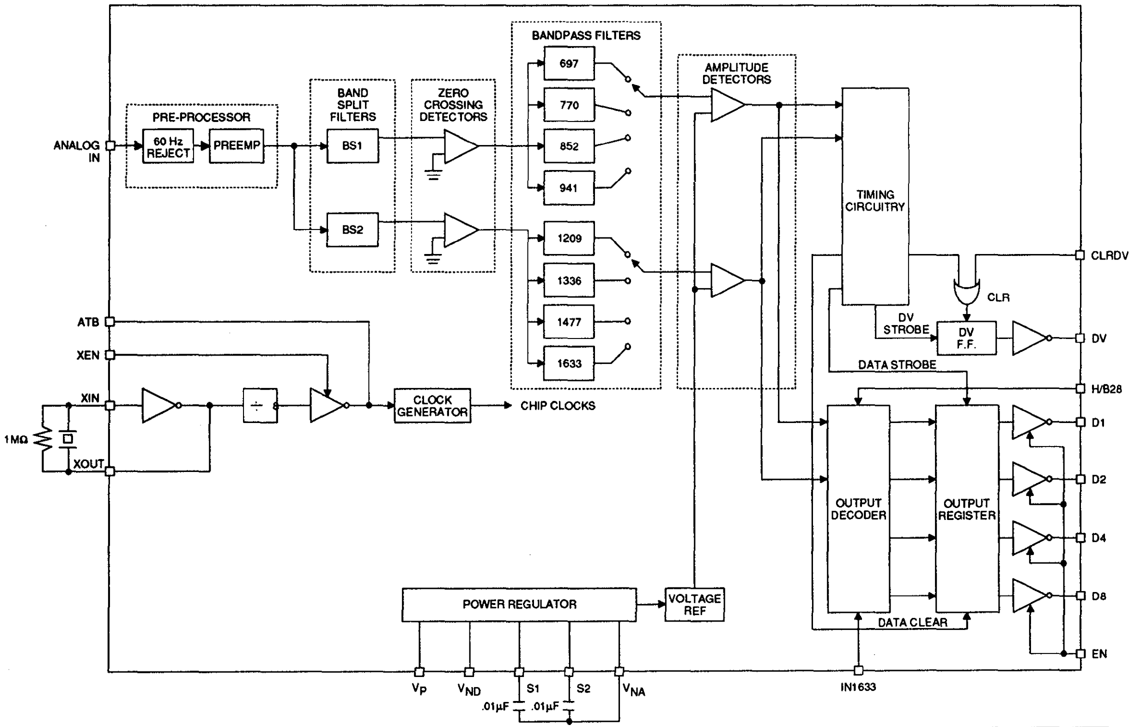
The SSI 75T201 is a complete Dual-Tone Multifrequency (DTMF) receiver detecting a selectable group of 12 or 16 standard digits. No front-end prefiltering is needed. The only external components required are an inexpensive 3.58 MHz television "colorburst" crystal (for frequency reference) and two low-tolerance bypass capacitors. Extremely high system density is made possible by using the clock output of a crystal connected SSI 75T201 receiver to drive the time bases of additional receivers. The SSI 75T201 is a monolithic integrated circuit fabricated with low-power, complementary symmetry MOS (CMOS) processing. It requires only a single low tolerance voltage supply and is packaged in a standard 22-pin DIP.

(Continued)

FEATURES

- **Central office quality**
- **NO front-end band-splitting filters required**
- **Single, low-tolerance, 12-volt supply**
- **Detects either 12 or 16 standard DTMF digits**
- **Uses inexpensive 3.579545 MHz crystal for reference**
- **Excellent speech immunity**
- **Output in either 4-bit hexadecimal code or binary coded 2-of-8**
- **22-pin DIP package for high system density**
- **Synchronous or handshake interface**
- **Three-state outputs**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 75T201 employs state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semicondutor process. The analog input is preprocessed by 60 Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

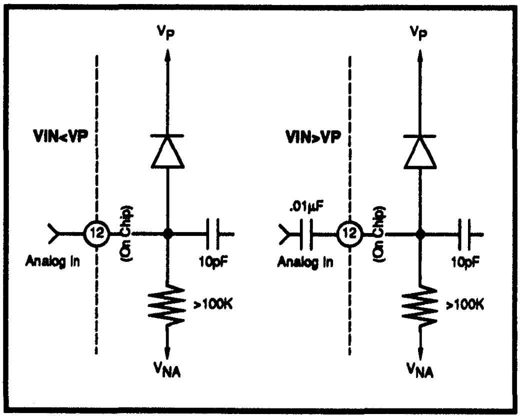


FIGURE 1: Input Coupling

CRYSTAL OSCILLATOR

The SSI 75T201 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T201's may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Twenty-five devices may run off a single crystal-connected SSI 75T201 as shown in Figure 2.

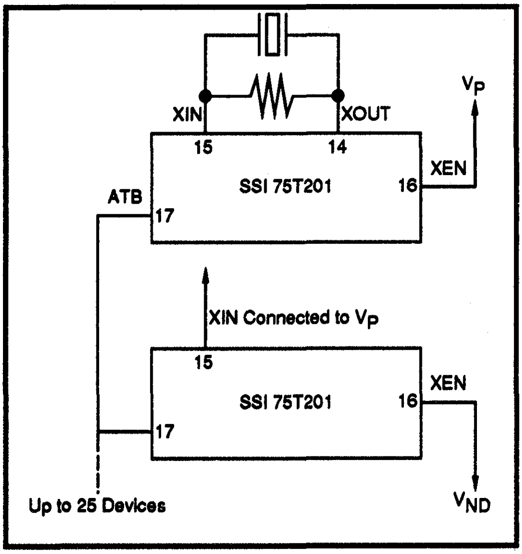


FIGURE 2: Crystal Connections

H/B28

This pin selects the format of the digital output code. When H/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: Output Codes

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633 Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, and D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the H/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever comes first.

INTERNAL BYPASS PINS, S1, S2

In order for the SSI 75T201 DTMF Receiver to function properly, these pins must be bypassed to V_{NA} with 0.01 µF ±20% capacitors.

POWER SUPPLY PINS, V_P, V_{NA}, V_{ND}

The analog (V_{NA}) and digital (V_{ND}) supplies are brought out separately to enhance analog noise immunity on the chip. V_{NA} and V_{ND} should be connected externally as shown in Figure 3.

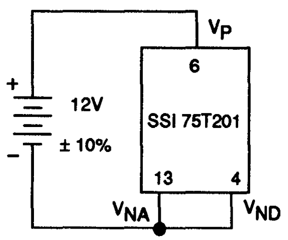


FIGURE 3: 12V System

N/C PINS

These pins have no internal connection and may be left floating.

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

FIGURE 4: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may damage the device. All SSI 75T201 unused inputs must be connected to V_P or V_{ND}, as appropriate.

PARAMETER	RATING	UNIT
DC Supply Voltage - V_P	Referenced to V_{NA}, V_{ND}	+16V
Operating Temperature		-40 to +85°C Ambient
Storage Temperature		-65 to +150°C
Power Dissipation (25°C)		1W
Input Voltage	All inputs except ANALOG IN	(V_P+ 0.5V) to (V_{ND} -0.5V)
ANALOG IN Voltage		(V_P + 0.5V) to (V_P - 22V)
DC Current into any Input		±1.0 mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

($-40°C \leq Ta \leq +85°C$, $V_P - V_{ND} = V_P - V_{NA} = 12V \pm 10\%$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		± (1.5+2 Hz)	±2.3	±3.0	% of *fo*
Amplitude for Detection	each tone	-24		+6	dBm ref. to 600Ω
Twist Tolerance	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-8		+4	dB
60 Hz Tolerance				2	Vrms
Dial Tone Tolerance	"precise" dial tone			0	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 750 µA load	V_{ND}		$V_{ND}+0.5$	V
(except XOUT)	"1" level, 750 µA load	$V_P-0.5$		V_P	V
Digital Inputs	"0" level	V_{ND}		**	V
(except H/B28, XEN)	"1" level	***		V_P	V
Digital Inputs	"0" level	V_{ND}		$V_{ND}+1$	V
H/B28, XEN	"1" level	V_P-1		V_P	V
Power Supply Noise	wide band			25	mVp-p
Supply Current	Ta = 25°C $V_P - V_{NA} = V_P - V_{ND} = 12V \pm 10\%$		29	50	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P - 22$	100 kΩ‖5 pF			

* dB referenced to lowest amplitude tone
** $V_{ND} + 0.3(V_P - V_{ND})$
*** $V_P - 0.3(V_P - V_{ND})$

TIMING CHARACTERISTICS

($-40°C \leq Ta \leq +85°C$, $V_P - V_{ND} = V_P - V_{NA} = 12V \pm 10\%$)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_V	Tone Detection Time		20	25	40	ms
t_{SLH}	Data Overlap of DV Rising Edge	CLRDV = V_{ND}, EN = V_P	7			µs
t_P	Pause Detection Time		25	32	40	ms
t_{DV}	Time between end of Tone and Fall of DV		40	45	50	ms

TIMING CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{shl} Data overlap of DV Falling Edge		4	4.56	4.8	ms
t_{phl} Prop. Delay: Rise of CLRDV to fall of DV	Cl = 300 pF Measured at 50% points			1	µs
Output Enable Time	Cl = 300 pF, Rl = 10K Measured from 50% point of Rising Edge of EN to the 50% point of the data output with Rl to opposite rail.			1	µs
Output Disable Time	Cl = 300 pF, Rl = 1K, ΔV = 1V Measured from 50% point of Falling Edge of EN to time at which output has changed 1V with Rl to opposite rail.			1	µs
Output 10-90% Transition Time	Cl = 300 pF			1	µs

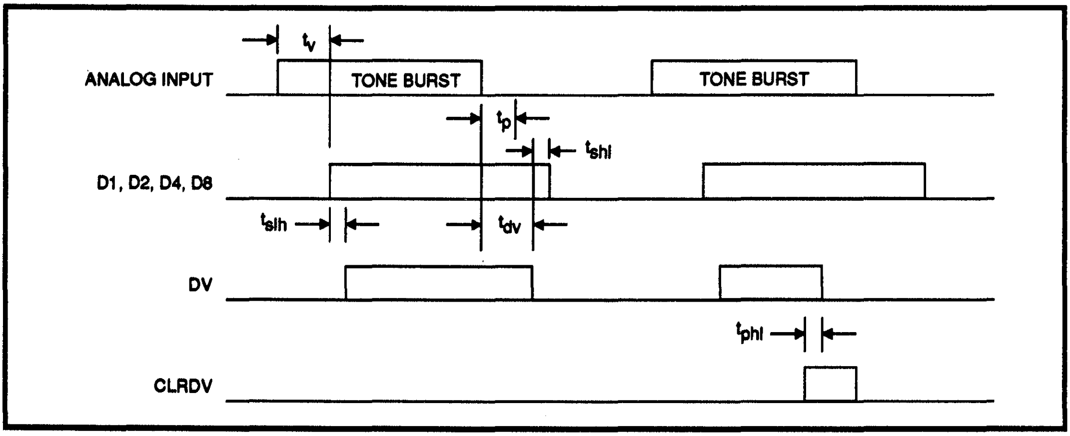


FIGURE 5: Timing Diagram

APPLICATION INFORMATION

TELEPHONE LINE INTERFACE

In applications that use the SSI 75T201 to decode DTMF signals from a phone line, a DAA (Direct Access Arrangement) must be implemented. Equipment intended for connection to the public telephone network must comply with and be registered in accordance with FCC Part 68. For PBX applications refer to EIA Standard RS-464.

Some of the basic guidelines are:

1) Maximum voltage and current ratings of the SSI 75T201 must not be exceeded; this calls for protection from ringing voltage, if applicable, which ranges from 80 to 120 volts RMS over a 20 to 80Hz frequency range.

2) The interface equipment must not breakdown with high-voltage transient tests (including a 2500 volt peak surge) as defined in the applicable document.

3) Phone line termination must be less than 200Ω DC and approximately 600Ω AC (200-3200 Hz).

4) Termination must be capable of sustaining phone line loop current (off-hook condition) which is typically 18 to 120 mA DC.

5) The phone line termination must be electrically balanced with respect to ground.

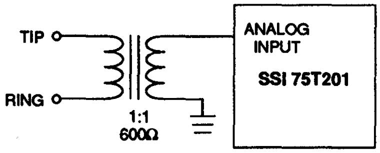


FIGURE 6: Simplified Interface

6) Public phone line termination equipment must be registered in accordance to FCC Part 68 or connected through registered protection circuitry. Registration typically takes about six months.

Figure 6 shows a simplified phone line interface using a 600Ω 1:1 line transformer. Transformers specially designed for phone line coupling are available from many transformer manufacturers.

Figure 7 shows a more featured version of Figure 6. These added options include:

1) A 150-volt surge protector to eliminate high voltage spikes.

2) A Texas Instruments TCM1520A ring detector, optically isolated from the supervisory circuitry.

3) Back-to-back Zener diodes to protect the DTMF (and optional multiplexer Op-Amp) from ringer voltage.

4) Audio multiplexer which allows voice or other audio to be placed on the line (a recorded message, for example) and not interfere with incoming DTMF tone detection.

An integrated voice circuit may also be implemented for line coupling, such as the Texas Instruments TCM1705A, however, this approach is typically more expensive than using a transformer as shown above.

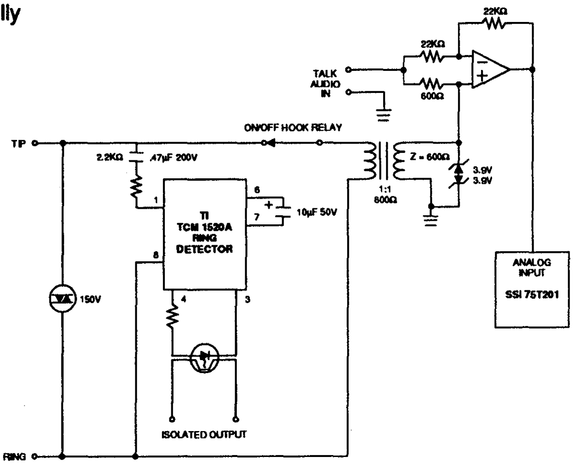
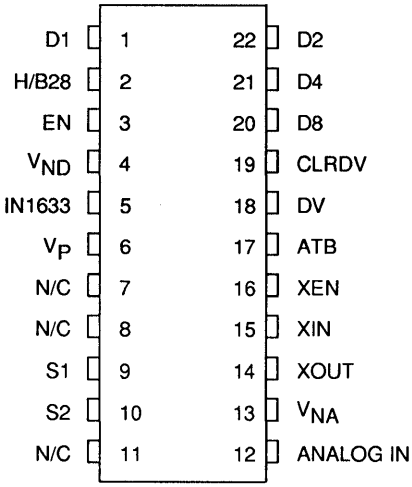


FIGURE 7: Full Featured Interface

SSI 75T201
Integrated
DTMF Receiver

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



22-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T201 22-Pin Plastic DIP	75T201 - IP	75T201 - IP

silicon systems®
A TDK Group Company

SSI 75T202/203
5V Low-Power DTMF Receiver

October 1991

DESCRIPTION

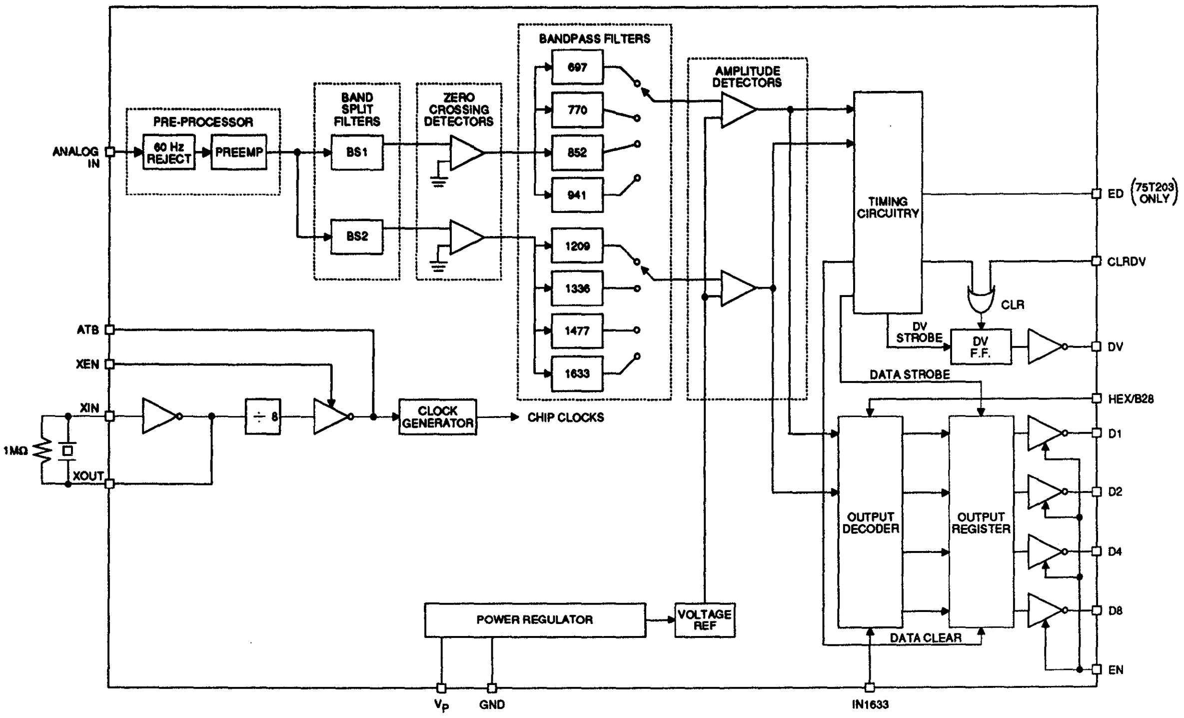
The SSI 75T202 and 75T203 are complete Dual-Tone Multifrequency (DTMF) receivers detecting a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally required components are an inexpensive 3.58-MHz television "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is made possible by using the clock output of a crystal-connected SSI 75T202 or 75T203 receiver to drive the time bases of additional receivers. Both are monolithic integrated circuits fabricated with low-power, complementary symmetry MOS (CMOS) processing. They require only a single low tolerance voltage supply and are packaged in a standard 18-pin plastic DIP.

(Continued)

FEATURES

- **Central office quality**
- **NO front-end band-splitting filters required**
- **Single, low-tolerance, 5-volt supply**
- **Detects either 12 or 16 standard DTMF digits**
- **Uses inexpensive 3.579545-MHz crystal for reference**
- **Excellent speech immunity**
- **Output in either 4-bit hexadecimal code or binary coded 2-of-8**
- **18-pin DIP package for high system density**
- **Synchronous or handshake interface**
- **Three-state outputs**
- **Early detect output (SSI 75T203 only)**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 75T202 and 75T203 employ state-of-the-art circuit technology to combine digital and analog functions on the same CMOS chip using a standard digital semicondutor process. The analog input is pre-processed by 60-Hz reject and band splitting filters and then hard-limited to provide AGC. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

The SSI 75T202 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics less then -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T202 and 75T203 contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T202's (or 75T203's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 75T202 or 75T203 as shown in Figure 2.

HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The table below describes the two output codes.

Hexadecimal					Binary Coded 2-of-8				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	2	0	0	0	1
3	0	0	1	1	3	0	0	1	0
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	1	0	0	0
8	1	0	0	0	8	1	0	0	1
9	1	0	0	1	9	1	0	1	0
0	1	0	1	0	0	1	1	0	1
*	1	0	1	1	*	1	1	0	0
#	1	1	0	0	#	1	1	1	0
A	1	1	0	1	A	0	0	1	1
B	1	1	1	0	B	0	1	1	1
C	1	1	1	1	C	1	0	1	1
D	0	0	0	0	D	1	1	1	1

TABLE 1: Output Codes

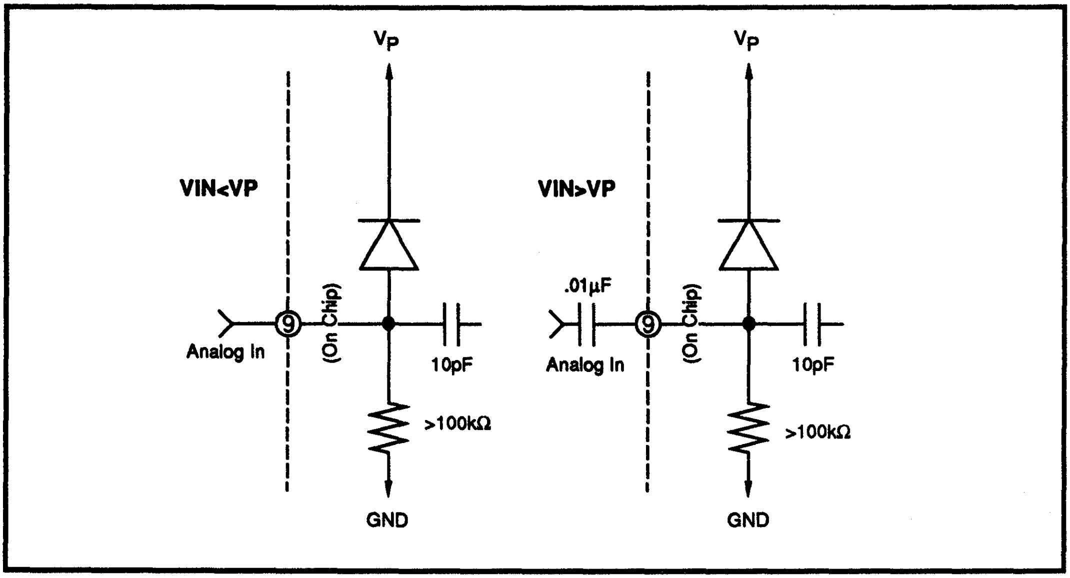


FIGURE 1: Input Coupling

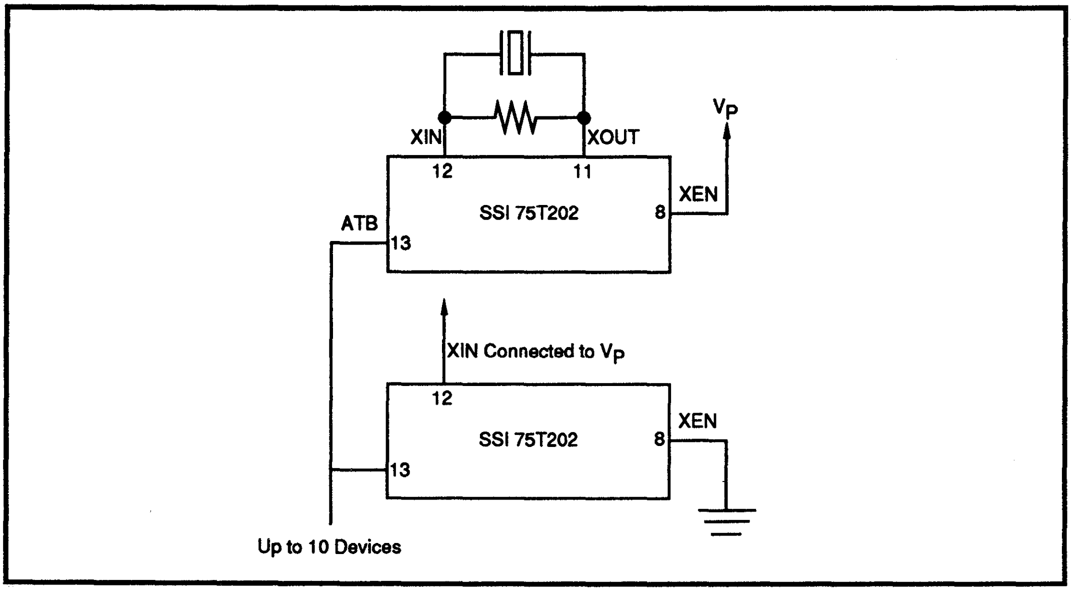


FIGURE 2: Crystal Connections

IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or the CLRDV is raised high, whichever is earlier.

ED (SSI 75T203 only)

The ED output goes high as soon as the SSI 75T203 begins to detect a DTMF tone pair and falls when the 75T203 begins to detect a pause. The D1, D2, D4, and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

N/C PINS

These pins have no internal connection and may be left floating.

DTMF DIALING MATRIX

See Figure 3. Please make note that column 3 is for special applications and is not normally used in telephone dialing.

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

FIGURE 3: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may damage the device. All SSI 75T202/203 unused inputs must be connected to V_P or GND, as appropriate.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P		+7V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		65mW
Input Voltage	All inputs except ANALOG IN	(V_P + .5V) to -.5V
ANALOG IN Voltage		(V_P + .5V) to (V_P - 10V)
DC Current into any Input		±1.0mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

($-40°C \leq T_A \leq +85°C$, $V_P = 5V \pm 10\%$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	% of fo
Amplitude for Detection	each tone	-32		-2	dBm ref. to 600Ω
Twist Tolerance	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-10		+10	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 400µA load	0		0.5	V
(except XOUT)	"1" level, 200µA load	V_P-0.5		V_P	V
Digital Inputs	"0" level	0		0.3V_P	V
	"1" level	0.7V_P		V_P	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \geq V_{IN} \geq V_P - 10$	100kΩ‖15pF			

* dB referenced to lowest amplitude tone

SSI 75T202/203 TIMING

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON} Tone Time	for detection	40	-	-	ms
	for rejection	-	-	20	ms
t_{OFF} Pause Time	for detection	40	-	-	ms
	for rejection	-	-	20	ms
t_D Detect Time		25	-	46	ms
t_R Release Time		35	-	50	ms
t_{SU} Data Setup Time		7	-	-	µs
t_H Data Hold Time		4.2	-	5.0	ms
t_{CL} DV Clear Time		-	160	250	ns
t_{PW} CLRDV Pulse Width		200	-	-	ns
t_{ED} ED Detect Time		7	-	22	ms
t_{ER} ED Release Time		2	-	18	ms
Output Enable Time	C_L = 50pF, R_L = 1kΩ	-	-	200	ns
Output Disable Time	C_L = 35pF, R_L = 500Ω	-	-	200	ns
Output Rise Time	C_L = 50pF	-	-	200	ns
Output Fall Time	C_L = 50pF	-	160	200	ns

SSI 75T202/203 TIMING (Continued)

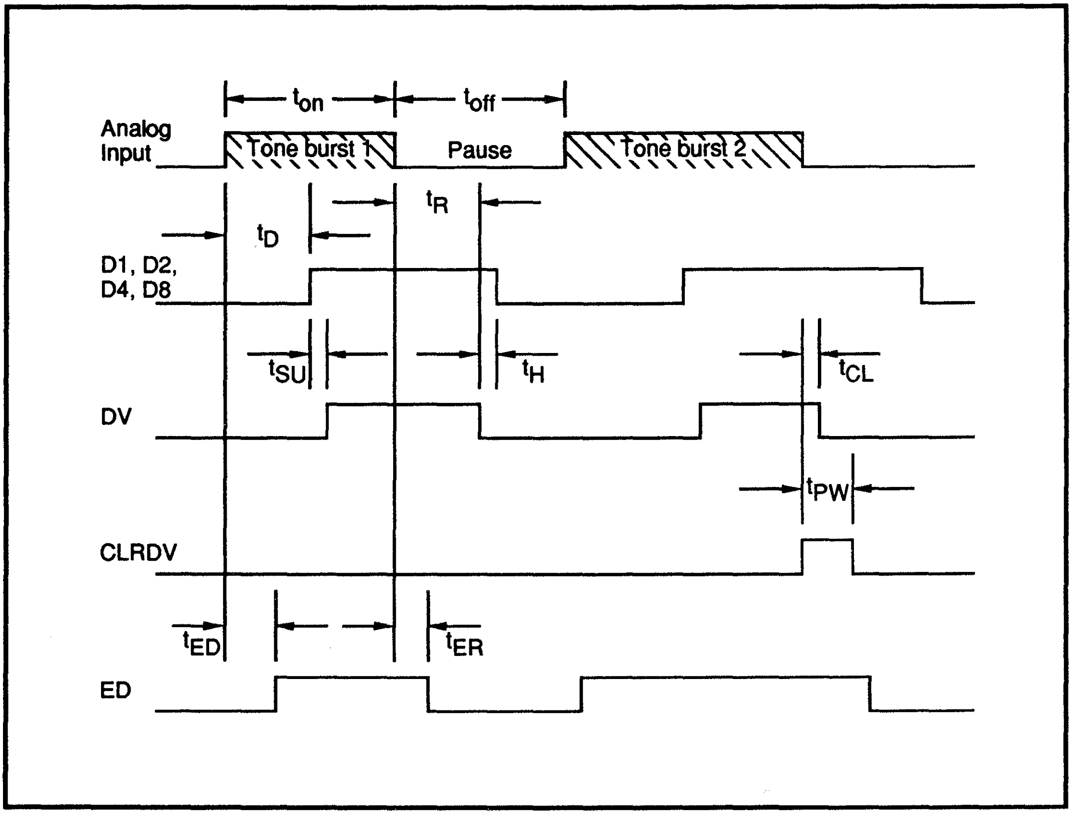
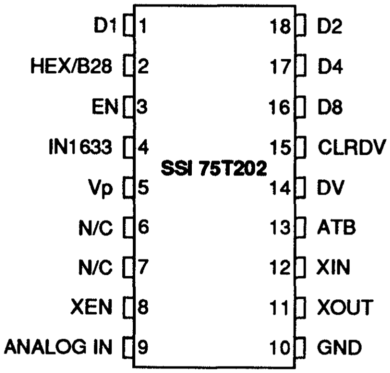


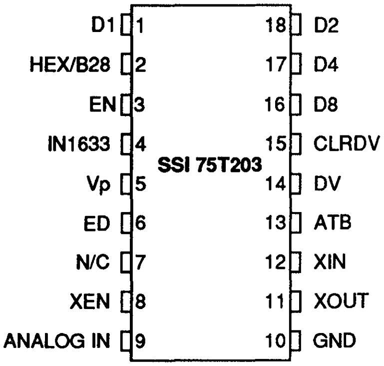
FIGURE 4: Timing Diagram

SSI 75T202/203
5V Low-Power
DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



18 - Pin DIP
SSI 75T202



18 - Pin DIP
SSI 75T203

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T202 18-pin Plastic DIP	75T202-IP	75T202-IP
SSI 75T203 18-pin Plastic DIP	75T203-IP	75T203-IP

silicon systems®
A TDK Group Company

SSI 75T204
5V Low-Power Subscriber DTMF Receiver

October 1991

DESCRIPTION

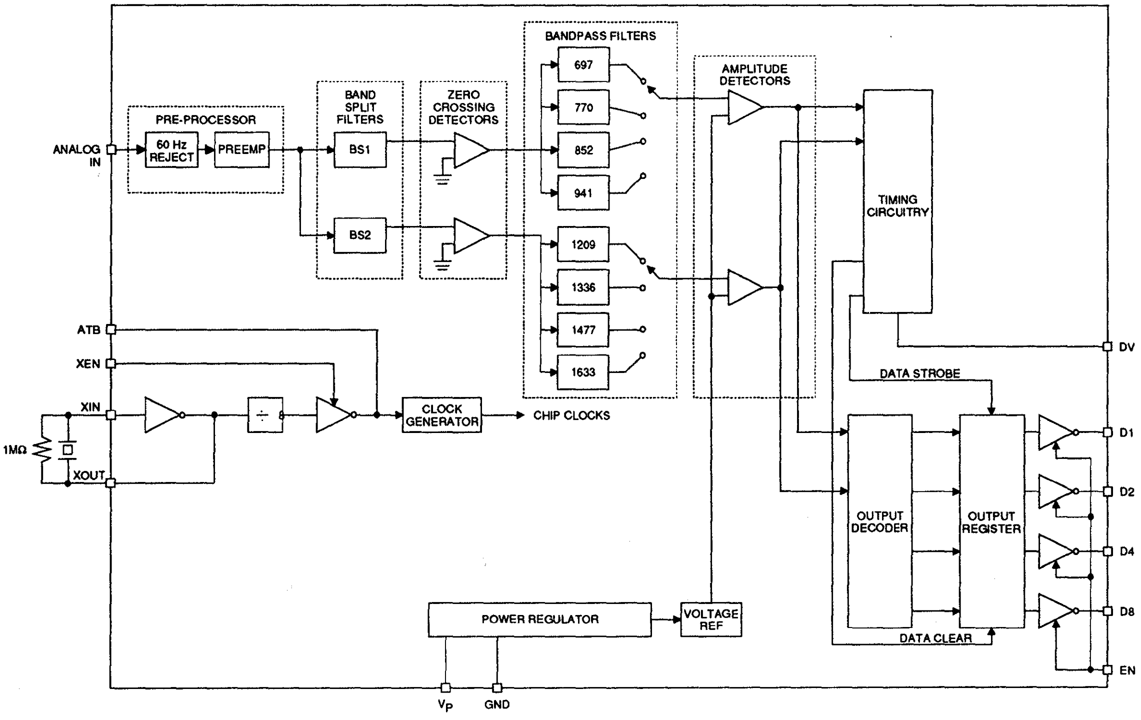
The SSI 75T204 is a complete Dual-Tone Multifrequency (DTMF) receiver that detects 16 standard digits. No front-end pre-filtering is needed. The only external components required are an inexpensive 3.58-MHz television "colorburst" crystal for frequency reference and a bias resistor. An Alternate Time Base (ATB) is provided to permit operation of up to 10 SSI 75T204's from a single crystal. The SSI 75T204 employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering, and digital circuitry on the same CMOS chip. The analog input signal is pre-processed by 60-Hz reject and band split filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to

(Continued)

FEATURES

- **Intended for applications with less requirements than the SSI 75T202**
- **14-pin plastic DIP or 16-pin SO package for high system density**
- **NO front-end band-splitting filters required**
- **Single low-tolerance 5-volt supply**
- **Detects all 16 standard DTMF digits.**
- **Uses an inexpensive 3.579545-MHz crystal**
- **Excellent speech immunity**
- **Output in 4-bit hexadecimal code**
- **Three-state outputs for microprocessor interface**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

measure the tone and pause durations and to provide output timing and decoding. The outputs interface directly to standard CMOS circuitry and are three-state enabled to facilitate bus-oriented architectures.

ANALOG IN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

The SSI 75T204 is designed to accept sinusoidal input wave forms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics less then -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The SSI 75T204 contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "colorburst" crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other SSI 75T204's (or 75T202's) may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single crystal-connected SSI 75T204 (or 75T202) as shown in Figure 2.

OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected (DV is high) and they are then cleared when a valid pause is timed. The hexadecimal codes are described in Table 1.

DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs.

N/C PINS

These pins have no internal connection and may be left floating.

Output Code				
Digit	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

TABLE 1: Output Codes

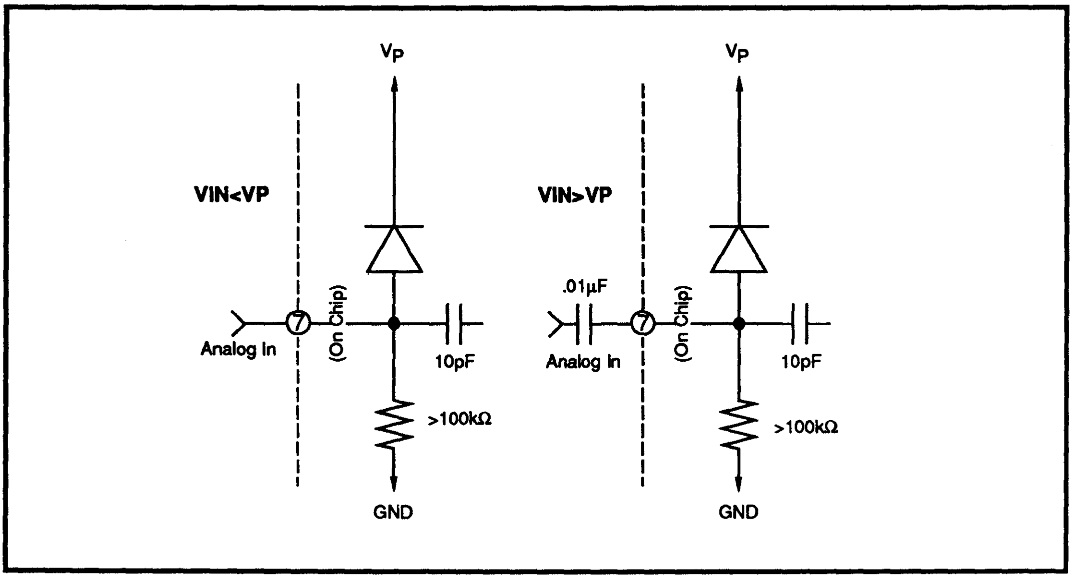


FIGURE 1: Input Coupling

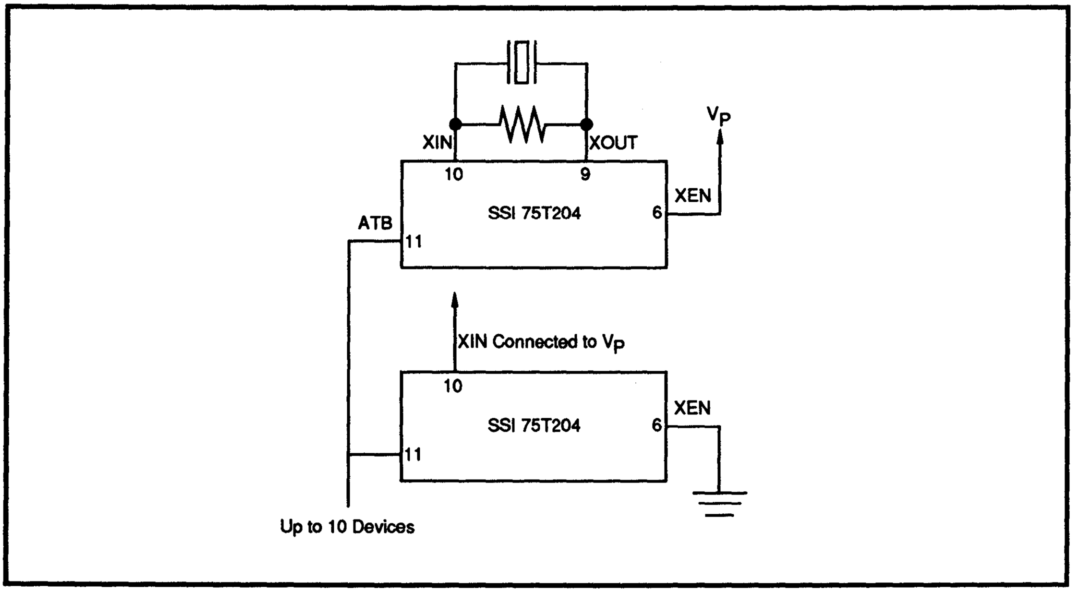


FIGURE 2: Crystal Connections

DTMF DIALING MATRIX

See Figure 3. Please note that column 3 is for special applications and is not normally used in telephone dialing.

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

FIGURE 3: DTMF Dialing Matrix

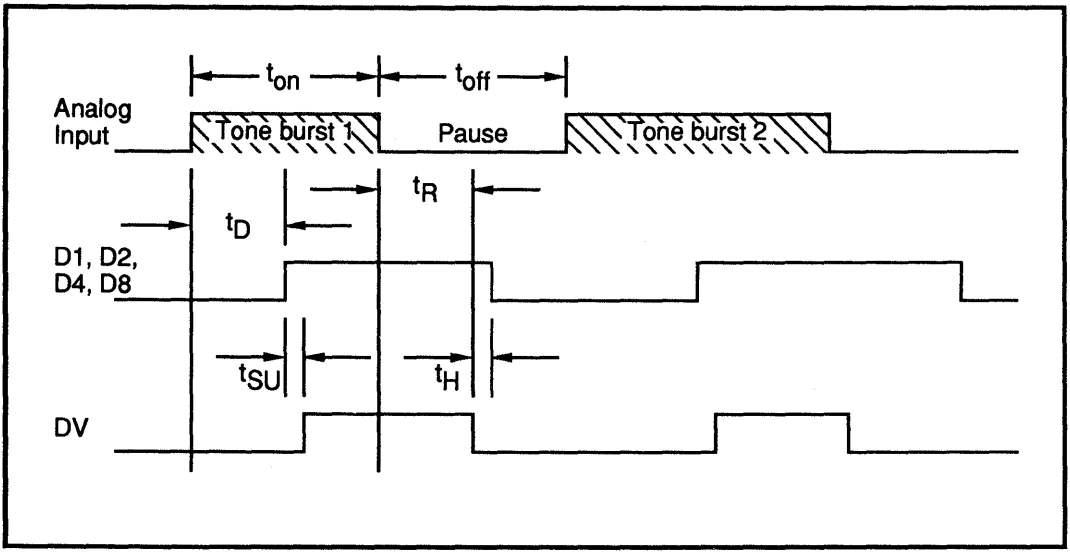


FIGURE 4: Timing Diagram

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697 Hz	Column 0 = 1209 Hz
Row 1 = 770 Hz	Column 1 = 1336 Hz
Row 2 = 852 Hz	Column 2 = 1477 Hz
Row 3 = 941 Hz	Column 3 = 1633 Hz

SSI 75T204 TIMING (Refer to Figure 4.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
t_{ON}	Tone Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_{OFF}	Pause Time	for detection	40	-	-	ms
		for rejection	-	-	20	ms
t_D	Detect Time		25	-	46	ms
t_R	Release Time		35	-	50	ms
t_{SU}	Data Setup Time		7	-	-	µs
t_H	Data Hold Time		4.2	-	5.0	ms
	Output Enable Time	C_L = 50pF, R_L = 1kΩ	-	-	200	ns
	Output Disable Time	C_L = 35pF, R_L = 500Ω	-	-	200	ns
	Output Rise Time	C_L = 50pF	-	-	200	ns
	Output Fall Time	C_L = 50pF	-	-	200	ns

APPLICATION INFORMATION

The SSI 75T204 will tolerate total input RMS noise up to 12dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the SSI 75T204 unnecessary. However, noise near the 56kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28kHz, the simple RC filter shown in Figure 5 may be employed to band limit the incoming signal.

Noise will also be reduced by placing a grounded trace around the XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case leave XOUT floating.

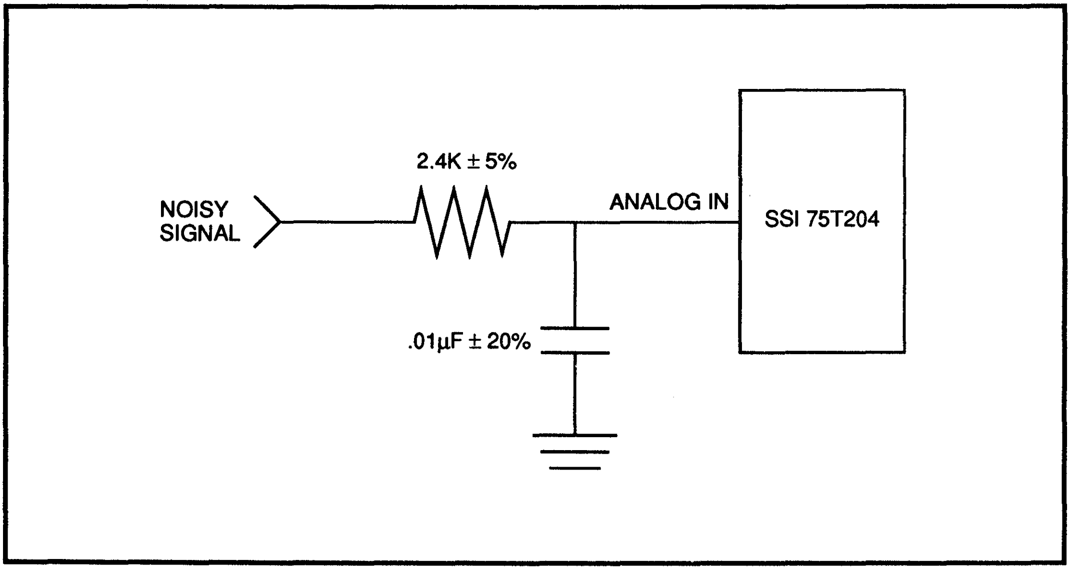


FIGURE 5: RC Filter

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may damage the device. All SSI 75T204 unused inputs must be connected to V_P or GND, as appropriate.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage - V_P		+7V
Operating Temperature		-40°C to +85°C Ambient
Storage Temperature		-65°C to +150°C
Power Dissipation (25°C)		65mW
Input Voltage	All inputs except ANALOG IN	(V_P + 0.5V) to -0.5V
ANALOG IN Voltage		(V_P + .5V) to (V_P - 10V)
DC Current into any Input		±1.0mA
Lead Temperature	Soldering, 10 sec.	300°C

ELECTRICAL CHARACTERISTICS

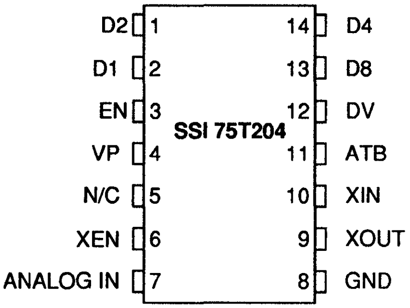
($-40°C \le T_A \le +85°C$, $V_P = 5V \pm 10\%$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	% of fo
Amplitude for Detection	each tone	-32		-2	dBm ref. to 600Ω
Twist Tolerance	$\text{Twist} = \frac{\text{High Tone}}{\text{Low Tone}}$	-10		+10	dB
60-Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	"precise" dial tone			0dB	dB*
Talk Off	MITEL tape #CM 7290		2		hits
Digital Outputs	"0" level, 400µA load	0		0.5	V
(except XOUT)	"1" level, 200µA load	V_P-0.5		V_P	V
Digital Inputs	"0" level	0		0.3V_P	V
	"1" level	0.7V_P		V_P	V
Power Supply Noise	wide band			10	mV p-p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL tape #CM 7290			-12	dB*
Input Impedance	$V_P \ge V_{IN} \ge V_P-10$	100KΩ||15pF			

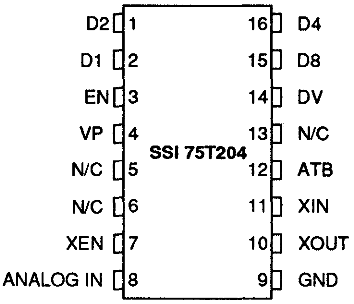
* dB referenced to lowest amplitude tone

SSI 75T204
5V Low-Power Subscriber DTMF Receiver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



14 - Pin DIP



16 - Lead SOL

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T204 14-pin PDIP	75T204-IP	75T204-IP
SSI 75T204 16-lead SOL	75T204-IL	75T204-IL

silicon systems®
A TDK Group Company

SSI 75T2089/2090/2091
DTMF Transceivers

DESCRIPTION

Silicon Systems' SSI 75T2089/2090/2091 are complete Dual-Tone Multifrequency (DTMF) Transceivers that can both generate and detect all 16 DTMF tone-pairs. These ICs integrate the performance-proven SSI 75T202 DTMF receiver with a DTMF generator circuit.

The DTMF receiver electrical characteristics are identical to the standard SSI 75T202 device characteristics. The DTMF generator provides performance similar to the Mostek MK5380, but with an improved (tighter) output amplitude range specification and with the addition of independent latch and reset controls.

An additional feature of the SSI 75T2090/2091 is "imprecise" call progress detector. The detector detects the presence of signals in the 305-640 Hz band.

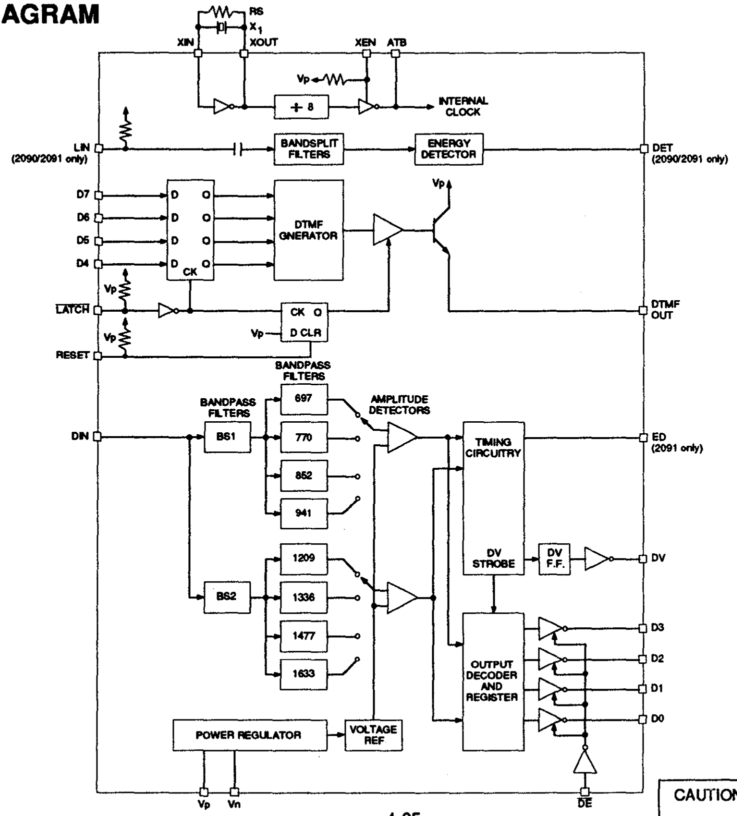
(Continued)

FEATURES

November 1991

- **DTMF Generator and Receiver on one-chip**
- **Call progress detection (2090/2091 only)**
- **Early detect output (2091 only)**
- **DTMF Receiver exhibits excellent speech immunity**
- **Analog input range from –32 to –2 dBm (ref 600 Ω)**
- **Three-state outputs (4-bit hexadecimal) from DTMF Receiver**
- **AC coupled, internally biased analog input**
- **Latched DTMF Generator inputs**
- **DTMF output typ. –8 dBm (Low Band) and –5.5 dBm (High Band)**
- **Easy interface for microprocessor dialing**
- **Uses inexpensive 3.579545 MHz crystal for reference**
- **Low-power 5 volt CMOS**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

The SSI 75T2091 also incorporates an early detect function which is useful in multi-channel radio scanning applications. The only external components necessary for the SSI 75T2089/2090/2091 are a 3.58 MHz "colorburst" crystal with a parallel 1MΩ resistor. This provides the time base for digital functions and switched-capacitor filters in the device. No external filtering is required.

CIRCUIT OPERATION

RECEIVER

The DTMF Receiver in the SSI 75T2089/2090/2091 detects the presence of a valid tone pair (indicating a single dialed digit) on a telephone line or other transmission medium. The analog input is pre-processed by 60 Hz reject and band-splitting filters, then hard-limited to provide Automatic Gain Control. Eight bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. The outputs will drive standard CMOS circuitry, and are three-state enabled to facilitate bus-oriented architectures.

DIN

This pin accepts the analog input. It is internally biased so that the input signal may be AC coupled. The input may be DC coupled as long as it does not exceed the positive supply. Proper input coupling is illustrated in Figure 1.

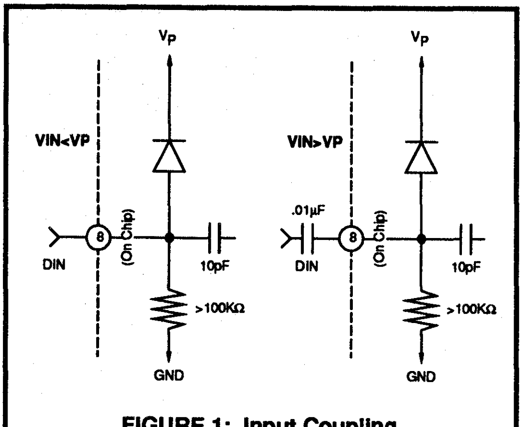


FIGURE 1: Input Coupling

The IC is designed to accept sinusoidal input waveforms but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics greater than -20 dB below the fundamental.

CRYSTAL OSCILLATOR

The IC contains an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" crystal. The crystal is placed between XIN and XOUT in parallel with a 1MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the crystal oscillator, the frequency accuracy of all portions of the IC depends on the time base tolerance. The SSI DTMF Receiver frequency response and timing is specified for a time base accuracy of at least ±0.005%. ATB is a clock output with the frequency of 1/8 of crystal. Other devices may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively, XOUT is left floating. XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. Ten devices may run off a single crystal-connected transceiver as shown in Figure 2.

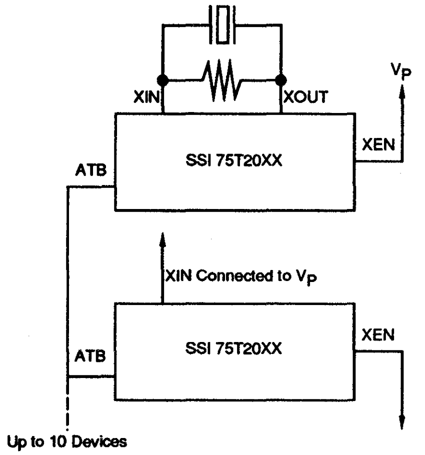


FIGURE 2: Crystal Connections

RECEIVER OUTPUTS AND THE $\overline{\text{DE}}$ PIN

Outputs D0, D1, D2, D3 are CMOS push-pull when enabled ($\overline{\text{DE}}$ low) and open-circuited (high impedance) when disabled ($\overline{\text{DE}}$ high). These digital outputs provide the hexadecimal code corresponding to the detected digit. Figure 3 shows that code.

The digital outputs become valid and DV signals a detection after a valid tone pair has been sensed. The outputs and DV are cleared when a valid pause has been timed.

	Hexadecimal Code			
Digit In Out	D7 D3	D6 D2	D5 D1	D4 D0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

FIGURE 3

ED OUTPUT (75T2091 only)

The ED output goes high as soon as the SSI 75T2091 begins to detect a DTMF tone pair and falls when the SSI 75T2091 begins to detect a pause. The D1, D2, D4, and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.

GENERATOR

The DTMF generator responds to a hexadecimal code input with a valid tone pair. Pins D4-D7 are the data inputs for the generator. A high to low transition on $\overline{\text{LATCH}}$ causes the hexadecimal code to be latched internally and generation of the appropriate DTMF tone pair to begin. The DTMF output is disabled by a high on RESET and will not resume until new data is latched in.

DIGITAL INPUTS

The D4, D5, D6, D7, $\overline{\text{LATCH}}$, RESET inputs to the DTMF generator may be interfaced to open-collector TTL with a pull-up resistor or standard CMOS. These inputs follow the same hexadecimal code format as the DTMF receiver output. Figure 4 shows the code for each digit. The dialing matrix and detection frequency table below list the frequencies of the digits.

	Col 0	Col 1	Col 2	Col 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

NOTE: Column 3 is for special applications and is not normally used in telephone dialing.

FIGURE 4: DTMF Dialing Matrix

DETECTION FREQUENCY

Low Group f_0	High Group f_0
Row 0 = 697Hz	Column 0 = 1209Hz
Row 1 = 770Hz	Column 1 = 1336Hz
Row 2 = 852Hz	Column 2 = 1477Hz
Row 3 = 941Hz	Column 3 = 1633Hz

DTMF OUT

The output amplitude characteristics listed in the specifications are given for a supply voltage of 5.0V. However, the output level is directly proportional to the supply, so variations in it will affect the DTMF output. A recommended line interface for this output is shown in Figure 5.

CALL PROGRESS DETECTION (75T2090/2091)

The 75T2090/2091 have a Call Progress Detector that consists of a bandpass filter and an energy detector for turning the on/off cadences into a microprocessor compatible signal.

DET OUTPUT (75T2090/2091)

The output is TTL compatible and will be of a frequency corresponding to the various candences of Call Progress signals such as: on 0.5 sec/off 0.5 sec for a busy tone, on 0.25 sec/off 0.25 sec for a reorder tone and on 0.8-1.2 sec/off 2.7-3.3 sec for an audible ring tone.

LIN INPUT (75T2090/2091)

This analog input accepts the call progress signal and should be used in the same manner as the receiver input DIN.

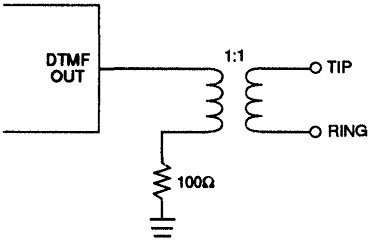


FIGURE 5: DTMF Output

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operating above absolute maximum ratings may damage the device.

PARAMETER	RATING	UNIT
DC Supply Voltage (Vp - Vn)	+7	V
Voltage at any Pin (Vn = 0)	-0.3 to Vp + 0.3	V
DIN Voltage	Vp + 0.5 to Vp - 10	V
Current through any Protection Device	±20	mA
Operating Temperature Range	-40 to + 85	°C
Storage Temperature	-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage		4.5		5.5	V
Power Supply Noise (wide band)				10	mV pp
Ambient Temperature		-40		+85	°C
Crystal Frequency (F Nominal = 3.579545MHz)		-0.01		+0.01	%
Crystal Shunt Resistor		0.8		1.2	MΩ
DTMF OUT Load Resistance		100			Ω

DIGITAL AND DC REQUIREMENTS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. The specifications do not apply to the following pins: LIN, DIN, XIN, XOUT, and DTMF OUT. Positive current is defined as entering the circuit. Vn = 0 unless otherwise stated.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current*			15	30	mA
Power Dissipation				225	mW
Input Voltage High		0.7Vp			V
Input Voltage Low				0.3Vp	V
Input Current High				10	µA
Input Current Low		-10			µA
Output Voltage High	Ioh = -0.2mA	Vp-0.5			V
Output Voltage Low	Iol = +0.4mA			Vn+0.5	V
* with DTMF output disabled					

DTMF RECEIVER: Electrical Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Frequency Detect Bandwidth		±(1.5+2Hz)	±2.3	±3.5	%Fo
Amplitude for Detection	Each Tone	-32		-2	dBm/tone
Twist Tolerance		-10		+10	dB
60Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	Precise Dial Tone			0	dB*
Speech Immunity	MITEL Tape #CM7290		2		hits
Noise Tolerance	MITEL Tape #CM7290			-12	dB*
Input Impedance		100			KΩ
* Referenced to lowest amplitude tone					

DTMF RECEIVER: Timing Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TON Tone Time for Detect		40			ms
TON Tone Time for No Detect				20	ms
TOFF Pause Time for Redetection		40			ms
TOFF Pause Time for Bridging				20	ms
TD1 Detect Time		25		46	ms
TR1 Release Time		35		50	ms

DTMF RECEIVER: Timing Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TSU1 Data Set Up Time		7			µs
THD1 Data Hold Time		4.2		5.0	ms
TED ED Detect Time	75T2091 only	7		22	ms
BER ED Release Time	75T2091 only	2		18	ms
Output Enable Time				200	ns
Output Disable Time				200	ns

DTMF GENERATOR: Electrical Characteristics

Frequency Accuracy		-1.0		+1.0	%Fo
Output Amplitude	R1 = 100Ω to Vn, Vp - Vn = 5.0V				
Low Band		-9.2		-7.2	dBm
High Band		-6.6		-4.6	dBm
Output Distortion	DC to 50 kHz			-20	dB

DTMF GENERATOR: Timing Characteristics

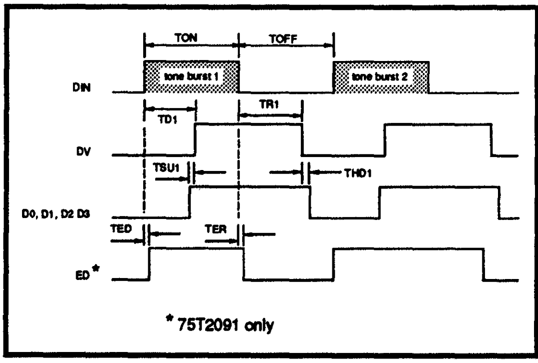
TSTART Start-Up Time				2.5	µs
TSU2 Data Set-Up Time		100			ns
THD2 Data Hold Time		50			ns
TRP RESET Pulse Width		100			ns
TPW $\overline{\text{LATCH}}$ Pulse Width		100			ns

CALL PROGRESS DETECTOR: Electrical Characteristics (75T2090/2091 only)

Amplitude for Detection	305 Hz-640 Hz	-40		0	dBm
Amplitude for No Detection	305 Hz-640 Hz			-50	dBm
	f>2200 Hz, <160 Hz			-25	dBm
Detect Output	Logic 0			.5	V
	Logic 1	4.5			V
"LIN" Input	Max. Voltage	VDD-10		VDD	V
Input Impedance	500 Hz	100			kΩ

CALL PROGRESS DETECTOR: Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TON Signal Time for Detect		40			ms
TON Signal Time for No Detect				10	ms
TOFF Interval Time for Detect		40			ms
TOFF Interval Time for No Detect				20	ms
TD2 Detect Time				40	ms
TR2 Release Time				40	ms



* 75T2091 only

FIGURE 6: DTMF Decoder

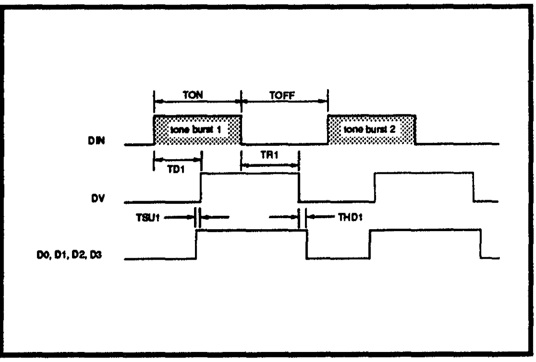
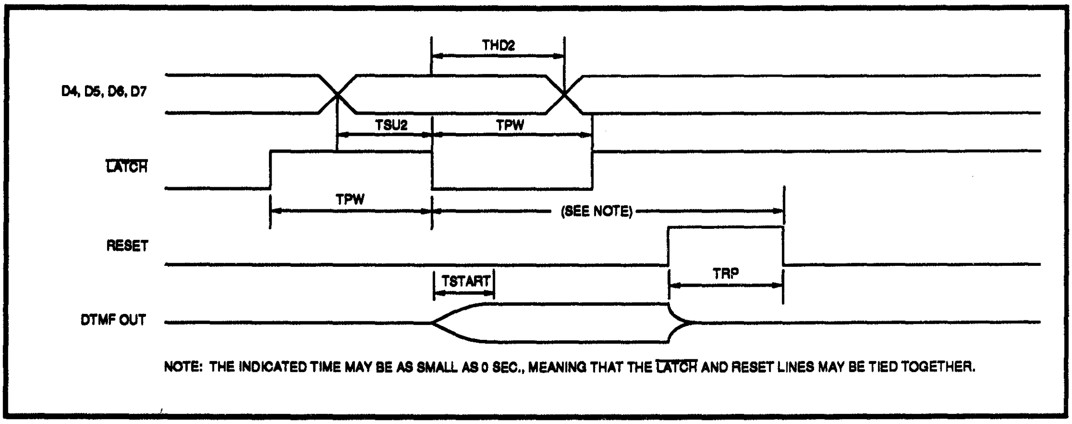


FIGURE 7: Call Progress Detector (75T2090/2091 only)

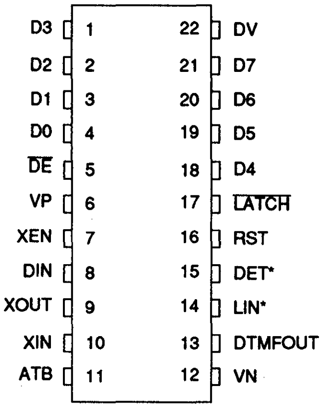


NOTE: THE INDICATED TIME MAY BE AS SMALL AS 0 SEC., MEANING THAT THE $\overline{\text{LATCH}}$ AND RESET LINES MAY BE TIED TOGETHER.

FIGURE 8: DTMF Generator

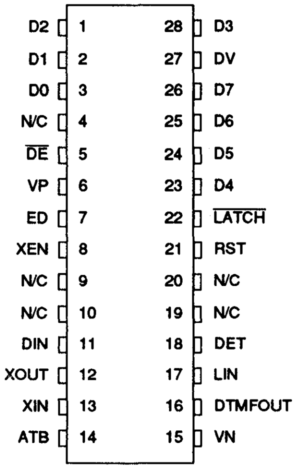
PACKAGE PIN DESIGNATIONS

(Top View)

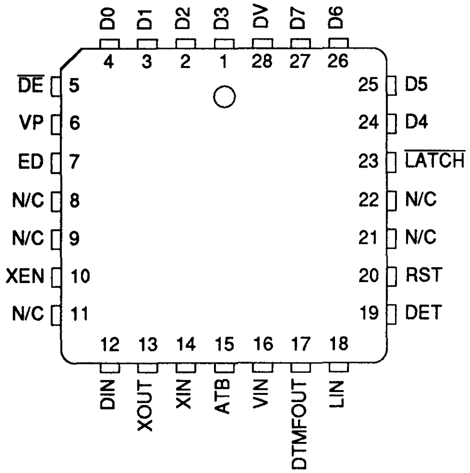


* 75T2090 only

75T2089/2090
22-Pin DIP



75T2091
28-Pin DIP



75T2091
28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T2089		
22-Pin Plastic DIP	75T2089 - IP	75T2089 - IP
SSI 75T2090		
22-Pin DIP	75T2090 - IP	75T2090 - IP
SSI 75T2091		
28-Pin Plastic DIP	75T2091 - IP	75T2091 - IP
28-Pin PLCC	75T2091 - IH	75T2091 - IH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

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SSI 75T980
Call Progress Tone Detector

July 1992

DESCRIPTION

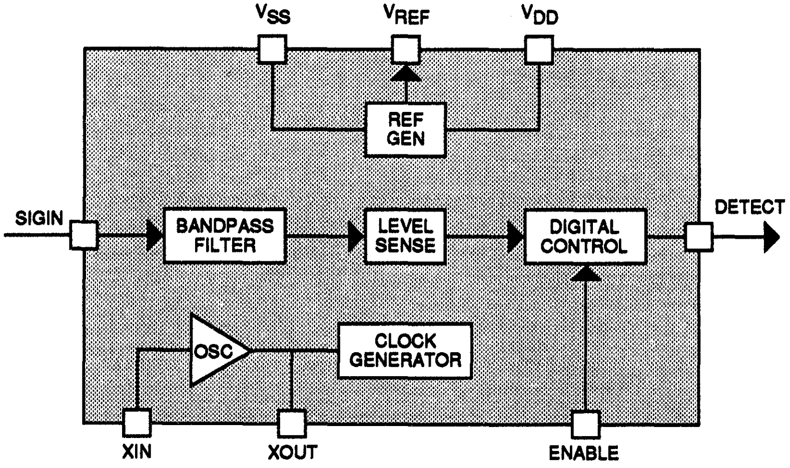
The SSI 75T980 Call Progress Tone Detector circuit allows automatic equipment to monitor tones in dial telephone systems that relate to the routing of calls. Such tones commonly include dial tones, circuits-busy tones, station-busy tones, audible ringing tones and others. By sensing signals in the range of 315 to 640 Hz, the SSI 75T980 does not require the use of precision tones to function. This means that tones which vary with location or call destination can be detected regardless of their exact frequency.

The low power CMOS switched capacitor filters used in the SSI 75T980 derive their accuracy from a 3.58 MHz clock, which in turn may be derived from other devices in the system being designed. The SSI 75T980 is available in a plastic 8-pin DIP and 16-pin SO packages.

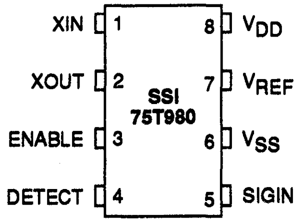
FEATURES

- **Detects tones throughout the telephone progress supervision band (315 to 640 Hz)**
- **Sensitivity to -38 dBm**
- **Dynamic range over 36 dB**
- **40 ms minimum detect (50 ms to output)**
- **Single supply CMOS (low power)**
- **Supply range 4.5 to 5.5 VDC**
- **Uses 3.58 MHz crystal or external clock**
- **8-pin DIP and 16-pin SO packages**
- **Second source of Teltone M-980**

BLOCK DIAGRAM



PIN DIAGRAMS



8-pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
SIGIN	I	Accepts analog input signal. See "Electrical Characteristics" for voltage levels, and "Timing Characteristics" for timing.
DETECT	O	Call progress detect output. Goes to logic "1" when signal in 315-640 Hz band is sensed. See "Timing Characteristics."
ENABLE	I	Application of logic "1" on this pin enables the output; logic "0" disables output.
VREF	O	Supplies voltage at half VDD for voltage reference of on-chip op amps.
XIN, XOUT	I	Crystal connections to on-chip oscillator circuit.
VDD	-	Positive power supply connection
Vss	-	Negative power supply connection

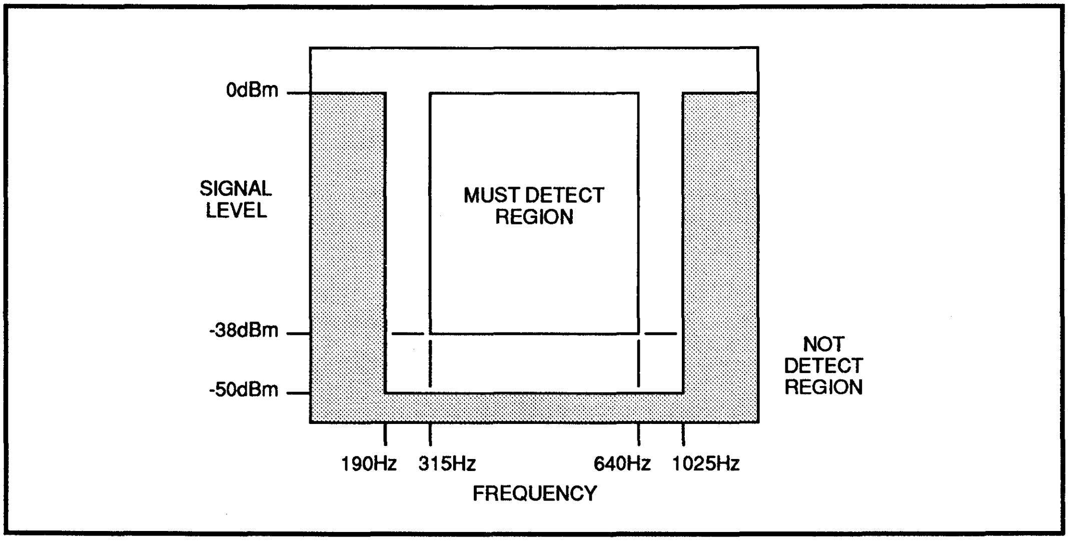


FIGURE 1: Detect and Reject Regions

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
DC Supply Voltage	VDD–Vss	16.0V
Input Voltage	All inputs except SIGNAL IN	(VDD + 0.5V) to (Vss – 0.5V)
SIGNAL IN Voltage		(VDD + 0.5V) to (Vss – 22V)
Storage Temperature		–65°C to 150°C
Operating Temperature		0°C to 70°C
Lead Temperature	Soldering, 5 sec.	260°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, VDD – Vss = 4.5V to 5.5V, dBm is referenced to 600Ω)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Supply Current	VDD – Vss = 5V	-	4	10	mA
Signal level for detection	315-640 Hz	–38	-	0	dBm
Signal level for rejection	315-640 Hz	-	-	–50	dBm
	f >1025 Hz, *f* <190 Hz	-	-	0	dBm
DETECT output (Iout = +1mA)	Logic 0	-	-	0.5	V
	Logic 1	4.5	-	-	V
ENABLE, XIN input (Iin=10µA)	Logic 0	Vss	-	Vss+0.2	V
	Logic 1	VDD–0.2	-	VDD	V
XIN duty cycle		40	-	60	%
XIN, XOUT loading		-	-	10	pF
VREF output	Deviation	–2	(VDD+Vss)/2	+2	%
	Resistance	3.25	-	6.75	kΩ
SIGIN input	Maximum voltage	VDD–10	-	VDD	V
	Impedance (500 Hz)	80	-	-	kΩ

ELECTRICAL SPECIFICATIONS (continued)

TIMING CHARACTERISTICS

(Ta = 25°C, VDD – VSS = 4.5V to 5.5V)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
t_{MD}	Signal duration for detection	315-640 Hz	40	-	ms
	Interval duration for detection	Signal dropping from –38 dBm to –50 dBm (t_2)	-	40	ms
		Signal dropping from 0 dBm to –50 dBm (t_1)	-	90	ms
t_B	Tone dropout bridging		-	20	ms

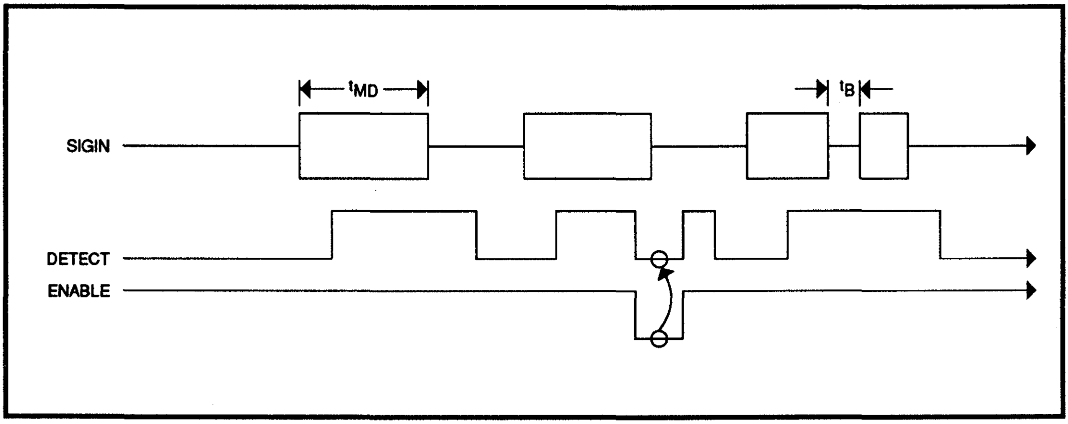


FIGURE 2: Basic Timing

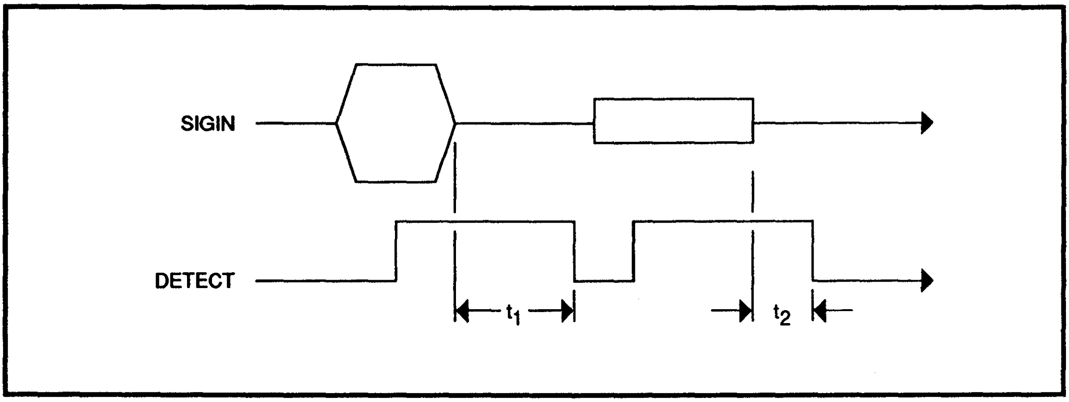


FIGURE 3: Effect of Amplitude on Timing

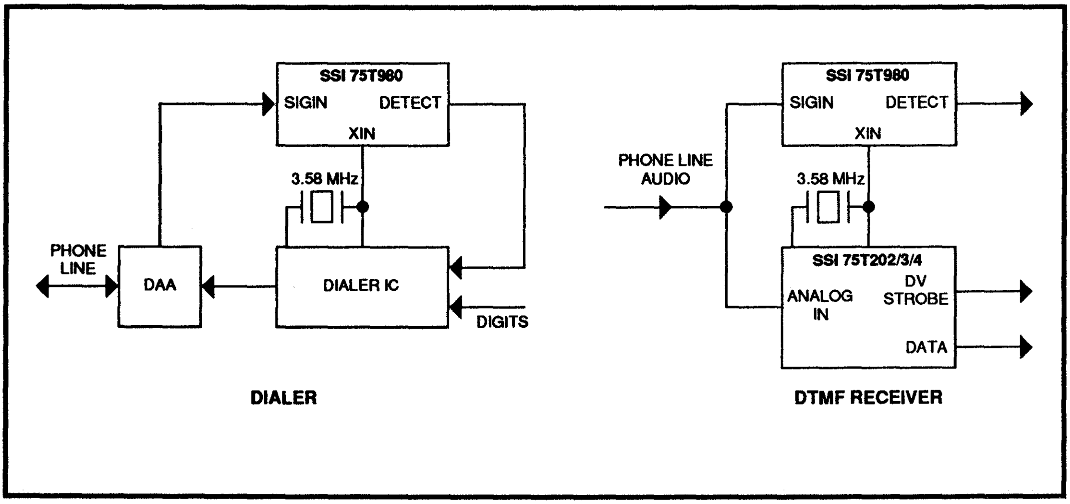
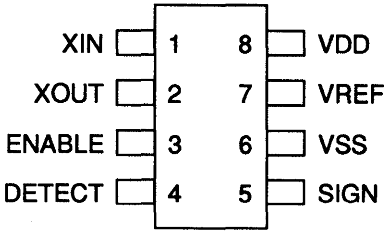


FIGURE 4: Applications Circuits

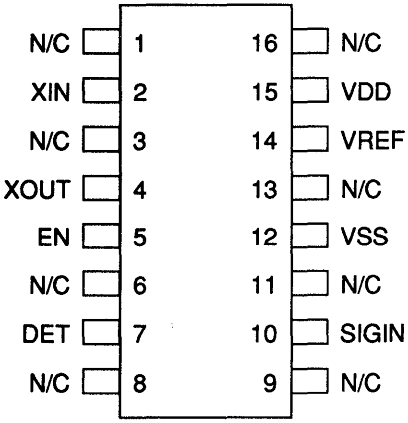
SSI 75T980
Call Progress
Tone Detector

PACKAGE PIN DESIGNATIONS

(Top View)



SSI 75T980-CP
8-PIN DIP



SSI 75T980C
16-PIN SO

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 75T980 8-pin Plastic DIP	75T980-CP	75T980-CP
SSI 75T980 16-pin SO Package	75T980-CL	75T980C

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SSI 78A093A/B
CMOS 12x8x1 Crosspoint Switch With Control Memory

July 1990

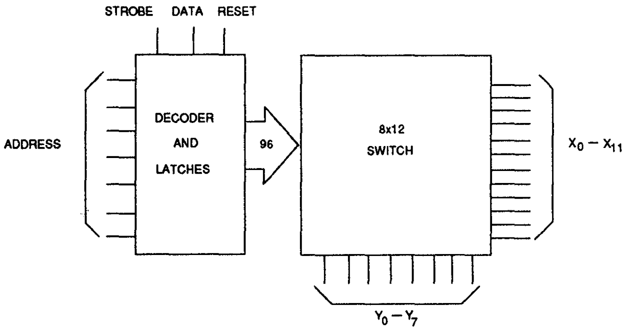
DESCRIPTION

The SSI 78A093 is a 12x8 matrix-array crosspoint-switching IC for telecom-switching and industrial control-routing applications. Standard integrated features include microprocessor-control inputs, line decoder, address latches, and 6 Vp-p analog-signal capability. The product is available with two different power supply configurations: The SSI 78A093A accepts power through the VSS and VDD pins; the SSI 78A093B has an altered pin-out and offers a separate logic ground pin. Both versions offer excellent crosstalk immunity, low feedthrough (–95dB at 1KHz), extra-high isolation between any two switches connected to X0 channel, and less than 1% total distortion at 0 dBm. The X0 channel is optimized for "ON HOLD" use by providing high isolation between switches connected to X0. The SSI 78A093 employs CMOS design technology for low-power operation. Power requirement for both the A and B versions of the SSI 78A093 is 5 to 16 volts. Both versions are packaged in a standard 40-pin plastic DIP or 44-pin PLCC.

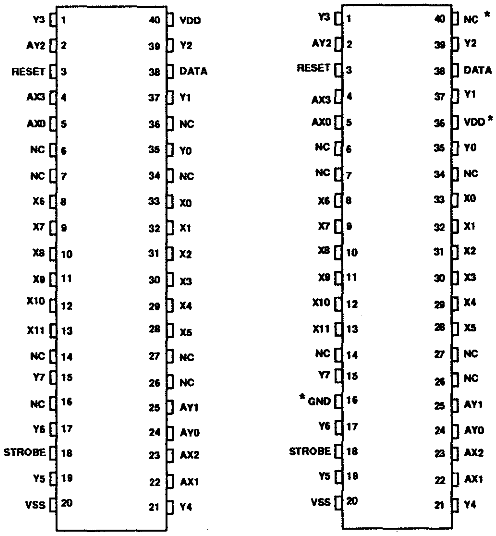
FEATURES

- **96 crosspoint switches in a 12x8 array**
- **µP-compatible control inputs**
- **On-chip line demultiplexer**
- **Low ON resistance: 28 ohms at VDD = 12V typical**
- **5 to 16-volt supply operating range**
- **6 Vp-p analog signal capability**
- **Address latches on-chip**
- **Optimized performance on X0 channel**
- **Less than 1% total distortion at 0 dBm**
- **-95 dB feedthrough at 1kHz**
- **Extra-low crosstalk between any two switches connected to X0**
- **78A093B version offers separate logic ground for flexible system design**
- **Low-power CMOS design**
- **TTL or CMOS-compatible inputs**
- **40-pin plastic DIP or 44-pin PLCC**

BLOCK DIAGRAM



PIN DIAGRAM



78A093A   78A093B

* different pins relative to 78A093A

NOTE: Please see last page for PLCC pinout.

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 78A093A/B
CMOS 12x8x1
Crosspoint Switch
With Control Memory

FUNCTIONAL DESCRIPTION

A functional block diagram of the device is presented in Figure 1. The IC contains a 12x8 matrix of analog switches, each with a latch to maintain its on (closed) or off (open) state. Seven ADDRESS lines, AX0-AX3 and AY0-AY2, are provided to address any one of the 96 switches. The DATA line may be held high to turn the switch on, or low to turn it off. The state of the ADDRESS and DATA lines can be set concurrently or separately. Finally, a positive pulse to the STROBE line initiates the action determined by the ADDRESS and DATA lines. All 96 switches may be turned off by forcing the RESET line high. All control lines (ADDRESS, DATA, STROBE, and RESET) are level sensitive.

The IC has two power supply configurations: the A-version has VDD and VSS power supply pins; the B-version has VDD, VSS and a GND pin. The GND pin is provided as a reference voltage for digital inputs. For proper operation, the positive supply must be at least 4.5 volts above GND.

The switches are designed to provide low resistance connections when turned on. Any Y switches connecting to the X0 channel are optimized to provide lower ON resistance. Furthermore, the X0 channel switches, when turned on, provide maximized isolation between the Y channels when X0 is grounded or connected to a low impedance source.

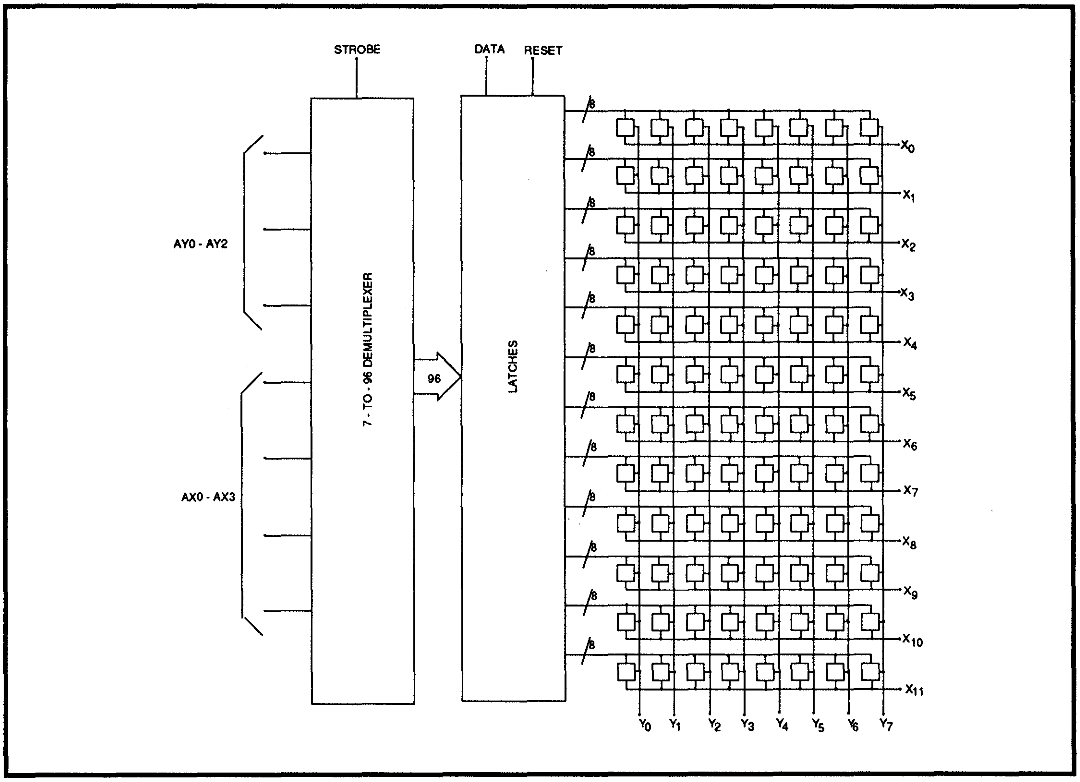


FIGURE: 1

PIN DESCRIPTION

NAME	A-PIN # (DIP)	B-PIN # (DIP)	TYPE	DESCRIPTION
POWER				
VDD	40	36	I	Positive power supply.
VSS	20	20	I	Negative power supply.
GND	-	16	I	Digital signal ground.
ADDRESS				
AX0-AX3	4, 5, 22, 23		I	X address lines. These 4 pins are used to select one of the 12 rows of switches. Refer to the truth table in figure 2, for legal addresses.
AY0-AY2	2, 24, 25		I	Y address lines. These 3 pins are used to select one of the 8 columns of switches. Refer to the truth table in figure 2, for legal addresses.
CONTROL				
DATA	38		I	This input determines if the selected switch will be turned on (closed) or off (opened). If the pin is held high, the selected switch will be closed. If the pin is held low, the switch will be opened.
STROBE	18		I	This pin enables whatever action is selected by the address and DATA pins. When the STROBE pin is held low, no switch openings or closing take place. When the STROBE pin is held high, the switch addressed by the select lines will be opened or closed (depending upon the state of the DATA pin).
RESET	3		I	Master Reset. This pin turns off (opens) all 96 switches. The states of the above control lines are irrelevant. This pin is active high.
DATA				
X0-X11	8-13, 28-33		I/O	Analog Input/Outputs. These pins are connected to the rows of the switch matrix.
Y0-Y7	1, 15, 17, 19, 21, 35, 37, 39		I/O	Analog Input/Outputs. These pins are connected to the columns of the switch matrix.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING	UNIT
VDD with respect to VSS	-0.5 to 17.6	V
GND (B-Version only)	VSS -0.5 to VDD +0.5	V
Storage Temperature	-65 to 150	°C
Control Signals	GND -0.5 to VDD +0.5	V
Analog Signals	7	Vpp
Lead Temperature (soldering, 10 seconds)	300	°C

Address							Connections
AX0	AX1	AX2	AX3	AY0	AY1	AY2	
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0	1	1	0	0	0	0	no connection
1	1	1	0	0	0	0	no connection
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0	1	1	1	0	0	0	no connection
1	1	1	1	0	0	0	no connection
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0 - Y1 ↓ ↓ X11- Y1
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0 - Y2 ↓ ↓ X11- Y2
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0 - Y3 ↓ ↓ X11- Y3
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0 - Y4 ↓ ↓ X11- Y4
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0 - Y5 ↓ ↓ X11- Y5
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0 - Y6 ↓ ↓ X11- Y6
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0 - Y7 ↓ ↓ X11- Y7

address not allowed

FIGURE 2: Truth Table

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside these limits.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
VDD with respect to VSS		4.5		16.0	V
VDD with respect to GND		4.5		16.0	V
GND with respect to VSS		0		5.5	V
Analog Input Voltages VIN				6	Vpp
Analog Currents				10	mA
Ambient Temperature		0		85	°C

D.C. CHARACTERISTICS

TA = 25°C, VSS = 0V, GND = 0, VDD = 13.2V, RL = 1K, CL = 50pF, UNLESS OTHERWISE NOTED. Positive current is defined as flowing into the device.

PARAMETERS	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current IDD			14	20	mA
CROSSPOINT					
ON resistance RON — X0 channel (X0-Yj)	VIN ≤ 6V		20		Ω
ON resistance RON — other channels (Xi-Yj)	VIN ≤ 6V		28	45	Ω
ON resistance var. Δ RON — X0 channel (X0-Yj)			5		Ω
ON resistance var. Δ RON — other channels (Xi-Yj)			15	25	Ω
X capacitance CX	(Switch off)			20	pF
Y capacitance CY	(Switch off)			30	pF
CONTROL					
Input HIGH voltage VIH	A-Version B-Version	2.0 GND +2.0			V V
Input LOW voltage VIL	A-Version B-Version			0.8 GND +0.8	V V
Input leakage IL		-0.1		0.1	µA

DYNAMIC CHARACTERISTICS AND TIMING

TA = 25°C, VDD = 13.2V, VSS = 0V, GND = 0V, RL = 1K, CL = 50 pF, UNLESS OTHERWISE NOTED. Digital input rise and fall times are 5nS. Output times are defined as the time to rise or fall from 0% to 10% of the full swing (see figure 3).

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
CROSSPOINT						
Propagation Delay		1 Vpp sine wave @ 10 kHz		18	30	ns
Distortion		1 Vpp sine wave		0.2	1.0	%
Feedthrough		10 kHz, any switch off		-90	-80	dB
Yi to Yj isolation on X0 channel		Any two Y channels: Yi, Yj, X0-Yi, X0-Yj are on Xo grounded, Rin = 1K		-90	-60	dB
Crosstalk		1Vp-p sine wave 1 kHz		-97		dB
		10 kHz		-92		
CONTROL						
Delay: strobe to out	TSZ			60	160	ns
Delay: address to out	TAZ				200	ns
Delay: data to out	TDZ				180	ns
Delay: reset to out	TRZ			100	180	ns
Data setup time	TSU			30		ns
Address setup time	TAS			30		ns
Data hold time	TH			30		ns
Address hold time	TAH			30		ns
Strobe Pulse Width	TST			50		ns
Reset Pulse Width	TRST			50		ns

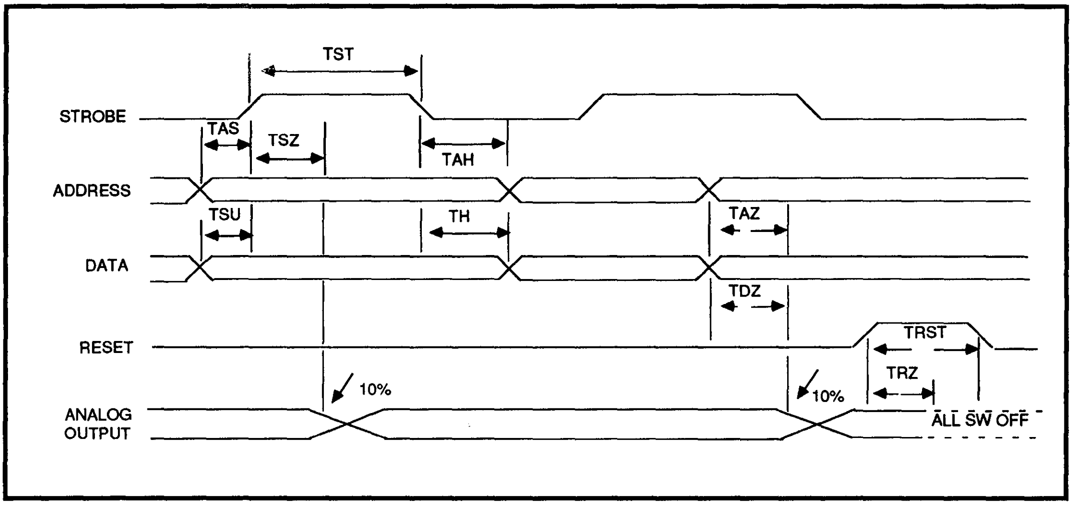


FIGURE 3: Timing Diagram

APPLICATIONS INFORMATION

Although the SSI 78A093 allows switching 96 possible signal paths, it is not limited to applications of only an 8x12x1 configuration. Figure 4 shows a method of addressing 4 separate 78A093's. In this example, the RESET, DATA, and ADDRESS lines are connected in parallel for the four devices. The logic for lines A, B and STROBE go to a 2-line to 4-line decoder with the STROBE used to both enable and clock the data. This decode (or a wider one) could be easily implemented with a single programmable logic device.

Figure 5 shows a case where both the X and Y lines have been expanded. This may be useful for applications where several different source/destination paths need to be controlled by a single controller. The A and B lines are decoded to select the desired device.

In Figure 6, the Y-lines of all devices are connected in parallel to allow an 8x48x1 switch configuration. The A and B inputs become in effect an extension of the X-address line. This could also be used to make a 32x12x1 matrix by tying the X-lines in parallel with the A and B inputs used as Y-address lines.

Figure 7 shows an application where switches in 2 devices are connected at the same time in a 12x8x2 matrix. This would be useful in applications requiring the switching of differential signals.

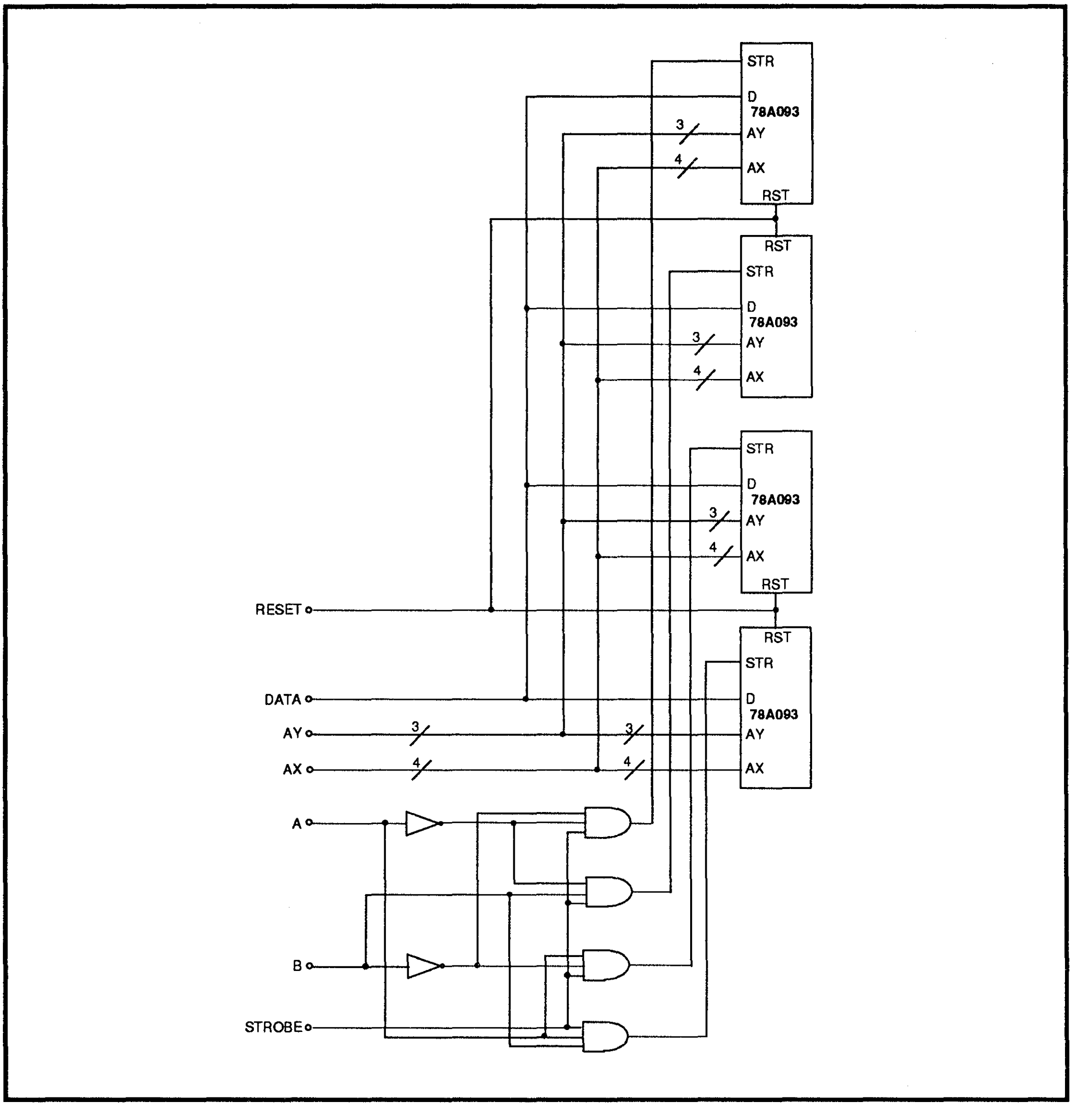


FIGURE 4

FIGURE 5

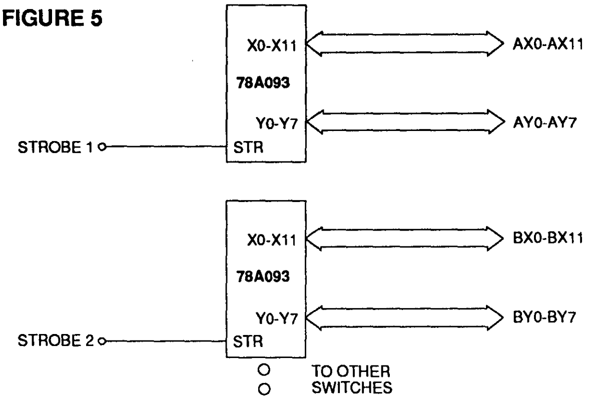


FIGURE 6

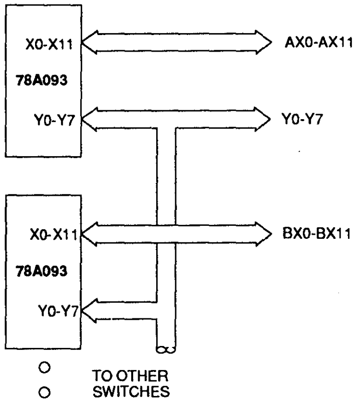
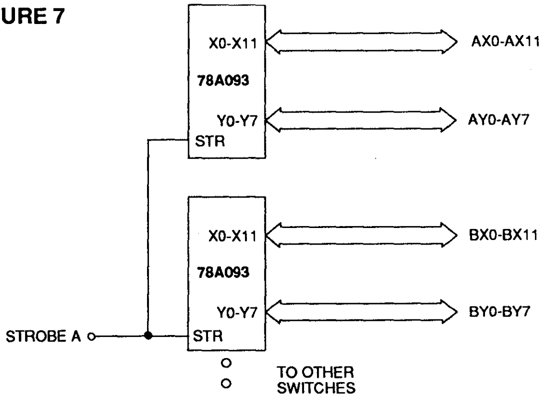


FIGURE 7



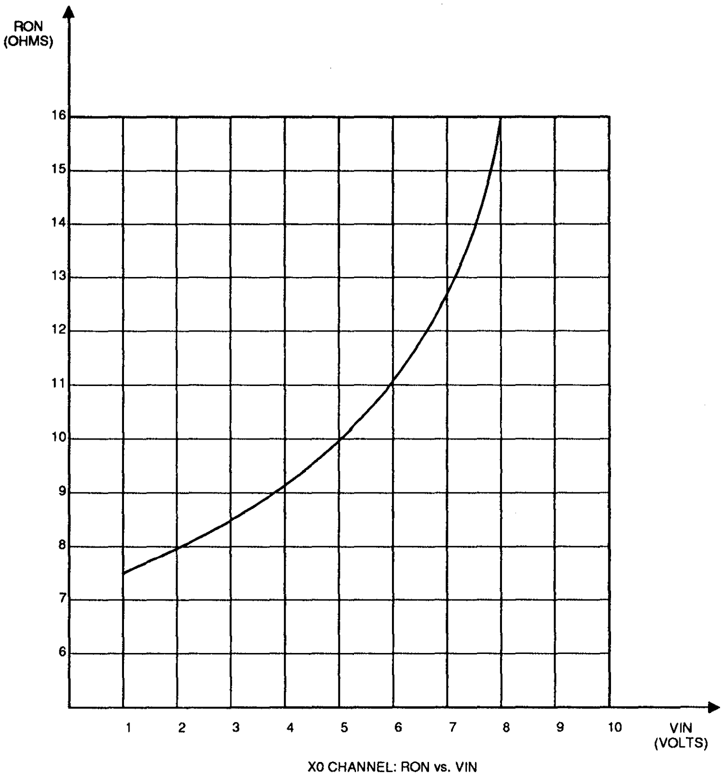


FIGURE 8: X0 - Channel: RON vs. VIN

Figure 8 is valid for all switches connected to the X0 channel only. The graph describes the behavior of the switch resistance RON as a function of the analog signal voltage VIN.

TEST CONDITIONS: VSS = 0V
VDD = 13.2V
RL = 1kΩ (Load Resistance)

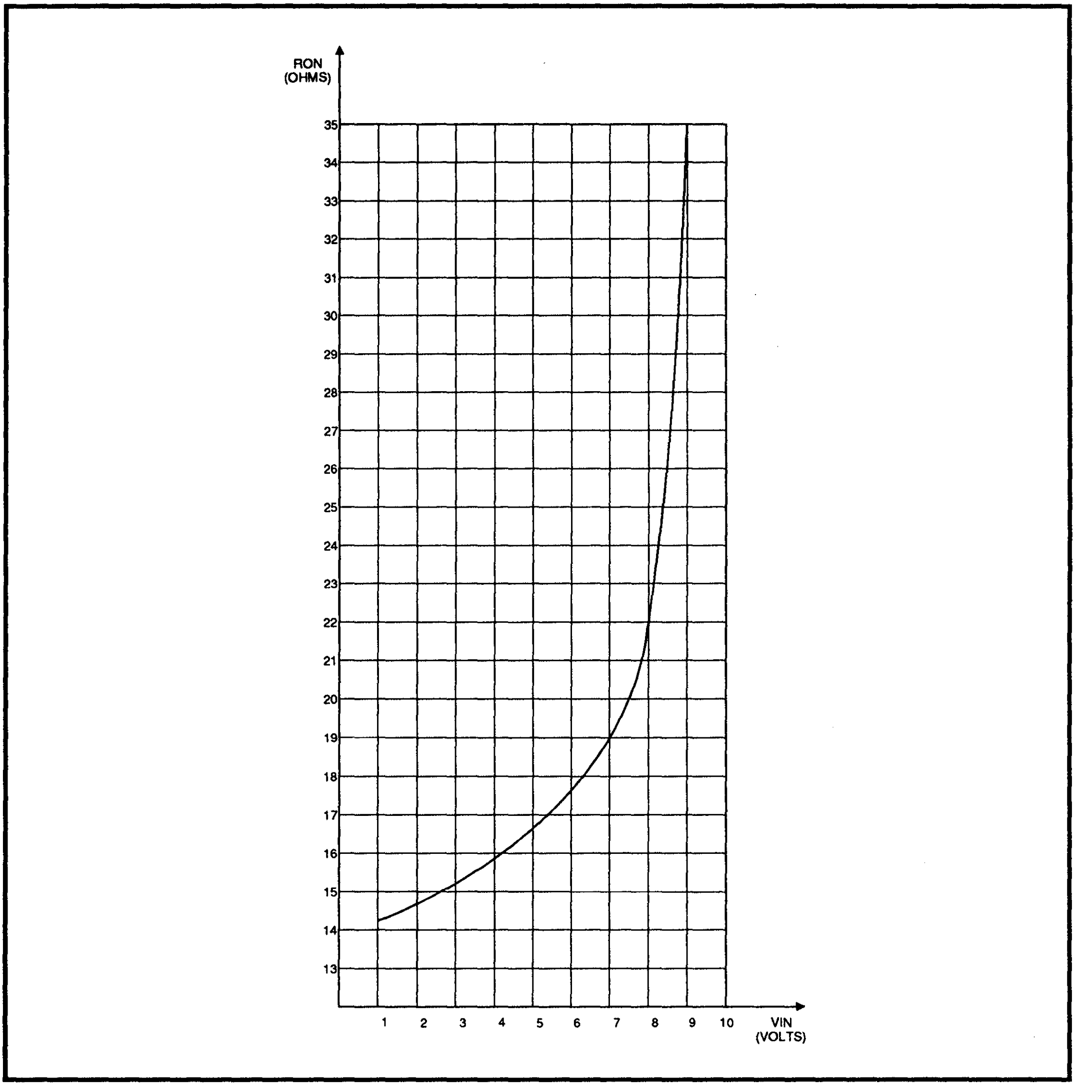


FIGURE 9: X1 - X11 Channel: RON vs. VIN

Figure 9 is valid for all switches connected to X1 thru X11 channels. The graph describes the behavior of the switch resistance RON as a function of the analog signal voltage VIN.

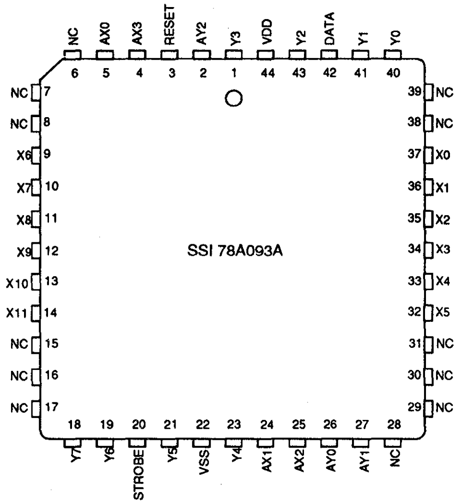
TEST CONDITIONS: VSS = 0V
VDD = 13.2V
RL = 1kΩ (Load Resistance)

SSI 78A093A/B
CMOS 12x8x1
Crosspoint Switch
With Control Memory

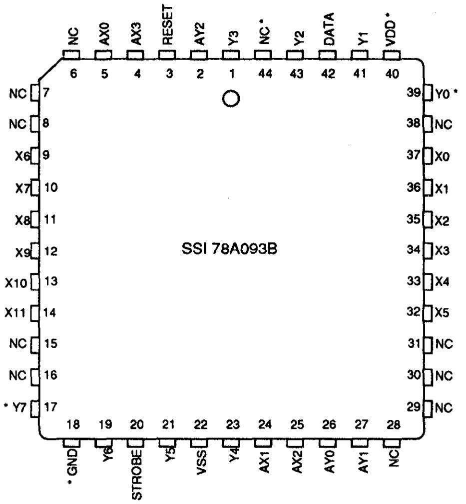
PACKAGE PIN DESIGNATIONS

(TOP VIEW)

Refer to the SSI Data Book for package dimensions.
Please see Page 1 for PDIP pinout.



44 - Pin PLCC
78A093A



44 - Pin PLCC
78A093B

* different pins relative to 78A093A

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78A093, Version A		
Plastic Dual-In-Line	78A093A-CP	78A093A-CP
PLCC	78A093A-CH	78A093A-CH
SSI 78A093, Version B		
Plastic Dual-In-Line	78A093B-CP	78A093B-CP
PLCC	78A093B-CH	78A093B-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

SSI 78A207
MFR1 Receiver

July 1990

DESCRIPTION

The SSI 78A207 is a single-chip, Multi-Frequency (MF) receiver that can detect all 15 tone-pairs, including ST and KP framing tones. This receiver is intended for use in equal access applications and thus meets both Bell and CCITT R1 central office register signalling specifications.

The SSI 78A207 employs state-of-the-art switched capacitor filters in CMOS technology. The receiver consists of a bank of channel-separation bandpass filters followed by zero-crossing detectors and frequency-measurement bandpass filters, an amplitude check circuit, a timer and decoder circuit, and a clock generator. The device does not attempt to identify strings of digits by the KP (key pulse) and ST (stop) tone pairs.

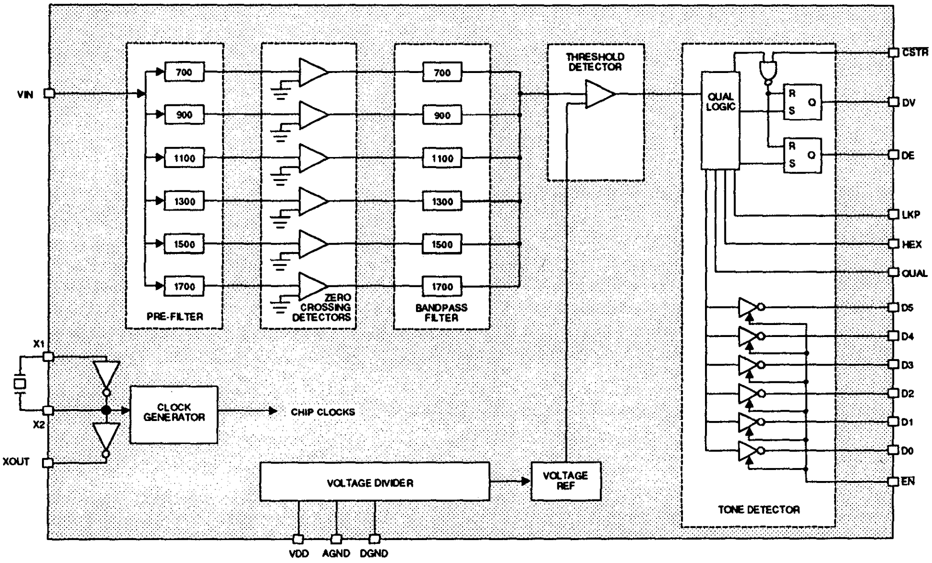
No anti-alias filtering is needed if the input signal is band-limited to 26 KHz. The only external component required is an inexpensive television "color burst" 3.58 MHz crystal.

The outputs interface directly with standard CMOS or TTL circuitry and are three-state enabled to facilitate bus-oriented architecture.

FEATURES

- **Meets Bell and CCITT R1 specifications**
- **20-pin plastic DIP**
- **Single low-tolerance 5V supply**
- **Detects all 15 tone-pairs including ST and KP**
- **Long KP capability**
- **Built-in amplitude discrimination**
- **Excellent noise tolerance**
- **Outputs in either "n of 6" or hexadecimal code**
- **Three-state outputs, CMOS-compatible and TTL-compatible**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

VIN

This pin accepts the analog input. It is internally biased to half the supply and is capacitively coupled to the channel separation filters. The input may be DC coupled as long as it does not exceed VDD or drop below GND. Equivalent input circuit is shown below in Figure 1.

CRYSTAL OSCILLATOR

The SSI 78A207 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low cost television "color-burst" crystal. The on-chip clock signals are generated from the oscillator. The crystal is connected between X1 and X2.

XOUT is a 3.58 MHz square wave capable of driving other circuits as long as the capacitive load does not exceed 50 pF. Other devices driven by XOUT should use X1 as the input pin, while X2 should be left floating.

LKP

The KP timer control: When high, the KP detect time is increased. When low, the KP detect time is the same as for other tones.

QUAL

Enables tone pair qualification. When low, the threshold detector outputs are passed to the data outputs (D0-D5) without validation in the format selected by the HEX pin. These outputs, plus strobes DV and DE, are updated once per 2.3 ms frame. Note that the strobes will cycle once per frame (even when the inputs are stable.) As always, data changes only when both strobes are low.

$\overline{\text{CSTR}}$

This input clears both the DV and DE strobes, and is active low. After $\overline{\text{CSTR}}$ is released, the strobes will remain low until a new detect (or error) occurs. The output data is latched by $\overline{\text{CSTR}}$ and will not change while $\overline{\text{CSTR}}$ is low, even in the event that a new detect is qualified internally. (Note that improper use of $\overline{\text{CSTR}}$ may result in missed detects.)

$\overline{\text{EN}}$

The three-state enable control: When low, the D0-D5 outputs are in the low impedance state. In an interrupt oriented microprocessor interface, $\overline{\text{EN}}$ and $\overline{\text{CSTR}}$ will often be tied together to provide automatic reset of the strobes when the output data is enabled.

STROBE PINS - DV AND DE

Valid data is indicated on the DV strobe pin, and data errors are indicated on the DE strobe pin. Whenever a valid 2 of 6 code has been detected, the DV strobe rises. It remains high until the code goes away, or the $\overline{\text{CSTR}}$ line is activated. When an invalid code is detected, e.g., 1 of 6, 3 of 6, etc., the DE strobe remains high until all errors stop, a valid tone pair is detected, or the $\overline{\text{CSTR}}$ line is activated. Once cleared by $\overline{\text{CSTR}}$, DE will not reactivate until a new invalid condition is detected. The DE and DV strobes will never be high simultaneously.

DATA OUTPUT MODES

The digital output format may be either "n of 6" or 4-bit hexadecimal.

For "hex" mode, the HEX pin is pulled high. Outputs D0 to D3 provide a 4-bit code identifying one of the 15 valid tone combinations according to Table1.

The outputs will be cleared to zero when no valid tone pair is present.

For the "n of 6" mode, the HEX pin is pulled low, and each output represents one of the six frequencies as shown below:

FREQUENCY	OUTPUT PIN
700	D0
900	D1
1100	D2
1300	D3
1500	D4
1700	D5

The outputs will be cleared to zero when no valid tone is present.

TABLE 1:

Channels	Tone Pair Freq.	Name	D3	D2	D1	D0
0-1	700, 900	1	0	0	0	1
0-2	700, 1100	2	0	0	1	0
1-2	900, 1100	3	0	0	1	1
0-3	700, 1300	4	0	1	0	0
1-3	900, 1300	5	0	1	0	1
2-3	1100, 1300	6	0	1	1	0
0-4	700, 1500	7	0	1	1	1
1-4	900, 1500	8	1	0	0	0
2-4	1100, 1500	9	1	0	0	1
3-4	1300, 1500	0	1	0	1	0
2-5	1100, 1700	KP	1	0	1	1
4-5	1500, 1700	ST	1	1	0	0
1-5	900, 1700	ST1	1	1	0	1
3-5	1300, 1700	ST2	1	1	1	0
0-5	700, 1700	ST3	1	1	1	1
	any other signal		0	0	0	0

NOTE: In the hex mode, D4 = DE and D5 = DV.

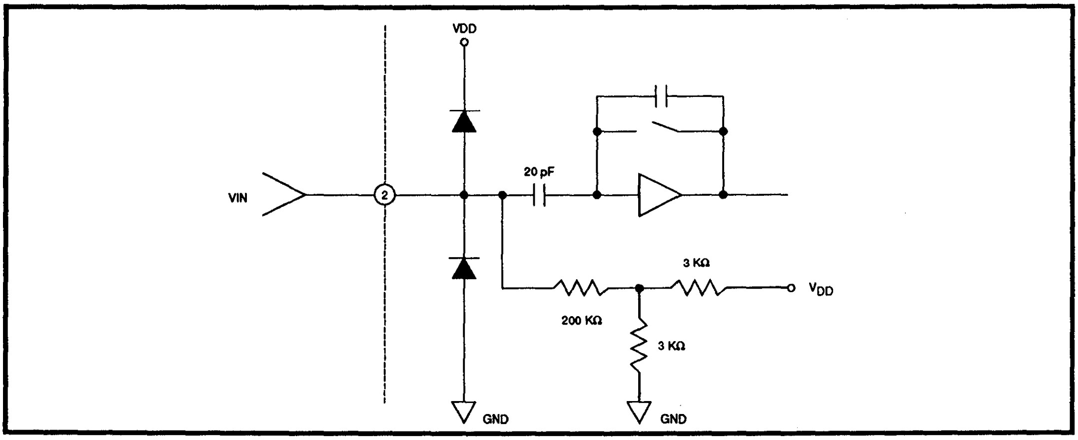


FIGURE 1: VIN Equivalent Input Circuit

TIMING SPECIFICATIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ton	Tone Time, KP (LKP = VDD)	detect	55			ms
Ton		reject			30	ms
Ton	Tone Time, KP (LKP = DGND)	detect	30			ms
Ton		reject			10	ms
Ton	Tone Time, All Others	detect	30			ms
Ton		reject			10	ms
Tpse	Pause Time	detect	20			ms
Tbr		reject			10	ms
Tsu	Data Setup Time		6			µs
Th	Data Hold Time		7			µs
Tskew	Tone Skew Tolerance				4	ms
Tstr	Minimum Strobe Pulse Width					
	QUAL High		20			ms
	QUAL Low		2			ms
Tsep	Minimum Strobe Separation					
	QUAL High		20			ms
	QUAL Low		2			ms
Tr	Rise Time DV, DE, D0-D5 10-90%	CL = 20 pF			100	ns
Tf	Fall Time DV, DE, D0-D5 10-90%	CL = 20 pF			100	ns
Tw	$\overline{\text{CSTR}}$ Width		50			ns
Ten	Data Enable Time	CL = 20 pF			100	ns
Tdis	Data Disable Time				100	ns
Trst	Strobe Reset Time	CL = 20 pF			100	ns

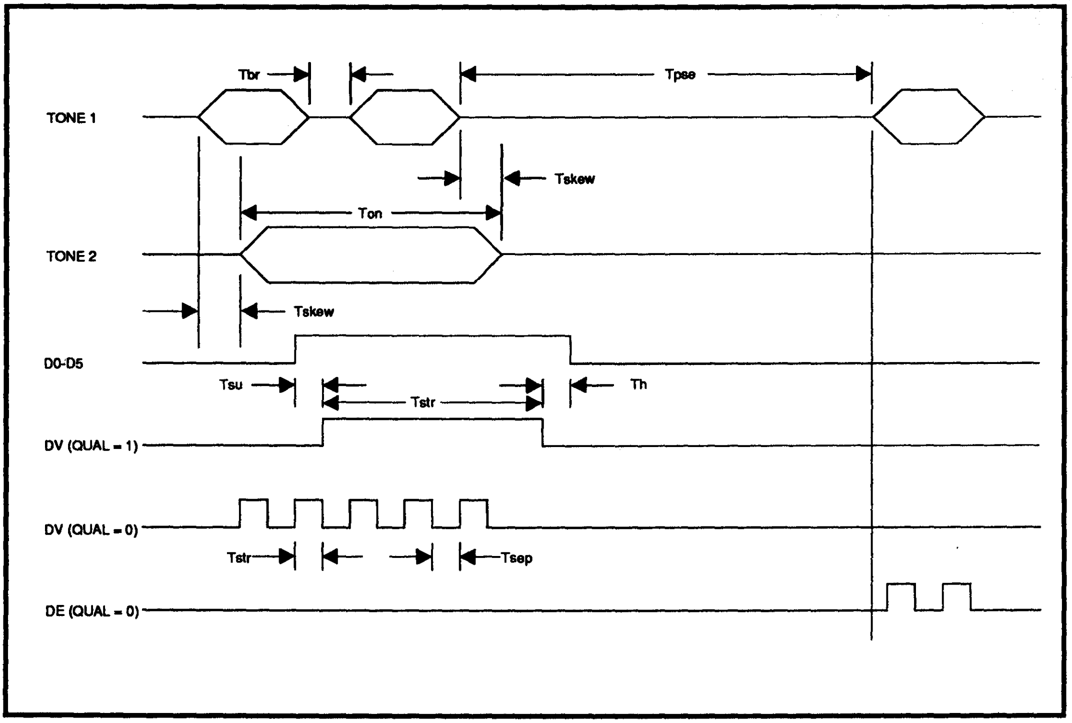


FIGURE 2: SSI 78A207 Timing Diagram

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Operating above absolute maximum ratings may damage the device.)

PARAMETER	RATING	UNIT
DC Supply Voltage V_{DD}	+ 7	V
Operating Temperature	0 to 70 (Ambient)	°C
Storage Temperature	65 to 150	°C
Power Dissipation (25°C) (Derate above TA=25°C @ 6.25 mW/°C)	650	mW
Input Voltage	(VDD + 0.3V) to -0.3	V
DC Current into any input	±10	mA
Lead Temperature (Soldering, 10 sec.)	300	°C

DC ELECTRICAL CHARACTERISTICS (0°C ≤ TA ≥ 70°C, VDD = 5V ± 10%)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idd Supply Current				20	mA
Vol Output Logic 0					
Iol = 8 mA				0.5	V
Iol = 1 mA				0.4	V
Voh Output Logic 1					
Ioh = -4 mA		VDD-1.0			V
Ioh = -1 mA		VDD-0.5			V
Vih Input Logic 1		2.0			V
Voh Input logic 0				0.8	V
Zin Analog Input Impedance (Input between VDD and AGND)		100K 30 pF			Ω
Iin Digital Input Current (Input between VDD and DGND)		-50		50	µA

AC CHARACTERISTICS (0°C ≤ TA ≥ 70°, VDD = 5V ± 10%)

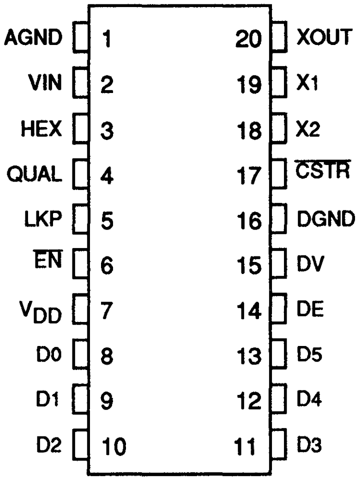
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
F Frequency for Detect Tolerance		±(0.015 xFo + 5)			Hz
A Amplitude for Detect	each tone	-25		0	dBm
		0.123		2.191	Vpp
AN Amplitude for no Detect				-35	dB
				0.039	Vpp
TW Twist Tolerance	$TW=\frac{\text{high tone}}{\text{low tone}}$	-6		+6	dB
T3 Third MF Tone Reject Amp	relative to highest amplitude tone	-15			dB
N60 60 HZ Tolerance	not more than one error	81			dBrn
	in 2500 10-digit calls	0.777			Vpp
N180 180 HZ Tolerance	same as above	68			dBrn
		0.174			Vpp
Nn Noise Tolerance[1]	same as above			-20	dB
NI Impulse Noise Tolerance[2]	same as above			+12	dB

NOTES: 1. C-message weighted. Measured with respect to highest amplitude tone.

2. With noise tape 201 per PUB 56201. Measured with respect to highest amplitude tone.

PACKAGE PIN DESIGNATIONS

(TOP VIEW)



20 - PIN DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78A207 20-Pin Plastic DIP	78A207-CP	78A207-CP

Notes:

Section 5

PCM PRODUCTS

silicon systems®
A TDK Group Company

SSI 78P233A
DS-1 Line Interface

January 1992

DESCRIPTION

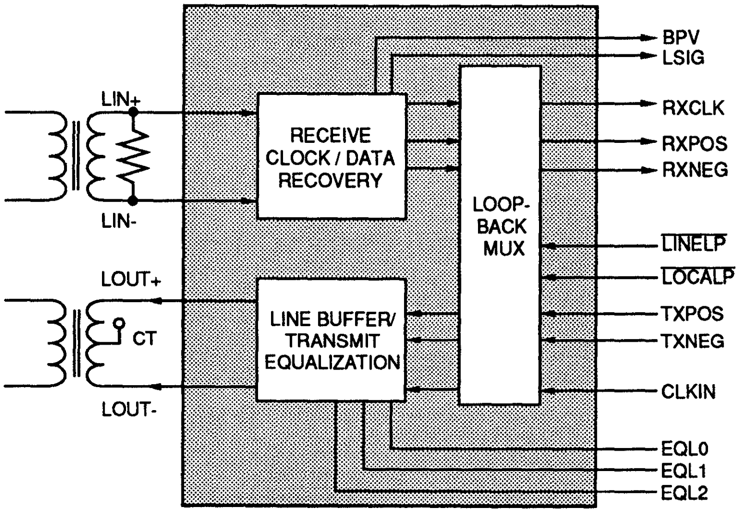
The SSI 78P233A DS-1 Line Interface is a bipolar integrated circuit that provides the interface functions necessary to convert DS-1-level signals to TTL-level and conversely. The receiver section accepts alternate-mark-inversion (AMI) encoded line data and provides separated and synchronized data and clock outputs. The transmitter section accepts data and clock and produces AMI pulses of appropriate shape for transmission. A loopback multiplexer is also provided that permits interchange of the signals between the sections.

The 78P233A requires a single 5V supply. It is available in a standard, 600-mil DIP package.

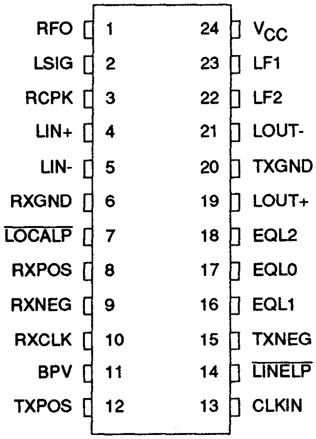
FEATURES

- **Single-chip transmit and receive DS-1 Line Interface**
- **Unique clock recovery circuit, requires no crystals or tuned components**
- **Variable jitter tolerance, adjustable with external components**
- **Pulse-shape transmission conformant with AT&T Compatibility Bulletin 119 specifications**
- **Six different line equalization settings for pulse-shaping at the DSX-1 level**
- **Two alternate transmit settings for 6V-peak pulses**
- **Standard unipolar TTL-level clock & data ports for easy equipment interface**
- **Line-loopback and local-loopback control**
- **Loss-of-signal indication**
- **Bipolar violation detection**

BLOCK DIAGRAM



PIN DIAGRAM



24-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The device consists of receiver and transmitter sections together with a "loopback" means which permits interchange of signals between the sections (See Figure 1).

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. To provide a tracking threshold for amplitude-detecting these pulses, the signal is peak detected and a fixed percentage of the peak value is applied to the comparators which detect individual positive and negative pulses. An external R-C network is required to provide the proper storage of the peak reference value. Should the detected peak value fall below an acceptable level, the Loss of Signal (LSIG) output becomes active. This output may be used as a logical control signal or is able to drive a fault indicator LED directly.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase-locked-oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. Non-precision external components are required, however, to establish the oscillator center frequency and loop bandwidth.

The phase-locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

Additional circuits are provided to detect received bipolar violations. These deviations from the alternate mark inversion format are detected when two or more successive pulses of the same polarity are received. A resultant violation output is in time coincidence with the violating received signal output.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line.

Internal equalizer networks are selected by combinations of the three Equalizer Select inputs so that the waveform at the terminal end of various lengths of cable is as required. Note that the transmitter output pulse widths are determined by the input clock width, so that it must be carefully controlled to provide acceptable outputs.

The transmitter pulse selection logical function is arranged so that the simultaneous occurrence of both positive and negative transmit data inputs inhibits the output driver. Moreover, the driver has a current-limiting feature which protects the circuit in the event of a shorted load or inadvertent shorting of an output to the supply voltage.

LOOPBACK CONTROL SECTION

The loopback control section is essentially a multiplexer which is capable of directing received data and clock to the transmitter section, or directing transmit input data and clock to the receiver outputs. This "looping" is controlled by two active low logic signals, $\overline{\text{LINELP}}$ and $\overline{\text{LOCALP}}$, respectively.

The bipolar violation output is held inactive when the circuits are in the Local Loopback mode.

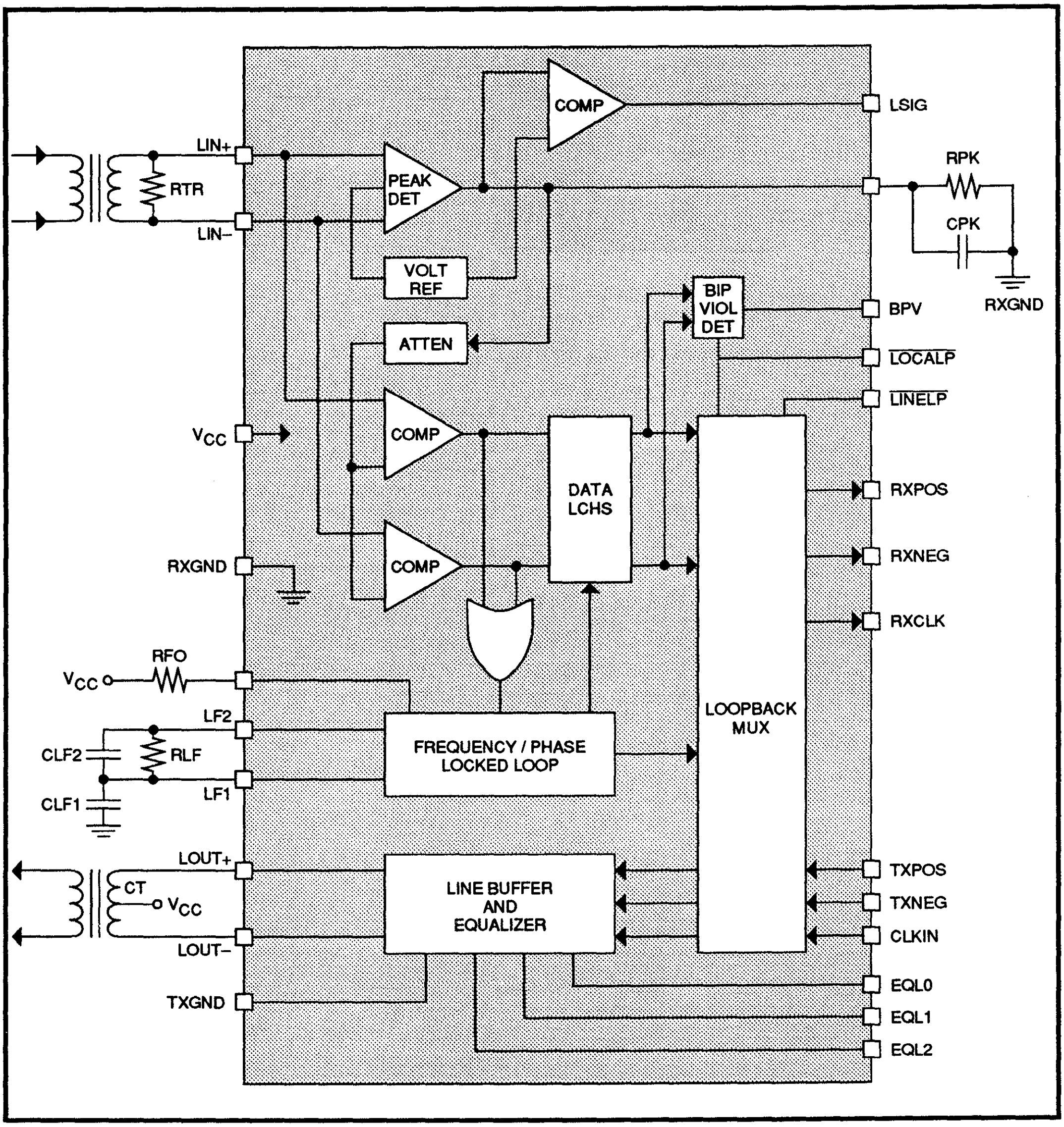


FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

I/O	LABEL	PIN NO.	DESCRIPTION
I	LIN+, LIN-	4, 5	Differential inputs, transformer-coupled from line.
O	RXPOS	8	Unipolar receiver output, active as result of positive pulse at inputs.
O	RXNEG	9	Unipolar receiver output, active as result of negative pulse at inputs.
O	RXCLK	10	Clock pulses recovered from line data.
O	LSIG	2	Loss-of-signal output indicating that input signal is less than threshold value.
O	BPV	11	Bipolar violation output, active as a result of successive pulses at inputs of same polarity.

TRANSMITTER

I	TXPOS	12	Unipolar transmitter data input, active high.
I	TXNEG	15	Unipolar transmitter data input, active high.
I	CLKIN	13	Transmitter clock input. Controls transmit pulse width. Transmit is active when low.
O	LOUT+	19	Output to transformer for positive data pulses.
O	LOUT-	21	Output to transformer for negative data pulses.
I	EQL0 EQL1 EQL2	17 16 18	Line equalizer control signals. Selected according to Table 1 for various cable lengths.

LOOPBACK CONTROL

I	$\overline{\text{LINELP}}$	14	Low level causes receiver recovered data and clock to be connected to the transmitter. Data and clock continue to be present at receiver outputs.
I	$\overline{\text{LOCALP}}$	7	Low level causes transmitter input data and clock to be connected to the receiver outputs. Input data continues to be transmitted.

PIN DESCRIPTION (continued)

EXTERNAL COMPONENT CONNECTION

I/O	LABEL	PIN NO.	DESCRIPTION
I	RFO	1	Resistor connected to Vcc to provide basic center frequency of receiver phase locked loop oscillator.
-	LF1 LF2	23 22	Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
-	RCPK	3	Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

-	Vcc	24	Positive supply terminal for receiver circuits.
-	RXGND	6	Ground terminal for receiver circuits.
-	TXGND	20	Ground terminal for transmitter driver circuits.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING	UNIT
V_{CC}, Supply Voltage	-0.5 to +7.0	V
Storage Temperature	-65 to 130	°C
Soldering Temperature (10 sec.)	260	°C
Voltage Applied to Logic Inputs	-0.3 to Vcc +0.3	V
Maximum Power Dissipation	800	mW
Junction Operating Temperature	0 to +130	°C

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Ta	Ambient temperature		0		70	°C
Vcc	Power supply voltage		4.75		5.25	V
VIH	High-level input voltage		2.0			V
VIL	Low-level input voltage				0.8	V
IOH	High-level output current	LSIG pin only; VO = 1.5V	-7		-13	mA

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO	Loop center frequency resistor	1% tolerance		6.04		kΩ
RLF	Loop filter resistor			12.0		kΩ
CLF1	Loop filter capacitor			0.022		µF
CLF2	Loop filter capacitor			430.0		pF
RPK	Peak-detector resistor			36.0		kΩ
CPK	Peak-detector capacitor		0.0015	0.015	0.15	µF
	Transmit line transformer	Refer to Table 3		---		---

D. C. ELECTRICAL CHARACTERISTICS
(T_A = 0°C to 70°C, Vcc = 5V ± 5%, unless otherwise specified.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Supply current	All outputs open		83	110	mA
IIH	High-level input current	VIH = 2.7V			20	µA
IIL	Low-level input current	VIL = 0.4V			-0.36	mA
VOH	High-level output voltage	IOH = -400 µA	2.7			V
VOL	Low-level output voltage	IOL = 2.0 mA		0.48	0.6	V
		IOL = 2.0 mA, LSIG pin			0.4	V
RIN	Receiver input resistance		800	1000	1250	Ω

DYNAMIC CHARACTERISTICS AND TIMING, TRANSMITTER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. Transmit pulse characteristics are obtained using a line transformer which has the characteristics shown in Table 3. Refer to Figure 2.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			648		nsec
TTC	Transmit clock pulse width			324		nsec
TTCNT	Transmit clock negative transition time				10	nsec
TTCPT	Transmit clock positive transition time				10	nsec
TTPDS TTNDS	Transmit data set-up time		15			nsec
TTPDH TTNDH	Transmit data hold time		0			nsec
TTPL	Transmit positive line pulse width	See Note 1	TTC-5		TTC+5	nsec
TTNL	Transmit negative line pulse width	See Note 1	TTPL-5		TTPL+5	nsec
POL	Transmit line pulses power level	See Note 2				
	Transmit line pulses waveshape	See Notes 2 & 3				
Note 1:	Measured at transformer with minimum line equalization					
Note 2:	Characteristics are in accordance with AT&T Compatibility Bulletin 119, Table 1 and Table 3 for line lengths and equalizer settings as shown in Table 1 of this document.					
Note 3:	Characteristics are in accordance with Table 2 for equalizer settings shown therein.					

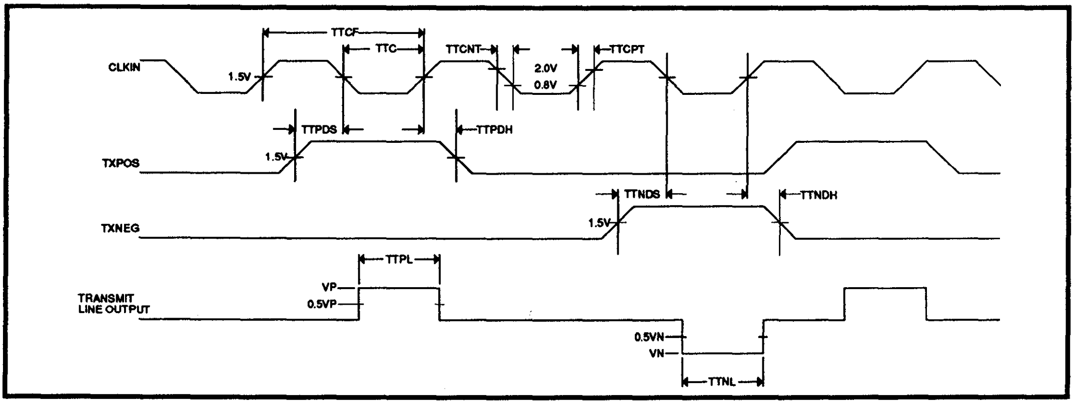


FIGURE 2: Transmit Waveforms

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. External component values as specified in Recommended Operating Conditions; see Note 1. Refer to Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage		±1.5		±3.7	Vpk
VLOS	Loss-of-signal indicating voltage		±0.5		±1.0	Vpk
TLOS	Loss-of-signal delay time	Timed from removal of input signal; See Note 2	0.7TPK		1.3TPK	sec
VDTH	Receive data detection threshold	Relative to peak amplitude	65		75	%
TSTAB	Receiver stabilization time	After application of input signal			5	msec
TRCF	Receive clock period			648		nsec
TRC	Receive clock pulse width		314	324	334	nsec
TRCPT	Receive clock positive transition time	C_L = 25 pF		5	10	nsec
	rise time	C_L = 25 pF; 10% - 90%		35	50	nsec
TRCNT	Receive clock negative transition time	C_L = 25 pF		3	10	nsec
	fall time	C_L = 25 pF; 10% - 90%		10	15	nsec
TRDP TRDN	Positive or negative receive data pulse width			648		nsec
TRDPS TRDNS	Receive data set-up time		290			nsec
TRDPH TRDNH	Receive data hold time		290			nsec
TRBV	Receive bipolar violation pulse width			648		nsec
TRBVS	Receive bipolar violation set-up time		290			nsec
TRBVH	Receive bipolar violation hold time		290			nsec
	Receive input jitter tolerance high frequency	sine, 10 kHz to 100 kHz	±100			nsec
	Receive input jitter tolerance low frequency	sine, 300 Hz or less	±4			µsec

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
KD	Clock Recovery Phase Detector Gain	(All 1's Data Pattern)	66		79	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Control Gain		0.15		0.20	Megrad/ sec. Volt
Note 1:	Input signal is transformer coupled, and in accordance with AT&T Compatibility Bulletin 119, Table 1, and Table 2 or Table 3; also, as attenuated by 0 to 655 feet of ABAM* cable.					
Note 2:	TPK = RPK x CPK x ln((VIN + 1.2V)/(VLOS + 1.2V))					
* ABAM is the trade name for 22-gauge twisted-pair cable manufactured by AT&T.						

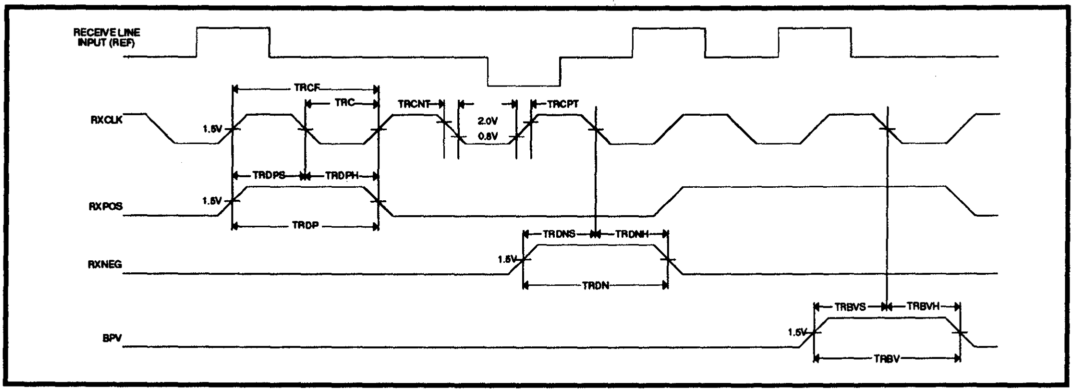


FIGURE 3: Receive Waveforms

TABLE 1: Equalizer Settings for Standard DSX-Level (3V-Peak Nominal) Pulses Versus ABAM Cable Length

CABLE LENGTH IN FEET	EQUALIZER SETTING		
	EQL0	EQL1	EQL2
0 to 50	0	0	0
51 to 131	1	0	0
131 to 262	0	1	0
262 to 393	1	1	0
393 to 524	0	0	1
524 to 655	1	0	1
Note: Output meets AT&T compatibility Bulletin 119, Figure 3, measured at the crossconnect. The only external transmit components required are a transformer as specified in Table 3 and proper line termination resistance.			

TABLE 2: Equalizer Settings for Non-DSX-Level (6V-Peak Nominal) Pulses

PULSE CHARACTERISTICS	EQUALIZER SETTING		
	EQL0	EQL1	EQL2
Rectangular 6.0 ± 0.6V pulse, 10% to 40% trailing edge overshoot	0	1	1
Rectangular 6.0 ± 0.6V pulse, less than 10% trailing edge overshoot	1	1	1
Note: Output waveform at transformer secondary; terminated in 100Ω load.			

TABLE 3: Transmit Line Transformer Characteristics

(Transmit line transformer characteristics are as specified below or as in Tautron's specification for part #5924-8301, Rev. A, 10/3/89).

CHARACTERISTIC	SYMBOL	MIN	NOM	MAX	UNIT
Turns ratio	N		1CT:1		
Primary open circuit inductance	Lp	1.25			mH
Primary leakage inductance	L1			2.0	µH
Primary volt-time product	ET	10			V-µsec
Primary DC resistance	Rp			1.0	Ω
Secondary DC resistance	Rs			1.0	Ω
Effective primary distributed capacitance	C'			15	pF

TABLE 4: Recommended Transmit Line Transformers

MANUFACTURER	PART NO.
AIE Magnetics	318-0765
AT&T	2745 AG
Pan-Mag (Tamura Corporation of America)	PHT-019
Pulse Engineering	PE 64936

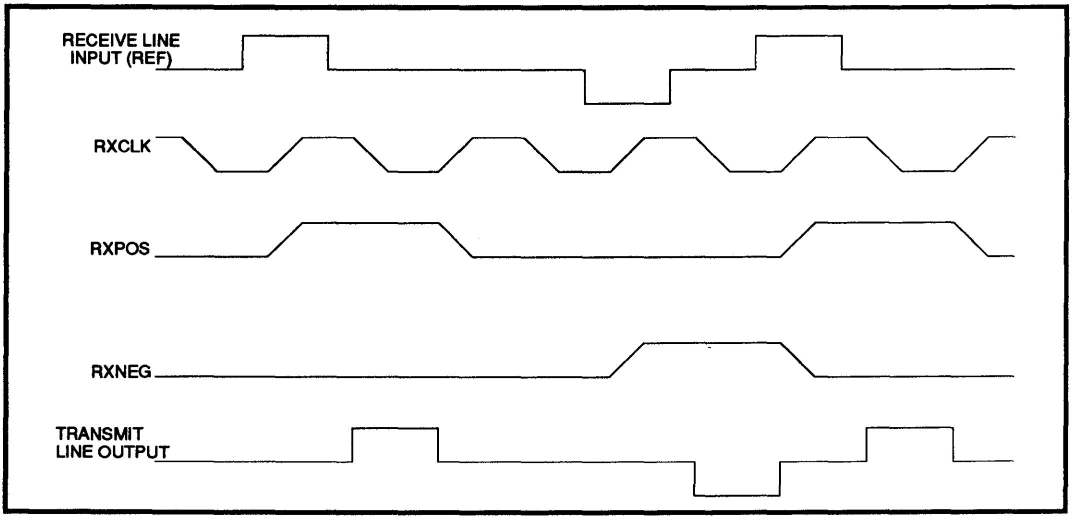


FIGURE 4: Line Loopback Waveforms

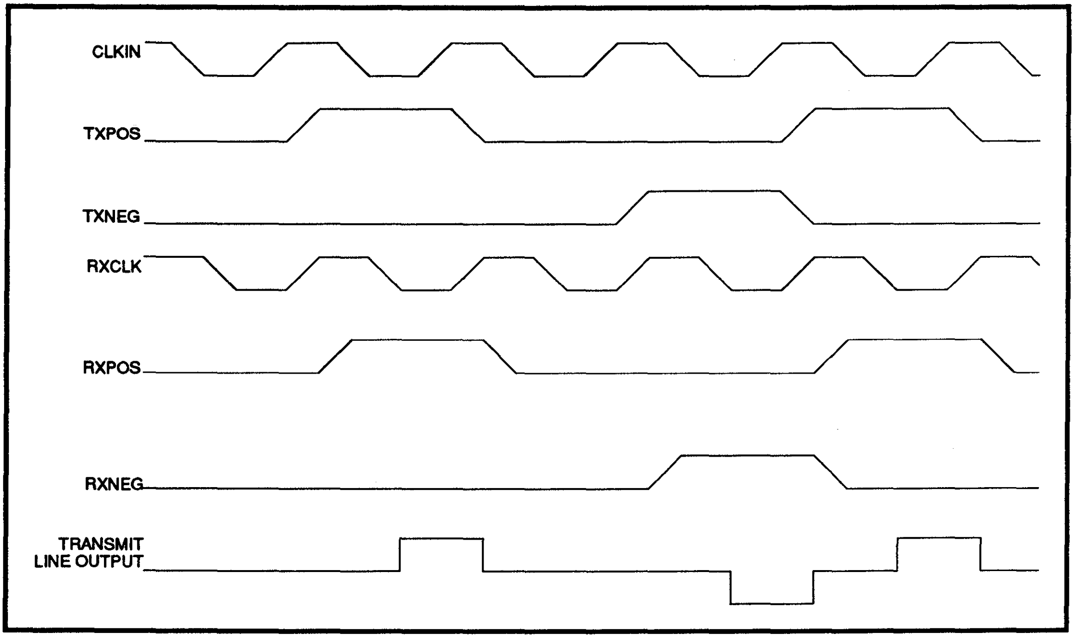
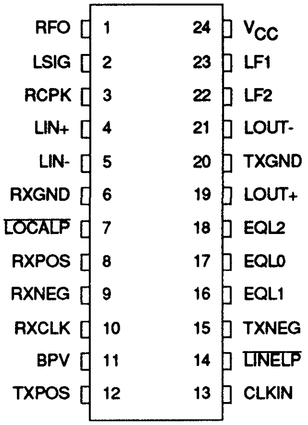


FIGURE 5: Local Loopback Waveforms

SSI 78P233A
DS-1 Line Interface

PACKAGE PIN DESIGNATIONS

(Top View)



24-Pin DIP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P233A, DS-1 Line Interface - 24-Pin		
Standard Width Plastic DIP (600 mil)	78P233A-CP	78P233A-CP

silicon systems®
A TDK Group Company

SSI 78P234
2048 KBit/s
PCM Interface Unit

October 1991

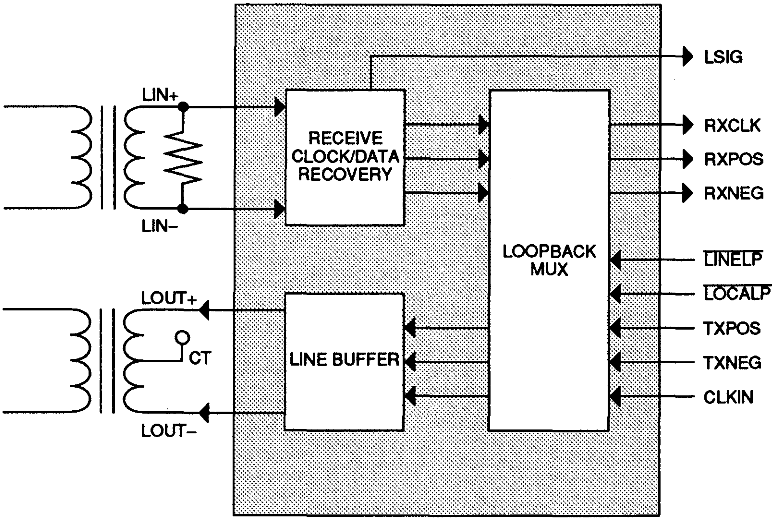
DESCRIPTION

The SSI 78P234 PCM Interface Unit is a bipolar integrated circuit which performs the functions of receiving and transmitting PCM signals in an Alternate-Mark-Inversion (AMI) format. The receiver accepts AMI-format line data and provides separated and synchronized TTL-level data and clock outputs. High-density bipolar three-encoded (HDB3) signals are passed through the chip transparently. The transmitter accepts TTL-level data and clock, typically HDB3-encoded, and produces AMI-format pulses of the appropriate shape for transmission. A loopback multiplexer is also provided that permits interchange of the signals between the sections. The SSI 78P234 requires a single 5V supply, and is available in both 20-pin DIP and small outline (SO) packages.

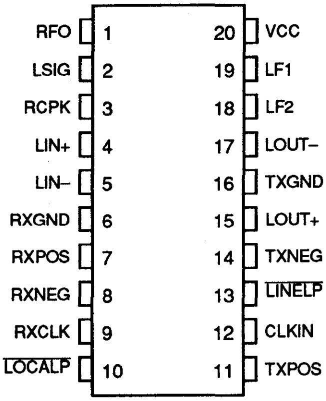
FEATURES

- **High-performance, low-cost solution for 2048 KBit/s PCM interface applications**
- **Both transmit and receive circuitry in a compact, 20-pin package**
- **Compliant with CCITT recommendations G.703 and G.823**
- **Unique clock-recovery circuit, requires no crystals or tuned components**
- **Standard unipolar TTL-level clock and data ports for easy equipment interface**
- **Line-loopback and local-loopback control**
- **Loss-of-signal indication**
- **Available in SO or dual-in-line packages**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The device consists of receiver and transmitter sections together with a "loopback" means which permits interchange of signals between the sections (see Figure 1).

RECEIVER

The receiver input is normally transformer-coupled to the source of encoded alternate polarity pulses. To provide a tracking threshold for amplitude-detecting these pulses, the signal is peak detected and a fixed percentage of the peak value is applied to the comparators which detect individual positive and negative pulses. An external R-C network is required to provide the proper storage of the peak reference value. Should the detected peak value fall below an acceptable level, the Loss of Signal (LSIG) output becomes active. This output may be used as a logical control signal or is able to drive a fault indicator LED directly.

Outputs of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase-locked-oscillator loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high-precision and/or adjustable oscillators or tuned circuits. Non-precision external components are required, however, to establish the oscillator center frequency and loop bandwidth.

The phase-locked reference oscillator is employed to strobe the detected data into output latches and is also available as an output for externally synchronizing the data.

TRANSMITTER

The transmitter combines unipolar logical inputs with an input clock to provide positive and negative output pulses onto a transformer-coupled line. Note that the transmitter output pulse widths are determined by the input clock width, so that it must be carefully controlled to provide acceptable outputs.

The transmitter pulse selection logical function is arranged so that the simultaneous occurrence of both positive and negative transmit data inputs inhibits the output driver. Moreover, the driver has a current-limiting feature which protects the circuit in the event of a shorted load or inadvertent shorting of an output to the supply voltage.

LOOPBACK CONTROL SECTION

The loopback control section is essentially a multiplexer which is capable of directing received data and clock to the transmitter section, or directing transmit input data and clock to the receiver outputs. This "looping" is controlled by two active low logic signals, $\overline{\text{LINELP}}$ and $\overline{\text{LOCALP}}$, respectively.

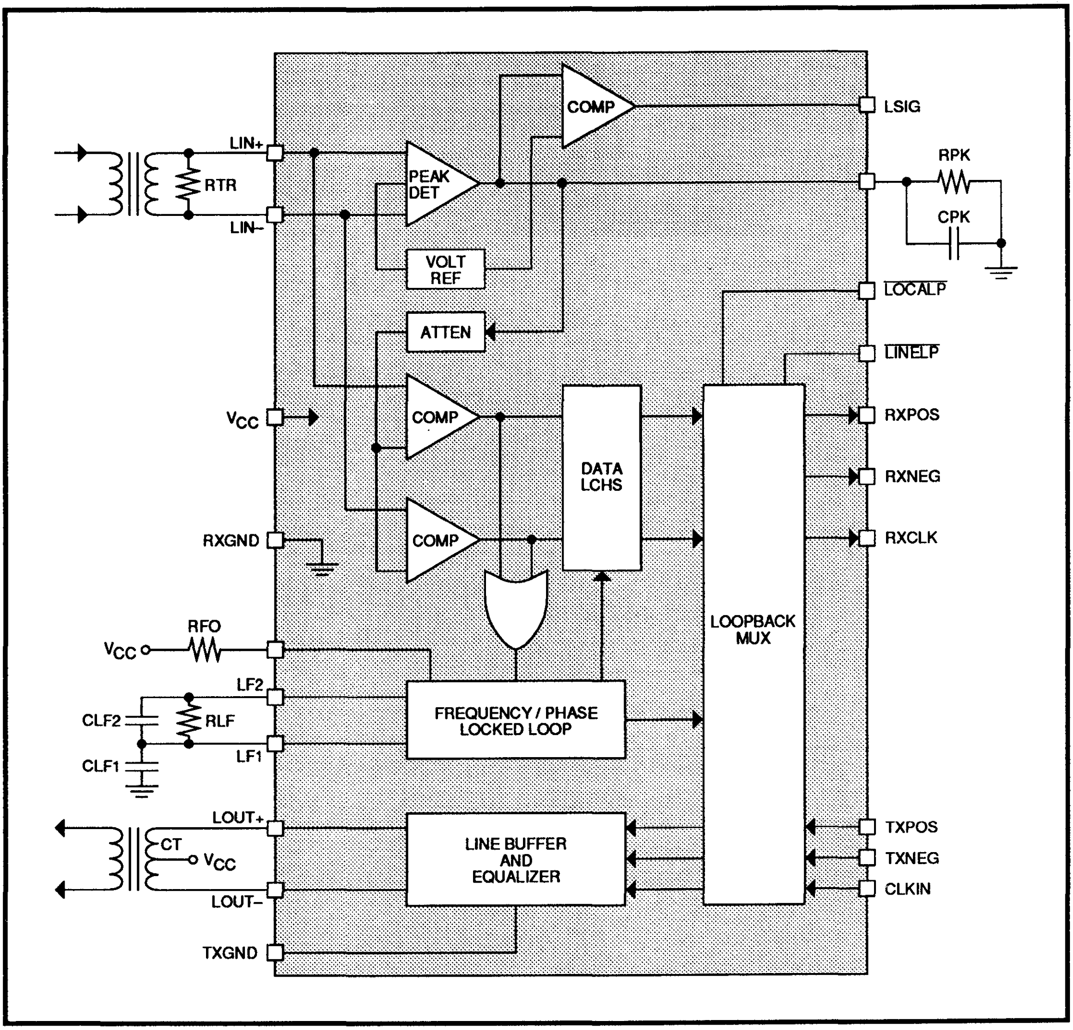


FIGURE 1: SSI 78P234 Functional Diagram

PIN DESCRIPTION

RECEIVER

I/O	LABEL	PIN NO.	DESCRIPTION
I	LIN+, LIN-	4, 5	Differential inputs, transformer-coupled from line.
O	RXPOS	7	Unipolar receiver output, active as result of positive pulse at inputs.
O	RXNEG	8	Unipolar receiver output, active as result of negative pulse at inputs.
O	RXCLK	9	Clock pulses recovered from line data.
O	LSIG	2	Loss-of-signal output indicating that input signal is less than threshold value.

TRANSMITTER

I	TXPOS	11	Unipolar transmitter data input, active high.
I	TXNEG	14	Unipolar transmitter data input, active high.
I	CLKIN	12	Transmitter clock input. Controls transmit pulse width. Transmit is active when low.
O	LOUT+	15	Output to transformer for positive data pulses.
O	LOUT-	17	Output to transformer for negative data pulses.

LOOPBACK CONTROL

I	$\overline{\text{LINELP}}$	13	Low level causes receiver recovered data and clock to be connected to the transmitter. Data and clock continue to be present at receiver outputs.
I	$\overline{\text{LOCALP}}$	10	Low level causes transmitter input data and clock to be connected to the receiver outputs. Input data continues to be transmitted.

PIN DESCRIPTION (Continued)

EXTERNAL COMPONENT CONNECTION

I/O	LABEL	PIN NO.	DESCRIPTION
I	RFO	1	Resistor connected to V_{CC} to provide basic center frequency of receiver phase locked loop oscillator.
-	LF1 LF2	19 18	Resistor-capacitor loop filter network to RXGND to establish bandwidth of phase locked loop.
-	RCPK	3	Parallel resistor-capacitor network connected to RXGND to determine charge/discharge characteristics of peak detector.

POWER

-	Vcc	20	Positive supply terminal for receiver circuits.
-	RXGND	6	Ground terminal for receiver circuits.
-	TXGND	16	Ground terminal for transmitter driver circuits.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	RATING
V_{CC}, Supply Voltage	-0.5 to +7.0V
Storage Temperature	-65 to 130°C
Soldering Temperature (10 sec.)	260°C
Voltage Applied to Logic Inputs	-0.5 to +7.0V
Maximum Power Dissipation	600 mW
Junction Operating Temperature	0 to +130°C

NOTE: All inputs and outputs are protected from static charge using built-in, industry standard protection devices and all outputs are short-circuit protected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Ta Ambient temperature		0		70	°C
V_{CC} Power supply voltage		4.75		5.25	V
VIH High-level input voltage		2.0			V
VIL Low-level input voltage				0.8	V
IOH High-level output current	LSIG pin only; VO = 1.5V	-7		-13	mA

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO Loop center frequency resistor			6.04		KΩ
RLF Loop filter resistor			10		KΩ
CLF1 Loop filter capacitor			0.015		µF
CLF2 Loop filter capacitor			200		pF
RPK Peak-detector resistor			36		KΩ
CPK Peak-detector capacitor		0.0015	0.015	0.15	µF
Transmit line transformer	Refer to Table 1		---		---

D. C. ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC Supply current	All outputs open			100	mA
IIH High-level input current	VIH = 2.7V			20	µA
IIL Low-level input current	VIL = 0.4V			-0.36	mA
VOH High-level output voltage	IOH = -400 µA	2.7			V
VOL Low-level output voltage	IOL = 4.0 mA; IOL = 2.0 mA, LSIG pin			0.4	V
RIN Receiver input resistance		800		1250	Ω

DYNAMIC CHARACTERISTICS AND TIMING, TRANSMITTER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. Transmit pulse characteristics are obtained using a line transformer which has the characteristics shown in Table 1, and with the appropriate resistive load. Refer to Figure 2.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			488		nsec
TTC	Transmit clock pulse width			244		nsec
TTCNT	Transmit clock negative transition time				10	nsec
TTCPT	Transmit clock positive transition time				10	nsec
TTPDS TTNDS	Transmit data set-up time		15			nsec
TTPDH TTNDH	Transmit data hold time		0			nsec
TTPL	Transmit positive line pulse width	Measured at transformer	TTC-5		TTC+5	nsec
TTNL	Transmit negative line pulse width		TTPL-5		TTPL+5	nsec
	Transmit line pulses waveshape	See Note				

Note: Characteristics are in accordance with Table 6 and Figure 15 of Rec. G.703.

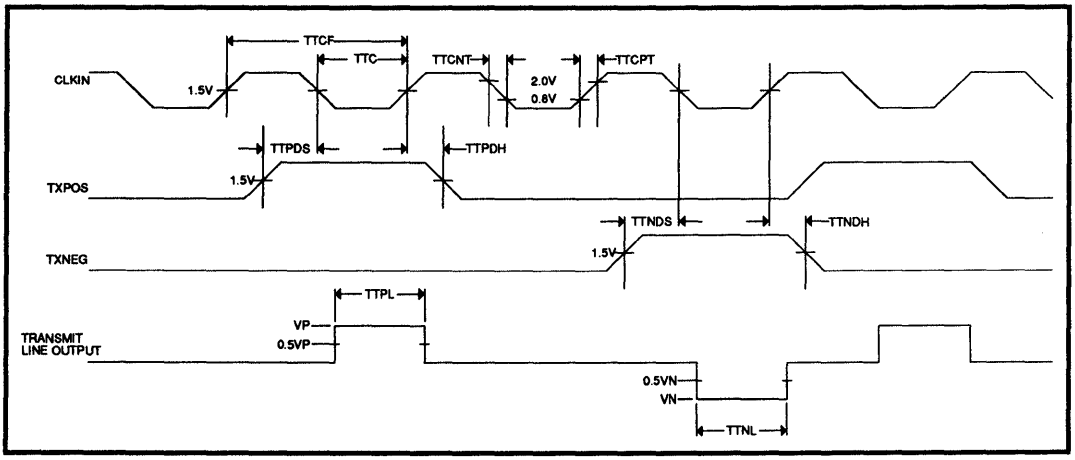


FIGURE 2: Transmit Waveforms

DYNAMIC CHARACTERISTICS AND TIMING, RECEIVER

(T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified. External component values as specified in Recommended Operating Conditions; see Note 1. Refer to Figure 3.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIN	Input signal voltage		±1.2		±3.9	Vpk
VLOS	Loss-of-signal indicating voltage		±0.5		±1.0	Vpk
TLOS	Loss-of-signal delay time	Timed from removal of input signal; See Note 2	0.7 TPK		1.3 TPK	sec
VDTH	Receive data detection threshold	Relative to peak amplitude	35		45	%
TSTAB	Receiver stabilization time	After application of input signal			5	msec
TRCF	Receive clock period			488		nsec
TRC	Receive clock pulse width			244		nsec
TRCPT	Receive clock positive transition time	C_L = 15 pF			15	nsec
TRCNT	Receive clock negative transition time	C_L = 15 pF			10	nsec
TRDP TRDN	Positive or negative receive data pulse width			488		nsec
TRDPS TRDNS	Receive data set-up time		210			nsec
TRDPH TRDNH	Receive data hold time		210			nsec
	Receive input jitter tolerance high frequency	sine, 18 KHz to 100 KHz	±100			nsec
	Receive input jitter tolerance low frequency	sine, 2.4 KHz	±750			nsec
KD	Clock Recovery Phase Detector Gain	(All 1's Data Pattern)	66		79	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Control Gain		0.40		0.55	Megrad/ sec. Volt

Note 1: Input signal is transformer coupled. In accordance with Paragraph 6.3 of Rec. G.703 and Table 2 of Rec. G.823.

Note 2: TPK = RPK x CPK x ln((VIN + 1.2v)/(VLOS + 1.2v))

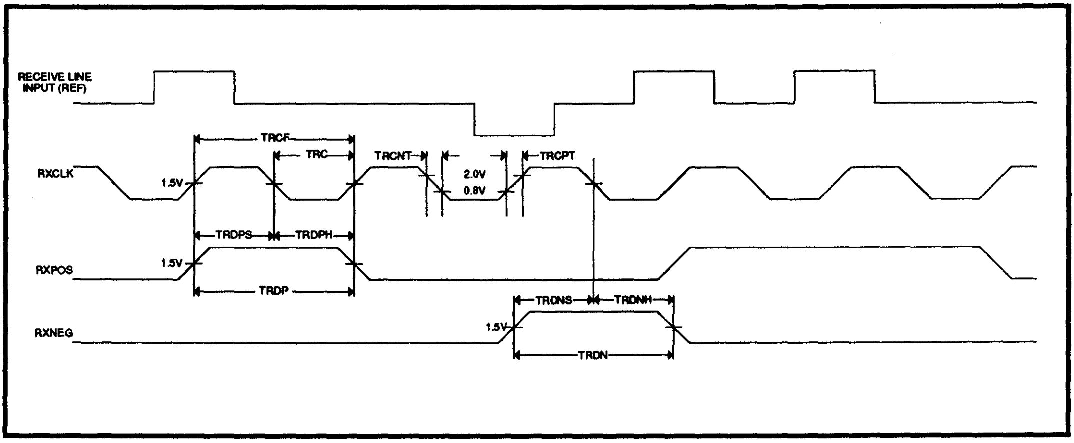


FIGURE 3: Receive Waveforms

LINE TRANSFORMERS

The SSI 78P234 is designed to connect to 75Ω coaxial or 120Ω symmetrical pair cabling. The transmitter must meet output pulse characteristics as specified by the CCITT (Table 6 of Rec. G.703) for each of these transmission media. It is important to choose a transformer that meets the specifications shown in Table 1 (below) to assure compliance with these requirements.

CHARACTERISTIC		SYMBOL	MIN	NOM	MAX	UNIT
Turns ratio	75Ω coax	N		2.53CT:1		
	120Ω twisted pair			2CT:1		
Primary open circuit inductance		Lp	3			mH
Primary leakage inductance		L1			4.0	μH
Primary volt-time product		ET	5			V-μsec
Primary DC resistance		Rp			2.5	Ω
Interwinding Capacitance		C_W			25	pF

TABLE 1: Transmit Line Transformer Characteristics

LINE TRANSFORMERS (Continued)

75Ω Coax Connection

Approximate turns ratios for connection to 75Ω coax are: 2.53 CT:1 for the transmitter and 1:1.26 (no CT) for the receiver. Some recommended transformers are listed in Table 2.

RCV/XMIT	TURNS RATIO	PART NUMBER	MANUFACTURER
XMIT	2.53CT:1	PE 64945	Pulse Engineering
XMIT	2.66CT:1	11816	Schott Corporation
RCV	1:1.26	PE 64938	Pulse Engineering

TABLE 2: Recommended Line Transformers for 75Ω Coax Connection

120Ω Symmetrical Pair Connection

Connection to 120Ω symmetrical pair requires a 2CT:1 ratio for the transmitter and 1:1 (no CT) on the receiver. Some recommendations are listed below.

RCV/XMIT	TURNS RATIO	PART NUMBER	MANUFACTURER
XMIT	2CT:1	1323	BH
XMIT	2CT:1	G52J12C	Pan-Mag
XMIT	2CT:1	11815	Schott Corporation
XMIT	1:1:1	PE 64931	Pulse Engineering
RCV	1:1	PE 64935	Pulse Engineering
RCV	1:1:1	G52J111P	Pan-Mag

TABLE 3: Recommended Line Transformers for 120Ω Symmetrical Pair Connection

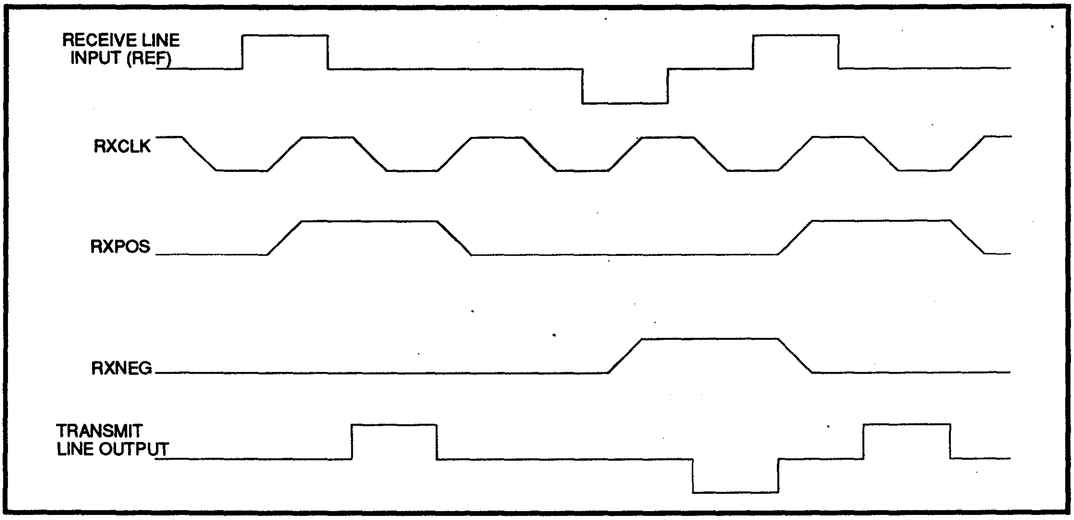


FIGURE 4: Line Loopback Waveforms

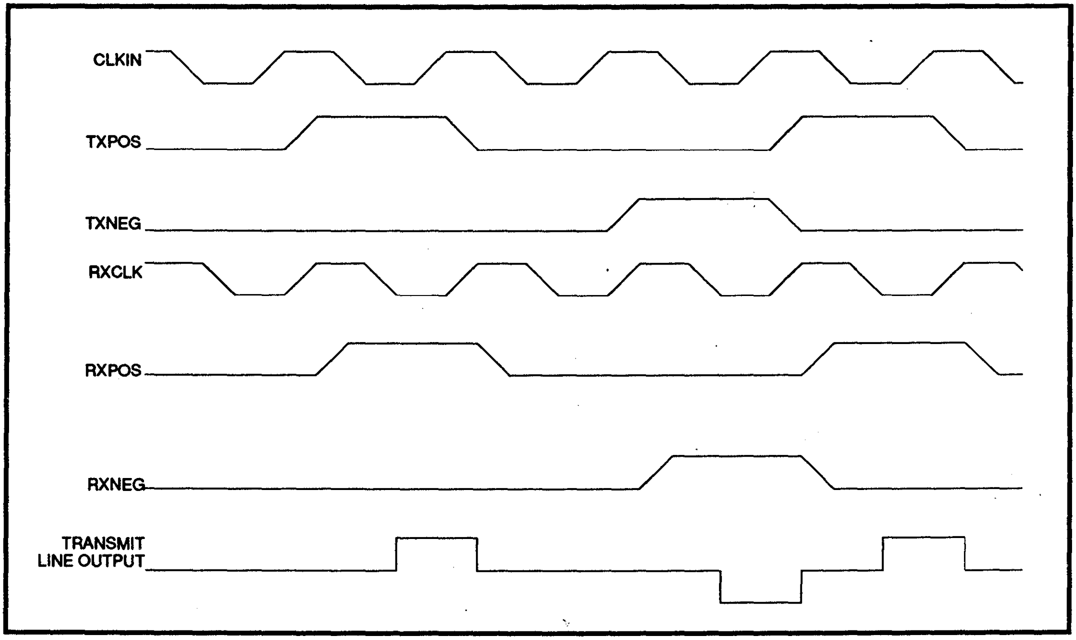
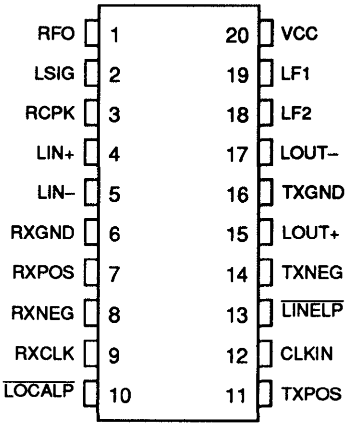


FIGURE 5: Local Loopback Waveforms

SSI 78P234
2048 KBit/s
PCM Interface Unit

PACKAGE PIN DESIGNATIONS

(Top View)



20-Pin DIP, SO

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
SSI 78P234		
20-Pin Plastic DIP	78P234-CP	78P234-CP
20-Pin SO	78P234-CL	78P234-CL

silicon systems®
A TDK Group Company

SSI 78P236
DS-3 Line Interface

December 1992

DESCRIPTION

The SSI 78P236 is a line interface transceiver IC intended for DS-3 (44.736 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, positive data, negative data, and low-level signal detector logical outputs. The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) equalizer may be selected to shape the outgoing pulses for shorter line lengths. The SSI 78P236 requires a single 5-volt supply and is available in DIP and surface mount packages.

FUNCTIONAL DESCRIPTION

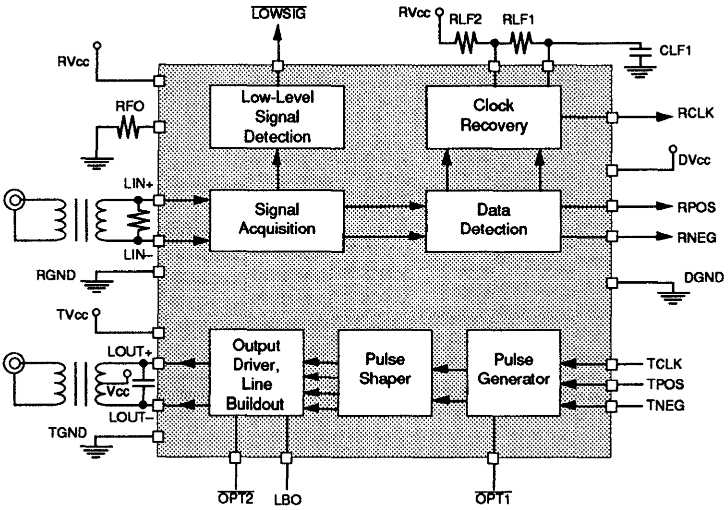
The SSI 78P236 is a single chip line interface IC designed to work with 44.736 Mbit/s DS-3 signals. The receiver recovers 44.736 MHz clock, positive data and negative data from an Alternate Mark Inversion (AMI) signal which has travelled a maximum of 450 feet from a DSX3 crosspoint over 75Ω coaxial cable (cable type WECO 728A, RG-59B or equivalent). The wide dynamic range of SSI 78P236 allows for additional resistive attenuation. The input DS-3 signal should be B3ZS coded.

(continued)

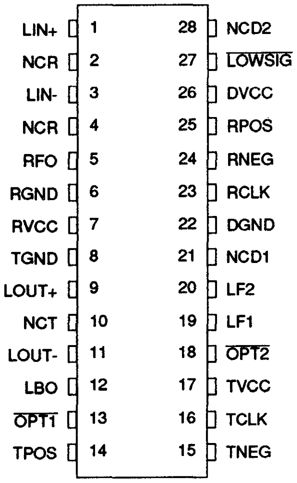
FEATURES

- **Single chip transmit and receive interface for DS-3 (44.736 Mbit/s) applications**
- **Unique clock recovery circuit, requires no crystals, tuned components or external clock**
- **Selectable transmit line buildout (LBO) to accommodate shorter line lengths**
- **Standard CMOS level unipolar POS and NEG data and CLK ports**
- **Compliant with ANSI T1.102 - 1987, TR-TSY-000499 and CCITT G.703**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **-40°C to +85°C operating range**
- **Pin-compatible with SSI 78P2361, 78P2362 and 78P7200**

BLOCK DIAGRAM



PIN DIAGRAM



28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION (continued)

The transmitter accepts CMOS level logical clock, positive data and negative data and converts them to the AMI signal to drive a 75Ω coaxial cable. Programmable internal Line Buildout (LBO) circuitry eliminates the need for external LBO networks. The shape of the transmitted signal through any cable length of 0 to 450 feet complies with the published templates of ANSI T.102-1987, CCITT G.703 and TR-TSY-000499. The SSI 78P236 is designed to work with a B3ZS coded signal. The B3ZS encoding and decoding functions are normally included in the DS-3 framer ICs or can easily be implemented in a PAL.

RECEIVER

The receiver input is normally transformer-coupled to the DS-3 signal. The inputs to the IC are internally referenced to RVCC so that when no transformer is used, a DC blocking capacitor of 0.01 µF should be used to isolate these pins from the DS-3 signal. Since the input impedance of the SSI 78P236 is high, the DS-3 line must be terminated in 75Ω. The input signal to the SSI 78P236 must be limited to a maximum of three consecutive zeros using a coding scheme such as B3ZS or HDB3.

The DS-3 signal is input to a variable gain differential amplifier whose output is maintained at a constant voltage level regardless of the input voltage level. The gain of this amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

The output of the variable gain amplifier is compared to a threshold value which is a fixed percentage of the signal peak. In this way, even though the input signal amplitude may fall below the minimum value that can be regulated by the variable gain circuit, the proper detection threshold is maintained.

Output of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high precision and/or adjustable oscillator or tuned circuits. The response characteristic for the phase locked loop is established by external filter components, RLF1, RLF2 and CLF1. The values of these components are specified such that the bandwidth of the phase locked loop is greater than 200 kHz.

The jitter tolerance of the SSI 78P236 exceeds the requirements of TR-TSY-000499 for the category II of equipments. The jitter transfer function is maximally flat so the IC doesn't add any jitter to the system.

Figure 2 shows the recovered clock (RCLK), positive data (RPOS) and negative data (RNEG) signals timing. The data is valid on the rising edge of the clock. The minimum setup and hold times allow easy interface to all DS-3 framer circuits. These signals are CMOS-level outputs.

Should the input signal fall below a minimum value, the $\overline{\text{LOWSIG}}$ pin goes active low. A time delay is provided before this output is active so the transient interruptions do not needlessly cause the indication.

TRANSMITTER

The transmitter accepts unipolar CMOS-level logical clock, positive data and negative data signals (TCLK, TPOS, TNEG) and generates high current drive pulses on the LOUT+ and LOUT- pins. When properly connected to a center tapped transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable (type WE728A or RG59B).

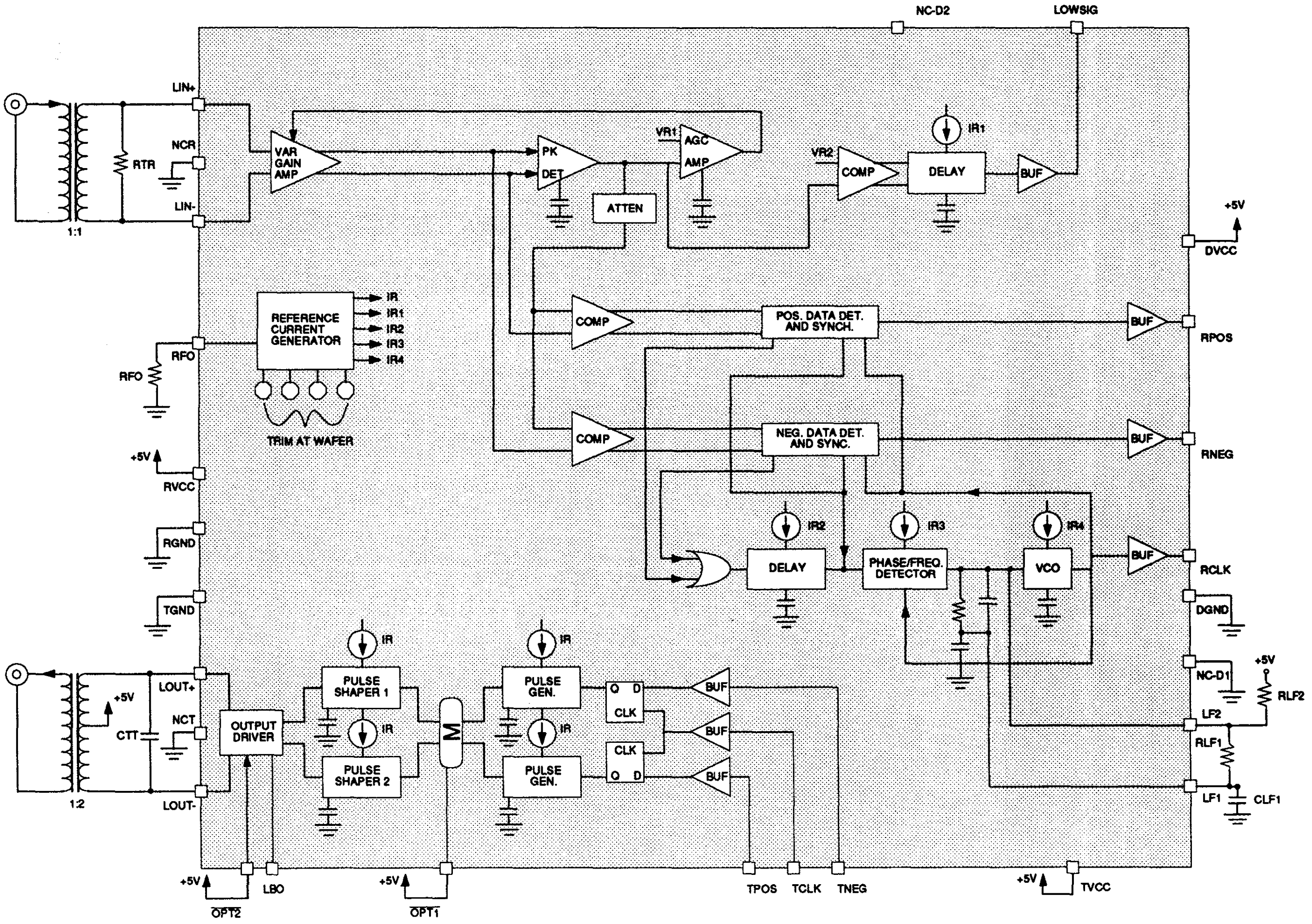
Figure 3 shows the timing for the transmitter logic signals. The output pulse width is internally set and is not sensitive to input clock (TCLK) pulse width.

When a recommended transformer is used, the transmitted pulse shape at the end of a 75Ω terminated cable of 0 to 450 feet will fit the template for DSX3 pulse published in ANSI T1.102-1987, BELLCORE TR-TSY-000499 and CCITT G.703 documents.

The SSI 78P236 incorporates a selectable Line Buildout (LBO) equalizer in the transmitter path. The LBO pin should be set HIGH if the cable is shorter than 225 feet. For longer cable lengths, the LBO pin should be set low.

The $\overline{\text{OPT1}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT1}}$ pin to LOW increases the transmitter power.

The $\overline{\text{OPT2}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT2}}$ pin to LOW disables the transmitter circuitry and reduces the power consumption of the IC by 125 mW.



Note: NC pins should be tied to the ground pin indicated by the trailing letter.

FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Selected for shorter cable lengths.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude when low.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NCR, NCT NCD1	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin (see figure 1) to minimize pin-to-pin coupling capacitance.
NCD2	-	No connect. This pin is not connected for compatibility to SSI 78P7200.

ELECTRICAL SPECIFICATIONS

(TA = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOULUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive 5.0V supply: TVcc, RVcc, DVcc	6.0	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Ambient Operating Temperature, TA	-40 to +85	°C
Pin Ratings: LIN+, LIN-, TPOS, TNEG, TCLK, LOUT+, LOUT-, LBO, RFO, LF2, LF1, $\overline{\text{OPT1}}$, $\overline{\text{OPT2}}$ Pins	-0.3 to Vcc +0.3	V
Pin Ratings: RPOS, RNEG, RCLK, $\overline{\text{LOWSIG}}$ Pins	-0.3 to Vcc +0.3	V
	or +12	mA

SUPPLY CURRENTS AND POWER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC Supply Current	Outputs Unloaded, normal operation, transmit and receive all 1's pattern		142	174	mA
P Power Dissipation	Outputs unloaded, TA = 85°C			0.93	W

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO Loop center frequency resistor	1% tolerance		5.23		kΩ
RLF1 Loop filter resistor	1%		20		kΩ
RLF2 Loop filter resistor	1%		100		kΩ
CLF1 Loop filter capacitor	5%		0.22		µF
RTR Receive termination resistor	1%		75		Ω
CTT Transmit termination capacitor	5%			20	pF

ELECTRICAL SPECIFICATIONS (Continued)

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, $\overline{\text{OPT1}}$.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input low voltage		-0.3		1.5	V
VIH	Input high voltage		3.5		Vcc +0.3	V
IIL	Input low current	VIL = 1.5V	-5.0		5.0	µA
IIH	Input high current	VIH = 3.5V	-5.0		5.0	µA
VOL	Output low voltage	IOL = 0.1 mA			1.0	V
VOH	Output high voltage	IOH = -0.1 mA	4.0			V

$\overline{\text{OPT2}}$ CHARACTERISTICS

VIL	Input low voltage	IIL = 0.4 mA			0.5	V
VIH	Input high voltage		2.0			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled as shown in Figure 1.
2. RFO = 5.25 kΩ
3. The circuit is connected as in Figure 1.
4. The maximum cable length (type 728-A or RG-59B) to DSX-3 point is 450 ft.

VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		50		%
VLOW	Receive data low signal threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		±55		mV
VLOWT	Receive data low signal delay	Relative to peak amplitude for 22.37 MHz sinusoidal input		1.5		µs
TRCF	Receive clock period			22.35		ns
TRC	Receive clock pulse width			12.24		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns

RECEIVER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRDP TRDN	Positive or negative receive data pulse width			22.35		ns
TRDPS TRDNS	Receive data set-up time		5	11.18	13.7	ns
TRDPH TRDNH	Receive data hold time		5	11.18	13.7	ns
	Receive input jitter tolerance high frequency	sine, 60 kHz to 300 kHz	±3.35			ns
			0.3			UIPP
	Receive input jitter tolerance low frequency	sine, 10 Hz to 2.3 kHz	±55.88			ns
			5.0			UIPP
KD	Clock Recovery Phase Detector Gain	All 1's data pattern KD = .418/RFO	72	80	88	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Gain		12	14.5	17	Mrad/ sec. -Volt

TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics TBD.
2. The circuit is connected as in Figure 1.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			22.35		ns
TTC	Transmit clock pulse width			11.18		ns
TTCNT	Transmit clock negative transition time			4.5	6	ns
TTCPT	Transmit clock positive transition time			4.5	6	ns
TTPDS TTNDS	Transmit data set-up time		3.5	11.18		ns
TTPDH TTNDH	Transmit data hold time		3.5	11.18		ns
TTPL	Transmit positive line pulse width	Measured at transformer, LBO = Low	10.62	11.18	12.0	ns

TRANSMITTER (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TTNL Transmit negative line pulse width	Measured at transformer, LBO = Low	10.62	11.18	12.0	ns
Transmit line pulse waveshape	See Note				

Note: Characteristics are in accordance with ANSI T1.102 - 1987, Table 5 and Figure 8.

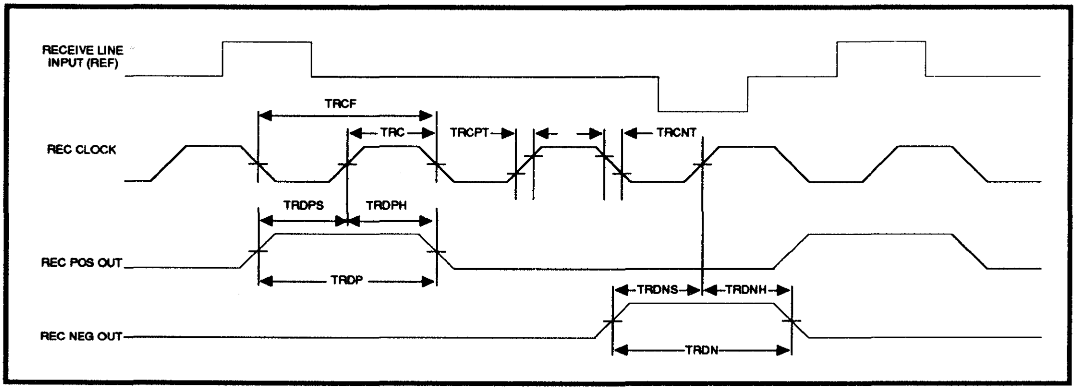


FIGURE 2: Receive Waveforms

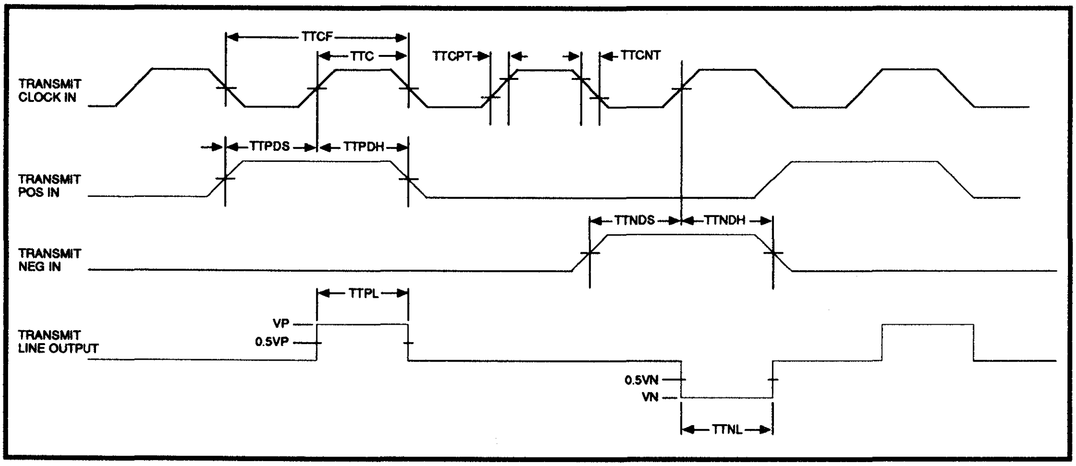
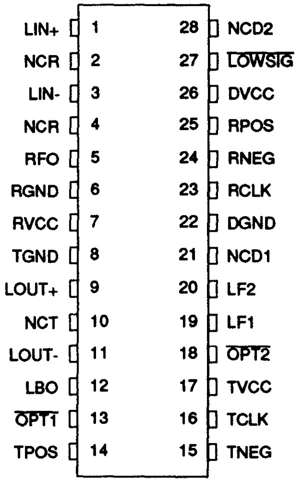


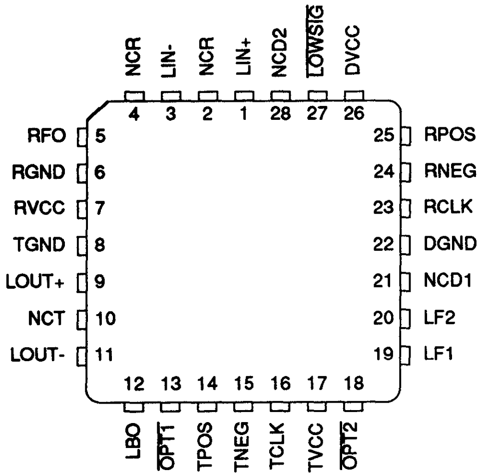
FIGURE 3: Transmit Waveforms

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78P236, DS-3 Line Interface – 28-pin		
Standard Width Plastic DIP (600 mil)	78P236-IP	78P236-IP
Surface Mount 28-pin PLCC	78P236-IH	78P236-IH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914

Notes:

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A TDK Group Company

SSI 78P2361
STS-1 Line Interface

December 1992

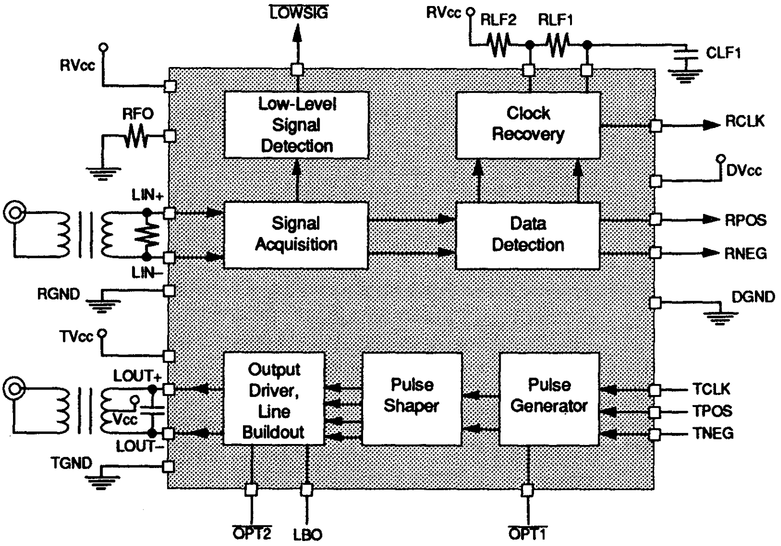
DESCRIPTION

The SSI 78P2361 is a line interface transceiver IC intended for STS-1 (51.84 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, positive data, negative data, and low-level signal detector logical outputs. The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) equalizer may be selected to shape the outgoing pulses for shorter line lengths. The SSI 78P2361 requires a single 5-volt supply and is available in DIP and surface mount packages.

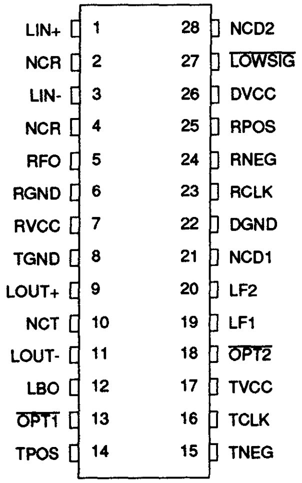
FEATURES

- **Single chip transmit and receive interface for STS-1 (51.84 Mbit/s) applications**
- **Unique clock recovery circuit, requires no crystals, tuned components or external clock**
- **Selectable transmit line buildout (LBO) to accommodate shorter line lengths**
- **Standard CMOS level unipolar POS and NEG data and CLK ports**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **-40°C to +85°C operating range**
- **Pin-compatible with SSI 78P236 and 78P2362**

BLOCK DIAGRAM



PIN DIAGRAM



28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78P2361 is a single chip line interface IC designed to work with 51.84 Mbit/s STS-1 signals. The receiver recovers 51.84 MHz clock, positive data and negative data from an Alternate Mark Inversion (AMI) signal which has travelled a maximum of 450 feet from a crosspoint over 75Ω coaxial cable (cable type WECO 728A, RG-59B or equivalent). The wide dynamic range of 78P2361 allows for additional resistive attenuation. The input STS-1 signal should be B3ZS coded.

The transmitter accepts CMOS level logical clock, positive data and negative data and converts them to the AMI signal to drive a 75Ω coaxial cable. Programmable internal Line Buildout (LBO) circuitry eliminates the need for external LBO networks. The shape of the transmitted signal through any cable length of 0 to 450 feet will match a scaled DS-3 template. The SSI 78P2361 is designed to work with a B3ZS coded signal. The B3ZS encoding and decoding functions are normally included in the STS-1 framer ICs or can easily be implemented in a PAL.

RECEIVER

The receiver input is normally transformer-coupled to the STS-1 signal. The inputs to the IC are internally referenced to RVCC so that when no transformer is used, a DC blocking capacitor of 0.01 µF should be used to isolate these pins from the STS-1 signal. Since the input impedance of the SSI 78P2361 is high, the STS-1 line must be terminated in 75Ω. The input signal to the SSI 78P2361 must be limited to a maximum of two consecutive zeros using a coding scheme such as B3ZS.

The STS-1 signal is input to a variable gain differential amplifier whose output is maintained at a constant voltage level regardless of the input voltage level. The gain of this amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

The output of the variable gain amplifier is compared to a threshold value which is a fixed percentage of the signal peak. In this way, even though the input signal amplitude may fall below the minimum value that can be regulated by the variable gain circuit, the proper detection threshold is maintained.

Output of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high precision and/or adjustable oscillator or tuned circuits.

The response characteristic for the phase locked loop is established by external filter components, RLF1, RLF2 and CLF1. The values of these components are specified such that the bandwidth of the phase locked loop is greater than 200 kHz.

The jitter transfer function of the 78P2361 should be set maximally flat so the IC doesn't add any jitter to the system.

Figure 2 shows the recovered clock (RCLK), positive data (RPOS) and negative data (RNEG) signals timing. The data is valid on the rising edge of the clock. The minimum setup and hold times allow easy interface to many STS-1 framer circuits. These signals are CMOS-level outputs.

Should the input signal fall below a minimum value, the $\overline{\text{LOWSIG}}$ pin goes active low. A time delay is provided before this output is active so the transient interruptions do not needlessly cause the indication.

TRANSMITTER

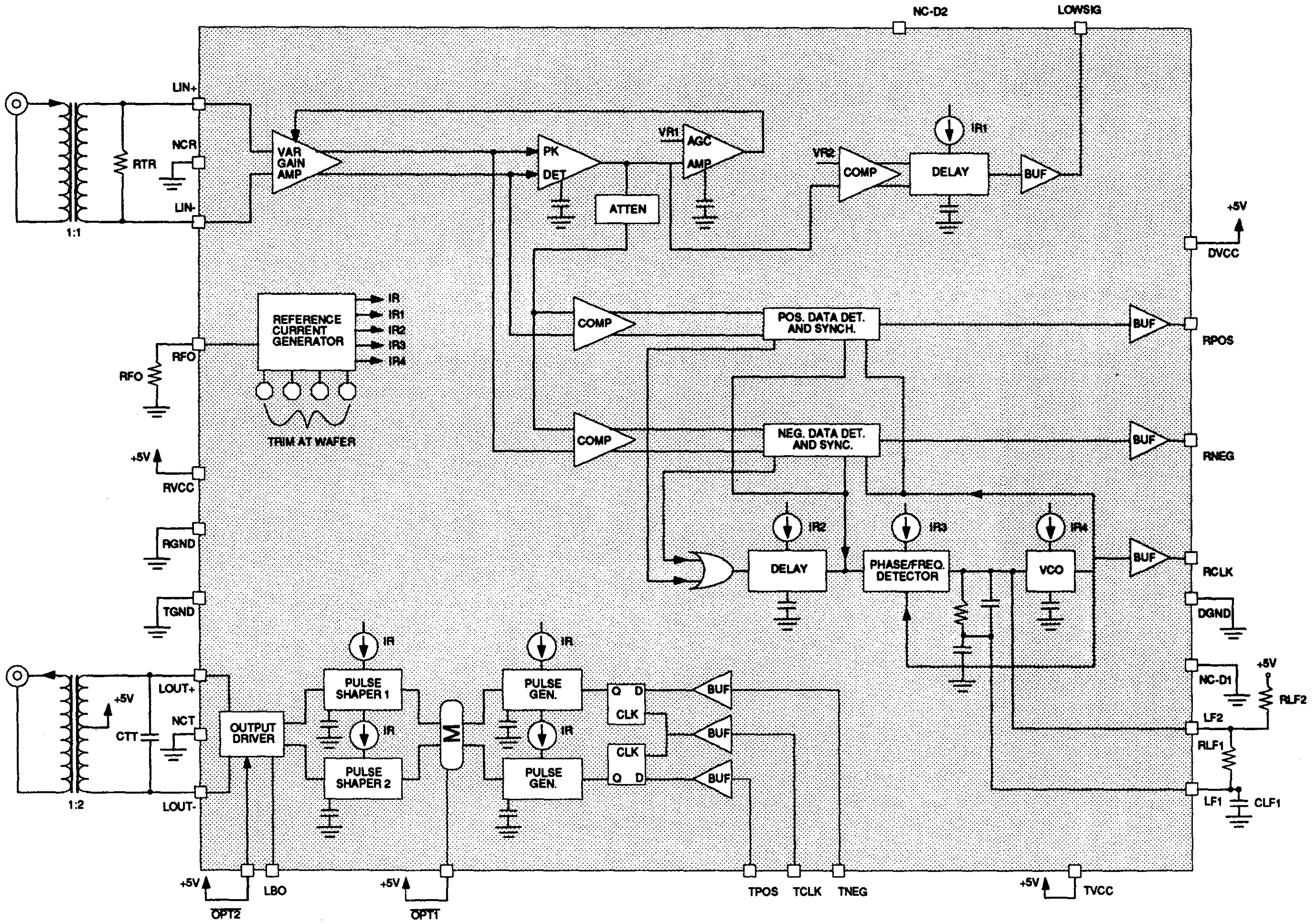
The transmitter accepts unipolar CMOS level logical clock, positive data and negative data signals (TCLK, TPOS, TNEG) and generates high current drive pulses on the LOUT+ and LOUT- pins. When properly connected to a center tapped transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable (type WE728A or RG59B).

Figure 3 shows the timing for the transmitter logic signals. The output pulse width is internally set and is not sensitive to input clock (TCLK) pulse width.

The SSI 78P2361 incorporates a selectable Line Buildout (LBO) equalizer in the transmitter path. The LBO pin should be set HIGH if the cable is shorter than 225 feet. For longer cable lengths, the LBO pin should be set LOW.

The $\overline{\text{OPT1}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT1}}$ pin to LOW increases the transmitter power.

The $\overline{\text{OPT2}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT2}}$ pin to LOW disables the transmitter circuity and reduces the power consumption of the IC by 125 mW.



Note: NC pins should be tied to the ground pin indicated by the trailing letter.

FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Selected for shorter cable lengths.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude when low.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NCR, NCT NCD1	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin (see figure 1) to minimize pin-to-pin coupling capacitance.
NCD2	-	No connect. This pin is not connected for compatibility to SSI 78P200.

ELECTRICAL SPECIFICATIONS

(TA = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOULUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive 5.0V supply: TVcc, RVcc, DVcc	6.0	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Ambient Operating Temperature, TA	-40 to +85	°C
Pin Ratings: LIN+, LIN-, TPOS, TNEG, TCLK, LOUT+, LOUT-, LBO, RFO, LF2, LF1, $\overline{\text{OPT1}}$, $\overline{\text{OPT2}}$ Pins	-0.3 to Vcc +0.3	V
Pin Ratings: RPOS, RNEG, RCLK, $\overline{\text{LOWSIG}}$ Pins	-0.3 to Vcc +0.3	V
	or +12	mA

SUPPLY CURRENTS AND POWER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC Supply Current	Outputs Unloaded, normal operation, transmit and receive all 1's pattern		142	174	mA
P Power Dissipation	Outputs unloaded, TA = 85°C			0.93	W

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO Loop center frequency resistor	1% tolerance		4.53		kΩ
RLF1 Loop filter resistor	1%		20		kΩ
RLF2 Loop filter resistor	5%		100		kΩ
CLF1 Loop filter capacitor	5%		0.22		µF
RTR Receive termination resistor	1%		75		Ω
CTT Transmit termination capacitor	5%			20	pF

ELECTRICAL SPECIFICATIONS (Continued)

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, $\overline{\text{OPT1}}$.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input low voltage		-0.3		1.5	V
VIH	Input high voltage		3.5		Vcc +0.3	V
IIL	Input low current	VIL = 1.5V	-5.0		5.0	µA
IIH	Input high current	VIH = 3.5V	-5.0		5.0	µA
VOL	Output low voltage	IOL = 0.1 mA			1.0	V
VOH	Output high voltage	IOH = -0.1 mA	4.0			V

$\overline{\text{OPT2}}$ CHARACTERISTICS

VIL	Input low voltage	IIL = 0.4 mA			0.5	V
VIH	Input high voltage		2.0			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled as shown in Figure 1.
2. RFO = 4.53 kΩ
3. The circuit is connected as in Figure 1.
4. The maximum cable length (type 728-A or RG-59B) to DSX-3 point is 450 ft.

VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 25.92 MHz sinusoidal input		50		%
VLOW	Receive data low signal threshold	Relative to peak amplitude for 25.92 MHz sinusoidal input		±55		mV
VLOWT	Receive data low signal delay	Relative to peak amplitude for 22.37 MHz sinusoidal input		1.5		µs
TRCF	Receive clock period			19.29		ns
TRC	Receive clock pulse width			10.99		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns

RECEIVER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRDP TRDN	Positive or negative receive data pulse width			19.29		ns
TRDPS TRDNS	Receive data set-up time		5	9.65	11.82	ns
TRDPH TRDNH	Receive data hold time		5	9.65	11.82	ns
	Receive input jitter tolerance	sine, 60 kHz	±2.89			ns
	high frequency	to 300 kHz	0.3			UIPP
	Receive input jitter tolerance	sine, 10 Hz to 2.3 kHz	±48.22			ns
	low frequency		5.0			UIPP
KD	Clock Recovery Phase Detector Gain	All 1's data pattern KD = .418/RFO	83	92	101	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Gain		12	14.5	17	Mrad/ sec. -Volt

TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics TBD.
2. The circuit is connected as in Figure 1.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			19.29		ns
TTC	Transmit clock pulse width		8.20	9.65	11.09	ns
TTCNT	Transmit clock negative transition time			4.5	6	ns
TTCPT	Transmit clock positive transition time			4.5	6	ns
TTPDS TTNDS	Transmit data set-up time		3.5	9.65		ns
TTPDH TTNDH	Transmit data hold time		3.5	9.65		ns
TTPL	Transmit positive line pulse width	Measured at transformer, LBO = Low		9.65		ns

TRANSMITTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTNL	Transmit negative line pulse width	Measured at transformer, LBO = Low		9.65		ns
	Transmit line pulse waveshape	See Note				

Note: The pulse template fits a scaled DSX-3 pulse template.

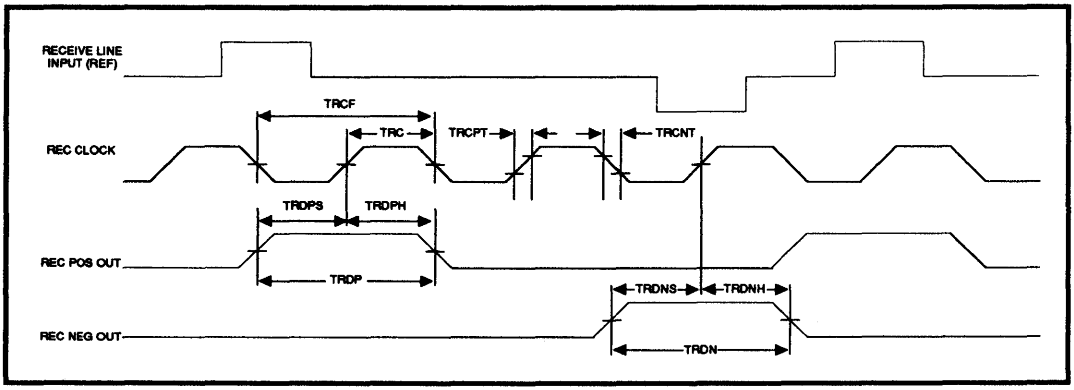


FIGURE 2: Receive Waveforms

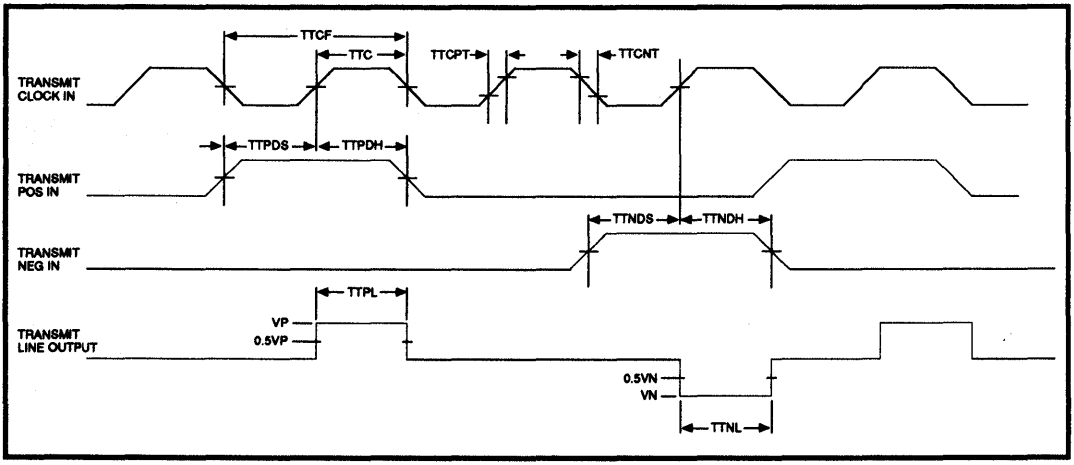
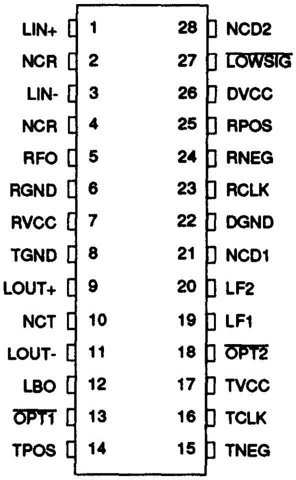


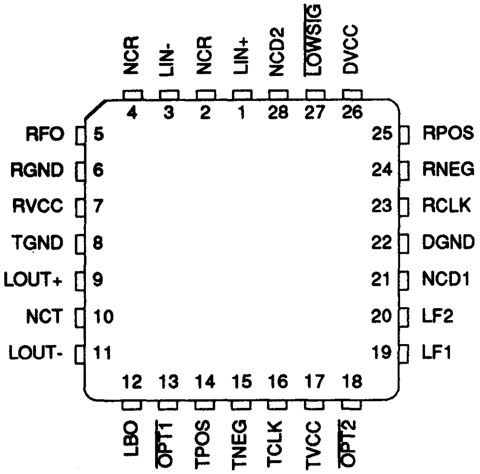
FIGURE 3: Transmit Waveforms

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin DIP



28-Pin PLCC

5

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78P2361, STS-1 Line Interface – 28-pin		
Standard Width Plastic DIP (600 mil)	78P2361-IP	78P2361-IP
Surface Mount 28-pin PLCC	78P2361-IH	78P2361-IH

Notes:

silicon systems®
A TDK Group Company

SSI 78P2362

34.368 Mbit/s Line Interface

Preliminary Data

December 1992

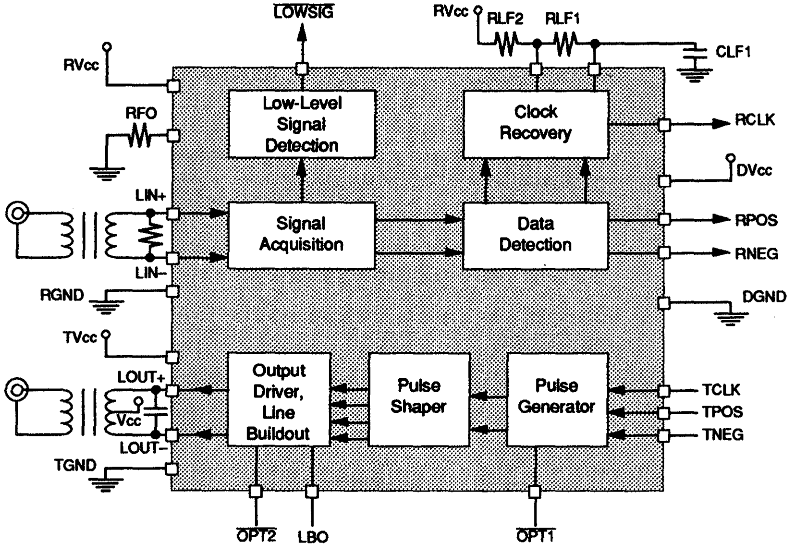
DESCRIPTION

The SSI 78P2362 is a line interface transceiver IC intended for 34.368 Mbit/s applications. The receiver has a very wide dynamic range and is designed to accept HDB3 encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, positive data, negative data, and low-level signal detector logical outputs. The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. The SSI 78P2362 requires a single 5-volt supply and is available in DIP and surface mount packages.

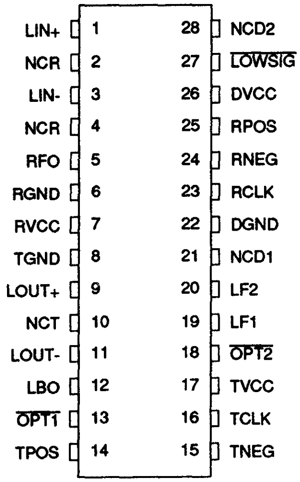
FEATURES

- **Single chip transmit and receive interface for E3 (34.368 Mbit/s) applications**
- **Unique clock recovery circuit, requires no crystals, tuned components or external clock**
- **Standard CMOS level unipolar POS and NEG data and CLK ports**
- **Compliant with CCITT recommendation G.703 and G.823**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **-40°C to +85°C operating range**
- **Pin-compatible with SSI 78P236 and 78P2361**

BLOCK DIAGRAM



PIN DIAGRAM



28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78P2362 is a single chip line interface IC designed to work with 34.368 Mbit/s E3 signals. The receiver recovers 34.368 MHz clock, positive data and negative data from an Alternate Mark Inversion (AMI) signal which has travelled a maximum of 450 feet from a crosspoint over 75Ω coaxial cable (cable type WECO 728A, RG-59B or equivalent). The wide dynamic range of SSI 78P2362 allows for additional resistive attenuation. The input E3 signal must be HDB3 coded.

The transmitter accepts CMOS level logical clock, positive data and negative data and converts them to the AMI signal to drive a 75Ω coaxial cable. The transmitted signal meets the requirements of the CCITT G.703 recommendations. The SSI 78P2362 is designed to work with HDB3 coded signal. The HDB3 encoding and decoding functions are normally included in the E3 framer ICs or can easily be implemented in a PAL.

RECEIVER

The receiver input is normally transformer-coupled to the E3 signal. The inputs to the IC are internally referenced to RVCC so that when no transformer is used, a DC blocking capacitor of 0.01 µF should be used to isolate these pins from the E3 signal. Since the input impedance of the SSI 78P2362 is high, the E3 line must be terminated in 75Ω. The input signal to the SSI 78P2362 must be limited to a maximum of three consecutive zeros using a coding scheme such as HDB3.

The E3 signal is input to a variable gain differential amplifier whose output is maintained at a constant voltage level regardless of the input voltage level. The gain of this amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

The output of the variable gain amplifier is compared to a threshold value which is a fixed percentage of the signal peak. In this way, even though the input signal amplitude may fall below the minimum value that can be regulated by the variable gain circuit, the proper detection threshold is maintained.

Output of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator. This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high precision and/or adjustable oscillator or tuned circuits.

The response characteristic for the phase locked loop is established by external filter components, RLF1, RLF2 and CLF1. The values of these components are specified such that the bandwidth of the phase locked loop is greater than 200 kHz.

The jitter tolerance of the SSI 78P236 meets the requirements of CCITT G.823. The jitter transfer function of the SSI 78P2362 should be maximally flat so the IC doesn't add any jitter to the system.

Figure 2 shows the recovered clock (RCLK), positive data (RPOS) and negative data (RNEG) signals timing. The data is valid on the rising edge of the clock. The minimum setup and hold times allow easy interface to many E3 framer circuits. These signals are CMOS-level outputs.

Should the input signal fall below a minimum value, the $\overline{\text{LOWSIG}}$ pin goes active low. A time delay is provided before this output is active so the transient interruptions do not needlessly cause the indication.

TRANSMITTER

The transmitter accepts unipolar CMOS level logical clock, positive data and negative data signals (TCLK, TPOS, TNEG) and generates high current drive pulses on the LOUT+ and LOUT- pins. When properly connected to a center tapped transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable (type WE728A or RG59B).

Figure 3 shows the timing for the transmitter logic signals. The output pulse width is internally set and is not sensitive to input clock (TCLK) pulse width.

The LBO pin should be set LOW. The $\overline{\text{OPT1}}$ pin should be set LOW.

The $\overline{\text{OPT2}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT2}}$ pin to LOW disables the transmitter circuity and reduces the power consumption of the IC by 125 mW.

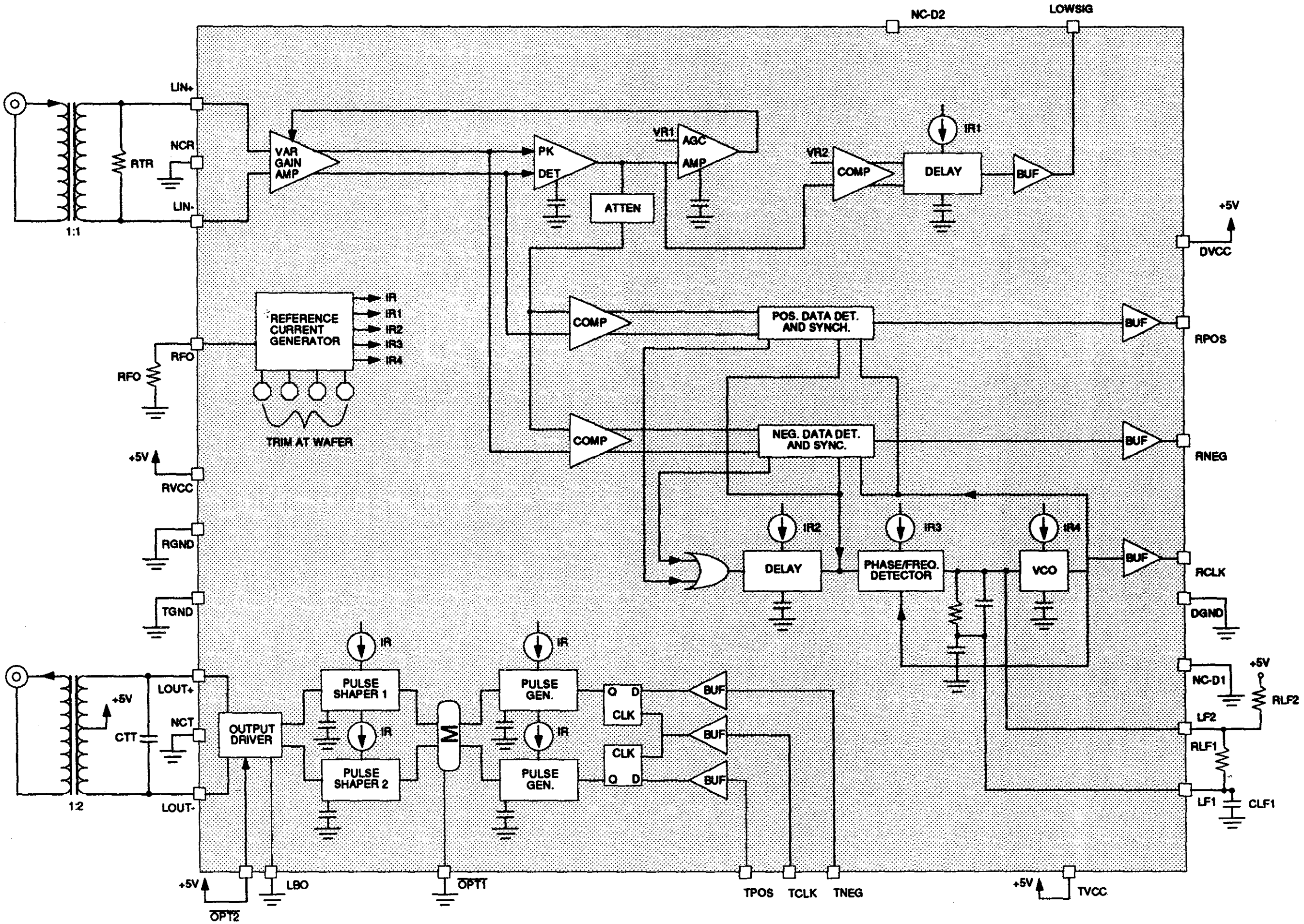


FIGURE 1: Functional Diagram

Note: NC pins should be tied to the ground pin indicated by the trailing letter.

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Attenuates output pulses. Should be tied low for normal CEPT E3 applications.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude. Should be tied low for normal CEPT E3 applications.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NCR, NCT NCD1	- -	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin (see figure 1) to minimize pin-to-pin coupling capacitance.
NCD2	-	No connect. This pin is not connected.

ELECTRICAL SPECIFICATIONS

(T_A = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOULUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive 5.0V supply: TVcc, RVcc, DVcc	6.0	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Ambient Operating Temperature, T_A	-40 to +85	°C
Pin Ratings: LIN+, LIN-, TPOS, TNEG, TCLK, LOUT+, LOUT-, LBO, RFO, LF2, LF1, $\overline{\text{OPT1}}$, $\overline{\text{OPT2}}$ Pins	-0.3 to Vcc +0.3	V
Pin Ratings: RPOS, RNEG, RCLK, $\overline{\text{LOWSIG}}$ Pins	-0.3 to Vcc +0.3	V
	or +12	mA

SUPPLY CURRENTS AND POWER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC Supply Current	Outputs Unloaded, normal operation, transmit and receive all 1's pattern		142	174	mA
P Power Dissipation	Outputs unloaded, T_A = 85°C			0.93	W

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO Loop center frequency resistor	1% tolerance		6.81		kΩ
RLF1 Loop filter resistor	1%		20		kΩ
RLF2 Loop filter resistor	1%		100		kΩ
CLF1 Loop filter capacitor	5%		0.22		µF
RTR Receive termination resistor	1%		75		Ω
CTT Transmit termination capacitor	5%			20	pF

ELECTRICAL SPECIFICATIONS (Continued)

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, $\overline{\text{OPT1}}$.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input low voltage		-0.3		1.5	V
VIH	Input high voltage		3.5		Vcc +0.3	V
IIL	Input low current	VIL = 1.5V	-5.0		5.0	µA
IIH	Input high current	VIH = 3.5V	-5.0		5.0	µA
VOL	Output low voltage	IOL = 0.1 mA			1.0	V
VOH	Output high voltage	IOH = -0.1 mA	4.0			V

$\overline{\text{OPT2}}$ CHARACTERISTICS

VIL	Input low voltage	IIL = 0.4 mA			0.5	V
VIH	Input high voltage		2.0			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled as shown in Figure 1.
2. RFO = 6.81 kΩ
3. The circuit is connected as in Figure 1.
4. The maximum cable length (type 728-A or RG-59B) to DSX-3 point is 450 ft.

VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 17.18 MHz sinusoidal input		50		%
VLOW	Receive data low signal threshold	Relative to peak amplitude for 17.18 MHz sinusoidal input		±55		mV
VLOWT	Receive data low signal delay	Relative to peak amplitude for 17.18 MHz sinusoidal input		1.5		µs
TRCF	Receive clock period			29.1		ns
TRC	Receive clock pulse width			16.58		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns

RECEIVER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRDP TRDN	Positive or negative receive data pulse width			29.1		ns
TRDPS TRDNS	Receive data set-up time		5	14.55	17.83	ns
TRDPH TRDNH	Receive data hold time		5	14.55	17.83	ns
	Receive input jitter tolerance	sine, 10 kHz	±2.18			ns
	high frequency	to 800 kHz	0.1			UIPP
	Receive input jitter tolerance	sine, 100 Hz to 1.0 kHz	±21.83			ns
	low frequency		10			UIPP
KD	Clock Recovery Phase Detector Gain	All 1's data pattern KD = .418/RFO	56	62	68	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Gain		12	14.5	17	Mrad/ sec. -Volt

TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics TBD.
2. The circuit is connected as in Figure 1.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			29.1		ns
TTC	Transmit clock pulse width		12.36	14.55	16.73	ns
TTCNT	Transmit clock negative transition time			4.5	6	ns
TTCPT	Transmit clock positive transition time			4.5	6	ns
TTPDS TTNDS	Transmit data set-up time		3.5	14.55		ns
TTPDH TTNDH	Transmit data hold time		3.5	14.55		ns
TTPL	Transmit positive line pulse width	Measured at $\overline{\text{OPT1}}$ = Low transformer, LBO = Low		14.5		ns

TRANSMITTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTNL	Transmit negative line pulse width	Measured at $\overline{\text{OPT1}}$ = Low transformer, LBO = Low		14.5		ns
	Transmit line pulse waveshape	See Note				

Note: Characteristics are in accordance with CCITT recommendation G.703.

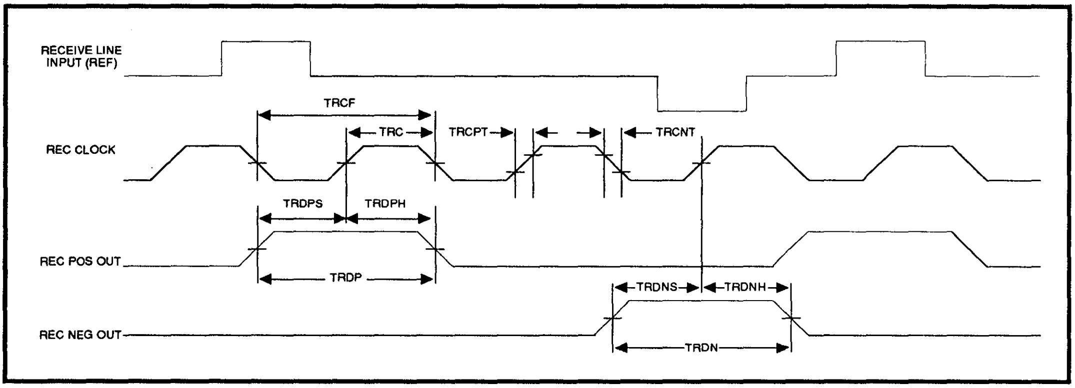


FIGURE 2: Receive Waveforms

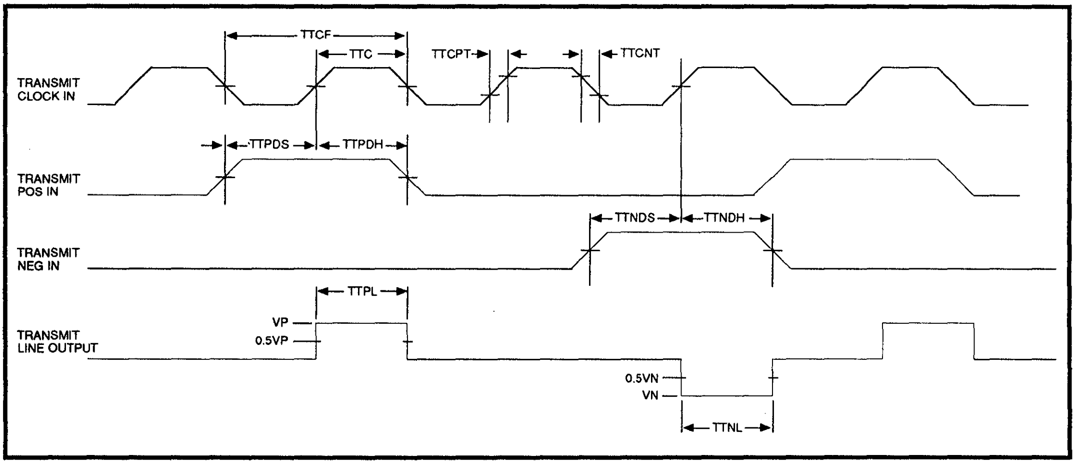
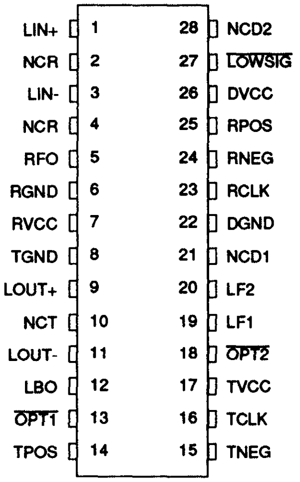


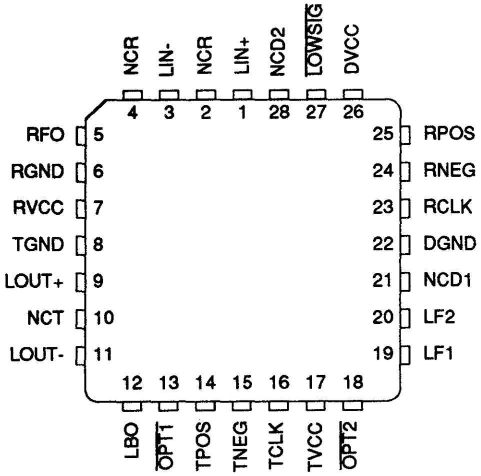
FIGURE 3: Transmit Waveforms

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78P2362, 34.368 Mbit/s Line Interface – 28-pin		
Standard Width Plastic DIP (600 mil)	78P2362-IP	78P2362-IP
Surface Mount 28-pin PLCC	78P2362-IH	78P2362-IH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Notes:

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SSI 78P300

T1/E1 Integrated Short Haul Transceiver with Receive Jitter Attenuation

November 1991

DESCRIPTION

The SSI 78P300 is a fully integrated transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1/CEPT) applications. Transmit pulse shapes (DSX-1 or E1/CEPT) are selectable for various line lengths and cable types.

The SSI 78P300 provides receive jitter attenuation starting at 6 Hz, and is microprocessor controllable through a serial interface.

The SSI 78P300 offers a variety of diagnostic features including transmit and receive monitoring. Clock inputs may be derived from an on-chip crystal oscillator or digital inputs. The SSI 78P300 uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

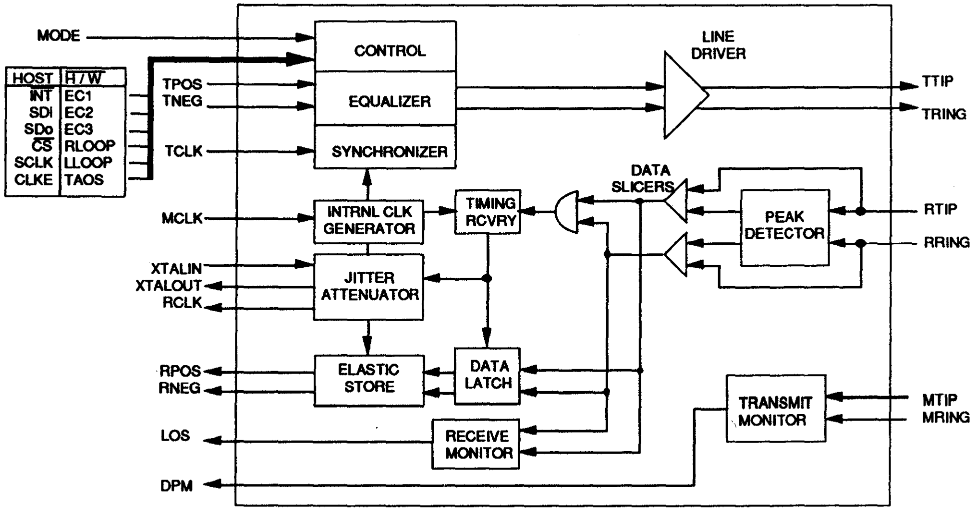
APPLICATIONS

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

FEATURES

- **Compatible with most popular PCM framers including the 2180A and 2181**
- **Line driver, data recovery and clock recovery functions**
- **Pin and functionally compatible with Crystal CS61574**
- **Minimum receive signal of 500 mV**
- **Selectable slicer levels (CEPT/DSX-1) improve SNR**
- **Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft**
- **Local and remote loopback functions**
- **Transmit Driver Performance Monitor (DPM) output**
- **Receive monitor with Loss of Signal (LOS) output**
- **Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz**
- **Microprocessor controllable**
- **Receive jitter attenuation starting at 6 Hz**
- **Available in 28 pin DIP or PLCC**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 78P300 is a fully integrated PCM transceiver for both 1.544 MHz (DSX-1) and 2.048 MHz (CEPT) applications. This transceiver allows transmission of digital data over existing twisted-pair installations.

The SSI 78P300 transceiver interfaces with two twisted-pair lines (one twisted-pair for transmit, one twisted-pair for receive) through standard pulse transformers and appropriate resistors.

TRANSMITTER

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 1 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The SSI 78P300 also matches FCC and ECSA specifications for CSU applications. 2.048 MHz pulses can drive coaxial or shielded twisted-pair lines using appropriate resistors in line with the output transformer.

DRIVER PERFORMANCE MONITOR

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with the TTIP and TRING at the output transformer. The DPM output level goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

LINE CODE

The SSI 78P300 transmits data as a 50% AMI line code as shown in Figure 2. Power consumption is reduced by activating the AMI line driver only to transmit a mark. The output driver is disabled during transmission of a space.

RECEIVER

The SSI 78P300 receives AMI signals from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 3 and Figure 3 for SSI 78P300 receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio.

For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For CEPT applications (EC inputs = 000) the threshold is set to 50 %.

The receiver is capable of accurately recovering signals with up to -13.6 dB of cable attenuation (from 2.4 V), corresponding to a received signal level of approximately 500 mV (1500 feet of ABAM cable.) Regardless of received signal level, the peak detectors are held above a minimum level of .3 V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and the RCLK output is replaced with the MCLK. If MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.

The LOS pin will reset as soon as a one (mark) is detected.Recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

JITTER ATTENUATION

Jitter attenuation of the SSI 78P300 clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 4 for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

OPERATING MODES

The SSI 78P300 transceiver can be controlled through hard-wired pins (Hardware mode). This transceiver can also be commanded to operate in one of several diagnostic modes.

The SSI 78P300 can be controlled by a microprocessor through a serial interface (Host mode). The mode of operation is set by the MODE pin logic level.

HOST MODE OPERATION

To allow a host microprocessor to access and control the SSI 78P300 through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 4 shows the serial interface data structure and timing.

The Host mode provides a latched Interrupt output ($\overline{\text{INT}}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	OUTPUT	CLOCK	VALID EDGE
LOW	RPOS RNEG SDO	RCLK RCLK SCLK	RISING RISING FALLING
HIGH	RPOS RNEG SDO	RCLK RCLK SCLK	FALLING FALLING RISING

The SSI 78P300 serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The SSI 78P300 contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to make a transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 5 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in Table 6, and Figures 5 and 6.

HARDWARE MODE OPERATION

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{\text{INT}}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

RESET OPERATION

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference in the SSI 78P300. If the SSI 78P300 crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and centers the oscillator, then begins calibration.

DIAGNOSTIC MODE OPERATION

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote loopback.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of 1's if the TAOS command is active) will be transmitted normally. When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

POWER REQUIREMENTS

The SSI 78P300 is a low-power CMOS device. It operates from a single +5V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ±.3V of each other, and decoupled to their respective grounds separately, as shown in Figure 7. Isolation between the transmit and receive circuits is provided internally.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
MCLK	I	Master Clock: A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK not applied, this pin should be grounded.
TCLK	I	Transmit Clock: Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS	I	Transmit Positive Data: Input for positive pulse to be transmitted on the twisted-pair or coaxial cable.
TNEG	I	Transmit Negative Data: Input for negative pulse to be transmitted on the twisted-pair or coaxial cable.
MODE	I	Mode Select: Setting MODE to logic 1 puts the SSI 78P300 in the Host mode. In the Host mode, the serial interface is used to control the SSI 78P300 and determined its status. Setting MODE to logic 0 puts the SSI 78P300 in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
RNEG/RPOS	O	Receive Negative Data/Receive Positive Data: Received data outputs. A signal on RNEG corresponds receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host Mode, CLKE determines the clock edge (RCLK) at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge or RCLK.
RCLK	O	Recovered Clock: This is the clock recovered from the signal received at RTIP and RRING.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
XTALIN/ XTALOUT	I/O	Crystal Input/Crystal Output: An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for CEPT applications with an 18.7 pF load) is required to enable the jitter attenuation function of the SSI 78P300. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
DPM	O	Driver Performance Monitor: DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
LOS	O	Loss Of Signal: LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is detected.
TTIP/TRING	O	Transmit Tip/Transmit Ring: Differential Driver Outputs. These outputs are designed to drive a 25 Ω load. The transmitter will drive 100 Ω shielded twisted-pair cable through a 2:1 step-up transformer without additional components. To drive 75 Ω coaxial cable, two 2.2 Ω resistors are required in series with the transformer.
TGND	-	Transmit Ground: Ground return for the transmit drivers power supply TV+.
TV+	I	Transmit Power Supply: +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
MTIP/MRING	I	Monitor Tip/Monitor Ring: These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another SSI 78P300. To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mod-level voltage. The monitor clock can range from 100 kHz to the TCLK frequency.
RTIP/RRING	I	Receive Tip/Receive Ring: The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RV+	I	Receive Power Supply: +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	-	Receive Ground: Ground return for power supply RV+.
$\overline{\text{INT}}$	O	Interrupt (Host Mode): This SSI 78P300 Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{\text{INT}}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{\text{INT}}$ is reset by clearing the respective register bit (LOS and/or DPM.)
EC1	I	Equalizer Control 1 (H/W Mode): The signal applied at this pin in the SSI 78P300 Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
SDI	I	Serial Data In (Host Mode): The serial data input stream is applied to this pin when the SSI 78P300 operates in the Host mode. SDI is sampled on the rising edge of SCLK.
EC2	I	Equalizer Control 2 (H/W Mode): The signal applied at this pin in the SSI 78P300 Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
SDO	O	Serial Data Out (Host Mode): The serial data from the on-chip register is output on this pin in the SSI 78P300 Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
EC3	I	Equalizer Control 3 (H/W Mode): The signal applied at this pin in the SSI 78P300 Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
$\overline{CS}$	I	Chip Select (Host Mode): This input is used to access the serial interface in the SSI 78P300 Host mode. For each read or write operation, $\overline{CS}$ must remain low for duration of operation.
RLOOP	I	Remote Loopback (H/W Mode): This input controls loopback functions in the SSI 78P300 Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset.
SCLK	I	Serial Clock (Host Mode): This clock is used in the SSI 78P300 Host mode to write data to or read data from the serial interface registers.
LLOOP	I	Local Loopback (H/W Mode): This input controls loopback functions in the SSI 78P300 Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
CLKE	I	Clock Edge (Host Mode): Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS	I	Transmit All Ones (H/W Mode): When set to a logic 1, TAOS causes the SSI 78P300 (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNITS
DC Supply (referenced to GND), RV+, TV+	0 to 6.0	V
Input Voltage, Any Pin, V_{IN} (see note 1)	RGND -.03 to RV+ +.03	V
Input Current, Any Pin, I_{in} (see note 2)	-10 to 10	mA
Ambient Operating Temperature, T_A	-40 to 85	°C
Storage Temperature, T_{STG}	-65 to 150	°C

[1] Excluding RTIP and RRING which must stay within -6V to RV+ + 0.3V.

[2] Transient currents of up to 100 mA will not cuase SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DC supply, RV+, TV+ (see note 1)		4.75	5.0	5.25	V
Ambient Operating Temp., T_A		-40	25	85	°C
Total Power Dissipation, P_D (see note 2)	100% Ones Density & Maximum Line Length @ 5.25V	-	620	-	mW

[1] TV+ must not exceed RV+ by more than ±0.3V.

[2] Power dissipation while driving 25Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50pF capacitive load.

DIGITAL CHARACTERISTICS

T_A = -40° to 85°C, V+ = 5.0 V± 5%, GND = 0V

V_{IH} High Level Input Voltage (pins 1-5, 10, 23-28) (see note 1, 2)		2.0	-	-	V
V_{IL} Low Level Input Voltage (pins 1-5, 10, 23-28) (see note 1, 2)		-	-	0.8	V
V_{OH} High Level Output Voltage (pins 6-8, 11, 12, 23, 25) (see note 1, 2)	I_{OUT} = -400 µA	2.4	-	-	V
V_{OL} Low Level Output Voltage (pins 6-8, 11, 12, 23, 25) (see note 1, 2)	I_{OUT} = 1.6 mA	-	-	0.4	V
I_{LL} Input Leakage Current		0		±10	µA
I_{3L} Three -State Leakage Current (pin 25) (see note 1)		0	-	±10	µA

[1] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.

[2] Output drivers will output CMOS logic levels into CMOS loads.

ELECTRICAL SPECIFICATIONS (continued)

ANALOG SPECIFICATIONS

T_A = -40° to 85°C, V+ = 5.0 V± 5%, GND = 0V

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
AMI Output Pulse Amplitudes	DSX-1	Measured at the DSX	2.4	3.0	3.6	V
	CEPT	Measured at Line Side	2.7	3.0	3.3	V
Load Presented to Transmitter Output			-	25	-	Ω
Jitted Added by the Transmitter (see note 1)	10 Hz - 8 kHz		-	-	0.01	UI
	8 kHz - 40 kHz		-	-	0.025	UI
	10 Hz - 40 kHz		-	-	0.025	UI
	Broad Band		-	-	0.05	UI
Sensitivity Below DSX	(0dB = 2.4V)		13.6	-	-	dB
			500	-	-	mV
Loss of Signal Threshold			-	0.3	-	V
Data Decision Threshold	DSX-1		-	65	-	%peak
	CEPT		-	50	-	%peak
Allowable Consecutive Zeros Before LOS			160	175	190	-
Input Jitter Tolerance 10 kHz - 100 kHz			0.4	-	-	UI
Jitter Attenuation Curve Corner Frequency (see note 2)			-	6	-	Hz

[1] Input signal to TCLK is jitter-free.

[2] Circuit attenuates jitter at 20 dB/decade above the corner frequency.

TABLE 1: Equalizer Control Inputs

EC3	EC2	EC1	LINE LENGTH	CABLE LOSS	APPLICATION	FREQUENCY
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		CEPT	2.048 MHz
0	1	0	FCC Part 68, Option A		CSU	1.544 MHz
0	1	1	ECSA T1C1.2			

TABLE 2: 78P300 Master Clock and Transmit Timing Characteristics

PARAMETER			CONDITIONS	MIN	NOM	MAX	UNIT
Master clock frequency	MCLK	DSX-1		-	1.544	-	MHz
	MCLK	CEPT		-	2.048	-	MHz
Master clock tolerance	MCLKt			-	±100	-	ppm
Master clock duty cycle	MCLKd			40	-	60	%
Crystal frequency	fc	DSX-1		-	6.176	-	MHz
	fc	CEPT		-	8.192	-	MHz
Transmit clock frequency	TCLK	DSX-1		-	1.544	-	MHz
	TCLK	CEPT		-	2.048	-	MHz
Transmit clock tolerance	TCLKt			-	-	±50	ppm
Transmit clock duty cycle	TCLKd			10	-	90	%
TPOS/TNEG to TCLK setup time	t_{SUT}			25	-	-	ns
TCLK to TPOS/TNEG Hold time	t_{HT}			25	-	-	ns

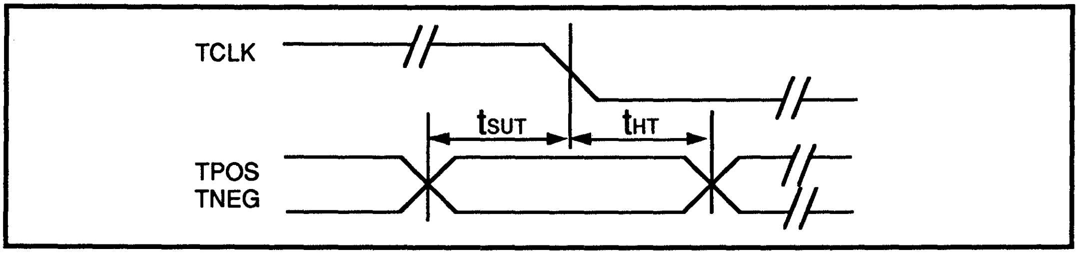


FIGURE 1: 78P300 Transmit Clock Timing Diagram

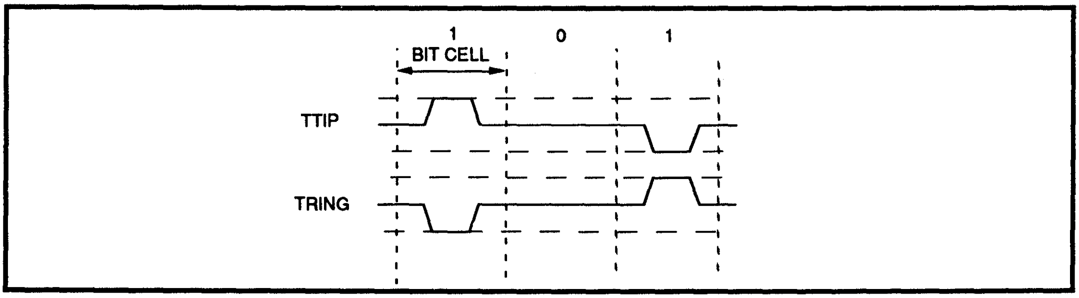


FIGURE 2: 50% AMI Coding Diagram

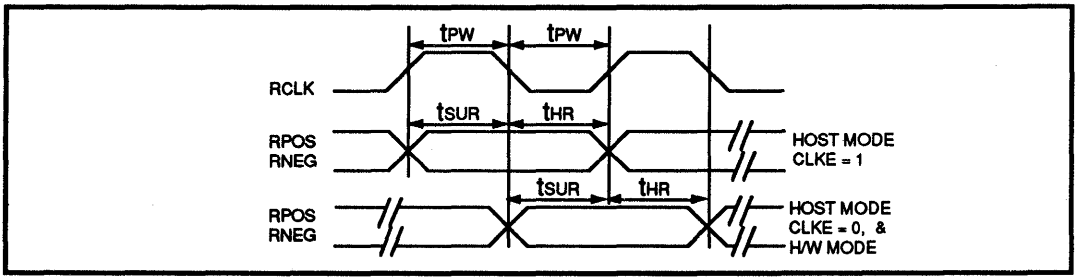


FIGURE 3: 78P300 Receive Clock Timing Diagram

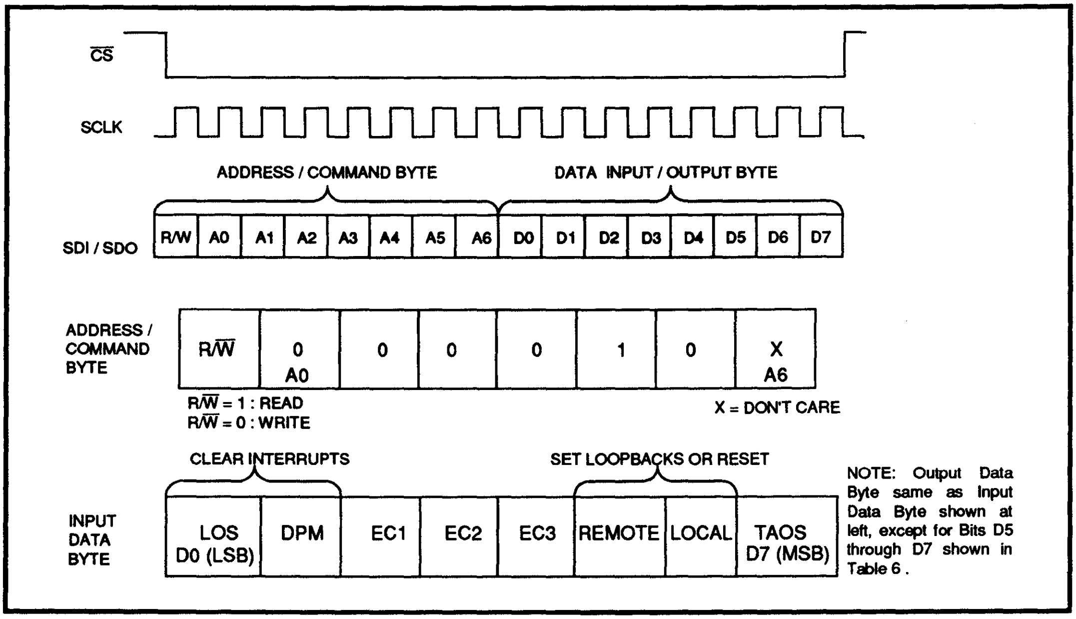
TABLE 3: 78P300 Receive Timing Characteristics

PARAMETER			CONDITIONS	MIN	NOM[1]	MAX	UNIT
Receive clock duty cycle RCLKd				40	-	60	%
Receive clock pulse width	t_{PW}	DSX-1		-	324	-	ns
	t_{PW}	CEPT		-	244	-	ns
RPOS/RNEG to RCLK	t_{SUR}	DSX-1		-	274	-	ns
rising setup time	t_{SUR}	CEPT		-	194	-	ns
RCLK rising to RPOS/	t_{HR}	DSX-1		-	274	-	ns
RNEG hold time	t_{HR}	CEPT		-	194	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

TABLE 4: SSI 78P300 Crystal Specifications (External)

PARAMETER	T1	CEPT
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25°C	±20 ppm @ 25°C
	±25 ppm from -40°C to + 85°C (Ref 25°C reading)	± 25 ppm from -40°C to + 85°C (Ref 25°C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm
	CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40 Ω Maximum	30 Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF Maximum C_M = 17 pF typical	HC49 (R3W), C_O = 7 pF Maximum C_M = 17 pF typical



NOTE: Output Data Byte same as Input Data Byte shown at left, except for Bits D5 through D7 shown in Table 6 .

FIGURE 4: SSI 78P300 Serial Interface Data Structure

TABLE 5: SSI 78P300 Serial Data Output Bits (See Figure 4)

BIT D5	BIT D6	BIT D7	STATUS
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

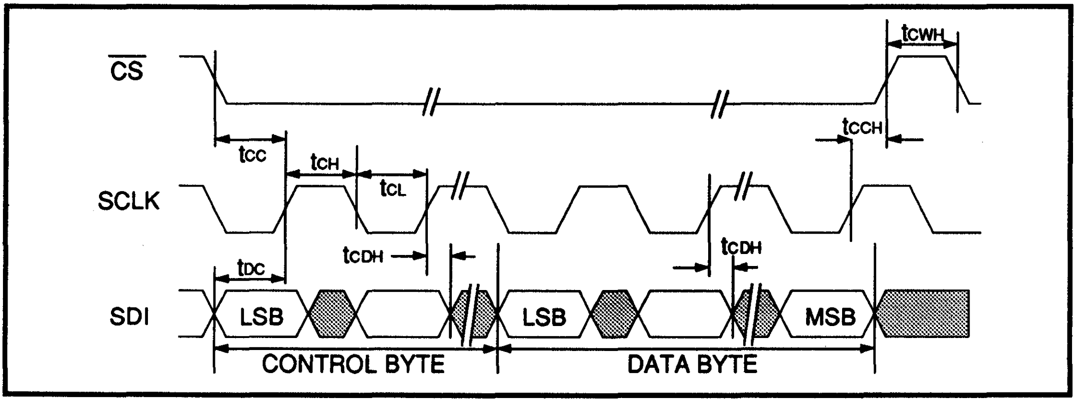


FIGURE 5: SSI 78P300 Serial Data Input Timing Diagram

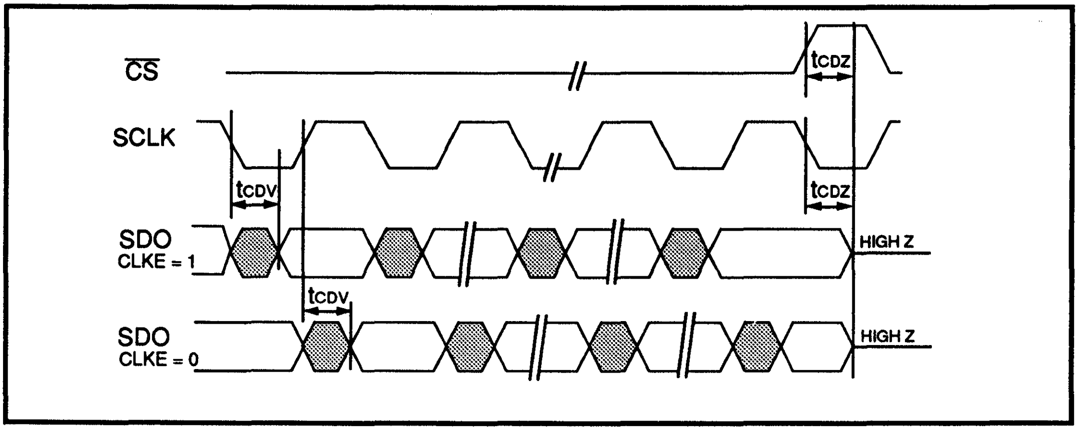


FIGURE 6: SSI 78P300 Serial Data Output Timing Diagram

TABLE 6: SSI 78P300 Serial I/O Timing Characteristics (See Figures 5 and 6)

PARAMETER		CONDITIONS	MIN	NOM[1]	MAX	UNIT
Rise/Fall time - any digital output	t_{RF}	Load 1.6 mA, 50 pF	-	-	100	ns
SDI to SCLK setup time	t_{DC}		50	-	-	ns
SCLK to SDI hold time	t_{CDH}		50	-	-	ns
SCLK low time	t_{CL}		240	-	-	ns
SCLK high time	t_{CH}		240	-	-	ns
SCLK rise and fall time	t_R, t_F		-	-	50	ns
CS to SCLK setup time	t_{CC}		50	-	-	ns
SCLK to CS hold time	t_{CCH}		50	-	-	ns
CS inactive time	t_{CWH}		250	-	-	ns
SCLK to SDO valid	t_{CDV}		-	-	200	ns
SCLK falling edge or CS rising edge to SDO high Z	t_{CDZ}		-	100	-	ns

[1] Typical figures are at 25°C and are for desing aid only; not guaranteed and not subject to production testing.

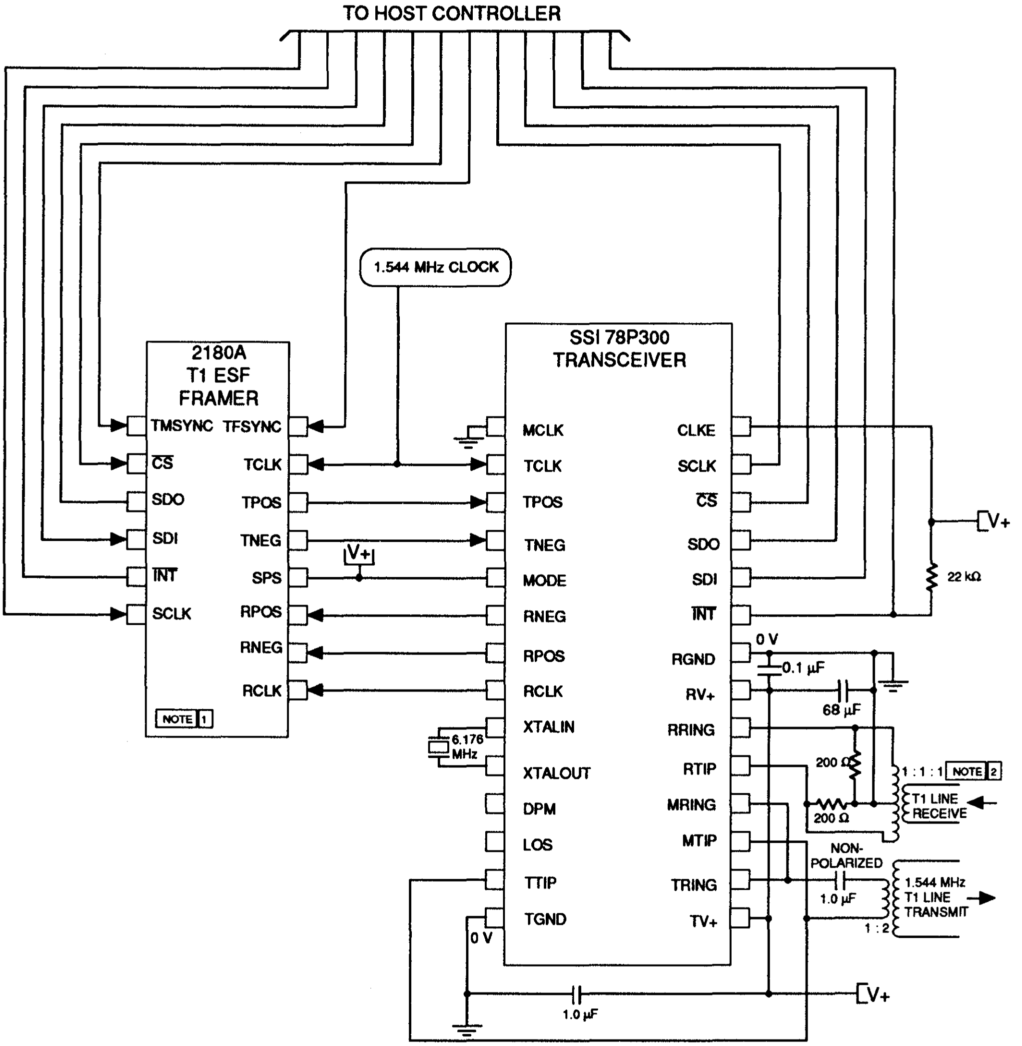
APPLICATION INFORMATION

SSI 78P300 1.544 MHz T1 INTERFACE APPLICATIONS

Figure 7 is a typical 1.544 MHz T1 application. The SSI 78P300 is shown in the Host mode with the 2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

SSI 78P300 2.048 MHz E1/CEPT INTERFACE APPLICATIONS

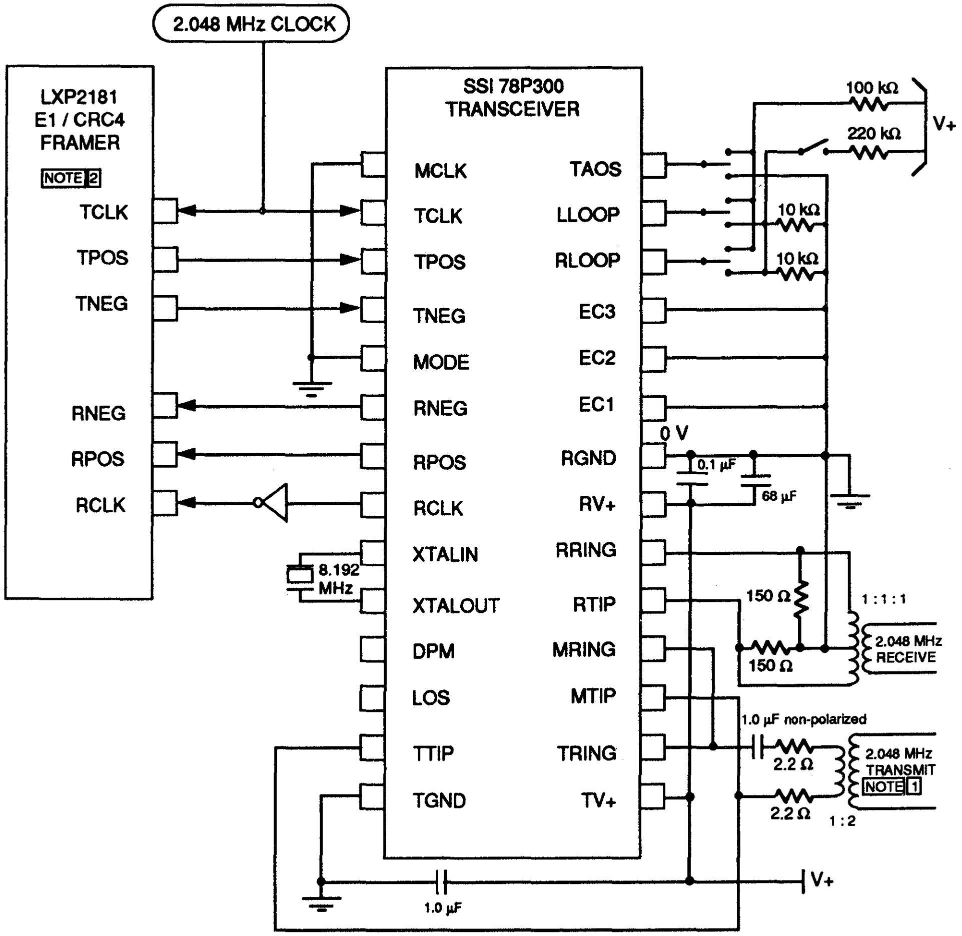
Figure 8 is a typical 2.048 MHz E1/CEPT application. The SSI 78P300 is shown in Hardware mode with the 2181 E1/CRC4 Framer. Resistors are installed in line with the transmit transformer for loading a 75 Ω coaxial cable. The in-line resistors are not required for transmission on 100 Ω shielded twisted-pair lines. As in the T1 application Figure 7, this configuration is illustrated with a crystal in place to enable the SSI 78P300 Jitter Attenuation Loop, and a single power supply bus. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function.



NOTE 1 THE SSI 78P300 IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP 2180A, LXP2181, DS2180A, MT8976, AND R8070.

NOTE 2 WHEN THE SSI 78P300 IS CONNECTED TO THE CROSS-CONNECT FRAME THROUGH A LOW LEVEL MONITOR JACK, RECEIVE TRANSFORMER SHOULD BE 1 : 2 : 2 TO BOOST THE INPUT SIGNAL.

FIGURE 7: Typical SSI 78P300 1.544 MHz T1 Application (Host Mode)



NOTE 1 2.2 Ω RESISTORS REQUIRED ONLY FOR 75 Ω COAXIAL CABLE. NOT REQUIRED FOR TRANSMISSION ONTO 100 Ω CABLE.

NOTE 2 THE SSI 78P300 IS COMPATIBLE WITH A WIDE VARIETY OF FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2181, DS2181, MT8979, AND R8070.

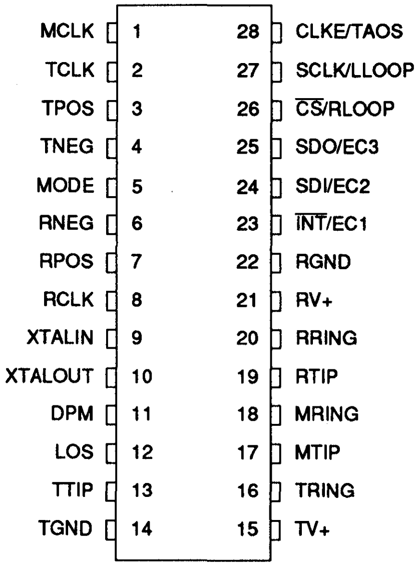
FIGURE 8: Typical SSI 78P300 2.048 MHz E1 Application (Hardware Mode)

SSI 78P300

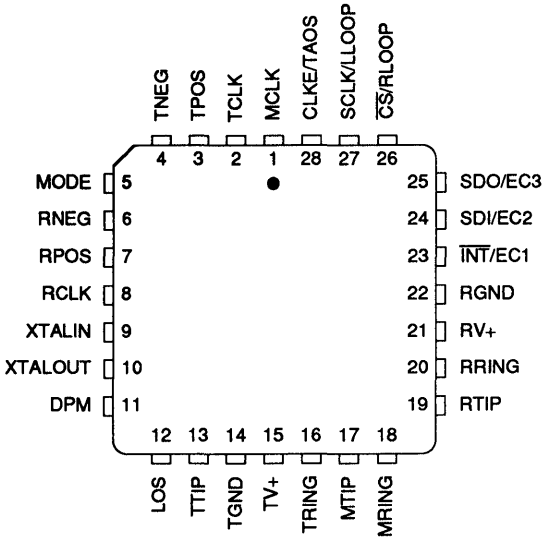
T1/E1 Integrated Short Haul Transceiver with Receive Jitter Attenuation

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P300 28-Pin PLCC	78P300-IH	78P300-IH
SSI 78P300 28-Pin DIP	78P300-IP	78P300-IP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

A TDK Group Company

SSI 78P304A

Low-Power T1/E1 Integrated Short Haul Transceiver with Receive Jitter Attenuation

October 1991

DESCRIPTION

The SSI 78P304A is a fully integrated low-power transceiver for both North American 1.544 MHz (T1), and European 2.048 MHz (E1/CEPT) applications. It features a constant low output impedance transmitter allowing for high transmitter return loss in E1 applications. Transmit pulse shapes (DSX-1 or E1/CEPT) are selectable for various line lengths and cable types.

The SSI 78P304A provides receive jitter attenuation starting at 3 Hz, and is microprocessor controllable through a serial interface.

The SSI 78P304A offers a variety of diagnostic features including transmit and receive monitoring. The device incorporates an on-chip crystal oscillator, and also accepts digital clock inputs. It uses an advanced double-poly, double-metal CMOS process and requires only a single 5-volt power supply.

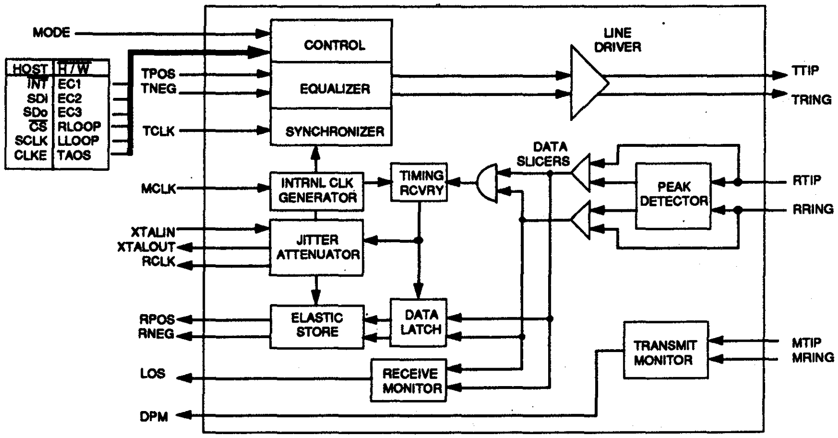
APPLICATIONS

- PCM / Voice Channel Banks
- Data Channel Bank / Concentrator
- T1 / E1 multiplexer
- Digital Access and Cross-connect Systems (DACS)
- Computer to PBX interface (CPI & DMI)
- High speed data transmission lines
- Interfacing Customer Premises Equipment to a CSU
- Digital Loop Carrier (DLC) terminals

FEATURES

- **Low power consumption (400 mW maximum) 40% less than the SSI 78P300**
- **Constant low output impedance transmitter regardless of data pattern**
- **High transmit and receive return loss**
- **Meets or exceeds all industry specifications including CCITT G.703, ANSI T1.403 and ATT Pub 62411**
- **Compatible with most popular PCM framers including the 2180A (T1) and 2181/2181A (E1)**
- **Line driver, data recovery and clock recovery functions**
- **Minimum receive signal of 500 mV**
- **Selectable slicer levels (CEPT/DSX-1) improve SNR**
- **Programmable transmit equalizer shapes pulses to meet DSX-1 pulse template from 0 to 655 ft**
- **Local and remote loopback functions**
  Transmit / Receive performance monitors with DPM and LOS outputs
- **Receiver jitter tolerance 0.4 UI from 40 kHz to 100 kHz**
- **Receive jitter attenuation starting at 3 Hz**
- **Microprocessor controllable**
- **Available in 28 pin DIP or PLCC**

FIGURE 1: BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The SSI 78P304A is a fully integrated PCM transceiver for both 1.544 MHz (DSX-1) and 2.048 MHz (E1) applications. It allows transmission of digital data over existing twisted-pair installations. The SSI 78P304A transceiver interfaces with two twisted-pair lines, one twisted-pair for transmit, one twisted-pair for receive.

TRANSMITTER

Data received for transmission onto the line is clocked serially into the device at TPOS and TNEG. Input synchronization is supplied by the transmit clock (TCLK). The transmitted pulse shape is determined by Equalizer Control signals EC1 through EC3 as shown in Table 1. Refer to Table 2 and Figure 2 for master and transmit clock timing characteristics. Shaped pulses are applied to the AMI line driver for transmission onto the line at TTIP and TRING. Equalizer Control signals may be hardwired in the Hardware mode, or input as part of the serial data stream (SDI) in the Host mode.

Pulses can be shaped for either 1.544 or 2.048 MHz applications. 1.544 MHz pulses for DSX-1 applications can be programmed to match line lengths from 0 to 655 feet of ABAM cable. The SSI 78P304A also matches FCC and ECSA specifications for CSU applications. A 1:1.15 transmit transformer is used for all 1.544 MHz systems.

2.048 MHz pulses can drive coaxial or shielded twisted-pair lines. For E1 systems, a 1:2 transmit transformer and series resistors are recommended. This design meets or exceeds all CCITT and European PTT specifications for transmit and receive return loss. A 1:1 or 1:1.26 transformer may be used without series resistors.

DRIVER PERFORMANCE MONITOR

The transceiver incorporates a Driver Performance Monitor (DPM) in parallel with TTIP and TRING at the output transformer. The DPM output goes high upon detection of 63 consecutive zeros. It is reset when a one is detected on the transmit line, or when a reset command is received.

LINE CODE

The SSI 78P304A transmits data as a 50% AMI line code as shown in Figure 3. The output driver maintains a constant low output impedance regardless of whether it is driving marks or spaces.

RECEIVER

The SSI 78P304A receives the signal input from one twisted-pair line on each side of a center-grounded transformer. Positive pulses are received at RTIP and negative pulses are received at RRING. Recovered data is output at RPOS and RNEG, and the recovered clock is output at RCLK. Refer to Table 3 and Figure 4 for SSI 78P304A receiver timing.

The signal received at RPOS and RNEG is processed through the peak detector and data slicers. The peak detector samples the inputs and determines the maximum value of the received signal. A percentage of the peak value is provided to the data slicers as a threshold level to ensure optimum signal-to-noise ratio. For DSX-1 applications (determined by Equalizer Control inputs EC1 - EC3 ≠ 000) the threshold is set to 70% of the peak value. This threshold is maintained above 65% for up to 15 successive zeros over the range of specified operating conditions. For E1 applications (EC inputs = 000 or 001) the threshold is 50%.

The receiver is capable of accurately recovering signals with up to -13.6 dB of attenuation (from 2.4V), corresponding to a received signal level of approximately 500 mV. Maximum line length is 1500 feet of ABAM cable (approximately 6 dB of attenuation). Regardless of received signal level, the peak detectors are held above a minimum level of .3V to provide immunity from impulsive noise.

After processing through the data slicers, the received signal is routed to the data and clock recovery sections, and to the receive monitor. The receive monitor generates a Loss of Signal (LOS) output upon receipt of 175 consecutive zeros (spaces). The receiver monitor loads a digital counter at the RCLK frequency. The count is incremented each time a zero is received, and reset to zero each time a one (mark) is received. Upon receipt of 175 consecutive zeros the LOS pin goes high, and a smooth transition replaces the RCLK output with the MCLK. (If MCLK is not supplied the RCLK output will be replaced with the centered crystal clock.) The LOS pin is reset immediately upon receipt of a one.

Recovered clock signals are supplied to the jitter attenuator and the data latch. The recovered data is passed to the elastic store where it is buffered and synchronized with the dejittered recovered clock (RCLK).

JITTER ATTENUATION

Jitter attenuation of the SSI 78P304A clock and data outputs is provided by a Jitter Attenuation Loop (JAL) and an Elastic Store (ES). An external crystal oscillating at 4 times the bit rate provides clock stabilization. Refer to Table 4 for crystal specifications. The ES is a 32 x 2-bit register. Recovered data is clocked into the ES with the recovered clock signal, and clocked out of the ES with the dejittered clock from the JAL. When the bit count in the ES is within two bits of overflowing or underflowing, the ES adjusts the output clock by 1/8 of a bit period. The ES produces an average delay of 16 bits in the receive path.

OPERATING MODES

The SSI 78P304A transceiver can be controlled through hard-wired pins (Hardware mode) or by a microprocessor through a serial interface (Host mode). The mode of operation is set by the MODE pin logic level. The SSI 78P304A can also be commanded to operate in one of several diagnostic modes.

HOST MODE OPERATION

To allow a host microprocessor to access and control the SSI 78P304A through the serial interface, MODE is set to 1. The serial interface (SDI/SDO) uses a 16-bit word consisting of an 8-bit Command/Address byte and an 8-bit Data byte. Figure 5 shows the serial interface data structure and timing.

The Host mode provides a latched Interrupt output ($\overline{\text{INT}}$) which is triggered by a change in the Loss of Signal (LOS) and/or Driver Performance Monitor (DPM) bits. The Interrupt is cleared when the interrupt condition no longer exists, and the host processor enables the respective bit in the serial input data byte. Host mode also allows control of the serial data and receive data output timing. The Clock Edge (CLKE) signal determines when these outputs are valid, relative to the Serial Clock (SCLK) or RCLK as follows:

CLKE	Output	Clock	Valid Edge
LOW	RPOS	RCLK	Rising
	RNEG	RCLK	Rising
	SDO	SCLK	Falling
HIGH	RPOS	RCLK	Falling
	RNEG	RCLK	Falling
	SDO	SCLK	Rising

The SSI 78P304A serial port is addressed by setting bit A4 in the Address/Command byte, corresponding to address 16. The SSI 78P304A contains only a single output data register so no complex chip addressing scheme is required. The register is accessed by causing the Chip Select (CS) input to make a transition from high to low. Bit 1 of the serial Address/Command byte provides Read/Write control when the chip is accessed. A logic 1 indicates a read operation, and a logic 0 indicates a write operation. Table 6 lists serial data output bit combinations for each status. Serial data I/O timing characteristics are shown in Table 6, and Figures 6 and 7.

HARDWARE MODE OPERATION

In Hardware mode the transceiver is accessed and controlled through individual pins. With the exception of the $\overline{\text{INT}}$ and CLKE functions, Hardware mode provides all the functions provided in the Host mode. In the Hardware mode RPOS and RNEG outputs are valid on the rising edge of RCLK. To operate in Hardware mode, MODE must be set to 0. Equalizer Control signals (EC1 through EC3) are input on the Interrupt, Serial Data In and Serial Data Out pins. Diagnostic control for Remote Loopback (RLOOP), Local Loopback (LLOOP), and Transmit All Ones (TAOS) modes is provided through the individual pins used to control serial interface timing in the Host mode.

RESET OPERATION

Upon power up, the transceiver is held static until the power supply reaches approximately 3V. Upon crossing this threshold, the device begins a 32 ms reset cycle to calibrate the transmit and receive delay lines and lock the Phase Lock Loop to the receive line. A reference clock is required to calibrate the delay lines. The transmitter reference is provided by TCLK. The crystal oscillator provides the receiver reference. If the 78P304A crystal oscillator is grounded, MCLK is used as the receiver reference clock.

The transceiver can also be reset from the Host or Hardware mode. In Host mode, reset is commanded by simultaneously writing RLOOP and LLOOP to the register. In Hardware mode, reset is commanded by holding RLOOP and LLOOP high simultaneously for 200 ns. Reset is initiated on the falling edge of the reset request. In either mode, reset clears and sets all registers to 0 and centers the oscillator, then calibration begins.

DIAGNOSTIC MODE OPERATION

In Transmit All Ones (TAOS) mode the TPOS and TNEG inputs to the transceiver are ignored. The transceiver transmits a continuous stream of 1's when the TAOS mode is activated. TAOS can be commanded simultaneously with Local Loopback, but is inhibited during Remote Loopback.

In Remote Loopback (RLOOP) mode, the transmit data and clock inputs (TPOS, TNEG and TCLK) are ignored. The RPOS and RNEG outputs are looped back through the transmit circuits and output on TTIP and TRING at the RCLK frequency. Receiver circuits are unaffected by the RLOOP command and continue to output the RPOS, RNEG and RCLK signals received from the twisted-pair line.

In Local Loopback (LLOOP) mode, the receiver circuits are inhibited. The transmit data and clock inputs (TPOS, TNEG and TCLK) are looped back onto the receive data and clock outputs (RPOS, RNEG and RCLK.) The transmitter circuits are unaffected by the LLOOP command. The TPOS and TNEG inputs (or a stream of 1's if the TAOS command is active) will be transmitted normally. When used in this mode with a crystal, the transceiver can be used as a stand-alone jitter attenuator.

POWER REQUIREMENTS

The SSI 78P304A is a low-power CMOS device. It operates from a single +5 V power supply which can be connected externally to both the transmitter and receiver. However, the two inputs must be within ± .3V of each other, and decoupled to their respective grounds separately, as shown in Figure 8. Isolation between the transmit and receive circuits is provided internally.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
MCLK	I	Master Clock: A 1.544 or 2.048 MHz clock input used to generate internal clocks. Upon Loss of Signal (LOS), RCLK is derived from MCLK. If MCLK is not applied, this pin should be grounded.
TCLK	I	Transmit Clock: Transmit clock input. TPOS and TNEG are sampled on the falling edge of TCLK.
TPOS	I	Transmit Positive Data: Input for positive pulse to be transmitted on the twisted-pair or coaxial cable.
TNEG	I	Transmit Negative Data: Input for negative pulse to be transmitted on the twisted-pair or coaxial cable.
MODE	I	Mode Select: Setting MODE to logic 1 puts the SSI 78P304A in the Host mode. In the Host mode, the serial interface is used to control the SSI 78Q904A and determine its status. Setting MODE to logic 0 puts the SSI 78P304A in the Hardware (H/W) mode. In the Hardware mode the serial interface is disabled and hard-wired pins are used to control configuration and report status.
RNEG / RPOS	O	Receive Negative/Positive Data: Received data outputs. A signal on RNEG corresponds to receipt of a negative pulse on RTIP and RRING. A signal on RPOS corresponds to receipt of a positive pulse on RTIP and RRING. RNEG and RPOS outputs are Non-Return-to-Zero (NRZ). In the Host mode, CLKE determines the clock edge at which these outputs are stable and valid. In the Hardware mode both outputs are stable and valid on the rising edge of RCLK.
RCLK	O	Recovered Clock: This is the clock recovered from the signal received at RTIP and RRING.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
XTALIN / XTALOUT	I	Crystal Input / Crystal Output: An external crystal operating at four times the bit rate (6.176 MHz for DSX-1, 8.192 MHz for E1 applications with an 18.7 pF load) is required to enable the jitter attenuation function of the SSI 78P304A. These pins may also be used to disable the jitter attenuator by connecting the XTALIN pin to the positive supply through a resistor, and tying the XTALOUT pin to ground.
DPM	O	Driver Performance Monitor: DPM goes to a logic 1 when the transmit monitor loop (MTIP and MRING) does not detect a signal for 63 ±2 clock periods. DPM remains at logic 1 until a signal is detected.
LOS	O	Loss of Signal: LOS goes to a logic 1 when 175 consecutive spaces have been detected. LOS returns to a logic 0 when a mark is received.
TTIP / TTRING	O	Transmit Tip / Transmit Ring: Differential Driver Outputs. These low impedance outputs achieve maximum power savings through a 1:1.15 transformer (T1), or a 1:1 or 1:1.26 transformer (E1) without additional components. To provide higher return loss for E1 systems, resistors may be used in series with a 1:2 transformer (use 15Ω resistors for 120Ω terminations, and 9.3 Ω resistors for 75Ω terminations.)
TGND	-	Transmit Ground: Ground return for the transmit drivers power supply TV+.
TV+	I	Transmit Power Supply: +5 VDC power supply input for the transmit drivers. TV+ must not vary from RV+ by more than ±0.3V.
MTIP / MRING	I	Monitor Tip / Monitor Ring: These pins are used to monitor the tip and ring transmit outputs. The transceiver can be connected to monitor its own output or the output of another 78P304A on the board. To prevent false interrupts in the host mode if the monitor is not used, apply a clock signal to one of the monitor pins and tie the other monitor pin to approximately the clock's mid-level voltage. The monitor clock can range from 100kHz to the TCLK frequency.
RTIP / RRING	O	Receive Tip / Receive Ring: The AMI signal received from the line is applied at these pins. A center-tapped, center-grounded, 2:1 step-up transformer is required on these pins. Data and clock from the signal applied at these pins are recovered and output on the RPOS/RNEG, and RCLK pins.
RV+	I	Received Power Supply: +5 VDC power supply for all circuits except the transmit drivers. (Transmit drivers are supplied by TV+.)
RGND	-	Receive Ground: Ground return for power supply RV+.
$\overline{\text{INT}}$	O	Interrupt (Host Mode): This SSI 78P304A Host mode output goes low to flag the host processor when LOS or DPM go active. $\overline{\text{INT}}$ is an open-drain output and should be tied to power supply RV+ through a resistor. $\overline{\text{INT}}$ is reset by clearing the respective register bit (LOS and/or DPM.)
EC1	I	Equalizer Control 1 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC2 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
SDI	I	Serial Data In (Host Mode): The serial data input stream is applied to this pin when the SSI 78P304A operates in the Host mode. SDI is sampled on the rising edge of SCLK.
EC2	I	Equalizer Control 2 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC1 and EC3 inputs to determine shape and amplitude of AMI output transmit pulses.
SDO	O	Serial Data Out (Host Mode): The serial data from the on-chip register is output on this pin in the SSI 78P304A Host mode. If CLKE is high, SDO is valid on the rising edge of SCLK. If CLKE is low SDO is valid on the falling edge of SCLK. This pin goes to a high-impedance state when the serial port is being written to and when $\overline{CS}$ is high.
EC3	I	Equalizer Control 3 (H/W Mode): The signal applied at this pin in the SSI 78P304A Hardware mode is used in conjunction with EC1 and EC2 inputs to determine shape and amplitude of AMI output transmit pulses.
$\overline{CS}$	I	Chip Select (Host Mode): This input is used to access the serial interface in the SSI 78P304A Host mode. For each read or write operation, $\overline{CS}$ must remain low for the duration of operation.
RLOOP	I	Remote Loopback (H/W Mode): This input controls loopback functions in the SSI 78P304A Hardware mode. Setting RLOOP to a logic 1 enables the Remote Loopback mode. Setting both RLOOP and LLOOP causes a Reset.
SCLK	I	Serial Clock (Host Mode): This clock is used in the SSI 78P304A Host mode to write data to or read data from the serial interface registers.
LLOOP	I	Local Loopback (H/W Mode): This input controls loopback functions in the SSI 78P304A Hardware mode. Setting LLOOP to a logic 1 enables the Local Loopback Mode.
CLKE	I	Clock Edge (Host Mode): Setting CLKE to logic 1 causes RPOS and RNEG to be valid on the falling edge of RCLK, and SDO to be valid on the rising edge of SCLK. When CLKE is a logic 0, RPOS and RNEG are valid on the rising edge of RCLK, and SDO is valid on the falling edge of SCLK.
TAOS	I	Transmit All Ones (H/W Mode): When set to a logic 1, TAOS causes the SSI 78P304A (Hardware mode) to transmit a continuous stream of marks at the TCLK frequency. Activating TAOS causes TPOS and TNEG inputs to be ignored. TAOS is inhibited during Remote Loopback.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device. Normal operation not guaranteed at these extremes.

PARAMETER		RATING	UNIT
DC supply (referenced to GND)	RV+, TV+	-0 to 6.0	V
Input voltage, any pin (see note 1)	V_{IN}	RGND -.03 to RV+ + 0.3	V
Input current, any pin (see note 2)	I_{IN}	-10 to +10	mA
Ambient operating temperature	T_A	-40 to 85	°C
Storage temperature	T_{STG}	-65 to 150	°C

[1] Excluding RTIP and RRING which must stay within -6V to RV+ + 0.3V.

[2] Transient currents of up to 100 mA will not cause SCR latch-up. TTIP, TRING, TV+ and TGND can withstand a continuous current of 100 mA.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	NOM	MAX	UNIT
DC supply (see note 1)		RV+, TV+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
Total power dissipation (see note 2)	P_D	100% ones density & max line length @ 5.25V	-	-	400	mW

[1] TV+ must not exceed RV+ by more than ± .3 V.

[2] Power dissipation while driving 25Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails and digital outputs are driving a 50 pF capacitive load.

DIGITAL CHARACTERISTICS (T_A = -40° to 85 °C, V+ = 5.0V ±5%, GND = 0V)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
High level input voltage (see notes 1 & 2)	V_{IH}		2.0	-	-	V
Low level input voltage (see notes 1 & 2)	V_{IL}		-	-	0.8	V
High level output voltage (see notes 1 & 2)	V_{OH}	I_{OUT} = -400 µA	2.4	-	-	V
Low level output voltage (see notes 1 & 2)	V_{OL}	I_{OUT} = 1.6 mA	-	-	0.4	V
Input leakage current (see note 3)	I_{LL}		0	-	±10	µA
Three-state leakage current (see note 2)	I_{3L}		0	-	±10	µA

[1] Functionality of pins 23 and 25 depends on mode. See Host / Hardware Mode descriptions.

[2] Output drivers will output CMOS logic levels into CMOS loads.

[3] Except MTIP and MRING I_{LL} = ± 50 µA.

ELECTRICAL SPECIFICATIONS (continued)

ANALOG SPECIFICATIONS (T_A = -40 to 85 °C, V+ = 5.0V ±5%, GND = 0V)

<table>
<tr><th colspan="2">PARAMETER</th><th>TEST CONDITIONS</th><th>MIN</th><th colspan="2">NOM</th><th>MAX</th><th>UNIT</th></tr>
<tr><td rowspan="2">AMI Output Pulse Amplitudes</td><td>DSX-1</td><td>measured at the DSX</td><td>2.4</td><td colspan="2">3.0</td><td>3.6</td><td>V</td></tr>
<tr><td>CEPT</td><td>measured at line side</td><td>2.7</td><td colspan="2">3.0</td><td>3.3</td><td>V</td></tr>
<tr><td colspan="2">Load presented to transmitter output</td><td></td><td>-</td><td colspan="2">75</td><td>-</td><td>Ω</td></tr>
<tr><td rowspan="4">Jitter added by the transmitter (see note 1)</td><td>10 Hz - 8 kHz</td><td></td><td>-</td><td colspan="2">-</td><td>0.01</td><td>UI</td></tr>
<tr><td>8 kHz - 40 kHz</td><td></td><td>-</td><td colspan="2">-</td><td>0.025</td><td>UI</td></tr>
<tr><td>10 Hz - 40 kHz</td><td></td><td>-</td><td colspan="2">-</td><td>0.025</td><td>UI</td></tr>
<tr><td>Broad Band</td><td></td><td>-</td><td colspan="2">-</td><td>0.05</td><td>UI</td></tr>
<tr><td colspan="2" rowspan="2">Sensitivity below DSX (0 dB = 2.4V)</td><td rowspan="2"></td><td>13.6</td><td colspan="2">-</td><td>-</td><td>dB</td></tr>
<tr><td>500</td><td colspan="2">-</td><td>-</td><td>mV</td></tr>
<tr><td colspan="2">Loss of Signal threshold</td><td></td><td>-</td><td colspan="2">0.3</td><td>-</td><td>V</td></tr>
<tr><td rowspan="2">Data decision threshold</td><td>DSX-1</td><td></td><td>-</td><td colspan="2">65</td><td>-</td><td>%peak</td></tr>
<tr><td>CEPT</td><td></td><td>-</td><td colspan="2">50</td><td>-</td><td>%peak</td></tr>
<tr><td colspan="2">Allowable consecutive zeros before LOS</td><td></td><td>160</td><td colspan="2">175</td><td>190</td><td>-</td></tr>
<tr><td>Input jitter tolerance</td><td>10 kHz - 100 kHz</td><td></td><td>0.4</td><td colspan="2">-</td><td>-</td><td>UI</td></tr>
<tr><td colspan="2">Jitter attenuation curve corner frequency (see note 2)</td><td></td><td>-</td><td colspan="2">3</td><td>-</td><td>Hz</td></tr>
<tr><td colspan="2" rowspan="2">Minimum Return Loss (see notes 3 & 4)</td><td rowspan="2"></td><td colspan="2">Transmit</td><td colspan="2">Receive</td><td rowspan="2"></td></tr>
<tr><td>Min</td><td>Typ</td><td>Min</td><td>Typ</td></tr>
<tr><td></td><td>51 kHz - 102 kHz</td><td></td><td>8</td><td>30</td><td>12</td><td>30</td><td>dB</td></tr>
<tr><td></td><td>102 kHz - 2.048 MHz</td><td></td><td>14</td><td>30</td><td>18</td><td>30</td><td>dB</td></tr>
<tr><td></td><td>2.048 MHz - 3.072 MHz</td><td></td><td>10</td><td>25</td><td>14</td><td>30</td><td>dB</td></tr>
</table>

[1] Input signal to TCLK is jitter-free.

[2] Circuit attenuates jitter at 20 dB/decade above the corner frequency.

[3] In accordance with CCITT G.703/RC6367A return loss specifications (CEPT), when wired as shown in Figure 9.

[4] Guaranteed by design.

TABLE 1: Equalizer Control Inputs for Transmitter

EC3	EC2	EC1	Line Length[1]	Cable Loss[2]	Application	Frequency
0	1	1	0 - 133 ft ABAM	0.6 dB	DSX-1	1.544 MHz
1	0	0	133 - 266 ft ABAM	1.2 dB		
1	0	1	266 - 399 ft ABAM	1.8 dB		
1	1	0	399 - 533 ft ABAM	2.4 dB		
1	1	1	533 - 655 ft ABAM	3.0 dB		
0	0	0	CCITT Recommendation G.703		E1 - Coax (75 Ω)	2.048 MHz
0	0	1			E1 - Twisted-pair (120 Ω)	
0	1	0	FCC Part 68, Option A		CSU	1.544 MHz
0	1	1	ECSA T1C1.2			

[1] Line length from transceiver to DSX-1 cross-connect point.

[2] Maximum cable loss at 772 kHz.

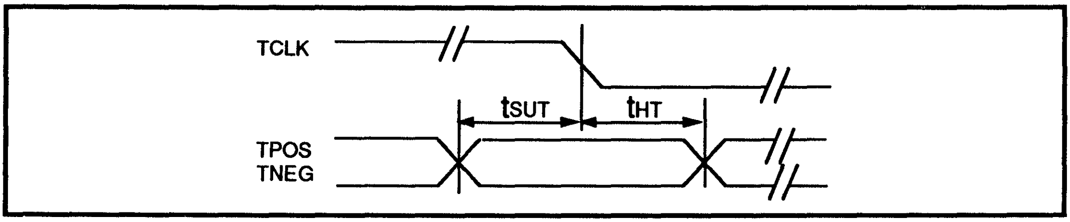


Figure 2: SSI 78P304A Transmit Clock Timing

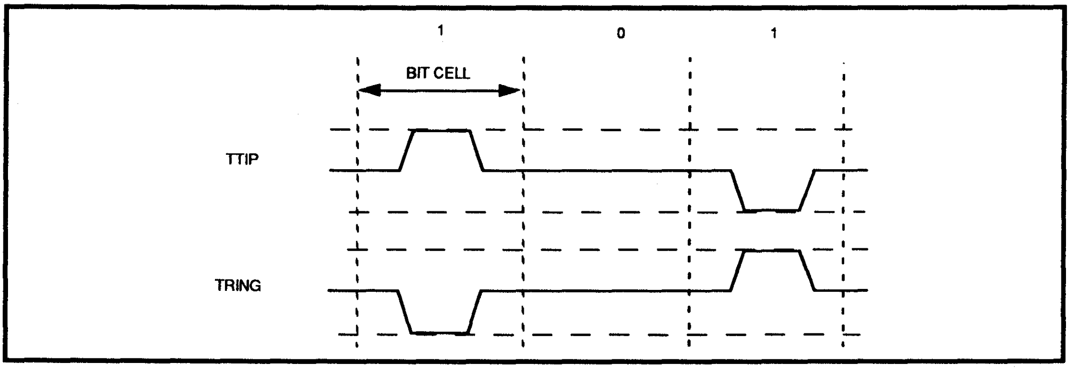


Figure 3: 50% AMI Coding

TABLE 2: SSI 78P304A Master Clock and Transmit Timing Characteristics (See Figure 2)

Parameter		Sym	Min	Typ[1]	Max	Units
Master clock frequency	DSX-1	MCLK	-	1.544	-	MHz
	E1	MCLK	-	2.048	-	MHz
Master clock tolerance		MCLKt	-	±100	-	ppm
Master clock duty cycle		MCLKd	40	-	60	%
Crystal frequency	DSX-1	fc	-	6.176	-	MHz
	E1	fc	-	8.192	-	MHz
Transmit clock frequency	DSX-1	TCLK	-	1.544	-	MHz
	E1	TCLK	-	2.048	-	MHz
Transmit clock tolerance		TCLKt	-	-	±50	ppm
Transmit clock duty cycle		TCLKd	40	-	60	%
TPOS/TNEG to TCLK setup time		t_{SUT}	25	-	-	ns
TCLK to TPOS/TNEG Hold time		t_{HT}	25	-	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

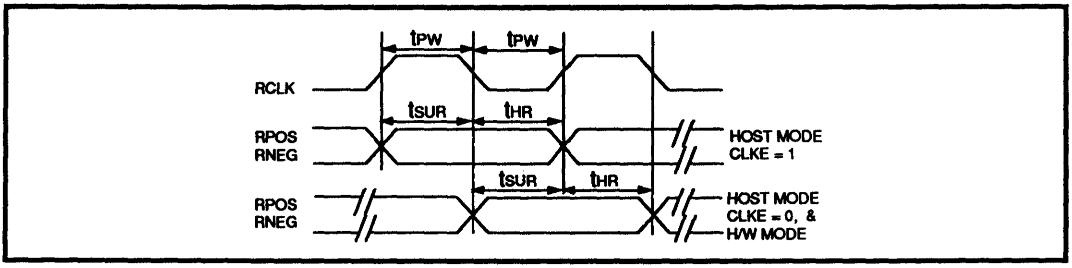


FIGURE 4: SSI 78P304A Receive Clock Timing

TABLE 3: SSI 78P304A Receive Timing Characteristics (See Figure 4)

Parameter		Sym	Min	Typ[1]	Max	Units
Receive clock duty cycle		RCLKd	40	-	60	%
Receive clock pulse width	DSX-1	t_{PW}	-	324	-	ns
	CEPT	t_{PW}	-	244	-	ns
RPOS / RNEG to RCLK rising setup time	DSX-1	t_{SUR}	-	274	-	ns
	CEPT	t_{SUR}	-	194	-	ns
RCLK rising to RPOS / RNEG hold time	DSX-1	t_{HR}	-	274	-	ns
	CEPT	tHR	-	194	-	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

TABLE 4: SSI 78P304A Crystal Specifications (External)

Parameter	T1	E1
Frequency	6.176 MHz	8.192 MHz
Frequency Stability	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)	±20 ppm @ 25° C ± 25 ppm from -40° C to + 85° C (Ref 25° C reading)
Pullability	CL = 11 pF to 18.7 pF, +ΔF = 175 to 195 ppm CL = 18.7 pF to 34 pF, -ΔF = 175 to 195 ppm	CL = 11 pF to 18.7 pF, +ΔF = 95 to 115 ppm CL = 18.7 pF to 34 pF, -ΔF = 95 to 115 ppm
Effective series resistance	40Ω Maximum	30Ω Maximum
Crystal cut	AT	AT
Resonance	Parallel	Parallel
Maximum drive level	2.0 mW	2.0 mW
Mode of operation	Fundamental	Fundamental
Crystal holder	HC49 (R3W), C_O = 7 pF maximum C_M = 17 pF typical	HC49 (R3W), C_O = 7 pF maximum C_M = 17 pF typical

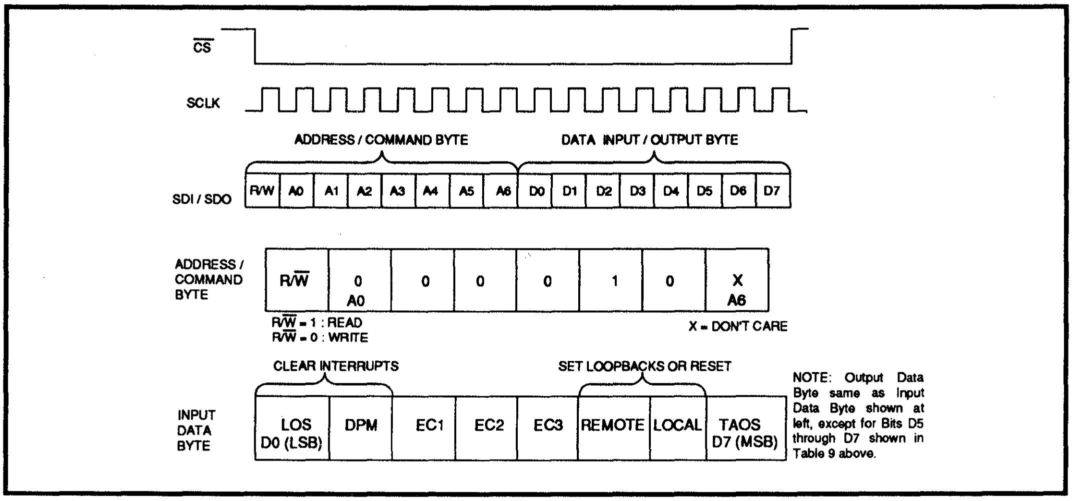


FIGURE 5: SSI 78P304A Serial Interface Data Structure

TABLE 5: SSI 78P304A Serial Data Output Bits (See Figure 5)

Bit D5	Bit D6	Bit D7	Status
0	0	0	Reset has occurred, or no program input.
0	0	1	TAOS active
0	1	0	Local Loopback active
0	1	1	TAOS and Local Loopback active
1	0	0	Remote Loopback active
1	0	1	DPM has changed state since last Clear DPM occurred
1	1	0	LOS has changed state since last Clear LOS occurred
1	1	1	LOS and DPM have both changed state since last Clear DPM and Clear LOS occurred

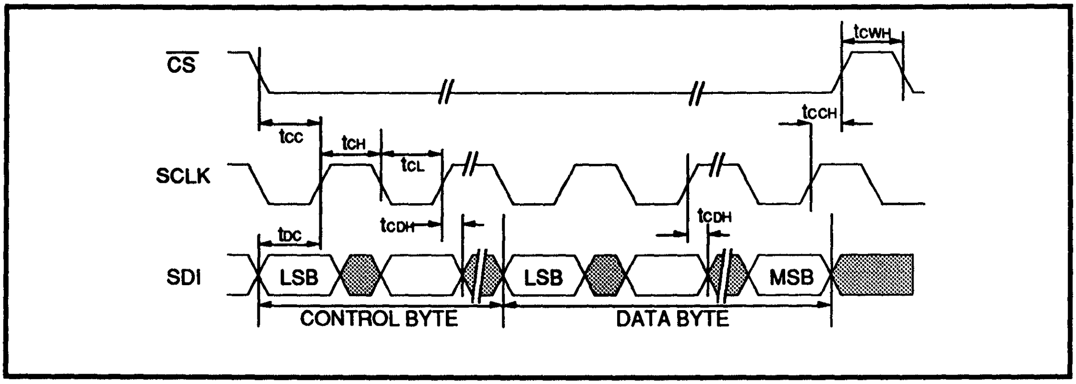


FIGURE 6: SSI 78P304A Serial Data Input Timing Diagram

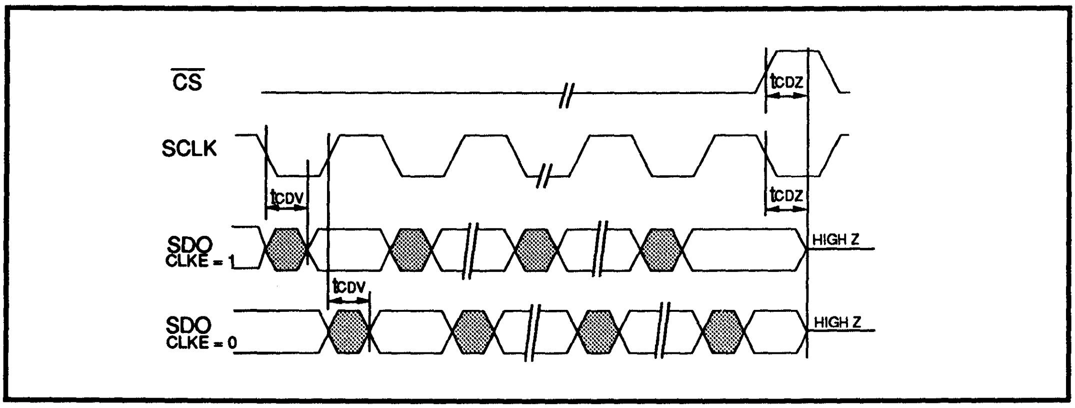


Figure 7: SSI 78P304A Serial Data Output Timing Diagram

TABLE 6: SSI 78P304A Serial I/O Timing Characteristics (See Figures 6 and 7)

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Rise/Fall time - any digital output	t_{RF}	-	-	100	ns	Load 1.6 mA, 50pF
SDI to SCLK setup time	t_{DC}	50	-	-	ns	
SCLK to SDI hold time	t_{CDH}	50	-	-	ns	
SCLK low time	t_{CL}	240	-	-	ns	
SCLK high time	t_{CH}	240	-	-	ns	
SCLK rise and fall time	t_R , t_F	-	-	50	ns	
$\overline{CS}$ to SCLK setup time	t_{CC}	50	-	-	ns	
SCLK to $\overline{CS}$ hold time	t_{CCH}	50	-	-	ns	
$\overline{CS}$ inactive time	t_{CWH}	250	-	-	ns	
SCLK to SDO valid	t_{CDV}	-	-	200	ns	
SCLK falling edge or $\overline{CS}$ rising edge to SDO high Z	t_{CDZ}	-	100	-	ns	

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

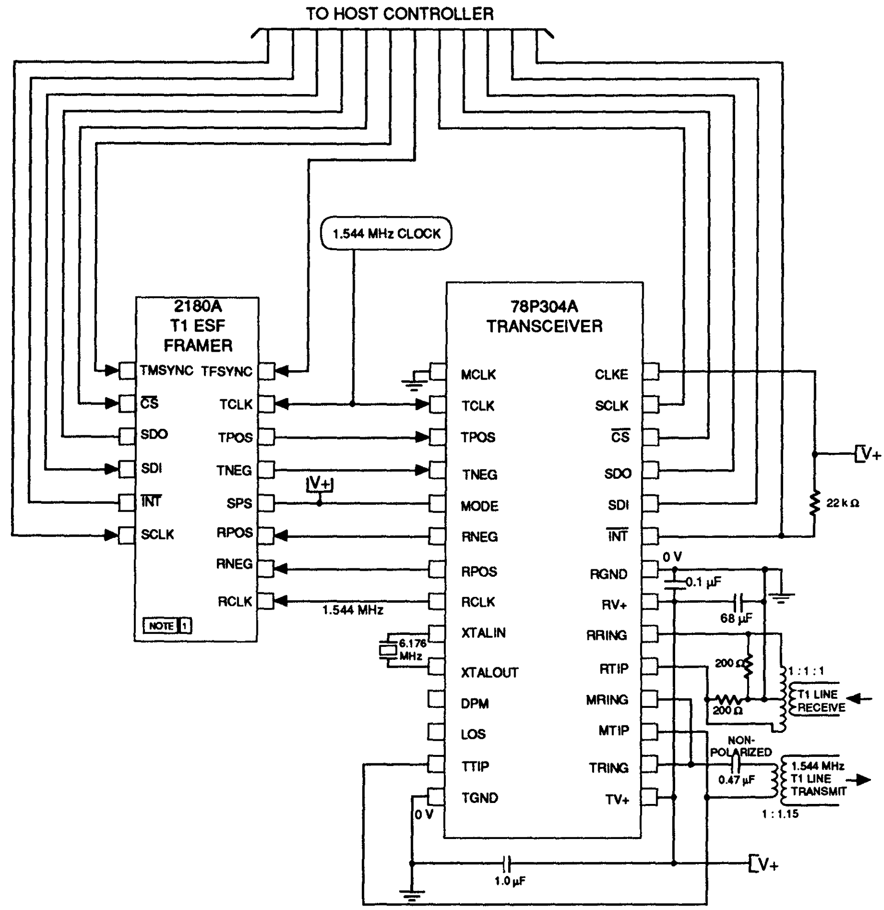
APPLICATION INFORMATION

1.544 MHz T1 INTERFACE APPLICATIONS

Figure 8 is a typical 1.544 MHz T1 application. The SSI 78P304A is shown in the Host mode with the 2180A T1/ESF Framer providing the digital interface with the host controller. Both devices are controlled through the serial interface. The power supply inputs are tied to a common bus with appropriate decoupling capacitors installed (1.0 µF on the transmit side, 68 µF and 0.1 µF on the receive side.)

TABLE 7: E1/CEPT Output Combinations

EC	75 Ω Coax	120 Ω TWP
0 0 1	1:1, Rt = 10 Ω	1:1, Rt = 0 Ω
0 0 1	1:2, Rt = 14.3 Ω	1:2, Rt = 15 Ω
0 0 0	1:1, Rt = 0 Ω	1:1.26, Rt = 0 Ω
0 0 0	1:2, Rt = 9.37 Ω	1:2, Rt = 8.7 Ω

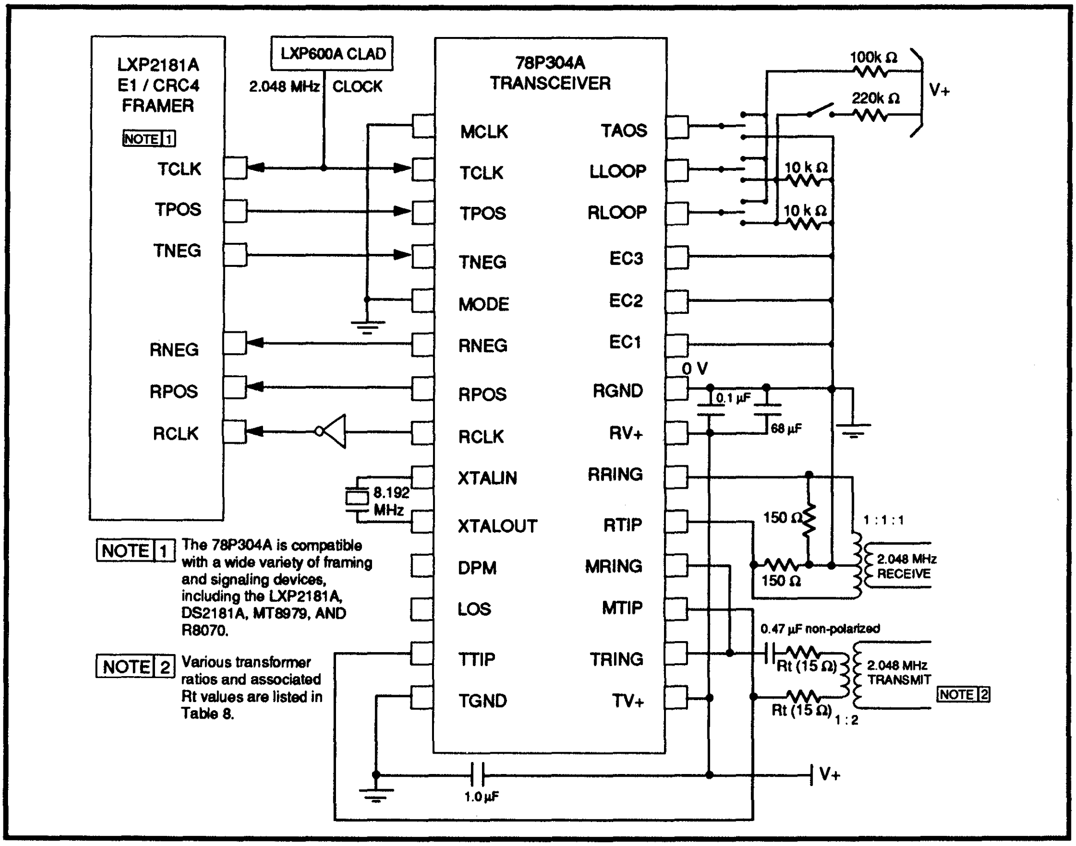


NOTE 1 THE SSI 78P304A IS COMPATIBLE WITH A WIDE VARIETY OF DIGITAL FRAMING AND SIGNALING DEVICES, INCLUDING THE LXP2180A, LXP2181, DS2180A, MT8976, AND R8070.

FIGURE 8: Typical SSI 78P304A 1.544 MHz T1 Application (Host Mode)

2.048 MHZ E1/CEPT INTERFACE APPLICATIONS

Figure 9 is a 2.048 MHz E1/CEPT coax application using EC code 000 and 15 Ω Rt resistors in line with the transmit transformer to provide high return loss. When high return loss is not a critical factor, a 1:1 or 1:1.26 transformer without in-line resistors provides maximum power savings. Table 7 lists transformer ratios and Rt values with associated 2.048 MHz EC codes for both 75Ω coax and 120Ω TWP. The SSI 78P304A is shown in Hardware mode with the 2181A E1/CRC4 Framer. The hard-wired control lines for TAOS, LLOOP and RLOOP are individually controllable, and the LLOOP and RLOOP lines are also tied to a single control for the Reset function. As in the T1 application Figure 8, this configuration is illustrated with a crystal in place to enable the SSI 78P304A Jitter Attenuation Loop, and a single power supply bus.



NOTE 1 The 78P304A is compatible with a wide variety of framing and signaling devices, including the LXP2181A, DS2181A, MT8979, AND R8070.

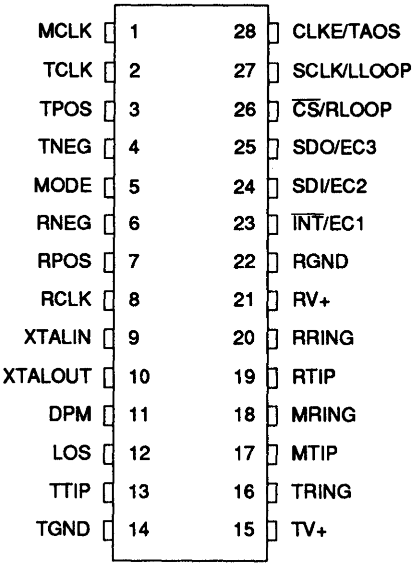
NOTE 2 Various transformer ratios and associated Rt values are listed in Table 8.

FIGURE 9: SSI 78P304A 2.048 MHz E1 Application (Hardware Mode)

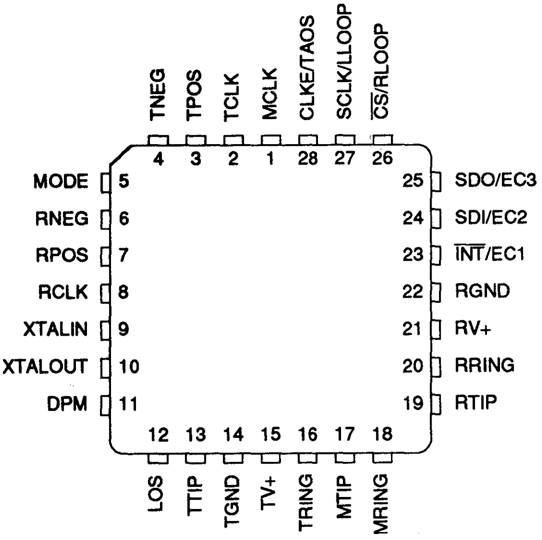
SSI 78P304A
Low-Power T1/E1 Integrated Short Haul Transceiver with Receiver Jitter Attenuation

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP



28-Pin PLCC

5

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78P304A 28-Pin DIP	78P304A-IP	78P304A-IP
SSI 78P304A 28-Pin PLCC	78P304A-IH	78P304A-IH

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 78P7200
DS-3 Line Interface with Receive Equalizer

December 1992

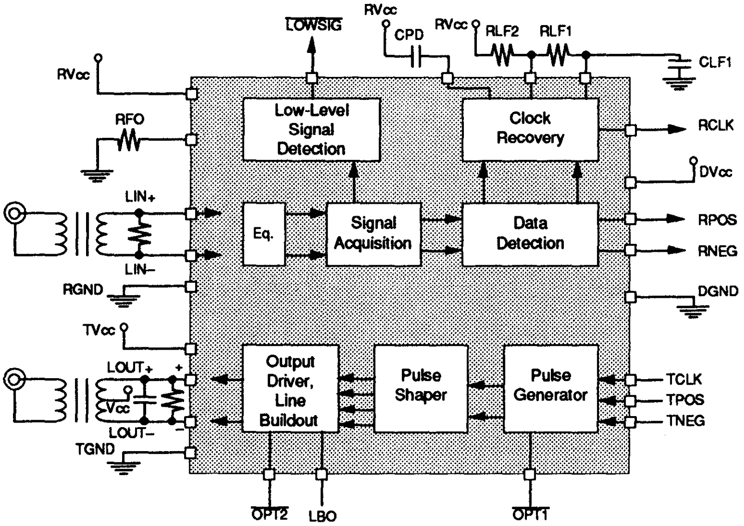
DESCRIPTION

The SSI 78P7200 is a line interface transceiver IC intended for DS-3 (44.736 Mbit/s) applications. The receiver has a very wide dynamic range and is designed to accept B3ZS-encoded Alternate-Mark Inversion (AMI) inputs; it provides clock, positive data, negative data, and low-level signal detector logical outputs. An on-chip equalizer improves the intersymbol interference tolerance on the receive path. The transmitter converts clock and data input signals into AMI pulses of the appropriate shape for transmission. A line buildout (LBO) equalizer may be selected to shape the outgoing pulses for shorter line lengths. The SSI 78P7200 requires a single 5 volt supply and is available in DIP and surface mount packages.

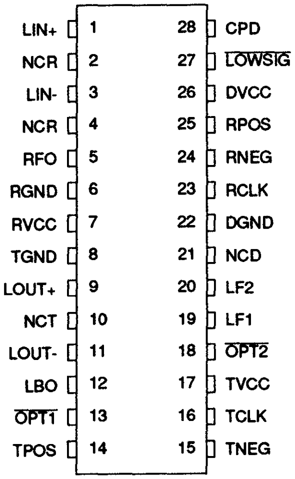
FEATURES

- **Single chip transmit and receive interface for DS-3 (44.736 Mbit/s) applications**
- **On-chip Receive Equalizer**
- **Unique clock recovery circuit, requires no crystals, tuned components or external clock**
- **Selectable transmit line buildout (LBO) to accommodate shorter line lengths**
- **Compliant with ANSI T1.102 - 1987, TR-TSY-000499 and CCITT G.703**
- **Low-level input signal indication**
- **Available in DIP or surface mount packages**
- **-40°C to +85°C operating range**
- **Pin-compatible with SSI 78P236, 78P2361 and 78P2362**

BLOCK DIAGRAM



PIN DIAGRAM



28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 78P7200
DS-3 Line Interface
with Receive Equalizer

FUNCTIONAL DESCRIPTION

The SSI 78P7200 is a single chip line interface IC designed to work with 44.736 Mbit/s DS-3 signals. The receiver recovers 44.736 MHz clock, positive data and negative data from an Alternate Mark Inversion (AMI) signal which has travelled a maximum of 450 feet from a DSX3 crosspoint over 75Ω coaxial cable (cable type WECO 728A, RG-59B or equivalent). The wide dynamic range of SSI 78P7200 allows for additional resistive attenuation. The input DS-3 signal should be B3ZS coded.

The transmitter accepts CMOS level logical clock, positive data and negative data and converts them to the AMI signal to drive a 75Ω coaxial cable. Programmable internal Line Buildout (LBO) circuitry eliminates the need for external LBO networks. The shape of the transmitted signal through any cable length of 0 to 450 feet complies with the published templates of ANSI T.102-1987, CCITT G.703 and TR-TSY-000499. The SSI 78P7200 is designed to work with a B3ZS coded signal. The B3ZS encoding and decoding functions are normally included in the DS-3 framer ICs or can easily be implemented in a PAL.

RECEIVER

The receiver input is normally transformer-coupled to the DS-3 signal. The inputs to the IC are internally referenced to RVCC so that when no transformer is used, a DC blocking capacitor of 0.01 µF should be used to isolate these pins from the DS-3 signal. Since the input impedance of the SSI 78P7200 is high, the DS-3 line must be terminated in 75Ω. The input signal to the SSI 78P7200 must be limited to a maximum of two consecutive zeros using a coding scheme such as B3ZS.

The DS-3 signal first enters a fixed equalizer which is designed to overcome the intersymbol interference caused by long cable lengths. The signal is then input to a variable gain differential amplifier whose output is maintained at a constant voltage level regardless of the input voltage level. The gain of this amplifier is adjusted by detecting the peak of the signal and comparing it to a fixed reference.

The output of the variable gain amplifier is compared to a threshold value which is a fixed percentage of the signal peak. In this way, even though the input signal amplitude may fall below the minimum value that can be regulated by the variable gain circuit, the proper detection threshold is maintained.

Output of the data comparators are connected to the clock recovery circuits. The clock recovery system employs a unique phase locked loop which has an auxiliary frequency-sensitive acquisition loop which is active only when cycle-slipping occurs between the received signal rate and the internal oscillator.

This system permits the loop to independently lock to the frequency and phase of the incoming data stream without the need for high precision and/or adjustable oscillator or tuned circuits.

The response characteristic for the phase locked loop is established by external filter components, RLF1, RLF2 and CLF1. The values of these components are specified such that the bandwidth of the phase locked loop is greater than 200 kHz.

The jitter tolerance of the SSI 78P7200 exceeds the requirements of TR-TSY-000499 for the category II of equipments. The jitter transfer function is maximally flat so the IC doesn't add any jitter to the system.

Figure 2 shows the recovered clock (RCLK), positive data (RPOS) and negative data (RNEG) signals timing. The data is valid on the rising edge of the clock. The minimum setup and hold times allow easy interface to all DS-3 framer circuits. These signals are CMOS-level outputs.

Should the input signal fall below a minimum value, the $\overline{\text{LOWSIG}}$ pin goes active low. A time delay is provided before this output is active so the transient interruptions do not needlessly cause the indication.

TRANSMITTER

The transmitter accepts unipolar CMOS level logical clock, positive data and negative data signals (TCLK, TPOS, TNEG) and generates high current drive pulses on the LOUT+ and LOUT- pins. When properly connected to a center tapped transformer, an AMI pulse is generated which can drive a 75Ω coaxial cable (type WE728A or RG59B).

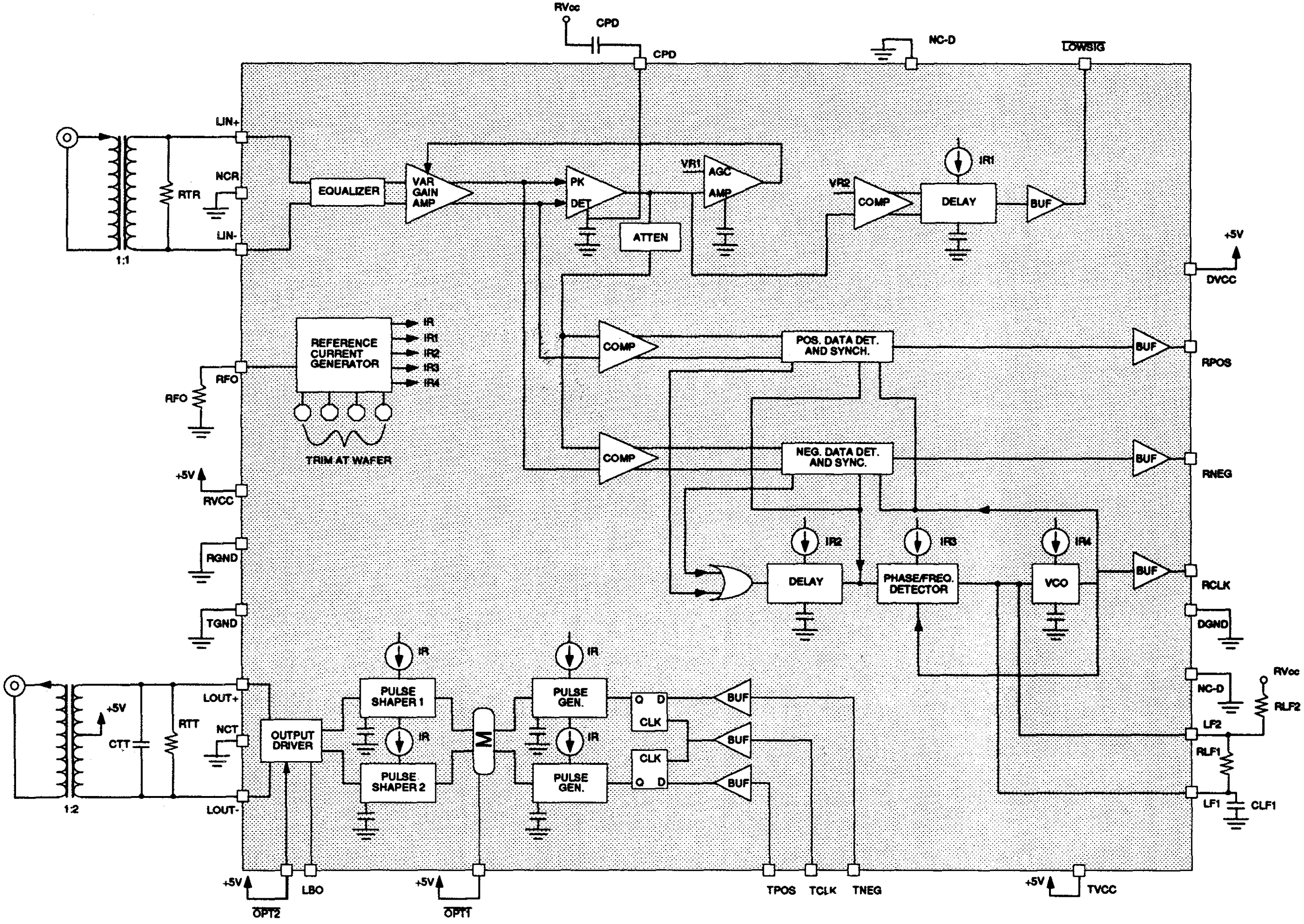
Figure 3 shows the timing for the transmitter logic signals. The output pulse width is internally set and is not sensitive to input clock (TCLK) pulse width.

When a recommended transformer is used, the transmitted pulse shape at the end of a 75Ω terminated cable of 0 to 450 feet will fit the template for DSX3 pulse published in ANSI T1.102-1987, BELLCORE TR-TSY-000499 and CCITT G.703 documents.

The SSI 78P7200 incorporates a selectable Line Buildout (LBO) equalizer in the transmitter path. The LBO pin should be set HIGH if the cable is shorter than 225 feet. For longer cable lengths, the LBO pin should be set LOW.

The $\overline{\text{OPT1}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT1}}$ pin to LOW increases the transmitter power.

The $\overline{\text{OPT2}}$ pin should be set HIGH for normal operation. Setting the $\overline{\text{OPT2}}$ pin to LOW disables the transmitter circuity and reduces the power consumption of the IC by 125 mW.



Note: NC pins should be tied to the ground pin indicated by the trailing letter.

FIGURE 1: Functional Diagram

PIN DESCRIPTION

RECEIVER

NAME	TYPE	DESCRIPTION
LIN+, LIN-	I	Differential inputs, transformer-coupled from line.
RPOS	O	Unipolar receiver output, active as result of positive pulse at inputs.
RNEG	O	Unipolar receiver output, active as result of negative pulse at inputs.
RCLK	O	Clock pulses recovered from line data.
$\overline{\text{LOWSIG}}$	O	Low signal logic output indicating that input signal is less than threshold value.

TRANSMITTER

TPOS	I	Unipolar transmitter data input, active high.
TNEG	I	Unipolar transmitter data input, active high.
TCLK	I	Transmitter clock input, active high.
LOUT+	O	Output to transformer for positive data pulses.
LOUT-	O	Output to transformer for negative data pulses.
LBO	I	Line buildout control. Selected for shorter cable lengths.
$\overline{\text{OPT1}}$	I	Transmit option 1. Selects faster output pulse transition time and higher amplitude when low.
$\overline{\text{OPT2}}$	I	Transmit option 2. Disables output driver and reduces output bias current when low.

EXTERNAL COMPONENT CONNECTION

RFO	I	Resistor connected to RGND to provide basic center frequency of receiver phase locked loop oscillator.
LF1, LF2	-	Resistor-capacitor loop filter network to establish bandwidth of phase locked loop.
CPD	-	Capacitor to RVcc that is connected to peak detector node to reduce signal-dependent ripple on that node.

POWER

TVcc	-	5V power supply for transmit circuits.
RVcc	-	5V power supply for receive circuits.
DVcc	-	5V power supply for receive logic circuits.
TGND	-	Ground return for transmit circuits.
RGND	-	Ground return for receive circuits.
DGND	-	Ground return for receive logic circuits.
NC	-	No connect. These pins are not connected to the chip. They should be tied to the appropriate ground pin (see figure 1) to minimize pin-to-pin coupling capacitance.

ELECTRICAL SPECIFICATIONS

(T_A = -40°C to 85°C, Vcc = 5V ±5%, unless otherwise noted.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value. Operation above absolute maximum ratings may permanently damage the device.

ABSOULUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive 5.0V supply: TVcc, RVcc, DVcc	6.0	V
Storage Temperature	-65 to 150	°C
Soldering Temperature (10 sec.)	260	°C
Ambient Operating Temperature, T_A	-40 to +85	°C
Pin Ratings: LIN+, LIN-, TPOS, TNEG, TCLK, LOUT+, LOUT-, LBO, RFO, LF2, LF1, $\overline{\text{OPT1}}$, $\overline{\text{OPT2}}$ Pins	-0.3 to Vcc +0.3	V
Pin Ratings: RPOS, RNEG, RCLK, $\overline{\text{LOWSIG}}$ Pins	-0.3 to Vcc +0.3	V
	or +12	mA

SUPPLY CURRENTS AND POWER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC Supply Current	Outputs Unloaded, normal operation, transmit and receive all 1's pattern		150	182	mA
P Power Dissipation	Outputs unloaded, TA = 85°C			0.93	W

EXTERNAL COMPONENTS (Refer to Figure 1 for location of components.)

RFO Loop center frequency resistor	1% tolerance		5.25		kΩ
RLF1 Loop filter resistor	1%		6.04		kΩ
RLF2 Loop filter resistor	1%		100		kΩ
CLF1 Loop filter capacitor	5%		0.22		µF
RTR Receive termination resistor	1%		75		Ω
CTT Transmit termination capacitor	5%			20	pF
RTT Transmit termination resistor	1%		301		Ω
CPD Peak detector capacitor	5%		0.022		µF

ELECTRICAL SPECIFICATIONS (Continued)

DIGITAL INPUTS AND OUTPUTS

(CMOS-compatible pins: $\overline{\text{LOWSIG}}$, RPOS, RNEG, RCLK, TPOS, TNEG, TCLK, LBO, $\overline{\text{OPT1}}$.) Currents flowing into the chip are positive. Current maximums are currents with the largest absolute value.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	Input low voltage		-0.3		1.5	V
VIH	Input high voltage		3.5		Vcc +0.3	V
IIL	Input low current	VIL = 1.5V	-5.0		5.0	µA
IIH	Input high current	VIH = 3.5V	-5.0		5.0	µA
VOL	Output low voltage	IOL = 0.1 mA			1.0	V
VOH	Output high voltage	IOH = -0.1 mA	4.0			V

$\overline{\text{OPT2}}$ CHARACTERISTICS

VIL	Input low voltage	IIL = 0.4 mA			0.5	V
VIH	Input high voltage		2.0			V

RECEIVER

All of the measurements for the receiver are made with the following conditions unless otherwise stated:

1. The input signal is transformer coupled as shown in Figure 1.
2. RFO = 5.25 kΩ
3. The circuit is connected as in Figure 1.
4. The maximum cable length (type 728-A or RG-59B) to DSX-3 point is 450 ft.

VIN	Input signal voltage	Input AC-Coupled	±0.045		±1.20	Vpk
RIN	Input Resistance	Input at chip's common mode voltage	15	20	30	kΩ
VDTH	Receive data detection threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		50		%
VLOW	Receive data low signal threshold	Relative to peak amplitude for 22.37 MHz sinusoidal input		±55		mV
VLOWT	Receive data low signal delay	Relative to peak amplitude for 22.37 MHz sinusoidal input		500		µs
TRCF	Receive clock period			22.35		ns
TRC	Receive clock pulse width			12.24		ns
TRCPT	Receive clock positive transition time	C_L = 15 pF		4.5	6	ns
TRCNT	Receive clock negative transition time	C_L = 15 pF		4.5	6	ns

RECEIVER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TRDP TRDN	Positive or negative receive data pulse width			22.35		ns
TRDPS TRDNS	Receive data set-up time		5	11.18	13.7	ns
TRDPH TRDNH	Receive data hold time		5	11.18	13.7	ns
	Receive input jitter tolerance	sine, 60 kHz	±3.35			ns
	high frequency	to 300 kHz	0.3			UIPP
	Receive input jitter tolerance	sine, 10 Hz to 2.3 kHz	±55.88			ns
	low frequency		5.0			UIPP
KD	Clock Recovery Phase Detector Gain	All 1's data pattern KD = .418/RFO	72	80	88	µA/Rad
KO	Clock Recovery Phase Locked Oscillator Gain		12	14.5	17	Mrad/ sec. -Volt

TRANSMITTER

All of the measurements for the transmitter are made with the following conditions unless otherwise stated:

1. Transmit pulse characteristics are obtained using a line transformer which has the characteristics TBD.
2. The circuit is connected as in Figure 1.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTCF	Transmit clock repetition period			22.35		ns
TTC	Transmit clock pulse width			11.18		ns
TTCNT	Transmit clock negative transition time			4.5	6	ns
TTCPT	Transmit clock positive transition time			4.5	6	ns
TTPDS TTNDS	Transmit data set-up time		3.5	11.18		ns
TTPDH TTNDH	Transmit data hold time		3.5	11.18		ns
TTPL	Transmit positive line pulse width	Measured at transformer, LBO = Low	10.62	11.18	12.0	ns

TRANSMITTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTNL	Transmit negative line pulse width	Measured at transformer, LBO = Low	10.62	11.18	12.0	ns
	Transmit line pulse waveshape	See Note				

Note: Characteristics are in accordance with ANSI T1.102 - 1987, Table 5 and Figure 8.

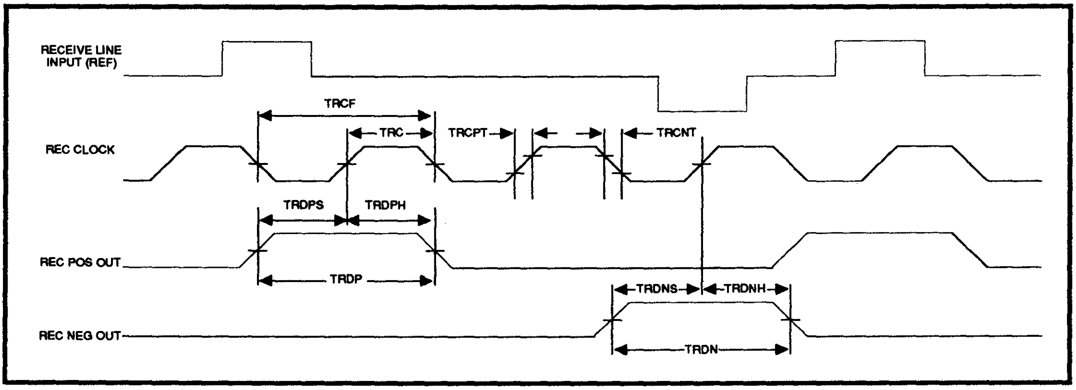


FIGURE 2: Receive Waveforms

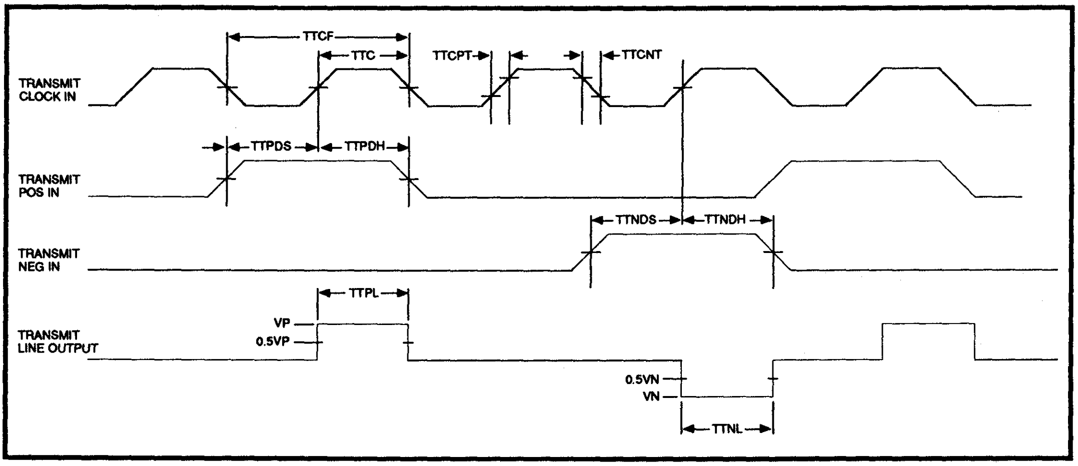
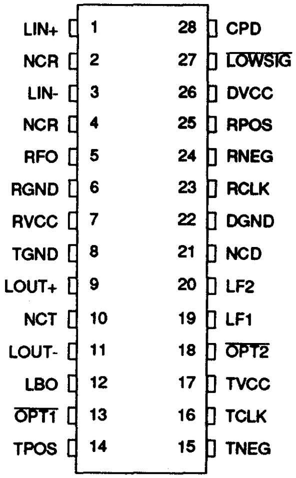


FIGURE 3: Transmit Waveforms

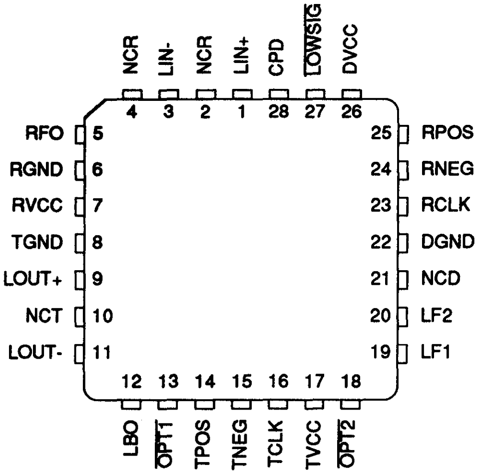
SSI 78P7200
DS-3 Line Interface with Receive Equalizer

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 78P7200, DS-3 Line Interface – 28-pin		
Standard Width Plastic DIP (600 mil)	78P7200-IP	78P7200-IP
Surface Mount 28-pin PLCC	78P7200-IH	78P7200-IH

Section 6

LAN PRODUCTS

silicon systems®
A TDK Group Company

SSI 78Q902
Ethernet Twisted-Pair Media Attachment Unit

December 1992

DESCRIPTION

The SSI 78Q902 twisted-pair Media Attachment Unit (TP-MAU) is designed to allow Ethernet connections to use the existing twisted-pair wiring plant through an Ethernet Attachment Unit Interface (AUI). The SSI 78Q902 provides the electrical interface between the AUI and the twisted-pair wire.

SSI 78Q902 functions include level-shifted data pass-through from one transmission media to another, collision detection, Signal Quality Error (SQE) testing and automatic correction of polarity reversal on the twisted pair input. It also includes LED drivers for transmit, receive, jabber, collision, reversed polarity detect and link functions.

The SSI 78Q902 is an advanced CMOS device and requires only a single 5-volt power supply.

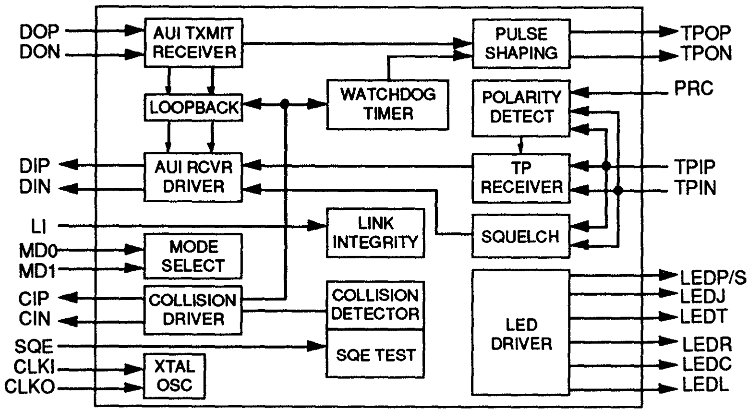
APPLICATIONS

- Computer/workstation interface boards
- LAN repeater
- External 10Base-T converter

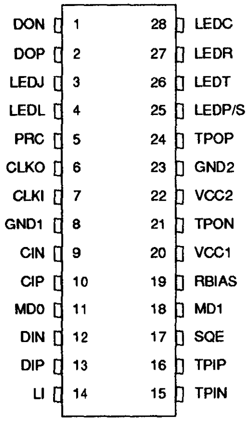
FEATURES

- **Meets or exceeds IEEE 802.3 standards for AUI and 10Base-T interface**
- **Direct interface to AUI and RJ45 connectors**
- **Automatic AUI/RJ45 selection**
- **Internal predistortion generation**
- **Internal common mode voltage generation**
- **Jabber function**
- **Selectable link test, SQE test disable**
- **Twisted-pair receive polarity reverse detection and selectable polarity correction**
- **LED driver for transmit, receive, jabber, collision, link and reversed polarity indicators or for flashing status indicator**
- **Single +5V supply, CMOS technology**
- **Available in 28-pin DIP or PLCC**

BLOCK DIAGRAM



PIN DIAGRAM



28-Pin DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78Q902 Media Attachment Unit (MAU) interfaces the Attachment Unit Interface (AUI) to the unshielded twisted pair cables, transferring data in both directions between the two. The AUI side of the interface comprises three circuits: Data Output (DO), Data Input (DI) and Collision Interface (CI). The twisted pair network side of the interface comprises two circuits: Twisted Pair Input (TPI) and Twisted Pair Output (TPO). In addition to the five basic circuits, the SSI 78Q902 contains an internal crystal oscillator, separate power and ground pins for analog and digital circuits, various logic controls and six LED drivers for status indications.

Functions are defined from the AUI side of the interface. The SSI 78Q902 Transmit function refers to data transmitted by the Data Terminal Equipment (DTE) through the AUI and MAU to the twisted pair network. The SSI 78Q902 Receive function refers to data received by the DTE through the MAU and AUI from the twisted pair network. In addition to basic transmit and receive functions, the SSI 78Q902 performs all required MAU functions defined by the IEEE 802.3 10Base-T specification such as collision detection, link integrity testing, Signal Quality Error (SQE), jabber control and loopback.

TRANSMIT FUNCTION

The SSI 78Q902 transfers Manchester encoded data from the AUI port of the DTE (the DO circuit) to the twisted pair network (the TPO circuit). The output signal on TPON and TPOP is pre-distorted to meet the 10 Base-T jitter template, and filtered to meet FCC requirements. The output waveform (after the transmit filter) is shown in Figure 1. If the differential inputs at the DO circuit fall below 75% of the threshold level for 8 bit times (typical), the SSI 78Q902 transmit function will enter the idle state. During idle periods, the SSI 78Q902 transmits link integrity test pulses on the TPO circuit.

RECEIVE FUNCTION

The SSI 78Q902 receive function transfers serial data from the twisted pair network (the TPI circuit) to the DTE (over the DI circuit of the AUI). An internal squelch function discriminates noise from link test pulses and valid data streams. Only valid data streams activate the receive function. If the differential inputs at the TPI circuit fall below 75% of the threshold level (unsquelched) for 8 bit times (typical), the SSI 78Q902 receive function will enter the idle state. The TPI threshold can be reduced by approximately 3 dB to allow for longer loops in low-noise environments. The reduced threshold is selected when MD1 = 0 and MD0 = 1.

DIFFERENTIAL INPUT MODE

In the differential input mode, the transmit interface consists of TXP and TXN, PE, PDC, and the Transmit Enable input ($\overline{\text{TEN}}$). Transmission starts when PE is high and $\overline{\text{TEN}}$ is low, and ends when either PE or $\overline{\text{TEN}}$ goes inactive. Predistortion control is provided by the PDC input.

POLARITY REVERSE FUNCTION

The SSI 78Q902 polarity reverse function uses both link pulses and end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight opposite receive link pulses are detected without receipt of a link pulse with the expected polarity. Reversed polarity is also detected if four frames are received with a reversed start-of-idle. Whenever polarity is reversed, these two counters are reset to zero. If the SSI 78Q902 enters the link fail state and no data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity is disabled, polarity detection is based only on received data pulses.)

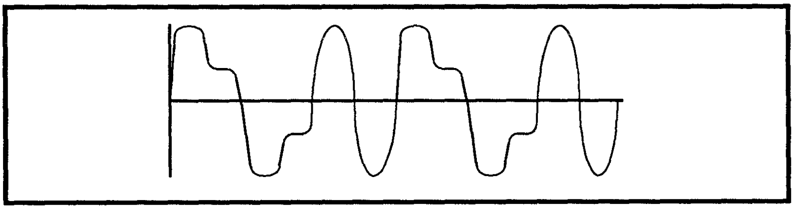


FIGURE 1: 78Q902 TPO Output Waveform

COLLISION DETECTION FUNCTION

The collision detection function operates on the twisted pair side of the interface. A collision is defined as the simultaneous presence of valid signals on both the TPI circuit and the TPO circuit. The SSI 78Q902 reports collisions to the AUI by sending a 10 MHz signal over the CI circuit. The collision report signal is output no more than 9 bit times (BT) after the chip detects a collision. If the TPI circuit becomes active while there is activity on the TPO circuit, the TPI data is passed to the DTE over the DI circuit, disabling the loopback. Figure 2 is a state diagram of the SSI 78Q902 collision detection function (refer to IEEE 802.3 10Base-T specification).

LOOPBACK FUNCTION

The SSI 78Q902 loopback function operates in conjunction with the transmit function. Data transmitted by the DTE is internally looped back within the SSI 78Q902 from the DO pins to the DI pins and returned to the DTE. The loopback function is disabled when a data collision occurs, clearing the DI circuit for the TPI data. Loopback is also disabled during link fail and jabber states.

SQE TEST FUNCTION

Figure 3 is a state diagram of the SQE Test function. The SQE test function is enabled when the SQE pin is tied high. When enabled, the SQE test sequence is transmitted to the controller after every successful transmission on the 10Base-T network. When a successful transmission is completed, the SSI 78Q902 transmits the SQE signal to the AUI over the CI circuit for 10 BT ± 5 BT. The SQE function can be disabled for hub applications by tying the SQE pin to ground.

JABBER CONTROL FUNCTION

Figure 4 is a state diagram of the SSI 78Q902 Jabber control function. The SSI 78Q902 on-chip watchdog timer prevents the DTE from locking into a continous transmit mode. When a transmission exceeds the time limit, the Watchdog timer disables the transmit and loopback functions, and sends the SQE signal to the DTE over the CI circuit. Once the SSI 78Q902 is in the jabber state, the DO circuit must remain idle for a period of 491 to 525 ms before it will exit the jabber state.

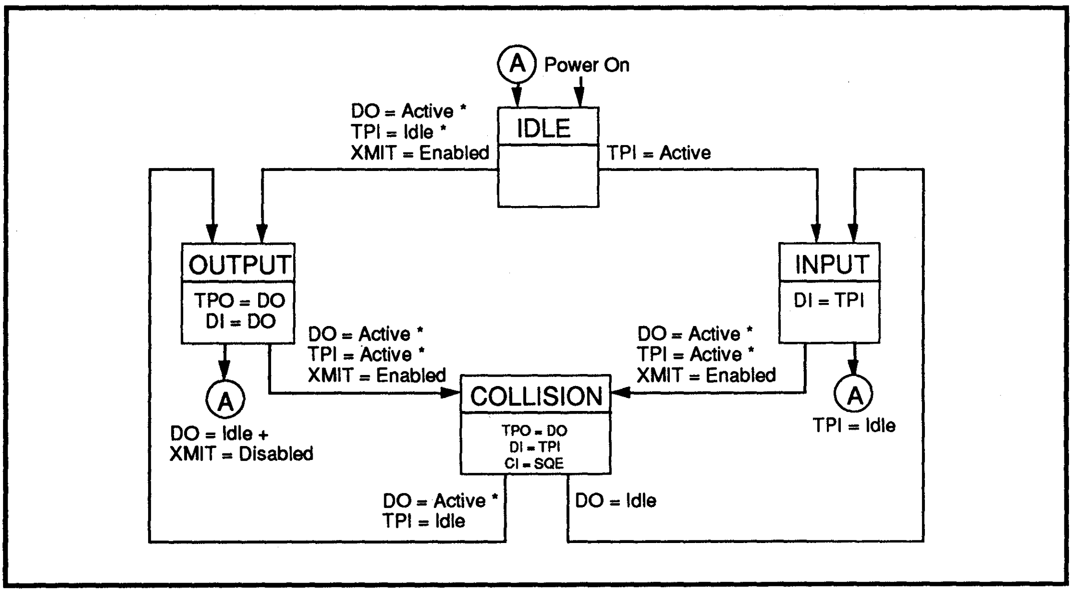


FIGURE 2: Collision Detection Function

LINK INTEGRITY TEST FUNCTION

Figure 5 is a state diagram of the SSI 78Q902 Link Integrity Test Function. The Link Integrity Test is used to determine the status of the receive side twisted pair cable. The link integrity test is enabled when the LI pin is tied high. When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50 - 150 ms, the chip enters a link fail state and disables the transmit and loopback functions. The SSI 78Q902 ignores any link integrity pulse with intervals less than 2 - 7 ms. The SSI 78Q902 will remain in the link fail state until it detects either a serial data packet or two or more link integrity pulses.

TEST MODE

The SSI 78Q902 Test mode is selected when a 2 to 2.5 MHz clock is input on the MD0 mode select pin. Test mode sets the internal counter chains to run at 1024 times their normal speed. The maximum transmit time, unjab time, Link Integrity timing and LED timing are reduced by a factor of 1024. During test operation, 10 MHz and 20 MHz signals are output on the PRC and SQE pins, respectively. When Test mode is selected, the SQE function cannot be disabled. In Test mode the PRC function can be disabled by the LI pin. Jabber can be disabled by setting MD1 = 0.

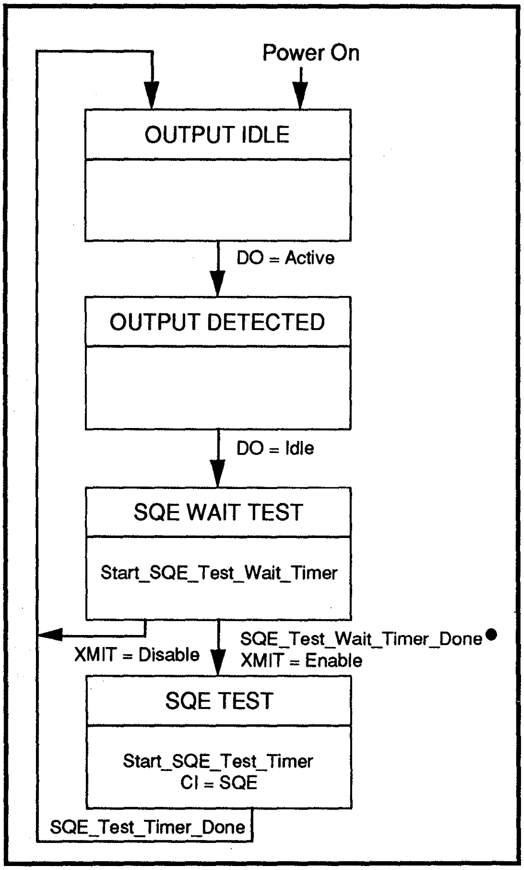


FIGURE 3: SQE Test Function

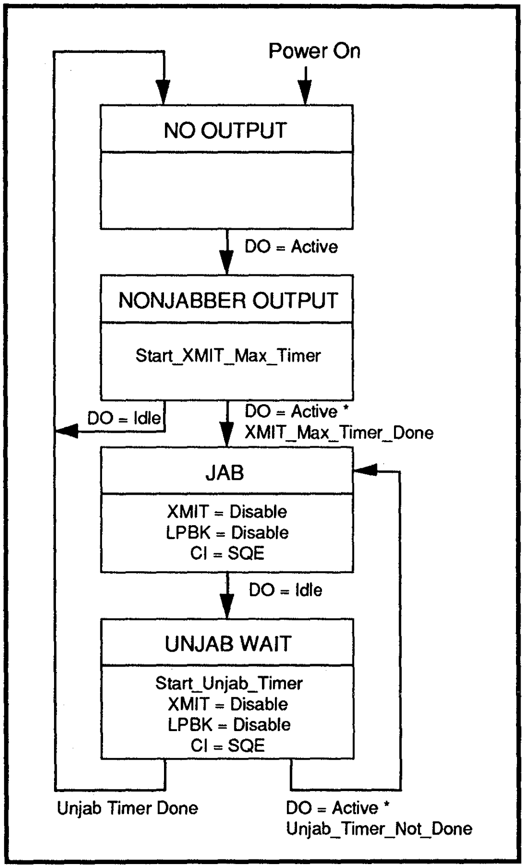


FIGURE 4: Jabber Control Function

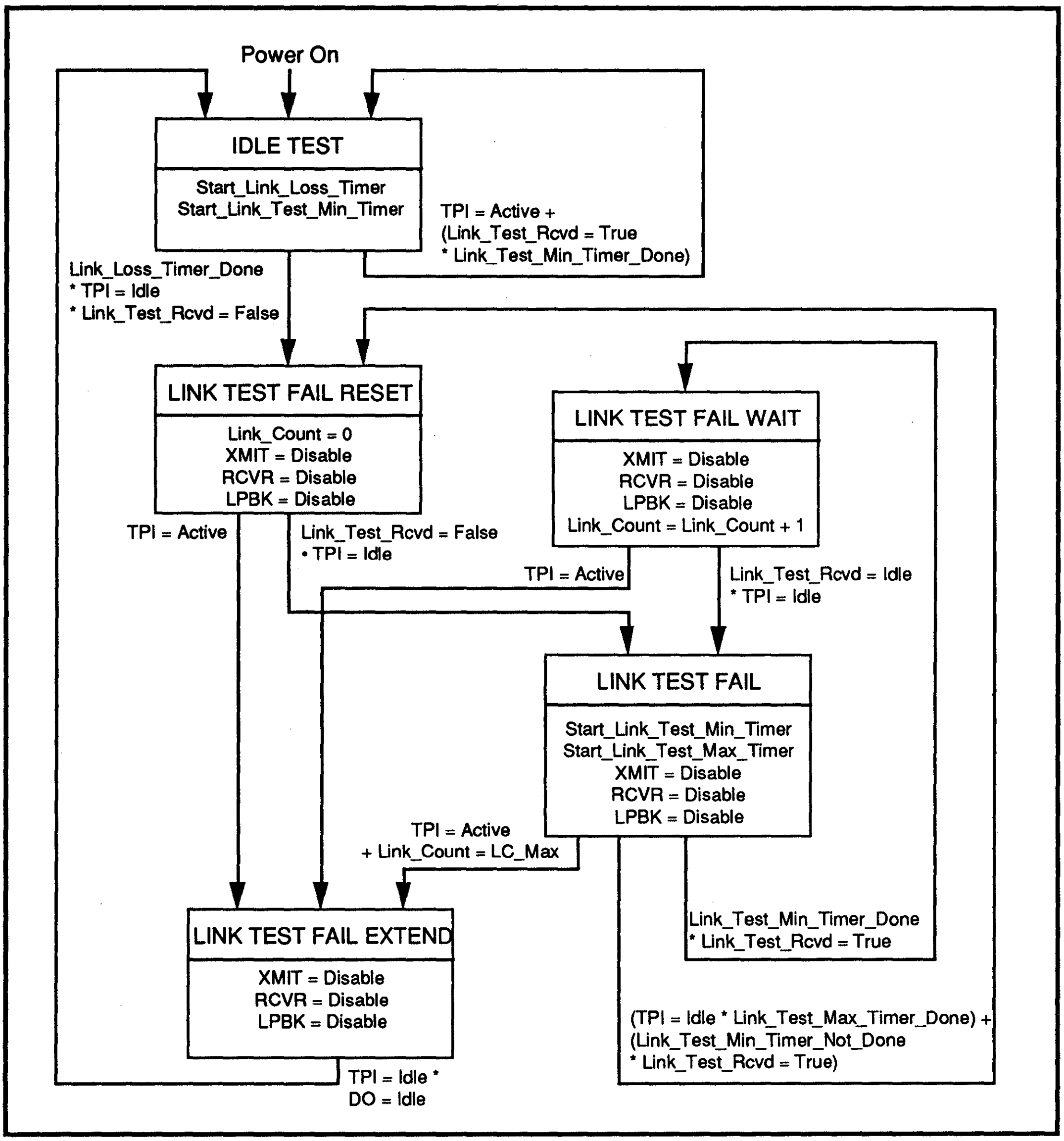


FIGURE 5: Link Integrity Test Function

TABLE 1: Mode Select Options

MD1	MD0	MODE
0	0	Base-T compliant MAU
0	1	Reduced squelch level
1	0	Half current AUI driver
1	1	DO, DI & CI ports disabled
1	Clock	Test mode, jabber on
0	Clock	Test mode, jabber disabled

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
DON/DOP	I	Data Out Negative/Data Out Positive: Differential input pair connected to the AUI transceiver DO circuit
LEDJ	I/O	Jabber LED Driver: Open drain driver for the Jabber indicator LED. Output goes active[1] when watchdog timer begins jab, and stays active until end of the unjab wait period (491 - 525 ms). When tied to ground, causes LEDP/S to act as a multi-function blinking status indicator.
LEDL	O	Link LED Driver: Open drain driver for the Link indicator LED. Output is active except during Link Fail or when Link Integrity Test is disabled.
PRC	I/O	Polarity Reverse Correction: The SSI 78Q902 automatically corrects reversed polarity at TPI when PRC is tied high. In Test mode, this pin is a 10 MHz output.
CLKO/CLKI	-	Crystal Oscillator: The SSI 78Q902 requires either a 20 MHz crystal (or ceramic resonator) connected across these pins, or a 20 MHz clock applied at CLKI.
GND1	-	Ground #1.
CIN/CIP	O	Collision Negative/Collision Positive: Differential driver output pair tied to the collision presence pair of the Ethernet transceiver AUI cable. The collision presence signal is a 10 MHz square wave. This output is activated when a collision is detected on the network, during self-test by the SQE sequence, or after the watchdog timer has expired to indicate the transmit wire pair has been disabled.
MD0	I	Mode Select 0: Selects operating modes in conjunction with MD1. See Table 1 above for mode select options.
DIN/DIP	O	Data In Negative/Data In Positive: Differential driver pair connected to the AUI transceiver DI circuit.

[1] LED drivers pull low when active.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
LI	I	Link Integrity Test Enable: Link integrity testing is enabled when this pin is tied high. With link test enabled, the SSI 78Q902 sends the link integrity signal in the absence of transmit traffic. It also recognizes received link test pulses, indicating the receive wire pair is present in the absence of transmit traffic.
TPIN/TPIP	I	Twisted Pair Receive Inputs: Differential receive inputs from the twisted pair input filter.
SQE	I/O	Signal Quality Error Test Enable: SQE is enabled when this pin is tie high. When enabled, the SSI 78Q902 sends the signal quality error test sequence to the CI of the AUI cable after every successful transmission to the media. In Test mode, SQE becomes a 20 MHz output.
MD1	I	Mode Select 1: Selects operating modes in conjunction with MD0, (see Table 1). MD1 clock input between 2.0 and 2.5 MHz enables Test mode.
RBIAS	-	Resistor Bias Control: Bias control pin for the operating circuit. Bias set from external resistor to ground. External resistor value = 12.4 kΩ (±1%).
VCC1	I	Power Supply 1: +5V power supply.
TPON/TPOP	O	Twisted Pair Transmit Outputs: Transmit drivers to the twisted-pair output filter. The output is Manchester encoded and pre-distorted to meet the 10Base-T template.
VCC2	I	Power Supply 2: +5V power supply.
GND2	-	Ground #2.
LEDP/S	O	Polarity/Status LED Driver: Open drain LED driver. In normal mode, LEDP/S is active when reversed polarity is detected. If LEDJ is tied to ground, the output LEDP/S indicates multiple status conditions as shown in Figure 6. On solid = Normal, 1 Blink = Link Down, 2 Blinks = Jabber, 5 Blinks = Polarity Reversed
LEDT	O	Transmit LED Driver: Open drain driver for the Transmit indicator LED. Output is active during transmit.
LEDR	O	Receive LED Driver: Open drain driver for the Receive indicator LED. Output is active during receive.
LEDC	O	Collision LED Driver: Open drain driver for the Collision indicator LED. Output is active when a collision occurs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNIT
Supply Voltage, Vcc	-0.3 to 6	V
Operating Temperature, T_{OP}	0 to +70	°C
Storage Temperature, T_{ST}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage[1], Vcc		4.75	5.0	5.25	V
Operating Temperature, T_{OP}		0	-	70	°C

[1] Maximum voltage differential between VCC1 and VCC2 must not exceed 0.3V.

SWITCHING CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

PARAMETER	CONDITIONS	MIN	NOM [1]	MAX	UNIT
Jabber Timing					
Maximum transmit time [2]		98.5	-	131	ms
Unjab time [2]		491	-	525	ms
Time from Jabber to CS0 on CIP/CIN[3]		0	-	900	ns
Link Integrity Timing					
Time link loss [2]		65	-	66	ms
Time between Link Integrity Pulses [2]		9	-	11	ms
Interval for valid receive Link Integrity Pulses [2]		4.1	-	65	ms
Collision Timing					
Simultaneous TPI/TPO to CSO state on CIN/CIP		0	-	900	ns
DO loopback to TPI on DI[3]		300	-	900	ns
CS0 state delay after TPI/DO idle[3]		-	-	900	ns
CS0 high pulse width		40	-	60	ns
CS0 low pulse width		40	-	60	ns
CS0 frequency		-	10	-	MHz

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

[2] Switching times reduced by a factor of 1024 during Test mode.

[3] Parameter is guaranteed by design; not subject to production testing.

SWITCHING CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%) (continued)

PARAMETER	CONDITIONS	MIN	NOM[1]	MAX	UNIT
SQE Timing					
SQE signal duration		500	-	1500	ns
Delay after last positive transition of DO		0.6	-	1.6	µs
LED Timing					
LEDC, LEDT, LEDR on time[2]		100	-	-	ms
LEDP/S on time[2] (See Figure 6)		-	164	-	ms
LEDP/S period [2] (See Figure 6)		-	328	-	ms
General					
Receive start-up delay		0	-	500	ns
Transmit start-up delay		0	-	200	ns
Loopback start-up delay		0	-	500	ns

[1] Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

[2] Switching times reduced by a factor of 1024 during Test mode.

I/O ELECTRICAL CHARACTERISTICS (Ta = 0 to 70 °C, Vcc = 5V ±5%)

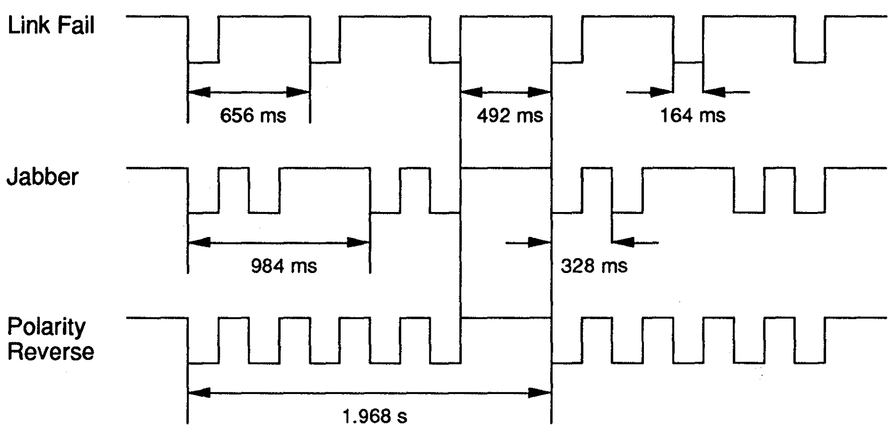
PARAMETER	CONDITIONS	MIN	NOM[1]	MAX	UNIT
Input low voltage[2] V_{IL}		-	-	0.8	V
Input high voltage[2] V_{IH}		2.0	-	-	V
Output low voltage V_{OL} (Open drain LED Driver[3])	R_{LOAD} = 2 kΩ	-	-	0.13	V
Supply current I_{CC}	Line Idle	-	60	69.3	mA
(Vcc1 = Vcc2 = 5.25V)	Line Active, transmitting all ones	-	125	140	mA
Input leakage current[4] I_{LL}	Input between VCC and GND	-	±1	±10	µA
Tristate leakage current I_{TS}	Output between VCC and GND	-	±1	±10	µA

[1] Typical figures are at 25°C and are for desing aid only; not guaranteed and not subject to production testing.

[2] MD0, MD1, SQE, PRC and LI pins. MD1 clock (test mode) must be CMOS level input.

[3] LED Drivers can sink up to 10 mA of drive current.

[4] Not including TPIN, TPIP, DOP or DON.



NOTE: LEDP/S status indications are shown in order of priority, i.e., Link Fail indication supersedes Jabber indication which supersedes Polarity Reverse (when PRC = 1). Reversed polarity conditions supersede Link Fail conditions when PRC = 0 (Polarity Correction Disabled). At the LEDL indicator, reversed polarity condition reported as Link Fail when PRC = 0. This allows the user to distinguish between actual link failure and apparent link failure due to polarity reversal.

FIGURE 6: LEDP/S Status Indication Timing

AUI ELECTRICAL CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

PARAMETER		CONDITIONS	MIN	NOM[1]	MAX	UNIT
Input low current	I_{IL}		-	-	-700	µA
Input high current	I_{IH}		-	-	500	µA
Differential output voltage	V_{OD}		±550	-	±1200	mA
Differential squelch threshold	V_{DS}		-	220	-	mV
Receive input impedance	Rz	Between DOP and DON	-	20	-	kΩ

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

TRANSMIT CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

PARAMETER	CONDITIONS	MIN	NOM[1]	MAX	UNIT
Transmit output impedance Z_{OUT}		-	5	-	Ω
Peak differential output voltage V_{OD}	Load = 200Ω at TPOP and TPON	±4.5	-	±5.2	V
Transmit timing jitter addition[2]	After Tx filter, 0 line length	-	-	±8	ns
Transmit timing jitter addition[2]	After Tx filter, line model as shown in IEEE 802.3 standard for 10Base-T	-	-	±3.5	ns

RECEIVE CHARACTERISTICS (Ta = 0 to 70°C, Vcc = 5V ±5%)

Receive input impedance Z_{IN}	Between TPIP/TPIN	-	20	-	kΩ
Differential squelch threshold V_{DS}		-	420	-	mV
Reduced squelch threshold V_{DSR}		-	300	-	mV
Receive timing jitter[2]		-	-	1.5	ns

[1] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

[2] Parameter is guaranteed by design; not subject to production testing.

APPLICATION INFORMATION

EXTERNAL MAU

Figure 7 shows the SSI 78Q902 in a typical external MAU application, interfacing between an AUI and the RJ45 connectors of the twisted pair network. A 20 MHz crystal (or ceramic resonator) connected across CLKI and CLKO provides the required clock signal. Transmit and receive filters are required in the TPO and TPI circuits. Details of the transmit and receive filters are shown in Figures 8 and 9, respectively. (Differential filters are also recommended.)

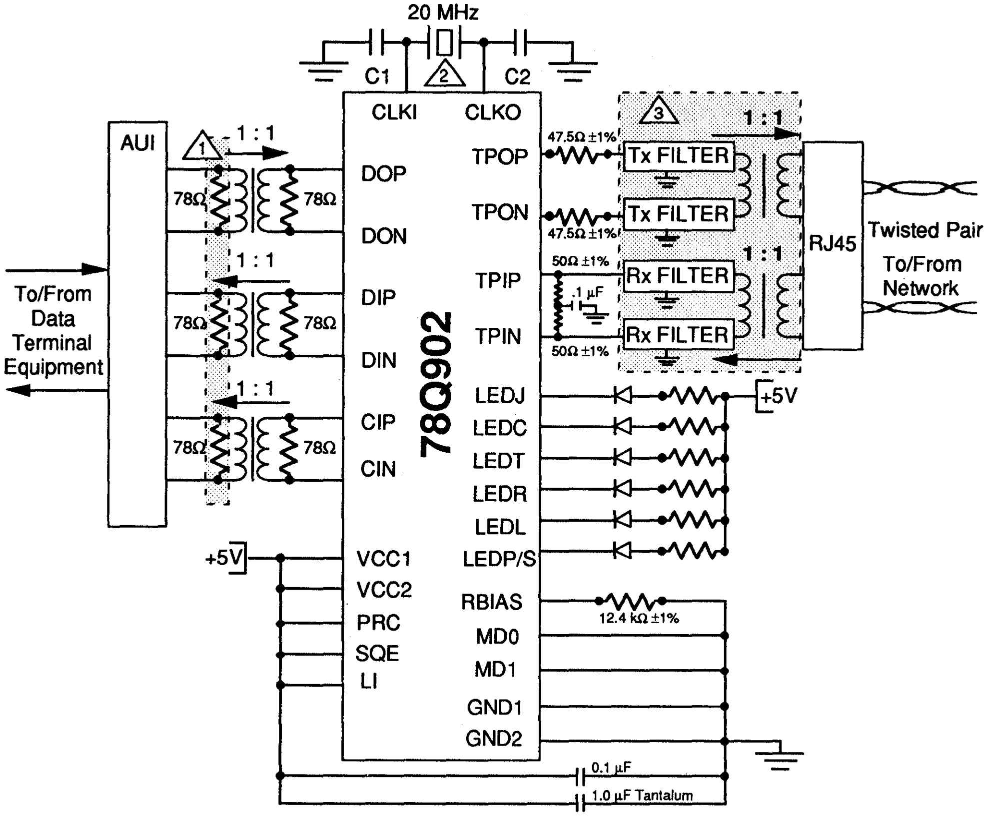
INTERNAL MAU

Figure 10 shows an internal MAU application which takes advantage of the SSI 78Q902's unique AUI/10Base-T switching feature to select either the D-connector (AUI) or the RJ45 connector (10Base-T). No termination resistors are used on the SSI 78Q902 side of the AUI interface to prevent impedance mismatch with the drop cable. The half current drive mode is used to maintain the same voltage levels in the absence of termination resistors. This application uses capacitive coupling instead of transformer coupling. MD1 is tied high so MD0 functions as the mode control switch.

When MD0 is low, the half current drive mode is selected. When MD0 is high, the SSI 78Q902 is effectively removed from the circuit. The 902 AUI ports (DO, DI and CI) are disabled isolating the SSI 78Q902 from the AUI. The SSI 78Q902 DI and CI ports go to a high impedance state and the DO port is ignored.

To implement an auto-select function, LEDL can be tied to MD0. This activates the 902/AUI interface when the TP link is active (data or link integrity pulses) and disables it when the link is inactive.

SSI 78Q902
Ethernet Twisted-Pair Media Attachment Unit



1 Typically, resistors on the AUI side of the transformer are already present in the terminal. If termination resistors are present in the terminal, the shaded resistors are not required.

2 A 20 MHz (±1%) crystal or ceramic resonator may be used at CLKI/CLKO.

3 Suitable integrated filter/transformers include TDK Corporation HIM 3000, Pulse Engineering PE65421, FilMag 78Z1120B and Valor PT3877.

FIGURE 7: SSI 78Q902 External MAU Application Diagram

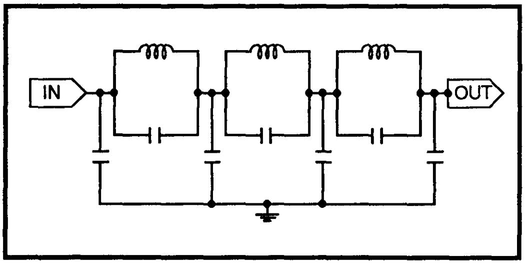


FIGURE 8: Transmit Filter Diagram

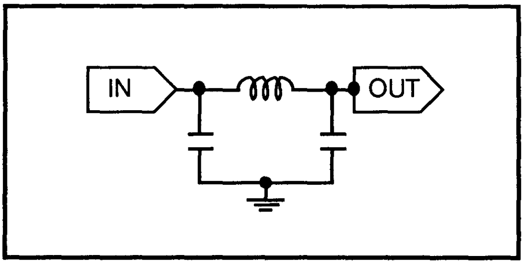
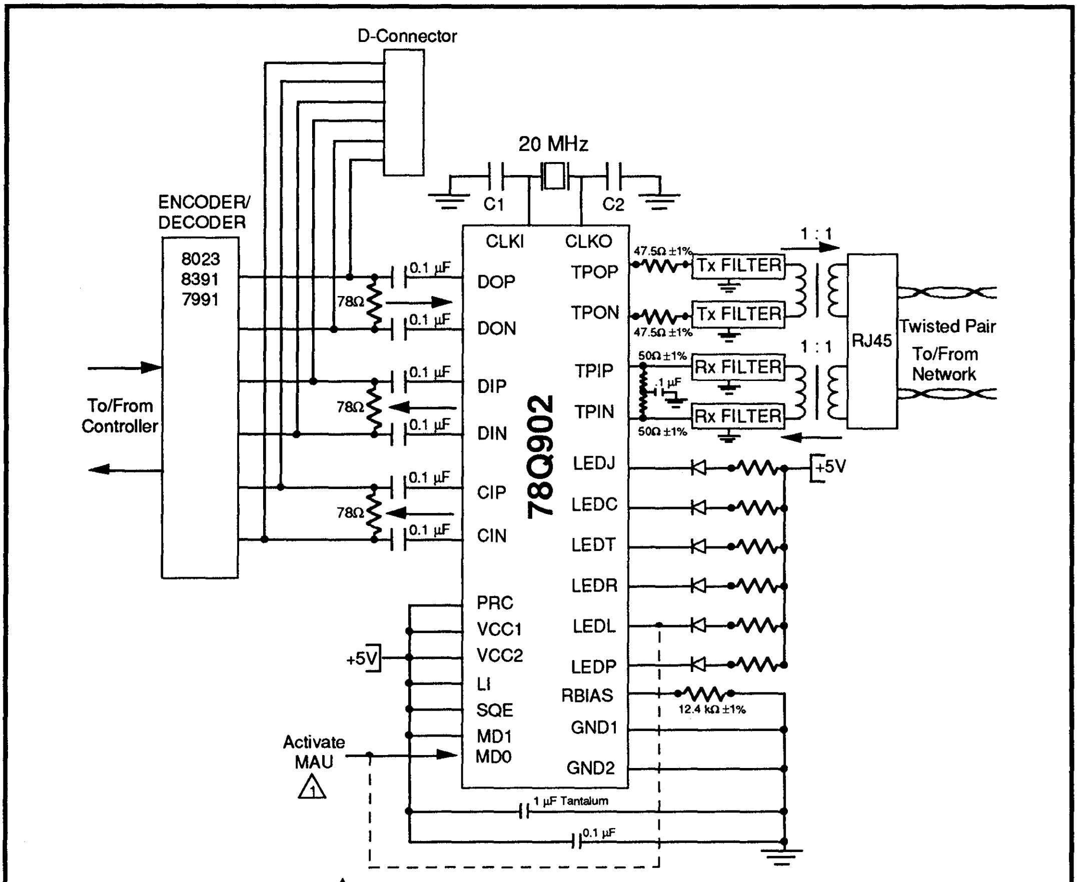


FIGURE 9: Receive Filter Diagram



1 Connect LEDL to MD0 to implement auto-select feature.

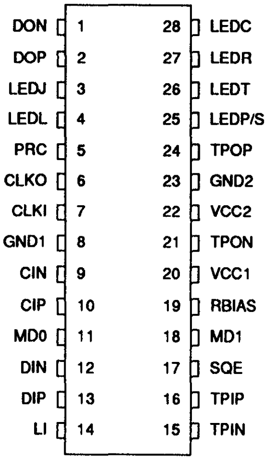
FIGURE 10: SSI 78Q902 Internal MAU Application Diagram

SSI 78Q902
Ethernet Twisted-Pair Media Attachment Unit

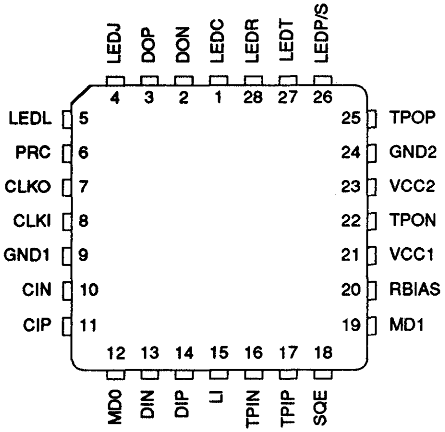
PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78Q902 28-Pin DIP	78Q902-CP	78Q902-CP
SSI 78Q902 28-Pin PLCC	78Q902-CH	78Q902-CH

silicon systems®
A TDK Group Company

SSI 78Q8330/8330A
Ethernet Coaxial Transceiver

January 1993

DESCRIPTION

The SSI 78Q8330 and SSI 78Q8330A are line transceivers for IEEE 802.3 coaxial cable applications. The SSI 78Q8330 is compliant with thin cable (10Base2) requirements and compatible with thick cable (10Base5) operation. The SSI 78Q8330A is tested to be compliant with both 10Base2 and 10Base5 requirements.

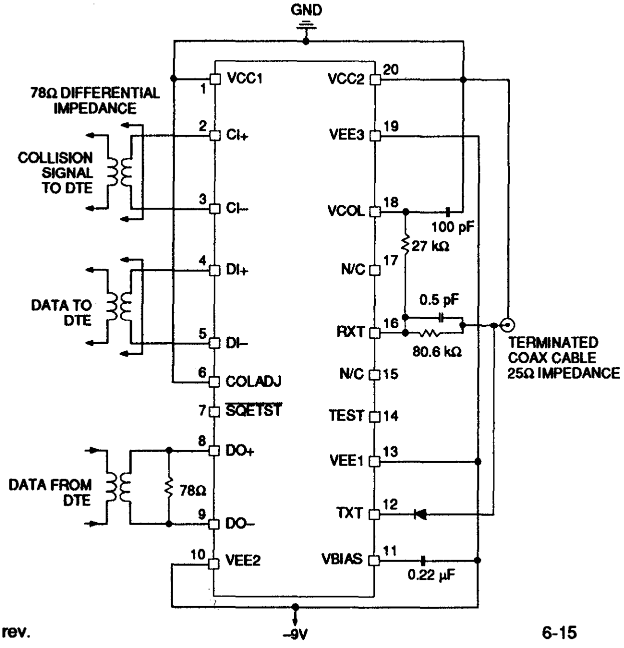
These transceivers provide the interface between the single-ended coaxial cable signals and the Manchester-encoded differential logic signals. Primary functional blocks include the receiver, transmitter, collision detection and jabber timer. These ICs may be used in either internal or external MAU environments.

The SSI 78Q8330/8330A design is optimized for low power consumption. Typical supply current while transmitting is 96 mA, and only 56 mA when not transmitting. The low power consumption coupled with 20-pin PLCC or 64-lead TQFP packaging make this product ideal for portable computer applications.

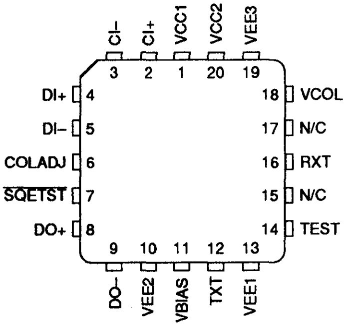
FEATURES

- **SSI 78Q8330 compliant with 10Base2 and compatible with 10Base5 requirements**
- **SSI 78Q8330A compliant with both 10Base2 and 10Base5 requirements**
- **Innovative design minimizes power consumption - ideal for portable computer applications**
- **Integrated jabber timer function**
- **Minimal external component count**
- **For internal or external MAU applications**
- **Available in 20-pin PLCC, DIP, or 64-lead TQFP**

SSI 78Q8330 CONNECTION DIAGRAM



PIN DIAGRAM



20-pin PLCC

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 78Q8330/8330A IEEE-802.3/Ethernet/ Cheapernet Transceiver consists of four sections: 1) Transmit - receives signals from DTE and sends it to the coaxial medium, 2) Receive - obtains data from medium and sends it to DTE, 3) Collision Detect - indicates to DTE any collision on the medium, and 4) Jabber - guards medium from DTE transmissions that are excessive in length.

TRANSMITTER

The SSI 78Q8330/8330A receives differential signals from the DTE over the AUI interface.

Differential data is received through a squelch network that rejects signals with pulse widths less than 7 ns, or with levels more positive than -175 mV peak. Signals with pulse widths wider than 50 ns and levels more negative than -275 mV peak from the DTE are guaranteed to be enabled. This minimizes false starts due to noise and ensures no valid packets are missed.

The coax driver provides the driving capability to ensure adequate signal level at the end of the maximum length network segment (500m 10Base5, 185m 10Base2) under the worst-case number of connections (100 nodes 10Base5, 30 nodes 10Base2). The required rise and fall times of data transmitted on the network are maintained by the driver. The driver's output is connected to the medium through external isolating diodes. To safeguard network integrity, the driver is disabled whenever power falls below the minimum operation voltage.

During transmission, the jabber controller monitors the duration that the transmit driver is active and disables the driver if the jabber time is exceeded. This prevents network tie-up due to a "jabbering" transmitter. Once disabled, the driver remains disabled for an additional 310-500 ms after the DO± pair is idle. During the disable time, the 10 MHz internal oscillator signal is sent on the CI± pair to the DTE.

When $\overline{\text{SQETST}}$ is tied to VEE, the IC generates a Collision Detect message at the end of every transmission. This signal is a self-test indication to the DTE that the Medium Attachment Unit (MAU) collision pair is operational.

RECEIVE AND CARRIER DETECT

Received signals are acquired from the coax tap through a high-impedance resistive divider. A high input-impedance (low capacitance, high bandwidth) DC-coupled input amplifier in the chip receives the signal. The received signal is internally AC coupled and then sliced. The carrier detector compares received signals to a reference. Signals meeting carrier squelch criteria are passed to the differential line driver within five bit times from the start of packet.

Received data is transmitted from the DI± pair through an isolation transformer of the AUI interface. Following the last transition in a packet, the DI± pair is held high for two bit times and then decreases to the idle level within eighty bit times.

COLLISION DETECT

The SSI 78Q8330/8330A detects collisions if two or more stations are transmitting on the network.

The average DC level of received signals is compared against the collision threshold reference. If the level is more negative than the reference, an enable signal is generated to the CI± pair.

The collision oscillator is a 10 MHz oscillator which drives the differential CI± pair to the DTE through an isolation transformer. This signal is gated to the CI± pair whenever there is a collision, a Collision Detect test is in progress, or the jabber controller is activated.

The CI± output meets the drive requirements for the AUI interface. The output stays high for two bit times at the end of the packet, decreasing to the idle level within eighty bit times.

JABBER FUNCTION

The jabber timer monitors the activity on the DO± pair and senses TXT faults. It inhibits transmission if the coax driver is active for longer than the jabber time (20-35 ms). A 10 MHz internal oscillator signal is enabled on the CI± pair for the fault duration after the jabber time is exceeded.

After the fault is removed, the jabber timer counts the unjab time of 310-500 ms before it enables the driver.

SQE TEST

A Signal Quality Error (SQE) test will occur at the end of every transmission if the $\overline{\text{SQETST}}$ pin is tied to VEE. An SQE test signal is a 10 MHz signal gated to the CI± pair. The SQE test ensures that the twisted pair assigned for collision notification to the DTE is intact and operational. The SQE test starts eight bit times after the last transition of the transmitted signal and lasts for a duration of eight bit times.

The SQE test can be disabled by connecting the $\overline{\text{SQETST}}$ pin to GND.

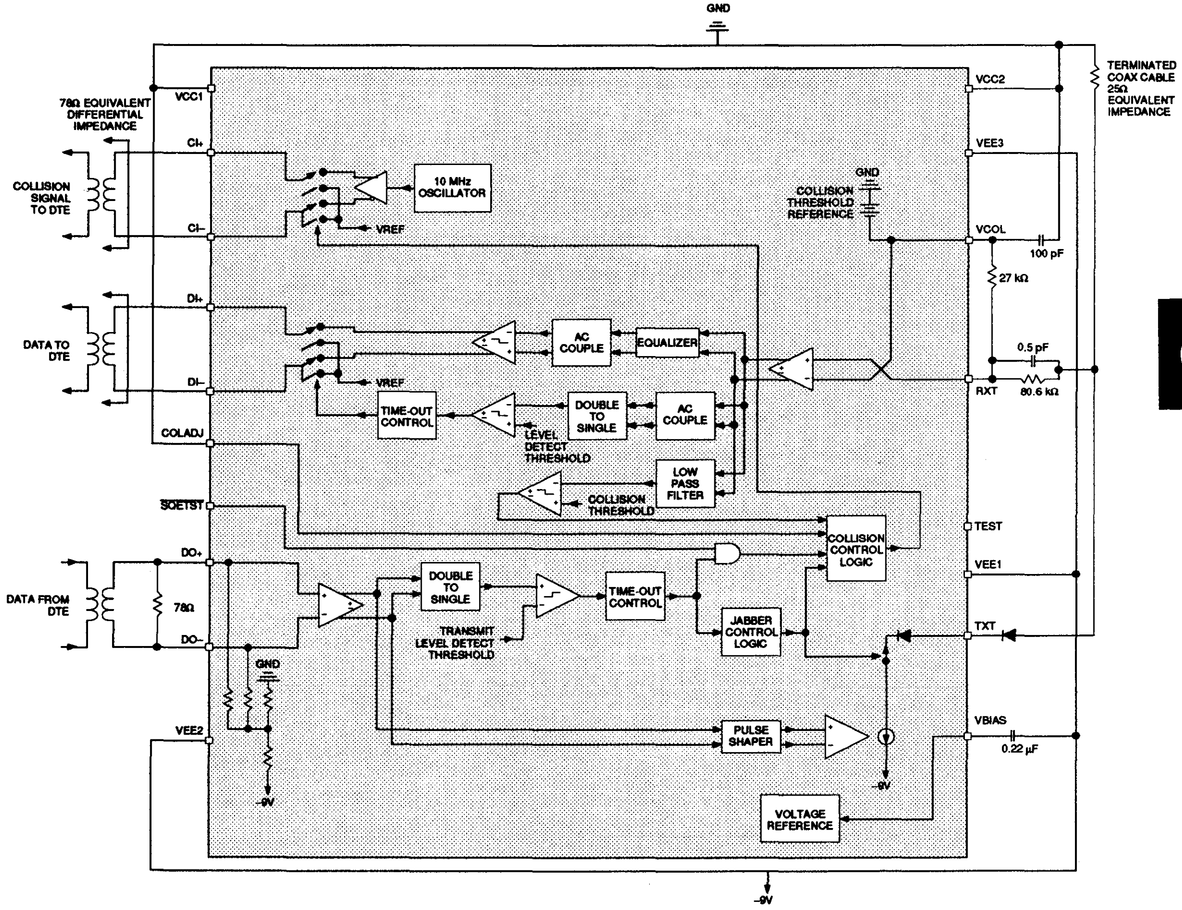


FIGURE 1 : Functional Diagram

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC1, VCC2	-	Positive supply to chip. Tied to external ground.
VEE1, VEE2, VEE3	-	Negative supply to chip. Tied to external -9 volts.
TXT	O	Open collector output current data to coax cable.
DO+, DO-	I	Differential input data from DTE.
RXT	I	Input data from coax cable.
VCOL	I	Collision threshold reference.
DI+, DI-	O	Differential output data to DTE.
CI+, CI-	O	Differential output collision detect signal to DTE.
$\overline{\text{SQETST}}$	I	Pin to activate collision detect test circuit.
VBIAS	-	External bypass pin for internally generated voltage bias.
TEST	I	Pin for placing chip in test mode.
COLADJ	I	Pin tied to VEE sets proper 10BASE5 collision threshold detect level. Pin left open sets proper 10BASE2 collision threshold detect level.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 8.1V < VCC-VEE < 9.9V and 0 °C < T(ambient) < +70 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value. Unless otherwise specified, test configuration is as shown in Figure 1.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage; Vcc (Relative to VEE Pins)	-0.5 to +12 V
VBIAS Pin	-40mA to +40 mA
All other Pins	VEE - 0.3V to VCC + 0.3V
Storage Temperature	-65 to 150 °C
Soldering (Reflow or Dip)	260 °C for 10 sec

POWER SUPPLY CURRENTS AND POWER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Current	Includes current from VCC1, VCC2, TXT pins				
Transmitter active			96	121	mA
Transmitter inactive			56	74	mA

TTL COMPATIBLE INPUTS: $\overline{\text{SQETST}}$ Pin

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Low Voltage Vil		VEE-0.3		VEE+0.8	V
Input High Voltage Vih		VEE+2.0 or pin open		VCC+0.3	V
Input Low Current	Vil = VEE + 0.4 V	+0.05		-0.4	mA
Input High Current	Vih = VEE + 2.4 V			100	µA

TRANSMITTER TO COAX

Input Capacitance CTXT TXT Pin	f = 10 MHz Transmitter inactive				
	8.1< VCC - VEE < 9.9V			9.5	pF
	0 < VCC - VEE < 8.1V			11.0	pF
Input Resistance RTXT TXT Pin	V(TXT) = VCC - 4V, Transmitter inactive	1000			kΩ
Differential Input ZDO Impedance DO+ to DO- Pins	f = 10 MHz	1.6		5.6	kΩ
DO+/- Common Ricm Mode Input Resistance	DO+ tied to DO-	1.5		2.8	kΩ
DO+/- Common Vicm Mode Output Voltage	DO+/- open	VEE+3.0		VEE+5.0	V
DO+/- Input Iidl & Current Iidh	VEE < V(DO+/-) <VCC, DO+ tied to DO-	-5		7	mA
Output Leakage IBTXT Current on TXT Pin	Transmitter Inactive	-0.5		+5.0	µA
TXT Output High VH Voltage	25 Ω TXT pin to VCC	VCC-.425		VCC	V
TXT Output Low VL Voltage	25 Ω TXT pin to VCC	VCC-2.200		VCC-1.625	V
TXT Differential VTXTHL Output Voltage	VTXTHL = VH-VL, 25 Ω TXT pin to VCC	1.400		2.200	V
TXT Average VTXTOFF Output Voltage	VTXTOFF = (VH+VL)/2 25 Ω TXT pin to VCC	VCC -1.125	VCC -1.00	VCC -.925	V
Differential Input VIDC Squelch Threshold	V(DO+)-V(DO-)	175	225	275	mVp
TXT Output Current tTXTR, Rise/Fall Time tTXTF	f = 5 and 10 MHz	20		30	ns

ELECTRICAL SPECIFICATIONS

TRANSMITTER TO COAX (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Difference In Driver Rise vs. Fall Times tTDRF	|tTXTR - tTXTF| f = 5 and 10 MHz		0.5	2	ns
Transmitter Turn On Delay tTON	f = 10 MHz 1 Bit = 100 ns			2	Bits
DO+/- Input Pulse Width to Stay On tPWSON				105	ns
DO+/- Input Pulse Width to Turn Off tPWOFF		200			ns
Transmit Static Delay tTSDR, tTSDF	f = 10 MHz		36	50	ns
Transmit Output Current Data tTSKEW	tTSKEW =tTSDR - tTSDF f = 5 and 10 MHz	-2.0		+2.0	ns
Jabber Control Time tJCT		20	30	35	ms
Jabber Reset Time tJRT		0.31	0.42	0.50	s
Jabber Recovery Time tJREC	Minimum gap between transmitted packets to prevent jabber activation	1.0			µs
TXT Output Current Pulse Harmonic Content f2,f3HA	f = 10 MHz, on specified board with 47 pF capacitor between TXT and GND 2nd, 3rd, Harmonics			-20	dB
f4, f5HA	4th, 5th Harmonics			-30	dB
f6,f7HA	6th, 7th Harmonics			-40	dB
f8HA	All Higher Harmonics			-50	dB

RECEIVER FROM COAX

Input Capacitance RXT Pin CRXT	20-pin PLCC		1.3	1.85	pF
Input Resistance RXT Pin RRXT	V(RXT) = VCC - 1.5V	120			kΩ
Input Bias Current RXT Pin IBRXT		-1.5		+20	µA
Receiver Carrier Sense Threshold (measured at coax) VCAT1	VCAT1 = VCC - V(RXTL), f = 5 MHz, V(RXTH) = VCC	400		800	mVp

RECEIVER FROM COAX (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Receiver Hysteresis (measured at coax)	VCAT2	VCAT2 = [V(RXTH)- V(RXTL)]/2 f = 5 MHz, [V(RXTH)+ V(RXTL)]/2 = VCC -1V			100	mVp
Receiver Turn-Off Holding Time	tROFF		200		1000	ns
Receiver Static Delay	tRSDR, tRSDF	f = 10 MHz		20	50	ns
Receiver Turn-On Delay	tRON	f = 10 MHz 1 Bit = 100 ns VLAT > VCC-600 mV		2	5	Bits
Receiver Output Data Symmetry	tRSKEW	tRSKEW = tRSDR -tRSDF f = 5 and 10 MHz, after first 2 µS from the input beginning packet	-2		2	ns

COLLISION DETECT CIRCUIT

With $\overline{SQETST}$ set high the collision detect output is enabled when a collision is detected on the coax and for jabber timeout. With $\overline{SQETST}$ set low the collision detect output is also enabled at the end of every transmission to the coax.

Collision Sense Threshold	VCOT	COLADJ pin to VEE (for 10BASE5)	VCC -1.492		VCC -1.629	V
		COLADJ pin open (for 10BASE2)	VCC -1.404		VCC -1.581	V
Collision Output Turn-On Delay	tCON			600	900	ns
Collision Reset Time	tCOFF				2000	ns
Collision Output Frequency	fCL	fCL= 1/(Tcl + Tch) 78Q8330A	8.5		11.5	MHz
		78Q8330	8.5		12.5	MHz
Collision Output Duty Cycle	tCOL	$tCOL = \frac{tch}{tch + tcl}$	40		60	%
Collision Detect Test Delay Time	tSTD		0.6		1.5	µs
Collision Detect Test Length	tSTL	1 Bit = 100ns	5	8	15	Bits
Collision Detect Test Holding Time	tHLD		200		1000	ns

ELECTRICAL SPECIFICATIONS

DI+/- AND CI+/- OUTPUT DRIVERS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Differential Output Voltage	VODC	V(CI+) - V(CI-), V(DI+) - V(DI-), RI = 78 Ω	±550		±850	mVp
CI+/- Common Mode Output Voltage	Vcmt1	Output active or idle, VBIAS = (VCC + VEE)/2 ± 5%	VBIAS -1.7		VBIAS - 0.5	V
DI+/- Common Mode Output Voltage	Vcmt2	Output active or idle	VCC-1.7		VCC-0.5	V
DI+/- or CI+/- Differential Output Voltage Imbalance	Vodi	Output active		±5	±20	mV
DI+/- or CI+/- Differential Output Idle Voltage	Vod Off	Output idle	-20		+20	mV
DI+/- or CI+/- Rise Time	tRR	20-80%, RI = 78			5	ns
DI+/- or CI+/- Fall Time	tRF	80-20%, RI = 78			5	ns

TEST MODE

The following test modes are entered by setting the voltage of the TEST pin:

1. Normal mode
2. tJRT and tJCT reduced by factor of 32
3. Activate transmitter and receiver, deactivate jabber and collision detect

TEST Pin Voltage	Mode 1		Pin Open		
	Mode 2	VEE+2.5		VEE+3.5	V
	Mode 3	VEE		VEE+0.2	V

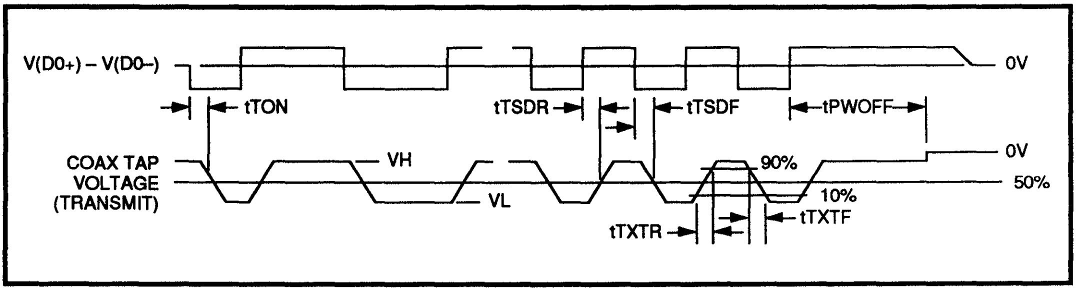


FIGURE 2 : Transmit Function

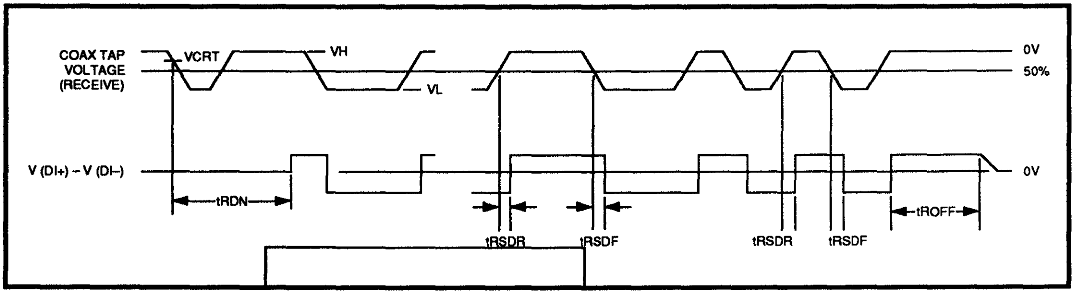


FIGURE 3: Receive Function

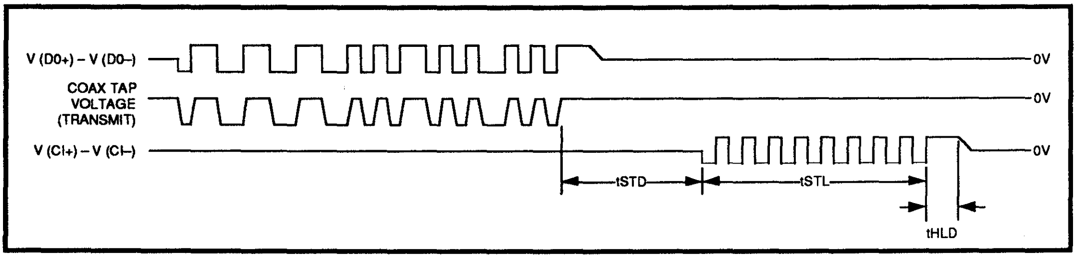


FIGURE 4: SQE Test

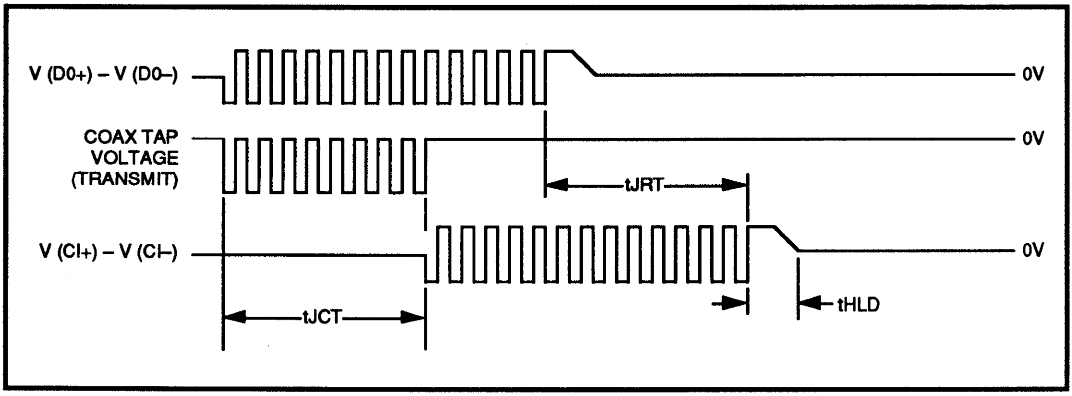


FIGURE 5: Jabber Function

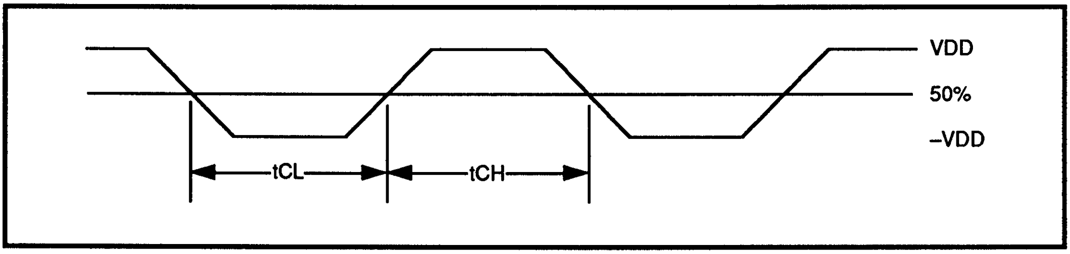


FIGURE 6 : CI± Parameters

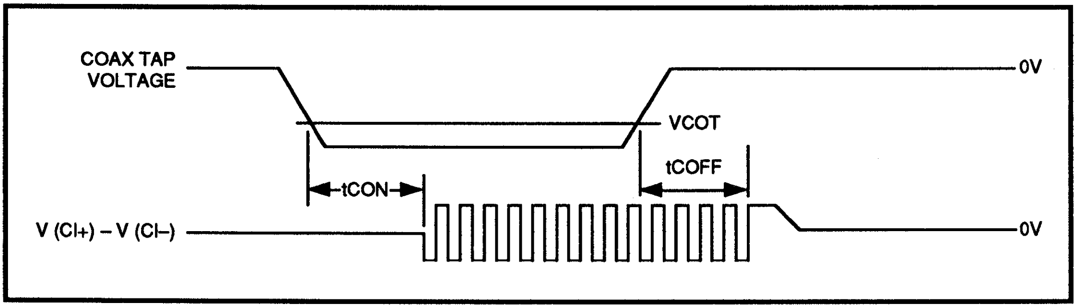
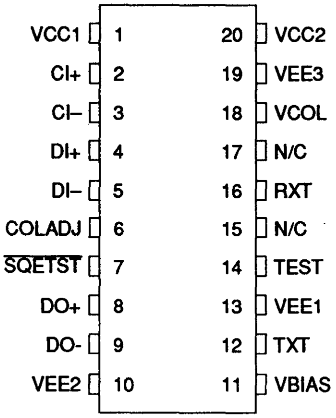


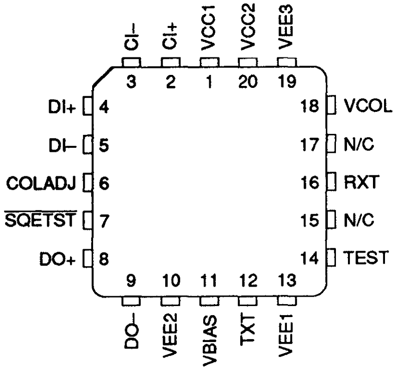
FIGURE 7: Collision Detect Timing

PACKAGE PIN DESIGNATIONS

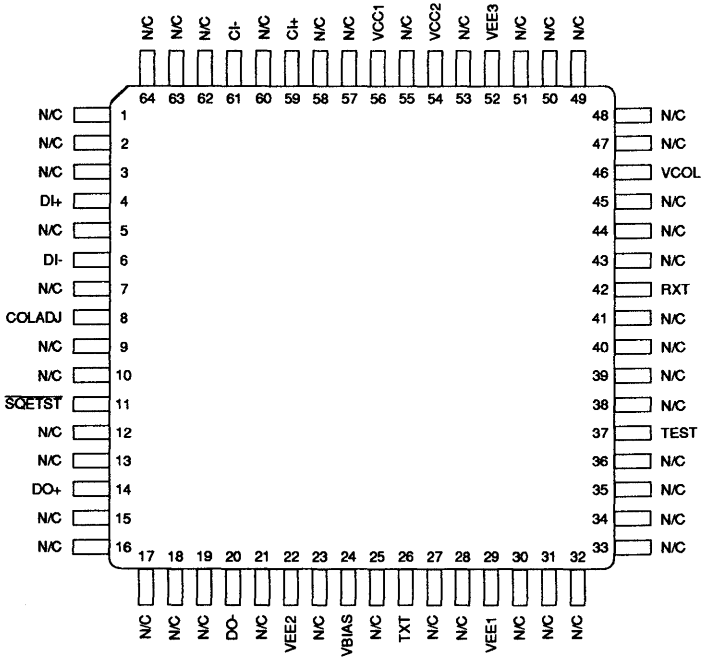
(Top View)



20-Pin DIP



20-Pin PLCC



64-Lead TQFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 78Q8330		
20-Pin Plastic DIP	78Q8330-CP	78Q8330-CP
20-Pin PLCC	78Q8330-CH	78Q8330-CH
64-Lead TQFP	78Q8330-CGT	78Q8330-CGT
SSI 78Q8330A		
20-Pin Plastic DIP	78Q8330A-CP	78Q8330A-CP
20-Pin PLCC	78Q8330A-CH	78Q8330A-CH
64-Lead TQFP	78Q8330A-CGT	78Q8330A-CGT

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914

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SSI 78Q8360
Ethernet Controller/ ENDEC Combo

Preliminary Data

December 1992

DESCRIPTION

The SSI 78Q8360 is a combination Media Access Controller (MAC) and 10 Mbit/s Manchester encoder/ decoder (ENDEC) with Attachment Unit Interface (AUI) for IEEE 802.3 applications. It is connected to the transmission medium through the AUI with a transceiver circuit such as the SSI 78Q8330 Ethernet Coax Transceiver or the 78Q902 10BaseT Transceiver. Connection to the host is accomplished via external bus decoding logic.

An intelligent Buffer Manager is controlled by the host read, host write, receive and transmit pointers, and the 8360 manages the pointers internally without any host intervention. The 8360 interleaves access to the buffer memory so that accesses from the host and from the network media seem to operate concurrently.

The 8360 has a sophisticated power management capability with three different operating modes allowing the user to maximize power savings. Interface with the host can be accomplished in several different ways: memory mapping, I/O mapping, programmable DMA or a combination of these. Big and little endian byte orderings make for simple bus interface to all standard microprocessors. The 78Q8360 is packaged in a 100-pin QFP or TQFP and uses a single 5V supply.

FEATURES

- **IEEE 802.3 and Ethernet 2.0 compliant**
- **Power management options include:**
  - **Intelligent power mode automatically shuts off unused circuitry**
  - **Standby mode reduces power while not in operation**
  - **Full power-down mode offers maximum power savings**
- **Advanced Buffer Manager architecture:**
  - **Automatic management of all pointers**
  - **Allows "simultaneous" access to data in buffer memory by both the network and host**
  - **High-speed received packet skip**
- **Configurable Buffer Memory for design flexibility:**
  - **Two-bank transmit buffer in 2, 4, 8, or 16 Kbyte sizes**
  - **Ring-structure receive buffer from 4 to 62 Kbytes**
- **Software-configurable system bus structure:**
  - **Compatible with major microprocessors**
  - **8- or 16-bit wide data path**
  - **Supports single and programmable burst DMA, I/O and interrupt operations**
- **Three different loopback modes**
- **Multicast address filtering via 64-element hash table**

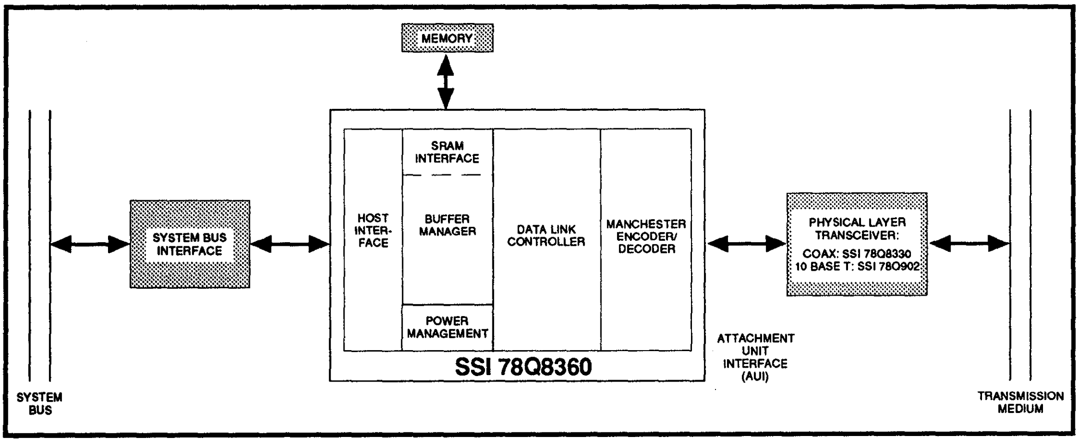


FIGURE 1: System Diagram

FUNCTIONAL DESCRIPTION

The 78Q8360 consists of five major blocks:

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- Host Interface
- Manchester ENDEC
- Power Management

A block diagram of the 78Q8360 is shown in Figure 2.

BUFFER MANAGER

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration, this makes the 8360 a high performance LAN controller.

The buffer memory is divided into two portions: transmit memory portion and receive memory portion. The transmit memory portion can be partitioned into 2K, 4K, 8K or 16 Kbyte buffer sizes. There is only one transmit bank if a 2 KB transmit buffer size is selected. If the transmit buffer size is greater than 2 KB, then the transmit buffer is configured into two banks of equal size. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be transmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62 KB depending on the buffer memory configuration which has a range of 8K to 64 KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from 4 sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the 8360 will assert a 'not ready' handshake to the host while servicing the Transmitter and/or Receiver. The 8360 arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operation appears to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the 8360 can potentially be receiving data from the medium and loading it into the receive buffer (if the 8360 is in a loop back mode or if self-reception occurs).

DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ANSI/IEEE 8802-3 CSMA/CD protocol. It consists of a Transmitter, a Receiver and CRC logic (which is shared by both transmit and receive operations). Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

HOST INTERFACE

The Host Interface (HIF) provides connection to the host system. It consists of the various registers, DMA circuits and ready logic. Both word and byte interfaces are supported as well as big endian and little endian data ordering. Host access to the buffer memory is through BMR8 (and BMR9). Reading from BMR8 will read a byte or word from the receive buffer and writing to BMR8 will write a byte or word to the transmit buffer. The ready logic is capable of delaying host access to the buffer memory with a time-out mechanism. Both single and burst DMA transfer modes are supported.

MANCHESTER ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to TDP and TDN outputs through the Attachment Unit Interface (AUI) driver. The decoder section performs three functions on the data received at RDP and RDN: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at the end of reception and during idle to save power. Jitter of up to 20 nsec can be tolerated by the decoder. Collisions detected at the transceiver are presented as a 10 MHz signal at CDP and CDN and are then converted to a logic level signal and passed to the DLC.

POWER MANAGEMENT

One very useful and important feature that the 8360 offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

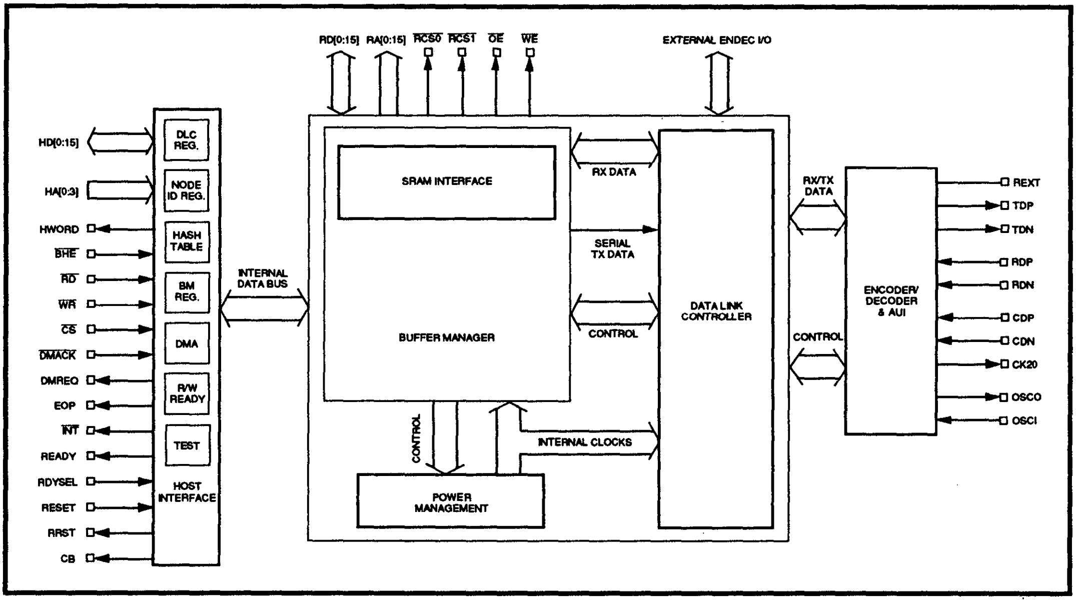


FIGURE 2: 78Q8360 Block Diagram

SSI 78Q8360
Ethernet Controller/
ENDEC Combo

PIN ASSIGNMENT TABLE – 100-Pin QFP

PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE
1	HD11	IO8U	26	DMREQ	O16	51	$\overline{\text{RCS0}}$	O4	76	OSCI	I^2
2	HD10	IO8U	27	$\overline{\text{DMACK}}$	I	52	$\overline{\text{RCS1}}$	O4	77	OSCO	O^2
3	VDD	P	28	VDD	P	53	VDD	P	78	AVDD	P
4	GND	P	29	$\overline{\text{RD}}$	I	54	RA0	O4	79	AGND	P
5	HD9	IO8U	30	$\overline{\text{WR}}$	I	55	RA1	O4	80	TXC	IO4U
6	HD8	IO8U	31	RESET	I^1	56	RA2	O4	81	RDN	AI
7	$\overline{\text{CS}}$	I	32	RD0	IO4U	57	RA3	O4	82	RDP	AI
8	$\overline{\text{BHE}}$	I	33	RD1	IO4U	58	RA4	O4	83	CDN	AI
9	HWORD	O4	34	RD2	IO4U	59	RA5	O4	84	CDP	AI
10	HA0	I	35	RD3	IO4U	60	RA6	O4	85	VDD	P
11	HA1	I	36	RD4	IO4U	61	RA7	O4	86	LOOP	IO4U
12	HA2	I	37	RD5	IO4U	62	RA8	O4	87	REXT	$-^3$
13	HA3	I	38	RD6	IO4U	63	RA9	O4	88	RXC	IO4U
14	READY	O4	39	RD7	IO4U	64	RA10	O4	89	CK20	O2
15	GND	P	40	GND	P	65	GND	P	90	GND	P
16	HD0	IO8	41	RD8	IO4U	66	RA11	O4	91	RXD	IO4U
17	HD1	IO8	42	RD9	IO4U	67	RA12	O4	92	COL	IO4U
18	HD2	IO8	43	RD10	IO4U	68	RA13	O4	93	CRS	IO4U
19	HD3	IO8	44	RD11	IO4U	69	RA14	O4	94	RDYSEL	I
20	HD4	IO8	45	RD12	IO4U	70	RA15	O4	95	CB	O4
21	HD5	IO8	46	RD13	IO4U	71	TXE	IO4U	96	RRST	O4
22	HD6	IO8	47	RD14	IO4U	72	TXD	IO4U	97	HD15	IO8U
23	HD7	IO8	48	RD15	IO4U	73	GND	P	98	HD14	IO8U
24	EOP	I	49	$\overline{\text{OE}}$	O4	74	TDN	AO	99	HD13	IO8U
25	$\overline{\text{INT}}$	O4	50	$\overline{\text{WE}}$	O4	75	TDP	AO	100	HD12	IO8U

Legend:

I:	Input (TTL level)
On:	Output with IOL = n mA
IOn:	Input (TTL level) and Output with IOL = n mA
IOnU:	IOn with "controlled" internal pull-up resistor
AI:	Analog Input
AO:	Analog Output
P:	Power

Notes:

[1] RESET has a Schmitt trigger and a pull-down resistor.

[2] OSCI and OSCO have CMOS level.

[3] REXT is connected to a resistor and then to analog ground.

PIN ASSIGNMENT TABLE – 100-Pin TQFP

PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE	PIN #	PIN NAME	TYPE
1	GND	P	26	$\overline{RD}$	I	51	RA0	O4	76	AGND	P
2	HD9	IO8U	27	$\overline{WR}$	I	52	RA1	O4	77	TXC	IO4U
3	HD8	IO8U	28	RESET	I^1	53	RA2	O4	78	RDN	AI
4	$\overline{CS}$	I	29	RD0	IO4U	54	RA3	O4	79	RDP	AI
5	$\overline{BHE}$	I	30	RD1	IO4U	55	RA4	O4	80	CDN	AI
6	HWORD	O4	31	RD2	IO4U	56	RA5	O4	81	CDP	AI
7	HA0	I	32	RD3	IO4U	57	RA6	O4	82	VDD	P
8	HA1	I	33	RD4	IO4U	58	RA7	O4	83	LOOP	IO4U
9	HA2	I	34	RD5	IO4U	59	RA8	O4	84	REXT	$-^3$
10	HA3	I	35	RD6	IO4U	60	RA9	O4	85	RXC	IO4U
11	READY	O4	36	RD7	IO4U	61	RA10	O4	86	CK20	O2
12	GND	P	37	GND	P	62	GND	P	87	GND	P
13	HD0	IO8	38	RD8	IO4U	63	RA11	O4	88	RXD	IO4U
14	HD1	IO8	39	RD9	IO4U	64	RA12	O4	89	COL	IO4U
15	HD2	IO8	40	RD10	IO4U	65	RA13	O4	90	CRS	IO4U
16	HD3	IO8	41	RD11	IO4U	66	RA14	O4	91	RDYSEL	I
17	HD4	IO8	42	RD12	IO4U	67	RA15	O4	92	CB	O4
18	HD5	IO8	43	RD13	IO4U	68	TXE	IO4U	93	RRST	O4
19	HD6	IO8	44	RD14	IO4U	69	TXD	IO4U	94	HD15	IO8U
20	HD7	IO8	45	RD15	IO4U	70	GND	P	95	HD14	IO8U
21	EOP	I	46	$\overline{OE}$	O4	71	TDN	AO	96	HD13	IO8U
22	$\overline{INT}$	O4	47	$\overline{WE}$	O4	72	TDP	AO	97	HD12	IO8U
23	DMREQ	O16	48	$\overline{RCS0}$	O4	73	OSCI	I^2	98	HD11	IO8U
24	$\overline{DMACK}$	I	49	$\overline{RCS1}$	O4	74	OSCO	O^2	99	HD10	IO8U
25	VDD	P	50	VDD	P	75	AVDD	P	100	VDD	P

Legend:

I:	Input (TTL level)
On:	Output with IOL = n mA
IOn:	Input (TTL level) and Output with IOL = n mA
IOnU:	IOn with "controlled" internal pull-up resistor
AI:	Analog Input
AO:	Analog Output
P:	Power

Notes:

[1] RESET has a Schmitt trigger and a pull-down resistor.

[2] OSCI and OSCO have CMOS level.

[3] REXT is connected to a resistor and then to analog ground.

PIN DESCRIPTION

HOST BUS INTERFACE

<table>
<tr><th>NAME</th><th>TYPE</th><th colspan="4">DESCRIPTION</th></tr>
<tr><td>RESET</td><td>I</td><td colspan="4">HARDWARE RESET. Active high. A minimum pulse length of 200 ns is required. This pin resets the 8360's internal pointers and registers to their appropriate states. NB: the 8360 must be reset after power on before usage.</td></tr>
<tr><td>READY</td><td>O</td><td colspan="4">READY. This output is asserted to indicate to the host that the 8360 is ready to complete the requested read or write operation. It will also be used if the device is unable to respond to read or write requests within 2.4 µs. In these situations, the 8360 will also assert $\overline{INT}$ and the host read error status bit (DLCR1 <6>) or host write error status bit (DLCR0 <0>). The polarity of the READY pin is determined by RDYSEL.</td></tr>
<tr><td>RDYSEL</td><td>I</td><td colspan="4">READY POLARITY SELECT. Control input to select the polarity of the READY pin. When RDYSEL is a '1', READY will be active high. If RDYSEL is a '0', READY will be an active low signal.</td></tr>
<tr><td>$\overline{WR}$</td><td>I</td><td colspan="4">WRITE. The $\overline{WR}$ pin is an active low input that enables a write operation from the host to the 8360's internal registers as selected by the host address inputs HA[0:3].</td></tr>
<tr><td>$\overline{RD}$</td><td>I</td><td colspan="4">READ. The $\overline{RD}$ pin is an active low input that enables a read operation by the host from the 8360's internal registers as selected by the host address inputs HA[0:3].</td></tr>
<tr><td>$\overline{CS}$</td><td>I</td><td colspan="4">CHIP SELECT. An active low input signal as the chip select for the 8360.</td></tr>
<tr><td rowspan="7">$\overline{BHE}$</td><td rowspan="7">I</td><td colspan="4">BYTE HIGH ENABLE. This is an active low byte/word control pin used only when the 8360 is configured for word transfer by HBYTE bit (DLCR6 <5>). Combinations of $\overline{BHE}$ and HA0 are used to select word, upper byte only or lower byte only transfers.</td></tr>
<tr><td>HBYTE</td><td>$\overline{BHE}$</td><td>HA0</td><td>FUNCTION</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Word transfer</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Byte transfer on high bus HD[8:15].</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Byte transfer on low bus HD[0:7].</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>X</td><td>X</td><td>Byte transfer (HD[0:7])</td></tr>
<tr><td>$\overline{INT}$</td><td>O</td><td colspan="4">INTERRUPT. This active low signal is asserted when the 8360 requires the intervention of the Host in the situations as depicted in DLCR0&1. The $\overline{INT}$ signal is masked by writing a '0' to the interrupt enable register.</td></tr>
<tr><td>EOP</td><td>I</td><td colspan="4">END OF PROCESS. Asserted at the end of a DMA transfer by the Host DMA controller. Further DMA requests (DMREQ) will be discontinued after EOP is asserted. Polarity can be selected via register bit (DLCR7 <1>).</td></tr>
<tr><td>DMREQ</td><td>O</td><td colspan="4">DMA REQUEST. The 8360 issues a DMREQ to the Host DMA controller to initiate a write to its transmit buffer or a read from its receive buffer.</td></tr>
</table>

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{DMACK}}$	I	DMA ACKNOWLEDGE. An active low signal issued by the Host DMA controller when it is ready to perform data transfers between the Host and the 8360's buffer memory via BMR8.
HA[0:3]	I	HOST ADDRESS. Selects the set of internal registers to be accessible by the 8360 for read or write operations.
HD[0:15]	I/O	HOST DATA BUS. A bi-directional, tri-state bus for data, command and status transfers between the Host and the 8360 with the direction being controlled by $\overline{\text{RD}}$ and $\overline{\text{WR}}$. The combinations of HBYTE, $\overline{\text{BHE}}$ and HA0 control the portion of the bus that is being utilized. HA[0:3] and RBNK <0:1> (DLCR7 <2:3>) select the set of internal registers for access.
HWORD	O	HOST WORD CONFIGURATION. This pin is the complement of the register bit HBYTE (DLCR6 <5>). If HBYTE is a '0', the Host interface is configured for word transfers. If HBYTE is a '1', the Host interface is configured for byte transfers on the lower bus, HD[0:7].

BUFFER MEMORY INTERFACE

$\overline{\text{RCS0}}$, $\overline{\text{RCS1}}$	O	RAM CHIP SELECT. $\overline{\text{RCS0}}$ and $\overline{\text{RCS1}}$ are active low chip select lines for the SRAM with $\overline{\text{RCS0}}$ as the least significant byte.
$\overline{\text{OE}}$	O	RAM OUTPUT ENABLE. Active low. This is the output enable asserted by the 8360 during buffer memory read cycles for the SRAM.
$\overline{\text{WE}}$	O	RAM WRITE ENABLE. Active low. This is the write enable asserted by the 8360 during buffer memory write cycles for the SRAM.
RD[0:15]	I/O	RAM DATA BUS. This is the data bus between the 8360 and the buffer memory. It can be configured for byte or word transfer depending on register bit RBYTE (DLCR6 <4>) RAM BYTE. For word transfers, the ordering of the most and least significant byte is defined by the register bit, INTLMOT (DLCR7 <0>).
RA[0:15]	O	RAM ADDRESS BUS. Addresses up to 64 KByte of SRAM buffer memory.

NETWORK INTERFACE

TDN, TDP	O	TRANSMIT DATA NEGATIVE and POSITIVE. Differential outputs to the transceiver for transmission.
RDN, RDP	I	RECEIVE DATA NEGATIVE and POSITIVE. Manchester differential inputs from the transceiver for reception.
CDN, CDP	I	COLLISION DETECT NEGATIVE and POSITIVE. When the transceiver detects a collision on the media, these differential inputs are driven by a 10 MHz signal.
REXT	-	EXTERNAL RESISTOR. External biasing resistor for the Attachment Unit Interface (AUI).

EXTERNAL ENCODER/DECODER INTERFACE

The following eight pins are provided for connection to an external encoder/decoder in the optional mode of using an external encoder/decoder with the 78Q8360. They are also used as monitor pins for test purposes. In normal network interface applications these pins are not used and are pulled-up internally. Optional modes of configuration are determined by the EEDCNTL <1:0> register bits DLCR7<7:6>.

CONTROLLER-ENCODER/DECODER INTERFACE

NAME	TYPE	DESCRIPTION
TXD	I/O	TRANSMIT DATA. Normally not used. (Non-Return to Zero) NRZ transmit serial data.
TXC	I/O	TRANSMIT CLOCK. Normally not used. A synchronous 10 MHz clock with the serially transmitted data, TXD.
TXE	I/O	TRANSMIT ENABLE. Normally not used. Enable for transmission.
COL	I/O	COLLISION. Normally not used. Active high collision signal.
LOOP	I/O	LOOP BACK. Normally not used. ENDEC loop back test signal.
RXD	I/O	RECEIVE DATA. Normally not used. NRZ serial receive data.
RXC	I/O	RECEIVE CLOCK. Normally not used. A synchronous 10 MHz recovered clock with the serially received data, RXD.
CRS	I/O	CARRIER SENSE. Normally not used. When asserted high, it signifies that a carrier is active in the media.

ENCODER/DECODER PIN INPUT/OUTPUT TABLE

<table>
<tr><th>EEDCNTL <1:0></th><th>MODE</th><th>TXD</th><th>TXC</th><th>TXE</th><th>LOOP</th><th>RXD</th><th>RXC</th><th>CRS</th><th>COL</th></tr>
<tr><td rowspan="2">00</td><td>Normal</td><td colspan="8">On-chip internal ENDEC is used with the 8360</td></tr>
<tr><td>78Q8360</td><td>ZU</td><td>ZU</td><td>ZU</td><td>ZU</td><td>ZU</td><td>ZU</td><td>ZU</td><td>ZU</td></tr>
<tr><td rowspan="2">01</td><td>78Q8360</td><td colspan="8">On-chip internal ENDEC is used with the 8360</td></tr>
<tr><td>Monitor</td><td>O</td><td>O</td><td>O</td><td>O</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
<tr><td rowspan="2">10</td><td>External</td><td colspan="8">External ENDEC is used with the 8360, internal ENDEC is off</td></tr>
<tr><td>ENDEC</td><td>O</td><td>I</td><td>O</td><td>O</td><td>I</td><td>I</td><td>I</td><td>I</td></tr>
<tr><td rowspan="2">11</td><td>ENDEC</td><td colspan="8">On-chip internal ENDEC is used only, the 8360 controller is off</td></tr>
<tr><td>Test</td><td>I</td><td>O</td><td>I</td><td>I</td><td>O</td><td>O</td><td>O</td><td>O</td></tr>
</table>

ZU: High impedance with internal pull-up

PIN DESCRIPTION (continued)

DEVICE POWER

NAME	TYPE	DESCRIPTION
VDD	P	POWER SUPPLY. A +5V DC (±5%) supply is required.
GND	P	SYSTEM GROUND.
AVDD	P	ANALOG VDD. The analog VDD pin required by the internal encoder/decoder is to be connected to a different VDD path from the digital VDD. A +5V DC (±5%) supply is required.
AGND	P	ANALOG GROUND. The analog ground required by the internal encoder/ decoder is to be connected to a separate GND path from the digital GND.

CRYSTAL OSCILLATOR

OSCI	I	OSCILLATOR IN. Connection for one side of the 20 MHz crystal or an input for an external 20 MHz clock source.
OSCO	O	OSCILLATOR OUT. Connection for other side of the 20 MHz crystal. Left unconnected if an external clock is used.

MISCELLANEOUS

CB	O	CONTROL BIT. A complement of the internal register bit, DLCR4 <2>, which is used to activate any external hardware.
RRST	O	REMOTE RESET. This pin follows the RMTRST register bit (DLCR1 <4>). The RMTRST bit is '1' only if a packet with the pattern 0900H in the Type Field is detected and ENA_RMTRST (DLCR5 <2>) is activated. This feature can be used by the nodes on the network to remotely-control external hardware.
CK20	O	20 MHz CLOCK: A 20 MHz free-running buffered clock output provided by the crystal oscillator circuit.

CONTROL AND STATUS REGISTERS

The registers in the 8360 can be divided into 5 groups: the Data Link Control Registers (DLCR0-7), Node ID registers (IDR8-13), Time Domain Reflectometry Registers (TDR14-15), Hash Table Registers (HTR8-15) and Buffer Memory Registers (BMR8-15).

The Data Link Control Registers contain the transmit and receive status information, interrupt enable, 8360 setup and software reset bit (DLCR6<7>). They are accessed through direct register addresses xxx0H through xxx7H. The Ethernet Node ID is stored in IDR 8-15. The TDR14-15 registers are used to provide the count value of the number of bits transmitted for each packet. This value can indicate whether a packet has completed its transmission or has encountered a collision. Both the Node ID and the Time Domain Reflectometry Registers can be accessed through direct register addresses xxx8H through xxxFH.

The Hash Table Registers (HTR8-15) provide a means for filtering incoming multicast packets. Any packet that does not match the hash table coding will be rejected. The HTR8-15 can be accessed by the bank-switching addresses RBNK<1:0> (DLCR7 <3:2>).

The final group of the registers belongs to the Buffer Memory Registers (BMR8-15). The tasks performed by these registers include transferring of packets between the host and the 8360 (via BMR8-9), collision control, DMA operations and activation of the transmit operation. A summary table of the registers and their addresses are tabulated below:

RBNK<1:0>	HA3	HA2	HA1	HA0	ADDRESS	DESCRIPTION
XX	0	0	0	0	DLCR0	Transmit Status
XX	0	0	0	1	DLCR1	Receive Status
XX	0	0	1	0	DLCR2	Transmit Interrupt Mask
XX	0	0	1	1	DLCR3	Receive Interrupt Mask
XX	0	1	0	0	DLCR4	Transmit Mode
XX	0	1	0	1	DLCR5	Receive Mode
XX	0	1	1	0	DLCR6	Configuration 1
XX	o	1	1	1	DLCR7	Configuration 2
00	1	0	0	0	IDR8	NODE ID 0
00	1	0	0	1	IDR9	NODE ID 1
00	1	0	1	0	IDR 10	NODE ID 2
00	1	0	1	1	IDR11	NODE ID 3
00	1	1	0	0	IDR12	NODE ID 4
00	1	1	0	1	IDR13	NODE ID 5
00	1	1	1	0	TDR14	TDR 0 (LSB)
00	1	1	1	1	TDR15	TDR 1 (MSB)

CONTROL AND STATUS REGISTERS (continued)

RBNK<1:0>	HA3	HA2	HA1	HA0	ADDRESS	DESCRIPTION
01	1	0	0	0	HTR8	Hash Table 0
01	1	0	0	1	HTR9	Hash Table 1
01	1	0	1	0	HTR10	Hash Table 2
01	1	0	1	1	HTR11	Hash Table 3
01	1	1	0	0	HTR12	Hash Table 4
01	1	1	0	1	HTR13	Hash Table 5
01	1	1	1	0	HTR14	Hash Table 6
01	1	1	1	1	HTR15	Hash Table 7
10	1	0	0	0	BMR8	Buffer Memory I/O Port
10	1	0	0	1	BMR9	Buffer Memory I/O Port (word mode)
10	1	0	1	0	BMR10	Transmit Start + Packet Count
10	1	0	1	1	BMR11	16 Collisions Control
10	1	1	0	0	BMR12	DMA Enable
10	1	1	0	1	BMR13	DMA Burst
10	1	1	1	0	BMR14	Skip Packet
10	1	1	1	1	BMR15	Reserved
11	X	X	X	X	-	RESERVED

Note: All registers are both word and byte accessible. In word mode, register bytes are paired up. IDR and HTR can only be accessed when $\overline{\text{ENADLC}}$ (DLCR 6<7>) is a '1'. In byte mode, only BMR8 will be used.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Supply voltage, V_{DD}	-0.5 to 6.0V
Input voltage, V_{IN}	-0.5 to V_{DD} + 0.5V
Output voltage, V_{OUT}	-0.5 to V_{DD} + 0.5V
Storage temperature, T_{STG}	-55 to 150°C
Lead temperature (max 10 sec soldering), T_L	250°C max

DC CHARACTERISTICS

(TA = 0°C to +70°C, V_{DD} = 5V ± 5%)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Low level input voltage	V_{IL}	TTL inputs	0		0.8	V
		OSCI pin	0		1.4	V
		RESET pin	0		1.2	V
High level input voltage	V_{IH}	TTL inputs	2.0		V_{DD}	V
		OSCI pin	3.2		V_{DD}	V
		RESET pin	1.8		V_{DD}	V
Low level output voltage	V_{OL}	Rated I_{OL}	0		0.4	V
		$I_{OL} = 20\ \mu A$	0		0.1	V
High level output voltage	V_{OH}	Rated I_{OH}	2.4		V_{DD}	V
		$I_{OH} = -20\ \mu A$	V_{DD} - 0.1		V_{DD}	V
Low level output current (1) (pin types On, IOn and IOnU)	I_{OL}	V_{OL} = 0.4V	n			mA
High level output current (1) (pin types On, IOn and IOnU)	I_{OH}	V_{OH} = 2.4V	-n			mA
Leakage current (input/output)	I_L		-10		10	µA
Supply current (2)	I_{DD}	Fully active			50	mA
		Idle			25	mA
Power down supply current (2)	I_{PWRDN}	Osc. on			5	mA
		Osc. off			1	mA

Note: (1) "n" refers to the rated output current and takes the value of 2, 4, 8, 16 depending on the pins.
(2) Inputs at VCC or GND. Fully active means 3 "simultaneous" operations: transmitting, receiving and either host write or read.

ELECTRICAL SPECIFICATIONS (continued)

AUI CHARACTERISITICS

(TA = 0 to 70 °C, VDD = 5V ±5%)
Input refers to RDP, N and CDP, N. Output refers to TDP, N.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
AC Common Mode Output Voltage V_{ACCM}				±40	mV
DC Common Mode Output Voltage V_{DCCM}		3.0	4.0	V_{DD}- 0.5	V
Differential Peak Output Voltage V_{OP}	R_{EXT} = 20 kΩ R_T = 78Ω	0.7	0.9	1.1	V
Output Current I_{OP}	R_{EXT} = 20 kΩ	9	11	13	mA
Input Squelch Threshold Voltage V_{SQ}		-140	-190	-260	mV
Open Circuit Input Bias Voltage V_{BIAS}		2.5	3.5	V_{DD}- 0.5	V

CAPACITANCE

Input pin capacitance C_{IN}				10	pF
Output pin capacitance C_{OUT}				10	pF
I/O pin capacitance C_{IO}				10	pF

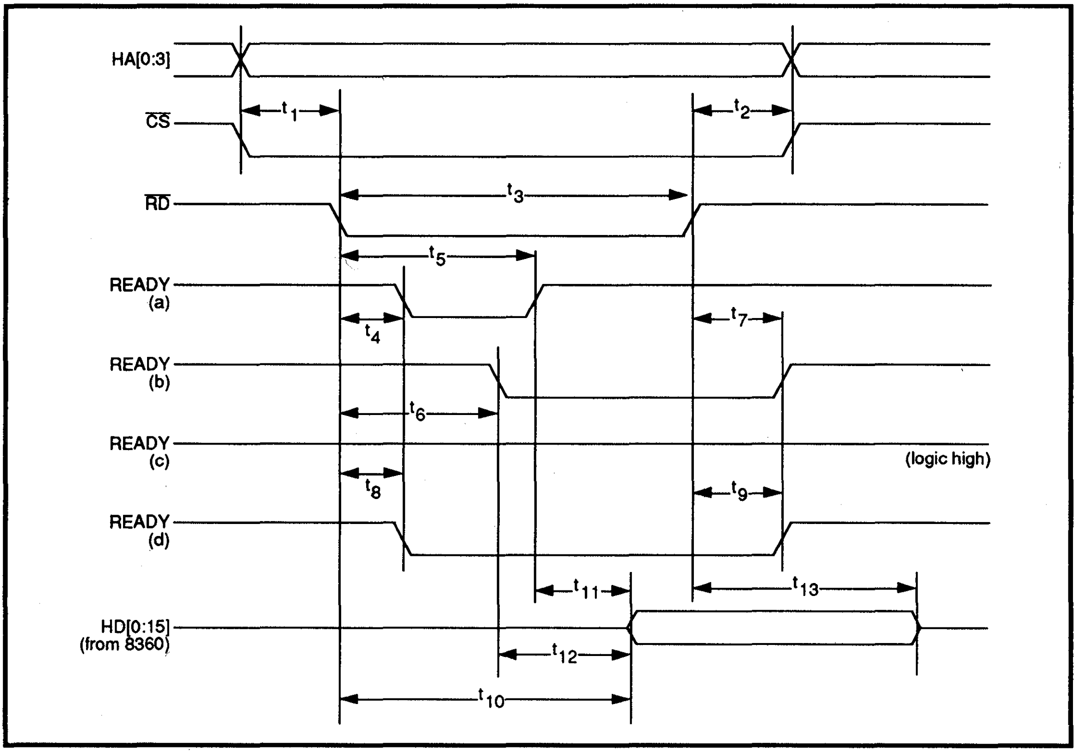


FIGURE 3: Read Cycle

TABLE 1: Read Cycle

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{\text{CS}}$ low to $\overline{\text{RD}}$ low; HA[0:3] valid to $\overline{\text{RD}}$ low t_1		0			ns
$\overline{\text{RD}}$ high to $\overline{\text{CS}}$ high; $\overline{\text{RD}}$ high to HA[0:3] invalid t_2		0			ns
$\overline{\text{RD}}$ low pulse width t_3		30			ns
$\overline{\text{RD}}$ low to READY low t_4	(a)	0		35	ns
$\overline{\text{RD}}$ low to READY high (1) t_5	(a)			400	ns
$\overline{\text{RD}}$ low to READY low (1) t_6	(b)	0		400	ns
$\overline{\text{RD}}$ high to READY high t_7	(b)	0		25	ns
$\overline{\text{RD}}$ low to READY low t_8	(d)	0		25	ns
$\overline{\text{RD}}$ high to READY high t_9	(d)	0		25	ns
$\overline{\text{RD}}$ low to HD[0:15] valid t_{10}	Register access			45	ns
READY high to HD[0:15] validt_{11}	Port access			0	ns
READY low to HD[0:15] valid t_{12}	Port access			0	ns
$\overline{\text{RD}}$ high to HD[0:15] invalid (data hold) t_{13}		10			ns

Note: (1) Maximum of 400 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active in "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host read error.

(a) For Buffer Memory Port when port is busy and RDYSEL = 1.
(b) For Buffer Memory Port when port is busy and RDYSEL = 0.
(c) For register or port is not busy and RDYSEL = 1.
(d) For register or port is not busy and RDYSEL = 0.

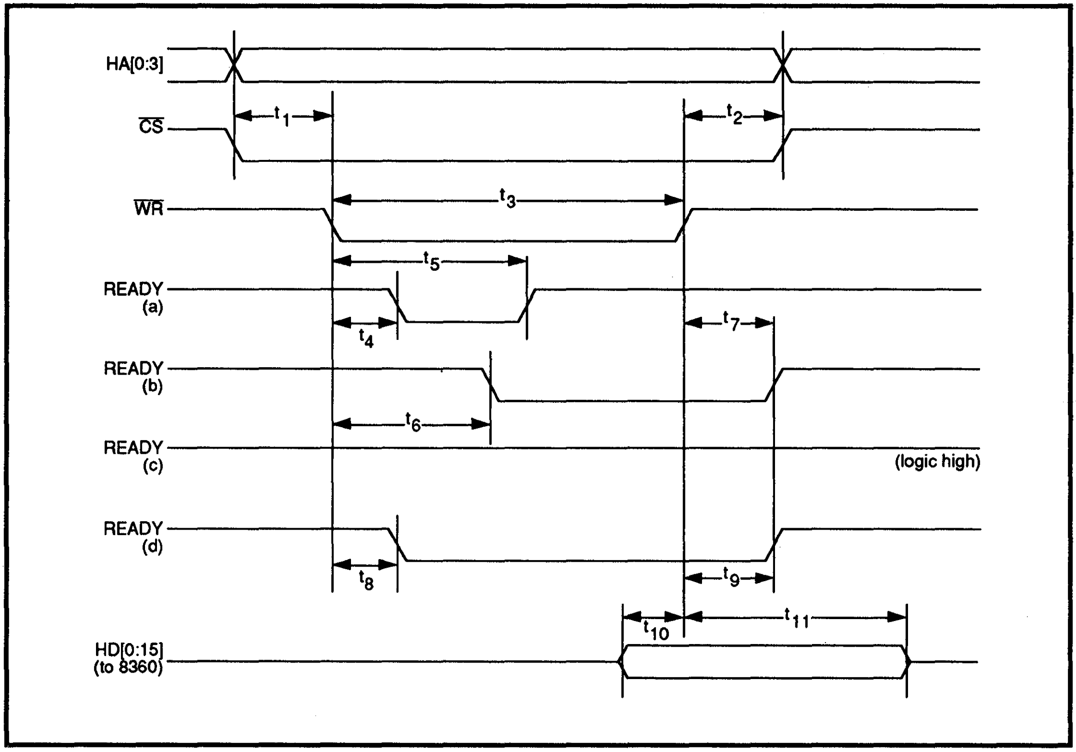


FIGURE 4: Write Cycle

TABLE 2: Write Cycle

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{CS}$ low to $\overline{WR}$ low; HA[0:3] valid to $\overline{WR}$ low t_1		0			ns
$\overline{WR}$ high to $\overline{CS}$ high; $\overline{WR}$ high to HA[0:3] invalid t_2		0			ns
$\overline{WR}$ low pulse width t_3		30			ns
$\overline{WR}$ low to READY low t_4	(a)	0		35	ns
$\overline{WR}$ low to READY high (1) t_5	(a)			400	ns
$\overline{WR}$ low to READY low (1) t_6	(b)	0		400	ns
$\overline{WR}$ high to READY high t_7	(b)			25	ns
$\overline{WR}$ low to READY low t_8	(d)	0		25	ns
$\overline{WR}$ high to READY high t_9	(d)	0		25	ns
HD[0:15] valid to $\overline{WR}$ high (data setup) t_{10}		15			ns
$\overline{WR}$ high to HD[0:15] invalid (data hold) t_{11}		10			ns

Note: (1) Maximum of 400 ns may occur if system makes contiguous system read cycles at less than 100 ns intervals, and both the transmitter and receiver are active on "loopback" reception (if the transmitter and receiver are idle, the max value becomes 250 ns). 2.4 µs max for host write error.
(a) For Buffer Memory Port when port is busy and RDYSEL = 1.
(b) For Buffer Memory Port when port is busy and RDYSEL = 0.
(c) For register or port is not busy and RDYSEL = 1.
(d) For register or port is not busy and RDYSEL = 0.

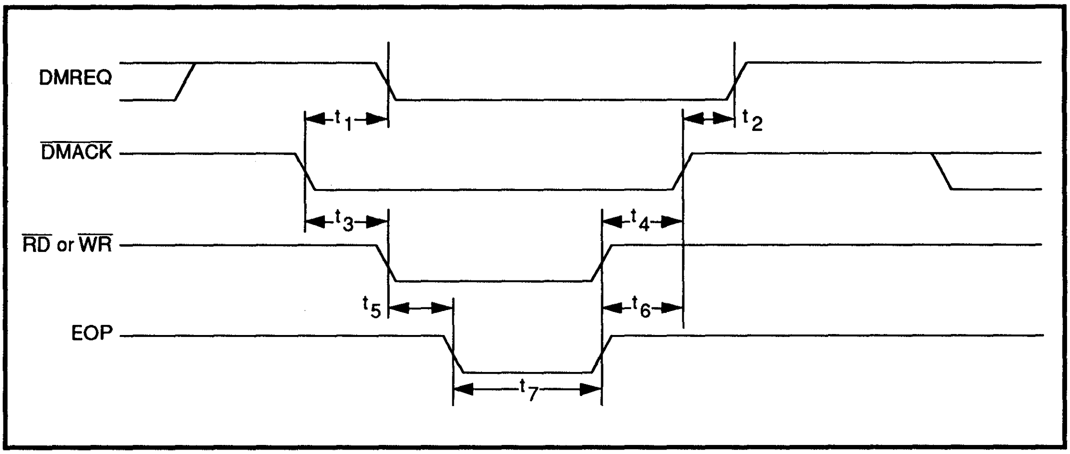


FIGURE 5: Single-Cycle DMA Timing

TABLE 3: Single-Cycle DMA Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{\text{DMACK}}$ low to DMREQ low t_1		0		20	ns
$\overline{\text{DMACK}}$ high to DMREQ high t_2		0		20	ns
$\overline{\text{DMACK}}$ low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ low t_3		0			ns
$\overline{\text{RD}}$ or $\overline{\text{WR}}$ high to $\overline{\text{DMACK}}$ high t_4		0			ns
$\overline{\text{RD}}$ or $\overline{\text{WR}}$ low to EOP low t_5		0			ns
EOP high to $\overline{\text{DMACK}}$ high t_6		0			ns
EOP low pulse width t_7		10			ns

Note: (1) An asserted EOP terminates any further DMREQ after $\overline{\text{DMACK}}$ returns high.
(2) The DMA cycle uses $\overline{\text{DMACK}}$ as the chip select. $\overline{\text{DMACK}}$ overrides $\overline{\text{CS}}$ and HA[0:3] if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.
(3) For READY timing and HD[0:15] timing, see Figure 3, t_4-t_{13}, and Figure 4, t_4-t_{11}.

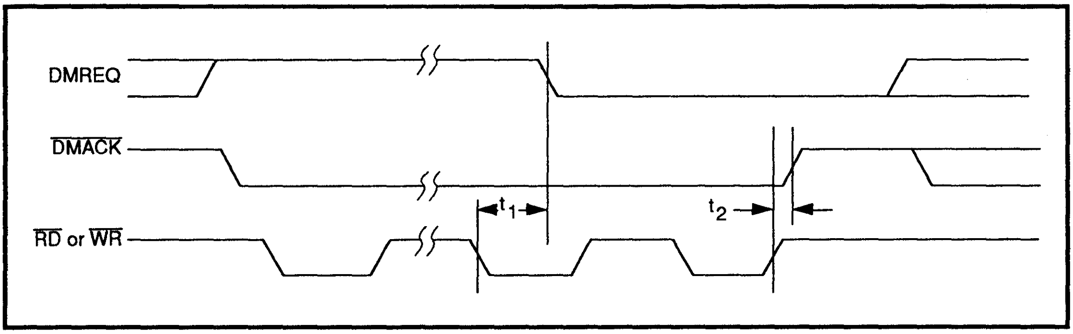


FIGURE 6: Burst DMA Timing

TABLE 4: Burst DMA Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{RD}$ or $\overline{WR}$ low to DMREQ low t_1				30	ns
$\overline{RD}$ or $\overline{WR}$ high to $\overline{DMACK}$ high t_2		0			ns

Note: (1) DMREQ goes low during the next-to-last transfer of the burst. $\overline{DMACK}$ should not go high until after the $\overline{RD}$ or $\overline{WR}$ pulse of the last transfer cycle goes high

(2) The DMA cycle uses $\overline{DMACK}$ as the chip select. $\overline{DMACK}$ overrides $\overline{CS}$ and HA[0:3] if they are both asserted at the same time, forcing selection of the Buffer Memory Port as in a DMA cycle.

(3) For READY timing and HD[0:15] timing, see Figure 3, t_4-t_{13}, and Figure 4, t_4-t_{11}.

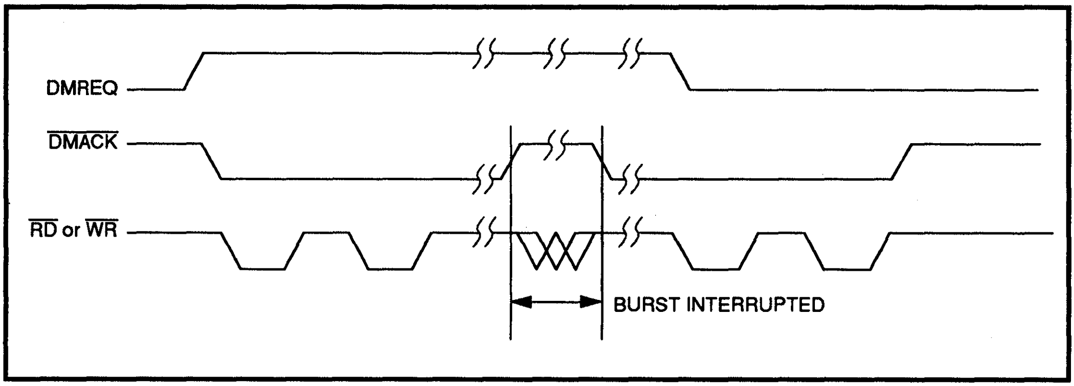


FIGURE 7: Burst DMA Interrupted by $\overline{\text{DMACK}}$

Note: Burst can be interrupted by $\overline{\text{DMACK}}$ high-going pulse during the burst. Burst will resume when $\overline{\text{DMACK}}$ returns low.

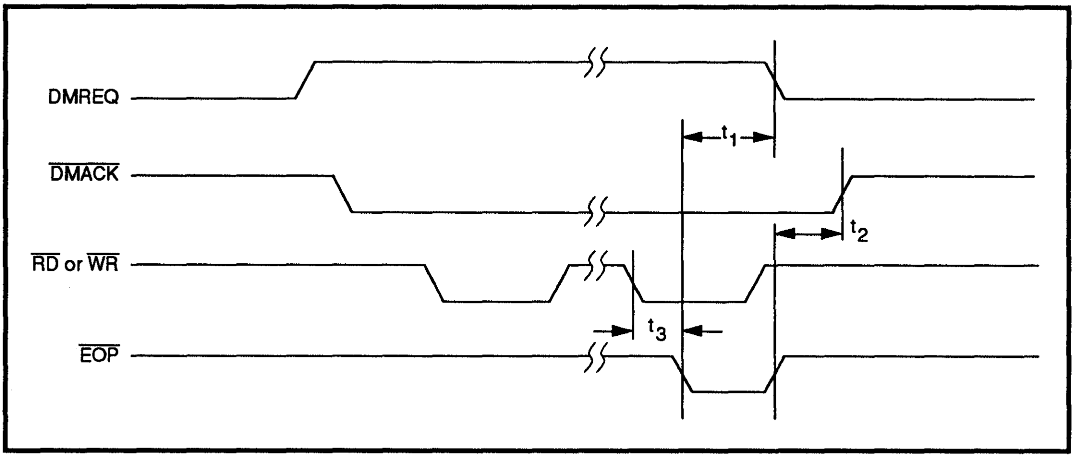


FIGURE 8: Burst DMA Terminated by EOP

TABLE 5: Burst DMA Terminated by EOP

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
EOP low to DMREQ low t_1		4		28	ns
EOP high to $\overline{\text{DMACK}}$ high t_2		3			ns
$\overline{\text{RD}}$ or $\overline{\text{WR}}$ low to EOP low t_3		0			ns

Note: EOP can be asserted during any transfer of the burst to terminate the process following that transfer.

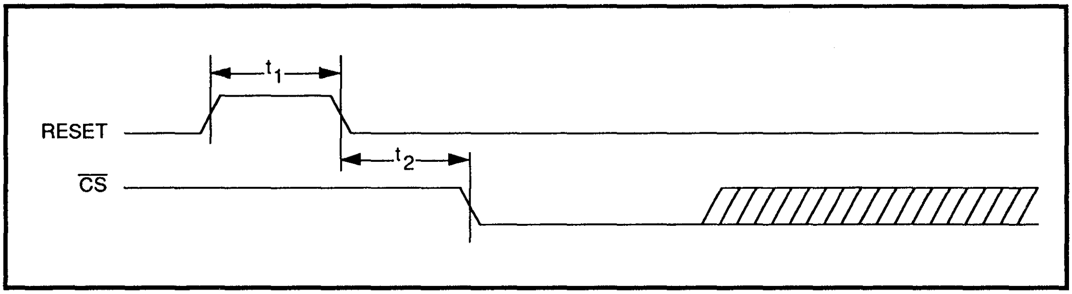


FIGURE 9: RESET Timing

TABLE 6: RESET Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RESET pulse width t_1		200			ns
RESET low to first $\overline{CS}$ low t_2		300			ns

Note: Before enabling transmit and receive functions ($\overline{ENADLC}$), wait 10 µs after reset pulse for internal calibration of DPLL.

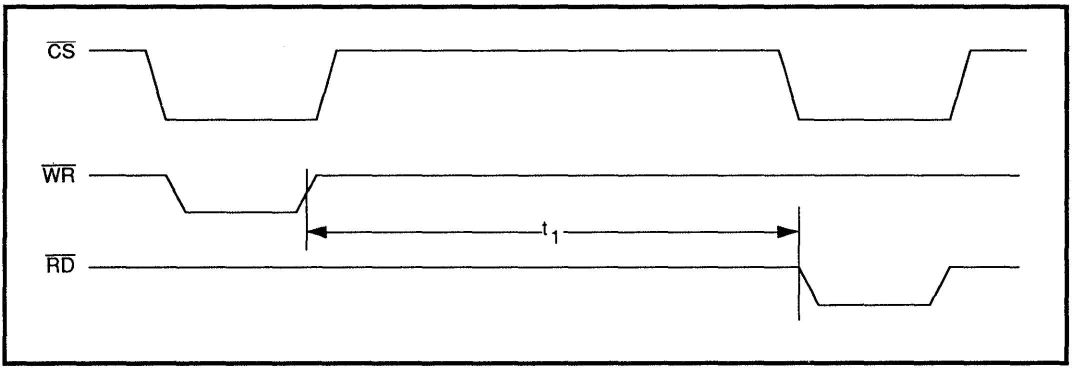


FIGURE 10: Skip Packet Timing

TABLE 7: Skip Packet Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Writing Skip Packet high to next Buffer Memory Port read t_1		200			ns

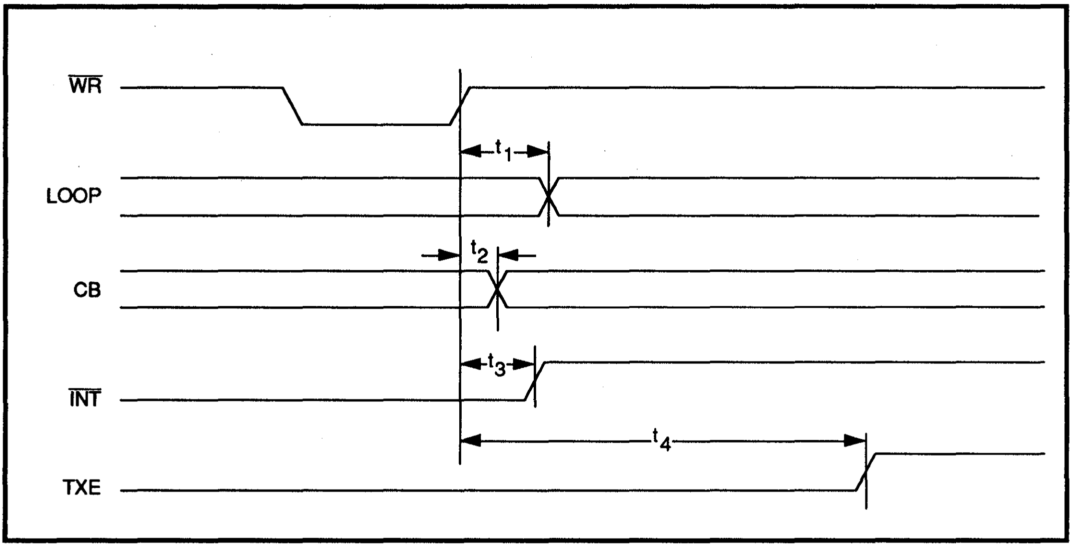


FIGURE 11: LOOP, CB and $\overline{INT}$ Timing

TABLE 8: LOOP, CB and $\overline{INT}$ Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Loopback Control (LOOP) delay t_1		5		30	ns
CB delay t_2		5		30	ns
$\overline{INT}$ signal clearing delay t_3		7		40	ns
Transmit enable delay after setting TXST high t_4	Network free and 8360 idle			1	µs

Note: TXST is BMR10<7>

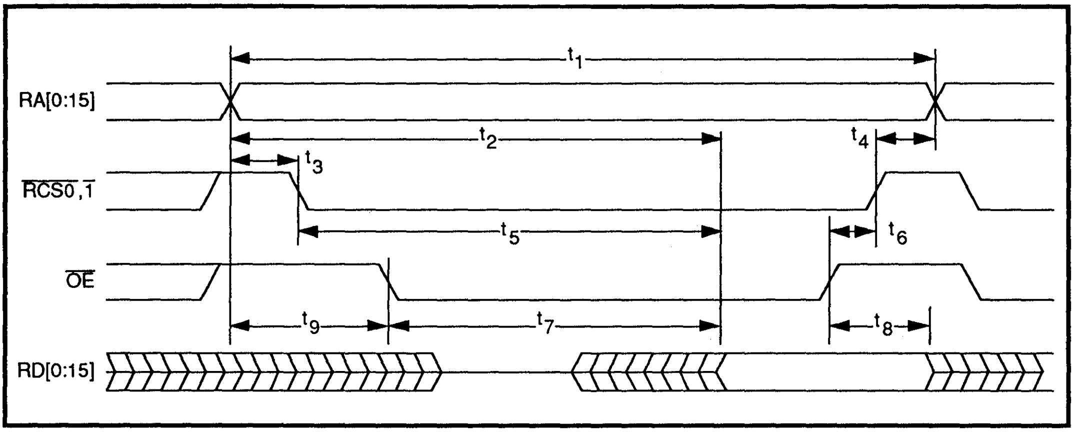


FIGURE 12: SRAM Read Timing

TABLE 9: SRAM Read Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Read cycle	t_1	RAMSP = 1	95			ns
		RAMSP = 0	145			ns
Address access time	t_2	RAMSP = 1			80	ns
		RAMSP = 0			130	ns
Address valid to $\overline{RCS0,1}$ low	t_3		0		5	ns
$\overline{RCS0,1}$ high to address invalid	t_4		0			ns
Chip select access time	t_5	RAMSP = 1			80	ns
		RAMSP = 0			130	ns
$\overline{OE}$ high to $\overline{RCS0,1}$ high	t_6		0		2	ns
Output enable access time	t_7				50	ns
Data hold time	t_8		0			ns
Address valid to $\overline{OE}$ low	t_9				30	ns

Note: Use SRAM with address access time of 80 ns or less for RAMSP = 1 and 130 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

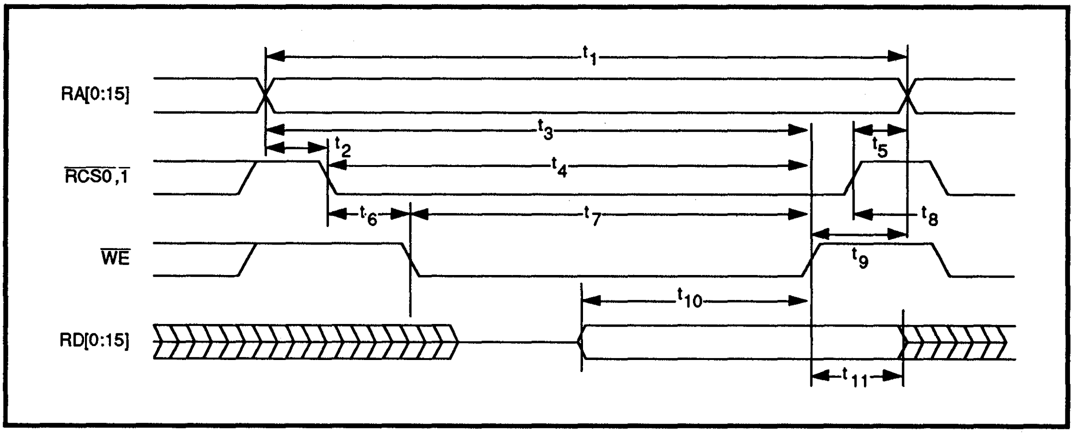


FIGURE 13: SRAM Write Timing

TABLE 10: SRAM Write Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Cycle t_1	RAMSP = 1	95			ns
	RAMSP= 0	145			ns
Address Valid to $\overline{\text{RCS0,1}}$ low t_2		0		5	ns
Address Valid to $\overline{\text{WE}}$ high t_3	RAMSP = 1	70			ns
	RAMSP = 0	120			ns
$\overline{\text{RCS0,1}}$ low to $\overline{\text{WE}}$ high t_4	RAMSP = 1	70			ns
	RAMSP = 0	120			ns
$\overline{\text{RCS0,1}}$ high to Address Invalid t_5		0			ns
$\overline{\text{RCS0,1}}$ low to $\overline{\text{WE}}$ low t_6		0			ns
$\overline{\text{WE}}$ Pulse Width t_7	RAMSP = 1	70			ns
	RAMSP = 0	120			ns
$\overline{\text{WE}}$ high to $\overline{\text{RCS0,1}}$ high t_8		0			ns
$\overline{\text{WE}}$ high to Address Invalid t_9		20			ns
Data Setup Time t_{10}		40			ns
Data Hold Time t_{11}		20			ns

Note: Use SRAM with address access time of 80 ns or less for RAMSP = 1 and 130 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

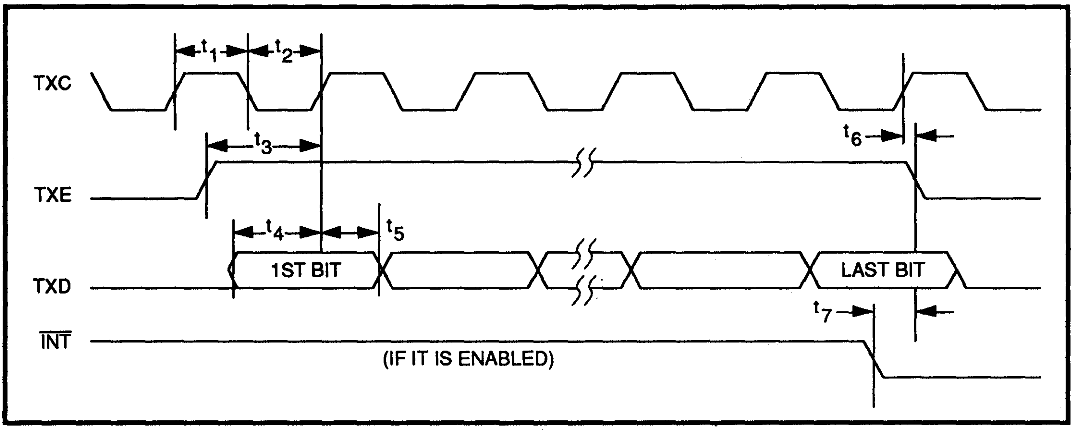


FIGURE 14: Transmit Timing

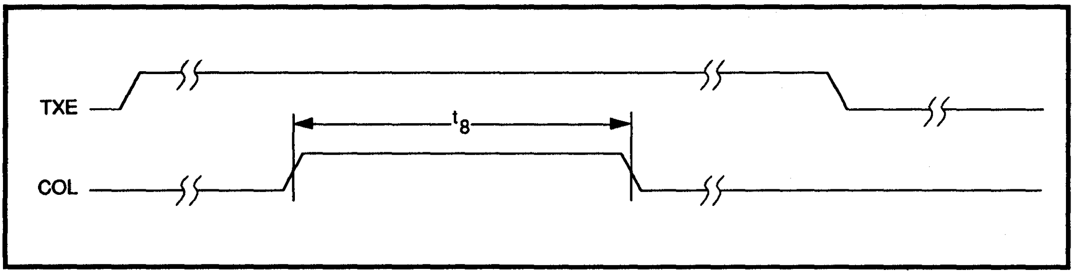


FIGURE 15: Transmit Timing

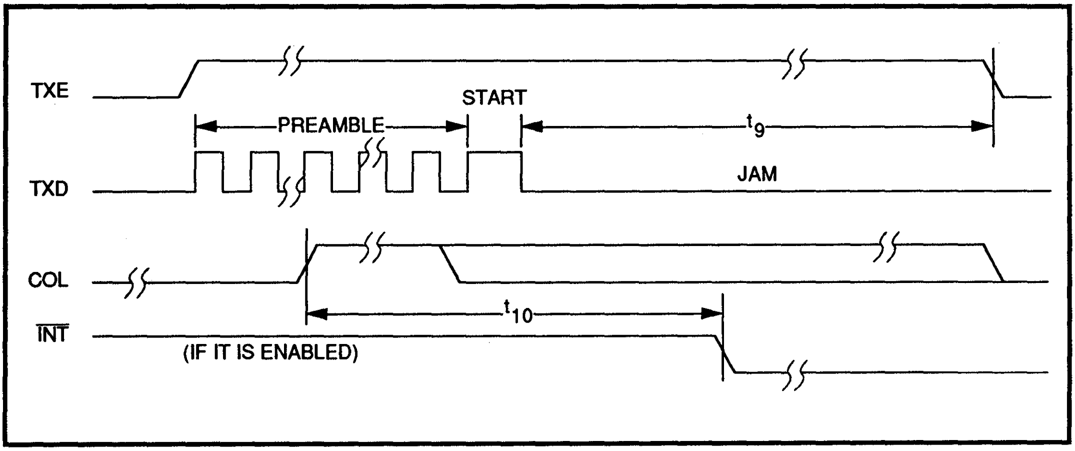


FIGURE 16: Transmit Timing

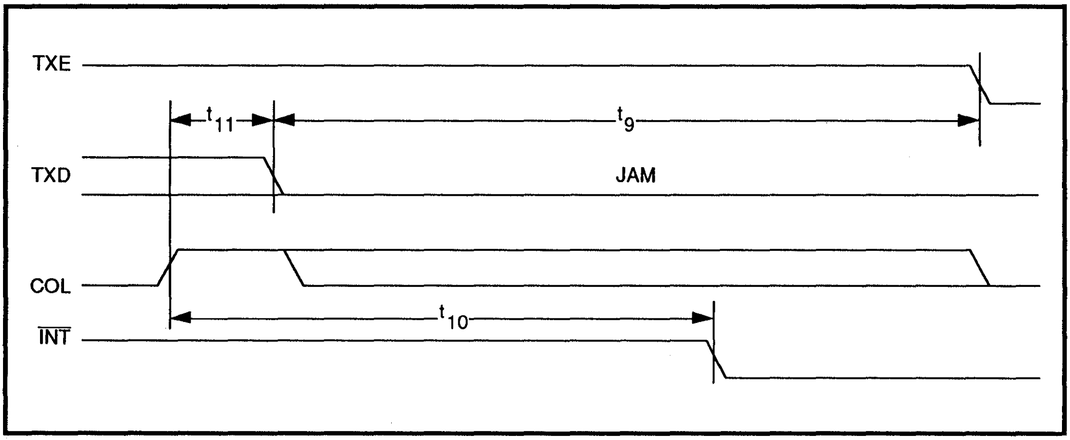


FIGURE 17: Transmit Timing

TABLE 11: Transmit Timing: Figure 14-17 (for external Encoder/Decoder mode)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Transmit clock high width t_1		45	50	55	ns
Transmit clock low width t_2		45	50	55	ns
TXE high to TXC high t_3		65	-	-	ns
Transmit data setup t_4		55	-	-	ns
Transmit data hold t_5		5	-	-	ns
TXC high to TXE low t_6		-	-	35	ns
Transmit interrupt low to transmit enable low t_7		-	1	-	TXC cycles
Minimum collision length t_8		200	-	-	ns
Jam period (1) t_9		-	32	-	TXC cycles
Transmit interrupt from collision t_{10}		-	-	5	TXC cycles
Collision at data field to first jam bit t_{11}		-	-	5	TXC cycles

Note: (1) The 32 jam bits consists of all zeroes.

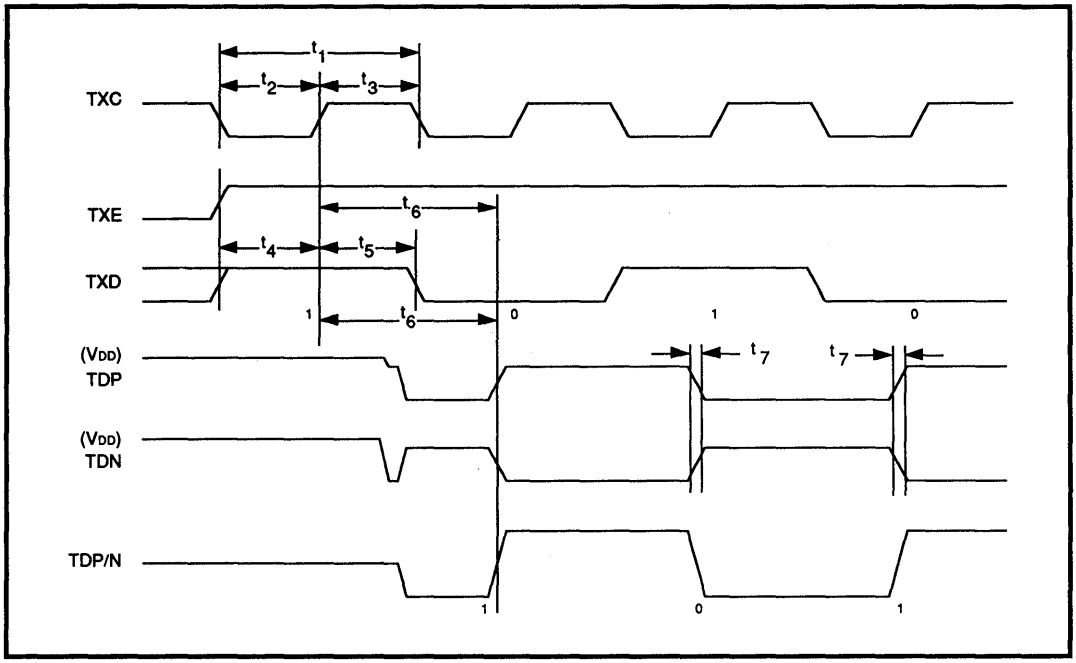


FIGURE 18: Transmit Start Timing

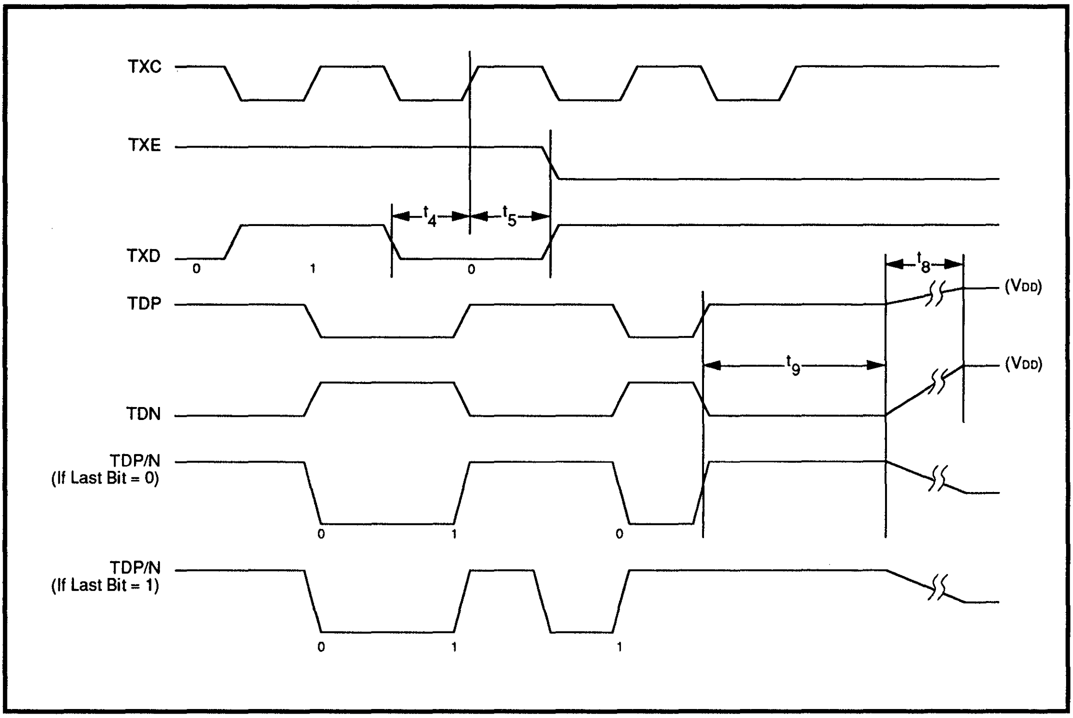


FIGURE 19: Transmit End Timing

TABLE 12: Transmit Start and End Timing: Figure 18-19 (for Encoder/Decoder Test mode)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TXC cycle time t_1		99.99	100	100.01	ns
TXC high width t_2		40	50	60	ns
TXC low width t_3		40	50	60	ns
TXD, TXE setup time to TXC t_4		-	30	-	ns
TXD, TXE hold time from TXC t_5		-	20	-	ns
TDP/N encode time t_6		-	90	-	ns
TDP,N fall/rise time t_7	20% to 80%, REXT = 20 kΩ, R_T = 78Ω	-	2	-	ns
TDP/N line voltage transition t_8		-	-	8	µs
TDP/N end-of-packet delimiter t_9		200	-	-	ns

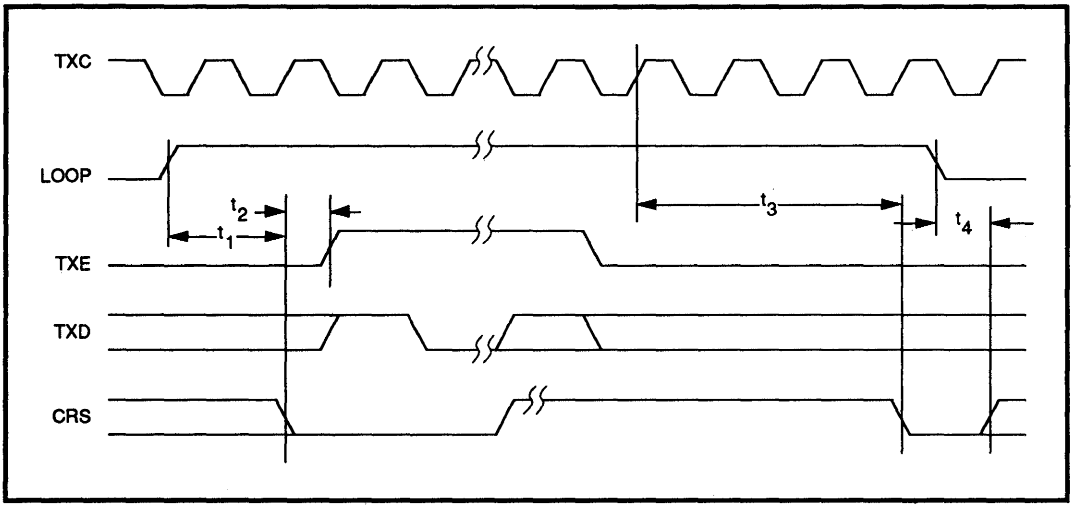


FIGURE 20: Loopback Timing

TABLE 13: Loopback Timing (for Encoder/Decoder test mode)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Loop receiving data purge time t_1		-	180	-	ns
Wait time from CRS low to TXE high t_2		9.6	-	-	µs
Data through time t_3		-	190	-	ns
Loop receiving data accept time t_4		-	30	-	ns

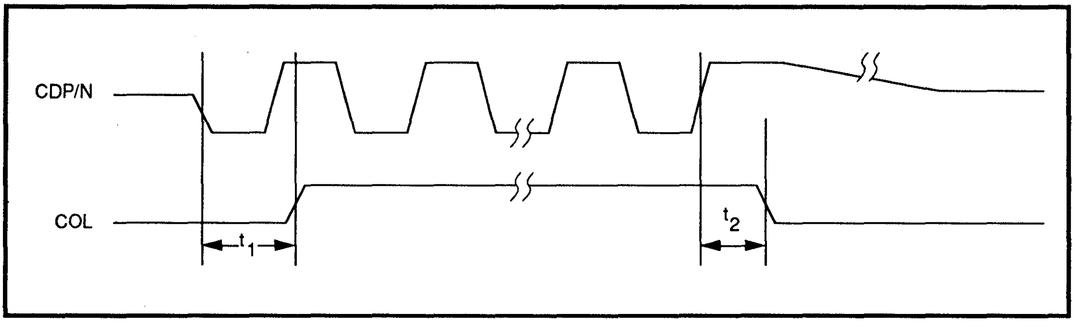


FIGURE 21: Collision Timing

TABLE 14: Collision Timing (for Encoder/Decoder Test mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
COL on delay time	t_1		–	40	50	ns
COL off delay time	t_2		–	270	300	ns

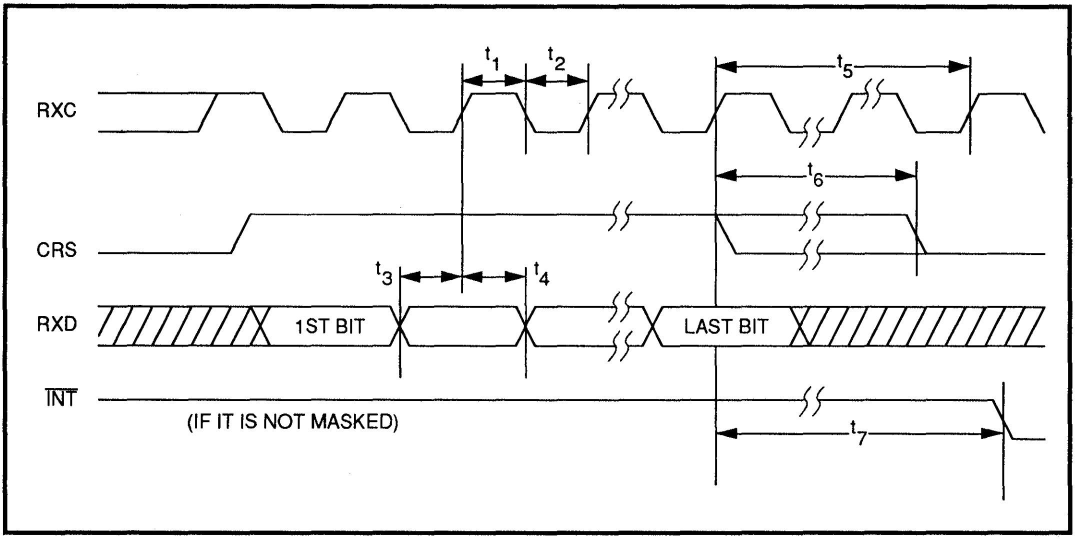


FIGURE 22: Receive Timing

TABLE 15: Receive Timing (for external Encoder/Decoder mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Receive clock high width	t_1		40			ns
Receive clock low width	t_2		40			ns
Receive data and carrier sense setup	t_3		20			ns
Receive data and carrier sense hold	t_4		20			ns
Number of RXC cycles after last bit	t_5		1			RXC cycles
Receive carrier sense drop after last bit	t_6				7	RXC cycles
Last bit of packet received to interrupt	t_7	Good packet			8	RXC cycles
		Bad packet			2	RXC cycles

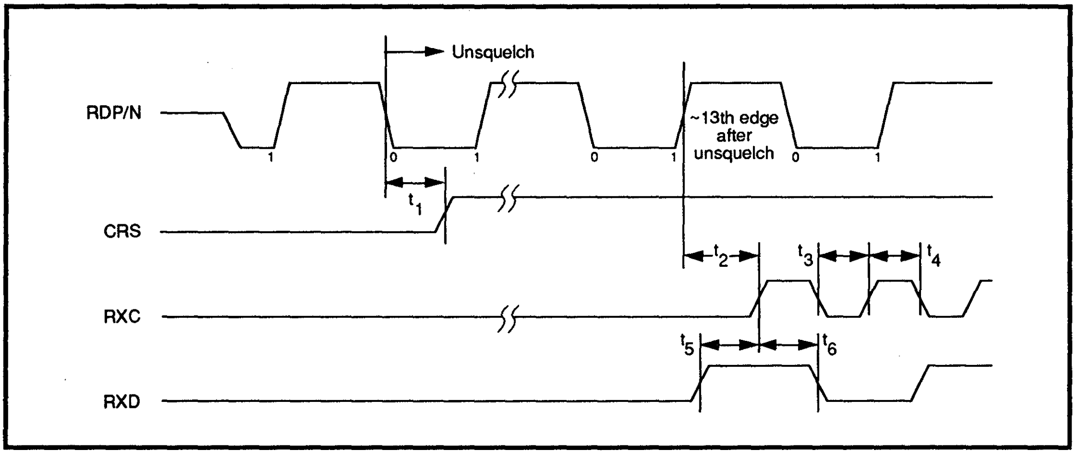


FIGURE 23: Receive Start Timing

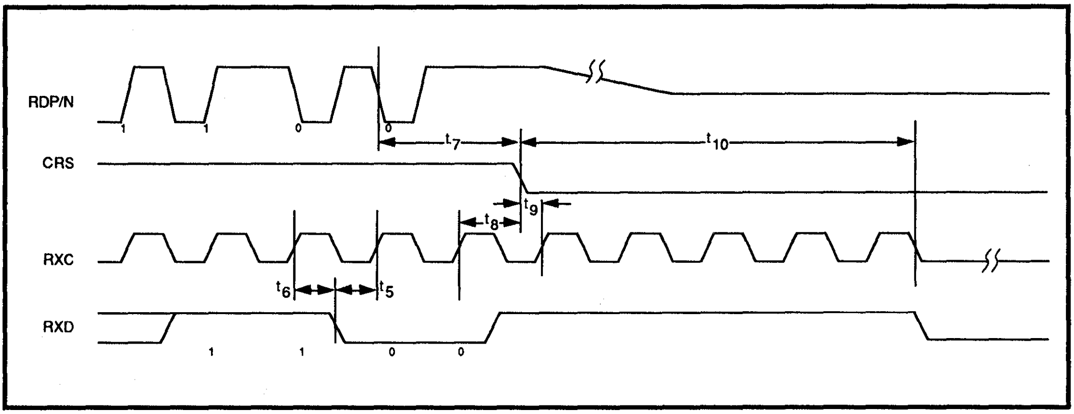


FIGURE 24: Receive End Timing

TABLE 16: Receive Timing: Figure 23-24 (for Encoder/Decoder Test mode)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
CRS on delay time	t_1		-	150	220	ns
RXC delay time	t_2		-	170	-	ns
RXC low time	t_3		35	50	-	ns
RXC high time	t_4		35	50	-	ns
RXD setup time to RXC	t_5		40	50	-	ns
RXD hold time from RXC	t_6		40	50	-	ns
CRS off delay time	t_7		-	220	-	ns
CRS high hold time	t_8		-	50	-	ns
CRS low setup time	t_9		-	50	-	ns
Number of RXC cycles after last bit	t_{10}		5	5	5	cycles

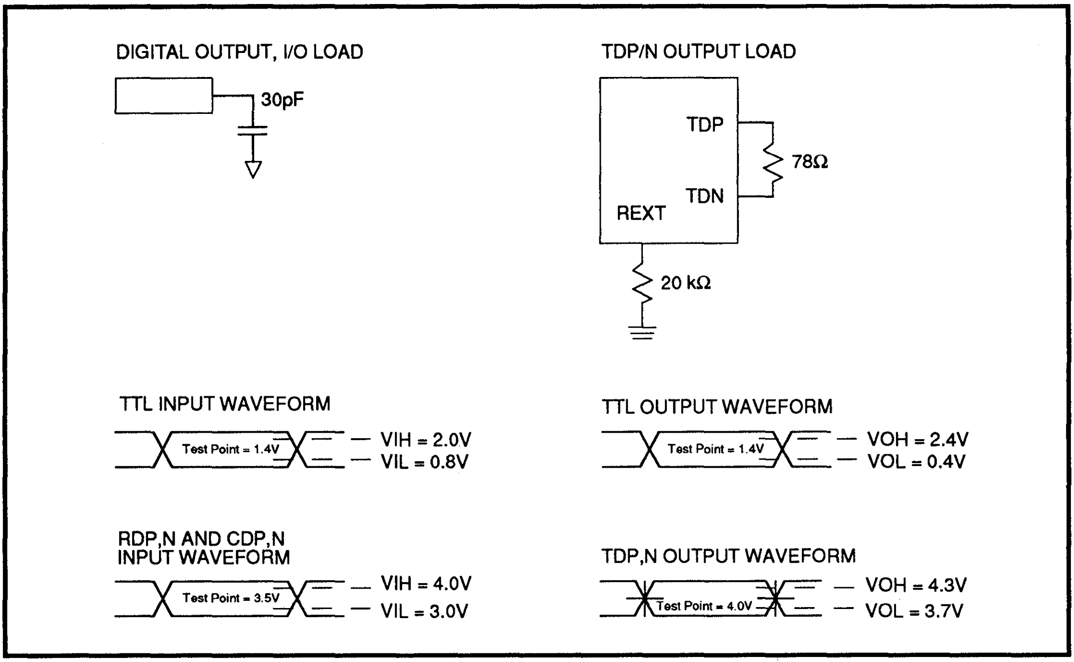
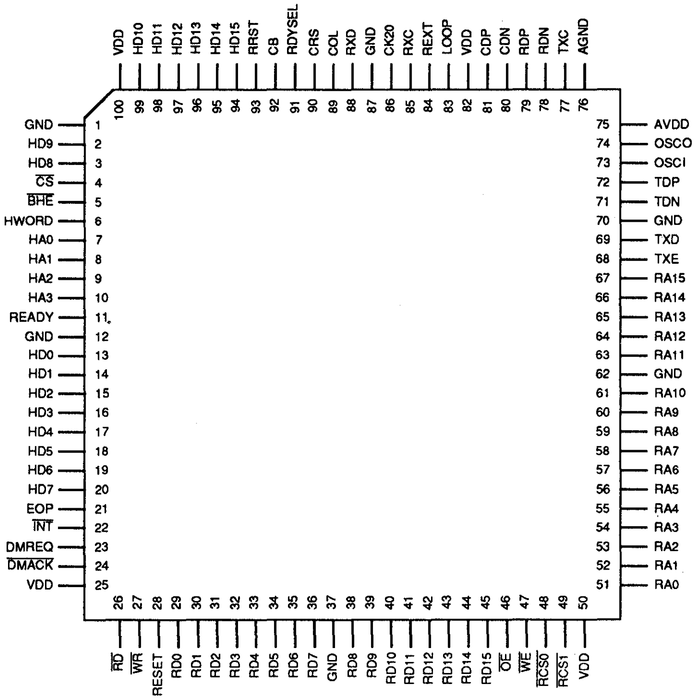


FIGURE 25: Test Conditions

SSI 78Q8360
Ethernet Controller/
ENDEC Combo

PACKAGE PIN DESIGNATIONS

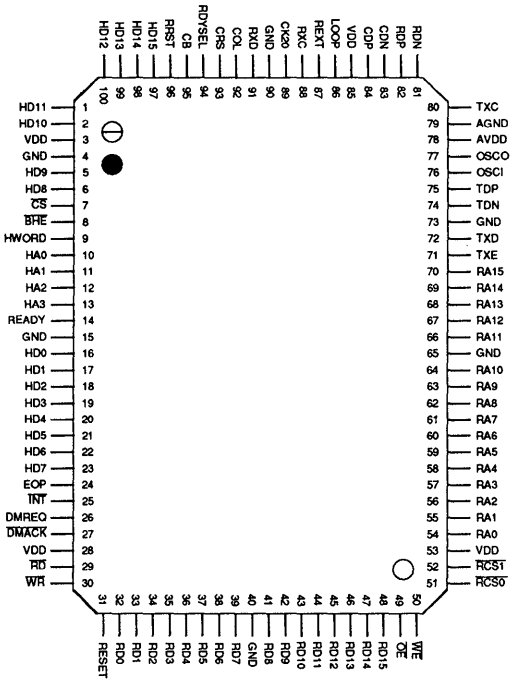
(Top View)



100-Lead TQFP

PACKAGE PIN DESIGNATIONS

(Top View)



100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 78Q8360 - Ethernet Controller/			
ENDEC Combo	100-pin QFP	78Q8360-CG	78Q8360-CG
	100-pin TQFP	78Q8360-CGT	78Q8360-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Notes:

silicon systems®
A TDK Group Company

SSI 78Q8370
PCMCIA Ethernet Combo
Advance Information

December 1992

DESCRIPTION

The SSI 78Q8370 is a highly integrated Ethernet IC for use in PCMCIA (Personal Computer Memory Card International Association) applications. It contains a Media Access Controller (MAC), a 10 Mbit/s Manchester encoder/decoder (ENDEC), a 10BaseT transceiver, a memory-card bus interface (PCMCIA), and an Attachment Unit Interface (AUI). This level of integration allows the user to implement a PCMCIA card for 10BaseT using only the SSI 78Q8370, external SRAM, and some passive components. The internal bus interface circuit allows connection to a PCMCIA 2.0 bus without other external components. The SSI 78Q8370 connects to twisted-pair media via line transformers through the on-chip transceiver circuit. Connection to other media such as coaxial cable is made through the AUI port to an external transceiver, such as the SSI 78Q8330 Ethernet Coax Transceiver.

The SSI 78Q8370 has a sophisticated power management capability with three different operating modes allowing the user to maximize power savings, making it ideal for use in PCMCIA applications. During normal operation, the IC monitors its own actions and shuts down the circuits that are not being used, resulting in the lowest possible operating power. It also has a standby mode which leaves only the oscillator running, and a full shutdown mode which also turns off the oscillator.

An intelligent Buffer Manager is controlled by the host read, host write, receive and transmit pointers, and the SSI 78Q8370 manages the pointers internally without any host intervention. The device interleaves access to the buffer memory so that accesses from the host and from the network media seem to operate concurrently. Interface with the host can be accomplished by memory mapping or I/O mapping. Big and little endian byte orderings make for simple bus interface to all standard microprocessors.

The SSI 78Q8370 is available in both a 100-lead QFP and thin QFP (TQFP) packages, and uses a single 5V supply.

FEATURES

- **Single-chip solution for 10BaseT/PCMCIA designs**
- **Integrated 10BaseT transceiver:**
  - **Programmable/automatic selection of twisted pair (RJ45) or AUI port**
  - **Receive polarity detection/correction on twisted-pair inputs**
- **Manchester Encoder/Decoder circuit**
- **AUI port for connection to 10Base2/5 transceiver or AUI cable**
- **Integrated bus interface compliant with PCMCIA 2.0 specification**
- **Protocol Contoller compliant with IEEE 802.3 and Ethernet 2.0**
- **Advanced Buffer Manager architecture:**
  - **Automatic management of all pointers**
  - **Allows "simultaneous" access to data in buffer memory by both the network and host**
  - **High-speed received packet skip**
- **Configurable Buffer Memory for design flexibility:**
  - **Two-bank transmit buffer in 2, 4, 8, or 16 Kbyte sizes**
  - **Ring-structure receive buffer from 4 to 30 Kbytes**
- **Software-configurable system bus structure:**
  - **Compatible with major microprocessors**
  - **8- or 16-bit wide data path communications with hosts**
- **Power management options include:**
  - **Intelligent power mode automatically shuts off unused circuitry**
  - **Standby mode reduces power while not in operation**
  - **Full power-down mode offers maximum power savings**
- **Three different loopback modes**
- **Multicast address filtering via 64-element hash table**
- **Available in 100-lead QFP and TQFP**

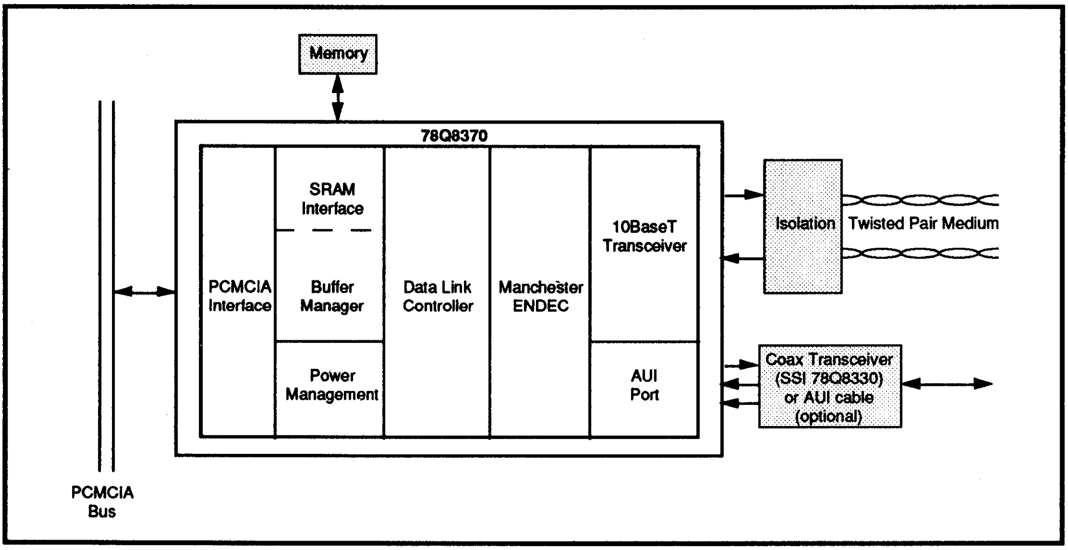


FIGURE 1: System Diagram

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Section 7

PROGRAMMABLE ELECTRONIC FILTERS

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A TDK Group Company

SSI 32F8001/8002
Low-Power Programmable Electronic Filter

Advance Information

December 1992

DESCRIPTION

The SSI 32F8001/8002 Programmable Electronic Filters provide an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation make the SSI 32F8001/8002 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8001 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal.

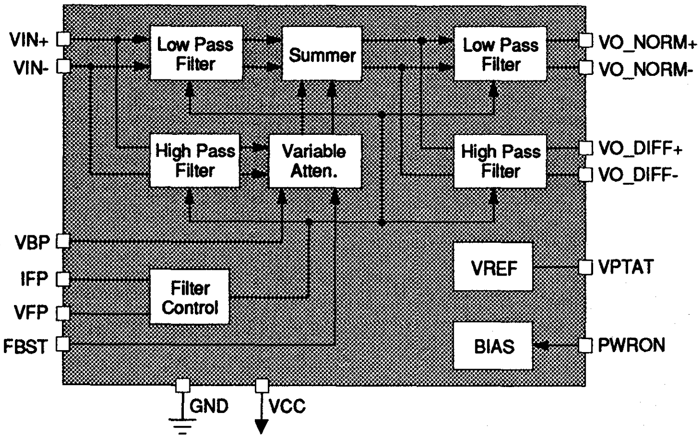
The SSI 32F8002 is identical to the SSI 32F8001, except for the cutoff frequency range, which is 6 to 18 MHz in the SSI 32F8002.

The SSI 32F8001/8002 require only a +5V supply and are available in 16-pin SON and SOL packages.

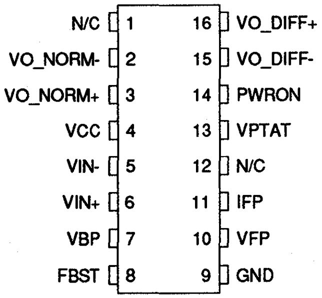
FEATURES

- **Ideal for multi-rate systems applications**
- **Programmable filter cutoff frequency (*fc* = 9 to 27 MHz, 32F8001; *fc* = 6 to 18 MHz, 32F8002)**
- **Programmable pulse slimming equalization (0 to 13 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 0.2 *fc* to *fc* here,**
  9 MHz ≤ *fc* ≤ 27 MHz SSI 32F8001
  6 MHz ≤ *fc* ≤ 18 MHz SSI 32F8002
- **Total harmonic distortion less than 1.5%**
- **No external filter components required**
- **+5V only operation**
- **16-pin SON and SOL package**
- **Pin compatible with SSI 32F8011**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8001/8002
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8001/8002 are high performance programmable electronic filters. They feature a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8001 programmable electronic filter can be set to a filter cutoff frequency from 9 to 27 MHz with no boost (6 to 18 MHz for the SSI 32F8002).

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8001/8002 output reference voltage VPTAT, or by means of an external resistor tied from the output voltage reference pin VPTAT to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the SSI 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the SSI 32D4661 by the reference voltage from the VPTAT pin of the SSI 32F8001/8002. This reference voltage is internally generated by a band-gap circuit in conjunction with a temperature varying reference to create a voltage which is proportional to absolute temperature.

The VPTAT voltage will compensate for internal temperature variation of the fc and boost circuits.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

fc (ideal, in MHz)

(32F8001) = 45.0 • IFP = 45.0 • IVFP • 1.8/VPTAT

(32F8002) = 30.0 • IFP = 30.0 • IVFP • 1.8/VPTAT

where IFP and IVFP are in mA, $0.2 < \text{IFP} < 0.6$ mA, and VPTAT is in volts. Ta = 25°C.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the SSI 32F8001/8002 cutoff frequency is set using voltage VPTAT to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

fc (ideal, in MHz)

(32F8001) = 45.0 • IFP = 45.0 • 1.8/(3 • Rx)

(32F8002) = 30.0 • IFP = 30.0 • 1.8/(3 • Rx)

Rx in kΩ

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB above the DC gain.

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VPTAT (provided by the VPTAT pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VPTAT and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[3.46(\text{VBP}/\text{VPTAT})+1]$, where $0 < \text{VBP} < \text{VPTAT}$.

POWER ON / OFF

The SSI 32F8001/8002 support a power down mode for minimal idle mode power dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN-	I	Differential Signal Inputs. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	O	Differential Normal Outputs. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	O	Differential Differentiated Outputs. For minimum time skew, these outputs should be AC coupled.
IFP	I	Frequency Program Input. The filter cutoff frequency *fc*, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VPTAT. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	I	Frequency Program Input. The filter cutoff frequency can be set by programming a current through a resistor from VPTAT to this pin. IFP should be left open when using this pin.
VBP	I	Frequency Boost Program Input. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VPTAT. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VPTAT and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	I	Frequency Boost. A high logic level or open enables the frequency boost circuitry. A low input disables this function.
PWRON	I	Power On. A high logic level enables the chip. A low level or open pin puts the chip in a low power state.
VPTAT	O	PTAT Reference Voltage. This pin outputs a reference voltage which is proportional to absolute temperature (PTAT). VBP, VFP or IFP must be referenced to this pin for proper operation.
VCC	O	+5 Volt Supply.
GND	I	Ground

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65 °C to +150 °C
Junction Operating Temperature, Tj	+130 °C
Supply Voltage, VCC	-0.5V to 7V
Voltage Applied to Inputs	-0.5V to VCC

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS
Supply voltage, VCC	4.50V < VCC < 5.50V
Ambient Temperature	0 °C < Ta < 70 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Characteristics						
Power Supply Current	ICC	PWRON ≤ 0.8V		0.1	0.5	mA
Power Supply Current	ICC	PWRON ≥ 2.0V		46	60	mA
Power Dissipation	PD	PWRON ≥ 2.0V, VCC = 5.0V		230	300	mW
		PWRON ≥ 2.0V, VCC = 5.5V		275	330	mW
		PWRON ≤ 0.8V		0.5	2.5	mW
DC Characteristics						
High Level Input Voltage	VIH	TTL input	2.0			V
Low Level Input Voltage	VIL				0.8	V
High Level Input Current	IIH	VIH = 2.7V			20	µA
Low Level Input Current	IIL	VIL = 0.4V			–1.5	mA
Filter Characteristics						
Filter Cutoff Frequency *(f -3dB)	*fc	32F8001 $fc = \frac{45\ \text{MHz}}{\text{mA}}(\text{IVFP})$	9.0		27.0	MHz
		IVFP = 0.2 to 0.6 µA, Ta = 25v °C				
		32F8002 $fc\frac{30\ \text{MHz}}{\text{mA}}(\text{IVFP})$	6		18	MHz
Filter fc Accuracy	FCA	fc = max.	–10		+10	%
VO_NORM Diff Gain	AO	F = 0.67 fc, FB = 0 dB	0.8		1.20	V/V
VO_DIFF Diff Gain	AD	F = 0.67 fc, FB = 0 dB	0.85AO		1.15AO	V/V
Frequency Boost at fc	FB	VBP = VPTAT fc = max.	11.5	13.0	14.5	dB
		fc = min.	11.0	12.5	14.0	dB
Frequency Boost Accuracy	FBA	VBP/VPTAT = 0.5255 fc = max.	–1		+1	dB
		VBP/VPTAT = 1.0 fc = max.	–1.5		+1.5	dB

Filter Characteristics (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Group Delay Variation Without Boost	TGDO	*fc* = max., $\frac{VBP}{VPTAT}=0$ 32F8001	–500		+500	ps
		F = 0.2 *fc* to *fc* 32F8002	-750		+750	ps
		fc = min., $\frac{VBP}{VPTAT}=0$ 32F8001	-1.5		+1.5	ns
		32F8002 F = 0.2 *fc* to *fc*	-2.25		+2.25	ns
		fc = 9 MHz - 27 MHz (32F8001) *fc* = 6 MHz - 18 MHz (32F8002) F = 0.2 *fc* to *fc* $\frac{VBP}{VPTAT}=0$	–2		+2	%
		fc = 9 MHz - 27 MHz, $\frac{VBP}{VPTAT}=0$ F = *fc* to 1.75 *fc* 32F8001	-4		+4	%
		fc = 6 MHz - 18 MHz, $\frac{VBP}{VPTAT}=0$ F = *fc* to 1.75 *fc* 32F8002	-3		+3	%
	TGDB	*fc* = max, VBP = VPTAT 32F8001	–500		+500	ps
		F = 0.2 *fc* to *fc* 32F8002	-750		+750	
		fc = min., VBP = VPTAT 32F8001	-1.5		+1.5	ns
		F = 0.2 to *fc* 32F8002	-2.25		+2.25	ns
		fc = 9 MHz - 27 MHz (32F8001) *fc* = 6 MHz - 18 MHz (32F8002) F = 0.2 *fc* to *fc*, VBP = VPTAT	–2		+2	%
		fc = 9 MHz - 27 MHz, VBP = VPTAT F = *fc* to 1.75 *fc* 32F8001	-4		+4	%
		fc = 6 MHz to 18 MHz, VBP = VPTAT F = *fc* to 1.75 *fc* 32F8002	-3		+3	%
Filter Input Dynamic Range	VIF	THD = 1% max, F = 0.67 *fc*, VBP = 0V (1000 pF across Rx)	1.0			Vpp
		THD = 1.5% max, F = 0.67 *fc*, VBP = 0V, Normal output (1000 pF across Rx)	1.5			Vpp
		THD = 2.0% max, F = 0.67 *fc*, VBP = 0V, Differentiated output (1000 pF across Rx)	1.5			Vpp

ELECTRICAL SPECIFICATIONS (continued)

Filter Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter Output Dynamic Range VOF	THD = 1% max, F = 0.67 *fc* RLOAD ≥ 1kΩ (1000 pF across Rx)	1.0			Vpp
Filter Diff Input Resistance RIN		3.0			kΩ
Filter Input Capacitance CIN				7	pF
Output Noise Voltage EOUT Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = max, VBP = 0V 32F8001		3.6		mVRms
	32F8002		3.3		
Output Noise Voltage EOUT Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = max, VBP = 0V 32F8001		2.3		mVRms
	32F8002		2.0		
Output Noise Voltage EOUT Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = max, VBP = VPTAT 32F8001		5.8		mVRms
	32F8002		5.0		
Output Noise Voltage EOUT Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = max, VBP = VPTAT 32F8001		2.9		mVRms
	32F8002		2.5		
Filter Output Sink Current IO–		1.0			mA
Filter Output Source Current IO+		2.0			mA
Filter Output Resistance RO (Single ended)	IO+ = 1.0 mA			60	Ω
Filter Control Characteristics					
Reference Voltage VPTAT	Tj = 25 °C		1.8		V
PTAT Voltage Input VFP			2/3 VPTAT		V
Programming Current Range IVFP	TA = 25 °C	0.2		0.6	mA
Programming Current Range V_{VBP}		0		VPTAT	V
Voltage at pin IFP V_{IFP}	I_{VFP} = 0 mA		2/3 VPTAT		V

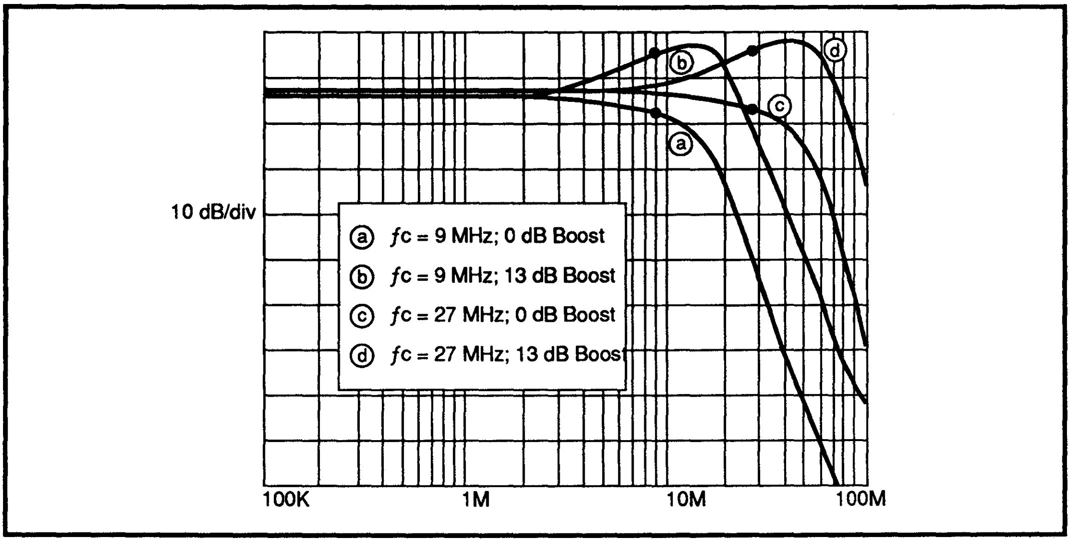


FIGURE 1: 32F8001 Normal Low Pass Response

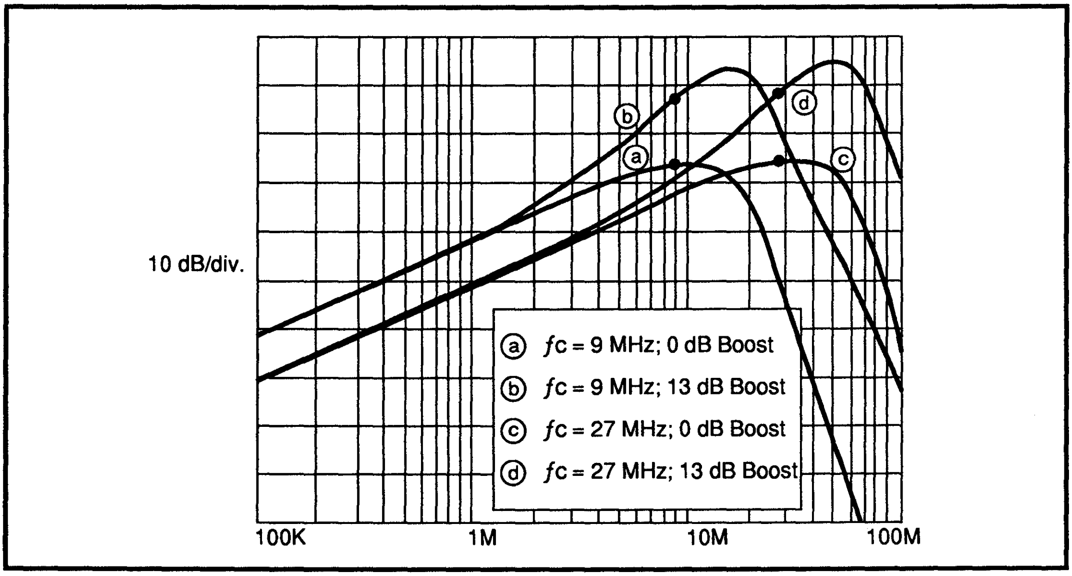


FIGURE 2: 32F8001 Differentiated Low Pass Response

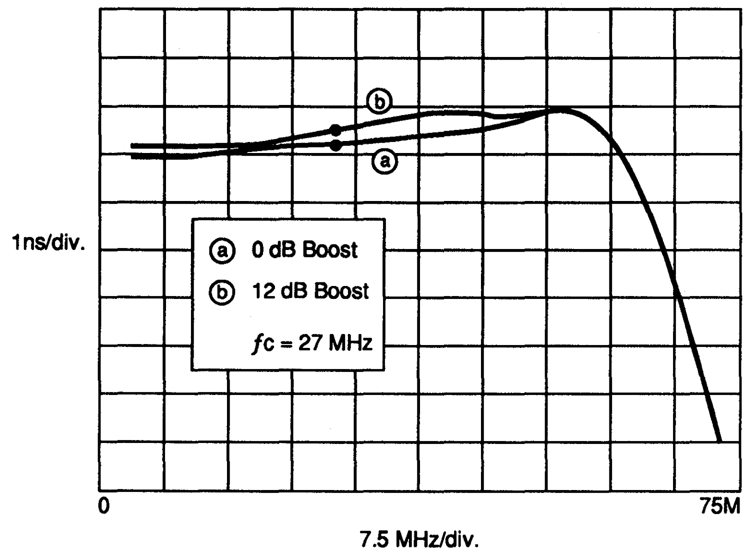
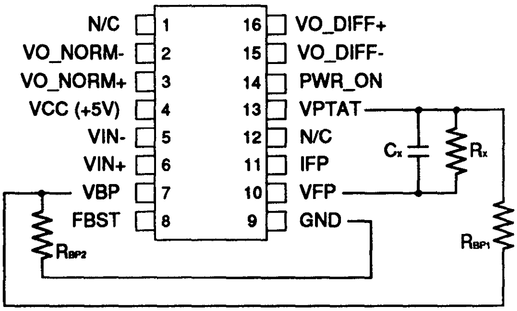


FIGURE 3: 32F8001 Group Delay Response with *fc* = 27 MHz



VPTAT = 1.8V (25 °C)

V_{VFP} = 2/3 (VPTAT)

IVFP range: 0.2 mA to 0.6 mA @25°C

(9 to 27 MHz no boost 32F8001)

(6 to 18 MHz no boost 32F8002)

Fixed frequency programming is accomplished as shown in the drawing above.

In this case IVFP (programming current) is equivalent to $\frac{\text{VPTAT}}{3} \bullet \frac{1}{R_x}$

i.e., fc = 27 MHz then

IVFP = 0.6 mA @25 °C Rx = 1 KΩ

Fixed boost programming is also accomplished as shown above. In this case V_{VBP} is set by a voltage divider, where V_{VBP} is a fraction of VPTAT.

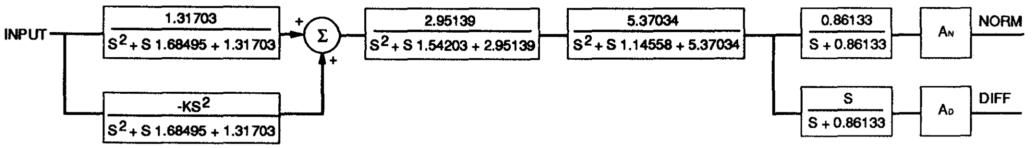
i.e., boost = 9 dB then,

VBP/VPTAT = 0.5255 9 dB = 20 log [3.46 (0.5255) + 1]

$$\frac{R_{BP2}}{R_{BP1}} = \frac{1}{\left(\frac{\text{VPTAT}}{\text{VBP}} - 1\right)} = 1.107$$

Cx = 1000 pF - Cx is needed for lower THD at lower fc.

FIGURE 4: 32F8001/8002 Applications Setup



Normalized for $\omega c = (2\pi)\,fc = 1$
AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc
Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$
Eq for $fc = 27$ MHz, $S = S / [(2\pi)(27 \times 10^6)]$

FIGURE 5: 32F8001/8002 Normalized Block Diagram

TABLE 1: 32F8001/8002 Frequency Boost Calculations

	Boost	K	$\frac{VBP}{VPTAT}$	Boost	K	$\frac{VBP}{VPTAT}$
Assuming 13 dB boost for VBP = VPTAT $\frac{VBP}{VPTAT} \cong \frac{\left(10^{(FB/20)}\right)-1}{3.46}$	1 dB	0.16	0.035	6 dB	1.31	0.288
	2 dB	0.34	0.075	7 dB	1.63	0.358
	3 dB	0.54	0.119	8 dB	1.99	0.437
	4 dB	0.77	0.169	9 dB	2.40	0.526
	5 dB	1.03	0.225	10 dB	2.85	0.625
				11 dB	3.36	0.737
				12 dB	3.43	0.862
				13 dB	4.57	1.00

	$\frac{VBP}{VPTAT}$	Boost	$\frac{VBP}{VPTAT}$	Boost
or, boost in dB $= 20\log\left[3.46\left(\frac{VBP}{VPTAT}\right)+1\right]$	0.1	2.581 dB	0.6	9.760 dB
	0.2	4.568 dB	0.7	10.686 dB
	0.3	6.184 dB	0.8	11.522 dB
	0.4	7.546 dB	0.9	12.285 dB
	0.5	8.723 dB	1.0	13 dB

TABLE 2: Calculations

Typical change in *f*-3 dB point with boost

Boost (dB)	Gain@*fc* (dB)	Gain@ peak (dB)	*f*peak/*fc*	*f*-3dB/*fc*
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59
10	7	8.40	1.48	2.66
11	8	9.59	1.51	2.73
12	9	10.77	1.51	2.80
13	10	11.92	1.53	2.87

Notes:
1. *fc* is the original programmed cutoff frequency with no boost
2. *f*-3 dB is the new -3 dB value with boost implemented
3. *f*peak is the frequency where the amplitude reaches its maximum value with boost implemented

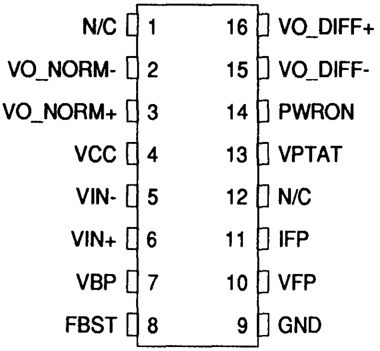
i.e., *fc* = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 19.8 MHz
*f*peak = 11.07 MHz

SSI 32F8001/8002
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS

(Top View)



32F8001/8002
16-pin SON, SOL

THERMAL CHARACTERISTICS: θja

16-lead SON (150 mil)	105°C/W
16-lead SOL (300 mil)	100°C/W

ORDERING INFORMATION

PART DESCRIPTION		ORDERING NUMBER	PACKAGE MARK
SSI 32F8001	16-Lead SON (150 mil)	32F8001-CN	32F8001-CN
	16-Lead SOL (300 mil)	32F8001-CL	32F8001-CL
SSI 32F8002	16-Lead SON (150 mil)	32F8002-CN	32F8002-CN
	16-Lead SOL (300 mil)	32F8002-CL	32F8002-CL

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

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A TDK Group Company

SSI 32F8011/8012
Programmable Electronic Filter

December 1992

DESCRIPTION

The SSI 32F8011/8012 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, Bessel–type, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programmability, combined with low group delay variation makes the SSI 32F8011/8012 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

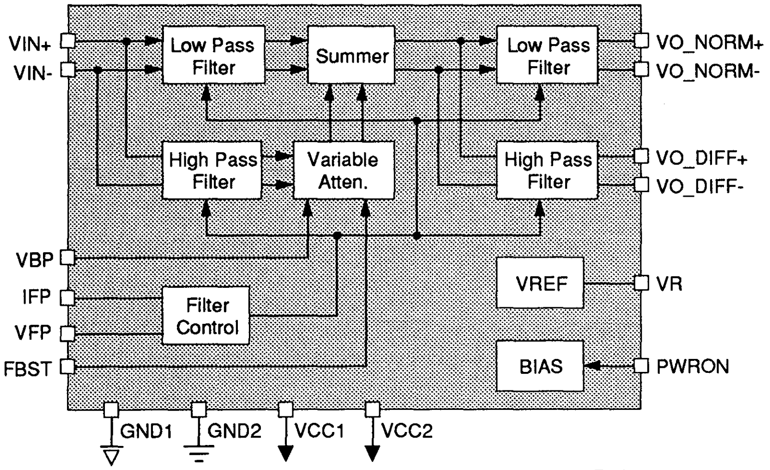
The SSI 32F8011/8012 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors, in addition boost can be switched in or out by a logic signal.

The SSI 32F8011/8012 requires only a +5V supply and is available in 16-pin SON and SOL packages.

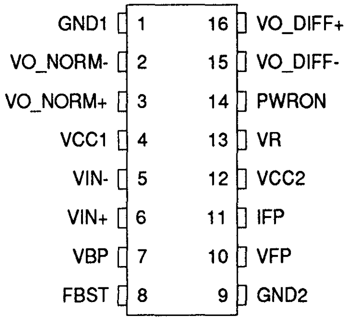
FEATURES

- **Ideal for:**
  - **- constant density recording applications**
  - **- cellular telephone applications**
  - **- radio**
  - **- data acquisition**
  - **- LAN**
- **Programmable filter cutoff frequency (SSI 32F8011 *fc* = 5 to 13 MHz) (SSI 32F8012 *fc* = 6 to 15 MHz)**
- **Programmable high frequency peaking (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±0.75 ns group delay variation from 0.2 *fc* to *fc* = 13 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-pin SON, and SOL packages**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8011/8012, a high performance programmable electronic filter, provides a low pass Bessel-type seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4720 Combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The programmable electronic filter can be set to a filter cutoff frequency from 5 to 13 MHz (with no boost) for SSI 32F8011 and 6 to 15 MHz for SSI 32F8012.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8011/8012 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8011/8012. This reference voltage is an internally generated bandgap reference, which typically varies less than 1% over supply voltage and temperature variation.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•IVFP•2.2/VR

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•IVFP•2.2/VR
where IFP and IVFP are in mA, 0.31<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8011/8012 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•2.2/(3•Rx)

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•2.2/(3•Rx)
where Rx is in kΩ, 0.917<Rx<2.366 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the output signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = 20 $\log_{10}$[1.884(VBP/VR)+1], where 0<VBP<VR.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector.
IFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin.
VBP	FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level or open circuit enables the chip. A low level puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC1, VCC2	+5 VOLT SUPPLY.
GND1, GND2	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC1, VCC2	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC + 0.5	V
IFP, VFP Inputs Maximum Current*	≤1.2	mA

* Exceeding this current may cause frequency programming lockup.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC1, VCC2	4.5 < VCC1,2 < 5.50	V
Ambient Temperature	0 < Ta < 70	°C

ELECTRICAL CHARACTERISTICS

Power Supply Characteristics (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
ICC Power Supply Current	PWRON ≤ 0.8V	VBP = VR		14	17	mA
		VBP = 0V		12	15	mA
ICC Power Supply Current	PWRON ≥ 2.0V			67	80	mA

DC Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VIH High Level Input Voltage	TTL input	2.0		VCC+0.3	V
VIL Low Level Input Voltage		-0.3		0.8	V
IIH High Level Input Current	VIH = 2.7V			20	µA
IIL Low Level Input Current	VIL = 0.4V			–1.5	mA

Filter Characteristics

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
FCA Filter *f*c Accuracy	using VFP pin	32F8011	11.7		14.3	MHz
	Rx = 0.917 kΩ	32F8012	13.5		16.5	MHz
AO VO_NORM Diff Gain	F = 0.67 *f*c, FB = 0 dB		0.8		1.20	V/V
AD VO_DIFF Diff Gain	F = 0.67 *f*c, FB = 0 dB		0.8AO		1.0AO	V/V
FBA Frequency Boost Accuracy	VBP = VR @ *f*c = 5 MHz		8.5	9.5	10.5	dB
TGD0 Group Delay Variation Without Boost*	*f*c = Max *f*c, VBP = 0V F = 0.2 *f*c to *f*c		–0.75		+0.75	ns
TGDB Group Delay Variation With Boost*	*f*c = Max *f*c, VBP = VR F = 0.2 *f*c to *f*c		–0.75		+0.75	ns
VIF Filter Input Dynamic Range	THD = 1% max, F = 0.67 *f*c (no boost)		1.5			Vpp
VOF Filter Output Dynamic Range	THD = 1% max, F = 0.67 *f*c		1.5			Vpp
RIN Filter Diff Input Resistance			3.0	3.8		kΩ
CIN Filter Diff Input Capacitance*				2.5	7	pF
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω, I*f*p = 0.8 mA, VBP = 0.0V			5.5	6.8	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*f*p = 0.8 mA, VBP = 0.0V			2.75	3.6	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω I*f*p = 0.8 mA, VBP = VR			6.0	8.1	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*f*p = 0.8 mA, VBP = VR			3.25	4.4	mVRms

* Not directly testable in production, design characteristic.

ELECTRICAL CHARACTERISTICS (continued)

Filter Characteristics (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance Single ended	Source Current (IO+) = 1 mA			60	Ω

Filter Control Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VR	Reference Voltage Output		2.0		2.40	V
I_{VR}	Reference Output Source Current				2.0	mA

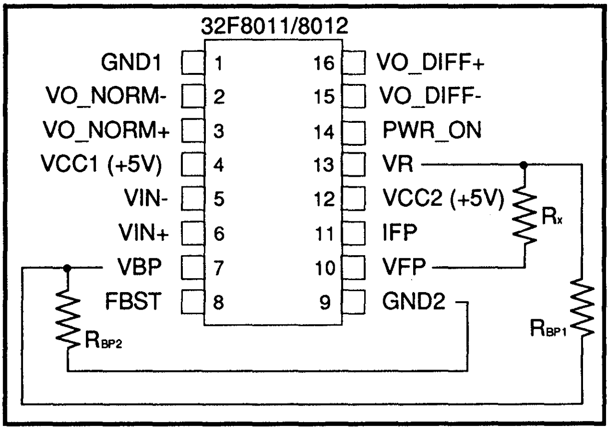


FIGURE 1: 32F8011/8012 Applications Setup, 16-Pin SO or DIP

VR = 2.2V	IVfp = 0.33VR/Rx
VFP = 0.667 VR	IVfp range: 0.31 mA to 0.8 mA (5 MHz to 13 MHz for SSI 32F8011) (6 MHz to 15 MHz for SSI 32F8012)

VFP is used when programming current is set with a resistor from VR. When VFP is used IFP must be left open.

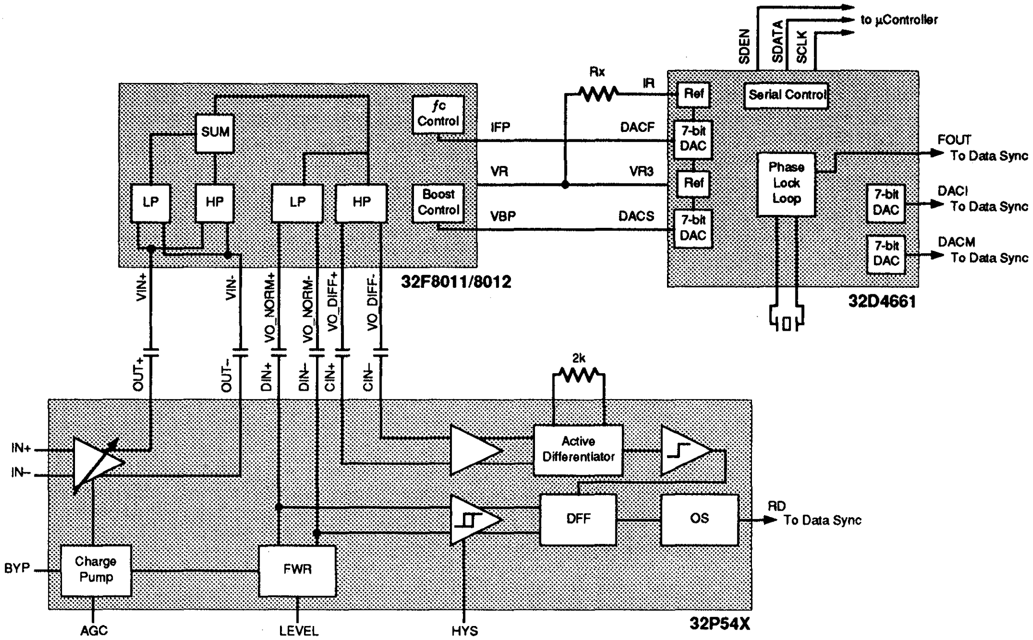


FIGURE 2: Applications Setup, Constant Density Recording
32F8011/8012, 32P54X, 32D4661

IOF = DACF output current

$IOF = (0.98F \bullet VR)/127Rx$

$Rx = (0.98F \bullet VR)/127IOF$

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

For range of Max ƒc then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

$Rx = (0.98)(2.2/0.8) = 2.7\ k\Omega$

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

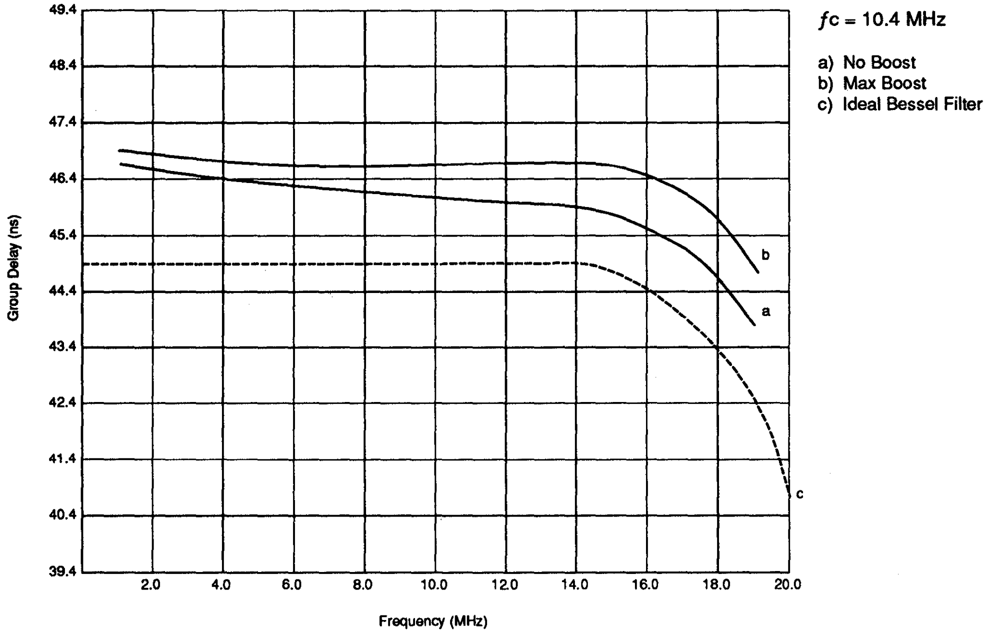


FIGURE 3: 32F8011/8012 Typical Group Delay Variation (Differentiated Output)

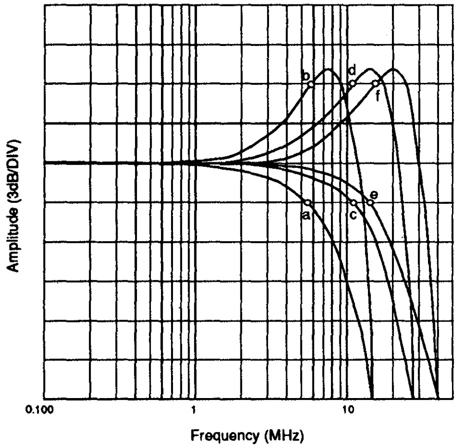


FIGURE 4: 32F8011/8012 Normal Low Pass Output Response (VO_NORM)

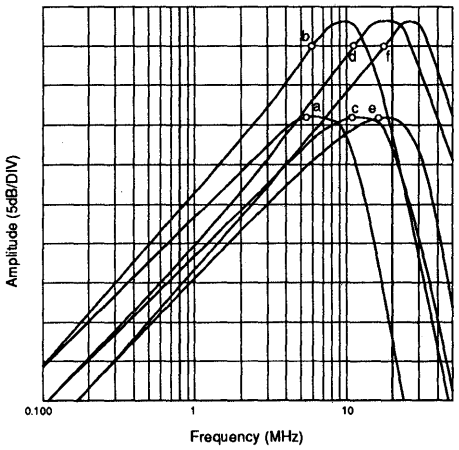
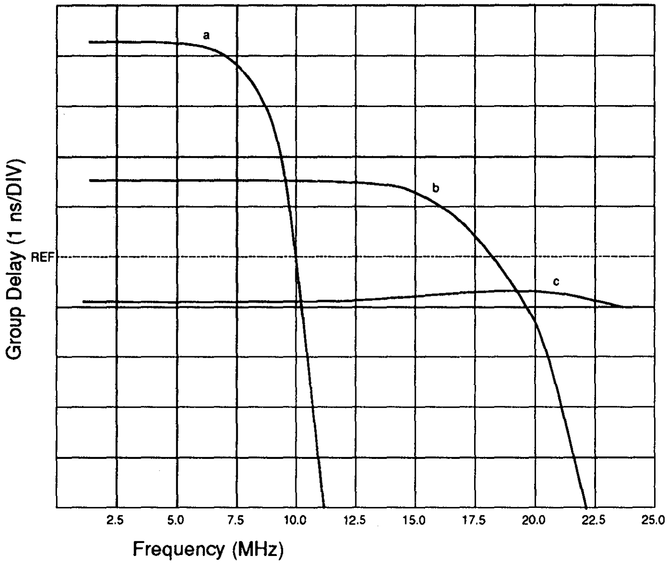


FIGURE 5: 32F8011/8012 Differented Low Pass Output Response (VO_DIFF)

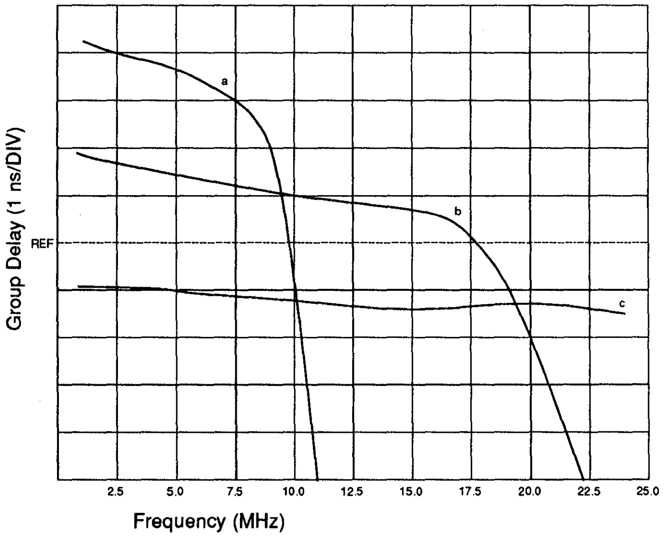
a) *fc* = 5 MHz No Boost
b) *fc* = 5 MHz Max Boost
c) *fc* = 10 MHz No Boost

d) *fc* = 10 MHz Max Boost
e) *fc* = 15 MHz No Boost
f) *fc* = 15 MHz Max Boost



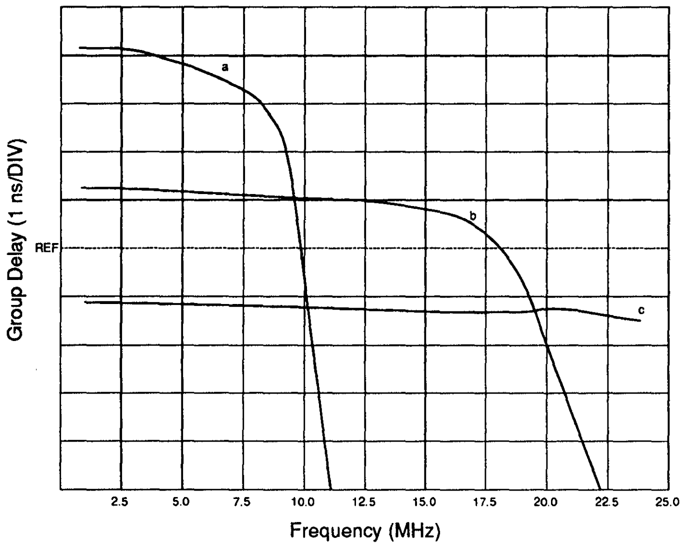
a) *fc* = 5 MHz (Ref = 80 ns)
b) *fc* = 10 MHz (Ref = 45 ns)
c) *fc* = 15 MHz (Ref = 35 ns)

FIGURE 6: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) Maximum Boost



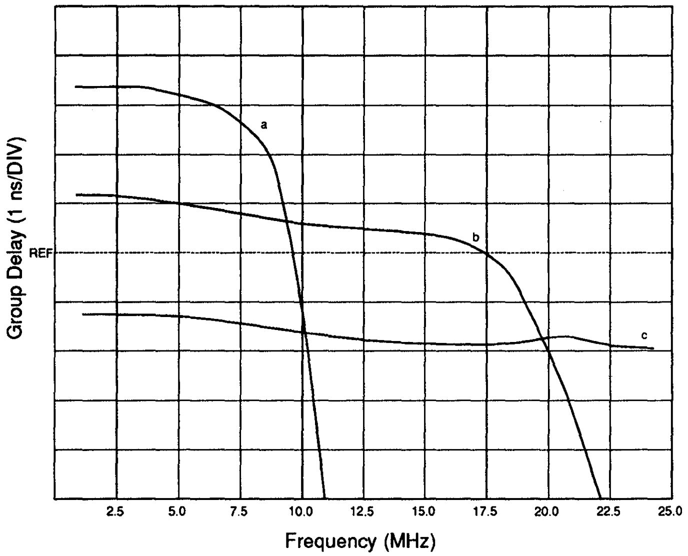
a) *fc* = 5 MHz (Ref = 80 ns)
b) *fc* = 10 MHz (Ref = 45 ns)
c) *fc* = 15 MHz (Ref = 35 ns)

FIGURE 7: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) No Boost



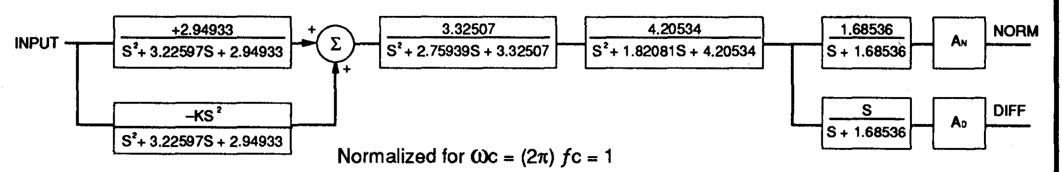
a) *fc* = 5 MHz (Ref = 80 ns)
b) *fc* = 10 MHz (Ref = 45 ns)
c) *fc* = 15 MHz (Ref = 35 ns)

FIGURE 8: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) Maximum Boost



a) *fc* = 5 MHz (Ref = 80 ns)
b) *fc* = 10 MHz (Ref = 45 ns)
c) *fc* = 15 MHz (Ref = 35 ns)

FIGURE 9: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) No Boost



Normalized for $\omega c = (2\pi)\ fc = 1$
AN and AD are adjusted for unity gain (0 dB) at $F = 0.67\ fc$
Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$
Eq for $fc = 13$ MHz, $S = S / [(2\pi)(13 \cdot 10^6)] = S / 8.16814^7$

FIGURE 12: 32F8011/8012 Normalized Block Diagram

TABLE 1: 32F8011/8012 Frequency Boost Calculations

Assuming 9.2 dB boost for VBP = VR	Boost	K	VBP/VR	Boost	K	VBP/VR
$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$	1 dB	0.36	0.065	6 dB	2.94	0.528
	2 dB	0.76	0.137	7 dB	3.65	0.658
	3 dB	1.22	0.219	8 dB	4.46	0.802
	4 dB	1.73	0.310	9 dB	5.36	0.965
	5 dB	2.30	0.413			

or,	VBP/VR	Boost	VBP/VR	Boost
boost in dB $\cong 20 \log \left[1.884 \left(\frac{VBP}{VR}\right)+1\right]$	0.1	1.499 dB	0.6	6.569 dB
	0.2	2.777 dB	0.7	7.305 dB
	0.3	3.891 dB	0.8	7.984 dB
	0.4	4.879 dB	0.9	8.613 dB
	0.5	5.765 dB	1.0	9.200 dB

TABLE 2: Calculations

Typical change in *f*-3 dB point with boost	Boost (dB)	Gain @ *fc* (dB)	Gain @ peak (dB)	fpeak/*fc*	f-3dB/*fc*
	0	-3	0.00	no peak	1.00
	1	-2	0.00	no peak	1.20
	2	-1	0.00	no peak	1.47
	3	0	0.15	0.62	1.74
	4	1	1.00	1.08	1.96
	5	2	2.12	1.24	2.13
	6	3	3.35	1.24	2.28
	7	4	4.56	1.39	2.42
	8	5	5.82	1.39	2.54
	9	6	7.04	1.39	2.66

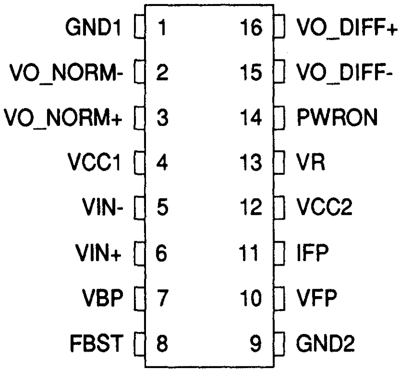
Notes:
1. *fc* is the original programmed cutoff frequency with no boost
2. *f*-3 dB is the new -3 dB value with boost implemented
3. fpeak is the frequency where the magnitude peaks with boost implemented

i.e., *fc* = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 27.69 MHz, fpeak = 16.12 MHz

SSI 32F8011/8012
Programmable
Electronic Filter

PIN DIAGRAM

(Top View)



16-pin SON, SOL

Thermal Characteristics: θjA

16-lead SON (150 mil)	105° C/W
16-lead SOL (300 mil)	100° C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8011		
16-lead SON (150 mil)	32F8011-CN	32F8011-CN
16-lead SOL (300 mil)	32F8011-CL	32F8011-CL
SSI 32F8012		
16-lead SON (150 mil)	32F8012-CN	32F8012-CN
16-lead SOL (300 mil)	32F8012-CL	32F8012-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Patent Nos. (497,863) (500,778) (516,717)

Notes:

silicon systems®
A TDK Group Company

SSI 32F8020A/8022A/8021/8023
Low-Power Programmable Electronic Filter

Preliminary Data

January 1993

DESCRIPTION

The SSI 32F8020A/8022A Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, .05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. The SSI 32F8021/8023 does not have differentiated outputs. This programability combined with low group delay variation makes the SSI 32F8020A/8022A/8021/8023 ideal for use in constant density recording applications. Double differentiation pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

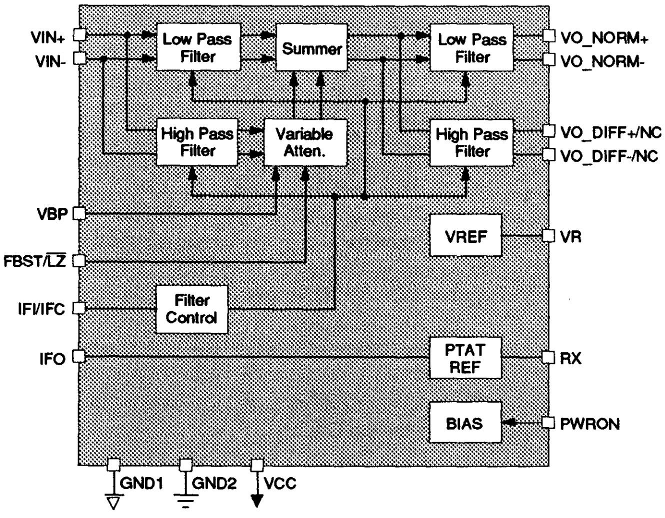
The SSI 32F8020A/8022A programmable equalization and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661

(continued)

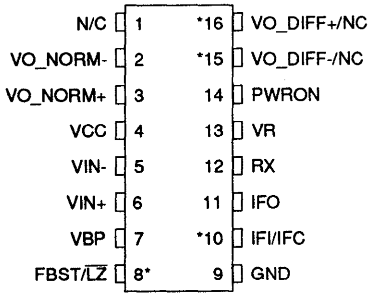
FEATURES

- **Ideal for constant density recording applications**
- **Programmable filter cutoff frequency (*f*c = 1.5 to 8 MHz)**
- **Programmable pulse slimming equalization (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs (SSI 32F8020A/8022A)**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 1.5 - 8 MHz**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-pin SON and SOL package**

BLOCK DIAGRAM



PIN DIAGRAM



* Pin 8	=	FBST - SSI 32F8020A/8021 $\overline{LZ}$ - SSI 32F8022A/8023
* Pin 10	=	IFI - SSI 32F8020A/8022A IFC - SSI 32F8021/8023
* Pin 15 & 16	=	VO_DIFF - SSI 32F8020A/8022A N/C - SSI 32F8021/8023

CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

SSI 32D4661 time base generator. Fixed characteristics are easily accomplished with three external resistors. External DACs are required for the SSI 32F8021/8023 to program the cutoff frequency. For the SSI 32F8020A/8021, equalization can be switched in or out by a logic signal.The input impedance of the SSI 32F8020A/8023 can be clamped low for fast recovery from input overload.

The SSI 32F8020A/8022A/8021/8023 require only a +5V supply and are available in 16-Lead SON and SOL packages.

FUNCTIONAL DESCRIPTION

The SSI 32F8020A/8022A/8021/8023 is a high performance programmable electronic filter. It features a 7-pole 0.05° phase equiripple filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54X family pulse detectors, and the SSI 32P4720 combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, of the SSI 32F8020A/8022A is defined as the -3dB filter bandwidth with no magnitude equalization applied, and is programmable from 1.5 MHz to 8 MHz.

The cutoff frequency is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$\mathrm{IFO} = \frac{0.75}{\mathrm{RX}} \text{ at } T = 27°\mathrm{C}$$

IFI should be made proportional to IFO for temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as follows:

$$fc(\mathrm{MHz}) = 8\mathrm{x}\frac{\mathrm{IFI}}{\mathrm{IFO}}\mathrm{x}\frac{1.25}{\mathrm{Rx}(\mathrm{k}\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(\mathrm{MHz}) = 8\,\mathrm{x}\frac{1.25}{\mathrm{Rx}(\mathrm{k}\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. The IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current from its reference to full scale output is used, a 5-kΩ RX is used. The fc is then given as follows:

$$fc(\mathrm{MHz}) = 8\mathrm{x}\frac{\mathrm{F\_Code}}{127}$$

where F_Code is the decimal code equivalent to the 7-bit digital input for the DACF. The cutoff frequency programming for the SSI 32F8021/8023 is shown in Figure 3.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 9 dB boost is applied, the magnitude response peaks up 6 dB above the DC gain.

The magnitude equalization is programmable with two pins: VR and VBP. The VR is a bandgap reference voltage, 2.2V typically. The voltage at the VBP pin determines the amount of high frequency boost. The boost function is as follows:

$$\mathrm{Boost(dB)} = 20\log_{10}[1.884(\frac{\mathrm{VBP}}{\mathrm{VR}})+1]$$

For a fixed boost setting, a resistor divider between VR to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VR should be the reference voltage to the DAC. The DAC output voltage is then proportional to VR. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters. When DACS is used, the boost relation then reduces to:

$$\mathrm{Boost(dB)} = 20\log_{10}[1.884(\frac{\mathrm{S\_Code}}{127})+1]$$

where S_Code is the decimal code equivalent to the 7-bit digital input for the DACS.

For the SSI 32F8020A/8021, the equalization function can be disabled when FBST is pulled to logic 0. For the SSI 32F8022A/8023, the VBP pin should be grounded to achieve 0 dB boost.

LOW INPUT IMPEDANCE (SSI 32F8022A/8023 only)

When the LZ is at logic 1 or left open, the SSI 32F8022A/8023 input is at high impedance state. When the LZ is pulled to logic 0, the SSI 32F8022A/8023 input is clamped to a low impedance state, 200 Ω typical.

POWER ON/OFF

The SSI 32F8020A/8022A/8021/8023 support a power down mode for minimal idle dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS.
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS.
RX	PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pin.
IFO	PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFI.
IFI	FREQUENCY PROGRAM INPUT. The filter cutoff frequency fc, is set by an external current IFI, injected into this pin. IFI must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO.
VBP	FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST (32F8020A/8021)	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. No boost is applied if the FBST pin is grounded, or at logic low.
$\overline{LZ}$ (32F8022A /8023)	LOW IMPEDANCE MODE. With a low logic level, the analog input impedance is switched low for fast recovery from input overload. With a high logic level or left open, the input is at high impedance state.
PWRON	POWER ON. A high logic level circuit enables the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC	+5 VOLT SUPPLY.
GND	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150 °C
Junction Operating Temperature, Tj	+130 °C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs	-0.5 to VCCV
Maximum Power Dissipation, fc = 8 MHz, Vcc = 5.5V	226 mW

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.50 < VCC < 5.50V
Ambient Temperature	0 < Ta < 70 °C

Power Supply Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC Power Supply Current	PWRON ≤ 0.8V			0.5	mA
	PWRON ≥ 2.2V SSI 32F8021/8023		26	32	mA
	PWRON ≥ 2.2V SSI 32F8020A/8022A		35	41	mA
PD Power Dissipation	PWRON ≤ 0.8V			3	mW
	PWRON ≥ 2.2V, VCC = 5V SSI 32F8021/8023		130	160	mW
	PWRON ≥ 2.2V, VCC = 5.5V SSI 32F8021/8023		143	176	mW
	PWRON ≥ 2.2V, VCC = 5V SSI 32F8020A/8022A		175	205	mW
	PWRON ≥ 2.2V, VCC = 5.5V SSI 32F8020A/8022A		193	226	mW

DC Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VIH High Level Input Voltage	TTL input	2.0			V
VIL Low Level Input Voltage				0.8	V
IIH High Level Input Current	VIH = 2.7V			20	µA
IIL Low Level Input Current	VIL = 0.4V			–1.5	mA
VICM VIN± Input Common Mode Voltage		(VCC -1.6) -0.25		(VCC -1.6) +0.25	V
VOCM VO_NORM± Output Common Mode Voltage		1.8		3.8	V
VOFFVO_NORM± Output Offset	VIN± open	-0.15		+0.25	V

Filter Characteristics

fc Filter Cutoff Frequency	Rx = 5kΩ $fc\ (\text{MHz}) = 8 \bullet \frac{\text{IFI}}{4 \bullet \text{IFO}}$ (32F8020A/8022A) $fc\ (\text{MHz}) = 8 \bullet \frac{\text{IFC}}{4 \bullet \text{IFO}}$ (32F8021/8023)	1.5		8.0	MHz
FCA Filter *fc* Accuracy	*fc* (nominal) = 8 MHz	–10		+10	%
AO VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.8	0.9	1.0	V/V
AD VO_DIFF Diff Gain (32F8020A/8022A)	F = 0.67 *fc*, FB = 0 dB	0.8AO		1.2AO	V/V
FB Frequency Boost at *fc*	$\text{FB(db)} = 20 \log \left[1.884 \left(\frac{\text{VBP}}{\text{VR}} \right) + 1 \right]$ VBP = VR		9.2		dB
FBA Frequency Boost Accuracy	FB (ideal) = 9.0 dB	–1		+1	dB
TGD0 Group Delay Variation Without Boost	*fc* = 8 MHz, VBP = 0V F = 0.2 *fc* to 1.75 *fc*	–1.3		+1.3	ns
	fc = 1.5 MHz - 8 MHz F = 0.2 *fc* to 1.75 *fc*, VBP = 0V	–2		+2	%
TGDB Group Delay Variation With Boost	*fc* = 8 MHz, VBP = VR F = 0.2 *fc* to 1.75 *fc*	–1.3		+1.3	ns
	fc = 1.5 MHz - 8 MHz F = 0.2 *fc* to 1.75 *fc*, VBP = VR	–2		+2	%
VIF Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp

ELECTRICAL SPECIFICATIONS (continued)

Filter Characteristics (continued)

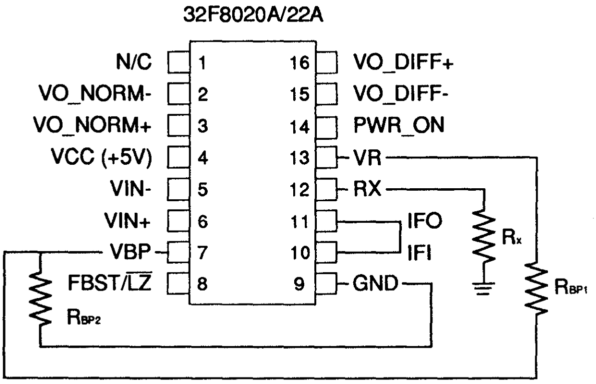
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VOF Filter Output Dynamic Range	THD = 1% max, F = 0.67 *f*c	1.0			Vpp
VIF Filter Input Dynamic Range	THD = 1.5%, F = 0.67 *f*c	1.5			Vpp
VOF Filter Output Dynamic Range	THD = 1.5%, F = 0.67 *f*c	1.5			Vpp
VIF Filter Input Dynamic Range	THD = 3% max, F = 0.67 *f*c	2.0			Vpp
VOF Filter Output Dynamic Range	THD = 3% max, F = 0.67 *f*c	2.0			Vpp
RIN Filter Diff Input Resistance	32F8020A/8021 32F8022A/8023 LZ = 1 or open	3.0	4.0		kΩ
	32F8022A/8023 LZ = 0		200	400	Ω
CIN Filter Input Capacitance				7	pF
EOUT Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *f*c = 8 MHz, VBP = 0.0V (32F8020A/8022A)		6.3	7.5	mVRms
EOUT Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *f*c = 8 MHz, VBP = 0.0V		2.7	4.0	mVRms
EOUT Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *f*c = 8 MHz, VBP = VR (32F8020A/8020A)		9.4	11.0	mVRms
EOUT Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *f*c = 8 MHz, VBP = VR		3.7	4.5	mVRms
IO– Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		2.0			mA
RO Filter Output Resistance (Single ended)	IO+ = 1.0 mA			60	Ω

Filter Control Characteristics

VR Reference Voltage		2.0		2.40	V
VBP Frequency Boost Control Voltage Range	VR = 2.2V FBOOST = 0 to 9.2 dB	0		2.2	V
VRX PTAT Reference Current Set Output Voltage	TA = 25°C IRX = 0 - 0.6 mA Rx > 1.25 kΩ		750		mV
IFO PTAT Reference Current, Output Current Range	TA = 25°C 1.25 kΩ < Rx < 6.8 kΩ IFO = VRX/Rx VRX = 750 mV	0.11		0.6	mA
RIFO IFO Output Impedance		50			kΩ
VIFO IFO Voltage Compliance		0		Vcc -1	V

Filter Control Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IFI PTAT Programming Current Range	TA = 25°C, VRX = 750 mV 32F8020A/8022A	0.11		0.6	mA
RIFI IFI Input Impedance	32F8020A/8022A	1.0		2.5	kΩ
VIFI IFI Voltage Compliance	32F8020A/8022A	0.5		2.5	V
IFC PTAT Programming Current Range	TA = 25 °C, VRX = 750 mV 32F8021/8023	0.11		0.6	mA
TPWRPower On Recovery Time	DC voltages within 20 mV of final values			300	ns
TBST Boost Change Recovery	DC voltages within 20 mV of final values			300	ns
TFBW Bandwidth Change Recovery	DC voltages within 20 mV of final values			300	ns



VR = 2.2V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

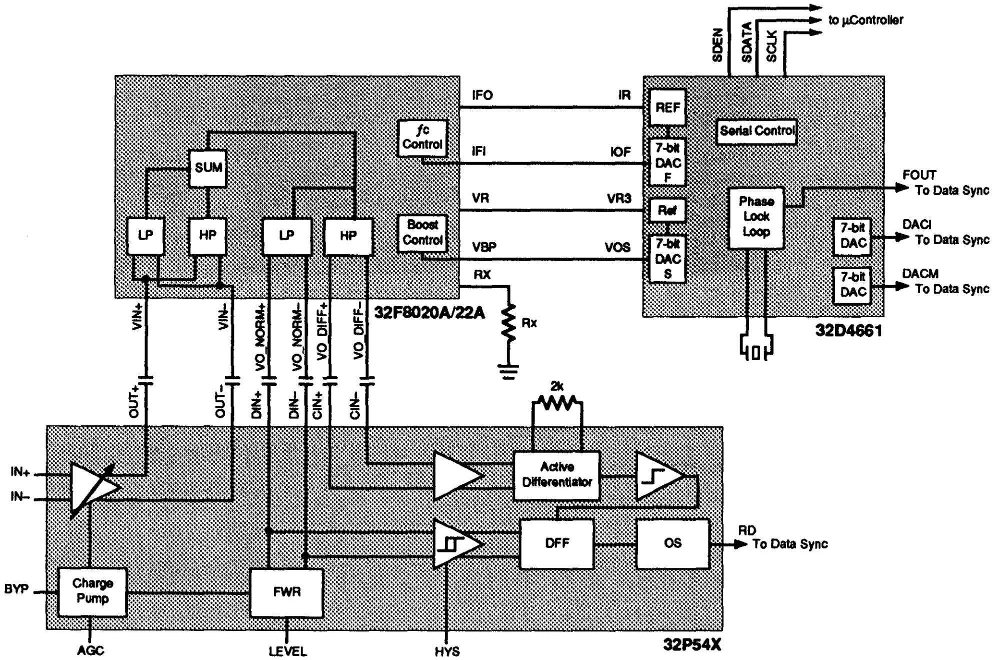
Fixed frequency programming is accomplished as shown in the drawing above. In this case IFI (programming current) is equivalent to IFO (reference current). Programming current is then set by VRX/Rx.

where: fc = 8.0 MHz then

IFI = IFO = 0.60 mA @25 °C

Rx = 750 mV/0.60 mA = 1.25 kΩ

FIGURE 1: 32F8020A/8022A Applications Setup



VR = 2.2V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

In this case the IFI (programming current) is scaled from IFO (reference current) through DACF on the 32D4661. DACF has a current gain of 4; therefore, the reference current should be set to 25% of the maximum desired IFI (programming current).

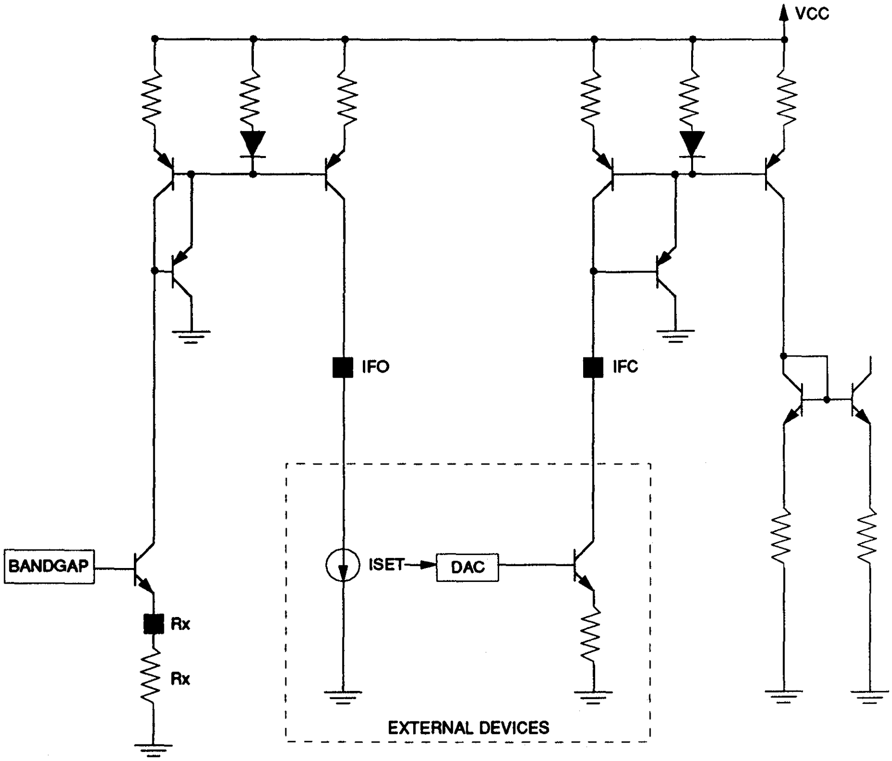
where: *fc* (max) = 8.0 MHZ then

IFI (max) = 0.60 mA @25°C

IFO (max) = 0.15 mA

therefore Rx = 750 mV/0.15 mA = 5 kΩ

FIGURE 2: Applications Setup, Constant Density Recording 32F8020A/8022A, 32P54X, 32D4661



VRX = 750 mV @25°C

IRX = IFO

IFC programming range: 0.11 mA to 0.60 mA @25°C
(1.5 to 8.0 MHz: No Boost)

The IFC (programming current) is scaled from IFO (reference current) by the set-up shown above. Assuming the DAC current gain = 4.0, then programming is accomplished as follows:

MAX programming current required: IFC = 0.6 mA (*fc* = 8.0 MHz) @25°C

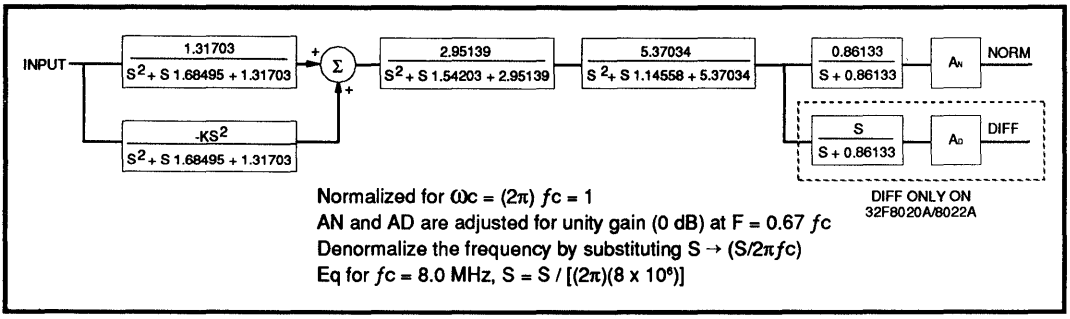
IFO = IFC/8 = 0.075 mA (MAX) @25°C

IRX = IFO

IRX = 750mV/Rx @25°C

Rx = 5 kΩ

FIGURE 3: 32F8021/8023 Frequency Programming



Normalized for $\omega c = (2\pi) fc = 1$
AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc
Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$
Eq for fc = 8.0 MHz, $S = S / [(2\pi)(8 \times 10^6)]$

FIGURE 4: 32F8020A/8022A/8021/8023 Normalized Block Diagram

TABLE 1: 32F8020A/8022A Frequency Boost Calculations

Assuming 9.2 dB boost for **VBP = VR**	**Boost**	**VBP/VR**	**K**
$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$	1 dB	0.065	0.16
	2 dB	0.137	0.34
	3 dB	0.219	0.54
	4 dB	0.310	0.77
	5 dB	0.413	1.03
	6 dB	0.528	1.31
	7 dB	0.658	1.63
	8 dB	0.802	1.99
	9 dB	0.965	2.40

or,	**VBP/VR**	**Boost**
boost in dB $\cong 20 \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$	0.1	1.499 dB
	0.2	2.777 dB
	0.3	3.891 dB
	0.4	4.879 dB
	0.5	5.765 dB
	0.6	6.569 dB
	0.7	7.305 dB
	0.8	7.984 dB
	0.9	8.613 dB
	1.0	9.200 dB

TABLE 2: Calculations

Typical change in *f*-3 dB point and frequency peak with boost.

Boost (dB)	Gain@*f*c (dB)	Gain@peak (dB)	*f*peak/*f*c	*f*-3 dB/*f*c
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59

NOTES:
1. *f*c is the original programmed cutoff frequency with no boost.
2. *f*-3 dB is the new -3 dB value with boost implemented.
3. *f*peak is the frequency where the magnitude peaks when boost is implemented.

i.e., *f*c = 8 MHz when boost = 0 dB if boost is programmed to 5 dB then
f-3 dB = 17.6 MHz
*f*peak = 9.84 MHz

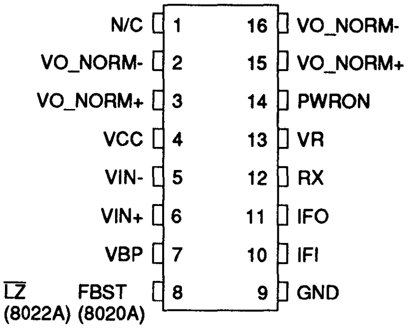
SSI 32F8020A/8022A/8021/8023
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS

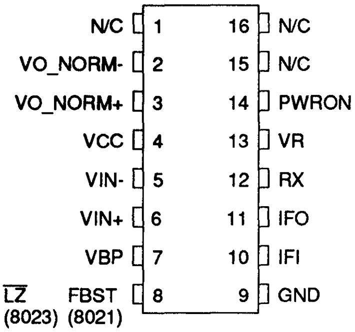
(Top View)

THERMAL CHARACTERISTICS: θja

16-Lead SOL (150 mil)	105° C/W
20-Lead SOV (300 mil)	100° C/W



32F8020A/8022A
16-Lead SON, SOL



32F8021/8023
16-Lead SON, SOL

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8020A	16-Lead SON	32F8020A-CN	32F8020A-CN
	16-Lead SOL	32F8020A-CL	32F8020A-CL
SSI 32F8022A	16-Lead SON	32F8022A-CN	32F8022A-CN
	16-Lead SOL	32F8022A-CL	32F8022A-CL
SSI 32F8021	16-Lead SON	32F8021-CN	32F8021-CN
	16-Lead SOL	32F8021-CL	32F8021-CL
SSI 32F8023	16-Lead SON	32F8023-CN	32F8023-CN
	16-Lead SOL	32F8023-CL	32F8023-CL

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Patent Pending - (497,863), (500,778)

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SSI 32F8030
Programmable Electronic Filter

June 1992

DESCRIPTION

The SSI 32F8030 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, 0.05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programability, combined with low group delay variation makes the SSI 32F8030 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

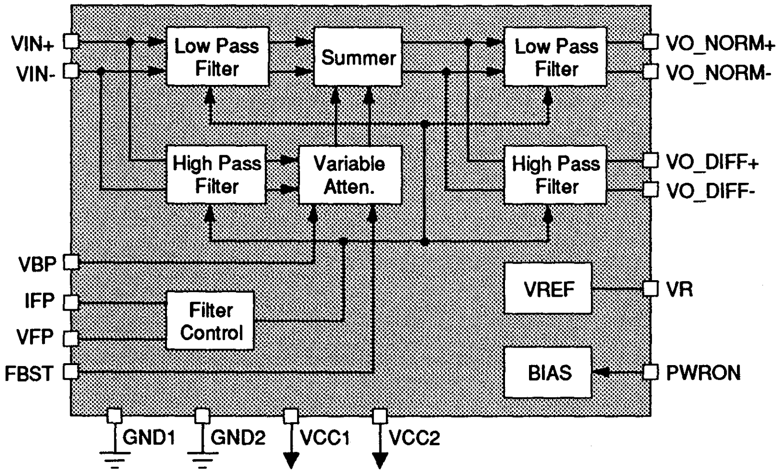
The SSI 32F8030 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors. In addition, boost can be switched in or out by a logic signal.

The SSI 32F8030 requires only a +5V supply and is available in 16-Lead SON, and SOL packages.

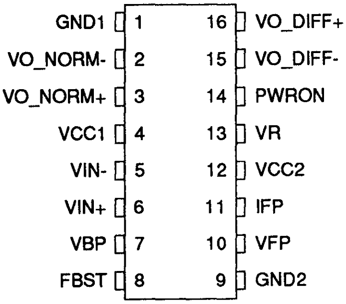
FEATURES

- **Ideal for:**
  - **- constant density recording applications**
  - **- magnetic tape recording**
- **Programmable filter cutoff frequency (fc = 250 kHz to 2.5 MHz)**
- **Programmable high frequency peaking (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±3.0% group delay variation from 0.2 fc to 1.75 fc, 0.25 MHz $\leq fc \leq$ 2.5 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-Lead SON, and SOL packages**
- **5 mW idle mode**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8030
Programmable
Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8030, a high performance programmable electronic filter, provides a low pass 0.05° Equiripple-type linear phase seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4720 Combo device (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8030 programmable electronic filter can be set to a filter cutoff frequency from 250 kHz to 2.5 MHz (with no boost).

Cutoff frequency programming can be established using either a current source fed into the IFP pin, whose output current is proportional to the SSI 32F8030 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8030. This reference voltage is an internally generated bandgap reference, which typically varies less than 1 % over voltage supply and temperature variation. (For the calculations below IVFP = current into IFP or VFP pins).

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10kHz), is related to the current IVFP injected into pin IFP by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•IVFP•2.2/VR, where IFP and IVFP are in mA, 0.08<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8030 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•2.2/(3•Rx) where Rx is in kΩ, & 0.917 kΩ <Rx<9.17 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the output signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = 20 $\log_{10}$[1.884(VBP/VR)+1], where 0<VBP<VR.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector.
IFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin.
VBP	FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level enables the chip. A low level puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC1, VCC2	+5 VOLT SUPPLY.
GND1, GND2	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC1, VCC2	-0.5 to 7V
Voltage Applied to Inputs	-0.5 to VCC + 0.5V
IFP, VFP Inputs Maximum Current	≤1.2 mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply voltage, VCC1, VCC2	4.5 < VCC1,2 < 5.50V
Ambient Temperature	0 < Ta < 70°C

ELECTRICAL SPECIFICATIONS

Power Supply Characteristics

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC Power Supply Current	PWRON ≤ 0.8V			0.5	mA
ICC Power Supply Current	PWRON ≥ 2.0V		28	42	mA
PD Power Dissipation	PWRON ≥ 2.0V		140	231	mW
PD Power Dissipation	PWRON ≤ 0.8V			3	mW

DC Characteristics

VIH High Level Input Voltage	TTL input	2.0		VCC+0.3	V
VIL Low Level Input Voltage		-0.3		0.8	V
IIH High Level Input Current	VIH = 2.7V			20	µA
IIL Low Level Input Current	VIL = 0.4V			–1.5	mA

Filter Characteristics

fc = 1.25 MHz unless otherwise stated

FCA Filter *fc* Accuracy	using IFP pin: IFP = 0.4 mA or using VFP pin: Rx = 1.84 kΩ	1.125		1.375	MHz
AO VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.8		1.20	V/V
AD VO_DIFF Diff Gain	F = 0.67 *fc*, FB = 0 dB	0.9AO		1.1AO	V/V
FBA Frequency Boost Accuracy	VBP = VR	8.0	9.2	10.4	dB
TGD0 Group Delay Variation Without Boost*	0.25 MHz ≤ *fc* ≤ 2.5 MHz F = 0.2 *fc* to 1.75 *fc*	–3		+3	%
TGDB Group Delay Variation With Boost*	0.25 MHz ≤ *fc* ≤ 2.5 MHz VBP = VR, F = 0.2 *fc* to 1.75 *fc*	–3		+3	%
VIF Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc* (no boost, 1000 pF capacitor across Rx)	1.0			Vpp
VOF Filter Normal Output Dynamic Range	THD = 1% max, F = 0.67 *fc* VBP = 0 (1000 pF capacitor across Rx)	1.0			Vpp
VOF Filter Normal Output Dynamic Range	THD = 1% max, F = 0.67 *fc* VBP = VR (1000 pF capacitor across Rx)	1.0			Vpp
VOF Filter Differentiated Output Dynamic Range	THD = 1% max, F = 0.67 *fc* VBP = 0 (1000 pF capacitor across Rx)	1.0			Vpp
VOF Filter Differentiated Output Dynamic Range	THD = 1% max, F = 0.67 *fc* VBP = VR (1000 pF capacitor across Rx)	1.0			Vpp

Filter Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RIN Filter Diff Input Resistance		3.0	4.0	5.0	kΩ
CIN Filter Diff Input Capacitance*			3.0		pF
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω, Ifp = 0.8 mA, VBP = 0.0V		2.7	3.2	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = 0.0V		1.6	2.0	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = VR		3.1	3.8	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = VR		1.8	2.2	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 10 MHz, Rs = 50Ω, Ifp = 0.08 mA, VBP = 0.0V		1.8	2.1	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = 0.0V		1.0	1.2	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = VR		2.0	2.5	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = VR		1.1	1.5	mVRms
IO- Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		2.0			mA
RO Filter Output Resistance**	Sinking 1 mA from pin			70	Ω

* Not directly testable in production, design characteristic.
** Single ended

Filter Control Characteristics

VR Reference Voltage Output		2.0		2.40	V
I_{VR} Reference Output Source Current				2.0	mA

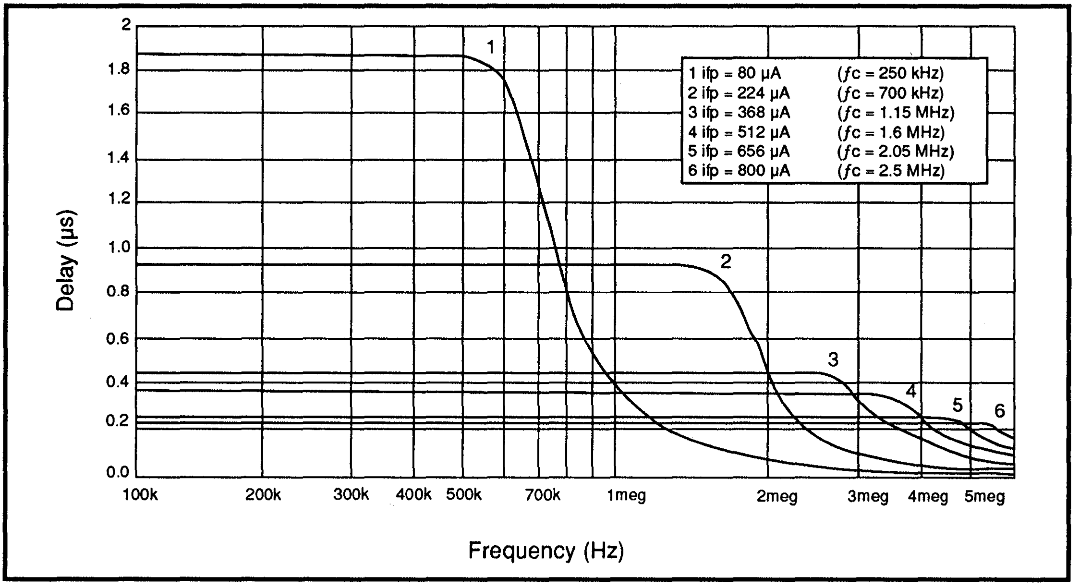


FIGURE 1: Typical Normal/Differentiated Output Group Delay Response

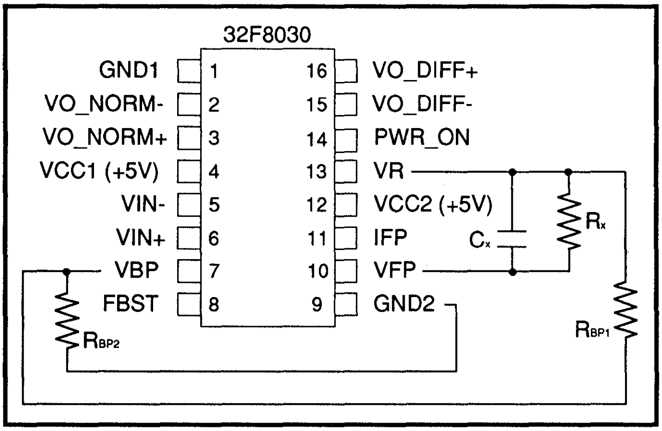
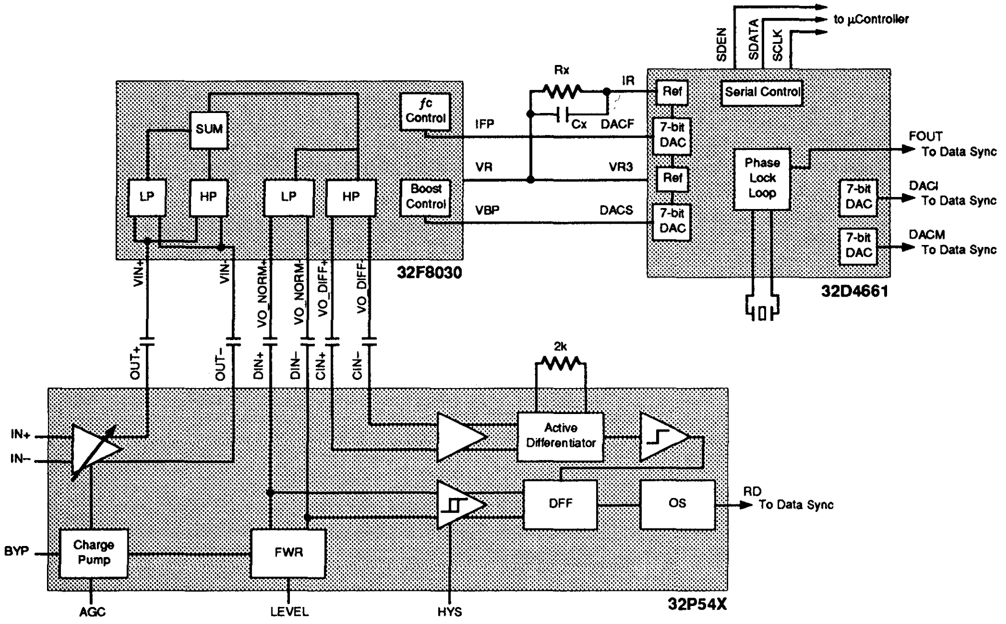


FIGURE 1: 32F8030 Applications Setup 16-Pin SO

VR = 2.2V	IVfp = .33VR/Rx
VFP = .667 VR	IVfp range: 0.08 mA to 0.8 mA (0.25 MHz to 2.5 MHz)

Cx = 1000 pF needed for THD at low ƒc

VFP is used when programming current is set with a resistor from VR. When VFP is used IFP must be left open.



IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

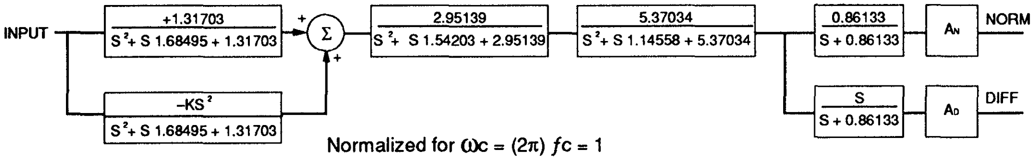
For range of Max *fc* = 2.5 MHz then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

FIGURE 2: Applications Setup, Constant Density Recording 32F8030, 32P54X, 32D4661



Normalized for $\omega c = (2\pi)\ fc = 1$

AN and AD are adjusted for unity gain (0 dB) at F = 0.67 *fc*

Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$

Eq for $fc = 2.5$ MHz, $S = S / [(2\pi)(2.5 \cdot 10^6)] = S / (1.57080 \cdot 10^7)$

FIGURE 3: 32F8030 Normalized Block Diagram

TABLE 1: 32F8030 Frequency Boost Calculations

	Boost	K	VBP/VR	Boost	K	VBP/VR
Assuming 9.2 dB boost for VBP = VR $\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$	1 dB	0.16	0.065	6 dB	1.31	0.288
	2 dB	0.34	0.137	7 dB	1.63	0.358
	3 dB	0.54	0.219	8 dB	1.99	0.437
	4 dB	0.77	0.310	9 dB	2.40	0.526
	5 dB	1.03	0.413			

or,	VBP/VR	Boost	VBP/VR	Boost
$\text{boost in dB} = 20\log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$	0.1	1.499 dB	0.6	6.569 dB
	0.2	2.777 dB	0.7	7.305 dB
	0.3	3.891 dB	0.8	7.984 dB
	0.4	4.879 dB	0.9	8.613 dB
	0.5	5.765 dB	1.0	9.200 dB

TABLE 2: Calculations

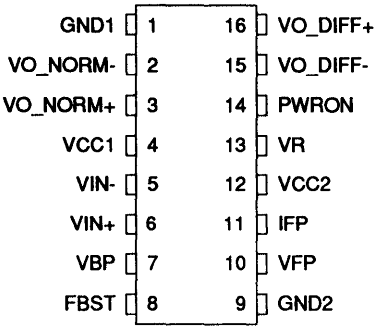
Typical change in ƒ-3 dB point with boost	Boost (dB)	Gain @ ƒc(dB)	Gain @ peak(dB)	ƒpeak/ƒc	f-3 dB/ƒc
	0	-3	0.00	no peak	1.00
	1	-2	0.00	no peak	1.21
	2	-1	0.00	no peak	1.51
	3	0	0.15	0.70	1.80
	4	1	0.99	1.05	2.04
	5	2	2.15	1.23	2.20
	6	3	3.41	1.33	2.33
	7	4	4.68	1.38	2.43
	8	5	5.94	1.43	2.51
	9	6	7.18	1.46	2.59

Notes: 1. ƒc is the original programmed cutoff frequency with no boost
2. ƒ-3 dB is the new -3 dB value with boost implemented
3. ƒpeak is the frequency where the magnitude peaks with boost implemented

i.e., ƒc = 2.5 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 5.5 MHz
ƒpeak = 3.075 MHz

PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON, SOL

Thermal Characteristics: θjA

16-lead SON (150 mil)	105° C/W
16-lead SOL (300 mil)	100° C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
16-lead SON (150 mil)	32F8030-CN	32F8030-CN
16-lead SOL (300 mil)	32F8030-CL	32F8030-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Notes:

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SSI 32F8101/8102/8103/8104
Low-Power Programmable Filter

Target Specification

January 1993

DESCRIPTION

The 32F810X is a high performance, low power, digitally programmable low-pass filter for applications requiring variable-frequency filtering. The device consists of three functional blocks: [1] a 7th-order 0.05° Equiripple Low-Pass filter, [2] two DACs for controlling the filter cutoff frequency and high-frequency peaking (boost), and [3] a Serial Port for programming the *fc* and Boost DACs. The device is offered in four frequency options: the 32F8101, 9-27 MHz; 32F8102, 6-18 MHz; 32F8103, 4-12 MHz; & 32F8104, 3-9 MHz.

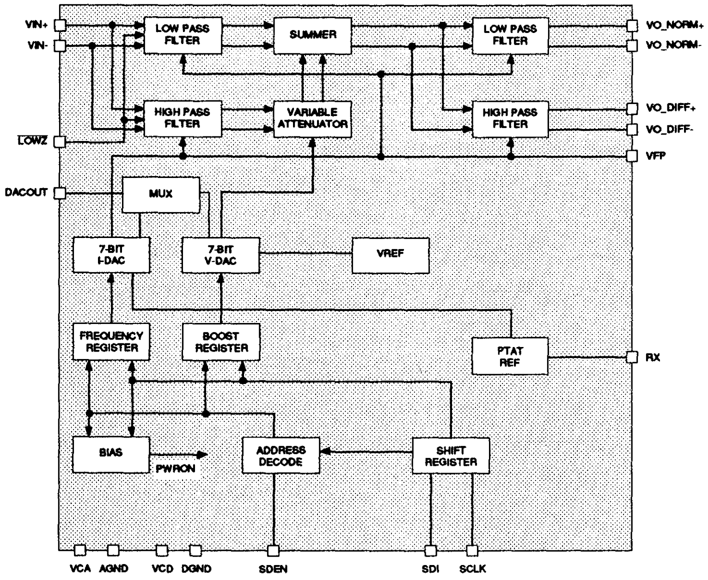
Cutoff frequency and boost are controlled by the two on-chip 7-bit DACs, which are programmed via the 3-line serial interface. Boost is programmable from 0 to 13 dB nominally, and is implemented using two symmetrical, real-axis zeroes. Both boost and *fc* control do not affect the flat group delay response.

The 32F81XX device is ideal for variable data rate and variable frequency shaping applications. It requires only a +5V supply and has an Idle mode for minimal power dissipation. The SSI 32F810X is available in 16-lead SON, and 20-Lead SOV packages.

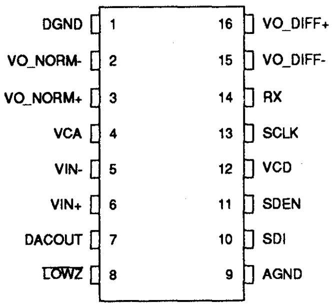
FEATURES

- **Programmable cutoff frequency:**
  - **32F8101 - 9 to 27 MHz**
  - **32F8102 - 6 to 18 MHz**
  - **32F8103 - 4 to 12 MHz**
  - **32F8104 - 3 to 9 MHz**
- **Programmable boost/equalization of 0 to 13 dB**
- **Matched normal and differentiated outputs**
- **± 10% *fc* accuracy**
- **± 2% maximum group delay variation**
- **Less than 1% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOWZ}}$ pin**
- **No external filter components required**

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F810X programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. High-frequency boost equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $Wc = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks2 + 17.98016)/D(s)] \times An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times Ad$$

Where D (s)=
$(S^2+1.68495s+1.31703)(S^2+1.54203\,s+2.95139)$
$(S^2+1\,.4558s+5.37034)(s+0.86133)$,

An and Ad are adjusted for a gain of 2 at $fs=(2/3)fc$.

Filter Operation

Normally AC coupled differential signals are applied to the FIP/FIN inputs of the filter, although DC coupling can be implemented. To improve settling time of the coupling capacitors, the FIP/FIN inputs are placed into a Low-Z state when the $\overline{\text{LOWZ}}$ pin is brought high. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 12.1 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control: The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

fc = 0.2126 x DACF (MHz) for the 32F8101
fc = 0.1417 x DACF (MHz) for the 32F8102
fc = 0.09449 x DACF (MHz) for the 32F8103
fc = 0.07087 x DACF (MHz) for the 32F8104
where DACF = Cutoff Frequency Control Register value (decimal)

The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3dB frequency.

TABLE 1: 3dB Cutoff Frequency Versus Boost Magnitude

BOOST (dB)	fc (3 dB)	BOOST (dB)	fc (3 dB)
0	1.00	7	2.41
1	1.22	8	2.53
2	1.47	9	2.65
3	1.74	10	2.73
4	1.95	11	2.81
5	2.13	12	2.88
6	2.28	13	2.96

Boost/Equalization Control

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost = 20 log [(0.0273 x FBCR) + 1] (dB)

For example, with the DAC set for maximum output (FBCR = 7Fhex or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the 32F810X. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin.

After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining seven bits determine the internal register to be accessed. The second byte contains the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

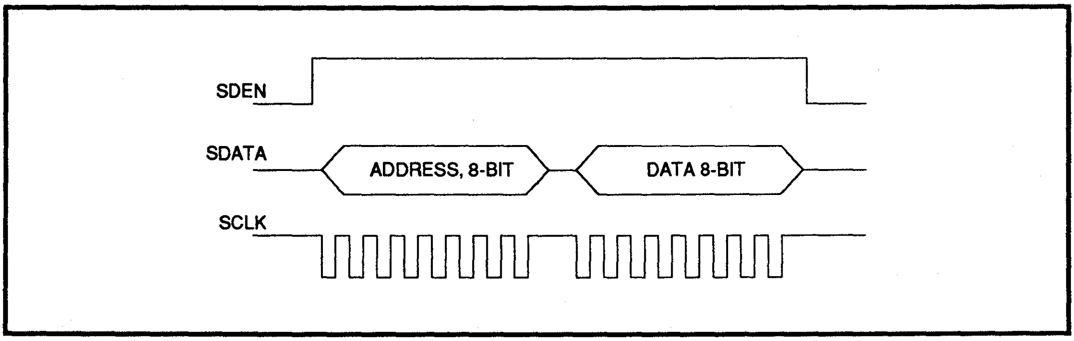


FIGURE 1: Serial Port Data Transfer Format

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VCA	-	Filter analog power supply pin
VCD	-	Serial port power supply pin
AGND	-	Filter analog ground pin
DGND	-	Serial port digital ground pin

INPUT PINS

VIN+, VIN-	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.

OUTPUT PINS

VO_DIFF+, VO_DIFF-	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentated outputs. These outputs are normally AC coupled.
VO_NORM+, VO_NORM-	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are normally AC coupled.
DACOUT	O	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register.
RX	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

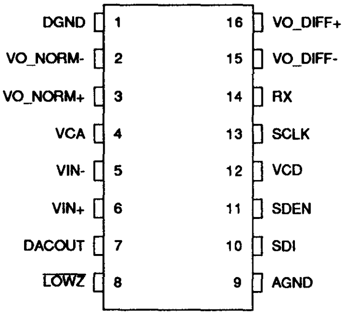
SDEN	I/O	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level TTL input enables the serial port.
SDI	I/O	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I/O	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

PACKAGE PIN DESIGNATIONS

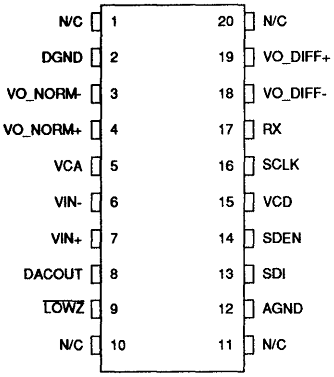
(Top View)

THERMAL CHARACTERISTICS: θja

16-lead SON	100° C/W
20-lead SOV	125° C/W



16-Lead SON



20-Lead SOV

Target Specification: The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32F8120
Low-Power Programmable Electronic Filter
Preliminary Data

December 1992

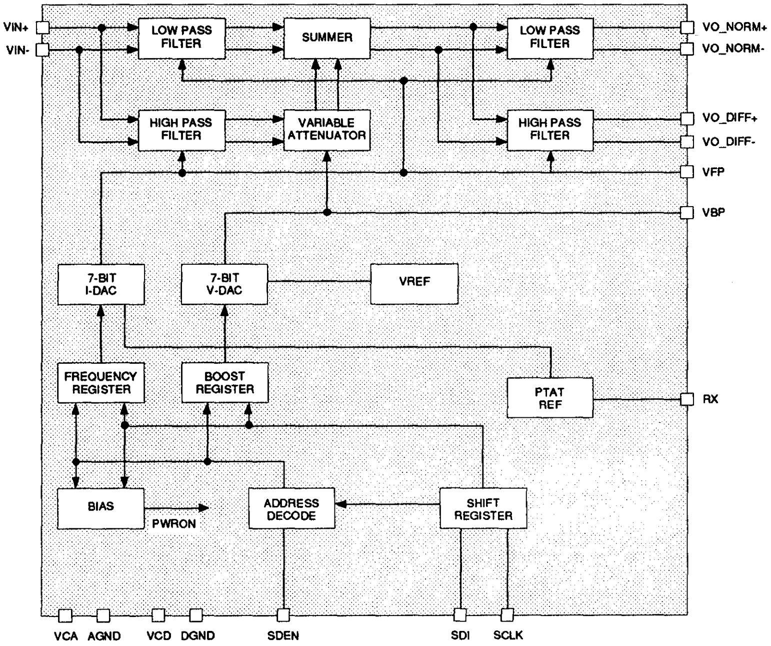
DESCRIPTION

The SSI 32F8120 is a continuous time, low pass filter with programmable bandwidth and high frequency boost. The low pass filter is a 2 zero / 7 pole 0.05° phase equiripple type, featuring excellent group delay characteristics. It features 1.5 - 8 MHz programmable bandwidth and 0-10 dB programmable boost. Both functions are controlled by 7-bit command words, which are input via a 3-line serial interface.

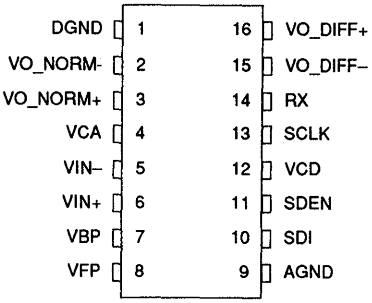
FEATURES

- **Programmable filter cutoff frequency (*fc* =1.5 to 8 MHz) with no external components**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **± 10% cutoff frequency accuracy**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device idle mode**
- **+5V only operation**
- **No external filter components required**
- **Supports constant density recording**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8120 programmable electronic filter can be set to a filter cutoff frequency from 1.5 to 8 MHz. The cutoff frequency can be set by using the serial port through pins SDI, SDEN, and SCLK. SDI is the serial data input for an 8-bit control shift register, SDEN is the control register enable, and SCLK is the control register clock. The data packet is transmitted MSB (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. See Table 1.

fc is determined by the equation:

$fc\ (\text{MHz}) = 0.061321\ (\text{F\_Code}) + 0.212264$

$1.5\ \text{MHz} \leq fc \leq 8\ \text{MHz}$

$21 \leq \text{F\_ Code} \leq 127$

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the V-DAC output, the boost can be determined. The amount of boost at the cutoff frequency is related to the V-DAC output by the following formula:

$$[\text{Ouput of V}-\text{DAC} = \text{VBP} = \text{VREF x } \frac{\text{S\_Code}}{127}]$$

BOOST (dB) = 20•log [0.01703 (S_Code) +1].

TABLE 1

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
X	0	0	0	S-MSB REGISTER	X	S6	S5	S4
X	0	0	1	S-LSB REGISTER	S3	S2	S1	S0
X	0	1	0	F-MSB REGISTER	X	F6	F5	F4
X	0	1	1	F-LSB REGISTER	F3	F2	F1	F0
X	1	1	1	P REGISTER	X	X	X	P0

X = Don't Care
S = 7-bit Boost (Slimming) Control
F = 7-bit Frequency (Bandwidth) Control
P = Power Down Control; PO = 1 for power up; PO = 0 for power down

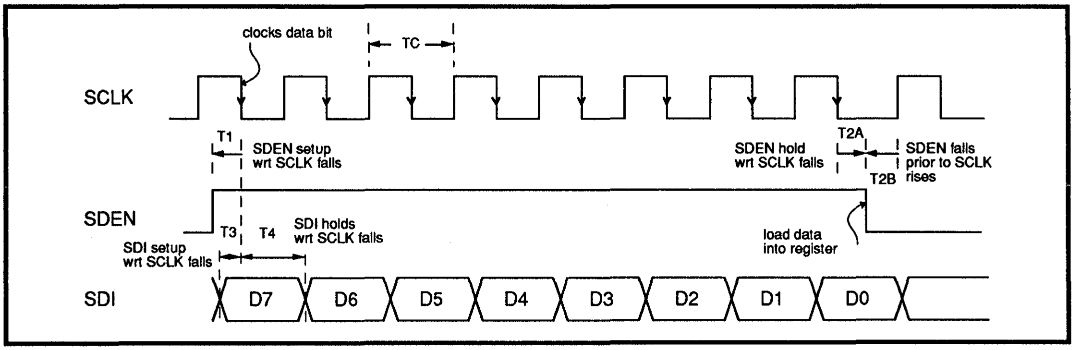


FIGURE 1: Serial Port Timing Diagram

PIN DESCRIPTIONS

NAME	TYPE	DESCRIPTION
VIN+, VIN–	I	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	O	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the pulse detector.
VO_DIFF+ VO_DIFF–	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum pulse pairing, these outputs should be AC coupled to the pulse detector.
SDEN	I	SERIAL DATA ENABLE. A logic HIGH level allows SERIAL CLOCK to clock data into the control register via the SERIAL DATA input. A logic LOW level latches the register data and issues the information to the appropriate circuitry.
SCLK	I	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	I	SERIAL DATA INPUT.
RX	–	REFERENCE CURRENT SET. With an external resistor (Rx = 5 kΩ ±1%) to ground, this pin gives a voltage proportional to the absolute temperature, setting the range for VFP.
VCA	I	ANALOG +5 VOLT SUPPLY.
VCD	I	DIGITAL +5 VOLT SUPPLY.
AGND	I	ANALOG GROUND.
DGND	I	DIGITAL GROUND.
VBP	O	BOOST PROGRAMMING VOLTAGE. Output of V-DAC which programs the boost.
VFP	O	CUTOFF FREQUENCY PROGRAMMING VOLTAGE. Output of I-DAC which programs the cutoff frequency.*

*A minimum load resistance of 150 kΩ should be used to avoid affecting the total minimum on-chip resistance of 1.35 kΩ.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150 °C
Junction Operating Temperature, Tj	+130 °C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCC V
Maximum Power Dissipation, *f*c = 8 MHz, Vcc = 5.5V	0.5W
T1 Lead Temperature (1/16" from case for 10 seconds)	260 °C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.5V < VCC < 5.5V
Ambient Temperature	0 °C < Ta < 70 °C
Tj Junction Temperature	0 °C < Tj < 130 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Isupply	VCC = 5.5V, outputs unloaded		55	75	mA
Idle Mode Current			9	13	mA
Idle to Active Mode Recovery Time				50	µs
Serial port program to output response time				50	µs
DC Characteristics					
VIH High Level Input Voltage	TTL input	2.0			V
VIL Low Level Input Voltage				0.8	V
IIH High Level Input Current	VIH = 2.7V			20	µA
IIL Low Level Input Current	VIL = 0.4V	−1.5			mA

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter Characteristics					
fc Filter Cutoff Frequency	*fc* = VFP, 21 ≤ F_Code ≤ 127	1.5		8	MHz
FCA Filter *fc* Accuracy	*fc* = VFP, 8 MHz	-10		+10	%
Cutoff Resolution	1.5 to 8 MHz	100			kHz
AO VO_NORM Diff Gain	F = 0.67 *fc*	0.7		1.1	V/V
AD VO_DIFF Diff Gain	F = 0.67 *fc*	0.90 AO		1.2 AO	V/V
FB Frequency Boost at *fc*	FB(dB) = 20 log [0.01703 (S_Code) +1]	0		10	dB
FBA Frequency Boost Accuracy	0 to 10 dB, Ta < 22 °C	–1.5		+1.5	dB
FBA Frequency Boost Accuracy	0 to 10 dB, Ta > 22 °C	–1		+1	dB
TGD0 Group Delay Variation Without Boost	0.2 *fc* - *fc*	–2% gdm		+2% gdm	ns
fc = 1.5 - 8 MHz gdm = group delay magnitude	*fc* - 1.75 *fc*	–3% gdm		+3% gdm	ns
TGDB Group Delay Variation With Boost	0.2 *fc* - *fc*	–2% gdm		+2% gdm	ns
fc = 1.5 - 8 MHz	*fc* - 1.75 *fc*	–3% gdm		+3% gdm	ns
Boost Resolution	1.5 to 8 MHz	.25			dB
VIF Filter Input Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 0.1 µF capacitor across Rx	1.5			Vppd
VOF Filter Output Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 0.1 µF capacitor across Rx	1.5			Vppd
VIF Filter Input Dynamic Range	THD = 3.5% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx	1.5			Vppd
VOF Filter Output Dynamic Range	THD = 3.5% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx	1.5			Vppd
VIF Filter Input Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 0.1 µF capacitor across Rx	1.0			Vppd
VOF Filter Output Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 0.1 µF capacitor across Rx	1.0			Vppd
VIF Filter Input Dynamic Range	THD = 2.0% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx, Ta < 22 °C	1.0			Vppd
VOF Filter Output Dynamic Range	THD = 2.0% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx, Ta < 22 °C	1.0			Vppd
VIF Filter Input Dynamic Range	THD = 1.5% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx, Ta < 22 °C	1.0			Vppd
VOF Filter Output Dynamic Range	THD = 1.5% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx, Ta < 22 °C	1.0			Vppd

ELECTRICAL SPECIFICATIONS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter Characteristics (continued)					
RIN Filter Diff Input Resistance		3.0			kΩ
CIN Filter Input Capacitance				7	pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 0 dB Boost		1.8	3	mVRms
	50Ω input				
	*f*c = 8 MHz 10 dB Boost		2.35	4	mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 0 dB Boost		4.2	6	mVRms
	50Ω input				
	*f*c = 8 MHz 10 dB Boost		5.85	9	mVRms
IO- Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA			60	Ω
TC Period, SCLK		100			ns
T1 SDEN Setup to SCLK Falls		0			ns
T2A SDEN Hold wrt SCLK Falls		0			ns
T2B SDEN Falls prior to SCLK Rises		25			ns
T3 SDI Setup to SCLK Falls		25			ns
T4 SDI Hold to SCLK Falls		25			ns
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCA, VCD	40	70		dB
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @5 MHz	30	50		dB
Bias: Vin+, Vin-	VCC = 5V	2.5	2.9	3.3	V
VO_NORM+, VO_NORM–	VCC = 5V	2.8	3.2	3.6	V
VO_DIFF+, VO_DIFF-	VCC = 5V	2.8	3.2	3.6	V
Change in Normal Output Offset	FDAC switched from 21-127		20		mV
Change in Differentiated Output Offset	FDAC switched from 21-127		20		mV

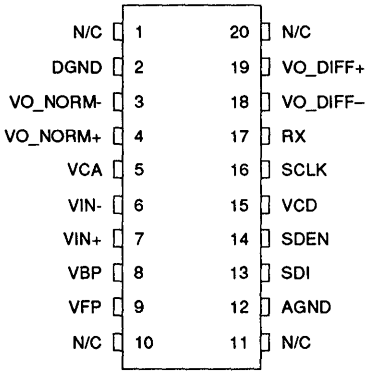
SSI 32F8120
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS

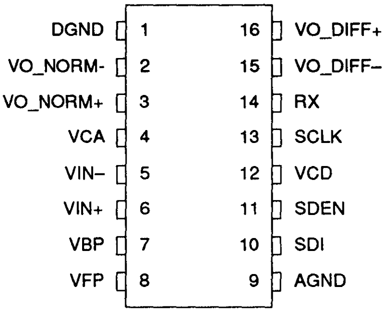
(Top View)

THERMAL CHARACTERISTICS: θja

16-lead SOL	100° C/W
20-lead SOV	125° C/W



20-Lead SOV



16-Lead SOL

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8120	16-Lead SOL	32F8120-CL	32F8120-CL
	20-Lead SOV	32F8120-CV	32F8120-CV

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Patent No. 5,063,309, Patent Pending 823,067

Notes:

silicon systems®
A TDK Group Company

SSI 32F8130/8131
Low-Power Programmable Electronic Filter

January 1993

DESCRIPTION

The SSI 32F8130/8131 Programmable Electronic Filters are digitally controlled low pass filters with a normal low pass output and a time differentiated low pass output. The low pass filter is of a 7-pole / 2-zero 0.05° phase equiripple type, with flat group delay response beyond the passband.

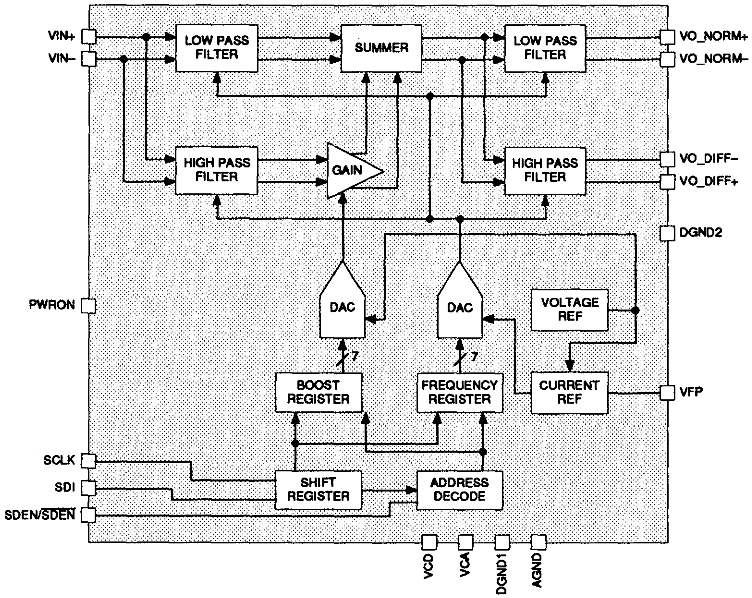
The SSI 32F8130/8131 bandwidth and boost are controlled by two on-chip 7-bit DACs, which are programmed via a 3-line serial interface. The SSI 32F8130 filter bandwidth is programmable from 250 kHz to 2.5 MHz. The SSI 32F8131 is programmable from 150 kHz to 1.4 MHz. The boost is programmable from 0 to 10 dB. Because the boost function is implemented as two zeros on the real axis with opposite sign, the flat group delay characteristic is not affected by the boost programming.

The SSI 32F8130/8131 are ideal for multi-rate, equalization applications. They require only a +5V supply and have a power down mode for minimal idle dissipation. The SSI 32F8130/8131 is available in a 16-lead SOL package.

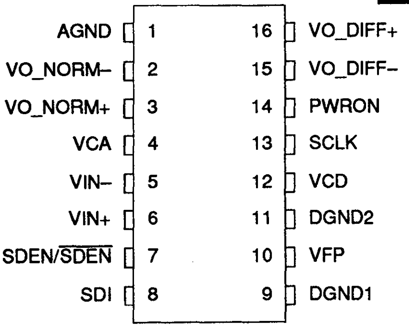
FEATURES

- **Programmable filter cutoff frequency (SSI 32F8130 FC=0.25 to 2.5 MHz, SSI 32F8131: FC = 0.15 to 1.4 MHz) with no external components, serial data connections to minimze pin count**
- **Power down mode (<5 mW)**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Programming via internal 7-bit DACs**
- **No external filter components required**
- **+5V only operation**
- **Supports constant density recording**

BLOCK DIAGRAM



PIN DIAGRAM



SSI 32F8130: Pin 7 = SDEN
SSI 32F8131: Pin 7 = $\overline{SDEN}$

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8130/8131
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8130/8131, a high performance programmable electronic filter, provides a 7-pole / 2-zero 0.05° equiripple linear phase low pass function with matched normal and time differentiated outputs. The device includes multiple biquads and first-order sections to accomplish the filter function, two 7-bit DACs for bandwidth and boost controls, a 3-line serial interface, and complete bias reference circuits. Only one external precision 8.25 kΩ resistor should be connected from the VFP pin to ground for operation. See Figure 1.

SERIAL INTERFACE

The SSI 32F8130/8131 allows easy digital controls of filter bandwidth and magnitude equalization via a 3-line serial interface. The three pins are SDI, SDEN and SCLK. SDI is the serial data input to an internal 8-bit shift register. SDEN is the shift register enable. SCLK is the shift register clock. Besides the 8-bit shift register which accepts data from the SDI input, there are four 4-bit registers which hold the filter bandwidth and boost controls. Two 4-bit registers are assigned to each control function, because a 7-bit binary control is required for each function.

The S-MSB register, whose address code is X000, holds the 3 MSBs of the boost control. The S-LSB register, whose address code is X001, holds the 4 LSBs of the boost control. The F-MSB register, whose address code is X010, holds the 4 MSBs of the cutoff frequency control. The F-LSB register, whose address code is X011, holds the 4 LSBs of the cutoff frequency control.

The serial interface consists of data packets, which are structured as 4-bit address decode followed by 4-bit data. Figure 2 shows the serial interface timing to successfully program the SSI 32F8130/8131.

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, is defined as the -3dB bandwidth with no magnitude equalization applied, and is programmable from 250 kHz to 2.5 MHz for SSI 32F8130, and 150 kHz to 1.4 MHz for SSI 32F8131. While the fc is controlled by an on-chip 7-bit DAC, the cutoff frequency resolution is better than 20-kHz step.

Let F_Code be the decimal equivalent of the 7-bit control. The cutoff frequency can be determined by the following equations:

SSI 32F8130 fc (kHz) = 18.2 x F_Code +70

SSI 32F8131 fc (kHz) = 10.81 x F_Code +37

where 12 < F_Code < 127.

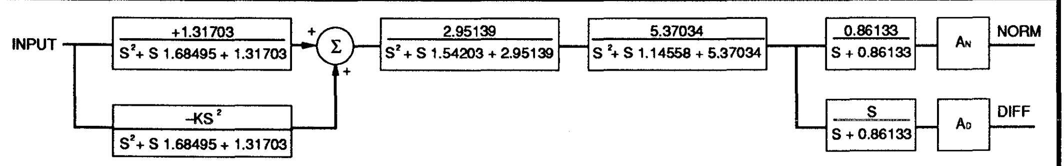
MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 10 dB boost is applied, the magnitude response peaks up 7 dB above the DC gain. This equalization function is also controlled by an on-chip 7-bit DAC.

Let S_Code be the decimal equivalent of the 7-bit control. The magnitude equalization can be determined by the equation:

Boost (dB) = $20 \times \log_{10} [0.01703 \times \text{S\_Code} + 1]$

where 0 < S_Code < 127.



Normalized for $\omega c = (2\pi)\, fc = 1$

AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc

Denormalize the frequency by substituting S → (S/2π fc)

Eq for $fc = 2.5$ MHz, $S = S / [(2\pi)(2.5 \cdot 10^6)] = S / (1.57080 \cdot 10^7)$

FIGURE 1: Normalized Transfer Function of the SSI 32F8130/8131

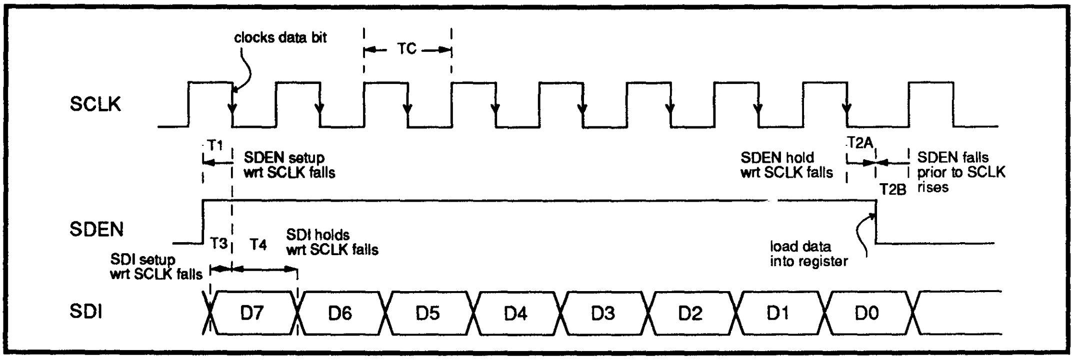


FIGURE 2: Serial Port Timing Relationship

Note:
The serial data enable function of the SSI 32F8130 and that of the SSI 32F8131 are of opposite polarity.

TABLE 1: Data Packet Fields

	ADDRESS BITS				USAGE	DATA BITS			
	D7	D6	D5	D4		D3	D2	D1	D0
R0	X	0	0	0	S - MSB REGISTER	X	S6	S5	S4
R1	X	0	0	1	S - LSB REGISTER	S3	S2	S1	S0
R2	X	0	1	0	F - MSB REGISTER	X	F6	F5	F4
R3	X	0	1	1	F - LSB REGISTER	F3	F2	F1	F0

X = Don't care bit.

SSI 32F8130/8131
Low-Power Programmable Electronic Filter

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN–	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the load.
VO_DIFF+ VO_DIFF–	DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to the load.
PWR_ON	POWER ON. A TTL high logic level enables the chip. A low level or open circuit puts the chip into a low power state.
SDEN (8130) $\overline{\text{SDEN}}$ (8131)	SERIAL DATA ENABLE. An active level allows SCLK to clock data into the shift register via the SDI input. An inactive level latches the register data and issues the information to the appropriate circuitry. Active level for SSI 32F8130 is HIGH, for SSI 32F8131 is LOW.
SCLK	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	SERIAL DATA INPUT.
VCA	ANALOG +5 VOLT SUPPLY.
VCD	DIGITAL +5 VOLT SUPPLY.
AGND	ANALOG GROUND.
DGND1 DGND2	DIGITAL GROUND.
VFP	CUTOFF FREQUENCY PROGRAMMING REFERENCE. A resistor of 8.25 kΩ should be connected between this pin and AGND.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC	-0.5 to 7	V
Voltage Applied to Inputs*	-0.5 to VCC	V
T1 Lead Temperature (1/16" from case for 10 seconds)	260	°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC	4.50 < VCC < 5.50	V
Ambient Temperature	0 < Ta < 70	°C
Tj Junction Temperature	0 < Tj < 130	°C

ELECTRICAL SPECIFICATIONS (continued)

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle Mode Current				1	mA
Isupply			60	70	mA
Power Dissipation	PWR_ON ≤ 0.8V			6	mW
	PWR_ON ≥ 2.0V		303	385	mW
Idle to Active Mode Recovery Time				50	µs
Serial port program to output response time				50	µs
DC Characteristics					
VIH High Level Input Voltage	TTL input	2.0			V
VIL Low Level Input Voltage				0.8	V
IIH High Level Input Current	VIH = 2.7V			20	µA
IIL Low Level Input Current	VIL = 0.4V			–1.5	mA
Filter Characteristics					
fc Filter Cutoff Frequency	12 < F_Code < 127 SSI 32F8130	0.25		2.5	MHz
	SSI 32F8131	0.15		1.4	MHz
FCA Filter *fc* Accuracy	over *fc* range	-10		+10	%
Cutoff Resolution	$\text{Resolution} = \frac{\text{Max fc}}{127}$ F8130		20		kHz
	F8131		12		kHz
AO VO_NORM Diff Gain	F = 0.67 *fc*	0.8		1.2	V/V
AD VO_DIFF Diff Gain	F = 0.67 *fc*	1.0 AO		1.2 AO	V/V
FB Frequency Boost at *fc*	FB(dB) = 20 log [.01703 (S_Code) + 1] 0 ≤ S_Code ≤ 127	0		10	dB
FBA Frequency Boost Accuracy	10 dB nominal	-1.5		+1.5	dB
TGD0 Group Delay Variation Without Boost	0.2 *fc* - *fc*	-2% gdm		+2% gdm	ns
fc = 0.25 - 2.5 MHz gdm = group delay magnitude	*fc* - 1.75 *fc*	-3% gdm		+3% gdm	ns
TGDB Group Delay Variation With Boost	0.2 *fc* - *fc*	-2% gdm		+2% gdm	ns
	fc - 1.75 *fc*	-3% gdm		+3% gdm	ns
Boost Resolution		.25			dB
VOF_N Filter Output Dynamic Range	THD = 1% max, Normal Output	1			Vpp

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter Characteristics (continued)					
VOF_D Filter Output Dynamic Range	THD = 1% max, Differentiated Output	1			Vpp
RIN Filter Diff Input Resistance		3.0	4.0	5.0	kΩ
CIN Filter Input Capacitance			3.0		pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 50Ω input *fc* = Max *fc* 0 dB Boost		1.2	1.9	mVRms
	10 dB Boost		1.4	2.0	mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 50Ω input *fc* = Max *fc* 0 dB Boost		2.1	2.7	mVRms
	10 dB Boost		2.5	3.4	mVRms
IO– Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA		50	70	Ω
T1 SDEN Set-up WRT SCLK Falls		0			ns
T2A SDEN Hold WRT SCLK Falls		0			ns
T2B SDEN Falls (rises for 8131) prior to SCLK rises		25			ns
T3 SDI Set-up WRT SCLK Falls		25			ns
T4 SDI Hold WRT SCLK Falls		25			ns
SCLK Period, TC		100			ns
Power Supply Rejection Ratio VO_NORM	100 mVpp from 10 kHz to 10 MHz on VCA, VCD	30	40		dB
Power Supply Rejection Ratio VO_DIFF		20	30		dB
Common Mode Rejection Ratio VO_NORM	Vin = 0VDC + 10 mVpp from 10 kHz to 10 MHz	30	40		dB
Common Mode Rejection Ratio VO_DIFF		20	30		dB
Bias: VO_NORM±	VCC = 5V	2.40	2.75	3.10	V
Vin±		2.20	2.35	2.80	V
VO_DIFF±		2.40	2.75	3.10	V
Normal Output Offset Variation	F_Code switched from 12-127	-200		200	mV
Differentiated Output Offset Variation	F_Code switched from 12-127	-200		200	mV

TABLE 1: Calculations

Typical change in *f*-3 dB point with boost

Boost (dB)	Gain@*f*c (dB)	Gain@ peak (dB)	*f*peak/*f*c	*f*-3dB/*f*c	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes:
1. *f*c is the original programmed cutoff frequency with no boost
2. *f*-3 dB is the new -3 dB value with boost implemented
3. *f*peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., *f*c = 1 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 2.20 MHz

*f*peak = 1.23 MHz

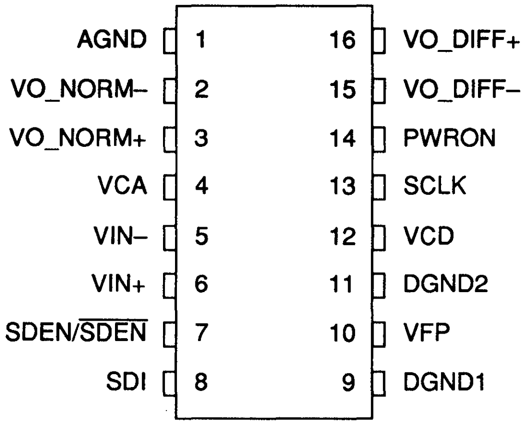
SSI 32F8130/8131
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS

(Top View)

THERMAL CHARACTERISTICS: θja

16-Lead SOL	100° C/W



16-Lead SOL

SSI 32F8130: Pin 7 = SDEN
SSI 32F8131: Pin 7 = $\overline{SDEN}$

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8130 16-Lead SOL	32F8130-CL	32F8130-CL
SSI 32F8131 16-Lead SOL	32F8131-CL	32F8131-CL

Patent No. 5,063,309
Patent Pending Nos. (516717) (823067)

Section 8

CUSTOM SOLUTIONS

8

silicon systems®
A TDK Group Company

CUSTOM SOLUTIONS

SILICON SYSTEMS LEADS THE WAY DEVELOPING MIXED-SIGNAL CUSTOM PRODUCTS.

This is a story about leadership. Silicon Systems is dedicated to taking the point in the creation of high-performance, application-specific custom, mixed-signal integrated circuits (MSICs®).

Such dedication means we bring a lot to the party. Including truly innovative analog, digital, and mixed analog/digital ICs. A full complement of mixed-signal CMOS, BiCMOS and Bipolar wafer fabrication processes, state-of-the-art automated design tools, production, assembly, test, and QA capability.

No one's more experienced

Our nearly 20 years of successful IC design work makes us the most experienced engineering team in the MSICs field. Add it all up and you get a company that saves you time and money while delivering you the most sophisticated mixed-signal custom ICs you can get.

Faster to market for mixed-signal applications

Whatever your mixed-signal design application, Silicon Systems gives you a competitive advantage. In communications, disk drives, other storage products, automotive control systems, or other analog/digital signal processing applications, you can depend on our technical know-how to do the job right and turn your design around faster.

CMOS. Bipolar. Analog. Digital. We've done it

Our designers are an experienced bunch. They're uniquely able to take a look at your specific application problem and move quickly to the right IC solution.

Our team is particularly adept at identifying key issues such as power, cost and performance trade-offs. So we can gear our efforts toward delivering you an optimized solution, manufactured with the appropriate fab process.

Technique	Application	Silicon Systems Designed Examples
CMOS Signal Processing	For analog continuous time and sampled data (switched-capacitor implementation) and digital signal processing (DSP) applications. Low-power capability also allows inclusion of ROMs, RAMs, and other analog/digital subsystems.	• 73K224 complete single-chip 2400 bit/s modem • C301 single-chip telephone headset amplifier • 14.4 kbit modem • Direct-broadcast satellite descrambler • Motor controllers • High-resolution analog data acquisition
Bipolar Signal Processing	For high-performance, low noise, wideband signal acquisition and processing applications. Offers TTL and/or ECL logic interfaces with high current drive.	• Sub 1 $\text{nV}/\sqrt{\text{Hz}}$ HDD R/W amplifiers • AGC, pulse detection amplifiers • High-speed data separators • Wideband transceivers • PLLs (phase locked loops) • Optical signal processing
Digital CMOS	For ASIC controllers, sequencers and data path applications with on-board ROM, RAM, and PLA sub-systems. Offers standard TTL and/or CMOS logic interfaces.	• Hard disk drive controllers • SCSI interface controllers • UARTs • Protocol controllers • Digital signal processors
Digital Bipolar	High-speed logic and interface circuitry. Offers standard logic or custom interfaces.	• Encoders and decoders • High-speed digital transceivers

The right mix of analog and digital

Providing total analog/digital systems on a chip allows you to meet your cost and performance objectives whether you're designing the next generation of communications devices, or perhaps an I/O multiplexer to control electronics in 21st century automobiles.

We've turned to CMOS to effectively implement low-power, highly integrated systems solutions for everything from modems and CATV satellite descramblers to hard disk drive controllers and digital signal processors.

We've gone the Bipolar route to meet the high-performance needs of products like wideband transceivers, R/W amplifiers, low-noise amplifiers, pulse detectors, high-speed data separators and high-performance, low-power combo devices.

Our BiCMOS technology promises to open up new horizons of product capability for applications demanding optimum performance at the lowest power.

SOPHISTICATED TOOLS FOR A CUSTOM DESIGN

At each of five design centers capable of worldwide service — Tustin, Santa Clara and Nevada City, California; Tokyo and Singapore — Silicon Systems employs PEGASYS™, an internal design automation system developed from carefully selected vendor tools and our own proprietary software. Using Mentor Graphics workstations for both electrical and physical design, PEGASYS helps create complex designs while significantly reducing schedules, costs and errors.

By integrating such helpful third-party tools and custom software, we're better able to design and analyze mixed-signal integrated circuits in all CMOS, Bipolar and BiCMOS technologies. It's an approach that has given us the edge in mixed-signal design and helped put Silicon Systems' customers in a favorable position in the marketplace.

Specifically, PEGASYS brings the following to each design:

- Fully integrated design environment
- Methodology for precision circuit design
- Integrated physical design
- Automatic place and route
- Complete layout verification

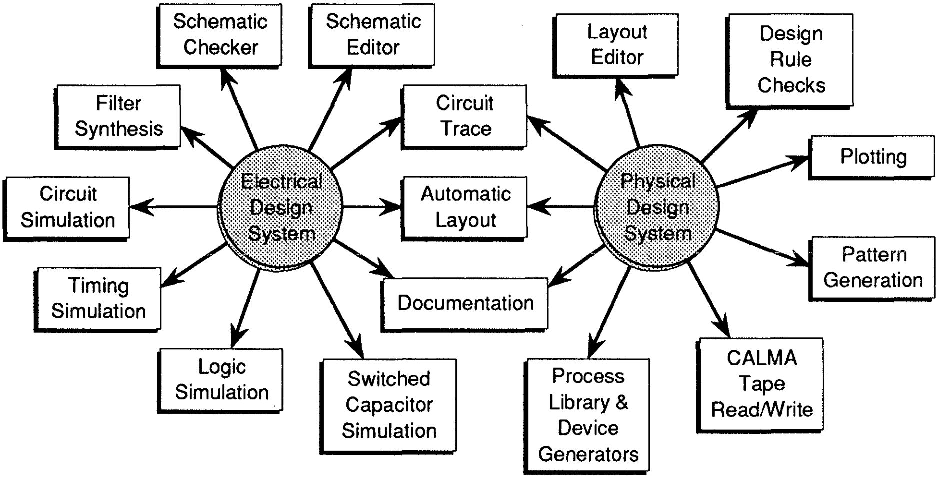
Our design automation staff integrates the third-party tools and optimizes their use on the Mentor platform. This framework can easily accommodate new tools when needed, and it enables us to support a combination of analog and digital design techniques in all CMOS, Bipolar and BiCMOS chip designs. By mixing design methodologies, we can achieve optimum systems performance, even when schedules are tight.

Electrical design

A single CAE (computer aided engineering) environment provides for schematic capture, simulation, synthesis and documentation. We support this software with extensive libraries of pre-designed cells and components. Highly specialized cells or components can be designed and enhanced where required. We simulate each circuit to meet precise performance specifications using:

- Analog circuit simulation
- Digital logic simulation
- Timing simulation
- Mixed-mode simulation
- Switched-capacitor filter simulation
- Behavioral simulation

Admittedly, simulation alone is not the key to perfecting performance. That's why we work aggressively to refine our understanding of models to make them work with simulation. Inside our progressive device modeling and characterization



(DMC) laboratory, we develop accurate circuit simulation models and parameters. The DMC lab provides complete device model data for our processes using capabilities such as AC measurement, statistical analysis and worst-case modeling. Accurate models are a cornerstone of our design-for-quality approach.

Physical design

Our PEGASYS layout system aids the mask designer through all physical design phases, ensuring consistency throughout the design cycle. This fully integrated environment provides for both full-custom design and automatic place-and-route design including these capabilities:

- Graphic editing
- On-line point-to-point routing
- Compaction
- On-line design rule checking
- Layout-to-schematic verification
- Parasitic extraction/back annotation
- Output in industry standard GDS format

The same physical design environment supports all processes and design methodologies.

Automatic place & route software

The automatic place-and-route capability speeds through physical design far more rapidly than a full-custom, hand-drawn approach. We have combined Cadence Design Systems' TANCELL™, the most area-efficient router on the market, with our proprietary tools. This flexible environment allows for floor planning and automatic routing, and it supports the combination of custom cells, standard cells and compiled blocks.

Layout-to-schematic trace and verification software

Our circuit-trace capability compares the completed IC layout to the schematic data base, using proprietary techniques and tools to guarantee quality. We help to eliminate layout errors through verification checks of both connectivity and component values. The resulting layout is an exact match of the schematic design. Further possible layout problems are identified during post-layout simulations using true parasitic modeling of capacitance and resistance interconnect. In short, all potential problems are fixed or addressed before first silicon fabrication.

KADS. A mutual drive for custom design

The Silicon Systems Key Account Design Service (KADS) program is our way of designing and developing custom IC solutions in a high-level cooperative partnership with our customers.

The KADS approach introduces the best minds in your company to Silicon Systems' mixed-signal specialists. Together we work closely, freely exchanging each other's ideas and experience in order to inspire breakthrough technical achievements and raise quality and creativity to a new level.

WHERE PROCESS MEETS NEED: CMOS

Silicon Systems offers two proven CMOS process technologies for creating low-power, highly integrated systems solutions. We use CH for 5V and12V applications and CG for 5V only needs. Both offer excellent analog performance. For a summary, see Table 1.

Our CH process achieves its higher (to 12V) operation via a DDD (double diffused drain) source/drain structure. This increases the S/D junction grading and breakdown voltage while lowering the associated junction capacitance.

The CH process also provides high quality, low voltage coefficient, precision poly-poly capacitors that support high performance switched-capacitor filtering and data conversion (A/D and D/A) circuits. Another important CH process feature for analog applications is found with our high Ω/' poly resistors. Their low voltage coefficient is important for low distortion, continuous time filters such as in anti-aliasing applications. Typical CMOS processes use unacceptable high-value well resistors, and do not provide poly-poly capacitors.

Improved CMOS reliability

Silicon Systems boosts your system's reliability by incorporating a well ring into the CH process. This improves well tie-down and increases latchup immunity. For harsher environments such as motor drivers or the automobile, we use an epitaxial (epi) substrate to provide latchup immunity of more than 200 mA.

CMOS CG. Low-power & high performance

Our CG CMOS process is specifically designed to support your 5V mixed-signal applications. Its smaller feature size (1.5µ, shrinkable to 1.2µ) allows for much higher levels of system integration, higher speed and lower power.

CG supports high performance analog circuitry with precision poly-poly capacitors as well as complex digital circuitry including DSPs, microcontrollers, data paths and memory.

For a cross-section view of the Silicon Systems CG CMOS process, see Figure 1.

BIPOLAR & BICMOS PROCESS TECHNOLOGIES

Our bipolar MSICs take advantage of two high-performance Bipolar processes: BK (for 12V applications) and BN (for 5V applications). The BK analog/digital process achieves its higher voltage operation and improves lateral PNP transistor performance by using a lightly-doped epi layer.

In BK we provide deep N+ and P+ enhancement layers to reduce both collector series and base resistance. Our use of up-junction isolation gives us a major reduction in device area, when compared with that of typical junction isolated processes. Metal-poly capacitors with a nitride dielectric are used for improving capacitor reliability.

BN. Low-power/ 8 Ghz Bipolar at 5 volts

A noteworthy feature of a minimum size BN process transistor is that it's only about 1/5th the size of a minimum size BK transistor. Because we employ full oxide isolation in BN, we can fabricate very fast, very small transistors and reduce sidewall capacitances. This supports not only high speed, but low power.

The BN process features high-performance NPN transistors to support mixing high-performance emitter coupled logic (ECL) with analog circuitry. To provide for strict TTL I/O compatibility, we use superior PtSi Schottky diodes.

The resulting speed and packing density allows you to effectively implement dense high-performance, low-power Bipolar analog/digital capability into your system designs.

For a feature-by-feature comparison of Silicon Systems' BK and BN Bipolar processes, see Table 3.

BiCMOS process technologies

High performance NPNs and CMOS transistors highlight our BiCMOS process. They support mixing high performance analog circuitry with high density digital logic.

We greatly improve response speed through the use of silicided base components and S/D regions that decrease extrinsic resistances in both types of active components while reducing the emitter-base and gate-source (drain) space.

BiCMOS is virtually immune to CMOS latch-up due to retro-grade wells. The high drive capability of Bipolar and the low-power/high-density capability of CMOS combine to enhance design potential considerably. Full-featured, 3-volt designs are one such example.

Process	Type	Application Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches Poly 1	Metal 1	Metal 2	Features
CH	Si-Gate, single metal, dual poly, PWell	12V	18V	3.6µ	5.8µ	6.4µ	n/a	• DDD S/D structure • Poly-poly capacitors • Low-voltage coefficient • High Ω /□poly resistors • Epi substrate option • Buried well-ring
CG	Si-Gate, dual metal, dual poly, PWell	5V	7V	1.5µ	3.0µ	4.5µ	6.0µ	• DDD S/D structure • Poly-poly capacitors • Shrinkable to 1.2µ

TABLE 1: CMOS Process Chart

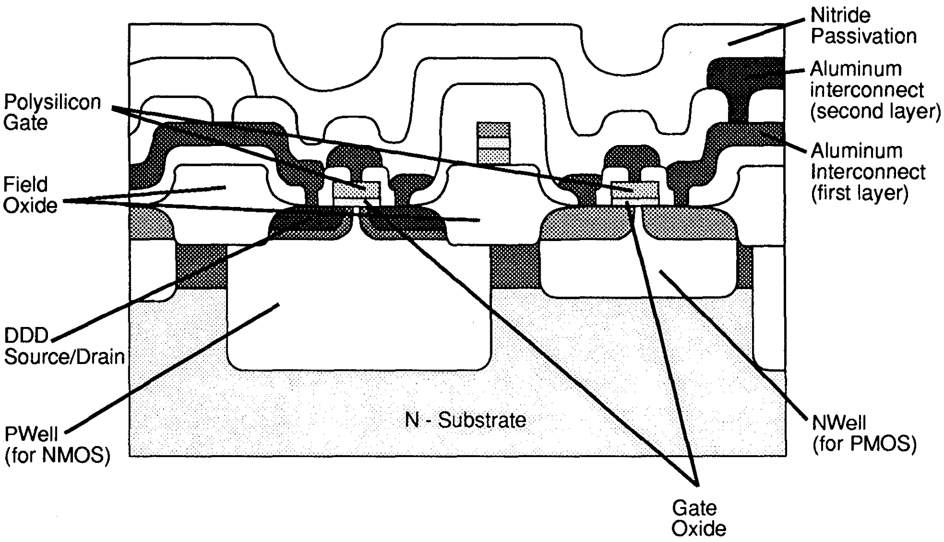


FIGURE 1: CG CMOS Process Transistor

Type	Appl. Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches				BV_{CEO}	NPN Ft	Emitter	Features
				Poly	M0	M1	M2				
Bipolar: Oxide isolated **CMOS:** Si-Gate, single poly, triple metal, PWell	5V	10V	1.0μ	2.6μ	3.2μ	3.8μ	5.0μ	8V	13 GHz	1.0μ	**Bipolar:** •High Perf. NPNs •PtSi Schottky Diodes •Gate Oxide Capacitors •Poly Capacitors •Sidewall Oxide Isolation •Fuses **CMOS:** •Lightly Doped Drains

TABLE 2: BiCMOS Process Chart

Process	Type	BV_{CEO}	NPN Ft	Emitter Size	M1 Pitch	M2 Pitch	Features
BK	Junction-isolated	12V	2 GHz	2.5μ	9.0μ	14.0μ	• Polysilicon emitters • Al Schottky diodes • Nitride capacitors • Ion implanted resistors • Up/down junction isolation • Collector/base plugs
BN	Oxide-isolated	6V	8 GHz	2.0μ	4.5μ	8.0μ	• High performance NPNs • PtSi Schotty diodes • Nitride capacitors • Ion implanted resistors • Sidewall oxide isolation • Collector/base plugs

TABLE 3: Bipolar Process Chart

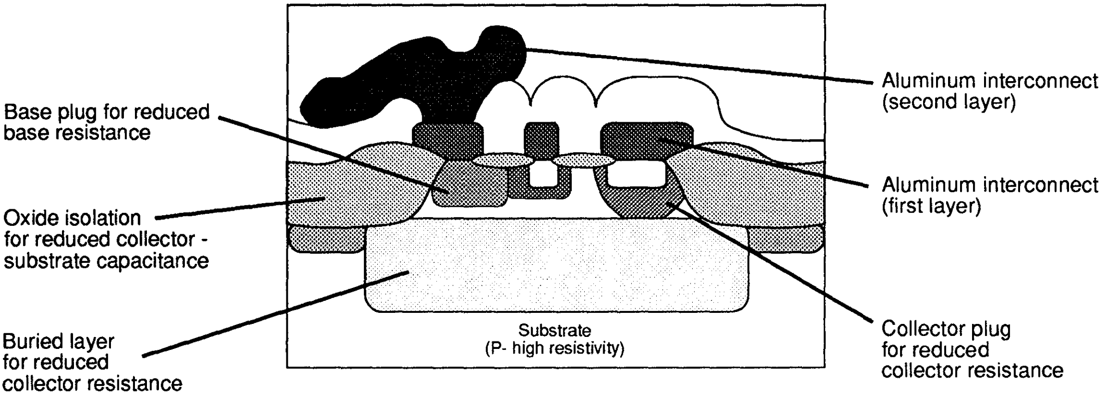


FIGURE 2: BN Bipolar Process NPN Transistor

A SUPERIOR FINISH FOR CMOS, BIPOLAR AND BICMOS

You might say this is the payoff window. The benefits of our process technologies, design tools and our unique custom approach all come together during wafer fabrication, test and assembly.

Our two manufacturing centers, located in Tustin and Santa Cruz, California, can offer specialized capabilities to match your particular fabrication requirements. Both facilities provide you with high resolution stepper photolithography technology, positive resist, dry plasma etch systems, high current ion implantation and automatic sputtering.

Fabrication sites in both Tustin and Santa Cruz accommodate 4- and 6-inch wafer fabrication and Bipolar, CMOS and BiCMOS processes.

The right package

Silicon Systems offers a wide range of packages to meet the small footprint requirements of advanced storage and communication products. We continue to be innovative in surface mount technology by providing PLCC, SO, VSOP, SSOP, QFP, TQFP and VTQFP packages. At our Singapore assembly & test facility we have the full capability to support high quality automated packaging while also maintaining rapid cycle times.

Promis. Quality through CAM

Process and Management Information System (PROMIS) underscores our commitment to computer-aided manufacturing (CAM). And to delivering you a superior quality product on time.

We use PROMIS to facilitate the data required in our manufacturing, monitoring and statistical process control (SPC) systems.

With PROMIS we more effectively manage our inventory, accurately track wafers in process, and closely monitor the clean room environment.

PROMIS also assists our SPC efforts, as does our commitment to fully train all of our manufacturing personnel in SPC basics.

We design for quality

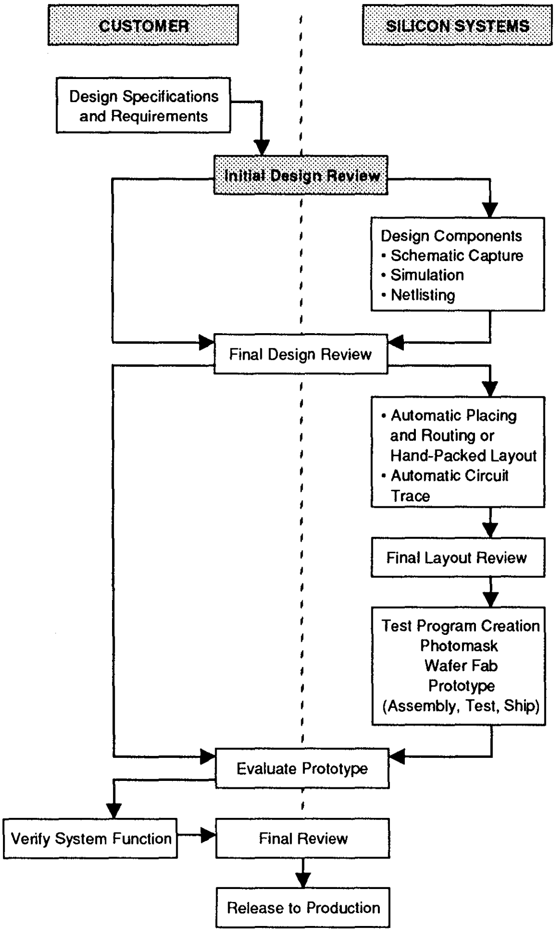
It's our view that quality is nothing less than absolute customer satisfaction. To achieve it, we begin far "upstream" in the product development process. Our design-for-quality approach scrutinizes the design itself with statistically based models, comprehensive simulation tools and vigorous design reviews.

The results of such an effort are IC products that boast lower defect rates, higher parametric performance and far fewer redesigns. Moreover, our persistence in improving quality keeps us focused on finding better and faster ways to satisfy future customer demands.

Quality that delivers

With effective systems such as PROMIS and our design-for-quality approach in place, Silicon Systems is prepared to deliver you finished products you can really depend on. On time. And within budget.

For details on how you can take best advantage of Silicon Systems' custom mixed-signal IC solutions, see your nearest Silicon Systems representative, or contact us. Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680. 714-573-6000. FAX: (714) 573-6914.



CUSTOMER INTERFACE FOR FULL-CUSTOM AND CELL-BASED DESIGNS

Section 9

RELIABILITY & QUALITY ASSURANCE

CONTINUOUS IMPROVEMENT MISSION & OBJECTIVE STATEMENT

Mission

Be the supplier of choice by exceeding customer expectations through continuous improvements in our products, systems and services.

Objectives

Provide world class quality in our products and services through focus on:

Customer Partnering
Cycle Time Improvement
Process and System Improvements

Develop a culture that ensures the consistent use of continuous improvement tools and fact based decision methodology by:

Senior Management Leadership
Employee Empowerment
Aggressive Goal Setting and Performance Measurement
Communication and Celebration of Successes

Alan V. King
President, CEO

Cheryl A. Stock
Vice President, Corporate R&QA

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Reliability and Quality Assurance

SECTION 1

1.1 INTRODUCTION

Silicon Systems is committed to the goal of customer satisfaction through the on-time delivery of defect free products that meet the customer's expectations and requirements. This section outlines Silicon Systems' ongoing activities for the control and continual improvement of quality in every aspect of our organization.

Silicon Systems is diligently working to maintain and improve its position as a world-class provider of mixed-signal integrated circuits (MSICs®).

We realize and practice the concept that quality and reliability must be designed and built into our products. In addition, Silicon Systems utilizes rigid inspections and data analysis to evaluate the acceptability and variation existing in incoming materials and performs stringent outgoing quality verification. The manufacturing process flow is encompassed by an effective system of test/inspection checks and in-line monitors which focus on the control and reduction of process variation. These gates and monitors ensure precise adherence to prescribed standards and procedures.

Silicon Systems also incorporates the use of statistical process control techniques into company operations. The control and reduction of the process variation by the use of statistical problem solving techniques, analytical controls and other quantitative methods ensures that Silicon Systems' products maintain the highest levels of quality and reliability.

Our Reliability and Quality Assurance organizations are committed to working closely with our customers to provide assistance and a continually improving level of product quality.

1.2 SILICON SYSTEMS' QUALITY MANDATE: CONTINUOUS IMPROVEMENT

Continuous improvement is Silicon System's strategic thrust for the 1990's. In order to ensure that all aspects of our business are encompassed by this mandate, Corporate Reliability & Quality Assurance has been chartered with the responsibility for developing, educating and overseeing the worldwide continuous improvement process. The continuous improvement initiative will lead to developing a new organizational culture, changing attitudes and stronger ownership and accountability for total customer satisfaction.

1.3 CHARACTERISTICS OF SILICON SYSTEMS' CONTINUOUS IMPROVEMENT PROCESS

- Executive Steering Committee leadership and direction - defines the right things to do and provides guidance - the right way to do them.
- Continuous improvement is measured everywhere and by everyone. Metrics that reflect pride in accomplishment are celebrated.
- Benchmarking is employed as a method to shorten learning curves and ensure successful ventures.
- Quality management and employee empowerment are encouraged at all levels.

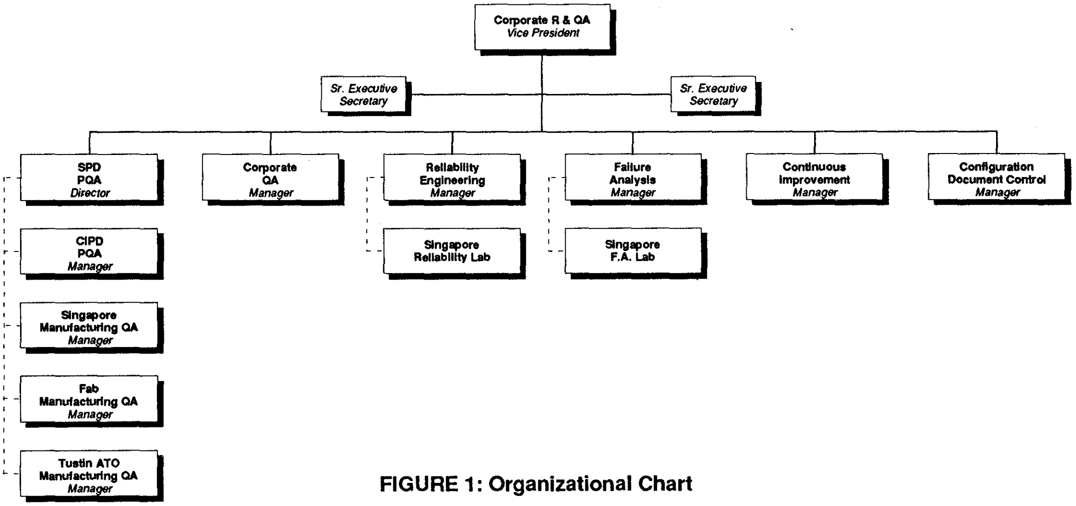


FIGURE 1: Organizational Chart

- Supplier partnership is a critical element of our quality strategy.

This is the essence of Silicon Systems - a total quality involved company - forward looking and immersed in the goal of customer satisfaction and best-in-class business pursuits.

1.4 CORPORATE RELIABILITY AND QUALITY ASSURANCE

It is the objective of the Corporate Reliability and Quality Assurance organization to ensure that proactive quality systems are in place to ensure that Silicon Systems' products will meet or exceed customer requirements and expectations. In addition, the Reliability and Quality Assurance organization works to facilitate the timely implementation of solutions and monitors the effectiveness of corrective actions. These organizational strategies support the continuing enhancement of quality consciousness throughout Silicon Systems.

SECTION 2: QUALITY ASSURANCE

2.1 QUALITY OBJECTIVES

While all Silicon Systems employees have direct responsibility for quality in their functions, the Quality Assurance Organizations have the ultimate responsibility for the reliable performance of our products. This is accomplished through the development, administration and assessment of formal quality systems which assure Silicon Systems' management, as well as our customers, that products will fulfill the requirements of customer purchase orders and all other specifications related to design, raw material and in process through completion of the finished product.

Corporate Quality Assurance supports, coordinates and actively participates in the formal qualification of suppliers, material, processes, and products, and the administration of quality systems and production monitors to assure that our products meet Silicon Systems quality standards. Product Quality Assurance provides the liaison between Silicon Systems and the customer for all product quality related concerns.

It is the practice of Silicon Systems to have corporate quality and reliability objectives encompass all of its activities. This starts with a strong commitment of support from the corporate level and continues with exceptional customer support long after the product has been shipped.

Silicon Systems emphasizes the belief that quality and reliability must be built into all of its products by ensuring that all employees are educated in the quality philosophy of the company. Some of the features built into Silicon Systems quality culture include:

1. Structured training programs directed at wafer fabrication, test, process control personnel and supporting organizations.
   - Team based problem solving methodologies.
   - Corporate-wide training of quality philosophy and statistical methods.
2. Stringent in-process inspection, gates, and monitors.
3. Rigorous evaluation of designs, materials, and processing procedures.
4. Stringent electrical testing (100% and QC AQL/Sample testing).
5. Ongoing reliability monitors and process verifications.
6. Real-time use of statistical process control methodology.
7. Corporate level audits of manufacturing, subcontractors, and suppliers.
8. Timely corrective action system.
9. Control of non-conforming material.

These focused quality methods result in products which deliver superior performance and reliability in the field.

2.2.1 INCOMING INSPECTIONS

Incoming inspection plays a key role in Silicon Systems' quality efforts. Small variations in incoming material can traverse the entire production cycle before being detected much later in the process. By paying strict attention to the monitoring of materials at the earliest possible stage, variation can be reduced, resulting in a stable uniform process.

2.2.2 IN-PROCESS INSPECTIONS

Silicon Systems has established key inspection monitors in such strategic areas as wafer fabrication, wafer probe, assembly, and final test. These quality monitoring tests are performed in addition to the intermediate and final inspections found in the manufacturing process.

Quality control monitors have been integrated throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediary manufacturing steps. This data is used to document quality trends or long term improvements in the quality of specific operations. Abnormality control is being used to enhance the effectiveness of this process. In process monitors such as oxide integrity, electromigration immunity and other parameters monitor long term reliability as well as circuit performance.

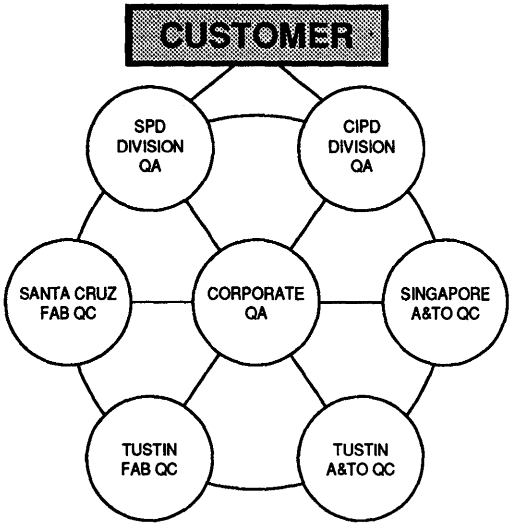


FIGURE 2
Quality Assurance Relationships
Quality Steering Committee

2.3 QUALITY STEERING COMMITTEE

The Corporate, Product and Manufacturing Quality Assurance organizations work closely together to provide leadership in the development, integration and assessment of Silicon Systems' worldwide quality systems and procedures.

This team approach ensures that policies and procedures are standardized and facilitates rapid improvement in products, processes and services.

2.4 DESIGN FOR QUALITY

Since the foundation of a reliable product is rooted in the design process, the Reliability and Quality Assurance organizations actively participate in comprehensive cross-functional reviews of design stages prior to the product's transition to production status. These review stages assure a predictable and effective development cycle. Other important design-related functions include ensuring that process specification revisions are translated into updated design parameters and the translation of manufacturing process capability into design guidelines. This is accomplished through the identification and monitoring of critical process and device parameters. Wafer level test at the early stages of process development also plays a critical role. These elements, included in Silicon Systems design for quality effort, support the development of robust design rules which are as insensitive as possible to inherent manufacturing variation. The result is a product that delivers predictable and reliable long term performance.

2.5 PPM REDUCTION PROGRAM

The primary purpose of a PPM reduction program is to provide a formalized feedback system in which data from nonconforming products can be used to improve future product consistency and reliability. The action portion of this program is accomplished in three stages:

1. Identification of defects by failure mode.
2. Identification of defect causes and initiation of corrective action.
3. Measurement of results and setting of improved goals.

The data summarized from the established PPM program is compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of defective parts per million (PPM). Founded on a statistically valid database of PPM data and an established five-year strategic plan identifying PPM improvement goals, Silicon Systems has consistently achieved excellent quality standards and will continue to progressively improve PPM standards.

2.6 COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) is used throughout Silicon Systems for the identification, control, collection and dissemination of timely information for logistics control. Silicon Systems also uses this type of computerized system for statistical process control and manufacturing monitoring. PROMIS, (PROcess Management and Information System), displays approved/controlled recipes, processes, and procedures; tracks work-in-process; reports accurate inventory information; allows continuous recording of facilities data; contains statistical analysis capabilities; and much more. PROMIS allows for a paperless facility, a major element in minimizing contamination of clean room areas.

TEST	CONDITIONS	PURPOSE OF EVALUATION
Biased temperature/humidity	85°C/85° %RH	Resistance to high humidity with bias
Highly accelerated stress test (HAST)	JDEC A110	Evaluates package integrity
High temperature operating life (HTOL)	Mil 883D, Method 1005	Resistance to electrical and thermal stress
Early Failure Rate	Mil 883D, Method 1005	Detect infant mortality
Steam pressure	121°C/15PSI	Resistance to high humidity
Temperature cycling	Mil 883D, Method 1010	Resistance to thermal excursion (air)
Thermal shock	Mil 883D, Method 1011	Resistance to thermal excursion (liquid)
Salt atmosphere	Mil 883D, Method 1009	Resistance to corrosive environment
Constant acceleration	Mil 883D, Method 2001	Resistance to constant acceleration
Mechanical shock	Mil 883D, Method 2002	Resistance to mechanical shocks
Solderability	Mil 883D, Method 2003	Evaluates solderability of leads
Lead integrity	Mil 883D, Method 2004	Evaluates lead integrity before board assembly
Vibration, variable frequency	Mil 883D, Method 2007	Resistance to vibration
Thermal resistance	Silicon Systems Method	Evaluates thermal dissipation
Electrostatic damage	Mil 883D, Method 3015	Evaluates ESD susceptability
Latch-up	Silicon Systems Method	Evaluates latch-up susceptibility
Seal fine and gross leak	Mil Std 883D, Method 1014	Evaluates hermeticity of sealed packages

TABLE 1: Reliability Stress Tests

SECTION 3: RELIABILITY

3.1 RELIABILITY PROGRAM

Silicon Systems has defined various programs that will characterize product reliability levels on a continuous basis. These programs can be categorically described by:

1. Qualifications
2. Production monitors
3. Evaluations
4. Failure analysis
5. Wafer level reliability
6. Data collection and presentation for improvement projects

3.2 QUALIFICATIONS

Extensive qualification testing and data collection ensures that all new product designs, processes, and packaging configurations meet the absolute maximum ratings of design and the worst case performance criteria for end users. A large database generated by means of accelerated stress testing results in a high degree of confidence in predicting final use performance. The qualification criteria used are periodically reviewed to be consistent with Silicon Systems' increasing quality and reliability goals in support of our customers.

3.3 PRODUCTION MONITORS

This program has been established to randomly select a statistically significant sample of production products for subjection to maximum stress test levels in order to evaluate the useful life of the product in a field use environment.

Table 1 lists reliability test methods that are in use at Silicon Systems. This analysis of production monitor at Silicon Systems provides valuable information on possible design/process changes which assure continued improved reliability. The monitors are periodically reviewed for effectiveness and improvements.

3.4 EVALUATIONS

The evaluation program at Silicon Systems is an ongoing effort that will continue defining standards which address the reliability assessment of the circuit design, process parameters, and package of a new product. This program continuously analyzes updated performance characteristics of product as they undergo improvement efforts at Silicon Systems.

3.5 FAILURE ANALYSIS

The failure analysis function is an integral part of the Quality and Reliability department at Silicon Systems. Silicon Systems has assembled a highly technical and sophisticated failure analysis laboratory and staff. This laboratory provides visual analysis, electrical reject mode analysis, and both destructive and non-destructive data to aid the engineers in developing corrective action for improvement. These test analyses may include metallurgical, optical, chemical, electrical, SEM with X-ray dispersive analysis, and E-Beam non-contact analysis as needed.

These conclusive in-house testing and analysis techniques, are complemented by outside support, such as scanning acoustic microscopy, focused ion beam, and complete surface and material analysis. This allows Silicon Systems to monitor all aspects of product manufacturing to ensure that the product of highest quality is shipped to our customers.

3.6 WAFER LEVEL RELIABILITY PROGRAM

A primary objective at Silicon Systems is to improve the reliability of our products through characterization of our manufacturing operations. The identification of specific failure mechanisms occuring in the wafer fabrication and assembly processes is a prerequisite to effective corrective action aimed at reducing defects and improving quality and reliability.

The primary advantage of wafer level reliability testing is the speed at which results can be derived, thereby providing additional response time and an early warning of process changes. This tool provides Silicon Systems with a very rapid analysis tool which allows for the early identification of possible problems and a determination of their origin.

The continuous improvement approach taken at Silicon Systems uses the wafer level reliability tests as tools to improve the process, identify potential problems, determine the sources of any process weakness and eliminate problems upstream in the process. This results in a focus on reliability improvement that goes well beyond merely determining the projected lifetime of a product to a detailed characterization, measurement and control of the specific parameters which actuallly determine product lifetime.

3.7 DATA COLLECTION AND PRESENTATION FOR IMPROVEMENT PROJECTS

Data collected from each element of the Reliability program is summarized for scope and impact and distributed among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review the performance of our product.

3.8 RELIABILITY METHODS

The Reliability Program utilizes a number of stress tests that are presently being used to define performance levels of our products. Many of these stress tests are per MIL-STD-883D as shown in Table 1.

3.9 RELIABILITY PREDICTION METHODOLOGY

At Silicon Systems, the Arrhenius model is used to relate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states $FR = A \exp(-Ea/KT)$

Where:

FR = Failure rate

A = Constant

Ea = Activation Energy (eV)

K = Boltzmann's constant 8.62×10^{-5} eV/ degree K

T = Absolute temperature (degree K)

SECTION 4: ELECTROSTATIC DISCHARGE PROGRAM

4.1 ESD PREVENTION

Silicon Systems recognizes that the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity is vital. ESD safe procedures are incorporated throughout all operations which come in contact with these devices. Continuous improvement in the ESD protection levels is being accomplished through the incorporation of increasingly robust protection devices during the circuit design process as well as work area improvements.

Silicon Systems' quality activity incorporates several protection measures for the control of ESD. Some of the preventive measures include handling of parts at static safe-guarded workstations, the wearing of wrist straps during all handling operations, the use of conductive lab coats in all test areas and all areas which handle parts and the packaging of components in conductive or anti-static containers.

NOTES

Section 10

PACKAGING/ORDERING INFORMATION

Silicon Systems

Packaging Index

SON is a 150 mil width package.

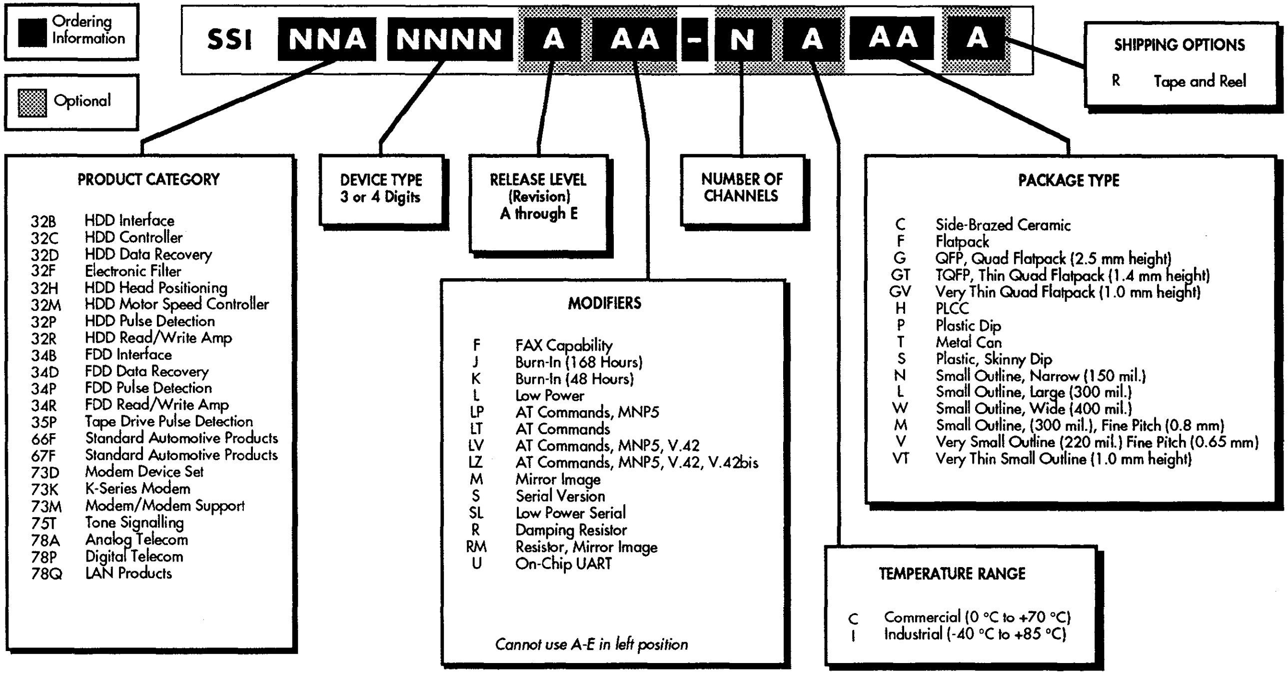
SOL is a 300 mil width package.

SOW is a 400 mil width package.

SOM is a 300 mil width package, fine pitch (0.8mm).

SOV is a 220 mil width package, fine pitch (0.65mm).

Silicon Systems
Ordering Information



PRODUCT CATEGORY (NNA)

32B	HDD Interface
32C	HDD Controller
32D	HDD Data Recovery
32F	Electronic Filter
32H	HDD Head Positioning
32M	HDD Motor Speed Controller
32P	HDD Pulse Detection
32R	HDD Read/Write Amp
34B	FDD Interface
34D	FDD Data Recovery
34P	FDD Pulse Detection
34R	FDD Read/Write Amp
35P	Tape Drive Pulse Detection
66F	Standard Automotive Products
67F	Standard Automotive Products
73D	Modem Device Set
73K	K-Series Modem
73M	Modem/Modem Support
75T	Tone Signalling
78A	Analog Telecom
78P	Digital Telecom
78Q	LAN Products

DEVICE TYPE (NNNN)
3 or 4 Digits

RELEASE LEVEL (A)
(Revision)
A through E

MODIFIERS (AA)

F	FAX Capability
J	Burn-In (168 Hours)
K	Burn-In (48 Hours)
L	Low Power
LP	AT Commands, MNP5
LT	AT Commands
LV	AT Commands, MNP5, V.42
LZ	AT Commands, MNP5, V.42, V.42bis
M	Mirror Image
S	Serial Version
SL	Low Power Serial
R	Damping Resistor
RM	Resistor, Mirror Image
U	On-Chip UART

Cannot use A-E in left position

NUMBER OF CHANNELS (N)

TEMPERATURE RANGE (A)

C	Commercial (0 °C to +70 °C)
I	Industrial (-40 °C to +85 °C)

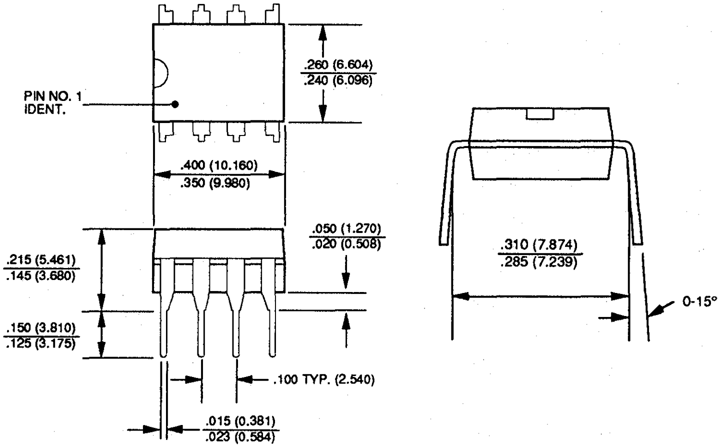
PACKAGE TYPE (AA)

C	Side-Brazed Ceramic
F	Flatpack
G	QFP, Quad Flatpack (2.5 mm height)
GT	TQFP, Thin Quad Flatpack (1.4 mm height)
GV	Very Thin Quad Flatpack (1.0 mm height)
H	PLCC
P	Plastic Dip
T	Metal Can
S	Plastic, Skinny Dip
N	Small Outline, Narrow (150 mil.)
L	Small Outline, Large (300 mil.)
W	Small Outline, Wide (400 mil.)
M	Small Outline, (300 mil.), Fine Pitch (0.8 mm)
V	Very Small Outline (220 mil.) Fine Pitch (0.65 mm)
VT	Very Thin Small Outline (1.0 mm height)

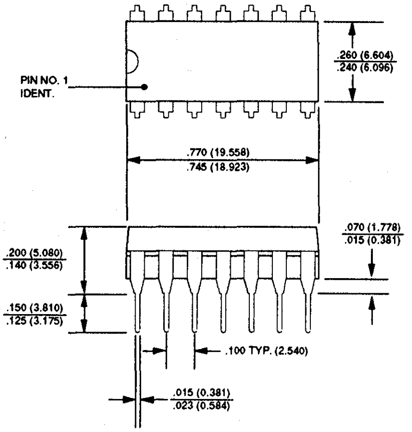
SHIPPING OPTIONS (A)

R	Tape and Reel

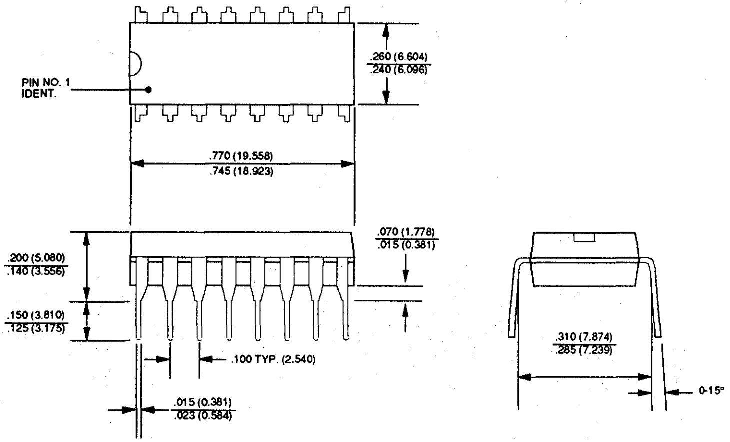
Package Information
(Plastic DIP)



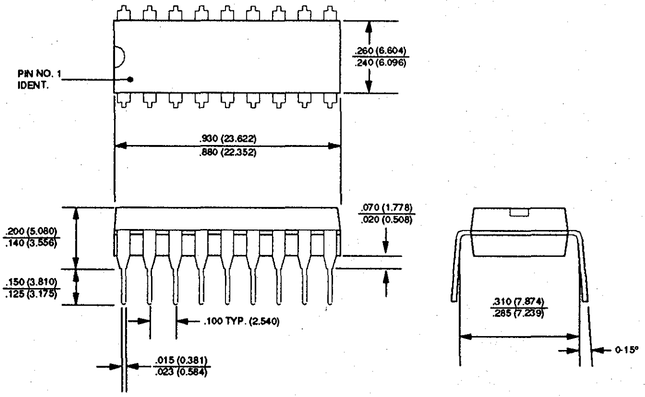
8-Pin Plastic



14-Pin Plastic



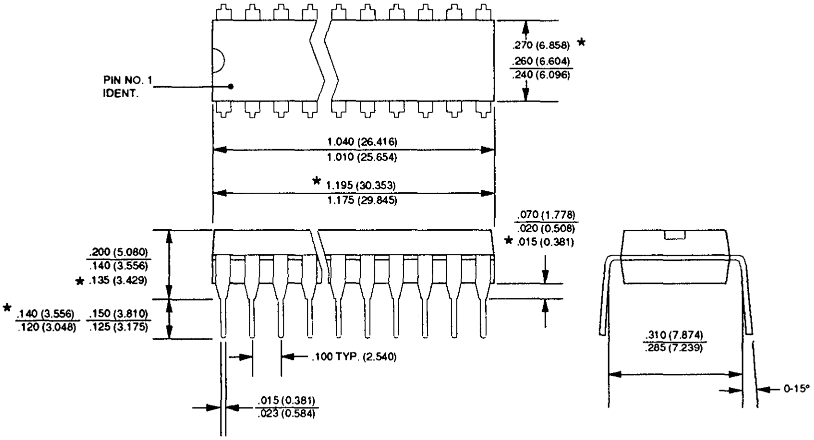
16-Pin Plastic



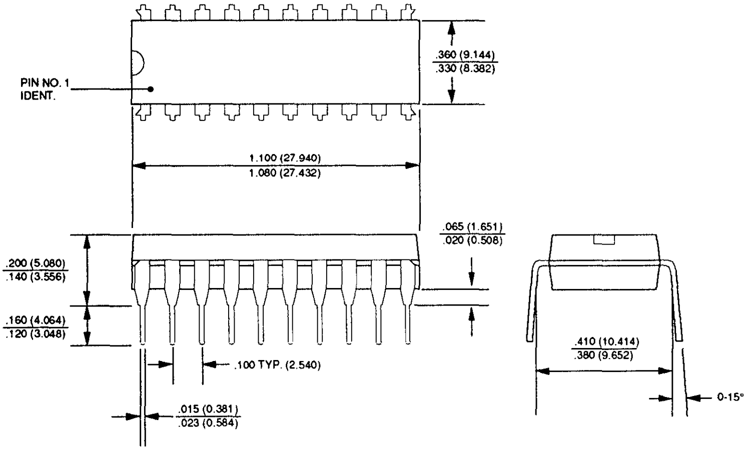
18-Pin Plastic

Package Information

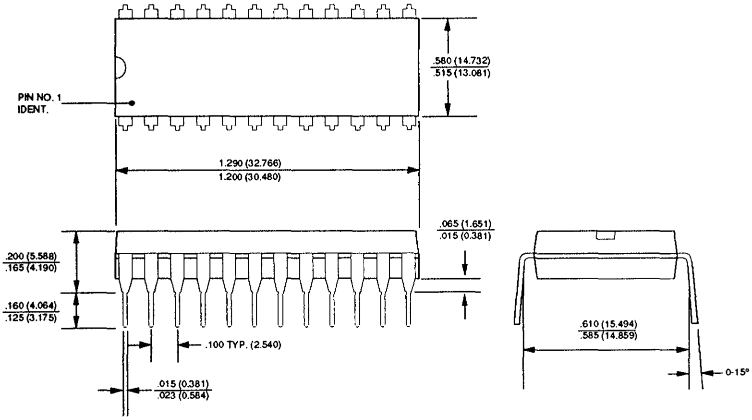
20 Pin Plastic
*24S Pin Plastic



22-Pin Plastic



24-Pin Plastic



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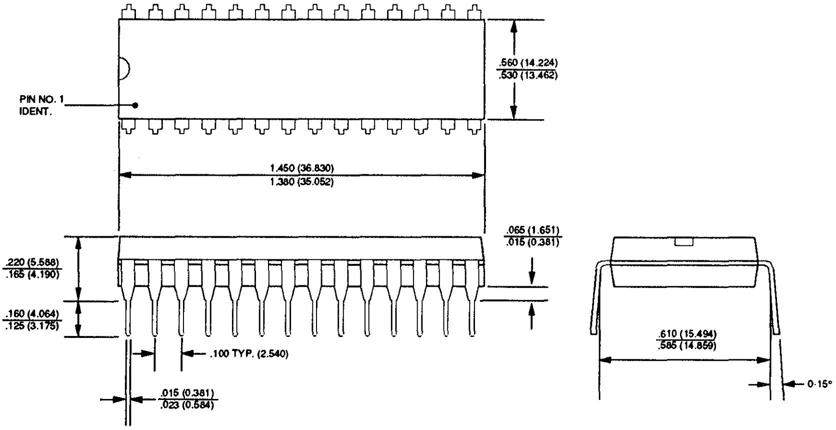
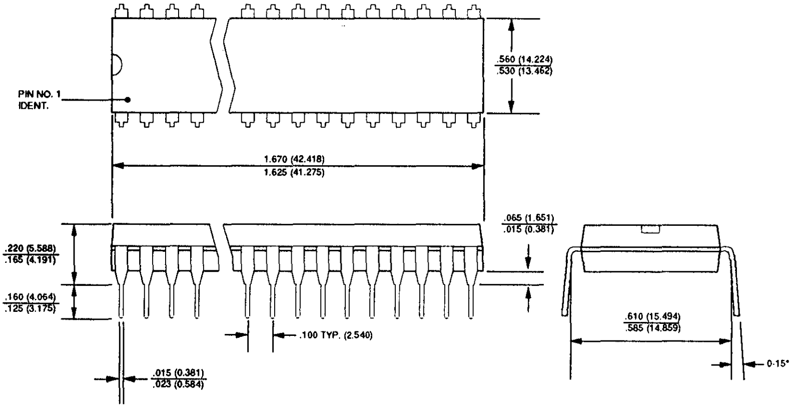
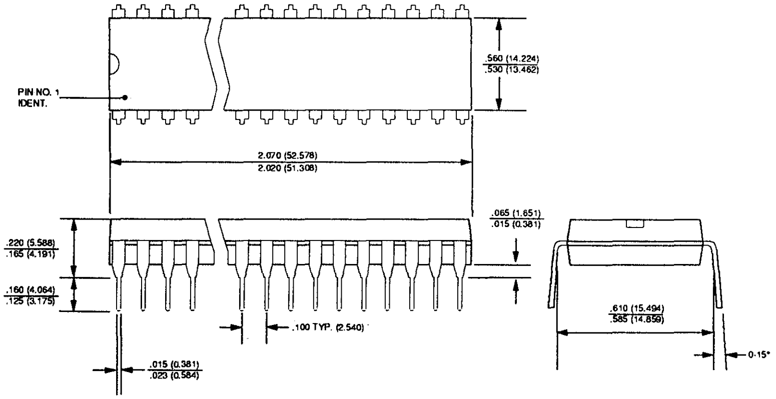


28-Pin Plastic



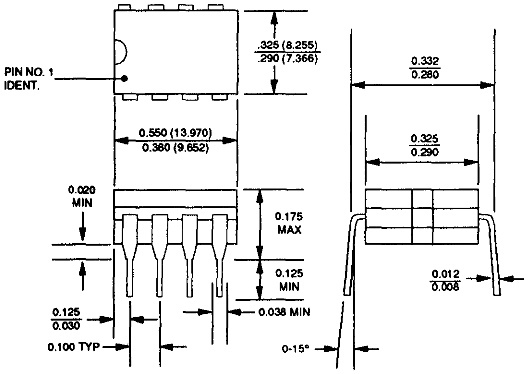
32-Pin Plastic



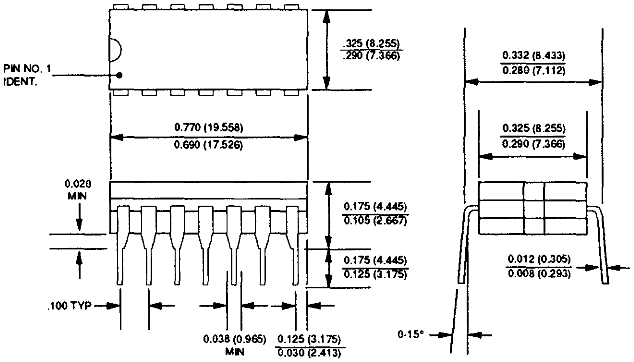
40-Pin Plastic

Package Information

Cerdip



8-Pin Cerdip



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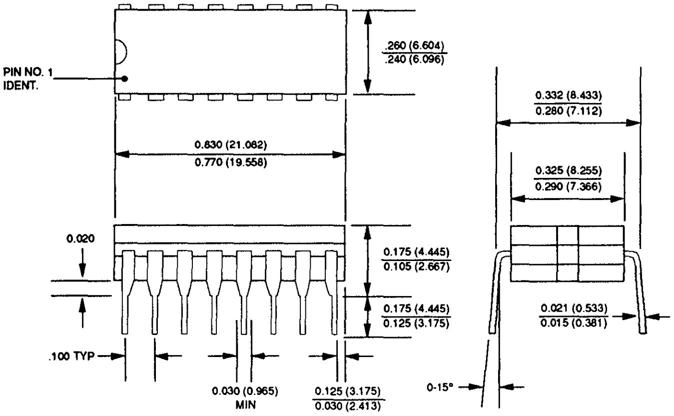

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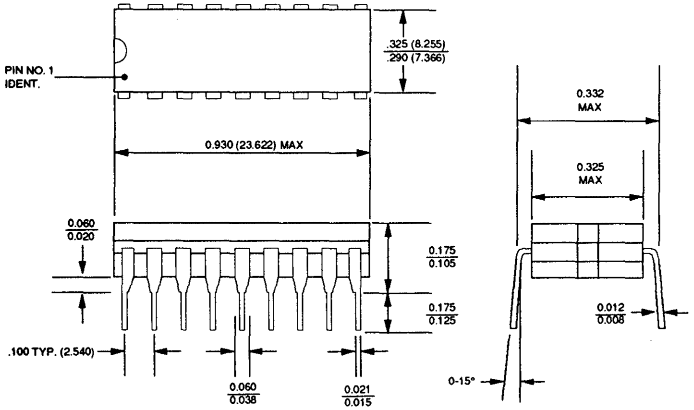
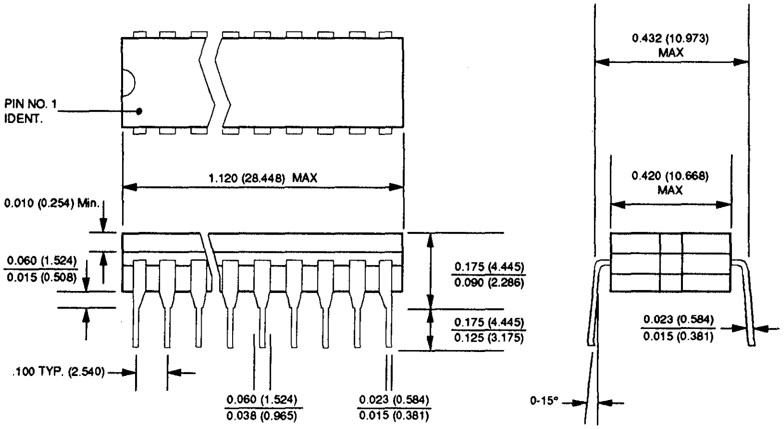


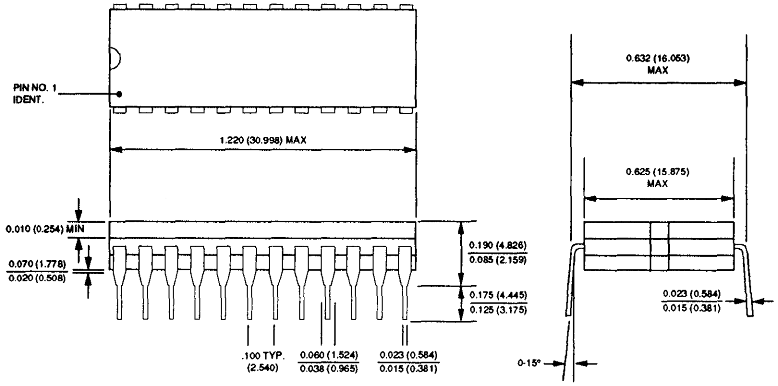
18-Pin Cerdip

Package Information

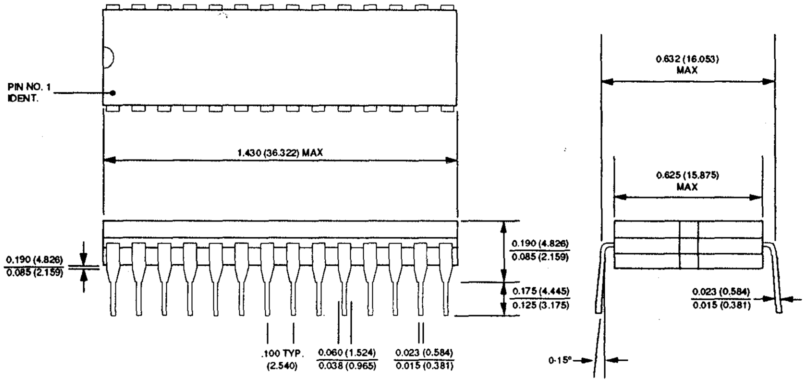
22-Pin Cerdip



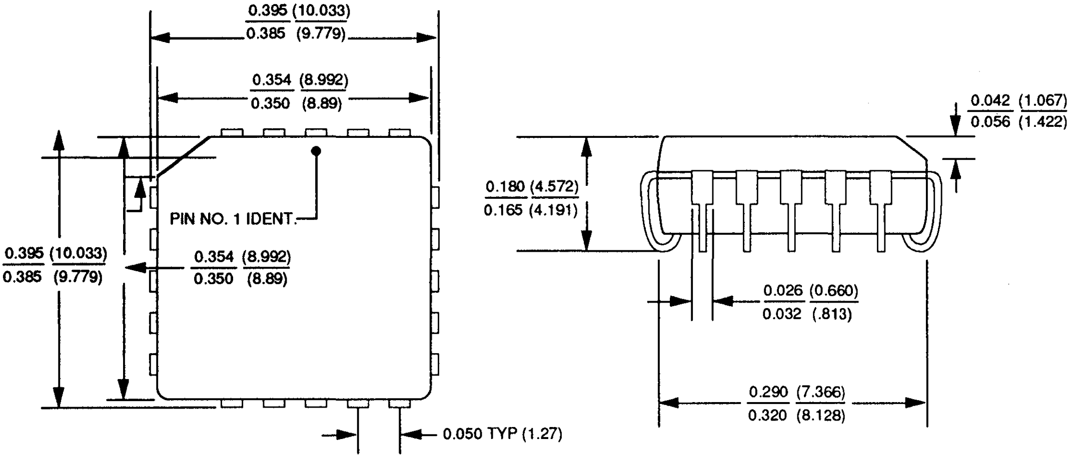
24-Pin Cerdip



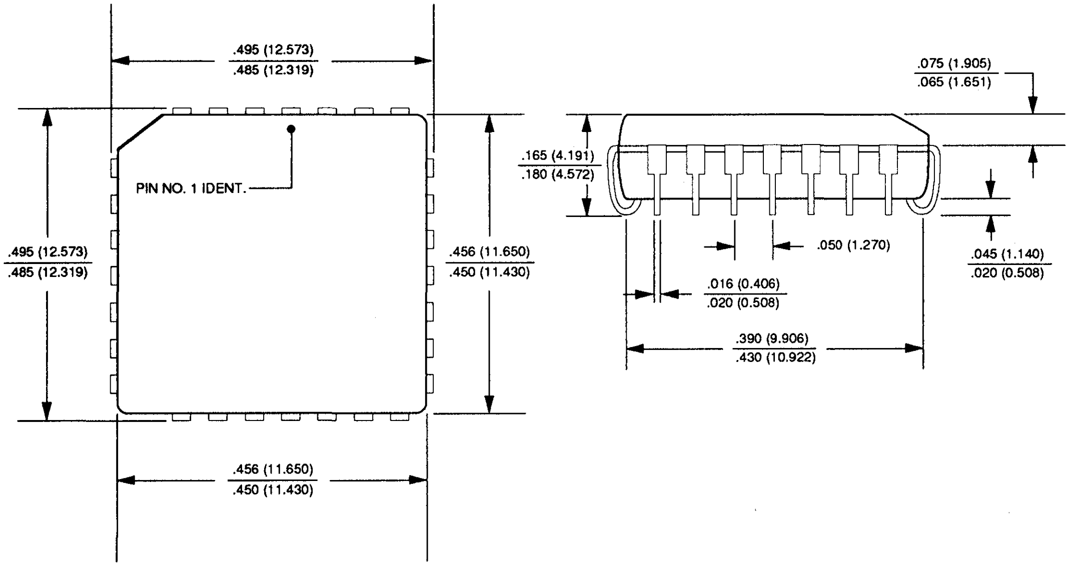
28-Pin Cerdip



Package Information
Quad (PLCC)

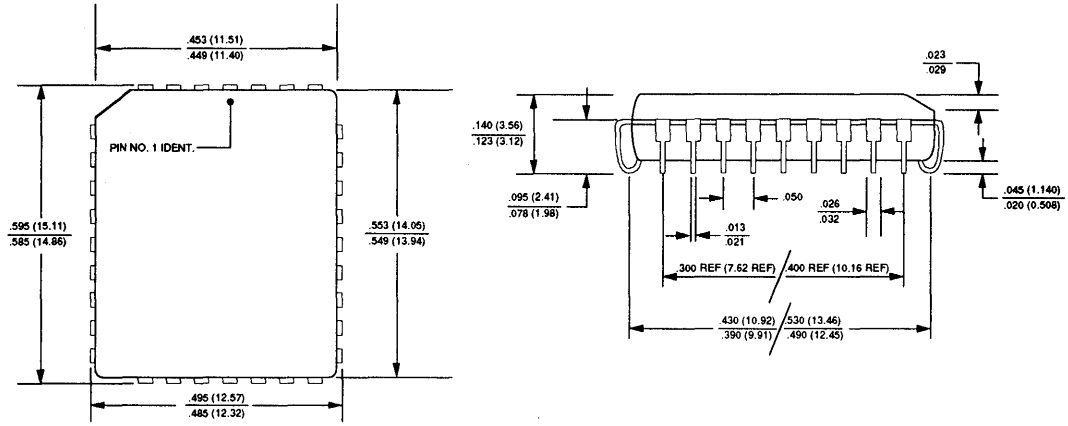


20-Pin Quad PLCC

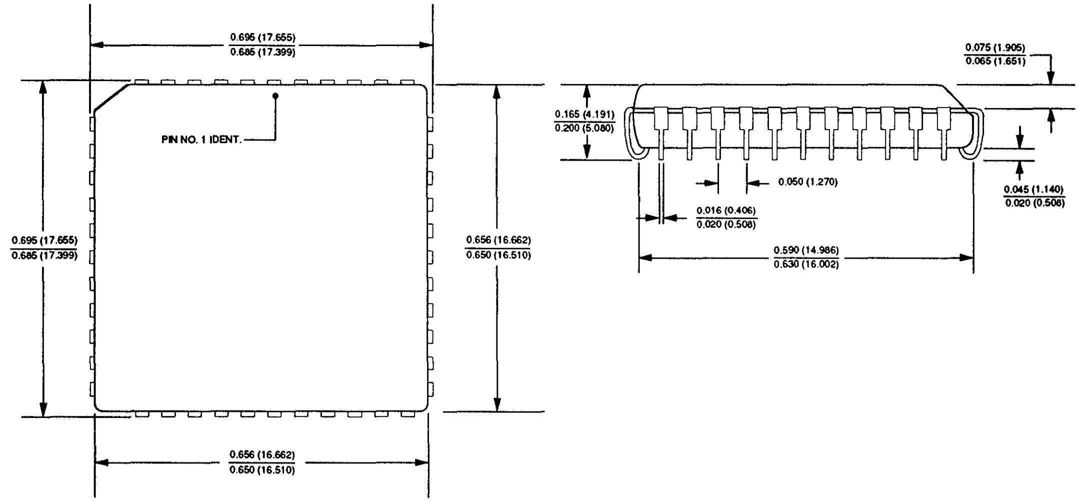


28-Pin Quad PLCC

Package Information

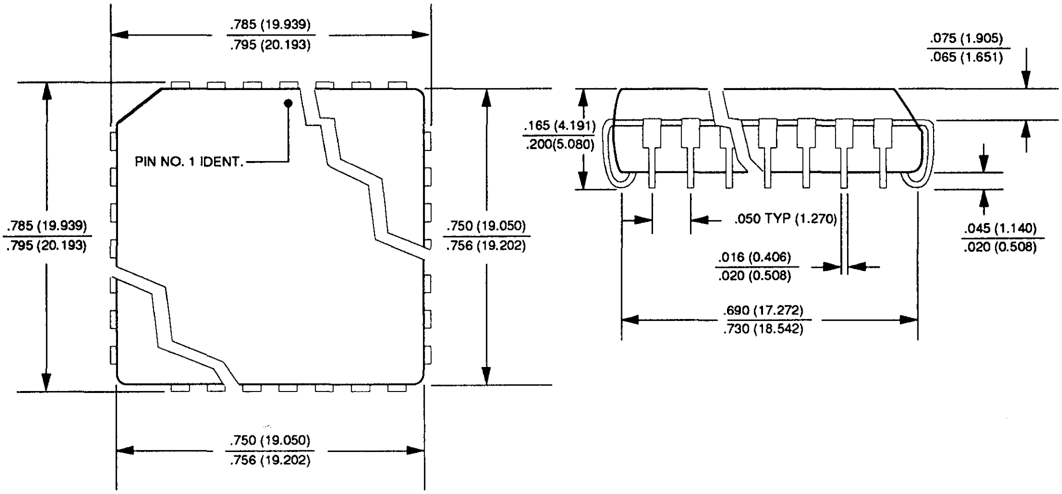


32-Pin Quad PLCC

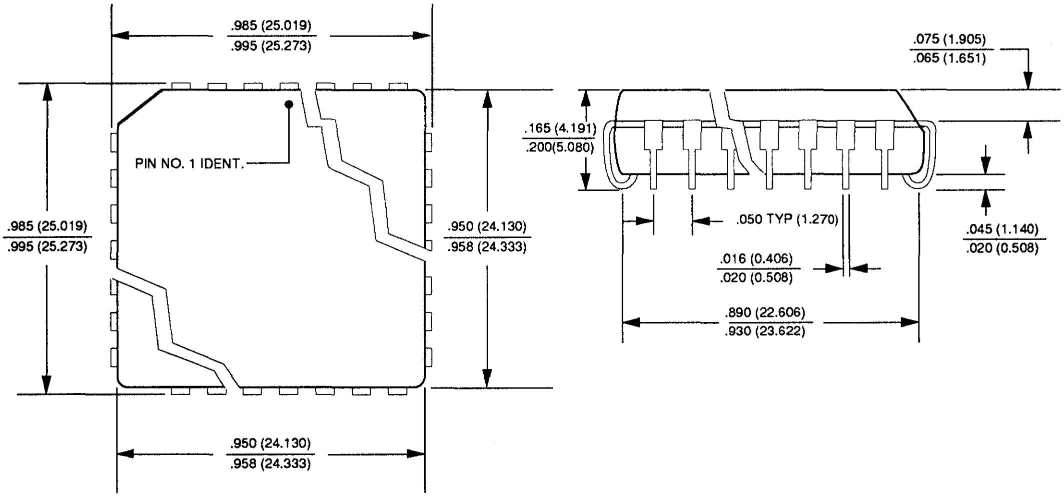


44-Pin Quad PLCC

Package Information

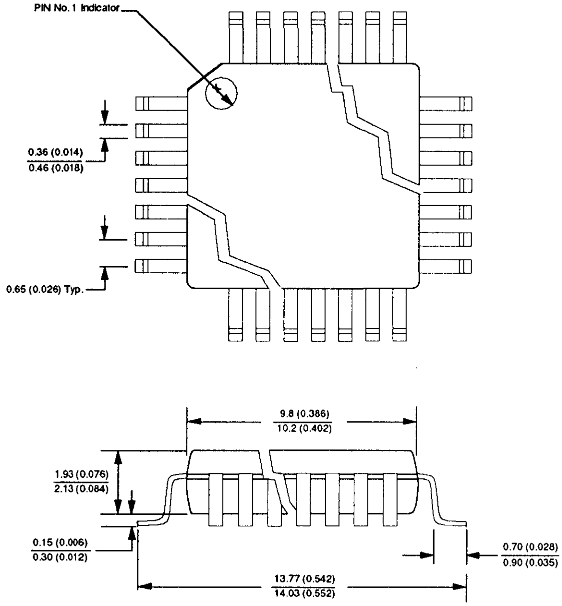


52-Pin Quad PLCC



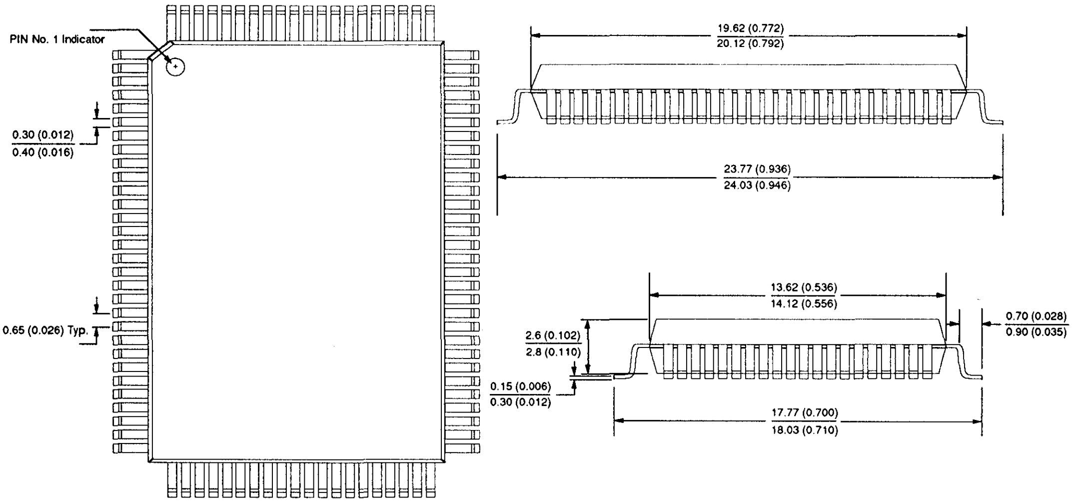
68-Pin Quad PLCC

Package Information
Quad Flatpack (QFP)



52-Lead Quad Flatpack

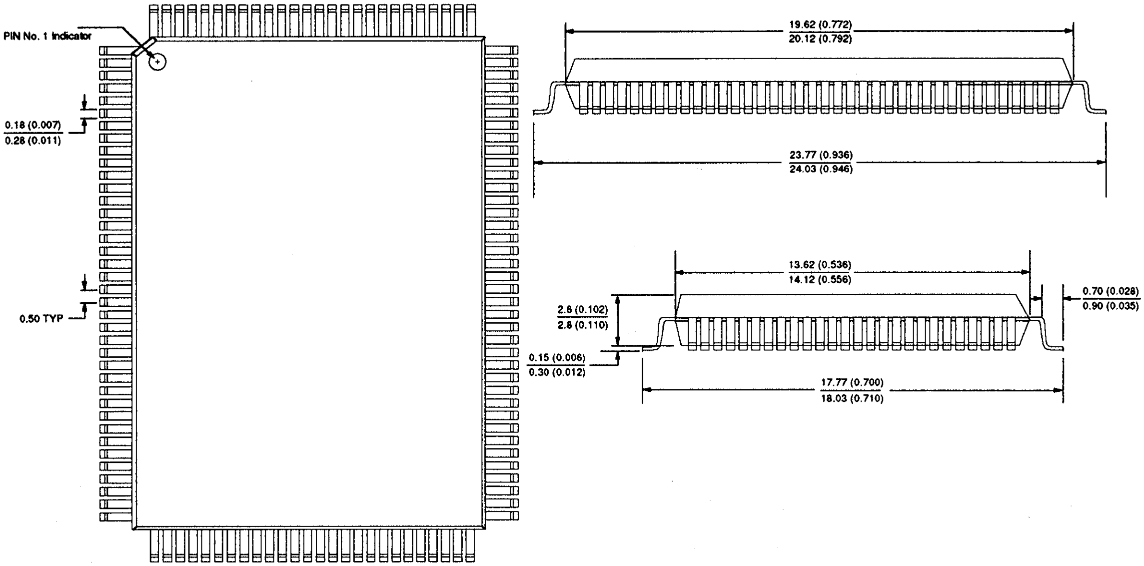
NOTE: Dimensions are in mm



100-Lead Quad Flatpack

NOTE: Dimensions are in mm

Package Information



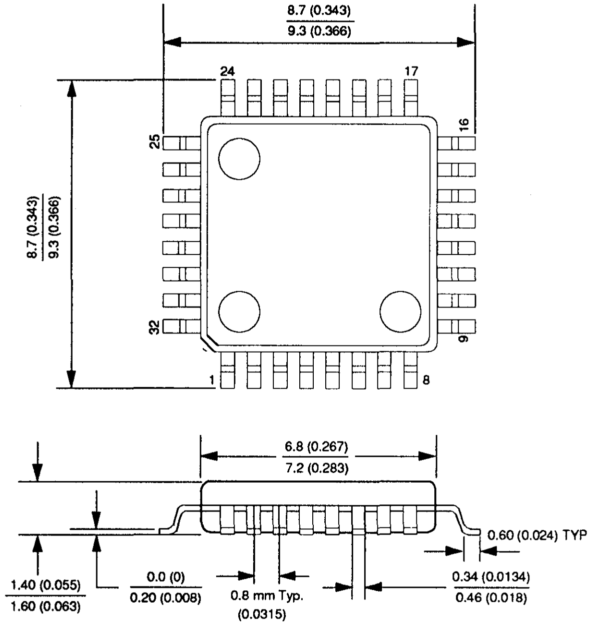
128-Lead Quad Flatpack

NOTE: Dimensions are in mm

Package Information
Thin Quad Flatpack (TQFP)

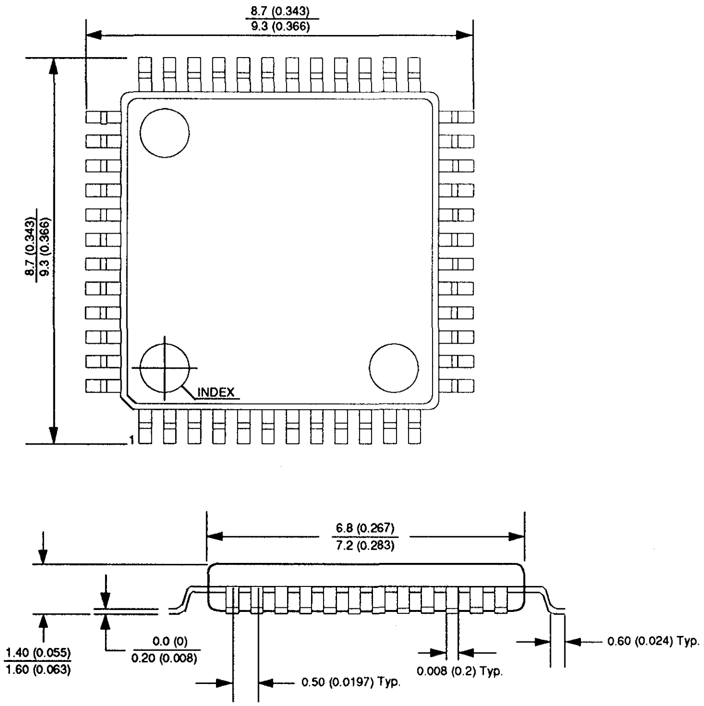
32-Lead Thin Quad Flatpack

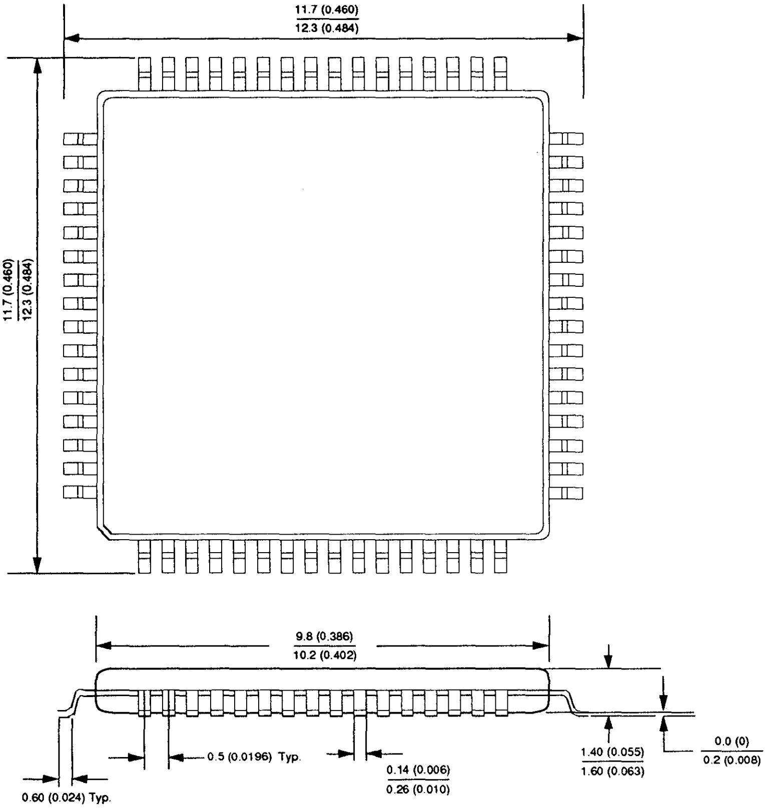
NOTE: Dimensions are in mm



48-Lead Thin Quad Flatpack

NOTE: Dimensions are in mm

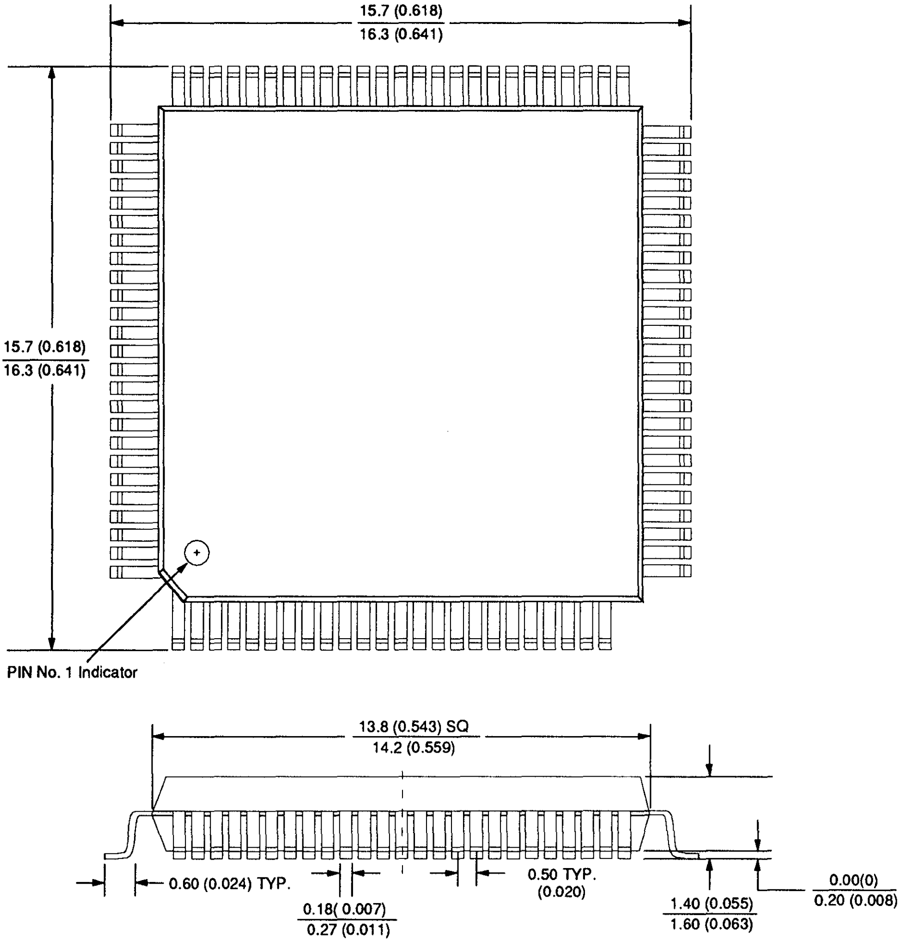




64-Lead Thin Quad Flatpack

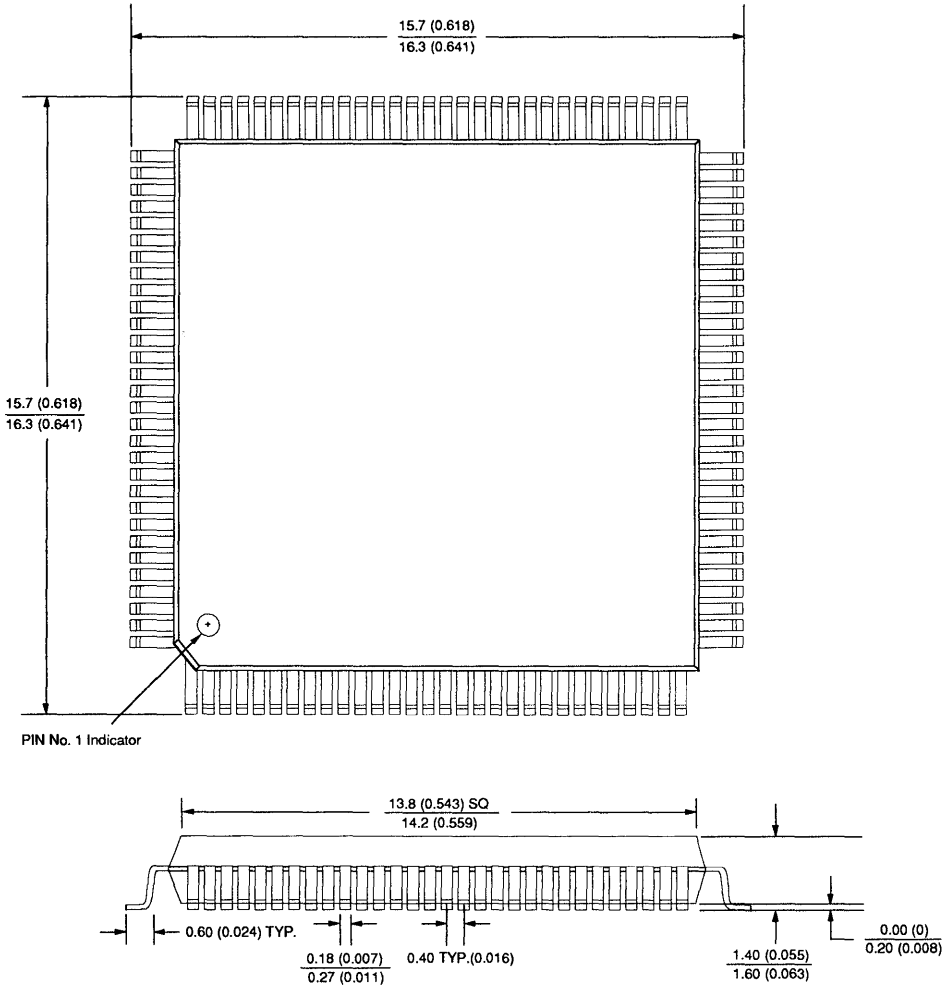
NOTE: Dimensions are in mm

Package Information



100-Lead Thin Quad Flatpack

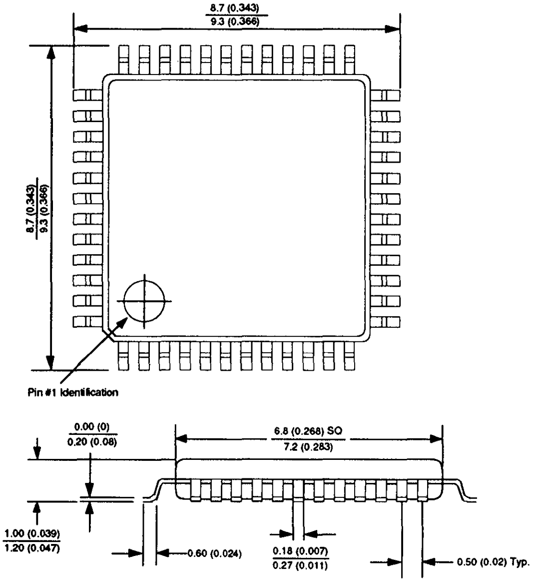
NOTE: Dimensions are in mm



120-Lead Thin Quad Flatpack

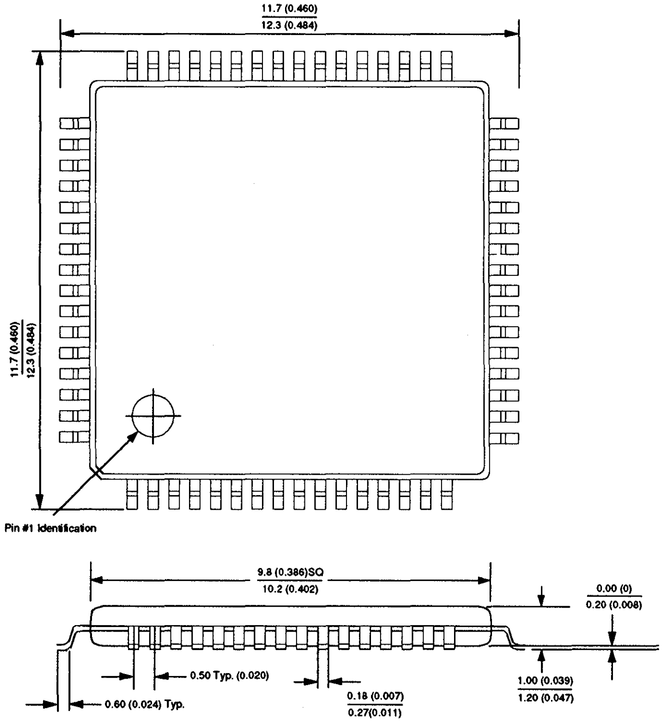
NOTE: Dimensions are in mm

Package Information
Very Thin Quad Flatpack (VTQFP)



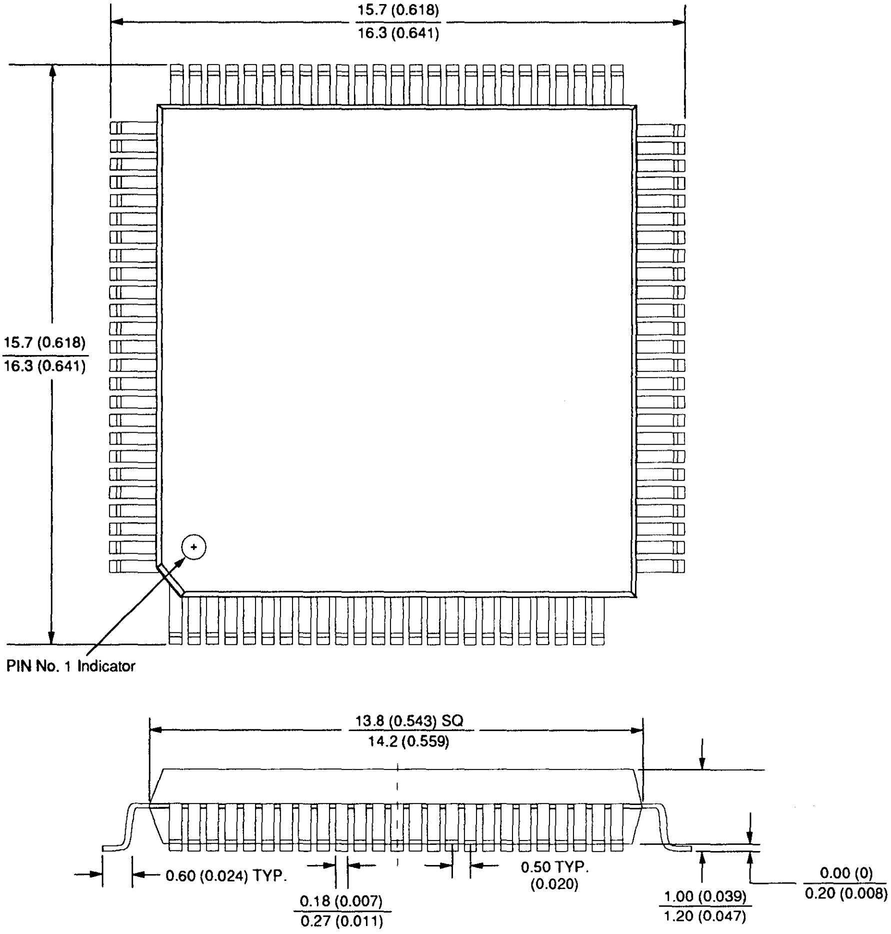
48-Lead VTQFP

NOTE: Dimensions are in mm



64-Lead VTQFP

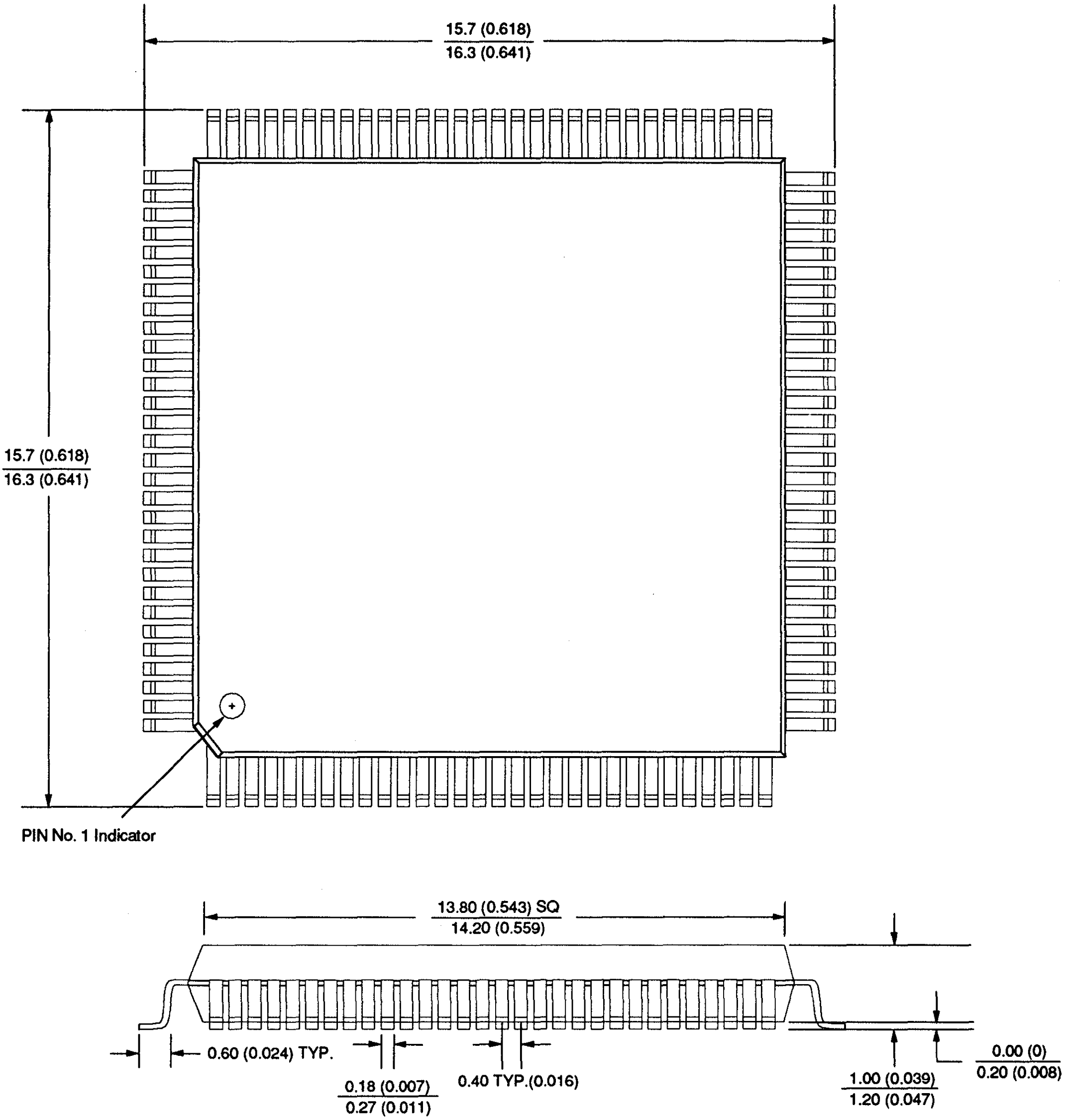
NOTE: Dimensions are in mm



100-Lead VTQFP

NOTE: Dimensions are in mm

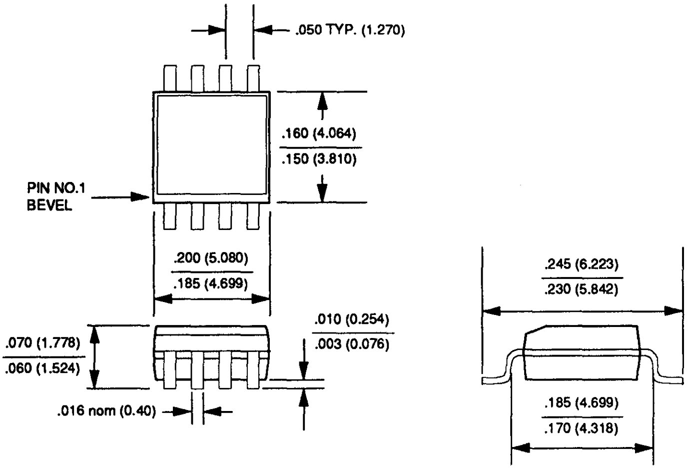
Package Information



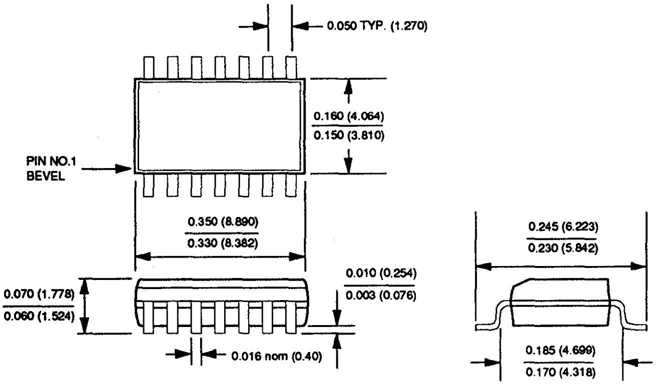
120-Lead VTQFP

NOTE: Dimensions are in mm

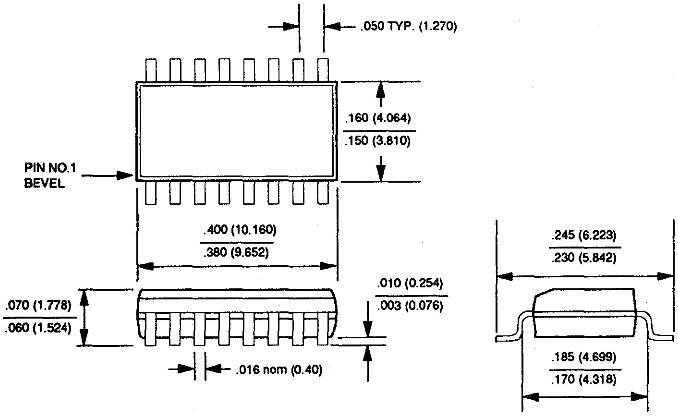
Package Information
SON



8-Lead SON

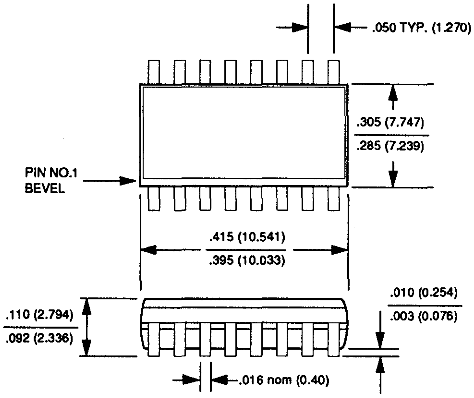


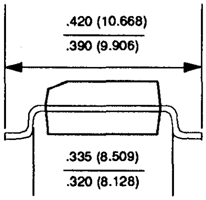
14-Lead SON

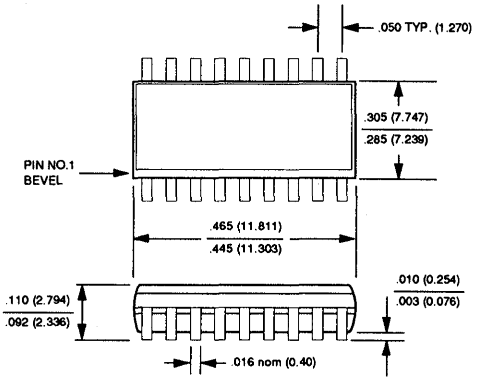


16-Lead SON

Package Information
SOL

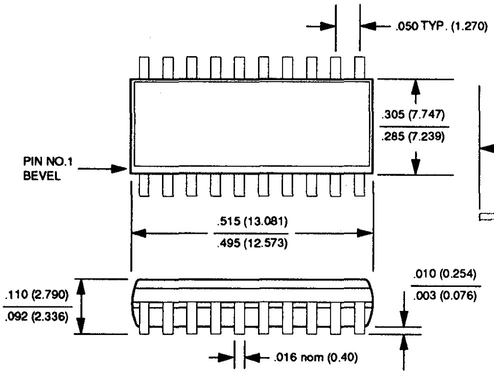


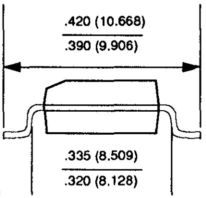


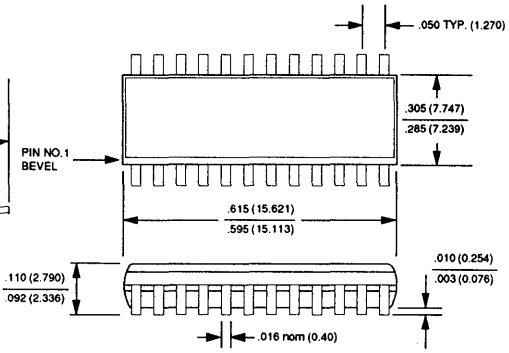


16-Lead SOL

18-Lead SOL

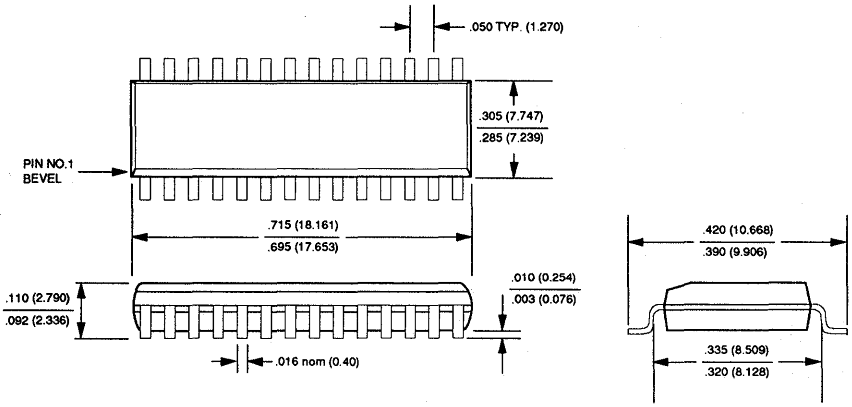






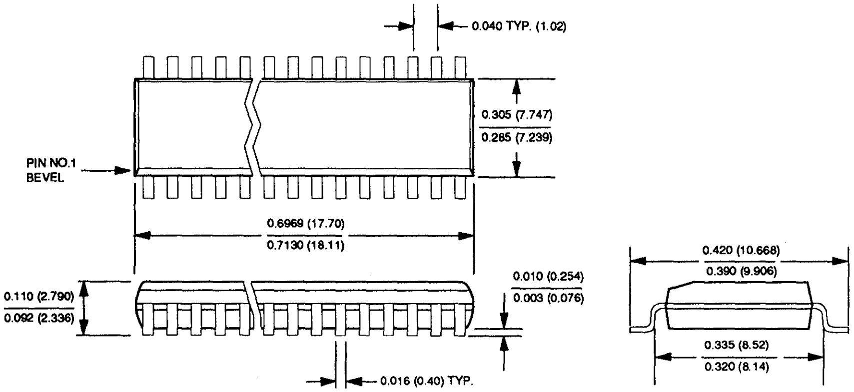
20-Lead SOL

24-Lead SOL

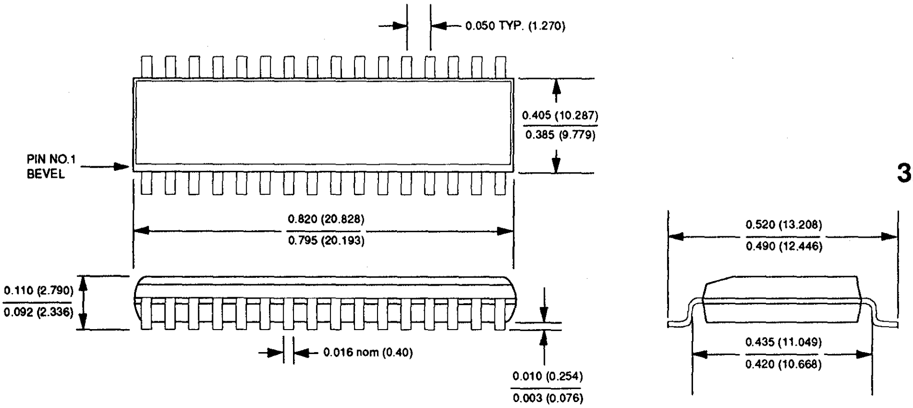


28-Lead SOL

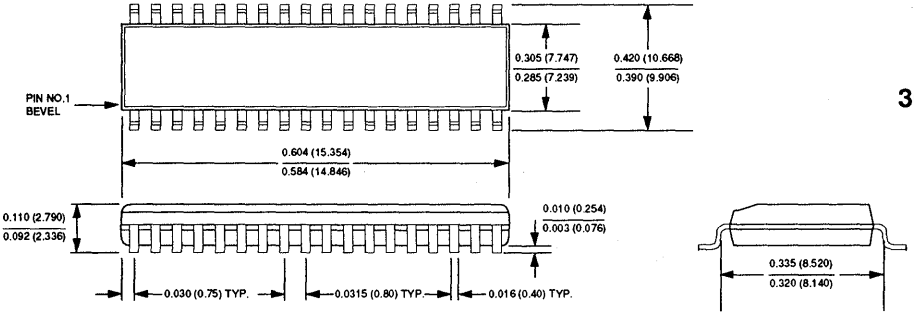
Package Information
SOL/SOM/SOW



34-Lead SOL

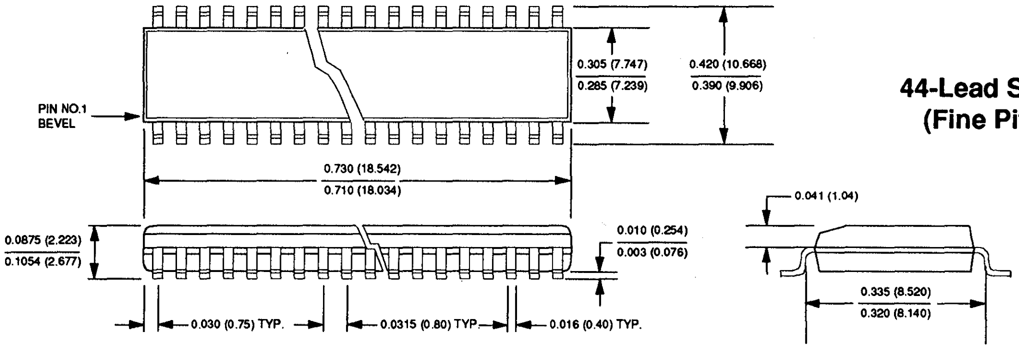


32-Lead SOW



36-Lead SOM (Fine Pitch)

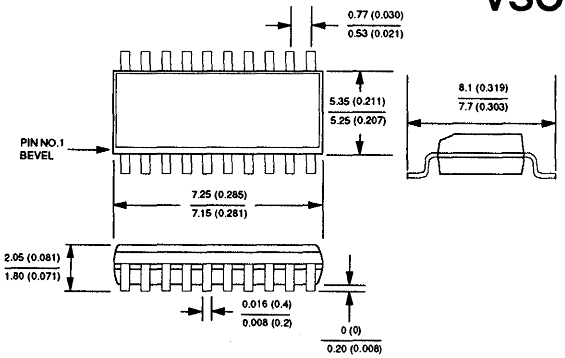
Package Information



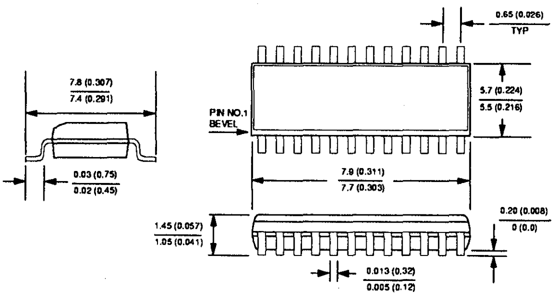
44-Lead SOM (Fine Pitch)

Package Information VSOP

NOTE: Dimensions are in mm



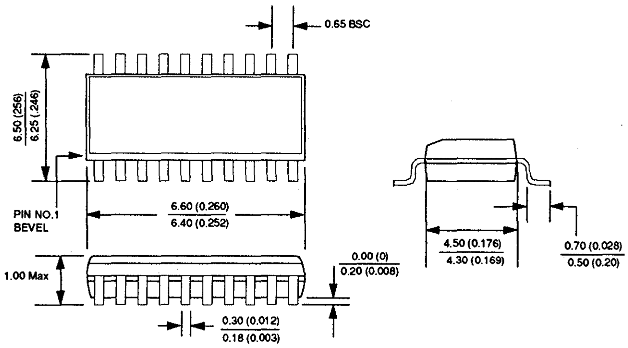
20-Lead VSOP



24-Lead VSOP

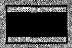
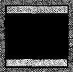
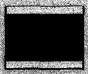
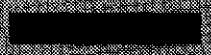
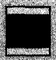
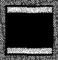
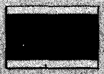
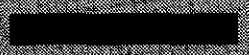
Package Information VTSOP

NOTE: Dimensions are in mm



20-Lead VTSOP

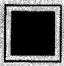
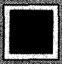
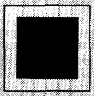
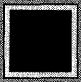
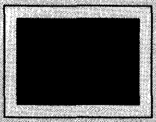
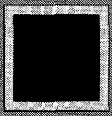
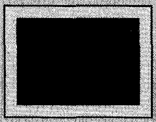
Small Outline Packages

PACKAGE TYPE	ACTUAL SIZE (AREA)	BODY SIZE (PITCH) mm	LAYOUT AREA mm^2	ACTUAL SIZE (HEIGHT)	HEIGHT mm
16 SON		9.8 x 3.9 (1.27)	9.8 x 6.0 = 58.8		1.65
16 SOL		10.2 x 7.5 (1.27)	10.2 x 10.2 = 104		2.54
20 SOL		12.8 x 7.5 (1.27)	12.8 x 10.2 = 130.6		2.54
24 SOL		15.4 x 7.5 (1.27)	15.4 x 10.2 = 157		2.54
20 SOV (VSOP)		7.2 x 5.4 (0.65)	7.2 x 7.9 = 56.9		1.9
24 SOV (VSOP)		7.8 x 5.6 (0.65)	7.8 x 7.9 = 59.3		1.25
36 SOM (SSOP)		15.1 x 7.5 (0.8)	15.1 x 10.2 = 154		2.54
44 SOM (SSOP)		18.3 x 7.5 (0.8)	18.3 x 10.2 = 186.7		2.54

■ = Actual Body Size: □ = Full Layout Area All dimensions are nominal values.

Small Form Factor Package Selector Guide

Quad Flatpack Packages

PACKAGE TYPE	ACTUAL SIZE (AREA)	BODY SIZE (PITCH) mm	LAYOUT AREA mm²	ACTUAL SIZE (HEIGHT)	HEIGHT mm
32G (QFP)		7.0 x 7.0 (0.8)	9.0 x 9.0 = 81		1.45
48 TQFP		7.0 x 7.0 (0.5)	9.0 x 9.0 = 81		1.4
52G (QFP)		10.0 x 10.0 (0.65)	14.0 x 14.0 = 196		2.2
64 TQFP		10.0 x 10.0 (0.5)	12.0 x 12.0 = 144		1.4
100G (QFP)		20.0 x 14.0 (0.65)	24.0 x 18.0 = 432		2.9
100 TQFP		14.0 x 14.0 (0.5)	17.2 x 17.2 = 296		1.4
128 QFP		20.0 x 14.0 (0.5)	24.0 x 18.0 = 432		2.54

■ = Actual Body Size: □ = Full Layout Area All dimensions are nominal values.

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Regional Offices & Sales Representatives

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HEADQUARTERS
Jon Tammel, Area Manager
Silicon Systems, Inc.
2001 Gateway Place
Suite 301 East
San Jose, CA 95110
Ph: (408) 453-7811
FAX: (408) 453-5988

CALIFORNIA
Magna Sales
Santa Clara
Ph: (408) 727-8753
FAX: (408) 727-8573

MINNESOTA
OHMS Technology, Inc.
Minneapolis
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FAX: (612) 932-2918

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Western Technical Sales
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FAX: (503) 644-8200

WASHINGTON
Western Technical Sales
Bellevue
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FAX: (206) 641-5829

Spokane
Ph: (509) 922-7600
FAX: (509) 922-7603

SOUTHWESTERN

HEADQUARTERS
Larry Cleland, Area Manager
Silicon Systems, Inc.
14351 Myford Road
Tustin, CA 92680
Ph: (714) 832-5310
FAX: (714) 832-5247

Colorado Sales Office
Howard Barlow
3445 Penrose Place, Suite 140
Boulder, CO 80301
Ph: (303) 440-9780
FAX: (303) 440-9783

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FAX: (602) 860-2712

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FAX: (719) 632-8419

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FAX: (208) 323-0834

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FAX: (505) 884-2258

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FAX: (512) 794-9987

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UTAH
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FAX: (801) 484-5408

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Ph: (603) 898-1444
FAX: (603) 898-9538

Georgia Sales Office
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Ph: (404) 409-8405
FAX: (404) 368-1060

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Brighton, MI 48116
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FAX: (313) 229-3266

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Huntsville
Ph: (205) 883-7893
FAX: (205) 882-6162

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FAX: (407) 671-4117

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West Caldwell
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Erdenheim, PA
Ph: (215) 233-4600
FAX: (215) 233-4702

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Electra Sales
Rochester
Ph: (716) 427-7860
FAX: (716) 427-0614

East Syracuse
Ph: (315) 463-1248
FAX: (315) 463-1717

Technical Marketing Group
Melville
Ph: (516) 351-8833
FAX: (516) 351-8667

NO. CAROLINA
Technology Mktg. Assoc. (TMA)
Raleigh
Ph: (919) 872-5104
FAX: (919) 872-5086

OHIO
Makin Associates
Cincinnati
Ph: (513) 871-2424
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FAX: (614) 793-0256

Solon
Ph: (216) 248-7370
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Omni Sales
Erdenheim
Ph: (215) 233-4600
FAX: (215) 233-4702

VIRGINIA
Burgin-Kreh Associates
Refer calls to
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Circuit Sales, Inc.
Brookfield
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Enerlec
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FAX: (604) 273-0884

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QUEBEC
Har-Tech
Pointe Claire
Ph: (514) 694-6110
FAX: (514) 694-8501

International

Distributors & Sales Representatives

EUROPE

HEADQUARTERS
Neil Harrison, Area Manager
Silicon Systems, Europe
The Business Centre
Gor-ray House
758-760 Great Cambridge Rd.
Enfield
Middlesex EN13RN
England
Ph: (44) 81-443-7061
FAX: (44) 81-443-7022
TLX: 825824 BUSTEC G (ref. ENFIELD)

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TLX: 603167 F

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FAX: (49) 89-857-3702

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TLX: 216-723 CARI GR

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FAX: 353-61-411888

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Milano
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FAX: (39) 2-9530-2780

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FAX: (31) 10-458-6482
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FAX: (41) 1-492-2255
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YUGOSLAVIA
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FAX: (90) 1-349-9430

RUSSIA
P.T.G.
Laguna Beach, California
Ph: (714) 499-6736

FAR EAST
(excluding Japan)

HEADQUARTERS
K. S. Ong, District Sales Manager
Silicon Systems, Singapore
3015A Ubi Road 1, #01-01
Kampong UBI Industrial Estate
Singapore 1440
Ph: (65) 744-7700
FAX: (65) 748-2431

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FAX: (408) 263-7585

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Seoul
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FAX: (82) 2-516-1151
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FAX: 604-281420

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FAX: (886) 2-777-5867
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THAILAND
Dynamar Computer Products
Bangkok
Ph: (662) 376-0132
FAX: (662) 376-0133

JAPAN

SSi/TDK CORP. HEADQUARTERS
Den Suzuki, Area Manager
1-13-1 Nihonbashi, Chuo-Ku
Tokyo 103, Japan
Ph: (81) 3-3278-5049
FAX: (81) 3-3278-5197
TLX: J24270
J26937

JAPAN
Internix
Tokyo
Ph: (81) 3-3369-1105
FAX: (81) 3-3363-8486
TLX: 781-26733

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Albuquerque, New Mexico
Ph: (505) 884-2256
FAX: (505) 884-2258

All other areas:

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Mexico City
Ph: (52) 5-754-6480
FAX: (52) 5-752-2787

Guadalajara
Ph: (52) 36-474250
FAX: (52) 36-473433

SOUTH AMERICA

ARGENTINA
Yel S.R.L.
Buenos Aires
Ph: (54) 45-7163
FAX: (54) 1-440-1533

BRAZIL
Hitech
Sao Paulo
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FAX: (55) 11-240-6250

CHILE
Victronics, Ltd.
Santiago Centro
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(56-2) 633-2787
FAX: (56-2) 633-4432

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FAX: (408) 255-6491
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FAX: (612) 881-9461

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NEW JERSEY
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Ph: (216) 349-4632

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Tulsa
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TEXAS
Austin
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Dallas
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Houston
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Salt Lake City
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Redmond
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Notes:

Notes:

Section 12

APPLICATION NOTES AND GLOSSARY

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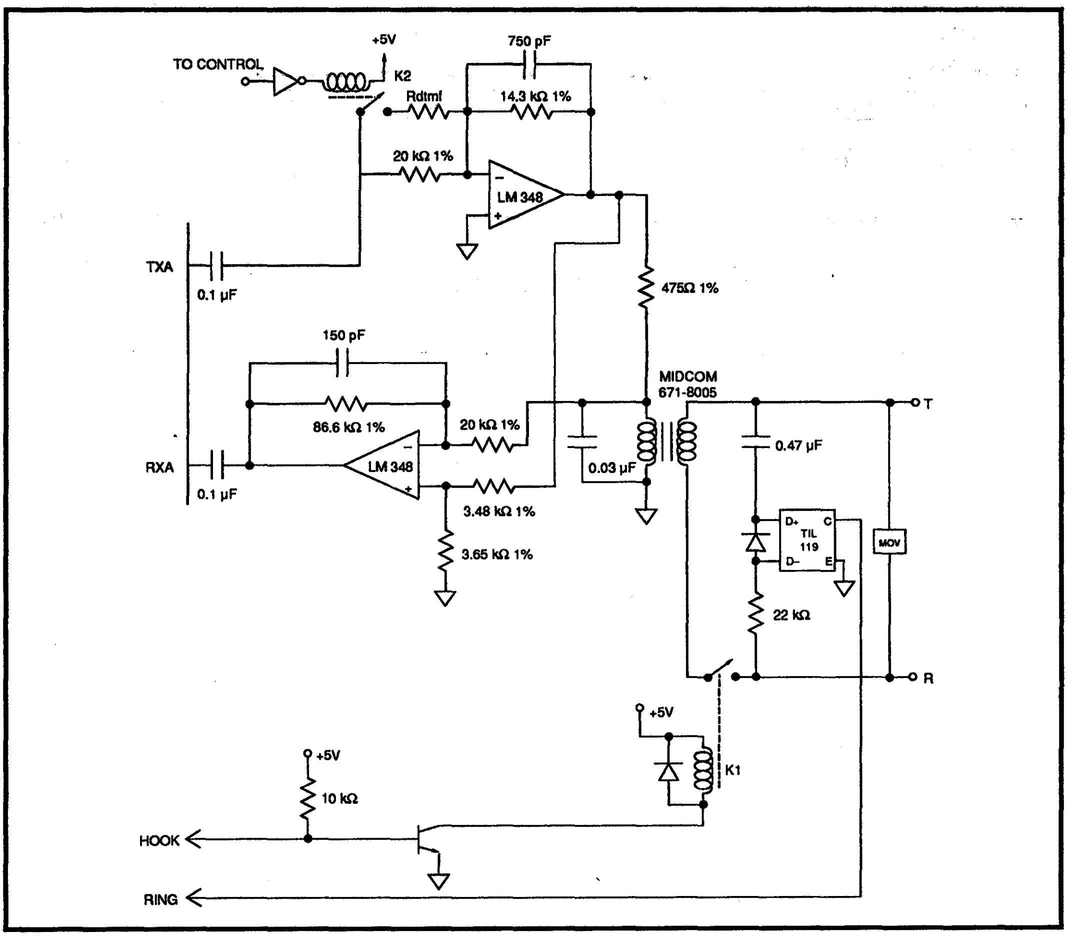
APPLICATION NOTE

Setting DTMF Levels for 1200 Bit/s K-Series Modems

Some applications of the K-series modems without output level adjustment may require setting the DTMF transmit level to something other than the normally transmitted level. This level is nominally about 5 dB higher than during data transmission. If the data is transmitted at -10 dBm, the DTMF levels will be at about -5 dBm, which is adequate in most applications.

The simplest way to change the relative levels of DTMF tones and data is to change the transmit gain during dialing. This can be accomplished as shown below. In this example, it is assumed that the DTMF tones are to be transmitted at a higher level than normal. Closing relay K2 will increase the gain of the transmit op-amp and allow a higher DTMF tone level during dialing. If it is desired to decrease the DTMF level, the relay can be open for dialing and closed for data. The value of the shunt resistor, Rdtmf, will be relatively large compared to the resistor R1, therefore the precision of Rdtmf is not as critical as R1. This means an analog switch or similar device could be used instead of a relay, with the on resistance of the switch not seriously affecting the tolerance of the gain setting.



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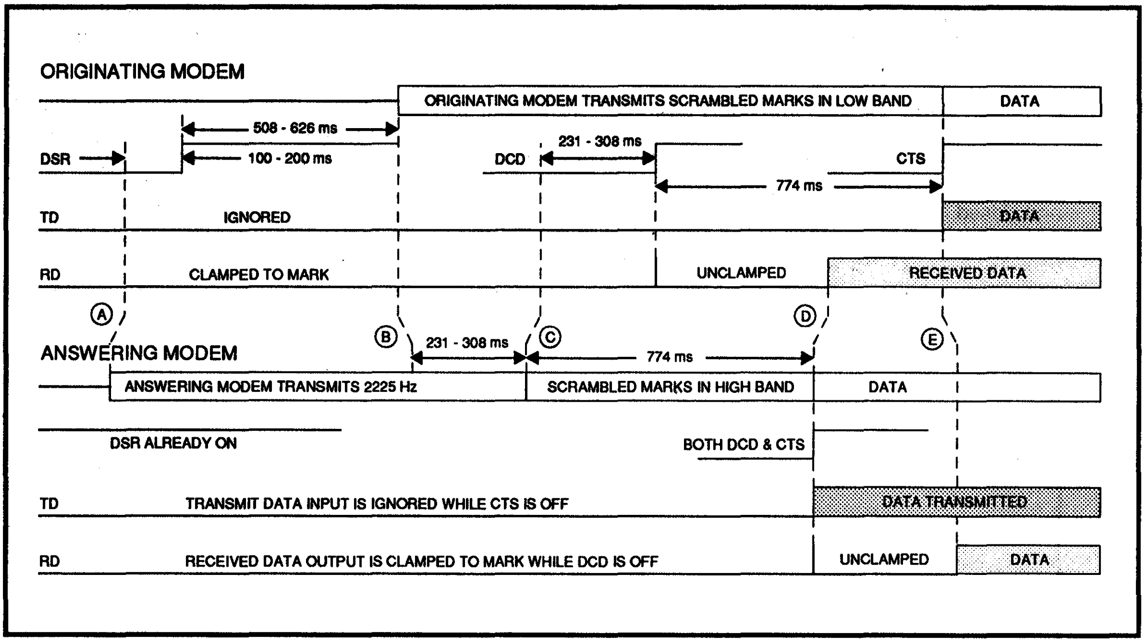
APPLICATION NOTE

SSI 73K212A High Speed Connect Sequence



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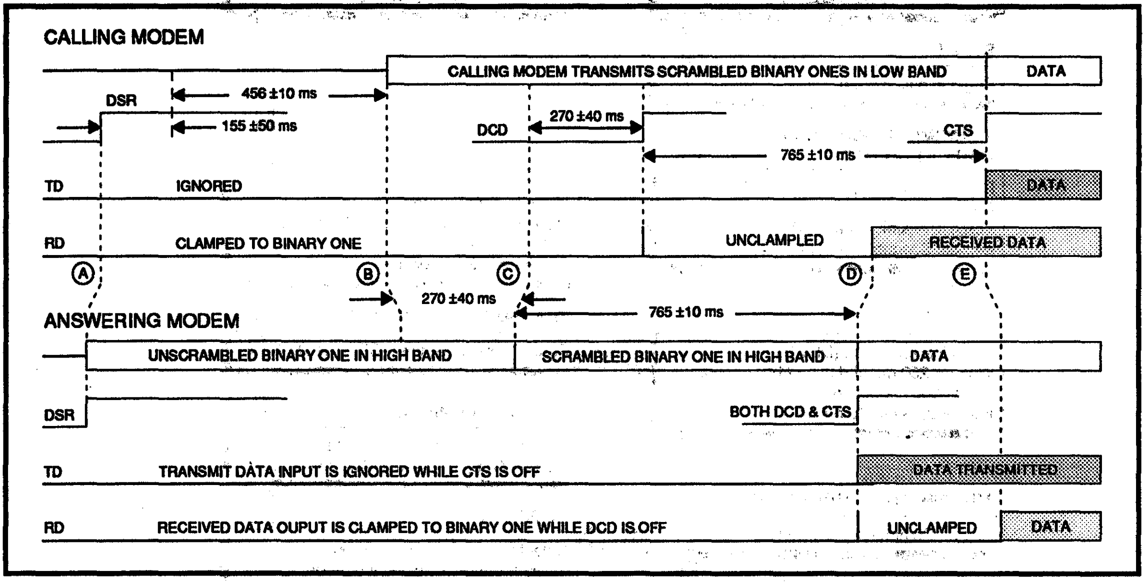
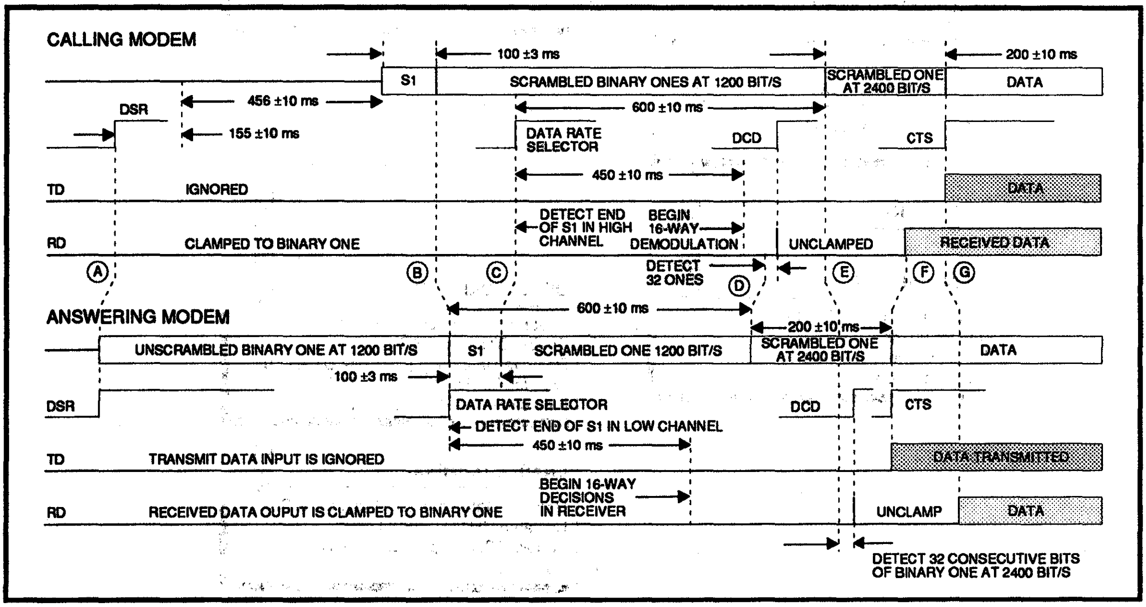
APPLICATION NOTE

V.22 & V.22bis Connect Sequences

V.22



V.22bis



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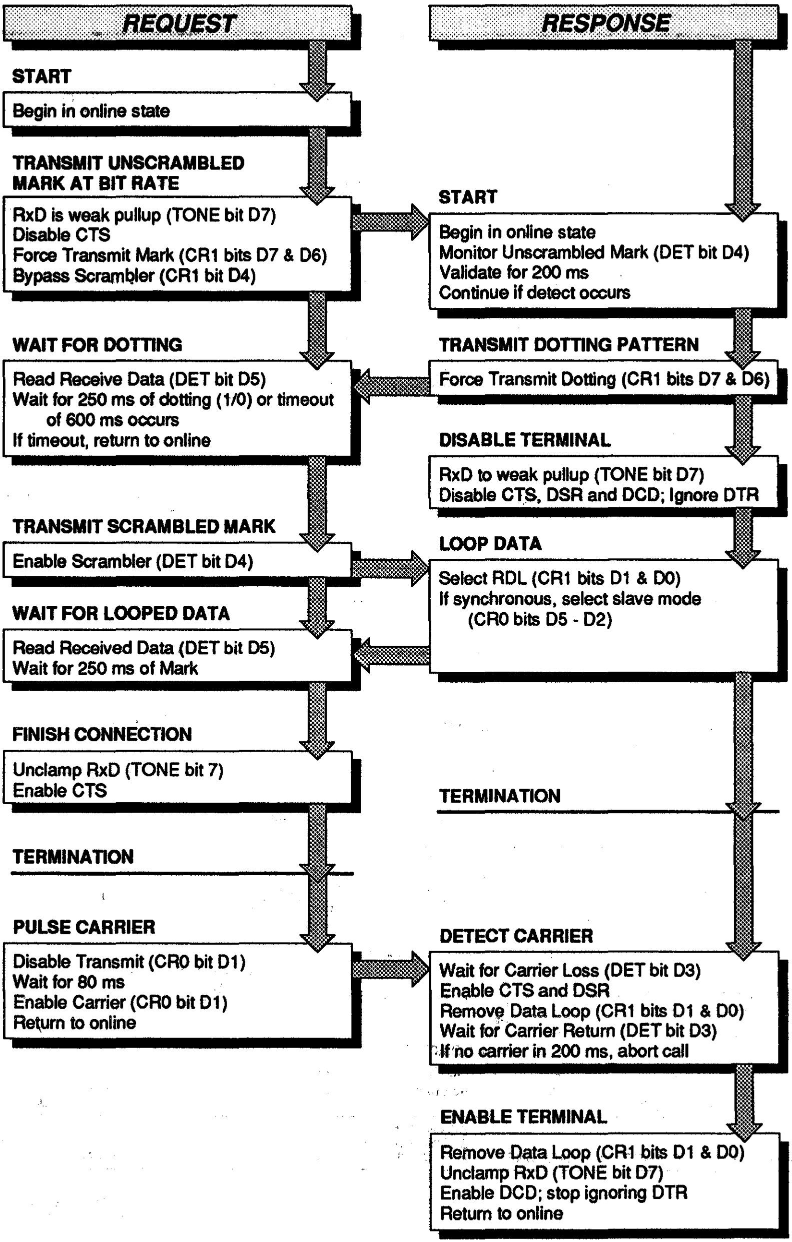
APPLICATION NOTE

Remote Loop Handshake Sequence



REQUEST

START

Begin in online state

TRANSMIT UNSCRAMBLED MARK AT BIT RATE

RxD is weak pullup (TONE bit D7)
Disable CTS
Force Transmit Mark (CR1 bits D7 & D6)
Bypass Scrambler (CR1 bit D4)

WAIT FOR DOTTING

Read Receive Data (DET bit D5)
Wait for 250 ms of dotting (1/0) or timeout of 600 ms occurs
If timeout, return to online

TRANSMIT SCRAMBLED MARK

Enable Scrambler (DET bit D4)

WAIT FOR LOOPED DATA

Read Received Data (DET bit D5)
Wait for 250 ms of Mark

FINISH CONNECTION

Unclamp RxD (TONE bit 7)
Enable CTS

TERMINATION

PULSE CARRIER

Disable Transmit (CR0 bit D1)
Wait for 80 ms
Enable Carrier (CR0 bit D1)
Return to online

RESPONSE

START

Begin in online state
Monitor Unscrambled Mark (DET bit D4)
Validate for 200 ms
Continue if detect occurs

TRANSMIT DOTTING PATTERN

Force Transmit Dotting (CR1 bits D7 & D6)

DISABLE TERMINAL

RxD to weak pullup (TONE bit D7)
Disable CTS, DSR and DCD; Ignore DTR

LOOP DATA

Select RDL (CR1 bits D1 & D0)
If synchronous, select slave mode (CR0 bits D5 - D2)

TERMINATION

DETECT CARRIER

Wait for Carrier Loss (DET bit D3)
Enable CTS and DSR
Remove Data Loop (CR1 bits D1 & D0)
Wait for Carrier Return (DET bit D3)
If no carrier in 200 ms, abort call

ENABLE TERMINAL

Remove Data Loop (CR1 bits D1 & D0)
Unclamp RxD (TONE bit D7)
Enable DCD; stop ignoring DTR
Return to online

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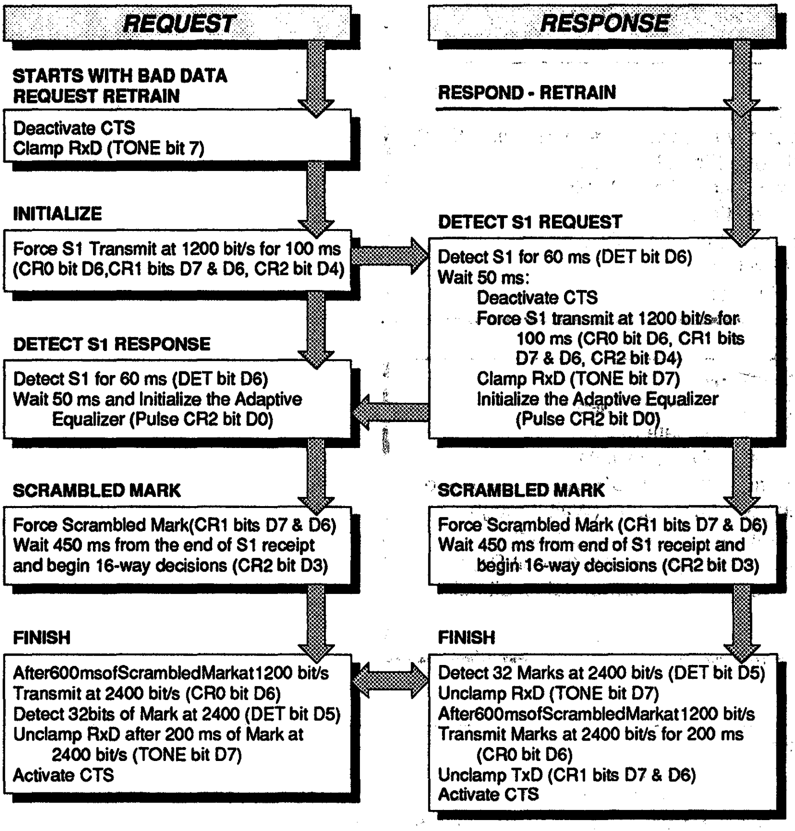
APPLICATION NOTE

SSI 73K224
Retrain at 2400



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APPLICATION NOTE

SSI 73K212 & 73K222 Originate Handshake Sequence

(RXD is in tri-state mode, TONE bit D7≤1)

DIAL

1. Go off hook
2. Bring out of power down mode (CR0 bits D5-D2)
3. Set DTMF tone (Tone bits D4-D0)
4. Turn on transmitter (Set CR0 bit D1)
5. Wait DTMF on time
6. Turn off transmitter (Clear CR0 bit D1)
7. Wait DTMF off time
8. Repeat 3-7 for all digits

WAIT FOR CARRIER

1. Start S7 (Wait for carrier) timeout
2. Set to Bell 103 originate mode (Set CR0 bits D5-D0 to 110001)
3. Wait for carrier detect bit (DR bit D3) to come on
4. Start sliding window counter (Wait through possible 2100 Hz answer tone period)
5. Qualify RXD mark* for 150 ms (DR bit D5) to detect answer modem (Carrier detect bit must also be on)
6. Raise DSR

FSK

1. Wait 100-200 ms
2. Raise DCD, start 755-774 ms timer; wait 426-446 ms, send FSK marks (Set CR1 bits D7 & D6 to 10, set CR0 bit D1)
3. At end of 755-774 ms timer period (started in #2 above); raise CTS, unclamp RXD & TXD from marking (clear TONE bit D7; clear CR1 bits D7 & D6)

DPSK

1. Wait 456 (V.22) or 508-626 ms (212A), switch to DPSK
2. Send scrambled marks (Set CR1 bits D7 & D6 to 10)
3. Qualify scrambled marks from answer modem for 150 ms
4. Wait for 231-302 ms of scrambled marks, raise DCD
5. Enable RXD (Tone bit D7)
6. Wait 774 ms, raise CTS, enable TXD (Clear CR1 bits D7 & D6)

*This may be either answer tone from a Bell modem or unscrambled marks from a V.22 modem

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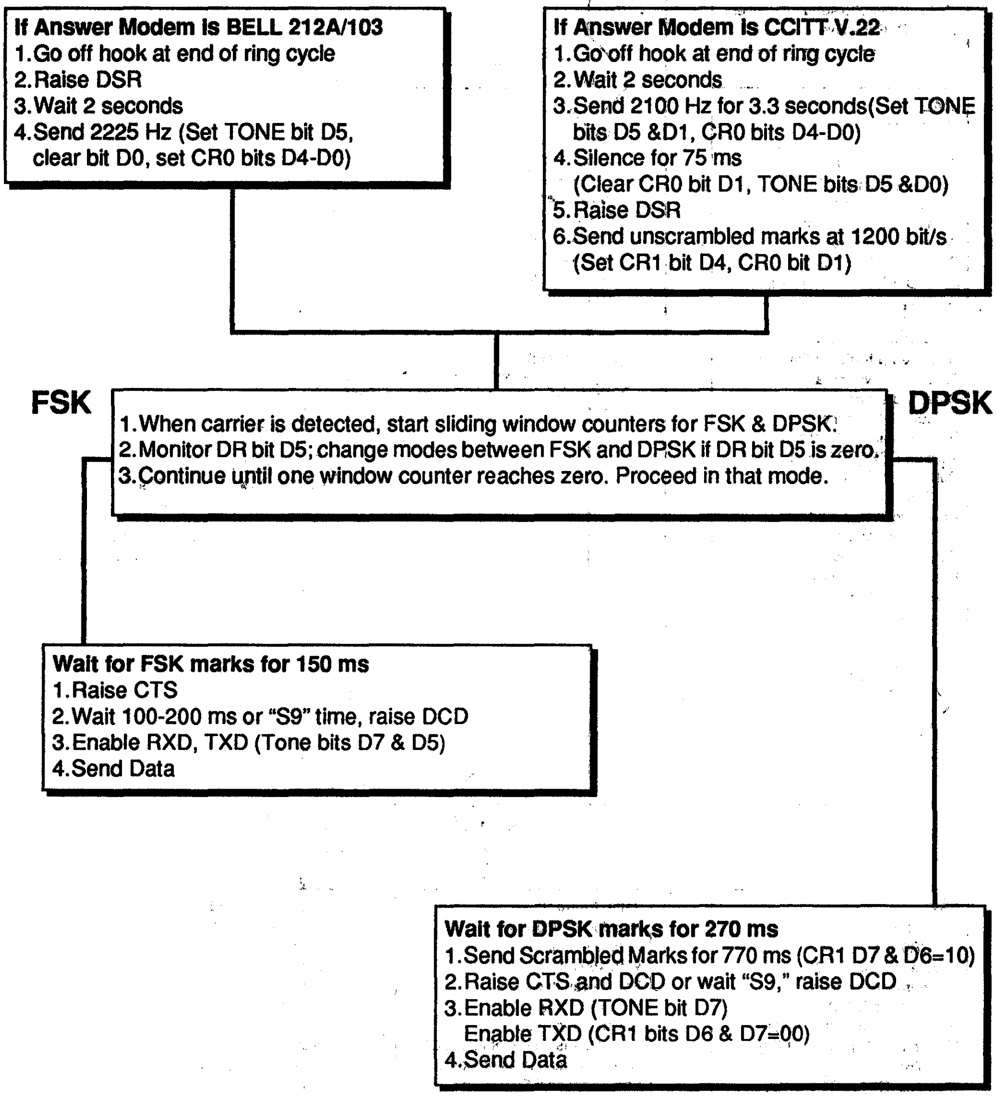
APPLICATION NOTE

SSI 73K212 & 73K222 Answer Handshake Sequence

(RXD is in tri-state mode, TONE bit D7=1)



If Answer Modem is BELL 212A/103
1. Go off hook at end of ring cycle
2. Raise DSR
3. Wait 2 seconds
4. Send 2225 Hz (Set TONE bit D5, clear bit D0, set CR0 bits D4-D0)

If Answer Modem is CCITT V.22
1. Go off hook at end of ring cycle
2. Wait 2 seconds
3. Send 2100 Hz for 3.3 seconds(Set TONE bits D5 &D1, CR0 bits D4-D0)
4. Silence for 75 ms (Clear CR0 bit D1, TONE bits D5 &D0)
5. Raise DSR
6. Send unscrambled marks at 1200 bit/s (Set CR1 bit D4, CR0 bit D1)

1. When carrier is detected, start sliding window counters for FSK & DPSK.
2. Monitor DR bit D5; change modes between FSK and DPSK if DR bit D5 is zero.
3. Continue until one window counter reaches zero. Proceed in that mode.

Wait for FSK marks for 150 ms
1. Raise CTS
2. Wait 100-200 ms or "S9" time, raise DCD
3. Enable RXD, TXD (Tone bits D7 & D5)
4. Send Data

Wait for DPSK marks for 270 ms
1. Send Scrambled Marks for 770 ms (CR1 D7 & D6=10)
2. Raise CTS and DCD or wait "S9," raise DCD
3. Enable RXD (TONE bit D7)
   Enable TXD (CR1 bits D6 & D7=00)
4. Send Data

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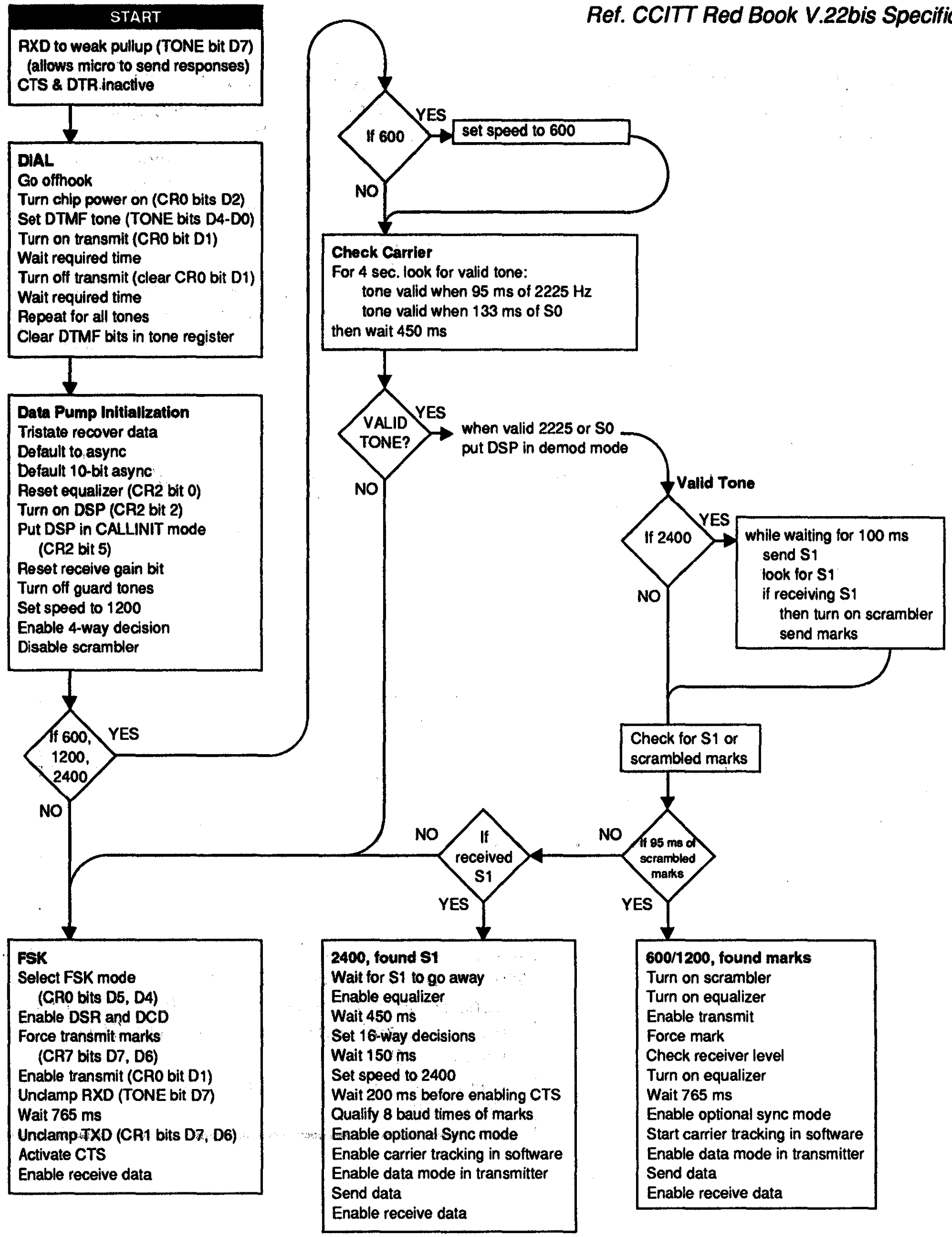
APPLICATION NOTE

SSI 73K224 Originate Handshake Sequence

Ref. CCITT Red Book V.22bis Specification



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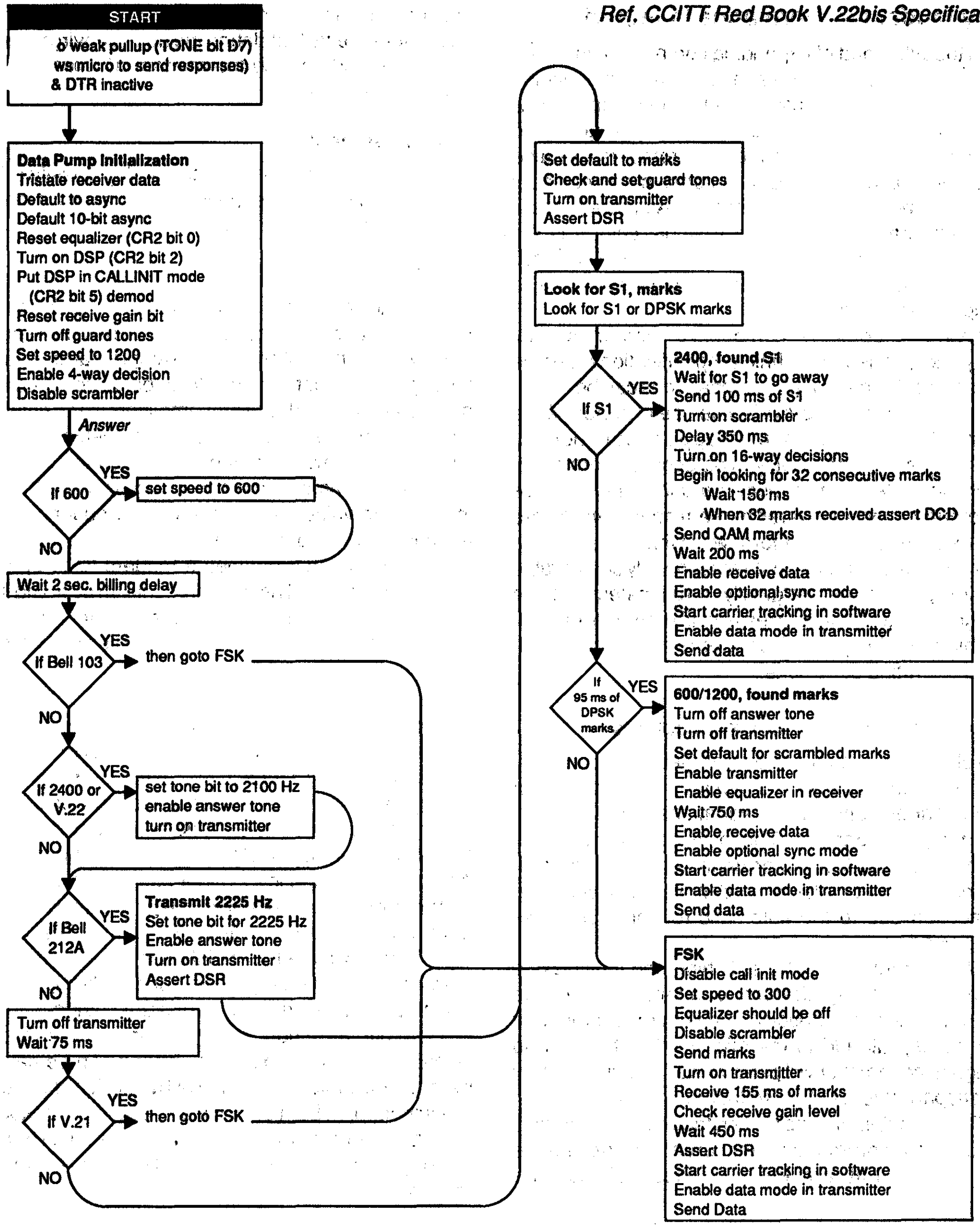
APPLICATION NOTE

SSI 73K224 Answer Handshake Sequence

Ref. CCITT Red Book V.22bis Specification



APPLICATION NOTE

Performance Testing

Silicon Systems K-Series Single-Chip Modem Family

Why Modem Performance Is Important

In today's world of expanding communications, the modem has become an essential element in providing data communications capability for such applications as personal computers, lap-top PCs, and hand-held portable terminals. To fit the requirements of these systems, the modem must become more compact even as it becomes more complex. As more modem functions are integrated onto a single chip, it is the modem IC that becomes the key to designing small footprint modems that integrate well into today's computer applications.

Trying to compare competitive modem ICs by analyzing published technical specifications can be misleading. No meaningful comparisons can be made, because data sheets provide little useful performance information. Products that appear functionally competitive can vary widely in datacom performance.

Hidden differences in modem architecture can have a profound effect on overall modem operation. Where one modem IC might perform well within a real-world operating environment, another seemingly comparable IC might perform just marginally. So ultimately what the designer needs is a way to realistically compare modem ICs by their ability to perform, error-free, under real-world operating conditions.

The Real World of Telecommunications

Telephone lines vary. In different geographical areas, factors such as age, technology, and upkeep of equipment all contribute to variations in the physical operating environment. The physical mechanics of call-routing introduce other uncertainties, since call-routing can be completely random in a typical dial-up connection due to the automatic routing techniques being used.

Also, differences in the switching and multiplexing methods used in different locations, as well as differences in the conductive medium (copper-wire or fiber-optics), all add to the mix, making it difficult to design a modem that will perform well in a manner that is transparent to all of these factors.

These equipment and routing factors that adversely affect data communications create performance aberrations that are known collectively as line impairments. These line impairments cause the real-world side-effects that define the actual environment in which the modem, and the modem IC, must survive and perform.

Line Impairments

Generally, line impairments can be classified into four categories: line noise, signal-level variations, phase distortion, and carrier offset.

Line Noise

Line noise is the most common impairment to efficient datacommunications and can manifest itself in many ways. Ambient noise, for example, can be caused by copper line conductors. Wideband noise can be generated by hybrid repeater amplifiers in the network. Crosstalk from adjacent lines can sometimes couple into the connection and add to noise on the line.

Generally, noise impairments occur within the 300 to 3000 Hz voiceband, since other frequencies are attenuated by repeaters or filters on the line. The specific quality that enables a modem IC to operate error-free in a noisy line environment can be found in its design architecture, which reflects the functional efficiency of both its components and its circuit layout.

Signal-Level Variations

High signal-level is one impairment in this category. This stronger-than-normal signal can occur when an unusually efficient connection is made, as when routed through a PBX or when the transmitter and receiver are within close proximity to one another. A maximum level for normal operation on a dial-up line might be -10 dBm. An abnormally high level might approach 0 dBm.

Low signal-levels result from high line-resistance or from long, circuitous call-routing paths. The lowest signal level expected on a dial-up line is -45 dBm. The ability of the modem to handle abnormally high or low signal-levels is defined by its dynamic range.

Gain hits are short, quick changes in the receive signal's amplitude. The phenomenon can be caused by trunk-line switching activity or by sudden changes in line impedance, both of which can cause a breakdown in data-transfer integrity. Gain hits can be offset by fast-tracking capability within the AGC circuitry of the modem IC.

Phase Distortion

These impairments include phase jitter, phase hits, and group/envelope delay. Phase jitter is a periodic shift in the phase of the received carrier, which can be caused by variations in the line characteristics or by imperfections in the transmitting modem. Phase hits are more instantaneous in nature. They are characterized by significant changes in phase in the received carrier and are caused by ongoing switching action in the dial-up network. Group delay (envelope delay) results from reactive line-impedance characteristics that induce phase shifts in the frequencies present in the received signal. The modem must correct for group-delay distortion. Failure to do so can result in a phenomenon known as intersymbol interference. This occurs when frequency elements from one signal-modulation period overlap those of another, making it difficult to detect the original phase-encoded information in the signal, thus introducing data errors.

Carrier Offset

This impairment refers to a shift in frequency between the transmitted signal and the received signal. The condition is often introduced during long-distance call routing, where frequency-division multiplexing combines lower-frequency voiceband signals into a higher frequency signal. This phenomenon can be offset by the modem's phase-lock-loop tracking capabilities.

How Modems Can Be Compared For Performance

In order to compare modem ICs realistically, the design engineer needs to test each device under conditions that reflect real-life telephone line conditions. To achieve this, a test environment must be set up to simulate a set of actual line characteristics that conform to specifications defined by Bell System published standards. The engineer can then subject each test modem to artificially induced impairments under each of these line-standard conditions and compare the specific performance of competitive modems. A range of line conditions must be used to show how the modem will operate over the random variety of lines that might be encountered in typical operation.

Line Standards

Characteristics for dial-up telephone lines are not commonly specified, but leased lines are conditioned lines for which linear-distortion characteristics, including frequency-response and envelope-distortion parameters, are guaranteed by the telephone company. The Bell System line standards define four premium line conditions that operate with characteristics similar to those found in dial-up lines. These lines, which allow for modem performance testing over a wide range of representative conditions, include the following:

The 3002 Line is the lowest quality leased line and represents the poorest environment for accurate data communications. Allowable amplitude variation is 15 dB over the voiceband range. Envelope delay can vary as much as 1750 microseconds over the 800 to 2600 Hz range.

The C1 Line is conditioned to a greater extent than the 3002 line and can be considered to represent the average in dial-up line characteristics. Amplitude variation over the frequency band of interest is limited to 8 dB. Allowable envelope delay is the same as for the 3002 line.

The C2 Line represents an intermediate-quality line for modem testing. Frequency response is limited to 8 dB amplitude variation. Envelope delay is improved to not more than 500 microseconds over a 1000 to 2600 Hz range.

The C4 Line represents the best line conditions to be expected in a dial-up telephone environment. Optimum modem performance would be expected using this standard. Group delay or attenuation is negligible. Frequency response is limited to 8 dB. Envelope delay distortion is held to less than 300 microseconds over a 1000 to 2600 Hz range.

The Testing Method

To qualify modem ICs for performance, the test method must be uniformly applied. A test unit is used to simulate each of the Bell System line standards and to generate the environmentally representative line impairments. A typical test set-up includes a line simulator, a personal computer, an RMS voltmeter, and a reference modem to test against. Control of the test parameters is handled by the PC connected to the test fixture through a GPIB data bus. The PC sets up and controls the line simulator, monitors the results, and accumulates the error count for each iteration.

Two modem ICs are compared in a typical test sequence. The modem IC to be tested is connected to the modem testing equipment via a breadboard evaluation fixture and is fed a continuous data stream for testing. The tester monitors the data received from the test modem and the data bit-errors are counted and plotted to signify the ratio between the number of bits transmitted compared to the number of transmission error-bits. This results in a statistical bit-error rate (BER).

The test method calls for a large sample of data errors to be simulated for each device, under each line condition. Multiple data points are taken for each test for each device. Test message data is transmitted in a random, broad-range pattern. Each data point results from the transmission of a million data bits and a complete test sequence on a single modem IC could represent 100 hours of test time before a realistic error sampling might be realized.

The SSI K-Series Modem ICs

Silicon Systems' K-Series family of modem ICs use an integrated analog/digital design philosophy for enhanced high-performance operation, which virtually eliminates data-error-related modem failures. These pin and function-compatible family products comply with the full range of relevant worldwide operating standards for data transfer speeds ranging from 300 to 2400 bit/s. The SSI 73K224L, the industry's first 2400 bit/s single-chip modem for both US and European standards, features adaptive equalization, which further enhances performance by giving the modem the ability to adapt automatically to varying line conditions.

The K-Series modem ICs are used in the sample test curves presented with this document as a base against which competitive performance information can be compared.

MODEM PERFORMANCE CHARACTERISTICS

The curves presented here define modem IC performance under a variety of line conditions while inducing disturbances that are typical of those encountered during data transmission on public service telephone lines. Test data was taken using an AEA Electronics' "Autotest I" modem test set and line simulator, operating under computer control. All tests were run full-duplex, using a Concord Data Systems 224 as the reference modem. A 511 pseudo-random-bit pattern was used with $1X10^6$ bits transmitted for each data point. Noise was C-message weighted and all signal-to-noise (S/N) ratios reflect total power similar to the CCITT V.56 measurement specification. The individual tests are defined as follows.

BER vs.S/N

This test measures the ability of the modem to operate over noisy lines with a minimum of data-transfer errors. Since some noise is generated in the best of dial-up lines, the modem must operate with the lowest S/N ratio possible. Optimum modem performance is indicated by test curves that are closest to the zero axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of operating conditions. Typically, a DPSK modem will exhibit better BER-performance test curves operating in the highband range than in the lowband.

BER vs. Receive Level

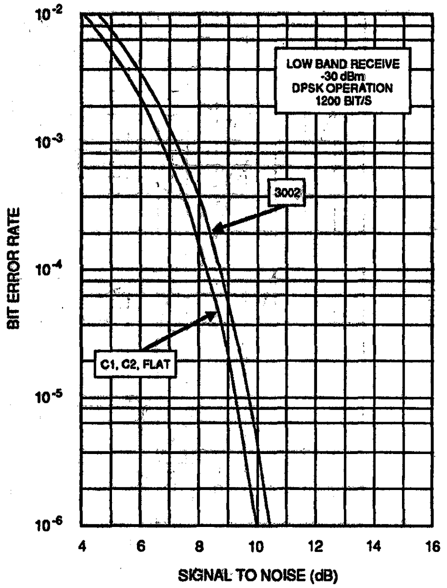
This test measures the dynamic range of the modem. Because signal levels vary widely over dial-up lines, the widest possible dynamic range is desirable. The minimum Bell specification calls for 36 dB of dynamic range. S/N ratios are held constant at the indicated values while the receive level is lowered from a very high to very low signal levels. The width of the "bowl" of these curves, taken at the BER point, is the measure of dynamic range.

BER vs. Phase Jitter

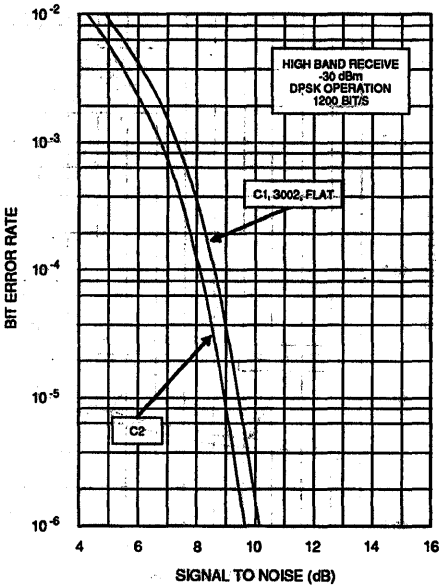
DPSK and QAM modulation is sensitive to phase jitter. Modems using these techniques need to be as tolerant as possible of phase jitter on the line. In this test, relatively flat curves indicate minimal degradation of performance when phase jitter is encountered on the line.

BER vs. Carrier Offset

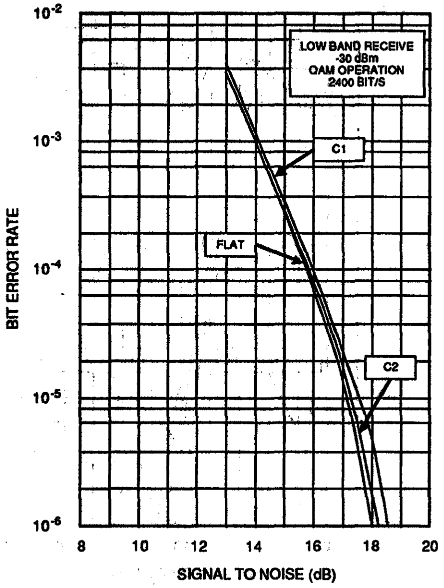
This parameter indicates how the modem's performance is affected by the shifts in carrier frequency encountered in normal public telephone network operation. Flat curves are an indication that there is no performance degradation from frequency offsets. The SSI K-Series modem ICs use a second-order, carrier-tracking phase-lock-loop that is insensitive to carrier offsets in excess of 10 Hz. Both the Bell and European/Japanese CCITT specifications allow as much as 7 Hz offset.



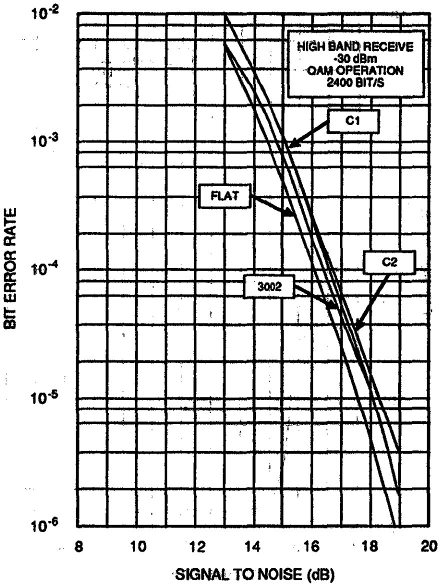
SSI 73K224L
BER vs. Signal to Noise



SSI 73K224L
BER vs. Signal to Noise

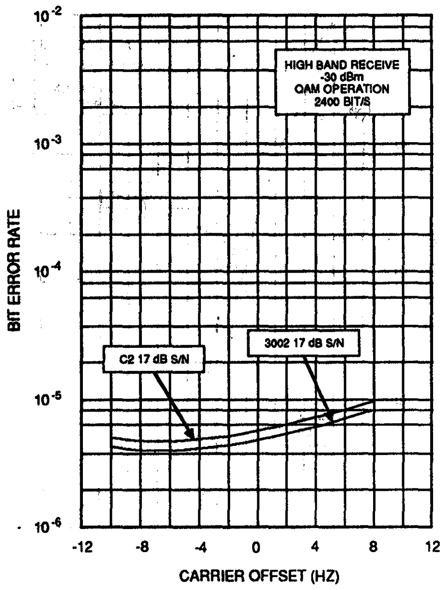


SSI 73K224L
BER vs. QAM-LOW

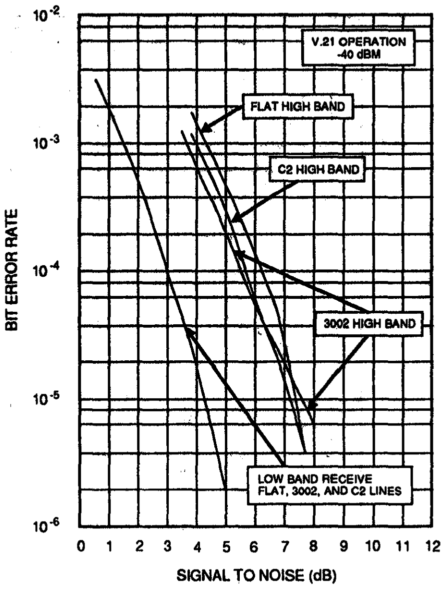


SSI 73K224L
BER vs. QAM-HIGH

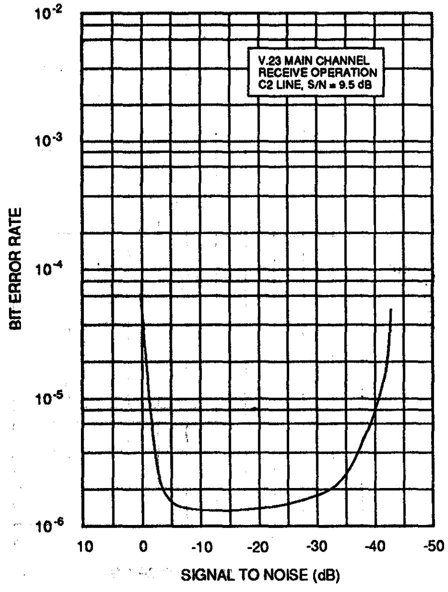
SSI 73K224L BER vs. Carrier Offset



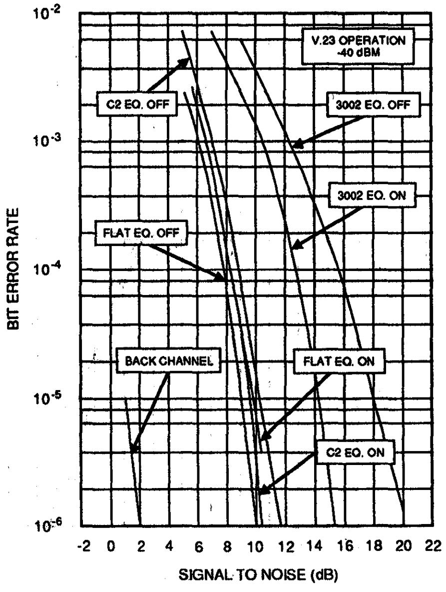
SSI 73K321L, 73K322L BER vs. Signal to Noise



*SSI 73K321L, 73K322L BER vs. Receive Level (V.23 only)



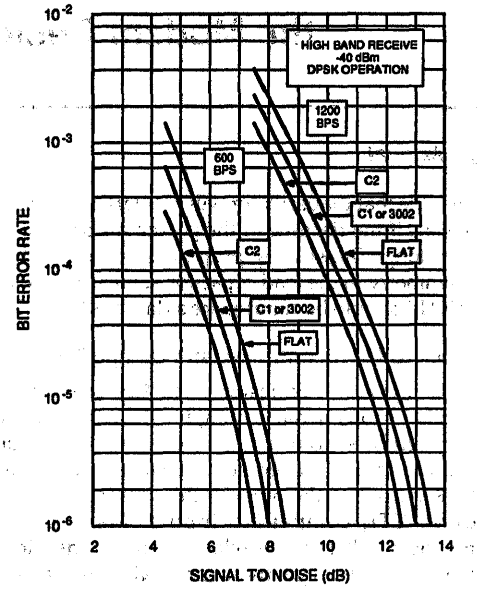
*SSI 73K321L, 73K322L BER vs. S/N (V.23 only)**



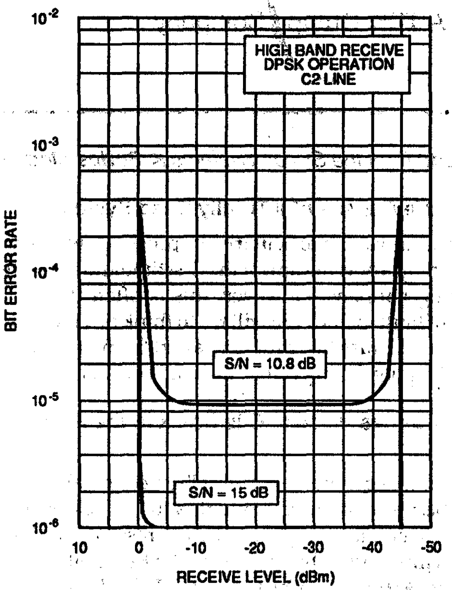
* = "EQ On" indicates bit CR1 D4 is set for additional phase equalization.

** = 73K302L performance is similar to that of the 73K322L. V.23 operation corresponds to Bell 202.

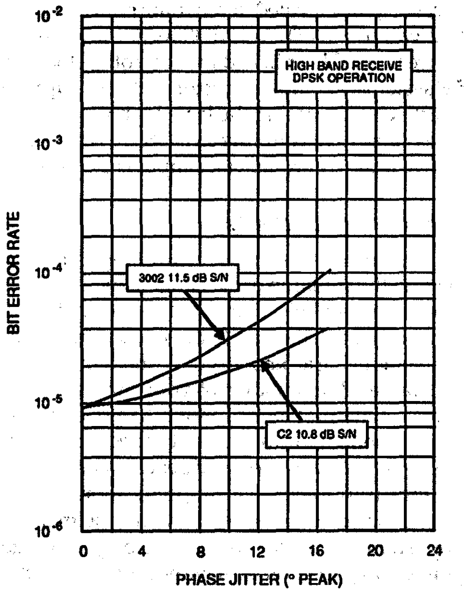
***SSI 73K322L**
BER vs. Signal to Noise



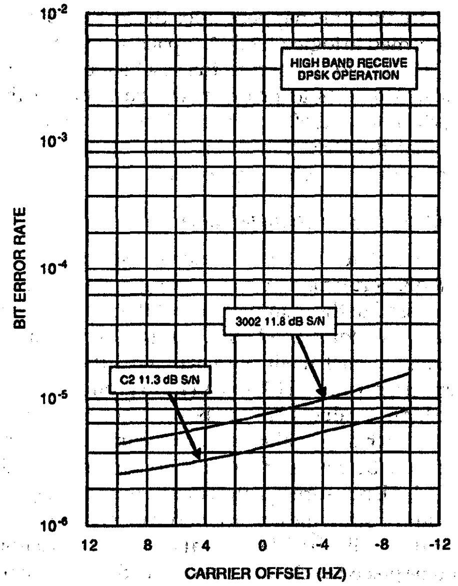
***SSI 73K322L**
BER vs. Receive Level



***SSI 73K322L**
BER vs. Phase Jitter



***SSI 73K322L**
BER vs. Carrier Offset



* = "EQ On" Indicates bit CR1 D4 is set for additional phase equalization.

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APPLICATION NOTE

Troubleshooting the Modem Design

Excerpt from the Silicon Systems K-Series Modem Design Manual

Possible Causes of a Totally Dead System

It is always particularly depressing when you power–up a new design for the first time and absolutely nothing happens. However, this is often the easiest type of fault to find. We will try to think of a few things that could cause this problem (apart from the obvious, like the plug falling out of the wall socket).

The K-Series Modem IC is Stuck in the Reset State

You will generally get very little cooperation from a K–Series modem IC while it is in the power-down state. It enters this state when a reset operation is performed, either by writing to the Reset bit (bit 2) in Control Register 1 or by taking the RESET input pin to logic ONE. Make sure that your firmware is bringing the part out of this state by writing something other than all ZEROs to bits 5 to 2 in Control Register 0. Also, make sure that this happens after the RESET pin has been returned to logic ZERO. A capacitor from this pin to VDD can hold the part in the reset state for many seconds. Attempts to program the part during this time will not take effect. For products with a DSP, check that the RESET DSP bit (CR2 bit D2) is also written with ONE when appropriate.

Crystal Oscillator Fails to Start

If a complete crystal oscillator is used to directly drive the K-Series modem, any starting problem should be addressed to the manufacturer of that device. If the internal oscillator is used with a crystal, there may be situations in which it will not start. Check the values of the capacitors from XTL1 and XTL2 to ground. If these are too high in value, 40 pF or above, the oscillator may not start. Such large values are not recommended and should not be necessary if the crystal is correctly specified. Also ensure that the circuit board is designed to minimize stray inductance and capacitance in the area of the oscillator. The crystal and both capacitors should be placed as close as possible to the XTL pins of the K-Series modem IC and connected by direct traces. The ground connection of the capacitors should be via wide traces to the digital grounding system. It is also possible that the oscillator will not start or will be slow to start if the risetime of the power supply voltage is very long. The starting properties are helped by the asymmetry in the load capacitor values, the capacitor at XTL1 should be about twice as large as that at XTL2.

Clock to Microcontroller Isn't Getting Through

Using the K-Series modem ICs on-chip clock oscillator to generate timing for the entire system is very efficient from the point of view of component count and EMI generation. However, note that the CLK output of the modem chip is specified only to drive TTL compatible inputs. Many common microcontrollers require clock inputs that rise closer to the supply voltage for logic ONE. We have seen applications which use the CLK pin to drive these inputs without problem, however, the low-power (5V supply) parts may give a lower logic ONE level than is necessary at elevated temperature. We recommend that you use a TTL to CMOS level converting buffer between the CLK pin and the controller clock input in 5V systems. A pull-up resistor to the 5V supply is not effective in increasing the logic high voltage. In some cases capacitive coupling to a CMOS input is also effective if the controller clock input is properly biased.

Connect Handshake Fails

If your system seems to be working well but cannot get into the situation of exchanging data with another modem, it is likely that you have a problem in the connect handshake. It is better to examine handshake problems using a "known good" modem at the remote end rather than another of your own systems. This helps isolate problems if more than one are present. Use a modem from an established and reputable manufacturer, as discounted generic modems may not conform fully to established specifications. Depending on the modulation mode, there may be many or few opportunities to fail so we can only offer general pointers to problems we have encountered in the past. It is very helpful to build extra diagnostic code into the handshake to diagnose unexpected conditions.

If things never start, check that the initial set-up of the chip is correct. The chip must be taken out of power-down before it will do anything and in DSP-based chips the DSP must have been reset after any previous call and then taken out of the reset state. (A DSP–based part cannot be used in a non-DSP socket without many such changes to the controller code; watch this when upgrading a 73K222 system to use a 73K224L.) If in CALLINIT mode the answer tone is not detected, check that you have selected the desired answer tone frequency by programming in the Tone Register. The selectivity of the answer tone detector is quite high, so verify that your answering modem is generating a frequency within the specifications of the modulation standard. You should be able to verify the operation of your various signal detectors with breakpoints in the controller code. If these do not fire at the appropriate point, the handshake is likely to hang-up or get out of step with the other modem. Be especially careful with the S1 detector, if this is failing you may get connections at 1200 bit/s which were supposed to be at 2400 bit/s. With DSP-based chips in QAM or DPSK modes, make sure that you are enabling the adaptive equalizer at the appropriate time. Enabling it too early, when the received signal is unsuitable for training, and too late, when there is too little time left before the gearshift to 2400 bit/s, can both give connect problems. Finally, make sure the crystal oscillator frequency is in specification as a gross error here can cause failure of the handshake.

Errors Committed Immediately After Handshake, With Later Improvement

We have seen situations in which a K-Series modem makes many data errors during the first few seconds of a connection, but then shapes up and performs normally thereafter. This is generally due to some problem in equalizer training in a DSP-based chip. The equalizer must be held in the initial state (bit 0 of CR2 = ZERO) up to the point in the handshake when scrambled DPSK binary ONES first appear at the receiver. It must then be released promptly (bit 0 of CR2 = ONE) and allowed to adapt so that it is fully trained before the gear shift to 2400 bit/s and the transition to data mode occurs. Enabling the equalizer too early will cause it to train on an unsuitable unscrambled signal. Because it adapts more rapidly immediately after being enabled, it may take a long time to recover from a bad solution when the correct receiver signal arrives. Enabling the equalizer too late reduces the time available for training before the received data is relied upon to be correct. If you have to put the equalizer back into the initialized state after a period of training, make sure that Equalizer Enable (bit 0 of CR2) stays at ZERO for at least 2 ms. It is better to have the Receiver Gain Boost bit dealt with before the equalizer is enabled, otherwise transients caused by changing this bit may upset the equalizer solution.

Errors Experienced at High Receive Signal Levels

If the error rate gets worse at high receive signal levels, you should look for some source of clipping in the receive path. Injecting a signal of known level at the line coupling transformer and looking at the RXA pin with an oscilloscope should enable you to isolate any problem in the line interface. Look for excessive gain in the receiver buffer amplifier or other causes of clipping at this point such as badly chosen op-amps for single 5V supply operation. If the signal at RXA looks good and you are using a DSP-based modem chip, it is possible that the controller is incorrectly inserting the 12 dB receiver gain boost even if the Receive Level bit in the Detect Register is set. Note that early data sheets for the 73K224L gave this bit the wrong sense, i.e., ONE for low level. Only set Receive Gain Boost if this bit is ZERO.

Errors Experienced at Low Receive Signal Levels

There can be many causes of data errors at low receive signal levels, almost all associated with the presence of some level of interference or noise in the receive path. If you are performing tests over the telephone network, make sure that the error rate you are experiencing is not to be expected from the background noise level on the line. It is best to use a line simulator or a direct connection through an attenuator if looking for system noise problems. The capacitor across the feedback resistor of the receiver buffer amplifier is important to attenuate out-of-band noise at the modem chip receiver input.

Distortion in the telephone line interface can be located by injecting low-level signals into the line terminals and examining the signal at the RXA pin with a spectrum analyzer. Look for crossover distortion in the receiver buffer amplifier. This can arise from a poorly chosen op–amp type, such as the LM324 which makes a transition from class A to class AB operation at low signal levels and is not suitable for this application. We have found LM348 and LM1458-type op-amps to be free from this problem. It is also possible for the line coupling transformer to introduce harmonic distortion, particularly when a large D.C. holding current is flowing.

In the absence of significant distortion, look for a high noise level at the RXA pin. Another symptom of this problem, apart from data errors, is that the Carrier Detect bit (bit 3 in DR) comes on or blinks when no signal is applied to the modem receiver. The system may also fail to disconnect at the end of a call. If this is your experience don't confine your search to the normal carrier bandwidth because the modem chip will also be susceptible to higher frequencies. Op-amps may be noisy or may self-oscillate at low level due to poor layout. If the op-amps themselves are not causing the noise, it may be due to poor circuit layout or grounding. If, finally, nothing suspicious is visible at the RXA pin then the noise must be getting into the receive signal inside the modem IC. This can be from the power supply and bias pins or from signals routed under the chip. Check the connections to GND, VDD, VREF and ISET pins for component values and placement and routing of decoupling components. You are more likely to have problems with supply noise if you are using a switching power supply. Look also for fast digital signals routed under the modem IC; these should be re-routed and a ground plane placed under the chip. Serious interference pickup problems can be created by two crystal oscillators producing beat frequencies in-band to the modem. We strongly recommend using one master crystal in the system. Check the gain in the receive path from the line terminals and, in DSP-based parts, the state of the Receive Gain Boost bit set by the controller. If either of these are incorrect, then noise in the chip will appear more significant compared to the signal.

The transmitter of the modem can be a source of noise in the receiver. It should not generate signals that are in–band to the receiver, but this can happen if either the buffer amplifier or the line transformer are causing harmonic distortion. This will be most noticeable in call mode, when the low band transmit signal has harmonics in the high band filter of the receiver. For 5V only systems, the choice of op-amps in the buffer amplifier and their D.C. bias point is crucial to obtaining a sufficient voltage swing without distortion. Because of its internal operation, a small amount of switching noise is present at the TXA pin. The capacitor across the buffer amplifier feedback resistor is important to prevent this signal from reaching the receiver. It is difficult to obtain good rejection of the transmit signal at the receiver for all practical line conditions, but you should check that your four-wire to two-wire hybrid circuit is operating correctly. For most terminations, the transmit signal at the RXA pin minus the receive buffer gain should be 6 dB below the level at the line.

Modem Works in Loopback but Fails to Connect or Makes Errors in Bursts with Some Other Modems

If anything appears "flaky" about the modem operation it is a good idea to check the oscillator frequency with a counter capable of resolving to at least ten parts per million. Using an oscilloscope is of no use whatsoever. Many systems that use crystal oscillators are not very particular about the exact frequency; this is not so of modems. Measure the frequency at the CLK pin and verify that it is between 11.0581 MHz and 11.0603 MHz. Do not measure at the XTL1 or XTL2 pins as the probe capacitance will alter the frequency of oscillation. Some causes of out–of–specification readings are: a) the wrong crystal frequency entirely, b) a series-resonant crystal, or c) a parallel-resonant crystal unmatched to the circuit capacitance.

Problems Unique to FSK Modes

The SSI 73K224L does not permit answer tone detection in FSK modes, so ensure that a mode other than FSK is selected before attempting to detect answer tones.

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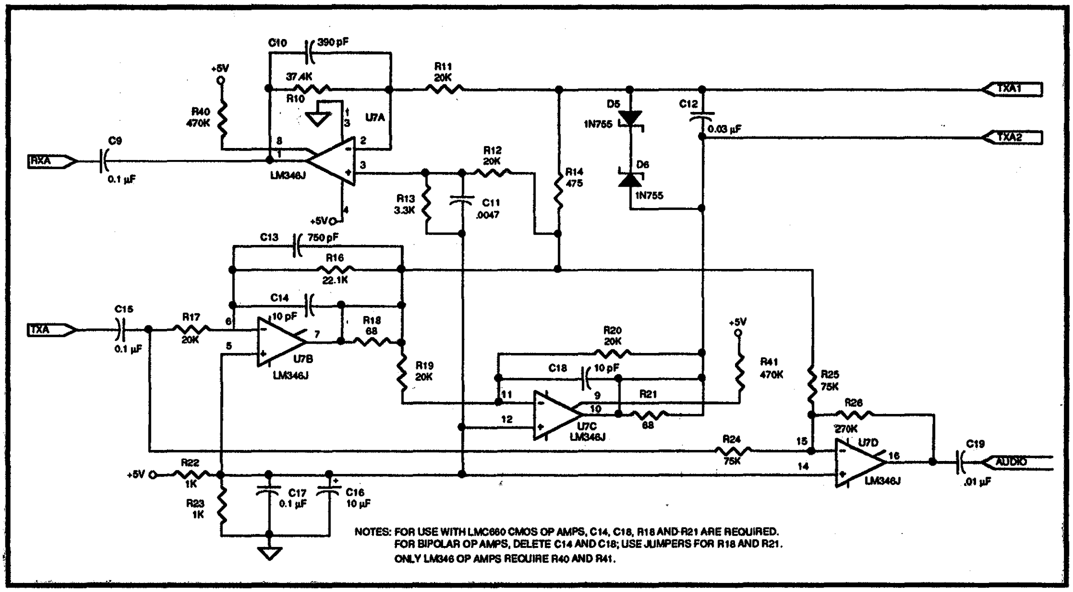
SSI 73M376
Integrated Line Interface

APPLICATION NOTE

In the past there have been numerous inquiries asking if we had an interface IC for the telephone side of our K-series modems. Until this time we have had to say no, but with a few opamps, a couple of transistors, a speaker driver, and a "few" other components you can build your own. Now there is a single device that is designed to be used for the line interface with our K-series modem ICs and performs a number of functions that are needed in most modem applications. It also significantly reduces the number of components required for the DAA circuitry. The 73M376 performs the hybrid function, has a speaker driver with volume control, and two relay drivers for the hook switch control. In addition there are two separate transmit paths available, a power down mode, and the relay drivers may be programed to reduce the power to the relay holding coils. This note will acquaint you with the advantages this part brings to modem designs.

One of the problems with traditional opamp hybrid designs is that there are few low cost opamps that will meet the requirements of operating from a single 5 volt power supply and also drive the required load. We have in the past recommended several standard opamps for this function, but have always had to qualify that recommendation because of the need for extra components or opamp spec limitations. In the past we have recommended the LMC660, although it required two additional resistors and capacitors; the LM348 which is not rated in the National Semiconductor data book for single 5 volt operation; and the LM346 which also requires two additional resistors. Now we can without reservation recommend our own 73M376.



NOTES: FOR USE WITH LMC660 CMOS OP AMPS, C14, C18, R18 AND R21 ARE REQUIRED.
FOR BIPOLAR OP AMPS, DELETE C14 AND C18; USE JUMPERS FOR R18 AND R21.
ONLY LM346 OP AMPS REQUIRE R40 AND R41.

FIGURE 1: Typical Opamp Hybrid Circuit

Figure 1 shows a typical opamp based hybrid design. This is the same design used in the 2402DEK demonstration board for the 73K224L. Provision was made for different opamps to be used although the board is normally supplied with the National Semiconductor LMC660 opamp. TXA and RXA connect directly to the K-series device. TXA1 and TXA2 connect to the telephone isolation transformer. AUDIO outputs the mixed transmitted and received signals so both may be heard.

Figure 2 shows the telephone interface for the 2402DEK. The schematic shows three transistors for three relays, but in most applications only one or two are used. A SPDT relay could be used for the hook switch (K1) and cut off (K2) relay functions. The telephone interface for our purposes also includes the "audio interface" since many applications require a loudspeaker to monitor the progress of a call. This must also include provisions for volume control and squelch when audio is not desired. The 4052 multiplexer is used for these purposes. The LM386N is used to drive a low impedance loudspeaker.

Figure 3 shows the equivalent circuit using the 73M376 Integrated Line Interface IC. The difference in parts count is apparent although the function is identical. The difference in board space between the two designs can be significant for small footprint internal laptop or notebook designs where real estate is at a premium.

The timing for power reduction mode for the relay drivers is controlled by the .01µF capacitor C17 connected to HTIMER. This determines the time full relay voltage is applied to the holding coil before going into low power hold state. HTIMER may alternately be driven by a TTL signal. The holding coil voltage is as much as 24% less than the normal applied voltage. If the power saving feature is not needed and you do not want to use the additional capacitor, the HTIMER pin may be grounded. Note also that the $\overline{\text{PWR}}$ pin connects to the $\overline{\text{HOOK}}$ so whenever the modem is on hook the 73M376 will be in power down mode. These are features that are significant where minimum power dissipation is an important factor.

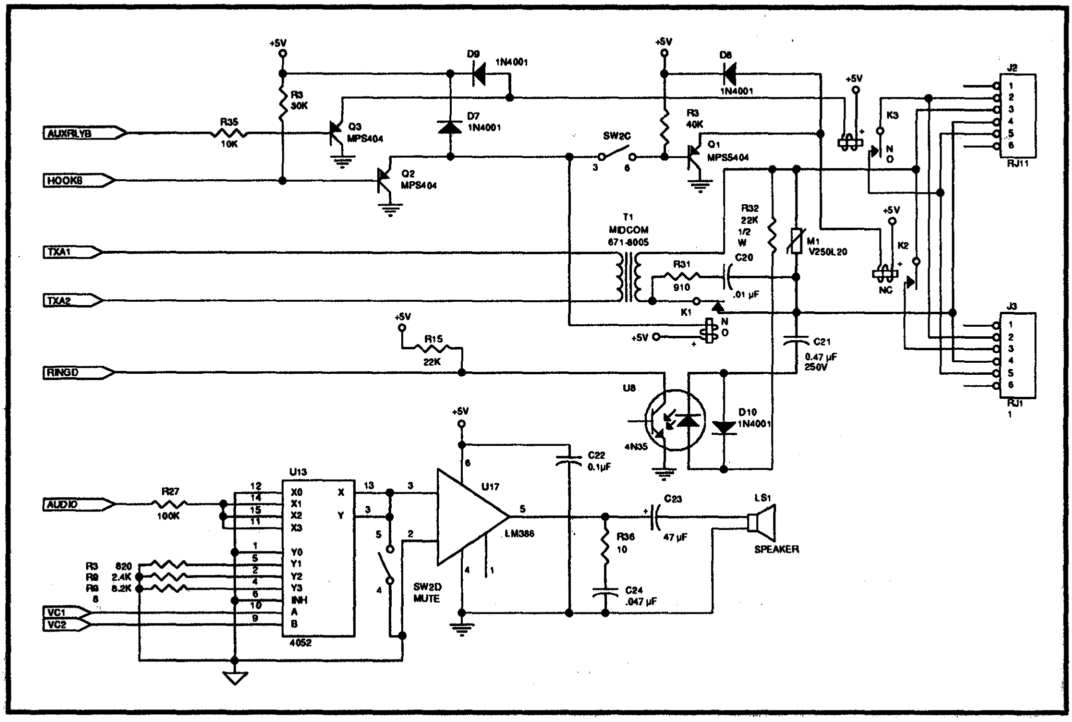


FIGURE 2: Telephone Interface Circuit

The 73M376 opamps are wideband high performance devices that need to be dealt with as with any similar opamp. The receive opamp stability is dependant on the input capacitance and the feed back resistance. The minimum feedback resistance should be 5KΩ, and the resistor used should be kept near that value. This prevents the high frequency gain from causing oscillation due to parasitic capacitance on the RCV pin. The RCV pin capacitance must be kept to a minimum. Socketing the 73M376 is not recommended since this tends to increase the parasitic capacitance. The output impedance of the receive amplifier is somewhat high, so addition of feedback capacitance to reduce high frequency gain in the amplifier will not be effective in this case. In cases where the input capacitance cannot be effectively controlled, a resistor from the RCV pin to the BIASC pin will reduce the loop gain and stabilize the amplifier but not affect the closed loop gain. This resistor value will range from 2K to 5K depending on the parasitic capacitance being encountered.

One feature of the 73M376 that is overlooked in this application is the alternate transmit path. This second path can be used to transmit the same signal at another level or a different signal such as FAX may be brought in and the gain set separately. TXAP and TXAOUTP are the input and output respectively of the second transmit path. This transmit path is electrically identical to TXA and TXAOUT and is selected when the MUX pin is low. Remember there is an additional 12 dB (nominal) gain after this gain setting stage for both transmit amplifiers. This means for a K-series part the actual gain set by the external resistors will be less than one.

The difference in the parts count between a discrete design and a 73M376 based design are significant. The active components are reduced from 5 devices to one; the passives from 30 devices to 12 for an equivalent function. Fewer components mean lower assembly cost and rework, and higher reliability. The savings in component cost can also be compelling in large volume, price sensitive products. The component savings can be from $.30 to $1.00 depending on the cost model used.

The 73M376 should be considered in all designs, but for today's ever shrinking computers there are even more compelling reasons the 73M376 should be used. There is a better way to build a telephone line interface now that the 73M376 is available.

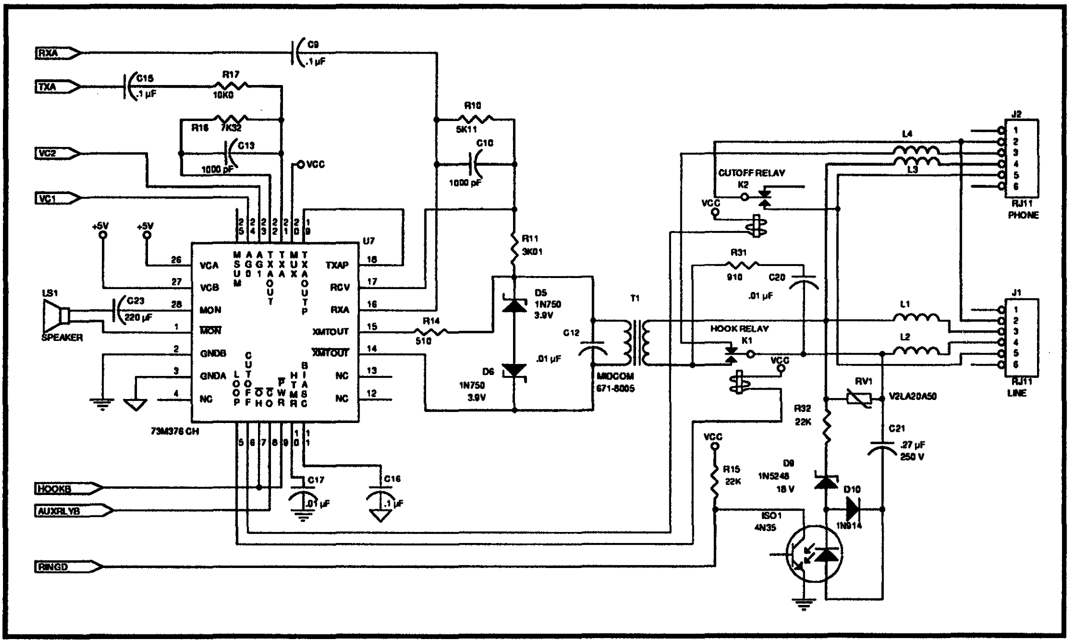


FIGURE 3: 73M376-based DAA Circuit

Notes:

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SSI 78P236/2361/2362/7200
Demo Board

APPLICATION NOTE

December 1992

DESCRIPTION

The 78P236 demo board is a PC board designed to facilitate the evaluation of the SSI 78P236 series of single chip transceiver ICs. The demo board can be used to test different transceiver ICs by changing various components. The demo board includes all of the necessary discrete components for the interface to a coded AMI line. A DIP switch allows easy control of the option pins on the IC. A loopback function is easily implemented using a slide switch. The same switch allows either an encoded signal (TPOS, TNEG, TCLK) or composite signal (TDATA, TCLK) be input to the transmitter. Simple test patterns can be injected into the data stream. Several jumpers allow the change of the transmitter and receiver clock polarity.

FEATURES

- **Allows easy evaluation of AMI transceiver ICs**
- **Includes all necessary external components**
- **Includes a digital loopback mechanical switch**
- **Generates ALL ONEs and repeated ONE/ZERO patterns**
- **Accepts composite Clock/Data and converts them to AMI pulses (No B3ZS encoding)**
- **Allows the use of either the receive clock or an external clock as the transmitter clock**
- **20-pin edge connector accepts flat coax cables and provides logical signals**

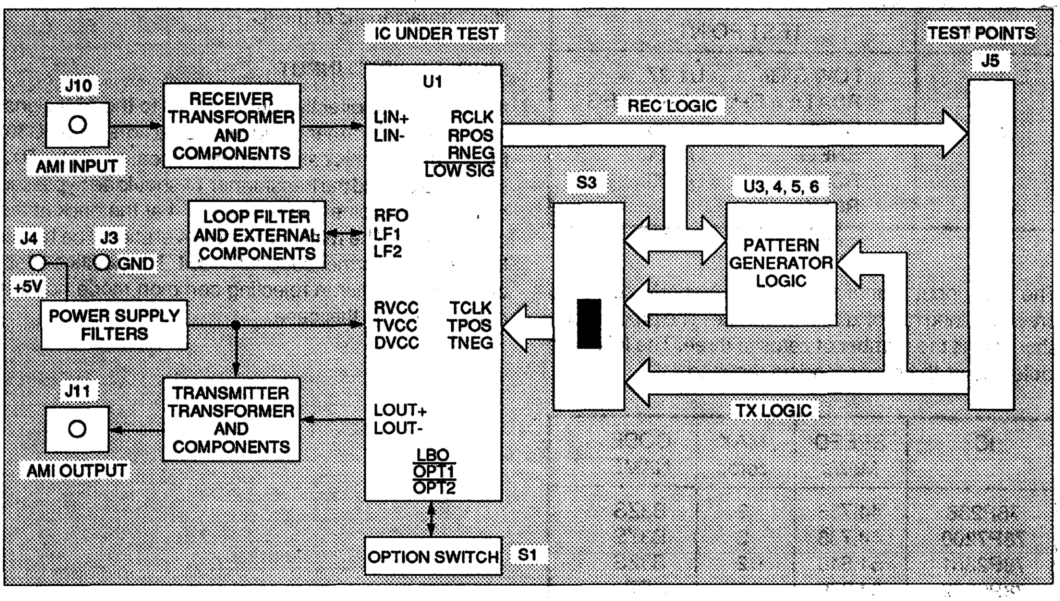

FIGURE 1: Demo Board Block Diagram

POWER SUPPLY CONNECTION

The demo board is constructed as a four layer PC board. The outer two layers carry the signals. The internal two layers are the segmented ground and power supply planes. Three segments separate the receive, transmit and logical ground and supply planes. The three ground planes are connected together using PC board traces at JP2 and JP8 positions. These traces can be cut to isolate the three planes from each other. The power supply planes are connected to a single +5V banana jack (J4) using LC filters of 4.7 µH and 0.1 µF. When a separate digital +5V supply is available, L1 is removed and the DVCC supply can be connected to J2.

RECEIVE SIGNAL PATH

The AMI signal is connected to the BNC connector J10. The maximum recommended distance of the demo board to a DSX crosspoint is 450 feet. The IC can handle added resistive attenuation as referenced by its minimum input signal level specification. The IC recovers clock, positive and negative data from the AMI signal. The following table shows the available receiver logical signals on the test points and edge connector J5:

J5 PIN	TEST POINT	
1	LOW SIG/	U1-27
3	RDATA = RPOS .OR. RNEG	
5	RPOS	U1-25
7	RNEG	U1-24
9	RCLK	U1-23
11	RCLK/	

The AMI input signal should be properly coded to prevent a long run of zeros on the line. The proper code should limit the number of zeros to three. The following table shows the proper coding required:

IC	SPEED Mbit/s	MAX zeros	CODE NAME
78P236	44.736	2	B3ZS
78P7200	44.736	2	B3ZS
78P2361	51.840	2	B3ZS
78P2362	34.368	3	HDB3

The demo board may be loaded with components which form a discrete equalizer for very long cables (R11, R12, R13, C31, L10). The AMI input signal to the IC can be monitored using a high impedance FET probe (TEKTRONIX P4064 or HP 1141A) connected to the TP14, TP15 pair.

The input signal is coupled through a 1:1 wideband transformer. The following table shows some of the suggested manufacturers of this part:

MANUFACTURER	PART NO.
Pulse Engineering	PE-65663
Coilcraft	WB2010-PC

The AMI line is terminated at 75 ohms using R10.

Table 1 shows the required external components for different ICs used for receiving AMI signals at different speeds. Resistor R2 sets the center frequency of the oscillator. Capacitor C6 is used to bypass any noise on R2. Resistors R3,R20 and capacitor C26 controls the jitter characteristic of the IC.

SINGLE ENDED INPUT

It is possible to directly couple the IC to the AMI signal without a transformer using two capacitors (C29, C30) for isolation. In this case jumpers in locations R11, R12 should be cut and the transformer T1 should be bypassed by connecting pins 1 to 6 and 3 to 4 at the back of the demo board. The minimum input level should be higher than the transformer coupled circuit. The positive effect of the transformer in rejecting common mode noise is not achieved in this case.

TRANSMIT SIGNAL PATH

The IC accepts CMOS level NRZ logical inputs (TCLK,TPOS,TNEG) and converts them to the proper AMI signal. As shown in Table 2, the three position switch S3 and jumpers JP1,5,6 allow selection of different sources for these logical signals. In its simplest case, placing S3 in the bottom position allows a digital loopback. The following table shows the test points and J5 edge connector pins used for the transmitter.

J5 PIN	TEST POINT	
15	TCLK	clock input
17	TNEG	negative data
19	TPOS	positive data
19	TDATA	composite data

The outputs of the IC, LOUT+ and LOUT-, are connected to a 1:1:1 wideband transformer. The following table shows some of the suggested transmitter transformers:

MANUFACTURER	PART NO.
Pulse Engineering	PE-65664
Minicircuit	T4-1

The transformer center tap is connected to the +5V supply through a filter comprised of a 4.7 µH inductor and a 0.1µF capacitor. The capacitor C27, when added to the PC board trace and the transformer input capacitances, will effect the pulse shape. This capacitor should be selected for individual PC boards. The objective is to meet a pulse template at any cable length up to a maximum of 450 feet. The generated AMI signal is available on the BNC connector, J11, and it can be monitored on TP12, TP13 pair using a high impedance probe.

OPTION PINS CONTROL

Switch S1 changes the logic level of the option pins on the IC which controls the transmitter. Table 3 shows the function of this switch.

PERFORMING TESTS WITH DEMO BOARD

The general test setup using the demo board is shown in Figure 2. When the switch S3 is placed in its bottom position (loopback), the receiver logical output signals (RCLK, RPOS, RNEG) from the IC are connected to the transmitter logical input (TCLK, TPOS, TNEG). As a result, the received AMI signal is transmitted back to the test equipment. Bit error rate testing will indicate the ability of the IC to receive and transmit the AMI signal with no errors.

As shown in Figure 2, 450 feet of 75 ohm coaxial cable (type RG59B) and resistive attenuation is inserted in the receive path to exercise the IC for its lowest input level. The following tests are performed on the receiver:

BIT ERROR RATE TEST

A pseudo-random pattern is generated by the test equipment. This pattern is created using a shift register of N bits. Preventing an all zero pattern, a combination of 2**N-1 patterns of N bits is created in a random manner. This pattern is used to simulate the live traffic on the AMI line. The following table shows the mostly used patterns to test the IC:

IC	RANDOM PATTERN	FIXED PATTERN
78P236	2**15-1	100100...
78P7200	2**15-1	100100...
78P2361	2**15-1	100100...
78P2362	2**23-1	10001000

When running these patterns, no bit errors are expected in the absence of any noise. The test is repeated for fixed patterns to exercise the IC for any pattern sensitivity.

JITTER TOLERANCE

Telecommunication equipments should be able to recover clock and correct data even if the AMI signal includes a reasonable amount of timing jitter. For this test, the test equipment adds jitter to the random AMI signal. For jitter at a set frequency, the amplitude of the jitter is slowly increased until bit errors are observed. This process is repeated at different frequencies and a plot of the maximum tolerated jitter vs the jitter frequency is made as shown in Figure 3. The IC should tolerate jitter in excess of specified requirements.

INTRINSIC JITTER

The jitter generated by the IC in the absence of any jitter on its transmitter logical input (TCLK, TPOS TNEG), should be minimal.

JITTER TRANSFER FUNCTION

The IC should not cause any amplification of the system jitter, i.e., no peaking should be observed in the jitter transfer function. This objective is achieved by selecting the PLL filter components for an overdamped response. The test equipment adds jitter to the AMI signal received by the IC. Measuring the jitter transmitted by the IC in the digital loopback mode indicates the shape of the transfer function. As shown in Figure 4, the IC adds no peaking and higher frequency jitter is attenuated.

TRANSMITTER TESTS

The AMI pulse generated by the IC can be tested for its shape, amplitude and frequency content over different lengths of cable. The demo board is usually placed in the loopback mode (S3 in bottom position).

PULSE FREQUENCY CONTENTS

For an AMI signal with an all ones pattern, the transmitted signal should have a frequency spectrum with the main component at half of the bit rate. The signal power at the harmonics including the component at the bit rate should be at least 20 dB lower than the main component. A spectrum analyzer is used for this purpose.

PULSE AMPLITUDE

The pulse amplitude for a pattern of 100100... is measured at different cable lengths by connecting the end of the cable to the scope using a 75 ohm termination adaptor (POMONA 4119). Except for the 78P2362, whose transmitted pulse amplitude is needed to be fairly exact (2 Vp-p ± 5%), other IC's transmit amplitude may fall in a wide range of amplitudes from 0.72 to 1.7 Vp-p.

PULSE TEMPLATE

The shape of the signal is examined by comparing it to the published templates. The test setup is shown in Figure 2. The program resident in the computer reads the transmitter waveform from the scope, scales it vertically, and plots it together with the published template masks. The pulse shape should meet the mask for all cable lengths from zero to 450 feet. The LBO pin as controlled by switch S1-1 should be properly set. For cable length of less than 225 feet this switch is open and for longer cables this switch should be closed. A typical pulse shapes for the 78P236 at the end of 450 feet of cable is shown in Figure 5.

PULSE IMBALANCE

The AMI pulse generated by the IC includes pulses of both negative and positive polarities. The pulse imbalance is examined by inverting the negative pulse using the scope and overlaying it on a typical positive pulse. No significant imbalance is observed.

TABLE 1: External Components List for Different ICs

Data sheet ref. ->		RFO	RLF1	RLF2	CLF1	RTR	RTT	CTT
Demo board ref. ->		R2	R3	R20	C26	R10	R6	C2
Unit ->		kΩ	kΩ	kΩ	µF	Ω	Ω	pF
78P236	44.736	5.23	20	100	0.22	75	None	10
78P7200	44.736	5.23	6.04	100	0.22	75	301	10
78P2361	51.840	4.64	20	100	0.22	75	None	10
78P2362	34.368	6.81	20	100	0.22	75	None	10

TABLE 2: Sources of the Transmitter Logical Signals

Switch	Source of: TPOS/TNEG		Source of: TCLK		Polarity of: TCLK	
S3			JP5 2-1	JP5 2-3	JP1 2-1	JP1 2-3
Top	External		RCLK	EXT	Buffered	Inverted
Middle	JP6 2-1	Converted from TDATA	RCLK	EXT	Buffered	Inverted
	JP6 2-3	Internally generated	RCLK	EXT	Buffered	Inverted
Bottom	RPOS / RNEG		RCLK	RCLK	RCLK	RCLK

TABLE 3: Function of the DIP Switch S1

Position	IC Pin	Function	Open	Closed
S1-1	LBO	TX cable length	L < 225'	L > 225'
S1-2	$\overline{\text{OPT1}}$	TX amplitude	Normal	Boost 2.7 dB
S1-3	$\overline{\text{OPT2}}$	TX disable	Enable	Disable
S1-4	None	test pattern' JP6 2-3, S3 Mid.	1010 ...	111 ...

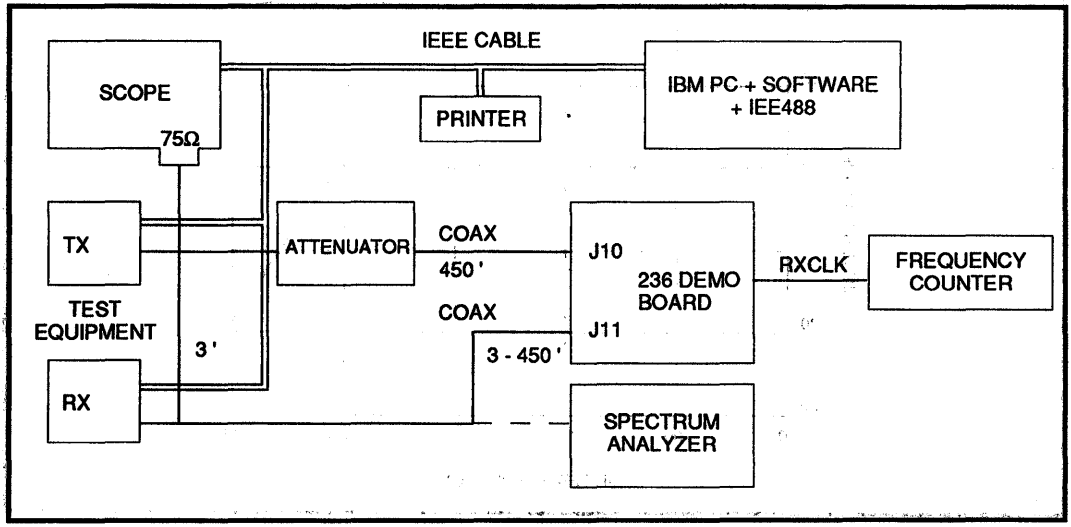

FIGURE 2: General Test Setup

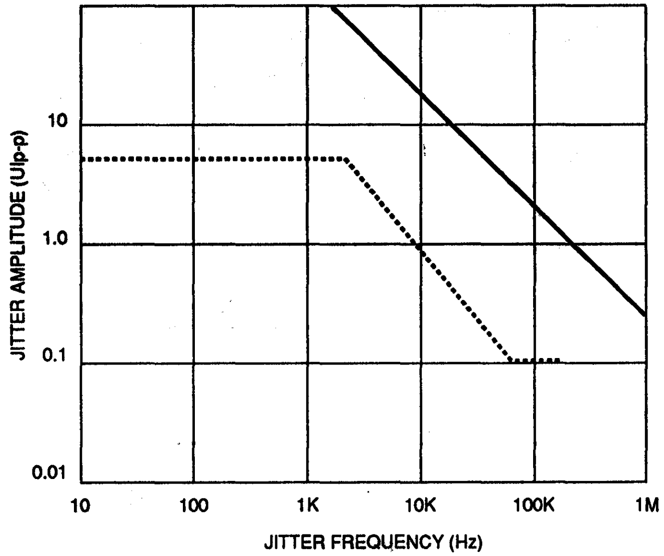

FIGURE 3: Jitter Tolerance for 78P236

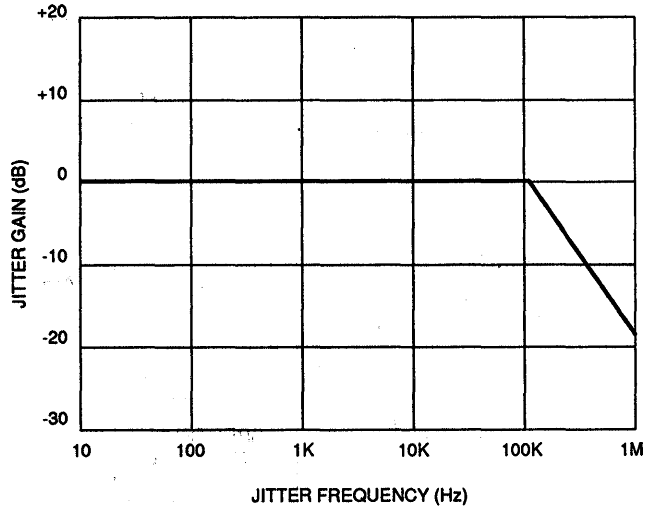

FIGURE 4: 78P236 Jitter Transfer Function
Loop Filter BW = 165 kHz

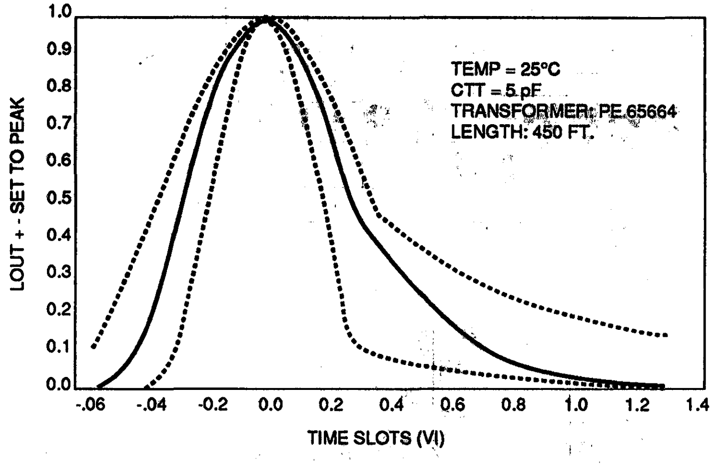

FIGURE 5: Transmitter Pulse Shape for 78P236

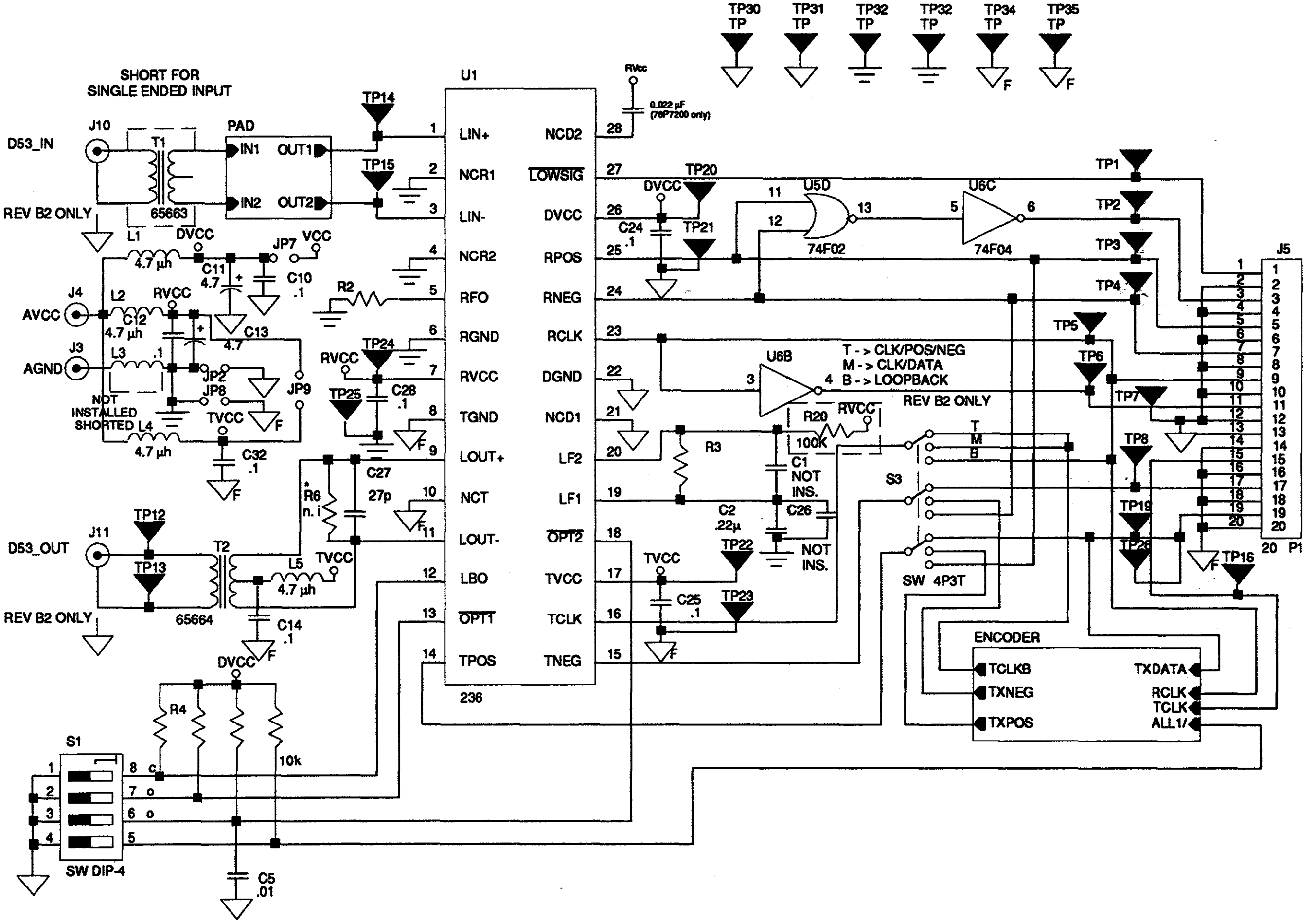

FIGURE 6: Demo Board Schematics

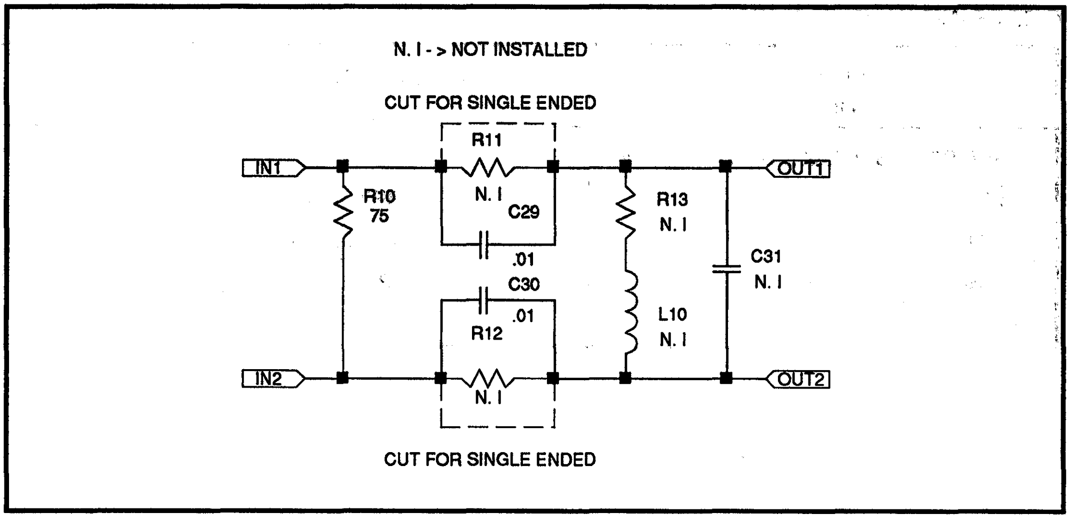

FIGURE 7: Pad / Equalizer

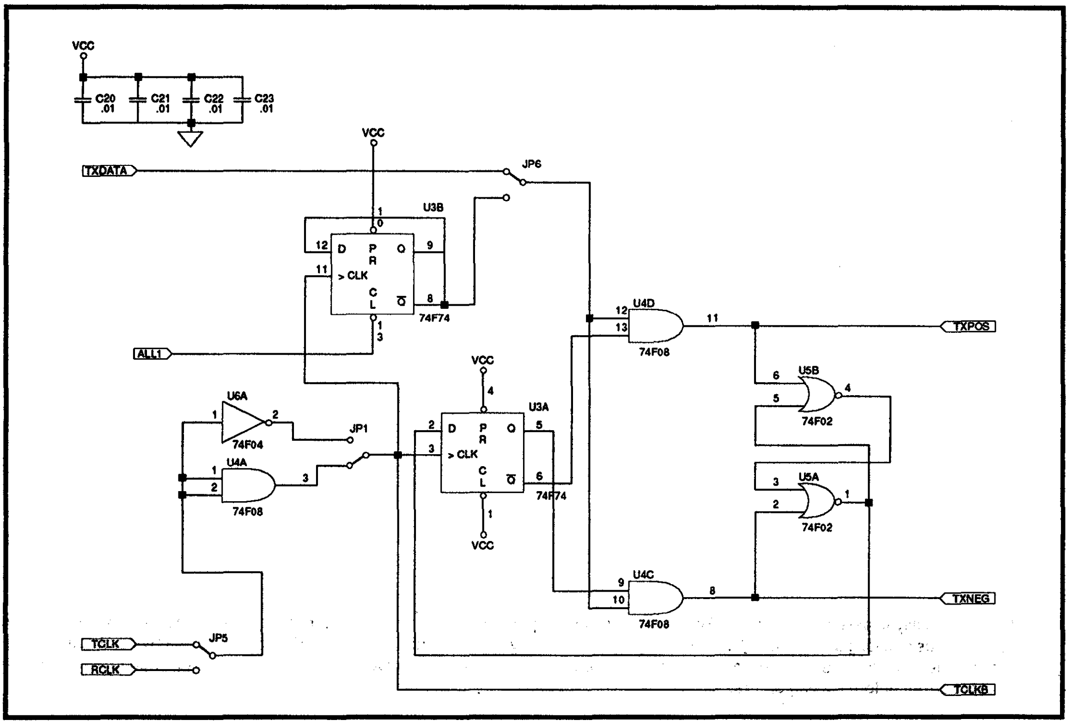

FIGURE 8: Encoder

SSI 78P236/2361/2362/7200
Demo Board

ORDERING INFORMATION

AMI SPEED Mbit/s		DEMO BOARD PART NUMBER
SSI 78P236/2361/2362/7200 Demo Board		
44.736	DS-3	78P236-DB
44.736	DS-3	78P7200-DB
51.840	STS-1	78P2361-DB
34.368	E-3	78P2362-DB

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Application Guide
Monolithic Dual-Tone Multi-Frequency (DTMF) Receivers

January 1993

INTRODUCTION

The Silicon Systems integrated DTMF Receivers and Transceivers are complete Touch-Tone™ detection and generation systems. Each can operate in a stand-alone mode for the majority of telecommunications applications, thereby providing the most economical implementation of DTMF signaling systems possible. Each combines precision active filters and analog circuits with digital control logic on a monolithic CMOS integrated circuit. SSI DTMF chip use is straightforward and the external component requirements are minimal. This application guide describes device operation, performance, system requirements and typical application circuits for the SSI DTMF chips.

HOW THE SILICON SYSTEMS DTMF CIRCUITS WORK

GENERAL DESCRIPTION OF OPERATION

The task of a DTMF Receiver is to detect the presence of a valid DTMF signal on a telephone line or other transmission medium. The presence of a valid DTMF signal indicates a single dialed digit; to generate a valid digit sequence, each DTMF signal must be separated by a valid pause.

Table 1 gives the established Bell system standards for a valid DTMF signal and a valid pause. The SSI DTMF Receivers meet or exceed these standards.

Similar device architecture is used in all SSI DTMF Receivers. Figure 1 shows the SSI 75T202 Block Diagram. This architecture is implemented in all Silicon Systems single chip receivers, as well as SSi Transceivers. In general terms, the detection scheme is as follows: The input signal is pre-filtered and then split into two bands, each of which contains only one DTMF tone group. The output of each band-split filter is amplified and limited by a zero-crossing detector. The limited signals, in the form of square waves, are passed through tone frequency bandpass filters. Digital logic is then used to provide detector sampling and determine detection validity, to present the digital output data in the correct format, and to provide device timing and control.

PARAMETER	VALUE
One Low-Group Tone, and	697, 770, 852 or 941 Hz
One High-Group Tone	1209, 1336, 1477 or 1633 Hz
Frequency Tolerance	fo ± (1.5% + 2 Hz)
Amplitude Range	-24 dB ≤ A ≤ 6 dBm @ 600Ω (Dynamic Range 30 dB)
Relative Amplitude (Twist)	$-8\,\text{dB} \leq \frac{\text{High Group Tone}}{\text{Low Group Tone}} \leq +4\,\text{dB}$
Duration	40 ms or longer
Inter-tone Pauses	40 ms or longer

TABLE 1: Bell System Standards

PERFORMANCE CONSTRAINTS

SPEECH IMMUNITY AND NOISE TOLERANCE

The two largest problems confronting a DTMF Receiver are:

1) Distinguishing between valid DTMF tone pairs and other speech or stray signals that contain DTMF tone pair frequencies. This is referred to as Speech Immunity.

2) Detecting valid tone pairs in the presence of noise, which is typically found in the telephone (or other transmission medium) environment. This is referred to as Noise Tolerance.

The SSI DTMF Receivers use several techniques to distinguish between valid tone pairs and other stray signals. These techniques are explained in later sections. Briefly, the techniques are:

1) Pre-filtering of audio signal. Removes supply noise and dial tone from input audio signal and emphasizes the voice frequency domain.

2) Zero-cross detection. Limits the acceptable level of noise during detection of a tone pair. Important for speech rejection.

3) Valid tone pair/pause sampling. Samples the detection filters and checks for consistency before a valid tone is declared.

DETAILED DESCRIPTION OF OPERATION

AUDIO PREPROCESSOR

The Audio Preprocessor is an analog filter that band limits the input analog signal between 500 Hz and 6 kHz. In addition, it emphasizes the 2 kHz to 6 kHz voice region.

Band limiting suppresses power supply and dial tone frequencies, and high frequency noise. The emphasized voice region helps to equalize the audio response since many phone lines tend to roll off at about 1 kHz. In addition, preservation of the upper voice frequencies is important in providing speech immunity.

TONE BAND SPLITTING

After the analog signal is preprocessed, it is split into two bands, each of which contains only one DTMF tone

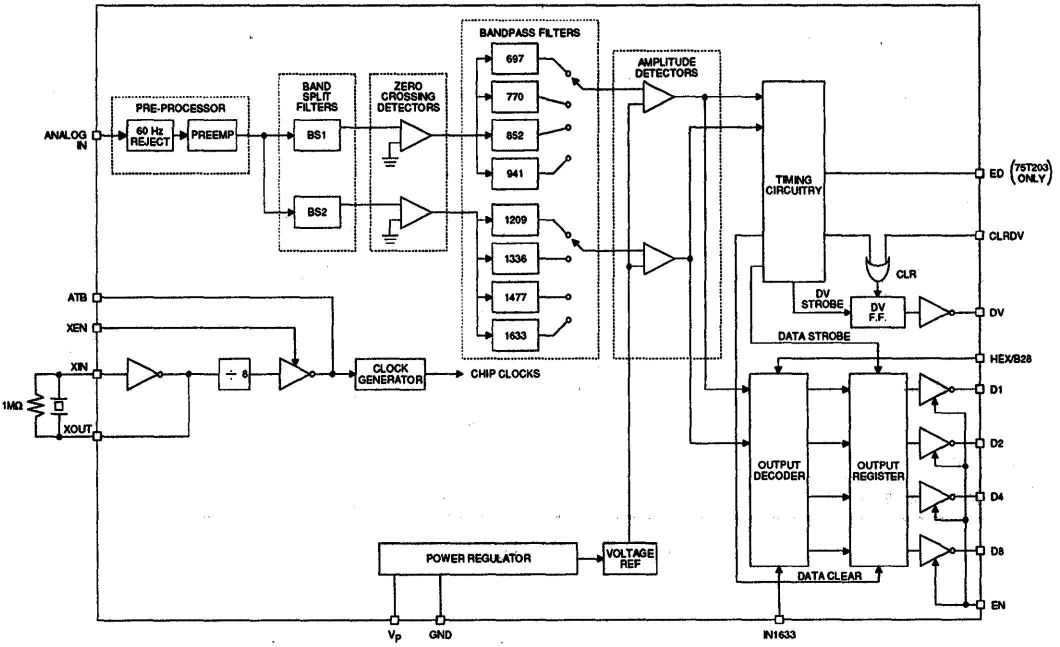


FIGURE 1: SSI 75T202 Block Diagram

group. The band-split filters are actually band-stop filters to maintain all frequencies except the *other* tone group; this is done to maintain all analog information to enhance speech immunity but not allow the other tone group to act as interfering noise for the band being detected. These band-stop filters have "floors" that limit the amount of tone pair twist which further enhances speech immunity. See device data sheets for acceptable twist limits.

ZERO-CROSSING DETECTORS

The output of each band-split filter is amplified and limited by a zero-crossing detector (limiter). The function of the zero-crossing detector is to produce a square wave at the prime frequency emanating from the band-split filter. If a pure tone is not present, as in the case of voice or other interfering noise, a rectangular wave with a variable period will result. Proportional to the interference, the limiter output power is spread over a broad frequency range as the zero crossings "dither." When a high level of noise or speech occurs, no single bandpass filter pair will contain significant power long enough to result in a tone detection. On the other hand, when a pure DTMF tone exists with acceptable noise levles, the output of the limiter will not have any significant dither and tone detection will occur. The zero-crossing detector also acts as AGC (Automatic Gain Control) in that the output amplitude is independent of input amplitude; this additionally establishes an acceptable signal-to-noise ratio not dependent on tone amplitude.

BANDPASS FILTERS & AMPLITUDE DETECTORS

The bandpass filters perform tone frequency discrimination. Their responses are tailored so that if the frequency of the limited square wave from the zero-crossing detector is within the tone frequency tolerance, the fitler output will exceed the amplitude detector threshold. The amplitude detectors are interrogated periodically by the digital control circuitry to acertain the presence of only one tone in each band for the required duration. In a similar fashion, valid pauses are measured by the absence of valid tone pairs for the specified time.

TIMING AND LOGIC

During the qualification process, the output decoder gererates the proper digital code for the received DTMF tone pair. After the fidelity and duration of this signal have been verified, the timing circuitry latches this code into the output register and raises the data valid (DV) flag.

The only precision external element needed for the SSI DTMF Receivers is a 3.58 MHz parallel resonant crystal (color-burst frequency) with a .01% tolerance for the on-board oscillator. A 1 MΩ 10% resistor should be connected in parallel with the crystal. This generates the precise clock for the filters and for the logic timing and control of the chip.

CIRCUIT IMPLEMENTATION

Standard CMOS technology is used for the entire circuit. Logic functions use standard low-power circuitry while the analog circuits use precision switched-capacitor-filter technology.

HOW TO USE THE SSI DTMF RECEIVERS

PRECAUTIONS

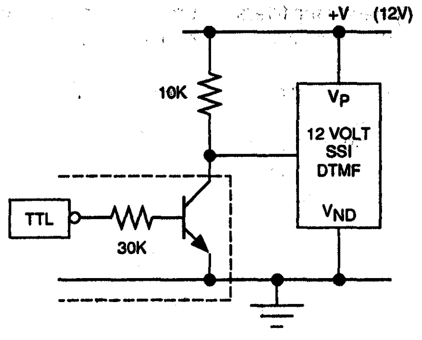
Although static protection devices are provided on the high-impedance inputs, normal handling precautions observed for CMOS devices should be used.

All CMOS parts are prone to a destructive latch-up mode. This behavior is inherent to these parts due to their physical structure. The latch-up mode can best be described as a low impedance, high current state existing between the power supply connections on a CMOS chip. This is also referred to as triggering of parasitic SCR behavior.

The most common cause of a latch-up mode is operating a CMOS part outside its rated power supply voltage. This over-voltage need not be applied at power supply pins only to cause latch-up. Latch-up can occur when over-voltage is applied at any input or output. For the SSI DTMF Receivers & Transceivers, the pin voltages should be constrained to the range between VN – 0.5V and VP + 0.5V (except the analog input pin whose conditions are discussed below). Clamping diodes should be utilized wherever necessary to ensure that voltage ratings are not exceeded.

Another cause for latch-up is fast dv/dt transients affecting the chip. These transients are encountered in applications that require the connection/disconnection of "live" boards. While these applications are very rare and their implementation is best avoided, it must be mentioned that whenever they are necessary, they present a severe environment for CMOS parts. Care must be taken in such instances to ensure that ground planes and rails are connected first and disconected last. This will go a long way in eliminating voltage transients.

Voltage transients that exist on power lines must also be eliminated. High voltage transients caused by switching of high current devices can trigger latch-up. High frequency decoupling is a requirement for the proper operation of the SSI DTMF devices. A 0.01µF to a 0.1µF ceramic decoupling capacitor should be connected to the power supply pin at the chip.



OPEN COLLECTOR INTERFACE

FIGURE 2: Interface Circuit for Conversion from TTL Output Levels to 12V SSI DTMF Input Levels

POWER SUPPLY

Excessive power supply noise should be avoided, and to aid the user in this regard, power supply hook-up options are provided on some devices.

Since the digital circuitry of the devices possess the high noise immunity characteristics of CMOS logic, it is the analog section that is affected most by power supply noise. On those SSI DTMF Receivers that have separate Analog Negative and Digital Negative supply connections (grounds), namely VNA and VND, an unfiltered supply may be used at VND. It is necessary that VND and VNA differ no more than 0.5V.

The analog circuitry of the devices require low power supply noise levels as specified on the device data sheet. The effects of excessive power supply noise are decreased tone amplitude sensitivity and less tone detection frequency bandwidth. Power supply noise can be significantly reduced by decoupling the chip with a 0.1µF ceramic capacitor. Power supply noise effects will be slightly less if the analog input is referenced to VP. This is normally accomplished by connecting VP to ground and utilizing a negative power supply.

DIGITAL INPUTS

The digital inputs are directly compatible with standard CMOS logic devices powered by VP and VN (or VND). The input logic levels should swing within 30% of VP or VN to insure detection. Any unused input must be tied to VN or VP. Figure 2 shows a method for interfacing TTL outputs to 12V SSI DTMF Receivers.

ANALOG INPUT

The analog input is the signal input pin for the devices, and is specially biased to facilitate its connection to external circuitry, as shown in Figure 3. The signal level at the analog input pin must not exceed the positive supply as stated on the device data sheets. If this condition cannot be guaranteed by the external circuitry, the signal must be AC coupled into the chip with a .01µF ± 20% capacitor.

ANALOG INPUT NOISE

The SSI DTMF Receivers will tolerate wide-band input noise of up to 12 dB below the lowest amplitude tone component during detection of a valid tone pair. Any single interference frequency (including tone harmonics) between 1 kHz and 6 kHz should be at least 20 dB below the lowest amplitude tone component. Adherence to these conditions will ensure reliable detection and full tone detection frequency bandwidth. Because of the internal band limiting, noise with frequencies above 8 kHz can remain unfiltered. However, noise near the 56 kHz internal switched-capacitor-filter sampling frequency will be aliased (folded back) into the audio spectrum; noise above 28 kHz therefore should be low-pass filtered with a circuit as shown in Figure 4 using a cut-off frequency (*f*c) of 6.6 kHz.

A 1 kHz cut-off frequency filter can be used on "normal" phone lines for special applications. When a phone line is particularly noisy, tone pair detection may be unreliable. A 1 kHz low pass filter will remove much of the noise energy but maintain the tone groups; however, a decreased speech immunity will result. This usage should only be considered for applications where speech immunity is not important, such as control paths that carry no speech.

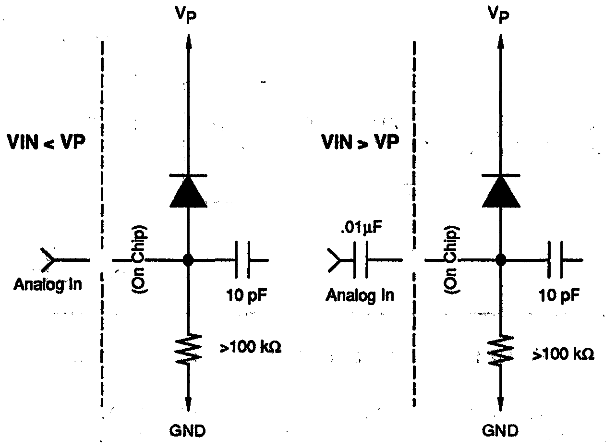


FIGURE 3: Direct and AC Coupled Configurations

Some DTMF tone pair generators output distorted tones which the SSI DTMF Receivers may not detect reliably (inexpensive extension telephones are an example). Most of the interfering harmonics of these may be removed by the use of a 3 kHz low-pass filter as in Figure 4. Some speech immunity degradation will result. It should be mentioned that when using low-pass filters, a higher cut-off frequency will preserve more of the speech immunity advantages.

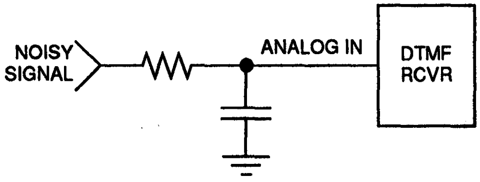
The SSI DTMF Receivers provide superior speech immunity and noise rejection. The analog signals are subjected to stringent criteria and rigorous qualification in order to assure that only true DTMF tone pairs are detected and decoded properly. Stray signal and noise with sufficient amplitude will cause a DTMF receiver to disqualify a DTMF tone pair.

Such a condition can be occasionally encountered when using DTMF "beepers." Beepers are normally used to transmit DTMF signals from dial-pulse phones. It has been observed that the non-linearity in the response of carbon microphones in telephone handsets introduces intermodulation products, which actually produce new frequency components. These components happen to fall direclty into the useful bandwidths of some of the basic tones that the receiver must detect. Because of the presence of these components (normally referred to as third-tone) with a valid DTMF tone, detection is disabled. To inhibit the more common higher frequency third tones from arriving to the receiver, the circuit shown in Figure 5 is suggested.

TELEPHONE LINE INTERFACE

In applications that use an SSI DTMF Receiver to decode DTMF signals from a phone line, a DAA (Direct Access Arrangement) must be implemented. Equipment intended for connection to the public telephone network must comply with and be registered in accordance to FCC Part 68. For PBX applications refer to EIA Standard RS-464.
Some of the basic guidelines are:

1) Maximum voltage and current ratings of the SSI DTMF Receivers must not be exceeded; this calls for protection from ringing voltage, if applicable, which ranges from 80 to 120V RMS over a 20 to 80 Hz frequency range.
2) The interface equipment must not breakdown with high-voltage transient tests (including a 2500V peak surge) as defined in the applicable document.
3) Phone line termination must be less than 200Ω DC and approximately 600Ω AC (200-3200 Hz).
4) Termination must be capable of sustaining phone line lop current (off-hook condition) which is typically 18 to 120 mA DC.
5) The phone line termination must be electrically balanced with respect to ground.
6) Public phone line termination equipment must be registered in accordance to FCC Part 68 or connected through registered protection circuitry. Registration typically takes about six months.



F_C (kHz)	R (kΩ) (±5%)	C (µF) (±20%)
1.0	1.6	0.1
3.1	5.1	.01
6.6	2.4	.01

SUGGESTED
COMPONENT VALUES

FIGURE 4: Filter for Use in Noisy Environments

Ready made DAA devices are also available. The SSI 73M9001 is a DAA Micromodule housed in a 30-pin DIP footprint.

Figure 6 shows a simplified phone line interface using a 600Ω 1:1 line transformer. Transformers specially designed for phone line coupling are available from many transformer manufacturers.
Figure 7 shows a more enhanced version of Figure 6. These added features include:

1) A 150V surge protector to eliminate high voltage spikes.
2) A Texas Instruments TCM 1520A ring detector, optically isolated from the supervisory circuitry.
3) Back-to-back Zener diodes to protect the DTMF (and optional multiplexer Op-Amp) from ringer voltage.
4) Audio multiplexer which allows voice or other audio to be placed on the line (a recorded message, for example) and not interfere with incoming DTMF tone detection.

OUTPUTS

The digital outputs of the SSI DTMF Receivers (except XOUT) swing between VP and VN (or VND) and are fully compatible with standard CMOS logic devices powered from VP and VN. The 5V DTMF devices will also interface directly to LSTTL. The 12V DTMF devices can interface to TTL or low voltage MOS with the circuit in Figure 8.

Data Outputs D8, D4, D2 and D1 are three-state enabled to facilitate interface to a three-state bus. Figure 9 shows the equivalent circuit for the data outputs in the high impedance state. Care must be taken to prevent either substrate diode in Figure 9 from becoming forward biased or damage may result.

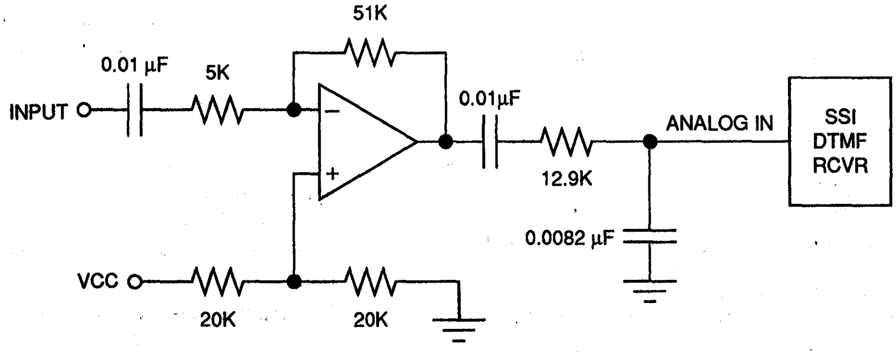


FIGURE 5: Filter for Use in Environments where a Third Tone Exists

TIMING

Within 40 ms of a valid tone pair appearing at the DTMF Receiver Analog Input, the Data Outputs D8, D4, D2 and D1 will become valid. Seven microseconds after the data outputs have become valid DV will be raised. DV will remain high and the outputs valid while the valid tone pair remains present. Refer to individual data sheets for the timing of signals.

SYSTEM INTERFACE

Provision has been made on the SSI DTMF Receivers (with the exception of SSI 75T204) for handshake interface with an outside monitoring system. In this mode, the DV strobe is polled by the monitoring system at least once every 40 ms to determine whether a new valid tone pair has been detected. If DV is high, the coded data is stored in the monitoring system and the CLRDV is pulsed high. With some systems operating in the handshake mode, it may be desirable to know when a valid pause has occurred. Ordinarily this would be indicated by the falling edge of DV. However, in the handshake mode, DV is cleared by the monitoring system each time a new valid tone pair is detected and, therefore, cannot be used to determine when a valid pause is detected. The detection of a valid pause in this case may be observed by detecting the clearing of the Data Outputs. Since, in hexadecimal format (the mode normally used with a handshake interface), the all zero state represents a commonly unused tone pair (D), the detection of a valid pause may be detected by connecting a four-input NOR gate to the device outputs and sensing the all zero state.

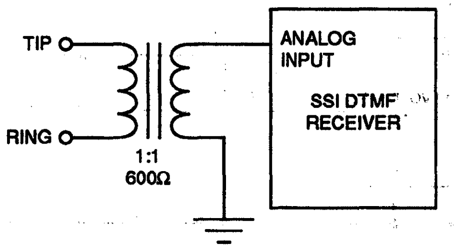


FIGURE 6: Simplified Phone Line Interface

TIME BASE

The SSI DTMF Receivers contain an on-chip oscillator for a 3.5795 MHz parallel resonant quartz crystal or ceramic resonator. The crystal (or resonator) is placed between XIN and XOUT in parallel with a 1 MΩ resistor, while XEN is tied high. Since the switched-capacitor-filter time base is derived from the oscillator, the tone detect band frequency tolerance is proportional to the time base tolerance. The SSI DTMF Receiver frequency response and timing is guaranteed with a time base accuracy of at least ± 0.01%. To obtain this accuracy the CTS Part No. MP036 or Workman Part No. CY1-C or

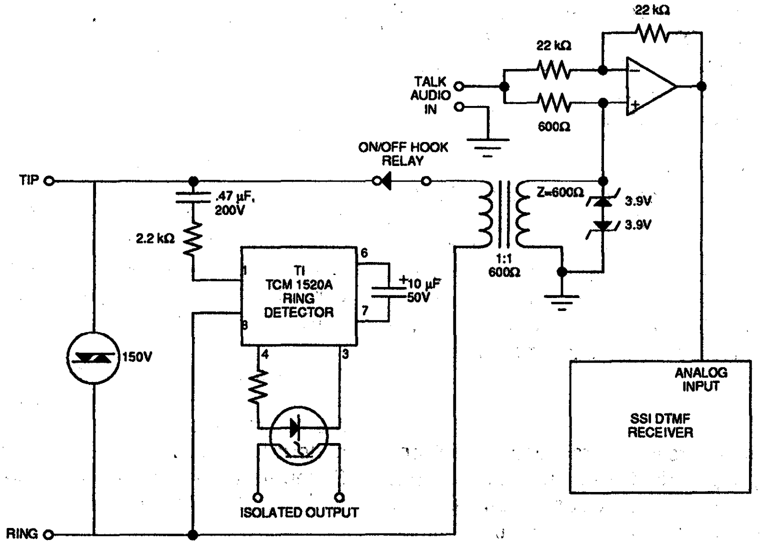


FIGURE 7: Full Featured Phone Line Interface

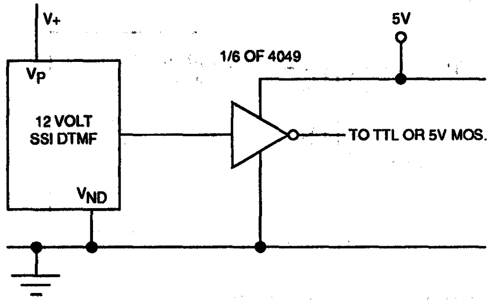


FIGURE 8: SSI 12V DTMF to TTL Level Interface

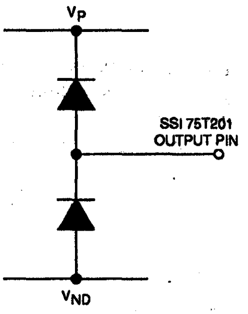


FIGURE 9: Equivalent Circuit of SSI DTMF Receiver Data Output in High Impedance State

equivalent quartz crystal is recommended. In less critical applications a suitable ceramic resonator may be implemented.

The use of a ceramic resonator requires the addition of two 30 pF ± 10% capacitors; one between XIN and VN (or VND) and the other between XOUT and VN (or VND). Extra caution should be used to avoid stray capacitance on the resonant circuit when using a ceramic resonator instead of a quartz crystal.

When the oscillator is connected as above and XEN is tied high, the ATB (Alternate Time Base) pin delivers a square wave output at one-eighth the oscillator frequency (447.443 kHz nominal). The ATB pin can be converted to a time base input by tying XEN low; ATB can then be externally driven from another device such as the ATB output of another DTMF. No crystal is required for the ATB input device; XIN must be tied high if unused. Several SSI DTMF Receivers can be driven with a single crystal (refer to device data sheet for fan-out limit).

XOUT is designed to drive a resonant circuit only and is not intended to drive additional devices. If a 3.58 MHz clock is needed for more than one device and it is desirable to use only one resonant device, an outside inverter should be used for the time base, buffered by a second inverter or buffer. The buffer output would then drive XIN of the SSI DTMF Receiver as well as the other device(s); XOUT must be left floating and XEN tied high.

DIAL TONE REJECTION

The SSI DTMF Receivers incorporate enough dial tone rejection circuitry to provide dial tone tolerance of up to 0 dB. Dial tone tolerance is defined as the total power of precise dial tone (350 Hz and 440 Hz as equal amplitudes) relative to the lowest amplitude tone in a valid tone pair. The filter of Figure 10 may be used for further dial tone rejection. This filter exhibits an elliptic highpass response that provides a minimum of 18 dB rejection at 350 Hz, and 24 dB rejection at 440 Hz so long as the component tolerances indicated are observed. The DTMF on-chip filter rejects 350 Hz at least 6 dB more than 440 Hz. Therefore, employing the filter of Figure 10 yields a dial tone tolerance of +24 dB.

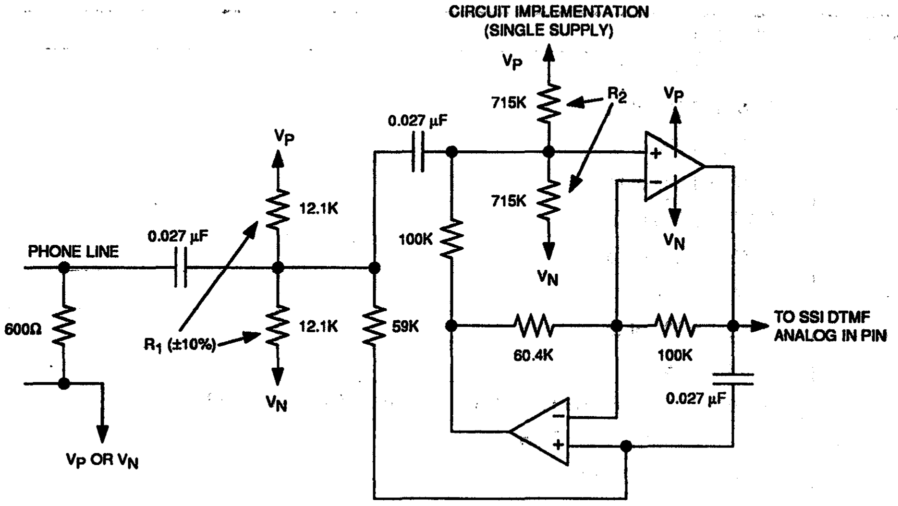
PRINTED CIRCUIT BOARD IMPLEMENTATION

The SSI DTMF Receivers are analog in nature and should be treated as such; circuit noise should be kept to a minimum. To be certain of this, all input and output lines should be kept away from noise sources (high frequency data or clock lines); this is especially true for the Analog Input. Noise in the ground or power supply lines can be avoided by running separate traces to supportive logic circuits or by running thicker (lower resistance) busses. Capacitance power supply bypassing should be performed at the device. Refer to the Power Supply section above.

PERFORMANCE DATA

A portion of the final SSI DTMF Receiver device characterization uses the Mitel CM7290 tone receiver test tape. The evaluation circuit shown in Figure 11 was used to characterize the SSI 75T201. The speed and output level of the tape deck must be adjusted so that the calibration tone at the beginning of the tape is at exactly 1000 Hz and 2V rms.

The Mitel tape tests yield similar results on all of the SSI DTMF Receivers. Test results for the SSI 75T201 are summarized in Table 2. In short, the measured performance data demonstrates that the SSI DTMF Receivers are monolithic realizations of a full "central office quality" DTMF Receiver.



Note: All resistors 1%, all caps 5%, unless noted, op-amps: 1/2 LM1458 or equivalent

FIGURE 10: Dial Tone Reject Filter

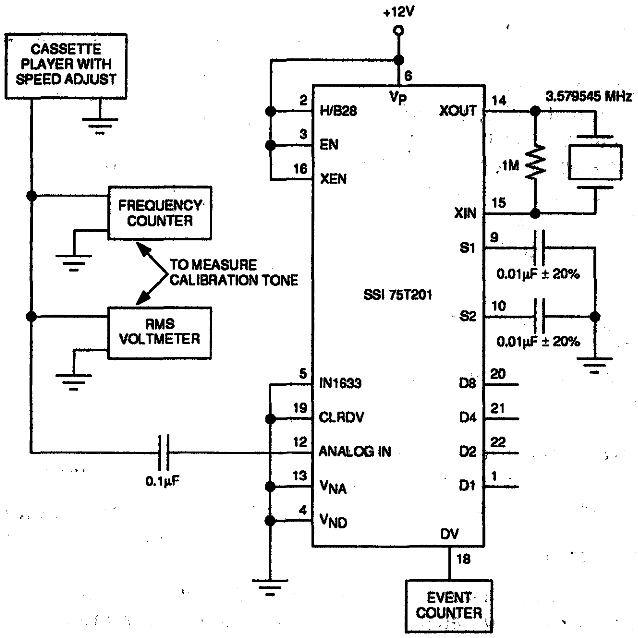


FIGURE 11: Circuit for Receiver Evaluation

TEST #	RESULTS
2a, b	B.W. = 5.0% of fo
2c, d	B.W. = 5.0% of fo
2e, f	B.W. = 5.3% of fo
2g, h	B.W. = 4.9% of fo
2i, j	B.W. = 5.0% of fo
2k, l	B.W. = 5.3% of fo
2m, n	B.W. = 5.3% of fo
2o, p	B.W. = 4.8% of fo
3	160 decodes
4	Acceptable Amplitude Ratio (Twist) = –19.1 dB to +15.2 dB
5	Dynamic Range = 32.5 dB
6	Guard Time = 23.3 ms
7	100% Successful Decodes at N/S Ratio of –12 dBV
8	2-3 Hits Typical on Talk-Off Test

TABLE 2: Mitel #CM7290 Tape Test Results for SSI 75T201 (Averaged for 10 parts)

APPLICATIONS

CREATING HEXADECIMAL "0" OUTPUT UPON DIGIT "0" DETECTION

To be consistent with pulse-dialing systems, the SSI DTMF Receivers provide a hexadecimal "10" output upon the detection of a digit "0" tone pair when in the hexadecimal code format. However, some applications may instead require a hexadecimal "0" with a digit "0" detection. The circuit of Figure 12 shows an easy method to recode the hexadecimal outputs to do this using only 4 NOR gates.

Note that this circuit will not give proper code for the " * ", "B", or "C" digits and will cause both digits "D" and "0" to output hexadecimal "0." This circuit should therefore be considered for numeric digits only. The output code format is shown in Table 3.

This circuit is useful for applications that require a display of dialed digits; the digit display usually requires a hexadecimal "0" input for a "0" to be displayed.

16-CHANNEL REMOTE CONTROL

DTMF signaling provides a simple, reliable means of transmitting information over a 2-wire twisted pair. The complete schematic of a 16-channel remote control is shown in Figure 13. When one of the key pad buttons is depressed, a tone pair is sent over the transmission medium to the SSI DTMF Receiver.

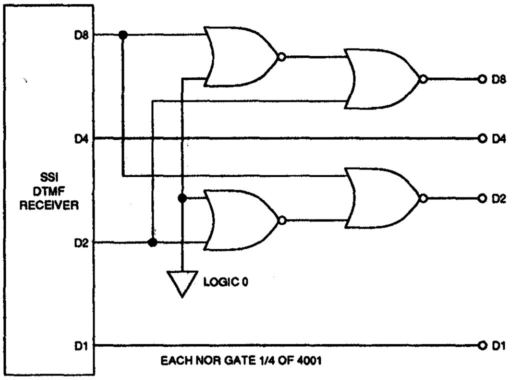


FIGURE 12: Hex "0" Out with Digit "0" Detect Conversion Circuit

The 4514 raises one of its 16 outputs in response to the 4-bit output code from the DTMF. The output at the 4514 will remain high until the next button is depressed.

Hexadecimal					Hexadecimal & Figure 12 Circuit				
Digit	D8	D4	D2	D1	Digit	D8	D4	D2	D1
1	0	0	0	1	1	0	0	0	1
2	0	0	1	0	2	0	0	1	0
3	0	0	1	1	3	0	0	1	1
4	0	1	0	0	4	0	1	0	0
5	0	1	0	1	5	0	1	0	1
6	0	1	1	0	6	0	1	1	0
7	0	1	1	1	7	0	1	1	1
8	1	0	0	0	8	1	0	0	0
9	1	0	0	1	9	1	0	0	1
0	1	0	1	0	0	0	0	0	0
*	1	0	1	1	*	0	0	0	1
#	1	1	0	0	#	1	1	0	0
A	1	1	0	1	A	1	1	0	1
B	1	1	1	0	B	0	1	0	0
C	1	1	1	1	C	0	1	0	1
D	0	0	0	0	D	0	0	0	0

TABLE 3: Output Code of Figure 13

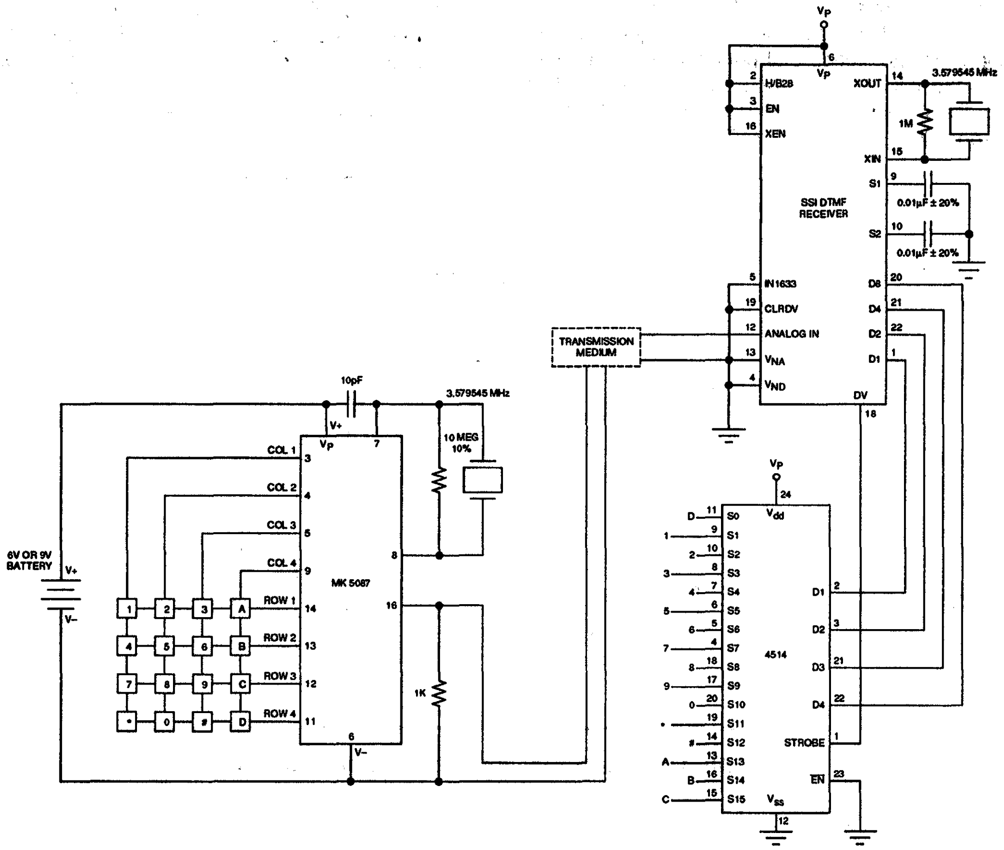


FIGURE 13: 16-Channel Remote Control

2-OF-8 OUTPUT DECODE

The circuit shown in Figure 14 can be used to convert the binary coded 2-of-8 to the actual 2-of-8 code (or 2-of-7 if detection of 1633 Hz tone is inhibited). The output data will be valid while DV is high. If it is desired to force the eight outputs to zero when a valid tone is not present, DV should be inverted and connected to both E–NOT inputs of the 4555.

DTMF TO ROTARY DIAL PULSE CONVERTER

The 2-of-8 output of Figure 14 can be modified to interface with a pulse dialer as shown in Figure 15. If a 12V DTMF is used the 4049 will translate the 12V outputs to the 5V swings required for the MK5099 pulse dialer.

Figure 16 shows the interface for adding pulse detection and counting to a SSI DTMF Receiver.

The loop detector provides a digital output representing the telephone loop circuit "make" and "break" condition associated with rotary pulse dialing. For the circuit of Figure 16, ground represents a "make" and VP a "break." The loop detector feeds dial pulses to IC-1, a binary counter, and to IC-2A, a re-triggerable "one-shot." When a dial pulse appears the Q1-NOT output of IC-2A immediately goes low, resetting IC-1. The clock input to IC-1 is delayed by R1-C1 so that reset and count input do not overlap. The binary outputs of IC-1 will reflect the pulse count and 0.2 seconds after the last pulse the Q1-NOT output will go high. C3-R3 differentiate this pulse and clock the output latch, IC-3, holding the output pulse until the next digit.

The 0.2 second timeout of IC-2A indicates the end of dial pulsing since even a slow (8 pps) dial would input another pulse every 0.125 seconds. The binary outputs of IC-1 are paralleled with those of the SSI DTMF Receiver circuit through diodes to the inputs of IC-3. A pulldown resistor is necessary on each IC-3 input pin. IC-1 must be a binary, not BCD, counter.

With a 4175 for IC-3 the output data is latched until the next valid input, whether from a rotary dial or dual tone instrument. A unique situation exists, however, when going on-hook. The loop detector will output a continuous level of VP which would trigger IC-2A and put a single count into IC-1. A high level from the loop detector also turns on Q1, pulling the clock input of IC-3 to ground. Since the loop detector output will be low at the completion of dialing, all outputs are valid even when the telephone is placed on-hook, an important consideration if output data is recorded.

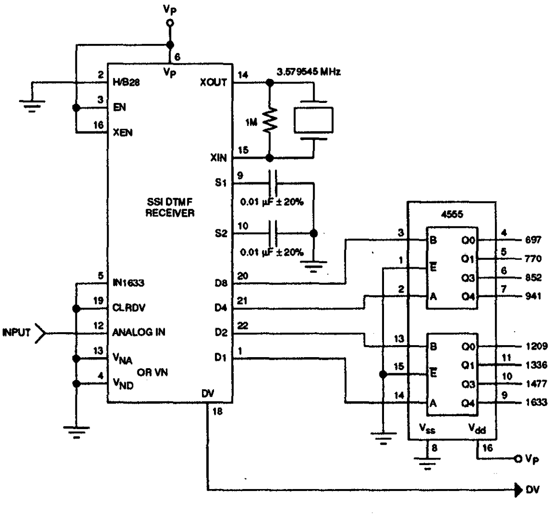


FIGURE 14: Touch-Tone™ to 2-of-8 Output Converter

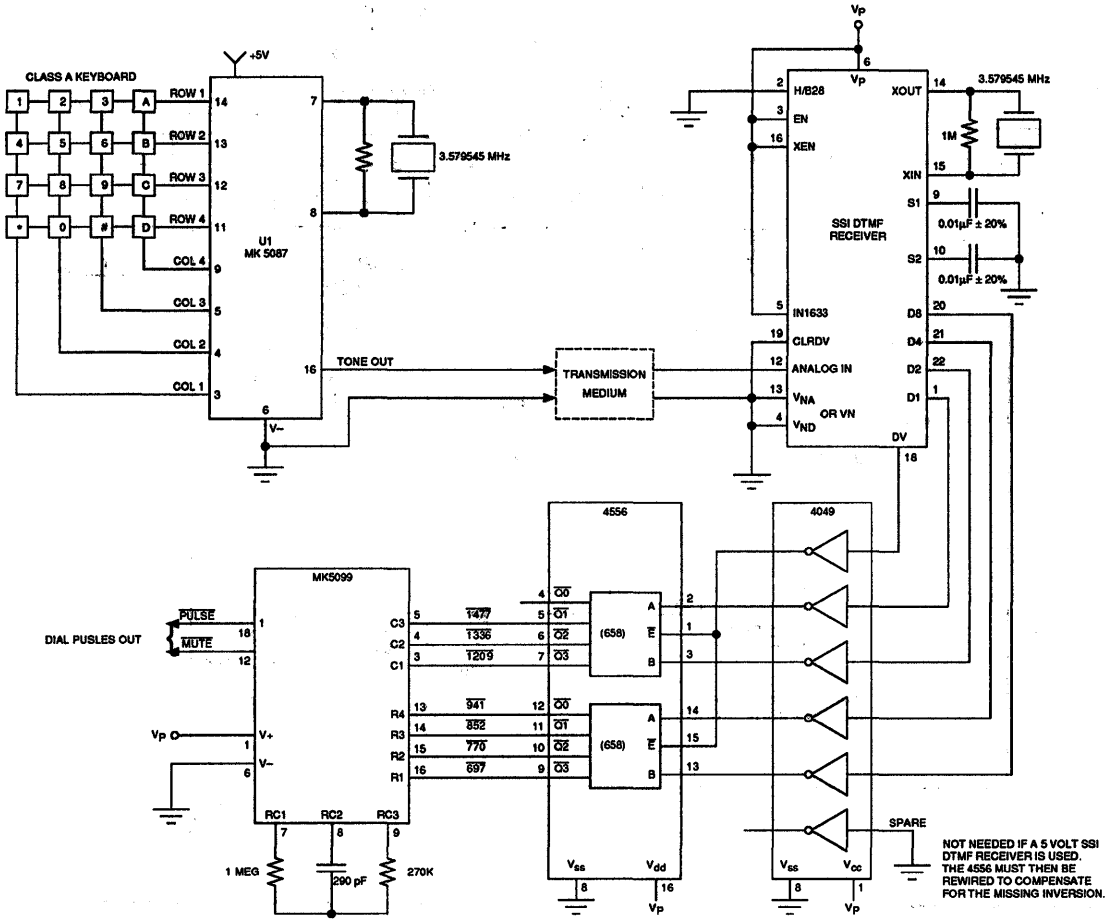
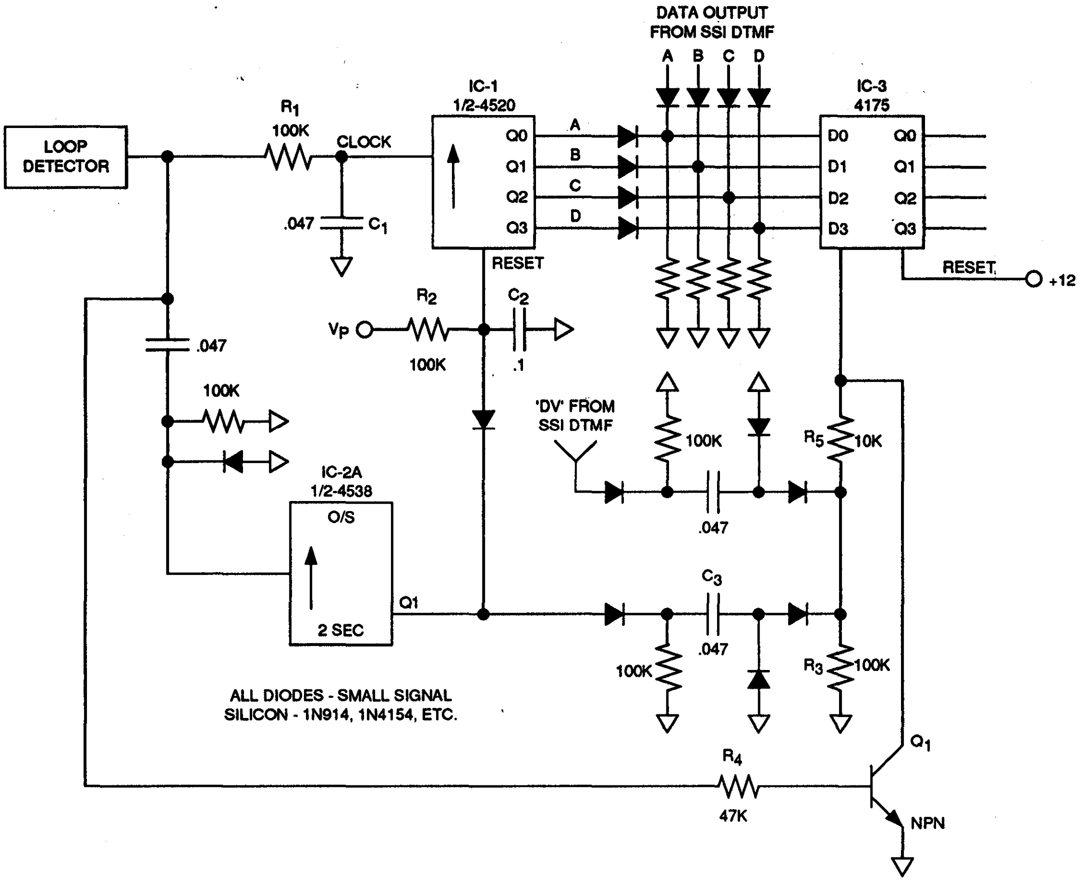


FIGURE 15: Touch-Tone™ to Rotary Dial Pulse Converter Adding Rotary Dial Pulse Detection Capabilities



ALL DIODES - SMALL SIGNAL
SILICON - 1N914, 1N4154, ETC.

FIGURE 16: Adding Pulse Detection and Counting to the SSI DTMF Receiver

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Using an SSI 73M650 Serial Packet Controller

APPLICATION NOTE

December 1992

Using a serial packet controller as a virtual UART, a personal computer's COM port can accept most synchronous or asynchronous communications protocols, while still looking to the PC host like a conventional asynchronous UART. This note will explain the technology and show how it can be used in a typical application. The application chosen is that of a fiber optic link to another computer at data rates of up to 1.2 Mbit/s.

Applications for a virtual UART stretch the imagination. It can be an Input/Output controller for any PC or workstation, regardless of the operating system. When built into a modem, it gives incredible design flexibility. For prototyping of communications links, it is a wonderful emulator. For LAN and WAN applications, it is a powerful packet controller. It is also ideal for multitasking applications such as allowing the PC to communicate with another device, while simultaneously running a non-communications program.

This unique functionality is embodied in the Silicon Systems' SSI 73M650 Serial Packet Controller (SPC). To the PC host, the 650 always looks like a common 550-type asynchronous UART, but, to a device communicating with the PC, the 650 can emulate virtually anything, including an 8530-type USART. With Manchester encode/decode capability, the 650 can even be used with fiber-optic communications links.

In addition to Manchester encoding, the 650 also supports NRZ, NRZI and FM encoding. Since the device is ideal for laptop, or portable PC applications, it includes a power-down mode to extend the computer's battery life. If the application calls for V.42 error control, the 650 includes 32-bit CRC error checking for full V.42 compatibility.

OPERATING MODES

The first step in designing with the 650 is selecting the mode of operation. Two basic modes are available: single-processor and dual-processor (Figure 1). Single-processor (see Figure 2) can be broken down further into two basic architectures, which will be discussed in the section on design decisions.

Primary among the reasons for using a single-processor design is cost savings. However the capabilities are far more limited than with a dual-processor design (see Figure 2). The single-processor configuration must be dedicated to a single task. It must share the host CPU. In most applications it is limited to a data rate of 9600 bits/s due to the interrupt handling limits of the host cpu. And, while it is compatible with the V.22bis data communications standard, including compression, it can not be used in designs requiring compliance with more advanced specifications, such as V.32 and V.42bis.

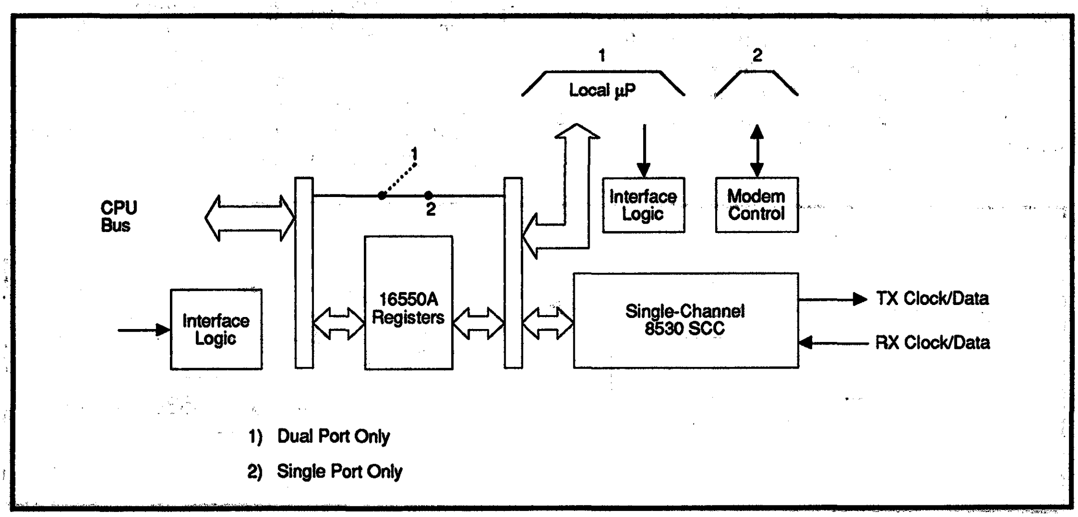


FIGURE 1: SSI 73M650 Block Diagram

OPERATING MODES (continued)

V.32 is a 9600 bit/s modem data pump modulation standard. V.42bis is a CCITT compression standard that is capable of up to 4:1 compression ratios.

Dual-processor designs offer the increased flexibility of multi-tasking. However, it also requires a dedicated microprocessor, albeit an inexpensive one. Much higher data rates can be handled, and compatibility can be achieved with standards such as:

- V.32 with compression
- V.32 at 9600 bit/s
- V.32 bis at 14,400 bit/s
- V.42 bis with 4:1 compression
- V.22 bis at 2400 bit/s

Single-processor decisions

If the single-processor mode is selected, several questions must be asked by the designer. The first has to do with the method of addressing the part. There are three addressing modes for the 650: 550; 8530; and 8530 in the 550 address space. The method of addressing that is selected depends upon the host software being used. If it expects to see a 550 UART, the 550 addressing mode must be used. Likewise, the expectations of the host software will also determine if either of the other two modes is correct.

Separate addressing and chip-select pins are available for the 550 and 8530 blocks. When the 8530 must be addressed in the 550 address space, the chip selects for both blocks have to be wired together. In addition, an external device, for example, an intelligent data pump, may be mapped into the same address space as the 550 register set.

Next, the designer needs to know whether the 650 will address external devices within the 550 address space. If the designer wishes to utilize the 650's internal decoder to address external devices, the external devices must be compatible with the bus timing produced by the 650.

Finally, the designer must decide whether to configure the 650 in a mailbox mode, utilizing the 550 block's 16-byte FIFO as a mailbox. In a mailbox mode, applications are possible where the 550's register set is required to interface to standard software, but the additional functionality of the 8530 is required for either synchronous communications or data compression.

Dual-processor decisions

The main advantage of the dual-processor mode is the addition of a dedicated microprocessor to control the 650. A simple inexpensive 8-bit microprocessor can be selected, such as an Intel 8051 or comparable part. With a dedicated microprocessor, it is no longer necessary to steal cycles from the host PC CPU to control the synchronous section of the 650.

As can be seen in Figure 4, along with the dedicated microprocessor, comes buffer storage (RAM). If a lot of buffer storage is required for the application, inexpensive dynamic RAM is suggested.

For the particular application under design, a decision has to be made about how much buffer storage is required, and what type of buffer storage will be used. The minimum buffer size is one packet of data. However, several packets should be stored to improve link efficiency. From a flow-control standpoint, the buffer needs to store enough data so that, when a control word is detected, the control action can be taken at the proper point in the data 5 stream.

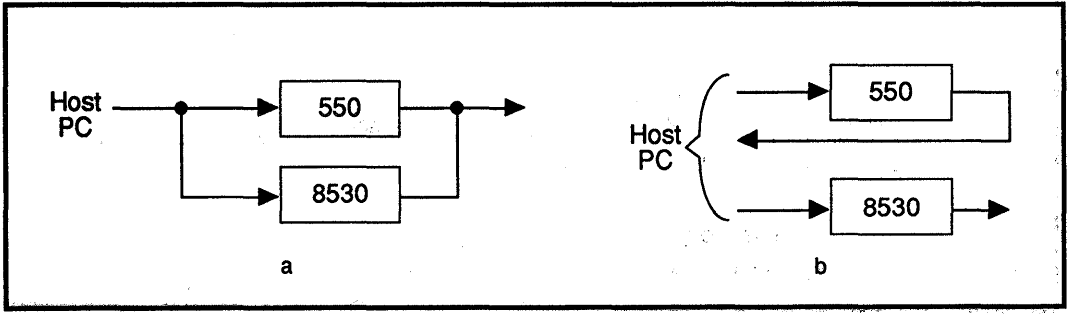


FIGURE 2: Operation Mode Architectures

Here the amount of buffer storage is related to the data rate and the time required to provide a signal to the other end of the link.

The designer needs to determine whether the control code will be resident in the dedicated microprocessor, or somewhere else in the system RAM. There are maintenance advantages to storing control code in RAM and downloading it to the microprocessor.

The next design decision is how to pass control information from the host cpu to the dedicated microprocessor. It is advantageous to use the scratch register for loading data path flow control information. If the flow control information is not put into the scratch register, it would have to be loaded in the data path itself. In this circumstance, additional intelligence is required to strip the flow control codes out of the data stream, and to act upon them.

Finally, the designer needs to decide whether to use the DMA lines to the host processor to speed up memory access. In most cases this will not be necessary.

DESIGNING A HIGH-SPEED FIBER-OPTIC DATA NETWORK

An excellent example of the use of the 650 is in the design of a high-speed fiber-optic data network. This network ties together several IBM-compatible personal computers, as well as an assortment of peripheral devices, which can be shared on the network. Particularly high-rates of data transfer are required, since large graphic files will be sent around the link, in order that the laser printer and plotter on the link can be used to print those files.

Rather than using an expensive hub file server, the network will have a ring configuration with no central file server (see Figure 5). Fiber-optic cable is the choice for the transmission medium due to its inherent resistance to RFI.

To use conventional communication software on the network, each station on the network must look like a 550-type UART. A serial form of communication protocol will be used for the devices to communicate together. This protocol will provide error detection and retransmission, to insure that data is transferred without being corrupted, and the protocol will provide a means for equal sharing of the resources between the demands of the users, to prevent the network from being dominated by the demands of a single user.

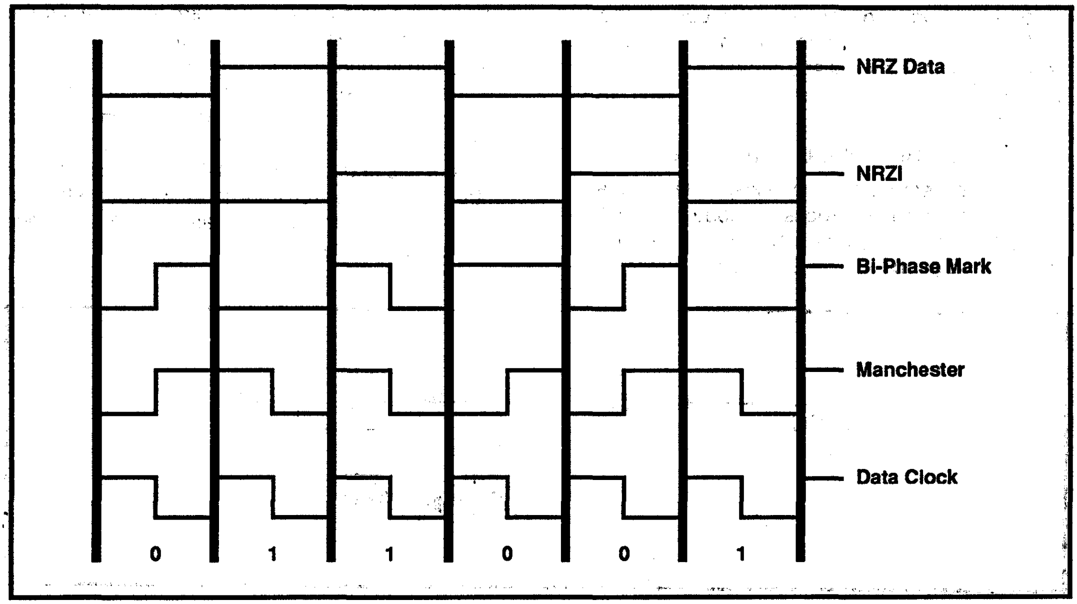


FIGURE 3: Methods of Encoding

DESIGNING A HIGH-SPEED FIBER-OPTIC DATA NETWORK

(continued)

A synchronous communications protocol, such as SDLC, will be used, since these protocols contain the desired error-checking facilities. SDLC has the drawback of requiring a clock to recover data from the network. However, SDLC can be transmitted, with Manchester clock encoding to encode the data clock with the serial data, to allow the clock to be recovered at the receiver. Encoding the clock along with the data has the advantage that any changes in the timing, due to effects of bias distortion occurring on data transmitted, will be performed on the clock information stored in the data stream as well. This insures that the data clock will always have the same timing in relation to the data being transmitted on the network. When the clock is recovered from the data path, the data clock will always occur with the correct timing for the serial communication controller to sample the serial receive data.

In order for the standard PCs on the network to communicate with conventional software, they need to see a conventional 550-type UART. However, a 550-type UART is an asynchronous device that cannot understand a synchronous protocol such as SDLC. Hence, some sort of protocol converter is required. The SSI 73M650 is selected for this application, since it can accept most any protocol and convert it to a signal that looks to the PC host like a standard 550-type UART.

SELECTING THE MODE OF OPERATION

Single-processor mode is not acceptable in this application, since, in single-processor mode, the 650 looks to the PC host like either a 550-type asynchronous UART or an 8530-type synchronous controller. However, it will not allow the PC-host to see a 550-type UART while the network sees an 8530-type synchronous controller to accept SDLC.

Therefore, dual-processor mode of operation will be used (see Figure 6), with a dedicated microprocessor and a RAM buffer. The built-in Manchester encoder will be used to transmit SDLC on a high-speed fiber-optic network. Although only 1K of buffer RAM is needed for data and about 3K are needed for control code, 32K of RAM will be used. 32K of RAM is one of the smallest, least expensive modules that can be readily used. Both data and control code will be stored in the buffer, with the control code being down-loaded to the microprocessor when needed. The scratch register in the 550 block will be used to load the control code.

To see how the 650 is used, look first at the data flow. Data that is loaded in octets in the 550 registers can then be read as octets by a control communications microprocessor from the "back-end" of the 550 register set. This data is normally moved into a temporary RAM storage location until there is enough data to form an SDLC data packet. The data is then moved from the temporary RAM buffer to the synchronous emulation block in the 650. The data is transmitted out in a packet, according to the protocol rules of SDLC loop transmission, with the synchronous controller forming the start flags and the data packet, with zero insertion per the requirements of SDLC loop protocol. The zero-inserted data is then encoded with the data-clock information through the Manchester encoder circuitry in the 650. The serial data stream is then transmitted to a fiber-optic driver for transmission over the link. When the last 8 bits of data is transmitted to the 650 by the control microprocessor from the temporary storage, the 650 transmits the correct frame check sequence and a required closing flag.

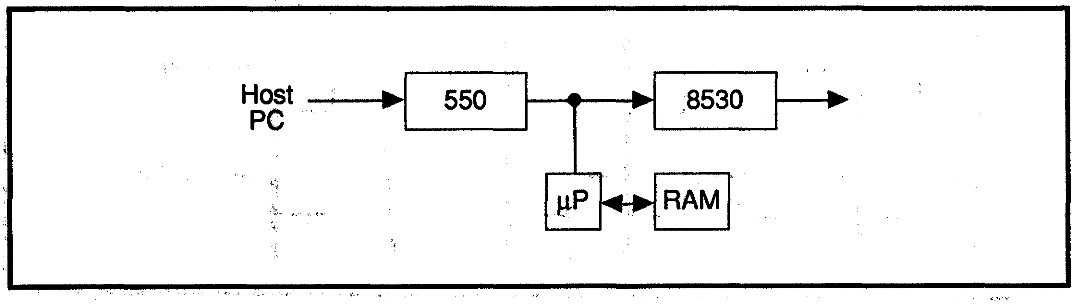


FIGURE 4: Buffer Storage

SELECTING THE MODE OF OPERATION (continued)

In SDLC, all data is transmitted from one controller, which is designated the master, to slave controllers on the loop. All data on a slave controller passes from the receive port to the transmit port. If the controller is actively "on loop," the data that is received is reclocked and retransmitted with a one-bit delay. This one-bit delay allows data to be retimed to reduce bias distortion caused by the fiber-optic network. Every slave controller passes data from its own receiver to its internal transmitter, to pass to the next slave controller down the line. The final slave controller transmits the packet of data back to the host controller's receiver.

SDLC AND EOP FLAGS

In an SDLC loop, the network starts with the host controller sending out an End Of Poll (EOP) flag. This is a flag that looks like a normal flag of 01111110, 07Eh, but which is modified slightly to 11111110, 07fh (note: in serial communications the LSB is transmitted first, and hence the bit pattern is shown rather than the actual binary number). This EOP flag is used by each slave controller to determine when it should transmit to the host controller.

When a slave controller encounters an EOP flag, it changes the EOP flag to a normal SDLC flag and transmits a data packet to the host controller. When the controller is finished transmitting, the controller attaches the correct frame check sequence (FCS) to the data packet and closes the frame with an EOP flag.

Since the first detected EOP is changed by the actively transmitting slave controller on the network to an SDLC flag, any downstream controllers are prevented from transmitting, since no EOP will be encountered. The downstream slave controller must wait until an EOP is encountered before the controller is allowed to transmit a packet of data to the host controller. A slave controller is normally restricted from transmitting for a set period of time after a frame has been shipped, to prevent domination of the network by upstream controllers.

In our network, a destination address byte is transmitted first, followed by a source address byte, followed by a control byte that contains a frame sequence number. The host software requires the host to acknowledge the reception from the slaves at least once every seven data frames. A slave data controller cannot transmit a data packet to the host until the last seven data packets have been acknowledged from the host controller. The host controller will not acknowledge a slave until EOP frames are detected back at the host's receiver.

The host receiver will only detect an EOP sequence of two adjacent EOP flags if a "no transmission" was attempted by a slave controller. Receiving two adjacent EOP flags indicates all slaves have had a fair chance to utilize the network. This method of arbitration prevents domination of the network by an upstream slave controller.

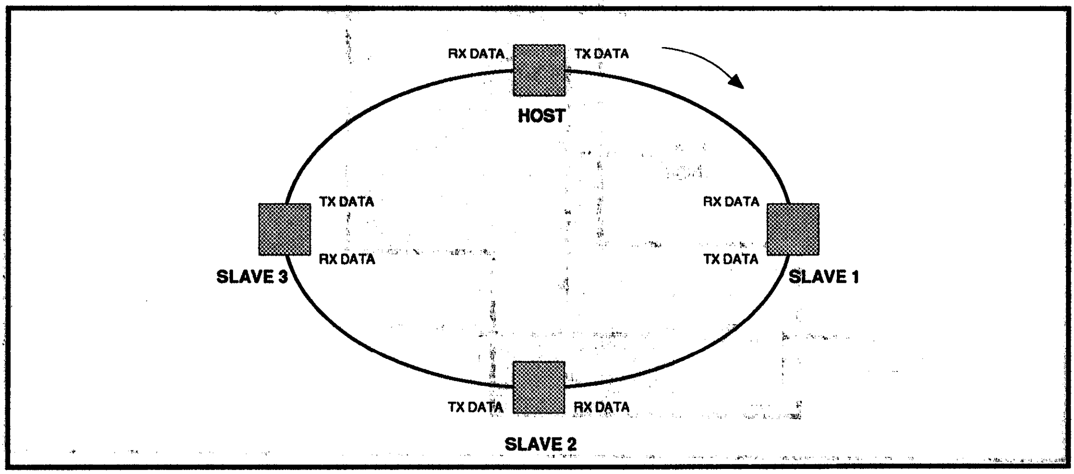


FIGURE 5: SDLC Loop Transmission

SDLC AND EOP FLAGS (continued)

Using this method of flow control, the host controller can modulate the use of the network by any slave controller. If data is being received from an upstream controller, the host may receive only a maximum of seven packets of data from a slave. This allows new EOP flags to make their way to the receivers of the downstream slave controllers. These controllers may place data on the network with the destination to the host controller, thereby using the EOP flag and changing the EOP flag to an SDLC flag. When the host controller senses more than one contiguous EOP flag in its receiver, the host controller can determine that all slaves have had an opportunity to utilize the communication channel. The host controller may then acknowledge the oldest frame, or all frames, from a slave controller, allowing the slave controller to transmit more data to the host controller.

The slave controller software is very simple. The controller software consists of RAM buffer routines to store data in RAM, which will be later transmitted, and a very simple controller device driver to control the 650. The 650 does most of the protocol work for the microprocessor.

DATA FLOW THROUGH THE 650

Data to be transmitted is read by the microprocessor from the 650 through the 16-byte FIFO in the 550 from the B channel of the synchronous controller. This data is transferred to RAM for storage. When the RAM storage is full, the microprocessor no longer reads data from the 550 FIFO, causing the host processor to wait. When a 256-byte packet of data is formed in the storage RAM, the controller waits for a valid EOP flag. The controller will also send a packet of less than 256 bytes when a receive FIFO time-out occurs, indicating that the host has no more data to transmit. When a valid EOP is indicated by the 650 to the microprocessor, the microprocessor adds a destination address byte, a source byte, a control byte and then data is transferred to the three-byte transmit FIFO within the 650 synchronous controller.

The microprocessor control software keeps a copy of the data received from the host until a message is received from the host controller that the data has been received correctly. When an acknowledgement packet is received from the host controller, the data is cleared from the directory in the slave controller.

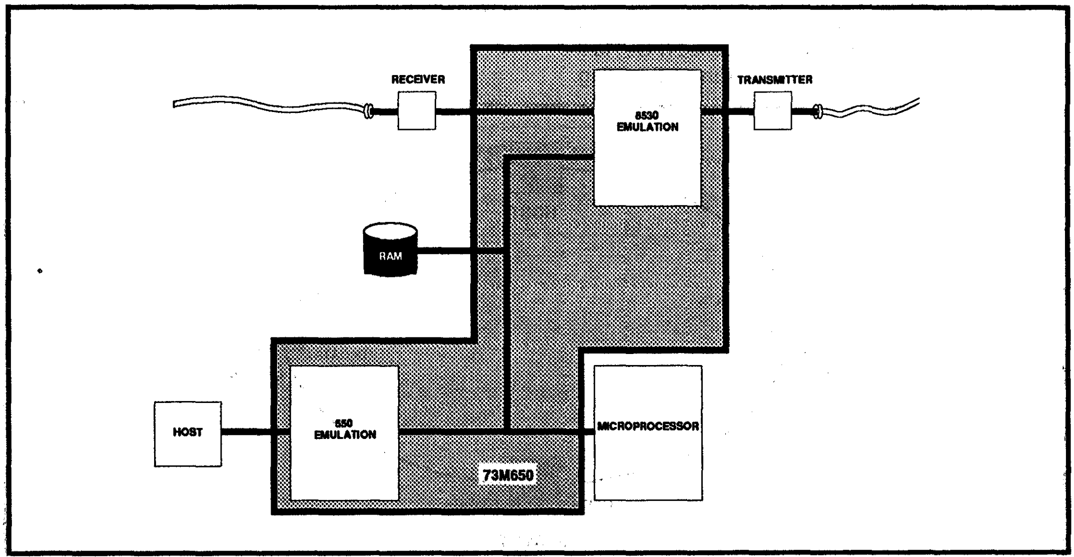


FIGURE 6: SSI 73M650 SDLC Loop

Using an SSI 73M650
Serial Packet Controller

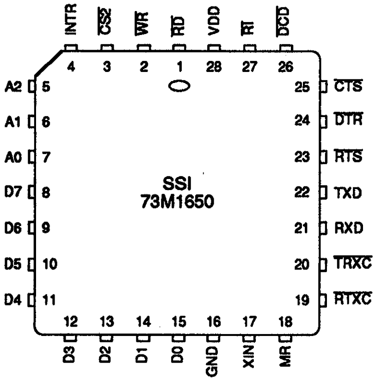
DATA FLOW THROUGH THE 650 (continued)

If an acknowledgement packet from the host controller indicates that the data frame was received corrupted, the packet and all newer packets waiting for acknowledgement from the host, are transmitted back to the host controller.

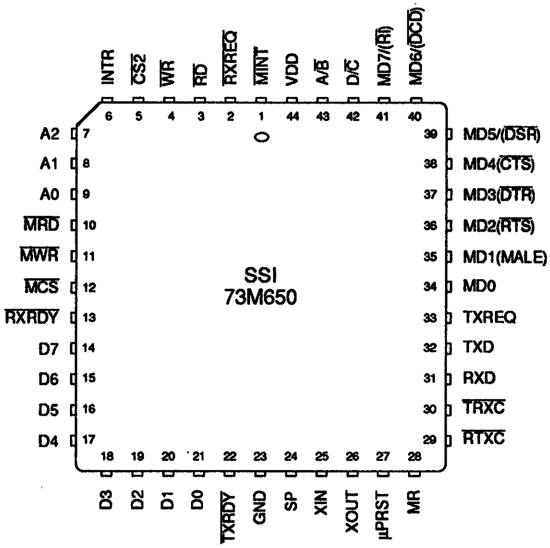
Using a fiber-optic network, with SDLC synchronous transmission protocol, and an SSI 73M650 Serial Packet Controller in each PC around the ring network, data can be transmitted at data rates of up to 1.2 Mbit/s. If external clock recovery circuitry is used, this data rate can even be higher.

For a complete SSI 73M650 data sheet contact your local Silicon Systems sales office.

PACKAGE PIN DESIGNATIONS
(Top View)



28-pin PLCC



44-pin PLCC

Notes:

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SSI 78Q8330
Ethernet Transceiver Demo Board
Application Note

January 1993

DESCRIPTION

The SSI 78Q8330 Demo Board is the evaluation vehicle for Silicon Systems' low power 78Q8330 Ethernet Transceiver IC. This board is designed to be connected to 10Base-2 thin coax cable that complies with the IEEE 802.3 standard for Local Area Networks. The board can be used as a transceiver unit and tied to a network interface board in through an AUI cable of up to 50 meters in length.

The SSI 78Q8330 works with thick coax cable (10Base-5) but different connection hardware must be used in such an application. Contact Silicon Systems' application engineering for more information.

Figure 2 shows a typical application with three systems already connected to the Ethernet 10Base-2 network. The Ethernet cable is then connected to the Demo Board at the BNC connector (BNC1). A 50Ω termination resistor must be placed at last station. The three pairs of differential signals (DI+/DI- data into the DTE, DO+/DO- data out of the DTE and CI+/CI- control into the DTE) are available at test points and at the 15-pin AUI cable. The AUI cable can be connected to a network interface board in the DTE. Please be sure that the network interface board is properly configured (either jumpers or software) to accept AUI (external) interface rather than an on-board (internal 10Base-2 or 10Base-T) interface.

FEATURES

- **Evaluation board for low power 10Base-2/ 10Base-5 transceiver**
- **Provides AUI port to connect to a network card**
- **Jumpers for easy change of heartbeat feature**
- **Test points to measure data to/from DTE using scopes**

BLOCK DIAGRAM

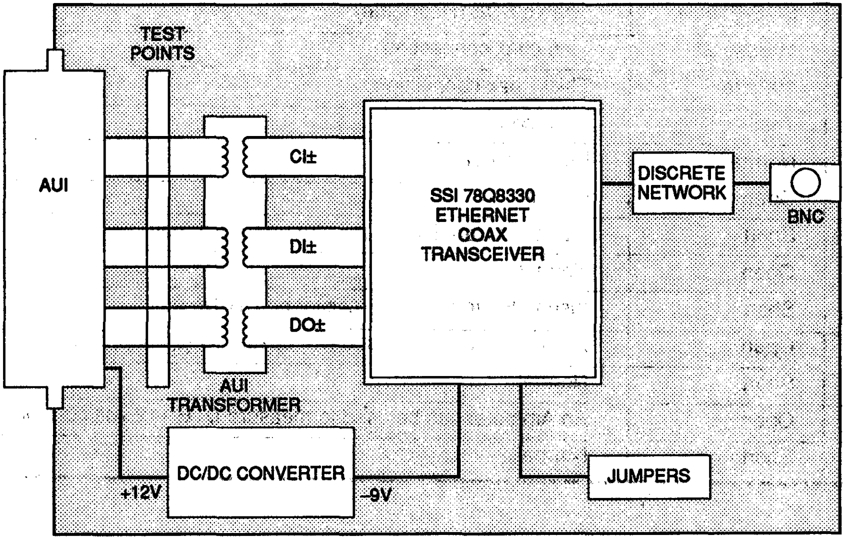


FIGURE 1: SSI 78Q8330 Demo Board Block Diagram

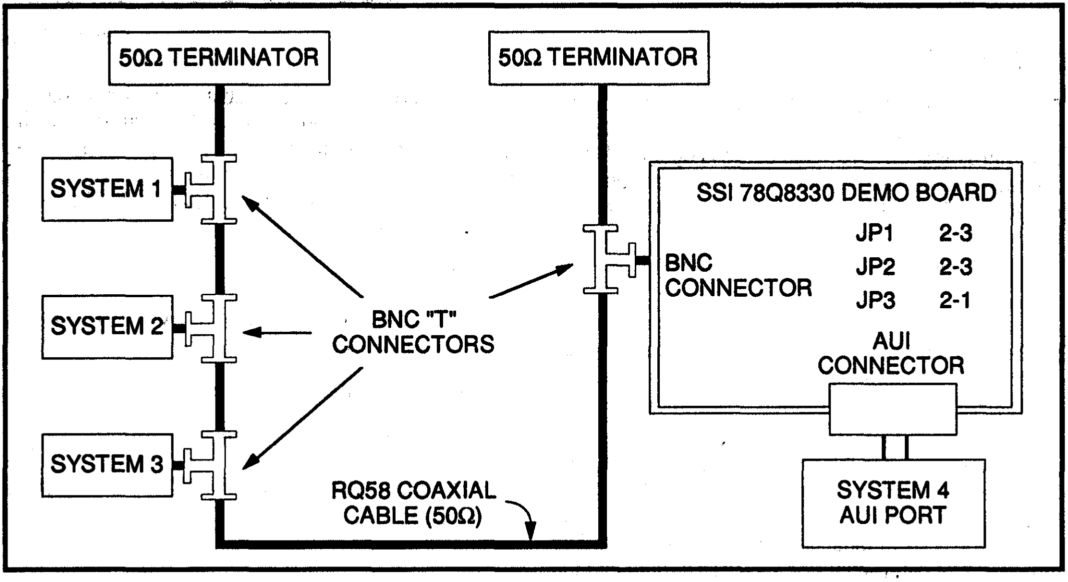


FIGURE 2: Silicon Systems' Typical LAN Connection Using Demo Board

TABLE 1: Jumper Description

JUMPER	CONNECTION	DESCRIPTION	
JP1	SQE-Disable	Disable SQE (Heartbeat)	Note 1
	SQE-Enable	Enable SQE (Heartbeat)	
JP2	10Base-2	Thin-coax connection	
	10Base-5	Thick coax connection	Note 2
JP3	Test	Test mode	Note 3
	Normal	Normal mode	
JP4	Open	Normal	Note 4
	Short	Insert 78Ω termination resistor on CI+/CI- pair	
JP5	Open	Normal	Note 4
	Short	Insert 78Ω termination resistor on DI+/DI- pair	
JP6	Open	An Ammeter can be used to measure IC -9V supply current	
	Short	Normal	
JP7	Open	An Ammeter can be used to measure DTE +12 volt current	
	Short	Normal	

TABLE 1: Jumper Description (continued)

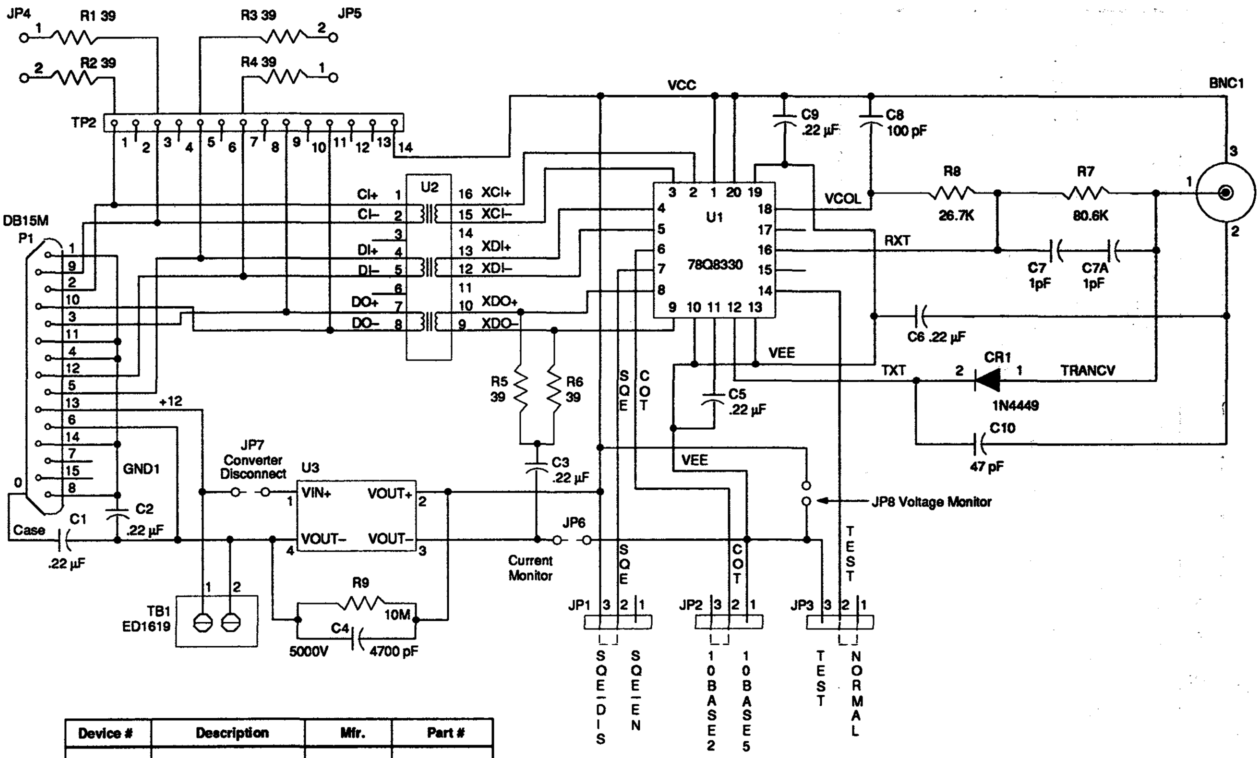
JUMPER	CONNECTION	DESCRIPTION
JP8	Open	This jumper is used to monitor IC -9V supply voltage. Top pin is -9V (VEE) and Bottom pin is GND (VCC)
	Short	ILLEGAL CONNECTION

NOTE: (1) SQE (heartbeat) inserts a 10 MHz signal on the CI+/CI- lines at the end of each transmission. The signal is used by the DTE for checking the transceiver. This signal is used by the DTE for checking the transceiver. This option must be disabled if the transceiver is connected to a repeater device.

(2) Contact Silicon Systems CIPD Application Engineering for more information on interface to thick coax (10Base-5).

(3) Place jumper in NORMAL mode.

(4) If on-board termination resistance is used, disconnect the AUI cable to avoid double termination.



Device #	Description	Mfr.	Part #
U2	AUI Transformers	Valor	LT6003
		TDK	TLA100-3E
U3	DC/DC Converter	Valor	PM6046
		TDK	CE-2094

FIGURE 3: Schematics of 78Q8330 Demo Board

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SSI 32F8001
Programmable Electronic Filter

Application Note

December 1992

INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space saving. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8001, cutoff frequency programmable from 9-27 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8001
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

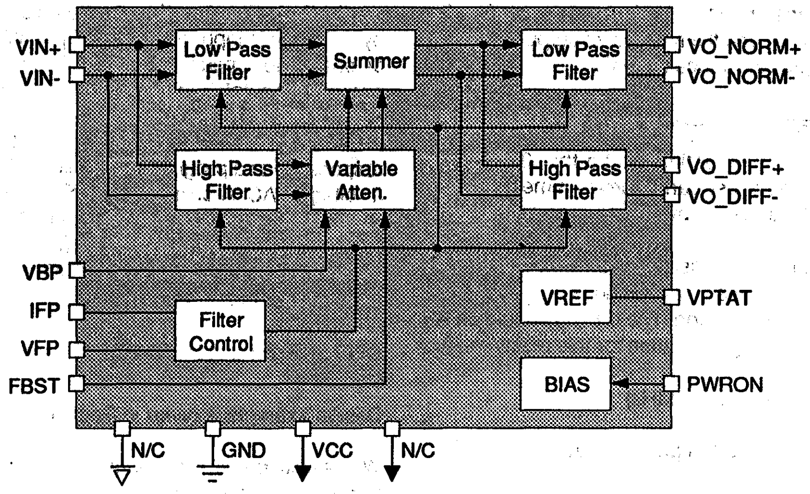
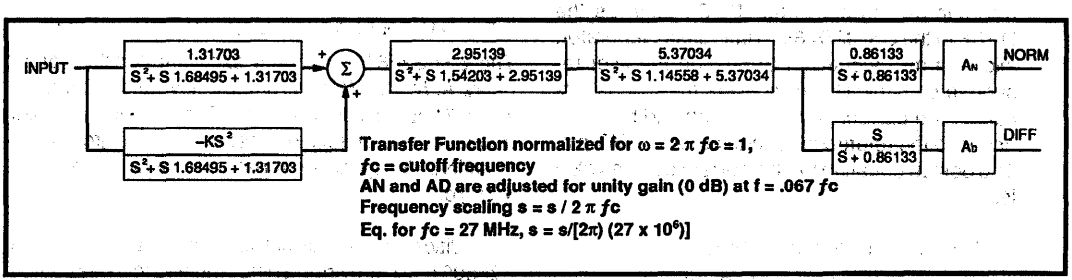


FIGURE 1: Block Diagram



Transfer Function normalized for $\omega = 2 \pi fc = 1$,
fc = cutoff frequency
AN and AD are adjusted for unity gain (0 dB) at f = .067 fc
Frequency scaling $s = s / 2 \pi fc$
Eq. for fc = 27 MHz, $s = s/[2\pi) (27 \times 10^6)]$

FIGURE 2: The SSI 32F8001 Transfer Function

CAUTION: Use handling procedures necessary for a static sensitive component.

1.0 DESCRIPTION

The SSI 32F8001 is a programmable 7-pole 0.05° equiripple linear phase low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8001 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As an equiripple linear phase type filter, the filter outputs exhibit constant group delay in the pass band and out to 1.75 fc. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8001 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. Typical differential input resistance is 4 kΩ.

1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3dB corner frequency with no boost, can be programmed between 9 - 27 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VPTAT and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 27 / fc (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. A current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy the current source DAC should be referenced to the reference voltage at the VPTAT pin. The design equation for this current source value is:

  IFP (mA) = 0.0222 x fc (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 1 kΩ resistor should be placed across the VPTAT and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the reference voltage at the VPTAT pin. The design equation for this current sink value is:

  IFP (mA) = 0.0222 x (27 - fc) (MHz)

  A design example is given in Section 4.

1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 13 dB at fc by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VPTAT pin for accuracy. The design equation for this control voltage is:

VBP = VPTAT x (10^(FB/20) - 1) / 3.46 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

1.3 OTHER FEATURES OF THE SSI 32F8001

The SSI 32F8001 features excellent constant group delay. At fc = 27 MHz, the group delay variation from 0.2 fc to fc is less than 0.5 ns. Furthermore, the high frequency boost function does not affect the group delay variation. Group delay variation is within ±3% out to 1.75 fc.

In addition to the normal low pass output, the SSI 32F8001 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8001 provides a reference voltage VPTAT for the DAC references. Because the internal filter control circuitry is referenced to VPTAT, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VPTAT.

The SSI 32F8001 can be switched into a sleep mode, dissipating less than 3 mW, by a TTL input at PWRON.

Two package options are available for the SSI 32F8001: 16-lead SOL and 16-lead SON. The small feature size of the 16-lead SON package offers significant board space saving.

2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8001 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize the signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

A programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8001 can be dynamically programmed through microprocessor control.

3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8001 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

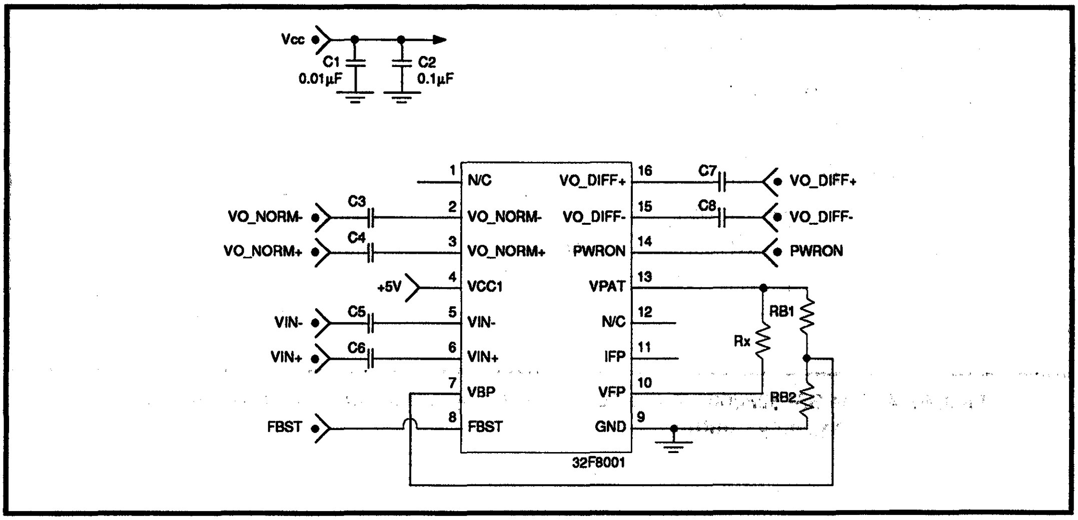


FIGURE 3: The 32F8001 Setup as a Fixed Response Filter

3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given *fc*, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 27 / *fc* (MHz)
  Voltage across Rx is 0.33 VPTAT. The current through Rx is 0.33 (VPTAT / Rx).
  Rx should be between 1 kΩ to 3 kΩ, i.e., *fc* between 9 MHz to 27 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 3.46 / (10^(FB / 20) - 1) - 1
- Total current drawn out of the VPTAT pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8001 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VPTAT. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8001 using an external current source DAC to control the filter's cutoff frequency.

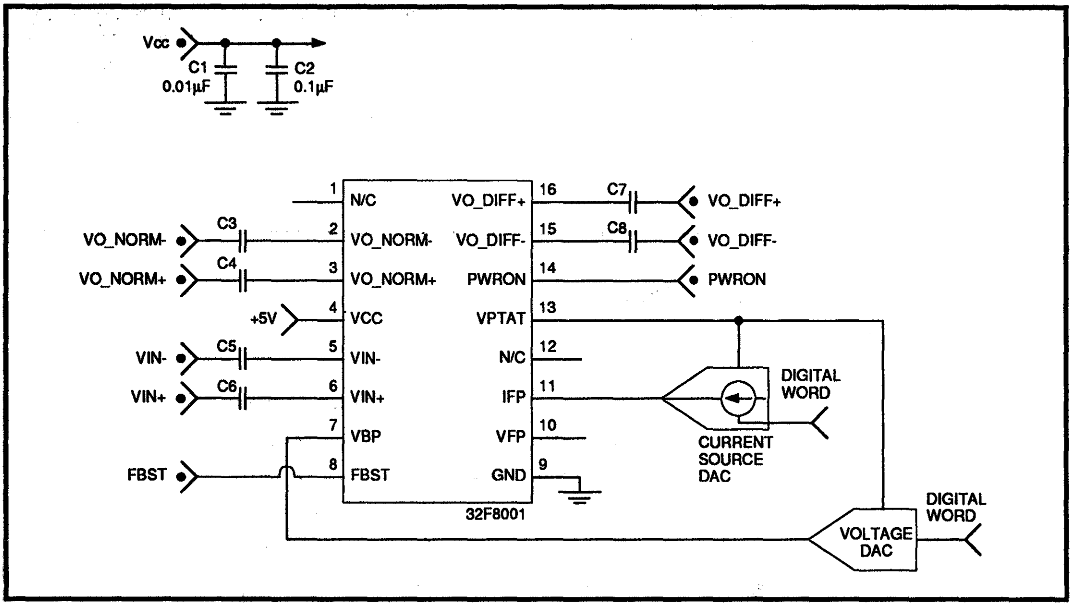


FIGURE 4: The SSI 32F8001 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control

Design guidelines for the SSI 32F8001:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VPTAT for accuracy.
- The reference bias current drawn from VR should be less than 2 mA.
- The current source output voltage compliance should be between 1.1V to 1.8V.
- The IFP current and the filter cutoff frequency are related as follows:

  $$fc \text{ (MHz)} = 45 \times \text{IFP (mA)} \times \frac{1.8}{\text{VPTAT}}$$

  IFP should be between 0.2 mA to 0.6 mA with VPTAT = 1.8V (at room temperature).
- The VBP voltage and the high frequency boost are related as follows:

  $$\text{FB} = 20 \times \log(3.46 \times \text{VBP} / \text{VPTAT} + 1) \text{ dB}$$

4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8001 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 1 kΩ between VPTAT and VFP.
- Both the current source DAC and the voltage DAC should reference to VPTAT for accuracy and temperature stability.
- The total current drawn from VPTAT should be less than 2mA. This includes the 0.6mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.4 mA.
- The current sink DAC output voltage compliance should be between 0.8V to 1.4V.
- The IFP current and the cutoff frequency are related as follows:

  $$\text{fc (MHz)} = 27 - 45 \times \text{IFP (mA)} \times \frac{\text{VPTAT}}{1.8}$$

  IFP should be between 0 mA to 0.4 mA.

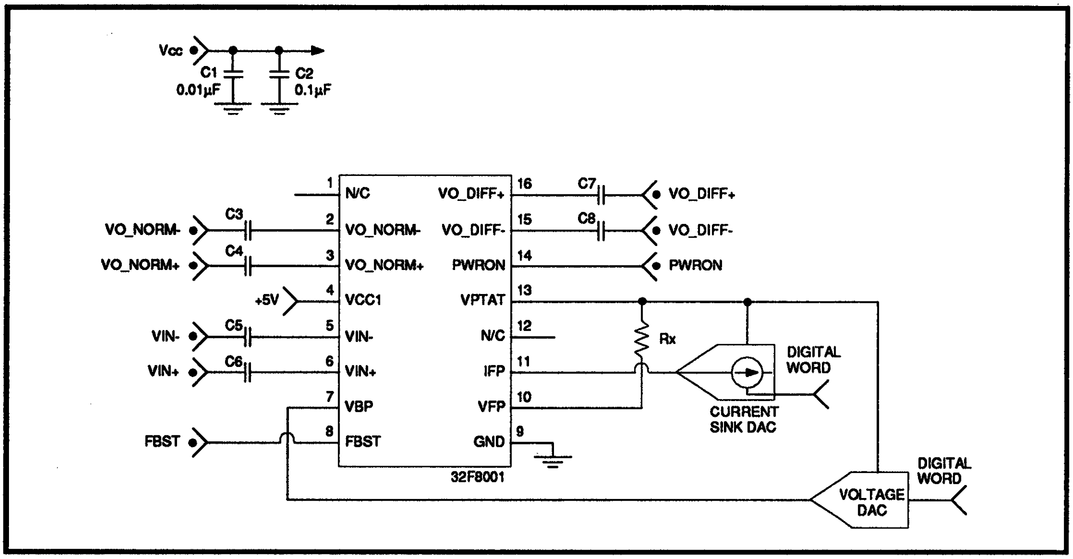


FIGURE 5: The SSI 32F8001 Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control

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SSI 32F8011
Programmable Electronic Filter
Application Note

December 1992

INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space saving. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8011, cutoff frequency programmable from 5 - 13 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8011
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

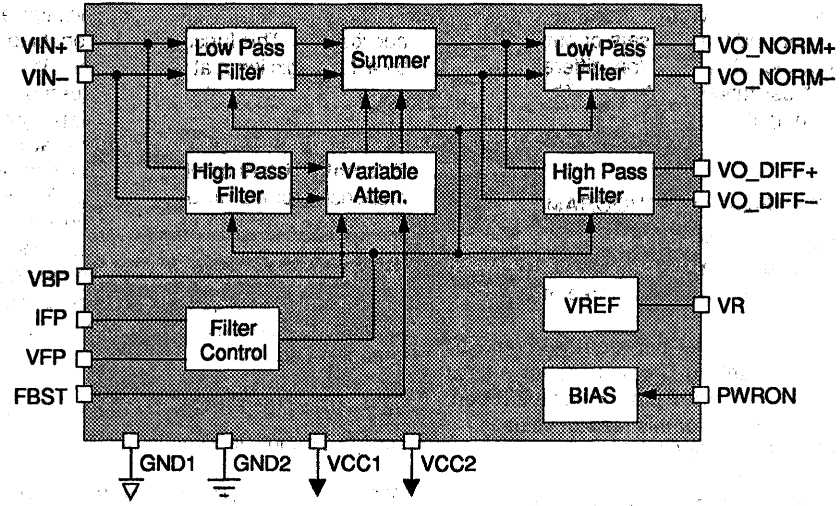
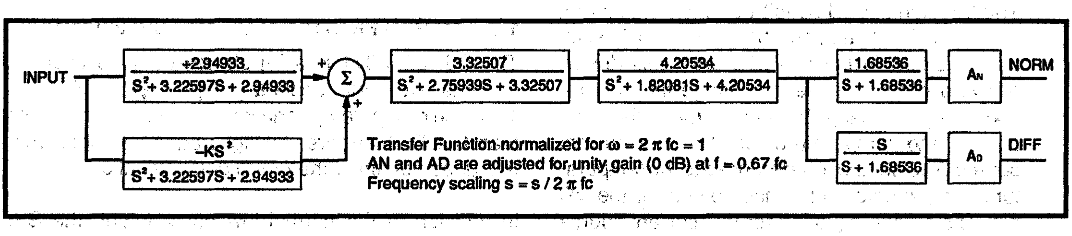


FIGURE 1: Block Diagram



Transfer Function normalized for $\omega = 2\pi fc = 1$
AN and AD are adjusted for unity gain (0 dB) at f = 0.67 fc
Frequency scaling $s = s / 2\pi fc$

FIGURE 2: The SSI 32F8011 Transfer Function

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8011
Programmable Electronic Filter

Application Note

1.0 DESCRIPTION

The SSI 32F8011 is a programmable 7-pole Bessel low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8011 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a Bessel type filter, the filter outputs exhibit constant group delay in the pass band. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8011 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is 1.5 Vpp differential, with differential input resistance 4 kΩ typical. The minimum recommended output load is 1 kΩ differential, AC coupled.

1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3dB corner frequency with no boost, can be programmed between 5 - 13 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VR and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 11.92 / fc (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. With a current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661, this design allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current source DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current source value is:

  IFP (mA) = 0.0615 x fc (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 917Ω resistor should be placed across the VR and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current sink value is:

  IFP (mA) = 0.0615 x (13 - fc) (MHz)

  A design example is given in Section 4.

1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 9 dB at *fc* by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability. The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

1.3 OTHER FEATURES OF THE SSI 32F8011

The SSI 32F8011 is a 7-pole Bessel type filter. It features excellent constant group delay. At *fc* = 13 MHz, the group delay variation from 0.2 fc to fc is less than 1ns. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8011 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

1.3 OTHER FEATURES OF THE SSI 32F8011 (continued)

The SSI 32F8011 provides a temperature compensated reference voltage, VR, for the DAC references. Because the internal filter control circuitry is referenced to VR, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VR.

The SSI 32F8011 can be switched into a sleep mode, dissipating only 60 mW, by a TTL input at PWRON.

Two package options are available for the SSI 32F8011: 16-lead SOL and 16-lead SON. The small feature size of the 16-pin SON package offers significant board space saving.

2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8011 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

Programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8011 can be dynamically programmed through microprocessor control.

3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8011 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

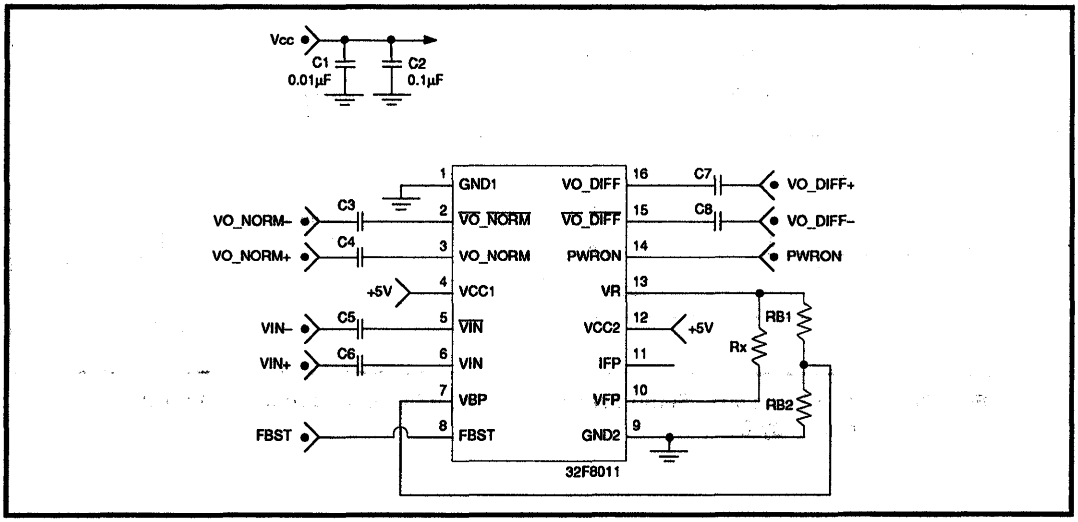


FIGURE 3: The 32F8011 Setup as a Fixed Response Filter

3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given fc, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 11.92 / fc (MHz)
  Voltage across Rx is 0.33 VR. The current through Rx is 0.33 (VR / Rx).
  Rx should be between 917 Ω to 2.38 kΩ, i.e., fc between 5 MHz to 13 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 1.884 / (10^(FB / 20) - 1) - 1
- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8011 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8011 using an external current source DAC to control the filter's cutoff frequency.

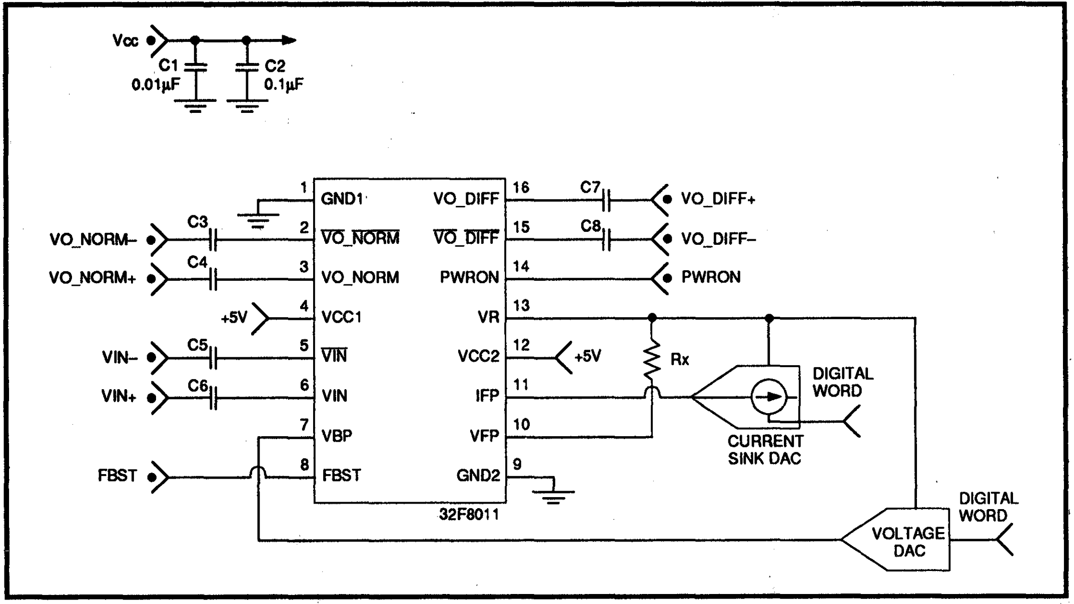


FIGURE 4: The SSI 32F8011 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC (continued)

Some design guidelines:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The reference bias current drawn from VR should be less than 2 mA.
- The current source output voltage compliance should be > 2.0 V.
- The IFP current and the filter cutoff frequency are related as follows:

  $$\text{fc (MHz)} = 16.25 \text{ x IFP (mA) x} \frac{VR}{2.2}$$

  IFP should be between 0.31 mA to 0.8 mA with VR = 2.2V.
- The VBP voltage and the high frequency boost are related as follows:

  FB = 20 x log (1.884 x VBP / VR + 1) dB

4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8011 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 917Ω between VR and VFP.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The total current drawn from VR should be less than 2mA. This includes the 0.8mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.2 mA.
- The current sink DAC output voltage compliance should be between 0.75V to 1.2V.
- The IFP current and the cutoff frequency are related as follows:

  $$\text{fc (MHz)} = 13 - 16.25 \text{ x IFP (mA) x} \frac{VR}{2.2}$$

  IFP should be between 0 mA to 0.49 mA.

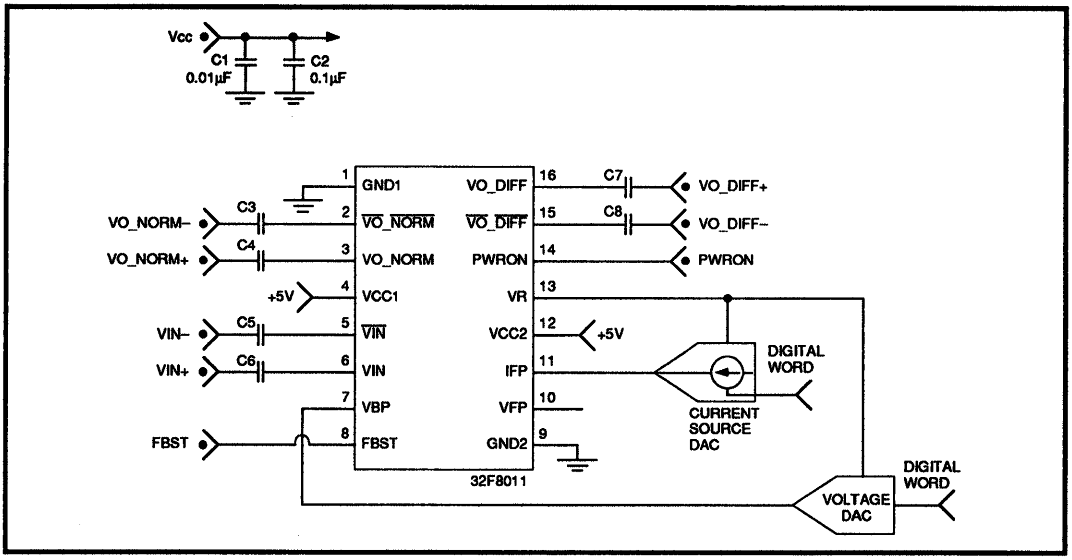


FIGURE 5: The SSI 32F8011 Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control

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SSI 32F8020A
Programmable Electronic Filter
Application Note

October 1992

INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space savings. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8020A, cutoff frequency programmable from 1.5 - 8 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8020A
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

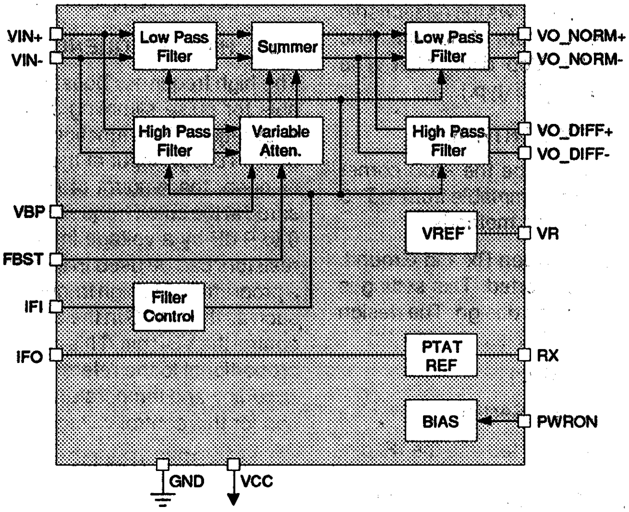
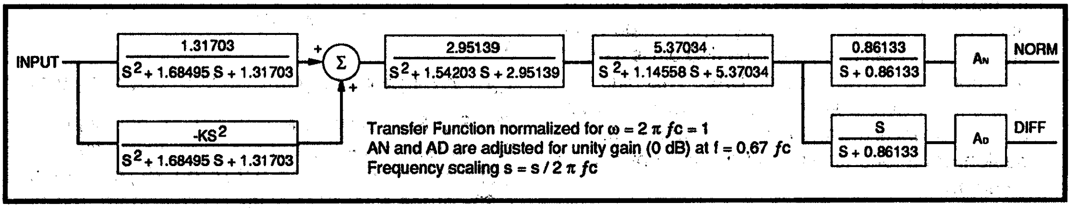


FIGURE 1: Block Diagram



Transfer Function normalized for ω = 2 π fc = 1
AN and AD are adjusted for unity gain (0 dB) at f = 0.67 fc
Frequency scaling s = s / 2 π fc

FIGURE 2: The SSI 32F8020A Transfer Function

SSI 32F8020A
Programmable Electronic Filter

Application Note

1.0 DESCRIPTION

The SSI 32F8020A is a programmable 7-pole 0.05° equiripple low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8020A cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a 0.05° equiripple type filter, the filter outputs exhibit constant group delay beyond its cutoff frequency. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8020A are differential signals, requiring external ac coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is 2.0 Vpp differential. The differential input resistance is 4 kΩ (typ.).

1.1 CUTOFF FREQUENCY CONTROL

The cutoff frequency, defined to be the -3dB corner frequency with no boost, is programmable from 1.5 - 8 MHz. It can be set by one of three methods:

1) A resistor is connected between Rx and Ground. The IFO and IFI pins are shorted. This setting is only used for a fixed response design. The design equation for this resistor value is:

   $$\text{Rx (k}\Omega\text{)} = 10.00 / fc \text{ (MHz)}$$

   A design example is given in Section 3.

2) A current source input can be fed into the IFI pin. With a current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, this design allows a microcontroller to change the filter response dynamically. A resistor from Rx to Ground is needed to establish a bias current on the IFO pin. To achieve the highest accuracy and temperature stability, this bias current on the IFO pin is used to reference the current source DAC. This bias current should be set such that the maximum DAC output current is 0.6 mA at room temperature. The design equations for Rx and the current source value are:

   $$\text{Rx (k}\Omega\text{)} = 0.75 / \text{IFO (mA) at T} = 27^{\circ}\text{C}$$

   $$\text{IFI (mA)} = 0.075 \times fc \text{ (MHz)}$$

   A design example is given in Section 4.

3) A current sink input can be fed into the IFI pin. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the proportional to absolute temperature voltage at the Rx pin, nominally at 750 mV. The DAC maximum sinking current should be at least 0.49 mA. A resistor from Rx to Ground is needed. The total current drawn from the Rx pin needs to be 0.6 mA at room temperature. The IFO and IFI pins are shorted. The design equations for Rx and this current sink value are:

   $$\text{Rx (k}\Omega\text{)} = 0.75 / (0.6 - I_{\text{DAC Bias}}) \text{ (mA)}$$

   $$\text{IFI (mA)} = 0.60 - 0.075 \times fc \text{ (MHz)}$$

   A design example is given in Section 4.

1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 9 dB by a voltage input at the VBP pin. External resistors can be used in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability. The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884

where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is also wider.

1.3 OTHER FEATURES OF THE SSI 32F8020A

The SSI 32F8020A is a 7-pole 0.05° equiripple type filter. It features excellent constant group delay. The group delay variation from 0.2 *fc* to 1.75 *fc* is less than ± 2% of the total filter delay. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8020A also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8020A provides a temperature compensated reference voltage, VR, and a proportional to absolute temperature voltage, Rx, for the DAC references. The filter cutoff frequency should be referenced to the current at the Rx pin. The high frequency boost control should be referenced to the voltage at the VR pin.

The SSI 32F8020A can be switched into a sleep mode, dissipating less than 2.5 mW, by a TTL low level input at the PWRON pin.

Three package options are available for the SSI 32F8020A: 16-pin DIP, 16-pin SOL and 16-pin SON. The small feature size of the 16-pin SON package offers significant board space saving.

2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8020A offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculations. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

A programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8020A can be dynamically programmed through microprocessor control.

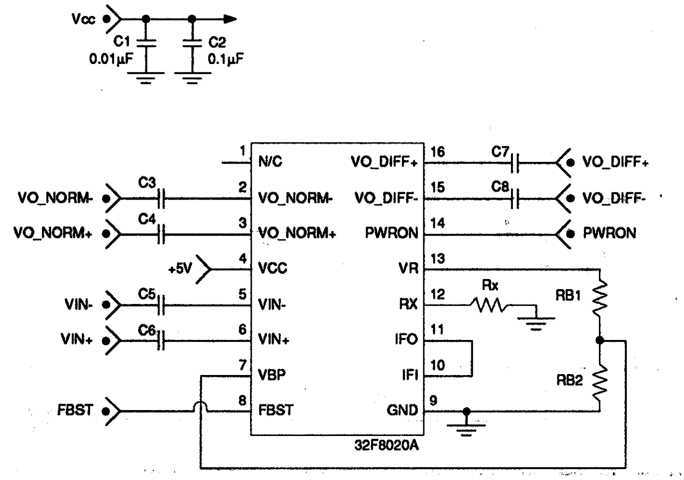


FIGURE 3: The 32F8020A Setup as a Fixed Response Filter

3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8020A as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

Given *fc*, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.

  Rx (kΩ) = 10.00 / *fc* (MHz)

  Voltage across Rx is 0.75V, and is proportional to the absolute temperature.

  Rx should be between 1.25 kΩ to 6.67 kΩ, i.e., *fc* between 1.5 MHz to 8 MHz.
- RB1/RB2 sets FB, and can be determined as follows:

  RB1 / RB2 = 1.884 / (10^(FB / 20) - 1) - 1
- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFO and IFI pins are shorted together.

4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8020A as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8020 using an external current source DAC to control the filter's cutoff frequency.

Some design guidelines:

- The current source DAC should be referenced to the IFO current. The voltage DAC should reference to VR.
- The reference bias current drawn from VR should be less than 2 mA.
- The IFO current biases the current source DAC for 0.6 mA maximum output at room temperature.

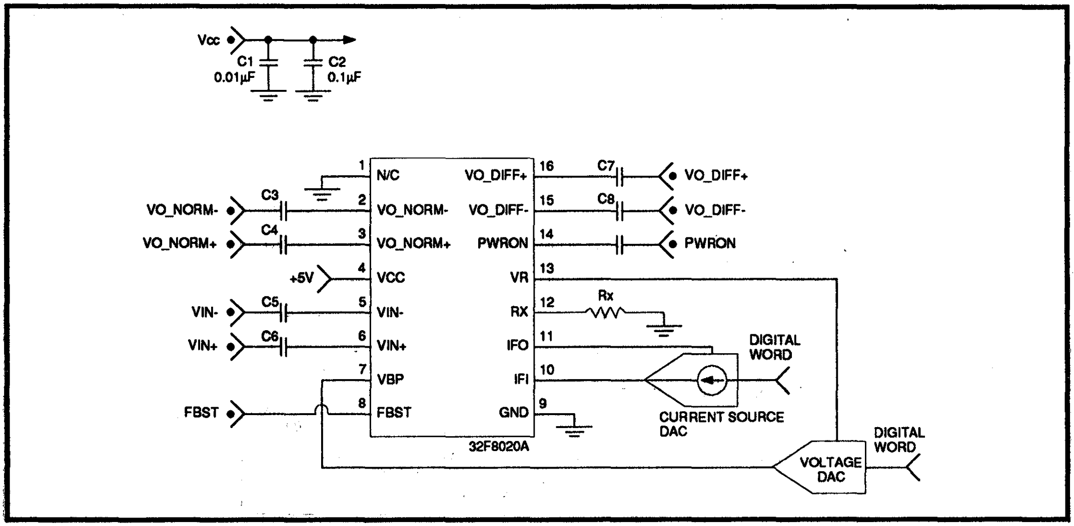


FIGURE 4: The SSI 32F8020A Setup Schematic Using a Current Source DAC for Cutoff Frequency Control

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC (continued)

- The Rx resistor determines the IFO current.

  $Rx\ (k\Omega) = 0.75\ /\ I_{DAC\ Bias}\ (mA)$
- The current source output voltage compliance should be between 0 to 2.5V.
- The IFI current and the filter cutoff frequency are related as follows:

  $fc\ (MHz) = 13.33 \times IFI\ (mA)$

  IFI should be between 0.11 mA to 0.6 mA at room temperature.
- The VBP voltage and the high frequency boost are related as follows:

  $FB = 20 \times \log(1.884 \times VBP\ /\ VR + 1)\ dB$

4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8020 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- The current sink DAC should reference to the voltage at the Rx pin.

  The voltage DAC should reference to VR.
- The IFO and IFI pins are shorted.
- The total current drawn from VR should be less than 2 mA.

  The total current drawn from the Rx pin should be 0.6 mA.

  $Rx\ (k\Omega) = 0.75\ /\ (\ 0.6 - I_{DAC\ Bias}\ )\ (mA)$
- The current sink DAC output voltage compliance should be between 0 to 2.5V.
- The IFI current and the cutoff frequency are related as follows:

  $fc\ (MHz) = 8 - 13.33 \times IFI\ (mA)$

  IFI should be between 0 mA to 0.49 mA.

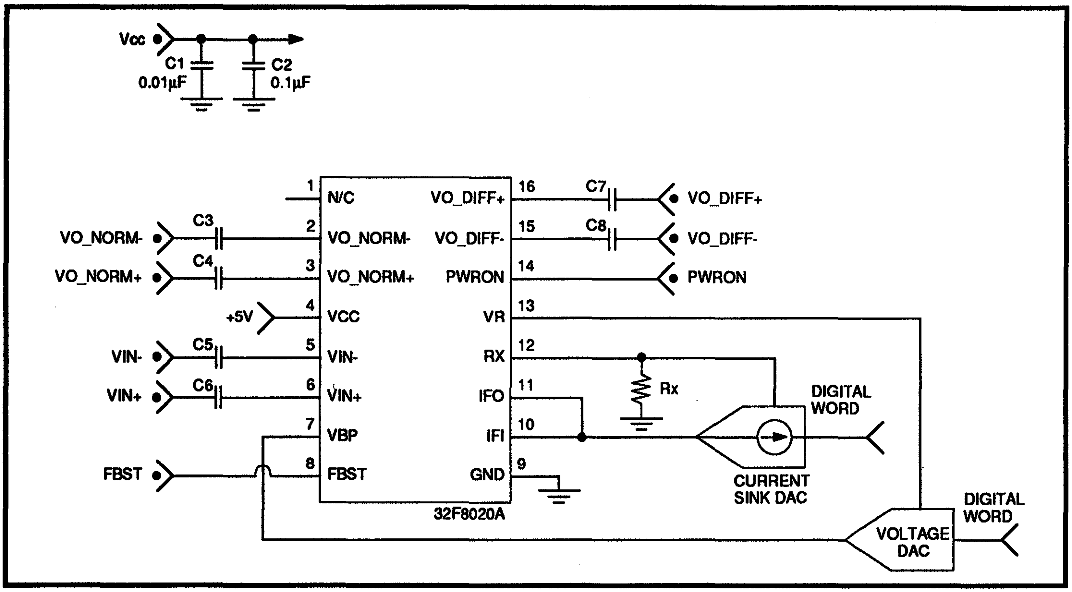


FIGURE 5: The SSI 32F8020A Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control

Notes:

silicon systems®
A TDK Group Company

SSI 32F8030
Programmable Electronic Filter

Application Note

December 1992

INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space savings. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8030, cutoff frequency programmable from 250 kHz - 2.5 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8030
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

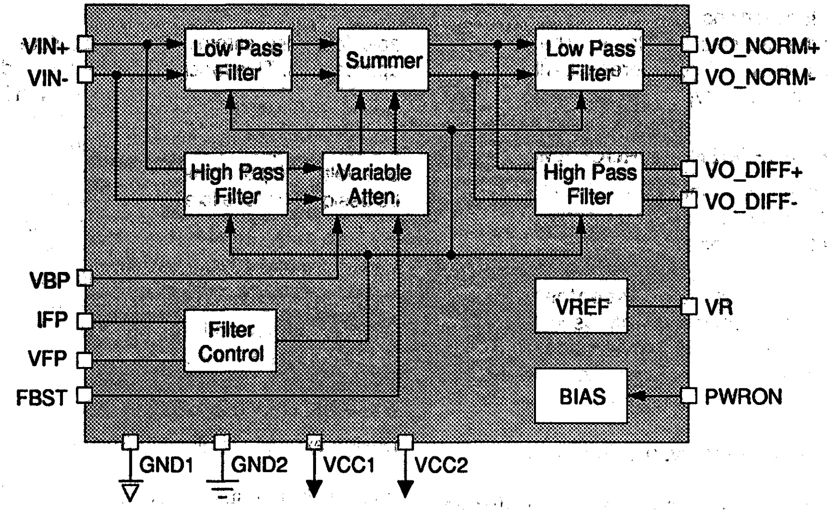
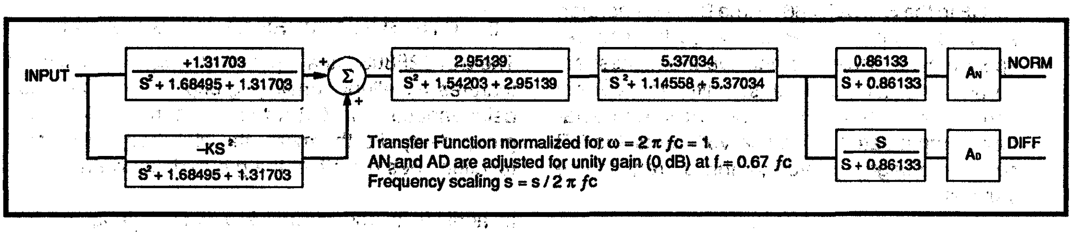


FIGURE 1: Block Diagram



Transfer Function normalized for $\omega = 2\pi fc = 1$
AN and AD are adjusted for unity gain (0 dB) at $f = 0.67\ fc$
Frequency scaling $s = s / 2\pi fc$

FIGURE 2: The SSI 32F8030 Transfer Function

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8030
Programmable Electronic Filter

1.0 DESCRIPTION

The SSI 32F8030 is a programmable 7-pole 0.05° Equiripple low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8030 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a 0.05° Equiripple type filter, the filter outputs exhibit constant group delay beyond the pass band. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8030 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is at least 1.0 Vpp differential, with differential input resistance 4 kΩ typical.

1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3 dB corner frequency with no boost, can be programmed between 250 kHz - 2.5 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VR and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 2.292 / fc (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. A current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current source DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current source value is:

  IFP (mA) = 0.320 x fc (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 917Ω resistor should be placed across the VR and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current sink value is:

  IFP (mA) = 0.320 x (2.5 - fc) (MHz)

  A design example is given in Section 4.

1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost measured at the cutoff frequency can be programmed from 0 to 9 dB by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability.The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

1.3 OTHER FEATURES OF THE SSI 32F8030

The SSI 32F8030 is a 7-pole 0.05° Equiripple filter. It features excellent constant group delay. The group delay variation from 0.2 fc to fc is less than 2% of mean group delay. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8030 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8030 provides a temperature compensated reference voltage, VR, for the DAC references. Because the internal filter control circuitry is referenced to VR, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VR.

The SSI 32F8030 can be switched into a sleep mode, dissipating < 5 mW, by a TTL input at PWRON.

Three package options are available for the SSI 32F8030: 16-pin DIP, 16-pin SOL and 16-pin SON. The small feature size of the 16-pin SON package offers significant board space saving.

2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8030 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize the signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

Programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8030 can be dynamically programmed through a microprocessor control.

3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8030 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

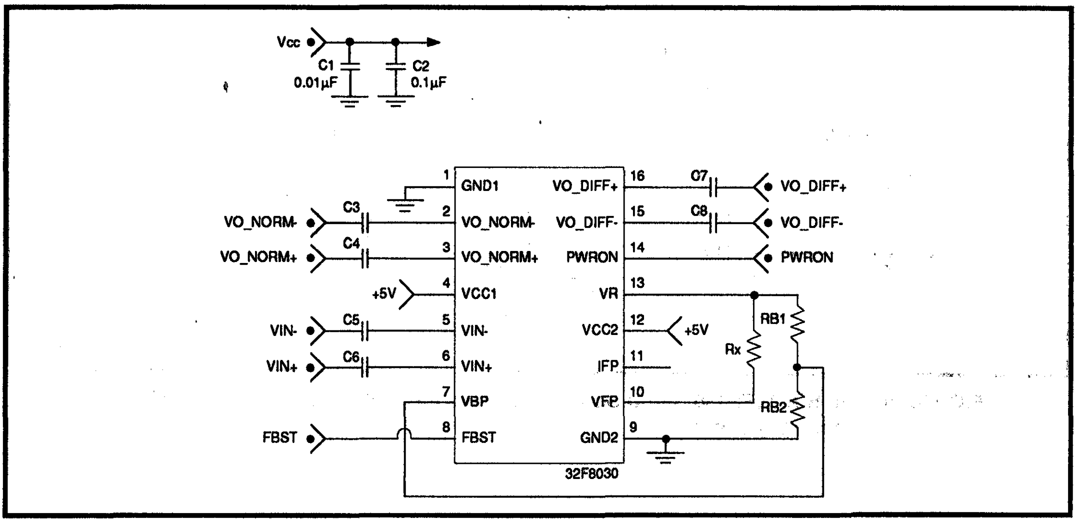


FIGURE 3: The 32F8030 Setup as a Fixed Response Filter

3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given fc, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 2.292 / fc (MHz)
  Voltage across Rx is 0.33 VR. The current through Rx is 0.33 (VR / Rx).
  Rx should be between 917Ω to 9.17 kΩ, i.e., fc between 250 kHz to 2.5 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 1.884 / (10^(FB / 20) - 1) - 1
- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8030 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8030 using an external current source DAC to control the filter's cutoff frequency.

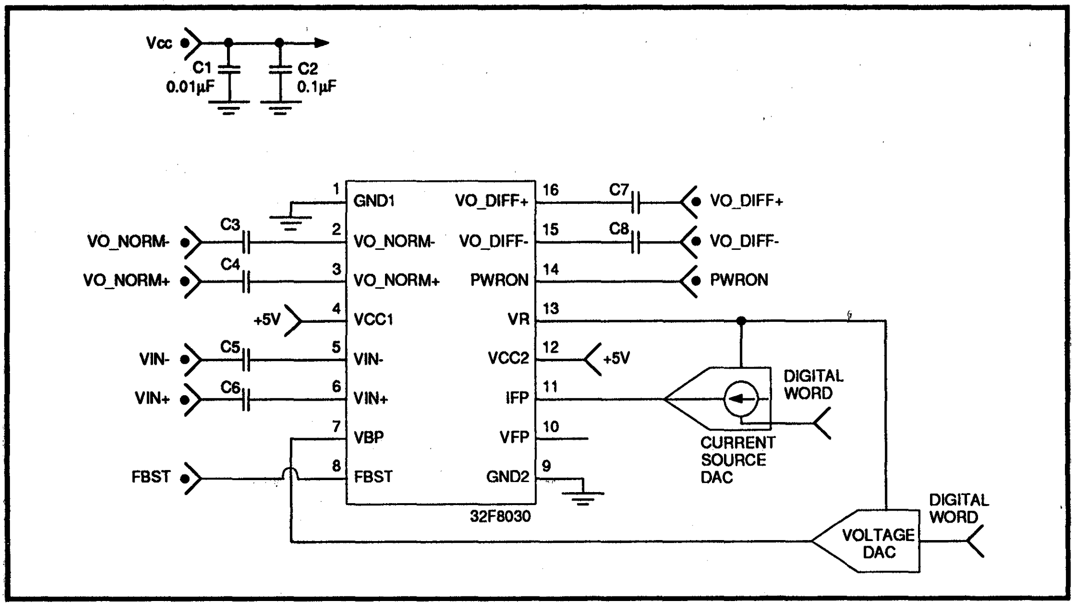


FIGURE 4: The SSI 32F8030 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control

Design guidelines for the SSI 32F8030:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The reference bias current drawn from VR should be less than 2 mA.
- The current source output voltage compliance should be between 1.3V to 2.1 V.
- The IFP current and the filter cutoff frequency are related as follows:

  fc (MHz) = 3.125 x IFP (mA)

  IFP should be between 0.08 mA to 0.8 mA.
- The VBP voltage and the high frequency boost are related as follows:

  FB = 20 x log (1.884 x VBP / VR + 1) dB

4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8030 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 917Ω between VR and VFP.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The total current drawn from VR should be less than 2 mA. This includes the 0.8 mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.2 mA.
- The current sink DAC output voltage compliance should be between 0.85V to 1.6V.
- The IFP current and the cutoff frequency are related as follows:

  fc (MHz) = 2.5 - 3.125 x IFP (mA)

  IFP should be between 0 mA to 0.72 mA.

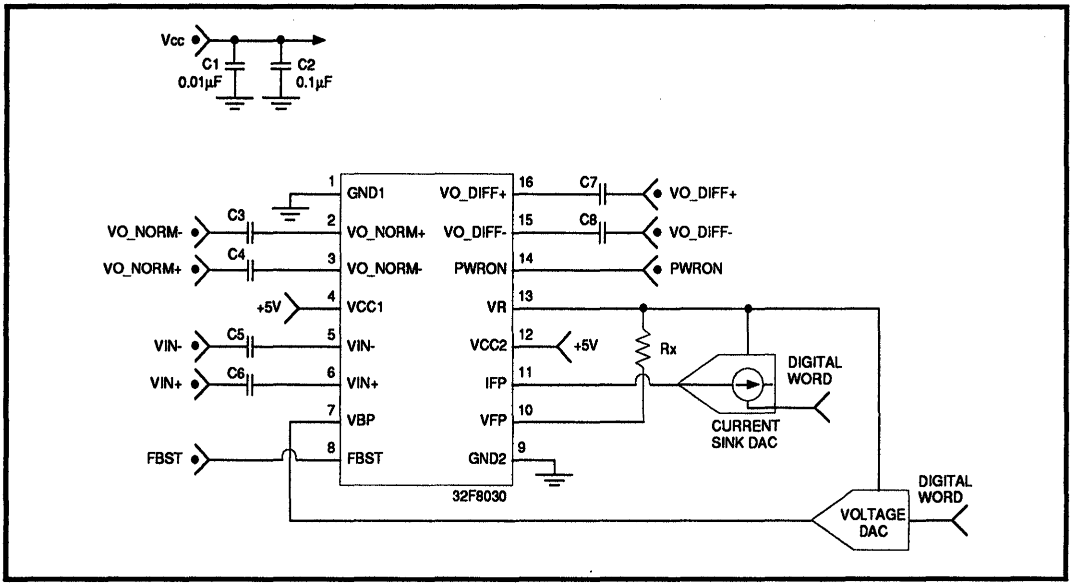


FIGURE 5: The SSI 32F8030 Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control

Notes:

Glossary

A

ACK - "Acknowledge" character. A transmission control character transmitted by a station as an affirmative response to the station with which a connection has been set up. An acknowledge character may also be used as an accuracy control character.

ACOUSTIC COUPLER - A type of low-speed modem interface frequently used with portable terminals. It sends and receives data using a conventional telephone handset and does not require an electrical connection to the line.

ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION (ADPCM) - An encoding technique, standardized by the CCITT, that allows an analog voice conversation to be carried within a 32K bps digital channel. Three or four bits are used to describe each sample, which represents the difference between two adjacent samples. Sampling is done 8,000 times per second.

ALGORITHM - A prescribed set of well-defined rules for the solution of a problem in a finite number of steps, e.g., A full statement of an arithmetic procedure for evaluating sine x to a stated precision.

AMPLITUDE - Magnitude or size. In waveforms or signals occurring in a data transmission, a complete definition of the waveform can be made if the voltage level is known at all times. In this case, the voltage level is called the amplitude.

AMPLITUDE MODULATION - Method of modifying the amplitude of a sine wave signal in order to encode information.

ANALOG LOOPBACK - A technique used for testing transmission equipment that isolates faults to the analog signal receiving or transmitting circuitry. Basically, where a device, such as a modem, echoes back a received (test) signal that is then compared with the original signal.

ANALOG SIGNAL - Signal in the form of a continuously varying physical quantity such as voltage, which reflects variations in some quantity.

ANSI - American National Standards Institute. A highly active group affiliated with the International Standards Organization (ISO) that prepares and establishes standards for transmission codes (e.g., ASCII), protocols (e.g., ADCCP), media (tape and diskette), and high level languages (e.g., Fortran and Cobol), among other things.

ANSWERBACK - A reply message from a terminal that verifies that the correct terminal has been reached and that it is operational.

APPLICATION LAYER - The top of the seven-layer OSI model, generally regarded as offering an interface to, and largely defined by, the network user; in IBM's SNA, the end-user layer.

ASCII - American Standard Code for Information Interchange. A 7-bit binary code that defines 128 standard characters for use in data communications.

ASYNCHRONOUS - Occurring without a regular or predictable time relationship to a specified event, e.g., The transmission of characters one at a time as they are keyed. Contrast with synchronous.

ASYNCHRONOUS TRANSMISSION - Transmission in which each information character, or sometimes each word or small block, is individually synchronized, usually by the use of start and stop elements. Also called start-stop or character asynchronous transmission.

ATTENUATION - A decrease in the power of a current, voltage, or power of a received signal in transmission between points because of loss through lines, equipment or other transmission devices. Usually measured in decibels.

AUTO-ANSWER - Automatic answering; the capability of a terminal, modem, computer, or a similar device to respond to an incoming call on a dial-up telephone line, and to establish a data connection with a remote device without operator intervention.

AUTOBAUD - The generally used term for automatically detecting the bit rate of a start/stop (character asynchronous) communication format by measuring the length of the start bit of the first character transmitted. Some modems extend this to additionally determine the parity in use by stipulating that the first two characters from the DTE should be "AT". The word autobaud comes from a popular misuse of baud rate to mean the same as bit rate.

AUTODIAL - Automatic dialing; the capability of a terminal, modem, computer, or a similar device to place a call over the switched telephone network, and establish a connection without operator intervention.

AUTOMATIC DIALER, OR AUTODIALER - Device which allows the user to dial preprogrammed numbers simply by pushing a single button.

B

BANDPASS FILTER - A circuit designed to allow a single band of frequencies to pass; neither of the cut-off frequencies can be zero or infinite.

BANDWIDTH - 1) The range of frequencies that can pass over a given circuit. The bandwidth determines the rate at which information can be transmitted through the circuit. The greater the bandwidth, the more information that can be sent through the circuit in a given amount of time. 2) Difference, expressed in hertz (Hz), between the highest and lowest frequencies of a transmission channel.

BASEBAND - Pertaining or referring to a signal in its original form and not changed by modulation. A baseband signal can be analog or digital.

BASEBAND SIGNALING - Transmission of a digital or analog signal at its original frequencies, i.e., a signal in its original form, not changed by modulation; can be an analog or digital signal.

BAUD - A measure of data rate, often misused to denote bits per second. A baud is equal to the number of discrete conditions or signal events per second. There is disagreement over the appropriate use of this word, since at speeds above 2400 bit/s, the baud rate does not always equal the data rate in bits per second.

BELLCORE - Bell Communications Research; organization established by the AT&T divestiture, representing and funded by the BOCs and RBOCs, for the purposes of establishing telephone network standards and interfaces; includes much of former Bell Labs.

BERT - Bit Error Rate Test. A test conducted by transmitting a known, pattern of bits (commonly 63, 511, or 2047 bits in length), comparing the pattern received with the pattern transmitted, and counting the number of bits received in error. Also see bit error rate. Contrast with BLERT.

BINARY CODE - Representation of quantities expressed in the base-2 number system.

BINARY SYNCHRONOUS COMMUNICATIONS - A half-duplex, character-oriented data communications protocol originated by IBM in 1964. It includes control characters and procedures for controlling the establishment of a valid connection and the transfer of data. Also called bisync and BSC. Although still enjoying widespread usage, it is being replaced by IBM's more efficient protocol, SDLC.

BIPOLAR - 1) The predominant signaling method used for digital transmission services, such as DDS and T1, in which the signal carrying the binary value successfully alternates between positive and negative polarities. Zero and one values are represented by the signal amplitude at either polarity, while no-value "spaces" are at zero amplitude. 2) A type of integrated circuit (IC or semiconductor) that uses NPN, PNP, and junction FET's as the primary active devices, as opposed to CMOS, which uses MOS FET's. See Alternate Mark Inversion.

BIT - The smallest unit of information used in data processing. It is a contraction of the words "binary digit."

BIT ERROR RATE (BER) - In data communications testing, the ratio between the total number of bits transmitted in a given message and the number of bits in that message received in error; a measure of the quality of a data transmission.

BITS PER SECOND (BIT/S) - Basic unit of measure for serial data transmission capacity; Kbit/s, or kilobits, for thousands of bits per second; Mbit/s, or megabit/s, for millions of bits per second, etc.

BOC - Bell Operating Company. One of 22 local telephone companies spun off from AT&T as a result of divestiture. The 22 operating companies are divided into seven regions and are held by seven RBHCs (Regional Bell Holding Company).

BROADBAND - Referring or pertaining to an analog circuit that provides more bandwidth than a voice grade telephone line, i.e., a circuit that operates at a frequency of 20 kHz or greater. Broadband channels are used for high-speed voice and data communications, radio and television broadcasting, some local area data networks, and many other services. Also called wideband.

BUFFER - A storage medium or device used for holding one or more blocks of data to compensate for a difference in rate of data flow, or time of occurrence of events, when transmitting data from one device to another.

BUS - 1) Physical transmission path or channel. Typically an electrical connection, with one or more conductors, wherein all attached devices receive all transmissions at the same time. Local network topology, such as used in Ethernet and the token bus, where all network nodes listen to all transmissions, selecting certain ones based on address identification. Involves some type of contention-control mechanism for accessing the bus transmission medium. In data communications, a network topology in which stations are arranged along a linear medium (e.g., a length of cable). 2) In computer architecture, a path over which information travels internally among various components of a system.

BYTE - Group of bits handled as a logical unit; usually 8.

C

CABLE - Assembly of one or more conductors within a protective sheath; constructed to allow the use of conductors separately or in groups.

CALL PROGRESS DETECTION (CPD) - A technique for monitoring the connection status during initiation of a telephone call by detecting presence and/or duty cycle of call progress signaling tones such as dial-tone or busy signals commonly used in the telephone network.

CALL PROGRESS TONES - Audible signals returned to the station user by the switching equipment to indicate the status of a call; dial tones and busy signals are common examples.

CCITT - Comite Consultatif International de Telephonie et de Telegraphie. Telegraph and Telephone Consultive Committee. An advisory committee to the International Telecommunications Union (ITU) whose recommendations covering telephony and telegraphy have international influence among telecommunications engineers, manufacturers, and administrators.

CENTRAL OFFICE (CO) - See Exchange

CHANNEL BANK - Equipment typically used in a telephone central office that performs multiplexing of lower speed, digital channels into a higher speed composite channel. The channel bank also detects and transmits signaling information for each channel, and transmits framing information so that time slots allocated to each channel can be identified by the receiver.

CHANNEL SERVICE UNIT (CSU) - A component of customer premises equipment (CPE) used to terminate a digital circuit, such as DDS or T1 at the customer site; performs certain line-conditioning functions, ensures network compliance per FCC rules and responds to loopback commands from central office; also, ensures proper ones density in transmitted bit stream and performs bipolar violation correction.

CHANNEL, VOICE GRADE - Channel suitable for transmission of speech, analog data, or facsimile, generally with a frequency range of about 300 to 3000 Hz.

CHARACTER - Letter, figure, number, punctuation, or other symbol contained in the message. In data communication, common characters are defined by 7- or 8-bit binary codes, such as ASCII.

CHIP - A commonly used term which refers to an integrated ciruit.

CIRCUIT, TWO-WIRE - A circuit formed by two conductors insulated from each other that can be used as either a one-way or two-way transmission path.

CLOCK - In logic or transmission, repetitive, precisely timed signal used to control a synchronous process.

CMOS - Complementary Metal-Oxide Semiconductor. A type of transistor, typicallly used in low-power integrated circuits.

COAXIAL CABLE - Cable consisting of an outer conductor surrounding an inner conductor, with a layer of insulating material in between. Such cable can carry a much higher bandwidth than a wire pair.

CPE - Customer Premises Equipment

CROSSPOINT - 1) Switching array element in an exchange that can be mechanical or electronic. 2) Two-state semiconductor switching device having a low transmission system impedance in one state and a very high one in the other.

CROSSTALK - Interference or an unwanted signal from one transmission circuit detected on another, usually an adjacent circuit.

CYCLIC REDUNDANCY CHECK (CRC) - A powerful error detection technique. Using a polynomial, a series of two 8-bit block check characters are generated that represent the entire block of data. The block check characters are incorporated into the transmission frame, then checked at the receiving end.

D

DATA COMMUNICATIONS EQUIPMENT (DCE) - Equipment that performs the functions required to connect data terminal equipment (DTE) to the data circuit. In a communications link, equipment that is either part of the network, an access-point to the network, a network node, or equipment at which a network circuit terminates; in the case of an RS-232C connection, the modem is usually regarded as DCE, while the user device is DTE, or data terminal equipment; in a CCITT X.25 connection, the network access and packet-switching node is viewed as the DCE.

DATA LINK - Any serial data communications transmission path, generally between two adjacent nodes or devices and without any intermediate switching nodes.

DATA SET - A synonym for modem used by AT&T and a few other vendors.

DATA SERVICE UNIT (DSU) - A device that replaces a modem on a Digital Data Service (DDS) line. The data service unit regenerates the digital signals for transmission over digital facilities.

DATA TERMINAL EQUIPMENT (DTE) - Equipment which is attached to a network to send or receive data, generally end-user devices, such as terminals and computers, that connect to DCE, which either generate or receive the data carried by the network; in RS-232C connections, designation as either DTE or DCE determines signaling role in handshaking; in a CCITT X.25 interface, the device or equipment that manages the interface at the user premises; see DCE.

dB - Decibel; unit for measuring relative strength of a signal parameter such as power, voltage, etc. The number of decibels is twenty times the logarithm (base 10) of the ratio of the power of two signals, or ratio of the power of one signal to a reference level.

dBm - Decibels relative to one milliwatt.

DDS - 1) Digital Data Service. A digital transmission service supporting speeds up to 56 Kbit/s. 2) Dataphone Digital Service. An AT&T leased line service offering digital transmission at speeds ranging from 2400 to 56 Kbit/s.

DELAY DISTORTION - The change in a signal from the transmitting end to the receiving end resulting from the tendency of some frequency components within a channel to take longer to be propagated than others.

DIAL-UP - The process of, or the equipment or facilities involved in, establishing a temporary connection via the switched telephone network.

DIAL TONE (DT) - Signal sent to an operator or subscriber indicating that the switch is ready to receive dial pulses.

DIGITAL - Referring to communications procedures, techniques, and equipment whereby information is encoded as either binary "1" or "0"; the representation of information in discrete binary form, discontinuous in time, as opposed to the analog representation of information in variable, but continuous, waveforms.

DIGITAL LOOPBACK - A technique for testing the digital processing circuitry of a communications device. It may be initiated locally, or remotely via a telecommunications circuit. The device being tested will echo back a received test message, after first decoding and then re-encoding it, the results of which are compared with the original message.

DIGITAL SIGNAL - Discrete or discontinuous signal; one whose various states are discrete intervals apart.

DIP - Dual-In-Line Package. Method of packaging electronic components for mounting on printed circuit boards.

DISTORTION - The modification of the waveform or shape of a signal caused by outside interference or by imperfections of the transmission system. Most forms of distortion are the result of the characteristics of the transmission system to the different frequency components.

DOTTING, DOUBLE DOTTING, PATTERN - The term "dotting" was coined by Bell to describe a data pattern consisting of alternate marks and spaces. The CCITT uses the full description of "alternating binary ones and zeros" on first needing this idea in a recommendation, but then abbreviate this to "reversals." By extrapolation, "double dotting" has come into use to refer to the data pattern termed "S1" which is used in V.22bis to indicate 2400 bit/s capability. The full description is "unscrambled double dibit 00 and 11 at 1200 bit/s for 100 ± 3 ms."

DS-1 - Digital Signal level 1; telephony term describing a digital transmission format in which 24 voice channels are multiplexed into one 1.544 Mbit/s (U.S.) T1 digital channel.

DS-3 - Digital Signal level 3; telephony term describing the 44.736 Mbit/s digital signal carried on a T3 facility.

DTMF - Dualtone Multifrequency (DTMF) - Basis for operation of most push button telephone sets. An in-band signalling technique in which a matrix combination of two frequencies, each from a group of four, are used to transmit numerical address information; it encodes 16 possible combinations of tone pairs using two groups of four tones each. The two groups of four frequencies are 697 Hz, 770 Hz, 852 Hz, and 941 Hz, and 1209 Hz, 1336 Hz, 1477 Hz, and 1633 Hz. DTMF is used primary for call initiation in GSTN telephone applications.

E

ECHO - The distortion created when a transmitted signal is reflected back to the originating station.

ECHO CANCELLER - A devise used to reduce or eliminate echo. It operates by placing a signal that is equal and opposite to the echo signal on the return transmission path.

ECHO SUPPRESSOR - A mechanism used to suppress echoes on long-distance analog connections. The device suppresses the transmission path opposite in direction to the one being used. This feature, although necessary for voice transmission, often interferes with data transmission.

EIA - Electronic Industries Association

EIA INTERFACE, EIA232D, RS 232C - The logical, electrical and physical characteristics of the connection between a DTE and a modem is set out in EIA specification 232D. Previously this has been known as RS232C. The logical characteristics are essentially similar to those specified in CCITT recommendation V.24 and the electrical characteristics to those in V.28.

ELECTROMAGNETIC INTERFERENCE (EMI) - Radiation leakage outside a transmission medium that results mainly from the use of high-frequency wave energy and signal modulation. EMI can be reduced by appropriate shielding.

EMI - See Electromagnetic Interference.

ENVELOPE DELAY - An analog line impairment involving a variation of signal delay with frequency across the data channel bandwidth.

EQUALIZATION - The introduction of components to an analog circuit by a modem to compensate for the attenuation (signal loss) variation and delay distortion with frequency (attenuation equalization) and propagation time variations with frequency (delay equalization). Generally, the higher the transmission rate, the greater the need for equalization.

ERROR - In data communications, any unwanted change in the original contents of a transmission.

ERROR BURST - A concentration of errors within a short period of time as compared with the average incidence of errors. Retransmission is the normal correction procedure in the event of an error burst.

ERROR CONTROL - A process of handling errors, which includes the detection and in some cases, the correction of errors.

EXCHANGE - Assembly of equipment in a communications system that controls the connection of incoming and outgoing lines, and includes the necessary signaling and supervisory functions. Different exchanges, or switches, can be costed to perform different functions, e.g., Local exchange, trunk exchange, etc. See Class of Exchange. Also known as Central Office (U.S. Term).

EXCHANGE, PRIVATE AUTOMATIC BRANCH (PABX) - Private automatic telephone exchange that provides for the switching of calls internally and to and from the public telephone network.

EXCHANGE, PRIVATE BRANCH (PBX) - Private, manually operated telephone exchange that provides private telephone service to an organization and that allows calls to be transmitted to or from the public telephone network.

EXCHANGE AREA - Area containing subscribers served by a local exchange.

F

FILTER - Circuit designed to transmit signals of frequencies within one or more frequency bands and to attenuate signals of other frequencies.

FIRMWARE - Permanent or semi-permanent control coding implemented at a micro-instruction level for an application program, instruction set, operating routine, or similar user-oriented function.

FLOW CONTROL - The use of buffering and other mechanisms, such as controls that turn a device on and off, to prevent data loss during transmission.

FOUR-WIRE CIRCUIT OR CHANNEL - A circuit containing two pairs of wire (or their logical equivalent) for simultaneous (i.e., full-duplex) two-way transmission. Contrast with two-wire channel.

FRAME - 1) A group of bits sent serially over a communications channel; generally a logical transmission unit sent between data-link-layer entities that contain its own control information for addressing and error checking. 2) A piece of equipment in a common carrier office where physical cross connections are made between circuits.

FRAMING - Control procedure used with multiplexed digital channels such as T1 carriers, whereby bits are inserted so the receiver can identify the time slots allocated to each subchannel. Framing bits can also carry alarm signals indicating specific alarm conditions.

FREQUENCY - Rate at which an event occurs, measured in hertz, kilohertz, megahertz, etc.

FREQUENCY BANDS - Frequency bands are defined arbitrarily as follows:

Range (MHz)	Name
0.03-0.3	Low frequency (LF)
0.3-3.0	Medium frequency (MF)
3-30	High frequency (HF)
30-300	Very High frequency (VHF)
300-3000	Ultra high frequency (UHF)
3000-30,000	Super high frequency (SHF) (micro wave)
30,000-300,000	Extremely high frequency (EHF)(millimeterwave)

FSK - Frequency Shift Keying. A method of modulation that uses two different frequencies, usually phase continous, to distinguish between a mark (digital 1) and a space (digital 0) when transmitting on an analog line. Used in modems operating at 1200 bit/s or slower.

FULL-DUPLEX - Pertaining to the capability to send and receive simultaneously.

G

GAIN - Denotes an increase in signal power in transmission from one point to another, usually expressed in dB.

GUARD TONE - In CCITT recommendations V.22 and V.22bis, guard tones may optionally be transmitted along with the data signal from the answering modem. A single frequency of either 1800 or 550 Hz is used and the data signal power must be reduced to keep the overall energy level the same as for transmission without guard tone. The purpose of the guard tone is to prevent the high-band data signal from interfering with the operation of billing apparatus in certain countries.

GSTN - General Switched Telephone Network

H

HALF-DUPLEX - Pertaining to the capability to send and receive but not simultaneously.

HANDSHAKE - An exchange of control sequences between two locations to set up the correct parameters for transmission.

HDLC - High-level Data Link Control. Bit-oriented communication protocol developed by the ISO (International Standards Organization).

HARMONIC DISTORTION - A waveform distortion, usually caused by the nonlinear frequency response of a transmission.

HERTZ (Hz) - A measure of electromagnetic frequency; one hertz is equal to one cycle per second.

HF - High Frequency.

HIGH FREQUENCY (HF) - Portion of the electromagnetic spectrum, typically used in short-wave radio applications. Frequencies in the 3 to 30 MHz range.

Hz - See Hertz.

I

IEEE - Institute of Electrical and Electronics Engineers.

INITIALIZE - To set counters, switches, addresses, or contents of storage to zero or other starting values at the beginning of, or at prescribed points in, the operation of a computer routine.

INTERFACE - A hardware and/or software link between two devices. The interface defines all signal characteristics and other specifications for physical interconnection of the devices.

INTEROFFICE TRUNK - Direct trunk between local central offices (Class 5 offices), or between Class 2, 3, or 4 offices; also called intertoll trunk.

ISO - International Organization for Standardization.

ITU - International Telecommunications Union. The parent organization of the CCITT.

J

JITTER - Slight movement of a transmission signal in time or phase that can introduce errors and loss of synchronization for high-speed synchronous communications. See Phase jitter.

K

KEY PULSING (KP) - Manual method of sending numerical and other signals by the operation of nonlocking pushkeys. Also called Key Sending.

KEY SERVICE UNIT (KSU) - Main operating unit of a key telephone system.

KEY TELEPHONE SYSTEM (KTS) - When more than one telephone line per set is required, pushbutton or key telephone systems offer flexibility and a wide variety of uses, e.g., pickup of several exchange lines, PABX station lines, private lines, and intercommunicating lines. Features of the system include pickup and holding intercommunications, visual and audible signals, cutoff, exclusion, and signaling.

KP - Key Pulse (signaling unlocking signal). See Key Pulsing.

kHz - Kilohertz, kilocycles per second.

KTU - Key Telephone Unit. See Key Service Unit.

L

LEASED LINE - A line rented exclusively to one customer for voice or data communications; dedicated circuit, typically supplied by the telephone company or transmission authority, that permanently connects two or more user locations and is for the sole use of the subscriber. Such circuits are generally voice grade in capacity and in range of frequencies supported, are typically analog, are used for voice or data, can be point-to-point, or multipoint, and can be enhanced with line conditioning. Also called private line, tie-line, or dedicated facility.

LED - Light-Emitting Diode.

LIGHT-EMITTING DIODE (LED) - Semiconductor junction diode that emits radiant energy and is used as a light source for fiber optic communications, particularly for short-haul links.

LIMITED-DISTANCE MODEM - A short-haul modem or line driver that operates over a limited distance. Some limited-distance modems operate at higher speeds than modems that are designed for use over analog telephone facilities, since line conditions can be better controlled.

LINE HIT - A transient disturbance causing a detectable error on a communications line.

LINE-LOADING - The process of installing loading coils in series with each conductor on a transmission line. Usually 88 milliHenry coils installed at 6,000 foot intervals.

LINK - 1) A physical circuit between two points. 2) A logical circuit between two users of a packet switched (or other) network permitting them to communicate (although different physical paths may be used).

LINK LAYER - The logical entity in the OSI model concerned with transmission of data between adjacent network nodes. It is the second layer processing in the OSI model, between the physical and the network layers.

LOADING COILS - An inductance coil installed at regular intervals along a transmission line. Used to improve the quality of voice grade circuits.

LOCAL EXCHANGE - Exchange in which subscribers' lines terminate. The exchange has access to other exchanges and to national trunk networks. Also called local central office, end office.

LOCAL LOOP - The part of a communications circuit between the subscriber's equipment and the equipment in the local exchange.

LOCAL TRUNK - Trunks between local exchanges.

LOSS (TRANSMISSION) - Decrease in energy of signal power in transmission along a circuit due to the resistance or impedance of the circuit or equipment.

M

MARK - The signal (communications channel state) corresponding to a binary one. The marking condition exists when current flows (current-loop channel) or when the voltage is more negative than -3 volts (EIA RS-232 channel).

MATRIX - In switch technology, that portion of the switch architecture where input leads and output leads meet, any pair of which may be connected to establish a through circuit. Also called switching matrix.

Mbit/s - Megabits per second.

MEGAHERTZ (MHz) - A unit of frequency equal to one million cycles per second.

MF - 1) Medium Frequency. 2) Multifrequency. See Dualtone Multifrequency Signaling (DTMF).

MODEM - A contraction of modulate and demodulate; a conversion device installed in pairs at each end of an analog communications line. The modem at the transmitting end modulates digital signals received locally from a computer or terminal; the modem at the receiving end demodulates the incoming signal, converting it back to its original (i.e., digital) format, and passes it to the destination business machine.

MODULATION - The application of information onto a carrier signal by varying one or more of the signal's basic characteristics (frequency, amplitude, or phase); the conversion of a signal from its original (e.g., digital) format to analog format.

MODULATION, PULSE CODE (PCM) - Digital transmission technique that involves sampling of an analog information signal at regular time intervals and coding the measured amplitude value into a series of binary values, which are transmitted by modulation of a pulsed, or intermittent, carrier. A common method of speech digitizing using 8-bit code words, or samples, and a sampling rate of 8 kHz.

Ms - Millisecond. One-thousandth of a second.

MULTIPLEXER - Device that enables more than one signal to be sent simultaneously over one physical channel.

MULTIPLEXING - Division of a transmission facility into two or more channels either by splitting the frequency band transmitted by the channel into narrower bands, each of which is used to constitute a distinct channel (frequency-division multiplex), or by allotting this common channel to several different information channels, one at a time (time-division multiplexing).

MUX - See Multiplexer.

N

NAK - "Negative acknowledge" character. A transmission control character that indicates a block of data was received incorrectly.

NOISE - Undesirable energy in a communications path, which interferes with the reception or processing of a signal.

Ns - Nanosecond; also nsec. One-billionth of a second.

O

OFF HOOK - By analogy with the normal household telephone, a modem is off-hook when it is using the telephone line to make a call. This is similar to raising the telephone handset, or taking it off the hook. Going off-hook is also known as "seizing the line."

ON-HOOK - By analogy with the normal household telephone, a modem is on-hook when it is not using the telephone line. As with a telephone where the handset is on the hook, the line may be used by other equipment to make a call. Going on-hook is also known as "dropping the line."

OSI - Open Systems Interconnection. Referring to the reference model, OSI is a logical structure for network operations standardized within the ISO; a seven-layer network architecture being used for the definition of network protocol standards to enable any OSI-compatible computer or device to communicate with any other OSI-compliant computer or device for a meaningful exchange of information.

OVERFLOW - Excess traffic on a particular route, which is offered to another (alternate) route.

P

PABX - Private Automatic Branch Exchange. See Exchange, Private Automatic Branch (PABX).

PACKET - A group of binary digits including data and call control signals that is switched as a composite whole. The data, call control signals, and error control information are arranged in a specified format.

PBX - Private Branch Exchange. See Exchange, Private Branch.

PHASE JITTER - In telephony, the measurement, in degrees out of phase, that an analog signal deviates from the referenced phase of the main data-carrying signal. Often caused by alternating current components in a telecommunications network; or: a random distortion of signal lengths caused by the rapid fluctuation of the frequency of the transmitted signal. Phase jitter interferes with interpretation of information by changing the timing.

PHASE MODULATION - One of three ways of modifying a sine wave signal to make it carry information. The sine wave or "carrier" has its phase changed in accordance with the information to be transmitted.

PROPAGATION DELAY - The period between the time when a signal is placed on a circuit and when it is recognized and acknowledged at the other end. Propagation delay is of great importance in satellite channels because of the great distances involved.

PROTOCOL - A set of procedures for establishing and controlling communications. Examples include BSC, SDLC, X.25, V.42, V.42bis, MNP, V.22bis handshake, etc.

PSK - Phase Shift Keying. A method of modulation that uses the differences in phase angle between two symbols to encode information. A reference oscillator determines the phase angle change of the incoming signal, which in turn determines which bit or dibit is being transmitted. DPSK (Differential Phase Shift Keying) is a variation of PSK which changes the phase relative to the previous phase.

PULSE CODE MODULATION (PCM) - A method of transmitting information by varying the characteristics of a sequence of pulses, in terms of amplitude, duration, phase, or number. Used to convert an analog signal into a digital bit stream for transmission.

R

REGENERATIVE REPEATER - 1) Repeater utilized in telegraph applications to retime and retransmit the received signal impulses and restore them to their original strength. These repeaters are speed- and code-sensitive and are intended for use with standard telegraph speeds and codes. 2) Repeater used in PCM or digital circuits which detects, retimes, and reconstructs the bits transmitted.

REGENERATOR - Equipment that takes a digital signal that has been distorted by transmission and produces from it a new signal in which the shape, timing, and amplitude of the pulses are that same as those of the original before distortion.

REPEATER - 1) In analog transmission, equipment that receives a pulse train, amplifies it and retimes it for retransmission. 2) In digital transmission, equipment that receives a pulse train, reconstructs it, retimes it, and often then amplifies the signal for retransmission. 3) In fiber optics, a device that decodes a low-power light signal, converts it to electrical energy, and then retransmits it via an LED or laser-generating light source. See also Regenerative Repeater.

REVERSE CHANNEL - A simultaneous low speed data path in the reverse direction over a half-duplex facility. Normally, it is used for positive/negative acknowledgements of previously received data blocks.

RINGER EQUIVALENCE NUMBER - This is a number that the FCC assigns to approved telecom equipment that measures how much load it places on the network during ringing. In the U.S.A., you can connect telephones, modems, FAX machines etc. In parallel to the same telephone line only as long as the sum of their ringer equivalence numbers is less than five. Most countries have a similar regulating system in force, although the methods used to arrive at the number vary widely.

RINGING SIGNAL - Any AC or DC signal transmitted over a line or trunk for the purpose of alerting a party at the distant end of an incoming call. The signal can operate a visual or sound-producing device.

RINGING TONE - Tone received by the calling telephone indicating that the called telephone is being rung. Also called Ringback.

S

SCRAMBLER/DESCRAMBLER - A scrambler function uses a defined method for modifying a data stream, in order to make the altered data stream appear random. A descrambler reverses the effect of the scrambler using the previously defined method to recover the original data stream. Most often used for data encryption, or to avoid transmitting repetitive data patters that can adversely affect data recovery in modems and other data transmission equipment.

SDLC - Synchronous Data Link Control: IBM bit oriented protocol providing for half-duplex transmission; associated with IBM's System Network Architecture (SNA).

SHIELDED PAIR - Two insulated wires in a cable wrapped with metallic braid or foil to prevent interference and provide noise-free transmission.

SIGNAL-TO-NOISE RATIO - The relative power of a signal as compared to the power of noise on a line. As the ratio decreases, it becomes more difficult to distinguish between information and interference.

SIMPLEX - Pertaining to the capability to move in one direction only. Contrast with half-duplex and full-duplex.

SIGNALING - Process by which a caller or equipment on the transmitting end of a line informs a particular party or equipment at the receiving end that a message is to be communicated.

SPACE - Opposite signal condition to a "mark." The signal (communications channnel state) corresponding to a binary zero. In an EIA RS-232 channel, the spacing condition exists when the voltage is more positive than +3 volts.

ST - Start (signal to indicate end of outpulsing).

START-STOP (SIGNALING) - Signaling in which each group of code elements corresponding to a character is preceded by a start signal that serves to prepare the receiving mechanism for the reception and registration of character, and is followed by a stop signal that serves to bring the receiving mechanism to rest in preparation for the reception of the next character. Also known as asynchronous transmission.

STOP-BIT - In asynchronous transmission, the quiescent state following the transmission of a character; usually 1-, or 2-bit times long.

STOP ELEMENT - Last bit of a character in asynchronous serial transmission, used to ensure recognition of the next start element.

SUBSCRIBER LINE - Telephone line connecting the exchange to the subscriber's station. Also called (U.S.term) access line and subscriber loop.

SYNCHRONOUS - Having a constant time interval between successive bits, characters, or events. Synchronous transmission doesn't use non-information bits (such as the start and stop bits in asynchronous transmission) to identify the beginning and end or characters, and thus is faster and more efficient than asynchronous transmission. The timing is achieved by transmitting sync characters prior to data or by extracting timing information from the carrier or reference.

SYNCHRONOUS NETWORK - Network in which all the communications links are synchronized to a common clock.

SYNCHRONOUS TRANSMISSION - Transmission process where the information and control characters are sent at regular, clocked intervals so that the sending and receiving terminals are operating continuously in step with each other.

T

T-CARRIER - A time-division multiplexed, digital transmission facility, operating at an aggregate data rate of 1.544 Mbit/s and above. T-carrier is a PCM system using 64 Kbit/s for a voice channel.

T1 - A digital facility used to transmit a DS-1 formatted digital signal at 1.544 Mbit/s; the equivalent of 24 voice channels.

T1C/T2/T3/T4 - Digital carrier facilities used to transmit signals at 3.152M, 6.312M, 44.736M, 274.176 Mbit/s, respectively.

T3 - A digital carrier facility used to transmit a DS-3 formatted digital carrier signal at 44.736 Mbit/s; the equivalent of 672 voice channels.

TOUCH-TONE - An AT&T trademark for dualtone multifrequency signaling equipment. Use of tones simplifies the switching system design and greatly expands the potential for adding features to telephone systems. It also speeds up the dialing operation for a person making a call.

TRANSCEIVER - Device that can transmit and receive traffic.

TRUNK - Transmission paths that are used to interconnect exchanges in the main telephone network; two switching centers, or a switching center and a distribution point, such as a telephone exchange line that terminates in a PABX network.

TTL - Transistor-Transistor Logic. Digital logic family having common electrical characteristics.

TURNAROUND TIME - The time required to reverse the direction of transmission, e.g; to change from receive mode to transmit mode in order to acknowledge on a half-duplex line. When individual blocks are acknowledged, as is required in certain protocols (e.g., IBM BSC) the turnaround time has a major effect on throughput, particularly if the propagation delay is lengthy, such as on a satellite channel.

TWO-WIRE CIRCUIT - Circuit formed of two conductors insulated from each other, providing a send and return path. Signals may pass in one or both directions.

V

VIDEOTEX - An interactive data communications application designed to allow unsophisticated users to converse with remote databases, enter data for transactions, and retrieve textual and graphics information for display on subscriber television sets or low-cost terminals.

VSLI - Very Large Scale Integration.

V SERIES RECOMMENDATIONS -
(CCITT V.xx Standards)
Also see Voiceband Modem Standards chart on page 9-12.

V.1 - Definitions of key terms for binary symbol notation, such as binary 0 = space, binary 1 = mark.

V.2 (1) - Specification of power levels for data transmission over telephone line.

V.4 - Definition of the order of bit transmission, the use of a parity bit, and the use of start/stop bits for asynchronous transmission.

V.5 - Specification of data-signaling rates (bit/s) for synchronous transmission in the switched telephone network.

V.6 - Specification of data signaling rates (bit/s) for synchronous transmission on leased telephone circuits.

V.7 - Definitions of other key terms used in the V-series recommendations.

V.10 - Description of an unbalanced physical level interchange circuit (unbalanced means one active wire between transmitter and receiver with ground providing the return).

V.11 - Description of a balanced physical level interchange circuit (balanced means two wires between the transmitter and receiver with both wires' signals constant with respect to Earth).

V.15 - Description of use of acoustic couplers for data transmission.

V.16 - Description of the transmission of ECG (electrocardiogram) signals on the telephone channel.

V.19 - Description of one-way parallel transmission modems using push-button telephone sets.

V.20 - Description of one-way parallel transmission modems, excluding push-button telephone sets.

V.22 - Operating at 1.2 Kbit/s, encodes two consecutive bit (dibits); the dibits are encoded as a change relative to the previous signal element.

V.22bis - Operating at 2.4 Kbit/s, encodes four consecutive bits (quadbits); the first two bits are encoded relative to the quadrant of the previous signal element, the last two bits are associated with the point in new quadrant.

V.24 - Definition of the interchange circuit pins between DTEs (data terminal equipment) and DCEs (data circuit-terminating equipment).

V.25 - (2) - Specifications for automatic-answering equipment.

V.25bis - (2) - Specifications for automatic-answering equipment.

V.28 - Description of unbalanced interchange circuits operating below 20 Kbit/s.

V.29 - Operating at 9.6 Kbit/s, encodes four consecutive bits (quadbits); the first bit determines the amplitude, the last three bits use the encoding scheme of V.27.

V.29 - Operating at 4.8 Kbit/s, encodes two consecutive bits (dibits); amplitude is constant and phase changes are the same as V.26.

V.31 - Description of low-speed interchange circuits (up to 75 Bit/s).

V.31bis - Description of low-speed interchange circuits (up to 1.2 Kbit/s).

V.32 - Operating at 9.6 Kbit/s, encodes four consecutive bits (quadbits); the bits are mapped to a QAM signal.

V.32 - Operating at 9.6 Kbit/s with Trellis-coded modulation (TCM), encodes four consecutive bits, two of which are used to generate a fifth bit; the bits are mapped to a QAM signal.

V.32 - Operating at 4.8 Kbit/s, encodes two consecutive bits (dibits), which are mapped to a QAM signal.

V.42 - Defines a method of error control.

V.42bis - Defines a method of data compression.

Note: In the United States, EIA RS-496 specifies these measurements and RS-366 specifies these procedures.

VOICE-GRADE CHANNEL - a channel with a frequency range from 300 to 3000 Hz and suitable for the transmission of speech, data, or facsimile.

W

WORD - A group of bits handled as a logical unit; usually 16.

Voiceband Modem Standards

CCITT Standard	Data Rate (Bit/s)	Full- or Half-Duplex	Channel Separation	Carrier Frequency (Hz)	Modulation Method	Modulation Rate (Baud)	Bits Encoded	Synchronous or Asynchronous	Back Channel	GSTN	Leased Lines	Equalization	Scrambler
V.21	300	Full	Frequency Division	1080, & 1750	Frequency Shift	300	1:1	Either	ND	Yes	No	ND	ND
V.22	1200	Full	Frequency Division	1200, & 2400	Phase Shift	600	2:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed	Yes
V.22	600	Full	Frequency Division	1200, & 2400	Phase Shift	600	1:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed	Yes
V.22bis	2400	Full	Frequency Division	1200, & 2400	Quadrature-Amplitude Modulation	600	4:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed/ Adaptive	Yes
V.22bis	1200	Full	Frequency Division	1200, & 2400	Quadrature-Amplitude Modulation	600	2:1	Either	ND	Yes	Point-to-Point 2-Wire	Fixed/ Adaptive	Yes
V.23	600 (1)	Half	N/A	1300, & 1700	Frequency Modulation	600	N/A	Either	Yes	Yes	No	ND	ND
V.23	1200 (1)	Half	N/A	1300, & 2100	Frequency Modulation	1200	N/A	Either	Yes	Yes	No	ND	ND
V.25	2400	Full	4-Wire	1800	Phase Shift	1200	2:1	Synchronous	Yes	No	Point-to-Point Multipoint 4-Wire	ND	ND
V.26bis	2400	Half	N/A	1800	Phase Shift	1200	2:1	Synchronous	Yes	Yes	No	Fixed	ND
V.26bis	1200	Half	N/A	1800	Phase Shift	1200	1:1	Synchronous	Yes	Yes	No	Fixed	ND
V.26ter	2400	Either	Echo Cancellation	1800	Phase Shift	1200	2:1	Either	ND	Yes	Point-to-Point 2-Wire	Either	Yes
V.26ter	1200	Either	Echo Cancellation	1800	Phase Shift	1200	1:1	Either	ND	Yes	Point-to-Point 2-Wire	Either	Yes
V.27	4800	Either	ND (3)	1800	Phase Shift	1600	3:1	Synchronous	Yes	No	Yes (3)	Manual	Yes
V.27bis	4800	Either	4-Wire (4)	1800	Phase Shift	1600	3:1	Synchronous	Yes	No	2-Wire, 4-Wire	Adaptive	Yes
V.27bis	2400	Either	4-Wire (4)	1800	Phase Shift	1200	2:1	Synchronous	Yes	No	2-Wire, 4-Wire	Adaptive	Yes
V.27ter	4800	Half	None	1800	Phase Shift	1800	3:1	Synchronous	Yes	Yes	No	Adaptive	Yes
V.27ter	2400	Half	None	1800	Phase Shift	1200	2:1	Synchronous	Yes	Yes	No	Adaptive	Yes
V.29	9600	Either	4-Wire	1700	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	No	No	Point-to-Point 4-Wire	Adaptive	Yes
V.29	7200	Either	4-Wire	1700	Phase Shift (5)	2400	3:1	Synchronous	ND	No	Point-to-Point 4-Wire	Adaptive	Yes
V.29	4800	Either	4-Wire	1700	Phase Shift (5)	2400	2:1	Synchronous	ND	No	Point-to-Point 4-Wire	Adaptive	Yes
V.32	9600	Full	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32bis	14400	Full (proposed)	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	4:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32	9600	Full	Echo Cancellation	1800	Trellis-Coded Modulation	2400	5:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.32	4800	Full	Echo Cancellation	1800	Quadrature-Amplitude Modulation	2400	2:1	Synchronous	ND	Yes	Point-to-Point 2-Wire	Adaptive	Yes
V.33	14400	Half						Synchronous	ND	Yes		Adaptive	Yes
Bell (U.S.) Standard													
103	300	Full	Frequency Division	2225 & 1270(m) 2025 & 1070(s)	Frequency Shift	300	1:1	Either	No	Yes	No	Fixed	No
201	2400	Half	None	1800	Phase Shift	1200	2:1	Synchronous	No	Yes	Point-to-Point 2-Wire	Adaptive	Yes
202	1200	Half	None	1200 & 2200	FSK	1200	1:1	Either	Yes	Yes	Point-to-Point 2-Wire	Fixed	No
208	4800	Half	None	1800	Quadrature-Amplitude Modulation	1600	3:1	Synchronous	No	Yes	Point-to-Point 2-Wire	Adaptive	Yes
212	1200	Full	Frequency Division	1200 & 2400	Phase Shift	600	2:1	Either	No	Yes	No	Fixed	Yes

1. Bit/s not used in specification; rate stated in baud
2. Half-duplex may still use a backward channel
3. Makes no mention of 4-wire (must be assumed)
4. For half-duplex, 2-wire used
5. Amplitude is constant on a relative basis

ND = Not defined (i.e., not specified in the recommendation)

Silicon Systems, Inc.
14351 Myford Road, Tustin, CA 92680
Ph (714) 573-6000, Fax (714) 573-6914

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