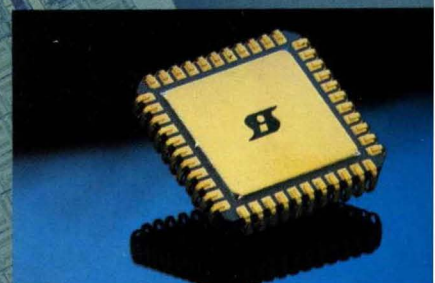


# Integrated Circuits Data Book

Siliconix Integrated Circuits Data Book



  
1988

 Siliconix

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**1988**

**INTEGRATED CIRCUITS**

**DATA BOOK**



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We solicit your comments and suggestions, and look forward to continually serving your future analog integrated circuit requirements.

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**NOTES:**

1. Obsolete product.
2. Contact factory on availability.

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DG172 ... 5-46	DG405 ... 5-212	DG569 .. 5-381	Si9100 ... 10-16
DG180 ... 5-51	DG408 ... 5-229	DG601 .. 5-407	Si9101 ... 10-16
DG181 ... 5-51	DG409 ... 5-229	DG908 .. 5-414	Si9102 ... 10-26
DG182 ... 5-51	DG411 ... 5-234	DG909 .. 5-414	Si9110 ... 10-35
DG183 ... 5-62	DF412 ... 9-2	Si2504 .. 6-22	Si9111 ... 10-35
DG184 ... 5-62	DG412 ... 5-234	Si3002 .. 5-425	Si9115 ... 10-43
DG185 ... 5-62	DG413 ... 5-234	SD5000 .. 7-81	Si9116 ... 10-43
DG186 ... 5-74	DG417 ... 5-245	SD5001 .. 7-81	Si9551 ... 9-12
DG187 ... 5-74	DG418 ... 5-245	SD5002 .. 7-81	Si9552 ... 9-12
DG188 ... 5-74	DG419 ... 5-245	DG5040 . 5-389	Si9553 ... 9-18
DG189 ... 5-85	DG421 ... 5-255	DG5041 . 5-389	Si9554 ... 9-18
DG190 ... 5-85	DG423 ... 5-255	DG5042 . 5-389	Si9555 ... 9-18
DG191 ... 5-85	DG425 ... 5-255	DG5043 . 5-389	Si9556 ... 9-18
DG200A .. 5-96	DG441 ... 5-265	DG5044 . 5-389	Si9560 ... 9-27

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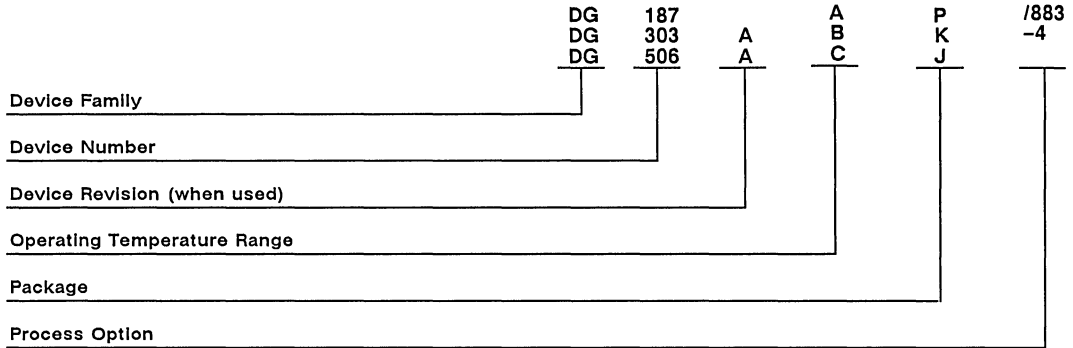






# DEVICE ORDERING INFORMATION

## Integrated Circuits and Power ICs



1

### DEVICE FAMILY

(1, 2, or 3 Letters)

- D - Drivers for FET Switches
- DF - Digital Function
- DG - Analog Switches and Analog Multiplexers
- DGP - Precision Analog Switch
- G - Multi-Channel FETs
- L - Linear
- LD - Linear Digital Combinations
- SD - Siliconix DMOS Product
- SI - Siliconix Proprietary Integrated Circuit or Second Source Part
- SJM - QPL Listed Part

### PACKAGE

(1 Letter)

- A - Metal Can
- H - Eight Pin Mini Dip-Plastic
- J - Dual-In-Line Package-Plastic
- K - Dual-In-Line Package-CERDIP
- L - Flat Package
- M - Ceramic J Bend Quad (CLCC)
- N - PLCC
- P - Dual-In-Line Package-Side Braze
- R - Dual-In-Line Package-Side Braze
- Y - Small Outline Package (SOIC)
- Z - Leadless Chip Carrier (LCC)

### DEVICE NUMBER

(3 or 4 Digit Numbers)

### OPERATING TEMPERATURE RANGE

(1 Letter)

- A -55 to 125°C
- B -25 to 85°C
- C 0 to 70°C
- D -40 to 85°C

B and D temperature range parts receive industrial processing unless a process option dash number is added to the part number.

C temperature range parts are given commercial processing.

All possible combinations of device types, temperature ranges, package types and MIL-883 process options are not necessarily available. Consult individual data book pages or sales office for complete information.

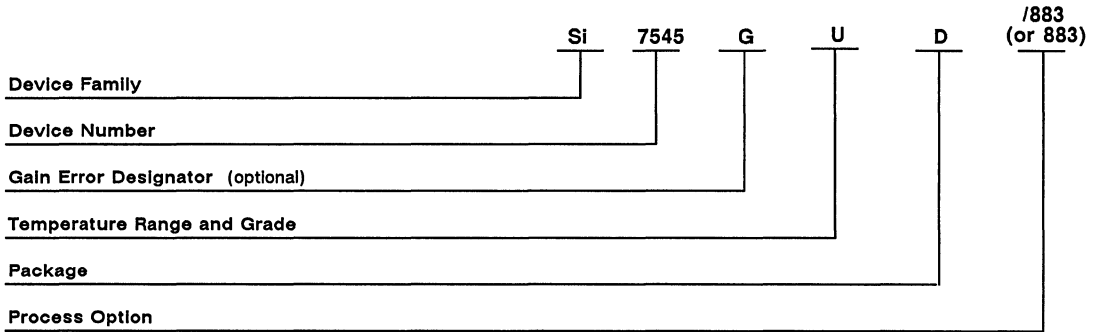
### PROCESS OPTION

- /883 - Processing to the current revision of MIL-STD-883, Level B. Compliant-Non JAN
- 2 - Non Compliant-Non JAN\*
- 4 - 160 Hour Burn-In
- /BS - BS9000 Compliant

\* Many older -2 processed parts are now upgraded to /883 process flows.

Note: Please refer to the following page for data acquisition nomenclature.

# Data Acquisiton



**TEMPERATURE RANGE**  
(1 Letter)

A	-40 to 85°C
B	-40 to 85°C
C	-40 to 85°C
J	0 to 70°C
K	0 to 70°C
L	0 to 70°C
S	-55 to 125°C
T	-55 to 125°C
U	-55 to 125°C

**GRADE**

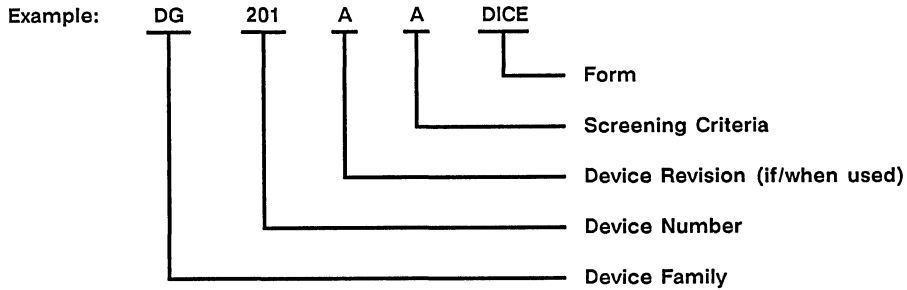
Good
Better
Best
Good
Better
Best
Good
Better
Best

**PACKAGE**  
(1 Letter)

D	- Side Braze DIP
E	- LCC
N	- Plastic DIP
P	- PLCC (Plastic Quad J-Bend)
Q	- CERDIP

# DIE ORDERING INFORMATION

## MONOLITHIC CHIPS



### DEVICE FAMILY

(1, 2 or 3 Letters)

- D** – Drivers for FET Switches
- DG** – Analog Switches
- DGP** – Precision Analog Switch
- G** – Multi-Channel FETs
- L** – Linear
- Si** – Siliconix Proprietary or Second Source Part

### SCREENING CRITERIA

(1 LETTER)

- A** – Electrically probed @ 25°C; visual criteria screening to MIL-STD-883, Method 2010 Condition B.
- I** – Electrically probed @ 25°C; visual criteria screening to Siliconix Specification 501B.

### DEVICE NUMBER

(3 or 4 Digit Numbers)

### FORM

(4 Letters)

- DICE** – Chips wafer packaged per Figure 1 in Die Process Information

## MULTICHIP

To order die which form multichip devices the driver chip and corresponding JFETs should be ordered using the geometry designations as shown in Table 1.

Example: For DG190 die, order  
CMJB1000  
and NC1000

To determine number of JFETs required to go with each driver in a multichip device, see number in parenthesis following geometry codes as shown in Table 1.

## OPTIONS

The following options are considered “special” and a special part number will be assigned:

1. Die in wafer form
2. Gold Backing on Integrated Circuit dice
3. Class A visual
4. Customer visual criteria

Please identify as “similar to \_\_\_\_\_ with following additional conditions \_\_\_\_\_”.

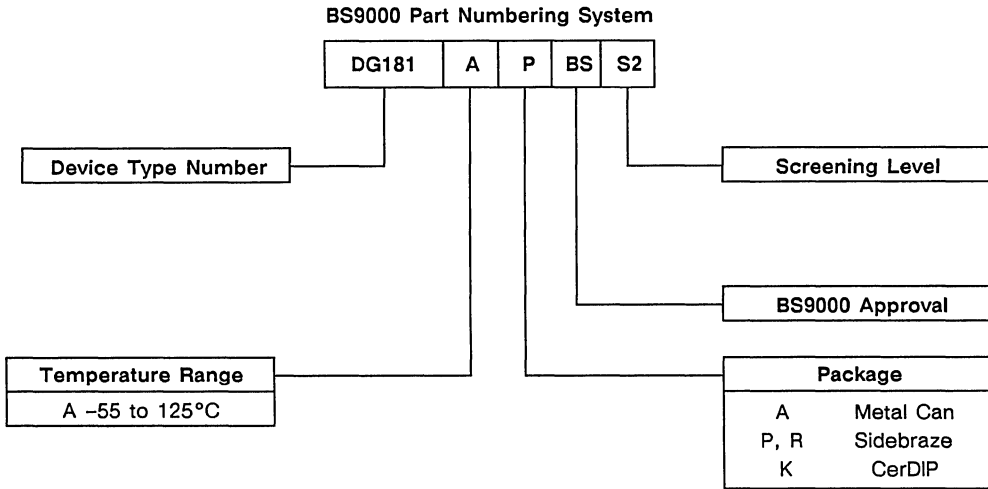


**Table 1**

<b>Siliconix Part No.</b>	<b>Geometry Code</b>		<b>Technology</b>
	<b>Driver</b>	<b>FET</b>	
DG126	LODC1000	NC2000(4)	JFET Switch
DG129	LODC1000	NC1000(4)	JFET Switch
DG133	LODC1000	NC1000(2)	JFET Switch
DG134	LODC1000	NC2000(2)	JFET Switch
DG139	LODF1000	NC1000(4)	JFET Switch
DG140	LODC1000	NIP1000(4)	JFET Switch
DG141	LODC1000	NIP1000(2)	JFET Switch
DG142	LODF1000	NC2000(4)	JFET Switch
DG143	LODF1000	NC2000(2)	JFET Switch
DG144	LODF1000	NC1000(2)	JFET Switch
DG145	LODF1000	NIP1000(4)	JFET Switch
DG146	LODF1000	NIP1000(2)	JFET Switch
DG180	CMJB1000	NIP1000(2)	JFET Switch
DG181	CMJB1000	NC1000(2)	JFET Switch
DG182	CMJB1000	NC2000(2)	JFET Switch
DG183	CMJA1000	NIP1000(4)	JFET Switch
DG184	CMJA1000	NC1000(4)	JFET Switch
DG185	CMJA1000	NC2000(4)	JFET Switch
DG186	CMJC1000	NIP1000(2)	JFET Switch
DG187	CMJC1000	NC1000(2)	JFET Switch
DG188	CMJC1000	NC2000(2)	JFET Switch
DG189	CMJB1000	NIP1000(4)	JFET Switch
DG190	CMJB1000	NC1000(4)	JFET Switch
DG191	CMJB1000	NC2000(4)	JFET Switch

# BS9000 ORDERING INFORMATION

## ANALOG SWITCHES AND MULTIPLEXERS



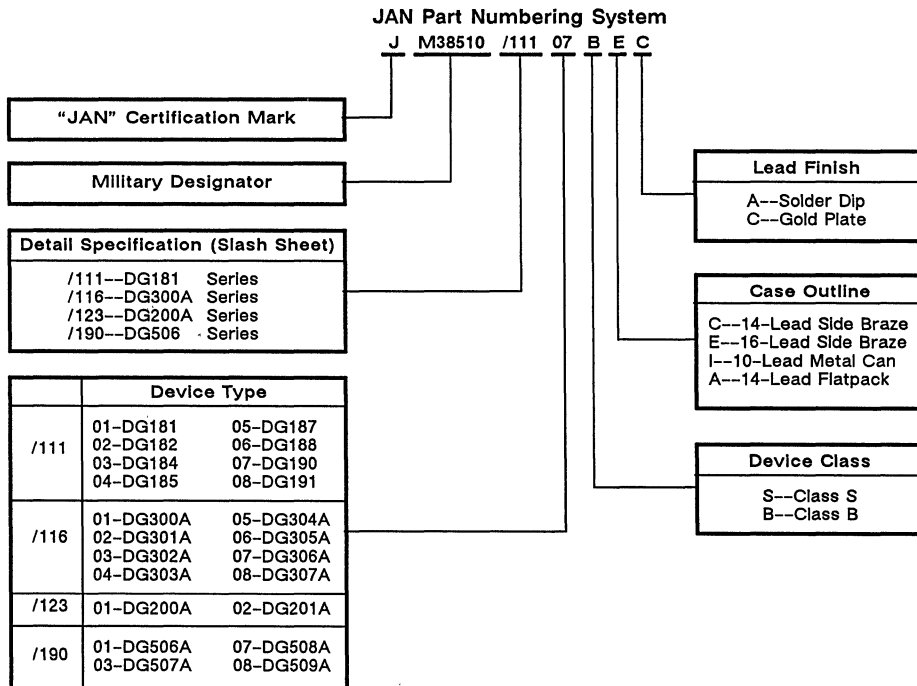
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Available Parts		
Ordering Part No.	Ordering Part No.	Ordering Part No.
DG181AABS S2	DG300AAABS S2	DG384AAKBS S2
DG185APBS S2	DG300AAKBS S2	DG390AAKBS S2
DG187APBS S2	DG301AAABS S2	
DG189APBS S2	DG301AAKBS S2	DG506AAKBS S2
	DG302AAKBS S2	DG507AAKBS S2
DG190APBS S2	DG303AAKBS S2	DG508AAKBS S2
DG191APBS S2	DG304AAABS S2	DG509AAKBS S2
	DG305AAABS S2	
DG200AAABS S2	DG307AAKBS S2	
DG200AAKBS S2	DG308AAKBS S2	

Contact one of the Siliconix sales offices for latest information.

# JAN38510 ORDERING INFORMATION ANALOG SWITCHES AND MULTIPLEXERS

Several Siliconix Analog Switches and multiplexers are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format: JM38510/XXXXX. Refer to the current Siliconix Price list for available part types and order numbers.



## Available JAN Parts

Generic Part Number	JAN Part Number	Order Part Number
DG181AP/883	JM38510/11101BCC	SJM181BCC
DG181AP/883	JM38510/11101BCA	SJM181BCA
DG181AA/883	JM38510/11101BIC	SJM181BIC
DG181AL/883	JM38510/11101BAC	SJM181BAC
DG182AP/883	JM38510/11102BCC	SJM182BCC
DG182AP/883	JM38510/11102BCA	SJM182BCA
DG182AA/883	JM38510/11102BIC	SJM182BIC
DG182AL/883	JM38510/11102BAC	SJM182BAC
DG184AP/883	JM38510/11103BEC	SJM184BEC
DG184AP/883	JM38510/11103BEA	SJM184BEA
DG184AL/883	JM38510/11103BAC	SJM184BAC
DG185AP/883	JM38510/11104BEC	SJM185BEC
DG185AP/883	JM38510/11104BEA	SJM185BEA
DG185AL/883	JM38510/11104BAC	SJM185BAC

**Available JAN Parts (continued)**

Generic Part Number	JAN Part Number	Order Part Number
DG187AP/883	JM38510/11105BCC	SJM187BCC
DG187AP/883	JM38510/11105BCA	SJM187BCA
DG187AA/883	JM38510/11105BIC	SJM187BIC
DG187AL/883	JM38510/11105BAC	SJM187BAC
DG188AP/883	JM38510/11106BCC	SJM188BCC
DG188AP/883	JM38510/11106BCA	SJM188BCA
DG188AA/883	JM38510/11106BIC	SJM188BIC
DG188AL/883	JM38510/11106BAC	SJM188BAC
DG190AP/883	JM38510/11107BEC	SJM190BEC
DG190AP/883	JM38510/11107BEA	SJM190BEA
DG190AL/883	JM38510/11107BAC	SJM190BAC
DG191AP/883	JM38510/11108BEC	SJM191BEC
DG191AP/883	JM38510/11108BEA	SJM191BEA
DG191AL/883	JM38510/11108BAC	SJM191BAC
DG200AAP/883	JM38510/12301BCC	SJM200BCC
DG200AAP/883	JM38510/12301BCA	SJM200BCA
DG200AAA/883	JM38510/12301BIC	SJM200BIC
DG201AAP/883	JM38510/12302BEC	SJM201BEC
DG201AAP/883	JM38510/12302BEA	SJM201BEA
DG300AAP/883	JM38510/11601BCC	SJM300BCC
DG300AAP/883	JM38510/11601BCA	SJM300BCA
DG300AAA/883	JM38510/11601BIC	SJM300BIC
DG301AAP/883	JM38510/11602BCC	SJM301BCC
DG301AAP/883	JM38510/11602BCA	SJM301BCA
DG301AAA/883	JM38510/11602BIC	SJM301BIC
DG302AAP/883	JM38510/11603BCC	SJM301BCC
DG302AAP/883	JM38510/11603BCA	SJM301BCA
DG303AAP/883	JM38510/11604BCC	SJM303BCC
DG303AAP/883	JM38510/11604BCA	SJM303BCA
DG304AAP/883	JM38510/11605BCC	SJM304BCC
DG304AAP/883	JM38510/11605BCA	SJM304BCA
DG304AAA/883	JM38510/11605BIC	SJM304BIC
DG305AAP/883	JM38510/11606BCC	SJM305BCC
DG305AAP/883	JM38510/11606BCA	SJM305BCA
DG305AAA/883	JM38510/11606BIC	SJM305BIC
DG306AAP/883	JM38510/11607BCC	SJM306BCC
DG306AAP/883	JM38510/11607BCA	SJM306BCA
DG307AAP/883	JM38510/11608BCC	SJM307BCC
DG307AAP/883	JM38510/11608BCA	SJM307BCA
DG506AAR/883	JM38510/19001BXC	SJM506BXC
DG507AAR/883	JM38510/19003BXC	SJM507BXC
DG508AAP/883	JM38510/19007BEA	SJM508BEA
DG508AAP/883	JM38510/19007BEC	SJM508BEC
DG509AAP/883	JM38510/19008BEA	SJM509BEA
DG509AAP/883	JM38510/19008BEC	SJM509BEC

**1**

# STANDARD MILITARY DRAWING (SMD) /883 Compliant/Non JAN Class B

Siliconix offers products which meet requirements of MIL-STD-883 paragraph 1.2.1 "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

## SMD Compliant/Non JAN

SMD/DESC Part #	Generic Part #
7705201EA	DG508AAK DESC
7705201EC	DG508AAK DESC
770520FC	DG508AAL DESC
7705301EA	DG201AAK DESC
7705301EC	DG201AAP DESC
7801401CA	DG129AP DESC
7801401CC	DG129AP DESC
8100601EA	DG5140AK DESC
8100601IC	DG5140AA DESC
8100602EA	DG5141AK DESC
8100602IC	DG5141AA DESC
8100603EA	DG5142AK DESC
8100603IC	DG5142AA DESC
8100604EA	DG5143AK DESC
8100605EA	DG5144AK DESC
8100605IC	DG5144AA DESC
8100606EA	DG5145AK DESC
8100609EA	DG5140AK DESC
8100609IC	DG5140AA DESC
8100610EA	DG5141AK DESC
8100610IC	DG5141AA DESC
8100611EA	DG5142AK DESC
8100611IC	DG5142AA DESC
8100612EA	DG5143AK DESC
8100613EA	DG5144AK DESC
8100613IC	DG5144AA DESC
8100614EA	DG5145AK DESC

## Class B /883 Compliant/Non JAN

Industry Part #	Siliconix Part #	Industry Part #	Siliconix Part #	Industry Part #	Siliconix Part #
AD7506JD/883	DG506AAR/883	AH0140D/883	DG140AP/883	AH0163D/883	DG145AP/883
AD7507JD/883	DG507AAR/883	AH0141D/883	DG141AP/883	AH0164D/883	DG139AP/883
AD7541ASD/883	SI7541ASD/883	AH0143D/883	DG143AP/883		DG405AK/883
AD7541ATD/883	SI7541ATD/883	AH0144D/883	DG144AP/883	DGM184AK/HR	DG405AK/883
AD7545SD/883	SI7545SD/883	AH0145D/883	DG145AP/883	DGM185AK/HR	DG405AK/883
AD7545TD/883	SI7545TD/883	AH0146D/883	DG146AP/883	DGM185AK/883B	DG405AK/883
AD7545UD/883	SI7545UD/883	AH0151D/883	DG141AP/883	DGM190AK/HR	DG403AK/883
AH0126D/883	DG126AP/883	AH0152D/883	DG133AP/883	DGM190AK/883B	DG403AK/883
AH0129D/883	DG129AP/883	AH0153D/883	DG140AP/883	DGM191AK/HR	DG403AK/883
AH0133D/883	DG133AP/883	AH0154D/883	DG129AP/883	DGP201AAK/883	DGP201AAK/883
AH0134D/883	DG134AP/883	AH0161D/883	DG146AP/883	DGP201AAZ/883	DGP201AAZ/883
AH0139D/883	DG139AP/883	AH0162D/883	DG144AP/883	DGP303AAK/883	DGP303AAK/883

## Class B /883 Compliant/Non JAN (Cont'd)

Industry Part #	Siliconix Part #	Industry Part #	Siliconix Part #	Industry Part #	Siliconix Part #
DGP303AAZ/883	DGP303AAZ/883	DG141AL	DG141AL/883	DG163AL-2	DG145AL/883
DGP508AAK/883	DGP508AAK/883	DG141AL-2	DG141AL/883	DG163AL/883	DG145AL/883
DGP508AAZ/883	DGP508AAZ/883	DG141AL/HR	DG141AL/883	DG163AP-2	DG145AP/883
DG123AL	DG123AL/883	DG141AL/883	DG141AL/883	DG163AP/883	DG145AP/883
DG123AL-2	DG123AL/883	DG141AP-2	DG141AP/883	DG164AL-2	DG139AL/883
DG123AL/HR	DG123AL/883	DG141AP/883	DG141AP/883	DG164AL/883	DG139AL/883
DG123AL/883	DG123AL/883	DG142AL	DG142AL/883	DG164AP-2	DG139AP/883
DG123AP-2	DG123AP/883	DG142AL-2	DG142AL/883	DG164AP/883	DG139AP/883
DG123AP/HR	DG123AP/883	DG142AL/HR	DG142AL/883	DG172AL	DG172AL/883
DG123AP/883	DG123AP/883	DG142AL/883	DG142AL/883	DG172AL-2	DG172AL/883
DG125AL	DG125AL/883	DG142AL/883B	DG142AL/883	DG172AL/883	DG172AL/883
DG125AL-2	DG125AL/883	DG142AP-2	DG142AP/883	DG180AA-2	DG180AA/883
DG125AL/HR	DG125AL/883	DG142AP/883	DG142AP/883	DG180AA/883	DG180AA/883
DG125AL/883	DG125AL/883	DG143AL	DG143AL/883	DG180AL-2	DG180AL/883
DG125AP-2	DG125AP/883	DG143AL-2	DG143AL/883	DG180AL/883	DG180AL/883
DG125AP/HR	DG125AP/883	DG143AL/HR	DG143AL/883	DG180AP-2	DG180AP/883
DG125AP/883	DG125AP/883	DG143AL/883B	DG143AL/883	DG180AP/883	DG180AP/883
DG126AK/HR	DG126AP/883	DG143AP-2	DG143AP/883	DG181AA-2	DG181AA/883
DG126AL	DG126AL/883	DG143AP/883	DG143AP/883	DG181AA/883	DG181AA/883
DG126AL-2	DG126AL/883	DG144AL	DG144AL/883	DG181AL	DG181AL/883
DG126AL/HR	DG126AL/883	DG144AL-2	DG144AL/883	DG181AL-2	DG181AL/883
DG126AL/883B	DG126AL/883	DG144AL/HR	DG144AL/883	DG181AL/883	DG181AL/883
DG126AP-2	DG126AP/883	DG144AL/883B	DG144AL/883	DG181AP-2	DG181AP/883
DG126AP/883	DG126AP/883	DG144AP-2	DG144AP/883	DG181AP/883	DG181AP/883
DG129AL	DG129AL/883	DG144AP/883	DG144AP/883	DG182AA-2	DG182AA/883
DG129AL-2	DG129AL/883	DG145AL	DG145AL/883	DG182AA/883	DG182AA/883
DG129AL/HR	DG129AL/883	DG145AL-2	DG145AL/883	DG182AL	DG182AL/883
DG129AL/883	DG129AL/883	DG145AL/883	DG145AL/883	DG182AL-2	DG182AL/883
DG129AL/883B	DG129AL/883	DG145AP-2	DG145AP/883	DG182AP-2	DG182AP/883
DG129AP-2	DG129AP/883	DG145AP/883	DG145AP/883	DG182AP/883	DG182AP/883
DG129AP/883	DG129AP/883	DG146AL-2	DG146AL/883	DG183AL	DG183AL/883
DG133AL	DG133AL/883	DG146AL/883	DG146AL/883	DG183AL-2	DG183AL/883
DG133AL-2	DG133AL/883	DG146AP-2	DG146AP/883	DG183AL/883	DG183AL/883
DG133AL/HR	DG133AL/883	DG146AP/883	DG146AP/883	DG183AP-2	DG183AP/883
DG133AL/883	DG133AL/883	DG151AL-2	DG141AL/883	DG183AP/883	DG183AP/883
DG133AL/883B	DG133AP/883	DG151AL/883	DG141AL/883	DG184AL	DG184AL/883
DG133AP-2	DG133AP/883	DG151AP-2	DG141AP/883	DG184AL-2	DG184AL/883
DG133AP/883	DG134AL/883	DG151AP/883	DG141AP/883	DG184AL/883	DG184AL/883
DG134AL	DG134AL/883	DG152AL-2	DG133AL/883	DG184AP-2	DG184AP/883
DG134AL-2	DG134AL/883	DG152AL/883	DG133AL/883	DG184AP/883	DG184AP/883
DG134AL/HR	DG134AL/883	DG152AP-2	DG133AP/883	DG185AL	DG185AL/883
DG134AL/883	DG134AL/883	DG152AP/883	DG133AP/883	DG185AL-2	DG185AL/883
DG134AL/883B	DG134AP/883	DG153AL-2	DG140AL/883	DG185AL/883	DG185AL/883
DG134AP-2	DG134AP/883	DG153AL/883	DG140AL/883	DG185AP-2	DG185AP/883
DG134AP/883	DG139AL/883	DG153AP-2	DG140AP/883	DG185AP/883	DG185AP/883
DG139AL	DG139AL/883	DG153AP/883	DG140AP/883	DG186AA-2	DG186AA/883
DG139AL-2	DG139AL/883	DG154AL-2	DG129AL/883	DG186AA/883	DG186AA/883
DG139AL/HR	DG139AL/883	DG154AL/883	DG129AL/883	DG186AL	DG186AL/883
DG139AL/883	DG139AL/883	DG154AP-2	DG129AP/883	DG186AL-2	DG186AL/883
DG139AL/883B	DG139AP/883	DG154AP/883	DG129AP/883	DG186AL/883	DG186AL/883
DG139AP-2	DG139AP/883	DG161AL-2	DG146AL/883	DG186AP-2	DG186AP/883
DG139AP/883	DG140AL/883	DG161AL/883	DG146AL/883	DG186AP/883	DG186AP/883
DG140AL	DG140AL/883	DG161AP-2	DG146AP/883	DG187AA-2	DG187AA/883
DG140AL-2	DG140AL/883	DG161AP/883	DG146AP/883	DG187AA/883	DG187AA/883
DG140AL/HR	DG140AL/883	DG162AL-2	DG144AL/883	DG187AL	DG187AL/883
DG140AL/883	DG140AP/883	DG162AL/883	DG144AL/883	DG187AL-2	DG187AL/883
DG140AP-2	DG140AP/883	DG162AP-2	DG144AP/883	DG187AL/883	DG187AL/883
DG140AP/HR	DG140AP/883	DG162AP/883	DG144AP/883	DG187AP-2	DG187AP/883
DG140AP/883	DG140AP/883				

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## Class B

### /883 Compliant/Non JAN (Cont'd)

Industry Part #	Siliconix Part #	Industry Part #	Siliconix Part #	Industry Part #	Siliconix Part #
DG187AP/883	DG187AP/883	DG301AAK-2	DG301AAK/883	DG501AP-2	DG501AP/883
DG188AA-2	DG188AA/883	DG301AAK/883	DG301AAK/883	DG501AP/883	DG501AP/883
DG188AA/883	DG188AA/883	DG301AAZ/883	DG301AAZ/883	DG503AP-2	DG503AP/883
DG188AL	DG188AL/883	DG302AAK-2	DG302AAK/883	DG5040AK-2	DG5040AK/883
DG188AL-2	DG188AL/883	DG302AAK/883	DG302AAK/883	DG5040AK/883	DG5040AK/883
DG188AL/883	DG188AL/883	DG303AAK-2	DG303AAK/883	DG5041AK-2	DG5041AK/883
DG188AP-2	DG188AP/883	DG303AAK/883	DG303AAK/883	DG5041AK/883	DG5041AK/883
DG188AP/883	DG188AP/883	DG303AAZ/883	DG303AAZ/883	DG5042AK-2	DG5042AK/883
DG189AL	DG189AL/883	DG304AAA-2	DG304AAA/883	DG5042AK/883	DG5042AK/883
DG189AL-2	DG189AL/883	DG304AAA/883	DG304AAA/883	DG5043AK-2	DG5043AK/883
DG189AL/883	DG189AL/883	DG304AAK-2	DG304AAK/883	DG5043AK/883	DG5043AK/883
DG189AP-2	DG189AP/883	DG304AAK/883	DG304AAK/883	DG5044AK-2	DG5044AK/883
DG189AP/883	DG189AP/883	DG305AAA-2	DG305AAA/883	DG5044AK/883	DG5044AK/883
DG190AL	DG190AL/883	DG305AAA/883	DG305AAA/883	DG5045AK-2	DG5045AK/883
DG190AL-2	DG190AL/883	DG305AAK-2	DG305AAK/883	DG5045AK/883	DG5045AK/883
DG190AL/883	DG190AL/883	DG305AAK/883	DG305AAK/883	DG5048AK/883	DG5048AK/883
DG190AP-2	DG190AP/883	DG306AAK-2	DG306AAK/883	DG5049AK/883	DG5049AK/883
DG190AP/883	DG190AP/883	DG306AAK/883	DG306AAK/883	DG5050AK/883	DG5050AK/883
DG191AL	DG191AL/883	DG307AAK-2	DG307AAK/883	DG5051AK/883	DG5051AK/883
DG191AL-2	DG191AL/883	DG307AAK/883	DG307AAK/883	DG506AAK-2	DG506AAK/883
DG191AL/883	DG191AL/883	DG307AAZ/883	DG307AAZ/883	DG506AAK/883	DG506AAK/883
DG191AP-2	DG191AP/883	DG308AAK-2	DG308AAK/883	DG506AAR-2	DG506AAR/883
DG191AP/883	DG191AP/883	DG308AAK/883	DG308AAK/883	DG506AAR/883	DG506AAR/883
DG200AAA-2	DG200AAA/883	DG309AK-2	DG309AK/883	DG506AAZ/883	DG506AAZ/883
DG200AAA/883	DG200AAA/883	DG309AK/883	DG309AK/883	DG507AAK-2	DG507AAK/883
DG200AAK-2	DG200AAK/883	DG381AAA-2	DG381AAA/883	DG507AAK/883	DG507AAK/883
DG200AAK/883	DG200AAK/883	DG381AAA/883	DG381AAA/883	DG507AAR-2	DG507AAR/883
DG200AAP-2	DG200AAP/883	DG381AAK-2	DG381AAK/883	DG507AAR/883	DG507AAR/883
DG200AAP/883	DG200AAP/883	DG381AAK/883	DG381AAK/883	DG507AAZ/883	DG507AAZ/883
DG201AAK-2	DG201AAK/883	DG384AAK-2	DG405AK/883	DG508AAK-2	DG508AAK/883
DG201AAK/883	DG201AAK/883	DG384AAK/883	DG405AK/883	DG508AAK/883	DG508AAK/883
DG201AAZ/883	DG201AAZ/883	DG387AAA-2	DG387AAA/883	DG508AAZ/883	DG508AAZ/883
DG201AK/883	DG201AK/883	DG387AAA/883	DG387AAA/883	DG509AAK-2	DG509AAK/883
DG202AK-2	DG202AK/883	DG387AAK-2	DG387AAK/883	DG509AAK/883	DG509AAK/883
DG202AK/883	DG202AK/883	DG387AAK/883	DG387AAK/883	DG509AAZ/883	DG509AAZ/883
DG221AK-2	DG221AK/883	DG390AAK-2	DG403AK/883	DG5140AK/883	DG5140AK/883
DG221AK/883	DG221AK/883	DG390AAK/883	DG403AK/883	DG5141AK/883	DG5141AK/883
DG243AK-2	DG243AK/883	DG400AK/883	DG400AK/883	DG5142AK/883	DG5142AK/883
DG243AK/883	DG243AK/883	DG401AK/883	DG401AK/883	DG5143AK/883	DG5143AK/883
DG271AK-2	DG271AK/883	DG401AZ	DG401AZ/883	DG5144AK/883	DG5144AK/883
DG271AK/883	DG271AK/883	DG401AZ/883	DG401AZ/883	DG5145AK/883	DG5145AK/883
DG271AZ/883	DG271AZ/883	DG402AK/883	DG402AK/883	DG534AP/883	DG534AP/883
DG281AA-2	DG181AA/883	DG403AK/883	DG403AK/883	DG535AP/883	DG535AP/883
DG281AA/883	DG181AA/883	DG403AZ	DG403AZ/883	DG536AM/883	DG536AM/883
DG281AP-2	DG181AP/883	DG403AZ/883	DG403AZ/883	DG538AP/883	DG538AP/883
DG281AP/883	DG181AP/883	DG404AK/883	DG404AK/883	DG540AP/883	DG540AP/883
DG284AP-2	DG184AP/883	DG405AK/883	DG405AK/883	DG541AK/883	DG541AK/883
DG284AP/883	DG184AP/883	DG405AZ	DG405AZ/883	DG542AK/883	DG542AK/883
DG287AA-2	DG187AA/883	DG405AZ/883	DG405AZ/883	DG548AK/883	DG548AK/883
DG287AA/883	DG187AA/883	DG411AK/883	DG411AK/883	DG548AZ/883	DG548AZ/883
DG287AP-2	DG187AP/883	DG411AZ/883	DG411AZ/883	DG601AP/883	DG601AP/883
DG287AP/883	DG187AP/883	DG412AK/883	DG412AK/883	DG841AM/883	DG841AM/883
DG290AP-2	DG190AP/883	DG412AZ/883	DG412AZ/883	DG908AK/883	DG908AK/883
DG290AP/883	DG190AP/883	DG413AK/883	DG413AK/883	DG908AZ/883	DG908AZ/883
DG300AAA-2	DG300AAA/883	DG413AZ/883	DG413AZ/883	D123AK/HR	D123AK/883
DG300AAA/883	DG300AAA/883	DG417AK/883	DG417AK/883	D123AL-2	D123AL/883
DG300AAK-2	DG300AAK/883	DG418AK/883	DG418AK/883	D123AL/883	D123AL/883
DG300AAK/883	DG300AAK/883	DG419AK/883	DG419AK/883	D123AP-2	D123AP/883
DG301AAA-2	DG301AAA/883	DG480AK/883	DG480AK/883	D123AP/883	D123AP/883
DG301AAA/883	DG301AAA/883	DG485AK/883	DG485AK/883	D125AK/HR	D125AK/883



## Class B /883 Compliant/Non JAN (Cont'd)

Industry Part #	Siliconix Part #	Industry Part #	Siliconix Part #	Industry Part #	Siliconix Part #
D125AL-2	D125AL/883	HI1-5041-8	DG5041AK/883	IH5144MJE/883	DG5144AK/883
D125AL/HR	D125AL/883	HI1-5042-8	DG5042AK/883	IH5145MJE/883	DG5145AK/883
D125AL/883	D125AL/883	HI1-5043-8	DG5043AK/883	L161AL-2	L161AL/883
D125AP-2	D125AP/883	HI1-5044-8	DG5044AK/883	L161AL/883	L161AL/883
D125AP/883	D125AP/883	HI1-5045-8	DG5045AK/883	L161AP-2	L161AP/883
D129AL-2	D125AL/883	HI1-506-8	DG506AAR/883	L161AP/883	L161AP/883
D129AL/HR	D129AL/883	HI1-506L-8	DG526AK/883	AD7541ASD/883	SI7541ASD/883
D129AL/883	D129AL/883	HI1-507-8	DG507AAR/883	IH5145MJE/883	SI7541ASE/883
D129AP-2	D129AP/883	HI1-507L-8	DG527AK/883	AD7541ATD/883	SI7541ATD/883
D129AP/HR	D129AP/883	HI1-508-8	DG508AAK/883	AD7541ATE/883	SI7541ATE/883
D129AP/883	D129AP/883	HI1-508L-8	DG528AK/883	AD7541SD/883	SI7541SD/883
D139AA-2	D139AA/883	HI1-509-8	DG509AAK/883	AD7541SE/883	SI7541SE/883
D139AP-2	D139AP/883	HI1-509L-8	DG529AK/883	AD7541TD/883	SI7541TD/883
D139AP/883	D139AP/883	HI2-200-8	DG200AAA/883	AD7541TE/883	SI7541TE/883
D169AK-2	D169AK/883	HI2-300-8	DG300AAA/883	AD7542SD/883	SI7542SD/883
D169AK/883	D169AK/883	HI2-301-8	DG301AAA/883	AD7542TD/883	SI7542TD/883
D169AP-2	D169AP/883	HI2-304-8	DG304AAA/883	AD7543SD/883	SI7543SD/883
D169AP/883	D169AP/883	HI2-305-8	DG305AAA/883	AD7543TD/883	SI7543TD/883
D469AP-2	D469AP/883	HI2-381-8	DG381AAA/883	AD7545UD/883	SI7545UD/883
D469AP/883	D469AP/883	HI2-387-8	DG387AAA/883	AD7545UE/883	SI7545UE/883
D470AP/883	D470AP/883	IH5040MJE/HR	DG5040AK/883	SI8603AK/883	SI8603AK/883
HI1-200-8	DG200AAK/883	IH5040MJE/883	DG5040AK/883	SI8604AK/883	SI8604AK/883
HI1-201-8	DG201AAK/883	IH5041MJE/HR	DG5041AK/883	SW-01BQ883	DG201AAK/883
HI1-300-8	DG300AAK/883	IH5041MJE/883	DG5041AK/883	SW-02BQ883	DG202AAK/883
HI1-301-8	DG301AAK/883	IH5042MJE/HR	DG5042AK/883	SW-05BK883	DG200AAA/883
HI1-302-8	DG302AAK/883	IH5042MJE/883	DG5042AK/883	SW-05BY883	DG200AAK/883
HI1-303-8	DG303AAK/883	IH5043MJE/HR	DG5043AK/883		
HI1-304-8	DG304AAK/883	IH5043MJE/883	DG5043AK/883		
HI1-305-8	DG305AAK/883	IH5044MJE/HR	DG5044AK/883		
HI1-306-8	DG306AAK/883	IH5044MJE/883	DG5044AK/883		
HI1-307-8	DG307AAK/883	IH5045MJE/HR	DG5045AK/883		
HI1-381-8	DG381AAK/883	IH5045MJE/883	DG5045AK/883		
HI1-384-8	DG405AK/883	IH5140MJE/883	DG5140AK/883		
HI1-387-8	DG387AAK/883	IH5141MJE/883	DG5141AK/883		
HI1-390-8	DG403AK/883	IH5142MJE/883	DG5142AK/883		
HI1-5040-8	DG5040AK/883	IH5143MJE/883	DG5143AK/883		

# BURN-IN CONNECTIONS

Part Type	Package Type	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
D125	P/L	-30V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K-GND				
D129	P/L	(7)	(7)	(7)	GND	(7)	(7)	10K+5V	GND	-30V	(13)	(13)	(13)	10K+5V	+5V				
D139 D169	P/L	---	N/C	10K-Pin 3	10K-Pin 4	+5V	+10V	+5V	GND	-20V	GND	10K-Pin 12	N/C	N/C					
D469		GND	+10V	GND	+10V	+10V	GND	GND	+10V	GND	N/C	N/C	N/C	N/C	+10V				
DG123	P/L	GND	GND	GND	-20V	4.7K+5V	4.7K+5V	4.7K+5V	4.7K+5V	4.7K+5V	GND	+5V	GND	GND	GND				
DG125	P/L	GND	GND	GND	-20V	GND	GND	GND	GND	GND	+5V	+5V	GND	GND	GND				
DG126 DG129	P/L	10K-GND	+10V	10K-GND	---	+10V	10K-GND	10K-GND	+10V	GND	GND	+10V	-20V	GND	+10V				
DG133 DG134	P/L	10K-GND	+10V	10K-GND	---	+10V	10K-GND	10K-GND	+10V	GND	GND	+10V	-20V	GND	+10V				
DG139 DG140	P/L	10K-GND	+10V	10K-GND	---	+10V	10K-GND	10K-GND	+10V	GND	GND	+10V	-20V	GND	+10V				
DG141		10K-GND	10V	10K-GND	---	10V	10K-GND	10K-GND	10V	GND	GND	10V	-20V	GND	10V				
DG142 DG143	P/L	10K-GND	+10V	10K-GND	---	+10V	10K-GND	10K-GND	+10V	GND	GND	+10V	-20V	GND	+10V				
DG144 DG145	P/L	10K-GND	+10V	10K-GND	---	+10V	10K-GND	10K-GND	+10V	GND	GND	+10V	-20V	GND	+10V				
DG146	P/L	10K-GND	+10V	10K-GND	---	+10V	10K-GND	10K-GND	+10V	GND	GND	+10V	-20V	GND	+10V				
DG172	P/L	To pin 14	GND	GND	---	-20V	GND	+5V	+5V	+5V	+5V	GND	+5V	To pin 14	7.5K-20V				
DG180 DG181	A	+15V	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND	+15V								
DG180 DG181	P/L	+15V	10K-GND	---	---	GND	+15V	+5V	GND	-15V	GND	---	---	10K-GND	+15V				
DG182	P/L	+15V	10K-GND	---	---	GND	+15V	+5V	GND	-15V	GND	---	---	10K-GND	+15V				
DG182 DG186	A	+15V	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND	+15V								
DG183 DG184 DG185	L	-15V	10K-GND	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V	10K-GND	10K-GND	-15V				
DG183 DG184 DG185	P	10K-GND	---	10K-GND	-15V	-15V	10K-GND	---	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V		
DG184	P	-15V	10K-GND	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V	10K-GND	10K-GND	-15V				
DG185	P	-15V	10K-GND	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V	10K-GND	10K-GND					
DG186 DG187 DG188	P/L	-15V	10K-GND	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V	10K-GND	10K-GND	-15V				
DG187 DG188	A	+15V	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND	+15V								
DG189 DG190 DG191	L	-15V	10K-GND	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V	10K-GND	10K-GND	-15V				
DG189 DG190 DG191	P	10K-GND	---	10K-GND	-15V	-15V	10K-GND	---	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V		

# BURN-IN CONNECTIONS

Part Type	Package Type	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG200	A	+15V	+15V	GND	(9)	(9)	-15V	--	(9)	10K-GND	+15V								
DG200A	P/L	+15V	--	GND	--	(10)	(10)	-15V	--	(10)	10K-GND	--	+15V	--	+15V				
DG201 DG201A	P/L	+15V	(15)	(15)	-15V	GND	(15)	(15)	+15V	+15V	(15)	(15)	--	+15V	(15)	10K-GND	+15V		
DG202		+15V	10K-GND	10K-GND	-15V	GND	10K-GND	10K-GND	+15V	+15V	10K-GND	10K-GND	N/C	+15V	10K-GND	10K-GND	+15V		
DG211	P	+15V	(15)	(15)	-15V	GND	(15)	(15)	+15V	+15V	(15)	(15)	+5V	+15V	(15)	10K-GND	+15V		
DG212		-15V	10K-GND	10K-GND	-15V	GND	10K-GND	10K-GND	-15V	-15V	10K-GND	10K-GND	+5V	+15V	10K-GND	10K-GND	-15V		
DG221		15V	10K-GND	10K-GND	-15V	GND	10K-GND	10K-GND	15V	15V	10K-GND	10K-GND	-15V	15V	10K-GND	10K-GND	15V		
DG243		(16)	--	(16)	(16)	(16)	(16)	--	(16)	(16)	GND	15V	5V	GND	-15V	GND	10K-GND		
DG271		+15V	10K-GND	10K-GND	-15V	GND	10K-GND	10K-GND	+15V	+15V	10K-GND	10K-GND	N/C	+15V	10K-GND	10K-GND	+15V		
DG300A	A	(9)	(9)	GND	--	GND	-15V	GND	(9)	10K-GND	+15V								
DG300A	P/L	--	(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
DG301A	A	(9)	(9)	GND	--	GND	-15V	GND	(9)	10K-GND	+15V								
DG301A	P/L	--	(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
DG302A	P/L	--	(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
DG303A	P/L	--	(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
DG304A	A	(9)	(9)	GND	--	GND	-15V	GND	(9)	10K-GND	+15V								
DG304A	P/L	--	(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
DG305A	A	(9)	(9)	GND	--	GND	-15V	GND	(9)	10K-GND	+15V								
DG305A	P/L	--	(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
DG306A	P	(9)	(9)	GND	--	GND	-15V	GND	(9)	10K-GND	+15V								
DG306A	P/L		(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
DG307A	P	(9)	(9)	GND	--	GND	-15V	GND	(9)	10K-GND	+15V								
DG307A	P/L		(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
DG308A	P	+15V	(15)	(15)	-15V	GND	(15)	(15)	+15V	+15V	(15)	(15)	--	+15V	(15)	10K-GND	+15V		
DG309		-15V	(15)	(15)	-15V	GND	(15)	(15)	-15V	-15V	(15)	(15)	--	(15)	(15)	10K-GND	-15V		
DG381A	A	+15V	10K-GND	N/C	N/C	GND	+15V	+5V	GND	-15V	GND	N/C	N/C	10K-GND	+15V				
DG381A	P	+15V	10K-GND	--	--	GND	+15V	+5V	GND	-15V	GND	--	--	10K-GND	+15V				

# BURN-IN CONNECTIONS

Part Type	Package Type	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG384A	L	-15V	10K-GND	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V	10K-GND	10K-GND	-15V				
DG384A	P	10K-GND	---	10K-GND	-15V	-15V	10K-GND	---	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V		
DG387A	P	-15V	10K-GND	10K-GND	+15V	GND	+15V	+5V	GND	-15V	GND	+15V	10K-GND	10K-GND	-15V				
DG390A	P	10K-GND		10K-GND	-15V	-15V	10K-GND		10K-GND	+15V	GND	+15V	+5 V	GND	-15V	GND	+15V		
DG400		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG401		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG402		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG403		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG404		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG405		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG411	P	+15V	(15)	(15)	-15V	GND	(15)	(15)	+15V	+15V	(15)	(15)	+5V	+15V	(15)	10K-GND	+15V		
DG417	K	10K-GND	N/C	GND	+15V	+5V	+15V	-15V	(3)										
DG421		10K-GND	GND	10K-GND	10K-GND	10K-GND	10K-GND	GND	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG423		10K-GND	GND	10K-GND	10K-GND	10K-GND	10K-GND	GND	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG425		10K-GND	GND	10K-GND	10K-GND	10K-GND	10K-GND	GND	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG501 DG503 S13705	P/L	(16)	(4)	(4)	+10V	(12)	(12)	(12)	(12)	(12)	(12)	(12)	-10V	-15V	(16)	(16)	GND		
DG508A	P/L	GND	GND	-15V	(12)	(12)	(12)	(12)	(12)	(12)	(12)	(12)	10K-GND	+15V	GND	GND	GND		
DG509A	P/L	GND	GND	-15V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10K-GND	+15V	GND	GND			
DG528	P	GND	GND	GND	-15V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10K-GND	+15V	GND	GND	GND	GND	
DG529	P	GND	GND	GND	-15V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K-GND	+15V	GND	GND	GND		
DG568		GND	GND	10K-+15V	-60	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10K-GND	10K-+60	GND	GND	GND	GND	
DG569		GND	GND	10K-+15V	10K-60	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K-GND	10K-+60	GND	GND	GND		
DG5040 DG5041	P	10K-GND	---	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG5042 DG5043	P	10K-GND	---	10K-GND	10K-GND	10K-GND	10K-GND	---	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG5044 DG5045	P	10K-GND	---	10K-GND	10K-GND	10K-GND	10K-GND	---	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG5140		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		

# BURN-IN CONNECTIONS

Part Type	Package Type	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG5141		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG5142		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG5143		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG5144		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DG5145		10K-GND	N/C	10K-GND	10K-GND	10K-GND	10K-GND	N/C	10K-GND	10K-GND	GND	+15V	+5V	GND	-15V	GND	10K-GND		
DGP303	P/L	—	(13)	(13)	(13)	(13)	GND	GND	-15V	GND	(13)	(13)	(13)	10K-GND	+15V				
G118	P/L	-15V	-15V	-15V	-15V	-15V	-15V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K-+10V			
G119	P/L	(14)	(14)	-15V	-15V	-15V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10K-+10V			
L144	P/L	3M $\Omega$ +15V	(13)	(11)	GND	GND	(9)	—	—	(6)	220-15V	(3)	GND	(2)	220-+15V				
L161	P	-15V	+15V	-15V	+15V	-15V	+15V	-15V	+15V	-15V	—	—	—	—	—	3M $\Omega$ +15V	+15V		
LD110		3K-5V	3K-5V	3K-5V	3K-5V	6K-5V	18 $\Omega$ 5V	100 $\Omega$ 5V	GND	18K-5V	30K-5V	18 $\Omega$ 5V	GND	3K-5V	3K-5V	3K-5V			
LD111		N/C	GND	+15V	GND	10K-+15	-15V	GND	N/C	Pin 11	GND	Pin 9	N/C	-1.36V	-15V	GND	+15V		
LD121		(18)	(18)	5V	GND	5K-5V	5K-5V	—	20K/200K-15V	(18)	(18)	(18)	(18)	(18)	5V	-15V	(18)	(18)	2.5K-5V
SI3002		N/C	N/C	N/C	Pin 9	GND	-20V	GND	GND	Pin 4	+10V								
SI7240		GND	GND	GND	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	1K-15V	10V	10V
SI7250		N/C	GND	N/C	N/C	N/C	N/C	N/C	GND	N/C	N/C	N/C	N/C	N/C	N/C	N/C	12V		
SI7541		GND	GND	GND	16	16	16	16	16	16	16	16	16	16	16	16	1K-+15V	+10V	+10V
SI7541A		GND	GND	GND	16	16	16	16	16	16	16	16	16	16	16	16	1K-+15V	+10V	+10V
SI7542		GND	GND	GND	GND	GND	1K-5V	1K-5V	GND	GND	1K-5V	1K-5V	GND	1K-5V	1K-5V	1K-5V	1K-5V		
SI7543		GND	GND	GND	GND	GND	1K-5V	1K-5V	GND	GND	1K-5V	1K-5V	GND	1K-5V	1K-5V	1K-5V	1K-5V		
SI7652		.1 $\mu$ F To Pin 8	.1 $\mu$ F To Pin 8	N/C	Pin 10	910 $\Omega$ To 10K To GND	N/C	680 $\Omega$ GND	.1 $\mu$ F To Pin 2	N/C	Pin 4	+15	N/C	N/C	N/C				
SI7660		—	—	GND	—	1K-5V	—	—	1K-5V										
SI7661		N/C	N/C	GND	N/C	1K-15V	N/C	N/C	1K-15V										
SI8603		+5V	CLK	5.6K-15V	5.6K-15V	5.6K-15V	5.6K-15V	5.6K-15V	Plns (11) (16)	GND	GND	+5V	Plns (16) (17)	5.6K-GND	5.6K-GND	5.6K-GND	5.6K-GND	22K-GND (11) (7)	
SI8604		+5V	CLK	5.6K-15V	5.6K-15V	5.6K-15V	5.6K-15V	5.6K-15V	Plns (11) (16)	GND	GND	+5V	Plns (16) (17)	5.6K-GND	5.6K-GND	5.6K-GND	5.6K-GND	22K-GND (11) (7)	

# BURN-IN CONNECTIONS

Part/ Pkg Type	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	
D470 28 Pin CDIP	(2)	+5V	+15V	(18)	-15V	(18)	+15V	(18)	-15V	(18)	+15V	+15V	GND	GND	10K GND	-15V	+15V	10K GND	-15V	(18)	+15V	(18)	
	-15V	(18)	+15V	NC	GND	GND																	
DF412/P	+5V	10K 2.5V	10K 2.5V	10K 2.5V	430 Ω 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V
	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V	GND	GND	GND	+5V	GND	+5V	GND	+5V	GND	400 pf- +5V	10K 2.5V	10K 2.5V	10K 2.5V	10K 2.5V					
DG506 DG506A	+15V	(28)		(28)	(28)	(28)	(28)	(28)	(28)	(28)	(28)	GND		GND	GND	GND	GND	GND	(28)	(28)	(28)	(28)	
	(28)	(28)	(28)	(28)	-15V	10K GND																	
DG507A/R	15V	10K GND	---	(2)	(2)	(2)	(2)	(2)	(2)	(2)	(2)	GND	---	GND	GND	GND	GND	GND	(2)	(2)	(2)	(2)	
	(2)	(2)	(2)	(2)	-15V	(2)																	
DG526	15V	(28)	GND	(28)	(28)	(28)	(28)	(28)	(28)	(28)	(28)	GND	GND	GND	GND	GND	GND	GND	(28)	(28)	(28)	(28)	
	(28)	(28)	(28)	(28)	-15V	10K GND																	
DG527	15V	(28)	GND	(28)	(28)	(28)	(28)	(28)	(28)	(28)	(28)	GND	GND	GND	GND	GND	GND	GND	(28)	(28)	(28)	(28)	
	(28)	(28)	(28)	(28)	-15V	10K GND																	
DG535	GND	18	18	18	18	18	18	18	18	18	18	GND	GND	GND	GND	GND	GND	18	18	10K- GND	18	18	
	18	18	18	18	18	10K +15V																	
DG536	10K +15V	GND	10K +15V	GND	10K +15V	GND	10K +15V	10K +15V	GND	GND	GND	GND	GND	GND	10K +15V	10K +15V	10K GND	GND	10K +15V	GND	10K +15V	GND	
DG566/ SB/J PLCC	(28)	(28)			(28)	(28)	(28)	(28)	(28)	(28)	10K 60V	10K 60V	(19)	(19)	(19)	(19)	(19)	(19)	GND	(28)	(28)	(28)	
	(28)	(28)	(28)		(28)	10K GND																	
SI2504	N/C	1.5K GND	PIN 14	1.5K GND	1.5K GND	1.5K GND	1.5K GND	1.5K GND	1.5K GND	N/C	+S	GND	CLK 2KHZ	Pin 3	N/C	1.5K GND	1.5K GND	1.5K GND	1.5K GND	1.5K GND	1.5K GND	1.5K GND	N/C
	1.5K GND	+5V																					
SI7135	100 Ω	400K +5 100K GND	GND	1.5 μF GND	.1μF GND	6.8m Ω	.1μF To pin 8	.1μF To pin 7	GND	400K +5 100K GND	100 Ω	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	20K To Pin 26	N/C	+5 Clk	
	N/C	GND	20K +5V	20K Pin 20	N/C	N/C	N/C																
SI7545	GND	GND	GND	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15	15
SI8601	+5V	8KHZ Clk	5.6K 5V	5.6K 5V	5.6K 5V	5.6K 5V	22K GND	GND	GND	GND	GND	GND	+5V	+5V	+5V	+5V	+5V	GND	+5V	GND	(7)	+5V	(7)
SI8602	+15V	+15V Clk	5.6K +15V	5.6K +15V	5.6K +15V	5.6K +15V	(27)	GND	GND	GND	GND	GND	+15V	+15V	+15V	+15V	GND	+15V	GND	(27)	+10V	(27)	
	5.6K GND	5.6K GND	5.6K GND	5.6K GND	22K GND	GND																	







# PROCESS OPTION FLOW CHARTS

## Military and Extended Hi-Rel

- Column I:** The first column identifies Siliconix' MIL-M-38510 Compliant JAN, Class B, process flow option. MIL-M-38510 JAN product will be processed in accordance with the applicable detail slash sheet requirements.
- Column II:** The /883 Compliant/Non-JAN, Class B process flow meets the requirements of MIL-STD-883, paragraph 1.2.1. Devices which are processed to this flow are identified within the generic part number suffix as /883.
- Column III:** The Extended Hi-Rel 1 flow offers customers, with Space type requirements, the option of a Space Rated flow for generation of specification control drawings.
- Column IV:** The Extended Hi-Rel 2 flow is offered to customers that can accept product that has SEM and a 240 hour static burn-in.

**PROCESS OPTION FLOW CHART**

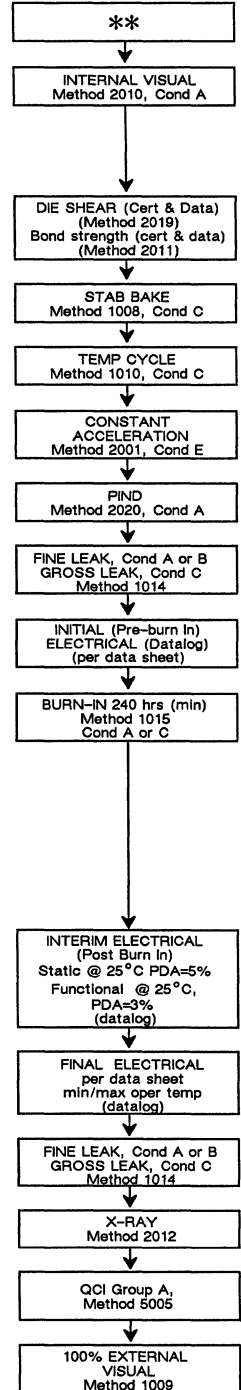
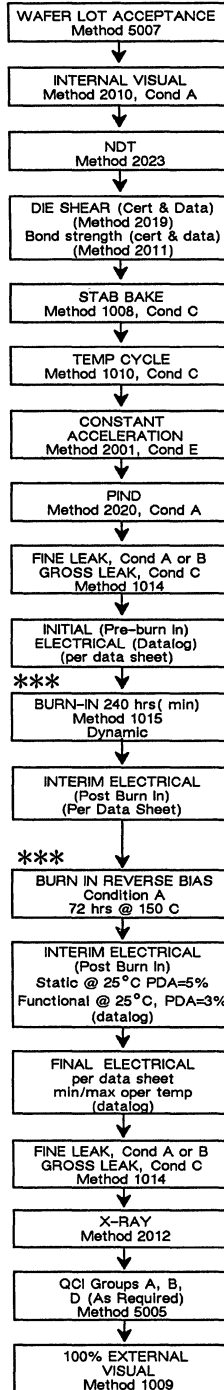
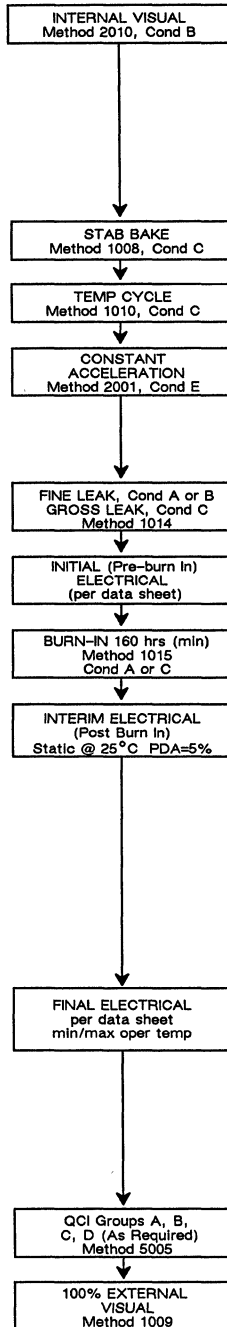
MIL-M-38510 JAN  
Class B

/883 Compliant/Non-JAN  
\* Method 5004/5005

Extended HI/Rel 1

Extended HI/Rel 2

P  
E  
R  
S  
L  
A  
S  
H  
S  
H  
E  
E  
T



\* MIL-STD-883  
The latest revision of  
MIL-STD-883 at time  
of order is applicable.

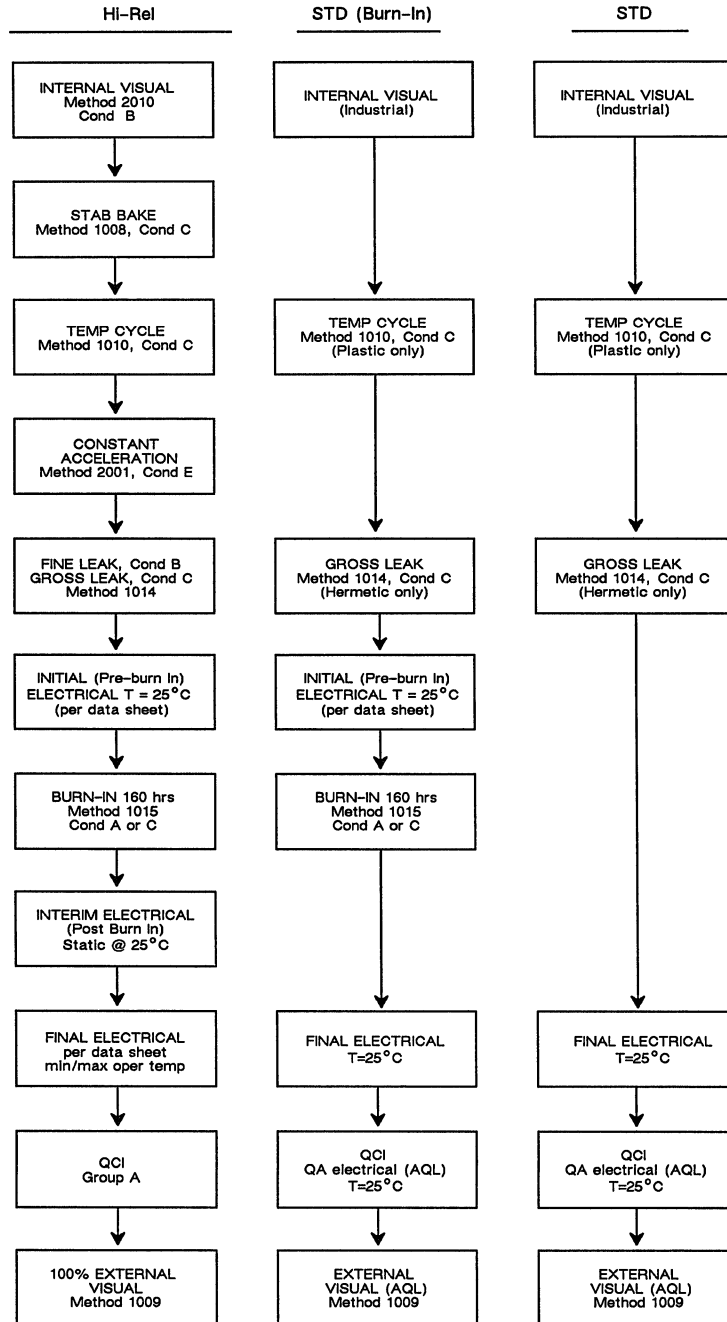
\*\* Available Option SEM

\*\*\* Dual burn-in may be  
performed in reverse.

## Hi-Rel and Standard Flow

- Column I:** This flow is for Military/Aerospace/Industrial customers that can use a noncompliant/non-JAN device in their equipment, while gaining the advantage of environmental and infant mortality screening.
- Column II:** The standard flow outlined within this column is intended for plastic and hermetic packages with burn-in.
- Column III:** The standard flow outline within this column is intended for plastic and hermetic packages without burn-in.

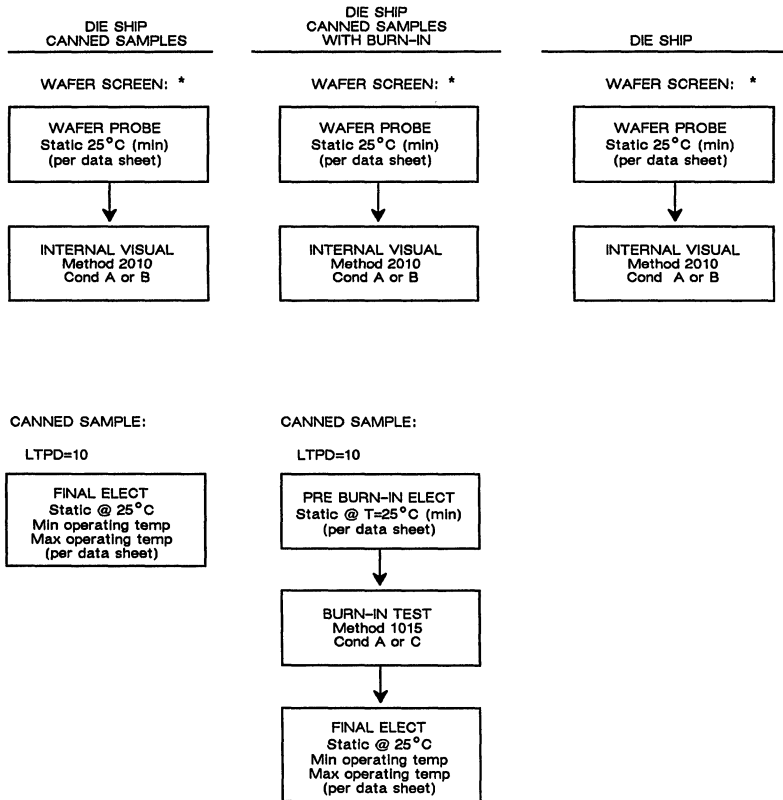
**PROCESS OPTION FLOW CHART**



# Die Shipments

- Column I:** This flow offers customers the option of assembling canned sample to verify the die are capable of meeting the military temperature range, electrical test limits. Die Attach and Bond Strength will also be performed to insure assembly operation.
- Column II:** Column II is the same as die/canned sample flow with burn-in added for confidence that die samples do not shift across this screen. Die Attach and Bond Strength will also be performed to insure assembly operation.
- Column III:** This column identifies Siliconix' die shipment option without canned samples.

### PROCESS OPTION FLOW CHART



\* Available Option SEM

# Die Process Information

Siliconix is a large-volume supplier of dice to the hybrid industry. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

## PHYSICAL DATA

Physical layout and dimensions are presented in the Die Topography section. Dimensions are shown as  $\frac{\text{Inches}}{(\text{mm})}$ . Dice are supplied to length and width dimensions which have an accuracy of  $\pm 3$  mils. Thickness will be  $15 \pm 1$  mils for integrated circuit die with gold backing, and  $21 \pm 1$  mils without gold backing, and  $8 \pm 2$  mils for FETs.

Bonding pad location may be identified from the die topography shown. Contact factory for ordering information. Each die or wafer is passivated with approximately  $8000 \text{ \AA}$  of either silicon nitride or non-crystalline glass. FET chips are supplied with gold backing; gold backing is available as an option for integrated circuits. Die metallization is deposited aluminum approximately  $12000 \text{ \AA}$  thick.

## DIE SCREENING CRITERIA

**Electrical Probe** -- All dice are 100% probed in wafer form at  $25^\circ\text{C}$  to DC parameters as shown on the wafer test limits specification (available upon request). Hot chuck is also available at additional cost.

**Visual Criteria** -- Each die receives a visual inspection to MIL-STD-883, Method 2010, Condition B criteria. Siliconix QC Department samples each lot to an LTPD of 10%. Alternative visual criteria, including Method 2010, Condition A, or Siliconix industrial criteria are available as options.

## PACKAGING

Die are supplied in dust-proof, anti-static waffle packs (see illustration - Figure 1)

## ASSEMBLY

The customer's interests will best be served if static sensitivity handling procedures are used.

## PART NUMBER DESIGNATIONS

See ordering information.

## OPTIONS

(Price will be quoted upon request.)

**SEM** -- Scanning electron microscope examination and control in accordance with MIL-STD-883 Method 2018 can be ordered on die and wafers. SEM wafer qualification should be specified as a separate line item on a request for quote.

**Wafer Qualification to Unprobed Parameters** -- Sample testing of purchased die to demonstrate capability to perform at data sheet temperature extremes or to switching times test limits by use of LTPD techniques can be provided at additional cost.

Visual inspection to customer generated specifications can be provided.

**Gold Backing** -- IC dice may be purchased with gold alloyed to the backside. This is a special order item. Gold thickness would be as follows:

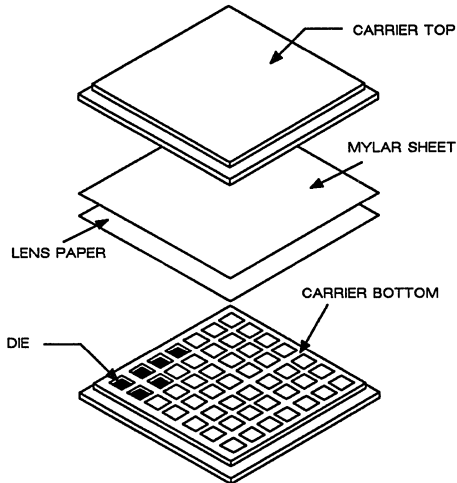
FETs (NC, NIP)       $1500 \text{ \AA}$  minimum

ICs (all)               $3500 \text{ \AA}$  minimum

**Hot Chuck** -- Siliconix can perform wafer sort at the high-temperature limit, at additional cost.

## CHIP PACKAGING

Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading and unloading and it also prevents die from rotating within the cavity.



NOTE: CARRIER TOP & BOTTOM SECURED BY CLIPS

Figure 1

### MULTI-CHIP DIE TOPOGRAPHY INFORMATION

Some of Siliconix's analog switches are of multi-chip design with inter-chip connections. For example, the

DG190 consists of a separate driver chip (CMJB) and four separate JFET transistors (NCB). Figure 2 illustrates the bonding diagram arrangement in the DIP package. The driver and the JFET switches are mounted so that the substrates are electrically isolated. The substrate of the driver is at the negative supply voltage while the substrate of the JFET switches is the gate connection. A pattern-bottom side braze package is used to connect the driver to the JFET gate.

The pin connections for the JFET switch chips can be determined from the chip section and switch chips can be determined from the chip section and switch pin-out in the data sheet.

### Die Diagrams/Dimensions

The negative image photos show the metallization pattern. Scale is normally 20x. Bonding pads are 4 mil (0.10 mm) square, glass-free aluminum metallization. Pad identification numbers usually correspond to pin numbers for the dual-in-line package on data sheets.

Wafer test limits are available upon request.

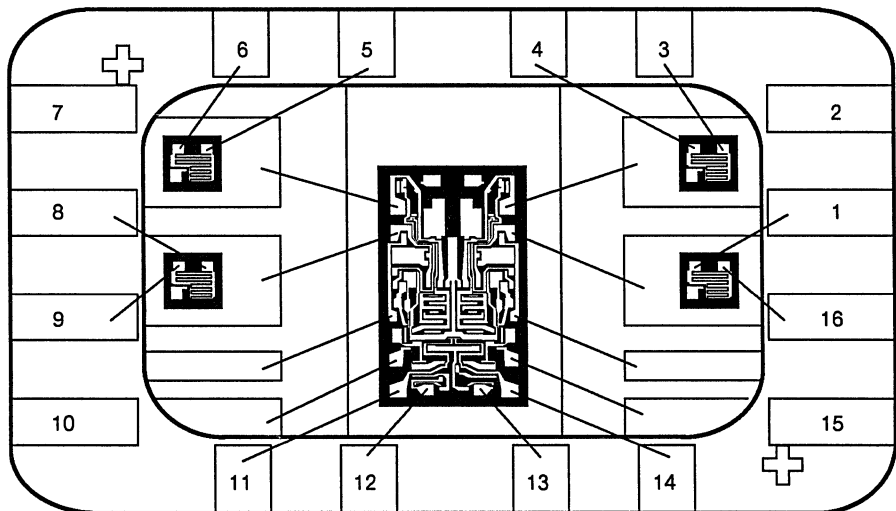
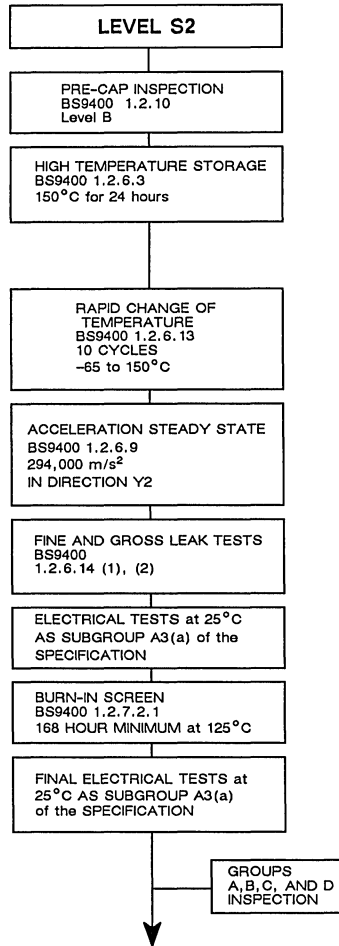


Figure 2. DG190 JFET Analog Switch



# BS9000 Series Process Option Flow Chart



2

**INSPECTION REQUIREMENTS:** All tests performed at  $T_{amb} = 25^{\circ}\text{C}$  unless otherwise specified.

## 100% SCREENING TEST PROCEDURES

Production batches containing greater than 10% defective units subsequent to burn-in will not be issued for release.

For complete details of screening and inspection refer to the appropriate detail specification available on request from your nearest Siliconix sales offices.







# ANALOG SWITCH SELECTOR CHART

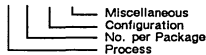
SWITCHING SPEED  $t_{(on)}$  OR  $t_{(off)}$ , WHICHEVER IS GREATER

r<sub>DS(on)</sub> - Drain-to-Source ON-Resistance

	10 ns	20/35 to 60/75 ns	125/150 ns	200 ns	250 ns	300 ns	500/600 ns	750 ns	1µs	1.5/1.6µs	2/2.5µs
175 Ω							DG201A (C, Q, SS) DG202 (C, Q, SS) DGP201A(C, Q, SS)	DG172 (P, S, CD, r)	DG211 (C, Q, SS) DG212 (C, Q, SS)	SI3002 (P, S, SD, r)	DG123 (P, S, CD, r) DG125 (P, S, CD, r)
100 Ω			DG441 (C, Q, SS) DG442 (C, Q, SS) DG444 (C, Q, SS) DG445 (C, Q, SS)	DG308A (C, Q, SS) DG309 (C, Q, SS)			DG221(C, Q, SS, L)				
80 Ω		DG540 (D, Q, SS) DG541 (D, Q, SS) DG542 (D, Q, SS)			DG182 (J, D, SS) DG185 (J, D, DS) DG188 (J, S, SD) DG191 (J, D, SD)				DG200A (C, D, SS)	DG126 (J, D, DS) DG134 (J, D, SS) DG142 (J, D, DD) DG143 (J, S, SD)	Radiation Resistant
50 Ω	SD210 (D, S, SS, r) SD211 (D, S, SS, r) SD212 (D, S, SS, r) SD213 (D, S, SS, r) SD214 (D, S, SS, r) SD215 (D, S, SS, r) SD2100(D, S, SS, r) SD2110(D, S, SS, r) SD2120(D, S, SS, r)	DG271 (C, Q, SS)	DG5140 (C, S, SS) DG5141 (C, D, SS)	DG5142 (C, S, SD) DG5143 (C, D, SD) DG5144 (C, S, DS) DG5145 (C, D, DS)	DG304A (C, D, SS) DG305A (C, S, SD) DG306A (C, D, DS) DG307A (C, D, SD) DGP303A(C, D, SD)	DG300A (C, D, SS) DG301A (C, S, SD) DG302A (C, D, DS) DG303A (C, D, SD) DG381A (C, D, SS) DG384A (C, D, DS) DG387A (C, S, SD) DG390A (C, D, SD)	DG5048 (C, D, SS) DG5049 (C, D, SS) DG5050 (C, S, SD) DG5051 (C, D, SD)		DG243(C, D, SD, M)		DG566 (H, 8, SS, r)
30 Ω	SD5000(D, Q, SS, r) SD5001(D, Q, SS, r) SD5002(D, Q, SS, r) SD5400(D, Q, SS, r) SD5401(D, Q, SS, r) SD5402(D, Q, SS, r) SD5200(D, Q, SS, r)	DG601 (L, Q, SS)	DG181 (J, D, SS) DG184 (J, D, DS) DG187 (J, S, SD) DG190 (J, D, SD)							DG129 (J, D, DS) DG133 (J, D, SS) DG139 (J, D, DD) DG144 (J, S, SD)	Radiation Resistant
25 Ω	SI2200(D, S, SS, r) SI2400(D, S, SS, r)		DG400 (C, S, SS) DG401 (C, D, SS) DG402 (C, S, SD) DG403 (C, D, SD) DG404 (C, S, DS) DG405 (C, D, DS) DG411 (C, Q, SS) DG412 (C, Q, SS) DG413 (C, Q, SS) DG417 (C, S, SS) DG418 (C, S, SS) DG419 (C, SD, S) DG421 (C, D, SS, L) DG423 (C, D, SD, L) DG425 (C, D, DS, L)								
10 Ω						DG180 (J, D, SS) DG183 (J, D, DS) DG186 (J, S, SD) DG189 (J, D, SD)				Radiation Resistant	DG140 (J, D, DS) DG141 (J, D, SS) DG145 (J, D, DD) DG146 (J, S, SD)

**Parenthesis Information**

( C, Q, SS, L )



**Process**

C = Plus-40 CMOS or 44 V Si-Gate  
 D = DMOS or D/CMOS  
 J = JFET  
 P = PMOS  
 H = High Voltage (D/CMOS)  
 L = Low Voltage CMOS (PolyMOS)

**No. per Package**

S = Single (1 per package)  
 D = Dual (2 per package)  
 Q = Quad (4 per package)  
 8 = Eight per package

**Configuration**

SS = Single-Pole Single-Throw  
 SD = Single-Pole Double-Throw  
 DS = Double-Pole Single-Throw  
 DD = Double-Pole Double-Throw  
 CD = Common Drain

**Miscellaneous**

r = r<sub>DS(ON)</sub> is a function of drive voltage  
 M = Make-Before-Break  
 L = Latchable Inputs



# ANALOG SWITCHES

Functional Configuration	Basic Part Number	Switch Type	r <sub>DS(on)</sub> MAX (Ω) (2)	I <sub>S(off)</sub> MAX2 nA	Supply Voltage			Volt. Range (2)	Switching Time (ns MAX)		MAX Supp. Range	Analog Voltage Range (V)	Logic Input for ON Switch	Levels		Comments	Package and Temperature Range Offerings:								
					V+	V-	V <sub>L</sub> (3)		t <sub>on</sub>	t <sub>off</sub>				V <sub>INL</sub>	V <sub>INH</sub>		Plastic DIP	Plastic SO	CerDIP	Side Braze	LCC	Flat Pack	Metal Can		
1 Ch. SPST	DG417	CMOS + 40	35	0.25	15	-15	5	30	175	145	44	V+ to V-	0	0.8	2.4	Mini DIP, Low Power	DJ	DY							
1 Ch. SPST	DG418	CMOS + 40	35	0.25	15	-15	5	30	175	145	44	V+ to V-	1	0.8	2.4	Mini DIP, Low Power	DJ	DY							
1 Ch. SPST	DG400	CMOS + 40	25	0.25	15	-15	5	30	175	145	44	V+ to V-	1	0.8	2.4	Low Power, High Perf.	DJ		AK						
1 Ch. SPST	DG5140	CMOS + 40	30	0.50	15	-15	5	30	200	125	44	V+ to V-	1	0.8	2.4	Use DG400 for New Designs	CJ		AK, CK						
1 Ch. SPST	DG5040	CMOS + 40	50	1.00	15	-15	5	30	1000	500	44	V+ to V-	1	0.8	2.4	Use DG400 for New Designs	CJ		AK, CK						
2 Ch. SPST	DG401	CMOS + 40	25	0.25	15	-15	5	30	125	75	44	V+ to V-	1	0.8	2.4	Low Power, High Perf.	DJ		AK		AZ				
2 Ch. SPST	DG421	CMOS + 40	35	0.25	15	-15	5	30	175	145	44	V+ to V-	1	0.8	2.4	On Board Latches	DJ		AK						
2 Ch. SPST	DG5048	CMOS + 40	25	0.50	15	-15	5	30	125	75	44	V+ to V-	1	0.8	2.4	Low Charge Injection	DJ		AK						
2 Ch. SPST	DG5141	CMOS + 40	30	0.50	15	-15	5	30	200	125	44	V+ to V-	1	0.8	2.4	Use DG401 for New Designs	CJ		AK, CK						
2 Ch. SPST	DG181	N-JFET	30	1.00	10	-20	5	20	150	130	36	(V+) to (V-)+7.5	0	0.8	2.0	Use DG401 for New Designs				AP, BP		AL	AA, BA		
2 Ch. SPST	DG181	N-JFET	30	1.00	15	-15	5	15	150	130	36		0	0.8	2.0	Use DG401 for New Designs				AP, BP		AL	AA, BA		
2 Ch. SPST	DG133	N-JFET	30	1.00	12	-18		20	600	1600	36	(V+)-2 to (V-)+8	1	0.8	2.5	Use DG401 for New Designs				AP, BP		AL			
2 Ch. SPST	DG304A	CMOS + 40	50	1.00	15	-15		30	250	150	44	V+ to V-	1	3.5	11.0	JAN Qualified	CJ		AK, BK, CK						
2 Ch. SPST	DG381A	CMOS + 40	50	1.00	15	-15		30	300	250	44	V+ to V-	0	0.8	4.0	Use DG401 for New Designs	CJ		AK, BK, CK				AA, BA, CA		
2 Ch. SPST	DG300A	CMOS + 40	50	1.00	15	-15		30	300	250	44	V+ to V-	1	0.8	4.0	JAN Qualified	CJ		AK, BK, CK				AA, BA, CA		
2 Ch. SPST	DG5041	CMOS + 40	50	1.00	15	-15	5	30	1000	500	44	V+ to V-	1	0.8	2.4	Use DG401 for New Designs	CJ		AK, CK				AA, BA, CA		
2 Ch. SPST	DG182	N-JFET	75	1.00	10	-20	5	20	250	130	36	(V+) to (V-)+5	0	0.8	2.0	Use DG401 for New Designs				AP, BP		AL	AA, BA		
2 Ch. SPST	DG182	N-JFET	75	1.00	15	-15	5	20	250	130	36		0	0.8	2.0	Use DG401 for New Designs				AP, BP		AL	AA, BA		
2 Ch. SPST	DG134	N-JFET	80	1.00	12	-18		20	600	1600	36	(V+)-2 to (V-)+5	1	0.8	2.5	Use DG401 for New Designs				AP, BP		AL			
2 Ch. SPST	DG180	N-JFET	10	10.00	10	-20	5	20	300	250	36	(V+) to (V-)+7.5	0	0.8	2.0	Use DG401 for New Designs				AP, BP		AL	AA, BA		
2 Ch. SPST	DG180	N-JFET	10	10.00	15	-15	5	15	300	250	36		0	0.8	2.0	Use DG401 for New Designs				AP, BP		AL	AA, BA		
2 Ch. SPST	DG141	N-JFET	10	10.00	12	-18		20	1000	2500	36	(V+)-2 to (V-)+8	1	0.8	2.5	Use DG401 for New Designs				AP, BP		AL			
2 Ch. SPST	DG200A	CMOS + 40	70	2.00	15	-15		30	1000	500	44	V+ to V-	0	0.8	2.4	JAN Qualified	CJ		AK, BK, CK				AA, BA, CA		
4 Ch. SPST	DG411	CMOS + 40	35	0.25	15	-15	5	30	175	145	44	V+ to V-	0	0.8	2.4	Low Power, High Perf.	DJ	DY	AK						
4 Ch. SPST	DG412	CMOS + 40	35	0.25	15	-15	5	30	175	145	44	V+ to V-	1	0.8	2.4	Low Power, High Perf.	DJ	DY	AK						
4 Ch. SPST	DG413	CMOS + 40	35	0.25	15	-15	5	30	175	145	44	V+ to V-	Note (6)	0.8	2.4	Low Power, High Perf.	DJ	DY	AK						
4 Ch. SPST	DG441	CMOS + 40	175	0.25	15	-15		30	175	145	44	V+ to V-	0	0.8	2.4	DG201A Upgrade	DJ	DY	AK						
4 Ch. SPST	DG445	CMOS + 40	175	0.25	15	-15	5	30	175	145	44	V+ to V-	0	0.8	2.4	DG212 Upgrade	DJ	DY	AK						
4 Ch. SPST	DGP201A	CMOS + 40	175	0.25	22	-22		44	600	450	44	V+ to V-	0	0.8	2.4	High Precision	DJ	DY	AK		AZ				
4 Ch. SPST	DG442	CMOS + 40	175	0.25	15	-15		30	175	145	44	V+ to V-	0	0.8	2.4	DG202 Upgrade	DJ	DY	AK						
4 Ch. SPST	DG444	CMOS + 40	175	0.25	15	-15	5	30	175	145	44	V+ to V-	0	0.8	2.4	DG211 Upgrade	DJ	DY	AK						

NOTES: 1. XXX Not recommended for new designs.

2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch, r<sub>DS(on)</sub> is also a function of supply and analog voltage. See individual data sheets for more details.

3. Logic supply voltage required for TTL compatible inputs.

4. Preliminary product. Specifications subject to change. Contact the factory for availability.

5. Input reference voltage of 2.5V is required. See individual data sheets for more details.

6. See data sheets for switch states of differential and multiple switches.

# ANALOG SWITCHES

Functional Configuration	Basic Part Number	Switch Type	r <sub>DS(on)</sub> MAX (Ω) (2)	I <sub>S(off)</sub> MAX nA	Supply Voltage			Volt. Range (2)	Switching Time (ns MAX)			MAX Supp. Range	Analog Voltage Range (V)	Input for ON Switch	Levels		Comments	Package and Temperature Range Offerings:					
					V <sub>+</sub>	V <sub>-</sub>	V <sub>L</sub> (3)		t <sub>on</sub>	t <sub>off</sub>	V <sub>inL</sub>				V <sub>inH</sub>	Plastic DIP		Plastic SO	CerDIP	Side Braze	LCC	Flat Pack	Metal Can
4 Ch. SPST	DG271	CMOS + 40	50	1.00	15	-15		30	75	75	44	V+ to V-	0	0.8	2.0	High Speed, Low Charge Inj.	CJ	DY	AK,BK,CK		AZ		
4 Ch. SPST	DG309	CMOS + 40	100	1.00	15	-15		30	200	150	44	V+ to V-	0	3.5	11.0	Single Supply	CJ	DY	AK,BK,CK				
4 Ch. SPST	DG308A	CMOS + 40	100	1.00	15	-15		30	200	150	44	V+ to V-	1	3.5	11.0	Single Supply	CJ	DY	AK,BK,CK				
4 Ch. SPST	DG221	CMOS + 40	100	1.00	15	-15		30	550	340	44	V+ to V-	0	0.8	2.4	Latchable Inputs	CJ	DY	AK,BK,CK				
4 Ch. SPST	DG172	PMOS	150	1.00	10	-20	5	20	300	750	36	(V+) to (V-)+10	0	0.8	2.0	Chip Select Function	CJ			AP,BP		AL	
4 Ch. SPST	DG201A	CMOS + 40	175	1.00	15	-15		30	600	450	44	V+ to V-	0	0.8	2.4	JAN Qualified	CJ	DY	AK,BK,CK		AZ	AL	
4 Ch. SPST	DG202	CMOS + 40	175	1.00	15	-15		30	600	450	44	V+ to V-	1	0.8	2.4	JAN Qualified	CJ						
4 Ch. SPST	DG540	D/CMOS	60	10.00	12	-3		10	90	50	18	(V+) -5 to V-	0	0.8	2.4	Wideband Video	DJ	DN		AP			
4 Ch. SPST	DG541	D/CMOS	60	10.00	12	-3		10	90	50	18	(V+) -5 to V-	0	0.8	2.4	Wideband Video	DJ	DY		AP			
4 Ch. SPST	DG212	CMOS + 40	175	5.00	15	-15	5	30	1000	500	44	V+ to V-	1	0.8	2.4	Low Cost	CJ	DY					
4 Ch. SPST	DG211	CMOS + 40	175	5.00	15	-15	5	30	1000	500	44	V+ to V-	0	0.8	2.4	Low Cost	CJ	DY					
5 Ch. SPST	DG125	PMOS	100	1.00	10	-20	5	20	300	2000	36	(V+) to (V-)+10	0	0.5	4.6	Low Standby Power				AP,BP		AL	
8 Ch. SPST	DG566	D/CMOS	100	5.00	60	-60	15	100	2000	1500	124	(V+)-10 to (V-)	0	4.0	11.0	High V, Serial Load	CJ			AP,DP			
1 Ch. SPDT	DG419	CMOS + 40	25	0.25	15	-15	5	30	125	75	44	V+ to V-	Note 6	0.8	2.4	Mini DIP, Low Power	DJ						
1 Ch. SPDT	DG402	CMOS + 40	25	0.25	15	-15	5	30	125	75	44	V+ to V-	Note 6	0.8	2.4	Low Power, High Perf.	DJ		AK				
1 Ch. SPDT	DG5050	CMOS + 40	25	0.50	15	-15	5	30	125	75	44	V+ to V-	Note 6	0.8	2.4	Low Charge Injection	DJ		AK				
1 Ch. SPDT	DG5142	CMOS + 40	30	0.50	15	-15	5	30	200	125	44	V+ to V-	Note 6	0.8	2.4	Use DG402 for New Designs	CJ		AK,CK				
1 Ch. SPDT	DG187	N-JFET	30	1.00	10	-20	5	20	150	130	36	(V+) to (V-)+7.5	Note 6	0.8	2.0	Use DG402 for New Designs				AP,BP		AL	AA,BA
1 Ch. SPDT	DG187	N-JFET	30	1.00	15	-15	5	15	150	130			Note 6	0.8	2.0	Use DG402 for New Designs				AP,BP		AL	AA,BA
1 Ch. SPDT	DG144	N-JFET	30	1.00	12	-18		20	800	1600	36	(V+)-2 to (V-)+8	Note 5	2.0	3.0	Use DG402 for New Designs				AP,BP		AL	
1 Ch. SPDT	DG301A	CMOS + 40	50	1.00	15	-15		30	300	250	44	V+ to V-	Note 6	0.8	4.0	JAN Qualified	CJ		AK,BK,CK			AL	AA,BA,CA
1 Ch. SPDT	DG387A	CMOS + 40	50	1.00	15	-15		30	300	250	44	V+ to V-	Note 6	0.8	4.0	Use DG402 for New Designs	CJ		AK,BK,CK			AL	AA,BA,CA
1 Ch. SPDT	DG305A	CMOS + 40	50	1.00	15	-15		30	250	150	44	V+ to V-	Note 6	3.5	11.0	JAN Qualified	CJ		AK,BK,CK			AL	AA,BA,CA
1 Ch. SPDT	DG5042	CMOS + 40	50	1.00	15	-15	5	30	1000	500	44	V+ to V-	Note 6	0.8	2.4	Break-Before-Make	CJ		AK,CK				
1 Ch. SPDT	DG188	N-JFET	75	1.00	15	-15	5	20	250	130			Note 6	0.8	2.0	Use DG402 for New Designs				AP,BP		AL	AA,BA
1 Ch. SPDT	DG188	N-JFET	75	1.00	10	-20	5	20	250	130	36	(V+) to (V-)+5	Note 6	0.8	2.0	Use DG402 for New Designs				AP,BP		AL	AA,BA
1 Ch. SPDT	DG143	N-JFET	80	1.00	12	-18		20	800	1600	36	(V+)-2 to (V-)+5	Note 5	2.0	3.0	Use DG402 for New Designs				AP,BP		AL	AA,BA
1 Ch. SPDT	DG186	N-JFET	10	10.00	15	-15	5	15	300	250			Note 6	0.8	2.0	Use DG402 for New Designs				AP,BP		AL	AA,BA
1 Ch. SPDT	SI3002	PMOS	100	1.00	10	-20		20	1000	1500	36	(V+) to (V-)+10	Note 6	0.8	2.0	Use DG402 for New Designs				AP,BP		AL	AA,BA
1 Ch. SPDT	DG186	N-JFET	10	10.00	10	-20	5	20	300	250	36	(V+) to (V-)+7.	Note 6	0.8	2.0	Use DG402 for New Designs				AP,BP		AL	AA,BA
1 Ch. SPDT	DG146	N-JFET	10	10.00	12	-18		20	1000	2500	36	(V+)-2 to (V-)+8	Note 5	2.0	3.0	Use DG402 for New Designs				AP,BP		AL	

- NOTES:
1. ~~XXX~~ Not recommended for new designs.
  2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch, r<sub>DS(on)</sub> is also a function of supply and analog voltage. See individual data sheets for more details.
  3. Logic supply voltage required for TTL compatible inputs.
  4. Preliminary product. Specifications subject to change. Contact the factory for availability.
  5. Input reference voltage of 2.5V is required. See individual data sheets for more details.
  6. See data sheets for switch states of differential and multiple switches.



# ANALOG SWITCHES

Functional Configuration	Basic Part Number	Switch Type	$r_{DS(on)}$ MAX ( $\Omega$ ) (2)	$I_{S(off)}$ MAX2 nA	Supply Voltage			Volt. Range (2)	Switching Time (ns Max)		MAX Supp. Range	Analog Voltage Range (V)	Logic Input for ON Switch	Logic Levels		Comments	Package and Temperature Range Offerings:							
					V+	V-	$V_L$ (3)		$t_{on}$	$t_{off}$				$V_{inL}$	$V_{inH}$		Plastic DIP	Plastic SO	CerDIP	Side Braze	LCC	Flat Pack	Metal Can	
					2 Ch. SPDT	DG423	CMOS + 40		25	0.25				15	-15		5	30	125	75	44	V+ to V-	Note 6	0.8
2 Ch. SPDT	DG403	CMOS + 40	25	0.25	15	-15	5	30	125	75	44	V+ to V-	Note 6	0.8	2.4	Low Power, High Perf.	DJ	DY	AK			AZ		
2 Ch. SPDT	DG5051	CMOS + 40	25	0.50	15	-15	5	30	125	75	44	V+ to V-	Note 6	0.8	2.4	Low Charge Injection	DJ	DY	AK					
2 Ch. SPDT	DGP303A	CMOS + 40	50	0.50	22	-22		30	300	250	44	V+ to V-	Note 6	0.8	4.0	High Precision	DJ	DY	AK			AZ		
2 Ch. SPDT	DG5143	CMOS + 40	30	0.50	15	-15	5	30	200	125	44	V+ to V-	Note 6	0.8	2.4	Use DG403 for New Designs	CJ		AK, CK					
2 Ch. SPDT	DG542	D/CMOS	60	10.00	12	-3		10	90	50	18	(V+) -5 to V-	Note 6	0.8	2.4	Wideband Video	DJ	DN		AP				
2 Ch. SPDT	DG190	N-JFET	30	1.00	15	-15	5	15	150	130			Note 6	0.8	2.0	Use DG403 for New Designs				AP, BP		AL		
2 Ch. SPDT	DG190	N-JFET	30	1.00	10	-20	5	20	150	130	36	(V+) to (V-)+7.5	Note 6	0.8	2.0	Use DG403 for New Designs				AP, BP		AL		
2 Ch. SPDT	DG307A	CMOS + 40	50	1.00	15	-15		30	250	150	44	V+ to V-	Note 6	3.5	11.0	JAN Qualified	CJ		AK, BK, CK				AL	
2 Ch. SPDT	DG303A	CMOS + 40	50	1.00	15	-15		30	300	250	44	V+ to V-	Note 6	0.8	4.0	JAN Qualified	CJ	DY	AK, BK, CK			AZ		
2 Ch. SPDT	DG5043	CMOS + 40	50	1.00	15	-15	5	30	1000	500	44	V+ to V-	Note 6	0.8	2.4	Use DG403 for New Designs	CJ		AK, CK					
2 Ch. SPDT	DG390A	CMOS + 40	50	1.00	15	-15		30	300	250	44	V+ to V-	Note 6	0.8	4.0	Use DG403 for New Designs	CJ		AK, BK, CK					
2 Ch. SPDT	DG243	CMOS + 40	50	1.00	15	-15	5	30	1000	500	44	V+ to V-	Note 6	0.8	2.0	Use DG403 for New Designs	CJ		AK, CK					
2 Ch. SPDT	DG191	N-JFET	75	1.00	10	-20	5	20	250	130	36	(V+) to (V-)+5	Note 6	0.8	2.0	Use DG403 for New Designs				AP, BP		AL		
2 Ch. SPDT	DG191	N-JFET	75	1.00	15	-15	5	20	250	130			Note 6	0.8	2.0	Use DG403 for New Designs				AP, BP		AL		
2 Ch. SPDT	DG189	N-JFET	10	10.00	10	-20	5	20	300	250	36	(V+) to (V-)+7.5	Note 6	0.8	2.0	Use DG403 for New Designs				AP, BP		AL		
2 Ch. SPDT	DG189	N-JFET	10	10.00	15	-15	5	15	300	250			Note 6	0.8	2.0	Use DG403 for New Designs				AP, BP		AL		
1 Ch. DPST	DG404	CMOS + 40	25	0.25	15	-15	5	30	125	75	44	V+ to V-	Note 6	0.8	2.4	Low Power, High Perf.	DJ		AK					
1 Ch. DPST	DG5144	CMOS + 40	30	0.50	15	-15	5	30	200	125	44	V+ to V-	Note 6	0.8	2.4	Use DG404 for New Designs	CJ		AK, CK					
1 Ch. DPST	DG5044	CMOS + 40	50	1.00	15	-15	5	30	1000	500	44	V+ to V-	Note 6	0.8	2.4	Use DG404 for New Designs	CJ		AK, CK					
2 Ch. DPST	DG425	CMOS + 40	25	0.25	15	-15	5	30	125	75	44	V+ to V-	Note 6	0.8	2.4	On Board Latches	DJ	DY	AK					
2 Ch. DPST	DG405	CMOS + 40	25	0.25	15	-15		30	125	75	44	V+ to V-	1	0.8	2.4	Low Power, High Perf.	DJ	DY	AK			AZ		
2 Ch. DPST	DG5049	CMOS + 40	25	0.50	15	-15		30	125	75	44	V+ to V-	1	0.8	2.4	Use DG405 for New Designs	DJ	DY	AK					
2 Ch. DPST	DG5145	CMOS + 40	30	0.50	15	-15		30	200	125	44	V+ to V-	1	0.8	2.4	Use DG405 for New Designs	CJ		AK, CK					
2 Ch. DPST	DG184	N-JFET	30	1.00	10	-20	5	20	150	130	36	(V+) to (V-)+7.5	1	0.8	2.0	Use DG405 for New Designs				AP, BP		AL		
2 Ch. DPST	DG184	N-JFET	30	1.00	15	-15	5	15	150	130			1	0.8	2.0	Use DG405 for New Designs				AP, BP		AL		

NOTES: 1. ~~XXX~~ Not recommended for new designs.

2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch,  $r_{DS(on)}$  is also a function of supply and analog voltage. See individual data sheets for more details.

3. Logic supply voltage required for TTL compatible inputs.

4. Preliminary product. Specifications subject to change. Contact the factory for availability.

5. Input reference voltage of 2.5V is required. See individual data sheets for more details.

6. See data sheets for switch states of differential and multiple switches.



# ANALOG SWITCHES

Functional Configuration	Basic Part Number	Switch Type	r <sub>DS(on)</sub> MAX (Ω) (2)	I <sub>S(off)</sub> MAX2 nA	Supply Voltage			Volt. Range (2)	Switching Time (ns Max)		MAX Supp. Range	Analog Voltage Range (V)	Logic Input for ON Switch	Logic Levels		Comments	Package and Temperature Range Offerings:								
					V+	V-	V <sub>L</sub> (3)		t <sub>on</sub>	t <sub>off</sub>				V <sub>inL</sub>	V <sub>inH</sub>		Plastic DIP	Plastic SO	CerDIP	Side Braze	LCC	Flat Pack	Metal Can		
2 Ch. DPST	DG129	N-JFET	30	1.00	12	-18		20	600	1600	36	(V+)-2 to (V-)+8	1	0.8	2.5	Use DG405 for New Designs					AP,BP		AL		
2 Ch. DPST	DG302A	CMOS + 40	50	1.00	15	-15		30	300	250	44	V+ to V-	1	0.8	4.0	JAN Qualified	CJ								
2 Ch. DPST	DG306A	CMOS + 40	50	1.00	15	-15		30	250	150	44	V+ to V-	1	3.5	11.0	JAN Qualified	CJ								
2 Ch. DPST	DG384A	CMOS + 40	50	1.00	15	-15		30	300	250	44	V+ to V-	1	0.8	4.0	Use DG405 for New Designs	CJ								
2 Ch. DPST	DG5045	CMOS + 40	50	1.00	15	-15		30	1000	500	44	V+ to V-	1	0.8	2.4	Use DG405 for New Designs	CJ								
2 Ch. DPST	DG185	N-JFET	75	1.00	15	-15	5	20	250	130			1	0.8	2.0	Use DG405 for New Designs							AL		
2 Ch. DPST	DG185	N-JFET	75	1.00	10	-20	5	20	250	130	36	(V+) to (V-)+5	1	0.8	2.0	Use DG405 for New Designs							AL		
2 Ch. DPST	DG126	N-JFET	80	1.00	12	-18		20	600	1600	36	(V+)-2 to (V-)+5	1	0.8	2.5	Use DG405 for New Designs							AL		
2 Ch. DPST	DG183	N-JFET	10	10.00	15	-15	5	15	300	250			1	0.8	2.0	Use DG405 for New Designs							AL	AA, BA	
2 Ch. DPST	DG140	N-JFET	10	10.00	12	-18		20	1000	2500	36	(V+)-2 to (V-)+8	1	0.8	2.5	Use DG405 for New Designs							AL		
2 Ch. DPST	DG183	N-JFET	10	10.00	10	-20	5	20	300	250	36	(V+) to (V-)+8	1	0.8	2.0	Use DG405 for New Designs							AL	AA, BA	
1 Ch. DPDT	DG139	N-JFET	30	1.00	12	-18		20	800	1600	36	(V+)-2 to (V-)+8	Note 5	2.0	3.0	Use DG403 for New Designs							AL		
1 Ch. DPDT	DG142	N-JFET	80	1.00	12	-18		20	800	1600	36	(V+)-2 to (V-)+5	Note 5	2.0	3.0	Use DG403 for New Designs							AL		
1 Ch. DPDT	DG145	N-JFET	10	10.00	12	-18		20	1000	2500	36	(V+)-2 to (V-)+8	Note 5	2.0	3.0	Use DG403 for New Designs							AL		

NOTES: 1. ~~XXX~~ Not recommended for new designs.

- For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch, r<sub>DS(on)</sub> is also a function of supply and analog voltage. See individual data sheets for more details.
- Logic supply voltage required for TTL compatible inputs.
- Preliminary product. Specifications subject to change. Contact the factory for availability.
- Input reference voltage of 2.5V is required. See individual data sheets for more details.
- See data sheets for switch states of differential and multiple switches.

# DRIVERS

Basic Part Number	# of Inputs	# of Outputs	Function	Input Logic for V <sub>OUTL</sub>	V <sub>inL</sub> (V)	V <sub>inH</sub> (V)	MAX Output Drive Current (mA)	MAX Output Swing (V)	Break-down (V)	t <sub>on</sub> (ns)	t <sub>off</sub> (ns)	Optimum Supply Voltage				Comments	Package and Temperature Ranges:				
												V <sub>+</sub>	V <sub>-</sub>	V <sub>L</sub>	V <sub>R</sub>		Plastic DIP	CerDIP	Side Braze	Flat Pack	Metal Can
D125	6	6	Six Separate Drivers	0	0.5	4.6	-5	-30	36	500	1500	10	-20	5		JFET Drivers			AP AP/883	AL AL/883	
D129	7	4	Four Channel Driver with Decode	1	0.7	2.2	-10	50	50	300	1500	10	-20	5	0	JFET Drivers					
D139	2	4	Dual Driver with Decode	Note 3	0	5	10	30	36	170	200	10	-20	5	0	Level Shifter, JFET Driver	CJ		AP AP/883		AA AA-2
D169	2	4	Dual Driver with Complementary Outputs	Note 3	0.8	2	+/- 40	33	36	170	200	15	-15	5	0	Smaller MOSPOWER Driver, 2-1/2 Bridge Level Shifter, Line Driver	CJ	AK AK/883	AP AP/883		
D469	8	4	Quad Driver with Complementary Inputs	Note 3	0.8	3	+/- 500	12.6	14	100	100	12	0	n/a	n/a	MOSPOWER Driver, 4 Separate Drivers, Low-V H-Bridge Driver	CJ		AP AP/883 BP		
D470	8	8	Octal Driver with Serial Input	Note 3	0.8	2.4	+/- 100	+/- 15	44	100	100	15	-15	n/a	n/a	FET Driver, 8 Separate Drivers, Serial Data Input	DJ		AP		

# FET SWITCHES

Basic Part Number	Sources	Drains	Gates	Switch Type	Pull-up On Gate	r <sub>DS(on)</sub> MAX		BV <sub>DSS</sub>	I <sub>s(off)</sub> (nA)	V <sub>GS(th)</sub>		Capacitances (pF)			Packages and Temp.	
						VS = 10V	VS = -10 V			MIN	MAX	C <sub>gs</sub> (C <sub>g</sub> ) MAX	C <sub>ds</sub> (C <sub>d</sub> ) MAX	C <sub>sb</sub> (C <sub>s</sub> ) MAX	Side Braze	Flat Pack
G118	6	1	8	SP6T	No	100	450	-30	0.5	-1.5	-4.0	0.9(typ)	0.4(typ)	2(typ)	AP, AP-2	AL, AL-2
G119	6	2	3	DP3T	Yes	100	450	-30	0.5	-1.5	-4.0	1.8(typ)	0.4(typ)	2(typ)	AP, AP-2	AL, AL-2
SD5000	4	4	4	4 X SPST	No	50	20	10	10.0	0.1	2.0	(3.5)	(1.6)	(5)		
SD5001	4	4	4	4 X SPST	No	50	20	10	10.0	0.1	2.0	(3.5)	(1.6)	(5)		
SD5002	4	4	4	4 X SPST	No	50	15	10	10.0	0.1	2.0	(3.5)	(1.6)	(5)		
SD5400	4	4	4	4 X SPST	No	50	20	10	10.0	0.1	2.0	(3.5)	(1.6)	(5)		
SD5401	4	4	4	4 X SPST	No	50	10	10	10.0	0.1	2.0	(3.5)	(1.6)	(5)		
SD5402	4	4	4	4 X SPST	No	50	15	10	10.0	0.1	2.0	(3.5)	(1.6)	(5)		

# ANALOG MULTIPLEXERS

Function	Basic Part Number	Input Latches	MAX $r_{DS(on)}$ ( $\Omega$ ) (2)	$I_D(off)$ (nA)	Analog Range (V) (2)	Trans. Time ( $\mu$ S)	Logic Levels (V)		Supply Voltages (V)			Comments	Package and Temp. Range Offerings:								
							$V_{inL}$	$V_{inH}$	$V_+$	$V_-$	$V_L$		Plastic DIP	CarDIP	Side Braze	Hermetic Quad/LCC	Quad PLCC	Flat Pack	SO		
Eight Ch. Serial Input Switch Array	DG480	YES	75	1	+/-15	0.2	0.8	2.4	15	-15		Any of Eight	DJ	AK							
Eight Ch. Serial Input Switch Array	DG485	YES	75	1	+/-15	0.2	0.8	2.4	15	-15	5	Low Power DG480	DJ	AK							
Eight Channel MUX + Enable	DG408	NO	100	1	+/-15	0.2	0.8	2.4	15	-15		High Performance	DJ	AK						DY	
Eight Ch. Single/Four Ch. Diff. MUX	DG538	YES	90	10	-5 to +10	0.3	0.8	2.4	15	-5		Wideband/Video	DJ		AP			DN			
Eight Channel MUX + Enable	DG908	NO	1000	1	+/-15	1.0	0.8	2.4	15	-15		Fault Protected	DJ	AK						DY	
Eight Channel MUX + Enable	DG501	NO	150	8	+/-5	1.5	0.6	3.5	5	-20			CJ		AP, BP						
Eight Channel MUX + Enable	S13705	NO	150	8	+/-5	1.5	0.6	3.5	5	-20				142K, 143K	AP, BP						
Eight Channel MUX + Enable	DG503	NO	150	8	+/-10	1.5	0.6	3.5	10	-20			CJ		AP, BP						
Eight Channel MUX + Enable	DGP508A	NO	400	2	+/-15	1.0	0.8	2.4	15	-15		Precision	DJ	AK, BK, CK					AL	CY, DY	
Eight Channel MUX + Enable	DG508A	NO	400	10	+/-15	1.0	0.8	2.4	15	-15			CJ	AK, BK, CK					AL	CY, DY	
Eight Channel MUX + Enable	DG528	YES	400	10	+/-15	1.0	0.8	2.4	15	-15		Latches On Board	CJ	AK, BK, CK							
Eight Channel MUX + Enable	DG568	YES	100	120	+/-50	2.0	4.0	11.0	60	-60	15	High Voltage	CJ	BP							
Eight Channel MUX + Enable	DG548A	NO	1500	10	+/-15	1.0	0.8	2.4	15	-15		Over Vol. Prot.	CJ	AK, BK			AZ				DY
Sixteen Channel MUX + Enable	DG536	YES	90	10	0 to 10	0.3	4.5	10.5	15	0		Wideband/Video	DJ		AP			AM	DN		
Sixteen Channel MUX + Enable	DG535	YES	90	10	0 to 10	0.3	4.5	10.5	15	0		Wideband/Video	DJ		AP						
Sixteen Channel MUX + Enable	DG506A	NO	400	10	+/-15	1.0	0.8	2.4	15	-15			CJ	AK, BK, CK	AR, BR, CR		AZ				
Sixteen Channel MUX + Enable	DG526	YES	400	10	+/-15	1.0	0.8	2.4	15	-15		Latches On Board	CJ	AK, BK, CK							
Four Channel Dual MUX	DG409	NO	100	1	+/-15	0.2	0.8	2.4	15	-15		High Performance	DJ	AK							DY
Eight Ch. Single/Four Ch. Diff. MUX	DG538	YES	90	10	-5 to +10	0.3	0.8	2.4	15	-5		Wideband/Video	DJ		AP						
Four Ch. Single/Two Ch. Diff. MUX	DG534	YES	90	10	-5 to +10	0.3	0.8	2.4	15	-5		Wideband/Video	DJ		AP				DN		
Four Channel Dual MUX	DGP509A	NO	400	10	+/-15	1.0	0.8	2.4	15	-15			CJ	AK, BK, CK							DY
Four Channel Dual MUX	DG529	YES	400	10	+/-15	1.0	0.8	2.4	15	-15		Latches On Board	CJ	AK, BK, CK							
Four Channel Dual MUX	DG509A	NO	400	10	+/-15	1.0	0.8	2.4	15	-15		Precision	CJ	AK, BK, CK							DY
Four Channel Dual MUX	DG569	YES	100	120	+/-50	2.0	4.0	11.0	60	-60	15	High Voltage	CJ	BP							
Eight Channel Dual MUX + Enable	DG507A	NO	400	5	+/-15	1.0	0.8	2.4	15	-15			CJ	AK, BK, CK	AR, BR, CR		AZ				
Eight Channel Dual MUX + Enable	DG527	YES	400	5	+/-15	1.0	0.8	2.4	15	-15		Latches On Board	CJ	AK, BK, CK							

Notes: 1. ~~XXX~~ Not recommended for new designs.

2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch,  $r_{DS(on)}$  is also a function of supply and analog voltage. See individual data sheets for more details.



# HIGH VOLTAGE MULTIPLEXERS

Function	Basic Part Number	Input Latches	MAX $t_{DS(on)}$ ( $\mu$ S)	$I_D(OFF)$ (nA)	Analog Voltage Range (V)	Transition Time ( $\mu$ S)	Logic Levels (V)		Supply Voltages (V)			Pkg. and Temp.	
							$V_{inL}$	$V_{inH}$	$V_+$	$V_-$	$V_L$	Plastic DIP	Side Braze DIP
Eight Channel MUX + Enable	DG568	YES	100	120	( $V_+$ ) - 10 to ( $V_-$ )	2.0	4.0	11.0	60	-60	15	CJ	AP, BP
Four Channel Dual MUX	DG569	YES	100	120	( $V_+$ ) - 10 to ( $V_-$ )	2.0	4.0	11.0	60	-60	15	CJ	AP, BP

# DATA CONVERSION PRODUCTS: A/Ds AND D/A

Function	Basic Part Number	Resolution (Bits)	$\text{INL}$	Gain Error	Settling/Conversion Time ( $\mu$ S)	Logic Levels ( $V_{Supply} = 15$ V)		Logic Levels ( $V_{Supply} = 5$ V)		MAX Supply Volt		Comments	Package and Temp. Range Offerings:				
						$V_{inL}$	$V_{inH}$	$V_{inL}$	$V_{inH}$	$V_+$	$V_-$		Plastic DIP	CerDIP	Side Braze	Hermetic Quad/LCC	Quad FLCC
8 Ch. Data Acq. Sys.	SI8601	8	0.5	0.25	25.0	n/a	n/a	1.5	3.5	6.5	0	$\mu$ P Interface, S/H on-board	DJ		AK, AK/883		
8 Ch. Data Acq. Sys.	SI8602	8	0.5	0.25	25.0	1.5	13.5	n/a	n/a	15	0	$\mu$ P Interface, S/H on-board	DJ		AK, AK/883		
A/D Converter	SI8603	8	0.25	0.25	25.0	n/a	n/a	1.5	3.5	6.5	0	$\mu$ P Interface, S/H on-board	DJ		AK, AK/883		DN
A/D Converter	SI8604	8	0.25	0.25	25.0	1.5	13.5	n/a	n/a	15	0	$\mu$ P Interface, S/H on-board	DJ		AK, AK/883		DN
Successive Approx. Reg.	SI2504	12	n/a	n/a	n/a	n/a	n/a	0.8	2.4	7.5	0	40 MHz Operation, Low Power	CJ		AK		
4 1/2 Digit A/D Converter	SI7135	15	1	1	500000	n/a	n/a	0.8	2.8	6	-9	DVM/DMM Applications	CJ	CK			DN
4 1/2 Digit A/D Converter	LD120/121A	15	1	1	200000	0.5	4	n/a	n/a	15	-15	DVM/DMM Applications	CJ				
4 1/2 Digit A/D Converter	LD122/121A	15	1	1	200000	0.5	4	n/a	n/a	15	-15	DVM/DMM Applications	CJ				
3 1/2 Digit A/D Converter	LD110/111A	11	1	1	25000	0.5	4	n/a	n/a	15	-15	DVM/DMM Applications	CJ				
CMOS Mult. DAC	SI7533	10	0.5	14	0.6	0.8	2.4	n/a	n/a	15	0	Replaces AD7520 and AD7533	JN,KN,LN	AQ,BQ,CQ	SD,TD,UD	TE	JP,KP
CMOS Mult. DAC	SI7541	12	0.5	12.5	0.6	0.8	2.4	n/a	n/a	15	0	Reduced Output Capacitance	JN,KN		SD,TD	TE	
CMOS Mult. DAC	SI7541A	12	0.5	1	0.6	0.8	2.4	n/a	n/a	15	0	Reduced Output Capacitance	JN,KN		SD,TD	TE	JP,KP
CMOS Voltage Out DAC	SI7240	12	0.5	1	0.6	0.8	2.4	n/a	n/a	15	0	Reduced Output Capacitance	JN,KN		SD,TD	TE	
CMOS Mult. DAC w/Latches	SI7545	12	0.5	1	2	1.5	13.5	0.8	2.4	15	0	$\mu$ P Compatible	JN,KN,LN		SD,TD,GUD	GUE	JP,LP
CMOS Mult. DAC w/Latches	SI7542	12	0.5	1	2	0.8	2.4	0.8	2.4	15	0	4 Bit Bus Input	JN,KN,GKN		SD,TD,GTD	GUE	
CMOS Mult. DAC Serial In	SI7543	12	0.5	1	2	0.8	2.4	0.8	2.4	15	0	Serial In	JN,KN,GKN		SD,TD,GTD	GUE	

Notes: 1. **XXX** Not recommended for new designs

2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch,  $t_{DS(on)}$  is also a function of supply and analog voltage. See individual data sheets for more details.

# LINEARS

Functional Configuration	Basic Part Number	Technology	Open Loop Gain (dB)	MIN Supply Voltage (V)	MAX Supply Voltage (V)	Input Offset Voltage (mV) MAX	TC Input Offset ( $\mu\text{V}/^{\circ}\text{C}$ )	Comments	Pkg. and Temp. Ranges:*			
									Plastic DIP	Side Braze	CarDIP	Metal Can
Triple Op Amp	L144	Bipolar	80.0	+/-1.5	+/-18	5.0	3.3	Programmable Supply Current	CJ	AP, BP, /883		
Quad Comparator	L161	Bipolar	80.0	+/-1.5	+/-18	3.0	n/a	Programmable Supply Current	CJ	AP, BP, /883		
Chopper Stabilized Op Amp	SI7652	CMOS	120.0	+/-3	+/-9	0.005	0.05	Ultra Precision	DJ, DH		DK	DA

# HIGH-VOLTAGE DISPLAY DRIVERS

Part Number	Description	Maximum Clock Rate $T_A = 25^{\circ}\text{C}$	Output Voltage @ Rated Current	Supply Voltages	Supply Currents (Worst Case Over Temp.)	Pkg. & Temp Ranges:*	
						44-Pin PLCC	44-Pin CLCC
SI9551/ SI9552	32-Channel Open Drain Output AC EL Row Drivers w/Serial Data Input	4 MHz	$V_{OLQ} = 30\text{ V (MAX)} @ 80\text{ mA}$ $I_{OFF} = 10\ \mu\text{A} @ V_{DD} = 200\text{ V}$	$V_L = 10.8\text{ to }15\text{ V}$	$I_L = 0.5\text{ mA}$	CN	AM
SI9553/ SI9554	32-Channel Push-pull Output AC EL Column Drivers w/Serial Data Input	10 MHz	$V_{OLQ} = 8\text{ V (MAX)} @ 15\text{ mA}$ $V_{OHQ} = 50\text{ V (MIN)} @ 15\text{ mA}$	$V_L = 10.8\text{ to }15\text{ V}$ $V_{DD} = 60\text{ V}$	$I_L = 0.5\text{ mA}$ $I_{DD} = 1\text{ mA}$	CN	AM
SI9555/ SI9556	32-Channel Push-pull Output AC EL Column Driver w/Serial Data Input	10 MHz	$V_{OLQ} = 8\text{ V (MAX)} @ 15\text{ mA}$ $V_{OHQ} = 70\text{ V (MIN)} @ 15\text{ mA}$	$V_L = 10.8\text{ to }15\text{ V}$ $V_{DD} = 80\text{ V}$	$I_L = 0.5\text{ mA}$ $I_{DD} = 5\text{ mA}$	CN	AM
SI9560	34-Channel Symmetric AC EL Row Driver	4 MHz	$V_{OLQ} = 30\text{ V (MAX)} @ 70\text{ mA}$ $V_{OHQ} = 195\text{ V (MIN)} @ 70\text{ mA}$	$V_L = 10.8\text{ to }15\text{ V}$ $V_{DD} = 225\text{ V}$	$I_L = 0.5\text{ mA}$ $I_{DD} = 8\text{ mA}$	CN	DM

Notes: 1. Assuming 1 mA of constant-current drive.

\* Available in Commercial, Industrial, and Military versions



## VOLTAGE CONVERTERS

Functional Configuration	Basic Part Number	Technology	MAX Input Current (mA)	MIN Supply Voltage (V)	MAX Supply Voltage (V)	MIN Output Voltage (V)	MAX Output Voltage (V)	Comments	Pkg. & Temp. Ranges:		
									Plastic DIP	Metal Can	SO
Voltage Doubler/Inverter	SI7660	CMOS	0.5	1.5	10	-10.0	20.0		CJ	AA, AA/883	CY
Voltage Doubler/Inverter	SI7661	CMOS	2.0	60.0	20	-20.0	40.0	Increased Voltage Range	CJ	AA, AA/883	CY

## SWITCHMODE REGULATORS/CONTROLLERS\*

Basic Part Number	MAX V <sub>IN</sub> (V)	MAX V <sub>OUT</sub> (V)	MAX I <sub>DS(ON)</sub> (A)	TYP R <sub>OUT</sub> (Ω)	TYP I <sub>SOURCE</sub> (mA)	TYP I <sub>SINK</sub> (mA)	V <sub>REF</sub> Accuracy	Pkg. & Temp. Ranges:		
								Plastic DIP	Cerdip	Surface-Mount
SI9100	70	150	5	-	-	-	± 1%	DJ	AK	DN
SI9101	70	150	5	-	-	-	± 10%	DJ	AK	DN
SI9102	120	200	7	-	-	-	± 1%	DJ	AK	DN
SI9110	120	-	-	20	150	200	± 1%	DJ	AK	DY
SI9111	120	-	-	20	150	200	± 10%	DJ	AK	DY
SI9115/ SI9116	300	-	-	-	150	200	± 1%	DJ	AK	DY

\* Regulators (SI9100/01/02) have onboard output MOSFETs. Controllers (SI9110/11/15/16) are designed to drive external MOSFETs.

**Cross Reference**

**4**





## Siliconix Direct Replacement

Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications.

## Siliconix Similar Replacement

Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed, as these parts may have different pin configurations. Before selecting a device as a substitute, compare the specifications. For devices not shown in this guide, or for additional information, the user should contact the nearest Siliconix sales office.

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
ADG200AA		DG200AAA	AD7521JP	SI7541AJP	
ADG200AA/883		DG200AAA/883	AD7521KN	SI7541AKN	
ADG200AP		DG200AAP	AD7521KP	SI7541AKP	
ADG200AP/883		DG200AAP/883	AD7521LN	SI7541AKN	
ADG200BA		DG200ABA	AD7521SD	SI7541ASD	
ADG200BP		DG200ABP	AD7521TD	SI7541ATD	
ADG200CJ		DG200ACJ	AD7521UD	SI7541ASD	
ADG201ABQ		DG411AK	AD7533AQ	SI7533AQ	
ADG201AKN		DG411DJ	AD7533BQ	SI7533BQ	
ADG201AP		DG411AK	AD7533CQ	SI7533CQ	
ADG201AP/883		DG411AK/883	AD7533JN	SI7533JN	
ADG201ATQ		DG411AK	AD7533KN	SI7533KN	
ADG201ATQ/883		DG411AK/883	AD7533LN	SI7533LN	
ADG201BP		DG411AK	AD7533LP	SI7533LP	
ADG201CJ		DG411DJ	AD7533SD	SI7533SD	
ADG202ABQ		DG412AK	AD7533TD	SI7533TD	
ADG202AKN		DG412DJ	AD7533UD	SI7533UD	
ADG202ATQ		DG412AK	AD7541AAQ	SI7541AAQ	
AD0145CD	DG145BP		AD7541ABQ	SI7541ABQ	
AD7240JN	SI7240JN		AD7541AJN	SI7541AJN	
AD7240KN	SI7240KN		AD7541AJP	SI7541AJP	
AD7240AQ	SI7240AQ		AD7541AKN	SI7541AKN	
AD7240BQ	SI7240BQ		AD7541AKP	SI7541AKP	
AD7240TD	SI7240TD		AD7541AQ	SI7541AQ	
AD7240SD	SI7240SD		AD7541ASD	SI7541ASD	
AD7501JD		DG501BK	AD7541ASD/883	SI7541ASD883	
AD7501JN		DG501CJ	AD7541ATD	SI7541ATD	
AD7501KD		DG501BK	AD7541ATD/883	SI7541ATD883	
AD7501KN		DG501CJ	AD7541BQ	SI7541BQ	
AD7501SD		DG501AK	AD7545AQ	SI7545AQ	
AD7503JD		DG503BK	AD7545BQ	SI7545BQ	
AD7503JN		DG503CJ	AD7545CQ	SI7545CQ	
AD7503KD		DG503BK	AD7545GCQ	SI7545GCQ	
AD7503KN		DG503CJ	AD7545GLN	SI7545GLN	
AD7503SD		DG503AK	AD7545GUD	SI7545GUD	
AD7506JD	DG506ABK		AD7545JN	SI7545JN	
AD7506JD/883	DG506AAR/883		AD7545JP	SI7545JP	
AD7506JN	DG506ACJ		AD7545KN	SI7545KN	
AD7506KD	DG506ABR		AD7545LN	SI7545LN	
AD7506KN	DG506ACJ		AD7545LP	SI7545LP	
AD7506SD	DG506AAK		AD7545SD	SI7545SD	
AD7506TD	DG506AAR		AD7545SD/883	SI7545SD/883	
AD7507JD	DG507ABK		AD7545TD	SI7545TD	
AD7507JD/883	DG507AAR/883		AD7545TD/883	SI7545TD/883	
AD7507JN	DG507ACJ		AD7545UD	SI7545UD	
AD7507KD	DG507ABR		AD7545UD/883	SI7545UD/883	
AD7507KN	DG507ACJ		AD7820LN	SI7820LN	
AD7507SD	DG507AAK		AD7820KN	SI7820KN	
AD7507TD	DG507AAR		AD7820LP	SI7820LP	
AD7508KD		DG508ABK	AD7820KP	SI7820KP	
AD7508KN		DG508ACJ	AD7820CQ	SI7820CQ	
AD7508SD		DG508AAK	AD7820BQ	SI7820BQ	
AD7509KD		DG509ABK	AD7820UQ	SI7820UQ	
AD7509KN		DG509ACJ	AD7820TQ	SI7820TQ	
AD7509SD		DG509AAK	AH0126CD	DG126BP	
AD7521JN	SI7541AJN				

# Cross Reference

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
AH0126D	DG126AP		CDG309AK		DG412AK
AH0126D/883	DG126AP/883		CDG309BJ		DG412DJ
AH0129CD	DG129BP		CDG309BK		DG412AK
AH0129D	DG129AP		CDG309CJ		DG412DJ
AH0129D/883	DG129AP/883		CDG309J		DG412AK
AH0133CD	DG133BP		CDG309N		DG412DJ
AH0133D	DG133AP		D123AK	D123AP	
AH0133D/883	DG133AP/883		D123AK/HR	D123AK/883	
AH0134CD	DG134BP		D123AP	D123AP	
AH0134D	DG134AP		D123AP-2	D123AP/883	
AH0134D/883	DG134AP/883		D123AP/883	D123AP/883	
AH0139CD	DG139BP		D123BK	D123BP	
AH0139D	DG139AP		D123BP	D123BP	
AH0139D/883	DG139AP/883		D125AK/HR	D125AP/883	
AH0140CD	DG140BP		D125AL	D125AL	
AH0140D	DG140AP		D125AL-2	D125AL/883	
AH0140D/883	DG140AP/883		D125AL/HR	D125AL/883	
AH0141CD	DG141BP		D125AL/883	D125AL/883	
AH0141D	DG141AP		D125AP	D125AP	
AH0141D/883	DG141AP/883		D125AP-2	D125AP/883	
AH0142CD	DG142BP		D125AP/883	D125AP/883	
AH0142D	DG142AP		D125BK	D125BP	
AH0143D	DG143AP		D125BP	D125BP	
AH0143D/883	DG143AP/883		D129AK	D129AP	
AH0144CD	DG144BP		D129AL	D129AL	
AH0144D	DG144AP		D129AL-2	D129AL/883	
AH0144D/883	DG144AP/883		D129AL/HR	D129AL/883	
AH0145D	DG145AP		D129AL/883	D129AL/883	
AH0145D/883	DG145AP/883		D129AP	D129AP	
AH0146CD	DG146AP		D129AP-2	D129AP/883	
AH0146D	DG146AP		D129AP/HR	D129AP/883	
AH0146D/883	DG146AP/883		D129AP/883	D129AP/883	
AH0151CD	DG141BP		D129BK	D129BP	
AH0151D	DG141AP		D129BP	D129BP	
AH0151D/883	DG141AP/883		D139AA	D139AA	
AH0152CD	DG133BP		D139AA-2	D139AA/883	
AH0152D	DG133AP		D139AA/883	D139AA/883	
AH0152D/883	DG133AP/883		D139AP	D139AP	
AH0153CD	DG140BP		D139AP-2	D139AP/883	
AH0153D	DG140AP		D139AP/883	D139AP/883	
AH0153D/883	DG140AP/883		D139BA	D139AA	
AH0154CD	DG129BP		D139BP	D139BP	
AH0154D	DG129AP		D139CJ	D139CJ	
AH0154D/883	DG129AP/883		D169AK	D169AK	
AH0161CD	DG146AP		D169AK-2	D169AK/883	
AH0161D	DG146AP		D169AK/883	D169AK/883	
AH0161D/883	DG146AP/883		D169AP	D169AP	
AH0162CD	DG144BP		D169AP-2	D169AP/883	
AH0162D	DG144AP		D169AP/883	D169AP/883	
AH0162D/883	DG144AP/883		D169CJ	D169CJ	
AH0163CD	DG145BP		D469AP	D469AP	
AH0163D	DG145AP		D469AP-2	D469AP/883	
AH0163D/883	DG145AP/883		D469AP/883	D469AP/883	
AH0164CD	DG139BP		D469BP	D469BP	
AH0164D	DG139AP		D469CJ	D469CJ	
AH0164D/883	DG139AP/883		D470AP	D470AP	
AM25L04XC	SI25HC04CJ		D470AP/883	D470AP/883	
AM2504C	SI25HC04CJ		D470DJ	D470DJ	
AM2504XC	SI25HC04CJ		DG123AL	DG123AL/883	
AM3705CD	DG501BP		DG123AL-2	DG123AL/883	
AM3705D	DG501AP		DG123AL/HR	DG123AL/883	
AN0120NA	SN0120NA		DG123AL/883	DG123AL/883	
AN0130NA	SN0130NA		DG123AP	DG123AP	
AN0140NA	SN0140NA		DG123AP-2	DG123AP/883	
CDG201AK		DG411AK	DG123AP/HR	DG123AP/883	
CDG201BJ		DG411DJ	DG123AP/883	DG123AP/883	
CDG201BK		DG411AK	DG123BP	DG123BP	
CDG211CJ		DG411DJ	DG125AL	DG125AL/883	
CDG308AK		DG411AK	DG125AL-2	DG125AL/883	
CDG308BJ		DG411DJ	DG125AL/HR	DG125AL/883	
CDG308BK		DG411AK	DG125AL/883	DG125AL/883	
CDG308CJ		DG411DJ	DG125AP	DG125AP	
CDG308J		DG411AK	DG125AP-2	DG125AP/883	
CDG308N		DG411DJ	DG125AP/HR	DG125AP/883	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
DG125AP/883	DG125AP/883		DG140AP	DG140AP	
DG125BP	DG125BP		DG140AP-2	DG140AP/883	
DG126AK		DG126AP	DG140AP/HR	DG140AP/883	
DG126AK/HR		DG126AP/883	DG140AP/883	DG140AP/883	
DG126AK/883		DG126AP/883	DG140BK		DG140BP
DG126AL	DG126AL/883		DG140BP	DG140BP	
DG126AL-2	DG126AL/883		DG141AK		DG141AP
DG126AL/HR	DG126AL/883		DG141AK/HR		DG141AP/883
DG126AL/883	DG126AL/883		DG141AK/883		DG141/883
DG126AP	DG126AP		DG141AL	DG141AL/883	
DG126AP-2	DG126AP/883		DG141AL-2	DG141AL/883	
DG126AP/HR	DG126AP/883		DG141AL/HR	DG141AL/883	
DG126AP/883	DG126AP/883		DG141AL/883	DG141AL/883	
DG126BK		DG126BP	DG141AP	DG141AP	
DG126BP	DG126BP		DG141AP-2	DG141AP/883	
DG129AK		DG129AP	DG141AP/HR	DG141AP/883	
DG129AK/HR		DG129AP/883	DG141AP/883	DG141AP/883	
DG129AK/883		DG129AP/883	DG141BK		DG141BP
DG129AL	DG129AL/883		DG141BP	DG141BP	
DG129AL-2	DG129AL/883		DG142AK		DG142AP
DG129AL/HR	DG129AL/883		DG142AK/HR		DG142AP/883
DG129AL/883	DG129AL/883		DG142AK/883		DG142AP/883
DG129AP	DG129AP		DG142AL	DG142AL/883	
DG129AP-2	DG129AP/883		DG142AL-2	DG142AL/883	
DG129AP/HR	DG129AP/883		DG142AL/HR	DG142AL/883	
DG129AP/883	DG129AP/883		DG142AL/883	DG142AL/883	
DG129BK		DG129BP	DG142AP	DG142AP	
DG129BP	DG129BP		DG142AP-2	DG142AP/883	
DG133AK		DG133AP	DG142AP/HR	DG142AL/883	
DG133AK/HR		DG133AP/883	DG142AP/883	DG142AP/883	
DG133AK/883		DG133AP/883	DG142BP	DG142BP	
DG133AL	DG133AL/883		DG143AK		DG143AP
DG133AL-2	DG133AL/883		DG143AK/HR		DG143AP/883
DG133AL/HR	DG133AL/883		DG143AK/883		DG143AP/883
DG133AL/883	DG133AL/883		DG143AL	DG143AL/883	
DG133AP	DG133AP		DG143AL-2	DG143AL/883	
DG133AP-2	DG133AP/883		DG143AL/HR	DG143AL/883	
DG133AP/883	DG133AP/883		DG143AL/883	DG143AL/883	
DG133BK		DG133BP	DG143AP	DG143AP	
DG133BP	DG133BP		DG143AP-2	DG143AP/883	
DG134AK		DG134AP	DG143AP/HR	DG143AP/883	
DG134AK-2		DG134AP/883	DG143AP/883	DG143AP/883	
DG134AK/HR		DG134AP/883	DG143BK		DG143AP
DG134AK/883		DG134AP/883	DG143BP	DG143AP	
DG134AL	DG134AL/883		DG144AK		DG144AP
DG134AL-2	DG134AL/883		DG144AK/HR		DG144AP/883
DG134AL/HR	DG134AL/883		DG144AK/883		DG144AP/883
DG134AL/883	DG134AL/883		DG144AL	DG144AL/883	
DG134AP	DG134AP		DG144AL-2	DG144AL/883	
DG134AP-2	DG134AP/883		DG144AL/HR	DG144AL/883	
DG134AP/883	DG134AP/883		DG144AL/883	DG144AL/883	
DG134BK		DG134BP	DG144AP	DG144AP	
DG134BP	DG134BP		DG144AP-2	DG144AP/883	
DG139AK		DG139AP	DG144AP/HR	DG144AP/883	
DG139AK/HR		DG139AP/883	DG144AP/883	DG144AP/883	
DG139AK/883		DG139/883	DG144BK		DG144AP
DG139AL	DG139AL/883		DG144BP	DG144AP	
DG139AL-2	DG139AL/883		DG145AK		DG145AP/883
DG139AL/HR	DG139AL/883		DG145AK-2		DG145AP/883
DG139AL/883	DG139AL/883		DG145AK/HR		DG145AP/883
DG139AP	DG139AP		DG145AL	DG145AL/883	
DG139AP-2	DG139AP/883		DG145AL-2	DG145AL/883	
DG139AP/HR	DG139AP/883		DG145AL/HR	DG145AL/883	
DG139AP/883	DG139AP/883		DG145AL/883	DG145AL/883	
DG139BK		DG139BP	DG145AP	DG145AP	
DG139BP	DG139BP		DG145AP-2	DG145AP/883	
DG140AK		DG140AP	DG145AP/HR	DG145AP/883	
DG140AK/HR		DG140AP/883	DG145AP/883	DG145AP/883	
DG140AK/883		DG140/883	DG145BK		DG145BP
DG140AL	DG140AL/883		DG145BP	DG145APDG146AK	
DG140AL-2	DG140AL/883		DG146AP		DG146AP/883
DG140AL/HR	DG140AL/883		DG146AK-2		DG146AP/883
DG140AL/883	DG140AL/883		DG146AK/HR		DG146AP/883

# Cross Reference

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
DG146AK/883		DG146AP/883	DG180AL	DG180AL/883	
DG146AL	DG146AL		DG180AL-2	DG180AL/883	
DG146AL-2	DG146AL/883		DG180AL/883	DG180AL/883	
DG146AL/HR	DG146AL/883		DG180AP	DG180AP	
DG146AL/883	DG146AL/883		DG180AP-2	DG180AP/883	
DG146AP	DG146AP		DG180AP/883	DG180AP/883	
DG146AP-2	DG146AP/883		DG180BA	DG180BA	
DG146AP/HR	DG146AP/883		DG180BP	DG180BP	
DG146AP/883	DG146AP/883		DG181AA	DG181AA	
DG146BK		DG146AP	DG181AA-2	DG181AA/883	
DG146BP	DG146AP		DG181AA/883	DG181AA/883	
DG151AL		DG141AL	DG181AL	DG181AL/883	
DG151AL-2		DG141AL/883	DG181AL-2	DG181AL/883	
DG151AL/883		DG141AL/883	DG181AL/883	DG181AL/883	
DG151AP		DG141AP	DG181AP	DG181AP	
DG151AP-2		DG141AP/883	DG181AP-2	DG181AP/883	
DG151AP/883		DG141AP/883	DG181AP/883	DG181AP/883	
DG151BP		DG141BP	DG181BA	DG181BA	
DG152AL		DG133AL	DG181BP	DG181BP	
DG152AL-2		DG133AL/883	DG182AA	DG182AA	
DG152AL/883		DG133AL/883	DG182AA-2	DG182AA/883	
DG152AP		DG133AP	DG182AA/883	DG182AA/883	
DG152AP-2		DG133AP/883	DG182AL	DG182AL/883	
DG152AP/883		DG133AP/883	DG182AL-2	DG182AL/883	
DG152BP		DG133BP	DG182AL/883	DG182AL/883	
DG153AL		DG140AL	DG182AP	DG182AP	
DG153AL-2		DG14AL/883	DG182AP-2	DG182AP/883	
DG153AL/883		DG140AL/883	DG182AP/883	DG182AP/883	
DG153AP		DG140AP	DG182BA	DG182BA	
DG153AP-2		DG140AP/883	DG182BP	DG182BP	
DG153AP/883		DG140AP/883	DG183AL	DG183AL/883	
DG153BP		DG140BP	DG183AL-2	DG183AL/883	
DG154AL		DG129AL	DG183AL/88S	DG183AL/883	
DG154AL-2		DG129AL/883	DG183AP	DG183AP	
DG154AL/883		DG129AL/883	DG183AP-2	DG183AP/883	
DG154AP		DG129AP	DG183AP/883	DG183AP/883	
DG154AP-2		DG129AP/883	DG183BP	DG183BP	
DG154AP/883		DG129AP/883	DG184AL	DG184AL/883	
DG154BP		DG129BP	DG184AL-2	DG184AL/883	
DG161AL		DG146AL	DG184AL/883	DG184AL/883	
DG161AL-2		DG146AL/883	DG184AP	DG184AP	
DG161AL/883		DG146AL/883	DG184AP-2	DG184AP/883	
DG161AP		DG146AP	DG184AP/883	DG184AP/883	
DG161AP-2		DG146AP/883	DG184BP	DG184BP	
DG161AP/883		DG146AP/883	DG185AL	DG185AL/883	
DG161BP		DG146AP	DG185AL-2	DG185AL/883	
DG162AL		DG144AL	DG185AL/883	DG185AL/883	
DG162AL-2		DG144AL/883	DG185AP	DG185AP	
DG162AL/883		DG144AL/883	DG185AP-2	DG185AP/883	
DG162AP		DG144AP	DG185AP/883	DG185AP/883	
DG162AP-2		DG144AP/883	DG185BP	DG185BP	
DG162AP/883		DG144AP/883	DG186AA	DG186AA	
DG162BP		DG144AP	DG186AA-2	DG186AA/883	
DG163AL		DG145AL	DG186AA/883	DG186AA/883	
DG163AL-2		DG145AL/883	DG186AL	DG186AL/883	
DG163AL/883		DG145AL/883	DG186AL-2	DG186AL/883	
DG163AP		DG145AP	DG186AL/883	DG186AL/883	
DG163AP-2		DG145AP/883	DG186AP	DG186AP	
DG163AP/883		DG145AP/883	DG186AP-2	DG186AP/883	
DG163BP		DG145BP	DG186AP/883	DG186AP/883	
DG164AL		DG139AL	DG186BA	DG186BA	
DG164AL-2		DG139AL/883	DG186BP	DG186BP	
DG164AL/883		DG139AL/883	DG187AA	DG187AA	
DG164AP		DG139AP	DG187AA-2	DG187AA/883	
DG164AP-2		DG139AP/883	DG187AA/883	DG187AA/883	
DG164AP/883		DG139AP/883	DG187AL	DG187AL/883	
DG164BP		DG139BP	DG187AL-2	DG187AL/883	
DG172AL	DG172AL/883		DG187AL/883	DG187AL/883	
DG172AL-2	DG172AL/883		DG187AP	DG187AP	
DG172AL/883	DG172AL/883		DG187AP-2	DG187AP/883	
DG180AA	DG180AA		DG187AP/883	DG187AP/883	
DG180AA-2	DG180AA/883		DG187BA	DG187BA	
DG180AA/883	DG180AA/883		DG187BK	DG187BK	

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
DG187BP	DG187BP		DG221AK	DG221AK	
DG188AA	DG188AA		DG221AK-2	DG221AK/883	
DG188AA-2	DG188AA/883		DG221AK/883	DG221AK/883	
DG188AA/883	DG188AA/883		DG221BK	DG221BK	
DG188AL	DG188AL/883		DG221CJ	DG221CJ	
DG188AL-2	DG188AL/883		DG221CK	DG221CK	
DG188AL/883	DG188AL/883		DG221CY	DG221CY	
DG188AP	DG188AP		DG221DY	DG221DY	
DG188AP-2	DG188AP/883		DG243AK	DG243AK	
DG188AP/883	DG188AP/883		DG243AK-2	DG243AK/883	
DG188BA	DG188BA		DG243AK/883	DG243AK/883	
DG188BP	DG188BP		DG243CJ	DG243CJ	
DG189AL	DG189AL/883		DG243CK	DG243CK	
DG189AL-2	DG189AL/883		DG243DJ	DG243DJ	
DG189AL/883	DG189AL/883		DG243DK	DG243DK	
DG189AP	DG189AP		DG271AK	DG271AK	
DG189AP-2	DG189AP/883		DG271AK-2	DG271AK/883	
DG189AP/883	DG189AP/883		DG271AK/883	DG271AK/883	
DG189BP	DG189BP		DG271AZ/883	DG271AZ/883	
DG190AL	DG190AL/883		DG271BK	DG271BK	
DG190AL-2	DG190AL/883		DG271CJ	DG271CJ	
DG190AL/883	DG190AL/883		DG271CK	DG271CK	
DG190AP	DG190AP		DG271CY	DG271DY	
DG190AP-2	DG190AP/883		DG271DY	DG271DY	
DG190AP/883	DG190AP/883		DG281AA		DG181AA
DG190BP	DG190BP		DG281AA-2		DG181AA/883
DG191AL	DG191AL/883		DG281AA/883		DG181AA/883
DG191AL-2	DG191AL/883		DG281AP		DG181AP
DG191AL/883	DG191AL/883		DG281AP-2		DG181AP/883
DG191AP	DG191AP		DG281AP/883		DG181AP/883
DG191AP-2	DG191AP/883		DG281BA		DG181BA
DG191AP/883	DG191AP/883		DG281BP		DG181BP
DG191BP	DG191BP		DG284AP		DG184AP
DG200AA	DG200AAA		DG284AP-2		DG184AP/883
DG200AAA	DG200AAA		DG284AP/883		DG184AP/883
DG200AAA-2	DG200AAA/883		DG284BP		DG184BP
DG200AAA/883	DG200AAA/883		DG287AA		DG187AA
DG200AAK	DG200AAK		DG287AA-2		DG187AA/883
DG200AAK-2	DG200AAK/883		DG287AA/883		DG187AA/883
DG200AAK/883	DG200AAK/883		DG287AP		DG187AP
DG200AAP	DG200AAP		DG287AP-2		DG187AP/883
DG200AAP-2	DG200AAP/883		DG287AP/883		DG187AP/883
DG200AAP/883	DG200AAP/883		DG287BA		DG187BA
DG200ABA	DG200ABA		DG287BP		DG187BP
DG200ABK	DG200ABK		DG290AP		DG190AP
DG200ABP	DG200ABP		DG290AP-2		DG190AP/883
DG200ACA	DG200ACA		DG290AP/883		DG190AP/883
DG200ACJ	DG200ACJ		DG290BP		DG190BP
DG200AK	DG200AAK		DG300AAA	DG300AAA	
DG200BA	DG200ABA		DG300AAA-2	DG300AAA/883	
DG200BK	DG200ABK		DG300AAA/883	DG300AAA/883	
DG200CJ	DG200ACJ		DG300AAK	DG300AAK	
DG201AAK	DG201AAK		DG300AAK-2	DG300AAK/883	
DG201AAK-2	DG201AAK/883		DG300AAK/883	DG300AAK/883	
DG201AAK/883	DG201AAK/883		DG300ABA	DG300ABA	
DG201AAZ/883	DG201AAZ/883		DG300ACA	DG300ACA	
DG201ABK	DG201ABK		DG300ACJ	DG300ACJ	
DG201ACJ	DG201ACJ		DG300ACK	DG300ACK	
DG201ACY	DG201ADY		DG301AAA	DG301AAA	
DG201ADY	DG201ADY		DG301AAA-2	DG301AAA/883	
DG201AK	DG201AAK		DG301AAA/883	DG301AAA/883	
DG201AK/883	DG201AAK/883		DG301AAK	DG301AAK	
DG201BK	DG201ABK		DG301AAK-2	DG301AAK/883	
DG201CJ	DG201ACJ		DG301AAK/883	DG301AAK/883	
DG202AK	DG202AK		DG301AAZ/883	DG301AAZ/883	
DG202AK-2	DG202AK/883		DG301ABA	DG301ABA	
DG202AK/883	DG202AK/883		DG301ACA	DG301ACA	
DG202BK	DG202AK		DG301ACJ	DG301ACJ	
DG202CJ	DG202CJ		DG301ACK	DG301ACK	
DG211CJ	DG211CJ		DG302AAK	DG302AAK	
DG211CY	DG211DY		DG302AAK-2	DG302AAK/883	
DG211DY	DG211DY		DG302AAK/883	DG302AAK/883	
DG212CJ	DG212CJ		DG302ACJ	DG302ACJ	
DG212CY	DG212DY		DG302ACK	DG302ACK	
DG212DY	DG212DY				

# Cross Reference

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
DG303AAK	DG303AAK		DG387AAK-2	DG387AAK/883	
DG303AAK-2	DG303AAK/883		DG387AAK/883	DG387AAK/883	
DG303AAK/883	DG303AAK/883		DG387ABA	DG387ABA	
DG303AAZ/883	DG303AAZ/883		DG387ABK	DG387ABK	
DG303ACJ	DG303ACJ		DG387ACA	DG387ACA	
DG303ACK	DG303AAK		DG387ACJ	DG387ACJ	
DG303ACY	DG303ADY		DG387ACK	DG387ACK	
DG303ADY	DG303ADY		DG390AAK	DG390AAK	
DG304AAA	DG304AAA		DG390AAK-2	DG390AAK/883	
DG304AAA-2	DG304AAA/883		DG390AAK/883	DG390AAK/883	
DG304AAA/883	DG304AAA/883		DG390ABK	DG390ABK	
DG304AAK	DG304AAK		DG390ACJ	DG390ACJ	
DG304AAK-2	DG304AAK/883		DG390ACK	DG390ACK	
DG304AAK/883	DG304AAK/883		DG400AK	DG400AK	
DG304ABA	DG304ABA		DG400AK/883	DG400AK/883	
DG304ACA	DG304ACA		DG400CJ	DG400DJ	
DG304ACJ	DG304ACJ		DG400CK	DG400AK	
DG304ACK	DG304ACK		DG400DJ	DG400DJ	
DG305AAA	DG305AAA		DG400DY	DG400DY	
DG305AAA-2	DG305AAA/883		DG401AK	DG401AK	
DG305AAA/883	DG305AAA/883		DG401AK/883	DG401AK/883	
DG305AAK	DG305AAK		DG401AZ	DG401AZ	
DG305AAK-2	DG305AAK/883		DG401AZ/883	DG401AZ/883	
DG305AAK/883	DG305AAK/883		DG401CJ	DG401DJ	
DG305ABA	DG305AAA		DG401CK	DG401AK	
DG305ABK	DG305AAK		DG401DJ	DG401DJ	
DG305ACA	DG305AAA		DG401DY	DG401DY	
DG305ACJ	DG305AAK		DG402AK	DG402AK	
DG305ACK	DG305AAK		DG402AK/883	DG402AK/883	
DG306AAK	DG306AAK		DG402CJ	DG402DJ	
DG306AAK-2	DG306AAK/883		DG402CK	DG402AK	
DG306AAK/883	DG306AAK/883		DG402DJ	DG402DJ	
DG306ABK	DG306AAK		DG402DY	DG402DY	
DG306ACJ	DG306AAK		DG403AK	DG403AK	
DG306ACK	DG306AAK		DG403AK/883	DG403AK/883	
DG307AAK	DG307AAK		DG403AZ	DG403AZ/883	
DG307AAK-2	DG307AAK/883		DG403AZ/883	DG403AZ/883	
DG307AAK/883	DG307AAK/883		DG403CJ	DG403DJ	
DG307AAZ/883	DG307AAZ/883		DG403CK	DG403AK	
DG307ABK	DG307ABK		DG403DJ	DG403DJ	
DG307ACJ	DG307ACJ		DG403DY	DG403DY	
DG307ACK	DG307ACK		DG404AK	DG404AK	
DG308AAK	DG308AAK		DG404AK/883	DG404AK/883	
DG308AAK-2	DG308AAK/883		DG404CJ	DG404DJ	
DG308AAK/883	DG308AAK/883		DG404CK	DG404AK	
DG308ACJ	DG308ACJ		DG404DJ	DG404DJ	
DG308ACK	DG308ACK		DG404DY	DG404DY	
DG308ADY	DG308ADY		DG405AK	DG405AK	
DG309AK	DG309AK		DG405AK/883	DG405AK/883	
DG309AK-2	DG309AK/883		DG405AZ	DG405AZ/883	
DG309AK/883	DG309AK/883		DG405AZ/883	DG405AZ/883	
DG309CJ	DG309CJ		DG405CJ	DG405DJ	
DG309CK	DG309CK		DG405CK	DG405AK	
DG309DY	DG309DY		DG405DJ	DG405DJ	
DG381AAA	DG381AAA		DG405DY	DG405DY	
DG381AAA-2	DG381AAA/883		DG408AK	DG408AK	
DG381AAA/883	DG381AAA/883		DG408AK/883	DG408AK/883	
DG381AAK	DG381AAK		DG408CJ	DG408DJ	
DG381AAK-2	DG381AAK/883		DG409AK	DG409AK	
DG381AAK/883	DG381AAK/883		DG409AK/883	DG409AK/883	
DG381ABA	DG381ABA		DG409DJ	DG409DJ	
DG381ABK	DG381ABK		DG409DY	DG409DY	
DG381ACA	DG381ACA		DG411AK	DG411AK	
DG381ACJ	DG381ACJ		DG411AK/883	DG411AK/883	
DG381ACK	DG381ACK		DG411DJ	DG411DJ	
DG384AAK	DG384AAK		DG411DY	DG411DY	
DG384AAK-2	DG384AAK/883		DG412AK	DG412AK	
DG384AAK/883	DG384AAK/883		DG412AK/883	DG412AK/883	
DG384ABK	DG384ABK		DG412DJ	DG412DJ	
DG384ACJ	DG384ACJ		DG412DY	DG412DY	
DG384ACK	DG384ACK		DG413AK	DG413AK	
DG387AAA	DG387AAA		DG413AK/883	DG413AK/883	
DG387AAA-2	DG387AAA/883		DG413DJ	DG413DJ	
DG387AAA/883	DG387AAA/883		DG413DY	DG413DY	
DG387AAK	DG387AAK				

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
DG417AK	DG417AK		DG5043AK-2	DG403AK/883	
DG417AK/883	DG417AK/883		DG5043AK/883	DG303AK/883	
DG417DJ	DG417DJ		DG5043CJ	DG403DJ	
DG417DY	DG417DY		DG5043CK	DG403AK	
DG418AK	DG418AK		DG5044AK	DG404AK	
DG418AK/883	DG418AK/883		DG5044AK-2	DG404AK/883	
DG418DJ	DG418DJ		DG5044AK/883	DG404AK/883	
DG418DY	DG418DY		DG5044CJ	DG404DJ	
DG419AK	DG419AK		DG5044CK	DG404AK	
DG419AK/883	DG419AK/883		DG5045AK	DG405AK	
DG419DJ	DG419DJ		DG5045AK-2	DG405AK/883	
DG419DY	DG419DY		DG5045AK/883	DG405AK/883	
DG421AK	DG421AK		DG5045CJ	DG405DJ	
DG421AK/883	DG421AK/883		DG5045CK	DG405AK	
DG421DJ	DG421DJ		DG5048AK/883	DG5048AK/883	
DG421DY	DG421DY		DG506AAK	DG506AAK	
DG423AK	DG423AK		DG506AAK-2	DG506AAK/883	
DG423AK/883	DG423AK/883		DG506AAK/883	DG506AAK/883	
DG423DJ	DG423DJ		DG506AAR	DG506AAR	
DG423DY	DG423DY		DG506AAR-2	DG506AAR/883	
DG425AK	DG425AK		DG506AAR/883	DG506AAR/883	
DG425AK/883	DG425AK/883		DG506AAZ/883	DG506AAZ/883	
DG425DJ	DG425DJ		DG506ABR	DG506ABR	
DG425DY	DG425DY		DG506ACJ	DG506ACJ	
DG441AK	DG441AK		DG506ACR	DG506ACR	
DG441AK/883	DG441AK/883		DG507AAK	DG507AAK	
DG441DJ	DG441DJ		DG507AAK-2	DG507AAK/883	
DG441DY	DG441DY		DG507AAK/883	DG507AAK/883	
DG442AK	DG442AK		DG507AAR	DG507AAR	
DG442AK/883	DG442AK/883		DG507AAR-2	DG507AAR/883	
DG442DJ	DG442DJ		DG507AAR/883	DG507AAR/883	
DG442DY	DG442DY		DG507AAZ/883	DG507AAZ/883	
DG444AK	DG444AK		DG507ABR	DG507ABR	
DG444AK/883	DG444AK/883		DG507ACJ	DG507ACJ	
DG444DJ	DG444DJ		DG507ACR	DG507ACR	
DG444DY	DG444DY		DG508AAK	DG508AAK	
DG445AK	DG445AK		DG508AAK-2	DG508AAK/883	
DG445AK/883	DG445AK/883		DG508AAK/883	DG508AAK/883	
DG445DJ	DG445DJ		DG508AAZ/883	DG508AAZ/883	
DG445DY	DG445DY		DG508ABK	DG508ABK	
DG480AK	DG480AK		DG508ABK	DG508ABK	
DG480AK/883	DG480AK/883		DG508ACJ	DG508ACJ	
DG480DJ	DG480DJ		DG508ACK	DG508ACK	
DG485AK	DG485AK		DG508ACY	DG508ACY	
DG485AK/883	DG485AK/883		DG508ADY	DG508ADY	
DG485DJ	DG485DJ		DG509AAK	DG509AAK	
DG501AK	DG501AP		DG509AAK-2	DG509AAK/883	
DG501AP	DG501AP		DG509AAK/883	DG509AAK/883	
DG501AP-2	DG501AP/883		DG509AAZ/883	DG509AAZ/883	
DG501AP/883	DG501AP/883		DG509ABK	DG509ABK	
DG501BK	DG501AP		DG509ACJ	DG509ACJ	
DG501BP	DG501AP		DG509ACK	DG509ACK	
DG501CJ	DG501CJ		DG509ADY	DG509ADY	
DG501DK	DG501AP		DG5140AK	DG400AK	
DG503AK	DG503AP		DG5140AK/883	DG400AK/883	
DG503AP	DG503AP		DG5140CJ	DG400DJ	
DG503AP-2	DG503AP/883		DG5140CK	DG400AK	
DG503BP	DG503AP		DG5141AK	DG401AK	
DG503CJ	DG503CJ		DG5141AK/883	DG401AK/883	
DG5040AK	DG400AK		DG5141CJ	DG401DJ	
DG5040AK-2	DG400AK/883		DG5141CK	DG401AK	
DG5040AK/883	DG400AK/883		DG5142AK	DG402AK	
DG5040CJ	DG400DJ		DG5142AK/883	DG402AK/883	
DG5040CK	DG400AK		DG5142CJ	DG402DJ	
DG5041AK	DG401AK		DG5142CK	DG402AK	
DG5041AK-2	DG401AK/883		DG5143AK/883	DG403AK/883	
DG5041AK/883	DG401AK/883		DG5143AKE	DG403AK	
DG5041CJ	DG401DJ		DG5143CJ	DG403DJ	
DG5041CK	DG401AK		DG5143CK	DG403AK	
DG5042AK	DG402AK		DG5144AK	DG404AK	
DG5042AK-2	DG402AK/883		DG5144AK/883	DG404AK/883	
DG5042AK/883	DG402AK/883		DG5144CJ	DG404DJ	
DG5042CJ	DG402DJ		DG5144CK	DG404AK	
DG5042CK	DG402AK		DG5145AK	DG405AK	
DG5043AK	DG403AK		DG5145AK/883	DG405AK/883	

# Cross Reference

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
DG5145CJ	DG405DJ		DGM182AL/883B		DG381AAL/883
DG5145CK	DG405AK		DGM182BA		DG381ABA
DG5241AK		DG421AK	DGM182BK		DG381ABK
DG5241CJ		DG421DJ	DGM182CJ		DG381ACJ
DG5241CK		DG421AK	DGM184AK	DG405AK	
DG5243AK		DG423AK	DGM184AK/HR	DG405AK/883	
DG5243CJ		DG423DJ	DGM184AK/883B	DG405AK/883	
DG5243CK		DG423AK	DGM184AL		DG184AL
DG5245AK		DG425AK	DGM184AL/HR		DG184AL/883
DG5245CJ		DG425DJ	DGM184AL/883B		DG184AL/883
DG5245CK		DG425AK	DGM184BK	DG405AK	
DG526AR	DG526AR		DGM184CJ	DG405DJ	
DG527AR	DG527AR		DGM185AK	DG405AK	
DG528AR	DG528AR		DGM185AK/HR	DG405AK/883	
DG529AR	DG529AR		DGM185AK/883B	DG405AK/883	
DG534AP/883	DG534AP/883		DGM185AL		DG185AL
DG534DJ	DG534DJ		DGM185AL/HR		DG185AL/883
DG535AP	DG535AP/883		DGM185AL/883B		DG185AL/883
DG535AP/883	DG535AP/883		DGM185BK	DG405AK	
DG535CY	DG536DN		DGM185CJ	DG405DJ	
DG535DJ	DG535DJ		DGM187AA		DG387AAA
DG536AM	DG536AM		DGM187AA/HR		DG387AAA/883
DG536CY	DG536DN		DGM187AA/883B		DG387AAA/883
DG536DN	DG536DN		DGM187AK		DG387AAK
DG536DY	DG536DY		DGM187AK/HR		DG387AAK
DG538AP	DG538AP		DGM187AK/883B		DG387AAK/883
DG538DJ	DG538DJ		DGM187BA		DG387ABA
DG538DN	DG538DN		DGM187BK		DG387ABK
DG546AK/883	DG546AK/883		DGM187CJ		DG387ACJ
DG546AZ/883	DG546AZ/883		DGM188AA		DG387AAA
DG546DJ	DG546DJ		DGM188AA/HR		DG387AAA/883
DG548AAK	DG548AAK		DGM188AA/883B		DG387AAA/883
DG548AAK/883	DG548AAK/883		DGM188AK		DG387AAK
DG548AAZ	DG548AAZ		DGM188AK/HR		DG387AAK
DG548ABK	DG548ABK		DGM188AL		DG387AAL
DG548ACJ	DG548ACJ		DGM188AL/HR		DG387AAL/883
DG548ADY	DG548ADY		DGM188AL/883B		DG387AAL/883
DG548DJ	DG548DJ		DGM188BA		DG387ABA
DG566AP	DG566AP		DGM188BK		DG387ABK
DG566AP-2	DG566AP-2		DGM188CJ		DG387ACJ
DG566CJ	DG566CJ		DGM190AK	DG403AK	
DG566DP	DG566DP		DGM190AK/HR	DG403AK/883	
DG568AP	DG568AP		DGM190AK/883B	DG403AK/883	
DG568AP-2	DG568AP-2		DGM190AL		DG190AL
DG568BP	DG568BP		DGM190AL/HR		DG190AL/883
DG568CJ	DG568CJ		DGM190AL/883B		DG190AL/883
DG569AP	DG569AP		DGM190BK	DG403AK	
DG569AP-2	DG569AP-2		DGM190CJ	DG403DJ	
DG569BP	DG569BP		DGM191AK	DG403AK	
DG569CJ	DG569CJ		DGM191AK/HR	DG403AK/883	
DG611AP/883	DG601AP/883		DGM191AK/883B	DG403AK	
DG611DJ	DG601DJ		DGM191AL		DG191AL
DG611DY	DG601DY		DGM191AL/HR		DG191AL/883
DG841AM/883	DG841AM/883		DGM191AL/883B		DG191AL/883
DG841DN	DG841DN		DGM191BK	DG403AK	
DG908AK	DG908AK		DGM191CJ	DG403DJ	
DG908AK/883	DG908AK/883		DGP201AAK	DGP201AAK	
DG908DJ	DG908DJ		DGP201AAK883	DGP201AAK883	
DG908DY	DG908DY		DGP201AAZ883	DGP201AAZ883	
DGM181AA		DG381AAA	DGP201ADJ	DGP201ADJ	
DGM181AA/HR		DG381AAA/883	DGP201ADY	DGP201ADY	
DGM181AA/883B		DG381AAA/883	DGP303AAK883	DGP303AAK883	
DGM181AK		DG381AAK	DGP303AAZ883	DGP303AAZ883	
DGM181AK/HR		DG381AAK	DGP303ADJ	DGP303ADJ	
DGM181AK/883B		DG381AAK/883	DGP303ADY	DGP303ADY	
DGM181BA		DG381ABA	DGP508AAK	DGP508AAK	
DGM181BK		DG381ABK	DGP508AAK883	DGP508AAK883	
DGM181CJ		DG381ACJ	DGP508AAZ883	DGP508AAZ883	
DGM182AA		DG381AAA	DGP508ADJ	DGP508ADJ	
DGM182AA/HR		DG381AAA/883	G116AP-2		G116AP
DGM182AA/883B		DG381AAA/883	G116BP	G116BP	
DGM182AK		DG381AAK	G117AL	G117AL	
DGM182AK/HR		DG381AAK/883	G117AL-2		G117AL
DGM182AL		DG381AAL	G118AP	G118AP	
DGM182AL/HR		DG381AAL/883			



Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
G119AL	G119AL		HI1-506L-8	DG526AK/883	
G119AL-2		GI19AL	HI1-507-2	DG507AAR	
G119AP	G119AP		HI1-507-8	DG507AAR/883	
HI1-200-2	DG200AAK		HI1-507A-2		DG507AAR
HI1-200-4	DG200ABK		HI1-507A-5		DG507ACR
HI1-200-5	DG200ACK		HI1-507A-7		DG507AAR/883
HI1-200-8	DG200AAK/883		HI1-507A-8		DG507AAR/883
HI1-201-2	DG201AAK		HI1-507L-2	DG527AK	
HI1-201-8	DG201AAK/883		HI1-507L-5	DG527CK	
HI1-201HS2		DG271AK	HI1-507L-8	DG527AK/883	
HI1-201HS5		DG271AK	HI1-508-2	DG508AAK	
HI1-201HS8		DG271AK/883	HI1-508-5	DG508ACK	
HI1-300-2	DG300AAK		HI1-508-8	DG508AAK/883	
HI1-300-5	DG300ACK		HI1-508A-2		DG548AK
HI1-300-8	DG300AAK/883		HI1-508A-5		DG548CK
HI1-301-2	DG301AAK		HI1-508A-7		DG548AK/883
HI1-301-5	DG301ACK		HI1-508A-8		DG548AK/883
HI1-301-8	DG301AAK/883		HI1-508L-2	DG528AK	
HI1-302-2	DG302AAK		HI1-508L-5	DG528CK	
HI1-302-5	DG302ACK		HI1-508L-8	DG528AK/883	
HI1-302-8	DG302AAK/883		HI1-509-2	DG509AAK	
HI1-303-2	DG303AAK		HI1-509-5	DG509ACK	
HI1-303-5	DG303ACK		HI1-509-8	DG509AAK/883	
HI1-303-8	DG303AAK/883		HI1-509L-2	DG529AK	
HI1-304-2	DG304AAK		HI1-509L-5	DG529CK	
HI1-304-5	DG304ACK		HI1-509L-8	DG529AK/883	
HI1-304-8	DG304AAK/883		HI1-548-1	DG548AK	
HI1-305-2	DG305AAK		HI1-548-5	DG548DJ	
HI1-305-5	DG305ACK		HI1-548-8	DG548AK/883	
HI1-305-8	DG305AAK/883		HI1-549-1	DG549AK	
HI1-306-2	DG306AAK		HI1-549-5	DG549DJ	
HI1-306-5	DG306ACK		HI1-549-8	DG549AK/883	
HI1-306-8	DG306AAK/883		HI1-7541JD-5	SI7541AJN	
HI1-307-2	DG307AAK		HI1-7541KD-5	SI7541AKN	
HI1-307-5	DG307ACK		HI1-7541SD-2	SI7541ASD	
HI1-307-8	DG307AAK/883		HI1-7541TD-2	SI7541ATD	
HI1-381-2	DG381AAK		HI2-200-2	DG200AAA	
HI1-381-5	DG381ACK		HI2-200-4	DG200ABA	
HI1-381-8	DG381AAK/883		HI2-200-5	DG200ACA	
HI1-384-2		DG384AAK	HI2-200-8	DG200AAA/883	
HI1-384-5		DG384AAK	HI2-300-2	DG300AAA	
HI1-384-8		DG384AAK/883	HI2-300-5	DG300ACA	
HI1-387-2	DG387AAK		HI2-300-8	DG300AAA/883	
HI1-387-5	DG387ACK		HI2-301-2	DG301AAA	
HI1-387-8	DG387AAK/883		HI2-301-5	DG301ACA	
HI1-390-2		DG390AAK	HI2-301-8	DG301AAA/883	
HI1-390-5		DG390AAK	HI2-304-2	DG304AAA	
HI1-390-8		DG390AAK/883	HI2-304-5	DG304ACA	
HI1-5040-2	DG400AK		HI2-304-8	DG304AAA/883	
HI1-5040-5	DG400ACK		HI2-305-2	DG305AAA	
HI1-5040-8	DG400AK/883		HI2-305-5	DG305ACA	
HI1-5041-2	DG401AK		HI2-305-8	DG305AAA/883	
HI1-5041-5	DG401ACK		HI2-381-2	DG381AAA	
HI1-5041-8	DG401AK/883		HI2-381-5	DG381ACA	
HI1-5042-2	DG402AK		HI2-381-8	DG381AAA/883	
HI1-5042-5	DG402ACK		HI2-387-2	DG387AAA	
HI1-5042-8	DG402AK/883		HI2-387-5	DG387ACA	
HI1-5043-2	DG403AK		HI2-387-8	DG387AAA/883	
HI1-5043-5	DG403ACK		HI3-200-5	DG200ACJ	
HI1-5043-8	DG403AK/883		HI3-201-5	DG201ACJ	
HI1-5044-2	DG404AK		HI3-201HS5		DG271DJ
HI1-5044-5	DG404ACK		HI3-300-5	DG300ACJ	
HI1-5044-8	DG404AK/883		HI3-301-5	DG301ACJ	
HI1-5045-2	DG405AK		HI3-302-5	DG302ACJ	
HI1-5045-5	DG405ACK		HI3-303-5	DG303ACJ	
HI1-5045-8	DG405AK/883		HI3-304-5	DG304ACJ	
HI1-506-2	DG506AAR		HI3-305-5	DG305ACJ	
HI1-506-7		DG506AAR/883	HI3-306-5	DG306ACJ	
HI1-506-8	DG506AAR/883		HI3-307-5	DG307ACJ	
HI1-506A-2		DG506AAR	HI3-381-5	DG381ACJ	
HI1-506A-5		DG506ABR	HI3-384-5		DG384ADJ
HI1-506A-7		DG506AAR/883	HI3-387-5		DG390ADJ
HI1-506A-8		DG506AAR/883	HI3-390-5		
HI1-506L-2	DG526AK		HI3-5040-5	DG400DJ	
HI1-506L-5	DG526CK				

# Cross Reference

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
H3-5041-5	DG401DJ		IH5043MJE/883	DG403AK/883	
H3-5042-5	DG402DJ		IH5044CJE	DG404AK	
H3-5043-5	DG403DJ		IH5044CPE	DG404DJ	
H3-5044-5	DG404DJ		IH5044MJE	DG404AK	
H3-5045-5	DG405DJ		IH5044MJE/HR	DG404AK/883	
H3-506-5	DG506ACJ		IH5044MJE/883	DG404AK/883	
H3-506L-5	DG526ACJ		IH5045CJE	DG405AK	
H3-507A-5		DG507ACJ	IH5045CPE	DG405DJ	
H3-507L-5	DG527CJ		IH5045MJE	DG405AK	
H3-508-5	DG508ACJ		IH5045MJE/HR	DG405AK/883	
H3-508A-5		DG548CJ	IH5045MJE/883	DG405AK/883	
H3-508L-5	DG528CJ		IH5108CPE	DG908DJ	
H3-509-5	DG509ACJ		IH5108JJE	DG908DK	
H3-509L-5	DG529CJ		IH5108MJE	DG908AK	
H4-506-8		DG506AAZ/883	IH5140CJE	DG400AAK	
H4-506A-8		DG506AAZ/883	IH5140CPE	DG400ADJ	
H4-507A-8		DO507AAZ/883	IH5140MJE	DG400AK	
H4-508A-8		DG547AAZ/883	IH5140MJE/883	DG400AK/883	
ICL7135CJl	SI7135CK		IH5141CJE	DG401AK	
ICL7135CPI	SI7135CJ		IH5141CPE	DG401DJ	
ICL7652CPA	SI7652DH		IH5141MJE	DG401AK	
ICL7652CPD	SI7652DJ		IH5141MJE/883	DG401AK/883	
ICL7652CTV	SI7652DA		IH5142CJE	DG402AK	
ICL7652JJD	SI7652DK		IH5142CPE	DG402DJ	
ICL7652ITV	SI7652DA		IH5142MJE	DG402AK	
ICL7660CBA	SI7660DY		IH5142MJE/883	DG402AK/883	
ICL7660CPA	SI7660CJ		IH5143CJE	DG403AK	
ICL7660CTV	SI7660CA		IH5143CPE	DG403DJ	
ICL7660MTV	SI7660AA		IH5143MJE	DG403AK	
ICL7660SCBA		SI7660DY	IH5143MJE/883	DG403AK/883	
ICL7660SCPA		SI7660CJ	IH5144CJE	DG404AK	
ICL7660SCTV		SI7660CA	IH5144CPE	DG404DJ	
ICL7660SMTV		SI7660AA	IH5144MJE	DG404AK	
ICL7662CPA	SI7661CJ		IH5144MJE/883	DG404AK/883	
ICL7662CTV	SI7661CA		IH5145CJE	DG405AK	
IH181CJD	DG181BP		IH5145CPE	DG405DJ	
IH181CTW	DG181BA		IH5145MJE	DG405AK	
IH181MTW	DG181AA		IH5145MJE/883	DG405AK/883	
IH182CJD	DG182BP		IH5208CPE	DG509ADJ	
IH182CTW	DG182BA		IH5208JJE	DG509ADK	
IH182MJD	DG182AP		IH5208MJE	DG509AAK	
IH182MTW	DG182AA		IH6108CJE		DG508ACK
IH184CJE	DG184BP		IH6108CPE		DG508ACJ
IH184MJE	DG184AP		IH6108MJE		DG508AAK
IH185CJE	DG185BP		IH6116CJl		DG506ACK
IH185MJE	DG185AP		IH6116CPI		DG506ACJ
IH187CTW	DG187BA		IH6116MJl		DG506AAK
IH187MJD	DG187AP		IH6208CJE		DG509ACK
IH187MTW	DG187AA		IH6208CPE		DG509ACJ
IH188CJD	DG187BP		IH6208MJE		DG509AAK
IH188CTW	DG188BA		IH6216CJl		DG507ACK
IH188MJD	DG188AP		IH6216CPI		DG507ACJ
IH188MTW	DG188AA		IH6216MJl		DG507AAK
IH190CJE	DG190BP		IH9108CPE	DG568CJ	
IH190MJE	DG190AP		IH9108JJE	DG568BP	
IH191CJE	DG191BP		IH9108MJE	DG568AP	
IH5040CJE	DG400AK		LD10CJ	LD110CJ	
IH5040CPE	DG400DJ		LD11ACJ	LD11ACJ	
IH5040MJE	DG400AK		LD14CR	LD114CR	
IH5040MJE/HR	DG400AK/883		LD120CJ	LD120CJ	
IH5040MJE/883	DG400AK/883		LD121ACJ	LD121ACJ	
IH5041CJE	DG401AK		LD122CJ	LD122CJ	
IH5041CPE	DG401DJ		LF11201D		DG411AK
IH5041MJE	DG401AK		LF11201N		DG411DJ
IH5041MJE/HR	DG401AK/883		LF11202D		DG412AK
IH5041MJE/883	DG401AK/883		LF12201D		DG411AK
IH5042CJE	DG402AK		LF12202D		DG412AK
IH5042CPE	DG402DJ		LF12202N		DG412DJ
IH5042MJE	DG402AK		LF13201D		DG411AK
IH5042MJE/HR	DG402AK/883		LF13201N		DG411DJ
IH5042MJE/883	DG402AK/883		LF13202D		DG412AK
IH5043CJE	DG403AK		LF13202N		DG412DJ
IH5043CPE	DG403DJ		LTC1044CH		SI7660CA
IH5043MJE	DG403AK		LTC1044MH		SI7660AA
IH5043MJE/HR	DG403AK/883				

Part Number	Siliconx Direct Replacement	Siliconx Similar Replacement	Part Number	Siliconx Direct Replacement	Siliconx Similar Replacement
LTC1052CH		SI7652DH1	PM7541ABX	SI7541ASD	
LTC1052CJ		SI7652DK	PM7541AGP	SI7541AKN	
LTC1052CN		SI7652CJ	PM7541ANP	SI7541AJN	
LTC1052MH		SI7652AA	PM7545AR	SI7545GUD	
LTC1052MJ		SI7652AK	PM7545BR	SI7545UD	
LTC7652CH		SI7652DH1	PM7545GP	SI7545GLN	
L144AL	L144AL		PM7545HP	SI7545LN	
L144BL	L144AL		PM7645AR	SI8045GUD	
L161AL-2	L161AL/883		PM7645BR	SI8045UD	
L161AL/883	L161AL/883		PM7645GP	SI8045GLN	
L161AP	L161AP		PM7645HP	SI8045LN	
L161AP-2	L161AP/883		SI25HC04CJ	SI2504CJ	
L161AP/883	L161AP/883		SI2504CJ	SI2504CJ	
L161BP	L161BP		SI3002		SI3002AA
L161CJ	L161CJ		SI3002A	SI3002AA	
MAX331MJE	DG411AK		SI3002AA	SI3002AA	
MAX332MJE	DG412AK		SI3002AP	SI3002AP	
MPC16S		DG506ABK	SI3002BK	SI3002BP	
MPC4D		DG509ADK	SI3002BP	SI3002BP	
MPC8D		DG507ABK	SI3705DK		DG501DK
MPC8S		DG508ADK	SI3705142K		DG501DK
MP200DIAA		DG200AAA	SI3705143K		DG501DK
MP200DIAP		DG200AAK	SI3705192K		DG501DK
MP200DIBA		DG200ABA	SI3705192P		DG501DK
MP200DICJ		DG200ACJ	SI3705193K		DG501DK
MP200DIPB		DG200ABK	SI6009DL		DG501DK
MP201DIAP		DG411AK	DG411AK	SI7240JN	G118AL
MP201DIBP		DG411AK	DG411AK	SI7240KN	
MP201DICJ		DG411DJ	SI7240AQ	SI7240KN	
MP302DIAP	DG302AP		SI7240BQ	SI7240AQ	
MP302DIBP	DG302BP		SI7240BQ	SI7240BQ	
MP302DICJ	DG302CJ		SI7240TD	SI7240TD	
MP303DIAP	DG303AP		SI7240SD	SI7240SD	
MP303DIBP	DG303BP		SI7250CK	SI7250CK	
MP303DICJ	DG303CJ		SI7533AQ	SI7533AQ	
MP7501JD		DG501BK	SI7533BQ	SI7533BQ	
MP7501JN		DG501CJ	SI7533CQ	SI7533CQ	
MP7501KD		DG501BK	SI7533JN	SI7533JN	
MP7501KN		DG501CJ	SI7533JP	SI7533JP	
MP7501SD		DG501AK	SI7533KN	SI7533KN	
MP7501TD		DG501AK	SI7533KP	SI7533KP	
MP7503JD		DG503BK	SI7533LN	SI7533LN	
MP7503JN		DG503CJ	SI7533SD	SI7533SD	
MP7503KD		DG503BK	SI7533TD	SI7533TD	
MP7503KN		DG503CJ	SI7533UD	SI7533UD	
MP7503SD		DG503AK	SI7541AJN	SI7541AJN	
MP7503TD		DG503AK	SI7541AKN	SI7541AKN	
MP7506JD	DG506ABK		SI7541ASD	SI7541ASD	
MP7506JN	DG506ACJ		SI7541ASD883	SI7541ASD883	
MP7506KD	DG506ABR		SI7541ASE883	SI7541ASE883	
MP7506KN	DG506ACJ		SI7541ATD	SI7541ATD	
MP7506SD	DG506AAK		SI7541ATD883	SI7541ATD883	
MP7506TD	DG506AAR		SI7541ATE883	SI7541ATE883	
MP7507JD	DG507ABK		SI7541JN	SI7541JN	
MP7507JN	DG507ACJ		SI7541KN	SI7541KN	
MP7507KD	DG507ABR		SI7541SD	SI7541SD	
MP7507KN	DG507ACJ		SI7541SD/883	SI7541SD/883	
MP7507SD	DG507AAK		SI7541SE/883	SI7541SE/883	
MP7507TD	DG507AAR		SI7541TD	SI7541TD	
MP7508KD		DG508ABK	SI7541TD/883	SI7541TD/883	
MP7508KN		DG508ACJ	SI7541TE/883	SI7541TE/883	
MP7508SD		DG508AAK	SI7542JN	SI7542JN	
MP7509KD		DG509ABK	SI7542KN	SI7542KN	
MP7509KN		DG509ACJ	SI7542SD/883	SI7542SD/883	
MP7509SD		DG509AAK	SI7542TD/883	SI7542TD/883	
MP7541TD	SI7541ATD		SI7543JN	SI7543JN	
MP7621JN	SI7541AJN		SI7543KN	SI7543KN	
MP7621KN	SI7541AKN		SI7543SD/883	SI7543SD/883	
MP7621SD	SI7541ASD		SI7543TD/883	SI7543TD/883	
MP7621TD	SI7541ATD		SI7545AE	SI7545AE	
MP7623JN	SI7541AJN		SI7545GLN	SI7545GLN	
MP7623KN	SI7541AKN		SI7545GUD	SI7545GUD	
MP7623SD	SI7541ASD		SI7545GUD/883	SI7545GUD/883	
MP7623TD	SI7541ATD		SI7545GUE/883	SI7545GUE/883	
PM7541AAX	SI7541ATD		SI7545JN	SI7545JN	

# Cross Reference

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
SI7545KN	SI7545KN		1109CP	DG400DJ	
SI7545LN	SI7545LN		1109MD	DG400AK	
SI7545SD	SI7545SD		1110CD	DG401AK	
SI7545TD	SI7545TD		1110MD	DG401AK	
SI7545UD	SI7545UD		11100P	DG401DJ	
SI7545UD/883	SI7545UD/883		1111CD	DG402AK	
SI7545UE/883	SI7545UE/883		1111CP	DG402DJ	
SI7652BA	SI7652DA		1111MD	DG402AK	
SI7652BK	SI7652DK		1112CD	DG403AK	
SI7652CA	SI7652DA		1112CP	DG403DJ	
SI7652CH	SI7652DH		1112MD	DG403AK	
SI7652CJ	SI7652DJ		1113CD	DG404AK	
SI7652DA	SI7652DA		1113CP	DG404DJ	
SI7652DH	SI7652DH		1113MD	DG404AK	
SI7652DJ	SI7652DJ		1114CD	DG405AK	
SI7652DK	SI7652DK		1114CP	DG405DJ	
SI7660AA	SI7660AA		1114MD	DG405AK	
SI7660CA	SI7660CA		1115CD	DG406AK	
SI7660CJ	SI7660CJ		1115CP	DG406DJ	
SI7660DY	SI7660DY		1115MD	DG406AK	
SI7661AA	SI7661AA		1116CD	DG407AK	
SI7661CA	SI7661CA		1116CP	DG407DJ	
SI7661CJ	SI7661CJ		1116MD	DG407AK	
SI7820LN	SI7820LN		38510/11101BAC	SJM181BAC	
SI7820KN	SI7820KN		38510/11101BCA	SJM181BCA	
SI7820LP	SI7820LP		38510/11101BCC	SJM181BCC	
SI7820KP	SI7820KP		38510/11101BIC	SJM181BIC	
SI7820CQ	SI7820CQ		38510/11102BAC	SJM182BAC	
SI7820BQ	SI7820BQ		38510/11102BCA	SJM182BCA	
SI7820UQ	SI7820UQ		38510/11102BCC	SJM182BCC	
SI7820TQ	SI7820TQ		38510/11102BIC	SJM182BIC	
SI7820TD/883	SI7820TD/883		38510/11103BAC	SJM184BAC	
SI8601AK/883	SI8601AK/883		38510/11103BEA	SJM184BEA	
SI8601DJ	SI8601DJ		38510/11103BEC	SJM184BEC	
SI8601DK	SI8601DK		38510/11104BAC	SJM185BAC	
SI8602AK/883	SI8602AK/883		38510/11104BEA	SJM185BEA	
SI8602DJ	SI8602DJ		38510/11104BEC	SJM185BEC	
SI8602DK	SI8602DK		38510/11105BAC	SJM187BAC	
SI8603AK/883	SI8603AK/883		38510/11105BCA	SJM187BCA	
SI8603DJ	SI8603DJ		38510/11105BCC	SJM187BCC	
SI8603DK	SI8603DK		38510/11105BIC	SJM187BIC	
SI8604AK/883	SI8604AK/883		38510/11106BAC	SJM188BAC	
SI8604DJ	SI8604DJ		38510/11106BCA	SJM188BCA	
SI8604DK	SI8604DK		38510/11106BCC	SJM188BCC	
SW-01BQ	DG201AAK		38510/11106BIC	SJM188BIC	
SW-01BQ883	DG201AAK/883		38510/11107BAC	SJM190BAC	
SW-01FQ	DG201ABK		38510/11107BEA	SJM190BEA	
SW-02BQ	DG202AAK		38510/11107BEC	SJM190BEC	
SW-02BQ883	DG202AAK/883		38510/11108BAC	SJM191BAC	
SW-02FQ	DG202ABK		38510/11108BEA	SJM191BEA	
SW-05BK	DG200AAA		38510/11108BEC	SJM191BEC	
SW-05BK883	DG200AAA/883		38510/11601BCA	SJM300BCA	
SW-05BY	DG200AAK		38510/11601BCC	SJM300BCC	
SW-05BY883	DG200AAK/883		38510/11601BIC	SJM300BIC	
SW-05FK	DG200ABA		38510/11602BCA	SJM301BCA	
SW-05FY	DG200ABK		38510/11602BCC	SJM301BCC	
SW-05GP	DG200ACJ		38510/11602BIC	SJM301BIC	
SW-201BQ		DG411AK	38510/11603BCA	SJM302BCA	
SW-201BQ883		DG411AK/883	38510/11603BCC	SJM302BCC	
SW-201FQ		DG411AK	38510/11604BCA	SJM303BCA	
SW-201GP		DG411DJ	38510/11604BCC	SJM303BCC	
SW-202BQ		DG412AK	38510/11605BCA	SJM304BCA	
SW-202BQ883		DG412AK/883	38510/11605BCC	SJM304BCC	
SW-202FQ		DG412AK	38510/11605BIC	SJM304BIC	
SW-202GP		DG412DJ	38510/11606BCA	SJM305BCA	
TL520N	SI8601DJ		38510/11606BCC	SJM305BCC	
TSC7135CJL	SI7135CK		38510/11606BIC	SJM305BIC	
TSC7135CPI	SI7135CJ		38510/11607BCA	SJM306BCA	
TSC7541JN	SI7541AJN		38510/11607BCC	SJM306BCC	
TSC7541KN	SI7541AKN		38510/11608BCA	SJM307BCA	
TSC7541SD	SI7541ASD		38510/11608BCC	SJM307BCC	
TSC7541TD	SI7541ATD		38510/12301ABCA	SJM200ABCA	
TSC7660COA	SI7660DY		38510/12301ABCC	SJM200ABCC	
TSC7660CPA	SI7660CJ		38510/12301ABIC	SJM200ABIC	
1109CD	DG400AK				

Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement	Part Number	Siliconix Direct Replacement	Siliconix Similar Replacement
38510/12302ABEA	SJM201ABEA		8100603EA	DG5142AK DESC	
38510/12302ABEC	SJM201ABEC		8100603IC	DG5142AA DESC	
38510/19001BXC	SJM506BXC		8100604EA	DG5143AK DESC	
38510/19003BXC	SJM507BXC		8100605EA	DG5144AK DESC	
38510/19007BEC	SJM508ABEC		8100605IC	DG5144AA DESC	
38510/19008BEC	SJM509ABEC		8100606EA	DG5145AK DESC	
7705201EA	DG508AAK DESC		8100609EA	DG5140AK DESC	
7705201EC	DG508AAK DESC		8100609IC	DG5140AA DESC	
7705301EA	DG201AAK DESC		8100610EA	DG5141AK DESC	
7705301EC	DG201AAK DESC		8100610IC	DG5141AA DESC	
7801401CA	DG129AK DESC		8100611EA	DG5142AK DESC	
7801401CC	DG129AP DESC		8100611IC	DG5142AA DESC	
8100601EA	DG5140AK DESC		8100612EA	DG5143AK DESC	
8100601IC	DG5140AA DESC		8100613EA	DG5144AK DESC	
8100602EA	DG5141AK DESC		8100613IC	DG5144AA DESC	
8100602IC	DG5141AA DESC		8100614EA	DG5145AK DESC	

This Cross Reference material is accurate to the best knowledge and belief of Siliconix Incorporated. Since individual circuit design and layout can influence device performance, the purchaser must be responsible for the ultimate selection and determination of interchangeability.





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# ANALOG SWITCHES AND MULTIPLEXERS

## INTRODUCTION

Siliconix is the world's leading supplier of high performance, precision solid-state analog switches and multiplexers. Through the implementation of state-of-the-art technologies (CMOS, DMOS, bipolar/PMOS, and JFET processes) in conjunction with advanced design techniques, the products shown in this section represent a broad selection of industrial, military, and commercial grade parts suiting a wide range of applications. Siliconix is dedicated to giving the designer the widest range of functions, performance, and packaging as standards to ensure ease of design.

The products in this section include all of the popular Siliconix "DG" series of single, dual, and quad analog switches, single-ended and differential multiplexers plus many new and preliminary devices.

Siliconix is branching out into the higher performance switch and multiplexer arena with our proprietary high voltage silicon gate DG400 family. The established DG200, DG300, and DG500 families are made on our mature metal gate process which gives adequate performance for many applications. If higher performance (i.e. lower ON resistance, leakage currents, and power dissipation with faster switching) is required in your application, then the DG400 family is recommended. Most of our DG4XX devices, including analog switches, multiplexers, latched switches, and switch arrays, incorporate ESDS protection  $> \pm 4000$  V. Single supply operation, charge injection optimization, and a wide range of packaging options including gull-wing small outline, PLCC and LCC packages are additional benefits of this family.

A wide range of preliminary products are covered in this section including multiplexers (DI and silicon gate), PolyMOS™ fast switches, and silicon gate switch arrays. In the near future, Siliconix will release two DI (dielectric isolation) multiplexers with overvoltage (DG548) and/or fault protection (DG908) and two high performance silicon gate multiplexers (DG408/409). If extremely fast switching and very low ON resistance are the most important parameters in your system, then the DG601 PolyMOS™ quad analog switches, pin compatible with the industry standards DG201A/202, are the devices of choice.

Switch arrays (serial-in, parallel-out) are a new architecture giving designers greater levels of flexibility in routing signals. The DG480/485 are silicon gate switch array multiplexers that allow control of any of eight switches. Now, summing node applications can be accomplished using a high performance switch array architecture.

Finally, Siliconix continues to expand the increasingly popular lines of U.S. MIL-M38510 QPL and European BS9000 approved parts which have been screened for use in military applications.

The following discuss important selection criteria for analog switches and multiplexers. See the detailed selector guide to make the job of selecting the correct part for a specific application easier.

## Functional Description

One of the most common control elements in electrical circuitry is the ON-OFF switch. The switch has evolved over the years from the manually operated circuit breaker of the early experimenters to the multi-switch integrated circuits of today. However, the function of the switch has remained the same; to electrically isolate or connect two sections of a circuit. The ideal switch has the following characteristics:

- 1) Zero ON resistance
- 2) Infinite OFF resistance
- 3) Instantaneous  $t_{ON}$  and  $t_{OFF}$  times

Although an analog switch is not perfect and can have many different parasitic elements (Figure 1), it can still be a very good approximation of the ideal switch. ON resistance ( $r_{DS(ON)}$ ) can be as low as  $10\ \Omega$ , OFF isolation can be as high as 90 dB (at 1 MHz), and switching speeds can reach 60 ns for a CMOS part, while PolyMOS™ can obtain 30 ns switching speeds.

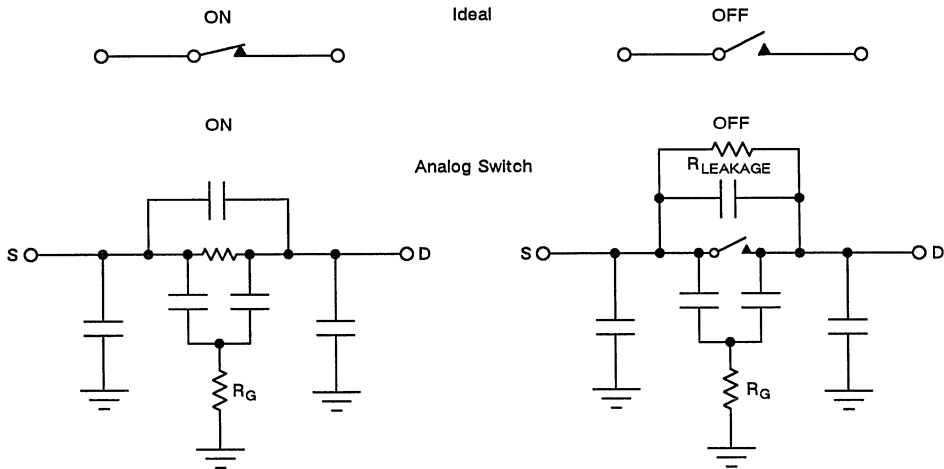


Figure 1. Comparison of the "Ideal" Switch to a Solid-state Analog Switch

## Analog Switch Types

Before discussing specific parameters of the Siliconix analog switch product line, a brief description and the prime differences between the four processes used in analog switches is provided.

### JFET

The n-channel JFETs used in analog switches such as the DG180 family are depletion mode devices. To maintain a depletion mode JFET switch in the ON state, the value  $V_{GS}$  should be at or near zero. The switch is turned OFF by making  $V_{GS}$  more negative than 6 volts. When the switch is ON,  $V_{GS}$  is maintained at zero by a floating gate drive circuit. This makes the ON resistance extremely constant over the entire analog signal range (Figure 2).

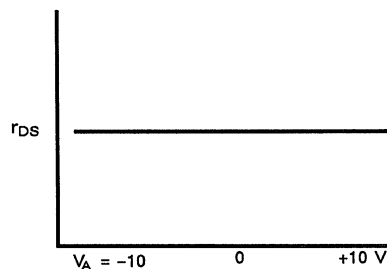


Figure 2. JFET "ON" Resistance

## PMOS

To maintain an enhancement mode PMOS switch in the ON state, the gate is held at a negative voltage that ensures that  $V_{GS}$  exceeds the threshold voltage of the FET even when the analog signal is at the extremes of its range. However, since the  $r_{DS(ON)}$  of a MOSFET is a function of  $V_{GS}$ , the ON resistance will vary with the analog signal voltage (Figure 3).

The variation in ON resistance of the PMOS analog switch is a serious limitation in some applications since it can cause distortion of the analog signal. This effect can be minimized if the load resistance is high compared to the switch resistance.

## DMOS

DMOS (double diffused MOS) switches are n-channel (NMOS) enhancement mode devices capable of sub-nanosecond switching speeds due to their short channel length and lateral, as opposed to vertical, current flow. Lateral construction also allows low parasitic capacitances which makes DMOS switches ideal for wideband signals (> 500 MHz). However, they exhibit similar ON resistance variations as the PMOS switches.

## CMOS

Since CMOS analog switches are parallel combinations of p- and n-channel MOSFETs, the effective ON resistance is a combination of the PMOS and NMOS resistance curves (Figure 4). This gives a fairly constant ON resistance over the entire analog voltage range. The CMOS switch also has the advantage of very low quiescent supply current because other than for channel leakage, no current flows in the driver except when a control input transition occurs.

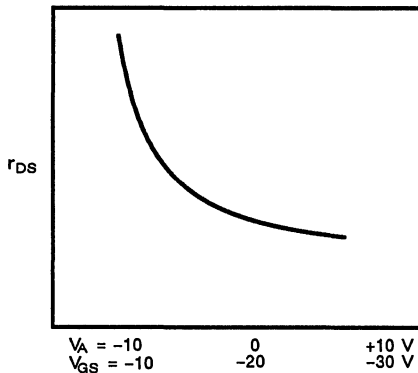


Figure 3. Variation of PMOS Switch Resistance with Signal Voltage

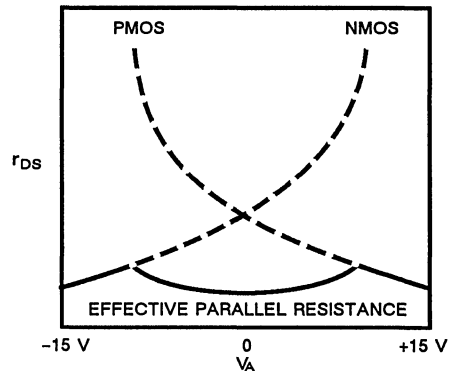
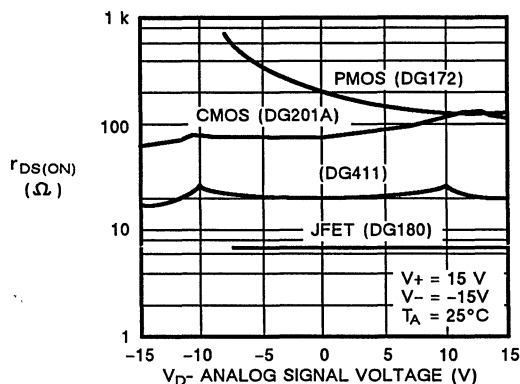


Figure 4. Graph of CMOS Switch Resistance vs. Analog Signal

## Metal Gate And Silicon Gate CMOS

Both metal and silicon gate technologies are incorporated into our CMOS processes, but each is used with separate product lines. The mature metal gate process, is used for our DG200, DG300, and DG500 families. Our newer silicon gate process (DG400 family) is recommended for applications needing state-of-the-art performance and versatility.

Figure 5 gives a comparison of the ON resistance curves for a JFET (DG180), a PMOS (DG172), a metal gate CMOS (DG201A) and a silicon gate CMOS (DG400) analog switches.



## Important Switch Parameters

Each switch family in the Siliconix product line has a set of distinct characteristics that make it suitable for certain types of applications. Several major specifications should be compared and prioritized before selecting an analog switch for a particular circuit.

### $r_{DS(ON)}$

This specification is simply the dc resistance of the channel when the analog switch is in the ON state. As explained earlier, the ON resistance of an analog switch depends upon the device type and the analog signal magnitude. Although the resistance may vary across the entire analog signal range, the worst case is normally specified on the data sheet.

### Switching Speed

Switching speed is the elapsed time from the application of the control signal on the input pin to the appearance (or disappearance) of the analog signal at the output. Switching speed can be affected by the load on the analog switch. Each data sheet shows a switching time test circuit with a standard load for comparison purposes.

### Switch Current

The amount of current that can be fed through the switch channel is sometimes important. For example, the DG411 can handle up to 100 mA of pulsed current or 30 mA of continuous current, while the DG180 can pass up to 200 mA of continuous current.

### Break-Before-Make vs. Make-Before-Break

For most analog switch applications, break-before-make switching is desired. This is the case because in most applications it is necessary to disconnect one signal source before connecting another to avoid source crosstalk. However, make-before-break switching is critical in some control circuits such as the feedback resistor gain selector for programmable gain op amps, to avoid opening the loop.

## Electrostatic Discharge Sensitivity (ESDS)

Electrostatic discharge is the transfer of charge that occurs when an object makes contact with a device at a different potential. The government, per MIL-883C method 3015, has classified three levels of voltage protection that a device must withstand on all pins (logic input pins are the most susceptible). Class 1 devices are protected to 1999 V, Class 2 from 2000 to 3999 V, and Class 3 protection is greater than 4000 V. Our DG200, DG300, DG506-509 families of metal gate devices are designed to withstand between 600 and 1999 V. Beginning with the DG411 series, all our new devices have Class 2 or 3 ESDS ratings and are marked accordingly.

## Charge Injection

Charge injection is the transfer of charge to a load from the gates of the FETs during switching. In a sample and hold circuit, charge injection is critical as the charge added or subtracted from the holding capacitor is seen as an error. The lower the charge injection the better. The DG400 family, especially the DG44X and DG411 series, are designed for balanced (near zero) charge injection. The DG601 and DG44X use internal compensation on the drain and/or source to minimize the charge injection seen by applications sensitive to this parameter.

## Power Supplies and Power Consumption

A bipolar supply means positive and negative voltages are used, while single supply means the negative supply is grounded. Most analog designs use bipolar supplies, but a growing number are turning to single supply operation to save board space and cost. Most of our devices work well with bipolar supplies but only a few function properly in the single supply mode. The DG400 family of analog switches and multiplexers not only functions superbly in a single supply mode, but is fully characterized and specified with  $V_+$  at 12 V and  $V_-$  at GND. The lower the power consumed by a device within a system the better. The DG400 family generally consumes under 10  $\mu\text{A}$  of supply current compared to the milliamps required by previous products.

## Interfacing

This can be one of the most important parameters of an analog switch application since so many possibilities exist. The two most important interface criteria are logic compatibility and microprocessor compatibility.

The two most common logic families are TTL and CMOS. The standard logic levels for both logics are displayed in Table 1. Remember that not all analog switches are compatible with both types of logic. Refer to the functional diagram section of each data sheet to determine the required logic levels.

Table 1

LOGIC	TTL	CMOS
"0"	$\leq 0.8 \text{ V}$	$\leq 1.5 \text{ V}$
"1"	$\geq 2.4 \text{ V}$	$\geq V_{CC}-1.5 \text{ V}$

Logic Levels for TTL and CMOS Compatibility

Microprocessor compatibility is a growing concern when designing with analog switches. Standard analog switches require a constant control signal present on the input to hold the switch in the desired position (ON or OFF). This could tie up a microprocessor control system unless external latches are added to control the switch. The DG221 and DG42X series have incorporated these latches, complete with control logic, onboard to minimize parts count and ease interface to microprocessor-based control systems.

## Multiplexing

Analog multiplexers represent a higher level of integration of analog switches. They have many (4, 8, 16, or more) inputs with only 1 or 2 common outputs. Multiplexers are used where it is necessary to transfer information from many signal channels at a transmitting point to a central or common receiving point, or vice versa. This is most often used when only one transmission line is available for all data transfer between points. The transmitted signals are in either analog or digital form, with multiplexers in this section being the analog variety that pass bipolar voltages or currents which are often obtained from transducers. The analog signals may represent any physical phenomenon such as temperature, pressure, velocity, speech, etc. Examples of this can be found in data acquisition, industrial process control, aircraft systems monitoring, medical electronics, telemetry, and communications.

### Differential vs. Single-Ended Multiplexing

When is it better to select a differential multiplexer versus a single-ended configuration? Figures 6 and 7 demonstrate both options. Single-ended multiplexing, as shown in Figure 6, applies to systems that have signal sources that are close to full-scale range and are referenced to a common point (usually ground). Another case is where differential signal sources with small signal amplitude (millivolt range) are generated by transducers. Instrumentation amplifiers can be used to provide a common reference for all of the signals and reduce feedthrough errors and losses while tailoring each signal source to a desired voltage (or current) to obtain the maximum resolution available in an A/D or D/A converter or other device driven by the multiplexer.

Differential multiplexing (Figure 7) is utilized when all signal sources are uniform or close to full-scale range and can tolerate switching transients or some mismatch without a significant degradation of the signal accuracy via the multiplexer. Major considerations are switch matching ( $r_{DS(ON)}$ ,  $I_{(OFF)}$ ), and capacitance), common-mode rejection, and the system's tolerance to switching transients introduced by the break-before-make switching sequence.

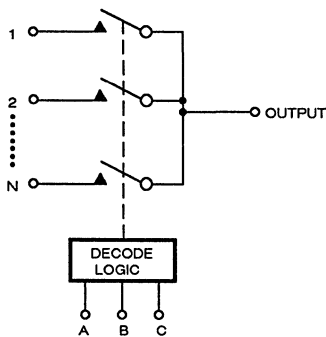


Figure 6. Single-Ended Multiplexing

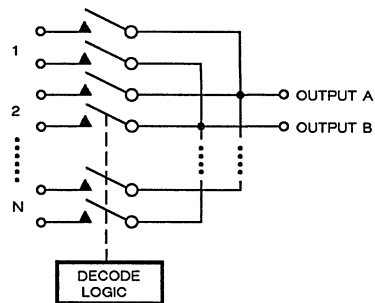


Figure 7. Differential Multiplexing

## Factors Affecting System Performance

In any multiplexer application, the following factors should be considered:

- 1) System Attenuation -- Includes loss in the analog signal caused by the multiplexer and the transmission path. This is a frequency dependent factor.
- 2) Channel Isolation -- At low frequencies, this is principally a function of channel OFF leakage currents, and at high frequencies, it is a function of device and system capacitances.
- 3) Crosstalk -- There are several sources of crosstalk, the main ones being overlapped between switching channels due to imperfect break-before-make switching, switch leakages, OFF switch capacitances, inter-switch capacitances, stray circuit capacitances, distortion in the transmission medium, etc.
- 4) Noise -- There are several sources of noise, including thermal or Johnson noise generated in any resistive components, crosstalk, leakages, switching transients, as well a thermal EMFs and transmission path pickup.
- 5) Switching Rate -- This is important in sampling system where it determines the maximum bandwidth frequency of the multiplexer (via the sampling theorem) and defines crosstalk errors.

# DG123

## 5-Channel SPST PMOS Analog Switch

### FEATURES

- Low Level Logic Control
- Make-Before-Break Switching Action
- Very Low Standby Power Requirements

### BENEFITS

- Reduces External Components Required
- Reduces Switching Errors

### APPLICATIONS

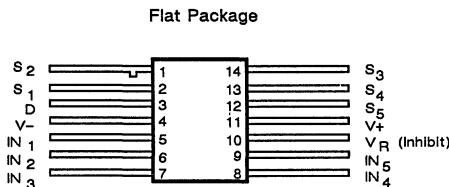
- Feedback Switching for Op Amps
- Commutation Systems
- Portable and Remote Operation

### DESCRIPTION

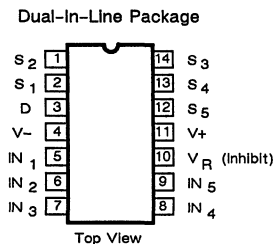
The DG123 is a 5-channel single-pole, single-throw analog switch designed for low level logic controlled analog switching in instrumentation, process control, and communications systems. Featuring make-before-break action, the DG123 can be used inside closed loop systems to select one of five inputs for multiplexing/demultiplexing of analog signals, or for gain bandwidth control (by switching passive elements), without opening the loop. The reference pin ( $V_R$ ) is normally connected to ground to allow a low-level input (0.4 V to 1.3 V) to control

the ON-OFF condition of each switch. The standby or OFF state power consumption is less than 0.5 mW. The DG123 is a bi-directional MOS switch, rated to handle  $\pm 10$  V analog signals at up to 30 mA continuous current. Each switch will block 20 V peak-to-peak signals when OFF. Package options are the 14-pin ceramic DIP and flatpack. The former is characterized for operation over the standard industrial, B suffix and military, A suffix temperature ranges, while the latter is specified for the military range only.

### PIN CONFIGURATION

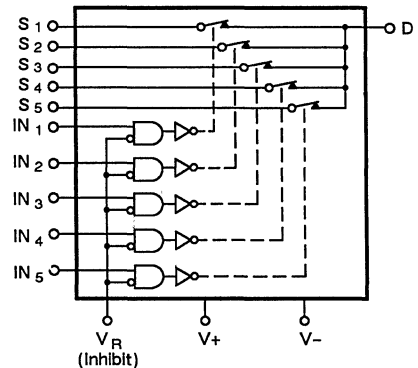


Top View  
Order Number: DG123AL/883



Order Numbers: DG123AP or DG123BP

### FUNCTIONAL BLOCK DIAGRAM



One 5-Channel Switch per Package\*

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq 0.4$  V  
Logic "1"  $\geq 1.3$  V

\* Switches Shown for Logic "1" Input



## ABSOLUTE MAXIMUM RATINGS

V <sub>+</sub> to V <sub>-</sub> .....	36 V
V <sub>D</sub> to V <sub>-</sub> .....	36 V
V <sub>S</sub> to V <sub>-</sub> .....	36 V
V <sub>D</sub> to V <sub>S</sub> .....	25 V
V <sub>S</sub> to V <sub>D</sub> .....	25 V
V <sub>R</sub> to V <sub>-</sub> .....	30 V
V <sub>IN</sub> to V <sub>-</sub> .....	30 V
V <sub>R</sub> to V <sub>IN</sub> .....	6 V
V <sub>IN</sub> to V <sub>R</sub> .....	2 V

Current (Any Terminal) .....	30 mA
Storage Temperature .....	-65 to 150°C
Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C
Power Dissipation (Package)*	
Flat Package** .....	750 mW
14-Pin DIP*** .....	825 mW

- \* All leads soldered or welded to PC board.
- \*\* Derate 10 mW/°C above 75°C.
- \*\*\* Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 10 V V <sub>-</sub> = -20 V V <sub>R</sub> = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-10	10	-10	10	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -1 mA I <sub>IN</sub> = 1 mA	V <sub>D</sub> = 10 V	1,3 2	70	100 125		125 150	Ω
			V <sub>D</sub> = 0	1,3 2	100	200 250		225 300	
			V <sub>D</sub> = -10 V	1,3 2	270	450 600		500 600	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V V <sub>IN</sub> = 0.4V	1 2		-1 -1000		-5 -100	nA	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>D</sub> = -10 V, V <sub>S</sub> = 10 V V <sub>IN</sub> = 0.4V	1 2		-1 -4000		-10 -300		
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 10 V I <sub>IN</sub> = 1 mA	1 2			4 4000	10 300		
<b>INPUT</b>									
Input Voltage HIGH	V <sub>INH</sub>	I <sub>IN</sub> = 1 mA	1 2 3			1 .8 1.3		1 1.0 1.3	V
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0.4 V	1,3 2			1 100		5 100	μA
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit (C <sub>L</sub> = 35 pF, R <sub>L</sub> = 2 kΩ)	1			0.3		0.5	μs
Turn-OFF Time	t <sub>OFF</sub>		1			2		2	

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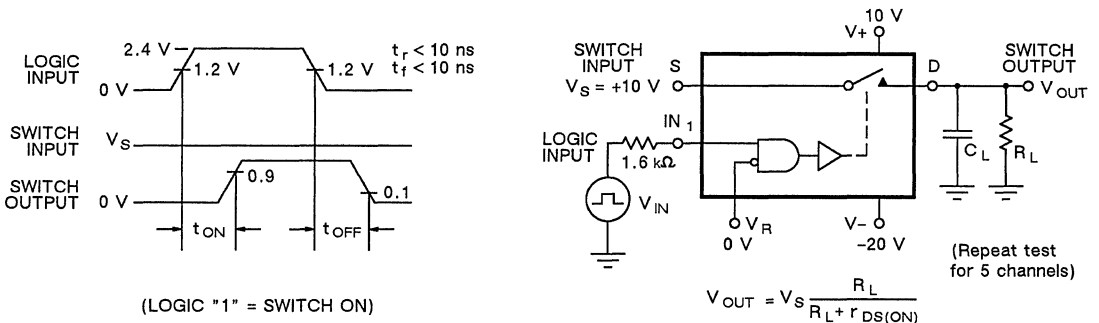
ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 10\text{ V}$ $V_- = -20\text{ V}$ $V_R = 0\text{ V}$			LIMITS				UNIT	
					A SUFFIX		B SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC (Cont'd)</b>										
Source-OFF Capacitance	$C_{S(OFF)}$	$V_S = 0\text{ V}, I_D = 0$ $f = 1\text{ MHz}$	1	5						pF
Drain-OFF Capacitance	$C_{D(OFF)}$	$V_D = 0\text{ V}, I_S = 0$ $f = 1\text{ MHz}$	1	18						
Off Isolation		$R_L = 100\ \Omega, C_L = 3\text{ pF}$ $f = 5\text{ MHz}$	1	>50						dB
<b>SUPPLY</b>										
Positive Supply Current	$I_+$	One Channel ON $I_{IN} = 1\text{ mA}$	1			3		3		mA
Negative Supply Current	$I_-$		1		-6		-6			
Reference Supply Current	$I_R$		1		-0.5		-0.5			
Positive Supply Current	$I_+$	All Channels OFF $V_{IN} = 0.4\text{ V}$	1			15		25		$\mu\text{A}$
Negative Supply Current	$I_-$		1		-20		-40			
Reference Supply Current	$I_R$		1		-10		-20			

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



# DG125

## 5-Channel SPST PMOS Analog Switch

### FEATURES

- Internal Zener Diode Protection
- Low Standby Power Requirements ( $P_{STDBY} < 0.5 \text{ mW}$ )
- Low OFF Leakage
- Low Level Logic Control

### BENEFITS

- Reduces Switching Errors
- Reduces External Components

### APPLICATIONS

- Communication Systems
- Portable and Battery Operation
- Op Amp Switching
- Variable Gain Switching

### DESCRIPTION

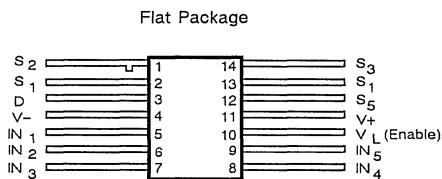
The DG125 is a 5-channel single-pole, single-throw analog switch designed for low level logic controlled analog switching in instrumentation, process control, and communications systems. Featuring make-before-break action, the DG125, built on Siliconix's PMOS process, can be used inside closed loop systems to select one or more of five inputs for multiplexing/demultiplexing, summing of analog signals, or for gain bandwidth control (by switching passive elements), without opening the loop.

In standby or OFF state, power consumption is less than 0.5 mW. The DG125 is a bi-directional MOS switch, rated to handle  $\pm 10 \text{ V}$  analog signals at up to 30 mA continuous current. Each switch will block 20 V peak-to-peak signals when OFF.

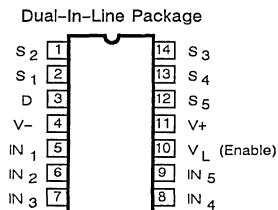
Packaging for the DG125 includes 14-pin side braze and flatpack options. Performance grades include both the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ) temperature ranges. The flatpack option is only available in the military grade.

**5**

### PIN CONFIGURATION

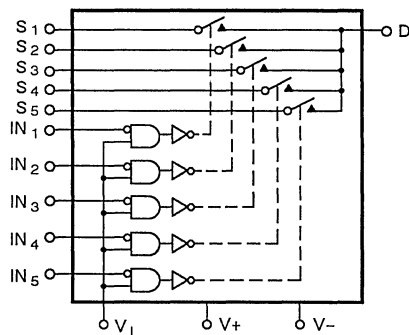


Top View  
Order Number: DG125AL/883



Top View  
Order Numbers: DG125AP or DG125BP

### FUNCTIONAL BLOCK DIAGRAM



One 5-Channel Switch per Package\*

Truth Table

LOGIC	SWITCH
0	ON
1	OFF

Logic "0"  $\leq 0.5 \text{ V}$   
Logic "1"  $\geq 4.1 \text{ V}$

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

$V_+$ to $V_-$ .....	36 V	Current, (Any Terminal) .....	30 mA
$V_D$ to $V_-$ .....	36 V	Storage Temperature .....	-65 to 150°C
$V_S$ to $V_-$ .....	36 V	Operating Temperature (A Suffix) .....	-55 to 125°C
$V_D$ to $V_S$ .....	25 V	(B Suffix) .....	-25 to 85°C
$V_S$ to $V_D$ .....	25 V	Power Dissipation (Package)*	
$V_L$ to $V_-$ .....	30 V	Flat Package** .....	750 mW
$V_{IN}$ to $V_-$ .....	30 V	14-Pin DIP*** .....	825 mW
$V_L$ to $V_{IN}$ .....	6 V	* All leads soldered or welded to PC board.	
		** Derate 10 mW/°C above 75°C.	
		*** Derate 11mW/°C above 75°C.	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 10\text{ V}$ $V_- = -20\text{ V}$ $V_L = 4.5\text{ V}$	LIMITS						UNIT	
			1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$		1,2,3		-10	10	-10	10	V	
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -1\text{ mA}$ $V_{IN} = 0.5\text{ V}$	$V_D = 10\text{ V}$	1,3 2	70		100 125		125 150	$\Omega$
			$V_D = 0\text{ V}$	1,3 2	100		200 250		225 300	
			$V_D = -10\text{ V}$	1,3 2	270		450 600		500 600	
Source OFF Leakage Current	$I_{S(OFF)}$	$V_S = -10\text{ V}, V_D = 10\text{ V}$ $V_{IN} = 4.1\text{ V}$	1 2	-0.02	-1 -1000			-5 -100	nA	
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_D = -10\text{ V}, V_S = 10\text{ V}$ $V_{IN} = 4.1\text{ V}$	1 2	-0.7	-1 -4000			-10 -300		
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_D = 10\text{ V}, V_{IN} = 0.5\text{ V}$ $I_S = 0$	1 2	-0.003		4 4000		10 300		
<b>INPUT</b>										
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 4.1\text{ V}$	1,3 2	0.006	-1 -10	1 10	-10 -10	10 10	$\mu\text{A}$	
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0.5\text{ V}$	1,3 2	-0.5	-0.7 -0.7			-1 -1	mA	
<b>DYNAMIC</b>										
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit	1	0.1		0.3		0.5	$\mu\text{s}$	
Turn-OFF Time	$t_{OFF}$		1	0.65		2		2		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = 10 V V <sub>-</sub> = -20 V V <sub>L</sub> = 4.5 V	LIMITS						UNIT	
			1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC (Cont'd)</b>										
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V, I <sub>D</sub> = 0 f = 1 MHz	1	3						pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0 V, I <sub>S</sub> = 0 f = 1 MHz	1	7						
Off Isolation		R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 3 pF f = 5 MHz	1	> 50						dB
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	One Channel ON V <sub>IN</sub> = 0.5 V	1	1.4		3		3		mA
Negative Supply Current	I <sub>-</sub>		1	-2.4		-6		-6		
Logic Supply Current	I <sub>L</sub>		1	1.15		3		3		
Positive Supply Current	I <sub>+</sub>	All Channels OFF V <sub>IN</sub> = 4.1 V	1	0.1		15		25		μA
Negative Supply Current	I <sub>-</sub>		1	-0.02		-20		-40		
Logic Supply Current	I <sub>L</sub>		1	0.04		20		20		

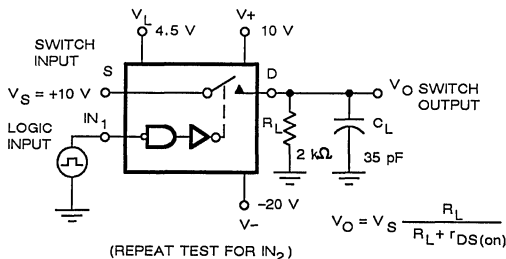
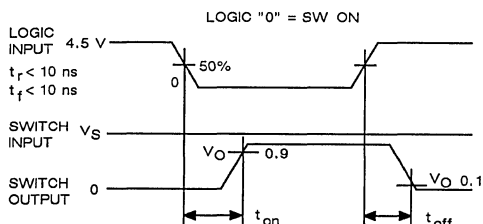
**5**

**NOTES:**

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- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for V<sub>S</sub> = constant with logic input waveform as shown. Note that V<sub>S</sub> may be + or - as per switching time test circuit. V<sub>O</sub> is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



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**APPLICATION HINTS**


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V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>L</sub> Logic Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
10	-20	4.5	4.1/0.5	-10 to 10
15	-15	4.5	4.1/0.5	-5 to 15
20	-10	4.5	4.1/0.5	0 to 20

# DG126/129/140

## Dual DPST JFET Analog Switches

### FEATURES

- < 1 mW Standby Power
- Bipolar Drivers
- Constant  $r_{DS(ON)}$  Over Signal Range
- OFF Isolation > 60 dB @ 1 MHz

### BENEFITS

- Minimizes Standby Power Requirements
- Better Radiation Tolerance
- Less Distortion
- Higher Frequency Switching

### APPLICATIONS

- Portable and Battery Powered Systems
- Switching in Satellite Applications
- Low Distortion Circuits
- High Frequency Switching Circuits

### DESCRIPTION

The DG126, DG129 and DG140 are dual double-pole single-throw analog switches for use in instrumentation, process control, and audio communication systems. This series is ideally suited for applications requiring a constant ON resistance over the entire analog range.

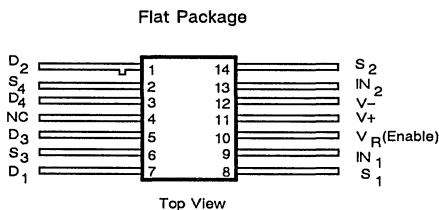
ON resistance for the DG126 is < 80  $\Omega$ , the DG129 < 30  $\Omega$  and the DG140 < 10  $\Omega$ , and ON leakage for all three is < 2 nA. With all switches OFF, total power consumption is < 750  $\mu$ W. These switches have Make-Before-Break action and due to the processing are relatively Radiation tolerant. An enable pin ( $V_R$ ) simplifies interfacing with microprocessor, or other logic. Package options are the 14-pin side braze and flat pack.

Each device contains four junction-type field-effect transistors (JFETS) to achieve constant on resistance. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With logic "0" at the driver input the switches will be OFF. With a logic "1" at the input the switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak.

Packaging for this series includes 14-pin side braze and flatpack options. Performance grades include both military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature ranges. The flatpack option is only available in the military grade.

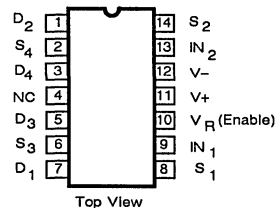
**5**

### PIN CONFIGURATION



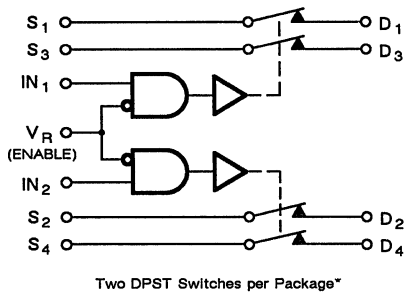
Order Numbers:  
DG126AL/883, DG129AL/883,  
DG140AL/883

Dual-In-Line Package



Order Numbers:  
DG126AP, DG126BP  
DG129AP, DG129BP  
DG140AP, DG140BP

## FUNCTIONAL BLOCK DIAGRAM



Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq 0.8$  V  
 Logic "1"  $\geq 2.5$  V

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V+ to VD	36 V
VD or VS to V-	36 V
VD to VS	$\pm 22$ V
V+ to VR	25 V
VR to V-	25 V
VIN to V-	30 V
V+ to VIN	25 V
VIN to VR	$\pm 6$ V

Current (Any Terminal)	30 mA
Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C

### Power Dissipation\*

Flat Package**	750 mW
14-pin DIP***	825 mW

\* All leads welded or soldered to PC board.

\*\* Derate 10 mW/°C above 75°C.

\*\*\* Derate 11 mW/°C above 75°C.

## ELECTRICAL CHARACTERISTICS<sup>a</sup>

DG126

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 12 V V- = -18 V VR = 0 V	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range	VANALOG		1,2,3		-10	10	-8	8	V
Drain-Source ON Resistance	rDS(ON)	IS = -10 mA VIN = 2.5 V	VD = 10 V	1,3 2	30	80 150		150	Ω
			VD = 8 V	1,3 2	25			100 150	
Source OFF Leakage Current	IS(OFF)	VIN = 0.8 V	VS = 10 V VD = -10 V	1 2	0.01	1 100			nA
			VS = 8 V VD = -8 V	1 2	0.05			5 100	
Drain OFF Leakage Current	ID(OFF)	VIN = 0.8 V	VD = 10 V VS = -10 V	1 2	0.005	1 100			nA
			VD = 8 V VS = -8 V	1 2	0.025			5 100	



ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG126		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = -18\text{ V}$ $V_R = 0\text{ V}$		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH (Cont'd)</b>										
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_{IN} = 2.5\text{ V}$	$V_D = V_S = -10\text{ V}$	1 2	-0.02	-2 -100				nA
			$V_D = V_S = -8\text{ V}$	1 2	-0.05		-5 -100			
<b>INPUT</b>										
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 2.5\text{ V}$		1,2 3	20		60 120		100 150	μA
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0.8\text{ V}$		1,3 2	0.004		0.1 2		4 4	
<b>DYNAMIC</b>										
Turn-ON Time <sup>e</sup>	$t_{ON}$	See Switching Time Test Circuit		1	0.4		0.6		1	μs
Turn-OFF Time <sup>e</sup>	$t_{OFF}$			1	1.3		1.6		2	
Source-OFF Capacitance	$C_{S(OFF)}$	$f = 1\text{ MHz}$	$V_S = 0, I_D = 0$	1	2.4					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		$V_D = 0, I_S = 0$	1	2.4					
Channel ON Capacitance	$C_{D+S(ON)}$		$V_D = V_S = 0$	1	2.8					
Off Isolation		$R_L = 75\Omega, f = 1\text{ MHz}$		1	>60					dB
<b>SUPPLY</b>										
Positive Supply Current	$I_+$	One Channel ON $V_{IN} = 2.5\text{ V}$		1	2.1		3		3.3	mA
Negative Supply Current	$I_-$			1	-1.2	-1.8		-2.0		
Reference Supply Current	$I_R$			1	-1	-1.4		-1.5		
Positive Supply Current	$I_+$	All Channels OFF Both $V_{IN} = 0\text{ V}$		1	0.1		25		25	μA
Negative Supply Current	$I_-$			1	-0.5	-25		-25		
Reference Supply Current	$I_R$			1	-0.5	-25		-25		

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ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG129
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = -18\text{ V}$ $V_R = 0\text{ V}$		LIMITS						UNIT
				1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analog Signal Range	$V_{\text{ANALOG}}$			1,2,3		-10	10	-8	8	V
Drain-Source ON Resistance	$r_{\text{DS(ON)}}$	$I_S = -10\text{ mA}$ $V_{\text{IN}} = 2.5\text{ V}$	$V_D = 10\text{ V}$	1,3 2	20		30 60			$\Omega$
			$V_D = 8\text{ V}$	1,3 2	30			50 75		
Source OFF Leakage Current	$I_{\text{S(OFF)}}$	$V_{\text{IN}} = 0.8\text{ V}$	$V_S = 10\text{ V}$ $V_D = -10\text{ V}$	1 2	0.03		1 100			nA
			$V_S = 8\text{ V}$ $V_D = -8\text{ V}$	1 2				5 100		
Drain OFF Leakage Current	$I_{\text{D(OFF)}}$	$V_{\text{IN}} = 0.8\text{ V}$	$V_D = 10\text{ V}$ $V_S = -10\text{ V}$	1 2	0.02		1 100			nA
			$V_D = 8\text{ V}$ $V_S = -8\text{ V}$	1 2	0.1			5 100		
Channel ON Leakage Current	$I_{\text{D(ON)}} + I_{\text{S(ON)}}$	$V_{\text{IN}} = 2.5\text{ V}$	$V_D = V_S = -10\text{ V}$	1 2	-0.03	-2 -100				nA
			$V_D = V_S = -8\text{ V}$	1 2	-0.08			-5 -100		
<b>INPUT</b>										
Input Current with Input Voltage HIGH	$I_{\text{INH}}$	$V_{\text{IN}} = 2.5\text{ V}$		1,2 3	15		60 120		100 150	$\mu\text{A}$
Input Current with Input Voltage LOW	$I_{\text{INL}}$	$V_{\text{IN}} = 0.8\text{ V}$		1,3 2	0.005		0.1 2		4 4	$\mu\text{A}$
<b>DYNAMIC</b>										
Turn-ON Time <sup>e</sup>	$t_{\text{ON}}$	See Switching Time Test Circuit		1	0.5		0.6		1	$\mu\text{s}$
Turn-OFF Time <sup>e</sup>	$t_{\text{OFF}}$			1	1.1		1.6		2	
Source-OFF Capacitance	$C_{\text{S(OFF)}}$	$f = 1\text{ MHz}$	$V_S = 0, I_D = 0$	1	2.4					pF
Drain-OFF Capacitance	$C_{\text{D(OFF)}}$		$V_D = 0, I_S = 0$	1	2.4					
Channel ON Capacitance	$C_{\text{D+S(ON)}}$		$V_D = V_S = 0$	1	2.8					
Off Isolation		$R_L = 75\Omega, f = 1\text{ MHz}$		1	>60					dB

ELECTRICAL CHARACTERISTICS <sup>a</sup>							DG129		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = -18\text{ V}$ $V_R = 0\text{ V}$	LIMITS						
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>SUPPLY</b>									
Positive Supply Current	$I_+$	One Channel ON $V_{IN} = 2.5\text{ V}$	1	2.5		3		3.3	mA
Negative Supply Current	$I_-$		1	-1.6	-1.8		-2.0		
Reference Supply Current	$I_R$		1	-1.1	-1.4		-1.5		
Positive Supply Current	$I_+$	All Channels OFF Both $V_{IN} = 0\text{ V}$	1	0.1		25		25	μA
Negative Supply Current	$I_-$		1	-0.5	-25		-25		
Reference Supply Current	$I_R$		1	-0.5	-25		-25		

ELECTRICAL CHARACTERISTICS <sup>a</sup>							DG140		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = -18\text{ V}$ $V_R = 0\text{ V}$	LIMITS						
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>SWITCH</b>									
Analog Signal Range	$V_{ANALOG}$		1,2,3		-10	10	-8	8	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -10\text{ mA}$ $V_{IN} = 2.5\text{ V}$	$V_D = 10\text{ V}$	1,3 2	6.3		10 20		Ω
			$V_D = 8\text{ V}$	1,3 2	9.5			15 25	
Source OFF Leakage Current	$I_{S(OFF)}$	$V_{IN} = 0.8\text{ V}$	$V_S = 10\text{ V}$ $V_D = -10\text{ V}$	1 2	0.04		10 1000		nA
			$V_S = 8\text{ V}$ $V_D = -8\text{ V}$	1 2	0.06			15 300	
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_{IN} = 0.8\text{ V}$	$V_D = 10\text{ V}$ $V_S = -10\text{ V}$	1 2			10 1000		
			$V_D = 8\text{ V}$ $V_S = -8\text{ V}$	1 2				15 300	
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_{IN} = 2.5\text{ V}$	$V_D = V_S = -10\text{ V}$	1 2	-0.4	-2 -100			
			$V_D = V_S = -8\text{ V}$	1 2	-1		-5 -100		

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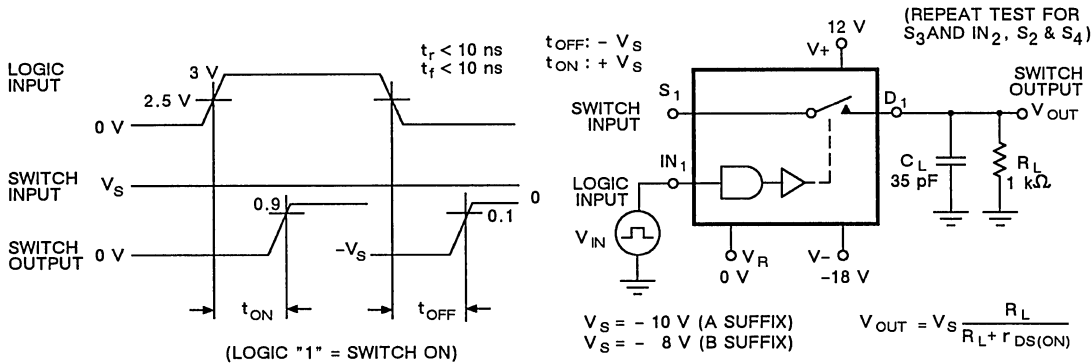
ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG140
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = -18\text{ V}$ $V_R = 0\text{ V}$	LIMITS						UNIT	
			1=25°C		2=125, 85°C		3=-55, -25°C			
					A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUT</b>										
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 2.5\text{ V}$	1, 2 3	13		60 120		100 150		$\mu\text{A}$
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0.8\text{ V}$	1, 3 2	0.004		0.1 2		4 4		
<b>DYNAMIC</b>										
Turn-ON Time <sup>e</sup>	$t_{ON}$	See Switching Time Test Circuit	1	0.6		1		1.5		$\mu\text{s}$
Turn-OFF Time <sup>e</sup>	$t_{OFF}$		1	1.15		2.5		2.5		
Source-OFF Capacitance	$C_{S(OFF)}$	$f = 1\text{ MHz}$	$V_S = 0, I_D = 0$		1	3				pF
Drain-OFF Capacitance	$C_{D(OFF)}$		$V_D = 0, I_S = 0$		1	3				
Channel ON Capacitance	$C_{D+S(ON)}$		$V_D = V_S = 0$		1	2.8				
Off Isolation		$R_L = 75\ \Omega, f = 1\text{ MHz}$	1	>50						dB
<b>SUPPLY</b>										
Positive Supply Current	$I_+$	One Channel ON $V_{IN} = 2.5\text{ V}$	1	2.4		3		3.3		mA
Negative Supply Current	$I_-$		1	-1.5	-1.8		-2.0			
Reference Supply Current	$I_R$		1	-1	-1.4		-1.5			
Positive Supply Current	$I_+$	All Channels OFF Both $V_{IN} = 0\text{ V}$	1	0.1		25		25		$\mu\text{A}$
Negative Supply Current	$I_-$		1	-0.5	-25		-25			
Reference Supply Current	$I_R$		1	-0.5	-25		-25			

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e.  $V_{IN}$  must be a step function with a minimum rise and fall time of 1 V/ $\mu\text{s}$ .

**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



**APPLICATION HINTS**

$V_+$ Positive Supply Voltage (V)	$V_-$ Negative Supply Voltage (V)	$V_R$ Reference Voltage (V)	$V_{IN}$ Logic Input Voltage $V_{INH}$ Min/ $V_{INL}$ Max (V)	$V_S$ or $V_D$ Analog Voltage Range (V)
12	-18	0	2.5/0.8	-10 to 10
15	-15	0	2.5/0.8	-7 to 13
7	-12	0	2.5/0.8	-5 to 5
5	-15	0	2.5/0.8	-7 to 3
5	-10	0	2.5/0.8	-2 to 3

# DG133/134/141

## Dual SPST JFET

### Analog Switches

#### FEATURES

- Low Standby Power (< 1  $\mu$ W)
- Bipolar Drivers
- Constant  $r_{DS(ON)}$  Over Signal Range
- High Off Isolation (> 60 dB @ 1 MHz)

#### BENEFITS

- Minimizes Standby Power Requirement
- Better Radiation Tolerance
- Less Signal Distortion
- Higher Frequency Switching

#### APPLICATIONS

- Portable and Battery Powered Systems
- Switching in Satellite Applications
- Low Distortion Circuits
- High Frequency Switching Circuits

#### DESCRIPTION

The DG133, DG134, and DG141 are dual precision single-pole, single-throw analog switches for use in process control, communication, and instrumentation applications. This series is ideally suited for applications requiring a constant ON resistance over the entire analog range.

ON resistance of the DG134 is < 80  $\Omega$ , the DG133 is < 30  $\Omega$ , and the DG141 is < 10  $\Omega$ , and ON shunt leakage for all three is < 2 nA. With both drivers in the "switch OFF" state, total power consumption is 750  $\mu$ W. Because JFET and bipolar processing is used, all three devices are relatively radiation tolerant.

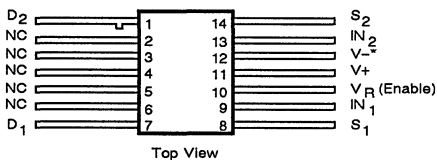
The DG133, DG134, and DG141 each contain two junction-type field-effect transistors (JFETs) de-

signed to function as two single-pole, single-throw electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2.5 V) to control the ON-OFF state of each switch. With a positive logic "0" at the driver input the switches will be OFF. With a positive logic "1" at the input the switches will be ON. In the ON state each switch will conduct current in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak.

Packaging for this series include a 14-pin side braze and flatpack options. Performance grades include both a military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature range. The flatpack option is only available in the military grade.

#### PIN CONFIGURATION

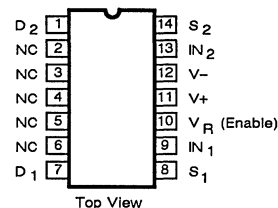
Flat Package



Order Numbers:

DG133AL/883, DG134AL/883  
DG141AL/883

Dual-In-Line Package

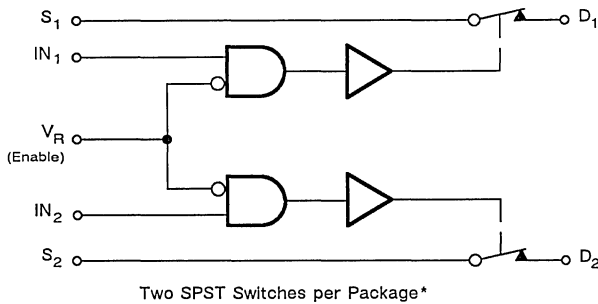


Order Numbers:

Side Braze: DG133AP, DG133BP  
DG134AP, DG134BP  
DG141AP, DG141BP

\* Common to Substate and Base of Package

## FUNCTIONAL BLOCK DIAGRAM



Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.5$  V

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V
V+ to VD	36 V
VD or VS to V-	36 V
VD to VS	$\pm 22$ V
V+ to VR	25 V
VR to V-	25 V
VIN to V-	30 V
V+ to VIN	25 V
VIN to VR	$\pm 6$ V

Current (Any Terminal)	30 mA
Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
Power Dissipation*	
Flat Package**	750 mW
14-Pin DIP***	825 mW

\* All leads welded or soldered to PC board.

\*\* Derate 10 mW/°C above 75°C.

\*\*\* Derate 11 mW/°C above 75°C.

**5**

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

DG133

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V+ = 12 V V- = -18 V VR = 0	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	VANALOG		1,2,3		-10	10	-8	8	V
Drain-Source ON Resistance	rDS(ON)	IS = -10 mA VIN = 2.5 V	VD = 10 V	1,3 2	20		30 60		Ω
			VD = 8 V	1,3 2	30			50 75	
Source OFF Leakage Current	IS(OFF)	VIN = 0.8 V	VS = 10 V VD = -10 V	1 2	0.03		1 100		nA
			VS = 8 V VD = -8 V	1 2				5 100	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG133	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = -18\text{ V}$ $V_R = 0\text{ V}$			LIMITS						UNIT
					1=25°C		A SUFFIX		B SUFFIX		
					TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH (Cont'd)</b>											
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_{IN} = 0.8\text{ V}$	$V_D = 10\text{ V}$ $V_S = -10\text{ V}$	1	0.02		1			nA	
			$V_D = 8\text{ V}$ $V_S = -8\text{ V}$	2	0.1			5	100		
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_{IN} = 2.5\text{ V}$	$V_D = V_S = -10\text{ V}$	1	-0.03	-2				nA	
			$V_D = V_S = -8\text{ V}$	2	-0.08			-5	-100		
<b>INPUT</b>											
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 2.5\text{ V}$		1,2			60		100	μA	
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0.8\text{ V}$		3			120		150		
<b>DYNAMIC</b>											
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit <sup>e</sup>			1		0.6		1	μs	
Turn-OFF Time	$t_{OFF}$				1		1.6		2		
Drain-OFF Capacitance	$C_{D(OFF)}$	$f = 1\text{ MHz}$	$V_D = 0\text{ V}$ $I_S = 0$	1	2.4					pF	
Source-OFF Capacitance	$C_{S(OFF)}$		$V_S = 0\text{ V}$ $I_D = 0$	1	2.4						
Channel-ON Capacitance	$C_{D(ON)} + C_{S(ON)}$		$V_D = V_S = 0$	1	2.8						
OFF Isolation	OIRR	$R_L = 75\ \Omega, f = 1\text{ MHz}$			1	>60				dB	
<b>SUPPLY</b>											
Positive Supply Current	$I_+$	One Channel ON $V_{IN} = 2.5\text{ V}$			1	2.1		3		3.3	mA
Negative Supply Current	$I_-$				1	-1.2	-1.8		-2		
Reference Supply Current	$I_R$				1	-1	-1.4		-1.5		



ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG133
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V		LIMITS						UNIT
				1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY (Cont'd)</b>										
Positive Supply Current	I <sub>+</sub>	All Channels OFF Both V <sub>IN</sub> = 0 V		1	0.1		25		25	μA
Negative Supply Current	I <sub>-</sub>			1	-0.5	-25		-25		
Reference Supply Current	I <sub>R</sub>			1	-0.5	-25		-25		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG134
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V		LIMITS						UNIT
				1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analogue Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-10	10	-8	8	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA V <sub>IN</sub> = 2.5 V	V <sub>D</sub> = 10 V	1,3 2	30		80 150			Ω
			V <sub>D</sub> = 8 V	1,3 2	35			100 150		
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 0.8 V	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V	1 2	0.01		1 100			nA
			V <sub>S</sub> = 8 V V <sub>D</sub> = -8 V	1 2	0.05			5 100		
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN</sub> = 0.8 V	V <sub>D</sub> = 10 V V <sub>S</sub> = -10 V	1 2	0.005		1 100			nA
			V <sub>D</sub> = 8 V V <sub>S</sub> = -8 V	1 2	0.025			5 100		
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>IN</sub> = 2.5 V	V <sub>D</sub> = V <sub>S</sub> = -10 V	1 2	-0.02	-2 -100				nA
			V <sub>D</sub> = V <sub>S</sub> = -8 V	1 2	-0.05			-5 -100		

**5**

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG134
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = -18\text{ V}$ $V_R = 0\text{ V}$		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				2=125, 85°C		-55 to 125°C		-25 to 85°C		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>										
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 2.5\text{ V}$	1,2 3			60 120		100 150		$\mu\text{A}$
Input Current with input Voltage LOW	$I_{INL}$	$V_{IN} = 0.8\text{ V}$	1,3 2			0.1 2		4 4		
<b>DYNAMIC</b>										
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit <sup>e</sup>		1			0.6		1	$\mu\text{s}$
Turn-OFF Time	$t_{OFF}$			1			1.6		2	
Drain-OFF Capacitance	$C_{D(OFF)}$	$f = 1\text{ MHz}$	$V_D = 0\text{ V}$ $I_S = 0$	1	2.4					$\text{pF}$
Source-OFF Capacitance	$C_{S(OFF)}$		$V_S = 0\text{ V}$ $I_D = 0$	1	2.4					
Channel-ON Capacitance	$C_{D(ON)} + C_{S(ON)}$		$V_D = V_S = 0$	1	2.8					
OFF Isolation	OIRR	$R_L = 75\ \Omega, f = 1\text{ MHz}$		1	>60					$\text{dB}$
<b>SUPPLY</b>										
Positive Supply Current	$I_+$	One Channel ON $V_{IN} = 2.5\text{ V}$		1	2.1		3		3.3	$\text{mA}$
Negative Supply Current	$I_-$			1	-1.2	-1.8		-2		
Reference Supply Current	$I_R$			1	-1	-1.4		-1.5		
Positive Supply Current	$I_+$	All Channels OFF Both $V_{IN} = 0\text{ V}$		1	0.1		25		25	$\mu\text{A}$
Negative Supply Current	$I_-$			1	-0.5	-25		-25		
Reference Supply Current	$I_R$			1	-0.5	-25		-25		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG141	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V			LIMITS						UNIT
					1=25°C		A SUFFIX		B SUFFIX		
					TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-10	10	-8	8	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA V <sub>IN</sub> = 2.5 V	V <sub>D</sub> = 10 V	1,3 2	6.3		10 20			Ω	
			V <sub>D</sub> = 8 V	1,3 2	9.5			15 25			
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 0.8 V	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V	1 2	0.04		10 1000			nA	
			V <sub>S</sub> = 8 V V <sub>D</sub> = -8 V	1 2	0.06			15 300			
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN</sub> = 0.8 V	V <sub>D</sub> = 10 V V <sub>S</sub> = -10 V	1 2			10 1000				
			V <sub>D</sub> = 8 V V <sub>S</sub> = -8 V	1 2				15 300			
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>IN</sub> = 2.5 V	V <sub>D</sub> = V <sub>S</sub> = -10 V	1 2	-0.4	-2 -100					
			V <sub>D</sub> = V <sub>S</sub> = -8 V	1 2	-1.0			-5 -100			
<b>INPUT</b>											
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 2.5 V		1,2 3			60 120		100 150	μA	
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0.8 V		1,3 2			0.1 2		4 4		
<b>DYNAMIC</b>											
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit <sup>e</sup>			1			1		1.5	μs
Turn-OFF Time	t <sub>OFF</sub>				1	1.15		2.5		2.5	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	f = 1 MHz	V <sub>D</sub> = 0 V I <sub>S</sub> = 0	1	3					pF	
Source-OFF Capacitance	C <sub>S(OFF)</sub>		V <sub>S</sub> = 0 V I <sub>D</sub> = 0	1	3						
Channel-ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0	1	2.8						
OFF Isolation	OIRR	R <sub>L</sub> = 75 Ω, f = 1 MHz			1	>50				dB	

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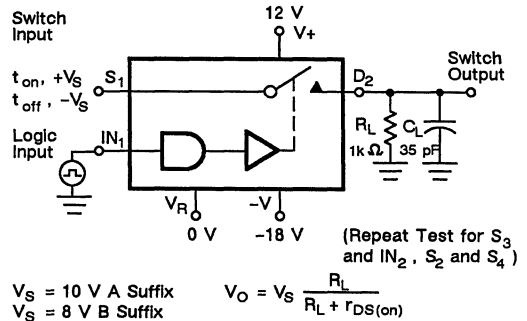
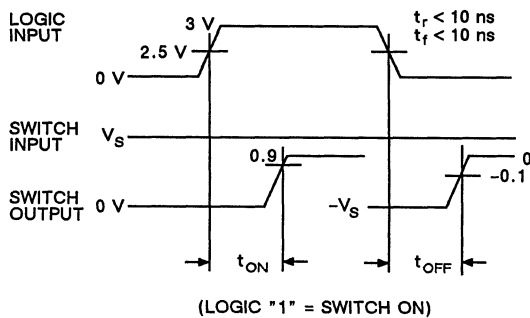
ELECTRICAL CHARACTERISTICS <sup>a</sup>							DG141		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V	LIMITS						
			1=25°C		A SUFFIX 2=125,85°C -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	One Channel ON V <sub>IN</sub> = 2.5 V	1	2.1		3		3.3	mA
Negative Supply Current	I <sub>-</sub>		1	-1.2	-1.8		-2		
Reference Supply Current	I <sub>R</sub>		1	-1	-1.4		-1.5		
Positive Supply Current	I <sub>+</sub>	All Channels OFF Both V <sub>IN</sub> = 0 V	1	0.1		25		25	μA
Negative Supply Current	I <sub>-</sub>		1	-0.5	-25		-25		
Reference Supply Current	I <sub>R</sub>		1	-0.5	-25		-25		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> must be a step function with a minimum rise and fall time of 1 V/μs.

### SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V<sub>S</sub> = constant with logic input waveform as shown. Note that V<sub>S</sub> may be + or - as per switching time test circuit. V<sub>O</sub> is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



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**APPLICATION HINTS**


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V <sub>+</sub> Positive Supply Voltage (V)	V <sub>-</sub> Negative Supply Voltage (V)	V <sub>R</sub> Reference Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
12	-18	0	2.5/0.8	-10 to 10
15	-15	0	2.5/0.8	-5 to 13
10	-10	0	2.5/0.8	0 to 8

# DG139/142/145

## Dual DPDT JFET

### Analog Swiches

#### FEATURES

- ( $< 1 \mu\text{W}$ ) Standby Power
- Bipolar Drivers
- Constant  $r_{DS(ON)}$  Over Signal Range
- High Off Isolation ( $> 60 \text{ dB @ 1 MHz}$ )

#### BENEFITS

- Minimizes Standby Power Requirement
- Better Radiation Tolerance than CMOS
- Less Signal Distortion than CMOS
- Higher Frequency Switching

#### APPLICATIONS

- Portable and Battery Powered Systems
- Switching in Satellite Applications
- Low Distortion Circuits
- High Frequency Switching Circuits

#### DESCRIPTION

The DG139, DG142, and DG145 are precision dual double-pole double-throw analog switches designed for use in low distortion, high frequency circuits.

ON resistance of the DG139 is  $< 30 \Omega$ , the DG142  $< 80 \Omega$  and the DG145 is  $< 10 \Omega$  and ON shunt leakage for all three is  $< 2 \text{ nA}$ . With both drivers in the "switch OFF" state, total power consumption is  $< 750 \mu\text{W}$ . By using the JFET process, all three analog switches are relatively radiation tolerant.

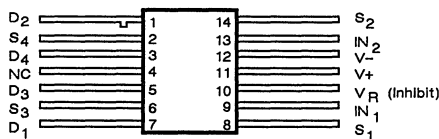
The DG139, DG142 and DG145 each contain four junction-type field-effect transistors (JFETs) designed to function as two double-pole double-throw electronic switches. Level-shifting drivers enable low-level inputs ( $2 \text{ V}$  to  $3 \text{ V}$ ) to control the ON-OFF state of the switches. The driver inputs are connected differentially, therefore with

input IN2 connected to a 2.5 voltage reference, a positive logic "0" at the input IN1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally grounded  $V_R$  terminal may be used as an "inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to  $V_R$ . In the ON state each switch conducts equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak.

Packaging for this series includes the 14-pin side braze and flatpack options. Performance grades include both a military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ) temperature range. The flatpack option is only available in the military grade.

#### PIN CONFIGURATION

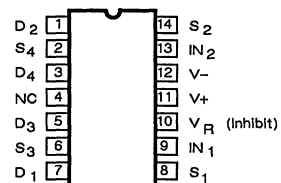
Flat Package



Top View

Order Numbers:  
DG139AL/883, DG142AL/883  
DG145AL/883

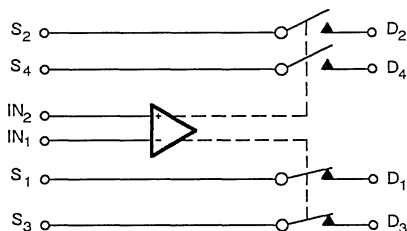
Dual-In-Line Package



Top View

Order Numbers:  
DG139AP, DG139BP  
DG142AP, DG142BP

**FUNCTIONAL BLOCK DIAGRAM**



Two DPDT Switches per Package\*

Truth Table

Logic	SW1 SW3	SW2 SW4
0	OFF	ON
1	ON	OFF

\*Switches Shown for Logic "1" Input at IN<sub>1</sub> and a 2.5 V reference at IN<sub>2</sub>

**ABSOLUTE MAXIMUM RATINGS**

V <sub>+</sub> to V <sub>-</sub> , V <sub>D</sub> or V <sub>S</sub> .....	36 V
V <sub>D</sub> or V <sub>S</sub> to V <sub>-</sub> .....	36 V
V <sub>D</sub> to V <sub>S</sub> .....	±22 V
V <sub>+</sub> to V <sub>R</sub> .....	25 V
V <sub>+</sub> to V <sub>IN1</sub> or V <sub>IN2</sub> .....	25 V
V <sub>R</sub> to V <sub>-</sub> .....	25 V
V <sub>IN1</sub> to V <sub>IN2</sub> .....	±6 V
V <sub>IN1</sub> or V <sub>IN2</sub> to V <sub>R</sub> .....	±6 V
V <sub>IN1</sub> or V <sub>IN2</sub> to V <sub>-</sub> .....	30 V

Current, (Any Terminal) .....	30 mA
Storage Temperature .....	-65 to 150°C
Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C
Power Dissipation*	
Flat Package** .....	750 mW
14-Pin DIP*** .....	825 mW

\* All leads welded or soldered to PC board.  
\*\* Derate 10 mW/°C above 75°C.  
\*\*\* Derate 11 mW/°C above 75°C.



ELECTRICAL CHARACTERISTICS <sup>a</sup>							DG139			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V <sub>IN2</sub> = 2.5 V	LIMITS						UNIT	
			TEMP	TYP <sup>d</sup>	A SUFFIX		B SUFFIX			
			1=25°C		-55 to 125°C		-25 to 85°C			
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-10	10	-8	8		V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA V <sub>IN1</sub> = 3 V (SW1, 3 ON)	V <sub>D</sub> = 10 V	1,3 2	20	30 60				Ω
		V <sub>IN1</sub> = 2 V (SW2, 4 ON)	V <sub>D</sub> = 8 V	1,3 2	35			50 75		
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW1, 3 OFF)	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V	1 2	0.15	1 100				nA
		V <sub>IN1</sub> = 3 V (SW2, 4 OFF)	V <sub>S</sub> = 8 V V <sub>D</sub> = -8 V	1 2	0.75			5 100		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG139	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:				LIMITS					
		$V_+ = 12\text{ V}$ $V_- = -18\text{ V}$ $V_R = 0$ $V_{IN2} = 2.5\text{ V}$				1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C	
						TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>
<b>SWITCH (Cont'd)</b>											
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_{IN1} = 2\text{ V}$ (SW1, 3 OFF) $V_{IN1} = 3\text{ V}$ (SW2, 4 OFF)	$V_D = 10\text{ V}$ $V_S = -10\text{ V}$	1	0.03		1				nA
			$V_D = 8\text{ V}$ $V_S = -8\text{ V}$	2	0.15			5	100		
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_{IN1} = 3\text{ V}$ (SW1, 3 ON) $V_{IN1} = 2\text{ V}$ (SW2, 4 ON)	$V_D = V_S = -10\text{ V}$	1	-0.05	-2					
			$V_D = V_S = -8\text{ V}$	2	-0.12			-5	-100		
<b>INPUT</b>											
Input 1 Current Input 1 Voltage LOW	$I_{IN1L}$	$V_{IN1} = 2\text{ V}$		1,3 2	0.001		0.1 2		4 4	μA	
Input 2 Current Input 2 Voltage LOW	$I_{IN2L}$	$V_{IN2} = 2\text{ V}, V_{IN1} = 2.5\text{ V}$		1,3 2	0.001		0.1 2		4 4		
Input 1 Current Input 1 Voltage HIGH	$I_{IN1H}$	$V_{IN1} = 3\text{ V}$		1,2 3	20		60 120		100 150		
Input 2 Current Input 2 Voltage HIGH	$I_{IN2H}$	$V_{IN2} = 3\text{ V}, V_{IN1} = 2.5\text{ V}$		1,2 3	20		60 120		100 150		
<b>DYNAMIC</b>											
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit <sup>e</sup>		1			0.8		1	μs	
Turn-OFF Time	$t_{OFF}$			1			1.6		2		
Drain-OFF Capacitance	$C_{D(OFF)}$	f = 1 MHz	$V_D = 0\text{ V}$ $I_S = 0$	1	2.4					pF	
Source-OFF Capacitance	$C_{S(OFF)}$		$V_S = 0\text{ V}$ $I_D = 0$	1	2.4						
Channel-ON Capacitance	$C_{D(ON)} + C_{S(ON)}$		$V_D = V_S = 0\text{ V}$	1	2.8						
OFF Isolation	OIRR	$R_L = 75\ \Omega, f = 1\text{ MHz}$		1	>60					dB	
<b>SUPPLY</b>											
Positive Supply Current	$I_+$	One Channel ON $V_{IN1} = 2\text{ V}$ or $V_{IN1} = 3\text{ V}$		1	2.6		4.2		4.5	mA	
Negative Supply Current	$I_-$			1	-1.3	-2		-2.2			
Reference Supply Current	$I_R$			1	-1.4	-2.2		-2.4			



ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG139	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V <sub>IN2</sub> = 2.5 V	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY (Cont'd)</b>									
Positive Supply Current	I <sub>+</sub>	All Channels OFF V <sub>IN1</sub> = V <sub>IN2</sub> = 0.8 V	1	0.75		25		25	μA
Negative Supply Current	I <sub>-</sub>		1	-1	-25		-25		
Reference Supply Current	I <sub>R</sub>		1	-0.2	-25		-25		

ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG142	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V <sub>IN2</sub> = 2.5 V	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-10	10	-8	8	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA V <sub>IN1</sub> = 3 V (SW1, 3 ON) V <sub>IN1</sub> = 2 V (SW2, 4 ON)	V <sub>D</sub> = 10 V	1,3 2	30		80 150		Ω
			V <sub>D</sub> = 8 V	1,3 2	35			100 150	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW1, 3 OFF) V <sub>IN1</sub> = 3 V (SW2, 4 OFF)	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V	1 2	0.01		1 100		nA
			V <sub>S</sub> = 8 V V <sub>D</sub> = -8 V	1 2	0.05			5 100	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW1, 3 OFF) V <sub>IN1</sub> = 3 V (SW2, 4 OFF)	V <sub>D</sub> = 10 V V <sub>S</sub> = -10 V	1 2	0.005		1 100		
			V <sub>D</sub> = 8 V V <sub>S</sub> = -8 V	1 2	0.025			5 100	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>IN1</sub> = 3 V (SW1, 3 ON) V <sub>IN1</sub> = 2 V (SW2, 4 ON)	V <sub>D</sub> = V <sub>S</sub> = -10 V	1 2	-0.02	-2 100			
			V <sub>D</sub> = V <sub>S</sub> = -8 V	1 2	-0.05			-5 -100	

**5**

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG142
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V <sub>IN2</sub> = 2.5 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		B SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUT</b>										
Input 1 Current Input 1 Voltage LOW	I <sub>IN1L</sub>	V <sub>IN1</sub> = 2 V	1,3 2	0.0005		0.1 2		4 4	μA	
Input 2 Current Input 2 Voltage LOW	I <sub>IN2L</sub>	V <sub>IN2</sub> = 2 V, V <sub>IN1</sub> = 2.5 V	1,3 2	0.001		0.1 2		4 4		
Input 1 Current Input 1 Voltage HIGH	I <sub>IN1H</sub>	V <sub>IN1</sub> = 3 V	1,2 3	25		60 120		100 150		
Input 2 Current Input 2 Voltage HIGH	I <sub>IN2H</sub>	V <sub>IN2</sub> = 3 V, V <sub>IN1</sub> = 2.5 V	1,2 3	25		60 120		100 150		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit <sup>e</sup>		1	0.5		0.8		1	μs
Turn-OFF Time	t <sub>OFF</sub>			1	1.1		1.6		2.0	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	f = 1 MHz	V <sub>D</sub> = 0 V I <sub>S</sub> = 0	1	2.4				pF	
Source-OFF Capacitance	C <sub>S(OFF)</sub>		V <sub>S</sub> = 0 V I <sub>D</sub> = 0	1	2.4					
Channel-ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	2.8					
OFF Isolation	OIRR	R <sub>L</sub> = 75 Ω, f = 1 MHz		1	>60					dB
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	One Channel ON V <sub>IN1</sub> = 2 V, V <sub>IN1</sub> = 3 V		1	2.6		4.2		4.5	mA
Negative Supply Current	I <sub>-</sub>			1	-1.3	-2		-2.2		
Reference Supply Current	I <sub>R</sub>			1	-1.4	-2.2		-2.4		
Positive Supply Current	I <sub>+</sub>	All Channels OFF V <sub>IN1</sub> = V <sub>IN2</sub> = 0.8 V		1	0.75		25		25	μA
Negative Supply Current	I <sub>-</sub>			1	-1	-25		-25		
Reference Supply Current	I <sub>R</sub>			1	-0.2	-25		-25		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG145	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V <sub>IN2</sub> = 2.5 V		LIMITS						UNIT	
				1=25°C		A SUFFIX		B SUFFIX			
				TEMP	TYP <sup>d</sup>	-55 to 125°C		-25 to 85°C			
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3			-10	10	-8	8	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA V <sub>IN1</sub> = 3 V (SW1, 3 ON)	V <sub>D</sub> = 10 V	1,3	7		10				Ω
			V <sub>D</sub> = 8 V	1,3					15	25	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW1, 3 OFF) V <sub>IN1</sub> = 3 V (SW2, 4 OFF)	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V	1	0.1		10				nA
			V <sub>S</sub> = 8 V V <sub>D</sub> = -8 V	1					15	300	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW1, 3 OFF) V <sub>IN1</sub> = 3 V (SW2, 4 OFF)	V <sub>D</sub> = 10 V V <sub>S</sub> = -10 V	1	0.1		10				nA
			V <sub>D</sub> = 8 V V <sub>S</sub> = -8 V	1					15	300	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>IN1</sub> = 3 V (SW1, 3 ON) V <sub>IN1</sub> = 2 V (SW2, 4 ON)	V <sub>D</sub> = V <sub>S</sub> = -10 V	1	-0.04	-2	100				nA
			V <sub>D</sub> = V <sub>S</sub> = -8 V	1					-5	-100	
<b>INPUT</b>											
Input 1 Current Input 1 Voltage LOW	I <sub>IN1L</sub>	V <sub>IN1</sub> = 2 V		1,3	0.001		0.1			4	μA
Input 2 Current Input 2 Voltage LOW	I <sub>IN2L</sub>	V <sub>IN2</sub> = 2 V, V <sub>IN1</sub> = 2.5 V		1,3	0.001		0.1			4	
Input 1 Current Input 1 Voltage HIGH	I <sub>IN1H</sub>	V <sub>IN1</sub> = 3 V		1,2	20		60			100	
Input 2 Current Input 2 Voltage HIGH	I <sub>IN2H</sub>	V <sub>IN2</sub> = 3 V, V <sub>IN1</sub> = 2.5 V		1,2	20		60			100	
<b>DYNAMIC</b>											
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit <sup>e</sup>		1	0.5		1			1.5	μs
Turn-OFF Time	t <sub>OFF</sub>			1	1.2		2.5		2.5		
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	f = 1 MHz	V <sub>D</sub> = 0 V I <sub>S</sub> = 0	1	3						pF
Source-OFF Capacitance	C <sub>S(OFF)</sub>		V <sub>S</sub> = 0 V I <sub>D</sub> = 0	1	3						
Channel-ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0	1	2.8						

**5**

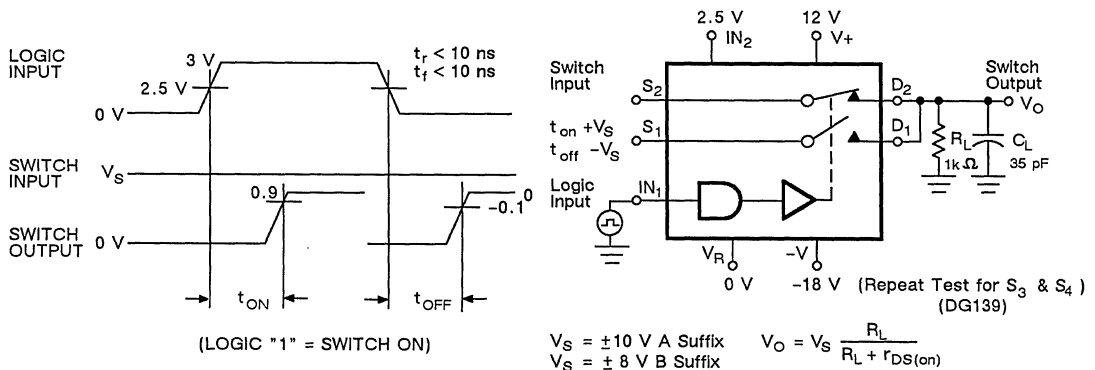
ELECTRICAL CHARACTERISTICS <sup>a</sup>							DG145		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V <sub>IN2</sub> = 2.5 V	LIMITS						
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>DYNAMIC (Cont'd)</b>									
OFF Isolation	OIRR	R <sub>L</sub> = 75 Ω, f = 1 MHz	1	>50					dB
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	One Channel ON V <sub>IN1</sub> = 2 V, V <sub>IN1</sub> = 3 V	1	2.6		4.2		4.5	mA
Negative Supply Current	I <sub>-</sub>		1	-1.2	-2		-2.2		
Reference Supply Current	I <sub>R</sub>		1	-1.4	-2.2		-2.4		
Positive Supply Current	I <sub>+</sub>	All Channels OFF V <sub>IN1</sub> = V <sub>IN2</sub> = 0.8 V	1	0.75		25		25	μA
Negative Supply Current	I <sub>-</sub>		1	-1	-25		-25		
Reference Supply Current	I <sub>R</sub>		1	-0.2	-25		-25		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> must be a step function with a minimum rise and fall time of 1 V/μs.

**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for V<sub>S</sub> = constant with logic input waveform as shown. Note that V<sub>S</sub> may be + or - as per switching time test circuit. V<sub>O</sub> is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



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## APPLICATION HINTS

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V <sub>+</sub> Positive Supply Voltage (V)	V <sub>-</sub> Negative Supply Voltage (V)	V <sub>R</sub> Reference Voltage (V)	V <sub>IN1</sub> Input 1 Voltage V <sub>INH</sub> / V <sub>INL</sub> (V)	V <sub>IN2</sub> Input 2 Voltage (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
12	-18	0	3/2	2.5	-10 to 10
15	-15	0	3/2	2.5	-5 to 13
5	-15	0	3/2	2.5	-5 to 3

# DG143/144/146

## SPDT JFET

### Analog Switches

#### FEATURES

- Low Standby Power ( $< 1 \mu W$ )
- Bipolar Drivers
- Constant  $r_{DS(ON)}$  Over Signal Range
- High Off Isolation ( $> 60 \text{ dB @ } 1 \text{ MHz}$ )

#### BENEFITS

- Minimizes Standby Power Requirement
- Better Radiation Tolerance
- Less Signal Distortion
- Higher Frequency Switching

#### APPLICATIONS

- Portable and Battery Powered Systems
- Switching in Satellite Applications
- Low Distortion Circuits
- High Frequency Switching Circuits

#### DESCRIPTION

The DG143, DG144, and DG146 are precision single-pole double-throw analog switches designed for use in low distortion, high frequency circuits.

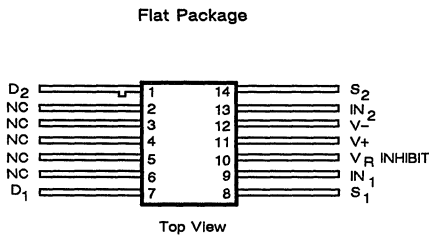
ON resistance of the DG143 is  $< 80 \Omega$ , the DG144  $< 30 \Omega$  and the DG146 is  $< 10 \Omega$  and ON shunt leakage for all three is  $< 2 \text{ nA}$ . With the driver in the "switch OFF" state, total power consumption is  $< 750 \mu W$ . By using the JFET process, all three analog switches are relatively radiation tolerant.

The DG143, DG144 and DG146 each contain two junction-type field-effect transistors (JFETs) designed to function as single-pole double-throw electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially, therefore with input  $IN_2$

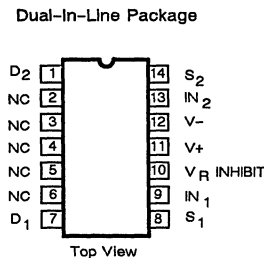
connected to a 2.5 voltage reference, a positive logic "0" at the input  $IN_1$  will turn switch 1 OFF and switch 2 ON. A positive logic "1" at  $IN_1$  will turn switch 1 ON and switch 2 OFF. The normally grounded  $V_R$  terminal may be used as an "inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to  $V_R$ . In the ON state each switch conducts equally well in either direction, and in the OFF state each switch will block voltages up to 20 V peak-to-peak.

Packaging for this series include a 14-pin side braze and flatpack options. Performance grades include both a military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ) temperature range. The flatpack option is only available in the military grade.

#### PIN CONFIGURATION

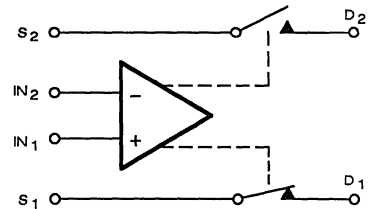


Order Numbers:  
DG143AL/883, DG144AL/883  
or DG146AL/883



Order Numbers:  
DG143AP, DG143BP  
DG144AP, DG144BP  
DG146AP, DG146BP

#### FUNCTIONAL BLOCK DIAGRAM



One SPDT Switch per Package\*

Truth Table

LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

\*Switches Shown for Logic "1" Input at  $IN_1$  and 2.5 V Reference at  $IN_2$

**ABSOLUTE MAXIMUM RATINGS**

V <sub>+</sub> to V <sub>-</sub> , V <sub>D</sub> or V <sub>S</sub> .....	36 V
V <sub>D</sub> or V <sub>S</sub> to V <sub>-</sub> .....	36 V
V <sub>D</sub> to V <sub>S</sub> .....	±22 V
V <sub>+</sub> to V <sub>R</sub> .....	25 V
V <sub>+</sub> to V <sub>IN1</sub> or V <sub>IN2</sub> .....	25 V
V <sub>R</sub> to V <sub>-</sub> .....	25 V
V <sub>IN1</sub> to V <sub>IN2</sub> .....	±6 V
V <sub>IN1</sub> or V <sub>IN2</sub> to V <sub>R</sub> .....	±6 V
V <sub>IN1</sub> or V <sub>IN2</sub> to V <sub>-</sub> .....	30 V

Current, (Any Terminal) .....	30 mA
Storage Temperature .....	-65 to 150°C
Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C

Power Dissipation*	
Flat Package** .....	750 mW
14-Pin DIP*** .....	825 mW

- \* All leads welded or soldered to PC board.
- \*\* Derate 10 mW/°C above 75°C.
- \*\*\* Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>							DG143			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V V <sub>IN2</sub> = 2.5 V		LIMITS						UNIT
				1=25°C		A SUFFIX 2=125,85°C 3=-55,-25°C		B SUFFIX -25 to 85°C		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-10	10	-8	8	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA V <sub>IN1</sub> = 3 V (SW1 ON) V <sub>IN1</sub> = 2 V (SW2 ON)	V <sub>D</sub> = 10 V	1,3 2	30		80 150			Ω
			V <sub>D</sub> = 8 V	1,3 2	35			100 150		
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW1 OFF) V <sub>IN1</sub> = 3 V (SW2 OFF)	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V	1 2	0.15		1 100			nA
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = 8 V V <sub>D</sub> = -8 V	1 2	0.75			5 100		
			V <sub>D</sub> = 10 V V <sub>S</sub> = -10 V	1 2	0.03		1 100			
			V <sub>D</sub> = 8 V V <sub>S</sub> = -8 V	1 2	0.15			5 100		
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>IN1</sub> = 3 V (SW1 ON) V <sub>IN1</sub> = 2 V (SW2 ON)	V <sub>D</sub> = V <sub>S</sub> = -10 V	1 2	-0.05	-2 -100				
			V <sub>D</sub> = V <sub>S</sub> = -8 V	1 2	-0.12			-5 -100		
<b>INPUT</b>										
Input 1 Current Input 1 Voltage LOW	I <sub>IN1L</sub>	V <sub>IN1</sub> = 2 V		1,3 2	0.001		0.1 2		4 4	μA
Input 2 Current Input 2 Voltage LOW	I <sub>IN2L</sub>	V <sub>IN2</sub> = 2 V, V <sub>IN1</sub> = 2.5 V		1,3 2	0.001		0.1 2		4 4	

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ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG143		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V V <sub>IN2</sub> = 2.5 V	LIMITS						UNIT	
			1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUT (Cont'd)</b>										
Input 1 Current Input 1 Voltage HIGH	I <sub>IN1H</sub>	V <sub>IN1</sub> = 3 V	1,2 3	25 35		60 120		100 150	μA	
Input 2 Current Input 2 Voltage HIGH	I <sub>IN2H</sub>	V <sub>IN2</sub> = 3 V, V <sub>IN1</sub> = 2.5 V	1,2 3	25 35		60 120		100 150		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit <sup>e</sup>	1	0.5		0.8		1	μs	
Turn-OFF Time	t <sub>OFF</sub>		1	1.1		1.6		2		
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	f = 1 MHz	V <sub>D</sub> = 0 V I <sub>S</sub> = 0	1	2.4				pF	
Source-OFF Capacitance	C <sub>S(OFF)</sub>			V <sub>S</sub> = 0 V I <sub>D</sub> = 0	1	2.4				
Channel-ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>				V <sub>D</sub> = V <sub>S</sub> = 0 V	1	2.8			
OFF Isolation		R <sub>L</sub> = 75 Ω, f = 1 MHz	1	> 60					dB	
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	One Channel ON V <sub>IN1</sub> = 2 V or V <sub>IN1</sub> = 3 V	1	2.6		4.2		4.5	mA	
Negative Supply Current	I <sub>-</sub>		1	-1.3	-2		-2.2			
Reference Supply Current	I <sub>R</sub>		1	-1.4	-2.2		-2.4			
Positive Supply Current	I <sub>+</sub>	All Channels OFF V <sub>IN1</sub> = V <sub>IN2</sub> = 0.8 V	1	0.75		25		25	μA	
Negative Supply Current	I <sub>-</sub>		1	-1	-25		-25			
Reference Supply Current	I <sub>R</sub>		1	0.5	-25		-25			



ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG144
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V V <sub>IN2</sub> = 2.5 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		B SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3			-10	10	-8	8	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA V <sub>IN1</sub> = 3 V (SW1 ON) V <sub>IN1</sub> = 2 V (SW2 ON)	V <sub>D</sub> = 10 V	1,3 2	20		30 60			Ω
			V <sub>D</sub> = 8 V	1,3 2	35				50 75	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW1 OFF) V <sub>IN1</sub> = 3 V (SW2 OFF)	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V	1 2	0.15		1 100			nA
			V <sub>S</sub> = 8 V V <sub>D</sub> = -8 V	1 2	0.75				5 100	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW2 OFF)	V <sub>D</sub> = 10 V V <sub>S</sub> = -10 V	1 2	0.03		1 100			
			V <sub>D</sub> = 8 V V <sub>S</sub> = -8 V	1 2	0.15				5 100	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>IN1</sub> = 3 V (SW1 ON) V <sub>IN1</sub> = 2 V (SW2 ON)	V <sub>D</sub> = V <sub>S</sub> = -10 V	1 2	-0.05	-2 -100				
			V <sub>D</sub> = V <sub>S</sub> = -8 V	1 2	-0.12				-5 -100	
<b>INPUT</b>										
Input 1 Current Input 1 Voltage LOW	I <sub>IN1L</sub>	V <sub>IN1</sub> = 2 V	1,3 2	0.001			0.1 2		4 4	μA
Input 2 Current Input 2 Voltage LOW	I <sub>IN2L</sub>	V <sub>IN2</sub> = 2 V, V <sub>IN1</sub> = 2.5 V	1,3 2	0.001			0.1 2		4 4	
Input 1 Current Input 1 Voltage HIGH	I <sub>IN1H</sub>	V <sub>IN1</sub> = 3 V	1,2 3	20			60 120		100 150	
Input 2 Current Input 2 Voltage HIGH	I <sub>IN2H</sub>	V <sub>IN2</sub> = 3 V, V <sub>IN1</sub> = 2.5 V	1,2 3	20			60 120		100 150	
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit <sup>e</sup>	1	0.5			0.8		1	μs
Turn-OFF Time	t <sub>OFF</sub>		1	1.0			1.6		2	

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ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG144
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V V <sub>IN2</sub> = 2.5 V		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>										
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	f = 1 MHz	V <sub>D</sub> = 0 V I <sub>S</sub> = 0	1	2.4					pF
Source-OFF Capacitance	C <sub>S(OFF)</sub>		V <sub>S</sub> = 0 V I <sub>D</sub> = 0	1	2.4					
Channel-ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	2.8					
OFF Isolation		R <sub>L</sub> = 75 Ω, f = 1 MHz		1	>60					dB
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	One Channel ON V <sub>IN1</sub> = 2 V or V <sub>IN1</sub> = 3V		1	2.6		4.2		4.5	mA
Negative Supply Current	I <sub>-</sub>			1	-1.3	-2		-2.2		
Reference Supply Current	I <sub>R</sub>			1	-1.4	-2.2		-2.4		
Positive Supply Current	I <sub>+</sub>	All Channels OFF V <sub>IN1</sub> = V <sub>IN2</sub> = 0.8 V		1	0.75		25		25	μA
Negative Supply Current	I <sub>-</sub>			1	-1	-25		-25		
Reference Supply Current	I <sub>R</sub>			1	-0.5	-25		-25		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG146	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V V <sub>IN2</sub> = 2.5 V		LIMITS						UNIT	
				1=25°C		A SUFFIX		B SUFFIX			
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3			-10	10	-8	8	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA V <sub>IN1</sub> = 3 V (SW1 ON) V <sub>IN1</sub> = 2 V (SW2 ON)	V <sub>D</sub> = 10 V	1,3 2	7		10 20				Ω
			V <sub>D</sub> = 8 V	1,3 2					15 25		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG146
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V V <sub>IN2</sub> = 2.5 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		B SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH (Cont'd)</b>										
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN1</sub> = 2 V (SW1 OFF)	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V	1 2	0.1		10 1000			nA
			V <sub>S</sub> = 8 V V <sub>D</sub> = -8 V	1 2				15 300		
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN1</sub> = 3 V (SW2 OFF)	V <sub>D</sub> = 10 V V <sub>S</sub> = -10 V	1 2	0.1		10 1000			
			V <sub>D</sub> = 8 V V <sub>S</sub> = -8 V	1 2				15 300		
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>IN1</sub> = 3 V (SW1 ON) V <sub>IN1</sub> = 2 V (SW2 ON)	V <sub>D</sub> = V <sub>S</sub> = -10 V	1 2	-0.04	-2 -100				
			V <sub>D</sub> = V <sub>S</sub> = -8 V	1 2				-5 -100		
<b>INPUT</b>										
Input 1 Current Input 1 Voltage LOW	I <sub>IN1L</sub>	V <sub>IN1</sub> = 2 V		1,3 2	0.001		0.1 2		4 4	μA
Input 2 Current Input 2 Voltage LOW	I <sub>IN2L</sub>	V <sub>IN2</sub> = 2 V, V <sub>IN1</sub> = 2.5 V		1,3 2	0.001		0.1 2		4 4	
Input 1 Current Input 1 Voltage HIGH	I <sub>IN1H</sub>	V <sub>IN1</sub> = 3 V		1,2 3	20		60 120		100 150	
Input 2 Current Input 2 Voltage HIGH	I <sub>IN2H</sub>	V <sub>IN2</sub> = 3 V, V <sub>IN1</sub> = 2.5 V		1,2 3	20		60 120		100 150	
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit <sup>e</sup>		1	0.5		1		1.5	μs
Turn-OFF Time	t <sub>OFF</sub>			1	1.2		2.5		2.5	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	f = 1 MHz	V <sub>D</sub> = 0 V I <sub>S</sub> = 0	1	3					pF
Source-OFF Capacitance	C <sub>S(OFF)</sub>		V <sub>S</sub> = 0 V I <sub>D</sub> = 0	1	3					
Channel-ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	2.8					
OFF Isolation		R <sub>L</sub> = 75 Ω, f = 1 MHz		1	>50					dB

**5**

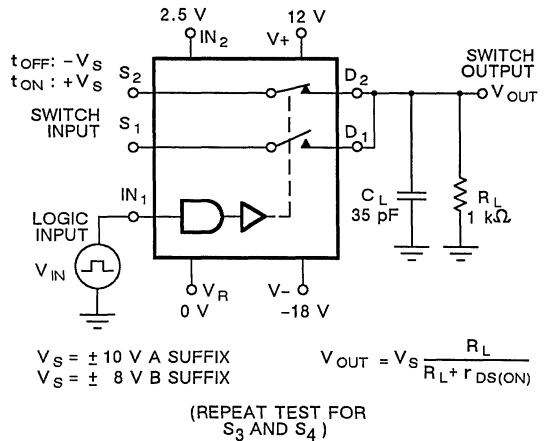
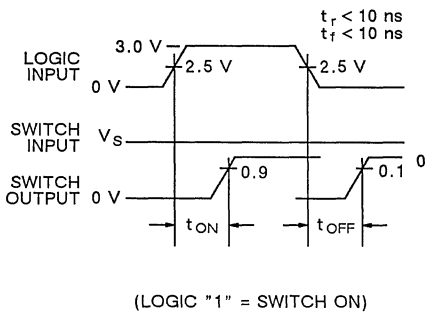
ELECTRICAL CHARACTERISTICS <sup>a</sup>							DG146		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = -18 V V <sub>R</sub> = 0 V V <sub>IN2</sub> = 2.5 V	LIMITS						
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	One Channel ON V <sub>IN1</sub> = 2 V or V <sub>IN1</sub> = 3V	1	2.6		4.2		4.5	mA
Negative Supply Current	I <sub>-</sub>		1	-1.2	-2		-2.2		
Reference Supply Current	I <sub>R</sub>		1	-1.4	-2.2		-2.4		
Positive Supply Current	I <sub>+</sub>	All Channels OFF V <sub>IN1</sub> = V <sub>IN2</sub> = 0.8 V	1	0.75		25		25	μA
Negative Supply Current	I <sub>-</sub>		1	-1	-25		-25		
Reference Supply Current	I <sub>R</sub>		1	-0.5	-25		-25		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> must be a step function with a minimum rise and fall time of 1 V/μs.

**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for V<sub>S</sub> = constant with logic input waveform as shown. Note that V<sub>S</sub> may be + or - as per switching time test circuit. V<sub>O</sub> is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



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**APPLICATION HINTS**


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V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>R</sub> Reference Voltage (V)	V <sub>IN1</sub> Input 1 Voltage V <sub>INH</sub> /V <sub>INL</sub> (V)	V <sub>IN2</sub> Input 2 Voltage (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
12	-18	0	3/2	2.5	-10 to 10
15	-15	0	3/2	2.5	-7 to 13
10	-15	0	3/2	2.5	-7 to 8

## Monolithic 4-Channel PMOS Analog Switch

### FEATURES

- TTL, CMOS Direct Interface
- Voltage Limiting Diodes Protect PMOS Gates
- Four Independent Switches
- Chip Select Pin ( $V_L$ )
- Make-Before-Break Switching

### BENEFITS

- Easy Interface
- Reduces External Protection Components
- Easily Expandable
- Will Not Leave Op Amp Input Floating

### APPLICATIONS

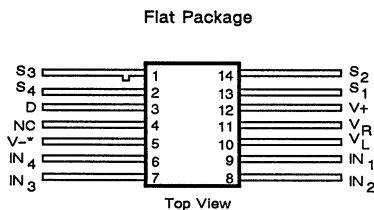
- Programmable Gain Amplifiers
- Sample/Hold
- Solid-State Logic Trees

### DESCRIPTION

The DG172 is a 4-channel single-pole, single-throw analog switch designed for low level logic controlled analog switching in instrumentation, process control, and communications. Featuring Make-Before-Break action, DG172 can be used inside closed loop systems to select one of four inputs for multiplexing/demultiplexing of analog signals or for gain bandwidth control (by switching passive elements) without opening the loop. The reference pin ( $V_R$ ) is normally connected to ground to allow TTL level inputs (0.8 V to 2.0 V) to control the

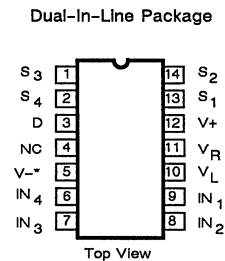
ON-OFF condition of each switch. The DG172 is a bi-directional MOS switch rated to handle 20 V peak-to-peak analog signals at up to 30 mA continuous current. Each switch will block 20 V peak-to-peak signals when OFF. Package options are the 14-pin ceramic and plastic DIP and flatpack. The former is characterized for operation over the standard industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ) and military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) temperature ranges, while the latter is specified for the military range only.

### PIN CONFIGURATION



Order Number:  
DG172AL/883

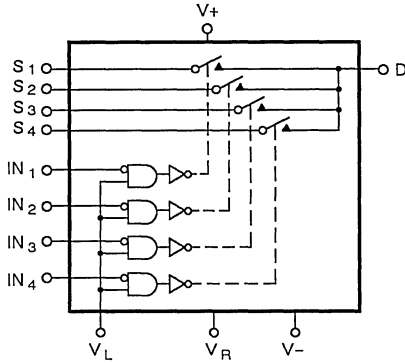
\* Common to Substrate and Base of Package



Order Numbers:

Side Braze: DG172AP, DG172BP  
Plastic: DG172CJ

**FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE**



One 4-Channel Switch per Package\*

Truth Table

LOGIC	SWITCH
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.0$  V

\*Switches Shown for Logic "1" Input

**ABSOLUTE MAXIMUM RATINGS**

V+ to V- .....	36 V	Storage Temperature (A & B Suffix) .....	-65 to 150°C
V+ to V <sub>D</sub> .....	25 V	(C Suffix) .....	-65 to 125°C
V+ to V <sub>S</sub> .....	25 V	Operating Temperature (A Suffix) .....	-55 to 125°C
V <sub>S</sub> to V- .....	36 V	(B Suffix) .....	-25 to 85°C
V <sub>D</sub> to V- .....	36 V	(C Suffix) .....	0 to 70°C
V <sub>S</sub> to V <sub>D</sub> .....	25 V	Power Dissipation (Package)*	
V <sub>L</sub> to V- .....	30 V	Flat Package** .....	750 mW
V <sub>L</sub> to V <sub>IN</sub> .....	$\pm 6$ V	14-Pin Ceramic DIP*** .....	825 mW
V <sub>L</sub> to V <sub>R</sub> .....	$\pm 6$ V	14-Pin Plastic DIP**** .....	470 mW
V <sub>IN</sub> to V <sub>R</sub> .....	$\pm 6$ V	* All leads welded or soldered to PC board.	
Current (Any Terminal) .....	20 mA	** Derate 10 mW/°C above 75°C.	
		*** Derate 11 mW/°C above 75°C.	
		**** Derate 6.3 mW/°C above 75°C.	

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**ELECTRICAL CHARACTERISTICS<sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 10 V V- = -20 V V <sub>R</sub> = 0 V V <sub>L</sub> = 5 V	LIMITS								UNIT
			1=25°C		A SUFFIX		B SUFFIX		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-10	10	-10	10	-10	10	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -1 mA V <sub>IN</sub> = 0.8 V	V <sub>D</sub> = 10 V	1,3	100	150	150	200			Ω
				2	130	250	250	300			
				2	130	350	300	300			
			V <sub>D</sub> = 0 V	1,3	130	200	225	300			
			V <sub>D</sub> = -10 V	1,3	300	450	500	600			
				2	300	600	600	600			

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 10 V V <sub>-</sub> = -20 V V <sub>R</sub> = 0 V V <sub>L</sub> = 5 V	LIMITS								UNIT
			1=25°C		A SUFFIX		B SUFFIX		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH (Cont'd)</b>											
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V V <sub>IN</sub> = 2 V	1 2	-0.03	-1 -1000		-5 -100		-10		nA
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>D</sub> = -10 V, V <sub>S</sub> = 10 V V <sub>IN</sub> = 2 V	1 2	-0.12	-4 -4000		-10 -300		-10		
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 10 V V <sub>IN</sub> = 0.8 V	1 2			4 4000		10 300		10	
<b>INPUT</b>											
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	1,3 2			0.1 10		1 10		1	μA
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1,3 2		-0.5 -0.5		-1 -1		-1		mA
<b>DYNAMIC</b>											
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1			0.3		0.5			μs
Turn-OFF Time	t <sub>OFF</sub>		1			0.75		1.0			
Source OFF <sup>c</sup> Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V, I <sub>D</sub> = 0 f = 1 MHz	1	5							pF
Drain OFF <sup>c</sup> Capacitance	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0 V, I <sub>S</sub> = 0 f = 1 MHz	1	18							
Channel ON <sup>c</sup> Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V, V <sub>IN</sub> = 0 V f = 140 kHz	1	28							
Off Isolation <sup>c</sup>		R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 3 pF f = 5 MHz	1	>50							dB
<b>SUPPLY</b>											
Positive Supply Current	I <sub>+</sub>	One Channel ON V <sub>IN</sub> = 0 V	1	1.3		3		3		3	mA
Negative Supply Current	I <sub>-</sub>		1	-2.0	-5.1		-5.1		-5.1		
Logic Supply Current	I <sub>L</sub>		1	2.5		5.7		5.7		5.7	
		1	0.8		2.1		2.1		2.1		
Reference Supply Current	I <sub>R</sub>	One Channel ON V <sub>IN</sub> = 0 V	1	-1.5	-3.6		-3.6		-3.6		



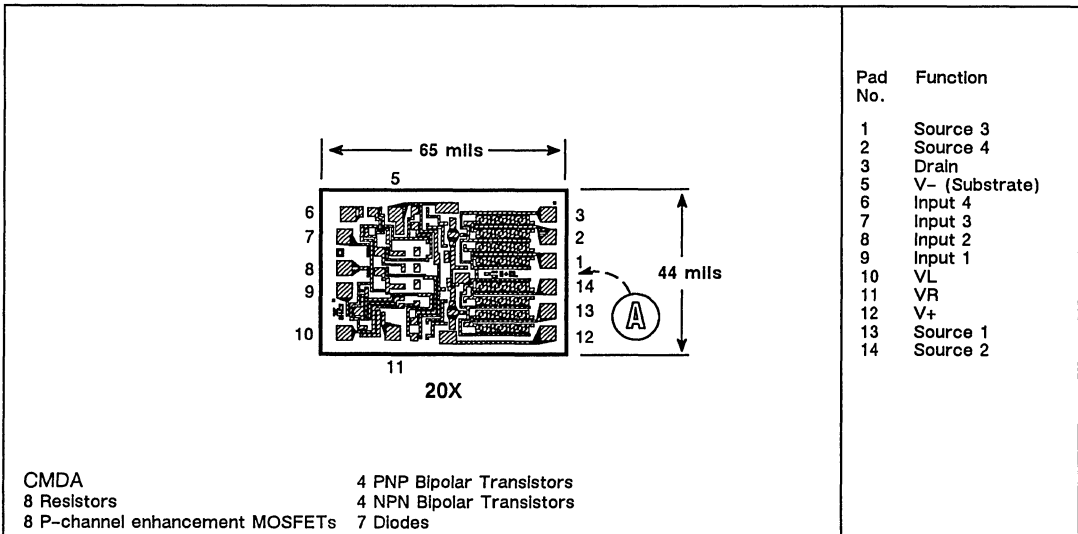
ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = 10 V V <sub>-</sub> = -20 V V <sub>R</sub> = 0 V V <sub>L</sub> = 5 V	LIMITS								UNIT
			1=25°C		A SUFFIX		B SUFFIX		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY</b>											
Positive Supply Current	I <sub>+</sub>	All Channels OFF V <sub>IN</sub> = 5 V	1	0.1		10		10		10	μA
Negative Supply Current	I <sub>-</sub>		1	-0.01	-20		-20		-20		
Logic Supply Current	I <sub>L</sub>	All Channels OFF V <sub>IN</sub> = 5 V I <sub>R</sub> = 0	1	2.0		4.5		4.5		4.5	mA
			1	0.1		10		10		10	μA
Reference Supply Current	I <sub>R</sub>	All Channels OFF V <sub>IN</sub> = 5 V	1	2.0	-4.5		-4.5		-4.5		mA

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

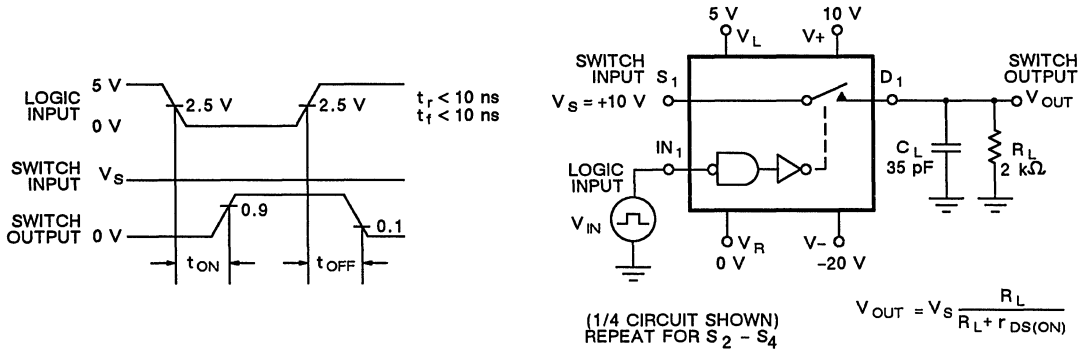
**DIE TOPOGRAPHY**

**5**



## SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



## APPLICATION HINTS\*

$V_+$ Positive Supply Voltage (V)	$V_-$ Negative Supply Voltage (V)	$V_R$ Reference Pin Connection	$V_L$ Logic Supply Voltage (V)	$V_{IN}$ Logic Input Voltage $V_{INH}$ Min/ $V_{INL}$ Max (V)	$V_S$ Analog Signal Range (V)
10**	-20	GND	5	2.0/0.8	-10 to 10
10**	-20	OPEN	5	4.6/0.5	-10 to 10
15	-15	GND	5	2.0/0.8	-5 to 15
20	-10	GND	5	2.0/0.8	0 to 20
5	-15	GND	5	2.0/0.8	-5 to 5
5	-25	GND	5	2.0/0.8	-15 to 5

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

\*\* Electrical Characteristics are based on  $V_+ = +10 \text{ V}$ ,  $V_- = -20 \text{ V}$  only.

## High-Speed Driver with Dual SPST JFET Switches

### FEATURES

- Constant ON Resistance over Entire Analog Range
- Low Leakage
- Low Crosstalk

### BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

### APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- D/A Ladder Switches

### DESCRIPTION

The DG180-182 are precision dual single-pole, single-throw (SPST) analog switches designed to provide accurate switching of video and audio signals. This series, like the entire DG180 family, is ideally suited for applications requiring a constant ON resistance over the entire analog range.

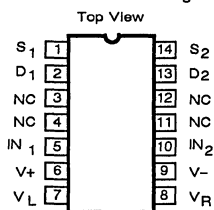
The major design difference is the ON resistance, being 10, 30, and 75  $\Omega$  for the DG180, DG181, and DG182 respectively. Reduced switching errors are achieved through low leakage current ( $I_{S(OFF)} < 1 \text{ nA}$  for the DG181/182). Applications which benefit from flat ON resistance include audio switching, video switching, and sample and holds.

Each device comprises four N-channel JFET transistors and a bipolar driver (TTL compatible) to achieve fast and accurate switch performance. In the ON state, each switch conducts current equally well in either direction. In the OFF condition, the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

Packaging options for the DG180-182 include a 14-pin side braze and 10-pin metal can options. The flatpack version is only available for the DG181. Performance grades include both a military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature ranges. The flatpack option is only available in the military grade.

### PIN CONFIGURATION

Dual-In-Line Package

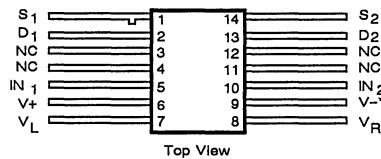


Order Numbers:

Side Braze:

- DG180AP or DG180BP
- DG181AP or DG181BP
- DG182AP or DG182BP

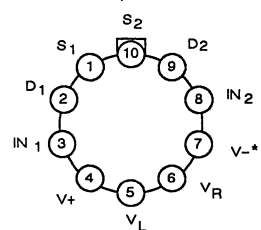
Flat Package



Order Number:

DG181AL/883

Top View



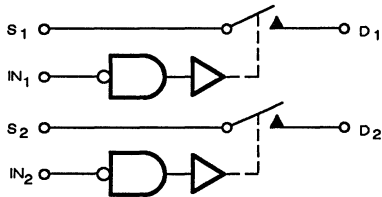
Metal Can Package

Order Numbers:

- DG180AA or DG180BA
- DG181AA or DG181BA
- DG182AA or DG182BA

\* Common to Substrate and Case

## FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package

Truth Table\*

LOGIC	SWITCH
0	ON
1	OFF

Logic "0" < 0.8 V  
 Logic "1"  $\geq$  2.0 V

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

$V_+$ to $V_-$	36 V
$V_+$ to $V_D$	33 V
$V_D$ to $V_-$	33 V
$V_D$ to $V_S$	$\pm 22$ V
$V_L$ to $V_-$	36 V
$V_L$ to $V_{IN}$	8 V
$V_L$ to $V_R$	8 V
$V_{IN}$ to $V_R$	8 V
$V_R$ to $V_-$	27 V
$V_R$ to $V_{IN}$	2 V
Current (S or D) DG180	200 mA
Current (S or D) DG181, DG182	30 mA

Current (All Other Pins)	30 mA
Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C

### Power Dissipation\*

10-Pin Metal Can**	450 mW
14-Pin DIP***	825 mW
14-Pin Flat Pack****	900 mW

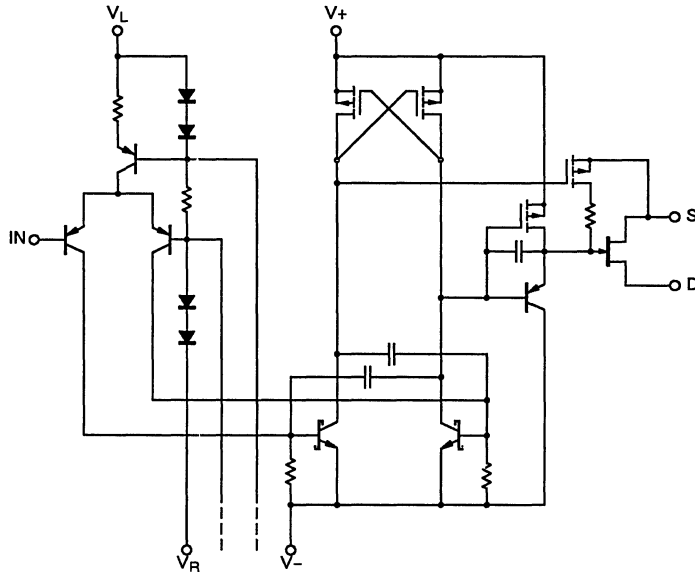
\* All leads welded or soldered to PC board.

\*\* Derate 6 mW/°C above 75°C.

\*\*\* Derate 11 mW/°C above 75°C.

\*\*\*\* Derate 10 mW/°C above 75°C.

## SCHEMATIC DIAGRAM (Typical Channel)



ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG180
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-7.5	15	-7.5	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -7.5 V V <sub>IN</sub> = 0.8 V		1,3 2	7.5		10 20		15 25	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.0 V	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.05		10 1000		15 300	nA
			V <sub>S</sub> = 7.5 V V <sub>D</sub> = -7.5 V	1 2	0.05		10 1000		15 300	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.04		10 1000		15 300	
			V <sub>S</sub> = -7.5 V V <sub>D</sub> = 7.5 V	1 2	0.03		10 1000		15 300	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = -7.5 V V <sub>IN</sub> = 0.8 V		1 2	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I <sub>DSS</sub>	2 ms Pulse Duration		1	300					mA
<b>INPUT</b>										
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V		1 2	<0.01		10 20		10 20	μA
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V		1,2,3	-30	-250		-250		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit		1	240		300		350	ns
Turn-OFF Time	t <sub>OFF</sub>			1	140		250		300	
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	1	21					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	1	17					
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	17					
OFF Isolation		f = 1 MHz, R <sub>L</sub> = 75 Ω		1	>55					dB

**5**

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG180
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		B SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 V or 5 V	1	0.6		1.5		1.5	mA	
Negative Supply Current	I <sub>-</sub>		1	-2.7	-5		-5			
Logic Supply Current	I <sub>L</sub>		1	3		4.5		4.5		
Reference Supply Current	I <sub>R</sub>		1	-1	-2		-2			

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG181
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		B SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-7.5	15	-7.5	15	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -7.5 V V <sub>IN</sub> = 0.8 V	1,3 2	18		30 60		50 75	Ω	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.0 V	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.05		1 100		5 100	nA
			V <sub>S</sub> = 7.5 V V <sub>D</sub> = -7.5 V	1 2	0.07		1 100		5 100	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.5		1 100		5 100	
			V <sub>S</sub> = -7.5 V V <sub>D</sub> = 7.5 V	1 2	0.6		1 100		5 100	
Channel ON Leakage Current	I <sub>D(ON)+</sub> I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = -7.5 V V <sub>IN</sub> = 0.8 V	1 2	-0.02	-2 -200		-10 -200			
<b>INPUT</b>										
Input Current with input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	1 2	<0.01		10 20		10 20	μA	
Input Current with input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1,2,3	-30	-250		-250			

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG181	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V			LIMITS						UNIT
					1=25°C		A SUFFIX		B SUFFIX		
					TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>											
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit			1	85		150		180	ns
Turn-OFF Time	t <sub>OFF</sub>				1	95		130		150	
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	V <sub>S</sub> = -5 V, I <sub>D</sub> = 0		1	9				pF	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0		1	6					
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V		1	14					
OFF Isolation		f = 1 MHz, R <sub>L</sub> = 75 Ω			1	>50					dB
<b>SUPPLY</b>											
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 V or 5 V			1	0.6		1.5		1.5	mA
Negative Supply Current	I <sub>-</sub>				1	-2.7	-5		-5		
Logic Supply Current	I <sub>L</sub>				1	3.1		4.5		4.5	
Reference Supply Current	I <sub>R</sub>				1	-1	-2		-2		

5

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG182	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V			LIMITS						UNIT
					1=25°C		A SUFFIX		B SUFFIX		
					TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>				1,2,3		-10	15	-10	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -10 V V <sub>IN</sub> = 0.8 V			1,3 2	35		75 150		100 150	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.0 V	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V		1 2	0.05		1 100		5 100	nA
			V <sub>S</sub> = 10 V, V <sub>D</sub> = -20 V		1 2	0.07		1 100		5 100	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG182
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH (Cont'd)</b>										
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN</sub> = 2.0 V	V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V	1	0.4		1		5	nA
			V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	2		100		100		
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = -10 V V <sub>IN</sub> = 0.8 V		1	-0.02	-2		-10		
				2		-200		-200		
<b>INPUT</b>										
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V		1	<0.01		10		10	μA
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V		1,2,3	-30	-250		-250		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit		1	120		250		300	ns
Turn-OFF Time	t <sub>OFF</sub>			1	100		130		150	
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	1	9					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	1	6					
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	14					
OFF Isolation		f = 1 MHz, R <sub>L</sub> = 75 Ω		1	>50					dB
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 V or 5 V		1	0.6		1.5		1.5	mA
Negative Supply Current	I <sub>-</sub>			1	-2.7	-5		-5		
Logic Supply Current	I <sub>L</sub>			1	3.1		4.5		4.5	
Reference Supply Current	I <sub>R</sub>			1	-1	-2		-2		

**NOTES:**

a. Refer to PROCESS OPTION FLOWCHART for additional information.

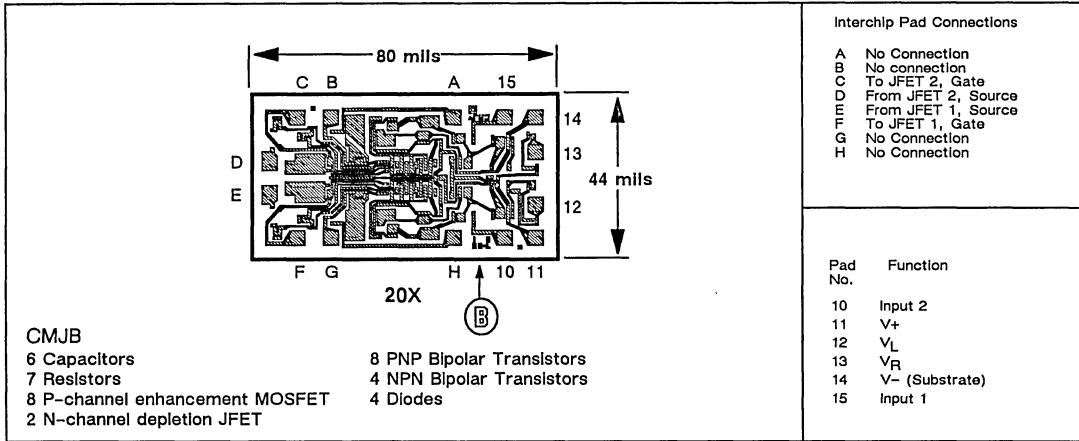
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Guaranteed by design, not subject to production test.

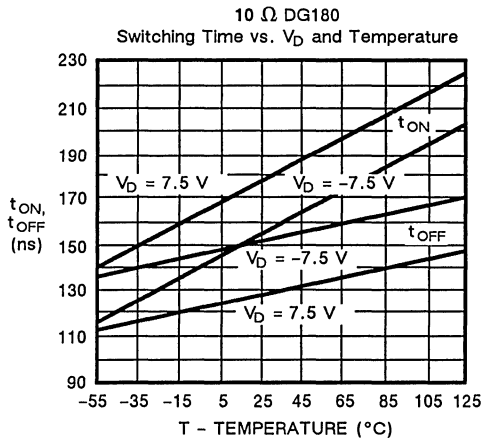
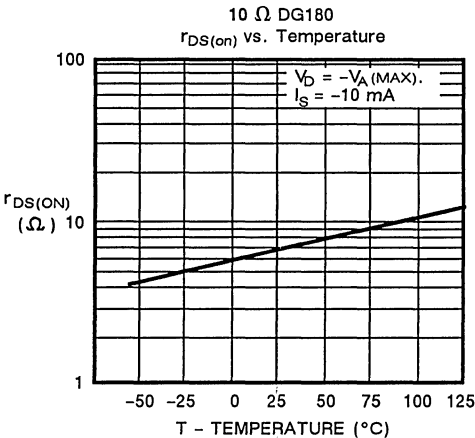
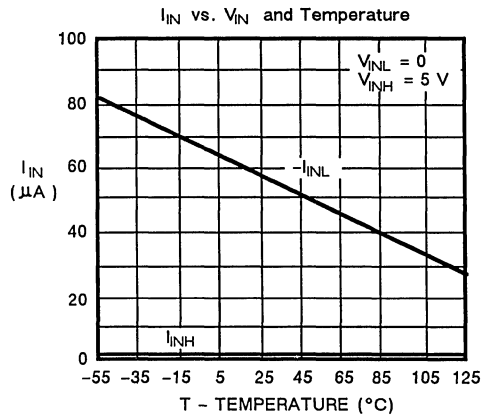
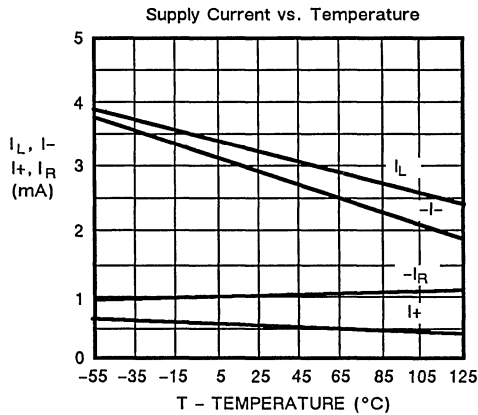
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.



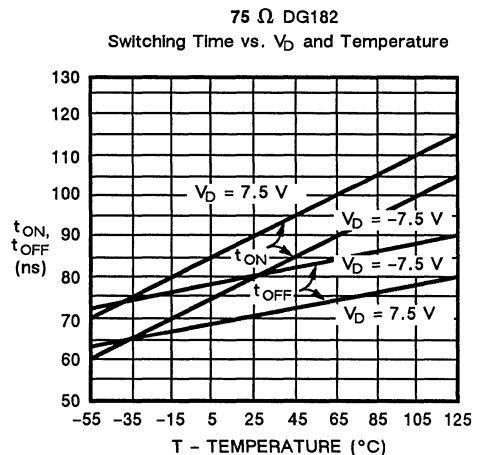
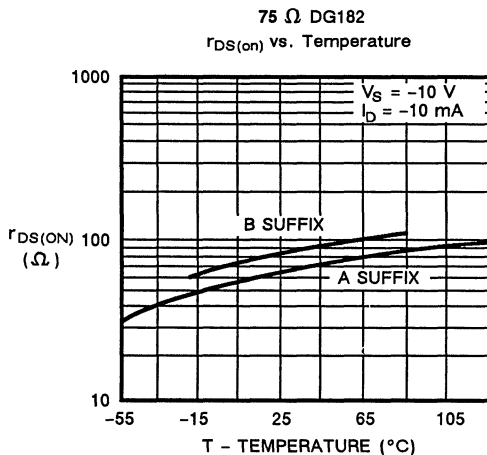
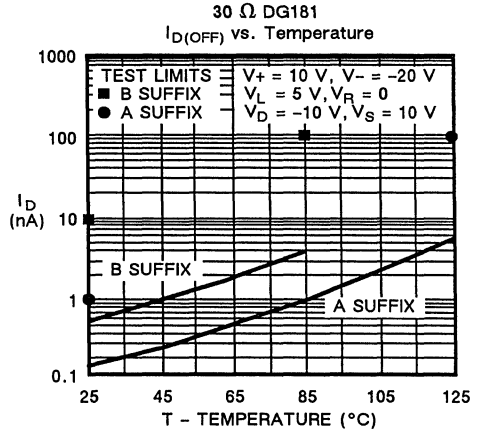
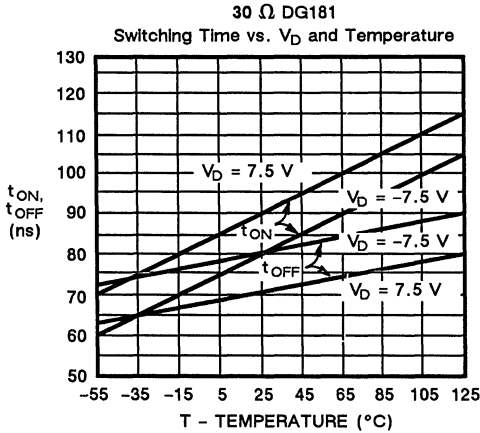
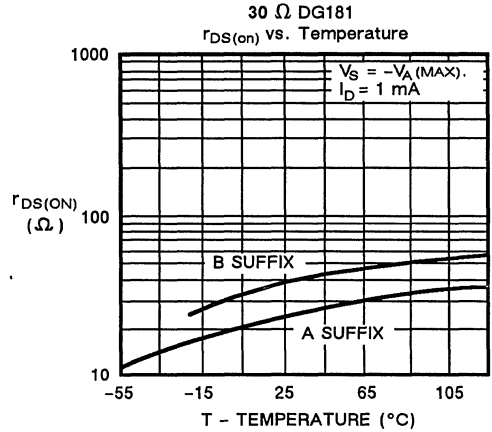
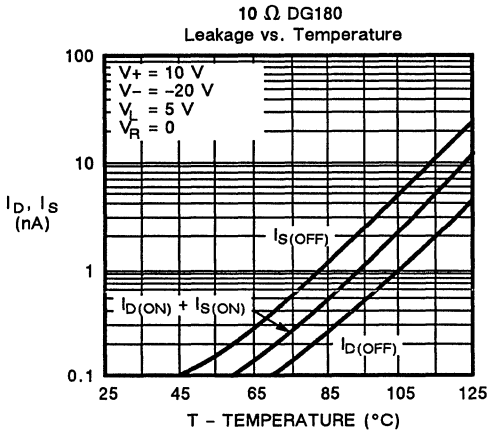
## DIE TOPOGRAPHY



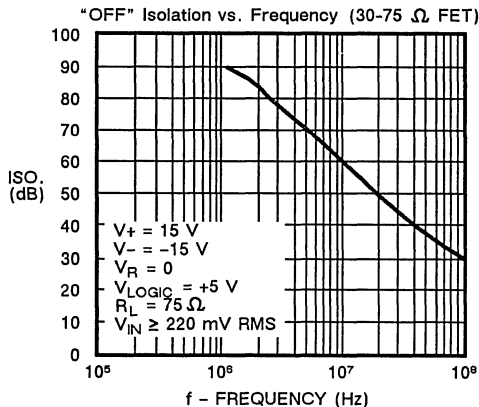
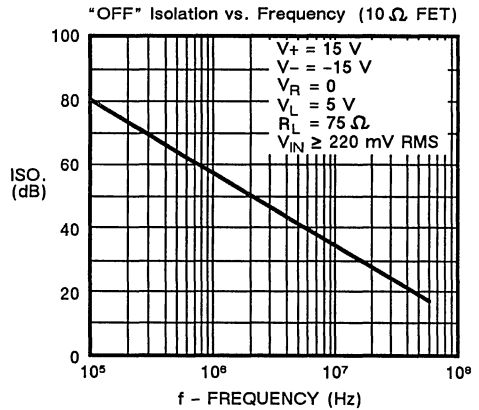
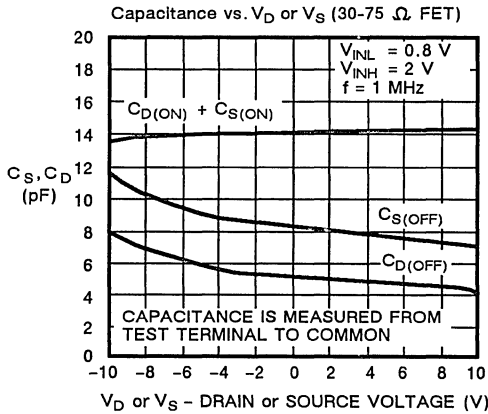
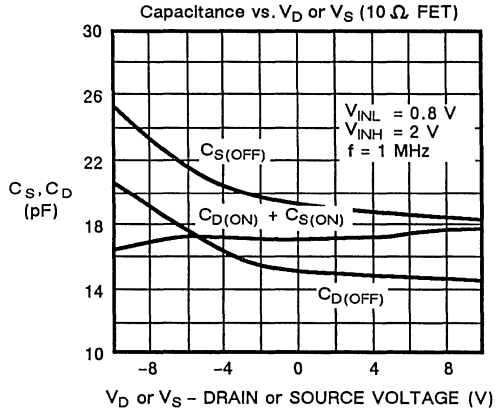
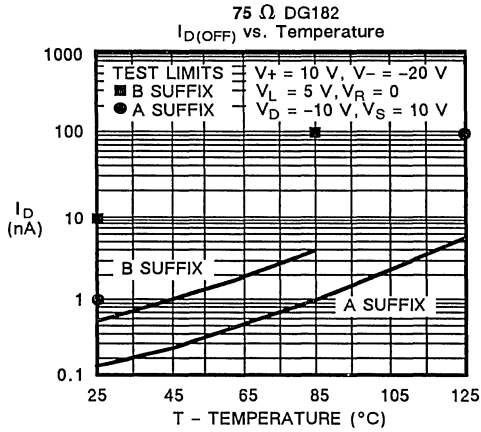
## TYPICAL CHARACTERISTICS



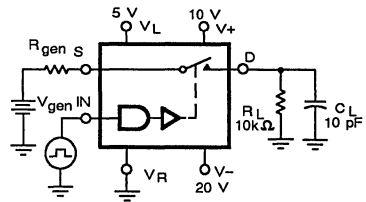
## TYPICAL CHARACTERISTICS (Cont'd)



## TYPICAL CHARACTERISTICS (Cont'd)



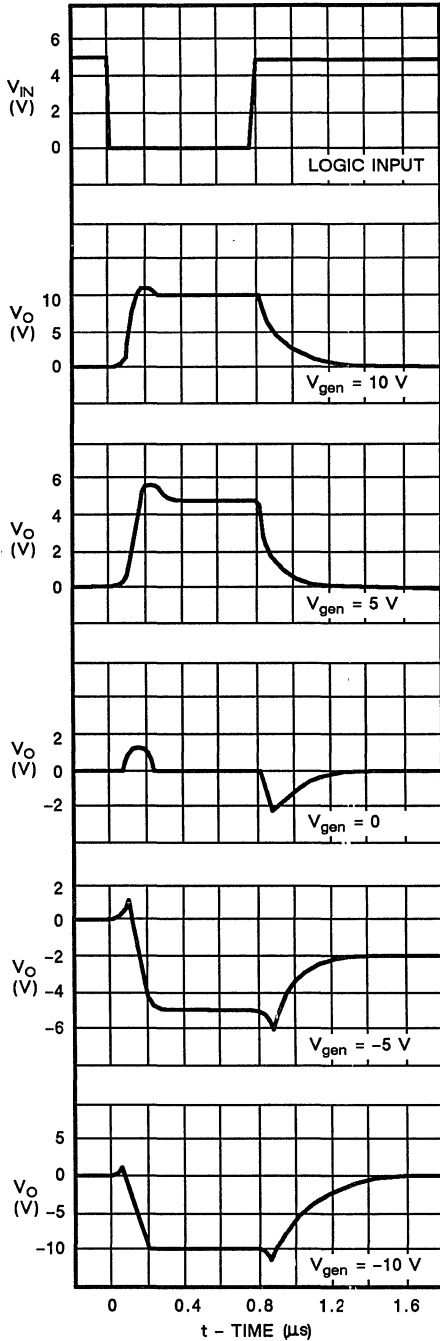
Typical delay, rise, fall, settling times, and switching transients in this circuit.



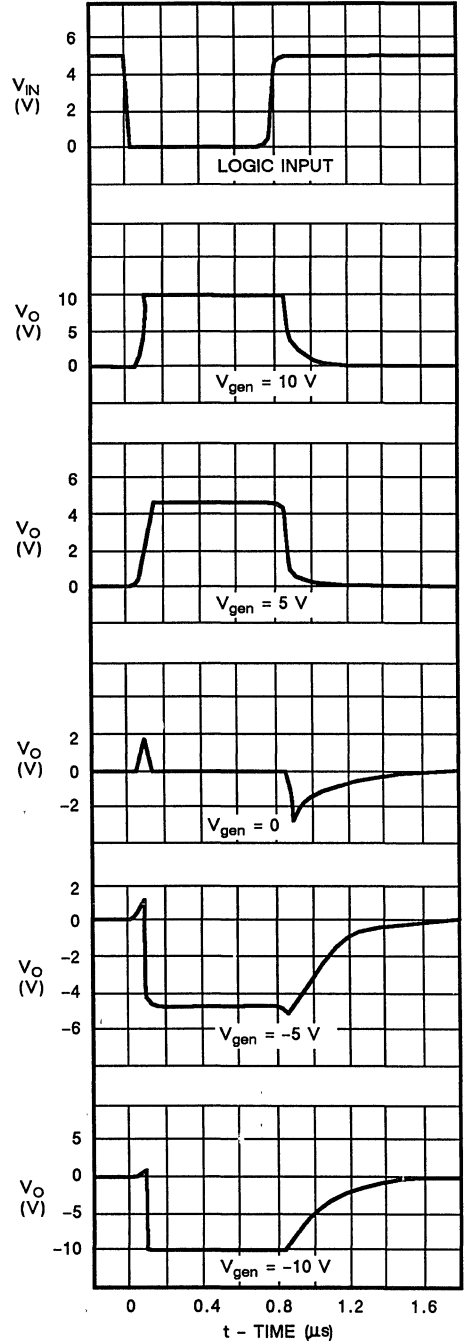
If  $R_{gen}$ ,  $R_L$ , or  $C_L$  is increased, there will be proportional increases in rise and/or fall times.

## TYPICAL CHARACTERISTICS (Cont'd)

DG180

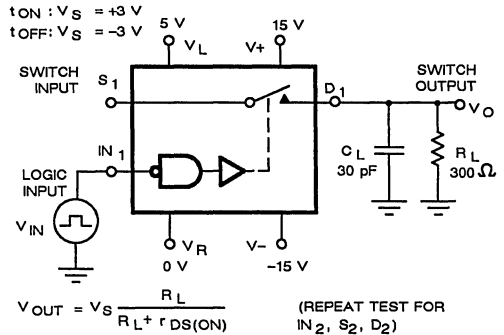
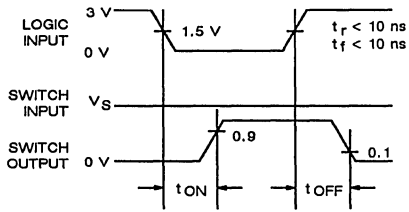


DG181, DG182



## SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for  $V_S =$  constant with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



## APPLICATION HINTS\*

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	VL Logic Supply Voltage (V)	VR Reference Supply Voltage (V)	VIN Logic Input Voltage VINH Min/ VINL Max (V)	VS Analog Voltage Range (V)
10 Ω and 30 Ω	15**	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
75 Ω	15**	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

\*\* Electrical Parameter Chart based on V+ = 15 V, V- = -15 V, VL = 5 V, VR = GND.

# DG183/184/185

## High-Speed Driver with Dual DPST JFET Switches

### FEATURES

- Constant ON Resistance over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Break-Before-Make Switching

### BENEFITS

- Low Distortion
- Reduced Switching Errors
- Improved Channel Isolation
- Eliminates Inadvertent Shorting Between Channels

### APPLICATIONS

- Audio Switching
- Precision Switching
- Video Switching
- Video Routing
- Sample/Hold D/A Ladder Switches

### DESCRIPTION

The DG183-185 are precision dual double-pole, single-throw (DPST) analog switches designed to provide accurate switching of audio and video signals. This series is ideally suited for applications requiring a constant ON resistance over the entire analog range.

The major design difference is in ON resistance, being 10, 30, and 75  $\Omega$  for the DG183, DG184 and DG185, respectively.

Reducing switching errors is also accomplished through low leakage ( $I_{S(OFF)} < 1 \mu A$  for the DG184/185). Applications which benefit from flat ON resistance include audio switching, video switching, and sample and holds.

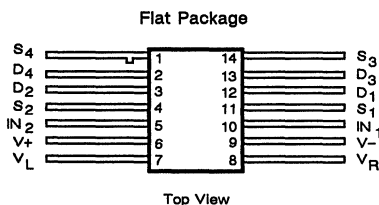
Each device consists of four N-channel JFET transistors and a bipolar driver (TTL compatible) to

achieve fast and accurate switch performance. The driver is designed to achieve Break-Before-Make switching action, eliminating inadvertent shorting and the crosstalk between channels that may result. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

Packaging options for the DG183-185 include a 16-pin side braze and flatpack. Performance grades include both the military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature ranges. The flatpack option is only available in the military grade.

The DG184 and DG185 are JAN qualified devices.

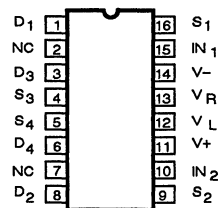
### PIN CONFIGURATION



Order Numbers:

DG184AL/883, DG185AL/883

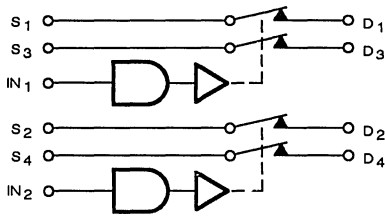
### Dual-In-Line Package



Order Numbers:

Side Braze:  
 DG183AP, DG183BP  
 DG184AP, DG184BP  
 DG185AP, DG185BP

## FUNCTIONAL BLOCK DIAGRAM



Two DPST Switches per Package\*

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0" < 0.8 V  
Logic "1" ≥ 2.0 V

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

V <sub>+</sub> to V <sub>-</sub>	36 V
V <sub>+</sub> to V <sub>D</sub>	33 V
V <sub>D</sub> to V <sub>-</sub>	33 V
V <sub>D</sub> to V <sub>S</sub>	±22 V
V <sub>L</sub> to V <sub>-</sub>	36 V
V <sub>L</sub> to V <sub>IN</sub>	8 V
V <sub>L</sub> to V <sub>R</sub>	8 V
V <sub>IN</sub> to V <sub>R</sub>	8 V
V <sub>R</sub> to V <sub>-</sub>	27 V
V <sub>R</sub> to V <sub>+</sub>	27 V
V <sub>R</sub> to V <sub>IN</sub>	2 V

Current (S or D) DG183	200 mA
Current (S or D) DG184, DG185	30 mA
Current (All Other Pins)	30 mA
Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C

### Power Dissipation\*

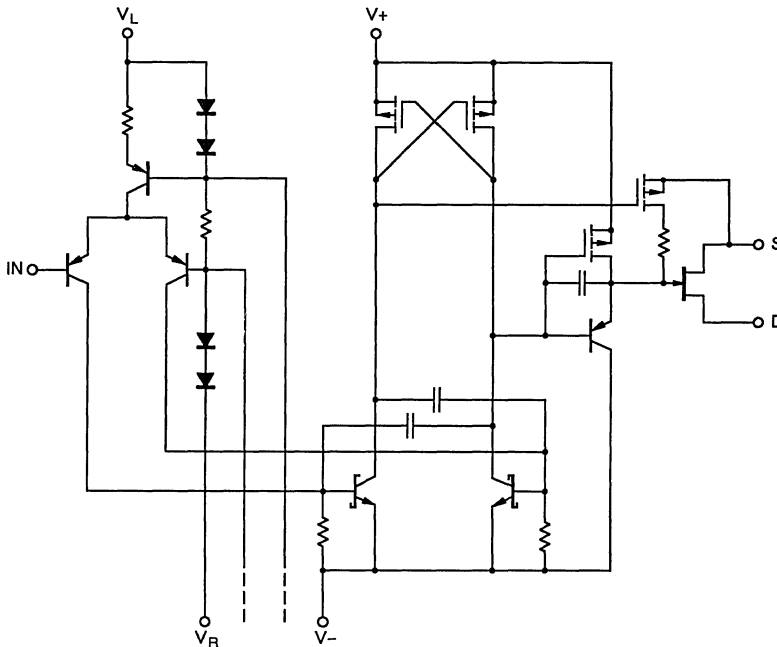
16-Pin DIP**	900 mW
Flat Pack***	900 mW

\* All leads welded or soldered to PC board

\*\* Derate 12 mW/°C above 75°C

\*\*\* Derate 10 mW/°C above 75°C

## SCHEMATIC DIAGRAM (Typical Channel)



ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG183
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ $V_R = 0\text{ V}$		LIMITS						UNIT
				1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$			1,2,3		-7.5	15	-7.5	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -10\text{ mA}$ , $V_D = -7.5\text{ V}$ $V_{IN} = 2.0\text{ V}$		1,3 2	7.5		10 20		15 25	$\Omega$
Source OFF Leakage Current	$I_{S(OFF)}$	$V_{IN} = 0.8\text{ V}$	$V_S = 10\text{ V}$ , $V_D = -10\text{ V}$ $V_+ = 10\text{ V}$ , $V_- = -20\text{ V}$	1 2	0.05		10 1000		15 300	nA
			$V_S = 7.5\text{ V}$ $V_D = -7.5\text{ V}$	1 2	0.05		10 1000		15 300	
Drain OFF Leakage Current	$I_{D(OFF)}$		$V_S = -10\text{ V}$ , $V_D = 10\text{ V}$ $V_+ = 10\text{ V}$ , $V_- = -20\text{ V}$	1 2	0.04		10 1000		15 300	
			$V_S = -7.5\text{ V}$ $V_D = 7.5\text{ V}$	1 2	0.03		10 1000		15 300	
Channel ON Leakage Current	$I_{D(ON)+I_{S(ON)}}$	$V_D = V_S = -7.5\text{ V}$ $V_{IN} = 2.0\text{ V}$		1 2	-0.1	-2 -200		-10 -200		
Saturation Drain Current	$I_{DSS}$	2 ms Pulse Duration		1	300					mA
<b>INPUT</b>										
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 5\text{ V}$		1 2	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0\text{ V}$		1,2,3	-30	-250		-250		
<b>DYNAMIC</b>										
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit		1	240		300		350	ns
Turn-OFF Time	$t_{OFF}$			1	140		250		300	
Source-OFF Capacitance	$C_{S(OFF)}$	$f = 1\text{ MHz}$	$V_S = -5\text{ V}$ , $I_D = 0$	1	21					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		$V_D = -5\text{ V}$ , $I_S = 0$	1	17					
Channel ON Capacitance	$C_{D(ON)+C_{S(ON)}}$		$V_D = V_S = 0$	1	17					
Off Isolation		$f = 1\text{ MHz}$ , $R_L = 75\Omega$		1	>55					dB



ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG183	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> (All) = 0 V	1			3		3	mA
		V <sub>IN</sub> (All) = 5 V	1			0.1		0.1	
Negative Supply Current	I <sub>-</sub>	V <sub>IN</sub> (All) = 0 V	1		-5.5		-5.5		
		V <sub>IN</sub> (All) = 5 V	1		-4		-4		
Logic Supply Current	I <sub>L</sub>	V <sub>IN</sub> (All) = 0 V	1			4.5		4.5	
		V <sub>IN</sub> (All) = 5 V	1			4.5		4.5	
Reference Supply Current	I <sub>R</sub>	V <sub>IN</sub> (All) = 0 V	1		-2		-2		
		V <sub>IN</sub> (All) = 5 V	1		-2		-2		

ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG184	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-7.5	15	-7.5	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -7.5 V V <sub>IN</sub> = 2.0 V	1,3 2	22		30 60		50 75	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 0.8 V	1 2	0.06		1 100		5 100	nA
						V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V			
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		1 2	0.04		1 100		5 100	
						V <sub>S</sub> = 7.5 V V <sub>D</sub> = -7.5 V			
Channel ON Leakage Current	I <sub>D(ON)</sub> † I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = -7.5 V V <sub>IN</sub> = 2.0 V	1 2	-0.02	-2 -200		-10 -200		
								V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG184	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ $V_R = 0\text{ V}$			LIMITS						UNIT
					1=25°C		A SUFFIX		B SUFFIX		
					TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>											
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 5\text{ V}$	1 2	<0.01		10 20		10 20		$\mu\text{A}$	
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0\text{ V}$	1,2,3	-30	-250			-250			
<b>DYNAMIC</b>											
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit		1	85		150		180	ns	
Turn-OFF Time	$t_{OFF}$			1	95		130		150		
Source-OFF Capacitance	$C_{S(OFF)}$	$f = 1\text{ MHz}$	$V_S = -5\text{ V}, I_D = 0$	1	9					pF	
Drain-OFF Capacitance	$C_{D(OFF)}$		$V_D = -5\text{ V}, I_S = 0$	1	6						
Channel ON Capacitance	$C_{D(ON)} + C_{S(ON)}$		$V_D = V_S = 0$	1	14						
Off Isolation		$f = 1\text{ MHz}, R_L = 75\ \Omega$	1	>50						dB	
<b>SUPPLY</b>											
Positive Supply Current	$I_+$	$V_{IN} (\text{All}) = 0\text{ V}$	1			3		3		mA	
		$V_{IN} (\text{All}) = 5\text{ V}$	1			0.1		0.1			
Negative Supply Current	$I_-$	$V_{IN} (\text{All}) = 0\text{ V}$	1		-5.5		-5.5				
		$V_{IN} (\text{All}) = 5\text{ V}$	1		-4		-4				
Logic Supply Current	$I_L$	$V_{IN} (\text{All}) = 0\text{ V}$	1			4.5		4.5			
		$V_{IN} (\text{All}) = 5\text{ V}$	1			4.5		4.5			
Reference Supply Current	$I_R$	$V_{IN} (\text{All}) = 0\text{ V}$	1		-2		-2				
		$V_{IN} (\text{All}) = 5\text{ V}$	1		-2		-2				

ELECTRICAL CHARACTERISTICS <sup>a</sup>							DG185				
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V		LIMITS						UNIT	
				1=25°C		A SUFFIX		B SUFFIX			
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-10	15	-10	15	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = -10 V V <sub>IN</sub> = 2.0 V		1,3 2	35		75 150		100 150	Ω	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 0.8 V	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V	1 2	0.05		1 100		5 100	nA	
			V <sub>S</sub> = 10 V, V <sub>-</sub> = -20 V								
	V <sub>S</sub> = 10 V V <sub>D</sub> = -10 V		1 2	0.07		1 100		5 100			
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V	1 2	0.04		1 100		5 100		
		V <sub>S</sub> = -10 V V <sub>D</sub> = 10 V	1 2	0.03		1 100		5 100			
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = -10 V V <sub>IN</sub> = 2.0 V		1 2	-0.03	-2 -200		-10 -200			
<b>INPUT</b>											
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V		1 2	<0.01		10 20		20	μA	
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V		1,2,3	-35	-250		-250			
<b>DYNAMIC</b>											
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit			1	120		250		300	ns
Turn-OFF Time	t <sub>OFF</sub>				1	100		130		150	
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	1	9					pF	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	1	6						
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	14						
Off Isolation		f = 1 MHz, R <sub>L</sub> = 75 Ω			1	>50					dB

ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG185	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> (All) = 0 V	1			3		3	mA
		V <sub>IN</sub> (All) = 5 V	1			0.1		0.1	
Negative Supply Current	I <sub>-</sub>	V <sub>IN</sub> (All) = 0 V	1		-5.5		-5.5		
		V <sub>IN</sub> (All) = 5 V	1		-4		-4		
Logic Supply Current	I <sub>L</sub>	V <sub>IN</sub> (All) = 0 V	1			4.5		4.5	
		V <sub>IN</sub> (All) = 5 V	1			4.5		4.5	
Reference Supply Current	I <sub>R</sub>	V <sub>IN</sub> (All) = 0 V	1		-2		-2		
		V <sub>IN</sub> (All) = 5 V	1		-2		-2		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**DIE TOPOGRAPHY (DRIVER)**

20X

**Interchip Pad Connections**

A	From JFET 1, Source
B	To JFET 1, Gate
C	To JFET 3, Gate
D	From JFET 3, Source
E	From JFET 4, Source
F	To JFET 4, Gate
G	To JFET 2, Gate
H	From JFET 2, Source

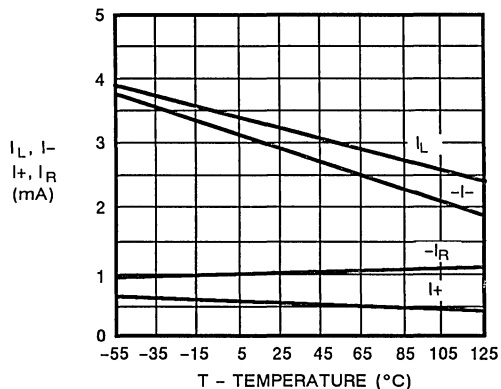
Pad No.	Function
10	Input 2
11	V <sub>+</sub>
12	V <sub>L</sub>
13	V <sub>R</sub>
14	V <sub>-</sub> (Substrate)
15	Input 1

CMJA

8 Capacitors	10 PNP Bipolar Transistors
7 Resistors	4 NPN Bipolar Transistors
12 P-channel enhancement MOSFETs	4 Diodes
4 N-channel depletion JFETs	

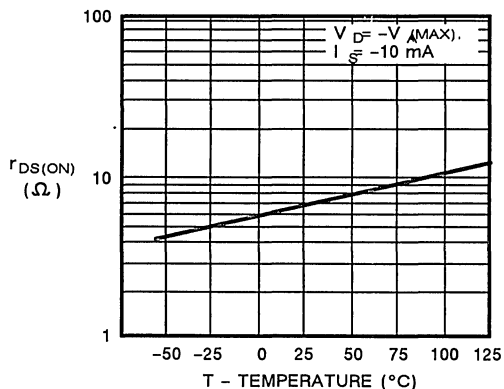
## TYPICAL CHARACTERISTICS

Supply Current vs. Temperature



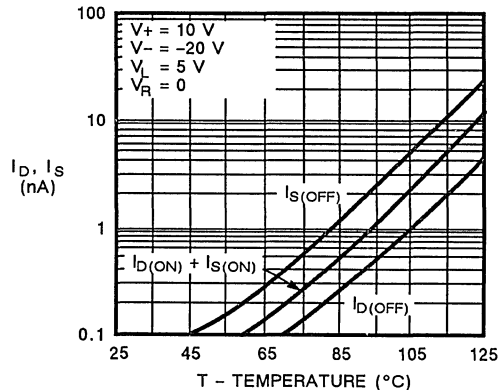
10 Ω DG183

$r_{DS(on)}$  vs. Temperature

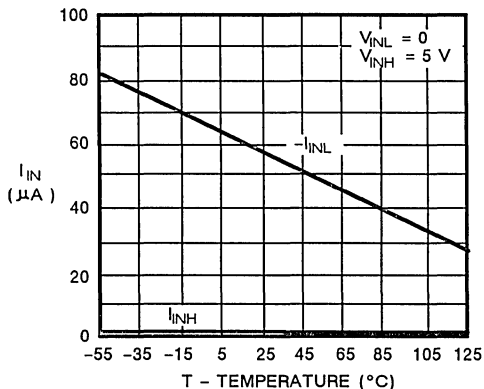


10 Ω DG183

Leakage vs. Temperature

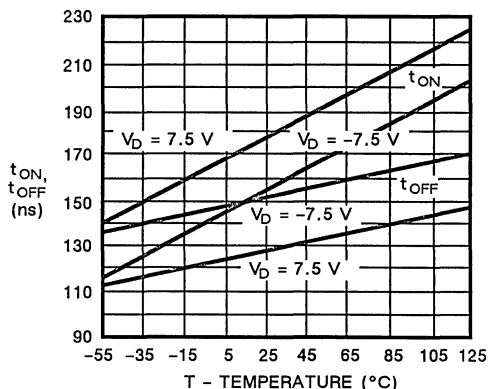


$I_{IN}$  vs.  $V_{IN}$  and Temperature



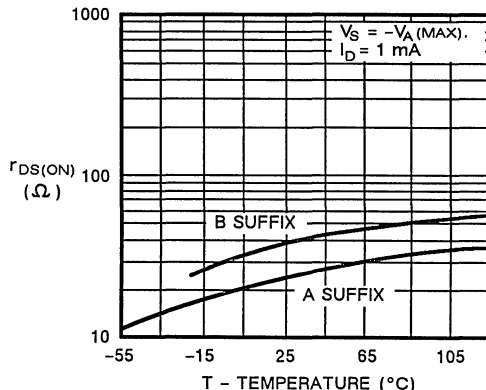
10 Ω DG183

Switching Time vs.  $V_D$  and Temperature

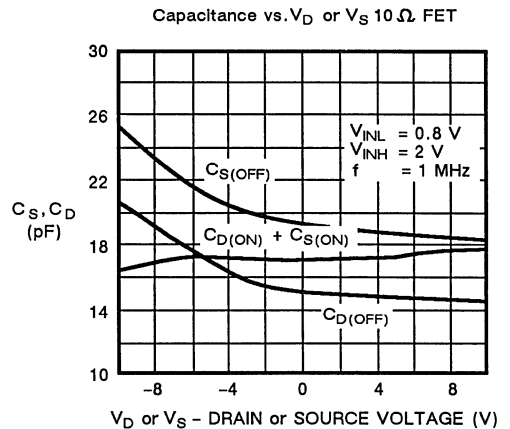
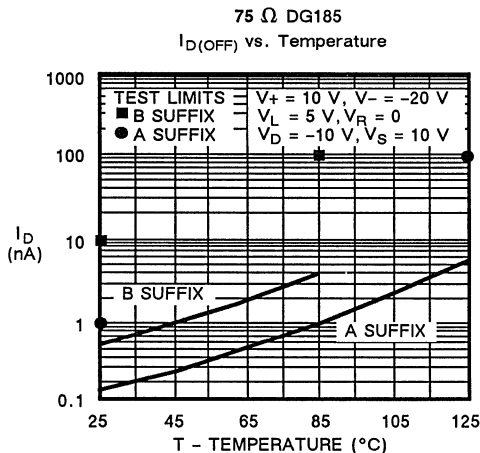
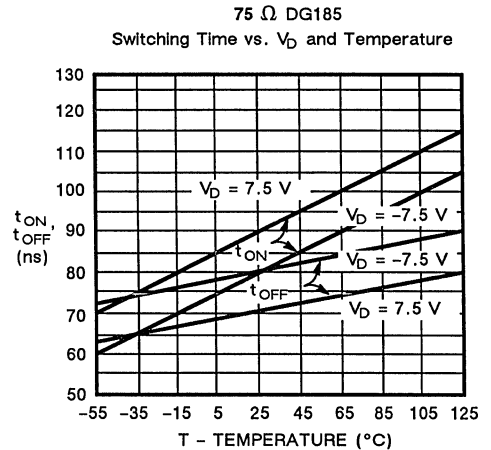
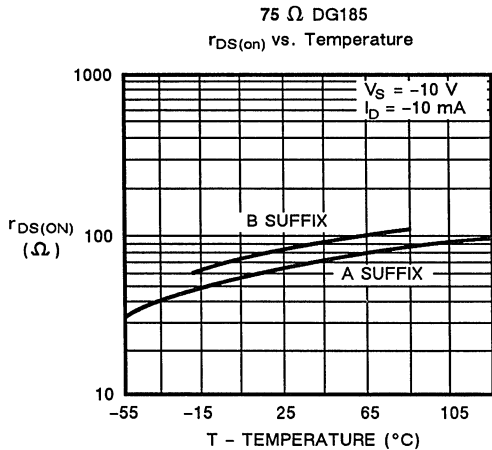
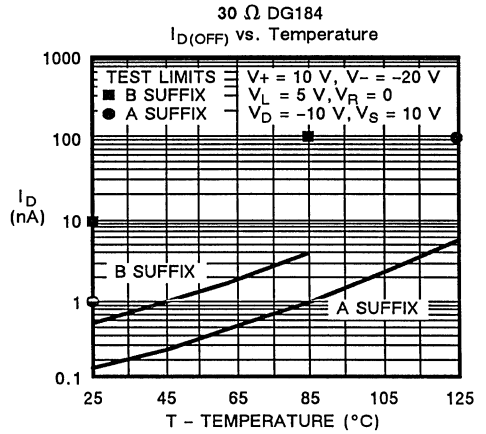
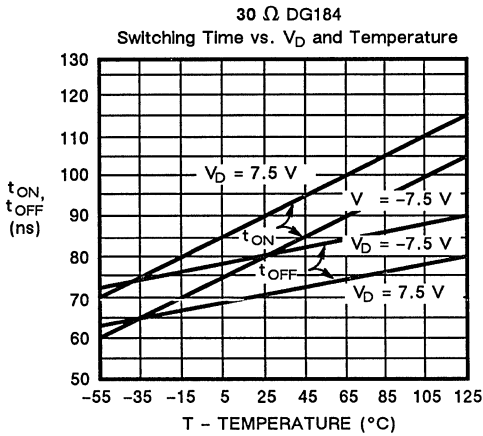


30 Ω DG184

$r_{DS(on)}$  vs. Temperature

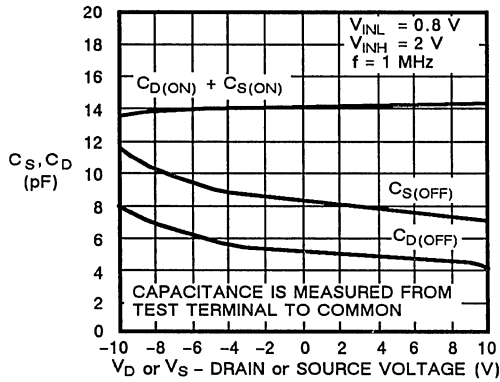


## TYPICAL CHARACTERISTICS (Cont'd)

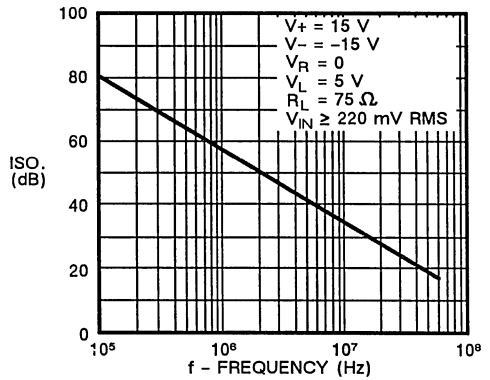


**TYPICAL CHARACTERISTICS (Cont'd)**

Capacitance vs.  $V_D$  or  $V_S$  30-75  $\Omega$  FET



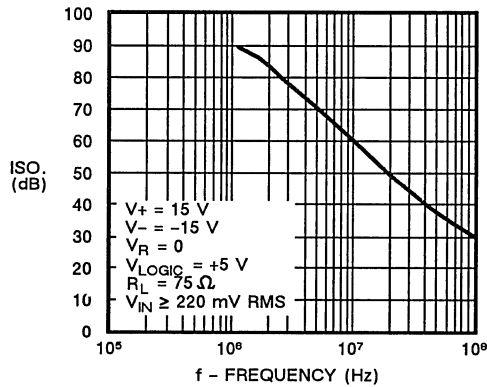
"OFF" Isolation vs. Frequency 10  $\Omega$  FET



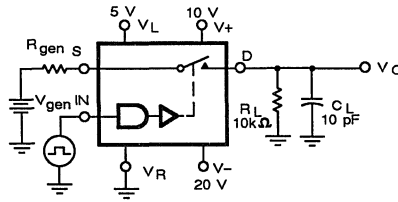
Typical delay, rise, fall, settling times, and switching transients in this circuit.

**5**

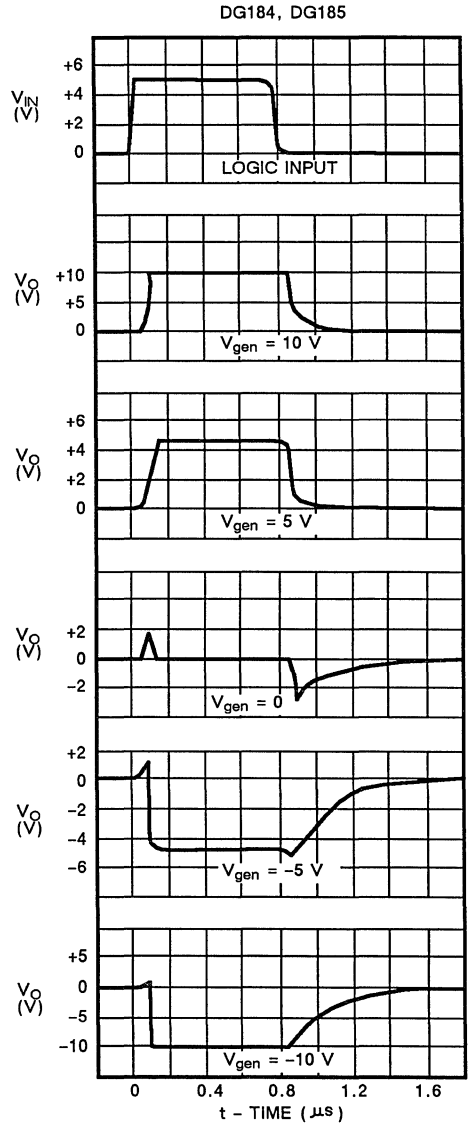
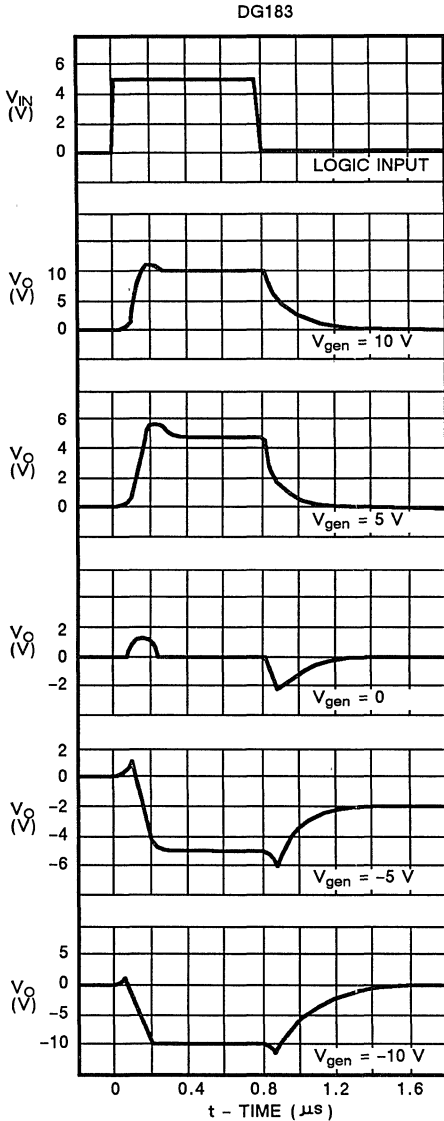
"OFF" Isolation vs. Frequency 30-75  $\Omega$  FET



## TYPICAL CHARACTERISTICS (Cont'd)



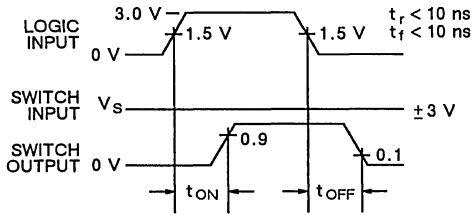
If  $R_{gen}$ ,  $R_L$ , or  $C_L$  is increased, there will be proportional increases in rise and/or fall times.



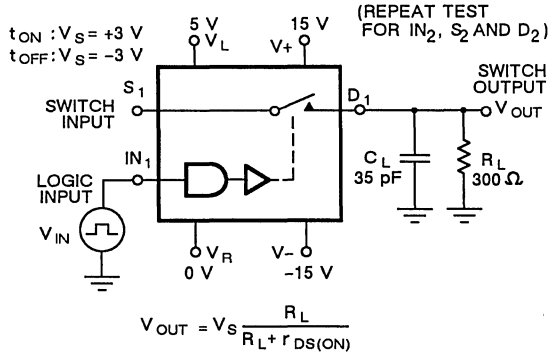


**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



(LOGIC "1" = SWITCH ON)



**APPLICATION HINTS\***

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>L</sub> Logic Supply Voltage (V)	V <sub>R</sub> Reference Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> Analog Voltage Range (V)
10 Ω and 30 Ω	15**	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
75 Ω	15**	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

\*\* Electrical Parameter Chart based on V+ = +15 V, V- = -15 V, V<sub>L</sub> = 5 V, V<sub>R</sub> = GND.

# DG186/187/188

## High-Speed Driver with SPDT JFET Switch

### FEATURES

- Constant ON Resistance over Entire Analog Range
- Low Leakage
- Low Crosstalk

### BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

### APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- D/A Ladder Switches

### DESCRIPTION

The DG186-188 are precision single-pole, double-throw (SPDT) analog switches designed to provide accurate switching of video and audio signals. This series, like the entire DG180 family, is ideally suited for applications requiring a constant ON resistance over the entire analog range.

The major design difference is the ON resistance, being 10, 30, and 75  $\Omega$  for the DG186, DG187, and DG188 respectively. Reduced switching errors are achieved through low leakage current ( $I_{S(OFF)} < 1$  nA for the DG187/188). Applications which benefit from flat ON resistance include audio switching, video switching, and sample-and-holds.

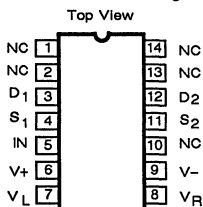
Each device comprises four N-channel JFET transistors and a bipolar driver (TTL compatible) to

achieve fast and accurate switch performance. The driver is designed to achieve break-before-make switching action, eliminating the inadvertent shorting between channels and the crosstalk which would result. In the ON state, each switch conducts current equally well in either direction. In the OFF condition, the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

Packaging for the DG186-188 includes a 14-pin side braze, flatpack, and 10-pin metal can options. Performance grades include both a military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature range. The flatpack option is only available in the military grade.

### PIN CONFIGURATION

Dual-In-Line Package

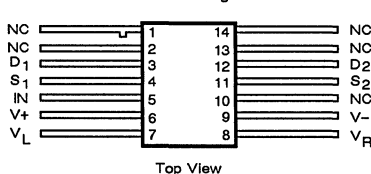


Order Numbers:

Side Braze:

DG186AP or DG186BP  
DG187AP or DG187BP  
DG188AP or DG188BP

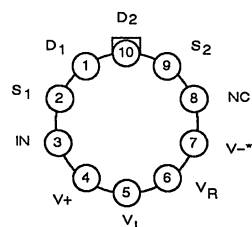
Flat Package



Order Numbers:

DG187AL/883 or DG188AL/883

Top View



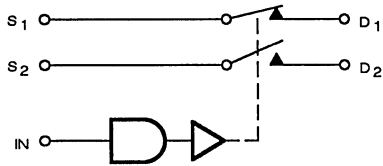
Metal Can Package

Order Numbers:

DG186AA or DG186BA  
DG187AA or DG187BA  
DG188AA or DG188BA

\*Common to Substrate and Case

## FUNCTIONAL BLOCK DIAGRAM



One SPDT Switch per Package

Truth Table\*

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.0$  V

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

$V_+$ to $V_-$ .....	36 V
$V_+$ to $V_D$ .....	33 V
$V_D$ to $V_-$ .....	33 V
$V_D$ to $V_S$ .....	$\pm 22$ V
$V_L$ to $V_-$ .....	36 V
$V_L$ to $V_{IN}$ .....	8 V
$V_L$ to $V_R$ .....	8 V
$V_{IN}$ to $V_R$ .....	8 V
$V_R$ to $V_-$ .....	27 V
$V_R$ to $V_{IN}$ .....	2 V
Current (S or D) DG186 .....	200 mA
Current (S or D) DG187, DG188 .....	30 mA

Current (All Other Pins) .....	30 mA
Storage Temperature .....	-65 to 150°C
Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C

### Power Dissipation\*

Metal Can** .....	450 mW
14-Pin DIP*** .....	825 mW
Flat Pack**** .....	900 mW

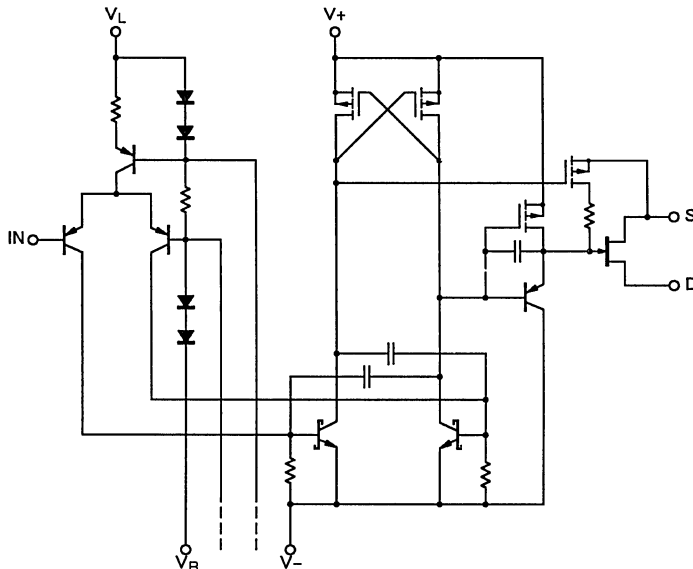
\* All leads welded or soldered to PC board.

\*\* Derate 6 mW/°C above 75°C.

\*\*\* Derate 11 mW/°C above 75°C.

\*\*\*\* Derate 10 mW/°C above 75°C.

## SCHEMATIC DIAGRAM (Typical Channel)



ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG186
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-7.5	15	-7.5	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>		V <sub>D</sub> = -7.5 V I <sub>S</sub> = -10 mA	1,3 2	7.5		10 20		15 25	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 0.8 V or 2.0 V <sup>e</sup>	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.05		10 1000		15 300	nA
			V <sub>S</sub> = 7.5 V V <sub>D</sub> = -7.5 V	1 2	0.05		10 1000		15 300	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.04		10 1000		15 300	
			V <sub>S</sub> = -7.5 V V <sub>D</sub> = 7.5 V	1 2	0.03		10 1000		15 300	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = -7.5 V	1 2	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I <sub>DSS</sub>	2 ms Pulse Duration		1	300					mA
<b>INPUT</b>										
Input Current with Input Voltage HIGH	I <sub>INH</sub>		V <sub>IN</sub> = 5 V	1 2	<0.01		10 20		10 20	μA
Input Current with Input Voltage LOW	I <sub>INL</sub>		V <sub>IN</sub> = 0 V	1,2,3	-30	-250		-250		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit		1	240		300		350	ns
Turn-OFF Time	t <sub>OFF</sub>			1	140		250		300	
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	1	21					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	1	17					
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	17					
OFF Isolation		f = 1 MHz, R <sub>L</sub> = 75 Ω		1	>55					dB

ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG186	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			2=125,85°C		-55 to 125°C		-25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 V or 5 V	1			0.8		0.8	mA
Negative Supply Current	I <sub>-</sub>		1		-3		-3		
Logic Supply Current	I <sub>L</sub>		1			3.2		3.2	
Reference Supply Current	I <sub>R</sub>		1		-2		-2		

ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG187	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			2=125,85°C		-55 to 125°C		-25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range	V <sub>ANALOG</sub>		1,2,3		-7.5	15	-7.5	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = -7.5 V I <sub>S</sub> = -10 mA	1,3 2	22		30 60		50 75	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.06		1 100		5 100	nA
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = 7.5 V V <sub>D</sub> = -7.5 V	1 2	0.13		1 100		5 100	
		V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.04		1 100		5 100	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = -7.5 V	1 2	-0.02	-2 -200		-10 -200		
<b>INPUT</b>									
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	1 2	<0.01		10 20		10 20	μA
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1,2,3	-30	-250		-250		

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ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG187
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1	85		150		180	ns	
Turn-OFF Time	t <sub>OFF</sub>		1	95		130		150		
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	1	9					pF	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>									V <sub>S</sub> = -5 V, I <sub>D</sub> = 0
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>									V <sub>D</sub> = -5 V, I <sub>S</sub> = 0
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V	1	14						
OFF Isolation		f = 1 MHz, R <sub>L</sub> = 75 Ω	1	>50					dB	
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> All = 0 V or 5 V	1			0.8		0.8	mA	
Negative Supply Current	I <sub>-</sub>		1		-3		-3			
Logic Supply Current	I <sub>L</sub>		1			3.2		3.2		
Reference Supply Current	I <sub>R</sub>		1		-2		-2			

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG188
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-10	15	-10	15	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = -10 V, V <sub>IN</sub> = 2.0 or 0.8 V <sup>e</sup> I <sub>S</sub> = -10 mA	1,3 2	35		75 150		100 150	Ω	

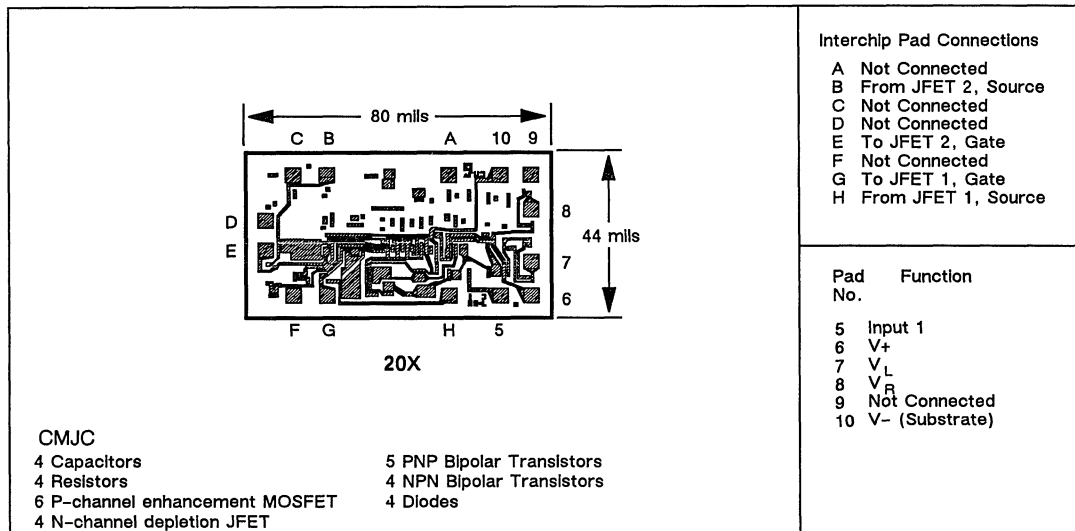
ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG188		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V				LIMITS						
						1=25°C		A SUFFIX		B SUFFIX		UNIT
						TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH (Cont'd)</b>												
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 0.8 V or 2.0 V <sup>a</sup>	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V	1	0.05		1		5	nA		
			V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	2		100		100				
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = 10 V	1	0.07		1		5			
			V <sub>D</sub> = -10 V	2		100		100				
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>		V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V	1	0.04		1		5			
			V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	2		100		100				
		V <sub>S</sub> = -10 V	1	0.05		1		5				
		V <sub>D</sub> = 10 V	2		100		100					
		V <sub>D</sub> = V <sub>S</sub> = -10 V	1	-0.03	-2		-10					
			2		-200		-200					
<b>INPUT</b>												
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	1	<0.01		10		10	μA			
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1,2,3	-30	-250		-250					
<b>DYNAMIC</b>												
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit		1	120		250		300	ns		
Turn-OFF Time	t <sub>OFF</sub>			1	100		130		150			
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	1	9				pF			
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	1	6							
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	14							
OFF Isolation		f = 1 MHz, R <sub>L</sub> = 75 Ω		1	>50				dB			
<b>SUPPLY</b>												
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 V or 5 V		1			0.8		0.8	mA		
Negative Supply Current	I <sub>-</sub>			1		-3		-3				
Logic Supply Current	I <sub>L</sub>			1			3.2		3.2			
Reference Supply Current	I <sub>R</sub>			1		-2		-2				

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

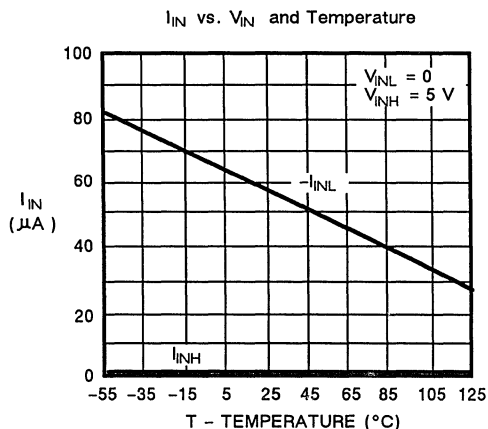
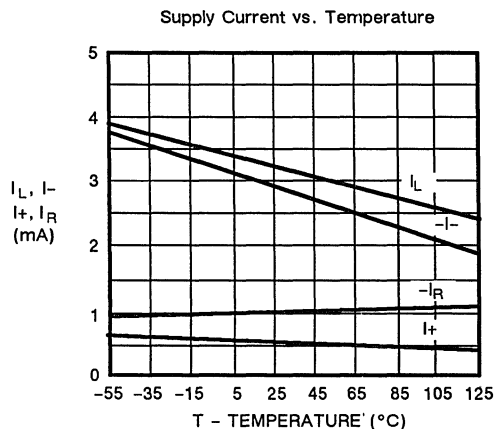
### NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- $V_{IN}$  = Input voltage to perform proper function.

## DIE TOPOGRAPHY (DRIVER)

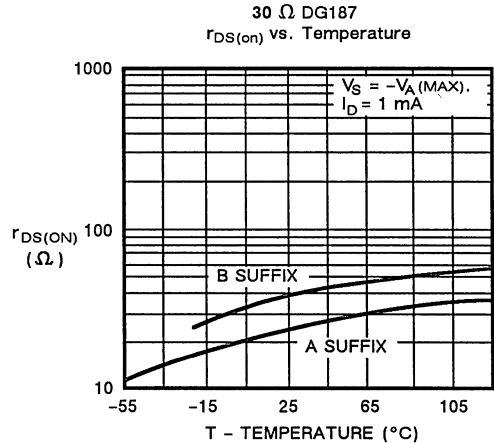
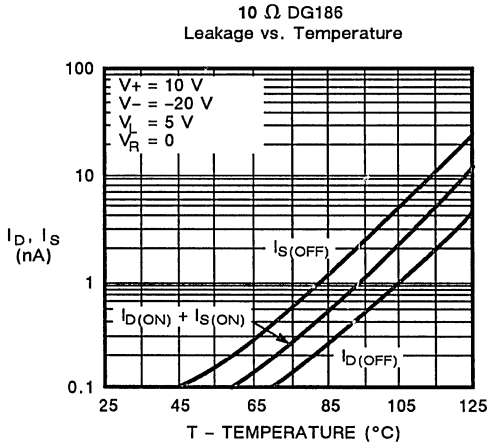
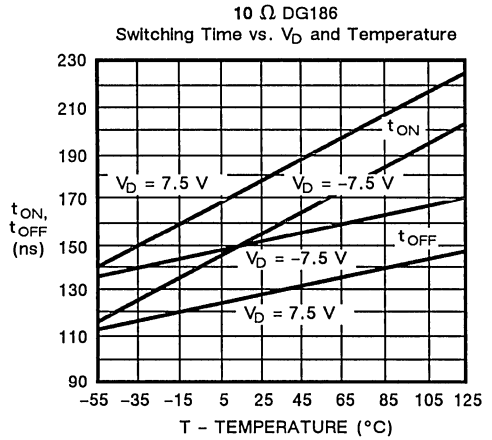
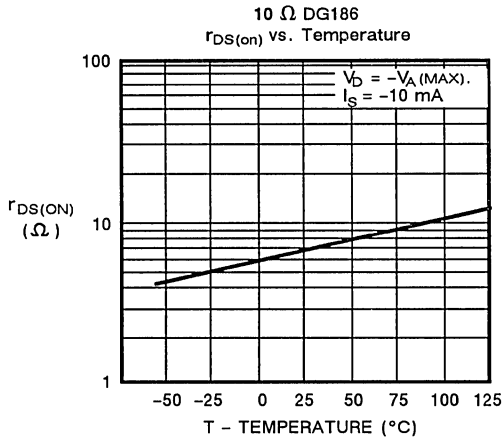


## TYPICAL CHARACTERISTICS

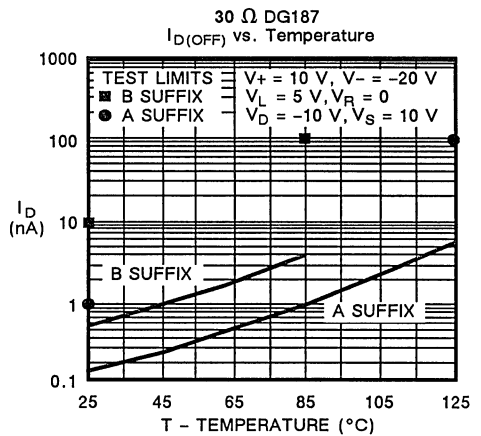
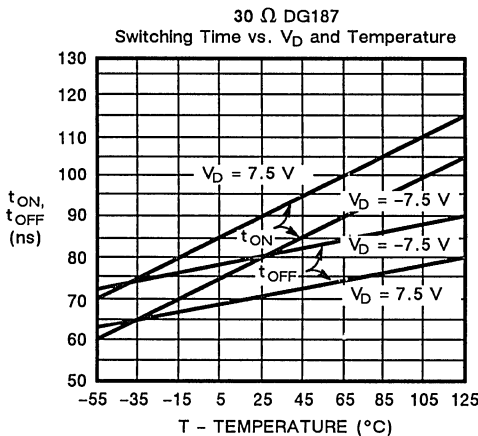




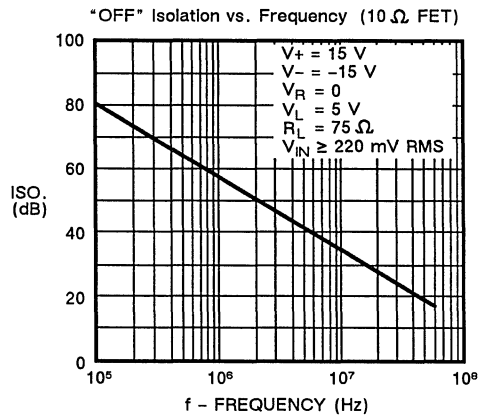
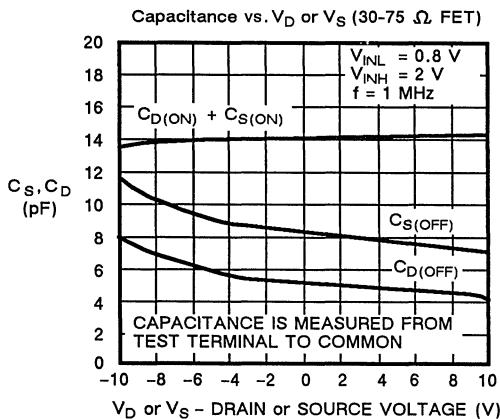
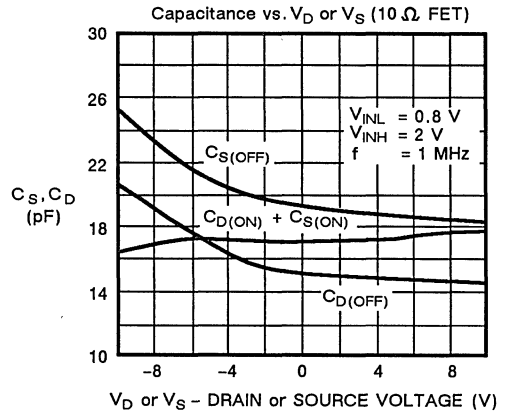
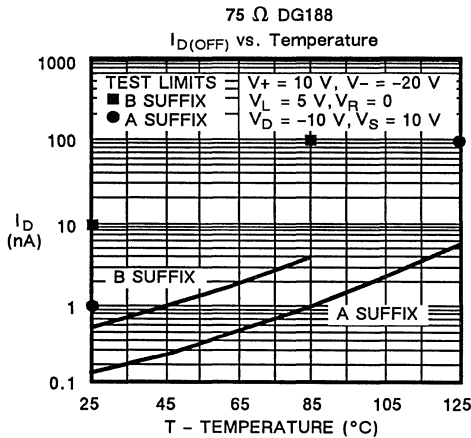
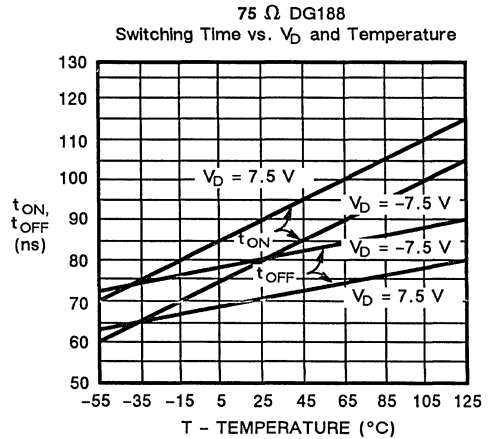
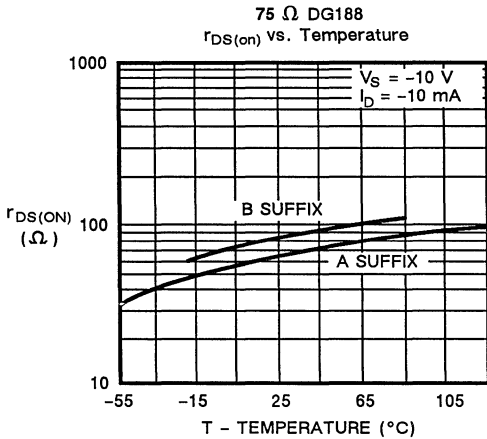
TYPICAL CHARACTERISTICS (Cont'd)



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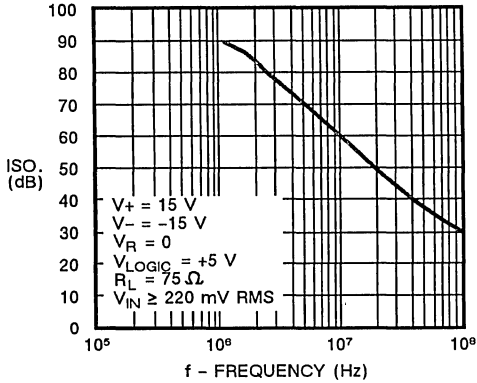


## TYPICAL CHARACTERISTICS (Cont'd)

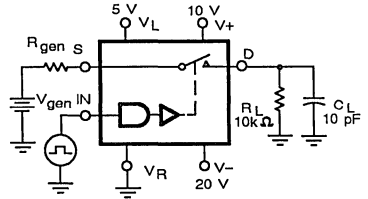


## TYPICAL CHARACTERISTICS (Cont'd)

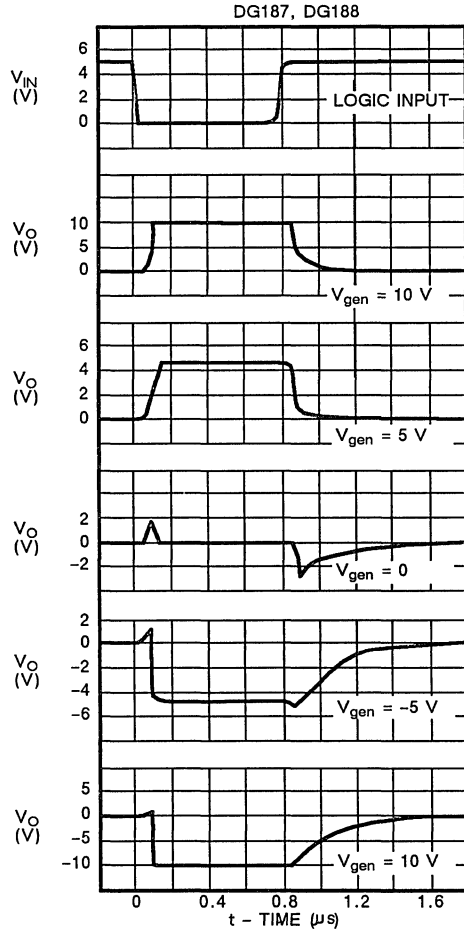
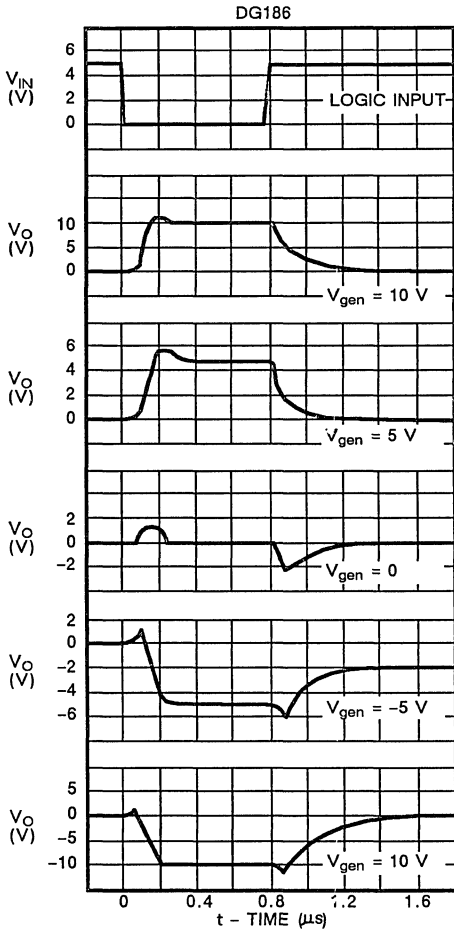
"OFF" Isolation vs. Frequency (30-75  $\Omega$  FET)



Typical delay, rise, fall, settling times, and switching transients in this circuit.

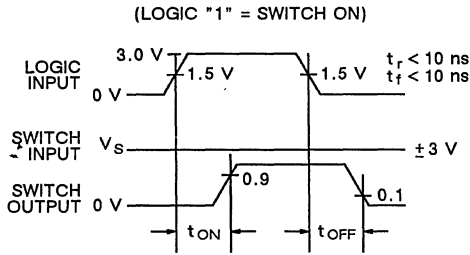


If  $R_{gen}$ ,  $R_L$ , or  $C_L$  is increased, there will be proportional increases in rise and/or fall times.

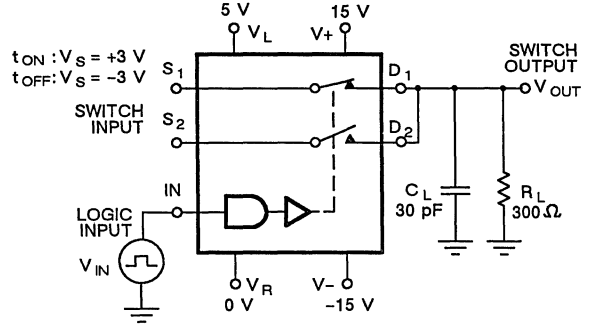


## SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



NOTE: LOGIC INPUT WAVEFORM IS INVERTED FOR SWITCHES THAT HAVE THE OPPOSITE LOGIC SENSE CONTROL.



$$V_{OUT} = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

## APPLICATION HINTS\*

Switch Family	$V_+$ Positive Supply Voltage (V)	$V_-$ Negative Supply Voltage (V)	$V_L$ Logic Supply Voltage (V)	$V_R$ Reference Supply Voltage (V)	$V_{IN}$ Logic Input Voltage $V_{INH} \text{ Min} / V_{INL} \text{ Max}$ (V)	$V_S$ Analog Voltage Range (V)
10 $\Omega$ and 30 $\Omega$	15**	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
75 $\Omega$	15**	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

\*\* Electrical Parameter Chart based on  $V_+ = 15 \text{ V}$ ,  $V_- = -15 \text{ V}$ ,  $V_L = 5 \text{ V}$ ,  $V_R = \text{GND}$ .

# DG189/190/191

## High-Speed Driver with Dual SPDT JFET Switches

### FEATURES

- Constant ON Resistance over Entire Analog Range
- Low Leakage
- Low Crosstalk

### BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

### APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- D/A Ladder Switches

### DESCRIPTION

The DG189-191 are precision dual single-pole, double-throw (SPDT) analog switches designed to provide accurate switching of video and audio signals. This series, like the entire DG180 family, is ideally suited for applications requiring a constant ON resistance over the entire analog range.

The major design difference is the ON resistance, being 10, 30, and 75  $\Omega$  for the DG189, DG190, and DG191 respectively. Reduced switching errors are achieved through low leakage current ( $I_{S(OFF)} < 1 \text{ nA}$  for the DG190/191). Applications which benefit from flat ON resistance include audio switching, video switching, and sample and holds.

Each device comprises four N-channel JFET transistors and a bipolar driver (TTL compatible) to

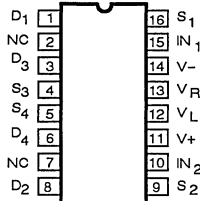
achieve fast and accurate switch performance. The driver is designed to achieve break-before-make switching action, eliminating the inadvertent shorting between channels and the crosstalk which would result. In the ON state, each switch conducts current equally well in either direction. In the OFF condition, the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

Packaging options for the DG189-191 include the 16-pin side braze, and the 14-pin flatpack. The flatpack version is only available for the DG190/191. Performance grades include both the military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature ranges. The flatpack option is only available in the military grade.

**5**

### PIN CONFIGURATION

Dual-In-Line Package  
Top View

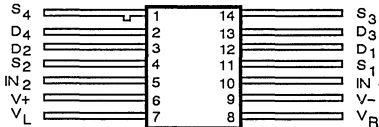


Order Numbers:

Side Braze:

DG189AP or DG189BP  
DG190AP or DG190BP  
DG191AP or DG191BP

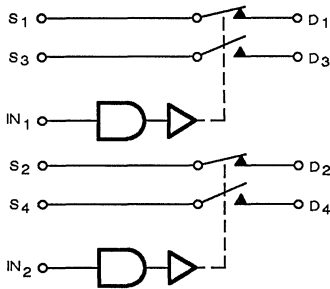
Flat Package  
Top View



Order Numbers:

DG190AL/883 or DG191AL/883

## FUNCTIONAL BLOCK DIAGRAM



Two SPDT Switches per Package\*

Truth Table

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Logic "0" < 0.8 V  
Logic "1" > 2.0 V

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

V <sub>+</sub> to V <sub>-</sub>	36 V
V <sub>+</sub> to V <sub>D</sub>	33 V
V <sub>D</sub> to V <sub>-</sub>	33 V
V <sub>D</sub> to V <sub>S</sub>	±22 V
V <sub>L</sub> to V <sub>-</sub>	36 V
V <sub>L</sub> to V <sub>IN</sub>	8 V
V <sub>L</sub> to V <sub>R</sub>	8 V
V <sub>IN</sub> to V <sub>R</sub>	8 V
V <sub>R</sub> to V <sub>-</sub>	27 V
V <sub>R</sub> to V <sub>IN</sub>	2 V
Current (S or D) DG189	200 mA

Current (S or D) DG190, DG191	30 mA
Current (All Other Pins)	30 mA
Storage Temperature	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C

### Power Dissipation\*

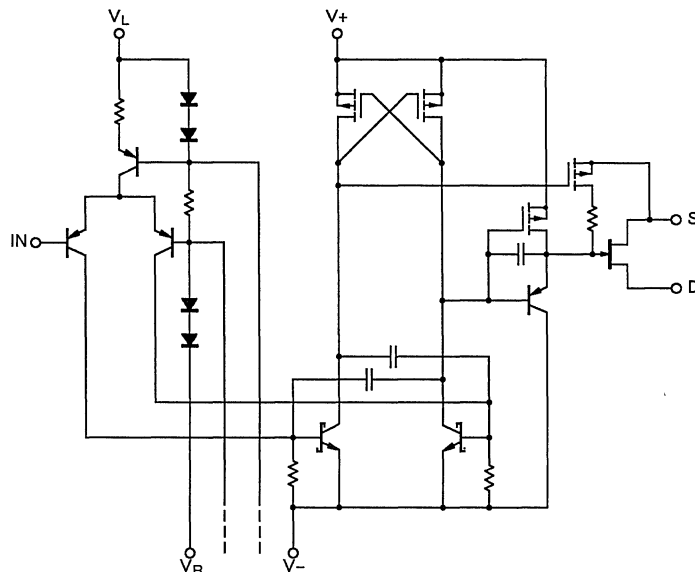
16-Pin DIP**	900 mW
14-Pin Flat Pack***	900 mW

\* All leads welded or soldered to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 10 mW/°C above 75°C.

## SCHEMATIC DIAGRAM (Typical Channel)



ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG189
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-7.5	15	-7.5	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>		V <sub>D</sub> = -7.5 V I <sub>S</sub> = -10 mA	1,3 2	7.5		10 20		15 25	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 0.8 V or 2.0 V <sup>e</sup>	V <sub>S</sub> = 10 V, V <sub>D</sub> = -10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.05		10 1000		15 300	nA
			V <sub>S</sub> = 7.5 V V <sub>D</sub> = -7.5 V	1 2	0.05		10 1000		15 300	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = -10 V, V <sub>D</sub> = 10 V V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V	1 2	0.04		10 1000		15 300	
			V <sub>S</sub> = -7.5 V V <sub>D</sub> = 7.5 V	1 2	0.03		10 1000		15 300	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = -7.5 V	1 2	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I <sub>DSS</sub>	2 ms Pulse Duration		1	300					mA
<b>INPUT</b>										
Input Current with Input Voltage HIGH	I <sub>INH</sub>		V <sub>IN</sub> = 5 V	1 2	<0.01		10 20		10 20	μA
Input Current with Input Voltage LOW	I <sub>INL</sub>		V <sub>IN</sub> = 0 V	1,2,3	-30	-250		-250		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>		See Switching Time Test Circuit	1	240		300		350	ns
Turn-OFF Time	t <sub>OFF</sub>			1	140		250		300	
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	V <sub>S</sub> = -5 V, I <sub>D</sub> = 0	1	21					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		V <sub>D</sub> = -5 V, I <sub>S</sub> = 0	1	17					
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 0 V	1	17					
OFF Isolation			f = 1 MHz, R <sub>L</sub> = 75 Ω	1	>55					dB

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG189
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ $V_R = 0\text{ V}$		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
SUPPLY										
Positive Supply Current	$I_+$	$V_{IN(All)} = 0\text{ V or }5\text{ V}$		1	0.6		1.5		1.5	mA
Negative Supply Current	$I_-$			1	-2.7	-5		-5		
Logic Supply Current	$I_L$			1	3.1		4.5		4.5	
Reference Supply Current	$I_R$			1	-1	-2		-2		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG190
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ $V_R = 0\text{ V}$		LIMITS						UNIT
				1=25°C		A SUFFIX		B SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
SWITCH										
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$			1,2,3		-7.5	15	-7.5	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$V_D = -7.5\text{ V}$ $I_S = -10\text{ mA}$		1,3 2	18		30 60		50 75	$\Omega$
Source OFF Leakage Current	$I_{S(OFF)}$	$V_S = 10\text{ V}, V_D = -10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$		1 2	0.06		1 100		5 100	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_S = 7.5\text{ V}$ $V_D = -7.5\text{ V}$		1 2	0.1		1 100		5 100	
		$V_S = -10\text{ V}, V_D = 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$		1 2	0.05		1 100		5 100	
Channel ON Leakage Current	$I_{D(ON)+}$ $I_{S(ON)}$	$V_D = V_S = -7.5\text{ V}$		1 2	-0.02	-2 -200		-10 -200		
INPUT										
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 5\text{ V}$		1 2	<0.01		10 20		10 20	$\mu\text{A}$
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0\text{ V}$		1,2,3	-30	-250		-250		



ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG190		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1	85		150		180	ns	
Turn-OFF Time	t <sub>OFF</sub>		1	95		130		150		
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	1	9					pF	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>									V <sub>S</sub> = -5 V, I <sub>D</sub> = 0
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>									V <sub>D</sub> = -5 V, I <sub>S</sub> = 0
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V	1	14						
OFF Isolation		f = 1 MHz, R <sub>L</sub> = 75 Ω	1	>50					dB	
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> (All) = 0 V or 5 V	1	0.6		1.5		1.5	mA	
Negative Supply Current	I <sub>-</sub>		1	-2.7	-5		-5			
Logic Supply Current	I <sub>L</sub>		1	3.1		4.5		4.5		
Reference Supply Current	I <sub>R</sub>		1	-1	-2		-2			

5

ELECTRICAL CHARACTERISTICS <sup>a</sup>								DG191	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V V <sub>R</sub> = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-10	15	-10	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = -10 V, V <sub>IN</sub> = 2.0 or 0.8 V <sup>e</sup> I <sub>S</sub> = -10 mA	1,3 2	35		75 150		100 150	Ω

ELECTRICAL CHARACTERISTICS <sup>a</sup>										DG191		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:				LIMITS						
		$V_+ = 15\text{ V}$ $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ $V_R = 0\text{ V}$				1=25°C		A SUFFIX		B SUFFIX		UNIT
						2=125, 85°C		-55 to 125°C		-25 to 85°C		
		TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>					
<b>SWITCH (Cont'd)</b>												
Source OFF Leakage Current	$I_{S(OFF)}$	$V_{IN} = 0.8\text{ V}$ or $2.0\text{ V}^e$	$V_S = 10\text{ V}, V_D = -10\text{ V}$	1	0.05		1		5	nA		
			$V_+ = 10\text{ V}, V_- = -20\text{ V}$	2		100		100				
Drain OFF Leakage Current	$I_{D(OFF)}$		$V_S = 10\text{ V}$ $V_D = -10\text{ V}$	1	0.07		1		5			
			$V_S = -10\text{ V}, V_D = 10\text{ V}$ $V_+ = 10\text{ V}, V_- = -20\text{ V}$	2		100		100				
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$		$V_S = -10\text{ V}$ $V_D = 10\text{ V}$	1	0.04		1		5			
			$V_S = -10\text{ V}$ $V_D = 10\text{ V}$	2	0.05		1		5			
		$V_D = V_S = -10\text{ V}$	1	-0.03	-2		-10					
			2		-200		-200					
<b>INPUT</b>												
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = 5\text{ V}$	1	<0.01		10		10	μA			
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0\text{ V}$	2		20		20					
			1,2,3	-35	-250		-250					
<b>DYNAMIC</b>												
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit	1	120		250		300	ns			
Turn-OFF Time	$t_{OFF}$		1	100		130		150				
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	$V_S = -5\text{ V}, I_D = 0$	1	9				pF			
Drain-OFF Capacitance	$C_{D(OFF)}$		$V_D = -5\text{ V}, I_S = 0$	1	6							
Channel ON Capacitance	$C_{D(ON)} + C_{S(ON)}$		$V_D = V_S = 0\text{ V}$	1	14							
OFF Isolation		f = 1 MHz, $R_L = 75\ \Omega$	1	>50					dB			
<b>SUPPLY</b>												
Positive Supply Current	$I_+$	$V_{IN} (\text{All}) = 0\text{ V or } 5\text{ V}$	1	0.6		1.5		1.5	mA			
Negative Supply Current	$I_-$		1	-2.7	-5		-5					
Logic Supply Current	$I_L$		1	3.1		4.5		4.5				
Reference Supply Current	$I_R$		1	-1	-2		-2					

**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e.  $V_{IN}$  = Input voltage to perform function.

**DIE TOPOGRAPHY (DRIVER)**

20X

**Interchip Pad Connections**

With 2 JFET's

- A No Connection
- B No connection
- C To JFET 2, Gate
- D From JFET 2, Source
- E From JFET 1, Source
- F To JFET 1, Gate
- G No Connection
- H No Connection

With 4 JFET's

- A From JFET 1, Source
- B To JFET 1, Gate
- C To JFET 3, Gate
- D From JFET 3, Source
- E From JFET 4, Gate
- F To JFET 4, Gate
- G To JFET 2, Gate
- H From JFET 2, Source

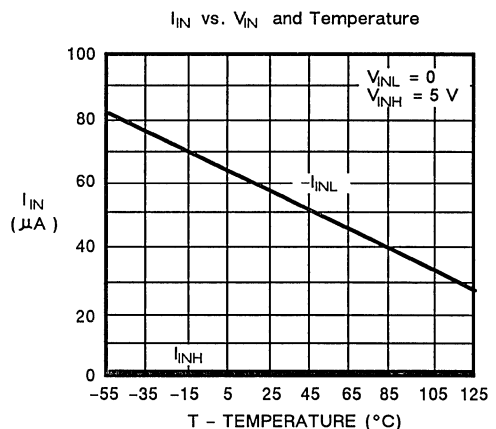
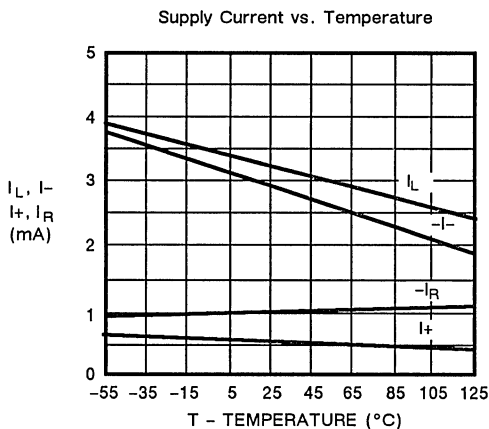
Pad No.	Function
10	Input 2
11	V+
12	V <sub>L</sub>
13	V <sub>R</sub>
14	V- (Substrate)
15	Input 1

**CMJB**

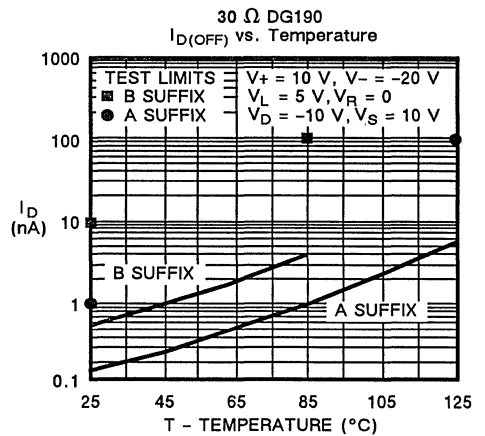
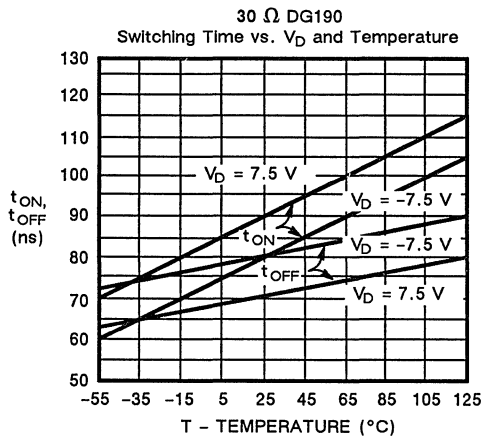
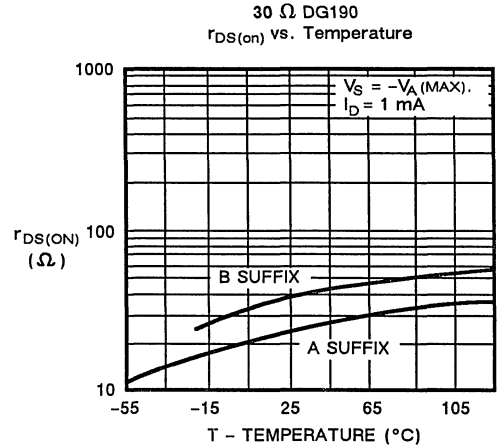
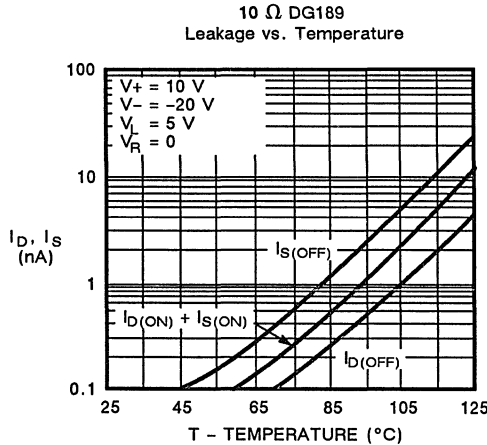
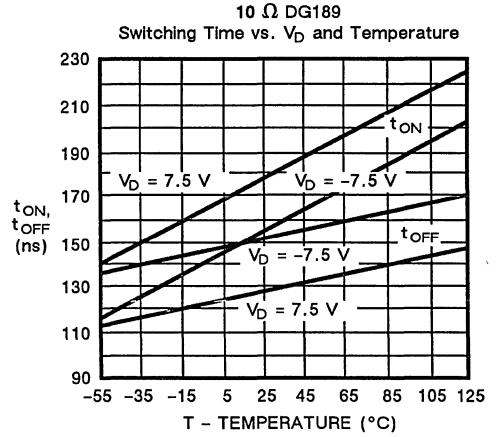
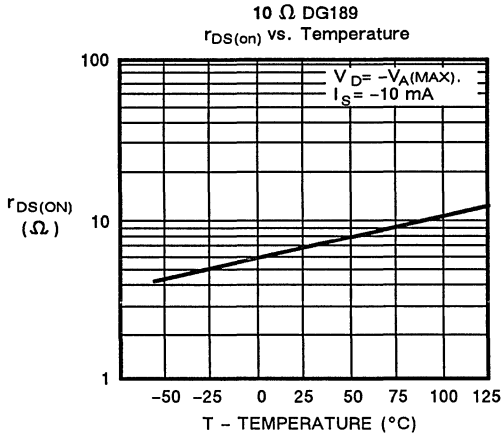
8 Capacitors	10 PNP Bipolar Transistors
7 Resistors	4 NPN Bipolar Transistors
12 P-channel enhancement MOSFET	4 Diodes
4 N-channel depletion JFET	

5

**TYPICAL CHARACTERISTICS**

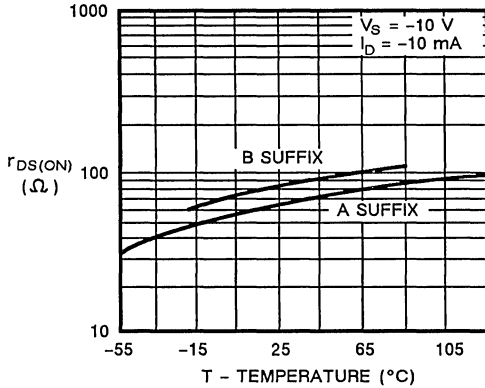


## TYPICAL CHARACTERISTICS (Cont'd)

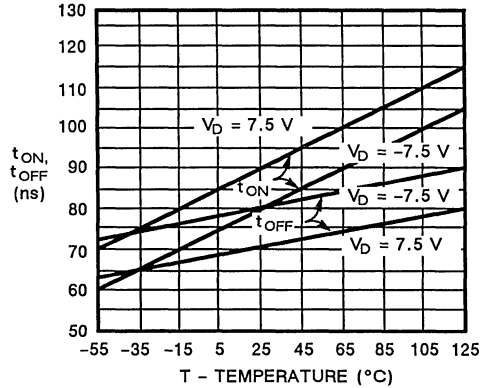


## TYPICAL CHARACTERISTICS (Cont'd)

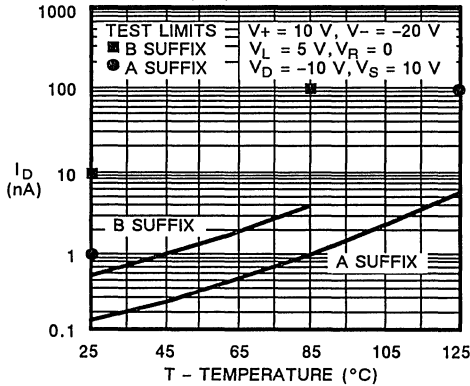
75 Ω DG191  
 $r_{DS(on)}$  vs. Temperature



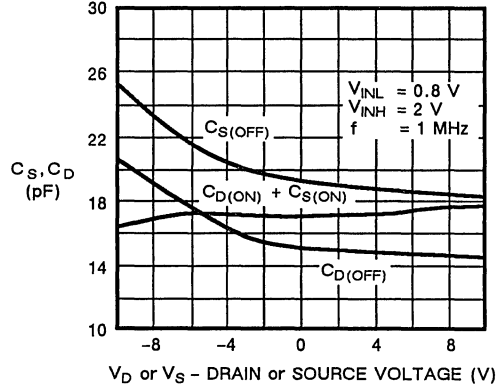
75 Ω DG191  
Switching Time vs.  $V_D$  and Temperature



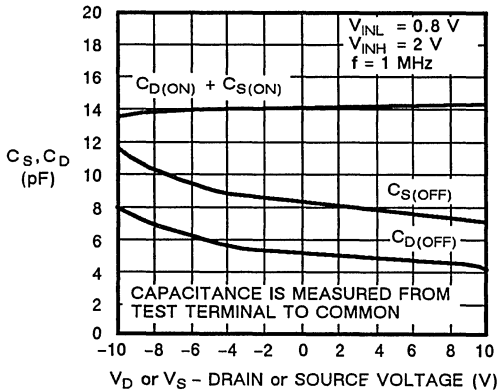
75 Ω DG191  
 $I_{D(OFF)}$  vs. Temperature



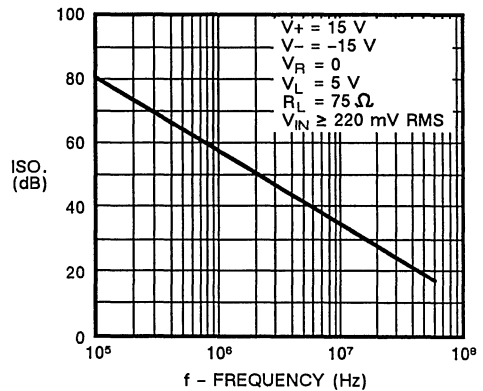
Capacitance vs.  $V_D$  or  $V_S$  (10 Ω FET)



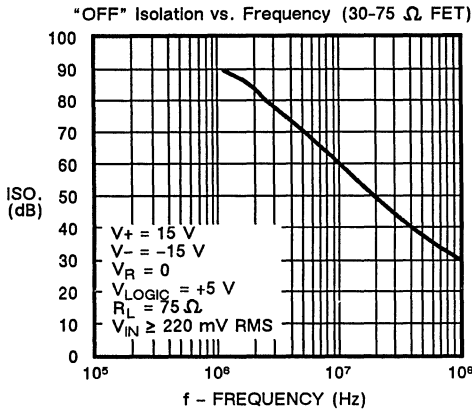
Capacitance vs.  $V_D$  or  $V_S$  (30-75 Ω FET)



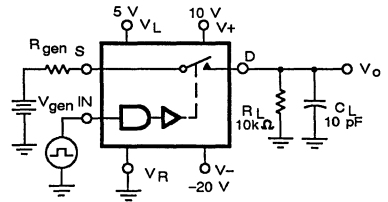
"OFF" Isolation vs. Frequency (10 Ω FET)



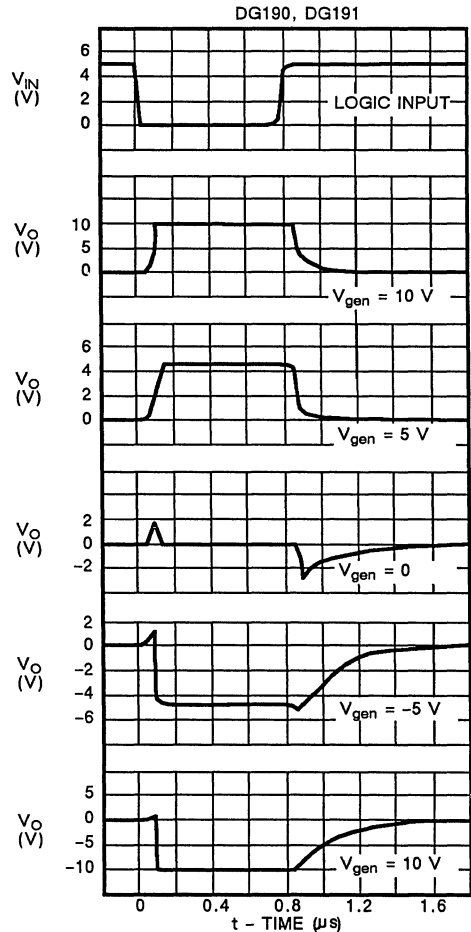
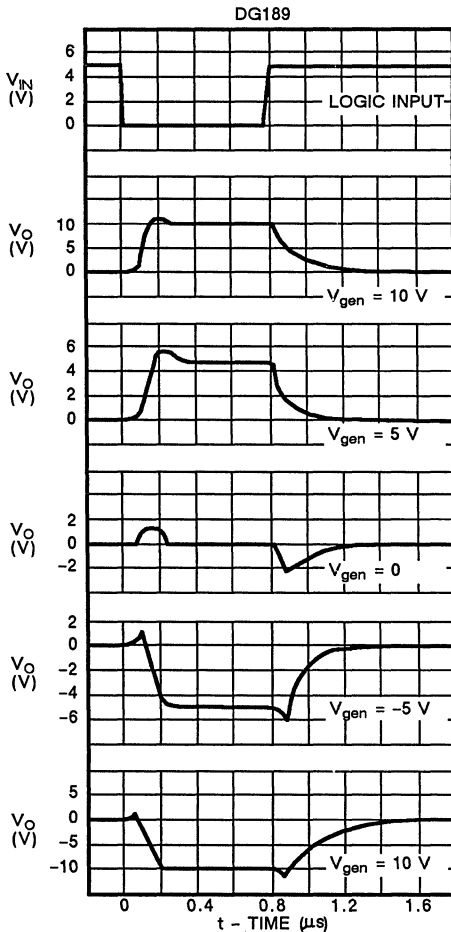
## TYPICAL CHARACTERISTICS (Cont'd)



Typical delay, rise, fall, settling times, and switching transients in this circuit.

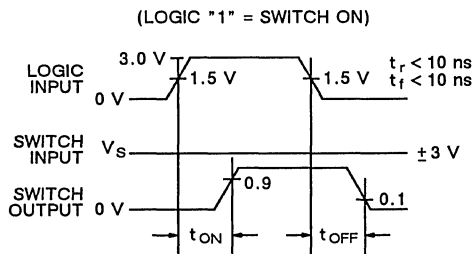


If  $R_{\text{gen}}$ ,  $R_L$ , or  $C_L$  is increased, there will be proportional increases in rise and/or fall times.

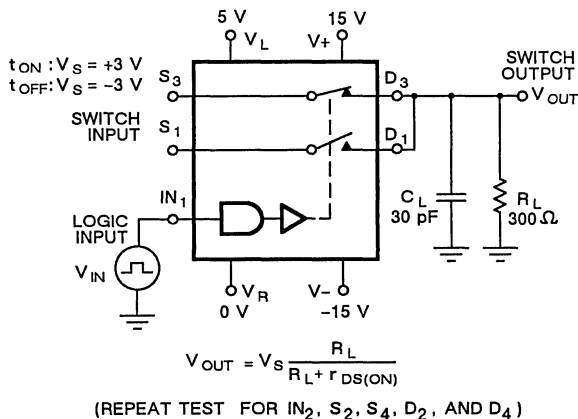


## SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



NOTE: LOGIC INPUT WAVEFORM IS INVERTED FOR SWITCHES THAT HAVE THE OPPOSITE LOGIC SENSE CONTROL.



## APPLICATION HINTS\*

**5**

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	VL Logic Supply Voltage (V)	VR Reference Supply Voltage (V)	VIN Logic Input Voltage VINH Min/ VINL Max (V)	VS Analog Voltage Range (V)
10 Ω and 30 Ω	15**	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
75 Ω	15**	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

\*\* Electrical Parameter Chart based on  $V_+ = 15 \text{ V}$ ,  $V_- = -15 \text{ V}$ ,  $V_L = 5 \text{ V}$ ,  $V_R = \text{GND}$ .

## Dual Monolithic SPST CMOS Analog Switch

### FEATURES

- $\pm 15$  V Input Signal Range
- 44 Volt Maximum Supply Ratings
- ON Resistance < 70  $\Omega$
- TTL and CMOS Compatibility
- Static Protected Logic Inputs

### BENEFITS

- Wide Dynamic Capabilities
- Higher Power Supply Tolerance
- Simple Interfacing
- Reduced External Component Count

### APPLICATIONS

- Servo Control Switching
- Programmable Gain Amplifiers
- Integration Reset Switching

### DESCRIPTION

The DG200A is a dual, single-pole, single-throw analog switch designed to provide general purpose switching of analog signals. This device is ideally suited for designs requiring a wide analog voltage range coupled with low ON resistance.

The DG200A is designed on Siliconix' PLUS-40 CMOS process to achieve a high voltage rating and superior switch performance. An epitaxial layer prevents latchup.

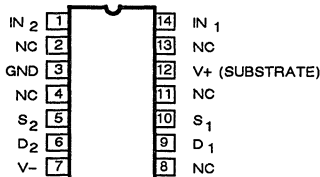
Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. In the ON condition, this bi-directional switch introduces no offset voltage of its own.

Packaging for the DG200A include a 14-pin CerDIP, metal can, and plastic DIP options. Performance grades include military, A suffix (-55 to 125°C), industrial, B suffix (-25 to 85°C), and commercial, C suffix (0 to 70°C) temperature ranges.

### PIN CONFIGURATION

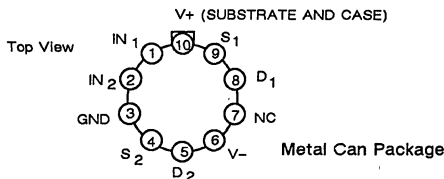
### FUNCTIONAL BLOCK DIAGRAM

Dual-In-Line Package



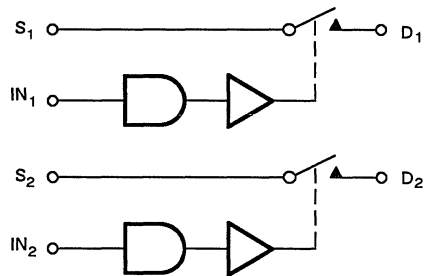
Top View  
Order Numbers:

CerDIP: DG200AAK, DG200AAK/883  
DG200ABK, DG200ACK  
Plastic: DG200ACJ



Order Numbers:

DG200AAA, DG200AAA/883  
DG200ABA, DG200ACA



Two SPST Switches per Package\*

TRUTH TABLE

LOGIC	SWITCH
0	ON
1	OFF

LOGIC "0"  $\leq 0.8$  V  
LOGIC "1"  $\geq 2.4$  V

\* Switches Shown for Logic "1" Input



**ABSOLUTE MAXIMUM RATINGS**

V<sub>+</sub> to V<sub>-</sub> ..... 44 V  
 GND to V<sub>-</sub> ..... 25 V  
 Digital Inputs<sup>1</sup>, V<sub>S</sub>, V<sub>D</sub> ..... (V<sub>-</sub>) -2 V to (V<sub>+</sub>) +2 V or  
 ..... 30 mA, whichever occurs first.  
 Current (Any Terminal) Continuous ..... 30 mA  
 Current S or D  
 (Pulsed at 1 ms, 10% Duty Cycle Max) ..... 100 mA  
 Operating Temperature (A Suffix) ..... -55 to 125°C  
 (B Suffix) ..... -25 to 85°C  
 (C Suffix) ..... 0 to 70°C

Storage Temperature (A & B Suffix) ..... -65 to 150°C  
 (C Suffix) ..... -65 to 125°C

Power Dissipation (Package)\*  
 Metal Can\*\* ..... 450 mW  
 14-Pin Ceramic DIP\*\*\* ..... 825 mW  
 14-Pin Plastic DIP\*\*\*\* ..... 470 mW

- \* All leads soldered or welded to PC board.
- \*\* Derate 6 mW/°C above 75°C.
- \*\*\* Derate 11 mW/°C above 75°C.
- \*\*\*\* Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = V	LIMITS						UNIT
			1=25°C		A SUFFIX		B,C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = ±10 V, V <sub>IN</sub> = 0.8 V I <sub>S</sub> = -1 mA	1,3 2	45		70 100		80 100	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.4 V	1 2	0.01		2 100		5 100	nA
		V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	-0.02	-2 -100		-5 -100		
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>D</sub> = 14 V V <sub>S</sub> = -14 V	1 2	0.01		2 100		5 100	
		V <sub>D</sub> = -14 V V <sub>S</sub> = 14 V	1 2	-0.02	-2 -100		-5 -100		
Channel ON Leakage Current <sup>f</sup>	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V, V <sub>IN</sub> = 0.8 V	1 2	0.1		2 200		5 200	
		V <sub>S</sub> = V <sub>D</sub> = -14 V, V <sub>IN</sub> = 0.8 V	1 2	-0.1	-2 -200		-5 -200		
<b>INPUT</b>									
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 2.4 V	1 2	0.0009	-0.5 -1		-1 -10		μA
		V <sub>IN</sub> = 15 V	1 2	0.005		.5 1		1 10	
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1 2	-0.0015	-0.5 -1		-1 -10		

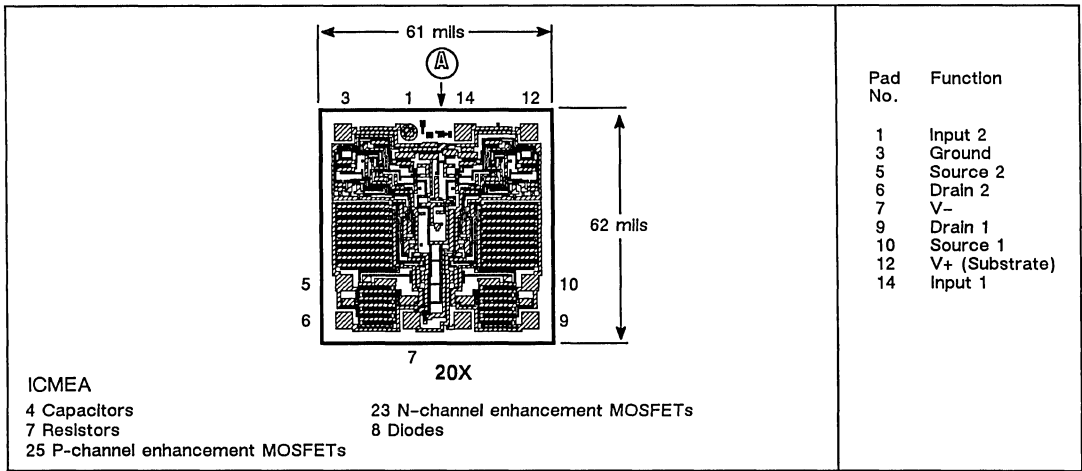
**5**

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		B,C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1	440		1000		1000	ns
Turn-OFF Time	t <sub>OFF</sub>		1	340		425		425	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>gen</sub> = 0 V R <sub>gen</sub> = 0 Ω	1	-10					pC
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V, V <sub>IN</sub> = 5 V f = 140 kHz	1	9					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0 V, V <sub>IN</sub> = 5 V f = 140 kHz	1	9					
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V V <sub>IN</sub> = 0 V	1	25					
OFF Isolation <sup>e</sup>		V <sub>IN</sub> = 5 V, Z <sub>L</sub> = 75 Ω V <sub>S</sub> = 2 V, f = 1 MHz	1	75					dB
Crosstalk (Channel-to-Channel)			1	90					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	Both Channels ON or OFF V <sub>IN</sub> = 0 V and 2.4 V	1	0.8		2		2	mA
Negative Supply Current	I <sub>-</sub>		1	-0.23	-1		-1		

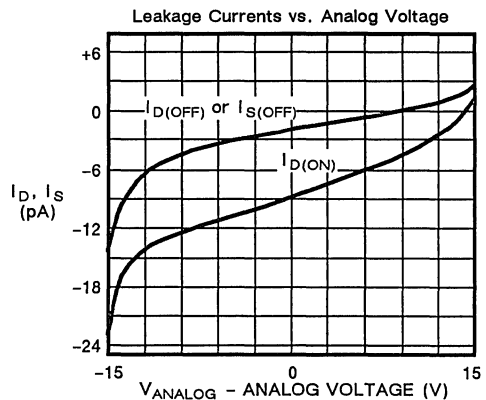
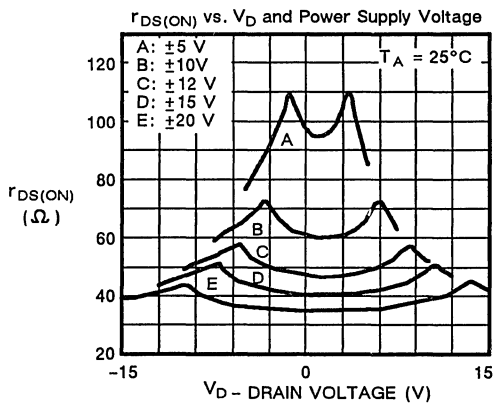
**NOTES:**

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- OFF Isolation Δ 20 log V<sub>S</sub>/V<sub>D</sub>, V<sub>S</sub> = input to OFF switch, V<sub>D</sub> = output.
- I<sub>D(ON)</sub> is leakage from driver into "ON" switch.

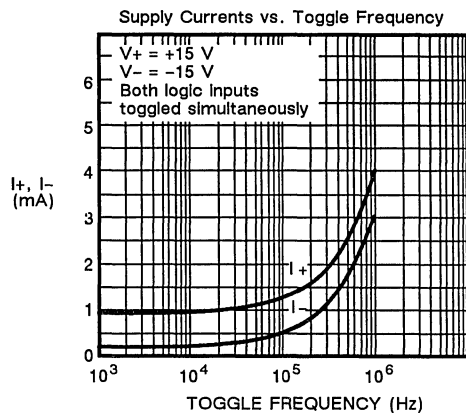
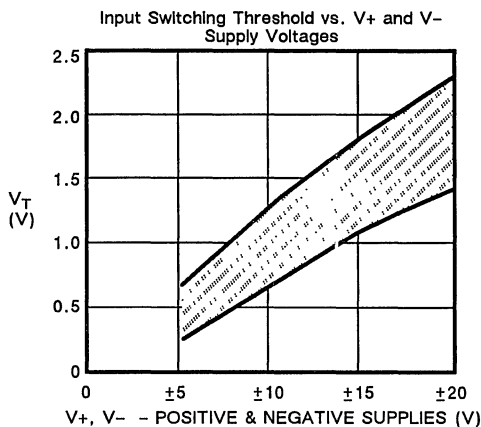
**DIE TOPOGRAPHY**



**TYPICAL CHARACTERISTICS**

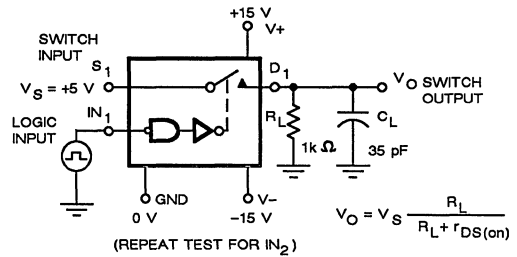
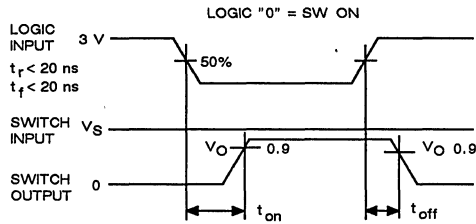


**5**

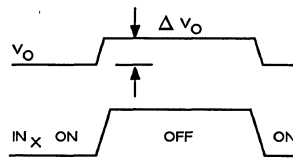
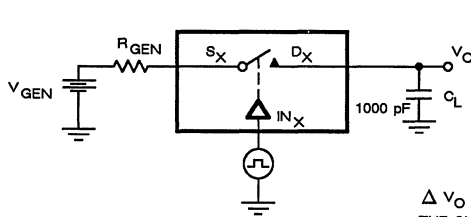


## SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

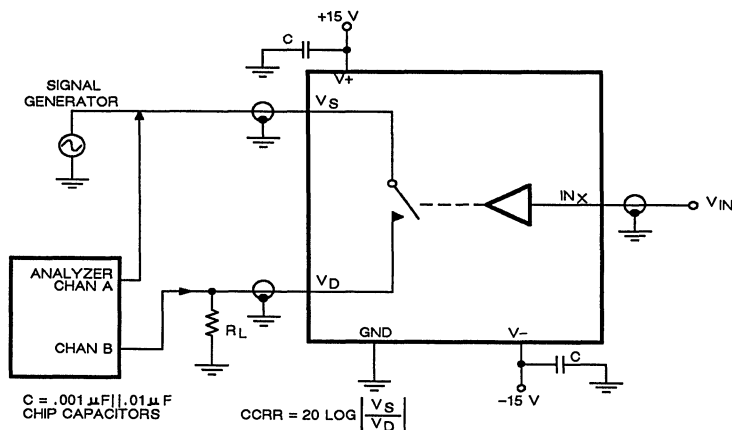


## CHARGE INJECTION TEST CIRCUIT

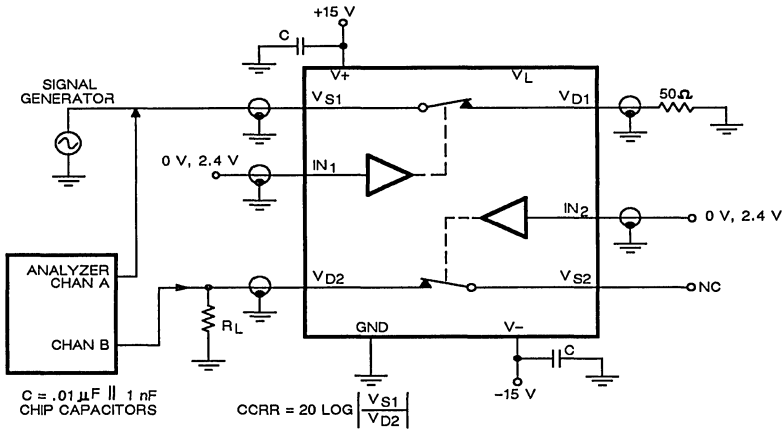


$\Delta V_O = \text{MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION}$   
 THE CHARGE INJECTION IN COULOMBS IS  $\Delta Q = C_L \times \Delta V_O$

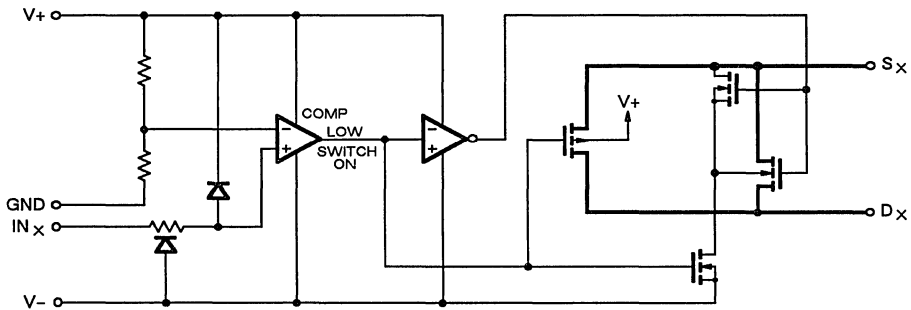
## OFF ISOLATION TEST CIRCUIT



**CHANNEL-TO-CHANNEL CROSSTALK TEST CIRCUIT**



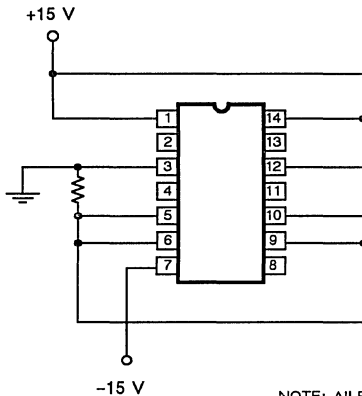
**SCHEMATIC DIAGRAM (Typical Channel)**



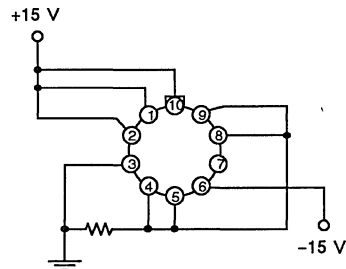
**5**

**BURN-IN DIAGRAMS**

Dual-In-Line Packages



Metal Can Package



NOTE: All Resistors are 10 kΩ unless otherwise specified.

## Precision Monolithic Quad SPST CMOS Analog Switch

### FEATURES

- $\pm 22$  Volt Input Range
- $10 \Omega$  Max  $\Delta r_{DS(ON)}$   
Any Combination Of Switches
- 0.25 nA Max At 25°C,  
 $\pm 15$  V
- 50 pC Max Charge Transfer Error
- Tested  $\Delta t_{ON}$  and  $\Delta t_{OFF} \leq 50$  ns

### BENEFITS

- Fully Tested Around  $\pm 10.8$ ,  $\pm 16.5$  and  $\pm 22$  V Supplies
- Pin Compatible With DG201A – Simplifies Upgrades
- Simplifies Worst Case Analysis
- TTL Compatible

### APPLICATIONS

- Precision Data Acquisition
- Automatic Test Equipment
- Radar Systems

### DESCRIPTION

The DGP201A is a precision quad single-pole single-throw analog switch designed for critical applications requiring improved performance over that obtainable with the popular DG201A. Produced on an enhanced proprietary high voltage process, the DGP201A has been fully specified with input analog signals to  $\pm 22$  V making it an ideal choice for high voltage applications or where the added margin of safety over traditional switches is of importance.

In addition to the low current leakage specifications, charge injection,  $\Delta r_{DS(ON)}$ ,  $\Delta t_{ON}$  and  $\Delta t_{OFF}$  have been tested and guaranteed at various input voltages to assure worst case error analysis. An epitaxial layer prevents latchup.

Packaging for this device includes a 16-Pin CerDIP, plastic, and small outline options. Performance grades include military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ) temperature ranges. Additionally, LCC packaging is available.

### PIN CONFIGURATION AND FUNCTION BLOCK DIAGRAM

#### Four SPST Switches per Package

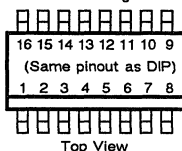
Truth Table

LOGIC	SWITCH
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V

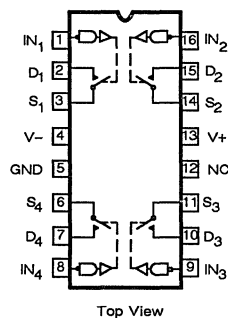
Logic "1"  $\geq 2.4$  V

SO Package



Order Number:  
DGP201ADY

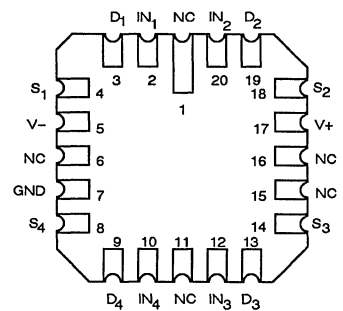
Dual-in-Line Package



Top View

Order Numbers:  
CerDIP: DGP201AAK  
DGP201AAK/883  
Plastic: DGP201ADJ

Leadless Chip Carrier



Top View

Order Number:  
DGP201AAZ/883

## THE DGP FAMILY OF ANALOG SWITCHES AND MULTIPLEXERS

Siliconix has improved its high voltage metal gate CMOS process to allow for lower variation performance. Additionally, through dramatic improvements in automated testing technology, specifications and limits that were previously untestable are now 100% tested and specified on the DGP201A data sheet.

The data sheet specification tables are in a new format as well. The format is that of a military drawing, where all specifications are 100% tested, eliminating any uncertainty about what is actually tested. Many parameters that were previously listed as "typical" or "guaranteed by design" are now 100% tested with minimum and maximum values, so that a worst case design can be realized.

For example, charge transfer error (or charge injection) was listed only as a typical value in the DG201A data sheet, and no maximum value was guaranteed. A maximum limit of 50 pico Coulombs has been established on the data sheet, and this value is 100% tested. This allows the design engineer to design precision switching circuits, such as sample-and-hold amplifiers, with fixed limits for the charge compensation circuit.

The DGP201A also specifies certain parameters that have never been seen on a DG201A standard product data sheet in min/max or typical form. An

important example of this is the variation of the switching time over all channels, which is specified with a maximum of 50 ns. The variation of "ON" resistance is similarly specified and 100% tested to be less than 10 ohms over six different drain voltage and source current conditions, over all four channels tested, resulting in 24 different readings. This specification is necessary for determining the worst-case distortion and signal level variation due to differences in channel resistance and ON resistance modulation effects.

Leakage currents are specified and tested to new lower limits at both room temperature and over the full temperature range. For example, the industrial range devices' leakages have been reduced from 100 nA (over temp) on the DG201A to 1 nA (over temp) on the DGP version. Additionally, the leakages are specified at the extremes of the operating ranges (e.g.  $\pm 16.5$  V instead of  $\pm 15$  V), where the leakages tend to be the highest. This is essential for designs where worst-case leakage must be well known, such as precision instruments and sample-and-hold amplifiers.

The operating range of the DGP201A is increased beyond that of the DG201A, up to  $\pm 22$  V and down to  $\pm 10.8$  V. This allows the switches to have guaranteed performance limits with power supplies as low as  $\pm 12$  V ( $\pm 10\%$ ).

### ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V <sup>-1</sup>	
V+	44 V
GND	25 V
Digital Inputs <sup>1</sup> V <sub>S</sub> , V <sub>D</sub>	(V-) - 2 V to (V+) + 2 V or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Current, S or D (Pulsed 1 ms 10% duty)	100 mA
Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	-55 to 125°C
(D Suffix)	-40 to 85°C

Power Dissipation (Package) *	
16-Pin Plastic DIP**	450 mW
16-Pin CerDIP***	900 mW
20-Pin LCC****	750 mW
16-Pin SO*****	600 mW

- \* All leads welded or soldered to PC board.
- \*\* Derate 6 mW/°C above 75°C.
- \*\*\* Derate 12 mW /°C above 75°C.
- \*\*\*\* Derate 10 mW/°C above 75°C.
- \*\*\*\*\* Derate 7.6 mW /°C above 75°C.

<sup>1</sup> Signals on S<sub>x</sub>, D<sub>x</sub>, or I<sub>Nx</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT	
			1=25°C		A SUFFIX		D SUFFIX			
			2=125,85°C		-55 to 125°C		-40 to 85°C			
			3=-55,-40°C		MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
				TEMP	TYP <sup>d</sup>					
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3			-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>+</sub> = 13.5 V, V <sub>-</sub> = -13.5 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±10.0 V	1,3 2	115			175 250		175 250	Ω
		V <sub>+</sub> = 10.8 V, V <sub>-</sub> = 10.8 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±7.5 V V <sub>IN</sub> = 0.4 V	1,3 2	145			250 325		250 325	
		V <sub>+</sub> = 22 V, V <sub>-</sub> = -22 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±15 V	1,3 2	85			125 225		125 225	
Delta Drain-Source ON Resistance	Δ r <sub>DS(ON)</sub>	V <sub>D</sub> = +5, 0, -5 V, I <sub>S</sub> = ±1 mA V <sub>IN</sub> = 0.8 V Worst Combination	1,3 2	5			10 15		10 15	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>D</sub> = -15.5 V V <sub>S</sub> = -15.5 V	1 2	0.015	-0.25 -20	0.25 20	-0.25 -2	0.25 2	
			V <sub>D</sub> = +15.5 V V <sub>S</sub> = +15.5 V	1 2	0.015	-0.25 -20	0.25 20	-0.25 -2	0.25 2	
		V <sub>+</sub> = 22 V V <sub>-</sub> = -22 V	V <sub>D</sub> = -21 V V <sub>S</sub> = -21 V	1 2	0.15	-2 -200	2 200	-2 -20	2 200	
			V <sub>D</sub> = +21 V V <sub>S</sub> = +21 V	1 2	0.15	-2 -200	2 200	-2 -200	2 200	
		V <sub>D</sub> = -5 V V <sub>S</sub> = -5 V		2				-10 10	-2 2	2
		V <sub>D</sub> = +5 V V <sub>S</sub> = +5 V		2				-10 10	-2 2	2
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>+</sub> = 13.5 V V <sub>-</sub> = -13.5 V	V <sub>D</sub> = -12.5 V V <sub>S</sub> = +12.5 V	1 2	-0.01		0.25 10		0.25 1	
			V <sub>D</sub> = +12.5 V V <sub>S</sub> = -12.5 V	1 2	-0.01	-0.25 -10		-0.25 -1		
		V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>D</sub> = -15.5 V V <sub>S</sub> = +15.5 V	1 2	0.015			0.25 10		0.25 1
			V <sub>D</sub> = +15.5 V V <sub>S</sub> = -15.5 V	1 2	-0.015	-0.25 -10		-0.25 -1		
		V <sub>+</sub> = 22 V V <sub>-</sub> = -22 V V <sub>IN</sub> = 3 V	V <sub>D</sub> = -21 V V <sub>S</sub> = +21 V	1 2	0.15			1 100		1 10
			V <sub>D</sub> = +21 V V <sub>S</sub> = -21 V	1 2	-0.15	-1 -100		-1 -10		
		V <sub>D</sub> = -5 V V <sub>S</sub> = +5 V		2				5		1
		V <sub>D</sub> = +5 V V <sub>S</sub> = -5 V		2				-5		-1



ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>		LIMITS						UNIT	
				1=25°C		A SUFFIX		D SUFFIX			
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH (Cont'd)</b>											
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>+</sub> = 13.5 V V <sub>-</sub> = -13.5 V	V <sub>D</sub> = -12.5 V V <sub>S</sub> = +12.5 V	1	0.01		0.25		0.25	nA	
			V <sub>D</sub> = +12.5 V V <sub>S</sub> = -12.5 V	2	-0.01	-0.25	-10		-0.25		-1
		V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>D</sub> = -15.5 V V <sub>S</sub> = +15.5 V	1	0.015		0.25		0.25		
			V <sub>D</sub> = +15.5 V V <sub>S</sub> = -15.5 V	2	-0.015	-0.25	-10		-0.25		-1
		V <sub>+</sub> = 22 V V <sub>-</sub> = -22 V V <sub>IN</sub> = 3 V	V <sub>D</sub> = -21 V V <sub>S</sub> = +21 V	1	0.15		1		1		
			V <sub>D</sub> = +21 V V <sub>S</sub> = -21 V	2	-0.15	-1	-100		-1		-10
		V <sub>D</sub> = -5 V V <sub>S</sub> = +5 V	2			5			1		
V <sub>D</sub> = +5 V V <sub>S</sub> = -5 V	2			-5			-1				
<b>INPUT</b>											
Input current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>+</sub> = 22 V, V <sub>-</sub> = -22 V V <sub>IN</sub> under test = 2.4 V		1	-0.005	-0.5	0.5	-0.5	0.5	μA	
		V <sub>+</sub> = 22 V, V <sub>-</sub> = -22 V V <sub>IN</sub> under test = 22 V		2	-0.005	-0.5	0.5	-0.5	0.5		
Input current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>+</sub> = 22 V, V <sub>-</sub> = -22 V V <sub>IN</sub> under test = 0 V		1	0.005	-0.5	0.5	-0.5	0.5		
<b>DYNAMIC</b>											
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuits		1	450		600		600	ns	
				2,3			800		800		
Turn-OFF Time	t <sub>OFF</sub>	1	320		450		450				
		2,3			600		600				
Delta t <sub>ON</sub>	Δ t <sub>ON</sub>	Worst Combination among channels of the t <sub>ON</sub> measurements		1	30		50		50		
				2,3			100		100		
Delta t <sub>OFF</sub>	Δ t <sub>OFF</sub>	Worst Combination among channels of the t <sub>OFF</sub> measurements		1	30		50		50		
				2,3			100		100		
Charge Injection	Q	R <sub>gen</sub> = 0 Ω C <sub>L</sub> = 10 nF	V <sub>gen</sub> = 0 V	1	25		50		50	pC	
			V <sub>gen</sub> = ± 10 V	1	33		100		100		
Source OFF Capacitance <sup>d</sup>	C <sub>S(OFF)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V		1	4.5					pF	

**5**

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
Drain OFF Capacitance <sup>d</sup>	C <sub>D(OFF)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	1	5.5					pF
Channel ON Capacitance <sup>d</sup>	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	1	15					
Crosstalk (Channel-to-Channel)		R <sub>L</sub> = 50 Ω    C <sub>L</sub> = 5 pF f = 1 MHz	1	95					dB
OFF Isolation		R <sub>L</sub> = 50 Ω    C <sub>L</sub> = 5 pF f = 1 MHz	1	80					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 or 5 V V <sub>±</sub> = ±16.5 V	1 2	0.8		1.5 2.5		1.5 2.5	mA
Negative Supply Current	I <sub>-</sub>	V <sub>IN</sub> = 0 or 5 V V <sub>±</sub> = ±16.5 V	1 2	0.26	-1 -2		-1 -2		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = Input voltage to perform proper function.

**DIE TOPOGRAPHY**

20X

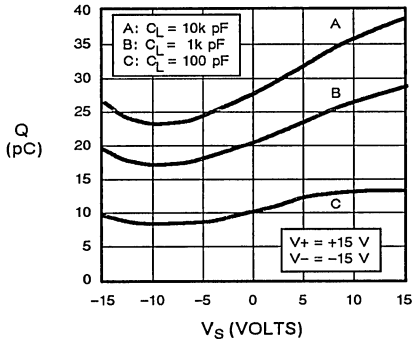
Pad No.	Function
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	GND
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

ICMCB

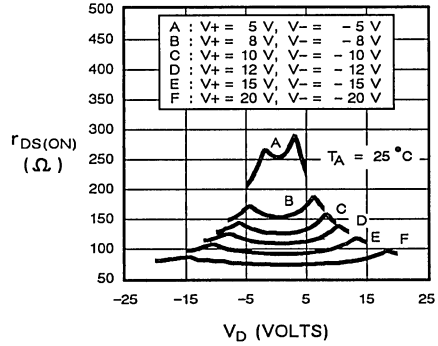
8 Capacitors	49 P-channel enhancement MOSFET
9 Resistors	45 N-channel enhancement MOSFET

## TYPICAL CHARACTERISTICS

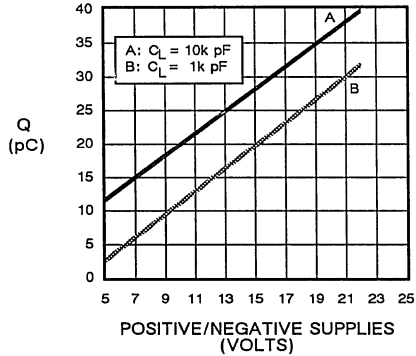
Charge Injection vs. Analog Voltage ( $V_S$ )



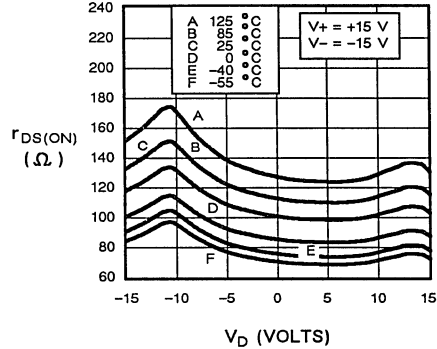
$r_{DS(ON)}$  vs.  $V_D$  and Power Supply Voltage



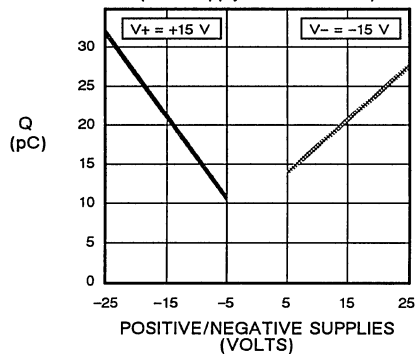
Charge Injection vs. Power Supply Voltage



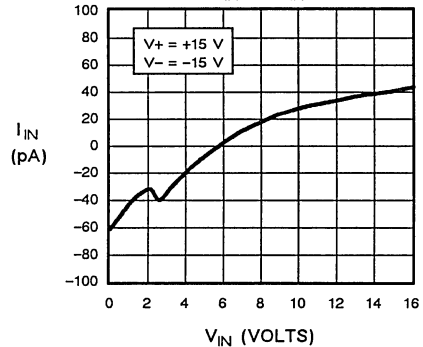
$r_{DS(ON)}$  vs.  $V_D$  and Temperature



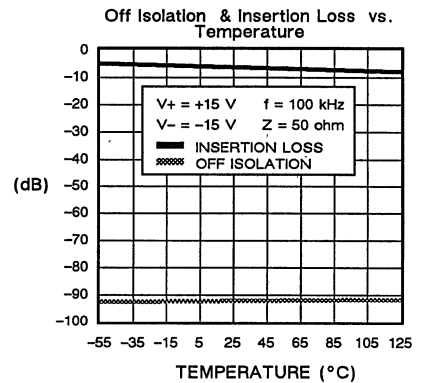
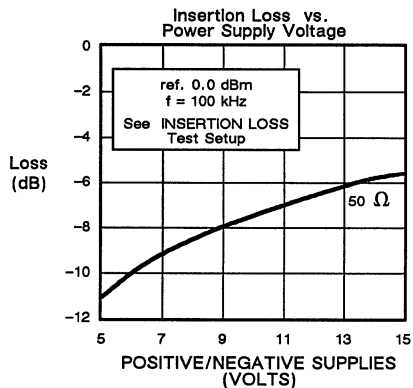
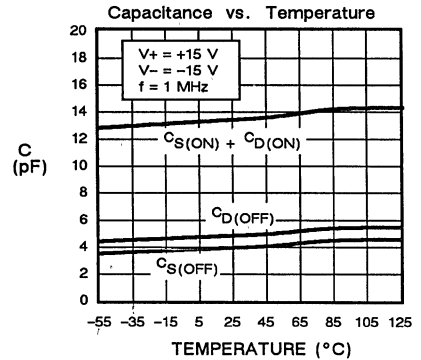
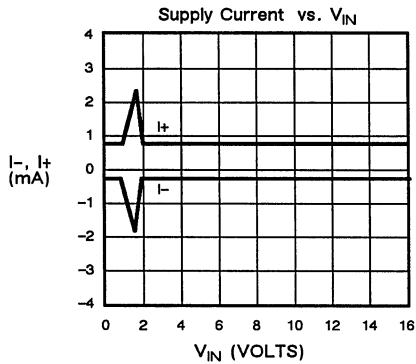
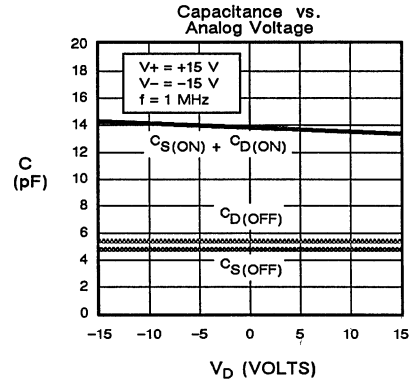
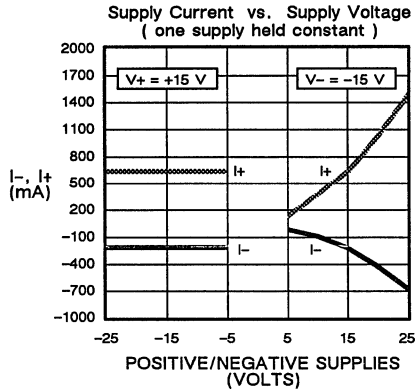
Charge Injection vs. Power Supply Voltage (one supply held constant)



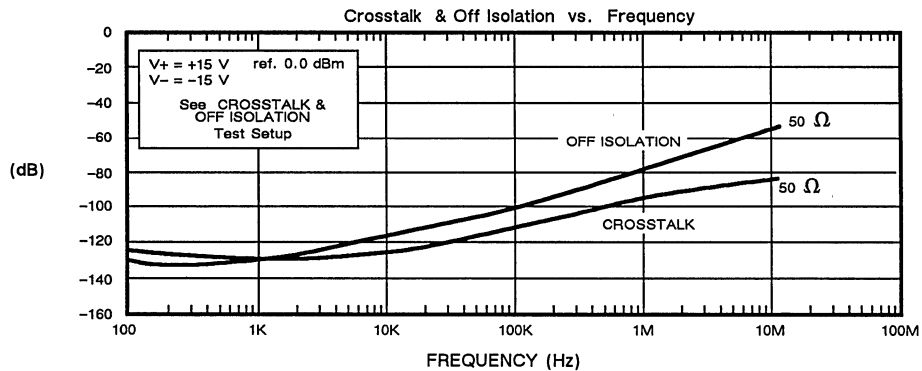
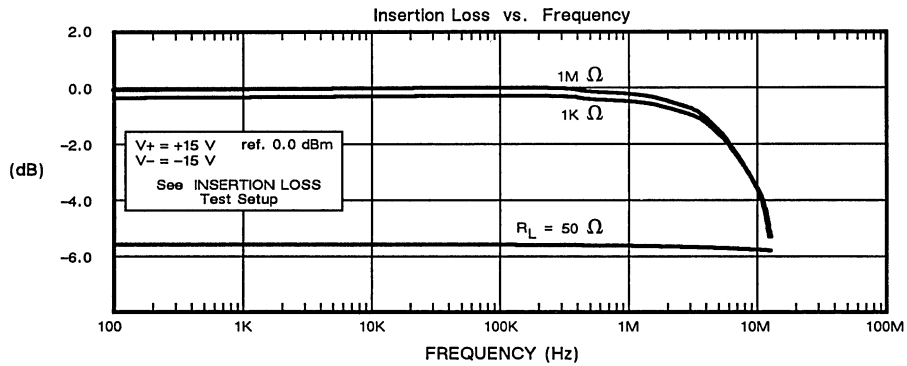
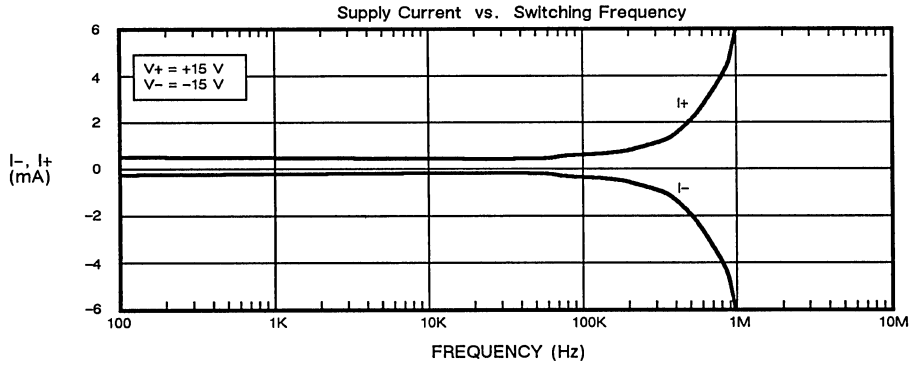
$I_{IN}$  vs.  $V_{IN}$



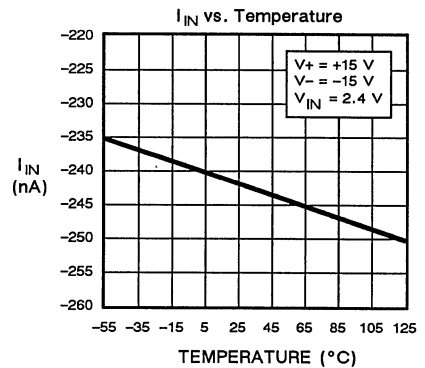
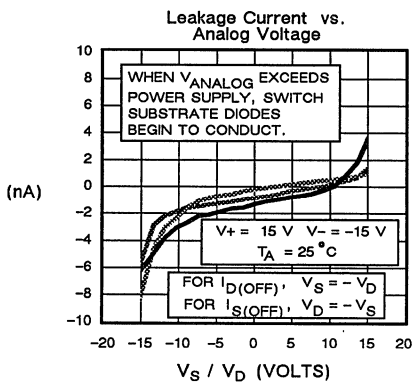
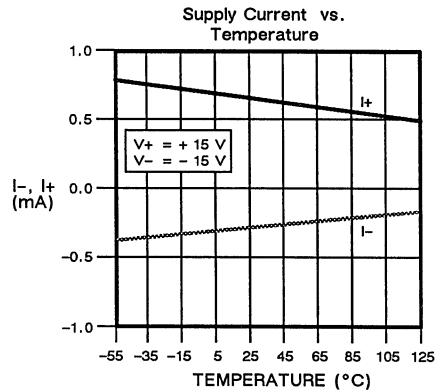
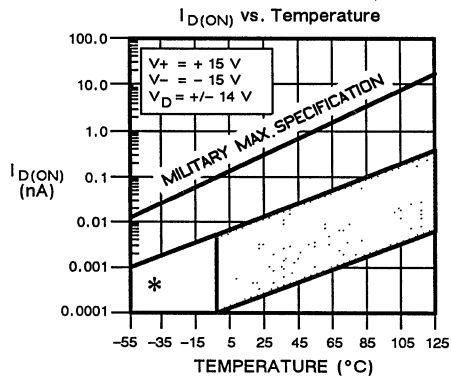
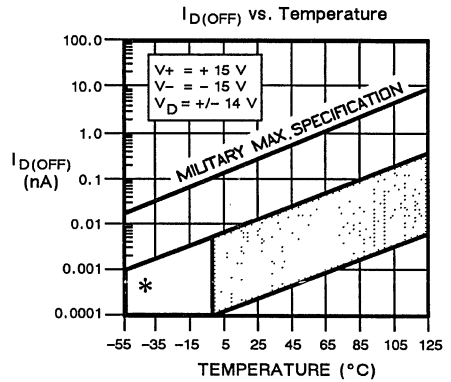
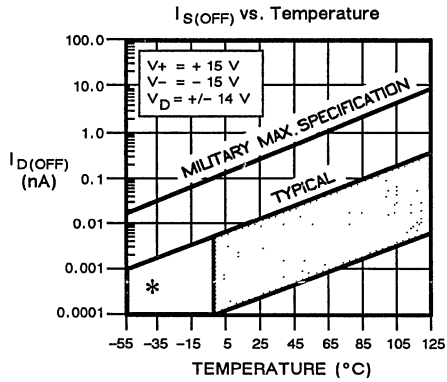
## TYPICAL CHARACTERISTICS



**TYPICAL CHARACTERISTICS**

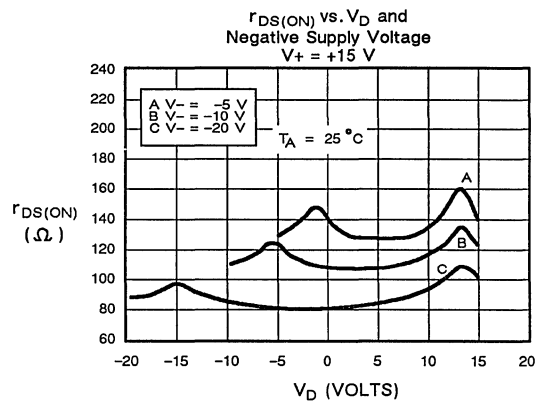
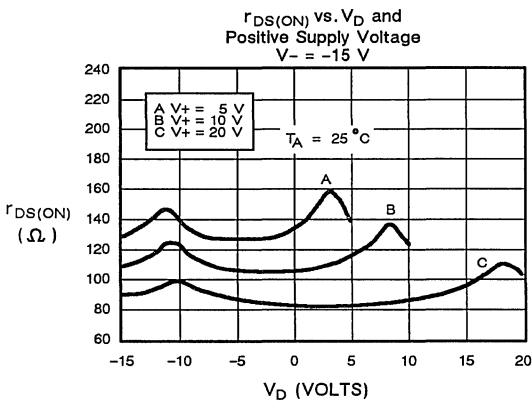
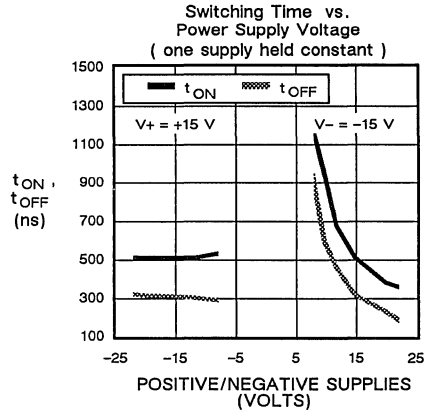
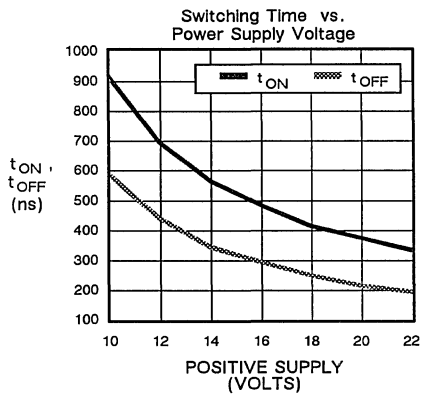
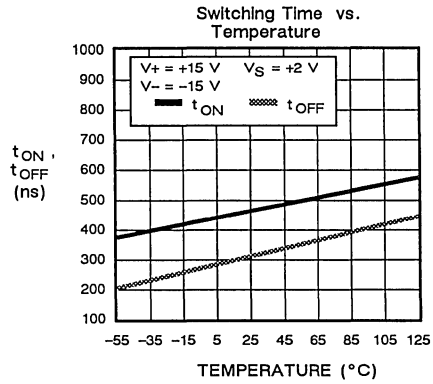
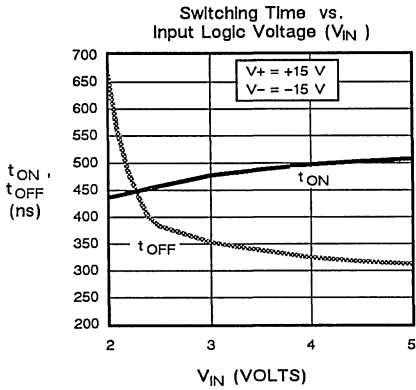


## TYPICAL CHARACTERISTICS

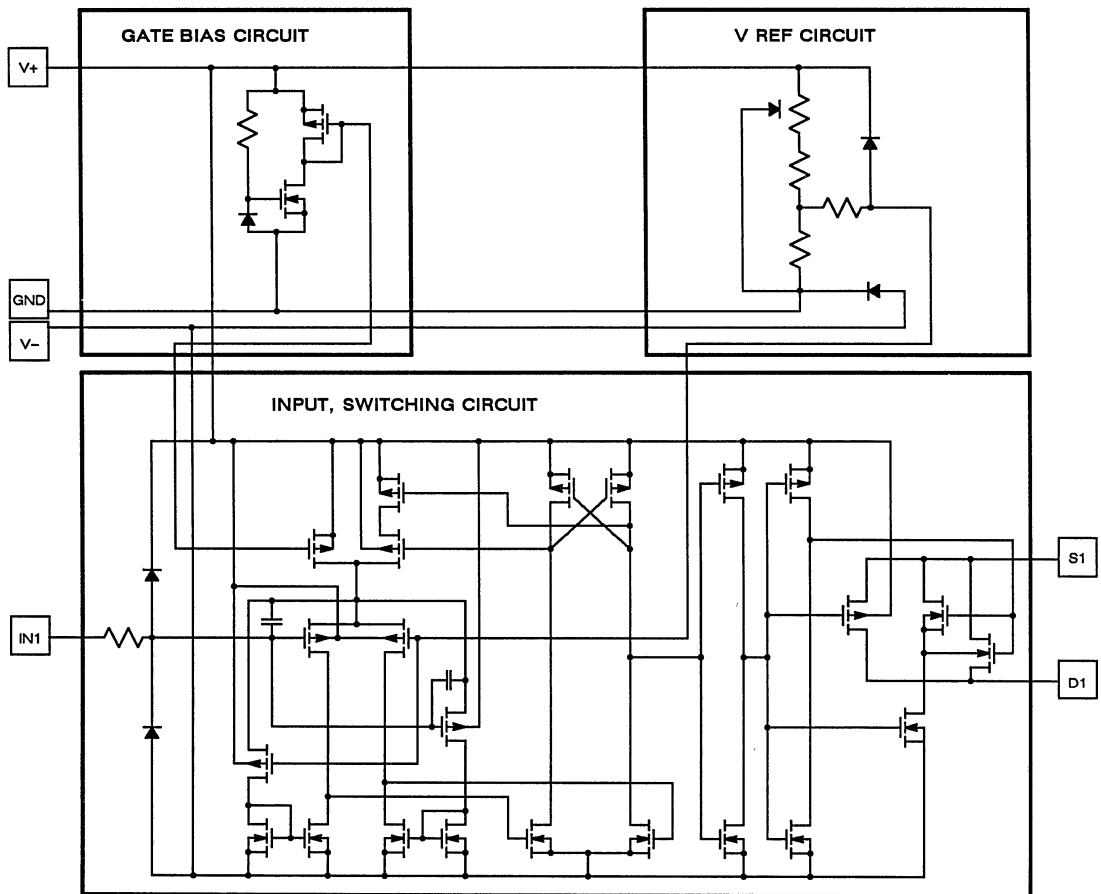


\* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

**TYPICAL CHARACTERISTICS**

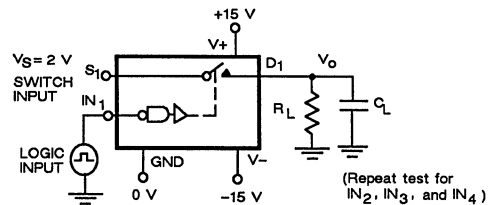
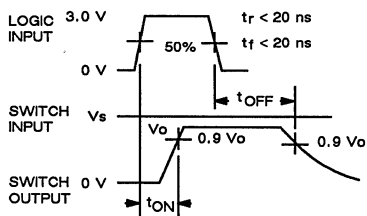


## SCHEMATIC DIAGRAM (Typical Channel)



## SWITCHING TIME TEST CIRCUITS

$V_o$  is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

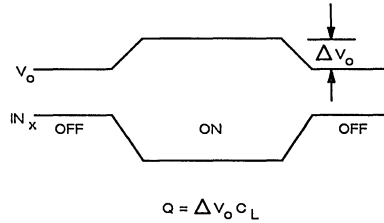
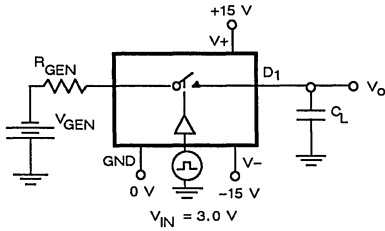


For load conditions, See Electrical Characteristics  
 $C_L$  (includes fixture and stray capacitance)

$$V_o = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

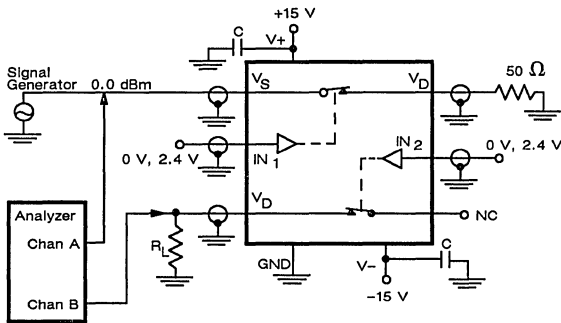


**CHARGE INJECTION TEST CIRCUIT**



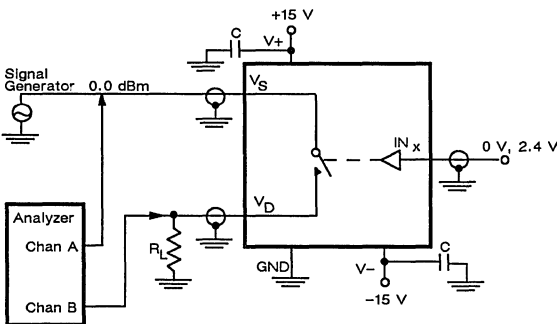
$$Q = \Delta V_O C_L$$

**CROSSTALK TEST CIRCUIT**



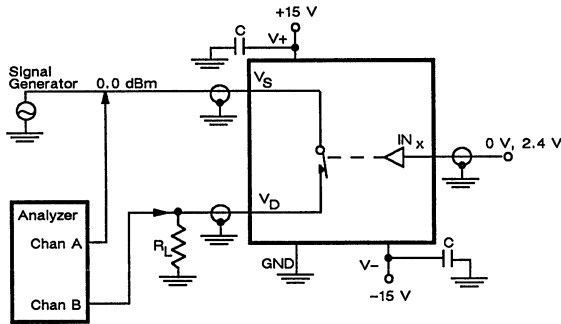
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

**OFF ISOLATION TEST CIRCUIT**



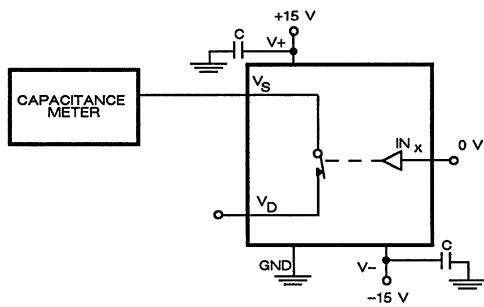
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## INSERTION LOSS TEST CIRCUIT



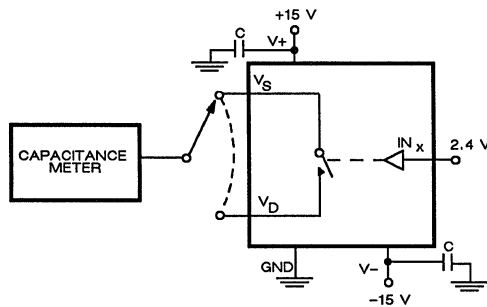
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## SOURCE/DRAIN ON CAPACITANCE



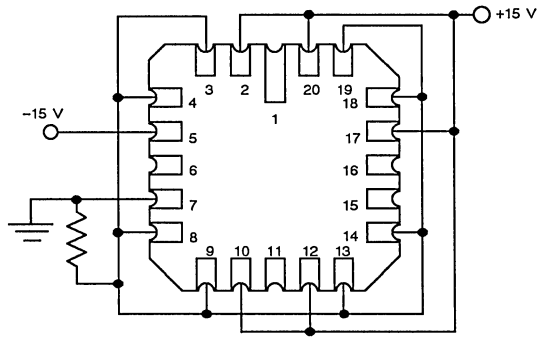
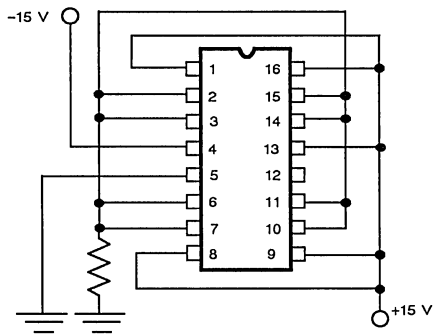
METER
BOONTON 72BD Capacitance Meter or equivalent

## SOURCE/DRAIN OFF CAPACITANCE



METER
BOONTON 72BD Capacitance Meter or equivalent

## BURN-IN CIRCUIT



Note: All Resistors are 10 k  $\Omega$  unless otherwise specified

Note: LCC package uses same circuit and conditions as the DIP

## PIN DESCRIPTION

SYMBOL	DESCRIPTION
S	An Analog Channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground
V <sub>L</sub>	Logic Supply Voltage

5

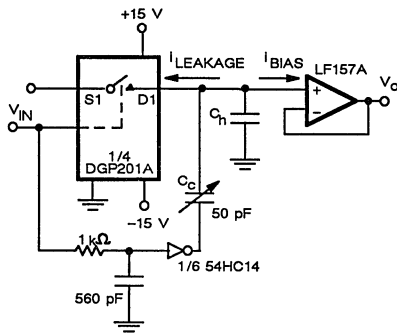
## APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
5	-5	1.0/0.2	-5 to 5
10	-10	1.5/0.5	-10 to 10
15	-15	2.4/0.8	-15 to 15
22	-22	3.0/1.2	-22 to 22

## APPLICATION HINTS (Cont'd)

### Sample-and-Hold Circuit:

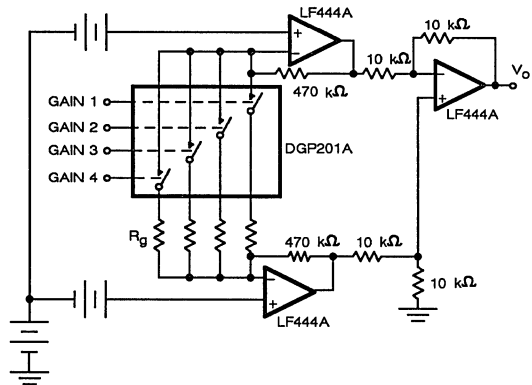
The DGP201A helps to reduce two common sources of error. First, its low charge injection reduces DC offset errors that would appear at the holding capacitor  $C_h$ . Second; its guaranteed low leakage current reduces the voltage drop rate during the holding period. When further charge injection is required, the Schmitt trigger (54HC14) and compensation capacitor  $C_C$  may be used to generate a charge of opposite polarity.



Sample-and-Hold Circuit

### Precision Instrumentation Amplifier With Digitally Programmable Gains:

This instrumentation-quality differential amplifier can be designed for high gains. The input stages take advantage of the low leakage characteristics of the DGP201A to provide switching of the gain setting resistors ( $R_g$ ) without causing excessive DC offsets.



Precision Instrumentation Amplifier with Digitally Programmable Gains

## Quad Monolithic SPST CMOS Analog Switches

### FEATURES

- $\pm 15$  Volt Input Range
- Low OFF Leakage ( $I_{S(OFF)} < 1$  nA)
- Low ON Resistance
- 44 V Maximum Supply Ratings
- TTL and CMOS Compatible
- Low Power Requirements
- Logic Inputs Accept Negative Voltages

### BENEFITS

- Wide Dynamic Range
- Low Distortion Switching
- No Pull-Up Resistors Required
- Reduced Power Supply Consumption
- Can be Driven from Comparators or Op Amps Without Limiting Resistors
- Multiple Sourced

### APPLICATIONS

- Disk Drives
- Radar Systems
- Communication Systems
- Low Transient Sample/Holds

### DESCRIPTION

The DG201A and DG202 are quad SPST analog switches designed to provide accurate switching over a wide range of input signals. By combining a low ON resistance and a wide signal range ( $\pm 15$  V) with low charge-transfer makes these devices well suited for industrial and military applications.

Built on Siliconix' high voltage metal gate process to achieve optimum switch performance, each switch conducts equally well in both directions when ON. When OFF these switches will block up to 30 V peak-to-peak and have a 44 V maximum power supply rating. ON resistance is very flat over the full  $\pm 15$  V analog range rivaling JFET performance

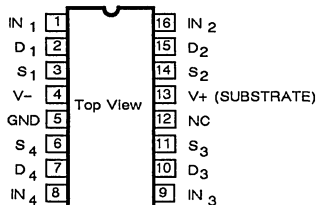
without the inherent dynamic range limitation. Internal pull-up resistors simplify interface to CMOS or TTL drive circuits. An epitaxial layer prevents latch up.

These two devices are differentiated by the type of switch actions, as shown in the functional block diagram. Package options for this series includes both the 16-pin plastic and CerDIP. Performance grades include the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ), industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ), commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ) and extended industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ) temperature ranges. Additionally, the DG201A is available in surface mount 20-pin LCC and 16-pin SO packages.

**5**

### PIN CONFIGURATION

Dual-In-Line Package

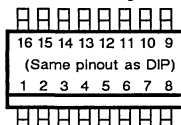


Order Numbers:

CerDIP: DG201AAK, DG201AAK/883  
 DG201ABK, DG201ACK  
 DG202AK, DG202AK/883  
 DG202BK, DG202CK

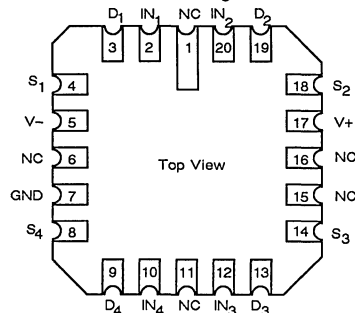
Plastic: DG201ACJ  
 DG202CJ

SO Package



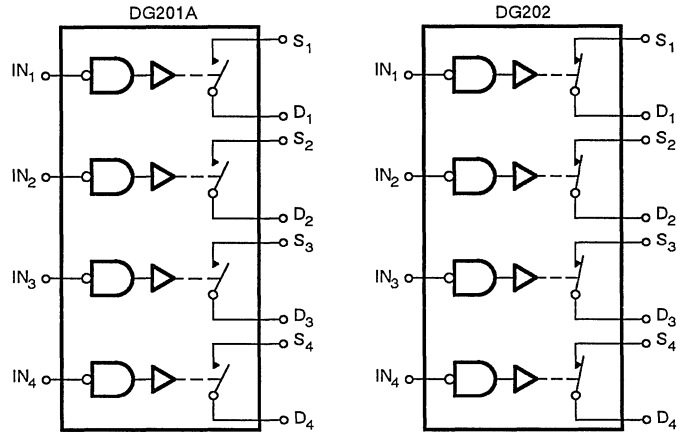
Order Number:  
 DG201ADY

LCC Package



Order Number:  
 DG201AAZ/883

## FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches Per Package\*

LOGIC	DG201A	DG202
0	ON	OFF
1	OFF	ON

LOGIC "0"  $\leq 0.8$  V  
LOGIC "1"  $\geq 2.4$  V

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs<sup>e</sup> V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2 V  
..... or 20 mA, whichever occurs first.

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D  
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature (K, Z Suffix) ..... -65 to 150°C  
(J, Y Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
(B Suffix) ..... -25 to 85°C  
(C Suffix) ..... 0 to 70°C  
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*

16-Pin CerDIP\*\* ..... 900 mW  
16-Pin Plastic Dip\*\*\* ..... 470 mW  
20-Pin LCC\*\*\*\* ..... 750 mW  
16-Pin SO\*\*\*\*\* ..... 640 mW

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6.5 mW/°C above 25°C.

\*\*\*\* Derate 10 mW/°C above 75°C.

\*\*\*\*\* Derate 7.6 mW/°C above 75°C

## ELECTRICAL CHARACTERISTICS<sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B,C,D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = ± 10 V I <sub>S</sub> = 1 mA V <sub>IN</sub> = 0.8 V (DG201A) V <sub>IN</sub> = 2.4 V (DG202)	1,3 2	115		175 250		175 250	Ω

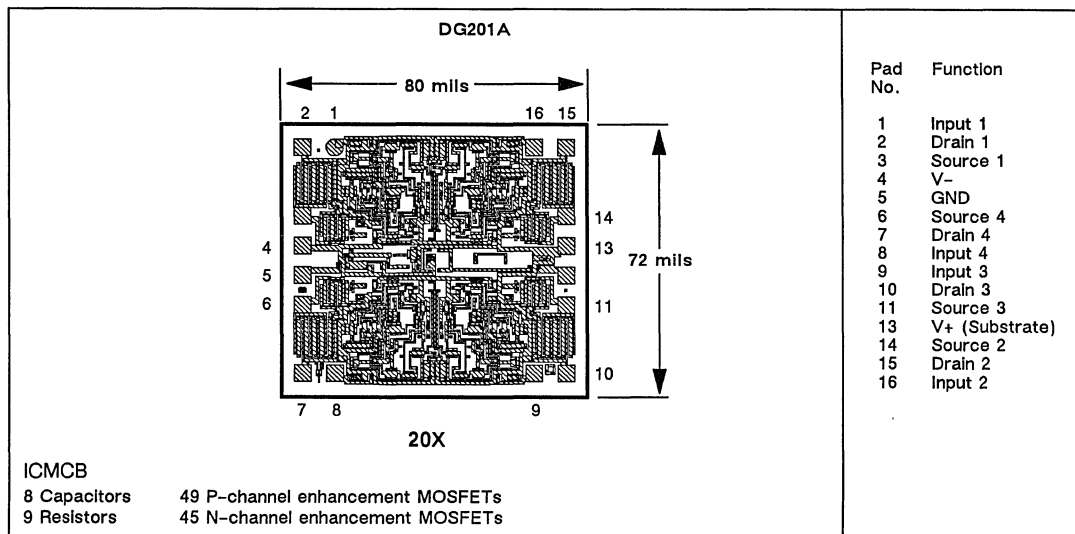
ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT		
			1=25°C 2=125,85,70°C 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B, C, D SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SWITCH (Cont'd)</b>											
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.4 V (DG201A)	V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	0.01		1 100		5 100	nA	
			V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	-0.02	-1 -100		-5 -100			
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN</sub> = 0.8 V (DG202)	V <sub>D</sub> = 14 V V <sub>S</sub> = -14 V	1 2	0.01		1 100		5 100		
			V <sub>D</sub> = -14 V V <sub>S</sub> = 14 V	1 2	-0.02	-1 -100		-5 -100			
Drain ON Leakage Current <sup>f</sup>	I <sub>D(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	V <sub>IN</sub> = 0.8 V (DG201A)	1 2	0.1		1 200		5 200		
			V <sub>IN</sub> = 2.4 V (DG202)	1 2	-0.15	-1 -200		-5 -200			
<b>INPUT</b>											
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 2.4 V		1 2	-0.0004	-1 -1		-1 -10		μA	
		V <sub>IN</sub> = 15 V		1 2	0.003		1 10		1 10		
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V		1 2	-0.0004	-1 -10		-1 -10			
<b>DYNAMIC</b>											
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit			1	480		600		600	ns
Turn-OFF Time	t <sub>OFF</sub>				1	370		450		450	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>gen</sub> = 0 V R <sub>gen</sub> = 0 Ω			1	20					pC
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V V <sub>IN</sub> = 5 V	f = 1 MHz	1	5						pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>			1	5						
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>			V <sub>D</sub> = V <sub>S</sub> = 0 V V <sub>IN</sub> = 0 V	1	16					
OFF Isolation		V <sub>IN</sub> = 5 V, Z <sub>L</sub> = 75 Ω V <sub>S</sub> = 2 V, f = 100 kHz			1	70					dB
Crosstalk (Channel-to-Channel)					1	90					

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		B, C, D SUFFIX		
			2=125, 85, 70°C		-55 to 125°C				
			3=-55, -25, 0°C						
			TEMP	TYP <sup>d</sup>	MIN	MAX <sup>b</sup>	MIN	MAX <sup>b</sup>	
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	All Channels ON or OFF	1	0.9		2		2	mA
Negative Supply Current	I <sub>-</sub>		1	-0.3	-1		-1		

**NOTES:**

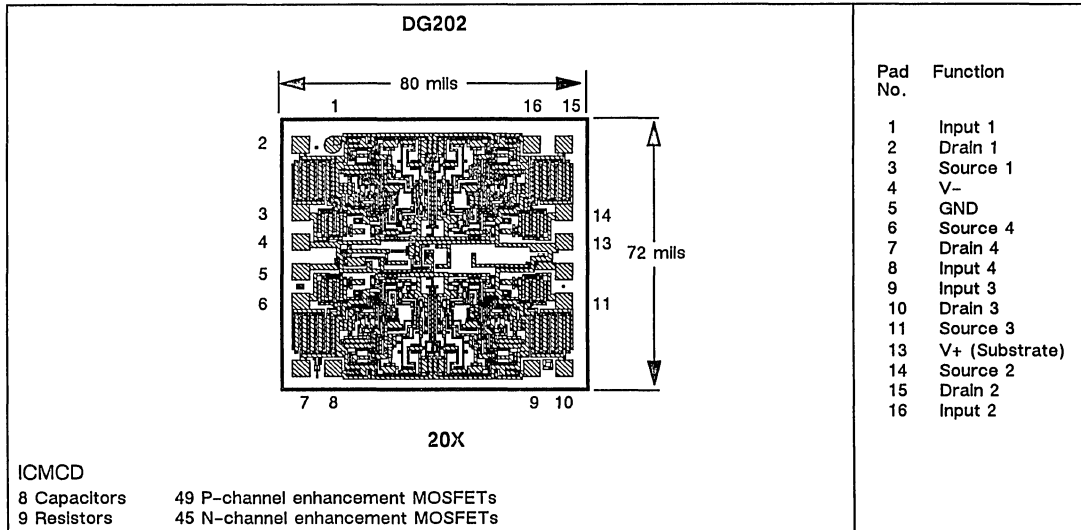
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Signals on S<sub>x</sub>, D<sub>x</sub>, or IN<sub>x</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- f. I<sub>D(ON)</sub> is leakage from driver into "ON" switch.

## DIE TOPOGRAPHY



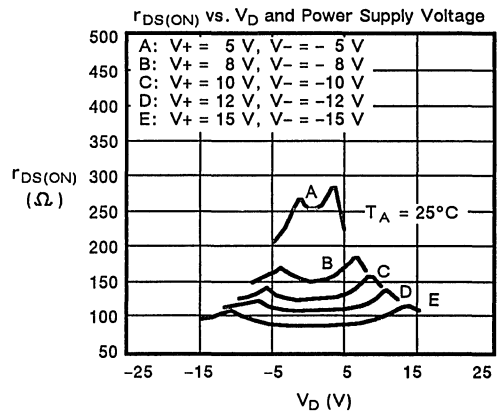
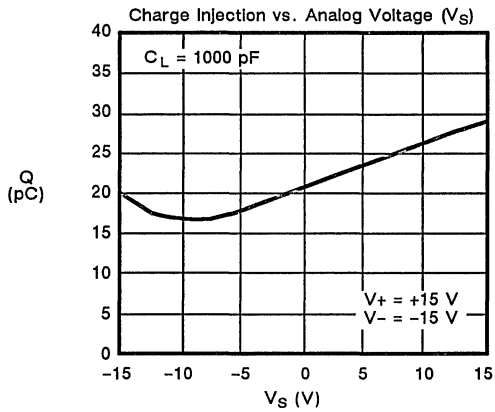


## DIE TOPOGRAPHY

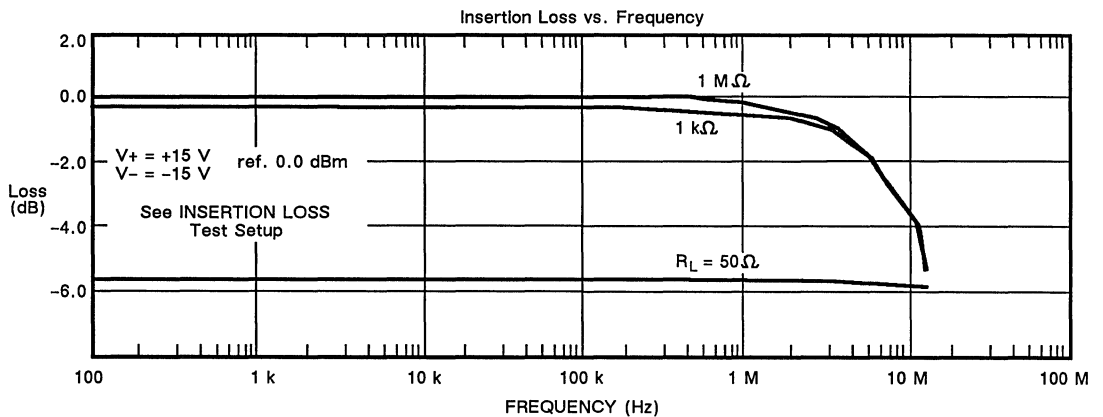
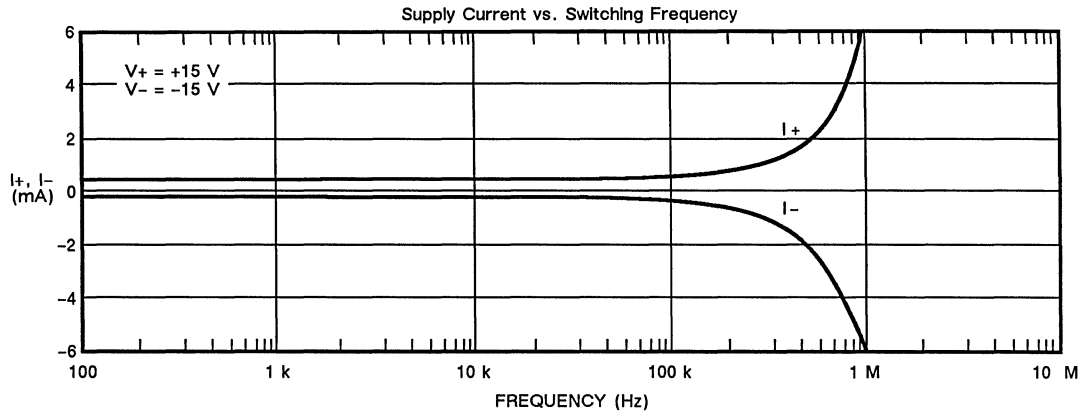
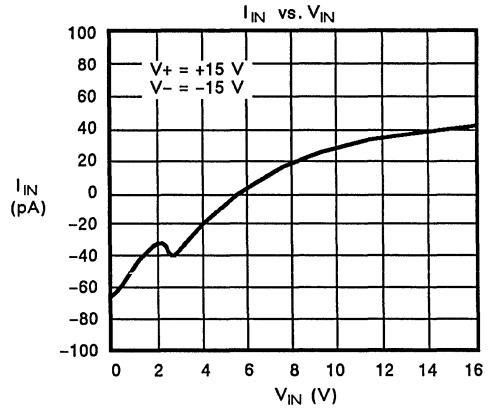
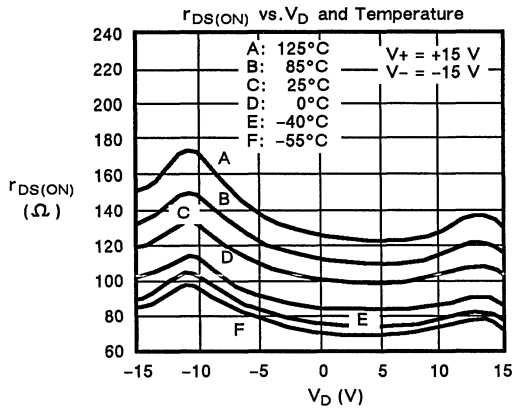


## TYPICAL CHARACTERISTICS

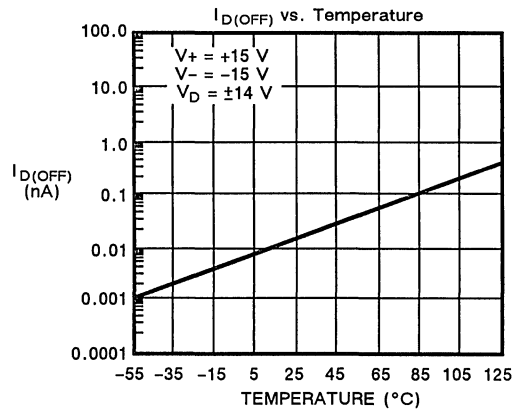
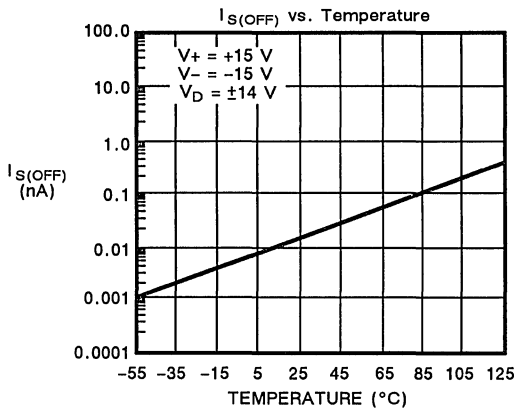
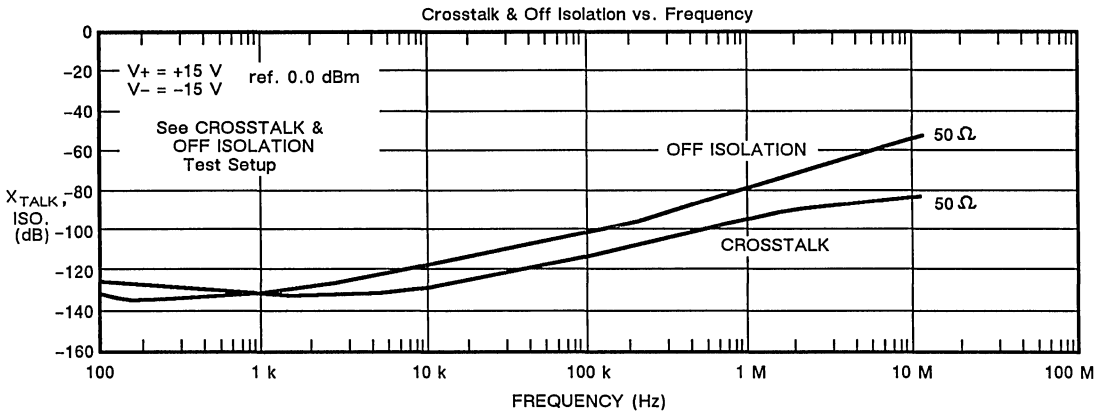
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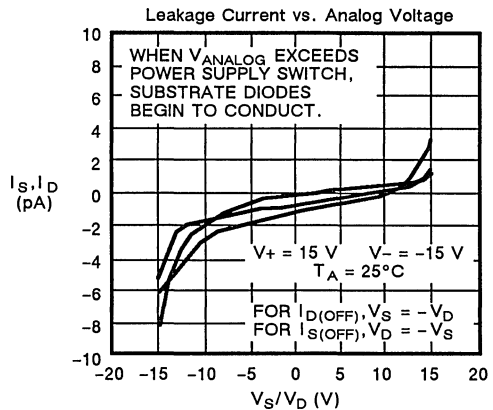
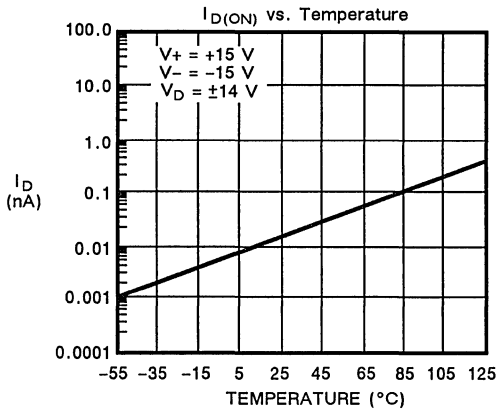
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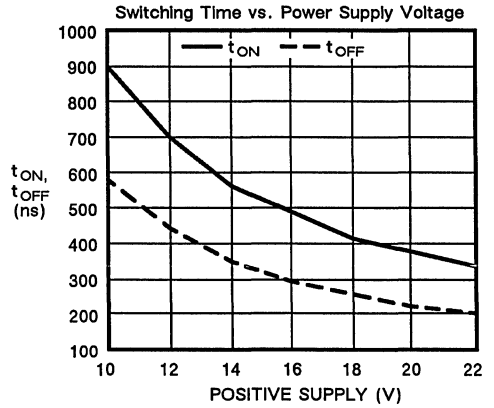
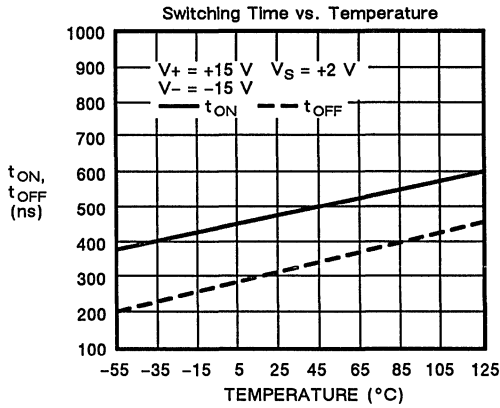
**TYPICAL CHARACTERISTICS (Cont'd)**



**5**

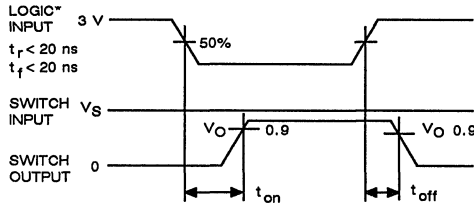


## TYPICAL CHARACTERISTICS (Cont'd)

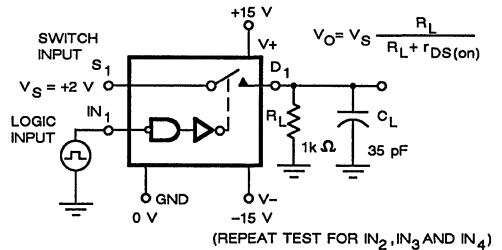


## SWITCHING TIME TEST CIRCUIT

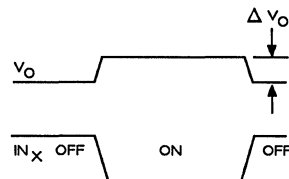
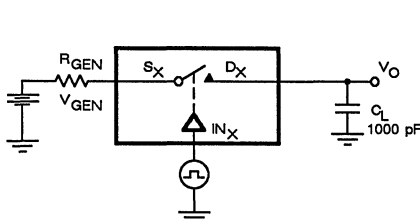
Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



\* Logic Shown for DG201A, Invert for DG202.

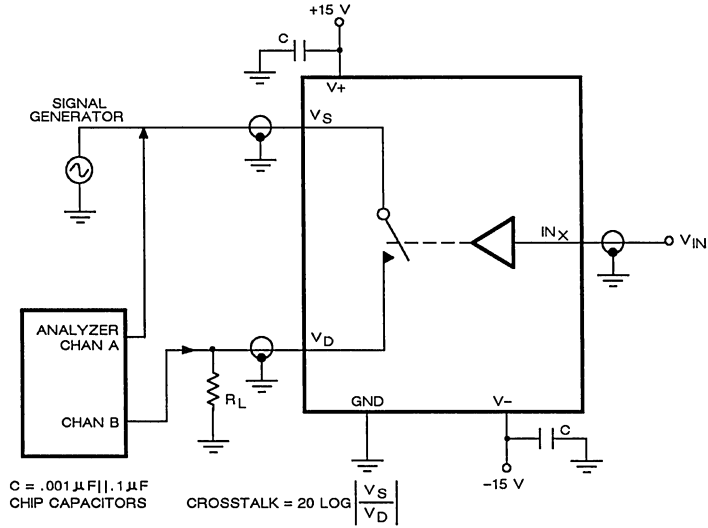


## CHARGE INJECTION TEST CIRCUIT



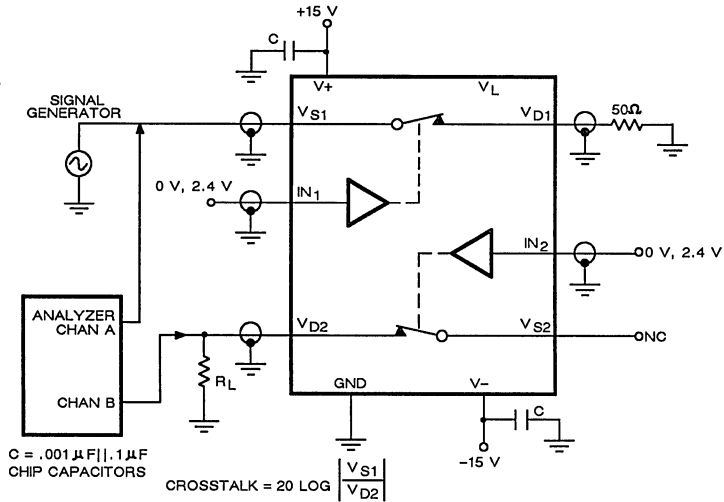
$\Delta V_O = \text{MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE CHARGE INJECTION IN COULOMBS IS } \Delta Q = C_L \times \Delta V_O$

**OFF ISOLATION TEST CIRCUIT**

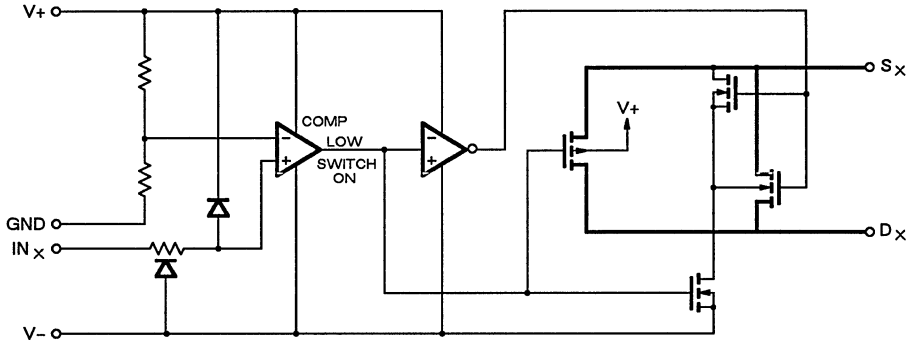


**CHANNEL-TO-CHANNEL CROSSTALK TEST CIRCUIT**

**5**



## SCHEMATIC DIAGRAM (Typical Channel)



## APPLICATION HINTS\*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15 **	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
10	-10	2.4/0.8	-10 to 10
8 ***	-8		-8 to 8

\* Application Hints are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

\*\* Electrical Characteristic chart based on V+ = +15 V, V- = -15 V.

\*\*\* Operation below 8 V is not recommended.

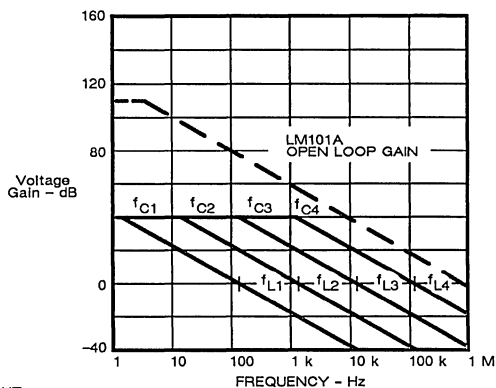
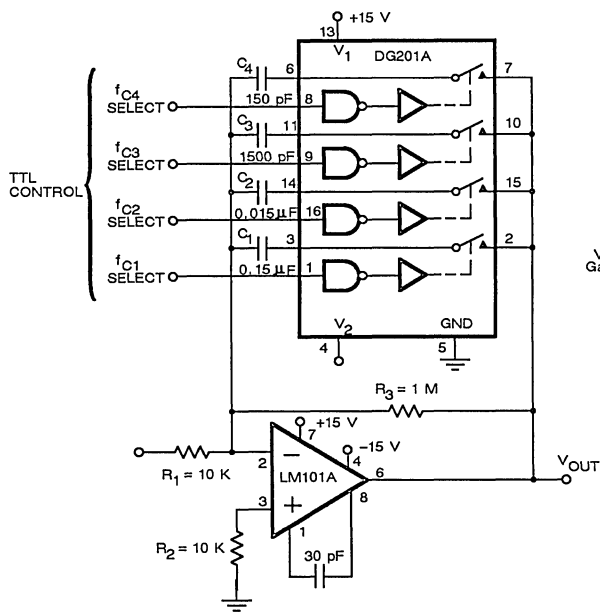
### DG201A

LOGIC INPUT	SWITCH STATE	LOGIC VOLT LEVEL
0	ON	≤ 0.8 V
1	OFF	≥ 2.4 V

### DG202

LOGIC INPUT	SWITCH STATE	LOGIC VOLT LEVEL
0	OFF	≤ 0.8 V
1	ON	≥ 2.4 V

## APPLICATIONS



$$A_L (\text{VOLTAGE GAIN BELOW BREAK FREQUENCY}) = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

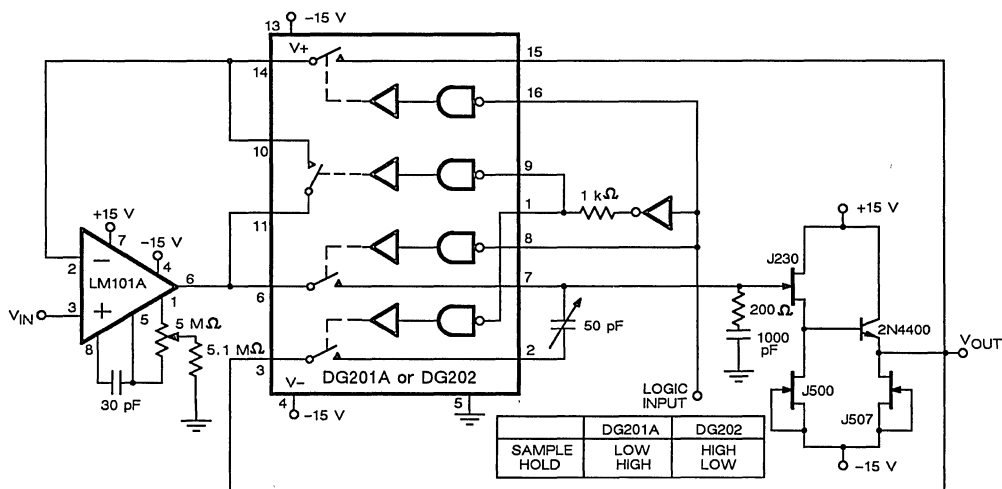
$$f_C (\text{BREAK FREQUENCY}) = \frac{1}{2\pi R_3 C_X}$$

$$f_L (\text{UNITY GAIN FREQUENCY}) = \frac{1}{2\pi R_1 C_X}$$

$$\text{MAX ATTENUATION} = -\frac{r_{DS(on)}}{10 \text{ K}} \approx -40 \text{ dB}$$

Active Low Pass Filter with Digitally Selected Break Frequency

5

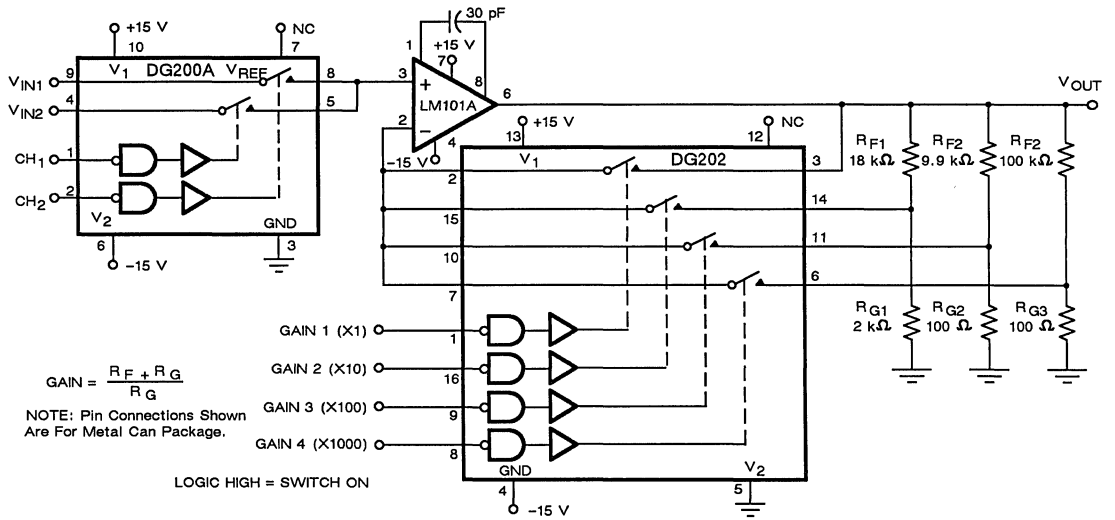


**TYPICAL PERFORMANCE**

- AQUISITION TIME = 25 μS
- APERTURE TIME = 1 μS
- SAMPLE TO HOLD OFFSET = 5 mV
- DROOP RATE = 5 mV/S

Sample and Hold

## APPLICATIONS



A Precision Amplifier with Digitally Programmable Inputs and Gains



## Low Cost 4-Channel Monolithic SPST CMOS Analog Switches

### FEATURES

- $\pm 15$  V Analog Signal Range
- TTL Compatibility
- PLUS-40 Process
- Logic Inputs Accept Negative Voltages
- ON Resistance < 175  $\Omega$

### BENEFITS

- Wide Signal Range
- Simple Logic Interface
- Reduced Power Consumption

### APPLICATIONS

- Disk Drives
- Video Terminals
- Communication Systems

### DESCRIPTION

The DG211 and DG212 are low cost quad single-pole single-throw analog switches for use in general purpose switching applications in communication, instrumentation and process control. These devices differ only in that the digital control logic is inverted, as shown in the truth table. The use of both p- and n-channel devices minimizes ON-resistance variations over the analog signal range.

Designed with the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 40 V, both switches will

handle  $\pm 15$  V input signals with ease, and have a continuous current rating of 20 mA. An epitaxial layer prevents latchup.

Both devices feature true bi-directional performance (with no offset voltage) in the ON condition, and will block signals to 30 V peak-to-peak in the OFF condition.

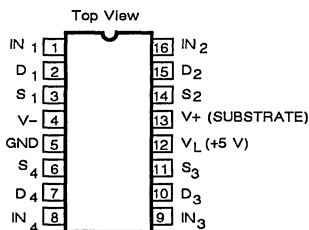
Packaging for this series includes 16-pin plastic DIP and small outline options. Performance grades include both commercial, C suffix (0 to 70°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

**5**

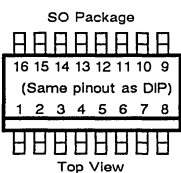
### PIN CONFIGURATION

### FUNCTIONAL BLOCK DIAGRAM

Dual-In-Line Package



Order Numbers:  
DG211CJ, DG212CJ

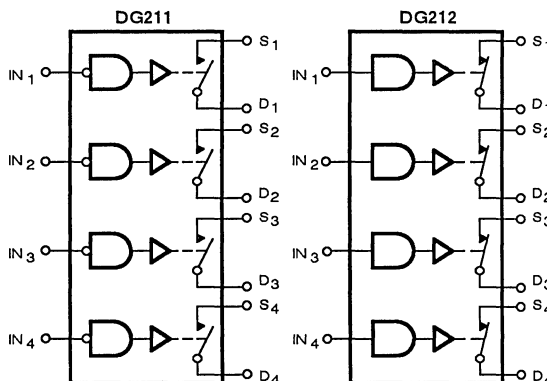


Order Numbers:  
DG211DY, DG212DY

Truth Table

LOGIC	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V



Four SPST Switches per Package\*

\* Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

V <sub>+</sub> to V <sub>-</sub> .....	40 V
V <sub>IN</sub> to GND .....	V <sub>-</sub> , V <sub>+</sub>
V <sub>L</sub> to GND .....	-0.3 V, 25 V
V <sub>S</sub> or V <sub>D</sub> to V <sub>+</sub> .....	0, -40 V
V <sub>S</sub> or V <sub>D</sub> to V <sub>-</sub> .....	0, 40 V
V <sub>+</sub> to GND .....	25 V
V <sub>-</sub> to GND .....	-25 V
Current, Any Terminal Except S or D .....	30 mA
Continuous Current, S or D .....	20 mA

Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max) .....	70 mA
Storage Temperature .....	-65 to 125°C
Operating Temperature (C Suffix) .....	0 to 70°C
(D Suffix) .....	40 to 85°C

Power Dissipation (Package)*	
16-Pin Plastic DIP** .....	470 mW
16-Pin Small Outline*** .....	600 mW

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 6.5 mW/°C above 25°C.

\*\*\* Derate 7.6 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS				UNIT
			1=25°C 2=85,70°C 3=-40,0°C		C, D SUFFIX 0 to 70°C -40 to 85°C		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>							
Analog Signal Range <sup>d</sup>	V <sub>ANALOG</sub>		1, 2		-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>IN</sub> = 0.8 V (DG211) V <sub>IN</sub> = 2.4 V (DG212) I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±10 V	1	115		175	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.4 V (DG211)	V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1	0.01	5	nA
			V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1	-0.02	-5	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN</sub> = 0.8 V (DG212)	V <sub>D</sub> = 14 V V <sub>S</sub> = -14 V	1	0.01	5	
			V <sub>D</sub> = -14 V V <sub>S</sub> = 14 V	1	-0.02	-5	
Drain ON Leakage Current <sup>f</sup>	I <sub>D(ON)</sub>	V <sub>IN</sub> = 0.8 V (DG211) V <sub>IN</sub> = 2.4 V (DG212)	V <sub>S</sub> = V <sub>D</sub> = +14 V	1	0.1	5	
			V <sub>S</sub> = V <sub>D</sub> = -14 V	1	-0.15	-5	
<b>INPUT</b>							
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 2.4 V	1	-0.0004	-1		μA
		V <sub>IN</sub> = 15 V	1	0.003		1	
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1	-0.0004	-1		

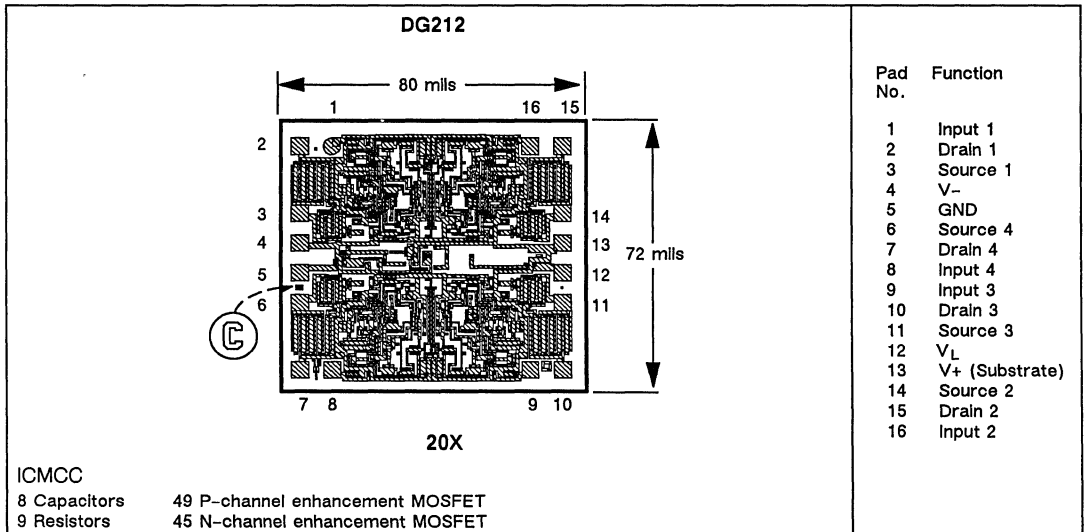
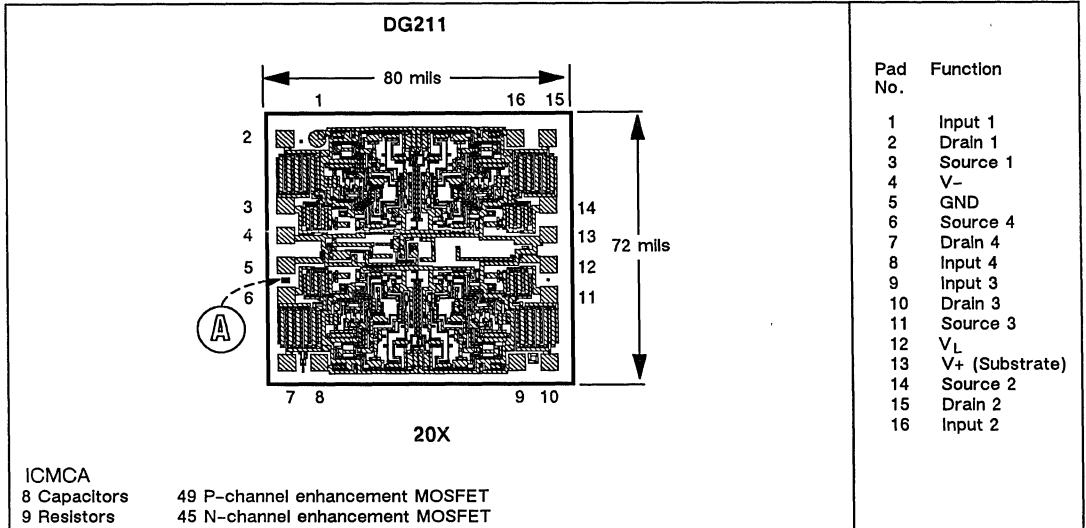
ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>		LIMITS				UNIT
				1=25°C 2=85,70°C 3=-40,0°C		C, D SUFFIX 0 to 70°C		
				TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>								
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit V <sub>S</sub> = 2 V		1	460		1000	ns
Turn-OFF Time	t <sub>OFF1</sub>			1	360		500	
	t <sub>OFF2</sub>			1	450			
Source-OFF Capacitance <sup>d</sup>	C <sub>S(OFF)</sub>	f = 1 MHz	V <sub>IN</sub> = 5 V V <sub>S</sub> = 0 V	1	5			pF
Drain-OFF Capacitance <sup>d</sup>	C <sub>D(OFF)</sub>		V <sub>IN</sub> = 5 V V <sub>D</sub> = 0 V	1	5			
Channel ON Capacitance <sup>d</sup>	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>IN</sub> = 0 V V <sub>S</sub> = V <sub>D</sub> = 0 V	1	16			
Off Isolation <sup>f</sup>		V <sub>IN</sub> = 5 V, R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 15 pF, V <sub>S</sub> = 1 VRMS f = 100 kHz		1	70			dB
Crosstalk (Channel-to-Channel)				1	90			
<b>SUPPLY</b>								
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>IN</sub> = 0 or 5.0 V		1	0.35		0.48	mA
Negative Supply Current	I <sub>-</sub>			1	0.3		0.48	
Logic Supply Current	I <sub>L</sub>			1	0.5		1.2	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = Input voltage to perform proper function.

f. OFF Isolation = 20 Log  $\frac{V_{IN}}{V_{OUT}}$

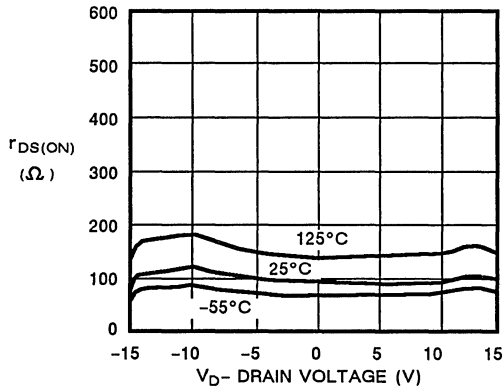
## DIE TOPOGRAPHY



**TYPICAL CHARACTERISTICS**

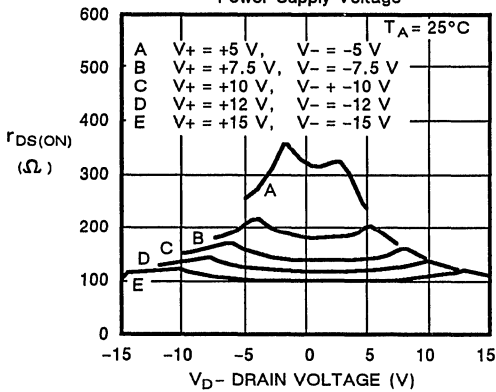
The electrical characteristic table guarantees the DG211 and DG212 for operation at  $\pm 15V$ ,  $\pm 10\%$ ; however, functional operation occurs over the designed range of  $\pm 5V$  to  $\pm 20V$  power supplies. These characteristic graphs show the effect of device parameters over several parameter permutations including power supply variations. These graphs are for design aid only and are not subject to production testing.

$r_{DS(ON)}$  vs.  $V_D$  Temperature

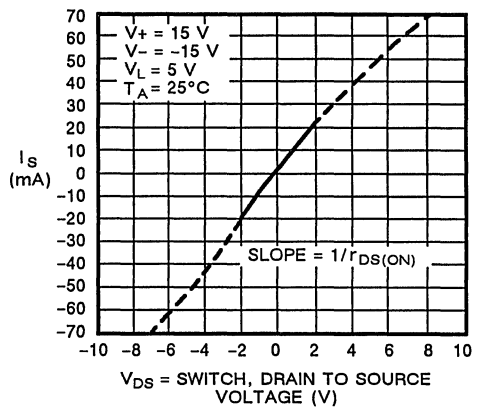


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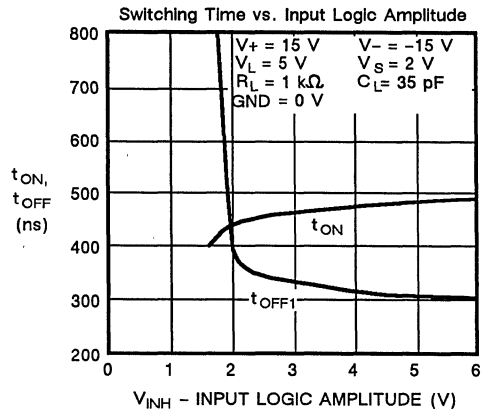
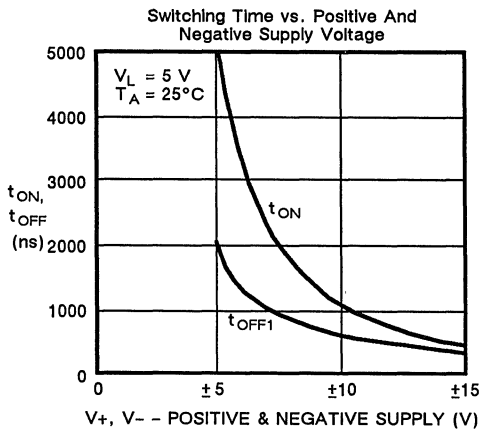
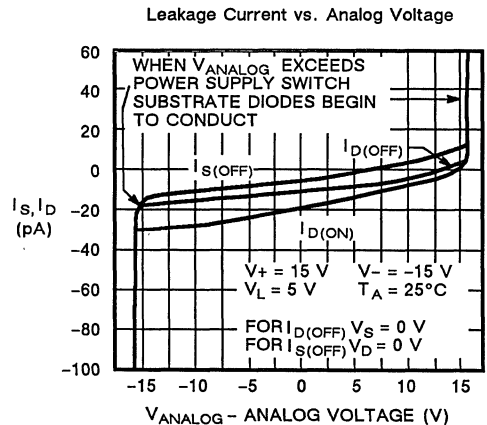
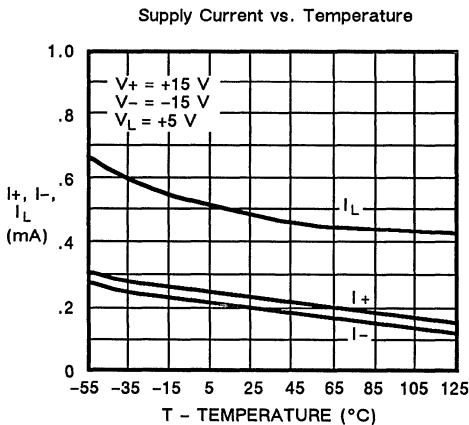
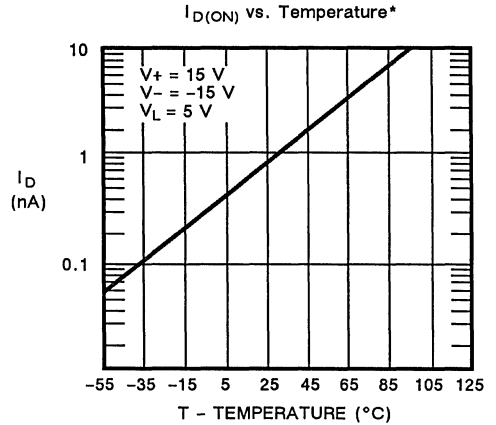
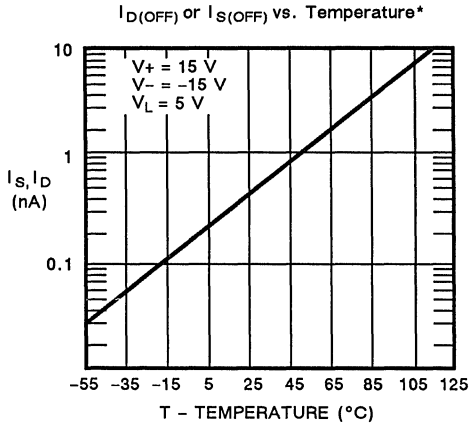
$r_{DS(ON)}$  vs.  $V_D$  and Power Supply Voltage



Switch Current vs. Switch Voltage



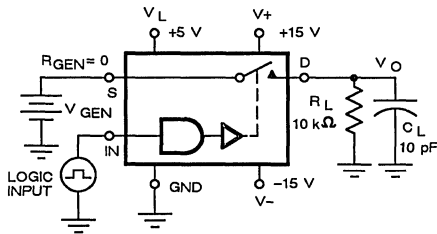
## TYPICAL CHARACTERISTICS (Cont'd)



\* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

**TYPICAL CHARACTERISTICS (Cont'd)**

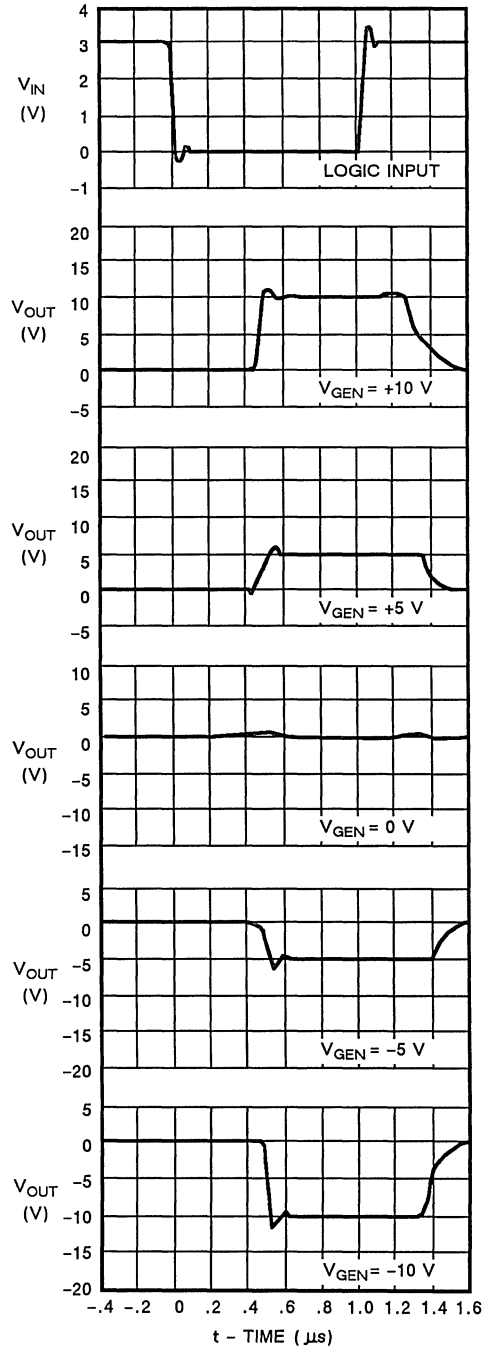
Typical delay, rise, fall settling times, and switching transients in this circuit.



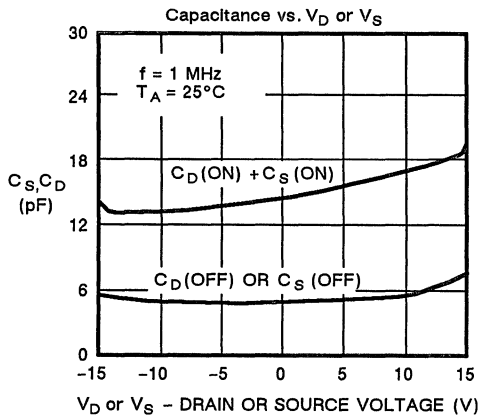
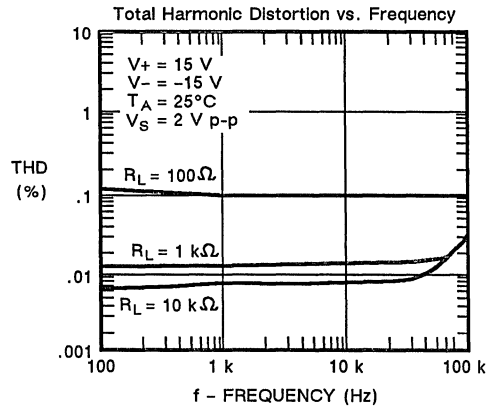
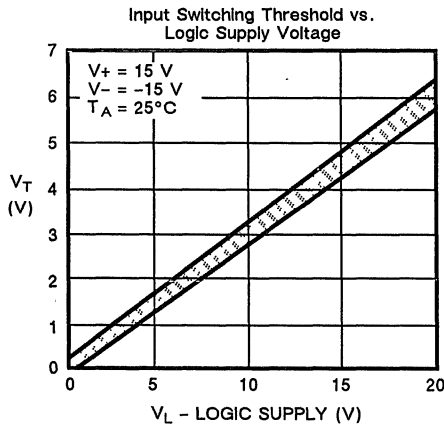
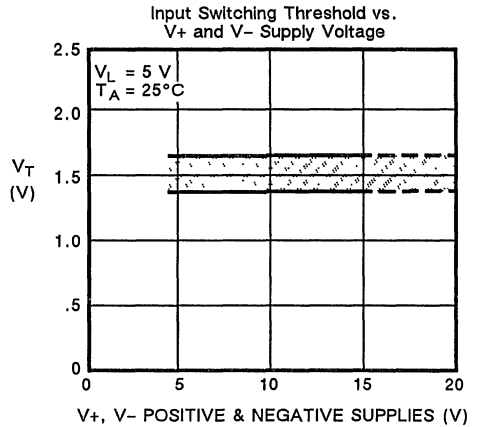
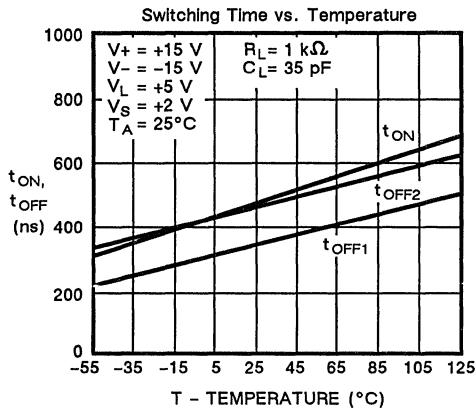
Turn-OFF time is primarily limited here by the RC time constant (50 ns) of the load.

If  $V_{GEN}$ ,  $R_L$  or  $C_L$  is increased, there will be a proportional increase in rise and/or fall RC times. Applying  $V_{GEN}$  to D rather than S results in much greater spikes.

DG211 Shown



## TYPICAL CHARACTERISTICS (Cont'd)

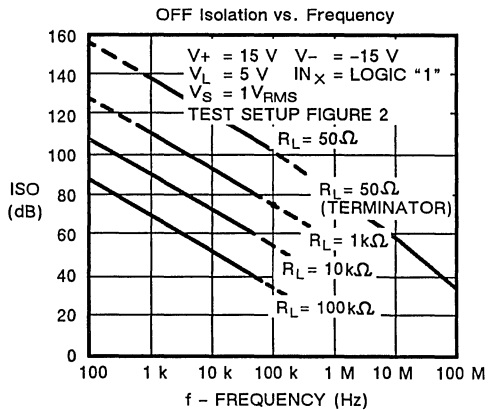
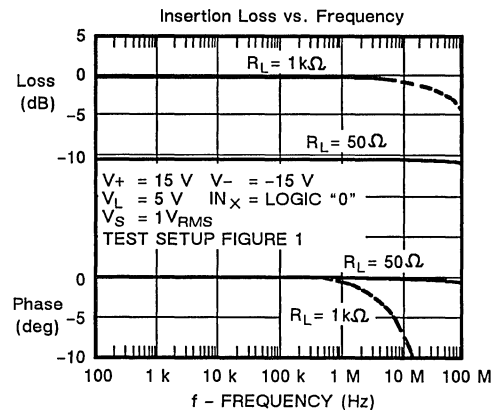
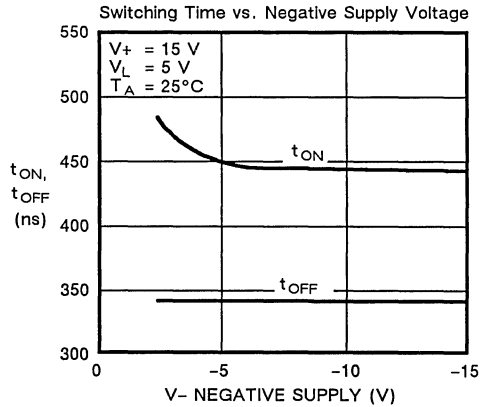
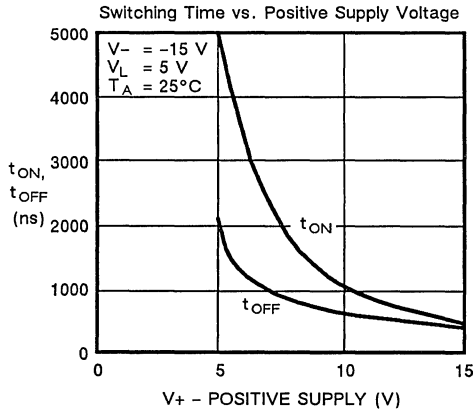
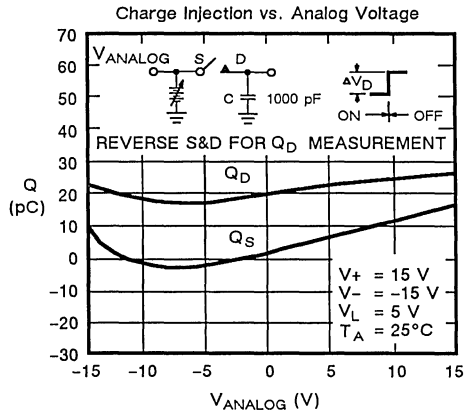
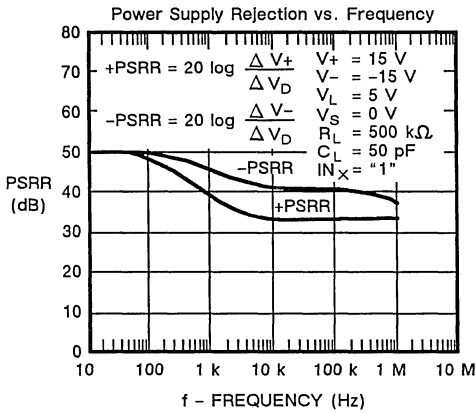


Some applications of the DG211 or DG212 will find the logic control inputs  $IN_X$  driven from the output of comparators or op-amps with nearly plus to minus 15 volt transitions. In these applications the user can shift the input logic transition voltage from the normal 1.6 V of TTL to zero volts by connecting the  $V_L$  pin to the GND pin. In this mode of operation the input offset voltage between  $IN_X$  and  $V_L$  (= GND) measure less than  $\pm 500\text{ mV}$ .

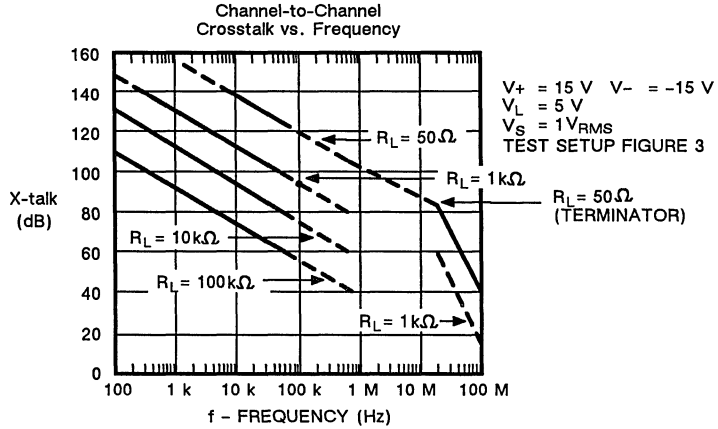
$V_L = 5\text{ V}$  presets the input threshold voltage for TTL logic compatibility. Improved noise immunity for CMOS logic compatibility results by connecting  $V_L$  to the  $V_{DD}$  terminal of the CMOS logic.



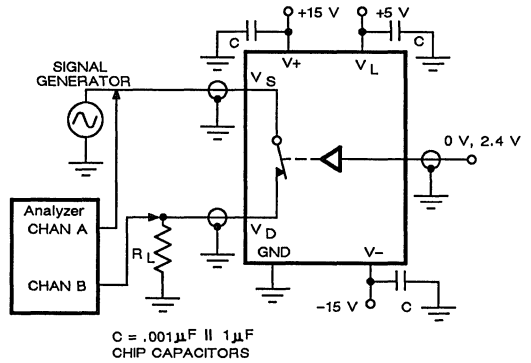
**TYPICAL CHARACTERISTICS (Cont'd)**



## TYPICAL CHARACTERISTICS (Cont'd)

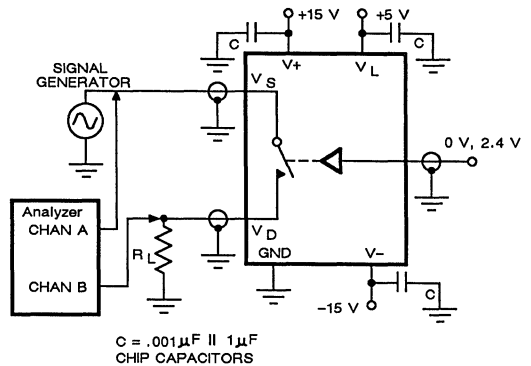


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 to 50 MHz	WAVETEK MOD 142	HP3575A GAIN-PHASE METER
1M to 100 MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER



**Figure 1. Testing Insertion Loss vs. Frequency**

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 to 50 MHz	HP3580A TRACKING OSC	HP3580A SPECTRUM ANALYZER
1M to 100 MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER
100k to 10 MHz	HP8568A TRACKING OSC	HP8568A SPECTRUM ANALYZER



**Figure 2. Testing OFF Isolation vs. Frequency**

**TYPICAL CHARACTERISTICS (Cont'd)**

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 to 50 MHz	HP3580A TRACKING OSC	HP3580A SPECTRUM ANALYZER
1M to 100 MHz	TEKTRONIX MOD 191	HP8405A VECTOR VOLT METER
100k to 10 MHz	HP8568A TRACKING OSC	HP8568A SPECTRUM ANALYZER

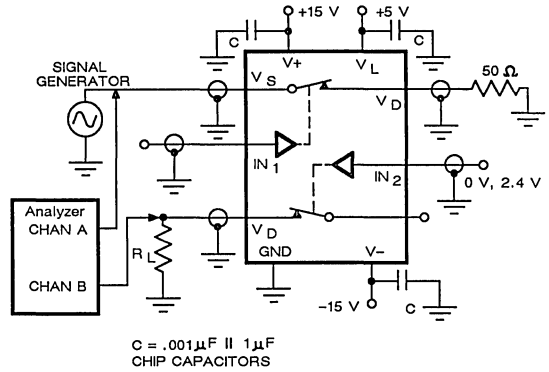
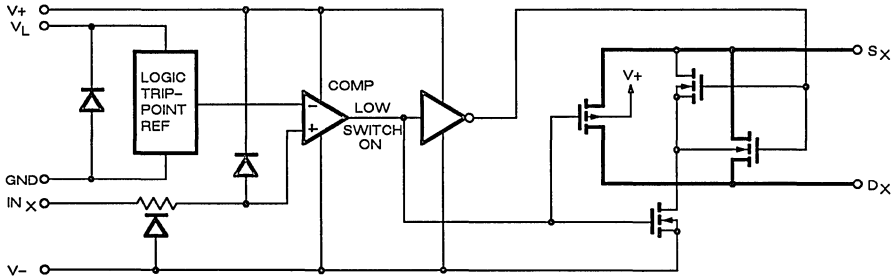


Figure 3. Testing Crosstalk vs. Frequency

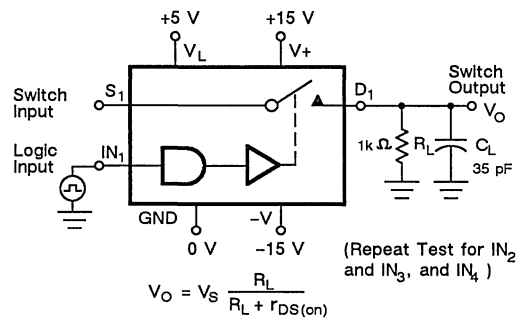
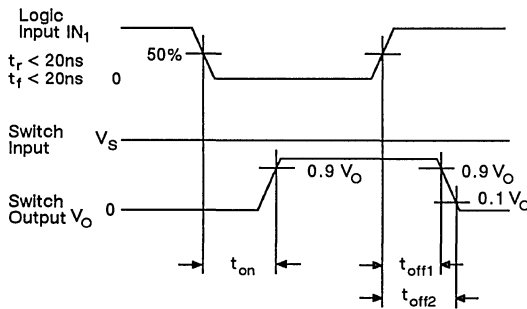
**SCHEMATIC DIAGRAM (Typical Channel)**



**5**

**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for  $V_S =$  constant with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



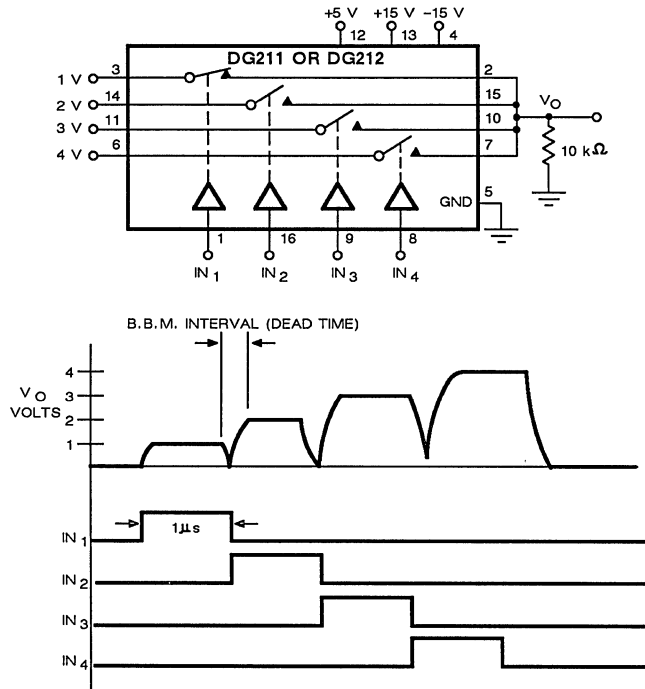


Figure 4. Four-Channel Analog Multiplexer

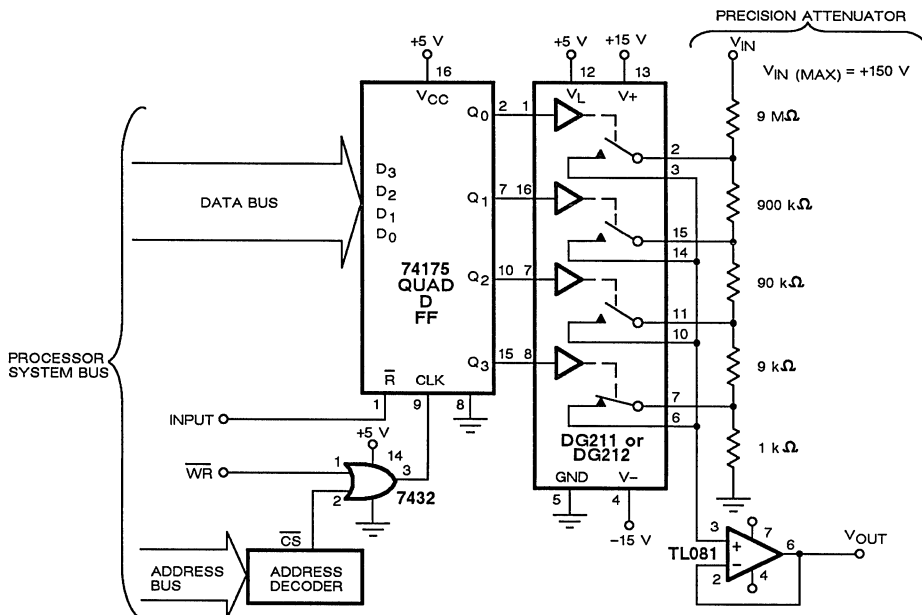


Figure 5. Microprocessor Controlled Analog Signal Attenuator

APPLICATIONS (Cont'd)

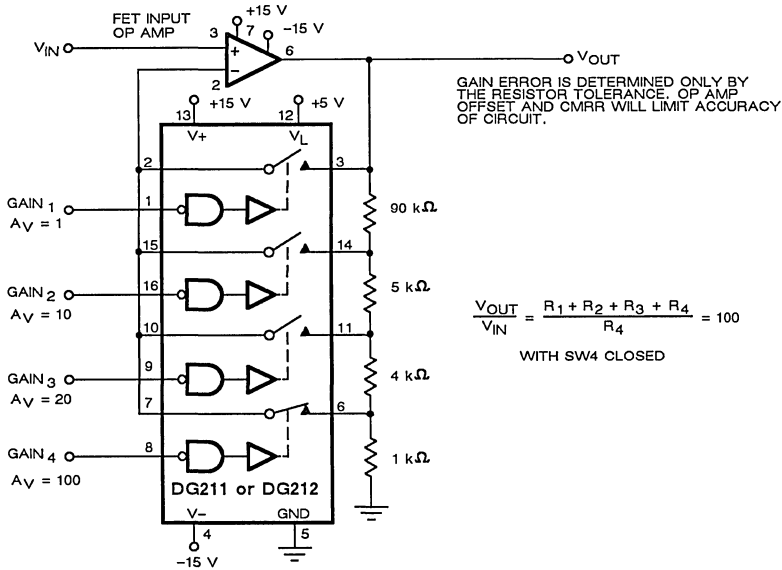


Figure 6. Precision-Weighted Resistor Programmable-Gain Amplifier

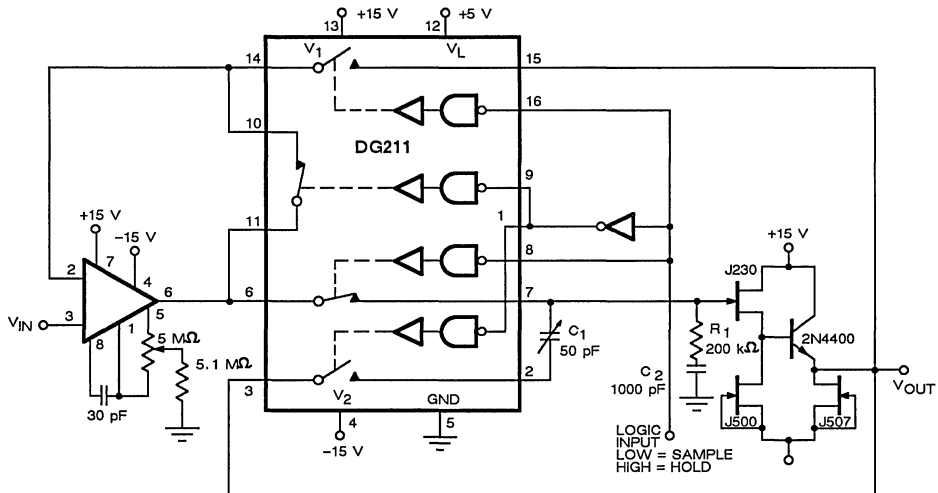


Figure 7. DG211 Sample-and-Hold

## APPLICATION HINTS\*

### DG211, DG212

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>L</sub> Logic Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
20	-20	5	2.4/0.8	-20 to 20
15	-15	5	2.4/0.8	-15 to 15
12	-12	5	2.4/0.8	-12 to 12
10	-10	5	2.4/0.8	-10 to 10
8**	-8	5	2.4/0.8	-8 to 8
10	-10	10	5/2	-10 to 10

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

\*\* Operation below ± 8 V is not recommended.

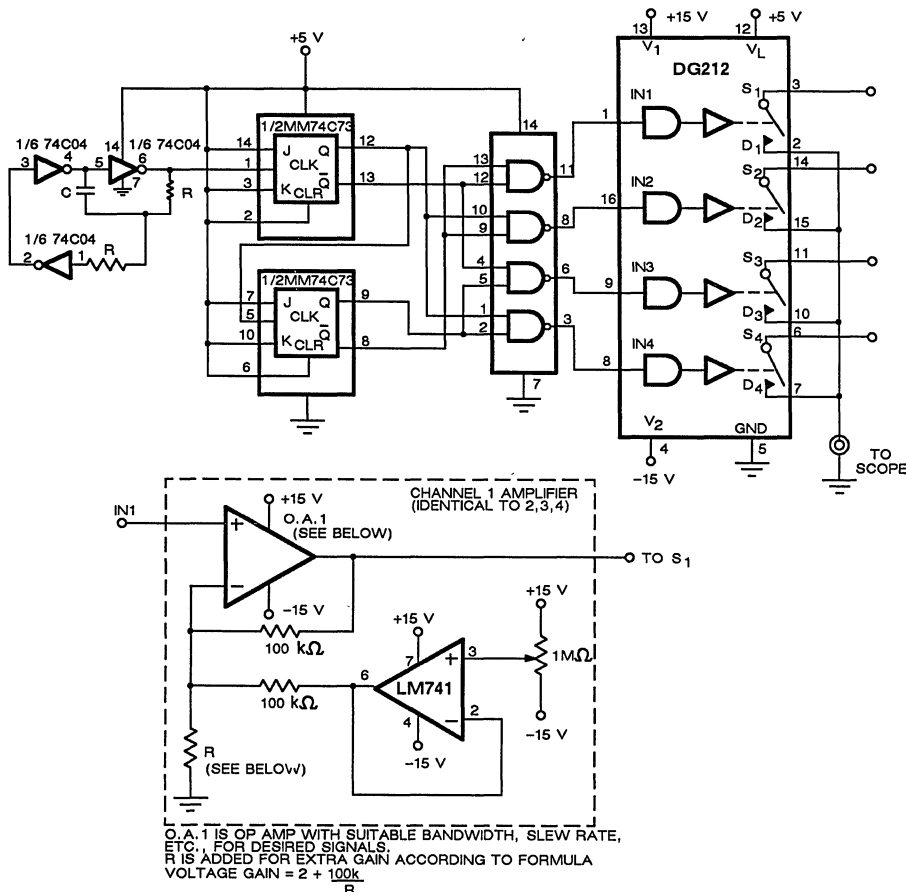


Figure 8. The "Scope Extender" Which Displays 4-Channels Simultaneously On A Single Trace Scope

# 4-Channel Monolithic SPST CMOS Analog Switch with Data Latches

## FEATURES

- Accepts 230 ns Write Pulse Width
- On Chip Regulator
- Built on PLUS-40 Process
- Latches Are Transparent with WR Low

## BENEFITS

- Compatible with Most  $\mu$ P Buses
- Allows Wide Power Supply Tolerance Without Affecting TTL Compatibility
- Reduced Power Supply Considerations
- Allows Flexibility of Design

## APPLICATIONS

- $\mu$ P Based Systems
- Automatic Test Equipment
- Communication Systems
- Data Acquisition Systems

## DESCRIPTION

The DG221 is a monolithic quad single-pole, single-throw analog switch designed for precision switching applications in communication, instrumentation and process control systems. Featuring independent onboard latches and a common WR pin, each DG221 can be memory mapped, and addressed as a single data byte for simultaneous switching.

Designed on the Siliconix PLUS-40 CMOS process to combine low power dissipation and ON resistance (60  $\Omega$  typ.) while handling continuous currents up to 20 mA. An epitaxial layer prevents latchup.

This device features true bidirectional performance in the ON condition, and will block signals to 30 V peak-to-peak in the OFF condition. ON resistance is extremely flat over the  $\pm 15$  V analog signal range.

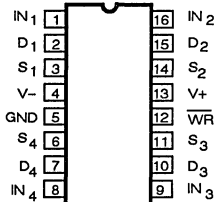
Packaging for this device includes 16-pin ceramic, plastic, and small outline options. Performance grades include military, A suffix (-55 to 125°C), both industrial, B and D suffix (-25, -40 to 85°C), and commercial, C suffix (0 to 70°C) temperature ranges.

**5**

## PIN CONFIGURATION

## FUNCTIONAL BLOCK DIAGRAM & TRUTH TABLE

Dual-In-Line Package



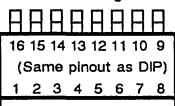
Top View

Order Numbers:

CerDIP: DG221AK, DG221AK/883,  
DG221BK, DG221CK

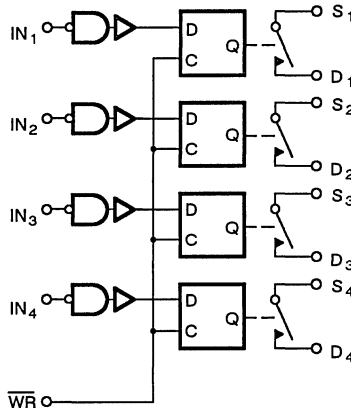
Plastic: DG221CJ

SO Package



Top View

Order Number:  
DG221DY



Four Latchable SPST Switches Per Package\*

\*Switches Shown for Logic "1" Input

Truth Table

IN <sub>x</sub>	$\overline{WR}$	SWITCH
0	0	ON
1	0	OFF
X	1	Maintains Previous State

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

$\overline{WR}$  input is level sensitive (not edge triggered)

## ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital inputs,  $\overline{WR}$ ,  $V_S$ ,  $V_D^f$  ... (V-) -2 V to (V+) +2 V or  
 ..... 20 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current S or D  
 (Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature (A & B Suffix) ..... -65 to 150°C  
 (C & D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
 (B Suffix) ..... -25 to 85°C  
 (C Suffix) ..... 0 to 70°C  
 (D Suffix) ..... -40 to 85°C

### Power Dissipation (Package)\*

16-Pin CerDIP\*\* ..... 900 mW  
 16-Pin Plastic DIP\*\*\* ..... 470 mW  
 16-Pin SO\*\*\*\* ..... 600 mW

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6.5 mW/°C above 75°C.

\*\*\*\* Derate 7.7 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = +15\text{ V}$ $V_- = -15\text{ V}$ $GND = \overline{WR} = 0\text{ V}$		LIMITS						UNIT
				1=25°C		A SUFFIX		B, C, D SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY</b>										
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$			1, 2, 3		-15	15	-15	15	V
Drain-Source <sup>e</sup> ON Resistance	$r_{DS(ON)}$	$V_{IN} = 0.8\text{ V}$ $I_S = -1\text{ mA}$	$V_D = 10\text{ V}$	1, 3 2	60		90 135		90 135	$\Omega$
			$V_D = -10\text{ V}$	1, 3 2	70		90 135		90 135	
Source OFF Leakage Current	$I_{S(OFF)}$	$V_{IN} = 2.4\text{ V}$	$V_S = 14\text{ V}$ $V_D = -14\text{ V}$	1 2	0.01		1 100		5 100	nA
			$V_S = -14\text{ V}$ $V_D = 14\text{ V}$	1 2	-0.02	-1 -100		-5 -100		
Drain OFF Leakage Current	$I_{D(OFF)}$		$V_S = -14\text{ V}$ $V_D = 14\text{ V}$	1 2	0.01		1 100		5 100	
			$V_S = 14\text{ V}$ $V_D = -14\text{ V}$	1 2	-0.02	-1 -100		-5 -100		
Drain ON Leakage Current	$I_{D(ON)}$	$V_{IN} = 0.8\text{ V}$	$V_D = V_S = 14\text{ V}$	1 2	0.1		1 200		5 200	
			$V_D = V_S = -14\text{ V}$	1 2	-0.15	-1 -200		-5 -200		
<b>INPUT</b>										
Input Current with Input Voltage HIGH	$I_{INH}$ $I_{\overline{WRH}}$	$V_{IN} = 2.4\text{ V}$	1 2	-0.0001		-1 -10		-1 -10		$\mu\text{A}$
		$V_{IN} = 15\text{ V}$	1 2	0.003		1 10		1 10		
Input Current with Input Voltage LOW	$I_{INL}$ $I_{\overline{WRL}}$	$V_{IN} = 0\text{ V}$	1 2	-0.0004		-1 -10		-1 -10		



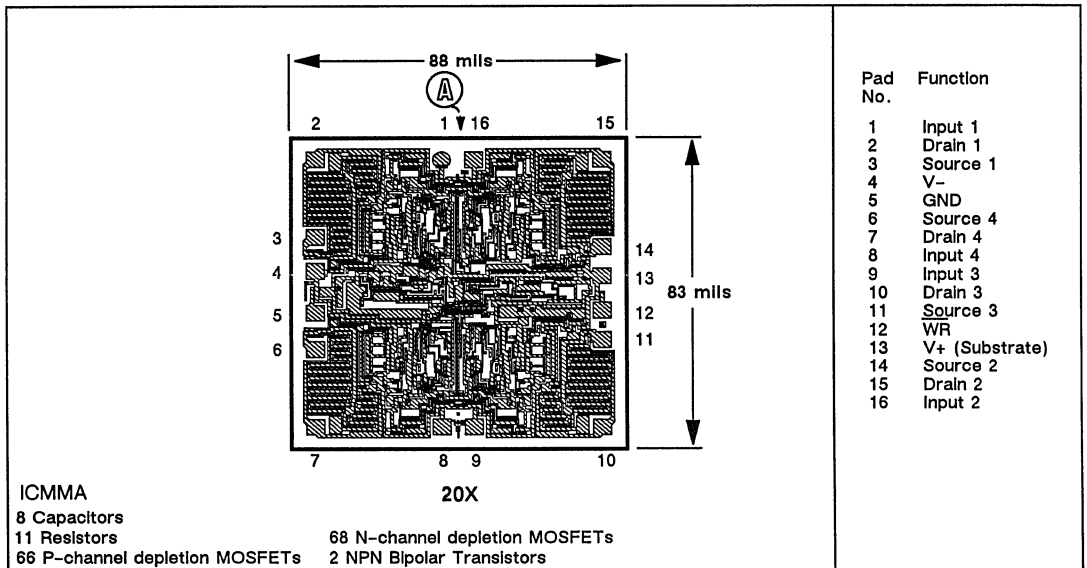
**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = +15\text{ V}$ $V_- = -15\text{ V}$ $GND = WR = 0\text{ V}$	LIMITS						UNIT	
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		A SUFFIX -55 to 125°C		B,C,D SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC</b>										
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit Figure 1	1			550		550	ns	
Turn-OFF Time	$t_{OFF}$		1			340		340		
Turn-ON Time Write	$t_{ON, \overline{WR}}$	See Switching Time Test Circuit Figure 2	1			550		550		
Turn-OFF Time Write	$t_{OFF, \overline{WR}}$		1			340		340		
Charge Injection	Q	$C_L = 1000\text{ pF}, V_{gen} = 0\text{ V}$ $R_{gen} = 0\ \Omega$	1	20					pC	
Source-OFF Capacitance	$C_{S(OFF)}$	$f = 1\text{ MHz}$	1	8					pF	
Drain-OFF Capacitance	$C_{D(OFF)}$									$V_S = 0\text{ V}$ $V_{IN} = 5\text{ V}$
Channel ON Capacitance	$C_{D(ON)} + C_{S(ON)}$									$V_D = V_S = 0\text{ V}$ $V_{IN} = 0\text{ V}$
OFF Isolation		$V_{IN} = 5\text{ V}$	1	70					dB	
Interchannel Crosstalk Isolation		$V_S = 1\text{ V}_{p-p}, f = 100\text{ kHz}$ $C_L = 15\text{ pF}, R_L = 1\text{ k}\Omega$	1	90					dB	
<b>SUPPLY</b>										
Positive Supply Current	I+	All Channels ON or OFF $V_{IN} = 0\text{ V}$ or $2.4\text{ V}$	1	0.8		1.5		1.5	mA	
Negative Supply Current	I-		1	-0.4	-1		-1			

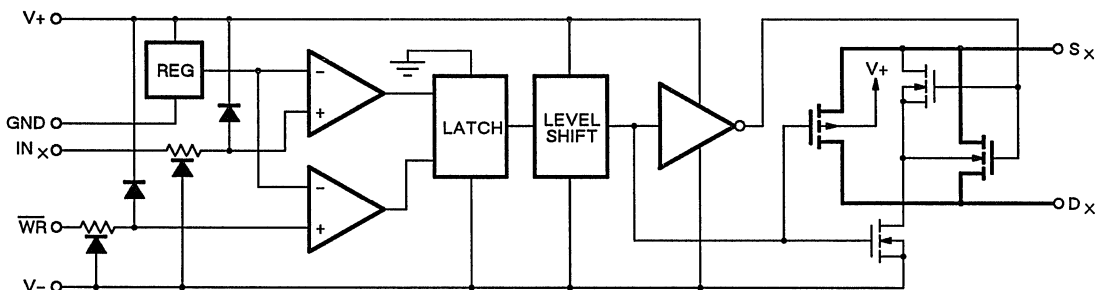
**NOTES:**

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- $\Delta r_{DS(ON)}$  is guaranteed to be within  $\pm 5\%$  switch-to-switch within a package (not a tested parameter).
- Signal on  $S_X, D_X, WR, IN_X$  exceeding  $V_+$  or  $V_-$  will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

## DIE TOPOGRAPHY



## FUNCTIONAL SCHEMATIC (Single Channel Shown)



**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

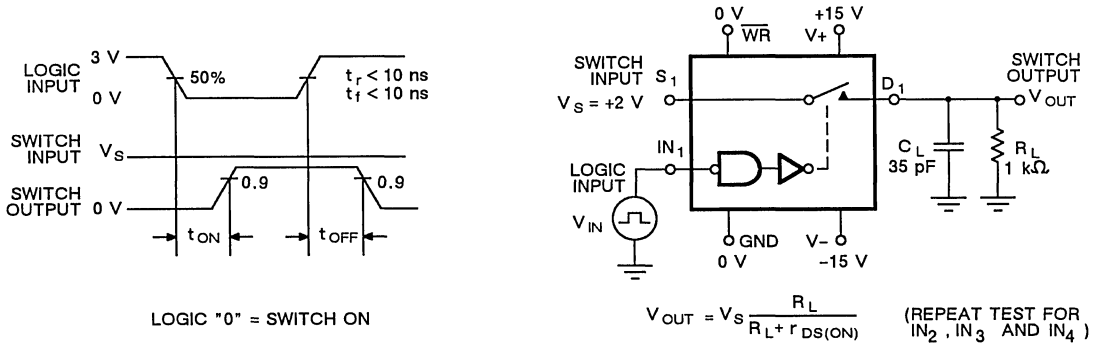


Figure 1

**$\overline{WR}$  SWITCHING TIME TEST CIRCUIT**

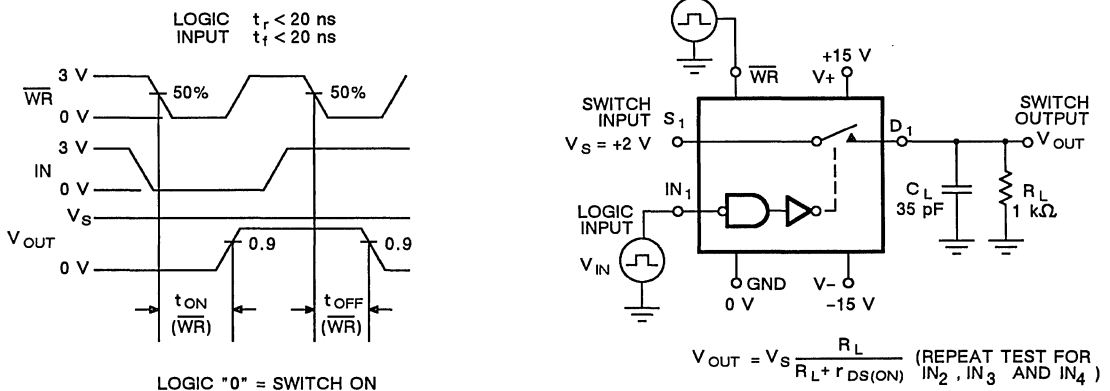


Figure 2

**$\overline{WR}$  SETUP CONDITIONS**

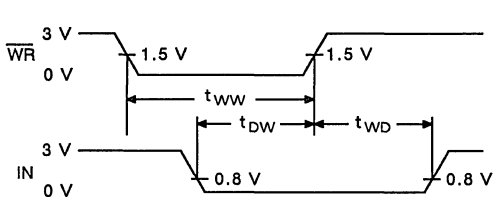
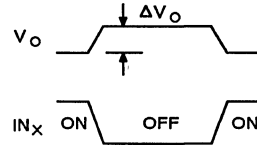
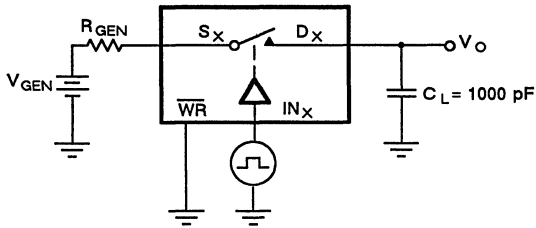


Figure 3

**$\overline{WR}$ /INPUT MINIMUM TIMING REQUIREMENTS**

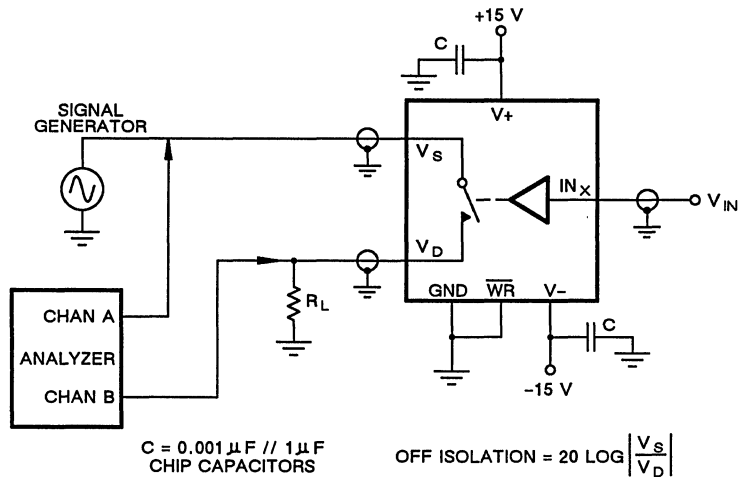
PARAMETER	MIN LIMIT	UNIT
Write Pulse Width	$t_{WW}$	230
Data Valid to Write	$t_{DW}$	180
Data Valid After Write	$t_{WD}$	30

## CHARGE INJECTION TEST CIRCUIT

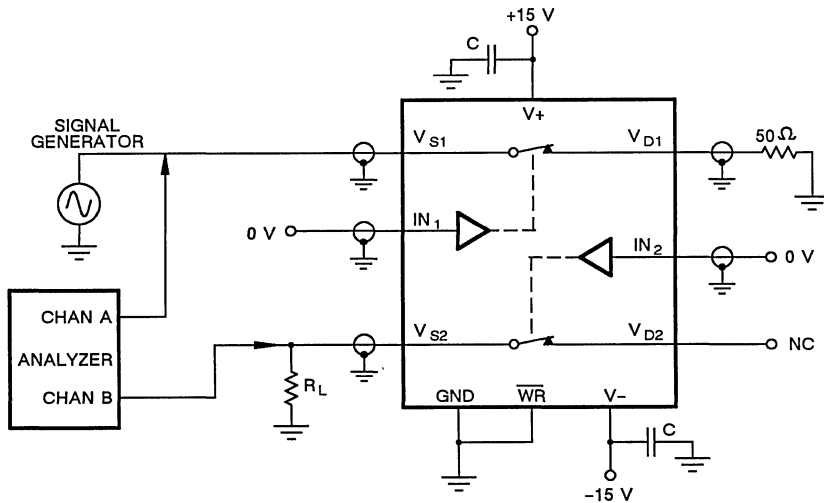


$\Delta V_O$  = measured voltage error due to charge injection.  
The error voltage in coulombs is  $\Delta Q = C_L \times \Delta V_O$ .

## OFF ISOLATION TEST CIRCUIT



**CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT**



$C = 0.001 \mu F \parallel 1 \mu F$   
CHIP CAPACITORS

$$CCRR = 20 \text{ LOG} \left| \frac{V_{S1}}{V_{D2}} \right|$$

**APPLICATION HINTS**

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND (V)	$\overline{WR}$ (V)	Input Logic Voltage (V)	Analog Signal Range (V)
15	-15	0	0.8/2.4	0.8/2.4	±15
20	-20	0	0.8/2.4	0.8/2.4	±20
10	-10	0	0.8/2.4	0.8/2.4	±10
10	-5	0	0.8/2.4	0.8/2.4	+10/-5

IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	$\overline{WR}$ *	ON Switch
0	0	0	0	0	All
1	1	1	1	0	None
0	1	1	1	0	1
1	0	1	1	0	2
1	1	0	1	0	3
1	1	1	0	0	4

$\overline{WR}$	IN <sub>1</sub>	IN <sub>2</sub>	IN <sub>3</sub>	IN <sub>4</sub>	Gain
0	0	1	1	1	0.1
0	1	0	1	1	0.01
0	1	1	0	1	0.001
0	1	1	1	0	0.0001

\*  $\overline{WR}$  may be held at "0" for temporary operation similar to DG201A's. With  $\overline{WR}$  at "0" SW1 will remain ON as long as "IN<sub>1</sub>" is held at "0".

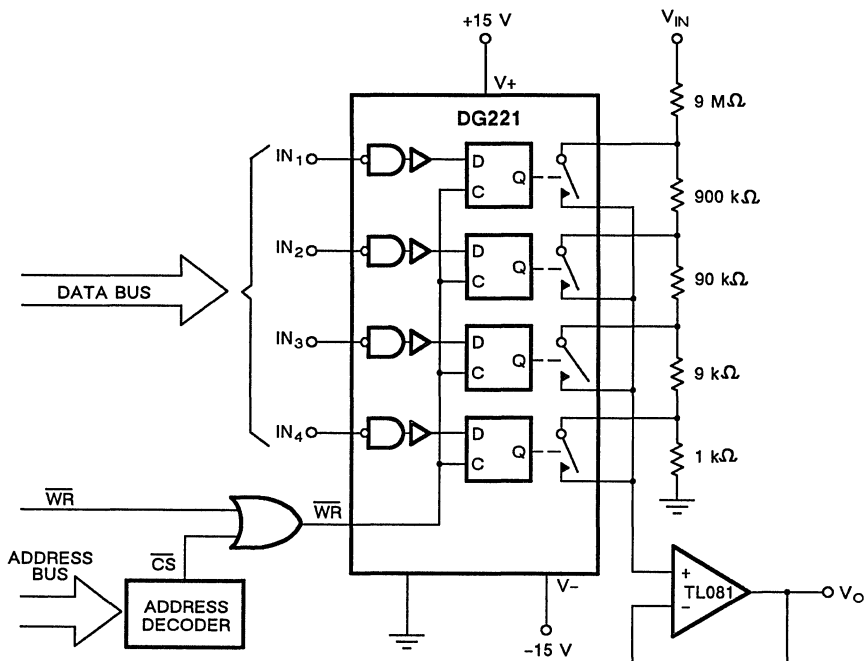


Figure 4.  $\mu$ P Controlled Analog Signal Attenuator

The TL081 is used as unity gain buffer while DG221 selected voltage divider provides attenuation.

# Monolithic General Purpose CMOS Analog Switch

## FEATURES

- PLUS-40 Process
- Make-Before-Break Operation
- Full Rail-to-Rail Analog Signal Range
- True TTL Compatibility

## BENEFITS

- Reduced Power Supply Considerations
- Reduced Switching Noise
- Reduced Need for Buffers
- Pull-Up Resistors Not Required

## APPLICATIONS

- Programmable Gain Amplifiers
- Analog Multiplexing
- Servo Control Systems

## DESCRIPTION

The DG243 is a monolithic dual SPDT analog switch designed for general switching applications in communication, instrumentation, and process control systems. Featuring make-before-break action, the DG243 can be used in closed loop systems to switch gain or bandwidth networks without opening the loop.

The DG243 is designed on the Siliconix PLUS-40 CMOS process to combine low power dissipation

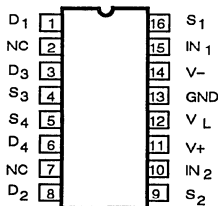
with a high breakdown voltage rating of 40 V. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 Volts peak-to-peak when OFF. ON resistance is fairly flat over the full  $\pm 15$  V analog signal range.

Packaging for this device includes a 16-pin CerDIP and plastic options. Performance grades include military, A suffix ( $-55$  to  $125^{\circ}\text{C}$ ) and commercial, C suffix ( $0$  to  $70^{\circ}\text{C}$ ) temperature ranges.

## PIN CONFIGURATION

Dual-In-Line Package



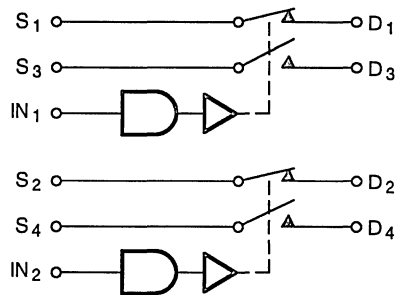
Top View

Order Numbers:

CerDIP: DG243AK, DG243AK/883

Plastic: DG243CK, DG243CJ

## FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package\*

Truth Table

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.0$  V

\*Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

Voltages referenced to V-

V+ ..... 44 V

V<sub>L</sub> ..... (GND -0.3 V) to 44 V

GND ..... 25 V

Digital Inputs<sup>a</sup> V<sub>S</sub>, V<sub>D</sub> ..... -2 V to (V+ +2V) or  
 ..... 30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA

Peak Current, S or D  
 (Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C  
 (C Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
 (C Suffix) ..... 0 to 70°C

Power Dissipation\*

16-Pin CerDIP\*\* ..... 900 mW

16-Pin Plastic DIP\*\*\* ..... 450 mW

\* All leads soldered or welded to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V <sub>L</sub> = 5 V	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = ± 10 V I <sub>S</sub> = 10 mA	1,3 2	30		50 75		50 75	Ω
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	0.2		1 100		1 100	nA
		V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	-0.3	-1 -100		-1 -100		
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	0.17		1 100		1 100	
		V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	-0.35	-1 -100		-1 -100		
Drain ON Leakage Current	I <sub>D(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	1 2	0.05		2 200		2 200	
		V <sub>S</sub> = V <sub>D</sub> = -14 V	1 2	-0.04	-2 -200		-2 -200		
<b>INPUT</b>									
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 2.0 V	1 2	-0.01	-1 -1	1 1	-1 -1	1 1	μA
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0.8 V	1 2	-0.005	-1 -1	1 1	-1 -1	1 1	

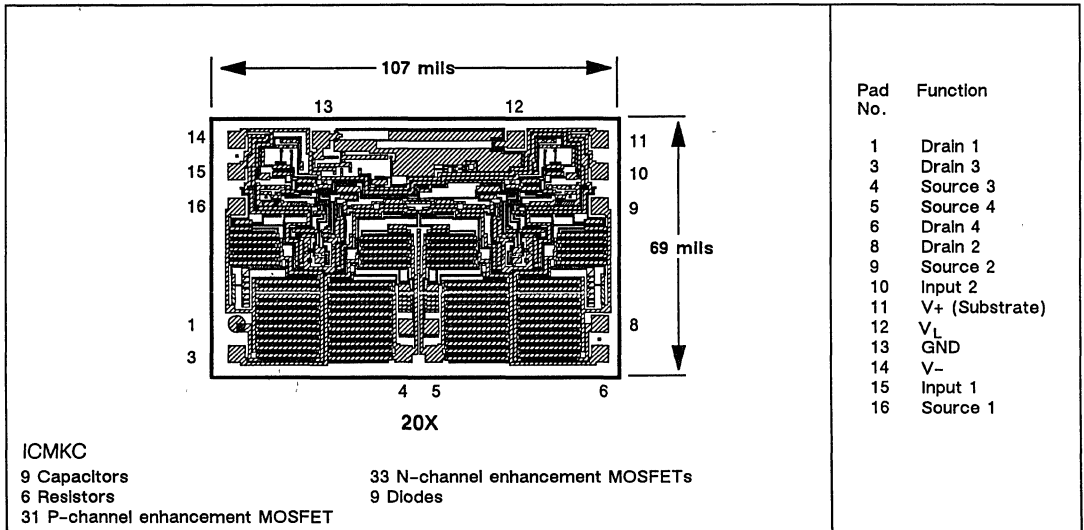


ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V <sub>L</sub> = 5 V	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1	250		500		700	ns
Turn-OFF Time	t <sub>OFF</sub>		1	390		1000		1200	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>gen</sub> = 0 V R <sub>gen</sub> = 0 Ω	1	60					pC
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V V <sub>IN</sub> = 0 V f = 1 MHz	1	15					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		1	17					
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		1	45					
OFF Isolation <sup>e</sup>		V <sub>IN</sub> = 5 V, Z <sub>L</sub> = 75 Ω	1	75					dB
Crosstalk (Channel-to-Channel)		V <sub>S</sub> = 2.0 V, f = 1MHz	1	89					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	All Channels ON or OFF	1	180		300		300	μA
Negative Supply Current	I <sub>-</sub>		1	-150	-300		-300		
Logic Supply Current	I <sub>L</sub>		1	100		300		300	
Ground Supply Current	I <sub>GND</sub>		1	-140	-300		-300		

**NOTES:**

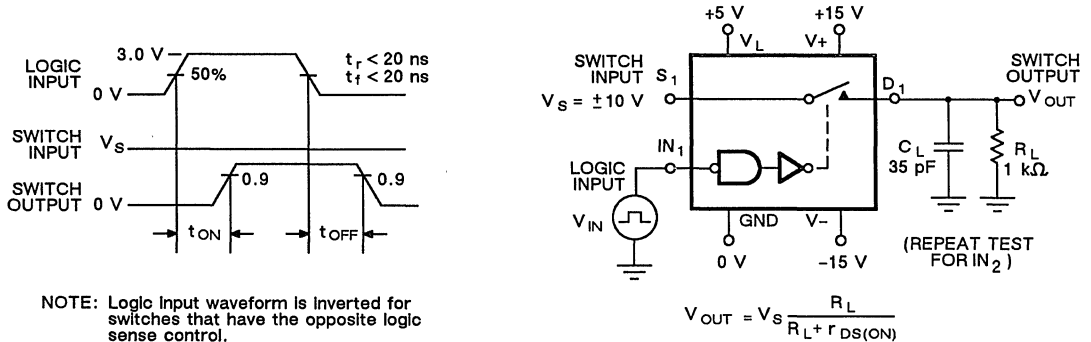
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = input voltage to perform proper function.  
 For Logic "1" - V<sub>INH</sub> = 2.0 V  
 For Logic "0" - V<sub>INL</sub> = 0.8 V

## DIE TOPOGRAPHY

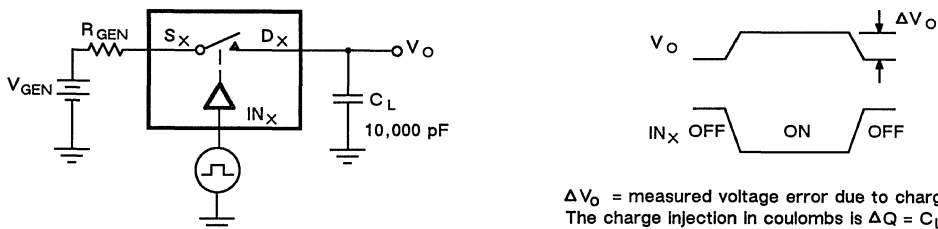


## SWITCHING TIME TEST CIRCUIT

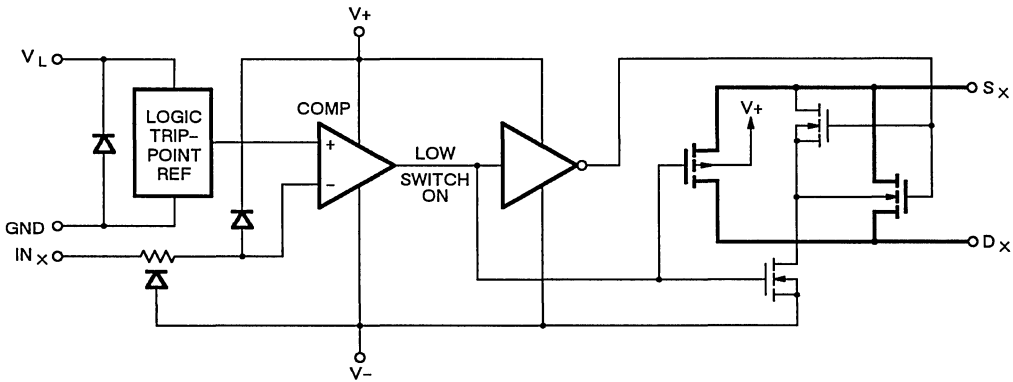
Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



## CHARGE INJECTION TEST CIRCUIT



**SCHEMATIC DIAGRAM (Typical Channel)**



**APPLICATIONS**

The make-before-break operation of the DG243 provides simple transient suppression in these two important applications.

Figure 1 shows a minimum amount of glitching during changes of gain states. The relatively low

impedance of the gain setting resistors 10 k $\Omega$ , 1 k $\Omega$ , 100  $\Omega$  shunt the injected charge to ground minimizing transient effects occurring at the inverting input of the op amp. Consequently, these transients are not amplified to V<sub>OUT</sub>.

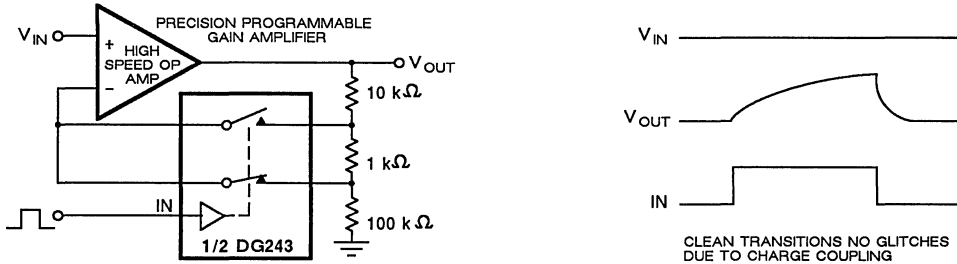


Figure 1. Improving Transient Response in Programmable Gain Amplifiers. "Getting Rid of Glitches".

Figure 2 takes advantage of the make-before-break operation of the DG243 by shorting transition current to real ground instead of virtual ground. The

best results are obtained by selecting an op amp with the proper offset voltage specification.

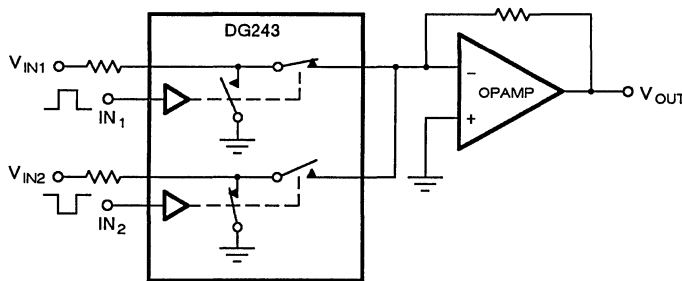


Figure 2. Minimizing Glitches in Audio Switching

## High-Speed Quad Monolithic SPST CMOS Analog Switch

### FEATURES

- Fast Switching  
 $t_{ON}, t_{OFF} < 60 \text{ ns}$
- Charge Injection  $< 9 \text{ pC}$
- $r_{DS(ON)} < 50 \Omega$
- TTL Compatible

### BENEFITS

- Faster System Operation
- Reduced Switching Glitches
- Low Impedance Operation

### APPLICATIONS

- High Speed Switching
- Sample/Hold
- Digital Filters
- Op Amp Gain Switching
- Disk Drives

### DESCRIPTION

The DG271 high speed quad single-pole single-throw analog switch is intended for applications that require low ON resistance ( $r_{DS(ON)} < 50 \Omega$ ), low leakage currents ( $I_{S(ON)} < 1 \text{ nA}$ ), and fast switching speeds ( $t_{ON} < 60 \text{ ns}$ ).

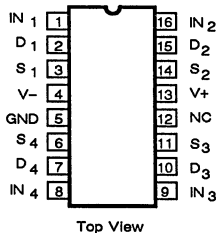
Built on Siliconix' proprietary high voltage silicon gate process to achieve superior ON/OFF performance, each switch conducts equally well in

both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. An epitaxial layer prevents latchup.

Packaging for this device includes the 20-pin LCC, 16-pin CerDIP, plastic DIP, and small outline options. Performance grades include military, A suffix ( $-55$  to  $125^\circ\text{C}$ ), commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ), and both industrial, B and D suffixes ( $-25$ ,  $-40$  to  $85^\circ\text{C}$ ) temperature ranges.

### PIN CONFIGURATION

Dual-In-Line Package

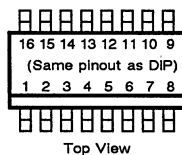


Order Numbers:

CerDIP: DG271AK, DG271AK/883  
DG271BK, DG271CK

Plastic: DG271CJ

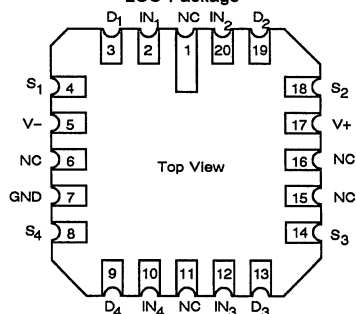
SO Package



Order Number:

DG271DY

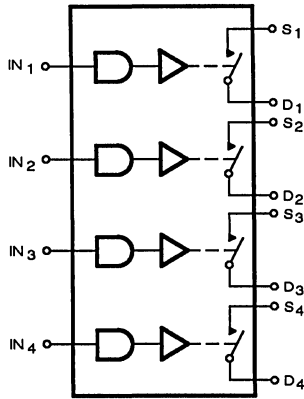
LCC Package



Order Number:  
DG271AZ/883

**FUNCTIONAL BLOCK DIAGRAM**

**TRUTH TABLE**



Four SPST Switches per Package\*

LOGIC	SWITCH
0	ON
1	OFF

Logic "0"  $\leq$  0.8 V

Logic "1"  $\geq$  2.0 V

\*Switches Shown for Logic "1" Input

**ABSOLUTE MAXIMUM RATINGS**

V+ to V- ..... 44 V  
 GND to V- ..... 25 V  
 Digital Inputs<sup>9</sup> V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2 V or  
 ..... 20 mA, whichever occurs first.  
 Current, Any Terminal Except S or D ..... 30 mA  
 Continuous Current, S or D ..... 20 mA  
 Peak Current, S or D  
 (Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA  
 Storage Temperature (A, B & D Suffix) .... -65 to 150°C  
 (C Suffix) ..... -65 to 125°C  
 Operating Temperature (A Suffix) ..... -55 to 125°C  
 (B Suffix) ..... -25 to 85°C

(C Suffix) ..... 0 to 70°C  
 (D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*  
 16-Pin CerDIP\*\* ..... 900 mW  
 16-Pin Plastic DIP\*\*\* ..... 470 mW  
 16-Pin Plastic SO\*\*\*\* ..... 600 mW  
 20-Pin LCC\*\*\*\*\* ..... 750 mW

- \* Device mounted with all leads soldered or welded to PC board.
- \*\* Derate 12 mW/°C above 75°C.
- \*\*\* Derate 6.5 mW/°C above 75°C.
- \*\*\*\* Derate 7.6 mW/°C above 75°C.
- \*\*\*\*\* Derate 7.6 mW/°C above 75°C.

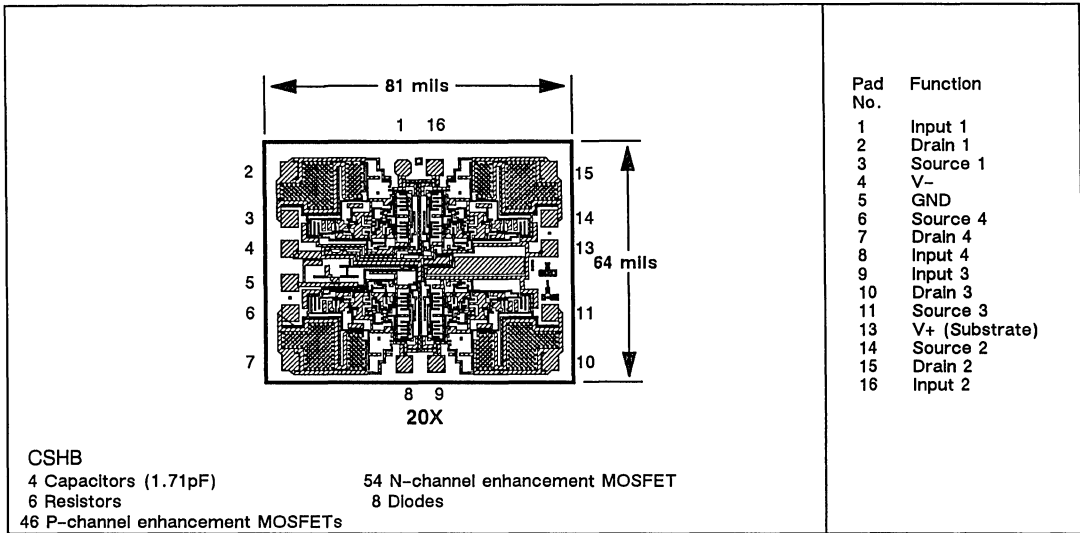
ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT	
			1=25°C 2=125,85,70°C 3=-55,-40,-25,0°C		A SUFFIX -55 to 125°C		B,C,D SUFFIX 0 to 70°C -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = 1 mA, V <sub>IN</sub> = 0.8 V V <sub>D</sub> = ± 10 V	1 2,3	32		50 75		50 75	Ω	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 2.0 V	V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2,3	0.05		1 100		1 100	nA
			V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2,3	0.05	-1 -100		-1 -100		
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>IN</sub> = 2.0 V	V <sub>D</sub> = 14 V V <sub>S</sub> = -14 V	1 2,3	0.05		1 100		1 100	
			V <sub>D</sub> = -14 V V <sub>S</sub> = 14 V	1 2,3	0.05	-1 -100		-1 -100		
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>IN</sub> = 0.8 V	V <sub>D</sub> = V <sub>S</sub> = 14 V	1 2,3	0.05		1 200		1 200	
			V <sub>D</sub> = V <sub>S</sub> = -14 V	1 2,3	0.05	-1 -200		-1 -200		
<b>INPUT</b>										
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 2.0 V	1 2,3	0.010	-1 -10		-1 -10		μA	
		V <sub>IN</sub> = 15 V	1 2,3	0.010		1 10		1 10		
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1 2,3	0.010	-1 -10		-1 -10			
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1 2,3	50		60 75		60 75	ns	
Turn-OFF Time	t <sub>OFF</sub>		1 2,3	45		60 75		60 75		
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>gen</sub> = 0 V R <sub>gen</sub> = 0 Ω	1	9					pC	
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	All Channels ON or OFF	1 2,3	4.3		7.5 11		7.5 11	mA	
Negative Supply Current	I <sub>-</sub>		1 2,3	-3.4	-6 -10		-6 -10			

**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

**NOTES:**

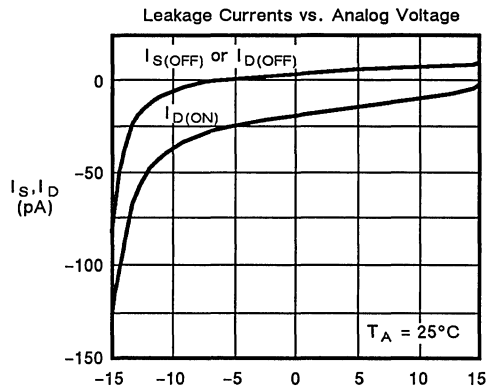
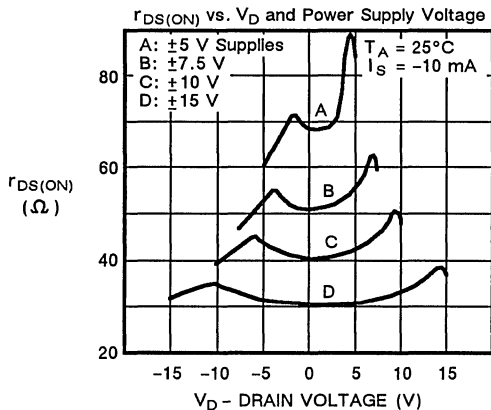
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e.  $V_{IN}$  = Input voltage to perform proper function.  
For Logic "1" -  $V_{INH} = 2.0$  V  
For Logic "0" -  $V_{INL} = 0.8$  V

**DIE TOPOGRAPHY**

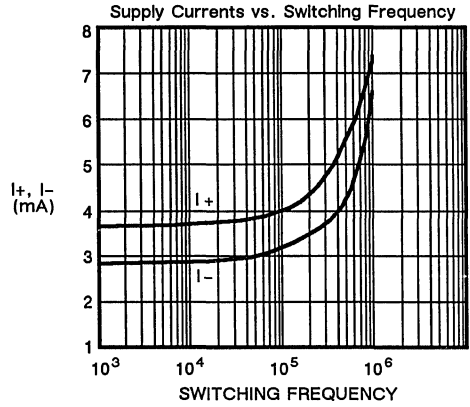
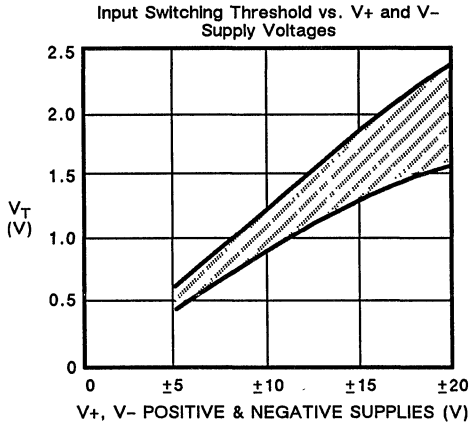


**5**

**TYPICAL CHARACTERISTICS**

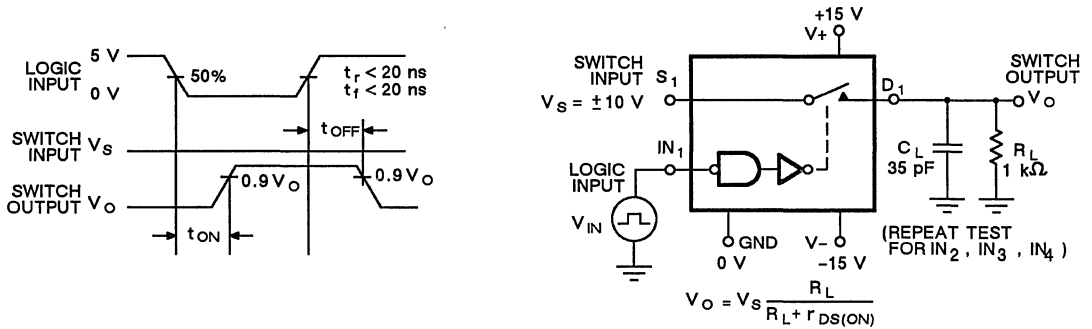


## TYPICAL CHARACTERISTICS (Cont'd)

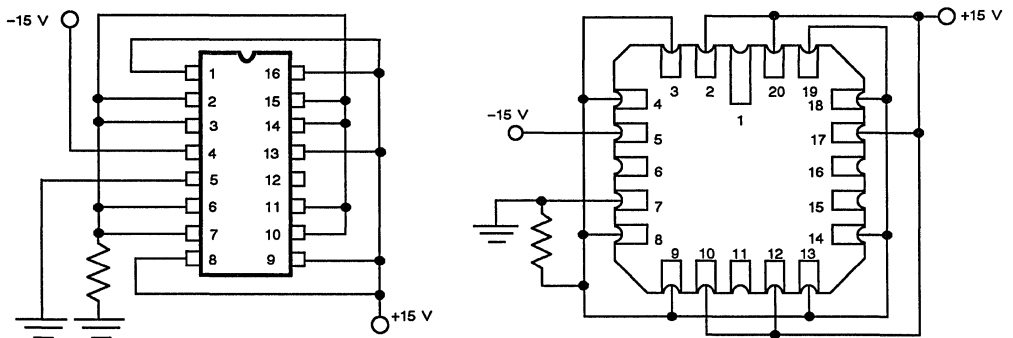


## SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



## BURN-IN CIRCUIT



Note: All Resistors are 10 k  $\Omega$  unless otherwise specified

Note: LCC package uses same circuit and conditions as the DIP



# DG300A/301A/302A/303A CMOS Analog Switches

## FEATURES

- Analog Signal Range  $\pm 15\text{ V}$
- Fast Switching ( $< 250\text{ ns}$ )
- Low  $r_{DS(ON)}$  ( $< 50\ \Omega$ )
- Single Supply Operation
- Latchproof CMOS

## BENEFITS

- Full Rail to Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

## APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Operated Circuits

## DESCRIPTION

The DG300A-DG303A family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

Designed on the Siliconix PLUS-40 CMOS process, these switches are latch proof, and are designed to block up to 30 Volts peak-to-peak when OFF. An epitaxial layer prevents latchup.

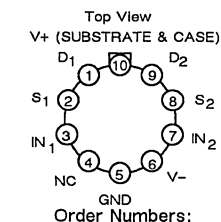
In the ON condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their fairly flat ON resistance.

Featuring low power consumption (a few mW) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are quasi TTL and CMOS compatible. Single supply operation is allowed by connecting the  $V^-$  rail to 0 volts.

Package options for this series include 14-pin CerDIP and plastic DIP. Performance grades include the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ), commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ), and industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ) temperature ranges. Additionally, the DG300A and DG301A are available in 10-pin metal cans, while the DG301A and DG303A are available in 20-pin LCC packages.

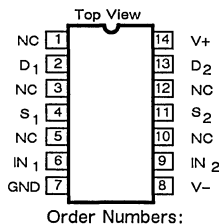
## PIN CONFIGURATION

### Metal Can Package



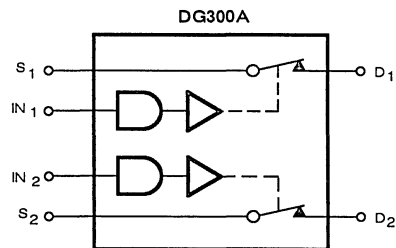
CerDIP: DG300AAA, DG300AAA/883  
DG300ABA, DG300ACA

### Dual-In-Line Package



CerDIP: DG300AAK, DG300AAK/883  
DG300ABK, DG300ACK  
Plastic: DG300ACJ

## FUNCTIONAL BLOCK DIAGRAM



LOGIC	SWITCH
0	OFF
1	ON

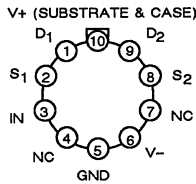
Logic "0"  $\leq 0.8\text{ V}$   
Logic "1"  $\geq 4.0\text{ V}$

Switches Shown for Logic "1" Input

## PIN CONFIGURATION (Cont'd)

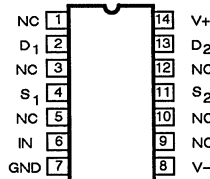
## FUNCTIONAL BLOCK DIAGRAM (Cont'd)

**Metal Can Package**  
Top View

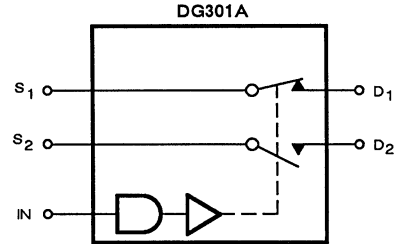


Order Numbers:  
DG301AAA, DG301AAA/883  
DG301ABA, DG301ACA

**Dual-In-Line Package**  
Top View



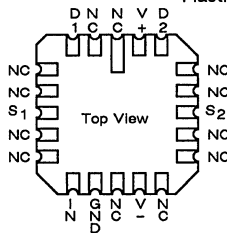
Order Numbers:  
CerDIP: DG301AAK, DG301AAK/883  
DG301ACK, DG301ABK  
Plastic: DG301ACJ



One SPDT Switch per Package\*

TRUTH TABLE\*\*

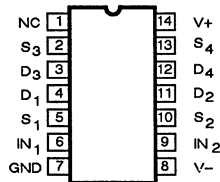
LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF



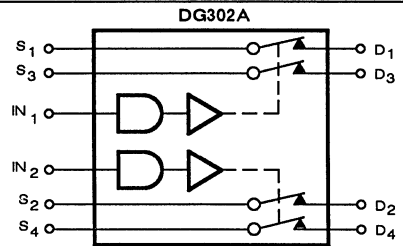
**LCC Package**

Order Number:  
DG301AAZ/883

**Dual-In-Line Package**  
Top View



Order Numbers:  
CerDIP: DG302AAK, DG302AAK/883  
DG302ABK, DG302ACK  
Plastic: DG302ACJ

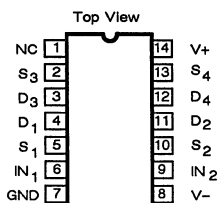


Two DPST Switches per Package\*

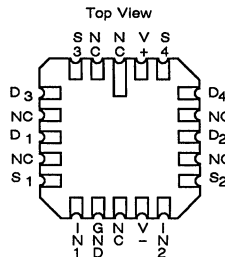
TRUTH TABLE\*\*

LOGIC	SWITCH
0	OFF
1	ON

**Dual-In-Line Package**

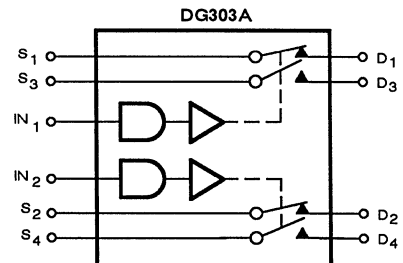


Order Numbers:  
CerDIP: DG303AAK, DG303AAK/883  
DG303ABK, DG303ACK  
Plastic: DG303ACJ



**LCC Package**

Order Number:  
DG303AAZ/883



Two SPDT Switches per Package\*

TRUTH TABLE\*\*

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

\* Switches Shown for Logic "1" Input  
\*\* Logic "0"  $\leq 0.8$  V, Logic "1"  $\geq 4.0$  V

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs, V<sub>S</sub>, V<sub>D</sub><sup>e</sup> ..... (V-) -2 V to (V+) +2V or  
..... 30 mA, whichever occurs first.

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA  
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A & B Suffix) ..... -65 to 150°C  
(C Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
(B Suffix) ..... -25 to 85°C  
(C Suffix) ..... 0 to 70°C

Power Dissipation\*

14-Pin CerDIP (K)\*\* ..... 825 mW

10-Pin Metal Can (A)\*\*\* ..... 450 mW

14-Pin Plastic DIP (J)\*\*\*\* ..... 470 mW

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 11 mW/°C above 75°C.

\*\*\* Derate 6 mW/°C above 75°C.

\*\*\*\* Derate 6.5 mW/°C above 75°C.

## ELECTRICAL CHARACTERISTICS<sup>a</sup>

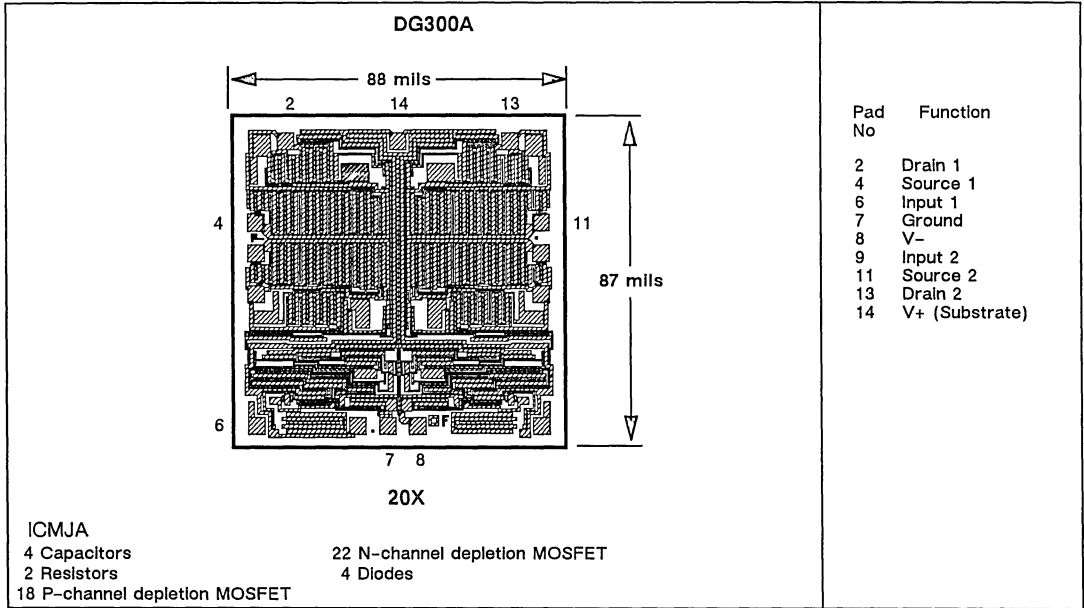
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V V- = -15 V GND = 0 V	LIMITS						UNIT
			1=25°C 2=125,85,70 °C 3=-55,-25,0 °C		A SUFFIX -55 to 125°C		B, C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = 10 V I <sub>S</sub> = -10 mA	1,3 2	30		50 75		50 75	Ω
		V <sub>D</sub> = -10 V I <sub>S</sub> = 10 mA	1,3 2	30		50 75		50 75	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	0.1		1 100		5 100	nA
		V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	-0.1	-1 -100		-5 -100		
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>D</sub> = 14 V V <sub>S</sub> = -14 V	1 2	0.1		1 100		5 100	
		V <sub>D</sub> = -14 V V <sub>S</sub> = 14 V	1 2	-0.1	-1 -100		-5 -100		
Drain ON Leakage Current	I <sub>D(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 14 V	1 2	0.1		1 100		5 100	
		V <sub>D</sub> = V <sub>S</sub> = -14 V	1 2	-0.1	-2 -200		-5 -200		
<b>INPUT</b>									
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	1 2,3	-0.001	-1 -1		-1		μA
		V <sub>IN</sub> = 15 V	1 2,3	0.001		1 1		1	
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1 2,3	-0.001	-1 -1		-1		

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT
			1=25°C 2=125,85,70 °C 3=-55,-25,0 °C		A SUFFIX -55 to 125°C		B, C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1	150		300			ns
Turn-OFF Time	t <sub>OFF</sub>		1	130		250			
Break-Before-Make Interval	t <sub>ON</sub> - t <sub>OFF</sub>	See Break-Before-Make Test Time Circuit DG301A/303A ONLY	1	50					
Charge Injection	Q	C <sub>L</sub> = 1 nF, R <sub>gen</sub> = 0Ω V <sub>gen</sub> = 0 V	1	3					pC
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>IN</sub> = 0.8 V or V <sub>IN</sub> = 4.0 V f = 1 MHz	V <sub>S</sub> = 0 V	1	14				pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		V <sub>D</sub> = 0 V	1	14				
Channel-ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>S</sub> = V <sub>D</sub> = 0 V	1	40				
Input Capacitance	C <sub>in</sub>		f = 1 MHz	V <sub>IN</sub> = 0 V	1	6			
			V <sub>IN</sub> = 15 V	1	7				
OFF Isolation		V <sub>IN</sub> = 0 V R <sub>L</sub> = 1 kΩ V <sub>S</sub> = 1 V <sub>rms</sub> f = 500 kHz	1	62					dB
Crosstalk (Channel-to-Channel)			1	74					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 4.0 V (One Input) (All Others = 0 V)	1,2 3	0.23		0.5 1		1.0	mA
Negative Supply Current	I <sub>-</sub>		1,3 2	-0.001	-10 -100		-100		
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0.8 V (All Inputs)	1,3 2	0.001		10 100		100	μA
Negative Supply Current	I <sub>-</sub>		1,3 2	-0.001	-10 -100		-100		

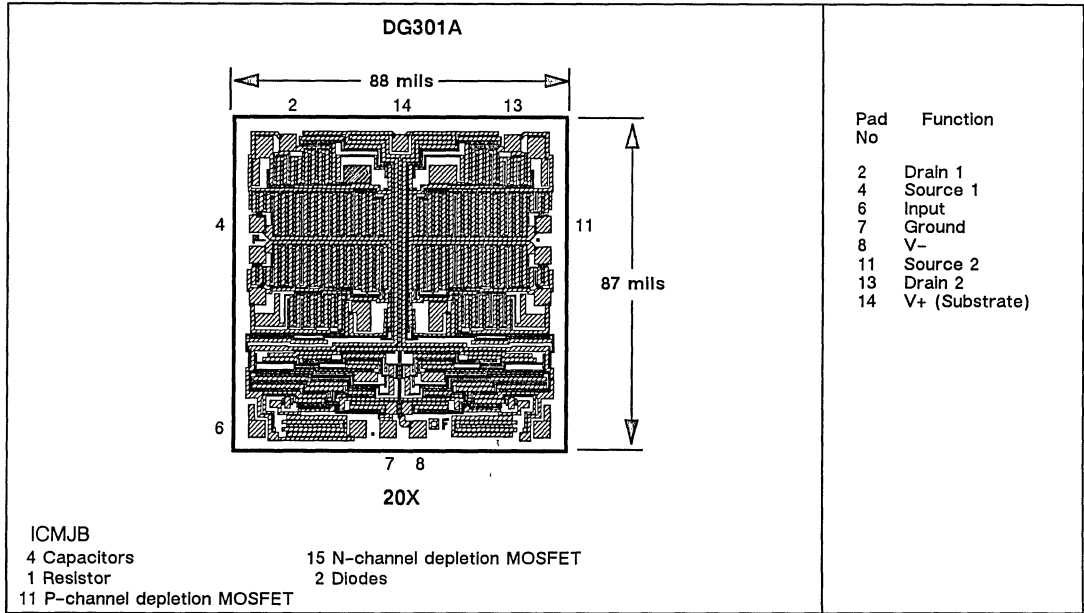
**NOTES:**

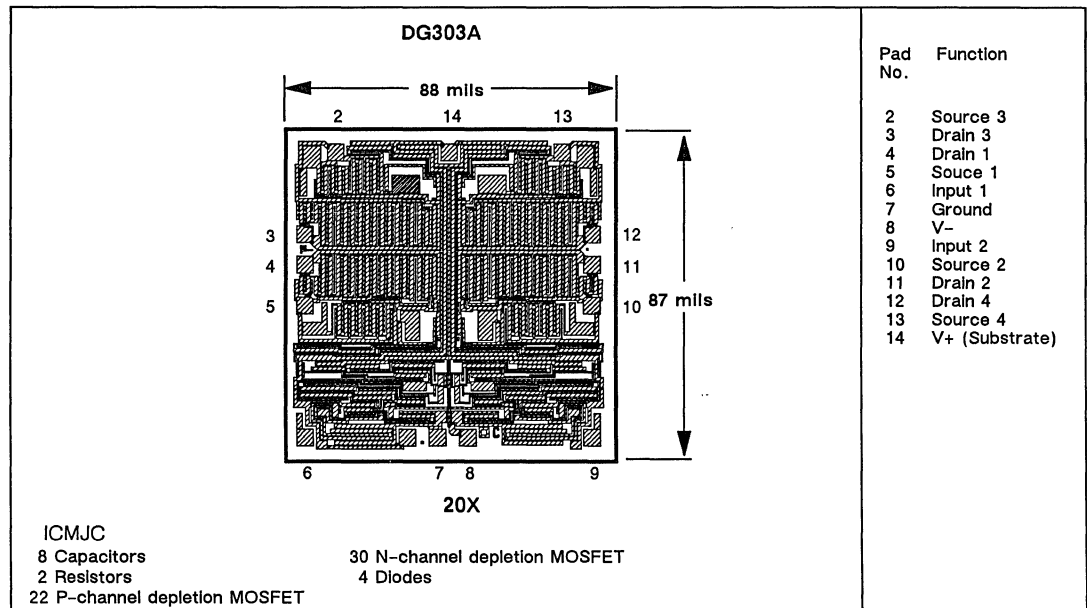
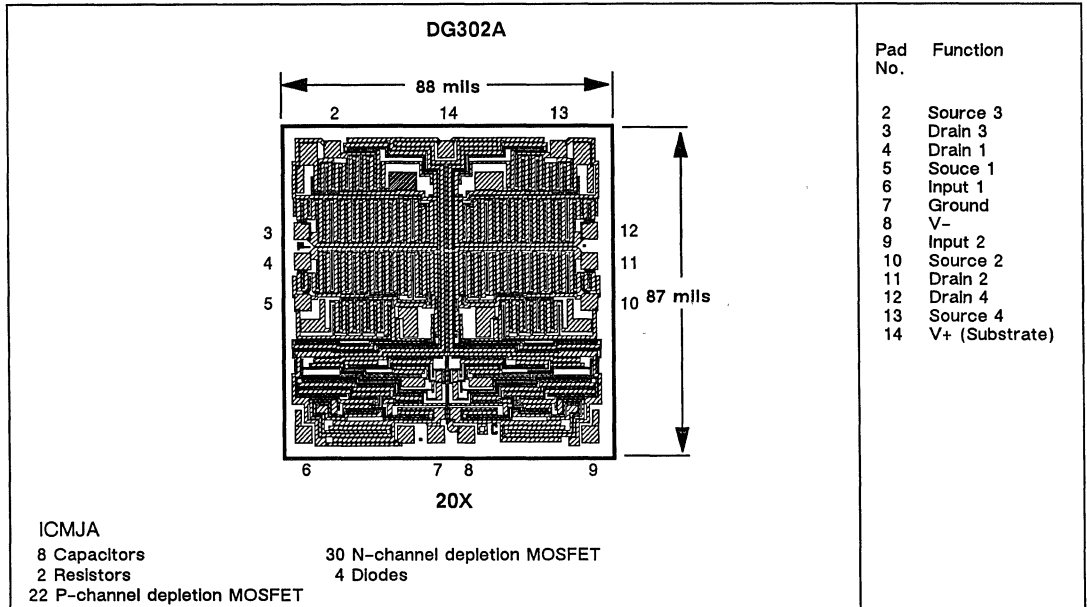
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Signals on S<sub>x</sub>, D<sub>x</sub>, or IN<sub>x</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
- OFF Isolation :  $20 \log \frac{V_S}{V_D}$ . V<sub>S</sub> = input to OFF switch, V<sub>D</sub> = Output.

**DIE TOPOGRAPHY**

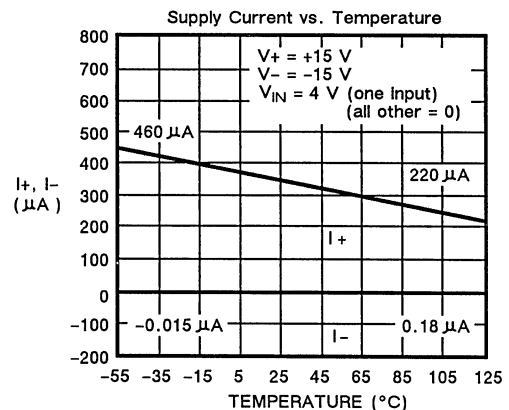
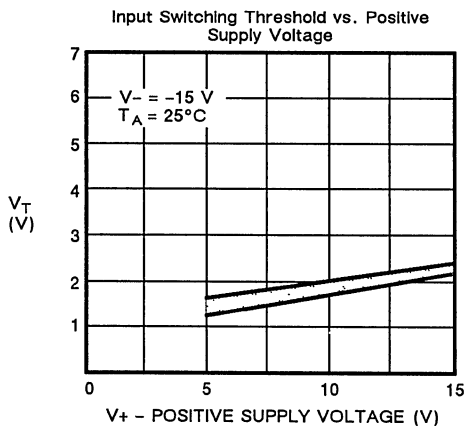
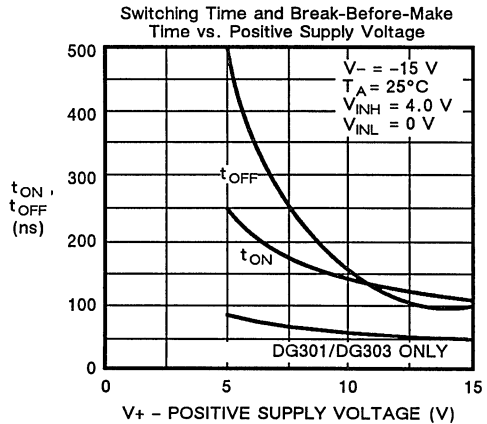
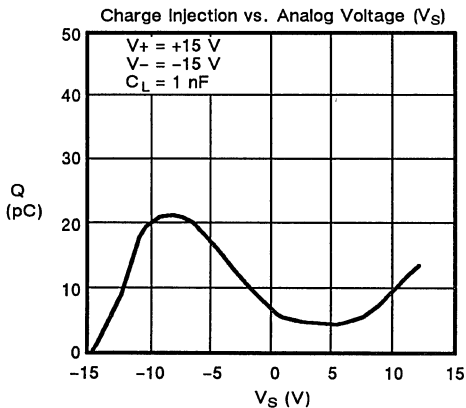
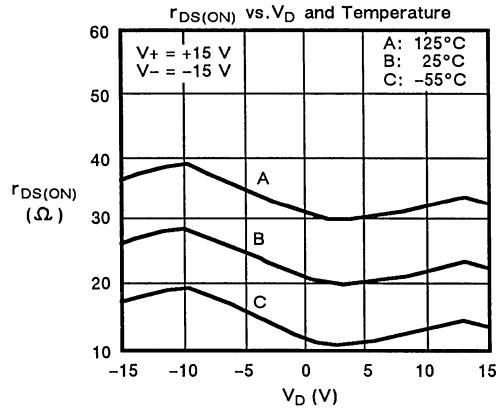
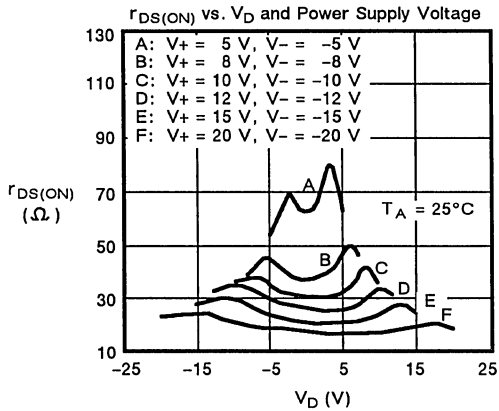


**5**

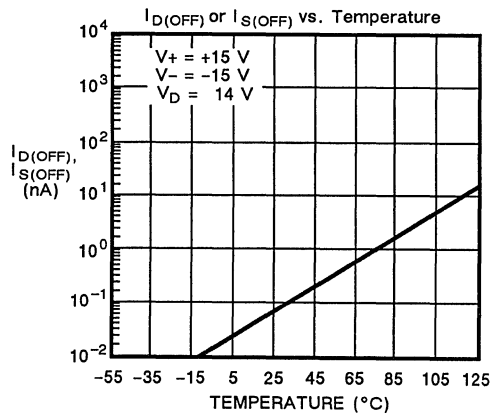
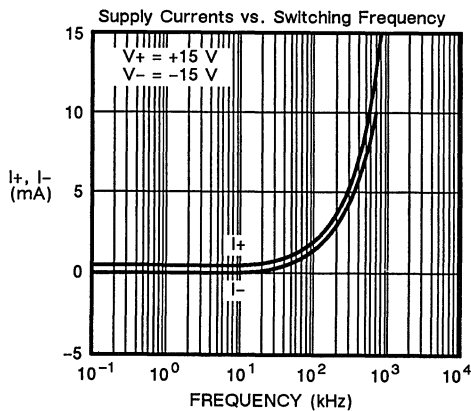
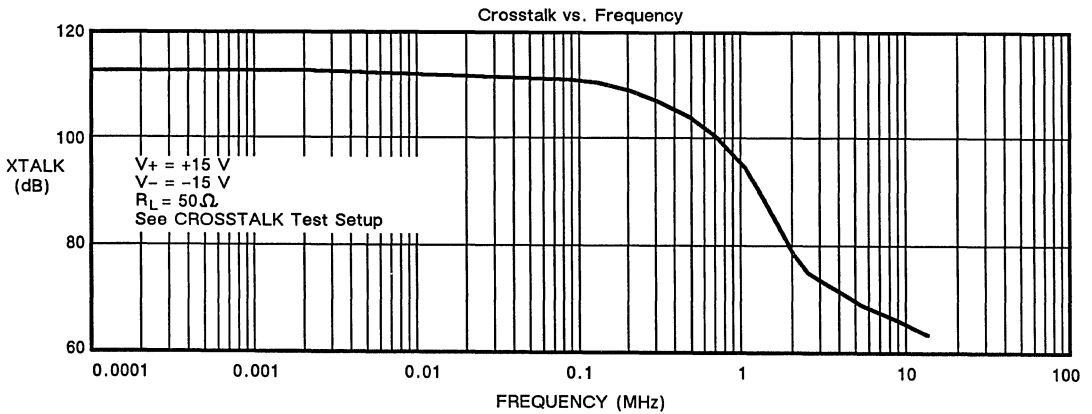
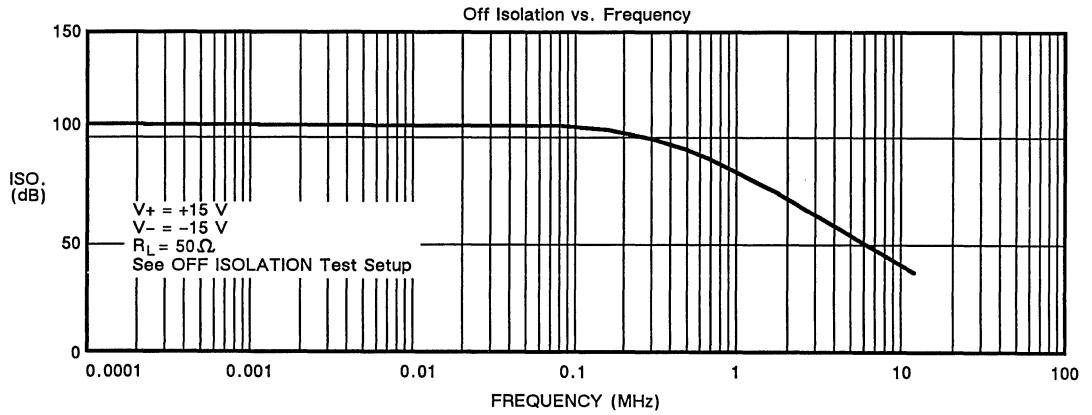




## TYPICAL CHARACTERISTICS

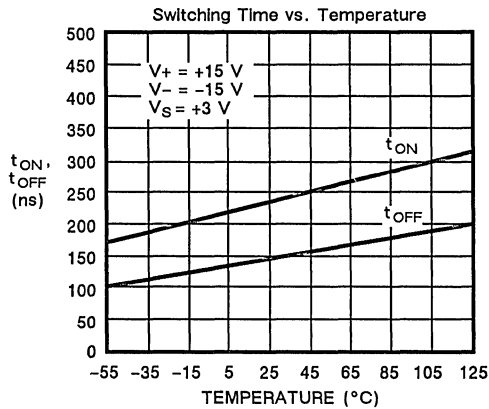
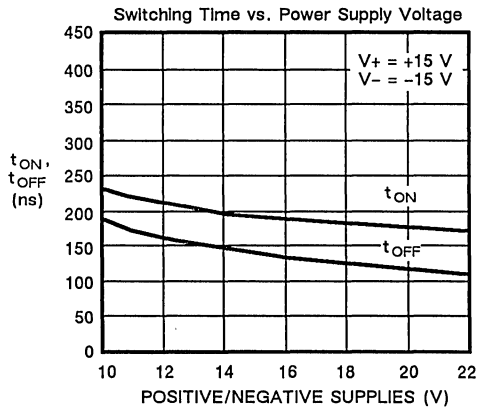
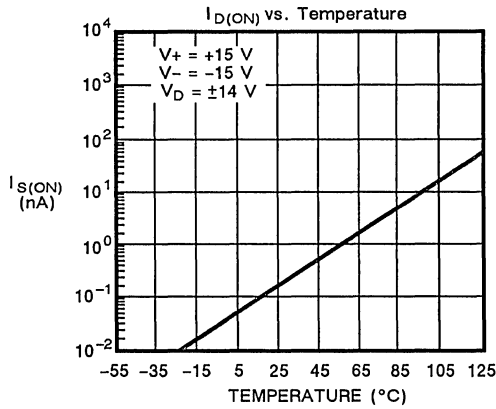


## TYPICAL CHARACTERISTICS (Cont'd)



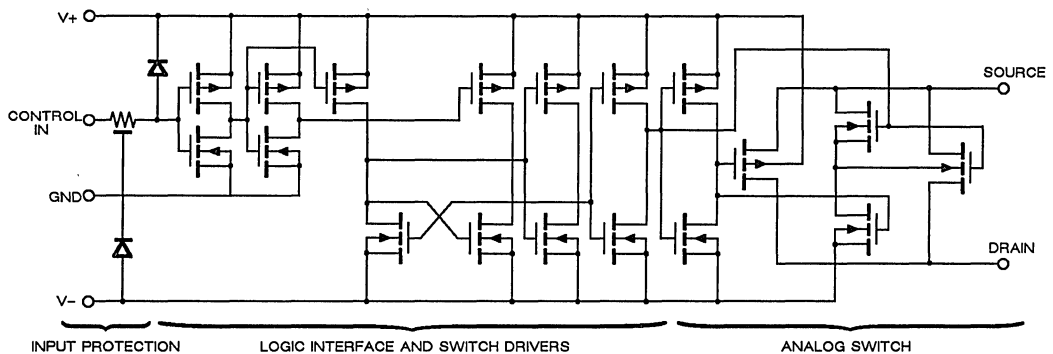


## TYPICAL CHARACTERISTICS (Cont'd)

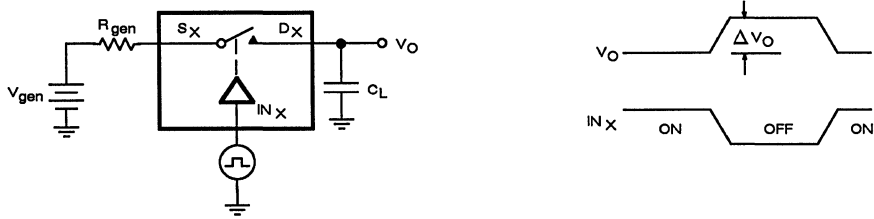


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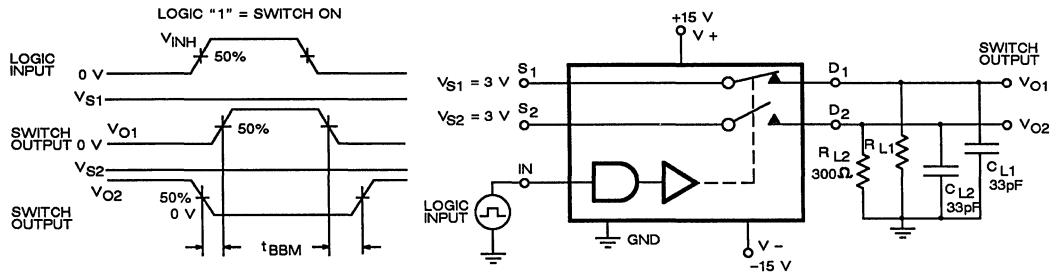
## SCHEMATIC DIAGRAM (Typical Channel)



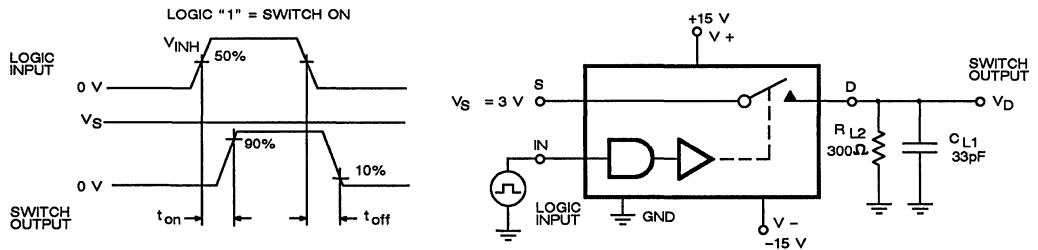
## CHARGE INJECTION TEST CIRCUIT



## BREAK-BEFORE-MAKE TIME TEST CIRCUIT SPDT (DG301A, DG303A)



## SWITCHING TIME TEST CIRCUIT

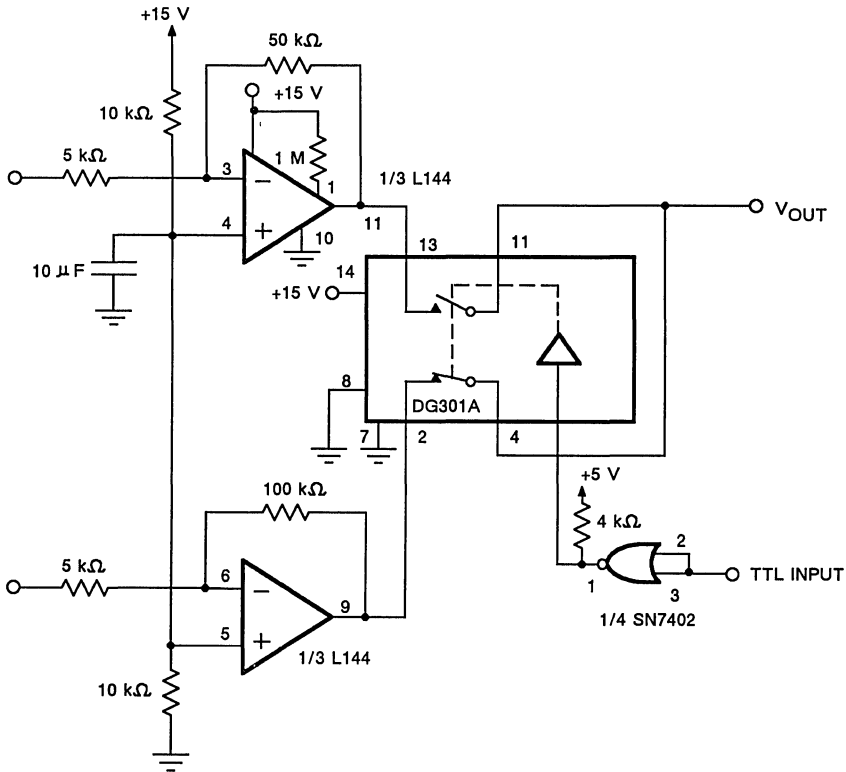
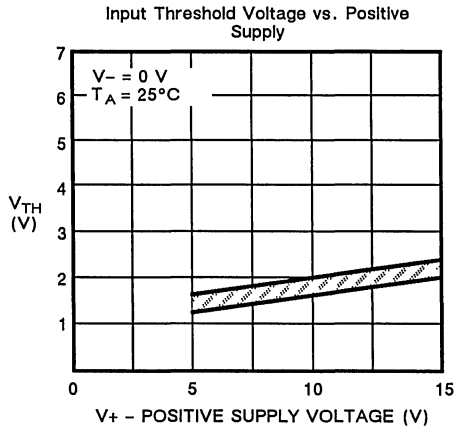


## APPLICATION HINTS

V <sub>+</sub> Positive Supply Voltage (V)	V <sub>-</sub> Negative Supply Voltage (V)	GND Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> Analog Voltage Range (V)
15	-15	0	4/0.8	-15 to 15
20	-20	0	4/0.8	-20 to 20
15	0	0	4/0.8	0 to 15

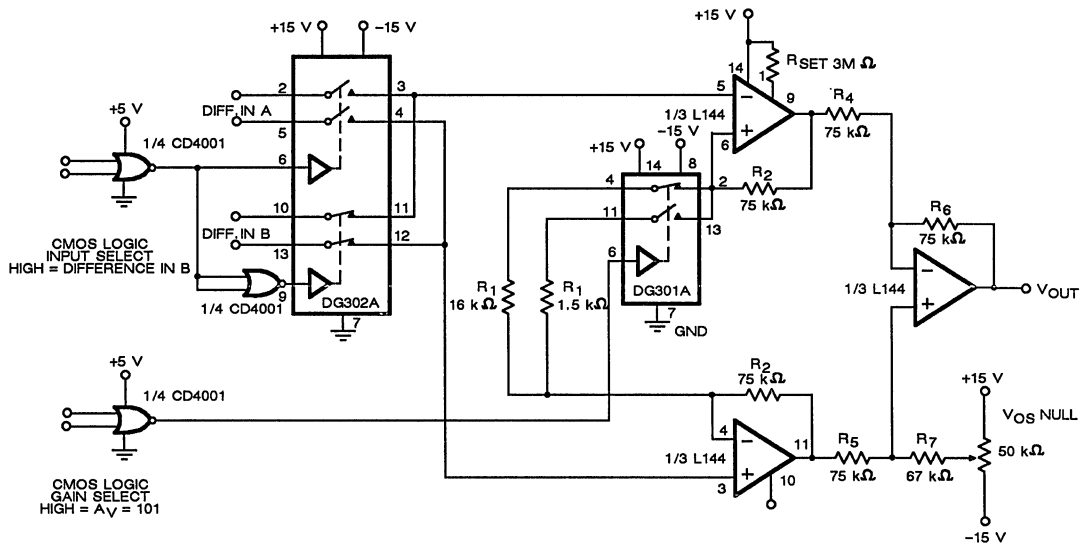
## APPLICATIONS

The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are: 1) Increased  $r_{DS(ON)}$ ; 2) slower switching speed. Typical curves for design aid are given in the figures below. The analog voltage should not go above or below the supply voltages which in single operation are  $V_+$  and 0 V.



Single Supply Op Amp Switching

## APPLICATIONS (Cont'd)



$R_{SET}$  programs L144 power dissipation, gain-bandwidth product. Refer to AN73-6 and the L144 data sheet.

Voltage gain of the Instrumentation amplifier is :

$$A_V = 1 + \frac{2R_2}{R_1} \quad (\text{In the circuit shown, } A_{V1} = 10.4, A_{V2} = 101)$$

### Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain

# DGP303A

## Precision Dual SPDT CMOS Analog Switch

### FEATURES

- $\pm 22$  Volt Input Range
- $10 \Omega$  Max  $\Delta r_{DS(ON)}$  Any Combination Of Switches
- 0.5 nA Max At 25°C,  $\pm 15$  V
- Tested  $\Delta t_{ON}$  and  $\Delta t_{OFF} < 50$  ns
- Pin Compatible with DG303A

### BENEFITS

- Fully Tested Around  $\pm 10.8, \pm 16.5$  And  $\pm 22$  V Supplies
- Increased Signal Range
- Reduced Switching Errors
- Better Channel-to-Channel Matching
- Simplifies Worst Case Analysis
- Simplifies Upgrades

### APPLICATIONS

- Precision Data Acquisition
- Automatic Test Equipment
- Precision Instrumentation
- Radar Systems

### DESCRIPTION

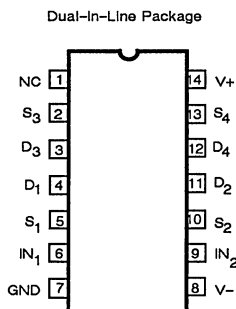
The DGP303A is a precision dual single-pole double-throw analog switch designed for critical applications requiring improved performance over that obtainable with the popular DG303A. Produced on an enhanced proprietary high voltage process, the DGP303A has been fully specified with input analog signals to  $\pm 22$  V, making it an ideal choice for high voltage applications or where the added margin of safety over traditional switches is of importance.

$r_{DS(ON)}$ ,  $t_{ON}$  and  $t_{OFF}$  have been tested and guaranteed at various input voltages to assure worst-case error analysis. An epitaxial layer prevents latchup.

Packaging for this device includes the 14-pin CerDIP and plastic DIP options. Performance grades include military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ) temperature ranges. Customers interested in SO packaging should design-in the DG403DY.

In addition to the low current leakage specifications,

### PIN CONFIGURATION



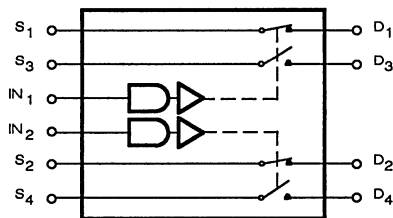
Top View

Order Numbers:

CerDIP: DGP303AAK  
DGP303AAK883

Plastic: DGP303ADJ

### FUNCTION BLOCK DIAGRAM



Two SPDT Switches per Package

Truth Table

LOGIC	SWITCH 1,2	SWITCH 3,4
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq 0.8$  V

Logic "1"  $\geq 4.0$  V

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-	Operating Temperature (A Suffix) . . . . .	-55 to 125°C
V+ . . . . .	(D Suffix) . . . . .	-40 to 85°C
GND . . . . .	Power Dissipation (Package)*	
Digital Inputs $V_S, V_D^1$ . . . . .	14-Pin Plastic DIP** . . . . .	450 mW
(V-) -2V to (V+) +2V . . . . .	14-Pin CerDIP*** . . . . .	900 mW
or 30 mA, whichever occurs first		
Continuous Current (Any Terminal) . . . . .	* All leads welded or soldered to PC board.	
30 mA	** Derate 6 mW /°C above 75°C.	
Current, S or D (Pulsed 1 ms 10% duty) . . . . .	*** Derate 12 mW /°C above 75°C.	
100 mA		
Storage Temperature (A Suffix) . . . . .	1 Signals on Sx, Dx, or INx exceeding V+ or V- will be	
-65 to 150°C	clamped by internal diodes. Limit forward diode	
(D Suffix) . . . . .	current to maximum current ratings.	
-65 to 125°C		

## THE DGP FAMILY OF ANALOG SWITCHES AND MULTIPLEXERS

Siliconix has improved its high-voltage metal-gate CMOS process to allow for lower leakage, higher voltage and lower variation performance. Additionally, through dramatic improvements in automated testing technology, specifications and limits that were previously untestable are now 100% tested and specified on the DGP303A data sheet.

The data sheet specification tables are in a new format as well. The format is that of a military drawing, where all specifications are 100% tested, eliminating any uncertainty about what is actually tested. Many parameters that were previously listed as "typical" or "guaranteed by design" are now 100% tested with minimum and maximum values, so that a worst case design can be realized.

The DGP303A also specified certain parameters that have never been seen on a DG303A standard product data sheet in min/max or typical form. An important example of this is the variation of the switching time over all channels, which is specified with a maximum of 50 ns. The variation of "ON" resistance is similarly specified and 100% tested to be less than 10  $\Omega$  over six different drain voltage and source current conditions, over all four channels tested, resulting in 24 different readings.

This specification is necessary for determining the worst-case distortion and signal level variation due to differences in channel resistance and "ON" resistance modulation effects. Also note that  $r_{DS(ON)}$  is measured at the lower extreme of the voltage operating level, (e.g.  $\pm 13.5$  V instead of  $\pm 15$  V) where  $r_{DS(ON)}$  is highest.

Leakage currents are specified and tested to new lower limits at both room temperature and over the full temperature range. For example, the industrial range devices' leakages have been reduced from 100 nA (over temp) on the DG303A to 5 nA (over temp) on the DGP version. Additionally, the leakages are specified at the extremes of the operating ranges (e.g.  $\pm 16.5$  V instead of  $\pm 15$  V), where the leakages tend to be the highest. This is essential for designs where worst-case leakage must be well known, such as precision instruments and sample-and-hold amplifiers.

The operating range of the DGP303A, up to  $\pm 22$  V and down to  $\pm 10.8$  V. This allows the switches to have guaranteed performance limits with power supplies as low as  $\pm 12$  V ( $\pm 10\%$ ),  $\pm 15$  V ( $\pm 10\%$ ), and up to  $\pm 20$  V ( $\pm 10\%$ ).

**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT	
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>+</sub> = 13.5 V, V <sub>-</sub> = -13.5 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±10.0 V	1,3 2	30		50 75		50 75	Ω	
		V <sub>+</sub> = 10.8 V, V <sub>-</sub> = 10.8 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±7.5 V V <sub>IN</sub> = 0.4 V	1,3 2	40		75 100		75 100		
		V <sub>+</sub> = 22 V, V <sub>-</sub> = -22 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±15 V	1,3 2	25		40 60		40 60		
Delta Drain-Source ON Resistance	Δ r <sub>DS(ON)</sub>	V <sub>D</sub> = +5, 0, -5 V, I <sub>S</sub> = ±1 mA V <sub>IN</sub> = 0.8 V Worst Combination	1,3 2	3		10 15		10 15		
Channel ON Leakage Current	I <sub>D(ON)</sub> <sup>+</sup> I <sub>S(ON)</sub>	V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>S</sub> = V <sub>D</sub> = 15.5 V	1 2	0.1	-0.5 -60	0.5 60	-0.5 -6	0.5 6	nA
			V <sub>S</sub> = V <sub>D</sub> = -15.5 V	1 2	0.1	-0.5 -60	0.5 60	-0.5 -6	0.5 6	
		V <sub>+</sub> = 22 V V <sub>-</sub> = -22 V	V <sub>D</sub> = V <sub>S</sub> = 21 V	1 2	0.4	-2 -200	2 200	-2 -20	2 20	
			V <sub>D</sub> = V <sub>S</sub> = -21 V	1 2	0.4	-2 -200	2 200	-2 -20	2 20	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>+</sub> = 13.5 V V <sub>-</sub> = -13.5 V	V <sub>D</sub> = -12.5 V V <sub>S</sub> = +12.5 V	1 2	0.1	-0.5 -50	0.5 50	-0.5 -5	0.5 5	nA
			V <sub>D</sub> = +12.5 V V <sub>S</sub> = -12.5 V	1 2	-0.1	-0.5 -50	0.5 50	-0.5 -5	0.5 5	
		V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>D</sub> = -15.5 V V <sub>S</sub> = +15.5 V	1 2	0.15	-0.5 -50	0.5 50	-0.5 -5	0.5 5	
			V <sub>D</sub> = +15.5 V V <sub>S</sub> = -15.5 V	1 2	-0.15	-0.5 -50	0.5 50	-0.5 -5	0.5 5	
		V <sub>+</sub> = 22 V V <sub>-</sub> = -22 V	V <sub>D</sub> = -21 V V <sub>S</sub> = +21 V	1 2	0.2	-2 -100	2 100	-2 -2	2 2	
			V <sub>D</sub> = +21 V V <sub>S</sub> = -21 V	1 2	-0.2	-2 -100	2 100	-2 -10	2 10	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>+</sub> = 13.5 V V <sub>-</sub> = -13.5 V	V <sub>D</sub> = -12.5 V V <sub>S</sub> = +12.5 V	1 2	0.1	-0.5 -50	0.5 50	-0.5 -5	0.5 5	nA
			V <sub>D</sub> = +12.5 V V <sub>S</sub> = -12.5 V	1 2	-0.1	-0.5 -50	0.5 50	-0.5 -5	0.5 5	
		V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>D</sub> = -15.5 V V <sub>S</sub> = +15.5 V	1 2	0.15	-0.5 -50	0.5 50	-0.5 -5	0.5 5	
			V <sub>D</sub> = +15.5 V V <sub>S</sub> = -15.5 V	1 2	-0.15	-0.5 -50	0.5 50	-0.5 -5	0.5 5	

**5**

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>		LIMITS						UNIT
				1=25°C		A SUFFIX		D SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH (Cont'd)</b>										
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>+</sub> = 22 V V <sub>-</sub> = -22 V	V <sub>D</sub> = -21 V	1	0.2	-2	2	-2	2	nA
			V <sub>S</sub> = +21 V	2		-100	100	-10	10	
			V <sub>D</sub> = +21 V	1	-0.2	-2	2	-2	2	
			V <sub>S</sub> = -21 V	2		-100	100	-10	10	
<b>INPUT</b>										
Input current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>+</sub> = 22 V, V <sub>-</sub> = -22 V V <sub>IN</sub> under test = 5 V	1	0.005	-0.5	0.5	-0.5	0.5	μA	
			2		-5	5	-5	5		
Input current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>+</sub> = 22 V, V <sub>-</sub> = -22 V V <sub>IN</sub> under test = 0 V	1	0.005	-0.5	0.5	-0.5	0.5		
			2		-5	5	-5	5		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuits	1,3	150		300		300	ns	
Turn-OFF Time	t <sub>OFF</sub>		2			400		400		
Delta t <sub>ON</sub>	Δ t <sub>ON</sub>		1,3	30		50		50		
Delta t <sub>OFF</sub>	Δ t <sub>OFF</sub>		2			100		100		
Charge Injection	Q	R <sub>gen</sub> = 0Ω C <sub>L</sub> = 10 nF	V <sub>gen</sub> = 0 V	1	35				pC	
			V <sub>gen</sub> = ± 10 V	1	45					
Source OFF Capacitance <sup>d</sup>	C <sub>S(OFF)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	1	14					pF	
Drain OFF Capacitance <sup>d</sup>	C <sub>D(OFF)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	1	14					pF	
Channel ON Capacitance <sup>d</sup>	C <sub>D + S(ON)</sub>		1	40						
Crosstalk (Channel-to-Channel)		R <sub>L</sub> = 75Ω    C <sub>L</sub> = 5 pF f = 1 MHz	1	64					dB	
OFF Isolation		R <sub>L</sub> = 75Ω    C <sub>L</sub> = 5 pF f = 1 MHz	1	56						

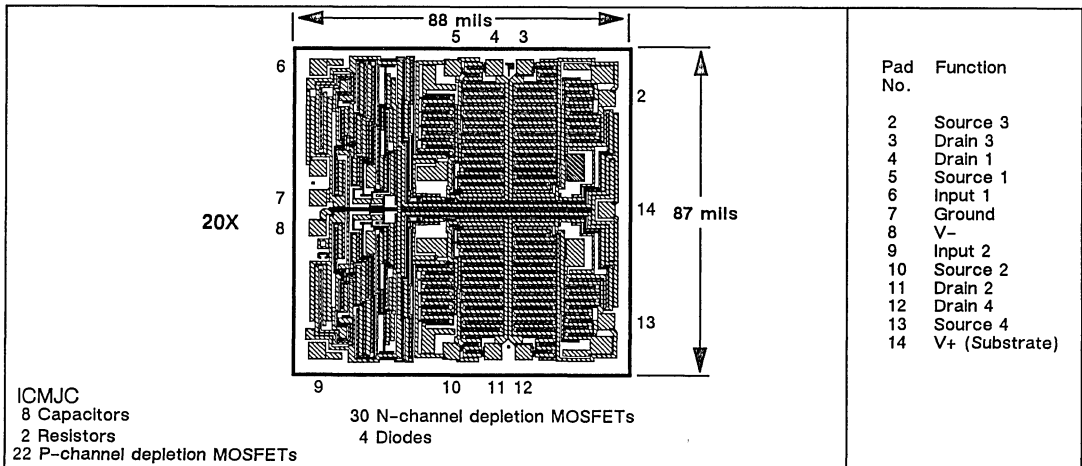


ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT	
			1=25°C		A SUFFIX		D SUFFIX			
			2=125,85°C		-55 to 125°C		-40 to 85°C			
		3=-55,-40°C		MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
		TEMP	TYP <sup>d</sup>							
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> (One Input) = 4V All Others = 0 V V <sub>±</sub> = ±16.5 V	1	0.45		0.6		0.6	mA	
		V <sub>IN</sub> = 0.8 V, All Inputs V <sub>±</sub> = ±16.5 V	1	0.001		10		10		
Negative Supply Current	I <sub>-</sub>	V <sub>IN</sub> (One Input) = 4 V All Others = 0 V V <sub>±</sub> = ±16.5 V	1	-0.001	-10		-10		μA	
		V <sub>IN</sub> = 0.8 V, All Inputs V <sub>±</sub> = ±16.5 V	1	-0.001	-10		-10			
			2		-100		-100			

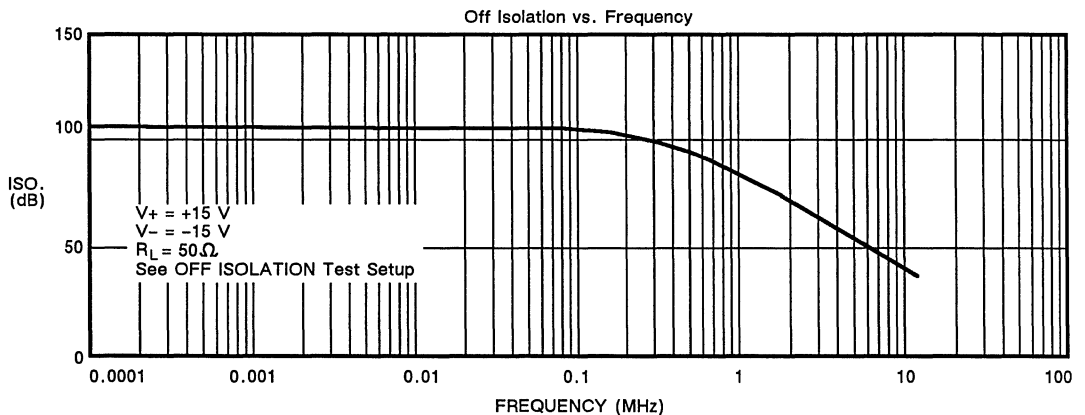
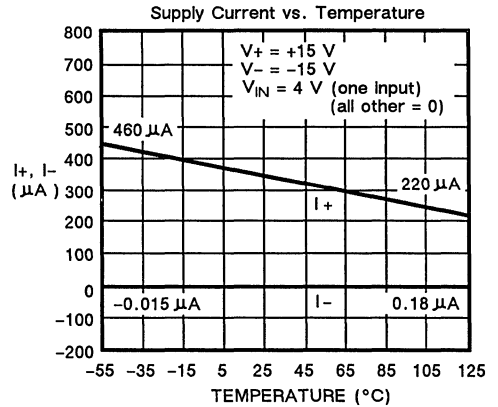
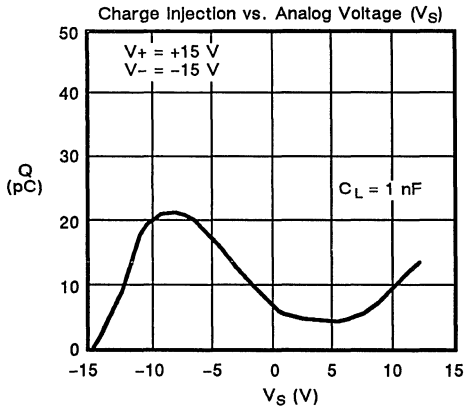
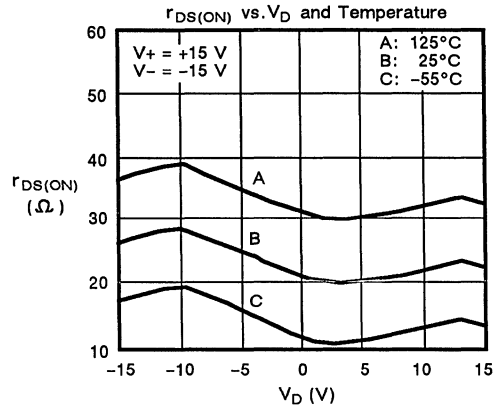
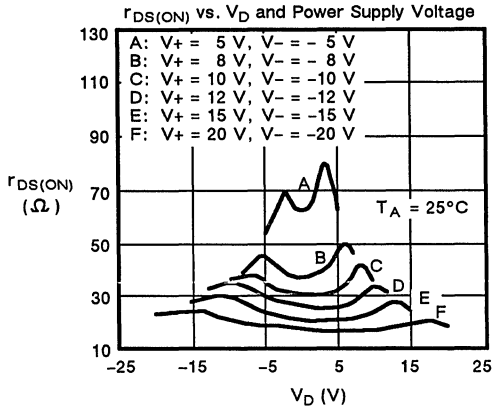
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = input voltage to perform proper function.

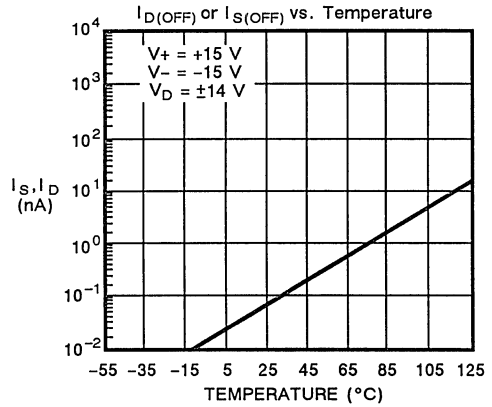
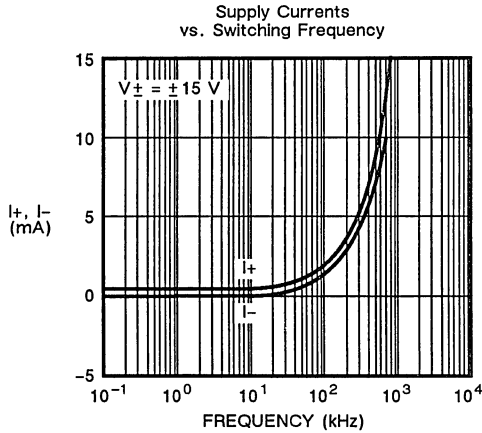
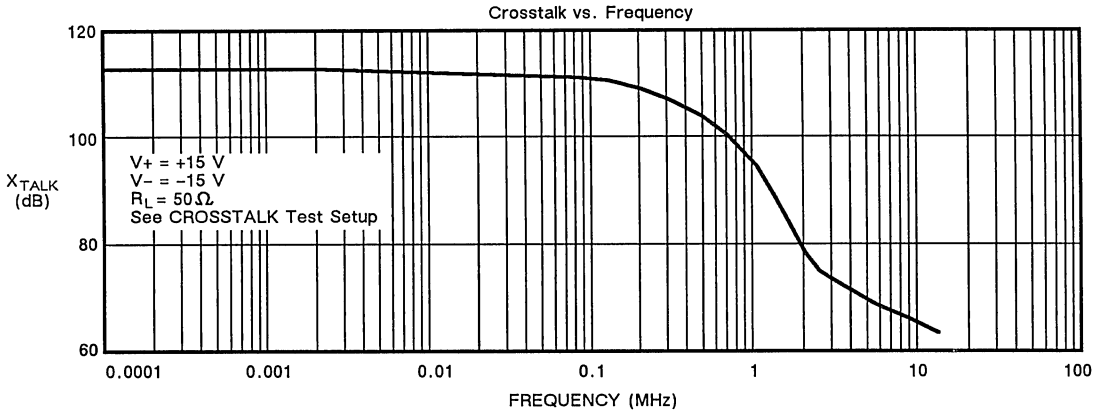
**DIE TOPOGRAPHY**



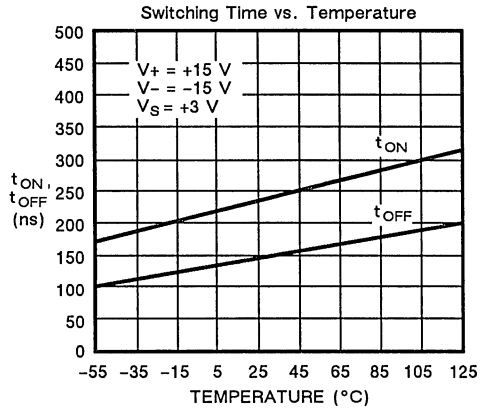
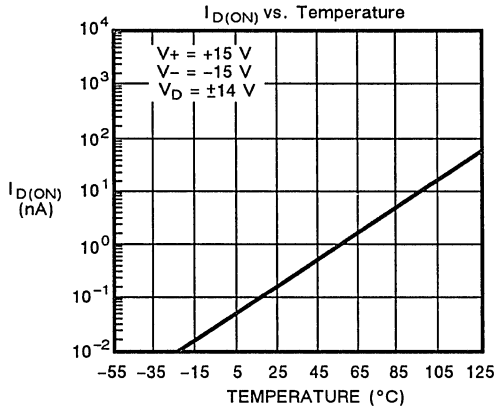
## TYPICAL CHARACTERISTICS



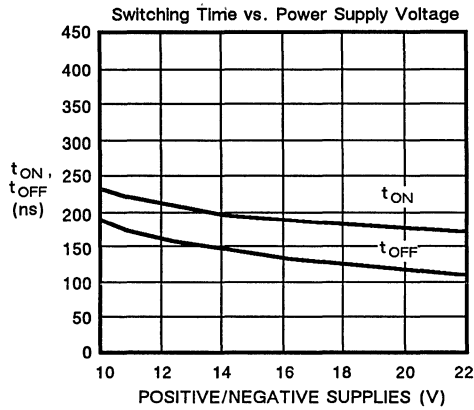
**TYPICAL CHARACTERISTICS**



**5**

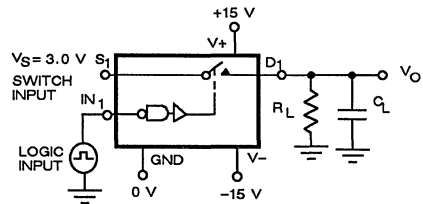
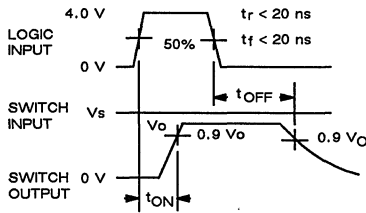


## TYPICAL CHARACTERISTICS



## SWITCHING TIME TEST CIRCUITS

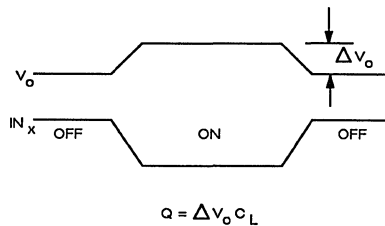
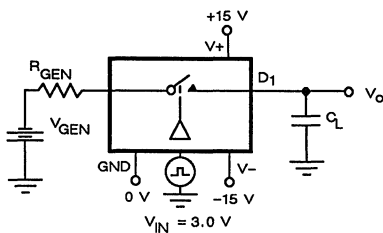
$V_o$  is the steady state output with the switch ON. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



For load conditions, See Electrical Characteristics  $C_L$  (includes fixture and stray capacitance)

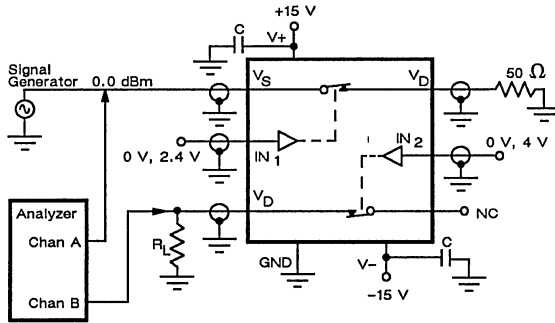
$$V_o = V_s \frac{R_L}{R_L + R_{DS(ON)}}$$

## CHARGE INJECTION TEST CIRCUIT



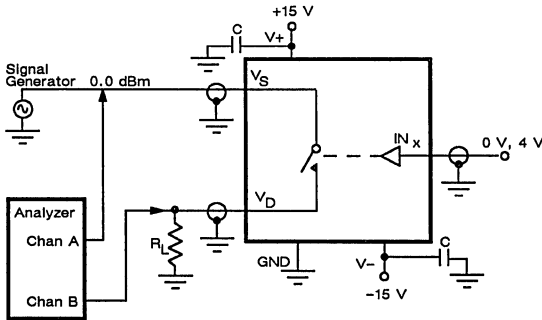
$$Q = \Delta V_o C_L$$

**CROSSTALK TEST CIRCUIT**



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

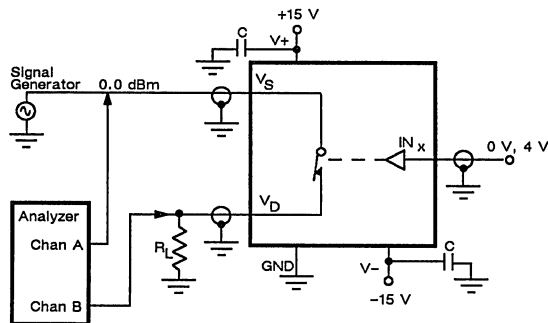
**OFF ISOLATION TEST CIRCUIT**



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

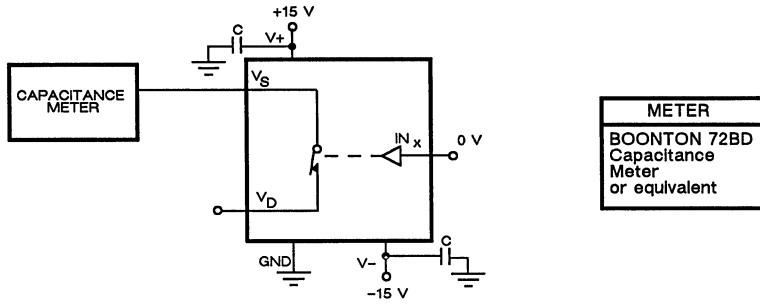
**5**

**INSERTION LOSS TEST CIRCUIT**

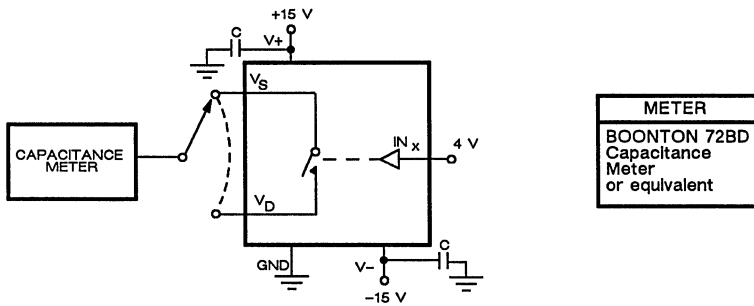


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

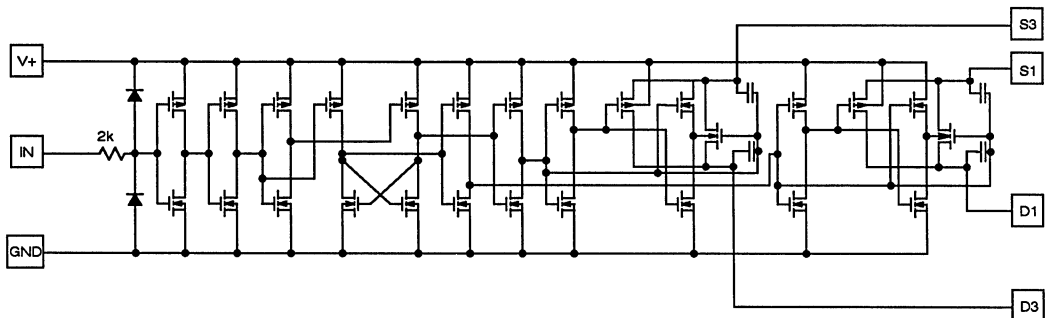
## SOURCE/DRAIN ON CAPACITANCE



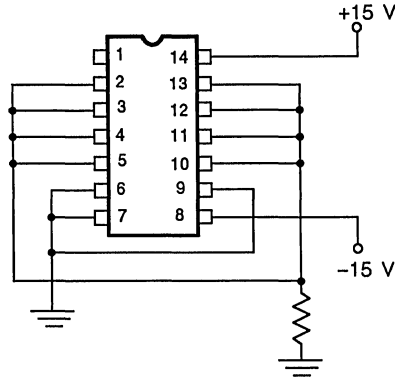
## SOURCE/DRAIN OFF CAPACITANCE



## SCHEMATIC DIAGRAM (Typical Channel)



## BURN-IN CIRCUIT



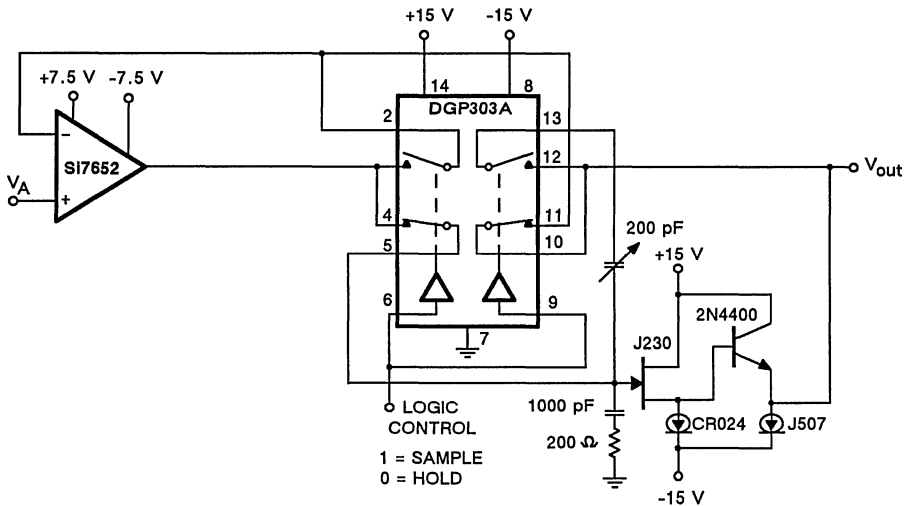
Note: All Resistors are 10 k $\Omega$  unless otherwise specified

## APPLICATION HINTS

The figure below shows a precision sample-and-hold amplifier using the DGP303A. The errors contributed by the analog switch are mostly attributed to charge injection and leakage. Charge

injection causes a dc offset to appear on the holding capacitor.

The low leakage of the DGP303A reduces the droop rate of the sample and hold.



Precision Sample & Hold

# DG304A/305A/306A/307A

## CMOS Analog Switches

### FEATURES

- $\pm 15$  V Input Range
- Fast Switching (< 250 ns)
- Low  $r_{DS(ON)}$  (< 50  $\Omega$ )
- Single Supply Operation
- CMOS Logic Levels

### BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Low Power Dissipation

### APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable Battery Operation

### DESCRIPTION

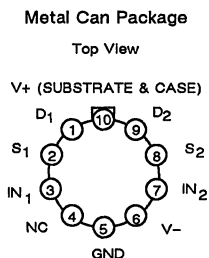
The DG304A through DG307A series of monolithic CMOS switches were designed for applications in communications, instrumentation and process control. This series is well suited for applications requiring fast switching and nearly flat ON resistance over the entire analog range.

Designed on Siliconix PLUS-40 CMOS process to achieve low power consumption (a few milliwatts) and excellent ON/OFF switch performance, making these ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation (for positive switch voltages) is afforded by connecting the V- rail to 0 V.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. These switches are CMOS input compatible.

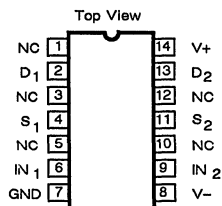
There are four devices in this series, which are differentiated by the type of switch action. Packaging for this series include the 14-pin CerDIP and plastic options. The 10-pin metal can option is also available for the DG304A/DG305A. Performance grades include the military, A suffix (-55 to 125°C), commercial, C suffix (0 to 70°C), and industrial, B suffix (-25 to 85°C) temperature ranges. Additionally, the DG307A is available in the LCC package.

### PIN CONFIGURATION



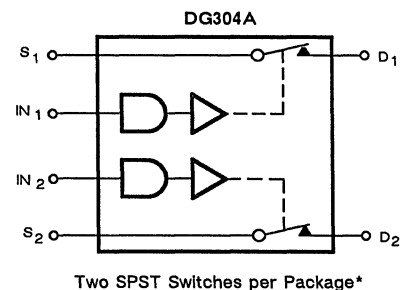
Order Numbers:  
DG304AAA, DG304AAA/883  
DG304ABA, DG304ACA

### Dual-In-Line Package



Order Numbers:  
CerDIP: DG304AAK, DG304AAK/883  
DG304ABK, DG304ACK  
Plastic: DG304ACJ

### FUNCTIONAL BLOCK DIAGRAM



LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq 3.5$  V  
Logic "1"  $\geq 11$  V

\* Switches Shown for Logic "1" Input

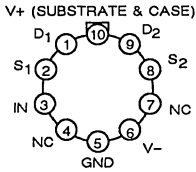


**PIN CONFIGURATION (Cont'd)**

**FUNCTIONAL BLOCK DIAGRAM (Cont'd)**

**Metal Can Package**

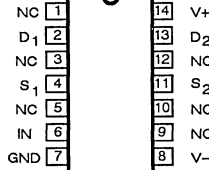
Top View



Order Numbers:  
DG305AAA, DG305AAA/883  
DG305ABA, DG305ACA

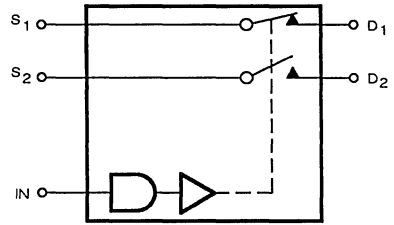
**Dual-In-Line Package**

Top View



Order Numbers:  
CerDIP: DG305AAK, DG305AAK/883  
DG305ABK, DG305ACK  
Plastic: DG305ACJ

**DG305A**



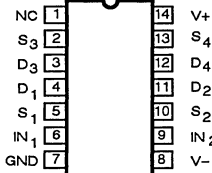
One SPDT Switch per Package\*

TRUTH TABLE\*\*

LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

**Dual-In-Line Package**

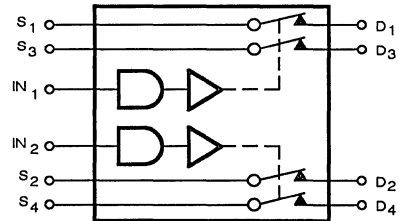
Top View



Order Numbers:

CerDIP: DG306AAK, DG306AAK/883  
DG306ABK, DG306ACK  
Plastic: DG306ACJ

**DG306A**



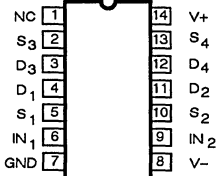
Two DPST Switches per Package\*

TRUTH TABLE\*\*

LOGIC	SWITCH
0	OFF
1	ON

**Dual-In-Line Package**

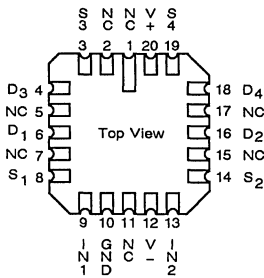
Top View



Order Numbers:

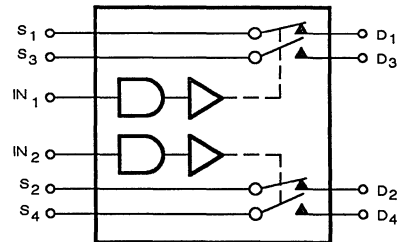
CerDIP: DG307AAK, DG307AAK/883  
DG307ABK, DG307ACK  
Plastic: DG307ACJ

**LCC Package**



Order Number:  
DG307AAZ/883

**DG307A**



Two SPDT Switches per Package\*

TRUTH TABLE\*\*

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

\* Switches Shown for Logic "1" Input  
\*\* Logic "0" ≤ 3.5 V, Logic "1" ≥ 4.0 V

## ABSOLUTE MAXIMUM RATINGS

V+ to V-	44 V
GND to V-	25 V
Digital Inputs, V <sub>S</sub> , V <sub>D</sub> <sup>g</sup>	(V-) -2 V to (V+) +2V or 30 mA, whichever occurs first.
Current, Any Terminal Except S or D	30 mA
Continuous Current, S or D	30 mA
(Pulsed at 1 ms, 10% duty cycle max)	100 mA
Storage Temperature (A & B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C

Power Dissipation*	
14-Pin CerDIP (K)**	825 mW
14-Pin Plastic DIP (J)***	470 mW
10-Pin Metal Can (A)****	450 mW
20-Pin LCC (Z)*****	750 mW

- \* Device mounted with all leads soldered or welded to PC board.
- \*\* Derate 11 mW/°C above 75°C.
- \*\*\* Derate 6.5 mW/°C above 25°C.
- \*\*\*\* Derate 6 mW/°C above 75°C.
- \*\*\*\*\* Derate 10 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: V+ = 15 V V- = -15 V GND = 0 V	LIMITS						UNIT		
			1=25°C 2=125,85,70°C 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B, C SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>	I <sub>S</sub> = 10 mA V <sub>IN</sub> = 3.5 or 11 V <sup>f</sup>	1,2,3		-15	15	-15	15	V		
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = 10 V I <sub>S</sub> = -10 mA	1,3 2	30		50 75		50 75	Ω		
		V <sub>D</sub> = -10 V I <sub>S</sub> = 10 mA	1,3 2	30		50 75		50 75			
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 3.5 V or V <sub>IN</sub> = 11 V <sup>f</sup>	V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	0.1		1 100		5 100	nA	
			V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	-0.1	-1 -100		-5 -100			
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	0.1		1 100		5 100		
			V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	-0.1	-1 -100		-5 -100			
Drain ON Leakage Current	I <sub>D(ON)</sub>		V <sub>D</sub> = V <sub>S</sub> = 14 V	1 2	0.1		1 100		5 100		
			V <sub>D</sub> = V <sub>S</sub> = -14 V	1 2	-0.1	-2 -200		-5 -200			
<b>INPUT</b>											
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	1 2,3	-0.001	-1 -1			-1		μA	
		V <sub>IN</sub> = 15 V	1 2,3	0.001		1 1		1			
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1 2,3	-0.001	-1 -1			-1			

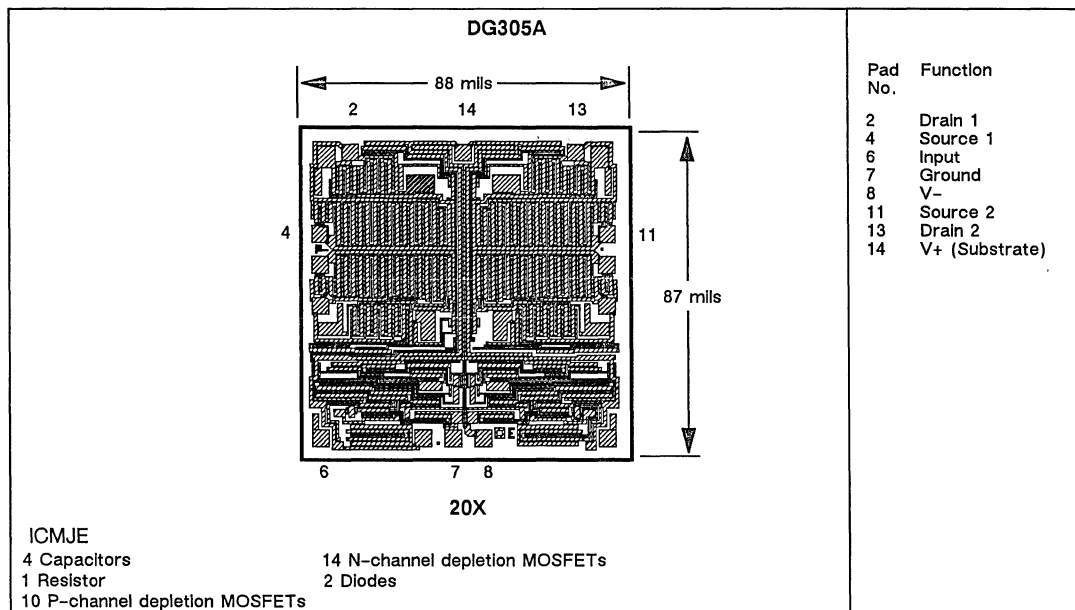
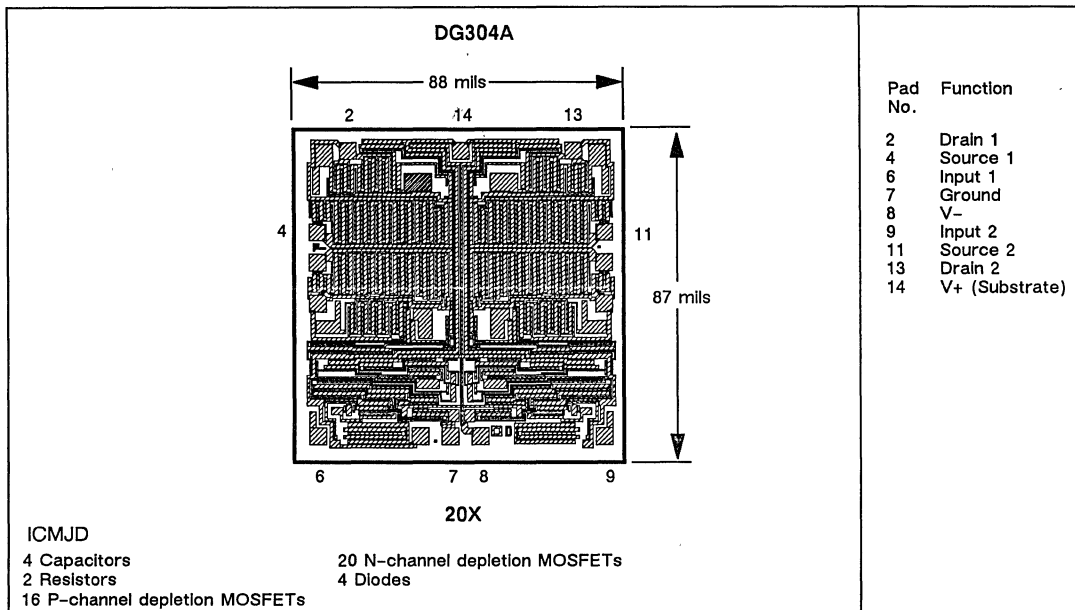
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B, C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1	110		250			ns
Turn-OFF Time	t <sub>OFF</sub>		1	70		150			
Break-Before-Make Interval	t <sub>ON</sub> - t <sub>OFF</sub>	See Break-Before-Make Test Time Circuit DG305A/307A ONLY	1	50					
Charge Injection	Q	C <sub>L</sub> = 0.01 μF, R <sub>gen</sub> = 1 Ω V <sub>gen</sub> = 0 V	1	30					pC
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>IN</sub> = 3.5 V or V <sub>IN</sub> = 11 V <sup>f</sup> f = 1 MHz	V <sub>S</sub> = 0 V	1	14				pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>			V <sub>D</sub> = 0 V	1	14			
Channel-ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		V <sub>S</sub> = V <sub>D</sub> = 0 V	1	40				
Input Capacitance	C <sub>IN</sub>	f = 1 MHz	V <sub>IN</sub> = 0 V	1	6				
			V <sub>IN</sub> = 15 V	1	7				
OFF Isolation <sup>g</sup>		V <sub>IN</sub> = 0 V R <sub>L</sub> = 1 kΩ V <sub>S</sub> = 1 V <sub>rms</sub> f = 500 kHz	1	62					dB
Crosstalk (Channel-to-Channel)			1	74					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 15 V (All Inputs)	1,3 2	0.001		10 100		100	μA
Negative Supply Current	I <sub>-</sub>		1,3 2	-0.001	-10 -100		-100		
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 V (All Inputs)	1,3 2	0.001		10 100		100	
Negative Supply Current	I <sub>-</sub>		1,3 2	-0.001	-10 -100		-100		

**NOTES:**

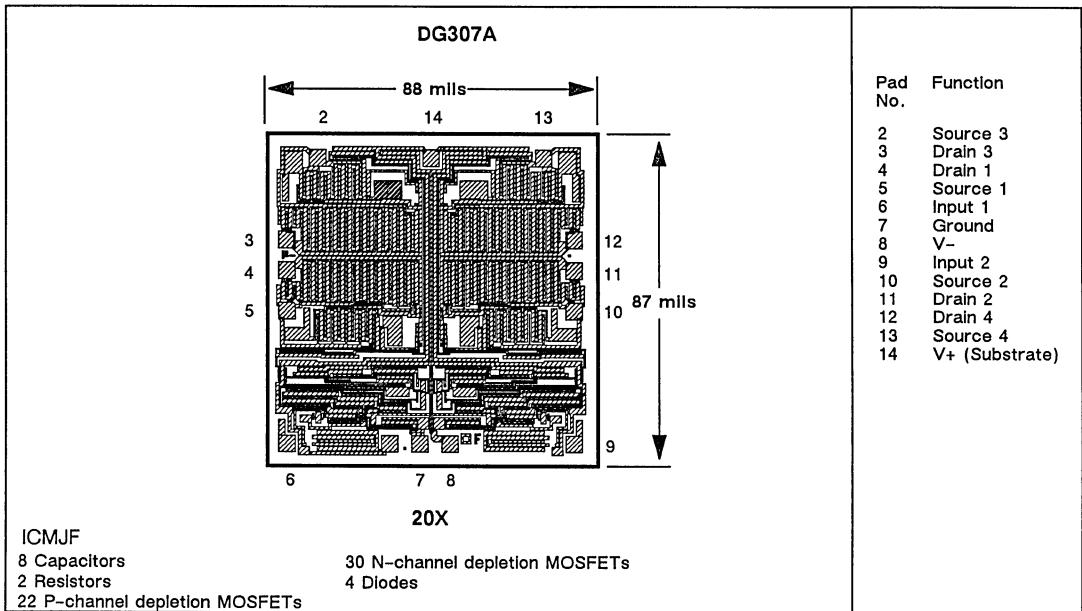
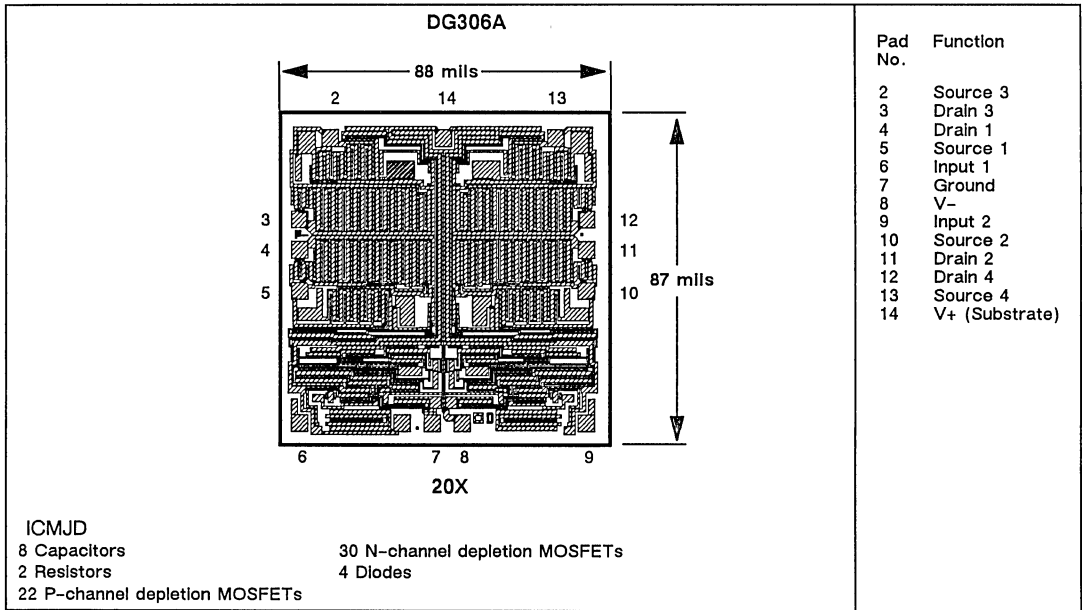
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Signals on S<sub>X</sub>, D<sub>X</sub>, or I<sub>NX</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
- V<sub>IN</sub> = Input voltage to perform proper function.
- OFF isolation = 20 log  $\frac{V_S}{V_D}$ . V<sub>S</sub> = input to OFF switch, V<sub>D</sub> = Output.

5

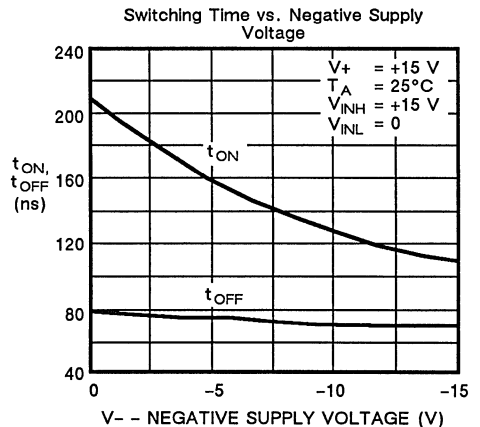
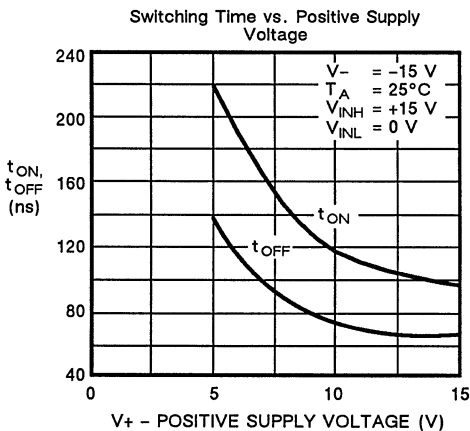
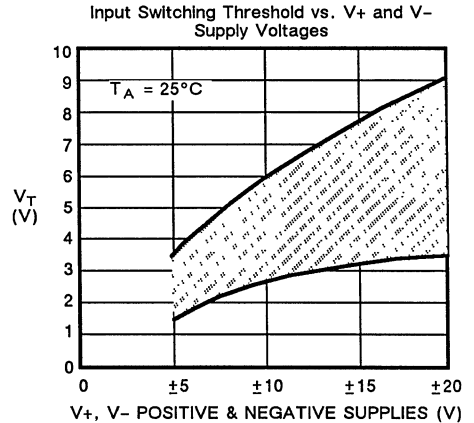
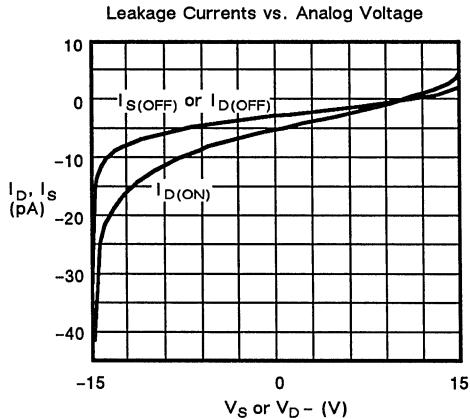
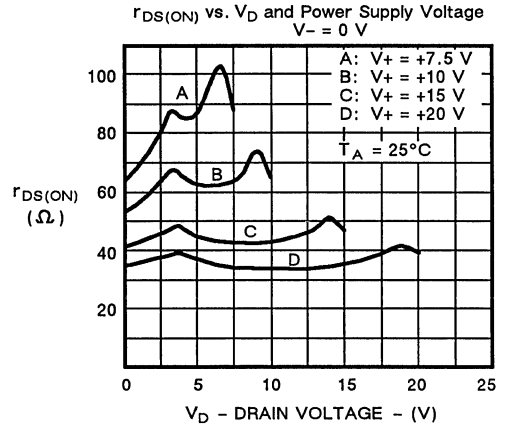
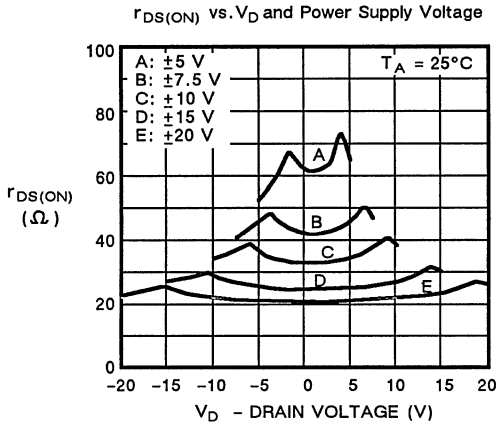
## DIE TOPOGRAPHY



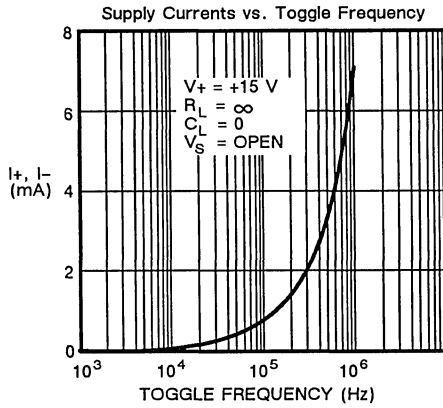
DIE TOPOGRAPHY (Cont'd)



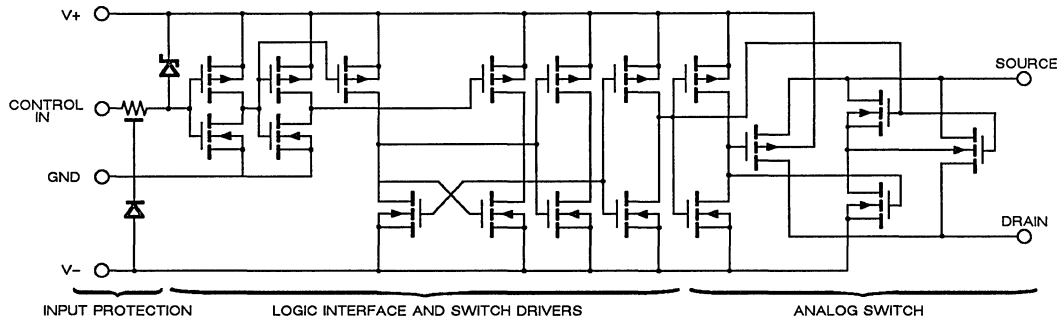
## TYPICAL CHARACTERISTICS



## TYPICAL CHARACTERISTICS (Cont'd)

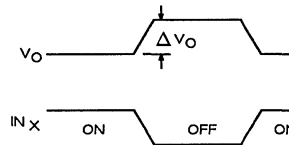
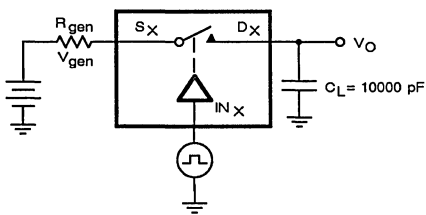


## SCHEMATIC DIAGRAM (Typical Channel)



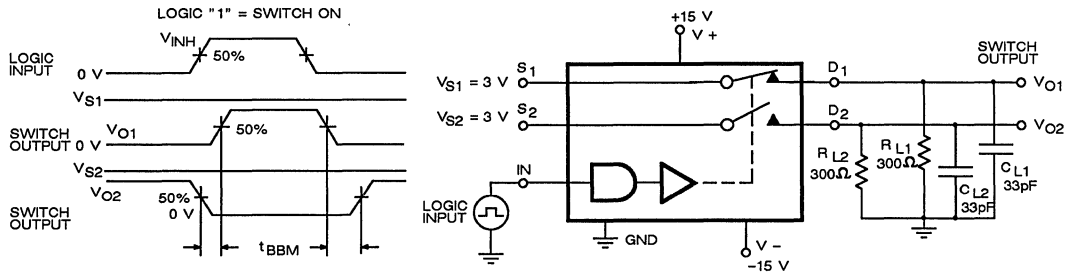
**5**

## CHARGE INJECTION TEST CIRCUIT

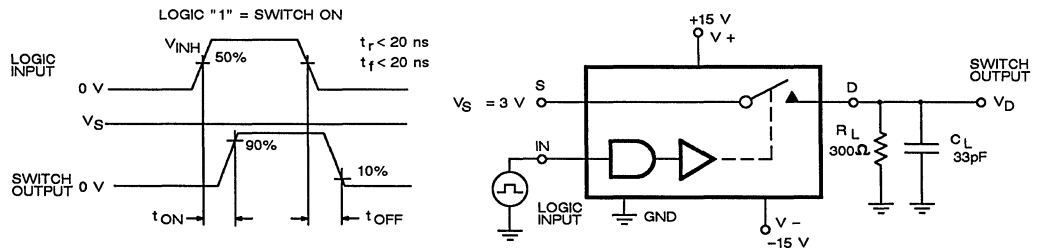


$\Delta V_O$  IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION  
 THE CHARGE INJECTION IN COULOMBS IS  $\Delta Q = C_L \times \Delta V_O$

## BREAK-BEFORE-MAKE TIME TEST CIRCUIT (DG305A, DG307A)



## SWITCHING TIME TEST CIRCUIT



## APPLICATION HINTS

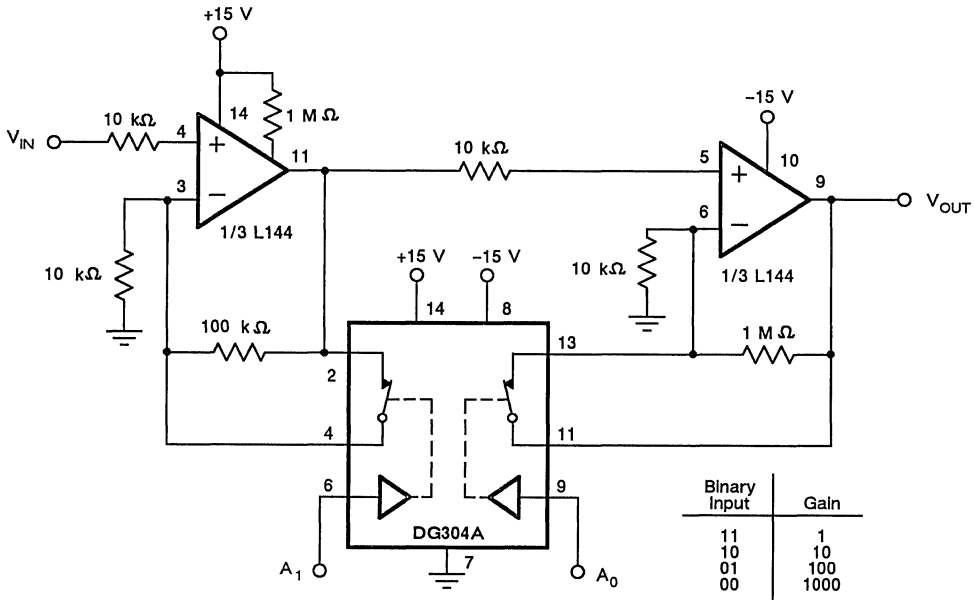
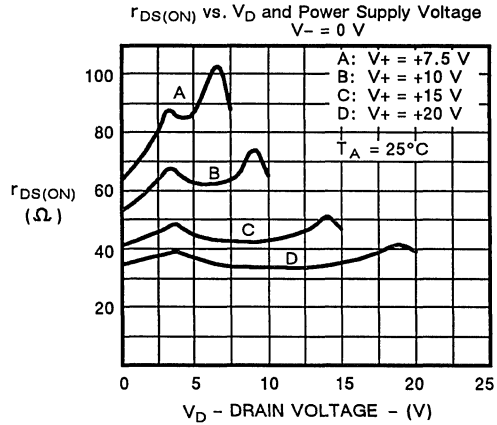
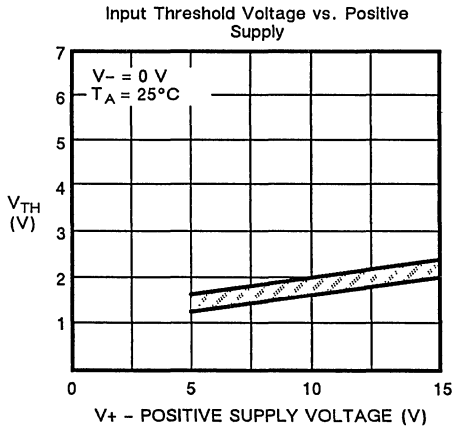
$V_+$ Positive Supply Voltage (V)	$V_-$ Negative Supply Voltage (V)	$V_{IN}$ Logic Input Voltage $V_{INH}$ Min/ $V_{INL}$ Max (V)	$V_S$ Analog Voltage Range (V)
15	-15	11/3.5	-15 to 15
20	-20	11/3.5	-20 to 20
15	0	11/3.5	0 to 15



## APPLICATIONS

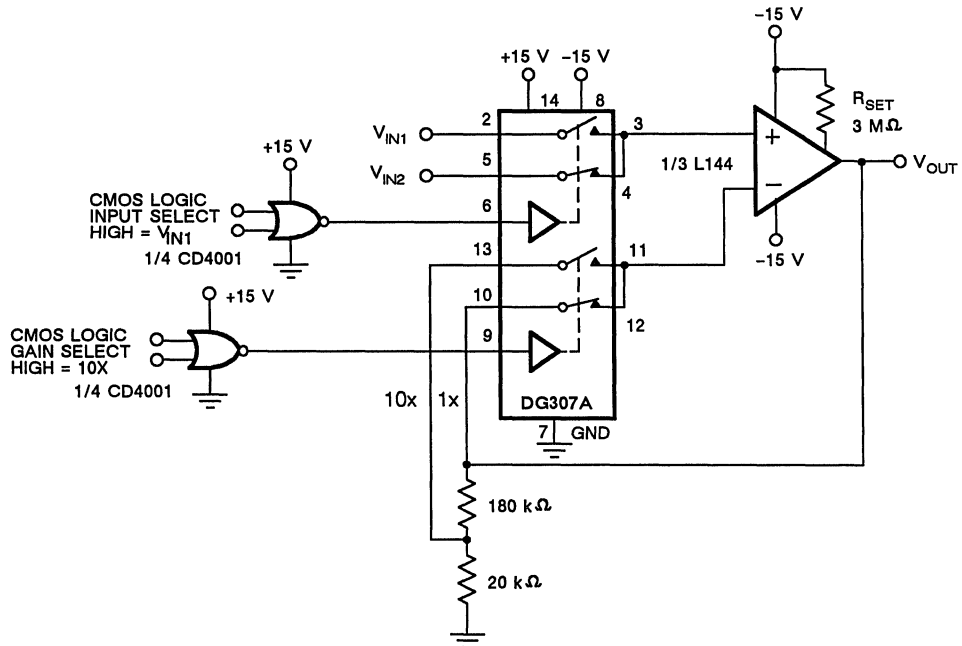
The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are: 1) Increased  $r_{DS(ON)}$ :

2) slower switching speed. Typical curves for design aid are given in the figures below. The analog voltage should not go above or below the supply voltages which in single operation are  $V_+$  and 0 volts.



Low Power Binary to  $10^n$  Gain  
Low Frequency Amplifier

## APPLICATIONS (Cont'd)



Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain

# DG308A/309

## Quad Monolithic SPST CMOS Analog Switches

### FEATURES

- $\pm 15$  V Input Range
- Low ON Resistance < 60  $\Omega$ , typ.
- Fast Switching < 130 ns, typ.
- Low Power Dissipation < 30  $\mu$ W, typ.
- CMOS Logic Compatible

### BENEFITS

- Rail-to-Rail Analog Signal Range
- Low Signal Errors
- Wide Dynamic Range
- Single or Dual Supply Capability
- Static Protected Logic Inputs

### APPLICATIONS

- Portable, Battery Instrumentation
- Communication Systems
- Computer Peripherals
- High Speed Multiplexing

### DESCRIPTION

The DG308A and DG309 are quad single-pole single-throw analog switches designed for high speed switching applications in communications, instrumentation, and process control. This series is well suited for applications requiring nearly a constant ON resistance over the entire analog range.

Featuring low ON resistance (< 60  $\Omega$ ) and fast switching (< 130 ns), the DG308A is supplied in the "normally-open" configuration while DG309 is supplied "normally-closed". Input thresholds are CMOS compatible.

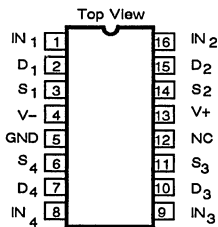
Designed with the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 44 V, each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. An epitaxial layer prevents latch up.

Packaging includes a 16-pin CerDIP and plastic DIP. Performance grades include military, A suffix (-55 to 125°C), commercial, C suffix (0 to 70°C), and industrial, B and D suffixes (-25, -40 to 85°C) temperature ranges. Additionally, both are offered in a 16-pin small outline package.



### PIN CONFIGURATION

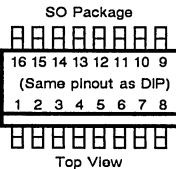
Dual-In-Line Package



Order Numbers:

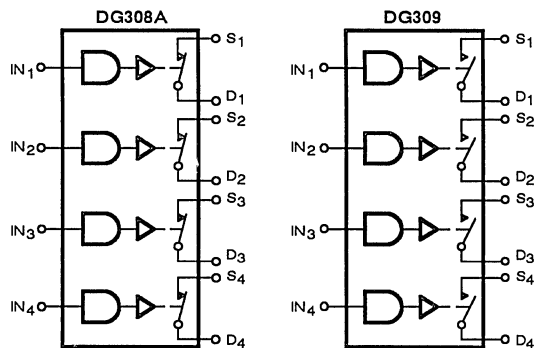
CerDIP:  
DG308AAK, DG308AAK/883  
DG308ABK, DG308ACK  
DG309AK, DG309AK/883  
DG309BK, DG309CK

Plastic:  
DG308ADJ or DG309DJ



Order Numbers:  
DG308ADY  
DG309DY

### FUNCTIONAL BLOCK DIAGRAM



Four SPST Switches per Package\*

Truth Table

LOGIC	DG308A	DG309
0	OFF	ON
1	ON	OFF

Logic "0" < 3.5 V  
Logic "1"  $\geq$  11 V

\* Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs, V<sub>S</sub>, V<sub>Df</sub> ..... (V-) -2 V to (V+) +2 V or  
..... 20 mA, whichever occurs first.

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D  
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature (A & B Suffix) ..... -65 to 150°C  
(C & D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
(B Suffix) ..... -25 to 85°C  
(C Suffix) ..... 0 to 70°C  
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*

16-Pin CerDIP\*\* ..... 900 mW

16-Pin Plastic DIP\*\*\* ..... 470 mW

16-Pin Plastic SO\*\*\*\* ..... 950 mW

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6.5 mW/°C above 25°C.

\*\*\*\* Derate 7.7 mW/°C above 25°C.

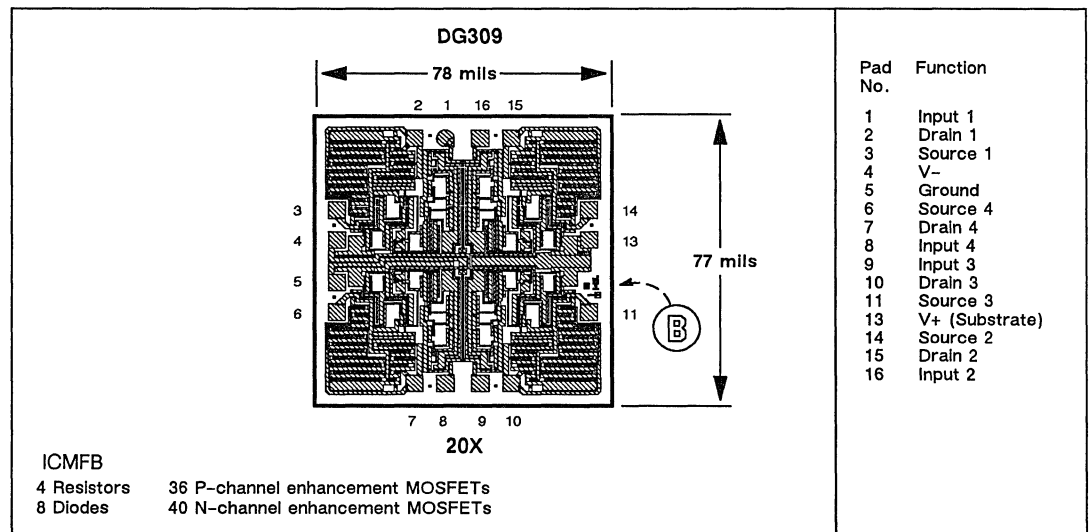
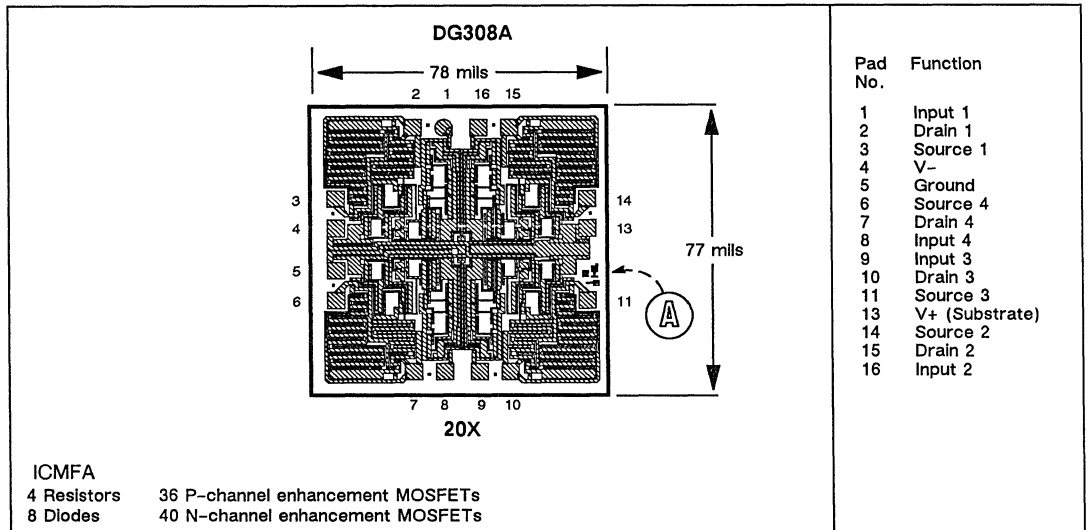
ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V		LIMITS						UNIT
				1=25°C 2=125,85,70°C 3=-55,-40,0 °C		A SUFFIX -55 to 125°C		B,C,D SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>IN</sub> = 11 V (DG308A)	V <sub>D</sub> = 10 V I <sub>S</sub> = 1 mA	1,3 2	60		100 150		100 125	Ω
		V <sub>IN</sub> = 3.5 V (DG309)	V <sub>D</sub> = -10 V I <sub>S</sub> = 1 mA	1,3 2	60		100 150		100 125	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>IN</sub> = 3.5 V (DG308A) V <sub>IN</sub> = 11 V (DG309)	V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	0.1		1 100		5 100	nA
			V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	-0.1	-1 -100		-5 -100		
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>D</sub> = 14 V V <sub>S</sub> = -14 V	1 2	0.1		1 100		5 100	
			V <sub>D</sub> = -14 V V <sub>S</sub> = 14 V	1 2	-0.1	-1 -100		-5 -100		
Drain ON Leakage Current <sup>f</sup>	I <sub>D(ON)</sub>	V <sub>IN</sub> = 11 V (DG308A)	V <sub>D</sub> = V <sub>S</sub> = 14 V	1 2	0.1		1 100		5 200	
		V <sub>IN</sub> = 3.5 V (DG309)	V <sub>D</sub> = V <sub>S</sub> = -14 V	1 2	-0.1	-2 -100		-5 -200		
<b>INPUT</b>										
Input Current with Input Voltage HIGH	I <sub>INH</sub>		V <sub>IN</sub> = 15 V	1,2	0.001		1		1	μA
Input Current with Input Voltage LOW	I <sub>INL</sub>		V <sub>IN</sub> = 0 V	1,2	-0.001	-1		-1		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = +15 V V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		B, C, D SUFFIX			
			2=125, 85, 70°C		-55 to 125°C					
		3=-55, -40, 0 °C		MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
				TEMP	TYP <sup>d</sup>					
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit	1	130		200		200	ns	
Turn-OFF Time	t <sub>OFF</sub>		1	90		150		150		
Charge Injection	Q	C <sub>L</sub> = 0.01 μF, V <sub>gen</sub> = 0 V R <sub>gen</sub> = 0 Ω	1	-10					pC	
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 140 kHz	1	11					pF	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>									V <sub>S</sub> = 0 V V <sub>IN</sub> = 0 V (DG308A) V <sub>IN</sub> = 15 V (DG309)
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>									V <sub>D</sub> = 0 V V <sub>IN</sub> = 0 V (DG308A) V <sub>IN</sub> = 15 V (DG309)
OFF Isolation <sup>e</sup>		Z <sub>L</sub> = 75 Ω, V <sub>S</sub> = 2 V <sub>p-p</sub> , f = 500 kHz V <sub>IN</sub> = 0 V (DG308A) V <sub>IN</sub> = 15 V (DG309)	1	78					dB	
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	All Channels ON or OFF V <sub>IN</sub> = 0 V or 15 V	1	0.001		10		100	μA	
Negative Supply Current	I <sub>-</sub>		2	-0.001	-10		-100			

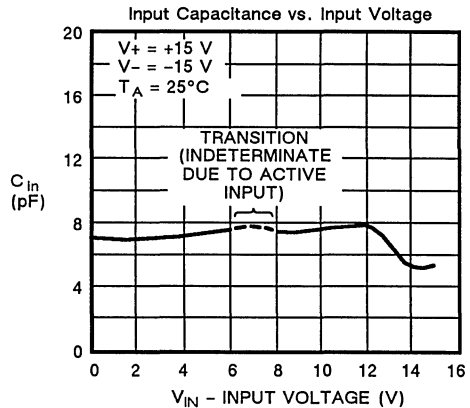
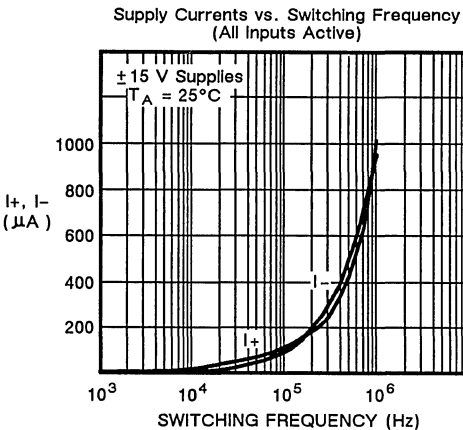
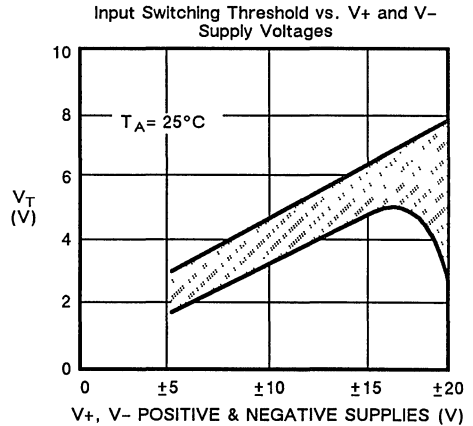
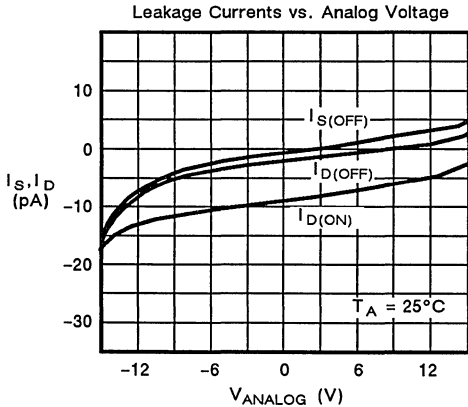
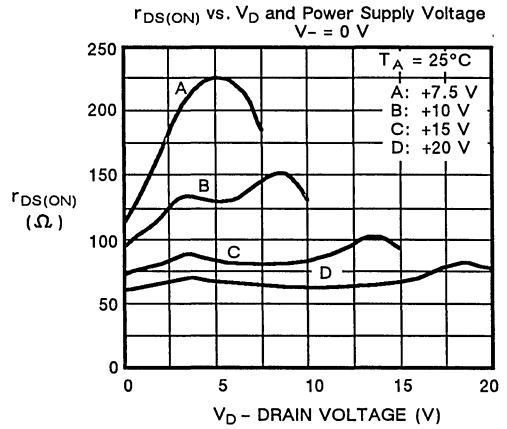
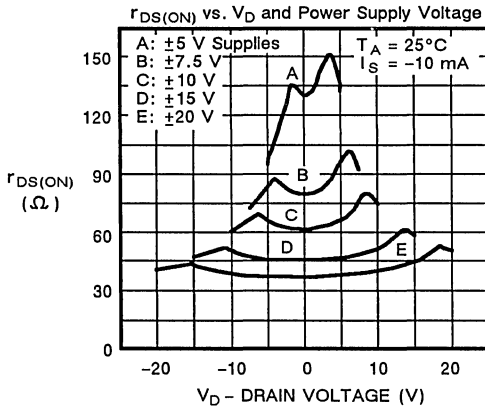
**NOTES:**

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- OFF Isolation = 20 log<sub>10</sub>  $\frac{V_D}{V_S}$ , V<sub>D</sub> = Output, V<sub>S</sub> = Input to OFF Switch.
- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current rating.

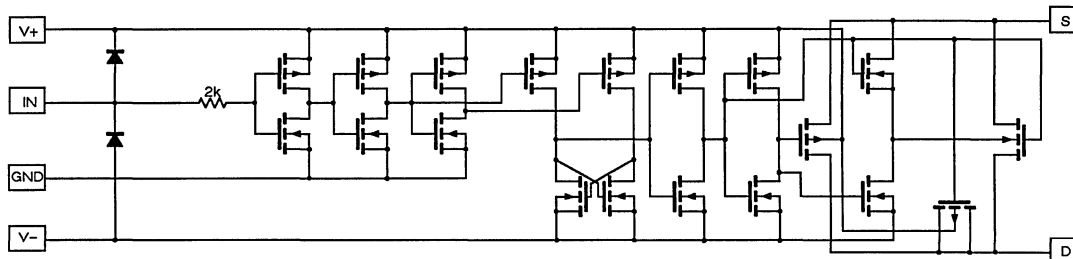
## DIE TOPOGRAPHY



**TYPICAL CHARACTERISTICS**

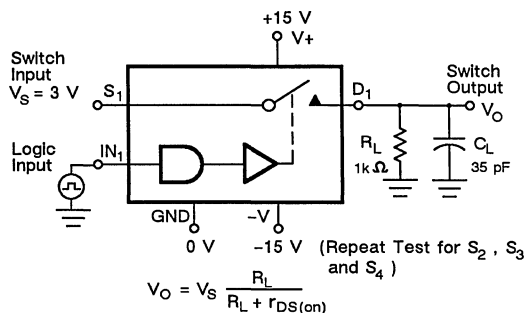
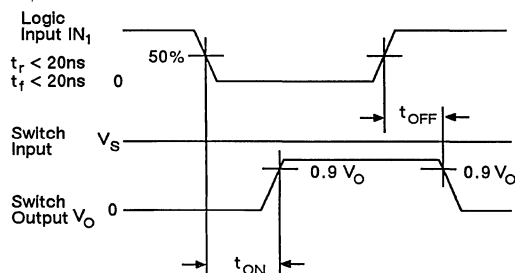


## SCHEMATIC DIAGRAM (Typical Channel)



## SWITCHING TIME TEST CIRCUIT

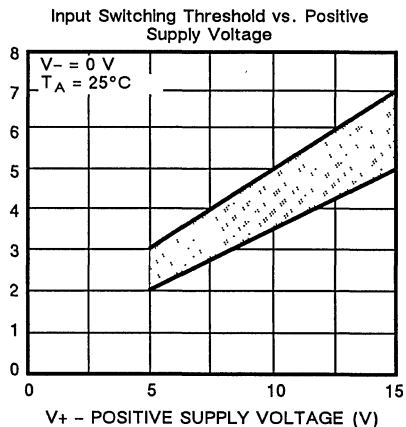
Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



## APPLICATIONS

### Single Supply Operation

The DG308A and DG309 will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased  $r_{DS(ON)}$ ; 2) slower switching speed. typical curve for aid in designing with single supplies are supplied in the figure below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are  $V_+$  and 0 volts.





# DG381A/384A/387A/390A

## General Purpose CMOS Analog Switches

### FEATURES

- $\pm 15$  V Input Range
- Low  $r_{DS(ON)}$  ( $< 75 \Omega$ )
- Single Supply Operation
- Pin and Function Compatible with the JFET DG180 Family

### BENEFITS

- Full Rail to Rail Analog Signal Range
- Minimizes Signal Error
- Low Power Dissipation

### APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable Battery Operation

### DESCRIPTION

The DG38XA series of monolithic CMOS analog switches was designed for applications in instrumentation, communications, and process control. This series is suited for applications requiring fast switching and nearly flat ON resistance over the entire voltage range.

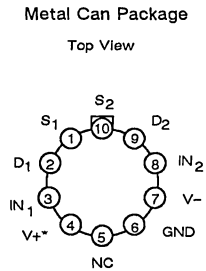
Designed on Siliconix' PLUS-40 CMOS process, the DG38XA series achieves low power consumption (3 mW typical) and excellent ON/OFF switch performance. This switch is ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents

latchup. Single supply operation is allowed by connecting the V- rail to 0 volts.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. These switches are quasi TTL and CMOS logic compatible.

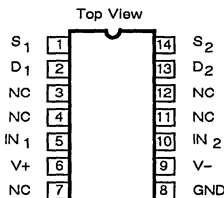
Packaging for this series includes the 14-pin CerDIP for the DG381A/DG387A, and the 16-pin CerDIP for the DG384A/DG390A. A 10-pin metal can option is available for the DG381A/DG387A. All devices are available in the plastic DIP version. Performance grades include the military, A suffix (-55 to 125°C), commercial, C suffix (0 to 70°C), and industrial, B suffix (-25 to 85°C) temperature ranges.

### PIN CONFIGURATION



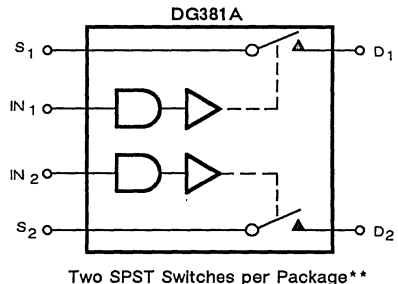
Order Numbers:  
DG381AAA, DG381ABA  
\*(SUBSTRATE & CASE)

Dual-In-Line Package



Order Numbers:  
CerDIP: DG381AAK, DG381AAK/883  
DG381ABK, DG381ACK  
Plastic: DG381ACJ

### FUNCTIONAL BLOCK DIAGRAM



LOGIC	SWITCH
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 4.0$  V

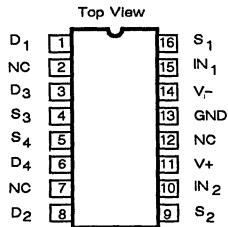
\*\*Switches Shown for Logic "1" Input

# DG381A/384A/387A/390A

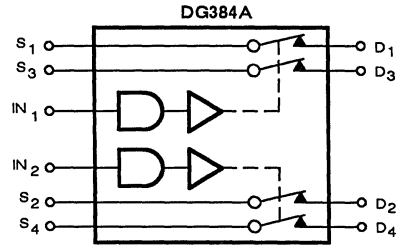
## PIN CONFIGURATION (Cont'd)

## FUNCTIONAL BLOCK DIAGRAM (Cont'd)

### Dual-In-Line Package



Order Numbers:  
CerDIP: DG384AAK, DG384AAK/883  
DG384ABK, DG384ACK  
Plastic: DG384ACJ

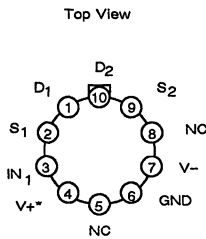


Two DPST Switches per Package \*

#### TRUTH TABLE\*\*

LOGIC	SWITCH
0	OFF
1	ON

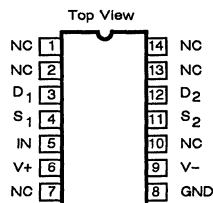
### Metal Can Package



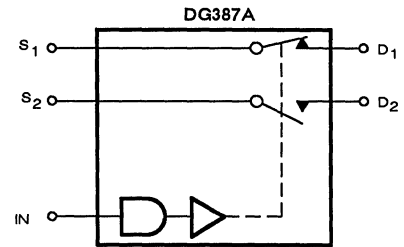
Order Numbers:  
DG387AAA, DG387AAA/883  
DG387ABA, DG387ACA

\*(Substrate and Case)

### Dual-In-Line Package



Order Numbers:  
CerDIP: DG387AAK, DG387AAK/883  
DG387ABK, DG387ACK  
Plastic: DG387ACJ

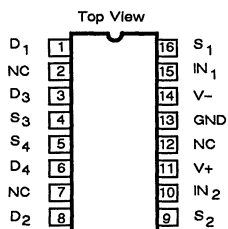


One SPDT Switch per Package \*

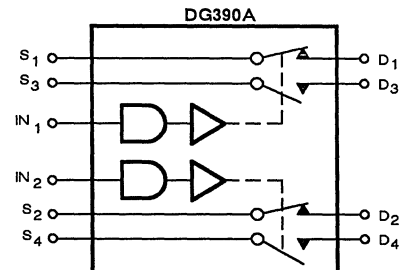
#### TRUTH TABLE\*\*

LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

### Dual-In-Line Package



Order Numbers:  
CerDIP: DG390AAK, DG390AAK/883  
DG390ABK, DG390ACK  
Plastic: DG390ACJ



Two SPDT Switches per Package \*

#### TRUTH TABLE\*\*

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

\* Switches Shown for Logic "1" Input  
\*\* Logic "0" ≤ 0.8 V, Logic "1" ≥ 4.0 V

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs, V<sub>S</sub>, V<sub>D</sub><sup>e</sup> ..... (V-) -2 V to (V+) +2V or  
..... 30 mA, whichever occurs first.

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA  
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A & B Suffix) ..... -65 to 150°C  
(C Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
(B Suffix) ..... -25 to 85°C  
(C Suffix) ..... 0 to 70°C

Power Dissipation\*

14-Pin CerDip (K)\*\* ..... 825 mW

14-Pin Plastic DIP (J)\*\*\* ..... 470 mW

10-Pin Metal Can (A)\*\*\*\* ..... 450 mW

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 11 mW/°C above 75°C.

\*\*\* Derate 6.5 mW/°C above 25°C.

\*\*\*\* Derate 6 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: V+ = 15 V V- = -15 V GND = 0V	LIMITS						UNIT		
			1=25°C 2=125,85,70°C 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B, C SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>	I <sub>S</sub> = 10 mA V <sub>IN</sub> = 0.8 V to 4.0 V <sup>f</sup>	1,2,3		-15	15	-15	15	V		
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>IN</sub> = 0.8 V or V <sub>IN</sub> = 4.0 V <sup>f</sup>	V <sub>D</sub> = 10 V I <sub>S</sub> = -10 mA	1,3 2	30		50 75		50 75	Ω	
			V <sub>D</sub> = -10 V I <sub>S</sub> = 10 mA	1,3 2	30		50 75		50 75		
Source OFF Leakage Current	I <sub>S(OFF)</sub>		V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	0.1		1 100			5 100	nA
			V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	-0.1	-1 -100			-5 -100		
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>S</sub> = -14 V V <sub>D</sub> = 14 V	1 2	0.1	-1 -100			-5 -100		
			V <sub>S</sub> = 14 V V <sub>D</sub> = -14 V	1 2	-0.1		1 100			5 100	
Drain ON Leakage Current	I <sub>D(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 14 V	1 2	0.1		1 100			5 100		
		V <sub>D</sub> = V <sub>S</sub> = -14 V	1 2	-0.1	-2 -200			-5 -200			
<b>INPUT</b>											
Input Current with Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V	1 2,3	-0.001	-1 -1			-1		μA	
		V <sub>IN</sub> = 15 V	1 2,3	0.001		1 1			1		
Input Current with Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1 2,3	-0.001	-1 -1			-1			

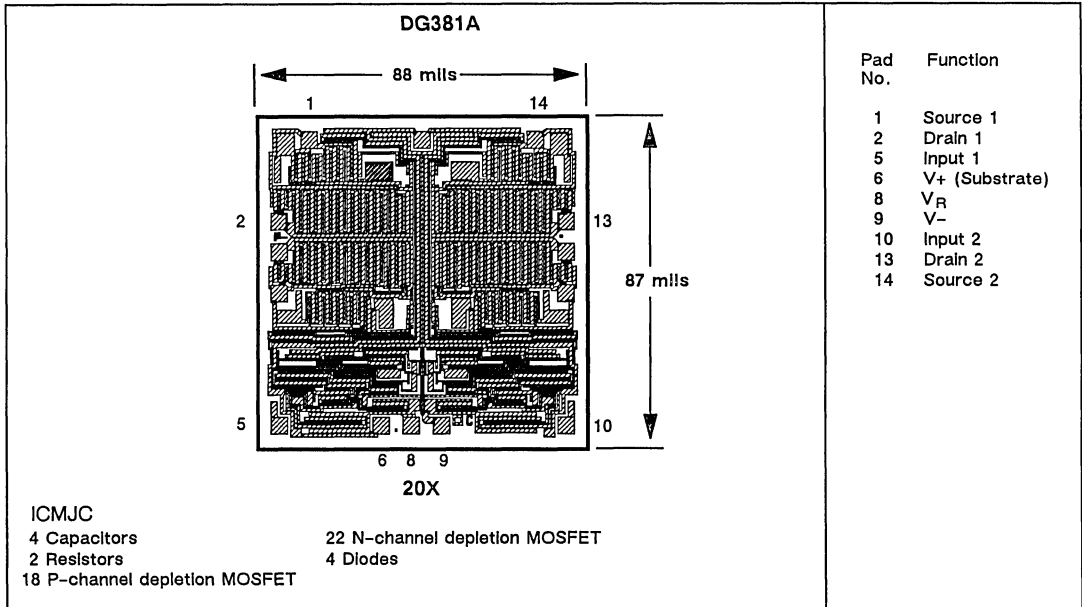


ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless otherwise specified: $V_+ = 15\text{ V}$ $V_- = -15\text{ V}$ $GND = 0\text{ V}$	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B, C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>									
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit	1	150		300			ns
Turn-OFF Time	$t_{OFF}$		1	130		250			
Break-Before-Make Interval	$t_{ON} - t_{OFF}$	See Break-Before-Make Test Time Circuit DG387A/390A ONLY	1	50					
Charge Injection	Q	$C_L = 0.01\ \mu\text{F}$ , $R_{gen} = 0\ \Omega$ $V_{gen} = 0\text{ V}$	1	10					pC
Source-OFF Capacitance	$C_{S(OFF)}$	$V_{IN} = 0.8\text{ V}$ or $V_{IN} = 4.0\text{ V}^f$ $f = 1\text{ MHz}$	$V_S = 0\text{ V}$	1	14				pF
Drain-OFF Capacitance	$C_{D(OFF)}$		$V_D = 0\text{ V}$	1	14				
Channel-ON Capacitance	$C_{D(ON)} + C_{S(ON)}$		$V_S = V_D = 0$	1	40				
Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$	$V_{IN} = 0\text{ V}$	1	6				
			$V_{IN} = 15\text{ V}$	1	7				
OFF Isolation <sup>f</sup>		$V_{IN} = 0\text{ V}$ $R_L = 1\text{ k}\ \Omega$ $V_S = 1\text{ V}_{rms}$ $f = 500\text{ kHz}$	1	62					dB
Crosstalk (Channel-to-Channel)			1	74					
<b>SUPPLY</b>									
Positive Supply Current	I+	$V_{IN} = 4\text{ V}$ (One Input) (All Others = 0)	1,2 3	0.23		0.5 1.0		1	mA
Negative Supply Current	I-		1,3 2	-0.001	-10 -100		-100		
Positive Supply Current	I+	$V_{IN} = 0.8\text{ V}$ (All Inputs)	1,3 2	0.001		10 100		100	$\mu\text{A}$
Negative Supply Current	I-		1,3 2	-0.001	-10 -100		-100		

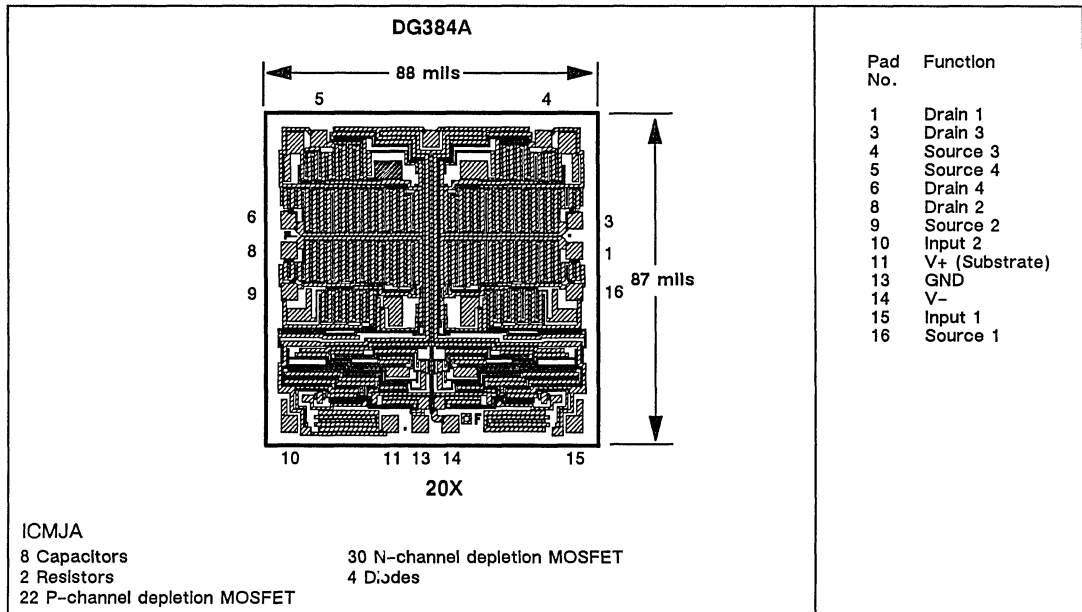
**NOTES:**

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Signals on  $S_X$ ,  $D_X$ , or  $IN_X$  exceeding  $V_+$  or  $V_-$  will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
- OFF Isolation:  $20 \log \frac{V_S}{V_D}$ .  $V_S$  = Input to OFF switch,  $V_D$  = Output.
- $V_{IN}$  = Input voltage to perform proper function.

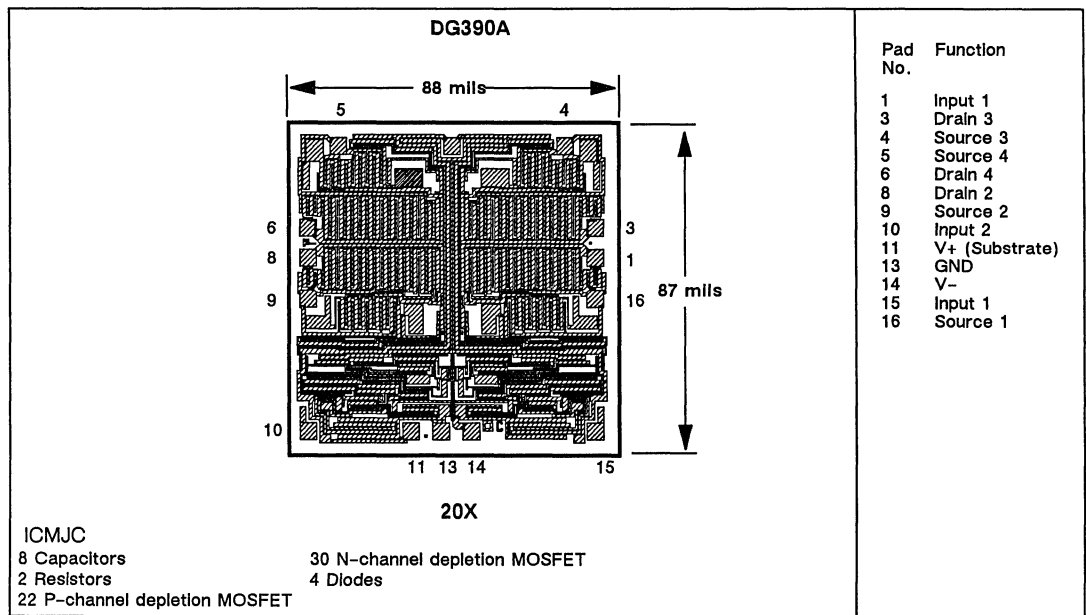
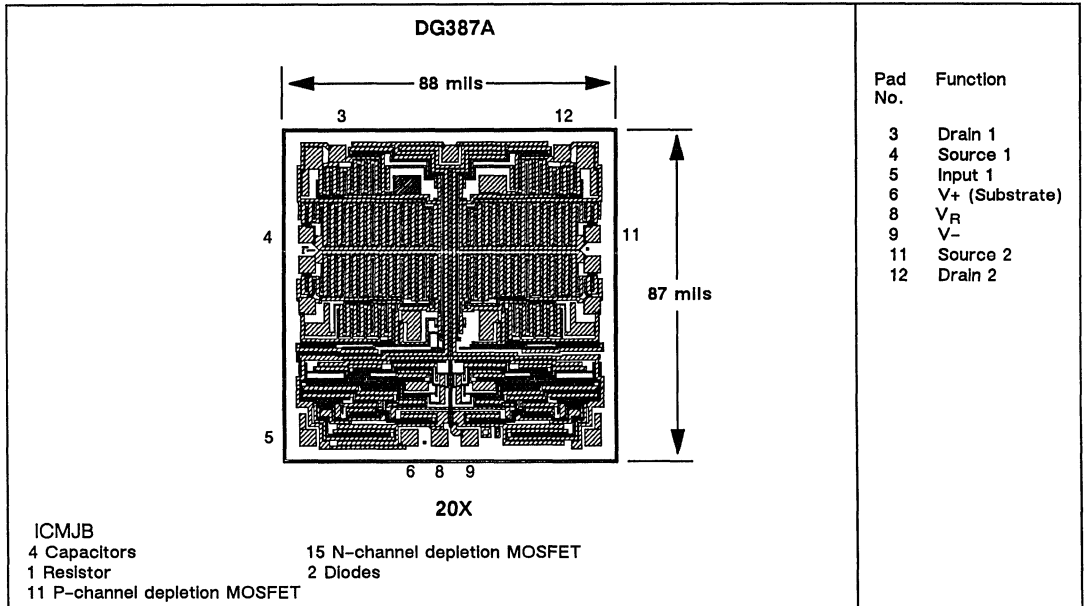
## DIE TOPOGRAPHY



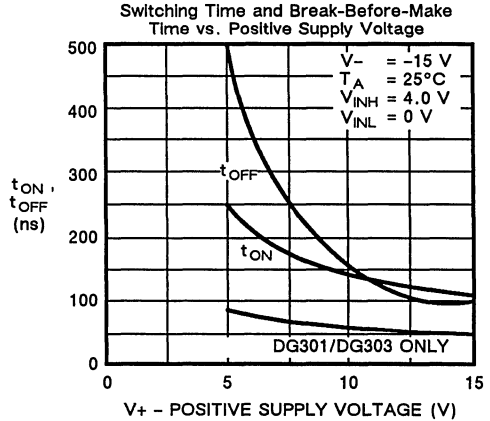
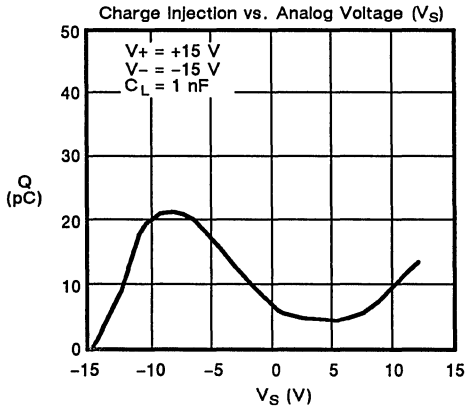
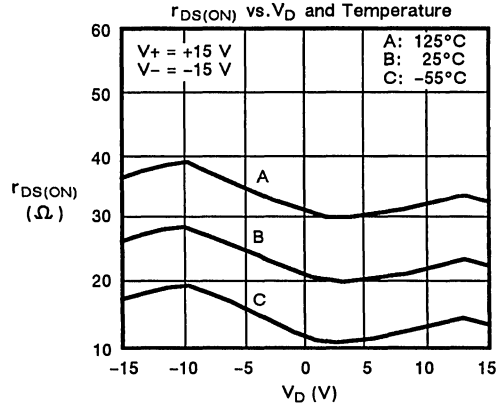
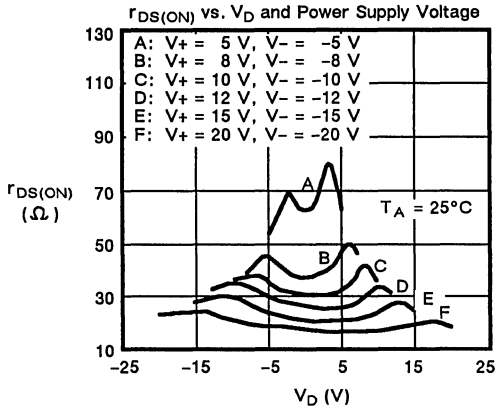
**5**



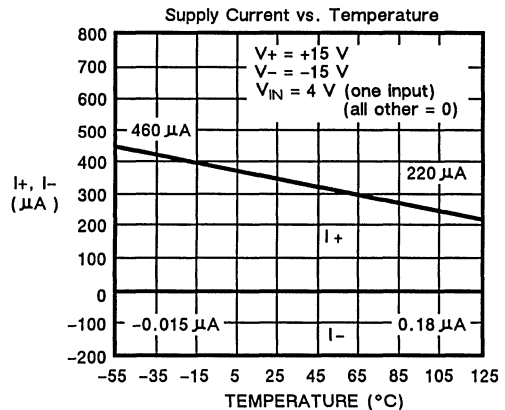
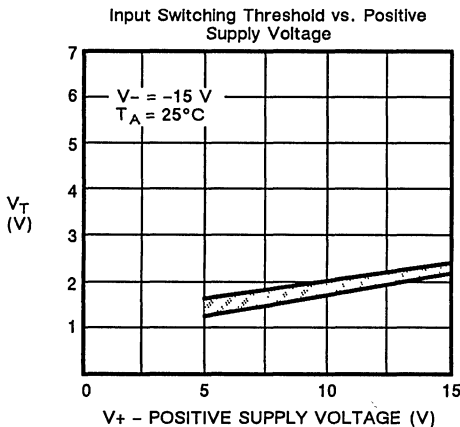
## DIE TOPOGRAPHY (Cont'd)



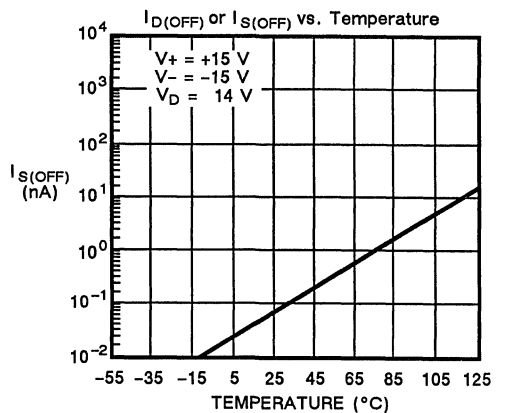
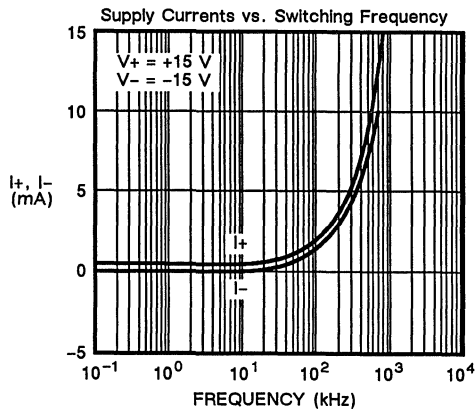
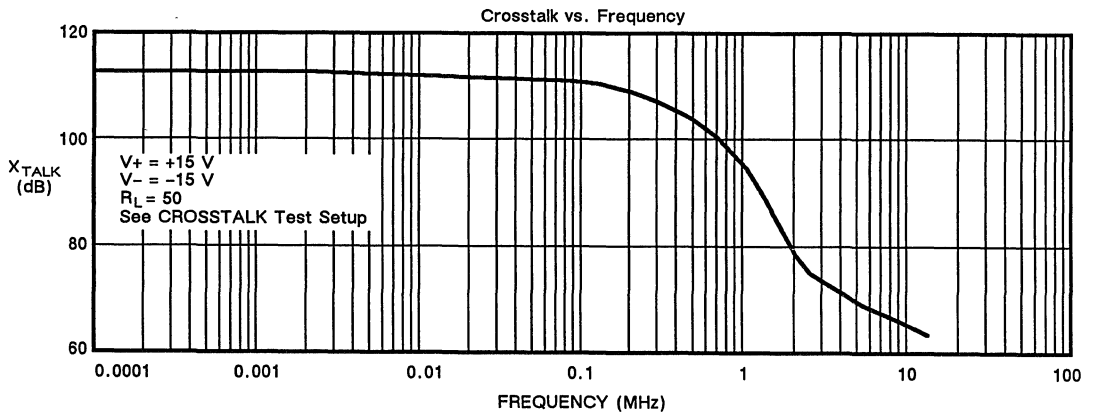
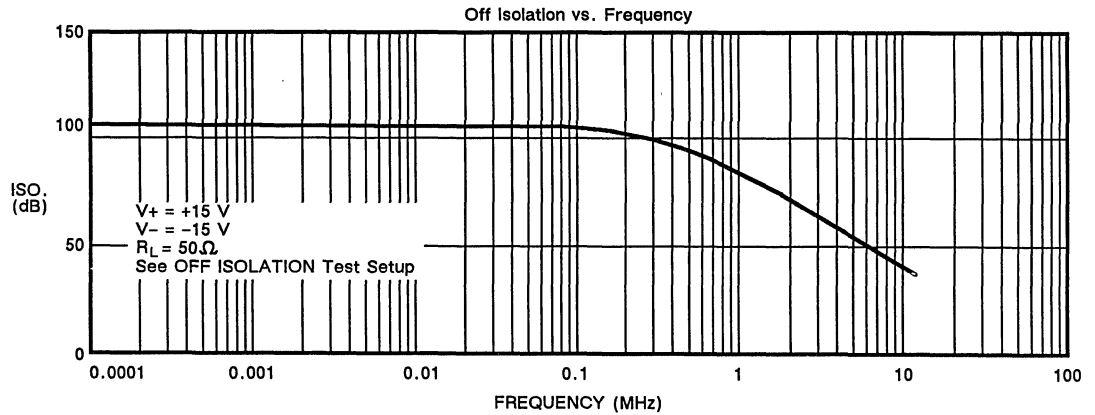
## TYPICAL CHARACTERISTICS



5

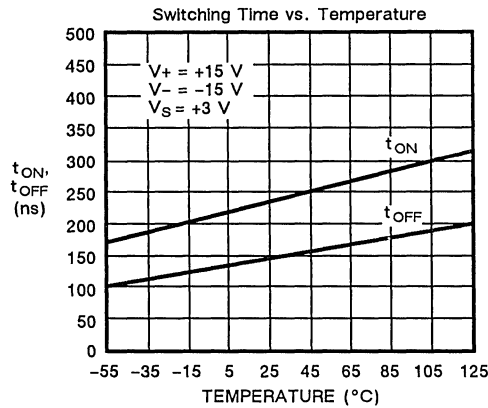
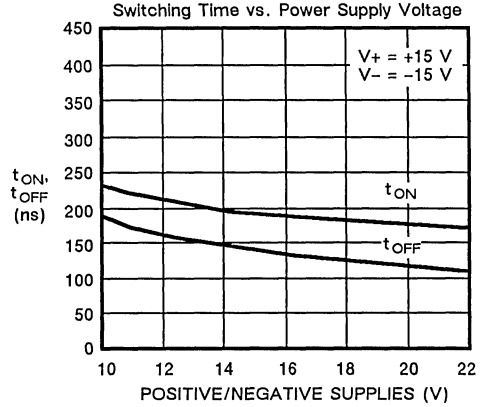
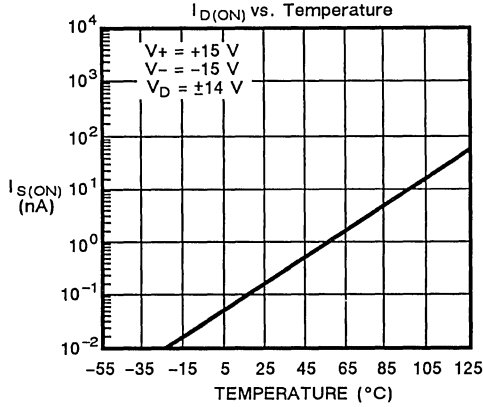


## TYPICAL CHARACTERISTICS (Cont'd)



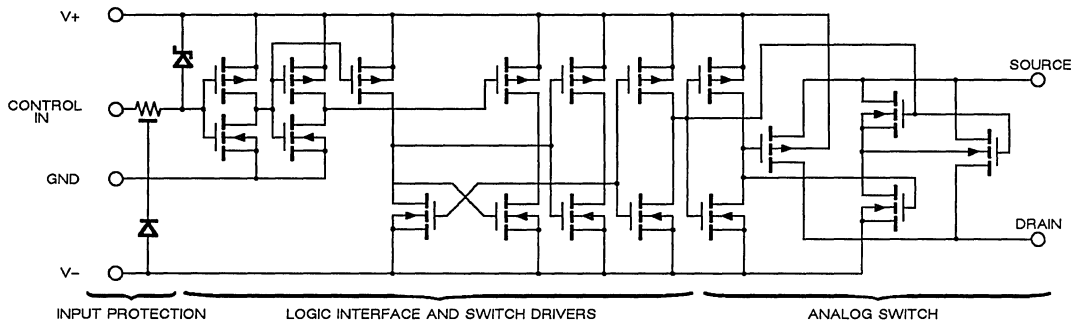


## TYPICAL CHARACTERISTICS (Cont'd)

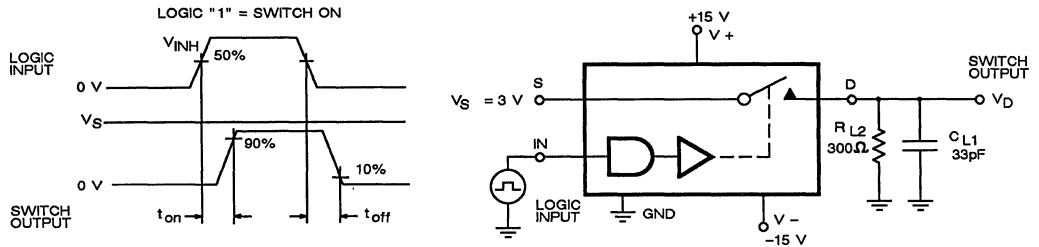


**5**

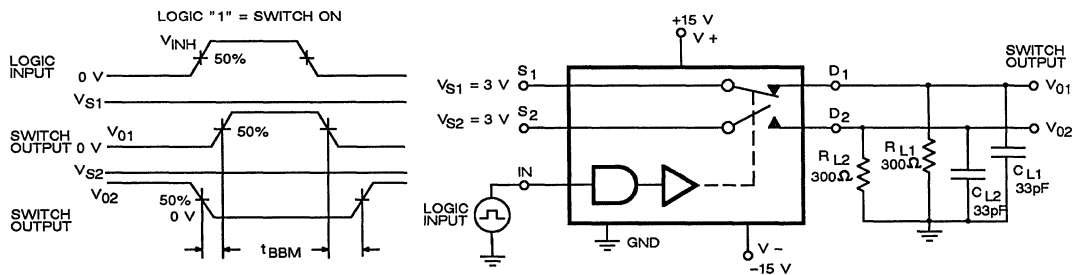
## SCHEMATIC DIAGRAM (Typical Channel)



## SWITCHING TIME TEST CIRCUIT



## BREAK-BEFORE-MAKE TIME TEST CIRCUIT SPDT (DG387A, DG390A)



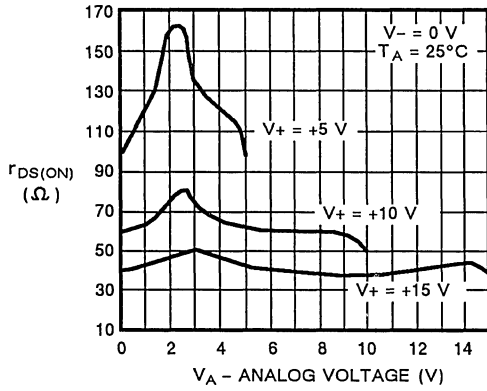
## APPLICATIONS

The DG38XA series of analog switches will switch positive analog signals while using a single positive supply. This allows their use in applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased  $r_{DS(ON)}$ ; 2) slower switching

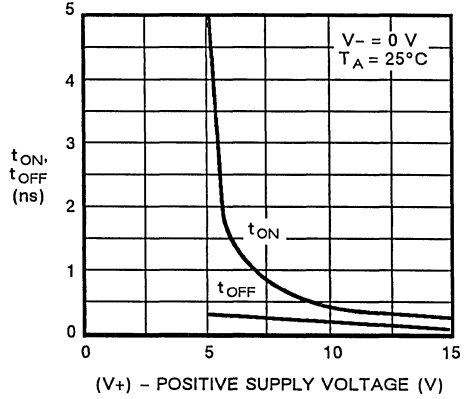
speed. Typical curves for aid in designing with single supplies are supplied in the figures below. The analog voltage should not go above or below the supply voltages which in single operation are  $V+$  and 0 volts.

APPLICATIONS (Cont'd)

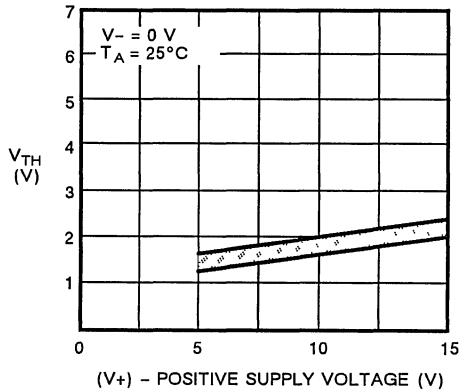
$r_{DS(ON)}$  vs. Analog and Positive Supply Voltage With  $V_- = 0$  V



Switching Time vs. ( $V_+$ ) - Positive Supply Voltage



Input Threshold Voltage vs. Positive Supply



## Low-Power – High-Speed CMOS Analog Switches

### FEATURES

- $\pm 15$  V Input Range
- ON Resistance < 35  $\Omega$
- Fast Switching Action  
 $t_{ON} < 150$  ns  
 $t_{OFF} < 100$  ns
- Ultra Low Power Requirements ( $P_D < 35$   $\mu$ W)
- TTL, CMOS Compatible

### BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

### APPLICATIONS

- High Performance Audio and Video Switching
- Sample and Hold Circuits
- Battery Operation

### DESCRIPTION

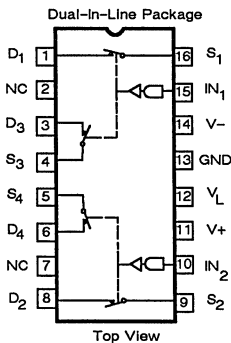
The DG400 family of monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (< 35  $\mu$ W) with high speed ( $t_{ON} < 150$  ns), the DG400 series is ideally suited for portable and battery powered industrial and military applications.

Built on the Siliconix proprietary high voltage silicon gate process to achieve high voltage rating and superior switch ON/OFF performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

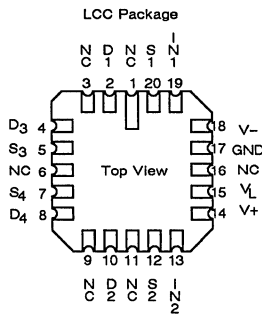
Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full  $\pm 15$  V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The six devices in this series are differentiated by the type of switch action as shown in the functional block diagrams. Package options include the 16-pin plastic, CerDIP and LCC package. Performance grades include industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ), and military, A suffix ( $-55$  to  $125^\circ\text{C}$ ). Additionally, the DG403 and DG405 are available in the narrow body surface mount package, SO-16.

### FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE



Order Numbers:  
 CerDIP: DG405AK  
 DG405AK/883  
 Plastic: DG405DJ



Order Number:  
 DG405AZ

### DG405

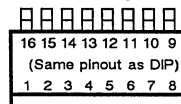
Two DPST Switches per Package

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V

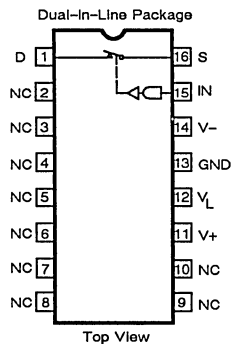
SO Package



(Same pinout as DIP)  
 1 2 3 4 5 6 7 8

Order Number:  
 DG405DY

## FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE (Cont'd)



Order Numbers:  
CerDIP: DG400AK  
DG400AK/883  
Plastic: DG400DJ

### DG400

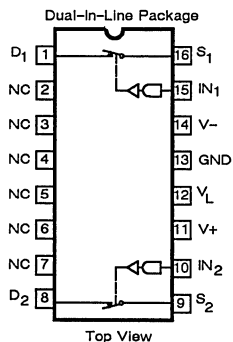
One SPST Switch per Package

Truth Table

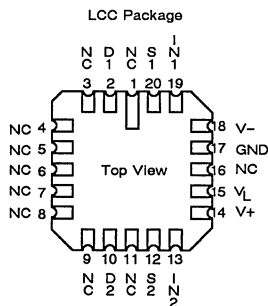
LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 "  $\leq$  0.8 V

Logic " 1 "  $\geq$  2.4 V



Order Numbers:  
CerDIP: DG401AK  
DG401AK/883  
Plastic: DG401DJ



Order Number:  
DG401AZ

### DG401

Two SPST Switches per Package

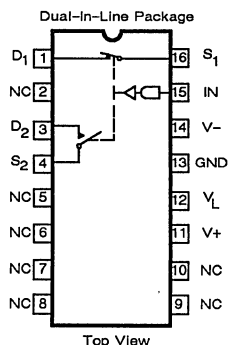
Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 "  $\leq$  0.8 V

Logic " 1 "  $\geq$  2.4 V

**5**



Order Numbers:  
CerDIP: DG402AK  
DG402AK/883  
Plastic: DG402DJ

### DG402

One SPDT Switch per Package

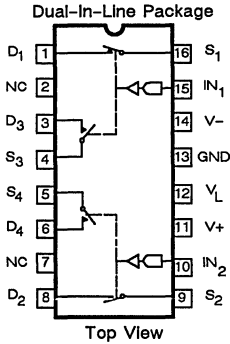
Truth Table

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Logic " 0 "  $\leq$  0.8 V

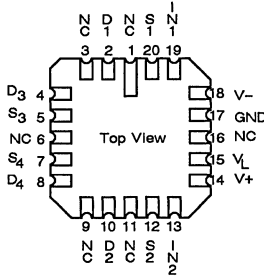
Logic " 1 "  $\geq$  2.4 V

## FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE (Cont'd)



Order Numbers:  
CerDIP: DG403AK  
          DG403AK/883  
Plastic: DG403DJ

Leadless Chip Carrier



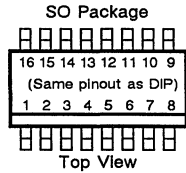
Order Number:  
DG403AZ

### DG403

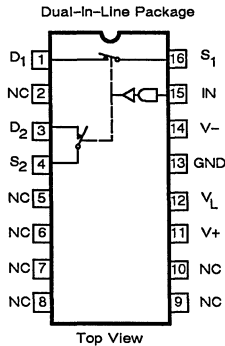
Two SPDT Switches per Package  
Truth Table

LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF	ON
1	ON	OFF

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.4 V



Order Number:  
DG403DY



Order Numbers:  
CerDIP: DG404AK  
          DG404AK/883  
Plastic: DG404DJ

### DG404

One DPST Switch per Package

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.4 V

## ABSOLUTE MAXIMUM RATINGS

V+ to V-	44V
GND to V-	25V
VL to V-	(GND - 0.3 V) to 44 V
Digital Inputs <sup>1</sup> VS, VD	(V-) -2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous	30 mA
Current, S or D (Pulsed 1 ms 10% duty)	100 mA
Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	-55 to 125°C
(D Suffix)	-40 to 85°C

### Power Dissipation (Package)\*

16-Pin Plastic DIP**	450 mW
16-Pin CerDIP***	900 mW
20-Pin LCC****	750 mW
16-Pin SO*****	600 mW

\* All leads welded or soldered to PC board.

\*\* Derate 6 mW/°C above 75°C

\*\*\* Derate 12 mW/°C above 75°C

\*\*\*\* Derate 10 mW/°C above 75°C

\*\*\*\*\* Derate 7.6 mW/°C above 75°C

<sup>1</sup> Signals on Sx, Dx or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V GND = 0 V V <sub>IN</sub> = 2.4V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX 2=125,85°C		D SUFFIX 3=-55,-40°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>				-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>+</sub> = 13.5 V, V <sub>-</sub> = -13.5 V I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±10 V	1 2,3	20		35 45		45 55	Ω
Delta Drain-Source ON Resistance	Δr <sub>DS(ON)</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V I <sub>S</sub> = -10 mA, V <sub>D</sub> = 5, 0, -5 V	1 2,3	3.0		3.0 5.0		3.0 5.0	
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>D</sub> = -15.5 V, V <sub>S</sub> = 15.5 V	1 2	-.01	-0.25 -20	0.25 20	-0.50 -20	0.50 20	nA
	I <sub>D(OFF)</sub>	V <sub>D</sub> = 15.5 V, V <sub>S</sub> = -15.5 V	1 2	-.01	-0.25 -20	0.25 20	-0.50 -20	0.50 20	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>D</sub> = V <sub>S</sub> = ±15.5 V	1 2		-0.4 -40	0.4 40	-1.0 -40	1.0 40	
<b>INPUT</b>									
Input Current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0.8 V All Other = 2.4 V	1,2	.005	-1.0	1.0	-1.0	1.0	μA
Input Current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 2.4 V All Other = 0.8 V	1,2	.005	-1.0	1.0	-1.0	1.0	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF See Figure 1A	1	100		150		150	ns
Turn-OFF Time	t <sub>OFF</sub>		1	60		100		100	
Break-Before-Make Time Delay	t <sub>D</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF DG402/DG403	1	20	10.0		10.0		
Charge Injection	Q	C <sub>L</sub> = 10,000 pF V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	1	60		100		100	pC
Off Isolation		R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	1	72					dB
Crosstalk <sup>f</sup> (Channel-to-Channel)		Any Other Channel Switches R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	1	90					
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V f = 1 MHz	1	12					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		1	12					
Drain and Source ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		1	39					

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V GND = 0 V V <sub>IN</sub> = 2.4V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	

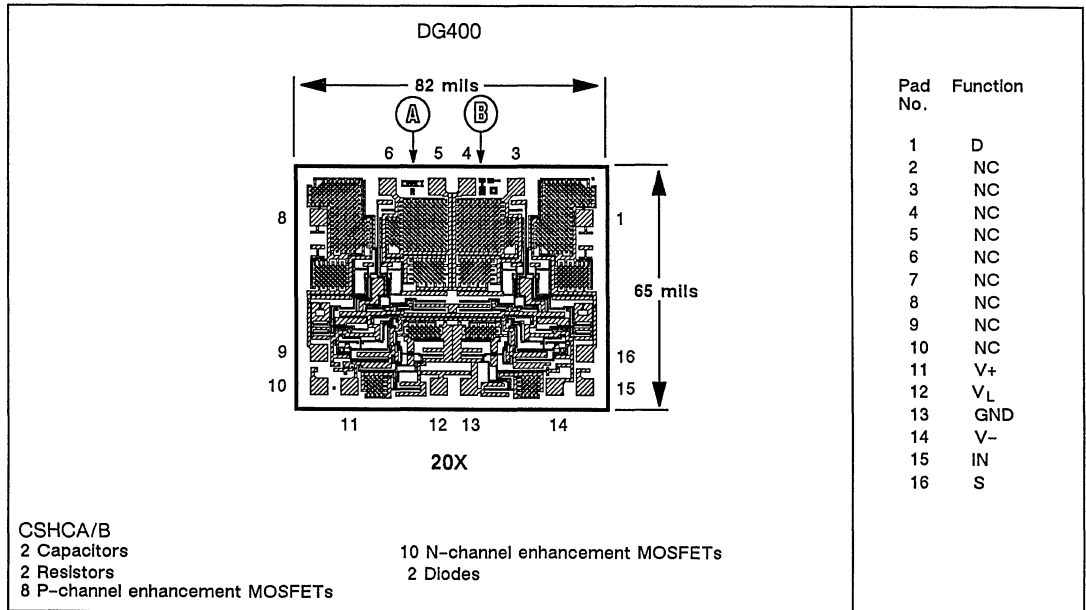
## SUPPLY

Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0.0 or 5.0 V	1	0.01		1		1	μA
Negative Supply Current	I <sub>-</sub>		2,3			5		5	
Logic Supply Current	I <sub>L</sub>		1	0.01		1		1	
Ground Current	I <sub>GND</sub>		2,3			5		5	

### NOTES:

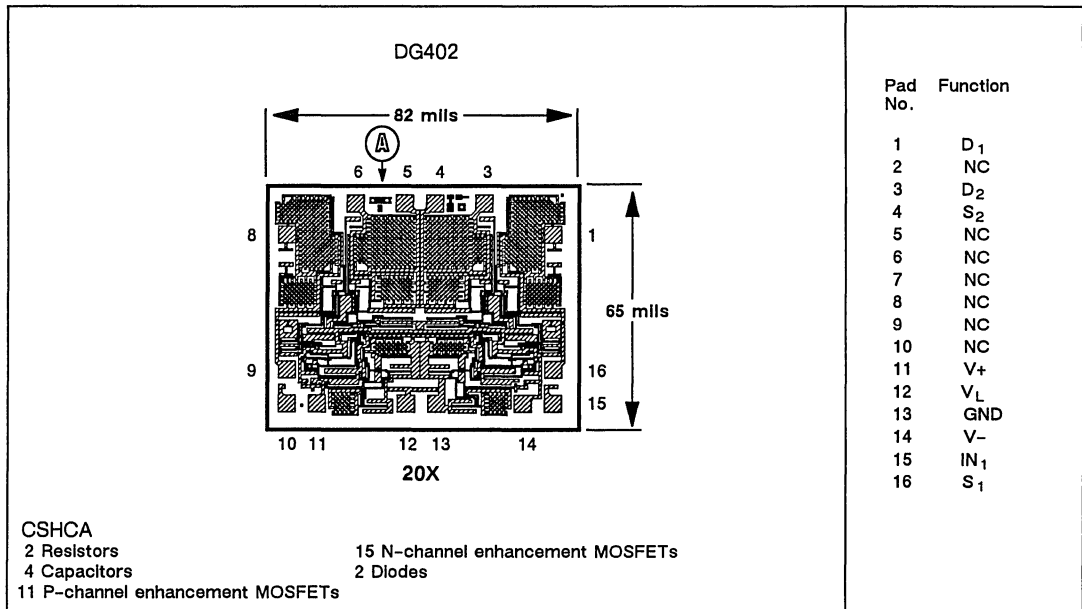
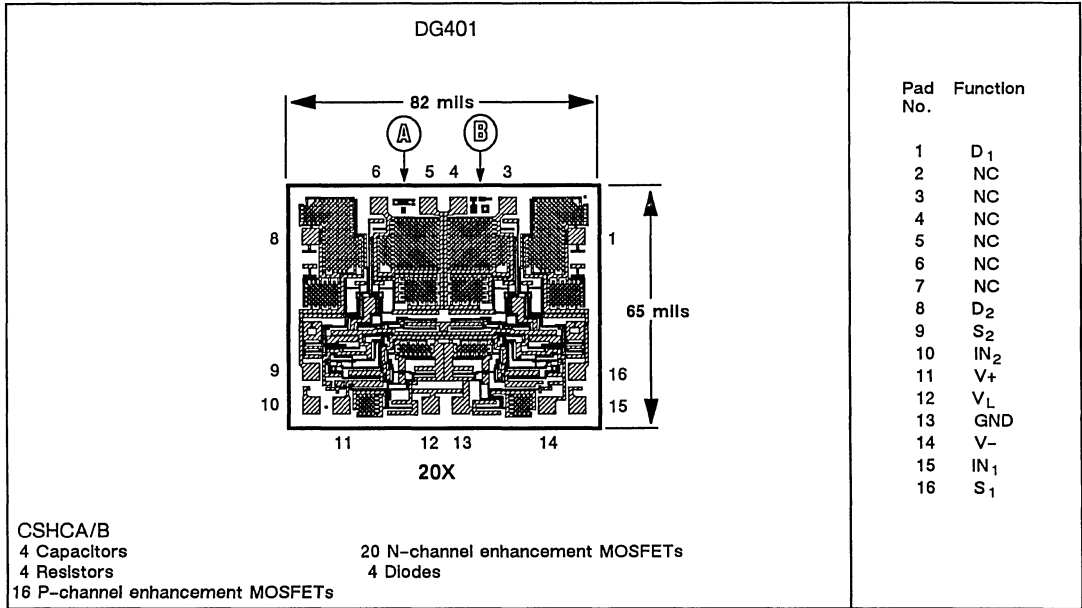
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- V<sub>IN</sub> = Input voltage to perform proper function.
- Crosstalk performance is improved to 110 dB (typ.) with LCC package.

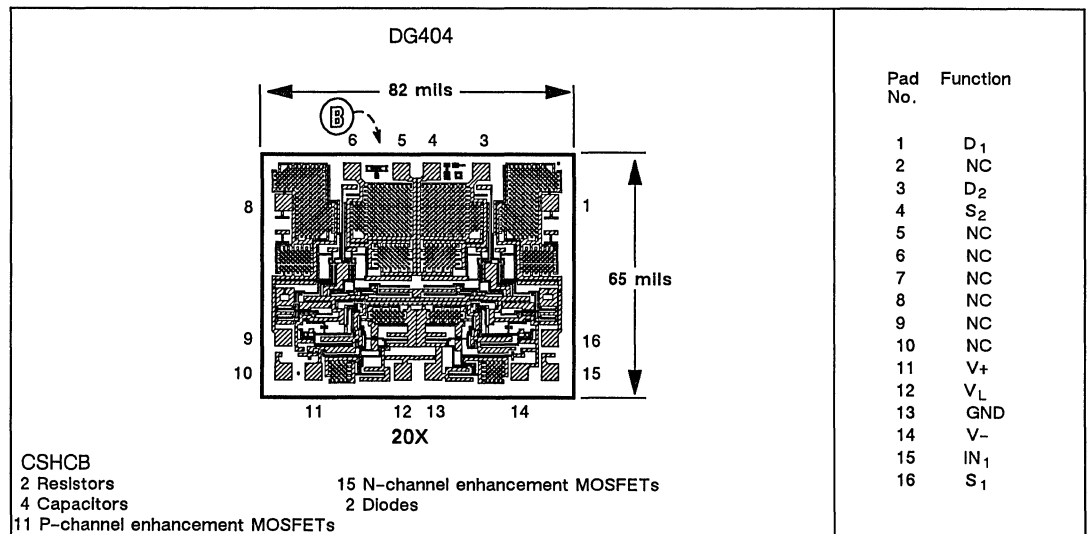
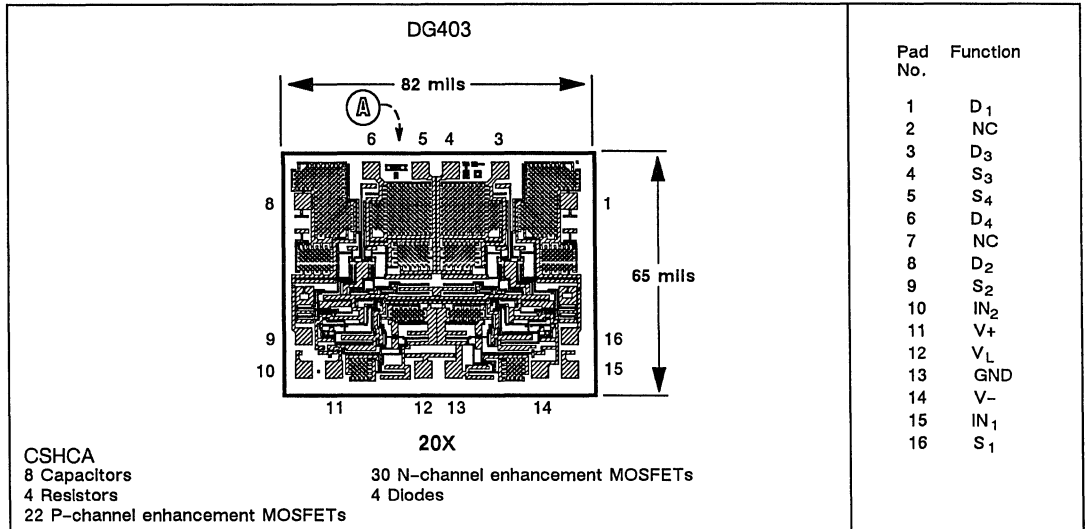
## DIE TOPOGRAPHY



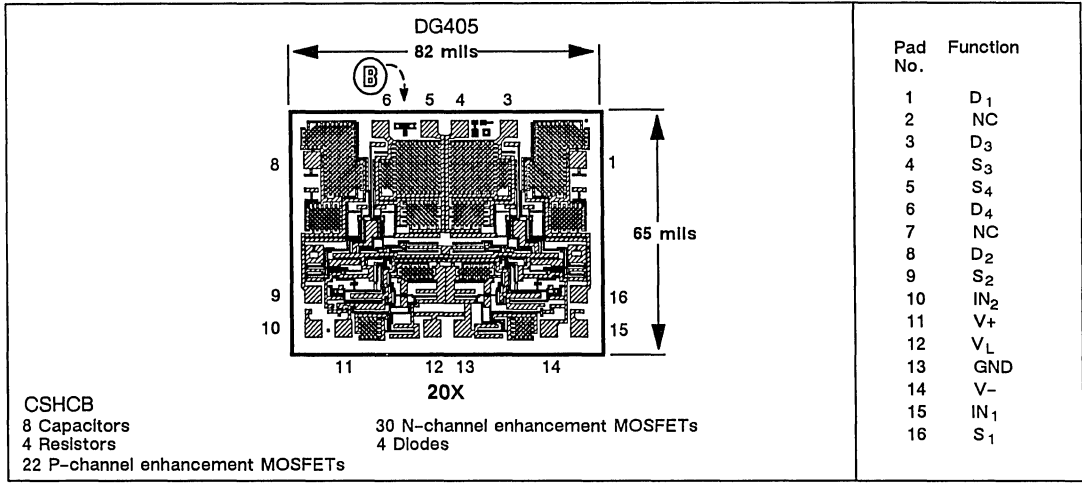


**DIE TOPOGRAPHY (Cont'd)**

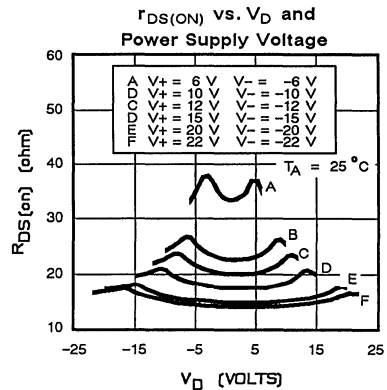
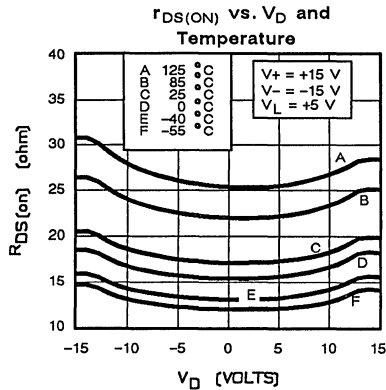
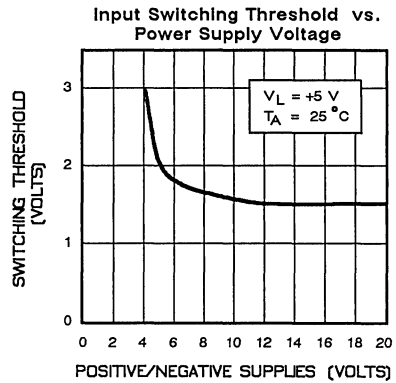
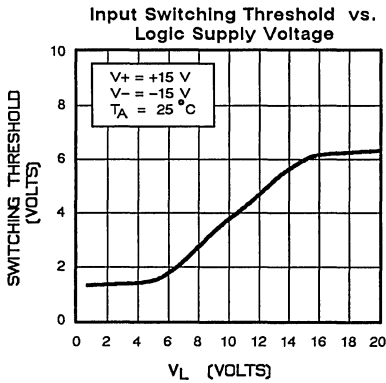




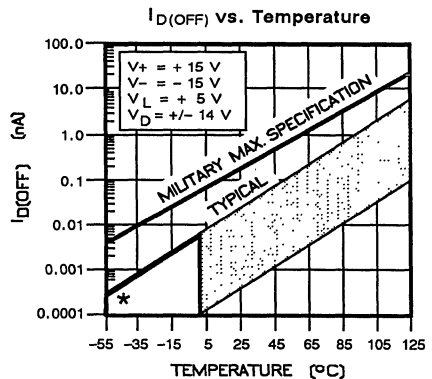
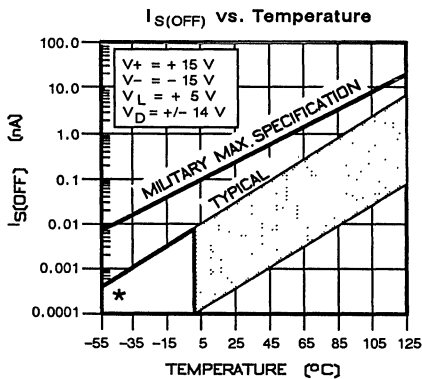
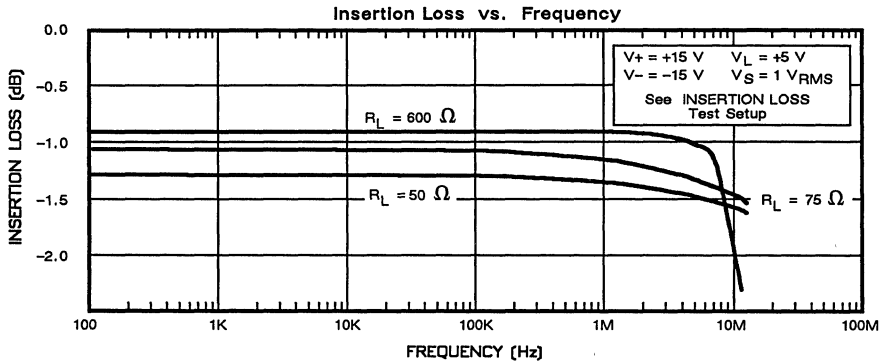
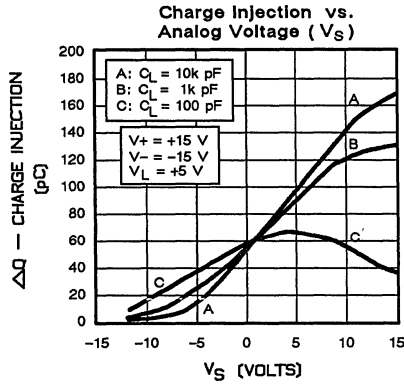
**DIE TOPOGRAPHY (Cont'd)**



**TYPICAL CHARACTERISTICS**

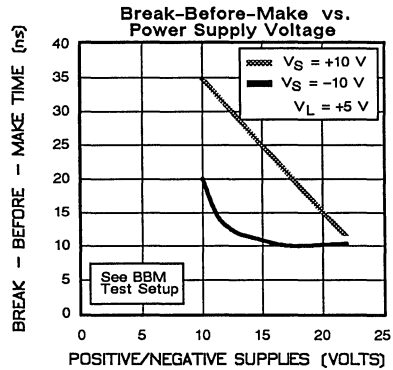
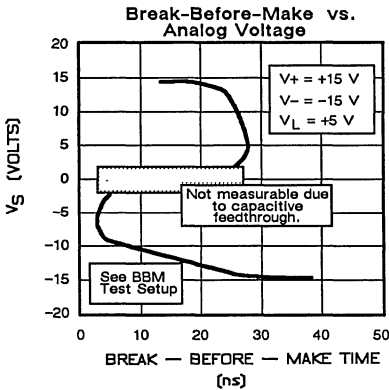
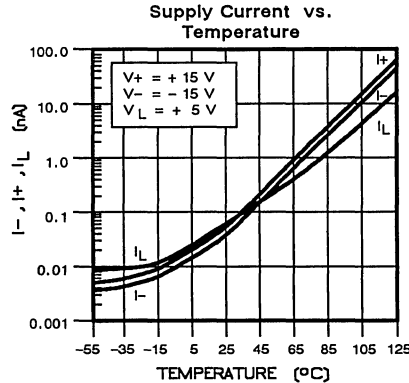
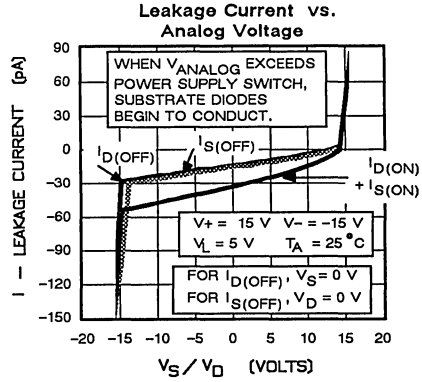
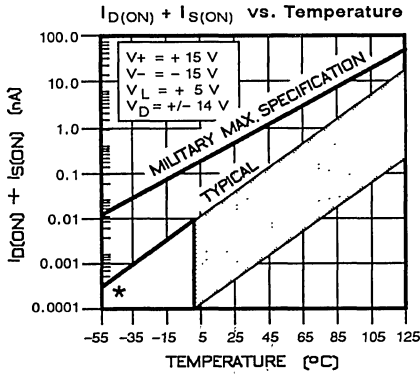


## TYPICAL CHARACTERISTICS (Cont'd)



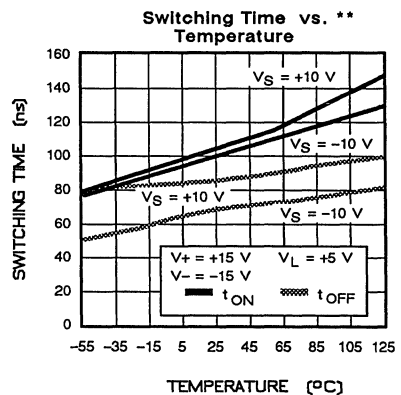
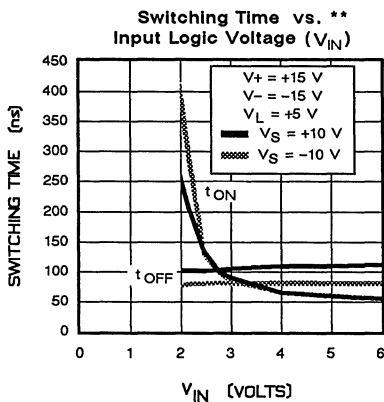
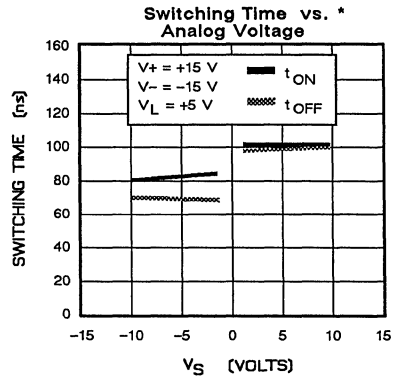
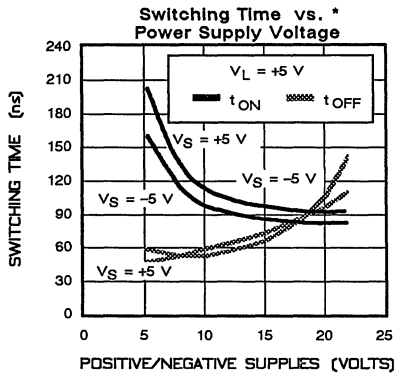
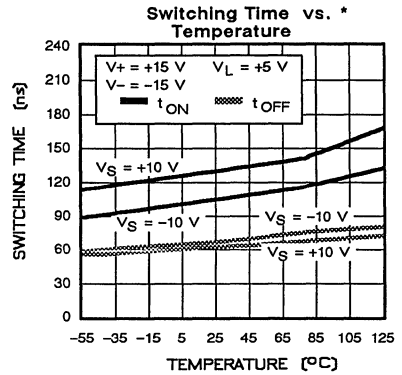
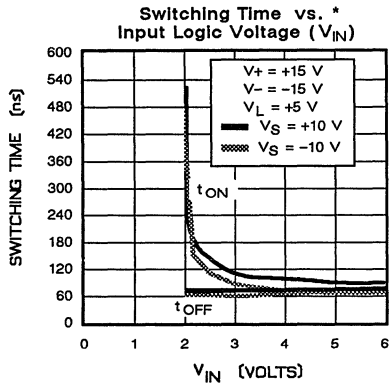
\* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

**TYPICAL CHARACTERISTICS (Cont'd)**



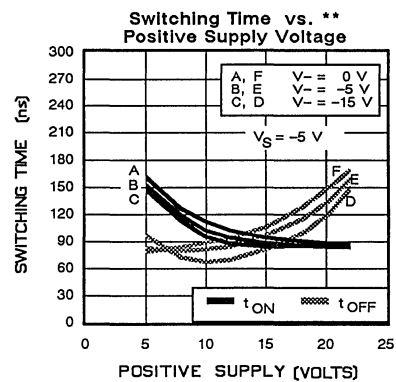
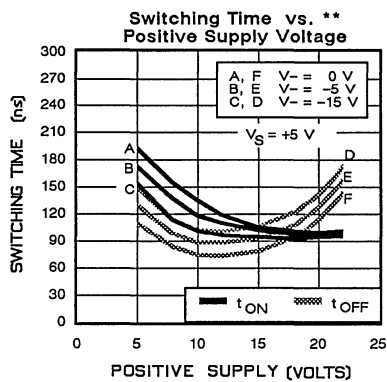
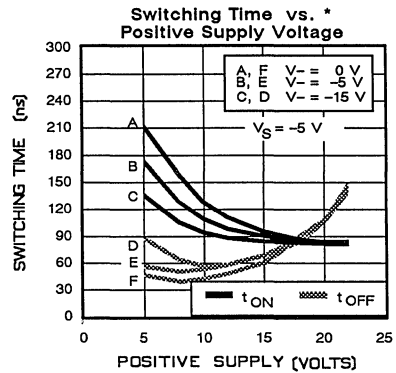
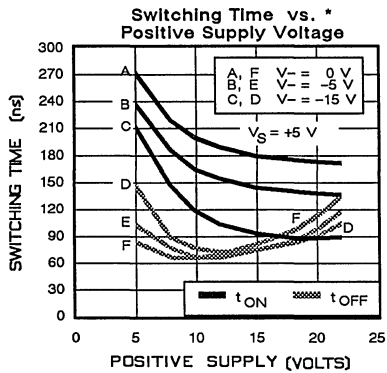
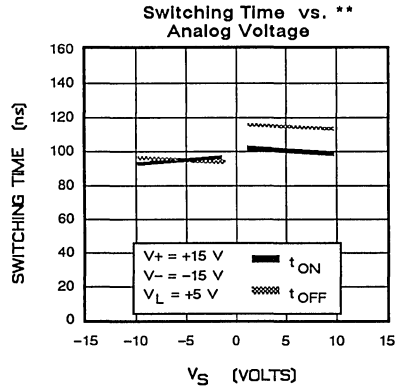
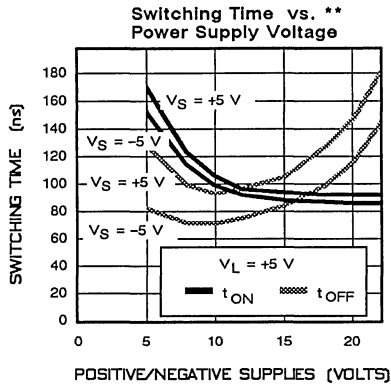
\* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

## TYPICAL CHARACTERISTICS (Cont'd)



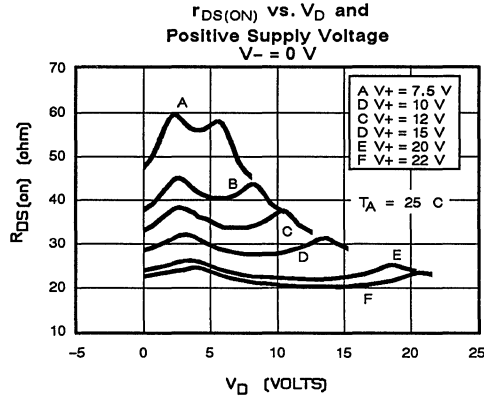
\* REFER TO FIGURE 1A FOR TEST CONDITIONS  
\*\* REFER TO FIGURE 1B FOR TEST CONDITIONS

**TYPICAL CHARACTERISTICS (Cont'd)**



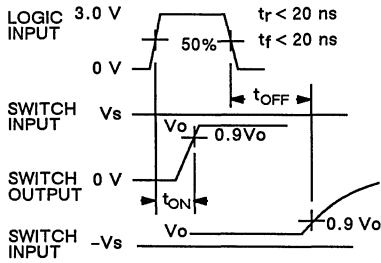
\* REFER TO FIGURE 1A FOR TEST CONDITIONS  
\*\* REFER TO FIGURE 1B FOR TEST CONDITIONS

## TYPICAL CHARACTERISTICS (Cont'd)

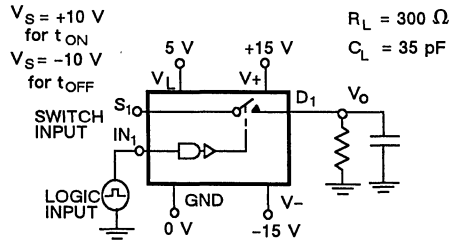


## SWITCHING TIME TEST CIRCUIT

$V_o$  is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic Input waveform is inverted for switches that have the opposite logic sense control



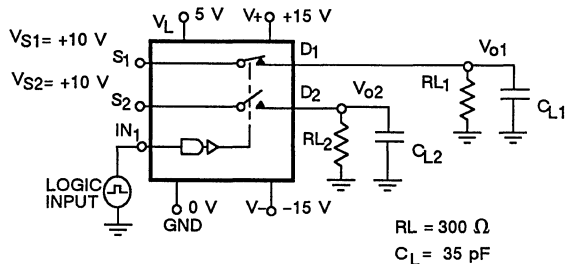
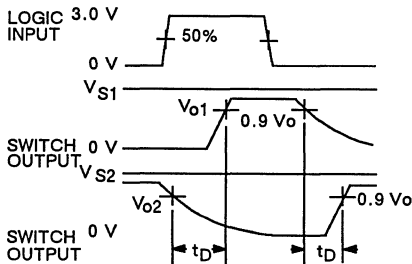
Repeat test for  $IN_2$  and  $S_2$

For load conditions, See Electrical Characteristics  
 $C_L$  (includes fixture and stray capacitance)

$$V_o = V_s \frac{R_L}{R_L + r_{DS(ON)}}$$

Figure 1

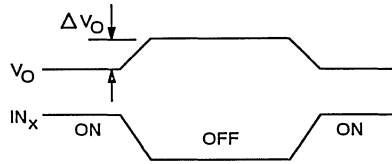
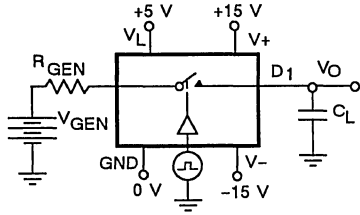
## BREAK-BEFORE-MAKE TEST CIRCUIT



(includes fixture and stray capacitance)

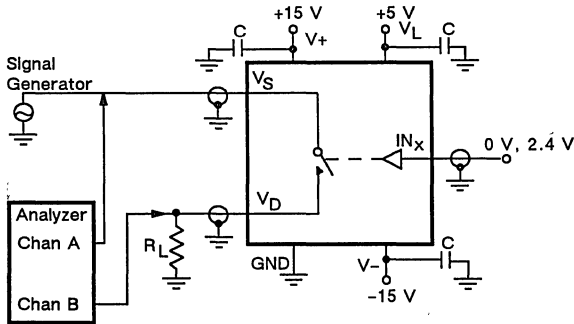


**CHARGE INJECTION TEST CIRCUIT**



$$Q = \Delta V_O C_L$$

**OFF ISOLATION TEST CIRCUIT**

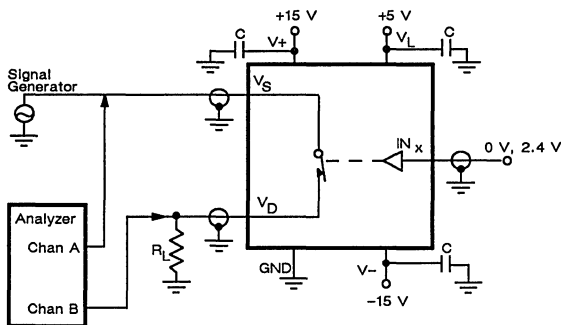


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

$$\text{OFF ISOLATION} = 20 \log \frac{V_D}{V_S}$$

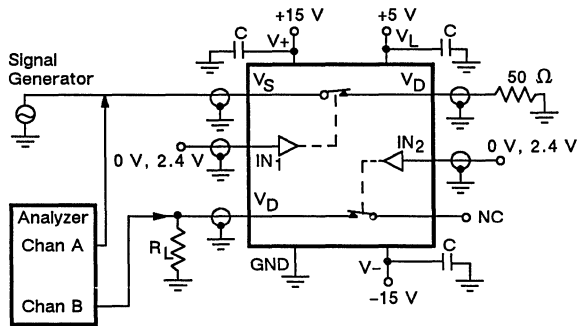
**5**

**INSERTION LOSS TEST CIRCUIT**



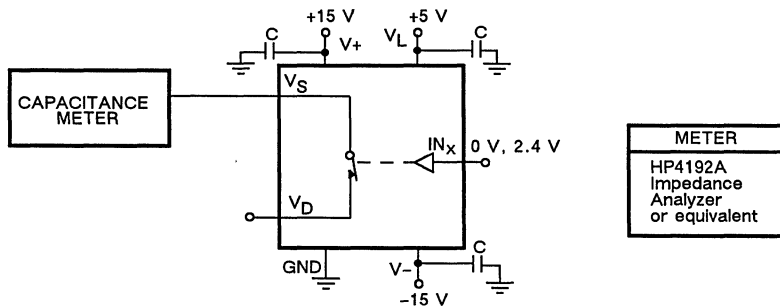
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## CROSSTALK TEST CIRCUIT

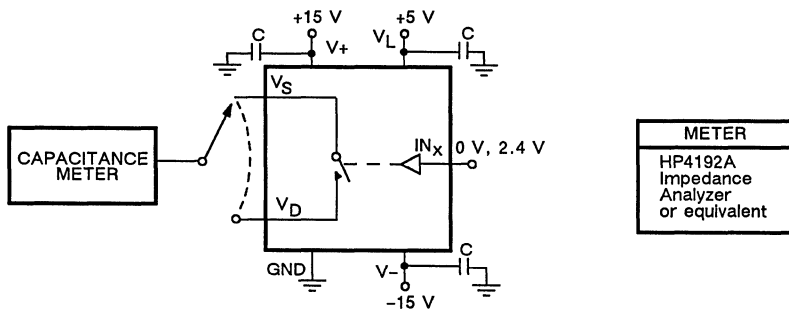


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

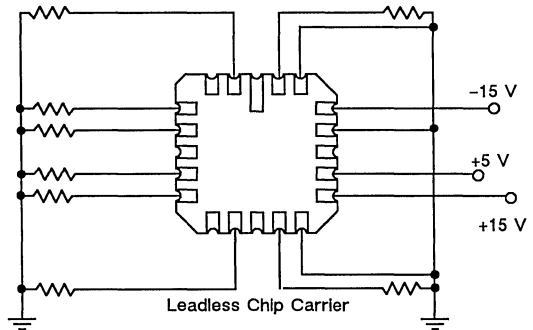
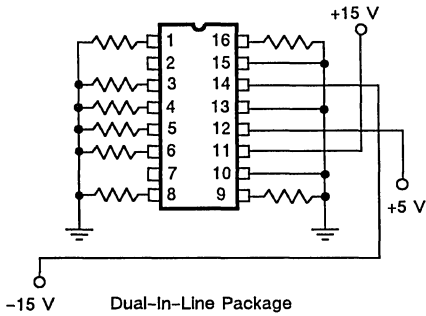
## SOURCE/DRAIN ON CAPACITANCE



## SOURCE/DRAIN OFF CAPACITANCE



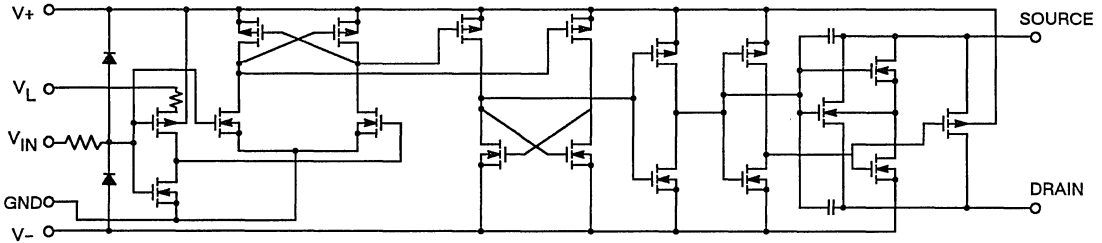
**BURN-IN CIRCUITS**



Note: All Resistors are 10 kΩ unless otherwise specified

Note: SO Package is the same as the DIP

**SCHEMATIC DIAGRAM (Typical Channel)**



**5**

**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
S	An Analog Channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground
VL	Logic Supply Voltage

## APPLICATIONS

### Stereo Source Selectors:

A single logic signal controls the status of all four switches of the device, simplifying stereo source switching. The low on-resistance ( $< 35 \Omega$ ) minimizes total harmonic distortion.

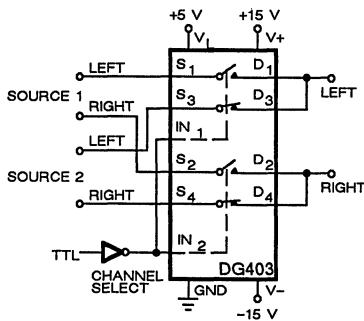
### Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the

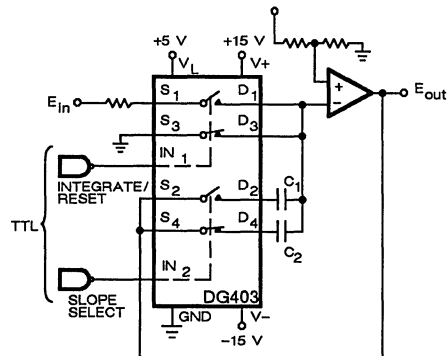
timing capacitor  $C_1$  or  $C_2$ . Another one selects  $E_{in}$  or discharges the capacitor in preparation for the next integration cycle.

### Band-Pass Switched Capacitor Filter:

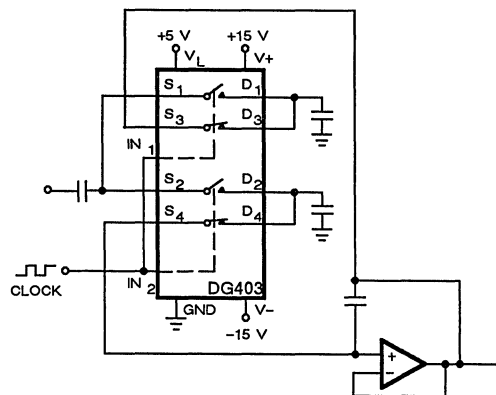
Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.



**Stereo Source Selector**



**Dual Slope Integrator**



**Band-Pass Switched Capacitor Filter**

# 8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

## FEATURES

- Low  $r_{DS(ON)}$  (100  $\Omega$  max)
- Low Charge Injection ( $Q < 10$  pC)
- Fast Transition Time (150 ns max)
- Low Power ( $I_S < 35\mu A$ )
- ESDS Protection  $> \pm 4000$  V

## BENEFITS

- Reduced Switching Errors
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness

## APPLICATIONS

- Data Acquisition Systems
- Audio Signal Routing and Multiplexing / Demultiplexing
- ATE Systems
- Battery Operated Systems
- High Rel Systems

## DESCRIPTION

The DG408 is an 8-channel single-ended analog multiplexer designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address ( $A_0, A_1, A_2$ ). The DG409, is a 4-channel differential analog multiplexer designed to connect 1 of 4 differential inputs to a common dual output as determined by its 2 bit binary address ( $A_0, A_1$ ). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An ON channel conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF for stacking several devices. All control inputs, address ( $A_x$ ) and enable (EN) are TTL compatible over the full specified operating temperature range.

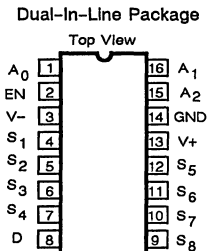
Applications for the DG408/409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts, allowing operation with  $\pm 20$  V supplies. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

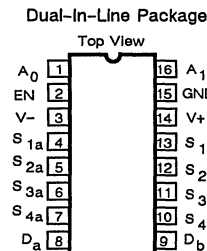
Both DG408 and DG409 are available in dual-in-line ceramic and plastic packages, and are specified for operation over the military, A suffix ( $-55$  to  $125^\circ C$ ) and industrial, D suffix ( $-40$  to  $85^\circ C$ ) temperature ranges.

**5**

## PIN CONFIGURATION

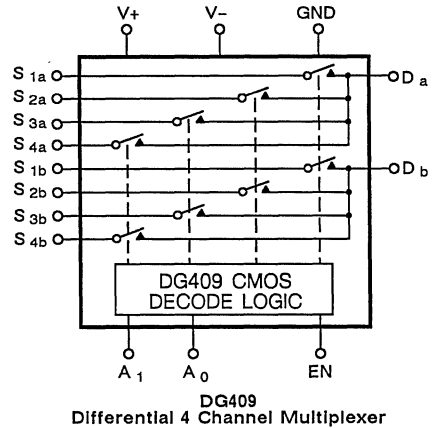
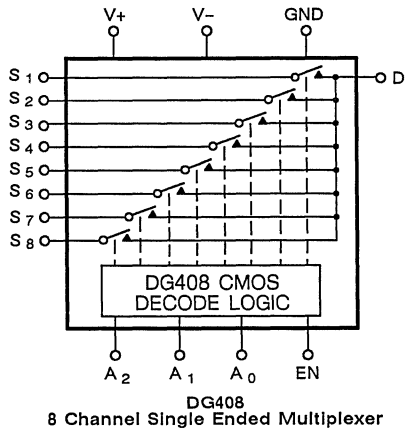


Order Numbers:  
CerDIP: DG408AK  
Plastic: DG408DJ



Order Numbers:  
CerDIP: DG409AK  
Plastic: DG409DJ

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs <sup>g</sup>, V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2 V or  
..... 20 mA, whichever occurs first.

Current (Any Terminal, Except S or D) ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D

(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA

Operating Temperature (A Suffix) ..... -55 to 125°C  
(D Suffix) ..... -40 to 85°C

Storage Temperature (A Suffix) ..... -65 to 150°C  
(D Suffix) ..... -65 to 125°C

Power Dissipation (Package) \*

16-Pin Ceramic DIP\*\* ..... 900 mW

16-Pin Plastic DIP\*\*\* ..... 470 mW

\* All leads soldered or welded to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6.3 mW/°C above 75°C.

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V
Drain-Source <sup>e</sup> ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = ±10 V, V <sub>AL</sub> = 0.8 V I <sub>S</sub> = -200 μA, V <sub>AH</sub> = 2.4 V Sequence Each Switch ON	1 2,3	40		100		100	Ω
Greatest Change In r <sub>DS(ON)</sub> Between Channels <sup>f</sup>	r <sub>DS(ON)</sub> Δ	-10 V < V <sub>S</sub> < 10 V	1			10		10	%
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>EN</sub> = 0 V	V <sub>S</sub> = ±10 V V <sub>D</sub> = ±10 V	1 2,3		0.25		0.25	nA
Drain OFF Leakage Current	DG408		V <sub>D</sub> = ±10 V V <sub>S</sub> = ±10 V	1 2,3		0.50		0.50	
	DG409		V <sub>D</sub> = ±10 V V <sub>S</sub> = ±10 V	1 2,3		0.25		0.25	

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $GND = 0\text{ V}$	LIMITS						UNIT		
			1=25°C		A SUFFIX		D SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SWITCH (Cont'd)</b>											
Drain ON Leakage Current	DG408	$I_{D(ON)}$	$V_S = V_D = \pm 10\text{ V}$	Sequence Each Switch ON $V_{AL} = 0.8\text{ V}$ $V_{AH} = 2.4\text{ V}$	1			0.50		0.50	nA
	DG409				2,3				0.25		
<b>INPUT</b>											
Logic Input Current Input Voltage HIGH	$I_{AH}$	$V_A = 2.4\text{ V}$	1		-10		-10			$\mu\text{A}$	
			2,3				10		10		
Logic Input Current Input Voltage LOW	$I_{AL}$	$V_{EN} = 0, 2.4\text{ V}$ , $V_A = 0\text{ V}$	1		-10	10	-10	10			
<b>DYNAMIC</b>											
Switching Time of Multiplexer	$t_{TRANS}$	See Figure 1	1			150		150		ns	
Break-Before-Make Interval	$t_{OPEN}$	See Figure 3	1		20		20				
Enable Turn ON Time	$t_{ON(EN)}$	See Figure 2	1			150		150			
Enable Turn OFF Time	$t_{OFF(EN)}$		1			150		150			
Charge Injection	Q		1	10						pC	
OFF Isolation		$V_{EN} = 0\text{ V}$ , $R_L = 1\text{ k}\Omega$ $C_L = 15\text{ pF}$ , $V_S = 7\text{ V}_{RMS}$ $f = 500\text{ kHz}$	1	90						dB	
Logic Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$	1	8						pF	
Source OFF Capacitance	$C_{S(OFF)}$	$V_{EN} = 0\text{ V}$ $f = 140\text{ kHz}$	$V_S = 0\text{ V}$		1	5					
Drain OFF Capacitance	$C_{D(OFF)}$		$V_D = 0\text{ V}$		1	40					
					1	20					
<b>SUPPLY</b>											
Positive Supply Current	$I_+$	$V_{EN} = 0\text{ V}$ , $V_A = 0\text{ V}$	1			35		35		$\mu\text{A}$	
Negative Supply Current	$I_-$		1		-35		-35				

5

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

### NOTES:

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Sequence each switch ON.

$$f. \Delta r_{DS(ON)} = \left( \frac{r_{DS(ON) \text{ MAX}} - r_{DS(ON) \text{ MIN}}}{r_{DS(ON) \text{ AVE}}} \right)$$

- g. Maximum voltages and currents can not necessarily be applied simultaneously.

## TRUTH TABLES

DG408

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG409

A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = V<sub>AL</sub> < 0.8 V, Logic "1" = V<sub>AH</sub> > 2.4 V

## SWITCHING TIME TEST CIRCUIT

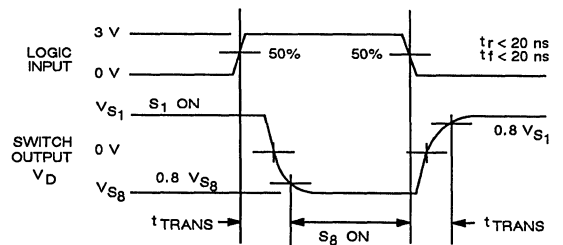
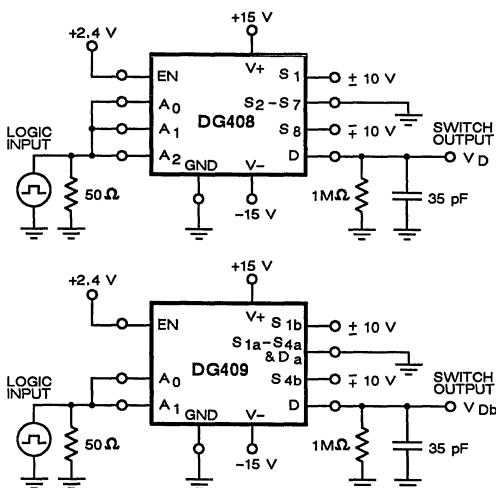
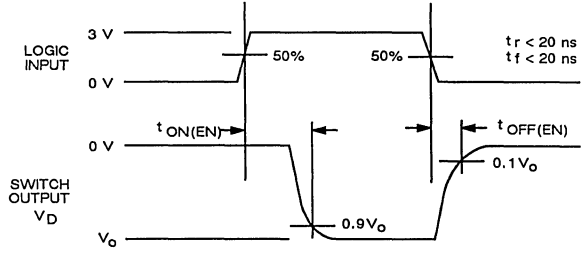
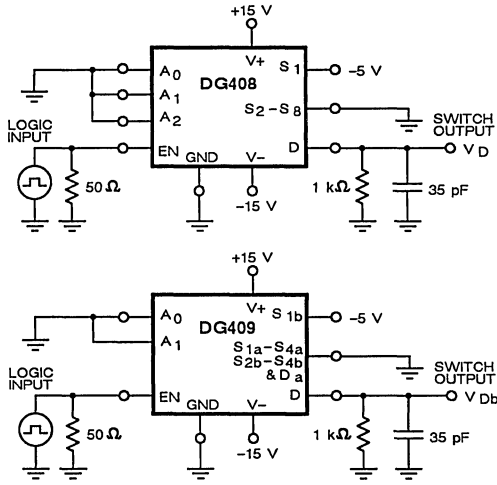


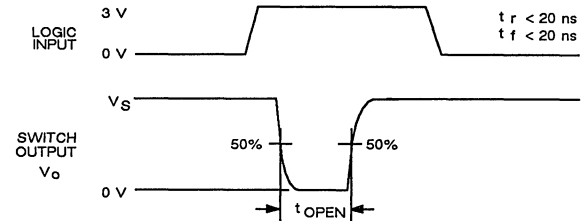
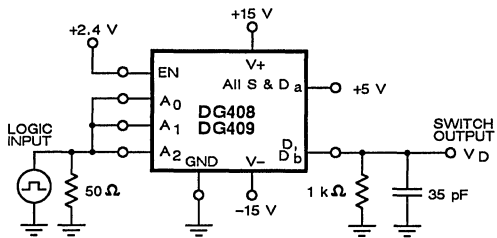
Figure 1



**SWITCHING TIME TEST CIRCUIT (Cont'd)**



**Figure 2**



**Figure 3**

## Precision Monolithic Quad SPST CMOS Analog Switches

### FEATURES

- $\pm 15$  Volt Input Range
- ON Resistance  $< 35 \Omega$
- Fast Switching Action  
 $t_{ON} < 175 \text{ ns}$   
 $t_{OFF} < 145 \text{ ns}$
- Ultra Low Power Requirements  
 $(P_D < 35 \mu\text{W})$
- TTL, CMOS Compatible
- ESDS Protection  $> \pm 4000 \text{ V}$

### BENEFITS

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

### APPLICATIONS

- High Performance Audio and Video Switching
- Precision Automatic Test Equipment
- Precision Data Acquisition
- Sample and Hold Circuits
- Communication Systems
- Battery Operated Systems

### DESCRIPTION

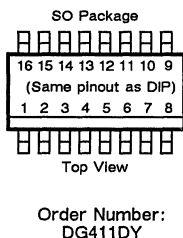
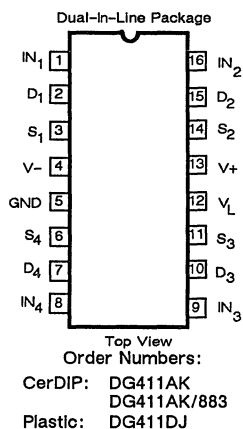
The DG411 series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog, audio and video signals. Combining low power ( $< 35 \mu\text{W}$ ) with high speed ( $t_{ON} < 175 \text{ ns}$ ), the DG411 family is ideally suited for portable and battery powered industrial and military applications.

To achieve high-voltage ratings and superior switching performance, the DG411 series was built on Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

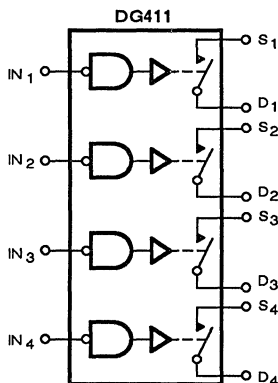
Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full  $\pm 15 \text{ V}$  analog range, rivaling JFET performance without the inherent dynamic range limitation.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams. Package options include the 16-pin CerDIP, plastic and small outline (SO) packages. Performance grades include both the industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ), and the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) temperature ranges.

### PIN CONFIGURATIONS



### FUNCTIONAL BLOCK DIAGRAM



DG411  
Four SPST Switches per Package  
Truth Table\*

LOGIC	SWITCH
0	ON
1	OFF

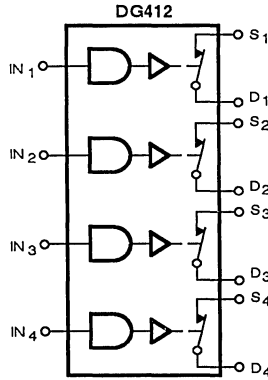
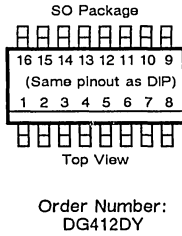
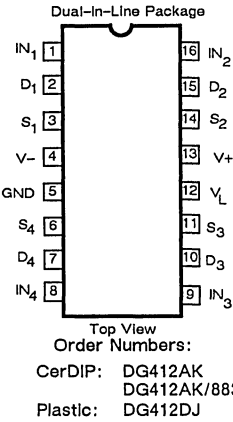
Logic "0"  $\leq 0.8 \text{ V}$

Logic "1"  $\geq 2.4 \text{ V}$

\*Switches shown for logic "1" input.

**PIN CONFIGURATIONS**

**FUNCTIONAL BLOCK DIAGRAM**



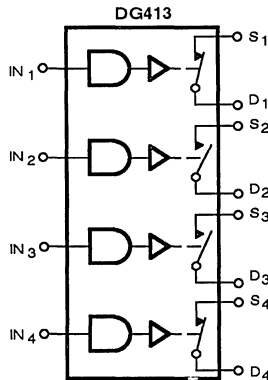
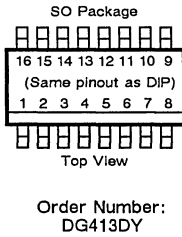
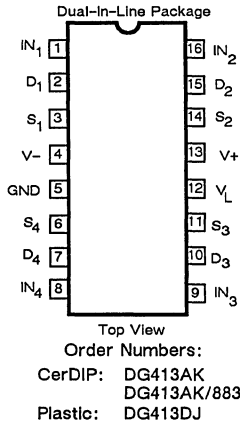
**DG412**  
Four SPST Switches per Package

Truth Table\*

LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq$  0.8 V  
Logic "1"  $\geq$  2.4 V

\*Switches shown for logic "1" input.



**DG413**  
Four SPST Switches per Package

Truth Table\*

LOGIC	SWITCH 1, 4	SWITCH 2, 3
0	OFF	ON
1	ON	OFF

Logic "0"  $\leq$  0.8 V  
Logic "1"  $\geq$  2.4 V

\*Switches shown for logic "1" input.

**5**

**ABSOLUTE MAXIMUM RATINGS**

- V+ to V- ..... 44 V
- GND to V- ..... 25 V
- VL ..... (GND -0.3 V) to 44 V
- Digital Inputs, VS, VD<sup>1</sup> ..... (V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
- Continuous Current (Any Terminal) ..... 30 mA
- Current, S or D (Pulsed 1 ms, 10% Duty Cycle) .. 100 mA
- Storage Temperature (A Suffix) ..... -65 to 150°C  
(D Suffix) ..... -65 to 125°C
- Operating Temperature (A Suffix) ..... -55 to 125°C  
(D Suffix) ..... -40 to 85°C

**Power Dissipation (Package)\***

- 16-Pin Plastic DIP\*\* ..... 470 mW
- 16-Pin CerDIP\*\*\* ..... 900 mW
- 16-Pin SO\*\*\*\* ..... 600 mW

- \* All leads welded or soldered to PC board.
- \*\* Derate 6 mW /°C above 25°C.
- \*\*\* Derate 12 mW /°C above 75°C.
- \*\*\*\* Derate 7.6 mW/°C above 75°C.

<sup>1</sup> Signals on Sx, Dx, or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ , $GND = 0\text{ V}$ $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$			LIMITS					
					1=25°C		A SUFFIX		D SUFFIX	
					TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$					-15	15	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -10\text{ mA}$ , $V_D = \pm 8.5\text{ V}$ $V_+ = 13.5\text{ V}$ , $V_- = -13.5\text{ V}$	1,3 2	25			35 45		35 45	$\Omega$
Switch OFF Leakage Current	$I_{S(OFF)}$	$V_+ = 16.5\text{ V}$ $V_- = -16.5\text{ V}$	1,3 2	-0.1	-0.25 -20	0.25 20	-0.25 -20	0.25 20	nA	
	$I_{D(OFF)}$									$V_D = -15.5\text{ V}$ $V_S = 15.5\text{ V}$
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$									$V_S = V_D = \pm 15.5\text{ V}$
<b>INPUT</b>										
Input Current with $V_{IN}$ LOW	$I_{IL}$	$V_{IN}$ Under Test = 0.8 V All Other = 2.4 V	1,2,3	.005	-0.5	0.5	-0.5	0.5	$\mu\text{A}$	
Input Current with $V_{IN}$ HIGH	$I_{IH}$	$V_{IN}$ Under Test = 2.4 V All Other = 0.8 V	1,2,3	.005	-0.5	0.5	-0.5	0.5		
<b>DYNAMIC</b>										
Turn-ON Time	$t_{ON}$	$R_L = 300\Omega$ , $C_L = 35\text{ pF}$ See Switching Time Test Circuit $V_S = \pm 10\text{ V}$	1,3	110		175		175	ns	
Turn-OFF Time	$t_{OFF}$		1,3	100		145		145		
Break-Before-Make Time Delay	$t_D$	DG413 Only $R_L = 300\Omega$ , $C_L = 35\text{ pF}$	1	25	10		10			
Charge Injection	Q	$V_{gen} = 0\text{ V}$ , $R_{gen} = 0\Omega$ $C_L = 10\text{ nF}$	1	5					pC	
OFF Isolation <sup>c</sup>		$R_L = 50\Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	1	68					dB	
Crosstalk <sup>c</sup> (Channel-to-Channel)		Any Other Channel Switches $R_L = 50\Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	1	85						
Source OFF Capacitance <sup>c</sup>	$C_{S(OFF)}$	$f = 1\text{ MHz}$	1	9					pF	
Drain OFF Capacitance <sup>c</sup>	$C_{D(OFF)}$		1	9						
Drain and Source ON <sup>c</sup> Capacitance	$C_{D(ON)} + C_{S(ON)}$		1	18						

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
SUPPLY									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0 or 5 V	1	.0001		1		1	μA
Negative Supply Current	I <sub>-</sub>		2			5		5	
Logic Supply Current	I <sub>L</sub>		1						
Ground Current	I <sub>GND</sub>		2						
			1						
			2						

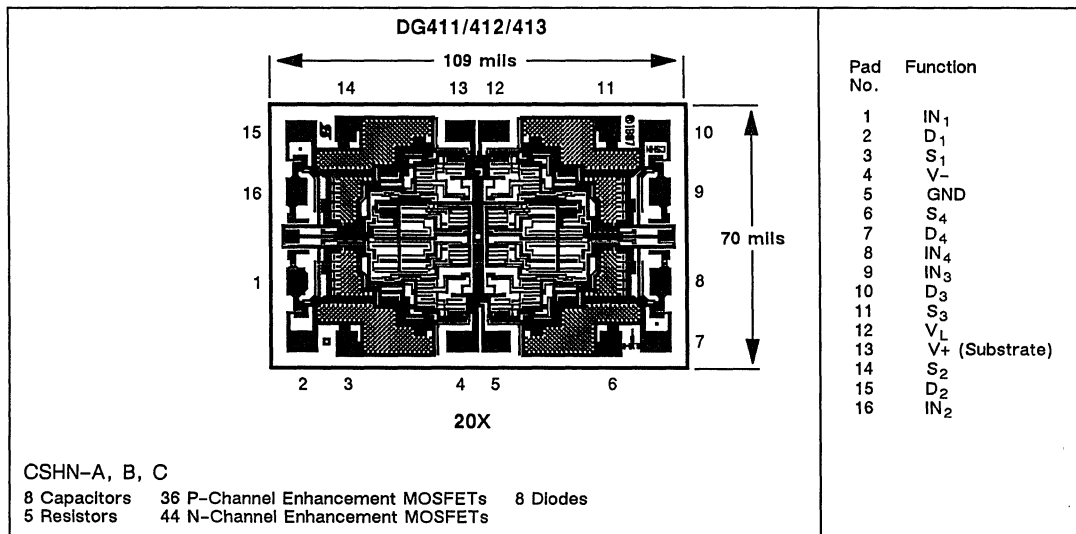
ELECTRICAL CHARACTERISTICS <sup>a</sup> (UNIPOLAR SUPPLY)									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V, V <sub>-</sub> = 0 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
SWITCH									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>				0	12	0	12	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 3.8 V V <sub>+</sub> = 10.8 V	1,3	40		80		80	Ω
			2			100		100	
DYNAMIC									
Turn-ON Time	t <sub>ON</sub>	R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35 pF	1,3	175		250		250	ns
Turn-OFF Time	t <sub>OFF</sub>	See Switching Time Test Circuit V <sub>S</sub> = 8 V	1,3	95		125		125	
Break-Before-Make Time Delay	t <sub>D</sub>	DG413 Only R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35 pF	1	25	10		10		
Charge Injection	Q	V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0Ω C <sub>L</sub> = 10 nF	1	25					pC
SUPPLY									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 or 5 V	V <sub>+</sub> = 13.2 V	1	.0001		1		1
Negative Supply Current	I <sub>-</sub>		2				5		5
Logic Supply Current	I <sub>L</sub>		V <sub>L</sub> = 5.25 V	1					
Ground Current	I <sub>GND</sub>			2					
				1					
				2					

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

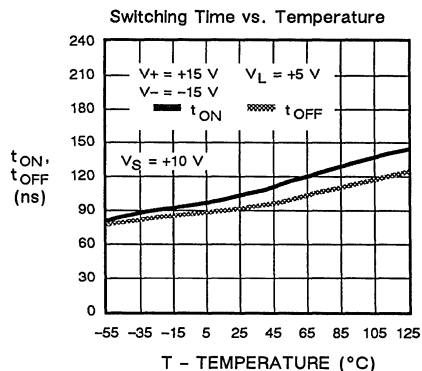
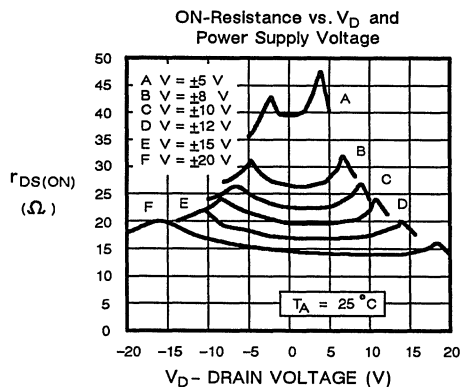
### NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- $V_{IN}$  = Input voltage to perform proper function.

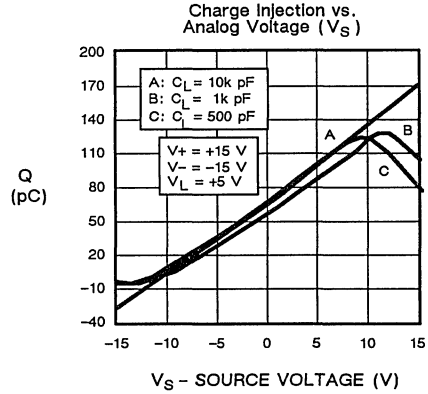
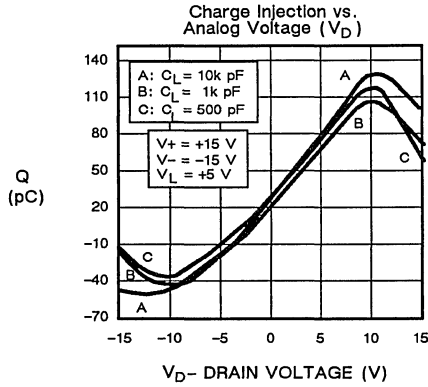
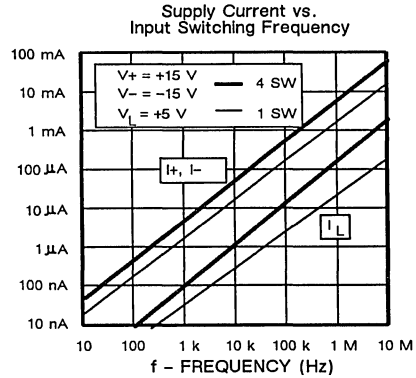
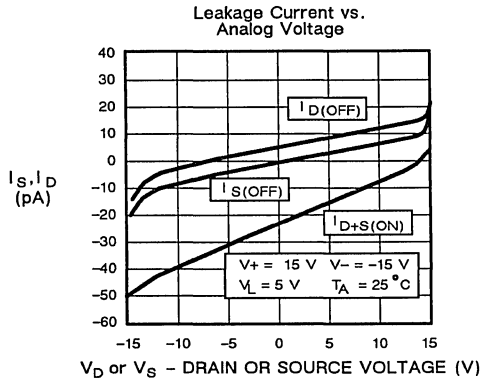
## DIE TOPOGRAPHY



## TYPICAL CHARACTERISTICS

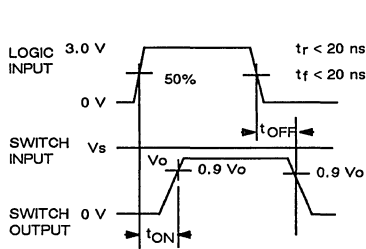


**TYPICAL CHARACTERISTICS (Cont'd)**

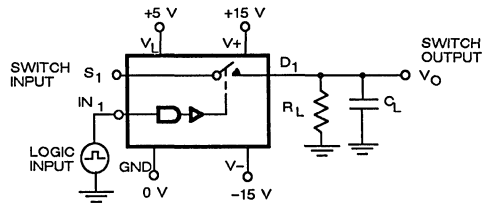


**SWITCHING TIME TEST CIRCUIT**

$V_O$  is the steady state output with the switch ON. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense

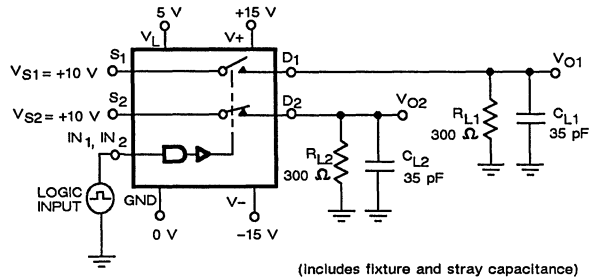
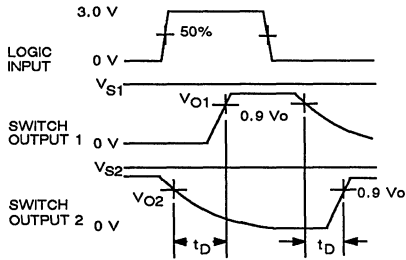


Repeat test for all IN and S.

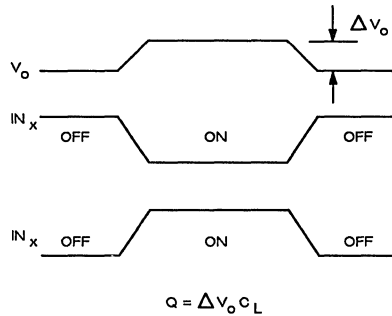
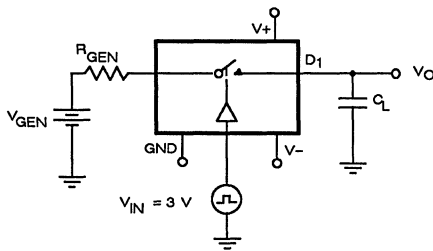
For load conditions, See Electrical Characteristics  $C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

## BREAK-BEFORE-MAKE TIME TEST CIRCUIT

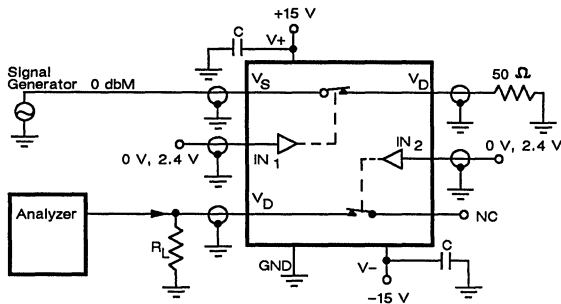


## CHARGE INJECTION TEST CIRCUIT



IN<sub>x</sub> dependent on switch configuration  
Input polarity determined by sense of switch

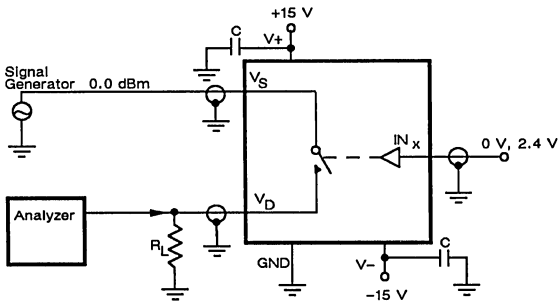
## CROSSTALK TEST CIRCUIT



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

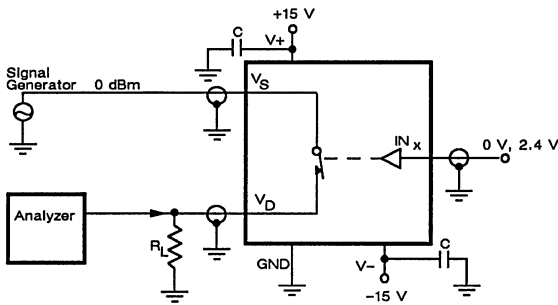


## OFF ISOLATION TEST CIRCUIT



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

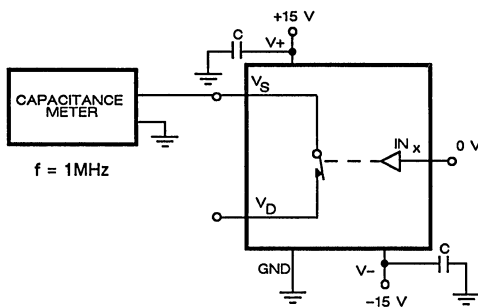
## INSERTION LOSS TEST CIRCUIT



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

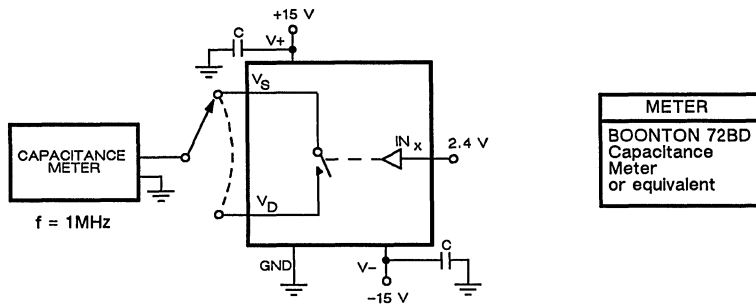
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## SOURCE/DRAIN ON CAPACITANCE

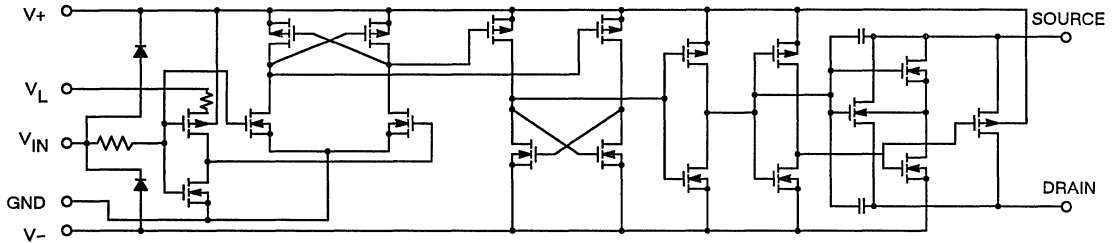


METER
BOONTON 72BD Capacitance Meter or equivalent

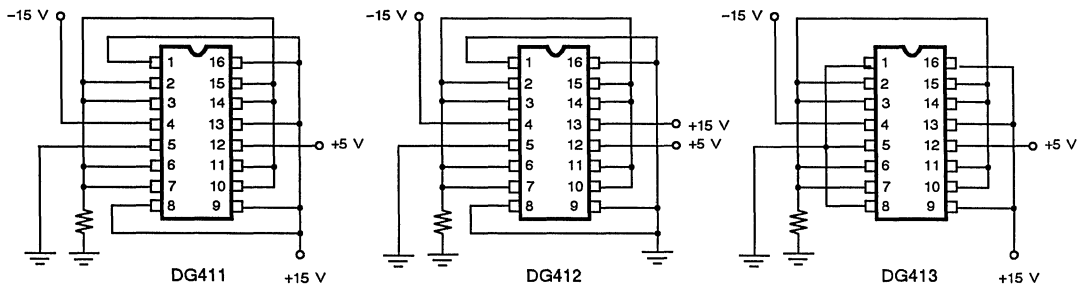
## SOURCE/DRAIN OFF CAPACITANCE



## SCHEMATIC DIAGRAM (Typical Channel)



## BURN-IN CIRCUITS



Note: All resistors are 10 kΩ unless otherwise specified.

## PIN DESCRIPTION

SYMBOL	DESCRIPTION
S	Analog Channel Input or Output
D	Analog Channel Output or Input
IN	Logic Control input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground
V <sub>L</sub>	Logic Supply Voltage

## APPLICATIONS

### Single Supply Operation:

The DG411/412/413 are characterized and tested for single supply operation at 12 volts. Although these devices can be operated with single supplies from 7.5 up to 22 V, 12 volts was selected as the test voltage because a majority of the applications use 12 volts. To function properly 12 volts is tied to pin 13 and 0 volts is tied to pin 4. Note: Pin 12 still requires 5 volts for proper TTL compatible switching.

### Fast Sample and Hold:

The bulk of errors in sample and hold circuits attributed to analog switches come from two parameters – leakage currents and charge injection. Both parameters cause completely different errors to take place. Leakage currents discharge the holding capacitor ( $C_H$ ) with time causing droop, while charge injection causes a dc offset to occur. The DG411/412/413's very low leakage current (250 pA) and charge injection (5 pC) specifications enhance sample and hold (Figure 1) accuracy.

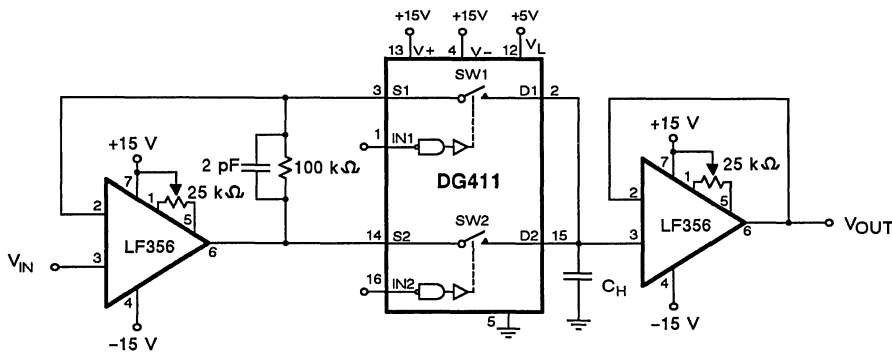


Figure 1. Fast, Accurate Sample and Hold

## APPLICATIONS (Cont'd)

### Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 2, where the inputs to

the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor thus preventing offsets from occurring at the output.

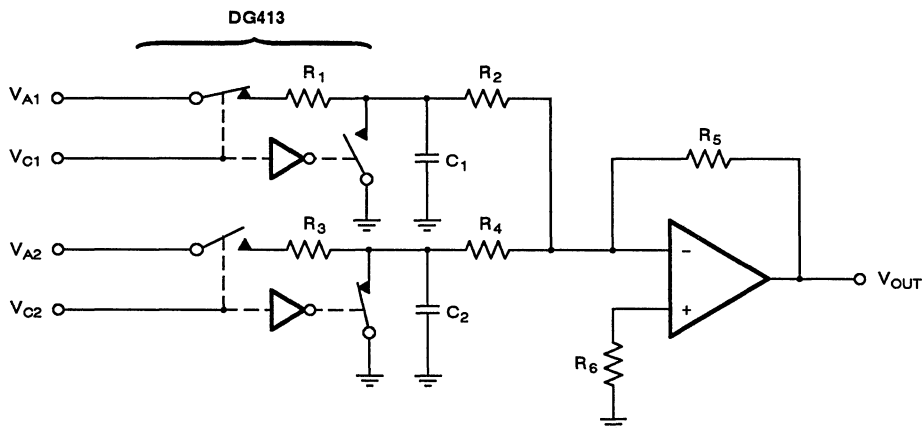


Figure 2. Summing Amplifier

# DG417/418/419

## Precision MiniDIP

### CMOS Analog Switches

#### FEATURES

- $\pm 15$  Volt Input Range
- ON Resistance < 35  $\Omega$
- Fast Switching Action  
 $t_{ON} < 175$  ns  
 $t_{OFF} < 145$  ns
- Ultra Low Power Requirements  
 $(P_D \leq 35 \mu W)$
- TTL and CMOS Compatible
- MiniDIP and SO Packaging
- ESDS Protection >  $\pm 4000$  V

#### BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing
- Reduced Board Space
- Improved Reliability

#### APPLICATIONS

- Precision Test Equipment
- Precision Instrumentation
- Battery Operated Systems
- Sample and Hold Circuits

#### DESCRIPTION

The DG417, DG418 and DG419 monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power (< 35  $\mu W$ ), low leakages, high speed, low ON resistance and small physical size, the DG417 series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

To achieve high voltage ratings and superior switching performance, the DG417 series is built on Siliconix's high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419, which is an SPDT configuration. An epitaxial layer

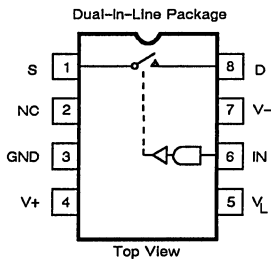
prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full  $\pm 15$  V analog range, rivaling JFET performance without the inherent dynamic range and supply voltage limitations.

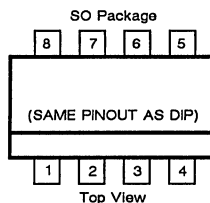
The three devices are differentiated by their switch action as shown in the functional block diagrams. Package options include the 8-pin plastic and ceramic DIP, and the small outline. Performance grades include both the industrial, D suffix (-40 to 85°C) and the military, A suffix (-55 to 125°C) temperature ranges.

**5**

#### PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM



Order Numbers:  
CerDIP: DG417AK, DG417AK/883  
Plastic: DG417DJ



Order Number:  
DG417DY

#### DG417

One SPST Switch per Package

Truth Table\*

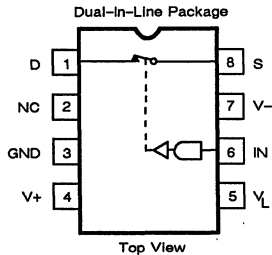
LOGIC	SWITCH
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V

Logic "1"  $\geq 2.4$  V

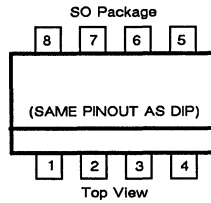
\* Switch Shown for Logic "1" Input

## PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM (Cont'd)



Top View

Order Numbers:  
CerDIP: DG418AK, DG418AK/883  
Plastic: DG418DJ



Top View

Order Number:  
DG418DY

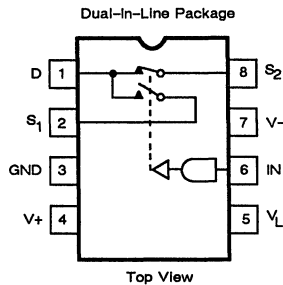
### DG418

One SPST Switch per Package

Truth Table\*

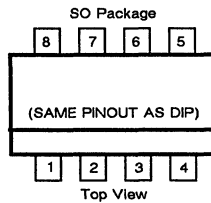
LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.4 V



Top View

Order Numbers:  
CerDIP: DG419AK, DG419AK/883  
Plastic: DG419DJ



Top View

Order Number:  
DG419DY

### DG419

One SPDT Switch per Package

Truth Table\*

LOGIC	SWITCH 1	SWITCH 2
0	ON	OFF
1	OFF	ON

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.4 V

\* Switches Shown for Logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

V<sub>L</sub> ..... (GND -0.3 V) to 44 V

Digital Inputs V<sub>S</sub>, V<sub>D</sub><sup>1</sup> ..... (V-) -2 V to (V+) + 2 V  
..... or 30 mA, whichever occurs first

Current, (Any Terminal) Continuous ..... 30 mA

Current (S or D) Pulsed 1 ms, 10% duty cycle ... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C  
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package) \*

8-Pin Plastic DIP\*\* ..... 400 mW

8-Pin CerDIP\*\*\* ..... 600 mW

8-Pin SO\*\*\*\* ..... 400 mW

\* All leads welded or soldered to PC board.

\*\* Derate 6 mW/°C above 75°C.

\*\*\* Derate 12 mW/°C above 75°C.

\*\*\*\* Derate 6.5 mW/°C above 75°C.

<sup>1</sup> Signals on S, D, or IN exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>					-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±12.5 V V <sub>+</sub> = 13.5 V, V <sub>-</sub> = -13.5 V	1 2,3	20			35 45		35 45	Ω
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>D</sub> = -15.5 V, V <sub>S</sub> = 15.5 V V <sub>D</sub> = 15.5 V, V <sub>S</sub> = -15.5 V	1 2,3	-0.1	-0.25 -20	0.25 20	-0.25 -20	0.25 20	nA	
	I <sub>D(OFF)</sub>		1 2,3	-0.1	-0.25 -20	0.25 20	-0.25 -20	0.25 20		
			DG419	1 2,3	-0.1	-0.75 -60	0.75 60	-0.75 -60		0.75 60
Channel ON Leakage Current	I <sub>D(ON)</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ±15.5 V	1 2,3	-0.4	-0.4 -40	0.4 40	-0.4 -40	0.4 40		
			DG419	1 2,3	-0.4	-0.75 -60	0.75 60	-0.75 -60	0.75 60	
<b>INPUT</b>										
Input Current with V <sub>IN</sub> Low	I <sub>IL</sub>	V <sub>IN</sub> = 0.8 V	1,2,3	.005	-0.5	0.5	-0.5	0.5	μA	
Input Current with V <sub>IN</sub> High	I <sub>IH</sub>	V <sub>IN</sub> = 2.4 V	1,2,3	.005	-0.5	0.5	-0.5	0.5		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	DG417, DG418 ONLY R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = ±10 V	1 2,3	100		175 250		175 250	ns	
Turn-OFF Time	t <sub>OFF</sub>	See Switching Time Test Circuit	1 2,3	60		145 210		145 210		
Transition Time	t <sub>trans</sub>	DG419 ONLY R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S1</sub> = ±10 V, V <sub>S2</sub> = ∓10 V	1 2,3			175 250		175 250		
Break-before-Make Time Delay	t <sub>D</sub>	DG419 ONLY R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S1</sub> = V <sub>S2</sub> = ±10 V	1	13	5		5			
Charge Injection	Q	C <sub>L</sub> = 10 nF V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	1	60					pC	
Source OFF Capacitance <sup>d</sup>	C <sub>S(OFF)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	1	8					pF	
Drain OFF Capacitance <sup>d</sup>	C <sub>D(OFF)</sub>		1	8						

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT	
			1=25°C		A SUFFIX		D SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC (Cont'd)</b>										
Channel ON Capacitance <sup>d</sup>	DG417 DG418	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	f = 1 MHz, V <sub>S</sub> = 0 V	1	30					pF
	DG419			1	35					
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0.0 or 5.0 V	1	.0001		1		1	μA	
Negative Supply Current	I <sub>-</sub>		2,3			5		5		
Logic Supply Current	I <sub>L</sub>		1	.0001		1		1		
Ground Current	I <sub>GND</sub>		2,3			5		5		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = input voltage to perform proper function.

## DIE TOPOGRAPHY

**DG417**

20X

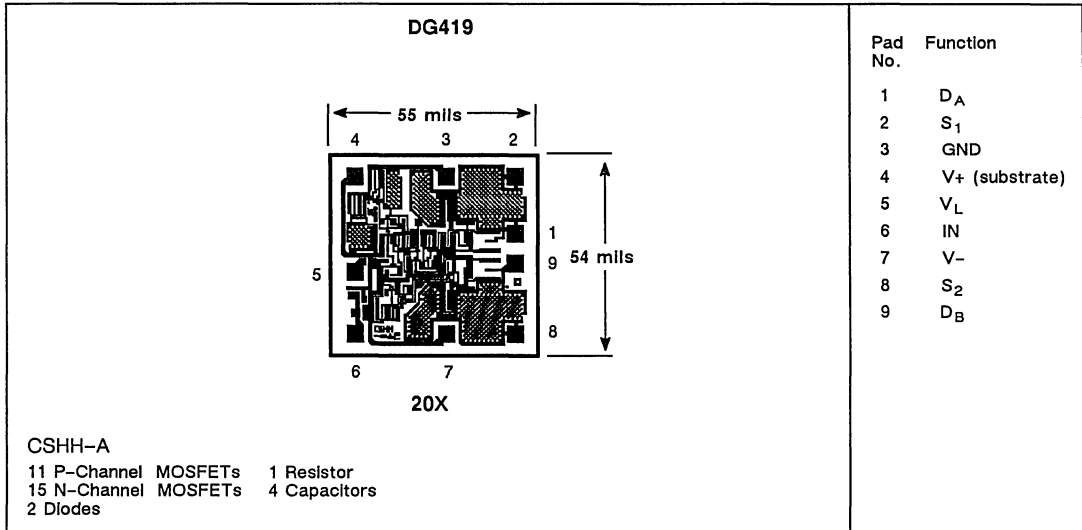
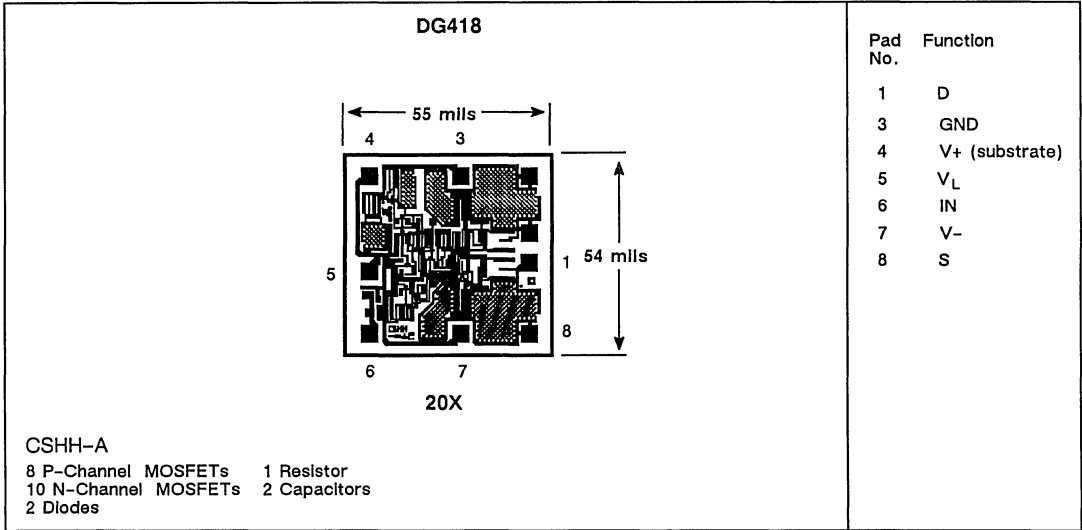
Pad No.	Function
1	D
2	S
3	GND
4	V <sub>+</sub> (substrate)
5	V <sub>L</sub>
6	IN
7	V <sub>-</sub>

CSHH-A

8 P-Channel MOSFETs	1 Resistor
10 N-Channel MOSFETs	2 Capacitors
2 Diodes	



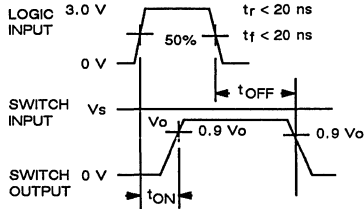
DIE TOPOGRAPHY (Cont'd)



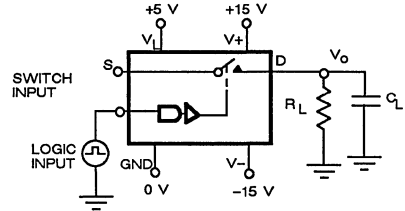
**5**

## SWITCHING TIME TEST CIRCUIT (DG417 AND DG418 ONLY)

$V_o$  is the steady state output with the switch ON. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



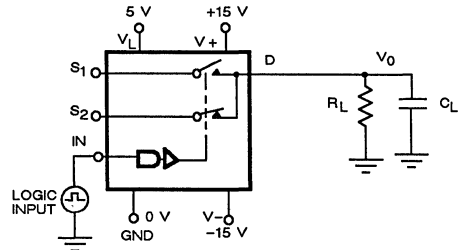
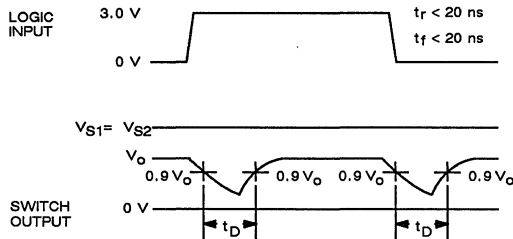
NOTE: Logic Input waveform is inverted for switches that have the opposite logic sense control



For load conditions, See Electrical Characteristics ( $C_L$  includes fixture and stray capacitance)

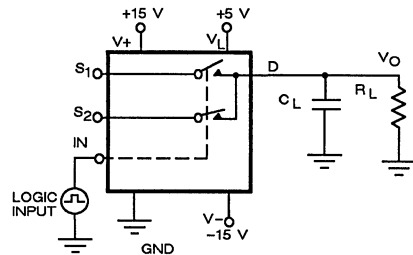
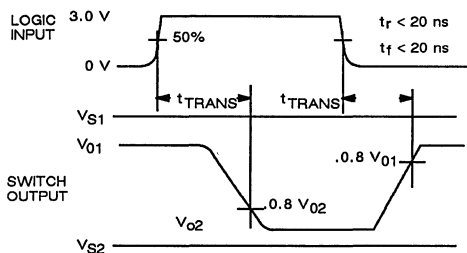
$$V_o = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

## BREAK-BEFORE-MAKE TIME TEST CIRCUIT (DG419 ONLY)



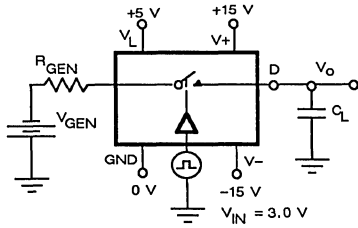
For Load Conditions, See Electrical Characteristics ( $C_L$  includes fixture and stray capacitance)

## TRANSITION TIME TEST CIRCUIT (DG419 ONLY)

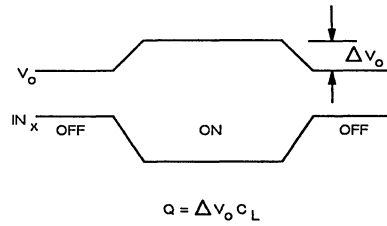


For Load Conditions, See Electrical Characteristics ( $C_L$  includes fixture and stray capacitance)

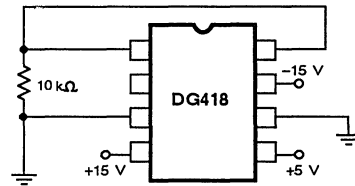
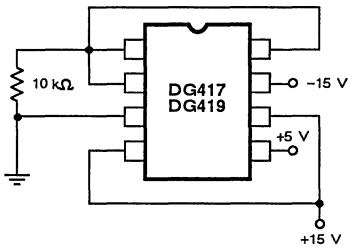
## CHARGE INJECTION TEST CIRCUIT



NOTE: FOR DG419  $R_{GEN1} = R_{GEN2}$   
 $V_{GEN1} = V_{GEN2}$

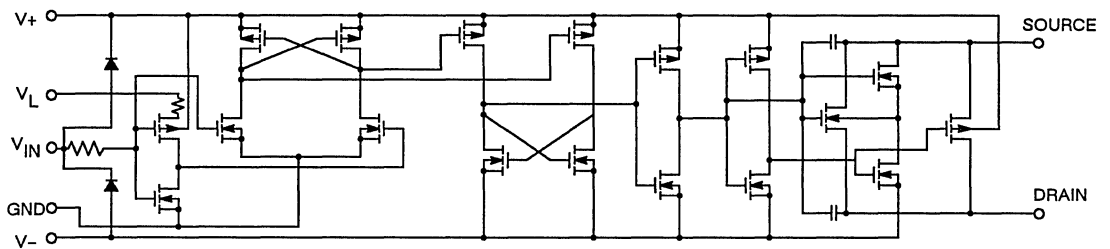


## BURN-IN CIRCUITS

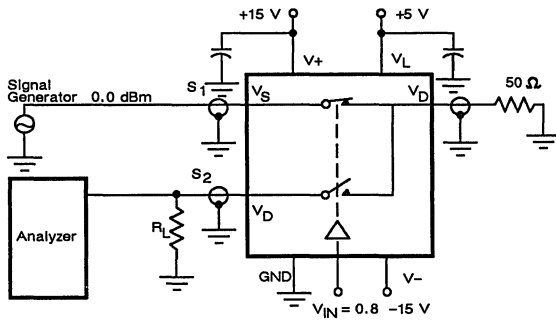


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## SCHEMATIC DIAGRAM (Typical Channel)



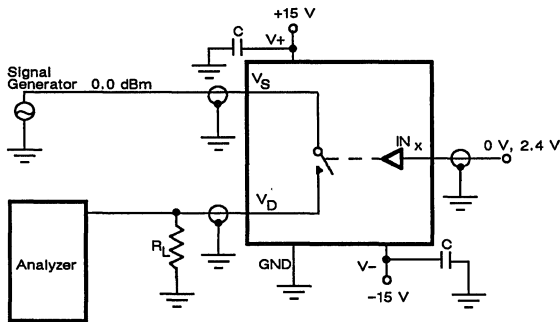
## CROSSTALK TEST CIRCUIT (DG419 ONLY)



REPEAT TEST, INTERCHANGING  $S_1$  AND  $S_2$ ,  $V_{IN} = 2.4$

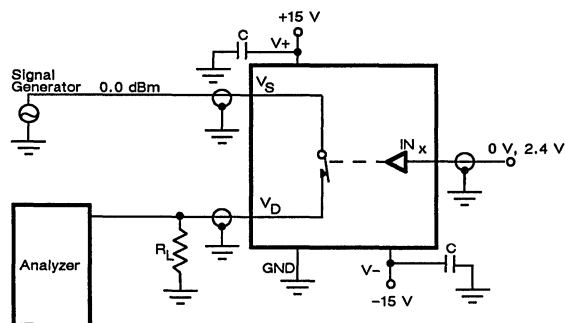
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## OFF ISOLATION TEST CIRCUIT



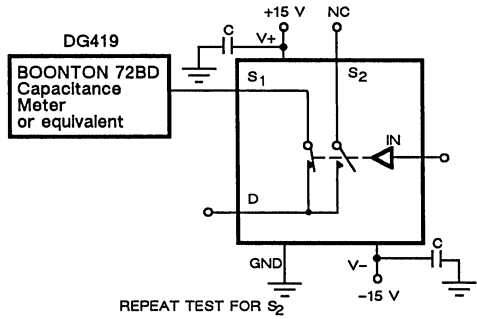
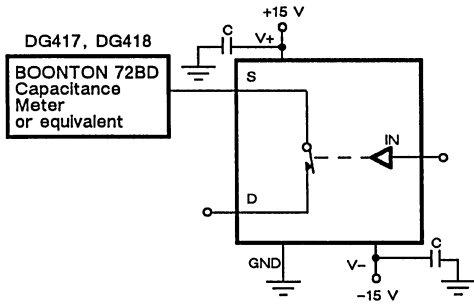
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## INSERTION LOSS TEST CIRCUIT

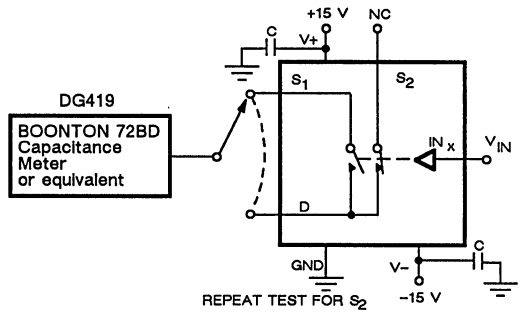
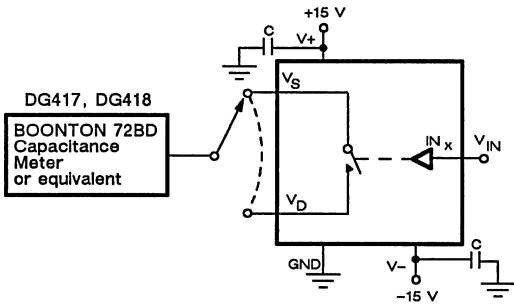


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

**SOURCE/DRAIN ON CAPACITANCE**

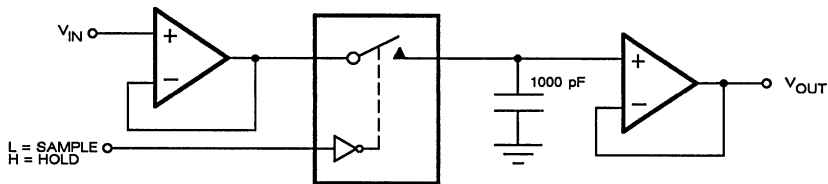


**SOURCE/DRAIN OFF CAPACITANCE**



**5**

**SAMPLE AND HOLD CIRCUIT**

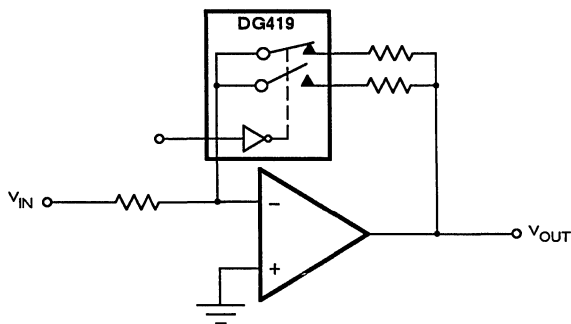


The DG417 minimizes offset errors due to its low charge injection. Throughput is improved because of its low ON resistance and fast switching speed.

---

**PROGRAMMABLE GAIN AMPLIFIER**


---



The DG419 accurately allows gain selection in a small package. Switching into virtual ground reduces distortion caused by  $r_{DS(ON)}$  variation as a function of analog signal amplitude.

---

**PIN DESCRIPTION**


---

SYMBOL	DESCRIPTION
S	An Analog channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground
V <sub>L</sub>	Logic Supply Voltage

# Low-Power – High-Speed Latchable CMOS Analog Switches

## FEATURES

- Latched Inputs
- $\pm 15$  Volt Input Range
- ON Resistance < 35  $\Omega$
- Fast Switching Action  
 $t_{ON} < 250$  ns
- Ultra Low Power Requirements  
( $P_D < 35 \mu W$ )
- TTL, CMOS Compatible

## BENEFITS

- Wide Dynamic Range
- $\mu P$  Compatible
- Reduced Component Count
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Battery Operation

## APPLICATIONS

- High Performance Data Bus Switching
- Precision Sample and Hold Circuits
- Digital Filters
- $\mu P$  Controlled Analog Systems

## DESCRIPTION

The DG421 series of dual monolithic analog switches features latchable logic inputs which simplify interfacing with microprocessors. This series combines fast switching speed ( $t_{ON} < 250$  ns), and low ON resistance ( $r_{DS(ON)} < 35 \Omega$ ) making it ideally suited for battery powered industrial and military applications that require  $\mu P$  compatible analog switches.

To achieve high-voltage ratings and superior switching performance, the DG421 series is built on Siliconix's high voltage silicon gate CMOS process. Break-before-make is guaranteed for the DG423. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON and blocks up to 30 volts peak-to-peak when OFF. ON resistance is nearly flat over the full

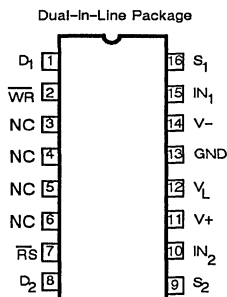
$\pm 15$  V analog range, rivaling JFET performance without the inherent dynamic range and supply voltage limitations.

When  $\overline{WR}$  is set LOW the  $\overline{IN}$  input data latches become transparent. When  $\overline{WR}$  goes HIGH the latches store the logic control data. The  $\overline{RS}$  pin is used to reset all the switches in the circuit to the default value (all inputs LOW) when it is set LOW.

This family offers three devices, which are differentiated by switch action as shown in the functional block diagrams. Packaging includes the 16-pin plastic and CerDIP DIPs. Performance grades include both the industrial, D suffix ( $-40$  to  $85^\circ C$ ) and the military, A suffix ( $-55$  to  $125^\circ C$ ) temperature ranges.

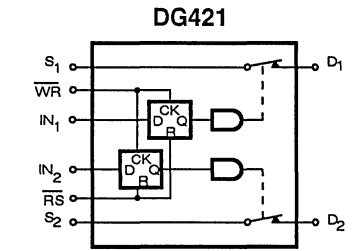
**5**

## PIN CONFIGURATION



Top View  
Order Numbers:  
CerDIP: DG421AK, DG421AK/883  
Plastic: DG421DJ

## FUNCTION BLOCK DIAGRAM



Two SPST Switches per Package

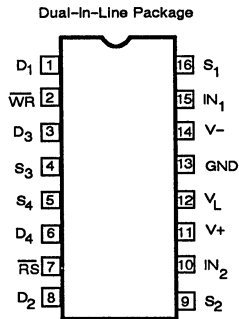
Truth Table

$\overline{WR}$	$\overline{RS}$	$IN_x$	SWITCH
0	1	0	OFF
		1	ON

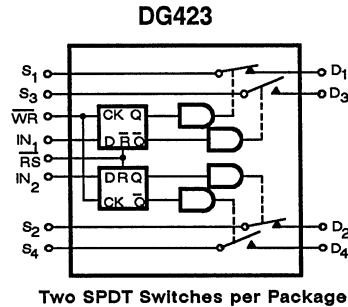
Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

## PIN CONFIGURATION

## FUNCTION BLOCK DIAGRAM



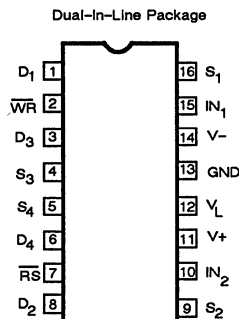
Top View  
 Order Numbers:  
 CerDIP: DG423AK, DG423AK/883  
 Plastic: DG423DJ



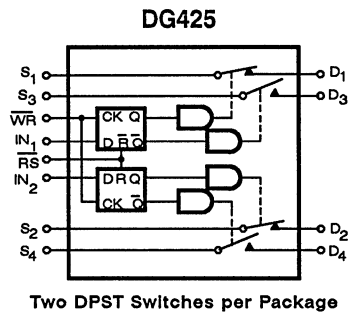
Truth Table

WR	$\overline{RS}$	$IN_X$	SWITCH 1, 2	SWITCH 3, 4
0	1	0 1	OFF ON	ON OFF

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V



Top View  
 Order Numbers:  
 CerDIP: DG425AK, DG425AK/883  
 Plastic: DG425DJ



Truth Table

WR	$\overline{RS}$	$IN_X$	SWITCH
0	1	0 1	OFF ON

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

- V+ ..... 44 V
- GND ..... 25 V
- VL ..... (GND -0.3 V) to 44 V
- Digital Inputs  $V_S, V_D^1$  ..... V- minus 2 V to (V+ plus 2 V)  
 ..... or 30 mA, whichever occurs first
- Continuous Current (Any Terminal) ..... 30 mA
- Current, S or D (Pulsed 1 ms, 10% duty) ..... 100 mA
- Storage Temperature (A Suffix) ..... -65 to 150°C  
 (D Suffix) ..... -65 to 125°C

- Operating Temperature (A Suffix) ..... -55 to 125°C  
 (D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*

- 16-Pin Plastic DIP\*\* ..... 450 mW
- 16-Pin CerDIP\*\*\* ..... 900 mW

\* All leads welded or soldered to PC Board.  
 \*\* Derate 6 mW/°C above 75°C.  
 \*\*\* Derate 12 mW/°C above 75°C.

1 Signals on Sx, Dx, or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.



## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_L = 5\text{ V}$ , $GND = 0\text{ V}$ $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^e$	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$				-15	15	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -10\text{ mA}$ , $V_D = \pm 8.5\text{ V}$ $V_+ = 13.5\text{ V}$ , $V_- = -13.5\text{ V}$	1,3 2	25		35 45		35 45	$\Omega$
Switch OFF Leakage Current	$I_{S(OFF)}$	$V_+ = 16.5\text{ V}$ , $V_- = -16.5\text{ V}$ $V_D = -15.5\text{ V}$ , $V_S = 15.5\text{ V}$	1 2	-0.01	-0.25 -20	0.25 20	-0.25 -20	0.25 20	nA
	$I_{D(OFF)}$	$V_D = 15.5\text{ V}$ , $V_S = -15.5\text{ V}$	1 2	-0.01	-0.25 -20	0.25 20	-0.25 -20	0.25 20	
Channel ON Leakage Current	$I_{D(ON)}$	$V_+ = 16.5\text{ V}$ , $V_- = -16.5\text{ V}$ $V_S = V_D = \pm 15.5\text{ V}$	1 2	-0.04	-0.4 -40	0.4 40	-0.4 -40	0.4 40	
<b>INPUT</b>									
Input Current with $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ under test = $0.8\text{ V}$ all other = $2.4\text{ V}$	1,2	0.005	-0.5	0.5	-0.5	0.5	$\mu\text{A}$
Input Current with $V_{IN}$ High	$I_{IH}$	$V_{IN}$ under test = $2.4\text{ V}$ all other = $0.8\text{ V}$	1,2	0.005	-0.5	0.5	-0.5	0.5	
<b>DYNAMIC</b>									
Turn-ON Time	$t_{ON}$	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ See Switching Time Test Circuit	1	170		250		250	ns
Turn-OFF Time	$t_{OFF}$		1	140		200		200	
Latch Timing	$t_{WW}$	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = \pm 10\text{ V}$	1		200		200		
	$t_{DW}$		1		100		100		
	$t_{WD}$		1		30		30		
Break-before-Make Time Delay	$t_D$	DG423 Only $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$	1	25	10		10		
Charge Injection <sup>c</sup>	Q	$C_L = 10\text{ nF}$ $V_{gen} = 0\text{ V}$ , $R_{gen} = 0\ \Omega$	1	60		100		100	pC
OFF Isolation Reject Ratio		$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ $f = 1\text{ MHz}$	1	68					dB
Crosstalk (Channel to Channel)		Between Any Two Channels $R_L = 50\ \Omega$ , $f = 1\text{ MHz}$ $C_L = 5\text{ pF}$	1	85					

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
Source OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	1	9					pF
Drain OFF Capacitance	C <sub>D(OFF)</sub>		1	9					
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		1	18					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0 or 5 V	1	.0001		1		1	μA
Negative Supply Current	I <sub>-</sub>		2			5		5	
Logic Supply Current	I <sub>L</sub>		1	-.0001	-1		-1		
Ground Current	I <sub>GND</sub>		2		-5		-5		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = input voltage to perform proper function.

**DIE TOPOGRAPHY**

93 mils

DG421

83 mils

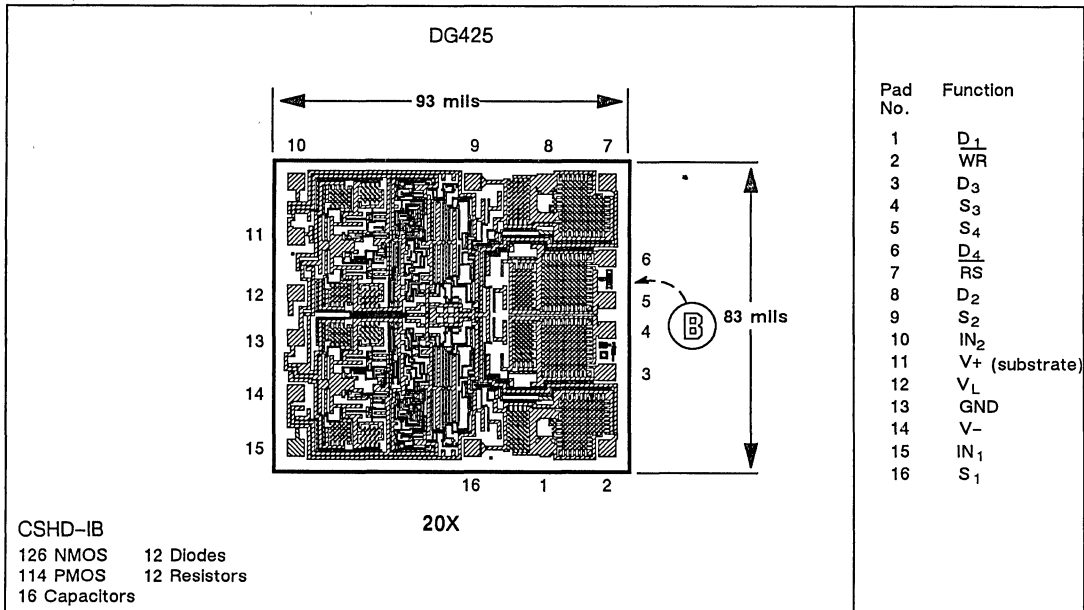
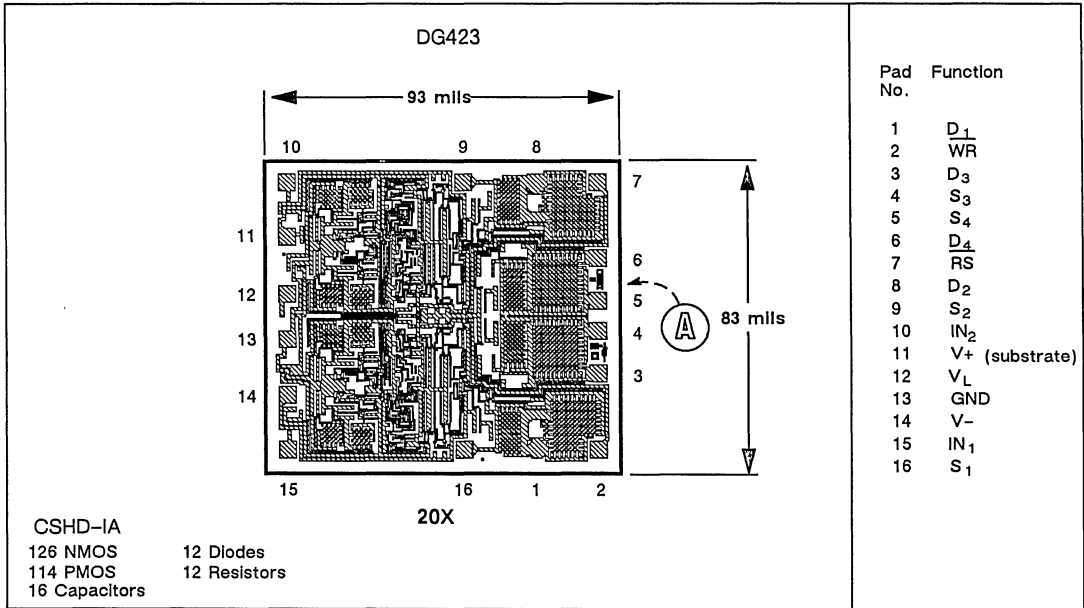
20X

Pad No.	Function
1	D <sub>1</sub>
2	WR
3	NC
4	NC
5	NC
6	NC
7	RS
8	D <sub>2</sub>
9	S <sub>2</sub>
10	IN <sub>2</sub>
11	V <sub>+</sub> (substrate)
12	V <sub>L</sub>
13	GND
14	V <sub>-</sub>
15	IN <sub>1</sub>
16	S <sub>1</sub>

CSHDIA or CSHDIB

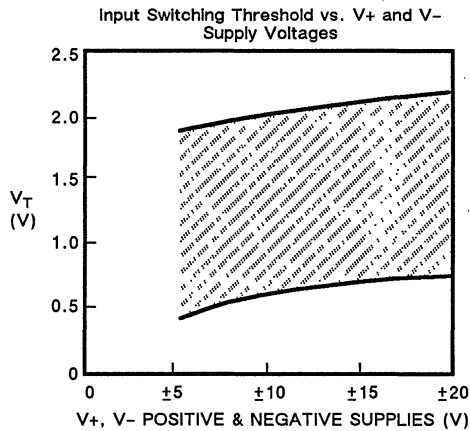
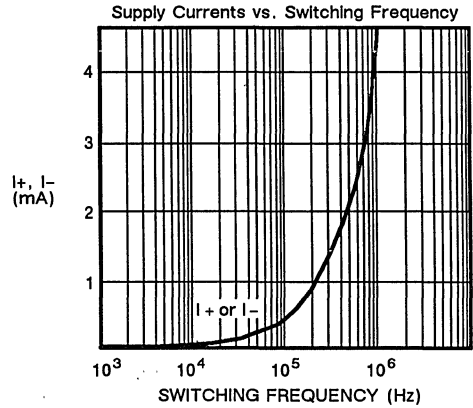
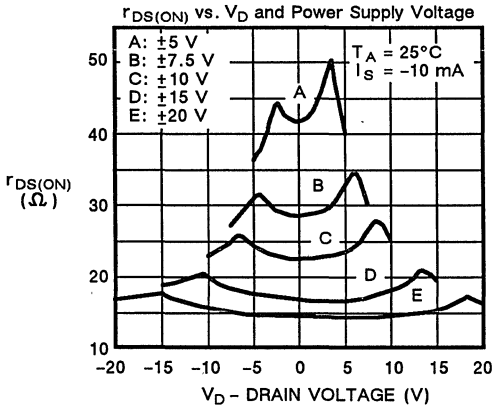
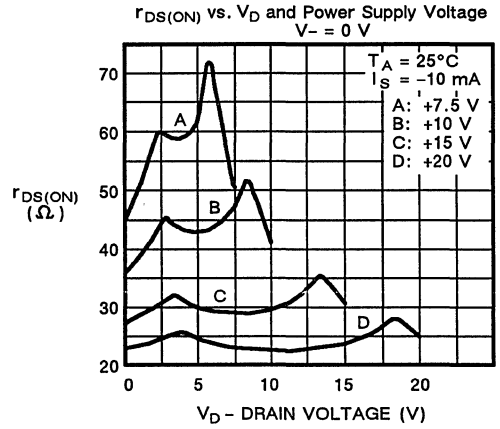
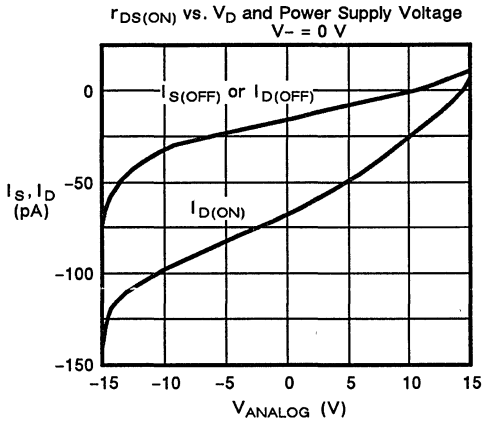
126 NMOS	16 Capacitors
114 PMOS	12 Diodes
	12 Resistors

**DIE TOPOGRAPHY (Cont'd)**



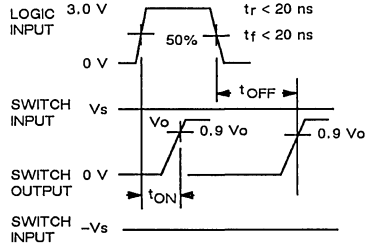
**5**

## TYPICAL CHARACTERISTICS

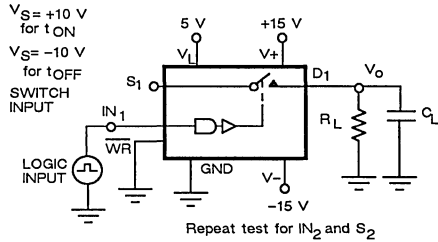


**SWITCHING TIME TEST CIRCUIT**

$V_o$  is the steady state output with the switch ON. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



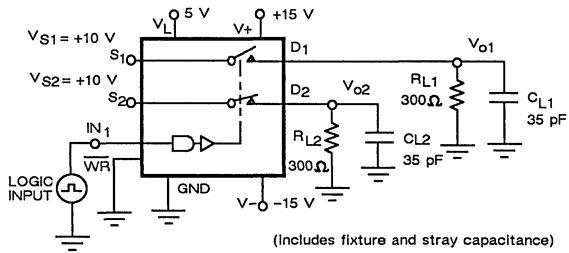
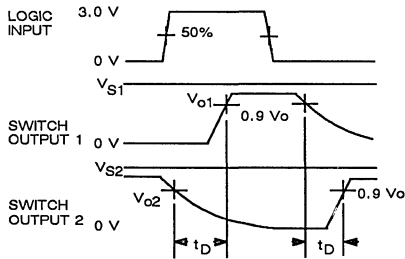
NOTE: Logic input waveform is inverted for switches that have the opposite logic sense control



Repeat test for  $IN_2$  and  $S_2$   
For load conditions, See Electrical Characteristics  
 $C_L$  (includes fixture and stray capacitance)

$$V_o = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

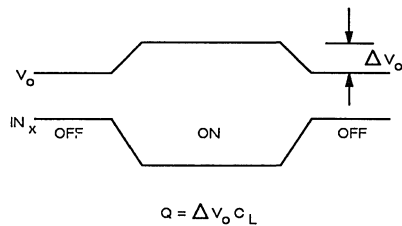
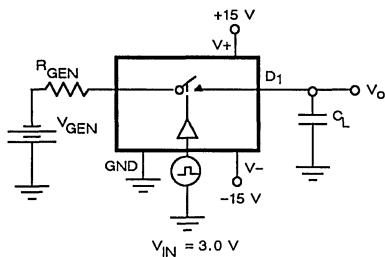
**BREAK-BEFORE-MAKE TIME TEST CIRCUIT**



(Includes fixture and stray capacitance)

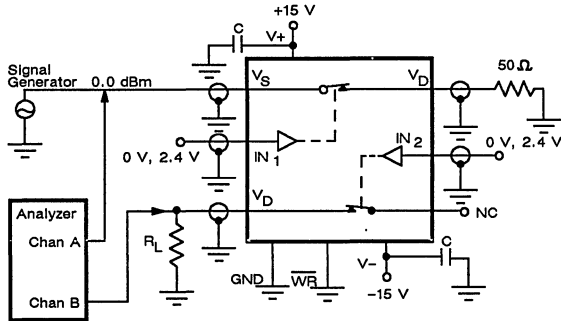
**5**

**CHARGE INJECTION TEST CIRCUIT**



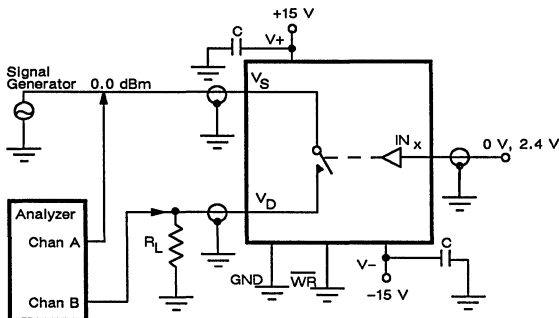
$$q = \Delta V_o C_L$$

## CROSSTALK TEST CIRCUIT



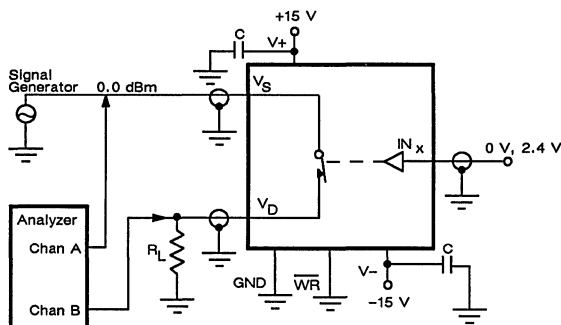
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## OFF ISOLATION TEST CIRCUIT



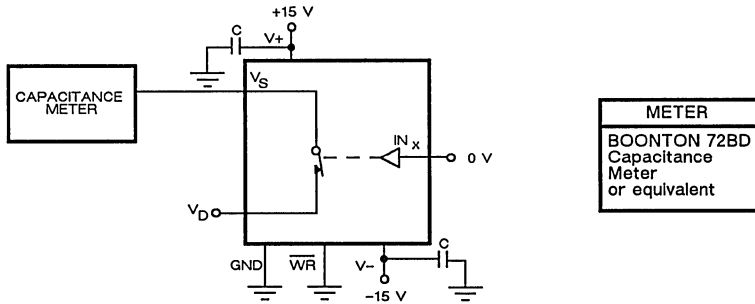
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## INSERTION LOSS TEST CIRCUIT

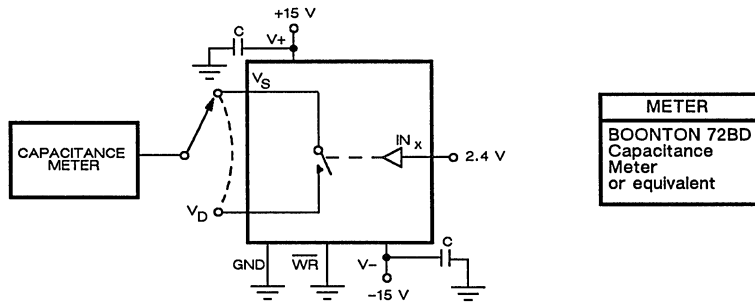


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

**SOURCE/DRAIN ON CAPACITANCE**



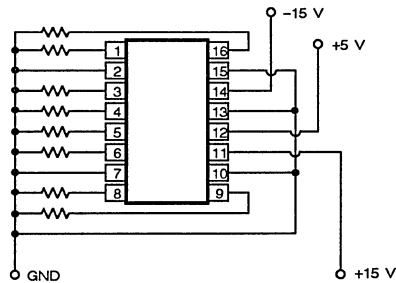
**SOURCE/DRAIN OFF CAPACITANCE**



5

**BURN-IN DIAGRAM**

**DG421/423/425**



All Resistors = 10k  $\Omega$

## PIN DESCRIPTION

### SYMBOL DESCRIPTION

S	An Analog Channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground
V <sub>L</sub>	Logic Supply Voltage
$\overline{WR}$	Latch Write Control Input
$\overline{RS}$	Latch Reset Control Input

## APPLICATIONS

Figure 1 shows a circuit configured to increase the effective resolution of the 12-bit DAC to 13 bits. The circuit operates with a sign plus magnitude code. A sign bit of "0" connects R3 to GND, giving 12-bit resolution per quadrant.

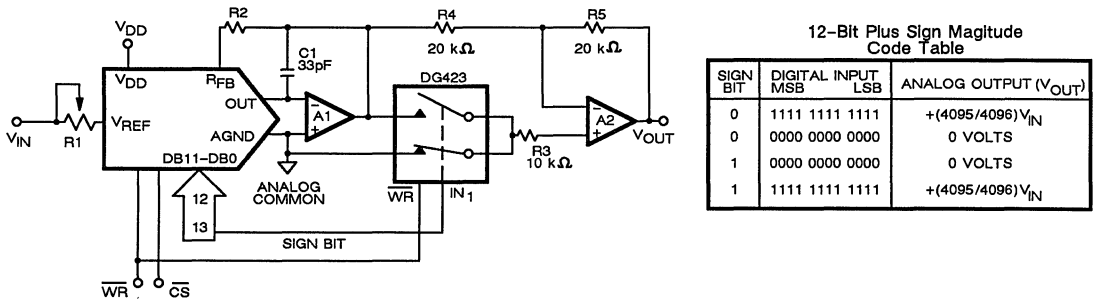


Figure 1. 12-Bit Plus Sign Magnitude D/A Converter

## LATCH TRUTH TABLE

IN <sub>x</sub>	$\overline{RS}$	$\overline{WR}$	LATCH/SWITCH X
X	1	0	TRANSPARENT LATCH OPERATION
X	1	$\downarrow$	CONTROL DATA LATCHED-IN. SWITCHES ON OR OFF AS SELECTED BY LAST IN <sub>x</sub>
X	0	X	ALL LATCHES RESET, SWITCHES ON OR OFF AS WHEN IN <sub>x</sub> =0, $\overline{WR}$ = 0, $\overline{RS}$ = 1
X	$\downarrow$	X	ALL LATCHES RESET, SWITCHES ON OR OFF AS WHEN IN <sub>x</sub> =0, $\overline{WR}$ = 0, $\overline{RS}$ = 1



# Monolithic Quad SPST CMOS Analog Switches

## FEATURES

- $\pm 15$  Volt Input Range
- ON Resistance < 80  $\Omega$
- Fast Switching Action  
 $t_{ON} < 160$  ns  
 $t_{OFF} < 80$  ns
- TTL, CMOS Compatible
- DG201A/DG202 Upgrades
- ESDS Protection  $> \pm 4000$  V
- Balanced Charge Injection

## BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Simple Interfacing

## APPLICATIONS

- Sample and Hold circuits
- Data Acquisition
- Automatic Test Equipment
- Audio and Video Switching
- Communication Systems
- Battery Operated Systems

## DESCRIPTION

The DG441 series of monolithic quad analog switches was designed to provide high speed, low error switching of analog, audio and video signals. Combining low ON resistance (< 80  $\Omega$ ) with high speed ( $t_{ON} < 160$  ns), makes the DG441 family ideally suited for upgrading DG201A/DG202 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high voltage ratings and superior switching performance, the DG441 series was built on Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 volts peak-to-peak when off. ON resistance is very flat over the full  $\pm 15$  V analog range, rivaling JFET performance without the inherent dynamic range limitation.

The two devices in this series are differentiated by the type of switch action as shown in the functional block diagrams for each. The DG441/442 are available in 16-pin plastic and CerDIP and SO packages. Performance grades include both a military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature range.

**5**

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

### DG441

Four SPST Switches per Package\*

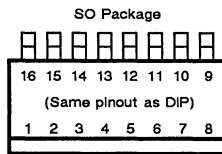
Truth Table

LOGIC	SWITCH
0	ON
1	OFF

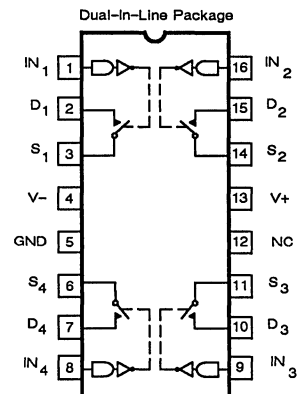
Logic "0"  $\leq 0.8$  V

Logic "1"  $\geq 2.4$  V

\* Switches Shown for Logic "1" Input



Top View  
Order Number:  
DG441DY



Top View  
Order Numbers:  
CerDIP: DG441AK  
 DG441AK/883  
 Plastic: DG441DJ

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION (Cont'd)

### DG442

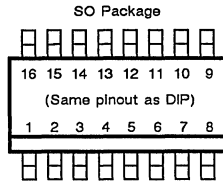
Four SPST Switches per Package

Truth Table

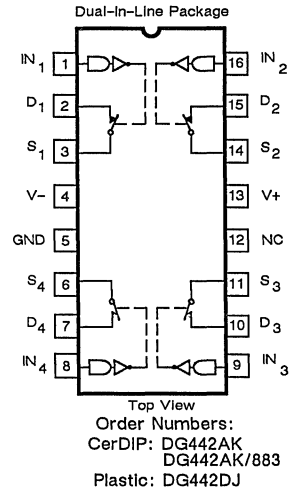
LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq 0.8$  V  
 Logic "1"  $\geq 2.4$  V

\* Switches Shown for Logic "1" Input



Top View  
 Order Number:  
 DG442DY



### ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V<sub>-</sub><sup>1</sup>

V+	44 V
GND	25 V
V <sub>L</sub>	(GND -0.,3 V) to 44 V
Digital Inputs V <sub>S</sub> , V <sub>D</sub> <sup>1</sup>	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle)	100 mA
Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
 (D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*

16-Pin Plastic DIP**	450 mW
16-Pin CerDIP***	900 mW
16-Pin SO****	600 mW

- \* All leads welded or soldered to PC Board.
- \*\* Derate 6 mW/°C above 75°C.
- \*\*\* Derate 12 mW/°C above 75°C.
- \*\*\*\*Derate 7.6 mW/°C above 75°C.

<sup>1</sup> Signals on S<sub>x</sub>, D<sub>x</sub>, or IN<sub>x</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

### ELECTRICAL CHARACTERISTICS<sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V V- = -15 V GND = 0 V V <sub>IN</sub> = 2.4, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>				-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ± 8.5 V V+ = 13.5 V, V- = -13.5 V	1,3 2			80 100		80 100	Ω
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>D</sub> = ± 15.5 V, V <sub>S</sub> = ∓ 15.5 V	1 2		-0.25 -20	0.25 20	-0.25 -20	0.25 20	nA
	I <sub>D(OFF)</sub>		1 2		-0.25 -20	0.25 20	-0.25 -20	0.25 20	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ± 15.5 V	1 2		-0.4 -40	0.4 40	-0.4 -40	0.4 40	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.4, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
Input Current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0.8 V All Other = 2.4 V	1,2		-0.5	0.5	-0.5	0.5	μA
Input Current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 2.4 V All Other = 0.8 V	1,2		-0.5	0.5	-0.5	0.5	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 5 pF See Figure 1 V <sub>S</sub> = ±10 V	1			160		160	ns
Turn-OFF Time	t <sub>OFF</sub>		1			80		80	
Charge Injection	Q	C <sub>L</sub> = 10 nF, V <sub>S</sub> = 0 V V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	1		-20	20	-20	20	pC
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0 or 5 V	1 2			100 100		100 100	μA
Negative Supply Current	I <sub>-</sub>		1 2		-1 -5		-1 -5		
Ground Current	I <sub>GND</sub>		1 2		-100 -100		-100 -100		

**5**

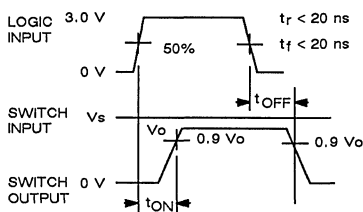
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
UNIPOLAR SUPPLY									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = 0 V GND = 0 V V <sub>IN</sub> = 2.4, 0.8 V	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>				0	12	0	12	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 3 V, 8 V V <sub>+</sub> = 10.8 V	1,3 2			160 200		160 200	Ω

ELECTRICAL CHARACTERISTICS <sup>a</sup>				UNIPOLAR SUPPLY						
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = 0 V GND = 0 V V <sub>IN</sub> = 2.4, 0.8 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		D SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF See Switching Time Test Circuit V <sub>S</sub> = 8 V	1			400		400	ns	
Turn-OFF Time	t <sub>OFF</sub>		1			200		200		
Charge Injection	Q	C <sub>L</sub> = 10 nF V <sub>gen</sub> = 6.6 V, R <sub>gen</sub> = 0 Ω V <sub>+</sub> = 13.2 V	1			-20	20	-20	20	pC
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 13.2 V V <sub>IN</sub> = 0 or 5 V	1 2			100 100		100 100	μA	
Negative Supply Current	I <sub>-</sub>	V <sub>IN</sub> = 0 or 5 V	1 2			-1 -100		-1 -100		
Ground Current	I <sub>GND</sub>		1 2			-100 -100		-100 -100		

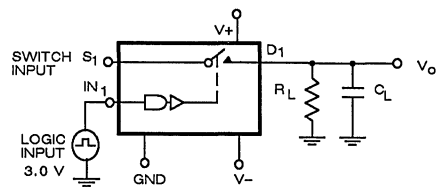
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = Input voltage to perform proper function.

## SWITCHING TIME TEST CIRCUIT



NOTE: Logic Input waveform is inverted for switches that have the opposite logic sense

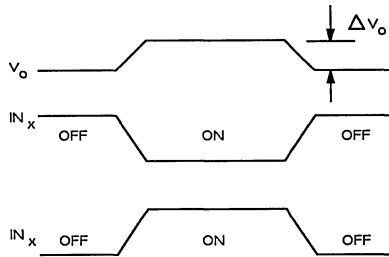
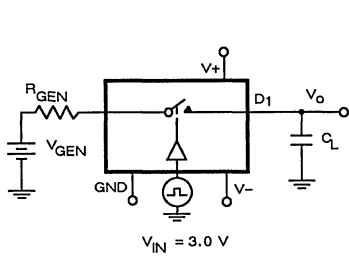


Repeat test for Ch 2, 3, 4

For load conditions, See Electrical Characteristics C<sub>L</sub> (Includes fixture and stray capacitance)

$$V_o = V_s \frac{R_L}{R_L + r_{DS(ON)}}$$

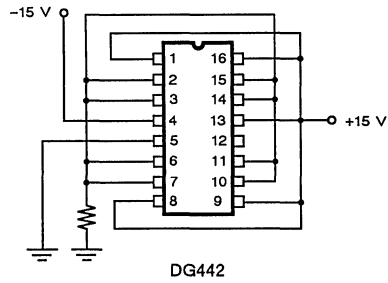
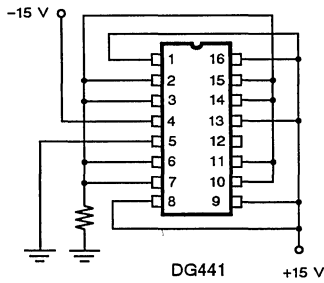
**CHARGE INJECTION TEST CIRCUIT**



$$q = \Delta V_o C_L$$

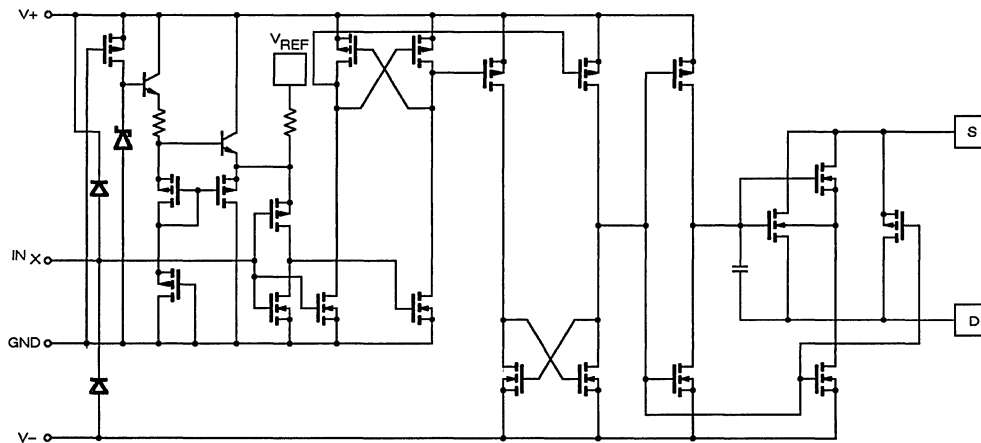
$I_{N_x}$  dependent on switch configuration  
Input Polarity determined by sense of switch

**BURN-IN CIRCUITS**

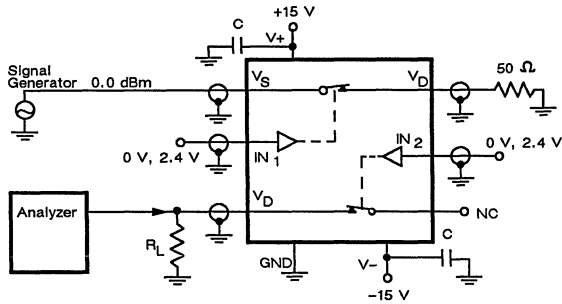


Note: All Resistors are 10 kΩ unless otherwise specified

**SCHEMATIC DIAGRAM (TYPICAL CHANNEL)**

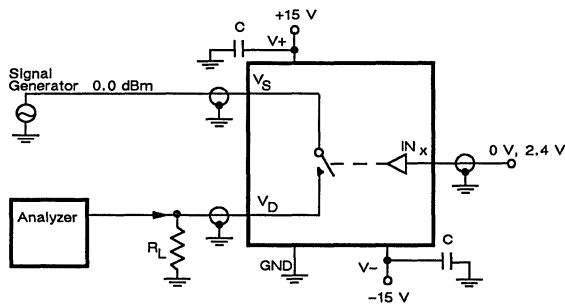


## CROSSTALK TEST CIRCUIT



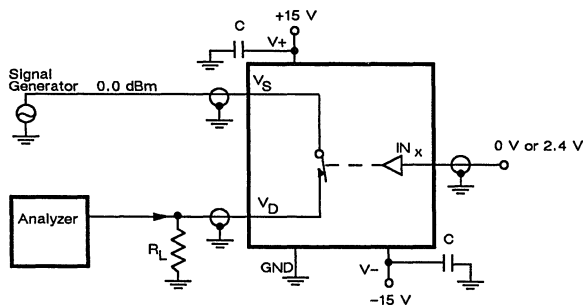
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## OFF ISOLATION TEST CIRCUIT



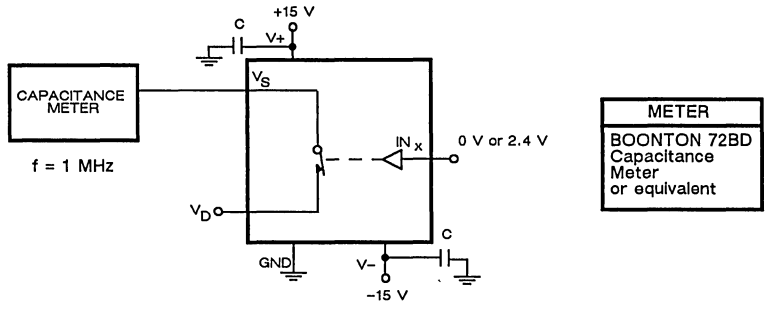
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## INSERTION LOSS TEST CIRCUIT

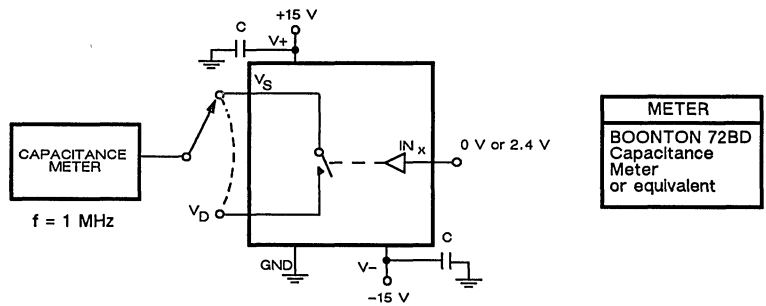


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

**SOURCE + DRAIN ON CAPACITANCE**



**SOURCE + DRAIN OFF CAPACITANCE**

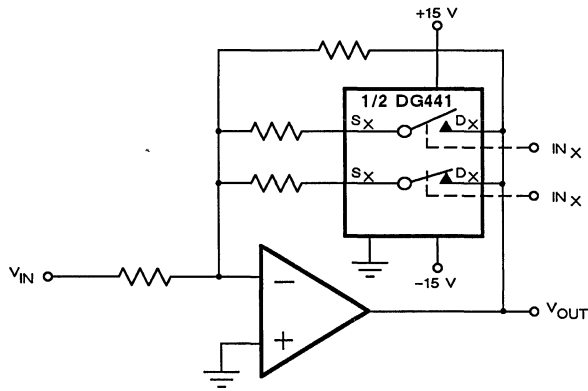


**PIN DESCRIPTION**

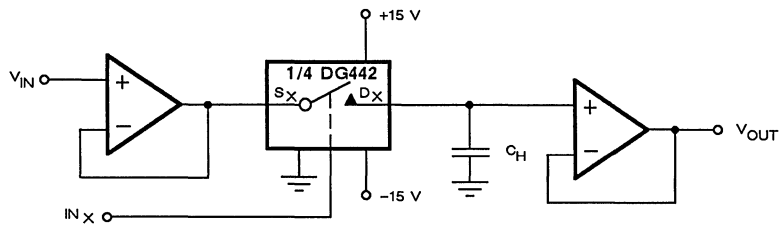
SYMBOL	DESCRIPTION
S	Analog Channel Input or Output
D	Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground

## APPLICATIONS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>INH</sub> (Min) HIGH Logic Input Voltage (V)	V <sub>INL</sub> (Max) LOW Logic Input Voltage (V)	V <sub>S</sub> or V <sub>D</sub> Analog Signal Range (V)
22	-22	2.4	0.8	-22 to 22
15	-15	2.4	0.8	-15 to 15
10	-10	2.4	0.8	-10 to 10
5	-5	2.0	0.5	-5 to 5
12	0	2.4	0.8	0 to 12



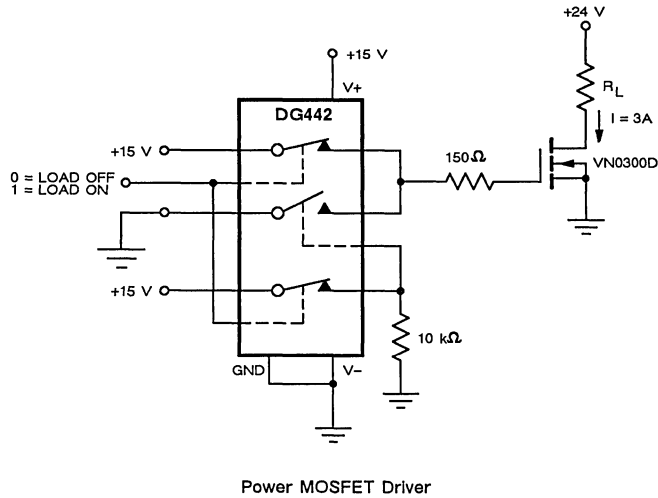
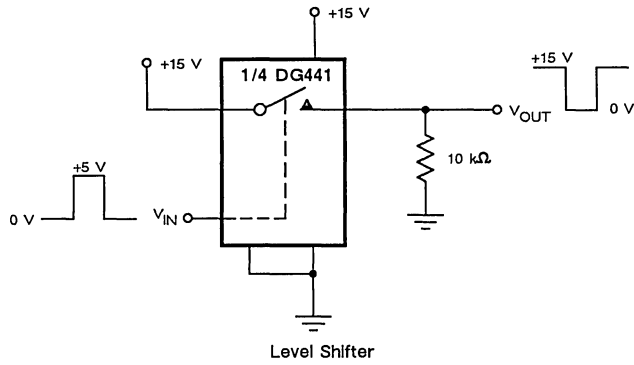
Programmable Gain Amplifier



H = SAMPLE  
L = HOLD

Sample and Hold





## Monolithic Quad SPST CMOS Analog Switches

### FEATURES

- $\pm 15$  Volt Input Range
- ON Resistance  $< 80 \Omega$
- Fast Switching Action  
 $t_{ON} < 160$  ns  
 $t_{OFF} < 80$  ns
- TTL, CMOS Compatible
- DG211/DG212 Upgrades
- ESDS Protection  $> \pm 4000$  V

### BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Simple Interfacing

### APPLICATIONS

- Sample and Hold circuits
- Data Acquisition
- Automatic Test Equipment
- Audio and Video Switching
- Communication Systems
- Battery Operated Systems

### DESCRIPTION

The DG444 series of monolithic quad analog switches was designed to provide high speed, low error switching of analog signals. Combining low power ( $< 35$  microwatts) with high speed ( $t_{ON} < 160$  ns), the DG444/445 is ideally suited for upgrading DG211/DG212 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high-voltage ratings and superior switching performance, the DG444 series was built on Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full  $\pm 15$  V analog range, rivaling JFET performance without the inherent dynamic range limitation.

The two devices in this series are differentiated by the type of switch action as shown in the functional block diagrams for each. Packaging options include the 16-pin plastic and small outline. The performance grade for this series is the industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ) temperature range.

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

#### DG444

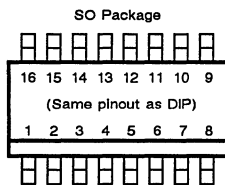
Four SPST Switches per Package

Truth Table

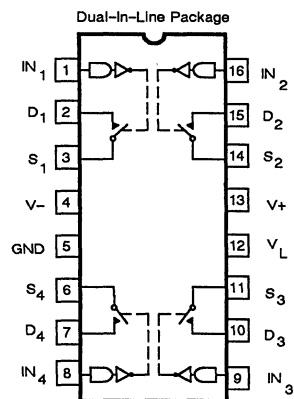
LOGIC	SWITCH
0	ON
1	OFF

Logic "0"  $\leq 0.8$  V

Logic "1"  $\geq 2.4$  V



Top View  
 Order Number:  
 DG444DY



Top View

Order Numbers:  
 DG444DJ

**FUNCTIONAL BLOCK DIAGRAM PIN CONFIGURATION**

**DG445**

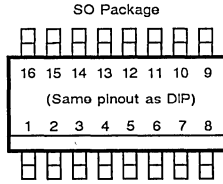
Four SPST Switches per Package

Truth Table

LOGIC	SWITCH
0	OFF
1	ON

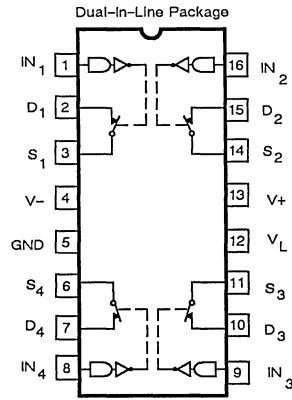
Logic "0"  $\leq$  0.8 V

Logic "1"  $\geq$  2.4 V



Top View

Order Number:  
DG445DY



Top View

Order Numbers:  
DG445DJ

**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to V-

- V+ ..... 44 V
- GND ..... 25 V
- VL ..... (GND -0.,3 V) to 44 V
- Digital Inputs VS, VD<sup>1</sup> ... (V- minus 2 V) to (V+ plus 2 V)  
..... or 30 mA, whichever occurs first
- Current (Any Terminal) continuous ..... 30 mA
- Current (S or D) Pulsed 1 ms, 10% duty ..... 100 mA
- Storage Temperature (D Suffix) ..... -65 to 125°C

Operating Temperature (D Suffix) ..... -40 to 85°C

Power Dissipation (Package) \*

- 16-Pin Plastic DIP\*\* ..... 450 mW
- 16-Pin SO\*\*\* ..... 600 mW

\* All leads welded or soldered to PC Board.

\*\* Derate 6 mW/°C above 75°C.

\*\*\* Derate 7.6 mW/°C above 75°C.

<sup>1</sup> Signals on Sx, Dx, or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

**5**

**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V V- = -15 V VL = 5 V GND = 0 V VIN = 2.4, 0.8 V <sup>e</sup>	LIMITS				UNIT
			1=25°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>							
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			-15	15	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ± 8.5 V V+ = 13.5 V, V- = -13.5 V	1,3 2			80 100 Ω	
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>D</sub> = ± 15.5 V, V <sub>S</sub> = ± 15.5 V	1 2		-0.25 -20	0.25 20	nA
	I <sub>D(OFF)</sub>		1 2		-0.25 -20	0.25 20	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V+ = 16.5 V, V- = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ± 15.5 V	1 2		-0.4 -40	0.4 -40	

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V GND = 0 V V <sub>IN</sub> = 2.4, 0.8 V <sup>e</sup>	LIMITS				UNIT
			1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>							
Input Current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0.8 V All Other = 2.4 V	1,2		-0.5	0.5	μA
Input Current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 2.4 V All Other = 0.8 V	1,2		-0.5	0.5	
<b>DYNAMIC</b>							
Turn-ON Time	t <sub>ON</sub>	R <sub>L</sub> = 1 k Ω, C <sub>L</sub> = 5 pF See Figure 1 V <sub>S</sub> = ±10 V	1			160	ns
Turn-OFF Time	t <sub>OFF</sub>		1			80	
Charge Injection <sup>c</sup>	Q	C <sub>L</sub> = 10 nF, V <sub>S</sub> = 0 V V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	1		-10	10	pC
<b>SUPPLY</b>							
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0 or 5 V	1 2			1 5	μA
Negative Supply Current	I <sub>-</sub>		1 2		-1 -5		
Logic Supply Current	I <sub>L</sub>		1 2			1 5	
Ground Current	I <sub>GND</sub>		1 2		-1 -5		

ELECTRICAL CHARACTERISTICS <sup>a</sup>								(UNIPOLAR SUPPLY)
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = 0 V V <sub>L</sub> = 5 V GND = 0 V V <sub>IN</sub> = 2.4, 0.8 V <sup>e</sup>	LIMITS				UNIT	
			1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>								
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>				0	12	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 3 V, 8 V V <sub>+</sub> = 10.8 V, V <sub>L</sub> = 5.25 V	1 2,3			160 200	Ω	

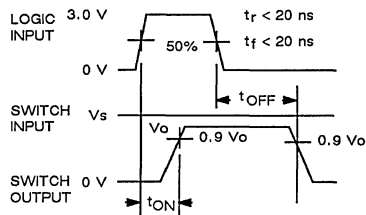
ELECTRICAL CHARACTERISTICS <sup>a</sup>			(UNIPOLAR SUPPLY)				
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = 0\text{ V}$ $V_L = 5\text{ V}$ $GND = 0\text{ V}$ $V_{IN} = 2.4, 0.8\text{ V}^e$	LIMITS				UNIT
			1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>							
Turn-ON Time	$t_{ON}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ See Figure 1 $V_S = 8\text{ V}$	1		400	ns	
Turn-OFF Time	$t_{OFF}$		1		200		
Charge Injection <sup>c</sup>	Q	$C_L = 10\text{ nF}, V_L = 5.25\text{ V}$ $V_{gen} = 6.6\text{ V}, R_{gen} = 0\Omega$ $V_+ = 13.2\text{ V}$	1		-40 40	pC	
<b>SUPPLY</b>							
Positive Supply Current	$I_+$	$V_+ = 13.2\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	1 2,3		1 5	$\mu\text{A}$	
Negative Supply Current	$I_-$	$V_{IN} = 0\text{ or }5\text{ V}$	1 2,3	-1 -5			
Logic Supply Current	$I_L$	$V_L = 5.25\text{ V}$ $V_{IN} = 0\text{ or }5\text{ V}$	1 2,3		1 5		
Ground Current	$I_{GND}$	$V_{IN} = 0\text{ or }5\text{ V}$	1 2,3	-1 -5			

**NOTES:**

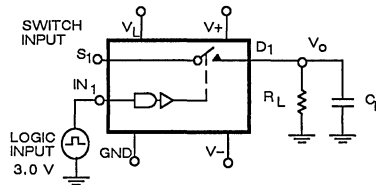
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e.  $V_{IN}$  = input voltage to perform proper function.

**SWITCHING TIME TEST CIRCUIT**

$V_O$  is the steady state output with the switch ON. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense

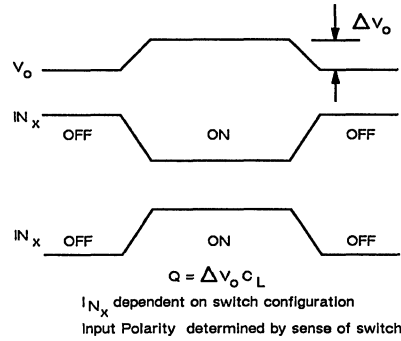
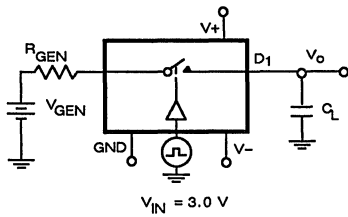


Repeat test for Ch 2, 3, 4

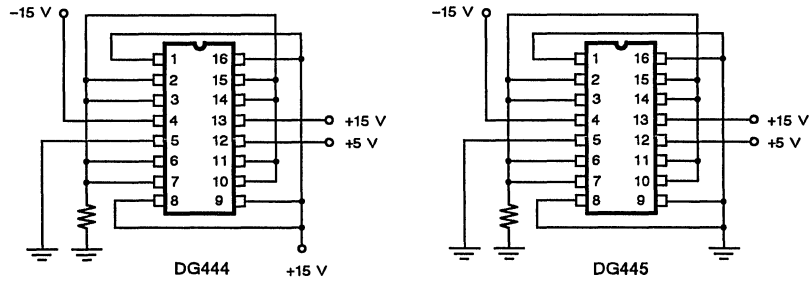
For load conditions, See Electrical Characteristics  $C_L$  (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

## CHARGE INJECTION TEST CIRCUIT

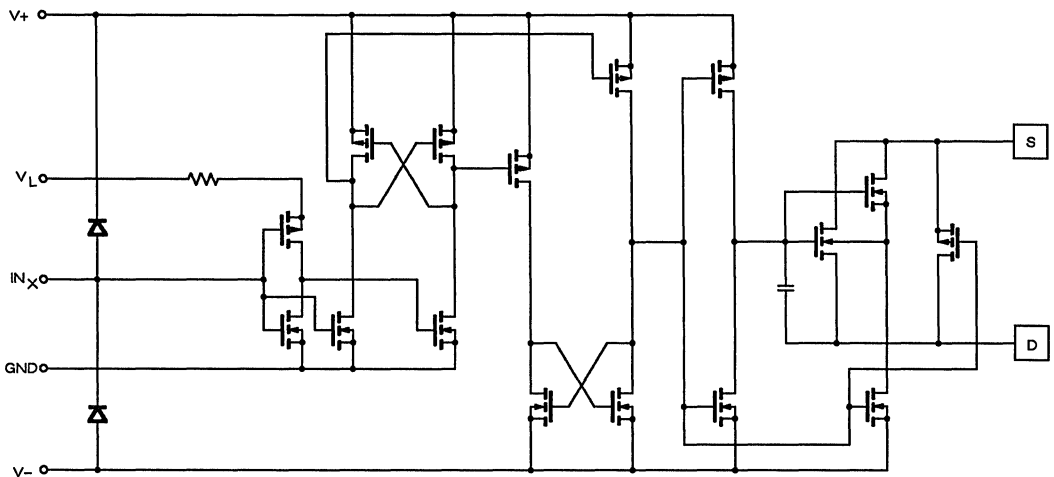


## BURN-IN CIRCUITS

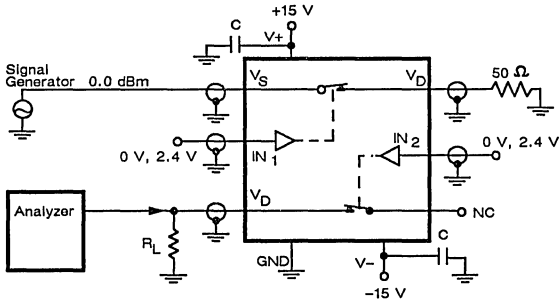


Note: All Resistors are 10 kΩ unless otherwise specified

## SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

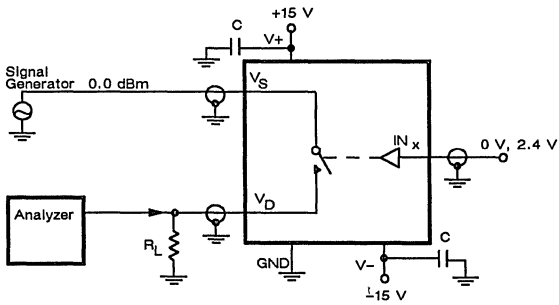


**CROSSTALK TEST CIRCUIT**



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

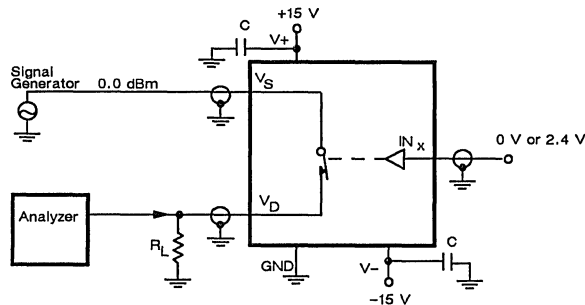
**OFF ISOLATION TEST CIRCUIT**



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

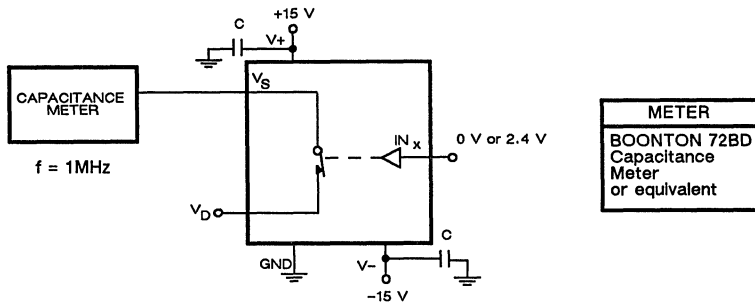
**5**

**INSERTION LOSS TEST CIRCUIT**

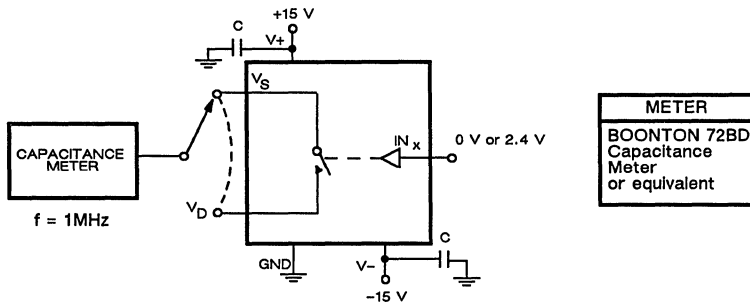


FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## SOURCE + DRAIN ON CAPACITANCE



## SOURCE + DRAIN OFF CAPACITANCE



## PIN DESCRIPTION

SYMBOL	DESCRIPTION
S	Analog Channel Input or Output
D	Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply Voltage
V-	Negative Supply Voltage
GND	Digital Ground
V <sub>L</sub>	Logic Supply Voltage



APPLICATIONS

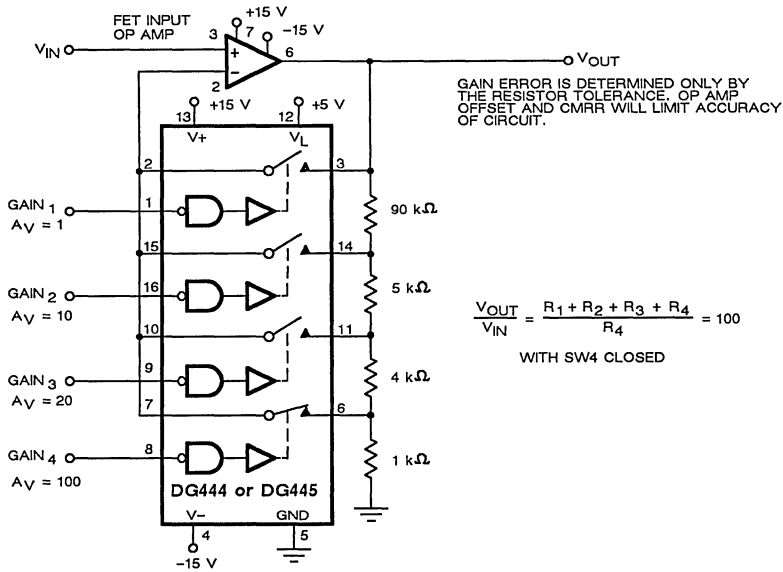


Figure 6. Precision-Weighted Resistor Programmable-Gain Amplifier

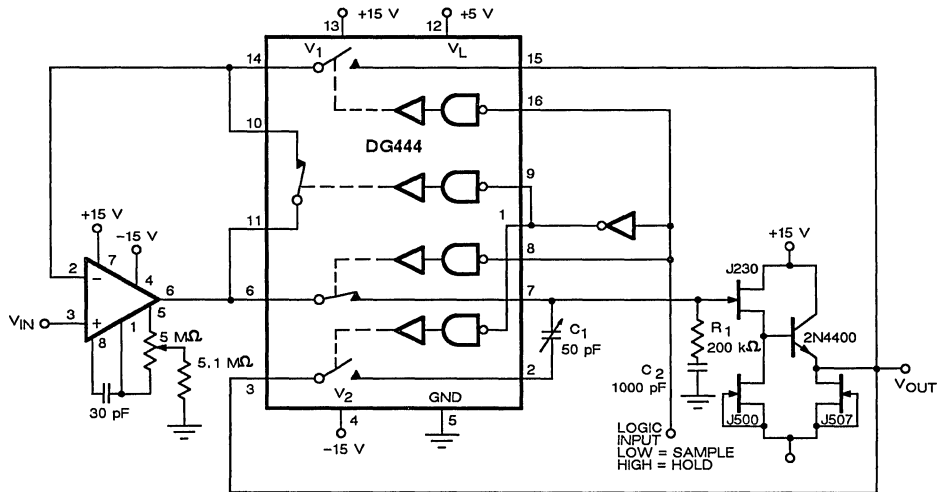


Figure 7. Precision Sample-and-Hold

## High-Speed CMOS Octal Analog Switch Array

### FEATURES

- $\pm 15$  Volt Input Range
- ON Resistance < 100  $\Omega$
- Fast Switching < 200 ns
- Any Combination of 8 SPST to the Output
- TTL and CMOS Compatible
- ESDS Protection >  $\pm 4000$  V

### BENEFITS

- Low Signal Distortion
- Devices Can Be Chained For System Expansion
- Master Reset To All OFF State
- Simple Interfacing

### APPLICATIONS

- Serial Data Acquisition and Process control
- Communication Systems
- Automotive and Avionics Systems
- ATE

### DESCRIPTION

The DG480 is an analog switch array configured as an 8-channel multiplexer for use in serial input data applications. Combining low ON resistance ( $r_{DS(ON)} < 100 \Omega$ ) and fast switching ( $t_{OFF} < 200$  ns) the DG480 is ideally suited for data acquisition, process control, communication, and avionic applications. Any, all or none of the 8 switches may be closed at any given time.

This device loads the input data serially into the input shift register with each clock pulse. The state of the shift register can be latched via LD at any point into an address register which holds the logic function to control the array. An  $\overline{RS}$  pin resets all the latches to a LOW condition. A serial output terminal  $D_{OUT}$  allows chaining of arrays for larger

matrix systems.

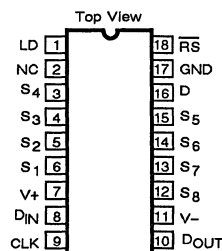
The DG480 is built on Siliconix high voltage silicon gate process to achieve high voltage ratings and superior switch ON/OFF performance. An epitaxial layer prevents latchup.

Each channel conducts equally well in either direction when ON and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full  $\pm 15$  V analog range, rivaling JFET performance without the inherent dynamic range limitation.

Packaging for the DG480 consists of the 18-pin CerDIP and plastic DIP packages. Temperature ranges available are military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ).

### PIN CONFIGURATION

Dual-In-Line Package

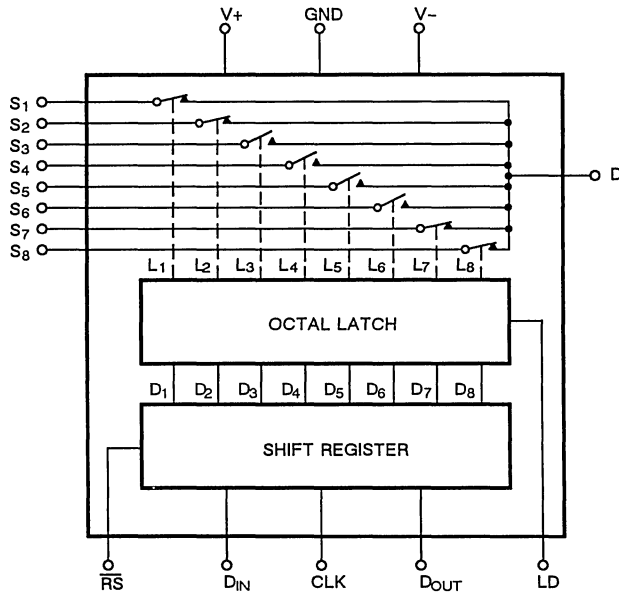


Order Numbers:

CerDIP: DG480AK, DG480AK/883

Plastic: DG480DJ

**FUNCTIONAL BLOCK DIAGRAM**



**TRUTH TABLES**

$\overline{RS}$	CLK*	D <sub>IN</sub>	D <sub>1</sub>	D <sub>N</sub>
1		0	0	D <sub>N-1</sub>
1		1	1	D <sub>N-1</sub>
1		X	D <sub>1</sub>	D <sub>N</sub> (NO CHANGE)
0	X	X	0	0

LD*	D <sub>N</sub>	L <sub>N</sub>	SW <sub>N</sub>
	0	0	OFF
	1	1	ON
	D <sub>N</sub>	L <sub>N</sub>	(NO CHANGE)

\*CLK and LD Inputs are Level Triggered

**ABSOLUTE MAXIMUM RATINGS**

V+ to V- ..... 44 V  
 GND to V- ..... 25 V  
 Digital Inputs V<sub>S</sub>, V<sub>D</sub><sup>1</sup> ..... (V-) -2 V to (V+)+ 2 V  
 ..... or 30 mA, whichever occurs first  
 Continuous Current (Any Terminal) ..... 30 mA  
 Current, S or D (Pulsed 1 ms, 10% duty cycle) .. 100 mA  
 Storage Temperature (A Suffix) ..... -65 to 150°C  
 (D Suffix) ..... -65 to 125°C  
 Operating Temperature (A Suffix) ..... -55 to 125°C  
 (D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*  
 18-Pin CerDIP\*\* ..... 600 mW  
 18-Pin Plastic DIP\*\*\* ..... 470 mW

\* All leads welded or soldered to PC Board.  
 \*\* Derate 9.2 mW/°C above 75°C.  
 \*\*\* Derate 16.5 mW/°C above 25°C.

<sup>1</sup> Signals on S<sub>x</sub>, D<sub>x</sub>, or I<sub>Nx</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

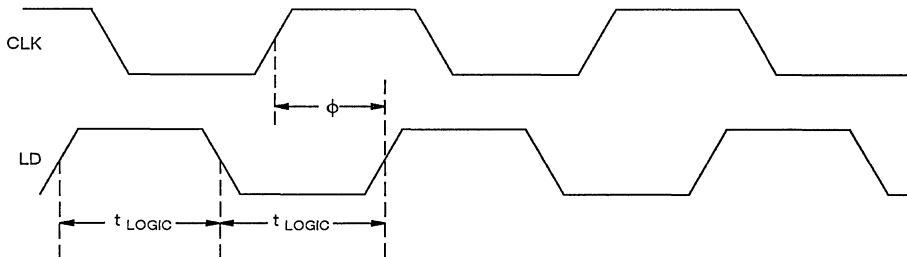
ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}, V_- = -15\text{ V}$ $GND = 0\text{ V}$ $V_{IN} = 2.0\text{ V}, 0.8\text{ V}^e$	LIMITS						UNIT	
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$					-15	15	-15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -10\text{ mA}, V_D = \pm 10\text{ V}$ $V_+ = 13.5\text{ V}, V_- = -13.5\text{ V}$	1,3 2				75 100		75 100	$\Omega$
Delta Drain-Source ON Resistance	$\Delta r_{DS(ON)}$	$\Delta r_{DS(ON)} = \frac{r_{DS(ON) MAX} - r_{DS(ON) MIN}}{r_{DS(ON) AVG}}$	1				10		10	%
Switch OFF Leakage Current	$I_{S(OFF)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_D = -14\text{ V}, V_S = 14\text{ V}$	1 2			-1 -20	1 20	-1 -20	1 20	nA
	$I_{D(OFF)}$	$V_D = 14\text{ V}, V_S = -14\text{ V}$	1 2			-10 -200	10 200	-10 -200	10 200	
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_+ = 16.5\text{ V}, V_- = -16.5\text{ V}$ $V_S = V_D = \pm 14\text{ V}$	1 2			-20 -500	20 500	-20 -500	20 500	
<b>INPUT</b>										
Input Current with $V_{IN}$ Low	$I_{IL}$	$V_{IN}$ under test = 0.8 V all other = 2.0 V	1 2			-1 -5	1 5	-1 -5	1 5	$\mu\text{A}$
Input Current with $V_{IN}$ High	$I_{IH}$	$V_{IN}$ under test = 2.0 V all other = 0.8 V	1 2			-1 -5	1 5	-1 -5	1 5	
<b>OUTPUT</b>										
Output Voltage with $V_{IN}$ Low - SO	$V_{OL}$	$V_{IN}$ under test = 0.8 V all other = 2.4 V	1,2				0.4		0.4	V
<b>DYNAMIC</b>										
Pulse Width for Logic	$t_{LOGIC}$	( $D_{IN}, LD, CLK, \overline{RS}$ ) See Figure	1 2			80 150		80 150		ns
Transition Time	$t_{TRAN}$	$R_L = 1\text{ M}\Omega, C_L = 35\text{ pF}$ $V_{S1} = 10\text{ V}, V_{S2} = -10\text{ V}$ 50% of $V_{LD}$ to 90% of $V_D$ See Figure	1 2				200 250		200 250	
Data Setup Time	$t_{DW}$		1			50		50		
Break-Before-Make	$t_{BREAK}$	$R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 10\text{ V}$ 90% of $V_D$ to 90% of $V_D$ See Figure	1 2			10 20		10 20		
Turn-ON Time	$t_{ON}$	50% of LD, $\overline{RS}$ to 90% of $V_D$ $R_L = 1\text{ k}\Omega, C_L = 35\text{ pF}$ See Figure 1A	1 2				200 250		200 250	
Turn-OFF Time	$t_{OFF}$		1 2				150 200		150 200	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.0 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
Charge Injection	Q	V <sub>S</sub> = 0 V, C <sub>L</sub> = 1000 pF	1	40					pC
OFF Isolation		R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	1	-65					dB
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω f = 1 MHz	1	7					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		1	55					
Drain and Source ON Capacitance	C <sub>S(ON)</sub> + C <sub>D(ON)</sub>		1	200					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0 or 5 V	1,2,3			100		100	μA
Negative Supply Current	I <sub>-</sub>		1,2,3		-1		-1		
Ground Current	I <sub>GND</sub>		1,2,3		-100		-100		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = input voltage to perform proper function.

**INPUT TIMING REQUIREMENTS**

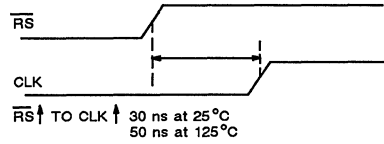
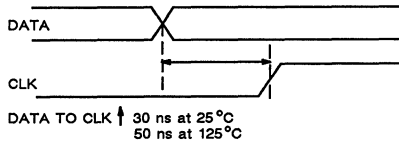


φ = for CLK and LD inputs of the same frequency  
The recommended phase delay of LD from CLK is 1/2 t<sub>LOGIC</sub> to t<sub>LOGIC</sub>

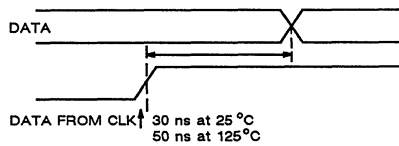
t<sub>LOGIC</sub>(MIN) : 80 ns at 25°C      V<sub>+</sub> = +15 V  
150 ns at 125°C                  V<sub>-</sub> = -15 V  
GND = 0 V

## INPUT TIMING REQUIREMENTS (Cont'd)

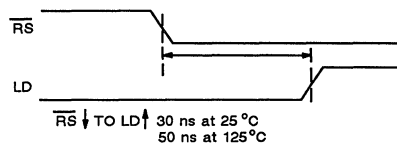
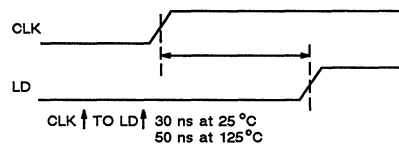
### SHIFT REGISTER SETUP



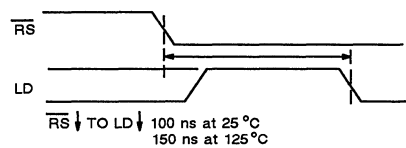
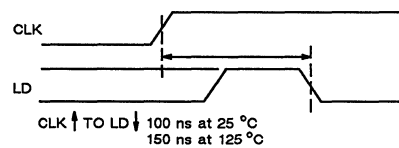
### SHIFT REGISTER HOLD



### ADDRESS REGISTER SETUP

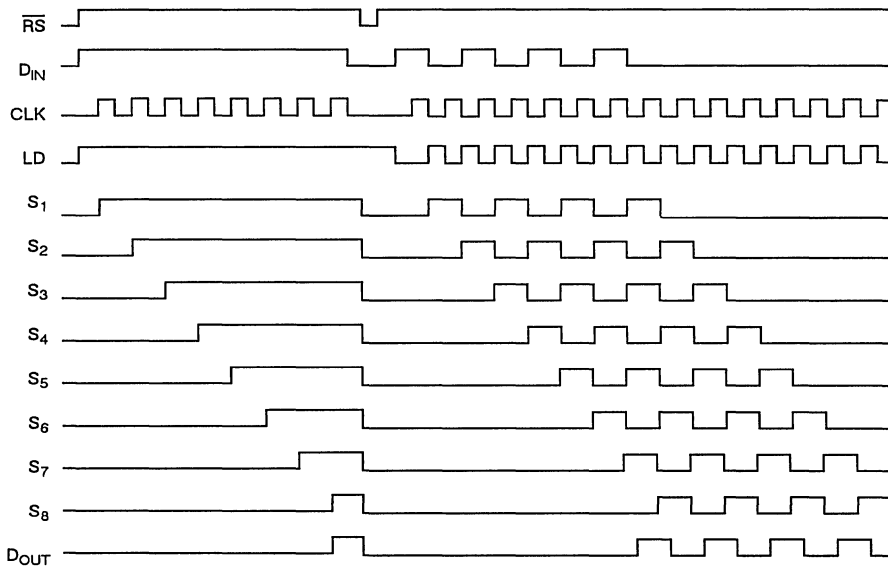


### ADDRESS REGISTER ENABLE



V<sub>+</sub> = +15 V, V<sub>-</sub> = -15 V, GND = 0 V  
INPUTS ARE 0 V TO 3 V

**TIMING DIAGRAM**



S<sub>1</sub>-S<sub>8</sub> and D<sub>OUT</sub> are expected output with the drain connected high.  
The sources require pull-downs of 1 k $\Omega$ .

## Low-Power – High-Speed CMOS Octal Analog Switch Array

### FEATURES

- $\pm 15$  Volt Input Range
- ON Resistance  $< 100 \Omega$
- Serial Data Input/Output
- Low Power ( $P_D < 35 \mu W$ )
- TTL and CMOS Compatible
- Any Combination of 8 SPST to the Output
- ESDS Protection  $> \pm 4000$  V

### BENEFITS

- Low Signal Distortion
- Reduced Switch Errors
- Devices Can Be Chained For System Expansion
- Reduced Power Supply
- Simple Interfacing

### APPLICATIONS

- Audio Switching and Routing
- Precision Switching
- Serial Data Acquisition and Process Control
- Battery and Remote Systems
- Automotive, Avionics and ATE Systems

### DESCRIPTION

The DG485 is an analog switch array configured as a low power 8-channel multiplexer for use in serial input applications. Combining low ON resistance ( $r_{DS(ON)} < 100 \Omega$ ) and fast switching ( $t_{OFF} < 200$  ns), the DG485 is ideally suited for data acquisition, process control, communication, and avionic applications. Any, all or none of the 8 switches may be closed at any given time.

This device loads the input data serially into the input shift register with each clock pulse. The state of the shift register can be latched via LOAD at any point into an address register which holds the logic function to control the array. An  $\overline{RS}$  pin resets all latch inputs to a LOW condition. A serial output

terminal ( $D_{OUT}$ ) allows chaining of arrays for larger matrix systems.

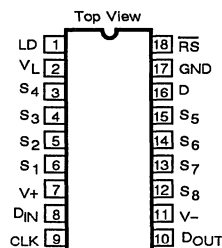
Built on the Siliconix high voltage silicon gate process the DG485 has a wide 44 V range. An epitaxial layer prevents latchup.

Each channel conducts equally well in either direction when ON and blocks up to 30 volts peak-to-peak when OFF. ON resistance is very flat over the full  $\pm 15$  V analog range, rivaling JFET performance without the inherent dynamic range limitation.

Packaging for the DG485 consists of the 18-pin CerDIP and plastic DIP. Temperature ranges available are military, A suffix ( $-55$  to  $125^\circ C$ ) and industrial, D suffix ( $-40$  to  $85^\circ C$ ).

### PIN CONFIGURATION

Dual-In-Line Package



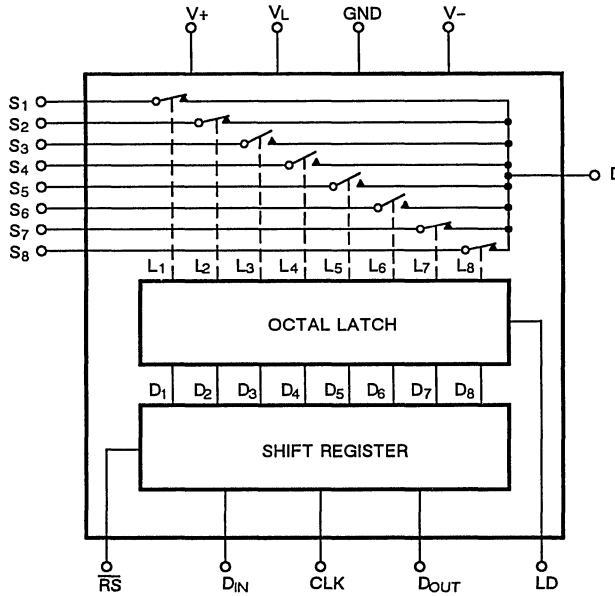
Order Numbers:

CerDIP: DG485AK, DG485AK/883

Plastic: DG485DJ



**FUNCTIONAL BLOCK DIAGRAM**



**TRUTH TABLE**

$\overline{RS}$	CLK*	D <sub>IN</sub>	D <sub>1</sub>	D <sub>N</sub>
1		0	0	D <sub>N-1</sub>
1		1	1	D <sub>N-1</sub>
1		X	D <sub>1</sub>	D <sub>N</sub> (NO CHANGE)
0	X	X	0	0

LD*	D <sub>N</sub>	L <sub>N</sub>	SW <sub>N</sub>
	0	0	OFF
	1	1	ON
	D <sub>N</sub>	L <sub>N</sub>	(NO CHANGE)

\*CLK and LD Inputs are Level Triggered

**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to V-

- V+ ..... 44 V
- GND ..... 25 V
- Digital Inputs V<sub>S</sub>, V<sub>D</sub><sup>1</sup> ..... (V-) -2 V to (V+) + 2 V  
..... or 30 mA, whichever occurs first
- Continuous Current (Any Terminal) ..... 30 mA
- Current, S or D (Pulsed 1 ms, 10% duty cycle) .. 100 mA
- Storage Temperature (A Suffix) ..... -65 to 150°C  
(D Suffix) ..... -65 to 125°C

- Operating Temperature (A Suffix) ..... -55 to 125°C  
(D Suffix) ..... -40 to 85°C

- Power Dissipation (Package) \*  
18-Pin CerDIP\*\* ..... 600 mW  
18-Pin Plastic DIP\*\*\* ..... 470 mW

- \* All leads welded or soldered to PC Board.
- \*\* Derate 9.2 mW/°C above 75°C.
- \*\*\* Derate 16.5 mW/°C above 25°C.

- 1 Signals on S<sub>x</sub>, D<sub>x</sub>, or I<sub>Nx</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.0 V, 0.8 V <sup>e</sup>	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C			
			2=125,85°C		3=-55,-40°C					
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>					-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±10 V V <sub>+</sub> = 13.5 V, V <sub>-</sub> = -13.5 V	1,3 2				75 100		75 100	Ω
Delta Drain-Source ON Resistance	Δr <sub>DS(ON)</sub>	$\frac{\Delta r_{DS(ON)}}{r_{DS(ON) MAX} - r_{DS(ON) MIN}}$ r <sub>DS(ON) AVG</sub>	1				10		10	%
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>D</sub> = -15.5 V, V <sub>S</sub> = 15.5 V	1 2			-1 -20	1 20	-1 -20	1 20	nA
	I <sub>D(OFF)</sub>	V <sub>D</sub> = 15.5 V, V <sub>S</sub> = -15.5 V	1 2			-10 -200	10 200	-10 -200	10 200	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>S</sub> = V <sub>D</sub> = ±15.5 V	1 2			-20 -500	20 500	-20 -500	20 500	
<b>INPUT</b>										
Input Current with V <sub>IN</sub> Low	I <sub>IL</sub>	V <sub>IN</sub> under test = 0.8 V all other = 2.4 V	1 2			-1 -5	1 5	-1 -5	1 5	μA
Input Current with V <sub>IN</sub> High	I <sub>IH</sub>	V <sub>IN</sub> under test = 2.4 V all other = 0.8 V	1 2			-1 -5	1 5	-1 -5	1 5	
<b>SERIAL DATA OUTPUT</b>										
Output Voltage with V <sub>IN</sub> Low - D <sub>OUT</sub>	V <sub>OL</sub>	I <sub>O</sub> = 3.2 mA, V <sub>+</sub> = 4.5 V	1,2				0.4		0.4	V
Output Voltage with V <sub>IN</sub> High - D <sub>OUT</sub>	V <sub>OH</sub>	I <sub>O</sub> = -160 μA V <sub>+</sub> = 22 V, V <sub>L</sub> = 4.75 V	1,2			2.7		2.7		
<b>DYNAMIC</b>										
Pulse Width for Logic	t <sub>LOGIC</sub>	( D <sub>IN</sub> , LD, CLK, RS ) See Figure	1 2			80 150		80 150		ns
Transistion Time	t <sub>TRAN</sub>	R <sub>L</sub> = 1 M, C <sub>L</sub> = 35 pF V <sub>S1</sub> = 10 V, V <sub>S2</sub> = -10 V 50% of V <sub>LD</sub> to 90% of V <sub>D</sub> See Figure	1 2				200 250		200 250	
Data Setup Time	t <sub>DW</sub>		1			50		50		
Break-Before-Make	t <sub>BREAK</sub>	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF V <sub>S1</sub> = V <sub>S2</sub> = 10 V 90% of V <sub>LD</sub> to 90% of V <sub>D</sub> See Figure	1 2			10 20		10 20		

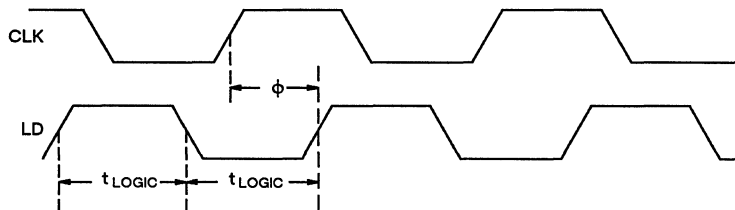
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V, GND = 0 V V <sub>IN</sub> = 2.0 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
Turn-ON Time	t <sub>ON</sub>	50% of LD, $\overline{RS}$ to 90% of V <sub>D</sub> R <sub>L</sub> = 1 k $\Omega$ , C <sub>L</sub> = 35 pF See Figure 1A	1			200		200	ns
			2			250		250	
Turn-OFF Time	t <sub>OFF</sub>		1			150		150	
			2			200		200	
Charge Injection	Q	V <sub>S</sub> = 0 V, C <sub>L</sub> = 1000 pF	1			60		60	pC
OFF Isolation <sup>c</sup>		R <sub>L</sub> = 50 $\Omega$ , C <sub>L</sub> = 5 pF f = 1 MHz	1	-65					dB
Source-OFF Capacitance <sup>c</sup>	C <sub>S(OFF)</sub>	V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 $\Omega$ f = 1 MHz	1	7					pF
Drain-OFF Capacitance <sup>c</sup>	C <sub>D(OFF)</sub>		1	55					
Drain and Source ON Capacitance <sup>c</sup>	C <sub>S(ON)</sub> + C <sub>D(ON)</sub>		1	200					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0 or 5 V V <sub>L</sub> = 5.25 V	1,2			1		1	$\mu$ A
Negative Supply Current	I <sub>-</sub>		1,2		-1		-1		
Logic Supply Current	I <sub>L</sub>		1,2			1		1	
Ground Current	I <sub>GND</sub>		1,2		-1		-1		

**NOTES:**

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- V<sub>IN</sub> = Input voltage to perform proper function.

**5**

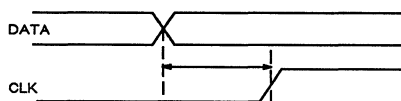
## INPUT TIMING REQUIREMENTS



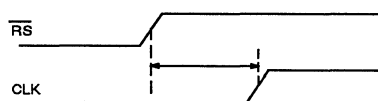
$\phi$  = for CLK and LD inputs of the same frequency  
The recommended phase delay of LD from CLK  
is  $1/2 t_{\text{LOGIC}}$  to  $t_{\text{LOGIC}}$

$t_{\text{LOGIC}}(\text{MIN})$ : 80 ns at 25°C	V+ = +15 V
150 ns at 125°C	V- = -15 V
	GND = 0 V

### SHIFT REGISTER SETUP

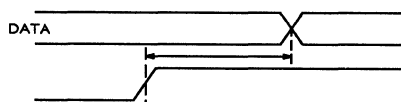


DATA TO CLK  $\uparrow$  30 ns at 25°C  
50 ns at 125°C



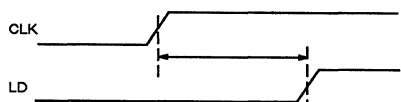
$\overline{\text{RS}}$   $\uparrow$  TO CLK  $\uparrow$  30 ns at 25°C  
50 ns at 125°C

### SHIFT REGISTER HOLD

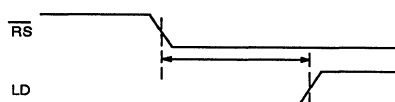


DATA FROM CLK  $\uparrow$  30 ns at 25°C  
50 ns at 125°C

### ADDRESS REGISTER SETUP

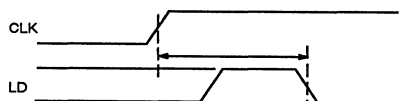


CLK  $\uparrow$  TO LD  $\uparrow$  30 ns at 25°C  
50 ns at 125°C

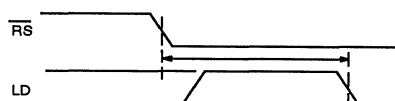


$\overline{\text{RS}}$   $\downarrow$  TO LD  $\uparrow$  30 ns at 25°C  
50 ns at 125°C

### ADDRESS REGISTER ENABLE



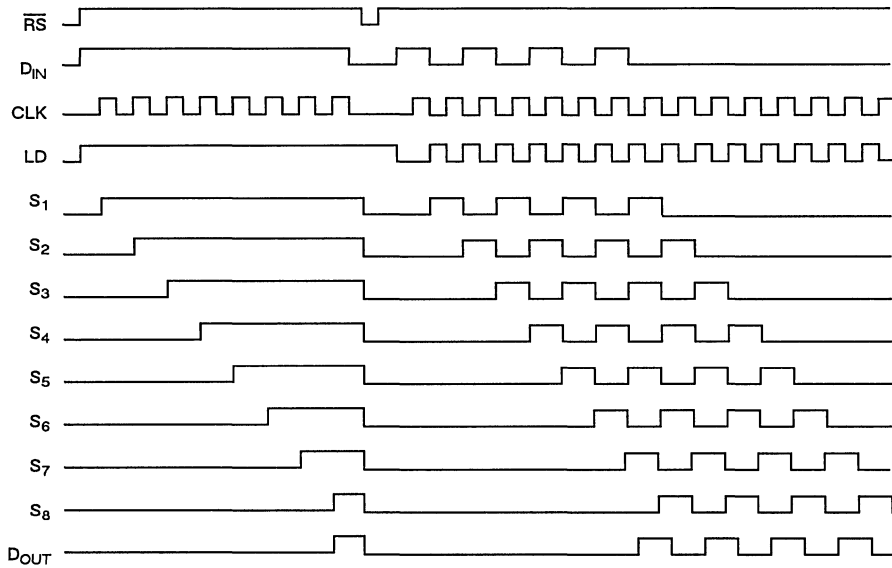
CLK  $\uparrow$  TO LD  $\downarrow$  100 ns at 25°C  
150 ns at 125°C



$\overline{\text{RS}}$   $\downarrow$  TO LD  $\downarrow$  100 ns at 25°C  
150 ns at 125°C

V+ = +15 V, V- = -15 V, GND = 0 V  
INPUTS ARE 0 V TO 3 V

**TIMING DIAGRAM**



S<sub>1</sub>–S<sub>8</sub> and D<sub>OUT</sub> are expected output with the drain connected high.  
The sources require pull-downs of 1 kΩ .

# DG501

## 8-Channel Multiplex Switch with Decode

### FEATURES

- Break-Before-Make Switching
- Pull-Up Resistors on Inputs
- Bi-Directional Signal Handling

### BENEFITS

- Reduced System Cross-Talk
- Easily Interfaced to TTL

### APPLICATIONS

- Multiplexing  $\pm 5$  V Analog Signals
- Data Acquisition Systems

### DESCRIPTION

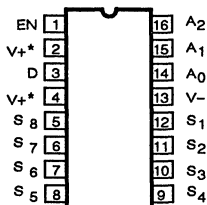
Designed for applications where single-ended, Break-Before-Make switching action is required, the DG501 is an 8-channel analog multiplexer that is capable of handling bi-directional signals up to  $\pm 5$  V. In addition, an "OFF" state can be activated by using a chip enable signal. In the OFF state, this device can block up to 10 V peak-to-peak signals. An on-chip decoder accepts a 3 bit binary word

which enables the selection of any one of the eight analog switches to be turned on individually. Pull-up resistors are provided at each logic input to simplify TTL interface. This device is available in either a 16-pin plastic or ceramic DIP and is available in commercial, C suffix (0 to 70°C), industrial, B suffix (-25 to 85°C) and military, A suffix (-55 to 125°C) temperature ranges.

### PIN CONFIGURATION

### TRUTH TABLE

Dual-In-Line Package



Top View

Order Numbers:

Slide Braze: DG501AP, DG501BP,

Plastic: DG501CJ

LOGIC INPUTS				CHANNEL
A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	EN	'ON'
L	L	L	H	S <sub>1</sub>
H	L	L	H	S <sub>2</sub>
L	H	L	H	S <sub>3</sub>
H	H	L	H	S <sub>4</sub>
L	L	H	H	S <sub>5</sub>
H	L	H	H	S <sub>6</sub>
L	H	H	H	S <sub>7</sub>
H	H	H	H	S <sub>8</sub>
X	X	X	L	OFF

Logic Levels\*

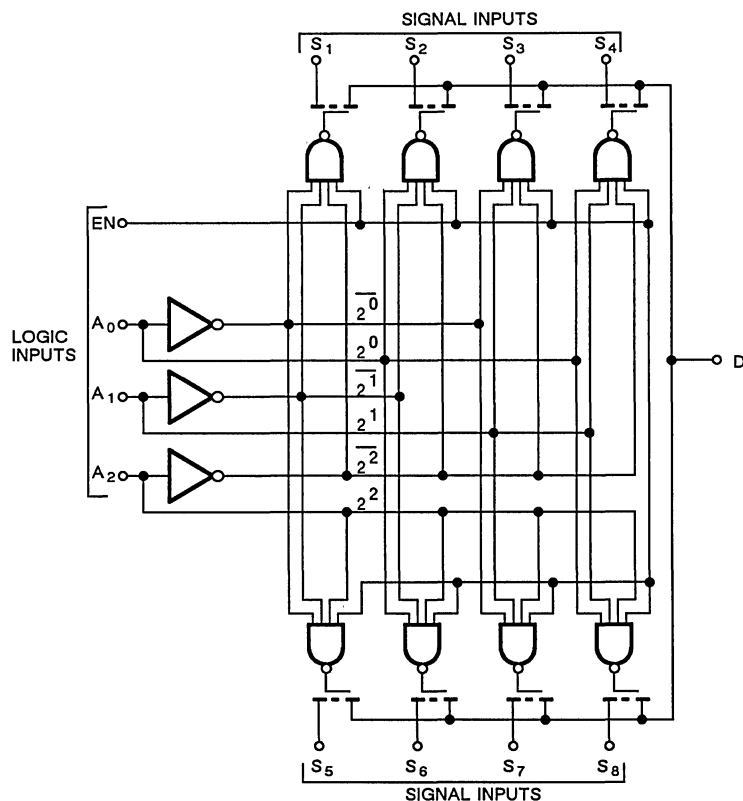
LOW:  $V_L = V_{LOW} < 0.6$  V

HIGH:  $V_H = V_{HIGH} > 3.5$  V

\* Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

\* For supply voltages of 5 V and -20 V

**FUNCTION BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

V+ to V-	30 V
V- to V+	-0.3 V
V+ to VA, VEN	30 V
VA, VEN to V+	-0.3 V
V+ to VD or VS	30 V
VD VS to V+	-0.3 V
VD to VS	±25 V
VA, VEN to V-	30 V
VD or VS to V-	30 V
Current, (Any Terminal)	-20 mA

Storage Temperature (A & B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C

Power Dissipation*	
16-Pin Ceramic DIP**	900 mW
16-Pin Plastic DIP***	470 mW

\* Device mounted with all leads welded or soldered to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 5\text{ V}$ , $V_- = -20\text{ V}$ $V_{EN} = 3.5\text{ V}$ $V_{AL} = 0.6\text{ V}$ $V_{AH} = 3.5\text{ V}$			LIMITS						UNIT
					1=25°C		A SUFFIX		B, C SUFFIX		
					TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$			1,2,3		-5	5	-5	5	V	
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -100\ \mu\text{A}$ $V_- = -15\text{ V}$	$V_D = 5\text{ V}$	1,3 2	75		200 300		200 300	$\Omega$	
			$V_D = 0\text{ V}$	1,3 2	97		250 375		250 350		
			$V_D = -5\text{ V}$	1,3 2	140		600 900		800 900		
		$I_S = -1\text{ mA}$ $V_- = -20\text{ V}$	$V_D = 5\text{ V}$	1,3 2	65		150 225		150 200		
			$V_D = 0\text{ V}$	1,3 2	80		200 300		200 300		
			$V_D = -5\text{ V}$	1,3 2	100		250 375		250 350		
Source OFF Leakage Current	$I_{S(OFF)}$	$V_S = -5\text{ V}$ , $V_D = 5\text{ V}$ $V_{EN} = 0.6\text{ V}$	1 2	-0.005	-1 -1000		-3 -150		nA		
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_D = -5\text{ V}$ , $V_S = 5\text{ V}$ $V_{EN} = 0.6\text{ V}$	1 2	-0.07	-8 -4000		-10 -500				
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_D = V_S = 5\text{ V}$	1 2	0.1		8 4000		10 500			
<b>INPUT</b>											
Logic Input Current Input Voltage LOW	$I_{INL}$	$V_{AL} = 0$	1	0.8	-1.2		-1.2		mA		
Logic Input Current Input Voltage HIGH	$I_{INH}$	$V_{AH} = 3.5\text{ V}$	1			-150		-150	$\mu\text{A}$		
<b>DYNAMIC</b>											
Switching Time	$t_{TRANS}$	See Switching Time Test Circuit $V_{S1} = \pm 1\text{ V}$ $V_{S8} = \mp 1\text{ V}$ $V_{S2}$ thru $V_{S7} = 0\text{ V}$	$V_- = -20\text{ V}$	1			1.5		2	$\mu\text{s}$	
			$V_- = -15\text{ V}$	1			2.5		3		
Break-Before-Make Interval	$t_{OPEN}$	See Switching Time Test Circuit $V_{S(A11)} = 1\text{ V}$	1	0.05						$\mu\text{s}$	
Turn-ON Time	$t_{ON}$		1	1.2							
Turn-OFF Time	$t_{OFF}$		1	0.8							

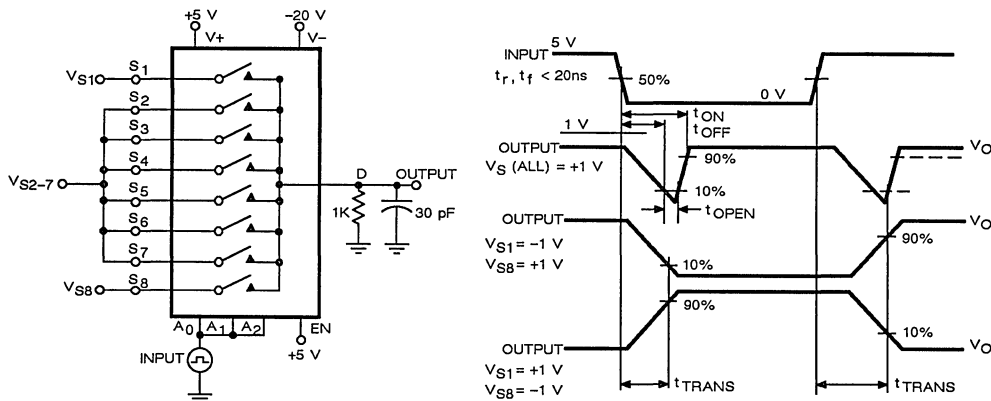


ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 5 V, V <sub>-</sub> = -20 V V <sub>EN</sub> = 3.5 V V <sub>AL</sub> = 0.6 V V <sub>AH</sub> = 3.5 V	LIMITS				UNIT		
			1=25°C		A SUFFIX			B, C SUFFIX	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		MIN <sup>b</sup>	MAX <sup>b</sup>
<b>DYNAMIC (Cont'd)</b>									
Turn-ON Time	t <sub>ON</sub>	See Switching Time Test Circuit V <sub>S(All)</sub> = 1 V V <sub>-</sub> = -15 V	1	2			μs		
Turn-OFF Time	t <sub>OFF</sub>		1	0.8					
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = V <sub>D</sub> = 5 V V <sub>EN</sub> = 0.6 V f = 1 MHz	1	10			pF		
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		1	20					
<b>SUPPLY</b>									
Drain Supply Current	I <sub>-</sub>	V <sub>EN</sub> = 0 V V <sub>AL(All)</sub> = 0 V	1	-2.6	-6		mA		
Source Supply Current	I <sub>+</sub>		1	5.6		8		8	
Drain Supply Current	I <sub>-</sub>	V <sub>EN</sub> = 3.5 V V <sub>AL(All)</sub> = 0 V	1	-2.4	-6		mA		
Source Supply Current	I <sub>+</sub>		1	4.9		7		7	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**SWITCHING TIME TEST CIRCUIT**



## APPLICATION HINTS\*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>EN</sub> Enable Input Voltage Min High/ Max Low (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
5**	-20	3.5/0.6	3.5/0.6	-5 to 5
5	-15	3.5/0.6	3.5/0.6	-5 to 5

\* Application Hints are for DESIGN AID ONLY, and not guaranteed and not subject to production testing.

\*\*Electrical parameters chart based on V+ = 5 V, V- = -20 V.

# 8-Channel Multiplex Switch with Decode

## FEATURES

- $\pm 10$  V Input Signal Range
- Break-Before-Make Switching
- Bi-directional Signal Handling

## BENEFITS

- Reduced System Crosstalk

## APPLICATIONS

- Data Acquisition
- Multiplexing Signals

## DESCRIPTION

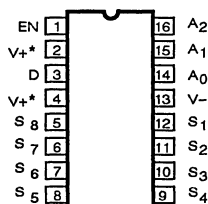
Designed for applications where single-ended, Break-Before-Make switching action is required, the DG503 is an 8-channel PMOS analog multiplexer that is capable of handling bi-directional signals up to  $\pm 10$  V. In addition, an "OFF" state can be activated by using a chip-enable signal. In the OFF state the device can block up to 20 V peak-to-peak signals. An on-chip decoder accepts a 3-bit binary

word which enables the selection of any one of eight analog switches to be turned on individually. Pull-up resistors are provided at each logic input to simplify TTL compatibility.

DG503 is available in a 16-pin plastic or ceramic DIP. Performance grades include the commercial, C suffix (0 to 70°C) and the military, A suffix (-55 to 125°C) temperature grades.

## PIN CONFIGURATION

Dual-In-Line Package



Top View

Order Numbers:  
Side Braze: DG503AP  
Plastic: DG503CJ

## TRUTH TABLE

LOGIC INPUTS				CHANNEL
A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	EN	'ON'
L	L	L	H	S <sub>1</sub>
H	L	L	H	S <sub>2</sub>
L	H	L	H	S <sub>3</sub>
H	H	L	H	S <sub>4</sub>
L	L	H	H	S <sub>5</sub>
H	L	H	H	S <sub>6</sub>
L	H	H	H	S <sub>7</sub>
H	H	H	H	S <sub>8</sub>
X	X	X	L	OFF

Logic Levels\*

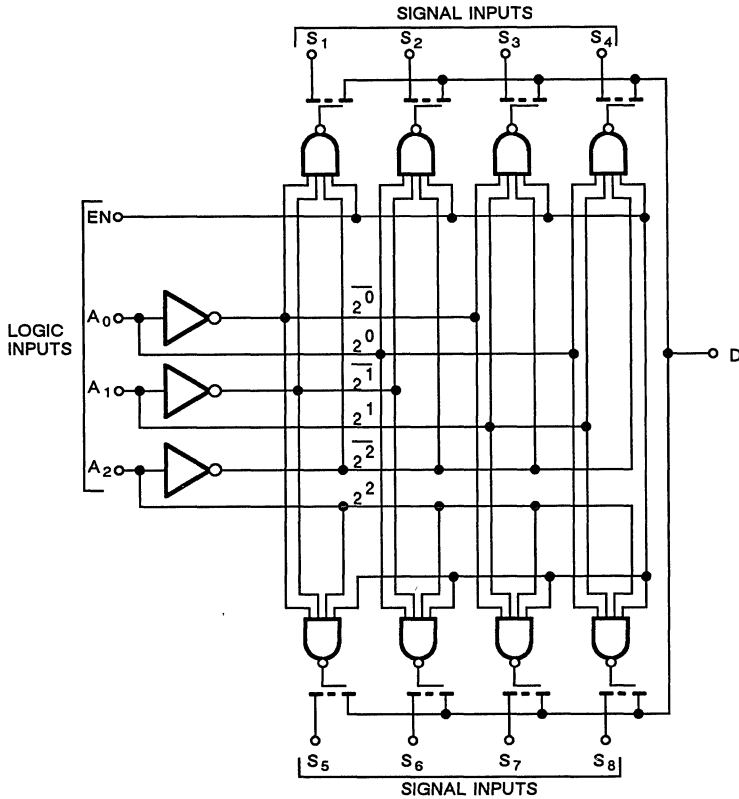
LOW:  $V_L = V_{LOW} \leq 0.6$  V

HIGH:  $V_H = V_{HIGH} \geq 8.5$  V

\* Both V+ lines are internally connected, either one or both may be used. V+ common to substrate.

\* For supply voltages of 10 V and -20 V

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

$V_+$ to $V_-$ .....	-0.3, 33 V
$V_+$ to $V_A, V_{EN}$ .....	-0.3, 33 V
$V_+$ to $V_D$ or $V_S$ .....	-0.3, 33 V
$V_D$ to $V_S$ .....	$\pm 25$ V
$V_A, V_{EN}$ to $V_-$ .....	33 V
$V_D$ or $V_S$ to $V_-$ .....	33 V
Current (Any Terminal) .....	-20 mA
Storage Temperature (A Suffix) .....	-65 to 150°C
(C Suffix) .....	-65 to 125°C

Operating Temperature (A Suffix) .....	-55 to 125°C
(C Suffix) .....	0 to 70°C

### Power Dissipation\*

16-Pin Side brazed DIP** .....	900 mW
16-Pin Plastic DIP*** .....	470 mW

All leads soldered or welded to PC board.

\* Derate 12 mW/°C above 75°C.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V V <sub>EN</sub> = 8.5 V V <sub>AL</sub> = 0.6 V V <sub>AH</sub> = 8.5 V GND = 0		LIMITS						UNIT
				1=25°C		A SUFFIX 2=125,85,70°C 3=-55,-25,0°C		C SUFFIX 0 to 70°C		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>			1,2,3		-10	10	-10	10	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -100 μA	V <sub>D</sub> = -10 V	1,3 2			800 1250		800 1000	Ω
			V <sub>D</sub> = 10 V	1,3 2		150 225		150 200		
		I <sub>S</sub> = -1 mA	V <sub>D</sub> = 0 V	1,3 2		250 375		250 350		
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>EN</sub> = 0.6 V	V <sub>D</sub> = 10 V V <sub>S</sub> = -10 V	1 2		-2 -2000	2 2000	-3 -150	3 150	nA
Drain OFF Leakage Current	I <sub>D(OFF)</sub>		V <sub>D</sub> = -10 V V <sub>S</sub> = 10 V	1 2		-8 -4000	8 4000	-10 500	10 500	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	Sequence Each Switch ON V <sub>D</sub> = V <sub>S</sub> = 10 V		1 2		-8 -4000	8 4000	-10 -500	10 500	
<b>INPUT</b>										
Logic Input Current Input Voltage LOW	I <sub>INL</sub>	V <sub>A</sub> = 0 V		1		-1		-1		μA
<b>DYNAMIC</b>										
Switching Time of Multiplexer	t <sub>TRANS</sub>	See Switching Time Test Circuit V <sub>S1</sub> = ±1 V, V <sub>S8</sub> = ∓1 V V <sub>S2</sub> thru V <sub>S7</sub> = 0 V		1			1.5		2.0	μs
Break-Before-Make Interval	t <sub>OPEN</sub>	See Switching Time Test Circuit V <sub>S(A11)</sub> = ±1 V		1	0.05					μs
Turn-ON Time	t <sub>ON</sub>			1	1.2					
Turn-OFF Time	t <sub>OFF</sub>			1	0.8					
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V V <sub>EN</sub> = 0.5 V f = 1 MHz		1	5					pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>			1	20					
<b>SUPPLY</b>										
Drain Supply Current	I <sub>-</sub>	V <sub>EN</sub> = 0 V		1	-2.6	-6		-6		mA
Source Supply Current	I <sub>+</sub>			1	5.6		8		8	

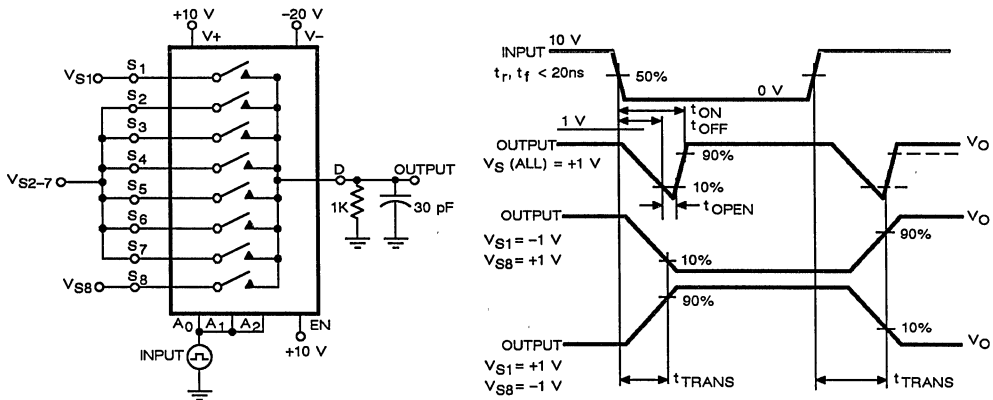
5

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 10 V, V <sub>-</sub> = -20 V V <sub>EN</sub> = 8.5 V V <sub>AL</sub> = 0.6 V V <sub>AH</sub> = 8.5 V GND = 0	LIMITS						UNIT
			1=25°C		A SUFFIX 2=125,85,70°C		C SUFFIX 3=-55,-25,0°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY (Cont'd)</b>									
Drain Supply Current	I <sub>-</sub>	V <sub>EN</sub> = 8.5 V V <sub>AL(All)</sub> = 0 V	1	-2.4	-6		-6		mA
Source Supply Current	I <sub>+</sub>		1	4.9		7		7	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**SWITCHING TIME TEST CIRCUIT**



**APPLICATION HINTS\***

V <sub>+</sub> Positive Supply Voltage (V)	V <sub>-</sub> Negative Supply Voltage (V)	V <sub>EN</sub> Enable Input Voltage Min High/ Max Low (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
10**	-20	8.5/0.6	8.5/0.6	-10 to 10
5	-20	3.5/0.6	3.5/0.6	-10 to 5
10	-15	8.5/0.6	8.5/0.6	-5 to 10
5	-15	3.5/0.6	3.5/0.6	-5 to 5

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

\*\*Electrical parameters chart based on V<sub>+</sub> = 10 V, V<sub>-</sub> = -20 V.

## 16-Channel and Dual 8-Channel CMOS Analog Multiplexers

### FEATURES

- TTL & CMOS Direct Control Over Military Temperature Range
- Low Power (30 mW typ.)
- Break-Before-Make Switching
- 44 V Power Supply Rating

### BENEFITS

- Easily Interfaced
- Reduced Power Consumption
- Reduced System Cross-Talk
- Environmentally Rugged

### APPLICATIONS

- Communication Systems
- Multiplexing Reference Signals
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing

### DESCRIPTION

DG506A and DG507A are 16- and dual 8-channel analog multiplexers, respectively, designed for selecting 1 of 16 (or 8) analog input signals and connecting it to a common output or, conversely, routing an analog signal to 1 of 16 (or 8) output loads. Break-before-make switching action protects against momentary shorting of the input signals.

The DG506A, an 16-channel single-ended analog multiplexer, is designed to connect 1 of 16 inputs to a common output as determined by a 4-bit binary address ( $A_0, A_1, A_2, A_3$ ). DG507A, a dual 8-channel analog multiplexer, is designed to connect 1 of 8 dual inputs to a common dual output as determined by its 3 bit binary address ( $A_0, A_1, A_2$ ) logic.

A channel in the ON state conducts current equally well in both directions (bidirectional switches). In the OFF state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF. All

control inputs, address ( $A_X$ ) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

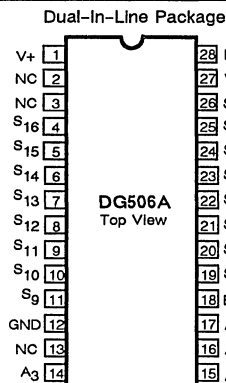
Designed in the Siliconix PLUS-40 process, the absolute maximum voltage rating is extended to 44 Volts, allowing increased operating headroom for standard  $\pm 15$  V signal swings and operation with  $\pm 20$  V supplies. An epitaxial layer prevents latch up.

Both DG506A and DG507A are available in dual-in-line ceramic and plastic packages, and are specified for operation over the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ), industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ), and commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ), temperature ranges.

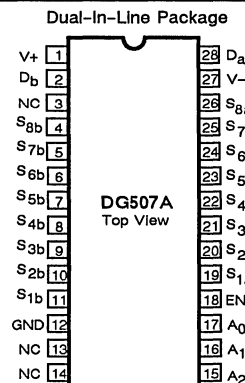
For applications requiring address data latching, the DG528/DG529 is recommended. For wideband/ video routing and multiplexing applications, the DG536 is recommended.

For more information, refer to Siliconix Application Note AN75-1 and AN73-2.

### PIN CONFIGURATION

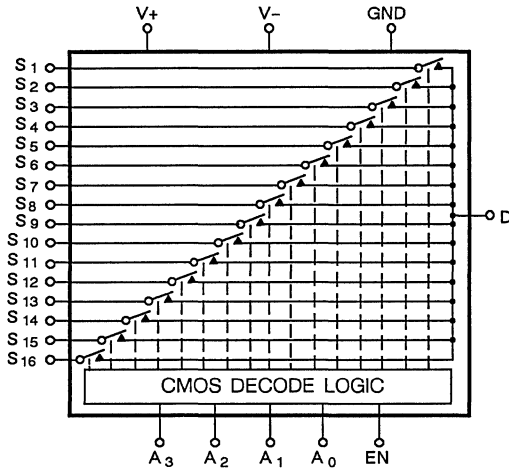


- Order Numbers:  
 Side Braze: DG506AAR  
 DG506ABR  
 DG506ACR  
 CerDIP: DG506AAK  
 DG506ABK  
 DG506ACK  
 Plastic: DG506ACJ

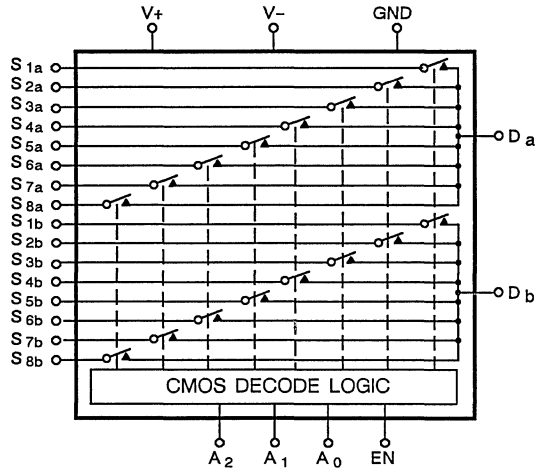


- Order Numbers:  
 Side Braze: DG507AAR  
 DG507ABR  
 DG507ACR  
 CerDIP: DG507AAK  
 DG507ABK  
 DG507ACK  
 Plastic: DG507ACJ

## FUNCTIONAL BLOCK DIAGRAM



**DG506A**  
16-Channel Single Ended Multiplexer



**DG507A**  
Differential 8-Channel Multiplexer

## ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs,  $V_S, V_D^h$  ..... (V-) -2 V to (V+) +2 V or  
..... 20 mA, whichever occurs first.

Current (Any Terminal, Except S or D) ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak CURRENT, S or D  
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA

Storage Temperature (A & B Suffix) ..... -65 to 150°C  
(C Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
(D Suffix) ..... -40 to 85°C  
(C Suffix) ..... 0 to 70°C

Power Dissipation (Package)\*

28-Pin Ceramic DIP\*\* ..... 1200 mW  
28-Pin Plastic DIP\*\*\* ..... 625 mW

\* All leads soldered or welded to PC board.

\*\* Derate 16 mW/°C above 75°C.

\*\*\* Derate 8.3 mW/°C above 75°C.

## ELECTRICAL CHARACTERISTICS<sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}, V_- = -15\text{ V}$ GND = 0	LIMITS						UNIT
			1=25°C		A SUFFIX		B, C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$		1,2,3		-15	15	-15	15	V
Drain-Source <sup>e</sup> ON Resistance	$r_{DS(ON)}$	$V_D = \pm 10\text{ V}, V_{AL} = 0.8\text{ V}$ $I_S = -200\ \mu\text{A}, V_{AH} = 2.4\text{ V}$	1,3 .2			400 500		450 550	$\Omega$
Greatest Change in $r_{DS(ON)}$ Between Channels <sup>f</sup>	$\frac{\Delta}{r_{DS(ON)}}$	-10 V < $V_S$ < 10 V	1	6					%



ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ GND = 0	LIMITS						UNIT		
			1=25°C		A SUFFIX		B, C SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SWITCH (Cont'd)</b>											
Source OFF Leakage Current	DG506A DG507A	$I_{S(OFF)}$	$V_{EN} = 0\text{ V}$	$V_S = \pm 10\text{ V}$	1		-1	1	-5	5	nA
				$V_D = \mp 10\text{ V}$	2		-50	50	-50	50	
Drain OFF Leakage Current				$V_D = \pm 10\text{ V}$	1		-10	10	-20	20	
				$V_S = \mp 10\text{ V}$	2		-300	300	-300	300	
				$V_D = \pm 10\text{ V}$	1		-5	5	-10	10	
				$V_S = \mp 10\text{ V}$	2		-200	200	-200	200	
Drain ON <sup>e,g</sup> Leakage Current	DG506A DG507A	$I_{D(ON)}$	$V_S = V_D = \pm 10\text{ V}$ $V_{AL} = 0.8\text{ V}$ $V_{AH} = 2.4\text{ V}$		1		-10	10	-20	20	
						2		-300	300	-300	
					1		-5	5	-10	10	
					2		-200	200	-200	200	
<b>INPUT</b>											
Logic Input Current Input Voltage High	$I_{AH}$	$V_A = 2.4\text{ V}$		1		-10		-10		$\mu\text{A}$	
					2		-30		-30		
		$V_A = 15\text{ V}$		1			10		10		
				2			30		30		
Logic Input Current Input Voltage Low	$I_{AL}$	$V_{EN} = 0, 2.4\text{ V}, V_A = 0\text{ V}$		1		-10		-10			
				2		-30		-30			
<b>DYNAMIC</b>											
Switching Time of Multiplexer	$t_{TRANS}$	See Figure 1		1	0.6		1			$\mu\text{s}$	
Break-Before-Make Interval	$t_{OPEN}$	See Figure 3		1	0.2					ns	
Enable Turn ON Time	$t_{ON(EN)}$	See Figure 2		1	1					$\mu\text{s}$	
Enable Turn OFF Time	$t_{OFF(ON)}$	See Figure 2		1	0.4						
Charge Injection	Q			1	20					pC	
OFF Isolation <sup>l</sup>		$V_{EN} = 0, R_L = 1\text{ k}\Omega$ $C_L = 15\text{ pF}, V_S = 7\text{ V}_{RMS}$ $f = 500\text{ kHz}$		1	68					dB	
Source OFF Capacitance	$C_{S(OFF)}$	$V_{EN} = 0$ $f = 140\text{ kHz}$	$V_S = 0$	1	6					pF	
Drain OFF Capacitance	DG506A		$V_D = 0$		1	45					
	DG507A				1	23					

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0	LIMITS				UNIT		
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C			B, C SUFFIX	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		MIN <sup>b</sup>	MAX <sup>b</sup>
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>EN</sub> = 0, V <sub>A</sub> = 0	1	1.3		2.4		2.4	mA
Negative Supply Current	I <sub>-</sub>		1	-0.7	-1.5		-1.5		

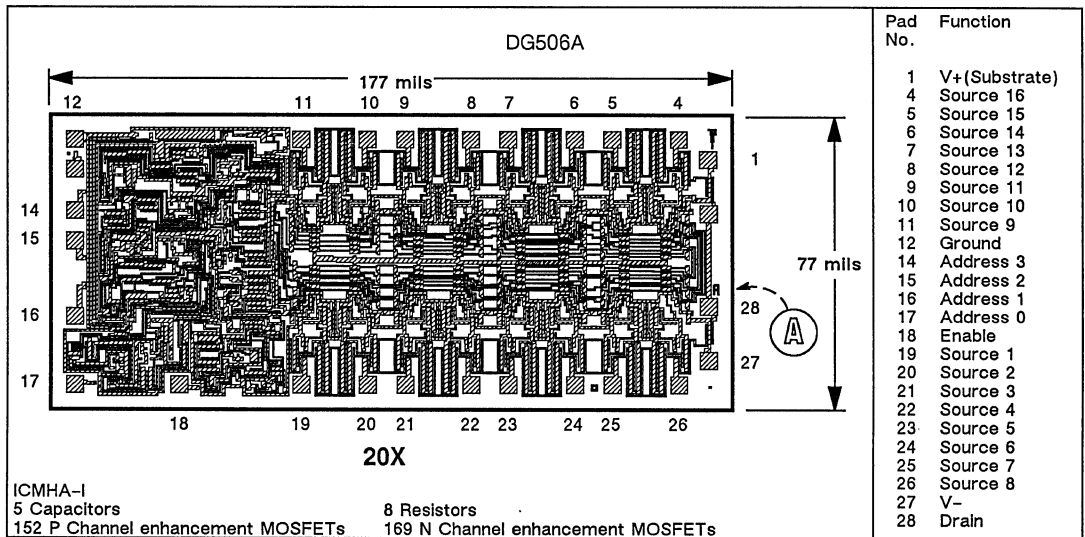
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Sequence each switch ON.

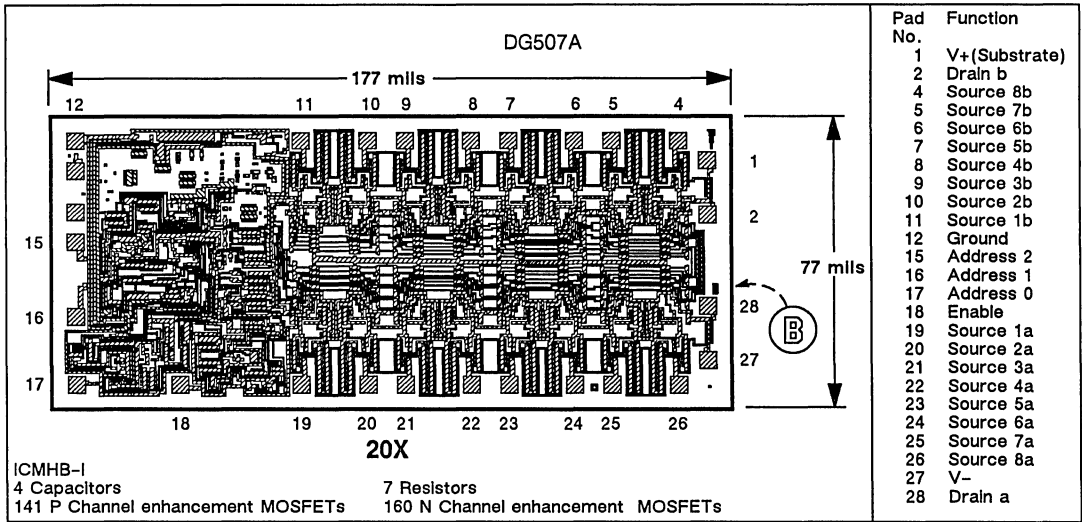
$$f. \Delta r_{DS(ON)} = \left( \frac{r_{DS(ON) \text{ MAX}} - r_{DS(ON) \text{ MIN}}}{r_{DS(ON) \text{ AVE}}} \right)$$

- g. I<sub>D(ON)</sub> is leakage from driver into "ON" switch.
- h. Signals on S<sub>x</sub>, D<sub>x</sub> or IN<sub>x</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- i. OFF Isolation = 20 log  $\frac{V_D}{V_S}$ , V<sub>S</sub> = Input to "OFF" switch, V<sub>D</sub> = output due to V<sub>S</sub>.

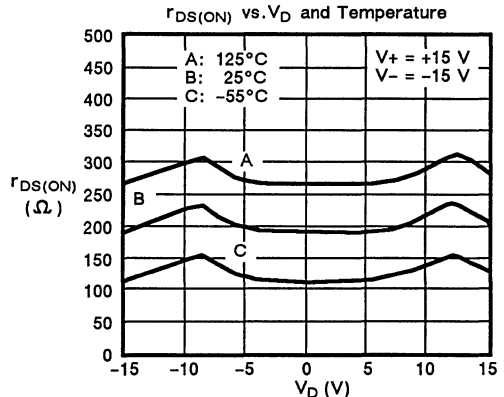
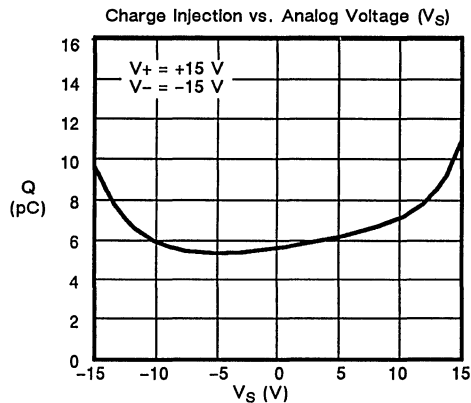
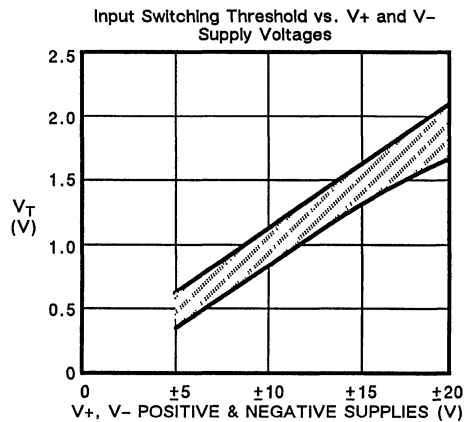
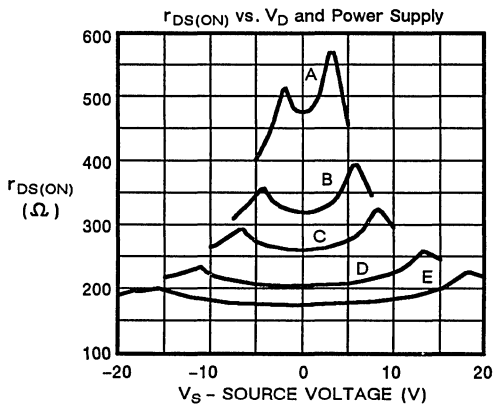
**DIE TOPOGRAPHY**



## DIE TOPOGRAPHY (Cont'd)



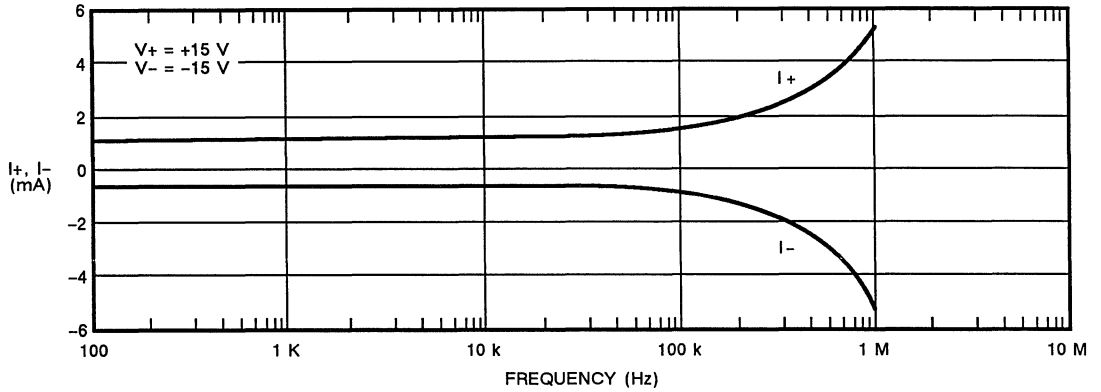
## TYPICAL CHARACTERISTICS



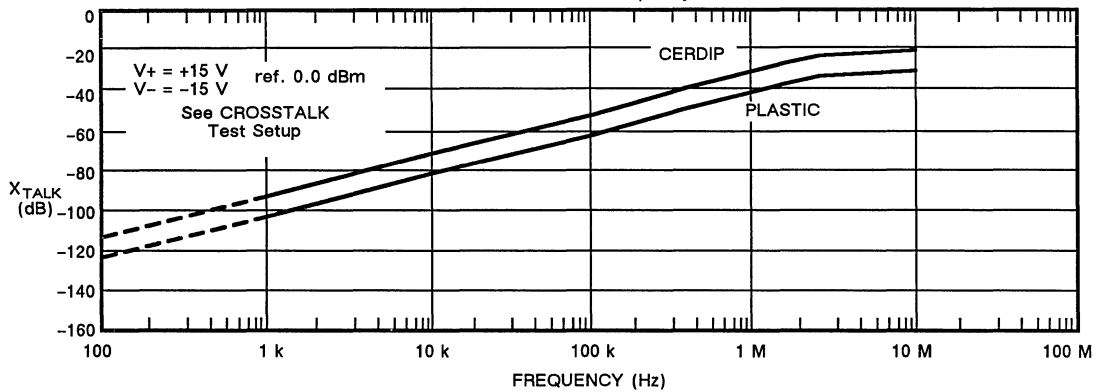
5

## TYPICAL CHARACTERISTICS (Cont'd)

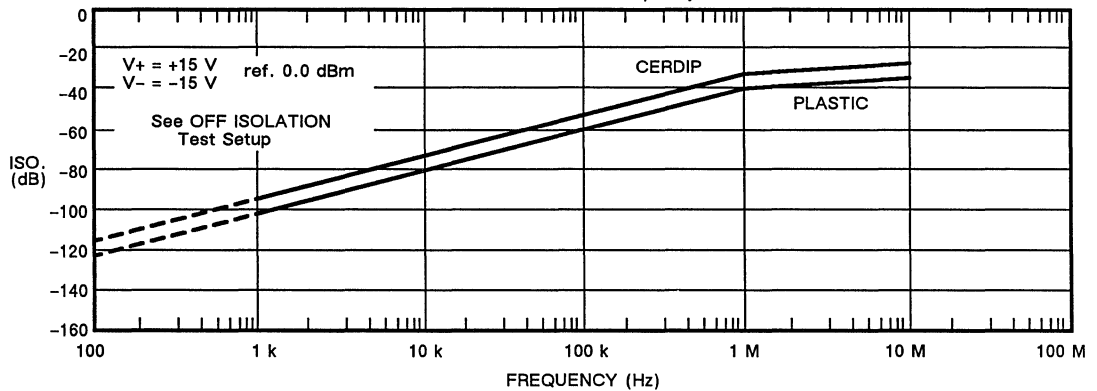
Supply Current vs. Switching Frequency



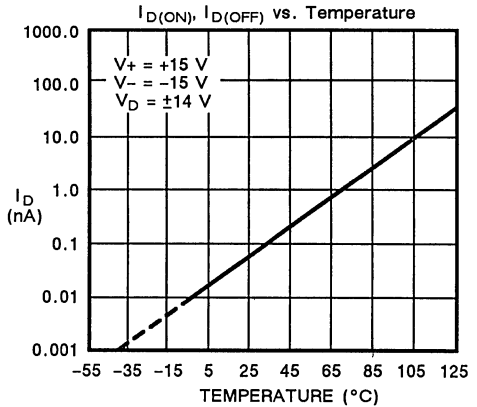
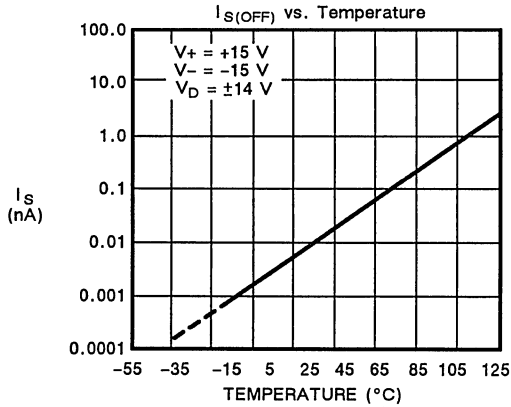
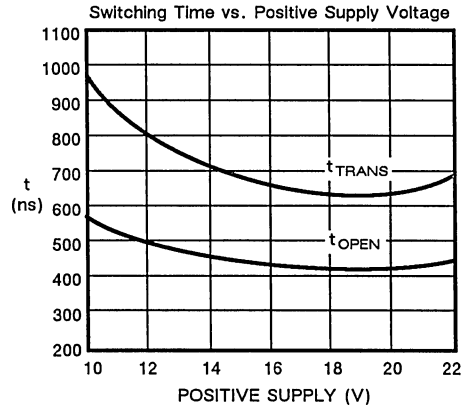
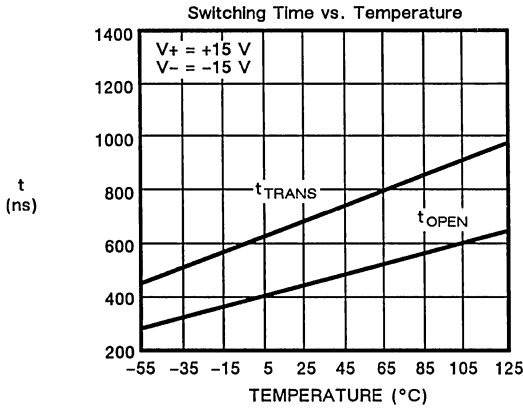
Crosstalk vs. Frequency



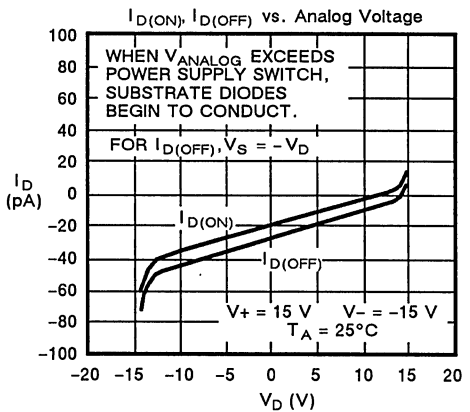
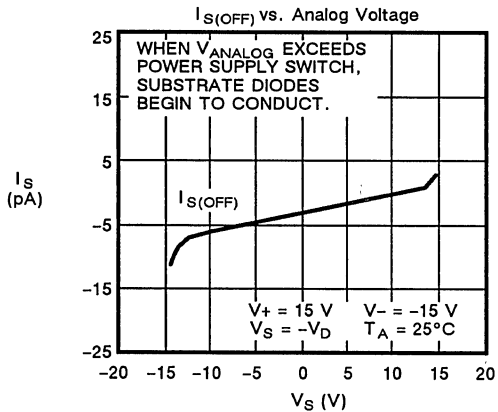
Off Isolation vs. Frequency



TYPICAL CHARACTERISTICS (Cont'd)



5



## TRUTH TABLES

DG506A

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG507A

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" =  $V_{AL} < 0.8 V$ , LOGIC "1" =  $V_{AH} > 2.4 V$

## t<sub>TRANSITION TIME TEST CIRCUIT</sub>

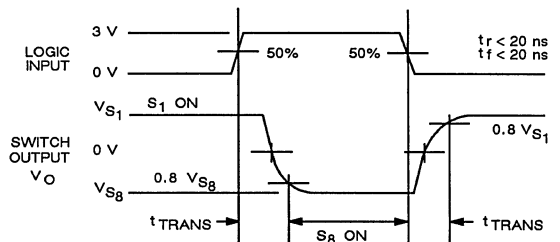
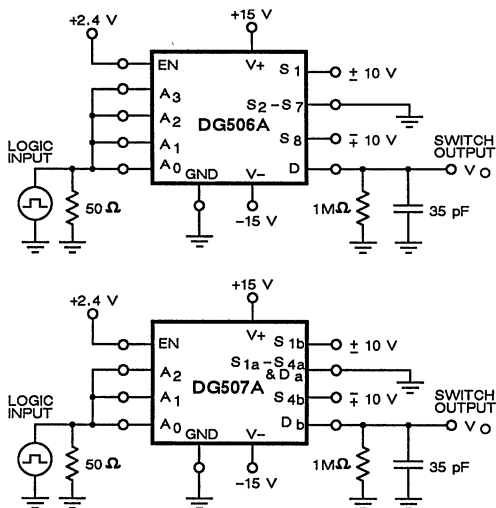


Figure 1

## t<sub>ON(EN)</sub> AND t<sub>OFF(EN)</sub> TIME TEST CIRCUIT

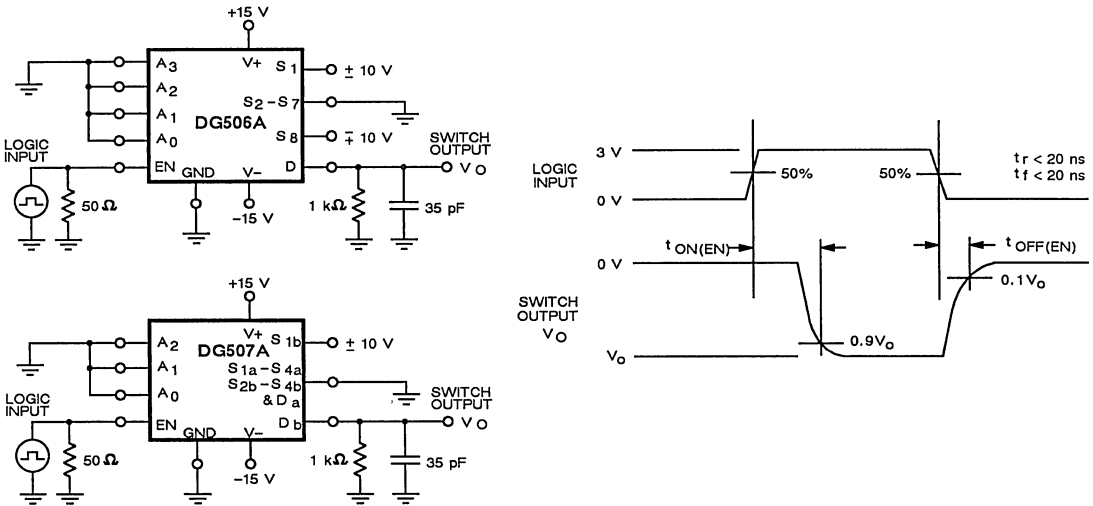


Figure 2

## t<sub>OPEN</sub> TIME TEST CIRCUIT

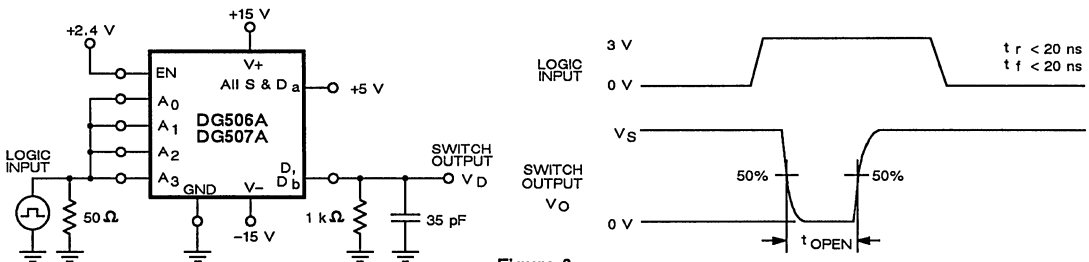
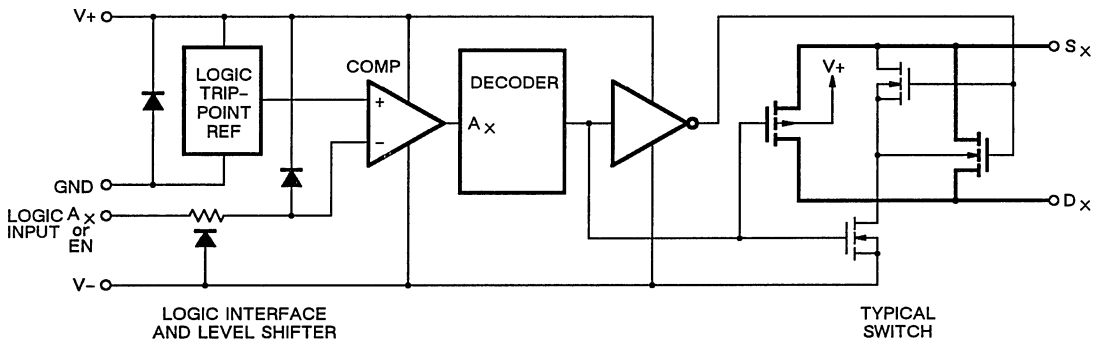


Figure 3

5

## SCHEMATIC DIAGRAM



## APPLICATION HINTS\*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15 **	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.6	-12 to 12
10	-10	2.4/0.5	-10 to 10
8 ***	-8	2.4/0.3	-8 to 8

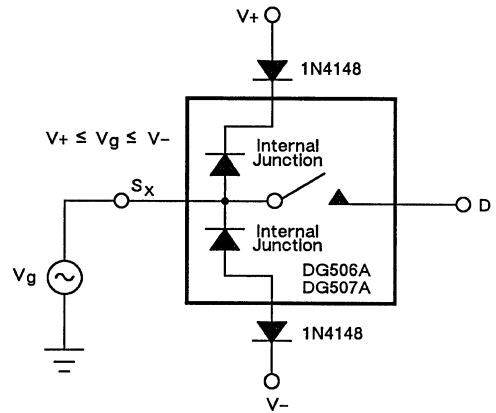
\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

\*\* Electrical Characteristics chart based on V+ = +15 V, V- = -15 V.

\*\*\* Operation below ±8 V is not recommended due to the shift in V<sub>INL</sub>(MAX).

### Overvoltage Protection

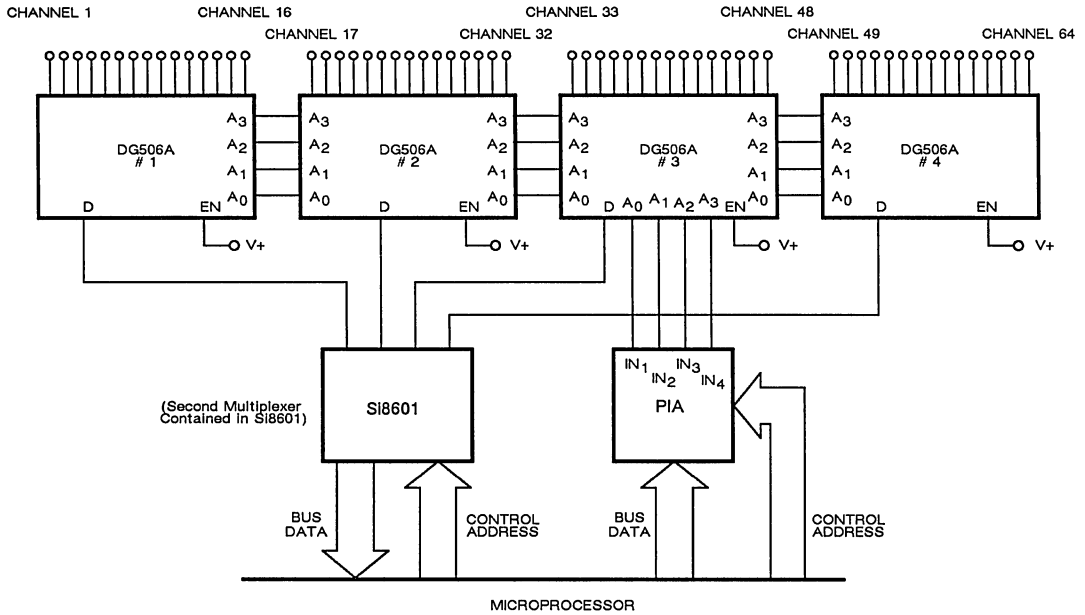
A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V<sub>s</sub> - (V-) doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.



Overvoltage Protection Using Blocking Diodes



**APPLICATIONS**



64-Channel 2-Level Multiplex System

## Precision 8-Channel CMOS Multiplexer/Demultiplexer

### FEATURES

- Fully Tested Around  $\pm 10.8, \pm 16.5$  and  $\pm 20$  V Supplies
- 10% (Max.) delta  $r_{DS(ON)}$
- 2.0 nA (Max.) Leakage at 25°C,  $\pm 16.5$  V
- Low Charge Injection ( $Q < 15$  pC)
- Pin-Compatible with DG508A

### BENEFITS

- Simplifies Worst-Case Analysis
- Reduces Channel-to-Channel Variations
- Reduces Switching Errors
- Reduces Switching Noise
- Simplifies Upgrading

### APPLICATIONS

- Automatic Test Equipment
- Communication Systems
- Precision Data Acquisition
- Precision Instrumentation
- Upgrading Old Designs

### DESCRIPTION

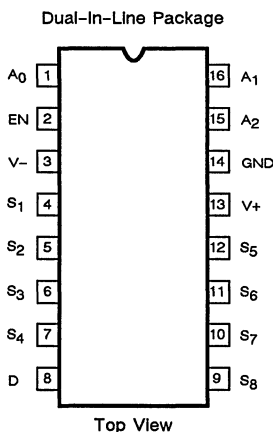
The DGP508A is a precision 8-channel CMOS analog multiplexer/demultiplexer which is specified with improved static and dynamic performance limits. The DGP508A features tighter leakage and delta  $r_{DS(ON)}$  limits and wider analog signal ranges than the industry-standard DG508A, yet maintains 100% pin and functional compatibility. This allows for precision system performance upgrading without redesign or layout of circuit boards. In addition, the specification limits and associated test conditions are in a military drawing format, simplifying source-control documentation and ensuring performance based upon a worst-case analysis. Refer to the "Detailed Description" for more information on the "DGP" family.

Produced on a proprietary high-voltage CMOS process, the DGP508A has been fully specified for signals up to  $\pm 20$  V, making it an ideal choice for extended range operation, or in systems with additional headroom requirements. An epitaxial layer prevents latchup.

The DGP508A is available in a 16-pin plastic DIP for the industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ) temperature range and the CerDIP for military (available with /883 processing), A suffix ( $-55$  to  $125^\circ\text{C}$ ) temperature operation.

For more information on the DGP508A, please refer to Siliconix Technical Article TA87-1.

### PIN CONFIGURATION

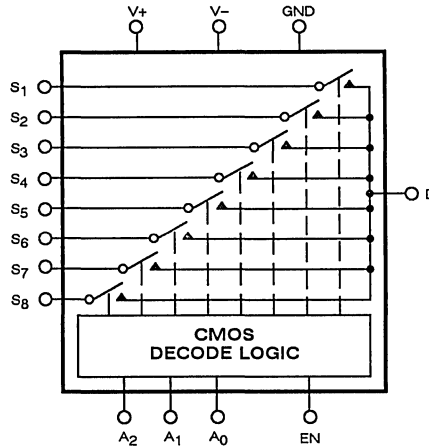


### TRUTH TABLE

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" =  $V_{AL} < 0.8$  V  
 Logic "1" =  $V_{AH} > 2.4$  V

**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs $V_S, V_D^1$	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current (Any Terminal) Continuous	30 mA
Current (S or D) Pulsed 1 ms 10% duty	100 mA
Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C

Operating Temperature (A Suffix)	-55 to 125°C
(D Suffix)	-40 to 85°C

Power Dissipation (Package) *	
16-Pin Plastic DIP**	450 mW
16-Pin CerDIP***	900 mW
16-Pin Small Outline****	900 mW

\* All leads welded or soldered to PC board.

\*\* Derate 6 mW/°C above 75°C.

\*\*\* Derate 12 mW/°C above 75°C.

\*\*\*\* Derate 7.7 mW/°C above 75°C.

1 Signals on  $S_X, D_X$  or  $IN_X$  exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

**5**

**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V GND = 0 V V <sub>AH</sub> = 2.4 V, V <sub>AL</sub> = 0.8 V V <sub>EN</sub> = 2.4 V	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Drain-Source <sup>e</sup> ON Resistance	r <sub>DS(ON)</sub>	V+ = 13.5 V, V- = -13.5 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±10.0 V	1,3 2	265		400 500		400 500	Ω
		V+ = 10.8 V, V- = -10.8 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±7.5 V V <sub>IN</sub> = 0.4 V	1,3 2	300		450 550		450 550	
		V+ = 20 V, V- = -20 V I <sub>S</sub> = 1 mA, V <sub>D</sub> = ±15 V	1,3 2	200		350 450		350 450	
Delta Drain-Source <sup>e</sup> ON Resistance	Δ r <sub>DS(ON)</sub>	V <sub>D</sub> = +5, 0, -5 V, I <sub>S</sub> = ±1 mA V <sub>IN</sub> = 0.8 V Worst Combination	1 2,3	20		40 50		40 50	

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>AH</sub> = 2.4 V, V <sub>AL</sub> = 0.8 V V <sub>EN</sub> = 2.4 V		LIMITS						UNIT		
				1=25°C		A SUFFIX		D SUFFIX				
				2=125, 85°C		-55 to 125°C		-40 to 85°C				
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SWITCH (Cont'd)</b>												
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>+</sub> = 13.5 V V <sub>-</sub> = -13.5 V	V <sub>D</sub> = -12.5 V V <sub>S</sub> = +12.5 V	1 2	0.01	-0.25 -10	0.25 10	-0.25 -2	0.25 2	nA		
			V <sub>D</sub> = +12.5 V V <sub>S</sub> = -12.5 V	1 2	-0.01	-0.25 -10	0.25 10	-0.25 -2	0.25 2			
		V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>D</sub> = -15.5 V V <sub>S</sub> = +15.5 V	1 2	0.01	-0.25 -10	0.25 10	-0.25 -2	0.25 2			
			V <sub>D</sub> = +15.5 V V <sub>S</sub> = -15.5 V	1 2	-0.01	-0.25 -10	0.25 10	-0.25 -2	0.25 2			
		V <sub>+</sub> = 20 V V <sub>-</sub> = -20 V	V <sub>D</sub> = -19 V V <sub>S</sub> = +19 V	1 2	0.03	-1 -50	1 50	-1 -10	1 10			
			V <sub>D</sub> = +19 V V <sub>S</sub> = -19 V	1 2	-0.03	-1 -50	1 50	-1 -10	1 10			
		V <sub>D</sub> = -5 V V <sub>S</sub> = +5 V		2		-5	5	-2	2			
		V <sub>D</sub> = +5 V V <sub>S</sub> = -5 V		2		-5	5	-2	2			
		Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>+</sub> = 13.5 V V <sub>-</sub> = -13.5 V	V <sub>D</sub> = -12.5 V V <sub>S</sub> = +12.5 V	1 2	0.08	-2 -100	2 100		-2 -20	2 20
					V <sub>D</sub> = +12.5 V V <sub>S</sub> = -12.5 V	1 2	-0.08	-2 -100	2 100		-2 -20	2 20
V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>D</sub> = -15.5 V V <sub>S</sub> = +15.5 V			1 2	0.10	-2 -100	2 100	-2 -20	2 20			
	V <sub>D</sub> = +15.5 V V <sub>S</sub> = -15.5 V			1 2	-0.10	-2 -100	2 100	-2 -20	2 20			
V <sub>+</sub> = 20 V V <sub>-</sub> = -20 V	V <sub>D</sub> = -19 V V <sub>S</sub> = +19 V			1 2	0.25	-5 -200	5 200	-5 -50	5 50			
	V <sub>D</sub> = +19 V V <sub>S</sub> = -19 V			1 2	-0.25	-5 -200	5 200	-5 -50	5 50			
V <sub>D</sub> = -5 V V <sub>S</sub> = +5 V				2		-50	50	-20	20			
V <sub>D</sub> = +5 V V <sub>S</sub> = -5 V				2		-50	50	-20	20			
Channel ON <sup>o</sup> Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>			V <sub>+</sub> = 16.5 V V <sub>-</sub> = -16.5 V	V <sub>D</sub> = +15.5 V V <sub>S</sub> = +15.5 V	1 2	0.10	-2 -100	2 100	-2 -20	2 20	
					V <sub>D</sub> = -15.5 V V <sub>S</sub> = -15.5 V	1 2	-0.10	-2 -100	2 100	-2 -20	2 20	
		V <sub>+</sub> = 20 V V <sub>-</sub> = -20 V	V <sub>D</sub> = +19 V V <sub>S</sub> = +19 V	1 2	0.25	-5 -200	5 200	-5 -50	5 50			
			V <sub>D</sub> = -19 V V <sub>S</sub> = -19 V	1 2	-0.25	-5 -200	5 200	-5 -50	5 50			

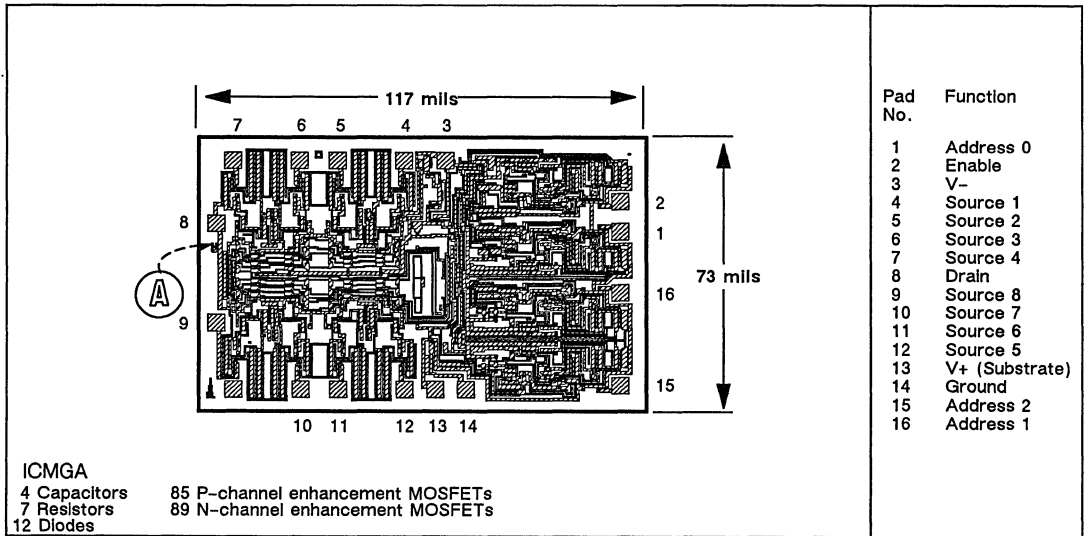
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>AH</sub> = 2.4 V, V <sub>AL</sub> = 0.8 V V <sub>EN</sub> = 2.4 V	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH (Cont'd)</b>									
Channel ON <sup>e</sup> Leakage Current (Continued)	I <sub>D(ON)</sub> <sup>+</sup>	V <sub>D</sub> = +5 V V <sub>S</sub> = +5 V	2		-50	50	-20	20	nA
	I <sub>S(ON)</sub>	V <sub>D</sub> = -5 V V <sub>S</sub> = -5 V	2		-50	50	-20	20	
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 2.4 V V <sub>A</sub> = 0 or 2.4 V V <sub>±</sub> = ±16.5 V	1,2 3	1.3		2.4 3		2.4 3	mA
	I <sub>+</sub> STANDBY		1,2 3	1.3		2.4 3		2.4 3	
Negative Supply Current	I <sub>-</sub>		1,2 3	-0.65	-1.5 -2		-1.5 -2		
	I <sub>-</sub> STANDBY		1,2 3	-0.65	-1.5 -2		-1.5 -2		
<b>INPUT</b>									
Input Current With V <sub>IN</sub> High	I <sub>AH</sub>	V <sub>+</sub> = 20 V, V <sub>-</sub> = -20 V V <sub>IN</sub> under test = 2.4 V	1,2	-0.001	-0.5	0.5	-0.5	0.5	μA
		V <sub>+</sub> = 20 V, V <sub>-</sub> = -20 V V <sub>IN</sub> under test = 20 V	1,2	0.004	-0.5	0.5	-0.5	0.5	
Input Current With V <sub>IN</sub> Low	I <sub>AL</sub>	V <sub>+</sub> = 20 V, V <sub>-</sub> = -20 V V <sub>IN</sub> under test = 0 V	1,2	0.01	-0.5	0.5	-0.5	0.5	
<b>DYNAMIC</b>									
Enable Turn-ON Time	t <sub>ON(EN)</sub>	See Switching Time Test Circuits	1,3 2	750		1000 1500		1000 1500	ns
Enable Turn-OFF Time	t <sub>OFF(EN)</sub>		1,3 2	350		1000 1500		1000 1500	
Multiplexer Switching Time	t <sub>TRANS</sub>		1,3 2	700		1000 1500		1000 1500	
Break-Before-Make Interval	t <sub>OPEN</sub>		1	450	50		50		
Charge Injection	Q	R <sub>gen</sub> = 0 Ω C <sub>L</sub> = 10 nF	V <sub>gen</sub> = 0 V		1	5.5		15	pC
			V <sub>gen</sub> = ±10 V		1	7		20	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>AH</sub> = 2.4 V, V <sub>AL</sub> = 0.8 V V <sub>EN</sub> = 2.4 V	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
Source OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz	1	5					pF
Drain OFF Capacitance	C <sub>D(OFF)</sub>		1	25					
Drain and Source ON Capacitance	C <sub>S(ON)</sub> + C <sub>D(ON)</sub>		1	30					
Crosstalk		f = 100 kHz	1	-60					dB
OFF Isolation			1	-60					
Insertion Loss			1	-1.6					

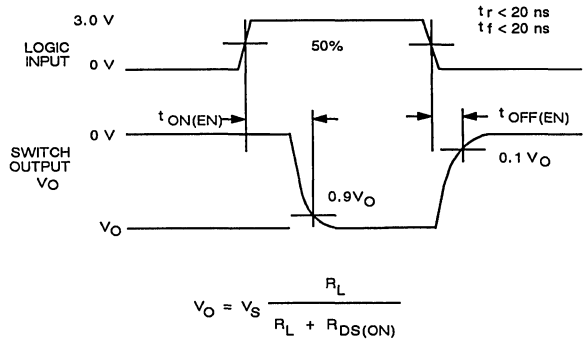
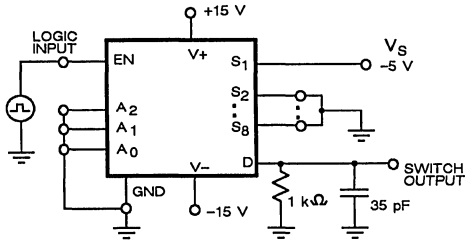
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Sequence each switch ON.

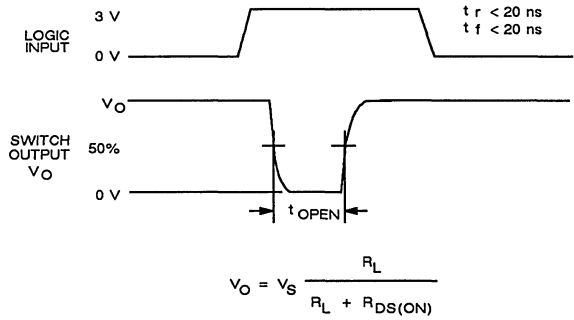
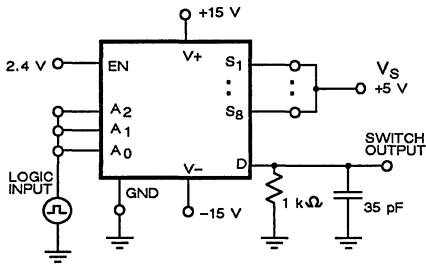
## DIE TOPOGRAPHY



**t<sub>ON(EN)</sub> AND t<sub>OFF(EN)</sub> TEST CIRCUIT**

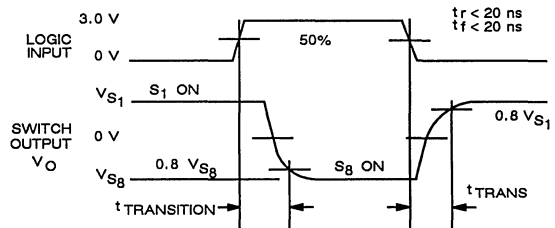
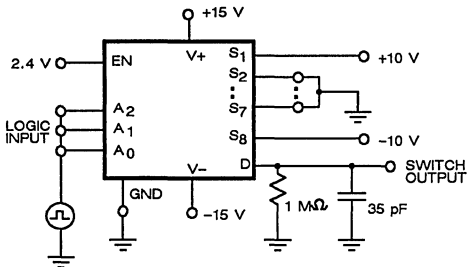


**t<sub>OPEN</sub> TEST CIRCUIT**

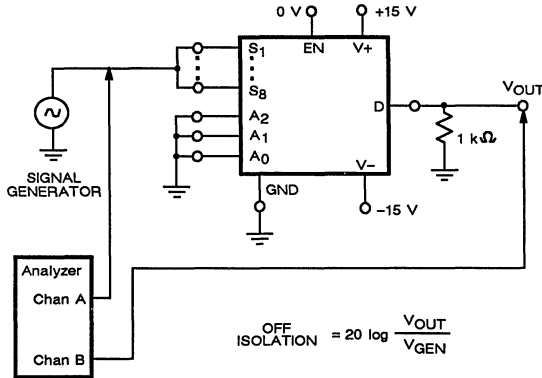


**5**

**t<sub>TRANSITION</sub> TEST CIRCUIT**

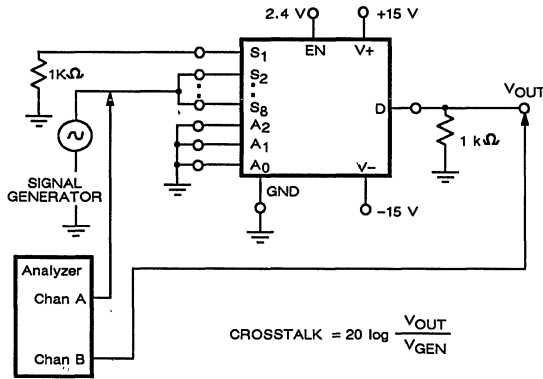


## OFF ISOLATION TEST CIRCUIT



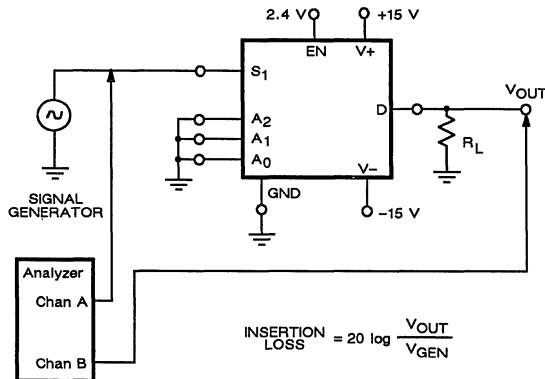
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

## CROSSTALK TEST CIRCUIT



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

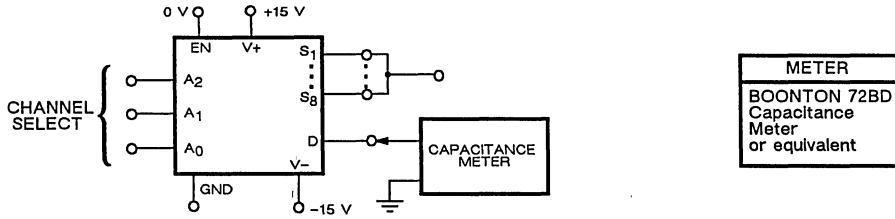
## INSERTION LOSS TEST CIRCUIT



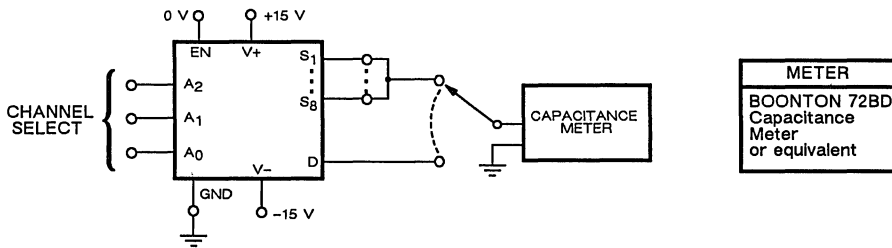
FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer



## DRAIN ON CAPACITANCE

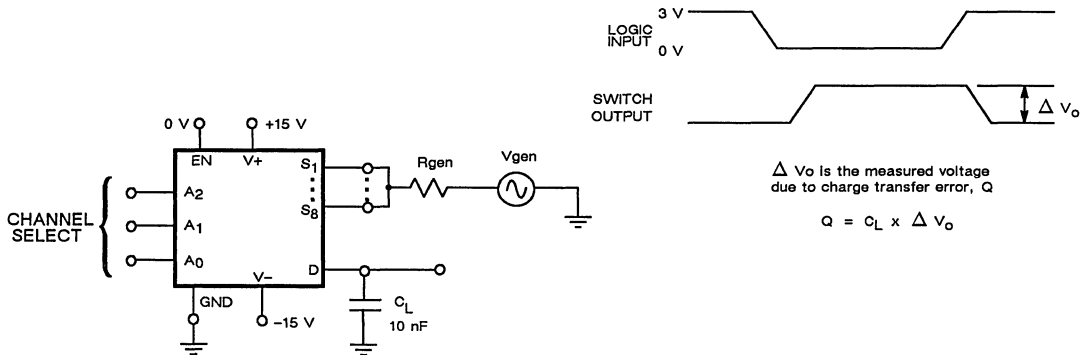


## SOURCE/DRAIN OFF CAPACITANCE

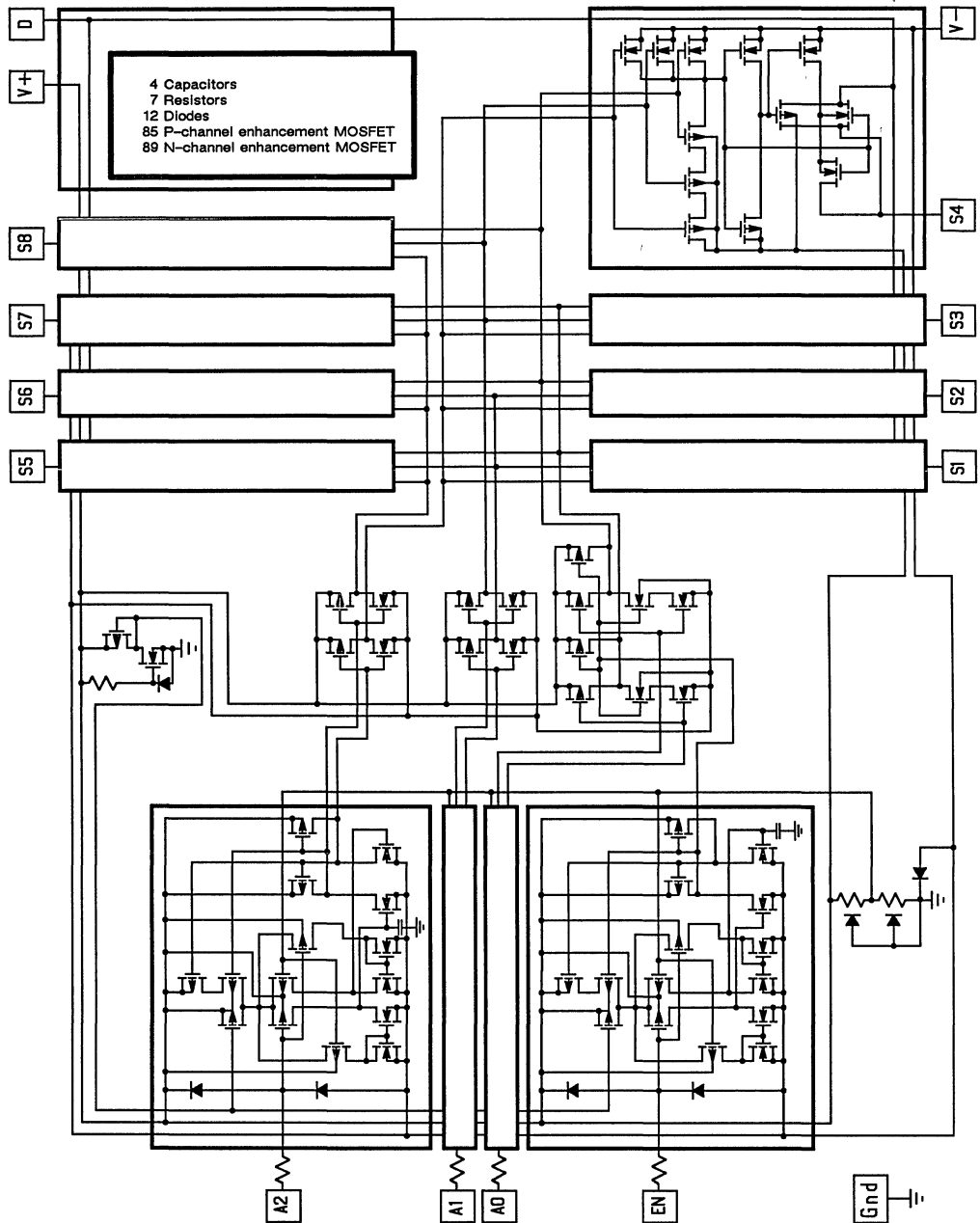


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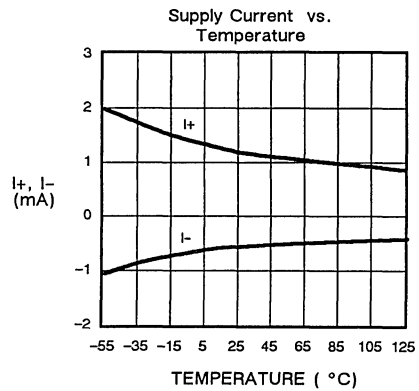
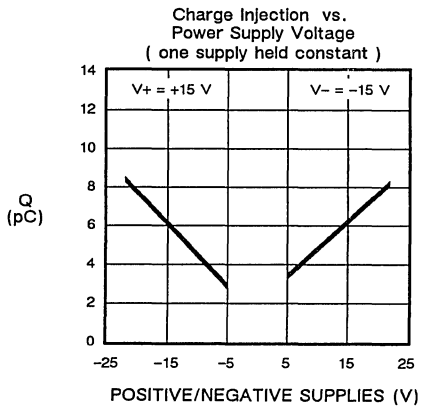
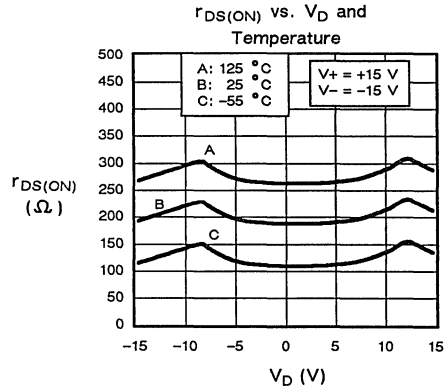
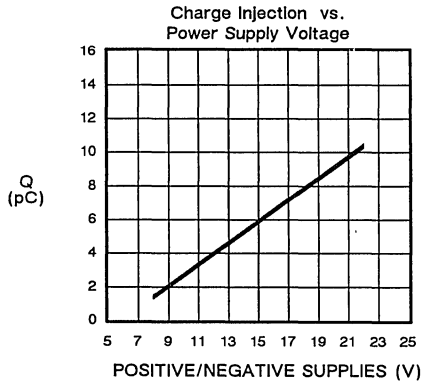
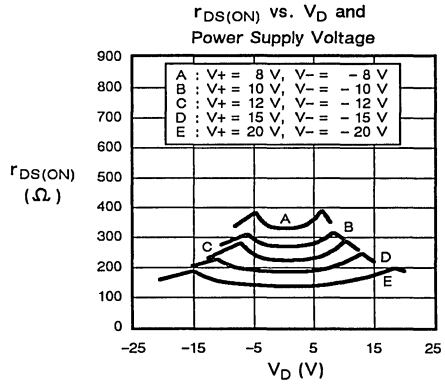
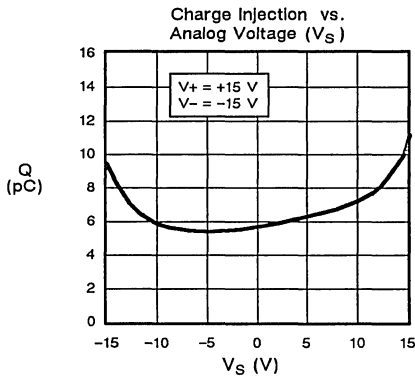
## CHARGE TRANSFER ERROR



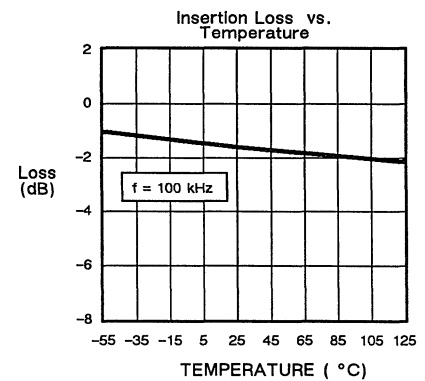
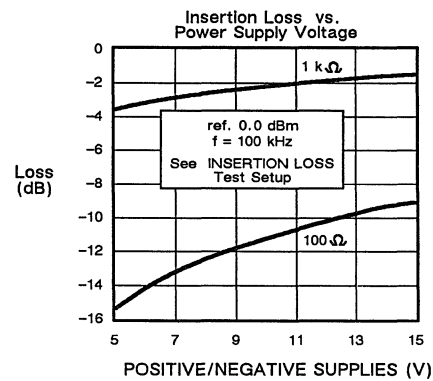
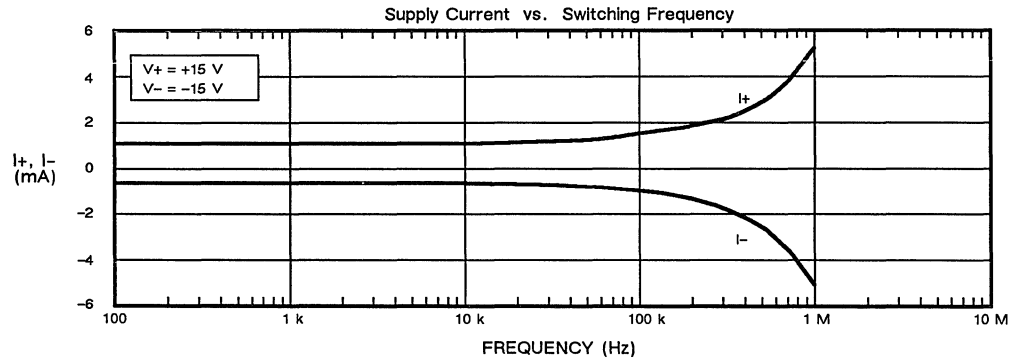
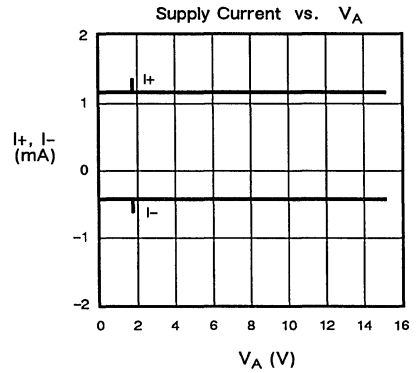
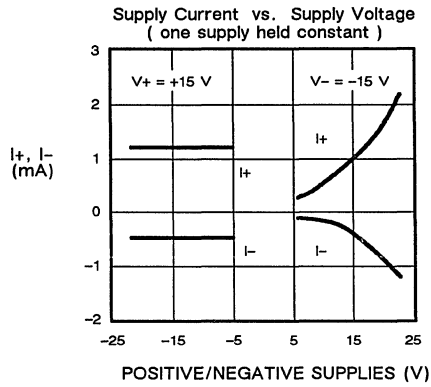
## SCHEMATIC DIAGRAM



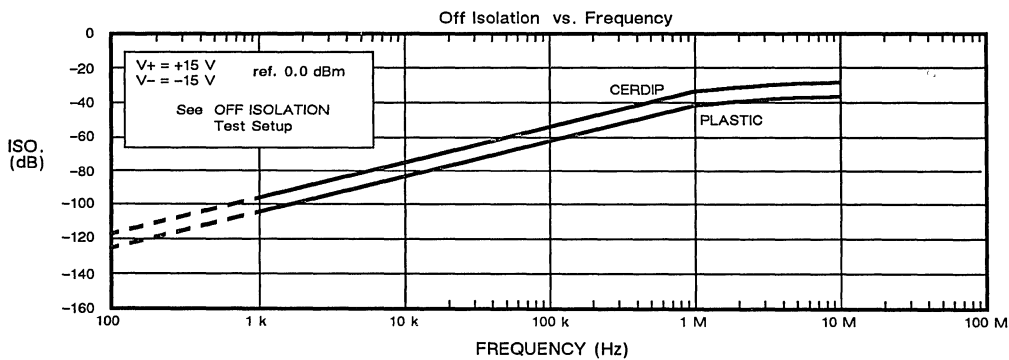
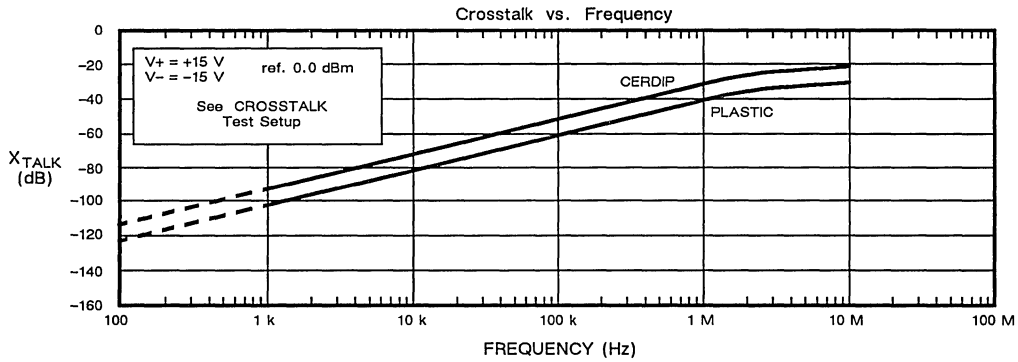
**TYPICAL CHARACTERISTICS**



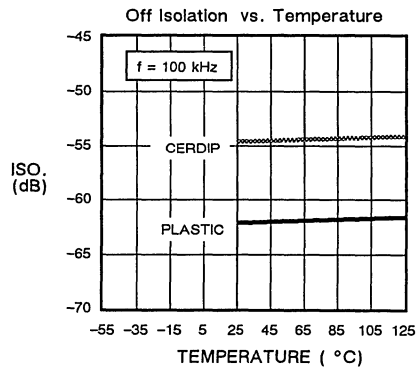
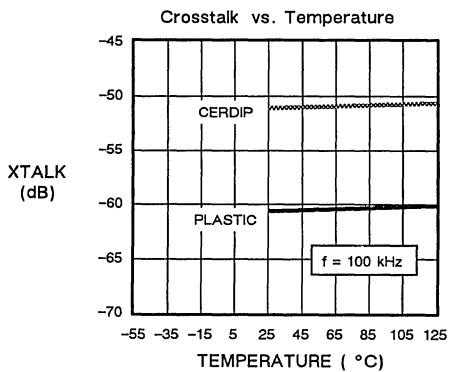
## TYPICAL CHARACTERISTICS (Cont'd)



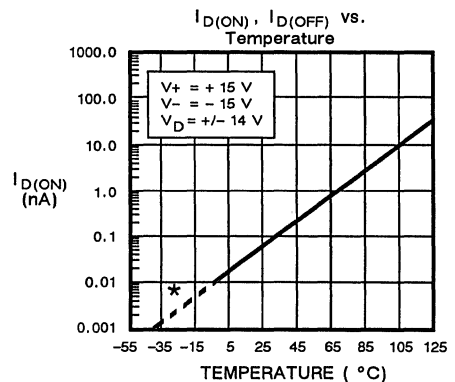
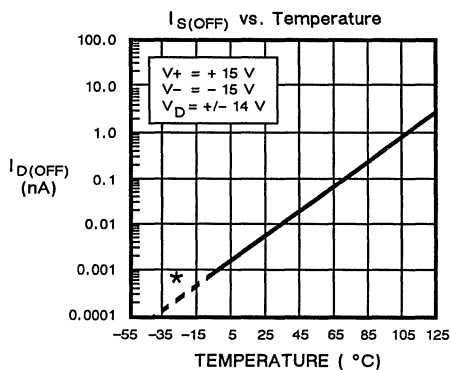
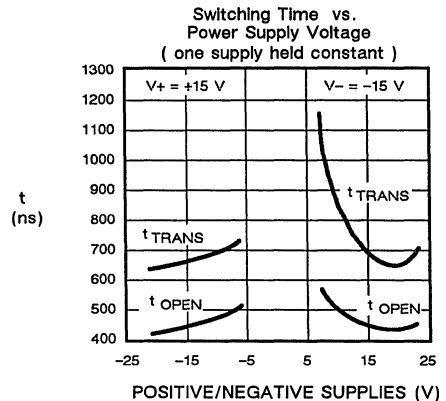
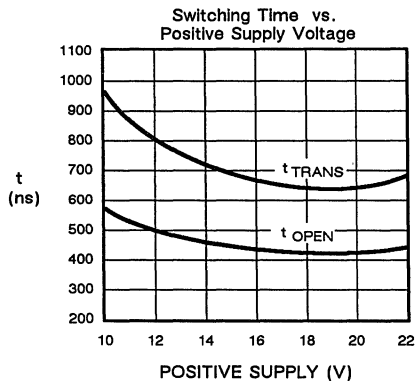
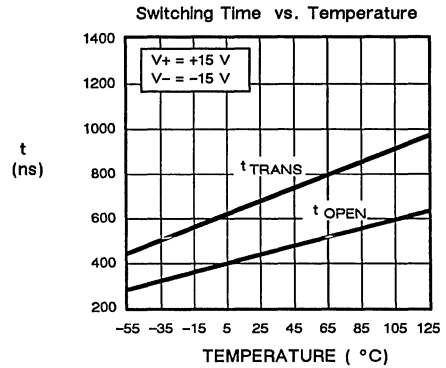
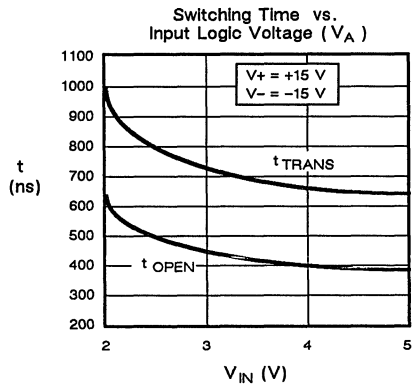
TYPICAL CHARACTERISTICS (Cont'd)



**5**

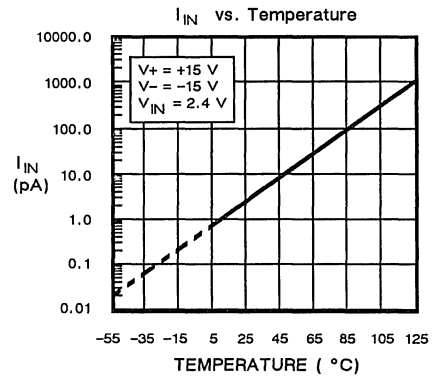
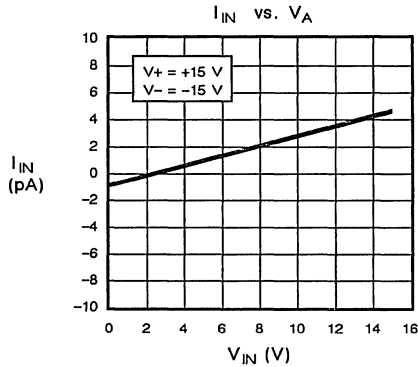
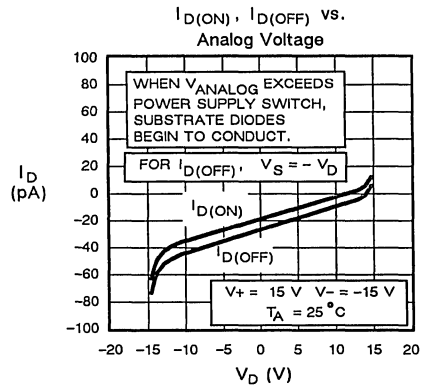
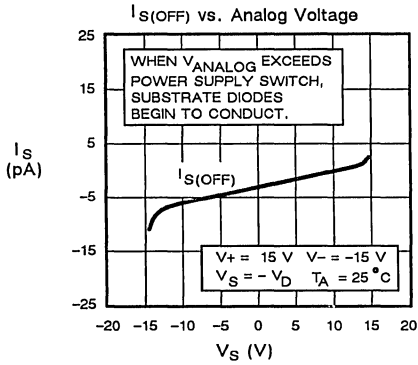


## TYPICAL CHARACTERISTICS (Cont'd)

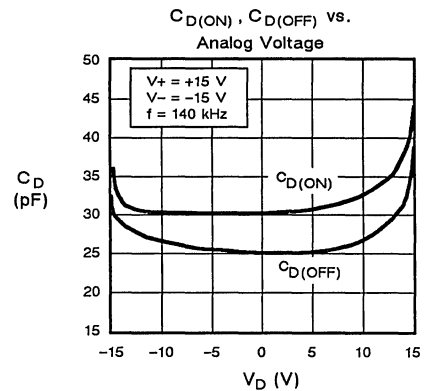
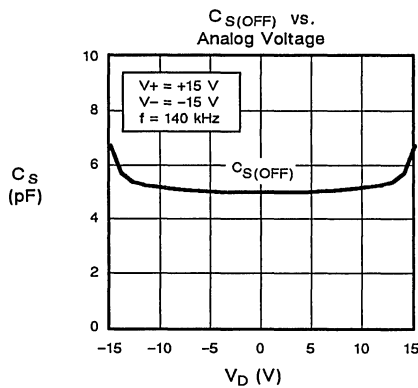


\* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

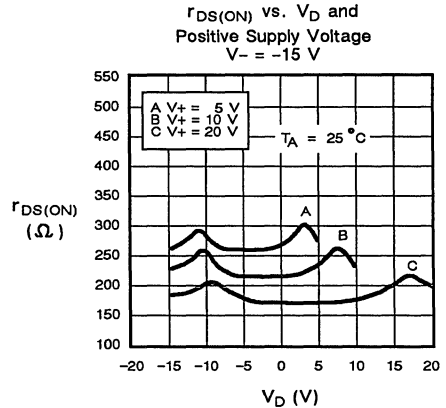
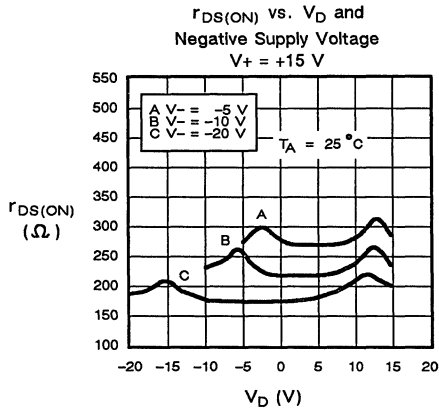
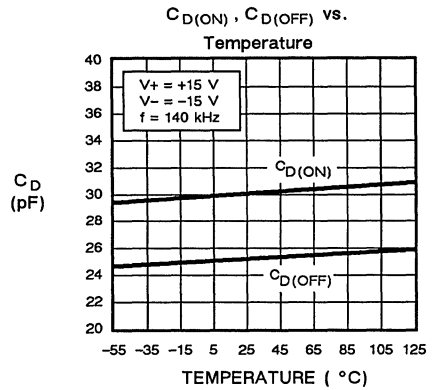
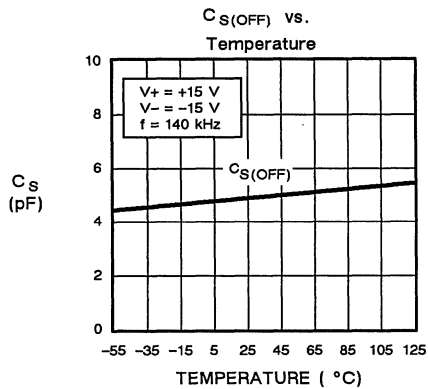
**TYPICAL CHARACTERISTICS (Cont'd)**



**5**



## TYPICAL CHARACTERISTICS (Cont'd)



## DETAILED DESCRIPTION

### The DGP Family Of Analog Switches And Multiplexers

Siliconix has improved its high voltage metal-gate CMOS process to allow for lower leakage, higher voltage and lower variation performance. Additionally, through dramatic improvements in automated testing technology, specifications and limits that were previously untestable are now 100% tested and specified on the DGP508A data sheet.

The data sheet specification tables are in a new format as well. The format is that of a military drawing, where all min/max specifications are 100% tested, eliminating any uncertainty about what is

actually tested. Many parameters that were previously listed as "typical" or "guaranteed by design" are now 100% tested with minimum and maximum values, so that a worst-case design can be realized.

For example, charge transfer error (or charge injection) was listed only as a typical value in the standard DG508/509A data sheet, and no maximum value was guaranteed. A maximum limit of 20 pC has been established on the data sheet, and this value is 100% tested. This allows the design engineer to design precision switching circuits, such as sample-and-hold amplifiers, with fixed limits for the charge compensation circuit.



**DETAILED DESCRIPTION (Cont'd)**

The DGP508A data sheet also specifies parameters that previously have never been specified. An example is the variation in switching time over all channels, specified to a 50 ns maximum. The variation of ON resistance is similarly specified and 100% tested to be less than 40 Ω over six different drain voltage and source current conditions, over all four channels tested, resulting in 48 different readings. This specification is necessary for determining the worst-case distortion and signal level variation due to differences in channel resistance and ON resistance modulation effects. Also note that  $r_{DS(ON)}$  is measured at the lower extreme of the voltage operating level, (e.g. ±13.5 V instead of ±15 V) where  $r_{DS(ON)}$  is highest.

Leakage currents are specified and tested to new

lower limits at both room temperature and over the full temperature range. For example, the industrial range devices' leakages have been reduced from 200 nA (over temp) on the DG508A to 50 nA (over temp) on the DGP version. Additionally, the leakages are specified at the extremes of the operating ranges (e.g. ±16.5 V instead of ±15 V), where the leakages tend to be the highest. This is essential for designs where worst-case leakage must be well known, such as precision instruments and sample-and-hold amplifiers.

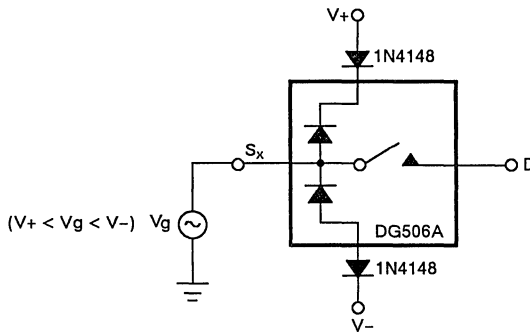
The tested supply range of the DGP508A is increased beyond that of the DG508A, up to ±20 V and down to ±10.8 V. This allows the switches to have guaranteed performance limits with power supplies as low as ±12 V (±10%), ±15 V (±10%), and up to ±20 V.

**APPLICATIONS**

**Overvoltage Protection**

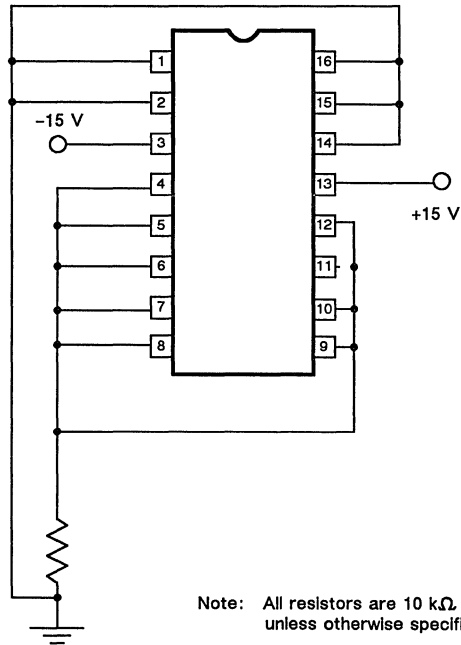
A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal  $V+$  or  $V-$  value. In this

case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference  $V_S - (V-)$  doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below  $V+$  and 1 V above  $V-$ , but it preserves the low channel resistance and low leakage characteristics of the device.



Overvoltage Protection Using Blocking Diodes

## BURN-IN DIAGRAM



Note: All resistors are 10 k $\Omega$  unless otherwise specified

## 8-Channel/Dual 4-Channel CMOS Analog Multiplexers

### FEATURES

- TTL & CMOS Direct Control Over Military Temperature Range
- Low Power (30 mW typ.)
- Break-Before-Make Switching
- 44 V Power Supply Rating

### BENEFITS

- Easily Interfaced
- Reduced Power Consumption
- Reduced System Cross-Talk
- Environmentally Rugged

### APPLICATIONS

- Communication Systems
- Multiplexing Reference Signals
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing

### DESCRIPTION

DG508A and DG509A are 8- and dual 4-channel analog multiplexers, respectively, designed for selecting 1 of 8 (or 4) analog input signals and connecting it to a common output or, conversely, routing an analog signal to 1 of 8 (or 4) output loads. Break-before-make switching action protects against momentary shorting of the input signals.

The DG508A, an 8-channel single-ended analog multiplexer, is designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address ( $A_0$ ,  $A_1$ ,  $A_2$ ). DG509A, a dual 4-channel analog multiplexer, is designed to connect 1 of 4 dual inputs to a common dual output as determined by its 2-bit binary address ( $A_0$ ,  $A_1$ ) logic.

A channel in the ON state conducts current equally well in both directions (bidirectional switches). In the OFF state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF. All control inputs, address ( $A_X$ ) and enable (EN) are

TTL or CMOS compatible over the full specified operating temperature range.

Designed in the Siliconix Plus 40 process, the absolute maximum voltage rating is extended to 44 Volts, allowing increased operating headroom for standard  $\pm 15$  V signal swings and operation with  $\pm 20$  V supplies. An epitaxial layer prevents latch up.

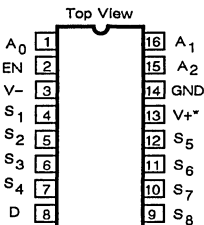
Both DG508A and DG509A are available in dual-in-line, CerDIP, plastic DIP and small outline packages, and are specified for operation over the military, A suffix (-55 to 125°C), industrial, B and D suffix (-25, -40 to 85°C), and commercial, C suffix (0 to 70°C), temperature ranges.

For higher precision applications, the DGP508A/DGP509A multiplexers are recommended. For applications requiring address data latching, the DG528/DG529 is recommended. For wideband/video routing and multiplexing applications, the DG538 is recommended.

For more information, refer to Siliconix Application Notes AN75-1 and AN73-2.

### PIN CONFIGURATION

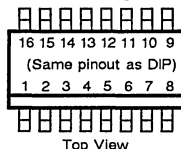
Dual-In-Line Package



Order Numbers:

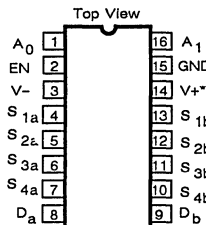
CerDIP: DG508AAK, DG508ABK, DG508ACK  
Plastic: DG508ACJ

SO Package



Order Number:  
DG508ADY

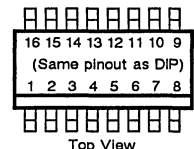
Dual-In-Line Package



Order Numbers:

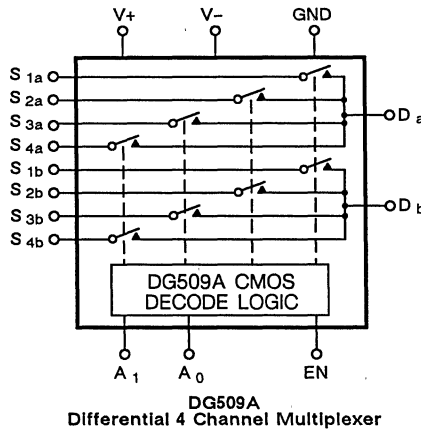
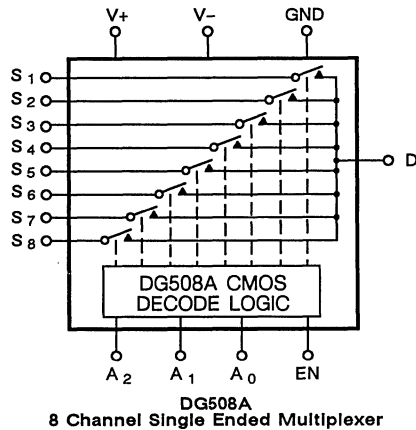
CerDIP: DG509AAK, DG509ABK, DG509ACK  
Plastic: DG509ACJ

SO Package



Order Number:  
DG509ADY

## FUNCTIONAL BLOCK DIAGRAM



### ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-	Operating Temperature (A Suffix) .....	-55 to 125°C
V+ .....	(B Suffix) .....	-25 to 85°C
GND .....	(C Suffix) .....	0 to 70°C
Digital Inputs <sup>h</sup> , V <sub>S</sub> , V <sub>D</sub> .....	(D Suffix) .....	-40 to 85°C
(v-) -2 V to (V+) +2 V or	Storage Temperature (K Suffix) .....	-65 to 150°C
20 mA, whichever occurs first.	(J and Y Suffix) .....	-65 to 125°C
Current (Any Terminal, Except S or D) .....	Power Dissipation (Package) *	
30 mA	16-Pin Ceramic DIP** .....	900 mW
Continuous Current, S or D .....	16-Pin Plastic DIP*** .....	470 mW
20 mA	16-Pin SO**** .....	900 mW
Peak Current, S or D		
(Pulsed at 1 ms, 10% Duty Cycle Max) .....	* All leads soldered or welded to PC board.	
40 mA	** Derate 12 mW/°C above 75°C.	
	*** Derate 6.3 mW/°C above 75°C.	
	**** Derate 7.7 mW/°C above 75°C.	

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ GND = 0 V	LIMITS						UNIT		
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		B, C, D SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SWITCH</b>											
Analog Signal Range <sup>c, h</sup>	$V_{\text{ANALOG}}$		1,2,3		-15	15	-15	15		V	
Drain-Source <sup>e</sup> ON Resistance	$r_{\text{DS(ON)}}$	$V_{\text{D}} = \pm 10\text{ V}$ , $V_{\text{AL}} = 0.8\text{ V}$ $I_{\text{S}} = -200\ \mu\text{A}$ , $V_{\text{AH}} = 2.4\text{ V}$	1,3 2			400 500		450 550		$\Omega$	
Greatest Change In $r_{\text{DS(ON)}}$ Between Channels <sup>f</sup>	$\frac{\Delta}{r_{\text{DS(ON)}}$	$-10\text{ V} < V_{\text{S}} < 10\text{ V}$	1	6						%	
Source OFF Leakage Current	$I_{\text{S(OFF)}}$	$V_{\text{EN}} = 0\text{ V}$	$V_{\text{S}} = \pm 10\text{ V}$ $V_{\text{D}} = \mp 10\text{ V}$	1 2	-1 -50	1 50	-5 -50	5 50		nA	
Drain OFF Leakage Current	DG508A		$V_{\text{D}} = \pm 10\text{ V}$ $V_{\text{S}} = \mp 10\text{ V}$	1 2	-10 -200	10 200	-20 -200	20 200			
	DG509A		$V_{\text{D}} = \pm 10\text{ V}$ $V_{\text{S}} = \mp 10\text{ V}$	1 2	-10 -100	10 100	-20 -100	20 100			
Drain ON <sup>e,g</sup> Leakage Current	DG508A		$V_{\text{S}} = V_{\text{D}} = \pm 10\text{ V}$ $V_{\text{AL}} = 0.8\text{ V}$ $V_{\text{AH}} = 2.4\text{ V}$		1 2	-10 -200	10 200	-20 -200	20 200		
	DG509A			1 2	-10 -100	10 100	-20 -100	20 100			
<b>INPUT</b>											
Logic Input Current <sup>h</sup> Input Voltage High	$I_{\text{AH}}$	$V_{\text{A}} = 2.4\text{ V}$		1 2	-0.002	-10 -30		-10 -30			$\mu\text{A}$
		$V_{\text{A}} = 15\text{ V}$	1 2	0.006		10 30		10 30			
Logic Input Current <sup>h</sup> Input Voltage Low	$I_{\text{AL}}$	$V_{\text{EN}} = 0\text{ V}$ or $2.4\text{ V}$ , $V_{\text{A}} = 0\text{ V}$	1 2	-0.002	-10 -30		-10 -30				
<b>DYNAMIC</b>											
Switching Time of Multiplexer	$t_{\text{TRANS}}$	See Figure 1	1	0.6		1				$\mu\text{s}$	
Break-Before-Make Interval	$t_{\text{OPEN}}$	See Figure 3	1	0.2							
Enable Turn ON Time	$t_{\text{ON(EN)}}$	See Figure 2	1	1		1.5					
Enable Turn OFF Time	$t_{\text{OFF(EN)}}$		1	0.4		1.0					
Charge Injection	Q		1	6						pC	
OFF Isolation		$V_{\text{EN}} = 0\text{ V}$ , $R_{\text{L}} = 1\text{ k}\Omega$ $C_{\text{L}} = 15\text{ pF}$ , $V_{\text{S}} = 7\text{ V}_{\text{RMS}}$ $f = 500\text{ kHz}$	1	68						dB	
Logic Input Capacitance	$C_{\text{in}}$	$f = 1\text{ MHz}$	1	8						pF	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		B, C, D SUFFIX			
			2=125,85°C		-55 to 125°C					
		3=-55,-40°C		MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
DYNAMIC (Cont'd)										
Source OFF Capacitance		C <sub>S(OFF)</sub>	V <sub>EN</sub> = 0 V f = 140 kHz	V <sub>S</sub> = 0	1	5				pF
Drain OFF Capacitance	DG508A	C <sub>D(OFF)</sub>		V <sub>D</sub> = 0	1	25				
	DG509A				1	12				
SUPPLY										
Positive Supply Current		I <sub>+</sub>	V <sub>EN</sub> = 0 V or 2.4 V	1	1.3		2.4		2.4	mA
Negative Supply Current		I <sub>-</sub>		1	-0.7	-1.5		-1.5		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Sequence each switch ON.

$$f. \Delta r_{DS(ON)} = \left( \frac{r_{DS(ON) \text{ MAX}} - r_{DS(ON) \text{ MIN}}}{r_{DS(ON) \text{ AVE}}} \right)$$

- g. I<sub>D(ON)</sub> is leakage from driver into "ON" switch.
- h. Signals on S<sub>x</sub>, D<sub>x</sub> or IN<sub>x</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

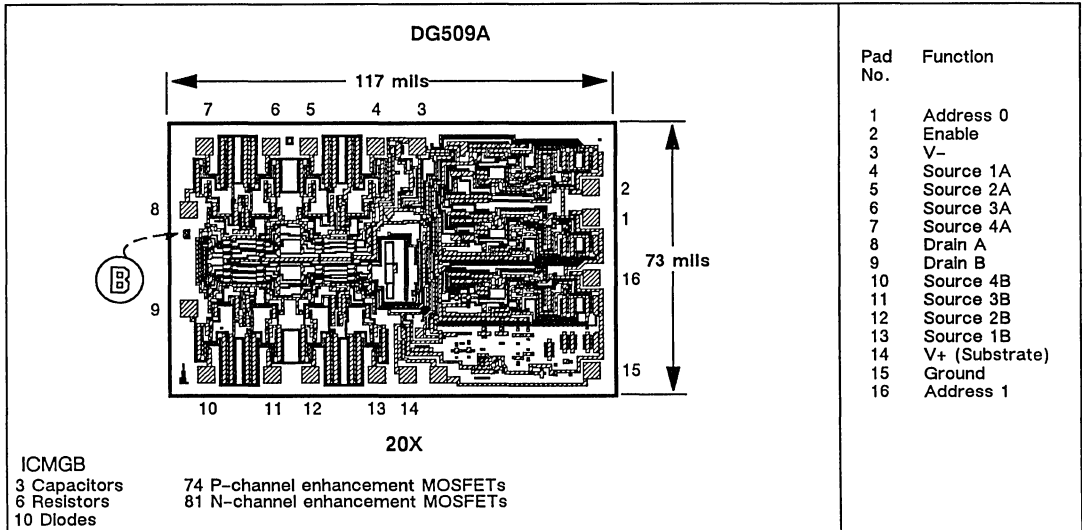
**DIE TOPOGRAPHY**

Pad No.	Function
1	Address 0
2	Enable
3	V <sub>-</sub>
4	Source 1
5	Source 2
6	Source 3
7	Source 4
8	Drain
9	Source 8
10	Source 7
11	Source 6
12	Source 5
13	V <sub>+</sub> (Substrate)
14	Ground
15	Address 2
16	Address 1

ICMGA  
 4 Capacitors  
 7 Resistors  
 12 Diodes

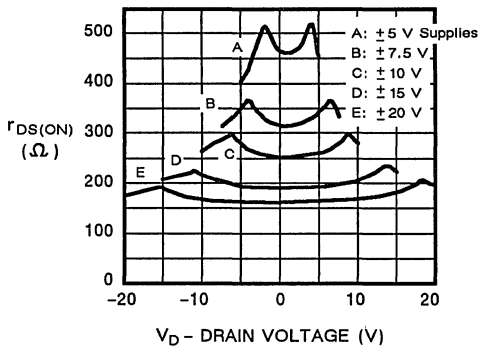
20X  
 85 P-channel enhancement MOSFETs  
 89 N-channel enhancement MOSFETs

**DIE TOPOGRAPHY (Cont'd)**

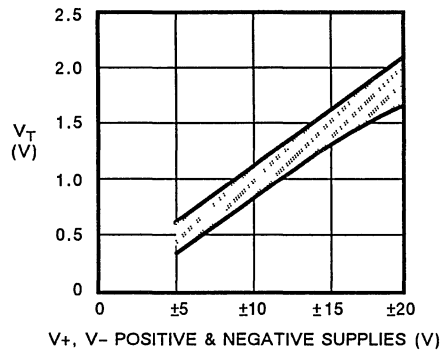


**TYPICAL CHARACTERISTICS**

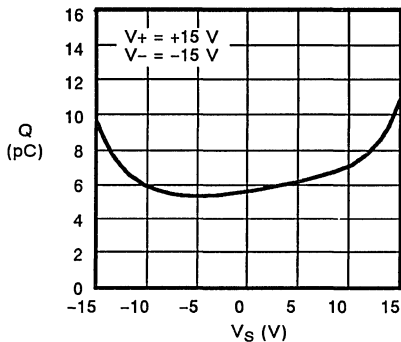
$r_{DS(ON)}$  vs.  $V_D$  and Power Supply



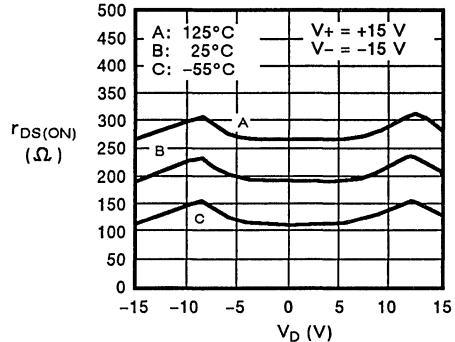
Input Switching Threshold vs.  $V_+$  and  $V_-$  Supply Voltages



Charge Injection vs. Analog Voltage ( $V_S$ )

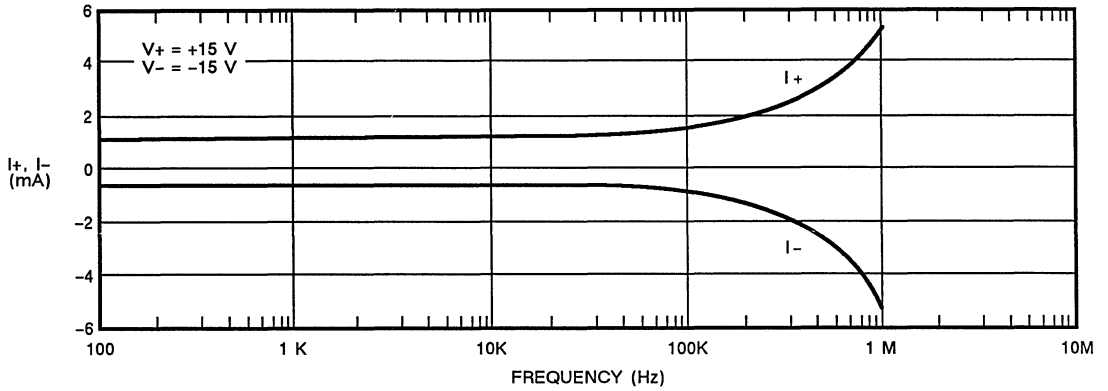


$r_{DS(ON)}$  vs.  $V_D$  and Temperature

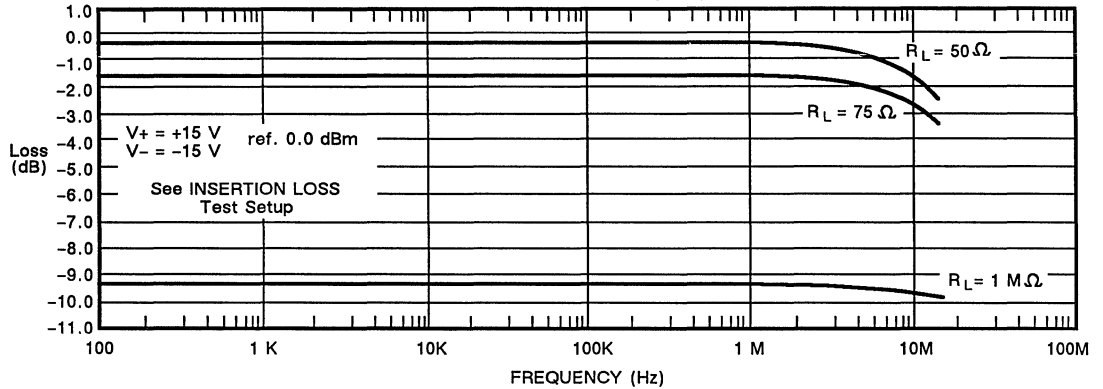


## TYPICAL CHARACTERISTICS (Cont'd)

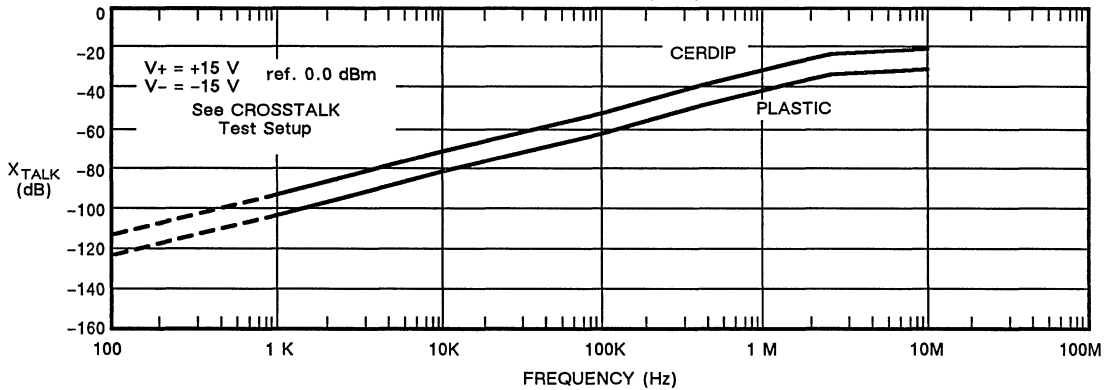
Supply Current vs. Switching Frequency



Insertion Loss vs. Frequency

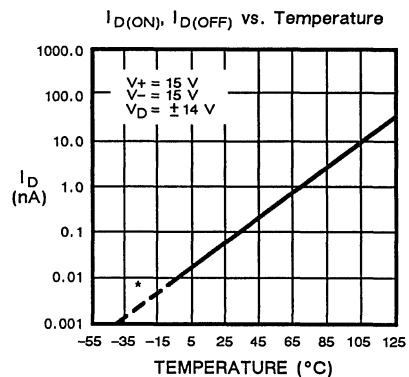
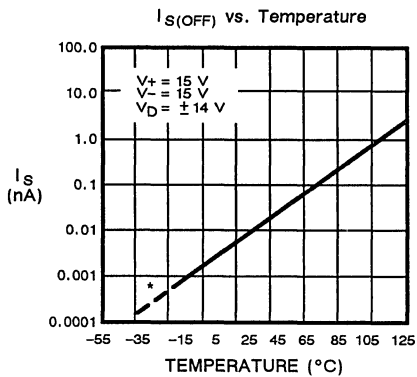
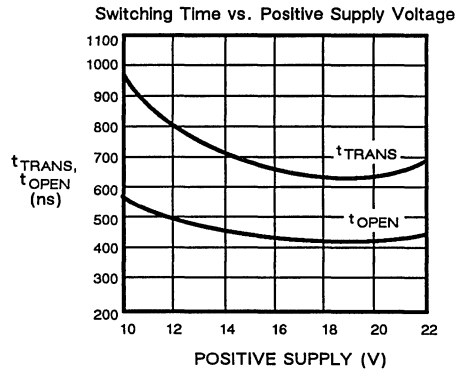
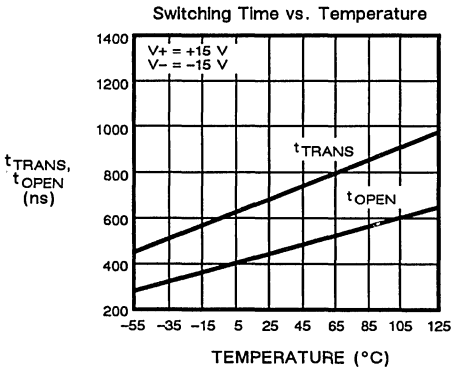
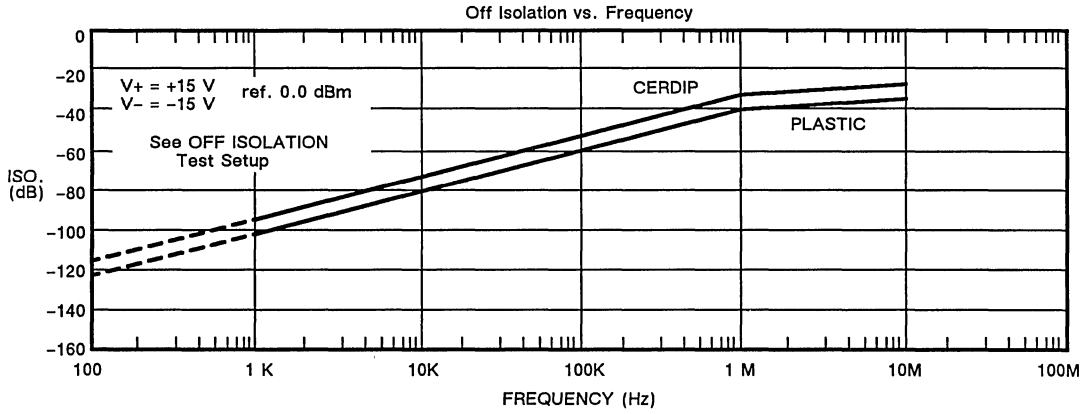


Crosstalk vs. Frequency



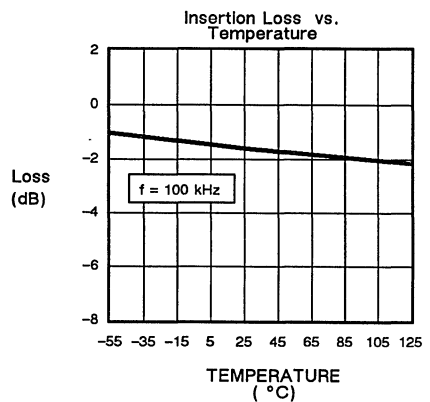
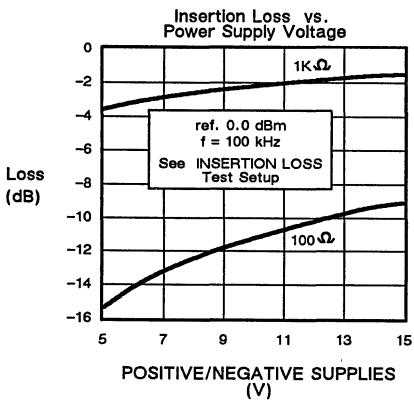
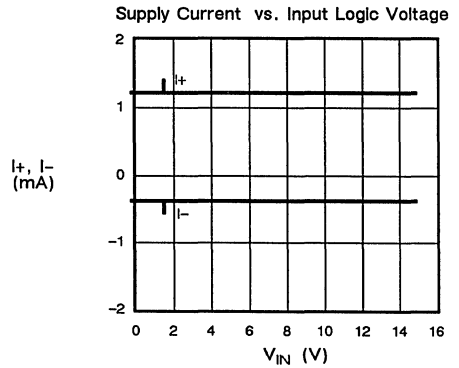
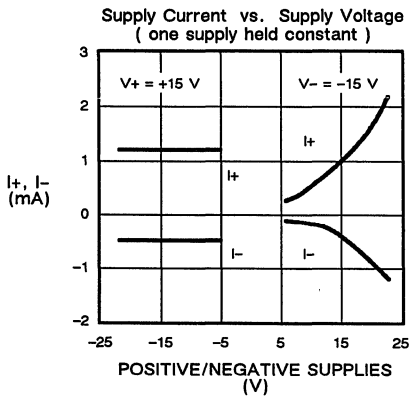
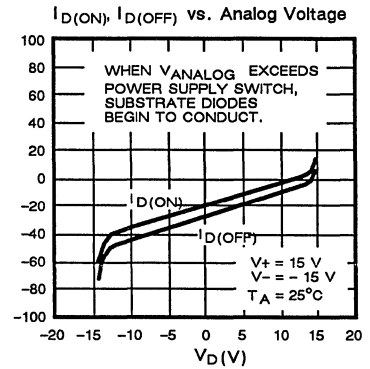
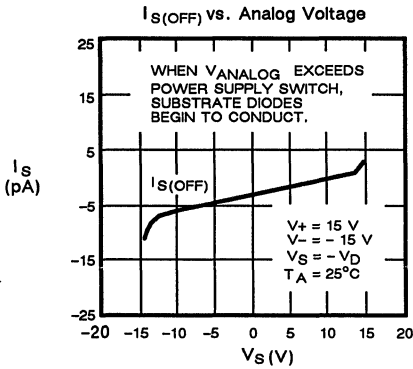


**TYPICAL CHARACTERISTICS (Cont'd)**



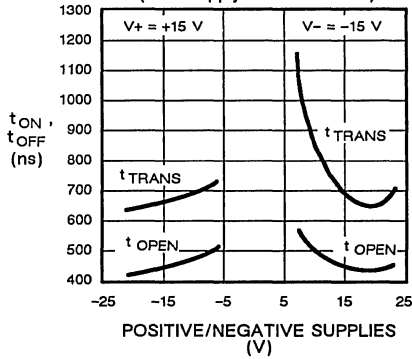
\* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

## TYPICAL CHARACTERISTICS (Cont'd)

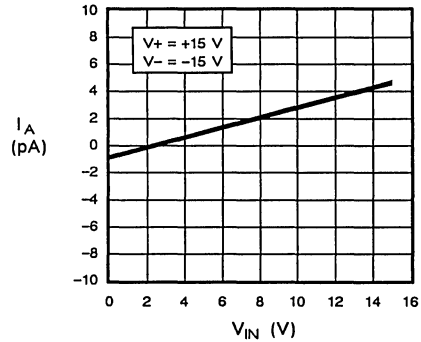


**TYPICAL CHARACTERISTICS (Cont'd)**

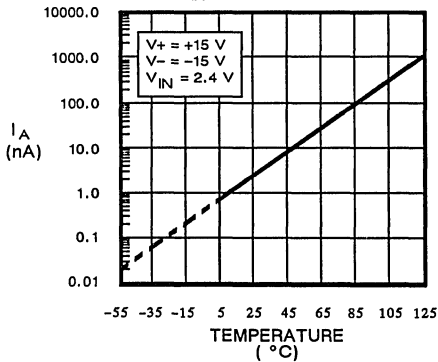
Switching Time vs. Power Supply Voltage  
(one supply held constant)



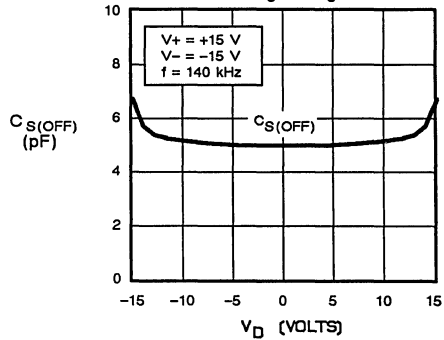
Input Logic Current vs. Input Logic Voltage



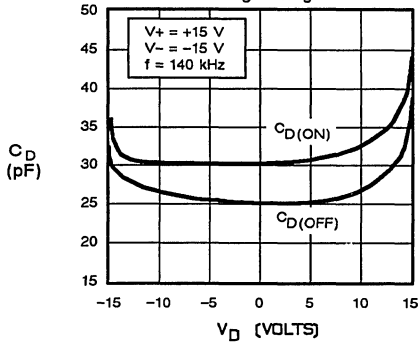
$I_{IN}$  vs. Temperature



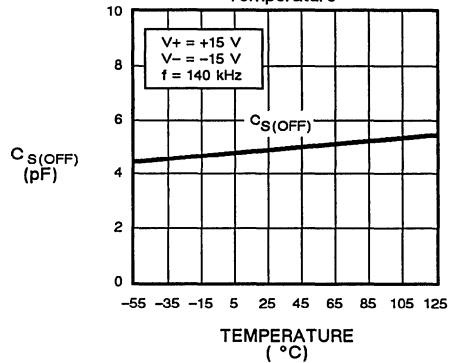
$C_{S(OFF)}$  vs. Analog Voltage



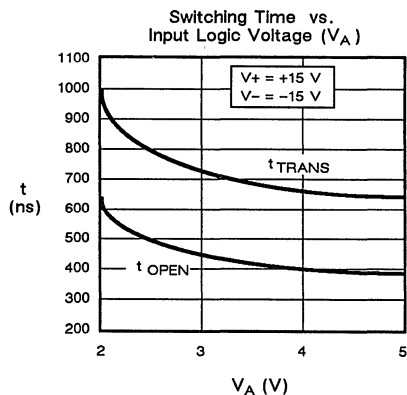
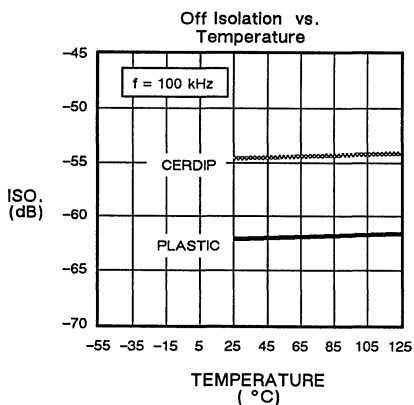
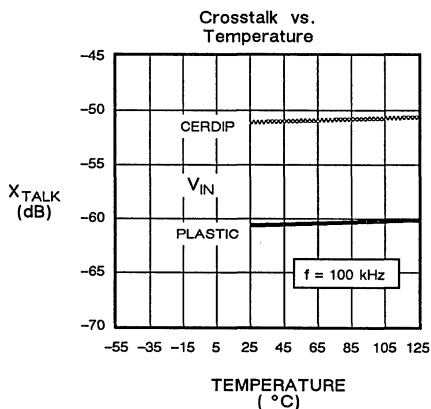
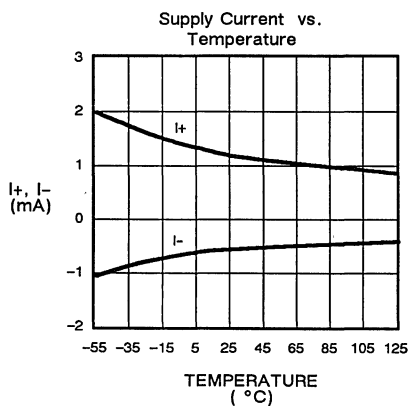
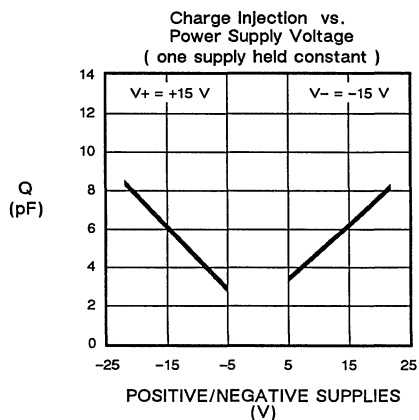
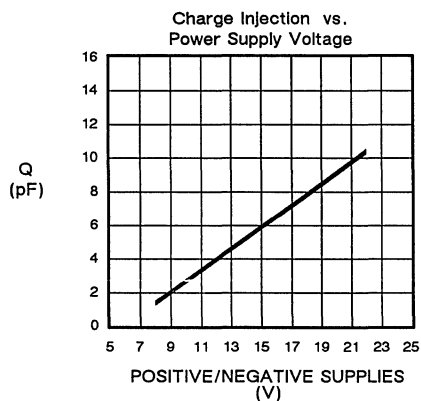
$C_{D(ON)}$ ,  $C_{D(OFF)}$  vs. Analog Voltage



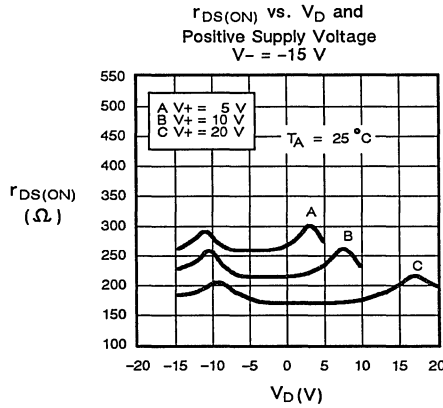
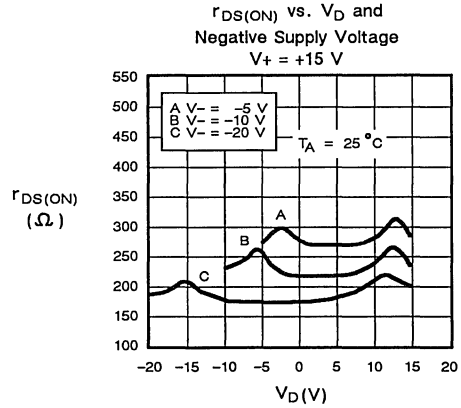
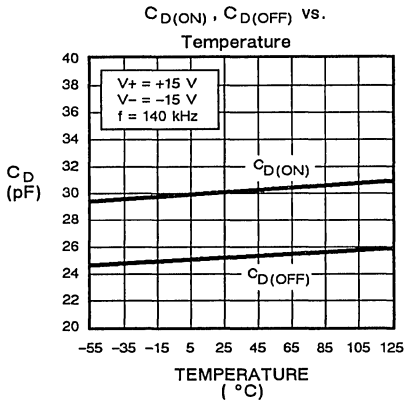
$C_{S(OFF)}$  vs. Temperature



## TYPICAL CHARACTERISTICS (Cont'd)



**TYPICAL CHARACTERISTICS (Cont'd)**



**5**

**TRUTH TABLES**

**DG508A**

$A_2$	$A_1$	$A_0$	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

**DG509A**

$A_1$	$A_0$	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" =  $V_{AL} \leq 0.8\text{ V}$ , Logic "1" =  $V_{AH} \geq 2.4\text{ V}$

## t<sub>TRANSITION</sub> TIME TEST CIRCUIT

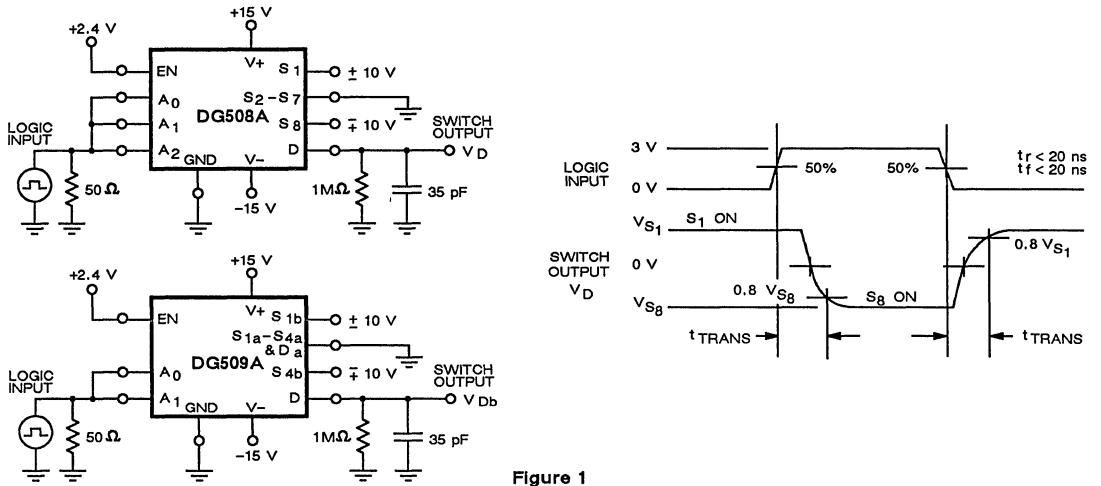


Figure 1

## t<sub>ON(EN)</sub> AND t<sub>OFF(EN)</sub> TIME TEST CIRCUIT

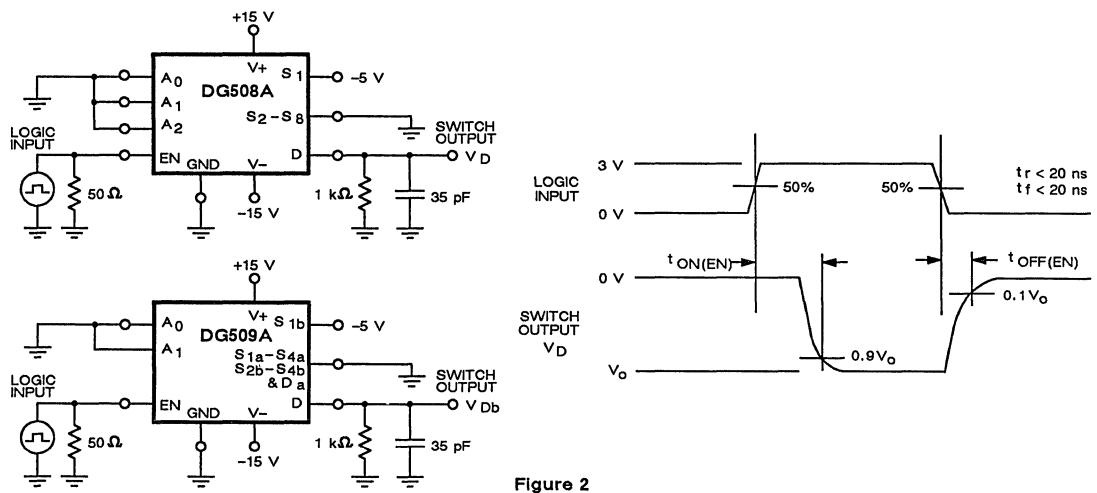


Figure 2

## t<sub>OPEN</sub> TIME TEST CIRCUIT

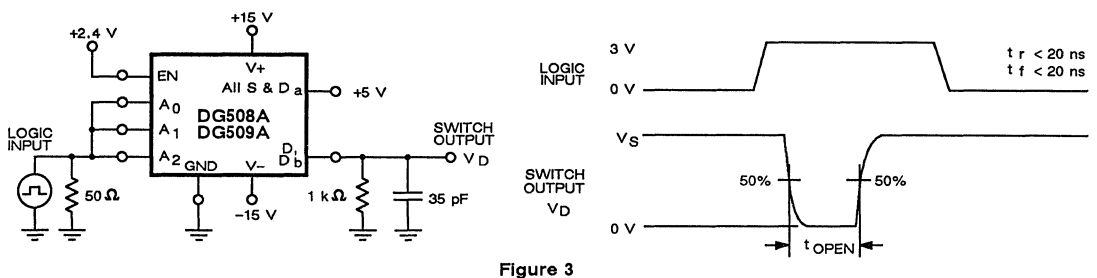


Figure 3

## APPLICATION HINTS\*

### Logic Inputs

Logic input circuitry protects the input MOS gate from static transients. A series MOS device shuts off when  $V_{IN}$  exceeds the positive power supply. Negative transients are clamped to ground by a diode clamp.

The input voltage characteristics have a current spike occurring at the transition voltage when the logic goes from  $V_{INH}$  to  $V_{INL}$ .

If a series resistor is used for additional static protection, it should be limited to less than 9.1 k  $\Omega$  to insure switching with worst case current spikes.

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15**	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
10	-10	2.4/0.6	-10 to 10
8	-8	2.4/0.4	-8 to 8

\* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

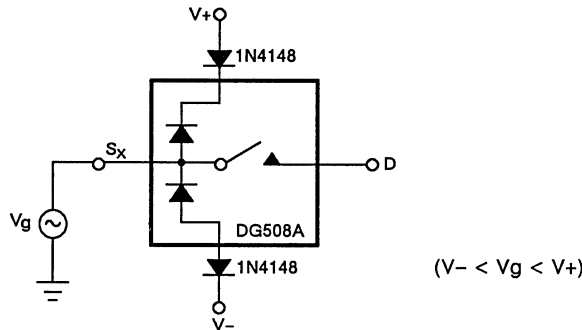
\*\* Electrical Characteristics chart based on V+ = +15 V, V- = -15 V.

\*\*\* Operation below  $\pm 8$  V is not recommended to the shift in  $V_{INL(MAX)}$ .

### Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this

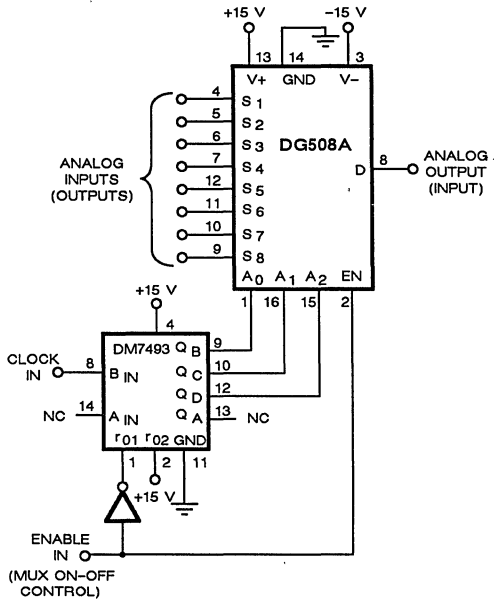
case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference  $V_S - (V-)$  doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.



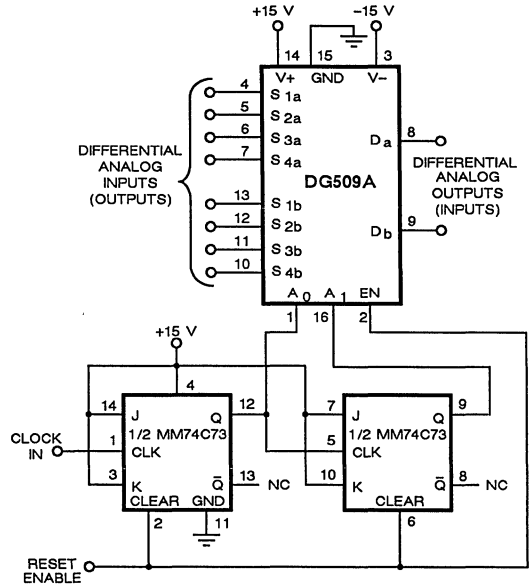
Overvoltage Protection Using Blocking Diodes

## APPLICATIONS

### 8 Channel Sequential Mux/Demux



### Differential 4 Channel Sequential Mux/Demux



Truth Table

	ENABLE	MUX SEQUENCE RATE	MUX INPUTS		DG508A SWITCH PAIR STATES (-DENOTES OFF)												
			A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>	S <sub>6</sub>	S <sub>7</sub>	S <sub>8</sub>				
<b>D G 5 0 9 A</b>	0	0	X	X	X	-	-	-	-	-	-	-	-	-	-	-	-
	1	0	0	0	0	ON	-	-	-	-	-	-	-	-	-	-	-
	1	1 pulse	1	0	0	-	ON	-	-	-	-	-	-	-	-	-	-
	1	2 pulses	0	1	0	-	-	ON	-	-	-	-	-	-	-	-	-
	1	3 pulses	1	1	0	-	-	-	ON	-	-	-	-	-	-	-	-
1	4 pulses	0	0	1	-	-	-	-	ON	-	-	-	-	-	-	-	
1	5 pulses	1	0	1	-	-	-	-	-	ON	-	-	-	-	-	-	
1	6 pulses	0	1	1	-	-	-	-	-	-	ON	-	-	-	-	-	
1	7 pulses	1	1	1	-	-	-	-	-	-	-	ON	-	-	-	-	
1	8 pulses	0	0	0	ON	-	-	-	-	-	-	-	-	-	-	-	



## 16-Channel and Dual 8-Channel Latchable Multiplexers

### FEATURES

- TTL Compatible
- 44 V Power Supply Rating
- On-board Address Latches
- $r_{DS(ON)} < 400 \Omega$
- Break-Before-Make

### BENEFITS

- Easily Interfaced
- Increased Analog Signal Range
- Microprocessor Bus Compatible
- Improved System Accuracy
- Reduced Crosstalk

### APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics And Military Systems
- Communication Systems
- Microprocessor Controlled Systems
- Audio Signal Multiplexing

### DESCRIPTION

DG526 and DG527 are 16 and 8-channel analog multiplexers, respectively, with on-chip address and control latches to simplify design in microprocessor based applications. Break-Before-Make switching action protects against momentary shorting of the input signals. Designed on the Siliconix PLUS-40 CMOS process, each bidirectional switch features low 400  $\Omega$  ON resistance over the full analog range, and will block signals to 30 V peak-to-peak in the unselected channels. All logic levels are TTL-compatible. An epitaxial layer prevents latch up.

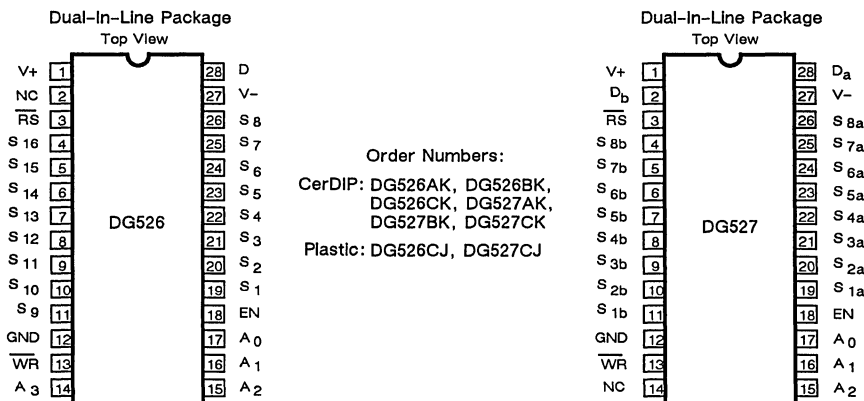
DG526 is a 16-channel single-ended analog multiplexer designed to connect 1 of 16 inputs to a common output as determined by a 4-bit binary address ( $A_0, A_1, A_2, A_3$ ). DG527, an 8-channel

dual analog multiplexer, is designed to connect 1 of 8 differential inputs to a common differential output as determined by its 3-bit binary address ( $A_0, A_1, A_2$ ) logic.

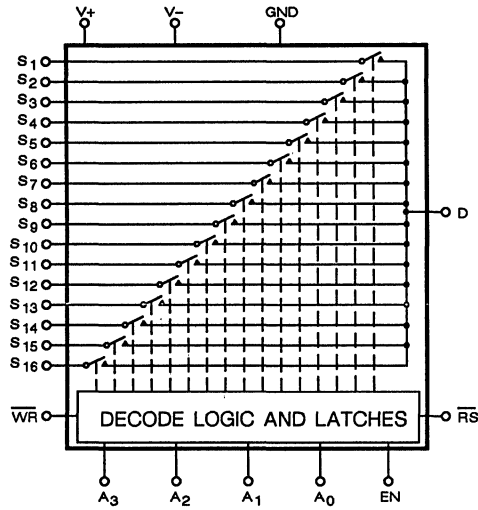
The on-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE. The DG526 is available in 28-pin CerDIP in the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ), industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ) temperature ranges, and in the plastic DIP for commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ) temperature operation.

For more information on the DG526 and DG527, please refer to Siliconix Application Note AN83-4.

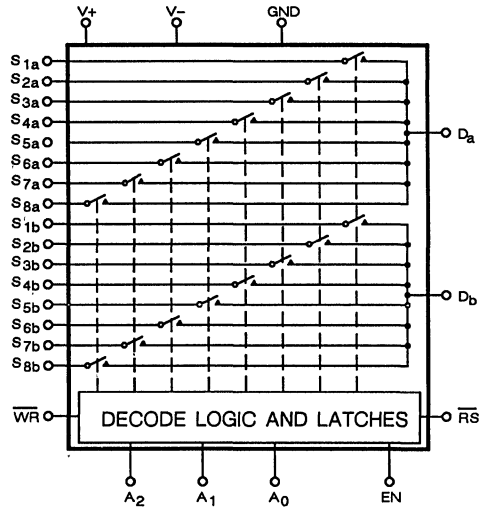
### PIN CONFIGURATION



## FUNCTIONAL BLOCK DIAGRAM



**DG526**  
16 Channel Single Ended Multiplexer



**DG527**  
Differential 8 Channel Multiplexer

## ABSOLUTE MAXIMUM RATINGS

### Voltage Referenced to V-

V+	44 V
GND	25 V
Digital Inputs, $V_S$ , $V_D^h$	(V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first.
Current (Any Terminal Except S or D)	30 mA
Continuous Current, S or D	20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max)	40 mA

Operating Temperature (A Suffix)	-55 to 125°C
(B Suffix)	-25 to 85°C
(C Suffix)	0 to 70°C
Storage Temperature (A & B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C

### Power dissipation (Package)\*

28-Pin CerDIP DIP**	1046 mW
28-Pin Plastic DIP**	1046 mW

\* All leads soldered or welded to PC board.

\*\* Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0, WR = 0 RS = 2.4 V	LIMITS				UNIT	
			1=25° C 2=125,70,85 °C 3=-55,-25,0 °C		ALL SUFFIXES			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>								
Analogue Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	V	
Drain-Source <sup>e</sup> ON Resistance	r <sub>DS(ON)</sub>	V <sub>D</sub> = ±10 V, V <sub>AL</sub> = 0.8 V I <sub>S</sub> = -200 μA, V <sub>AH</sub> = 2.4 V	1, 3 2	250		400 500	Ω	
Greatest Change In r <sub>DS(ON)</sub> Between Channels <sup>f</sup>	Δ r <sub>DS(ON)</sub>	-10 V < V <sub>S</sub> < 10 V	1	6			%	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>EN</sub> = 0 V	V <sub>S</sub> = ±10 V V <sub>D</sub> = ∓10 V	1 2	0.02	-1 -50	1 50	nA
Drain OFF Leakage Current	DG526 DG527		V <sub>D</sub> = ±10 V V <sub>S</sub> = ∓10 V	1 2	0.2	-10 -300	10 300	
	V <sub>D</sub> = ±10 V V <sub>S</sub> = ∓10 V		1 2	0.2	-10 -200	10 200		
Drain ON Leakage Current <sup>e,g</sup>	DG526 DG527	V <sub>S</sub> = V <sub>D</sub> = ±10 V V <sub>EN</sub> = 2.4 V V <sub>AL</sub> = 0.8 V V <sub>AH</sub> = 2.4 V	1 2	0.2	-10 -300	10 300		
	1 2		0.2	-10 -200	10 200			
<b>INPUT</b>								
Logic Input Current Input Voltage High	I <sub>AH</sub>	V <sub>A</sub> = 2.4 V	1 2	0.02	-10 -30	20 30	μA	
		V <sub>A</sub> = 15 V	1 2	0.02	-10 -30	10 30		
Logic Input Current Input Voltage Low	I <sub>AL</sub>	V <sub>EN</sub> = 0 or 2.4 V, V <sub>A</sub> = 0 V RS = 0 V, WR = 0 V	1 2	0.01	-10 -30	10 30		
<b>DYNAMIC</b>								
Switching Time of Multiplexer	t <sub>TRANS</sub>	See Figure 3	1	0.65		1	μs	
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 5	1	0.2				
Enable and Write Turn ON Time	t <sub>ON(EN,WR)</sub>	See Figure 4 and 6	1	0.7		1.5		
Enable and Reset Turn OFF Time	t <sub>OFF(EN,RS)</sub>	See Figure 4 and 7	1	0.4		1		
Charge Injection	Q	See Figure 8	1	10			pC	
OFF Isolation		V <sub>EN</sub> = 0, R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF, V <sub>S</sub> = 7 V <sub>RMS</sub> f = 500 kHz	1	55			dB	
Logic Input Capacitance	C <sub>In</sub>	f = 1 MHz	1	6			pF	

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0, WR = 0 RS = 2.4 V	LIMITS				UNIT	
			1=25° C 2=125,70,85 °C 3=-55,-25,0 °C		ALL SUFFIXES			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC (Cont'd)</b>								
Source OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>EN</sub> = 0 f = 140 kHz	V <sub>S</sub> = 0	1	10		PF	
Drain OFF Capacitance	DG526		C <sub>D(OFF)</sub>	V <sub>D</sub> = 0	1	65		
	DG527				1	35		
<b>MINIMUM INPUT TIMING REQUIREMENTS</b>								
WR Pulse Width	t <sub>WV</sub>	See Figure 1	1,2,3	260	300		ns	
A <sub>X</sub> , EN Data Valid to WR	t <sub>DW</sub>	(Stabilization Time) See Figure 1	1,2,3	150	180			
A <sub>X</sub> , EN Data Valid after WR	t <sub>WD</sub>	(Hold Time) See Figure 1	1,2,3	20	30			
RS Pulse Width <sup>l</sup>	t <sub>RS</sub>	See Figure 2 V <sub>S</sub> = 5 V	1,2,3	350	500			
<b>SUPPLY</b>								
Positive Supply Current	I <sub>+</sub>	V <sub>EN</sub> = 0, V <sub>A</sub> = 0	1, 2,3	2.0		3.0 4.5	mA	
Negative Supply Current	I <sub>-</sub>		1, 2,3	-1.2	-2.0 -3.2			

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Sequence each switch ON.

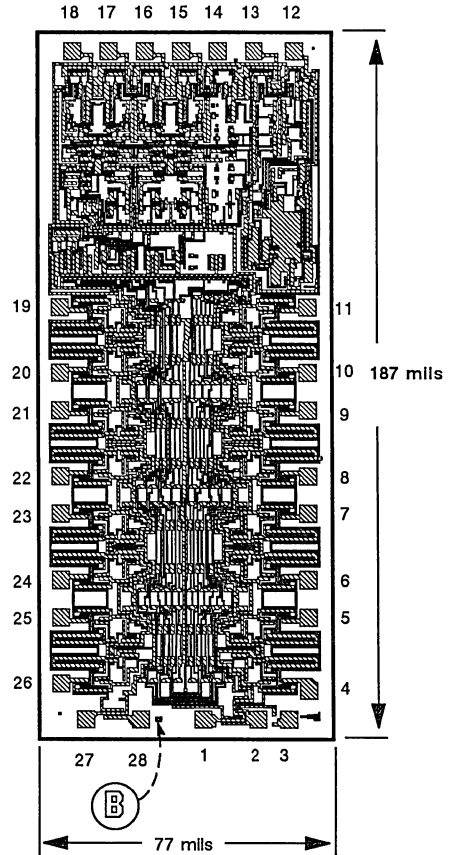
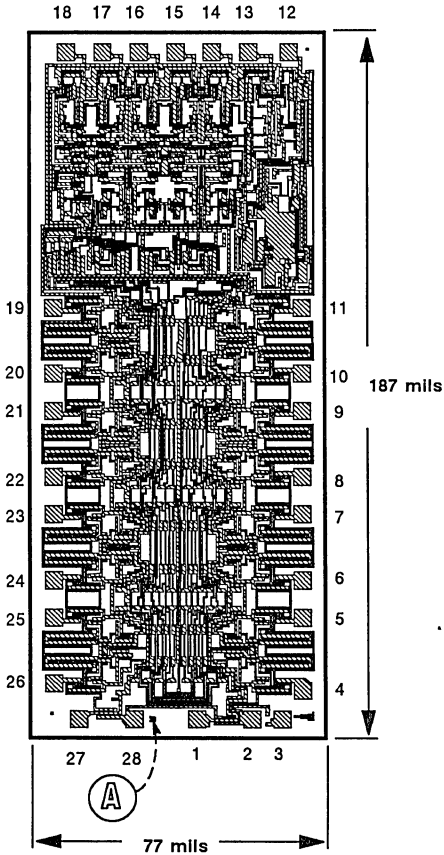
$$f. \Delta r_{DS(ON)} = \left( \frac{r_{DS(ON) \text{ MAX}} - r_{DS(ON) \text{ MIN}}}{r_{DS(ON) \text{ AVE}}} \right)$$

- g. I<sub>D(ON)</sub> is leakage from driver into "ON" switch.
- h. Signals on S<sub>X</sub>, D<sub>X</sub>, IN<sub>X</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- i. Period of Reset (RS) pulse must be at least 50 μs during or after power ON.

**DIE TOPOGRAPHIES**

**DG526**

**DG527**



**20X**

**20X**

Pad No.	Function
1	V+ (substrate)
2	No connection
3	RS
4	S <sub>16</sub>
5	S <sub>15</sub>
6	S <sub>13</sub>
7	S <sub>14</sub>
8	S <sub>12</sub>
9	S <sub>11</sub>
10	S <sub>10</sub>
11	S <sub>9</sub>
12	GND
13	WR
14	A <sub>3</sub>

Pad No.	Function
15	A <sub>2</sub>
16	A <sub>1</sub>
17	A <sub>0</sub>
18	EN
19	S <sub>1</sub>
20	S <sub>2</sub>
21	S <sub>3</sub>
22	S <sub>4</sub>
23	S <sub>5</sub>
24	S <sub>6</sub>
25	S <sub>7</sub>
26	S <sub>8</sub>
27	V-
28	D

Pad No.	Function
1	V+ (substrate)
2	D
3	RS
4	S <sub>8b</sub>
5	S <sub>7b</sub>
6	S <sub>6b</sub>
7	S <sub>5b</sub>
8	S <sub>4b</sub>
9	S <sub>3b</sub>
10	S <sub>2b</sub>
11	S <sub>9</sub>
12	GND
13	WR
14	No Connection

Pad No.	Function
15	A <sub>2</sub>
16	A <sub>1</sub>
17	A <sub>0</sub>
18	EN
19	S <sub>1a</sub>
20	S <sub>2a</sub>
21	S <sub>3a</sub>
22	S <sub>4a</sub>
23	S <sub>5a</sub>
24	S <sub>6a</sub>
25	S <sub>7a</sub>
26	S <sub>8a</sub>
27	V-
28	D <sub>a</sub>

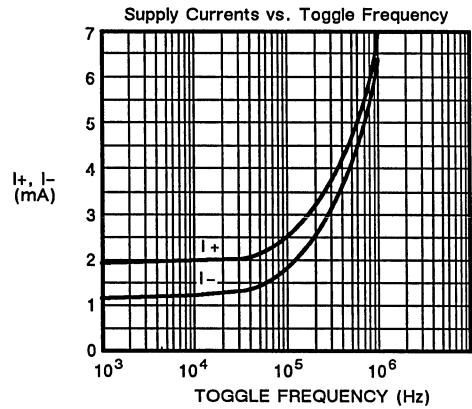
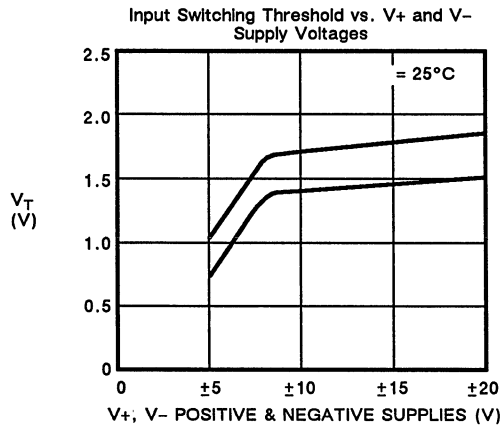
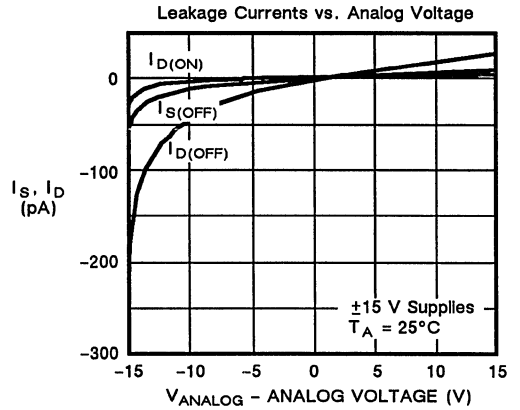
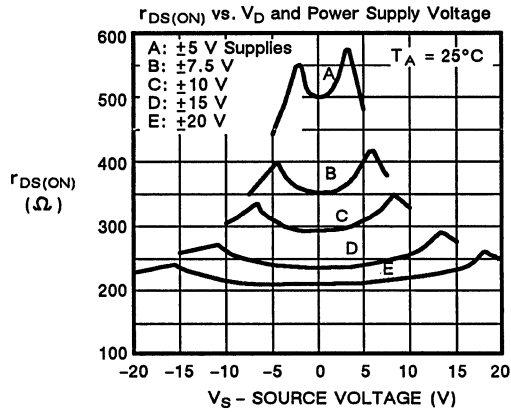
**ICMNA**

- 10 Resistors
- 14 Diodes
- 2 Zener Diodes
- 177 P-channel enhancement MOSFET
- 201 N-channel enhancement MOSFET
- 2 PNP Bipolar Transistors

**ICMNB**

- 9 Resistors
- 16 Diodes
- 2 Zener Diodes
- 164 P-channel enhancement MOSFET
- 189 N-channel enhancement MOSFET
- 2 PNP Bipolar Transistors

## TYPICAL CHARACTERISTICS



**TRUTH TABLES**

**DG526**

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching							
X	X	X	X	X		1	Maintains previous switch condition
Reset							
X	X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation							
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

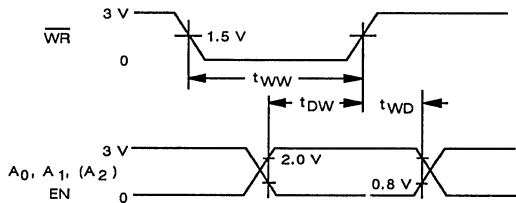
**DG527**

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching						
X	X	X	X		1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

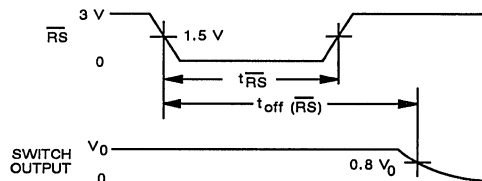
Logic "1":  $V_{AH} > 2.4 \text{ V}$

Logic "0":  $V_{AL} < 0.8 \text{ V}$

**TIMING DIAGRAMS**



**Figure 1**



**Figure 2**

## TRANSITION TIME TEST CIRCUIT

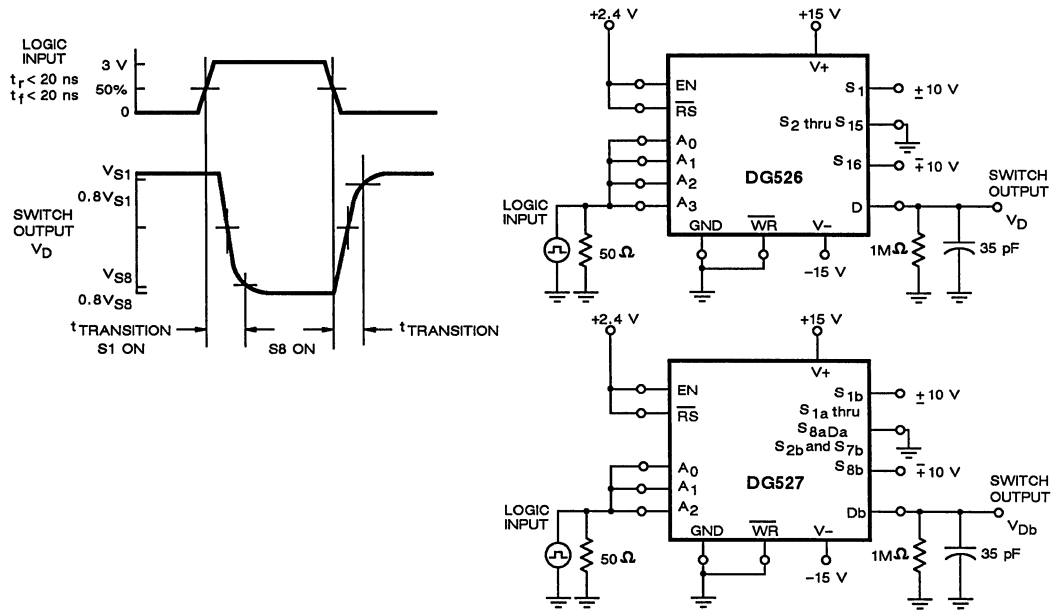


Figure 3

## ENABLE $t_{\text{ON}}/t_{\text{OFF}}$ TIME TEST CIRCUIT

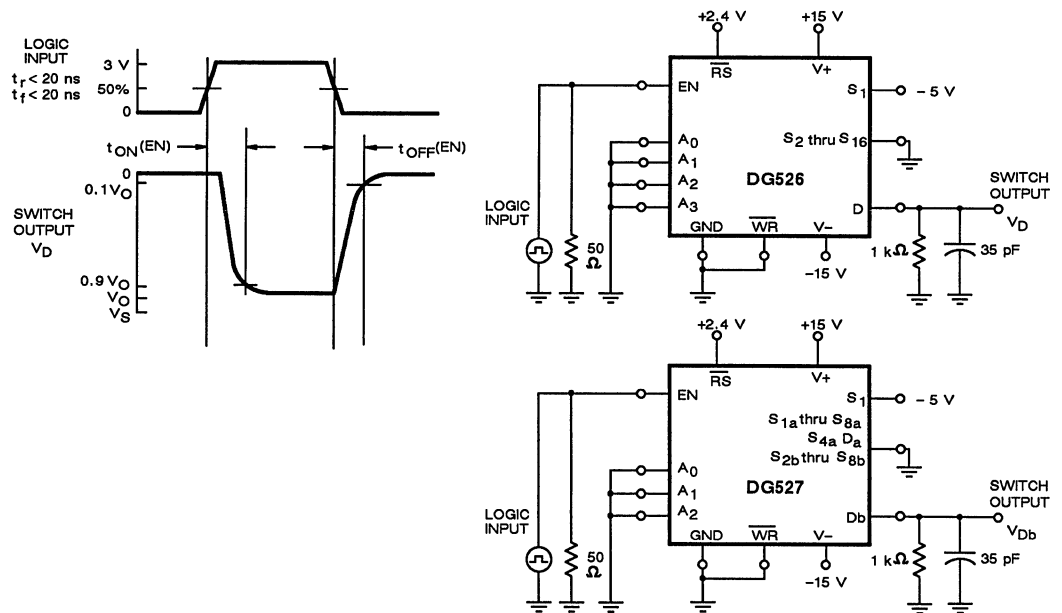


Figure 4



**OPEN TIME (B.B.M.) INTERVAL TEST CIRCUIT**

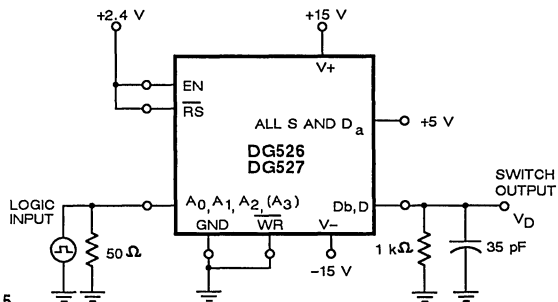
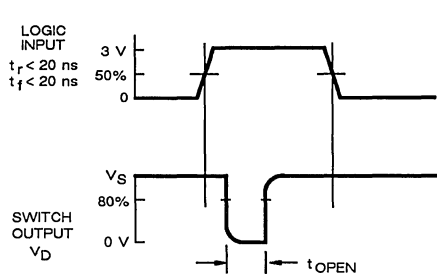


Figure 5

**WRITE TURN-ON TIME  $t_{ON}(\overline{WR})$  TEST CIRCUIT**

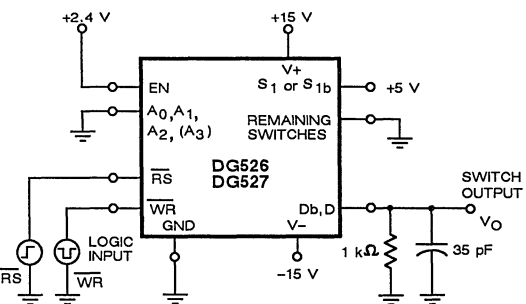
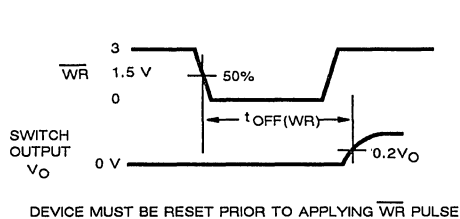


Figure 6

**RESET TURN-OFF TIME  $t_{OFF}(\overline{RS})$  TEST CIRCUIT**

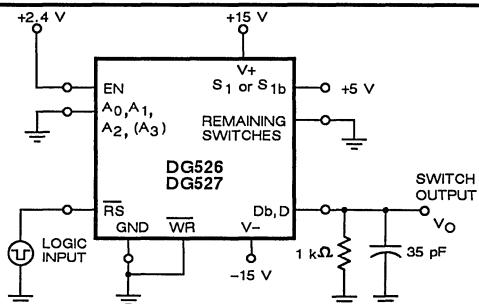
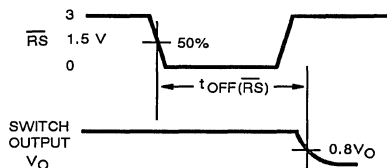
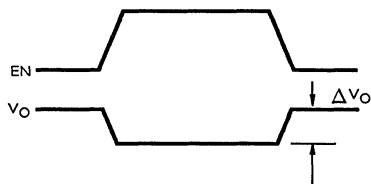
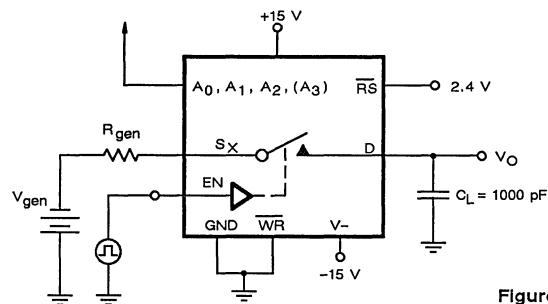


Figure 7

**CHARGE INJECTION TEST CIRCUIT**



$\Delta V_O$  IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE CHARGE IN COULOMBS IS  $Q = C_L \times \Delta V_O$

Figure 8

## DETAILED DESCRIPTION

The internal structure of the DG526 and DG527 includes a 5 V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel N and P-channel MOSFETs (see figure 9).

The input protection on the logic lines  $A_0$ ,  $A_1$ ,  $A_2$ ,  $A_3$ , EN and control lines  $\overline{WR}$ ,  $\overline{RS}$  shown in figure 9 minimize susceptibility to static encountered during handling and operational transients.

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D type latch. The level sensitive D latch continuously places the  $D_X$  input signal on the  $Q_X$  output when the CLK ( $\overline{WR}$ ) input is low, resulting in transparent operation. As soon as CLK ( $\overline{WR}$ ) returns high the latch holds the data last present on

the  $D_X$  input at the  $Q_X$  output, subject to the "Minimum Input Timing Requirements" table.

Following the latches the  $Q_X$  signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full ON/OFF switch operation for any analog signal present between the  $V_+$  and  $V_-$  supply pins.

The enable (EN) pin is used to enable the address latches during the  $\overline{WR}$  pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The  $\overline{RS}$  pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The  $\overline{WR}$  pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

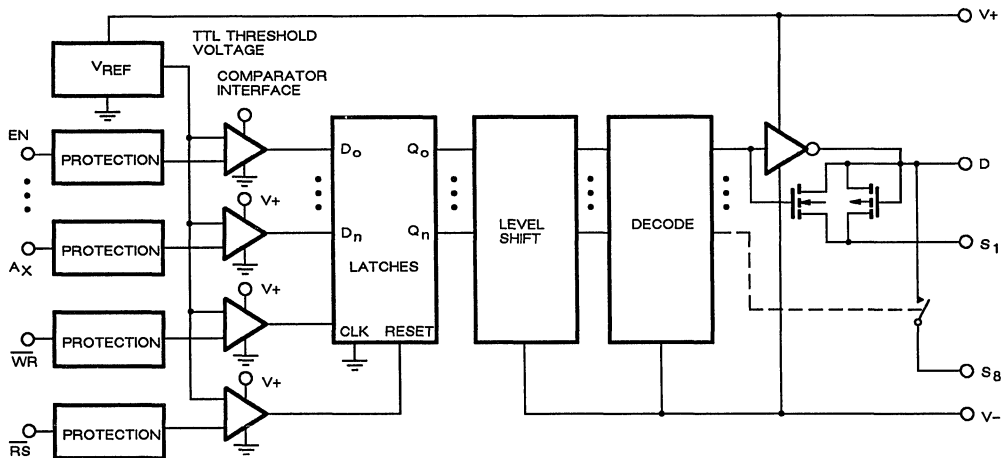


Figure 9. DG526/527 Simplified Internal Structure

## APPLICATIONS

### INTRODUCTION

The DG526 and DG527 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular

switch state (e.g., switch 1 ON) until the microprocessor determines it is necessary to turn different switches ON or turn all switches OFF.

The input latches become transparent when  $\overline{WR}$  is held low; therefore, these multiplexers operate by direct command of the coded switch state on the address inputs. In this mode the DG526 is identical

**APPLICATIONS (Cont'd)**

to the very popular DG506 even sharing the same pin locations. The same is true of the DG527 versus the popular DG507.

**CIRCUIT OPERATION (See Figure 10)**

Initially during system power-up  $\overline{RS}$  would be active LOW maintaining all 16 switches in the OFF state. After  $\overline{RS}$  returned HIGH the DG526 maintains all switches in the OFF state. As soon as the system program was ready to perform a write operation to the address assigned to the DG526, the address decoder would provide a  $\overline{CS}$  active LOW signal which is gated with the WRITE ( $\overline{WR}$ ) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the  $\overline{WR}$  signal returns to the HIGH state, (positive edge) the input latches of the DG526 save the data from the DATA BUS. The coded

information in the  $A_0, A_1, A_2, A_3,$  and EN latches is decoded and the appropriate switch is turned ON.

The EN latch allows all switches to be turned OFF under program control. This becomes useful when two or more DG526s are cascaded to build 32-line and larger analog signal input multiplexers.

Figure 11 illustrates one use of the DG527. Dual multiplexers are generally used with differential or instrumentation amplifiers in process control applications to eliminate errors due to common mode signals. In this circuit however, advantage is taken of the dual multiplexing capability of the switch. This is achieved by using the multiplexer to select pairs of R.C. networks to control the pulse width of the multivibrator. This can be a particularly useful feature in process control applications where there is a requirement for a variable width sample "window" for different control signals.

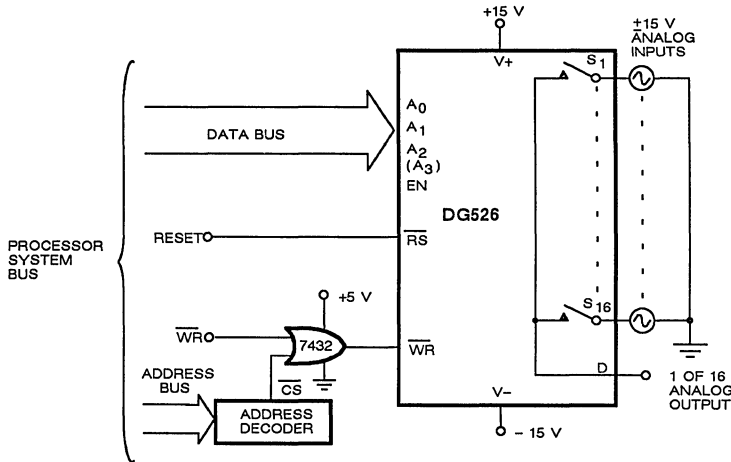


Figure 10

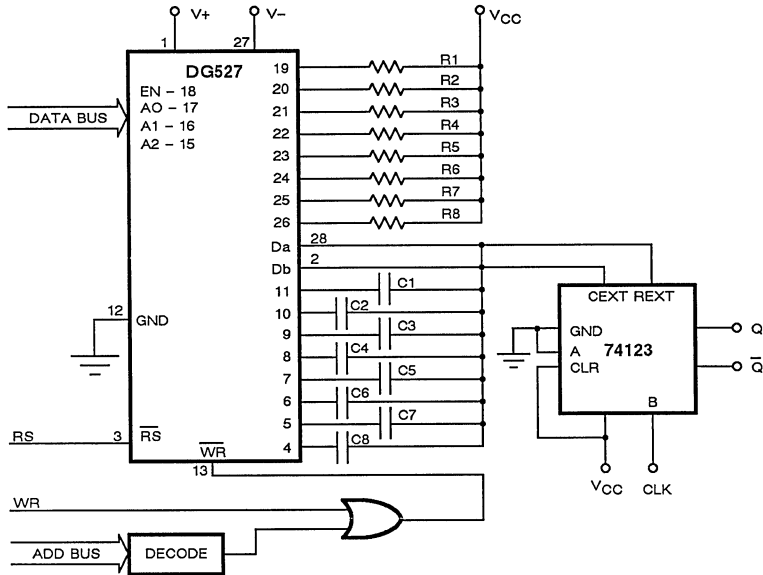


Figure 11.  $\mu$ P-selected Pulse-Width Control

### APPLICATIONS HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Analog & Power Supply GND (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
20	-20	GND	2.4/0.8	± 20
15	-15	GND	2.4/0.8	± 15
8	-8	GND	2.4/0.8	± 8

## 8-Channel and Dual 4-Channel Latchable Multiplexers

### FEATURES

- TTL Compatible
- 44 V Power Supply Rating
- On-board Address Latches
- $r_{DS(ON)} < 400 \Omega$
- Break-Before-Make

### BENEFITS

- Easily Interfaced
- Increased Analog Signal Range
- Microprocessor Bus Compatible
- Improved System Accuracy
- Reduced Crosstalk

### APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics And Military Systems
- Communication Systems
- Microprocessor Controlled Systems
- Audio Signal Multiplexing

### DESCRIPTION

DG528 and DG529 are 8 and 4-channel analog multiplexers, respectively, with on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary shorting of the input signals. Designed on the Siliconix PLUS-40 CMOS process, each bidirectional switch features low  $400 \Omega$  ON resistance over the full analog range, and will block signals to 30 V peak-to-peak in the unselected channels. All logic levels are TTL compatible.

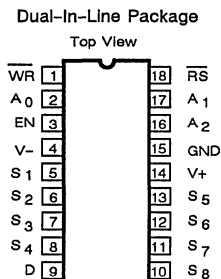
DG528 is an 8-channel single-ended analog multiplexer designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address ( $A_0, A_1, A_2$ ). DG529, a 4-channel dual

analog multiplexer, is designed to connect 1 of 4 dual inputs to a common dual output as determined by its 2-bit binary address ( $A_0, A_1$ ) logic. An epitaxial layer prevents latchup.

The on-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE. The DG528 is available in 18-pin CerDIP in the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ), industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ) and commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ) temperature ranges, and in the plastic DIP for commercial temperature operation.

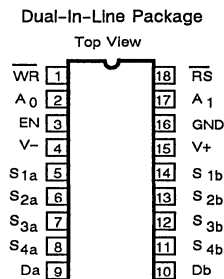
For more information on the DG528 and DG529, please refer to Siliconix Application Note AN83-4.

### PIN CONFIGURATION



Order Numbers:  
CerDIP: DG528AK, DG528BK,  
DG528CK

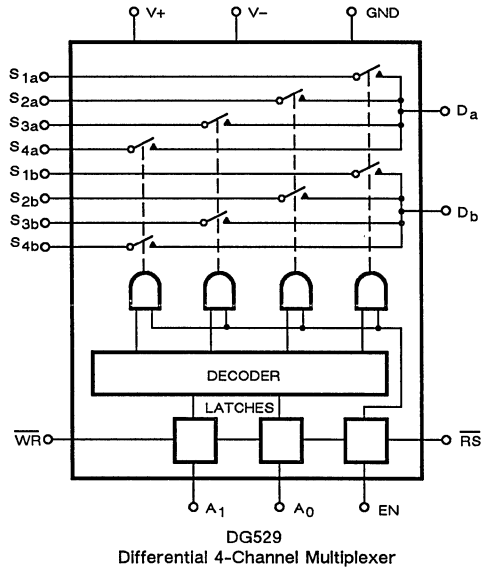
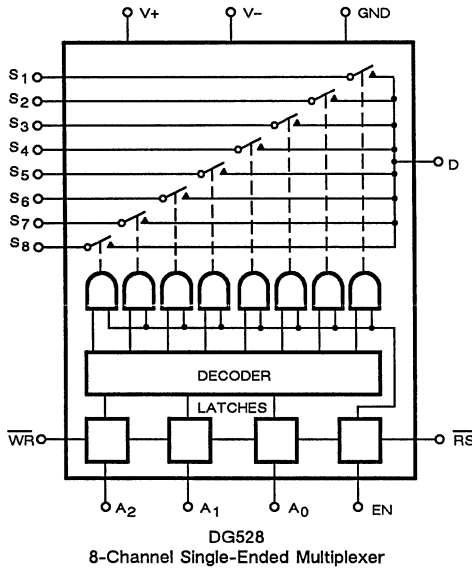
Plastic: DG528CJ



Order Numbers:  
CerDIP: DG529AK, DG529BK,  
DG529CK

Plastic: DG529CJ

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs,  $V_S, V_D^H$  ..... (V-) -2 V to (V+) +2 V or  
..... 20 mA, whichever occurs first.

Current (Any Terminal Except S or D) ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D  
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA

Operating Temperature (A Suffix) ..... -55 to 125°C

(B Suffix) ..... -25 to 85°C

(C Suffix) ..... 0 to 70°C

Storage Temperature (A & B Suffix) ..... -65 to 150°C

(C Suffix) ..... -65 to 125°C

Power Dissipation (Package)\*

18-Pin Ceramic DIP\*\* ..... 900 mW

18-Pin Plastic DIP\*\*\* ..... 470 mW

\* All leads soldered or welded to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6.3 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $GND = 0$ , $WR = 0$ $RS = 2.4\text{ V}$	LIMITS						UNIT		
			1=25°C 2=125,70,85°C 3=-55,-25,0°C		A SUFFIX -55 to 125°C		B, C SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SWITCH</b>											
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$		1,2,3		-15	15	-15	15	V		
Drain-Source <sup>e</sup> ON Resistance	$r_{DS(ON)}$	$V_D = \pm 10\text{ V}$ , $V_{AL} = 0.8\text{ V}$ $I_S = -200\text{ }\mu\text{A}$ , $V_{AH} = 2.4\text{ V}$	1,3 2	270		400 500		450 500	$\Omega$		
Greatest Change in $r_{DS(ON)}$ Between Channels <sup>f</sup>	$\Delta r_{DS(ON)}$	$-10\text{ V} < V_S < 10\text{ V}$	1	6					%		
Source OFF Leakage Current	$I_{S(OFF)}$	$V_{EN} = 0\text{ V}$	$V_S = \pm 10\text{ V}$ $V_D = \mp 10\text{ V}$	1 2	-0.005	-1 -50	1 50	-5 -50	5 50	nA	
Drain OFF Leakage Current	DG528		$I_{D(OFF)}$	$V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$	1 2	-0.015	-10 -200	10 200	-20 -200		20 200
				DG529	$V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$	1 2	-0.008	-10 -100	10 100		-20 -100
Drain ON Leakage Current	DG528		$I_{D(ON)}^{e,9}$	$V_S = V_D = \pm 10\text{ V}$ $V_{EN} = 2.4\text{ V}$ $V_{AL} = 0.8\text{ V}$ $V_{AH} = 2.4\text{ V}$	1 2	-0.03	-10 -200	10 200	-20 -200		20 200
	DG529	1 2			-0.015	-10 -100	10 100	-20 -100	20 100		
<b>INPUT</b>											
Logic Input Current Input Voltage High	$I_{AH}$	$V_A = 2.4\text{ V}$	1 2	-0.002	-10 -30			-10 -30		$\mu\text{A}$	
		$V_A = 15\text{ V}$	1 2	0.006		10 30			10 30		
Logic Input Current Input Voltage Low	$I_{AL}$	$V_{EN} = 0\text{ or }2.4\text{ V}$ , $V_A = 0\text{ V}$ $RS = 0\text{ V}$ , $WR = 0\text{ V}$	1 2	-0.002	-10 -30			-10 -30			
<b>DYNAMIC</b>											
Switching Time of Multiplexer	$t_{TRANS}$	See Figure 3	1	0.6			1			$\mu\text{s}$	
Break-Before-Make Interval	$t_{OPEN}$	See Figure 5	1	0.2							
Enable and Write Turn ON Time	$t_{ON(EN,WR)}$	See Figure 4 and 6	1	1			1.5				
Enable and Reset Turn OFF Time	$t_{OFF(EN,RS)}$	See Figure 4 and 7	1	0.4			1				
Charge Injection	Q	See Figure 8	1	4						pC	
OFF Isolation		$V_{EN} = 0$ , $R_L = 1\text{ k}\Omega$ $C_L = 15\text{ pF}$ , $V_S = 7\text{ V}_{RMS}$ $f = 500\text{ kHz}$	1	68						dB	
Logic Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$	1	2.5						pF	

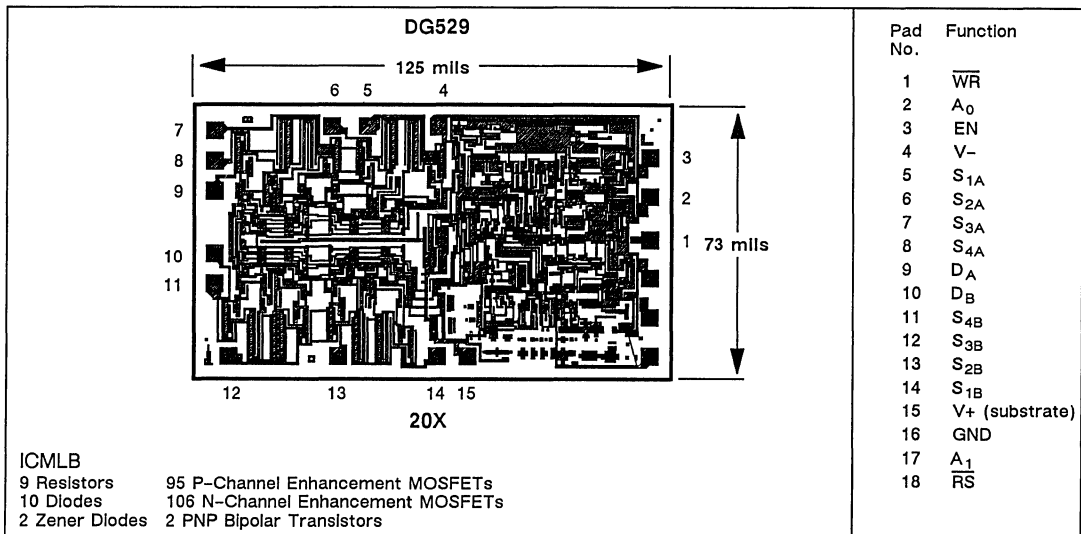
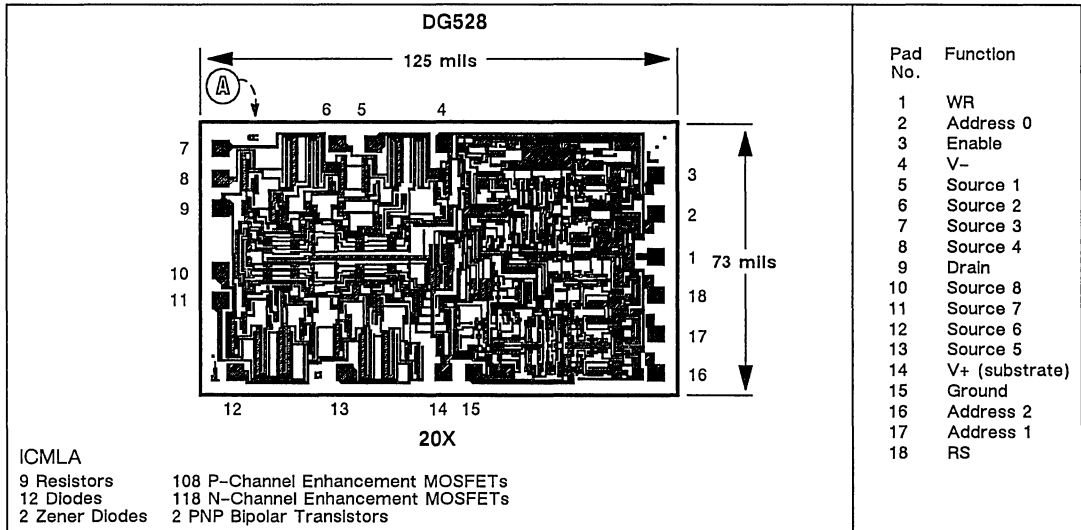
ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0, WR = 0 RS = 2.4 V	LIMITS						UNIT		
			1=25°C		A SUFFIX		B, C SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>DYNAMIC (Cont'd)</b>											
Source OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>EN</sub> = 0 f = 140 kHz	V <sub>S</sub> = 0	1	5					pF	
Drain OFF Capacitance	DG528		C <sub>D(OFF)</sub>	V <sub>D</sub> = 0	1	25					
	DG529				1	12					
<b>MINIMUM INPUT TIMING REQUIREMENTS</b>											
WR Pulse Width	t <sub>WW</sub>	See Figure 1	1,2,3			300		300		ns	
A <sub>X</sub> , EN Data Valid to WR	t <sub>DW</sub>	(Stabilization Time) See Figure 1	1,2,3			180		180			
A <sub>X</sub> , EN Data Valid after WR	t <sub>WD</sub>	(Hold Time) See Figure 1	1,2,3			30		30			
RS Pulse Width <sup>i</sup>	t <sub>RS</sub>	See Figure 2 V <sub>S</sub> = 5 V	1,2,3			500		500			
<b>SUPPLY</b>											
Positive Supply Current	I <sub>+</sub>	V <sub>EN</sub> = 0, V <sub>A</sub> = 0	1			2.5		2.5		mA	
Negative Supply Current	I <sub>-</sub>		1			-1.5		-1.5			

**NOTES:**

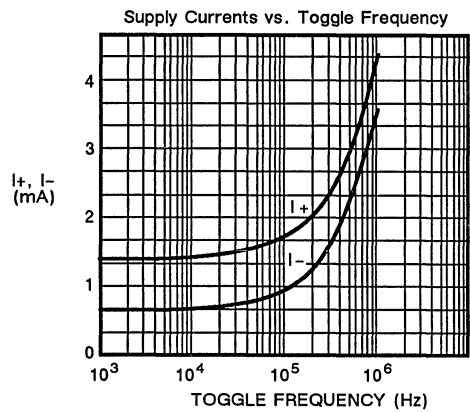
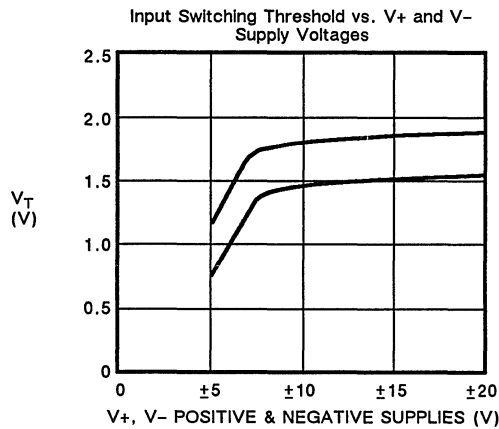
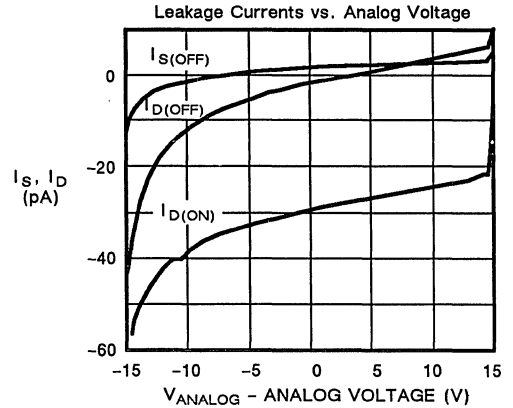
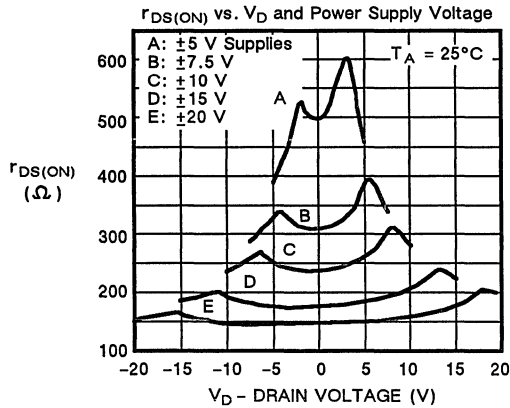
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Sequence each switch ON.
- $$f. \Delta r_{DS(ON)} = \left( \frac{r_{DS(ON) MAX} - r_{DS(ON) MIN}}{r_{DS(ON) AVE}} \right)$$
- I<sub>D(ON)</sub> is leakage from driver into "ON" switch.
- Signals on S<sub>X</sub>, D<sub>X</sub>, IN<sub>X</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- Period of Reset (RS) pulse must be at least 50 μs during or after power ON.



**DIE TOPOGRAPHY**



## TYPICAL CHARACTERISTICS



**TRUTH TABLES**

**DG528**

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching						
X	X	X	X		1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

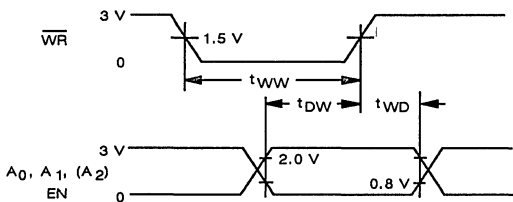
**DG529**

A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching					
X	X	X		1	Maintains previous switch condition
Reset					
X	X	X	X	0	NONE (latches cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

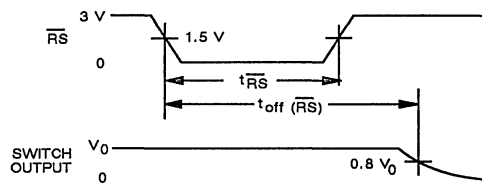
Logic "1":  $V_{AH} \geq 2.4 \text{ V}$

Logic "0":  $V_{AL} \leq 0.8 \text{ V}$

**TIMING DIAGRAMS**

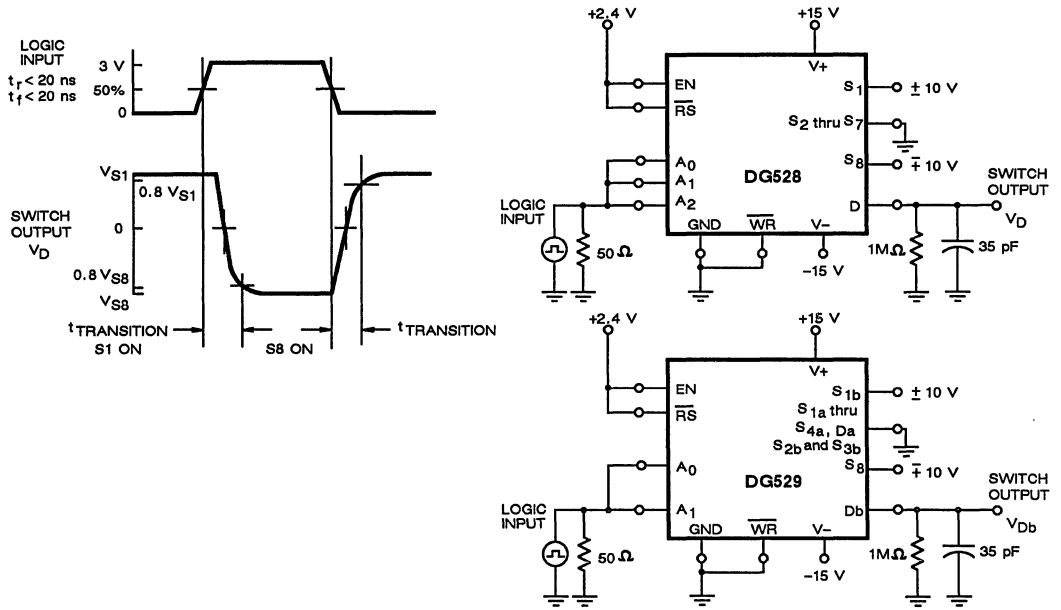


**Figure 1**

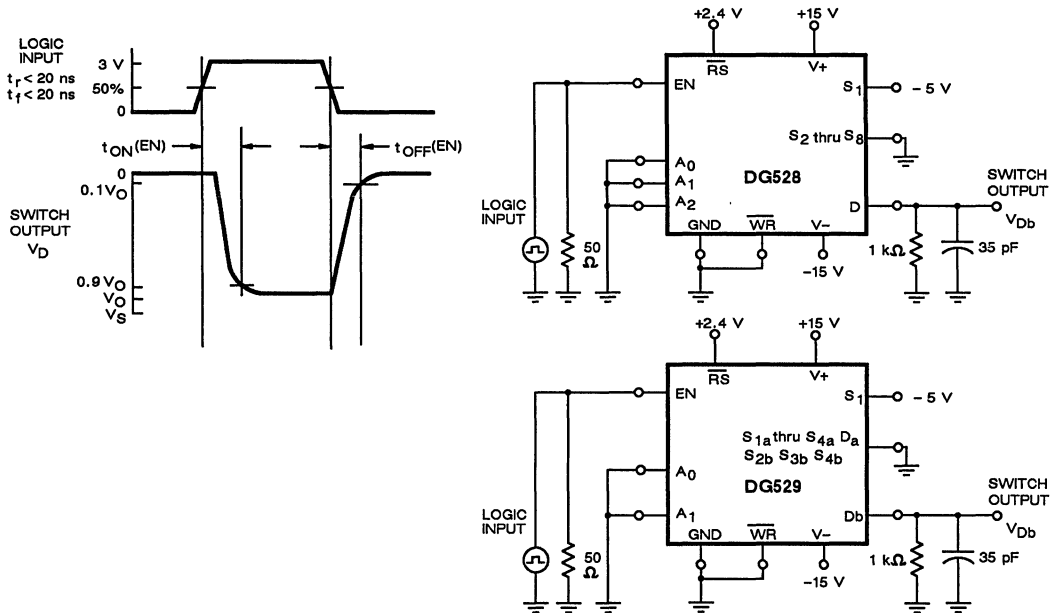


**Figure 2**

## TRANSITION TIME TEST CIRCUIT



## ENABLE $t_{\text{ON}}/t_{\text{OFF}}$ TIME TEST CIRCUIT



**OPEN TIME (B.B.M.) INTERVAL TEST CIRCUIT**

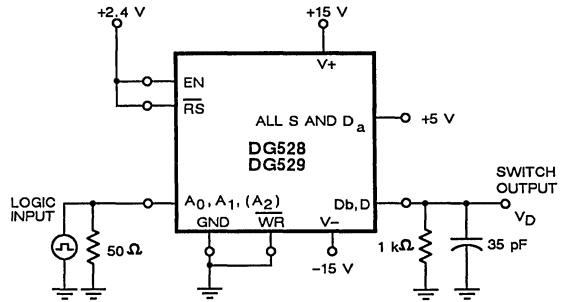
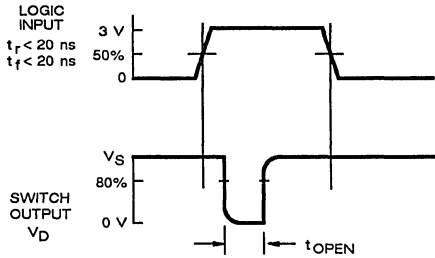


Figure 5

**WRITE TURN-ON TIME  $t_{ON}(\overline{WR})$  TEST CIRCUIT**

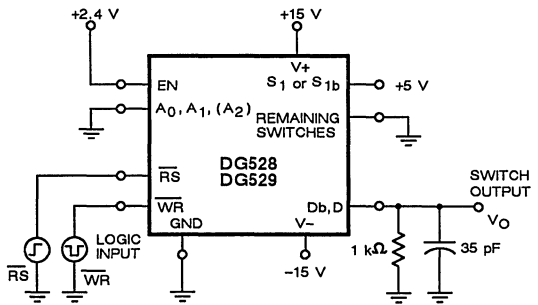
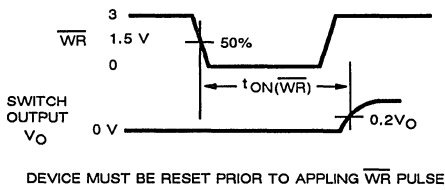


Figure 6

**RESET TURN-OFF TIME  $t_{OFF}(\overline{RS})$  TEST CIRCUIT**

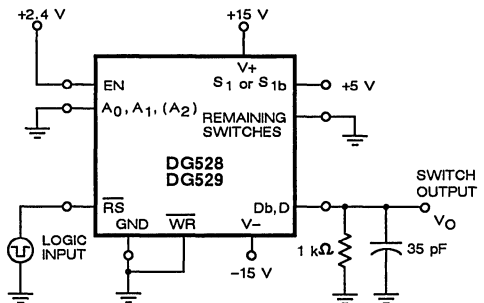
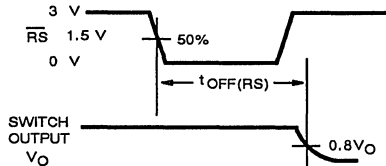


Figure 7

## CHARGE INJECTION TEST CIRCUIT

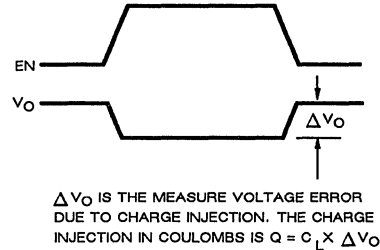
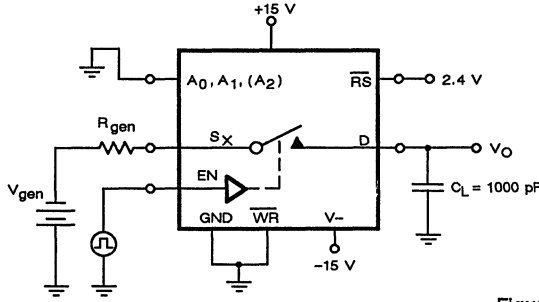


Figure 8

## DETAILED DESCRIPTION

The internal structure of the DG528 and DG529 includes a 5 V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel N and P-channel MOSFETs (see figure 9).

The input protection on the logic lines  $A_0$ ,  $A_1$ ,  $A_2$ , EN and control lines WR, RS shown in figure 9 minimize susceptibility to static encountered during handling and operational transients.

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D type latch. The level sensitive D latch continuously places the  $D_X$  input signal on the  $Q_X$  output when the CLK (WR) input is low, resulting in transparent operation. As soon as CLK (WR) returns high the latch holds the data last present on

the  $D_X$  input at the  $Q_X$  output, subject to the "Minimum Input Timing Requirements" table.

Following the latches the  $Q_X$  signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full ON/OFF switch operation for any analog signal present between the  $V_+$  and  $V_-$  supply pins.

The enable (EN) pin is used to enable the address latches during the WR pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The RS pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The WR pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

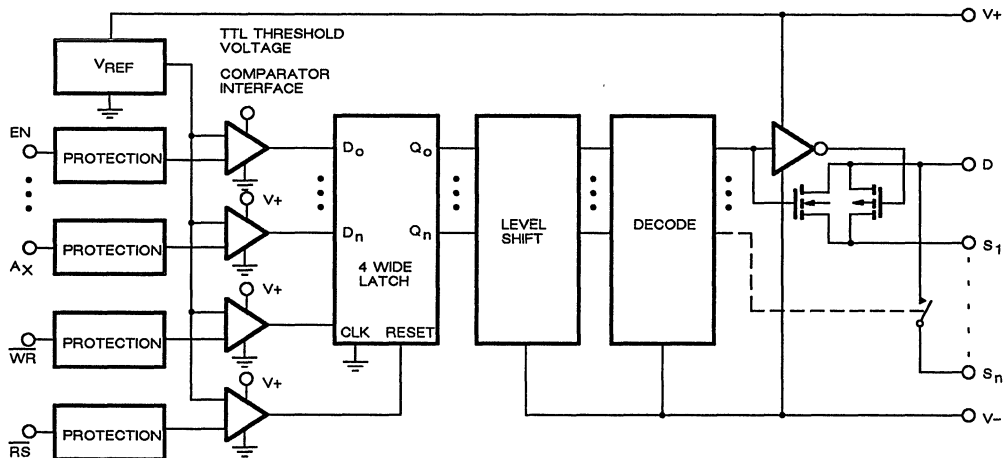


Figure 9. DG528/529 Simplified Internal Structure

**APPLICATIONS**

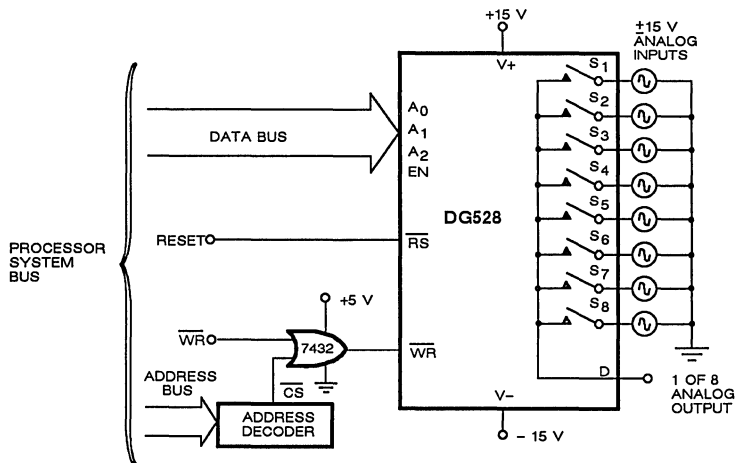
**BUS INTERFACING (See Figure 10)**

The DG528 and DG529 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 ON) until the microprocessor determines it is necessary to turn different switches ON or turn all switches OFF.

The input latches become transparent when  $\overline{WR}$  is held low; therefore, these multiplexers operate by direct command of the coded switch state on  $A_2$ ,  $A_1$ ,  $A_0$ . In this mode the DG528 is identical to the very popular DG508 even sharing the same pin locations. The same is true of the DG529 versus the popular DG509.

Initially during system power-up  $\overline{RS}$  would be active LOW maintaining all 8 switches in the OFF state. After  $\overline{RS}$  returned HIGH the DG528 maintains all switches in the OFF state. As soon as the system program was ready to perform a write operation to the address assigned to the DG528, the address decoder would provide a  $\overline{CS}$  active LOW signal which is gated with the WRITE ( $\overline{WR}$ ) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the  $\overline{WR}$  signal returns to the HIGH state, (positive edge) the input latches of the DG528 save the data from the DATA BUS. The coded information in the  $A_0$ ,  $A_1$ ,  $A_2$ , and EN latches is decoded and the appropriate switch is turned ON.

The EN latch allows all switches to be turned OFF under program control. This becomes useful when two or more DG528s are cascaded to build 16-line and larger analog signal input multiplexers.



**Figure 10. Bus Interface**

## APPLICATIONS HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Analog & Power Supply GND (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH</sub> Min/ V <sub>INL</sub> Max (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
20	-20	GND	2.4/0.8	± 20
15	-15	GND	2.4/0.8	± 15
8	-8	GND	2.4/0.8	± 8



# 8-Channel and Dual 4-Channel CMOS Analog Multiplexers with Overvoltage Protection

## FEATURES

- Analog/Digital Overvoltage Protection
- Fail Safe With Power Loss (No Latchup)
- Break-Before-Make Switching
- TTL and CMOS Compatible Inputs

## BENEFITS

- Improved Ruggedness
- Power Loss Protected
- Prevents Adjacent Channel Crosstalk
- Standard Logic Interface

## APPLICATIONS

- Data Acquisition Systems
- Industrial Process Control
- Avionics Test Equipment
- High Rel Control Systems

## DESCRIPTION

The DG548 and DG549 are dielectrically isolated 8- and 4-channel analog multiplexers, respectively, incorporating overvoltage protection. They withstand analog input voltages greater than the supplies. This is advantageous in systems where the analog inputs originate outside the equipment. The DG548/DG549 can withstand continuous inputs up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are lost, while input signals are still present. These multiplexers can withstand brief input transient spikes of several hundred volts which otherwise

would require complex external protection networks. Necessarily, ON resistance is higher than the DG508A/DG509A but very low leakage currents combine to produce low errors.

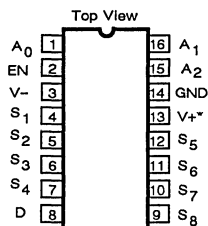
The DG548 and DG549 are pin compatible with the industry-standard DG508A and DG509A multiplexers.

The DG548 and DG549 are offered in 16-pin plastic and CerDIP packages for operation over the commercial, C suffix (0 to 70°C) and military, A suffix (-55 to 125°C) temperature ranges.

**5**

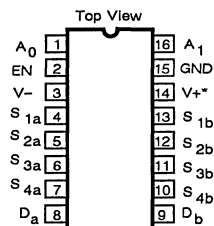
## PIN CONFIGURATION

Dual-In-Line Package



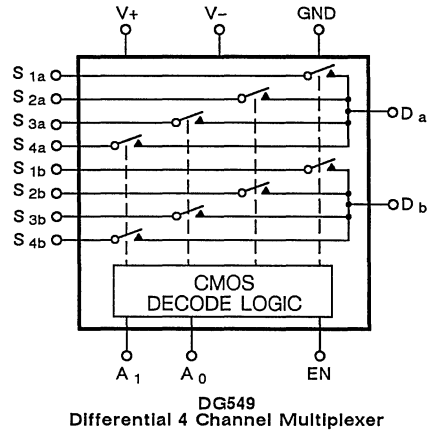
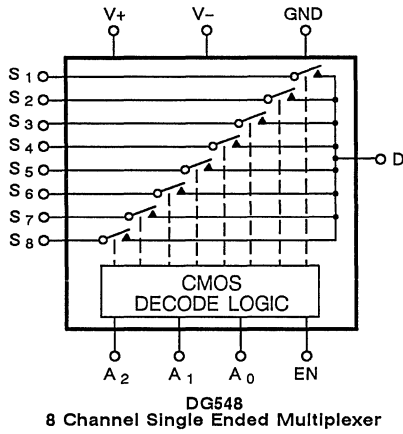
Order Numbers:  
DG548AK, DG548BK  
DG548CK, DG548CJ

Dual-In-Line Package



Order Numbers:  
DG549AK, DG549BK  
DG549CK, DG549CJ

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

V<sub>EN</sub>, V<sub>A</sub>, Digital Input ..... (V-) -4 V to (V+) +4 V

V<sub>S</sub>, Analog Input Overvoltage with Power ON ..... (V-) -20 V to (V+) +20 V

V<sub>S</sub>, Analog Input Overvoltage with Power OFF ..... -35 V to +35 V

Continuous Current, S or D ..... 20 mA

Peak current, S or D  
(Pulsed at 1 ms, 10% duty cycle max) ..... 40 mA

Operating Temperature (A Suffix) ..... -55 to 125°C  
(C Suffix) ..... 0 to 70°C

Storage Temperature (A Suffix) ..... -65 to 150°C  
(C Suffix) ..... -65 to 125°C

Power Dissipation (Package)\*

16-Pin Ceramic DIP\*\* ..... 900 mW

16-Pin Plastic DIP\*\*\* ..... 600 mW

\* All leads soldered or welded to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6.3 mW/°C above 25°C.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS<sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>AH</sub> = 4.0 V, V <sub>AL</sub> = 0.8 V	LIMITS						UNIT
			1=25°C		A SUFFIX		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V
ON Resistance <sup>e</sup>	r <sub>DS(ON)</sub>	V <sub>D</sub> = ±10 V, I <sub>D</sub> = -100 μA	1 2,3	1.2		1.5 1.8		1.8 2.0	kΩ
r <sub>DS(ON)</sub> Match Between Channels <sup>f</sup>	Δ r <sub>DS(ON)</sub>	V <sub>S</sub> = 0 V, I <sub>D</sub> = -100 μA	1	6					%

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>AH</sub> = 4.0 V, V <sub>AL</sub> = 0.8 V			LIMITS						UNIT
					1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		
					TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH (Cont'd)</b>											
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>EN</sub> = 0 V	V <sub>S</sub> = ±10 V V <sub>D</sub> = ∓10 V	1 2,3	0.03	-0.5 -50	0.5 50	-0.5 -50	0.5 50	nA	
Drain OFF Leakage Current			DG548	V <sub>D</sub> = ±10 V V <sub>S</sub> = ∓10 V	1 2,3	1	-5 -250	5 250	-5 -250		5 250
			DG549	V <sub>D</sub> = ±10 V V <sub>S</sub> = ∓10 V	1 2,3	0.5	-2.5 -125	2.5 125	-2.5 -125		2.5 125
I <sub>D(OFF)</sub> with Input Overvoltage Applied	I <sub>DOV</sub>	Analog Overvoltage = ±33 V (See Figure 1)		1 2,3	4	-20 -2000	20 2000	-20 -2000	20 2000		
Differential OFF Drain Leakage Current	I <sub>DIFF</sub>	DG549 Only		1,2,3		-50	50	-50	50		
Drain ON Leakage Current	I <sub>D(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = ±10 V	Sequence Each Switch ON V <sub>AL</sub> = 0.8 V V <sub>AH</sub> = 2.4 V	1 2,3	0.1	-1 -250	1 250	-1 -250	1 250		
				1 2,3	0.05	-0.5 -125	0.5 125	-0.5 -125	0.5 125		
<b>INPUT</b>											
Input LOW Threshold	V <sub>AL</sub>			1,2,3			0.8		0.8	V	
Input HIGH Threshold	V <sub>AH</sub>			1,2,3		2.4		2.4			
Logic Input Current	I <sub>A</sub>	V <sub>A</sub> = 2.4 V or 0.8 V		1,2,3		-1	1	-1	1	μA	
<b>DYNAMIC</b>											
Access Time	t <sub>A</sub>	See Figure 2		1	0.5		1		1	μs	
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 3		1	80	25		25		ns	
Enable Delay Turn ON Time	t <sub>ON(EN)</sub>	See Figure 4		1 2,3	300		500 1000		500 1000		
Enable Delay Turn OFF Time	t <sub>OFF(EN)</sub>			1 2,3	300		500 1000		500 1000		
Settling Time	t <sub>s</sub>	0.1 %		1	1.2						μs
		0.025%		1	3.5						
OFF Isolation		V <sub>EN</sub> = 7 V, R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 3 pF, V <sub>S</sub> = 3 V <sub>RMS</sub> f = 500 kHz		1	68					dB	
Logic Input Capacitance	C <sub>in</sub>	f = 1 MHz		1	5					pF	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>t</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>AH</sub> = 4.0 V, V <sub>AL</sub> = 0.8 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		C SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC (Cont'd)</b>										
Source OFF Capacitance	C <sub>S(OFF)</sub>		1	5						
Drain OFF Capacitance	DG548	C <sub>D(OFF)</sub>	1	25						pF
	DG549		1	12						
ON State Input Capacitance	DG548	C <sub>S(ON)</sub>	1	30						
	DG549		1	17						
Positive Supply Current	I <sub>+</sub>	V <sub>EN</sub> = HIGH or LOW V <sub>A</sub> = 0 V	1,2,3	0.5		2.0		2.0		mA
Negative Supply Current	I <sub>-</sub>		1,2,3	-0.02	-1		-1			

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

## SWITCHING TIME TEST CIRCUITS

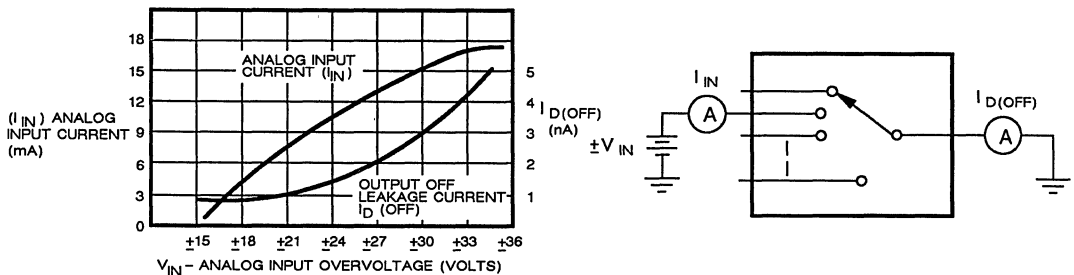
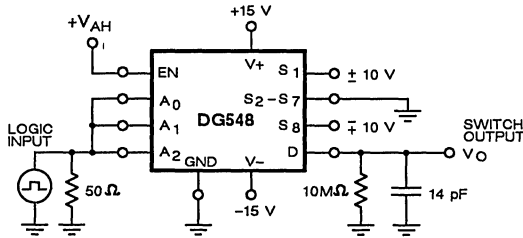


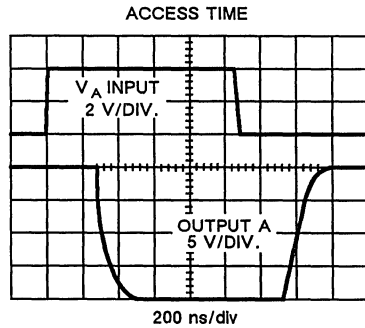
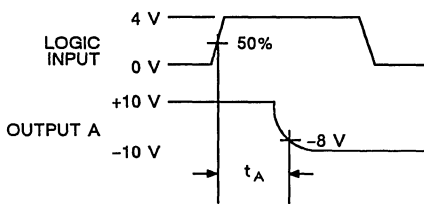
Figure 1. Analog Input Overvoltage Characteristics

**SWITCHING TIME TEST CIRCUITS (Cont'd)**

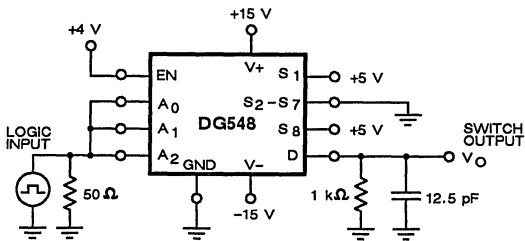


\* Similar Connection for DG549

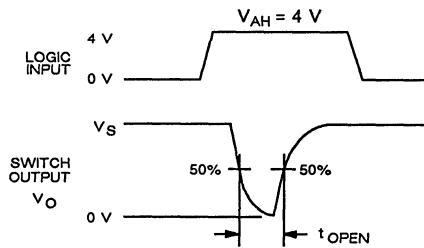
**Figure 2. Access Time vs. Logic Level (High)**



**Figure 3. Access Time**

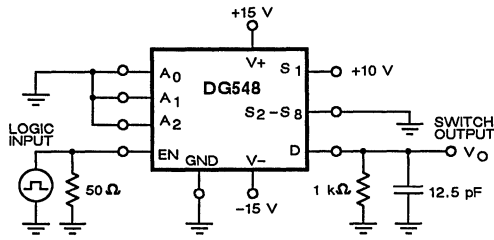


\* Similar Connection for DG549



**Figure 4. Break-Before-Make Delay**

## SWITCHING TIME TEST CIRCUITS (Cont'd)



\* Similar Connection for DG549

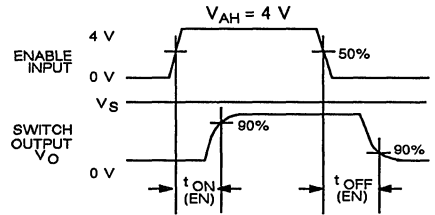


Figure 5. Enable Delay

## TRUTH TABLES

DG548

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG549

A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" =  $V_{AL} \leq 0.8$  Logic "1" =  $V_{AH} \geq 2.4$  V

# Serial-loading Octal SPST High-Voltage Analog Switch

## FEATURES

- $\pm 50$  Volt Analog Range
- Serial Data Interface
- Low  $r_{DS(ON)}$  ( $< 40 \Omega$  with  $\pm 60$  V Supplies)
- Bidirectional Switching

## BENEFITS

- Extended Voltage Range
- Single Wire Interface
- Reduced Switching Errors
- Blocks Bipolar Signals

## APPLICATIONS

- Ultrasound Systems
- Microprocessor-Controlled Systems
- Automatic Test Equipment
- High Voltage ( $\pm 60$  V) Systems

## DESCRIPTION

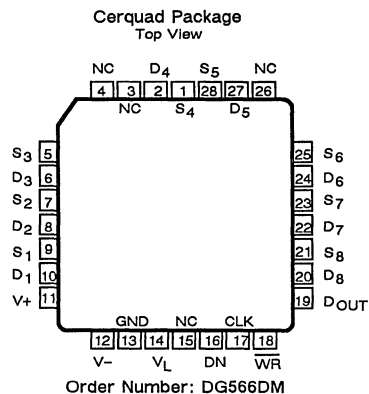
The DG566 is a high voltage D/CMOS octal (8-channel) array of analog switches with a serial data interface controlling the state of each switch independently. This allows selection of none, any or all eight channels simultaneously. In addition to its high analog voltage range of  $\pm 50$  V, the DG566 features low ON-resistance ( $30 \Omega$  typical), low quiescent power consumption ( $270 \mu W$  maximum), and bidirectional switching over the full analog signal range.

The serial data interface simplifies control in remote applications. The  $\overline{WR}$  pin controls latching of the analog switch control inputs. The clock input (CK) shifts the data through the register, but does not change the state of the switches until the latches are enabled via  $\overline{WR}$ . The logic levels are set by the  $V_L$  input, ranging from a minimum of 8 V to a rated maximum of 18 V.

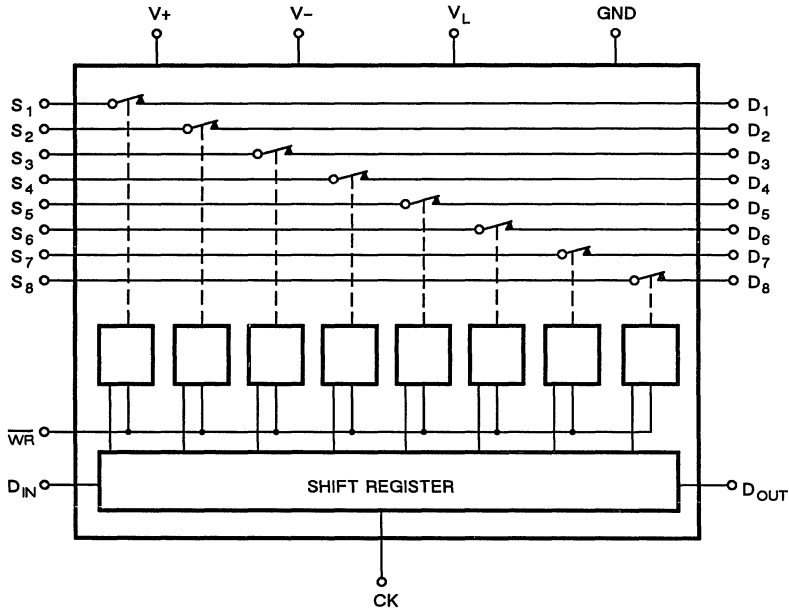
Built in a proprietary high-voltage D/CMOS process, the DG566 achieves high voltage signal control while maintaining low ON-resistance, low leakage ( $I_{S(OFF)} < 5$  nA at 50 V), and fast transition times ( $< 2 \mu s$ ).

The DG566 is available in the Cerquad package for surface mount applications. It is specified for operation over the industrial, D suffix ( $-40$  to  $85^\circ C$ ) temperature range.

## PIN CONFIGURATION



## FUNCTIONAL BLOCK DIAGRAM & TRUTH TABLE



8 Latchable SPST Switches Per Package \*

D <sub>INX</sub>	$\overline{WR}$	SWITCH
0	0	OFF
1	0	ON
X	1	Maintains Previous State

Logic "0"  $\leq 3.5$  V

Logic "1"  $\geq 11.5$  V

$\overline{WR}$  Input is level sensitive (not edge-triggered)

\*SWITCHES SHOWN FOR LOGIC "1" INPUT

### ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND

V+ ..... 62 V

V- ..... -62 V

V<sub>L</sub> ..... 18 V

Logic Input Voltage ..... -0.3 V to V<sub>L</sub> + 0.3 V

Continuous Current, S or D ..... 90 mA

Peak Current, S or D

(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 400 mA

Storage Temperature ..... -65 to 125°C

Operating Temperature (D Suffix) ..... -40 to 85°C

Power Dissipation\*

28-Pin Cerquad\*\* ..... 450 mW

\* Device mounted with all leads soldered or welded to a PC board.

\*\* Derate 6 mW/°C above 75°C.



**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

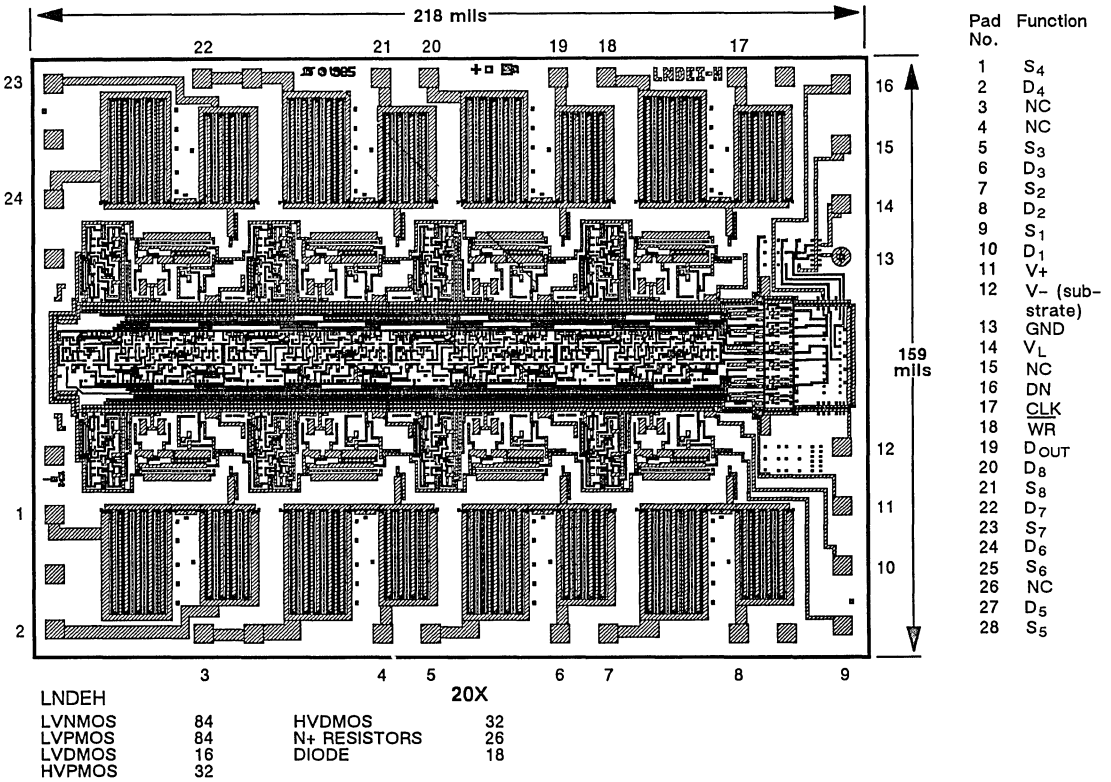
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 60 V V <sub>-</sub> = -60 V V <sub>L</sub> = 15 V WR = GND = 0 V	LIMITS				UNIT	
			1=25 °C 2=85 °C 3=-40 °C		D SUFFIX -40 to 85 °C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>								
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3			-50 50	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = 20 mA	-50 V < V <sub>D</sub> < 30 V	1 2,3	25		40 60	Ω
			30 V < V <sub>D</sub> < 40 V	1 2,3	30		50 80	
			40 V < V <sub>D</sub> < 50 V	1 2,3	50		100 150	
ON Resistance Variation	Δr <sub>DS(ON)</sub>	I <sub>D(all)</sub> = 5 mA V <sub>S(all)</sub> = 0 V	1	± 2		± 5	%	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>D</sub> = -50 V	V <sub>S</sub> = 0 V	1 2,3	0.5		2 50	nA
			V <sub>S</sub> = 50 V	1 2,3	1		5 100	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = -50 V	V <sub>D</sub> = 0 V	1 2,3	0.5		2 50	
			V <sub>D</sub> = 50 V	1 2,3	1		5 100	
Drain ON Leakage Current	I <sub>D(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V		1 2,3	2		10 5 k	
		V <sub>S</sub> = V <sub>D</sub> = 50 V		1 2,3	5		20 10 k	
<b>INPUT <sup>f</sup></b>								
Logic Input LOW Voltage	V <sub>INL</sub>		1				3.5	V
Logic Input HIGH Voltage	V <sub>INH</sub>		1			11.5		
Logic Input Current Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1	0.002			2.0	μA
Logic Input Current Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = V <sub>L</sub>	1	0.002			2.0	
Turn ON Time	t <sub>ON</sub>	R <sub>L</sub> = 5 kΩ C <sub>L</sub> = 50 pF See Figures 1 and 2	1	0.5			2	μs
Turn OFF Time	t <sub>OFF</sub>		1	0.2			1.5	

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 60 V V <sub>-</sub> = -60 V V <sub>L</sub> = 15 V WR = GND = 0 V	LIMITS				UNIT
			1=25 °C 2=85 °C 3=-40 °C		D SUFFIX -40 to 85 °C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>							
Setup Time to $\overline{\text{WR}}$	t <sub>SD</sub>	See Figure 2	1	20	100		ns
Hold Time from $\overline{\text{WR}}$	t <sub>HD</sub>		1		25		
Write Pulse Width	t <sub>WR</sub>		1		35		
Clock Delay to Data Out	t <sub>DO</sub>		1	250		30	
Data Setup Time to Clock	t <sub>SU</sub>		1		0		
Data Hold Time from Clock	t <sub>H</sub>		1		35		
Source OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V	1	15			pF
Drain OFF Capacitance	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0 V	1	15			
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	V <sub>S</sub> = 0 V, V <sub>WR</sub> = V <sub>L</sub> f = 140 kHz	1	110			
OFF Isolation		R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 3 pF V <sub>S</sub> = 10 Vp-p, f = 10 kHz	1	65			dB
<b>SUPPLY</b>							
Positive Supply Current	I <sub>+</sub>	V <sub>IN(all)</sub> = 0 V or 15 V <sup>f</sup>	1 2,3	0.002		2 2	μA
Negative Supply Current	I <sub>-</sub>		1 2,3	0.002		2 2	
Logic Supply Current	I <sub>L</sub>		1 2,3	0.002		2 2	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Pulsed at 1 ms, 10% duty cycle.
- f. "Inputs" refer to digital Inputs D<sub>1</sub>-D<sub>8</sub>,  $\overline{\text{WR}}$  and CK.

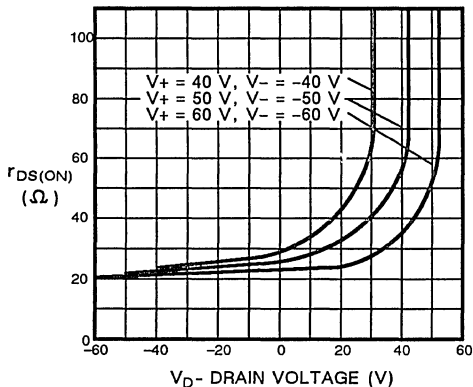
**DIE TOPOGRAPHY**



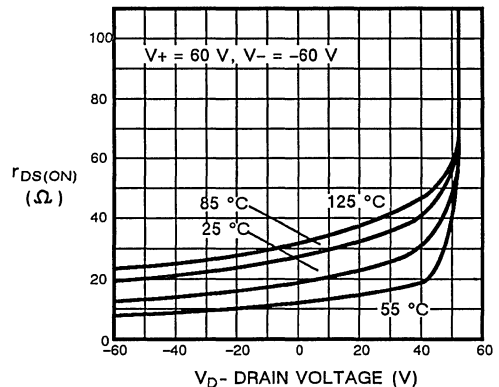
**5**

**TYPICAL CHARACTERISTICS**

Drain-Source ON Resistance vs.  $V_D$  and Power Supply Voltages



Drain-Source ON Resistance vs. Temperature



## SWITCHING TIME TEST CIRCUITS

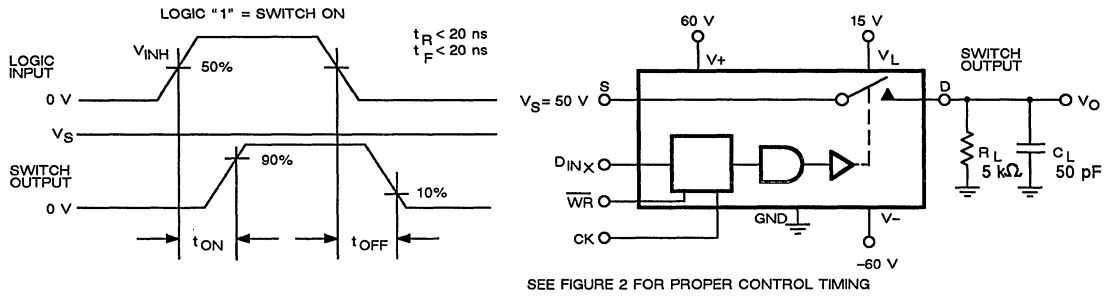


Figure 1. Switching Time Test Circuit

## TIMING DIAGRAM

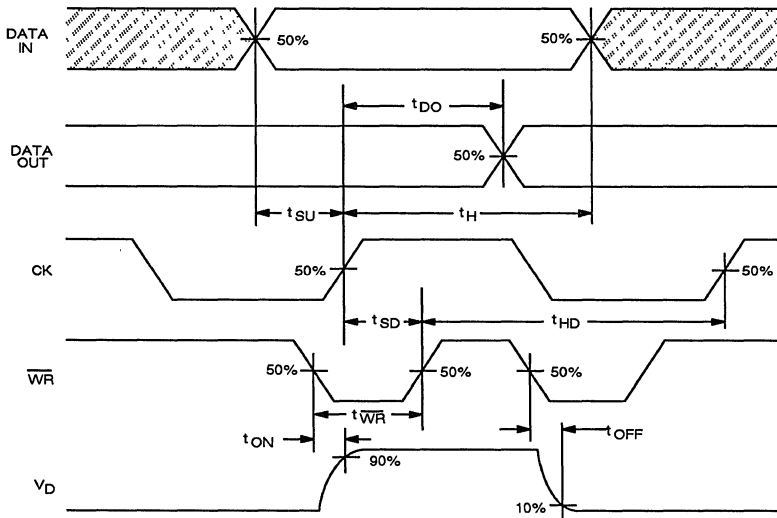


Figure 2. Timing Diagram

# 8- and Dual 4-Channel High-Voltage CMOS Multiplexers with Latches

## FEATURES

- $\pm 50$  V Signal Range
- On-Board Address Latches
- Low  $r_{DS(ON)}$  ( $< 40 \Omega$  with  $\pm 60$  V Supplies)
- Bidirectional Switching

## BENEFITS

- Extended Voltage Range
- Microprocessor Compatible (15 V CMOS)
- Reduced Switching Errors
- Blocks Bipolar Signals

## APPLICATIONS

- High Voltage ( $\pm 60$  V) Systems
- Microprocessor Controlled Systems
- Automatic Test Equipment
- Communications Systems

## DESCRIPTION

The DG568 and DG569 are 8- and 4-channel multiplexers respectively, designed for high voltage ( $\pm 50$  V) applications in microprocessor based instrumentation and process control. Both multiplexers feature low ON resistance (30 ohms typ.) and true bi-directional switch action over the full analog signal range. In addition, on-board data latches and control inputs are provided to simplify interfacing with most microprocessors.

The DG568 provides 8-channel single ended multiplexing and demultiplexing, while the DG569 is designed for 4-channel differential switching applications. Address inputs with latches ( $A_0, A_1,$

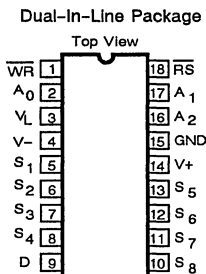
and  $A_2$ ), chip select  $\overline{WR}$  and device reset  $\overline{RS}$  (all channels off), are the logic controls which store, or clear, the switch address-inputs.  $\overline{RS}$  also simplifies switch turn-off during system powerup or reset.

Built in a proprietary high-voltage D/CMOS process, these devices achieve high voltage signal control, while maintaining low ON-resistance, low leakage, and fast transition times.

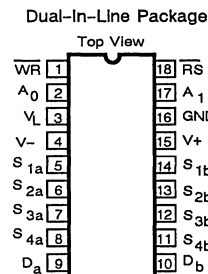
Both devices are provided in the 18-pin side braze package, and are specified over the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ) temperature ranges.

**5**

## PIN CONFIGURATION

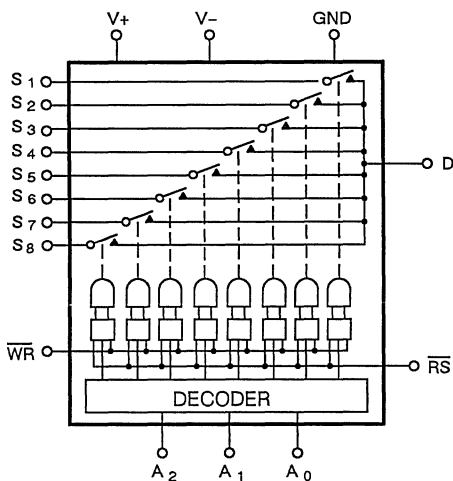


Order Numbers:  
Side Braze: DG568AP, DG568BP

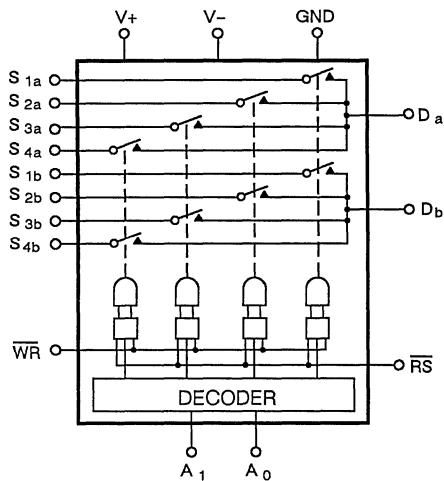


Order Numbers:  
Side Braze: DG569AP, DG569BP

## FUNCTIONAL BLOCK DIAGRAM



**DG568**  
8-Channel Single Ended Multiplexer



**DG569**  
Differential 4-Channel Multiplexer

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND

V+ ..... 62 V

V- ..... -62 V

V<sub>L</sub> ..... 18 V

Digital Inputs ..... -0.3 V to V<sub>L</sub> + 0.3 V

Continuous Current, S or D ..... 90 mA

Peak Current, S or D  
(Pulsed at 1 ms, 10% duty cycle) ..... 400 mA

Operating Temperature (A Suffix) ..... -55 to 125°C  
(B Suffix) ..... -25 to 85°C

Storage Temperature (A and B Suffixes) .. -65 to 150°C

Power Dissipation (Package)\*  
18-Pin Side Braze\*\* ..... 900 mW

\* All leads soldered or welded to PC board.

\*\* Derate 12 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 60 V V- = -60 V V <sub>L</sub> = V <sub>RS</sub> = 15 V V <sub>WR</sub> = GND = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-50	50	-50	50	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	-50 V < V <sub>D</sub> < 30 V I <sub>S</sub> = 20 mA	1 2,3	25		40 75		40 65	Ω
		30 V < V <sub>D</sub> < 40 V I <sub>S</sub> = 20 mA	1 2,3	30		50 100		50 80	
		40 V < V <sub>D</sub> < 50 V I <sub>S</sub> = 20 mA	1 2,3	50		100 250		100 150	

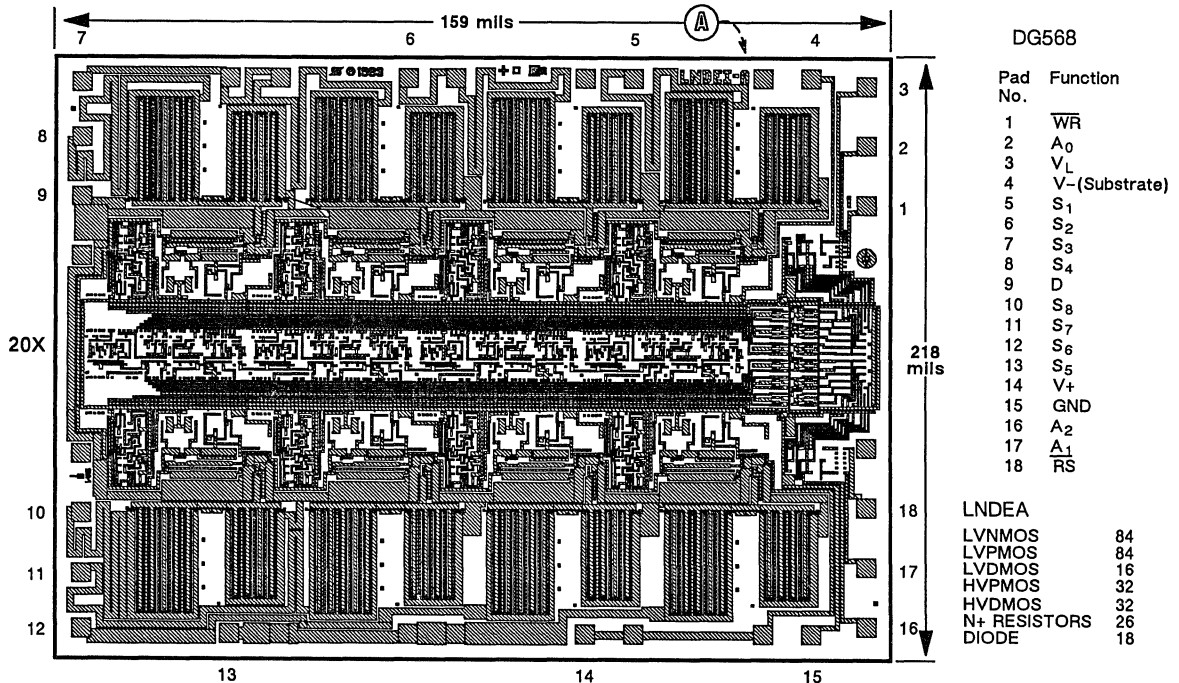
ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 60 V V <sub>-</sub> = -60 V V <sub>L</sub> = V <sub>RS</sub> = 15 V V <sub>WR</sub> = GND = 0 V	LIMITS							
			1=25°C		2=125,85°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>
<b>SWITCH</b>										
Source OFF Leakage Current	I <sub>S(OFF)</sub>	See Figure 1 V <sub>D</sub> = -50 V	V <sub>S</sub> = 0 V	1 2,3	0.5		2 500		2 50	nA
			V <sub>S</sub> = 50 V	1 2,3	1		5 750		5 100	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	See Figure 2 V <sub>S</sub> = -50 V	V <sub>D</sub> = 0 V	1 2,3	1.5		10 10,000		10 1000	
			V <sub>D</sub> = 50 V	1 2,3	5		25 15,000		25 2000	
Drain ON Leakage Current	I <sub>D(ON)</sub>	See Figure 3	V <sub>S</sub> = V <sub>D</sub> = 0 V	1 2,3	2		10 10,000		10 5000	
			V <sub>D</sub> = 50 V	1 2,3	5		20 20,000		20 10,000	
<b>INPUT <sup>e</sup></b>										
Logic Input Current Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V	1	0.002		2		2	μA	
Logic Input Current Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = V <sub>L</sub>	1	0.002		2		2		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON(WR)</sub>	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF See Figure 4	1	0.5		2		2	μs	
Turn-OFF Time	t <sub>OFF(RS)</sub>	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 50 pF See Figure 5	1	0.2		1		1		
Break-Before-Make Interval	t <sub>BBM</sub>		1	300	50		50		ns	
Access Time	t <sub>A</sub>	See Figure 4	1	100	20		20			
Write Pulse Width	t <sub>WR</sub>		1	60	300		300			
Reset Pulse Width	t <sub>RS</sub>	See Figure 5	1	90	300		300			
Source-OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V	1	15					pF	
Drain-OFF Capacitance	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0 V	1	85						
Channel ON Capacitance	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>	V <sub>S</sub> = 0 V, V <sub>WR</sub> = V <sub>L</sub> f = 140 kHz to 1 MHz	1	110						
Off Isolation		V <sub>RS</sub> = 0 V, R <sub>L</sub> = 2 k, C <sub>L</sub> = 3 pF V <sub>S</sub> = 10 V <sub>p-p</sub> , f = 10 kHz	1	65					dB	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 60 V V <sub>-</sub> = -60 V V <sub>L</sub> = V <sub>RS</sub> = 15 V V <sub>WR</sub> = GND = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> (All) = 0 V or 15 V <sup>e</sup>	1	0.002		2		2	μA
Negative Supply Current	I <sub>-</sub>		1	0.003		2		2	
Logic Supply Current	I <sub>L</sub>		1	0.002		2		2	
Minimum Supply Voltage	V <sub>+</sub> (min)		1	40					V
Minimum Logic Supply Voltage	V <sub>L</sub> (min)		1	8					

**NOTES:**

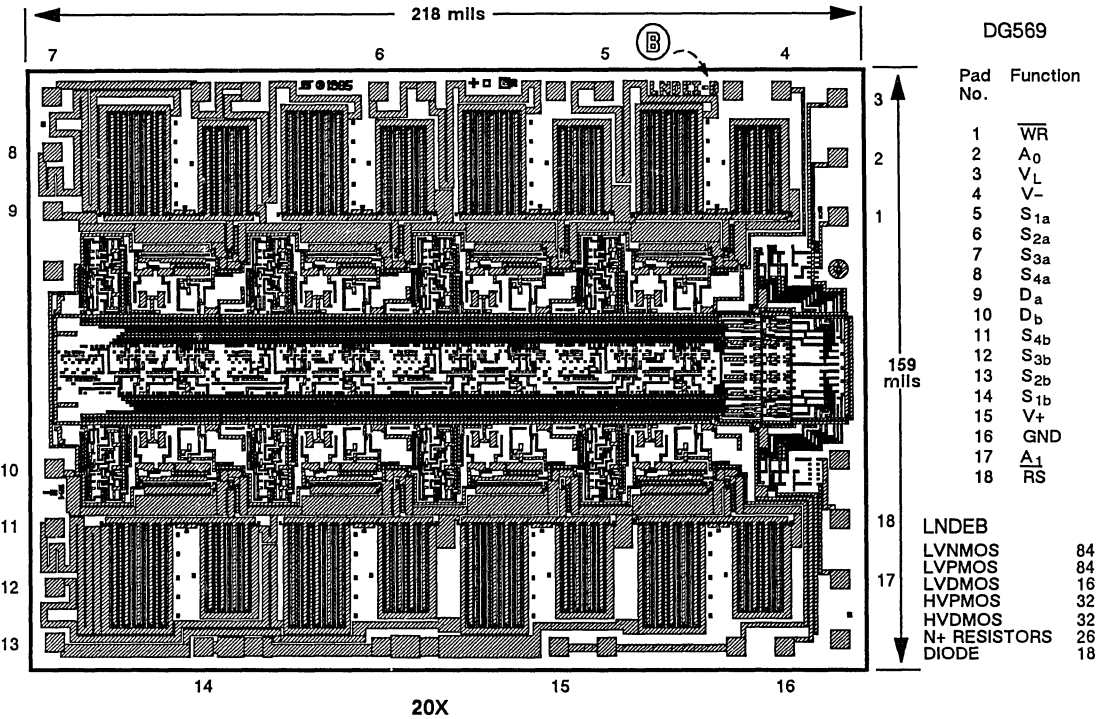
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. "Inputs" refer to digital inputs A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>, RS and WR.

**DIE TOPOGRAPHY**





**DIE TOPOGRAPHY (Cont'd)**



**TRUTH TABLES**

**DG568**

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	$\overline{WR}$	$\overline{RS}$	ON Switch
X	X	X		1	Maintains previous switch condition
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	1	0	1	2
0	1	0	0	1	3
0	1	1	0	1	4
1	0	0	0	1	5
1	0	1	0	1	6
1	1	0	0	1	7
1	1	1	0	1	8

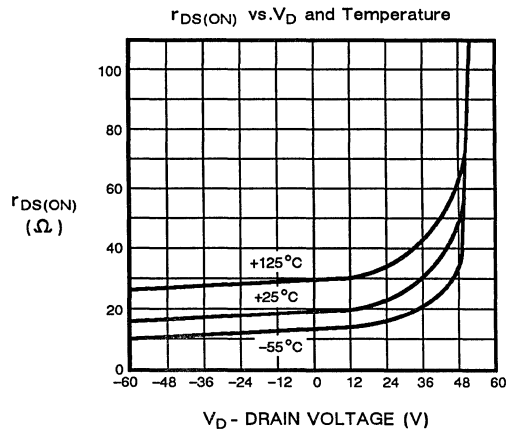
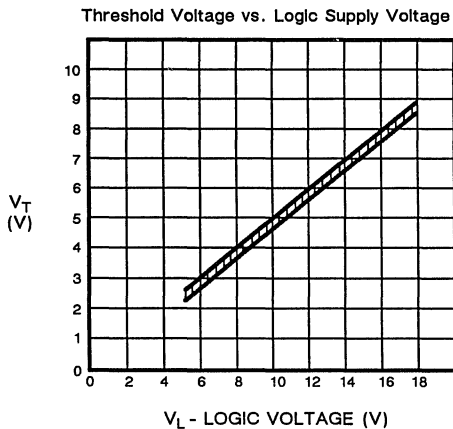
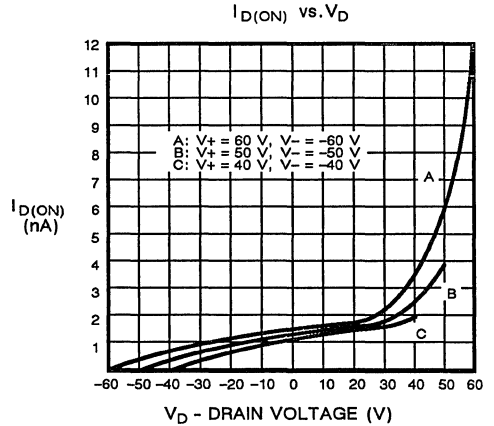
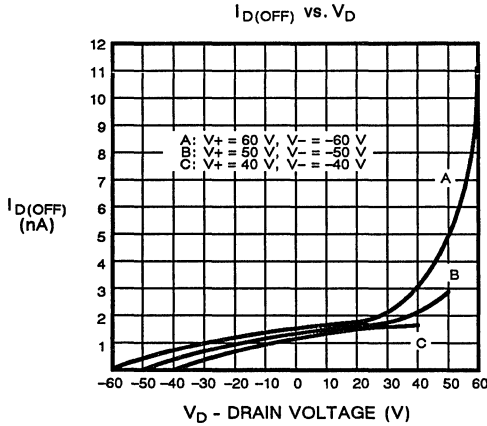
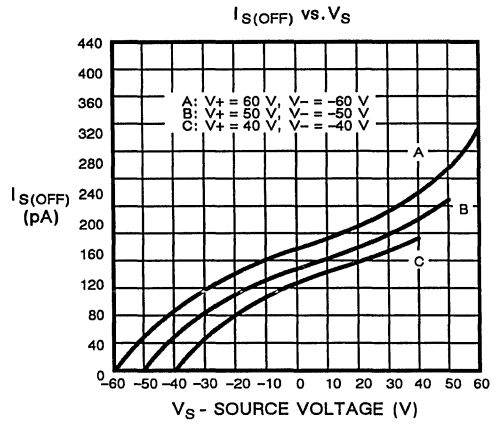
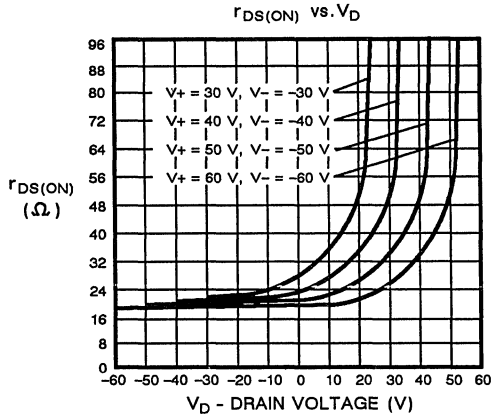
**DG569**

A <sub>1</sub>	A <sub>0</sub>	$\overline{WR}$	$\overline{RS}$	ON Switch
X	X		1	Maintains previous switch condition
X	X	X	0	NONE
0	0	0	1	1
0	1	0	1	2
1	0	0	1	3
1	1	0	1	4

Logic "1": V<sub>IN</sub> = V<sub>WRH</sub> ≥ 0.7 V<sub>L</sub>

Logic "1": V<sub>IN</sub> = V<sub>WRL</sub> ≤ 1 V

## TYPICAL CHARACTERISTICS (Cont'd)



## LEAKAGE TEST CIRCUITS

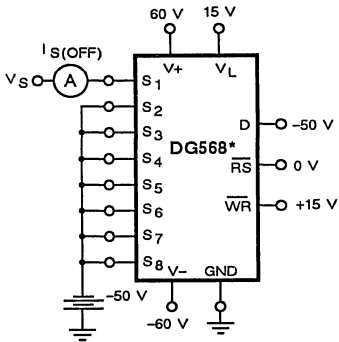


Figure 1.  $I_{S(OFF)}$  Test Circuit

\* Similar connections for DG569

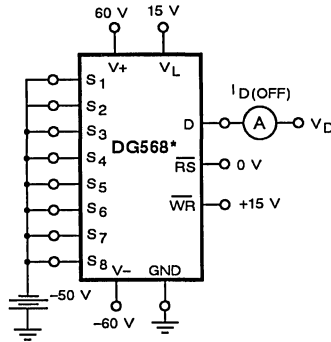


Figure 2.  $I_{D(OFF)}$  Test Circuit

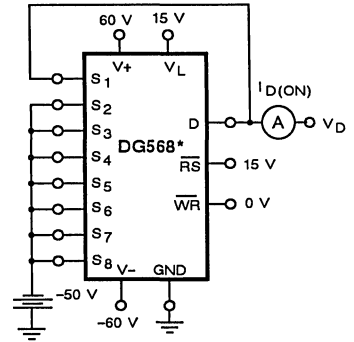
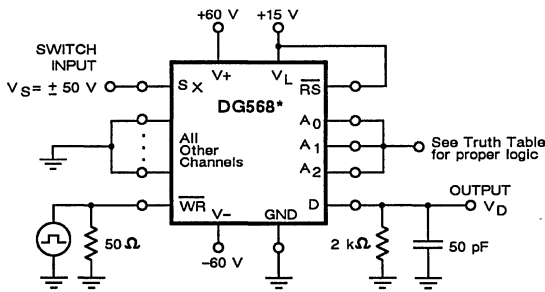


Figure 3.  $I_{D(ON)}$  Test Circuit

## $t_{ON(WR)}$ TIME TEST CIRCUIT



\* Similar connections for DG569

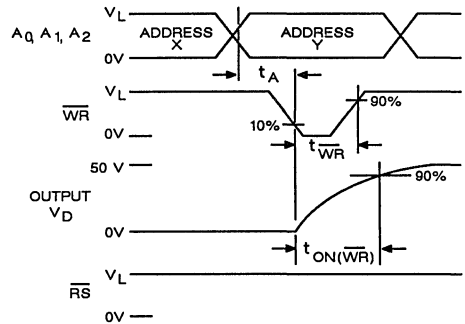
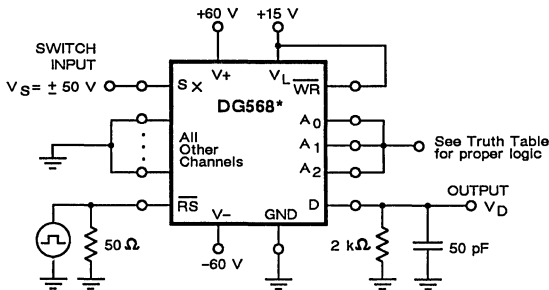


Figure 4.  $\overline{WR}$  Turn-ON Time

5

## $t_{OFF(RS)}$ TIME TEST CIRCUIT



\* Similar connections for DG569

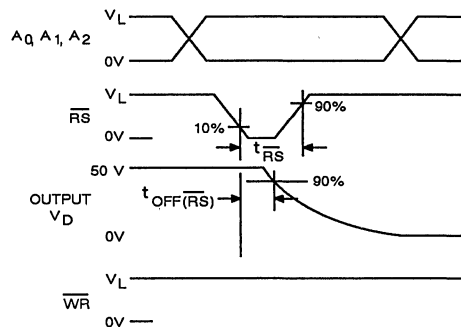
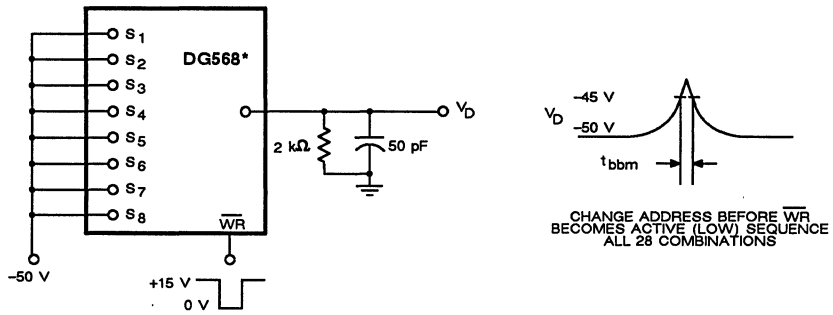


Figure 5.  $\overline{RS}$  Turn-OFF Time

## BREAK-BEFORE-MAKE TEST CIRCUIT



# Monolithic General Purpose CMOS Analog Switches

## FEATURES

- $\pm 15$  Volt Input Range
- ON Resistance  $< 50 \Omega$
- Break-Before-Make Switching
- TTL and CMOS Compatible

## BENEFITS

- Improved Signal Headroom
- Reduced Switching Errors
- No Shorting of Inputs
- Simple Interfacing

## APPLICATIONS

- Audio Switching
- Sample and Hold Circuits

## DESCRIPTION

The DG5040 family of solid state analog switches are recommended for general purpose applications in instrumentation, and process control. Built on the Siliconix PLUS 40 high voltage CMOS monolithic process, these devices provide ease-of-use and performance advantages to the system designer. Key performance features of the 5040 series are  $1 \mu\text{s}$  switching, low power supply requirements, and break-before-make switching which guarantees that an ON channel will be turned OFF before an OFF channel can turn ON. Each switch conducts equally in either direction, when ON, and blocks up to 30 volts peak-to-peak when OFF. OFF leakage

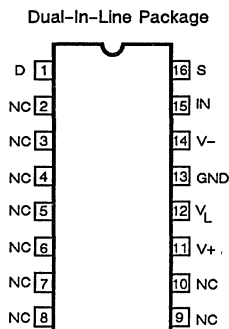
current is 1 nA maximum. A epitaxial layer prevents latch up.

There are six devices in this series, which are differentiated by the type of switch action as shown in the functional block diagrams. In all cases the switches are bidirectional and maintain almost constant ON resistance throughout their operating range.

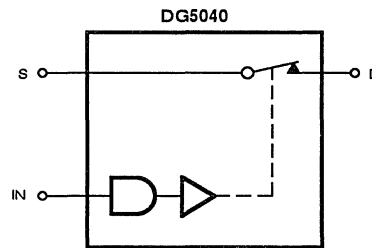
Package options include the 16-pin plastic and CerDIP. Temperature grades include commercial, C suffix (0 to 70°C), and military, A suffix (-55 to 125°C). For new designs, upgrade to the DG400-405 devices.

**5**

## PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE



Top View  
Order Numbers:  
CerDIP: DG5040AK  
          DG5040CK  
Plastic: DG5040CJ



One SPST Switch per Package

Truth Table\*

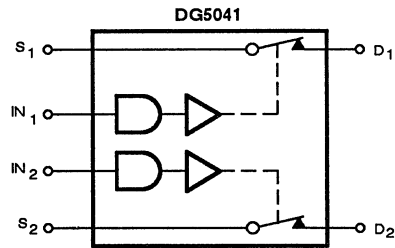
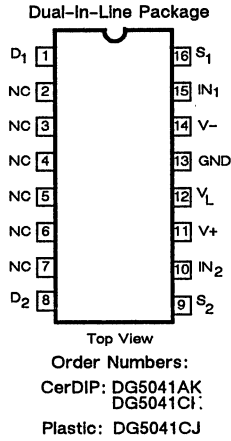
LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq 0.8 \text{ V}$

Logic "1"  $\geq 2.0 \text{ V}$

\*Switches Shown for Logic "1" Input.

## PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE (Cont'd)

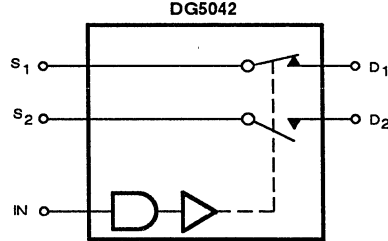
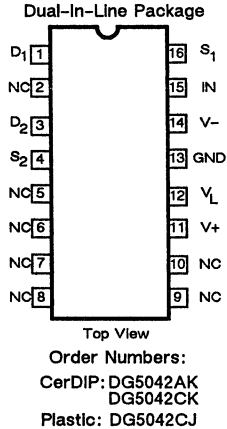


Two SPST Switches per Package

Truth Table\*

LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\lesseqgtr$  0.8 V  
Logic "1"  $\gtrless$  2.0 V

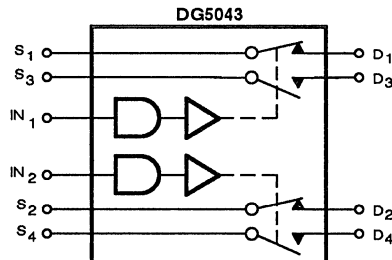
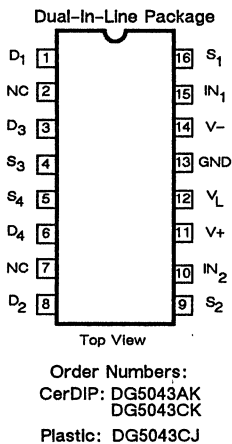


One SPDT Switch per Package

Truth Table\*

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Logic "0"  $\lesseqgtr$  0.8 V  
Logic "1"  $\gtrless$  2.0 V



Two SPDT Switches per Package\*

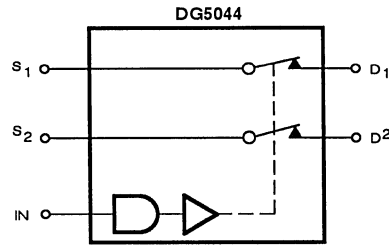
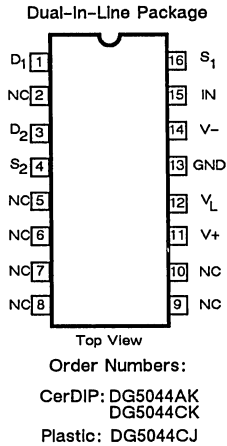
Truth Table\*

LOGIC	SWITCH 1 SWITCH 2	SWITCH 3 SWITCH 4
0	OFF ON	ON OFF
1	ON OFF	OFF ON

Logic "0"  $\lesseqgtr$  0.8 V  
Logic "1"  $\gtrless$  2.0 V

\*Switches Shown for Logic "1" Input

**PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE (Cont'd)**

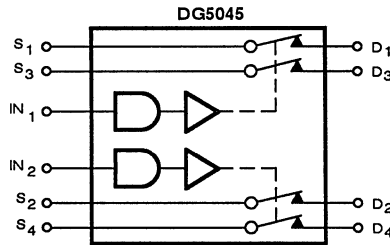
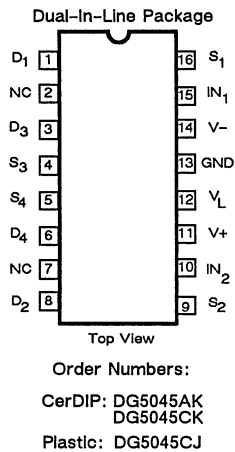


One DPST Switch per Package

Truth Table\*

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.0 V



Two DPST Switches per Package

Truth Table\*

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.0 V

\*Switches Shown for Logic "1" Input

**5**

**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to V-

V+ ..... 44V

VL ..... (GND - 0.3 V) to 44 V

GND ..... 25V

Digital Inputs<sup>f</sup> V<sub>S</sub>, V<sub>D</sub> ... (V- minus 2 V) to (V+ plus 2 V)  
or 30 mA, whichever occurs first

Current (any terminal except S or D) ..... 30 mA

Continuous Current (S or D) ..... 30 mA

Peak Current (S or D)

Pulsed 1 ms 10% duty cycle max ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C  
(C Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
(C Suffix) ..... 0 to 70°C

Power Dissipation\*

16-Pin Plastic DIP\*\* ..... 450 mW

16-Pin Ceramic DIP\*\*\* ..... 900 mW

\* All leads welded or soldered to PC board.

\*\* Derate 6 mW/°C above 75°C

\*\*\* Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V GND = 0 V V <sub>IN</sub> = 2.0 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C 2=125,70°C 3=-55,0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-15	15	-15	15	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±10 V	1,3 2			50 75		50 75	Ω
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>D</sub> = -14 V, V <sub>S</sub> = 14 V	1 2		-1 -100	1 100	-1 -100	1 100	nA
	I <sub>D(OFF)</sub>	V <sub>D</sub> = 14 V, V <sub>S</sub> = -14 V	1 2		-1 -100	1 100	-1 -100	1 100	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 14 V	1 2			2 200		2 200	nA
		V <sub>S</sub> = V <sub>D</sub> = -14 V	1 2		-2 -200		-2 -200		
<b>INPUT</b>									
Input Current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>IN</sub> under test = 0.8 V	1,2		-1.0	1.0	-1.0	1.0	μA
Input Current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>IN</sub> under test = 2.0 V	1,2		-1.0	1.0	-1.0	1.0	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	V <sub>S</sub> = ±10 V R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 35 pF See Figure 1A	1			1000		1200	ns
Turn-OFF Time	t <sub>OFF</sub>		1			500		700	
Charge Injection <sup>c</sup>	Q	C <sub>L</sub> = 10,000 pF V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω	1	30					pC
Off Isolation <sup>c</sup>		R <sub>L</sub> = 75 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	1	75					dB
Crosstalk <sup>c</sup> (Channel-to-Channel)		R <sub>L</sub> = 75 Ω, V <sub>S</sub> = 2 Vp-p f = 1 MHz	1	89					
Source-OFF Capacitance <sup>c</sup>	C <sub>S(OFF)</sub>	V <sub>D</sub> = V <sub>S</sub> = 0 V f = 1 MHz	1	15					pF
Drain-OFF Capacitance <sup>c</sup>	C <sub>D(OFF)</sub>		1	17					
Channel ON Capacitance <sup>c</sup>	C <sub>D(ON)</sub> + C <sub>S(ON)</sub>		1	45					

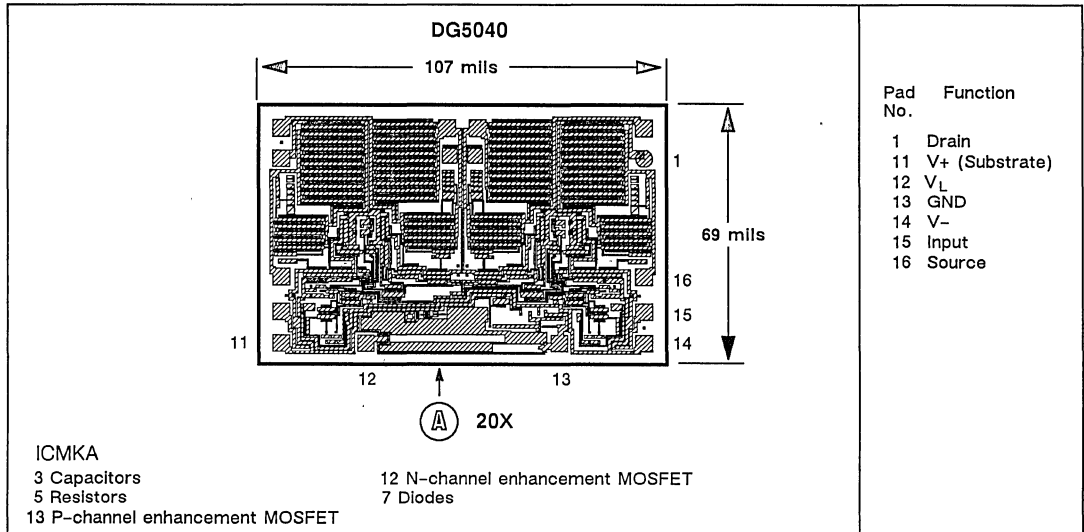


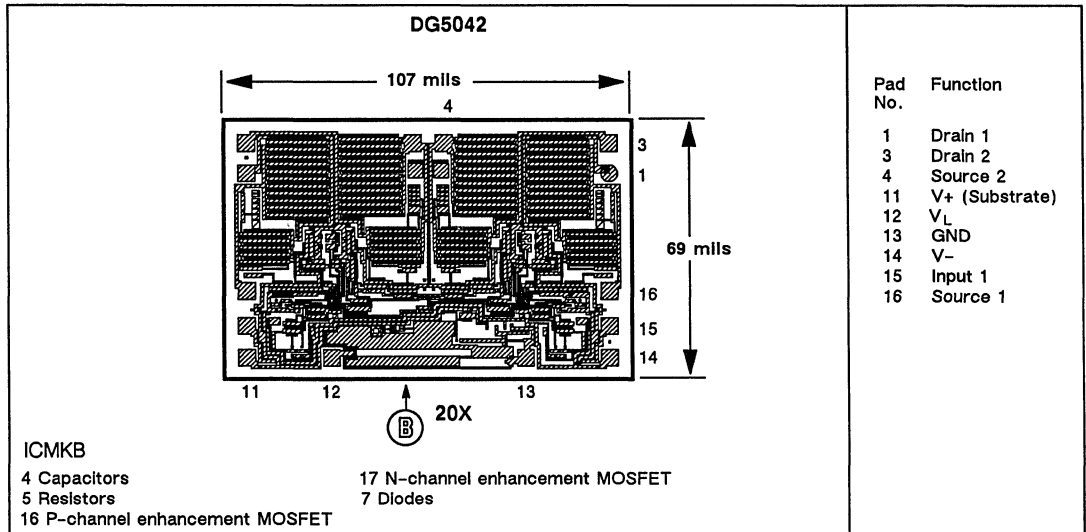
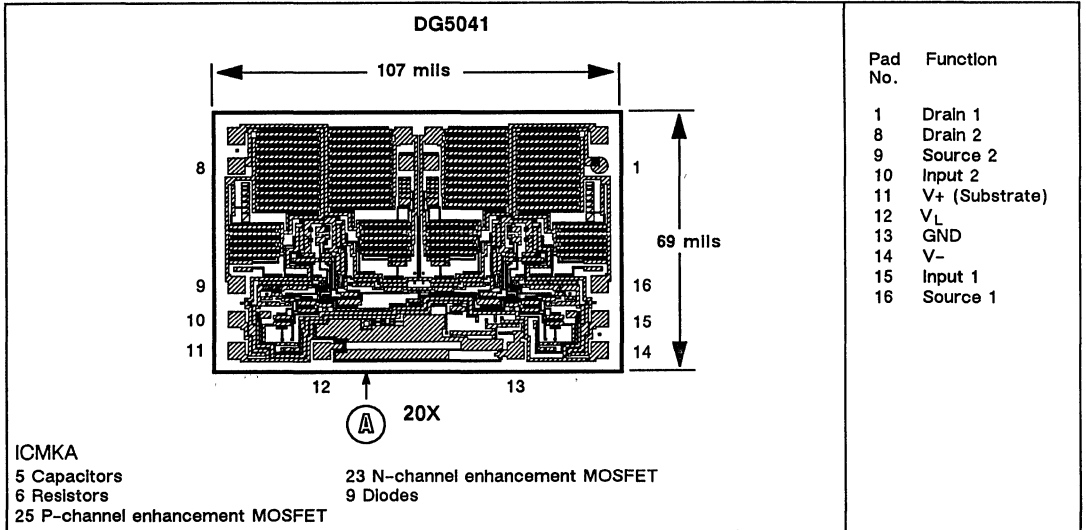
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V GND = 0 V V <sub>IN</sub> = 2.0 V, 0.8 V <sup>e</sup>	LIMITS				UNIT		
			1=25°C		A SUFFIX			C SUFFIX	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		MIN <sup>b</sup>	MAX <sup>b</sup>
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0.0 or 2.4 V	1,2		300		300	μA	
Negative Supply Current	I <sub>-</sub>		1,2		-300		-300		
Logic Supply Current	I <sub>L</sub>		1,2		300		300		
Ground Current	I <sub>GND</sub>		1,2		-300		-300		

**NOTES:**

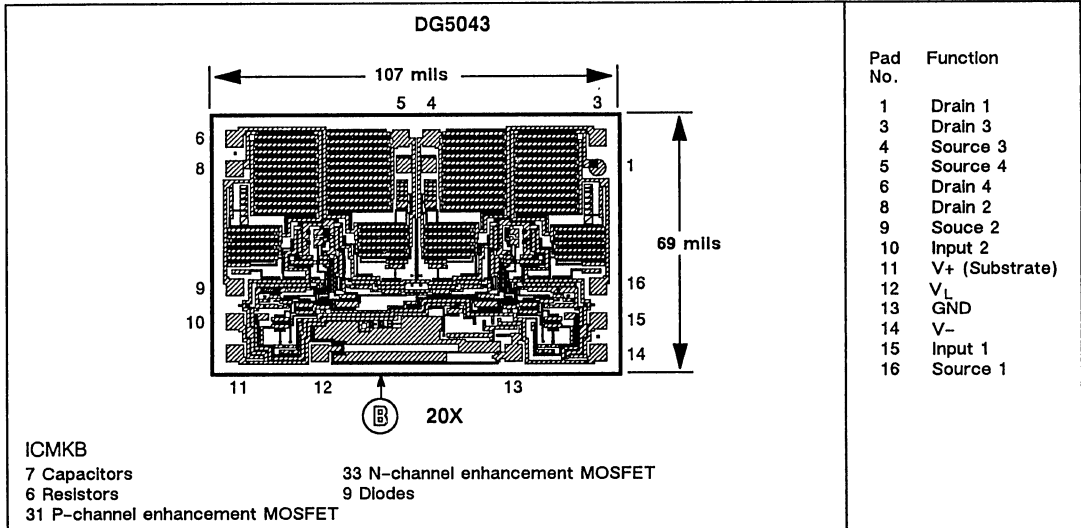
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = Input voltage to perform proper function.
- f. Signals on S<sub>X</sub>, D<sub>X</sub> or IN<sub>X</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to 30 mA.

**DIE TOPOGRAPHY**

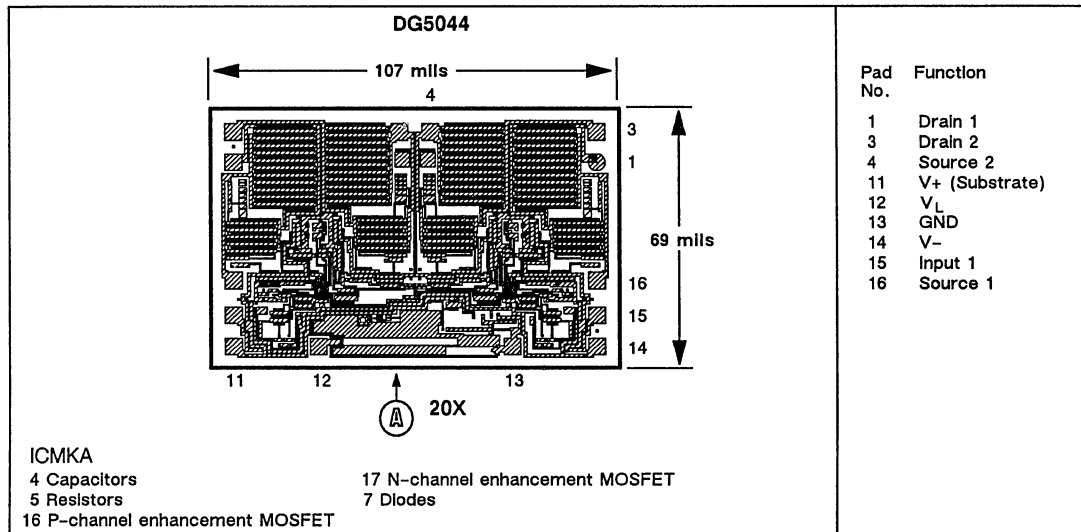




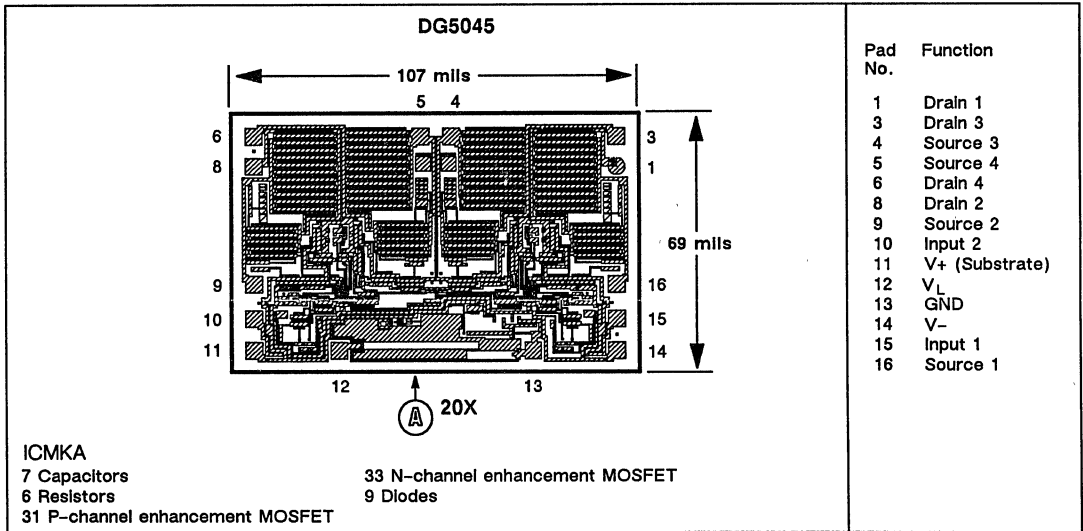
**DIE TOPOGRAPHY (Cont'd)**



**5**

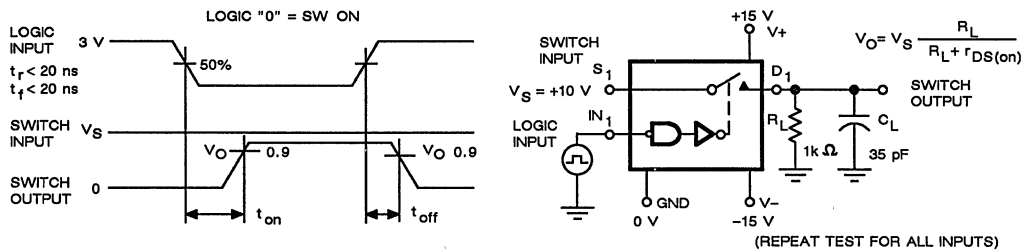


## DIE TOPOGRAPHY (Cont'd)

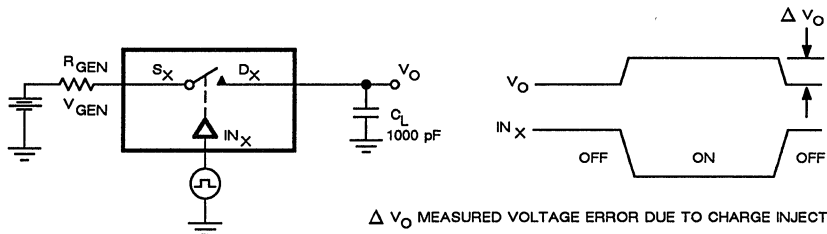


## SWITCHING TIME TEST CIRCUIT

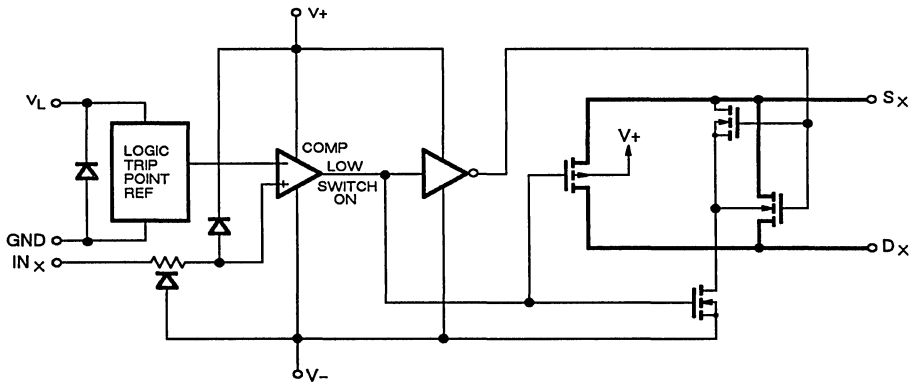
Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



## CHARGE INJECTION TEST CIRCUIT



**SCHEMATIC DIAGRAM (Typical Channel)**



## Low-Power – High-Speed CMOS Analog Switches

### FEATURES

- $\pm 15$  Volt Input Range
- ON Resistance < 50  $\Omega$
- Very Fast Switching Action  
( $t_{ON} < 100$  ns)  
( $t_{OFF} < 75$  ns)
- Ultra Low Power Requirements  
( $I_S < 1 \mu A$ )
- TTL and CMOS Compatible

### BENEFITS

- Improved Signal Headroom
- Low Signal Errors
- Break-Before-Make Switching Action
- Reduced Power Consumption
- Simple Interfacing

### APPLICATIONS

- Audio Switching
- Precision Switching
- High-Speed Switching
- Battery-Operated Systems

### DESCRIPTION

The DG5140 family of solid state analog switches is built on the Siliconix proprietary high voltage silicon gate process to achieve high voltage rating and superior switch time ON/OFF performance. Key performance features of the DG5140 series are break-before-make switching action to guarantee that an ON channel will be turned OFF before the OFF channel can turn ON, ultra-low power supply requirements, and TTL and CMOS compatibility. Each switch conducts equally well in both directions when ON and blocks up to 30 Volts peak-to-peak when OFF. With switch OFF leakage less than 100 pA and maximum power supply current of 1  $\mu A$

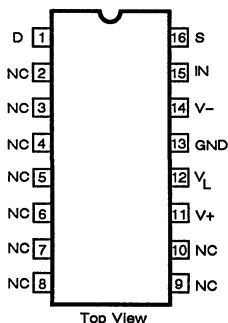
(A Suffix), these switches are ideal for battery powered industrial and military applications. An epitaxial layer prevents latchup.

There are six devices in this series, which are differentiated by the type of switch action as shown in the functional block diagrams. In all cases the switches are bidirectional and maintain almost constant ON resistance throughout their operating range.

Package options include the 16-pin plastic and ceramic DIP. Temperature grades include commercial, C suffix (0 to 70°C), and military, A suffix (-55 to 125°C).

### PIN CONFIGURATION

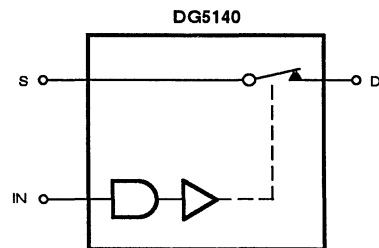
Dual-In-Line Package



Top View

Order Numbers:  
CerDIP: DG5140AK, DG5140AK/883,  
DG5140CK  
Plastic: DG5140CJ

### FUNCTIONAL BLOCK DIAGRAM



One SPST Switch per Package

Truth Table \*

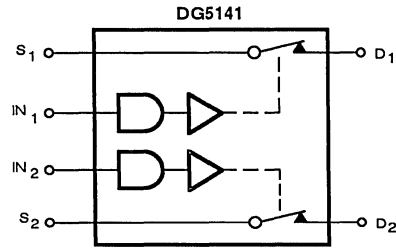
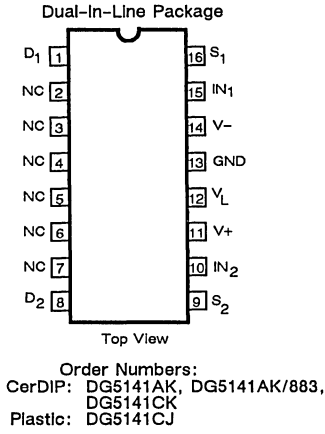
LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq 0.8$  V  
Logic "1"  $\geq 2.4$  V

\* Switches Shown for Logic "1" Input

**PIN CONFIGURATION (Cont'd)**

**FUNCTIONAL BLOCK DIAGRAM (Cont'd)**

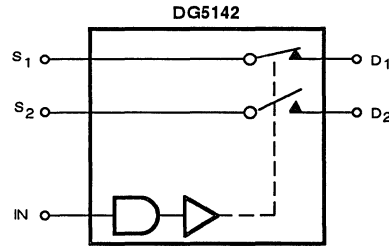
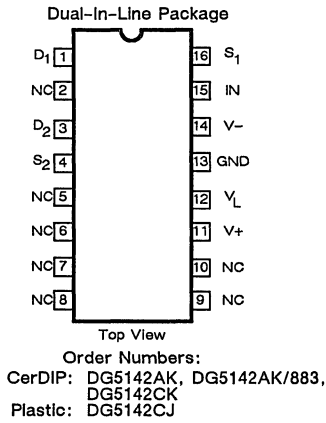


Two SPST Switches per Package

Truth Table \*

LOGIC	SWITCH
0	OFF
1	ON

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.4 V

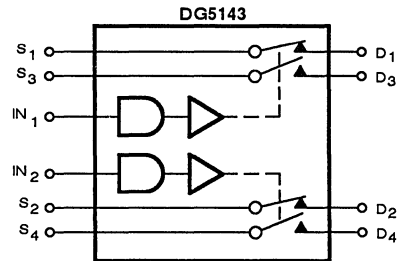
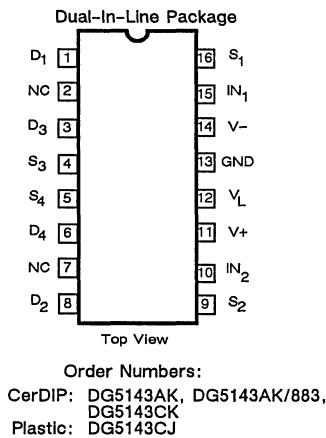


One SPDT Switch per Package

Truth Table \*

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.4 V



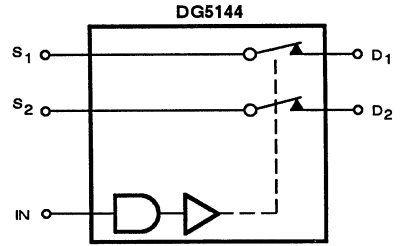
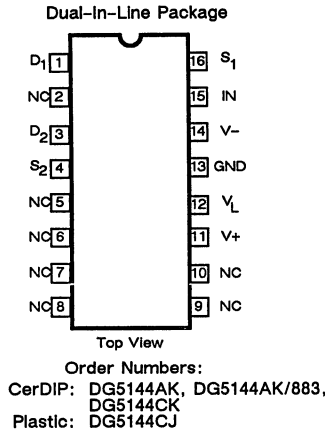
Two SPDT Switches per Package

Truth Table \*

LOGIC	SWITCH 1	SWITCH 2	SWITCH 3	SWITCH 4
0	OFF	ON	ON	OFF
1	ON	ON	OFF	OFF

Logic " 0 "  $\leq$  0.8 V  
Logic " 1 "  $\geq$  2.4 V

\* Switches Shown for Logic "1" Input

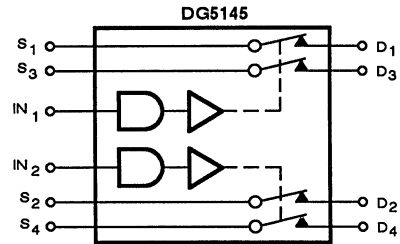
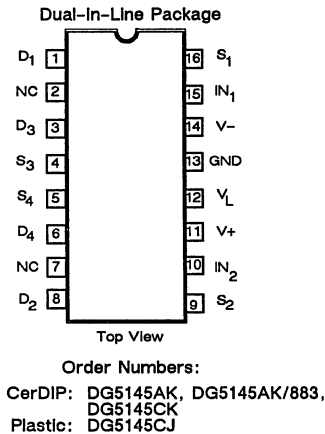


One DPST Switch per Package

Truth Table \*

LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V



Two DPST Switches per Package

Truth Table \*

LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq$  0.8 V  
 Logic "1"  $\geq$  2.4 V

\* Switches Shown for Logic "1" Input

### ABSOLUTE MAXIMUM RATINGS

(V+) - (V-)	< 36 V
(V+) - (V <sub>D</sub> )	< 30 V
(V <sub>D</sub> ) - (V-)	< 30 V
(V <sub>D</sub> ) - (V <sub>S</sub> )	< ±22 V
(V <sub>L</sub> ) - (V-)	< 33 V
(V <sub>L</sub> ) - (V <sub>IN</sub> )	< 30 V
V <sub>L</sub>	< 20 V
V <sub>IN</sub>	< 20 V
Continuous Current, Any Terminal	30 mA

Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	100 mA
Storage Temperature (A Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	-55 to 125°C
(C Suffix)	0 to 70°C
Power Dissipation (Package)*	
16-Pin Plastic DIP**	450 mW
16-Pin CerDIP***	900 mW

\* All leads welded or soldered to PC board.

\*\* Derate 6 mW/°C above 75°C.

\*\*\* Derate 12 mW/°C above 75°C.



## ELECTRICAL CHARACTERISTICS <sup>a</sup>

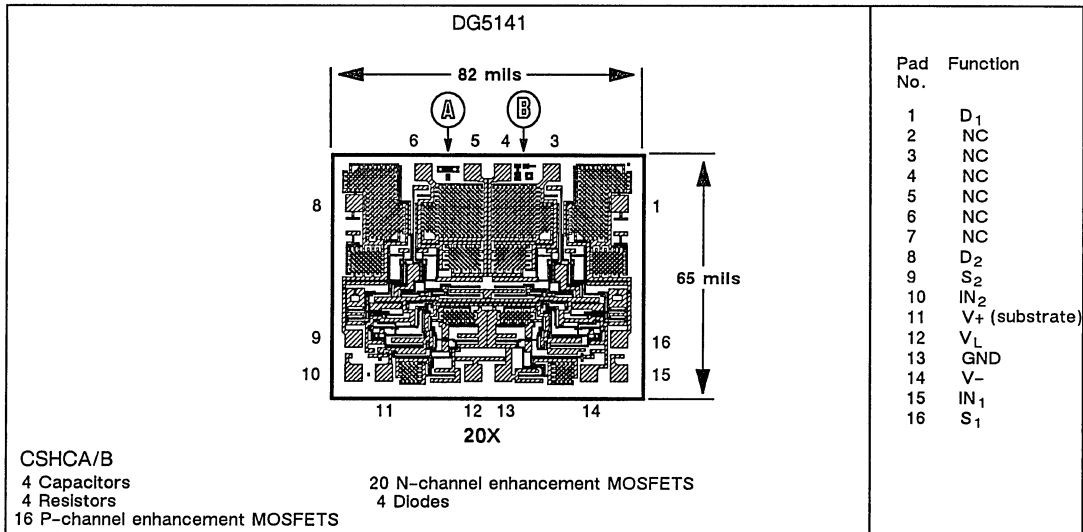
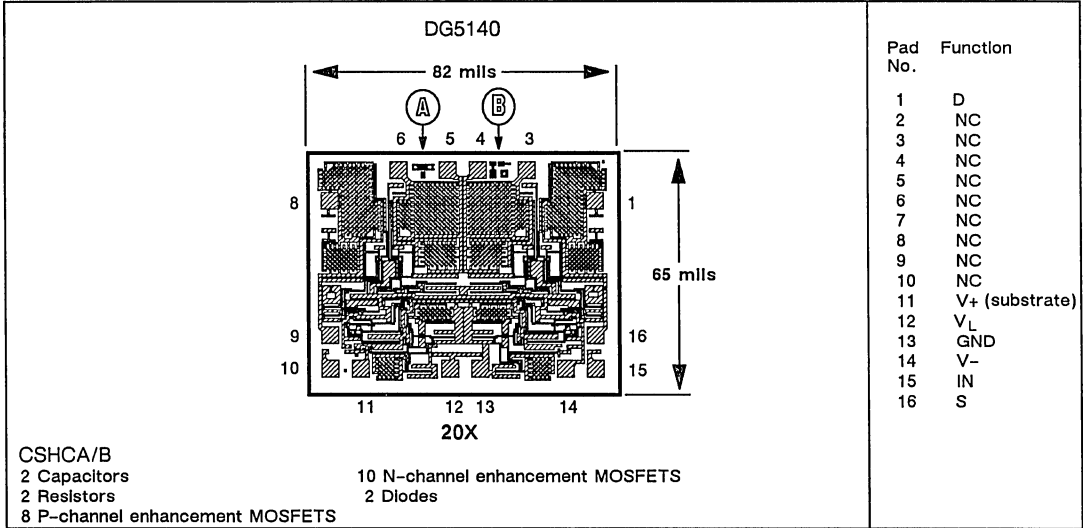
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-14	14	-14	14	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±10 V	1 2, 3			50 75		75 100	Ω
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>D</sub> = -10 V, V <sub>S</sub> = 10 V V <sub>D</sub> = 10 V, V <sub>S</sub> = -10 V	1 2			0.5 20		5 20	nA
	I <sub>D(OFF)</sub>		1 2			0.5 20		5 20	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = -10 to 10 V	1 2			1 40		2 40	
<b>INPUT</b>									
Input Current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>IN</sub> under test = 0.8 V All Other = 2.4 V	1,2			1		1	μA
Input Current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>IN</sub> under test = 2.4 V All Other = 0.8 V	1,2			1		1	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF See Figure 1 DG5140-DG5145	1			150		175	
Turn-OFF Time	t <sub>OFF</sub>		1			125		150	
Switch ON Time <sup>c</sup>	t <sub>ON</sub>	DG5140 DG5141	Figure 2	1		100		150	ns
			Figure 3	1		150		175	
		DG5142 DG5143	Figure 2 and 4	1		175		250	
			Figure 5	1		200		300	
Switch OFF Time <sup>c</sup>	t <sub>OFF</sub>	DG5140 DG5141	Figure 2	1		75		125	
			Figure 3	1		125		150	
		DG5142 DG5143 DG5144 DG5145	Figures 2, 3, 4 and 5	1		125		150	
				1		125		150	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V V <sub>-</sub> = -15 V V <sub>L</sub> = 5 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
Break-Before-Make Time	t <sub>ON</sub> - t <sub>OFF</sub>	See Figure 2	1		10		5		ns
			1		10		5		
Charge Injection <sup>c</sup>	Q	C <sub>L</sub> = 10,000 pF V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0Ω	1			100		150	pC
Off Isolation <sup>c</sup>		R <sub>L</sub> = 100Ω, C <sub>L</sub> ≤ 5 pF f = 1 MHz	1		-54		-50		dB
Crosstalk <sup>c</sup> (Channel-to-Channel)		Any Other Channel Switches R <sub>L</sub> = 100Ω, C <sub>L</sub> ≤ 5 pF f = 1 MHz	1			-54		-50	
SUPPLY									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 V or 5 V Switch Duty Cycle < 10%	1			1		10	μA
Negative Supply Current	I <sub>-</sub>		1		-1		-10		
Logic Supply Current	I <sub>L</sub>		1			1		10	
Ground Current	I <sub>GND</sub>		1		-1		-10		

**NOTES:**

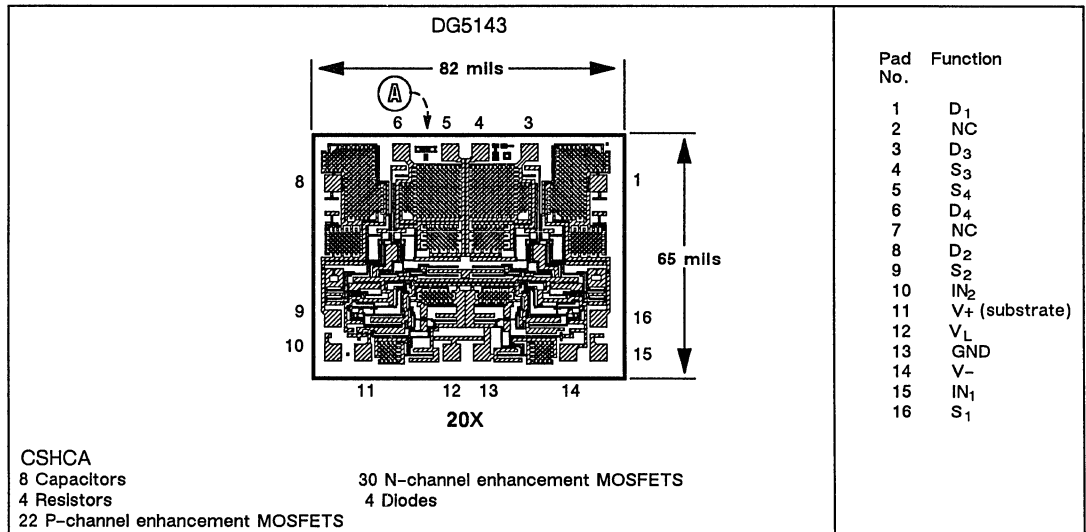
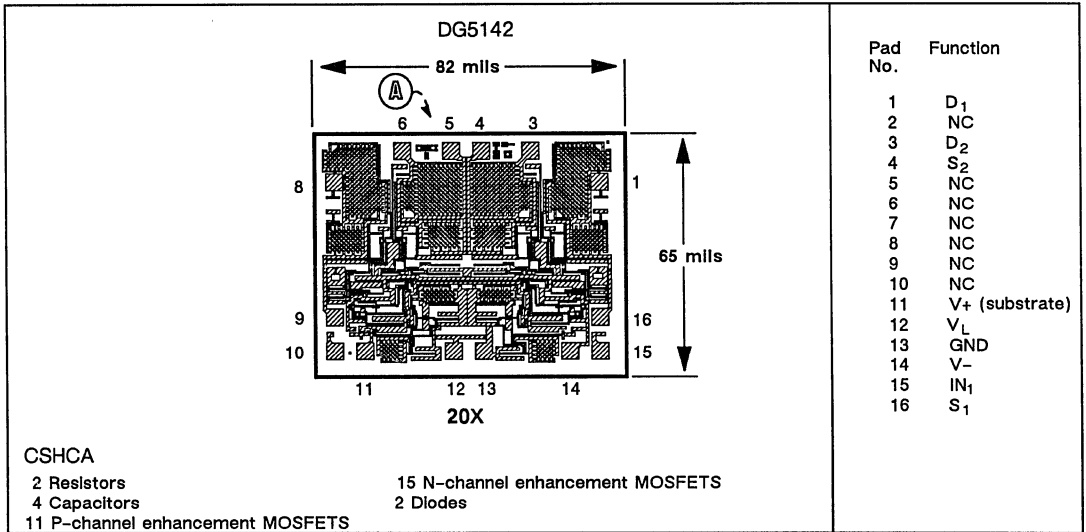
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = Input voltage to perform proper function.
- f. Signals on S<sub>X</sub>, D<sub>X</sub> or IN<sub>X</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to 30 mA.

**DIE TOPOGRAPHY**

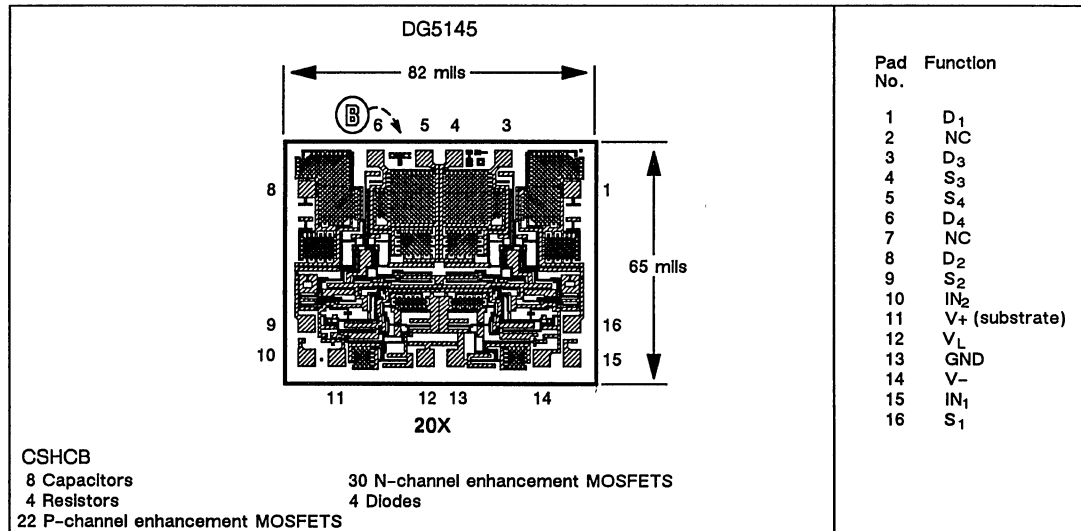
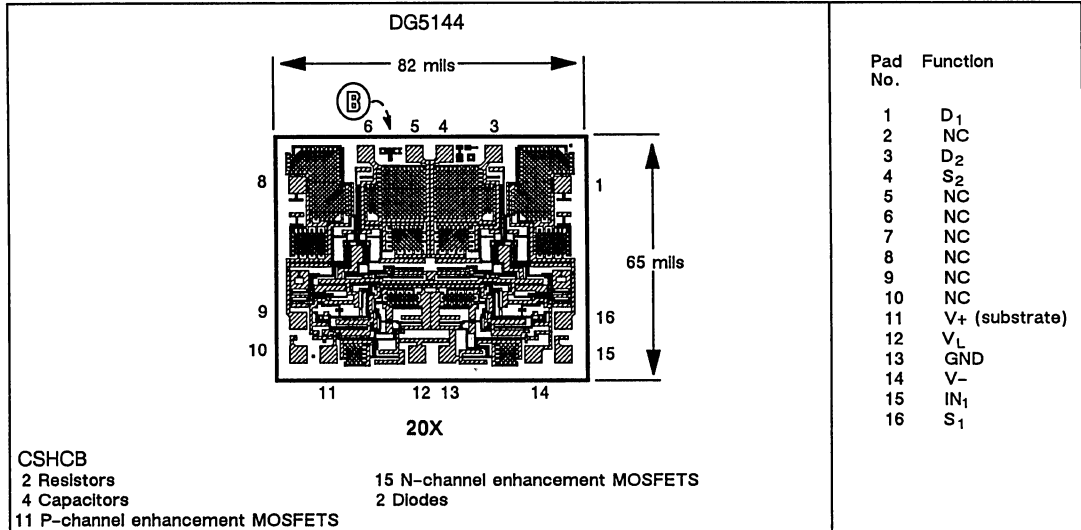


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## DIE TOPOGRAPHY (Cont'd)



**DIE TOPOGRAPHY (Cont'd)**



## SWITCHING TIME TEST CIRCUITS

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

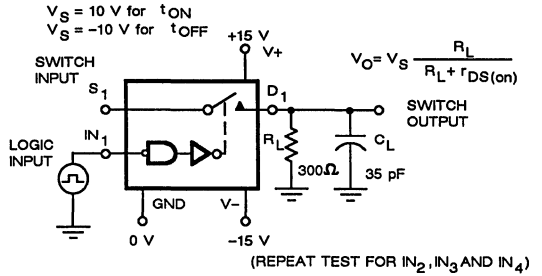
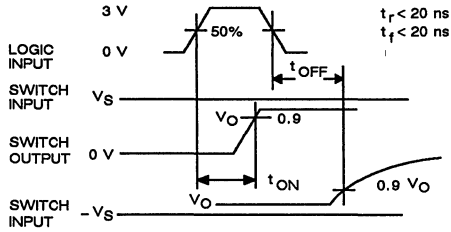


Figure 1.

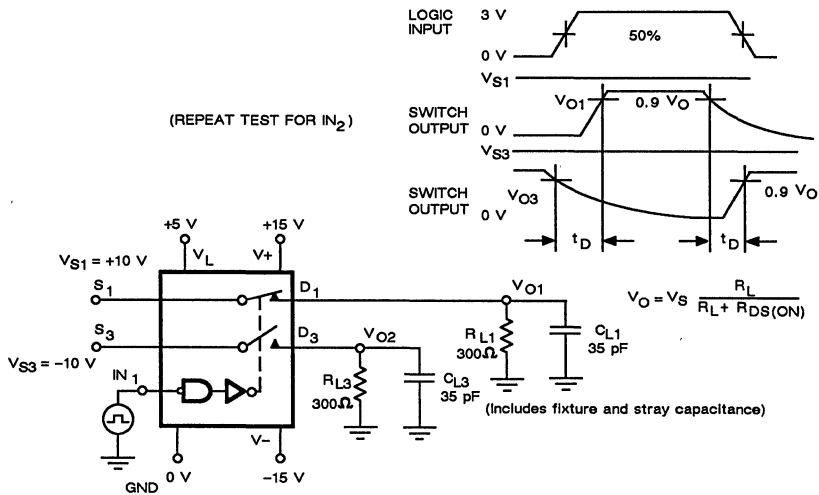


Figure 2.

## High-Speed Quad SPST CMOS Analog Switch

### FEATURES

- Fast Switching Action  
 $t_{ON} < 20 \text{ ns}$   
 $t_{OFF} < 35 \text{ ns}$
- Low ON Resistance  
 $(r_{DS(ON)} < 30 \Omega)$
- Single-Supply Operation  
 (5 V to 12 V)
- Low Charge Injection  
 $(Q < 10 \text{ pC})$
- TTL Compatible
- ESDS Protection  $> \pm 4000 \text{ V}$

### BENEFITS

- Improved Data Throughput
- Reduced Switching Errors
- Simplified Power Supply
- Reduced Switching Transients
- Simplified Interfacing
- Improved Reliability

### APPLICATIONS

- Fast Sample/Hold
- Precision Instrumentation
- Computer Peripherals
- Low Noise  
 Op Amp Gain Switching
- Military Systems

### DESCRIPTION

The DG601 is a high performance quad SPST CMOS analog switch intended for applications where fast switching, low charge injection and low ON resistance are required. The DG601 features single-supply operation, and is TTL-compatible with either a single 12 V supply, a single 5 V supply, or with 5 V supplies.

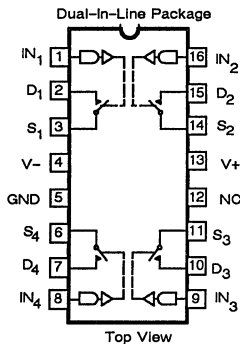
Applications for the DG601 include 12 V systems requiring TTL or 5 V logic levels, such as disk drives and other computer peripherals. The fast switching time and low charge injection make the DG601 ideal

for high speed data acquisition applications such as sample and hold amplifiers, channel selection and gain ranging.

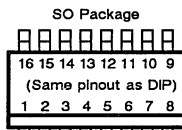
The DG601 is built on the Siliconix proprietary PolyMOS process, allowing 22 V rail-to-rail maximum operation and low parasitic capacitance to facilitate high speed switching. It is available in 16-pin plastic DIP and SO packages for industrial, D suffix (-40 to 85°C), and in the CerDIP for military, A suffix (-55 to 125°C) temperature ranges.

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### FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION & TRUTH TABLE



Order Numbers:  
 CerDIP: DG601AK  
 Plastic: DG601DJ



Order Number:  
 DG601DY

Four SPST Switches per Package

Truth Table	
LOGIC	SWITCH
0	ON
1	OFF

Logic "0"  $\leq 0.8 \text{ V}$   
 Logic "1"  $\geq 2.0 \text{ V}$

## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V<sub>-1</sub>

V<sub>+</sub> ..... 22 V

GND ..... 13 V

Digital Inputs<sup>1</sup>, V<sub>S</sub>, V<sub>D</sub> ..... (V<sub>-</sub>) -2 V to (V<sub>+</sub>) plus 2 V  
..... or 30 mA, whichever occurs first

Current (any terminal) ..... 30 mA

Current (S or D) ..... 100 mA  
(Pulsed 1 ms at 10% duty cycle)

ESDS Protection<sup>c</sup> ..... ±4000 V

Storage Temperature (A Suffix) ..... -65 to 150°C  
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C  
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package) \*

16-Pin Plastic DIP\*\* ..... 470 mW

16-Pin CerDIP\*\*\* ..... 900 mW

16-Pin SO\*\*\*\* ..... 900 mW

- \* All leads welded or soldered to PC board
- \*\* Derate 6.5 mW/°C above 25°C
- \*\*\* Derate 12 mW/°C above 75°C
- \*\*\*\* Derate 7.7 mW/°C above 25°C

1. Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V<sub>+</sub> or V<sub>-</sub> will be clamped by internal diodes. Limit forward diode current to 30 mA.

ELECTRICAL CHARACTERISTICS <sup>a</sup>								PART 1	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = 0 V GND = 0 V V <sub>IN</sub> = 2.0, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		0	12	0	12	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>+</sub> = 10.8 I <sub>S</sub> = 1 mA, V <sub>D</sub> = 10 V, 2 V	1,3 2			30 50		30 50	Ω
Delta Drain-Source ON Resistance	Δr <sub>DS(ON)</sub>	V <sub>+</sub> = 10.8 I <sub>S</sub> = -10 mA, V <sub>D</sub> = 3 V, 9 V	1,3 2			3 5		3 5	
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>+</sub> = 13.2 V, V <sub>-</sub> = 0 V V <sub>D</sub> = 12.2 V, 1 V V <sub>S</sub> = 1 V, 12.2 V	1 2		-1 -100	1 100	-1 -100	1 100	nA
	I <sub>D(OFF)</sub>		1 2		-1 -100	1 100	-1 -100	1 100	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>+</sub> = 13.2 V, V <sub>-</sub> = 0 V V <sub>S</sub> , V <sub>D</sub> = 1 V, 12.2 V	1 2		-1 -200	1 200	-1 -200	1 200	
<b>INPUT</b>									
Input Current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0 V All Other = 5 V	1,2		-10		-10		μA
Input Current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 5 V All Other = 0 V	1,2			10		10	
<b>DYNAMIC</b>									
Turn-ON Time	t <sub>ON</sub>	R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35 pF See Figure 1	1			35		35	ns
Turn-OFF Time	t <sub>OFF</sub>		1			20		20	
Break-Before-Make Time Delay	t <sub>d</sub>	R <sub>L</sub> = 300Ω, C <sub>L</sub> = 35 pF	1		15		15		



ELECTRICAL CHARACTERISTICS <sup>a</sup>							PART 1		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = 0 V GND = 0 V V <sub>IN</sub> = 2.0, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
Charge Injection	Q	C <sub>L</sub> = 1,000 pF V <sub>gen</sub> = 6 V, R <sub>gen</sub> = 0 Ω See Figure 2	1			15		15	pC
Off Isolation	OIRR	R <sub>L</sub> = 75 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	1						dB
Crosstalk (Channel-to-Channel)		Any Other Channel Switches R <sub>L</sub> = 75 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	1						
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz V <sub>S</sub> = 0 V	1						pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		1						
Drain and Source ON Capacitance	C <sub>S(ON)</sub> + C <sub>D(ON)</sub>		1						
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0.0 V or 5.0 V	1,2 3			6 8		6 8	mA
Negative Supply Current	I <sub>-</sub>		1,2 3		-6 -8		-6 -8		

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ELECTRICAL CHARACTERISTICS <sup>a</sup>							PART 2		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 5 V V <sub>-</sub> = -5 V GND = 0 V V <sub>IN</sub> = 2.0, 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		1,2,3		-5	5	-5	5	V
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	V <sub>+</sub> = 4.5 V, V <sub>-</sub> = -4.5 V I <sub>S</sub> = -10 mA, V <sub>D</sub> = ±	1,3 2			40 60		40 60	Ω
Delta Drain-Source ON Resistance	Δr <sub>DS(ON)</sub>	V <sub>+</sub> = 4.5 V, V <sub>-</sub> = -4.5 V I <sub>S</sub> = -10 mA, V <sub>D</sub> = 5, 0, -5 V	1,3 2			4 6		4 6	
Switch OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>+</sub> = 5.5 V, V <sub>-</sub> = -5.5 V V <sub>D</sub> = ± 4.5 V V <sub>S</sub> = ± 4.5 V	1 2		-1 -100	1 100	-1 -100	1 100	nA
	I <sub>D(OFF)</sub>		1 2		-1 -100	1 100	-1 -100	1 100	
Channel ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>+</sub> = 5.5 V, V <sub>-</sub> = -5.5 V V <sub>S</sub> = V <sub>D</sub> = ± 4.5 V	1 2		-1 -200	1 200	-1 -200	1 200	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										PART 2
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 5 V V <sub>-</sub> = -5 V GND = 0 V V <sub>IN</sub> = 2.0, 0.8 V <sup>e</sup>	LIMITS						UNIT	
			1=25°C		A SUFFIX		D SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUT</b>										
Input Current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0 V All Other = 5 V	1,2		-10		-10			μA
Input Current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 5 V All Other = 0 V	1,2			10		10		
<b>DYNAMIC</b>										
Turn-ON Time	t <sub>ON</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF See Figure 1	1			50		50		ns
Turn-OFF Time	t <sub>OFF</sub>		1			30		30		
Break-Before-Make Time Delay	t <sub>d</sub>	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF	1		15		15			
Charge Injection	Q	C <sub>L</sub> = 1,000 pF V <sub>gen</sub> = 0 V, R <sub>gen</sub> = 0 Ω See Figure 2	1		-15	15	-15	15		pC
Off Isolation	OIRR	R <sub>L</sub> = 75 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	1							dB
Crosstalk (Channel-to-Channel)		Any Other Channel Switches R <sub>L</sub> = 75 Ω, C <sub>L</sub> = 5 pF f = 1 MHz	1							
Source-OFF Capacitance	C <sub>S(OFF)</sub>	f = 1 MHz V <sub>S</sub> = 0 V	1							pF
Drain-OFF Capacitance	C <sub>D(OFF)</sub>		1							
Drain and Source ON Capacitance	C <sub>S(ON)</sub> + C <sub>D(ON)</sub>		1							
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 5.5 V, V <sub>-</sub> = -5.5 V V <sub>IN</sub> = 0.0 V or 5.0 V	1,2 3			5 6		5 6		mA
Negative Supply Current	I <sub>-</sub>		1,2 3		-5 -6		-5 -6			

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

**PART 3**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 5\text{ V}$ $V_- = 0\text{ V}$ $GND = 0\text{ V}$ $V_{IN} = 2.0, 0.8\text{ V}^e$	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$		1,2,3		0	5	0	5	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$V_+ = 4.5\text{ V}$ $I_S = -10\text{ mA}, V_D = 2, 3.5\text{ V}$	1,3 2			100 125		100 125	$\Omega$
Delta Drain-Source ON Resistance	$\Delta r_{DS(ON)}$	$V_+ = 4.5\text{ V}$ $I_S = -10\text{ mA}, V_D = 2, 3.5\text{ V}$	1,3 2			10 12.5		10 12.5	
Switch OFF Leakage Current	$I_{S(OFF)}$	$V_+ = 5.5\text{ V}$	$V_D = 1\text{ V}$ $V_S = 4.5\text{ V}$	1 2		-1 -100	1 100	-1 -100	1 100
	$I_{D(OFF)}$		$V_D = 4.5\text{ V}$ $V_S = 1\text{ V}$	1 2		-1 -100	1 100	-1 -100	1 100
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_+ = 5.5\text{ V}$ $V_S = V_D = 4.5, 1\text{ V}$	1 2		-1 -200	1 200	-1 -200	1 200	nA
<b>INPUT</b>									
Input Current with $V_{IN}$ LOW	$I_{IL}$	$V_{IN}$ Under Test = 0 V All Other = 5 V	1,2		-10		-10		$\mu\text{A}$
Input Current with $V_{IN}$ HIGH	$I_{IH}$	$V_{IN}$ Under Test = 5 V All Other = 0 V	1,2			10		10	
<b>DYNAMIC</b>									
Turn-ON Time	$t_{ON}$	$R_L = 300\Omega, C_L = 35\text{ pF}$ See Figure 1	1			55		55	ns
Turn-OFF Time	$t_{OFF}$		1			35		35	
Break-Before-Make Time Delay	$t_d$	$R_L = 300\Omega, C_L = 35\text{ pF}$	1		20		20		
Charge Injection	Q	$C_L = 1,000\text{ pF}$ $V_{gen} = 2.5\text{ V}, R_{gen} = 0\Omega$ See Figure 2	1		-15	15	-15	15	pC
Off Isolation	OIRR	$R_L = 75\Omega, C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	1						dB
Crosstalk (Channel-to-Channel)		Any Other Channel Switches $R_L = 75\Omega, C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	1						
Source-OFF Capacitance	$C_{S(OFF)}$	$f = 1\text{ MHz}$ $V_S = 0\text{ V}$	1						pF
Drain-OFF Capacitance	$C_{D(OFF)}$		1						
Drain and Source ON Capacitance	$C_{S(ON)} + C_{D(ON)}$		1						

ELECTRICAL CHARACTERISTICS <sup>a</sup>							PART 3			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 5 V V <sub>-</sub> = 0 V GND = 0 V V <sub>IN</sub> = 2.0, 0.8 V <sup>e</sup>	LIMITS							
			1=25°C		A SUFFIX		D SUFFIX			
			2=125,85°C		-55 to 125°C		-40 to 85°C			
		3=-55,-40°C		MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 5.5 V V <sub>IN</sub> = 0.0 V or 5.0 V	1,2			3			3	mA
			3			4		4		
Negative Supply Current	I <sub>-</sub>		1		-3		-3			
			2,3		-4		-4			

**NOTES:**

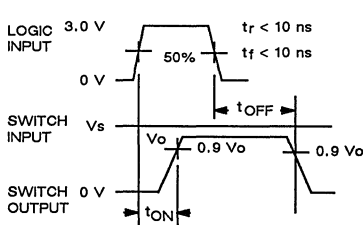
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. V<sub>IN</sub> = input voltage to perform proper function.

**PIN DESCRIPTION**

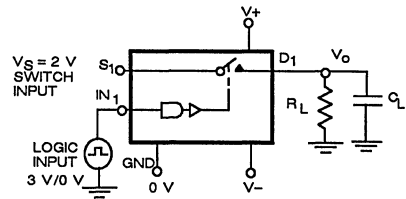
PIN NUMBER	SYMBOL	DESCRIPTION
2, 7, 10, 15	D	An Analog Channel Input or Output
3, 6, 11, 14	S	An Analog Channel Input or Output
1, 8, 9, 16	IN	Logic Control Input
13	V <sub>+</sub>	Positive Supply Voltage
4	V <sub>-</sub>	Negative Supply Voltage
5	GND	Digital Ground

**SWITCHING TIME TEST CIRCUITS**

V<sub>O</sub> is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic Input waveform is inverted for switches that have the opposite logic sense

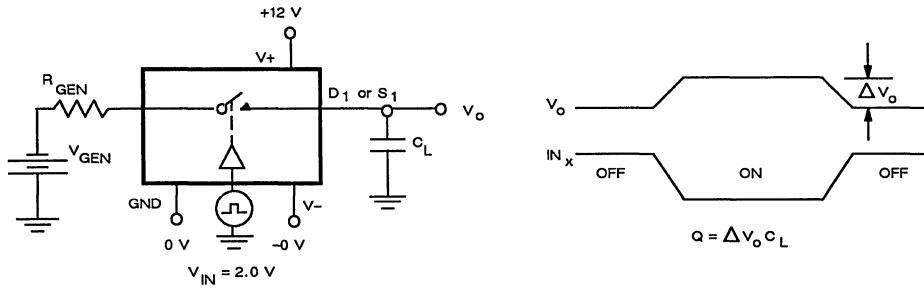


For load conditions, See Electrical Characteristics  
C<sub>L</sub> (Includes fixture and stray capacitance)

$$V_o = V_s \frac{R_L}{R_L + r_{DS(ON)}}$$

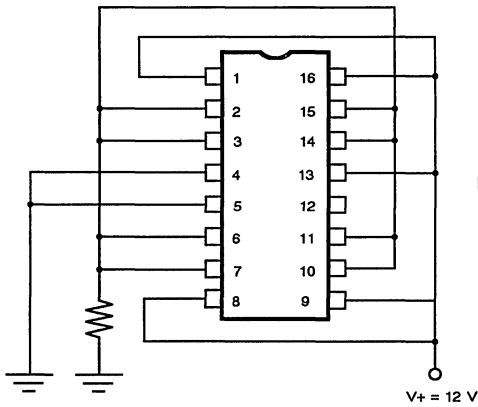
Figure 1

**CHARGE INJECTION TEST CIRCUIT**



**Figure 2**

**BURN-IN CIRCUIT**



Note: All Resistors are 10 kΩ unless otherwise specified.  
SO Package is the same as the DIP.

## 8-Channel/Dual 4-Channel Fault Protected CMOS Analog Multiplexers

### FEATURES

- All Channels OFF When Power OFF, For Analog Signals Up to  $\pm 25$  V
- Any Channel Turns OFF If Input Exceeds Supply Rails
- Fast Switching (300 ns max)
- Break-Before-Make Switching
- TTL And CMOS Compatible

### BENEFITS

- Increased Reliability and Ruggedness
- Power-Down and Overvoltage Protected
- Increased Throughput Rate
- Channels Remain Isolated When A Fault Condition Occurs
- Simplified Logic Interface

### APPLICATIONS

- Avionics
- Data Acquisition Systems
- Industrial Process Control Systems
- High-Rel Control Systems
- Audio Signal Routing

### DESCRIPTION

The DG908 and DG909 are 8-channel and dual 4-channel, respectively, dielectrically isolated CMOS monolithic analog multiplexers. These multiplexers are pin and function compatible with the DG508A/DG509A and similar devices, but add power-down, overvoltage and fault protection features. A series N-P-N MOSFET switch structure ensures that OFF channels will stay OFF even if the inputs exceed the supply rails by up to  $\pm 35$  V. An ON channel will be limited to an output level of about 1.5 V less than the supply rails, thus affording protection to any following circuitry.

Binary 3-bit address and Enable inputs allow selection of any or none of the channels. All logic

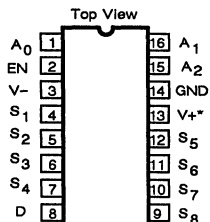
inputs are TTL compatible for easy logic interface; the Enable input also facilitates MUX expansion and cascading.

The DG908 and DG909 are intended for applications where the multiplexer inputs must look directly to the outside world, such as data acquisition system front ends, and other analog multiplexing applications where high device ruggedness is required.

Packaging options include the 16-pin plastic DIP for operation over the industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ) temperature range, and the 16-pin CerDIP for military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) temperature operation.

### PIN CONFIGURATION

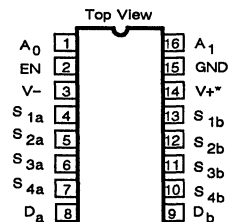
Dual-In-Line Package



Order Numbers:

CerDIP: DG908AK  
Plastic: DG908DJ

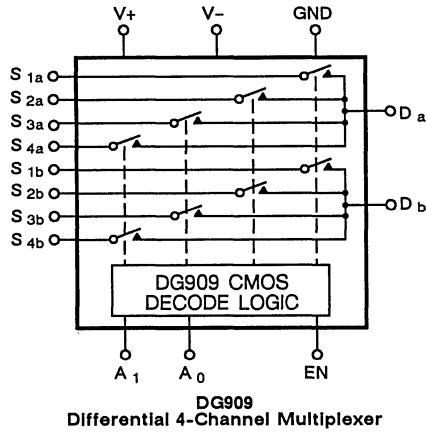
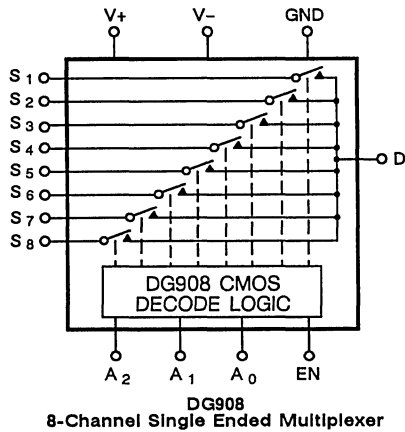
Dual-In-Line Package



Order Numbers:

CerDIP: DG909AK  
Plastic: DG909DJ

**FUNCTIONAL BLOCK DIAGRAM**



**ORDERING INFORMATION**

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG908AK	-55 to 125°C	CerDIP
DG908DJ	-40 to 85°C	PDIP
DG909AK	-55 to 125°C	CerDIP
DG909DJ	-40 to 85°C	PDIP

**5**

**ABSOLUTE MAXIMUM RATINGS**

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

V<sub>EN</sub>, V<sub>A</sub> Digital Input ..... (V-) -4V to (V+) +4 V

V<sub>S</sub>, Analog Input Overvoltage

With Power ON ..... (V-) -20 V to (V+) +20 V

V<sub>S</sub>, Analog Input Overvoltage

With Power OFF ..... -35 V to +35 V

Continuous Current, S or D ..... 20 mA

Peak Current, S or D

(Pulsed at 1 ms, 10% duty cycle max) ..... 40 mA

Operating Temperature (A Suffix) ..... -55 to 125°C

(D Suffix) ..... -40 to 85°C

Storage Temperature (A Suffix) ..... -65 to 150°C

(D Suffix) ..... -65 to 125°C

Power dissipation (package)\*

16-Pin Plastic DIP\*\* ..... 600 mW

16-Pin CerDIP\*\*\* ..... 900 mW

\* All leads soldered or welded to PC board.

\*\* Derate 6.3 mW/°C above 25°C

\*\*\* Derate 12 mW/°C above 75°C.

**CAUTION**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the

operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $\text{GND} = 0\text{ V}$ $V_{AL} = 0.8\text{ V}$ , $V_{AH} = 2.4\text{ V}$	LIMITS						UNIT	
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$		1,2,3			-13	13	-13	13	V
ON Resistance <sup>e</sup>	$r_{DS(ON)}$	$V_D = \pm 10\text{ V}$ , $V_{AL} = 0.8\text{ V}$ $I_D = -100\ \mu\text{A}$	1 2,3				600 900		600 900	$\Omega$
$r_{DS(ON)}$ Match Between Channels <sup>f</sup>	$\Delta r_{DS(ON)}$	$V_S = 0\text{ V}$ , $I_D = -100\ \mu\text{A}$	1	5			10		10	%
Source OFF Leakage Current	$I_{S(OFF)}$	$V_{EN} = 0\text{ V}$	$V_S = \pm 10\text{ V}$ $V_D = \mp 10\text{ V}$	1 2,3	0.02	-0.5 -50	0.5 50	-0.5 -50	0.5 50	nA
Drain OFF Leakage Current	DG908 DG909		$V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$	1 2,3	0.02	-1 -100	1 100	-1 -100	1 100	
			$V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$	1 2,3	0.04	-0.5 -50	0.5 50	-0.5 -50	0.5 50	
Drain ON Leakage Current	DG908 DG909	Sequence Each Switch ON $V_{AL} = 0.8\text{ V}$ , $V_{AH} = 2.4\text{ V}$ $V_S = V_D = \pm 10\text{ V}$	1 2,3	0.1	-2 -100	2 100	-2 -100	2 100		
			1 2,3	0.05	-1 -50	1 50	-1 -50	1 50		
<b>FAULT PROTECTION</b>										
$I_S$ with Power OFF		$V_+ = V_- = V_{EN} = V_D = 0\text{ V}$ $V_A = 0\text{ V}$ , $V_S = \pm 25\text{ V}$	1	1			2		5	$\mu\text{A}$
$I_{S(OFF)}$ with Overvoltage		$V_S = \pm 25\text{ V}$ $V_D = \pm 10\text{ V}$	1	1			2		10	
<b>INPUT</b>										
Input LOW Threshold	$V_{AL}$		1,2,3				0.8		0.8	V
Input HIGH Threshold	$V_{AH}$		1,2,3			2.4		2.4		
Logic Input Current	$I_A$	$V_A = 2.4\text{ V}$ or $0.8\text{ V}$	1 2,3			-1 -30	1 30	-1 -30	1 30	$\mu\text{A}$
<b>DYNAMIC</b>										
Switching Time of Multiplexer	$t_{TRANS}$		1				0.3		0.3	$\mu\text{s}$
Break-Before-Make Interval	$t_{OPEN}$		1			40		40		ns
Enable Turn ON Time	$t_{ON(EN)}$		1				0.6		0.6	$\mu\text{s}$
Enable Turn OFF Time	$t_{OFF(EN)}$		1				0.3		0.3	



ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>AL</sub> = 0.8 V, V <sub>AH</sub> = 2.4 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		D SUFFIX			
			2=125,85°C		-55 to 125°C		-40 to 85°C			
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>										
Settling Time	t <sub>s</sub>	0.1 %		1	1					μs
		0.01%		1	3					
OFF Isolation		V <sub>EN</sub> = 0 V, R <sub>L</sub> = 200Ω, C <sub>L</sub> = 3 pF, V <sub>S</sub> = 3 V <sub>RMS</sub> f = 500 kHz		1	60					dB
Source OFF Capacitance	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V		1	5					pF
Drain OFF Capacitance	DG908	V <sub>EN</sub> = 0 V f = 140 kHz	V <sub>D</sub> = 0 V	1	25					
	DG909			1	12					
Input to Output Capacitance	C <sub>DS(OFF)</sub>			1	0.1					
ON State Input Capacitance	DG908	C <sub>S(ON)</sub>			1	30				
	DG909				1	17				
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	V <sub>EN</sub> = 0 V, V <sub>A</sub> = 0 V		1,2 3			0.4 0.6		0.4 0.6	mA
Negative Supply Current	I <sub>-</sub>			1,2 3		-0.4 -0.6		-0.4 -0.6		

**5**

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Sequence each switch ON.

$$f. \Delta r_{DS(ON)} = \left( \frac{r_{DS(ON) \text{ MAX}} - r_{DS(ON) \text{ MIN}}}{r_{DS(ON) \text{ AVE}}} \right)$$

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**TRUTH TABLES**


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**DG908**

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

**DG909**

A <sub>1</sub>	A <sub>0</sub>	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" =  $V_{AL} \leq 0.8 \text{ V}$ , Logic "1" =  $V_{AH} \geq 2.4 \text{ V}$

## Monolithic 6-Channel Enhancement-type MOSFET Switch

### FEATURES

- Internal Zener Diode Protects the Gate
- Six Switches Per Chip

### BENEFITS

- Reduces External Component Requirements

### APPLICATIONS

- Switching Analog Signals
- Multiplexing
- Designed to Operate with D125, D129 and D139

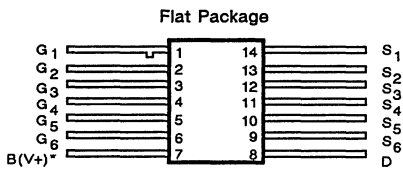
### DESCRIPTION

The G118 contains six enhancement-mode P-channel MOSFETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 20 V

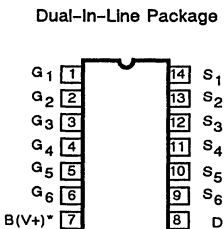
peak-to-peak. The switches are integrated on a common substrate (body). They have a common drain terminal (D) which will function equally well as a common source; likewise, the source terminals will function as drains.

### PIN CONFIGURATION

### FUNCTIONAL BLOCK DIAGRAM

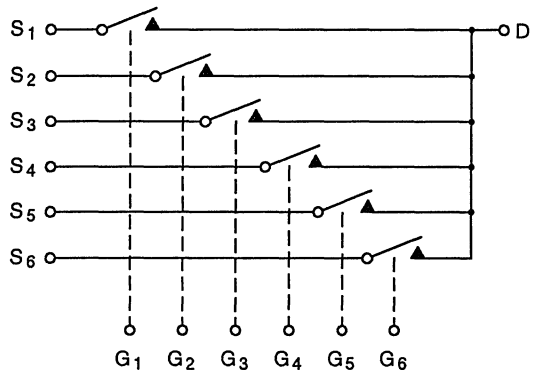


Top View  
Order Number: G118AL



Top View  
Order Numbers: G118AP or G118BP

\* Common to Substrate and Base of Package



## ABSOLUTE MAXIMUM RATINGS

$V_S$ to $V_B$ .....	2 V
$V_B$ to $V_S$ .....	30 V
$V_D$ to $V_B$ .....	2 V
$V_B$ to $V_D$ .....	30 V
$V_D$ to $V_S$ .....	$\pm 30$ V
$V_S$ to $V_D$ .....	$\pm 30$ V
$V_B$ to $V_G$ .....	35 V
$I_S, I_D$ .....	100 mA

$I_G$ .....	5 mA
Storage Temperature .....	-65 to 150°C
Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C

### Power Dissipation\*

Flat Package** .....	750 mW
14-Pin DIP*** .....	825 mW

\* All leads soldered or welded to PC board.

\*\* Derate 10 mW/°C above 75°C.

\*\*\* Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DB} = 0$ V $V_{PB} = 0$ V	LIMITS						UNIT	
			1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>STATIC</b>										
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -1$ mA	$V_{DB} = 0$ V $V_{GD} = -30$ V	1,3 2			100 125		125 150	$\Omega$
			$V_{DB} = -10$ V $V_{GD} = -20$ V	1,3 2			200 250		250 300	
			$V_{DB} = -20$ V $V_{GD} = -10$ V	1,3 2			450 600		500 600	
Source OFF Leakage Current	$I_{S(OFF)}$	$V_{SD} = -20$ V $V_{GD} = 0$ V	1 2		-0.5 -500		-0.5 -500		nA	
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_{DS} = -20$ V, $V_{GD} = 0$ V $V_{SB} = 0$ V	1 2		-3 -3000		-10 -1000			
Gate-Channel Leakage Current	$I_{GSS}$	$V_{GB} = -20$ V	1 2		-0.5 -500		-5 -500			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$I_D = -10$ $\mu$ A, $V_{DG} = 0$ V $V_{SB} = 0$ V	1,2,3		-4	-1.5	-4	-1.5	V	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = -50$ $\mu$ A, $V_{GS} = 0$ V $V_{SB} = 0$ V	1,2,3			-30		-30		
Source-Drain Breakdown Voltage	$V_{(BR)SDS}$	$I_S = -10$ $\mu$ A, $V_{GD} = 0$ V	1,2,3			-30		-30		
Gate-Body Breakdown Voltage	$V_{(BR)GBS}$	$I_G = -10$ $\mu$ A	1,2,3		-90	-35	-90	-35		
<b>DYNAMIC</b>										
Gate-Source Capacitance	$C_{gs}$	$V_{GB} = 0$ V $f = 1$ MHz $V_{DB} = V_{SB} = 0$ Body Guarded	Drain Guarded	1	0.9				pF	
Gate-Drain Capacitance	$C_{gd}$		Source Guarded	1	0.9					
Drain-Source OFF Capacitance	$C_{ds(off)}$		Gate Guarded	1	0.4					

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DB} = 0\text{ V}$ $V_{PB} = 0\text{ V}$	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			2=125, 85°C		-55 to 125°C		-25 to 85°C		
3=-55, -25°C		MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT	
<b>DYNAMIC (Cont'd)</b>									
Source-Body Capacitance	$C_{sb}$	$V_{DB} = 0, V_{SB} = -5\text{ V}$ Drain and Gate Guarded	1	2.0					pF
Drain-Body Capacitance	$C_{db}$	$V_{SB} = 0, V_{DB} = -5\text{ V}$ Gate and Source Guarded	1	12					

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

## Monolithic 6-Channel Enhancement-type MOSFET Switch

### FEATURES

- Integrated MOSFET for Each Gate to Provide "Pull-UP" Current for Gate-Driver Circuit
- Internal Zener Diode Protects the Gate
- Six Switches Per Chip
- Low  $r_{DS(ON)}$  (100  $\Omega$ )

### BENEFITS

- Reduces External Component Requirements

### APPLICATIONS

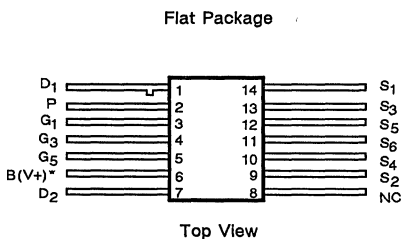
- Differential Input Analog Signal Switching
- Multiplexing
- Designed to Operate with D125, D129 and D139

### DESCRIPTION

The G119 contains six enhancement-mode P-channel MOSFETs designed to function as analog switches. In the ON state each switch will conduct current equally well in either direction, and in the OFF state each switch will block voltages up to 30 V peak-to-peak. The switches are integrated onto a silicon substrate (body) and are internally connected into two groups of three switches per group. This arrangement facilitates the switching or multiplexing of differential analog signals. Each

group has a common drain terminal ( $D_1$  and  $D_2$ ) which will function equally well as a common source. Each gate terminal ( $G$ ) controls a pair of switches and is provided with a normally-OFF "pull-up" MOSFET which may be turned ON to provide a current source to the gate-driving circuit. The pull-ups are turned ON or OFF by connecting the "P" terminal to a negative supply or to the "B" terminal respectively.

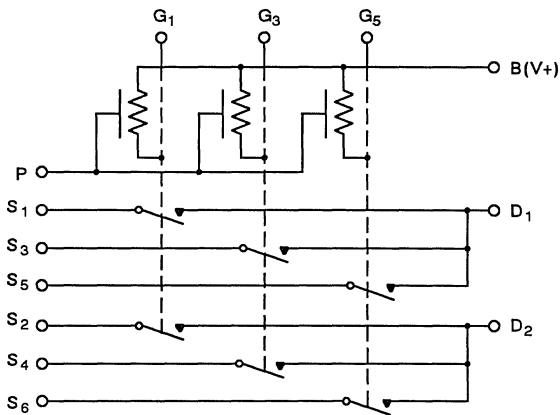
### PIN CONFIGURATION



Order Numbers:  
G119AL or G119BL

\* Common to Substrate and Base of Package

### FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

$V_B$ to $V_S$ .....	-2 to 30 V
$V_B$ to $V_D$ .....	-2 to 30 V
$V_D$ to $V_S$ .....	$\pm$ 30 V
$V_B$ to $V_G$ , $V_B$ to $V_P$ .....	35 V
$I_S$ , $I_D$ .....	100 mA
$I_G$ .....	5 mA

$I_P$ .....	100 $\mu$ A
Storage Temperature .....	-65 to 150°C
Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C
Power Dissipation* .....	750 mW

\* All leads soldered or welded to PC board.  
Derate 10 mW/°C above 75°C.

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DB} = 0$ V $V_{PB} = 0$ V	LIMITS						UNIT			
			1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C					
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>				
<b>STATIC</b>												
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -1$ mA	$V_{DB} = 0$ V $V_{GD} = -30$ V	1,3 2			100 125		125 150	$\Omega$		
			$V_{DB} = -10$ V $V_{GD} = -20$ V	1,3 2			200 250		250 300			
			$V_{DB} = -20$ V $V_{GD} = -10$ V	1,3 2			450 600		500 600			
Source OFF Leakage Current	$I_{S(OFF)}$	$V_{SD} = -20$ V $V_{GD} = 0$ V	1 2		-0.5 -500			-5 -500				
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_{DS} = -20$ V, $V_{GD} = 0$ V $V_{SB} = 0$ V	1 2		-1.5 -1500			-10 -1000	nA			
Gate ON Currents	$I_{G(ON)}$	$V_{GB} = -30$ V $V_{PB} = -30$ V	1		-2.4	-0.8		-2.4	-0.8	mA		
Gate-Channel Leakage Current	$I_{GSS}$	$V_{GB} = -20$ V	1 2		-0.5 -500			-5 -500		nA		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$I_D = -10$ $\mu$ A, $V_{DG} = 0$ V $V_{SB} = 0$ V	1,2,3		-4	-1.5		-4	-1.5	V		
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$I_D = -50$ $\mu$ A, $V_{GS} = 0$ V $V_{SB} = 0$ V	1,2,3					-30	-30			
Source-Drain Breakdown Voltage	$V_{(BR)SDS}$	$I_S = -10$ $\mu$ A, $V_{GD} = 0$ V	1,2,3					-30	-30			
Gate-Body Breakdown Voltage	$V_{(BR)GBS}$	$I_G = -10$ $\mu$ A	1,2,3					-90	-35		-90	-35
Pull-Up Gate-Body Breakdown Voltage	$V_{(BR)PBS}$	$I_P = -10$ $\mu$ A $V_{GB} = 0$ V	1,2,3					-90	-35		-90	-35

5

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DB} = 0\text{ V}$ $V_{PB} = 0\text{ V}$	LIMITS						UNIT	
			1=25°C		A SUFFIX		B SUFFIX			
			2=125, 85°C		-55 to 125°C		-25 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
DYNAMIC <sup>e</sup>										
Gate-Source Capacitance	$C_{gs}$	$V_{GB} = 0\text{ V}$ $f = 1\text{ MHz}$ $V_{DB} = V_{SB} = 0$ Body Guarded	Drain Guarded	1	1.8					pF
Gate-Drain Capacitance	$C_{gd}$		Source Guarded	1	1.8					
Drain-Source OFF Capacitance	$C_{ds(off)}$		Gate Guarded	1	0.4					
Source-Body Capacitance	$C_{sb}$	$V_{DB} = 0, V_{SB} = -5\text{ V}$ Drain and Gate Guarded	1	2.0						
Drain-Body Capacitance	$C_{db}$	$V_{SB} = 0, V_{DB} = -5\text{ V}$ Gate and Source Guarded	1	6.0						

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
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- e.  $V_{GB} = 0\text{ V}$ ,  $f = 1\text{ MHz}$ .



# Si3002

## Monolithic SPDT MOS Switch with Driver

### FEATURES

- Internal Gate Protection Zener Diodes
- TTL and Compatible Input

### BENEFITS

- Reduces External Component Requirements
- Easily Interfaced

### APPLICATIONS

- Switching Analog Signals

### DESCRIPTION

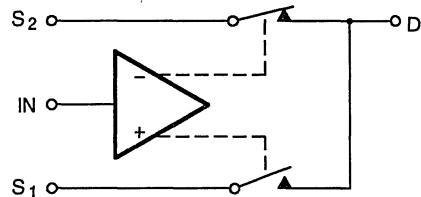
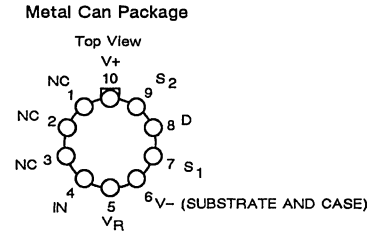
The Si3002 contains two P-channel MOS field-effect transistors designed to function as single-pole double-throw analog switches. A level-shifting driver enables a low-level input (0.8 to 2 V) to control the ON-OFF state of the switches. In the ON state, each switch will conduct current equally well in either direction. In the OFF state the switches will block voltages up to 20 V peak-to-peak. With logic

"0" at the driver input, a common drain (D) is connected through an ON switch to source ( $S_1$ ). With logic "1" at the input, "D" is connected to  $S_2$ . Switch action is make-before-break.

The Si3002 is available in 10-pin metal can and 14-pin side braze DIP for operation over the military, A suffix (-55 to 125°C) and the industrial, B suffix (-25 to 85°C) temperature ranges.

### PIN CONFIGURATION

### FUNCTIONAL BLOCK DIAGRAM

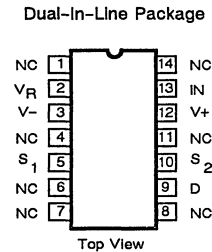


One SPDT Switch per Package\*

Truth Table

LOGIC	SW1	SW2
0	ON	OFF
1	OFF	ON

\*Switches Shown for Logic "1" Input



Order Numbers: SI3002AP, SI3002BP

## ABSOLUTE MAXIMUM RATINGS

$V_+$ to $V_-$ .....	36 V	Storage Temperature .....	-65 to 150°C
$V_+$ to $V_S$ or $V_D$ .....	25 V	Operating Temperature (A Suffix) .....	-55 to 125°C
$V_+$ to $V_R$ or $V_{IN}$ .....	12 V	(B Suffix) .....	-25 to 85°C
$V_D$ to $V_-$ .....	36 V	Power Dissipation (Package)*	
$V_S$ to $V_-$ .....	36 V	Metal Can** .....	450 mW
$V_D$ to $V_S$ .....	$\pm 25$ V	14-Pin DIP*** .....	825 mW
$V_{IN}$ to $V_R$ .....	6 V	* Device mounted with all leads soldered or welded to PC board.	
CURRENT, (Any Terminal) .....	30 mA	** Derate 6 mW/°C above 75°C.	
		*** Derate 11 mW/°C above 75°C.	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 10$ V $V_- = -20$ V $V_R = 0$ V	LIMITS						UNIT
			1=25°C		A SUFFIX		B SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$		1,2,3		-10	10	-10	10	V
Drain-Source ON Resistance	$r_{DS(ON)}$	$V_D = 10$ V	$I_S = -1$ mA $V_{INL} = 0.8$ V $V_{INH} = 2.0$ V	1,3		100		100	$\Omega$
		$V_D = 0$ V		2		150		150	
		$V_D = -10$ V		2		400		400	
Source OFF Leakage Current	$I_{S(OFF)}$	$V_S = -10$ V $V_D = 10$ V	$V_{INL} = 0.8$ V $V_{INH} = 2.0$ V	1		-1		-5	nA
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$	$V_D = -10$ V $I_S = 0$		2,3		-1000		-100	
				1		-2		-10	
				2,3		-2000		-200	
<b>INPUT</b>									
Input Current (Voltage LOW)	$I_{INL}$	$V_{IN} = 0$ (SW <sub>1</sub> ON)	1		-0.8		-0.8		mA
			2		-0.6		-0.8		
					-1.0		-1.0		
Input Current (Voltage HIGH)	$I_{INH}$	$V_{IN} = 0$ (SW <sub>2</sub> ON)	1,3			0.1		0.1	$\mu$ A
			2			10		10	
<b>DYNAMIC</b>									
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit	1			1		1	$\mu$ s
Turn-OFF Time	$t_{OFF}$		1			1.5		1.5	
Source OFF Capacitance	$C_{S(OFF)}$	$V_S = 0$ , $f = 1$ MHz	1	6					pF

**ELECTRICAL CHARACTERISTICS <sup>a</sup> (Cont'd)**

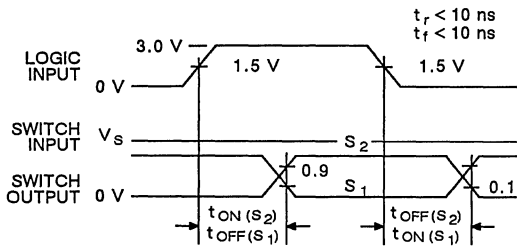
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 10\text{ V}$ $V_- = -20\text{ V}$ $V_R = 0\text{ V}$	LIMITS						UNIT
			1=25°C		A SUFFIX 2=125,85°C 3=-55,-40°C		B SUFFIX -25 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
Positive Supply Current	$I_+$	$V_{IN} = 0\text{ V}$	1			3.0		3.5	mA
Negative Supply Current	$I_-$		1		-3.0		-3.0		
Reference Supply Current	$I_{REF}$		1		-0.1		-0.1		
Positive Supply Current	$I_+$	$V_{IN} = 5\text{ V}$	1			3.0		3.5	
Negative Supply Current	$I_-$		1		-3.0		-3.0		
Reference Supply Current	$I_{REF}$		1		-1.5		-1.5		

**NOTES:**

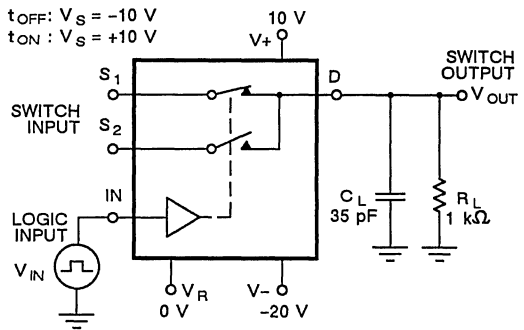
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**SWITCHING TIME TEST CIRCUIT**

Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch on.



Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



$$V_{OUT} = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$





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# DATA CONVERSION

## INTRODUCTION

Siliconix manufactures a variety of data conversion devices, including 12-bit digital-to-analog converters (DACs, or D/As), 8-bit data acquisition systems (DASs), high resolution integrating analog-to-digital converters (ADCs, or A/Ds), and a high speed 12-bit successive approximation register (SAR). This section of the data book includes the complete spectrum of Siliconix data conversion components.

### Digital-to-Analog Converters

Siliconix offers the industry-standard Si75XX family of 10- and 12-bit CMOS multiplying DACs, including the Si7533, Si7240, Si7541, Si7541A, Si7542, Si7543 and Si7545 devices. This family is based on the Siliconix proprietary PolyMOS™ process, utilizing highly stable thin-film resistors which are laser-trimmed for excellent accuracy. Each of these devices features improved dynamic performance over the industry-standard products in this family, having been designed for reduced glitch impulse, reduced propagation delay, and improved settling time.

### Data Acquisition Systems and Analog-to-Digital Converters

The Siliconix proprietary Si860X family are 8-bit data acquisition systems with 25 microsecond conversion times. The Si8601 is an 8-bit 8-channel system intended for 5 V single-supply operation, with a 5 Volt analog range. The Si8602 is the 15 V version of the Si8601, intended for military applications and other systems that need a 10 Volt signal range. The Si8603 and Si8604 are low-cost single-channel versions of the Si8601 and Si8602 respectively. Each of these data acquisition systems and A/Ds contain on-board sample and hold functions and microprocessor interfaces to simplify design and reduce board space and component count.

The Si2504 is a high-speed, low-power successive approximation register which is used as a building block in custom and hybrid high-performance 12-bit A/D converters. It features improved clock rate (to 40 MHz, compared with the 25 MHz industry-standard), and reduced supply current (10 mA, compared to the industry-standard 100 mA) to allow faster and more efficient custom A/D converter design.

### High Resolution A/D Converter Systems

Siliconix pioneered the development of monolithic A/D converters for display applications in the early 1970's with the LD110/111 quantized feedback 3 1/2-digit A/D converter chip set. Today, Siliconix offers improved resolution and accuracy in display converters up to the 4 1/2-digit (approximately 15 bit) level, with the LD120/121A, LD122/121A chip sets and the single-chip Si7135. The Si7135 is the premium monolithic 4 1/2-digit converter available, offering improved linearity and reduced rollover error compared to the generic 7135 converter.

## GLOSSARY OF TERMS

### Accuracy

May be specified in absolute and/or relative terms. Absolute accuracy is interpreted as a measure of the total error of the converter, and is expressed in terms of the difference between the actual analog output and the output expected for a given input digital code. Relative accuracy, on the other hand, is more an interpretation of the non-linearity of the converter and is specified in terms of the difference between the actual analog output and the output expected (based on the relative, or actual full scale output of the converter) for a given input code.

Absolute accuracy measurements should be made under a set of standard conditions, with the signal sources and measuring equipment traceable to some acceptable standard. The error is specified in LSB or percent of full scale range.

### Compliance Voltage

For a current output D/A converter, this is the maximum voltage range on the output terminal over which the current output of a DAC can vary for the DAC to meet an absolute accuracy as specified (usually  $\pm 1/2$  LSB).

### Differential Linearity (DNL)

The measured difference in output between any two adjacent digital codes should be exactly 1 LSB (or F.S.  $\times 2^{-n}$  for an n-bit converter.) Any deviation from the ideal difference is called differential non-linearity, and is expressed in submultiples of an LSB. Differential linearity errors greater than 1 LSB can result in non-monotonic performance in a D/A converter, and missing codes in an A/D converter.

### Feedthrough

An AC specification for a multiplying DAC which defines the frequency at which a specified peak-to-peak AC signal is seen at the DAC output with all bits in the OFF state. It is usually specified as %, ppm, or fractions of an LSB for a given set of input conditions.

### Four Quadrant

For a multiplying D/A converter, "four quadrant" means that both the reference signal and the number

represented by the digital input signal may be of either polarity. The converter is expected to obey the rules of multiplication for algebraic sign.

### Gain

The gain of the converter is the analog scale factor that describes the nominal conversion relationship between the converter's full scale output and its analog (or reference) input. The gain is generally adjustable by the user (externally) to full scale  $\times (1-2^{-n})$  with all bits ON. For bipolar operation adjust output to F.S.  $[1-2^{-(n-1)}]$  with all bits ON.

### Least Significant Bit (LSB)

In a binary numerical system, the LSB is the bit that represents the least, or smallest, value. For example, in the natural binary number 1101 (decimal 13, or  $2^3 + 2^2 + 0^1 + 2^0$ ), the right-most digit is the LSB. It thus represents the smallest analog change that can be resolved in an n-bit converter and is equal to the full scale output range divided by  $2^n$  where n = number of bits,  $LSB = FS/2^n$ .

### Linearity

Linearity error of a converter, which implies the integral linearity error, is the deviation of the analog output from an ideal straight line, and is usually specified in % or ppm of the Full Scale range or submultiples of 1 LSB. The straight line can be either a "best straight line", or "end point". The former is derived empirically by manipulating the offset and/or gain of the converter to minimize the deviations of the actual analog output from the manipulated best line. The latter assumes the idealized line passes through the "end points" of the converter after it has been calibrated (zero and full scale).

### Monotonicity

A D/A converter is said to be monotonic if the output either increases or remains constant with increasing digital input codes. The statement monotonic (over temperature) is sometimes substituted for a differential non-linearity specification as a DNL specification of 1 LSB is not a sufficient condition for monotonic behavior.



## Most-Significant Bit (MSB)

In a binary numerical system, the MSB is the bit that represents the largest value, or weight. For example, in the natural binary number 1101 (decimal 13, or  $2^3 + 2^2 + 0^1 + 2^0$ ), the leftmost digit (or "1") is the MSB. Its analog weight, relative to full scale, is FS/2. In bipolar applications the MSB also indicates the polarity of the number represented by the rest of the bits.

## Offset (Zero Scale Error)

The measured analog output when the digital input code corresponds to an analog value of zero. Generally expressed as a percentage of Full Scale range but is also expressed in ppm, LSB's or in units of current or voltage.

## Resolution

The number of states ( $2^n$ ) that the Full Scale range may be divided into or resolved, where  $n$  = number of bits. This is usually expressed as a number of bits ( $n$ ).

## Settling Time

The elapsed time for the analog output to reach its final value within a specified error band after the corresponding digital input code has been changed. It is usually specified as a Full Scale range change and measured from the 50% point of the digital input code change to the time the output reaches the final value within the specified error band.

## Stability

The stability of a converter is usually related to changes in its characteristics as a function of temperature and time. While such measurements are difficult and time consuming, those related to temperature are often sufficiently critical to warrant their inclusion in the characteristic data. (See also Temperature Coefficient.)

## Switching Time (Propagation Delay)

In a D/A converter the switching time is the time it takes for the logic and switches to change from one state (ON or OFF) to the other. It includes delay and rise time, but does not include settling time, and is measured from the 50% point of the logic input to the 50% point of the changing analog output signal.

## Temperature Coefficient

In general, temperature coefficients are expressed as fractions of an LSB/°C and then over the rated temperature range. The temperature coefficient (or T.C.) can then be defined as the change in the parameter divided by the corresponding temperature change, and is usually specified for gain, offset and linearity parameters.

## Zero and Gain-Adjustment Principles

For unipolar applications first adjust the D/A converter for zero output with all bits OFF. Then with all bits ON, adjust the output for full scale – 1 LSB.

For bipolar applications, in offset binary, adjust the D/A converter's "zero" for negative full scale with all bits OFF. Then with all bits ON set the gain for full scale – 2 LSB.

## 3 1/2-Digit A/D Converter Set

### FEATURES

- Buffered Reference Input
- MOSFET Input
- Auto-Zero System
- Auto-Polarity
- Over and Under Range Signals

### BENEFITS

- High Gain Stability
- Reduced Signal Loading
- Reduced Offset and Drift Over Temperature
- Reduced External Parts Count
- Easily Interfaced

### APPLICATIONS

- High Performance Digital Voltmeters
- Digital Panel Meters
- Digital Instrumentation Readouts
- $\mu$ P A/D Interface Subsystem
- Auto-Zeroed Microvolt or Strain Gauge Systems

### DESCRIPTION

The LD110 and LD111A form a precision 3 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation. Except for a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

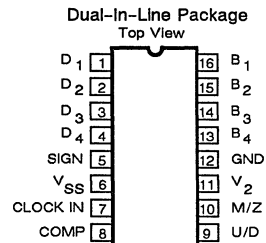
The monolithic LD111A high performance analog processor contains a bipolar comparator, a bipolar integrating amplifier, a bipolar reference amplifier, two MOSFET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. The high impedance input and reference buffer amplifiers eliminate source loading errors and provide the outstanding temperature coefficient inherent in this system. Break-before-make switch action ensures that neither the analog input nor the reference voltages will be shorted to ground at any time.

The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing

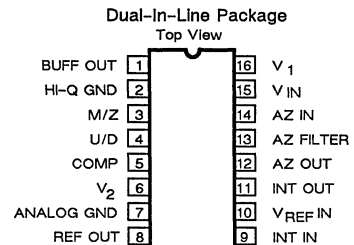
function of the analog processor. Seventeen static latches store the 3 1/2 digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2, and 4.

Both devices are supplied in the 16-pin plastic DIP, and are specified for operation over the commercial, C suffix (0 to 70°C) temperature range.

### PIN CONFIGURATION

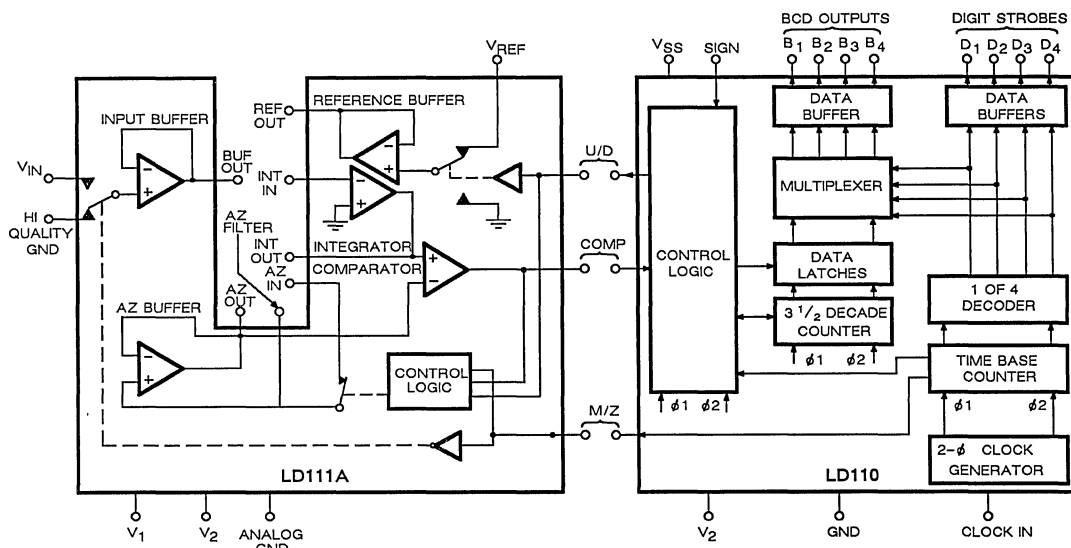


Order Number: LD110CJ



Order Number: LD111ACJ

## FUNCTIONAL BLOCK DIAGRAM



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS

### ABSOLUTE MAXIMUM RATINGS

$I_{IN}$ (Pin 15, 2) .....	$\pm 1$ mA
$V_1 - V_2$ (LD111A) .....	30 V
$V_{SS}$ .....	6 V
$V_{SS} - V_2$ (LD110) .....	20 V
V On Any Pin Relative to $V_{SS}$ (LD110) .....	0.3 V to -20 V

$V_{REF}$ .....	$V_1$
Operating Temperature .....	0 to 70°C
Storage Temperature .....	-65 to 125°C
Power Dissipation (Package) * .....	750 mW

\* Device mounted with all leads welded or soldered to PC Board. Derate 6.3 mW/°C above 25°C.

**6**

ELECTRICAL CHARACTERISTICS <sup>a</sup>						
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_1 = 12$ V, $V_2 = -12$ V $V_{SS} = 5$ V $V_{REF} = 8.2$ V $R_1 = 100$ k $\Omega$	LIMITS: $T_A = 25^\circ\text{C}$			UNIT
			TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SYSTEM</b>						
Analog Input Range	$V_{ANALOG}$		-2	2		V
Linearity			0.02			% rdg
Noise		Noise apparent when going from one steady reading to another.	0.1			LSB <sub>p-p</sub>

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>1</sub> = 12 V, V <sub>2</sub> = -12 V V <sub>SS</sub> = 5 V V <sub>REF</sub> = 8.2 V R <sub>1</sub> = 100 kΩ	LIMITS: T <sub>A</sub> = 25 °C			UNIT	
			TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SYSTEM (Cont'd)</b>							
Gain T.C.			5			ppm/°C	
Normal Mode Rejection	NMR	f <sub>NOISE</sub> = 60 Hz	40			dB	
Clock Frequency	f <sub>in</sub>	50 % Duty Cycle	30.7	2	250	kHz	
ON Resistance Auto Zero Switch	r <sub>DS(ON)</sub>	V <sub>AZ(IN)</sub> = -4.0 V I <sub>S</sub> = -30 μA	6		20	kΩ	
<b>INPUT</b>							
Clock Input Current LOW	I <sub>CL</sub>	V <sub>CLOCK(IN)</sub> = 0.4 V		-500		μA	
Input Bias Current	I <sub>IN</sub>		4			pA	
COMP, LD110	I <sub>INL</sub>	V <sub>IN</sub> = -12 V	-700	-1500	-50	μA	
<b>AMPLIFIER</b>							
Reference Buffer	I <sub>SOURCE</sub>	V <sub>OUT</sub> = 0 V	V <sub>IN(L/U/D)</sub> = 0.8 V	-800		-400	μA
AZ Buffer	I <sub>SINK</sub>		V <sub>AZ</sub> = -4 V	800			
Input Buffer	I <sub>SINK</sub>		V <sub>IN</sub> = -2 V	800	400		
	I <sub>SOURCE</sub>		V <sub>IN</sub> = 2 V	-100		-50	
AZ Buffer	V <sub>OS</sub>				-100	100	mV
<b>OUTPUT</b>							
Measure/Zero Voltage, Low	V <sub>OL1</sub>	I <sub>OL</sub> = 150 μA			0.6	V	
Measure/Zero Voltage, High	V <sub>OH1</sub>	I <sub>OH</sub> = -200 μA		2.4			
Up/Down Logic Voltage, Low	V <sub>OL2</sub>	I <sub>OL</sub> = 250 μA			0.6		
Up/Down Logic Voltage, High	V <sub>OH2</sub>	I <sub>OH</sub> = -200 μA		2.4			
Analog Comparator Voltage	V <sub>OH3</sub>	I <sub>OH</sub> = -100 μA		2.4			

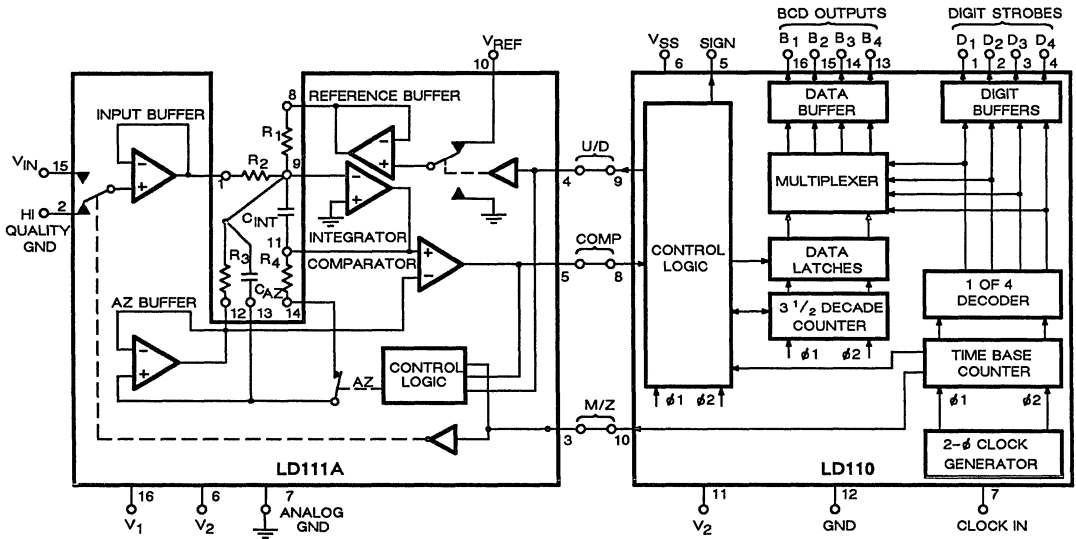
ELECTRICAL CHARACTERISTICS <sup>a</sup>						
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>1</sub> = 12 V, V <sub>2</sub> = -12 V V <sub>SS</sub> = 5 V V <sub>REF</sub> = 8.2 V R <sub>1</sub> = 100 kΩ	LIMITS: T <sub>A</sub> = 25 °C			UNIT
			TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>OUTPUT (Cont'd)</b>						
DigIts, Bits Voltage, Low	V <sub>OL3</sub>	I <sub>OL</sub> = 1.6 mA			0.6	V
Sign Voltage, Low	V <sub>OL4</sub>				0.65	
Data Bits Voltage, High	V <sub>OH4</sub>	I <sub>OH</sub> = -200 μA		2.4		
DigIts, Sign Voltage, High	V <sub>OH5</sub>	I <sub>OH</sub> = -800 μA		2.4		
<b>SUPPLY</b>						
V <sub>1</sub> Supply Current LD111A	I <sub>1</sub>		2.2		4	mA
V <sub>2</sub> Supply Current LD111A	I <sub>2A</sub>		-1.8	-4		
V <sub>2</sub> Supply Current LD110	I <sub>2D</sub>		-17	-23		
V <sub>SS</sub> Supply Current LD110	I <sub>SS</sub>		17.4		24	
Power Supply Rejection Ratio, V <sub>1</sub>	PSRR <sub>1</sub>		85	80		dB
Power Supply Rejection Ratio, V <sub>2</sub>	PSRR <sub>2</sub>		65	60		
Reference Voltage Rejection		R <sub>REF</sub> = R <sub>2</sub> = 100 kΩ V <sub>IN</sub> = 2 V	1			% Δ rdg per Δ V <sub>REF</sub>

**NOTES:**

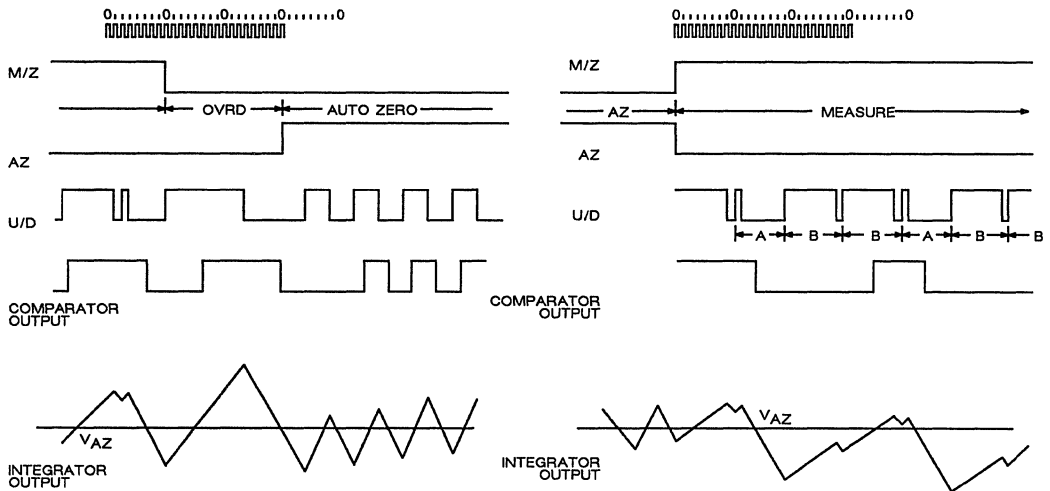
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

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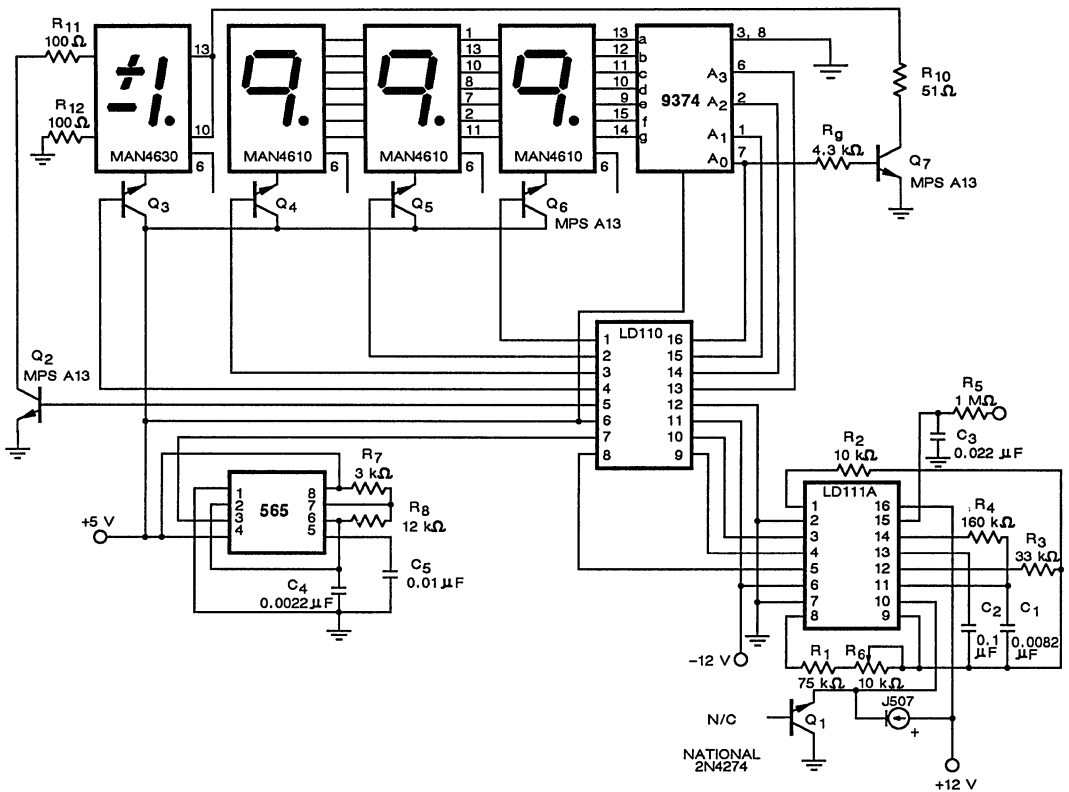
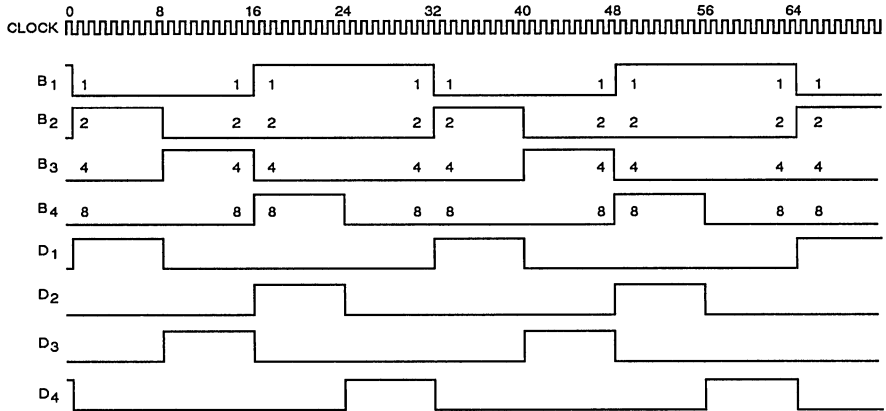
## FUNCTIONAL OPERATION



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS



**FUNCTIONAL OPERATION (Cont'd)**



**6**

# LD120/121A

## 4 1/2-Digit A/D Converter Set

### FEATURES

- 0.005%  $\pm 1$  Count Accuracy
- $\pm 200.0$  mV and  $\pm 2.000$  V Ranges
- Auto-zero
- Auto-polarity
- Over and Under Range Outputs

### BENEFITS

- High System Performance
- Single Resistor Programming
- Nulls Out Offsets
- Single Reference
- Easily Interfaced

### APPLICATIONS

- High Accuracy Digital Voltmeters and Panel Meters
- Digital Scales and Thermometers
- $\mu$ P Data Acquisition Systems
- Scientific Instrumentation

### DESCRIPTION

The LD120 and LD121A form a precision 4 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation. Except for a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

The LD120 analog processor is fabricated with a unique PMOS/Bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered in the LD120 to

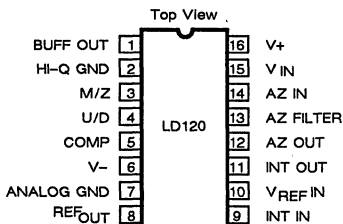
eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD120 directly interfaces to the LD121A digital processor with no additional active components required.

The LD121A synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4-1/2 digits of multiplexed BCD data. (All outputs are TTL compatible.) Overage is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

Both devices are supplied in space saving 300 mil dual-in-line plastic packages for operation in the commercial, C suffix (0 to 70°C) temperature range.

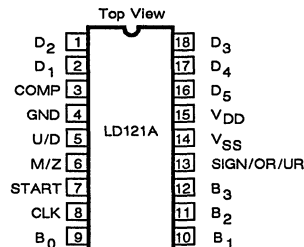
### PIN CONFIGURATION

Dual-In-Line Package



Order Number: LD120CJ

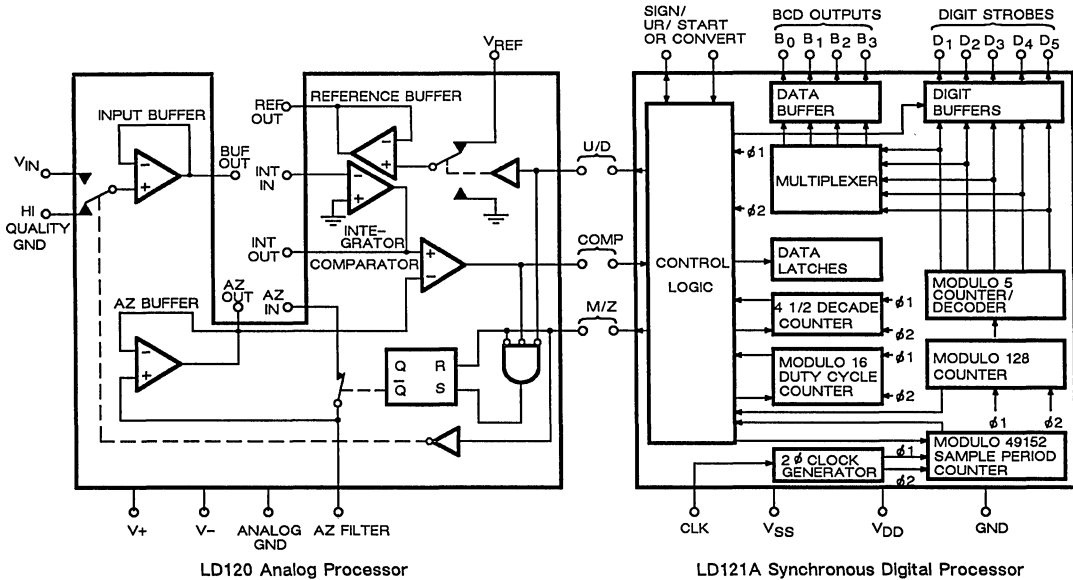
Dual-In-Line Package



Order Number: LD121ACJ



**FUNCTIONAL BLOCK DIAGRAM**



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

**ABSOLUTE MAXIMUM RATINGS**

$V_{IN}$ (Pin 15, 2 LD120) .....	$V_- < V_{IN} < V_+$
$I_{INPUT}$ (LD120) .....	$\pm 1$ mA
$V_+ - V_-$ (LD120) .....	32 V
$V_{SS} - V_{DD}$ (LD121A) .....	20 V
Any Pin (LD121A) .....	$V_{DD}$ to $V_{SS} \pm 0.3$ V

$V_{REF}$ .....	$V_+$
Operating Temperature .....	0 to 70°C
Storage Temperature .....	-65 to 125°C
Power Dissipation (Package)* .....	750 mW

\* Device mounted with all leads welded or soldered to PC Board. Derated 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = V_{DD} = -12\text{ V}$ $V_{SS} = 5\text{ V}$	LIMITS				UNIT		
			1=25°C		C SUFFIX				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>SYSTEM <sup>⊕</sup></b>									
Linearity		$f_{\text{CLOCK}} = 163.84\text{ kHz}$ $V_{\text{REF}} = 6.8\text{ V}$	2 V Scale	1	$\pm 1/4$	-1	1	Count	
			200 mV Scale	1	$\pm 1/2$	-2	2		
Noise <sup>f</sup>			2 V Scale	1	$1/3$		1		
			200 mV Scale	1	$1/2$		2		
Normal Mode Rejection Ratio	NMRR			$f_L = 50\text{ Hz}$ or 60 Hz	1	40			dB
Power Supply Rejection Ratio	PSRR				1	80			
Gain T.C.					1	5		15	ppm/°C
Zero Drift				$C_{\text{STRG}} = 1\text{ }\mu\text{F}$ $R_{\text{IN}} \leq 100\text{ k}\Omega$	1	1		5	Count

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
LD120 (LINEAR CIRCUIT)								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 12\text{ V}$ $V_- = V_{DD} = -12\text{ V}$ $V_{SS} = 5\text{ V}$	LIMITS				UNIT	
			1=25°C		C SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUT BUFFER</b>								
Analog Input Voltage	$V_{\text{ANALOG}}$			1		-5	5	V
Output Source Current	$I_{\text{SOURCE}}$	$V_{\text{IN}} = 2\text{ V}$ , Buff Out = 0 V		1	-100		-50	$\mu\text{A}$
Output Sink Current	$I_{\text{SINK}}$	$V_{\text{IN}} = -2\text{ V}$ , Buff Out = 0 V		1	800	400		
Input Current	$I_{\text{IN}}$	$V_{\text{IN}} = \pm 2.8\text{ V}$		1	2			pA
Common-Mode Rejection Ratio	CMRR			1	-72			dB
Input Current/ Input Voltage HIGH	$I_{\text{IH}}$	M/Z, U/D Inputs	$V_{\text{IN}} = 2.0\text{ V}$	1			20	$\mu\text{A}$
Input Current/ Input Voltage LOW	$I_{\text{IL}}$		$V_{\text{IN}} = 0.8\text{ V}$	1		-100		

ELECTRICAL CHARACTERISTICS <sup>a</sup>			LD120 (LINEAR CIRCUIT) (Cont'd)				
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = V <sub>DD</sub> = -12 V V <sub>SS</sub> = 5 V	LIMITS				UNIT
			1=25°C		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>AZ BUFFER</b>							
Output Source Current	I <sub>SOURCE</sub>		1	-100			μA
Output Sink Current	I <sub>SINK</sub>		1	800			
Offset Voltage	V <sub>OS</sub>	V <sub>OUT</sub> = 0 V	1		-50	50	mV
On Resistance <sup>g</sup>	r <sub>DS(ON)</sub>	V <sub>STRG</sub> = -4 V I <sub>DS</sub> = 30 μA	1	6		20	kΩ
<b>REFERENCE BUFFER</b>							
Reference Buffer Source Current	I <sub>SOURCE</sub>	V <sub>IN</sub> (U/D IN) = 0.8 V V <sub>O</sub> = 0 V	1	-800		-400	μA
Reference Buffer Sink Current	I <sub>SINK</sub>	V <sub>IN</sub> (U/D IN) = 2.0 V V <sub>O</sub> = 2 V	1	100			
<b>INTEGRATOR</b>							
Integrator Source Current <sup>h</sup>	I <sub>SOURCE</sub>	V <sub>IN</sub> (INT. IN) = -100 mV V <sub>O</sub> = 0 V	1	-100		-50	μA
Integrator Sink Current <sup>h</sup>	I <sub>SINK</sub>	V <sub>IN</sub> (INT. IN) = 100 mV V <sub>O</sub> = 0 V	1	800	400		
Output Swing			1		-10	10	V
<b>COMPARATOR</b>							
Comparator Output Swing	V <sub>OUT</sub>	R <sub>L</sub> = 10 k to 5 V AZ Filter IN = 100 mV Integrator OUT = 0 V	1		-5		V
Comparator Offset Voltage	V <sub>OS</sub>		1		-5	5	mV
<b>SUPPLY</b>							
Positive Supply Voltage	V <sub>+</sub>		1	12	9	15	V
Negative Supply Voltage	V <sub>-</sub>		1	-12	-15	-9	
Positive Supply Current	I <sub>+</sub>		1			3.5	mA
Negative Supply Current	I <sub>-</sub>		1		-3.5		

ELECTRICAL CHARACTERISTICS <sup>a</sup>				LD121 (DIGITAL CIRCUIT)			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = V <sub>DD</sub> = -12 V V <sub>SS</sub> = 5 V	LIMITS				UNIT
			1=25°C		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUTS</b>							
Input Voltage HIGH	V <sub>INH</sub>	Comparator Input, Sign/UR/OR/Blink <sup>1</sup> Start, CLK IN	1		4		V
Input Voltage LOW	V <sub>INL</sub>		1			0.5	
Input Current/ Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V (Sign/OR/UR <sup>1</sup> )	1	170		300	μA
Input Current/ Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V (Start Convert, Clock)	1	-150	-400		
<b>OUTPUTS</b>							
Output Voltage HIGH	V <sub>OH</sub>	Bit Lines Sign/OR/UR Digital Strobes	I <sub>OH</sub> = -40 μA	1		2.4	V
Output Voltage LOW	V <sub>OL</sub>		I <sub>OL</sub> = 1.6 mA	1			
Output Voltage HIGH	V <sub>OH</sub>	M/Z	I <sub>OH</sub> = -150 μA	1		4	V
Output Voltage LOW	V <sub>OL</sub>		I <sub>OL</sub> = 0.8 mA	1			
Output Voltage HIGH	V <sub>OH</sub>	U/D	I <sub>OH</sub> = -0.5 μA			4	V
Output Voltage LOW	V <sub>OL</sub>		I <sub>OL</sub> = 0.8 mA				
<b>DYNAMIC</b>							
Start Convert <sup>1</sup>	t <sub>p</sub>		1		20		μs
Clock Frequency	f <sub>CLOCK</sub>	50% Duty Cycle	1		50	250	kHz
Rep. Rate (Strobes)		f <sub>CLOCK</sub> ÷ 640	1		78	470	Hz
<b>SUPPLY</b>							
Positive Supply Voltage	V <sub>SS</sub>	Range Over Which Functionality Is Guaranteed	1	5	4.5	5.5	V
Negative Supply Voltage	V <sub>DD</sub>		1	-12	-13.2	-10.8	
Positive Supply Current <sup>k</sup>	I <sub>SS</sub>		1	14		25	mA
Negative Supply Current	I <sub>DD</sub>		1	-14	-25		

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## ELECTRICAL CHARACTERISTICS <sup>a</sup>

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### NOTES:

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. System parameters not directly tested.
- f. Bit width over which reading is stable 95% of the time.
- g.  $V_{STRG}$  must be more positive than  $-4$  V.
- h. Reference source impedance must be less than  $10\text{ k}\Omega$ .
- i. Pin characteristic only during D4 strobe time.
- j. Minimum positive going pulse width to initiate conversion.
- k. All outputs disconnected.

## 4 1/2-Digit A/D Converter Set

### FEATURES

- 0.005%  $\pm 1$  Count Accuracy
- Two Ranges
- Auto-zero
- Auto-polarity
- Over and Under Range Outputs

### BENEFITS

- High System Performance
- Single Resistor Programming
- Nulls Out Offsets
- Single Reference
- Easily Interfaced

### APPLICATIONS

- High Accuracy Digital Voltmeters and Panel Meters
- Digital Scales and Thermometers
- $\mu$ P Data Acquisition Systems
- Scientific Instrumentation

### DESCRIPTION

The LD122 and LD121A form a precision 4 1/2 digit A/D converter system for use in display and microprocessor based data acquisition applications. Based on Siliconix's "Quantized Feedback" technique, intrinsic features include auto-polarity, auto-zero, and ratiometric operation.

The LD122/LD121A combination is used to extend system resolution beyond the 10  $\mu$ V maximum available from the LD120/LD121A system. By adding a user selected low noise input amplifier and appropriate filter, any input resolution can be achieved. Except for this added buffer and a stable reference, no critical components are required to achieve rated performance. The technique used offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts. Thus, critical, high resolution performance is not required of either the integrator or the comparator.

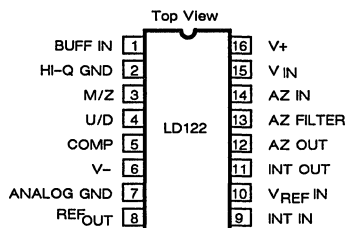
The LD122 analog processor is fabricated with a

unique combined PMOS/Bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered on the LD122 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD122 directly interfaces the LD121A digital processor with no additional active components required.

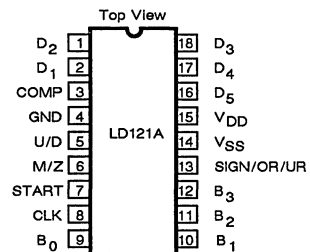
The LD121A synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4-1/2 digits of multiplexed BCD data. (All outputs are TTL compatible.) Overage is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user's option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

Both devices are supplied in space saving 300 mil dual-in-line plastic packages and in the commercial, C suffix (0 to 70°C) temperature range.

### PIN CONFIGURATION

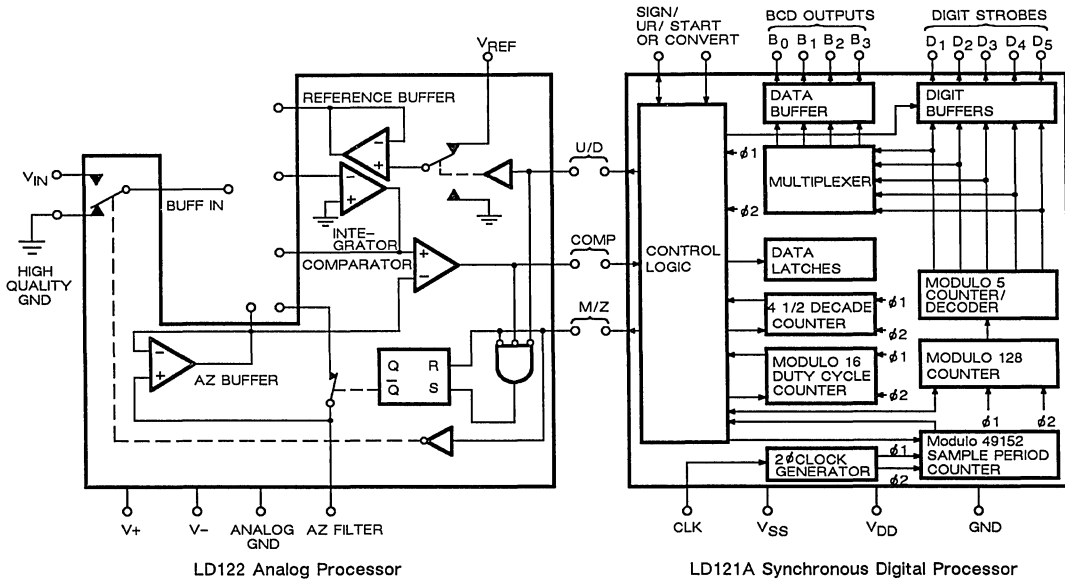


Order Number: LD122CJ



Order Number: LD121ACJ

## FUNCTIONAL BLOCK DIAGRAM



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

### ABSOLUTE MAXIMUM RATINGS

$V_{IN}$ (Pin 15, 2 LD122) .....	$V^- < V_{IN} < V^+$
$V^+ - V^-$ (LD122) .....	32 V
$V_{SS} - V_{DD}$ (LD121A) .....	20 V
Any Pin (LD121A) .....	$V_{DD}$ to $V_{SS} \pm 0.3$ V
$V_{REF}$ .....	$V^+$

Operating Temperature .....	0 to 70°C
Storage Temperature .....	-65 to 125°C
Power Dissipation (Package)* .....	750 mW

\* Device mounted with all leads welded or soldered to PC Board. Derated 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = V <sub>DD</sub> = -12 V V <sub>SS</sub> = 5 V	LIMITS				UNIT	
			1=25°C		C SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SYSTEM <sup>e</sup></b>								
Linearity		f <sub>CLOCK</sub> = 163.84 kHz V <sub>REF</sub> = 6.8 V	2 V Scale	1	± ¼	-1	1	Count
			200 mV Scale	1	± ½	-2	2	
Noise <sup>f</sup>			2 V Scale	1	⅓		1	
			200 mV Scale	1	½		2	
Normal Mode Rejection Ratio	NMRR		f <sub>L</sub> = 50 Hz or 60 Hz	1	40			dB
Power Supply Rejection Ratio	PSRR			1	80			
Gain T.C.				1	5		15	ppm/°C
Zero Drift			C <sub>STRG</sub> = 1 μF R <sub>IN</sub> ≤ 100 kΩ	1	1		5	Count

ELECTRICAL CHARACTERISTICS <sup>a</sup>									LD122 (LINEAR CIRCUIT)		
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = V <sub>DD</sub> = -12 V V <sub>SS</sub> = 5 V	LIMITS				UNIT				
			1=25°C		C SUFFIX						
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>					
<b>INPUT BUFFER</b>											
Analog Input Voltage	V <sub>ANALOG</sub>		1		-3	3	V				
ON Resistance V <sub>IN</sub> or HI-Q Switches	r <sub>DS(ON)</sub>	V <sub>A</sub> = 1 V	1			5.5	kΩ				
		V <sub>A</sub> = -1 V	1			8					
Leakage Current Switch ON or OFF	I <sub>LEAKAGE</sub>	V <sub>IN</sub> = ±2.8 V	1	2			pA				
Input Current/ Input Voltage HIGH	I <sub>IH</sub>	M/Z, U/D Inputs	V <sub>IN</sub> = 2.0 V	1		20	μA				
Input Current/ Input Voltage LOW	I <sub>IL</sub>		V <sub>IN</sub> = 0.8 V	1		-100					



ELECTRICAL CHARACTERISTICS <sup>a</sup>			LD122 (LINEAR CIRCUIT) (Cont'd)				
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = V <sub>DD</sub> = -12 V V <sub>SS</sub> = 5 V	LIMITS				UNIT
			1=25°C		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>AZ BUFFER</b>							
Output Source Current	I <sub>SOURCE</sub>		1	-100			μA
Output Sink Current	I <sub>SINK</sub>		1	800			
Offset Voltage	V <sub>OS</sub>	V <sub>OUT</sub> = 0 V	1		-50	50	mV
On Resistance <sup>g</sup>	r <sub>DS(ON)</sub>	V <sub>STRG</sub> = -4 V I <sub>DS</sub> = 30 μA	1	6		20	kΩ
<b>REFERENCE BUFFER</b>							
Reference Buffer Source Current	I <sub>SOURCE</sub>	V <sub>IN</sub> (U/D IN) = 0.8 V V <sub>O</sub> = 0 V	1	-800		-400	μA
Reference Buffer Sink Current	I <sub>SINK</sub>	V <sub>IN</sub> (U/D IN) = 0.2 V V <sub>O</sub> = 2 V	1	100			
<b>INTEGRATOR</b>							
Integrator Source Current <sup>h</sup>	I <sub>SOURCE</sub>	V <sub>IN</sub> (INT. IN) = -100 mV V <sub>O</sub> = 0 V	1	-100		-50	μA
Integrator Sink Current <sup>h</sup>	I <sub>SINK</sub>	V <sub>IN</sub> (INT. IN) = 100 mV V <sub>O</sub> = 0 V	1	800	400		
Output Swing			1		-10	10	V
<b>COMPARATOR</b>							
Comparator Output Swing	V <sub>OUT</sub>	R <sub>L</sub> = 10 k to 5 V AZ Filter IN = 100 mV Integrator OUT = 0 V	1		-5		V
Comparator Offset Voltage	V <sub>OS</sub>		1		-5	5	mV
<b>SUPPLY</b>							
Positive Supply Voltage	V <sub>+</sub>		1	12	9	15	V
Negative Supply Voltage	V <sub>-</sub>		1	-12	-15	-9	
Positive Supply Current	I <sub>+</sub>		1			3.5	mA
Negative Supply Current	I <sub>-</sub>		1		-3		
Ground Current	I <sub>GND</sub>	M/Z, U/D = 2.4 V			-2		

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ELECTRICAL CHARACTERISTICS <sup>a</sup>				LD121 (DIGITAL CIRCUIT)				
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 12 V V <sub>-</sub> = V <sub>DD</sub> = -12 V V <sub>SS</sub> = 5 V	LIMITS				UNIT	
			1=25°C		C SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUTS</b>								
Input Voltage HIGH	V <sub>INH</sub>	Comparator Input, Sign/UR/OR/Blink <sup>1</sup> Start, CLK IN	1		4		V	
Input Voltage LOW	V <sub>INL</sub>		1			0.5		
Input Current/ Input Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 5 V (Sign/OR/UR <sup>1</sup> )	1	170		300	μA	
Input Current/ Input Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V (Start Convert, Clock)	1	-150	-400			
<b>OUTPUTS</b>								
Output Voltage HIGH	V <sub>OH</sub>	Bit Lines Sign/OR/UR Digital Strokes	I <sub>OH</sub> = -40 μA	1		2.4	V	
Output Voltage LOW	V <sub>OL</sub>		I <sub>OL</sub> = 1.6 mA	1		0.6		
Output Voltage HIGH	V <sub>OH</sub>	M/Z	I <sub>OH</sub> = -150 μA	1		4		
Output Voltage LOW	V <sub>OL</sub>		I <sub>OL</sub> = 0.8 mA	1		0.6		
Output Voltage HIGH	V <sub>OH</sub>	U/D	I <sub>OH</sub> = -0.5 μA			4		
Output Voltage LOW	V <sub>OL</sub>		I <sub>OL</sub> = 0.8 mA			0.6		
<b>DYNAMIC</b>								
Start Convert <sup>l</sup>	t <sub>p</sub>		1		20		μs	
Clock Frequency	f <sub>CLOCK</sub>	50% Duty Cycle	1		50	250	kHz	
Rep. Rate (Strokes)		f <sub>CLOCK</sub> ÷ 640	1		78	470	Hz	
<b>SUPPLY</b>								
Positive Supply Voltage	V <sub>SS</sub>	Range Over Which Functionality Is Guaranteed	1	5	4.5	5.5	V	
Negative Supply Voltage	V <sub>DD</sub>		1	-12	-13.2	-10.8		
Positive Supply Current <sup>k</sup>	I <sub>SS</sub>		1	14		25	mA	
Negative Supply Current	I <sub>DD</sub>		1	-14	-25			

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## ELECTRICAL CHARACTERISTICS <sup>a</sup>

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NOTES:

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. System parameters not directly tested.
- f. Bit width over which reading is stable 95% of the time.
- g.  $V_{STRG}$  must be more positive than  $-4$  V.
- h. Reference source impedance must be less than  $10$  k $\Omega$ .
- i. Pin characteristic only during D4 strobe time.
- j. Minimum positive going pulse width to initiate conversion.
- k. All outputs disconnected.

# Si2504

## High Speed 12-Bit SAR

### FEATURES

- High Speed (40 MHz typ.)
- Low Quiescent Power ( $I_{CC} < 10\mu A$ )
- Three-State Outputs
- Expandable Via Cascading
- Can Be Short-Cycled

### BENEFITS

- Reduced Conversion Time
- Reduced Power Consumption
- Allows In-Circuit Trims
- Facilitates Higher Resolution A/D Converters
- Optimizes Conversion Time

### APPLICATIONS

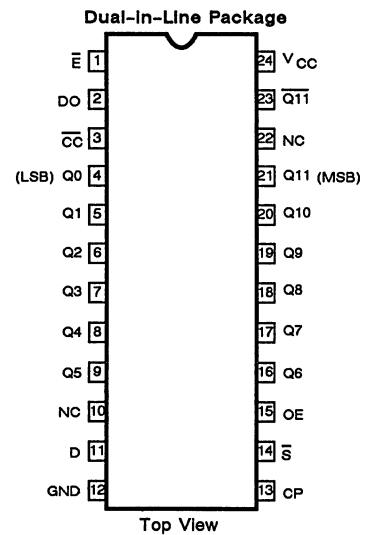
- High-Speed A/D Converters
- Low-Power Data Acquisition Systems
- Laser-Trimmed A/D Converters
- High Resolution A/D Converters
- Variable-Resolution Systems

### DESCRIPTION

The Si2504 is a high-speed, low power CMOS 12-Bit SAR (successive approximation register) that contains all of the necessary digital control and storage to build a 12-Bit successive-approximation A/D converter when combined with a 12-Bit D/A converter and a comparator. The register can be cascaded for applications requiring more than 12 bits of resolution, and may be short-cycled to reduce the conversion time in lower-resolution applications. Applications include custom and/or hybrid A/D converters with resolutions from 8 to 12 bits, and up to 24 bits when cascading two devices. The 12 data outputs have 3-state output buffers, allowing the SAR to be placed in a high-impedance mode, allowing the D/A converter in an A/D system to be trimmed without contending with the output of the SAR.

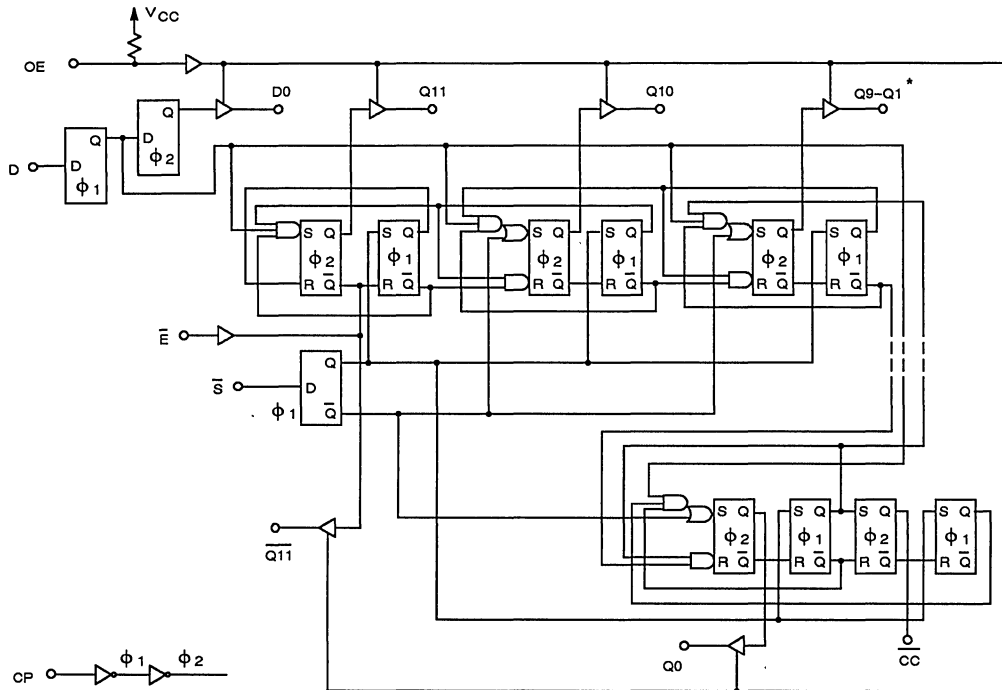
The Si2504 is built in a 2 micron silicon-gate CMOS process, allowing high speed operation at reduced power, with TTL-compatible data inputs and outputs. It is available in a 0.600" wide 24-pin plastic DIP for operation over the commercial, C suffix (0 to 70°C) temperature range. The Si2504 is also available in die form, inspected to MIL-STD-883, method 2010, visual B.

### PIN CONFIGURATION



Order Numbers:  
Si2504C.J  
Plastic DIP  
Si2504 Dice

**FUNCTIONAL BLOCK DIAGRAM**



\* Cell logic is repeated for stages Q9 to Q1.

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**ABSOLUTE MAXIMUM RATINGS**

All Voltages Referenced to GND

$V_{CC}$ .....	-0.3 V to 7 V
Voltage Applied to Outputs .....	-0.3 V to $V_{CC} + 0.3$ V
Output Current .....	10 mA
Input Voltage .....	-0.3 V to $V_{CC} + 0.3$ V
Input Current .....	-30 to 5 mA

Storage Temperature .....

Operating Temperature .....

Power Dissipation (Package) \*

24-Pin Plastic DIP\*\* .....

\* All leads welded or soldered to PC board.

\*\* Derate 11.0 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{CC} = 5\text{ V} \pm 10\%$	LIMITS				UNIT	
			1=25 °C 2=70 °C 3=0 °C		C SUFFIX			
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>STATIC</b>								
High Level Output Voltage	$V_{OH}$	$I_{OH} = -2\text{ mA}$	1,2,3		3		V	
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 6\text{ mA}$	1,2,3			0.4		
High Level Input Voltage	$V_{INH}$	$V_{CC} = 5.5\text{ V}$	1,2,3		2.4			
Low Level Input Voltage	$V_{INL}$	$V_{CC} = 4.5\text{ V}$	1,2,3			0.6		
Pull-Up Resistance (OE only)	$R_{pup}$		1,2,3	500	100	900	k $\Omega$	
Input Leakage Current (except OE)	$I_{IN}$	$V_{IH} = V_{CC}, V_{IL} = \text{GND}$ $V_{CC} = 5.5\text{ V}$	1,2,3		-1	1	$\mu\text{A}$	
Output OFF State Leakage Current (except CC)	$I_{OZ}$	OE = 0 V, $V_{OUT} = V_{CC}$ or GND $V_{CC} = 5.5\text{ V}$	1,2,3		-1	1		
Static Supply Current	$I_Q$	$I_{OH} = I_{OL} = 0\text{ A}$	1,2,3			10		
Output Short Circuit <sup>d</sup> Current	$I_{SC}$	$V_{CC} = 5.5\text{ V}, V_{OUT} = 0\text{ V}$	1,2,3	-30			mA	
Supply Current	$I_{CC}$	$V_{IN} = 0\text{ V}$ or $5\text{ V}$ $f_{CLOCK} = 16.67\text{ MHz}$	1,2,3			17		
<b>DYNAMIC</b>								
Turn OFF Delay CP to Output LOW	$t_{PD-}$	$C_L = 15\text{ pF}$	Outputs Q11, $\overline{Q11}$	1	22		44	ns
			Outputs Except Q11, $\overline{Q11}$	1	15		44	
Turn OFF Delay CP to Output HIGH	$t_{PD+}$		1	15		44		
Data Setup Time	$t_{S(D)}$		1	4	-10	10		
Start Input Setup Time	$t_{S(\overline{S})}$		1	16	0	25		
Turn OFF Delay $\overline{E}$ to Q11 HIGH	$t_{PD+}(\overline{E})$		CP = HIGH $\overline{S}$ = LOW	1	10		44	
Turn ON Delay $\overline{E}$ to Q11 LOW	$t_{PD-}(\overline{E})$			1	30		44	
Bus Release Time OE to Outputs High Impedance	$t_{OER}$		$R_L = 3\text{ k}\Omega$	1	40		44	
Bus Access Time OE to Outputs $V_{IH}$ or $V_{IL}$	$t_{OEA}$			1	22		44	

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{CC} = 5\text{ V} \pm 10\%$	LIMITS				UNIT
			1=25 °C 2=70 °C 3=0 °C		C SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>							
Minimum Low Clock Pulse	$t_{PWL(CP)}$		1	23	30		ns
Minimum High Clock Pulse	$t_{PWH(CP)}$		1	10	30		
Maximum Clock Frequency	$f_{MAX}$		1	40		16.67	MHz

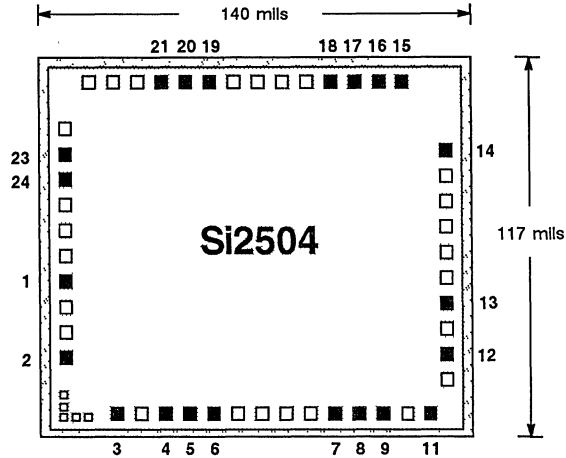
DIE SORT LIMITS							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{CC} = 5\text{ V} \pm 10\%$	LIMITS				UNIT
			1=25 °C		C SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>STATIC</b>							
High Level Output Voltage	$V_{OH}$	$I_{OH} = -2\text{ mA}$	1		3		V
Low Level Output Voltage	$V_{OL}$	$I_{OL} = 6\text{ mA}$	1			0.4	
High Level Input Voltage	$V_{INH}$	$V_{CC} = 5.5\text{ V}$	1		2.4		
Low Level Input Voltage	$V_{INL}$	$V_{CC} = 4.5\text{ V}$	1			0.6	
Pull-Up Resistance (OE only)	$R_{pup}$		1	500	100	900	k $\Omega$
Input Leakage Current (except OE)	$I_{IN}$	$V_{IH} = V_{CC}, V_{IL} = \text{GND}$ $V_{CC} = 5.5\text{ V}$	1		-1.0	1.0	$\mu\text{A}$
Output OFF State Leakage Current (except $\overline{CC}$ )	$I_{OZ}$	$\text{OE} = 0\text{ V}, V_{OUT} = V_{CC}\text{ or GND}$ $V_{CC} = 5.5\text{ V}$	1		-1.0	1.0	
Static Supply Current	$I_Q$	$I_{OH} = I_{OL} = 0\text{ V}$	1			10.0	
Output Short Circuit <sup>d</sup> Current	$I_{SC}$	$V_{CC} = \text{Max}, V_{OUT} = 0\text{ V}$	1	-30			mA

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. No more than one output should be short circuited at one time. Duration of short circuit should be less than 1 s.

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## DIE TOPOGRAPHY



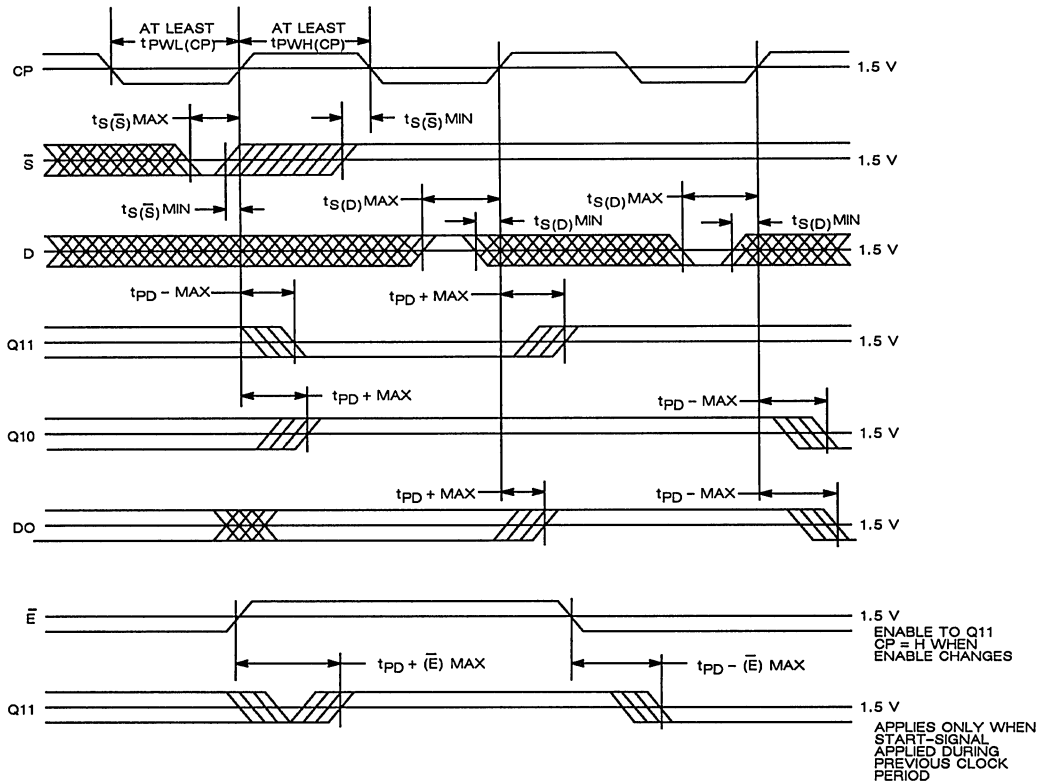
## TRUTH TABLE

TIME	INPUTS				OUTPUTS														
	$t_n$	D	$\bar{S}$	$\bar{E}$	OE	DO	Q <sub>11</sub>	Q <sub>10</sub>	Q <sub>9</sub>	Q <sub>8</sub>	Q <sub>7</sub>	Q <sub>6</sub>	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	$\overline{CC}$
0	X	L	L	H		X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	H		X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	H		D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	H		D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	H		D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	H		D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	H		D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	H		D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	H		D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	H		D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	H		D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	H		D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	H		D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	H		D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	H		X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	H		X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	X	X	X	L		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	NC

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, NC = No Change, Z = HIGH Impedance

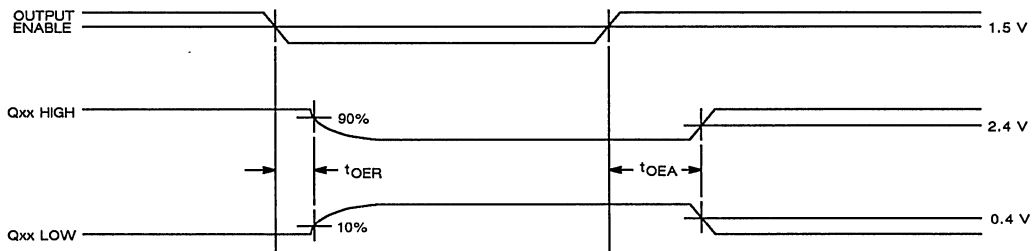


**SWITCHING TIME WAVEFORMS**



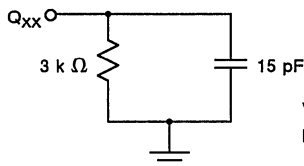
**6**

**SWITCHING TIME WAVEFORMS (OUTPUT ENABLE)**

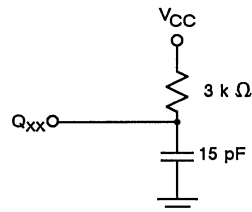


**TEST CONDITIONS:**



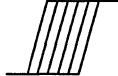
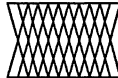
$V_{OH}$  to HIGH - Z or HIGH - Z to  $V_{OH}$



$V_{OL}$  to HIGH - Z or HIGH - Z to  $V_{OL}$



## DEFINITIONS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

KEY TO TIMING DIAGRAM

- $t_{PD-}$  The propagation delay from the clock signal LOW  $\rightarrow$  HIGH transition to an output signal HIGH  $\rightarrow$  LOW transition.
- $t_{PD+}$  The propagation delay from the clock signal LOW  $\rightarrow$  HIGH transition to an output signal LOW  $\rightarrow$  HIGH transition.
- $t_{PD-}(\bar{E})$  The propagation delay from the Enable signal HIGH  $\rightarrow$  LOW transition to the Q11 output signal HIGH  $\rightarrow$  LOW transition.
- $t_{PD+}(\bar{E})$  The propagation delay from the Enable signal LOW  $\rightarrow$  HIGH transition to the Q11 output signal LOW  $\rightarrow$  HIGH transition.
- $t_{S(D)}$  The set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between  $t_s$  max and  $t_s$  min before the clock.
- $t_{S}(\bar{S})$  The set-up time required for a LOW level to be present at the  $\bar{S}$  input prior to the clock transition from LOW to HIGH in order for the register to be reset, or the time required for a HIGH level to be present on  $\bar{S}$  before the HIGH to LOW clock transition to prevent resetting.
- $t_{PW(CP)}$  The minimum clock pulse width (LOW or HIGH) required for proper register operation.
- $t_{OER}$  The delay from OE to a 10% change in the outputs when loaded with 3 k $\Omega$  and 15 pF.
- $t_{OEA}$  The delay from OE to an output crossing 2.4 V or 0.4 V when loaded with 3 k $\Omega$  and 15 pF.

## OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock changes from HIGH-to-LOW, and a set of slave latches, that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter. It accepts data at the D input of the register and sends the data to the appropriate slave latch. This data appears at the register output and the DO output on the Si2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW, ready for the next iteration and so on for each successive bit conversion cycle.

The register is reset by holding the  $\bar{S}$  (Start) signal LOW during a full clock LOW-to-HIGH transition. The register synchronously resets the state Q11 LOW, and all the remaining register outputs HIGH. The  $\overline{CC}$  (Conversion Complete) signal is also set HIGH at this time. After the clock has gone HIGH resetting the register, the  $\bar{S}$  signal must be removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the Q11 register bit. The Q10 register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the Q10 register bit and Q9 is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the  $\overline{CC}$  signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

## OPERATION (Cont'd)

In order to allow one's or two's complement conversion, the complementary output of the most significant register bit is made available.

An active LOW enable input ( $\overline{E}$ ) allows devices to be cascaded together to form a longer register. This is done by paralleling the clock, D and  $\overline{S}$  inputs and connecting the  $\overline{CC}$  output to the  $\overline{E}$  input of the next less significant device. When the Start signal resets the registers, the  $\overline{CC}$  and  $\overline{E}$  signals go HIGH, starting conversion in the MS Device and inhibiting the next less significant device from accepting data

until the previous device is full and its  $\overline{CC}$  goes LOW. If only one device is used the  $\overline{E}$  input should be held at a LOW logic level. If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the  $\overline{CC}$  signal to indicate the end of conversion.

The Q and DO outputs may be forced into a high impedance state by bringing OE LOW. This allows busing on common microprocessor buses or laser trimming of hybrid circuits without damaging the Si2504.

## APPLICATION HINTS

1. The register can be used with current switches that require either a LOW voltage level or a HIGH voltage level to turn the switch on. If current switches are used which turn on with a LOW logic level, the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a HIGH logic level then the digital output is active HIGH; a logic "1" is represented as a HIGH voltage level.
2. For a maximum digital error of  $\pm 1/2$  LSB the comparator must be biased. If current switches that require a LOW logic level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a HIGH logic level to turn ON then the comparator must be biased -1/2 LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion. Additional data input gating should be used to eliminate the possibility of false BCD coding.
4. The register can be used to perform 2's complement conversion by offsetting the comparator 1/2 full range +1/2 LSB and using  $\overline{Q11}$  as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the Start input the OR function of  $\overline{CC}$  and the appropriate register output.

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
1	$\overline{E}$	Register ENABLE. This input is used to expand the length of the register and when HIGH forces the Q11 register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (GND).
2	DO	The serial DATA OUTPUT.
3	$\overline{CC}$	CONVERSION COMPLETE output. This output remains HIGH during conversion and goes LOW when a conversion is complete.
4-9	Q0-Q5	Register OUTPUTS. The six least significant bits of the register. Q0 is the LSB.

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**PIN DESCRIPTION (Cont'd)**


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PIN NUMBER	SYMBOL	DESCRIPTION
10	NC	No connection.
11	D	Serial DATA Input.
12	GND	Ground.
13	CP	CLOCK PULSE Input.
14	$\bar{S}$	START input. Holding this input LOW for at least one clock period will reset the register to Q11 = LOW and Q0 – Q10 = HIGH. A LOW of one clock period is not necessary if it meets the set-up time requirements of the $\bar{S}$ input.
15	OE	OUTPUT ENABLE input. A LOW on this input will disable the Q11 – Q0, $\bar{Q}11$ outputs putting them in a HIGH IMPEDANCE state. This input has an internal pull-up and needs no connection for normal operation.
16–21	Q6–Q11	Register OUTPUTS. The six most significant bits of the register. Q11 is the MSB.
22	NC	No Connection.
23	$\bar{Q}11$	Complementary output of the MSB register.
24	$V_{CC}$	Positive power supply input.

## Precision 4 1/2-Digit Single Chip CMOS A/D Converter

### FEATURES

- Accuracy  $\pm 1$  Count in  $\pm 20,000$  Counts
- 1 pA Input Current
- Auto Zero
- Differential Input (CMRR = 86 dB typ.)
- 15 mW Power Consumption
- Multiplexed BCD Outputs

### BENEFITS

- Improves System Accuracy
- Reduced Loading of High Impedance Sources
- No External Zero Adjust
- Improved Common-Mode Signal Rejection
- Battery Operation
- Simplifies Display Interfacing

### APPLICATIONS

- High Resolution Data Acquisition (15 bit)
- Direct Measurement of High Impedance Signals
- Precision DMM and DVM's
- Temperature Measuring Instruments
- Remote Data Measurement
- Panel Meters

### DESCRIPTION

The Si7135 is a precision 4 1/2 digit integrating A/D converter system for use in display and microprocessor based data acquisition applications. Based on the reliable dual slope conversion technique, intrinsic features include 2.0000 V full scale range, differential inputs, auto-polarity, auto-zero, and ratiometric operation to achieve a high level of versatility for the systems designer. The multiplexed BCD outputs, when connected to display drivers, make the Si7135 an ideal solution for visual display DVM/DPM applications.

Manufactured on the Siliconix proprietary PolyMOS process, the Si7135 exhibits improved linearity over the industry-standard ICL7135, eliminating the linearizing components required by the generic devices. An epitaxial layer prevents latchup.

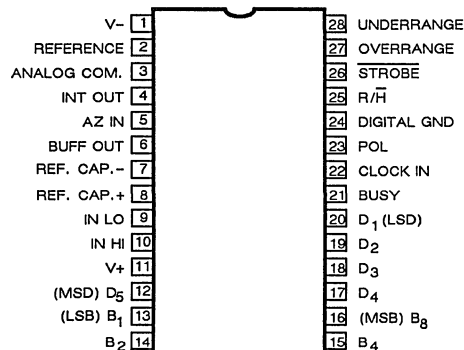
Package options include the 28-pin plastic DIP, CerDIP, and PLCC packages. All are rated for performance over the commercial, C suffix (0 to 70°C) temperature range.

For more information on the Si7135, please refer to Siliconix Application Note AN83-14.

**6**

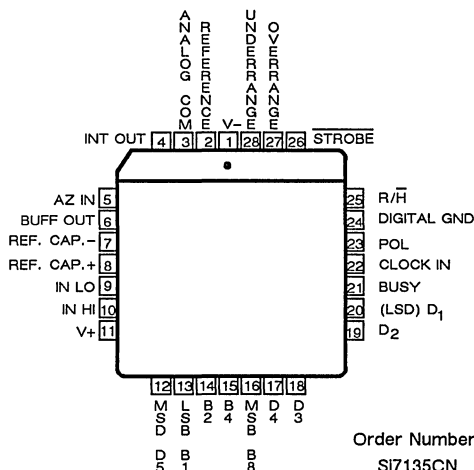
### PIN CONFIGURATION

Dual-In-Line Package



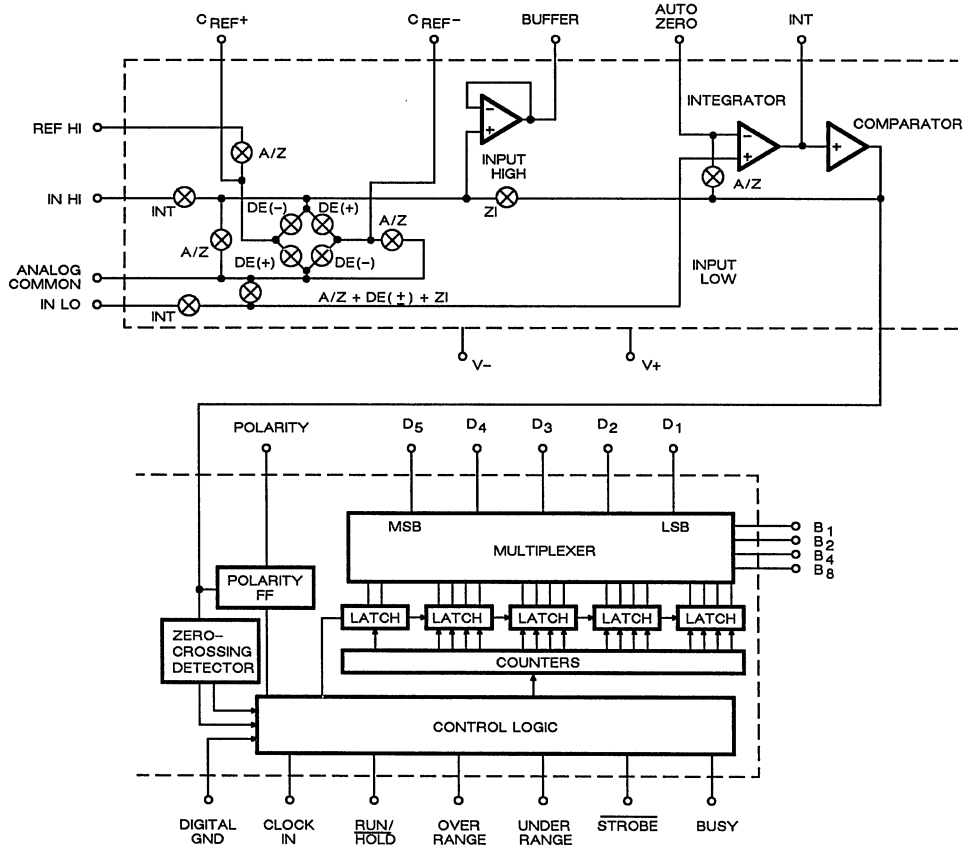
Order Numbers:  
CerDIP: Si7135CK  
Plastic: Si7135CJ

PLCC-28 Package



Order Number:  
Si7135CN

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

### Supply Voltage

V+	.....	6 V
V-	.....	-9 V

Analog Input Voltage (either input)<sup>d</sup> ..... V+ to V-

Reference Input Voltage (either input) ..... V+ to V-

Clock Input ..... GND to V+

### Power Dissipation \*

Ceramic Package	.....	1000 mW
Plastic Package	.....	800 mW
PLCC	.....	450 mW

Operating Temperature ..... 0 to 70°C

Storage Temperature ..... -65 to 125°C

Lead Temperature (Soldering, 10 s) ..... 300°C

\* Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

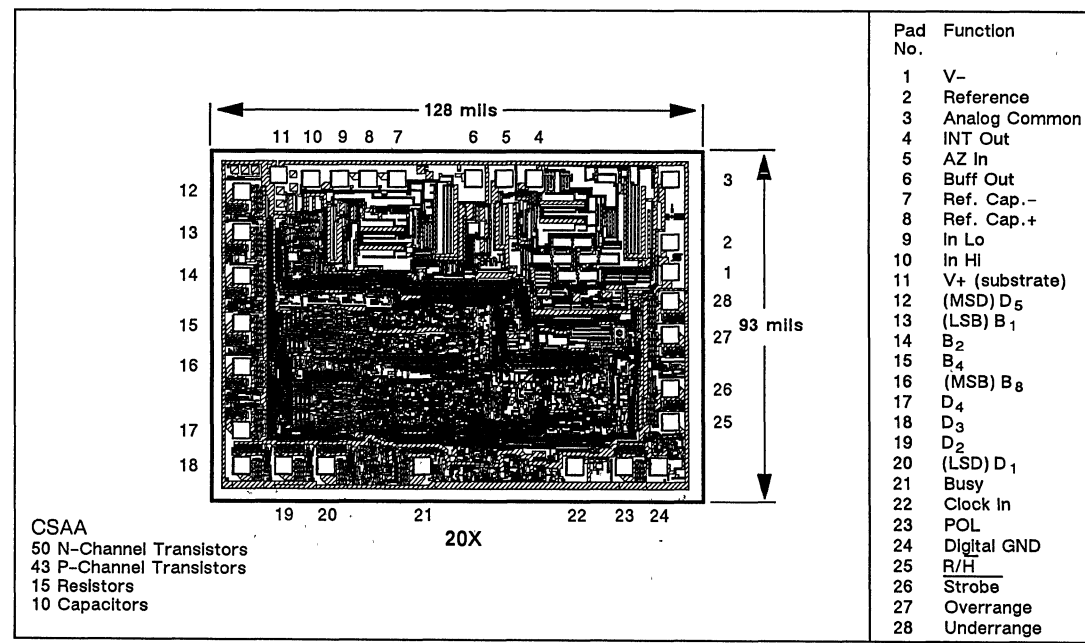
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 5 V, V <sub>-</sub> = -5 f <sub>clock</sub> = 120 kHz Full Scale = 2.0000 V	LIMITS				UNIT	
			1=25 °C 2=70 °C 3=0 °C		C SUFFIX			
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>ANALOG</b>								
Analog Input Range	V <sub>INPUT</sub>		1		-2	2	V	
Zero Input Reading		See Figure 1 V <sub>IN</sub> = 0 V	1	± 0.0000	-0.0000	0.0000	Digital Reading	
Ratiometric Reading		See Figure 1 V <sub>IN</sub> = V <sub>REF</sub>	1	0.9999	0.9998	1.0000		
Linearity Error <sup>e</sup>	INL	See Figure 1 -2 V ≤ V <sub>IN</sub> ≤ 2 V	1	0.5		1.5	Counts (LSB)	
Differential Non-linearity <sup>f</sup>	DNL		1	0.01				
Rollover Error <sup>g</sup>			1	1		3		
Input Leakage Current	I <sub>ILK</sub>	V <sub>IN</sub> = 0 V	1	1		10	pA	
Noise <sup>h</sup>	e <sub>N</sub>	See Figure 1 V <sub>IN</sub> = 0 V	1	15			μV	
<b>DIGITAL INPUTS</b>								
Input HIGH Voltage	V <sub>INH</sub>	See Figure 2 CLOCK IN, RUN/HOLD	1	2.2	2.8		V	
Input LOW Voltage	V <sub>INL</sub>		1	1.6		0.8		
Input HIGH Current	I <sub>INH</sub>		V <sub>IN</sub> = 5 V	1	0.02		0.1	mA
Input LOW Current	I <sub>INL</sub>		V <sub>IN</sub> = 0 V	1	0.1		10	μA
<b>DIGITAL OUTPUTS</b>								
Output Voltage LOW	V <sub>OL</sub>	I <sub>OL</sub> = 1.6 mA	1	0.25		0.4	V	
Output Voltage HIGH	V <sub>OH</sub>	Pins 12-20 I <sub>OH</sub> = -1 mA	1	4.2	2.4			
		Pins 21, 23, 26, 27, 28 I <sub>OH</sub> = -10 μA	1	4.99	4.9			
<b>SUPPLY</b>								
+5 V Supply Range	V <sub>+</sub>		1	5	4	6	V	
-5 V Supply Range	V <sub>-</sub>		1	-5				

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 5 V, V <sub>-</sub> = -5 f <sub>clock</sub> = 120 kHz Full Scale = 2.0000 V	LIMITS				UNIT
			1=25 °C 2=70 °C 3=0 °C		C SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY (Cont'd)</b>							
+ 5 V Supply Current	I+		1	1.1		3	mA
- 5 V Supply Current	I-		1	0.8		3	
<b>DYNAMIC</b>							
Clock Frequency <sup>d</sup>			1	120	dc	200	kHz

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. Input voltages may exceed the supply voltages provided the input current is limited to 100µA.
- e. Error of reading from best straight line.
- f. Difference between worst case step of adjacent counts and ideal step.
- g. Difference in reading for equal positive and negative readings near full scale.
- h. Peak-to-peak value not exceeding 95% of the time.
- i. The temperature range can be extended beyond 70 °C as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the Si7135.
- j. This specification relates to the clock frequency range over which the Si7135 will correctly perform its various functions. See the MAXIMUM CLOCK FREQUENCY section of the description for limitations on the clock frequency range in a system.

**DIE TOPOGRAPHY**





**TEST CIRCUITS**

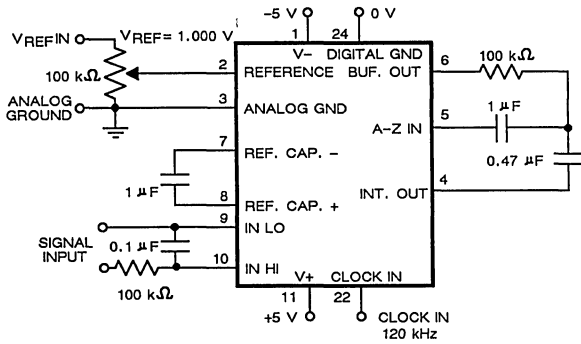


Figure 1. SI7135 Test Circuit

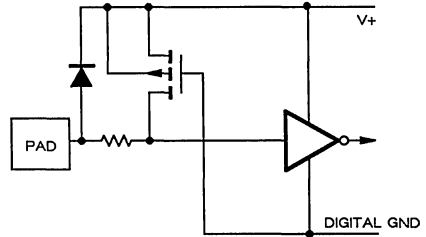


Figure 2. Logic Input Circuit

**DETAILED DESCRIPTION**

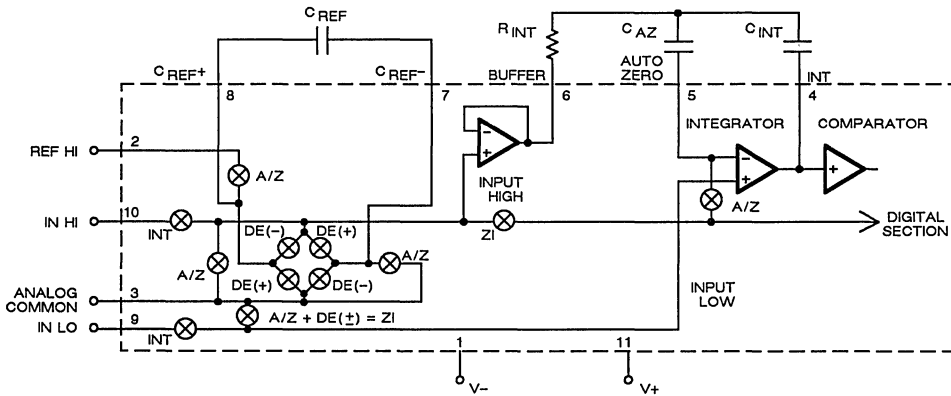


Figure 3. Analog Section of the SI7135

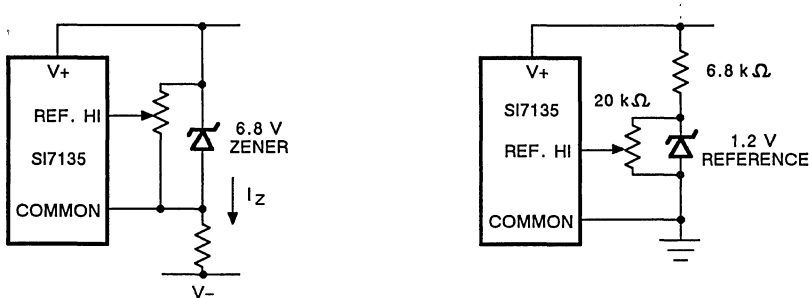


Figure 4. Generating External References

## DETAILED DESCRIPTION (Cont'd)

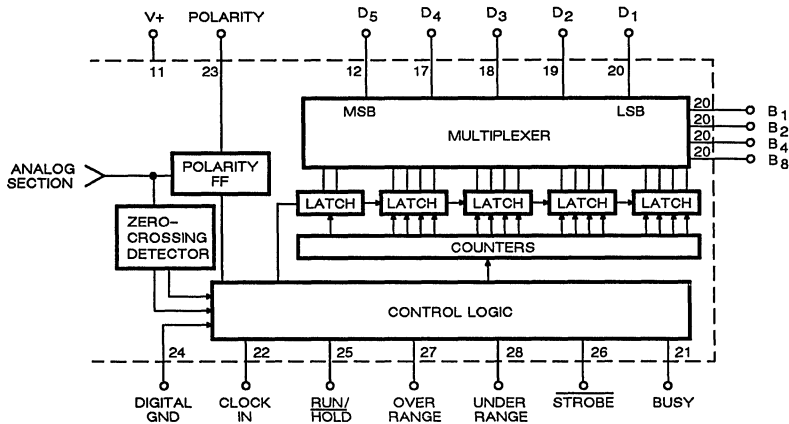


Figure 5. Digital Section

## ANALOG SECTION

Figure 3 shows the block diagram of the analog section for the Si7135, figure 5 shows the digital section, and figure 6 shows the timing diagram. Each measurement cycle is divided into four phases. They are (1) AUTO-ZERO (AZ), (2) SIGNAL INTEGRATE (SI), (3) REFERENCE INTEGRATE (RI) and (4) ZERO INTEGRATOR (ZI).

1. **AUTO-ZERO (AZ) PHASE:** First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor  $C_{AZ}$  to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than  $10 \mu\text{V}$ .
2. **SIGNAL INTEGRATE (SI) PHASE:** During this phase, the auto-zero loop is opened, the internal short is removed, and the internal input high and input low nodes are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be

within a common mode range which is specified from 0.5 V below the positive supply to 1.0 V above the negative supply. If the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the Polarity flip flop.

3. **REFERENCE INTEGRATE (RI) PHASE:** IN LO is internally connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the value of input signal. Specifically the digital reading displayed is

$$10,000 \frac{V_{IN}}{V_{REF}}$$

4. **ZERO INTEGRATOR (ZI) PHASE:** First, IN LO is shorted to analog COMMON. Second, a feedback loop is closed around the system to IN HI to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

**DETAILED DESCRIPTION (Cont'd)****DIFFERENTIAL INPUT**

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 V below the positive supply to 1.0 V above the negative supply. In this range the system has a typical CMRR of 86 dB. However, since the integrator also swings with the common mode voltage, care must be taken to insure that the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4 V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 V of either supply without loss of linearity.

**ANALOG COMMON**

Analog COMMON is used as the input low return during AUTO-ZERO and REFERENCE INTEGRATE. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

**REFERENCE**

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Figure 4.

**DIGITAL SECTION**

Figure 5 shows the digital section of the Si7135. The Si7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

1. RUN/HOLD ( $\overline{R/H}$ ) (Pin 25): When high (or open) the Si7135 will free-run with equally spaced measurement cycles every 40,002 clock pulses. If taken low, the Si7135 will continue the full measurement cycle and then hold this reading as long as  $\overline{R/H}$  is held low. A short

positive pulse (greater than 300 ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of AUTO-ZERO. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if  $\overline{R/H}$  is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

2. STROBE (Pin 26): This is a negative-going output pulse that aids in transferring the BCD data to external latches for UARTs or microprocessors. There are 5 negative-going STROBE pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first STROBE pulse goes negative for 1/2 clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the STROBE pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional STROBE pulses will be sent until a new measurement is available.
3. BUSY (Pin 21): BUSY goes high at the beginning of signal integration and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an overrange). The internal latches are loaded during the first clock pulse after BUSY goes high and are latched at the end of this clock pulse. The circuit automatically reverts to AUTO-ZERO when not BUSY, so it may also be considered a ( $\overline{ZI} + \overline{AZ}$ ) signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with CLOCK and subtract 10,001 counts from the number of pulses received -- as mentioned previously there is one "no-count" pulse in each REFERENCE INTEGRATE cycle.

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**DETAILED DESCRIPTION (Cont'd)**


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4. **OVER-RANGE (Pin 27):** This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output is set at the end of BUSY and is reset to zero at the beginning of REFERENCE INTEGRATE in the next measurement cycle.
5. **UNDER-RANGE (Pin 28):** This pin goes positive when the reading is 9% of range or less. The output flip-flop is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of SIGNAL INTEGRATE of the next reading.
6. **POLARITY (POL) (Pin 23):** This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (-) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is revalidated for the next measurement.
7. **DIGIT DRIVES (Pins 12, 17, 18, 19 and 20):** Each digit drive is a positive-going signal that lasts for 200 clock pulses. The scan sequence is D<sub>5</sub> (MSD), D<sub>4</sub>, D<sub>3</sub>, D<sub>2</sub> and D<sub>1</sub> (LSD). All five digits are scanned and this scan is continuous unless an overrange occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference integrate when D<sub>5</sub> will start the scan again. This can give a blinking display as a visual indication of overrange.
8. **BCD (Pins 13, 14, 15 and 16):** The binary coded decimal bits B<sub>8</sub>, B<sub>4</sub>, B<sub>2</sub> and B<sub>1</sub> are positive logic signals that go on simultaneously with the digit driver signal.

---

**COMPONENT VALUE SELECTION**


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For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate.

**INTEGRATING RESISTOR**

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100  $\mu$ A of quiescent current. They can supply 20  $\mu$ A of drive current with negligible non-linearity. Values of 5 to 40  $\mu$ A give good results, with nominal of 20  $\mu$ A, and the exact value of integrating resistor may be chosen by:

$$R_{INT} = \frac{\text{full scale voltage}}{20 \mu\text{A}}$$

**INTEGRATING CAPACITOR**

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance build-up will not saturate the integrator swing (approximately 0.3 V from either supply.) For  $\pm 5$  V supplies and analog COMMON tied to supply ground, a  $\pm 3.5$  to

4 V full scale integrator swing is fine, and 0.47  $\mu$ F is nominal. In general, the value of C<sub>INT</sub> is given by:

$$C_{INT} = \frac{(10,000) \times (\text{clock period}) \times I_{INT}}{\text{integrator output voltage swing}} =$$

$$C_{INT} = \frac{(10,000) \times (\text{clock period}) \times (20 \mu\text{A})}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

**AUTO-ZERO AND REFERENCE CAPACITOR**

The size of the auto-zero capacitor has some influence on the noise of the system, e.g. a large capacitor reduces noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

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**COMPONENT VALUE SELECTION (Cont'd)**

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The dielectric absorption of the reference and auto-zero capacitors are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper capacitors can be used here if accurate readings are not required for the first few seconds of recovery.

**REFERENCE VOLTAGE**

The analog input voltage ( $V_{IN}$ ) required to generate a full-scale output is:  $V_{IN} = 2 V_{REF}$ .

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

**MAXIMUM CLOCK FREQUENCY**

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3  $\mu$ s delay, and at a clock frequency of 160 kHz (6  $\mu$ s period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50  $\mu$ V input, 1 to 2 with 150  $\mu$ V, 2 to 3 at 250  $\mu$ V, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to 1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The clock frequency may be extended above 160 kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage onto the integrator output at the beginning of the REFERENCE INTEGRATE phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3.

At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitors. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60 Hz pickup, the SIGNAL INTEGRATE cycle should be a multiple of 60 Hz. Oscillator frequencies of 300 kHz, 200 kHz, 150 kHz, 120 kHz, 100 kHz, 40 kHz, 33 1/3 kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 250 kHz, 166 2/3 kHz, 125 kHz, 100 kHz, etc. would be suitable. Note that 100 kHz (2.5 readings/seconds) will reject both 50 and 60 Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. If the multiplexed output display takes significant current from the logic supply, the clock should have good PSRR.

**ZERO-CROSSING FLIP-FLOP**

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have decayed. False zero-crossings caused by clock pulses are not recognized. The flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

**EVALUATING THE ERROR SOURCES**

Errors from the "ideal" cycle are caused by:

1. Capacitor voltage droop due to leakage.
2. Capacitor voltage change due to charge "drain-off" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.

## COMPONENT VALUE SELECTION (Cont'd)

4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity due to dielectric absorption.
6. Charge lost by  $C_{REF}$  in charging  $C_{STRAY}$ .
7. Charge lost by  $C_{AZ}$  and  $C_{INT}$  to charge  $C_{STRAY}$ .

### NOISE

The peak-to-peak noise around zero is approximately 15  $\mu\text{V}$  (peak-to-peak value not exceeded 95% of the time.) Near full scale, this value increases to approximately 30  $\mu\text{V}$ . Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

### ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of Si7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

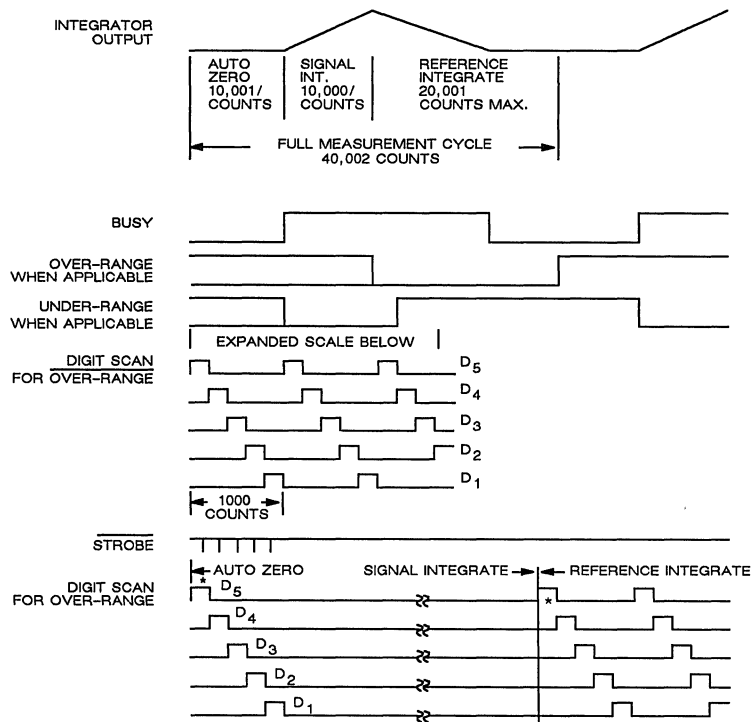
### POWER SUPPLIES

The Si7135 is designed to work from  $\pm 5\text{ V}$  supplies. However, in selected applications, no negative supply is required. The conditions to use a single +5 V supply are:

1. The input signal can be referenced to center of the common mode range of the converter.
2. The signal is less than  $\pm 1.5\text{ V}$ .

See "DIFFERENTIAL INPUT" for a discussion of the effects this will have on the integrator swing without loss of linearity.

## TIMING DIAGRAM



\* FIRST D<sub>5</sub> OF AZ AND REF INT ONE COUNT LONGER

Figure 6. Timing Diagram

**APPLICATIONS**

The popular LCD displays can be interfaced to the output of the Si7135 with suitable display drivers, such as shown in Figure 7. A standard CMOS 4000 series LCD driver circuit is used for displaying the 1/2 digit, the polarity, and an 'overrange' flag. Of

course, another full driver circuit could be ganged to the one shown, if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-1/2 digit ( $\pm 2.0000$  V) A/D.

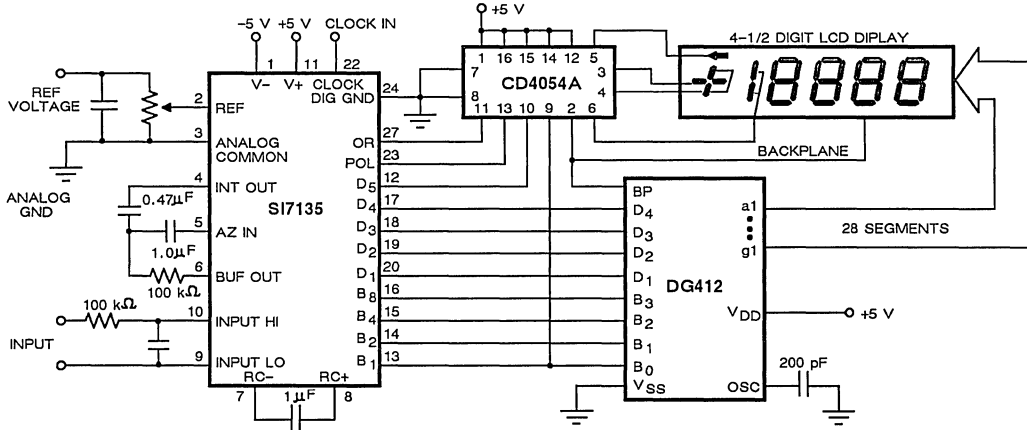


Figure 7. Driving LCD Display

**INTERFACING WITH MICROPROCESSORS**

Circuits to interface the Si7135 directly with two popular microprocessors are shown in Figures 8 and 9. The 8080/8048 and the MC6800 families with 8-bit words need to have polarity, overrange and underrange multiplexed onto the digit 5 word. In each case the microprocessor can instruct the ADC

when to begin a measurement and when to hold this measurement.

The Si7135 is designed to work from  $\pm 5$  V supplies. However, if a negative supply is not available, it can be generated using 2 capacitors, and an inexpensive Si7660 or Si7661 IC (Figure 10).

**6**

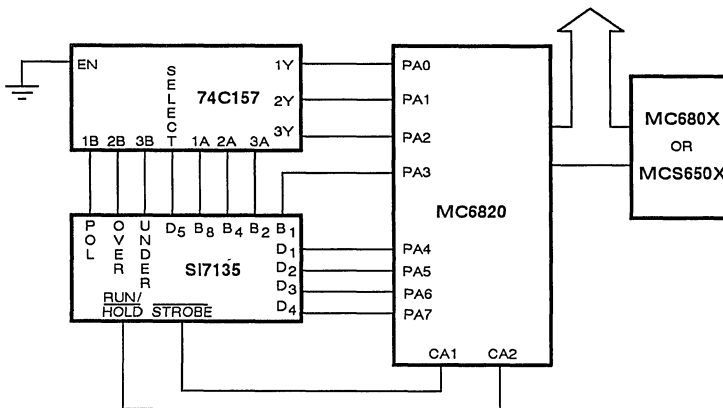


Figure 8. Interface to 680X and 650X Families

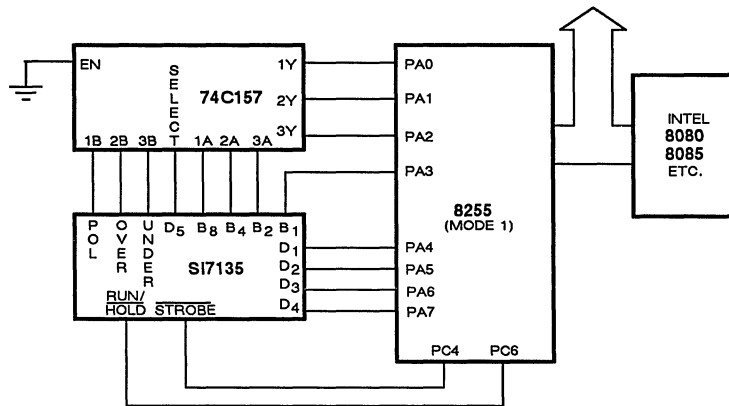


Figure 9. Interface to 8080 Family

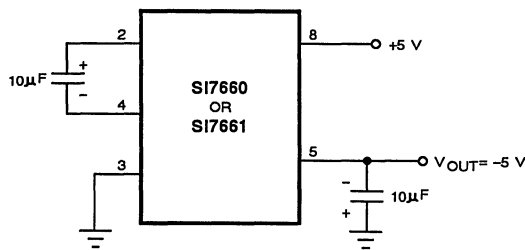


Figure 10. Generating a -5 V Supply From a +5 V Supply

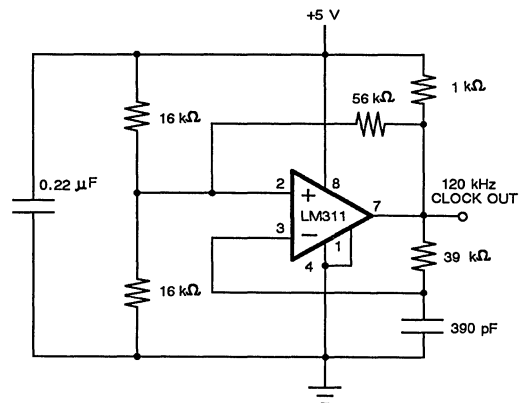


Figure 11. Comparator Clock Circuit

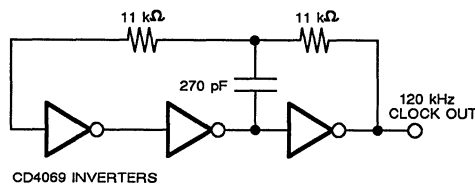


Figure 12. R - C Clock Circuit



# Si7240

## 12-Bit CMOS

### Voltage-Output DAC

#### FEATURES

- Fast Voltage Settling Time: 550 ns to 0.01%
- Total Unadjusted Error: 1 LSB Max
- Low Power Single-Supply Operation (30 mW)
- Excellent Differential Nonlinearity: 1/2 LSB Max over Temperature

#### BENEFITS

- Improved Data Throughput
- Improved Accuracy
- Reduced Power Supply
- Eliminates Instability In Servo Loops

#### APPLICATIONS

- High Speed A/D Converters
- Programmable Gain Amplifiers
- Battery-Powered Instrumentation
- Head Positioning Servos

#### DESCRIPTION

The Si7240 is a fast settling (550 ns typically to 1/2 LSB) 12-bit voltage-output digital-to-analog converter. The Si7240 operates with a single +15 V  $V_{DD}$  supply and exhibits exceptionally fast settling times due to the small (and code independent) value of capacitance at the output of the DAC. The Si7240 features 1 LSB total unadjusted error, allowing fixed reference operation without the need for external trims. All grades are guaranteed monotonic to 12 bits over all temperature ranges, in both the voltage mode and the current mode.

Applications for the Si7240 include high-speed A/D converters, digitally-controlled power supplies and

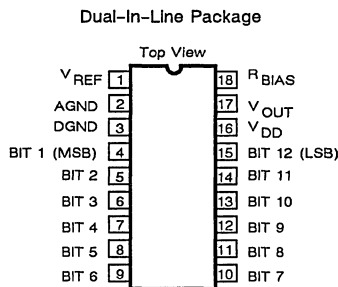
references, and digital servo systems. Its low power consumption and single-supply operation makes it ideal for battery operated and remote instrumentation applications.

Built on the Siliconix PolyMOS process, the Si7240 uses highly stable thin film resistors which are laser-trimmed for excellent accuracy. An epitaxial layer prevents latchup.

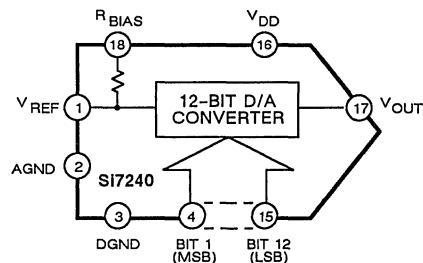
The Si7240 is available in 18-pin plastic commercial, J, K suffix (0 to 70°C), industrial, A, B suffix (-40 to 85°C), and military, S, T suffix (-55 to 125°C) temperature range.

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#### PIN CONFIGURATION



#### FUNCTION BLOCK DIAGRAM



#### ORDERING INFORMATION

Total Unadjusted Error	Plastic	CerDIP	Side Brazed Ceramic
$T_A = T_{MIN}$ to $T_{MAX}$	0 to 70°C	-40 to 85°C	-55 to 125°C
+1/2, -2 LSB	Si7240JN	Si7240AQ	Si7240SD
+1/4, -1 1/2 LSB	Si7240KN	Si7240BQ	Si7240TD

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to DGND	-0.3 V, +17 V	Power Dissipation (Any Package) to 75°C	450 mW
Digital Input Voltage to DGND	-0.3V, $V_{DD}$	Derates above 75°C	6 mW/°C
$V_{BIAS}$ , $V_{OUT}$ to DGND	$\pm 25$ V	Operating Temperature (J, K Suffix)	0 to 70°C
$V_{REF}$ to DGND	-0.3 V, $V_{DD}$	(A, B, Suffix)	-40 to 85°C
AGND to DGND	-0.3V, $V_{DD}$	(S, T Suffix)	-55 to 125°C
		Storage Temperature	-65 to 150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 15$ V, $V_{REF} = 1.23$ V AGND = DGND = $R_{BIAS} = 0$ V	LIMITS						UNIT
			1=25°C		K, B, T SUFFIX		J, A, S SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>ACCURACY</b>									
Resolution	N		1, 2, 3		12		12		Bits
Total Unadjusted Error <sup>e, f</sup>	$E_T$		1 2, 3		-1.0 -1.5	0.5 0.5	-1.25 -2.0	0.5 0.5	LSB
Relative Accuracy <sup>e, f</sup>	INL		1 2, 3		-1.0 -1.5	0.5 0.5	-1.25 -2.0	0.5 0.5	
Full Scale (Gain) Error <sup>e, f</sup>	GE		1 2, 3		-0.5 -0.5	0.5 0.5	-1.25 -2.0	0.5 0.5	
Full Scale (Gain) <sup>c</sup> Tempco	$TC_{GE}$	$\Delta$ Full Scale / $\Delta$ Temperature	1, 2, 3		-1.2	1.2	-6	6	ppm/ °C
Zero Code (Offset) Error <sup>e, f</sup>	$V_{OS}$		1 2, 3		-0.5 -0.5	0.125 0.25	-0.5 -0.5	0.25 0.5	LSB
Differential Non-linearity <sup>e, f</sup>	DNL	Monotonic to 12-Bits	1, 2, 3		-0.5	0.5	-0.5	0.5	
Power Supply Rejection Ratio	PSRR	$V_{DD} = 15.5$ V to 14.5 V All Digital Inputs HIGH	1 2, 3		-0.005 -0.01	0.005 0.01	-0.005 -0.01	0.005 0.01	% per %
<b>REFERENCE INPUT</b>									
Input Resistance (Pin 1)	$R_{REF}$	Approximately 0.67 X $R_{LADDER}$	1, 2, 3		4.7		4.7		k $\Omega$
Input Capacitance <sup>c</sup> (Pin 1)	$C_{REF}$	All Digital Inputs LOW	1, 2, 3			40		40	pF
		All Digital Inputs HIGH	1, 2, 3			100		100	
<b>DIGITAL INPUT</b>									
Input HIGH Voltage	$V_{INH}$		1, 2, 3		2.4		2.4		V
Input LOW Voltage	$V_{INL}$		1, 2, 3			0.8		0.8	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 15\text{ V}$ , $V_{REF} = 1.23\text{ V}$ $AGND = DGND = R_{BIAS} = 0\text{ V}$	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		K,B,T SUFFIX		J,A,S SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DIGITAL INPUTS (Cont'd)</b>									
Input Leakage Current	$I_{IN}$	$V_{IN} = 0\text{ V}$ or $15\text{ V}$	1,2,3		-1	1	-1	1	$\mu\text{A}$
Input Capacitance	$C_{IN}$		1,2,3			8		8	pF
<b>ANALOG OUTPUT</b>									
Output Capacitance <sup>c</sup> (Pin 17)	$C_{OUT}$		1,2,3			2.8		2.8	pF
Output Resistance (Pin 17)	$R_{OUT}$		1,2,3	12	7	15	7	15	$k\Omega$
Output Resistance Tempco	$TC_{RO}$		1,2,3	-300					ppm/ °C
Blas Resistor	$R_{BIAS}$		1,2,3	12	7	15	7	15	$k\Omega$
Blas and Ladder Resistor Matching			1,2,3	0.1					%
<b>DYNAMIC</b>									
Propagation Delay <sup>c, g</sup>	$t_{PD}$	Measured From 50% of Digital Input to 10% of Final Analog Output	1,2,3			100		100	ns
Voltage Settling Time <sup>c, g, h, i, j</sup>	$t_s$	To 0.01% of FSR For All 0's to All 1's or all 1's to All 0's	1,2,3	550		900		900	
Voltage Settling Time (J, K Grades)		To 0.04% of FSR For All 0's to All 1's or all 1's to All 0's	1,2,3	470					
		To 0.2% of FSR For All 0's to All 1's or all 1's to All 0's	1,2,3	400					
Glitch Impulse <sup>g</sup>				45				nV-s	
<b>POWER SUPPLY</b>									
$V_{DD}$ Range	$V_{DD}$	Accuracy Is Guaranteed At $V_{DD} = 15\text{ V}$	1,2,3		5	16	5	16	V
Supply Current	$I_{DD}$	All Digital Inputs $V_{IL}$ or $V_{IH}$	1,2,3			2		2	mA
		All Digital Inputs 0 V or $V_{DD}$	1,2,3			100		100	$\mu\text{A}$

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**ELECTRICAL CHARACTERISTICS**<sup>a</sup>


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**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e.  $1 \text{ LSB} = V_{\text{REF}}/4096$ .
- f. DAC Load  $R_L > 10^{10} \Omega$ .
- g. Input logic levels 0 V and 5 V.
- h. External load = 2.8 pF.
- i. Side braze versions exhibit 10% longer settling times than plastic versions.
- j. FSR = Full Scale Range.

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**CAUTION**


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ESD (Electro-Static-Discharge-Sensitive) device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy

electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

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**DEFINITION OF TERMS**


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**TOTAL UNADJUSTED ERROR**

This is a comprehensive specification which includes gain error, relative accuracy and zero code offset when configured as shown in Figure 5.

Absolute full scale is  $V_{\text{REF}} - 1 \text{ LSB (IDEAL)}$  where 1

LSB (IDEAL) is  $\frac{V_{\text{REF}}}{4096}$ .

Note: "ERROR" defined is ACTUAL VALUE - IDEAL VALUE.

**DIFFERENTIAL NONLINEARITY**

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1 \text{ LSB max}$  over the operating temperature range ensures monotonicity.

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**DETAILED DESCRIPTION**


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**CIRCUIT INFORMATION****Analog Section**

The Si7240 12-bit voltage DAC consists of a highly stable thin film R-2R ladder and twelve high speed N MOS single pole double throw switches.

The Si7240 has low capacitance at the  $V_{\text{OUT}}$  terminal, and hence exhibits fast output voltage settling times.

The simplified circuit diagram of the D/A converter is shown in Figure 1.

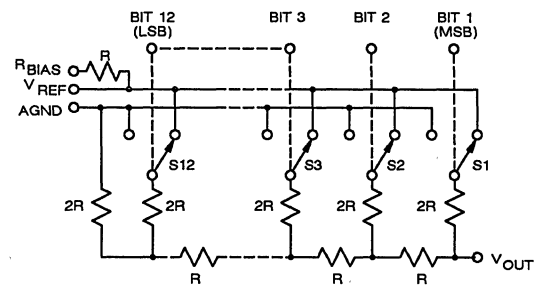


Figure 1. Si7240 Functional Diagram (Inputs High)

**DETAILED DESCRIPTION**

**Digital Section**

The 12 digital inputs are designed to be both TTL and 5 V CMOS compatible when  $V_{DD}$  equals +15 V. All logic inputs are static protected MOS gates with typical input currents of less than 1 nA. Internal input protection is achieved by an on-chip distributed diode from GND to each MOS gate. To minimize power supply current, it is recommended that the digital input voltages be driven as close to the supply rails ( $V_{DD}$  and GND) as practically possible.

**DYNAMIC PERFORMANCE**

**Output Impedance**

When operated in the voltage switching mode the Si7240 exhibits code independent (fixed) output capacitance and output resistance. This means that settling time of the Si7240 is virtually the same for all code changes when operated as per Figure 4.

In contrast, the output impedance and thus the settling time of current mode DACs is code dependent. Moreover, with a current mode CMOS DAC the large output capacitance places a limitation on the realizable settling time, even when using a fast output op amp.

The low values of output capacitance of the Si7240 ensure very fast voltage settling when configured with a high speed follower.

**Settling Time**

The time taken for voltage settling of the Si7240 to less than 1/2 LSB is given by the approximation:

\* Settling Time -  $t_{PD} + 9R (C_{OUT} + C_{EXT})$

$t_{PD}$  - Logic Propagation Delay

R - DAC Ladder Resistance

$C_{OUT}$  - DAC Output Capacitance

$C_{EXT}$  - Capacitance due to External Circuit.

\* Assuming very high load impedance.

Figure 2 shows the output voltage transient response waveform for the transition resulting when all digital inputs change from 0 to +5 V.

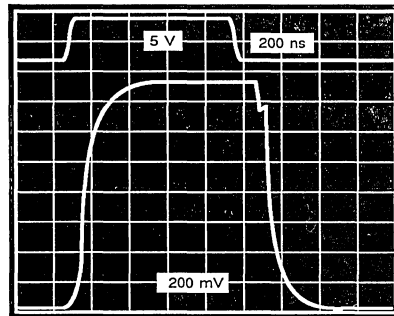


Figure 2. Si7240 Transient Response Waveform

Figure 3 shows the glitch energy waveform for the major transition. Figure 10 shows the circuit used to achieve the waveforms shown in Figures 8 and 9.

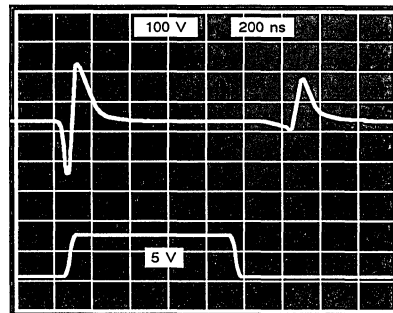


Figure 3. Si7240 Major Transition Glitch

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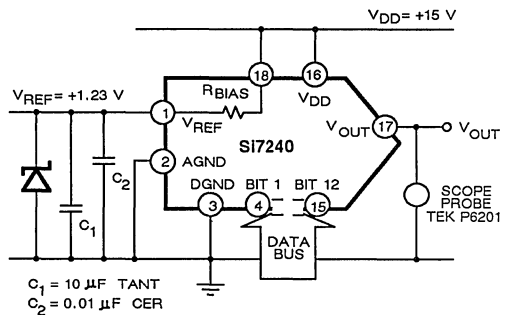


Figure 4. Dynamic Performance Test Circuit

**DETAILED DESCRIPTION (Cont'd)**
**VOLTAGE REFERENCE**

The input impedance at the  $V_{REF}$  pin of the Si7240 is code dependent and can vary from 7 k $\Omega$  up to infinity. The nodal capacitance at the reference terminal is also code dependent and typically varies

from 40 pF to 90 pF. Therefore it is essential that the reference be adequately decoupled at pin 1 of the Si7240 in order to present a low output impedance and thus maintain full accuracy under changing load conditions.

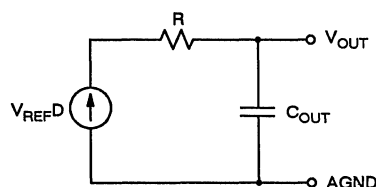
**APPLICATIONS**
**LOAD IMPEDANCE**

The Si7240 equivalent output circuit of Figure 5 shows a Thevenin voltage source  $V_{REFD}$  with a fixed output resistance and capacitance of  $R$  and  $C_{OUT}$  respectively.  $D$  is a fractional representation of the digital input word  $N$  i.e.  $D = N/4096$ .

Resistive loading at pin 17 of the Si7240 causes scale factor error. Op amp bias current through the DAC output impedance (12 k $\Omega$  nominal) introduces an offset term.

For example, a 60 M $\Omega$  load resistance on pin 17 introduces a 1 LSB scale factor error at pin 17. Op amp bias current of 25 nA introduces a 1 LSB offset term. Effects of amplifier bias current can be minimized by ensuring the parallel combination of  $R_1$  and  $R_2$  (Figure 6) is equal to the DAC's output impedance at pin 17 (nominally 12 k $\Omega$ ). If the amplifier circuit (of Figure 6) is configured to provide a gain of +1, resistor  $R_2$  should be included and should equal 12 k $\Omega$  to minimize output error due to bias current.

Figure 5 shows the equivalent circuit of the output of the Si7240.



$R$  - DAC LADDER RESISTANCE (12 k $\Omega$  TYP)  
 $C_{OUT}$  - DAC OUTPUT CAPACITANCE (2.8 pF MAX)  
 $V_{REFD}$  - THEVENIN VOLTAGE SOURCE ( $0 \leq D \leq 4095/4096$ )

Figure 5. Equivalent Output Circuit of Si7240

The Si7240 can operate in several different modes. Each mode has its own particular characteristics. These are summarized below and discussed in detail in the paragraphs following.

**OPERATION MODES**
**VOLTAGE SWITCHING MODE**

The circuit in Figure 6 shows the Si7240 connected in the voltage switching mode. Since  $V_{OUT}$  is the

same polarity as  $V_{REF}$ , this configuration allows single supply operation. Note that the voltage  $V_{REF}$  must always be positive with respect to DGND in order to prevent parasitic transistor turn-on.

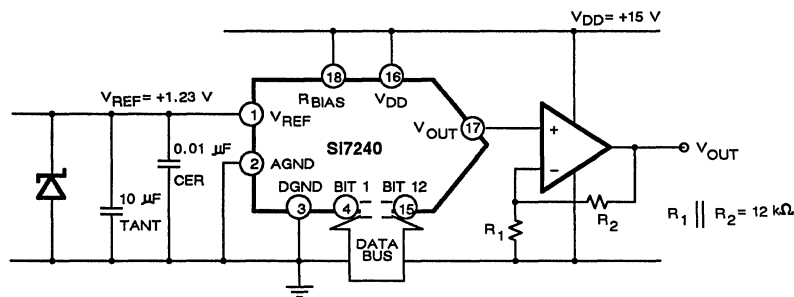


Figure 6. Si7240 in Single Supply Voltage Switching

**OPERATION MODES (Cont'd)**

To maintain linearity, the voltages at  $V_{REF}$  and AGND should remain within 2.0 volts of each other for a  $V_{DD}$  of +15 V. If  $V_{DD}$  is reduced from 15 V or the differential voltage between  $V_{REF}$  and AGND is increased to more than 2.0 volts, the accuracy of the DAC will be degraded. Note that the output voltage range has been extended by using a noninverting gain stage.

The output  $V_{OUT}$  is expressed as:

$$V_{OUT} = V_{REF} (D) \left( \frac{R_1 + R_2}{R_2} \right)$$

Where D is a fractional representation of the digital input word ( $0 \leq D \leq 4095/4096$ ).

Fastest settling can be achieved by using a dual supply op amp.

**VOLTAGE SWITCHING MODE WITH AGND BIAS VOLTAGE**

AGND can be biased above DGND to provide an offset "zero" analog output voltage level. Figure 7 shows this circuit configuration. As in Figure 6, the output voltage range has been extended by using a noninverting gain stage to buffer the DAC.

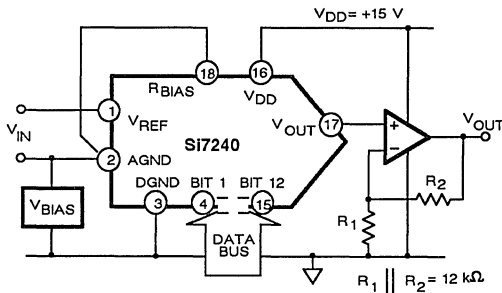


Figure 7. Si7240 in Single Supply Voltage Switching Mode with AGND Bias Voltage

The output voltage  $V_{OUT}$  is expressed as:

$$V_{OUT} = V_{BIAS} \left( \frac{R_1 + R_2}{R_2} \right) + V_{IN} (D) \left( \frac{R_1 + R_2}{R_2} \right)$$

Where  $V_{IN} \leq +2.0$  V, and where D is a fractional representation of the digital input word ( $0 \leq D$

$\leq 4095/4096$ ).

The effect of  $R_{BIAS}$  on total unadjusted error and differential nonlinearity will be the same as reducing  $V_{DD}$  by the amount of the offset.

**VOLTAGE SWITCHING MODE - OFFSET BINARY OPERATION**

Figure 8 shows a circuit used to implement offset binary coding in the voltage switching mode. Mismatch between  $R_1$  and  $R_2$  causes both offset and full scale error, therefore, these resistors must match (to within 0.01%) and track over temperature.

Table 1 shows the digital code vs. output voltage relationship for Figure 8.

**Table 1**  
Offset Binary Code Table for  
Figure 8 with  $R_1 = R_2$

Digital Input	Analog Output
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF} \cdot \left( \frac{2047}{2048} \right)$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 V
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}$

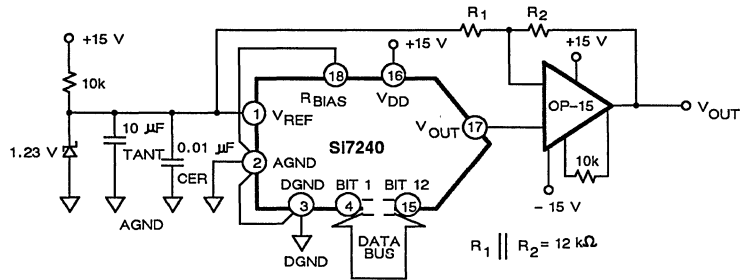


Figure 8. Si7240 in Offset-Binary Voltage-Switching Mode



# Si7533

## CMOS 10-Bit Multiplying DAC

### FEATURES

- Full Four Quadrant Multiplication
- 1/2 LSB INL
- Low Gain Drift (<math>\pm 0.1\%</math> over temp)
- TTL/CMOS Compatible

### BENEFITS

- Allows AC Attenuation Without Biasing
- True 10-Bit Linearity
- Reduced Calibration
- Simplified Logic Interface

### APPLICATIONS

- Programmable Gain Amplifiers
- Digitally Controlled Attenuators And Amplifiers
- Remote Systems
- Motion Control Systems
- Programmable Power Supplies

### DESCRIPTION

The Si7533 is a CMOS multiplying digital-to-analog converter which provides 10 bit accuracy and full four-quadrant multiplication. It is pin- and function-compatible with Analog Devices' AD7533 and AD7520, and is recommended for updating existing AD7520 applications.

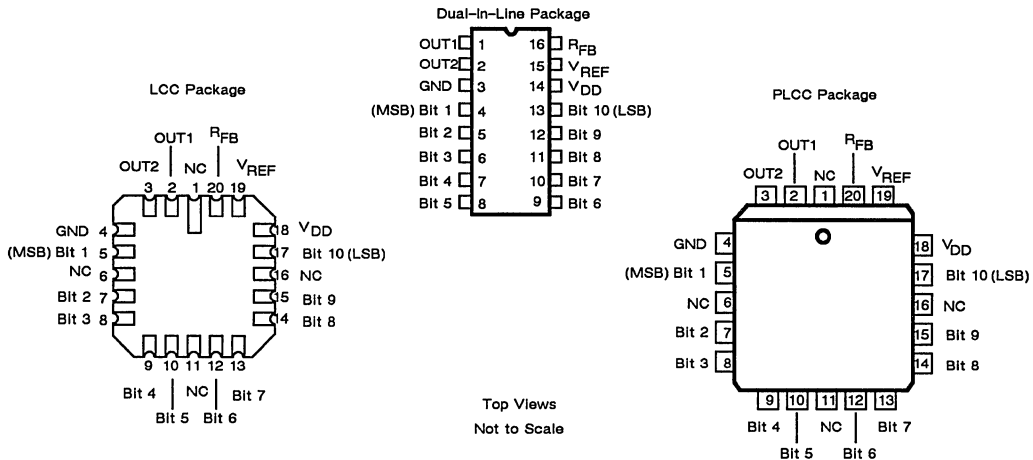
Built on the Siliconix proprietary PolyMOS™ process, the Si7533 uses laser-trimmed thin film resistors to provide full 10-bit linearity, 1.4% maximum gain error, and less than 0.1% gain drift over the full range of temperatures. An epitaxial layer prevents latchup.

Applications include digitally-controlled attenuators, filters, amplifiers and power supplies, disk drive head positioning, servo loops, industrial controllers and avionic systems.

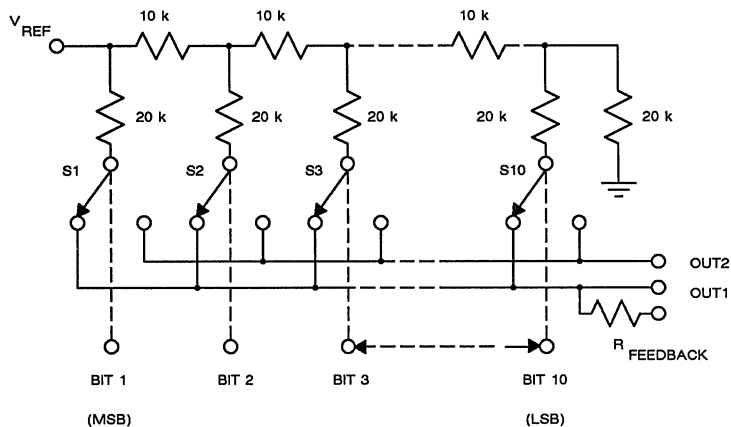
The Si7533 is available in 16-pin Plastic DIP, CerDIP, and Side Braze packages for operation over the commercial, J, K, L suffix (0 to 70°C), industrial, A, B, C suffix (-40 to 85°C) and military, S, T, U suffix (-55 to 125°C) temperature ranges, respectively. For surface mount applications, the Si7533 is available in the 20-pin PLCC for commercial and LCC for military applications.

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### PIN CONFIGURATION



## FUNCTIONAL BLOCK DIAGRAM



## ORDERING INFORMATION

Relative Accuracy $T_{min}$ - $T_{max}$	Temperature Range and Package				
	Plastic		CerDIP	Side Brazed	Ceramic LCC
	DIP	PLCC			
	0 to 70 °C	0 to 70 °C	-40 to 85 °C	-55 to 125 °C	-55 to 125 °C
± 0.05%	SI7533LN	SI7533LP	SI7533CQ	SI7533UD	SI7533UE
± 0.1%	SI7533KN	SI7533KP	SI7533BQ	SI7533TD	SI7533TE
± 0.2%	SI7533JN	SI7533JP	SI7533AQ	SI7533SD	SI7533SE

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND	-0.3 V, +17 V
$V_{REF}$ to GND	±25 V
$V_{RFB}$ to GND	±25 V
Digital Input Voltage to GND	-0.3 V to $V_{DD}$
$V_{OUT1}, V_{OUT2}$ to GND	-0.3 V to $V_{DD}$
Storage Temperature (D, E, Q Suffix)	-65 to 150 °C
(N, P Suffix)	-65 to 125 °C
Operating Temperature (D, E Suffix)	-55 to 125 °C
(Q Suffix)	-40 to 85 °C
(N, P Suffix)	0 to 70 °C

### Power Dissipation (Package)\*

16-Pin Plastic DIP**	470 mW
16-Pin Ceramic Side Brazed***	900 mW
16-Pin CerDIP****	900 mW
20-Pin PLCC****	450 mW

\* All leads welded or soldered to PC Board.

\*\* Derate 6.5 mW/°C above 25°C.

\*\*\* Derate 12 mW/°C above 75°C.

\*\*\*\* Derate 10 mW/°C above 25°C.

## CAUTION

ESD (Electro-Static-Discharge-Sensitive) device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy

electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 15\text{ V}$ , $V_{REF} = 10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier = OP-07		LIMITS				UNIT
				1=25°C 2=125,85,70°C 3=-55,-40,0°C		ALL GRADES		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>ACCURACY</b>								
Resolution	N		1,2,3		10		Bits	
Relative Accuracy <sup>e, h</sup>	INL	J, A, S Grades	1,2,3		-0.2	0.2	% FSR	
		K, B, T Grades	1,2,3		-0.1	0.1		
		L, C, U Grades	1,2,3		-0.05	0.05		
Gain Error <sup>e, h</sup>	$G_{FSE}$	Measured Using Internal $R_{FB}$	1 2,3		-1.4 -1.5	1.4 1.5		
Gain Drift <sup>c, e, h</sup>			1,2,3		-0.1	0.1		
Output Leakage Current	$I_{OUT1(OFF)}$	$V_{REF} = \pm 10\text{ V}$	All Digital Inputs = $V_{IL}$	1 2,3	-50 -200	50 200	nA	
	$I_{OUT2(OFF)}$		All Digital Inputs = $V_{IH}$	1 2,3	-50 -200	50 200		
<b>REFERENCE INPUT</b>								
Reference Input Resistance <sup>f</sup>	$R_{REF}$		1,2,3	10	5	20	k $\Omega$	
<b>LOGIC INPUT</b>								
Input HIGH Voltage	$V_{IH}$		1,2,3		2.4		V	
Input LOW Voltage	$V_{IL}$		1,2,3			0.8		
Input Leakage Current	$I_{IN}$	Digital Inputs = 0 V or $V_{DD}$	1,2,3		-1	1	$\mu\text{A}$	
Input Capacitance <sup>c</sup>	$C_{IN}$		1,2,3				5	pF
<b>SUPPLY</b>								
Power Supply Rejection		$\Delta\text{Gain} / \Delta V_{DD}$ $V_{DD} = 14\text{ to }17\text{ V}$	1 2,3		-0.005 -0.008	0.005 0.008	% per %	
$V_{DD}$ Range <sup>c</sup>	$V_{DD}$	+15 V for Rated Accuracy	1,2,3		5	16	V	
Supply Current	$I_{DD}$	All Digital Inputs $V_{IL}$ or $V_{IH}$	1,2,3			2	mA	

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ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 15\text{ V}$ , $V_{REF} = 10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier = OP-07	LIMITS				UNIT	
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		ALL GRADES			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC ACCURACY</b>								
Feedthrough Error <sup>c, 1</sup> ( $V_{REF}$ to $OUT_1$ )		Digital Inputs = $V_{IL}$ $V_{REF} = \pm 10\text{ V}$ , 100 kHz Sine Wave	1 2,3	1.4 2.8			% FSR	
Output Current Settling Time <sup>c, 9</sup>	$t_s$	To 0.05% of FSR $OUT_1$ Load = 100 $\Omega$	1 2,3			600 800	ns	
Output Capacitance <sup>c</sup>	$C_{OUT}$	Digital Inputs = $V_{IH}$	$OUT_1$	1,2,3			80	pF
			$OUT_2$	1,2,3			40	
		Digital Inputs = $V_{IL}$	$OUT_1$	1,2,3			40	
			$OUT_2$	1,2,3			80	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. FSR = Full Scale Range =  $-(V_{REF})^{(10^{23}/10^{24})}$  in unipolar mode.
- f. Absolute TC for  $R_{REF}$  is approximately -300 ppm/°C.
- g. Digital Inputs =  $V_{IH}$  to  $V_{IL}$  or  $V_{IL}$  to  $V_{IH}$ .
- h. 0.1% FSR = 1 LSB = 1 mV.
- i. Feed through for Side Braze package versions is improved to typically 0.4% FSR.

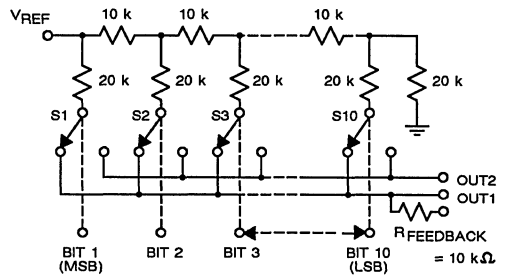
**DETAILED DESCRIPTION**

The Si7533 is a 10-bit multiplying Digital-to-Analog Converter consisting of a highly stable thin film R-2R ladder network and ten single-pole double-throw current steering NMOS analog switches on a monolithic chip. The binary weighted CMOS level shifters provide low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most applications.

The binary weighted currents are switched between the  $OUT_1$  and  $OUT_2$  bus lines, thus maintaining a constant current in each leg of the ladder regardless of switch states.

The input resistance at  $V_{REF}$  (Figure 1) is always equal to the value " $R_{REF}$ " and is the R-2R ladder characteristic resistance. Since  $R_{REF}$  at the  $V_{REF}$  pin is constant, the reference terminal can be driven by a reference voltage or a reference current, be it positive, negative or AC. If a current

source is used, a low TC external feedback resistor RFB is recommended to define the scale factor.



**Figure 1.** Si7533 Functional Diagram (All Inputs HIGH)

Figure 2 illustrates the typical NMOS SPDT switch with its associated CMOS level shifter/driver.

**DETAILED DESCRIPTION (Cont'd)**

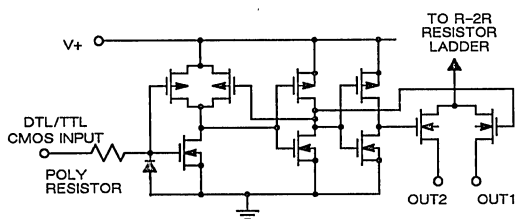


Figure 2. Simplified Schematic Single SPDT Switch

inputs LOW. All reference current is switched to OUT2. The current sources  $I_{LEAKAGE}$  are composed of surface and junction leakages to the substrate. The  $1/1024$  current source represents the constant 1 LSB current drain through the ladder termination resistor. The output capacitance on OUT2 (with all its switches ON) is 80 pF, whereas on OUT1 it is only 40 pF.

The output capacitances are dependent upon the digital input code and vary between the LOW and HIGH values.

Analysis of the circuit for all digital inputs HIGH, as shown in in Figure 4 is similar to Figure 3; however the "ON" switches are now on OUT1, hence the 80 pF at that terminal.

**EQUIVALENT CIRCUIT ANALYSIS**

Figure 3 shows the equivalent circuit for all digital

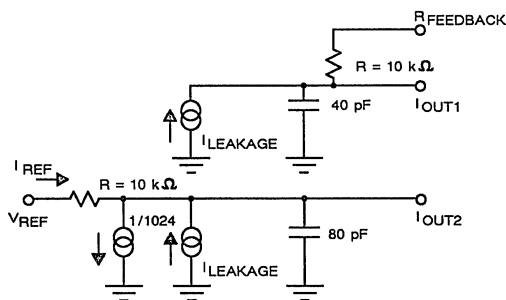


Figure 3. Si7533 Equivalent Circuit (All Inputs LOW)

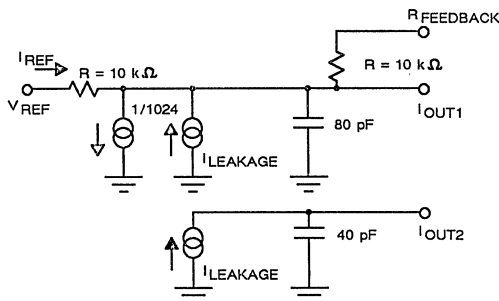


Figure 4. Si7533 Equivalent Circuit (All Inputs HIGH)



**APPLICATIONS**

**APPLICATIONS HINTS**

Static linearity of the Si7533 depends upon the potential of OUT1 and OUT2 (pins 1 and 2) being exactly equal to GND (pin 3). In most applications the DAC is connected to an external output op amp with its non-inverting input tied to ground, which converts its current output into a voltage output signal. The op amp selected should have a low input bias current (typically less than 75 nA) and low drift over the operating temperature range. The

amplifier's input offset voltage should be nulled to less than 10% of 1 LSB. The non-inverting input should be connected directly to GND without the usual input bias current compensation resistor. This resistor can cause variable offsets which would create errors. Ground loops should be avoided by taking all pins going to GND to a common point.

The  $V_{DD}$  power supply should have a low noise level and not have transients greater than +17 V.

APPLICATIONS (Cont'd)

Unused digital inputs must be grounded or taken to  $V_{DD}$ . It is also recommended that all digital inputs be taken to ground via a high value (1 M $\Omega$ ) resistor to prevent the accumulation of static charges whenever the PC board is not connected to the system.

**OUTPUT OFFSET:** CMOS DACs exhibit a code dependent output resistance which can cause a code dependent error voltage at the output of the amplifier. The maximum value of this error is 0.67  $V_{OS}$ , where  $V_{OS}$  is the amplifier input offset voltage.

To maintain monotonicity it is recommended that  $V_{OS}$  be no greater than  $(100 \times 10^{-6}) V_{REF}$  over the operating temperature range. It is also important that  $V_{OS}$  be nulled, either by using the op amp's nulling pins or an external network.

**DIGITAL GLITCHES:** One cause of glitches is capacitive coupling from the digital lines to the OUT1 and OUT2 terminals. This can be minimized by guarding the analog pins of the Si7533 (pins 1, 2, 15, 16) from the digital input pins by a ground track run between pins 2 and 3 and between pins 14 and 15. Note that the analog pins are at one end of the package separated from the digital inputs by  $V_{DD}$  and GND to aid guarding.

**OUTPUT AMPLIFIER:** For low speed applications the AC specifications of the op amp are not critical. In high-speed applications, however, slew rate, settling time, open-loop gain, gain/phase margin specifications of the amplifier should be selected for the desired performance. As mentioned before, the usual bias current compensation resistor at the inverting input of the op amp should not be used. Instead, the amplifier should have a low input bias current over the operating temperature range.

**UNIPOLAR BINARY OPERATION  
(2-QUADRANT MULTIPLICATION)**

Figure 5 shows the circuit configuration required for unipolar binary (2-quadrant multiplication) operation. With a DC voltage or current-reference (positive or negative) applied at pin 15, the circuit is a unipolar Digital-to-Analog converter. With an AC reference this circuit provides 2-quadrant

multiplication (digitally controlled attenuation). The reference input voltage can range between -20 V and +20 V due to the ability of  $V_{REF}$  to exceed  $V_{DD}$ .

Table 1 shows the digital code input analog voltage

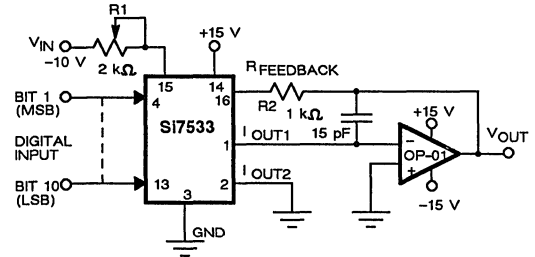


Figure 5. Unipolar Binary Operation  
(2 - Quadrant)

correspondence. R1 provides full-scale trimming (load the DAC with 1111111111, adjust R1 for  $V_{OUT} = -V_{REF}(1023/1024)$ ). Full-scale can also be adjusted by omitting R1 and R2 and trimming the magnitude of  $V_{REF}$ .

TABLE 1.

DIGITAL INPUT MSB    LSB	ANALOG OUTPUT ( $V_{OUT}$ )
1111111111	$-(1023/1024) V_{IN}$
1000000000	$-(512/1024) V_{IN}$
0000000001	$-(1/1024) V_{IN}$
0000000000	0 V

Unipolar Binary Code Table for Circuit  
of Figure 5

**BIPOLAR BINARY OPERATION  
(4-QUADRANT MULTIPLICATION)**

Figure 6 illustrates the recommended circuit for bipolar operation. With a DC reference of either polarity the circuit provides offset binary operation. With an AC reference, the nine LSBs provide digitally controlled attenuation of the reference input while the MSB provides polarity control.

APPLICATIONS (Cont'd)

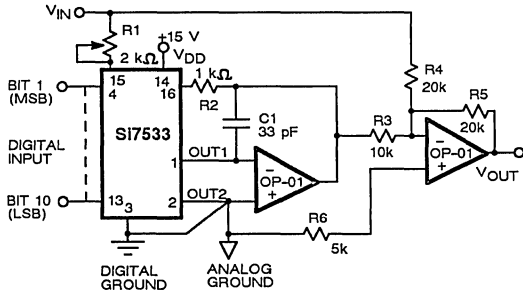


Figure 6. Bipolar Operation  
(4 - Quadrant Multiplication)

With the DAC loaded to 1000000000, adjust R1 for  $V_{OUT} = 0$  V (alternatively, R1 and R2 can be omitted and the ratio of R3 to R4 can be adjusted for  $V_{OUT} = 0$  V). Full-scale trimming can be performed by adjusting  $V_{REF}$  or by adjusting the value of R5.

As in unipolar operation the amplifiers must be chosen for low input offset voltage and low input bias current. The input offset voltage of both amplifiers should be adjusted to less than 0.4 mV and be better than 2 mV over the operating temperature range of interest. R3, R4 and R5 must be matched. Mismatches of R5 to R4 and (2 X R3) cause full-scale error. Mismatch of (2 X R3) to R4 causes both offset and full-scale errors.

Table 2 illustrates the relationship between the offset binary digital codes and the analog output voltage.

TABLE 2.

DIGITAL INPUT MSB    LSB	ANALOG OUTPUT ( $V_{OUT}$ )
11111111	$+(511/512) V_{IN}$
10000000	$+(1/512) V_{IN}$
10000000	0 V
01111111	$-(1/512) V_{IN}$
00000000	$-V_{IN}$

Bipolar Binary Code Table for Circuit  
of Figure 6

SINGLE SUPPLY OPERATION

The circuit of Figure 7 shows the Si7533 connected in a voltage switching configuration. The reference voltage is applied to OUT1 and OUT2 is connected to ground. The DAC output is available at pin 15 ( $V_{REF}$  pin) and has a constant output impedance equal to  $R_{REF}$ . The internal feedback resistor (pin 16) is not used. For better linearity in the voltage switching mode, the Si7240 should be specified.

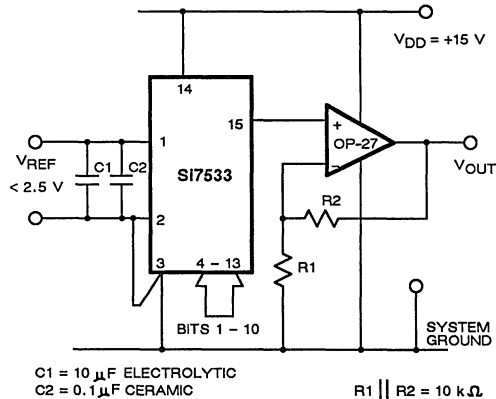


Figure 7. Single Supply Operation  
Using Voltage Switching

The reference voltage must always be positive in the voltage switching mode. If pin 1 goes below -0.3 V an internal diode will be turned on. If not limited a large current will flow and may cause device damage. Since the Si7533 is protected for SCR latch-up, removing the abnormally negative reference voltage will restore normal operation provided the maximum current handling capacity (20 mA) has not been exceeded.

Loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the ability of the reference voltage source to handle the changing load conditions. For this reason bypassing of the reference source is required. To maintain linearity the reference voltage at pin 1 should remain within 2.5 V of GND, for a  $V_{DD} = 15$  V. If  $V_{DD}$  is reduced or the reference voltage increased, the DAC's linearity and differential nonlinearity will be degraded.

# Si7541

## CMOS 12-Bit Multiplying DAC

### FEATURES

- 12-Bit Linearity (INL < 1/2 LSB)
- Four Quadrant Multiplication
- Fast Settling (600 ns)
- Monotonic (DNL < 1/2 LSB)
- TTL/CMOS Compatible

### BENEFITS

- Improves System Absolute Accuracy
- Allows Bipolar Reference Inputs
- Increases Data Throughput
- Closed-Loop Servo Stability
- Simplifies Logic Interfacing

### APPLICATIONS

- ATE Systems
- Digitally Controlled Gain/Attenuation
- Function Generators
- Closed-Loop Servo Systems
- Hybrid/Custom A/D Converters

### DESCRIPTION

The Si7541 is a 12-Bit multiplying digital-to-analog converter which features true 12-bit integral linearity and monotonicity, fast settling time (600 ns), TTL-compatible logic inputs, and low gain drift of 5 ppm/°C (max). The 1/2 LSB differential nonlinearity specification guarantees monotonicity, thus eliminating instability in closed-loop systems.

Multiplying applications for the Si7541 include digitally controlled amplifiers, attenuators, filters and power supplies. The fast settling time makes the Si7541 ideal for high speed data conversion and hybrid or custom A/D converters.

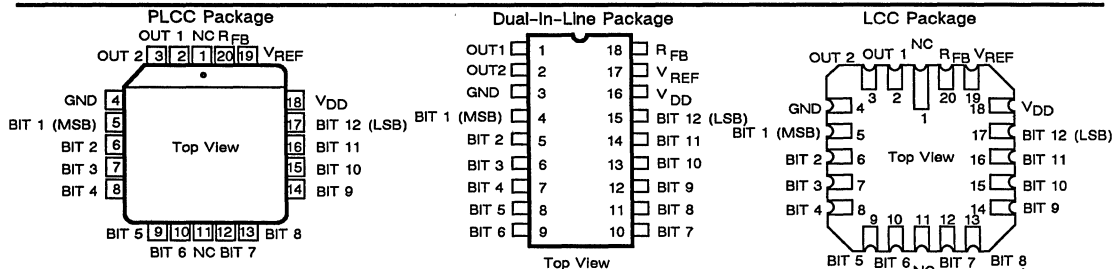
The Si7541 is built using the Siliconix advanced 5-micron CMOS process known as PolyMOS™, allowing fast settling time and low glitch impulse. Highly-stable thin film resistors are included on the

chip for low drift over temperature and time. These are laser-trimmed to achieve 1/2 LSB integral nonlinearity (INL) and reduced gain error. An epitaxial layer prevents latch up.

The Si7541 is available in 18-pin PDIP, CerDIP and side braze DIP packages for commercial, J, K suffix (0 to 70°C), industrial, A, B suffix (-40 to 85°C) and military, S, T suffix (-55 to 125°C) operation, respectively. For surface mount applications, the Si7541 is available in the PLCC-20 (0 to 70°C) and the hermetic LCC-20 (-55 to 125°C). Each package and temperature range is available in two linearity grades.

For more information on the Si7541, please refer to Siliconix Application Note AN87-3.

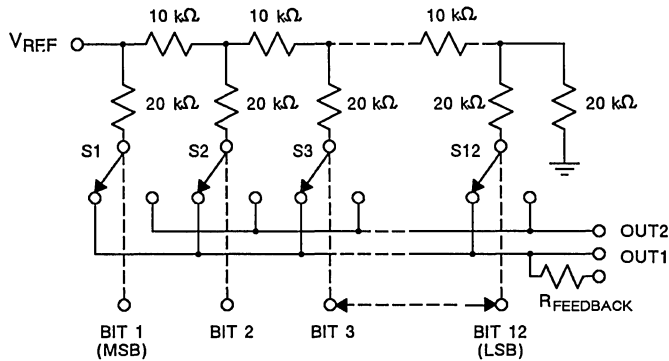
### PIN CONFIGURATION & ORDERING INFORMATION



INL T <sub>min</sub> - T <sub>max</sub> (LSB)	GAIN ERROR T <sub>a</sub> = 25° C (LSB)	TEMPERATURE RANGE AND PACKAGE				
		PLCC 0 to 70°C	PDIP 0 to 70°C	CerDIP -40 to 85°C	SIDE BRAZE -55 to 125°C	LCC -55 to 125°C
± 1	± 12.5	SI7541JP	SI7541JN	SI7541AQ	SI7541SD	SI7541SE
± 1/2	± 12.5	SI7541KP	SI7541KN	SI7541BQ	SI7541TD	SI7541TE



**FUNCTION BLOCK DIAGRAM**



**DEFINITION OF TERMS**

**GAIN ERROR**

Gain error or full-scale error is a measure of the difference between an ideal DAC's and the actual device output. For the Si7541, ideal full-scale output is  $-(4095/4096) \cdot (V_{REF})$ . Gain error is adjustable to zero using external trims as shown in Figures 5 and 6.

**OUTPUT LEAKAGE CURRENT**

This is the current that appears at OUT1 with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

**MULTIPLYING FEEDTHROUGH ERROR**

This is the AC error due to capacitive feedthrough from  $V_{REF}$  to OUT1 with DAC loaded to all 0's.

**OUTPUT CURRENT SETTLING TIME**

This is the time required for the output current of the DAC to settle to within 1/2 LSB into 100  $\Omega$ , and is specified for a zero to full scale digital input change.

**PROPAGATION DELAY**

This is a measure of the internal circuit delay from the time a digital input changes to the point when the analog output at OUT1 reaches 90% of its final value.

**DIGITAL TO ANALOG GLITCH IMPULSE**

This is a measure of the area of the impulse injected to the analog outputs when the digital inputs change state. It is usually specified as the area of the impulse in nV-secs. It is measured with  $V_{REF} = GND$  and an LH0032 as the output op amp, and phase compensation capacitor = 0 pF.

**6**

**ABSOLUTE MAXIMUM RATINGS**

$V_{DD}$ to GND .....	17 V
$V_{REF}$ to GND .....	25 V
$V_{RFB}$ to GND .....	25 V
Digital Input Voltage to GND .....	-0.3 V to $V_{DD}$
$V_{OUT1}$ , $V_{OUT2}$ to GND .....	-0.3 V to $V_{DD}$
Storage Temperature (D, Q, E Suffix) .....	-65 to 150°C
(N, P Suffix) .....	-65 to 125°C

Operating Temperature (S, T Suffix) .....	-55 to 125°C
(A, B Suffix) .....	-40 to 85°C
(J, K Suffix) .....	0 to 70°C

Power Dissipation (Package)*	
N, P Suffixes ** .....	470 mW
D, E, Q Suffixes *** .....	900 mW

- \* All leads welded or soldered to PC board.
- \*\* Derate 6.5 mW/°C above 25°C
- \*\*\* Derate 12 mW/°C above 75°C

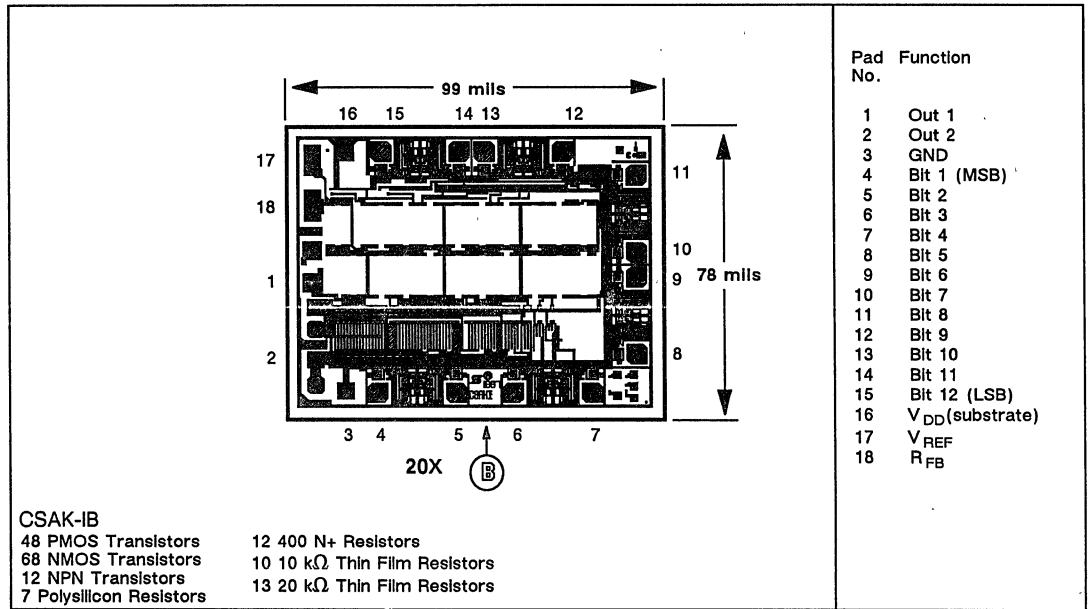
ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = +15 V, V <sub>REF</sub> = +10 V V <sub>OUT1</sub> = V <sub>OUT2</sub> = 0V Output Amplifier: OP-07		LIMITS						UNIT
				1=25°C 2=125,85,70°C 3=-55,-40,0°C		B, K, T GRADE		A, J, S GRADE		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>ACCURACY</b>										
Resolution	N			1,2,3		12		12		LSB
Relative Accuracy (Integral Non-Linearity)	INL	(1LSB = 0.024% of Full Scale)		1,2,3		-1/2	1/2	-1	1	
Differential Nonlinearity	DNL			1,2,3		-1/2	1/2	-1	1	
Gain Error	G <sub>FSE</sub>	Measured Using Internal R <sub>FB</sub>		1 2,3		-12.5 -16.7	12.5 16.7	-12.5 -16.7	12.5 16.7	
Gain Temp Coefficient <sup>c</sup>	TCG <sub>FS</sub>	Δ Gain / Δ Temperature		1,2,3	2	-5	5	-5	5	ppm/°C
Output Leakage Current	I <sub>OUT1</sub>	V <sub>REF</sub> = ±10 V	All Digital Inputs = 0 V	1		-5	5	-5	5	nA
				2,3		B: -10 K: -10 T: -200	10 10 200	A: -10 J: -10 S: -200	10 10 200	
	I <sub>OUT2</sub>		All Digital Inputs = V <sub>DD</sub>	1		-5	5	-5	5	
				2,3		B: -10 K: -10 T: -200	10 10 200	A: -10 J: -10 S: -200	10 10 200	
<b>REFERENCE</b>										
Reference Input Resistance (Pin 17 to GND)	R <sub>REF</sub>			1,2,3	10	7	18	7	18	kΩ
<b>INPUT</b>										
Input HIGH Voltage	V <sub>IH</sub>			1,2,3		2.4		2.4		V
Input LOW Voltage	V <sub>IL</sub>			1,2,3			0.8		0.8	
Input Current	I <sub>IN</sub>			1,2,3		-1	1	-1	1	μA
Input Capacitance <sup>c</sup>	C <sub>IN</sub>	V <sub>IN</sub> = 0 V					8		8	pF
<b>SUPPLY</b>										
Power Supply Rejection	PSRR	Δ Gain / Δ V <sub>DD</sub> , Δ V <sub>DD</sub> = ±5%		1 2,3		-0.01 -0.02	0.01 0.02	-0.01 -0.02	0.01 0.02	%per%
V <sub>DD</sub> Range <sup>e</sup>				1,2,3		5	16	5	16	V

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = +15 V, V <sub>REF</sub> = +10 V V <sub>OUT1</sub> = V <sub>OUT2</sub> = 0V Output Amplifier: OP-07	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		B, K, T GRADE		A, J, S GRADE		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY (Cont'd)</b>									
Supply Current	I <sub>DD</sub>	All Digital Inputs V <sub>IL</sub> or V <sub>IH</sub>	1,2,3			2		2	mA
		All Digital Inputs 0 V or V <sub>DD</sub>	1 2,3			100 500		100 500	μA
<b>DYNAMIC</b>									
Propagation Delay	t <sub>PD</sub>	From 50% of Digital Input to 90% of Final Analog Output OUT1 load = 100Ω C <sub>EXT</sub> = 13 pF Digital Inputs = 0 V to V <sub>DD</sub> or V <sub>DD</sub> to 0V	1	100					ns
Digital-to-Analog Glitch Impulse	I <sub>S</sub>	Output Amplifier: LH0032 V <sub>REF</sub> = 0 V, C <sub>F</sub> = 0 pF Digital Inputs = 0 V to V <sub>DD</sub> or V <sub>DD</sub> to 0V	1	1000					nV-s
Multiplying Feedthrough Error (V <sub>REF</sub> to OUT1)	MF <sub>ER</sub>	V <sub>REF</sub> = 20 V <sub>p-p</sub> , Sinewave @ 10 kHz	1	1					mV p-p
Output Current Settling Time	t <sub>S</sub>	To 0.01% of Full Scale Range OUT1 load = 100Ω C <sub>EXT</sub> = 13 pF Digital Inputs = 0 V to V <sub>DD</sub> or V <sub>DD</sub> to 0V	1	0.6					μs
Output Capacitance <sup>c</sup>	C <sub>OUT1</sub>	Digital Inputs = V <sub>IH</sub> V <sub>IL</sub>	1,2,3			200 70		200 70	pF
	C <sub>OUT2</sub>					70 200		70 200	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Accuracy is not guaranteed over this range.

## DIE TOPOGRAPHY



## CAUTION

ESD (Electro-Static-Discharge-Sensitive) device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy

electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

## DETAILED DESCRIPTION

The Si7541 is a 12-bit multiplying Digital-to-Analog Converter consisting of a highly stable thin film R-2R ladder network and twelve single-pole double-throw current steering NMOS analog switches on a monolithic chip. The binarily weighted CMOS level shifters provide low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most applications.

The binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each leg of the ladder regardless of switch states.

The input resistance at V<sub>REF</sub> (Figure 1) is always equal to the value "R<sub>REF</sub>" and is the R-2R ladder characteristic resistance. Since R<sub>REF</sub> at the V<sub>REF</sub> pin is constant, the reference terminal can be

driven by a reference voltage or a reference current, be it positive, negative or AC. If a current source is used, a low TC external feedback resistor R<sub>FB</sub> is recommended to define the scale factor.

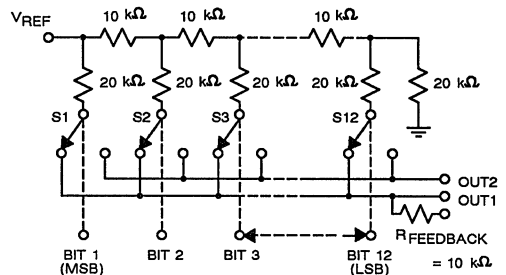
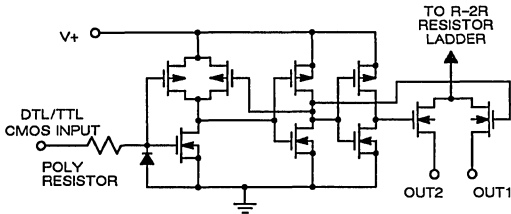


Figure 1. Si7541 Functional Diagram (All Inputs HIGH)

**DETAILED DESCRIPTION**

Figure 2 illustrates the typical NMOS SPDT switch with its associated CMOS level shifter/driver.



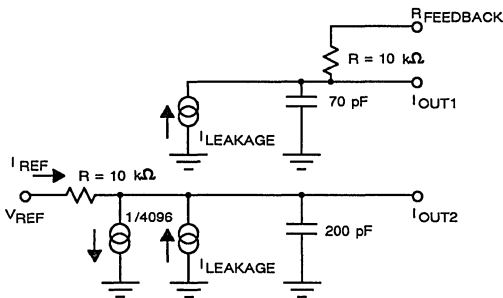
**Figure 2.** Simplified Schematic Single SPDT Switch

**EQUIVALENT CIRCUIT ANALYSIS**

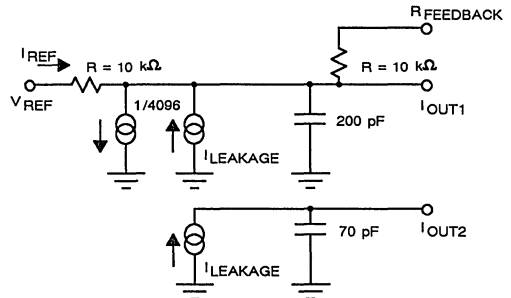
Figure 3 shows the equivalent circuit for all digital inputs LOW. All reference current is switched to OUT2. The current sources  $I_{LEAKAGE}$  are composed of surface and junction leakages to the substrate. The  $1/4096$  current source represents the constant 1 LSB current drain through the ladder termination resistor. The output capacitance on OUT2 (with all its switches ON) is 200 pF, whereas on OUT1 it is only 70 pF.

The output capacitances are dependent upon the digital input code and vary between the LOW and HIGH values.

Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4 is similar to Figure 3; however the "ON" switches are now on OUT1, hence the 200 pF at that terminal.



**Figure 3.** Si7541 Equivalent Circuit (All Inputs LOW)



**Figure 4.** Si7541 Equivalent Circuit (All Inputs HIGH)

**APPLICATIONS**

**APPLICATIONS HINTS**

Static linearity of the Si7541 depends upon the potential of OUT1 and OUT2 (pins 1 and 2) being exactly equal to GND (pin 3). In most applications the DAC is connected to an external output op amp with its non-inverting input tied to ground, which converts its current output into a voltage output signal. The op amp selected should have a low

input bias current (typically less than 75 nA) and low drift over the operating temperature range. The amplifier's input offset voltage should be nulled to less than 10% of 1 LSB (typically less than  $\pm 200\text{ }\mu\text{V}$ ). The non-inverting input should be connected directly to GND without the usual input bias current compensation resistor. This resistor can cause variable offsets which would create

## APPLICATIONS (Cont'd)

errors. Ground loops should be avoided by taking all pins going to GND to a common point.

The  $V_{DD}$  power supply should have a low noise level and not have transients greater than +17 V.

Unused digital inputs must be grounded or taken to  $V_{DD}$ . It is also recommended that all digital inputs be taken to ground via a high value (1 M $\Omega$ ) resistor to prevent the accumulation of static charges whenever the PC board is not connected to the system.

**OUTPUT OFFSET:** CMOS DACs exhibit a code dependent output resistance which can cause a code dependent error voltage at the output of the amplifier. The maximum value of this error is  $0.67 V_{OS}$ , where  $V_{OS}$  is the amplifier input offset voltage.

To maintain monotonicity it is recommended that  $V_{OS}$  be no greater than  $(25 \times 10^{-6}) (V_{REF})$  over the operating temperature range. It is also important that  $V_{OS}$  be nulled, either by using the op amp's nulling pins or an external network.

**DIGITAL GLITCHES:** One cause of glitches is capacitive coupling from the digital lines to the OUT1 and OUT2 terminals. This can be minimized by guarding the analog pins of the Si7541 (pins 1, 2, 17, 18) from the digital input pins by a ground track run between pins 16 and 17. Note that the analog pins are at one end of the package separated from the digital inputs by  $V_{DD}$  and GND to aid guarding.

**TEMPERATURE COEFFICIENTS:** The Gain temperature coefficient of the Si7541 has a maximum value of 5 ppm/ $^{\circ}$ C and a typical of 2 ppm/ $^{\circ}$ C. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100 $^{\circ}$ C temperature range. When trim resistors R1 and R2 are required to adjust full scale range, low temperature coefficient (approximately 50 ppm/ $^{\circ}$ C) resistors or trim-pots should be selected.

**OUTPUT AMPLIFIER:** For low speed applications the AC specifications of the op amp are not critical. In high-speed applications, however, slew rate, settling time, open-loop gain, gain/phase margin specifications of the amplifier should be selected for the desired performance. As mentioned before, the usual bias current compensation resistor at the inverting input of the op amp should not be used.

Instead, the amplifier should have a low input bias current over the operating temperature range.

### UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 5 shows the circuit configuration required for unipolar binary (2-quadrant multiplication) operation. With a DC voltage or current-reference (positive or negative) applied at pin 17, the circuit is a unipolar Digital-to-Analog converter. With an AC reference this circuit provides 2-quadrant multiplication (digitally controlled attenuation). The reference input voltage can range between -20 V and +20 V due to the ability of  $V_{REF}$  to exceed  $V_{DD}$ .

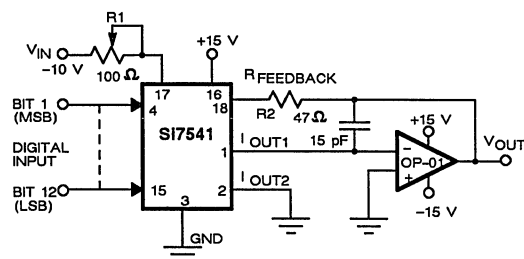


Figure 5. Unipolar Binary Operation  
(2 - Quadrant)

Table 1 shows the digital code input analog voltage correspondence. R1 provides full-scale trimming (load the DAC with 1111 1111 1111, adjust R1 for  $V_{OUT} = -V_{REF} (4095/4096)$ ). Full-scale can also be adjusted by omitting R1 and R2 and trimming the magnitude of  $V_{REF}$ .

TABLE 1

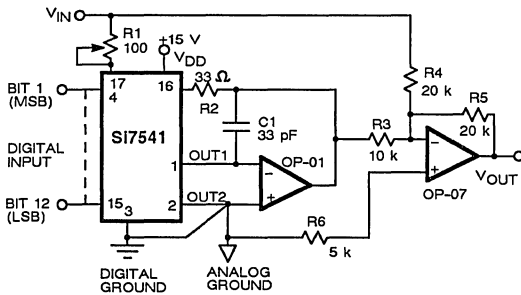
DIGITAL INPUT MSB    LSB	ANALOG OUTPUT ( $V_{OUT}$ )
1111 1111 1111	$-(4095/4096) V_{IN}$
1000 0000 0000	$-(2048/4096) V_{IN}$
0000 0000 0001	$-(1/4096) V_{IN}$
0000 0000 0000	0 V

Unipolar Binary Code Table for Circuit  
of Figure 5

**APPLICATIONS (Cont'd)**

**BIPOLAR BINARY OPERATION  
(4-QUADRANT MULTIPLICATION)**

Figure 6 illustrates the recommended circuit for bipolar operation. With a DC reference of either polarity the circuit provides offset binary operation. With an AC reference, the eleven LSBs provide digitally controlled attenuation of the reference input while the MSB provides polarity control.



**Figure 6.** Bipolar Operation  
(4 - Quadrant Multiplication)

With the DAC loaded to 1000 0000 0000, adjust R1 for  $V_{OUT} = 0 V$  (alternatively, R1 and R2 can be omitted and the ratio of R3 to R4 can be adjusted for  $V_{OUT} = 0 V$ ). Full-scale trimming can be performed by adjusting  $V_{REF}$  or by adjusting the value of R5.

As in unipolar operation the amplifiers must be chosen for low input offset voltage and low input bias current. The input offset voltage of both amplifiers should be adjusted to less than 0.1 mV and be better than 0.5 mV over the operating temperature range of interest. R3, R4 and R5 must be matched. Mismatches of R5 to R4 and  $(2 \times R3)$  cause full-scale error. Mismatch of  $(2 \times R3)$  to R4 causes both offset and full-scale errors.

Table 2 illustrates the relationship between the offset binary digital codes and the analog output voltage.

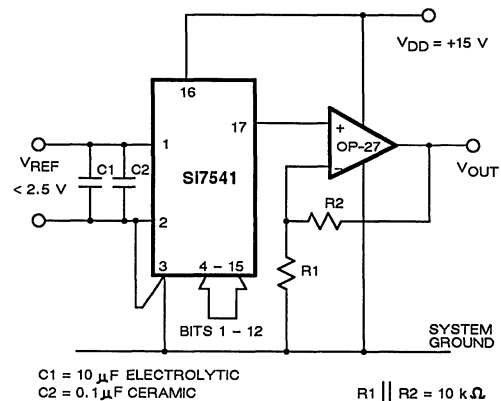
**TABLE 2**

DIGITAL INPUT MSB LSB	ANALOG OUTPUT ( $V_{OUT}$ )
1111 1111 1111	$+(2047/2048) V_{IN}$
1000 0000 0001	$+(1/2048) V_{IN}$
1000 0000 0000	0 V
0111 1111 1111	$-(1/2048)V$
0000 0000 0000	$-V_{IN}$

**Bipolar Binary Code Table for Circuit  
of Figure 6**

**SINGLE SUPPLY OPERATION**

The circuit of Figure 7 shows the Si7541 connected in a voltage switching configuration. The reference voltage is applied to OUT1 and OUT2 is connected to ground. The DAC output is available at pin 17 ( $V_{REF}$  pin) and has a constant output impedance equal to  $R_{REF}$ . The internal feedback resistor (pin 18) is not used. For better linearity in the voltage switching mode, the Si7240 should be specified.



**Figure 7.** Single Supply Operation  
Using Voltage Switching

The reference voltage must always be positive in the voltage switching mode. If pin 1 goes below  $-0.3 V$  an internal diode will be turned on. If not limited a large current will flow and may cause device damage. Since the Si7541 is protected for SCR latch-up, removing the abnormally negative reference voltage will restore normal operation

## APPLICATIONS (Cont'd)

provided the maximum current handling capacity (20 mA) has not been exceeded.

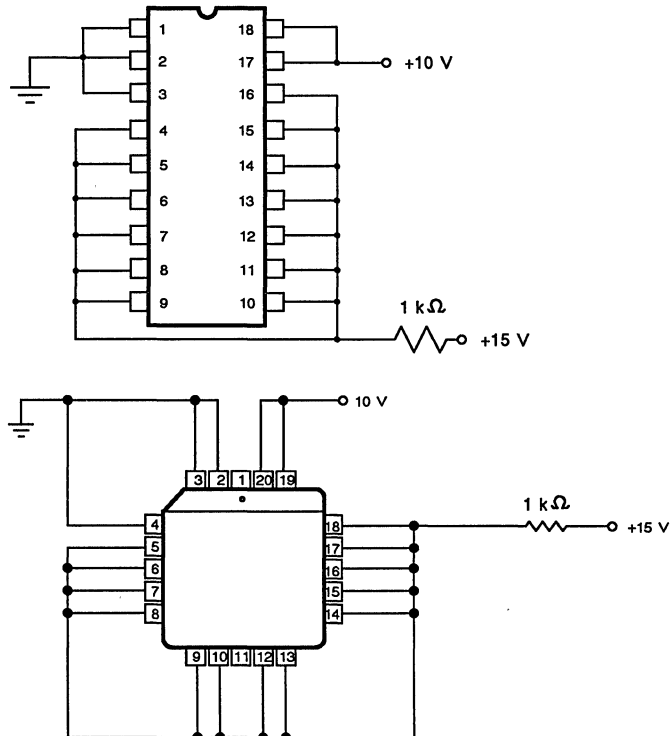
Loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the ability of the reference voltage source to handle the changing load

conditions. For this reason bypassing of the reference source is required. To maintain linearity the reference voltage at pin 1 should remain within 2.5 V of GND, for a  $V_{DD} = 15$  V. If  $V_{DD}$  is reduced or the reference voltage increased, the DAC's linearity and differential nonlinearity will be degraded.

## PIN DESCRIPTION

PIN NUMBER	DESCRIPTION	PIN NUMBER	DESCRIPTION
1	Current OUTPUT 1	10	Digital Input (Bit 7)
2	Current OUTPUT 2	11	Digital Input (Bit 8)
3	Digital Ground	12	Digital Input (Bit 9)
4	Digital Input (Bit 1) (MSB)	13	Digital Input (Bit 10)
5	Digital Input (Bit 2)	14	Digital Input (Bit 11)
6	Digital Input (Bit 3)	15	Digital Input (Bit 12) (LSB)
7	Digital Input (Bit 4)	16	Positive Power Supply
8	Digital Input (Bit 5)	17	Reference Input Voltage
9	Digital Input (Bit 6)	18	Internal Feedback Resistor

## BURN-IN CIRCUITS





# Si7541A

## CMOS 12-Bit Multiplying DAC

### FEATURES

- 12-Bit Linearity (INL < 1/2 LSB)
- Four Quadrant Multiplication
- Gain Error < 1 LSB
- Fast Settling (300 ns typ.)
- Monotonic (DNL < 1/2 LSB)
- TTL/CMOS Compatible

### BENEFITS

- Improves System Absolute Accuracy
- Allows Bipolar Reference Inputs
- Reduces Trims
- Increases Data Throughput
- No Seek Errors in Servos
- Simplifies Logic Interfacing

### APPLICATIONS

- ATE Systems
- Digitally Controlled Gain/Attenuation
- Function Generators
- Closed-Loop Servo Systems
- Hybrid/Custom A/D Converters

### DESCRIPTION

The Si7541A is a 12-Bit multiplying digital-to-analog converter which features true 12-bit integral linearity and monotonicity, low gain error (1 LSB), fast settling time (300 ns typ.), TTL-compatible logic inputs, and low gain drift of 5 ppm/°C. The low gain error reduces trim requirements in the system, and the 1/2 LSB differential nonlinearity specification guarantees monotonicity, thus eliminating instability in closed-loop systems.

Multiplying applications for the Si7541A include digitally controlled amplifiers, attenuators, filters and power supplies. The fast settling time makes the Si7541A ideal for high speed data conversion and hybrid or custom A/D converters.

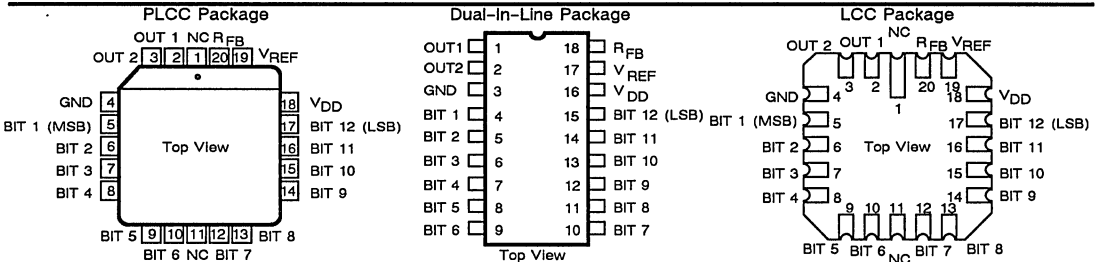
The Si7541A is built using the Siliconix advanced 5-micron CMOS process known as PolyMOS™, allowing fast settling time and low glitch impulse.

Highly-stable thin film resistors are included on the chip for low drift over temperature and time. These are laser-trimmed to achieve 1/2 LSB integral nonlinearity (INL) and reduced gain error. The epitaxial layer prevents latch up.

The Si7541A is available in 18-pin PDIP, CerDIP and side braze DIP packages for commercial, J, K suffix (0 to 70°C), industrial, A, B suffix (-40 to 85°C) and military, S, T suffix (-55 to 125°C) operation, respectively. For surface mount applications, the Si7541A is available in the PLCC-20 (0 to 70°C) and the hermetic LCC-20 (-55 to 125°C). Each package and temperature range is available in two linearity grades.

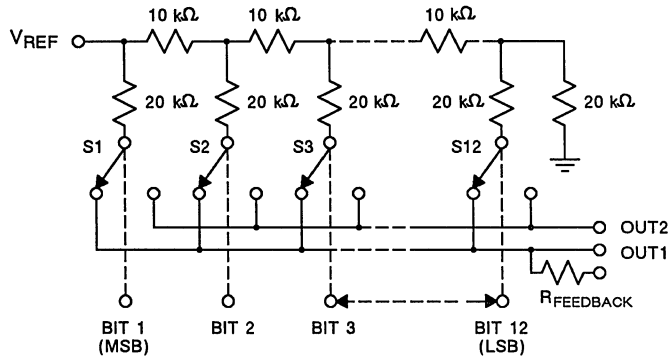
For more information on the Si7541A, please refer to Siliconix Application Note AN87-3.

### PIN CONFIGURATION & ORDERING INFORMATION



INL T <sub>min</sub> - T <sub>max</sub> (LSB)	GAIN ERROR T <sub>a</sub> = 25° C (LSB)	TEMPERATURE RANGE AND PACKAGE				
		PLCC 0 to 70°C	PDIP 0 to 70°C	CerDIP -40 to 85°C	SIDE BRAZE -55 to 125°C	LCC -55 to 125°C
± 1	± 6	SI7541AJP	SI7541AJN	SI7541AAQ	SI7541ASD	SI7541ASE
± 1/2	± 1	SI7541AKP	SI7541AKN	SI7541ABQ	SI7541ATD	SI7541ATE

## FUNCTION BLOCK DIAGRAM



## DEFINITION OF TERMS

**MULTIPLYING DAC**

Digital-to-Analog Converters (DACs) are devices that convert digital data into analog values. A multiplying DAC is a device capable of handling variable reference sources. Its output is the product of two variables: the number represented by the digital input code and the analog reference voltage.

**RESOLUTION**

Resolution indicates the number of digital input bits. A 12-bit DAC resolves the full-scale range (FSR) into  $2^{12} = 4096$  states.

**LSB**

Value of the Least Significant Bit. For example, a 12-bit unipolar converter has a 1 LSB step value equal to  $V_{REF}/2^{12}$  or  $V_{REF}/4096$  (Volts).

**RELATIVE ACCURACY**

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the DAC transfer function. It is measured after adjusting for zero and full scale errors and is expressed in % of full scale range or (sub)multiples of 1 LSB.

**DIFFERENTIAL NONLINEARITY**

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB max over the operating temperature range ensures monotonicity.

**GAIN ERROR**

Gain error or full-scale error is a measure of the difference between an ideal DAC's and the actual

device output. For the Si7541A, ideal full-scale output is  $-(4095/4096) \cdot (V_{REF})$ . Gain error is adjustable to zero using external trims as shown in Figures 5 and 6.

**OUTPUT LEAKAGE CURRENT**

This is the current that appears at OUT1 with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

**MULTIPLYING FEEDTHROUGH ERROR**

This is the AC error due to capacitive feedthrough from  $V_{REF}$  to OUT1 with DAC loaded to all 0's.

**OUTPUT CURRENT SETTLING TIME**

This is the time required for the output current of the DAC to settle to within 1/2 LSB into 100  $\Omega$ , and is specified for a zero to full scale digital input change.

**PROPAGATION DELAY**

This is a measure of the internal circuit delay from the time a digital input changes to the point when the analog output at OUT1 reaches 90% of its final value.

**DIGITAL TO ANALOG GLITCH IMPULSE**

This is a measure of the area of the impulse injected to the analog outputs when the digital inputs change state. It is usually specified as the area of the impulse in nV-secs. It is measured with  $V_{REF} = \text{GND}$  and an LH0032 as the output op amp, and phase compensation capacitor = 0 pF.

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to GND	17 V
$V_{REF}$ to GND	25 V
$V_{RFB}$ to GND	25 V
Digital Input Voltage to GND	-0.3 V to $V_{DD}$
$V_{OUT1}$ , $V_{OUT2}$ to GND	-0.3 V to $V_{DD}$
Storage Temperature (D, Q, E Suffix)	-65 to 150°C
(N, P Suffix)	-65 to 125°C

Operating Temperature (S, T Suffix)	-55 to 125°C
(A, B Suffix)	-40 to 85°C
(J, K Suffix)	0 to 70°C

### Power Dissipation (Package)\*

N, P Suffixes **	470 mW
D, E, Q Suffixes ***	900 mW

\* All leads welded or soldered to PC board.

\*\* Derate 6.5 mW/°C above 25°C

\*\*\* Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = +15\text{ V}$ , $V_{REF} = +10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier: OP-07	LIMITS								UNIT
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		B, K, T GRADE		A, J, S GRADE		TEMP	TYP <sup>d</sup>	
			MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>ACCURACY</b>											
Resolution	N		1,2,3		12		12				LSB
Relative Accuracy (Integral Non-Linearity)	INL	(1LSB = 0.024% of Full Scale)	1,2,3		-1/2	1/2	-1	1			
Differential Nonlinearity	DNL		1,2,3		-1/2	1/2	-1	1			
Gain Error	$G_{FSE}$	Measured Using Internal $R_{FB}$	1 2,3		-1 -3	1 3	-6 -8	6 8			
Gain Temp Coefficient <sup>c</sup>	$TCG_{FS}$	$\Delta$ Gain / $\Delta$ Temperature	1,2,3	2	-5	5	-5	5		ppm/°C	
Output Leakage Current	$I_{OUT1}$	$V_{REF} = \pm 10\text{ V}$	All Digital Inputs = 0 V	1		-5	5	-5	5	nA	
				2,3		B: -10 K: -10 T: -200	10 10 200	A: -10 J: -10 S: -200	10 10 200		
	$I_{OUT2}$		All Digital Inputs = $V_{DD}$	1		-5	5	-5	5		
				2,3		B: -10 K: -10 T: -200	10 10 200	A: -10 J: -10 S: -200	10 10 200		
<b>REFERENCE</b>											
Reference Input Resistance (Pin 17 to GND)	$R_{REF}$		1,2,3	10	7	18	7	18		k $\Omega$	
<b>INPUT</b>											
Input HIGH Voltage	$V_{IH}$		1,2,3		2.4		2.4			V	
Input LOW Voltage	$V_{IL}$		1,2,3			0.8		0.8		V	

**6**

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = +15\text{ V}$ , $V_{REF} = +10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier: OP-07	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		B, K, T GRADE		A, J, S GRADE		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT (Cont'd)</b>									
Input Current	$I_{IN}$		1,2,3		-1	1	-1	1	$\mu\text{A}$
Input Capacitance <sup>c</sup>	$C_{IN}$	$V_{IN} = 0\text{ V}$				8		8	pF
<b>SUPPLY</b>									
Power Supply Rejection	PSRR	$\Delta\text{Gain} / \Delta V_{DD}$ , $\Delta V_{DD} = \pm 5\%$	1 2,3		-0.01 -0.02	0.01 0.02	-0.01 -0.02	0.01 0.02	%per%
$V_{DD}$ Range <sup>e</sup>			1,2,3		5	16	5	16	V
Supply Current	$I_{DD}$	All Digital Inputs $V_{IL}$ or $V_{IH}$	1,2,3			2		2	mA
		All Digital Inputs 0 V or $V_{DD}$	1 2,3			100 500		100 500	$\mu\text{A}$
<b>DYNAMIC</b>									
Propagation Delay	$t_{PD}$	From 50% of Digital Input to 90% of Final Analog Output OUT1 load = 100 $\Omega$ $C_{EXT} = 13\text{ pF}$ Digital Inputs = 0 V to $V_{DD}$ or $V_{DD}$ to 0V	1	100					ns
Digital-to-Analog Glitch Impulse	$I_S$	Output Amplifier: LH0032 $V_{REF} = 0\text{ V}$ , $C_F = 0\text{ pF}$ Digital Inputs = 0 V to $V_{DD}$ or $V_{DD}$ to 0V	1	1000					nV-s
Multiplying Feedthrough Error ( $V_{REF}$ to OUT1)	MFER	$V_{REF} = 20\text{ V}_{p-p}$ , Sinewave @ 10 kHz	1	1					mV p-p
Output Current Settling Time	$t_S$	To 0.01% of Full Scale Range OUT1 load = 100 $\Omega$ $C_{EXT} = 13\text{ pF}$ Digital Inputs = 0 V to $V_{DD}$ or $V_{DD}$ to 0V	1	0.3					$\mu\text{s}$
Output Capacitance <sup>c</sup>	$C_{OUT1}$	Digital Inputs = $V_{IH}$ $V_{IL}$	1,2,3			200 70		200 70	pF
	$C_{OUT2}$					70 200		70 200	

## NOTES:

a. Refer to PROCESS OPTION FLOWCHART for additional information.

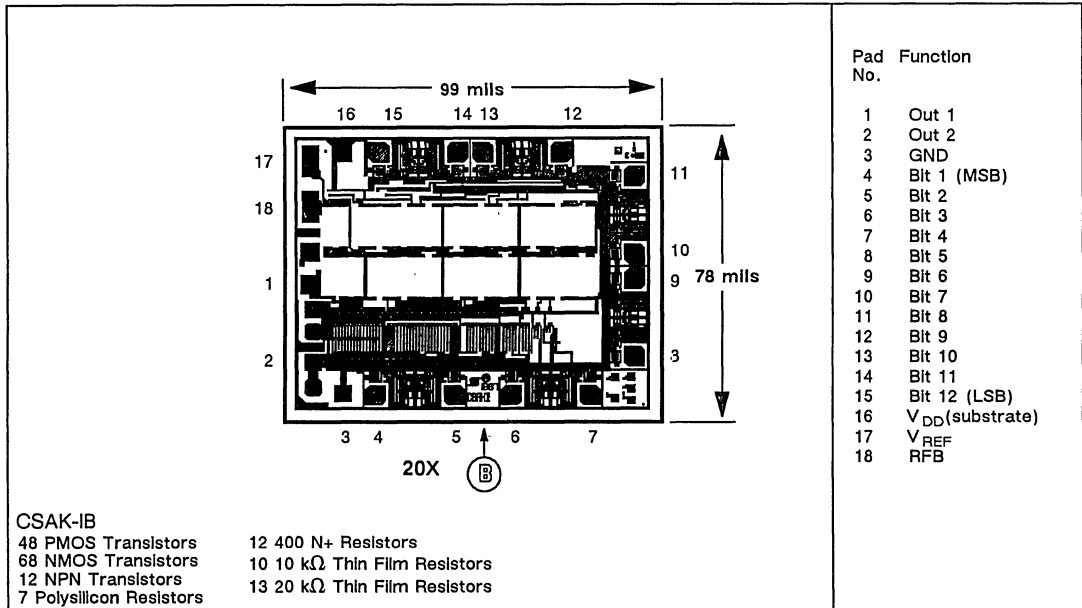
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

c. Guaranteed by design, not subject to production test.

d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

e. Accuracy is not guaranteed over this range.

**DIE TOPOGRAPHY**



**CAUTION**

ESDS (Electro-Static-Discharge-Sensitive) device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy

electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

**6**

**DETAILED DESCRIPTION**

The Si7541A is a 12-bit multiplying Digital-to-Analog Converter consisting of a highly stable thin film R-2R ladder network and twelve single-pole double-throw current steering NMOS analog switches on a monolithic chip. The binary weighted CMOS level shifters provide low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most applications.

The binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each leg of the ladder regardless of switch states.

The input resistance at V<sub>REF</sub> (Figure 1) is always equal to the value "R<sub>REF</sub>" and is the R-2R ladder characteristic resistance. Since R<sub>REF</sub> at the V<sub>REF</sub> pin is constant, the reference terminal can be

driven by a reference voltage or a reference current, be it positive, negative or AC. If a current source is used, a low TC external feedback resistor RFB is recommended to define the scale factor.

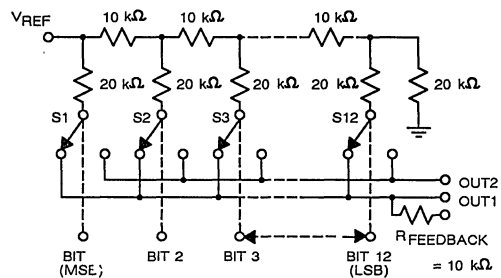


Figure 1. Si7541A Functional Diagram (All Inputs HIGH)

## DETAILED DESCRIPTION

Figure 2 illustrates the typical NMOS SPDT switch with its associated CMOS level shifter/driver.

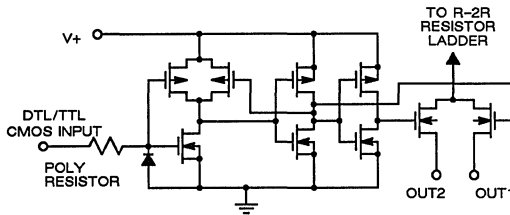


Figure 2. Simplified Schematic Single SPDT Switch

## EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for all digital inputs LOW. All reference current is switched to OUT2. The current sources  $I_{LEAKAGE}$  are composed of surface and junction leakages to the substrate. The  $1/4096$  current source represents the constant 1 LSB current drain through the ladder termination resistor. The output capacitance on OUT2 (with all its switches ON) is 200 pF, whereas on OUT1 it is only 70 pF.

The output capacitances are dependent upon the digital input code and vary between the LOW and HIGH values.

Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4 is similar to Figure 3; however the "ON" switches are now on OUT1, hence the 200 pF at that terminal.

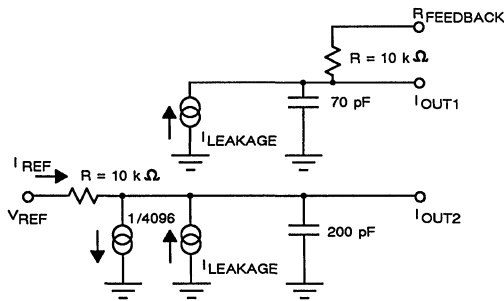


Figure 3. Si7541A Equivalent Circuit (All Inputs LOW)

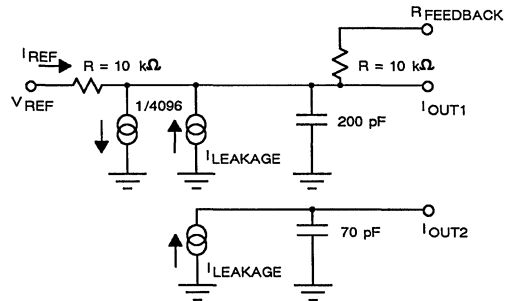


Figure 4. Si7541A Equivalent Circuit (All Inputs HIGH)

## APPLICATIONS

### APPLICATIONS HINTS

Static linearity of the Si7541A depends upon the potential of OUT1 and OUT2 (pins 1 and 2) being exactly equal to GND (pin 3). In most applications the DAC is connected to an external output op amp with its non-inverting input tied to ground, which converts its current output into a voltage output signal. The op amp selected should have a low

input bias current (typically less than 75 nA) and low drift over the operating temperature range. The amplifier's input offset voltage should be nulled to less than 10% of 1 LSB (typically less than  $\pm 200\text{ }\mu\text{V}$ ). The non-inverting input should be connected directly to GND without the usual input bias current compensation resistor. This resistor can cause variable offsets which would create

## APPLICATIONS (Cont'd)

errors. Ground loops should be avoided by taking all pins going to GND to a common point.

The  $V_{DD}$  power supply should have a low noise level and not have transients greater than +17 V.

Unused digital inputs must be grounded or taken to  $V_{DD}$ . It is also recommended that all digital inputs be taken to ground via a high value (1 M $\Omega$ ) resistor to prevent the accumulation of static charges whenever the PC board is not connected to the system.

**OUTPUT OFFSET:** CMOS DACs exhibit a code dependent output resistance which can cause a code dependent error voltage at the output of the amplifier. The maximum value of this error is 0.67  $V_{OS}$ , where  $V_{OS}$  is the amplifier input offset voltage.

To maintain monotonicity it is recommended that  $V_{OS}$  be no greater than  $(25 \times 10^{-6}) (V_{REF})$  over the operating temperature range. It is also important that  $V_{OS}$  be nulled, either by using the op amp's nulling pins or an external network.

**DIGITAL GLITCHES:** One cause of glitches is capacitive coupling from the digital lines to the OUT1 and OUT2 terminals. This can be minimized by guarding the analog pins of the Si7541A (pins 1, 2, 17, 18) from the digital input pins by a ground track run between pins 2 and 3 and between pins 16 and 17. Note that the analog pins are at one end of the package separated from the digital inputs by  $V_{DD}$  and GND to aid guarding.

**TEMPERATURE COEFFICIENTS:** The Gain temperature coefficient of the Si7541A has a maximum value of 5 ppm/ $^{\circ}$ C and a typical of 2 ppm/ $^{\circ}$ C This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100 $^{\circ}$ C temperature range. When trim resistors R1 and R2 are required to adjust full scale range, low temperature coefficient (approximately 50 ppm/ $^{\circ}$ C) resistors or trim-pots should be selected.

**OUTPUT AMPLIFIER:** For low speed applications the AC specifications of the op amp are not critical. In high-speed applications, however, slew rate, settling time, open-loop gain, gain/phase margin specifications of the amplifier should be selected for the desired performance. As mentioned before, the usual bias current compensation resistor at the inverting input of the op amp should not be used.

Instead, the amplifier should have a low input bias current over the operating temperature range.

### UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 5 shows the circuit configuration required for unipolar binary (2-quadrant multiplication) operation. With a DC voltage or current-reference (positive or negative) applied at pin 17, the circuit is a unipolar Digital-to-Analog converter. With an AC reference this circuit provides 2-quadrant multiplication (digitally controlled attenuation). The reference input voltage can range between -20 V and +20 V due to the ability of  $V_{REF}$  to exceed  $V_{DD}$ .

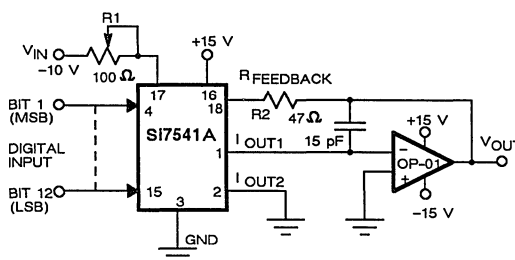


Figure 5. Unipolar Binary Operation  
(2 - Quadrant)

Table 1 shows the digital code input analog voltage correspondence. R1 provides full-scale trimming (load the DAC with 1111 1111 1111, adjust R1 for  $V_{OUT} = -V_{REF}$ ). Full-scale can also be adjusted by omitting R1 and R2 and trimming the magnitude of  $V_{REF}$ .

TABLE 1

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT ( $V_{OUT}$ )
1111	1111 1111	$-(4095/4096) V_{IN}$
1000	0000 0000	$-(2048/4096) V_{IN}$
0000	0000 0001	$-(1/4096) V_{IN}$
0000	0000 0000	0 V

Unipolar Binary Code Table for Circuit  
of Figure 5

## APPLICATIONS (Cont'd)

### BIPOLAR BINARY OPERATION (4-QUADRANT MULTIPLICATION)

Figure 6 illustrates the recommended circuit for bipolar operation. With a DC reference of either polarity the circuit provides offset binary operation. With an AC reference, the eleven LSBs provide digitally controlled attenuation of the reference input while the MSB provides polarity control.

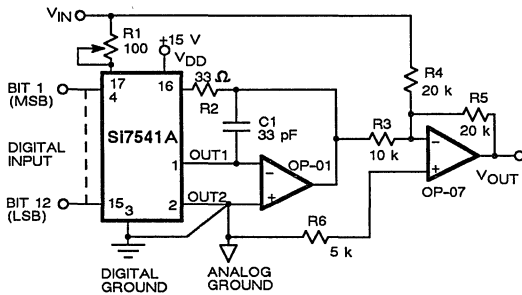


Figure 6. Bipolar Operation  
(4 - Quadrant Multiplication)

With the DAC loaded to 1000 0000 0000, adjust R1 for  $V_{OUT} = 0$  V (alternatively, R1 and R2 can be omitted and the ratio of R3 to R4 can be adjusted for  $V_{OUT} = 0$  V). Full-scale trimming can be performed by adjusting  $V_{REF}$  or by adjusting the value of R5.

As in unipolar operation the amplifiers must be chosen for low input offset voltage and low input bias current. The input offset voltage of both amplifiers should be adjusted to less than 0.1 mV and be better than 0.5 mV over the operating temperature range of interest. R3, R4 and R5 must be matched. Mismatches of R5 to R4 and  $(2 \times R3)$  cause full-scale error. Mismatch of  $(2 \times R3)$  to R4 causes both offset and full-scale errors.

Table 2 illustrates the relationship between the offset binary digital codes and the analog output voltage.

TABLE 2

DIGITAL INPUT MSB      LSB	ANALOG OUTPUT ( $V_{OUT}$ )
1111 1111 1111	$+(2047/2048) V_{IN}$
1000 0000 0001	$+(1/2048) V_{IN}$
1000 0000 0000	0 V
0111 1111 1111	$-(1/2048)V$
0000 0000 0000	$-V_{IN}$

Bipolar Binary Code Table for Circuit of Figure 6

### SINGLE SUPPLY OPERATION

The circuit of Figure 7 shows the Si7541A connected in a voltage switching configuration. The reference voltage is applied to OUT1 and OUT2 is connected to ground. The DAC output is available at pin 17 ( $V_{REF}$  pin) and has a constant output impedance equal to  $R_{REF}$ . The internal feedback resistor (pin 18) is not used. For better linearity in the voltage switching mode, the Si7240 should be specified.

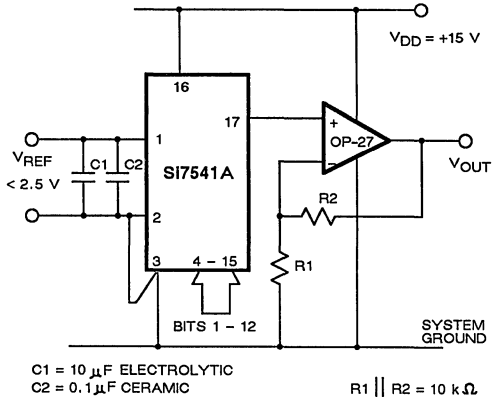


Figure 7. Single Supply Operation  
Using Voltage Switching

The reference voltage must always be positive in the voltage switching mode. If pin 1 goes below -0.3 V an internal diode will be turned on. If not limited a large current will flow and may cause device damage. Since the Si7541A is protected for SCR latch-up, removing the abnormally negative reference voltage will restore normal operation



## APPLICATIONS (Cont'd)

provided the maximum current handling capacity (20 mA) has not been exceeded.

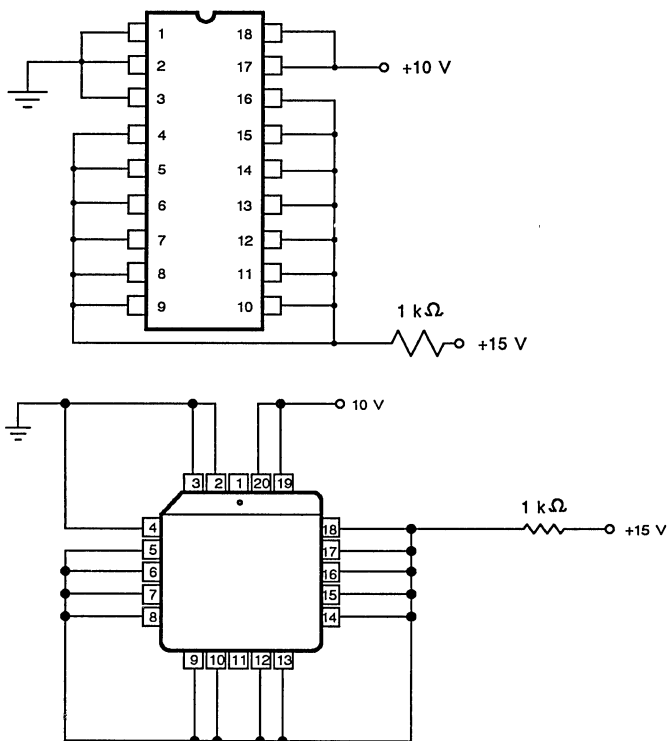
Loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the ability of the reference voltage source to handle the changing load

conditions. For this reason bypassing of the reference source is required. To maintain linearity the reference voltage at pin 1 should remain within 2.5 V of GND, for a  $V_{DD} = 15$  V. If  $V_{DD}$  is reduced or the reference voltage increased, the DAC's linearity and differential nonlinearity will be degraded.

## PIN DESCRIPTION (DIP)

PIN NUMBER	DESCRIPTION	PIN NUMBER	DESCRIPTION
1	Current OUTPUT 1	10	Digital Input (Bit 7)
2	Current OUTPUT 2	11	Digital Input (Bit 8)
3	Digital Ground	12	Digital Input (Bit 9)
4	Digital Input (Bit 1) (MSB)	13	Digital Input (Bit 10)
5	Digital Input (Bit 2)	14	Digital Input (Bit 11)
6	Digital Input (Bit 3)	15	Digital Input (Bit 12) (LSB)
7	Digital Input (Bit 4)	16	Positive Power Supply
8	Digital Input (Bit 5)	17	Reference Input Voltage
9	Digital Input (Bit 6)	18	Internal Feedback Resistor

## BURN-IN CIRCUITS



# Microprocessor-Compatible 12-Bit CMOS Multiplying DAC

## FEATURES

- Double-Buffered 4-Bit TTL-Compatible Latches
- True 12-Bit Linearity (INL < 1/2 LSB)
- Low Gain Drift: (5 ppm/°C max)
- Full 4-quadrant Multiplication
- Single +5 Volt Supply Operation

## BENEFITS

- Simplified Microprocessor Interface
- Improved System Accuracy
- Reduced Calibration Requirements
- Allows AC Attenuation Without Biasing
- Reduced Power Consumption

## APPLICATIONS

- 4 and 8-Bit Microprocessor Controlled Systems
- ATE
- Instrumentation
- Digitally-Controlled Attenuators
- Avionics

## DESCRIPTION

The Si7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

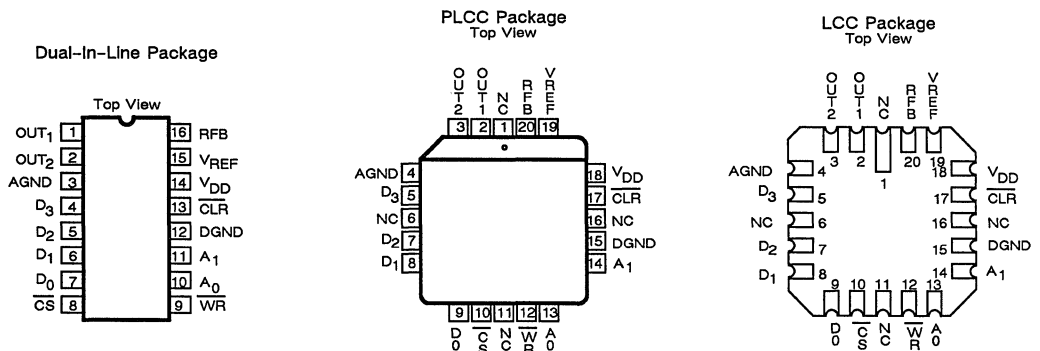
The Si7542 consists of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A Clear input allows the DAC register to be easily reset to all zeros when powering up the device.

The Si7542 is manufactured using the Siliconix

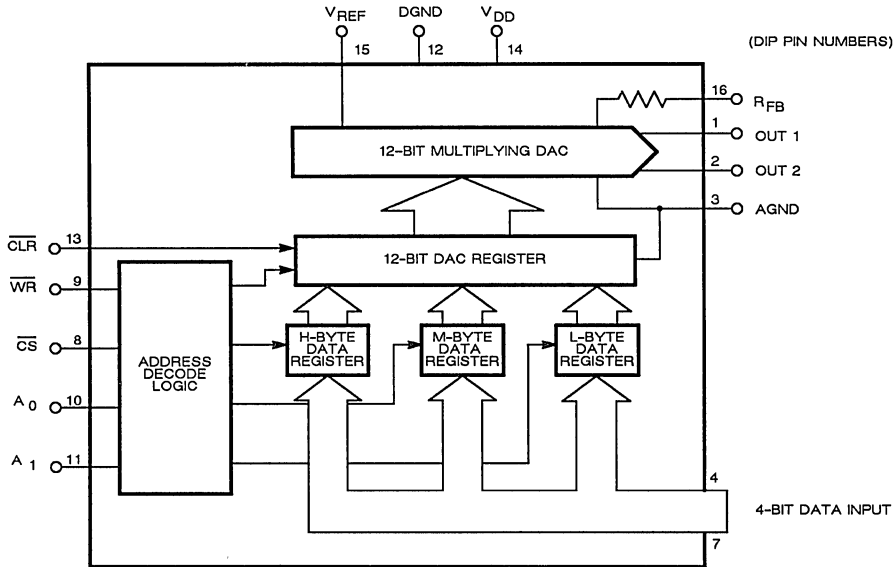
PolyMOS™ process with thin film resistors, which are laser trimmed for high accuracy. Multiplying capability, 12-bit linearity, low power dissipation, +5 V operation, small size and easy  $\mu$ P interface make the Si7542 ideal for many instrumentation, industrial control and avionics applications. An epitaxial layer prevents latchup.

The Si7542 is available in the following packages and temperature ranges: 16-pin plastic DIP and PLCC-20 for commercial, J, K suffix (0 to 70°C) operation, 16-pin CerDIP for industrial, A, B suffix (-40 to 85°C) operation, 16-pin Side Braze and LCC-20 for military, S, T suffix (-55 to 125°C) operation.

## PIN CONFIGURATION



**FUNCTIONAL BLOCK DIAGRAM**



**ORDERING INFORMATION**

INL T <sub>min</sub> - T <sub>max</sub> (LSB)	GAIN ERROR T <sub>a</sub> = 25°C (LSB)	TEMPERATURE RANGE AND PACKAGE				
		PLASTIC 0 to 70°C	PLCC-20 0 to 70°C	CerDIP -40 to 85°C	SIDE BRAZE -55 to 125°C	LCC-20 -55 to 125°C
± 1	± 12.3	SI7542JN	SI7542JP	SI7542AQ	SI7542SD	SI7542SE
± 1/2	± 12.3	SI7542KN	SI7542KP	SI7542BQ	SI7542TD	SI7542TE
± 1/2	± 1	SI7542GKN	SI7542GKP	SI7542GBQ	SI7542GTD	SI7542GTE

**6**

**ABSOLUTE MAXIMUM RATINGS\***

V<sub>DD</sub> to AGND ..... -0.3 V, +17 V  
 V<sub>DD</sub> to DGND ..... -0.3 V, +17 V  
 V<sub>REF</sub> to AGND ..... ±25 V  
 V<sub>RFB</sub> to AGND ..... ±25 V  
 Digital Input Voltage to DGND ..... -0.3 V, +15.3 V  
 V<sub>OUT1</sub>, V<sub>OUT2</sub> to AGND ..... -0.3 V, +15.3 V  
 AGND to DGND ..... -0.3 V to V<sub>DD</sub>  
 DGND to AGND ..... -0.3 V to V<sub>DD</sub>  
 Storage Temperature ..... -65 to 150°C  
 Operating Temperature:  
 (N, P Suffix) ..... 0 to 70°C  
 (Q Suffix) ..... -40 to 85°C

(D, E Suffix) ..... -55 to 125°C

Power Dissipation (Package)\*\*  
 16-Pin Plastic DIP\*\*\* ..... 470 mW  
 16-Pin Ceramic Side Braze\*\*\*\* ..... 900 mW  
 20-Pin Plastic Leaded Chip Carrier ..... 450 mW  
 20-Pin LCC\*\*\*\* ..... 900 mW

\* Stress ratings only. Exposure to absolute max rating conditions for extended periods may affect device reliability.

\*\* All leads welded or soldered to PC Board.

\*\*\* Derate 6.5 mW/°C above 25°C.

\*\*\*\* Derate 12 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = +5\text{ V}$ , $V_{REF} = +10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier: OP-07		LIMITS				UNIT
				1=25°C		ALL GRADES EXCEPT AS NOTED		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>ACCURACY</b>								
Resolution	N			1,2,3		12		Bits
Relative Accuracy (Integral Non-Linearity)	INL	(1LSB = 0.024% of Full Scale)	All Other Grades	1,2,3		-0.5	0.5	LSB
			A, J, S Grades	1,2,3		-1	1	
Differential Nonlinearity	DNL	Monotonic to 12-Bits		1,2,3		-1	1	LSB
		A, J, S Grades		1,2,3		-2	2	
Gain Error <sup>e</sup>	$G_{FSE}$	GB, GK, GT Grades		1 2,3		-1 -2	1 2	LSB
		J, K Grades		1 2,3		-12.3 -13.5	12.3 13.5	
		A, B, S, T Grades		1 2,3		-12.3 -14.5	12.3 14.5	
Gain Temp Coefficient <sup>e</sup>	$TC_{GFS}$	$\Delta\text{Gain} / \Delta\text{Temperature}$		1,2,3	2	-5	5	ppm/ °C
Power Supply Rejection	PSRR	$\Delta\text{Gain} / \Delta V_{DD}$ $V_{DD} = \pm 5\%$		1 2,3		-0.005 -0.01	0.005 0.01	% per %
Output Leakage Current	$I_{OUT1}$ , $I_{OUT2}$	DAC Loaded with All Zeros: $I_{OUT1}$ DAC Loaded with All Ones: $I_{OUT2}$		1 2,3		-1 -200	1 200	nA
		J, K, GK Grades		1 2,3		-1 -10	1 10	
<b>DYNAMIC</b>								
Current Settling Time <sup>c, f</sup>	$t_s$			1,2,3			2	$\mu\text{s}$
Multiplying Feedthrough Error <sup>c, g</sup>	FT	$V_{REF} = \pm 10\text{ V}$ 10 kHz Sine Wave		1,2,3			2.5	mV <sub>p-p</sub>
Output Capacitance <sup>c</sup>	$C_{OUT1}$	DAC Loaded to All Zeros		1,2,3			70	pF
		DAC Loaded to All Ones		1,2,3			200	
	$C_{OUT2}$	DAC Loaded to All Zeros		1,2,3			200	
		DAC Loaded to All Ones		1,2,3			70	

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = +5\text{ V}$ , $V_{REF} = +10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier: OP-07	LIMITS				UNIT	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>REFERENCE</b>								
Reference Input Resistance	$R_{REF}$		1,2,3	10	8	25	k $\Omega$	
<b>LOGIC INPUTS</b>								
Logic HIGH Voltage	$V_{IH}$		1,2,3		3		V	
Logic LOW Voltage	$V_{IL}$		1,2,3			0.8		
Input Current	$I_{IN}$	$V_{IN} = 0\text{ V}$ or $V_{DD}$	1,2,3	0.001	-1	1	$\mu\text{A}$	
Input Capacitance <sup>e</sup>	$C_{IN}$	$V_{IN} = 0\text{ V}$	1,2,3			8	pF	
<b>TIMING <sup>h</sup></b>								
WRITE Pulse Width	$t_{WR}$	See Timing Diagram (Figure 7)	1,2,3	120	220		ns	
Address to WRITE Hold Time	$t_{AWH}$		1,2,3	50	65			
Chip Select to WRITE Hold Time	$t_{CWH}$		1,2,3	50	100			
CLEAR Pulse	$t_{CLR}$		1,2,3	200	300			
Chip Select to WRITE Setup Time	Byte Loading $t_{CWS}$		1,2,3	60	130			
Address Valid to WRITE Setup Time			$t_{AWS}$	1,2,3	80	180		
Data Setup Time			$t_{DS}$	1,2,3	50	65		
Data Hold Time			$t_{DH}$	1,2,3	50	65		
Chip Select to WRITE Setup Time	DAC Loading $t_{CWS}$		1,2,3	60	150			
Address Valid to WRITE Setup Time			$t_{AWS}$	1,2,3	120	240		
<b>SUPPLY</b>								
Supply Voltage	$V_{DD}$	5 V $\pm$ 5% for Specified Performance	1,2,3		4.5	16.5	V	
Supply Current	$I_{DD}$	Digital Inputs = $V_{IH}$ or $V_{IL}$	1,2,3			2.5	mA	

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**ELECTRICAL CHARACTERISTICS<sup>a</sup> (Cont'd.)**


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**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Gain error is measured using internal  $R_{FB}$  only. Gain error can be trimmed to zero using circuits of Figures 5 and 6.
- f. Measured to  $1/2$  LSB. OUT1 Load =  $100 \Omega$ , DAC output measured from falling edge of WR.
- g. Feedthrough error may be reduced by connecting the metal lid on the side braze package to DGND.
- h. Sample tested at  $25^\circ\text{C}$  to ensure compliance.

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**CAUTION**


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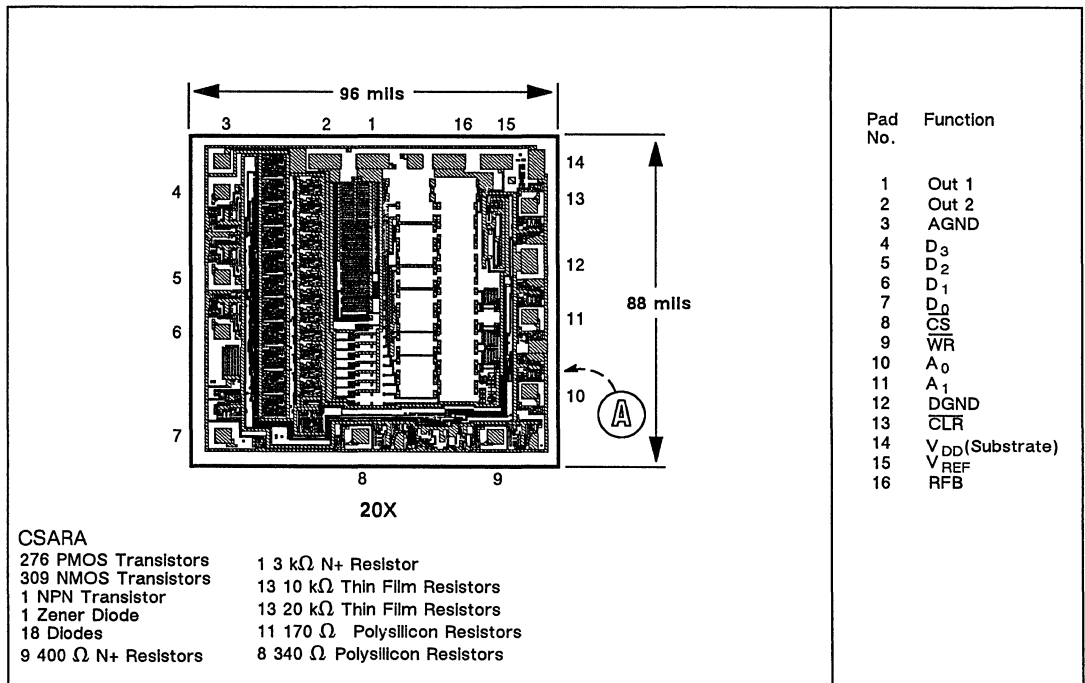
ESDS (Electro-Static-Discharge-Sensitive) device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy

electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

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**DIE TOPOGRAPHY**


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**DEFINITION OF TERMS**

**RELATIVE ACCURACY**

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1 LSB.

**DIFFERENTIAL NONLINEARITY**

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB max over the operating temperature range insures monotonicity.

**GAIN ERROR**

Gain error or full-scale error is a measure of the difference between an ideal DAC's and the actual device output. For the Si7542, ideal full-scale output is  $-(4095/4096) \cdot (V_{REF})$ . Gain error is adjustable to zero using external trims as shown in Figures 5 and 6.

**OUTPUT LEAKAGE CURRENT**

Current which appears at OUT1 with the DAC register loaded to all 0's or at OUT2 with the DAC register loaded to all 1's.

**MULTIPLYING FEEDTHROUGH ERROR**

AC error due to capacitive feedthrough from  $V_{REF}$  terminal to OUT1 with DAC register loaded to all 0's.

**DETAILED DESCRIPTION**

**GENERAL CIRCUIT INFORMATION**

The Si7542, a 12-bit multiplying D/A converter, consists of a highly stable thin-film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used, that is, the binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

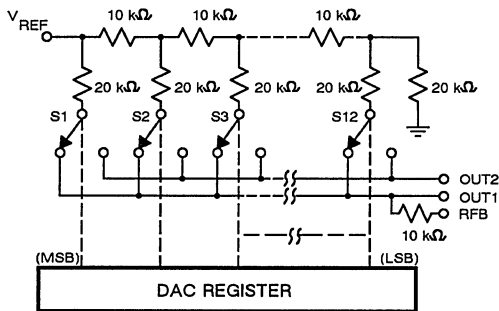


Figure 1. Si7542 Functional Diagram (All Inputs HIGH)

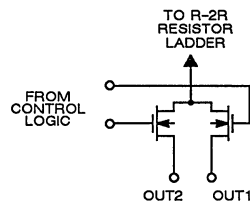


Figure 2. Simplified Schematic, Single SPDT Switch

One of the current switches is shown in Figure 2. The input resistance at  $V_{REF}$  (Figure 1) is always equal to  $R_{LDR}$  ( $R_{LDR}$  is the R-2R ladder characteristic resistance and is equal to value " $R_{REF}$ "). Since  $R_{REF}$  at the  $V_{REF}$  pin is constant, the reference terminal can be driven by a reference voltage or a reference current, AC or DC, of positive or negative polarity. (If a current source is used, a low temperature coefficient external RFB is recommended to define scale factor.)

## DETAILED DESCRIPTION (Cont'd)

### EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In Figure 3 with all digital inputs LOW, the reference current is switched to OUT2. The current source  $I_{LEAKAGE}$  is composed of surface and junction leakages to the substrate, while the  $1/4096$  current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200 pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 70 pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 200 pF at that terminal.

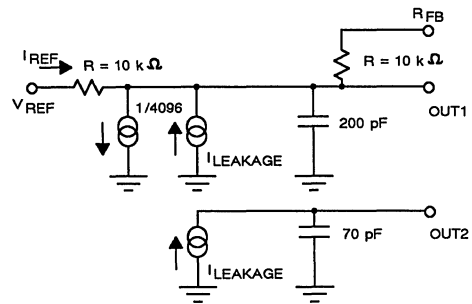


Figure 4. Si7542 Equivalent Circuit (All Inputs HIGH)

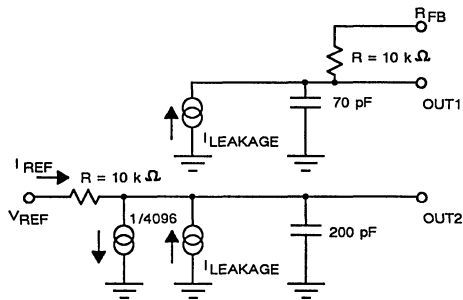


Figure 3. Si7542 Equivalent Circuit (All Inputs LOW)

## APPLICATIONS

### UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 5 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a DC reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an AC reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 1.

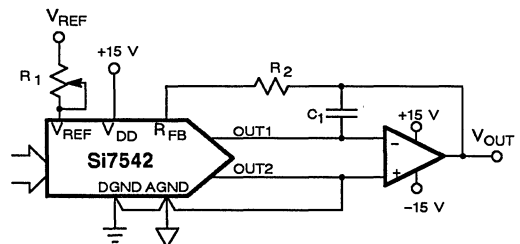


Figure 5. Unipolar Binary Operation (2 - Quadrant)



**APPLICATIONS (Cont'd)**

TABLE 1.

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT (V <sub>OUT</sub> )
1111	1111 1111	$-(4095/4096) V_{REF}$
1000	0000 0000	$-(1/2) V_{REF}$
0000	0000 0001	$-(1/4096) V_{REF}$
0000	0000 0000	0 V

Unipolar Binary Code Table for Circuit of Figure 5

R1 provides full scale trim capability, i.e. load the DAC register to 1111 1111 1111, adjust R1 for  $V_{OUT} = (4095/4096) (-V_{REF})$ . Alternatively, full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25 pF) may be required for stability when using a high speed amplifier. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and the output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide  $V_{OS} < 10\%$  of the voltage resolution at  $V_{OUT}$ . Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at  $V_{OUT}$  equal to  $I_B$  times  $R_{FB}$ ;  $R_{FB}$  is nominally 10 kΩ).

**BIPOLAR OPERATION  
(4-QUADRANT MULTIPLICATION)**

Figure 6 and Table 2 illustrate the circuitry and code relationship for bipolar operation. With a DC reference (positive or negative polarity) the circuit provides offset binary operation. With an AC reference, the eleven LSBs provide digitally controlled attenuation of the AC reference while the MSB provides polarity control.

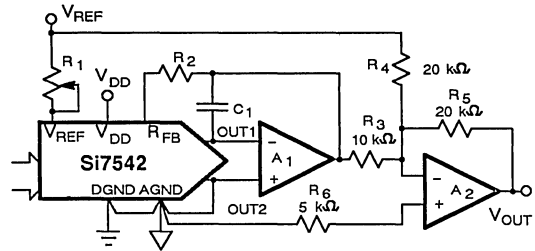


Figure 6. Bipolar Operation (4 - Quadrant Multiplication)

TABLE 2.

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT (V <sub>OUT</sub> )
1111	1111 1111	$+(2047/2048) V_{REF}$
1000	0000 0001	$+(1/2048) V_{REF}$
1000	0000 0000	0 V
0111	1111 1111	$-(1/2048) V_{REF}$
0000	0000 0000	$-V_{REF}$

Bipolar Binary Code Table for Circuit of Figure 6

With the DAC register loaded to 1000 0000 0000, adjust R1 for  $V_{OUT} = 0$  V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for  $V_{OUT} = 0$  V). Full scale trimming can be accomplished by adjusting the amplitude of  $V_{REF}$  or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low  $V_{OS}$  and low  $I_B$ . R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10 pF to 25 pF) may be required for stability.

**INTERFACE LOGIC INFORMATION**

The Si7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown in Figure 8. CS is the decoded device address, and is derived by decoding the three higher order address bits. A0 and A1 are the operation address, and are decoded internally in the Si7542 to point to the desired loading operation (i.e., load high byte,

## APPLICATIONS (Cont'd)

middle byte, low byte or DAC register). Table 3 shows the Si7542 truth table.

All data loading operations are identical to the write cycle of a RAM as shown in Figure 7.

Additionally, the  $\overline{\text{CLR}}$  input allows the Si7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the Si7542 in a unipolar mode (Figure 5), a  $\overline{\text{CLEAR}}$  causes the DAC output to assume 0 V. In the bipolar mode (Figure 6), a  $\overline{\text{CLEAR}}$  causes the DAC output to go to  $-\text{V}_{\text{REF}}$ .

### IN SUMMARY:

1. The Si7542 DAC register can be asynchronously cleared with the  $\overline{\text{CLR}}$  input.
2. Each Si7542 requires four locations in memory.
3. Performing any of the four basic loading operations (i.e., load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) is accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

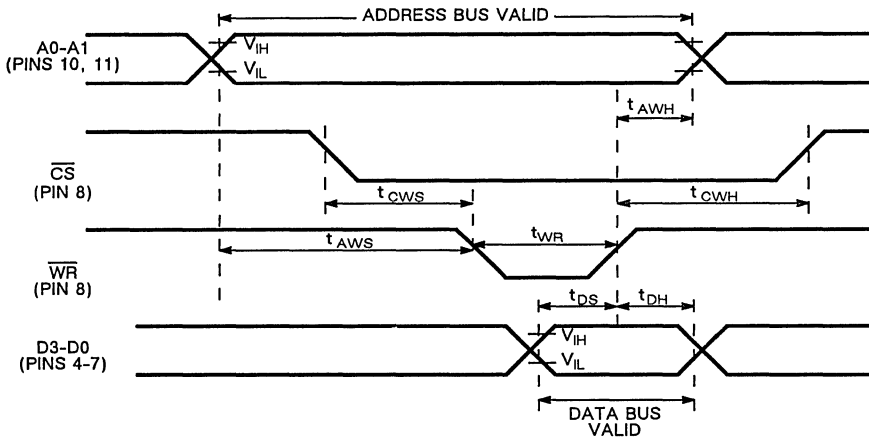
TABLE 3. Si7542 Truth Table

Si7542 Control Inputs <sup>1</sup>					Si7542 Operation
A1	A0	$\overline{\text{CS}}$	$\overline{\text{WR}}^{2,3}$	$\overline{\text{CLR}}$	
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000
X	X	1	X	1	No Operation Device Not Selected
0	0	0	$\uparrow$	1	Load LOW-Byte <sup>4</sup> Data Register
0	1	0	$\uparrow$	1	Load MIDDLE-Byte <sup>4</sup> Data Register
1	0	0	$\uparrow$	1	Load HIGH-Byte <sup>4</sup> Data Register
1	1	0	$\uparrow$	1	Load 12-Bit DAC Register with Data in LOW-Byte, MIDDLE-Byte and HIGH-Byte Data Registers

#### Notes:

1. 1 Indicates logic HIGH, 0 indicates logic LOW, X indicates don't care.
2. This control signal is level triggered.
3.  $\uparrow$  indicates register latches are transparent when  $\overline{\text{WR}} = 0$ , data are stored on edge shown.
4. (MSB) XXXX    XXXX    XXXX (LSB)  
          HIGH-    MIDDLE-    LOW-  
          Byte    Byte    Byte

**APPLICATIONS (Cont'd)**



NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS  $\frac{V_{IH} + V_{IL}}{2}$

Figure 7. Si7542 Timing Diagram

**APPLICATION HINTS**

The Si7542 is a precision 12-bit multiplying DAC designed for system interface. To ensure system performance consistent with Si7542 specifications, careful attention must be given to the following:

- 1. Ground Management:** Voltage differences between the Si7542 AGND and DGND cause loss of accuracy. (DC voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output.) The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the Si7542. In more complex systems where the AGND-DGND connection is at a distant place, it is recommended that diodes be connected in inverse parallel between the Si7542 AGND and DGND pins (1N914 or equivalent).
- 2. Output Amplifier Offset:** CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output which depends on  $V_{OS}$  ( $V_{OS}$  is amplifier input offset voltage). This differential nonlinearity term adds to the R-2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier  $V_{OS}$

be no greater than 10% of the DAC's output resolution over the temperature range of interest (output resolution =  $V_{REF}/4096$ ).

- 3. High Frequency Considerations:** Si7542 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0 dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
- 4. Gain Temperature Coefficients:** The gain temperature coefficient of the Si7542 has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to gain shifts of 2.0 LSBs and 0.82 LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 5 and 6 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:

## APPLICATION HINTS (Cont'd)

$$\text{T. C. Contribution due to R1} = - \frac{R1}{R_{REF}} (\gamma_1 + 300)$$

$$\text{T. C. Contribution due to R2} = + \frac{R2}{R_{REF}} (\gamma_2 + 300)$$

Where  $\gamma_1$  and  $\gamma_2$  are the temperature coefficients in ppm/°C of R1 and R2 respectively and  $R_{REF}$  is the DAC input  $R_{REF}$  resistance at the  $V_{REF}$  terminal. For high quality wire-wound resistors and trimming potentiometers  $\gamma$  is of the the order of 50 ppm/°C. It will be seen that if R1 and R2 are small compared with  $R_{REF}$  their contribution to gain temperature coefficient will also be small. For the

standard Si7542 gain error specification of  $\pm 12.3$  LSBs it is recommended that  $R1 = 120 \Omega$  and  $R2 = 60 \Omega$ . With  $\gamma = 50$ , these values result in an overall maximum gain error temperature coefficient of:

$$5 \text{ ppm/}^\circ\text{C} + \frac{60 \Omega}{10 \text{ k}\Omega} (50 + 300) = 6.5 \text{ ppm/}^\circ\text{C}$$

However, if the Si7542GTD is used which has a specified gain error of  $\pm 1$  LSB, then with  $R1 = 10 \Omega$  and  $R2 = 5 \Omega$  the maximum gain temperature coefficient is increased by only 0.17 ppm/°C. Where possible R1 should be a select-on-test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases.

## INTERFACING

## Si7542 INTERFACE TO MC6800

A typical 6800 system configuration is shown in Figure 8. Since the Si7542 contains four registers, each Si7542 is assigned four locations in memory. A0 and A1 provide the operational addresses and are decoded internally to point to the desired register. Register loading is accomplished by executing a memory WRITE instruction to one of the

four addresses. Table 4 gives a sample loading subroutine.

Choosing an arbitrary start address of 7542, locations 7558, 7559 and 755A select the low, middle and high byte registers respectively while address 755B selects the 12-bit DAC register. The 12-bit data to be passed to the subroutine is stored in 4-bit bytes in the lower halves of locations 755C, 755D and 755E.

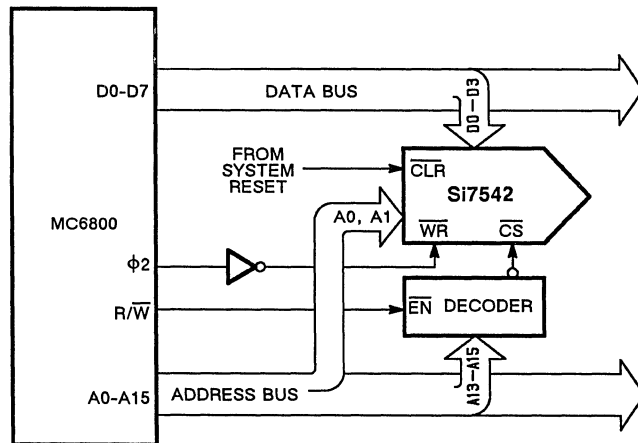


Figure 8. Interfacing the Si7542 to an MC6800 Microprocessor

**INTERFACING**

**TABLE 4.**  
Sample Subroutine for Si7542-MC6800 Interface

LOC	CODE	MNEM	REMARKS
XXXX	BD	JSR	Jump to subroutine
XXXY	75		
XXXZ	42		
7542	B6	LDA	Low-Byte Data -> A
7543	75		
7544	5C		
7545	B7	STA	Load Low-Byte register
7546	75		
7547	58		
7548	B6	LDA	Med-Byte data -> A
7549	75		
754A	5D		
754B	B7	STA	Load Med-Byte register
754C	75		
754D	59		
754E	B6	LDA	High-Byte data -> A
754F	75		
7550	5E		
7551	B7	STA	Load High-Byte register
7552	75		
7553	5A		
7554	B7	STA	DAC register loaded
7555	75		
7556	5B		
7557	39	RTS	Return from subroutine
7558			Low-Byte register address
7559			Med-Byte register address
755A			High-Byte register address
755B			DAC register address
755C			Low-Byte data
755D			Med-Byte data
755E			High-Byte data

**Si7542 INTERFACE TO 8085A**

The typical 8085A system configuration is shown in Figure 9. The Si7542  $\overline{CS}$  input is decoded from the three high order address lines A13-A15. The 8085A WR output is directly connected to the WR input of the Si7542. Table 5 gives a sample loading subroutine. The 12-bit data to be passed to the subroutine is stored in locations 755D and 755E. The four most significant data bits are assumed to occupy the lower half of 755E. Locations 7559, 755A, 755B and 755C select the low byte, middle byte, high byte and DAC registers respectively.

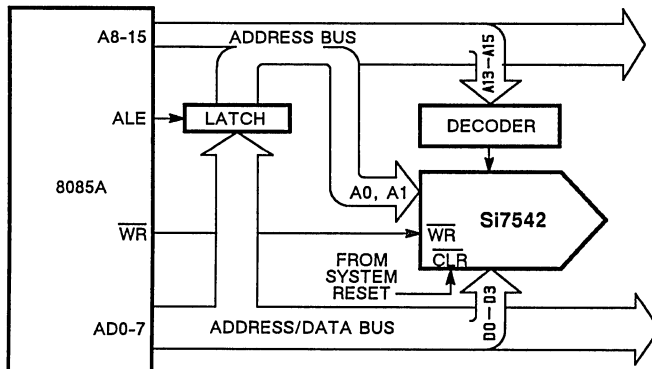


Figure 9. Interfacing the Si7542 to an 8085 Microprocessor

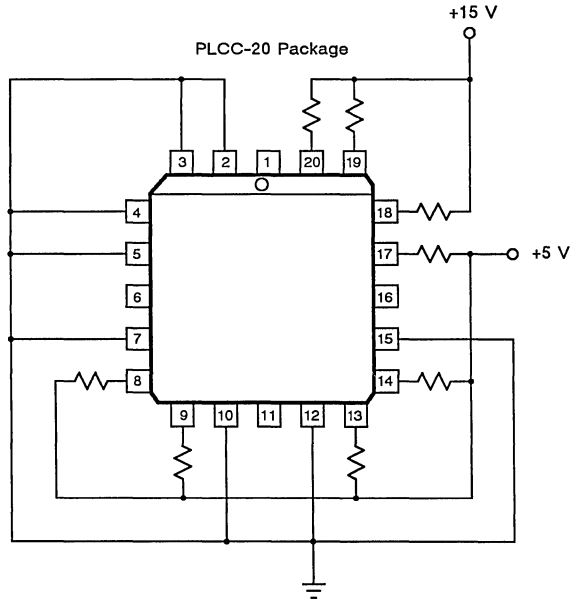
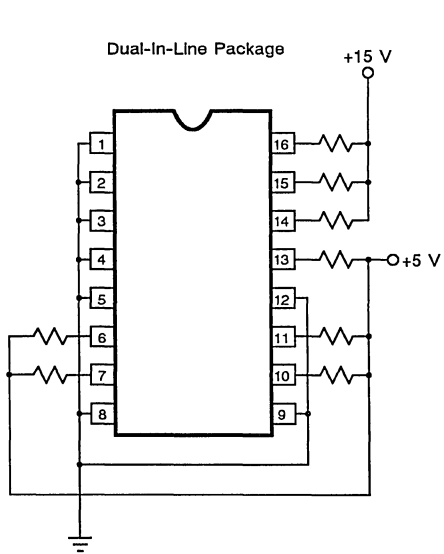
TABLE 5.  
Sample Subroutine for Si7542-8085A Interface

LOC	CODE	MINEM	REMARKS
XXXX	CD	CAL	Call subroutine
XXXZ	75		
7542	3A	LDA	Low- and Med- Byte data -> A
7543	75		
7544	5D		
7545	32	STA	Load Low-Byte register
7546	75		
7547	59		
7548	1F	RAR	Rotate right (4 times)
7549	1F	RAR	
754A	1F	RAR	
754B	1F	RAR	
754C	32	STA	Load Med-Byte register
754D	75		
754E	5A		
754F	3A	LDA	High-Byte data -> A
7550	75		
7551	5E		
7552	32	STA	Load High-Byte register
7553	75		
7554	5B		
7555	32	STA	Load DAC register
7556	75		
7557	5C		
7558	C9	RET	Return
7559			Low-Byte register address
755A			Med-Byte register address
755B			High-Byte register address
755C			DAC register address
755D			Low- and Med-Byte data
755E			High-Byte data

## PIN DESCRIPTION (DIP)

PIN NUMBER	SYMBOL	DESCRIPTION	PIN NUMBER	SYMBOL	DESCRIPTION
1	OUT1	Current Output 1	9	$\overline{WR}$	WRITE Input
2	OUT2	Current Output 2	10	A0	Address Bus Input
3	AGND	Analog Ground	11	A1	Address Bus Input
4	D3	Data Input (MSB)	12	$\overline{DGND}$	Digital Ground
5	D2	Data Input	13	$\overline{CLR}$	Clear Input
6	D1	Data Input	14	V <sub>DD</sub>	+V Supply Input
7	$\overline{D0}$	Data Input (LSB)	15	V <sub>REF</sub>	Reference Input
8	$\overline{CS}$	Chip Select Input	16	R <sub>FB</sub>	DAC Feedback Resistor

**BURN-IN DIAGRAMS**



NOTE: All resistors are 1 k $\Omega$ .

# Si7543

## CMOS 12-Bit Serial Input DAC

### FEATURES

- Serial Load On Positive Or Negative Strobe
- Nonlinearity:  $\pm 1/2$  LSB  $T_{min}$  to  $T_{max}$
- Low Gain Drift: 2 ppm/°C Typ. 5 ppm/°C Max.
- Full 4-Quadrant Multiplication
- Single +5 Volt Supply Operation

### BENEFITS

- Reduced Pin Count and Board Space
- Improved Accuracy
- Reduced Calibration
- Simplified Interface
- Reduced Power

### APPLICATIONS

- Industrial Process Control
- Instrumentation
- Digital Attenuation
- Analog Multiplication
- Remote Sensing

### DESCRIPTION

The Si7543 is a precision CMOS 12-bit multiplying DAC. Its serial data input reduces the number of input data lines required, resulting in a smaller package.

The Si7543 includes two registers and a multiplying DAC. Register A is a serial-to-parallel shift register. The data is clocked from the SRI pin into this register on the edge of the strobe input; either the rising or the falling edge can be selected. After Register A is full the contents are transferred to Register B, a separate DAC register, by using the load inputs. Register B can be reset at any time by use of the CLR (clear) input.

True 12-bit linearity (1/2 LSB), low gain tempco (5 ppm/°C), and low gain error (1 LSB) eliminate the need for DAC calibration and improve system

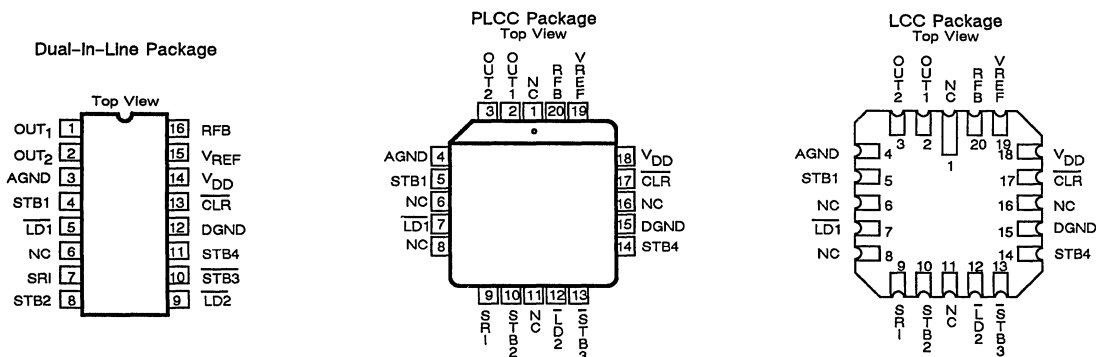
accuracy. The full 4-quadrant multiplying capability facilitates digitally-controlled attenuation and control of ac signals without requiring a dc bias.

Applications include serial interface control loops, remote data acquisition and conversion, avionics, and portable instrumentation.

Built on the Siliconix PolyMOS™ process, the Si7543 uses highly-stable thin film resistors which are laser-trimmed for high accuracy. An epitaxial layer prevents latchup.

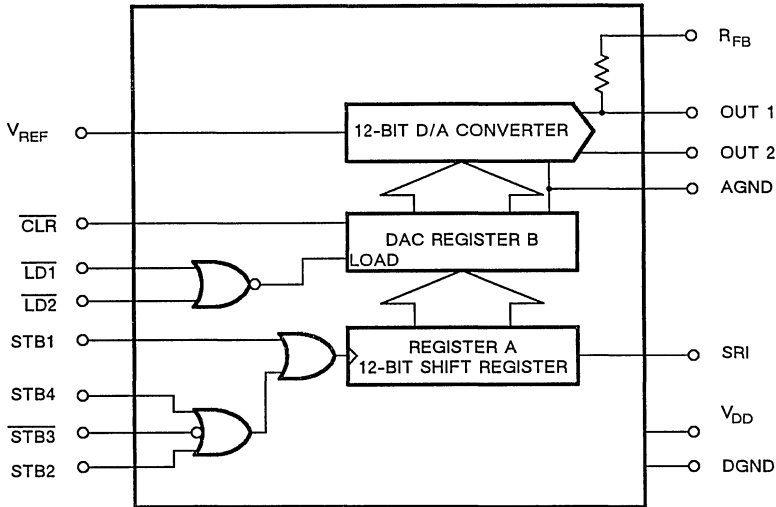
Packaging options include the 16-pin side braze DIP and LCC-20 for military, S, T suffix (–55 to 125°C) operation, 16-pin CerDIP for industrial, A, B suffix (–40 to 85°C) operation, the 16-pin plastic DIP and PLCC-20 for commercial, J, K suffix (0 to 70°C) operation.

### PIN CONFIGURATION





**FUNCTIONAL BLOCK DIAGRAM**



**ORDERING INFORMATION**

INL T <sub>min</sub> - T <sub>max</sub> (LSB)	GAIN ERROR T <sub>a</sub> = 25° C (LSB)	TEMPERATURE RANGE AND PACKAGE				
		PLASTIC 0 to 70° C	PLCC-20 0 to 70° C	CerDIP -40 to 85° C	SIDE BRAZE -55 to 125° C	LCC -55 to 125° C
± 1	± 12.3	SI7543JN	SI7543JP	SI7543AQ	SI7543SD	SI7543SE
± 1/2	± 12.3	SI7543KN	SI7543KP	SI7543BQ	SI7543TD	SI7543TE
± 1/2	± 1	SI7543GKN	SI7543GKP	SI7543GBQ	SI7543GTD	SI7543GTE

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**ABSOLUTE MAXIMUM RATINGS \***

V <sub>DD</sub> to AGND	-0.3, +17 V
V <sub>DD</sub> to DGND	-0.3, +17 V
V <sub>REF</sub> to AGND	±25 V
V <sub>RFB</sub> to AGND	±25 V
Digital Input Voltage to DGND	-0.3 V, +15.3 V
V <sub>OUT1</sub> , V <sub>OUT2</sub> to AGND	-0.3 V, +15.3 V
AGND to DGND	V <sub>DD</sub>
DGND to AGND	V <sub>DD</sub>
Storage Temperature	-65 to 150° C

Operating Temperature (N, P Suffix)	0 to 70° C
(Q Suffix)	-40 to 85° C
(D, E Suffix)	-55 to 125° C

Power Dissipation (Package)**	
16-Pin Plastic DIP***	470 mW
16-Pin Ceramic Side Braze****	900 mW
20-Pin Plastic Leaded Chip Carrier***	450 mW
20-Pin LCC****	900 mW

\* Stress ratings only. Exposure to absolute max rating conditions for extended periods may affect device reliability.

\*\* All leads welded or soldered to PC Board.

\*\*\* Derate 6.5 mW/°C above 25° C.

\*\*\*\* Derate 12 mW/°C above 75° C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 5\text{ V}$ , $V_{REF} = +10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier: OP-07		LIMITS				UNIT	
				1=25°C		2=125,85,70°C			ALL GRADES EXCEPT AS NOTED
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>ACCURACY</b>									
Resolution	N			1,2,3		12		Bits	
Relative Accuracy (Integral Non-Linearity)	INL	(1LSB = 0.024% of Full Scale)	A, J, S Grades	1,2,3		-1	1	LSB	
			All Other Grades	1,2,3		-0.5	0.5		
Differential Nonlinearity	DNL	A, J, S Grades		1,2,3		-2	2	LSB	
		All Other Grades		1,2,3		-1	1		
Gain Error <sup>e</sup>	G <sub>FSE</sub>	G Grade		1		-1	1	LSB	
		All Other Grades		1		-12.3	12.3		
		GB, GK Grades		2,3		-1	1		
		GT Grade		2,3		-2	2		
		J, K Grades		2,3		-13.5	13.5		
		S, T, Grades		2,3		-14.5	14.5		
		A, B Grades		2,3		-13.5	13.5		
Gain Temp Coefficient <sup>c</sup>	TC <sub>GFS</sub>	$\Delta$ Gain / $\Delta$ Temperature		1,2,3	2	-5	5	ppm/ °C	
Power Supply Rejection	PSRR	$\Delta$ Gain / $\Delta$ V <sub>DD</sub> V <sub>DD</sub> = $\pm 5\%$		1 2,3		-0.005 -0.01	0.005 0.01	% per %	
Output Leakage Current (Pin 4 = OUT1) (Pin 5 = OUT2)	I <sub>OUT1</sub> , I <sub>OUT2</sub>	DAC Loaded with All Zeros: I <sub>OUT1</sub> DAC Loaded with All Ones: I <sub>OUT2</sub>		1		-5	5	nA	
		J, K, GK Grades		2,3		-10	10		
		All Other Grades		2,3		-200	200		
<b>DYNAMIC</b>									
Current Settling Time <sup>c, g</sup>	t <sub>s</sub>			1,2,3			2	$\mu$ s	
Multiplying Feedthrough Error <sup>c, g</sup>	FT	V <sub>REF</sub> = $\pm 10\text{ V}$ 10 kHz Sine Wave		1,2,3			2.5	mV <sub>P-P</sub>	

**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 5\text{ V}$ , $V_{REF} = +10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier: OP-07	LIMITS				UNIT
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		ALL GRADES EXCEPT AS NOTED		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>							
Reference Input Resistance (Pin 15)	$R_{REF}$		1,2,3	10	8	25	k $\Omega$
Output Capacitance <sup>c</sup>	$C_{OUT1}$	DAC Loaded to All Zeros	1,2,3			70	pF
		DAC Loaded to All Ones	1,2,3			200	
	$C_{OUT2}$	DAC Loaded to All Zeros	1,2,3			200	
		DAC Loaded to All Ones	1,2,3			70	
<b>LOGIC INPUTS</b>							
Logic HIGH Voltage	$V_{IH}$		1,2,3		3		V
Logic LOW Voltage	$V_{IL}$		1,2,3			0.8	
Input Current	$I_{IN}$	$V_{IN} = 0\text{ V or }V_{DD}$	1,2,3	<0.001	-1	1	$\mu\text{A}$
Input Capacitance <sup>c</sup>	$C_{IN}$		1,2,3			8	pF
<b>TIMING <sup>h</sup></b>							
Serial Input to Strobe Setup Time	$t_{DS1}$	STB1 Used as a Strobe	1 2,3			50 100	ns
	$t_{DS4}$	STB4 Used as a Strobe	1,2,3			0	
	$t_{DS3}$	$\overline{\text{STB3}}$ Used as a Strobe	1,2,3			0	
	$t_{DS2}$	STB2 used as a Strobe	1 2,3			20 40	
Serial Input to Strobe Hold Time	$t_{DH1}$	STB1 Used as a Strobe	1 2,3			30 60	
	$t_{DH4}$	STB4 Used as a Strobe	1 2,3			80 160	
	$t_{DH3}$	$\overline{\text{STB3}}$ Used as a Strobe	1 2,3			80 160	
	$t_{DH2}$	STB2 used as a Strobe	1 2,3			60 120	

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ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 5\text{ V}$ , $V_{REF} = +10\text{ V}$ $V_{OUT1} = V_{OUT2} = 0\text{ V}$ Output Amplifier: OP-07	LIMITS				UNIT
			1=25°C		ALL GRADES EXCEPT AS NOTED		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>TIMING <sup>h</sup> (Cont'd)</b>							
SRI Data Pulse Width	$t_{SRI}$		1 2,3			80 160	ns
STB1 Pulse Width	$t_{STB1}$		1 2,3			80 160	
STB4 Pulse Width	$t_{STB4}$		1 2,3			100 200	
$\overline{\text{STB3}}$ Pulse Width	$t_{STB3}$		1 2,3			100 200	
STB2 Pulse Width	$t_{STB2}$		1 2,3			80 160	
Load Pulse Width	$t_{LD1}$ , $t_{LD2}$		1 2,3			150 300	
Min. Time Between Strobing LSB into Register A and Loading Register B	$t_{ASB}$		1,2,3			0	
$\overline{\text{CLR}}$ Pulse Width	$t_{CLR}$		1 2,3			200 400	
<b>SUPPLY</b>							
Supply Voltage	$V_{DD}$		1,2,3		5		V
Supply Current	$I_{DD}$	Digital Inputs = $V_{IH}$ or $V_{IL}$	1,2,3			2.5	mA

## NOTES:

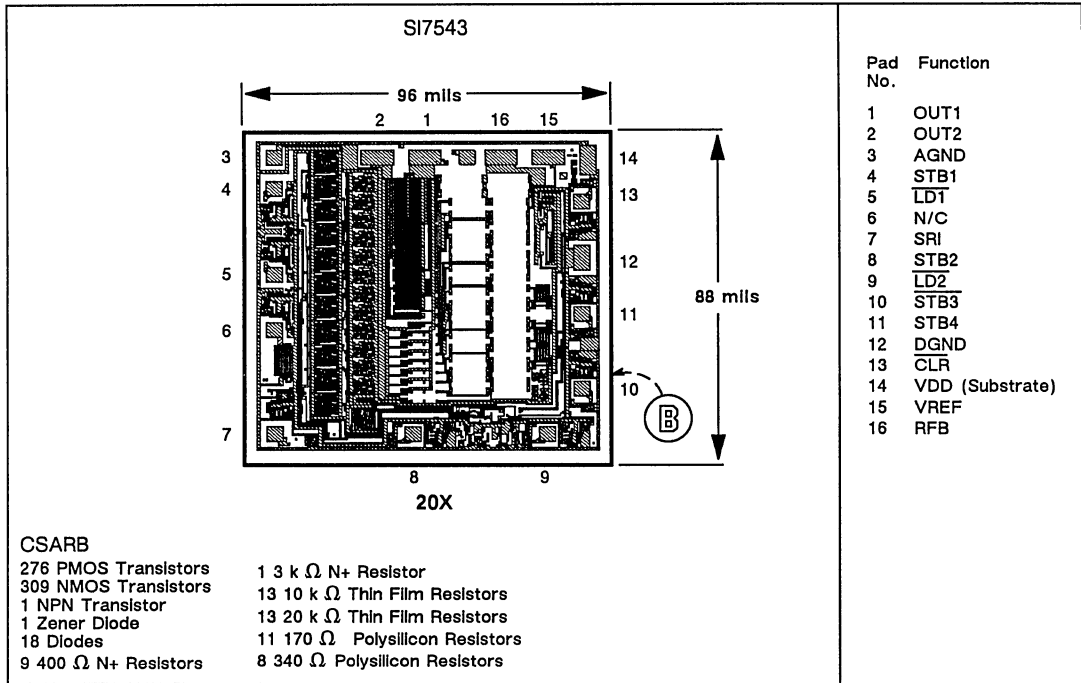
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Gain error is measured using internal  $R_{FB}$  only. Gain error can be trimmed to zero using circuits of Figures 6 and 7.
- Measured to  $1/2$  LSB. OUT1 Load =  $100\ \Omega$ , DAC output measured from falling edge of LD1 and LD2.
- Feedthrough error may be reduced by connecting the metal lid on the side braze package to DGND.
- Sample tested at 25°C to ensure compliance.

## CAUTION

ESDS (Electro-Static-Discharge-Sensitive) device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy

electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

**DIE TOPOGRAPHY**



**DEFINITION OF TERMS**

**RELATIVE ACCURACY**

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1 LSB.

**DIFFERENTIAL NONLINEARITY**

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range insures monotonicity.

**GAIN ERROR**

Gain error or full-scale error is a measure of the difference between an ideal DAC's and the actual device output. For the Si7543, ideal full-scale output is  $-(4095/4096) \cdot (V_{REF})$ . Gain error is adjustable to zero using external trims as shown in Figures 6 and 7.

**OUTPUT LEAKAGE CURRENT**

Current which appears at OUT1 with the DAC register loaded to all 0's or at OUT2 with the DAC register loaded to all 1's.

**MULTIPLYING FEEDTHROUGH ERROR**

AC error due to capacitive feedthrough from  $V_{REF}$  terminal to OUT1 with DAC register loaded to all 0's.

## DETAILED DESCRIPTION

The Si7543 includes two registers and a 12-bit DAC. The DAC circuit consists of an R-2R resistor array as shown in Figure 1. Thin-film resistors are used, which are laser-trimmed for accuracy. Depending upon the status of each input bit, the binary weighted currents are switched to either OUT1 or OUT2. This maintains a constant current through each ladder leg regardless of the switch state. A typical NMOS current switch is shown in Figure 2.

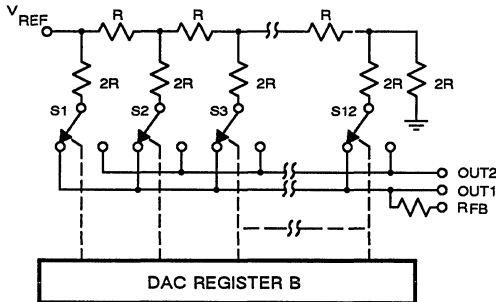


Figure 1. Si7543 Functional Diagram (All Inputs HIGH)

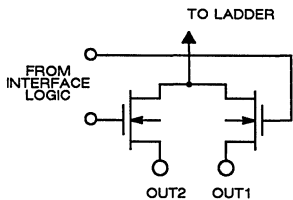


Figure 2. Simplified Schematic, Single SPDT Switch

The output current is a function of  $V_{REF}$  and the digital input code. (Hence the term *multiplying* DAC.) The input resistance at  $V_{REF}$  is equal to value "R" and does not change with input code.  $V_{REF}$  can be either a fixed or time varying voltage or current, of positive or negative polarity. If a current source is used for the reference input, then a low temperature coefficient resistor should be used for  $R_{FB}$  to minimize gain variation with temperature.

### EQUIVALENT CIRCUIT ANALYSIS

Figures 3 and 4 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW or HIGH respectively.

When all digital inputs are LOW, the equivalent circuit appears as shown in Figure 3. There are two current components shown:  $I_{REF}$  and  $I_{LEAKAGE}$ . The  $I_{REF}/4096$  current source is actually the 1 LSB current which flows through the ladder termination resistor to GND. The  $I_{LEAKAGE}$  current sources represent surface and junction leakages to the substrate.

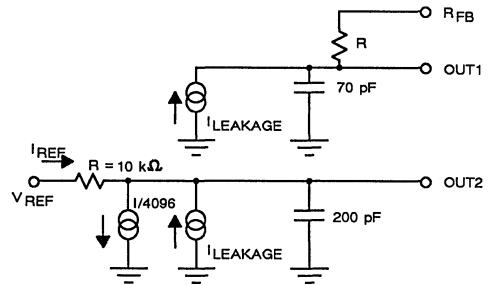


Figure 3. Si7543 Equivalent Circuit (All Inputs LOW)

The 70 pF capacitor on OUT1 represents the OFF capacitance of the output switch. The 200 pF capacitor on OUT2 represents the switch ON capacitance.

A similar analysis holds when all digital inputs are HIGH, as shown in Figure 4. Notice that in this case, the 200 pF is on OUT1 and the 70 pF is on OUT2. This capacitance is code-dependent and is a function of the number of ON switches which are connected to a specific output.

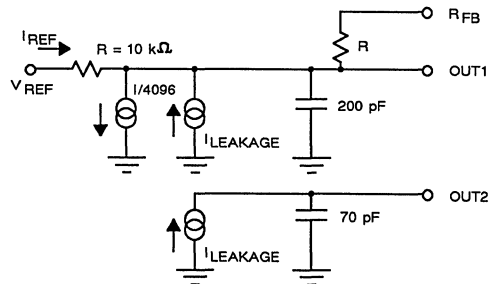


Figure 4. Si7543 Equivalent Circuit (All Inputs HIGH)

**DETAILED DESCRIPTION**

**INTERFACE LOGIC**

As previously stated, the Si7543 includes two registers. The timing diagram is shown in Figure 5 and the truth table in Table 1. Register A is a

serial-to-parallel shift register. The data is clocked from the SRI pin into this register on the rising edge of STB1, STB2, or STB4 or on the falling edge of STB3.

TABLE 1. Si7543 Truth Table

Si7543 Control Inputs							Si7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	STB3	STB2	STB1	CLR	LD2	LD1		
0	1	0	1	X	X	X	Data Appearing at SRI Strobe Into Register A	2, 3
0	1	1	0	X	X	X		
0	1	0	0	X	X	X		
1	1	0	0	X	X	X		
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	X	1					
				0	X	X	Clear Register B to Code 0000 0000 0000 (Asynchronous Operation)	1, 3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0		

**NOTES:**

1. CLR = 0 asynchronously resets Register B to 0000 0000 000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown 1 is positive edge 0 is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.
4. (MSB) XXXX XXXX XXXX (LSB)

HIGH-Byte    MIDDLE-Byte    LOW-Byte

After Register A is full the contents are transferred to Register B, a separate DAC register, by bringing LD1 and LD2 momentarily LOW. Register B can be reset (0000 0000 0000) at any time by bringing CLR momentarily LOW. This can be used to initialize the Si7543 at power up, or to rapidly bring the DAC

output to a known state. When operating in the unipolar mode (Figure 6), a CLEAR sends the DAC output voltage to 0 V. When in the bipolar mode (Figure 7), a CLEAR sends the DAC output to -VREF.

## DETAILED DESCRIPTION (Cont'd)

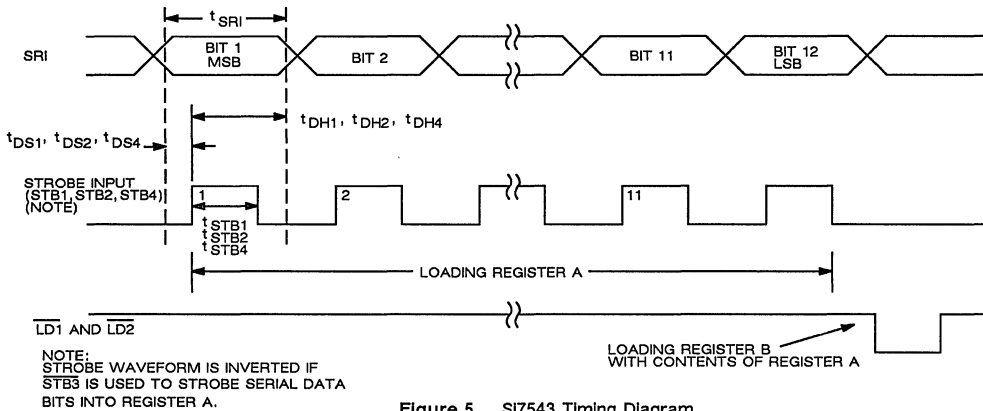


Figure 5. Si7543 Timing Diagram

## APPLICATIONS INFORMATION

### UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the simplest Si7543 configuration. The logic inputs are omitted for clarity. The input to  $V_{REF}$  can be either positive or negative; with a dc reference voltage or current the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant reference multiplication (digitally controlled attenuation). The input/output relationship is shown in Table 2.

TABLE 2.

DIGITAL INPUT MSB    LSB	ANALOG OUTPUT ( $V_{OUT}$ )
1111 1111 1111	$-(4095/4096) V_{REF}$
1000 0000 0000	$-(1/2) V_{REF}$
0000 0000 0001	$-(1/4096) V_{REF}$
0000 0000 0000	0 V

Unipolar Binary Code Table for Circuit  
of Figure 6

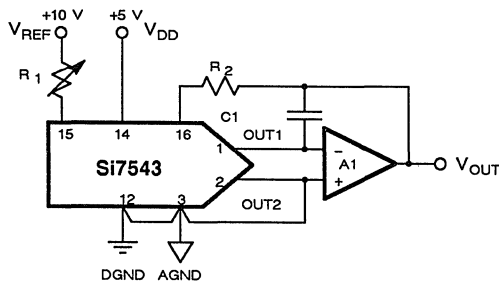


Figure 6. Unipolar Binary Operation  
(2 - Quadrant Multiplication)

$R_1$  can be used to provide full-scale trim capability. (Load the DAC register to 1111 1111 1111 and adjust  $R_1$  for  $V_{OUT} = -V_{REF} (4095/4096)$ .) Alternatively, the full scale can be adjusted by omitting  $R_1$  and  $R_2$  and trimming the  $V_{REF}$  magnitude. (See also the Application Hint "Gain Temperature Coefficients".)

$C_1$  (10 to 25 pF) is used for phase compensation and may be required for stability when using a high speed amplifier. (See the Application Hint "High Frequency Considerations".)



**APPLICATIONS INFORMATION**

For amplifier A1 considerations, refer to the Application Hint "Output Offset".

**BIPOLAR OPERATION  
(4-QUADRANT MULTIPLICATION)**

The circuit for bipolar operation is shown in Figure 7, accompanied by the input/output relationship in Table 3. With a positive or negative dc reference, the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the reference while the MSB provides polarity control.

TABLE 3.

DIGITAL INPUT MSB      LSB	ANALOG OUTPUT (V <sub>OUT</sub> )
1111 1111 1111	$+(2047/2048) V_{REF}$
1000 0000 0001	$+(1/2048) V_{REF}$
1000 0000 0000	0 V
0111 1111 1111	$-(1/2048) V_{REF}$
0000 0000 0000	$-V_{REF}$

Bipolar Binary Code Table for Circuit of Figure 7

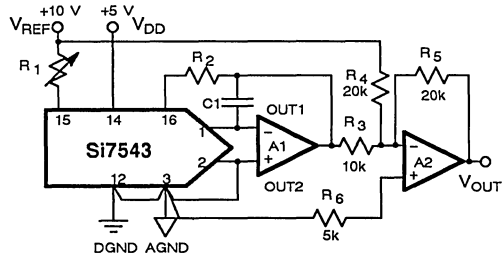


Figure 7. Bipolar Operation (4 - Quadrant Multiplication)

Unlike the unipolar circuit of Figure 6, the 0 V level as well as the full-scale must be trimmed in this circuit. To trim the 0 V level, load the DAC register with 1000 0000 0000, and adjust R1 for V<sub>OUT</sub> = 0 V. Alternatively, R1 and R2 can be omitted and the ratio of R3 to R4 adjusted for V<sub>OUT</sub> = 0 V. Full scale can be trimmed by adjusting the amplitude of V<sub>REF</sub> or by varying the value of R5.

**APPLICATIONS HINTS**

**GROUND MANAGEMENT**

Voltage differences between the Si7543 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the Si7543. In more complex systems where the AGND-DGND connection is at a distant point, it is recommended that diodes be connected in inverse parallel between the Si7543 AGND and DGND pins (1N914 or equivalent).

**OUTPUT OFFSET**

CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent

error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is  $0.67 \cdot V_{OS}$  where  $V_{OS}$  is the amplifier input offset voltage. It is recommended that  $V_{OS}$  be no greater than 0.1 LSB over the operating temperature range. The bias current causes an output offset at V<sub>OUT</sub> equal to  $I_B \cdot R_{FB}$ .

**HIGH FREQUENCY CONSIDERATIONS**

The Si7543 output capacitance and the amplifier feedback resistance combine to add a pole to the open loop response. This reduces the closed loop bandwidth, and may also cause ringing or oscillation if the pole frequency is less than the amplifier's 0 dB crossover frequency. Adding a phase compensation capacitor in parallel with the feedback resistor can restore stability to the circuit.

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**APPLICATIONS HINTS**


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**TEMPERATURE COEFFICIENTS**

The gain temperature coefficient of the Si7543 has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to gain shifts of 2 LSBs and 0.8 LSB, respectively, over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full-scale range, the temperature coefficient of R1 and R2 should also be taken into account. Resistors with temperature coefficients of 50 ppm/°C will usually give acceptable results. For

the standard Si7543 with a maximum gain error of  $\pm 12.3$  LSBs, suitable values for R1 and R2 are 120  $\Omega$  and 60  $\Omega$ , respectively. This results in a maximum additional gain error temperature coefficient of approximately 3 ppm/°C.

However, if the Si7543 GTD is used (max gain error = 1 LSB), then with R1 = 10  $\Omega$  and R2 = 5  $\Omega$  the additional gain error temperature coefficient is only 0.25 ppm/°C maximum.

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**INTERFACING**


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**Si7543 INTERFACE TO MC6800**

The circuit in Figure 8 and the sample subroutine shown in Table 4 demonstrate one method of interfacing the Si7543 to an MC6800 microprocessor. If the starting address for the subroutine is 7543 (Hex), then the data can be stored at the end of the listing in locations 755D (middle and lower bytes) and 755E (high byte), as follows:

```
755D: 76543210
755E: BA98XXXX
```

where "B" is bit 11 (MSB), "0" is bit 0 (LSB), and so on.

Data line D7 from the 6800 is used as the serial input to the Si7543 SRI pin. Starting with the MSB, the data is strobed one bit at a time into Register A. After all 12 data bits have been sent to the Si7543, they are then loaded into Register B. Address bits 13, 14, and 15 of the 6800 are used to determine STB3 (A000) and LD2 (B000).

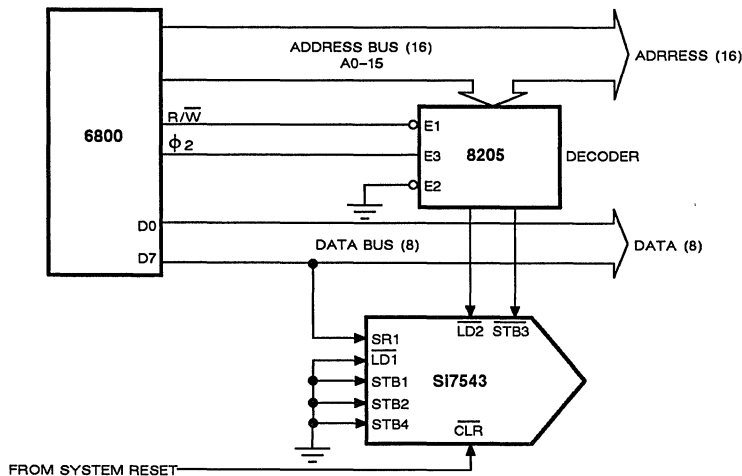


Figure 8. Interfacing the Si7543 to an MC6800 Microprocessor

**INTERFACING (Cont'd)**

**TABLE 4.**  
**Sample Subroutine for Si7543-MC6800 Interface**

<u>LABEL</u>	<u>MNEMONIC</u>	<u>OPERAND</u>	<u>COMMENT</u>
7543	LDA	A,755E	Put upper 4 bits in Acc A
	BSR	SEND	Send bits 11 through 8 to SI7543
	LDA	A,755D	Put lower 8 bits in Acc A
	BSR	SEND	Send bits 7 through 4
	BSR	SEND	Send bits 3 through 0
	STA	A,B000	Load data into SI7543 Register B
	RTS		
	SEND	LDA	B,#04
STA		A,A000	Strobe data into SI7543
ROL		A	Move next bit into position
DEC		B	
BNE		SEND	Repeat until 4 bits sent
RTS			

**SI7543 INTERFACE TO 8085A**

Figure 9 and Table 5 show how the Si7543 can be interfaced to the 8085. In this example, it is assumed that the data to be sent is present in the H and L registers as follows:

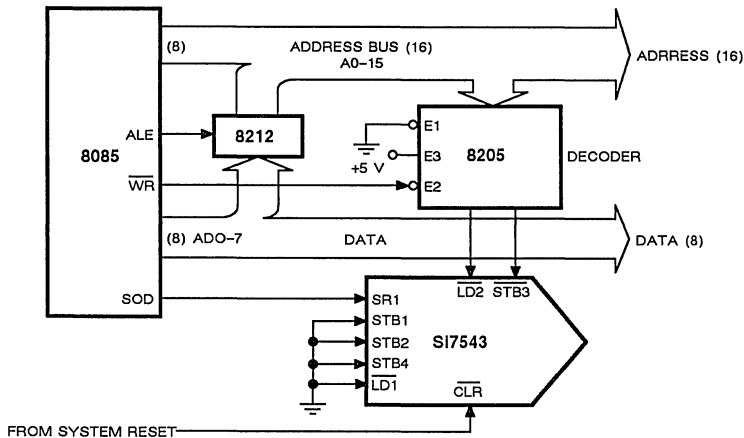
Register H: XXXXBA98

Register L: 786543210

where "B" is bit 11 (MSB), "0" is bit 0 (LSB), and so on.

Since bit 7 of the Accumulator will be used for the serial data bit, the data is first left-justified in

Registers H and L. Bit 6 of the Accumulator is the Serial Output Enable bit, and must be set before the SIM instruction is used. The ORA instruction puts the next data bit into bit 7 of the Accumulator, keeping SOE asserted at the same time. The AI instruction masks out all bits except 6 and 7, insuring that no flags are inadvertently reset. Address bits 13, 14, and 15 are used to determine STB3 and LD2. The data is strobed into the Si7543 by writing to location A000. After all 12 bits have been sent, writing to location B000 loads the data into Register B of the Si7543.



**Figure 9.** Interfacing the Si7543 to an 8085 Microprocessor

## INTERFACING (Cont'd)

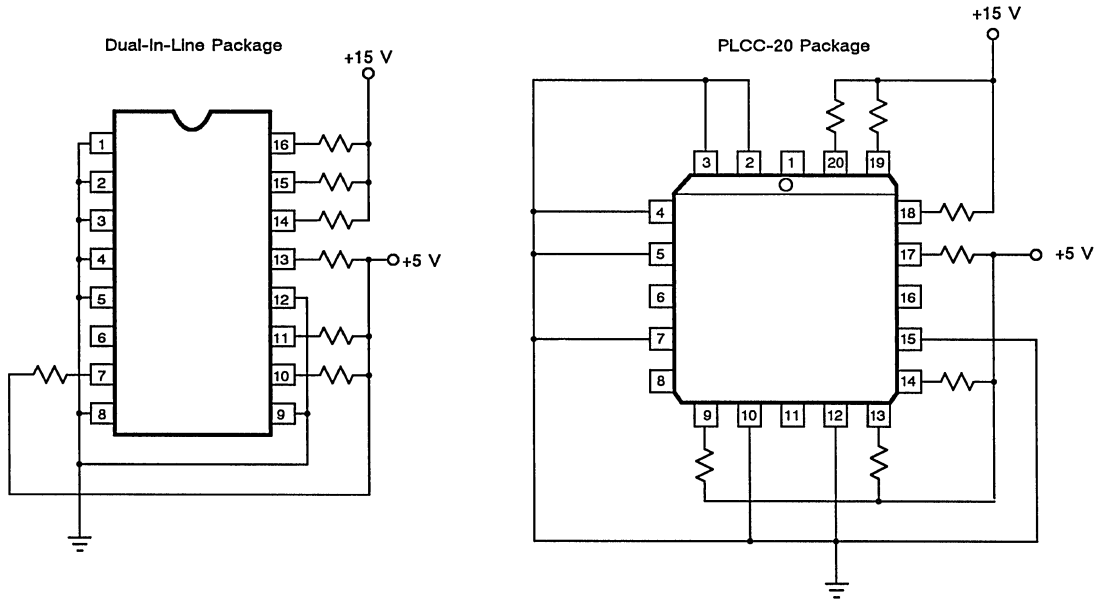
TABLE 5.  
Sample Subroutine for Si7543-8085A Interface

<u>LABEL</u>	<u>MNEMONIC</u>	<u>OPERAND</u>	<u>COMMENT</u>
7543	MVI	B,04	Left-justify data
	DAD	H	by shifting H and L
	DCR	B	left four times
	JNZ	7543	
SEND	MVI	B,0C	Counter for 12 bits
	MVI	A,70	Enable Serial Output (SOD)
	ORA	H	Preserve SOE and data bit
	ANI	C0	Don't reset flags
	SIM		Latch data bit into SOD FF
	STA	A000	Strobe data into Si7543
	DAD	H	Shift next bit into D7 of H
	DCR	B	
	JNZ	SEND	Repeat until 12 bits sent
	STA	B000	Load Register B of Si7543
	RET		

## PIN DESCRIPTION (DIP)

<u>PIN NUMBER</u>	<u>SYMBOL</u>	<u>DESCRIPTION</u>	<u>PIN NUMBER</u>	<u>SYMBOL</u>	<u>DESCRIPTION</u>
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground.	9	<u>LD2</u>	DAC Register B Load <u>2</u> input. When <u>LD1</u> and <u>LD2</u> go low the contents of Register A are loaded into DAC Register B.
2	OUT2	DAC current output bus. Normally terminated at AGND.	10	<u>STB3</u>	Register A Strobe 3 input, see Table 2.
3	AGND	Analog Ground	11	STB4	Register A Strobe 4 input, see Table 2.
4	STB1	Register A Strobe 1 input, see Table 2.	12	DGND	Digital Ground.
5	<u>LD1</u>	DAC Register B Load 1 input. When <u>LD1</u> and <u>LD2</u> go low the contents of Register A are loaded into DAC Register B.	13	<u>CLR</u>	Register B CLEAR input (active LOW) can be used to asynchronously reset Register B to 0000 0000 0000
6	N/C	No Connection.	14	V <sub>DD</sub>	+5 V Supply Input
7	SRI	Serial Data Input to Register A.	15	V <sub>REF</sub>	Reference input. Can be positive or negative dc voltage or ac signal.
8	STB2	Register A Strobe 2 input, see Table 2.	16	R <sub>FB</sub>	DAC Feedback Resistor.

**BURN-IN DIAGRAMS**



NOTE: All resistors are 1 kΩ .

# Si7545

## CMOS 12-Bit Buffered Multiplying DAC

### FEATURES

- On-Board Latches
- INL < 1/2 LSB
- Low Gain TC: 2 ppm/°C
- Four Quadrant Multiplication
- Low Gain Error ( $G_{FSE} < 1 \text{ LSB}$ )

### BENEFITS

- Simplified Microprocessor Interface
- True 12-Bit Linearity
- Improved Stability Over Temperature
- Accepts Bipolar Reference Inputs
- Reduced System Calibration

### APPLICATIONS

- Microprocessor Controlled Systems
- ATE Systems
- Power Supplies
- $\mu\text{P}$  Controlled Gain/Attenuation
- Function Generators

### DESCRIPTION

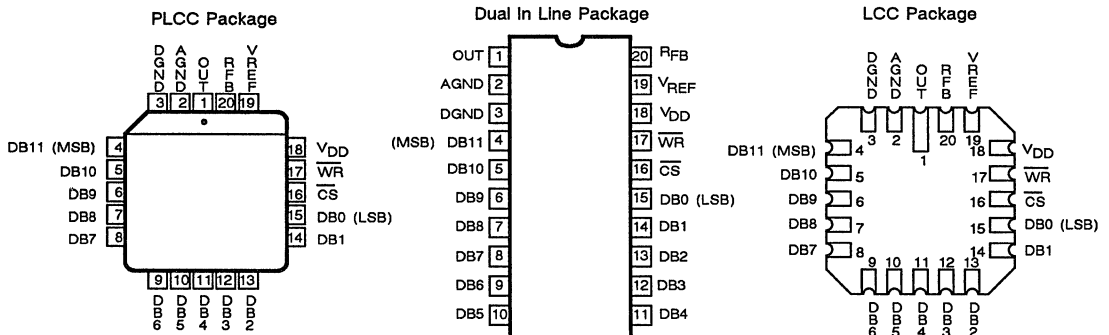
The Si7545 is a monolithic 12-Bit CMOS digital-to-analog converter with an on-board 12-Bit wide latch to simplify the interface to a data bus. The R-2R ladder DAC allows four-quadrant multiplication for ac attenuation applications. The Si7545 allows flexibility in supply voltage and logic levels, being specified for TTL-compatible operation when used with a single 5 V power supply. CMOS logic compatibility is specified when operated from a single 15 V supply.

The Si7545 is ideal for microprocessor-controlled data conversion applications such as function generation, power supplies, ATE systems, and process control. As a four-quadrant multiplying DAC, the Si7545 has applications in gain control, attenuation, filtering and programmable references.

The Si7545 is built on the Siliconix proprietary advanced 5-micron CMOS process known as PolyMOS™. Highly stable thin-film resistors are used to provide superior matching and stability over both temperature and time. Laser trimming is used to achieve true 12-Bit linearity and low gain error. An epitaxial layer prevents latchup.

The Si7545 is available in the 20-lead PDIP and PLCC packages for operation over the commercial, J, K, L suffix (0 to 70°C) temperature range, the 20-lead CerDIP for industrial, A, B, C suffix (-40 to 85°C) operation, and the 20-lead side braze and LCC packages for military, S, T, U suffix (-55 to 125°C) temperature range operation. Four accuracy grades are available for each temperature range.

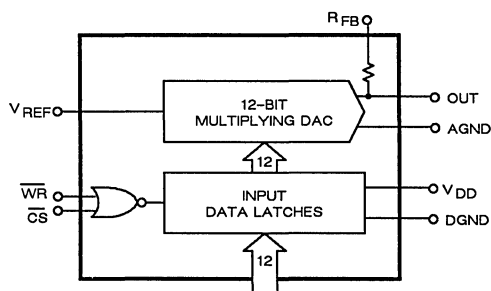
### PIN CONFIGURATION



## ORDERING INFORMATION

INL T <sub>min</sub> - T <sub>max</sub> (LSB)	GAIN ERROR T <sub>a</sub> = 25°C (LSB)	TEMPERATURE RANGE AND PACKAGE				
		PLCC 0 to 70°C	PDIP 0 to 70°C	CerDIP -40 to 85°C	SIDE BRAZE -55 to 125°C	LCC -55 to 125°C
± 2	±20	SI7545JP	SI7545JN	SI7545AQ	SI7545SD	SI7545SE
± 1	±10	SI7545KP	SI7545KN	SI7545BQ	SI7545TD	SI7545TE
± 1/2	± 5	SI7545LP	SI7545LN	SI7545CQ	SI7545UD	SI7545UE
± 1/2	± 1	SI7545GLP	SI7545GLN	SI7545GCQ	SI7545GUD	SI7545GUE

## FUNCTIONAL BLOCK DIAGRAM



## DEFINITION OF TERMS

### MULTIPLYING DAC

Digital-to-Analog Converters (DACs) are devices that convert digital data into analog values. A multiplying DAC is a device capable of handling variable reference sources. Its output is the product of two variables: the number represented by the digital input code and the analog reference voltage.

### RESOLUTION

Resolution indicates the number of digital input bits. A 12-bit DAC resolves the full-scale range (FSR) into  $2^{12} = 4096$  states.

### LSB

Value of the Least Significant Bit. For example, a 12-bit unipolar converter has a 1 LSB step value equal to  $V_{REF} / 2^{12}$  or  $V_{REF}/4096$  (Volts).

### RELATIVE ACCURACY (INL)

Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end points of the DAC

transfer function. It is measured after adjusting for zero and full scale errors and is expressed in % of full scale range or (sub)multiples of 1 LSB.

### DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of  $\pm 1$  LSB max over the operating temperature range ensures monotonicity.

### GAIN ERROR

Gain error or full-scale error is a measure of the difference between an ideal DAC's and the actual device output. For the Si7545, ideal full-scale output is  $-(4095/4096) (V_{REF})$ . Gain error is adjustable to zero using external trims as shown in Figures 4 and 5.

### OUTPUT LEAKAGE CURRENT

This is the current that appears at OUT1 with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

## DEFINITION OF TERMS (Cont'd)

### OUTPUT CURRENT SETTLING TIME

This is the time required for the output current of the DAC to settle to within 1/2 LSB into 100 Ω, and is specified for a zero to full scale digital input change.

### PROPAGATION DELAY

This is a measure of the internal circuit delay from the time a digital input changes to the point when

the analog output at OUT1 reaches 90% of its final value.

### DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the area of the impulse injected to the analog outputs when the digital inputs change state. It is usually specified as the area of the impulse in nV-secs. It is measured with  $V_{REF} = GND$  and an LH0032 as the output op amp, and phase compensation capacitor = 0 pF.

## ABSOLUTE MAXIMUM RATINGS\*

$V_{DD}$ to DGND .....	-0.3 V, 17 V
$V_{REF}$ to DGND .....	± 25 V
$V_{RFB}$ to DGND .....	± 25 V
Digital Input Voltage to DGND .....	-0.3 V to $V_{DD}$
$V_{OUT}$ to DGND .....	-0.3 V to $V_{DD}$
$V_{AGND}$ to DGND .....	-0.3 V to $V_{DD}$
Storage Temperature (D, Q, E Suffix) .....	-65 to 150°C
(N, P Suffix) .....	-65 to 125°C
Power Dissipation (Package)**	
20-Pin Plastic DIP and PLCC***	470 mW

20-Pin CerDIP****	900 mW
20-Pin Ceramic Side Braze****	900 mW
20-Pin LCC****	900 mW

#### Operating Temperature:

Commercial Grades (J, K, L, GL) .....	0 to 70°C
Industrial Grades (A, B, C, GC) .....	-40 to 85°C
Extended Grades (S, T, U, GU) .....	-55 to 125°C

\* Stress rating only. Exposure to absolute max rating conditions for extended periods may affect device reliability.

\*\* All leads welded or soldered to PC board.

\*\*\* Derate 6.5 mW/°C above 25°C.

\*\*\*\* Derate 12 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>				(5 Volt Operation)					
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = +5$ V, $V_{REF} = +10$ V $V_{OUT} = 0$ V, AGND = DGND Output Amplifier: OP-07	LIMITS						UNIT
			1=25°C		C, L, U GC, GL, GU GRADE		A, J, S B, K, T GRADE		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>ACCURACY</b>									
Resolution	N		1,2,3		12		12		Bits
Relative Accuracy (Integral Non-Linearity)	INL	(1LSB = 0.024% of Full Scale)	1,2,3		-0.5	0.5	B, K, T: -1 A, J, S: -2	1 2	LSB
Differential Nonlinearity	DNL		1,2,3		-1	1	B, K, T: -1 A, J, S: -4	1 4	
Gain Error <sup>e</sup>	$G_{FSE}$	Measured Using Internal $R_{FB}$ DAC Register Loaded With: 1111 1111 1111	1 2,3	GC, GL, GU: -1 GC, GL, GU: -2	1 2				
			1 2,3	C, L, U: -5 C, L, U: -6	5 6				
			1,2,3				B, K, T: -10 A, J, S: -20	10 20	
Gain Temp Coefficient <sup>c</sup>	$TC_{BFS}$	$\Delta$ Gain / $\Delta$ Temperature	1,2,3	2	-5	5	-5	5	ppm/ °C



ELECTRICAL CHARACTERISTICS <sup>a</sup>										(5 Volt Operation)			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = +5 V, V <sub>REF</sub> = +10 V V <sub>OUT</sub> = 0 V, AGND = DGND Output Amplifier: OP-07	LIMITS								UNIT		
			1=25°C		2=125,85,70°C		3=-55,-40,0°C		C, L, U GC, GL, GU GRADE			A, J, S B, K, T GRADE	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>ACCURACY (Cont'd)</b>													
DC Supply Rejection	PSRR	$\Delta \text{Gain} / \Delta V_{DD}$ V <sub>DD</sub> = ± 5%	1		-0.015	0.015	-0.015	0.015			% per %		
Output Leakage Current	I <sub>OUT(OFF)</sub>	All Digital Inputs = 0 V	1		-10	10	-10	10			nA		
			2,3		C,GC: -50 L,GL: -50 U,GU:-200	50 50 200	A,B: -50 J,K: -50 S,T: -200	50 50 200					
<b>DYNAMIC</b>													
Current Settling Time <sup>c</sup>	t <sub>s</sub>	To 0.5 LSB, Load = 100 Ω C <sub>EXT</sub> = 13 pF, CS = 0 V <sup>f</sup> Measured From Falling Edge of WR .	1,2,3			1			1		μs		
Propagation Delay <sup>c</sup>	t <sub>PD</sub>	Load = 100 Ω, C <sub>EXT</sub> = 13 pF <sup>f</sup>	1			300			300		ns		
Digital-to-Analog Glitch Impulse	I <sub>s</sub>	V <sub>REF</sub> = AGND Output Amplifier: LH0032 <sup>f</sup>	1	400							nV- sec		
AC Feedthrough at OUT <sup>g</sup>	FT	V <sub>REF</sub> = ±10 V 10 kHz Sinewave	1,2,3	1							mV p-p		
<b>REFERENCE</b>													
Reference Input Resistance (Pin 19 to GND)	R <sub>REF</sub>		1	10	7	25	7	25			kΩ		
R <sub>REFTC</sub>	R <sub>REFTC</sub>		1,2,3	-300							ppm/ °C		
<b>OUTPUT</b>													
Output Capacitance <sup>e</sup>	C <sub>OUT</sub>	$\overline{WR} = 0 \text{ V}$ CS = 0 V	1,2,3			70 150			70 150		pF		
<b>INPUT</b>													
Input HIGH Voltage	V <sub>IH</sub>		1,2,3		2.4			2.4			V		
Input LOW Voltage	V <sub>IL</sub>		1,2,3			0.8			0.8				
Input Current <sup>h</sup>	I <sub>IN</sub>	V <sub>IN</sub> = 0 V or V <sub>DD</sub>	1		-1	1	-1	1			μA		
Input Capacitance <sup>e</sup>	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	DBO-DB11	1,2,3			5		5		pF		
			$\overline{WR}, \overline{CS}$	1,2,3			20		20				

ELECTRICAL CHARACTERISTICS <sup>a</sup>										(5 Volt Operation)			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = +5 V, V <sub>REF</sub> = +10 V V <sub>OUT</sub> = 0 V, AGND = DGND Output Amplifier: OP-07	LIMITS								UNIT		
			1=25°C		2=125,85,70°C		C,L,U GC, GL, GU GRADE		A, J, S B, K, T GRADE				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>					
<b>TIMING</b>													
Chip Select to Write Setup Time	t <sub>CS</sub>	See Timing Diagram Figure 1	1 2,3	200 270	280 380		280 380			ns			
Chip Select to Write Hold Time	t <sub>CH</sub>		1,2,3		0		0						
Write Pulse Width	t <sub>WR</sub>	t <sub>CS</sub> ≥ t <sub>WR</sub> , t <sub>CH</sub> ≥ 0	1 2,3	175 280	250 400		250 400						
Data Setup Time	t <sub>DS</sub>		1 2,3	100 150	140 210		140 210						
Data Hold Time	t <sub>DH</sub>		1,2,3		10		10						
<b>SUPPLY</b>													
V <sub>DD</sub> Range <sup>l</sup>	V <sub>DD</sub>		1,2,3		4.5	16.5	4.5	16.5	V				
Supply Current	I <sub>DD</sub>	All Digital Inputs V <sub>IH</sub> or V <sub>IL</sub>	1,2,3			2		2	mA				
		All Digital Input 0 V or V <sub>DD</sub>	1 2,3	0.01 0.01		0.1 0.5		0.1 0.5					

ELECTRICAL CHARACTERISTICS <sup>a</sup>										(15 Volt Operation)			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = +15 V, V <sub>REF</sub> = +10 V V <sub>OUT</sub> = 0 V, AGND = DGND Output Amplifier: OP-07	LIMITS								UNIT		
			1=25°C		2=125,85,70°C		C,L,U GC, GL, GU GRADE		A, J, S B, K, T GRADE				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>					
<b>ACCURACY</b>													
Resolution	N		1,2,3		12		12		Bits				
Relative Accuracy (Integral Non-Linearity)	INL	(1LSB = 0.024% of Full Scale)	1,2,3		-0.5	0.5	B, K, T: -1 A, J, S: -2	1 2	LSB				
Differential Nonlinearity	DNL		1,2,3		-1	1	B, K, T: -1 A, J, S: -4	1 4					
Gain Error <sup>e</sup>	G <sub>FSE</sub>	Measured Using Internal R <sub>FB</sub> DAC Register Loaded With: 1111 1111 1111	1 2,3	GC, GL, GU: -6 GC, GL, GU: -7	6 7								
			1,2,3	C, L, U: -10	10								
			1,2,3			B, K, T: -15 A, J, S: -25	15 25						
Gain Temp Coefficient <sup>f</sup>	TC <sub>BFS</sub>	Δ Gain / Δ Temperature	1,2,3	2	-10	10	-10	10	ppm/ °C				

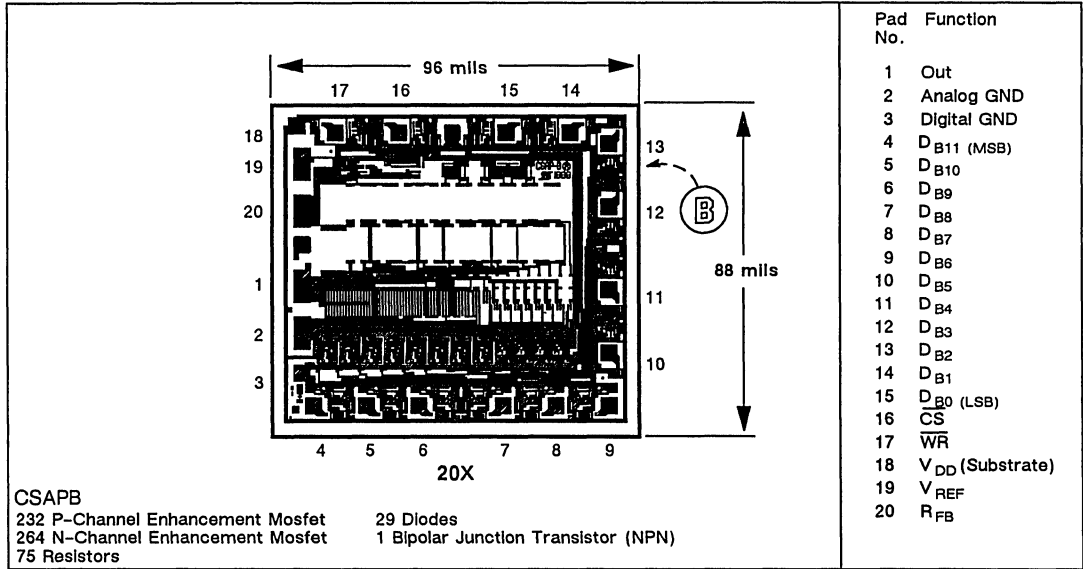
ELECTRICAL CHARACTERISTICS <sup>a</sup>										(15 Volt Operation)	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = +15 V, V <sub>REF</sub> = +10 V V <sub>OUT</sub> = 0 V, AGND = DGND Output Amplifier: OP-07		LIMITS						UNIT	
				1=25°C 2=125,85,70°C 3=-55,-40,0°C		C, L, U GC, GL, GU GRADE		A, J, S B, K, T GRADE			
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>ACCURACY (Cont'd)</b>											
DC Supply Rejection	PSRR	$\Delta$ Gain / $\Delta$ V <sub>DD</sub> V <sub>DD</sub> = ±5%	1 2,3		-0.01 -0.02	0.01 0.02	-0.01 -0.02	0.01 0.02	% per %		
Output Leakage Current	I <sub>OUT(OFF)</sub>	All Digital Inputs = 0 V	1 2,3		-10 C,GC: -50 L,GL: -50 U,GU:-200	10 50 50 200	-10 A,B: -50 J,K: -50 S,T: -200	10 50 50 200	nA		
<b>DYNAMIC</b>											
Current Settling Time <sup>c</sup>	t <sub>S</sub>	To 0.5 LSB, Load = 100 Ω C <sub>EXT</sub> = 13 pF, CS = 0 V <sup>f</sup> Measured From Falling Edge of WR .	1,2,3			2		2	μs		
Propagation Delay <sup>c</sup>	t <sub>PD</sub>	Load = 100 Ω, C <sub>EXT</sub> = 13 pF <sup>f</sup>	1			250		250	ns		
Digital-to-Analog Glitch Impulse	I <sub>S</sub>	V <sub>REF</sub> = AGND Output Amplifier: LH0032 <sup>f</sup>	1	250					nV- sec		
AC Feedthrough at OUT <sup>g</sup>	FT	V <sub>REF</sub> = ±10 V 10 kHz Sinewave	1,2,3	1					mV p-p		
<b>REFERENCE</b>											
Reference Input Resistance (Pin 19 to GND)	R <sub>REF</sub>		1	10	7	25	7	25	kΩ		
R <sub>REFTC</sub>	R <sub>REFTC</sub>		1,2,3	-300					ppm/ °C		
<b>OUTPUT</b>											
Output Capacitance <sup>c</sup>	C <sub>OUT</sub>	$\overline{WR} = 0$ V CS = 0 V	1,2,3			70 150		70 150	pF		
<b>INPUT</b>											
Input HIGH Voltage	V <sub>IH</sub>		1,2,3		13.5		13.5		V		
Input LOW Voltage	V <sub>IL</sub>		1,2,3			1.5		1.5			
Input Current <sup>h</sup>	I <sub>IN</sub>	V <sub>IN</sub> = 0 V or V <sub>DD</sub>	1 2,3		-1 -10	1 10	-1 -10	1 10	μA		
Input Capacitance <sup>c</sup>	C <sub>IN</sub>	V <sub>IN</sub> = 0 V	DBO-DB11	1,2,3				5	5	pF	
			$\overline{WR}, \overline{CS}$	1,2,3					20		20

ELECTRICAL CHARACTERISTICS <sup>a</sup>										(15 Volt Operation)	
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = +15 V, V <sub>REF</sub> = +10 V V <sub>OUT</sub> = 0 V, AGND = DGND Output Amplifier: OP-07	LIMITS							UNIT	
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		C,L,U GC, GL, GU GRADE		A, J, S B, K, T GRADE				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>TIMING</b>											
Chip Select to Write Setup Time	t <sub>CS</sub>	See Timing Diagram Figure 1	1 2,3	120 150	180 200		180 200			ns	
Chip Select to Write Hold Time	t <sub>CH</sub>		1,2,3		0		0				
Write Pulse Width	t <sub>WR</sub>	t <sub>CS</sub> ≥ t <sub>WR</sub> , t <sub>CH</sub> ≥ 0	1 2,3	100 170	160 240		160 240				
Data Setup Time	t <sub>DS</sub>		1 2,3	60 80	90 120		90 120				
Data Hold Time	t <sub>DH</sub>		1,2,3		10		10				
<b>SUPPLY</b>											
V <sub>DD</sub> Range <sup>l</sup>	V <sub>DD</sub>		1,2,3		4.5	16.5	4.5	16.5	V		
Supply Current	I <sub>DD</sub>	All Digital Inputs V <sub>IH</sub> or V <sub>IL</sub>	1,2,3			2		2	mA		
		All Digital Input 0 V or V <sub>DD</sub>	1 2,3	0.01 0.01		0.1 0.5		0.1 0.5			

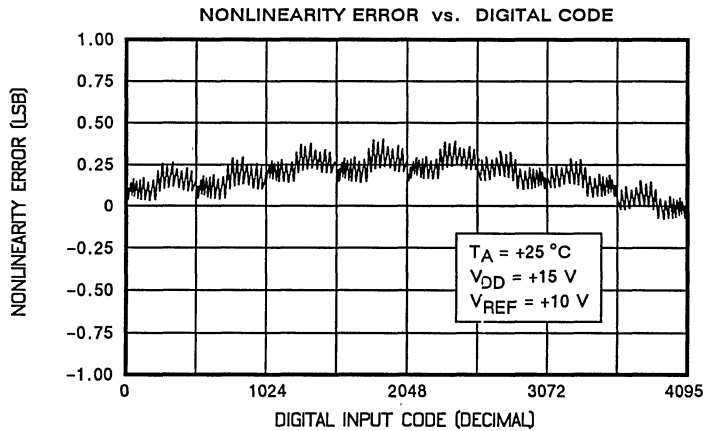
## NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- This includes the effect of 5 ppm max Gain TC.
- DB0-DB11 = 0 V to V<sub>DD</sub> or V<sub>DD</sub> to 0 V.
- Feedthrough can be further reduced by connecting the metal lid on the side braze package (Suffix D) to DGND.
- Logic inputs are MOS gates. Typical input current (+25 °C) is less than 1 nA.
- Accuracy is not guaranteed over this range.

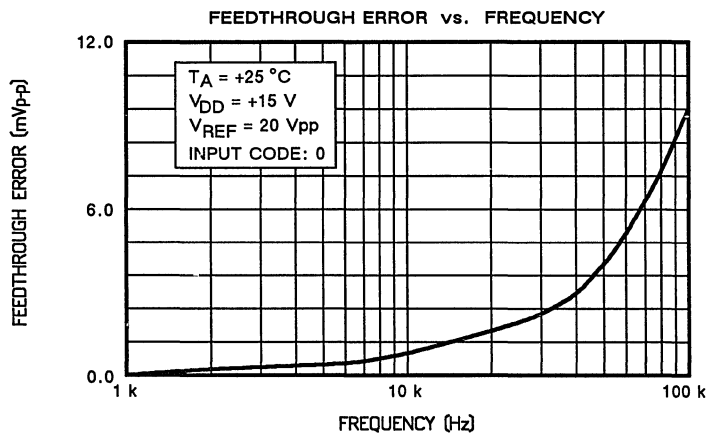
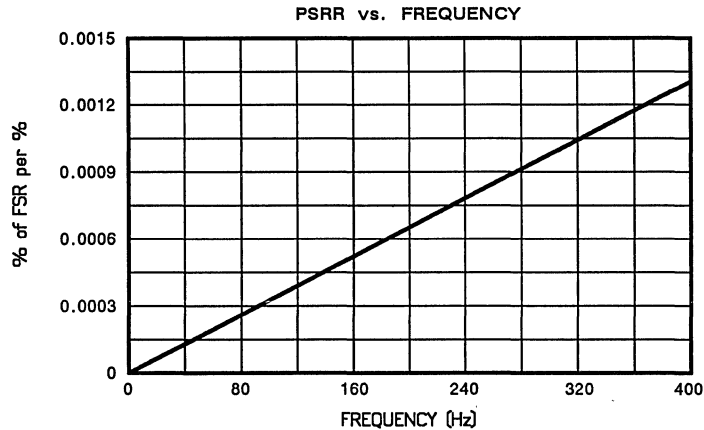
**DIE TOPOGRAPHY**



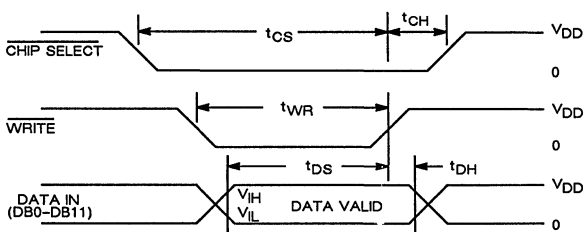
**TYPICAL CHARACTERISTICS**



## TYPICAL CHARACTERISTICS (Cont'd)



### WRITE CYCLE TIMING DIAGRAM



#### MODE SELECTION:

##### WRITE MODE:

$\overline{\text{CS}}$  and  $\overline{\text{WR}}$  low, DAC responds to data bus (DB0-DB11) inputs.

##### HOLD MODE:

Either  $\overline{\text{CS}}$  or  $\overline{\text{WR}}$  high, data bus (DB0-DB11) is locked out; DAC holds last data present when  $\overline{\text{WR}}$  or  $\overline{\text{CS}}$  assumed high state.

#### NOTES:

$V_{DD} = +5\text{ V}$ ;  $t_r = t_f = 20\text{ ns}$

$V_{DD} = +15\text{ V}$ ;  $t_r = t_f = 40\text{ ns}$

All input signal rise and fall times are measured from 10% to 90% of  $V_{DD}$ .

Timing measurement reference level is  $(V_{IH} + V_{IL})/2$ .

### CAUTION

ESD (Electro-Static-Discharge-Sensitive) device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy

electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

**DETAILED DESCRIPTION**

**D/A Converter Section**

Figure 1 shows a simplified circuit of the D/A converter section of the Si7545 and Figure 2 gives an approximate equivalent circuit. Note that the ladder termination resistor is connected to AGND. R is typically 10 kΩ.

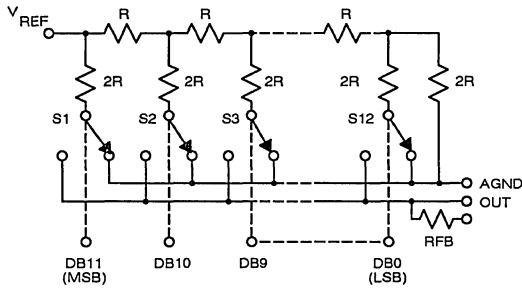


Figure 1. Simplified D/A Circuit of Si7545

The binary weighted currents are switched between the OUT bus line and AGND by n-channel SPDT analog switches, thus maintaining a constant current in each ladder leg independent of switch states.

The capacitance at the OUT bus line, C<sub>OUT</sub>, is code dependent and varies from 70 pF (all switches to AGND) to 150 pF (all switches to OUT).

One of the current switches is shown in Figure 2. The input resistance at V<sub>REF</sub> (Figure 1) is always equal to R<sub>REF</sub> (R<sub>REF</sub> is the R-2R ladder characteristic resistance and is equal to "R"). Since R<sub>REF</sub> at the V<sub>REF</sub> pin is constant, the reference terminal can be driven by a reference voltage or a reference current ac or dc, of positive

or negative polarity. (If a current source is used, a low temperature coefficient external R<sub>FB</sub> is recommended to define scale factor.)

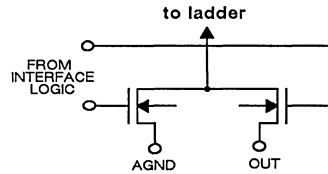


Figure 2. n-channel Current Steering Switch

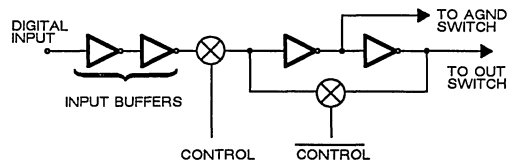


Figure 3. Digital Input Structure

The input buffers are simple CMOS inverters designed such that when the Si7545 is operated with V<sub>DD</sub> = 5 V, the buffers convert TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V<sub>IN</sub> is in the region of 2.0 to 3.5 V the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V<sub>DD</sub> and DGND) as is practically possible.

The Si7545 may be operated with any supply voltage in the range 4.5 V < V<sub>DD</sub> < 16.5 V. With V<sub>DD</sub> = 5 V the input logic levels are TTL compatible, otherwise they will be CMOS compatible only.

**APPLICATIONS**

Figures 4 and 5 show simple unipolar and bipolar circuits using the Si7545. Resistor R1 is used to trim for full scale (see Table 1). The top grade versions (Si7545GCQ, Si7545GLN, Si7545GUD), have a guaranteed maximum gain error of +1 LSB at 25°C, which allows the user to eliminate the gain trim resistors in many applications. Capacitor C1 provides phase compensation and helps prevent

overshoot and ringing when using high speed operational amplifiers. The circuits of Figures 4, 5, and 6 have constant input impedance at the V<sub>REF</sub> terminal.

The circuit of Figure 4 can be used as a fixed reference DAC so that it provides an analog output voltage in the range 0 V to -V<sub>IN</sub> (the inversion is introduced by the op amp); or V<sub>IN</sub> can be an ac

## APPLICATIONS (Cont'd)

signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier).

$V_{IN}$  can be any voltage in the range  $\pm 20$  V (provided the op amp can handle such voltages) since  $V_{REF}$  is permitted to exceed  $V_{DD}$ . Table 2 shows the code relationships for the circuit of Figure 4.

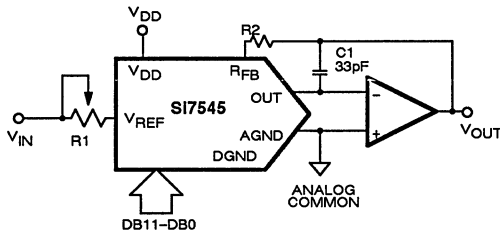


Figure 4. Unipolar Binary Operation

TABLE 1

TRIM RESISTOR	A, J, S	B, K, T	C, L, U	GC, GL, GU
R1	500	200	100	500
R2	150	68	33	150

Recommended Trim Resistor Values vs. Grade for  $V_{DD} = +5$  V

TABLE 2

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT ( $V_{OUT}$ )
1111	1111 1111	$-(4095/4096)V_{IN}$
1000	0000 0000	$-(2048/4096)V_{IN}$
0000	0000 0001	$-(1/4096)V_{IN}$
0000	0000 0000	0 VOLTS

Unipolar Binary Code Table for Circuit of Figure 4

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive-OR instruction and omitting the inverter. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wire-wound or

metal foil), so that their temperature coefficients match. Mismatch of R5 to R4 and R3 causes full scale error.

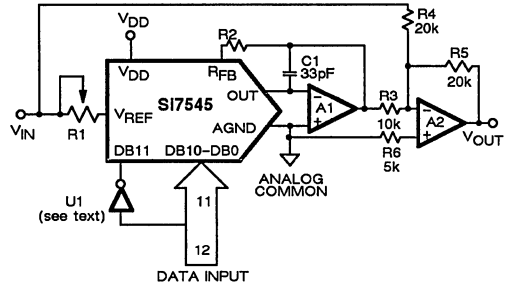


Figure 5. Bipolar Operation (2's Complement Code)

TABLE 3

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT ( $V_{OUT}$ )
0111	1111 1111	$+(2047/2048)V_{IN}$
0000	0000 0001	$+(1/2048)V_{IN}$
0000	0000 0000	0 VOLTS
1111	1111 1111	$-(1/2048)V_{IN}$
1000	0000 0000	$-V_{IN}$

2's Complement Code Table for Circuit of Figure 5

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with single plus magnitude code and has the advantage that it gives 12-bit resolution per quadrant for the circuit of Figure 5. The DG423 is a CMOS single-pole double-throw analog switch with data latches.

TABLE 4

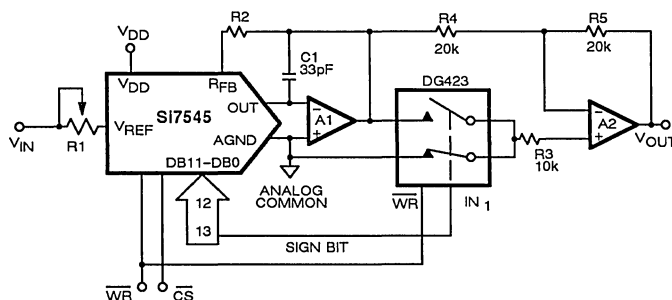
SIGN BIT	DIGITAL INPUT MSB	LSB	ANALOG OUTPUT ( $V_{OUT}$ )
0	1111	1111 1111	$+(4095/4096)V_{IN}$
0	0000	0000 0000	0 VOLTS
1	0000	0000 0000	0 VOLTS
1	1111	1111 1111	$-(4095/4096)V_{IN}$

Note: Sign Bit of "0" connects R3 to GND

12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6



**APPLICATIONS (Cont'd)**



**Figure 6.** 12-Bit Plus Sign Magnitude D/A Converter

**APPLICATION HINTS**

**OUTPUT OFFSET**

CMOS DACs exhibit a code dependent output resistance which in turn causes a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity is  $0.67 V_{OS}$  where  $V_{OS}$  is the amplifier input offset voltage. It is recommended that  $V_{OS}$  be no greater than 10% of 1 LSB over the operating temperature range to assure monotonic operation.

**GROUND MANAGEMENT**

Transient voltages or AC between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie them together at the Si7545. In more complex systems where the AGND and DGND tie on the back plane, it is recommended that two diodes (1N4148 or equivalent) be connected in inverse parallel between the Si7545 AGND and DGND pins.

**DIGITAL GLITCHES**

When  $\overline{WR}$  and  $\overline{CS}$  are both low the latches are transparent and the DAC inputs follow the data inputs. Some bus systems do not always have valid data for the whole period during which  $\overline{WR}$  is low and as a result invalid data can briefly appear at the DAC inputs during a write cycle. This can cause unwanted glitches at the DAC output. The solution to this problem, if it occurs, is to retime the write pulse  $\overline{WR}$  so that it only occurs when data is valid.

Another cause of glitches is capacitive coupling from the digital lines to the OUT and AGND terminals. This can be minimized by screening the analog pins (Pins 1,2,19,20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the Si7545. Note how the analog pins are at one end of the package and separated from the digital pins by  $V_{DD}$  and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections, particularly in circuits with high currents and fast rise and fall times.

This type of crosstalk is minimized by using the Si7545 with a  $V_{DD} = 5 V$ . Great care should be taken to ensure that the 5 V used to power up the Si7545 is properly filtered and free from digitally induced noise.

**TEMPERATURE COEFFICIENTS**

The gain temperature coefficient of the Si7545 has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. this corresponds to worst case gain shifts of 2 LSB's and 0.8 LSB, respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account.

**SINGLE SUPPLY OPERATION**

The ladder termination resistor of the Si7545 (Figure 1) is connected to AGND. This arrangement is particularly suitable for single supply operation because OUT and AGND may be biased at a voltage between DGND and  $V_{DD}$ . OUT and AGND should

## APPLICATION HINTS (Cont'd)

never go more than 0.3 volts less than DGND or an internal diode will be turned on and a heavy current may flow which will damage the device. (The Si7545 is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices.)

Figure 7 shows the Si7545 connected in a voltage switching mode. OUT is connected to the reference voltage and AGND is connected to DGND. The DAC output voltage is available at the  $V_{REF}$  pin and has a constant output impedance equal to  $R$ .  $R_{FB}$  is not used in this circuit.

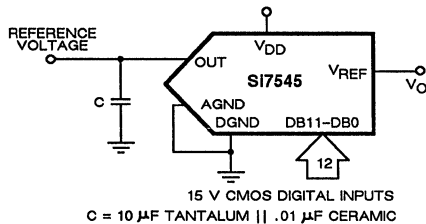
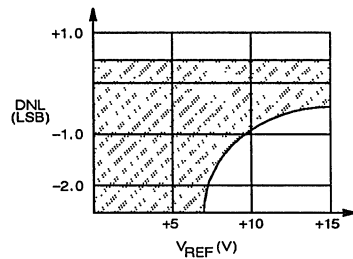


Figure 7. Voltage Switching Mode

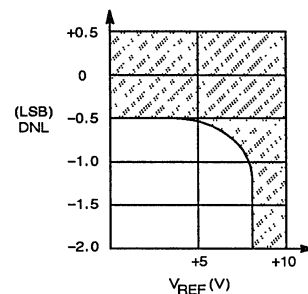
The loading of the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage to the changing load conditions. Good results can be obtained by decoupling  $V_{REF}$  with a 10  $\mu\text{F}$  tantalum capacitor in parallel with a 0.01  $\mu\text{F}$  ceramic.

To maintain linearity the voltages at OUT and AGND should remain within 2.5 volts of each other, for a  $V_{DD}$  of 15 V. If  $V_{DD}$  is reduced from 15 V or the differential voltage between OUT and AGND is increased to more than 2.5 V, the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded. Figures 8 and 9 show typical curves illustrating this effect for various values of reference voltage and  $V_{DD}$ . If the output voltage is required to be offset from ground by some value, then OUT and AGND may be biased up. The effect on linearity and differential nonlinearity will be the same as reducing  $V_{DD}$  by the amount of the offset.



Differential NonLinearity vs.  $V_{DD}$  for Figure 7 Circuit. Reference voltage = 2.5 V. Shaded area shows the range of values that typically occur for the L and U grades.

Figure 8.



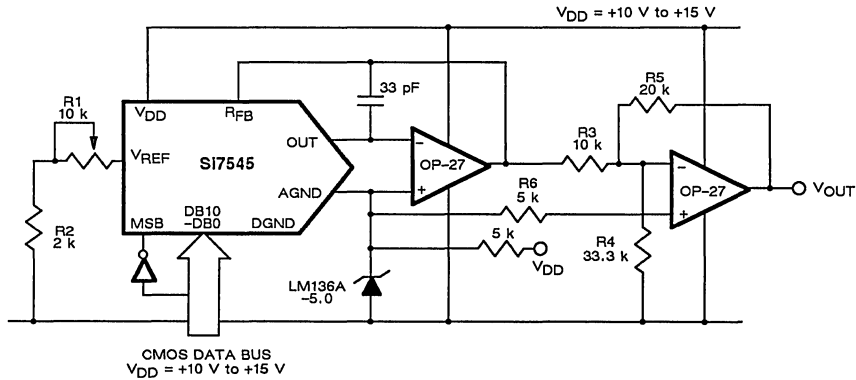
Differential NonLinearity vs.  $V_{DD}$  for Figure 7 Circuit. Reference voltage = 15 V. Shaded area shows the range of values that typically occur for the L and U grades.

Figure 9.

The circuits of Figures 4, 5 and 6 can all be converted to single supply operation by biasing AGND to some voltage between  $V_{DD}$  and DGND. Figure 10 shows the 2's complement bipolar circuit of Figure 5 modified to give a range from 2 V to 8 V about a "Pseudo-analog ground" of 5 V.

This voltage range would allow operation from a simple  $V_{DD}$  of 10 V to 15 V. The LM136A-5.0 voltage reference fixes AGND at 5 V.  $V_{IN}$  is set at 2 V by means of the series resistors  $R_1$  and  $R_2$ . There is no need to buffer the  $V_{REF}$  input to the Si7545 with an amplifier because the input impedance of the DAC is constant. Note however, that since the temperature coefficient of the D/A reference input resistance is typically  $-300 \text{ ppm}/^\circ\text{C}$ , applications which experience wide temperature variations may require a buffer amplifier to generate the 2.0 V at the  $V_{REF}$  pin. Other output voltage ranges can be obtained by

**APPLICATION HINTS (Cont'd)**



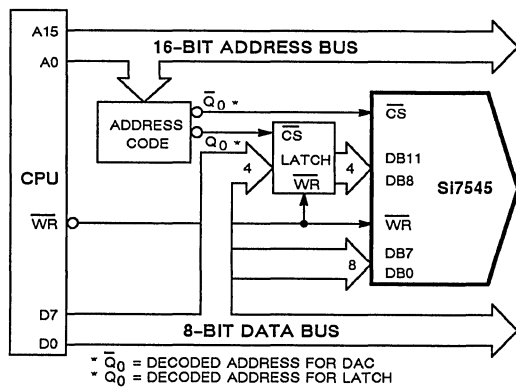
**Figure 10.** Single Supply "Bipolar" 2's Complement DAC

changing R4 to shift the zero point and (R1 + R2) to change the slope, or gain of the D/A transfer function. VDD must be kept at least 4.5 V about OUT to ensure that linearity is preserved.

**MICROPROCESSOR INTERFACING**

The Si7545 can interface directly to either 8- or 16-bit microprocessors via its 12-bit wide data latch using standard CS and WR control signals.

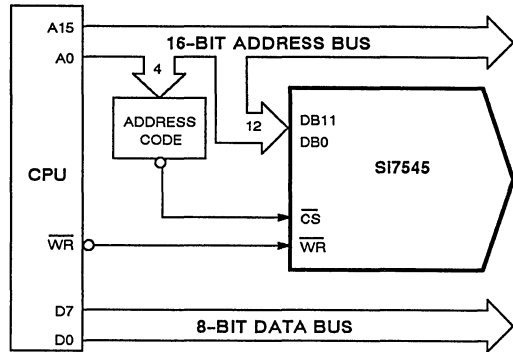
A typical interface circuit for an 8-bit processor is shown in Figure 11. This arrangement uses two memory addresses, one for the lower 8-bits of data and one for the upper 4-bits of data into the DAC via the latch.



**Figure 11.** 8-Bit Processor to Si7545 Interface

Figure 12 shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower address lines of the processor's address bus to supply data to the DAC, thus each Si7545 connected in this way uses 4 k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12-bits contain the data for the DAC and the upper 4-bits contain the address of the 4k block at which the DAC resides.

**6**

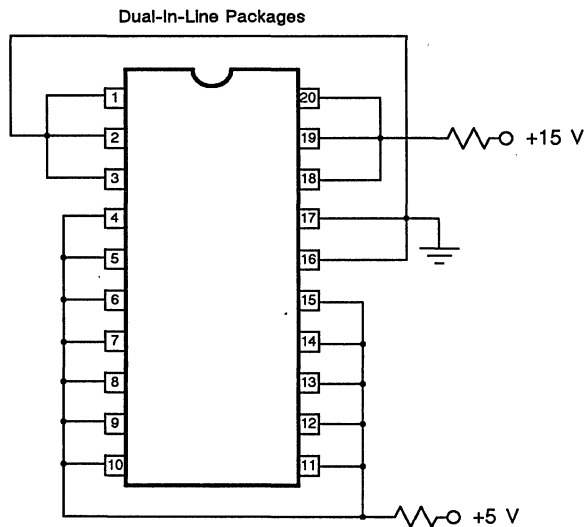


**Figure 12.** Connecting the Si7545 to an 8-Bit Microprocessor via the Address Bus

## PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
1	OUT	Current Output
2	AGND	Analog Ground
3	DGND	Digital Ground
4	DB11	Digital Input (Bit 11 MSB)
5	DB10	Digital Input (Bit 10)
6	DB9	Digital Input (Bit 9)
7	DB8	Digital Input (Bit 8)
8	DB7	Digital Input (Bit 7)
9	DB6	Digital Input (Bit 6)
10	DB5	Digital Input (Bit 5)
11	DB4	Digital Input (Bit 5)
12	DB3	digital Input (Bit 3)
13	DB2	Digital Input (Bit 2)
14	DB1	Digital Input (Bit 1)
15	DB0	Digital Input (Bit 0)
16	$\overline{CS}$	Chip Select Input
17	$\overline{WR}$	Write Input
18	$V_{DD}$	Positive Power Supply
19	$V_{REF}$	Reference Input Voltage
20	$R_{FB}$	Internal Feedback Resistor

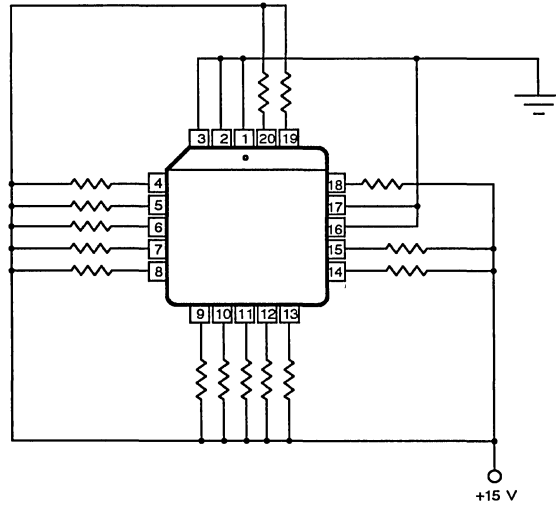
## BURN-IN CIRCUIT



Note: All Resistors are 1 k $\Omega$  unless otherwise specified

## BURN-IN CIRCUIT (Cont'd)

PLCC Package



Note: All resistors are 1 k $\Omega$  unless otherwise specified

# Si7820

## CMOS Subranging 8-Bit A/D Converter

### FEATURES

- Fast Conversion Time  
1.34  $\mu$ s Maximum
- 1/2 LSB Total Unadjusted Error
- Single +5 V Supply
- On-Board  $\mu$ P Interface

### BENEFITS

- Increased Data Throughput
- No Accuracy Trims Required
- Simplified Power Supply Requirements
- Simplified  $\mu$ P Interface

### APPLICATIONS

- Digital Signal Processing
- High Speed Data Acquisition
- 5 Volt Systems
- $\mu$ P Controlled Servos

### DESCRIPTION

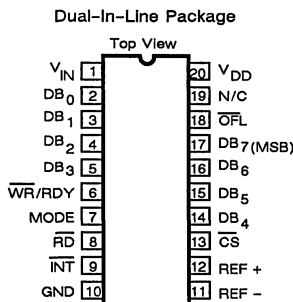
The Si7820 is a high speed, microprocessor compatible, 8-bit analog-to-digital converter which uses a subranging (half-flash) technique to achieve a conversion time of 1.34  $\mu$ s. The converter has a 0 V to +5 V analog input range and uses a single +5 V supply.

The Si7820 will easily interface with microprocessors by appearing as a memory location or I/O port without the need for external interfacing logic. The data outputs use latched, three-state buffers to allow direct connection to a microprocessor data bus or system input port. An over-flow output is provided for cascading devices to achieve higher resolution. The Si7820 is pin compatible with the industry-standard AD7820 and ADC0820 devices.

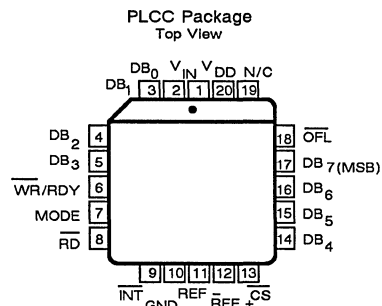
Applications include high speed data acquisition, real-time digital signal processing, FAX communications systems, oversampled audio digitizing, and digital servo systems such as head positioning for disk drives.

The Si7820 is built using the Siliconix proprietary PolyMOS process, allowing a mix of high density fast digital logic with high performance analog circuitry. An epitaxial layer prevents latchup. It is available in the 20-pin PDIP and PLCC-20 for operation over the commercial K, L suffix (0 to 70°C), 20-pin CerDIP for industrial, B, C suffix (-40 to 85°C) temperature range, and for military, T, U suffix (-55 to 125°C) temperature operation.

### PIN CONFIGURATION

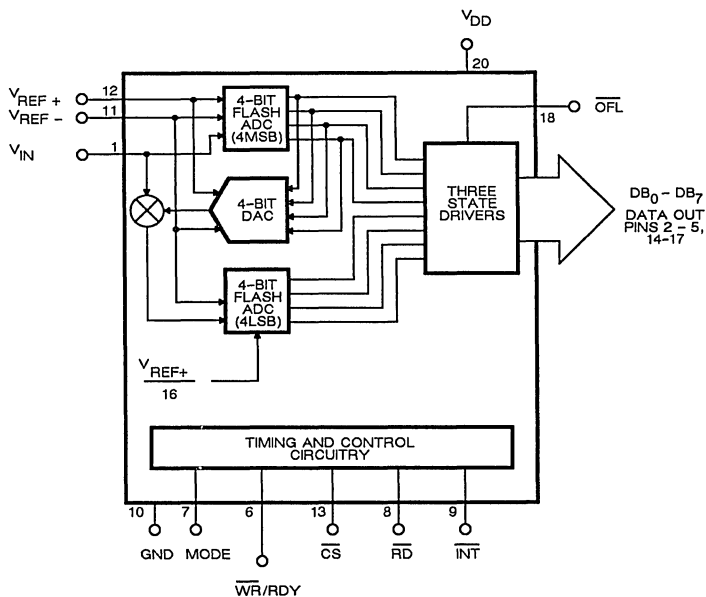


Order Number:  
SI7820



Order Number:  
SI7820

**FUNCTIONAL BLOCK DIAGRAM**



**ORDERING INFORMATION**

PART	TEMP. RANGE	PACKAGE*	ERROR
Si7820LN	0 to 70°C	Plastic DIP	+1/2 LSB
Si7820KN	0 to 70°C	Plastic DIP	+1 LSB
Si7820LP	0 to 70°C	PLCC	+1/2 LSB
Si7820KP	0 to 70°C	PLCC	+1 LSB
Si7820CQ	-40 to 85°C	CerDIP	+1/2 LSB
Si7820BQ	-40 to 85°C	CerDIP	+1 LSB
Si7820UQ	-55 to 125°C	CerDIP	+1/2 LSB
Si7820TQ	-55 to 125°C	CerDIP	+1 LSB

\* All devices -- 20 lead packages.  
\*\* Consult factory for dice specifications.

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage,  $V_{DD}$  to GND ..... 0 V, 10 V  
 Voltage at any other pins  
 (Pins 1-9, 11-18) ..... GND -0.3 V,  $V_{DD}$  +0.3 V  
 Power Dissipation (Any Package) to 75°C ..... 450 mW  
 Derate Above 75°C by ..... 6mW/°C

Operating Temperature Ranges  
 Si7820LN/KN/LP/KP ..... 0 to 70°C  
 Si7820BQ/CQ ..... -40 to 85°C  
 Si7820TQ/UQ ..... -55 to 125°C  
 Storage Temperature Range ..... -65 to 160°C  
 Lead Temperature (Soldering 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 5\text{ V}$ , $V_{REF+} = 5\text{ V}$ $V_{REF-} = 0\text{ V}$ , RD-Mode GND = 0 V	LIMITS						UNIT		
			1=25°C		2=125,85,70°C		T, U SUFFIX -55 to 125°C			B, C, K, L SUFFIX	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>ACCURACY</b>											
Resolution		No Missing Codes	1,2,3		8		8		Bits		
Total Unadjusted Error <sup>e</sup>		L, C, U Grades	1,2,3		-1/2	1/2	-1/2	1/2	LSB		
		B, K, T Grades	1,2,3		-1	1	-1	1			
<b>REFERENCE INPUT</b>											
Reference Input Resistance	$R_{IN}$		1 2,3	2.2	1.4 1.25	4.0 4.0	1.4 1.25	4.0 4.0	k $\Omega$		
$V_{REF+}$ Input Voltage Range			1,2,3		0	5.1	0	5.1	V		
$V_{REF-}$ Input Voltage Range			1,2,3		-0.1	5.1	-0.1	5.1			
<b>ANALOG INPUT</b>											
Analog Input Range	$V_{INR}$		1,2,3		-0.1	5.1	-0.1	5.1	V		
Analog Input Capacitance	$C_{VIN}$		1	45					pF		
Analog Input Current	$I_{VIN}$	$V_{IN} = 0\text{ V to }5\text{ V}$	1 2,3		-0.3 -3	0.3 3	-0.3 -3	0.3 3	$\mu\text{A}$		
Slew Rate <sup>f</sup>	SR		1	0.2		0.1		0.1	V/ $\mu\text{s}$		
<b>LOGIC INPUTS</b>											
Input HIGH Voltage	$V_{INH}$	$\overline{\text{CS}}$ , $\overline{\text{WR}}$ , $\overline{\text{RD}}$ Inputs	1,2,3		2.4		2.4		V		
		Mode Input	1,2,3		3.5		3.5				
Input LOW Voltage	$V_{INL}$	$\overline{\text{CS}}$ , $\overline{\text{WR}}$ , $\overline{\text{RD}}$ Inputs	1,2,3			0.8		0.8	V		
		Mode Input	1,2,3			1.5		1.5			
Input HIGH Current	$I_{INH}$	$\overline{\text{CS}}$ , $\overline{\text{RD}}$ Inputs	1 2,3			0.3 1.0		0.3 1.0	$\mu\text{A}$		
		$\overline{\text{WR}}$ Input	1 2,3			0.3 3.0		0.3 3.0			
		Mode Input	1 2,3	50		150 200		150 200			



## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 5\text{ V}$ , $V_{REF+} = 5\text{ V}$ $V_{REF-} = 0\text{ V}$ , RD-Mode $GND = 0\text{ V}$	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		T, U SUFFIX -55 to 125°C		B, C, K, L SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>LOGIC INPUTS (Cont'd)</b>									
Input LOW Current	$I_{INL}$	$\overline{CS}$ , $\overline{WR}$ , $\overline{RD}$ Mode Inputs	1 2,3		-0.3 -1.0		-0.3 -1.0		$\mu\text{A}$
Input Capacitance <sup>c</sup>	$C_{IN}$		1,2,3	5		8		8	pF
<b>LOGIC OUTPUTS</b>									
Output HIGH Voltage DB0-DB7, $\overline{OFL}$ , INT Outputs	$V_{OH}$	$V_{DD} = 4.75\text{ V}$	$I_{OUT} = -360\ \mu\text{A}$	1,2,3		4.0		4.0	V
			$I_{OUT} = -10\ \mu\text{A}$	1,2,3		4.5		4.5	
Output LOW Voltage DB0-DB7, $\overline{OFL}$ , INT RDY	$V_{OL}$		$I_{OUT} = 1.6\ \text{mA}$	1,2,3			0.4		
Three-State Current DB0-DB7, RDY			1 2,3		-0.3 -3.0	0.3 3.0	-0.3 -3.0	0.3 3.0	$\mu\text{A}$
Output Source Current DB0-DB7, $\overline{OFL}$ , INT	$I_{SRC}$	$V_{OUT} = 0$	1,2,3	-25	-10		-10		mA
Output Sink Current DB0-DB7, $\overline{OFL}$ , INT RDY	$I_{SINK}$	$V_{OUT} = V_{DD}$	1,2,3	40	15		15		
Output Capacitance <sup>c</sup> DB0-DB7, $\overline{OFL}$ , INT RDY	$C_{OUT}$		1,2,3	5		8		8	pF
<b>POWER SUPPLY</b>									
Supply Voltage	$V_{DD}$	5 V $\pm 5\%$ for Specified Performance	1,2,3		4.75	5.25	4.75	5.25	V
Supply Current	$I_{DD}$	$\overline{CS} = \overline{WR} = \overline{RD} = 0$	1 2,3	5		10 15		10 15	mA
Power Dissipation			1	25					
Power Supply Sensitivity	PSS	$V_{DD} = 5\text{ V} \pm 5\%$	1,2,3	$\pm 1/16$	$-1/4$	$1/4$	$-1/4$	$1/4$	LSB
<b>TIMING <sup>f,g</sup></b>									
$\overline{CS}$ to $\overline{RD}$ , $\overline{WR}$ Setup Timing	$t_{CSS}$		1,2,3		0		0		ns
$\overline{CS}$ to $\overline{RD}$ , $\overline{WR}$ Hold Time	$t_{CSH}$		1,2,3		0		0		
$\overline{CS}$ to $\overline{RDY}$ Delay	$t_{RDY}$	$C_L = 50\ \text{pF}$ , $R = 3\ \text{k}\Omega$	1 2,3	35		70 100		70 90	
Conversion Time (RD Mode)	$t_{ORD}$		1 2,3	1.2		1.6 2.5		1.6 2.0	$\mu\text{s}$

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = 5 V, V <sub>REF+</sub> = 5 V V <sub>REF-</sub> = 0 V, RD-Mode GND = 0 V	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		T, U SUFFIX -55 to 125°C		B, C, K, L SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>TIMING <sup>f,g</sup> (Cont'd)</b>									
Data Access Time <sup>h</sup> (RD Mode)	t <sub>ACC0</sub>	See Figure 4	1 2,3	t <sub>CRD+10</sub>		t <sub>CRD+20</sub> t <sub>CRD+50</sub>		t <sub>CRD+20</sub> t <sub>CRD+35</sub>	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	t <sub>INTH</sub>	C <sub>L</sub> = 50 pF	1 2,3	60		125 225		125 175	
Data Hold Time <sup>i</sup>	t <sub>DH</sub>		1 2,3	40		60 100		60 80	
Delay Time Between Conversions	t <sub>P</sub>		1 2,3		500 600		500 600		
Write Pulse Width	t <sub>WR</sub>		1,2,3		0.6	50	0.6	50	μs
Conversion Time (WR / RD Mode)	t <sub>CWR-RD</sub>		1 2,3		1.34 1.53		1.34 1.50		
Delay Between WR and RD Pulses	t <sub>RD</sub>		1 2,3		600 700		600 700		ns
Data Access Time (WR / RD Mode) <sup>h</sup>	t <sub>ACC1</sub>	t <sub>RD</sub> < t <sub>INTL</sub> See Figure 6	1 2,3	110		160 250		160 225	
$\overline{RD}$ to $\overline{INT}$ Delay	t <sub>RI</sub>		1 2,3	100		140 225		140 200	
$\overline{WR}$ to $\overline{INT}$ Delay	t <sub>INTL</sub>		1 2,3	600		1000 1700		1000 1400	
Data Access Time (WR / RD Mode) <sup>h</sup>	t <sub>ACC2</sub>	t <sub>RD</sub> > t <sub>INTL</sub> See Figure 5	1 2,3	60		70 110		70 90	
$\overline{WR}$ to $\overline{INT}$ Delay (Stand-Alone)	t <sub>IHW</sub>	C <sub>L</sub> = 50 pF	1 2,3	70		100 150		100 130	
Data Access Time After INT	t <sub>ID</sub>			10		50 75		50 65	

## NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Total unadjusted error includes offset, full-scale and linearity errors.
- Sample tested at 25°C to ensure compliance.
- All input control signals are specified with t<sub>R</sub> = t<sub>F</sub> = 20 ns (10% to 90% of 5 V).
- Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
- Defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

**SWITCHING TIME TEST CIRCUITS**

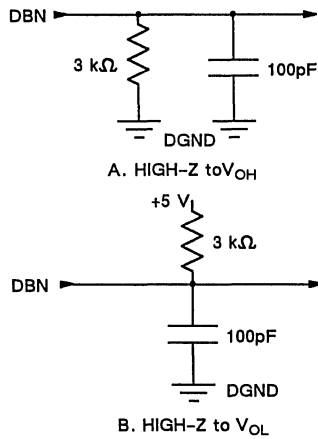


Figure 1. Load Circuits for Data Access Time Test

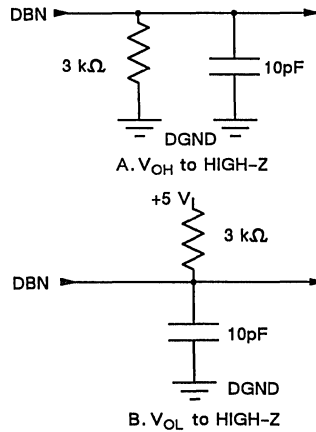


Figure 2. Load Circuits for Data Hold Time Test

**CAUTION**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the

operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

**PIN DESCRIPTION**

PIN NUMBER	SYMBOL	DESCRIPTION
1	$V_{IN}$	Analog input; range = $GND < V_{IN} < V_{DD}$ .
2	DB0	Three-state data output, bit 0 (LSB).
3	DB1	Three-state data output, bit 1.
4	DB2	Three-state data output, bit 2.
5	DB3	Three-state data output, bit 3.
6	$\overline{WR}/RDY$	WRITE control input/READY status output. See Digital Interface section.
7	MODE	Mode selection input. This input is internally pulled low with a 50 $\mu A$ current source. RD Mode: MODE low/open. WR-RD Mode: MODE high.
8	$\overline{RD}$	READ input. $\overline{RD}$ must be low to access data. See Digital Interface section.
9	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
10	GND	Ground.
11	$V_{REF-}$	Lower limit of reference span. Sets the zero code voltage. Range: GND to $V_{REF+}$ .

## PIN DESCRIPTION (Cont'd)

PIN NUMBER	SYMBOL	DESCRIPTION
12	$V_{REF+}$	Upper limit of reference span. Sets the Full Scale input voltage. Range: $V_{REF-}$ to $V_{DD}$ .
13	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to recognize $\overline{WR}$ or $\overline{RD}$ inputs.
14	DB4	Three-state data output, bit 4.
15	DB5	Three-state data output, bit 5.
16	DB6	Three-state data output, bit 6.
17	DB7	Three-state data output, bit 7 (MSB).
18	$\overline{OFL}$	Overflow Output. If the analog input is greater than $V_{REF+}$ , $\overline{OFL}$ will be high at the end of the conversion. It can be used to cascade two or more devices to increase resolution.
19	NC	No Connection.
20	$V_{DD}$	Power supply voltage, +5 V.

## DETAILED DESCRIPTION

## Converter Operation

The Si7820 uses a "half-flash" conversion technique (see Functional Block Diagram). Two 4-bit flash A/D converter sections are used to achieve an 8-bit result. Using 15 comparators, the upper 4-bit MS (most significant) flash A/D compares the unknown input voltage to the reference ladder and provides the upper four data bits.

An internal DAC uses the MS bits to generate the analog result from the first flash conversion, and generates a residue voltage which is the difference of the unknown input and the DAC voltage. The residue is then compared to the reference ladder using 15 LS (least significant) flash comparators to obtain the lower four bits of the output. An additional overrange comparator detects if the analog input is greater than the reference voltage.

## Operating Sequence

The operating sequence for the WR-RD Mode is shown in Figure 3. The conversion is initiated by a falling edge of  $\overline{WR}$ . The comparator inputs track the analog input voltage for the duration of  $\overline{WR}$  low. A minimum of 600 ns is required for the input voltage to be acquired. When  $\overline{WR}$  returns high, the MS flash result is latched into the output buffers and the LS conversion begins.  $\overline{INT}$  goes low approximately

600 ns later, indicating end of conversion, and that the lower 4 data bits are latched into the output buffers.  $\overline{RD}$  going low then accesses the data.

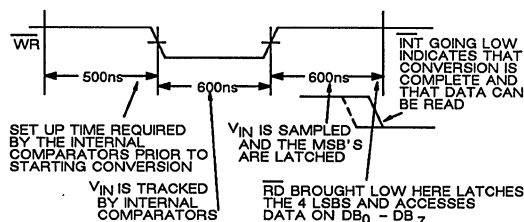


Figure 3. Operating Sequence (WR-RD Mode)

If an externally controlled conversion time is required, the  $\overline{RD}$  line can be brought low as soon as 600 ns after  $\overline{WR}$  goes high. This will latch the lower 4 data bits and output the conversion result on  $DB_0 - DB_7$ . At least 500 ns setup time is required from  $\overline{INT}$  going low to the start of another conversion ( $\overline{WR}$  going low).

**DETAILED DESCRIPTION (Cont'd)**

**Digital Interface**

The Si7820 has two basic interface modes which are set by the status of the MODE input pin. When this pin is low, the converter is in the RD mode, when this pin is high the converter is set up for the WR-RD mode.

**RD Mode**

In RD mode, conversion control and data access is controlled by the RD input (see Figure 4). The conversion is initiated by taking RD low. RD is then kept low until output data appears. This mode is useful for microprocessors which can be forced into a WAIT state. The processor can start a conversion, wait, and then read data with a single READ instruction.

Pin 6 (WR/RDY) is configured as a status output (RDY) in RD mode. This output can be used to drive the READ or WAIT input of a processor. RDY is an open drain output (with no internal pull-up device) which goes low after the falling edge of CS and goes high impedance at the end of the conversion. An INT output is also provided which goes low at the end of the conversion and returns high on the rising edge of CS or RD.

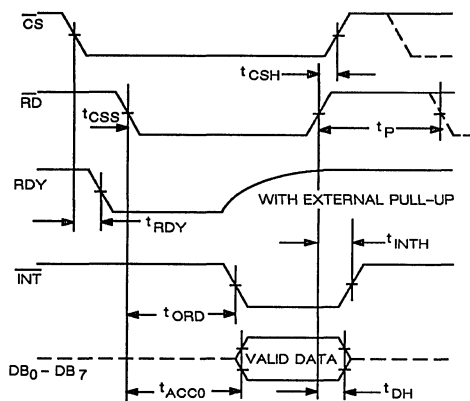


Figure 4. RD Mode Timing

**WR-RD Mode**

In the WR-RD mode, pin 6 (WR/RDY) is configured as the WRITE input for the converter. With CS low, a

conversion is initiated on the falling edge of WR. Several options exist for reading the data from the converter.

**Using Internal Delay**

In the first of these options the processor waits for INT output to go low before reading the data (Figure 5). INT typically goes low 600 ns after the rising edge of WR, indicating that the conversion is complete and the result is available in the output latch. With CS low, data outputs DB0-DB7 can be accessed by pulling RD low. INT is then reset by the rising edge of CS or RD.

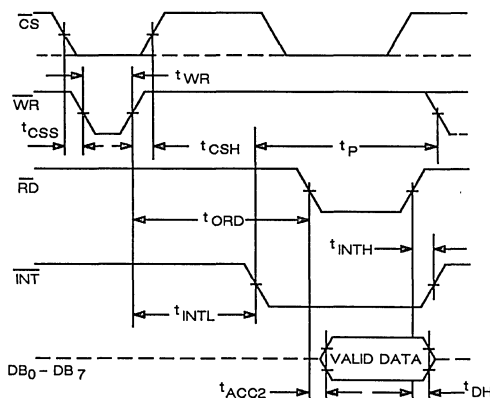


Figure 5. WR-RD Mode Timing ( t<sub>RD</sub> > t<sub>INTL</sub> )

**Reading Before Delay**

An alternative option can be used to externally control the conversion time (see Figure 6). The internally generated 600 ns delay varies somewhat with temperature and supply voltage (see Typical Operating Characteristics) and can be overridden with RD. To achieve this, the status of INT is ignored and RD is brought low as soon as 600 ns after the rising edge of WR. This completes the conversion and enables the output buffers, DB0-DB7, which contain the conversion result. INT also goes low after the falling edge of RD and is reset on the rising edge of RD or CS.

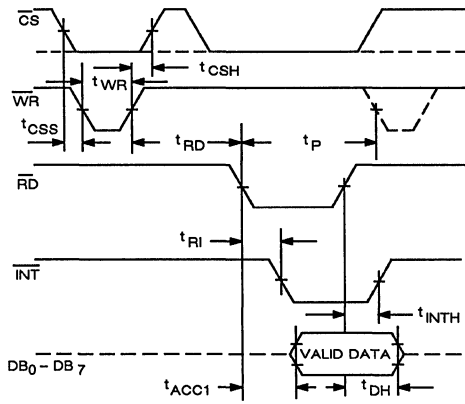


Figure 6. WR-RD Mode Timing (  $t_{RD} > t_{INTL}$  )

**Pipelined Operation**

In addition to the two standard WR-RD mode options, "pipe-lined" operation can be achieved by tying WR and RD together (see Figure 7). With CS low, WR and RD going low initiates a conversion, and reads the result of the previous conversion at the same time.

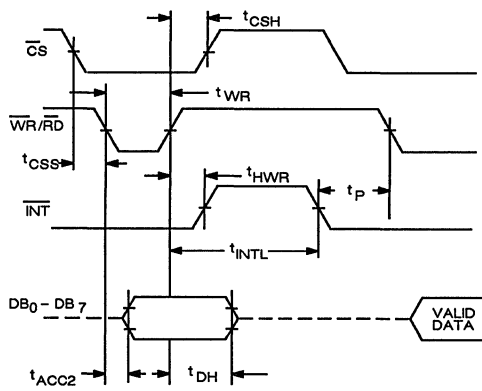


Figure 7. WR-RD Mode Pipe-Lined Timing  $\overline{WR} = \overline{RD}$

**Stand-Alone Operation**

The converter can also be used in a stand-alone operation (see Figure 8). CS and RD are tied low

and a conversion is initiated by pulling WS low. Output data is valid approximately 600 ns after the rising edge of WR.

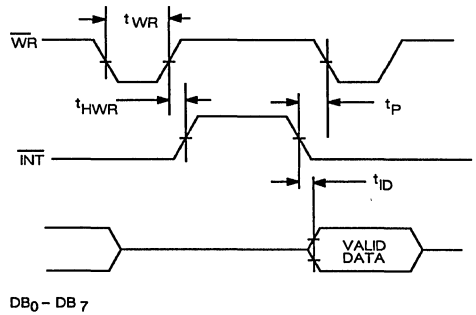


Figure 8. WR-RD Mode Stand-Alone Timing  $\overline{CS} = \overline{RD} = 0$

**Analog Considerations**

The VREF+ and VREF- input set the full-scale and zero input voltages of the A/D. In other words, the voltage at VREF- defines the input which produces an output code of all zeroes and the voltage at VREF+ defines the input which produces an output code of all ones (see Figure 9).

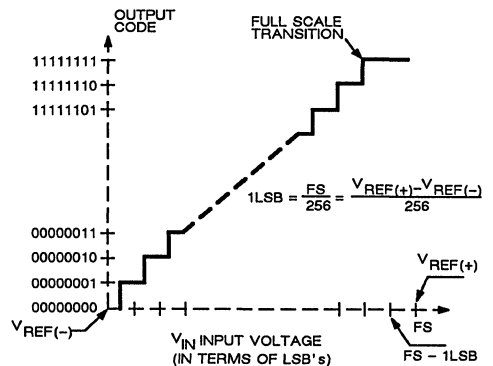


Figure 9. Transfer Function

**DETAILED DESCRIPTION (Cont'd)**

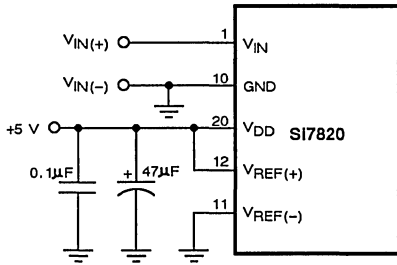


Figure 10a. Power Supply as Reference

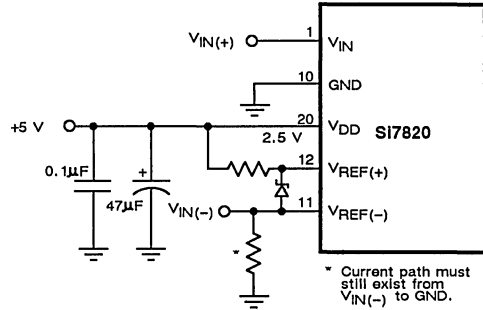


Figure 10b. Input Not Referenced to GND

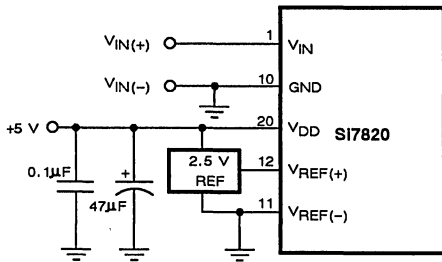


Figure 10c. External Reference 2.5 V Full-Scale

## 8-Bit Data Acquisition Systems

### FEATURES

- Total Unadjusted Error < 1/2 LSB (Si8603)
- Fast Conversion Time (25  $\mu$ s maximum)
- Low Power (2.5 mW)
- On-Chip S/H Function
- On-Board 8-Channel Multiplexer (Si8601)
- Microprocessor Interface

### BENEFITS

- Eliminates External Trims
- Increased Data Throughput
- Reduced System Power Consumption
- Reduced Aperture Error
- Eliminates Additional Supplies
- Reduced Board Space and Component Count

### APPLICATIONS

- $\mu$ P/PC-Based Data Acquisition Systems
- Voice/Telecom Systems
- Battery-Operated Systems
- Audio Digitizing
- Remote Data Acquisition
- High Density Systems

### DESCRIPTION

The Si8601 and Si8603 are 8-bit data acquisition systems which include an A/D converter, sample-and-hold function, and a microprocessor interface on one monolithic chip. The Si8603 is a single-channel version, while the Si8601 includes an on-board 8-channel analog multiplexer and decode logic to form a complete 8-channel data acquisition system. The Si8601 and Si8603 are designed for 5 V single-supply operation and TTL-level logic interfacing. For 15 V operation, refer to the Si8602/8604 data sheet.

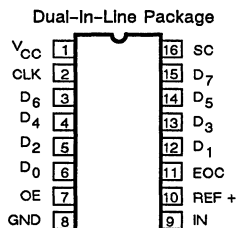
Built in the Siliconix proprietary PolyMOS™ process, the Si8601/8603 use a capacitive-ladder A/D conversion technique to achieve low power, high speed and less than 1/2 LSB total unadjusted error without the need for thin film resistors or laser trimming. The capacitive ladder architecture creates an on-board sample/hold function,

reducing the aperture time of the converter to less than 90 ns. This facilitates digitizing rapidly-slewing analog signals with a minimum of error. An epitaxial layer prevents latchup.

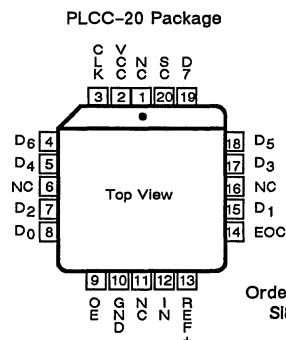
The total unadjusted error specification of 1/2 LSB (Si8603) eliminates the need for any external trims or adjustments, further reducing system cost and enhancing overall reliability.

The Si8601 is available in 28-pin plastic and ceramic DIP. The Si8603 is available in 16-pin plastic and ceramic DIP. Both are available in industrial, D suffix (-40 to 85°C) and military, A suffix (-55 to 125°C) temperature ranges and in /883 versions as well. For surface mount applications, the Si8601 is available in the PLCC-28, and the Si8603 in the PLCC-20. For more information on the Si8601, please refer to Siliconix application Note AN83-13.

### PIN CONFIGURATION



Order Numbers:  
CerDIP: Si8603DJ  
Plastic: Si8603AK, Si8603DK

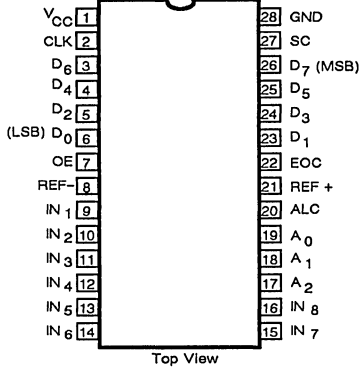


Order Number:  
Si8603DN



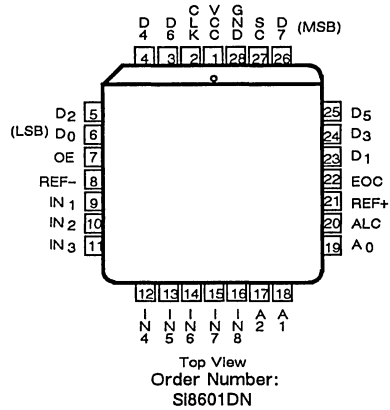
## PIN CONFIGURATION (Cont'd)

Dual-In-Line Package



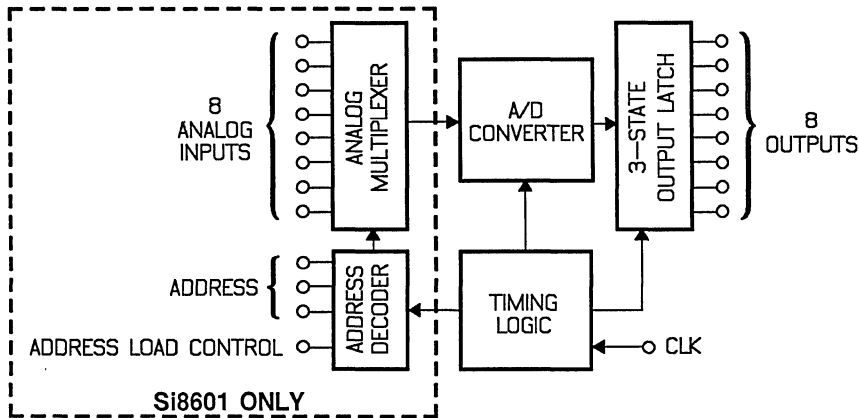
Order Numbers:  
CerDIP: Si8601AK  
          Si8601DK  
Plastic: Si8601DJ

PLCC-28 Package



Top View  
Order Number:  
Si8601DN

## FUNCTIONAL BLOCK DIAGRAM



**6**

## ABSOLUTE MAXIMUM RATINGS

Reference Input Voltage Range, $V_{REF-}$ .....	-0.3 V to $V_{REF+}$
Reference Input Voltage Range, $V_{REF+}$ .....	$V_{REF-}$ to $V_{CC} + 0.3$ V
Supply Voltage, $V_{CC}$ .....	6.5 V
Input Voltage Range, All Inputs .....	-0.3 V to $V_{CC} + 0.3$ V
Storage Temperature (K Suffix) .....	-65 to 150°C
(J, N Suffix) .....	-65 to 150°C
Operating Temperature (A Suffix) .....	-55 to 125°C
(D Suffix) .....	-40 to 85°C

Power Dissipation (Package)*	
28-Pin Ceramic DIP**	1046 mW
16-Pin Ceramic DIP***	900 mW
28-Pin Plastic DIP****	1046 mW
16-Pin Plastic DIP*****	900 mW
28-Pin PLCC*****	900 mW
20-Pin PLCC*****	900 mW

- \* All leads welded or soldered on PC Board.
- \*\* Derate 6.5 mW/°C above 25°C.
- \*\*\* Derate 12 mW/°C above 75°C.
- \*\*\*\* Derate 6.5 mW/°C above 25°C.
- \*\*\*\*\* Derate 12 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a, m, n</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_{CC} = 5\text{ V}$ $f_{CLOCK} = 1.04\text{ MHz}$	LIMITS				UNIT	
			1=25 °C 2=125,85 °C 3=-55,-40 °C		All Grades			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUT</b>								
Input Channel ON State Current <sup>e</sup>	$I_{ON(PEAK)}$	$V_{IN} = 2.5\text{ V}$	1	-5			$\mu\text{A}$	
Input Channel OFF State Current <sup>f</sup>	$I_{OFF}$	$V_{IN} = 5\text{ V}$	1			200	nA	
		$V_{IN} = 0\text{ V}$	1		-200			
		$V_{IN} = 5\text{ V}$	2,3			1000		
		$V_{IN} = 0\text{ V}$	2,3		-1000			
Analog Input Voltage <sup>g</sup>	$V_{ANALOG}$		1,2,3		$V_{REF-}$	$V_{REF+}$	V	
High Level Input Voltage	$V_{IH}$		1,2,3		$V_{CC}-1.5$			
Low Level Input Voltage	$V_{IL}$		1,2,3			1.5		
High Level Input Current <sup>f</sup>	$I_{IH}$	$V_{IN} = 5\text{ V}$	1,2,3			1	$\mu\text{A}$	
Low Level Input Current <sup>f</sup>	$I_{IL}$	$V_{IN} = 0\text{ V}$	1,2,3			-1		
<b>OUTPUT</b>								
High Level Output Voltage	$V_{OH}$	$I_O = -360\ \mu\text{A}$	1,2,3		4		V	
Low Level Output Voltage	$V_{OL}$	$I_O = 1.6\text{ mA}$	Data Outputs	1,2,3		0.4		
			End Of Conversion	1,2,3		0.4		
OFF State Output Current <sup>q</sup>	$I_{OS}$	$V_{REF} = 5\text{ V}$	1,2,3			1	$\mu\text{A}$	
		$V_{BUS} = 0\text{ V}$	1,2,3			-1		
<b>SUPPLY</b>								
Supply Current <sup>h</sup>	$I_{CC}$	$V_{REF+}$ is open, $V_{REF-} = 0\text{ V}$ $V_{IL} = 0\text{ V}$ , $V_{IH} = 5\text{ V}$	1 2,3	10 10		50 200	$\mu\text{A}$	
Supply Current Plus Reference Current <sup>h</sup>	$I_{CC} + I_{REF}$	$V_{CC} = 5\text{ V}$ $V_{IL} = 0\text{ V}$ , $V_{IH} = 5\text{ V}$	1			1	mA	
Supply Voltage <sup>l, c</sup>	$V_{CC}$	Refer to "Operating Range" Graph	1,2,3		3	6.5	V	

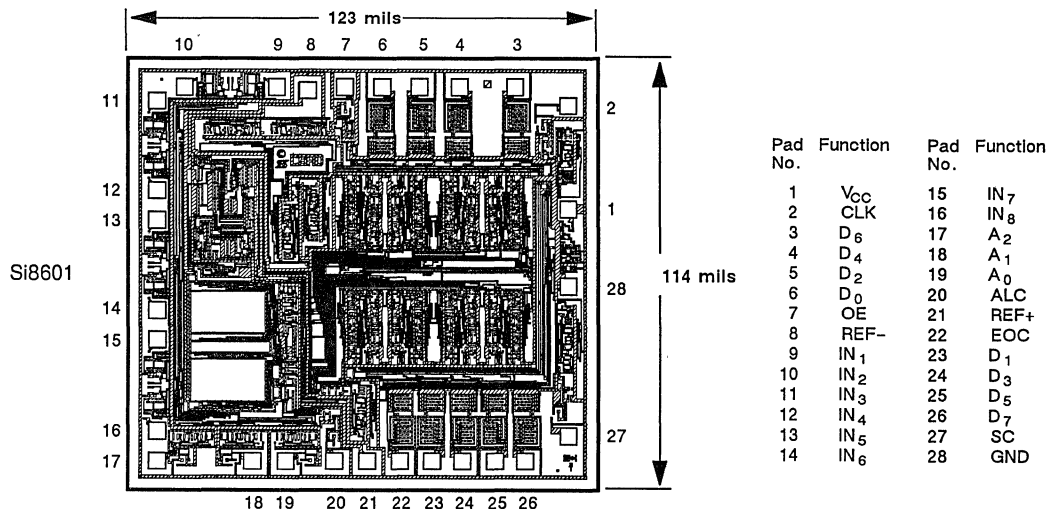
ELECTRICAL CHARACTERISTICS <sup>a, m, n</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>CC</sub> = 5 V f <sub>CLOCK</sub> = 1.04 MHz	LIMITS				UNIT
			1=25 °C 2=125,85 °C 3=-55,-40 °C		All Grades		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY (Cont'd)</b>							
Positive Reference Voltage <sup>a, l</sup>	V <sub>REF+</sub>	Refer to "Operating Range" Graph	1		3 <sup>c</sup>	V <sub>CC</sub>	V
Negative Reference Voltage <sup>a, c</sup>	V <sub>REF-</sub>		1		0	0.3 <sup>c</sup>	
Voltage Between V <sub>CC</sub> and V <sub>REF+</sub> Terminals <sup>l</sup>	V <sub>CC</sub> -V <sub>REF+</sub>	Refer to "Operating Range" Graph	1	0			
<b>DYNAMIC</b>							
Control Input Capacitance	C <sub>1</sub>		1,2,3	2.5			pF
Data Output Capacitance	C <sub>0</sub>		1,2,3	5.5			
Supply Voltage Sensitivity	PSR		1,2,3	0.05			%/V
Zero Error <sup>j</sup>	ZE	V <sub>CC</sub> = 4.75 V & 5.25 V f <sub>CLOCK</sub> = 1.04 MHz	1,2,3	0.25			LSB
Linearity Error <sup>j</sup>	INL		1,2,3	0.25			
Total Unadjusted Error <sup>j</sup>	E <sub>TOT</sub>		1 2,3	0.25	-0.50 -0.75	0.50 0.75	
Differential Nonlinearity	DNL		1,2,3		-0.5	0.5	
<b>TIMING</b>							
Clock Frequency <sup>l</sup>	f <sub>CLOCK</sub>	V <sub>CC</sub> = 3 V		100			kHz
		V <sub>CC</sub> = 5 V	1,2,3			1040	
Start Pulse Width	t <sub>SC</sub>		1		100		ns
Address Load Control Pulse Width	t <sub>ALC</sub>		1		200		
Address Set Up Time	t <sub>SU</sub>	Si8601 ONLY	1		50		
Address Hold Time	t <sub>H</sub>		1		50		
Input Voltage Stable <sup>l</sup>	t <sub>IS</sub>		1		8		Clock Periods

ELECTRICAL CHARACTERISTICS <sup>a, m, n</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$ $V_{REF+} = V_{CC}, V_{REF-} = 0 \text{ V}$ $f_{CLOCK} = 1.04 \text{ MHz}$	LIMITS				UNIT
			1=25 °C 2=125, 85 °C 3=-55, -40 °C		All Grades		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>TIMING (Cont'd)</b>							
End of Conversion Delay Time	$t_{DEC}$		1		0	200	ns
Conversion Time <sup>k</sup>	$t_{CONV}$	$f_{CLOCK} = 1.04 \text{ MHz}$ $t_{SC} = 100 \text{ ns}$	1, 2, 3			25	$\mu\text{s}$
Output Enable Time	$t_{OE}$	$C_L = 50 \text{ pF}$	1	100		250	ns
Output Disable Time	$t_{OD}$	$C_L = 10 \text{ pF}$ $R_L = 10 \text{ k}\Omega$	1	100		250	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Decays exponentially during first clock high period.
- f. Channel addressed with clock OFF.
- g. Analog input voltage greater than  $V_{REF+}$  converts as all ones and less than  $V_{REF-}$  as all zeros.
- h. Current increases linearly with frequency of the clock at a rate of approximately 10% per 100 kHz.
- i. For proper operation the maximum clock rate must be lowered as the voltage across the reference terminals is lowered below 4.75 V. The maximum clock rate must be lowered by  $0.68 f_{CLOCK} / \text{volt}$  multiplication factor.  $V_{REF+}$  must be above 3.0 V or  $V_{CC} - 1.0 \text{ V}$ , whichever is higher.
- j. All errors are measured with reference to an ideal straight-line transfer curve from 1/2 LSB to ( $V_{CC} - 1/2 \text{ LSB}$ ).
- k. Source resistance  $< 1 \text{ k}\Omega$ .
- m. All voltage values are with respect to ground terminal.
- n. All dc parameters are 100% tested at 25°C. Lots are sample tested for ac parameters and high and low temperature limits to assure conformance with specifications.
- q.  $V_{BUS}$  is the voltage applied to the output pins when the digital outputs are in OFF state.

**DIE TOPOGRAPHY**



Pad No.	Function	Pad No.	Function
1	$V_{CC}$	15	$IN_7$
2	CLK	16	$IN_8$
3	$D_6$	17	$A_2$
4	$D_4$	18	$A_1$
5	$D_2$	19	$A_0$
6	$D_0$	20	ALC
7	OE	21	REF+
8	REF-	22	EOC
9	$IN_1$	23	$D_1$
10	$IN_2$	24	$D_3$
11	$IN_3$	25	$D_5$
12	$IN_4$	26	$D_7$
13	$IN_5$	27	SC
14	$IN_6$	28	GND

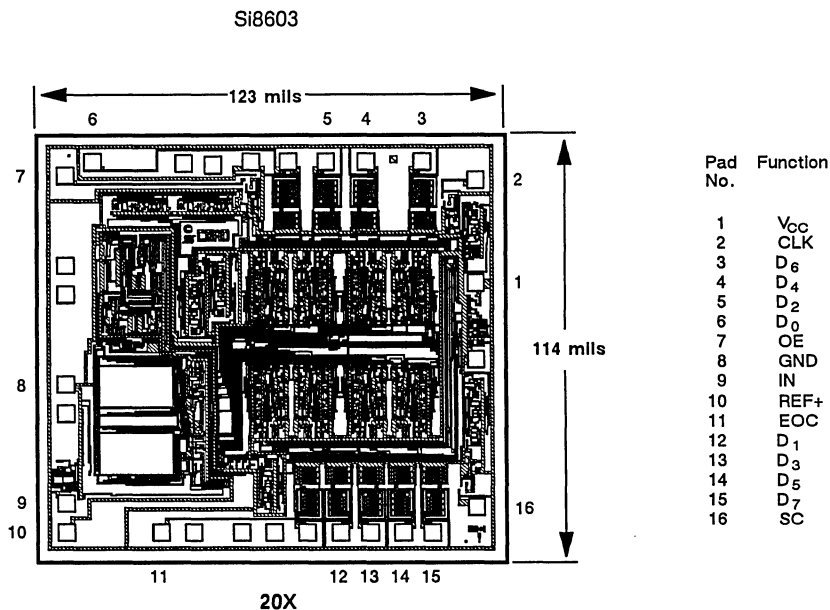
CSAD

20X

493 P-Channel Enhancement MOSFETs  
477 N-Channel Enhancement MOSFETs

13 Capacitors  
7 Resistors

## DIE TOPOGRAPHY (Cont'd)



CSBD

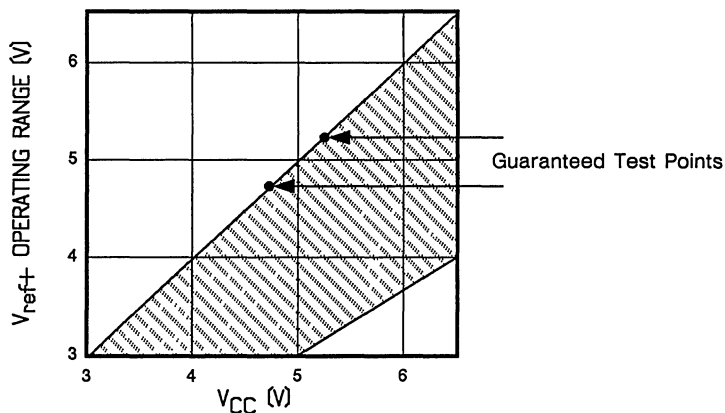
425 P-Channel Enhancement MOSFETs

409 N-Channel Enhancement MOSFETs

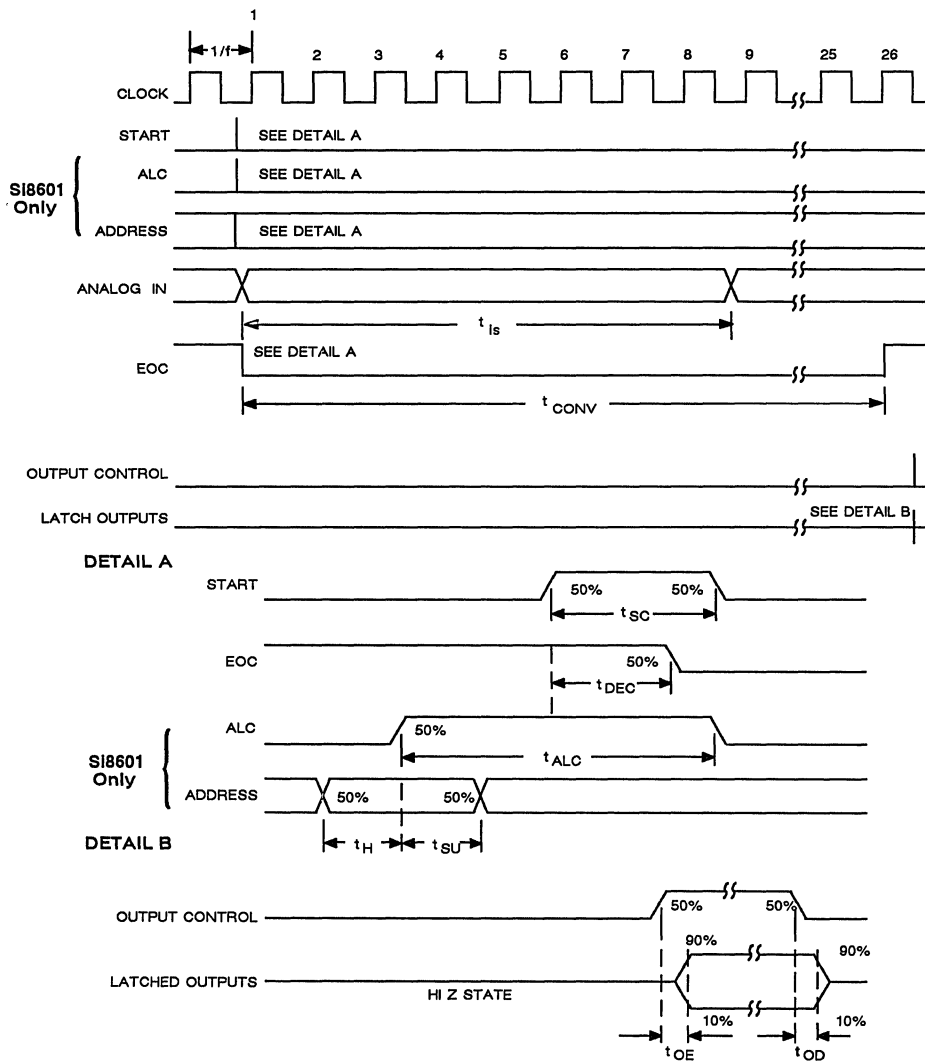
13 Capacitors

7 Resistors

## OPERATING RANGE OF V<sub>REF+</sub>



## TIMING



## DETAILED DESCRIPTION

### PRINCIPLES OF OPERATION

Si8601 with On-chip Eight Channel MUX:

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the input address code. The Address Load Control (ALC) transfers and latches the code into the address decoder on the positive edge of the ALC signal. The output latch is reset by the positive edge of the Start

Conversion (SC) pulse. Sampling starts with the positive edge of the SC pulse and lasts for 8 clock periods from its falling edge. The conversion process can be interrupted by a new SC pulse before the end of 24 clock periods. Continuous conversion may be accomplished by connecting the End of Conversion (EOC) output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

**DETAILED DESCRIPTION (Cont'd)**

**MULTIPLEXER FUNCTION TABLE**

INPUTS			ADDRESS LOAD CONTROL	SELECTED ANALOG CHANNEL
ADDRESS A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	0	0	LOW to HIGH	1
0	0	1	LOW to HIGH	2
0	1	0	LOW to HIGH	3
0	1	1	LOW to HIGH	4
1	0	0	LOW to HIGH	5
1	0	1	LOW to HIGH	6
1	1	0	LOW to HIGH	7
1	1	1	LOW to HIGH	8

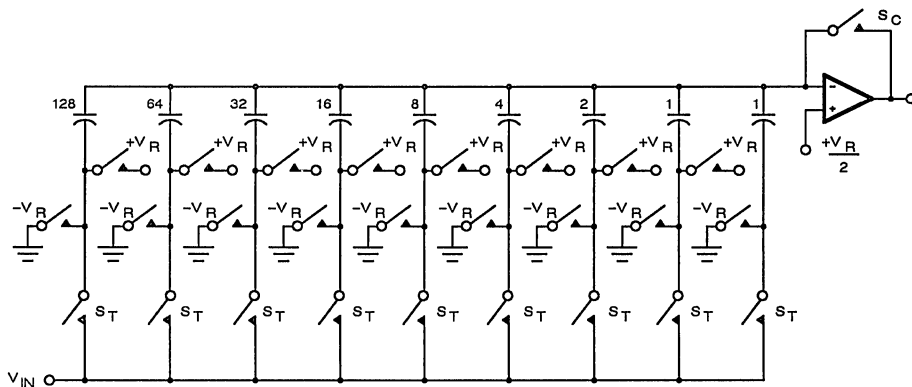
**SWITCHED CAPACITOR A/D CONVERTER**

The CMOS comparator in the (SAR) successive-approximation system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch SC and all ST switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all ST and SC switches are opened and the comparator

begins identifying bits by identifying the charge on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the comparator looks at the first capacitor (binary weight = 128). One pole of this capacitor is switched to the reference voltage, and the equivalent poles of all the other capacitors on the ladder are switched to ground. If the voltage at the summing node is greater than the trip-point of the comparator (approximately one-half the reference voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to ground. If the voltage at the summing node is less than the trip-point of the comparator, this 128-weight capacitor remains connected to the reference input through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are tested.

As can be seen, with each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive-approximation, but relies on charge shifting rather than the traditional successive-approximation register and reference D/A to count and weigh the bits from MSB to LSB.



**Figure 1. Simplified Successive Approximation Register**

## DETAILED DESCRIPTION (Cont'd)

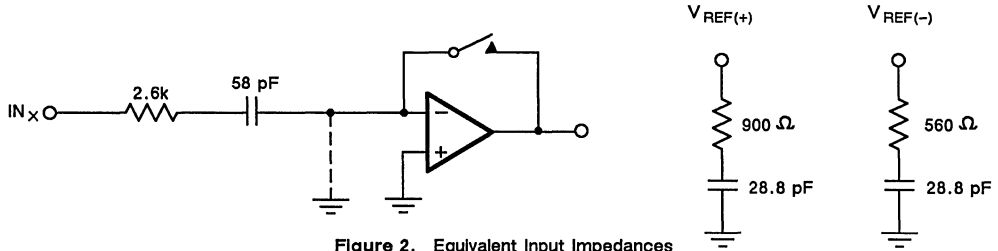


Figure 2. Equivalent Input Impedances

## APPLICATIONS

The Si8601 and Si8603 are CMOS Converters using charge redistribution to achieve A/D conversion. This allows ratiometric conversion. In a single-supply system,  $V_{REF-}$  will be connected to

ground and  $V_{REF+}$  will be connected to  $V_{CC}$ . The output will then be a simple proportional ratio between analog input voltage and  $V_{CC}$  (Figure 3). The general relationship is:

$$\frac{D_{OUT}}{2^8} = \frac{V_{IN}}{(V_{REF+}) - (V_{REF-})}$$

- Where  $D_{OUT}$  = Digital Output
- $V_{IN}$  = Analog Input
- $V_{REF+}$  = Positive Reference Potential
- $V_{REF-}$  = Negative Reference Potential

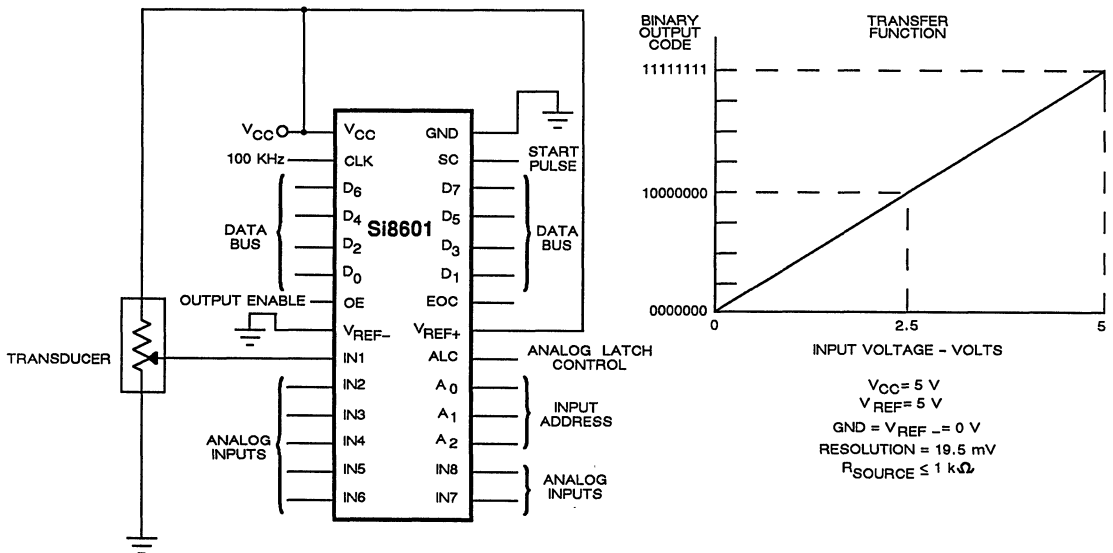


Figure 3. Ratiometric System



**APPLICATIONS (Cont'd)**

**MEMORY MAPPED OPERATION**

When operating in the memory mapped mode, the data outputs and address input are tied directly to their corresponding busses. The OC, START, and ALC lines are used to tri-state the digital outputs when appropriate. Figure 4 shows the schematic diagram of the memory mapped data acquisition system. Note the A15 is the only address decoding

line used for this example. To eliminate memory map redundancy, a more sophisticated address decoding circuit would be needed. The NOR gates of the 4001 combine the address decoding,  $\overline{\text{READ}}$  and  $\overline{\text{WRITE}}$  signals to control the data acquisition system. The EOC pin is tied to the RST 6.5 of the 8085 to notify the microprocessor when the conversion has been completed and when the data outputs are ready to be read.

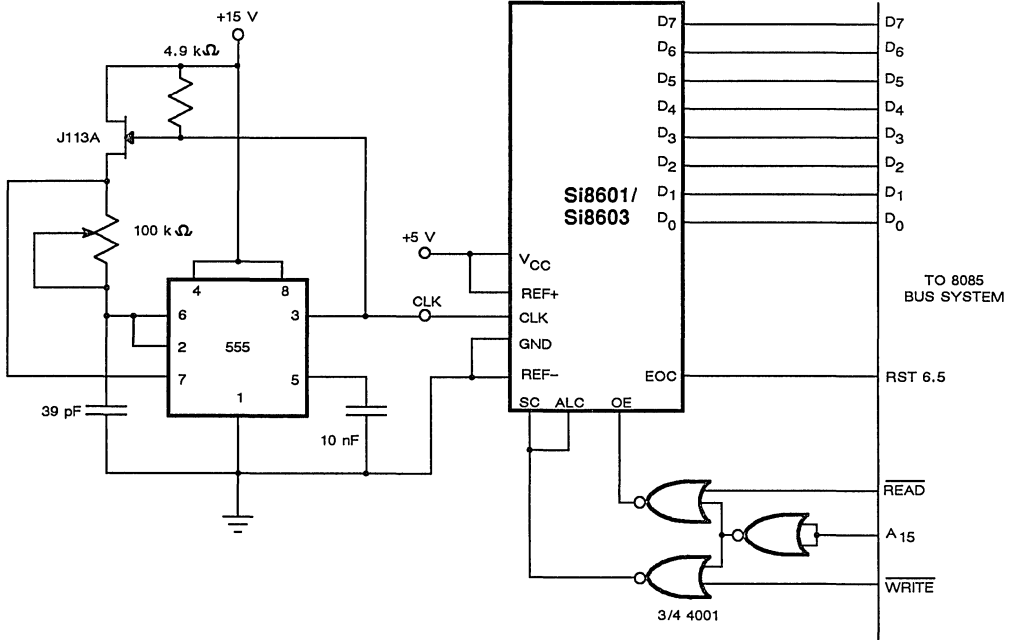


Figure 4. Schematic Diagram of a Memory Mapped Interface

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**PIN CONFIGURATION (Si8601 8-CHANNEL DATA ACQUISITION SYSTEM)**


---

PIN NUMBER	SYMBOL	DESCRIPTION
1	V <sub>CC</sub>	Input for the positive supply voltage.
2	CLK	Input for the CLOCK. The clock amplitude must conform to the V <sub>IH</sub> and V <sub>IL</sub> of the specifications and the rise time should be > 10 ns.
3–6	D6, D4, D2, D0	Digital DATA OUTPUTS, Bit 0 (Pin 6) is the LSB.
7	OE	Logic input for OUTPUT ENABLE. Connects the three–state output latches to the microprocessor BUS.
8	REF–	Input for the most negative voltage of the reference. It is normally grounded unless compressed mode operation is desired.
9–16	IN1–IN8	ANALOG INPUTS of the 8–channel multiplexer (channel 1–Pin 9, channel 8–Pin 16).
17–19	A2–A0	The three ADDRESS INPUTS that select the one–of–eight analog inputs to be converted.
20	ALC	ADDRESS LOAD CONTROL input that latches the input address into the multiplexer.
21	REF+	Input for the most positive voltage of the reference.
22	EOC	END OF CONVERSION output that goes high at the end of conversion.
23–26	D1, D3, D5, D7	Digital DATA OUTPUTS. Bit 7 (Pin 26) is the MSB.
27	SC	START CONVERSION input that initiates the conversion process.
28	GND	Power supply and analog GROUND.

---

**PIN CONFIGURATION (Si8603 8-BIT DATA ACQUISITION SYSTEM, DIP VERSION)**


---

PIN NUMBER	SYMBOL	DESCRIPTION
1	V <sub>CC</sub>	Input for the positive supply voltage.
2	CLK	Input for the CLOCK. The clock amplitude must conform to the V <sub>IH</sub> and V <sub>IL</sub> of the specifications and the rise time should be > 10 ns.
3–6	D6, D4, D2, D0	Digital DATA OUTPUTS, Bit 0 (Pin 6) is the LSB.
7	OE	Logic input for OUTPUT ENABLE. Connects the three–state output latches to the microprocessor BUS.
8	GND	Power supply and analog ground.
9	IN	ANALOG INPUT
10	REF+	Input for the positive reference voltage.
11	EOC	END OF CONVERSION output that goes high at the end of conversion.
12,13,14,15	D1, D3, D5, D7	Digital DATA OUTPUTS. Bit 7 (Pin 15) is the MSB.
16	SC	START CONVERSION input that initiates the conversion process.

**GENERAL PRECAUTIONS (For All Applications)**

1. V<sub>REF+</sub> must NEVER exceed V<sub>CC</sub> by more than 50 mV.
2. V<sub>REF–</sub> must NEVER be more negative than GND by more than 50 mV.
3. Under no condition should any voltage be applied to any pin before V<sub>CC</sub> (prevents latch–up).

# 8-Bit Data Acquisition Systems

## FEATURES

- Total Unadjusted Error < 1/2 LSB (Si8604)
- Fast Conversion Time (25  $\mu$ s maximum)
- Low Power (9 mW typ.)
- On-Chip S/H Function
- Single Supply Operation
- On-Board 8-Channel Multiplexer (Si8602)
- Microprocessor Interface

## BENEFITS

- Eliminates External Trims
- Increased Data Throughput
- Reduced System Power Consumption
- Reduced Aperture Error
- 15 V Military Systems
- Reduced Board Space and Component Count

## APPLICATIONS

- $\mu$ P/PC-Based Data Acquisition Systems
- Voice/Telecom Systems
- Battery-Operated Systems
- Audio Digitizing
- Remote Data Acquisition
- High Density Systems

## DESCRIPTION

The Si8602 and Si8604 are 8-bit data acquisition systems which include an A/D converter, sample-and-hold function, and a microprocessor interface on one monolithic chip. The Si8604 is a single-channel version, while the Si8602 includes an on-board 8-channel analog multiplexer and decode logic to form a complete 8-channel data acquisition system. The Si8602 and Si8604 are designed for 15 V single-supply operation, 0 to 10 V Analog Range and CMOS logic interfacing.

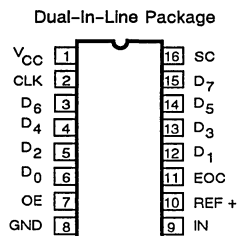
Built in the Siliconix proprietary PolyMOS™ process, the Si8602/8604 use a capacitive-ladder A/D conversion technique to achieve low power, high speed and less than 1/2 LSB total unadjusted error without the need for thin film resistors or laser

trimming. The capacitive ladder architecture creates an on-board sample/hold function, reducing the aperture time of the converter to less than 90 ns. This facilitates digitizing rapidly-slewing analog signals with a minimum of error. An epitaxial layer prevents latchup.

The Si8602 is available in 28-pin plastic and ceramic DIP. The Si8604 is available in 16-pin plastic and ceramic DIP. Both are available in industrial, D suffix (–40 to 85°C) and military, A suffix (–55 to 125°C) temperature ranges and in /883 versions as well. For surface mount applications, the Si8602 is available in the PLCC-28, and the Si8604 in the PLCC-20. For more information on the Si8602, please refer to Siliconix application Note AN83-13.

**6**

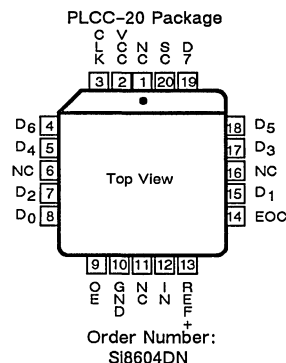
## PIN CONFIGURATION



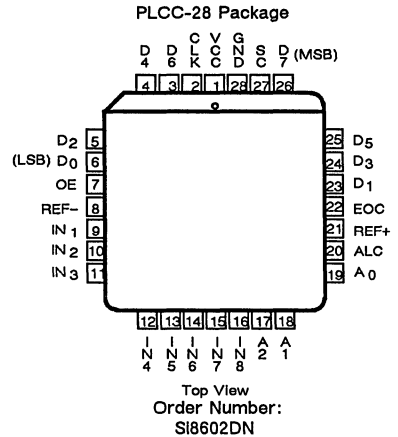
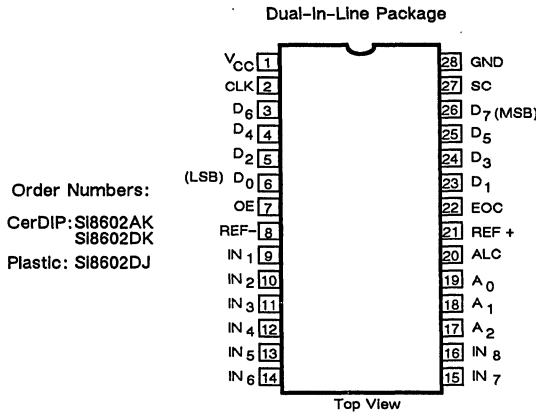
Top View

Order Numbers:

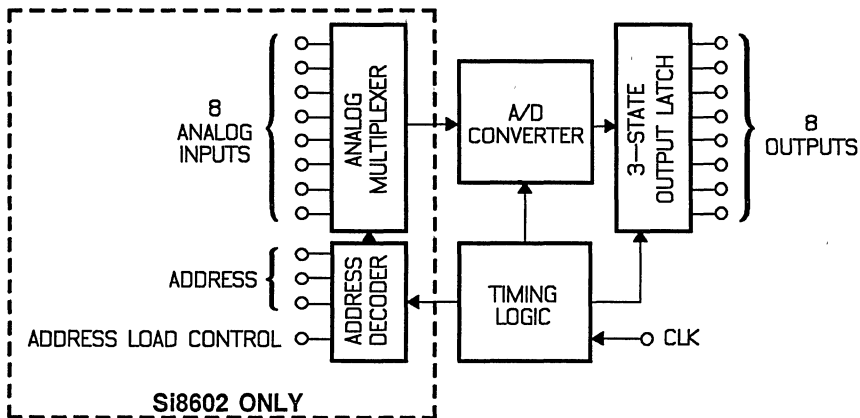
CerDIP: Si8604DJ  
Plastic: Si8604AK, Si8604DK



## PIN CONFIGURATION (Cont'd)



## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Reference Input Voltage Range, V <sub>REF-</sub>	-0.3 V to V <sub>REF+</sub>
Reference Input Voltage Range, V <sub>REF+</sub>	V <sub>REF-</sub> to V <sub>CC</sub> + 0.3 V
Supply Voltage, V <sub>CC</sub>	16.5 V
Input Voltage Range, All Inputs	-0.3 V to V <sub>CC</sub> + 0.3 V
Storage Temperature (K Suffix)	-65 to 150°C
(J, N Suffix)	-65 to 150°C
Operating Temperature (A Suffix)	-55 to 125°C
(D Suffix)	-40 to 85°C

Power Dissipation (Package)*	
28-Pin Ceramic DIP**	1046 mW
16-Pin Ceramic DIP***	900 mW
28-Pin Plastic DIP****	1046 mW
16-Pin Plastic DIP*****	900 mW
28-Pin PLCC*****	900 mW
20-Pin PLCC*****	900 mW

- \* All leads welded or soldered on PC Board.
- \*\* Derate 6.5 mW/°C above 25°C.
- \*\*\* Derate 12 mW/°C above 75°C.
- \*\*\*\* Derate 6.5 mW/°C above 25°C.
- \*\*\*\*\* Derate 12 mW/°C above 75°C.

## ELECTRICAL CHARACTERISTICS <sup>a, m, n</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_{CC} = 15\text{ V}$ $f_{CLOCK} = 1.04\text{ MHz}$	LIMITS				UNIT
			1=25 °C 2=125,85 °C 3=-55, -40 °C		All Grades		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>							
Input Channel ON State Current <sup>e</sup>	$I_{ON(PEAK)}$	$V_{IN} = 5\text{ V}$	1	-5		$\mu\text{A}$	
Input Channel OFF State Current <sup>f</sup>	$I_{OFF}$	$V_{IN} = 15\text{ V}$	1		200	nA	
		$V_{IN} = 0\text{ V}$	1		-200		
		$V_{IN} = 15\text{ V}$	2,3		1000		
		$V_{IN} = 0\text{ V}$	2,3		-1000		
Analog Input Voltage <sup>g</sup>	$V_{ANALOG}$		1,2,3		$V_{REF-}$ $V_{REF+}$		
High Level Input Voltage	$V_{IH}$		1,2,3		$V_{CC}-1.5$	V	
Low Level Input Voltage	$V_{IL}$		1,2,3		1.5		
High Level Input Current <sup>f</sup>	$I_{IH}$		1,2,3		1	$\mu\text{A}$	
Low Level Input Current <sup>f</sup>	$I_{IL}$	$V_{IN} = 0\text{ V}$	1,2,3		-1		
<b>OUTPUT</b>							
High Level Output Voltage	$V_{OH}$	$I_O = -360\ \mu\text{A}$	1,2,3		14	V	
			1,2,3		9		
Low Level Output Voltage	$V_{OL}$	$I_O = 1.6\text{ mA}$	Data Outputs	1,2,3		0.4	
			End Of Conversion	1,2,3		0.4	
OFF State Output Current <sup>q</sup>	$I_{OS}$	$V_{BUS} = 15\text{ V}$	1,2,3		1	$\mu\text{A}$	
		$V_{BUS} = 0\text{ V}$	1,2,3		-1		
<b>SUPPLY</b>							
Supply Current <sup>h</sup>	$I_{CC}$	$V_{REF+}$ is open, $V_{REF-} = 0\text{ V}$ $V_{IL} = 0\text{ V}$ , $V_{IH} = 15\text{ V}$	1,2,3	0.6		2 mA	

ELECTRICAL CHARACTERISTICS <sup>a, m, n</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_{CC} = 15\text{ V}$ $f_{CLOCK} = 1.04\text{ MHz}$	LIMITS				UNIT
			1=25 °C 2=125, 85 °C 3=-55, -40 °C		All Grades		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY (Cont'd)</b>							
Supply Voltage <sup>l, c</sup>	$V_{CC}$	Refer to "Operating Range" Graph	1,2,3		10.8	16.5	V
Positive Reference Voltage <sup>g, i</sup>	$V_{REF+}$	Refer to "Operating Range" Graph	1		8 <sup>c</sup>	10	
Negative Reference Voltage <sup>g</sup>	$V_{REF-}$		1		0	0.3 <sup>c</sup>	
Voltage Between $V_{CC}$ and $V_{REF+}$ Terminals	$V_{CC-}$ $V_{REF+}$	Refer to "Operating Range" Graph	1	0			
<b>DYNAMIC</b>							
Control Input Capacitance	$C_1$		1,2,3	2.5			pF
Data Output Capacitance	$C_0$		1,2,3	5.5			
Supply Voltage Sensitivity	PSR		1,2,3	0.05			%/V
Zero Error <sup>j</sup>	ZE	$V_{CC} = 16.5\text{ V} \ \& \ 10.8\text{ V}$ $f_{CLOCK} = 1.04\text{ MHz}$	1,2,3	0.25	-0.5	0.5	LSB
Full Scale Error			1,2,3	0.25	-0.75	0.75	
Relative Nonlinearity	INL		1,2,3	0.25	-0.5	0.5	
Differential Nonlinearity	DNL		1,2,3	0.25	-0.5	0.5	
<b>TIMING</b>							
Clock Frequency <sup>l, c</sup>	$f_{CLOCK}$		1,2,3			1.5	MHz
Start Pulse Width	$t_{SC}$		1		100		ns
Address Load Control Pulse Width	$t_{ALC}$	Si8602 ONLY	1		200		
Address Set Up Time	$t_{SU}$		1		50		
Address Hold Time	$t_H$		1		50		
Input Voltage Stable <sup>l</sup>	$t_{IS}$		1		8		Clock Periods
End of Conversion Delay Time	$t_{DEC}$		1		0	200	ns

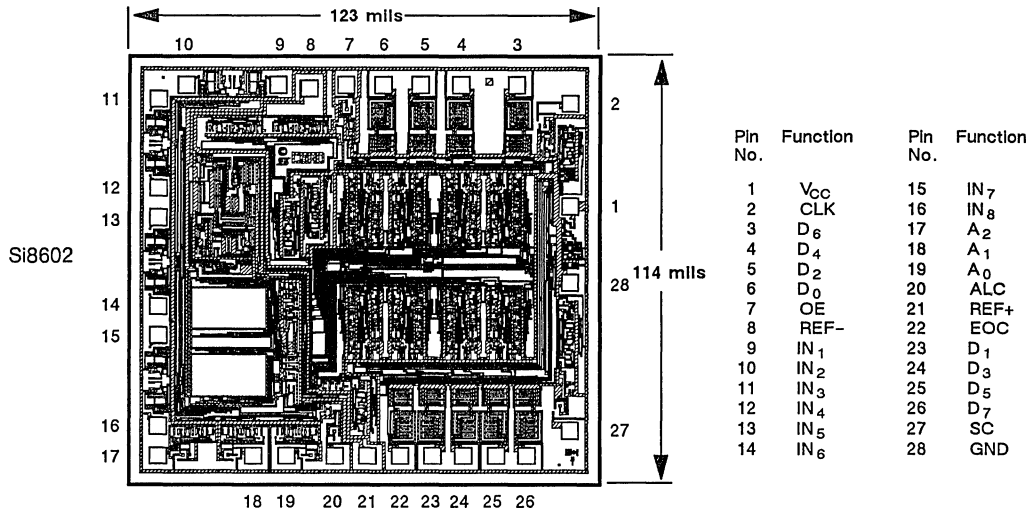
ELECTRICAL CHARACTERISTICS <sup>a, m, n</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{CC} = 10.8\text{ V to }16.5\text{ V}$ $V_{REF+} = 10\text{ V}, V_{REF-} = 0\text{ V}$ $f_{CLOCK} = 1.04\text{ MHz}$	LIMITS				UNIT
			1=25 °C 2=125,85 °C 3=-55,-40 °C		All Grades		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>TIMING (Cont'd)</b>							
Conversion Time <sup>k</sup>	$t_{CONV}$	$t_{SC} = 100\text{ ns}$	1,2,3		25	$\mu\text{s}$	
Output Enable Time	$t_{OE}$	$C_L = 50\text{ pF}$	1	100	200	ns	
Output Disable Time	$t_{OD}$	$C_L = 10\text{ pF}$ $R_L = 10\text{ k}\Omega$	1	100	200		

**NOTES:**

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Decays exponentially during first clock high period.
- Channel addressed with clock OFF.
- Analog input voltage greater than  $V_{REF+}$  converts as all ones and less than  $V_{REF-}$  as all zeros.
- Current increases linearly with frequency of the clock at a rate of approximately 10% per 100 kHz.
- For proper operation the maximum clock rate must be lowered as the voltage across the reference terminals is lowered below 10 V. The maximum clock rate must be lowered by 0.68  $f_{CLOCK}/\text{volt}$  multiplication factor.  $V_{REF+}$  must be above 3.0 V or  $V_{CC} - 1.0\text{ V}$ , whichever is higher.
- All errors are measured with reference to an ideal straight-line transfer curve from 1/2 LSB to  $(V_{CC} - 1/2\text{ LSB})$ .
- Source resistance < 1 k $\Omega$ .
- All voltage values are with respect to ground terminal.
- All dc parameters are 100% tested at 25°C. Lots are sample tested for ac parameters and high and low temperature limits to assure conformance with specifications.
- $V_{BUS}$  is the voltage applied to the output pins when the digital outputs are in the OFF state.

**DIE TOPOGRAPHY**

**6**

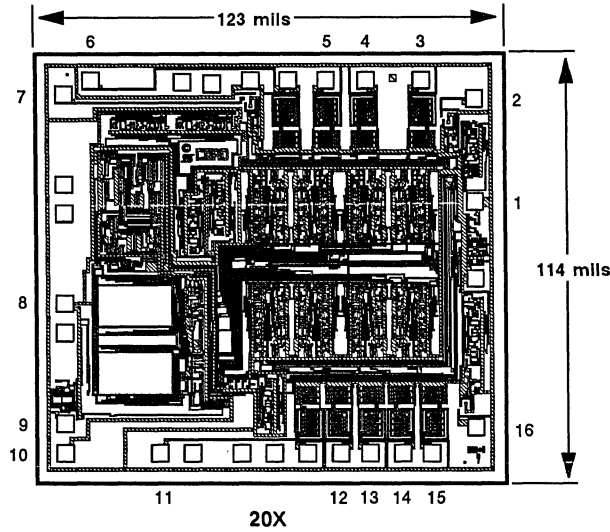


**CSAD**

493 P-Channel Enhancement MOSFETs      13 Capacitors  
477 N-Channel Enhancement MOSFETs      7 Resistors

## DIE TOPOGRAPHY (Cont'd)

Si8604



Pad No.	Function
1	V <sub>CC</sub> (Substrate)
2	CLK
3	D <sub>6</sub>
4	D <sub>4</sub>
5	D <sub>2</sub>
6	D <sub>0</sub>
7	OE
8	GND
9	IN
10	REF+
11	EOC
12	D <sub>1</sub>
13	D <sub>3</sub>
14	D <sub>5</sub>
15	D <sub>7</sub>
16	SC

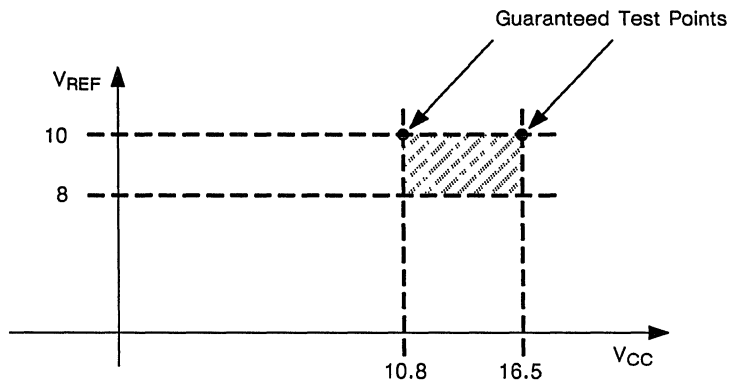
CSBD

425 P-Channel Enhancement MOSFETs  
409 N-Channel Enhancement MOSFETs

20X

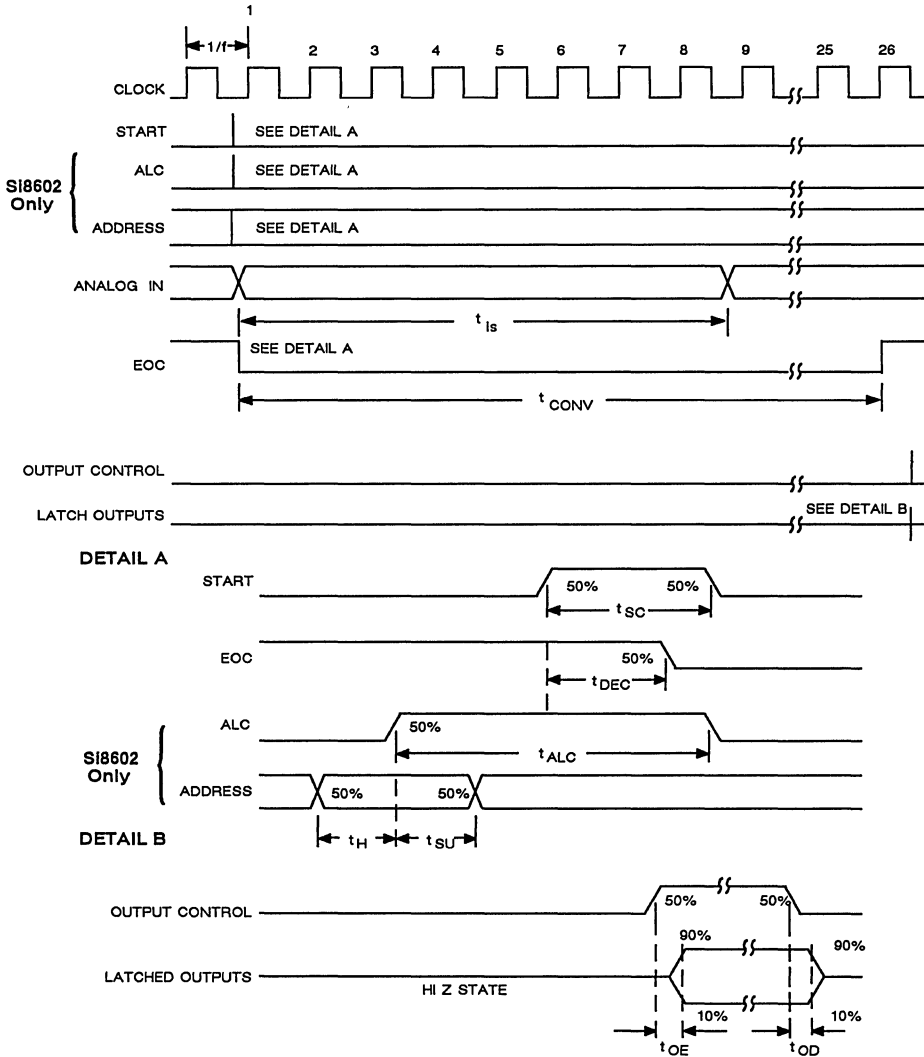
13 Capacitors  
7 Resistors

## OPERATING RANGE OF V<sub>REF+</sub> AND V<sub>CC</sub>





**TIMING**



**DETAILED DESCRIPTION**

**PRINCIPLES OF OPERATION**

Si8602 with On-chip Eight Channel MUX:

The analog multiplexer selects 1 of 8 single-ended input channels as determined by the input address code. The Address Load Control (ALC) transfers and latches the code into the address decoder on the positive edge of the ALC signal. The output latch is reset by the positive edge of the Start

Conversion (SC) pulse. Sampling starts with the positive edge of the SC pulse and lasts for 8 clock periods from its falling edge. The conversion process can be interrupted by a new SC pulse before the end of 24 clock periods. Continuous conversion may be accomplished by connecting the End of Conversion (EOC) output to the start input. If used in this mode an external pulse should be applied after power up to assure start up.

MULTIPLEXER FUNCTION TABLE

INPUTS			ADDRESS LOAD CONTROL	SELECTED ANALOG CHANNEL
ADDRESS A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		
0	0	0	LOW to HIGH	1
0	0	1	LOW to HIGH	2
0	1	0	LOW to HIGH	3
0	1	1	LOW to HIGH	4
1	0	0	LOW to HIGH	5
1	0	1	LOW to HIGH	6
1	1	0	LOW to HIGH	7
1	1	1	LOW to HIGH	8

### SWITCHED CAPACITOR A/D CONVERTER

The CMOS comparator in the (SAR) successive-approximation system determines each bit by examining the charge on a series of binary-weighted capacitors (Figure 1). In the first phase of the conversion process, the analog input is sampled by closing switch SC and all ST switches, and by simultaneously charging all the capacitors to the input voltage.

In the next phase of the conversion process, all ST and SC switches are opened and the comparator

begins identifying bits by identifying the charge on each capacitor relative to the reference voltage. In the switching sequence, all eight capacitors are examined separately until all 8 bits are identified, and then the charge-convert sequence is repeated. In the first step of the conversion phase, the comparator looks at the first capacitor (binary weight = 128). One pole of this capacitor is switched to the reference voltage, and the equivalent poles of all the other capacitors on the ladder are switched to ground. If the voltage at the summing node is greater than the trip-point of the comparator (approximately one-half the reference voltage), a bit is placed in the output register, and the 128-weight capacitor is switched to ground. If the voltage at the summing node is less than the trip-point of the comparator, this 128-weight capacitor remains connected to the reference input through the remainder of the capacitor-sampling (bit-counting) process. The process is repeated for the 64-weight capacitor, the 32-weight capacitor, and so forth down the line, until all bits are tested.

As can be seen, with each step of the capacitor-sampling process, the initial charge is redistributed among the capacitors. The conversion process is successive-approximation, but relies on charge shifting rather than the traditional successive-approximation register and reference D/A to count and weigh the bits from MSB to LSB.

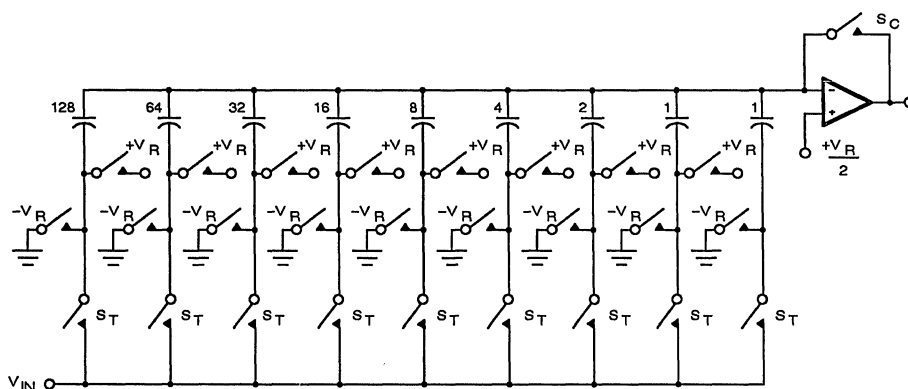


Figure 1. Simplified Successive Approximation Register

**DETAILED DESCRIPTION (Cont'd)**

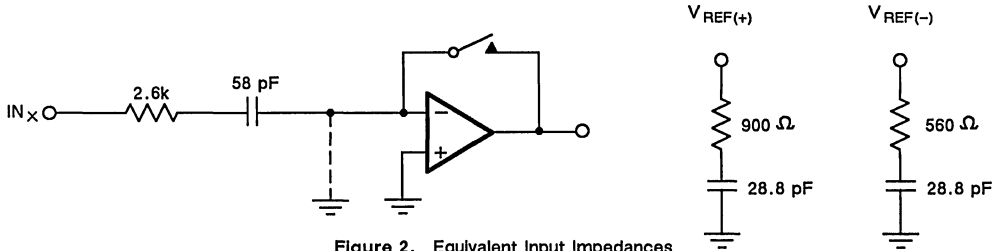


Figure 2. Equivalent Input Impedances

**APPLICATIONS**

The Si8602 and Si8604 are CMOS Converters using charge redistribution to achieve A/D conversion. This allows ratiometric conversion. In a single-supply system,  $V_{REF-}$  will be connected to

ground and  $V_{REF+}$  will be connected to  $V_{CC}$ . The output will then be a simple proportional ratio between analog input voltage and  $V_{CC}$  (Figure 3). The general relationship is:

$$\frac{D_{OUT}}{2^8} = \frac{V_{IN}}{(V_{REF+}) - (V_{REF-})}$$

- Where  $D_{OUT}$  = Digital Output (0 to 255)
- $V_{IN}$  = Analog Input
- $V_{REF+}$  = Positive Reference Potential
- $V_{REF-}$  = Negative Reference Potential

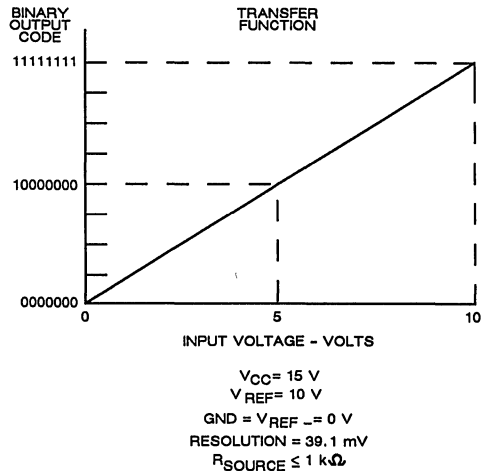
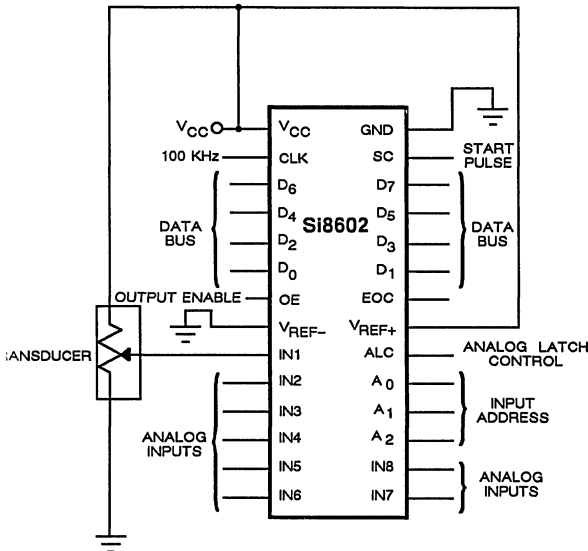


Figure 3. Ratiometric System

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**PIN CONFIGURATION (Si8602 8-CHANNEL DATA ACQUISITION SYSTEM)**


---

PIN NUMBER	SYMBOL	DESCRIPTION
1	V <sub>CC</sub>	Input for the positive supply voltage.
2	CLK	Input for the CLOCK. The clock amplitude must conform to the V <sub>IH</sub> and V <sub>IL</sub> of the specifications and the rise time should be > 10 ns.
3–6	D6, D4, D2, D0	Digital DATA OUTPUTS, Bit 0 (Pin 6) is the LSB.
7	OE	Logic input for OUTPUT ENABLE. Connects the three–state output latches to the microprocessor BUS.
8	REF–	Input for the most negative voltage of the reference. It is normally grounded unless compressed mode operation is desired.
9–16	IN1–IN8	ANALOG INPUTS of the 8–channel multiplexer (channel 1–Pin 9, channel 8–Pin 16).
17–19	A2–A0	The three ADDRESS INPUTS that select the one–of–eight analog inputs to be converted.
20	ALC	ADDRESS LOAD CONTROL input that latches the input address into the multiplexer.
21	REF+	Input for the most positive voltage of the reference.
22	EOC	END OF CONVERSION output that goes high at the end of conversion.
23–26	D1, D3, D5, D7	Digital DATA OUTPUTS. Bit 7 (Pin 26) is the MSB.
27	SC	START CONVERSION input that initiates the conversion process.
28	GND	Power supply and analog GROUND.

---

**PIN CONFIGURATION (Si8604 8-BIT DATA ACQUISITION SYSTEM, DIP VERSION)**


---

PIN NUMBER	SYMBOL	DESCRIPTION
1	V <sub>CC</sub>	Input for the positive supply voltage.
2	CLK	Input for the CLOCK. The clock amplitude must conform to the V <sub>IH</sub> and V <sub>IL</sub> of the specifications and the rise time should be > 10 ns.
3–6	D6, D4, D2, D0	Digital DATA OUTPUTS, Bit 0 (Pin 6) is the LSB.
7	OE	Logic input for OUTPUT ENABLE. Connects the three–state output latches to the microprocessor BUS.
8	GND	Power supply and analog ground.
9	IN	ANALOG INPUT
10	REF+	Input for the positive reference voltage.
11	EOC	END OF CONVERSION output that goes high at the end of conversion.
12,13,14,15	D1, D3, D5, D7	Digital DATA OUTPUTS. Bit 7 (Pin 15) is the MSB.
16	SC	START CONVERSION input that initiates the conversion process.

**GENERAL PRECAUTIONS (For All Applications)**

1. V<sub>REF+</sub> must NEVER exceed V<sub>CC</sub> by more than 50 mV.
2. V<sub>REF–</sub> must NEVER be more negative than GND by more than 50 mV.
3. Under no condition should any voltage be applied to any pin before V<sub>CC</sub> (prevents latch–up).



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# WIDEBAND/VIDEO

## INTRODUCTION

Siliconix manufactures analog switches and multiplexers for wideband/video applications using Double Diffused MOS (DMOS) technology. DMOS FETs are n-channel enhancement-mode MOSFET's which exhibit very low capacitance and ON resistance, compared to conventional CMOS devices. The result is wide bandwidth switches, from discretes such as the SD210 and SD5000 families, through D/CMOS "T" switches and multiplexers which feature crosstalk and off isolation performance as high as 100 dB at 5 MHz and 3 dB bandwidths in excess of 500 MHz. These devices are ideal for broadcast video, digital data routing, high end workstation networks and imaging applications from medical to military.

## DMOS Switch Arrays

The SD500X and SD540Xs are monolithic arrays of four DMOS FETs without drivers. Their low capacitance and low ON resistance make them ideal for high speed wideband switching and sampling applications.

## D/CMOS "T" Switches

The DG54X family of wideband/video "T" switches includes the DG540, DG541 and DG542 switches. The DG540 and DG541 are quad SPST switches, and the DG542 is a dual SPDT (or dual changeover) function. The DG540 employs interstitial ground lines between adjacent channels to achieve improved isolation and reduced crosstalk. The DG541 uses the standard DG201A pin-out, hence has slightly inferior performance than the DG540, but is available in a lower cost, smaller package. Each of these switches uses DMOS "T" switches for fast switching, wide bandwidths and excellent isolation.

## D/CMOS Wideband/Video Multiplexers

The DG535 and DG536 are 16-channel wideband/video multiplexers which use the Siliconix D/CMOS process to combine wideband DMOS "T" switches with high density, high speed CMOS logic and switch drivers to form complete monolithic wideband/video multiplexing systems. These devices include on-board latches to hold the address selection data and all of the necessary control logic to facilitate connection into larger arrays, matrices and multiplexers. The DG534 and DG538 are 4- and 8-channel wideband/video multiplexers which, like the DG535 and DG536, feature address latches and control logic with the addition of data readback and TTL-compatibility. They make excellent wideband/video crosspoints, routers, and multiplexers, reducing board space, power dissipation, component count and cost while simplifying system design and improving reliability.

For detailed information on these products please refer to their individual data sheets and to application notes AN85-3, AN86-1, and AN88-2.

---

## GLOSSARY OF TERMS

### Bandwidth

The "3 dB down" point of the frequency response characteristic.

### Crosspoint Switch

A two-dimensional array of analog switches or analog multiplexers that allows for the routing of signals from any input to any output.

### Crosstalk

A measure of how much of an unwanted signal appears on a given analog channel due to spurious capacitive or inductive coupling from another channel.

### D/CMOS

Semiconductor process that combines DMOS FETs and CMOS logic on a monolithic chip.

## Differential Gain

Expressed as a percentage, this is a form of distortion that appears as changes in the amplitude of the chrominance (color) signal as a function of luminance (brightness) amplitude.

## Differential Multiplexer

Analog multiplexer that selects both the high and the low side of each signal. It can be thought of as two single-ended multiplexers operating in tandem.

## Differential Phase

Measured in degrees is the phase shift of the color subcarriers resulting from changes in luminance level.

## DMOS

(Double Diffused MOS) Type of field effect transistor featuring low  $r_{DS(ON)}$  and low capacitance.

## Input Capacitance

Capacitive load that the input terminal of an analog switch presents to the signal source. It is specified both with the switch ON or OFF.

## Insertion Loss

Expressed in dB, is a measure of the signal loss caused by the impedance of the analog switch at a given frequency.

## Off Isolation

A measure of how much of the signal applied to an "open" switch appears at its output due to parasitic components such as gate-to-channel capacitance and lead inductances.

## ON-Resistance

DC input-to-output resistance of an analog switch channel when the switch is turned ON.

## Output Buffer

An amplifier, typically with a gain of two, which is normally used at the output of a video multiplexer to drive a length of double terminated coaxial cable.

## Output Capacitance

Capacitive load that the output of an OFF switch adds to the output node.

## PLCC Package

Plastic leaded chip carrier. Surface mount package characterized for its small size and reliable lead-to-printed circuit board mechanical interface.

## Readback

Feature that allows for the inspection of the control latch contents in a multiplexer.

## Single Ended Multiplexers

Array of analog switches that selects one of several analog input signals.

## "T" Switch

Analog switch configuration consisting of two series switches and a shunt switch to ground. It is used to dramatically improve the off-isolation of the array.

## Video

Electrical signals carrying dynamic visual information.

## Video Buffer

An amplifier whose function is to reduce the capacitive loading effect of several video multiplexer inputs on a common signal source. This is normally a unity gain buffer.

## Wideband

A relative term, as used in this book it refers to a frequency spectrum at least more than 2 MHz wide.



# 4-Channel/Dual 2-Channel Wideband/Video Multiplexer

## FEATURES

- Wide Bandwidth (500 MHz)
- Very Low Crosstalk (-97 dB @ 5 MHz)
- On-Board TTL-compatible Latches with Readback
- Optional Negative Supply Input
- Low  $r_{DS(ON)}$  (90  $\Omega$  max)
- Single-ended 4-channel or Dual 2-channel Operation
- ESDS Protection >  $\pm 4000$  V

## BENEFITS

- Improved System Bandwidth
- Improved Channel Off-isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

## APPLICATIONS

- Wideband Signal Routing and Multiplexing
- High-end Video Systems
- $\mu$ P-controlled Systems
- Direct Coupled Systems
- ATE Systems

## DESCRIPTION

The DG534 is a digitally selectable 4-channel or dual 2-channel analog multiplexer designed for wideband operation. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low ON resistance and low capacitance of the DG534 make it ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without DC biasing.

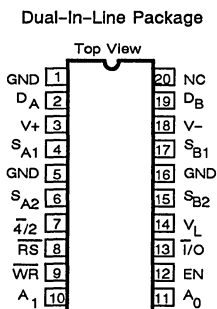
The DG534 is built on a D/CMOS process that combines n-channel DMOS switching FETs with

low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of OFF isolation. Crosstalk is reduced to -97 dB at 5 MHz on the DG534 by including a ground line between each adjacent signal path.

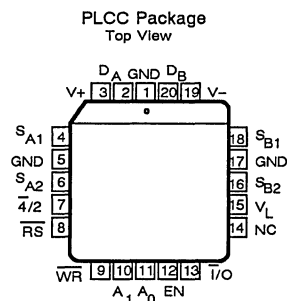
The DG534 is available in 20-pin plastic DIP and PLCC packages for operation over the industrial, D suffix (-40 to 85°C) temperature range. The 20-lead side braze DIP is available for military, A suffix (-55 to 125°C) temperature range operation.

For more information please refer to Siliconix Applications Note AN88-2.

## PIN CONFIGURATION

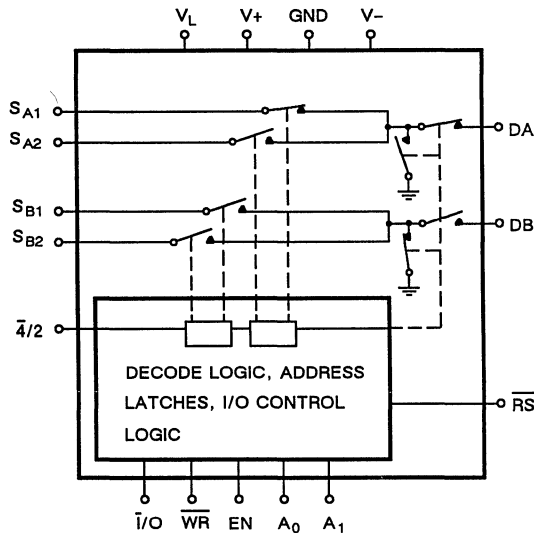


Order Numbers:  
Side Braze: DG534AP,  
Plastic: DG534DJ



Order Number:  
DG534DN

All four input switches are "T" switches.



$\bar{I/O}$	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	$\bar{4}/2$	ON SWITCH
X	X	X	X	$\bar{H}$	1	1	Maintains previous state
X	X	X	X	X	0	X	None (latches cleared)
X	X	X	0	0	1	X	None
0	0	0	1	0	1	0	SA1
0	0	1	1	0	1	0	SA2
0	1	0	1	0	1	0	SB1
0	1	1	1	0	1	0	SB2
0	X	0	1	0	1	1	SA1 & SB1
0	X	1	1	0	1	1	SA2 & SB2
1	NOTE 2, 3		1	1	1	Note 1	Latches Transparent

Logic "1" :  $V_{AH} \geq 2.0 V$

Logic "0" :  $V_{AL} \leq 0.8 V$

- $\bar{4}/2$  can be either H or L but should not change during these operations.
- In this condition the pins A<sub>0</sub> and A<sub>1</sub> become outputs and reflect the contents of the latches. Please see timing waveforms for more detail.
- EN must be latched HIGH to allow proper address data readback operation.

## ABSOLUTE MAXIMUM RATINGS

V <sub>+</sub> to GND	.....	-0.3 V to +22 V
V <sub>+</sub> to V <sub>-</sub>	.....	-0.3 V to +22 V
V <sub>-</sub> to GND	.....	-10 V to +0.3 V
Digital Inputs	..... (V <sub>-</sub> minus 0.3 V) to (V <sub>+</sub> plus 0.3 V)	or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	.....	(V <sub>-</sub> minus 0.3 V) to (V <sub>-</sub> plus 14 V)
		or 20 mA, whichever occurs first
CURRENT (any terminal) Continuous	.....	20 mA
CURRENT (S or D) Pulsed 1 ms 10% duty	.....	40 mA
Storage Temperature (A Suffix)	.....	-65 to 150°C
	(D Suffix)	.....-65 to 125°C
Operating Temperature (A Suffix)	.....	-55 to 125°C
	(D Suffix)	.....-40 to 85°C

Power Dissipation (Package) \*

20-Pin Plastic DIP**	.....	625 mW
20-Pin Side Braze DIP***	.....	1200 mW
20-Pin Quad J Lead Plastic****	.....	450 mW

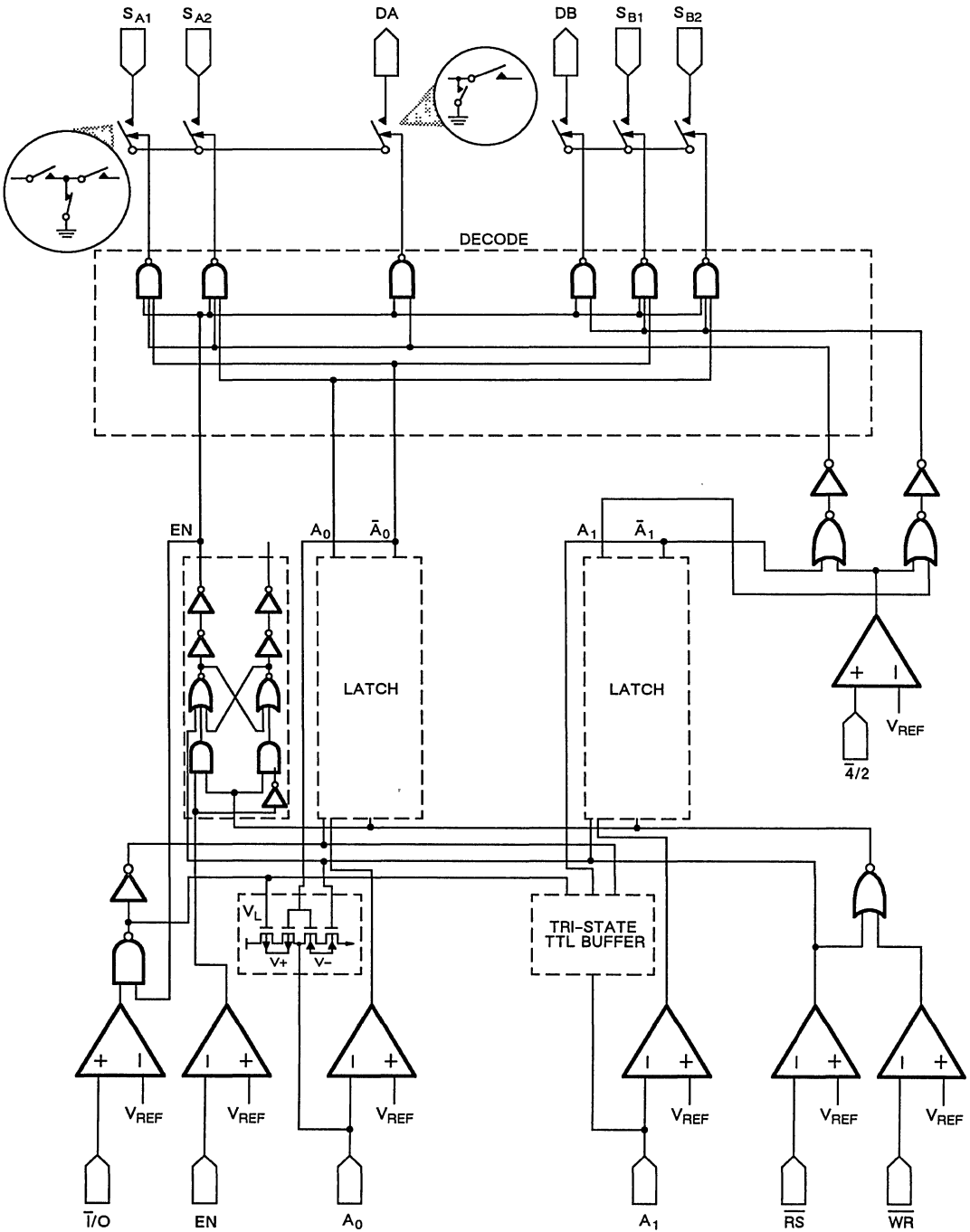
\* All leads welded or soldered to PC board.

\*\* Derate 8.3 mW/°C above 75°C

\*\*\* Derate 16 mW/°C above 75°C

\*\*\*\* Derate 6 mW/°C above 75°C

**CONTROL CIRCUITRY**



**7**

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V V <sub>L</sub> = +5 V, GND = 0 V $\overline{WR}$ = 0.8 V RS, EN = 2 V	LIMITS						UNIT	
			1=25°C		A SUFFIX		D SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>	V <sub>-</sub> = -5 V	1		-5	8	-5	8	V	
Drain - Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>S</sub> = 0 V V <sub>AIL</sub> = 0.8 V, V <sub>AIH</sub> = 2 V Sequence each switch ON	1,3 2	45		90 120		90 120	Ω	
Resistance Match Between Channels	$\Delta$ r <sub>DS(ON)</sub>		1			9		9		
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 8 V, V <sub>D</sub> = 0 V EN = 0.8 V	1,3 2		-5 -50	5 50	-5 -50	5 50	nA	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = 0 V, V <sub>D</sub> = 8 V EN = 0.8 V	1,3 2		-20 -500	20 500	-20 -500	20 500		
Total Switch ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 8 V	1,3 2		-10 -1000	10 1000	-10 -100	10 100		
<b>INPUT</b>										
Address Output Current	I <sub>AO</sub>	V <sub>AO</sub> = 2.7 V	1,2,3		-400		-400		μA	
		V <sub>AO</sub> = 0.4 V	1,2,3			400		400		
Input Voltage High	V <sub>AIH</sub>	See Figure 13 Note 1	1,2,3		2		2		V	
Input Voltage Low	V <sub>AIL</sub>		1,2,3			0.8		0.8		
Address Input Current	I <sub>AI</sub>	V <sub>AI</sub> = 0 V or 2 V or 15 V	1,3 2	0.1	-1 -10	1 10	-1 -10	1 10	μA	
<b>DYNAMIC</b>										
ON State Input Cap. <sup>c</sup>	C <sub>S(ON)</sub>	See Figure 11	PLCC DIP	1 1	23 27		35		30 35	pF
OFF State Input Cap. <sup>c</sup>	C <sub>S(OFF)</sub>	See Figure 12	PLCC DIP	1 1	2 3		5		4 5	
OFF State Output Cap. <sup>c</sup>	C <sub>D(OFF)</sub>	See Figure 12	PLCC DIP	1 1	4 6		10		8 10	
Multiplexer Switching Time	t <sub>TRANS</sub>	See Figure 4		1,3 2			300 500		300 500	ns
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 4		1,2,3		50		50		
EN, $\overline{WR}$ Turn on Time	t <sub>ON</sub>	See Figures 2 & 3		1,3 2			300 500		300 500	
EN, Turn OFF Time	t <sub>OFF</sub>	See Figure 2		1,3 2			150 300		150 300	

**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+ </sub> = 15 V, V <sub>- </sub> = -3 V V <sub>L </sub> = +5 V, GND = 0 V WR = 0.8 V RS, EN = 2 V		LIMITS						UNIT
				1=25°C		A SUFFIX		D SUFFIX		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
				2=125,85°C	-55 to 125°C	-40 to 85°C				
				3=-55,-40°C						

**DYNAMIC (Cont'd)**

Charge Injection	Q	See Figure 5		1	-70					pC
Chip Disabled Crosstalk (See Figure 8)	XTALK <sub>(CD)</sub>	R <sub>L </sub> = 75Ω f = 5 MHz EN = 0.8 V	PLCC DIP	1 1	-75 -65					dB
Adjacent Input Crosstalk (See Figure 9)	XTALK <sub>(AI)</sub>	R <sub>IN </sub> = 10 Ω R <sub>L </sub> = 10 kΩ f = 5 MHz	PLCC DIP	1 1	-97 -87					
		R <sub>IN </sub> = 75Ω R <sub>L </sub> = 75Ω f = 5 MHz	PLCC DIP	1 1	-80 -70					
All Hostile Crosstalk (See Figure 7)	XTALK <sub>(AH)</sub>	R <sub>IN </sub> = 10 Ω R <sub>L </sub> = 10 kΩ f = 5 MHz	PLCC DIP	1 1	-77 -72					
		R <sub>IN </sub> = 75Ω R <sub>L </sub> = 75Ω f = 5 MHz	PLCC DIP	1 1	-77 -72					
Differential Crosstalk (See Figure 10)	XTALK <sub>(DIFF)</sub>	R <sub>IN </sub> = 10 Ω R <sub>L </sub> = 10 kΩ f = 5 MHz	PLCC DIP	1 1	-84 -84					
		R <sub>IN </sub> = 75Ω R <sub>L </sub> = 75Ω f = 5 MHz	PLCC DIP	1 1	-84 -84					
Bandwidth	BW	R <sub>L </sub> = 50 Ω, See Figure 6		1	500					MHz

**SUPPLY**

Positive Supply Current	I <sub>+</sub>	Any One Channel Selected With Address Inputs at GND or V <sub>+</sub>	1,2 3	0.6		2 5		2 5	mA
Negative Supply Current	I <sub>-</sub>		1,2 3	0.6	-1.8 -2		-1.8 -2		
Operating Supply Voltage Range	V <sub>+</sub> to V <sub>-</sub>	See Figure 13 Functional Test Only	1,2,3		10	21	10	21	V
	V <sub>-</sub> to GND		1,2,3		-5.5	0	-5.5	0	
	V <sub>+</sub> to GND		1,2,3		10	21	10	21	
Logic Supply Current	I <sub>L</sub>		1,2,3	150		500		500	μA

**TIMING**

Reset to Write	t <sub>RW</sub>	See Figure 1	1,2,3		50		50		ns
WR, RS Minimum pulse Width	t <sub>MPW</sub>	See Figure 1	1,2,3		200		200		
A <sub>0</sub> , A <sub>1</sub> , EN Data Valid To Strobe	t <sub>DW</sub>	See Figure 1	1,2,3		100		100		

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V V <sub>L</sub> = +5 V, GND = 0 V WR = 0.8 V RS, EN = 2 V	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>TIMING (Cont'd)</b>									
A <sub>0</sub> , A <sub>1</sub> , EN Data Valid After Strobe	t <sub>WD</sub>	See Figure 1	1,2,3		50		50	ns	
Address Bus Tristate	t <sub>AZ</sub>	See Figure 1	1	50					
Address Bus Output	t <sub>AO</sub>	See Figure 1	1		200		200		
Address Bus Input	t <sub>AI</sub>	See Figure 1	1		200		200		

**NOTES:**

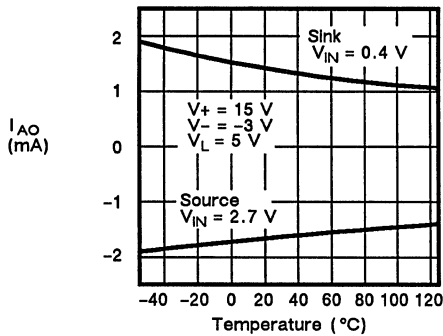
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY at 25°C, not guaranteed nor subject to production testing.
- e. Analog signal range is measured from the GND pin to the designated Source (Input) pin, and indicates the limits of functionality. Performance limits are only guaranteed for stated test conditions.

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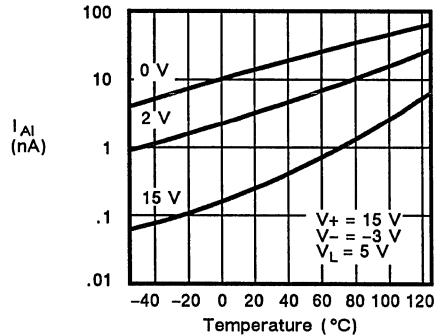
**TYPICAL CHARACTERISTICS**

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Address Output Current vs. Temperature

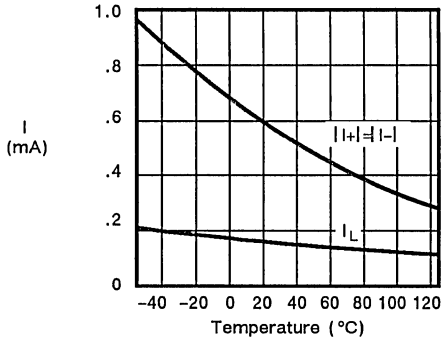


Logic/Address Input Current vs. Temperature

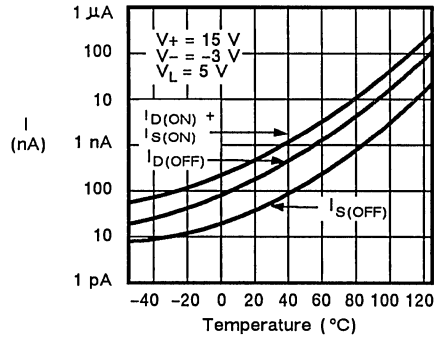


**TYPICAL CHARACTERISTICS**

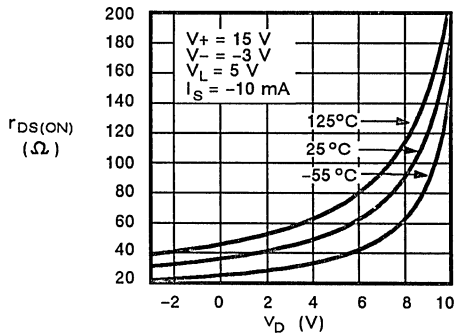
**Supply Currents vs. Temperature**



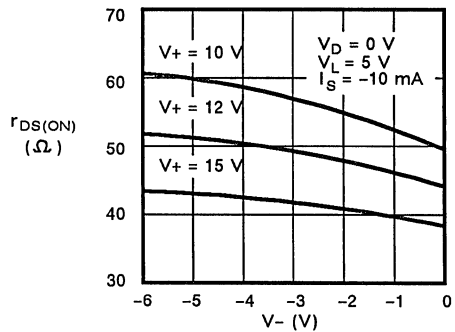
**Leakage vs. Temperature**



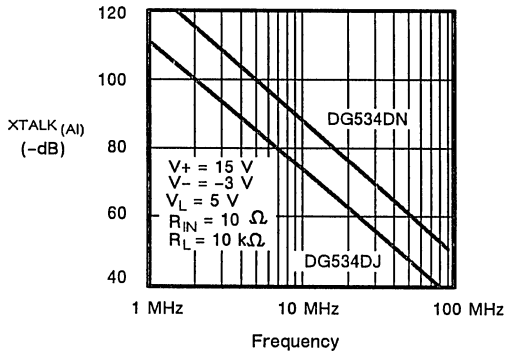
**r<sub>DS(ON)</sub> vs. Drain Voltage**



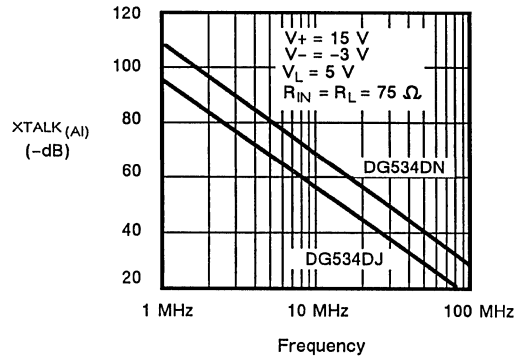
**r<sub>DS(ON)</sub> vs. V-; V+ Constant**



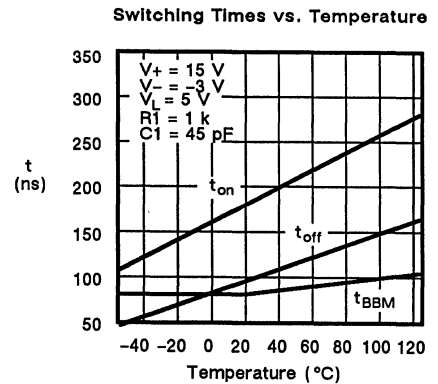
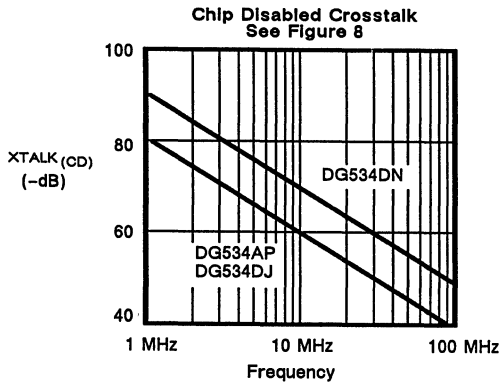
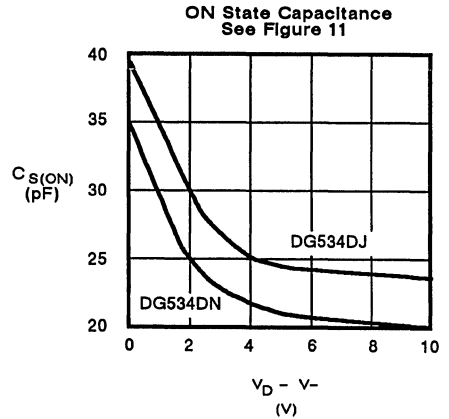
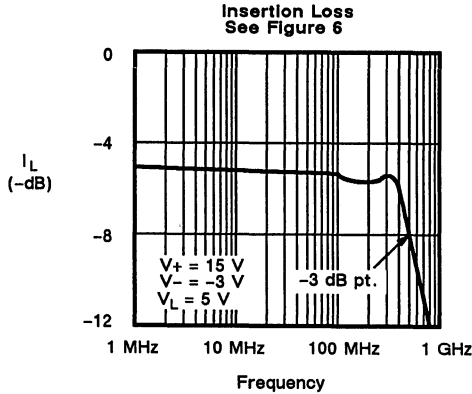
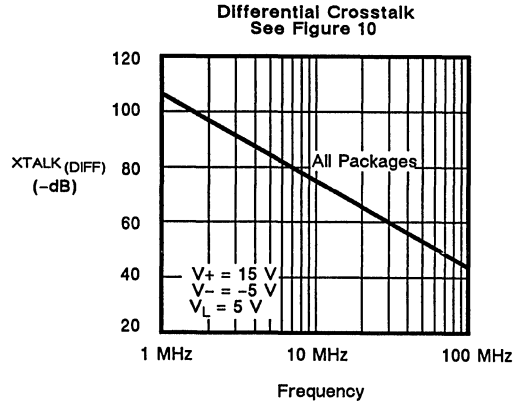
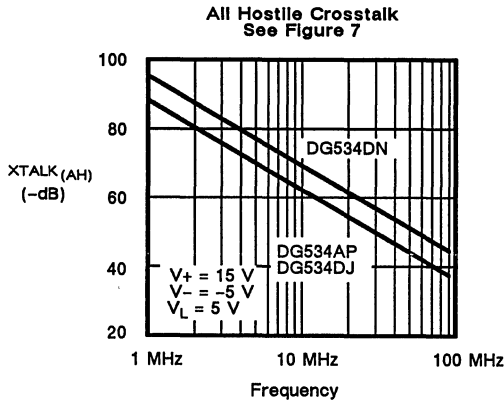
**Adjacent Input Crosstalk**  
See Figure 9



**Adjacent Input Crosstalk**  
See Figure 9

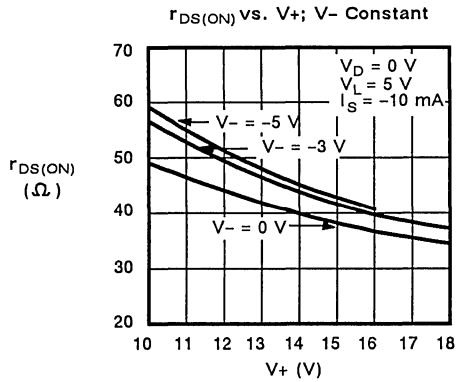


## TYPICAL CHARACTERISTICS (Cont'd)





**TYPICAL CHARACTERISTICS (Cont'd)**



**INPUT TIMING REQUIREMENTS**

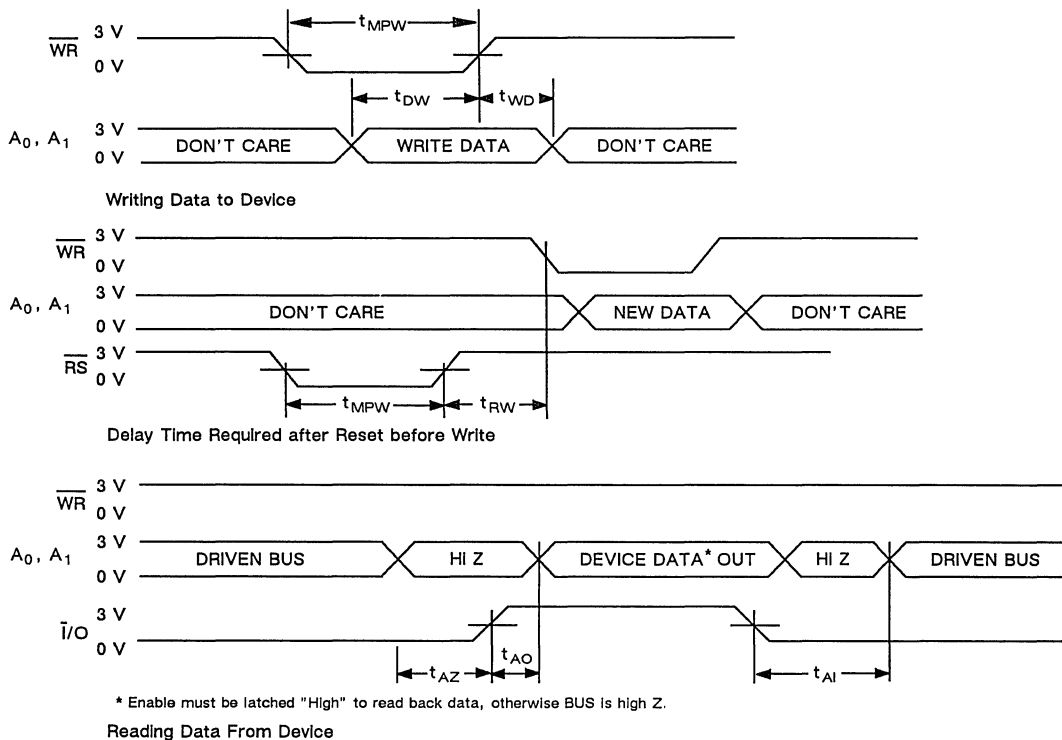


Figure 1

## EN TURN ON/OFF TIME TEST CIRCUIT

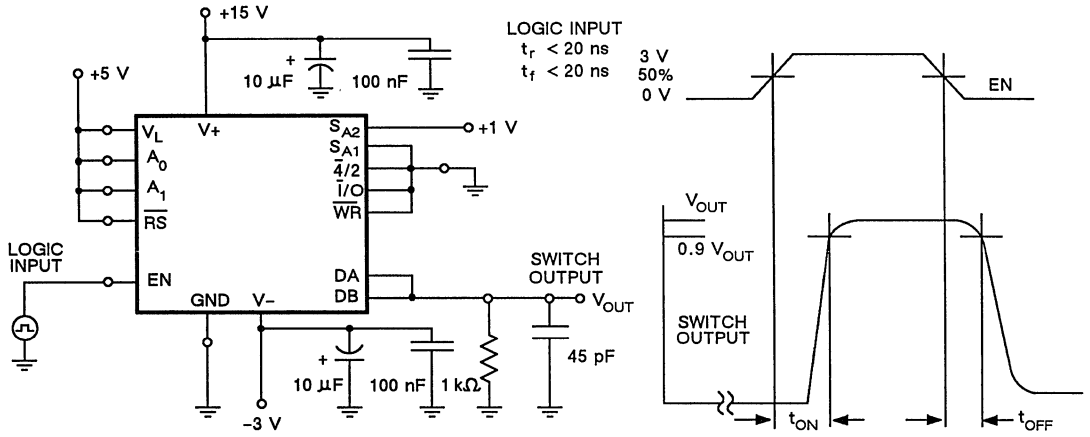


Figure 2

## WR TURN ON TIME TEST CIRCUIT

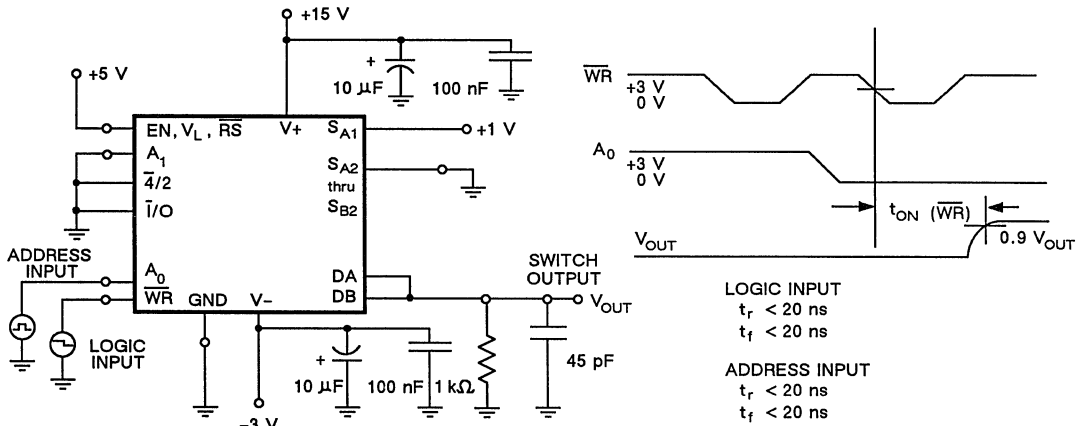


Figure 3

**TRANSITION TIME and BREAK-BEFORE-MAKE INTERVAL TEST CIRCUIT**

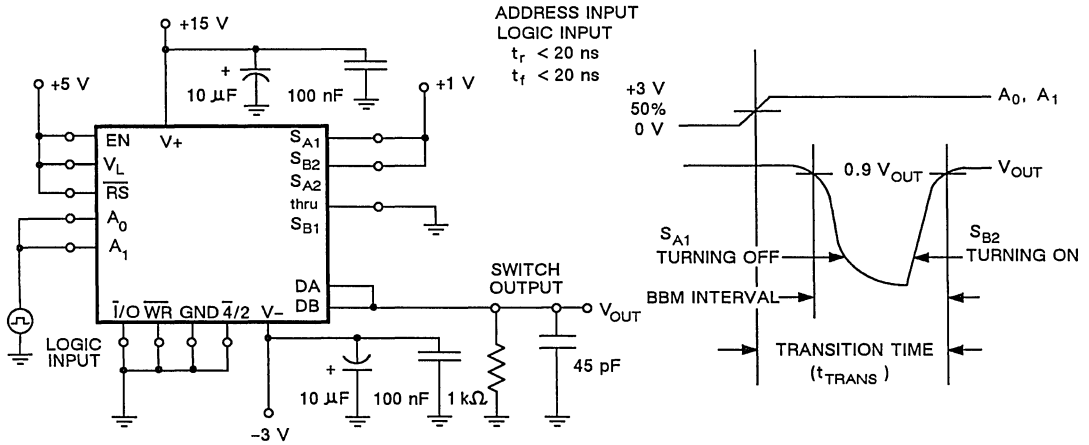


Figure 4

**CHARGE INJECTION TEST CIRCUIT**

**-3 dB BANDWIDTH TEST CIRCUIT**

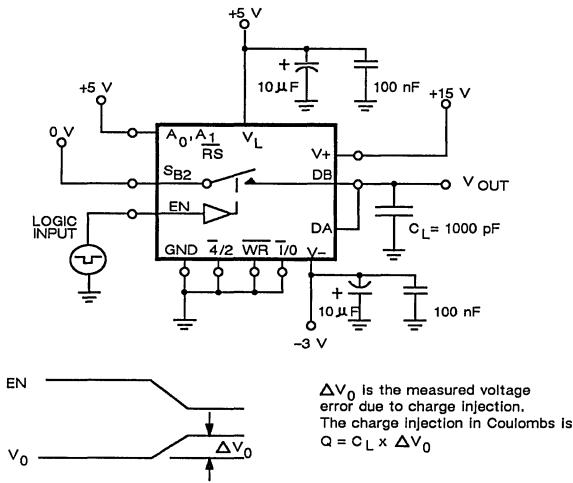


Figure 5

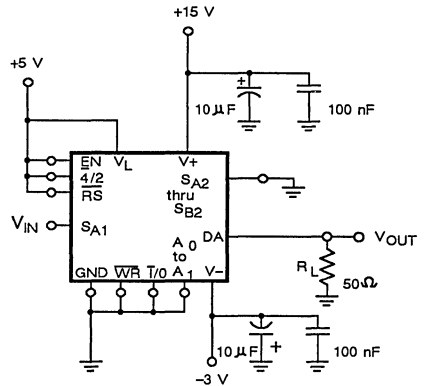
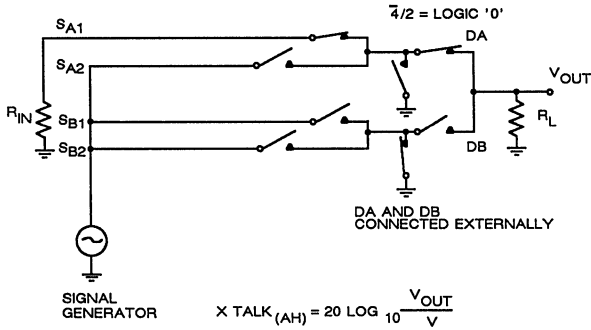


Figure 6

ALL HOSTILE CROSSTALK - X TALK (AH)

CHIP DISABLED CROSSTALK - X TALK (CD)



Note: SA1 on or any other one channel on.

Figure 7

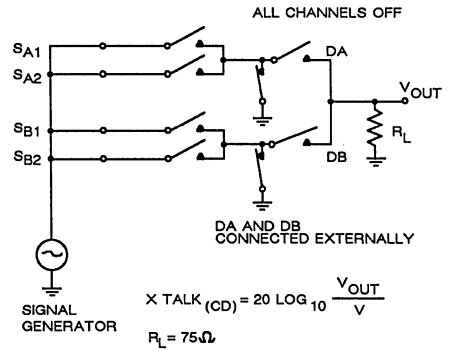


Figure 8

ADJACENT INPUT CROSSTALK - X TALK (AI)

DIFFERENTIAL CROSSTALK - XTALK (DIFF)

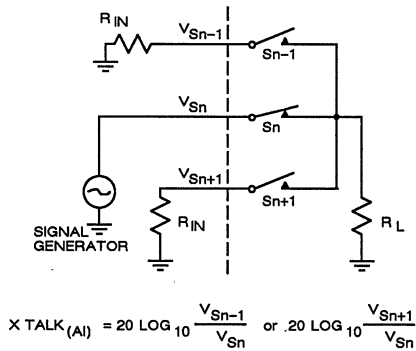


Figure 9

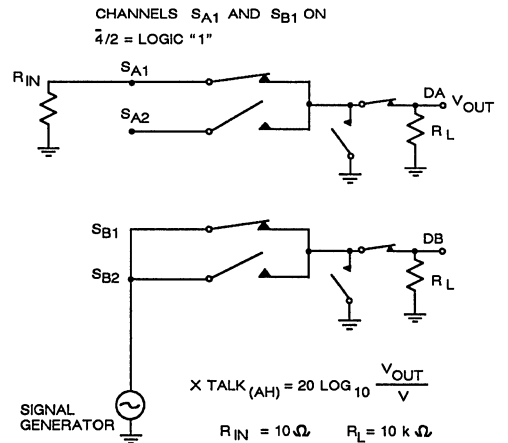


Figure 10

**ON STATE INPUT CAPACITANCE**

**OFF STATE INPUT/OUTPUT CAPACITANCE**

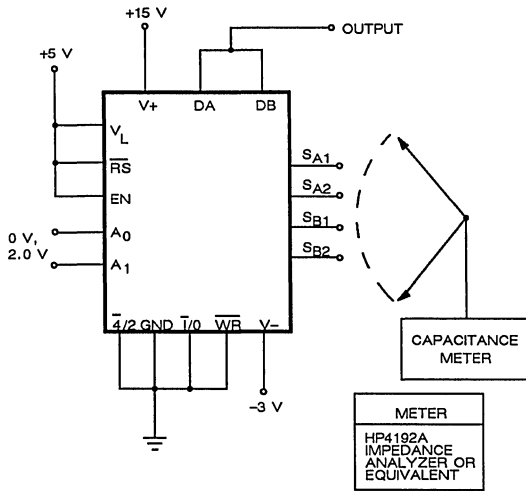


Figure 11

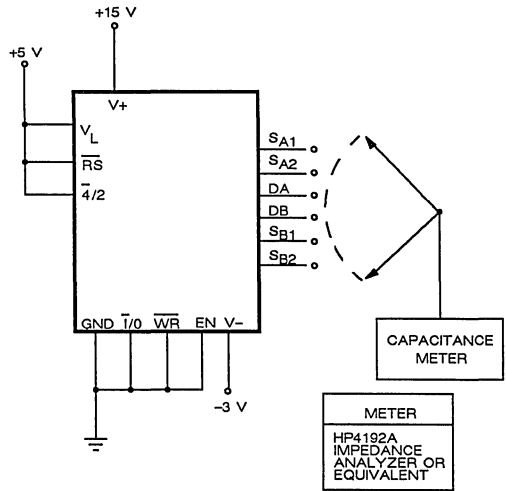
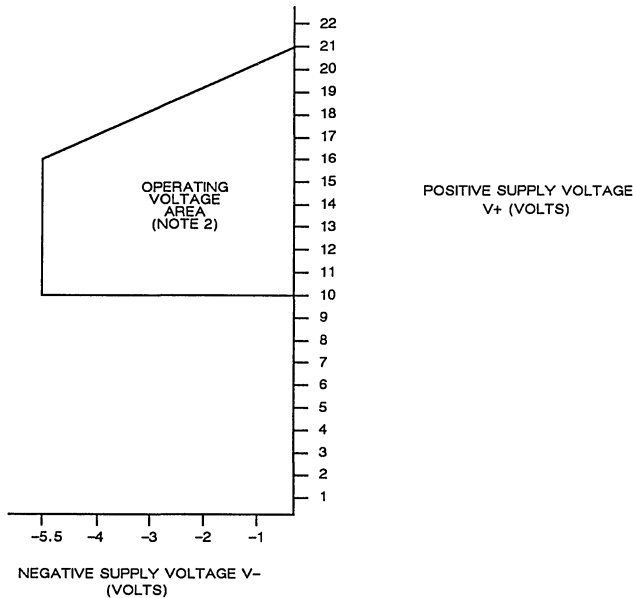


Figure 12

**OPERATING VOLTAGE RANGE**

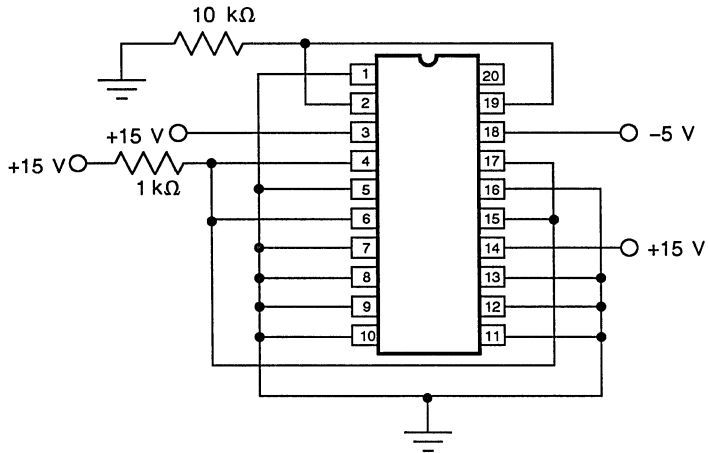


**Note:**

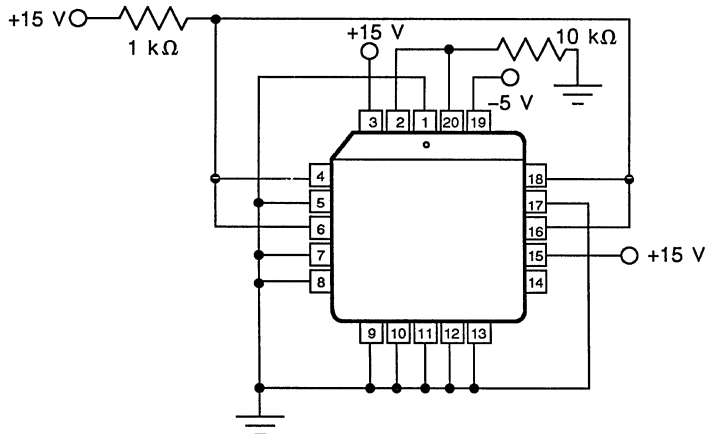
1. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10µF tantalum bead in parallel with 100 nF ceramic disc.
2. Production tested with V+ = 15 V and V- = -3.0 V
3. At VL = 5 V ± 10%, 0.8/2.0 V TTL compatibility is maintained over the entire operating voltage range.

Figure 13

## BURN-IN CIRCUIT - 20-LEAD DUAL-IN-LINE



## BURN-IN CIRCUIT - 20-LEAD PLCC



## PIN DESCRIPTION (DUAL-IN-LINE PACKAGE)

PIN NUMBER	SYMBOL	DESCRIPTION
2	DA	Analog output
3	V+	Positive supply voltage (must be decoupled)
7	$\overline{4/2}$	4 by 1 or 2 by 2 select
8	$\overline{RS}$	Reset
9	$\overline{WR}$	Write command that latches $A_0$ , $A_1$ , EN
10	$A_1$	Binary address inputs that determine which input channel(s) is connected to the output(s)
11	$A_0$	
12	EN	Input to activate multiplexer
13	$\overline{I/O}$	Pin to read from or write to the address latches
14	$V_L$	Logic supply voltage
18	V-	Negative supply voltage (must be decoupled)
19	DB	Analog output
4	$S_{A1}$	Analog input
6	$S_{A2}$	Analog input
15	$S_{B2}$	Analog input
17	$S_{B1}$	Analog input
1, 5, 16	GND	Analog and digital grounds. All GND pins should be connected externally to optimize dynamic performance.
20	NC	No Connection

## APPLICATIONS

### Device Description

The DG534 D/CMOS wideband multiplexer offers 4-channel single-ended or dual 2-channel functions. An  $\overline{4/2}$  logic input pin selects the single-ended or dual mode.

To meet the high dynamic performance demands of video, high definition TV, digital data routing (in excess of 100 Mbps), etc., the DG534 is fabricated with DMOS transistors configured in 'T' arrangements with second level 'L' configurations (see Functional Block Diagram).

Use of DMOS technology yields devices with very low capacitance and low  $r_{DS(ON)}$ . This directly relates to improved high frequency signal handling, higher switching speeds, while maintaining low insertion loss

figures. 'T' and 'L' switch configurations further improve dynamic performance by greatly reducing hostile crosstalk and output node capacitance.

### Frequency Response

A single multiplexer on-channel exhibits both resistance ( $r_{DS(ON)}$ ) and capacitance ( $C_{S(ON)}$ ). This RC combination causes a frequency dependent attenuation of the analog signal. The -3 dB bandwidth of the DG534 is typically 500 MHz (into 50  $\Omega$ ). This figure of 500 MHz illustrates that the switch-channel cannot be represented by a simple RC combination. The ON capacitance of the channel is distributed along the ON resistance, and hence becomes a more complex multi-stage network of R's and C's making up the total  $r_{DS(ON)}$  and  $C_{S(ON)}$ .

### Power Supplies and Decoupling

A useful feature of the DG534 is its power supply flexibility. It can be operated from dual supply, or a single positive supply ( $V_-$  connected to 0 V) if required. Recommended operating voltage range is shown in Figure 13.

Note that the analog signal must not exceed  $V_-$  by more than  $-0.3$  V (see absolute maximum ratings). However, the addition of a  $V_-$  pin has a number of advantages:

- 1) It allows flexibility in analog signal handling, i.e. with  $V_- = -5$  V and  $V_+ = 15$  V, up to  $\pm 5$  V ac signals can be accepted.
  - 2) The value of ON capacitance ( $C_{S(ON)}$ ) may be reduced by increasing the reverse bias across the internal FET body to source junction. For more information see curve of  $C_{S(ON)}$  versus ( $V_D$  minus  $V_-$ ) voltage in typical characteristic data section.  $V_+$  has no effect on  $C_{S(ON)}$ .
- It is useful to note that tests indicate that optimum video differential phase and gain occur when  $V_-$  is  $-3$  V.
- 3)  $V_-$  eliminates the need to bias the analog signal using potential dividers and large decoupling capacitors.

It is established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG534 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

#### Rules:

- (a) Decoupling capacitors should be incorporated on all power supply pins ( $V_+$ ,  $V_-$ ,  $V_L$ ).
- (b) They should be mounted as close as possible to the device pins.
- (c) Capacitors should have good frequency characteristics - tantalum bead and/or ceramic disc types are suitable.

Recommended decoupling capacitors are 1 to 10  $\mu$ F tantalum bead, in parallel with 100 nF ceramic or polyester.

- (d) Additional high frequency protection may be provided by 51  $\Omega$  carbon film resistors con-

nected in series with the power supply pins (see Figure 14).

### Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by the DG534. Some tips for minimizing stray effects are:

- i) Use extensive ground planes on double sided pcb separating adjacent signal paths. Multilayer pcb is even better.
- ii) Keep signal paths as short as practically possible with all-channel paths of near equal length.

Slight improvements in performance can be obtained by using DG534DN parts in preference to DG534DJ. The stray effects of the quad PLCC package are better than those of the 20-pin dual-in-line package.

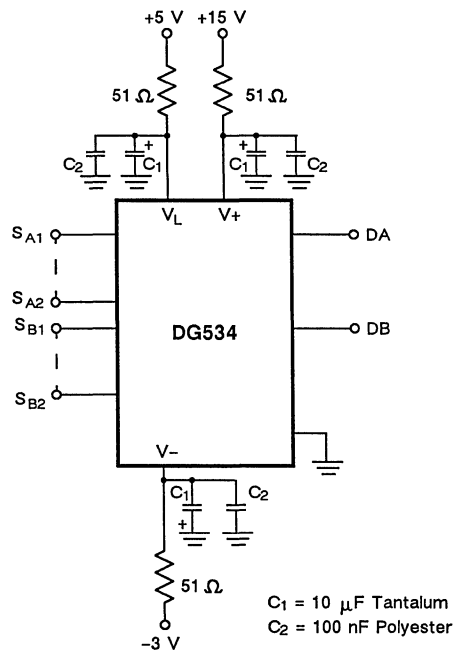


Figure 14. DG534 Power Supply Decoupling



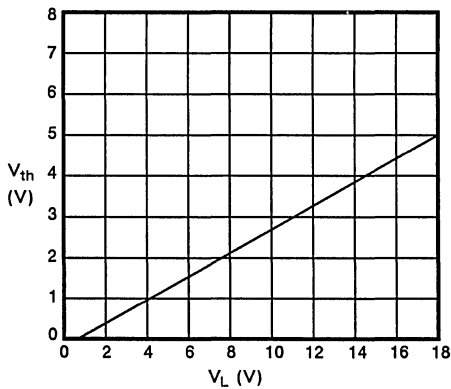
**APPLICATIONS (Cont'd)**

**Interfacing**

Logic interfacing is easily accomplished with the DG534. Comprehensive addressing and control functions are incorporated in the design.

The addition of a  $V_L$  pin permits interface to various logic types. The device is primarily designed to be TTL logic compatible with +5 V applied to  $V_L$ . The DG534 actual switching threshold can be raised simply by increasing  $V_L$ .

A typical DG534 switching threshold versus  $V_L$  is shown in Figure 15.



**Figure 15.** DG534 Switching Threshold Voltage vs.  $V_L$

The device features an address readback (Tally) facility, whereby the last address written to the device may be output to the system. This allows improved status monitoring and handshaking without additional external components.

Output buffers are recommended to reduce insertion loss and to drive coaxial cables. For low power video routing applications or for unity gain input buffers

This function is controlled by the  $\bar{I/O}$  pin, which directly addresses the tri-state buffers applied to the address inputs ( $A_0, A_1$ ). Address inputs can be assigned to accept data (when  $\bar{I/O} = 0; \overline{WR} = 0; \overline{RS} = 1$ ) or output data (when  $\bar{I/O} = 1; \overline{WR} = 1; \overline{RS} = 1$ ) or reflect a high impedance and latched state (when  $\bar{I/O} = 0; \overline{WR} = 1; \overline{RS} = 1$ ).

NOTE: ( $\overline{EN}$ ) must be latched HIGH to allow proper readback, otherwise readback is suppressed.

When the  $\bar{I/O}$  assigns the address output condition, the address output can sink or source current for logic low and high respectively. Note that  $V_L$  is the logic high output condition. This point must be respected if  $V_L$  is varied for input logic threshold shifting.

Note:  $V_L$  must not exceed  $V+$  by more than +0.3 V. This must also apply when the power supply is turned on, i.e.  $V+$  must rise ahead of  $V_L$ .

Further control pins facilitate easy microprocessor interface. On chip address, data latches are activated by  $\overline{WR}$ , which serves as a strobe type function eliminating the need for peripheral latch or memory  $\bar{I/O}$  port devices. Also, for ease of interface, a direct reset function ( $\overline{RS}$ ) allows all latches to be cleared and switches opened. Reset should be used during power up, etc., to avoid spurious switch action. See Figure 16.

Channel address data can only be entered during  $\overline{WR}$  low, when the address latches are transparent and  $\bar{I/O}$  is low. Similarly data readback is only operational when  $\overline{WR}$  and  $\bar{I/O}$  are high.

Siliconix 2N5911/2N5912 JFETs may be employed in source-follower buffer circuits as shown in figure 17.

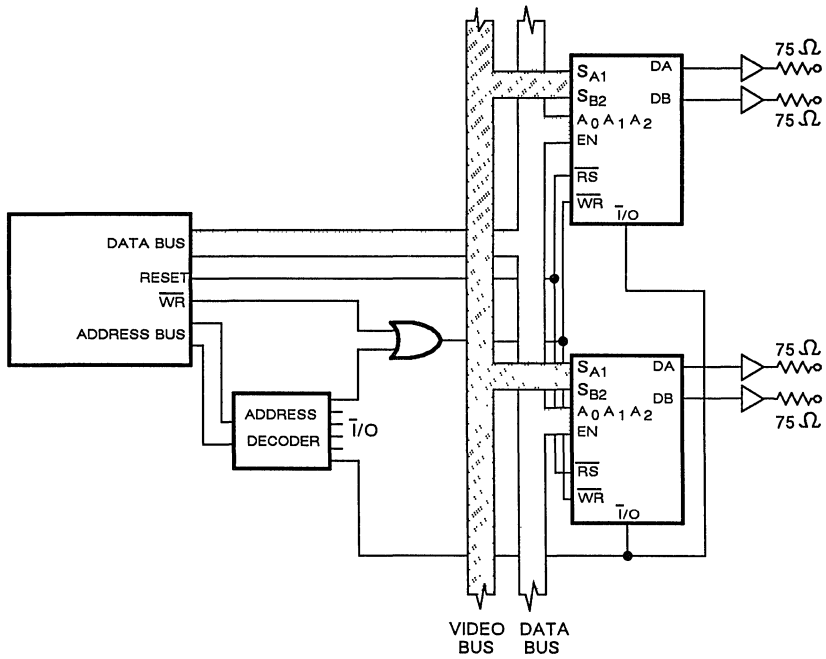


Figure 16. DG534 in a Video Matrix

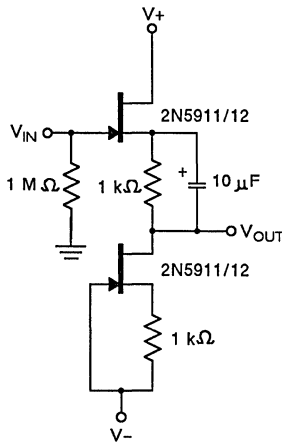


Figure 17. Discrete Video Buffer

# DG535

## 16-Channel Wideband/Video Multiplexer

### FEATURES

- -83 dB Single Channel Crosstalk at 5 MHz
- > 200 MHz Bandwidth
- 3 pF Input Capacitance
- 9 pF Output Capacitance
- Low Power (75  $\mu$ W)
- 90  $\Omega$  (max)  $r_{DS(ON)}$
- $\mu$ P Interface Latches
- Fast Switching (300 ns)
- ESDS Protection >  $\pm 4000$  V

### BENEFITS

- Improved Isolation Between Channels
- Reduced Insertion Loss at High Frequencies
- Allows Formation of Large Matrices
- Minimizes System Power
- Simplifies  $\mu$ P Interface
- Improves Data Throughput

### APPLICATIONS

- Video Switching/Routing
- High Speed Data Routing
- Wideband Signal Multiplexing
- Crosspoint Arrays
- Precision Data Acquisition
- FLIR Systems
- $\mu$ P-Based Systems

### DESCRIPTION

The DG535 is a 16-channel multiplexer designed for routing one of 16 wideband analog or digital input signals to a single output. It features low input and output capacitance, low ON resistance, and n-channel DMOS "T" switches, resulting in wide bandwidth, low crosstalk and high "OFF" isolation. The switch FETs were designed to pass signals in either direction, allowing the DG535 to be used as a demultiplexer as well as a multiplexer.

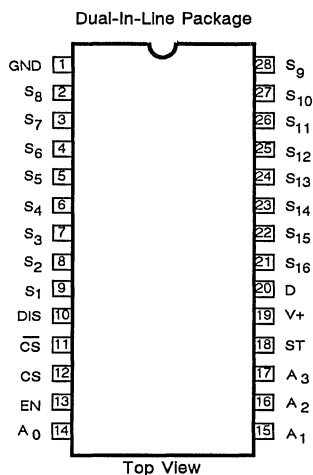
The DG535 includes on-board data latches and decode logic, facilitating a simplified microprocessor interface. Additional Chip Select and Enable inputs simplify addressing in larger matrices. The fast transition time of 300 ns (max) and low ON resistance 90  $\Omega$  (max) makes the DG535 ideal for multiplexing high speed signals through precision data acquisition systems. Single-supply operation and a low 75  $\mu$ W power dissipation allow operation in battery powered systems and in multi-channel crosspoints and multiplexers with vastly reduced power supply requirements.

The technology used in the DG535 is called D/CMOS. This process combines low-capacitance DMOS FETs on the same substrate with dense, high-speed, low-power CMOS. The DMOS FETs are configured as "T" switches to improve OFF isolation and reduce crosstalk. The CMOS devices form all of the latches, decode logic and switch driver circuitry, resulting in a combination of high performance and high functional integration.

The DG535 is available in the plastic 28-lead DIP for the industrial, D suffix (-40 to 85°C), and the 28-lead side braze DIP for military, A suffix (-55 to 125°C) temperature range operations. For surface mount versions, see the DG536 data sheet.

For more information on the DG535, please refer to Siliconix Application Note AN86-1.

### PIN CONFIGURATION

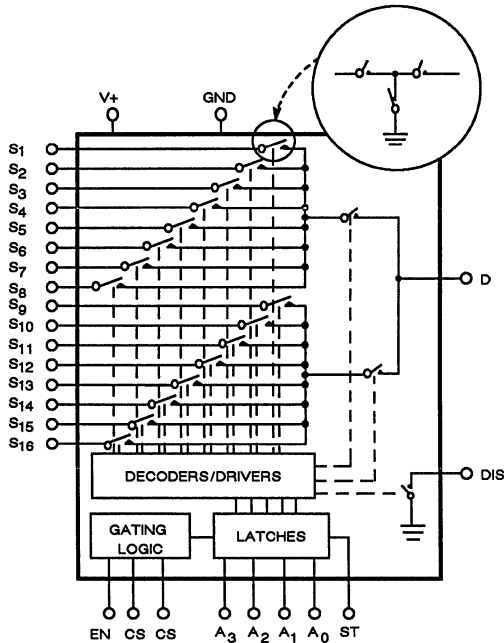


#### Ordering Information:

DG535AP	DG535DJ
DG535AP/883	Plastic DIP
Side Braze DIP	

## FUNCTIONAL BLOCK DIAGRAM

## TRUTH TABLE



EN	CS	$\overline{\text{CS}}$	ST	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Input Channel Selected	Disable Output
0	X	X						NONE	HIGH Z
X	0	X	1	X	X	X	X		
X	X	1							
					0	0	0	S1	LOW Z
					0	0	0	S2	
					0	0	1	S3	
					0	0	1	S4	
					0	1	0	S5	
					0	1	0	S6	
					0	1	1	S7	
1	1	0	1	0	1	1	1	S8	
					1	0	0	S9	
					1	0	0	S10	
					1	0	1	S11	
					1	0	1	S12	
					1	1	0	S13	
					1	1	0	S14	
					1	1	1	S15	
					1	1	1	S16	
X	X	X	0	X	X	X	X	Maintains previous switch condition	HIGH Z or LOW Z

Logic "1" :  $V_{AH} \geq 10.5 \text{ V}$

Logic "0" :  $V_{AL} \leq 4.5 \text{ V}$

1. LOW Z, HIGH Z = Impedance of Disable Output to GND. Disable output is current sink when any channel is selected.
2. Strobe Input (ST) is level triggered.

## ABSOLUTE MAXIMUM RATINGS

V<sub>+</sub> to GND ..... -0.3 V to +18 V

Digital Inputs ..... (GND - 0.3 V) to (V<sub>+</sub> plus 2 V)  
..... or 20 mA, whichever occurs first

V<sub>S</sub>, V<sub>D</sub> ..... (GND - 0.3 V) to (V<sub>+</sub> plus 2 V)  
..... or 20 mA, whichever occurs first

Current (any terminal) Continuous ..... 20 mA

Current (S or D) Pulsed 1 ms 10% duty cycle .... 40 mA

Storage Temperature (A Suffix) ..... -65 to 150°C

(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C

(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*

28-Pin Plastic DIP\*\* ..... 625 mW

28-Pin Side Braze DIP\*\*\* ..... 1200 mW

\* All leads welded or soldered to PC board.

\*\* Derate 8.3 mW/°C above 75°C

\*\*\* Derate 16 mW/°C above 75°C

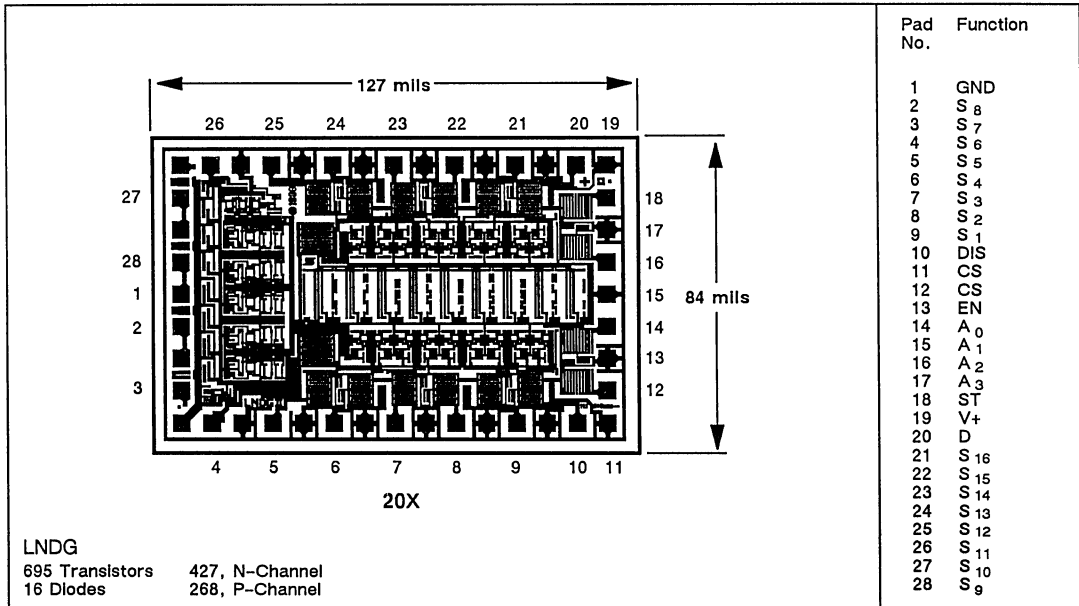
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $GND = 0\text{ V}$ $ST, \overline{CS} = 10.5\text{ V}$ $\overline{CS} = 4.5\text{ V}$	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>d</sup>	$V_{ANALOG}$		1		0	10	0	10	V
Drain - Source ON Resistance	$r_{DS(ON)}$	$I_S = -1\text{ mA}$ , $V_D = 3\text{ V}$ $V_{AH} = 4.5\text{ V}$ , $V_{AL} = 10.5\text{ V}$ Sequence Each Switch ON $EN = 10.5\text{ V}$	1,3 2	55		90 120		90 120	$\Omega$
Resistance Match Between Channels	$\Delta r_{DS(ON)}$		1			9		9	
Source OFF Leakage Current	$I_{S(OFF)}$	$V_S = 3\text{ V}$ , $V_D = 0\text{ V}$ $EN = 4.5\text{ V}$	1 2		-10 -100	10 100	-10 -100	10 100	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	$V_S = 0\text{ V}$ , $V_D = 3\text{ V}$ $EN = 4.5\text{ V}$	1 2		-10 -500	10 500	-10 -100	10 100	
Total Switch ON Leakage Current	$I_{D(ON)}$	$V_S = V_D = 3\text{ V}$ $EN = 10.5\text{ V}$	1 2		-10 -1000	10 1000	-10 -100	10 100	
Disable Output	$R_{DISABLE}$	$I_{DISABLE} = 1\text{ mA}$ $EN = 10.5\text{ V}$	1,3 2	100		200 250		200 250	$\Omega$
<b>INPUT</b>									
Input Voltage High	$V_{AIH}$		1,2,3		10.5		10.5		V
Input Voltage Low	$V_{AIL}$		1,2,3			4.5		4.5	
Address Input Current	$I_{AI}$	$V_{AI} = 0\text{ V}$ or $15\text{ V}$	1,3 2	<0.01	-10 -100	10 100	-10 -100	10 100	nA
<b>DYNAMIC</b>									
ON State Input Cap.	$C_{S(ON)}$	$V_D = V_S = 3\text{ V}$	1	40					pF
OFF State Input Cap.	$C_{S(OFF)}$	$V_S = 3\text{ V}$	1	3					
OFF State Output Cap.	$C_{D(OFF)}$	$V_D = 3\text{ V}$	1	9					
Multiplexer Switching Time	$t_{TRANS}$	See Figure 4	1 2,3			300 300		300	ns
Break-Before-Make Interval	$t_{OPEN}$	See Figure 4	1 2,3		25 25		25		
EN, CS, $\overline{CS}$ , ST Turn ON Time	$t_{ON}$	See Figures 2 & 3	1 2,3			300 300		300	
EN, CS, $\overline{CS}$ Turn OFF Time	$t_{OFF}$	See Figure 2	1 2,3			150 150		150	
Charge Injection	Q	See Figure 5	1	-35					

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = 15 V, GND = 0 V ST, CS = 10.5 V CS̄ = 4.5 V	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
Single-Channel Crosstalk	XTALK <sub>(SC)</sub>	R <sub>IN</sub> = 75 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz See Figure 9	1	-83					dB
Chip Disabled Crosstalk (See Figure 8)	XTALK <sub>(CD)</sub>	R <sub>L</sub> = 75 kΩ, f = 5 MHz EN = 0.8 V	1	-60					
Adjacent Input Crosstalk (See Figure 10)	XTALK <sub>(AI)</sub>	R <sub>IN</sub> = 10 Ω, R <sub>L</sub> = 10 kΩ f = 5 MHz	1	-72					
All Hostile Crosstalk (See Figure 7)	XTALK <sub>(AH)</sub>		1	-60					
Bandwidth	BW	R <sub>L</sub> = 75 kΩ, See Figure 6	1	>200					MHz
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	Any One Channel Selected With Address Inputs at GND or V <sub>+</sub>	1,3 2	5		50 100		50 100	μA
Operating Supply Voltage Range	V <sub>+</sub> to GND		1,2,3		10	16.5	10	16.5	V
<b>MINIMUM INPUT TIMING REQUIREMENTS</b>									
Strobe Pulse Width	t <sub>SW</sub>	See Figure 1	1,2,3		200		200		ns
A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> , CS, CS̄, EN Data Valid To Strobe	t <sub>DW</sub>	See Figure 1	1,2,3		100		100		
A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> , CS, CS̄, EN Data Valid After Strobe	t <sub>WD</sub>	See Figure 1	1,2,3		50		50		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. Analog signal range is measured from the GND pin to the designated Source (Input) pin.

**DIE TOPOGRAPHY**



**INPUT TIMING REQUIREMENTS**

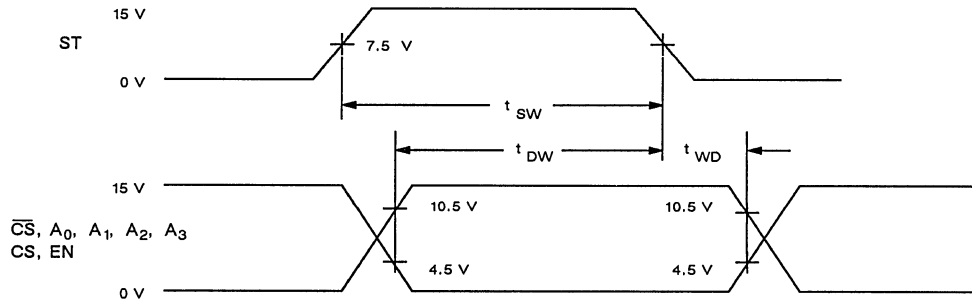


Figure 1

## EN, CS, $\overline{CS}$ , TURN ON/OFF TIME TEST CIRCUIT

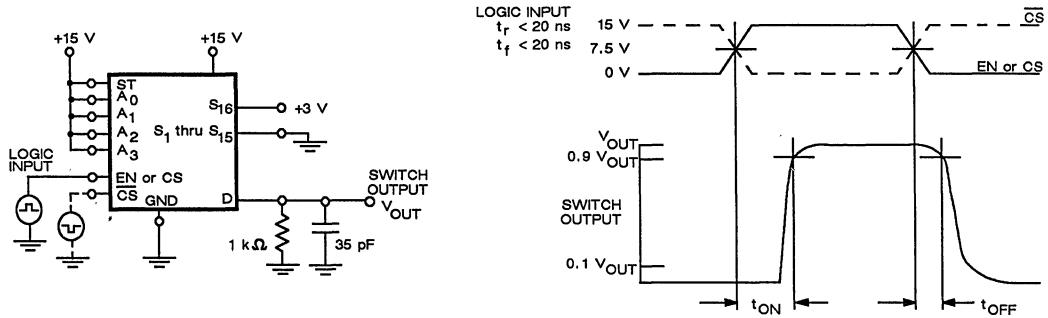


Figure 2

## STROBE (ST) TURN ON TIME TEST CIRCUIT

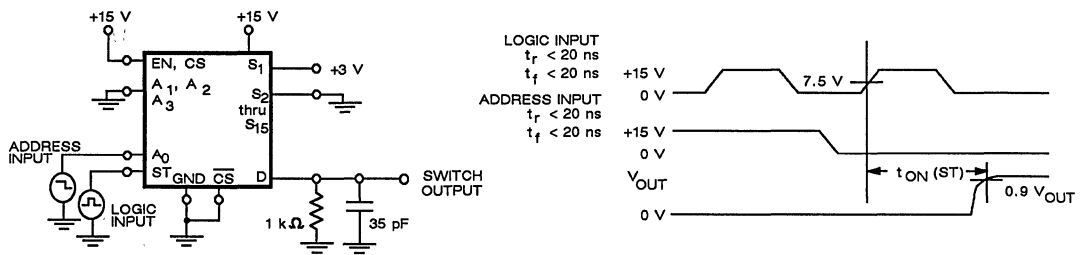


Figure 3

## TRANSITION TIME and BREAK-BEFORE-MAKE INTERVAL TEST CIRCUIT

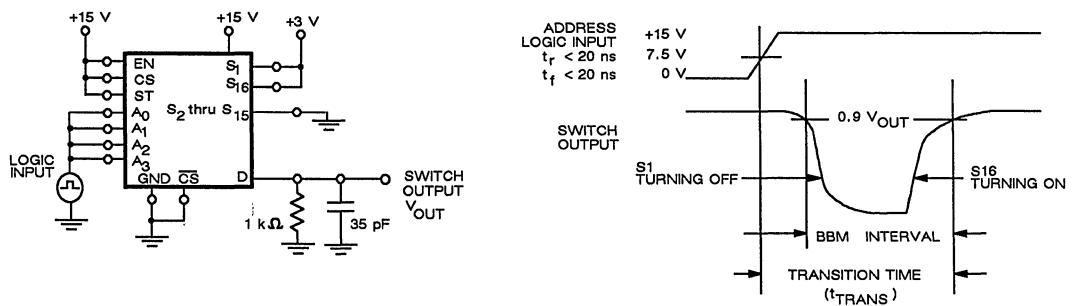


Figure 4



**CHARGE INJECTION TEST CIRCUIT**

**BANDWIDTH TEST CIRCUIT**

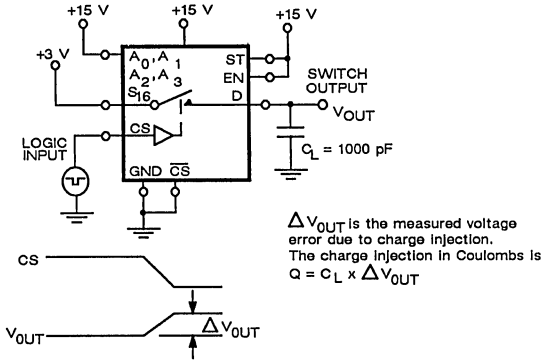


Figure 5

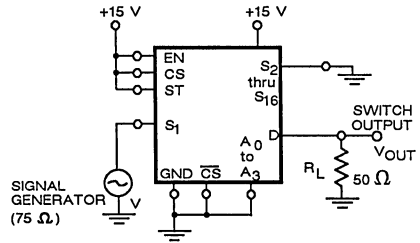


Figure 6

**ALL HOSTILE CROSSTALK - X TALK (AH)**

**CHIP DISABLED CROSSTALK - X TALK (CD)**

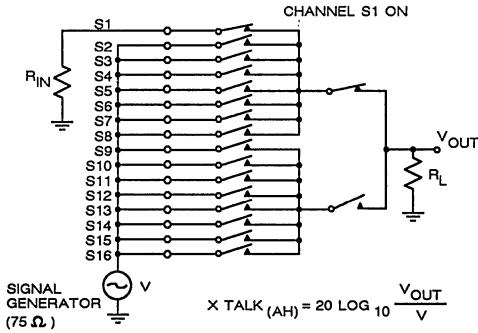


Figure 7

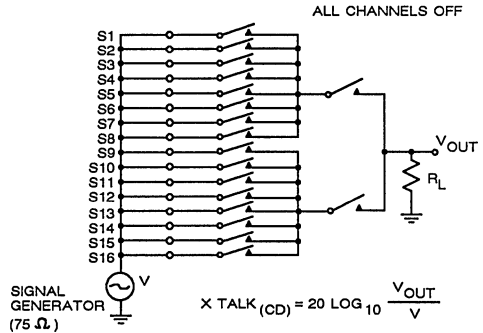
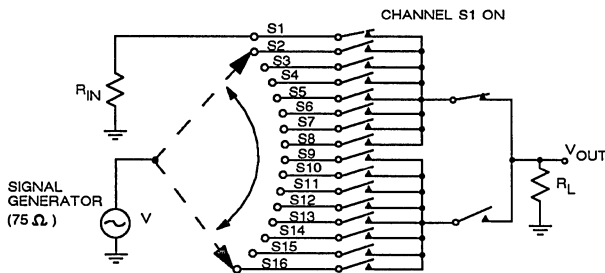


Figure 8



**SINGLE CHANNEL CROSSTALK - X TALK (SC)**

**ADJACENT INPUT CROSSTALK - X TALK (AI)**



- NOTES:
1. Any individual channel between S2 and S16 can be selected
  2.  $X TALK_{(SC)} = \text{Average value of } 20 \text{ LOG } 10 \frac{V_{OUT}}{V}$  is scanned sequentially from S2 to S16

Figure 9

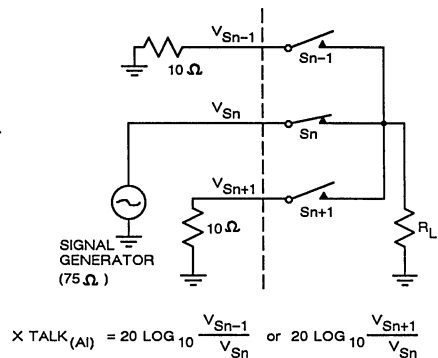
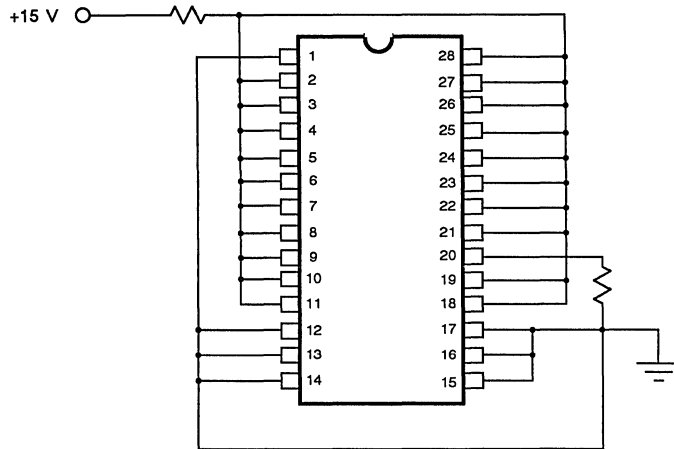


Figure 10

## BURN-IN CIRCUIT

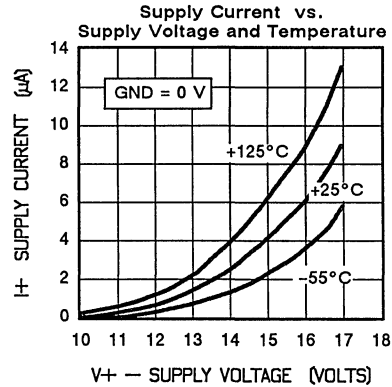
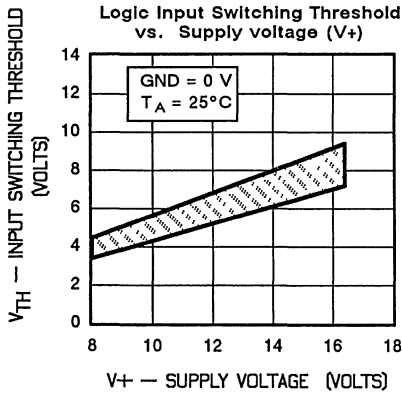
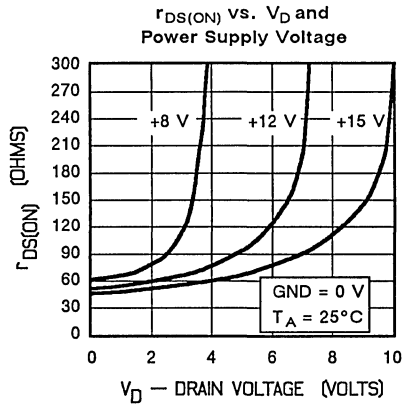
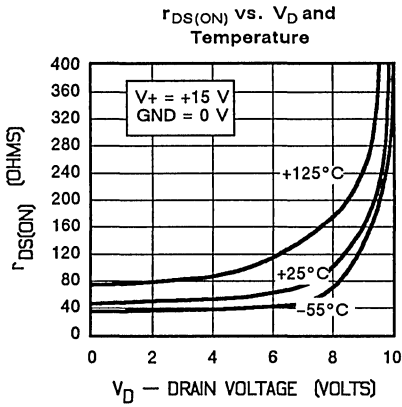


Note: All Resistors are 10 k $\Omega$  unless otherwise specified

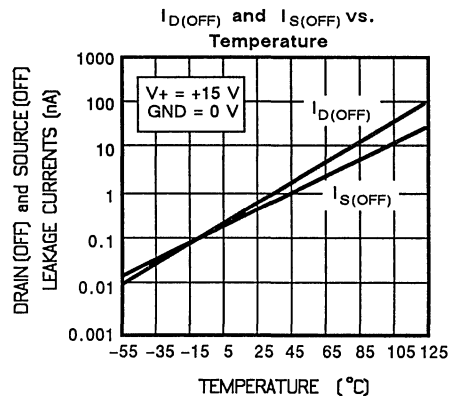
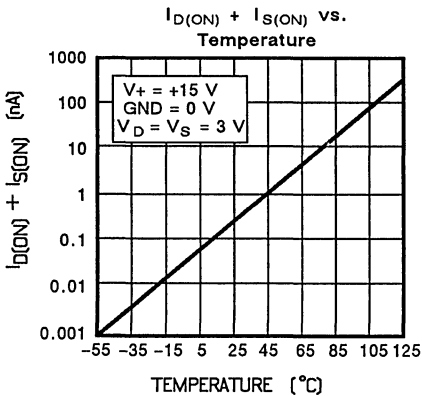
## PIN DESCRIPTION

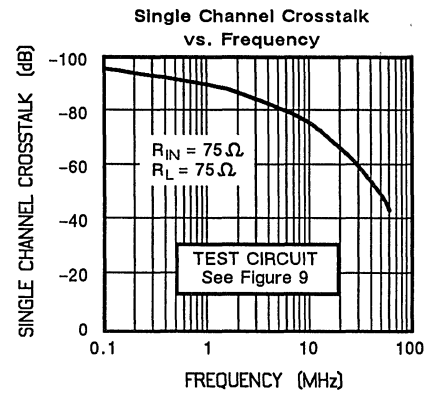
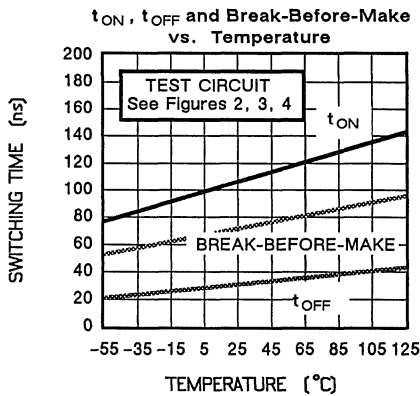
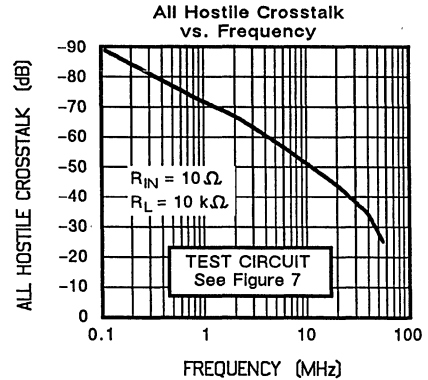
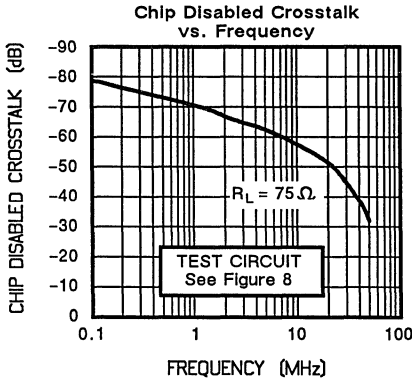
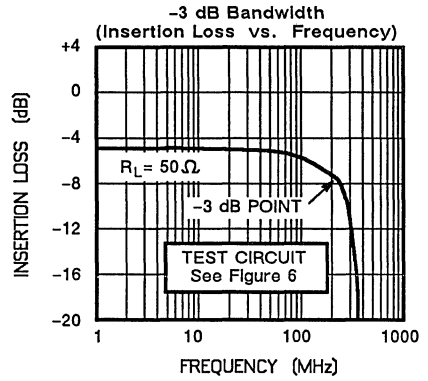
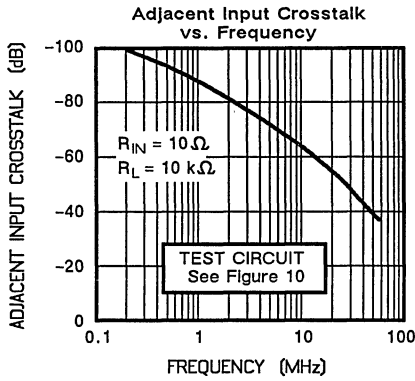
PIN NUMBER	SYMBOL	DESCRIPTION
1	GND	Analog Signal Ground and Most Negative Potential
2	S8	Channel 8 Analog Input
3	S7	Channel 7 Analog Input
4	S6	Channel 6 Analog Input
5	S5	Channel 5 Analog Input
6	S4	Channel 4 Analog Input
7	S3	Channel 3 Analog Input
8	S2	Channel 2 Analog Input
9	S1	Channel 1 Analog Input
10	DIS	Open drain high Impedance output when DG535 is disabled (all channels OFF). When DG535 is enabled (any channel selected) this output is current sink to Analog GND.
11,12,13	$\overline{CS}$ , CS, EN	Logic inputs to select required Multiplexer(s) when using several Multiplexers in a system
14 - 17	A <sub>0</sub> - A <sub>3</sub>	Four binary address inputs that determine which one of the sixteen channels is selected.
18	ST	Strobe input that latches A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> , $\overline{CS}$ , CS, EN
19	V+	Positive supply voltage
20	D	Analog output of Multiplexer or Analog Input if device used in Demultiplexer configuration.
21	S16	Channel 16 Analog Input
22	S15	Channel 15 Analog Input
23	S14	Channel 14 Analog Input
24	S13	Channel 13 Analog Input
25	S12	Channel 12 Analog Input
26	S11	Channel 11 Analog Input
27	S10	Channel 10 Analog Input
28	S9	Channel 9 Analog Input

TYPICAL CHARACTERISTICS



7





**DETAILED DESCRIPTION**

The DG535 is a 16-channel single-ended multiplexer with on-chip address logic and control latches.

The circuit connects one of sixteen inputs (S1, S2,...S16) to a common output (D) under the control of a 4 bit binary address (A<sub>0</sub> to A<sub>3</sub>). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of 3 independent logic inputs (EN, CS and  $\overline{CS}$ ) are provided on chip. These inputs are gated together (see Figure 11) and only when EN = CS = 1 and  $\overline{CS}$  = 0 is true can an output switch be selected by the appropriate address input (A<sub>0</sub> to A<sub>3</sub>). This necessary logic condition can then be latched by Strobe (ST) going low.

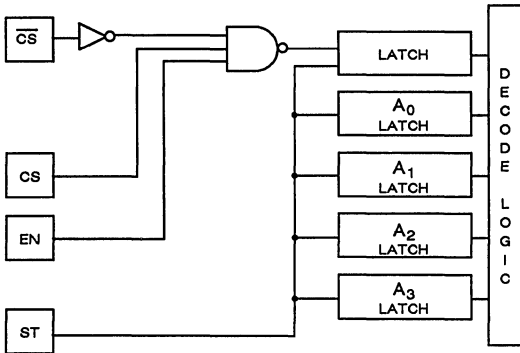


Figure 11.  $\overline{CS}$ , CS, EN, ST Control Logic

Break-before-make switching is included to prevent momentary shorting of an input channel when changing from one input to another.

The device features a two-level switch arrangement whereby two banks of eight switches (first level) are

connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure 12).

With this method SW2 operates out of phase with SW1 and SW3. In the ON condition SW1 and SW3 are closed with SW2 open whereas in the OFF condition SW1 and SW3 are open and SW2 closed. In the OFF condition the input to SW3 is effectively the isolation leakage of SW1 working into the ON resistance of SW2 (typically 200  $\Omega$ ).

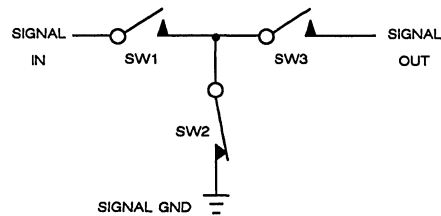


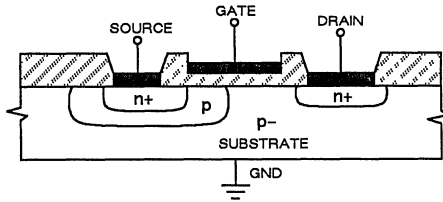
Figure 12. "T" Switch Arrangement

The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output (Pin 7) can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG535 has extensive applications where any high frequency video, audio or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using N channel DMOS FETs for the "T" and series switches.

A cross section of a switch is shown in Figure 13.



**Figure 13.** Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure 13 that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e. 20 mA).

Since no PN junctions exist between the signal path and V+, positive overvoltages are not a problem, unless the breakdown voltage of the DMOS source terminal (see Figure 13) (+18 V) is exceeded. Positive overvoltage conditions must not exceed +18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown occurring.

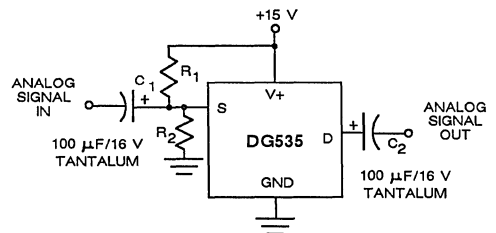
The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device

### DC BIASING

To avoid negative overvoltage conditions and subsequent distortion of analog signals, dc biasing

is necessary. Biasing is not required, however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to  $\pm 200$  mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure 14.



**Figure 14.** Simple Bias Circuit

R1 and R2 are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase performance. Capacitor C1 blocks the DC bias voltage from being coupled back to the analog signal source and C2 blocks the DC bias from the output signal. Both C1 and C2 should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies.

Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method would be to offset the supply voltages (see Figure 15).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.

**DETAILED DESCRIPTION (Cont'd)**

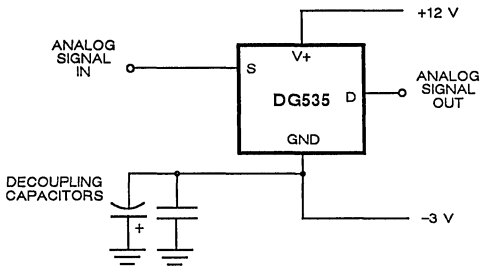


Figure 15. DG535 With Offset Supply

**Note:** TTL to CMOS level shifting is easily obtained by using a MC14504B.

**CIRCUIT LAYOUT**

Good circuit board layout and extensive shielding is essential for optimizing the high frequency performance of the DG535. Stray capacitances on

the PC board and/or connecting leads will considerably degrade the A.C. performance. Hence, signal paths must be kept as short as practically possible, with extensive ground planes separating signal tracks.

**8-CHANNEL VIDEO MULTIPLEXING**

If only 8 channels are needed, the crosstalk can be further reduced by using inputs from the top and bottom halves of the DG535 two-level switching architecture and grounding alternating signal input pins. For example, use S1, S3, S5, S7, S9, S11, S13, and S15 for the signal paths and ground the remaining inputs S2, S4, ... S16 and provide a logic "0" to A<sub>0</sub>. This will provide additional shielding between channels for reduced crosstalk, and the eight signal channels will be addressed via the three addressing MSBs (Figure 16).

For higher frequency applications or applications where even lower levels of crosstalk are required, the Siliconix DG536 is recommended.

**Truth Table**

EN	CS	$\overline{CS}$	ST	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	Input Channel Selected	Disable Output
0	X	X						NONE	HIGH Z
X	0	X	1	X	X	X	X		
X	X	1							
1	1	0	1	0	0	0	0	S1	LOW Z
				0	0	1	0	S3	
				0	1	0	0	S5	
				0	1	1	0	S7	
				1	0	0	0	S9	
				1	0	1	0	S11	
				1	1	0	0	S13	
				1	1	1	0	S15	
X	X	X	0	X	X	X	X	Maintains previous switch condition	HIGH Z or LOW Z

Logic " 1 " : V<sub>AH</sub> ≥ 10.5 V  
 Logic " 0 " : V<sub>AL</sub> ≤ 4.5 V

**Pinout**

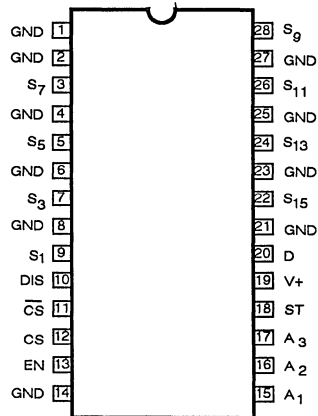


Figure 16. The DG535 as an 8-Channel Video Multiplexer

## 16-Channel Wideband/Video Multiplexer

### FEATURES

- -100 dB Single Channel Crosstalk at 5 MHz
- 300 MHz Bandwidth
- 4 pF (max) Input and 12 pF Output Capacitance
- Low Power (75  $\mu$ W)
- 90  $\Omega$  (max)
- $\mu$ P Interface Latches
- ESDS Protection >  $\pm$  4000

### BENEFITS

- Improved OFF Isolation
- Reduced Insertion Loss at High Frequencies
- Reduced Input Buffer Requirements
- Minimizes System Power
- Reduced Noise
- Simplifies Bus Interface

### APPLICATIONS

- Video Switching/Routing
- High Speed Data Routing
- Wideband Signal Multiplexing
- Precision Data Acquisition
- Crosspoint Arrays
- FLIR Systems
- Audio Switching

### DESCRIPTION

The DG536 is a 16-Channel multiplexer designed for routing one of 16 wideband analog or digital input signals to a single output. It features low input and output capacitance, low ON resistance, and n-channel DMOS "T" switches, resulting in wide bandwidth, low crosstalk and high "OFF" isolation. The switch FETs were designed to pass signals in either direction, allowing the DG536 to be used as a demultiplexer as well as a multiplexer.

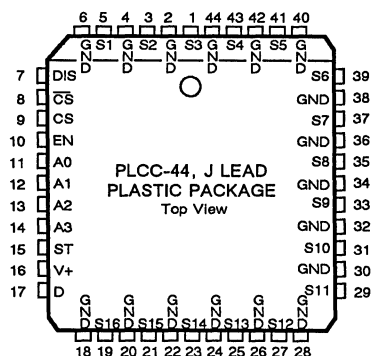
The DG536 includes on-board data latches and decode logic, facilitating a simplified microprocessor interface. Additional Chip Select and Enable inputs simplify addressing in larger matrices. The fast transition time of 300 ns (max) and low ON resistance 90  $\Omega$  (max) makes the DG536 ideal for multiplexing high speed signals through fast data acquisition systems. Single-supply operation and a low 75  $\mu$ W power dissipation allows operation in battery powered systems and in multi-channel crosspoints and multiplexers with vastly reduced power supply requirements.

The technology used in the DG536 is called D/CMOS. This process combines low-capacitance DMOS FETs on the same substrate with dense, high-speed, low-power CMOS.

The DG536 is available in the plastic PLCC-44 for industrial, D suffix (-40 to 85°C), and the 44-lead ceramic J-lead hermetic package for military, A suffix (-55 to 125°C) temperature ranges. For through-hole (DIP) versions, see the DG535 data sheet.

For more information on the DG536, please refer to Siliconix Application Note AN86-1.

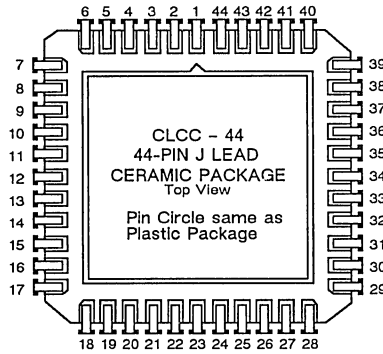
### PIN CONFIGURATION



Order Number:  
DG536DN



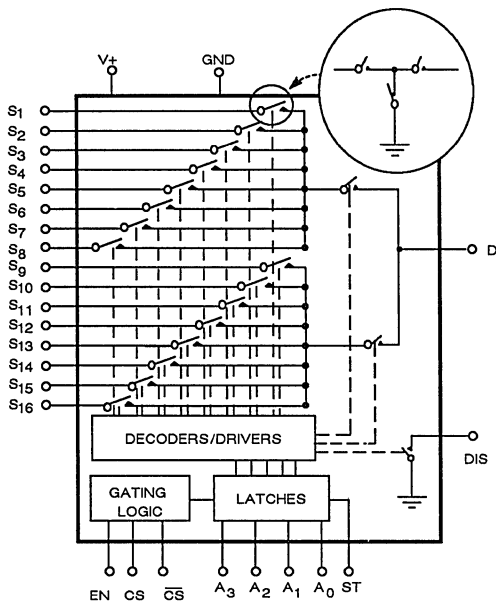
**PIN CONFIGURATION (Cont'd)**



Order Number:  
DG536AM/883

**FUNCTIONAL BLOCK DIAGRAM**

**TRUTH TABLE**



EN	CS	$\overline{CS}$	ST	A3	A2	A1	A0	Input Channel Selected	Disable Output
0	X	X							
X	0	X	1	X	X	X	X	NONE	HIGH Z
X	X	1							
					0	0	0	S1	LOW Z
					0	0	0	S2	
					0	0	1	S3	
					0	0	1	S4	
					0	1	0	S5	
					0	1	0	S6	
					0	1	1	S7	
					0	1	1	S8	
					1	0	0	S9	
					1	0	0	S10	
					1	0	1	S11	
					1	0	1	S12	
					1	1	0	S13	
					1	1	0	S14	
					1	1	1	S15	
					1	1	1	S16	
X	X	X	0	X	X	X	X	Maintains previous switch condition	HIGH Z or LOW Z

Logic " 1 " :  $V_{AH} \geq 10.5 V$

Logic " 0 " :  $V_{AL} \leq 4.5 V$

1. LOW Z, HIGH Z = Impedance of Disable Output to GND. Disable output is current sink when any channel is selected.
2. Strobe input (ST) is level triggered.

## ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... -0.3 V to +18 V	Storage Temperature (A Suffix) ..... -65 to 150°C (D Suffix) ..... -65 to 125°C
Digital Inputs ..... (GND - 0.3 V) to (V+ plus 2 V) ..... or 20 mA, whichever occurs first	Operating Temperature (A Suffix) ..... -55 to 125°C (D Suffix) ..... -40 to 85°C
V <sub>S</sub> ,V <sub>D</sub> ..... (GND - 0.3 V) to V+ plus 2 V) ..... or 20 mA, whichever occurs first	Power Dissipation (Package)* 44-Pin J Lead Ceramic** ..... 825 mW 44-Pin J Lead Plastic*** ..... 450 mW
Current (any terminal) Continuous ..... 20 mA	* All leads welded or soldered to PC board.
Current (S or D) Pulsed 1 ms 10% duty cycle .... 40 mA	** Derate 11 mW/°C above 75°C *** Derate 6 mW/°C above 75°C

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

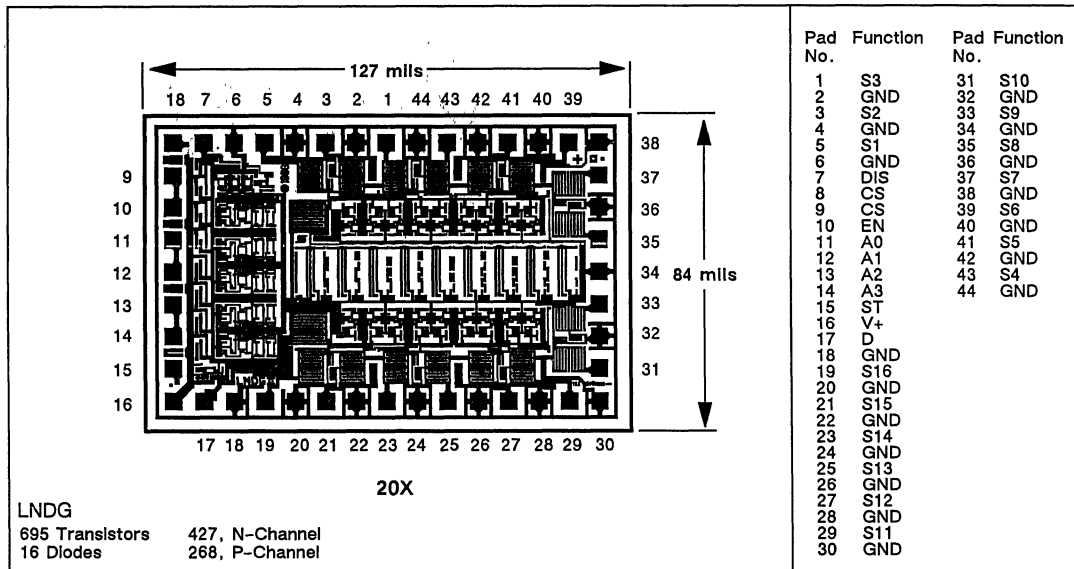
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V+ = 15 V, GND = 0 V ST, CS = 10.5 V CS = 4.5 V	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>		1		0	10	0	10	V
Drain - Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = 1 mA, V <sub>D</sub> = 3 V V <sub>AH</sub> = 4.5 V, V <sub>AL</sub> = 10.5 V Sequence Each Switch ON EN = 10.5 V	1,3 2	55		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta$ r <sub>DS(ON)</sub>		1			9		9	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 3 V, V <sub>D</sub> = 0 V EN = 4.5 V	1 2		-10 -100	10 100	-10 -100	10 100	nA
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = 0 V, V <sub>D</sub> = 3 V EN = 4.5 V	1 2		-10 -500	10 500	-10 -100	10 100	
Total Switch ON Leakage Current	I <sub>D(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 3 V EN = 10.5 V	1 2		-10 -1000	10 1000	-10 -100	10 100	
Disable Output	R <sub>DISABLE</sub>	I <sub>DISABLE</sub> = 1 mA EN = 10.5 V	1,3 2	100		200 250		200 250	Ω
<b>INPUT</b>									
Input Voltage High	V <sub>AIH</sub>		1,2,3		10.5		10.5		V
Input Voltage Low	V <sub>AiL</sub>		1,2,3			4.5		4.5	
Address Input Current	I <sub>Ai</sub>	V <sub>A</sub> = GND or V+	1 2	<0.01	-10 -100	10 100	-10 -100	10 100	μA
<b>DYNAMIC</b>									
ON State Input Cap. <sup>c</sup>	C <sub>S(ON)</sub>	V <sub>D</sub> = V <sub>S</sub> = 3 V	1	32		45		45	pF
OFF State Input Cap. <sup>c</sup>	C <sub>S(OFF)</sub>	V <sub>S</sub> = 3 V	1	2		4		4	
OFF State Output Cap. <sup>c</sup>	C <sub>D(OFF)</sub>	V <sub>D</sub> = 3 V	1	8		12		12	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>+</sub> = 15 V, GND = 0 V ST, CS = 10.5 V CS̄ = 4.5 V	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
Multiplexer Switching Time	t <sub>TRANS</sub>	See Figure 4	1 2,3			300 300		300	ns
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 4	1 2,3		25 25		25		
EN, CS, CS̄, ST Turn ON Time	t <sub>ON</sub>	See Figures 2 & 3	1 2,3			300 300		300	
EN, CS, CS̄ Turn OFF Time	t <sub>OFF</sub>	See Figure 2	1 2,3			150 150		150	
Charge Injection	Q	See Figure 5	1	-35					pC
Single-Channel Crosstalk	XTALK <sub>(SC)</sub>	R <sub>IN</sub> = 75 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz See Figure 9	1	-100					dB
Chip Disabled Crosstalk (See Figure 8)	XTALK <sub>(CD)</sub>	R <sub>IN</sub> = R <sub>L</sub> = 75 Ω, f = 5 MHz EN = 4.5 V	1	-85					
Adjacent Input Crosstalk (See Figure 10)	XTALK <sub>(AI)</sub>	R <sub>IN</sub> = 10 Ω, R <sub>L</sub> = 10 kΩ f = 5 MHz	1	-92					
All Hostile Crosstalk <sup>c</sup> (See Figure 7)	XTALK <sub>(AH)</sub>		1	-74	-60		-60		
Bandwidth	BW	R <sub>L</sub> = 50 Ω, See Figure 6	1	300					MHz
<b>SUPPLY</b>									
Supply Current	I <sub>+</sub>	Any One Channel Selected With Address Inputs at GND or V <sub>+</sub>	1,3 2	5		50 100		50 100	μA
Voltage Current	V <sub>+</sub>		1,2,3		10	16.5	10	16.5	V
<b>MINIMUM INPUT TIMING REQUIREMENTS</b>									
Strobe Pulse Width	t <sub>SW</sub>	See Figure 1	1,2,3		200		200		ns
A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> , CS, CS̄, EN Data Valid To Strobe	t <sub>DW</sub>	See Figure 1	1,2,3		100		100		
A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> , CS, CS̄, EN Data Valid After Strobe	t <sub>WD</sub>	See Figure 1	1,2,3		50		50		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Analog signal range is measured from the GND pin to the designated Source (input) pin.

## DIE TOPOGRAPHY



## INPUT TIMING REQUIREMENTS

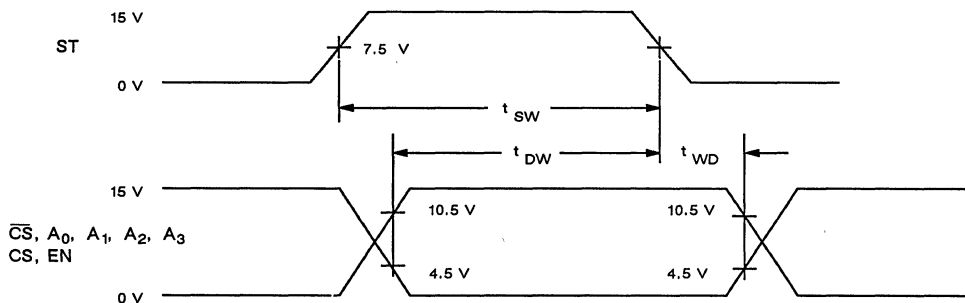


Figure 1

**EN, CS,  $\overline{CS}$ , TURN ON/OFF TIME TEST CIRCUIT**

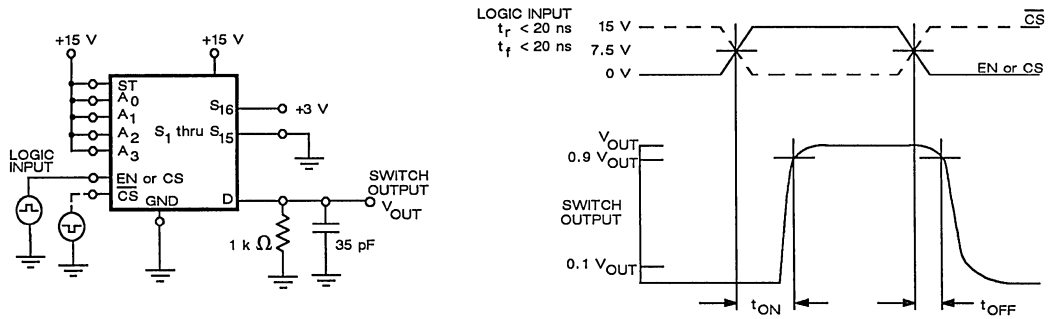


Figure 2

**STROBE (ST) TURN ON TIME TEST CIRCUIT**

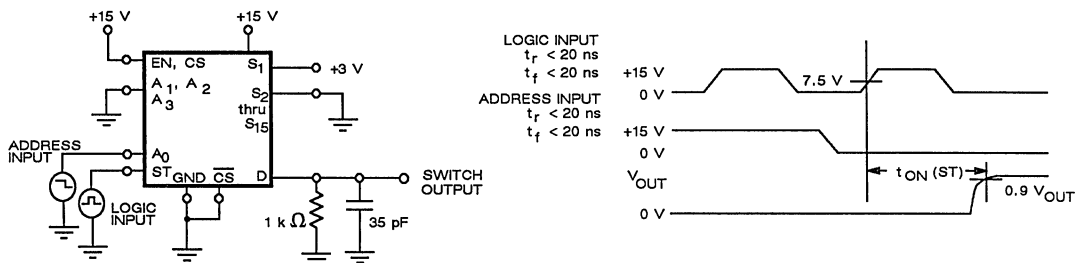


Figure 3

7

**TRANSITION TIME and BREAK-BEFORE-MAKE INTERVAL TEST CIRCUIT**

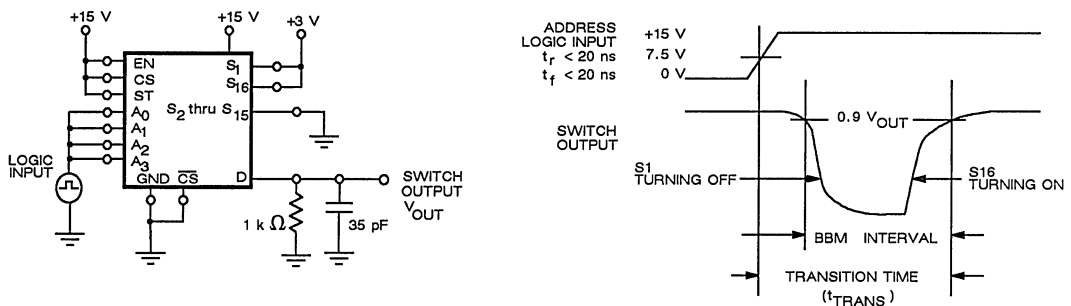


Figure 4

## CHARGE INJECTION TEST CIRCUIT

## BANDWIDTH TEST CIRCUIT

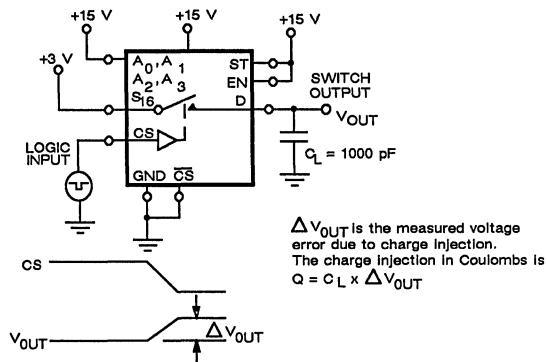


Figure 5

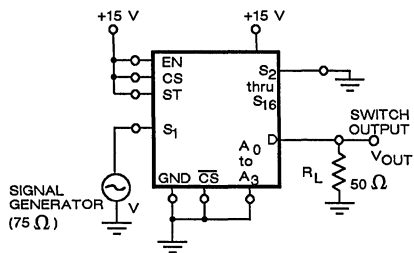


Figure 6

## ALL HOSTILE CROSSTALK - X TALK (AH)

## CHIP DISABLED CROSSTALK - X TALK (CD)

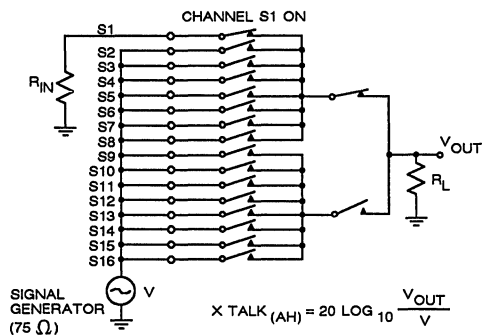


Figure 7

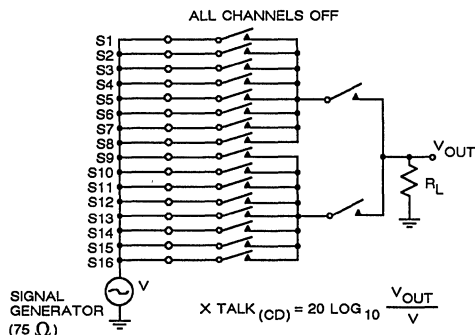
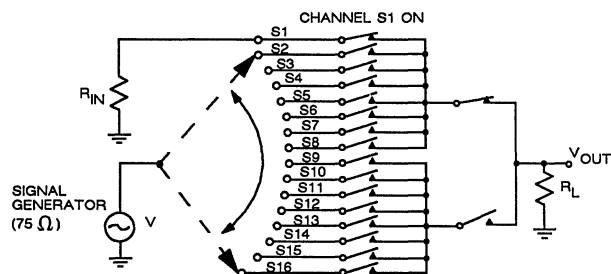


Figure 8

## SINGLE CHANNEL CROSSTALK - X TALK (SC)

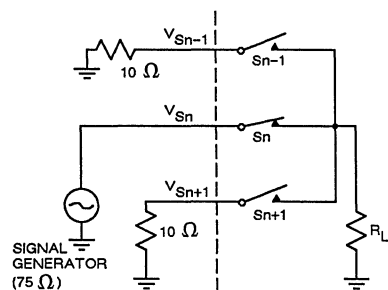
## ADJACENT INPUT CROSSTALK - X TALK (AI)



**NOTES:**

- Any individual channel between S2 and S16 can be selected
- $X \text{ TALK}_{(SC)} = \text{Average value of } 20 \text{ LOG}_{10} \frac{V_{OUT}}{V}$  is scanned sequentially from S2 to S16

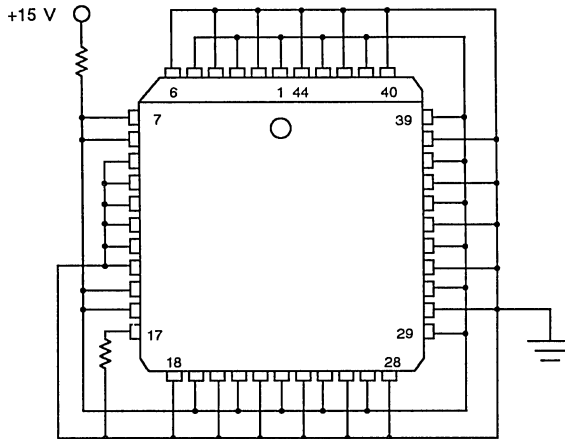
Figure 9



$$X \text{ TALK}_{(AI)} = 20 \text{ LOG}_{10} \frac{V_{Sn-1}}{V_{Sn}} \text{ or } 20 \text{ LOG}_{10} \frac{V_{Sn+1}}{V_{Sn}}$$

Figure 10

**BURN-IN CIRCUIT**

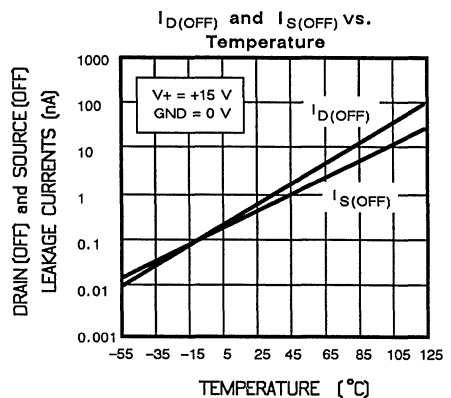
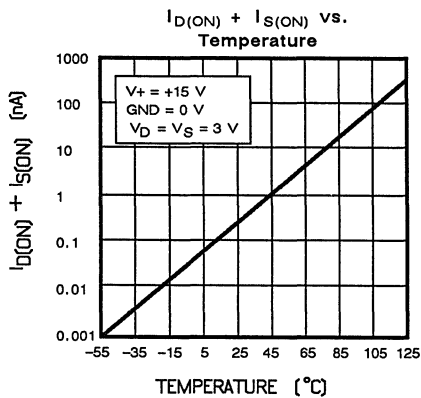
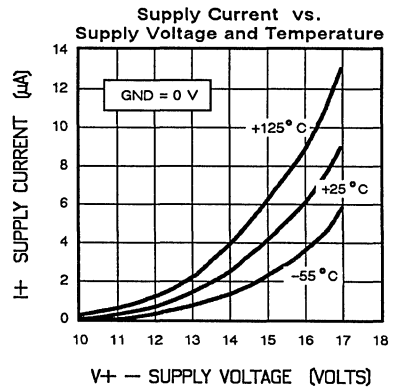
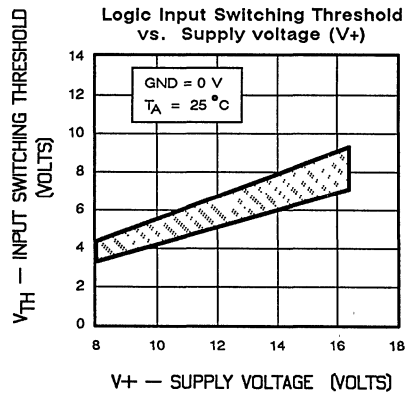
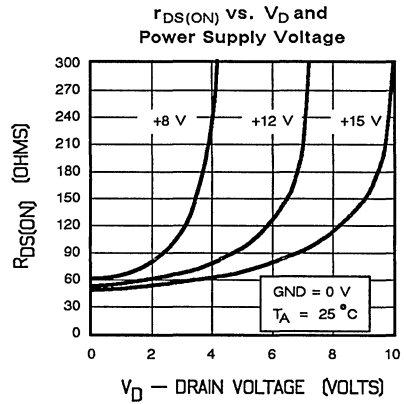
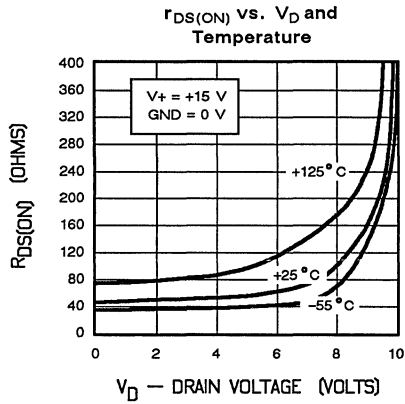


Note: All Resistors are 10 kΩ unless otherwise specified

**PIN DESCRIPTION**

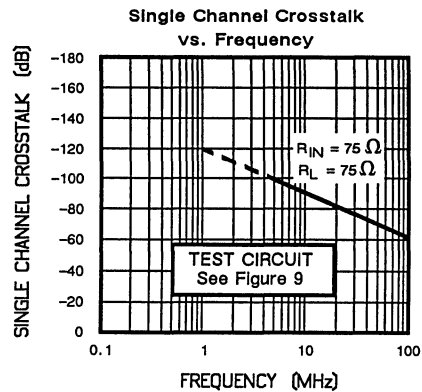
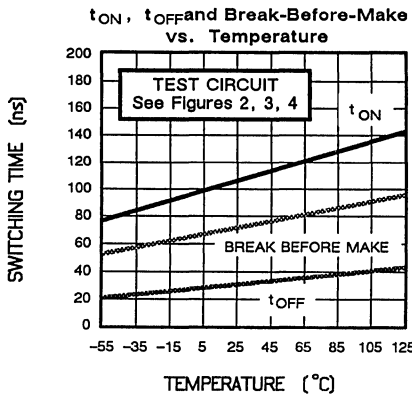
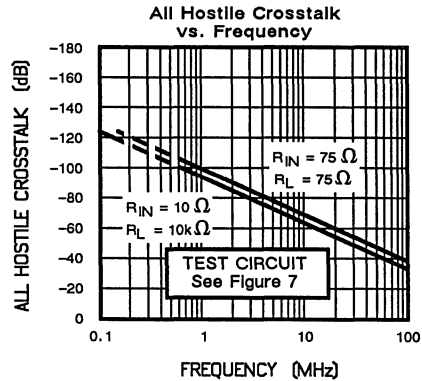
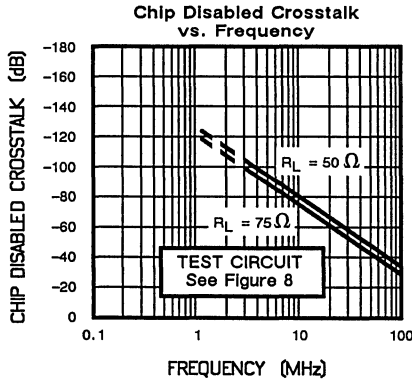
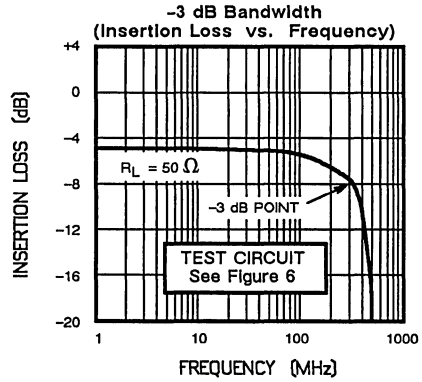
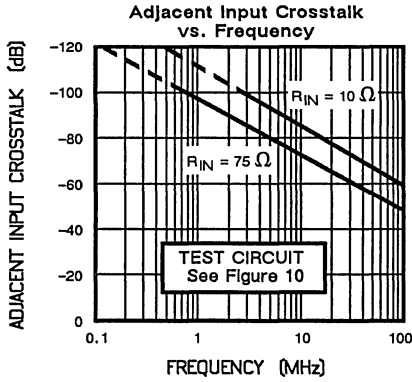
PIN NUMBER	SYMBOL	DESCRIPTION
1	S3	Channel 3 Analog Input
3	S2	Channel 2 Analog Input
5	S1	Channel 1 Analog Input
7	DIS	Open drain impedance output when the DG536 is disabled (all channels OFF). When the DG536 is enabled (any channel selected) this output is current sink to Analog GND.
8,9,10	$\overline{CS}$ , CS, EN	Logic Inputs to select required Multiplexer(s) when using several Multiplexers in a system.
11 - 14	A <sub>0</sub> - A <sub>3</sub>	Four binary address inputs that determine which one of the sixteen channels is selected.
15	ST	Strobe input that latches A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , A <sub>3</sub> , $\overline{CS}$ , CS, EN
16	V+	Positive supply voltage
17	D	Analog output of Multiplexer or Analog input if device used in Demultiplexer configuration.
19	S16	Channel 16 Analog Input
21	S15	Channel 15 Analog Input
23	S14	Channel 14 Analog input
25	S13	Channel 13 Analog Input
27	S12	Channel 12 Analog input
29	S11	Channel 11 Analog input
31	S10	Channel 10 Analog input
33	S9	Channel 9 Analog Input
35	S8	Channel 8 Analog Input
37	S7	Channel 7 Analog Input
39	S6	Channel 6 Analog Input
41	S5	Channel 5 Analog Input
43	S4	Channel 4 Analog Input
2,4,6,18,20, 22,24,26,28, 30,32,34,36, 38,40,42,44	GND	Analog signal ground and most negative potential. All pins should be connected externally to ensure dynamic performance.

## TYPICAL CHARACTERISTICS





TYPICAL CHARACTERISTICS (Cont'd)



## DETAILED DESCRIPTION

The DG536 is a 16-channel single-ended multiplexer with on-chip address logic and control latches.

The circuit connects one of sixteen inputs (S1, S2,...S16) to a common output (D) under the control of a 4 bit binary address (A<sub>0</sub> to A<sub>3</sub>). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of 3 independent logic inputs (EN, CS and  $\overline{CS}$ ) are provided on chip. These inputs are gated together (see Figure 11) and only when EN = CS = 1 and  $\overline{CS}$  = 0 is true can an output switch be selected by the appropriate address input (A<sub>0</sub> to A<sub>3</sub>). This necessary logic condition can then be latched by Strobe (ST) going low.

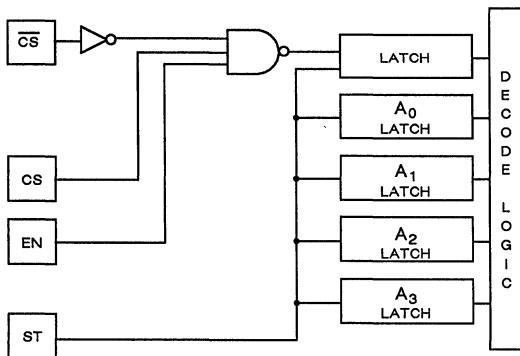


Figure 11.  $\overline{CS}$ , CS, EN, ST Control Logic

Break-before-make switching is included to prevent momentary shorting of an input channel when changing from one input to another.

The device features a two-level switch arrangement whereby two banks of eight switches (first level) are

connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure 12).

With this method SW2 operates out of phase with SW1 and SW3. In the ON condition SW1 and SW3 are closed with SW2 open where as in the OFF condition SW1 and SW3 are open and SW2 closed. In the OFF condition the input to SW3 is effectively the isolation leakage of SW1 working into the ON resistance of SW2 (typically 200  $\Omega$ ).

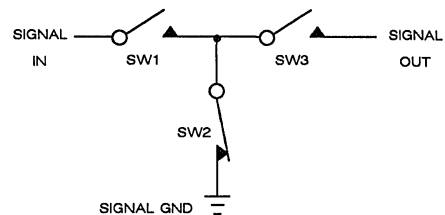


Figure 12. "T" Switch Arrangement

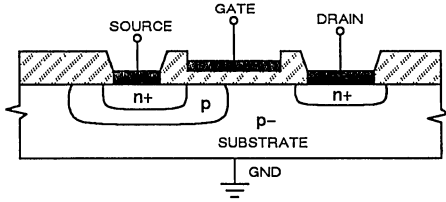
The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output (Pin 7) can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG536 has extensive applications where any high frequency video, audio or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using N channel DMOS FETs for the "T" and series switches.

A cross section of a switch is shown in Figure 13.

**DETAILED DESCRIPTION (Cont'd)**



**Figure 13.** Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure 13 that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e. 20 mA).

Since no PN junctions exist between the signal path and V+, positive overvoltages are not a problem, unless the breakdown voltage of the DMOS source terminal (see Figure 13) (+18 V) is exceeded. Positive overvoltage conditions must not exceed +18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown occurring.

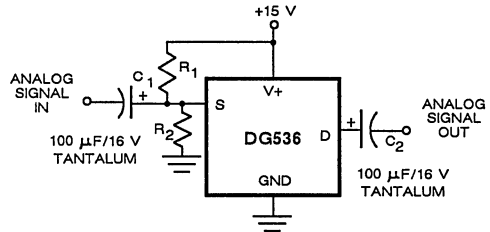
The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device

**DC BIASING**

To avoid negative overvoltage conditions and subsequent distortion of ac analog signals, dc biasing is necessary. Biasing is not required,

however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to  $\pm 200$  mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure 14.



**Figure 14.** Simple Bias Circuit

R1 and R2 are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase performance. Capacitor C1 blocks the DC bias voltage from being coupled back to the analog signal source and C2 blocks the DC bias from the output signal. Both C1 and C2 should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies.

Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method would be to offset the supply voltages (see Figure 15).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.

## DETAILED DESCRIPTION (Cont'd)

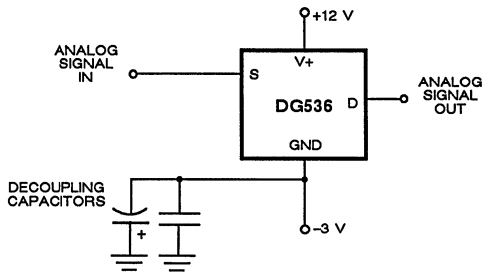


Figure 15. DG536 With Offset Supply

TTL to CMOS level shifting is easily obtained by using a MC14504B.

### CIRCUIT LAYOUT

Good circuit board layout and extensive shielding is essential for optimizing the high frequency performance of the DG536. Stray capacitances on the PC board and/or connecting leads will considerably degrade the ac performance. Hence, signal paths must be kept as short as practically possible, with extensive ground planes separating signal tracks.

# 8-Channel/Dual 4-Channel Wideband/Video Multiplexer

## FEATURES

- Wide Bandwidth (500 MHz)
- Very Low Crosstalk (-97 dB @ 5 MHz)
- On-Board TTL-compatible Latches with Readback
- Optional Negative Supply Input
- Low  $r_{DS(ON)}$  (90  $\Omega$  max)
- Single-ended 8-channel or Dual 4-channel operation
- ESDS Protection >  $\pm 4000$  V

## BENEFITS

- Improved System Bandwidth
- Improved Channel Off-isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

## APPLICATIONS

- Wideband Signal Routing and Multiplexing
- High-end Video Systems
- $\mu$ P-controlled Systems
- Direct Coupled Systems
- ATE Systems

## DESCRIPTION

The DG538 is an electrically-selectable 8-channel or dual 4-channel analog multiplexer designed for wideband operation. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low ON resistance and low capacitance of the DG538 makes it ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without DC biasing.

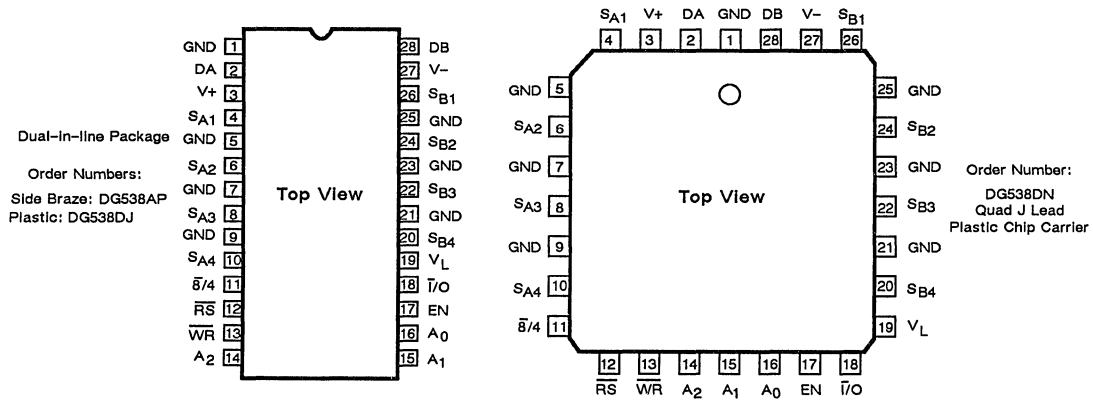
The DG538 is built on a D/CMOS process that combines n-channel DMOS switching FETs with

low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of OFF isolation. Crosstalk is reduced to -97 dB at 5 MHz on the DG538 by including a ground line between each adjacent signal path.

The DG538 is available in 28-pin plastic DIP and PLCC packages for operation over the industrial, D suffix (-40 to 85°C) temperature range. The 28-lead side braze DIP is available for military, A suffix (-55 to 125°C) temperature range operation.

**7**

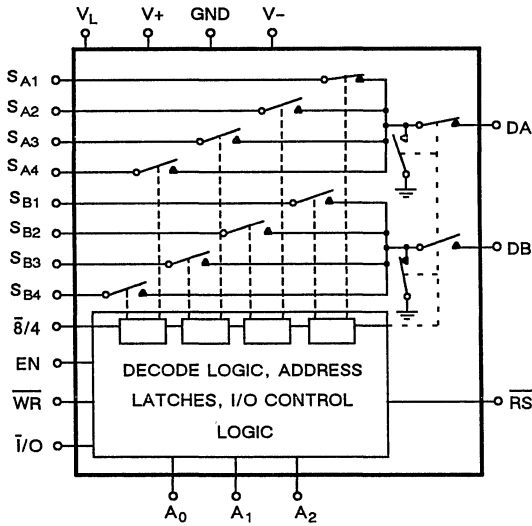
## PIN CONFIGURATION



## FUNCTIONAL BLOCK DIAGRAM

## TRUTH TABLE

All eight input switches are "T" switches.



$\bar{I}/O$	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	$\bar{8}/4$	ON SWITCH
X	X	X	X	X	1	1	1	Maintains previous state
X	X	X	X	X	X	0	X	None (latches cleared)
X	X	X	X	0	0	1	X	None
0	0	0	0	1	0	1	0	SA1
0	0	0	1	1	0	1	0	SA2
0	0	1	0	1	0	1	0	SA3
0	0	1	1	1	0	1	0	SA4
0	1	0	0	1	0	1	0	SB1
0	1	0	1	1	0	1	0	SB2
0	1	1	0	1	0	1	0	SB3
0	1	1	1	1	0	1	0	SB4
0	X	0	0	1	0	1	1	SA1 & SB1
0	X	0	1	1	0	1	1	SA2 & SB2
0	X	1	0	1	0	1	1	SA3 & SB3
0	X	1	1	1	0	1	1	SA4 & SB4
1	NOTE 2, 3				1	1	1	Note 1

Logic "1" :  $V_{AH} \geq 2.0 V$

Logic "0" :  $V_{AL} \leq 0.8 V$

- $\bar{8}/4$  can be either H or L but should not change during these operations.
- In this condition the pins A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> become outputs and reflect the contents of the latches. Please see timing waveforms for more detail.
- EN must be latched HIGH to allow proper address data readback operation.

## ABSOLUTE MAXIMUM RATINGS

V <sub>+</sub> to GND	.....	-0.3 V to +22 V
V <sub>+</sub> to V <sub>-</sub>	.....	-0.3 V to +22 V
V <sub>-</sub> to GND	.....	-10 V to +0.3 V
Digital Inputs	..... (V <sub>-</sub> minus 0.3 V) to (V <sub>+</sub> plus 0.3 V) or 20 mA, whichever occurs first	
V <sub>S</sub> , V <sub>D</sub>	..... (V <sub>-</sub> minus 0.3 V) to (V <sub>-</sub> plus 14 V) or 20 mA, whichever occurs first	
CURRENT (any terminal) Continuous	.....	20 mA
CURRENT (S or D) Pulsed 1 ms 10% duty	.....	40 mA
Storage Temperature (A Suffix)	.....	-65 to 150°C
(D Suffix)	.....	-65 to 125°C
Operating Temperature (A Suffix)	.....	-55 to 125°C
(D Suffix)	.....	-40 to 85°C

### Power Dissipation (Package)\*

28-pin Plastic DIP**	.....	625 mW
28-pin Side Braze DIP***	.....	1200 mW
28-pin Quad J Lead Plastic****	.....	450 mW

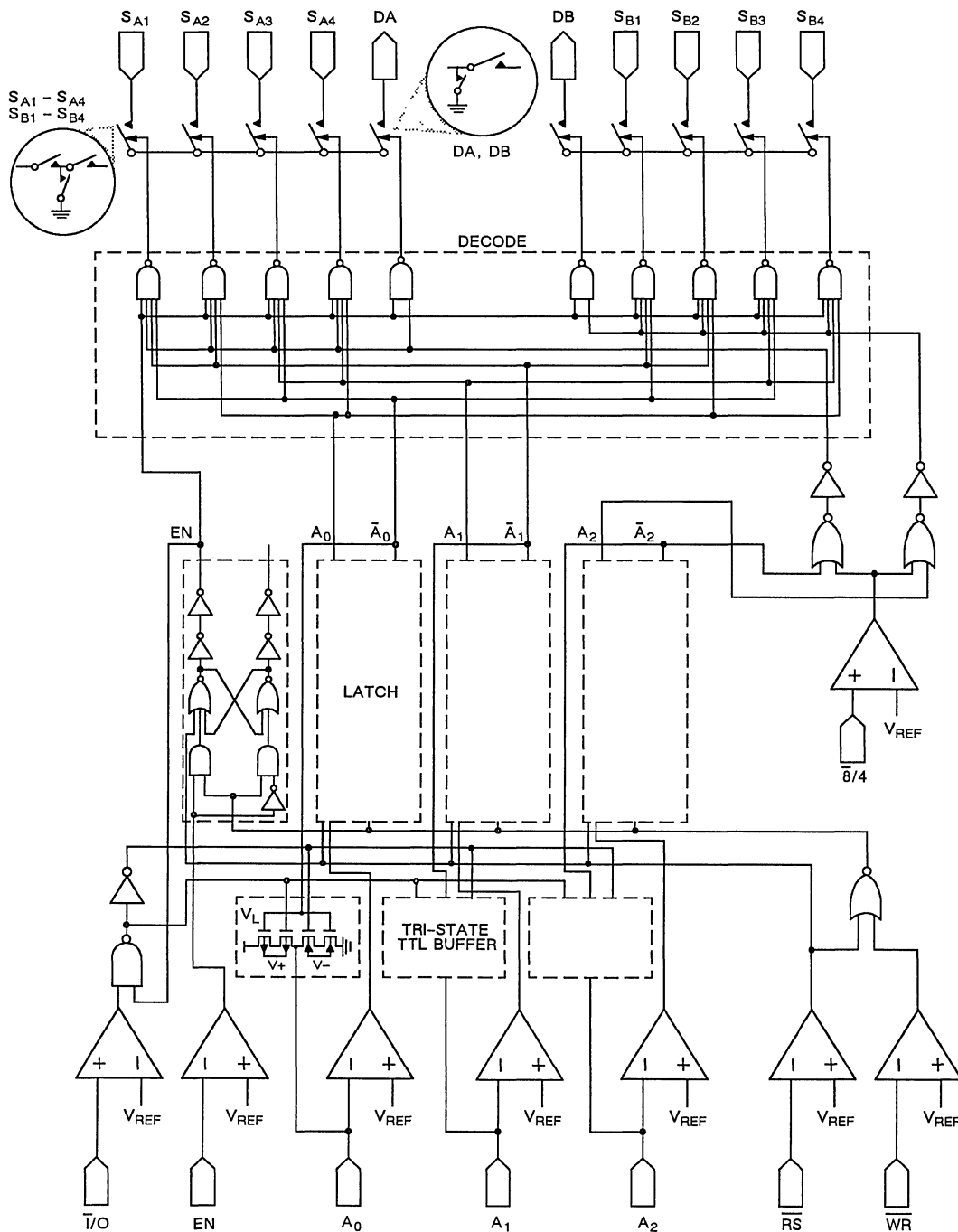
\* All leads welded or soldered to PC board.

\*\* Derate 8.3 mW/°C above 75°C

\*\*\* Derate 16 mW/°C above 75°C

\*\*\*\* Derate 6 mW/°C above 75°C

**CONTROL CIRCUITRY**



Note:  $V_{REF}$  is Internally generated from  $V_L$

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V V <sub>L</sub> = +5 V, GND = 0 V $\overline{WR}$ = 0.8 V RS, EN = 2 V	LIMITS						UNIT	
			1=25°C		2=125,85°C		3=-55,-40°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>SWITCH</b>										
Analog Signal Range <sup>e</sup>	V <sub>ANALOG</sub>	V <sub>-</sub> = -5 V	1		-5	8	-5	8	V	
Drain - Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>S</sub> = 0 V V <sub>AIL</sub> = 0.8 V, V <sub>AIH</sub> = 2 V Sequence each switch ON	1,3 2	45		90 120		90 120	Ω	
Resistance Match Between Channels	Δ r <sub>DS(ON)</sub>		1			9		9		
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 8 V, V <sub>D</sub> = 0 V EN = 0.8 V	1,3 2		-5 -50	5 50	-5 -50	5 50	nA	
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = 0 V, V <sub>D</sub> = 8 V EN = 0.8 V	1,3 2		-20 -500	20 500	-20 -500	20 500		
Total Switch ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 8 V	1,3 2		-10 -1000	10 1000	-10 -100	10 100		
<b>INPUT</b>										
Address Output Current	I <sub>AO</sub>	V <sub>AO</sub> = 2.7 V	1,2,3		-400		-400		μA	
		V <sub>AO</sub> = 0.4 V	1,2,3			400		400		
Input Voltage High	V <sub>AIH</sub>	See Figure 13 Note 1	1,2,3		2		2		V	
Input Voltage Low	V <sub>AIL</sub>		1,2,3			0.8		0.8		
Address Input Current	I <sub>AI</sub>	V <sub>AI</sub> = 0 V or 2 V or 15 V	1,3 2	0.1	-1 -10	1 10	-1 -10	1 10	μA	
<b>DYNAMIC</b>										
ON State Input Cap. <sup>c</sup>	C <sub>S(ON)</sub>	See Figure 11	PLCC DIP	1 1	23 27		35		30 35	pF
OFF State Input Cap. <sup>c</sup>	C <sub>S(OFF)</sub>	See Figure 12	PLCC DIP	1 1	2 3		5		4 5	
OFF State Output Cap. <sup>c</sup>	C <sub>D(OFF)</sub>	See Figure 12	PLCC DIP	1 1	4 6		10		8 10	
Multiplexer Switching Time	t <sub>TRANS</sub>	See Figure 4		1,3 2			300 500		300 500	ns
Break-Before-Make Interval	t <sub>OPEN</sub>	See Figure 4		1,2,3		50		50		
EN, $\overline{WR}$ Turn on Time	t <sub>ON</sub>	See Figures 2 & 3		1,3 2			300 500		300 500	
EN, Turn OFF Time	t <sub>OFF</sub>	See Figure 2		1,3 2			150 300		150 300	



ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V V <sub>L</sub> = +5 V, GND = 0 V WR = 0.8 V RS, EN = 2 V		LIMITS						UNIT
				1=25°C		DG538AP		DG538DN		
				TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>										
Charge Injection	Q	See Figure 5		1	-70					pC
Chip Disabled Crosstalk (See Figure 8)	XTALK (CD)	R <sub>L</sub> = 75 Ω f = 5 MHz EN = 0.8 V	PLCC DIP	1 1	-75 -65					dB
Adjacent Input Crosstalk (See Figure 9)	XTALK (AI)	R <sub>IN</sub> = 10 Ω R <sub>L</sub> = 10 k Ω f = 5 MHz	PLCC DIP	1 1	-97 -87					
		R <sub>IN</sub> = 75 Ω R <sub>L</sub> = 75 Ω f = 5 MHz	PLCC DIP	1 1	-80 -70					
All Hostile Crosstalk (See Figure 7)	XTALK (AH)	R <sub>IN</sub> = 10 Ω R <sub>L</sub> = 10 k Ω f = 5 MHz	PLCC DIP	1 1	-77 -72					
		R <sub>IN</sub> = 75 Ω R <sub>L</sub> = 75 Ω f = 5 MHz	PLCC DIP	1 1	-77 -72					
Differential Crosstalk (See Figure 10)	XTALK (DIFF)	R <sub>IN</sub> = 10 Ω R <sub>L</sub> = 10 k Ω f = 5 MHz	PLCC DIP	1 1	-84 -84					
		R <sub>IN</sub> = 75 Ω R <sub>L</sub> = 75 Ω f = 5 MHz	PLCC DIP	1 1	-84 -84					
Bandwidth	BW	R <sub>L</sub> = 50 Ω, See Figure 6		1	500					MHz
<b>SUPPLY</b>										
Positive Supply Current	I <sub>+</sub>	Any One Channel Selected With Address Inputs at GND or V <sub>+</sub>		1,2 3	0.6		2 5		2 5	mA
Negative Supply Current	I <sub>-</sub>			1,2 3	0.6	-1.8 -2.0		-1.8 -2.0		
Operating Supply Voltage Range	V <sub>+</sub> to V <sub>-</sub>	See Figure 13 Functional Test Only		1,2,3		10	21	10	21	V
	V <sub>-</sub> to GND			1,2,3		-5.5	0	-5.5	0	
	V <sub>+</sub> to GND			1,2,3		10	21	10	21	
Logic Supply Current	I <sub>L</sub>			1,2,3	150		500		500	μA
<b>TIMING</b>										
Reset to Write	t <sub>RW</sub>	See Figure 1		1,2,3		50		50		ns
WR, RS Minimum pulse Width	t <sub>MPW</sub>	See Figure 1		1,2,3		200		200		
A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , EN Data Valid To Strobe	t <sub>DW</sub>	See Figure 1		1,2,3		100		100		

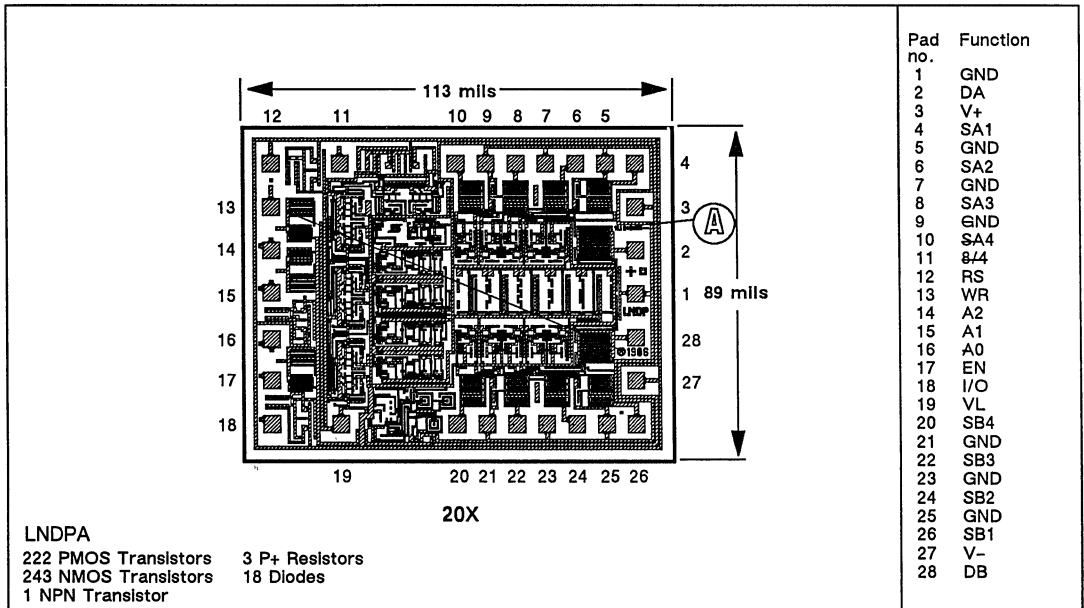
7

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V V <sub>L</sub> = +5 V, GND = 0 V WR = 0.8 V RS, EN = 2 V	LIMITS						UNIT
			1=25°C		2=125, 85°C		3=-55, -40°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
TIMING (Cont'd)									
A <sub>0</sub> , A <sub>1</sub> , A <sub>2</sub> , EN Data Valid After Strobe	t <sub>WD</sub>	See Figure 1	1,2,3		50		50		ns
Address Bus Tristate	t <sub>AZ</sub>	See Figure 1	1	50					
Address Bus Output	t <sub>AO</sub>	See Figure 1	1		200		200		
Address Bus Input	t <sub>AI</sub>	See Figure 1	1		200		200		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY at 25°C, not guaranteed nor subject to production testing.
- e. Analog signal range is measured from the GND pin to the designated Source (input) pin, and indicates the limits of functionality. Performance limits are only guaranteed for stated test conditions.

**DIE TOPOGRAPHY**



**INPUT TIMING REQUIREMENTS**

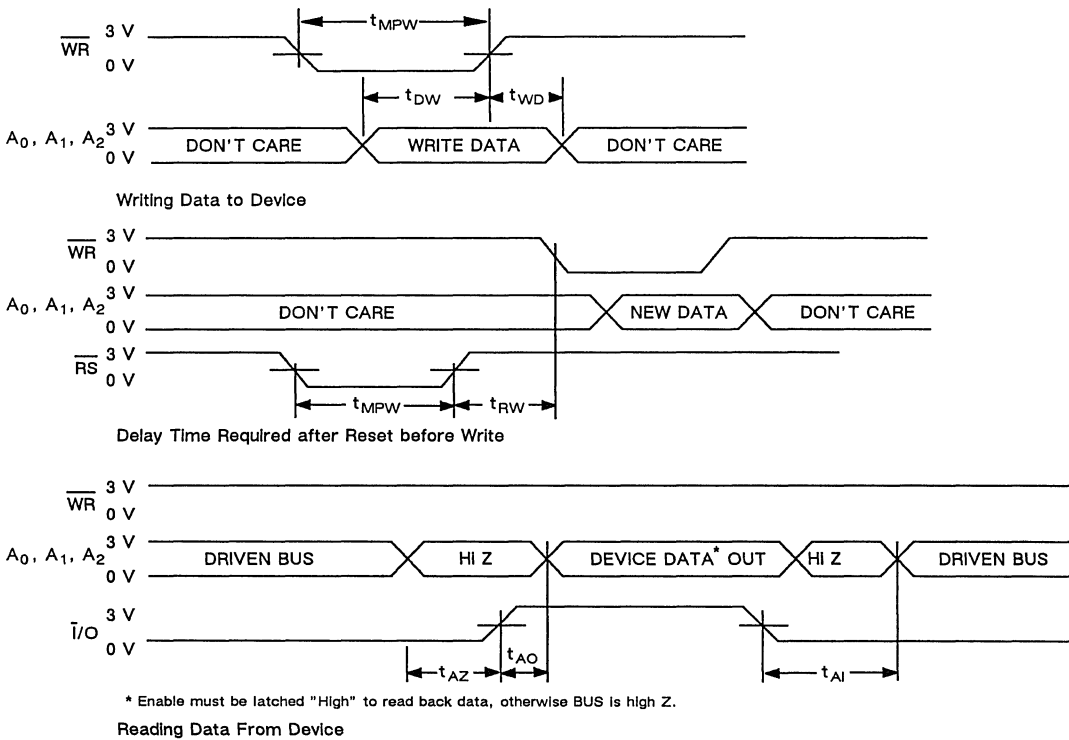


Figure 1

**EN TURN ON/OFF TIME TEST CIRCUIT**

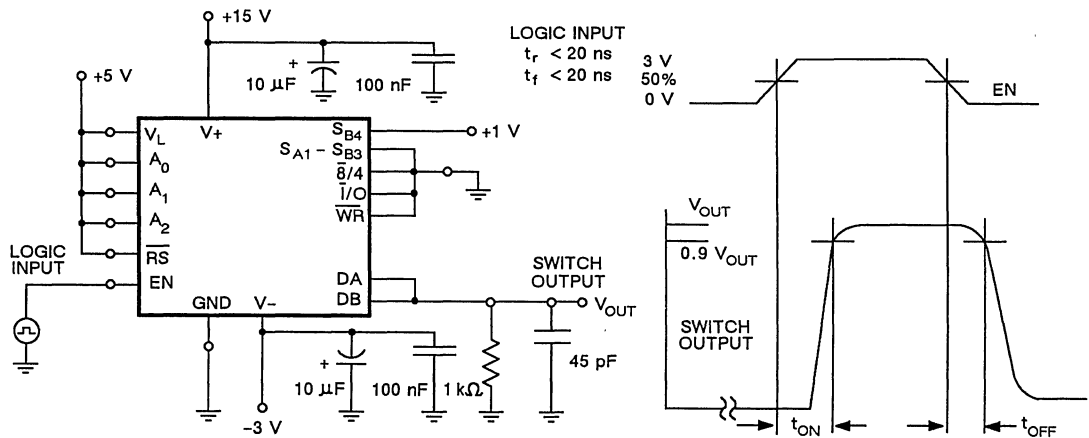


Figure 2

## WR TURN ON TIME TEST CIRCUIT

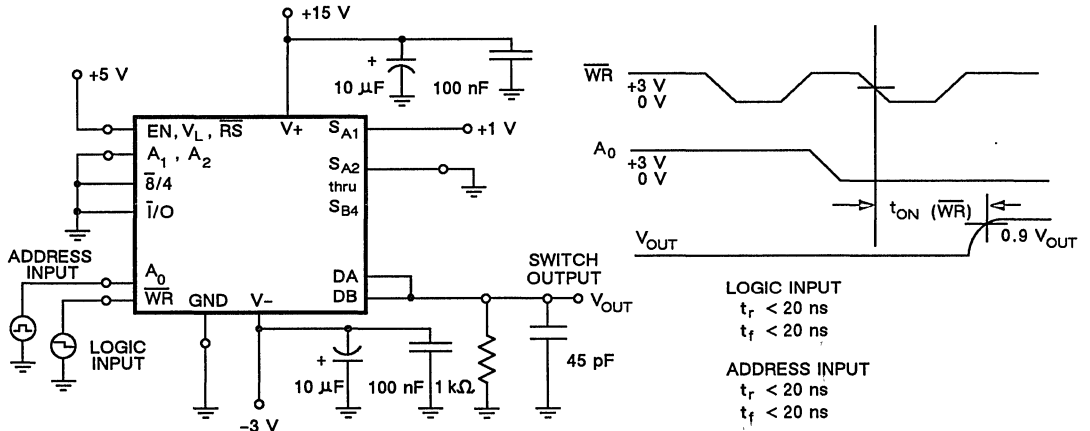


Figure 3

## TRANSITION TIME and BREAK-BEFORE-MAKE INTERVAL TEST CIRCUIT

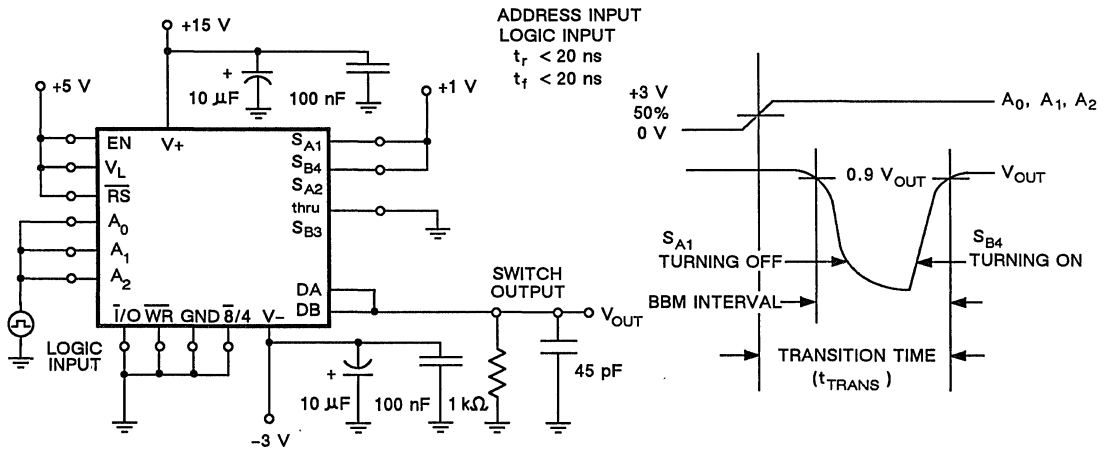
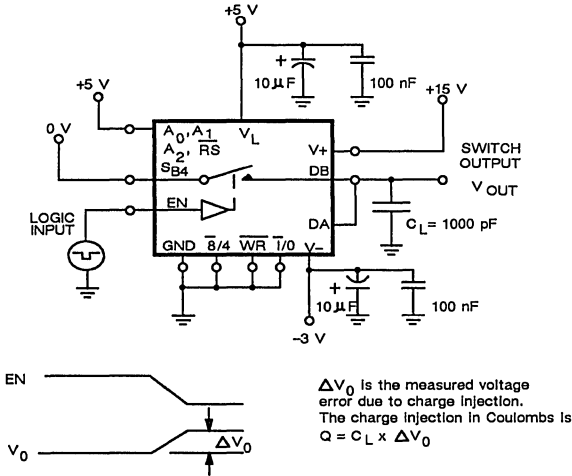


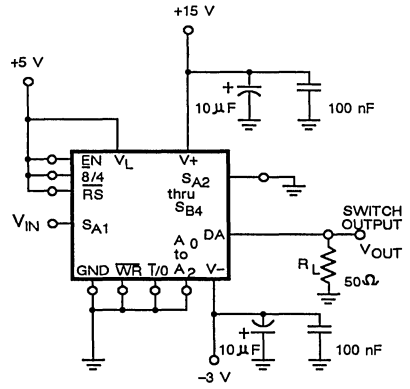
Figure 4

**CHARGE INJECTION TEST CIRCUIT**

**-3 dB BANDWIDTH TEST CIRCUIT**



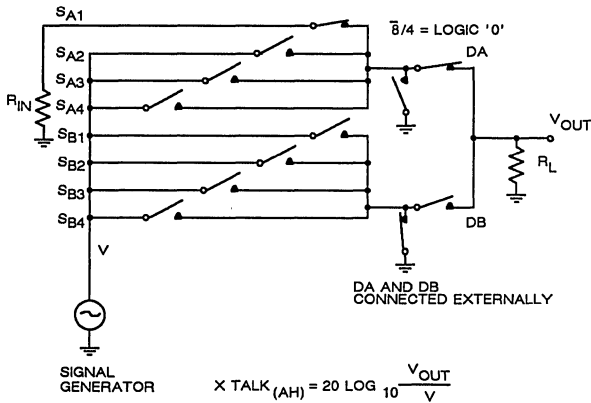
**Figure 5**



**Figure 6**

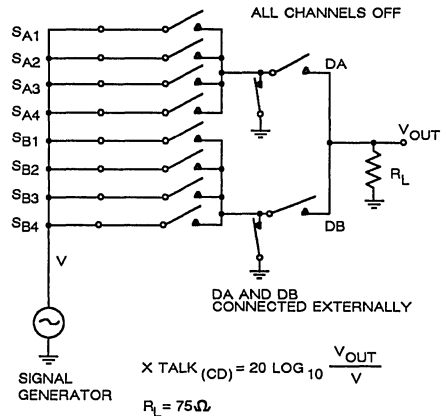
**ALL HOSTILE CROSSTALK - X TALK (AH)**

**CHIP DISABLED CROSSTALK - X TALK (CD)**



Note: SA1 on or any other one channel on.

**Figure 7**



**Figure 8**

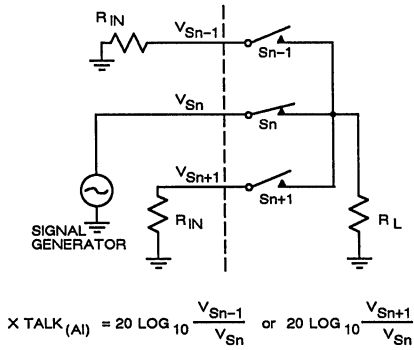


Figure 9

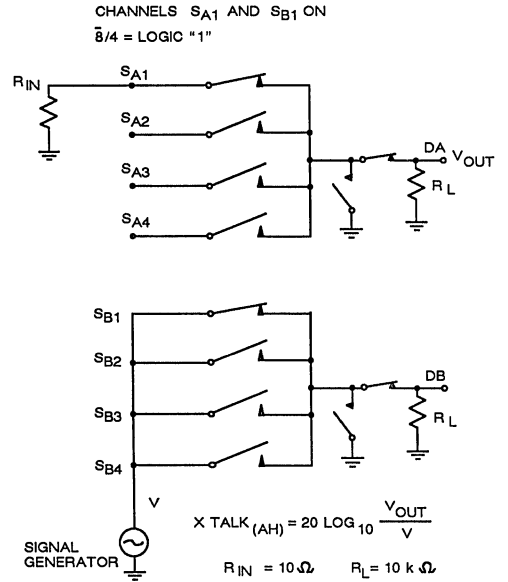


Figure 10

### ON STATE INPUT CAPACITANCE

### OFF STATE INPUT/OUTPUT CAPACITANCE

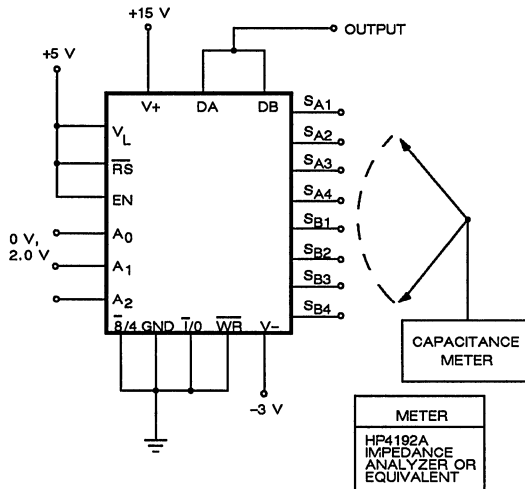


Figure 11

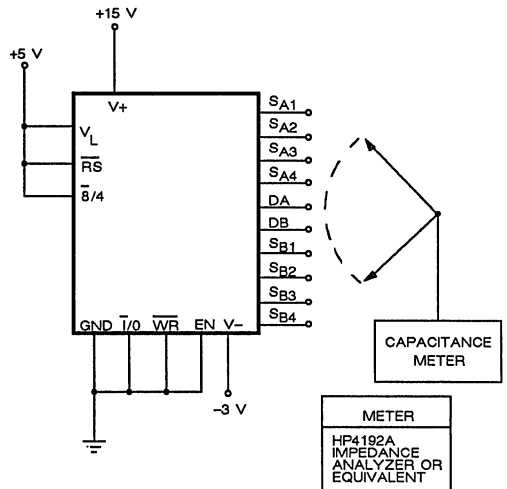
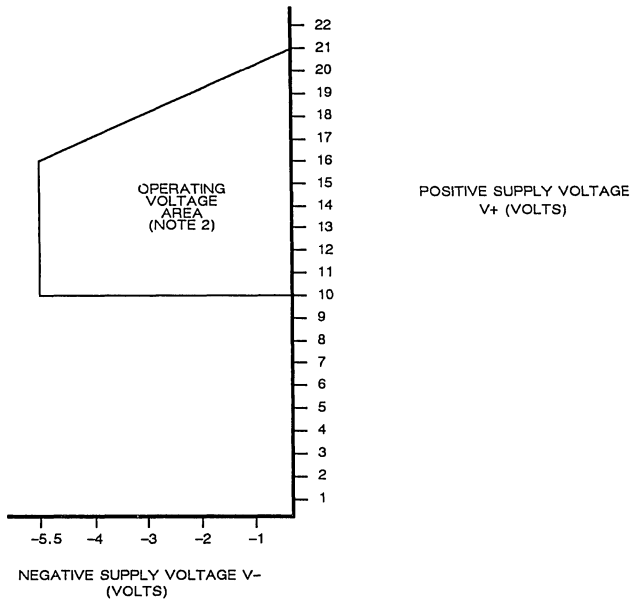


Figure 12

**OPERATING VOLTAGE RANGE**

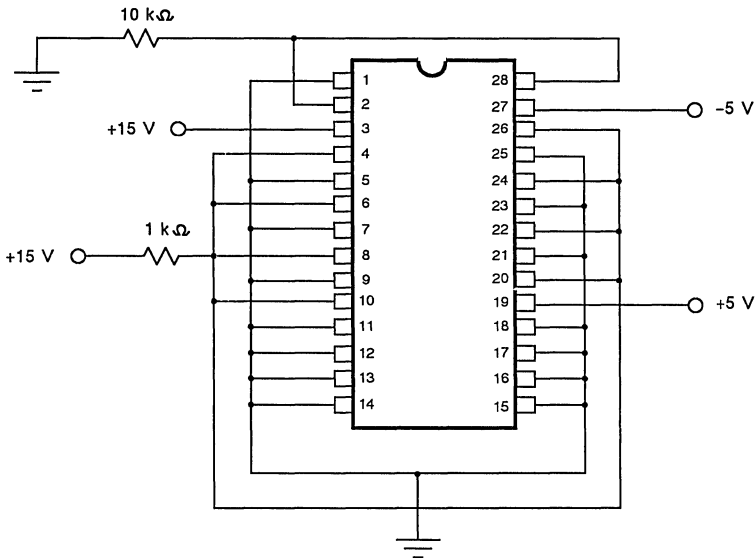


**Note:**

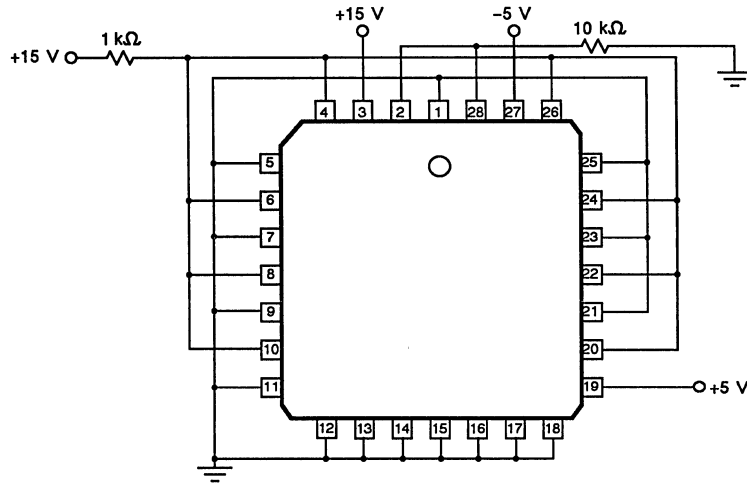
1. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins.  
Typical decoupling capacitors would be 10µF tantalum bead in parallel with 100 nF ceramic disc.
2. Production tested with V+ = 15 V and V- = -3.0 V
3. At V<sub>L</sub> = 5 V ± 10%, 0.8/2.0 V TTL compatibility is maintained over the entire operating voltage range.

**Figure 13**

**BURN-IN CIRCUIT – 28-LEAD DUAL-IN-LINE**



## BURN-IN CIRCUIT - 28-LEAD PLCC



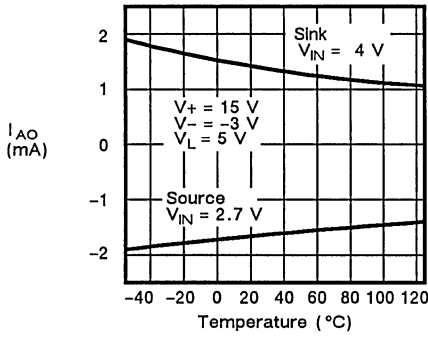
### PIN DESCRIPTION

PIN NUMBER	SYMBOL	DESCRIPTION
2	DA	Analog output
3	V+	Positive supply voltage (must be decoupled)
11	$\bar{S}/4$	8 by 1 or 4 by 2 select
12	$\bar{RS}$	Reset
13	$\bar{WR}$	Write command that latches $A_0, A_1, A_2, EN$
14	$A_2$	Binary address inputs that determine which input channel(s) is connected to the output(s)
15	$A_1$	
16	$A_0$	
17	EN	Input to activate multiplexer
18	$\bar{I/O}$	Pin to read from or write to the address latches
19	$V_L$	Logic supply voltage
27	V-	Negative supply voltage (must be decoupled)
28	DB	Analog output
4	$S_{A1}$	Analog input
6	$S_{A2}$	Analog input
8	$S_{A3}$	Analog input
10	$S_{A4}$	Analog input
20	$S_{B4}$	Analog input
22	$S_{B3}$	Analog input
24	$S_{B2}$	Analog input
26	$S_{B1}$	Analog input
1, 5, 7, 9	GND	Analog and digital ground.
21, 23, 25		All GND pins should be connected externally to optimize dynamic performance.

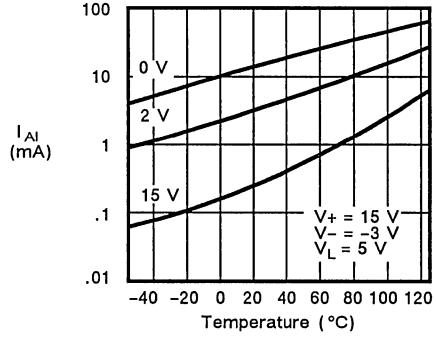


**TYPICAL CHARACTERISTICS**

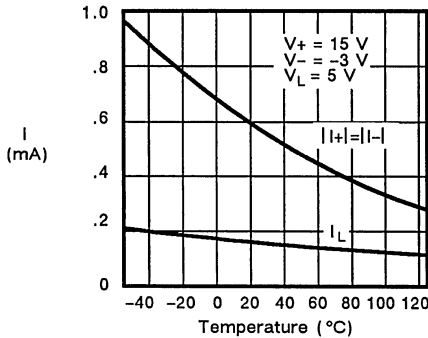
**Address Output Current vs. Temperature**



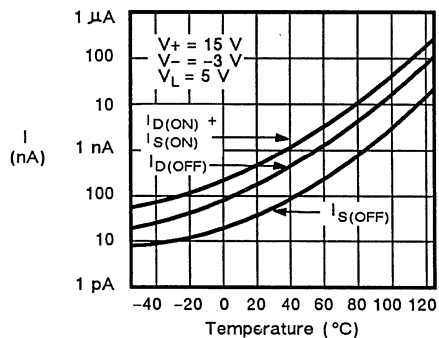
**Logic/Address Input Current vs. Temperature**



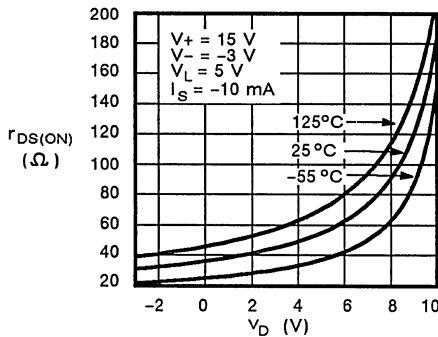
**Supply Currents vs. Temperature**



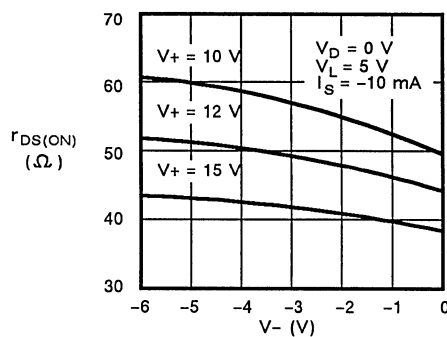
**Leakage vs. Temperature**



**$r_{DS(ON)}$  vs. Drain Voltage**

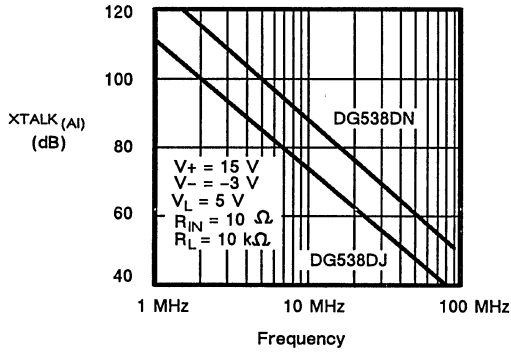


**$r_{DS(ON)}$  vs.  $V_-$ ;  $V_+$  Constant**

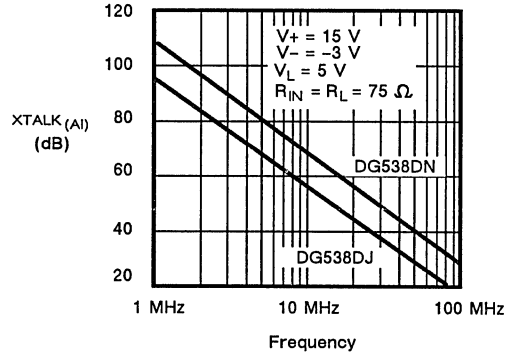


## TYPICAL CHARACTERISTICS (Cont'd)

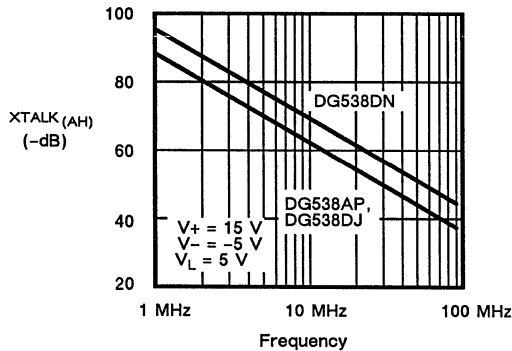
**Adjacent Input Crosstalk**  
See Figure 9



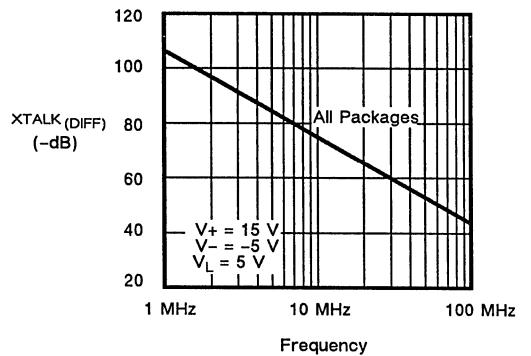
**Adjacent Input Crosstalk**  
See Figure 9



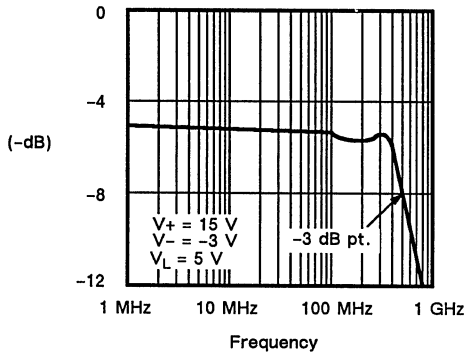
**All Hostile Crosstalk**  
See Figure 7



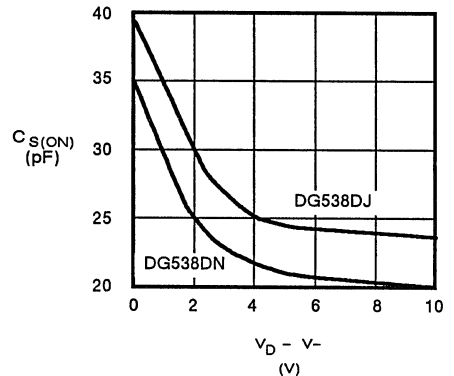
**Differential Crosstalk**  
See Figure 10



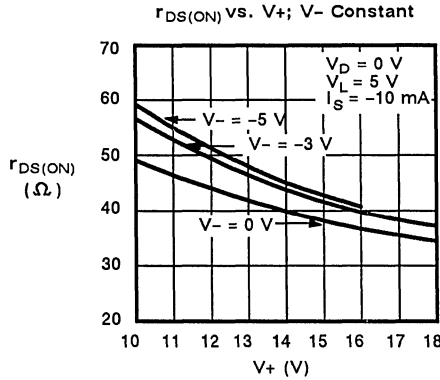
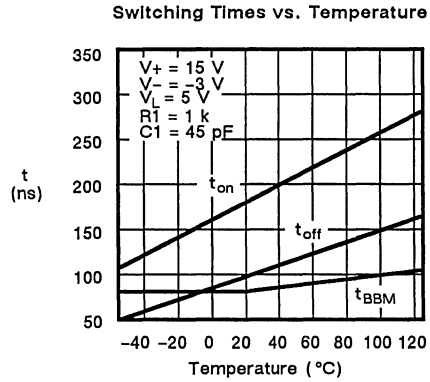
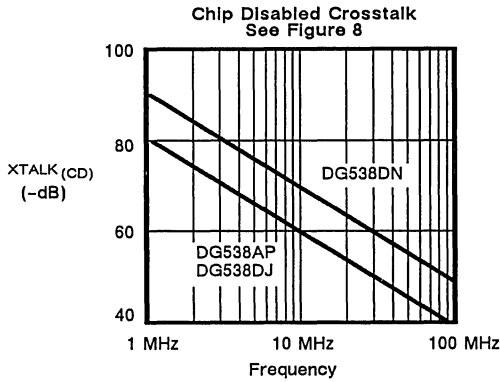
**Insertion Loss**  
See Figure 6



**ON State Capacitance**  
See Figure 11



**TYPICAL CHARACTERISTICS (Cont'd)**



**APPLICATIONS**

**Device Description**

The DG538 D/CMOS wideband multiplexer offers 8-channel single-ended or dual 4-channel functions. An  $\bar{8}/4$  logic input pin selects the single-ended or dual mode.

To meet the high dynamic performance demands of video, high definition TV, digital data routing (in excess of 100 Mb/s), etc., the DG538 is fabricated with DMOS transistors configured in 'T' arrangements with second level 'L' configurations (see Functional Block Diagram).

Use of DMOS technology yields devices with very low capacitance and low  $r_{DS(ON)}$ . This directly relates to improved high frequency signal handling, higher switching speeds, while maintaining low insertion loss figures. 'T' and 'L' switch configurations further improve dynamic performance by greatly reducing hostile crosstalk and output node capacitance.

**Frequency Response**

A single multiplexer on-channel exhibits both resistance ( $r_{DS(ON)}$ ) and capacitance ( $C_{S(ON)}$ ). This RC combination causes a frequency dependent attenuation of the analog signal. The -3 dB bandwidth of

## APPLICATIONS (Cont'd)

the DG538 is typically 500 MHz (into 50  $\Omega$ ). This figure of 500 MHz illustrates that the switch-channel cannot be represented by a simple RC combination. The ON capacitance of the channel is distributed along the ON resistance, and hence becomes a more complex multi-stage network of R's and C's making up the total  $r_{DS(ON)}$  and  $C_{S(ON)}$ .

### Power Supplies and Decoupling

A useful feature of the DG538 is its power supply flexibility. It can be operated from dual supply, or a single positive supply ( $V_-$  connected to 0 V) if required. Recommended operating voltage range is shown in Figure 13.

Note that the analog signal must not exceed  $V_-$  by more than -0.3 V (see absolute maximum ratings). However, the addition of a  $V_-$  pin has a number of advantages:

1. It allows flexibility in analog signal handling, i.e. with  $V_- = -5$  V and  $V_+ = 15$  V, up to  $\pm 5$  V ac signals can be accepted.
2. The value of ON capacitance ( $C_{S(ON)}$ ) may be reduced by increasing the reverse bias across the internal FET body to source junction. For more information see curve of  $C_{S(ON)}$  versus ( $V_D$  minus  $V_-$ ) voltage in typical characteristic data section.  $V_+$  has no effect on  $C_{S(ON)}$ .  
It is useful to note that tests indicate that optimum video differential phase and gain occur when  $V_-$  is -3 V.
3.  $V_-$  eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

It is established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG538 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

### Rules:

- a. Decoupling capacitors should be incorporated on all power supply pins ( $V_+$ ,  $V_-$ ,  $V_L$ ).

- b. They should be mounted as close as possible to the device pins.
- c. Capacitors should have good frequency characteristics - tantalum bead and/or ceramic disc types are suitable.

Recommended decoupling capacitors are 1 to 10  $\mu$ F tantalum bead, plus 10 to 100 nF ceramic or polyester.

- d. Additional high frequency protection may be provided by 51  $\Omega$  carbon film resistors connected in series with the power supply pins (see Figure 14).

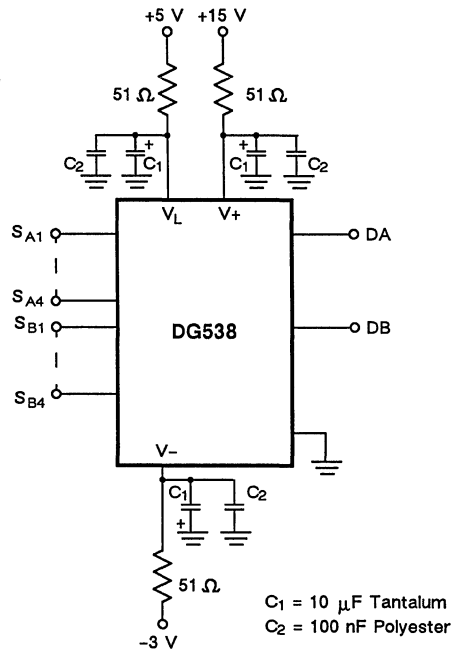


Figure 14. DG538 Power Supply Decoupling

**APPLICATIONS (Cont'd)**

**Board Layout**

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by the DG538. Some tips for minimizing stray effects are:

- i. Use extensive ground planes on double sided pcb separating adjacent signal paths. Multilayer pcb is even better.
- ii. Keep signal paths as short as practically possible with all-channel paths of near equal length.

Slight improvements in performance can be obtained by using DG538DN parts in preference to DG538DJ. The stray effects of the quad PLCC package are better than those of the 28-pin dual-in-line package.

**Interfacing**

Logic interfacing is easily accomplished with the DG538. Comprehensive addressing and control functions are incorporated in the design.

The addition of a  $V_L$  pin permits interface to various logic types. The device is primarily designed to be TTL logic compatible with +5 V applied to  $V_L$ . The DG538 actual switching threshold can be raised simply by increasing  $V_L$ .

A typical DG538 switching threshold versus  $V_L$  is shown in Figure 15.

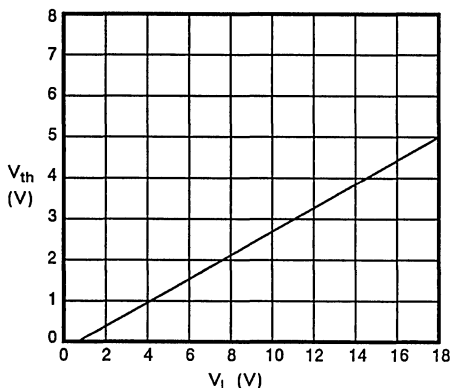


Figure 15. DG538 Switching Threshold Voltage vs.  $V_L$

The device features an address readback (Tally) facility, whereby the last address written to the device

may be output to the system. This allows improved status monitoring and handshaking without additional external components.

This function is controlled by the  $\bar{I/O}$  pin, which directly addresses the tri-state buffers applied to the address inputs ( $A_0$ - $A_2$ ). Address inputs can be assigned to accept data (when  $\bar{I/O} = 0$ ;  $\overline{WR} = 0$ ;  $\overline{RS} = 1$ ) or output data (when  $\bar{I/O} = 1$ ;  $\overline{WR} = 1$ ;  $\overline{RS} = 1$ ) or reflect a high impedance and latched state (when  $\bar{I/O} = 0$ ;  $\overline{WR} = 1$ ;  $\overline{RS} = 1$ ).

NOTE: (EN) must have been latched HIGH to allow proper readback, otherwise readback is suppressed.

When the  $\bar{I/O}$  assigns the address output condition, the address output can sink or source current for logic low and high respectively. Note that  $V_L$  is the logic high output condition. This point must be respected if  $V_L$  is varied for input logic threshold shifting.

Note:  $V_L$  must not exceed  $V+$  by more than +0.3 V. This must also apply when the power supply is turned on, i.e.  $V+$  must rise ahead of  $V_L$ .

Further control pins facilitate easy microprocessor interface. On chip address, data latches are activated by  $\overline{WR}$ , which serves as a strobe type function eliminating the need for peripheral latch or memory  $\bar{I/O}$  port devices. Also, for ease of interface, a direct reset function ( $\overline{RS}$ ) allows all latches to be cleared and switches opened. Reset should be used during power up, etc., to avoid spurious switch action. See Figure 16.

Channel address data can only be entered during  $\overline{WR}$  low, when the address latches are transparent and  $\bar{I/O}$  is low. Similarly data readback is only operational when  $\overline{WR}$  and  $\bar{I/O}$  are high.

Multiplexer output buffers are recommended to reduce insertion loss and transmission errors caused by ON resistance modulation effects. For low power power routing applications, a Siliconix 2N5911/2N5912 JFET may be employed in a source-follower circuit as shown below.

Note: For additional information please refer to AN88-2.

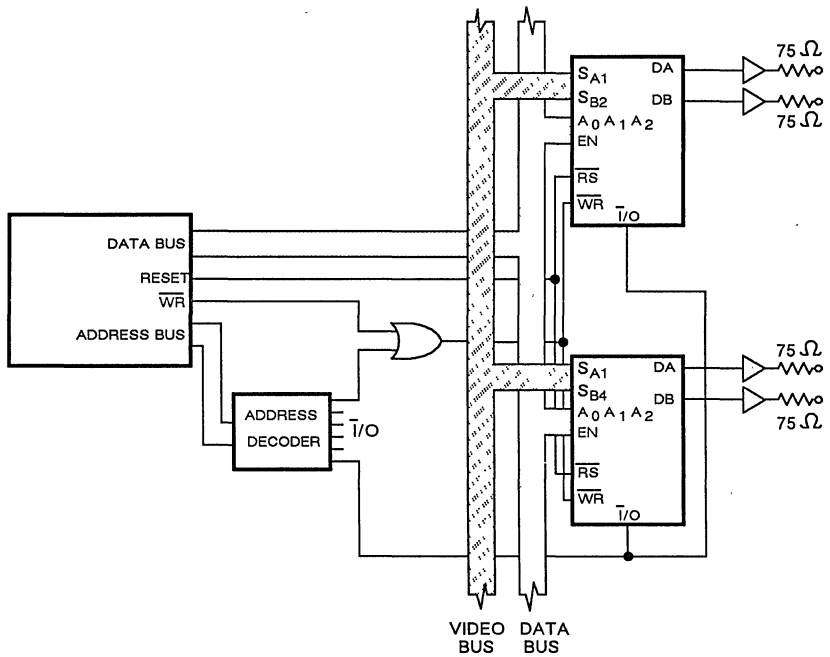


Figure 16. DG538 in a Video Matrix

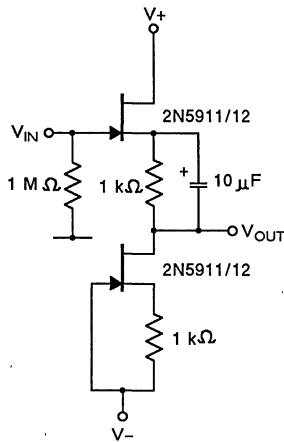


Figure 17. Discrete Video Buffer

# Quad SPST Wideband/ Video "T" Switch

## FEATURES

- Wide Bandwidth (500 MHz)
- Very Low Crosstalk ( -85 dB) and High OFF Isolation (-75 dB) at 5 MHz
- "T" Switch Configuration
- TTL Compatible
- Fast Switching ( $t_{ON} < 70$  ns)
- ESDS Protection  $> \pm 4000$  V
- Low  $r_{DS(ON)} < 75 \Omega$

## BENEFITS

- Improved Data Throughput
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Reduced Power Consumption

## APPLICATIONS

- Video Switching
- High Frequency Crosspoints
- Local and Wide Area Networks
- Video Routing
- Fast Data Acquisition
- ATE
- Radar/FLIR Systems

## DESCRIPTION

The DG540 is a very high performance monolithic quad SPST wideband/video switch designed for switching wide bandwidth analog and digital signals. By utilizing "T" switching techniques on each channel this device gives exceptionally low crosstalk and high OFF isolation. The crosstalk and OFF isolation are further improved by the introduction of GND pins between signal pins.

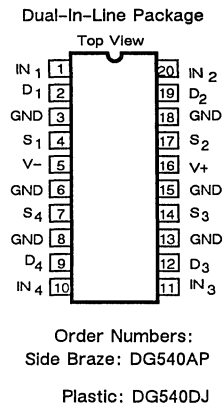
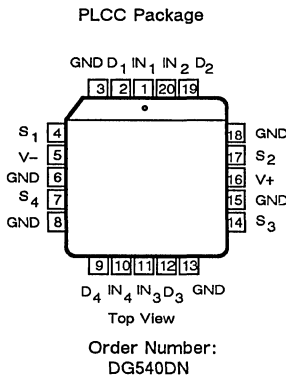
To achieve TTL compatibility with superior switching

performance, the DG540 was built on the Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when ON. Capacitance has been minimized to ensure fast switching.

Packaging includes the 20-pin side braze, plastic, and PLCC options. Performance grades include military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

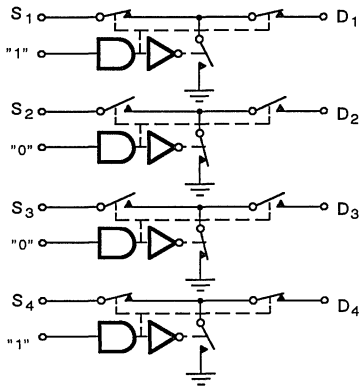
**7**

## PIN CONFIGURATION



## FUNCTIONAL BLOCK DIAGRAM

## TRUTH TABLE



LOGIC	SWITCH
0	OFF
1	ON

Logic "0"  $\leq 0.8$  V  
 Logic "1"  $\geq 2.0$  V

## ABSOLUTE MAXIMUM RATINGS

V+ to V-	-0.3 V to 19 V
V+ to GND	-0.3 V to +19 V
V- to GND	-19 V to +0.3 V
Digital Inputs	(V-) -0.3 V to (V+) +0.3 V or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub>	(V-) -0.3 V to (V-) +19 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal)	20 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max)	40 mA

Storage Temperature (A Suffix)	-65 to 150°C
(D Suffix)	-65 to 125°C
Operating Temperature (A Suffix)	-55 to 125°C
(D Suffix)	-40 to 85°C

### Power Dissipation (Package) \*

20-Pin Size Braze DIP**	900 mW
20-Pin Plastic DIP***	800 mW
16-Pin PLCC****	800 mW

\* All leads welded or soldered to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 7 mW/°C above 25°C.

\*\*\*\* Derate 10 mW/°C above 75°C.

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V GND = 0 V V <sub>INH</sub> = 2 V, V <sub>INL</sub> = 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>	V <sub>-</sub> = -5 V	1,2,3		-5	8	-5	8	V
Drain - Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 0 V	1,3	40		60		60	Ω
Resistance Match Between Channels	$\Delta$ r <sub>DS(ON)</sub>		2			100		75	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V, V <sub>D</sub> = 10 V	1	-0.05	-10	10	-10	10	nA
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = 10 V, V <sub>D</sub> = 0 V	2		-500	500	-100	100	
Total Switch ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V	1	-0.07	-10	10	-10	10	
			2		-1000	1000	-100	100	



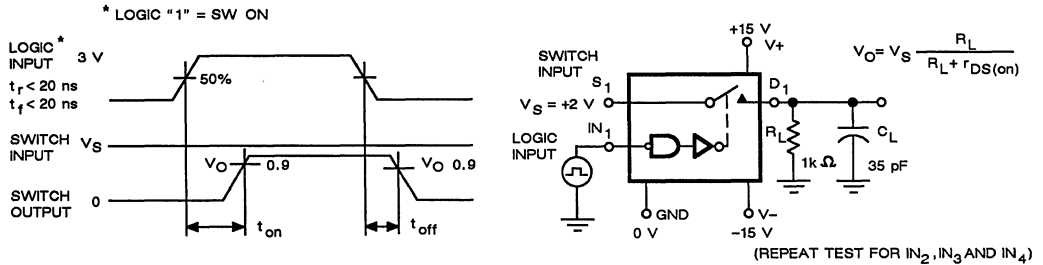
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V GND = 0 V V <sub>INH</sub> = 2 V, V <sub>INL</sub> = 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
Input Voltage High	V <sub>INH</sub>		1 2,3		2 2		2 2		V
Input Voltage Low	V <sub>INL</sub>		1 2,3			0.8 0.8		0.8 0.8	
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = GND or V <sub>+</sub>	1 2,3	0.05	-1 -20	1 20	-1 -20	1 20	μA
<b>DYNAMIC</b>									
OFF State Input Cap. <sup>c</sup>	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V	1	2		4		4	pF
OFF State Output Cap. <sup>c</sup>	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0 V	1	2		4		4	
ON State Input Cap. <sup>c</sup>	C <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V	1	14		20		20	
Bandwidth	BW	R <sub>L</sub> = 50 Ω See Bandwidth Test Circuit	1	500					MHz
Turn ON Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 35 pF, 50% to 90% See Switching Time Test Circuit	1 2,3	45		70 110		70 110	ns
Turn OFF Time	t <sub>OFF</sub>		1 2,3	20		50 85		50 85	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>D</sub> = 0 V See Test Circuit	1	25					pC
OFF Isolation		R <sub>IN</sub> = 75 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz, See Test Circuit	1	-75					dB
All Hostile Crosstalk <sup>c</sup>	XTALK <sub>(AH)</sub>	R <sub>IN</sub> = 10 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz, See Test Circuit	1	-85					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	All Channels ON or OFF	1 2,3	2.7		5 7		5 7	mA
Negative Supply Current	I <sub>-</sub>		1 2,3	2.3	-5 -7		-5 -7		

**NOTES:**

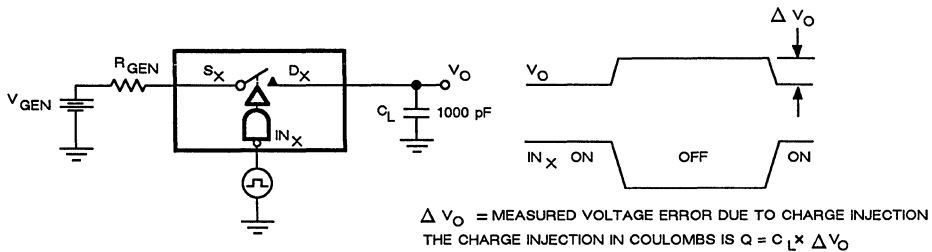
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- V<sub>IN</sub> = Input voltage to perform proper function.

## SWITCHING TIME TEST CIRCUIT

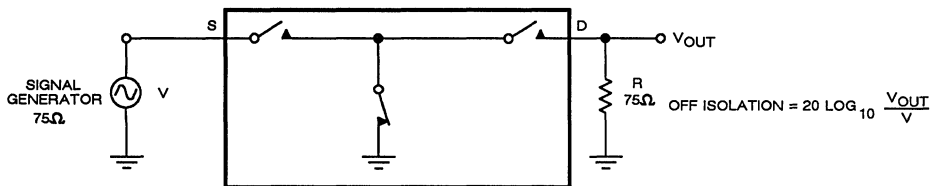
Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



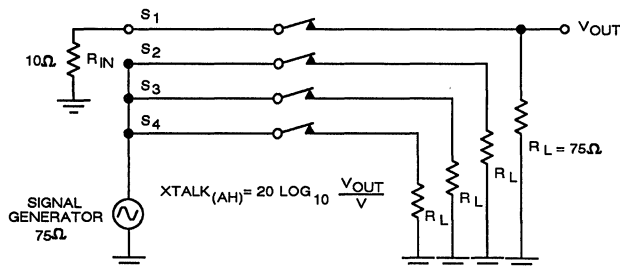
## CHARGE INJECTION TEST CIRCUIT



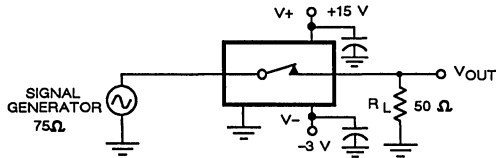
## OFF ISOLATION TEST CIRCUIT



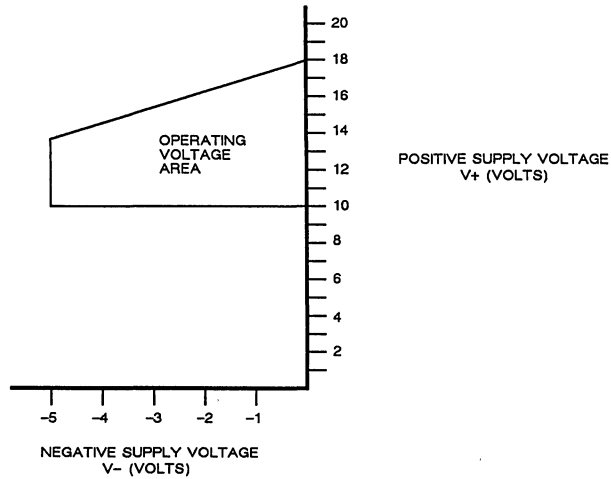
## ALL HOSTILE CROSSTALK - X TALK (AH)



**BANDWIDTH TEST CIRCUIT**



**OPERATING SUPPLY VOLTAGE RANGE**



**Note:**

1. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10  $\mu$ F tantalum bead in parallel with 100 nF ceramic disc.
2. Production tested with V+ = 15 V and V- = -3.0 V

**7**

**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
S	An Analog Channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply voltage
V-	Negative Supply Voltage
GND	Analog and Digital Ground

## Quad SPST Wideband/ Video "T" Switch

### FEATURES

- Wide Bandwidth (350 MHz)
- Very Low Crosstalk (-85 dB at 5 MHz)
- "T" Switch Configuration
- TTL Compatible
- Fast Switching ( $t_{ON} < 70$  ns)
- ESDS Protection  $> \pm 4000$  V
- Low  $r_{DS(ON)} < 75 \Omega$
- DG201A Pinout

### BENEFITS

- Improved Data Throughput
- Easily Interfaced
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Reduced Power Consumption

### APPLICATIONS

- Video Switching
- High Frequency Crosspoints
- Local and Wide Area Networks
- Video Routing
- Fast Data Acquisition
- ATE
- Radar/FLIR Systems

### DESCRIPTION

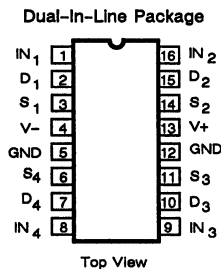
The DG541 is a high performance monolithic quad SPST wideband/video switch designed for switching wide bandwidth analog and digital signals. By utilizing "T" switching techniques on each channel this device gives exceptionally low crosstalk and high OFF isolation. Also, the DG541 is pin compatible with the industry standard DG201A analog switch.

To achieve TTL compatibility with superior switching

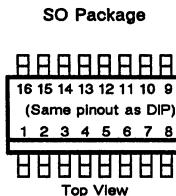
performance, the DG541 was built on the Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when ON. Capacitance has been minimized to ensure fast switching.

Packaging includes 16-pin side braze, plastic, and small outline options. Performance grades include military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

### PIN CONFIGURATION



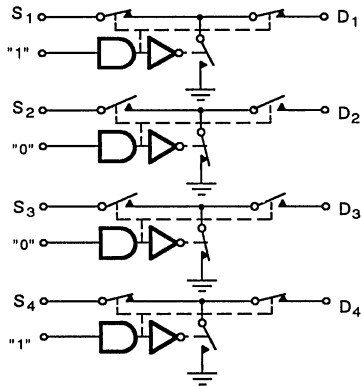
Order Numbers:  
Side Braze: DG541AP, DG541AP/883  
Plastic: DG541DJ



Order Number:  
DG541DY

**FUNCTIONAL BLOCK DIAGRAM**

**TRUTH TABLE**



LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.8 V  
Logic "1" ≥ 2.0 V

**ABSOLUTE MAXIMUM RATINGS**

V<sub>+</sub> to V<sub>-</sub> ..... -0.3 V to 19 V  
 V<sub>+</sub> to GND ..... -0.3 V to +19 V  
 V<sub>-</sub> to GND ..... -19 V to +0.3 V  
 Digital Inputs ..... (V<sub>-</sub>) -0.3 V to (V<sub>+</sub>) +0.3 V  
 or 20 mA, whichever occurs first  
 V<sub>S</sub>, V<sub>D</sub> ..... (V<sub>-</sub>) -0.3 V to (V<sub>-</sub>) + 19 V  
 or 20 mA, whichever occurs first  
 Continuous Current (Any Terminal) ..... 20 mA  
 Current, S or D (Pulsed 1 ms, 10% duty  
 cycle max) ..... 40 mA

Storage Temperature (A Suffix) ..... -65 to 150°C  
 (D Suffix) ..... -65 to 125°C  
 Operating Temperature (A Suffix) ..... -55 to 125°C  
 (D Suffix) ..... -40 to 85°C  
 Power Dissipation (Package)\*  
 16-Pin Side Braze\*\*\* ..... 900 mW  
 16-Pin Plastic DIP\*\*\* ..... 450 mW  
 16-Pin SO\*\*\*\* ..... 600 mW

\* All leads welded or soldered to PC board.  
 \*\* Derate 12 mW/°C above 75°C.  
 \*\*\* Derate 6 mW/°C above 75°C.  
 \*\*\*\* Derate 7.6 mW/°C above 75°C.

**ELECTRICAL CHARACTERISTICS<sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V GND = 0 V V <sub>INH</sub> = 2 V, V <sub>INL</sub> = 0.8 V <sup>g</sup>	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>	V <sub>-</sub> = -5V	1,2,3		-5	8	-5	8	V
Drain - Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 0 V	1,3 2	40		60 100		60 75	Ω
Resistance Match Between Channels	Δ r <sub>DS(ON)</sub>		1	2		6		6	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V, V <sub>D</sub> = 10 V	1 2	-0.05	-10 -500	10 500	-10 -100	10 100	nA
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = 10 V, V <sub>D</sub> = 0 V	1 2	-0.05	-10 -500	10 500	-10 -100	10 100	
Total Switch ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V	1 2	-0.07	-10 -1000	10 1000	-10 -100	10 100	

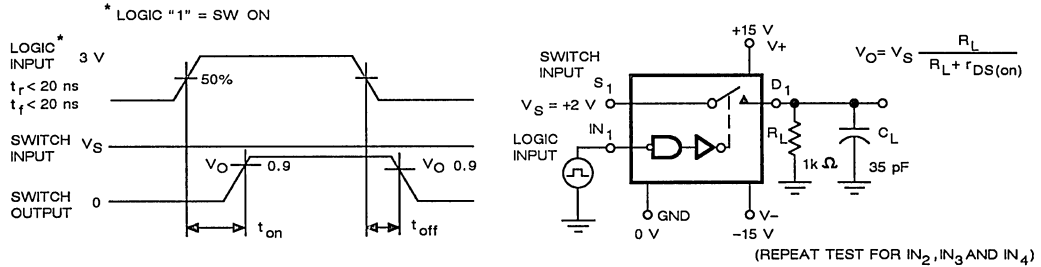
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V GND = 0 V V <sub>INH</sub> = 2 V, V <sub>INL</sub> = 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
Input Voltage High	V <sub>INH</sub>		1 2,3		2 2		2 2		V
Input Voltage Low	V <sub>INL</sub>		1 2,3			0.8 0.8		0.8 0.8	
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = GND or V <sub>+</sub>	1 2	0.05	-1 -20	1 20	-1 -20	1 20	μA
<b>DYNAMIC</b>									
OFF State Input Cap. <sup>c</sup>	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V	1	2		4		4	pF
OFF State Output Cap. <sup>c</sup>	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0 V	1	2		4		4	
ON State Input Cap. <sup>c</sup>	C <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V	1	14		20		20	
Bandwidth	BW	R <sub>L</sub> = 50 Ω See Figure 6	1	350					MHz
Turn ON Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 35 pF, 50% to 90% See Switching Time Test Circuit	1 2,3	45		70 140		70 140	ns
Turn OFF Time	t <sub>OFF</sub>		1 2,3	20		50 85		50 85	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>D</sub> = 0 V See Test Circuit	1	25					pC
OFF Isolation		R <sub>IN</sub> = 75 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz, See Test Circuit	1	-58					dB
All Hostile Crosstalk <sup>c</sup>	XTALK <sub>(AH)</sub>	R <sub>IN</sub> = 10 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz, See Test Circuit	1	-85					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	All Channels ON or OFF	1,2 3	2.7		5 7		5 7	mA
Negative Supply Current	I <sub>-</sub>		1,2 3	2.3	-5 -7		-5 -7		

**NOTES:**

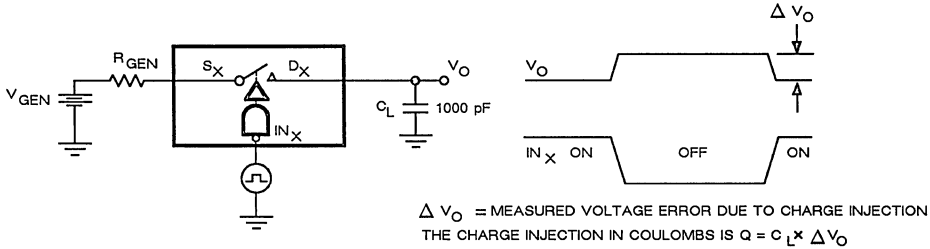
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- V<sub>IN</sub> = Input voltage to perform proper function.

SWITCHING TIME TEST CIRCUIT

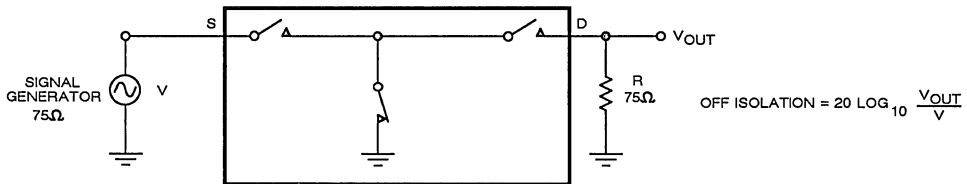
Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



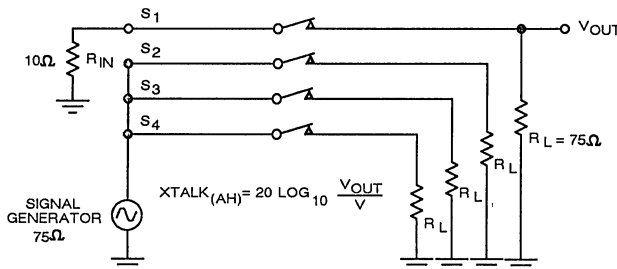
CHARGE INJECTION TEST CIRCUIT



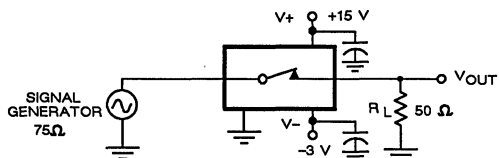
OFF ISOLATION TEST CIRCUIT



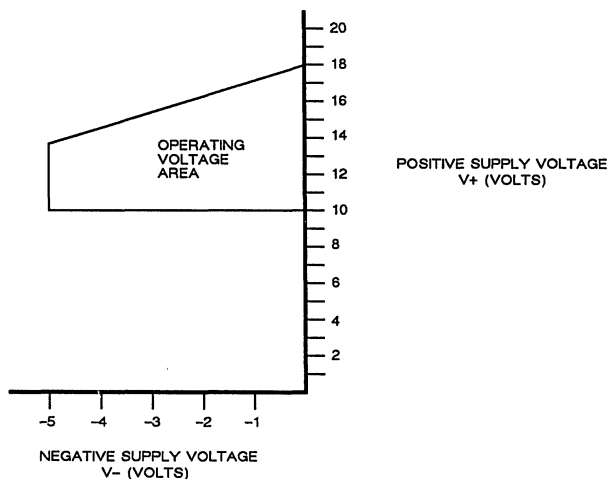
ALL HOSTILE CROSSTALK - X TALK (AH)



## BANDWIDTH TEST CIRCUIT



## OPERATING SUPPLY VOLTAGE RANGE



**Note:**

1. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10 $\mu$ F tantalum bead in parallel with 100 nF ceramic disc.
2. Production tested with V+ = 15 V and V- = -3.0 V

## PIN DESCRIPTION

SYMBOL	DESCRIPTION
S	An Analog Channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply voltage
V-	Negative Supply Voltage
GND	Analog and Digital Ground



## Dual SPDT Wideband/ Video "T" Switch

### FEATURES

- Wide Bandwidth (500 MHz)
- Very Low Crosstalk ( -85 dB) and High OFF Isolation (-75 dB) at 5 MHz
- TTL Compatible
- Low  $r_{DS(ON)} < 75 \Omega$
- "T" Switching Configuration
- ESDS Protection  $> \pm 4000 V$
- Fast Switching ( $t_{ON} < 100 ns$ )
- Break-Before-Make Switching

### BENEFITS

- Improved Data Throughput
- Easily Interfaced
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Reduced Power Consumption

### APPLICATIONS

- Video Switching
- High Frequency Crosspoints
- Local and Wide Area Networks
- Video Routing
- Fast Data Acquisition
- ATE
- Radar/FLIR Systems

### DESCRIPTION

The DG542 is a very high performance monolithic dual SPDT wideband/video switch designed for switching wide bandwidth analog and digital signals. By utilizing "T" switching techniques on each channel this device gives exceptionally low crosstalk and high OFF isolation. The crosstalk and OFF isolation are further improved by the introduction of GND pins between signal pins.

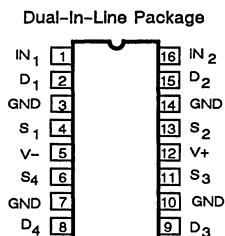
To achieve TTL compatibility with superior switching performance, the DG542 was built on the Siliconix

proprietary D/CMOS process. Each switch conducts equally well in both directions when ON. Capacitance has been minimized to ensure fast switching.

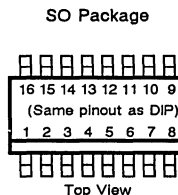
Packaging includes the 16-pin side braze, plastic, and small outline options. Performance grades include military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

**7**

### PIN CONFIGURATION



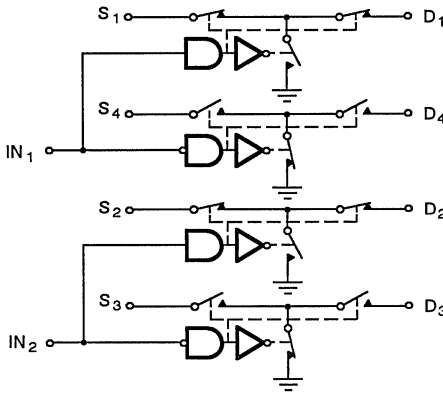
Top View  
Order Numbers:  
Side Braze: DG542AP, DG542AP/883  
Plastic: DG542DJ



Order Number:  
DG542DY

## FUNCTIONAL BLOCK DIAGRAM

## TRUTH TABLE



Truth Table\*

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V  
 Logic "1" ≥ 2.0 V

\* All Switches shown for logic "1" Input

## ABSOLUTE MAXIMUM RATINGS

V <sub>+</sub> to V <sub>-</sub> .....	-0.3 V to 19 V
V <sub>+</sub> to GND .....	-0.3 V to +19 V
V <sub>-</sub> to GND .....	-19 V to +0.3 V
Digital Inputs .....	(V <sub>-</sub> ) -0.3 V to (V <sub>+</sub> ) +0.3 V or 20 mA, whichever occurs first
V <sub>S</sub> , V <sub>D</sub> .....	(V <sub>-</sub> ) -0.3 V to (V <sub>-</sub> ) + 19 V or 20 mA, whichever occurs first
Continuous Current (Any Terminal) .....	20 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max) .....	40 mA

Storage Temperature (A Suffix) .....	-65 to 150°C
(D Suffix) .....	-65 to 125°C
Operating Temperature (A Suffix) .....	-55 to 125°C
(D Suffix) .....	-40 to 85°C

### Power Dissipation (Package)\*

16-Pin Side Braze** .....	900 mW
16-Pin Plastic DIP*** .....	450 mW
16-Pin SO**** .....	600 mW

\* All leads welded or soldered to PC board.

\*\* Derate 12 mW/°C above 75°C.

\*\*\* Derate 6 mW/°C above 75°C.

\*\*\*\* Derate 7.6 mW/°C above 75°C.

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V GND = 0 V V <sub>INH</sub> = 2 V, V <sub>INL</sub> = 0.8 V <sup>o</sup>	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SWITCH</b>									
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>	V <sub>-</sub> = -5 V	1,2,3		-5	8	-5	8	V
Drain - Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -10 mA, V <sub>D</sub> = 0 V	1,3 2	40		60 100		60 75	Ω
Resistance Match Between Channels	r <sub>ΔDS(ON)</sub>		1	2		6		6	
Source OFF Leakage Current	I <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V, V <sub>D</sub> = 10 V	1 2	-0.05	-10 -500	10 500	-10 -100	10 100	nA
Drain OFF Leakage Current	I <sub>D(OFF)</sub>	V <sub>S</sub> = 10 V, V <sub>D</sub> = 0 V	1 2	-0.05	-10 -500	10 500	-10 -100	10 100	
Total Switch ON Leakage Current	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V	1 2	-0.07	-10 -1000	10 1000	-10 -100	10 100	

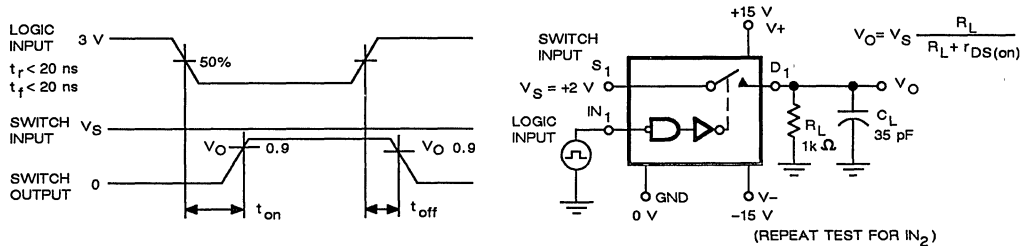
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -3 V GND = 0 V V <sub>INH</sub> = 2 V, V <sub>INL</sub> = 0.8 V <sup>e</sup>	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
Input Voltage HIGH	V <sub>INH</sub>		1 2,3		2 2		2 2		V
Input Voltage LOW	V <sub>INL</sub>		1 2,3			0.8 0.8		0.8 0.8	
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = GND or V <sub>+</sub>	1 2,3	0.05	-1 -20	1 20	-1 -20	1 20	μA
<b>DYNAMIC</b>									
OFF State Input Cap. <sup>c</sup>	C <sub>S(OFF)</sub>	V <sub>S</sub> = 0 V	1	2		4		4	pF
OFF State Output Cap. <sup>c</sup>	C <sub>D(OFF)</sub>	V <sub>D</sub> = 0 V	1	2		4		4	
ON State Input Cap. <sup>c</sup>	C <sub>S(ON)</sub>	V <sub>S</sub> = V <sub>D</sub> = 0 V	1	14		20		20	
Bandwidth	BW	R <sub>L</sub> = 50 Ω See Test Circuit	1	500					MHz
Break-Before-Make Interval	t <sub>OPEN</sub>	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 35 pF, 50% to 90% See Test Circuit	1		10		10		ns
Turn ON Time	t <sub>ON</sub>	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 35 pF, 50% to 90% See Test Circuit	1 2,3	65		100 140		100 140	
Turn OFF Time	t <sub>OFF</sub>		1 2,3	25		60 85		60 85	
Charge Injection	Q	C <sub>L</sub> = 1000 pF, V <sub>D</sub> = 0 V See Test Circuit	1	25					pC
OFF Isolation		R <sub>IN</sub> = 75 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz, See Test Circuit	1	-75					dB
All Hostile Crosstalk	XTALK <sub>(AH)</sub>	R <sub>IN</sub> = 10 Ω, R <sub>L</sub> = 75 Ω f = 5 MHz, See Test Circuit	1	-85					
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	All Channels ON or OFF	1 2,3	2.7		5 7		5 7	mA
Negative Supply Current	I <sub>-</sub>		1 2,3	2.3	-5 -7		-5 -7		

**NOTES:**

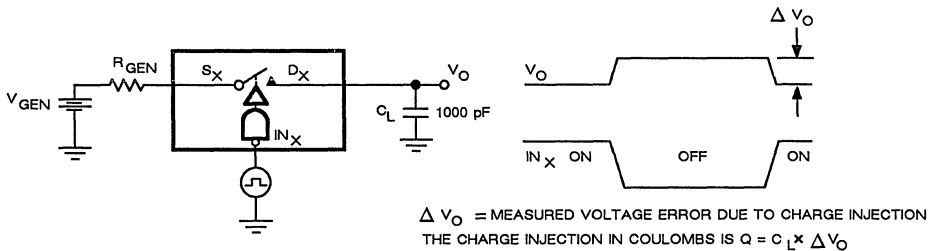
- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- V<sub>IN</sub> = Input voltage to perform proper function.

## SWITCHING TIME TEST CIRCUIT

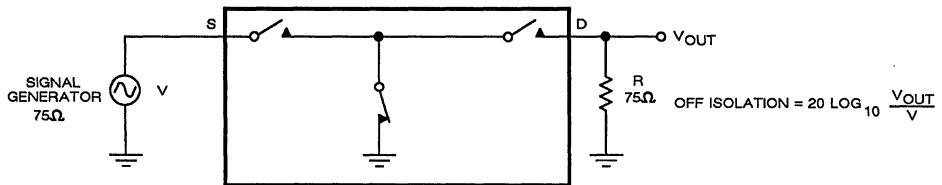
Switch output waveform shown for  $V_S = \text{constant}$  with logic input waveform as shown. Note that  $V_S$  may be + or - as per switching time test circuit.  $V_O$  is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



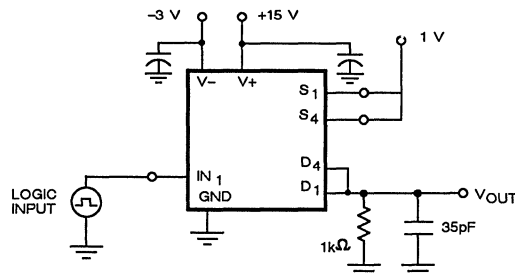
## CHARGE INJECTION TEST CIRCUIT



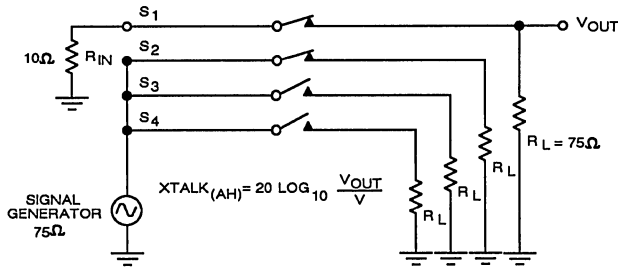
## OFF ISOLATION TEST CIRCUIT



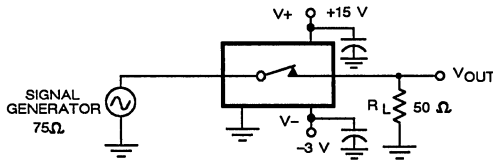
## BREAK-BEFORE-MAKE TEST CIRCUIT



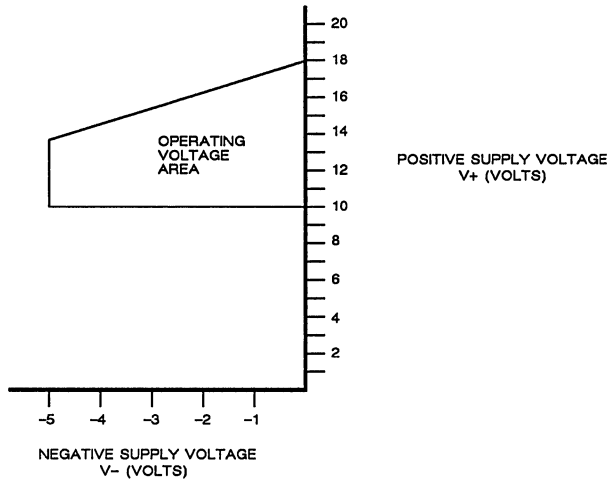
**ALL HOSTILE CROSSTALK – X TALK (AH)**



**BANDWIDTH TEST CIRCUIT**



**OPERATING SUPPLY VOLTAGE RANGE**



**Note:**

- Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10µF tantalum bead in parallel with 100 nF ceramic disc.
- Production tested with V+ = 15 V and V- = -3.0 V

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## PIN DESCRIPTION

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SYMBOL	DESCRIPTION
S	An Analog Channel Input or Output
D	An Analog Channel Output or Input
IN	Logic Control Input
V+	Positive Supply voltage
V-	Negative Supply Voltage
GND	Analog and Digital Ground

# SD5000/5001/5002 DMOS FET Quad Analog Switch Arrays

## FEATURES

- Low "ON" Resistance  
(70  $\Omega$  max @  $V_{GS} = 5$  V)
- Low Source Capacitance  
( $C_S < 5$  pF)
- Low Drain Capacitance  
( $C_D < 1.6$  pF)
- Low Crosstalk  
(-60 dB @ 1 MHz)
- Fast Switching Speed  
( $t_{ON} < 1$  ns)

## BENEFITS

- Low Insertion Loss
- Reduces Buffer Drive Requirements
- Reduces Summing Node Capacitance
- Improves Channel Isolation
- Increases Sampling Rate

## APPLICATIONS

- Audio Switching
- Wideband Switching
- Wideband Multiplexing
- Video Crosspoints
- Sample and Hold

## DESCRIPTION

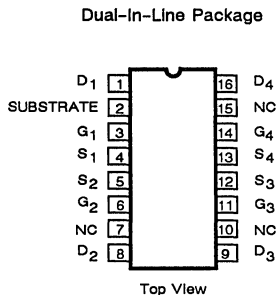
The Siliconix SD5000 series is a monolithic array of n-channel enhancement-mode DMOS FETs configured as single-pole, single-throw analog switches. Their low capacitance, low ON resistance and fast switching speed make them ideal for high speed switching of audio, video, and high frequency signals in communications, instrumentation, and process control applications. Designed on the Siliconix DMOS process, the SD5000 is rated for analog signals of  $\pm 10$  V while the SD5001 and SD5002 are rated for  $\pm 5$  V and  $\pm 7.5$  V respectively.

The threshold voltage for all switches is 2 V maximum, simplifying the logic interface for low level signal applications.

The SD5000 family is available in 16-pin plastic and sidebrazed dual-in-line packages, and is rated for operation over the (0 to 85°C) temperature range. For information on surface mount versions, see the SD5400 series data sheet.

For more information, please refer to Siliconix Application Notes AN83-7, AN83-15, and "DMOS FET Analog Switches and Switch Arrays".

## PIN CONFIGURATION

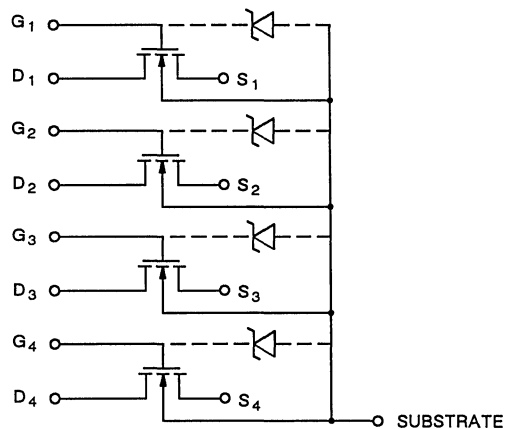


Order Numbers:

Side Braze: SD5000I, SD5001I, SD5002I

PDIP: SD5000N, SD5001N, SD5002N

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

	SD5000	SD5001	SD5002	SD5000	SD5001	SD5002	
$V_{DS}$ .....	20 V	10 V	15 V	$V_{GD}$ .....	30/-25 V	25/-15 V	30/-22.5 V
$V_{SD}^e$ .....	20 V	10 V	15 V	$I_D$ .....	50 mA		
$V_{DB}$ .....	25 V	15 V	22.5 V	Operating Temperature .....	0 to 85°C		
$V_{SB}$ .....	25 V	15 V	22.5 V	Storage Temperature .....	-55 to 150°C		
$V_{GS}$ .....	30/-25 V	25/-15 V	30/-22.5 V	Power Dissipation (Package) <sup>f</sup> .....	640 mW		
$V_{GB}$ .....	30/-0.3 V	25/-0.3 V	30/-0.3 V	(Each Device) .....	300 mW		

ELECTRICAL CHARACTERISTICS <sup>a</sup>					T <sub>A</sub> = 25°C		
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNIT
			DEVICE	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>STATIC</b>							
Analog Signal Range <sup>c</sup>	V <sub>ANALOG</sub>		SD5000		-10	10	V
			SD5001		-5	5	
			SD5002		-7.5	7.5	
Drain-Source Breakdown Voltage	BV <sub>DS</sub>	V <sub>GS</sub> = V <sub>BS</sub> = -5 V I <sub>D</sub> = 10 nA	SD5000	25	20		
			SD5001	25	10		
			SD5002	25	15		
Source-Drain Breakdown Voltage	BV <sub>SD</sub>	V <sub>GD</sub> = V <sub>BD</sub> = -5 V I <sub>S</sub> = 10 nA	SD5000		20		
			SD5001		10		
			SD5002		15		
Drain-Substrate Breakdown Voltage	BV <sub>DB</sub>	V <sub>GB</sub> = 0 V, I <sub>D</sub> = 10 nA Source Open	SD5000		25		
			SD5001		15		
			SD5002		22.5		
Source-Substrate Breakdown Voltage	BV <sub>SB</sub>	V <sub>GB</sub> = 0 V, I <sub>S</sub> = 10 μA Drain Open	SD5000		25		
			SD5001		15		
			SD5002		22.5		



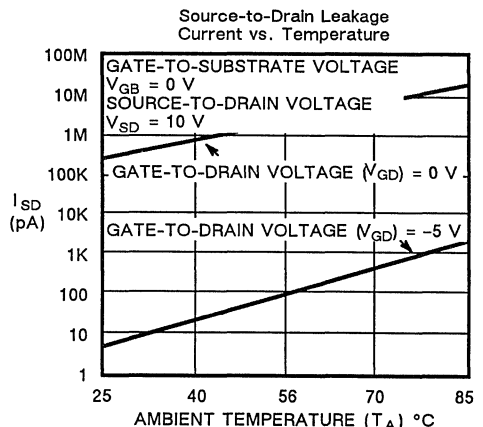
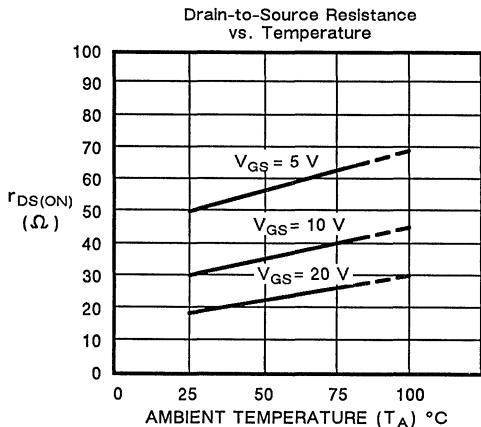
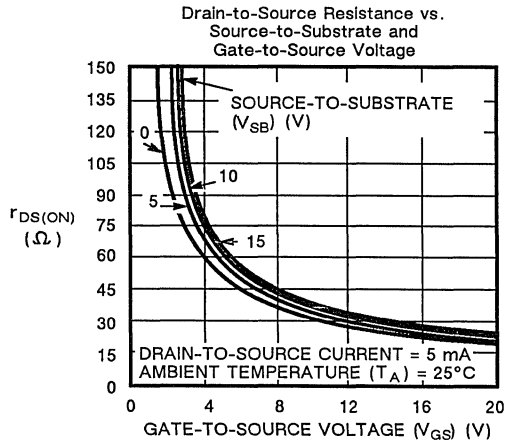
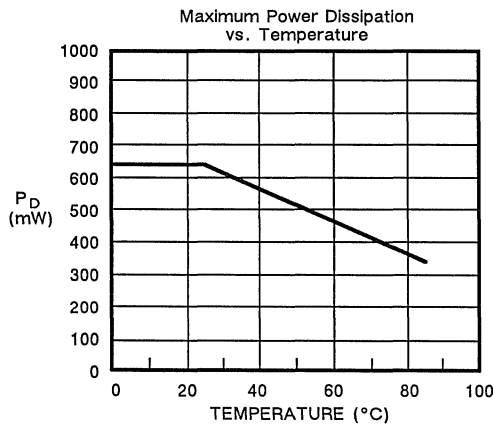
ELECTRICAL CHARACTERISTICS <sup>a</sup>								$T_A = 25^\circ\text{C}$	
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNIT		
			DEVICE	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>STATIC (Cont'd)</b>									
Drain-Source Leakage Current	$I_{DS(OFF)}$	$V_{GS} = V_{BS} = -5\text{ V}$	$V_{DS} = 20\text{ V}$	SD5000	1		10	nA	
			$V_{DS} = 10\text{ V}$	SD5001	1		10		
			$V_{DS} = 15\text{ V}$	SD5002	1		10		
Source-Drain Leakage Current	$I_{SD(OFF)}$	$V_{GD} = V_{BD} = -5\text{ V}$	$V_{SD} = 20\text{ V}$	SD5000	1		10	nA	
			$V_{SD} = 10\text{ V}$	SD5001	1		10		
			$V_{SD} = 15\text{ V}$	SD5002	1		10		
Gate Leakage Current	$I_{GBS}$	$V_{DB} = V_{SB} = 0\text{ V}$	$V_{GB} = 30\text{ V}$	SD5000			1	$\mu\text{A}$	
			$V_{GB} = 25\text{ V}$	SD5001			1		
			$V_{GB} = 30\text{ V}$	SD5002			1		
Threshold Voltage	$V_T$	$V_{DS} = V_{GS} = V_T$ $I_D = 1\ \mu\text{A}, V_{SB} = 0\text{ V}$			1.0	0.1	2.0	V	
Drain-Source ON Resistance	$r_{DS(ON)}$	$I_D = 1\text{ mA}$ $V_{SB} = 0\text{ V}$	$V_{GS} = 5\text{ V}$	All		50		70	$\Omega$
			$V_{GS} = 10\text{ V}$			30			
			$V_{GS} = 15\text{ V}$			23			
			$V_{GS} = 20\text{ V}$			19			
Resistance Match <sup>e</sup>	$\Delta r_{DS(ON)}$		$V_{GS} = 5\text{ V}$		1		5	V	
<b>DYNAMIC</b>									
Gate Node Capacitance	$C_G$	$V_{DS} = 10\text{ V}$ $V_{GS} = V_{BS} = -15\text{ V}$ $f = 1\text{ MHz}$	All		2.4		3.5	pF	
Drain Node Capacitance	$C_D$				1.3		1.6		
Source Node Capacitance	$C_S$				3.5		5		
Reverse Transfer Capacitance	$C_{DG}$				0.3		0.5		

ELECTRICAL CHARACTERISTICS <sup>a</sup>				LIMITS			$T_A = 25^\circ\text{C}$
PARAMETER	SYMBOL	TEST CONDITIONS	DEVICE	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>DYNAMIC (Cont'd)</b>							
Forward Transconductance	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ mA}$ $V_{SB} = 0\text{ V}, f = 1\text{ kHz}$	All	15	10		mS
Crosstalk	XTALK	See Test Circuits 1 and 2 $f = 3\text{ kHz}$		-107			dB

**NOTES:**

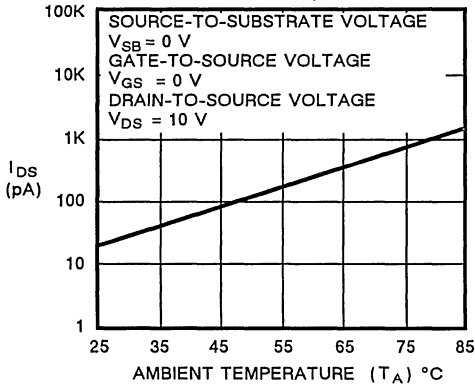
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Refer to test conditions specified in Electrical Characteristics Tables.
- f. Derate 5 mW/°C above 25°C.

## TYPICAL CHARACTERISTICS

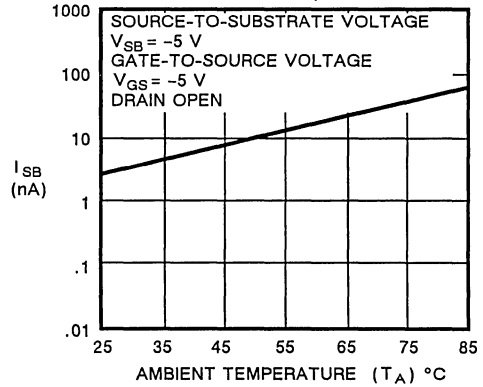


## TYPICAL CHARACTERISTICS

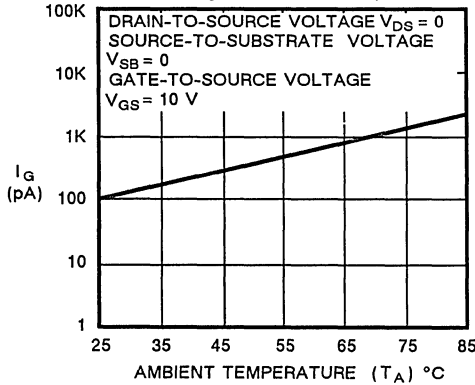
Drain-to-Source Leakage  
Current vs. Temperature



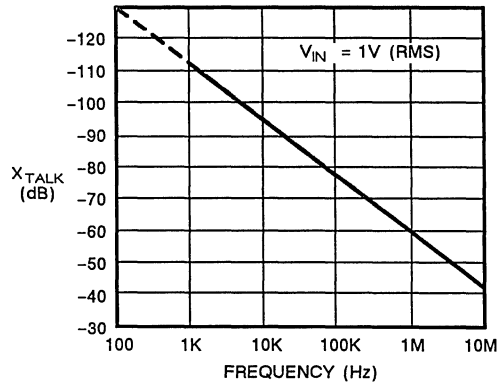
Source-to-Substrate Leakage  
Current vs. Temperature



Gate Leakage Current vs. Temperature



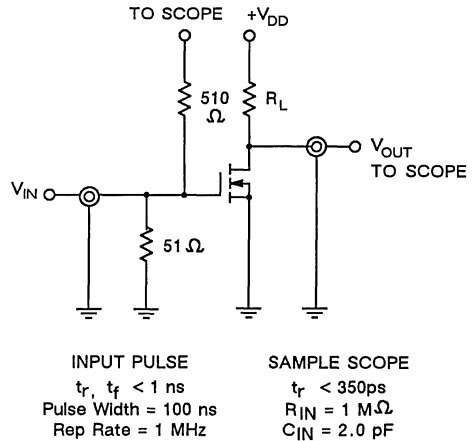
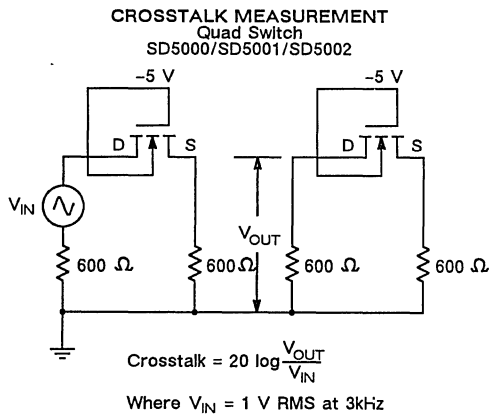
Crosstalk vs. Frequency



7

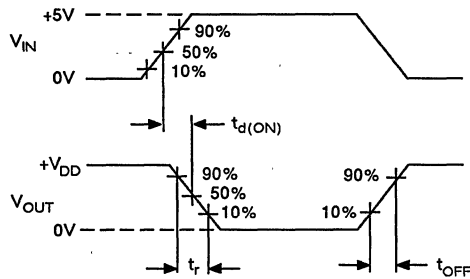
## TEST CIRCUIT

## SWITCHING TEST CIRCUIT



## SWITCHING WAVEFORMS

## SWITCHING CHARACTERISTICS



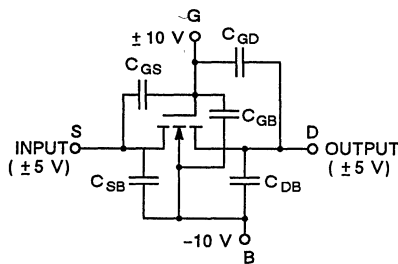
V <sub>DD</sub>	R <sub>L</sub>	t <sub>d(on)</sub> (ns)		t <sub>r</sub> (ns)		*t <sub>OFF</sub> (ns)	
		TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1 k	0.9		1.0		14.0	

\*t<sub>OFF</sub> is dependent on R<sub>L</sub> and does not depend on the device characteristics.

## THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of  $\pm 10$  V for the SD5000,  $\pm 5$  V for the SD5001 and  $\pm 7.5$  V for the SD5002. Each switch of the array is a DMOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally OFF when gate-to-source voltage ( $V_{GS}$ ) is 0 V. When  $V_{GS}$  exceeds the threshold voltage,  $V_T$ , the FET switch starts to turn ON. With  $V_{GS}$  in excess of +10 V, a low resistance path (typically 30  $\Omega$ ) exists between input and output of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for  $\pm 5$  V analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output.

When analog signals are routed from one point to another the important factors are isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation. The SD5000 series offers superior performance in all these areas (Figure 1).



**Isolation.** ON resistance is typically 30  $\Omega$  and OFF resistance is typically  $10^{10}$   $\Omega$ , which results in an OFF to ON resistance ratio in excess of  $10^9$ . Isolation from output to input from 3 kHz analog signals is typically -107 dB, and at 1MHz the isolation is typically -60 dB.

**Feedback and feedthrough transients** are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitches" are minimized, resulting in "clean" signals at the output.

**Insertion loss** depends upon the source and load impedances involved. As an example, for 600  $\Omega$  source impedance the insertion loss for voice signals (1 V<sub>RMS</sub> @ 3 kHz) is less than 0.3 dB. Thus the SD5000 series makes good telephone cross-point switches.

**Speed.** Because of the low ON resistance and low input capacitance, the SD5000 switches turn ON at subnanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30 dB @ 1 GHz).

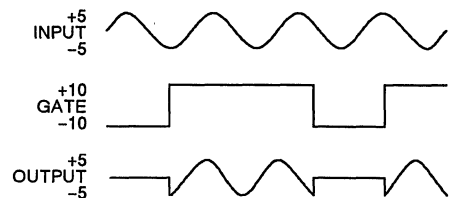


Figure 1

## APPLICATION

Figure 2 shows an SD5002 configured for operation as a one of two channel video switch. The "L" switches of the two channels are terminated at the input by the two  $R_O$  resistors, allowing impedance

matching to various transmission line impedances. The switches can be directly controlled by standard CMOS or TTL logic gates. For more detailed information on this application, see AN83-15.

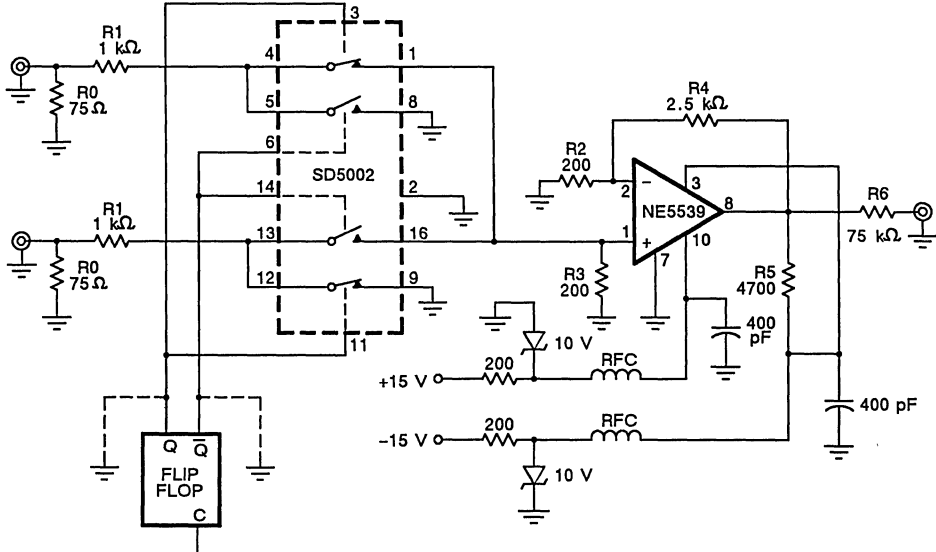


Figure 2. High Performance Video Switch

# SD5400/5401/5402

## DMOS FET Quad

### Analog Switch Arrays

#### FEATURES

- Low "ON" Resistance  
( $70 \Omega$  max @  $V_{GS} = 5 V$ )
- Low Source Capacitance  
( $C_S < 6 pF$ )
- Low Drain Capacitance  
( $C_D < 2 pF$ )
- Low Crosstalk  
( $-60 dB @ 1 MHz$ )
- Fast Switching Speed  
( $t_{ON} < 1 ns$ )
- Small Outline Package

#### BENEFITS

- Low Insertion Loss
- Reduces Buffer Drive Requirements
- Reduces Summing Node Capacitance
- Improves Channel Isolation
- Increases Sampling Rate
- Reduces Board Space

#### APPLICATIONS

- Audio Switching
- Wideband Switching
- Wideband Multiplexing
- Video Crosspoints
- Sample and Hold

#### DESCRIPTION

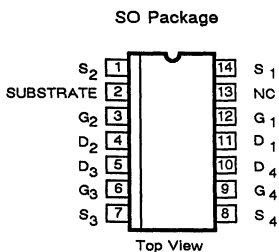
The Siliconix SD5400 series is a monolithic array of n-channel enhancement-mode DMOS FETs configured as single-pole, single-throw analog switches. Their low capacitance, low ON resistance and fast switching speed make them ideal for high speed switching of audio, video, and high frequency signals in communications, instrumentation, and process control applications. Designed on the Siliconix DMOS process, the SD5400 is rated for analog signals of  $\pm 10 V$  while the SD5401 and SD5402 are rated for  $\pm 5 V$  and  $\pm 7.5 V$  respectively. The threshold voltage for all switches is  $2 V$

maximum, simplifying the logic interface for low level signal applications.

The SD5400 family is available in a 14-pin plastic Small Outline (SO) package for surface mount applications, and is rated for operation over the commercial, C suffix (0 to  $70^\circ C$ ) temperature range. For conventional through hole DIP packages, please refer to the SD5000 series data sheet.

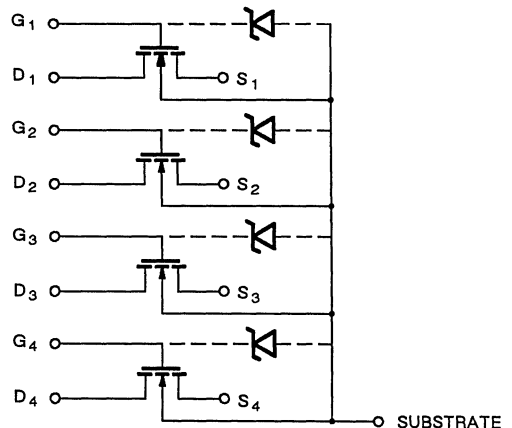
For more information, please refer to Siliconix Application Notes AN83-7, AN83-15, and "DMOS FET Analog Switches and Switch Arrays".

#### PIN CONFIGURATION



Order Numbers:  
SD5400CY, SD5401CY  
SD5402CY

#### FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

	SD5400	SD5401	SD5402		SD5400	SD5401	SD5402
$V_{DS}$ .....	20 V	10 V	15 V	$V_{GD}$ .....	30/-25 V	25/-15 V	30/-22.5 V
$V_{SD}^e$ .....	20 V	10 V	15 V	$I_D$ .....	50 mA		
$V_{DB}$ .....	25 V	15 V	22.5 V	Operating Temperature .....	0 to 70°C		
$V_{SB}$ .....	25 V	15 V	22.5 V	Storage Temperature .....	-55 to 150°C		
$V_{GS}$ .....	30/-25 V	25/-15 V	30/-22.5 V	Power Dissipation (Package) <sup>f</sup> .....	640 mW		300 mW
$V_{GB}$ .....	30/-0.3 V	25/-0.3 V	30/-0.3 V	(Each Device) .....			

ELECTRICAL CHARACTERISTICS <sup>a</sup>				$T_A = 25^\circ\text{C}$			
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNIT
			DEVICE	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>STATIC</b>							
Analog Signal Range <sup>c</sup>	$V_{ANALOG}$		SD5400		-10	10	V
			SD5401		-5	5	
			SD5402		-7.5	7.5	
Drain-Source Breakdown Voltage	$BV_{DS}$	$V_{GS} = V_{BS} = -5\text{ V}$ $I_D = 10\text{ nA}$	SD5400	25	20		V
			SD5401	25	10		
			SD5402	25	15		
Source-Drain Breakdown Voltage	$BV_{SD}$	$V_{GD} = V_{BD} = -5\text{ V}$ $I_S = 10\text{ nA}$	SD5400		20		V
			SD5401		10		
			SD5402		15		
Drain-Substrate Breakdown Voltage	$BV_{DB}$	$V_{GB} = 0\text{ V}, I_D = 10\text{ nA}$ Source Open	SD5400		25		V
			SD5401		15		
			SD5402		22.5		
Source-Substrate Breakdown Voltage	$BV_{SB}$	$V_{GB} = 0\text{ V}, I_S = 10\text{ }\mu\text{A}$ Drain Open	SD5400		25		V
			SD5401		15		
			SD5402		22.5		

ELECTRICAL CHARACTERISTICS <sup>a</sup>						T <sub>A</sub> = 25°C			
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNIT		
			DEVICE	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>STATIC (Cont'd)</b>									
Drain-Source Leakage Current	I <sub>DS(OFF)</sub>	V <sub>GS</sub> = V <sub>BS</sub> = -5 V	V <sub>DS</sub> = 20 V	SD5400	1		10	nA	
			V <sub>DS</sub> = 10 V	SD5401	1		10		
			V <sub>DS</sub> = 15 V	SD5402	1		10		
Source-Drain Leakage Current	I <sub>SD(OFF)</sub>	V <sub>GD</sub> = V <sub>BD</sub> = -5 V	V <sub>SD</sub> = 20 V	SD5400	1		10	nA	
			V <sub>SD</sub> = 10 V	SD5401	1		10		
			V <sub>SD</sub> = 15 V	SD5402	1		10		
Gate Leakage Current	I <sub>GBS</sub>	V <sub>DB</sub> = V <sub>SB</sub> = 0 V	V <sub>GB</sub> = 30 V	SD5400			1	μA	
			V <sub>GB</sub> = 25 V	SD5401			1		
			V <sub>GB</sub> = 30 V	SD5402			1		
Threshold Voltage	V <sub>T</sub>	V <sub>DS</sub> = V <sub>GS</sub> = V <sub>T</sub> I <sub>D</sub> = 1 μA, V <sub>SB</sub> = 0 V			1.0	0.1	2.0	V	
Drain-Source ON Resistance	r <sub>DS(ON)</sub>	I <sub>D</sub> = 1 mA V <sub>SB</sub> = 0 V	V <sub>GS</sub> = 5 V	All		50		70	Ω
			V <sub>GS</sub> = 10 V			30			
			V <sub>GS</sub> = 15 V			23			
			V <sub>GS</sub> = 20 V			19			
Resistance Match <sup>c</sup>	Δr <sub>DS(ON)</sub>		V <sub>GS</sub> = 5 V		1		5		
<b>DYNAMIC</b>									
Gate Node Capacitance	C <sub>G</sub>	V <sub>DS</sub> = 10 V V <sub>GS</sub> = V <sub>BS</sub> = -15 V f = 1 MHz	All		2.4		3.5	pF	
Drain Node Capacitance	C <sub>D</sub>				1.3		2		
Source Node Capacitance	C <sub>S</sub>				3.5		6		
Reverse Transfer Capacitance	C <sub>DG</sub>				0.3		0.5		



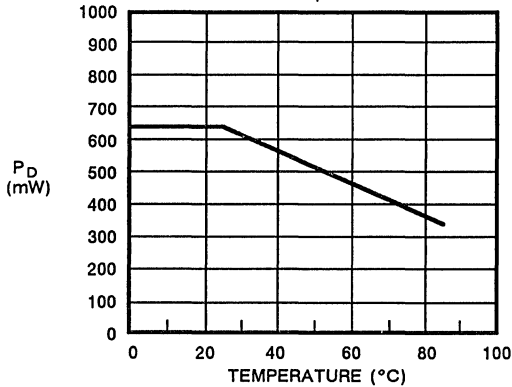
ELECTRICAL CHARACTERISTICS <sup>a</sup>				T <sub>A</sub> = 25°C			
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			DEVICE	TYP <sup>d</sup>	MIN <sup>b</sup>		MAX <sup>b</sup>
<b>DYNAMIC (Cont'd)</b>							
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 mA V <sub>SB</sub> = 0 V, f = 1 kHz	All	15	10		mS
Crosstalk	XTALK	See Test Circuits 1 and 2 f = 3 kHz		-107			

**NOTES:**

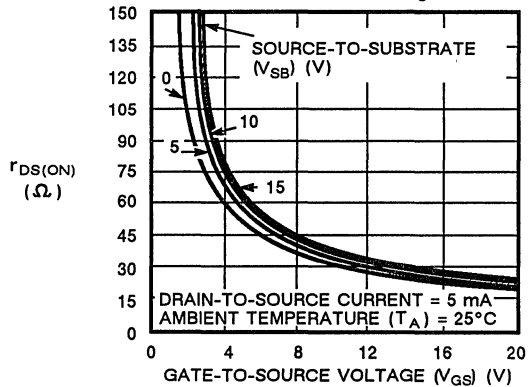
- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Refer to test conditions specified in Electrical Characteristics Tables.
- f. Derate 5 mW/°C above 25°C.

## TYPICAL CHARACTERISTICS

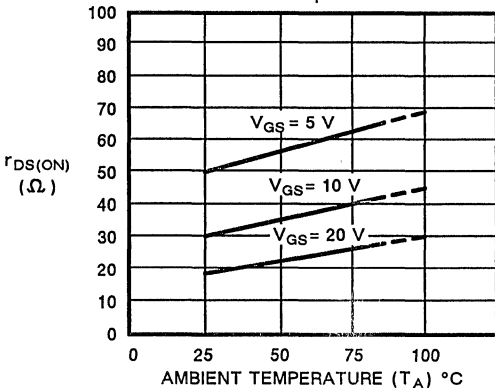
Maximum Power Dissipation vs. Temperature



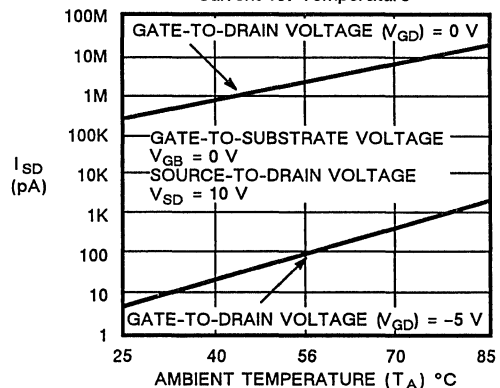
Drain-to-Source Resistance vs. Source-to-Substrate and Gate-to-Source Voltage



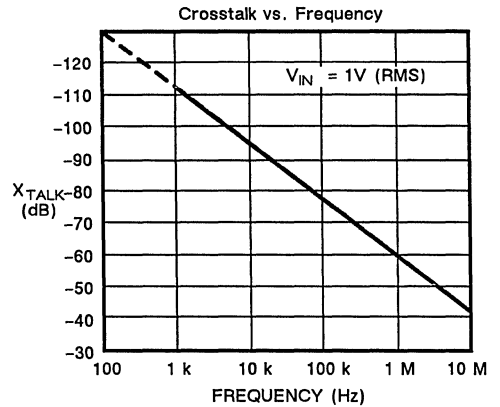
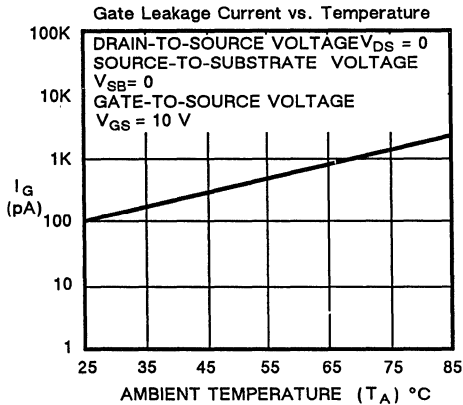
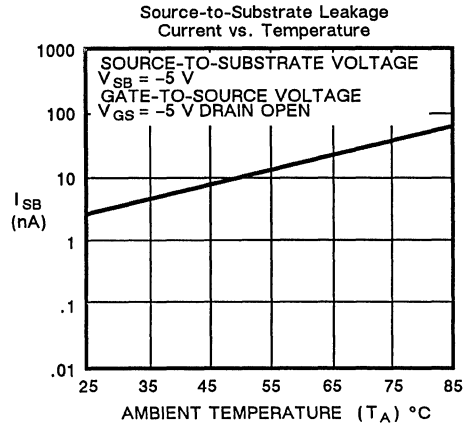
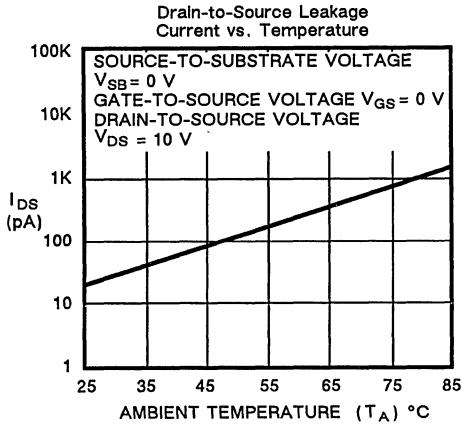
Drain-to-Source Resistance vs. Temperature



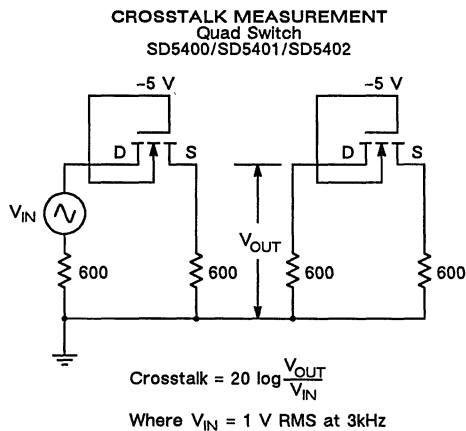
Source-to-Drain Leakage Current vs. Temperature



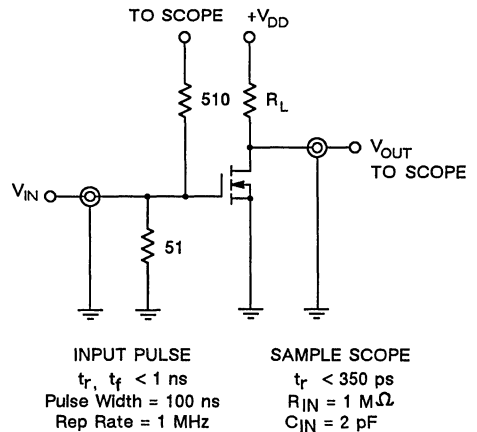
## TYPICAL CHARACTERISTICS



### TEST CIRCUIT

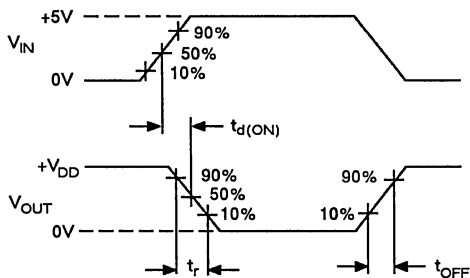


### SWITCHING TEST CIRCUIT



## SWITCHING WAVEFORMS

## SWITCHING CHARACTERISTICS

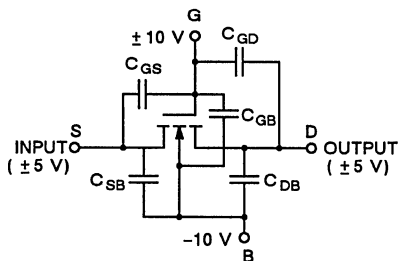


V <sub>DD</sub>	R <sub>L</sub>	t <sub>d(on)</sub> (ns)		t <sub>r</sub> (ns)		*t <sub>OFF</sub> (ns)	
		TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	
10	680	0.7		0.8		9.0	
15	1 k	0.9		1.0		14.0	

\* t<sub>OFF</sub> is dependent on R<sub>L</sub> and does not depend on the device characteristics.

## THEORY OF OPERATION

The SD5400 series consists of four SPST switches with analog signal capability of  $\pm 10$  V for the SD5400,  $\pm 5$  V for the SD5401 and  $\pm 7.5$  V for the SD5402. Each switch of the array is a DMOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally OFF when gate-to-source voltage ( $V_{GS}$ ) is 0 V. When  $V_{GS}$  exceeds the threshold voltage,  $V_T$ , the FET switch starts to turn ON. With  $V_{GS}$  in excess of +10 V, a low resistance path (typically 30  $\Omega$ ) exists between input and output of the switch. Figure 1 shows the normal mode of operation of a single switch of the array for  $\pm 5$  V analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. When analog signals are routed from one point to another the important factors are isolation, crosstalk between switches, feedthrough and feedback transients, insertion loss and speed of operation. The SD5400 series offers superior performance in all these areas (Figure 1).



Isolation. ON resistance is typically 30  $\Omega$  and OFF resistance is typically  $10^{10}$   $\Omega$ , which results in an OFF to ON resistance ratio in excess of  $10^8$ . Isolation from output to input from 3 kHz analog signals is typically -107 dB, and at 1MHz the isolation is typically 60 dB.

Feedback and feedthrough transients are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitches" are minimized, resulting in "clean" signals at the output.

Insertion loss depends upon the source and load impedances involved. As an example, for 600  $\Omega$  source impedance the insertion loss for voice signals (1 V<sub>RMS</sub> @ 3 kHz) is less than 0.3 dB. Thus the SD5400 series makes good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance, the SD5400 switches turn ON at subnanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30 dB @ 1 GHz).

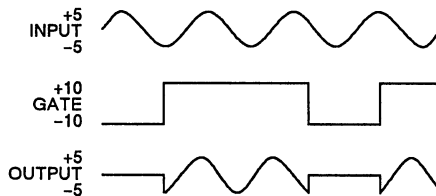


Figure 1

## APPLICATION

Figure 2 shows an SD5402 configured for operation as an audio crosspoint switch. For more detailed information on this application, see AN83-7.

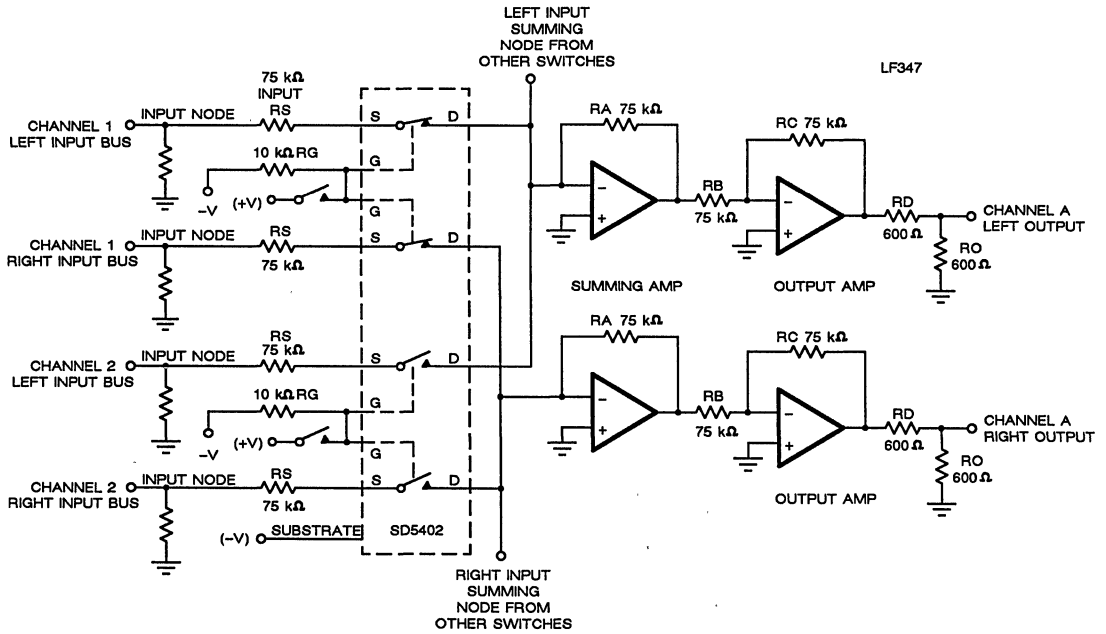


Figure 2. Audio Crosspoint Switch



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# SPECIAL FUNCTIONS

## INTRODUCTION

This section is made up of a wide variety of special functions ranging from MOSPOWER drivers, op amps, and a comparator to a ring demodulator/balanced mixer. All of these devices function as interface circuitry for various analog applications.

## DRIVERS

Large MOSFET geometries are characterized by both high threshold voltages (up to 10 V) and large gate node capacitances (up to 5000 pF). As a result, large voltage swings combined with large source and sink currents are required to charge and discharge the gate capacitance in high speed switching applications. For this reason an interface is needed to translate TTL or low voltage CMOS logic levels to drive power MOSFET switches. The D125/129/139/169/469 allow direct connection of microprocessor or logic systems to power MOSFETs for such applications as stepper motor drives, relay drivers, switch-mode power supplies, and bubble memories.

The D169 Dual High Voltage Driver features complementary outputs that can translate up to  $\pm 18$  V and handle as much as  $\pm 40$  mA. The D469 Quad High Current Power Driver is designed to drive high power MOSFET H-Bridge configurations where up to 1.5 A of peak current drive is required for signals originating from 5 volt TTL or up to 12 volt CMOS logic signal sources.

The D470 is an octal driver with a serial input logic format. The D470 translates voltages up to  $\pm 22$  V. This device is excellent for driving discrete FETs, such as 2 SD5000s, which saves board space and cost.

The Si7250 Bubble Memory Power Driver is designed to provide up to 200 mA current drive to the Siliconix VQ7250 MOSPOWER driver for driving bubble memory coil crosspoint matrix systems from TTL compatible logic signal sources.

## OPERATIONAL AMPLIFIERS

An operational amplifier is a direct-coupled high-gain device that provides controlled amounts of gain and signal shaping when used in negative feedback circuits. The L144, a micropower triple amplifier, is built on Siliconix' Bipolar-PMOS process giving low power consumption for portable and battery powered applications. The performance characteristics of the device (bias current, slew rate, and power consumption) can be tailored with a single resistor easing design considerations.

The Si7652 low-noise chopper-stabilized op amp uses an internal offset-nulling amplifier to zero out input offset voltage errors; thus, low noise, low input offset voltage, and low drift are gained for designers seeking precision.

## COMPARATORS

A comparator provides a logic level output which designates the amplitude relationship between 2 signals. The L161, a quad comparator, is built on Siliconix' Bipolar-PMOS process and developed for low power applications in pulse generators, cross-over detectors, DC to DC converters, or wherever comparator functions are required. Similar to the L144, performance characteristics (input current, slew rate, and supply current) can be set with a single resistor.

## RING DEMODULATOR/BALANCED MIXER

One of the best approaches to mix, modulate, multiply, or compare 2 RF signals is through a ring of closely matched MOSFETs. When the Si8901, a quad MOS switch configured as a ring demodulator, is used as a

balanced mixer, the close approximation to the square-law response available with MOSFETs minimizes harmonic distortion, while the essentially capacitive gates consume much less local oscillator power than other balanced mixer designs. As a multiplier, the high 1 db compression point and low noise floor allow an exceptionally wide range of signals to be processed. In a modulator configuration, the close matching of the 4 devices minimizes distortion and harmonic resonances. In any application, the use of active devices minimizes losses through the stage, and in some cases allows actual gain to be achieved.

## DEFINITION OF TERMS

### Common Mode Error Voltage (CMEV)

An operational amplifier (and differential input comparator) is designed to respond only to signals appearing between its input terminals and not to those in common with both. If the output error voltage, due to a known magnitude of common mode voltage (CMV), is referred to the input (by dividing by the closed loop gain), it reflects the equivalent input signal required to generate that output, and is thus called Common-Mode-Voltage-Error.

### Common-Mode Range (CMR)

CMR is defined as the range of common mode voltage on the input terminals for which operation within specifications is assured.

### Common-Mode Rejection Ratio (CMRR)

While CMRR is defined as the ratio of common-mode voltage (CMV) to Common Mode Error Voltage (CMEV), it is complicated by the fact that it is highly non-linear, and is also a function of frequency and temperature. Siliconix measures CMRR at DC and at the specified CMV limits, unless otherwise noted.

### DC Open Loop Voltage Gain ( $A_{VOL}$ )

Open loop gain is specified as the ratio of the change in output voltage (over a specified range) to the change in the differential input voltage producing it. As this parameter is very much frequency dependent, open loop gain is specified at DC and a typical open loop response curve is given for each type in the data sheet.

### Input Bias Current ( $I_{BIAS}$ )

Bias current is the input current required at either input terminal to drive the output to zero (assumes zero input voltage). Siliconix specifies the maximum

value at either input terminal. Variations with temperature and supply voltage are specified separately.

### Input Offset Current ( $I_{OS}$ )

Offset current is defined as the difference between the current into the two input terminals when the output is at zero volts.

### Input Offset Voltage ( $V_{OS}$ )

The input offset voltage is the DC input voltage required to provide zero voltage at the output of the amplifier when the input signal and input bias currents are at zero. The power supply and temperature dependent terms are specified separately.

### Power-Supply Rejection Ratio (PSRR)

PSRR is the inverse ratio of the change in input offset voltage to the change in power supply voltage producing it. PSRR is specified in dB or  $V/V$ .

### Response Time ( $t_r$ )

The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. Logic threshold is defined as the voltage at the output of the comparator at which the loading logic circuitry changes its digital state, or, as 1.4 V when the loading logic circuitry is not used.

### Slew Rate ( $S_r$ )

The maximum rate of change in the output voltage when supplying the rated output.

### Unity Gain (Small-Signal) Bandwidth

Defined as the frequency at which the open-loop response becomes unity. It is specified for small signals as slew rate limits the frequency at which full output voltage swing can be obtained.



# D125

## Monolithic 6-Channel FET Switch Drivers

### FEATURES

- TTL Compatible
- DC Level Shifting to > 19 V
- Fast Switching ( $t_{OFF} < 1.5 \mu s$ )

### BENEFITS

- Reduces System Component Requirements
- Fast Level Shifting

### APPLICATIONS

- Interfacing Low Level Logic to MOSFETs or JFETs

### DESCRIPTION

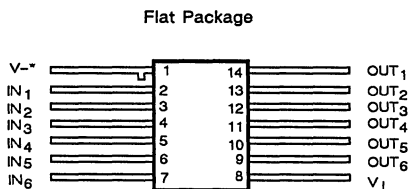
The D125 contains six drivers, designed to perform the level-shifting and amplification needed to interface low-level logic outputs and field-effect transistor switches (MOSFET or JFET). With the input logic supply, ( $V_L$ ), at 5 V, the driver output reference, ( $V_-$ ) may be set between  $-1$  and  $-25$  V. Each output is designed to sink 5 mA of current in the ON condition, and to hold off up to 30 V in the OFF condition. The input stage is a base-input PNP

transistor, with the emitter returned to the  $V_L$  supply through a resistor. To turn the driver ON, the logic stage driving it must be capable of sinking 0.7 mA.

Package options include the 14-pin side braze and flatpack packages. Performance grades include both the industrial, B suffix ( $-25$  to  $85^\circ C$ ) and military, A suffix ( $-55$  to  $125^\circ C$ ) temperature ranges.

### PIN CONFIGURATION

### FUNCTIONAL BLOCK DIAGRAM

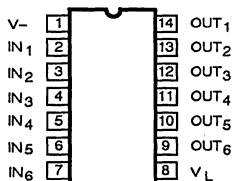


Top View

Order Numbers: D125AL/883

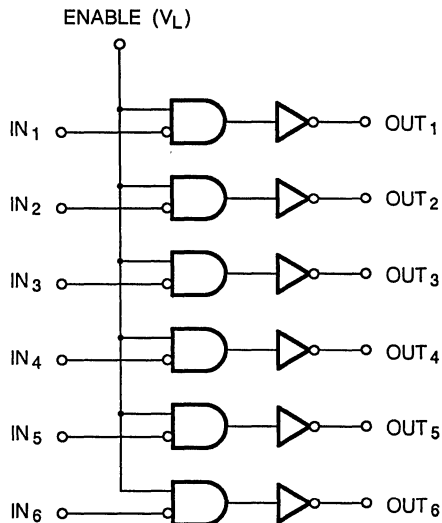
\* Common to Substate and Base of Package

Dual-In-Line Package



Top View

Order Numbers:  
D125AP, D125BP



## ABSOLUTE MAXIMUM RATINGS

$V_O$ to $V_-$ .....	36 V
$V_L$ to $V_-$ .....	30 V
$V_{IN}$ to $V_-$ .....	30 V
$V_{IN}$ to $V_L$ .....	$\pm 6$ V
Current, (Any Terminal) .....	30 mA
Storage Temperature .....	-65 to 150°C

Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C

Power dissipation\*

Flat Package** .....	750 mW
14-Pin DIP*** .....	825 mW

\* All leads soldered or welded to PC board.

\*\* Derate 10 mW/°C above 75°C.

\*\*\* Derate 11 mW/°C above 75°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_- = 20$ V $V_L = 5$ V	LIMITS								UNIT
			1=25°C 2=125,85°C 3=-55,-25°C		A SUFFIX -55 to 125°C		B SUFFIX -25 to 85°C				
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>OUTPUT</b>											
Output Voltage LOW	$V_{OL}$	$I_O = 5$ mA, $V_L = 4.5$ V $V_{IN} = 0.5$ V	1,3 2	-19.8		-19.6 -19.5		-19.6 -19.5		V	
Output Current HIGH	$I_{OH}$	$V_O = 10$ V $V_{IN} = 4.6$ V	1,3 2	0.005		0.1 10		0.1 10		$\mu$ A	
<b>INPUT</b>											
Input Current Voltage HIGH	$I_{INH}$	$V_{IN} = 4.6$ V	1,3 2	0.001	-1 -10	1 10	-1 -20	1 20		$\mu$ A	
Input Current Voltage LOW	$I_{INL}$	$V_{IN} = 0$	1,2,3	-0.15	-0.7		-1			mA	
<b>DYNAMIC</b>											
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit	1	0.11		0.5		0.5		$\mu$ s	
Turn-OFF Time	$t_{OFF}$		1	1.05		1.2		1.5			
<b>SUPPLY</b>											
Negative Supply Current	$I_-$	$V_{IN1} = 0$ All Other $V_{IN} = 4.6$ V	1,2,3	-1.5	-2.5		-2.5			mA	
Logic Supply Current	$I_L$		1,2,3	1.6		2.5		2.5			
Negative Supply Current	$I_-$	All $V_{IN} = 4.6$ V	1,3 2	-0.09	-2 -200		-2 -100			$\mu$ A	
Logic Supply Current	$I_L$		1,3 2	0.09		1 100		2 100			

NOTES:

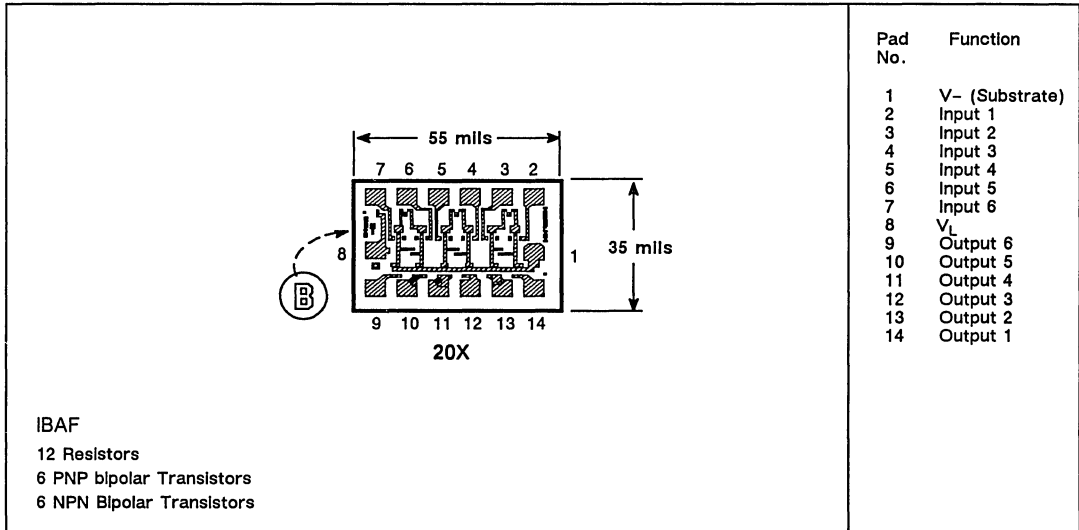
a. Refer to PROCESS OPTION FLOWCHART for additional information.

b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

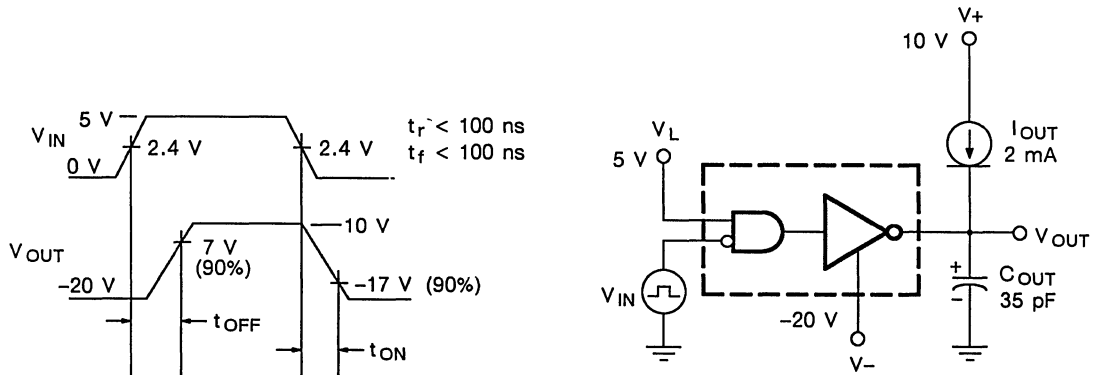
c. Guaranteed by design, not subject to production test.

d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**DIE TOPOGRAPHY**



**SWITCHING TIME TEST CIRCUIT**



## 4-Channel MOSFET Switch Driver with Decode

### FEATURES

- TTL Compatible
- 4 Independent Drivers
- Output Sink Current to 10 mA
- DC Level Shifts to >19 V

### BENEFITS

- Reduces System Component Requirements
- Fast Level Shifting

### APPLICATIONS

- Interfacing Low Level Logic to MOSFETs or JFETs
- Designed to Interface with G118 and G119

### DESCRIPTION

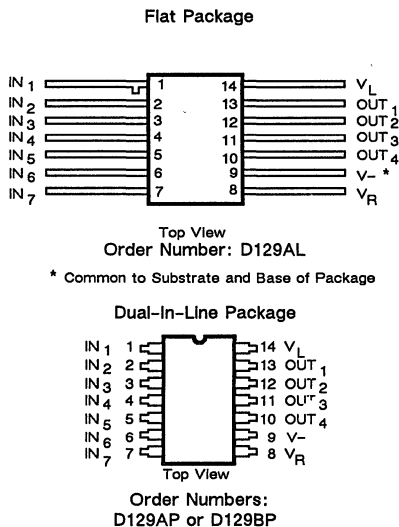
The D129 is a four-channel driver designed to provide the DC level-shifting and amplification functions needed to interface low-level logic outputs (0.7 to 2.2 V) and field-effect transistor switch inputs (up to 50 V peak-to-peak). With an input logic supply of 5 V, the output transistor emitter, ( $V_-$ ), may be set at any voltage between -5 and -30 V. In the ON state, the output collector will sink up to 10 mA of current, and in the OFF state will hold off voltages up to 50 V above  $V_-$ . Each of the four drivers has a 3-input logic gate, and the driver will be ON when each of the inputs

are either open or at positive logic "1".

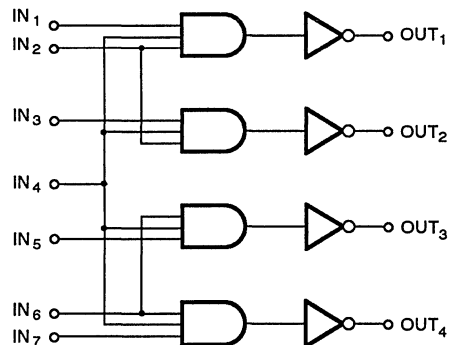
With any of the inputs either grounded or at positive logic "0", the driver will be OFF. Some of the logic inputs to the four gates are internally connected to facilitate decoding from a binary counter, however, one input to each gate provides a means for independent operation of each driver, if desired.

Package options include the 14-pin side braze and flatpack packages. Performance grades include both the industrial, B suffix (-25 to 85°C) and military, A suffix (-55 to 125°C) temperature ranges.

### PIN CONFIGURATION



### FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

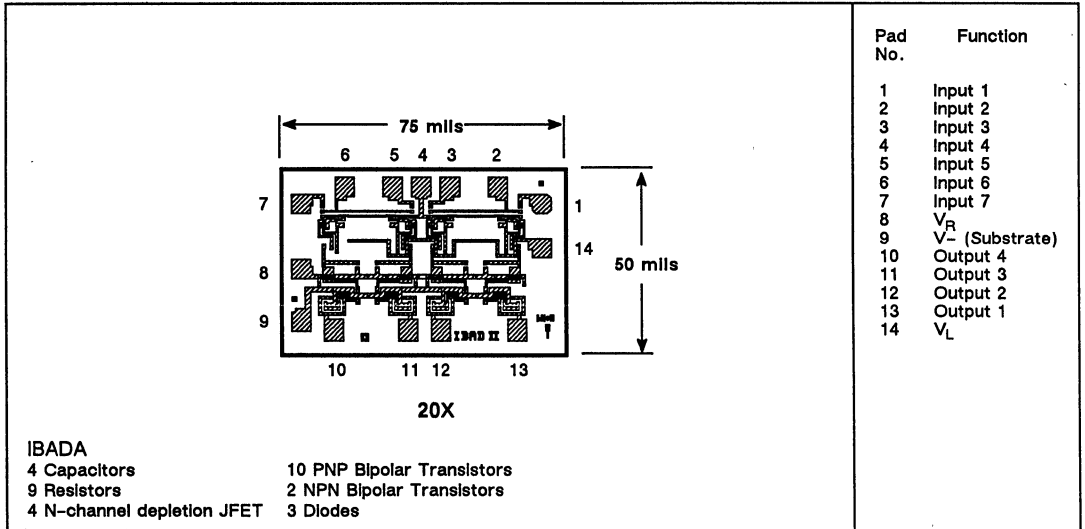
$V_O$ to $V_-$ (A Suffix) .....	50 V	Operating Temperature (A Suffix) .....	-55 to 125°C
$V_O$ to $V_-$ (B Suffix) .....	36 V	(B Suffix) .....	-25 to 85°C
$V_R$ to $V_-$ (A Suffix) .....	33 V	Power Dissipation*	
$V_R$ to $V_-$ (B Suffix) .....	24 V	Flatpack** .....	750 mW
$V_L$ to $V_R$ .....	8 V	14-Pin DIP*** .....	825 mW
$V_{IN}$ to $V_R$ .....	$\pm 6$ V	* All leads soldered or welded to PC board.	
$V_{IN}$ to $V_{IN}$ (Any Other $V_{IN}$ Terminals) .....	6 V	** Derate 10 mW/°C above 75°C.	
Current, (Any Terminal) .....	30 mA	*** Derate 11 mW/°C above 75°C.	
Storage Temperature .....	-65 to 150°C		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_L = 5$ V $V_- = -20$ V $V_R = 0$ V	LIMITS						UNIT	
			1=25°C		A SUFFIX		B SUFFIX			
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>OUTPUT</b>										
Output Voltage, LOW	$V_{OL}$	$V_{IN} = 2.2$ V $V_L = 4.5$ V	$I_{OUT} = 10$ mA	1,3 2	-19.8		-19.3 -19.0		-19.25 -19.0	V
			$I_{OUT} = 1$ mA	1	-19.75		-19.8			
Output Current, HIGH	$I_{OH}$	$V_O = 10$ V $V_{IN} = 0.7$ V		1,3 2	0.005		0.1 20		0.2 10	$\mu$ A
<b>INPUT</b>										
Input Current, Voltage HIGH	$I_{INH}$	$V_{IN} = 5$ V, Input Under Test $V_{IN} = 0$ V, All Other Inputs		1,3 2			0.25 5		1 5	$\mu$ A
Input Current, Voltage LOW	$I_{INL}$	$V_{IN} = 0$ V, $V_L = 5.5$ V		1 2 3	-0.2	-200 -160 -250		-225 -200 -250		
<b>DYNAMIC</b>										
Turn-ON Time	$t_{ON}$	See Switching Time Test Circuit ( $C_L = 35$ pF)		1	0.22		0.3		0.3	$\mu$ s
Turn-OFF Time	$t_{OFF}$			1	1.16		1.5		1.5	
<b>SUPPLY</b>										
Negative Supply Current	$I_-$	$V_- = -20$ V $V_L = 5.5$ V	One Channel ON	1	-1.5	-2		-2.25		mA
Logic Supply Current	$I_L$			1	2.2		3		3.3	
Negative Supply Current	$I_-$		All $V_{IN} = 0$ V All Channels OFF	1	-0.01	-10		-25		$\mu$ A
Logic Supply Current	$I_L$			1	0.46		0.75		1	mA

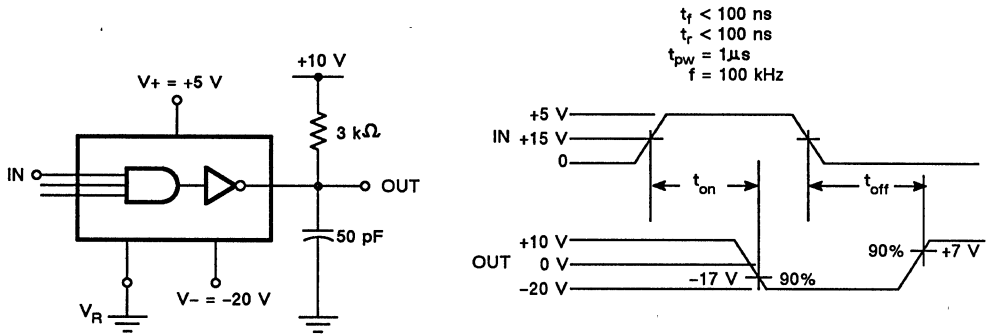
NOTES:  
a. Refer to PROCESS OPTION FLOWCHART for additional information.  
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.  
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.



## DIE TOPOGRAPHY



## SWITCHING TIME AND TEST CIRCUIT



# Monolithic 2-Channel FET Switch Driver

## FEATURES

- Complementary Outputs
- 150 ns Propagation Time
- 30 V Output Swing
- Current Source Coupling
- TTL Compatible

## BENEFITS

- Versatile
- Minimizes Switching Time
- Easily Interfaced

## APPLICATIONS

- Interfaces Low Level Signal to FET Switches
- TTL to CMOS
- TTL to PROM Logic Levels
- Double-throw Switch Control

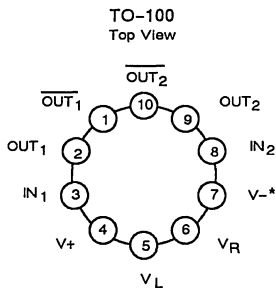
## DESCRIPTION

The D139 is a dual low level to high level voltage translator with complementary outputs. Uses include bipolar to MOS logic interface and bipolar logic to FET analog switch control. The following characteristics of the input circuit provide an ideal interface to the common logic forms TTL, CMOS, and DTL: light loading ( $\sim 1/3$  TTL load) to "0" inputs, a 1.2 V trip point, and high input impedance with high breakdown to "1" inputs. The output can drive up to 30 V peak-to-peak into pure capacitive loads or moderate resistive loads. Current source coupling between the input and output and split

power supplies allow wide flexibility in the actual output voltage levels. Complementary outputs permit maximum application versatility, allowing functions such a double-throw analog switch control. A positive logic "1" at the input provides a "1" at OUT and a "0" at  $\overline{\text{OUT}}$ .

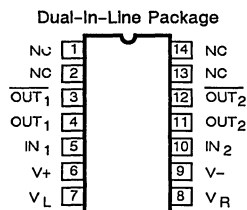
The D139 is offered in 10-pin metal can, plus 14-pin PDIP, side braze and flat pack packages. Performance grades include military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ) temperature range.

## PIN CONFIGURATION

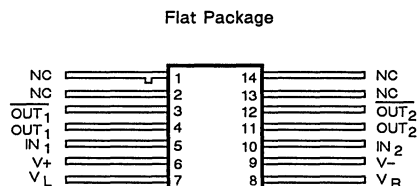


Order Number: D139AA /883

\*Common to Substrate and Case

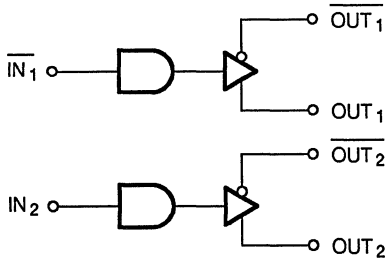


Top View  
Order Number:  
Side Braze: D139AP/883  
Plastic: D139CJ



Order Number:  
D139AL/883

## FUNCTIONAL BLOCK DIAGRAM



LOGIC	OUT	$\overline{\text{OUT}}$
0	V-	V+
1	V+	V-

Logic "0"  $\leq 0.8$  V  
 Logic "1"  $\geq 2.0$  V

## ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V	Operating Temperature (A Suffix)	-55 to 125°C
V+ to $V_R$	36 V	(C Suffix)	0 to 70°C
V+ to $V_O$	36 V	Storage Temperature (A Suffix)	-65 to 150°C
$V_L$ to $V_R$	8 V	(C Suffix)	-65 to 125°C
$V_{IN}$ to $V_R$	8 V	Power Dissipation* (L Package)**	900 mW
$V_R$ to V-	36 V	(P Package)***	825 mW
$V_L$ to V-	36 V	(A Package)****	450 mW
$V_O$ to V-	36 V	Thermal Resistance ( $\theta_{JA}$ , J Package)	0.16°C/mW
$V_L$ to $V_{IN}$	8 V	* All leads soldered or welded to PC board.	
CURRENT, (Any Terminal) DC	12 mA	** Derate 10 mW/°C above 75°C.	
Peak Current (Any Terminal)		*** Derate 11 mW/°C above 75°C.	
(200 $\mu$ s pulse width, 100 pps)	100 mA	**** Derate 6 mW/°C above 25°C.	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 10 V, $V_L$ = 5 V V- = -20 V, $V_R$ = 0 V	LIMITS						UNIT	
			1=25°C 2=125, 70°C 3=-55, 0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>OUTPUT</b>										
Output Voltage HIGH V+ to $V_O$	$V_{OH}$ , $V_{\overline{OH}}$	$V_{IH} = 2$ V for $V_{OH}$	$I_{OUT} = -10$ $\mu$ A	1 2 3	0.6		0.9 0.7 1.1		0.9 0.7 1.1	V
			$I_{OUT} = -2$ mA	1,2,3	0.82		1.5		1.5	
Output Voltage LOW $V_O$ to V-	$V_{OL}$ , $V_{\overline{OL}}$	$V_{IL} = 0.8$ for $V_{OL}$	$I_{OUT} = 10$ $\mu$ A	1 2 3	0.52		1.1 0.9 1.3		1.1 0.9 1.3	
			$I_{OUT} = 2$ mA	1,2,3			1.5		1.5	
<b>INPUT</b>										
Input Current Voltage HIGH	$I_{INH}$	$V_{IN} = 5$ V		1 2	0.003		10 20		10 20	$\mu$ A
Input Current Voltage LOW	$I_{INL}$	$V_{IN} = 0$ V		1,2 3	-18	-500 -600		-500 -600		



ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 10 V, V <sub>L</sub> = 5 V V <sub>-</sub> = -20 V, V <sub>R</sub> = 0 V	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>									
Switching Time LOW to High, Delay Plus Rise Time	t <sub>(+)</sub>	See Switching Time Test Circuit C <sub>L</sub> = 35 pF	1	65		170		170	ns
Switching Time HIGH to Low, Delay Plus Fall Time	t <sub>(-)</sub>		1	90		200		200	
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>IN</sub> = 0 or 5 V	1	0.01		0.1		0.1	mA
Logic Supply Current	I <sub>L</sub>		1	2.2		4		4	
Negative Supply Current	I <sub>-</sub>		1	-1.6	-3		-3		
Reference Supply Current Input Voltage HIGH	I <sub>RH</sub>	V <sub>IN1</sub> = V <sub>IN2</sub> = 5 V	1	-0.66	-1.6		-1.6		
Reference Supply Current Input Voltage LOW	I <sub>RL</sub>	V <sub>IN1</sub> = V <sub>IN2</sub> = 0 V	1	-0.63	-1.1		-1.1		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. All dc parameters are 100% tested at 25°C. Lots are sample-tested for ac parameters and HIGH and LOW temperature limits to assure conformance with specifications.

**DIE TOPOGRAPHY**

68 mils

43 mils

20X

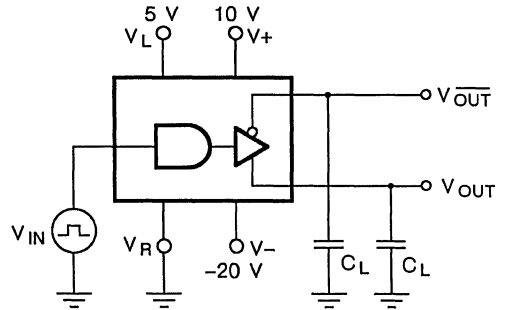
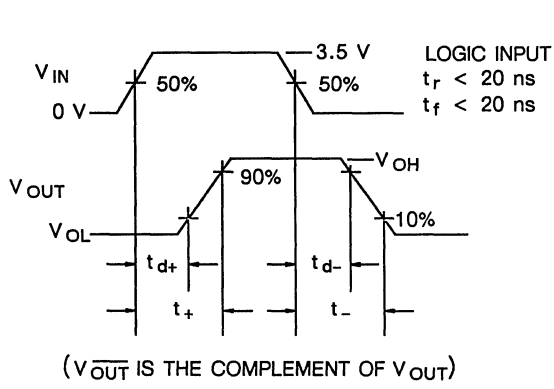
Pad No.	Function
3	Out 1
4	Out 1
5	Input 1
6	V <sub>+</sub>
7	V <sub>L</sub>
8	V <sub>R</sub>
9	V <sub>-</sub> (Substrate)
10	Input 2
11	Out 2
12	Out 2

**CMOA**

4 Diodes	4 P-channel enhancement MOSFET
4 Capacitors	10 PNP Bipolar Transistors
11 Resistors	12 NPN Bipolar Transistors



## SWITCHING TIME TEST CIRCUIT



# Dual High-Voltage Driver

## FEATURES

- 33 V Output at  $\pm 40$  mA
- Variable Input Threshold
- 70 ns Delay Time
- Complementary Outputs

## BENEFITS

- Wide Output Swing
- Logic Family Flexibility
- Fast Switching
- Drive Coupler H Bridge Power Circuit

## APPLICATIONS

- Analog Multiplexing
- Interface Logic to MOS Power
- Logic Level Translation
- Driver for PIN Diodes and FET Switches
- Line Driver

## DESCRIPTION

The D169 is a versatile high-voltage dual driver designed with complementary outputs making it excellent for driving capacitive loads. By combining a wide output voltage swing (33 V) with fast switching (100 ns delay) make this device well suited for driving power MOSFET configurations.

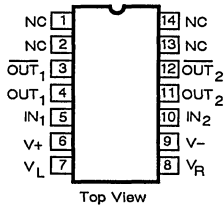
A differential input stage with adjustable threshold provides high input impedance and easy interfacing to low level logic or analog inputs. Current-source coupling to the output stage allows flexibility in output voltage levels, while the complementary emitter-follower outputs can source and sink currents of up to  $\pm 40$  mA. Each channel of the D169 has 2 separate outputs that are complemen-

tary ( $\overline{\text{OUT}}$  and  $\text{OUT}$ ) allowing easier driving of MOSPOWER devices. The output can be operated by single or split supplies.

The D169 is especially adept in driving capacitive loads such as power MOSFETS, long cables, timing capacitors, and PIN diodes. Analog multiplexing is simplified by the wide range of interface logic levels accepted, and wide output voltage swing.

Packaging for this device includes 14-pin side-braze, CerDIP, and plastic DIP options. Performance grades include military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ) temperature ranges.

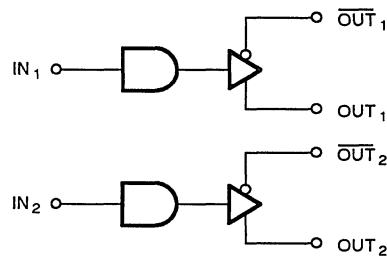
## PIN CONFIGURATION



### Order Numbers:

Slide Braze: D169AP, D169AP/883  
CerDIP: D169AK, D169AK/883  
Plastic: D169CJ

## FUNCTIONAL BLOCK DIAGRAM



LOGIC	OUT	$\overline{\text{OUT}}$
0	V-	V+
1	V+	V-

Logic "0"  $\leq 0.8$  V

Logic "1"  $\geq 2.0$  V

## ABSOLUTE MAXIMUM RATINGS

V <sub>+</sub> to V <sub>-</sub> , V <sub>+</sub> to V <sub>R</sub> , V <sub>+</sub> to V <sub>O</sub> .....	36 V
V <sub>L</sub> to V <sub>R</sub> , V <sub>IN</sub> to V <sub>R</sub> , and V <sub>L</sub> to V <sub>IN</sub> .....	10 V
V <sub>R</sub> to V <sub>-</sub> , V <sub>L</sub> to V <sub>-</sub> , and V <sub>O</sub> to V <sub>-</sub> .....	36 V
Current (Any Terminal) DC .....	40 mA
Peak (Pulsed 1 ms, 10% Duty Cycle) .....	150 mA
Operating Temperature (A Suffix) .....	-55 to 125°C
(C Suffix) .....	0 to 70°C
Storage Temperature (A Suffix) .....	-65 to 150°C
(C Suffix) .....	-65 to 125°C

Power Dissipation*	
14-Pin Side braze DIP** .....	825 mW
14-Pin CerDIP*** .....	825 mW
14-Pin Plastic DIP**** .....	470 mW

Thermal Resistance (θ<sub>JA</sub>, J Package) .... 0.16°C /mW

- \* All leads soldered or welded to PC board.
- \*\* Derate 11 mW/°C above 75°C.
- \*\*\* Derate 11 mW/°C above 75°C.
- \*\*\*\* Derate 6.5 mW /°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>											
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>L</sub> = 5 V V <sub>-</sub> = -15 V, V <sub>R</sub> = 0 V	LIMITS						UNIT		
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 TO 70°C				
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>OUTPUT</b>											
Output Voltage HIGH (V <sub>+</sub> to V <sub>O</sub> )	V <sub>OH</sub> /V <sub>OH</sub>	V <sub>IH</sub> = 2.0 V or V <sub>IL</sub> = 0.8	I <sub>OUT</sub> = 1 mA	1,2 3	0.7		1 1.1		1 1.1	V	
			I <sub>OUT</sub> = 40 mA	1,3 2	1.5		2.5 3.1		2.5 3.1		
Output Voltage LOW (V <sub>O</sub> to V <sub>-</sub> )	V <sub>OL</sub> /V <sub>OL</sub>		I <sub>OUT</sub> = 1 mA	1,2,3	-0.75	-1.2		-1.2			
			I <sub>OUT</sub> = 40 mA	1,3 2	-2.2	-3 -4		-3 -4			
<b>INPUT</b>											
Input Current Voltage HIGH	I <sub>INH</sub>	V <sub>IN</sub> = 3 V		1 2	1		5 5000		5 5000	nA	
Input Current Voltage LOW	I <sub>INL</sub>	V <sub>IN</sub> = 0 V		1,2 3	-25	-50 -100		-50 -100		μA	
<b>DYNAMIC</b>											
Switching Time Low to High, Delay Plus Rise Time	t <sup>(+)</sup>	See Switching Time Test Circuit (C <sub>L</sub> = 35 pF)		1	80		170		170	ns	
Switching Time High to Low, Delay Plus Fall Time	t <sup>(-)</sup>			1	90		200		200		

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 15\text{ V}$ , $V_L = 5\text{ V}$ $V_- = -15\text{ V}$ , $V_R = 0\text{ V}$	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 TO 70°C		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SUPPLY</b>									
Switching Crossover Level	$V_{XO}$	$C_L = 200\text{ pF}$	1	0.9					V
Positive Supply Current	$I_+$	$V_{IN1} = V_{IN2} = 0\text{ V}$ No Load	1			0.1		0.1	mA
Logic Supply Current	$I_L$		1	3.2		4		4	
Negative Supply Current	$I_-$		1	-2.2	-3.0		-3.0		
Reference Supply Current	$I_R$		1	1.0		1.5		1.5	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**DIE TOPOGRAPHY**

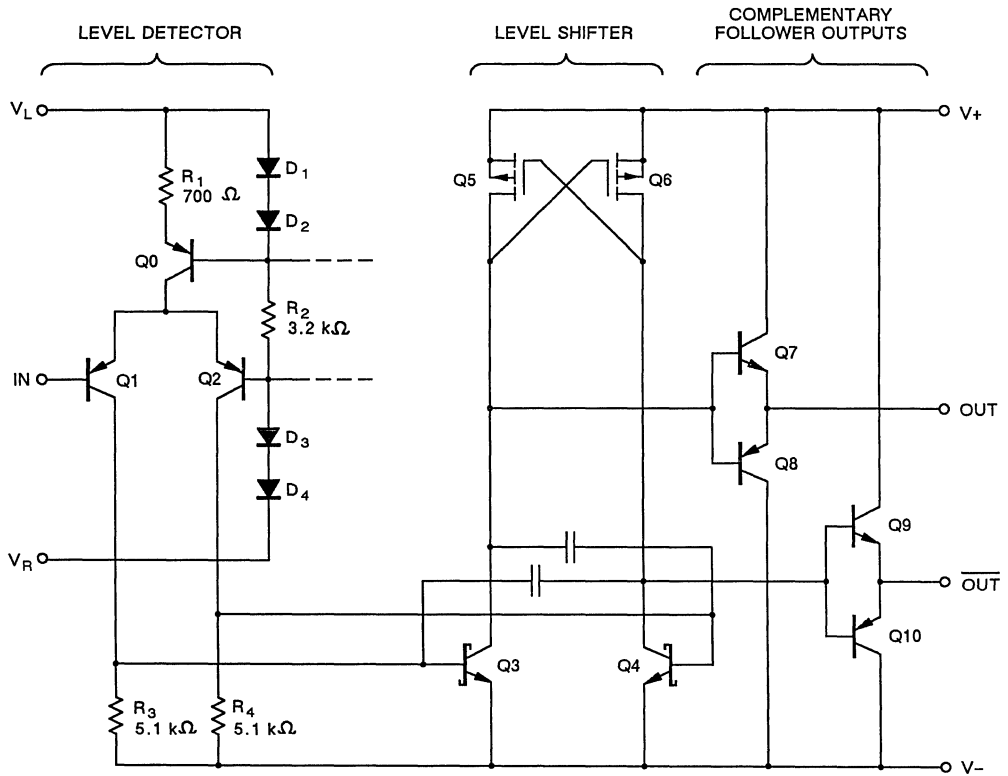
**20X**

Pad No.	Function
3	$\overline{\text{OUT}}_1$
4	$\text{OUT}_1$
5	$\text{IN}_1$
6	$V_+$
7	$V_L$
8	$V_R$
9	$V_-$ (Substrate)
10	$\text{IN}_2$
11	$\text{OUT}_2$
12	$\text{OUT}_2$

**CMOB**

4 Diodes	4 P-Channel Enhancement MOSFETs
4 Capacitors	10 PNP Bipolar Transistors
7 Resistors	8 NPN Bipolar Transistors

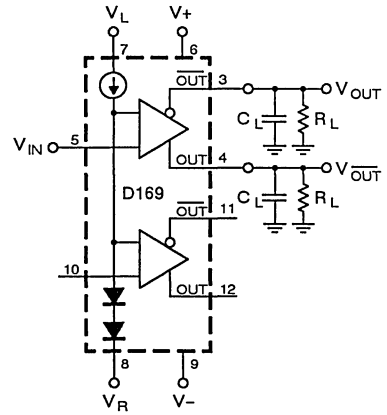
## SCHEMATIC DIAGRAM (One Channel)



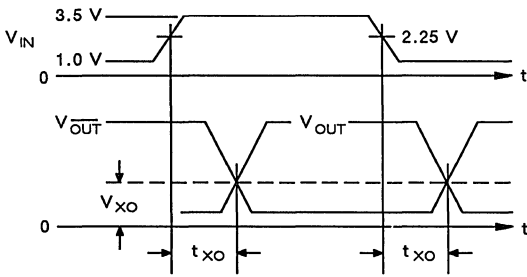
**SWITCHING TIME TEST CIRCUITS**

TEST #	V <sub>L</sub>	V <sub>R</sub>	V <sub>+</sub>	V <sub>-</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>IN</sub>		WAVE-FORMS
							V <sub>IL</sub>	V <sub>IH</sub>	
1	5 V	0.7 V	10 V	0	200 pF	-	1 V	3.5 V	A
2	5 V	0.7 V	15 V	0	0	510 Ω	1 V	3.5 V	B
3	5 V	0.7 V	10 V	0	200 pF	-	1 V	3.5 V	B
4	5 V	0.7 V	10 V	0	1000 pF	-	1 V	3.5 V	B
5	5 V	0	15 V	-15 V	200 pF	-	0	3.5 V	B
6	5 V	0	15 V	-15 V	1000 pF	-	0	3.5 V	B

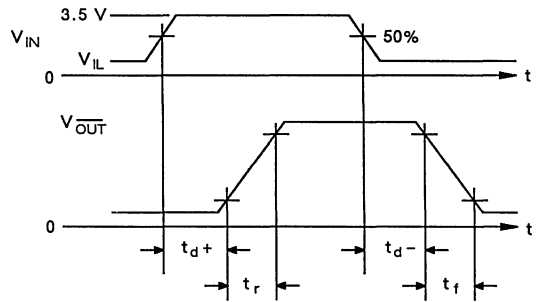
Test Conditions



Test Circuit



Waveforms A



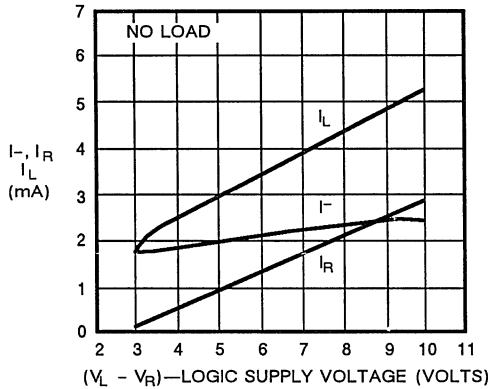
Waveforms B

Parameter	Test 2	Tests 5 & 6		Tests 3 & 4		Units
	Resistive I <sub>O</sub> = 25 mA	V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V		V <sub>+</sub> = 15 V, V <sub>-</sub> = 0 V		
		Capacitive Load		Capacitive Load		
		200 pF	1000 pF	200 pF	1000 pF	
Low-to-High Delay Time, t <sub>D+</sub>	70	95	220	110	230	ns
Rise Time, t <sub>R+</sub>	35	60	240	55	200	ns
High-to-Low Delay Time, t <sub>D-</sub>	50	50	80	55	80	ns
Fall Time, t <sub>F-</sub>	25	110	400	80	275	ns

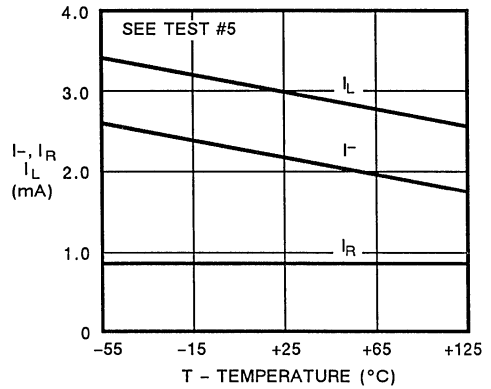
Typical Switching Times

## TYPICAL CHARACTERISTICS

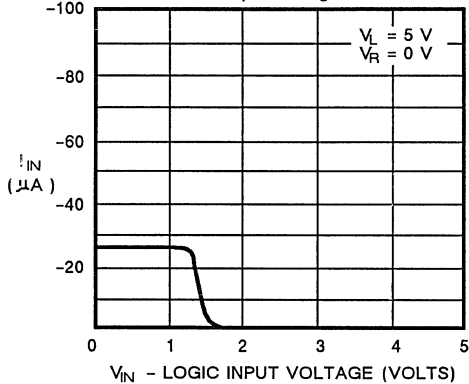
Supply Current Variation with Logic Supply



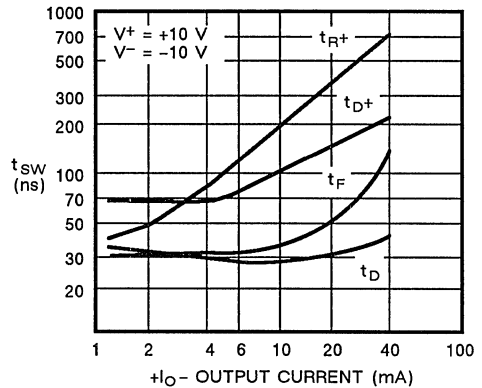
Effect of Temperature on Supply Currents



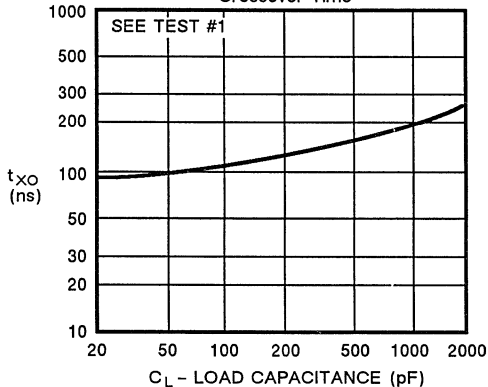
Logic Input Current vs. Logic Input Voltage



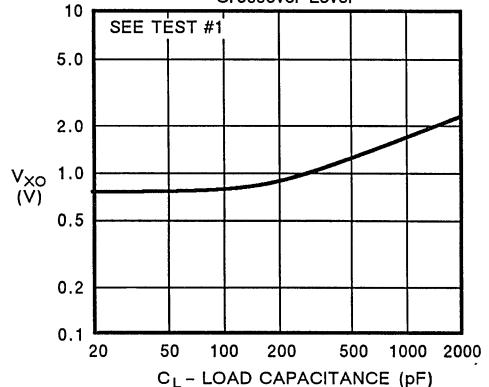
Switching Times with Resistive Load



Effect of Load Capacitance on Crossover Time

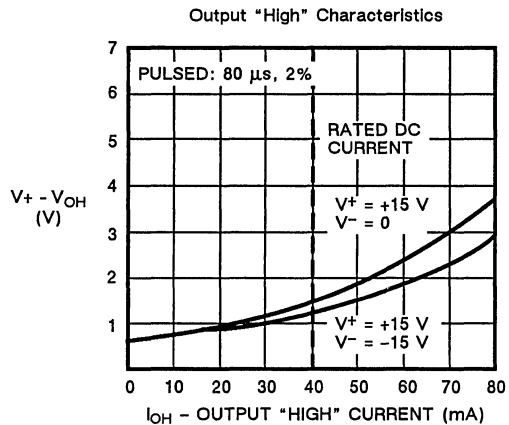
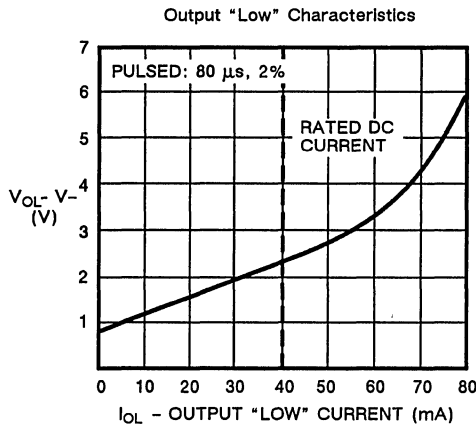
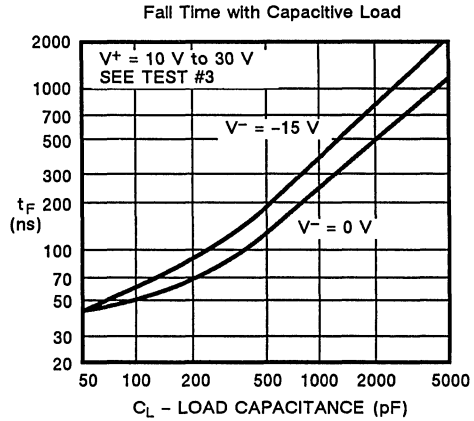
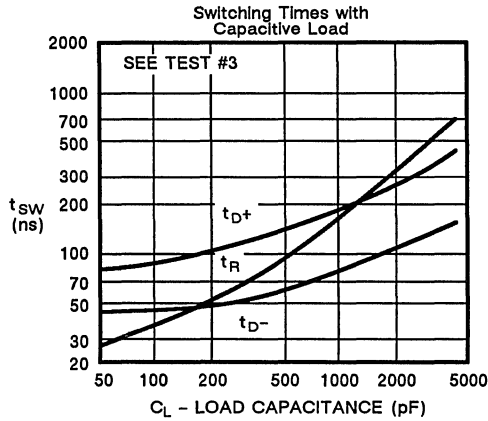
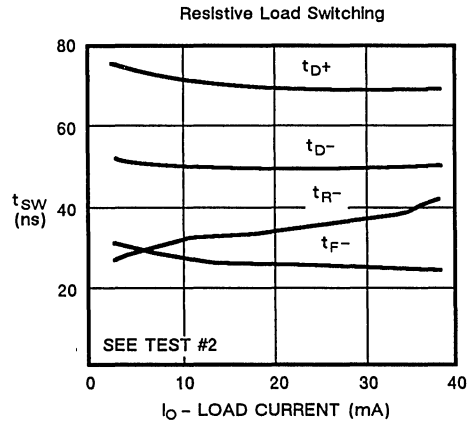
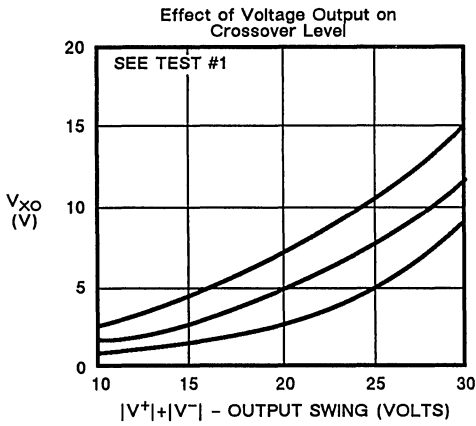


Effect of Load Capacitance on Crossover Level

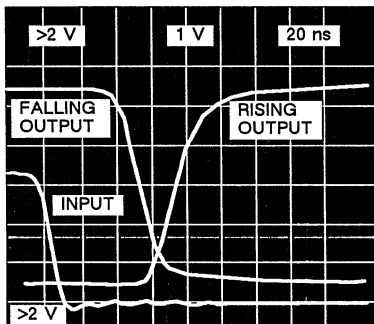




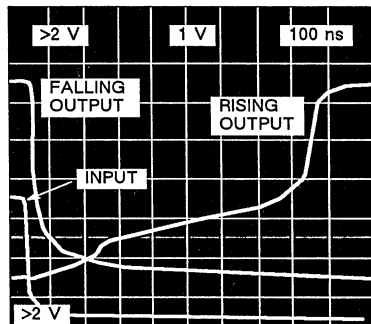
**TYPICAL CHARACTERISTICS**



## OPERATING GUIDELINES



40 mA LOAD,  $V_+ = 20\text{ V}$ ,  $V_- = 0\text{ V}$   
Switching Waveform



+40 mA LOAD,  $V_+ = 10\text{ V}$ ,  $V_- = -10\text{ V}$   
Switching Waveform

For proper performance of the D169 circuit, certain guidelines must be followed for the power supply and input terminals. These are listed below.

TERMINAL	ALLOWABLE CONDITIONS
$V_+$ (Pin 6) $V_-$ (Pin 9)	Any positive voltage Any negative voltage or zero volts
$V_R$ (Pin 8)	$\geq V_{EE} + 1\text{ V}$ (Input Threshold = $V_R + 1.4\text{ V}$ )
$V_L$ (Pin 7)	$V_L - V_R \geq 4\text{ V}$
IN1L, IN2L (Pins 5, 10)	$\geq V_{EE} + 1\text{ V}$
IN1H, IN2H (Pins 5, 10)	$\geq V_{EE} + 3\text{ V}$

## CIRCUIT OPERATION

The D169 circuit has three sections: (1) an input level detector, (2) a level shifter, and (3) a pair of complementary emitter-follower outputs. This arrangement provides a high input impedance, high output drive capability, and compatibility with a wide range of power supply levels. The input threshold level can be easily varied to accept various logic levels. Output swing is set by the  $V_+$  and  $V_-$  power supply levels.

### Level Detector

Transistors  $Q_1$  and  $Q_2$  form a differential input pair. Transistor  $Q_0$ , resistor  $R_1$ , and diodes  $D_1$  and  $D_2$  form a current source of about 1 mA which drives

the common emitter connection. The voltage between supply levels  $V_L$  and  $V_R$  determines the trip point where the circuit changes state. With  $V_R$  grounded, the trip point is about 1.4 volts, depending somewhat on the voltage  $V_L$ . The input characteristics are shown in Figure 5.

### Level Shifter

Schottky-clamped transistors  $Q_3$  and  $Q_4$  along with P-channel MOSFETs  $Q_5$  and  $Q_6$  form a complementary-coupled switching stage. This configuration draws no idle current and permits a change of state within 100 ns after the input signal passes the trip point. The circuit delays are such that the

**CIRCUIT OPERATION (Cont'd)**

that the switching action approaches a "break-before-make" sequence as shown in Figure 15. The response times are essentially independent of the input signal level and rise time.

The time measured from the input signal step to where the output waveforms from OUT and  $\overline{\text{OUT}}$  cross is called cross-over time. The voltage level at that time with respect to  $V_-$  is called crossover voltage. This point is of importance when driving certain loads where a break-before-make action is necessary to avoid high current surges. The crossover time is essentially independent of output voltage swing, but is affected by the load capacitance as shown in Figure 7. The delay time of the negative going waveform from OUT and  $\overline{\text{OUT}}$  is not

significantly affected by load capacitance; however the delay time of the positive going waveform experiences a delay which is fairly sensitive to load capacitance. This feature reduces the dependence of crossover voltage on the load capacitance as shown in Figure 8. However, the output voltage swing does exert considerable influence upon crossover level as indicated in Figure 9.

In order to provide adequate drive to  $Q_3$  and  $Q_4$ , the voltage at the collector of the differential pair must be more positive than the  $V_-$  level plus the base emitter drop of the schottky transistors. This dictates that the "low" level of  $V_{IN}$  should exceed  $V_-$  by at least one volt.

**APPLICATIONS**

**Totem-Pole Driver with Bootstrapping**

When driving MOSPOWER in a totem-pole output configuration (see Figure 17), it is necessary to have the gate voltage 10 to 15 volts positive with respect to the source in order to handle load currents near the MOSPOWER maximum ratings. The D169 lends itself to bootstrapping because of its high voltage ratings.

In the circuit shown, the voltage on the 2000 pF bootstrap capacitors is applied via diode "OR" gates to the  $V_+$  terminal; therefore, regardless of which output is high, 30 V is present at  $V_+$ . Maximum switching frequency is determined by the input capacitance of the MOSPOWER transistors used.

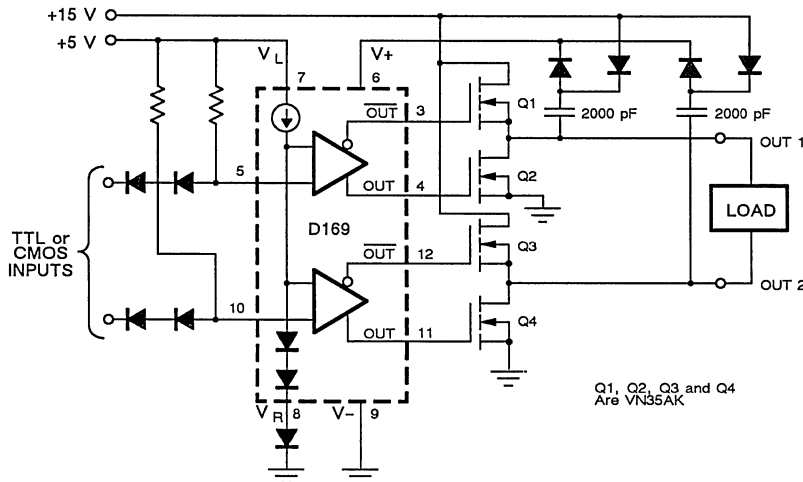


Figure 17. Totem-Pole Driver with Bootstrapping

## APPLICATIONS (Cont'd)

### Voltage-to-Frequency Converter

A simple, low-cost VFC can be designed using the D169 and a single op amp (see figure 18). The D169 serves as a level detector and provides complementary outputs. The op amp is used to integrate the input signal  $V_{IN}$  with a time constant of  $R_1C_1$ . The input, which must be negative, causes a positive ramp at the output of the integrator which is then summed with a negative zener voltage. When the ramp is positive enough to cause the D169 input (pin 10) to exceed the logic threshold of 1.4 V, then the D169 outputs change state and

OUT 2 flips from negative to positive. This positive output of approximately 11 V puts transistor  $Q_1$  into saturation which then resets the integrator to near zero. The integrator peak differential voltage  $\Delta V$  will be approximately 9.2 V. The output frequency  $f_O$ , neglecting the short reset interval, will be

$$f_O = \frac{1}{R_1 C_1 \Delta V} V_{IN}, V_{IN} < 0$$

The pulse repetition rate,  $f_O$ , is directly proportional to the negative input voltage  $V_{IN}$ .

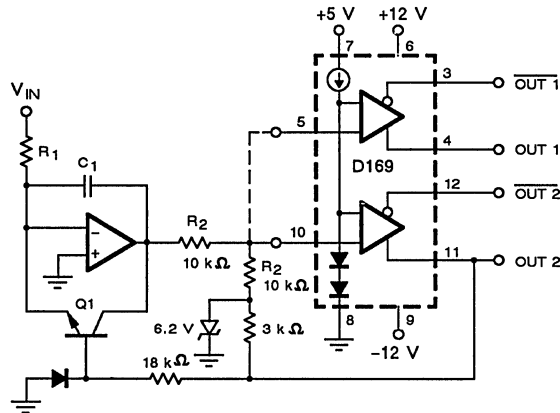


Figure 18. D169 Used as a Voltage-to-Frequency Converter

### H-BRIDGE SWITCH APPLICATION

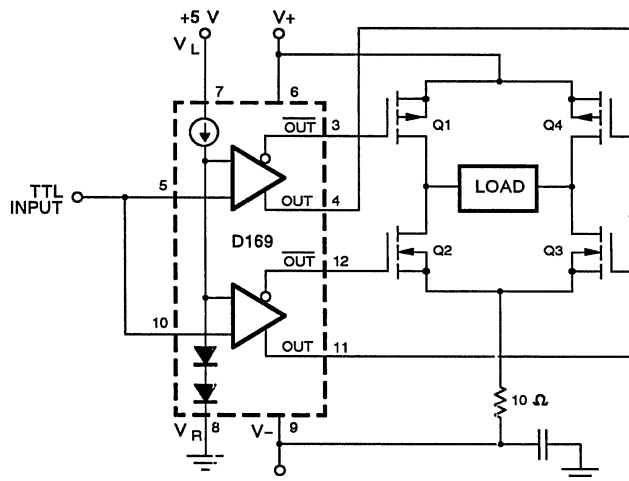


Figure 19. Driver for MOSPOWER H-Switch

# D469

## Quad High-Current Power Driver

### FEATURES

- High Current Drive (Up to 1A)
- Single Power-Supply
- TTL/CMOS Compatible Inputs

### BENEFITS

- Efficient Drive For Large MOSPOWER FETs
- Low Standby Power Consumption
- Easily Interfaced

### APPLICATIONS

- H-Bridge Drives
- Motor Drives
- Complementary Switching

### DESCRIPTION

The D469 is a quad high current driver designed to interface low current logic to power MOSFETs in motor controls and other power control applications. This 4-channel power driver can source or sink up to 1 A at 2% duty cycles or  $\pm 250$  mA continuously.

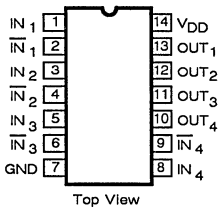
To achieve high current driving capability, the D469

is built on the Siliconix PolyMOS™ process. An epitaxial layer prevents latchup.

The D469 is available in 14-pin side braze and plastic packages. Performance grades include the military, A suffix (-55 to 125°C), industrial, B suffix (-25 to 85°C), and commercial, C suffix (0 to 70°C) temperature ranges. For further information please refer to application note AN88-1.

### PIN CONFIGURATION

Dual-In-Line Package

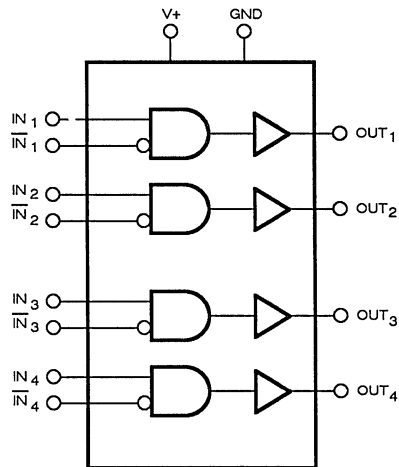


Order Numbers:  
Side Braze: D469AP, D469AP/883,  
D469BP  
Plastic: D469CJ

Truth Table

IN <sub>x</sub>	$\overline{\text{IN}}_x$	OUT <sub>x</sub>
0	0	GND
0	1	GND
1	0	V <sub>DD</sub>
1	1	GND

### FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

	P Package	J Package
Ambient Temperature Under Bias .....	-55 to 125°C	Operating Temperature .. -55 to 125°C .....
Storage Temperature .....	-65 to 150°C	0 to 70°C
Voltage on Any Pin with Respect to Ground .....	-0.3 to $V_{DD} + 0.3$ V	Junction Temperature .....
Supply Voltage, $V_{DD}$ .....	-0.3 to 14 V	150°C .....
Continuous Output Current .....	$\pm 250$ mA	125°C
Peak Output Current (Pulsed at 1 ms, 2% Duty Cycle) .....	$\pm 1$ A	Power Dissipation .....
		825 mW .....
		625 mW
		Derating .....
		11 mW/°C ... 6.25 mW/°C
		above 75°C ... above 25°C
		$\theta_{JA}$ .....
		91°C/W .....
		160°C/W
		(No Airflow) .... (No Airflow)

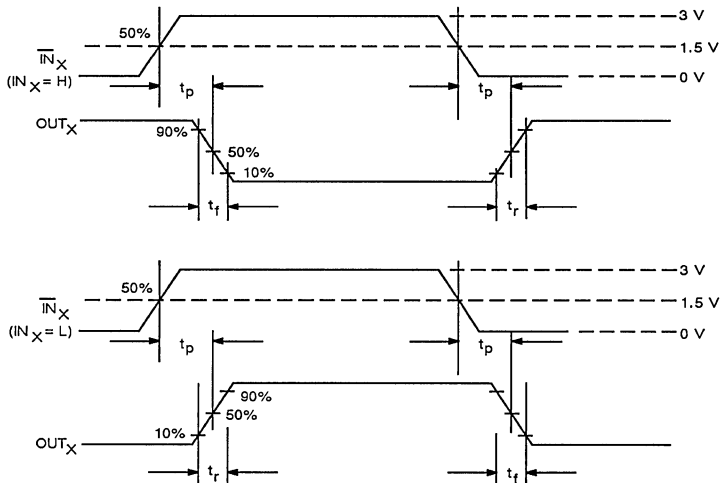
ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_{DD} = 12$ V	LIMITS				UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A, B, C SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>							
Input Voltage HIGH	$V_{INH}$		1, 2, 3		3		V
Input Voltage LOW	$V_{INL}$		1, 2, 3			0.8	
Input Current with Input Voltage HIGH	$I_{INH}$	$V_{IN} = V_{DD}$	1, 2	0.001		10	$\mu$ A
Input Current with Input Voltage LOW	$I_{INL}$	$V_{IN} = 0$ V	1, 2	0.001	-10		
<b>OUTPUT</b>							
Output Voltage HIGH	$V_{OUTH}$	$I_{OUT} = -100$ mA One Output at a Time	1, 2, 3	11.1	10		V
		$I_{OUT} = -10$ mA	1, 2, 3	11.9	11.8		
Output Voltage LOW	$V_{OUTL}$	$I_{OUT} = 100$ mA One Output at a Time	1, 2, 3	0.6		2	
		$I_{OUT} = 10$ mA	1, 2, 3	0.07		0.2	
Output Source Current	$I_{OS+}$	$V_O = 0$ V, 2% Duty Cycle	1	1			A
Output Sink Current	$I_{OS-}$	$V_O = 12$ V, 2% Duty Cycle	1	-1			

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_{DD} = 12\text{ V}$	LIMITS				UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A,B,C SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC</b>							
Propagation Delay	$t_{px}$	$C_L = 500\text{ pF}$	1	60		100	ns
Rise Time	$t_r$		2			150	
Fall Time	$t_f$		1	25			
Input Capacitance	$C_{in}$		1	5			pF
<b>SUPPLY</b>							
Supply Current	$I_{DD}$	$I_{N_X} = \bar{I}_{N_X} = 0\text{ V}, V_{DD} = 12.6\text{ V}$	1 2	3		7.5 10	mA
		$I_{N_X} = \bar{I}_{N_X} = 3\text{ V}, V_{DD} = 12.6\text{ V}$	1,2 3	10		20 30	
		$f = 100\text{ kHz}, V_{DD} = 12.6\text{ V}$ $C_L = 500\text{ pF}$ One Output at a Time	1 2	7		20 20	

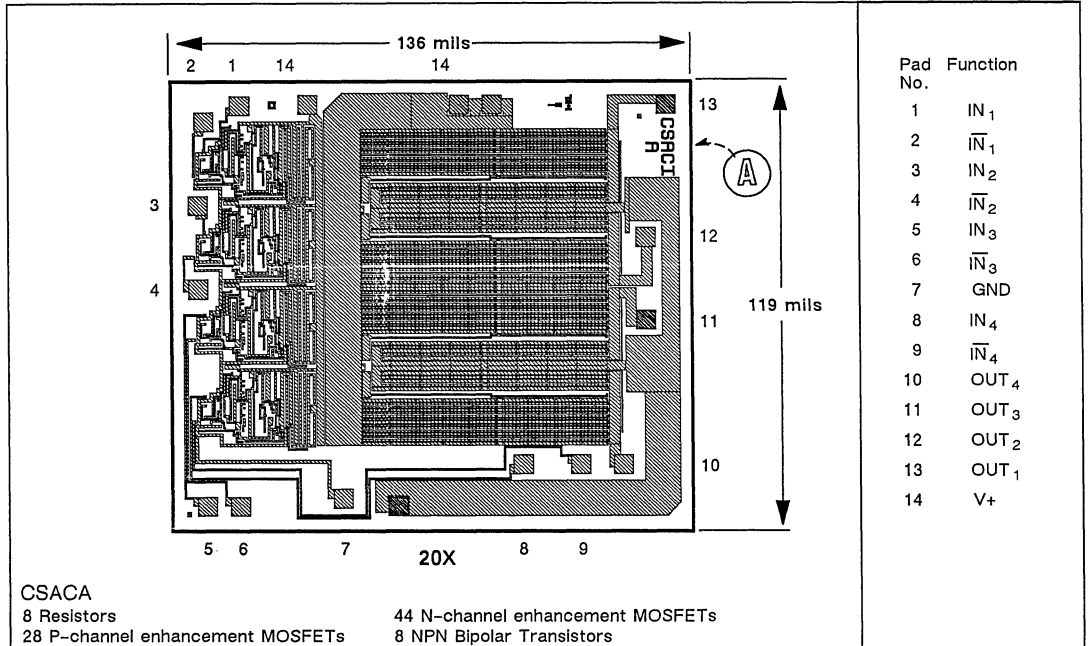
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

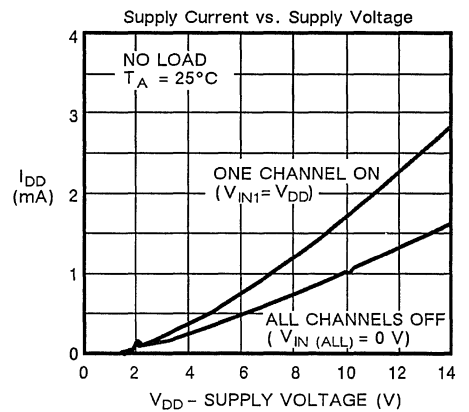
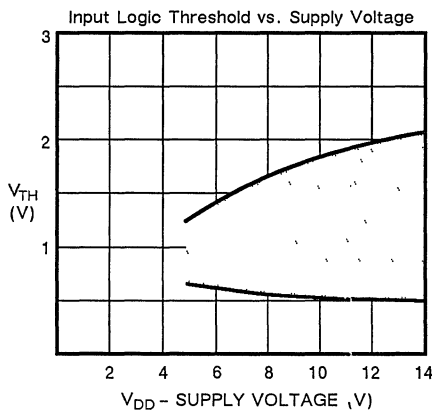
**AC TESTING CONDITIONS**



## DIE TOPOGRAPHY

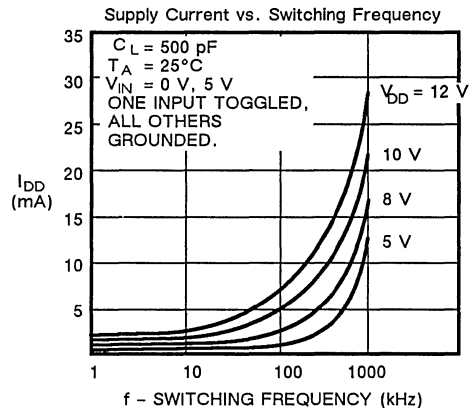
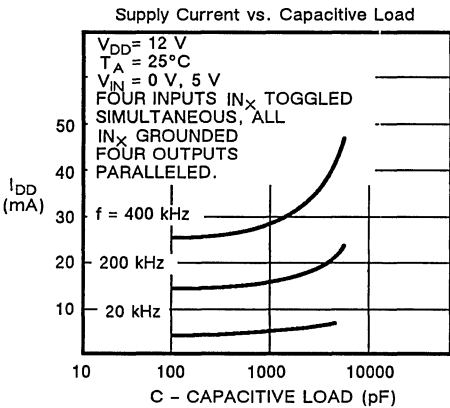
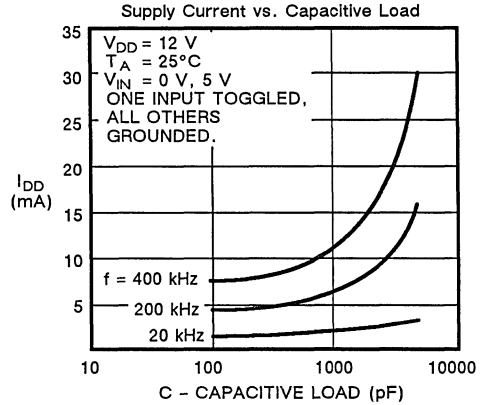
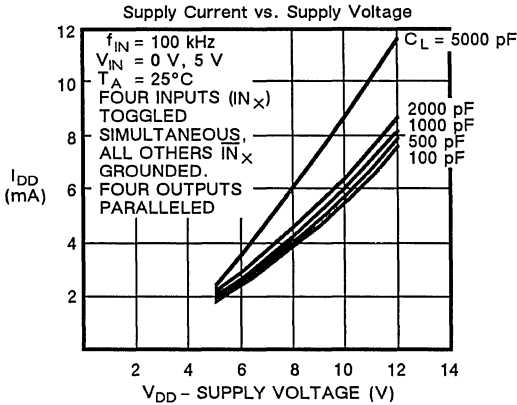
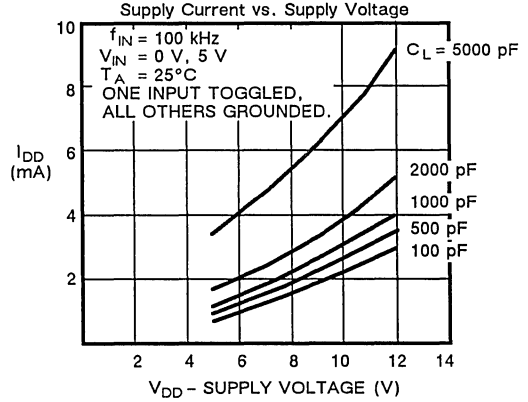
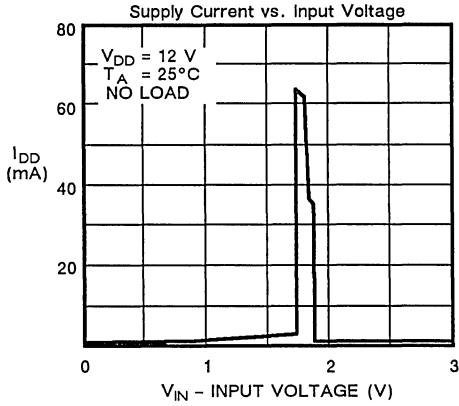


## TYPICAL CHARACTERISTICS

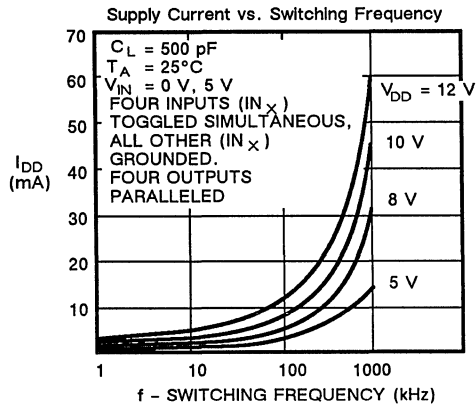




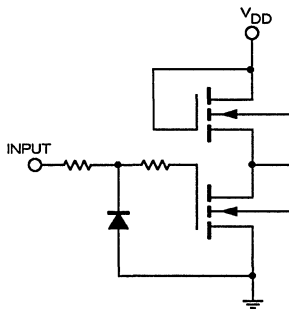
**TYPICAL CHARACTERISTICS (Cont'd)**



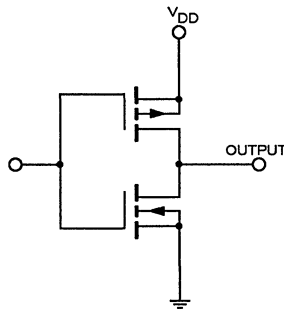
## TYPICAL CHARACTERISTICS (Cont'd)



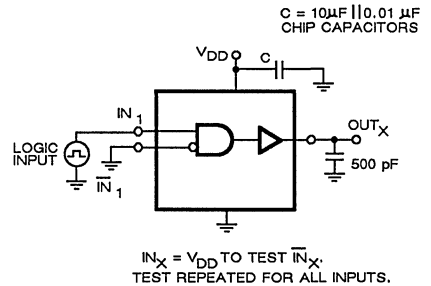
### INPUT STRUCTURE



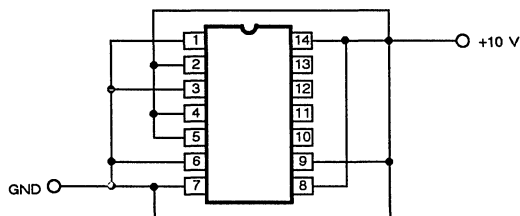
### OUTPUT STRUCTURE



### SWITCHING TIME TEST CIRCUIT



### BURN-IN DIAGRAM



### PIN DESCRIPTION

SYMBOL	DESCRIPTION
$IN_X$	Non-Inverting Logic Control Input
$\overline{IN}_X$	Inverting Logic Control Input
GND	Ground
OUT	Buffered Output
$V_{DD}$	Positive Supply Voltage

# Low-Power – High-Speed Octal CMOS Driver with Serial Interface

## FEATURES

- Up to  $\pm 22$  Volt Output Range
- Low Propagation Delays (< 200 ns)
- Any combination of 8 Outputs
- TTL and CMOS Compatible
- Independent Output Voltages
- ESDS Protection >  $\pm 4000$  V

## BENEFITS

- Devices Can Be Chained For System Expansion
- Master Reset To All Drivers
- Simple Interfacing
- Reduced Parts Count
- Increased Versatility

## APPLICATIONS

- Automotive and Avionics Systems
- ATE
- Serial Data Acquisition and Process control
- Communication Systems
- Display Drivers

## DESCRIPTION

The D470 is a CMOS driver array configured as eight power buffers for use in serial input applications. By combining high output current capability ( $I_{OPEAK} = 200$  mA) and low propagation delays ( $t_{PR} < 150$  ns) the D470 is ideally suited for driving discrete devices in automotive, ATE, and process control applications.

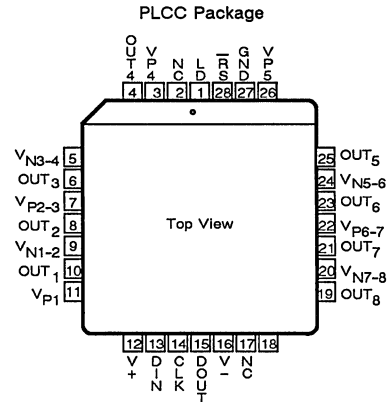
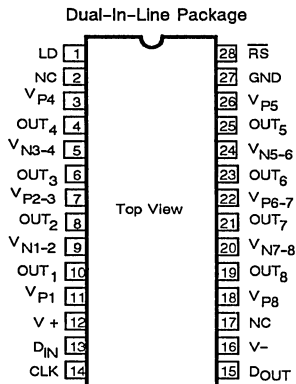
This device loads data serially into the input shift register with each clock pulse. The state of the shift register can be latched via LOAD (LD) at any point into an address register which holds the logic bits to control each individual driver. A  $\overline{RS}$  pin resets all the latches which in turn reset the power buffers. A

serial data output terminal  $D_{OUT}$  allows chaining of power drivers for larger matrix systems. The output voltages may be made independent or equal to  $V_+$  and  $V_-$  for added flexibility.

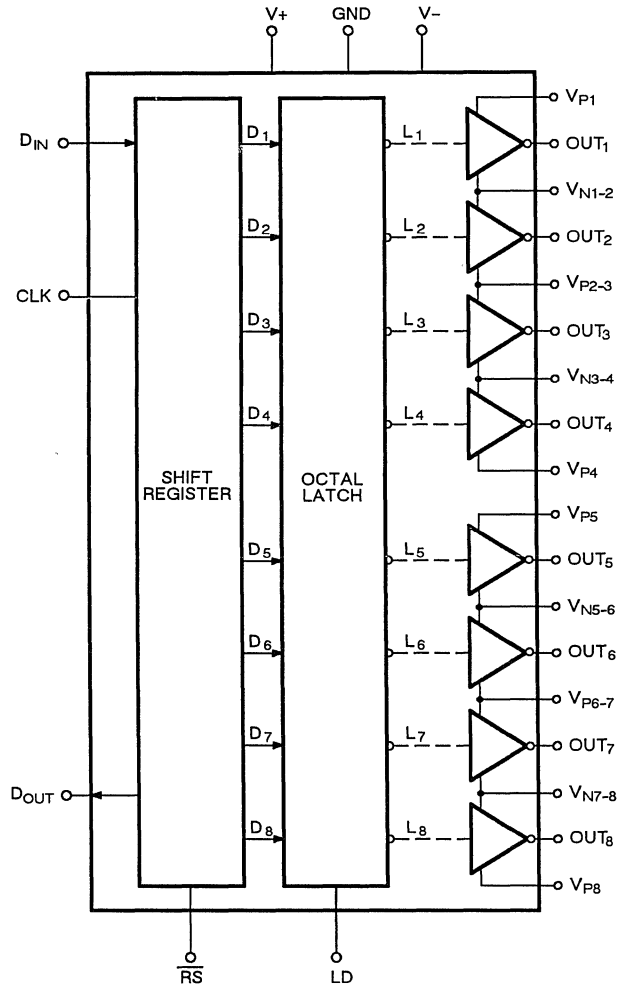
The D470 is built on Siliconix' high voltage silicon gate process to achieve high voltage ratings and high output current capability. An epitaxial layer prevents latchup.

Packaging for the D470 consists of the 28-pin CerDIP, plastic DIP, and PLCC. Performance grades available are military, A suffix ( $-55$  to  $125^\circ\text{C}$ ) and industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ).

## PIN CONFIGURATION



## FUNCTIONAL BLOCK DIAGRAM

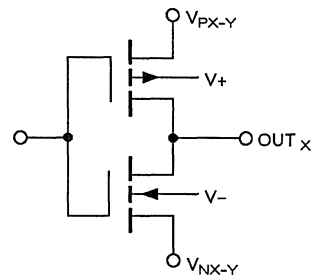


### TRUTH TABLE

$\overline{RS}$	CLK*	D <sub>IN</sub>	D <sub>1</sub>	D <sub>n</sub>
1		0	0	D <sub>n-1</sub>
1		1	1	D <sub>n-1</sub>
1		X	D <sub>1</sub>	D (NO CHANGE)
0	X	X	0	0

### OUTPUT STRUCTURE

LD*	D <sub>1</sub>	L <sub>1</sub>	OUT <sub>1</sub>
	0	1	V <sub>N1-2</sub>
	1	0	V <sub>P1</sub>
	D <sub>1</sub>	L <sub>1</sub>	(NO CHANGE)



\* CLK and LD are level sensitive inputs.

**ABSOLUTE MAXIMUM RATINGS**

V+ to V- ..... 44 V  
 GND to V- ..... 25 V  
 Digital Inputs, V<sub>PX-Y</sub>, V<sub>NX-Y</sub><sup>1</sup> ... (V-) -2 V to (V+) + 2 V  
 or 30 mA, whichever occurs first  
 Continuous Current (Any Terminal) ..... 30 mA  
 Current, I<sub>OS</sub> (Pulsed 1 ms 10% duty cycle) ..... 200 mA  
 Storage Temperature (A Suffix) ..... -65 to 150°C  
 (D Suffix) ..... -65 to 125°C  
 Operating Temperature (A Suffix) ..... -55 to 125°C  
 (D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*  
 28-Pin CerDIP\*\* ..... 1200 mW  
 28-Pin Plastic\*\*\* ..... 625 mW  
 28-Pin PLCC\*\*\*\* ..... 450 mW

- \* All leads welded or soldered to PC Board.
- \*\* Derate 16 mW/°C above 75°C.
- \*\*\* Derate 8.3 mW/°C above 75°C.
- \*\*\*\* Derate 6 mW/°C above 75°C.

<sup>1</sup> Signals exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 15 V, V- = -15 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>d</sup>	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DRIVER</b>									
Output Voltage HIGH	V <sub>OH</sub>	I <sub>O</sub> = -5 mA	1,3 2		14.6 14.4		14.6 14.4		V
		I <sub>O</sub> = -30 mA	1,3 2		11 9		11 9		
Output Voltage LOW	V <sub>OL</sub>	I <sub>O</sub> = 5 mA	1,3 2		-14.6 -14.4		-14.6 -14.4		
		I <sub>O</sub> = 30 mA	1,3 2		-11 -9		-11 -9		
Output Source Current	I <sub>OS+</sub>	V <sub>O</sub> = -15 V Pulsed	1,3 2		200 150		200 150		mA
		V <sub>O</sub> = 0 V Pulsed	1,3 2		175 125		175 125		
Output Sink Current	I <sub>OS-</sub>	V <sub>O</sub> = 15 V Pulsed	1,3 2		-125 -100		-125 -100		
		V <sub>O</sub> = 0 V Pulsed	1,3 2		-125 -100		-125 -100		
<b>LOGIC INPUT</b>									
Input Current with V <sub>IN</sub> LOW	I <sub>IL</sub>	V <sub>IN</sub> Under Test = 0.8 V All Other = 2.4 V	1,2		-1	1	-1	1	µA
Input Current with V <sub>IN</sub> HIGH	I <sub>IH</sub>	V <sub>IN</sub> Under Test = 2.4 V All Other = 0.8 V	1,2		-1	1	-1	1	

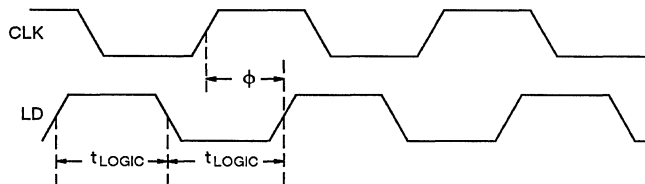
**8**

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>+</sub> = 15 V, V <sub>-</sub> = -15 V GND = 0 V V <sub>IN</sub> = 2.4 V, 0.8 V <sup>d</sup>	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>LOGIC OUTPUT</b>									
Output Voltage LOW (D <sub>OUT</sub> )	V <sub>OL</sub>	I <sub>O</sub> = 3.2 mA	1,2		0.4		0.4	V	
Output Voltage HIGH (D <sub>OUT</sub> )	V <sub>OH</sub>	I <sub>O</sub> = -80 μA	1,2	2.4		2.4		V	
<b>DYNAMIC</b>									
Pulse Width for Logic Inputs	t <sub>LOGIC</sub>	(D <sub>IN</sub> , LD, CLK, $\overline{RS}$ )	1 2	80 150		80 150		ns	
Propagation Delay (Rise)	t <sub>PR</sub>	V <sub>IN</sub> = LD, C <sub>L</sub> = 500 pF 50% of V <sub>IN</sub> to 50% of V <sub>O</sub>	1 2		150 200		250 200		
Propagation Delay (Fall)	t <sub>PF</sub>		1 2		200 250		200 250		
Data Setup Time	t <sub>DW</sub>		1,2	50		50			
<b>SUPPLY</b>									
Positive Supply Current	I <sub>+</sub>	V <sub>+</sub> = 16.5 V, V <sub>-</sub> = -16.5 V V <sub>IN</sub> = 0 or 5 V	1,2		100		100	μA	
Negative Supply Current	I <sub>-</sub>		1,2		-1		-1		
Ground Current	I <sub>GND</sub>		1,2		-100		-100		

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. V<sub>IN</sub> = Input voltage to perform proper function.

## INPUT TIMING REQUIREMENTS

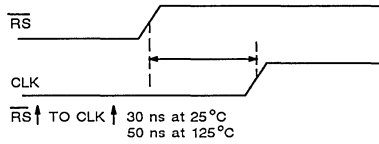
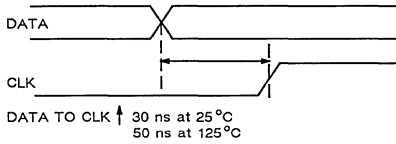


φ = for CLK and LD inputs of the same frequency  
The recommended phase delay of LD from CLK is 1/2 t<sub>LOGIC</sub> to t<sub>LOGIC</sub>

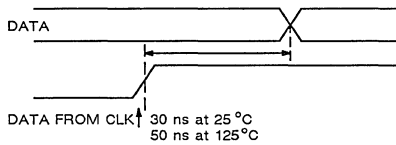
t<sub>LOGIC</sub>(MIN) : 80 ns at 25°C      V<sub>+</sub> = +15 V  
150 ns at 125°C                  V<sub>-</sub> = -15 V  
GND = 0 V

**INPUT TIMING REQUIRMENTS (Cont'd)**

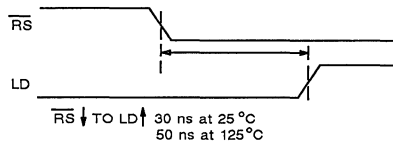
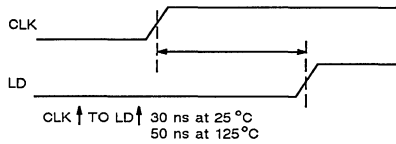
SHIFT REGISTER SETUP



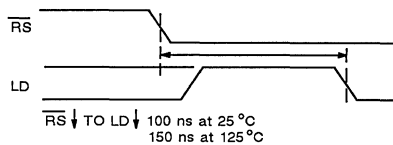
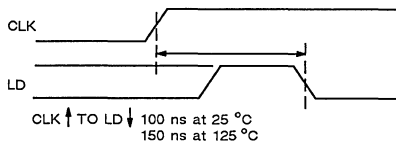
SHIFT REGISTER HOLD



ADDRESS REGISTER SETUP

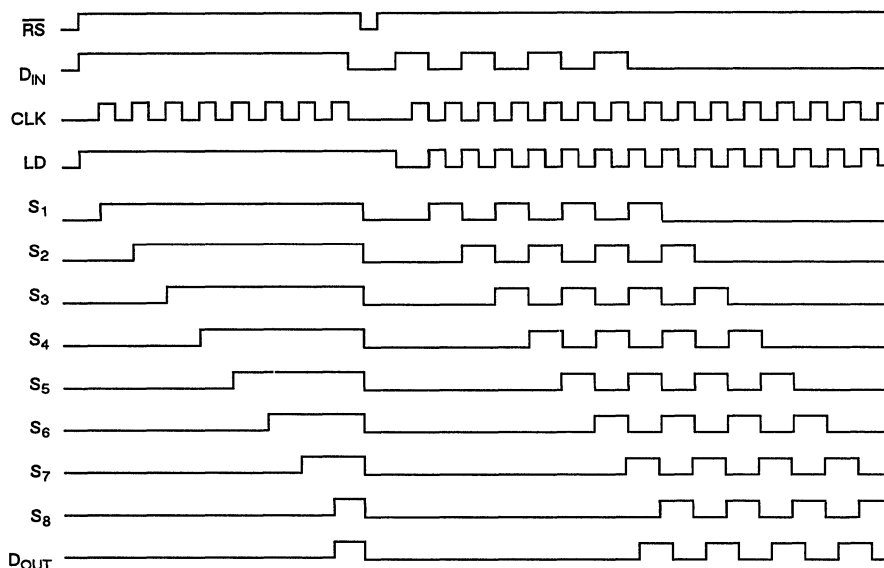


ADDRESS REGISTER ENABLE



V<sub>+</sub> = +15 V, V<sub>-</sub> = -15 V, GND = 0 V  
INPUTS ARE 0 V TO 3 V

## TIMING DIAGRAM



$S_1 - S_8$  and  $D_{OUT}$  are expected output with the drain connected high.  
The sources require pull-downs of 1 k $\Omega$ .

## PIN DESCRIPTION

### SYMBOL DESCRIPTION

LD	Logic LOAD DATA Input. When HIGH it loads the contents of the shift register into the octal latch.
NC	No Connection
$V_{PX-Y}$	Positive power supply voltage common to buffers X and Y.
$OUT_X$	Buffer X output
$V_{NX-Y}$	Negative Power Supply Voltage, common to buffers X and Y.
$V_+$	Positive Supply Voltage
$D_{IN}$	Serial Data Input. TTL Compatible for $V_+ = +4.5$ V up to +22 V.
CLK	Clock. The d-type master-slave flip-flops that make the shift register are updated during the positive transitions of the clock.
$D_{OUT}$	Serial Data Output. TTL compatible output levels. Can be used to chain several devices.
$V_-$	Negative Supply Voltage.
GND	Digital Ground.
$\overline{RS}$	RESET. When LOW this input clears the contents of the shift register to an all zeroes state.



# L144

## Low-Power Triple Operational Amplifier

### FEATURES

- Three Amplifiers in One Package
- Low Power Consumption
- Programmable Supply Current
- Operates From  $\pm 1.5$  to  $\pm 15$  V
- Drives Large Capacitive Loads ( $< 1000$  pF)

### BENEFITS

- Reduces Board Space and Parts Count
- Reduces System Power Supply Requirements
- Easily Tailored to Optimize Circuit Performance
- Eliminates Additional Supply Voltages
- Increases System Stability

### APPLICATIONS

- Instrumentation Amplifiers
- Battery-Powered Systems
- Remote Data Sensing
- Voltage Comparators
- Active Filters

### DESCRIPTION

The Siliconix L144 is a low cost triple operational amplifier designed for general purpose applications where low power is a primary consideration. Features include operation with supply voltages as low as  $\pm 1.5$  VDC, programmable supply current (with single resistor), and internal compensation to ensure stability under all conditions of resistive feedback. The L144 will drive capacitive loads to 1000 pF, and the output stages are short-circuit protected.

The programmable supply current of the L144 allows the user to minimize the effects of the speed-power trade-offs associated with all op amps. The three amplifier architecture is excellent for instrumentation-amplifier configurations. The

unity-gain stable internal compensation allows simplified operation in buffer, active filter, and gain stage applications.

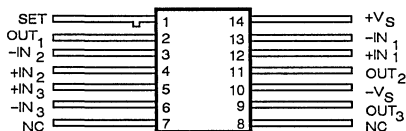
The L144 is built in a standard bipolar process, allowing low-drift operation over a wide range of power supply voltages and temperatures. Package options include the popular 14-pin side braze and plastic DIP, and the flat pack. The L144 device is specified for operation over the military, A suffix ( $-55$  to  $125^\circ\text{C}$ ), industrial, B suffix ( $-25$  to  $85^\circ\text{C}$ ), and the commercial, C suffix ( $0$  to  $70^\circ\text{C}$ ) temperature ranges.

For more information on the L144, please refer to Siliconix Application Note AN73-6.



### PIN CONFIGURATION

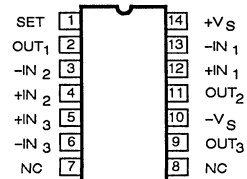
Flat Package



Top View

Order Numbers: L144AL /883

Dual-In-Line Package



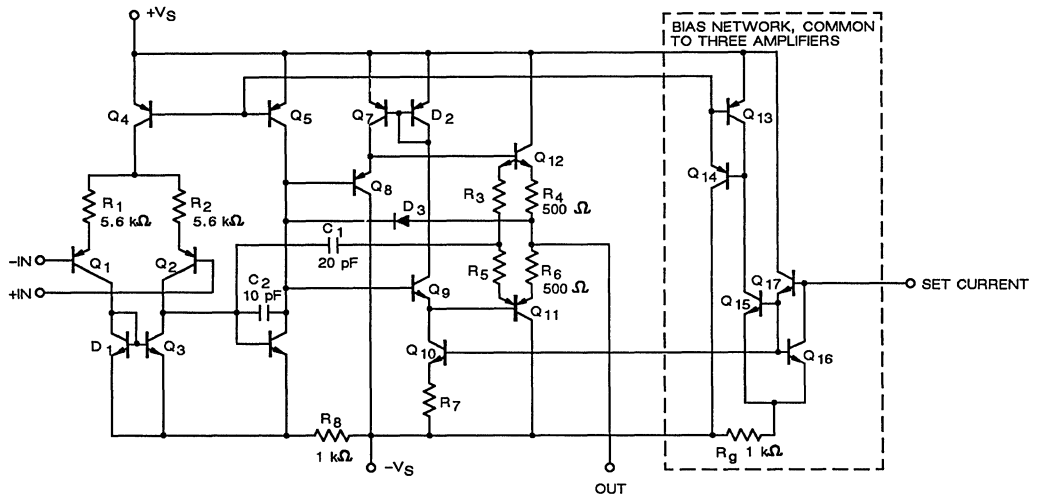
Top View

Order Numbers:

Side Braze: L144AP, L144AP/883  
L144BP, L144BP/883

Plastic: L144CJ

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Supply voltage .....	$\pm 18$ V
Differential Input Voltage .....	$\pm 30$ V
Input Voltage* (A, B Suffix) .....	$\pm 18$ V
(C Suffix) .....	$\pm 15$ V
Output Short Circuit Duration** .....	Indefinite
Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C
(C Suffix) .....	0 to 70°C
Storage Temperature (A and B Suffix) .....	-65 to 150°C
(C Suffix) .....	-65 to 125°C

Lead Temperature (Soldering 60 s) .....	300°C
Power Dissipation (Package)***	
Flat Package .....	750 mW
14-Pin Ceramic DIP .....	825 mW
Plastic DIP .....	470 mW

- \* For supply voltages  $< \pm 18$  V, maximum input voltage is equal to the supply voltage.
- \*\* Continuous short circuit is allowed for case temperatures to  $+125^\circ\text{C}$  and ambient temperature to  $+70^\circ\text{C}$ .
- \*\*\* All leads welded or soldered to P.C. board. Derate 10 mW/ $^\circ\text{C}$  for the flat package, 11 mW/ $^\circ\text{C}$  for the 14-pin DIP above  $+75^\circ\text{C}$  and 6.3 mW/ $^\circ\text{C}$  above  $25^\circ\text{C}$  for the plastic DIP.

## ELECTRICAL CHARACTERISTICS<sup>a, e</sup>

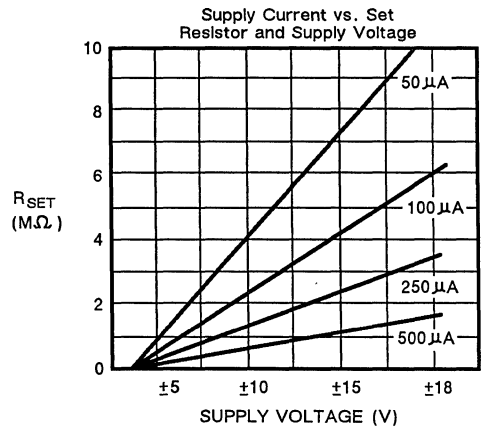
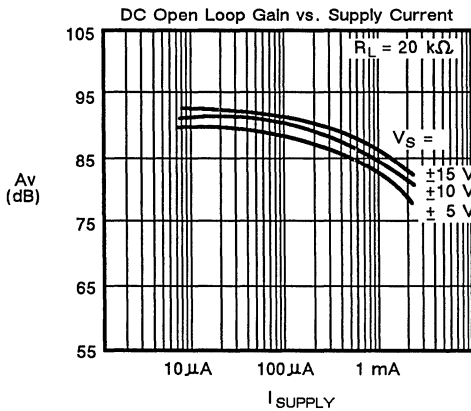
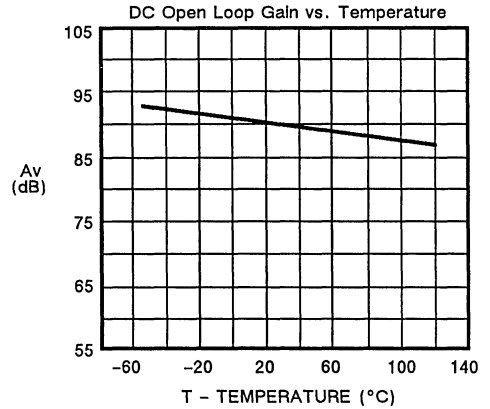
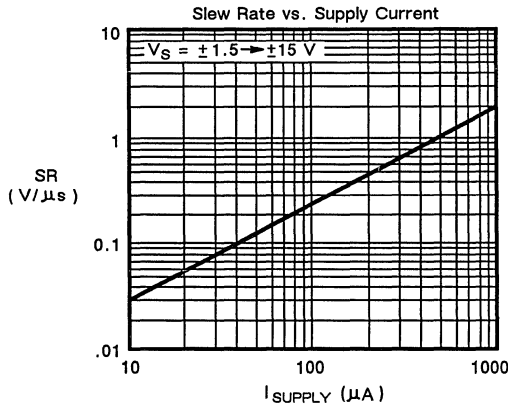
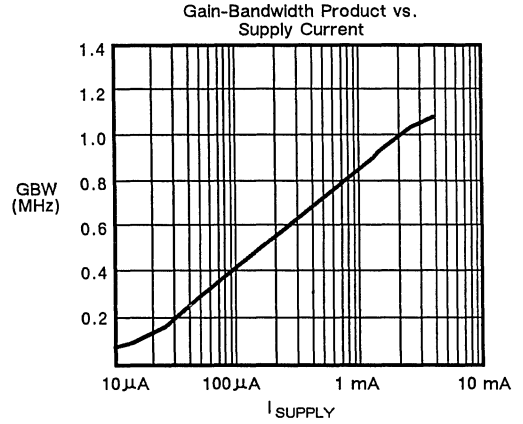
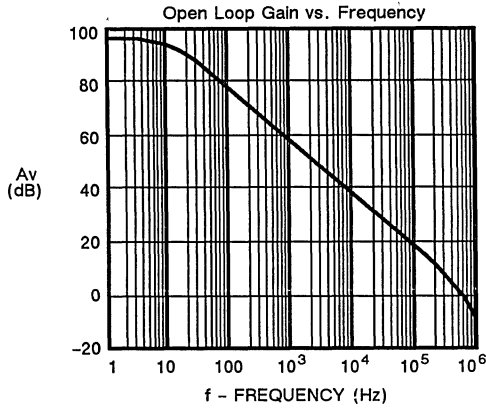
PARAMETER	SYMBOL	Test Conditions <sup>d</sup> Unless Otherwise Specified: $V_S = \pm 15\text{V}$ , $R_L = 50\text{ k}\Omega$ $R_{SET} = 3\text{ M}\Omega$ (Pin 1 to 14)	LIMITS						UNIT
			1=25°C		A/B SUFFIX		C SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
Input Offset Voltage	$V_{OS}$	$R_S \leq 50\text{ k}\Omega$	1 2,3	1	5 6		10	mV	
Offset Voltage Tempco	$TC_{VOS}$	$R_S \leq 50\text{ k}\Omega$	1	3.3				$\mu\text{V}/^\circ\text{C}$	

ELECTRICAL CHARACTERISTICS <sup>a, e</sup>									
PARAMETER	SYMBOL	Test Conditions <sup>d</sup> Unless Otherwise Specified: $V_S = \pm 15V$ , $R_L = 50\text{ k}\Omega$ $R_{SET} = 3\text{ M}\Omega$ (Pin 1 to 14)	LIMITS						UNIT
			1=25°C		A/B SUFFIX		C SUFFIX		
			2=125,85,70°C		MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
			TEMP	TYP <sup>c</sup>					
<b>INPUT (Cont'd)</b>									
Input Offset Current	$I_{OS}$		1	2		50		70	nA
Input Bias Current	$I_{BIAS}$		1,2	-100	-200		-250		
<b>OUTPUT</b>									
Output Voltage Swing	$V_{OUT}$		1	$\pm 14$	-10	10	-10	10	V
Output Voltage Swing	$V_{OUT}$	$V_S = \pm 1.5\text{ V}$ , $R_{SET} = 120\text{ k}\Omega$	1	$\pm 0.5$					
Output Short Circuit Current	$I_{SC}$	$R_L = 0\ \Omega$	1	1.5		15		15	mA
<b>DYNAMIC</b>									
DC Open Loop Voltage Gain	$A_{VOL}$		1,2,3	30	3		1		V/mV
Slew Rate	SR		1	0.4					V/ $\mu$ s
Unity Gain Bandwidth	GBW		1	0.6					MHz
Crosstalk		$f = 100\text{ Hz}$	1	-100					dB
Common Mode Rejection Ratio	CMRR	$V_{IN} = \pm 12\text{ V}$	1	90	80		70		
<b>SUPPLY</b>									
Power Supply Rejection Ratio	PSRR		1	90	80		80		dB
Supply Current	$I_S$	Unity Gain, $V_{IN} = 0\text{ V}$ On All Amplifiers	1		350		400		$\mu$ A

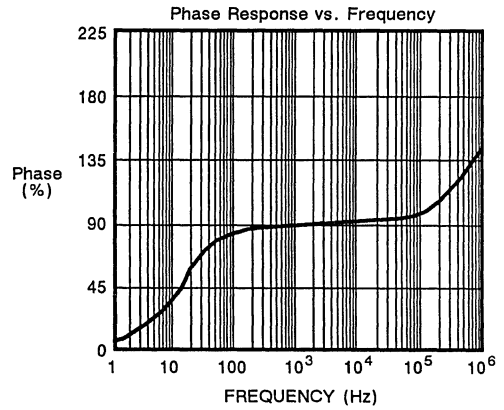
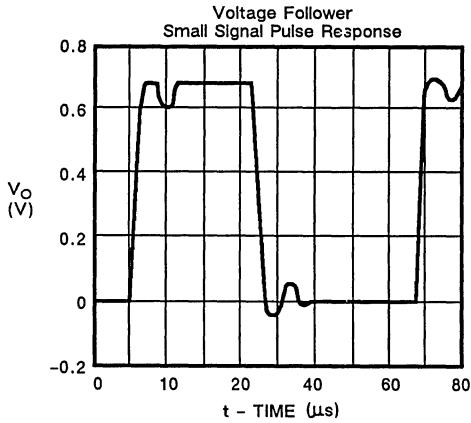
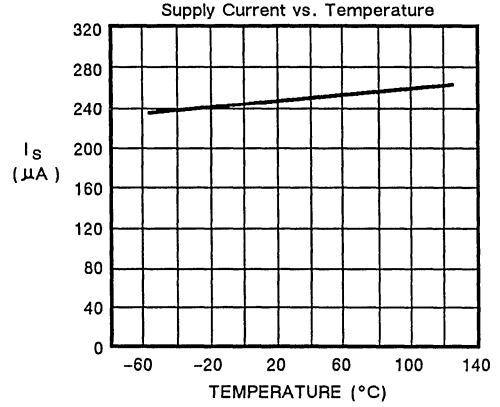
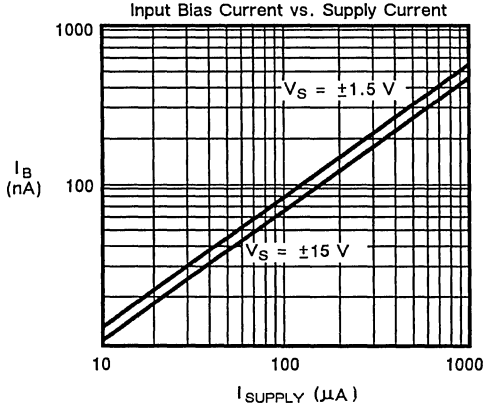
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d.  $I_{SET}$  is adjustable. See typical characteristics.
- e. All dc parameters are 100% tested at 25°C. Lots are sample-tested for ac parameters and high and low temperature limits to assure conformance with specifications.

## TYPICAL CHARACTERISTICS

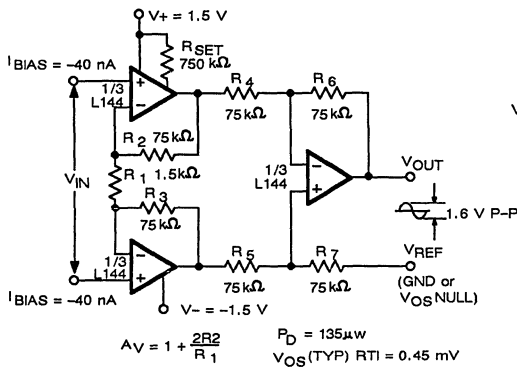


TYPICAL CHARACTERISTICS

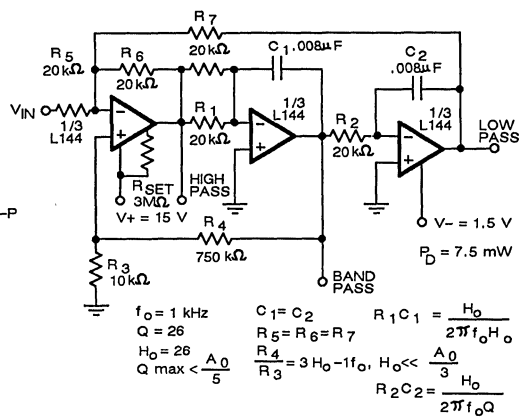


## APPLICATIONS

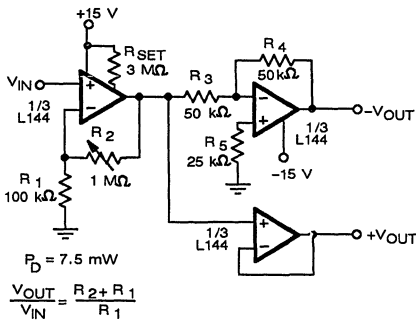
### Instrumentation Amplifier



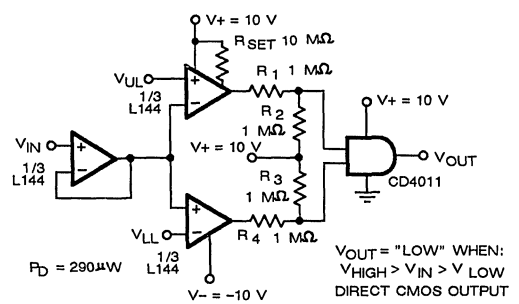
### Active Filter



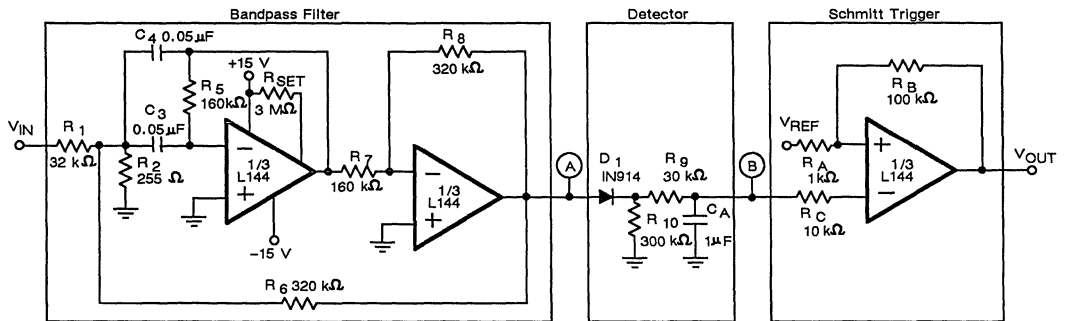
### Precision Phase Splitter



### Double-Ended Limit Comparator



### 500 Hz Tone Detector



GIVEN  $Q, f_o, C$  THEN  $R_5 = \frac{Q}{2\pi f_o C}$   $Q$  normally from 10 to 50,  $K$  is chosen for component value convenience.  
 LET  $C = C_3 = C_4$   $1 < K < 10$   $R_8 = R_6 = K R_5$   
 THEN  $R_7 = R_5$  for convenience  $R_1 = \frac{K R_5}{H_o}$  IN THIS CIRCUIT  $H_o = 10$   
 $R_1 = \frac{R_5}{\frac{H_o + 1}{Q_2 - K}}$   $f_o = 500\text{ Hz}$   $Q = 25$

$$f_{3db} = \frac{f_o}{100}$$

$$V_{HIGH} = \frac{V_{ref} R_B + 14 R_A}{R_A + R_B}$$

$$V_{LOW} = \frac{V_{ref} R_B - 14 R_A}{R_A + R_B}$$

# L161

## Micropower Quad Comparator

### FEATURES

- Programmable Supply Current
- Ultra-Low Power Consumption
- Four Comparators on Single Chip
- Direct CMOS Logic Compatibility
- Input Sensing Near Ground

### BENEFITS

- Allows User to Program Speed/Power Trade-Off
- Minimizes System Power Requirements
- Reduces Board Space
- Simplifies Logic Interface
- Simplifies Single-Supply Operation

### APPLICATIONS

- Smart Munitions
- Battery-Operated Systems
- Miniaturized Systems
- CMOS Logic Systems
- Level Detectors
- Window Comparators
- Oscillators and Ramp Generators

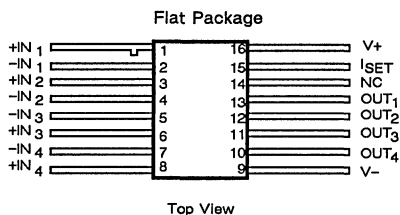
### DESCRIPTION

The L161 is a monolithic quad comparator featuring control of both DC and AC parameters with a single power-supply current setting resistor. Operation at very low supply current levels with power dissipation typically in the microwatt region makes the L161 ideally suited for battery operation. The programmable supply current feature allows the user to optimize the speed-power trade-off to the specific application, truly minimizing system power dissipation. The L161 is fabricated in a standard

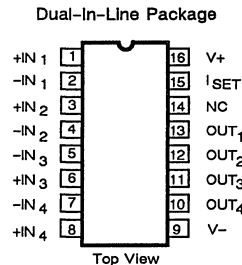
bipolar process, resulting in a wide range of operating supply voltages and currents, and allowing low-drift operation over the entire military temperature range. The L161 is available in the 16-pin plastic DIP. Performance grades include a military, A suffix (-55 to 125°C), industrial, B suffix (-25 to 85°C), and commercial, C suffix (0 to 70°C) operation.

For more information on the L161, please refer to Siliconix Application Note AN76-7.

### PIN CONFIGURATION



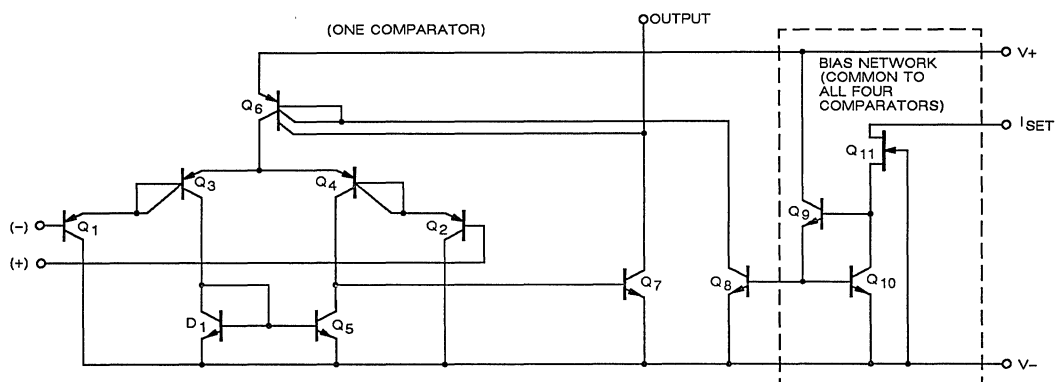
Order Numbers: L161AL/883



Order Numbers:

Side Braze: L161AP, L161BP  
Plastic: L161CJ

## SCHEMATIC DIAGRAM (ONE COMPARATOR)



### ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Differential Input Voltage	±30 V
Input Voltage*	±18 V
Output Short Circuit Duration**	Indefinite
Operating Temperature	
(A Suffix)	-55 to +125°C
(B Suffix)	-25 to +85°C
(C Suffix)	0 to +70°C
Storage Temperature	
(A and B Suffix)	-65 to 150°C
(C Suffix)	-65 to 125°C

### Power Dissipation (Package)\*\*\*

Flat Package	750 mW
16-pin DIP (Side braze)	900 mW
16-pin Plastic DIP	470 mW

\* For supply voltages  $< \pm 18$  V, maximum input voltage is equal to the supply voltage.

\*\* Continuous short circuit current is allowed for case temperature to +125°C and ambient temperature to +70°C.

\*\*\* All leads welded or soldered to PC board. Derate 10 mW/°C above 75°C for the flat package, 12 mW/°C above 75°C for the side braze DIP and 6.3 mW/°C above 25°C for the plastic DIP.

### LOW POWER ELECTRICAL CHARACTERISTICS<sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_S = \pm 3$ V, $I_{SET} = 10$ $\mu$ A $R_L = 10$ M $\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX		B,C SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
Input Offset Voltage	$V_{OS}$		1 2,3	1 1		3 5		6	mV
Input Offset Current	$I_{OS}$		1	1		20		25	nA
Input Bias Current	$I_{BT}$		1	20		100		200	



LOW POWER ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_S = \pm 3\text{ V}$ , $I_{SET} = 10\ \mu\text{A}$ $R_L = 10\ \text{M}\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX		B,C SUFFIX		
			2=125,85,70°C						
			3=-25,-55,0°C		TYP <sup>c</sup>		MIN <sup>b</sup> MAX <sup>b</sup>		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>OUTPUT</b>									
DC Open Loop Voltage Gain	$A_{VOL}$		1,2 3	30 30	20 10		10 5		V/mV
Low Output Voltage <sup>d</sup>	$V_{OL}$	$R_L = 20\ \text{k}\Omega$	1	-2.95		-2.6		-2.6	V
High Output Voltage <sup>d</sup>	$V_{OH}$	$R_L = 200\ \text{k}\Omega$	1	2.9	2.5		2.5		
<b>DYNAMIC</b>									
Common Mode Range	CMR	Positive Limit Negative Limit	1	1.3 -3.0					V
Response Time	t	100 mV Overdrive $C_L = 10\ \text{pF}$	1	5					$\mu\text{s}$
Common Mode Rejection Ratio	CMRR	$V_{IN} = \text{CMR}$	1	90	75		75		dB
<b>SUPPLY</b>									
Power Supply Rejection Ratio	PSRR		1	80	65		65		dB
Supply Current <sup>e</sup>	$I_S$	All Outputs Low $R_L = \infty$	1 2,3	210 210		325 325		325 350	$\mu\text{A}$

HIGH POWER ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions <sup>d</sup> Unless Otherwise Specified: $V_S = \pm 15\ \text{V}$ , $I_{SET} = 100\ \mu\text{A}$ $R_L = 2\ \text{M}\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX		B,C SUFFIX		
			2=125,85,70°C						
			3=-25,-55,0°C		TYP <sup>c</sup>		MIN <sup>b</sup> MAX <sup>b</sup>		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	UNIT
<b>INPUT</b>									
Input Offset Voltage	$V_{OS}$		1 2,3	1.5 1.5		3 6		6	mV
Input Offset Current	$I_{OS}$		1	5		60		90	nA
Input Bias Current	$I_{BT}$		1 2,3	100 100		400 500		800	

HIGH POWER ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_S = \pm 15\text{ V}$ , $I_{SET} = 100\ \mu\text{A}$ $R_L = 2\ \text{M}\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX		B,C SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>OUTPUT</b>									
DC Open Loop Voltage Gain	$A_{VOL}$		1,2 3	100 100	50 25		30 15		V/mV
Low Output Voltage <sup>d</sup>	$V_{OL}$	$R_L = 20\ \text{k}\Omega$	1	-14.9		-14.6		-14.6	V
High Output Voltage <sup>d</sup>	$V_{OH}$	$R_L = 200\ \text{k}\Omega$	1	14.9	14.5		14.5		
<b>DYNAMIC</b>									
Common Mode Range	CMR	Positive Limit	1	13					V
		Negative Limit	1	-15					
Response Time	t	100 mV Overdrive $C_L = 10\ \text{pF}$	1	1					$\mu\text{s}$
Common Mode Rejection Ratio	CMRR	$V_{IN} = \text{CMR}$	1	90	75		75		dB
<b>SUPPLY</b>									
Power Supply Rejection Ratio	PSRR		1	80	65		65		dB
Supply Current <sup>e</sup>	$I_S$	All Outputs Low $R_L = \infty$	1 2,3	2.1 2.1		3.75 4.0		3.75 4.0	mA

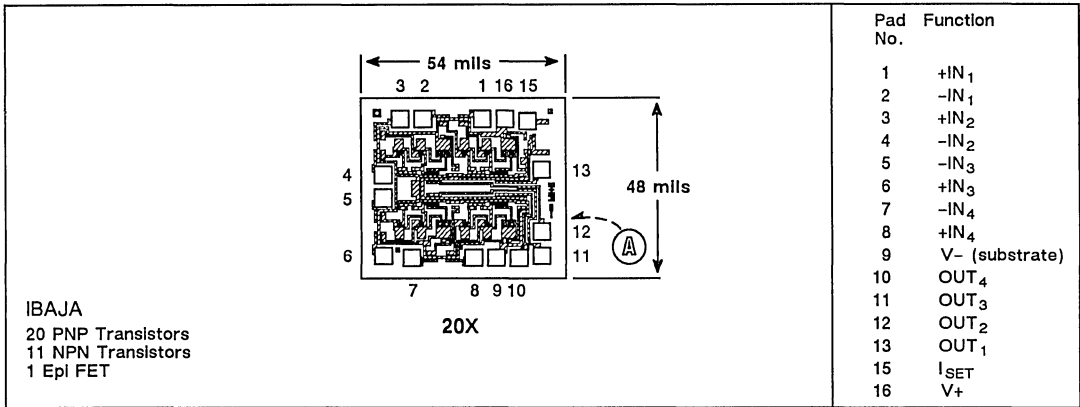
**NOTES:**

- Refer to PROCESS OPTION FLOWCHART for additional information.
  - The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
  - Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
  - The output current drive of the L161 is non-symmetrical. This facilitates the wire-ORing of two comparator outputs.
  - The output pull-down current is typically 75-100 times the pull-up current.
- Set current ( $I_{SET}$ ) and supply current ( $I_{SUPPLY}$ ) can be determined by the following formulas:

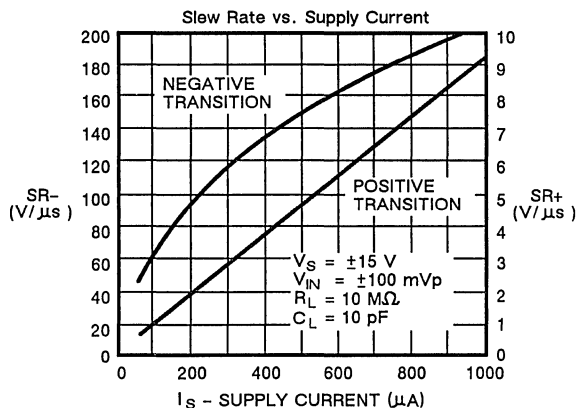
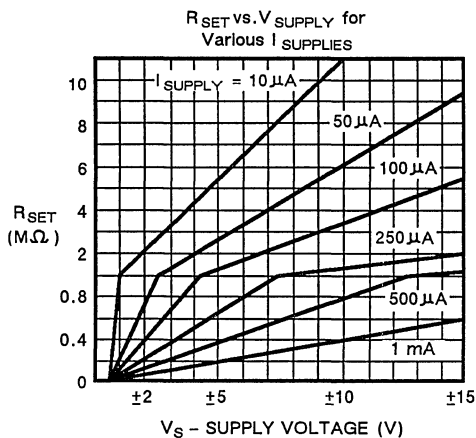
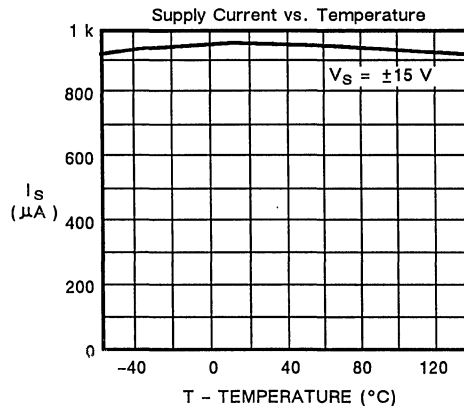
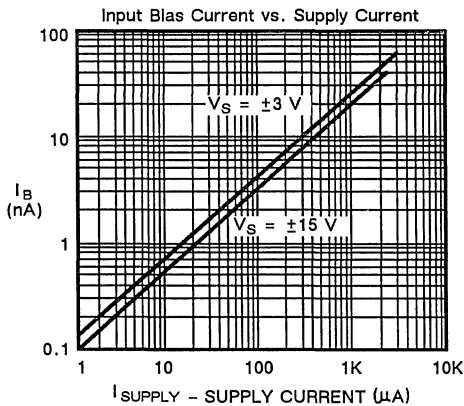
$$I_{SET} = \frac{[(V+) - (2V_{BE}) - (V-)]}{R_{SET}}$$

$$I_{SUPPLY} = 21 \times I_{SET}$$

**DIE TOPOGRAPHY**



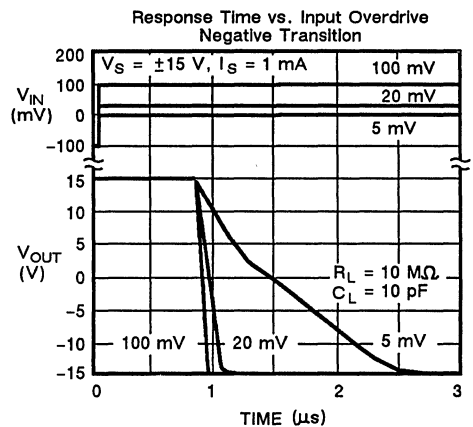
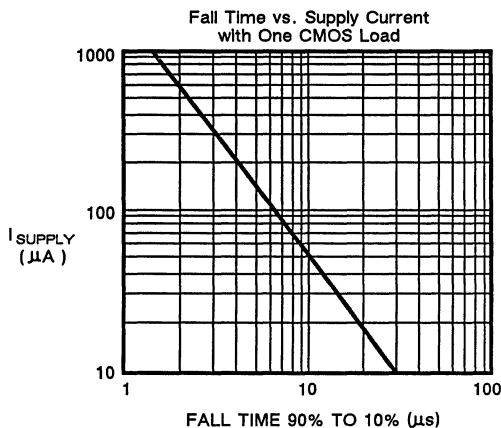
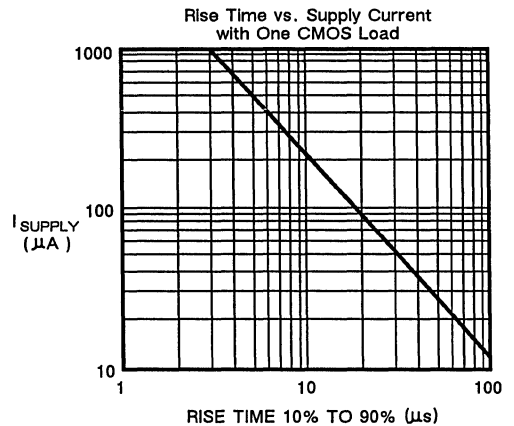
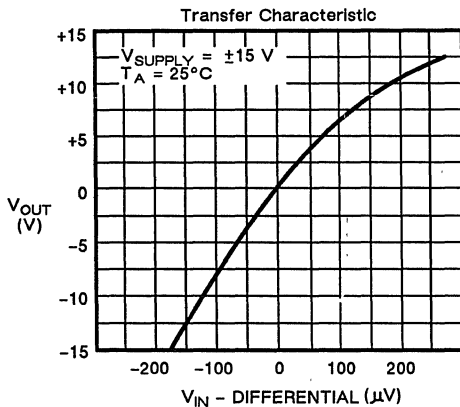
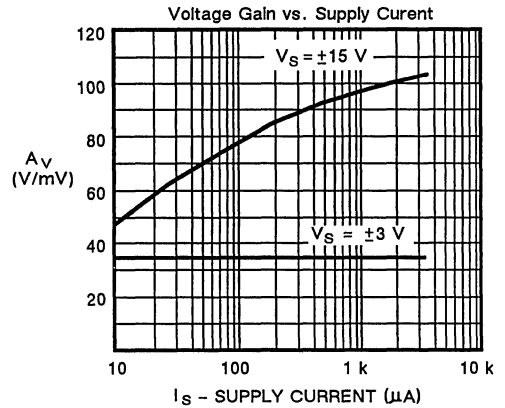
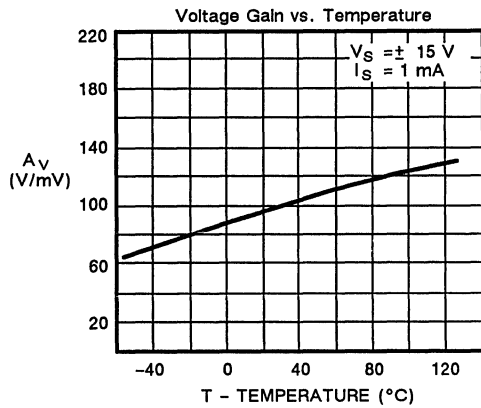
**TYPICAL CHARACTERISTICS**



NOTE: The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically  $2[V_+ - 1 - (V_-)/R_{SET}]$  and the pull-down current capability is typically from 75 to 150 times the pull-up current.

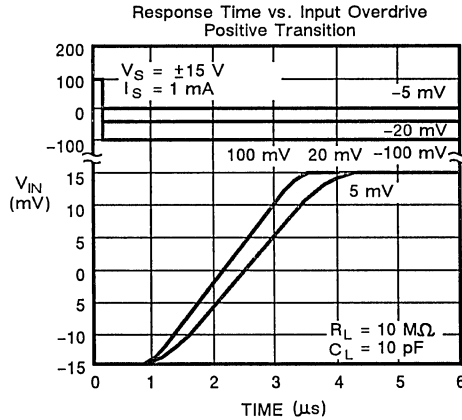


## TYPICAL CHARACTERISTICS (Cont'd)



NOTE: The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically  $2[(V_+) - 1 - (V_-) / R_{SET}]$  and the pull-down current capability is typically from 75 to 150 times the pull-up current.

**TYPICAL CHARACTERISTICS (Cont'd)**



NOTE: The output current drive of each comparator in the L161 is non-symmetrical. The pull-up current is typically  $2[(V+) - 1 - (V-)/R_{SET}]$  and the pull-down current capability is typically from 75 to 150 times the pull-up current.

**APPLICATIONS**

The L161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias current, slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations -- typically in the low microwatt region -- is possible. The L161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

The L161 is fabricated using standard bipolar

processing. The circuit (Figure 1) is composed of five major blocks -- four comparators and a common bias network. Q1 - Q6 and D1 form a darlington differential amplifier with double-to-single ended conversion. Q6 is a dual current source whose outputs are exactly twice the current flowing through Q8. The collector current of Q8 is a function of the current supplied externally to Q9 - Q10, which in turn is known as the set current or  $I_{SET}$ . This set current is established by a resistor connected between the  $I_{SET}$  terminal and a voltage source, most commonly the positive supply. Q11 prevents excessive current from flowing through Q9 and Q10 in the event the  $I_{SET}$  terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

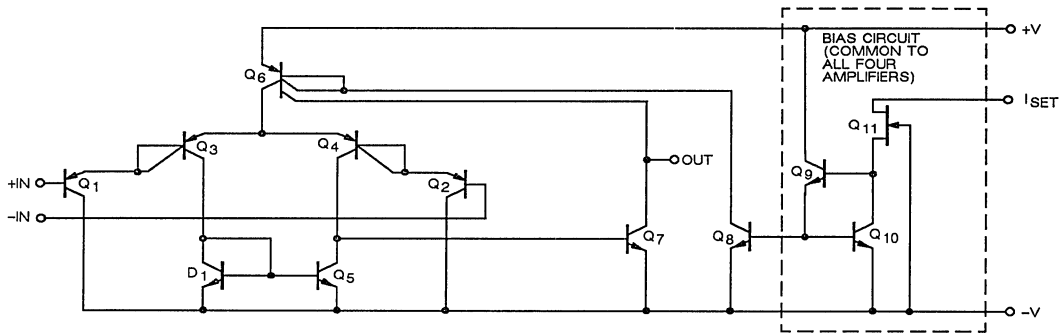


Figure 1. Schematic of One Channel of the L161 Plus the Common Bias Network

## APPLICATIONS (Cont'd)

### SETTING THE SET CURRENT

The set current can be expressed as:

$$I_{SET} = \frac{(V+) - (2 V_{BE}) - (V-)}{R_{SET}} \quad (1)$$

where  $V+$  is the voltage to which the control resistor is connected,  $V-$  is the negative supply voltage,  $V_{BE}$  is the base emitter drop of Q9 or Q10 (about 0.7 V), and  $R_{SET}$  is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of Ohms Law. There is also an analytical relationship between  $I_{SET}$  and the total supply current:

$$\begin{aligned} I_{SUPPLY} &= (I_{SET} \text{ (current sourced by Q6 to Q8)}) \\ &+ 2 I_{SET} \text{ (current sourced to the differential amplifier by Q6)} \\ &+ 2 I_{SET} \text{ (current sourced to the comparator output by Q6)} \\ &\times 4 \text{ (the total number of comparators)} \\ &+ I_{SET} \text{ (current sourced through Q11, Q10, and Q9 to } V-) \\ &= (I_{SET} + 2 I_{SET} + 2 I_{SET}) \times 4 + I_{SET} \\ &= 21 I_{SET} \end{aligned} \quad (2)$$

The output current pulldown capability ( $I_{OL}$ ) of the L161 is about 2 orders of magnitude greater than the high output drive current, ( $I_{OH}$ ), which allows wire-ORing the outputs.  $I_{OH}$  is simply the current sourced by Q6:

$$I_{OH} = 2 \times I_{SET} \quad (3)$$

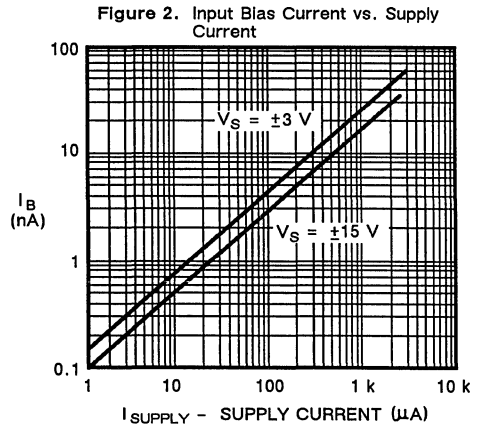
$I_{OL}$  is found by multiplying the current sourced by the collector of Q6 by the gain Q7:

$$I_{OL} = \beta (Q7) \times 2 I_{SET} \quad (4)$$

The beta of Q7 is about 75-150.

### INPUT BIAS CURRENT

Input bias current is a function of the betas of input devices Q1 - Q2 and  $I_{SET}$ . This is difficult to express analytically because  $\beta$  varies greatly with both processing and collector current; however it is roughly proportional to the set current and can easily be determined experimentally (see Figure 2).



### GAIN

Gain varies logarithmically with changes in supply voltage and linearly with changes in set current. Primary causes are the decrease in output impedance of Q7 with decreasing supply voltage and an increase in transistor betas with increasing set current. Other AC parameters such as slew rate and transition time are also effected by set current; however, current dependent parameters such as beta and chip capacitances make mathematical expressions imprecise. These relationships have been determined empirically and are presented in Figure 3 and 4.

APPLICATIONS (Cont'd)

Figure 3. Slew Rate vs. Supply Current

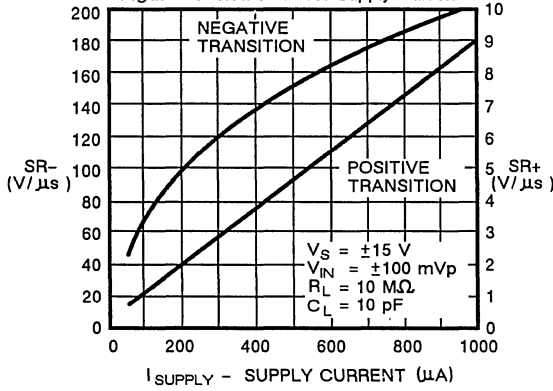
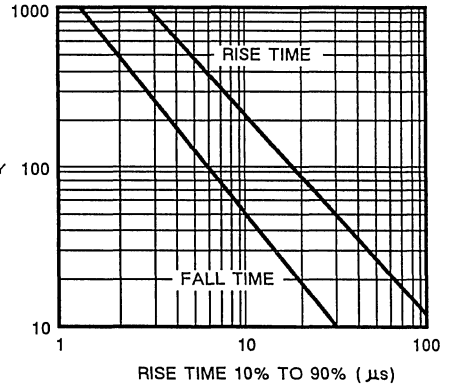
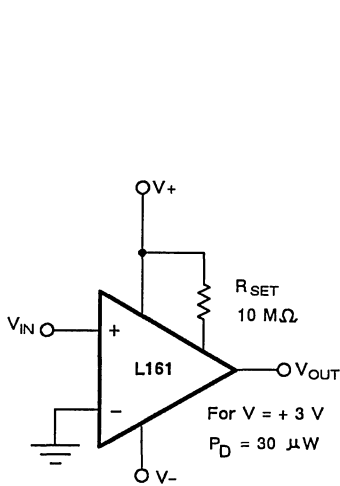


Figure 4. Rise and Fall Times vs. Supply Current With One CMOS Load

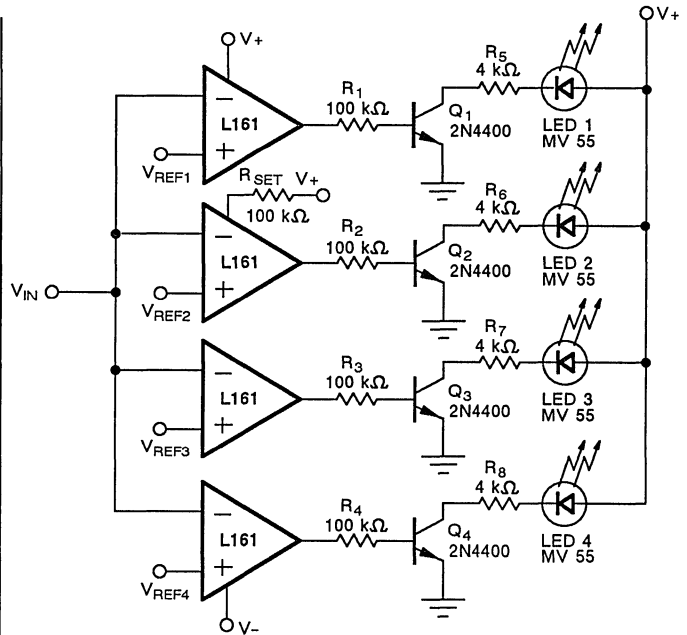


The designer's ability to program the key parameters of the L161 enables him to program just enough supply current to meet his design objectives. This coupled with the L161's performance using only microwatts of power makes

it ideal for any micropower or battery-powered system, as well as a replacement for existing higher power comparators. The following applications illustrate the flexibility and unique capabilities of the L161.

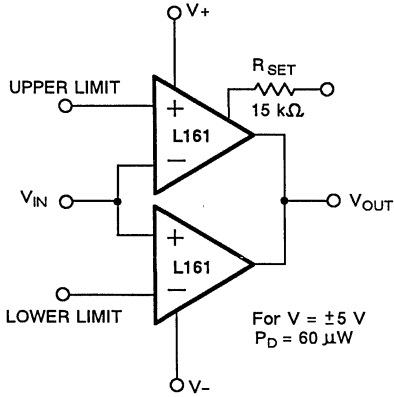


Zero Crossing Detector

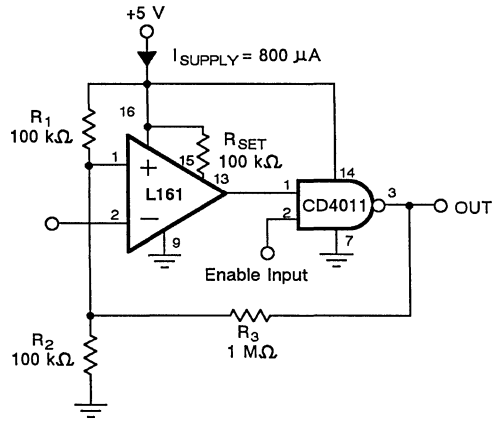


Voltage Level Detector

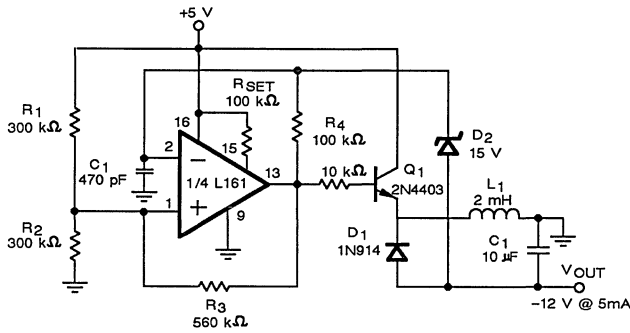
## APPLICATIONS (Cont'd)



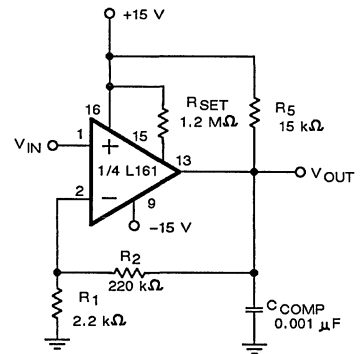
Double Ended Limit Detector



CMOS Line Receiver



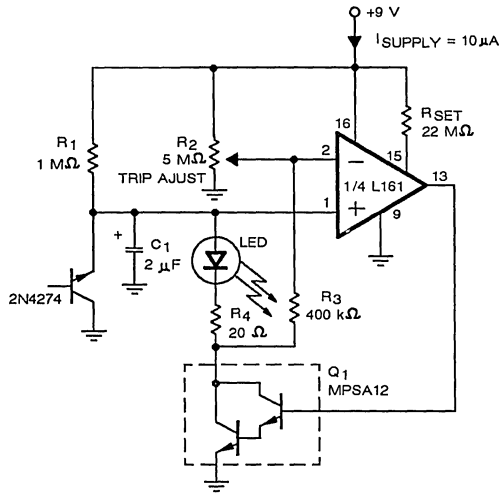
A Regulated DC to DC Converter



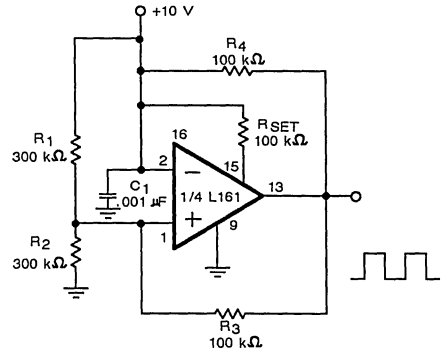
The L161 as an X100 Operational Amplifier



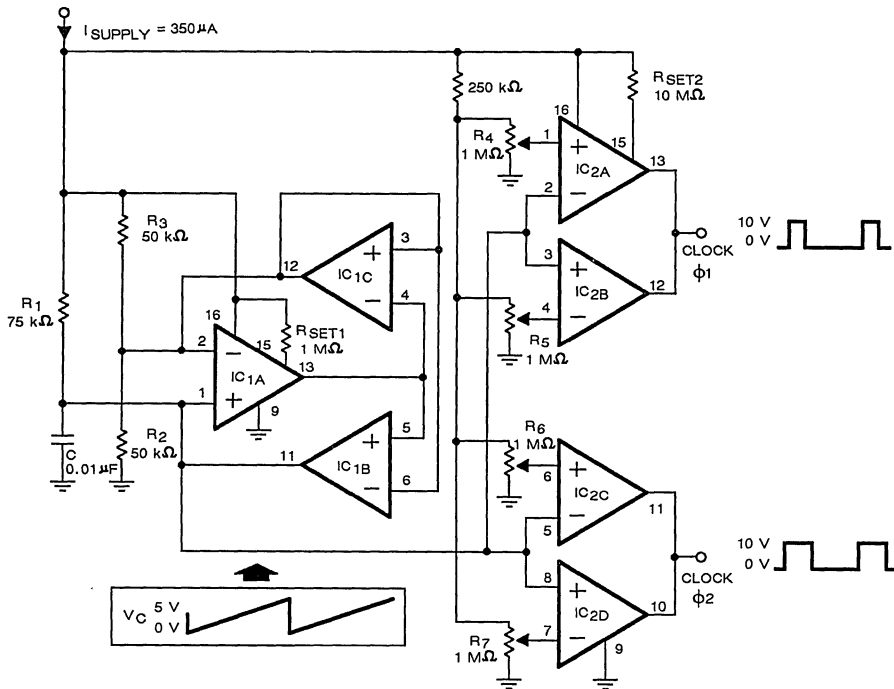
APPLICATIONS (Cont'd)



A Low Battery Indicator



Square Wave Oscillator



A Versatile 2 φ Pulse Generator

# Si7250

## Bubble Memory Power Driver

### FEATURES

- TTL Compatible Inputs
- Transition Time < 25 ns with 500 pF Load
- Power Fail Reset
- Single Voltage Power Supply

### BENEFITS

- Very Low Standby Power
- Easy To Interface
- Protection of Bubble Memories

### APPLICATIONS

- Bubble Memory Coil Pre-Driver

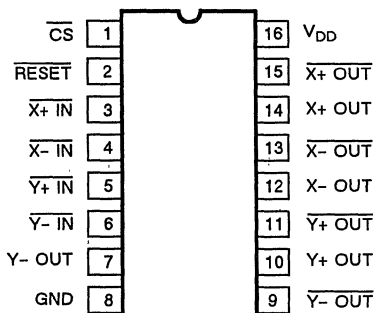
### DESCRIPTION

The Si7250 is a low power coil predriver for direct use with the Siliconix VQ7254 quad MOSPOWER array to drive magnetic bubble memory coils. Its high speed ( $t_{\text{TRANS}} < 25 \text{ ns}$  with 500 pF load), TTL compatible inputs and complementary outputs make this device ideal for driving high gate capacitance MOSPOWER devices.

The Si7250 is built on the Siliconix proprietary PolyMOS process, allowing superior current handling capabilities. A power fail reset pin protects memory contents in the event of power failure.

Packaging options include the 16-pin CerDIP for commercial, C suffix (0 to 70°C) temperature operation.

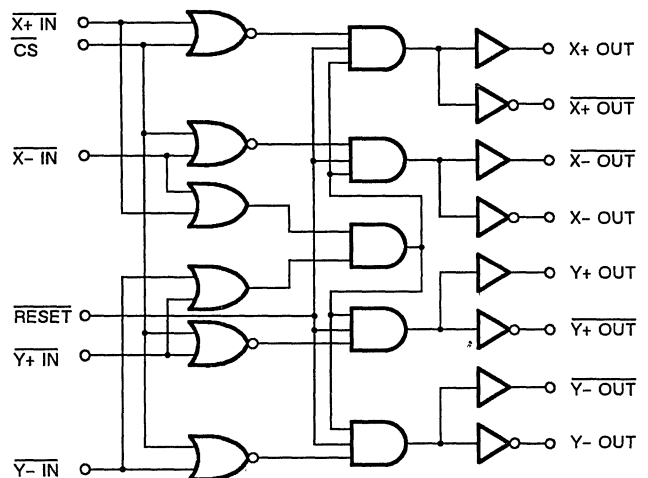
### PIN CONFIGURATION



Top View

Order Number: SI7250CK

### FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias ..... -20 to 80°C  
 Storage Temperature ..... -65 to 150°C  
 Voltage On Any Pin with Respect to Ground ..... -0.5 to  $V_{DD} + 0.5$  V  
 Supply Voltage,  $V_{DD}$  ..... -0.5 to +14 V

Output Current ..... 250 mA  
 ..... (One Output @ 100% Duty Cycle)  
 Maximum Operating Junction Temperature 150°C  
 $\theta_{JC} = 25^\circ\text{C/W}$   
 $\theta_{JA} = 75^\circ\text{C/W}$  (No Airflow)  
 Operating Temperature ..... 0 to 70°C  
 Storage Temperature ..... -65 to 150°C

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 12\text{ V} \pm 10\%$	LIMITS				UNIT
			1=25°C 2=70°C 3=0°C		C SUFFIX 0 to 70°C		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>							
Input Current	$ I_{IN} $	$V_I = 0.8\text{ V}$	1,2,3			10	$\mu\text{A}$
Low Level Input Voltage	$V_{IL}$		1,2,3			0.8	V
High Level Input Voltage	$V_{IH}$		1,2,3		2.2		
<b>OUTPUT</b>							
Output Low Voltage	$V_{OL1}$	$I_{OL} = 100\text{ mA}$	1,2,3	1.45		2	V
	$V_{OL2}$	$I_{OL} = 10\text{ mA}$	1,2,3	0.1		0.2	
Output High Voltage	$V_{OH1}$	$I_{OH} = -100\text{ mA}$	1,2,3	$V_{DD} - 1.4$	$V_{DD} - 2$		
	$V_{OH2}$	$I_{OH} = -10\text{ mA}$	1,2,3	$V_{DD} - 0.1$	$V_{DD} - 0.2$		
Output Sink Current	$I_{OL}$	$V_{OL} = 2\text{ V}$ , 30% Duty Cycle	1,2,3			100	mA
Output Source Current	$ I_{OH} $	$V_{OH} = V_{DD} - 2\text{ V}$ , 30% Duty Cycle	1,2,3			100	
<b>DYNAMIC</b>							
Propagation Delay from $X+ IN$ , $X- IN$ , $Y+ IN$ , $Y- IN$	$t_p$	500 pF Load	1,2,3	55		100	ns
Propagation Delay from $\overline{CS}$ or $\overline{RESET}$	$t_p$		1,2,3	90		150	
Rise Time (10% to 90%)	$t_r$		1,2,3	25		45	

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = \pm 10\%$	LIMITS				UNIT
			1=25 °C 2=70 °C 3=0 °C		C SUFFIX 0 to 70 °C		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>							
Fall Time (90% to 10%)	$t_f$	500 pF Load	1,2,3	25		45	ns
Skew Between an Output and Its Complement	$t_s$		1,2,3	10		20	
Input Capacitance	$C_{in}$		1,2,3			10	pF
<b>SUPPLY</b>							
Supply Current	$I_{DD0}$	Chip Deslected $\overline{CS} = V_{IH}, V_{DD} = 12.6 V$	1,2,3	1		4.5	mA
	$I_{DD1}$	$f = 100 kHz, V_{DD} = 12.6 V$ Output Unloaded	1,2,3			75	
	$I_{DD2}$	$f = 200 kHz, V_{DD} = 12.6 V$ Output Unloaded	1,2,3			90	

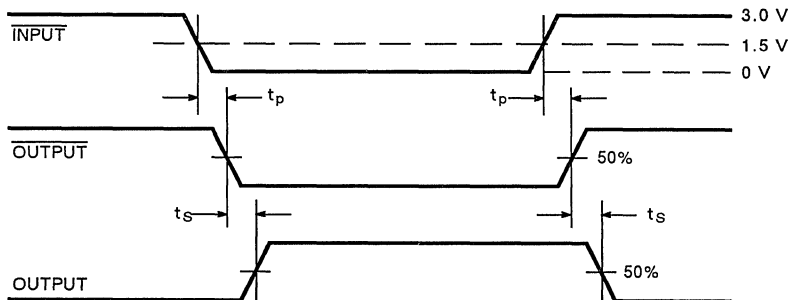
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

---

**AC TEST CONDITIONS**

---



**PIN DESCRIPTION**

**CS (Pin 1)**

Chip select is active low. When high, chip is deselected and I<sub>DD</sub> is significantly reduced. Chip Select is most commonly used for system expansion.

**RESET (Pin 2)**

Active low input from RESET.OUT of the controller results in removal of power from the chip so that bubble memory is protected in the event of power supply failure.

**X+ IN, X- IN (Pins 3, 4)**

Active low inputs from controller which turn ON the high current X outputs.

X- OUT, X- OUT, X+ OUT, X+ OUT (Pins 12-15)  
High current outputs and their complements for driving the gates of the VQ7254 QUAD MOSPOWER FETs which in turn drive the X coils of the bubble memory.

**Y+ IN, Y- IN (Pins 5, 6)**

Active low inputs from controller which turn on the high current Y outputs.

**Y- OUT, Y+ OUT, Y+ OUT, Y- OUT (Pins 9-11 and 7)**

High current outputs and their complements for driving the gates of the VQ7254 QUAD MOSPOWER FETs which in turn drive the Y coils of the bubble memory.

**TRUTH TABLE**

INPUT PINS						OUTPUT PINS								
1 CS	2 R	3 X+	4 X-	5 Y+	6 Y-	7 Y-	9 Y-	10 Y+	11 Y+	12 X-	13 X-	14 X+	15 X+	
1	X	X	X	X	X	0	1	0	1	0	1	0	1	
X	0	X	X	X	X	0	1	0	1	0	1	0	1	
8 INPUT STATES DECODED														
0	1	0	1	0	1	0	1	1	0	0	1	1	0	
0	1	0	1	1	0	1	0	0	1	0	1	1	0	
0	1	0	1	1	1	0	1	0	1	0	1	1	0	
0	1	1	0	0	1	0	1	1	0	1	0	0	1	
0	1	1	0	1	0	1	0	0	1	1	0	0	1	
0	1	1	0	1	1	0	1	0	1	1	0	0	1	
0	1	1	1	0	1	0	1	1	0	0	1	0	1	
0	1	1	1	1	0	1	0	0	1	0	1	0	1	
The 8 remaining input states are not decoded resulting in a reset output condition. This is to prevent the inadvertent shorting of any power drivers directly across the supplies in a standard bubble memory configuration.														
0	1	0	0	0	0	0	1	0	1	0	1	0	1	
0	1	0	0	0	1	0	1	0	1	0	1	0	1	
0	1	0	0	1	0	0	1	0	1	0	1	0	1	
0	1	0	0	1	1	0	1	0	1	0	1	0	1	
0	1	0	1	0	0	0	1	0	1	0	1	0	1	
0	1	1	0	0	0	0	1	0	1	0	1	0	1	
0	1	1	1	0	0	0	1	0	1	0	1	0	1	
0	1	1	1	1	1	0	1	0	1	0	1	0	1	

# Chopper-Stabilized Operational Amplifier

## FEATURES

- Ultra-Low Input Offset Voltage ( $V_{OS} < 5 \mu V$ )
- Low Input Bias Current ( $I_B < 30 \text{ pA}$ )
- Low Drift ( $TC_{VOS} < 50 \text{ pV}/^\circ\text{C}$ )
- Low Noise ( $e_n < 0.2 \mu V_{p-p}$ )
- High Open-Loop Gain ( $A_{VOL} > 120 \text{ dB}$ )

## BENEFITS

- Improved System Accuracy
- Reduces Loading of High Z Sources
- Eliminates Trims for Offset and Drift
- Improves Input Resolution
- Reduces Linearity Errors in High Gain Designs

## APPLICATIONS

- Precision Amplifiers
- High Impedance Transducer Amplifiers
- Remote High Resolution Systems
- Integrating A/D Preamplifiers
- Low Level Signal Sensing

## DESCRIPTION

The Si7652 is a chopper-stabilized operational amplifier designed to achieve virtually zero change in voltage offset ( $V_{OS}$ ) with both temperature and time. By freeing the design from costly potentiometer adjustments, overall circuit reliability and performance are greatly enhanced.

There are two versions of the Si7652. The 8-lead versions rely on the internal 400 Hz oscillator to run the chopper, while the 14-lead versions allow the user to connect an external oscillator for specialized applications where synchronization may be desirable. The 14-lead version also allows for the connection of an output voltage clamp circuit to minimize overload recovery time.

With a low maximum input offset voltage of  $5 \mu V$  and a low drift of  $50 \text{ pV}/^\circ\text{C}$  (maximum), the Si7652

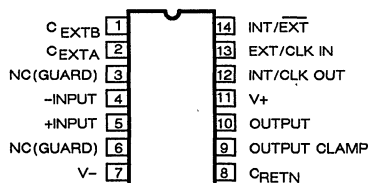
is ideal for high-resolution signal conditioning. Its low drift over time and temperature benefits remote systems where recalibration is difficult and/or costly.

Built on the Siliconix proprietary PolyMOS™ process, Si7652 also features low bias and offset current errors, and has been designed to minimize the charge injection errors normally associated with chopper designs.

Package options include the 8-lead metal can and MINIDIP, and the 14-lead plastic and ceramic DIP. Operation is specified over the industrial, D suffix ( $-40$  to  $85^\circ\text{C}$ ) temperature range.

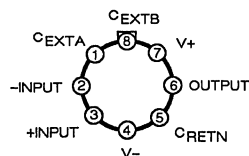
For more information on the Si7652, please refer to Siliconix Application Note AN87-4.

## PIN CONFIGURATION

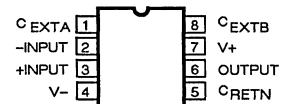


Order Numbers:

CerDIP: SI7652DK  
Plastic: SI7652DJ

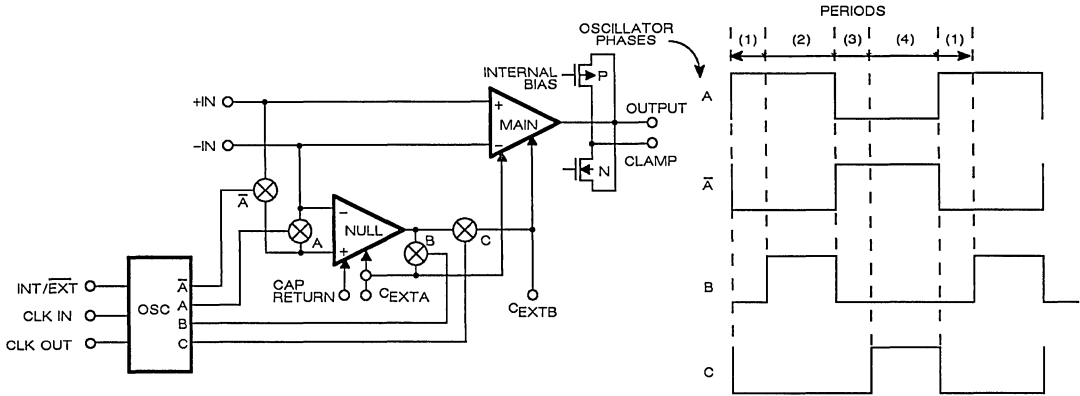


Order Number:  
SI7652DA



Order Number:  
SI7652DH

**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage ( $V_+$  to  $V_-$ ) ..... 18 V  
 Input Voltage ..... ( $V_-$ ) -0.3 to ( $V_+$ ) +0.3 V  
 Oscillator Control Voltage .....  $V_+$  to  $V_-$   
 Current, Any Terminal ..... 10 mA  
 Current, Any Terminal (while operating)<sup>h</sup> ..... 100  $\mu$ A  
 Duration of Output Short Circuit ..... Indefinite  
 Storage Temperature ..... -65 to 150°C  
 (J, H Package) ..... -65 to 125°C

Operating Temperature (D Suffix) ..... -40 to 85°C

Power Dissipation (Package)\*  
 16-Pin DIP\*\* ..... 900 mW  
 16-Pin Plastic DIP\*\*\* ..... 470 mW  
 Metal Can\*\*\*\* ..... 450 mW

\* All leads soldered or welded to PC Board.  
 \*\* Derate 12 mW/°C above 75°C.  
 \*\*\* Derate 6.5 mW/°C above 25°C.  
 \*\*\*\* Derate 6 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 5\text{ V}$ $V_- = -5\text{ V}$ (See Test Circuit, Figure 1)	LIMITS				UNIT
			1=25 °C 2=85 °C 3=-40 °C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>							
Input Offset Voltage	$V_{OS}$		1	$\pm 0.7$	-5	5	$\mu$ V
Input Bias Current	$I_B$		1 2,3	$\pm 15$ $\pm 100$	-30	30	pA
Input Offset Current	$I_{OS}$		1	$\pm 25$	-60	60	
Offset Voltage Tempco <sup>e</sup>	$TC_{VOS}$		1,2,3	10		50	nV/°C
Input Resistance	$R_{IN}$		1	$10^{12}$			$\Omega$

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 5\text{ V}$ $V_- = -5\text{ V}$ (See Test Circuit, Figure 1)	LIMITS				UNIT
			1=25 °C 2=85 °C 3=-40 °C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT (Cont'd)</b>							
Input Noise Voltage	$e_n$	$R_S = 100\Omega$ , DC to 1 Hz	1	0.2			$\mu\text{V}_{\text{p-p}}$
		DC to 10 Hz	1	0.7			
Input Noise Current	$I_n$	$f = 10\text{ Hz}$	1	0.01			$\text{pA}/\sqrt{\text{Hz}}$
<b>DYNAMIC</b>							
Common-Mode Voltage Range <sup>h</sup>	CMR		1		-4.3	3.5	V
Common-Mode Rejection Ratio	CMRR	Within CMR	1	130	110		dB
Power Supply Rejection Ratio	PSRR	$\pm 3\text{ V}$ to $\pm 8\text{ V}$	1	130	110		
Internal Chopping Frequency <sup>f</sup>	$f_{\text{CH}}$		1	400			Hz
Clamp ON Current <sup>g</sup>		$R_L = 100\text{ k}\Omega$	1	100	25		$\mu\text{A}$
Clamp OFF Current <sup>g</sup>		$-4.0\text{ V} < V_{\text{OUT}} < 4.0\text{ V}$	1	1			pA
Output Voltage <sup>e</sup>	$V_{\text{OUT}}$	$R_L = 10\text{ k}\Omega$	1	$\pm 4.85$	-4.7	4.7	V
		$R_L = 100\text{ k}\Omega$	1	$\pm 4.95$			
Open-Loop Voltage Gain	$A_{\text{VOL}}$	$R_L = 10\text{ k}\Omega$ , $V_{\text{OUT}} = \pm 4\text{ V}$	1	150	120		dB
Unity-Gain Bandwidth	GBW		1	0.45			MHz
Slew Rate	SR	$C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$	1	0.5			$\text{V}/\mu\text{s}$
Rise Time	$t_r$		1	0.8			$\mu\text{s}$
Overshoot			1	20			%
<b>SUPPLY</b>							
$V_+$ to $V_-$ Range	$V_S$		1		5	16	V
Supply Current	$I_S$	$R_L = \infty$	1	2.0		35	mA

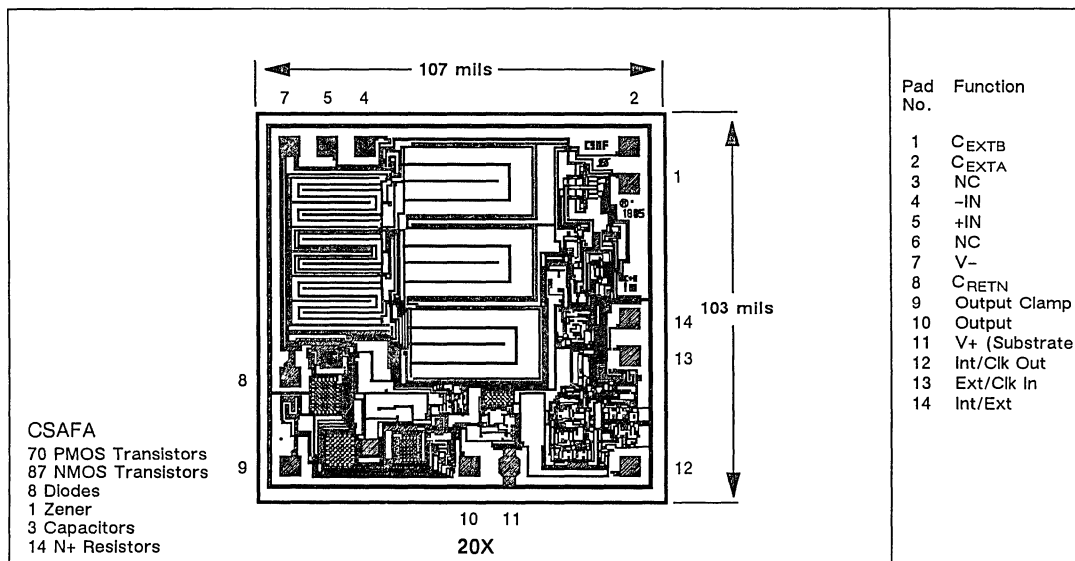


**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

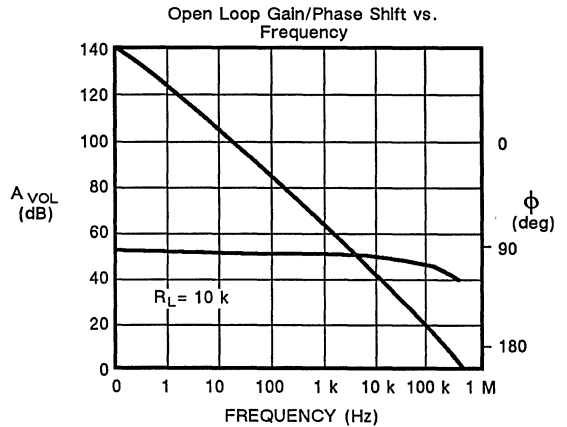
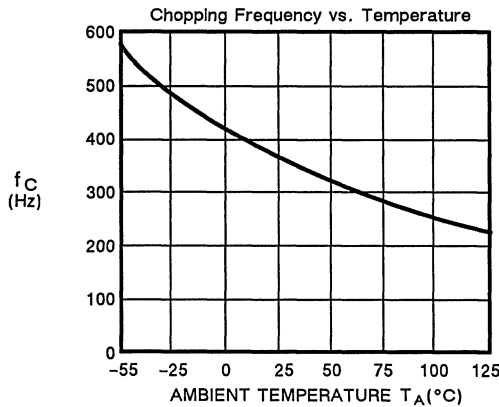
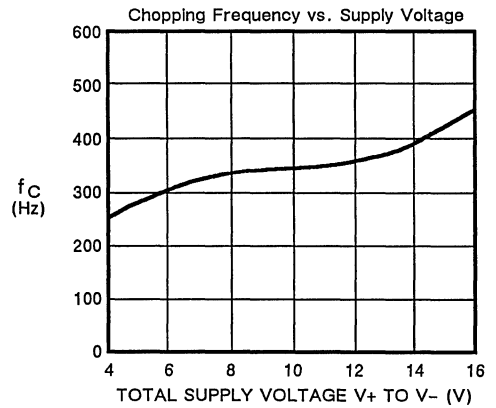
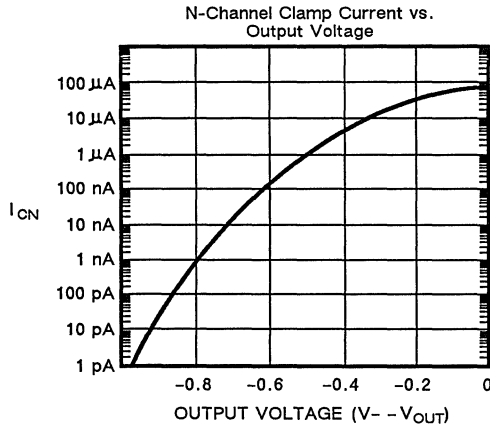
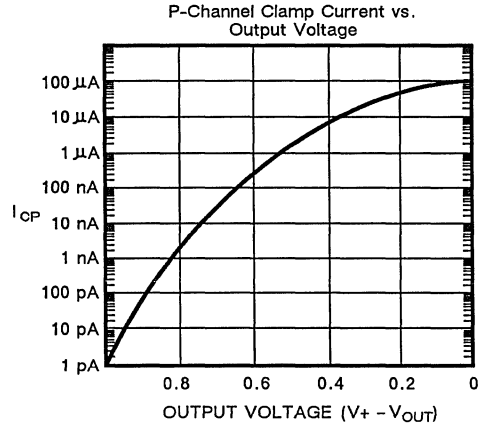
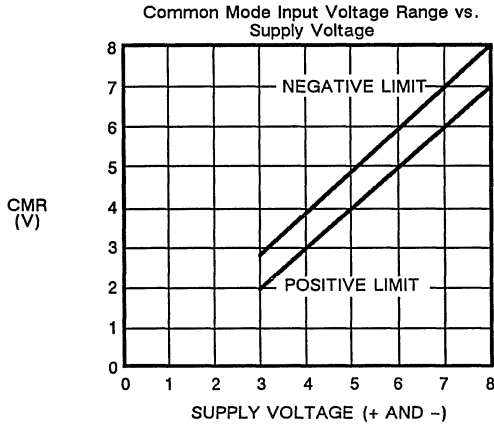
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Output clamp not connected.
- f. Pins 12 through 14 open (DIP packages only).
- g. See Output CLAMP under DETAILED DESCRIPTION.
- h. Limiting input current to 100  $\mu$ A is recommended to avoid latch-up problems.

**DIE TOPOGRAPHY**

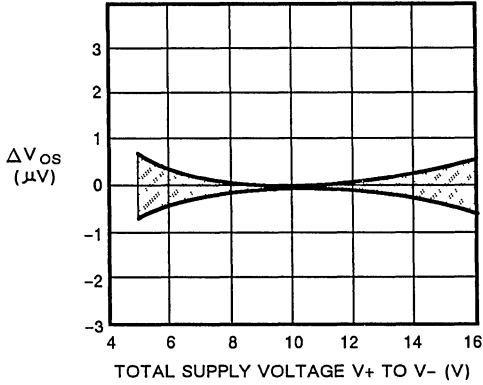


## TYPICAL CHARACTERISTICS

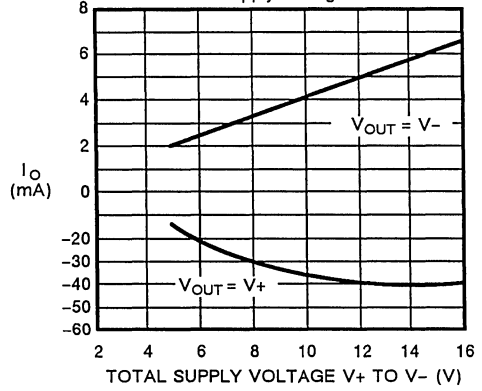


**TYPICAL CHARACTERISTICS**

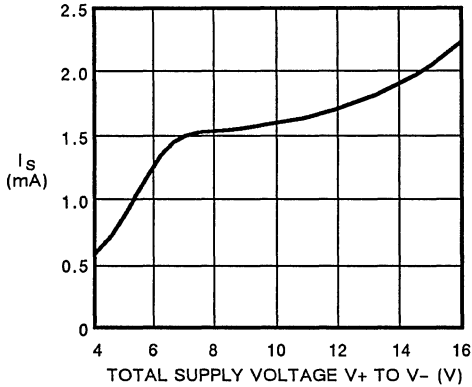
Input Offset Voltage Change vs. Supply Voltage



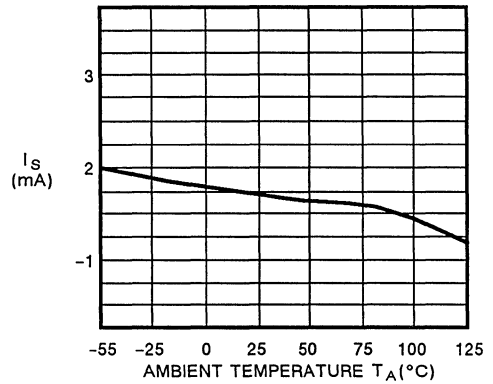
Maximum Output Current vs. Supply Voltage



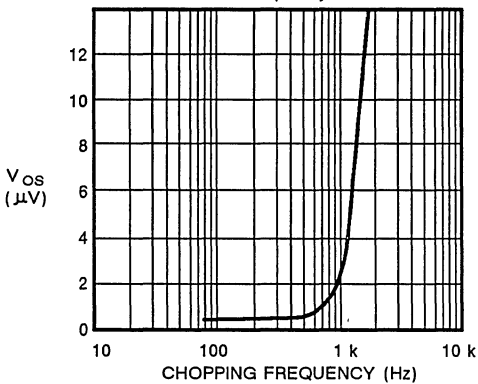
Supply Current vs. Supply Voltage



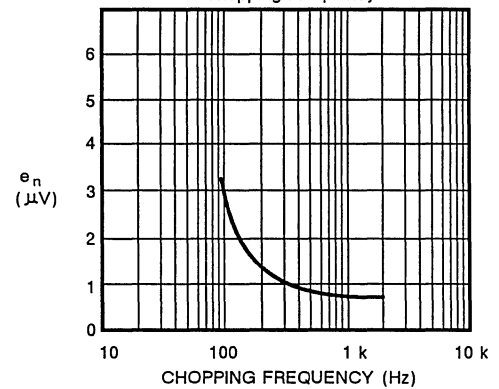
Supply Current vs. Temperature



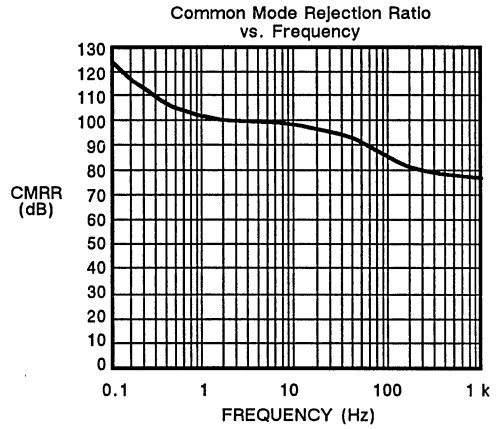
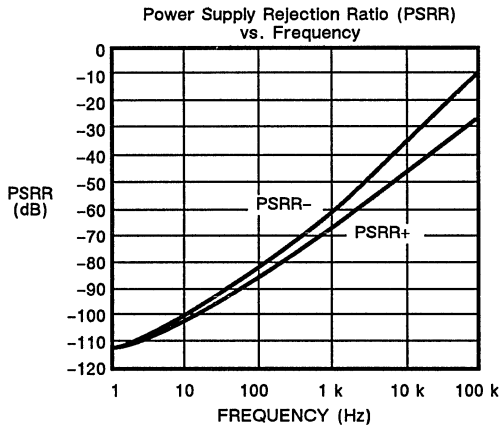
Input Offset Voltage vs. Chopping Frequency



DC to 10 Hz P-P Noise Voltage vs. Chopping Frequency



## TYPICAL CHARACTERISTICS



## TEST CIRCUIT

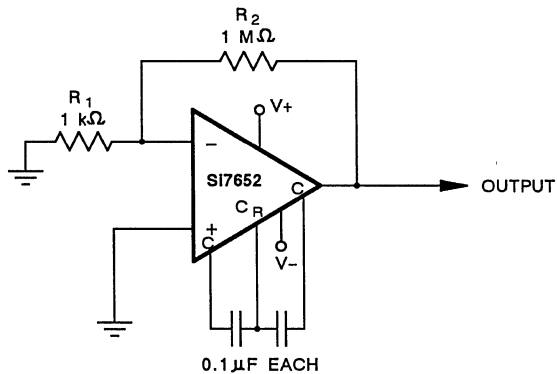


Figure 1.

## DETAILED DESCRIPTION

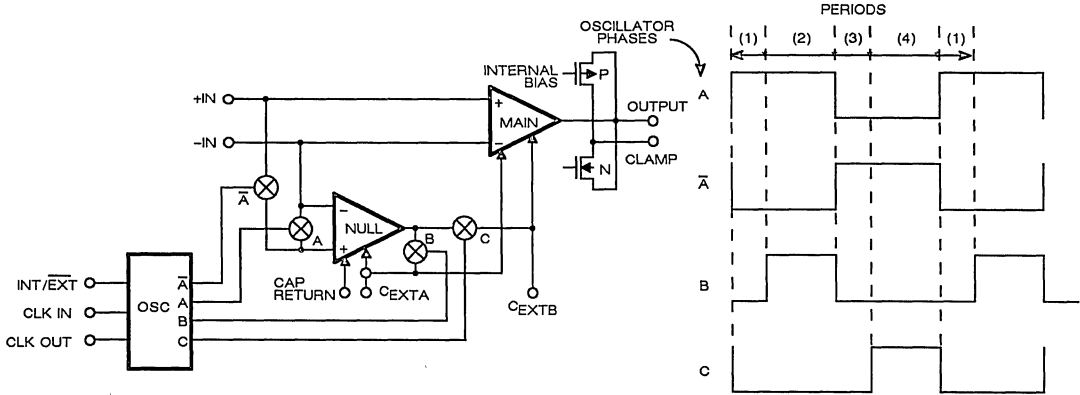
### Circuit Operation

A block diagram of the chopper stabilized amplifier is shown in Figure 2. The main amplifier is connected directly to the output. The nulling amplifier, which is controlled by the oscillator/clock circuit, alternates between nulling itself and the main amplifier. The nulling potentials are stored in the external nulling capacitors. The nulling circuitry

works independent of signal level, and functions over the entire power supply and common mode range.

Charge injection at the input terminals is minimized by careful design in the input switches. Feedthrough injection, which is the main cause of chopping spikes in the output, is also minimized.

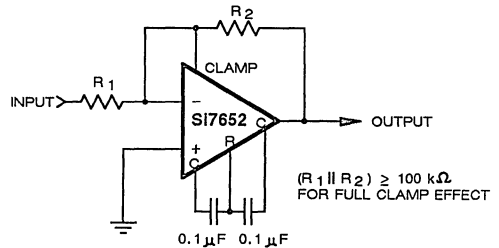
**DETAILED DESCRIPTION (Cont'd)**



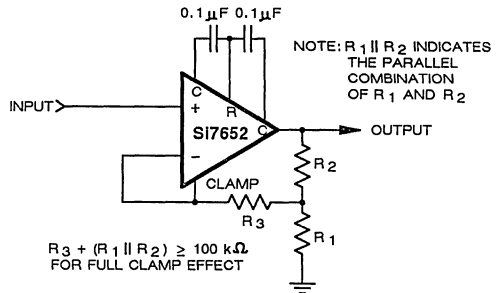
**Figure 2. Functional Block Diagram**

**Output Clamp**

Overload recovery can be a significant problem in chopper stabilized designs. This is because the time constant of the filter at the output of the nulling amplifier can be measured in minutes. If the output goes to either of the supply rails, the inputs are no longer at "virtual ground". The nulling amplifier sees the differential voltage at the input as an error and tries to correct it, saturating the nulling circuit. Therefore, it is appropriate to clamp the output of the main amplifier to insure that there is a low impedance current feedback path to the summing (inverting) input of the amplifier before the output reaches either supply rail. For best results, the clamp resistance should be greater than 100 kΩ. Output clamping does reduce the output swing slightly. Figure 3 shows the Si7652 in inverting and noninverting clamped amplifier circuits.



**Figure 3(a). Inverting Amplifier with Clamp**



**Figure 3(b). Non-Inverting Amplifier with Clamp**

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**DETAILED DESCRIPTION (Cont'd)**

---

**Clock**

The nominal operating frequency of the internal clock/oscillator is 400 Hz. Although the clock is not adjustable on the 8-pin versions of the Si7652, the 14-pin versions allow selection of either internal or external clocking. The INT/ $\overline{\text{EXT}}$  pin should be left floating for use with the internal clock, or tied to V<sub>-</sub> if an external clock signal is applied to the EXT CLK IN pin. The duty cycle of the external clock is not important at lower frequencies because the internal oscillator circuitry provides a 50% switching duty cycle. When operating at frequencies above 500 Hz, a 50% to 80% positive duty cycle is preferred because the nulling capacitors are charged only when EXT CLK IN is high. The external clock can swing between either V<sub>+</sub> and GND or V<sub>+</sub> and V<sub>-</sub> since the logic threshold is approximately 2.5 V below V<sub>+</sub>.

To avoid capacitor imbalance during an overload, a strobe signal may be applied to EXT CLK IN. Neither capacitor will be charged if the strobe signal is low during the time that the overload is applied.

**Component Selection**

The only external components required by the Si7652 are two nulling capacitors. The correct value for the capacitors when using the internal 400 Hz oscillator can be anywhere between 0.1 and 1  $\mu\text{F}$ . Capacitors toward the 1  $\mu\text{F}$  value will allow minimum clock noise in broadband applications, while capacitors toward the 0.1  $\mu\text{F}$  value will provide lower offset in limited bandwidth applications. When using an external clock, the capacitors should be scaled proportionally to the relationship of the chopping frequency to the nulling time constant.

Low grade capacitors such as ceramic are satisfactory for most applications. However, film capacitors are preferred. Low dielectric absorption capacitors such as polypropylene will yield the lowest settling at turn-on. Ceramic capacitors may take as long as several seconds to settle to within 1  $\mu\text{V}$ .

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**APPLICATIONS**

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**Output Loading**

The Si7652 is similar to a transconductance amplifier in that the open loop gain is proportional to load resistance. This phenomenon becomes important when the load impedance is lower than the typical 18 k $\Omega$  output impedance of the device. For example, the open loop gain will be 17 dB lower with a 1 k $\Omega$  load than with a 10 k $\Omega$  load. This has little importance if the amplifier is used only in DC applications, since the DC gain is typically better than 120 dB even with a 1 k $\Omega$  load. However, the best wideband frequency response will occur with a load resistor of 10 k $\Omega$  or higher. The response will be 20 dB per decade from 0.1 Hz to 500 kHz, with phase shifts of less than 2 degrees in the transition region where the main amplifier takes over from the null amplifier.

**Thermo-Electric Effects**

Thermo-electric effects developed in thermocouple junctions of dissimilar materials ultimately limit precision DC measurements. Unless all junctions are at the same temperature, thermoelectric voltage from 0.1 to as high as 20-30  $\mu\text{V}/^\circ\text{C}$  will be generated. In order to realize the extremely low

offset voltages that the Si7652 can provide it is essential to take special precautions to avoid temperature gradients. All components should be shielded from air movement, especially that caused by power dissipating elements. Power supply voltages and power dissipation should be kept to a minimum, and low thermo-electric coefficient connections should be used where possible. Separation from surrounding heat dissipating elements is advised, and high impedance loads are preferable.

**Latch-up**

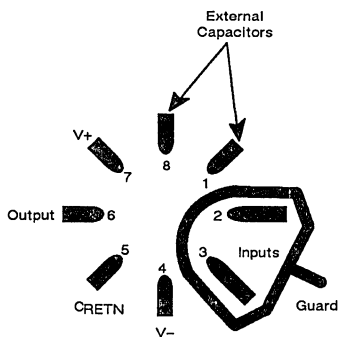
A parasitic four-layer SCR structure is a characteristic of all junction-isolated CMOS devices. SCR action can occur under certain circumstances, drawing excessive supply current and possibly destroying the device. To avoid this condition, no voltages greater than 0.3 V beyond the supply rails should be applied to any pin. The power supplies should be established either at the same time as or before any input signals are applied. If this is not possible, the input current must be limited to less than 1 mA to avoid latch-up during the fault condition.

**APPLICATIONS (Cont'd)**

**Input Guarding**

To fully realize the low leakage inputs of the Si7652, special care must be taken in layout and preparation of the printed circuit board. All contamination must be cleaned away with alcohol or TCE and compressed air, and the assembled board should be sealed to prevent recontamination in the future.

Even proper cleaning cannot stop all leakages since the inputs of the amplifier are adjacent to terminals that carry supply potentials. This can be reduced by placing a guard ring around the input terminals. The 14-pin package has the pins on either side of the inputs unconnected to ease the layout of the guard. An 8-pin metal can should be laid out using a 10-pin socket pattern. The two extra pins are situated one on each side of the inputs to facilitate guarding (see Figure 4(a)). The guard ring should be connected to a low-impedance point that is roughly the same voltage as the inputs. Leakages from the adjacent pins are absorbed by the guard. Figure 4(b) gives typical guarding connections.



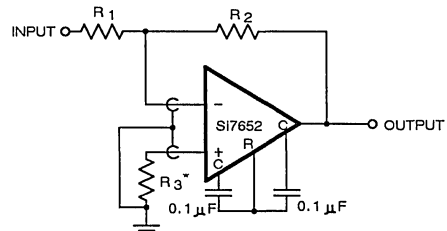
Bottom View  
Board layout for input guarding with TO-99 package.

Figure 4(a). Board layout for input guarding with TO-99 package

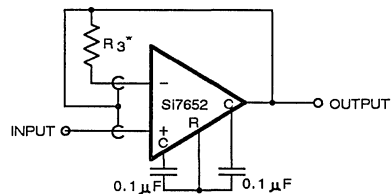
**Pin Compatibility**

The 8-pin versions of the Si7652 have been laid out to correspond with the pin-out of industry standard 8-pin devices. The only difference is the connection of the nulling capacitors to pins 1 and 8, normally used for offset nulling on other op amps.

OP-05 and OP-07 op amp circuits can also be converted to the Si7652. This is done by replacing

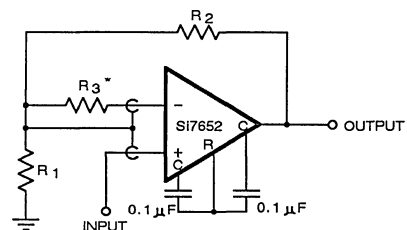


INVERTING AMP



FOLLOWER

\* USE R<sub>3</sub> TO COMPENSATE FOR LARGE SOURCE RESISTANCES, OR FOR CLAMP OPERATION (SEE FIGURE 3)



NOTE:  $\frac{R_1 R_2}{R_1 + R_2}$  SHOULD BE LOW IMPEDANCE FOR OPTIMUM GUARDING

NON-INVERTING AMPLIFIER

Figure 4(b). Typical Guarding Connections

the offset-null potentiometer between pins 1, 8, and V+ by two capacitors from those pins to V-. For LM108 substitution, the compensation capacitor is replaced by the external nulling capacitors.

**Typical Applications**

The Si7652 will find use wherever improved offset and bias current are required. In basic inverting (Figure 5) and noninverting (Figure 6) configurations, the only limitations are the supply voltage ( $\pm 8$  V max.) and the output drive capability (10 k load min). These limitations can be bypassed by the use of an output boost circuit as shown in Figure 7.

## APPLICATIONS (Cont'd)

Because the combination of the two op amps form a composite amplifier, the loop gain stability should be checked carefully when the feedback network is added.

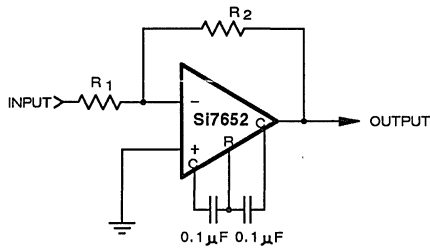


Figure 5. Inverting Amplifier

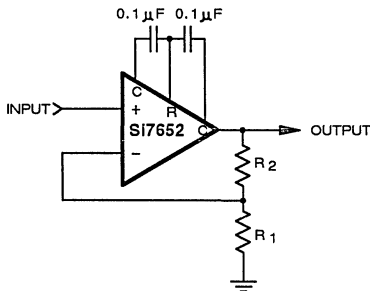


Figure 6. Non-Inverting Amplifier

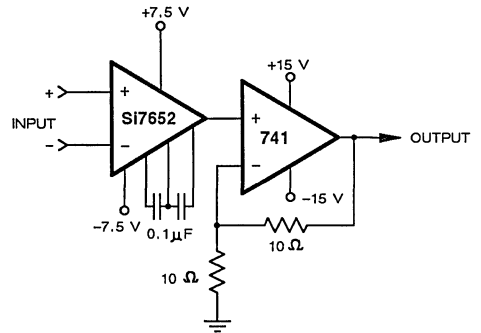


Figure 7. Using the 741 to Boost the Output of the Si7652

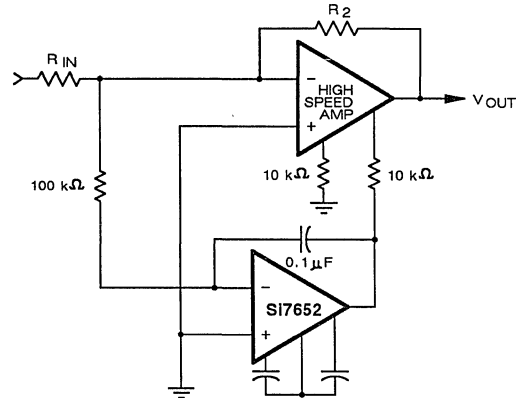


Figure 8. Nulling a High Speed Op-Amp



## Ring Demodulator/ Balanced Mixer

### FEATURES

- Low ON Resistance
- < 2% Device Matching Error
- High Third Order Intercept Point (+35 dB)

### BENEFITS

- Usable to 250 MHz
- Low Harmonic Distortion
- Wide Dynamic Range

### APPLICATIONS

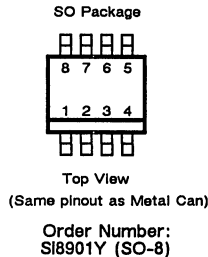
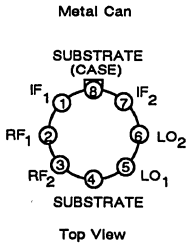
- RF Mixers
- CATV Encoders and Decoders
- Modulators
- Demodulators
- Phase Sensitive Detectors
- Pagers

### DESCRIPTION

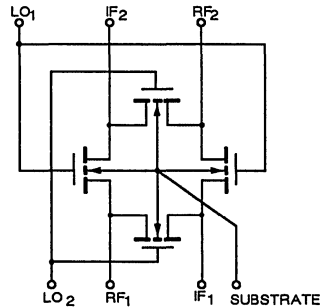
The Si8901 Ring Demodulator/Balanced Mixer offers significant improvements for RF mixer applications where low third order harmonic distortion has been a problem. Combining matching with very low junction capacitance, (< 3 pF), low ON resistance (30  $\Omega$ ) and very high OFF resistance (>  $10^9 \Omega$ ), the

Si8901 accepts an RF and a local oscillator (LO) input and provides a high fidelity IF output with typical conversion loss of -8 dB at frequencies up to 200 MHz. Available in an 8-pin TO-78 and SO-8 package, this device is specified over -25 to 85°C temperature range.

### PIN CONFIGURATION

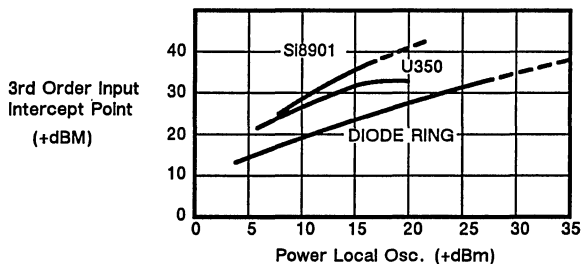


### FUNCTION BLOCK DIAGRAM



**8**

### PERFORMANCE COMPARISON



## ABSOLUTE MAXIMUM RATINGS

$V_{DS}$ Drain to Source .....	15 V	$V_{GD}$ Gate to Drain .....	-22.5 V to 30 V
$V_{DB}$ Drain to Substrate .....	22.5 V	$I_D$ Drain Current .....	50 mA
$V_{SB}$ Source to Substrate .....	22.5 V	Operating Temperature .....	-25 to 85°C
$V_{GS}$ Gate to Source .....	-22.5 V to 30 V	Storage Temperature .....	-65 to 150°C
$V_{GB}$ Gate to Substrate .....	-0.3 V to 30 V	Power Dissipation (A Package)* .....	640 mW
		* Derate 5 mW/°C above 25°C.	

ELECTRICAL CHARACTERISTICS <sup>a</sup>				T <sub>A</sub> = 25°C				
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS				UNIT	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>STATIC</b>								
Drain-Source Breakdown Voltage	$V_{(BR)DS}$	$V_{GS} = V_{SB} = -5$ V $I_S = 10$ nA		25	15			
Source-Drain Breakdown Voltage	$V_{(BR)SD}$	$V_{GD} = V_{DB} = -5$ V $I_D = 10$ nA			15			
Drain-Substrate Breakdown Voltage	$V_{(BR)DB}$	Source Open $V_{GB} = 0$ V, $I_D = 10$ nA			22.5		V	
Source-Substrate Breakdown Voltage	$V_{(BR)SB}$	Drain Open $V_{GB} = 0$ V, $I_D = 10$ nA			22.5			
Threshold Voltage	$V_T$	$V_{DS} = V_{GS} = V_T$ $I_S = 1$ μA, $V_{SB} = 0$ V		1	0.1	2.0		
Drain-Source "ON" Resistance	$r_{DS(ON)}$	$I_D = 10$ mA $V_{SB} = 0$ V	$V_{GS} = 5$ V		50		75	Ω
			$V_{GS} = 10$ V		30			
			$V_{GS} = 15$ V		23			
			$V_{GS} = 20$ V		19			
Resistance Matching	$\Delta r_{DS(ON)}$		$V_{GS} = 5$ V		3		7	
<b>DYNAMIC</b>								
LO <sub>1</sub> - LO <sub>2</sub> Capacitance	$C_{gg}$	$V_{DS} = 0$ V, $V_{BS} = -5.5$ V $V_{GS} = 4$ V			4.4		pF	
Conversion Loss	$L_c$	See Figure 1, P <sub>LO</sub> = +17 dBm			8		dB	
Third Order Intercept <sup>c</sup>	IMD <sub>3</sub>				+35			
Maximum Operation Frequency	$f_{MAX}$				250		MHz	

### NOTES:

- Refer to PROCESS OPTION FLOWCHART for additional information.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

**APPLICATION HINTS**

Schematic of the basic commutation-type HF double-balanced mixer using resonant-gate excitation. Recommended reading is AN85-2 "A Commutation Double-Balanced MOSFET Mixer of High Dynamic Range."

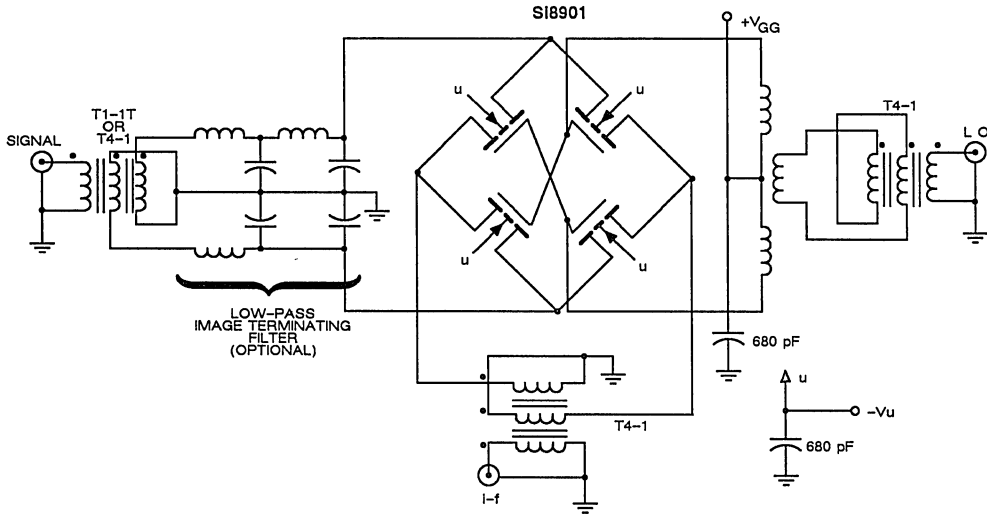


Figure 1.

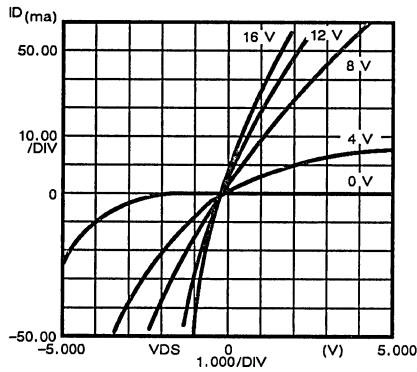


Figure 2. First and Third Quadrant I-E Characteristics Showing Effect of Gate Voltage Leading to Large-Signal Overload Distortion







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Si9560: Electroluminescent Symmetric Row Driver .....	9-27

# DISPLAY DRIVERS

## INTRODUCTION

Ever since the invention of the CRT, designers have looked for smaller, more rugged alternatives. Today, many flat panel technologies are gaining a significant share of the information display market with their compactness (often less than .5 inches thick), their rugged, solid-state construction, and their low power consumption. These display technologies are of particular interest to the military and portable computer markets, where the above criteria are most important.

Siliconix began its association with flat-panel displays by supplying 7-segment LCD drivers for use with digital panel meters. More recently, Siliconix has used its high-voltage D/CMOS power IC process to supply display drivers to Electroluminescent (EL) display manufacturers. Row and column drivers for flat panel displays are supplied for a wide range of applications from commercial desktop computers to military avionics control panels. Siliconix drivers are also specified in plasma, vacuum fluorescent, and LCD applications due to their high performance characteristics.

The Si9551 and Si9552 are first-generation open-drain row drivers designed for driving the row electrodes of electroluminescent graphics display panels. When combined with either the Si9553 and Si9554 (60 V), or the Si9555 and Si9556 (80 V) column drivers, they provide the interface between logic-level video control circuitry and the high-voltage display panel.

The Si9560 is a second-generation row driver designed to give higher performance and longer life to AC TFEL (Thin Film EL) panels. It features a bi-directional shift register so that only one part is required for both sides of the panel, and 225 V, 100 mA push-pull outputs to maximize brightness and minimize latent imaging.

The DF412 is a four digit liquid crystal display decoder/driver IC containing all of the necessary circuitry to decode up to four digits of multiplexed BCD information and derive the ac signals required to directly drive a four-digit seven-segment liquid crystal display.

## 4-Digit LCD Decoder/Driver

### FEATURES

- Decodes up to 4 7-segment BCD Digits
- Interfaces with Most Logic Families
- On Chip Oscillator
- Low Power Consumption (1.5 mW typ.)
- Digit Blanking

### BENEFITS

- Reduces Complexity
- Eliminates DC Bias Levels That Shorten Display Lifetime
- One External Component
- No Display Buffering Required

### APPLICATIONS

- Driving Liquid Crystal Displays
- Digital Multimeters
- Flowmeter Digital Readouts
- Portable Instruments

### DESCRIPTION

The DF412 4-digit LCD Decoder Driver is a CMOS Monolithic device employing multiplexed BCD to LCD Decoding. A single DF412 contains all of the circuitry needed to decode up to 4 digits of multiplexed BCD information and derive the AC signals needed to directly drive a 4-digit LCD display. To eliminate leading zeroes, a BCD input of 1111 blanks a digit.

An internal oscillator, its frequency being controlled by an external capacitor, develops a backplane signal (BP) that is a square wave swinging between ground ( $V_{SS}$ ) and the positive supply ( $V_{DD}$ ). Segment drivers supply square waves of the same frequency as the backplane but either in phase for an OFF segment or out of phase for an ON

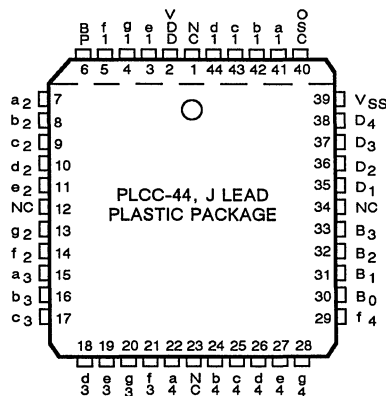
segment. In this manner, the net DC potential applied between segment and backplane is zero, a necessary requirement for long display life.

Digital input levels are defined as input voltages  $> 4$  V being a logic "1" and input voltages  $< 0.8$  V being a logic "0" with  $V_{DD} = 5$  V.

BCD input data is decoded into 7-segment form using an on board ROM. The 7-segment data is then latched into the appropriate static latches via the digit strobe inputs and control logic.

The pinout of the DF412 allows easy PC board interface to dual-in-line LCDs as well as edge connecting types of displays. The DF412 is available in the PLCC-44 package for industrial, D suffix ( $-40$  to  $85^{\circ}\text{C}$ ) temperature range operation.

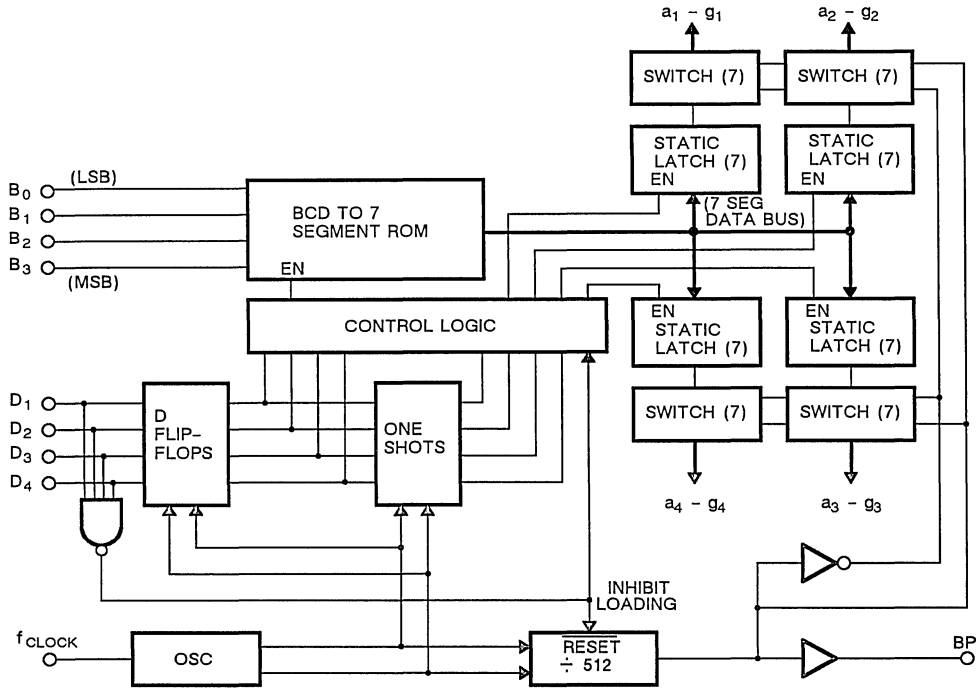
### PIN CONFIGURATION



Order Number:  
DF412DN



**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

$V_{DD} - V_{SS}$  ..... -0.3 V to 8 V  
 Voltage on Any Pin .....  $V_{SS} - 0.3$  V to  $V_{DD} + 0.3$  V  
 Current at Any Pin ..... 10 mA  
 Operating Temperature (D suffix) ..... -40 to 85°C

Storage Temperature ..... -65 to 125°C  
 Power Dissipation\* ..... 450 mW  
 \* Device mounted with all leads welded or soldered to PC board. Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 5$ V $V_{SS} = 0$ V $C_{osc} = 200$ pF	LIMITS				UNIT
			1 = 25°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>d</sup>	
<b>INPUT</b>							
Digital Input Leakage Current	$I_{IN(DIGITS)}$	$V_{IN} = 5$ V	1	0.01		1	μA
Oscillator Input Current	$I_{IN(CLK)}$	$V_{IN} = 5$ V	1	350			
		$V_{IN} = 0$ V	1	-350			



ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = 5 V V <sub>SS</sub> = 0 V C <sub>osc</sub> = 200 pF	LIMITS				UNIT
			1 = 25°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT (Cont'd)</b>							
Digital Input Logic LOW Voltage	V <sub>INL</sub>	BCD and DS Inputs	1			0.8	V
		Clock Input	1			0.5	
Digital Input Logic HIGH Voltage	V <sub>INH</sub>	BCD and DS Inputs	1		4		
		Clock Input	1		4.5		
<b>OUTPUT</b>							
Segment Output Voltage in "0" State	V <sub>OL</sub> (Segment)	I <sub>OL</sub> = 250 μA	1	0.3		0.7	V
		I <sub>OL</sub> = 25 μA	1	0.03			
Segment Output Voltage in "1" State	V <sub>OH</sub> (Segment)	I <sub>OH</sub> = -250 μA	1	4.7	4.3		
		I <sub>OH</sub> = -25 μA	1	4.97			
Backplane Output Voltage in "0" State	V <sub>OL</sub> (Backplane)	I <sub>OL</sub> = 5 mA	1	0.3		0.7	
		I <sub>OL</sub> = 0.5 mA	1	0.03			
Backplane Output Voltage in "1" State	V <sub>OH</sub> (Backplane)	I <sub>OH</sub> = -5 mA	1	4.7	4.3		
		I <sub>OH</sub> = -0.5 mA	1	4.97			
<b>DYNAMIC</b>							
Segment Output Rise Time	t <sub>r</sub> (Segments)	C <sub>LOAD</sub> = 200 pF	1	1			μs
Segment Output Fall Time	t <sub>f</sub> (Segments)		1	1			
Backplane Output Rise Time	t <sub>r</sub> (Backplane)	C <sub>LOAD</sub> = 3900 pF	1	0.8			
Backplane Output Fall Time	t <sub>f</sub> (Backplane)		1	0.8			
Backplane Frequency Minimum LCD	f <sub>BP1</sub>	C <sub>osc</sub> = 3800 pF	1	30			Hz
Backplane Frequency Maximum LCD	f <sub>BP2</sub>	C <sub>osc</sub> = 1000 pF	1	100			

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V <sub>DD</sub> = 5 V V <sub>SS</sub> = 0 V C <sub>osc</sub> = 200 pF	LIMITS				UNIT
			1 = 25°C		D SUFFIX -40 to 85°C		
			2 = 85°C	3 = -40°C	MIN <sup>b</sup>	MAX <sup>b</sup>	
			TEMP	TYP <sup>d</sup>			
<b>SUPPLY</b>							
Supply Current Digital Inputs Static	I <sub>DD</sub>	See Figure 2	1	140		400	μA
Supply Current Digital Inputs Dynamic	I <sub>DD</sub>	See Figure 3	1	155			
Operating Supply Voltage <sup>d</sup>	V <sub>DD</sub>		1	5	3.5	6	V

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. Operation over the supply voltage range is functionally tested. The dc and ac parametric testing is performed only at specific test conditions.

**PIN FUNCTION DESCRIPTION**

**OSC (Oscillator)** -- A capacitor connected between the oscillator (OSC) and ground completes the integral clock generator. The frequency of the clock generator (f<sub>OSC</sub>) is determined by the capacitance value and the V<sub>DD</sub> voltage, as seen in Figure 4. For driving LCDs with a 30 Hz to 100 Hz backplane frequency range, the typical oscillator capacitor is 1000 pF to 3800 pF (for V<sub>DD</sub> = 5 V). The oscillator pin can also be driven with an external clock whose output swings within 10% of V<sub>DD</sub> and V<sub>SS</sub>. This is useful when synchronization of more than one DF412 is necessary, such as when driving displays of more than 4 digits on a single backplane.

**BP (Backplane)** -- The backplane of the liquid crystal display is driven by this pin whose output is a squarewave swinging between V<sub>DD</sub> and V<sub>SS</sub>. The frequency of the backplane signal is f<sub>OSC</sub>/512. Most LCDs require backplane frequencies of between 30 Hz and 100 Hz. See Figure 4 for a graph of oscillator capacitance vs. backplane frequency.

**Digit Strobes D<sub>1</sub>-D<sub>4</sub> and BCD Inputs B<sub>3</sub>, B<sub>2</sub>, B<sub>1</sub> and B<sub>0</sub>** -- Multiplexed BCD information is entered into the DF412 by presenting the appropriate BCD code to the inputs B<sub>3</sub>, B<sub>2</sub>, B<sub>1</sub> and B<sub>0</sub> and by pulsing the appropriate digit strobe input D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub>, or D<sub>4</sub> with positive true logic i.e. V<sub>INH</sub> > (0.8 X V<sub>DD</sub> for logic 1,

V<sub>INL</sub> < 0.8 V for logic 0. The minimum pulse width of a digit strobe should be not less than one period of the oscillator frequency. Information presented at the BCD inputs (B<sub>3</sub>, B<sub>2</sub>, B<sub>1</sub>, B<sub>0</sub>) must be valid during the digit strobe pulse. See the timing requirements in Figure 1.

The digit strobe inputs are shaped by the input logic shown in Figure 8a. This logic causes a strobe signal which is a signal clock period wide. The active time of this data load strobe (shown in Figure 8b) enables the BCD to 7-segment decoding ROM, which brings the new 7-segment data to the output latches. Delay time for data to get from BCD input to the segment outputs is typically 2 μs - 3 μs. The end of the data load strobe is triggered by the second negative clock edge following the digit strobe going high. At this edge, the segment outputs are latched, storing the 7-segment information for this digit. This input structure is the basis for the timing requirements of the DF412, shown in Figure 1.

The digit strobe input structure can actually load more than one digit at a time from the same BCD input. The loading of multiple digits can save time for microprocessor applications, such as for zeroes, or blanks. However, all four digits cannot be simultaneously loaded due to a special decode of D<sub>1</sub> • D<sub>2</sub> • D<sub>3</sub> • D<sub>4</sub> which causes a reset of the



## PIN FUNCTION DESCRIPTION (Cont'd)

backplane divider and inhibits loading of the BCD data. Unused Digit Strokes should be tied to ground, to avoid them floating to a logic 1 condition which could cause an inadvertent reset condition. The reset condition stops the backplane square wave, putting the DF412 drive in a steady voltage state which would degrade the LCD when used in a long term application.

When ganging more than one DF412 together, it is necessary to synchronize the individual backplane signals to insure proper segment-backplane signal phase relationships. This is easily accomplished by initially pulling all digit strobe inputs high and by then driving the ganged DF412s with a common oscillator. By comparing the individual backplane

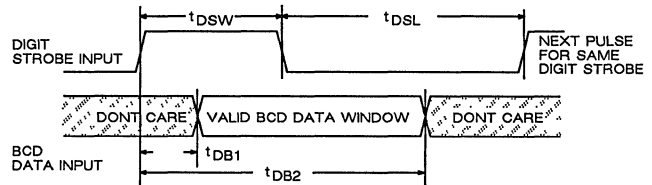
signals of two DF412s with an exclusive OR gate (see Figure 9) a continual checking of the backplane phase relationships can be accomplished. Should the individual backplane signals become out of phase an automatic reset will occur and proper phase will once again be established.

**Segment Outputs** -- Segments are driven with the DF412 segment outputs which generate square waves that are either in phase with the backplane for an OFF segment or out of phase with the backplane for an ON segment. Output swings of the drivers are between  $V_{DD}$  and  $V_{SS}$ . The CMOS output drivers provide matched resistance to both  $V_{DD}$  and ground, eliminating any net DC voltage component on the LCD thus maximizing display life.

## TRUTH TABLE

B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	Display Character
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	A
1	0	1	1	B
1	1	0	0	C
1	1	0	1	D
1	1	1	0	E
1	1	1	1	BLANK

## TIMING WAVEFORMS AND DEFINITIONS



Recommended Drive Conditions*		Min	Max
$t_{CP}$	Clock Period	19.5 $\mu s$ **	65 $\mu s$ **
$t_{DSW}$	Digit Strobe Pulse Width	$t_{CP} + 1 \mu s$	-
$t_{DSL}$	Digit Strobe Low Time	2 $t_{CP}$	-
$t_{DB1}$	Digit Strobe to BCD Setup Time	$-\infty$	$t_{CP} - 2 \mu s$
$t_{DB2}$	Digit Strobe to BCD Hold Time	2 $t_{CP} + 2 \mu s$	$\infty$

\* These minimum/maximum conditions indicate the necessary conditions to insure operation. They are based on design structure (shown in Figure 8a) with sufficient guardband to allow for propagation delay changes. They are not tested nor guaranteed.

\*\* The min-max clock periods correspond to a 30 Hz-100 Hz LCD backplane frequency range.

Figure 1

**TEST CIRCUITS**

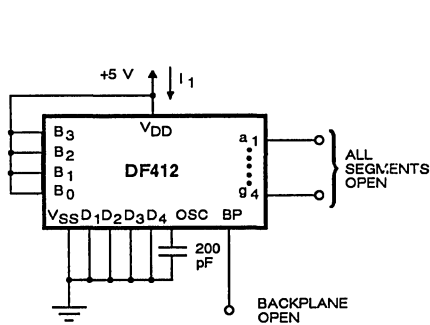


Figure 2. Static Supply Current Test Setup

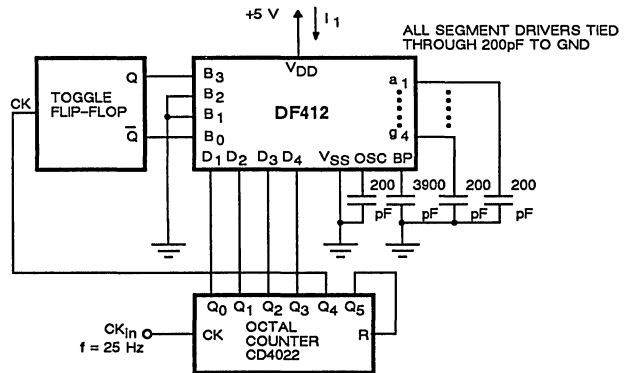
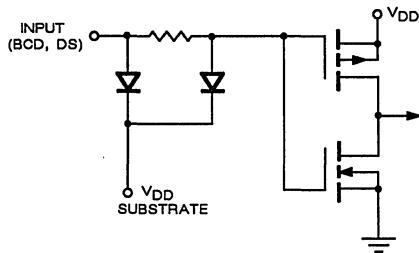
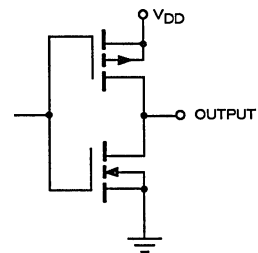


Figure 3. Dynamic Supply Current Test Setup

**INPUT-OUTPUT SCHEMATICS**

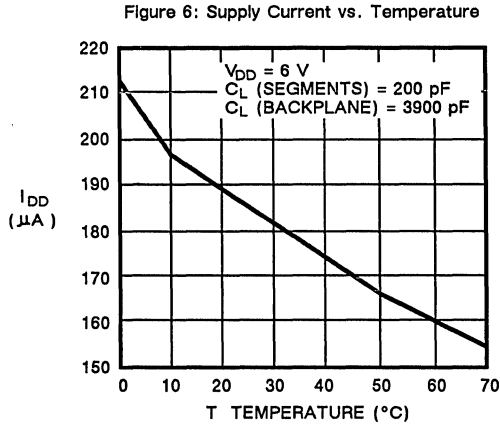
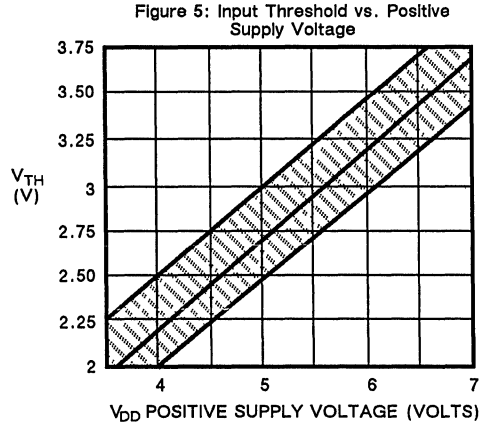
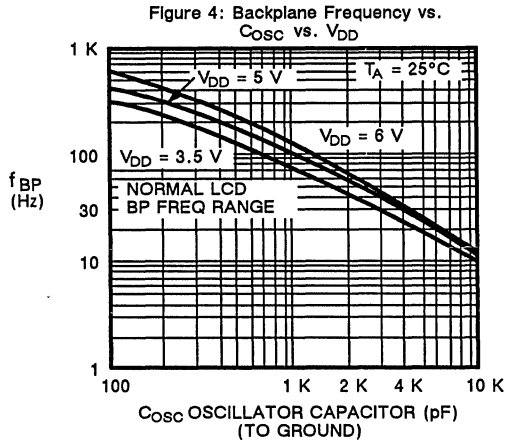


Input Structure

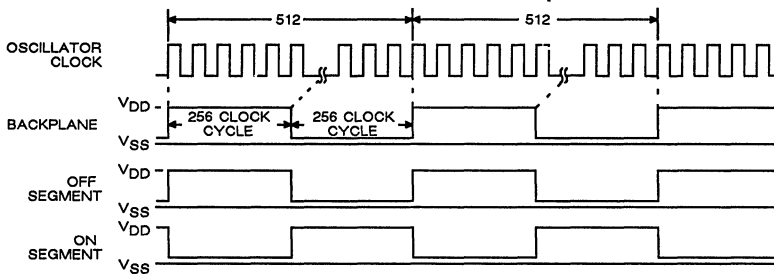


Output Structure

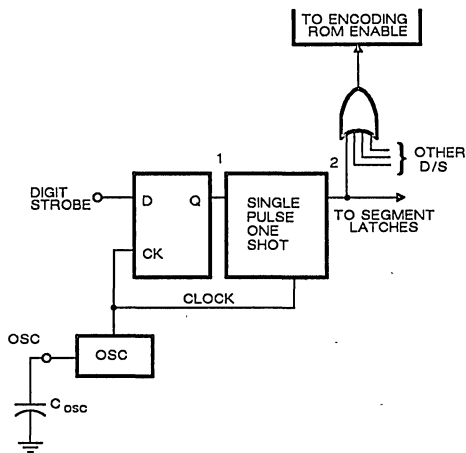
## TYPICAL CHARACTERISTICS



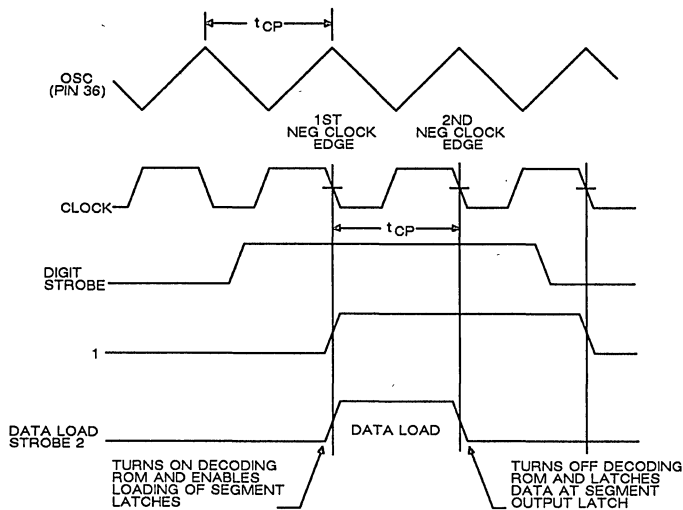
## TYPICAL WAVEFORMS



**DIGIT STROBE INPUT STAGE**



**Figure 7. Digit Strobe Input Circuit**



**Figure 8. Digit Strobe and Clock Timing Relationships to Data Loading**



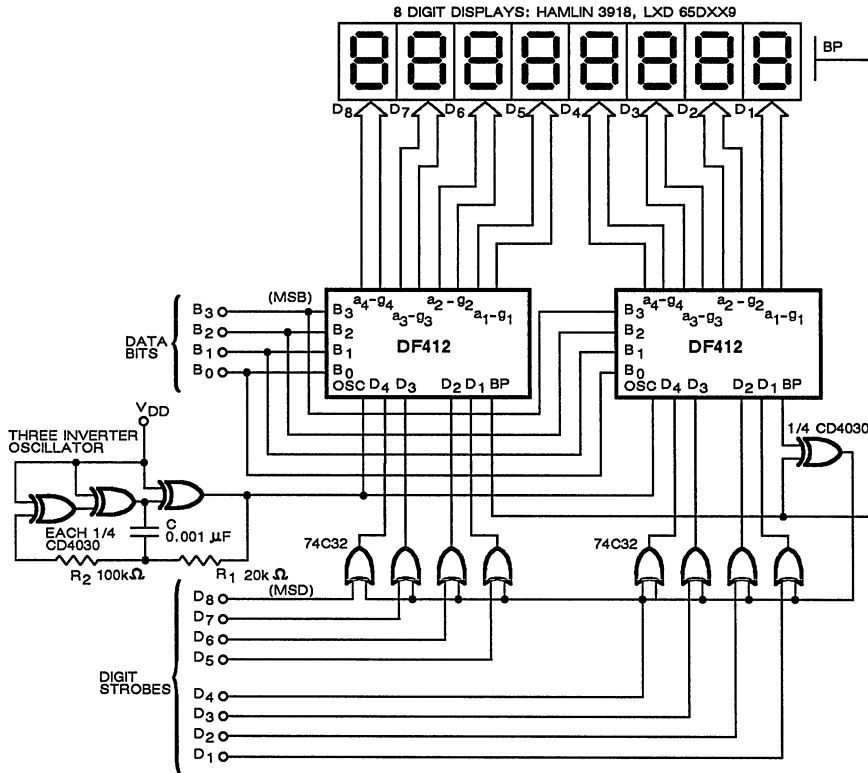


Figure 9. Ganged DF412's Drive 8 Digit LCD

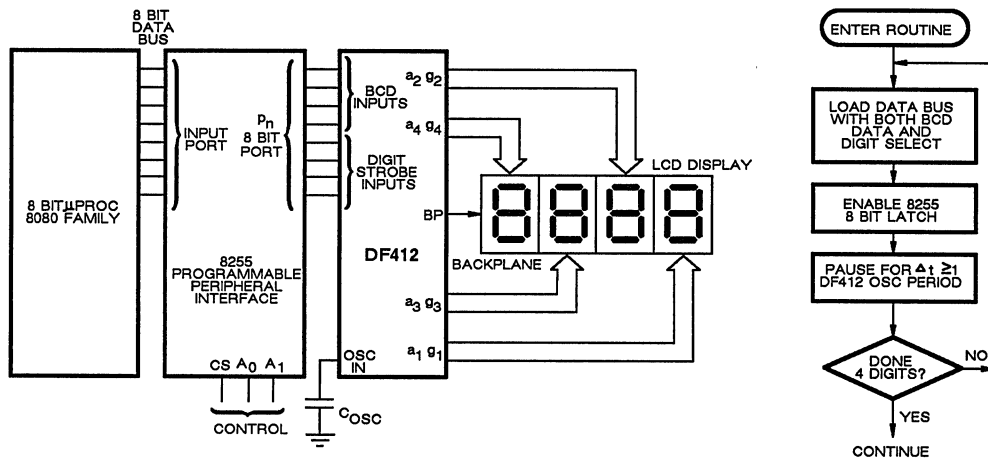


Figure 10. The DF412 Allows simple Interface to the LCD Display from an 8080 Microprocessor. Data Transfer is made with an 8-bit Dump. Bringing both the BCD Input and the Digit Strobes to the Chip in Parallel.



APPLICATIONS (Cont'd)

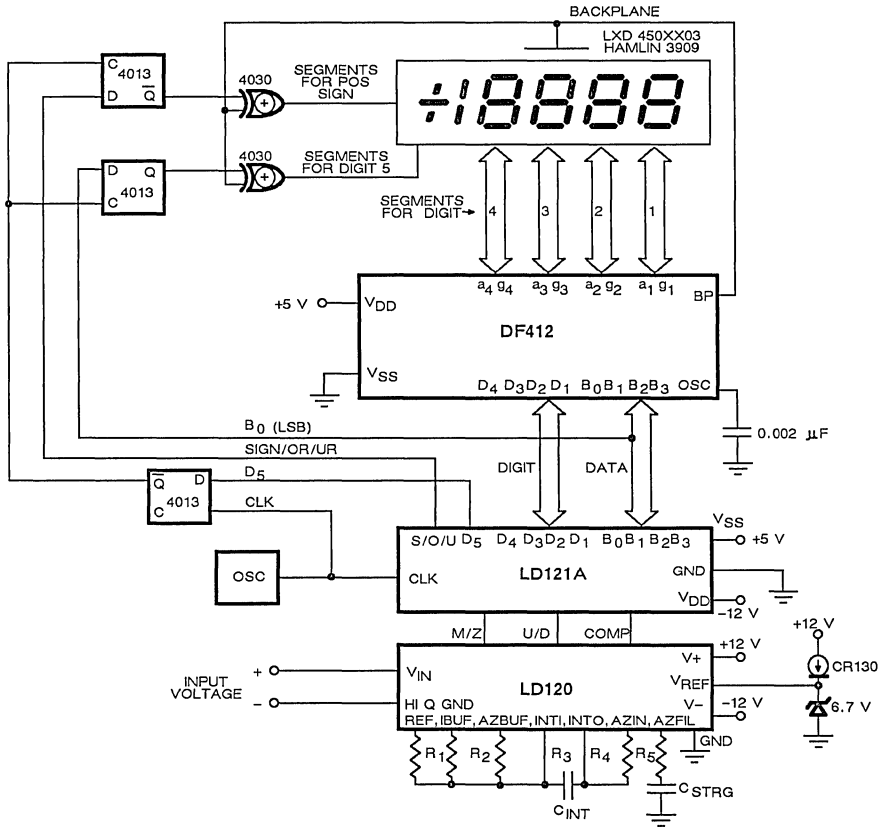


Figure 11. 4 1/2 Digit LCD-DVM

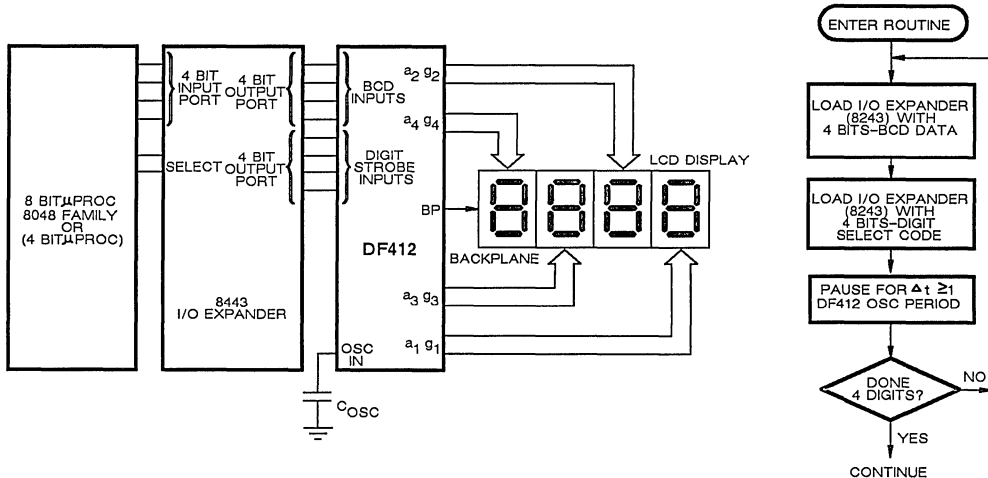


Figure 12. Simple LCD Interface with 8048 Family of Microprocessors. Data Transfer is made with two 4-Bit Ports, Loaded with 4-Bit Dumps. Note in the Flow chart that the BCD Data is latched to the expander first, then the Digit Strobe is sent out. This insures proper data being loaded in.

# Electroluminescent Row Drivers

### FEATURES

- 32 Channels Per Device
- 225 V, Open-Drain DMOS Outputs
- 80 mA Output Current Capability
- 32-Bit Shift Register
- CMOS Compatible Inputs

### APPLICATIONS

- Electroluminescent Displays
- ATE

### DESCRIPTION

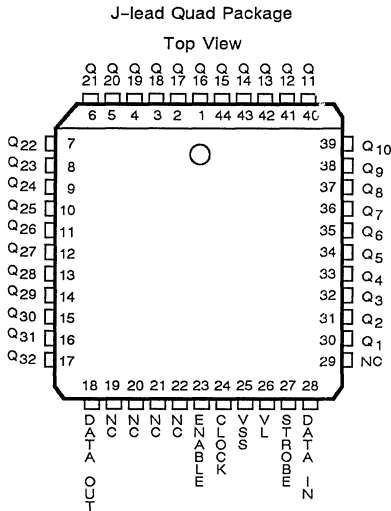
The Si9551 and Si9552 are monolithic D/CMOS integrated circuits designed to drive the row electrodes of electroluminescent displays. Each driver has 32-bit shift register and 32 high voltage outputs. The Si9551 output order has been reversed from the Si9552 for circuit board layout considerations.

New data is shifted into the 32-bit register during the falling edge of the clock input. The ENABLE and STROBE lines allow the row driver signal on V<sub>SS</sub> to

be connected to all of the Q outputs, none of the Q outputs, or the Q output selected by the shift register. Devices may be cascaded together using the serial output which is always enabled.

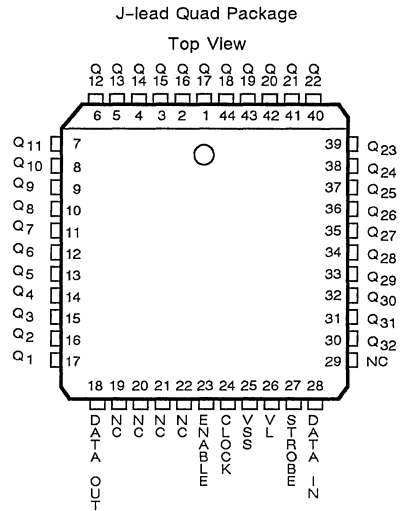
The Si9551 and Si9552 are available in 44-pin ceramic and plastic J-lead quad packages, and are specified over the military, A suffix (-55 to 125°C) and commercial, C suffix (0 to 70°C) temperature ranges.

### PIN CONFIGURATION



Order Numbers:

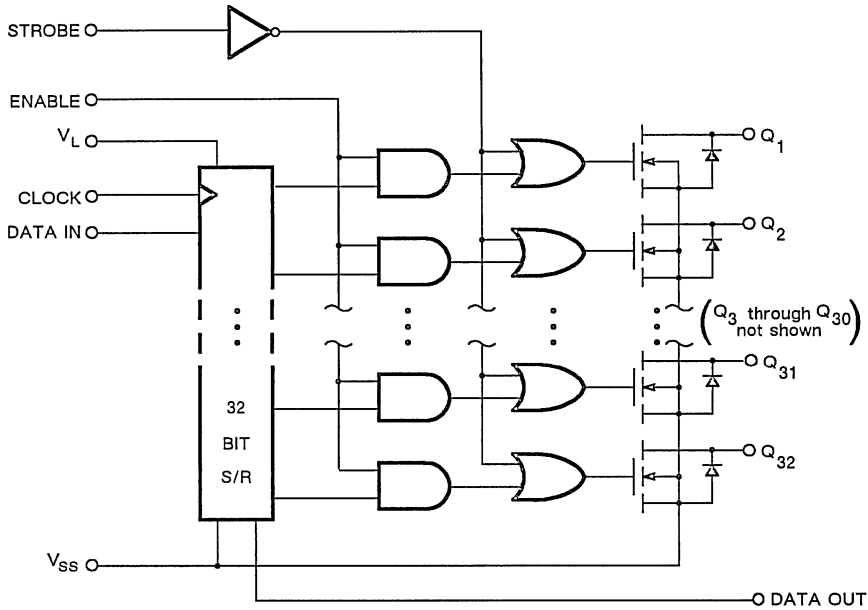
Ceramic: Si9551AM  
Plastic: Si9551CN



Order Numbers:

Ceramic: Si9552AM  
Plastic: Si9552CN

**FUNCTIONAL BLOCK DIAGRAM**



**TRUTH TABLE**

FUNCTION	CONTROL INPUTS			INTERNAL SHIFT REGISTER	Q OUTPUTS (Serial output is always enabled)
	CLOCK	ENABLE	STROBE		
LOAD		X	X	$Q_n \rightarrow Q_{n+1}$	Determined by ENABLE and STROBE
		X	X	No Change	
ENABLE	X	L	H	Determined by CLOCK	All off
STROBE	X	H	H		Data out
	X	X	L		All on

**ABSOLUTE MAXIMUM RATINGS**

$V_L$  ..... 18 V  
 Input Voltage .....  $-0.3\text{ V to }V_L + 0.3\text{ V}$   
 Q Output Voltage ..... 225 V  
 $V_{SS}$  Terminal Current ..... 1.5 A  
 Storage Temperature (A Suffix) .....  $-65\text{ to }150^\circ\text{C}$   
 (C Suffix) .....  $-65\text{ to }125^\circ\text{C}$

Operating Temperature (A Suffix) .....  $-55\text{ to }125^\circ\text{C}$   
 (C Suffix) .....  $0\text{ to }70^\circ\text{C}$

Power Dissipation (Package)\*  
 Plastic Quad Package\*\* ..... 1700 mW  
 Ceramic Quad Package\*\*\* ..... 2000 mW

\* All leads welded or soldered to PC board.  
 \*\* Derate 13.6 mW /°C above 25°C.  
 \*\*\* Derate 16 mW /°C above 25°C.

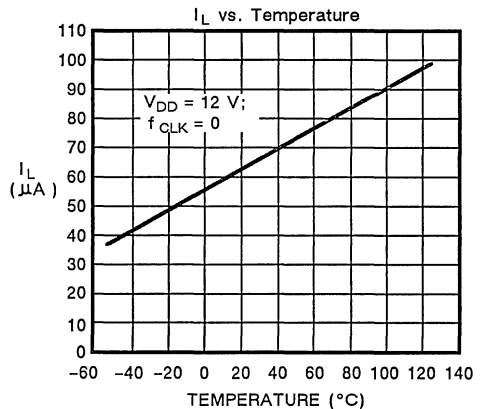
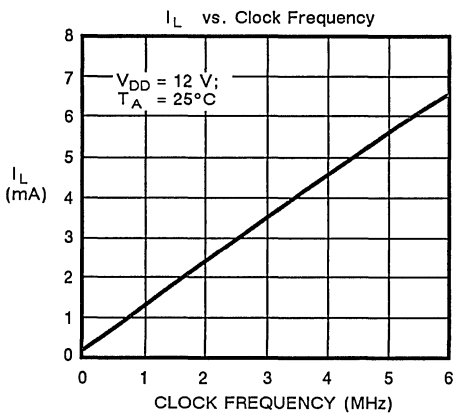
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_L = 12\text{ V}$ $V_{SS} = 0\text{ V}$	LIMITS						UNIT
			1=25°C		A SUFFIX		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
High Level Input Voltage	$V_{IH}$	$V_L = 10.8\text{ V}$	1		8.1		8.1		V
		$V_L = 15\text{ V}$	1		11.25		11.25		
Low Level Input Voltage	$V_{IL}$	$V_L = 10.8\text{ V}$	1		2.7		2.7		
		$V_L = 15\text{ V}$	1		3.75		3.75		
High Level Input Current	$I_{IH}$	$V_{IN} = 12\text{ V}$	1,2,3		1		1	$\mu\text{A}$	
Low Level Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$	1,2,3		-1		-1		
<b>Q OUTPUT <sup>e</sup></b>									
Low Level Output Current	$I_{OLQ}$	$V_L = 10.8\text{ V}$	1		80		80		mA
		$V_L = 15\text{ V}$	1		90		90		
Low Level Output Voltage	$V_{OLQ}$	$I_{OQ} = 80\text{ mA}$	1,2,3		30		30	V	
Off-State Output Current	$I_{O(OFF)}$	$V_{OQ} = 200\text{ V}$	1,2,3		10		10	$\mu\text{A}$	
Clamp Current	$I_{OK}$		1		-45		-45	mA	
<b>SERIAL OUTPUT</b>									
High Level Output Voltage	$V_{OHS}$	$I_{OHS} = -100\text{ }\mu\text{A}$	1,2,3		11.5		11.5	V	
Low Level Output Voltage	$V_{OLS}$	$I_{OLS} = 100\text{ }\mu\text{A}$	1,2,3		0.5		0.5		
<b>DYNAMIC</b>									
Clock Frequency	$f_{CLOCK}$		1,2,3		0	4	0	4	MHz
Pulse Duration Clock High or Low	$t_W$		1		125		125		ns
Data Setup Time before Rising Clock	$t_{SU}$		1		100		100		
Data Hold Time after Rising Clock	$t_H$		1		100		100		

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_L = 12\text{ V}$ $V_{SS} = 0\text{ V}$	LIMITS						UNIT	
			1=25°C		A SUFFIX		C SUFFIX			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC (Cont'd)</b>										
Delay Time High to Low Level Serial Output from Clock	$t_{DHL}$	$C_L = 10\text{ pF to }V_{SS}$	1			150		150	ns	
Delay Time Low to High Level Serial Output from Clock	$t_{DLH}$		1			200		200		
Turn-On Time Q Outputs fro Enable	$t_{ON}$	$I_{OL} = 50\text{ mA}$ $R_L = 2\text{ k}\Omega\text{ to }130\text{ V Supply}$	1			500		500		
<b>SUPPLY</b>										
$V_L$ Supply Voltage	$V_L$		1,2,3			10.8	15	10.8	15	V
$V_L$ Supply Current	$I_L$		1,2,3				0.5		0.5	mA

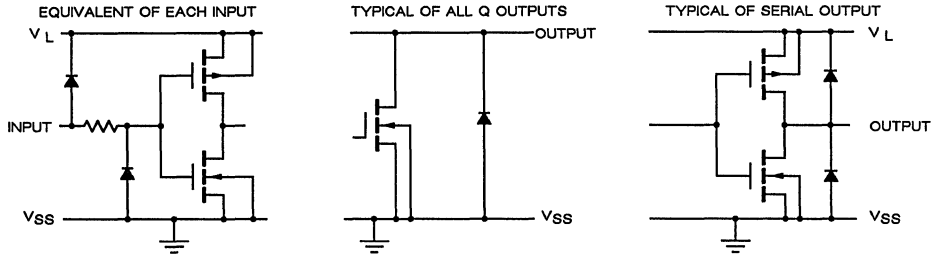
**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Output current measurements pulse duration = 300  $\mu\text{s}$ , duty cycle = 2%.

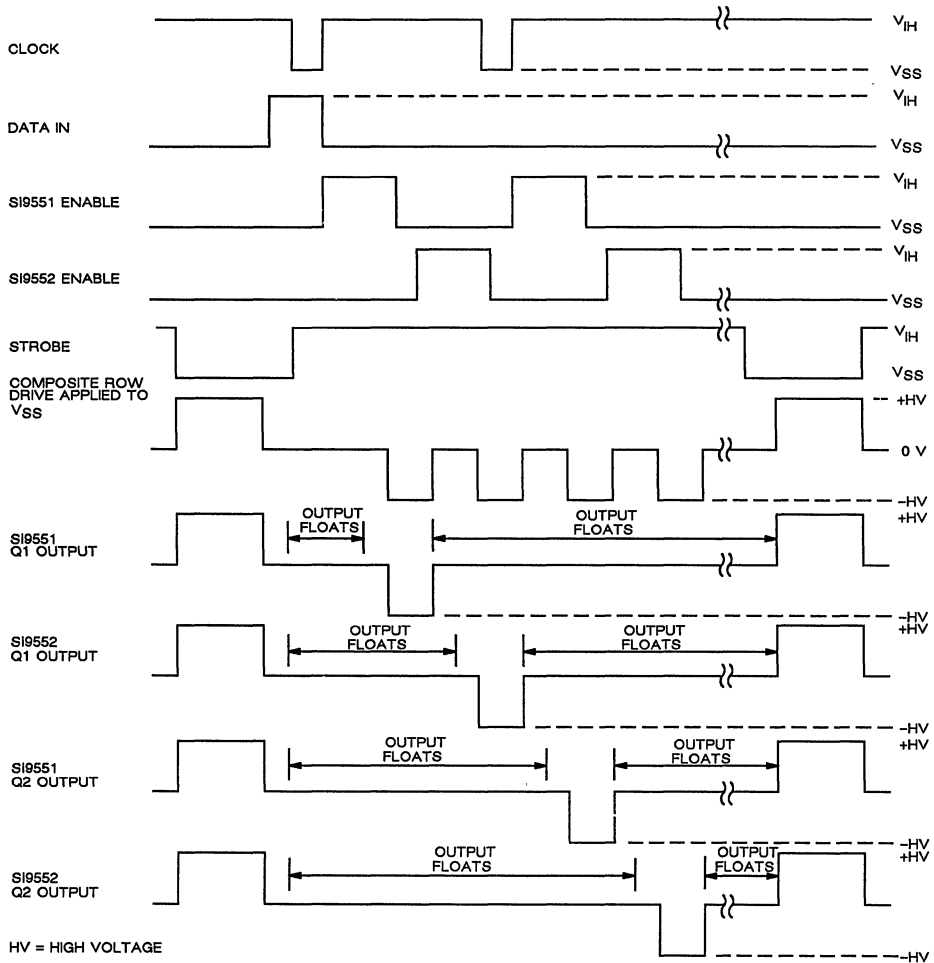
**TYPICAL CHARACTERISTICS**



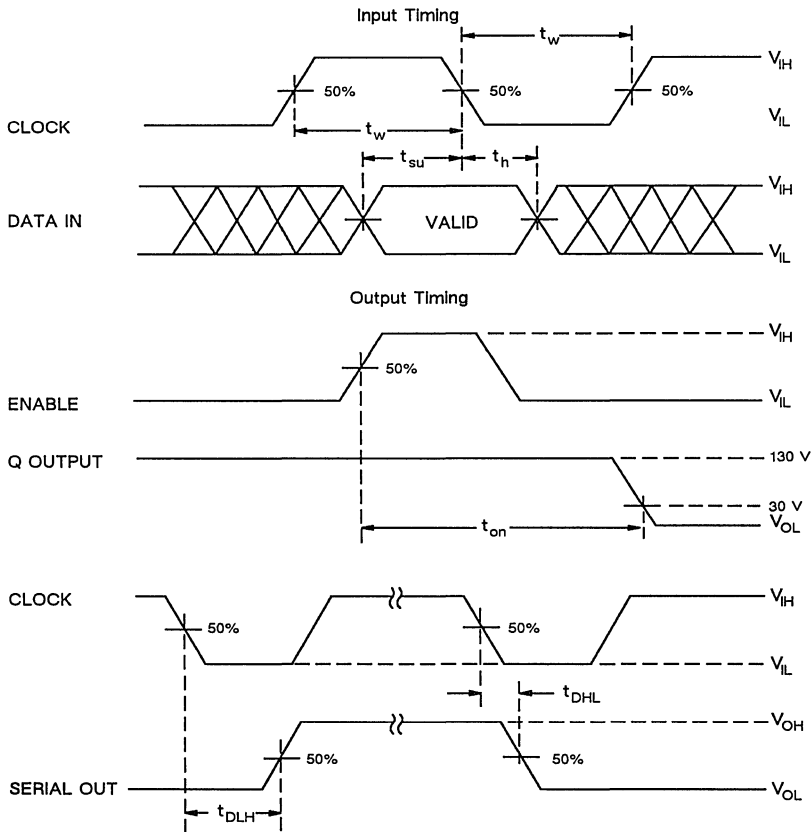
## SCHEMATIC DIAGRAMS



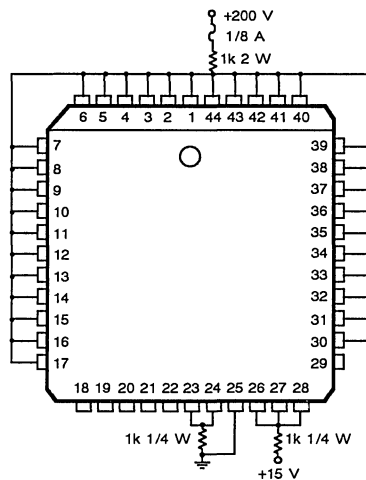
## TYPICAL OPERATING SEQUENCE



## TYPICAL WAVEFORMS



## BURN IN DIAGRAM



## Electroluminescent Column Drivers

### FEATURES

- 32 Channels Per Device
- 60 V or 80 V Push-Pull Outputs
- 15 mA Output Source and Sink Current Capability
- High Speed Serial Data Input
- 32-Bit Latch

### APPLICATIONS

- Electroluminescent Displays
- Non-Impact Printers

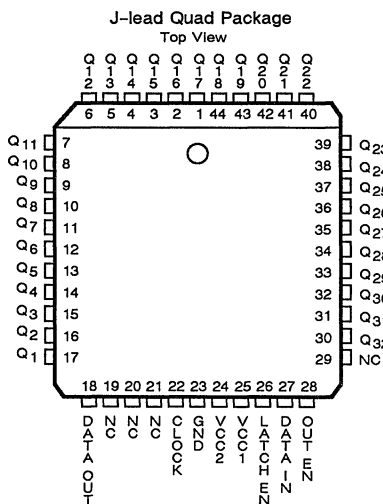
### DESCRIPTION

The Si9553 and Si9554 are monolithic D/CMOS integrated circuits designed to drive the column electrodes of electroluminescent displays. Each device has a 32-bit shift register, 32-bit latch, and 32 high voltage, push-pull output drivers. The Si9553/5 channel pin out has been reversed from the Si9554/6 for circuit board layout considerations. New data is shifted into the 32-bit register during the rising edge of the clock input. Data is transferred from the shift register to the latches

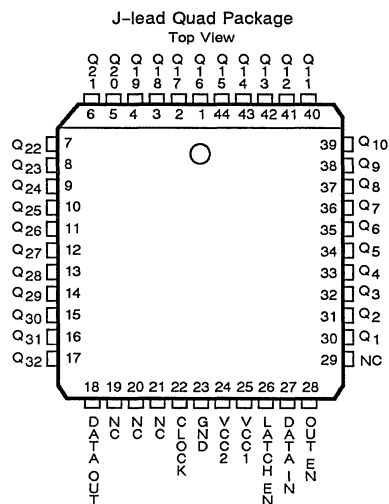
when the Latch Enable is high. The Q outputs are low when Output Enable is low and determined by the latches when Output Enable is high. Devices may be cascaded together using the serial output which is always enabled.

The Si9553, Si9554, Si9555, and Si9556 are available in 44-pin quad J-lead plastic and ceramic packages, specified over the commercial, C suffix (0 to 70°C) and military, A suffix (-55 to 125°C) temperature ranges.

### PIN CONFIGURATION



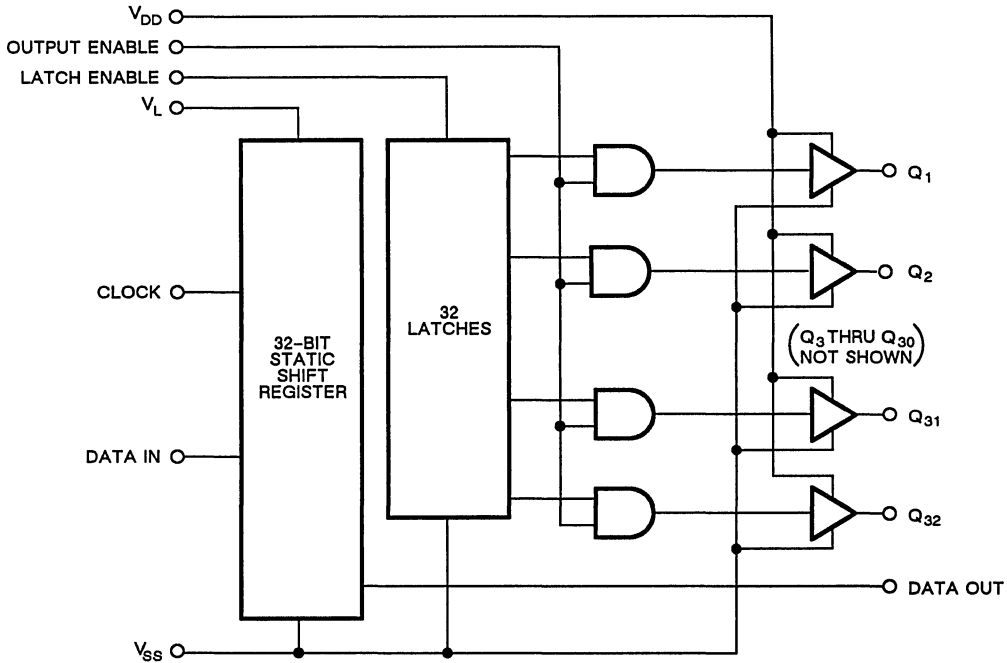
Order Numbers:  
CERQUAD: Si9553AM Si9555AM  
PLCC: Si9553CN Si9555CN



Order Numbers:  
CERQUAD: Si9554AM Si9556AM  
PLCC: Si9554CN Si9556CN



## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

$V_L$ .....	18 V
$V_{DD}$ (Si9553/4) .....	70 V
(Si9555/6) .....	90 V
Input Voltage .....	-0.3 to $V_L$ +0.3 V
$V_{SS}$ Current .....	700 mA
Operating Temperature (A Suffix) .....	-55 to 125°C
(C Suffix) .....	0 to 70°C
Storage Temperature .....	-65 to 150°C

Lead Temperature .....	300°C
(1/16" from case for 10 seconds)	
Power Dissipation (Package)*	
Plastic Quad Package** .....	1700 mW
Ceramic Quad Package*** .....	2000 mW

- \* All leads welded or soldered to PC board.
- \*\* Derate 13.6 mW/°C above 25°C.
- \*\*\* Derate 16 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>				Si9553/9554				
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 60$ V, $V_L = 12$ V $V_{SS} = 0$ V	LIMITS					
			1=25°C 2=125,70°C 3=-55,0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C	
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>
<b>INPUT</b>								
High Level Input Voltage	$V_{IH}$	$V_L = 10.8$ V	1		8.1		8.1	V
		$V_L = 15$ V	1		11.25		11.25	

ELECTRICAL CHARACTERISTICS <sup>a</sup>										Si9553/9554
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 60\text{ V}$ , $V_L = 12\text{ V}$ $V_{SS} = 0\text{ V}$	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUT {Cont'd}</b>										
Low Level Input Voltage	$V_{IL}$	$V_L = 10.8\text{ V}$	1			2.7		2.7	V	
		$V_L = 15\text{ V}$	1			3.75		3.75		
High Level Input Current	$I_{IH}$	$V_{IN} = 12\text{ V}$	1			1		1	$\mu\text{A}$	
Low Level Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$	1			-1		-1		
<b>Q OUTPUT <sup>e</sup></b>										
High Level Output Current	$I_{OHQ}$		1,2,3			-15		-15	mA	
Low Level Output Current	$I_{OLQ}$		1,2,3			15		15		
Clamp Current	$I_{OK}$		1,2,3			20		20		
High Level Output Voltage	$V_{OHQ}$	$I_{OHQ} = -15\text{ mA}$	1,2,3			50		52	V	
Low Level Output Voltage	$V_{OLQ}$	$I_{OLQ} = 15\text{ mA}$	1,2,3			10		8		
<b>SERIAL OUTPUT</b>										
High Level Output Voltage	$V_{OHS}$	$I_{OHS} = -100\text{ }\mu\text{A}$	1,2,3			11.5		11.5	V	
Low Level Output Voltage	$V_{OLS}$	$I_{OLS} = 100\text{ }\mu\text{A}$	1,2,3			0.5		0.5		
<b>DYNAMIC</b>										
Clock Frequency	$f_{CLOCK}$		1,2,3	12		0	8	0	10	MHz
Pulse Duration Clock High or Low	$t_W$		1			50		50	ns	
Data Setup Time before Rising Clock	$t_{SU}$		1			25		25		
Data Hold Time after Rising Clock	$t_H$		1			25		25		
Delay Time High to Low Level Serial Output from Clock	$t_{DHL}$	$C_L = 10\text{ pF}$ to $V_{SS}$ See Delay Time Waveforms	1			75		75		
Delay Time Low to High Level Serial Output from Clock	$t_{DLH}$		1			75		75		

ELECTRICAL CHARACTERISTICS <sup>a</sup>							Si9553/9554			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 60\text{ V}$ , $V_L = 12\text{ V}$ $V_{SS} = 0\text{ V}$	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>DYNAMIC (Cont'd)</b>										
Propagation Delay Time High to Low Level Q Outputs from LE	$t_{PHL}$	$R_L = 3.8\text{ k}\Omega$ to $V_{DD}$ $I_{OL} = 15\text{ mA}$	1			500		500	ns	
Propagation Delay Time Low to High Level Q Outputs from LE	$t_{PLH}$	$R_L = 3.8\text{ k}\Omega$ to $V_{SS}$ $I_{OL} = -15\text{ mA}$	1			500		500		
<b>SUPPLY</b>										
$V_L$ Supply Voltage	$V_L$		1,2,3			10.8	15	10.8	15	V
$V_{DD}$ Supply Voltage	$V_{DD}$		1,2,3			0	60	0	60	
$V_L$ Supply Current	$I_L$	$f_{CLOCK} = 0$	1				1		0.5	mA
$V_{DD}$ Supply Current	$I_{DD}$	All Outputs High or Low	1				1		1	

ELECTRICAL CHARACTERISTICS <sup>a</sup>							Si9555/9556			
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 80\text{ V}$ , $V_L = 12\text{ V}$ $V_{SS} = 0\text{ V}$	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>INPUT</b>										
High Level Input Voltage	$V_{IH}$	$V_L = 10.8\text{ V}$	1			8.1		8.1	V	
		$V_L = 15\text{ V}$	1			11.25		11.25		
Low Level Input Voltage	$V_{IL}$	$V_L = 10.8\text{ V}$	1				2.7	2.7		
		$V_L = 15\text{ V}$	1				3.75	3.75		
High Level Input Current	$I_{IH}$	$V_{IN} = 12\text{ V}$	1				1	1	$\mu\text{A}$	
Low Level Input Current	$I_{IL}$	$V_{IN} = 0\text{ V}$	1				-1	-1		

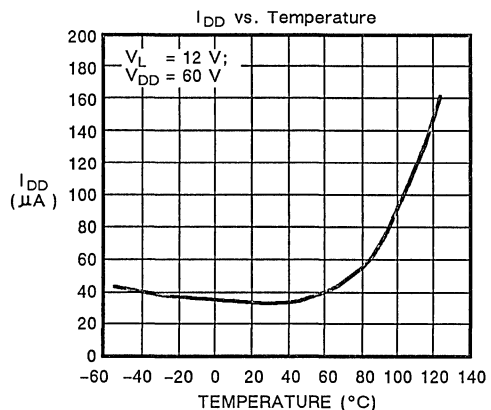
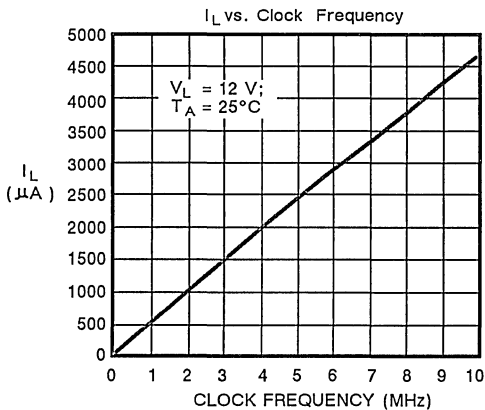
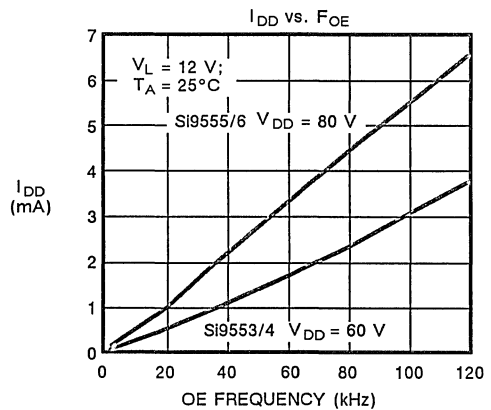
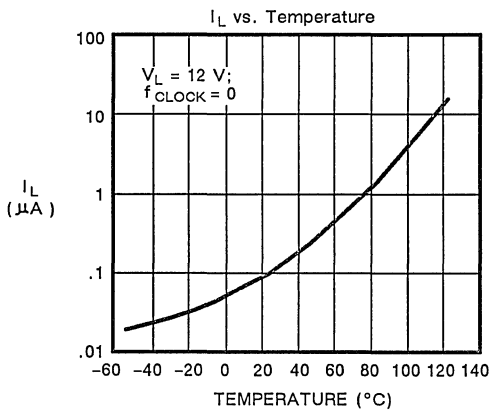
ELECTRICAL CHARACTERISTICS <sup>a</sup>										Si9555/9556
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_{DD} = 80\text{ V}$ , $V_L = 12\text{ V}$ $V_{SS} = 0\text{ V}$	LIMITS						UNIT	
			1=25°C 2=125,70°C 3=-55,0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>Q OUTPUT <sup>a</sup></b>										
High Level Output Current	$I_{OHQ}$		1,2,3		-15		-15			mA
Low Level Output Current	$I_{OLQ}$		1,2,3		15		15			
Clamp Current	$I_{OK}$		1,2,3			20		20		
High Level Output Voltage	$V_{OHQ}$	$I_{OHQ} = -15\text{ mA}$	1,2,3		70		72		V	
Low Level Output Voltage	$V_{OLQ}$	$I_{OLQ} = 15\text{ mA}$	1,2,3			10		8		
<b>SERIAL OUTPUT</b>										
High Level Output Voltage	$V_{OHS}$	$I_{OHS} = -100\text{ }\mu\text{A}$	1,2,3		11.5		11.5		V	
Low Level Output Voltage	$V_{OLS}$	$I_{OLS} = 100\text{ }\mu\text{A}$	1,2,3			0.5		0.5		
<b>DYNAMIC</b>										
Clock Frequency	$f_{CLOCK}$		1,2,3	12	0	8	0	10	MHz	
Pulse Duration Clock High or Low	$t_W$		1		50		50		ns	
Data Setup Time before Rising Clock	$t_{SU}$		1		25		25			
Data Hold Time after Rising Clock	$t_H$		1		25		25			
Delay Time High to Low Level Serial Output from Clock	$t_{DHL}$	$C_L = 10\text{ pF}$ to $V_{SS}$ See Delay Time Waveforms	1			75		75	ns	
Delay Time Low to High Level Serial Output from Clock	$t_{DLH}$		1			75		75		
Propogation Delay Time High to Low Level Q Outputs from LE	$t_{PHL}$	$R_L = 3.8\text{ k}\Omega$ to $V_{DD}$ $I_{OL} = 15\text{ mA}$	1			500		500		
Propogation Delay Time Low to High Level Q Outputs from LE	$t_{PLH}$	$R_L = 3.8\text{ k}\Omega$ to $V_{SS}$ $I_{OL} = -15\text{ mA}$	1			500		500		
<b>SUPPLY</b>										
$V_L$ Supply Voltage	$V_L$		1,2,3		10.8	15	10.8	15	V	
$V_{DD}$ Supply Voltage	$V_{DD}$		1,2,3		0	80	0	80		

ELECTRICAL CHARACTERISTICS <sup>a</sup>			Si9555/9556						
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 80\text{ V}$ , $V_L = 12\text{ V}$ $V_{SS} = 0\text{ V}$	LIMITS					UNIT	
			1=25°C 2=125,70°C 3=-55,0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>		MAX <sup>b</sup>
<b>SUPPLY (Cont'd)</b>									
$V_L$ Supply Current	$I_L$	$f_{\text{CLOCK}} = 0$	1			1		0.5	mA
$V_{DD}$ Supply Current	$I_{DD}$	All Outputs High	1,2,3			5		5	
		All Outputs Low	1,2,3			2		2	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Output current measurements pulse duration = 300  $\mu\text{s}$ , duty cycle = 2%

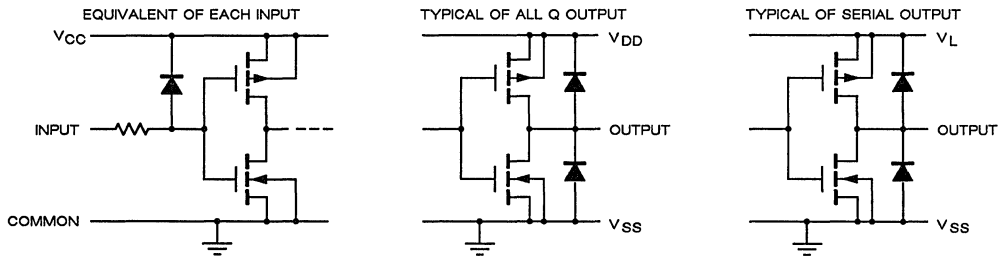
**TYPICAL CHARACTERISTICS**



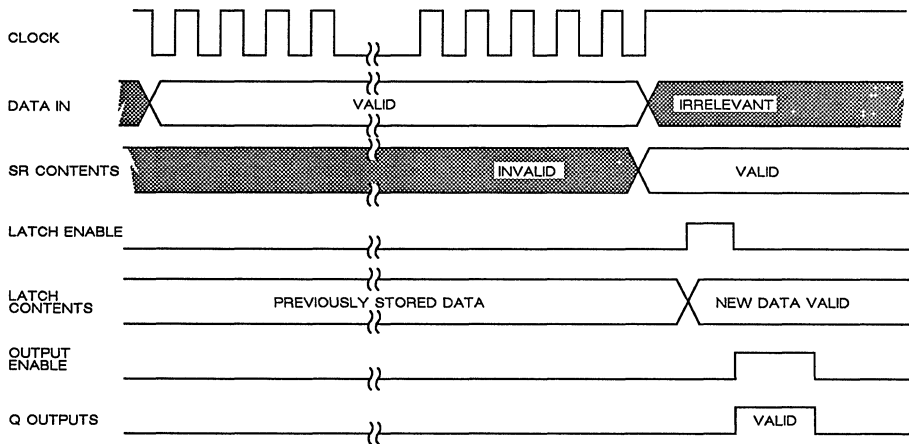
## TRUTH TABLE

FUNCTION	CLOCK	LATCH ENABLE	OUTPUT ENABLE	INTERNAL SHIFT REGISTER	LATCHES	Q OUTPUTS (Serial output is always enabled)
LOAD		X	X	Shift Data	Determined by Latch Enable	Determined by Output Enable
		X	X	No Change		
LATCH	X	L	X	Determined by CLOCK	Hold	
	X	H	X		New Data	
OUTPUT ENABLE	X	X	L		Determined by Latch Enable	All Q outputs low
	X	X	H			Data Out

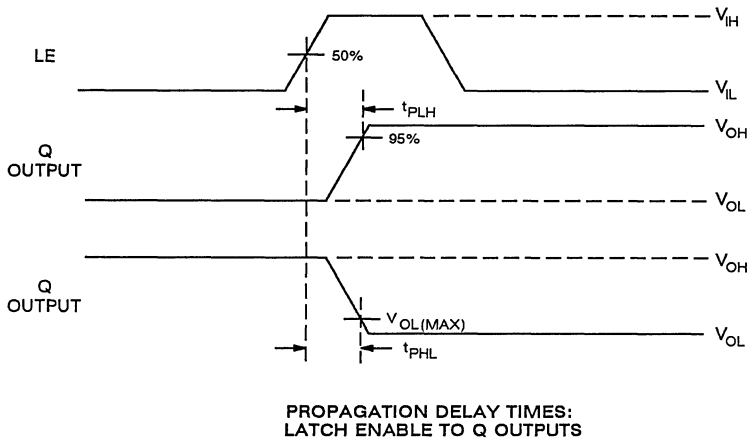
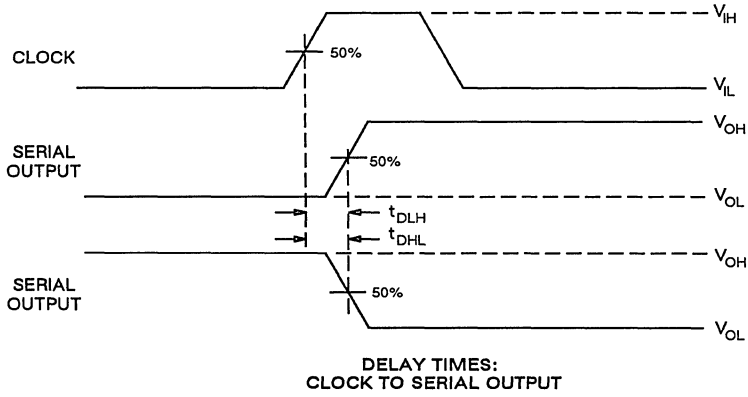
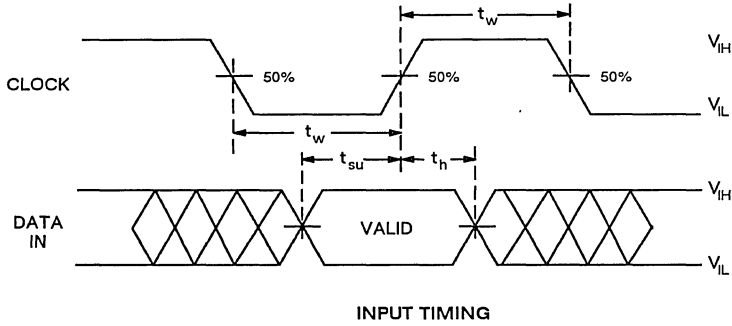
## SCHEMATIC DIAGRAMS



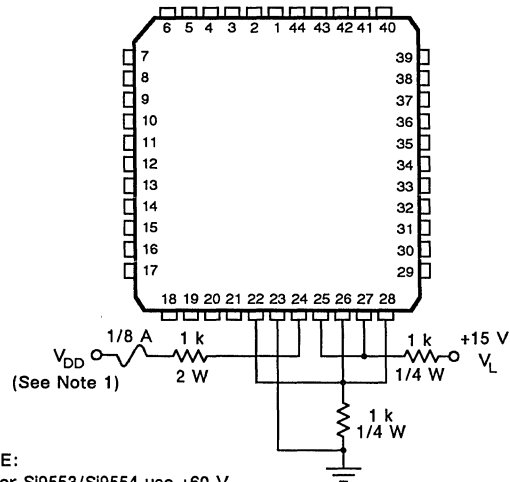
## TYPICAL OPERATING SEQUENCE



**TYPICAL WAVEFORMS**



## BURN-IN DIAGRAM



**NOTE:**

1. For Si9553/Si9554 use +60 V  
For Si9555/Si9556 use +80 V



## Electroluminescent Symmetric Row Driver

### FEATURES

- 230 V Push-Pull Outputs
- 100 mA Source/Sink Current
- 34 Outputs Per Device
- Right/Left Shift Pin
- Polarity Output Gating

### APPLICATIONS

- Flat Panel Displays
- High-Voltage Line Drivers
- Non-Impact Printers

### DESCRIPTION

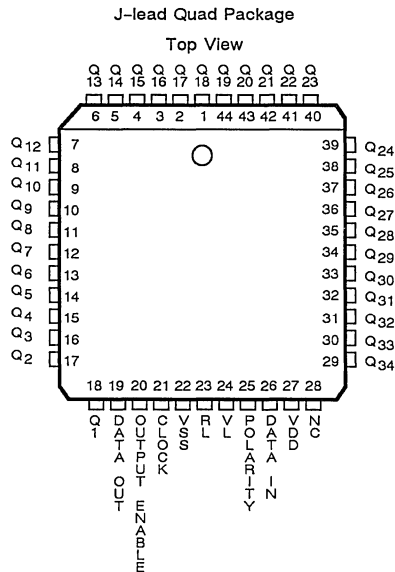
The Si9560 is a monolithic D/CMOS integrated circuit designed to interface video controllers to the high-voltage row electrodes of AC thin-film electroluminescent (ACTFEL) flat panel displays. The Si9560 features 34 push-pull outputs and shift register steering for easier use with large area (640 X 200/400) displays.

The shift register steering is controlled by the R/L shift pin which can be tied to  $V_{SS}$  for clockwise, or to  $V_L$  for counterclockwise operation. The outputs

are controlled by the OUTPUT ENABLE and POLARITY pins. New data is shifted on the falling edge of CLOCK. If OE is high, a logic high data bit will turn on the output as determined by POLARITY. POLARITY high pulls the output up to  $V_{DD}$ , while POLARITY low pulls the output down to  $V_{SS}$ .

The Si9560 is available in 44-lead plastic or ceramic J-lead quad packages, and is specified over the commercial, C suffix (0 to 70°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

### PIN CONFIGURATION

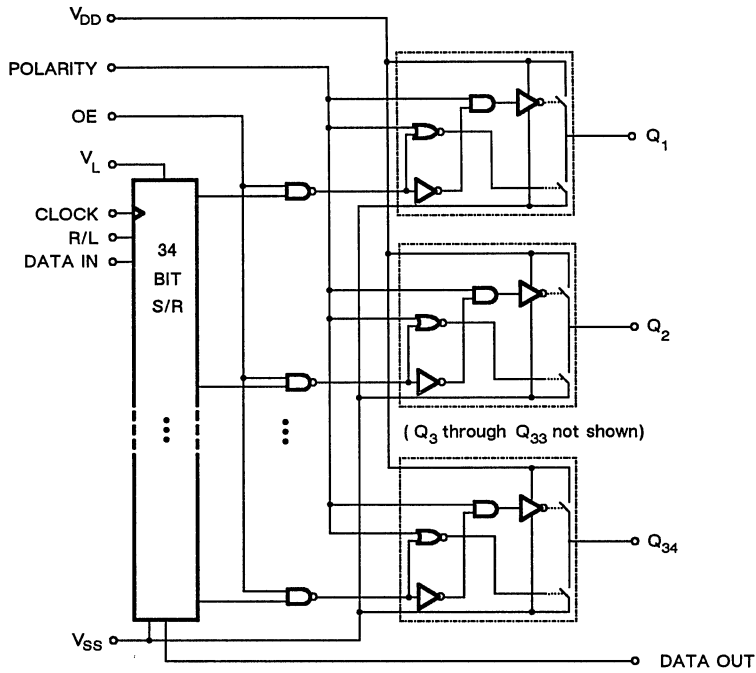


Order Numbers:

Plastic: Si9560CN  
Ceramic: Si9560DM



## FUNCTIONAL BLOCK DIAGRAM



## TRUTH TABLES

FUNCTION	CLOCK	R/L	SHIFT REGISTER	DATA OUT
LOAD		L	$Q_n \rightarrow Q_{n+1}$	$Q_{34}$
		H	$Q_n \rightarrow Q_{n-1}$	$Q_1$
	No	X	No Change	No Change

DATA	ENABLE	POL	OUTPUT
X	L	X	All OFF
H	H	H	H
H	H	L	L
L	H	X	OFF

L = Logic 0, H = Logic 1, X = Don't Care

**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to  $V_{SS}$

$V_{DD}$  ..... 240 V

$V_L$  ..... 16.5 V

Logic Inputs ..... -0.3 V to  $V_L + 0.3$  V  
(CK, R/L, DATA IN, POLARITY, OE)

$I_{SS}$  (Pulsed) ..... 1.0 A

Storage Temperature (D, C Suffix) ..... -65 to 125°C

Operating Temperature (D Suffix) ..... -40 to 85°C  
(C Suffix) ..... 0 to 70°C

Power dissipation (Package)\*

44-Pin Plastic Quad\*\* ..... 1700 mW  
44-Pin Ceramic Quad\*\*\* ..... 2000 mW

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 13.6 mW/°C above 25°C.

\*\*\* Derate 16 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 225$ V <sup>e</sup> $V_L = 12$ V $V_{SS} = 0$ V	LIMITS						UNIT
			1=25°C 2=85,70°C 3=-40,0°C		D SUFFIX		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
High Level Input Voltage	$V_{IH}$	$V_L = 10.8$ V	1		8.1		8.1		V
		$V_L = 13.2$ V	1		9.9		9.9		
Low Level Input Voltage	$V_{IL}$	$V_L = 10.8$ V	1			2.7		2.7	
		$V_L = 13.2$ V	1			3.3		3.3	
High Level Input Current	$I_{IH}$	$V_I = 12$ V	1,2,3			1		1	$\mu$ A
Low Level Input Current	$I_{IL}$	$V_I = 0$ V	1,2,3			-1		-1	$\mu$ A
<b>Q OUTPUTS</b>									
Off State Output Current	$I_{D(OFF)}$	$V_{DD} = V_O = 230$ V	1,2,3		20		20		$\mu$ A
		$V_{DD} = 230$ V, $V_O = 0$ V	1,2,3		-20		-20		
High Level Output Voltage Q Outputs	$V_{OHQ}$	$I_O = -70$ mA	1,2,3		195		195		V
Low Level Output Voltage Q Outputs	$V_{OLQ}$	$I_O = 70$ mA	1,2,3			30		30	
Low Level Q Output Current	$I_{OLQ}$	$V_L = 10.8$ V to 13.2 V	1		100		100		mA
High Level Q Output Current	$I_{OHQ}$		1		-100		-100		
Output Clamp Current	$I_{OK}$		1,2,3		-100	100	-100	100	



ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 225 \text{ V}^e$ $V_L = 12 \text{ V}$ $V_{SS} = 0 \text{ V}$	LIMITS						UNIT
			1=25°C 2=85,70°C 3=-40,0°C		D SUFFIX		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>SERIAL OUTPUT</b>									
High Level Output Voltage Serial Output	$V_{OHS}$	$I_O = -100 \mu\text{A}$	1,2,3		11		11		V
Low Level Output Voltage Serial Output	$V_{OLS}$	$I_O = 100 \mu\text{A}$	1,2,3			1		1	
<b>DYNAMIC</b>									
Clock Frequency	$f_{\text{CLOCK}}$		1		0	4	0	4	MHz
Pulse Duration Clock High or Low	$t_w$		1		125		125		ns
Data Setup Time Before Falling Clock	$t_{\text{sud}}$	See Input Timing Voltage Waveforms	1		100		100		ns
Data Setup Time After Falling Clock	$t_{\text{hd}}$		1		100		100		
Setup Time Clock Low Before $V_{DD}\uparrow$ or $V_{SS}\uparrow$	$t_{\text{suc}}$		1		300		300		
Setup Time Enable High Before $V_{DD}\uparrow$ or $V_{SS}\uparrow$	$t_{\text{sue}}$		1		300		300		
Setup Time Polarity High or Low Before $V_{DD}\uparrow$ or $V_{SS}\uparrow$	$t_{\text{sup}}$		1		300		300		
Hold Time Clock High After $V_{DD}\uparrow$ or $V_{SS}\uparrow$	$t_{\text{hc}}$		1		500		500		
Hold Time Enable High After $V_{DD}\uparrow$ or $V_{SS}\uparrow$	$t_{\text{he}}$		1		300		300		
Hold Time Polarity High or Low After $V_{DD}\uparrow$ or $V_{SS}\uparrow$	$t_{\text{hp}}$		1		300		300		
Delay Time High to Low Level Output from Clock	$t_{\text{dHL}}$	$C_L = 10 \text{ pF}$ to Ground	1			150		150	
Delay Time, Low to High Level Output from Clock	$t_{\text{dLH}}$		1			200		200	
Transition Time High to Low Level Serial Output	$t_{\text{tHL}}$		1			200		200	
Transition Time Low to High Level Serial Output	$t_{\text{tLH}}$		1			100		100	
High Level Turn-on Time Q Outputs from Enable	$t_{\text{onH}}$		$I_{OH} = -50 \text{ mA}$ , $V_{OH} = 195 \text{ V}$ $R_L = 2 \text{ k}\Omega$ to 95 V	1			500		500
Low Level Turn-on Time Q Outputs from Enable	$t_{\text{onL}}$	$I_{OL} = 50 \text{ mA}$ , $V_{OL} = 30 \text{ V}$ $R_L = 2 \text{ k}\Omega$ to 130 V	1			500		500	

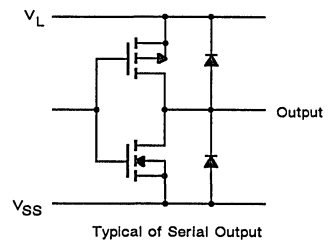
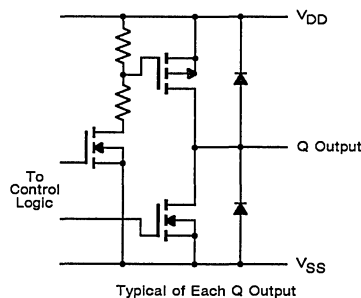
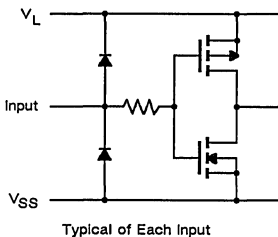
ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_{DD} = 225\text{ V}^e$ $V_L = 12\text{ V}$ $V_{SS} = 0\text{ V}$	LIMITS						UNIT
			1=25°C		D SUFFIX		C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>									
High Level Turn-off Time Q Outputs from Enable	$t_{offH}$	$I_{OH} = -50\text{ mA}$ , $V_{OH} = 195\text{ V}$ $R_L = 2\text{ k}\Omega$ to $95\text{ V}$	1			1500		1500	
Low Level Turn-off Time Q Outputs from Enable	$t_{offL}$	$I_{OL} = 50\text{ mA}$ , $V_{OL} = 30\text{ V}$ $R_L = 2\text{ k}\Omega$ to $130\text{ V}$	1			500		500	
Slew Rate, $V_{DD}$ or $V_{SS}$		With One Active Output Driving a $4.7\text{ nF}$ Load to $V_{DD}$ or $V_{SS}$	1			45		45	V/ $\mu$ s
<b>SUPPLY</b>									
Logic Supply Voltage	$V_L$		1,2,3		10.8	15	10.8	15	V
$V_{DD}$ Supply Voltage <sup>e</sup>	$V_{DD}$		1,2,3		0	230	0	230	
Logic Supply Current	$I_L$	$f_{CLOCK} = 0$	1,2,3			0.5		0.5	mA
		$f_{CLOCK} = 16\text{ kHz}$ , 1 Output ON	1			2		2	
$V_{DD}$ Supply Current	$I_{DD}$	All Outputs OFF	1,2,3			8		5	
		1 Output ON	1,2,3			15		10	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e.  $V_{DD}$  must be  $< 60\text{ V}$  above  $V_{SS}$  during switch transitions. Slew rate of  $V_{DD}$  or  $V_{SS}$  should be kept below  $45\text{ V}/\mu\text{s}$ .
- f. Output current measurements pulse duration =  $300\text{ }\mu\text{s}$ , duty cycle = 2%.



**SCHEMATIC DIAGRAMS**







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# POWER CONVERSION

## INTRODUCTION

Virtually every piece of electronic equipment in the world requires a dc power supply. This supply converts power from a battery or an ac line (or sometimes both) into voltages and currents which are useful to the specific piece of electronic equipment it serves. Usually, the outputs must remain constant despite changes in input voltage, output load, and ambient temperature. In addition, the supply should have high conversion efficiency; inject a minimum of noise, ripple, or distortion onto its input or output; be small in volume, light in weight, and low in cost.

Siliconix power conversion circuits bring effective solutions to the problems of supplying power to electronic systems, while meeting the above criteria. Siliconix presently supplies three types of power conversion circuits: high-voltage switchmode regulators, high-voltage switchmode controllers, and charge pump voltage converters.

The high-voltage switchmode regulators and controllers made by Siliconix employ high-performance D/CMOS power IC technology to combine CMOS current-mode controllers with high-voltage input regulation and output switching. This design allows Siliconix to build extremely high efficiency switchmode power supply circuits that can run directly from high-voltage inputs such as PBX or ISDN phone lines, or 110 VAC power lines.

The Si9100, Si9101, and Si9102 are switchmode regulators which include an integrated 5  $\Omega$  output MOSFET capable of supplying up to 5 Watt loads. They can be configured in single-ended converter topologies, and can be run directly from input voltages as high as 120 V. The major applications for these devices are in telecommunications equipment such as PBX feature phones, ISDN terminals, line-powered modems, and central office electronic equipment.

The Si9110 and Si9111 are switchmode controllers with the same features as the switchmode regulators, except that a push-pull output driver is utilized for driving an external MOSFET switch for higher power applications. These devices are generally used in telecommunications power supply applications greater than 5 Watts, as well as for general purpose dc/dc power converters.

The Si9115 and Si9116 are switchmode controllers designed to run directly from the rectified 110 Volt ac power line. Typical applications are in power supplies for electronic controls in appliances, small computers, and high-voltage avionics systems.

Our family of low-cost CMOS charge pump voltage converters are used in applications where a single dc supply is available. These monolithic products feature high conversion efficiency, minimum noise and distortion, and minimum space requirements. They can be configured for voltage inversion or voltage doubling, and require only a few external components (typically 2 electrolytic capacitors). A typical application would be negative rail generation in a circuit with a battery supply.

The Si7660 is a charge pump converter that inverts or doubles input voltages from 1.5 Volts to 10 Volts. It features power conversion efficiencies up to 98%. The Si7661 is a higher-voltage version of the Si7660 intended for input voltages from 7.5 Volts to 20 Volts.

# Si7660

## Monolithic CMOS Voltage Converter

### FEATURES

- Improved - No External Diode Required
- Conversion of +5 V Logic Supply to  $\pm 5$  V Supplies
- 99.7% Typical Open Circuit Voltage Conversion Efficiency
- 95% Typical Power Efficiency
- Operating Voltage Range of 1.5 V to 10.0 V
- Requires Only 2 Capacitors

### BENEFITS

- Inexpensive Negative Supply from Positive Supply
- Easy to Use
- Minimum Parts Count
- Small Size
- No Diode Drop at Output

### APPLICATIONS

- On Board Negative Supply for Dynamic RAMs
- Localized  $\mu$ -Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies for Analog Switches
- Data Acquisition Systems

### DESCRIPTION

The Siliconix Si7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7660 performs a supply voltage conversion from positive to negative for an input range of +1.5 V to +10.0 V, resulting in a complementary output voltage of -1.5 V to -10.0 V with the addition of only 2 capacitors.

Typical applications for the Si7660 are data acquisition and microprocessor based systems where a +5 V supply is available for the digital functions, and an additional -5 V supply is required for the analog functions. The Si7660 is also ideally suited for providing low current, -5 V body bias supply for dynamic RAMs.

Contained on the chip are a voltage regulator, RC oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and

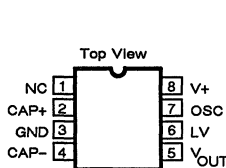
ensures that the output N-channel switch substrates are not forward-biased. The epitaxial layer prevents latch up.

The oscillator, when unloaded, oscillates at a nominal frequency of 12 kHz for an input supply voltage of 1.5 to 10 V. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

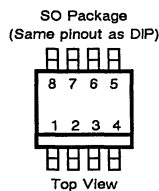
The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low voltage (LV) operation. At high voltages (+3.5 to +10 V), the "LV" pin should be left disconnected.

Packaging for this device includes the 8-pin metal can, plastic miniDIP, and SO options. Performance grades include military, A suffix (-55 to 125°C), industrial, D suffix (-40 to 85°C), and commercial, C suffix (0 to 70°C) temperature ranges. For additional information please refer to Applications Note AN84-2.

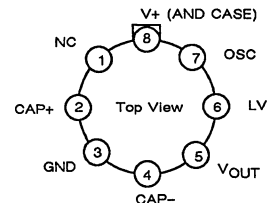
### PIN CONFIGURATION



Order Number:  
Plastic: SI7660CJ

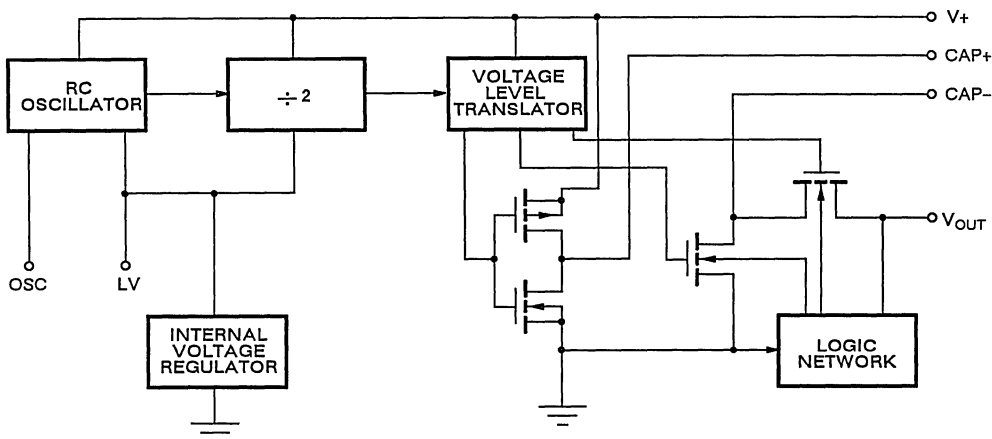


Order Number:  
SI7660DY



Order Number:  
SI7660AA, SI7660AA/883, SI7660BA, SI7660CA

**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage .....	11 V
Oscillator Input Voltage .....	-0.3 V to (V+ +0.3 V) for V+ < 5.5 V
.....	(V+ -5.5 V) to (V+ +0.3 V) for V+ > 5.5 V
LV .....	No connection for V+ > 3.5 V
Storage Temperature (A & B Suffix) .....	-65 to 150°C
..... (C & D Suffix) .....	-65 to 125°C
Operating Temperature (A Suffix) .....	-55 to 125°C
..... (B Suffix) .....	-25 to 85°C
..... (C Suffix) .....	0 to 70°C
..... (D Suffix) .....	-40 to 85°C

Power Dissipation:*	
8-Pin Metal Can** .....	500 mW
8-Pin Plastic DIP*** .....	300 mW
SO-8*** .....	300 mW

- \* All leads welded or soldered to PC board.
- \*\* Derate 6 mW/°C above 75°C.
- \*\*\* Derate 10 mW/°C above 75°C.

**ELECTRICAL CHARACTERISTICS <sup>a</sup>**

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = 5 V C <sub>osc</sub> = 0 <sup>d</sup>	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40,-20,0 °C		A SUFFIX		B,C,D SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>									
Supply Voltage Range LOW	V+ <sub>L</sub>	R <sub>L</sub> = 10 kΩ, LV = GND	1,2,3		1.5	3.5	1.5	3.5	V
Supply Voltage Range HIGH	V+ <sub>H</sub>	R <sub>L</sub> = 10 kΩ, LV = NC	1,2,3		3	10	3	10	
Supply Current	I+	R <sub>L</sub> = ∞, LV = OPEN	1,2,3	100		500		500	μA

**10**

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: $V_+ = 5\text{ V}$ $C_{osc} = 0^d$	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40,-20,0°C		A SUFFIX		B, C, D SUFFIX		
			TEMP	TYP <sup>c</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>OUTPUT</b>									
Output Source Resistance	$R_{OUT}$	$V_+ = 5\text{ V}$ , LV = OPEN $I_O = 20\text{ mA}$	1 3 2	55		100 120 150		100 120 120	$\Omega$
		$V_+ = 2\text{ V}$ , LV = GND $I_O = 3\text{ mA}$	1,2,3			300		300	
Power Conversion Efficiency	$PE_1$	$R_L = 5\text{ k}\Omega$	1	98	95		95		%
Voltage Conversion Efficiency	$V_{OUT}E_1$	$R_L = \infty$	1	99.9	97		97		%
<b>DYNAMIC</b>									
Oscillator Frequency <sup>d</sup>	$f_{osc}$		1	12					kHz
Oscillator Impedance	$Z_{osc}$	$V_+ = 2\text{ V}$ , LV = GND	1	1					M $\Omega$
		$V_+ = 5\text{ V}$	1	100					k $\Omega$

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. For  $C_{osc} > 1000\text{ pF}$ ,  $C_1$  and  $C_2$  should be increased to  $100\text{ }\mu\text{F}$ .  $C_1$  = Pump Capacitor,  $C_2$  = Reservoir Capacitor.

## DIE TOPOGRAPHY

64 mils  
3 2

64 mils  
8

5 6 7  
20X

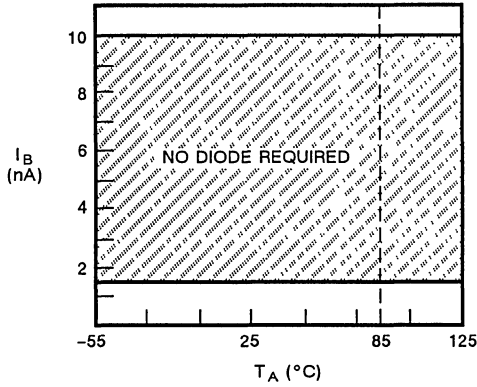
Pad No.	Function
2	CAP+
3	GND
4	CAP-
5	$V_{OUT}$
6	LV
7	OSC
8	$V_+$

**CSABA**

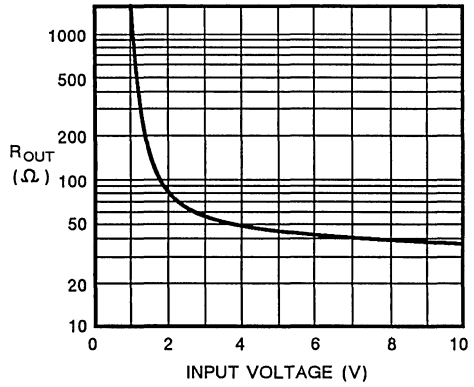
- 2 Resistors
- 1 Zener Diode
- 40 P-channel enhancement MOSFETs
- 1 Diode
- 3 Capacitors
- 48 N-channel enhancement MOSFETs

**TYPICAL CHARACTERISTICS**

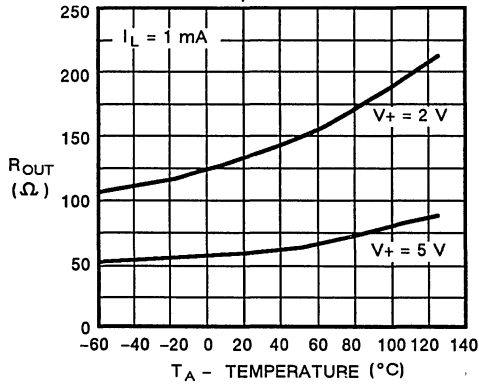
**Figure 1. Operating Voltage as a Function of Temperature**



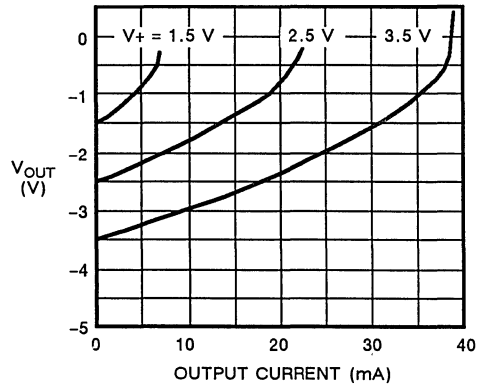
**Figure 2. Output Source Resistance as a Function of Supply Voltage**



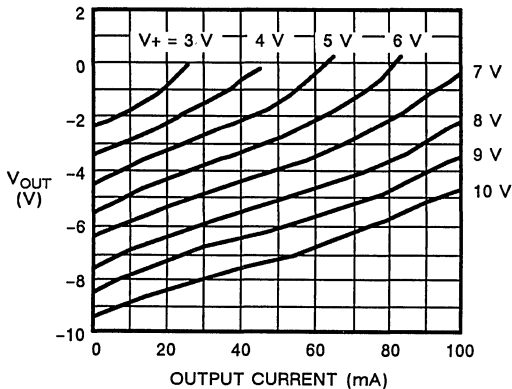
**Figure 3. Output Source Resistance vs. Temperature**



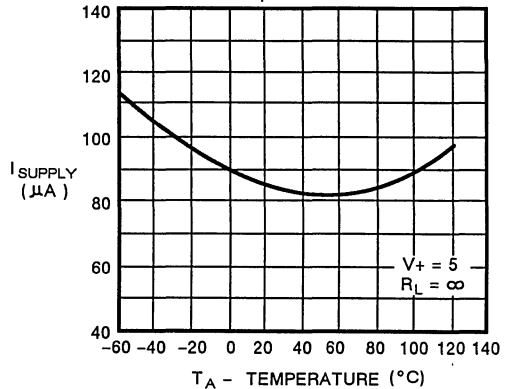
**Figure 4. Typical Si7660 Output LV = GND**



**Figure 5. Typical Si7660 Output LV OPEN**

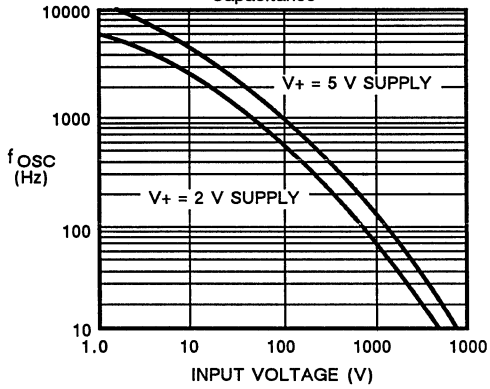


**Figure 6. Typical Supply Current vs. Temperature**

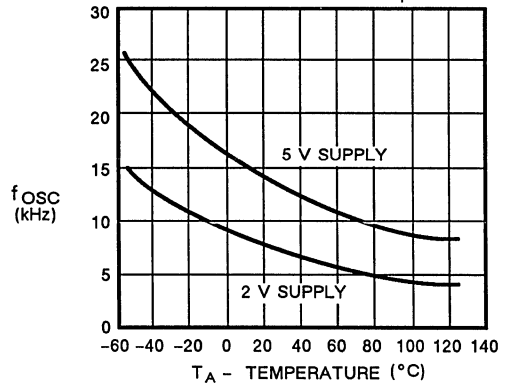


## TYPICAL CHARACTERISTICS (Cont'd)

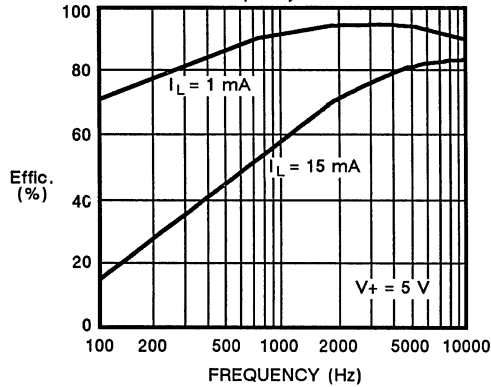
**Figure 7.** Oscillation Frequency as a Function of External OSC. Capacitance



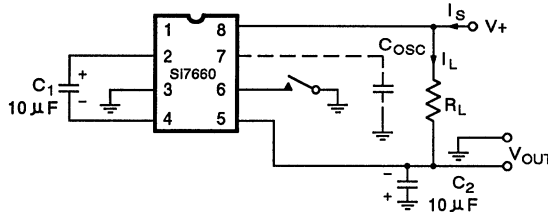
**Figure 8.** Unloaded Oscillator Frequency as a function of Temperature



**Figure 9.** Power Conversion Efficiency as a Function of OSC. Frequency



## SWITCHING TIME TEST CIRCUIT



**PIN DESCRIPTION**

Pin Number	Symbol	Pin Description
1	NC	No connection.
2	CAP+	Positive terminal connection for pump capacitor.
3	GND	Input and/or output ground reference.
4	CAP-	Negative terminal connection for pump capacitor.
5	V <sub>OUT</sub>	Output of the voltage converter.
6	LV	Low Voltage. Connection to ground shorts out internal power supply regulator for operation below 3.5 V.
7	OSC	Oscillator input. External clock input to this pin will override the internal oscillator. The internal oscillator frequency can be slowed by connecting an external capacitor between this pin and ground. (See Figure 8.)
8	V+	Input voltage connection.

**APPLICATIONS**

The Siliconix Si7660 is a VOLTAGE source, not a CURRENT source. Therefore, any heavy load current will either greatly reduce the output voltage (possibly out of the desired range) or cause the device to go into power shutdown. To avoid problems, keep the VOLTAGE conversion concept in mind.

The Si7660 is intended for use as a voltage inverter. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. Some of the possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication. For more information refer to Application Note AN84-2.

There are many applications where a low current negative supply made with an Si7660 would do just as well as a full conventional negative supply or dc-to-dc converter module. Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems.

If the output ripple of the Si7660 is too great for a particular application, the value of the pump (C<sub>1</sub>, Fig. 10) and reservoir (C<sub>2</sub>, Fig. 10) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device.

The maximum recommended capacitor size is 1000 μF.

The previous version of the Si7660 required a diode in series with pin 5 when operating above 6.5 V. The improved Si7660 does not require this diode. The improved version will work in existing circuits which have the diode.

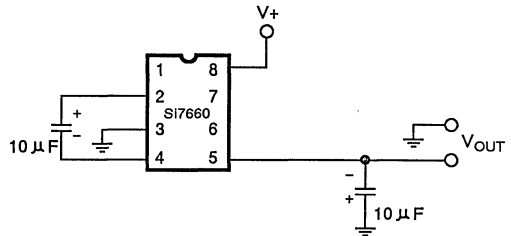


Figure 10. Basic Voltage Inverter Circuit

Figure 11 shows a circuit that will produce two output voltages utilizing both of the Si7660 features (i.e. inversion and doubling). The combined output current must be limited so the maximum device dissipation is not exceeded.

Two Si7660's can be paralleled to reduce the effective output resistance of the converter. The output voltage at a given current is increased since the voltage drop is halved when the devices are connected as shown in Figure 12.

## APPLICATIONS (Cont'd)

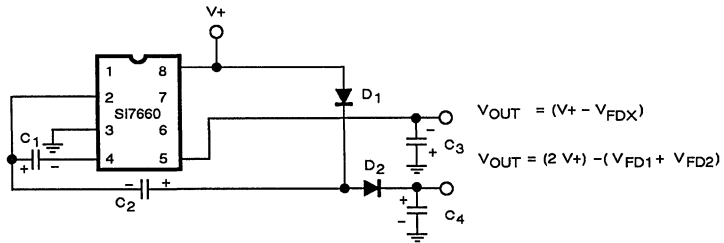


Figure 11. Combination Inverter/Multiplier Circuit

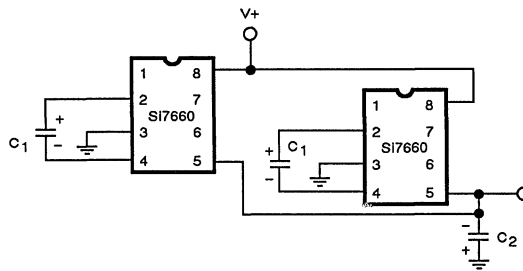
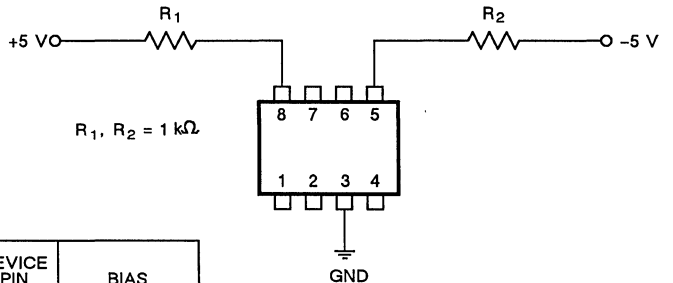
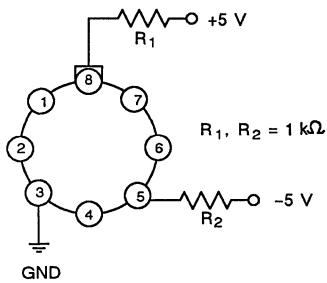


Figure 12. Paralleling Two Si7660's to Reduce the Effective Output Resistance

## BURN-IN DIAGRAM



DEVICE PIN	BIAS
1	NC
2	NC
3	GND
4	NC
5	R <sub>2</sub> to -5 V
6	NC
7	NC
8	R <sub>1</sub> to +5 V



# Si7661 Monolithic CMOS Voltage Converter

## FEATURES

- Conversion of +4.5 V to +20 V Logic Supply to -4.5 V to -20 V Supplies
- Voltage Multiplication ( $V_{OUT} = (-) nV_{IN}$ )
- 99.7% Typical Open Circuit Voltage Conversion Efficiency
- 95% Typical Power Efficiency

## BENEFITS

- Inexpensive Negative Supply Generation
- Easy to Use, Requires Only 2 External Capacitors
- Minimum Parts Count
- Small Size

## APPLICATIONS

- On board Negative Supply for Dynamic RAMs
- Localized  $\mu$ -Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies for Analog Switches
- Data Acquisition Systems
- Up to -20 V for Op Amps, and other Linear Circuits

## DESCRIPTION

The Siliconix Si7661 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7661 performs a supply voltage conversion from positive to negative for an input range of +4.5 V to +20 V, resulting in a complementary output voltage of -4.5 V to -20 V with the addition of only 2 capacitors.

Typical applications for the Si7661 are data acquisition and microprocessor based systems, where a +4.5 to +20 V supply is available for the digital functions, and an additional -5 to -20 V supply is required for analog devices, such as op amps. The Si7661 is also ideally suited for providing low current, -5 V body bias supply for dynamic RAMs.

Contained on the chip are a voltage regulator, RC oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and ensures that the output N-channel switch substrates are not forward-biased. An epitaxial layer prevents latchup.

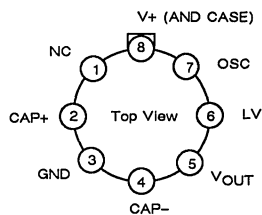
The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 4.5 to 20 V. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low

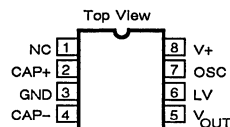
voltage (LV) operation. At high voltages (+8 to +20 V), the "LV" pin should be left disconnected.

Packaging for this device includes 8-pin metal can and plastic MiniDIP options. Performance grades include military, A suffix (-55 to 125°C), industrial, D suffix (-40 to 85°C), and commercial, C suffix (0 to 70°C) temperature ranges. For more information refer to AN84-2.

## PIN CONFIGURATION

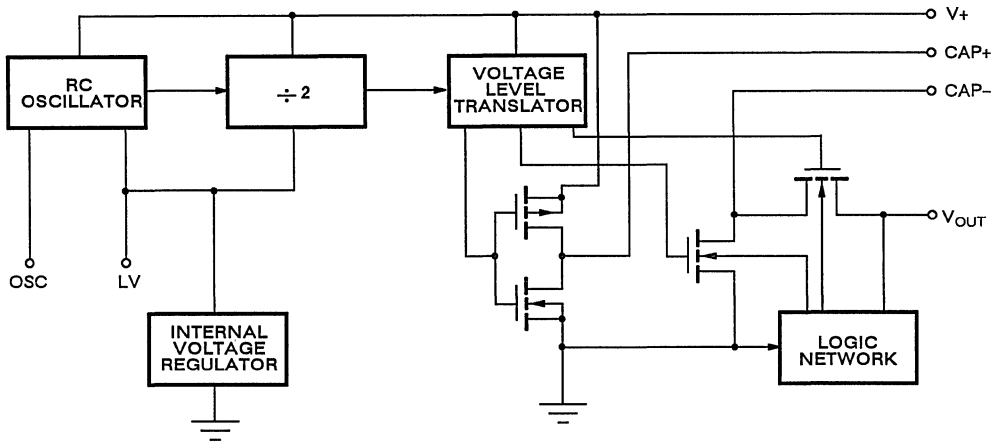


Order Numbers:  
SI7661AA, SI7661BA, SI7661CA



Order Number:  
Plastic: SI7661CJ

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	22 V
Oscillator Input Voltage .....	-0.3 V to (V <sub>+</sub> + 0.3 V) for V <sub>+</sub> < 8 V
.....	(V <sub>+</sub> - 8 V) to (V <sub>+</sub> + 0.2 V) for V <sub>+</sub> > 8 V
LV .....	No Connection for V <sub>+</sub> > 9 V
Storage Temperature (A & B Suffix) .....	-65 to 150°C
(C Suffix) .....	-65 to 125°C

Operating Temperature (A Suffix) .....	-55 to 125°C
(B Suffix) .....	-25 to 85°C
(C Suffix) .....	0 to 70°C

Power Dissipation*	
8-Pin Metal Can** .....	500 mW
8-Pin Plastic DIP*** .....	500 mW

- \* All leads welded or soldered to PC board.
- \*\* Derate 6 mW/°C above 75°C.
- \*\*\* Derate 6.6 mW/°C above 25°C.

## ELECTRICAL CHARACTERISTICS<sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  C <sub>osc</sub> = 0 <sup>e</sup>	LIMITS				UNIT
			1=25°C 2=125, 85, 70 °C 3=-55, -25, 0 °C		A, B, C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>INPUT</b>							
Supply Voltage Range (LV)	V <sub>+ LV</sub>	R <sub>L</sub> = 10 kΩ, LV = 0 V	1, 2, 3		4.5	9	V
Supply Voltage Range	V <sub>+</sub>	R <sub>L</sub> = 10 kΩ, LV OPEN	1, 2, 3		8	20	
Supply Current	I <sub>+</sub>	V <sub>+</sub> = 4.5 V, R <sub>L</sub> = ∞, LV = 0 V	1	100		500	μA
		V <sub>+</sub> = 15 V, R <sub>L</sub> = ∞, LV OPEN	1	0.7		2	mA

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $C_{osc} = 0^e$	LIMITS				UNIT
			1=25 °C 2=125,85,70 °C 3=-55,-25,0 °C		A,B,C SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>OUTPUT</b>							
Output Source Resistance	$R_{OUT}$	$V_+ = 4.5\text{ V}, LV = 0\text{ V}$ $I_O = 3\text{ mA}$	1	75			$\Omega$
		$V_+ = 15\text{ V}, LV\text{ OPEN}$ $I_O = 20\text{ mA}$	1,3 2	55		100 120	
Power Conversion Efficiency	$PE_1$	$V_+ = 15\text{ V}, R_L = 2\text{ k}\Omega$	1	92			%
Voltage Conversion Efficiency	$V_{OUT}E_1$	$V_+ = 15\text{ V}, R_L = \infty$	1	99.7	97		
<b>DYNAMIC</b>							
Oscillator Frequency <sup>o</sup>	$f_{osc}$	$V_+ = 15\text{ V}$	1	10			kHz
Oscillator Impedance	$Z_{osc}$	$V_+ = 4.5\text{ V}, LV = 0\text{ V}$	1	1			M $\Omega$
		$V_+ = 15\text{ V}$	1	100			k $\Omega$

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. For  $C_{osc} > 1000\text{ pF}$ ,  $C_1$  and  $C_2$  should be increased to  $100\text{ }\mu\text{F}$ .  $C_1$  = Pump Capacitor,  $C_2$  = Reservoir Capacitor.

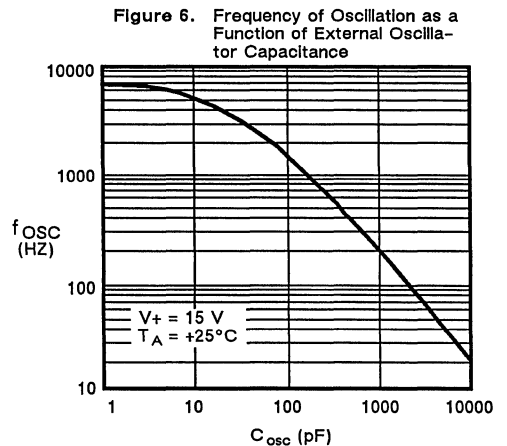
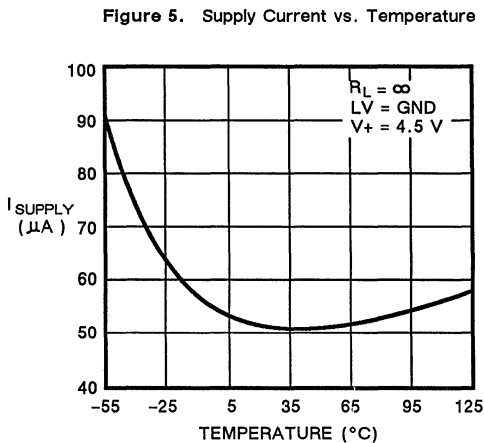
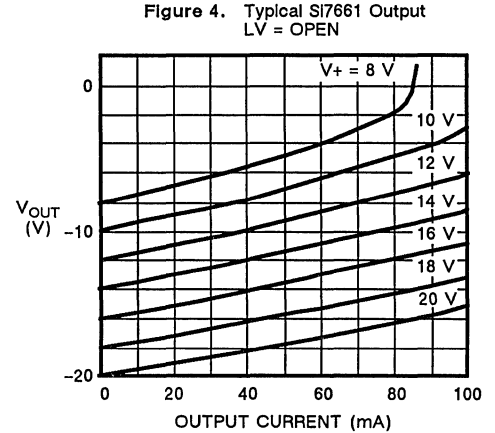
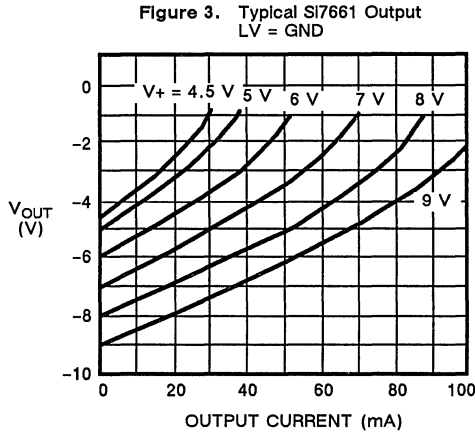
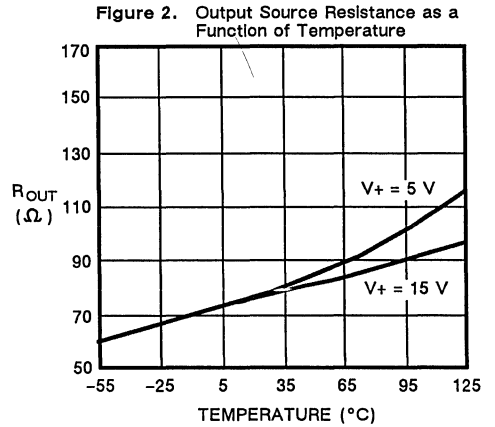
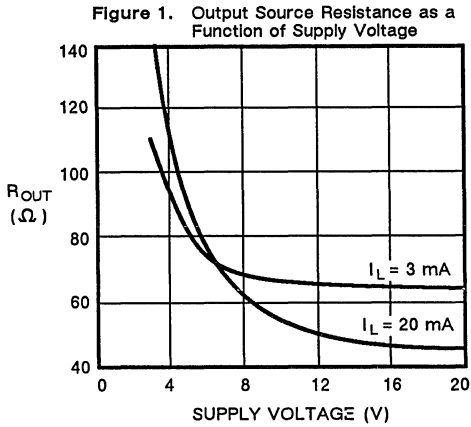
**DIE TOPOGRAPHY**

Pad No.	Function
2	CAP+
3	GND
4	CAP-
5	$V_{OUT}$
6	$V_L$
7	OSC
8	$V_+$

CSHA

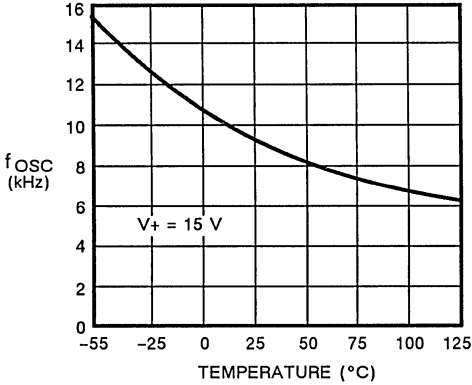
3 Capacitors	47 N-Channel Enhancement Mosfets
1 Resistor	40 P-Channel Enhancement Mosfets
1 Zener Diode	

## TYPICAL CHARACTERISTICS

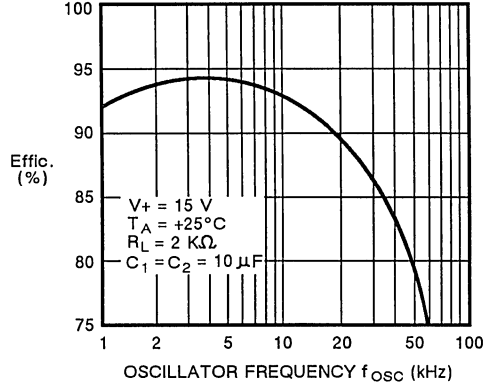


**TYPICAL CHARACTERISTICS**

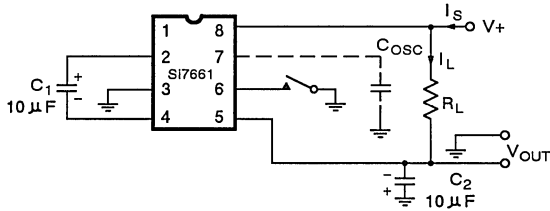
**Figure 7. Unloaded Oscillator Frequency as a Function of Temperature**



**Figure 8. Si7661 Power Efficiency vs. Oscillator Frequency**



**SWITCHING TIME TEST CIRCUIT**



**PIN DESCRIPTION**

PIN NUMBER	SYMBOL	PIN DESCRIPTION
1	NC	No connection.
2	CAP+	Positive terminal connection for pump capacitor.
3	GND	Input and/or output ground reference.
4	CAP-	Negative terminal connection for pump capacitor.
5	V <sub>OUT</sub>	Output of the voltage converter.
6	LV	Low Voltage. Connection to ground shorts out internal power supply regulator for operation below 9.0 volts.
7	OSC	Oscillator input. External clock input to this pin will override the internal oscillator. The internal oscillator frequency can be slowed by connecting an external capacitor between this pin and ground. (See figure 6.)
8	V <sub>+</sub>	Input voltage connection.

## APPLICATION HINTS

The Siliconix Si7661 device is a VOLTAGE source, not a CURRENT source. Therefore, any heavy load current will either greatly reduce the output voltage (possibly out of the desired range) or will cause the device to go into power shutdown. To avoid problems, keep the VOLTAGE conversion concept in mind.

The Si7661 is intended for use as a voltage inverter. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. Some of the possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication. For more information refer to Application Note AN84-2.

There are many applications where a low current negative supply made with an Si7661 would do just as well as a full conventional negative supply or DC-to-DC converter module. Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems.

In addition, the extended input voltage range of the Si7661 lends itself for use as a negative generator for most op-amp applications.

If the output ripple of the Si7661 is too great for a particular application, the value of the pump ( $C_1$ , figure 9) and reservoir ( $C_2$ ) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device. The maximum recommended capacitor size is 1000  $\mu\text{F}$ .

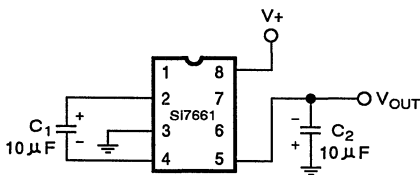


Figure 9. Basic Inverter Circuit

When an external clock is used to drive the Si7661 a 1000  $\Omega$  resistor should be used between the clock source and the OSC input (pin 7) as shown in Figure 10.

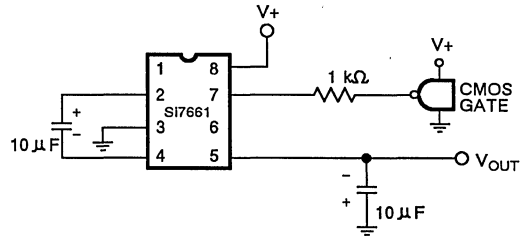
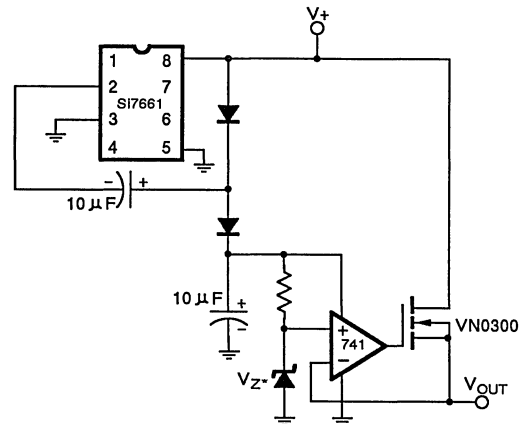


Figure 10. Driving the Si7661 with an External Clock

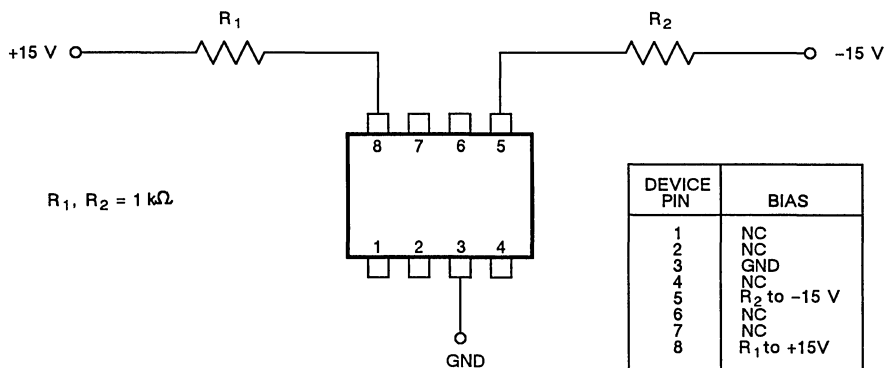
Figure 11 shows a regulator that will operate with much less than 1 volt drop between  $V_+$  and  $V_{OUT}$  at large output currents. Most three terminal voltage regulators would exhibit a drop of a volt or more under these conditions.



\* The Zener Voltage sets the output of the regulator.

Figure 11. Low Loss Regulator Circuit

**BURN-IN DIAGRAM**



# Si9100/9101

## 1-Watt, High-Voltage Switchmode Regulators

### FEATURES

- 10 to 70 V Input Range
- Current-mode Control
- On chip 150 V, 5  $\Omega$  MOSFET Switch
- Reference Selection  
Si9100 –  $\pm 1\%$   
Si9101 –  $\pm 10\%$
- High Efficiency Operation  
( $> 80\%$ )
- Internal Start-up Circuit
- Internal Oscillator  
(up to 1 MHz)

### APPLICATIONS

- ISDN Terminals
- PBX Equipment
- Modems
- Feature Telephones
- DC/DC Converters
- Distributed Power Systems

### DESCRIPTION

The Si9100/Si9101 high-voltage switchmode regulators are monolithic D/CMOS integrated circuits which contain most of the components necessary to implement a 1-watt, high-efficiency dc to dc converter. They can either be operated from a low-voltage dc supply, or directly from a 10 to 70 V unregulated dc power source.

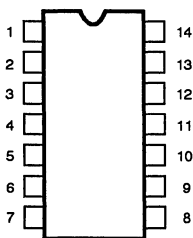
The switchmode regulator subsystem includes high-voltage start-up circuitry, oscillator, voltage reference, current-mode PWM circuitry and a high-speed, 150 V, 5  $\Omega$  MOSFET switch. Additional features include primary current sense,

SHUTDOWN and RESET logic inputs, and external clock synchronization. This device may be used with an appropriate transformer to implement most single ended isolated power converter topologies (i.e., flyback and forward), or by using an external reference can generate a +5 V non-isolated output from a -48 V source.

The Si9100/Si9101 is available in 14-pin plastic, CerDIP and PLCC 20-pin packages, and is specified over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

### PIN CONFIGURATION

Dual-In-Line Package

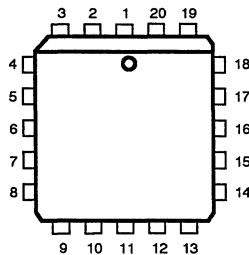


Top View

Order Numbers:

CerDIP:  
Si9100AK, Si9101AK  
Plastic:  
Si9100DJ, Si9101DJ

PLCC Package



Top View

Order Number:

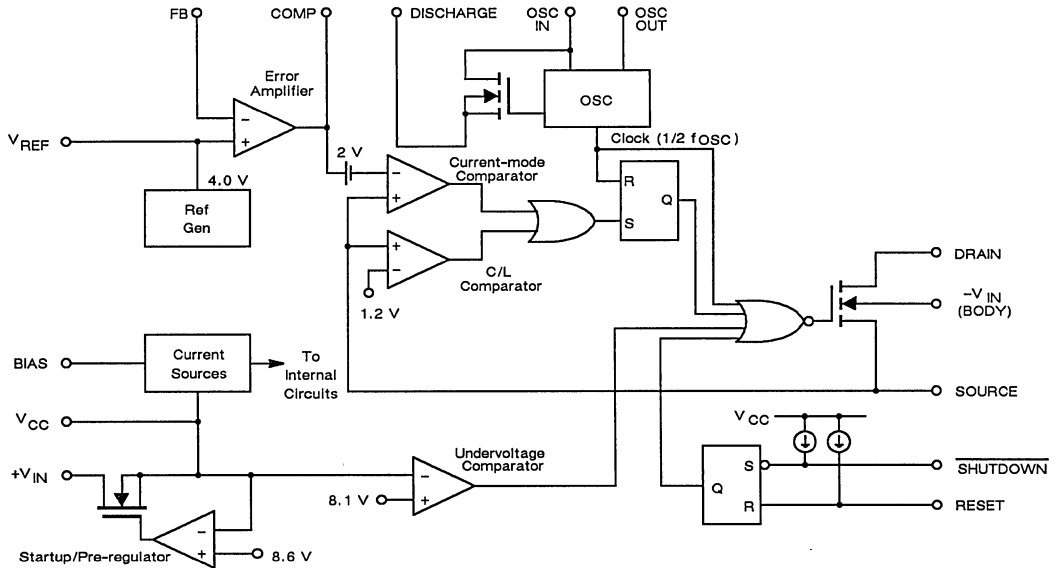
Si9100DN, Si9101DN

FUNCTION	14-pin DIP Pin #	PLCC-20* Pin #
BIAS	1	2
+VIN	2	3
DRAIN	3	5
SOURCE	4	7
-VIN	5	8
VCC	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
VREF	10	14
SHUTDOWN	11	16
RESET	12	17
COMP	13	18
FB	14	20

\* Pins 1, 4, 6, 13, 15 and 19 = N/C



**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to  $-V_{IN}$

$V_{CC}$ .....	15.0 V
$+V_{IN}$ .....	70 V
$V_{DS}$ .....	150 V
$I_D$ (Peak) (Note 1) .....	2.5 A
$I_D$ (rms) .....	350 mA

Logic Inputs (RESET, SHUTDOWN, OSC IN) .....

Linear Inputs (FEEDBACK, SOURCE) .....	-0.3 V to 7.0 V
HV Preregulator Input Current (continuous) .....	3 mA

Note 1: 300  $\mu$ s pulse, 2% duty cycle

Storage Temperature (A Suffix) .....	-65 to 150°C
(D Suffix) .....	-65 to 125°C

Operating Temperature (A Suffix) .....	-55 to 125°C
(D Suffix) .....	-40 to 85°C

Junction Temperature ( $T_J$ ) .....

Power Dissipation (Package) *	
14-Pin Ceramic DIP (K Suffix) ** .....	1000 mW
14-Pin Plastic DIP (J Suffix) *** .....	750 mW
20-Pin PLCC (N Suffix) **** .....	1400 mW

Thermal Impedance ( $\theta_{JA}$ )	
14-Pin Ceramic DIP .....	100°C/W
14-Pin Plastic DIP .....	167°C/W
20-Pin PLCC .....	90°C/W

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 10 mW/°C above 50°C

\*\*\* Derate 6 mW/°C above 25°C

\*\*\*\* Derate 11 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS <sup>a</sup>										
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS							UNIT
			1=25°C		A SUFFIX		D SUFFIX			
			2=125,85°C		-55 to 125°C		-40 to 85°C			
			3=-55,-40°C		MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
		TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>			
<b>REFERENCE</b>										
Output Voltage	$V_R$	$R_L = 10\text{ M}\Omega$ (See Detailed Description)	1	4.0						V
Output Impedance	$Z_{OUT}$		1	30						k $\Omega$
Short Circuit Current		$V_{REF} = -V_{IN}$	1	100						$\mu\text{A}$
Temperature Stability			2,3	1						mV/°C
<b>OSCILLATOR</b>										
Maximum Frequency	$f_{OSC}$	$R_{OSC} = 0$	1	3	1		1			MHz
Initial Accuracy		See Note e	1	100	80	120	80	120		kHz
Voltage Stability	$V_{OSC}$	$9.5\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	1	$\pm 3$						%
Temperature Coefficient			2,3	500						ppm/°C
<b>ERROR AMPLIFIER</b>										
Feedback Input Voltage	$V_{FB}$	FB Tied to COMP See Detailed Description Reference Section	Si9100	1	4.00	3.96	4.04	3.96	4.04	V
			Si9101	1	4.00	3.60	4.40	3.60	4.40	
Input BIAS Current		$V_{FB} = 4.0\text{ V}$	1	25		500		500		nA
Open Loop Voltage Gain	$A_{VOL}$		1	80	60		60			dB
Unity Gain Bandwidth			1	1						MHz
Output Impedance	$Z_{OUT}$		1	50						k $\Omega$
Output Current	$I_{OUT}$	Source $V_{FB} = 3.4\text{ V}$	1	2.0	1.4		1.4		mA	
		Sink $V_{FB} = 4.5\text{ V}$	1	0.15	.12		.12			
Power Supply Rejection	PSRR	$9.5\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	1	70						dB

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS						UNIT
			1=25°C 2=125,85°C 3=-55,-40°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>CURRENT LIMIT</b>									
Threshold Voltage	$V_{SOURCE}$	$R_L = 100\ \Omega$ , from DRAIN to $V_{CC}$ $V_{FB} = 0\text{ V}$	1	1.2	1.0	1.4	1.0	1.4	V
Delay to Output	$t_d$	$R_L = 100\ \Omega$ , from DRAIN to $V_{CC}$ $V_{SOURCE} = 1.4\text{ V}$ , See Figure 1	1	150		200		200	ns
<b>PREREGULATOR/STARTUP</b>									
Input Voltage	$+V_{IN}$	$I_{IN} = 100\ \mu\text{A}$	1			70		70	V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq 9.4\text{ V}$	1			10		10	$\mu\text{A}$
$V_{CC}$ Preregulator Turn-OFF Threshold Voltage		$I_{PREREGULATOR} = 10\ \mu\text{A}$	1	8.6		9.4		9.4	V
Undervoltage Lockout		$R_L = 100\ \Omega$ , from DRAIN to $V_{CC}$ (See Detailed Description)	1	8.1		8.9		8.9	
<b>SUPPLY</b>									
Supply Current	$I_{CC}$		1	0.6		1.0		1.0	mA
Bias Current	$I_{BIAS}$		1	15					$\mu\text{A}$
<b>LOGIC</b>									
SHUTDOWN Delay	$t_{SD}$	$V_{SOURCE} = -V_{IN}$ See Figure 2	1	50		100		100	ns
SHUTDOWN Pulse Width	$t_{SW}$	See Figure 3	1		50		50		
RESET Pulse Width	$t_{RW}$		1		50		50		
Latching Pulse Width SHUTDOWN and RESET LOW	$t_{LW}$		1		25		25		
Input LOW Voltage	$V_{IL}$		1			2.0		2.0	V
Input HIGH Voltage	$V_{IH}$		1		8.0		8.0		
Input Current Input Voltage HIGH	$I_{IH}$	$V_{IN} = 10\text{ V}$	1	1		5		5	$\mu\text{A}$
Input Current Input Voltage LOW	$I_{IL}$	$V_{IN} = 0\text{ V}$	1	-25		-35		-35	

**10**

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>MOSFET SWITCH</b>									
Breakdown Voltage	$V_{(BR)DSS}$	$V_{SOURCE} = V_{SHUTDOWN} = 0\text{ V}$ $I_{DRAIN} = 100\text{ }\mu\text{A}$	2,3	180	150		150		V
Drain-Source ON Resistance <sup>f</sup>	$r_{DS(ON)}$	$V_{SOURCE} = 0\text{ V}$ $I_{DRAIN} = 100\text{ mA}$	1	3		5		5	$\Omega$
Drain OFF Leakage Current	$I_{DSS}$	$V_{SOURCE} = V_{SHUTDOWN} = 0\text{ V}$ $V_{DRAIN} = 100\text{ V}$	1			10		10	$\mu\text{A}$
Drain Capacitance	$C_{DS}$	$V_{SOURCE} = V_{SHUTDOWN} = 0\text{ V}$	1	250					pF

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e.  $C_{STRAY}$  Pin 8 = 0 pF.
- f. Temperature coefficient of  $r_{DS(ON)}$  is 0.75% per °C, typical.

## TIMING WAVEFORMS

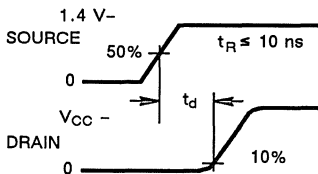


Figure 1

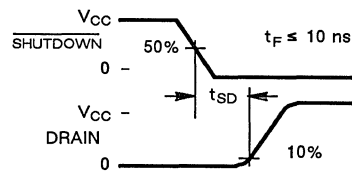


Figure 2

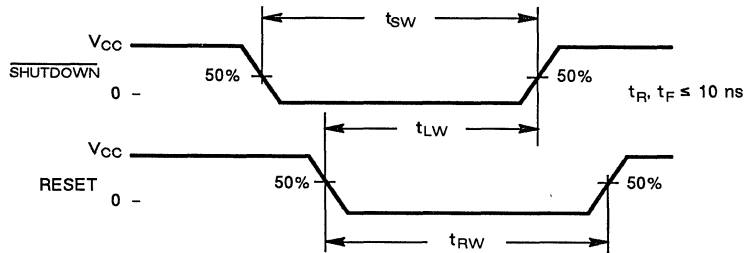


Figure 3

**TYPICAL CHARACTERISTICS**

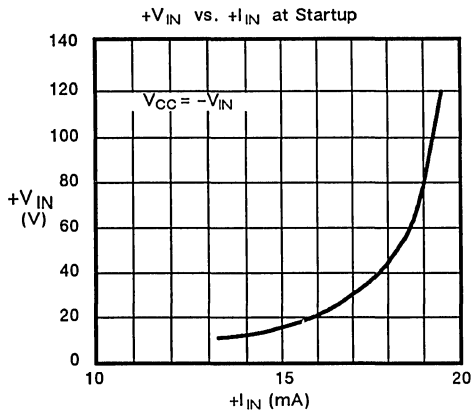


Figure 4

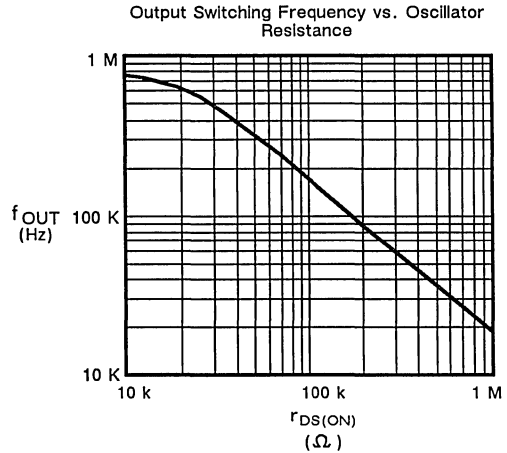


Figure 5

**DETAILED DESCRIPTION**

**PREREGULATOR/STARTUP SECTION**

Due to the low quiescent current requirement of the Si9100 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary “bootstrap” winding on the output inductor or transformer.

When power is first applied during startup, +V<sub>IN</sub> (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between +V<sub>IN</sub> and V<sub>CC</sub> (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V<sub>CC</sub> pin. The constant current is disabled when V<sub>CC</sub> exceeds 8.6 V. If V<sub>CC</sub> is not forced to exceed the 8.6 V threshold, then V<sub>CC</sub> will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V<sub>CC</sub> exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation

can be minimized by providing an external power source to V<sub>CC</sub> such that the constant current source is always disabled.

**NOTE:** During startup or when V<sub>CC</sub> drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start up time can result in device damage. See Figure 4 for calculation of power dissipation during start up.

**BIAS**

To properly set the bias for the Si9100, a 390 kΩ resistor should be tied from BIAS (pin 1) to -V<sub>IN</sub> (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the SHUTDOWN and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

**REFERENCE SECTION**

The reference section of the Si9100 consists of a temperature compensated buried zener and trimmable divider network. The output of the reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4.0 V. This automatically compensates for the input offset voltage in the error amplifier.

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**DETAILED DESCRIPTION (Cont'd)**


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The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9101 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a dc bias point for the error amplifier.

#### ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier ( $V_{REF}$ ) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

#### OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to  $-V_{IN}$  for normal internal oscillator operation. A frequency divider in

the logic section limits switch duty cycle to  $\leq 50\%$  by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude, typical values would be 1000 pF in series with 10 k $\Omega$  to pin 8.

#### SHUTDOWN AND RESET



SHUTDOWN (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, SHUTDOWN can be either a latched or unlatched input. The output is OFF whenever SHUTDOWN is low. By simultaneously having SHUTDOWN and RESET low, the latch is set and SHUTDOWN has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the SHUTDOWN or RESET pins to provide variable shutdown time.

#### OUTPUT SWITCH

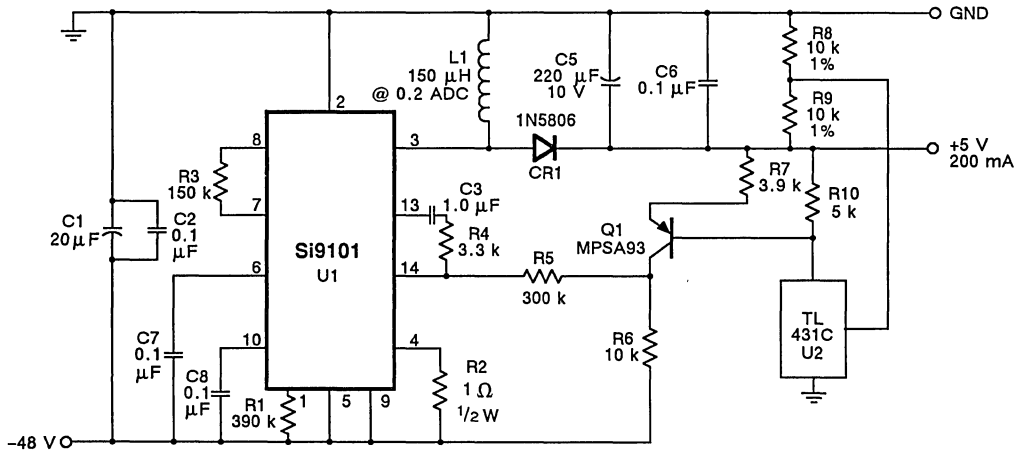
The output switch is a 5  $\Omega$ , 150 V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9100 is connected internally to  $-V_{IN}$  and is independent of the SOURCE.

Table 1. Truth Table for the SHUTDOWN and RESET Pins.

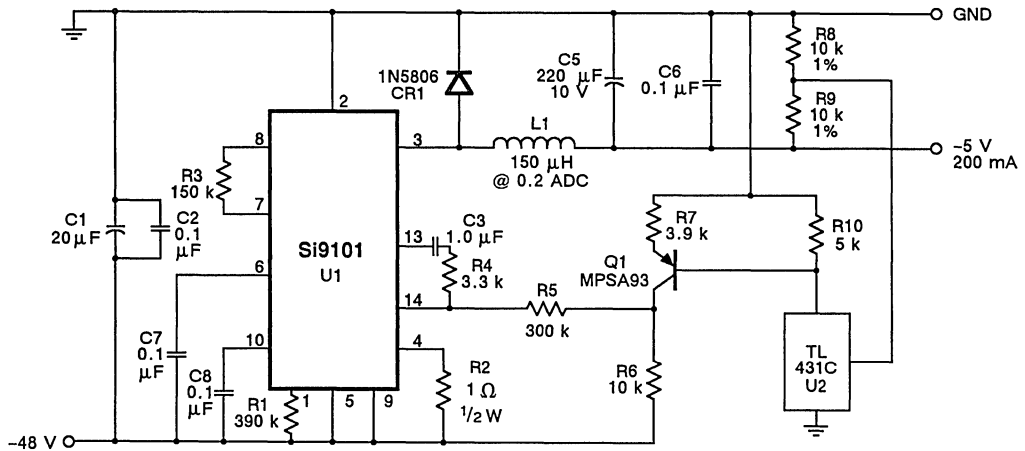
SHUTDOWN	RESET	OUTPUT
H	H	Normal Operation
H		Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
	L	OFF (Latched) (No Change)

APPLICATIONS

BUCK-BOOST  
NON-ISOLATED 1 W SUPPLY

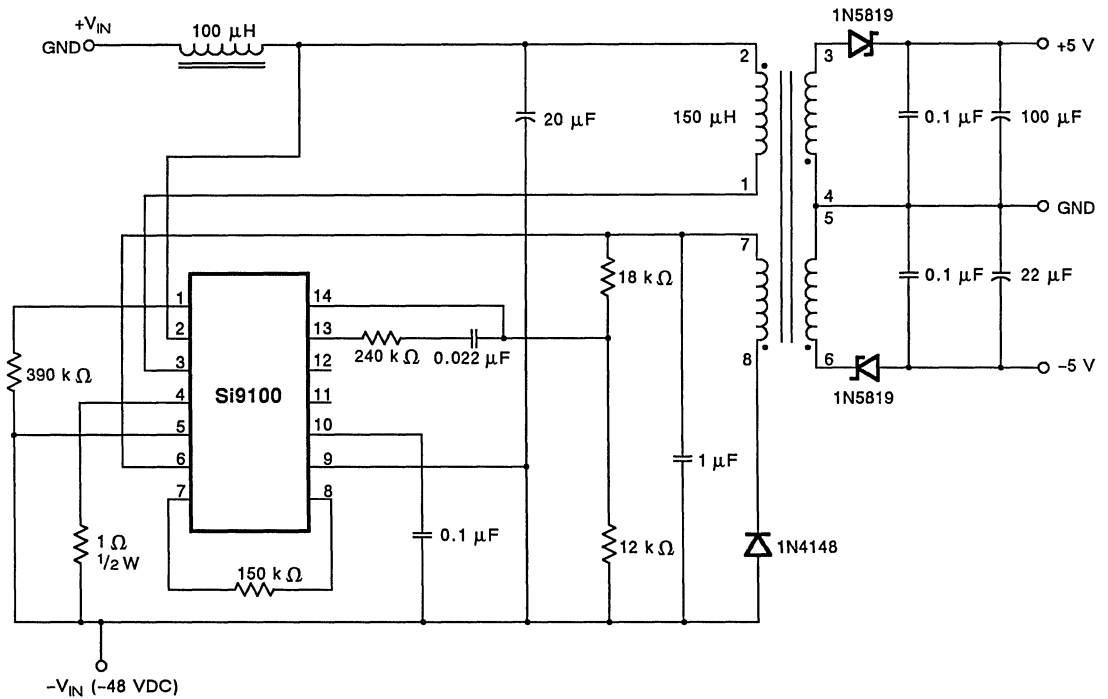


NON-ISOLATED 1 W SUPPLY (BUCK)



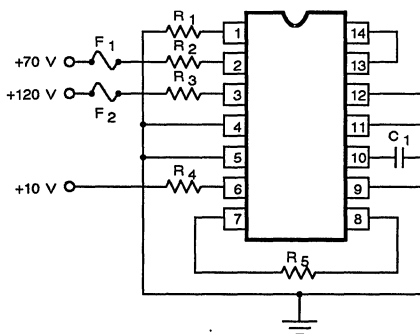
## APPLICATIONS (Cont'd)

### ONE WATT FLYBACK CONVERTER FOR TELECOMMUNICATIONS POWER SUPPLIES \*



\* For additional information on using the Si9100 in telecommunications and ISDN power supplies, see AN87-1 and AN87-2.

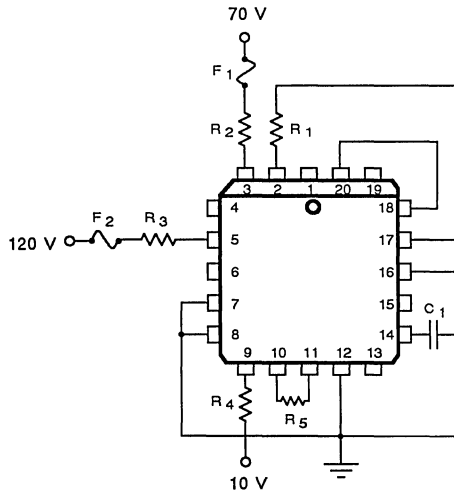
## DUAL-IN-LINE BURN-IN CIRCUIT



- NOTES:
1.  $R_1 = 390 \text{ k}\Omega$ , 1/4 W
  2.  $R_2$  &  $R_3 = 1 \text{ k}\Omega$ , 2 W
  3.  $R_4 = 100 \Omega$ , 1/4 W
  4.  $R_5 = 330 \text{ k}\Omega$ , 1/4 W
  5.  $F_1, F_2 = 1/16 \text{ A}$
  6.  $C_1 = 0.1 \mu\text{F}$ , 50 V



## PLCC BURN-IN CIRCUIT



- NOTES:
1.  $R_1 = 390\text{ k}\Omega$ , 1/4 W
  2.  $R_2$  &  $R_3 = 1\text{ k}\Omega$ , 2 W
  3.  $R_4 = 100\Omega$ , 1/4 W
  4.  $R_5 = 330\text{ k}\Omega$ , 1/4 W
  5.  $F_1, F_2 = 1/16\text{ A}$
  6.  $C_1 = 0.1\text{ }\mu\text{F}$ , 50 V

# 1-Watt, High-Voltage Switchmode Regulator

## FEATURES

- 10 to 120 V Input Range
- Current-mode Control
- On chip 200 V, 7  $\Omega$  MOSFET Switch
- SHUTDOWN and RESET Function
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (up to 1 MHz)

## APPLICATIONS

- ISDN Terminals
- PBX Equipment
- Modems
- Feature Telephones
- DC/DC Converters
- Distributed Power Systems

## DESCRIPTION

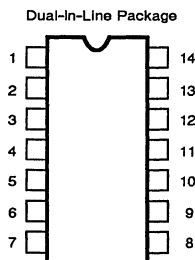
The Si9102 high-voltage switchmode regulator is a monolithic D/CMOS integrated circuit which contains most of the components necessary to implement a 1-watt, high-efficiency dc to dc converter. It can either be operated from a low-voltage dc supply, or directly from a 10 to 120 V unregulated dc power source.

The switchmode regulator subsystem includes high-voltage start-up circuitry, oscillator, voltage reference, current-mode PWM circuitry and a high-speed, 200 V, 7  $\Omega$  MOSFET switch. Additional features include primary current sense,

SHUTDOWN and RESET logic inputs, and external clock synchronization. This device may be used with an appropriate transformer to implement most single ended isolated power converter topologies (i.e., flyback and forward), or by using an external reference can generate a +5 V non-isolated output from a -10 to -96 V source.

The Si9102 is available in 14-pin plastic, CerDIP and 20-pin PLCC packages, and is specified over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

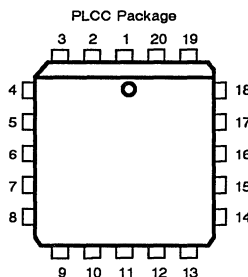
## PIN CONFIGURATION



Top View

Order Numbers:

Plastic: Si9102AJ  
CerDIP: Si9102DK



Top View

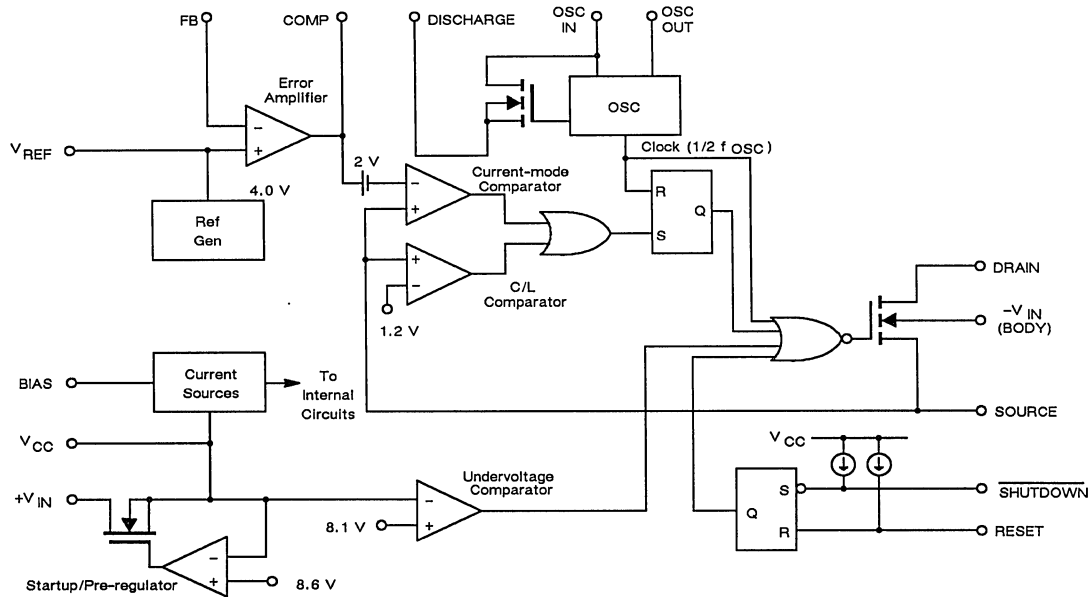
Order Number:

Plastic: Si9102DN

FUNCTION	14-pin DIP Pin #	PLCC-20* Pin #
BIAS	1	2
+VIN	2	3
DRAIN	3	5
SOURCE	4	7
-VIN	5	8
V <sub>CC</sub>	6	9
OSC OUT	7	10
OSC IN	8	11
DISCHARGE	9	12
V <sub>REF</sub>	10	14
SHUTDOWN	11	16
RESET	12	17
COMP	13	18
FB	14	20

\* Pins 1, 4, 6, 13, 15 and 19 = N/C

**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Voltages Referenced to  $-V_{IN}$

$V_{CC}$ .....	15.0 V
$+V_{IN}$ .....	120 V
$V_{DS}$ .....	200 V
$I_D$ (Peak) (Note 1) .....	2 A
$I_D$ (rms) .....	250 mA

Logic Inputs (RESET, SHUTDOWN, OSC IN) ..... -0.3 V to  $V_{CC} + 0.3$  V

Linear Inputs (FEEDBACK, SOURCE) ..... -0.3 V to 7.0 V

HV Preregulator Input Current (continuous) ..... 3 mA

Note 1: 300  $\mu$ s pulse, 2% duty cycle

Storage Temperature (A Suffix) .....	-65 to 150°C
(D Suffix) .....	-65 to 125°C

Operating Temperature (A Suffix) .....	-55 to 125°C
(D Suffix) .....	-40 to 85°C

Junction Temperature ( $T_J$ ) ..... 150°C

Power Dissipation (Package)*	
14-Pin Ceramic DIP (K Suffix)**	1000 mW
14-Pin Plastic DIP (J Suffix)***	750 mW
20-Pin PLCC (N Suffix)****	1400 mW

Thermal Impedance ( $\theta_{JA}$ )	
14-Pin Ceramic DIP .....	100°C/W
14-Pin Plastic DIP .....	167°C/W
20-Pin PLCC .....	90°C/W

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 10 mW/°C above 50°C

\*\*\* Derate 6 mW/°C above 25°C

\*\*\*\* Derate 11 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS						UNIT
					A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>REFERENCE</b>									
Output Voltage	$V_R$	$R_L = 10\text{ M}\Omega$ (See Detailed Description)	1	4.0					V
Output Impedance	$Z_{OUT}$		1	30					$\text{k}\Omega$
Short Circuit Current		$V_{REF} = -V_{IN}$	1	100					$\mu\text{A}$
Temperature Stability			2,3	1					$\text{mV}/^\circ\text{C}$
<b>OSCILLATOR</b>									
Maximum Frequency	$f_{OSC}$	$R_{OSC} = 0$	1	3	1		1		MHz
Initial Accuracy		See Note e	1	100	80	120	80	120	kHz
Voltage Stability	$V_{OSC}$	$9.5\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	1	$\pm 3$					%
Temperature Coefficient			2,3	500					$\text{ppm}/^\circ\text{C}$
<b>ERROR AMPLIFIER</b>									
Feedback Input Voltage	$V_{FB}$	FB Tied to COMP (See Detailed Description Reference Section)	1	4.00	3.96	4.04	3.96	4.04	V
Input BIAS Current		$V_{FB} = 4.0\text{ V}$	1	25		500		500	nA
Open Loop Voltage Gain	$A_{VOL}$		1	80	60		60		dB
Unity Gain Bandwidth			1	1					MHz
Output Impedance	$Z_{OUT}$		1	50					$\text{k}\Omega$
Output Current	$I_{OUT}$	Source $V_{FB} = 3.4\text{ V}$	1	2.0	1.4		1.4		mA
		Sink $V_{FB} = 4.5\text{ V}$	1	0.15	.12		.12		
Power Supply Rejection	PSRR	$9.5\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	1	70					dB

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			2=125,85°C		-55 to 125°C		-40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>CURRENT LIMIT</b>									
Threshold Voltage	$V_{SOURCE}$	$R_L = 100\ \Omega$ , from DRAIN to $V_{CC}$ $V_{FB} = 0\text{ V}$	1	1.2	1.0	1.4	1.0	1.4	V
Delay to Output	$t_d$	$R_L = 100\ \Omega$ , from DRAIN to $V_{CC}$ $V_{SOURCE} = 1.4\text{ V}$ , See Figure 1	1	150		200		200	ns
<b>PREREGULATOR/STARTUP</b>									
Input Voltage	$+V_{IN}$	$I_{IN} = 100\ \mu\text{A}$	1			120		120	V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq 9.4\text{ V}$	1			10		10	$\mu\text{A}$
$V_{CC}$ Preregulator Turn-OFF Threshold Voltage		$I_{PREREGULATOR} = 10\ \mu\text{A}$	1	8.6		9.4		9.4	V
Undervoltage Lockout		$R_L = 100\ \Omega$ , from DRAIN to $V_{CC}$ (See Detailed Description)	1	8.1		8.9		8.9	
<b>SUPPLY</b>									
Supply Current	$I_{CC}$		1	0.6		1.0		1.0	mA
Bias Current	$I_{BIAS}$		1	15					$\mu\text{A}$
<b>LOGIC</b>									
SHUTDOWN Delay	$t_{SD}$	$V_{SOURCE} = -V_{IN}$ See Figure 2	1	50		100		100	ns
SHUTDOWN Pulse Width	$t_{SW}$	See Figure 3	1		50		50		
RESET Pulse Width	$t_{RW}$		1		50		50		
Latching Pulse Width SHUTDOWN and RESET LOW	$t_{LW}$		1		25		25		
Input LOW Voltage	$V_{IL}$			1			2.0		2.0
Input HIGH Voltage	$V_{IH}$		1		8.0		8.0		
Input Current Input Voltage HIGH	$I_{IH}$	$V_{IN} = 10\text{ V}$	1	1		5		5	$\mu\text{A}$
Input Current Input Voltage LOW	$I_{IL}$	$V_{IN} = 0\text{ V}$	1	-25		-35		-35	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>MOSFET SWITCH</b>									
Breakdown Voltage	$V_{(BR)DSS}$	$V_{SOURCE} = V_{SHUTDOWN} = 0\text{ V}$ $I_{DRAIN} = 100\text{ }\mu\text{A}$	2,3	220	200		200		V
Drain-Source ON Resistance <sup>e</sup>	$r_{DS(ON)}$	$V_{SOURCE} = 0\text{ V}$ $I_{DRAIN} = 100\text{ mA}$	1	5		7		7	$\Omega$
Drain OFF Leakage Current	$I_{DSS}$	$V_{SOURCE} = V_{SHUTDOWN} = 0\text{ V}$ $V_{DRAIN} = 100\text{ V}$	1			10		10	$\mu\text{A}$
Drain Capacitance	$C_{DS}$	$V_{SOURCE} = V_{SHUTDOWN} = 0\text{ V}$	1	250					pF

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. Temperature coefficient of  $r_{DS(ON)}$  is 0.75% per °C, typical.
- f.  $C_{STRAY}$  Pin 8 = 0 pF.

## TIMING WAVEFORMS

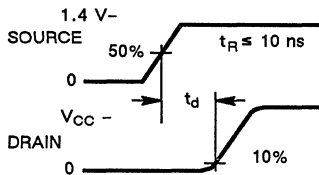


Figure 1

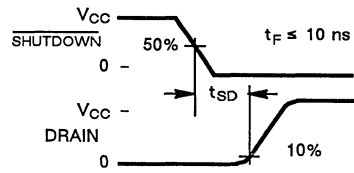


Figure 2

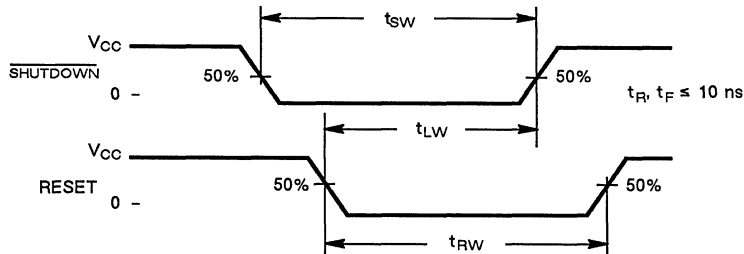


Figure 3

TYPICAL CHARACTERISTICS

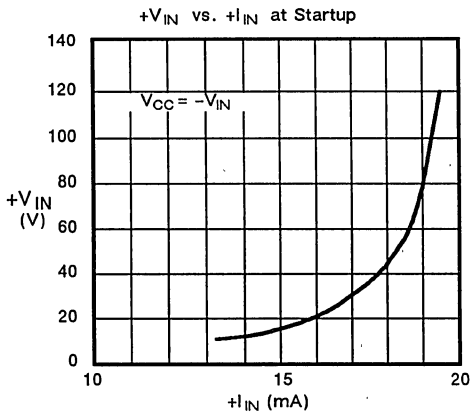


Figure 4

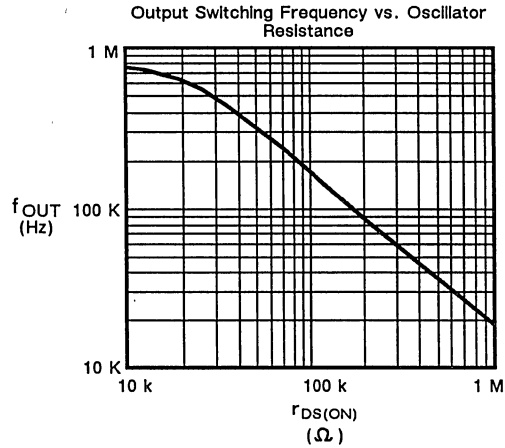


Figure 5

DETAILED DESCRIPTION

PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9102 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary "bootstrap" winding on the output inductor or transformer.

When power is first applied during startup, +V<sub>IN</sub> (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between +V<sub>IN</sub> and V<sub>CC</sub> (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V<sub>CC</sub> pin. The constant current is disabled when V<sub>CC</sub> exceeds 8.6 V. If V<sub>CC</sub> is not forced to exceed the 8.6 V threshold, then V<sub>CC</sub> will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V<sub>CC</sub> exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the

MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V<sub>CC</sub> such that the constant current source is always disabled.

**NOTE:** During startup or when V<sub>CC</sub> drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 96 V input, approximately 2 W). Excessive start up time can result in device damage. See Figure 4 for calculation of power dissipation during start up.

BIAS

To properly set the bias for the Si9102, a 390 kΩ resistor should be tied from BIAS (pin 1) to -V<sub>IN</sub> (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the SHUTDOWN and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

REFERENCE SECTION

The reference section of the Si9102 consists of a temperature compensated buried zener and trimmable divider network. The output of the

---

**DETAILED DESCRIPTION**


---

reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4.0 V. The trimming procedure that is used on the Si9102 brings the output of the error amplifier (which is configured for unity gain during trimming) to within  $\pm 1\%$  of 4.0 V. This automatically compensates for the input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

#### ERROR AMPLIFIER

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier ( $V_{REF}$ ) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

#### OSCILLATOR SECTION

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to  $-V_{IN}$  for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to  $\leq 50\%$  by locking the switching frequency to one half of the oscillator frequency.



Remote synchronization can be accomplished by capacitive coupling of a SYNCHRONIZATION pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude, typical values would be 1000 pF in series with 10 k $\Omega$  to pin 8.

#### SHUTDOWN AND RESET

SHUTDOWN (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, SHUTDOWN can be either a latched or unlatched input. The output is OFF whenever SHUTDOWN is low. By simultaneously having SHUTDOWN and RESET low, the latch is set and SHUTDOWN has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the SHUTDOWN or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the SHUTDOWN and RESET Pins.

SHUTDOWN	RESET	OUTPUT
H	H	Normal Operation
H		Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
	L	OFF (Latched) (No Change)

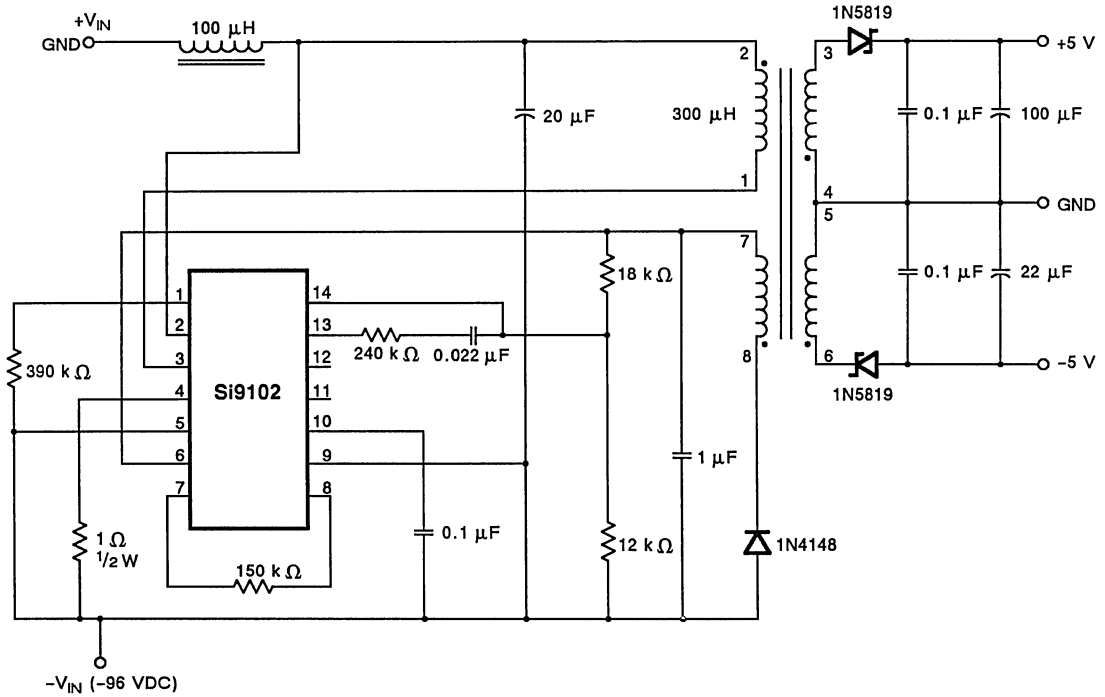
#### OUTPUT SWITCH

The output switch is a 7  $\Omega$ , 200 V lateral DMOS device. Like discrete MOSFETs, the switch contains an intrinsic body-drain diode. However, the body contact in the Si9102 is connected internally to  $-V_{IN}$  and is independent of the SOURCE.

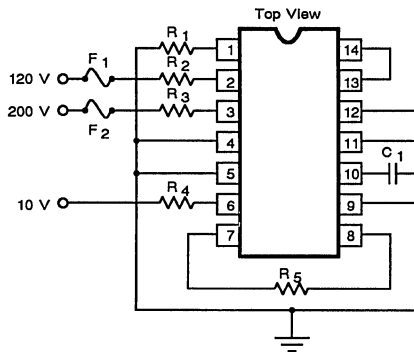


**APPLICATIONS**

**FLYBACK CONVERTER FOR DOUBLE BATTERY TELECOMMUNICATIONS POWER SUPPLIES**

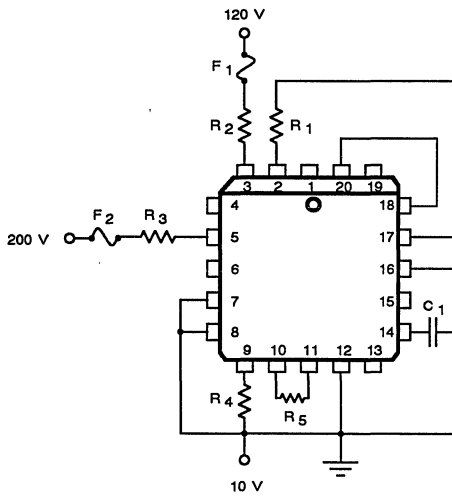


**DUAL-IN-LINE BURN-IN CIRCUIT**



- NOTES:  $R_1 = 390 \text{ k}\Omega$ , 1/4 W  
 $R_2 = 1 \text{ k}\Omega$ , 2 W  
 $R_3 = 1 \text{ k}\Omega$ , 2 W  
 $R_4 = 100 \Omega$ , 1/4 W  
 $R_5 = 330 \text{ k}\Omega$ , 1/4 W  
 $C_1 = 0.1 \mu\text{F}$ , 50 V

## PLCC BURN-IN CIRCUIT



- NOTES:  $R_1 = 390 \text{ k}\Omega$ , 1/4 W  
 $R_2 = 1 \text{ k}\Omega$ , 2 W  
 $R_3 = 1 \text{ k}\Omega$ , 2 W  
 $R_4 = 100 \Omega$ , 1/4 W  
 $R_5 = 330 \text{ k}\Omega$ , 1/4 W  
 $C_1 = 0.1 \mu\text{F}$ , 50 V

# Si9110/9111

## High-voltage Switchmode Controllers

### FEATURES

- 10 to 120 V Input Range
- Current-mode Control
- High-Speed, Source-Sink Output Drive
- High Efficiency Operation (> 80%)
- Internal Start-up Circuit
- Internal Oscillator (up to 1 MHz)
- Reference Selection  
Si9110 –  $\pm 1\%$   
Si9111 –  $\pm 10\%$

### APPLICATIONS

- DC/DC Converters
- Distributed Power Systems
- ISDN Equipment
- PBX Equipment
- Modems

### DESCRIPTION

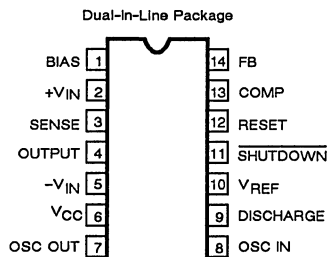
The Si9110/9111 are D/CMOS integrated circuits designed for use as high-performance switchmode controllers. A high-voltage DMOS input allows the controller to work over a wide range of input voltages (10- to 120-VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce internal power consumption to less than 10 mW.

The on-chip oscillator frequency is set by an external resistor, and can be easily synchronized to an external system clock. SHUTDOWN and RESET inputs allow external logic control, and these inputs can also be used to provide a variable shutdown

time for fault protection. A push-pull output driver provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. When combined with an output MOSFET and transformer, the Si9110 or Si9111 can be used to implement most single-ended power converter topologies (i.e., flyback and forward).

The Si9110 and Si9111 are available in 14-pin plastic, SO-IC and CerDIP packages, and are specified over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

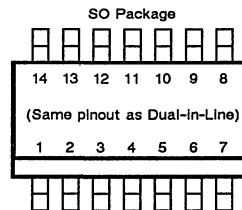
### PIN CONFIGURATION



Top View

Order Numbers:

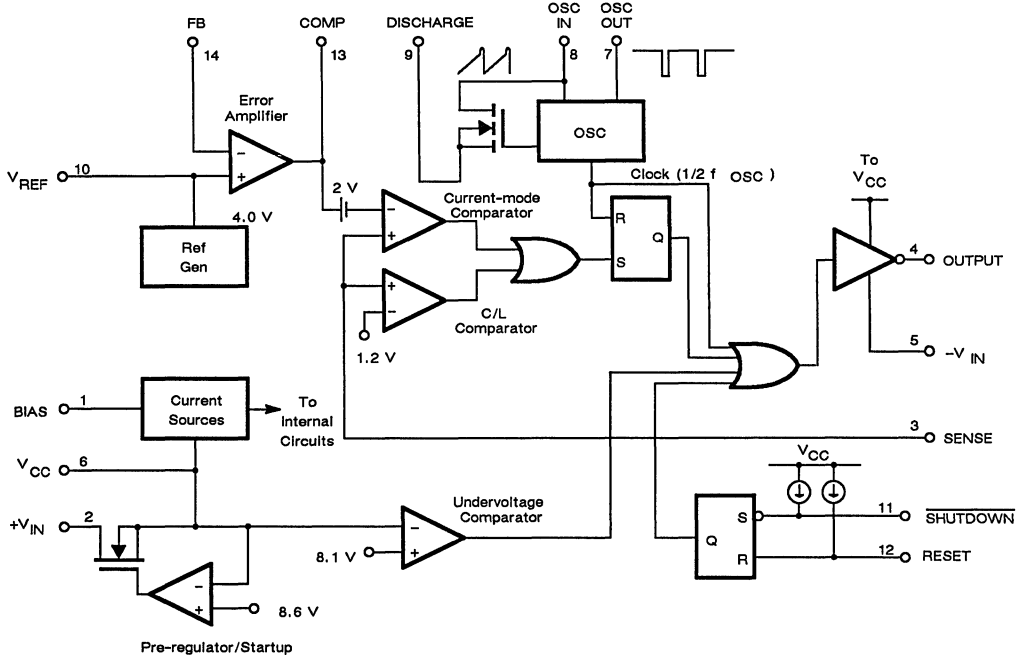
CerDIP: Si9110AK, Si9111AK  
Plastic: Si9110DJ, Si9111DJ



Top View

Order Numbers:  
Si9110DY, Si9111DY

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to  $-V_{IN}$

$V_{CC}$ .....	15.0 V
$+V_{IN}$ .....	120 V

Logic Inputs (RESET, SHUTDOWN, OSC IN) .....

Linear Inputs (FEEDBACK, SENSE) .....

HV Preregulator Input Current (continuous) .....

Storage Temperature (A, D Suffix) .....

Operating Temperature (A Suffix) .....

Junction Temperature ( $T_J$ ) .....

Power Dissipation (Package)*	
14-Pin Ceramic DIP (K Suffix)**	1000 mW
14-Pin Plastic DIP (J Suffix)***	750 mW
14-Pin SO-IC (Y Suffix)****	800 mW

Thermal Impedance ( $\theta_{JA}$ )	
14-Pin Ceramic DIP .....	100°C/W
14-Pin Plastic DIP .....	167°C/W
14-Pin SO-IC .....	140°C/W

\* Device mounted with all leads soldered or welded to PC board.

\*\* Derate 10 mW/°C above 50°C

\*\*\* Derate 6 mW/°C above 25°C

\*\*\*\* Derate 7 mW/°C above 25°C

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 48\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS						UNIT	
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>REFERENCE</b>										
Output Voltage	$V_R$	$R_L = 10\text{ M}\Omega$ (See Detailed Description)	1	4.0					V	
Output Impedance	$Z_{OUT}$		1	30					k $\Omega$	
Short Circuit Current		$V_{REF} = -V_{IN}$	1	100					$\mu\text{A}$	
Temperature Stability			2,3	1					mV/°C	
<b>OSCILLATOR</b>										
Maximum Frequency	$f_{OSC}$	$R_{OSC} = 0$	1	3	1		1		MHz	
Initial Accuracy		See Note e	1	100	80	120	80	120	kHz	
Voltage Stability	$V_{OSC}$	$9.5\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	1	$\pm 3$					%	
Temperature Coefficient			2,3	500					ppm/°C	
<b>ERROR AMPLIFIER</b>										
Feedback Input Voltage	$V_{FB}$	FB Tied to COMP See Detailed Description Reference Section	Si9110	1	4.00	3.96	4.04	3.96	4.04	V
			Si9111	1	4.00	3.60	4.40	3.60	4.40	
Input BIAS Current		$V_{FB} = 4.0\text{ V}$	1	25		500		500	nA	
Open Loop Voltage Gain	$A_{VOL}$		1	80	60		60		dB	
Unity Gain Bandwidth			1	1					MHz	
Output Impedance	$Z_{OUT}$		1	50					k $\Omega$	
Output Current	$I_{OUT}$	Source $V_{FB} = 3.4\text{ V}$	1	2.0	1.4		1.4		mA	
		Sink $V_{FB} = 4.5\text{ V}$	1	0.15	.12		.12			
Power Supply Rejection	PSRR	$9.5\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	1	70					dB	

ELECTRICAL CHARACTERISTICS <sup>a</sup>									
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0$ V $V_{CC} = 10$ V, $+V_{IN} = 48$ V $R_{BIAS} = 390$ k $\Omega$ $R_{OSC} = 330$ k $\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX		D SUFFIX		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>CURRENT LIMIT</b>									
Threshold Voltage	$V_{SOURCE}$	$V_{FB} = 0$ V	1	1.2	1.0	1.4	1.0	1.4	V
Delay to Output	$t_d$	$V_{SENSE} = 1.4$ V, See Figure 1	1	100		150		150	ns
<b>PREREGULATOR/STARTUP</b>									
Input Voltage	$+V_{IN}$	$I_{IN} = 10$ $\mu$ A	1			120		120	V
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq 9.4$ V	1			10		10	$\mu$ A
$V_{CC}$ Preregulator Turn-OFF Threshold Voltage		$I_{PREREGULATOR} = 10$ $\mu$ A	1	8.6		9.4		9.4	V
Undervoltage Lockout		$I_{OUTPUT} = 1$ mA (See Detailed Description)	1	8.1		8.9		8.9	
<b>SUPPLY</b>									
Supply Current	$I_{CC}$		1	0.6		1.0		1.0	mA
Bias Current	$I_{BIAS}$		1	15					$\mu$ A
<b>LOGIC</b>									
$\overline{\text{SHUTDOWN}}$ Delay	$t_{SD}$	$C_L = 500$ pF $V_{SENSE} = -V_{IN}$ See Figure 2	1	50		100		100	ns
$\overline{\text{SHUTDOWN}}$ Pulse Width	$t_{SW}$	See Figure 3	1		50		50		
RESET Pulse Width	$t_{RW}$		1		50		50		
Latching Pulse Width SHUTDOWN and RESET LOW	$t_{LW}$		1		25		25		
Input LOW Voltage	$V_{IL}$		1			2.0		2.0	V
Input HIGH Voltage	$V_{IH}$		1		8.0		8.0		
Input Current Input Voltage HIGH	$I_{IH}$	$V_{IN} = 10$ V	1	1		5		5	$\mu$ A
Input Current Input Voltage LOW	$I_{IL}$	$V_{IN} = 0$ V	1	-25		-35		-35	

## ELECTRICAL CHARACTERISTICS <sup>a</sup>

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0$ V $V_{CC} = 10$ V, $+V_{IN} = 48$ V $R_{BIAS} = 390$ k $\Omega$ $R_{OSC} = 330$ k $\Omega$	LIMITS						UNIT
			1=25°C		A SUFFIX -55 to 125°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>OUTPUT</b>									
Output HIGH Voltage	$V_{OH}$	$I_{OUT} = 1$ mA	1 2,3		9.90 9.75		9.90 9.75		V
Output LOW Voltage	$V_{OL}$	$I_{OUT} = -1$ mA	1 2,3		0.10 0.25		0.10 0.25		
Output Resistance	$R_{OUT}$		1 2,3	20 25		30 50		30 35	$\Omega$
Rise Time	$t_r$	$C_L = 500$ pF	1	40		75		75	ns
Fall Time	$t_f$		1	40		75		75	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e.  $C_{STRAY}$  Pin 8 = 0 pF.

## TIMING WAVEFORMS

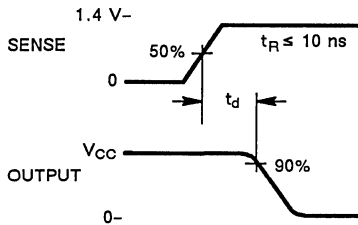


Figure 1

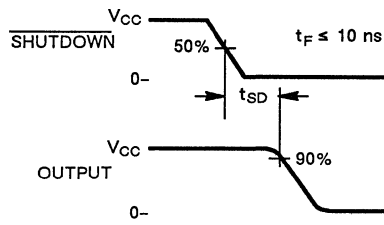


Figure 2

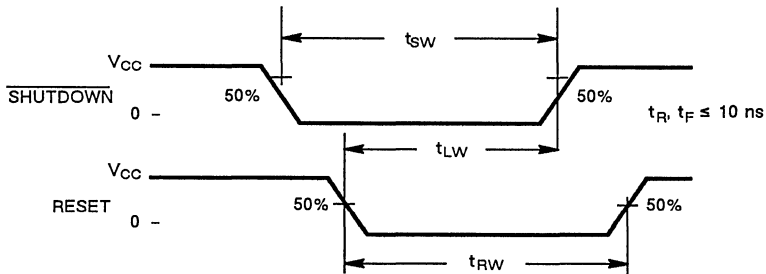
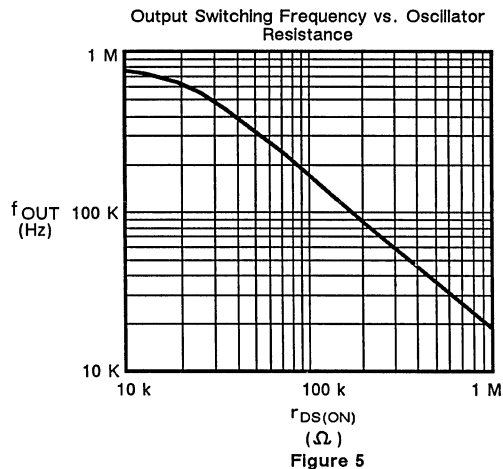
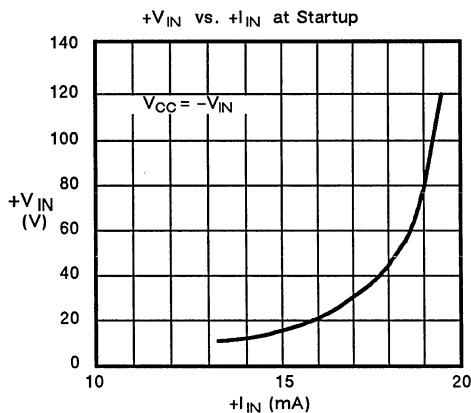


Figure 3

## TYPICAL CHARACTERISTICS



## DETAILED DESCRIPTION

## PREREGULATOR/STARTUP SECTION

Due to the low quiescent current requirement of the Si9110/Si9111 control circuitry, bias power can be supplied from the unregulated input power source, from an external regulated low-voltage supply, or from an auxiliary “bootstrap” winding on the output inductor or transformer.

When power is first applied during startup, +V<sub>IN</sub> (pin 2) will draw a constant current. The magnitude of this current is determined by a high-voltage depletion MOSFET device which is connected between +V<sub>IN</sub> and V<sub>CC</sub> (pin 6). This startup circuitry provides initial power to the IC by charging an external bypass capacitance connected to the V<sub>CC</sub> pin. The constant current is disabled when V<sub>CC</sub> exceeds 8.6 V. If V<sub>CC</sub> is not forced to exceed the 8.6 V threshold, then V<sub>CC</sub> will be regulated to a nominal value of 8.6 V by the preregulator circuit.

As the supply voltage rises toward the normal operating conditions, an internal undervoltage (UV) lockout circuit keeps the output MOSFET disabled until V<sub>CC</sub> exceeds the undervoltage lockout threshold (typically 8.1 V). This guarantees that the control logic will be functioning properly and that sufficient gate drive voltage is available before the

MOSFET turns ON. The design of the IC is such that the undervoltage lockout threshold will not exceed the preregulator turn-off voltage. Power dissipation can be minimized by providing an external power source to V<sub>CC</sub> such that the constant current source is always disabled.

**NOTE:** During startup or when V<sub>CC</sub> drops below 8.6 V the startup circuit is capable of sourcing up to 20 mA. This may lead to a high level of power dissipation in the IC (for a 48 V input, approximately 1 W). Excessive start up time can result in device damage. See Figure 4 for calculation of power dissipation during start up.

## BIAS

To properly set the bias for the Si9110/Si9111, a 390 kΩ resistor should be tied from BIAS (pin 1) to -V<sub>IN</sub> (pin 5). This determines the magnitude of bias current in all of the analog sections and the pull-up current for the SHUTDOWN and RESET pins. The current flowing in the bias resistor is nominally 15 μA.

## REFERENCE SECTION

The reference section of the Si9110 consists of a temperature compensated buried zener and trimmable divider network. The output of the



**DETAILED DESCRIPTION (Cont'd)**

reference section is connected internally to the non-inverting input of the error amplifier. Nominal reference output voltage is 4.0 V. The trimming procedure that is used on the Si9110 brings the output of the error amplifier (which is configured for unity gain during trimming) to within  $\pm 1\%$  of 4.0 V. this automatically compensates for input offset voltage in the error amplifier.

The output impedance of the reference section has been purposely made high so that a low impedance external voltage source can be used to override the internal voltage source, if desired, without otherwise altering the performance of the device.

Applications which use a separate external reference, such as non-isolated converter topologies and circuits employing optical coupling in the feedback loop, do not require a trimmed voltage reference with 1% accuracy. The Si9101 accommodates the requirements of these applications at a lower cost, by leaving the reference voltage untrimmed. The 10% accurate reference thus provided is sufficient to establish a DC bias point for the error amplifier.

**ERROR AMPLIFIER**

Closed-loop regulation is provided by the error amplifier, which is intended for use with "around-the-amplifier" compensation. A MOS differential input stage provides for low input current. The noninverting input to the error amplifier ( $V_{REF}$ ) is internally connected to the output of the reference supply and should be bypassed with a small capacitor to ground.

**OSCILLATOR SECTION**

The oscillator consists of a ring of CMOS inverters, capacitors, and a capacitor discharge switch. Frequency is set by an external resistor between the OSC IN and OSC OUT pins. (See Figure 5 for details of resistor value vs. frequency.) The DISCHARGE pin should be tied to  $-V_{IN}$  for normal internal oscillator operation. A frequency divider in the logic section limits switch duty cycle to  $\leq 50\%$  by locking the switching frequency to one half of the oscillator frequency.

Remote synchronization pulse into the OSC IN (pin 8) terminal. For a 5 V pulse amplitude, typical



values would be 1000 pF in series with 10 k $\Omega$  to pin 8.

**SHUTDOWN AND RESET**

SHUTDOWN (pin 11) and RESET (pin 12) are intended for overriding the output MOSFET switch via external control logic. The two inputs are fed through a latch preceding the output switch. Depending on the logic state of RESET, SHUTDOWN can be either a latched or unlatched input. The output is OFF whenever SHUTDOWN is low. By simultaneously having SHUTDOWN and RESET low, the latch is set and SHUTDOWN has no effect until RESET goes high. The truth table for these inputs is given in Table 1.

Both pins have internal current source pull-ups and can be left disconnected when not in use. An added feature of the current sources is the ability to connect a capacitor and an open-collector driver to the SHUTDOWN or RESET pins to provide variable shutdown time.

Table 1. Truth Table for the SHUTDOWN and RESET Pins.

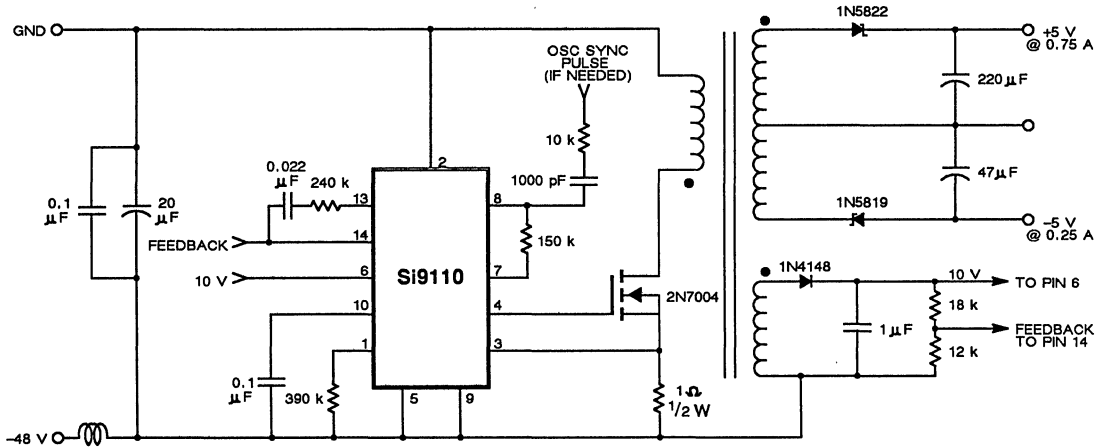
SHUTDOWN	RESET	OUTPUT
H	H	Normal Operation
H		Normal Operation (No Change)
L	H	OFF (Not Latched)
L	L	OFF (Latched)
	L	OFF (Latched) (No Change)

**OUTPUT SWITCH**

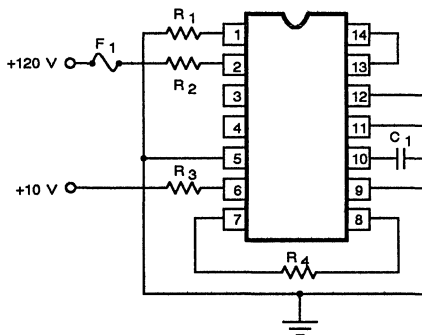
The push-pull driver output has a typical ON resistance of 20  $\Omega$ . Maximum switching times are specified at 75 ns for a 500 pF load. This is sufficient to directly drive MOSFETs such as the 2N7004, 2N7005, IRFD120 and IRFD220. Larger devices can be driven, but switching times will be longer, resulting in higher switching losses. In order to drive large MOSPOWER devices, it is necessary to use an external driver IC, such as the Siliconix D469. the D469 can switch very large devices such as the SMM20N50 (500 V, 0.3  $\Omega$ ) in approximately 100 ns.

## APPLICATIONS

### 5-WATT POWER SUPPLY FOR TELECOM APPLICATIONS



## BURN-IN CIRCUIT



- NOTES:
- R<sub>1</sub> = 390 kΩ, 1/4 W
  - R<sub>2</sub> = 1 kΩ, 2 W
  - R<sub>3</sub> = 1 kΩ, 2 W
  - R<sub>4</sub> = 100 Ω, 1/4 W
  - R<sub>5</sub> = 330 kΩ, 1/4 W
  - C<sub>1</sub> = 0.1 μF, 50 V

# Si9115/9116

## Off-Line Switchmode Controllers

### FEATURES

- 10 to 300 V Input Range
- Current-Mode Control
- High-Speed, Source-Sink Output Drive
- SHUTDOWN and RESET Functions
- High Efficiency Operation (> 80%)
- Internal Start-Up-Circuit
- Internal Oscillator (Up to 1 MHz)

### APPLICATIONS

- Off-Line Switchmode Power Supplies
- Housekeeping Power Supplies
- Distributed Power Systems

### DESCRIPTION

The Si9115 and Si9116 are D/CMOS integrated circuits designed for use as high-performance switchmode controllers. High-voltage DMOS inputs allow the controllers to work over a wide range of input voltages (10 to 300 VDC). Current-mode PWM control circuitry is implemented in CMOS to reduce quiescent current to less than 1 mA.

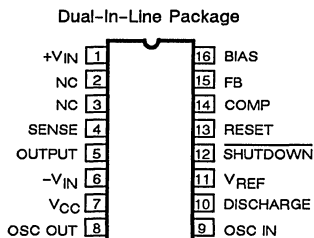
The on-chip oscillator frequency is set by an external resistor, and can easily be synchronized to an external system clock. SHUTDOWN and RESET inputs allow external logic control, and these inputs can also be used to provide a variable shutdown time for fault protection. A push-pull output driver

provides high-speed switching for MOSPOWER devices large enough to supply 50 W of output power. These devices, when combined with an output MOSFET and transformer, can be used to implement most single-ended power converter topologies (i.e., flyback and forward).

The Si9116 provides an inverted polarity output to facilitate interfacing to a high current MOSFET driver stage.

The Si9115 and Si9116 are available in 16-pin plastic DIP and SOIC packages, and are specified over the industrial, D suffix (-40 to 85°C) temperature range.

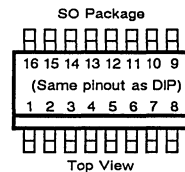
### PIN CONFIGURATION



Top View

Order Numbers:

Plastic: Si9115DJ, Si9116DJ

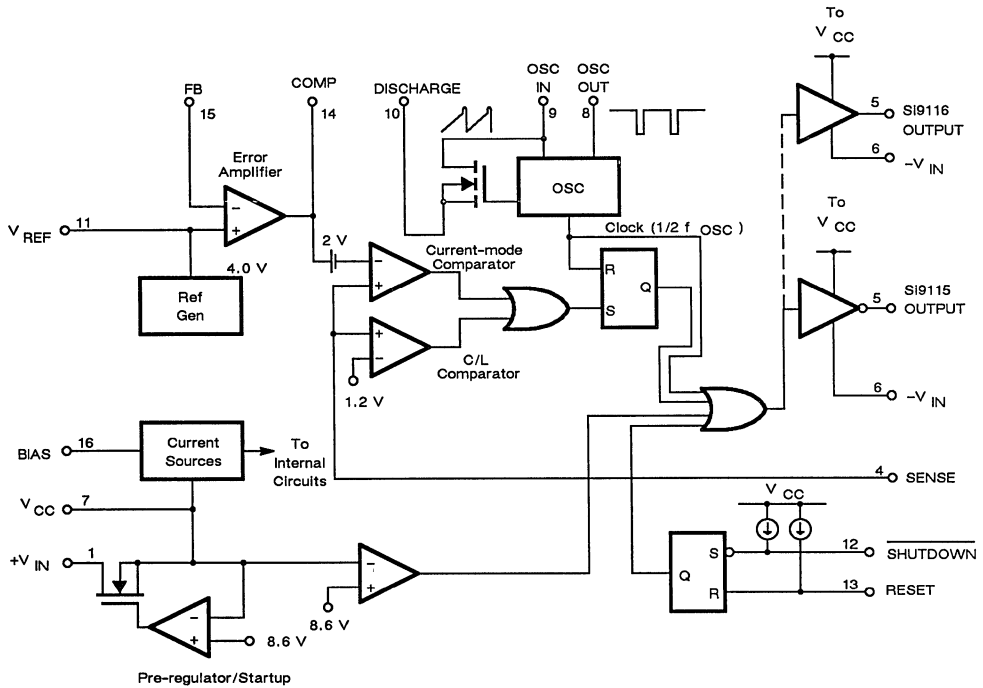


Top View

Order Numbers:

Si9115DY, Si9116DY

## FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Voltages Reference to  $-V_{IN}$

$V_{CC}$  ..... 15 V

$+V_{IN}$  ..... 300 V

Logic Inputs .....  $-0.3$  V to  $V_{CC} + 0.3$  V  
(RESET, SHUTDOWN, OSC IN)

Linear Inputs .....  $-0.3$  V to 7 V  
(FEEDBACK)

HV Preregulator Input Current (Continuous) ..... 2 mA

Continuous Output Current (Source or Sink) ..... 125 mA

Storage Temperature .....  $-65$  to  $125^\circ\text{C}$

Operating Temperature .....  $-40$  to  $85^\circ\text{C}$

Junction Temperature ( $T_J$ ) .....  $150^\circ\text{C}$

Power Dissipation (Package)\*

16-Pin Plastic DIP\*\* (J Suffix) ..... 750 mW

16-Pin SO\*\*\* (Y Suffix) ..... 800 mW

Thermal Impedance ( $\theta_{JA}$ )

16-Pin Plastic DIP .....  $167^\circ\text{C/W}$

16-Pin SO .....  $156^\circ\text{C/W}$

\* Device mounted with all leads soldered or welded to PC Board.

\*\* Derate  $6 \text{ mW}/^\circ\text{C}$  above  $25^\circ\text{C}$ .

\*\*\* Derate  $6.5 \text{ mW}/^\circ\text{C}$  above  $25^\circ\text{C}$ .

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 160\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS				UNIT
			1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>REFERENCE</b>							
Output Voltage	$V_R$	$R_L = 10\text{ M}\Omega$ (See Detailed Description)	1	4.0			V
Output Impedance	$Z_{OUT}$		1	30			k $\Omega$
Short Circuit Current		$V_{REF} = -V_{IN}$	1	100			$\mu\text{A}$
Temperature Stability			2,3	1			mW/°C
<b>OSCILLATOR</b>							
Maximum Frequency	$f_{OSC}$	$R_{OSC} = 0$	1	3	1		MHz
Initial Accuracy <sup>9</sup>			1	100	80	120	kHz
Voltage Stability	$V_{OSC}$	$9.5\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	1	$\pm 3$			%
Temperature Coefficient			2,3	500			ppm/°C
<b>ERROR AMPLIFIER</b>							
Feedback Input Voltage	$V_{FB}$	FB Tied to COMP (See Detailed Description)	1		3.96	4.04	V
Input BIAS Current		$V_{FB} = 4.0\text{ V}$	1	25		500	nA
Open Loop Voltage Gain	$A_{VOL}$		1	80	60		dB
Unity Gain Bandwidth			1	1			MHz
Output Impedance	$Z_{OUT}$		1	50			k $\Omega$
Output Current	$I_{OUT}$	Source $V_{FB} = 3.4\text{ V}$ $V_{COMP} = 5\text{ V}$	1	2.0	1.4		mA
		Sink $V_{FB} = 4.5\text{ V}$ $V_{COMP} = 0.5\text{ V}$	1	0.15	0.12		
Power Supply Rejection	PSRR	$9.5\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	1	70			dB

ELECTRICAL CHARACTERISTICS <sup>a</sup>								
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = $-V_{IN} = 0\text{ V}$ $V_{CC} = 10\text{ V}$ , $+V_{IN} = 160\text{ V}$ $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	LIMITS				UNIT	
			1=25 °C 2=85 °C 3=-40 °C		D SUFFIX -40 to 85°C			
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>		
<b>CURRENT LIMIT</b>								
Threshold Voltage	$V_{SENSE}$	$V_{FB} = 0\text{ V}$	1	1.2	1.0	1.4	V	
Delay to Output	$t_d$	$V_{SENSE} = 1.4\text{ V}$ See Figure 1	1	100		150	ns	
<b>PREREGULATOR/STARTUP</b>								
Input Voltage	$+V_{IN}$	$I_{IN} = 10\text{ }\mu\text{A}$	1		300		V	
Input Leakage Current	$+I_{IN}$	$V_{CC} \geq 9.4\text{ V}$	1			10	$\mu\text{A}$	
$V_{CC}$ Preregulator Turn-OFF Threshold Voltage		$I_{Preregulator} = 10\text{ }\mu\text{A}$	1	8.6		9.4	V	
Undervoltage Lockout		$R_L = 100\text{ }\Omega$ from DRAIN to $V_{CC}$ (See Detailed Description)	1	8.1		8.9		
<b>SUPPLY</b>								
Supply Current	$I_{CC}$	$C_L = 500\text{ pF}$ at Pin 4	1	0.75	1.2	1.2	mA	
Bias Current	$I_{BIAS}$		1	15			$\mu\text{A}$	
<b>LOGIC</b>								
SHUTDOWN Delay	$t_{SD}$	$C_L = 500\text{ pF}$ , $V_{SENSE} = -V_{IN}$ See Figure 2	1	50		100	ns	
SHUTDOWN Pulse Width	$t_{SW}$		See Figure 3	1		50		
RESET Pulse Width	$t_{RW}$	1			50			
Latching Pulse Width SHUTDOWN and RESET LOW	$t_{LW}$	1			25			
Input LOW Voltage	$V_{IL}$		1			2.0	V	
Input HIGH Voltage	$V_{IH}$		1		8.0			
Input Current Input Voltage HIGH	$I_{IH}$	$V_{IN} = 10\text{ V}$	1	1		5	$\mu\text{A}$	

ELECTRICAL CHARACTERISTICS <sup>a</sup>							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: DISCHARGE = -V <sub>IN</sub> = 0 V V <sub>CC</sub> = 10 V, +V <sub>IN</sub> = 160 V R <sub>BIAS</sub> = 390 kΩ R <sub>OSC</sub> = 330 kΩ	LIMITS				UNIT
			1=25°C 2=85°C 3=-40°C		D SUFFIX -40 to 85°C		
			TEMP	TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>OUTPUT</b>							
Output HIGH Voltage	V <sub>OH</sub>	I <sub>OUT</sub> = 1 mA	1 2,3		9.90 9.75		V
Output LOW Voltage	V <sub>OL</sub>	I <sub>OUT</sub> = -1 mA	1 2,3			0.10 0.25	
Output Resistance	R <sub>OUT</sub>		1 2,3	20 25			Ω
Rise Time	T <sub>R</sub>	C <sub>L</sub> = 500 pF	1	40		75	ns
Fall Time	T <sub>F</sub>		1	40		75	

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- e. C<sub>STRAY</sub> ≤ 2 pF on pin 8.

**TIMING WAVEFORMS**

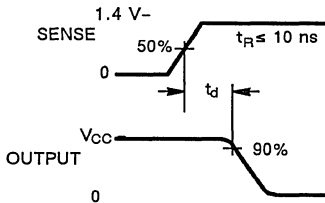


Figure 1.

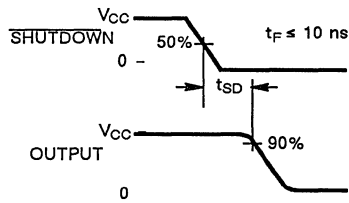


Figure 2.

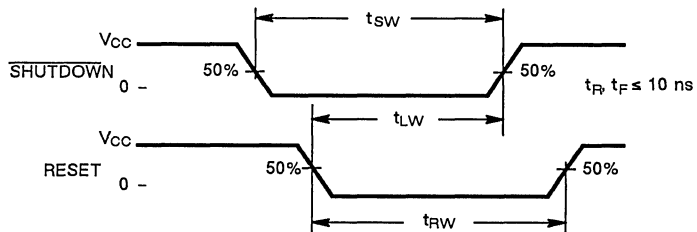


Figure 3.









# ASIC

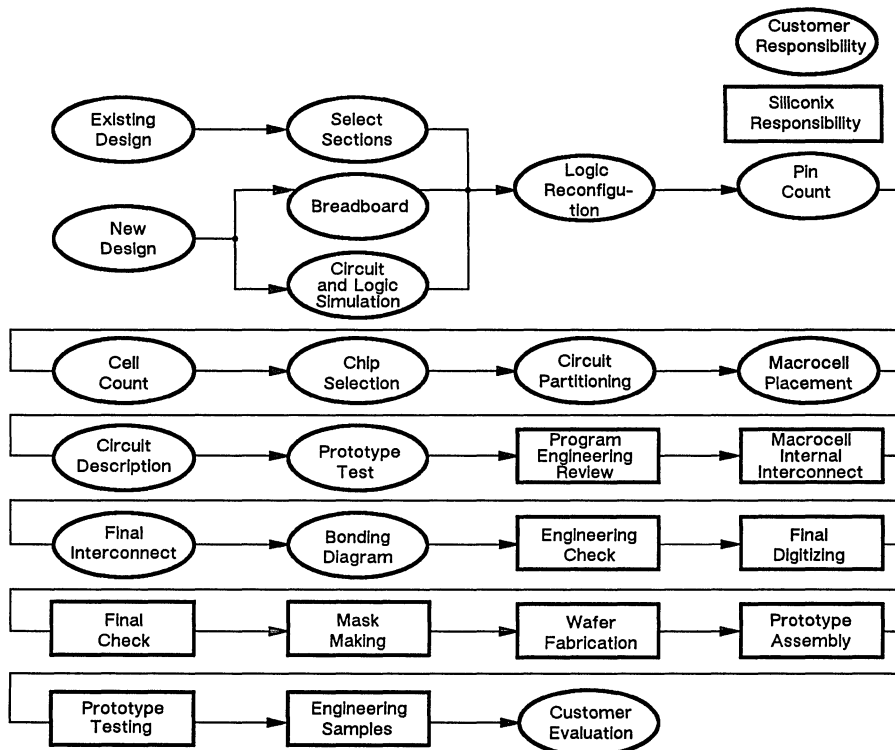
## INTRODUCTION

Siliconix offers a family of seven different arrays ranging in size from 350 to 1500 gates in silicon gate HCMOS which combine analog technology with fast, high-density array logic. Unlike strictly digital gate arrays, the Siliconix ISO5 arrays have the flexibility to implement both analog and digital functions, thus providing a unique linear/digital integrated solution.

Our family has on-chip processing of analog functions such as comparators, operational amplifiers and analog switches. In addition, it has the ability to operate from 2.4 to 12.0 volts and has on-chip level translation for interfacing TTL to CMOS logic levels and 12 V MOSFET gate enhancement. The HCMOS technology offers high noise margins, low power consumption and high switching speeds, with an average gate delay of 4.0 ns through a two-input NAND gate.

All Siliconix arrays are supported on approved CAD workstations, and are accompanied with extensive macro libraries. Our arrays carry the same quality and reliability as any Siliconix product, with class B or Mil Standard 883 compliant processing available.

Siliconix is committed to providing solutions for linear/digital applications. Our research into new technologies that will allow higher levels of integration for combining analog and digital functions is on-going. The next generation of mixed-mode gate arrays will include architectures that will enable improved-performance analog processing in addition to high density, high speed digital capabilities.



Flow Diagram - ISO5 Gate Arrays Design Approach

## **Full custom conversion**

If production quantities rise significantly above your initial expectations, it may become necessary to convert your gate array to a full custom design. This will enable you to obtain the lowest possible cost per unit at a minimum risk since the gate array will serve as a sort of integrated breadboard.

## **Production**

Once you have completed evaluation of your prototypes and are satisfied that they meet all your specifications, we then enter the production phase. During this phase, we fine tune the test program to assure that all necessary parametric testing is being performed. The leadtime for production shipments is typically 10 weeks from receipt of purchase order.

## **Getting Started**

The first step to beginning your Siliconix CMOS gate array design is to order your design manual. Once you have received your design manual, you are ready to begin your design. The manual allows you to use several different approaches, depending upon whether you are initiating a new design or integrating an existing design. Prototypes are typically delivered 8 to 10 weeks from the time we receive your final integration package and purchase order.

## FEATURES

- Operating Voltage From 2.4 to 12.5 V
- On Chip Level Translation For High Voltage Systems
- On Chip Processing Of Analog Functions, Such As Comparators, Operational Amplifiers, Analog Switches And Timers
- On Chip Low Power Quartz And RC Oscillators (Quartz Oscillator Is External)
- Average Gate Delay 4.0 ns Through Two Input NAND Gate And Interconnection (Fanout = 2,  $V_{DD} = 5\text{ V}$ )
- Completely Supported Military Processing Through MIL 38510 Qual Packaging
- Single Output Drive Up To 10 mA, Can be Paralleled Outputs For Higher Drive
- Fully Supported By Approved CAD Systems
- Extensive Macro Library.
- All I/O Cells Configurable As Inputs, Outputs Or Bidirectional
- TTL/CMOS I/O Compatibility
- Complete Packaging Capability (Plastic, CerDIP, Ceramic)

## DESCRIPTION

The ISO5 family of gate arrays from Siliconix provides high performance, with speeds matching high speed bipolar technologies such as LSTTL. At the same time, this family offers high noise margin, ease of design and the low power consumption of CMOS technology. The ISO5 series is implemented in 5 micron technology with single-layer metalization. A wide range of arrays is offered from 180 gates to 2400. Pad counts range from 40 to 100.

A unique feature of this array family, enhanced by

its 12.5 V operating capability, is the ability to implement analog functions and hence realize single-chip, mixed-mode solutions. In addition to the advantages of higher density and performance, the integration is realized using a gate array technique which translates into into low-cost, quick-turn solutions. The results are higher reliability, much lower power consumption, a more efficient system solution, lower product and manufacturing costs and product brought to the market in a timely manner.

## ARRAY STRUCTURE

The ISO5 series of arrays is a high performance family of 9 arrays manufactured using a 5 micron CMOS technology. The average propagation delay through a two input NAND gate (Fanout = 2) is approximately 4.0 ns. This family uses a single layer of metal and programmable contacts to personalize arrays for customer applications. Figure 1 shows the organization of the basic array.

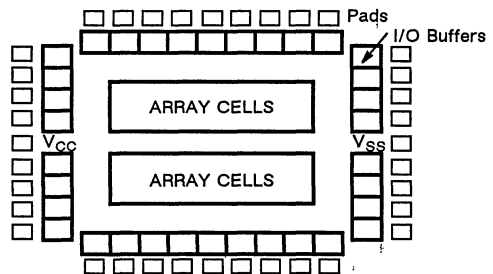


Figure 1. ISO5 Basic Array Organization

## ISO5 GATE ARRAY SIZES

Description	I	A	B	C	D	E	F	G	H
2-Input NAND Gate	180	360	540	720	960	1200	1500	1800	2400
Maximum I/O	30	36	48	54	62	68	76	82	90
Number of Pads	40	46	58	64	72	78	86	92	100

## PACKAGE TYPES

TYPE	NUMBER OF PINS
Plastic Dual in Line (PDIP) .....	14, 16, 18, 24, 28, 40, 48
Ceramic Dual in Line (CDIP) .....	14, 16, 18, 24, 28, 40
Ceramic Leadless Chip Carriers (LCC) .....	24, 28, 40, 44, 48, 68
Ceramic Leaded Chip Carriers (Flatpack) .....	24, 28, 40, 44, 68, 84
Plastic J Lead Chip Carriers (PLCC) .....	28, 44, 68, 84
Ceramic J Lead Chip Carriers .....	44
Ceramic Pin Grid Arrays (PGA) .....	68, 84, 100, 120, 144

\* Contact factory for package details and alternate package data.

## ABSOLUTE MAXIMUM RATINGS

$V_{SS} = 0\text{ V}$	Output Voltage, $V_{OUT}$ .....	-0.3 to $V_{DD} + 0.3\text{ V}$
$T_A = 25^\circ\text{C}$	Storage Temperature, $T_{STG}$ .....	-65 to $150^\circ\text{C}$
Supply Voltage, $V_{DD}$ .....	Recommended Operating Conditions:	
Input Voltage, $V_{IN}$ .....	Supply Voltage, $V_{DD}$ .....	2.4 to $12.5\text{ V}$
	Operating Temperature, $T_{OPR}$ .....	-55 to $125^\circ\text{C}$

## ELECTRICAL CHARACTERISTICS<sup>a</sup> $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  $V_{DD} = 5.0\text{ V}$	LIMITS			UNIT
			TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DIGITAL INPUTS</b>						
Input HIGH Voltage	$V_{IH}$	CMOS Interface		3.5		V
		TTL Interface		2.0		
Input LOW Voltage	$V_{IL}$	CMOS Interface			1.5	
		TTL Interface			0.4	

ELECTRICAL CHARACTERISTICS <sup>a</sup> T <sub>A</sub> = 25 °C						
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>DD</sub> = 5.0 V	LIMITS			UNIT
			TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DIGITAL INPUTS (Cont'd)</b>						
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = 0 or V <sub>DD</sub>	0.1		10	μA
Input Capacitance	C <sub>IN</sub>	All Digital Inputs	7			pF
<b>DIGITAL OUTPUTS</b>						
HIGH Level Output Voltage	V <sub>OH</sub>	I <sub>O</sub>   < 1 μA		4.95		V
LOW Level Output Voltage	V <sub>OL</sub>				0.05	
Output LOW Current (Sink Current)	I <sub>OL</sub>	V <sub>O(max)</sub> = 0.4 V	10	6		mA
		V <sub>O(max)</sub> = 2.5 V	40			
Output HIGH Current (Source Current)	I <sub>OH</sub>	V <sub>O(min)</sub> = 2.5 V	-15		-12	
		V <sub>O(min)</sub> = 3.5 V	-12			
Three-State Output Leakage Current	I <sub>OZ</sub>	V <sub>O</sub> = 0 or V <sub>DD</sub>	0.1		10	μA
<b>SUPPLY</b>						
Quiescent Current	I <sub>DD</sub>	All Inputs = 0 or V <sub>DD</sub> No Analog Functions	0.1		10	μA
Supply Voltage <sup>c</sup>	V <sub>DD</sub>	V <sub>DD</sub> = 5.0 V for Conformance to Data Sheet		2.4	12.5	V
<b>DYNAMIC</b>						
Internal Gate Delay	t <sub>pd</sub>	2 - Input NAND Fanout = 2	HIGH to LOW	4.5		ns
			LOW to HIGH	3.5		
TTL Input Delay		IP2 Fanout = 4	HIGH to LOW	10		
			LOW to HIGH	4		
CMOS Input Delay		IBI01 Fanout = 4	HIGH to LOW	3		
			LOW to HIGH	3.5		

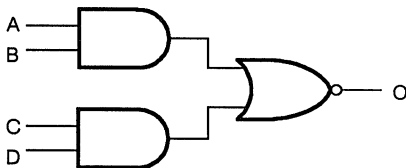
ELECTRICAL CHARACTERISTICS <sup>a</sup> T <sub>A</sub> = 25 °C							
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified:  V <sub>DD</sub> = 5.0 V		LIMITS			UNIT
				TYP <sup>d</sup>	MIN <sup>b</sup>	MAX <sup>b</sup>	
<b>DYNAMIC (Cont'd)</b>							
Level Shifted TTL Input Delay	t <sub>pd</sub>	LSIUT1, V <sub>DD</sub> = 12 V Fanout = 4, V <sub>SS</sub> = 5 V	HIGH to LOW	15			ns
			LOW to HIGH	14			
Level Shifted CMOS Input Delay		LS1UC1, V <sub>DD</sub> = 12 V Fanout = 4, V <sub>SS</sub> = 5 V	HIGH to LOW	12			
			LOW to HIGH	10			
TTL Output Delay		OB, 50 pF Load	HIGH to LOW	18			
			LOW to HIGH	7.5			
CMOS Output Delay		OB1, 50 pF Load	HIGH to LOW	18.5			
			LOW to HIGH	20.5			
Power Dissipation per Gate	pd/f			< 3			μW/MHz

**NOTES:**

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Guaranteed by design, not subject to production test.
- d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

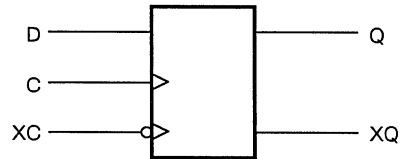
**ISO5 TYPICAL MACROS\***

2-Input AND/NOR Gate



t<sub>pdHL</sub> = 8 ns  
t<sub>pdLH</sub> = 2.8 ns

D-Flip Flop without Reset

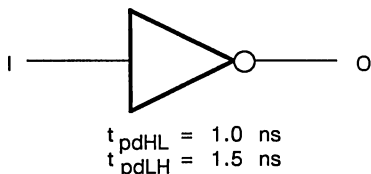


t<sub>pdHL</sub> = 6 ns  
t<sub>pdLH</sub> = 6.8 ns

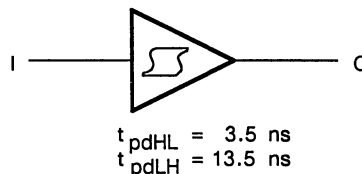


**ISO5 TYPICAL MACROS\* (Cont'd)**

Inverting Balanced Output Buffer



Schmitt Trigger with TTL Input



\* Fanout = 0

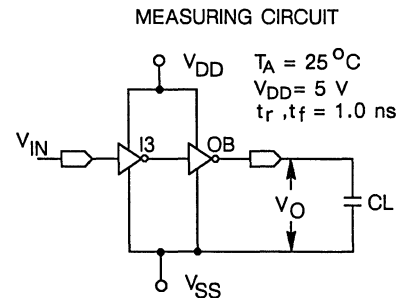
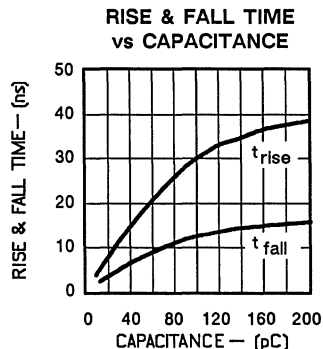
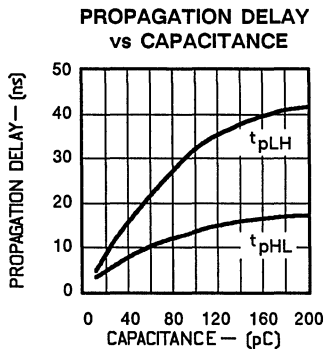
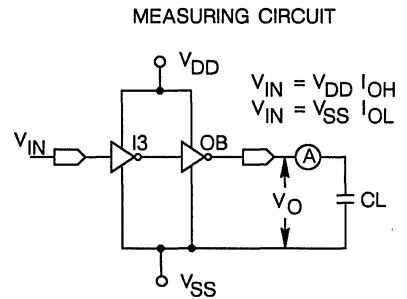
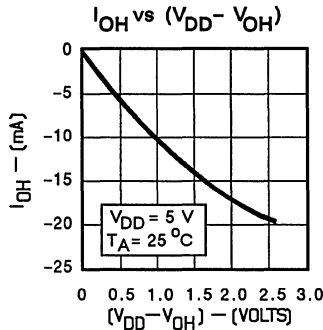
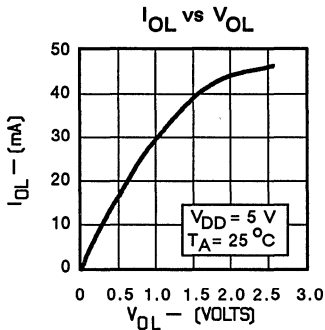
**ISO5 MACRO LIBRARY**

MACRO NAME	FUNCTION	# OF NA2 EQUIVALENTS	MACRO NAME	FUNCTION	# OF NA2 EQUIVALENTS
<b>GATES</b>			IN4	Four Inverters	2.0
NA2	2-Input NAND Gate	1.0	IN5	Five Inverters	2.5
NA3	3-Input NAND Gate	1.5	IN6	Six Inverters	3.0
NA4	4-Input NAND Gate	2.0	IN7	Seven Inverters	3.5
NA5	5-Input NAND Gate	2.5	IN8	Eight Inverters	4.0
NA6	6-Input NAND Gate	3.0	IN9	Nine Inverters	4.5
NO2	2-Input NOR Gate	1.0	ID1	Delay Inverter	1.5
NO3	3-Input NOR Gate	1.5	ID2	Delay Inverter	3.0
NO4	4-Input NOR Gate	2.0	<b>FLIP/FLOPS/LATCHES</b>		
XO	Exclusive OR	2.5	FF1	D Flip Flop (DFF)	6.0
XOS	Exclusive OR with SAB Structure	1.5	FF2	DFF with XRESET	6.0
XN	Exclusive NOR	2.5	FF3	DFF with RESET	6.0
XNS	Exclusive NOR with SAB Structure	1.5	FF4	DFF with XSET	6.0
<b>COMPLEX GATES</b>			FF5	DFF with SET	6.0
AN1	AND-NOR 2/1	1.5	FF6	DFF with XSET & XRESET	7.5
AN2	AND-NOR 2/2	2.0	FF7	DFF with SET & RESET	7.5
AN3	AND-NOR 2/1/1	2.0	FF9	DFF with XSET, XRESET1 & XRESET2	9.0
AN4	AND-NOR 3/2	2.5	FF10	DFF with XRESET1, XSET1 & XSET2	9.0
AN5	AND-NOR 3/3	3.0	T2	Toggle FF with XRESET	6.0
AN6	AND-NOR 2/2/2	3.0	L1	D-Latch	3.0
ON1	OR-NAND 2/1	1.5	L2	D-Latch with XRESET	3.0
ON2	OR-NAND 2/2	2.0	L3	D-Latch with SET	3.0
ON3	OR-NAND 2/1/1	2.0	<b>TRANSMISSION GATES</b>		
ON4	OR-NAND 3/2	2.5	TGC	Transmission Gate Core Cell	1.5
ON5	OR-NAND 3/3	3.0	TGIO	Transmission Gate I/O Cell	I/O
ON6	OR-NAND 2/2/2	3.0	<b>SINGLE TRANSISTOR DEVICES</b>		
<b>INVERTERS</b>			NCHC	N-Channel Transistor 55/5	1.0
IN1	Single Inverter	0.5	NCHIO	N-Channel Transistor 275/5	I/O
IN2	Double Inverter	1.0	PCHC	P-Channel Transistor 55/5	1.0
IN3	Triple Inverter	1.5	PCHIO	P-Channel Transistor 275/5	I/O

## ISO5 MACRO LIBRARY (Cont'd)

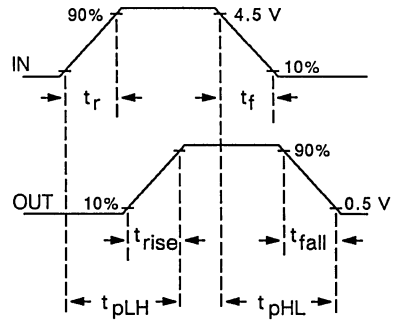
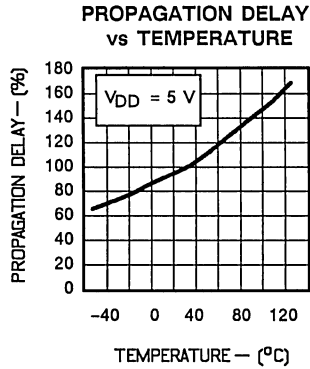
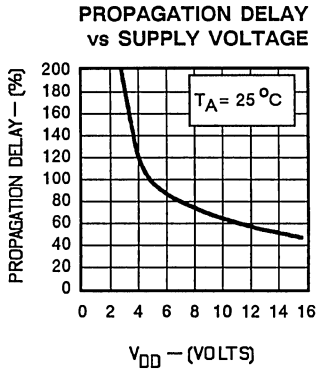
MACRO NAME	FUNCTION	# OF NA2 EQUIVALENTS	MACRO NAME	FUNCTION	# OF NA2 EQUIVALENTS
<b>INTERFACE/SCHMITT TRIGGERS</b>					
LSIUC1	Input Upward Level Shifter CMOS	6.0 + I/O	OB1	Inverting Balanced Output Buffer	I/O
LSIUT1	Input Upward Level Shifter TTL	15.0 + I/O	OB2	Tri-State Output Buffer	I/O
LSODC1	Output Downward Level Shifter	1 + I/O	OB3	Open Drain-N Output Buffer	I/O
ST1	Schmitt Trigger with TTL Input	3.0 + I/O	OB4	Open Drain-P Output Buffer	I/O
ST2	Schmitt Trigger w/CMOS Input	4.5 + I/O	TS1	Internal Inverting Tri-State w/Enable	1.5
ST3	Schmitt Trigger w/CMOS Input	3.0 + I/O	TS2	Internal Inverting Tri-State w/Enable Bar	1.5
ST4	Schmitt Trigger w/CMOS Input	5.0 + I/O	TS3	3-State Output Buffer Driver w/Enable	4.5
ST5	Schmitt Trgger w/CMOS Input	4.0 + I/O	TS4	3-State Output Buffer Driver w/Enable Bar	4.5
<b>I/O</b>					
IBC1	Balanced CMOS Input Inv Buffer Core	1.5 + I/O	<b>MULTIPLEXERS</b>		
IBIO1	Balanced CMOS Input Inv Buffer I/O	I/O	SAB	2 to 1 Multiplexer	1.5
IP1	Inverter with 6N/1P Ratio	1.5 + I/O	<b>OSCILLATORS</b>		
IP2	Input Buffer with 6N/1P Ratio	I/O	OSCQSP	Standard Power Quartz Oscillator	4.5
IP3	Input Buffer with 3N/1P Ratio	I/O	OSCQLP	Low Power Quartz Oscillator	6.0
IP4	Inverter with 3N/1P Ratio	1.5 + I/O	OSCRC	RC Oscillator	3.0
IP5	Inverter with 5N/1P Ratio	1.5 + I/O	OSCRCXE	RC Oscillator with XENABLE	4.5
IP	Input Protection	I/O	<b>ANALOG CELLS</b>		
IPB	Input Protection	I/O	AS1	Analog Switch	I/O
IPC	Input Protection (Corner Device)	I/O	COMP1	Comparator	15.0
IPCA	Input Protection (Corner Device)	I/O	OPAMP1	Operational Amplifier	15.0
IPCB	Input Protection (Corner Device)	I/O	DIFF1	Differential Amplifier	9.0
IOB1	Input/Output Buffer	I/O	<b>MEMORY CELLS</b>		
IOBA	Bldirectional I/O	I/O	RAM1	Random Access Memory	3.0
OB	Inverting Output Buffer	I/O			

## TYPICAL CHARACTERISTICS



**TYPICAL CHARACTERISTICS**

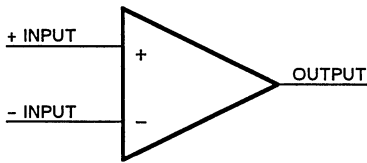
**TIMING DIAGRAM**



**ANALOG CIRCUITS**

**OPERATIONAL AMPLIFIER — (OPAMP1)**

**Functional Block Diagram:**



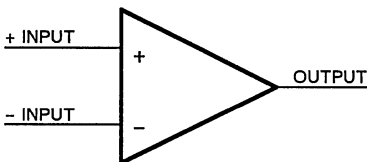
**Typical Electrical Characteristics:**

Test Conditions: V<sub>DD</sub> = 12 V, T<sub>A</sub> = 25 °C

Parameter	Value
Unity Gain Bandwidth	8 MHz
DC Offset	15 mV
DC Gain	>70 dB
Power Consumption (no signal, no load)	< 1200 μW
Typical Operating Frequency Range	0 to 1 MHz
Typical Supply Voltage Range	2.4 to 14 V
Maximum Output Current: Sink (I <sub>OL</sub> )	1 mA
Source (I <sub>OH</sub> )	1 mA
Slew Rate	35 V/μs

**DIFFERENTIAL AMPLIFIER — (DIFF1)**

**Functional Block Diagram:**



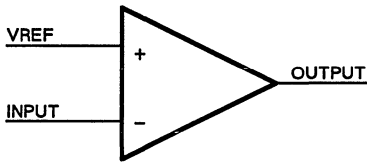
**Typical Electrical Characteristics:**

Test Conditions: V<sub>DD</sub> = 12 V, T<sub>A</sub> = 25 °C

Parameter	Value
Maximum operating frequency	8 MHz
DC Offset	15 mV
Power Consumption (no signal, no load)	< 1200 μW
Typical Supply Voltage Range	2.4 to 14 V
Slew Rate	35 V/μs

### COMPARATOR - (COMP1)

Functional Block Diagram:



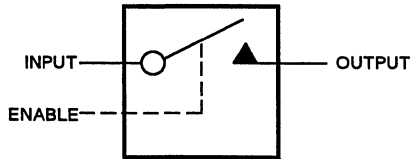
Typical Electrical Characteristics:

Test Conditions:  $V_{DD} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$

Parameter	Value
Maximum operating frequency	8 MHz
DC Offset	15 mV
Power Consumption (no signal, no load)	< 1200 $\mu\text{W}$
Typical Supply Voltage Range	2.4 to 14 V
Slew Rate	35 V/ $\mu\text{s}$

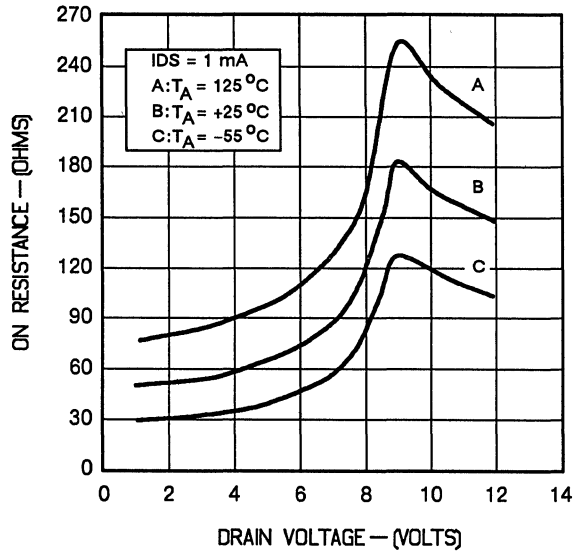
### ANALOG SWITCH - (AS1)

Functional Block Diagram:



Typical Performance Characteristics:

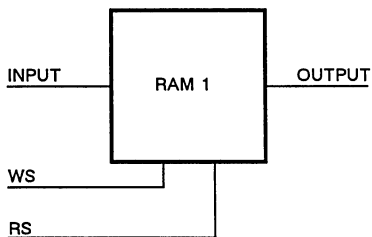
#### ON RESISTANCE vs DRAIN VOLTAGE



**MEMORY CELLS**

**MEMORY CELL – (RAM1)**

**Functional Block Diagram:**



**Typical Electrical Characteristics:**

Test Conditions:  $V_{DD} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$

Parameter	Value
Write Settling Time	20 ns
Read-out Time	20 ns

\* WS = Write Select      RS = Read Select

**TIMERS – PRECISION TIMER – (555)**

**Circuit Description:**

This precision timer is capable of producing accurate time delays or frequencies. It is ideal for applications that require excellent frequency stability and high supply voltage rejection. In addition, this timer can be used as a precision Schmitt trigger or threshold detection circuit.

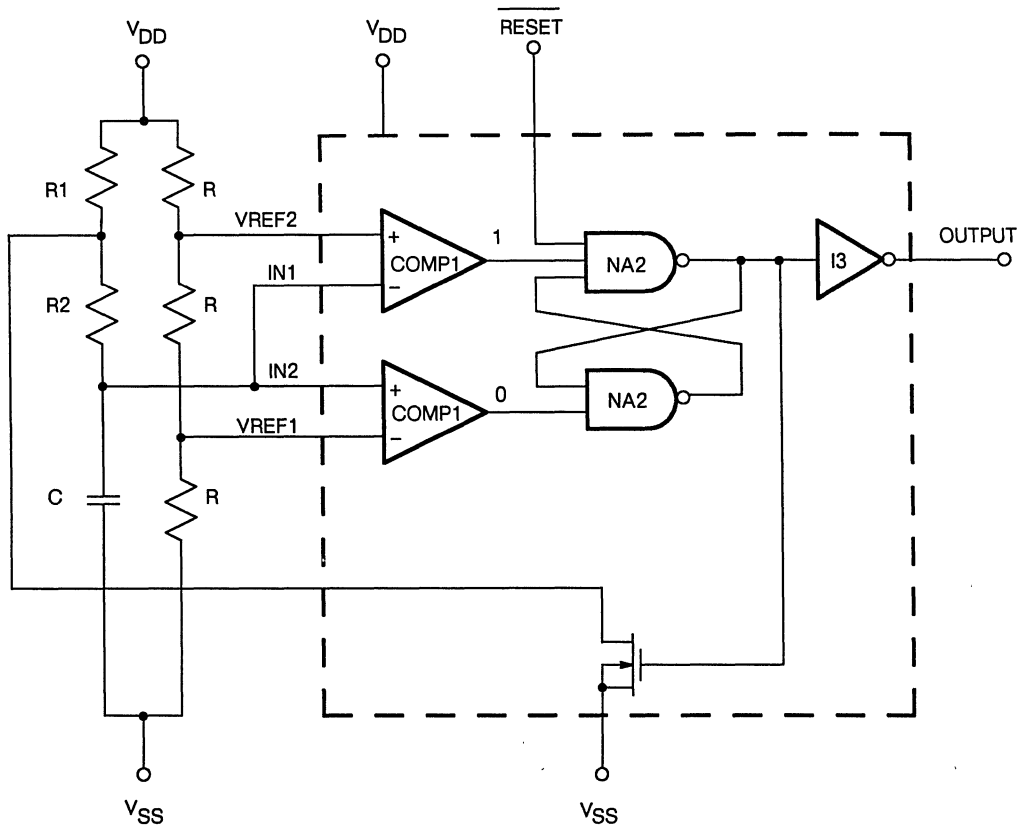
The threshold levels are set by three external resistors, R. To achieve minimum voltage dependency, the voltage supply of the resistor-ladder has been connected to the voltage supply of the timer. The reset pin, when enabled, discharges the capacitor and disables the charging process.

**Typical Electrical Characteristics:**

Test Conditions:  $V_{DD} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$

Parameter	Value
Typical Operating Frequency	0 to 4 MHz
Typical Supply Voltage Range	2.4 to 14 V
$\Delta f$ over Operating Range	$< \pm 5\%$
DC Current, $I_{DD}$ (IN1 and IN2 at $V_{SS}$ without load)	300 $\mu\text{A}$ to 900 $\mu\text{A}$
Operating Temperature Range	-55 to +125 $^\circ\text{C}$

### FUNCTIONAL BLOCK DIAGRAM



### EQUIVALENT GATE COUNT FOR APPROXIMATION OF ARRAY SIZE

DEVICE	CELLS	DESCRIPTION	DEVICE	CELLS	DESCRIPTION
4000	4	Dual 3-Input NOR Gate/Inv	4015	42	Dual 4-Bit Static Shift Register
4001	4	Quad 2-Input NOR Gate	4016	6	Dual Analog Switch/Quad Mult.
4002	3	Dual 4-Input NOR Gate	4017	34	Decade Johnson Counter/Divider
4006	100	18-Bit Static Shift Register	4018	40	Presetable Divide by N Counter
4007	1	Dual Pair + Inverter	4020	139	14-Bit Binary Counter
4008	51	4-Bit Full Adder (O.C.)	4021	80	8-Bit Static Shift Register
4011	4	Quad 2-Input NAND Gate	4022	30	Octal Counter/Divider
4012	3	Dual 4-Input NAND Gate	4023	3	Triple 3-Input NAND Gate
4013	18	Dual Type D FF Gate	4024	45	Seven Stage Ripple Counter
4014	53	8-Bit Static Shift Register	4025	3	Triple 3-Input NOR Gate

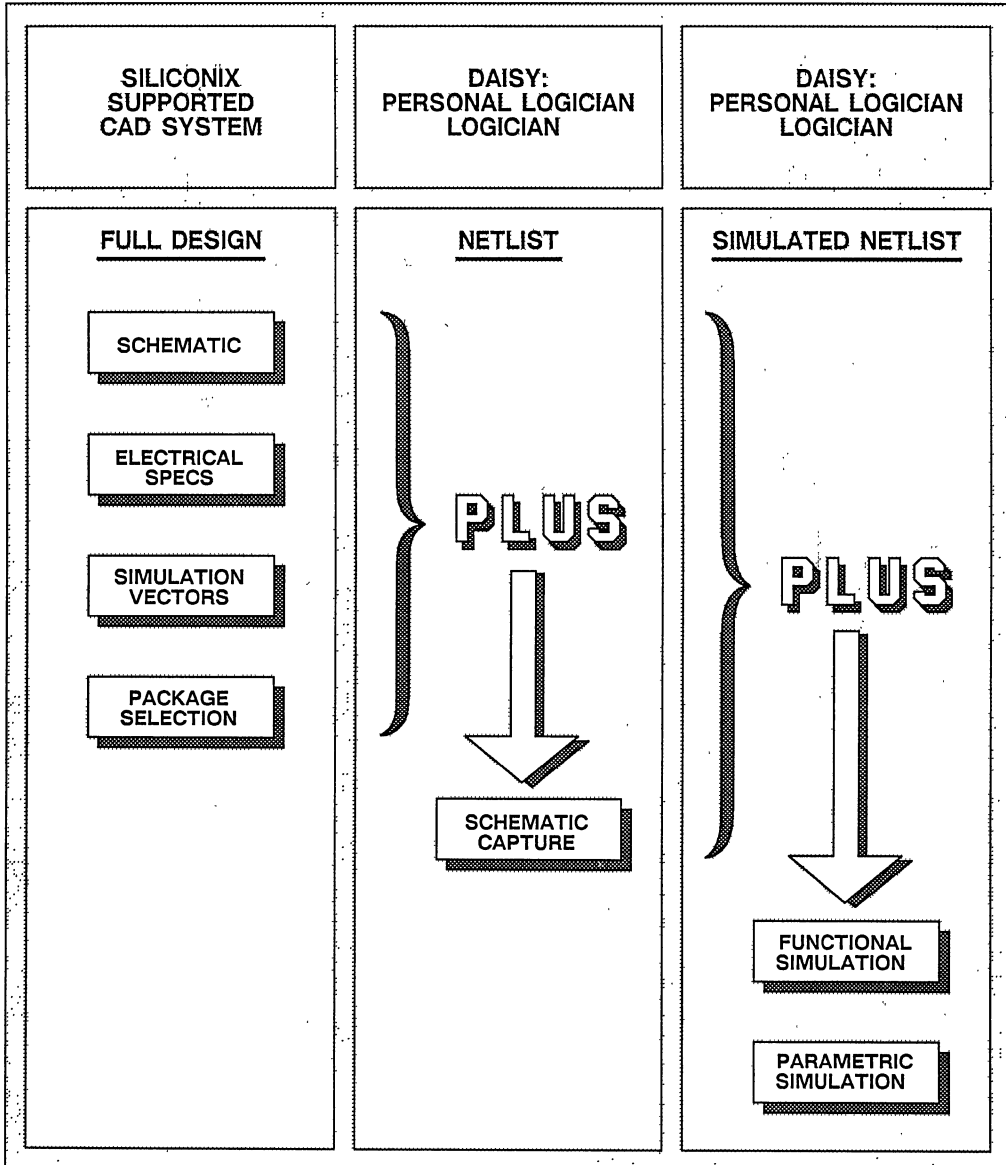
**EQUIVALENT GATE COUNT FOR APPROXIMATION OF ARRAY SIZE (Cont'd)**

DEVICE	CELLS	DESCRIPTION	DEVICE	CELLS	DESCRIPTION
4027	24	Dual J-K Flip Flop	4510	74	BCD Up/Down Counter
4028	24	BCD to Decimal Decoder	4512	25	8-Channel Data Selector
4029	55	Binary/Decade Up/Down Counter	4513	64	BCD to 7 Seg. Latch/Dec./Driver
4032	46	Triple Serial Adder (Positive)	4514	68	4/16 Line Decoder (High)
4034	145	8-Bit Universal Bus Register	4515	78	4/16 Line Decoder (Low)
4035	43	4-Stage Shift Register	4516	147	Binary Up/Down Counter
4038	45	Triple Serial Adder (Negative)	4518	70	Dual BCD Up Counter
4042	40	Quad Latch Coder/Driver	4519	23	4-Bit AND/OR Selector
4043	16	Quad NOR R-S Latch	4520	64	Dual Binary Up Counter
4044	16	Quad NAND R-S Latch	4522	74	BCD Divide-by-N Counter
4046	10	Phase Locked Loop	4526	74	Binary Divide-by-N Counter
4049	6	Hex Inverter/Buffer	4528	26	Dual Monostable Multivibrator
4050	10	Hex Buffer	4529	38	Dual 4-Channel Multiplexer
4051	33	8-Channel Analog Multiplexer	7400	3	Quad 2-NAND Gate
4052	65	Dual 4-Channel Analog Multiplexer	7401	3	Quad 2-NAND Gate (O.C.)
4053	105	Triple 3-Channel Analog Mult.	7402	4	Quad 2-NOR Gate
4066	24	Quad Bilateral Switch	7403	4	Quad 2-NAND Gate (O.C.)
4068	12	8-Input NAND Gate	7404	3	Hex Inverter
4069	4	Hex Inverter	7405	3	Hex Inverter
4070	8	Quad Exclusive OR Gate	7408	4	Quad 2-AND Gate
4071	13	Quad 2-Input OR Gate	7409	4	Quad 2-AND Gate (O.C.)
4072	13	Dual 4-Input OR Gate	7410	3	Triple 3-NAND Gate
4073	15	Triple 3-Input AND Gate	7411	5	Triple 3-AND Gate
4075	15	Triple 3-Input OR Gate	7412	3	Triple 3-NAND Gate (O.C.)
4076	40	Quad D-Type Register	7413	8	Dual Schmitt Trigger
4077	8	Quad Exclusive NOR Gate	7414	24	Hex Schmitt Trigger
4078	12	8-Input NOR Gate	7415	5	3-AND Gate (O.C.)
4081	14	Quad 2-Input AND Gate	7420	3	Dual 4-NAND Gate
4082	12	Dual 4-Input AND Gate	7421	4	Dual 4-AND Gate
4093	9	Quad 2-1 and Schmitt Trigger	7422	3	Dual 4-NAND Gate (O.C.)
4094	93	8-Stage Shift/Store Register	7426	4	High Volt Quad 2-NAND Gate
4099	65	8-Bit Addressable Latch	7427	3	Triple 3-NOR Gate
40160	74	Decade Counter	7430	3	8-Input NAND Gate *
40161	74	Binary Counter	7432	4	Quad 2-OR Gate
40162	74	Decade Counter	7437	3	Quad 2-NAND Buffer
40163	76	Binary Counter	7438	3	Quad 2-NAND Buffer (O.C.)
40174	86	Hex D Flip Flop	7440	3	Dual 4-NAND Buffer
40175	24	Quad D Flip Flop	7442	26	BCD to Decimal Decoder
40194	129	4-Bit Univ. Shift Register	7447	48	BCD/7-Segment Decoder/Driver
4502	8	Strobed Hex Inverter/Buffer	7448	51	BCD/7-Segment Decoder/Driver
4503	6	Hex Three-State Buffer	7451	10	Dual 2-AND-OR-INV Gate
4504	5	Hex Level Shifter	7454	9	Quad 2-AND-OR-INV Gate
4508	17	Dual 4-Bit Latch	7455	5	Dual 4-Input Gate

## EQUIVALENT GATE COUNT FOR APPROXIMATION OF ARRAY SIZE (Cont'd)

DEVICE	CELLS	DESCRIPTION	DEVICE	CELLS	DESCRIPTION
7473	24	Low Power-Schottky Dual J-K FF	74164	35	8-Bit Shift Register
7474	16	Dual D Flip Flop	74168	105	Decade Up/Down Counter
7475	29	Quad Latch	74169	87	Binary Up/Down Counter
7476	28	Dual J-K Flip Flop	74173	56	Tri-State Quad D Register
7477	32	Quad Latch	74174	36	Hex D Flip Flop
7478	28	Dual J-K W/Pre Co	74175	24	Quad D Flip Flop
7483	47	4-Bit Full Adder	74190	108	Up/Down Decade Counter
7585	111	4-Bit Magnitude Comparator	74191	109	Up/Down Binary Counter
7486	8	Quad Exclusive OR Gate	74192	104	Up/Down Decade Counter
74107	24	Dual J-K Flip Flop	74193	105	Up/Down Binary Counter
74109	24	Dual J-K Flip Flop	74196	80	Presetable Decade Counter
74112	28	J-K Flip Flop (Negative)	74197	77	Presetable Binary Counter
74113	24	Dual J-K Flip Flop	74247	48	BCD/7-Segment Decoder/Driver
74114	28	Dual J-K Flip Flop	74248	48	BCD/7-Segment Decoder/Driver
74125	8	Tri-State Quad Buffer	74249	40	BCD/7-Segment Decoder/Driver
74126	8	Tri-State Quad Buffer	74253	48	Dual 4-Input Multiplexer***
74132	16	Quad Schmitt Trigger	74257	12	Quad 2-Input Multiplexer***
74138	24	Expandable 3/8 Decoder	74266	8	Quad Exclusive NOR Gate
74139	18	Expandable Dual 2/4 Decoder	74279	12	Quad Set-Reset Latch
74151	86	8-Input Multiplexer	74283	53	4-Bit Full Adder
74153	24	Dual 4-Input Multiplexer	74353	24	Tri-State Dual 4-Bit Mux (Inv Out)
74154	130	4-Line to 16-Line Decoder**	74365	33	Tri-State Hex Buffer
74155	20	Dual 2/4 Demultiplexer	74366	29	Tri-State Hex Inverter
74156	20	Dual J-K Flip Flop	74367	21	Tri-State Hex Buffer
74157	32	Quad 2/1 Multiplexer	74368	16	Tri-State Hex Buffer
74158	32	Quad 2/1 Multiplexer (Inv Out)	74373	64	Tri-State Octal D Flip Flop
74160	87	Preset Decade Counter	74386	8	Quad Exclusive OR Gate
74161	91	Preset Binary Counter			
74162	90	Preset Decade Counter (Syn-Cir)			* Do not use except for slow speeds
74163	93	Preset Binary Counter (Syn-Cir)			** Simpler using transmission gates
					***Use transmission gates and decode









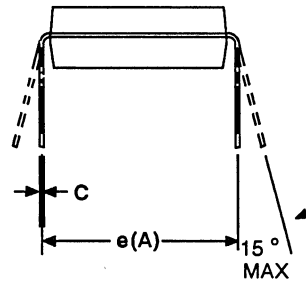
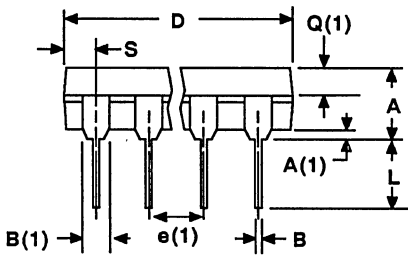
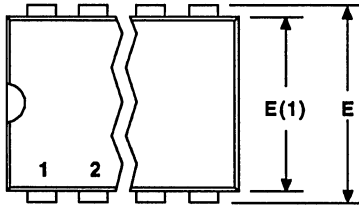
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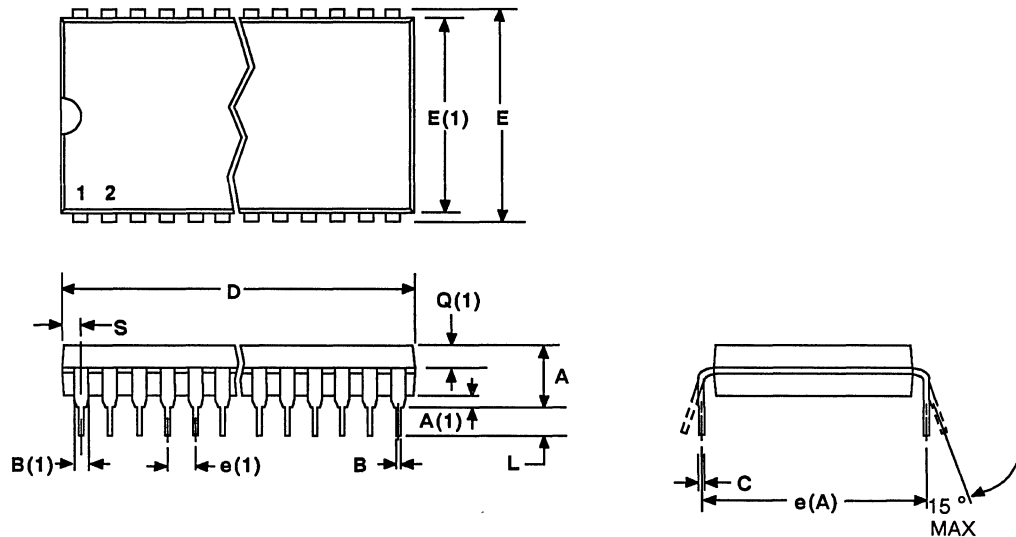
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# Plastic DIP (J, N Suffix), 8-16 Leads

DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.81	5.08	.150	.200
A(1)	.38	1.27	.015	.050
B	.38	.51	.015	.020
B(1)	.89	1.65	.035	.065
C	.20	.30	.008	.012
D-8	9.65	11.68	.380	.460
D-14	17.27	19.30	.680	.760
D-16	18.93	21.33	.745	.840
D-18	22.35	24.38	.880	.960
D-20	24.89	26.92	.980	1.060
E	7.62	8.26	.300	.325
E(1)	5.59	7.11	.220	.280
e(1)	2.29	2.79	.090	.110
e(A)	7.37	7.87	.290	.310
L	3.175	3.81	.125	.150
Q(1)	1.27	2.03	.050	.080
S-8	1.02	2.03	.040	.080
S-14	1.02	2.03	.040	.080
S-16	.38	1.52	.015	.060
S-18	1.02	2.03	.040	.080
S-20	1.02	2.03	.040	.080

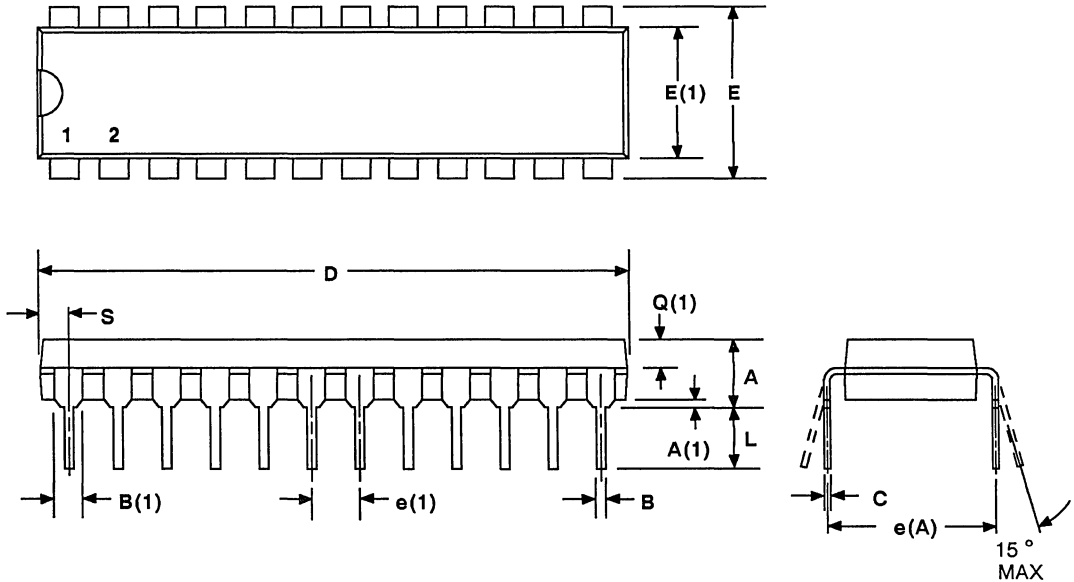


# Plastic DIP (J, N Suffix), 24-48 Leads



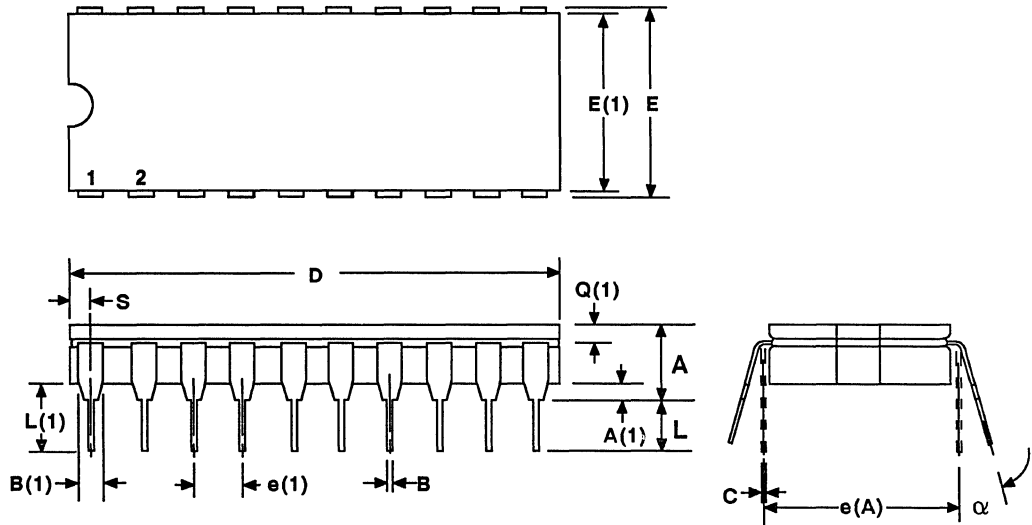
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.81	5.08	.150	.200
A(1)	.38	1.27	.015	.050
B	.38	.51	.015	.020
B(1)	.89	1.65	.035	.065
C	.20	.30	.008	.012
D-24	29.97	33.02	1.180	1.300
D-28	35.05	38.10	1.380	1.500
D-40	50.29	53.34	1.980	2.100
D-48	60.45	63.50	2.380	2.500
E	15.24	15.88	.600	.625
E(1)	13.21	14.73	.520	.580
e(1)	2.29	2.79	.090	.110
e(A)	14.99	15.49	.590	.610
L	3.175	5.08	.125	.200
Q(1)	1.27	2.03	.050	.080
S	1.02	2.54	.040	.100

# Plastic DIP (J, N Suffix), 24 Leads, 0.3" Narrow Body



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.81	5.08	.150	.200
A(1)	.38	1.27	.015	.050
B	.38	.51	.015	.020
B(1)	.89	1.65	.035	.065
C	.20	.30	.008	.012
D	29.97	32.00	1.180	1.260
E	7.62	8.26	.300	.325
E(1)	5.59	7.11	.220	.280
e(1)	2.29	2.79	.090	.110
e(A)	7.37	7.87	.290	.310
L	3.175	3.81	.125	.150
Q(1)	1.27	2.03	.050	.080
S	1.02	2.03	.040	.080

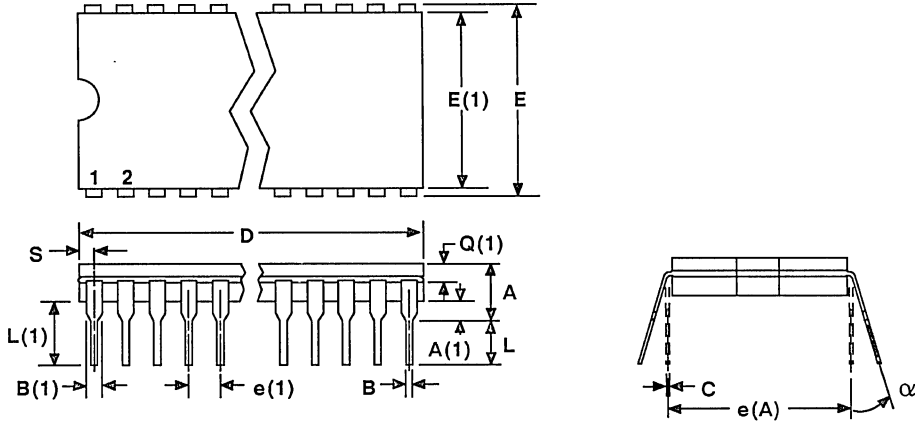
# CerDIP (K, Q Suffix), 14-20 Leads



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.06	5.08	.160	.200
A(1)	.51	1.14	.020	.045
B	.38	.51	.015	.020
B(1)	1.14	1.65	.045	.065
C	.20	.30	.008	.012
D-14	19.05	19.56	.750	.770
D-16	19.05	19.56	.750	.770
D-18	22.35	22.86	.880	.900
D-20	23.88	24.38	.940	.960
E	7.62	8.26	.300	.325
E(1)	6.60	7.62	.260	.300
e(1)	2.54 BSC		.100 BSC	
e(A)	7.62 BSC		.300 BSC	
L	3.18	3.81	.125	.150
L(1)	3.81	5.08	.150	.200
Q(1)	1.27	2.16	.050	.085
S-14	1.65	2.41	.065	.095
S-16	.38	1.14	.015	.045
S-18	.76	1.52	.030	.060
S-20	.25	1.02	.010	.040
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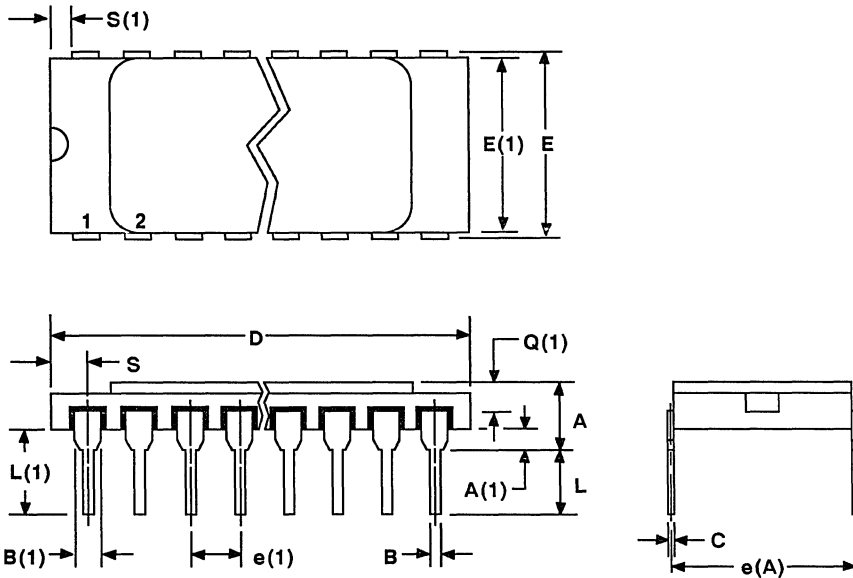


# CerDIP (K, Q Suffix), 24-40 Leads, 0.6" Wide Body



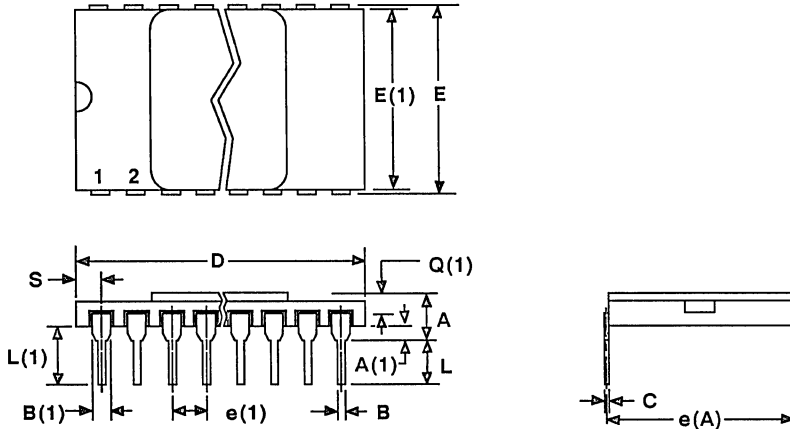
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.06	5.08	.160	.200
A(1)	.51	1.14	.020	.045
B	.38	.51	.015	.020
B(1)	1.14	1.65	.045	.065
C	.20	.30	.008	.012
D-24	31.50	32.00	1.240	1.260
D-28	36.58	37.08	1.440	1.460
D-40	51.82	52.32	2.040	2.060
e(1)	2.54 BSC		.100 BSC	
e(A)	15.24 BSC		.600 BSC	
E	15.24	15.88	.600	.625
E1	12.95	13.46	.510	.530
L	3.18	3.81	.125	.150
L1	3.81	5.08	.150	.200
Q1	1.27	2.16	.050	.085
S	1.52	2.29	.060	.090
$\alpha$	0°	15°	0°	15°

# Side Braze DIP (P, D Suffix), 14-24 Leads



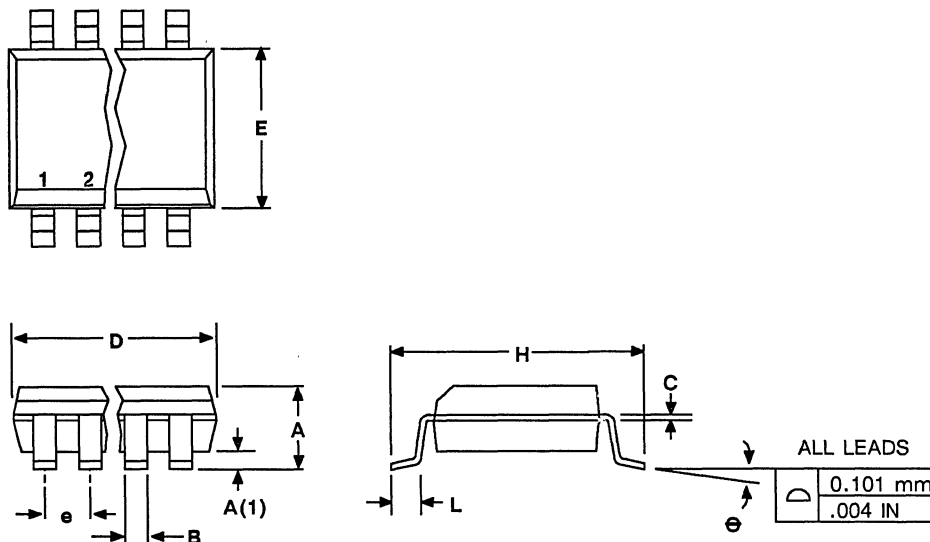
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.67	4.44	.105	.175
A(1)	.64	1.39	.025	.055
B	.38	.53	.015	.021
B(1)	.97	1.52	.038	.060
C	.20	.30	.008	.012
D-14	17.53	19.55	.690	.770
D-16	19.56	21.08	.770	.830
D-18	22.36	23.62	.880	.930
D-20	24.89	26.16	.980	1.030
D-24	29.97	31.24	1.180	1.230
E	7.37	8.25	.290	.325
E(1)	7.12	7.87	.280	.310
e(1)	2.54 BSC		.100 BSC	
e(A)	7.62 BSC		.300 BSC	
L	3.18	4.44	.125	.175
Q(1)	.25	-	.010	-
S-14	.77	2.41	.030	.095
S-16	.51	1.65	.020	.065
S-18	.77	1.65	.030	.065
S-20	.77	1.65	.030	.065
S-24	.77	2.41	.030	.095

# Side Braze DIP (P, R, D Suffix) 24-48 Leads, 0.6" Wide Body



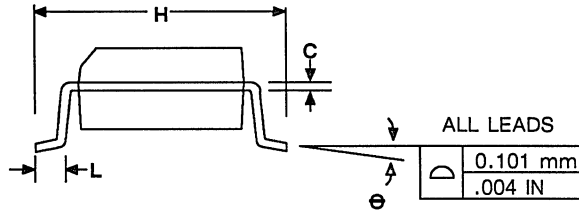
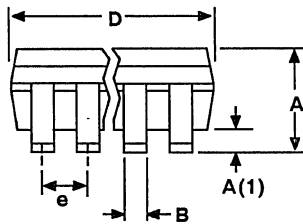
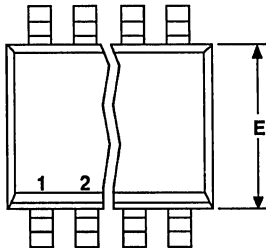
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	4.83	.085	.190
A(1)	.51	1.78	.020	.070
B	.38	.58	.015	.023
B(1)	.97	1.52	.038	.060
C	.20	.30	.008	.012
D-24	29.98	30.98	1.180	1.220
D-28	35.06	36.22	1.380	1.430
D-40	50.30	51.56	1.980	2.030
D-48	60.45	61.72	2.380	2.430
E	15.12	15.87	.595	.625
E(1)	14.73	15.49	.580	.610
e(1)	2.54 BSC		.100 BSC	
e(A)	15.24 BSC		.600 BSC	
L	3.18	4.45	.125	.175
Q(1)	.25	-	.010	-
S	.76	1.65	.030	.065

# SO Package (Y Suffix), 8-16 Leads



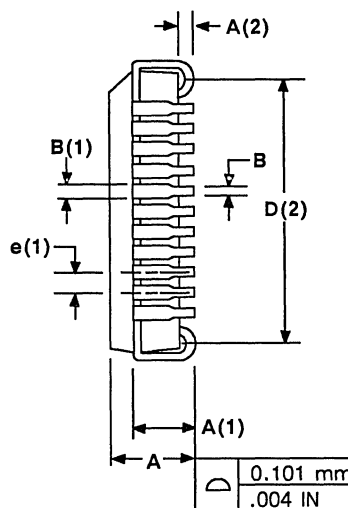
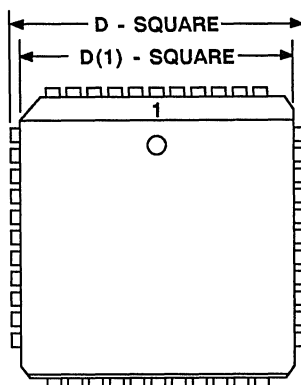
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	.053	.069
A(1)	.10	.20	.004	.008
B	.35	.45	.014	.018
C	.18	.23	.007	.009
D-8	4.60	5.20	.181	.205
D-14	8.35	8.95	.329	.352
D-16	9.60	10.20	.378	.402
E	3.55	4.05	.140	.160
e	1.27 BSC		.050 BSC	
H	5.70	6.30	.224	.248
L	.60	.80	.024	.031
$\theta$	0°	8°	0°	8°

# SO Package (Y Suffix), 16-28 Leads, Wide Body



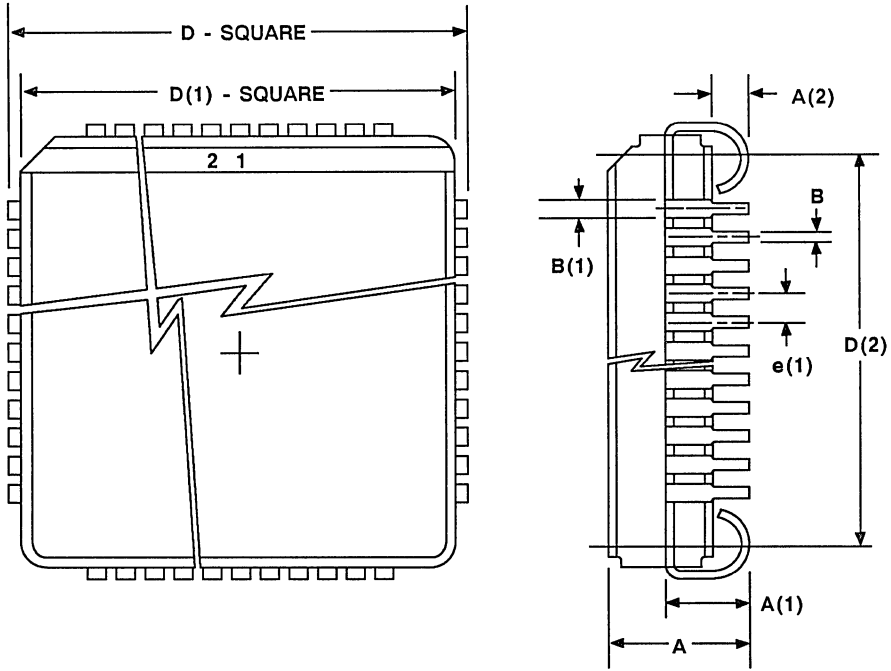
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.15	2.90	.085	.114
A(1)	.10	.30	.004	.012
B	.35	.45	.014	.018
C	.23	.28	.009	.011
D-16	9.95	10.75	.392	.423
D-18	11.25	12.45	.443	.490
D-20	12.50	13.30	.492	.524
D-24	15.05	15.85	.593	.624
D-28	17.60	18.40	.693	.724
E	7.25	8.00	.285	.315
e	1.27 BSC		.050 BSC	
H	9.80	10.60	.386	.417
L	.60	1.00	.024	.039
$\theta$	0°	8°	0°	8°

# PLCC Package (N, P Suffix), 20-84 Leads



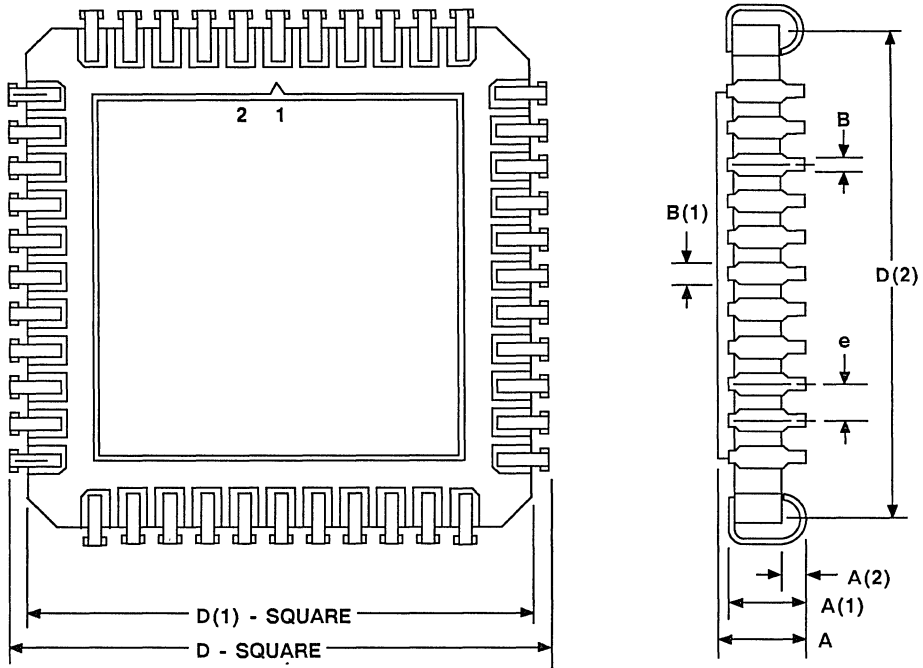
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	4.57	.165	.180
A(1)	2.29	3.04	.090	.120
A(2)	.51	-	.020	-
B	.331	.553	.013	.021
B(1)	.661	.812	.026	.032
D-20	9.78	10.03	.385	.395
D-28	12.32	12.57	.485	.495
D-44	17.40	17.65	.685	.695
D-52	19.94	20.19	.785	.795
D-68	25.02	25.57	.985	.995
D-84	30.10	30.35	1.185	1.195
D(1)-20	8.890	9.042	.350	.356
D(1)-28	11.430	11.582	.450	.456
D(1)-44	16.510	16.662	.650	.656
D(1)-52	19.050	19.202	.750	.756
D(1)-68	24.130	24.330	.950	.958
D(1)-84	29.210	29.413	1.150	1.158
D(2)-20	7.37	8.38	.290	.330
D(2)-28	9.91	10.92	.390	.430
D(2)-44	14.99	16.00	.590	.630
D(2)-52	17.53	18.54	.690	.730
D(2)-68	22.61	23.62	.890	.930
D(2)-84	27.69	28.70	1.090	1.130
e(1)	1.27 BSC		.050 BSC	

# CerQuad Package (M Suffix), 28 & 44 Leads



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	4.83	.165	.190
A(1)	2.29	3.04	.090	.120
A(2)	.51	-	.020	-
B	.46	.56	.018	.022
B(1)	.66	.81	.026	.032
D-28	12.32	12.57	.485	.495
D-44	17.40	17.65	.685	.695
D(1)-28	11.23	11.63	.442	.458
D(1)-44	16.31	16.71	.642	.658
D(2)-28	9.91	10.92	.390	.430
D(2)-44	14.99	16.00	.590	.630
e(1)	1.27 BSC		.050 BSC	

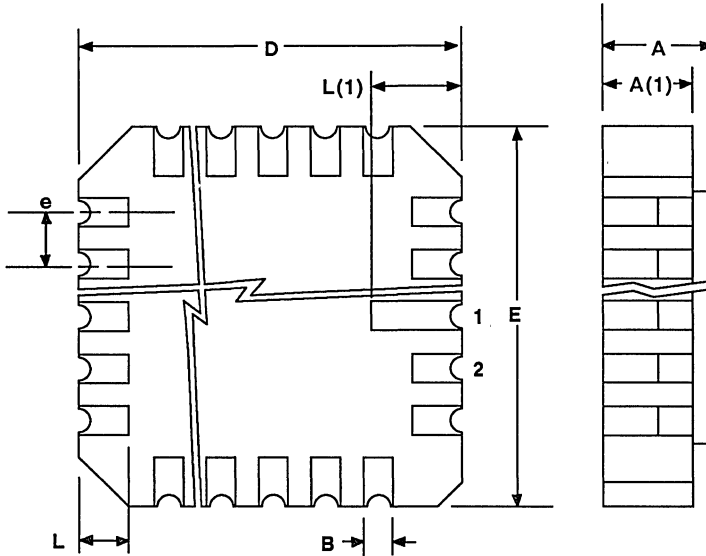
# CLCC Package (M Suffix), 44 Lead



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.54	3.43	.100	.135
A(1)	2.03	3.30	.080	.130
A(2)	.64	-	.025	-
B	.33	.58	.013	.023
B(1)	.51	.81	.020	.032
D	17.27	17.78	.680	.700
D(1)	15.95	16.81	.628	.662
D(2)	14.99	16.51	.590	.650
e	1.27 BSC		.050 BSC	

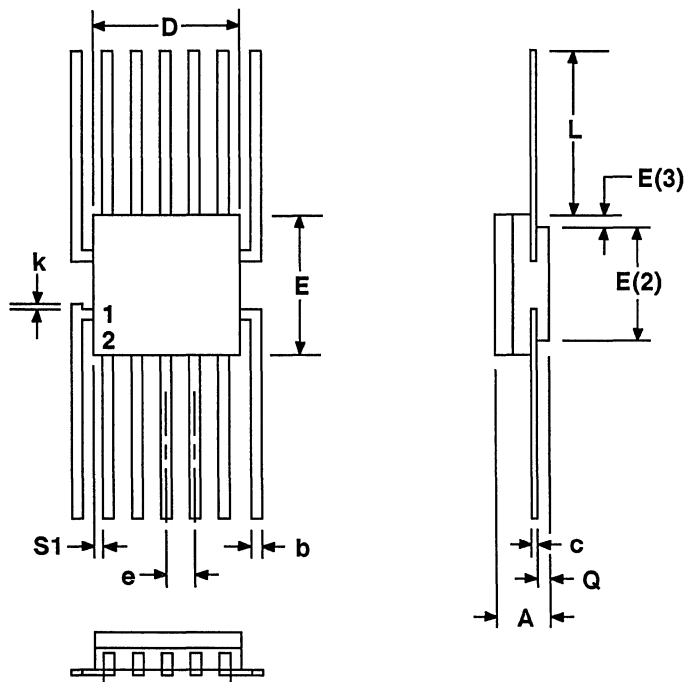


# LCC Package (Z, E Suffix), 20 & 28 Leads



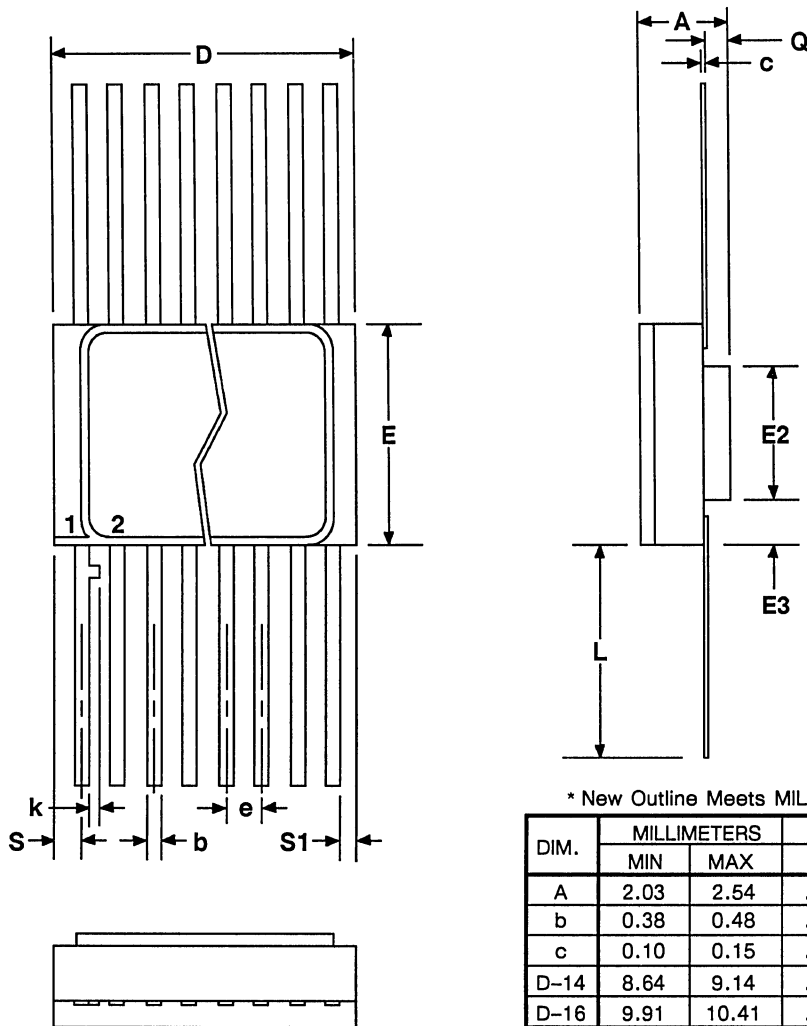
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	2.54	.060	.100
A(1)	1.27	2.16	.050	.085
B	.56	.71	.022	.028
D-20	8.69	9.09	.342	.358
D-28	11.23	11.63	.442	.458
E-20	8.69	9.09	.342	.358
E-28	11.23	11.63	.442	.458
e	1.27 BSC		.050 BSC	
L	1.14	1.40	.045	.055
L(1)	1.96	2.36	.077	.093

# Flat Package (L Suffix), 14 Lead, Obsolete Version



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.78	2.16	.070	.085
b	.38	.48	.015	.019
c	.10	.15	.004	.006
D	6.10	6.60	.240	.265
E	6.10	6.60	.240	.265
e	1.27 BSC		.050 BSC	
E(2)	4.32	5.08	.170	.200
E(3)	.76	1.02	.030	.040
k	.20	.38	.008	.015
L	7.37	8.89	.290	.350
Q	.25	.51	.010	.020
S1	.25	.64	.010	.025

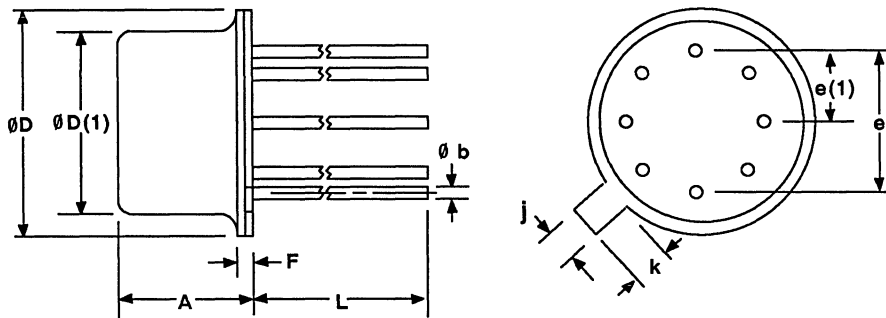
# Flat Package (L Suffix), 14 & 16 Leads



\* New Outline Meets MIL-M-38510G

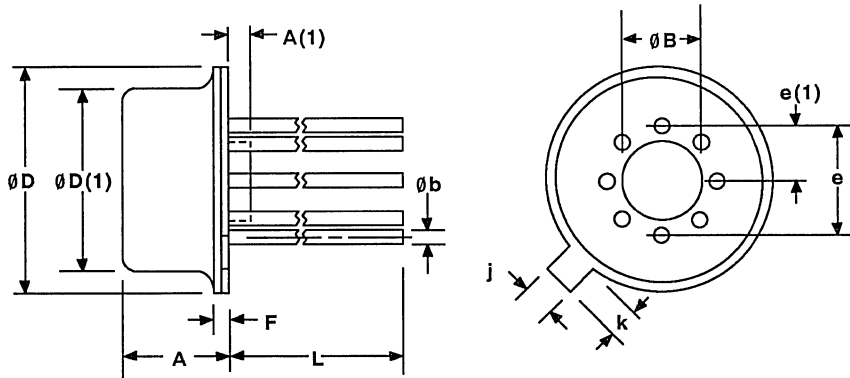
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.03	2.54	.080	.100
b	0.38	0.48	.015	.019
c	0.10	0.15	.004	.006
D-14	8.64	9.14	.340	.410
D-16	9.91	10.41	.390	.410
E-14	6.10	6.60	.240	.260
E-16	6.60	7.11	.260	.280
e	1.27 BSC		.050 BSC	
E2	4.45	4.95	.175	.195
E3	0.76	1.27	.030	.050
k	0.20	0.38	.008	.015
L	7.62	8.89	.300	.350
Q	0.66	1.14	.026	.045
S	-	1.14	-	.045
S1	0.13	-	.005	-

# MO-002AG (Formerly TO-78)



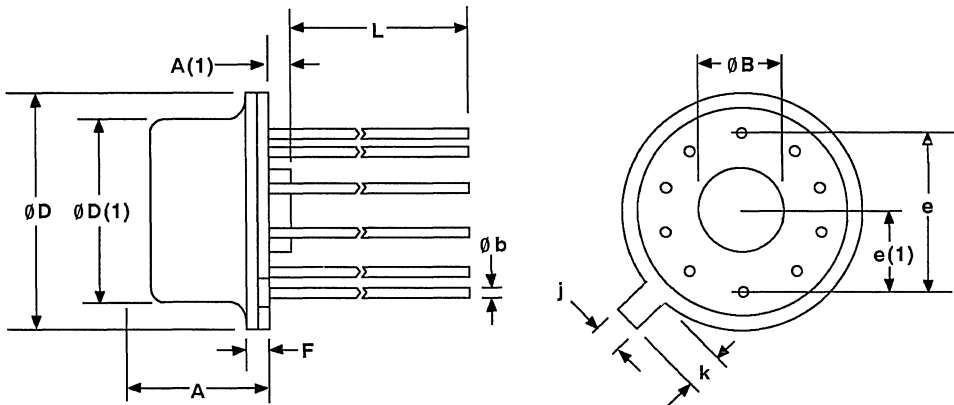
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.19	4.70	.165	.185
Ø b	.41	.53	.016	.021
Ø D	8.51	9.39	.335	.370
Ø D(1)	7.75	8.50	.305	.335
e	5.08 BSC		.200 BSC	
e(1)	2.54 BSC		.100 BSC	
F	-	1.02	-	.040
j	.71	.86	.028	.034
k	.74	1.14	.029	.045
L	12.70	-	.500	-

# MO-002AK (Formerly TO-99)



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.19	4.70	.165	.185
A(1)	.25	1.01	.010	.040
$\varnothing B$	3.56	4.06	.120	.160
$\varnothing b$	.41	.53	.016	.021
$\varnothing D$	8.51	9.39	.335	.370
$\varnothing D(1)$	7.75	8.50	.305	.335
e	5.08 BSC		.200 BSC	
e(1)	2.54 BSC		.100 BSC	
F	-	1.02	-	.040
j	.71	.86	.028	.034
k	.74	1.14	.029	.045
L	12.70	-	.500	-

# MO-006AD (Formerly TO-100)



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.19	4.70	.165	.185
A(1)	.25	1.02	.010	.040
$\emptyset B$	2.79	4.06	.120	.160
$\emptyset b$	.41	.53	.016	.021
$\emptyset D$	8.51	9.39	.335	.370
$\emptyset D(1)$	7.75	8.50	.305	.335
e	5.84 BSC		.230 BSC	
e(1)	2.92 BSC		.115 BSC	
F	-	1.02	-	.040
j	.71	.86	.028	.034
k	.74	1.14	.029	.045
L	12.70	-	.500	-



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# MICROPROCESSOR - COMPATIBLE MULTIPLEXERS FACILITATE VIDEO SWITCHING DESIGNS

Gareth Powell  
February 1988

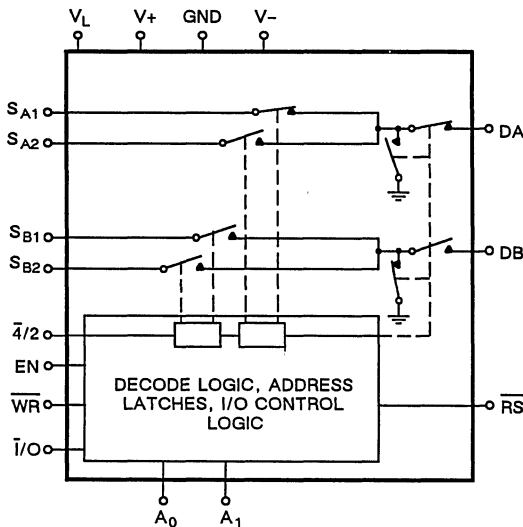
For many new communications systems – such as ISDN (Integrated Services Digital Network), cable TV, and local area networks (LANs) – traditional switching techniques have become inadequate. To meet the demands of these applications, semiconductor switching devices must now handle wider bandwidths and offer more on-chip features to achieve low chip-count solutions. Higher integration, smaller packages, easier device paralleling/combining, and improved dynamic performance are essential features for designing large-capacity switching systems.

Analog video information is frequently digitized for processing in frame grabbers, TV standard converter (e.g., NTSC to PAL), time-base correction, special effects, or merely as a means of reducing noise levels and enhancing resolution. However, the price paid for the advantages of the digital technique is the substantially wider bandwidth occupied by the digitized signal. Thus, in a typical 8-bit conversion, the

sampling rate must be at least three times the chrominance subcarrier frequency of 4.43 MHz: that is, 13.3 MHz. Thus, the bit rate is  $8 \times 13.3 = 106.44$  Mbps. This bandwidth requirement precludes the use of a majority of components and switching techniques commonly employed in video systems.

Video switching applications, such as high-definition TV, digital video equipment, and broadcast studio switches have forced improvements in semiconductor switch performance. The Siliconix DG534 and DG538 are members of a fast growing family of multiplexer/demultiplexer devices with performance characteristics optimized for wideband switching applications. This application note presents the benefits of the DG534 and DG538 in a diverse range of wideband switching applications, highlighting the devices' performance features and providing useful circuit design techniques.

All four DG534 Input switches are "T" switches.



All eight DG538 Input switches are "T" switches.

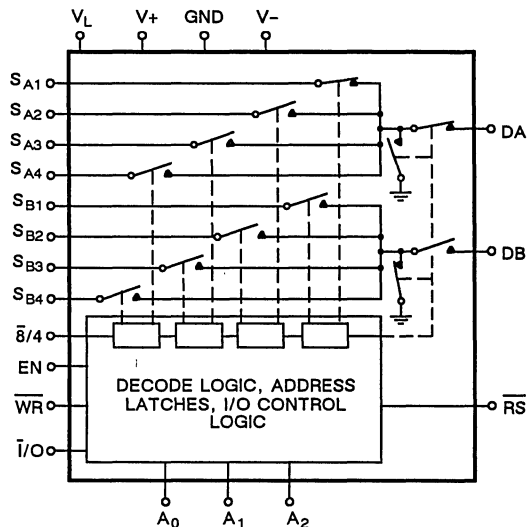


Figure 1. DG534 and DG538 Functional Schematics

## Device Description

The DG538 is a wideband single-ended 8-to-1 or differential 4-channel multiplexer. Several DG538s can easily be configured to create a more complex matrix or to handle crosspoint functions. The DG534, similar to the DG538 with half the number of channels, is a 4-to-1 single-ended or a 2-to-1 differential multiplexer.

D/CMOS processing enables these devices to be optimized for high-frequency signal handling with low ON-resistance while on-chip CMOS circuitry provides all the level shifting, logic interfacing, and latching functions that permit easy system design. The switch structure utilizes lateral n-channel DMOS transistors configured in a "T" arrangement, as shown in Figure 1. The "T" switches are arranged into two groups. Each group is selected by the second-stage "L" switches. This two-level switching configuration minimizes channel capacitance and off-state signal crosstalk (maximizes OFF-isolation).

For comparison, Figure 2 shows the single-channel crosstalk characteristics of the DG538 video multiplexer and the industry-standard DG508A. Note the 35-dB performance improvement of the DG538 versus the standard CMOS 8-channel multiplexer.

The DG538 data sheet specifies all-hostile crosstalk. This is a much more rigorous test specification than

single-channel crosstalk since it requires all seven "off" channels to be tied together. More crosstalk signal is seen at the switch under these test conditions because there are seven parallel paths, as opposed to only one, and the crosstalk contribution of the package and the PC board are also more apparent. Nevertheless, the all-hostile crosstalk of the DG534 and DG538 approaches -70 dB at 5 MHz, easily meeting most video switching requirements.

It is not merely the "T" and "L" configurations that give improved crosstalk. Careful on-chip layout and optimum device sizing were also required. A small device exhibits low intrinsic capacitances, but has greater ON-resistance and, hence, will give a greater insertion loss. However, by employing DMOS (double diffused MOS) FETs for the switches, an excellent compromise between  $r_{DS(ON)}$  and intrinsic capacitances is achieved.

Figure 3 shows a cross section of an n-channel device made with the D/CMOS process, incorporating DMOS and PMOS transistors. The fabrication of the "T" switch is shown. The short-channel feature of the DMOS devices offers 8 to 10 times less channel capacitance than a conventional lateral NMOS transistor for a given  $r_{DS(ON)}$ . Figure 3 also shows the n- and p-channel devices that form the CMOS logic interface, level shifting, and latches.

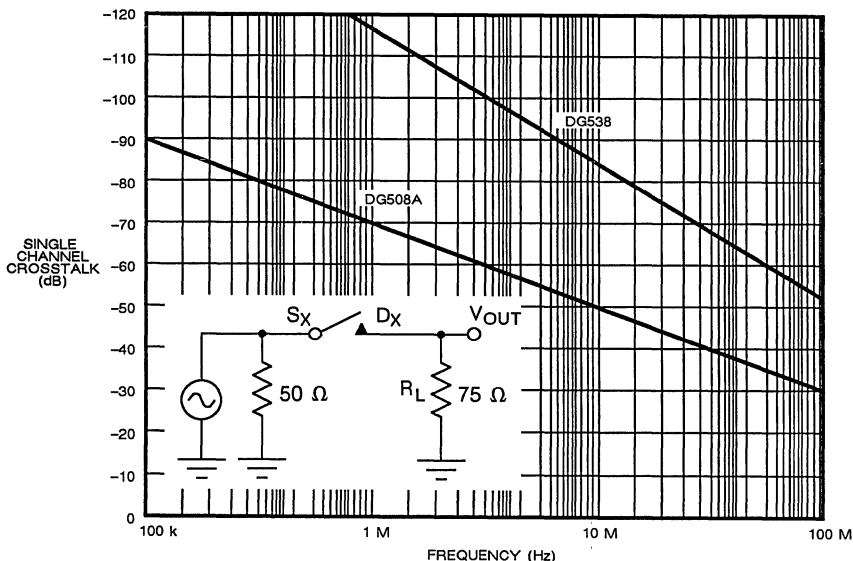


Figure 2. DG538/DG508A Single-Channel Crosstalk vs. Frequency

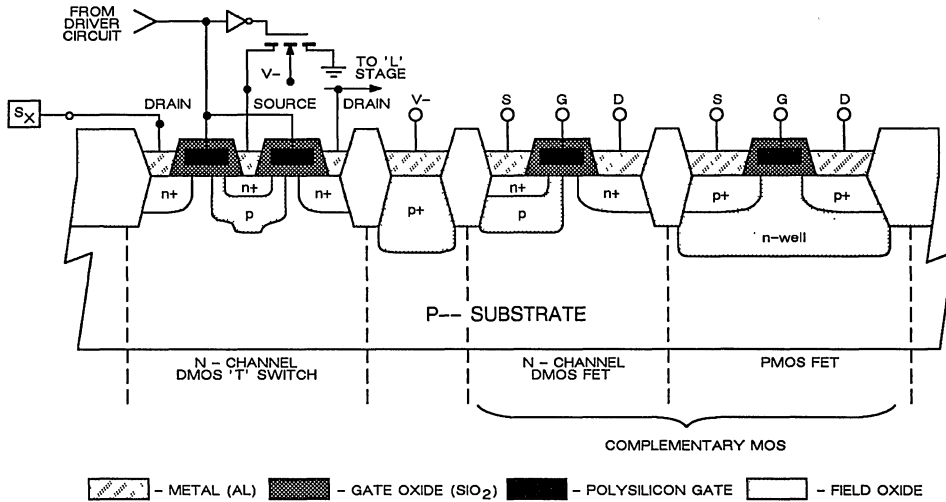


Figure 3. Cross Section of the D/CMOS Process

The cross section shows many pn junctions which would become forward biased if signals applied to the device were more negative than the "p" substrate. For this reason, when handling ac signals, the substrate is connected to a negative voltage ( $V^-$ ) to allow signals to swing below ground.

Using a negative supply also optimizes device capacitances. The body effect on DMOS devices causes the ON-state capacitance to change as a function of  $V^-$ . For a fixed analog signal,  $C_{ON}$  reduces exponentially as the source-to-substrate voltage increases (see Figure 4). Other performance benefits can be attained by choosing a particular  $V^-$  (see Figure 19).

In the event of an overvoltage (analog signal going more than a diode drop beyond  $V^-$ ), the pn junction between the source or drain and the substrate will forward bias, causing a large current to flow. This fault current will not damage the device as long as the current flow is less than 20 mA. However, low-impedance source circuitry is typical of many applications; for example, the output impedance of a video buffer amplifier is 75  $\Omega$ . Thus, a means of current limiting should be employed in circuits where overvoltage transients are possible. Figure 5 shows a transient protection scheme that uses a diode in  $V^-$ . This diode (normally forward biased) becomes reverse bi-

ased with overvoltage transients, thus eliminating fault current flow.

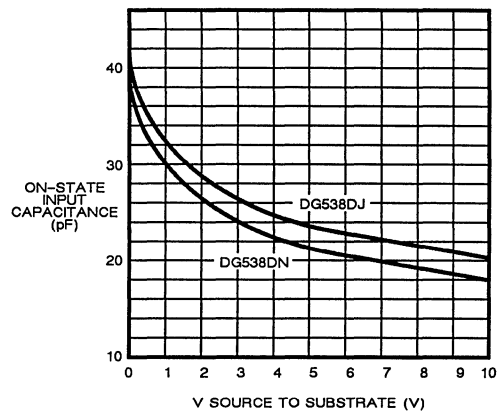


Figure 4. DG538 ON-state Input Capacitance vs. Source-to-Substrate Voltage

Positive overvoltages ( $> V^+$ ) are a different problem. The switch will merely turn OFF (no enhancement) if signals approach or exceed  $V^+$ . The DMOS drain diffusion has a fairly high breakdown voltage (typically  $> 30$  V). Large avalanche currents can flow during

breakdown, therefore, either the signals must be externally clamped to avoid exceeding breakdown voltage, or a means of external fault current limiting should be adopted. Since the source diffusion will only develop a voltage during the switch "ON" state, under normal supply conditions this breakdown (source-to-substrate) is unlikely to occur due to the device turning OFF when the source voltage,  $V_S$ , approaches  $V_+$ . Therefore, external positive overvoltage protection is only required when transients or overvoltages are expected to be in excess of +30 V.

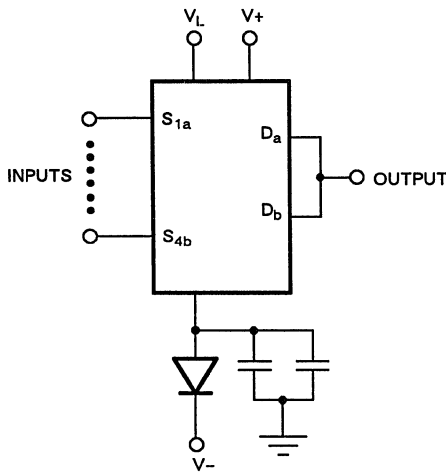


Figure 5. Negative Overvoltage Transient Protection

## Addressing and Logic

A DG538 device can be configured as a single-ended or as a differential multiplexer by applying the appropriate logic to the  $\bar{8}/4$  pin. When this pin is high (the differential condition), address  $A_2$  is not used. Note that  $D_A$  and  $D_B$  must be externally connected for the single-ended mode.

The logic trip-point reference for the internal comparators is derived from logic voltage,  $V_L$ , i.e., when  $V_L = +5$  V, true TTL compatibility is achieved. In this case, the logic levels required to activate the various control pins ( $\bar{8}/4$ ,  $\bar{I/O}$ ,  $EN$ ,  $A_X$ ,  $\overline{WR}$ ,  $\overline{RS}$ ) are 0.8 V and 2 V. Variation of  $V_L$  enables the switching threshold to be shifted (Figure 6).

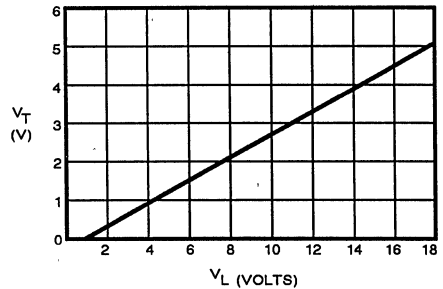


Figure 6. DG538 Switching Threshold vs. Logic Supply Voltage ( $V_L$ )

The DG538 and DG534 have tri-state latches on their address pins, allowing three modes of operation:

1. **Input Data.** In this mode, the multiplexer accepts data applied to  $A_X$  causing appropriate switch selection. This mode is selected by the following logic conditions:

$$\begin{aligned} \bar{I/O} &= 0 \text{ (input mode)} \\ \overline{WR} &= 0 \text{ (latches transparent)} \\ EN &= 1 \text{ (device enabled)} \\ \overline{RS} &= 1 \end{aligned}$$

2. **High Impedance.** In this mode, the address pins assume a high impedance (open circuit) state. It is selected by

$$\begin{aligned} \bar{I/O} &= 0 \\ \overline{WR} &= 1 \text{ (data latched state)} \\ EN &= X \\ \overline{RS} &= 1 \end{aligned}$$

The tri-state (high-impedance) mode of operation is particularly useful in microprocessor-controlled systems. It enables many devices to be paralleled on a common control bus without significant loading. This feature helps fulfill the demands of large matrix systems.

By decoding the microprocessor's address bus, the DG538/DG534 can be activated to respond to logic control signals transmitted by the microprocessor on its data bus, only when required to do so.

3. **Output Data.** The last data written to the latches are reflected as logic outputs on  $A_0$ ,  $A_1$ , and  $A_2$ . This is achieved when

$$\overline{I/O} = 1 \text{ (output mode)}$$

$$\overline{WR} = 1$$

$$EN = 1$$

$$\overline{RS} = 1$$

The “data readback” feature is convenient in handshaking functions where “route-selected” status monitoring is required. This also eliminates additional peripheral devices for this function. Data readback may also be used to preserve the switch configuration during and after a power failure to the microprocessor. Normally after power failure, the microprocessor must go through a complete system reset routine. Provided power to the DG538/DG534 has not been disrupted, when the microprocessor’s power is re-established, it can poll the multiplexers and resume immediate control. This capability simplifies microprocessor software requirements and reduces service interruptions.

In the address output state, the address outputs can source or sink 0.4 mA. Logic high from the address output is  $V_L$ . When operating  $V_L$  at voltages higher than +5 V, it is important to consider the possibility of damaging effects on TTL devices connected to the address bus.

To ease microprocessor interfacing, additional control pins are featured.

- $\overline{WR}$ . This input activates the data latches for strobing-in an address word when  $\overline{WR}$  goes low (i.e., transparent latches). The strobing signal is normally obtained by decoding the microprocessor address data. This pin eliminates the need for external latches or peripheral devices such as I/O ports for connection to the microprocessor’s bus.
- $\overline{RS}$ . This input initiates a direct reset command that clears all data latches and opens all switches. This pin can be used as a “master re-

set.” It is of particular significance during system power-up since the microprocessor’s reset control pin may be used to clear all switches prior to channel/routing selection. Thus, the software used to sequentially clear all multiplexers is unnecessary.

Figure 7 illustrates the ease of microprocessor interface with the DG538 and shows an alternate use for the  $\overline{RS}$  function as a chip-select control in a 32-to-1 video switching application. The  $\overline{RS}$  function overrides all other control signals. Note that  $\overline{RS}$  is not a latched input. An external D-type latch is required so that  $A_4$  can be connected directly to the data bus.  $A_0$  to  $A_3$  are latched internally to the DG538.

The 8085 microprocessor data bus (after having its low-order address lines demultiplexed) connects directly to the address inputs ( $A_0$  to  $A_2$ ) on all the DG538s and on  $A_3$  and  $A_4$ . The system responds to stimuli on the data bus only when a write command is received. A write signal is produced by first decoding three (or more) lines of the high-order address lines using a 3-to-8 decoder and then gating (OR) one of the decoder output lines with the microprocessor’s  $\overline{WR}$  output. This enables switch selection only when the appropriate address data is received; otherwise, switch states remain latched and their control inputs are all in the high-impedance mode, leaving the microprocessor’s data bus free to execute other routines.

Switch inputs 1 to 32 can be selected by a 5-bit word transmitted on the data bus coinciding with a write signal.

Even though the  $\overline{RS}$  pins on the four DG538 devices are used for chip select, a direct reset or no-channel-selected condition is easily achieved using a CMOS analog switch (DG303A), as shown in Figure 7.

An important consideration for direct microprocessor interface is input timing compatibility. Table 1 shows minimum input timing requirements of the DG538/DG534 compared with the corresponding minimum output timing specifications of some popular microprocessors.

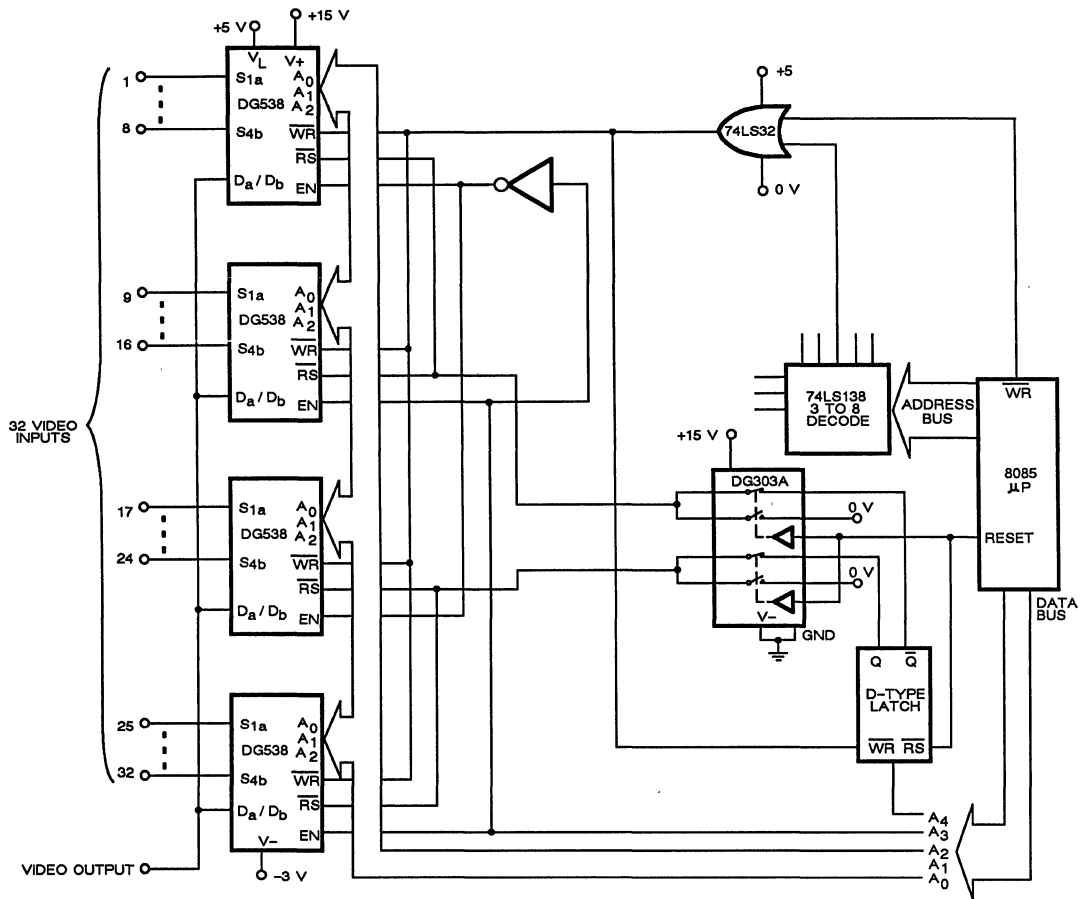


Figure 7. A 32-Channel Single-Ended Wideband Multiplexer Controlled by an 8085

Methods of interface to other microprocessors are shown in Figure 8. An address decoder (for a memory-mapped type of operation) is required for all interface circuits. Various gating arrangements are required, depending on the microprocessor's peripheral control output architecture.

In some cases, it might be convenient to use  $\overline{RS}$  as a

power-up failsafe. The circuit shown in Figure 9 illustrates a method for using  $\overline{RS}$  as a power-up delay circuit. This allows microprocessor buses or control logic sources to stabilize after power-up before the DG538 responds to control signals. During power-up, indeterminate logic states and/or transients might be present on control or data lines. The RC values are set to ignore spurious control signals.

TABLE 1. Microprocessor Timing Compatibility

PARAMETER		DG538/4	8085A	8085A-2	Z80	6800	
$t_{WW}$	Width of Control Low ( $\overline{WR}$ )	(ns)	200 (min)	400 (min)	230 (min)	360 (min)	470 (min)
$t_{DW}$	Data Valid to Trailing Edge of Write	(ns)	100 (min)	420 (min)	230 (min)	200 (min)	575 (min)
$t_{WD}$	Data Valid to Trailing Edge of Write	(ns)	50 (min)	100 (min)	60 (min)	100 (min)	150 (min)

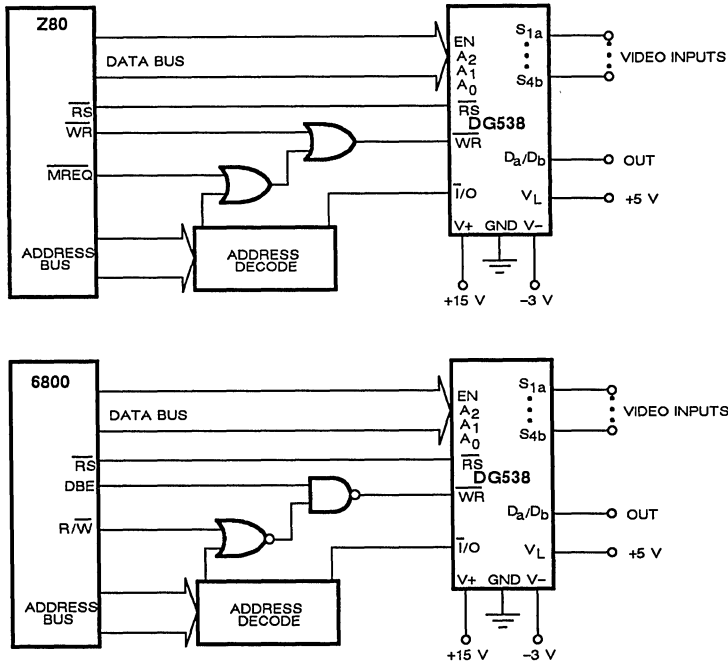


Figure 8. Other Microprocessor Interfaces

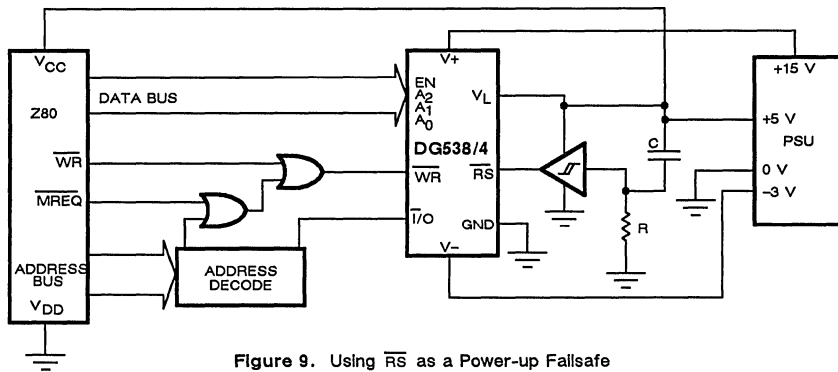


Figure 9. Using  $\overline{RS}$  as a Power-up Fallsafe

**Characteristics**

The DG538 and DG534 data sheets include detailed operating characteristics, typical parameters, and limit values. The important dynamic characteristics, such as crosstalk and bandwidth, are plotted against frequency (to 100 MHz) to help designers predict system performance, since these parameters are

measures of the ON-state and OFF-state multiplexer performance.

Specialized video specifications not included on the data sheet are presented here to provide a better understanding of the devices' performance and suitability for a wide range of video and general wideband switching applications.

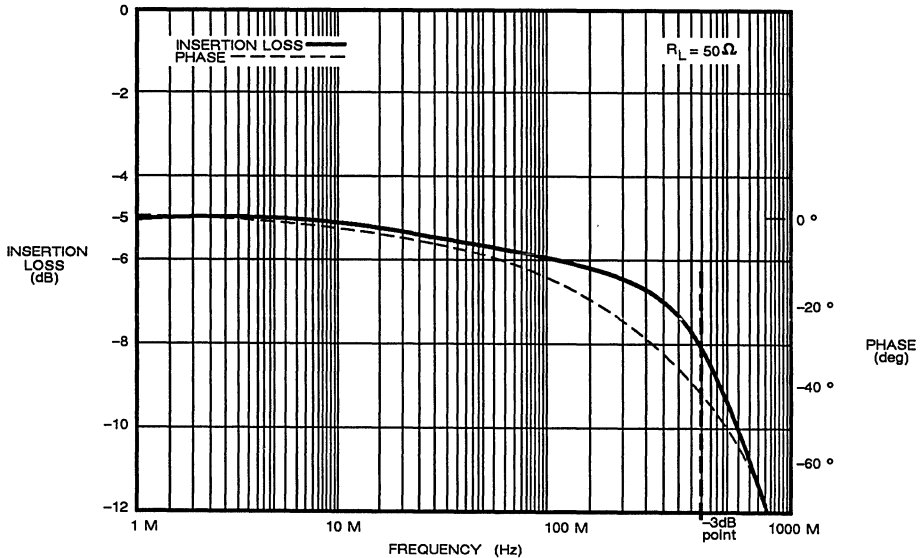


Figure 10. DG538 Bandwidth and Phase Response

**Bandwidth** is a measure of the ON-state performance and is defined as the frequency at which the signal falls -3 dB from the low-frequency insertion loss figure. Figure 10 shows the typical frequency characteristics of the DG538 measured on an HP8573A network analyzer.

Since a multiplexer channel exhibits ON-resistance,  $r_{DS(ON)}$ , and ON-state capacitance,  $C_{(ON)}$ , increasing signal frequencies are progressively attenuated. However, it is a common misconception that the bandwidth can be calculated from the  $r_{DS(ON)}$  and  $C_{(ON)}$  specifications given on the data sheet.

The -3 dB frequency for the model shown in Figure 11 is given by the formula:

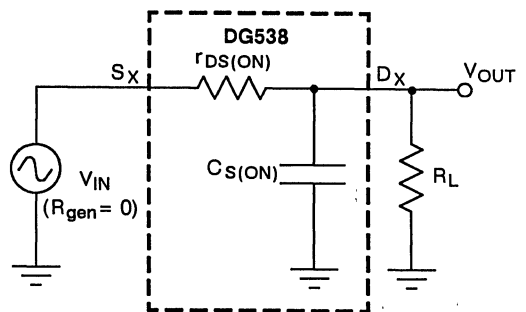
$$-3 \text{ dB} = \frac{1}{2 \pi \left[ \frac{R_L \times r_{DS(ON)}}{R_L + r_{DS(ON)}} \right] C_{(ON)}}$$

Substituting  $R_L = 50 \Omega$ ,  $r_{DS(ON)} = 50 \Omega$ , and  $C_{(ON)} = 23 \text{ pF}$  gives an  $f_{-3 \text{ dB}} \approx 310 \text{ MHz}$

The measured frequency response for the same  $50 \Omega$  load (Figure 10) shows a -3 dB point of

over 500 MHz. This apparent discrepancy results because the  $r_{DS(ON)}$  and  $C_{(ON)}$  are distributed among the five DMOS FETs that form the "T" and "L" switches.

A SPICE simulation of the model shown in Figure 12 gave a 510 MHz -3 dB point, which is much closer to the measured value (see Figure 13).



$$\text{INSERTION LOSS (dB)} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Figure 11. Erroneous Model for Frequency Response Calculations



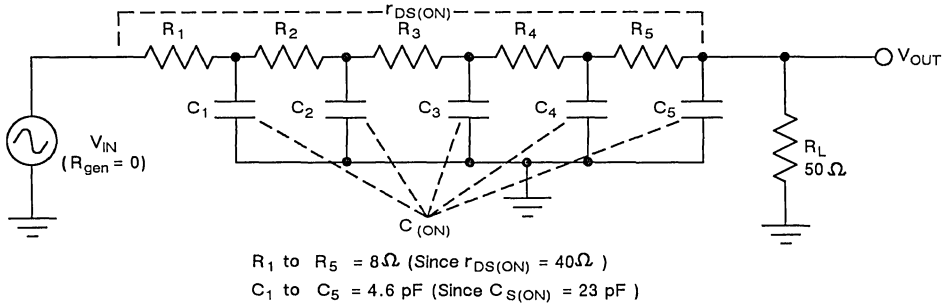


Figure 12. Five-Stage RC Model

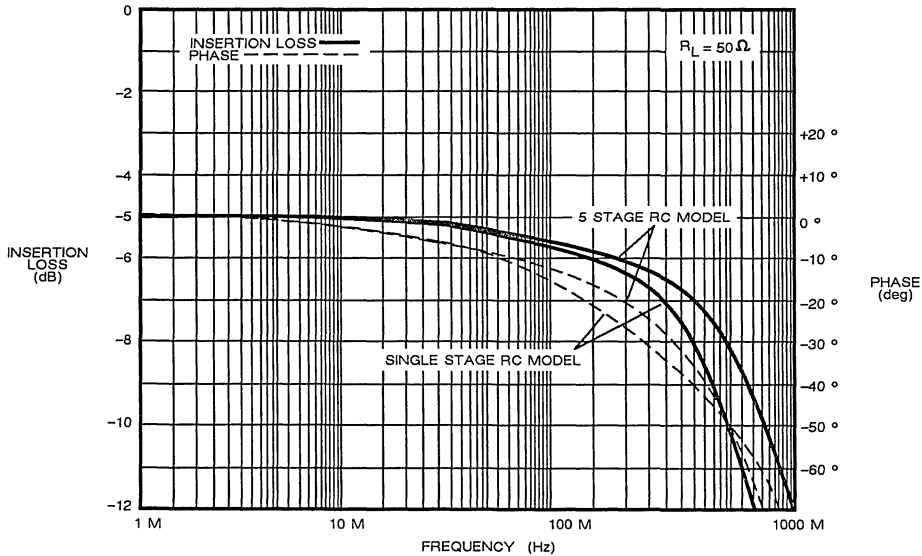


Figure 13. Bandwidth and Phase Response for the Models of Figures 11 and 12

Note that the equivalent five-stage RC circuit shown in Figure 12 is not a complete model of the DG538 transmission path. However, it does illustrate the effect of distributed parameters. An actual model would be far more complex, with other reactive elements that incorporate package capacitances, inductances, etc.

In the absence of a better model, the circuit shown in Figure 12 is useful for predicting bandwidths in

crosspoint systems where the frequency response will be affected by paralleling devices (Figure 14).

A  $10\Omega$  source impedance is included in Figure 14. This source impedance simulates the low-output impedance of a video buffer amplifier generally employed at the input to the matrix. The simulation results of the circuit, using single-stage and five-stage models for different numbers of parallel channels, are shown in Table 2.

Table 2.

Number of Parallel Channels	-3 dB Bandwidth ( $20 \text{ LOG } \frac{V_{OUT}}{V_{IN}}$ )	
	Single R-C Stage (Figure 11)	5 Stage R-C (Figure 12)
1	280 MHz	400 MHz
2	250 MHz	340 MHz
4	225 MHz	260 MHz
8	185 MHz	200 MHz
16	170 MHz	160 MHz

The “flat” response over the bandwidth of interest is an important requirement for video applications. The Independent Television Companies Association (ITCA) specifies the following gain/frequency limits for a video switching matrix.

Mid- to high-frequency response:

$$\pm 0.1 \text{ dB between } 100 \text{ kHz and } 5.5 \text{ MHz}$$

$$\pm 0.25 \text{ dB between } 5.5 \text{ MHz and } 8 \text{ MHz}$$

Above 8 MHz:

“Response shall fall continuously and smoothly”

Although this specification is for 625-line PAL systems used in the United Kingdom, it is a typical specification and similar to other standards, such as NTSC and sequential color and memory (SECAM).

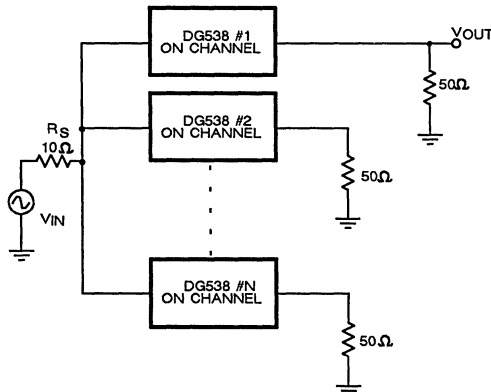


Figure 14. Equivalent Diagram of an 8 X N Crosspoint Using DG538s when one  $V_{IN}$  is selected to All Outputs

High-definition TV has much tighter tolerances since it requires bandwidths to 25 MHz. The 0 to 30 MHz frequency response of the DG538 and DG534, shown in Figure 15, is well within the required limits.

**Group Delay**, sometimes called envelope delay or deviation from linear phase, is the phase-shift rate of change through a circuit or equipment with respect to frequency, or alternatively, non-linearity of the group frequency response. In a transient waveform which has a continuous spectrum, the group delay becomes the transmission time of a packet of spectral components. It follows, therefore, that if the group delay is constant for all the required bandwidth, there will be no difference in the arrival times of the various spectral components which make up the bandwidth.

Because many different frequency components make up a video waveform, this parameter is of particular relevance in video applications. The measured group delay response of the DG538 is shown in Figure 15. It satisfies the most demanding video requirements. The plot shows less than 500 ps over a 30 MHz frequency range.

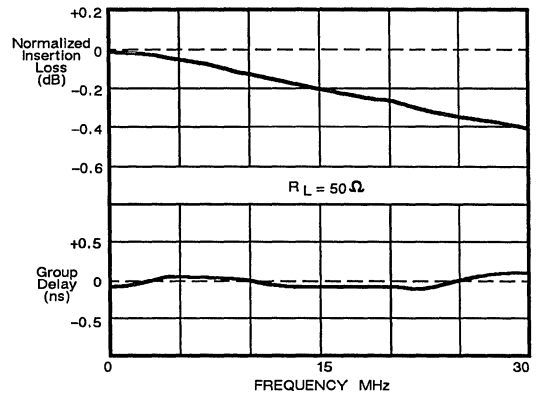


Figure 15. DG538/DG534 Group Delay and Normalized Insertion Loss Response to 30 MHz

## Non-Linearity Distortions

Color video can be divided into two groups: component video [separate red (R), green (G), and blue (B) signals] and composite video, which contains color and brightness (chroma and luma) information in a single waveform.

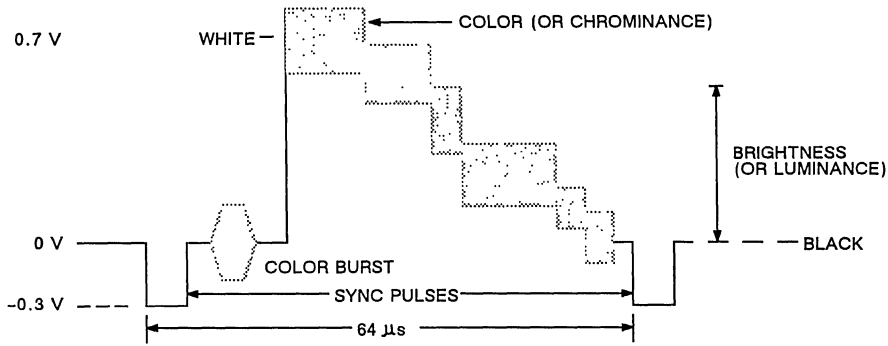


Figure 16. Basic Composite TV Signal

Composite video has various specifications that relate to the interaction of chroma and luma. In particular, differential gain and differential phase must be specified for video components or systems. To illustrate these distortions, consider the basic composite TV signal. Figure 16 shows a typical color TV signal. The sync pulses, occurring every 64  $\mu$ s, synchronize horizontal line deflection. The color signal contains both luminance and chrominance. When this signal is processed by a domestic TV receiver, the red, green, and blue components are recovered and used to modulate three individual electron beams.

The amplitude of the chroma contains the color intensity (color saturation), and its phase difference with respect to the color burst determines the blend (hue) of color.

- Differential Phase.** Measured in degrees, this is the phase shift of the color subcarrier resulting from a change in the amplitude of the associated luminance component. Differential phase shows up in NTSC pictures as a change in hue, a color change more noticeable in a shaded area of the picture.

Frequency related phase shifts (as opposed to differential phase) will cause no change in picture quality since both color burst and chrominance are equally shifted.

- Differential Gain.** Expressed as a percentage, this is a form of distortion resulting from changes in the amplitude of the chrominance signal as a function of luminance amplitude.

The effect on NTSC and PAL pictures is a change in color saturation with changing luminance level. The eye is fairly tolerant to differential gain since the resulting picture changes are fairly subtle. For instance, a brightly colored car traveling from a sunny area of the picture to a shaded area would appear as though its body color intensity had suddenly changed.

Specialized equipment is employed to measure differential phase and gain. Specifications, such as ITCA, require standard test signals and dedicated test equipment and techniques. Recognized standard test waveforms are shown in Figure 17.

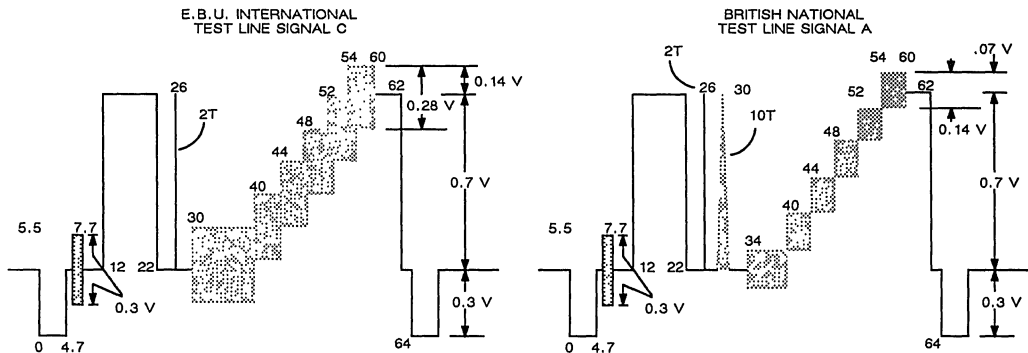


Figure 17. Standard Test Waveforms

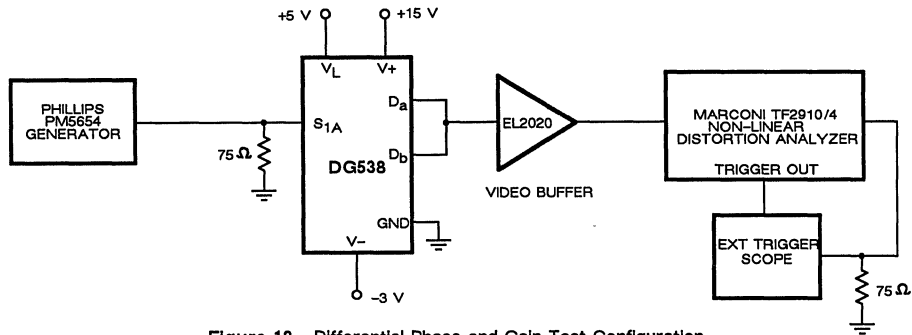


Figure 18. Differential Phase and Gain Test Configuration

Chrominance amplitude variation over the five Average Picture Levels (APLs) indicates differential gain. Differential gain is expressed as the greatest change (in %) of the chrominance amplitude with respect to its amplitude at black level. Similarly, differential phase is the greatest change in chrominance phase shift referred to the phase of the chrominance at black level. Test configuration and equipment used to characterize the DG538 for differential phase and gain are shown in Figure 18.

The equipment shown in Figure 18 must be correctly terminated, or signal amplitudes are affected giving erroneous results. A video buffer (EL2020) provides a 75 Ω resistance to the signal generator, and the signal through the switch meets the standard 1 V<sub>p-p</sub> amplitude. Since most applications use a video buffer following the multiplexer, this configuration is very realistic. The inherent non-linearity of the circuit (bypassing the DG538) is first measured, and then subtracted from the measured value when the device under test is inserted.

## Supply Variation Effects on Non-linearity Distortion

Supply voltage variation causes various transmission impedance changes. Therefore, both differential phase and gain are heavily dependent on power supply values. Figures 19 and 20 show the typical variation of differential phase and gain versus positive and negative supply. These curves enable optimization of performance by careful choice of supplies.

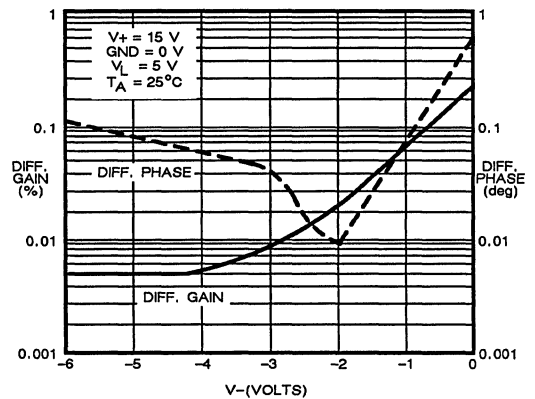


Figure 19. Differential Gain/Phase vs. V-

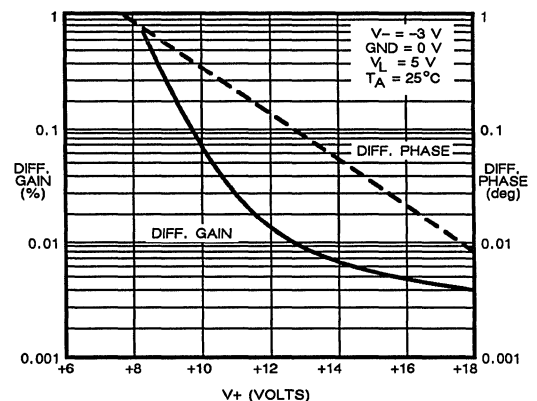
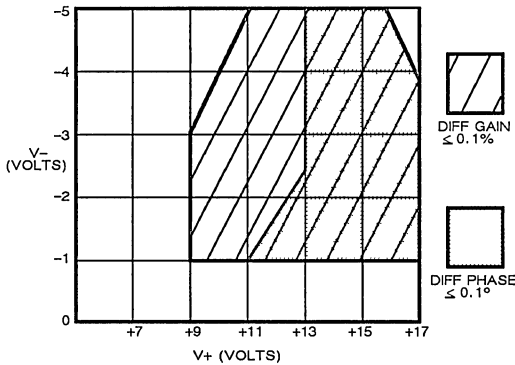


Figure 20. Differential Gain/Phase vs. V+

Generally, high-performance video switching systems require less than 0.5% differential gain and 0.5° differential phase. Therefore, limits of 0.1% and 0.1° could be applied to a single switch component. Figure 21 shows the power supply operating area that achieves < 0.1% and 0.1° performance for DG538 devices.

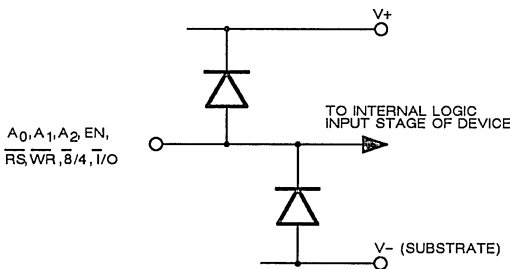


**Figure 21.** DG538 Supply Ranges to Maintain < 0.1% and 0.1° Differential Gain and Phase

**Handling Precautions**

All MOS devices can be damaged by the presence of excessively high electric fields in the gate-oxide region. Such fields can cause the gate oxide to rupture, rendering the device unusable. Mishandling MOS devices may cause catastrophic damage from the build-up of static electricity in the human body, which can reach many thousands of volts.

To reduce electrostatic discharge (ESD) susceptibility in the DG534/DG538, all logic inputs are protected by the circuit shown in Figure 22.



**Figure 22.** ESD Protection Circuit

Typically, the diode clamps provide ESD protection up to 2 kV on any logic input pin. Standard static handling and assembly precautions should, nevertheless, be used to ensure maximum reliability. Anti-static clothing, conductive table-tops, grounded-tip soldering irons, and ensuring that all voltage sources are turned off during the insertion or removal of devices or PCBs are recommended.

**Power-Up Sequence**

A pn junction exists between  $V_L$  and  $V_+$ , which, in the event of  $V_L$  being present before  $V_+$  (i.e.  $V_L > V_+$ ), will become forward biased. Under these conditions, large currents may flow and damage the device. To avoid this condition, the power-up sequence should ensure that  $V_L$  does not come up before  $V_+$ . Normally, this will not present a problem if  $V_+$  and  $V_L$  are derived from the same power supply.

**Printed Circuit Board (PCB) Layout and Decoupling**

Selecting components optimized for high-frequency signals does not guarantee adequate circuit performance. Good layout techniques are also very important. At high frequencies, stray capacitance between long adjacent signal lines can provide low impedance paths that couple with one another. Power supply lines can couple rf signals from one circuit to another. Components or sockets that protrude on a PCB surface may act as small antennas which pick up or radiate rf signals. To avoid these problems, be sure signal paths between components are as short as possible and make extensive use of ground planes and shielding between adjacent signal paths.

The DG534 and DG538 have ground pins isolating adjacent channels. These, when connected to grounded shielding paths, give excellent ac performance.

Power supplies should be bypassed by the use of decoupling capacitors mounted as close to the device supply pins as possible. This is of particular importance for the DG534/DG538 since the device substrate connects directly to  $V_-$ . Two capacitors on each power supply are recommended. A ceramic capacitor of 0.01 to 0.1  $\mu\text{F}$ , provides high-frequency signal bypassing, and a tantalum capacitor (1 to 10  $\mu\text{F}$ ) is adequate to bypass low frequencies. Further decoupling can be achieved by adding a low-value series resistor (e.g. 51  $\Omega$ ) in the supply line.

Components should be assembled on a PCB in a low profile. The DG538, for example, is available as a 28-pin quad surface-mount package or a 28-pin dual-in-line package. The latter has poorer crosstalk performance because it has a larger lead frame and because the device pins are connected through the board. Using sockets should be avoided because they degrade device performance significantly.

## Applications

Applications for the DG538 and DG534 are many and varied, ranging from high-frequency signal switching to lower-frequency, low-level signal routing.

## Video Systems

The DG534 and DG538 multiplexers are ideal for many wideband switching applications, such as high-resolution financial data networks, forward-looking in-

frared (FLIR) detectors (night vision systems), CAT (computer aided tomography) scanners, and NMR (nuclear magnetic resonance) medical imaging.

Figure 23 shows the DG538 as an 8-to-1 video source selector. This circuit has many applications in industrial process monitoring systems or in security systems where eight separate video cameras connect to a single monitor in a sequence. The circuit uses three bits to automatically select each source in turn. An override feature can be incorporated to disable the counter and provide manual channel selection.

An example of a differential configuration application is shown in Figure 24. This circuit may be used in component video systems such as TV camera signal routing. Two devices are required for routing four separate RGB sources and their corresponding audio, sync, or timecode signals. Note that the channel select or address bus is common to all devices.

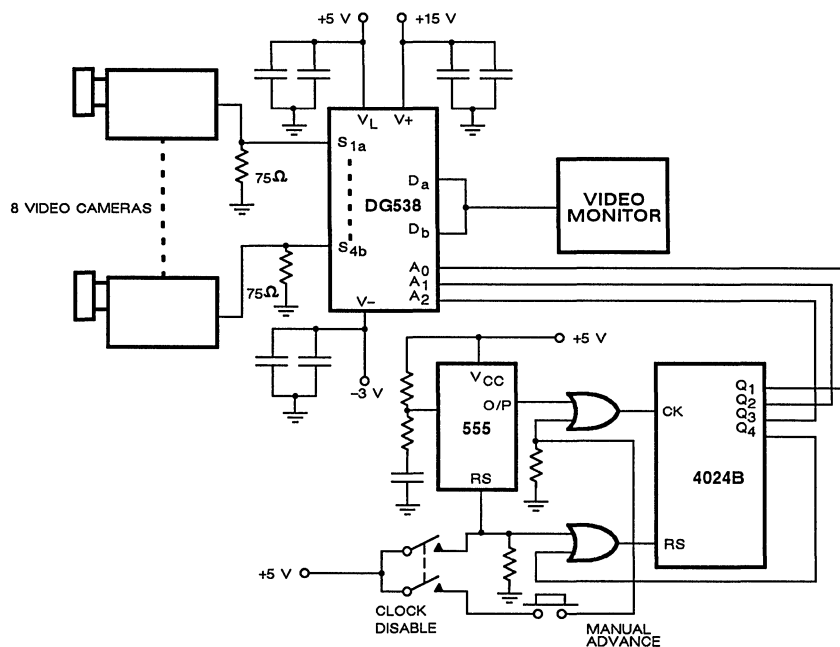
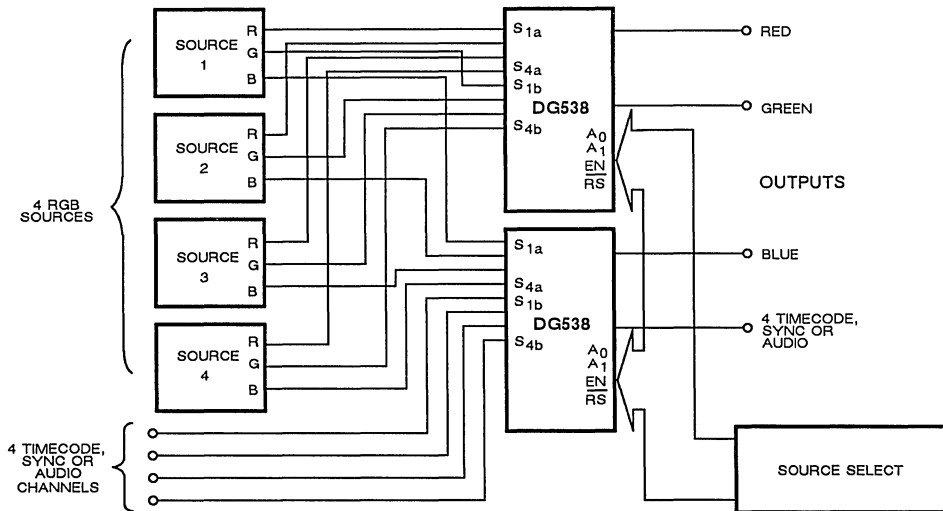


Figure 23. Basic Closed-Circuit TV System



**Figure 24.** An RGB Plus Timecode, Sync, 2 Audio Switching System

A majority of video applications require crosspoint configurations, where a number of inputs must be switched to a number of outputs. Applications requiring this type of matrix switching (both analog and digital) range from PCM (Pulse Code Modulation) or telecommunications data switching to financial information routing. A basic crosspoint configuration (8 x 4) is shown in Figure 25. The data-write control strobes address information to each DG538. In turn, the actual address data (for the required route) is present on the address or route-assign bus. Video output buffers are normally used to drive lengths of 75  $\Omega$  coax cable.

In Figure 25, the loading of switch capacitances and

buffer input impedances on a given video source will vary, depending on the number of outputs. For example, when a single source is switched to all four outputs, it is loaded by  $4 \times C_{S(ON)}$  ( $\sim 92$  pF) plus  $4 \times C_{in}$  of buffer. This increased loading affects the frequency response and phase shift of the output signal.

Figure 26 illustrates this effect by showing the frequency response of a single output signal for an increasing number of channels connected to the source. Additional channels (2, 3, and 4) are loaded with 10 k $\Omega$  to simulate the input impedance of video buffers.

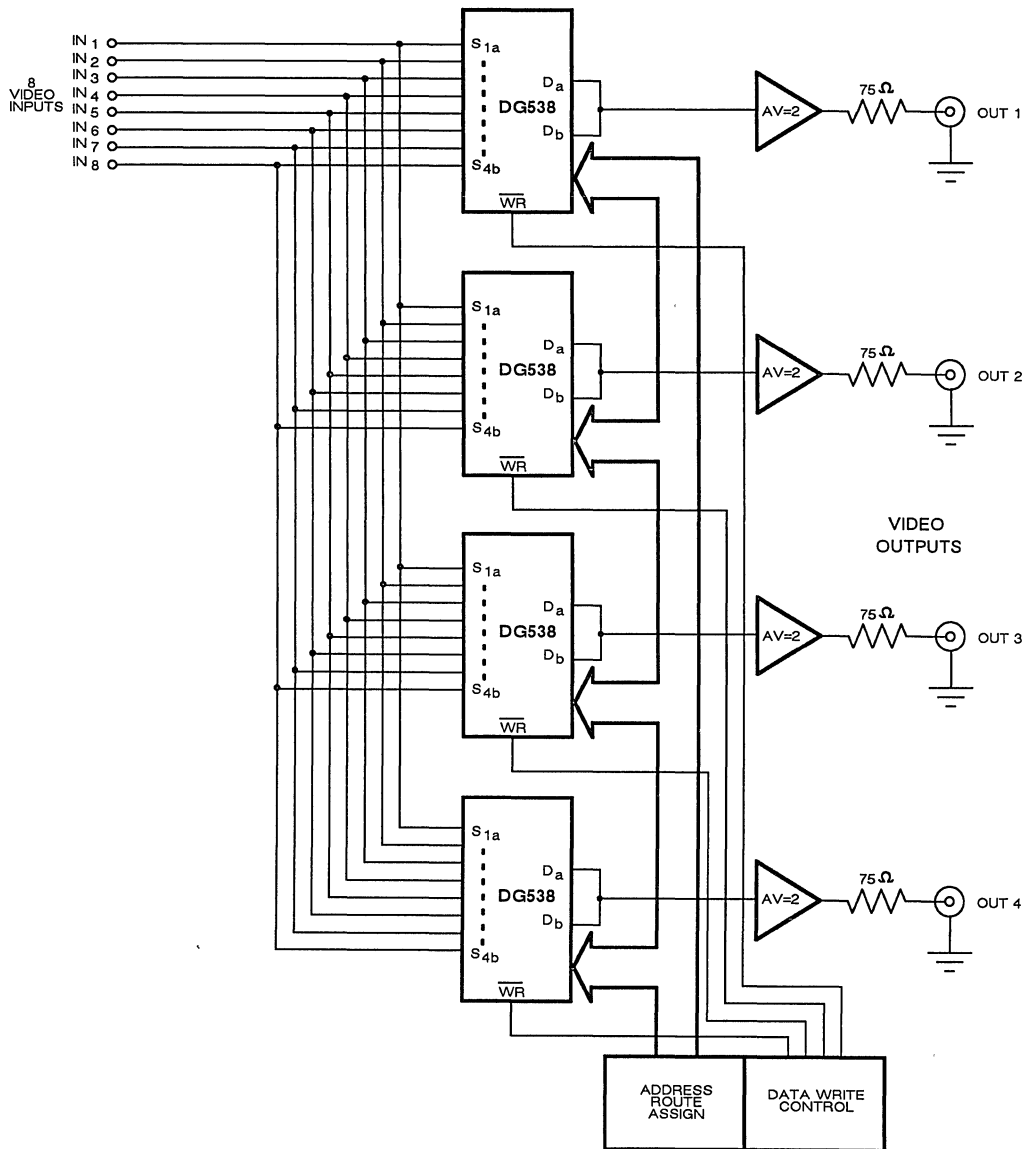


Figure 25. An 8 X 4 Crosspoint Switch



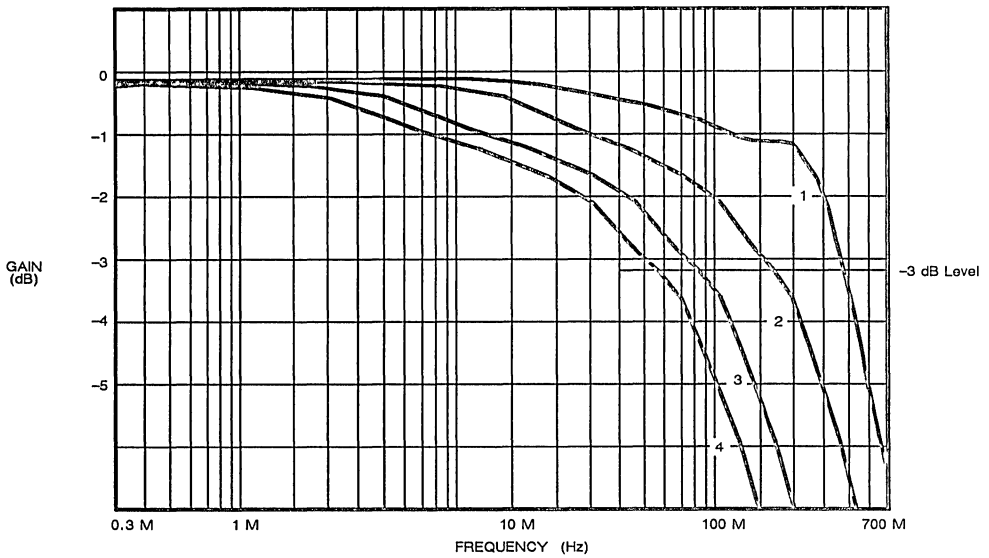


Figure 26. Frequency Response of 8 X 4 Matrix

Figure 27 shows the measured frequency response of any of four DG538s connected to a common signal source. In this circuit, an EL2020 wideband op amp (with its input resistance padded down to 1 k $\Omega$  to improve switch bandwidth) was used as a buffer. The dotted line shows the frequency characteristics of the EL2020 alone. The gain response meets the  $\pm 0.1$  MHz to 5.5 MHz requirement of ITCA systems.

Better performance can be achieved using an improved video buffer, such as an OPA633.

If an increased number of outputs is required, input buffers may be used to avoid performance degradation below tolerable limits. Thus, to maintain the performance shown in Figure 27, no more than four DG538s should be connected to a given input buffer.

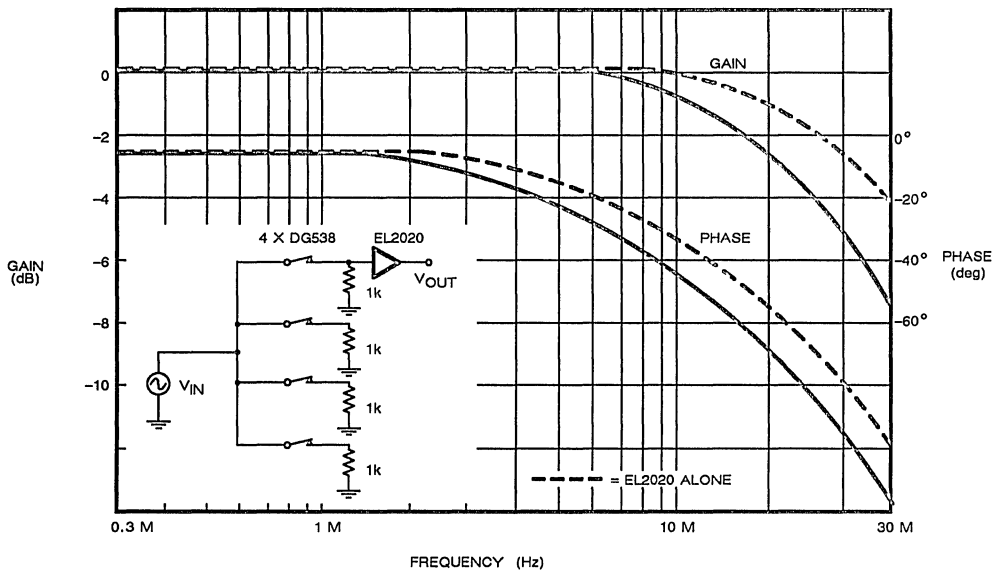


Figure 27. Frequency Response of Four DG538s Buffered with EL2020s

Since each input buffer drives only four switch impedances and their corresponding output buffer input impedances, no major output power is required (unlike the output buffers which must drive up to 2 V into each 75 Ω cable). Therefore, it is sufficient to employ inexpensive and simple discrete buffers, such as source or emitter follower circuits that require only a transistor (FET or bipolar) plus a resistor. Because simple input buffer designs (Figures 28 and 29) are inexpensive, they are feasible for buffering every input in demanding, high-definition applications.

Some applications might demand a dc-coupled system that retains all the dc contents of the signal applied to the buffer. For these applications, the follower circuit shown in Figure 29 may be used. This circuit, which exhibits a low dc offset of <40 mV, uses a Siliconix U440 dual FET to maintain simplicity and efficient use of board space. Lower offsets can be accomplished by using a dual FET with better matching characteristics (e.g., U232).

In the circuit shown in Figure 28,  $f_{-3dB} \approx 300$  MHz for  $R_{gen} = 75 \Omega$ , while offering a low input capacitance. The output signal for this circuit has some dc offset; however, this is not usually a problem because the output of the matrix is frequently ac coupled with a dc restoration (black-level clamp) circuit employed at a later stage. Figure 30 shows a simple black-level clamp circuit that employs a DG271 high-speed analog switch.

Figure 31 shows a large 32 x 4 crosspoint matrix. It is frequently better, in terms of system flexibility, to use a smaller crosspoint card (e.g., 8 x 4) as the basic building block. This 8 x 4 card must be designed to allow expansion of the total number of inputs or outputs required by the system.

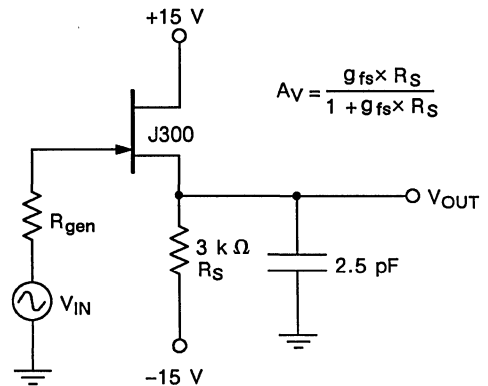


Figure 28. Single FET Source Follower

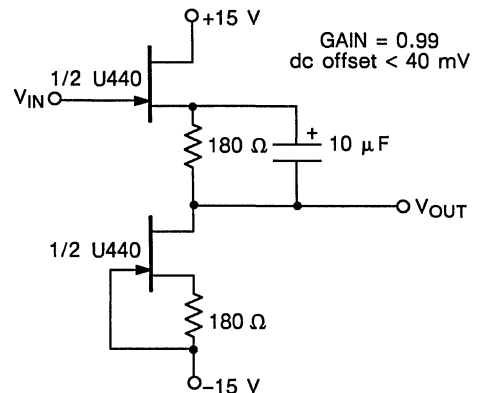


Figure 29. FET Buffer Uses Matched JFETs for Low DC Offset

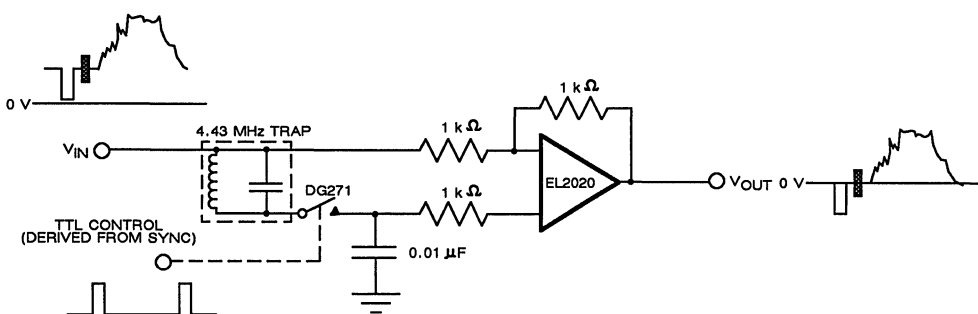


Figure 30. Simple Black-Level Clamp Circuit

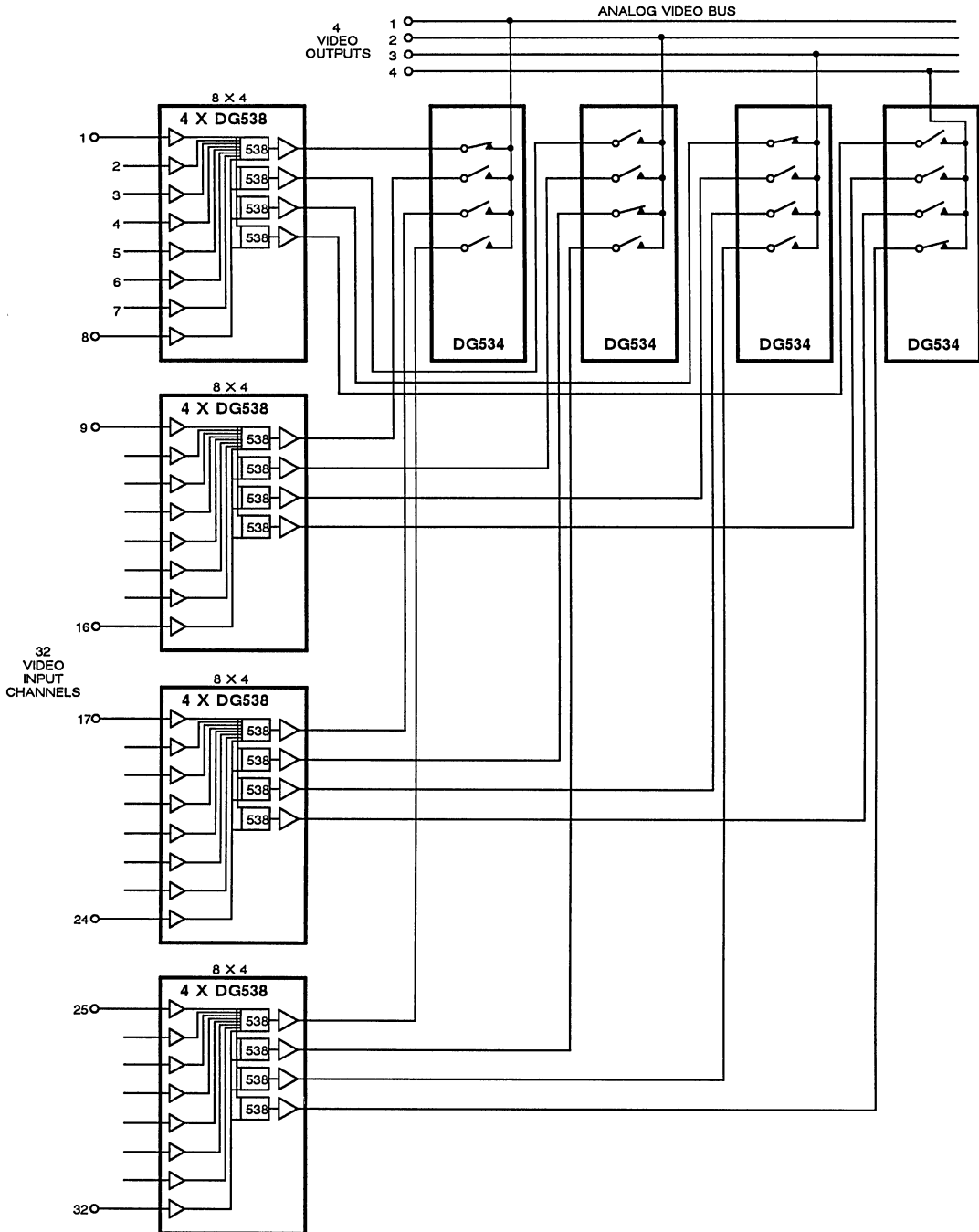


Figure 31. 32 X 4 Crosspoint with Bus Isolation

Assuming each card has eight input buffers and four output buffers as shown, expansion of system outputs is easily accomplished by paralleling the inputs to the switch cards. Since each card has all its inputs buffered, many cards may be connected to provide multiple outputs without producing significant loading on the signal sources. However, expanding the number of system inputs is more difficult. Each card output has a low-impedance video buffer that prevents simple paralleling, which would greatly overload the analog video bus. By using DG534 devices in a 4-to-1 mode as a submultiplexing configuration, as shown in Figure 35, each line of the video bus sees only one card output at a time.

Figure 32 shows a method for transmitting dc power down the video coax. This system can be adopted in remote switching locations where a power source is

not available or in hazardous industrial environments where mains-derived power supplies are not permitted. Alternatively, this technique could be adopted in a cable TV application, where the channel switcher or selector could be powered from the incoming video lines. The dc power is coupled to the video coax lines using a 1 mH choke, and it is isolated or removed from the video signal using the capacitors (C1, C2, and C3).

Another popular video-signal manipulation application is digitally controlled gain or attenuation circuits. For example, digitally controlled gain may be required for level trimming different video channels to be switched to a single processing path.

Figure 33 shows a DG538 in a dual 4-by-1 arrangement designed to switch four video sources while providing level compensation and/or gain for each.

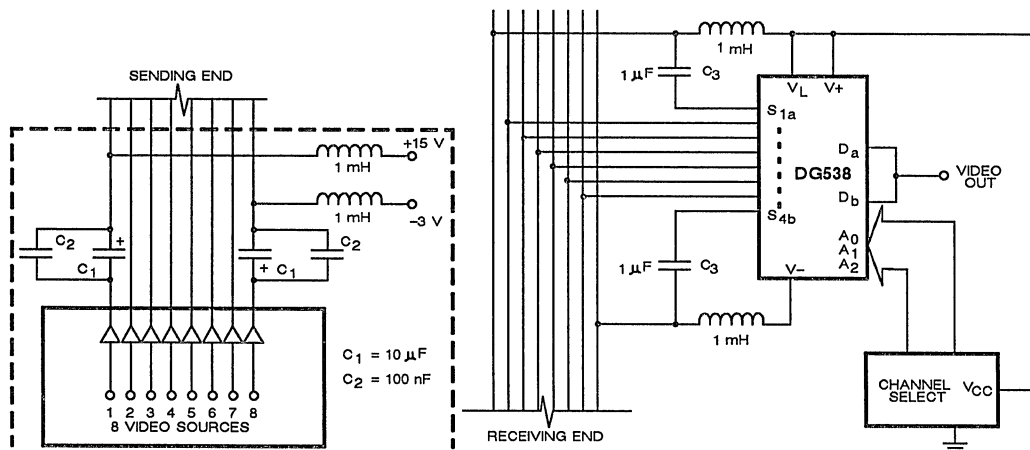


Figure 32. Phantom-Powered Remote Video Switch

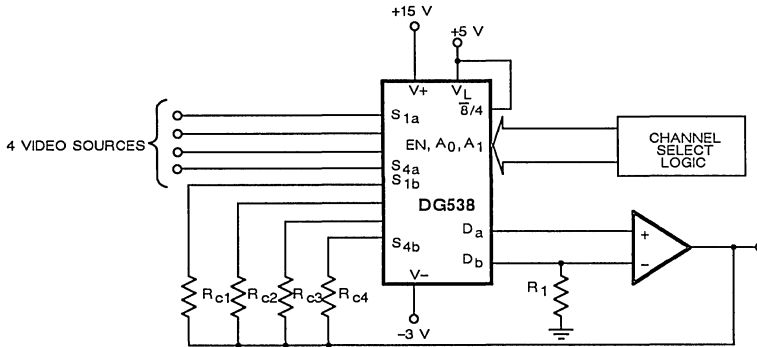


Figure 33. Programmable Gain Video Selector

**Data Acquisition Front-End Applications**

A typical data acquisition system comprises front-end sensor stages followed by signal conditioning stages. The analog sensor signal, after being amplified and filtered, is sampled and digitized using a sample-and-hold circuit and an analog-to-digital converter. The digitized signal is then processed, usually under microprocessor control.

Usually, many analog channels must be processed. Due to the high cost of signal-conditioning, fast sam-

ple-and-hold, and flash analog-to-digital converter components, it is more feasible to employ a front-end multiplexer so that each channel can be processed in turn.

The circuit shown in Figure 34 uses a wideband multiplexer for accurate manipulation of the high-frequency input signals. The "user friendly" control and microprocessor-interface features of the DG538, combined with its proven high-frequency signal handling, make it ideal for this circuit.

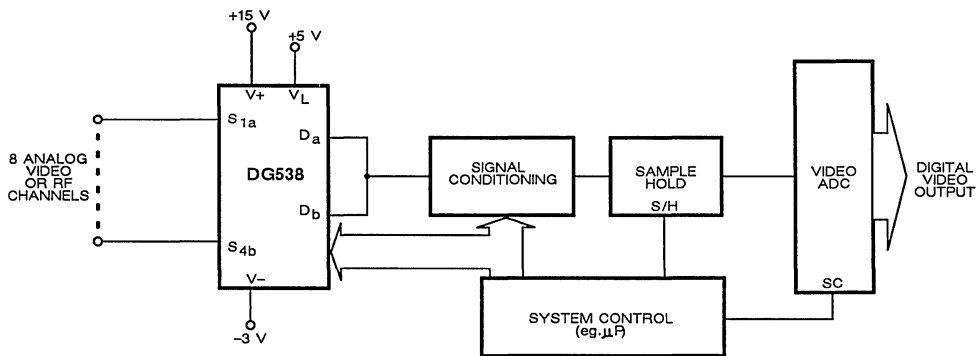


Figure 34. A Basic Multichannel Video/rf Processing Circuit

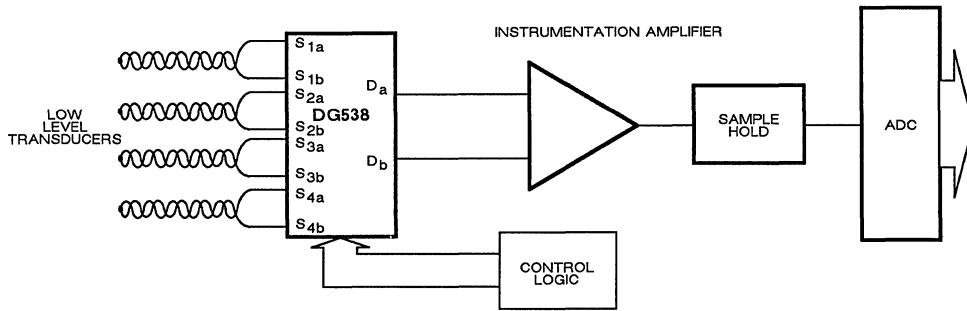


Figure 35. A High-Accuracy Low-Level Signal Processing System

The DG534 and DG538 are also effective devices for switching low-level signals. Commonly, data acquisition systems monitor a number of sensor signals that could be the output of various temperature, pressure, or vibration transducers. Generally, these are low-frequency (often dc), low-level signals. Thermocouples, for example, typically have millivolt outputs with tens of  $\mu\text{V}/^\circ\text{C}$  resolution. To accurately monitor small temperature changes, the multiplexer must not introduce any dc offset or noise. Since the circuitry must handle small signal levels that are prone to noise/mains pickup, digital crosstalk, etc., apply the same layout rules used for high-frequency designs, such as sufficient grounding and shielding.

The DG538, with its interchannel ground pin and symmetrical on-chip layout, improves circuit accuracy. A differential signal handling system is an established means of low-level transducer interfacing. This system rejects noise pickup, switching transients, and metallic junction dc offsets as common-mode signals. A highly accurate low-level transducer interface circuit using a DG538 in its differential mode is shown in Figure 35.

### Data Acquisition System Signal Conditioning

Before sampling and digitizing, an analog signal frequently requires "cleaning up" and ranging, a process known as signal conditioning. System front ends will invariably pick up unwanted signals. Signal carry-

ing leads often pass areas that superimpose mains hum, radio-frequency interference, or digital noise on the analog signal to be processed. A well-designed and balanced differential twisted-pair system, such as the one illustrated in Figure 35, will minimize these common-mode signals.

### Filtering

Filter circuits are widely used in the signal conditioning stage. Most often, they take the form of low-pass, high-pass, or band-pass configurations that remove unwanted signals outside the required bandwidth. Figure 36 shows a general configuration for an active first-order all-pass circuit that can be used for providing a digitally controlled variable-phase shift, where the phase shift is given by

$$\beta(\omega) = 2 \tan^{-1} \omega RC$$

and the delay is found from  $t_d = \frac{2 RC}{(\omega RC)^2 + 1}$

Note:  $-\omega C = 1/RC =$  cut-off frequency. For constant delay,  $\omega < 0.1 RC$ .

The circuit shown in Figure 36 may be employed as a phase correction system to equalize phase delays associated with different signal paths. A video crosspoint, for example, will exhibit a varying phase delay due to changing load capacitance on the transmission path when a single input connects to between 1 and n outputs (Figure 25).

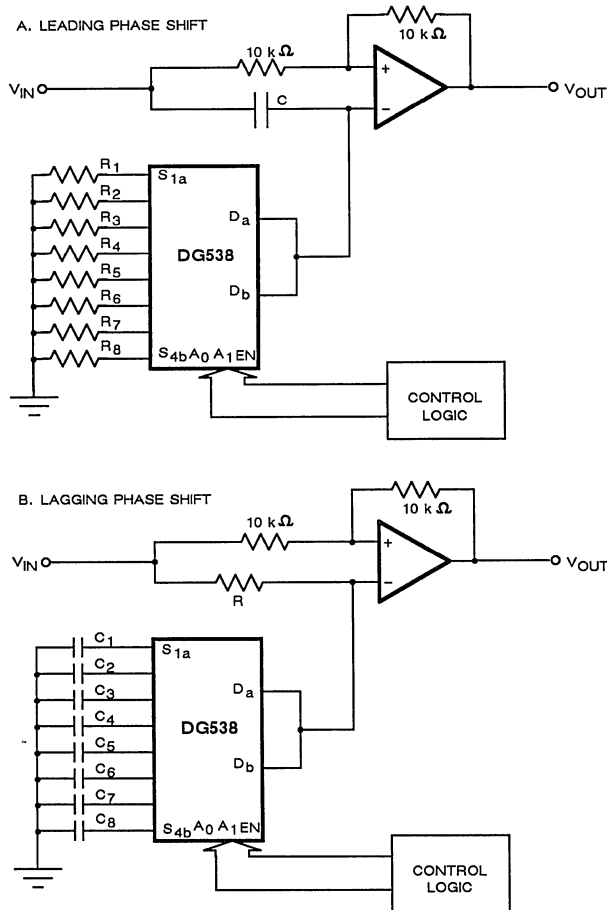


Figure 36. A Digitally Controlled Phase Shifter

**Conclusion**

This application note has provided information for video, audio, and data acquisition switching system

designers. Using the DG534 and DG538 microprocessor-compatible multiplexers from Siliconix simplifies the design task and improves system performance.

# APPLICATIONS FOR THE D469 A HIGH CURRENT POWER DRIVER

James A. Harnden  
January 1988

## INTRODUCTION

Many applications operate MOSPOWER devices as ON/OFF switches. In applications where device switching speed is of less concern and the MOSPOWER device's gate capacitance ( $C_{ISS}$ ) is sufficiently low, they may be driven directly by logic devices such as CMOS or TTL with a pull-up resistor. The prime advantages that encourage use of MOSPOWER devices over bipolar transistors however, is the efficiency gained from reduced  $r_{DS(ON)}$  voltage drop and increased switching speeds. The gate of a MOSPOWER device is capacitive ( $C_{ISS}$ ). The value of  $C_{ISS}$  is directly related to the device's size and switching speed is directly proportional to the gate driver's output impedance (R/C). To take advantage of the increased switching speed of larger MOSPOWER devices, a more robust driver than simple logic devices is required.

The D469 was designed as an optimized driver for MOSPOWER devices. It contains four independent

drive channels, and each channel can be configured as a logically inverting or non-inverting driver. Since the D469 is a CMOS device it is compatible with low power CMOS logic and microprocessors and draws minimal quiescent current (2.5 mA). The D469 switching times (typically 25 ns) are specified with a 500 pF load, but higher capacitive loads may be driven at the penalty of proportionally increased transition times. Output impedance of the D469 (both pull-up and pull-down) is typically less than  $8 \Omega$ , permitting peak (transient) charging currents of approximately 1.2 amps (at low duty-cycles).

## Applications Of The D469 Quad Driver

The D469 quad driver is well suited to applications such as motor drives. Motors ranging from fractional to integral horsepower can be driven directly with MOSPOWER devices. The D469 provides optimized gate drive signals and simplifies interface to the logic level control circuitry.

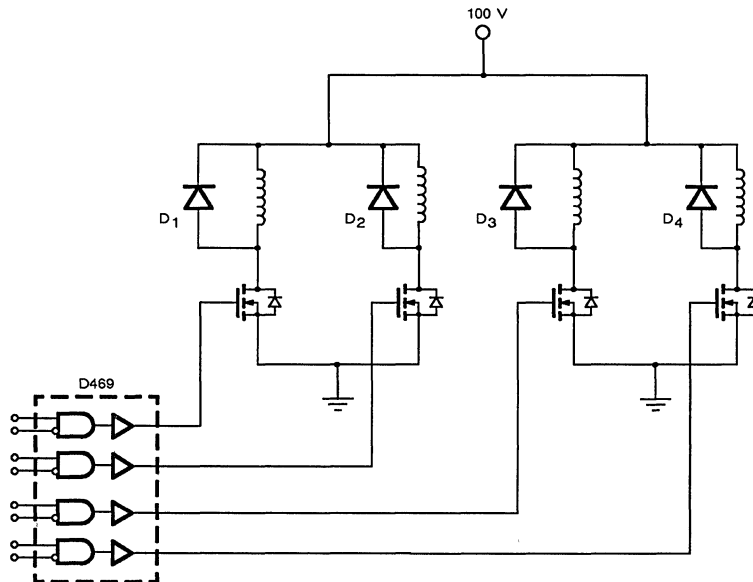


Figure 1. Unipolar MOSPOWER Stepper Motor Drive



Figure 1 illustrates a "unipolar" configuration widely used in stepper motor drives. In this application the MOSPOWER devices are operated as "low side" switches with their sources, and the D469 gate driver, referenced directly to ground. Diodes  $D_1 - D_4$  protect the MOSPOWER devices from overvoltage as a result of flyback voltage generated by the motor winding when a MOSPOWER device is turned off.

MOSPOWER devices offer distinct advantages in low-voltage motor drive applications. Mobile, battery powered applications such as automotive, aircraft, boats, satellites, missiles and mobile robotics are improved by the efficiency of MOSPOWER devices. Power consumed during transition decreases motor performance and increases heat that must be dissipated. New low ON resistance MOSPOWER geometries increase current handling capability for a given heat sink or decrease heat sink requirements at any given current level. Using an efficient gate driver like the D469 can further increase efficiency by minimizing quiescent current and transition times as well as providing sufficient gate voltage to minimize the MOSPOWER devices  $r_{DS(ON)}$  voltage drop.

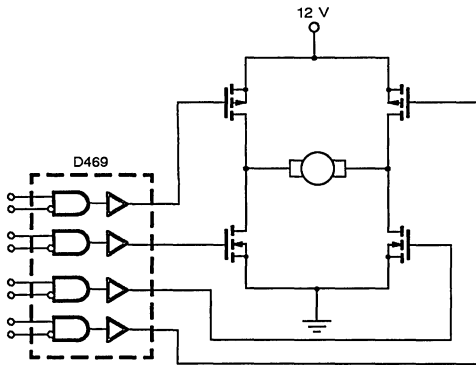


Figure 2. Low-voltage Complementary MOSPOWER H-bridge

In figure 2 a low voltage H-bridge configuration is demonstrated which provides the motor with bi-directional (bipolar) current drive capability. This arrangement works particularly well in applications that use a single 12 volt battery to power the motor and electronics. By using N-channel MOSPOWER devices as "low-side" switches (sources referenced to ground) and P-channel MOSPOWER devices as "high-side" switches (sources referenced to the battery voltage) the gates of all four devices can be driven directly by one D469 quad MOSPOWER driver.

P-channel MOSPOWER devices are now available with breakdown voltages up to 500 V. As figure 3 illustrates, driving the gates of P-channel high-side devices in a high voltage bridge is slightly more complex than the previous low voltage applications, but still considerably less complex than when n-channel high-side switches are used. Although P-channel devices typically cost more than N-channel devices for a given  $r_{DS(ON)}$  rating, the added device cost is often offset by the inexpensive gate-drive circuitry.

In figure 3 a depletion mode device is used as a series linear regulator to create a power supply 12 V below the bridge power supply, to power the D469 MOSPOWER gate driver. Current through the series regulator can be calculated based on the average current needed to drive the total gate capacitance at the percentage of the total duty cycle, plus the quiescent current of the D469. Capacitor  $C_1$  supplies the peak current needed for transient (gate drive) conditions.

One particular advantage inherent to this drive technique is that it holds the P-channel upper devices "normally OFF". Absence of a gate drive signal results in the gate-source of  $Q_1$  clamped in a safe (low impedance) state. This gate drive technique provides a safe "power-up" condition, as well as additional failure protection should the low supply voltage be interrupted during operation.

### The "All N-Channel" Half-Bridge

Bridges using N-channel devices in both the upper and lower switch locations always offer advantages when pushing the "state-of-the-art". The lowest  $r_{DS(ON)}$  and highest breakdown voltage MOSPOWER devices in the marketplace will always be N-channel. N-channel material offers more than twice the current-carrying efficiency (carrier mobility) of P-channel material, per unit area. A P-channel device of comparable current, voltage, and  $r_{DS(ON)}$  ratings, constructed with comparable cell density, will be more than twice the die area of its N-channel complement.

Using N-channel devices in the upper quadrants of the H-bridge complicates gate drive. The gate of the N-channel device must be 10 to 12 V positive (with reference to its source) to turn the device fully ON. In a half-bridge, the high-side N-channel device's source may be at any voltage between a diode

drop below ground and a diode drop above the motor drive voltage. To drive the gate properly, a separate voltage must be generated that is referenced to the high-side N-channel device's source and capable of going at least 10 volts above the motor voltage.

In Figure 4, a JFET ( $Q_3$ ) is used to provide the P-channel power MOSFET with low gate-source impedance when turned OFF. The J107 has an  $r_{DS(ON)}$  rat-

ing of less than  $10 \Omega$  when the gate-source voltage is less than 4.0 V (minimum cutoff-voltage). Zener diode  $D_1$  protects the P-channel power MOSFET gate-source from excessive voltage. Zener diode  $D_3$  protects the gate-source of JFET  $Q_3$  from excessive voltage when  $Q_4/Q_5$  are ON. The CR100 ( $D_2$ ) is a constant-current (1.0 mA) diode used to turn the JFET ( $Q_3$ ) ON when  $Q_5$  is turned OFF.

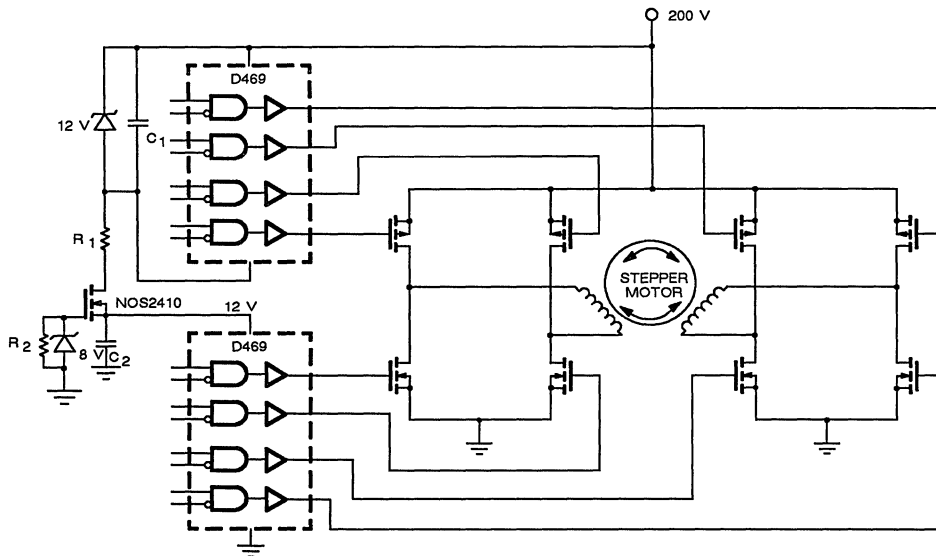


Figure 3. High-Voltage Complementary MOSPOWER H-bridge

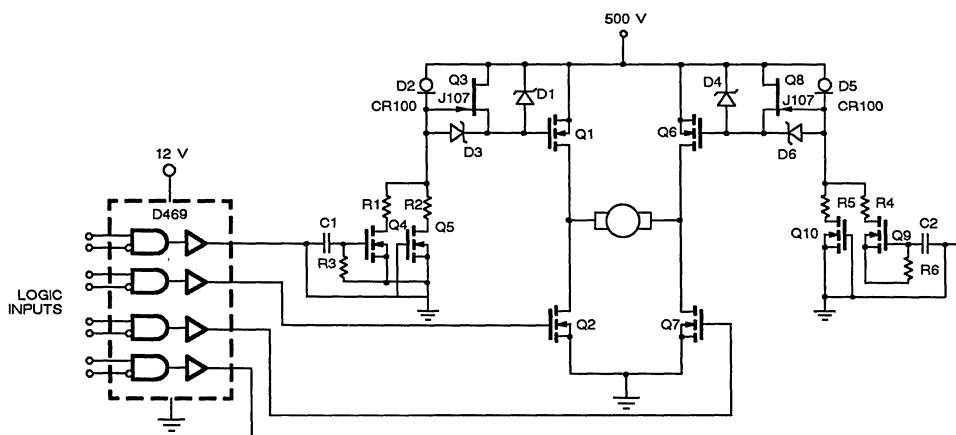


Figure 4. "JFET Clamp" for High-side P-Channel Gate Drive

$Q_4$ ,  $Q_5$ ,  $R_1$ ,  $R_2$ ,  $R_3$  and  $C_1$  form a bi-level current source used to drive the JFET clamp ( $Q_3$ ) and upper P-channel power MOSFET ( $Q_1$ ). When  $Q_4$  and  $Q_5$  are driven on by the preceding logic, they initially source current at a level set by  $R_1$  and  $R_2$ . The gate  $D_3$  drives the P-channel gate to a voltage level clamped by diode  $D_1$ , turning the power MOSFET ( $Q_1$ ) ON. After the power MOSFET is turned ON the current source value is reduced by approximately an order or magnitude to maintain the power MOSFET's enhancement voltage. Peak current timing is set by the time constant of  $R_3$  and  $C_1$  and the maintenance current level is set by the value of  $R_2$ .

When the current source driver is turned OFF, constant current diode  $D_2$  pulls the gate of JFET  $Q_3$  to the high voltage rail, turning  $Q_1$  OFF. The P-channel devices gate is driven OFF at essentially the same rate as the rise of  $Q_3$ 's gate, and held securely OFF by the low impedance of  $Q_3$ . JFETs (or N-channel depletion mode power MOSFETs which could also be used in this circuit) can easily provide ON resistance low enough to prevent transients on the MOSFET's drain (dv/dt) from generating enough voltage at the gate to allow spurious turn-ON.

In Figure 5, a high frequency oscillator (100 kHz) and a small bi-filar wound pulse transformer are used to form floating 12 V power supplies, referenced to the source of each upper N-channel device. The value of supply capacitors  $C_1$  and  $C_2$  are chosen based on capacitance values of the N-channel gates being driven, the duty-cycle and the quiescent current of

the floating opto-coupler buffer and emitter follower output buffer stage. Diodes  $D_1$  and  $D_2$  are added to protect the power MOSFETs gate from overvoltage conditions. An opto-coupler is used to isolate gate drive signals, and the emitter follower output stage provides low impedance gate drive.

The high-side drive configuration in Figure 5 allows "static" operation. The high-side N-channel devices can be held ON in a steady-state condition, providing a switching range from dc to the maximum bridge operating frequency. The oscillator operates continuously to provide power for the two floating gate-drive supplies. In this arrangement, the pulse transformer can be driven at a much higher frequency than the modulation frequency, making the transformer smaller and less critical than in configurations that drive the gate directly through a pulse transformer.

A dynamic "bootstrap" gate drive isolation technique is demonstrated in Figure 6. Dynamic isolation is compatible with several styles of motor drive and current control that result in continuous modulation. If dynamic gate drive techniques can be applied they often result in reduced cost by eliminating high cost items such as high performance opto-isolators. This configuration of isolation has one other inherent feature when compared to the floating power supply technique discussed previously. When the upper MOSPOWER device is turned OFF, its gate is clamped to the source (by low-impedance P-channel device  $Q_2$ ) to prevent spurious dv/dt turn-ON (See Siliconix MOSPOWER Applications Handbook – dv<sub>DS</sub>/dt Turn-ON in MOSFETs).

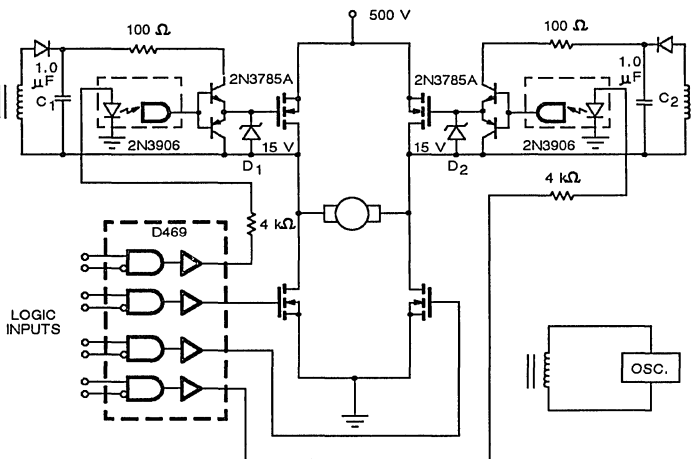


Figure 5. All N-channel Bridge with Opto-Coupled Logic Signal

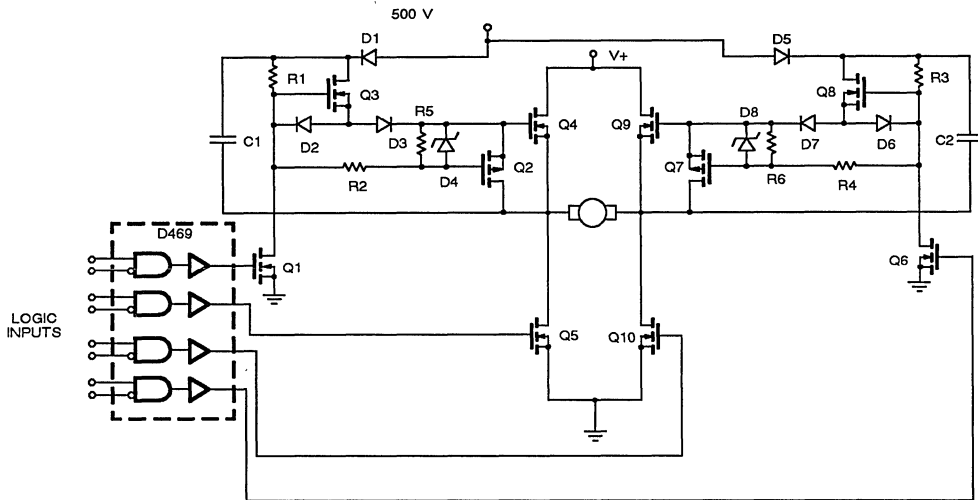


Figure 6. Bootstrap High-side N-channel Gate Drive Isolation

In operation, when  $Q_1$  is turned ON, the P-channel clamp ( $Q_2$ ) assures the gate-source of  $Q_4$  remains shorted. While  $Q_1$  is ON,  $Q_5$  (the lower output MOSPOWER device) will be turned ON. The bootstrap capacitor is then charged from the low-voltage supply, via  $D_1$  and  $Q_5$ . When  $Q_1$  is turned OFF,  $Q_2$  is also turned OFF releasing the clamp across  $Q_4$ 's gate-source.  $R_1$  is allowed to pull the gate of  $Q_3$  high, turning it ON. This switches current into the capacitive gate of  $Q_4$ , via  $D_1$ ,  $Q_3$  and  $D_3$ . As  $Q_4$  begins to turn ON, voltage at the source begins to rise toward the positive motor drive voltage. As it rises it carries with it the reference (low) end of the bootstrap capacitor.  $D_1$  (which has to be a fast recovery diode) reverses, protecting the bootstrap capacitor's charge. Above this point, remaining gate charge must be supplied by the bootstrap capacitor, which must be at least an order of magnitude larger than the MOSPOWER gate capacitance ( $Q_4$ ) being driven. When the upper MOSPOWER device ( $Q_4$ ) is fully enhanced, the source will be an  $r_{DS(ON)}$  drop below the motor drive voltage and its source will be held at the voltage potential remaining in the bootstrap capacitor, minus voltage drops of  $Q_3$  and  $D_3$ . The leakage current of MOSPOWER device ( $Q_4$ ) will limit the amount of time a high level can be maintained without allowing the stored capacitor voltage to "droop"

to a dangerous voltage level. As a general rule, 8 volts is a reasonable (absolute minimum) gate drive voltage droop to allow. With less than 8 volts of gate drive, the  $r_{DS(ON)}$  of  $Q_4$  will increase rapidly, increasing power dissipation and motor drive voltage losses.

## Summary

Designing a power MOSFET bridge for a motor drive application requires, as with any power circuit, an understanding of economic and performance requirements. Both design requirements will impact the selection of an "optimized" gate drive technique for the MOSPOWER devices. Some methods of isolating the high-side gate drive are advantageous at low voltages but become inefficient or otherwise unsatisfactory at higher voltages. Other isolation techniques work well over a wide range of voltages but are less economical. Still others provide economic advantages but are incompatible with the controller's modulation scheme. Each isolated high-side gate drive technique will be well suited to a range of applications and less than the optimum choice in others. As demonstrated in this applications note, most of these gate drive circuits can benefit from a flexible and economical integrated circuit such as the D469 CMOS quad driver.

# IMPROVE SYSTEM PRECISION WITH THE SI7652 CHOPPER-STABILIZED OPERATIONAL AMPLIFIER

By Carl Jones and Steve Moore  
June 1987

## Conventional Op Amp Limitations

The performance of standard operational amplifier circuits is significantly limited when operating with low-level dc signals. These limitations are caused by the relatively large voltage and current offsets of conventional op amps. The most significant source of error is the input offset voltage,  $V_{OS}$ . Even a low-offset op amp, such as the OP-05, has a typical  $V_{OS}$  of  $70 \mu\text{V}$ . This offset voltage produces an output error of  $70 \text{ mV}$  with a circuit gain of 1000. To reduce this error, most standard op amps offer offset nulling terminals. Offset nulling is accomplished by connecting a potentiometer across the nulling terminals and trimming the offset to an acceptable value. This procedure is time consuming and expensive because the potentiometer for each op amp must be individually adjusted.

Another problem associated with op amps operating with dc signals is offset drift. Because  $V_{OS}$  drifts over time, the potentiometers must be periodically re-adjusted. This re-adjustment is both expensive and inconvenient, especially with remotely located circuits.  $V_{OS}$  also drifts with changes in temperature, and in some cases, the drift can be hundreds of  $\mu\text{V}/^\circ\text{C}$ . This temperature drift is a major limitation when amplifying low-level dc signals in an unstable temperature environment.

In addition to the input offset voltage, there are also offset currents which induce errors at the output. The difference in these currents is called the input offset current ( $I_{OS}$ ) and the mean  $I_{OS}$  value is called the input bias current ( $I_B$ ). The output offset caused by these small currents depends on the feedback elements and input drive impedance. Figures 1 and 2 show the relationship between the previously discussed input offsets, the feedback network, and the resulting output errors.

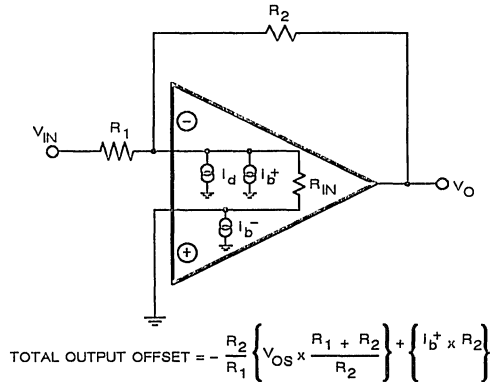


Figure 1. An Operational Amplifier in an Inverting Configuration - Equivalent Circuit

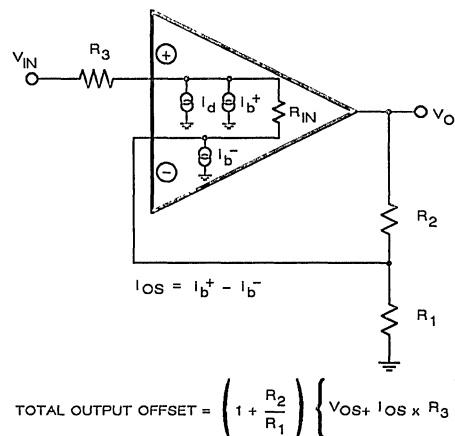


Figure 2. An Operational Amplifier in a Non-Inverting Configuration - Equivalent Circuit

## The Si7652 Solution for Precision Performance

The Si7652 is designed specifically for low-level dc applications. With a maximum input offset voltage of  $5 \mu\text{V}$  ( $0.7 \mu\text{V}$  typical), the Si7652 offers designers dramatically improved input resolution. Also, both the temperature and the time drifts in  $V_{OS}$  are virtually eliminated. Thus, the external trim potentiometer and the costly and inconvenient periodic adjustments are unnecessary.

To achieve these performance features, the Si7652 utilizes a differential "chopper-stabilized" approach. However, unlike previous chopper amplifiers, the main amplifier is always connected to the output of the device. This allows the Si7652 to operate without the large output glitches that occur with traditional chopper amplifier designs. Careful design of the switching circuitry has minimized the charge injection errors that are normally associated with chopper designs. The design used for the Si7652 has excellent common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) ratings, which are both typically 130 dB.

Built with the Siliconix PolyMOS process, the MOSFET input devices of the Si7652 require extremely low bias currents and have low input offset currents, thereby minimizing another potential source of error. Additionally, the Si7652 has extremely low noise. The input  $1/f$  noise (low frequency) is typically less than  $0.2 \mu\text{V}$  (p-p). The input noise current is a negligible  $0.01 \text{ pA}/\sqrt{\text{Hz}}$ .

Another valuable feature of the Si7652 is its very high open-loop voltage gain ( $A_{VOL}$ ), specified at a minimum of 120 dB (typically 150 dB).

## The Si7652 Chopper Operation

The very low input offset voltage of the Si7652 is achieved by using an internal nulling amplifier which alternately nulls itself and the main amplifier. A diagram for the basic procedure is shown in Figure 3, and the operating sequence is explained below.

**Period 1:** Initially, switch A is closed and switch  $\bar{A}$  is opened, thus short-circuiting the inputs of the nulling amplifier. Any dc voltage at the output of this amplifier is due to offsets within the amplifier.

**Period 2:** After allowing the output of the nulling amplifier to settle, switch B is closed. The appropriate nulling potential is then applied to the nulling amplifier. The external capacitor, CEXT A, stores this potential for the second half of the complete cycle.

**Period 3:** Switches A and B open, and switch  $\bar{A}$  closes. This connects the inputs of the nulling amplifier across the inputs of the main amplifier. Since the offsets of the nulling amplifier have already been corrected, the output is now due to the main amplifier offsets.

**Period 4:** By now, the output of the nulling amplifier has settled. Switch C is now closed and a correcting potential is applied to the main amplifier. This potential is stored on CEXT B while the procedure is repeated.

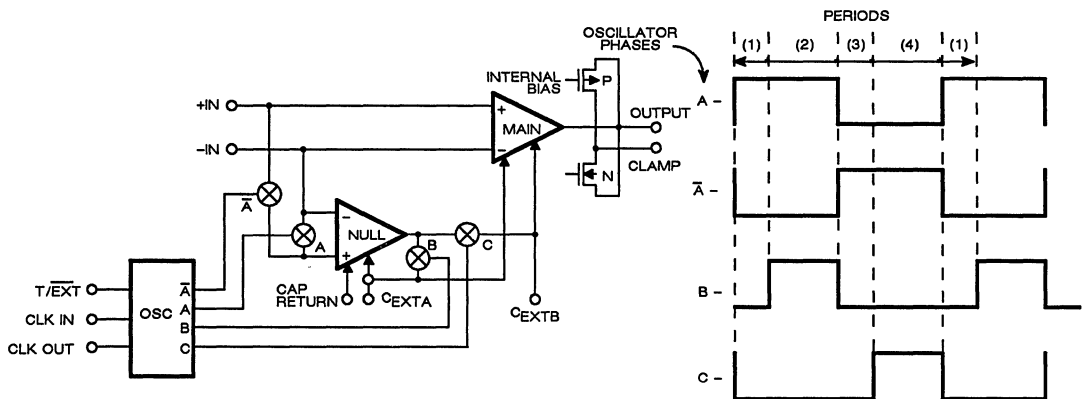


Figure 3. Functional Block Diagram

All logic signals required to drive the switches are derived from an internal, 400-Hz, oscillator. The 14-pin version of the Si7652 provides the option of using an external clock. The external clock input may be used to synchronize the Si7652, switching to the system clock to reduce the effects of the input switching glitch.

## Clamp Circuit Prevents Overload Recovery Delays

The basic inverting amplifier configuration is shown in Figure 4. If the input signal is within the correct operating range (determined by the supplies and the gain), then the differential input at the Si7652 inputs ( $V_{diff}$ ) is virtually zero. However, during an overload condition, the amplifier output stage saturates and can no longer drive the feedback network which maintains accuracy. For example, consider a case where  $R_1 = 1K$ ,  $R_2 = 100K$  (this gives a closed-loop voltage gain ( $A_v$ ) =  $-100$ ), and supply rails of  $\pm 5$  V. An input voltage ( $V_i$ ) of 100 mV will result in an output voltage of  $100 \text{ mV} \times -100 = -10$  V. This voltage, however, is beyond the range of the power supplies, and the output saturates at  $-5$  V. The feedback network applies a voltage which is less than the voltage required to maintain  $V_{diff}$  at zero. The nulling amplifier can only interpret this voltage as an offset, and when it attempts to correct for the offset, the external capacitor, CEXT B, is charged to the supply rail. When the amplifier comes out of saturation, it may take several seconds to discharge the external capacitor and restore operation of the chopper.

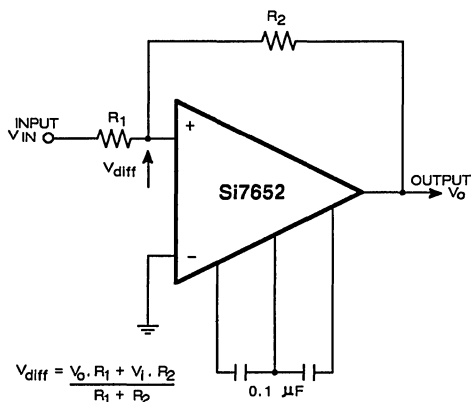


Figure 4. Basic Inverting Amplifier

To overcome the overload recovery problem, the 14-pin version of the Si7652 includes an output clamp circuit (Figure 5). This consists of the two comple-

mentary MOSFETs in parallel. The common sources of the parallel MOSFETs are tied to the output, and their common drains are brought out via the clamp pin.

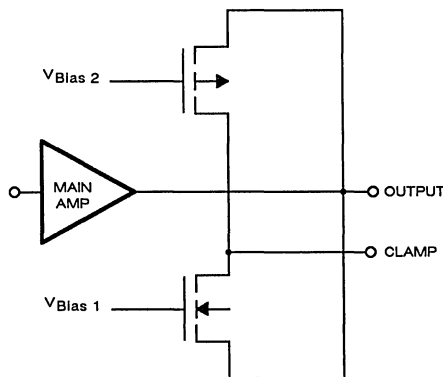


Figure 5. The Use of Complementary MOS to Implement an Output Clamp

The gate threshold voltages are set so that one of the MOSFETs turns on when the output swings within a few hundred millivolts of a supply rail.

If the clamp pin is connected to the summing point of the amplifier, the MOSFETs are effectively in parallel with the feedback resistor ( $R_2$ ). As the output approaches one of the rails, the clamp MOSFETs can be considered variable resistors, reducing the gain of the amplifier (see Figure 6). The effect of using the clamp on the overload recovery time is shown in Figures 7a and 7b.

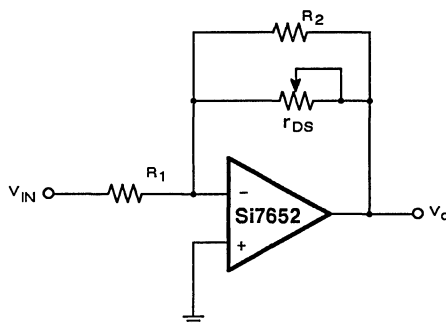


Figure 6. Reduction of Gain Resulting From the Clamp Connection

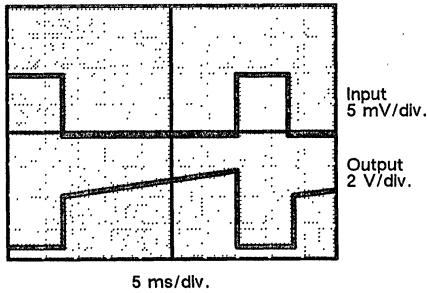


Figure 7a. An Oscilloscope Showing the Overload Recovery Time Without Clamp

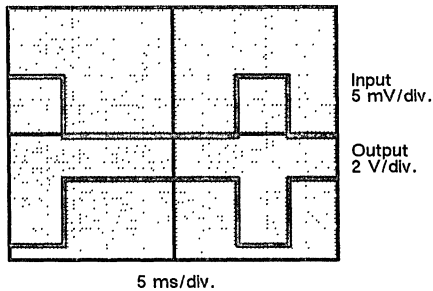


Figure 7b. An Oscilloscope Showing the Overload Recovery Time With Clamp

The clamp circuit has already been discussed as a means of minimizing the overload recovery time of the capacitors. Another method is to inhibit capacitor charging during an overload. In the Si7652, this charging is inhibited by detecting the overload conditions and applying a low strobe signal to EXT CLK IN for the duration of the overload.

### Tips for Ensuring Precision Operation

In systems that resolve microvolts, errors that are often ignored must be taken into consideration. Three of the most common error sources are: thermally generated error voltages [thermal electromotive force (EMF)], leakage currents, and transformer fields.

Thermal EMF is usually the main error source in low-level signal applications. Whenever two metals or

semiconductors are connected, a small potential difference, or EMF, is produced across the junction. This EMF increases as the temperature increases. Thermal EMFs can be as large as a few  $\mu\text{V}$ , a significant value for low-level signals. Also, these EMFs can vary by as much as a few  $\mu\text{V}/^\circ\text{C}$ , causing additional drift errors. To avoid offset errors due to thermal EMFs, it may be necessary to add junctions. Since the amplifier is differential, the number of junctions must be equal before each input. An example of this design is shown in Figure 8.

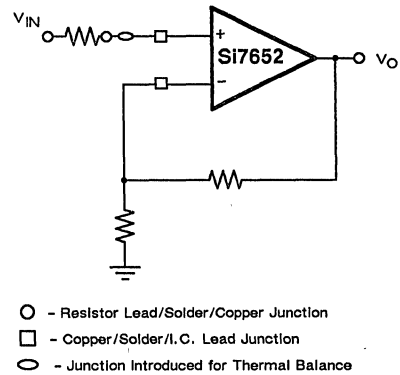


Figure 8. Using Junctions to Equalize Thermal EMF's

To balance the temperature effects apparent at the inputs, it is important to design a symmetrical circuit. Lead lengths on components ahead of the inputs should also be equal. Figure 9 shows a test circuit which illustrates these design features.

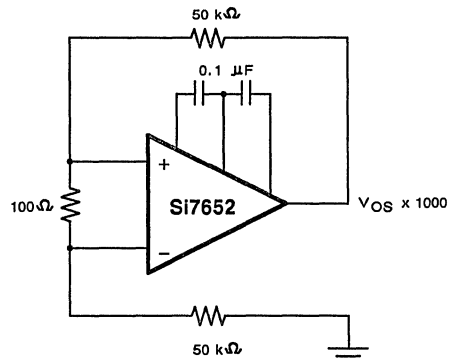


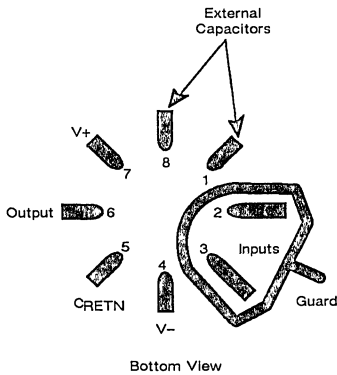
Figure 9. A Thermally Balanced Test Circuit



Placing high-power dissipative (i.e., hot) circuit elements away from the chopper-stabilized amplifier is one precaution. Fans are another source which create large temperature gradients. If cooling is necessary, another method should be employed.

**Leakage Effects**

Leakages from circuit elements such as diodes and capacitors must be carefully considered in high-impedance systems. Additionally, leakage from contaminated PC boards and sockets can cause unforeseen errors at the microvolt level. Input guarding, as shown in Figure 10, may be necessary.



Board layout for input guarding with TO-99 package.

**Figure 10.** Guarding the Input From Board Leakages

**Transformer Fields**

Electromagnetic fields are another source of error when dealing with low-level signals. If possible, transformers should be placed on a different board than the chopper-stabilized amplifier. If space restrictions or high-quality grounding requires that a transformer be mounted near the amplifier, use a shielded transformer. If shielded transformers are too costly, careful layout can often produce acceptable results.

It is also advisable to keep low-level signal paths as short as possible and to keep high-energy circuitry away from the low-level signal path.

**Output Loading Considerations**

Because the open-loop gain is proportional to the output load, output loading is an important practical

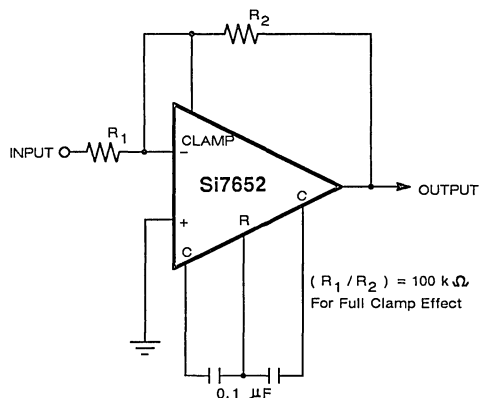
consideration when using a chopper-stabilized amplifier. The wideband frequency of the device deteriorates when the load impedance is less than the typical output impedance of 18 K. Therefore, load impedances should be greater than 18 K. In this case, the open-loop response will be 20 dB per decade from 0.1 Hz to 500 Hz with phase shifts less than 2° in the transition region where the main amplifier takes over from the nulling amplifier. No problem occurs with dc input signals, since the dc gain is typically greater than 120 dB even with the load impedance of only 1 K.

**Latch-Up-Free Operation**

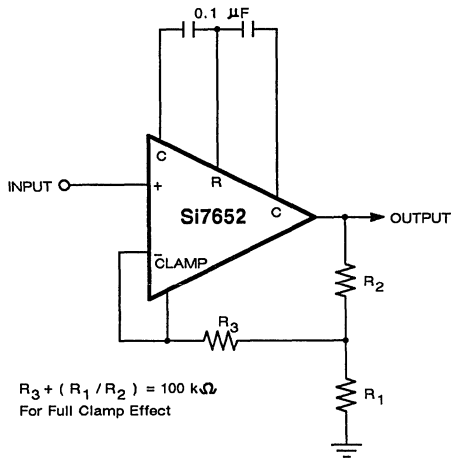
All junction-isolated CMOS devices inherently contain parasitic SCR pnpn structures. If the SCR is turned on, excessive supply current may be drawn, thus destroying the device. However, if no voltage exceeds any supply voltage by more than 0.3 V, excessive supply current is not drawn. In addition, the power supplies should reach their operating voltages either before or at the same time as the input signals. If one of these fault conditions occurs, the input current must be limited to less than 1 mA to avoid latch-up.

**Simple Application Circuits**

Figures 11 and 12 show the Si7652 in the basic inverting and non-inverting amplifier configurations. The connections for the optional clamp circuit are also shown.



**Figure 11.** The Si7652 Configured as an Inverting Amplifier



## Increasing the Output Range

A simple circuit used to boost the Si7652 output is shown in Figures 13 and 14. These figures show both the inverting and non-inverting configurations. To ensure stability, it may be necessary to use a small capacitor (10 nF), as illustrated. With these configurations, the precision input characteristics of the Si7652 are maintained while achieving the output voltage and current range of the output op amp.

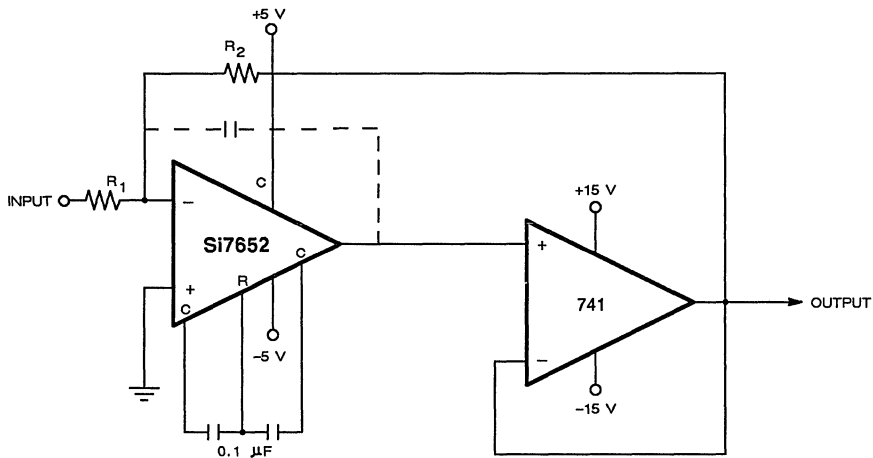


Figure 13. An Output Boost Circuit for The Si7652 (Inverting configuration)

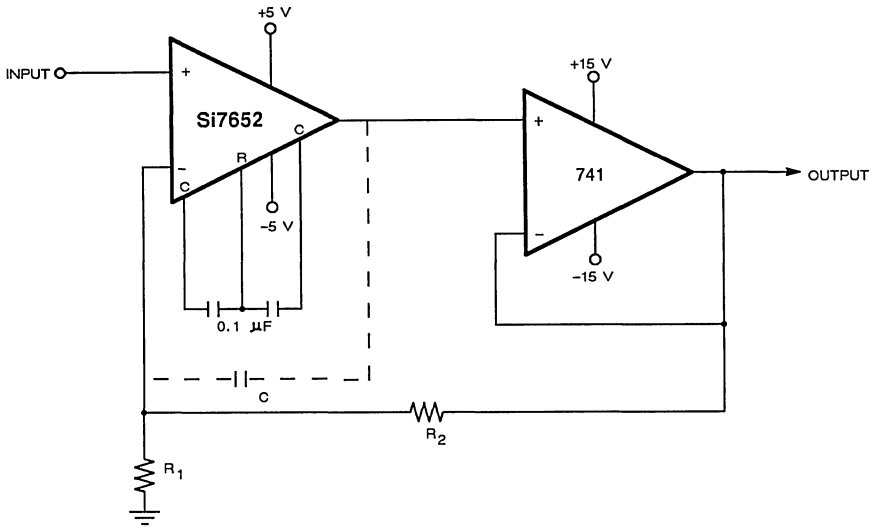


Figure 14. An Output Boost Circuit for The Si7652 (non-inverting configuration)

Figure 15 shows the use of analog switches with the Si7652 to allow a number of inputs and/or gains to be digitally selected. A variation of this concept may also be used to produce a programmable precision

voltage reference suitable for A/D and D/A converters. A circuit for this application is shown in Figure 16.

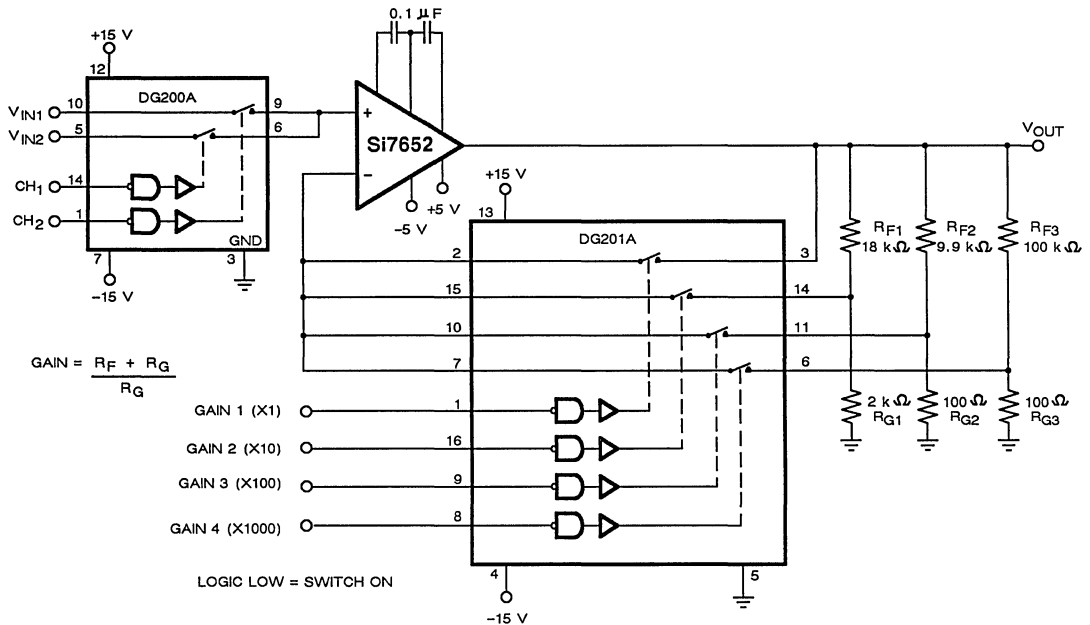


Figure 15. The Si7652 used with analog switches to obtain digitallly selectable inputs and/or gain.

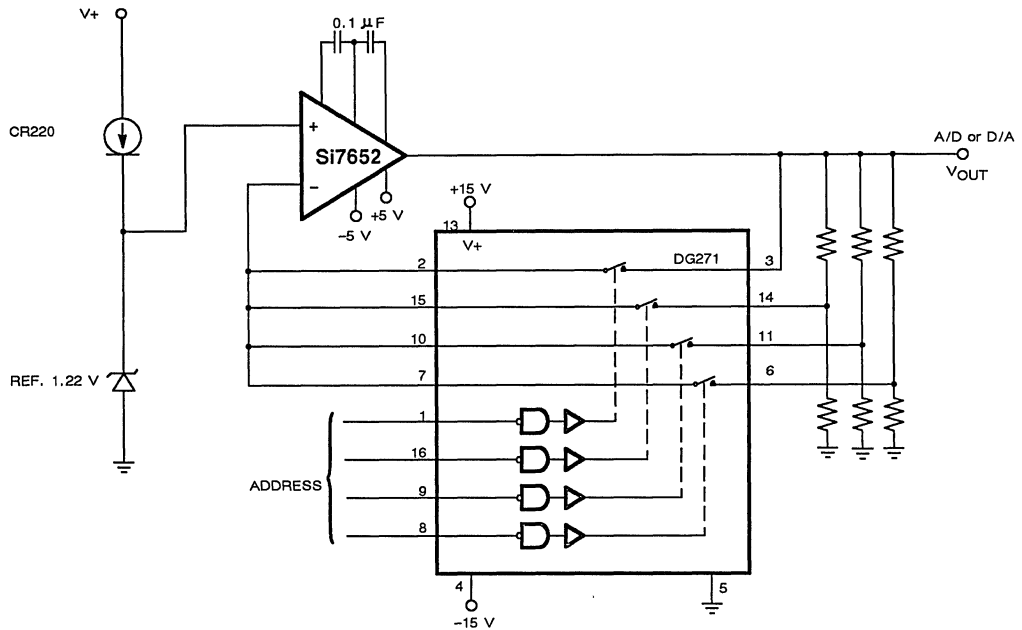


Figure 16. The Si7652 used with analog switches to obtain a programmable precision voltage reference

The precision voltage reference circuit shown in Figure 16 uses a constant current source to feed a bandgap reference diode. This arrangement gives an accurate voltage reference which is stable with temperature (to 10 mV/°C). The Si7652 has negligible effect on its precision or temperature stability, since it has low input offset voltage, low input bias currents, and virtually no temperature drift. The output reference voltage can be easily programmed to accommodate different ranges for the A/D or D/A converter. However, because the current sourcing capability of the Si7652 is limited to 6 mA, some applications may require an output boost as shown in Figure 13. The DG271 analog switch selects a variety of gain configurations for the Si7652, resulting in a digitally programmable precision voltage reference with very low drift.

### The Si7652 as an A/D Input Amplifier

The Si7652 chopper-stabilized amplifier is ideal for increasing the sensitivity of an A/D converter, such as the 4 1/2-digit Si7135. The pre-amplifier boosts  $V_{IN}$ , so the minimum voltage to be measured is much greater than the noise present in the A/D converter.

To do this successfully, the pre-amplifier must have low noise. In the configuration shown in Figure 17, the Si7652 has a bandwidth limited to less than 1 Hz, which gives a typical input noise voltage of 0.2  $\mu$ V. If the pre-amplifier has a gain of 10, the system is capable of a measurement resolution of 10  $\mu$ V. This circuit supplies a 100  $\mu$ V input to the Si7135 compared to a total noise of 17  $\mu$ V (i.e., 2  $\mu$ V of output noise from the Si7652 plus 15  $\mu$ V (typical) of noise due to the Si7135).

Other A/D converters with low input impedances require buffering to maintain system accuracy. For example, the high-resolution (12-bit) successive-approximation A/D converter shown in the data acquisition system in Figure 18 has an input impedance of 20 k $\Omega$ . The DG508A 8-channel multiplexer has a nominal on-resistance of 500  $\Omega$  at the input. If the multiplexer output was used to drive the A/D converter input without buffering, the variations in channel on-resistance that could occur from lot to lot may be as high as 50% of the nominal value. With a 20-k $\Omega$  load, this configuration produces a system error of 1.5%, or 75 LSB in a 12-bit system.

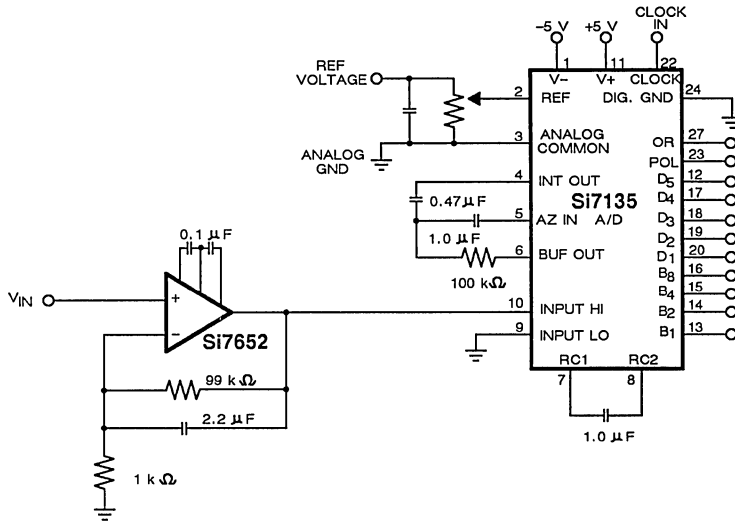


Figure 17. The Si7652 as a Pre-amplifier For an A/D Converter

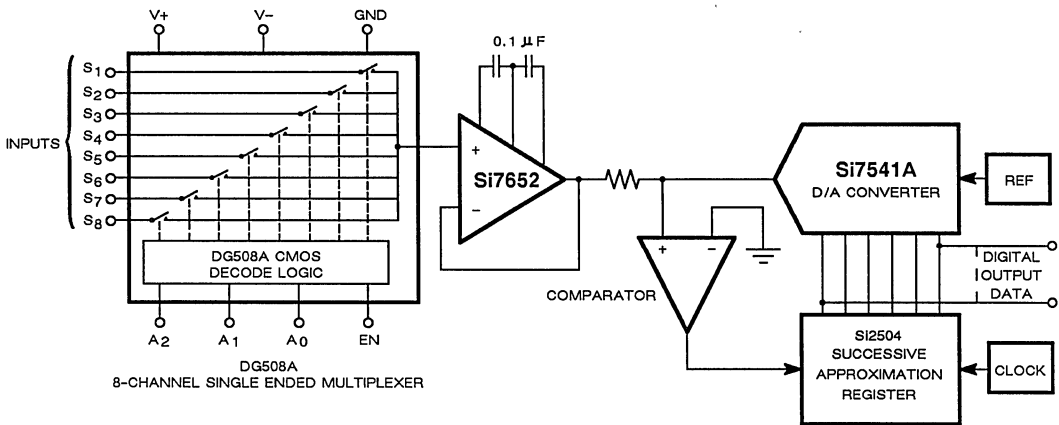


Figure 18. Data Acquisition System

The Si7652 has an input impedance of  $10^{12}$  and an input bias current maximum of 30 pA. The Si7652 may be used as a unity-gain buffer between the multiplexer output and the A/D converter input. This configuration reduces system sensitivity to variations in the multiplexer's on-resistance to the point where those variations contribute a negligible error.

### Sample-and-Hold Applications

In the same data acquisition system, if the input sig-

nal varies during the A/D conversion, an error, which is dependent upon both the speed of the A/D converter and the slew rate of the incoming signal, is generated. A sample-and-hold circuit, shown in Figure 19, reduces this error by taking a sample of the input signal and holding it constant during the A/D conversion. The sample-and-hold performance is determined by the speed of the analog switch, the charge injection of the switch, the size of the hold capacitor, and the input bias current and offset voltage of the op amp.

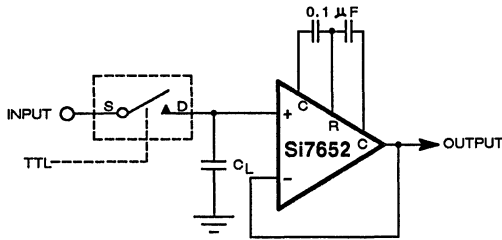


Figure 19. Basic Sample-and-Hold Circuit

## Precision Sample-and-Hold Amplifier

The precision sample-and-hold circuit shown in Figure 20 uses a DG271 analog switch in conjunction with the Si7652. The DG271 is a high-speed switch ( $t_{on/off} < 75$  ns) with very low charge injection (typically 9 pC). Also, to further reduce the effects of charge injection, a capacitor (C1) is added to cancel the charge-induced offsets (pedestal errors). This system keeps pedestal error below 5 mV. If greater accuracy is needed, the capacitor (C2) can be adjusted to totally cancel the coupled charge offsets. The size of the hold capacitor is based on a compromise between input tracking time and droop rate. Aperture time is approximately 100 ns, and the acquisition time is less than 20  $\mu$ s. The measured droop rate (1 mV/sec.) is largely due to the analog switch

leakage. Better droop rate can be achieved with a slight loss in acquisition speed, using the DGP201A precision analog switch in place of the DG271.

By offsetting the supplies of the Si7652 as shown,  $V_{IN}$  will range from 0 to 12 V.

## Low Offset Maintains D/A Linearity

The output amplifier performance often limits the D/A converter accuracy. The popular CMOS D/A converters show an output impedance which is code-dependent, and thus, any offset voltage generated by the D/A output amplifier results in a combination of system offset and nonlinearity which is impossible to trim out. Figure 21 shows the Si7652 used as an output amplifier that performs the current-to-voltage conversion for an Si7541A 12-bit D/A converter. The low offset voltage of the Si7652 is critical to maintaining system linearity.

To demonstrate the importance of a low-offset, low-drift output amplifier, consider the effect of using a biFET op amp in place of the Si7652. The high slew rate and low noise of the industry-standard OP-15 make it useful as an output amplifier for the Si7541A. The top-grade offset voltage of the OP-15 is 250  $\mu$ V at 25°C, and it shows considerable drift over the 0 to 70°C temperature range, reaching a worst-case

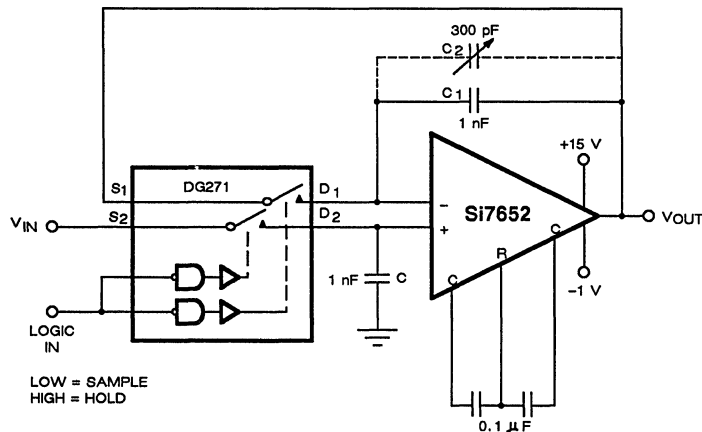


Figure 20. A Practical Sample and Hold Circuit

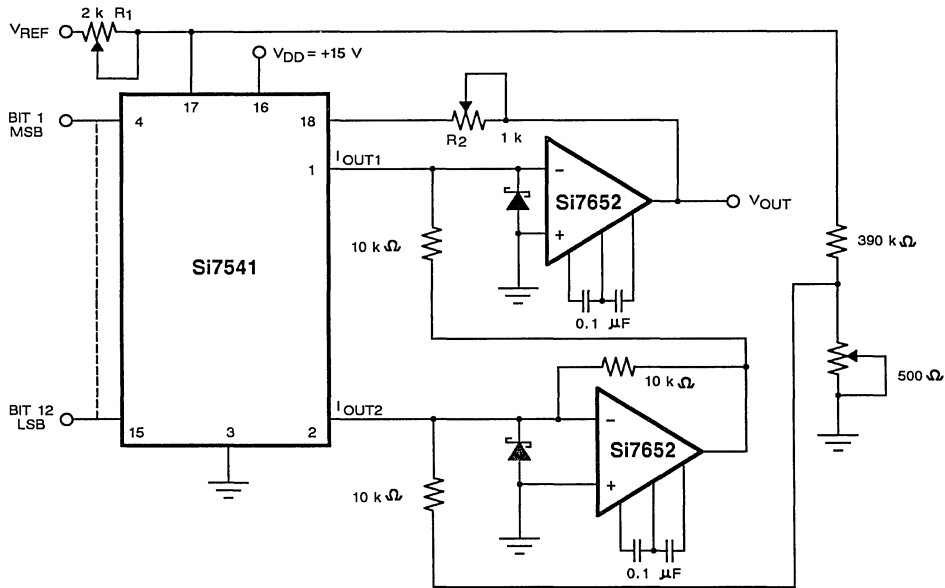


Figure 21. The Si7652 Used as a DAC Output Amplifier

value of 10 mV. A 10-mV offset equals 16 LSB in a 12-bit system with a 2.5-V full-scale range. The linearity error introduced is calculated by dividing the offset by the deviation in the D/A output resistance; the resulting error current is a fraction of the full-scale D/A converter current. The output resistance of the Si7541A can vary as much as 5 kΩ over the D/A converter range. Therefore, with a 10-mV offset from the op amp, the error current could reach  $10 \text{ mV}/5 \text{ k}\Omega = 2 \mu\text{A}$ . With a  $250 \mu\text{A}$  full-scale D/A converter current, the LSB is  $250 \mu\text{A}/4096 = 61 \text{ nA}$ . Thus, the linearity error introduced is  $2 \mu\text{A}/61 \text{ nA}$ , which equals 33 LSB.

The total offset of the Si7652 over temperature is less than 10 μV, three orders of magnitude lower than the 10 mV offset using the OP-15. Hence, significant reductions in offset and nonlinearity are made using the Si7652.

### Differential Thermocouple Amplifier

The circuit shown in Figure 22 is designed to measure the low-level outputs of a thermocouple. Thermocouples usually exhibit a thermal EMF between 7 and 75 μV/°C. These low-level signals require the use of

an amplifier with a low offset voltage and low input bias current. Also, using the standard instrumentation amplifier ensures high input impedance operation. The Si7652 has a maximum input bias current of 30 pA and an input impedance of  $10^{12}$ . Thus, the measurement error is dominated by the contribution of the analog switch leakage and on-resistance, in addition to thermal EMFs as previously discussed. These errors can be eliminated by using a differential measuring technique and by carefully balancing the thermal EMFs in each branch of the differential amplifier configuration. Figure 23 shows how unwanted thermal EMFs cancel in a differential system. Another advantage of using a differential system is that other common-mode errors (e.g., ac noise, leakage offsets, and switching transients) are also rejected. A temperature reference is also included to provide a zero reading at the reference temperature (often 0°C). The temperature reference subtracts a voltage, equal in magnitude to the EMF, which would be generated by the thermocouple. There are various methods of obtaining a temperature reference, including using an ice bath, ice point cells, and electronic cold-junction compensators. Figure 23 shows the effect of using a temperature reference.

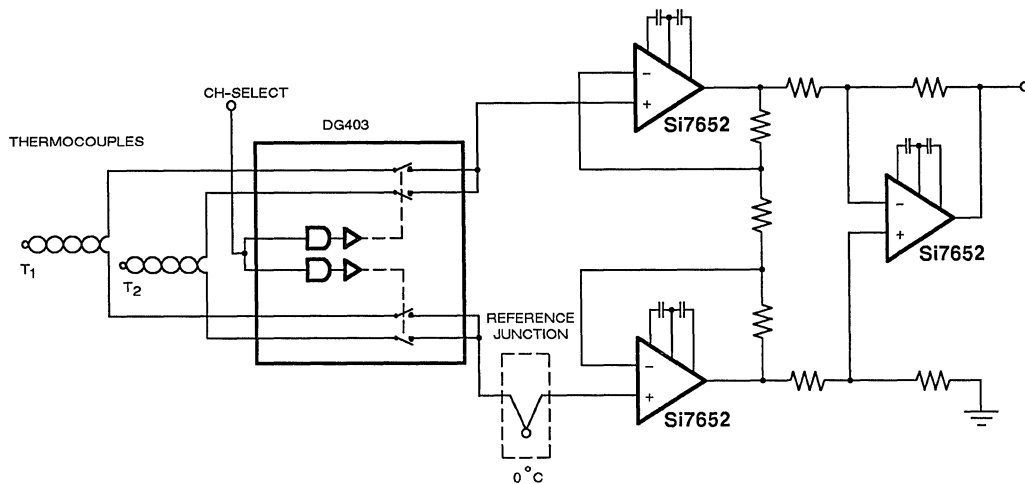
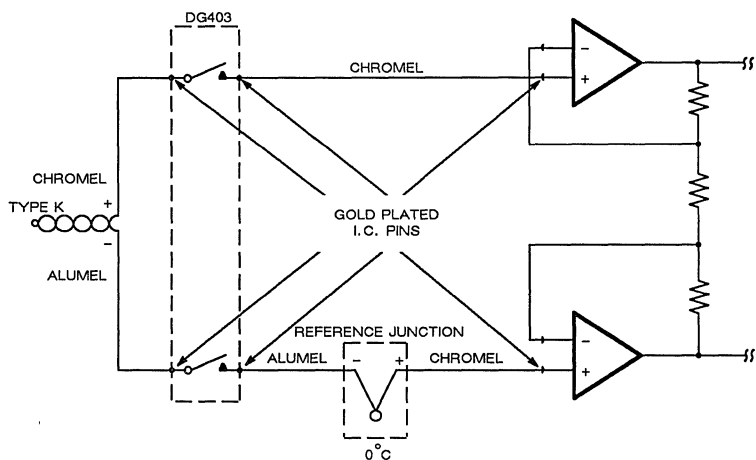


Figure 22. Differential Measurement of Low Level Thermocouple Outputs



Metal Junction

Thermocouple Potentials

Chromel: Alumel

e1

Chromel: Gold

e2

Alumel: Gold

e3

The total thermocouple potential seen by the instrumentation amplifier is:

$$-e2 + e2 + e1 - e3 + e3 - e1 \Big|_{0^{\circ}\text{C}} = e1 - e1 \Big|_{0^{\circ}\text{C}}$$

Figure 23. Simple Model to Illustrate the Differential Cancellation of Thermal EMFs



# THE SI7541A 12-BIT CMOS MULTIPLYING DAC THEORY AND APPLICATIONS

By Jack Armijos and Carl Jones  
August 1987

## INTRODUCTION

This application note provides the information needed to understand CMOS digital-to-analog converter (DAC) operation and to implement successful designs using the Si7541A 12-bit DAC. The basic principles of DACs and their main error sources are presented. In addition, a detailed description of the Si7541A 12-bit DAC and the results of a comparative study with respect to other presently available alternate sources is provided. A series of application circuits with practical recommendations is then presented. This note ends with an appendix covering voltage references and resistance ladders.

## BASIC DAC PRINCIPLES

Some of the basic concepts and definitions associated with DACs are best understood by first understanding the function of a simple DAC.

### Definition

A DAC is essentially a digitally controlled potentiometer that produces an analog output (voltage or current) that is a fraction of the full-scale setting. The full scale setting or value is determined by the magnitude of the reference voltage chosen. If the reference changes, the DAC output changes. Therefore, to improve system accuracy, a precision reference must be used.

## Basic DAC Circuit

A basic DAC can be built using a voltage reference, a set of binary weighted resistors, and a set of switches (Figure 2). An output amplifier converts current to voltage and provides a low-impedance voltage output. In this example, the op amp holds one end of all switches at 0 V. The currents flowing through the resistors are binary-weighted. Each switch is operated by a digital bit, open for a zero and closed for a "one".

A DAC translates digital data from a data processor into an analog waveform containing information that can be used in the "real world". Figure 1 shows a simplified block diagram illustrating the use of a DAC to make a computer talk.

Each switch that closes adds a binary-weighted current increment to the summing node connected to the amplifier's inverting input. The negative output voltage is proportional to the total current and, thus, to the binary value represented by the digital input code.

For resolutions exceeding 4 bits, this scheme is not practical. For example, in 8-bit conversion, the required resistance ratio is 128:1 (e.g., 1.28 M $\Omega$  to 10 k $\Omega$ ). If discrete resistors are used, cost and size are increased, and temperature tracking, matching, and parasitic impedances become a problem.

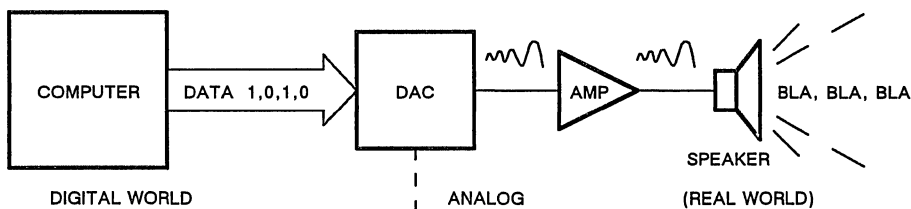


Figure 1. A Basic DAC Application

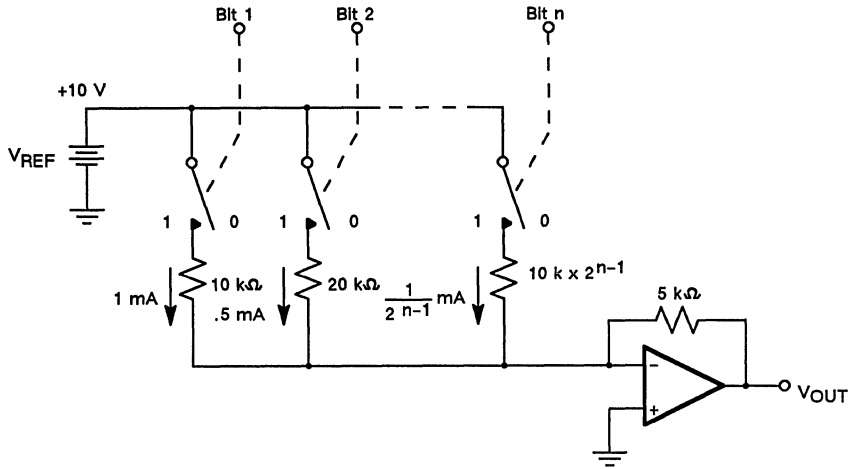


Figure 2. A Simple DAC Using Binary-weighted Resistors

**Typical Specifications**

DAC performance is measured in several areas: accuracy (both absolute and with respect to full scale), linearity (both integral and differential), offset, noise, conversion time, and output transients (glitch impulse). Also of importance are the long-term stability of these parameters as well as their sensitivity to temperature variations.

Transfer Function. Figure 3 is the transfer function of an ideal unipolar 3-bit DAC. It consists of a set of discrete points, corresponding to all the digital codes that can be input to the device. A 12-bit DAC, for example, will have  $2^{12} = 4096$  points. The ideal DAC has a linear transfer function; that is, all points fall on a straight line.

The transfer function can be unipolar (output values have only one polarity) or bipolar (the output can be either positive or negative), depending on how the DAC is configured. Sometimes the reference quantity is a variable input signal. This produces a multiplying DAC since the output becomes the product of two variables: the analog reference voltage and the number represented by the digital input code. Both variables may vary from zero to full scale and have positive or negative values.

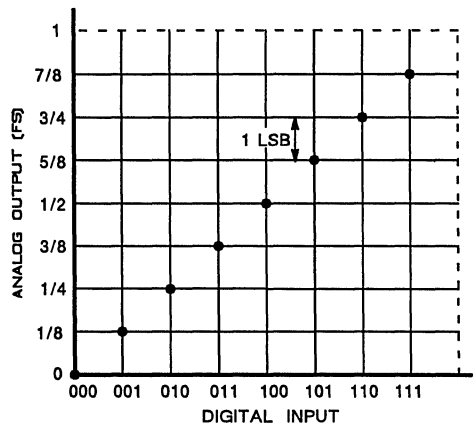


Figure 3. Unipolar Transfer Function for an ideal 3-bit DAC

Figure 4 shows the transfer function of a bipolar 3-bit DAC. The digital coding used can be offset binary or two's complement [the most significant bit (MSB) is complemented.] In the bipolar mode, the maximum output value is still 1 least significant bit (LSB) below full scale (FS), but an LSB is twice as large as it is in the unipolar mode because the total output swing is now  $(2 FS - 1 LSB)$ .

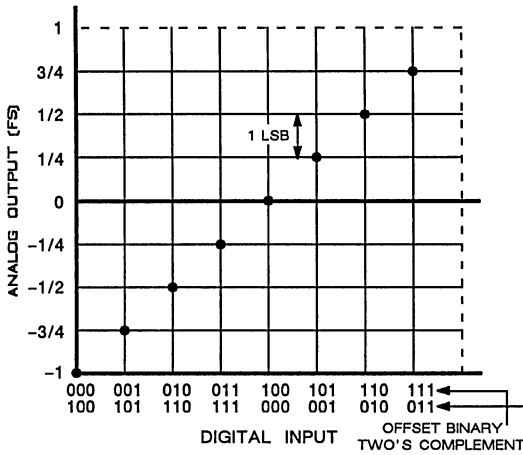


Figure 4. Bipolar DAC Transfer Function

**Resolution.** Resolution refers to the number of different output voltage levels that the DAC can produce. It also indicates the number of digital input bits. (Twelve-bit DACs resolve the full-scale range into 4096 states.)

**Monotonicity.** The output of a monotonic DAC is one that either increases or remains constant for increasing input so that the output will always be a single-valued function of the input. This is an important specification, especially in automatic control applications.

**Accuracy.** The absolute static accuracy of a DAC refers to how closely its transfer function follows the transfer function of an ideal DAC. Three types of error are used to quantify the accuracy of a DAC: offset, gain, and integral (non-)linearity errors.

In many applications, adjustments can be made to trim out or compensate for the offset and gain errors by providing endpoint autocalibration. On the other hand, it is usually impractical to compensate for linearity errors.

**Offset Error.** Figure 5 shows the result of offset error. The transfer function is parallel to the ideal but offset by 2 LSBs. (For a unipolar 12-bit converter, 1 LSB =  $V_{REF} / 4096$ ).

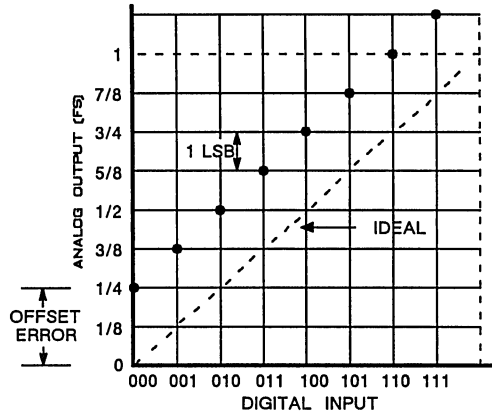


Figure 5. An Offset Error of +2 LSB

**Gain Error.** Figure 6 shows the effect of gain error. In this case, the slope of the transfer function differs from the ideal DAC. Gain error or full-scale error is measured with an all ones input code.

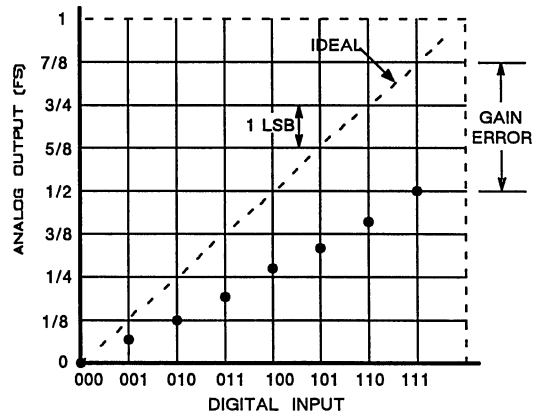


Figure 6. A Gain Error of -3 LSB

**Relative Accuracy.** This term is also known as integral non-linearity, integral linearity error, or endpoint linearity. Relative accuracy is the maximum deviation from a straight line drawn through zero and full-scale at any point in the transfer function. It is measured after adjusting for zero and full-scale errors, and can be expressed as a percentage of full-scale range or (sub)multiples of 1 LSB. Figure 7 illustrates non-symmetrical integral linearity errors.

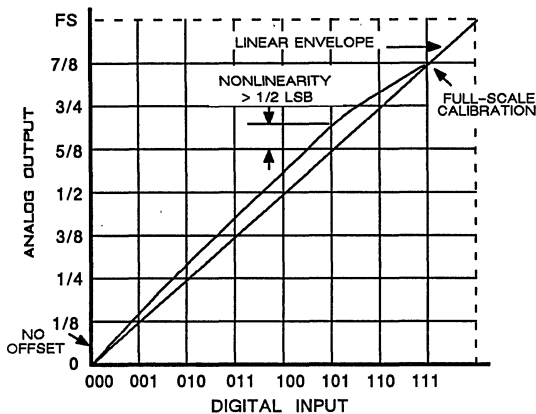


Figure 7. Non-symmetrical Integral Linearity Errors

**Differential Non-linearity.** Also known as differential linearity error, differential non-linearity is the maximum deviation of any analog output step between adjacent input codes, from the ideal step value of 1 LSB. Differential non-linearity is a quantitative measure of monotonicity. It is also a measure of the maximum step size. A specified differential non-linearity of  $\pm 1$  LSB maximum over the operating temperature range guarantees monotonicity.

**Gain Temperature Coefficient (Gain TC).** Most modern CMOS DACs have gain TCs on the order of  $\pm 5$  ppm/ $^{\circ}$ C. This specification is used to determine the worst-case gain variation caused by temperature variations and the difference between TCs of the feedback resistor and the R-2R ladder. The worst-case corresponds to a  $10^{\circ}$ C segment of the total temperature range. For a temperature variation from  $-25$  to  $125^{\circ}$ C, the average TC is generally better than  $\pm 3$  ppm/ $^{\circ}$ C. However, for worst-case analysis, it is often assumed that the worst-case gain TC applies over the whole operating temperature range.

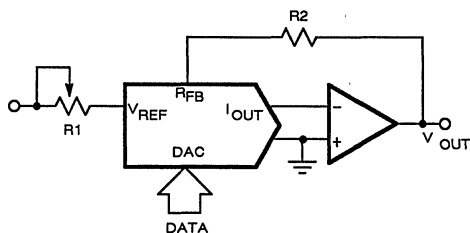


Figure 8. Gain Trim Circuit for CMOS DACs

**Gain Trim Circuit.** One may compensate for gain error and the ideal full-scale value may be restored by using a fixed resistor and a trim potentiometer, as shown in Figure 8.

The maximum values for R1 and R2 may be calculated using

$$R1_{max} = \frac{2 |e| R_{max}}{100}$$

$$R2_{max} = \frac{R1_{max}}{2}$$

where R max = maximum specific value of the R-2R ladder ( $V_{REF}$  max)

e = gain error (%)

The TCs of the DAC, of the external resistors R1 and R2, and of the operational amplifier cause variations in the full-scale output with temperature. The TCs of the R-2R ladder and the feedback resistor are approximately  $-300$  ppm/ $^{\circ}$ C; however, careful design allows their ratio to track so the total effect is better than a  $\pm 5$  ppm/ $^{\circ}$ C TC.

The worst-case additional TCs due to R1 and R2 are

$$R1 = \frac{-2 |e| R_{max}}{100 R_{min}} (\gamma_1 - \gamma)$$

$$R2 = \frac{+ |e| R_{max}}{100 R_{min}} (\gamma_2 - \gamma)$$

where  $\gamma$  = TC of the DAC resistor material in ppm/ $^{\circ}$ C  $\gamma_1$  and  $\gamma_2$  = TCs of R1 and R2, respectively, in ppm/ $^{\circ}$ C

If R1 and R2 have the same TCs, the overall additional TC is given by

$$\text{additional TC} = \frac{R2 - R1}{R} (\gamma_1 - \gamma)$$

The potentiometer's TC usually varies with setting, making it difficult to match the TC of the fixed resistor. Therefore, it is advisable to use "select-on-test" fixed resistors for R1. To minimize the additional TC

introduced by the trim components, it is preferable to use devices with an improved figure of merit.

$$\text{figure of merit} = \frac{|e| R_{\text{max}}}{R_{\text{min}}}$$

For instance, selected 12-bit DACs specify gain errors of  $\pm 1$  LSB at 25°C. This represents more than a twelfold improvement in the figure of merit. For most applications, this tight specification either eliminates the need for gain trimming or makes R1 and R2 so small that the additional TC becomes negligible.

Leakage Effects on Gain. In precision applications, gain error shifts with temperature can also be caused by op amp offset and input bias drifts, changes in  $V_{\text{REF}}$ , and leakage currents.

The  $I_{\text{OUT}}$  leakage current effect on gain is negligible at and below room temperatures, but above 100°C, the effect of leakage on gain is considerable. Leakage has two main sources:

1. Leakage which is fairly constant and independent of input code, comes from the  $V_{\text{DD}}$  supply.
2. In the off state, leakage comes through switches from the R-2R ladder. For an all-zeros input code, this leakage has a maximum effect because all switches are off; however, when there are all ones at the input, a minimum effect results. The leakage current magnitude is a direct consequence of fabrication process, chip layout, and operating temperature.

Although exaggerated, Figures 9 and 10 illustrate the gain shifts produced by the two types of leakage and for the two polarities of  $V_{\text{REF}}$ .

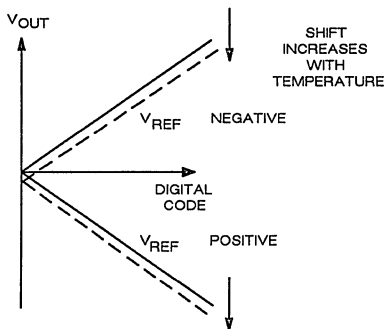


Figure 9. Gain Shift Due to Leakage From  $V_{\text{DD}}$

Leakage from  $V_{\text{DD}}$  produces a parallel shift; whereas, leakage from the analog switches tends to produce a rotation of the transfer function.

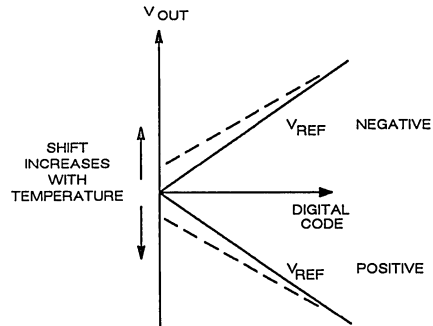


Figure 10. Gain Shift Due to OFF-switch Leakage

With a negative  $V_{\text{REF}}$ , the two leakage effects tend to cancel each other near zero and give a net gain decrease at full scale. However, the trim resistors R1 and R2 introduce a positive TC; the combined result is a reduction in gain variation with temperature.

For positive values of  $V_{\text{REF}}$ , the two leakage effects and the TC of R1 and R2 are added, producing more gain variation with temperature than occur with negative reference applications.

Leakages can also be caused by film residues from cleaning solvents used during printed circuit board manufacture. Therefore, such residues should be avoided for precision DAC applications.

Multiplying Feedthrough Error. Multiplying feedthrough error is an ac error that results from capacitive feedthrough from  $V_{\text{REF}}$  to OUT1 with the DAC loaded to all zeros.

Output Current Settling Time. The time required for the output current of the DAC to settle to within 1/2 LSB for a zero to full-scale digital input stimulus is known as output current settling time. It is measured with an  $R_{\text{L}} = 100 \Omega$ ,  $C_{\text{EXT}} = 15 \text{ pF}$ .

Digital-to-Analog (D/A) Glitch Impulse. D/A glitch impulse is a measure of the area of the impulse injected to the analog outputs when the digital inputs change state. It is usually specified as the area of the impulse in nV-s. It is measured with  $V_{\text{REF}} = \text{GND}$  and an LH0032 as the output op amp and the phase-compensation capacitor = 0 pF.

## DETAILED DESCRIPTION OF THE SI7541A

The Si7541A is a 12-bit multiplying DAC consisting of a highly stable thin-film R-2R ladder network and 12 single-pole double-throw (SPDT) current steering NMOS analog switches on a monolithic chip. The binary weighted CMOS level shifters provide low power TTL/CMOS-compatible operation. An external voltage or current reference and an op amp are required for most applications.

The binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each leg of the ladder, regardless of switch states.

The input resistance at  $V_{REF}$  (Figure 11) is always equal to the "R<sub>REF</sub>" and is the R-2R ladder characteristic resistance. Since R<sub>REF</sub> at the  $V_{REF}$  pin is constant, the reference terminal can be driven by a reference voltage or a reference current, either positive, negative, or ac. If a current source is used, a low value TC external feedback resistor R<sub>FB</sub> is recommended to define the scale factor.

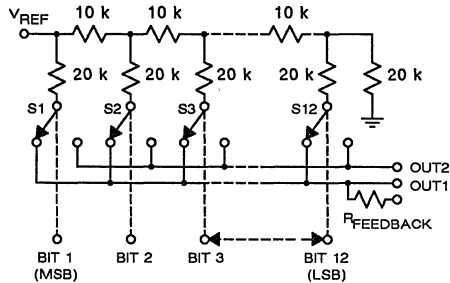


Figure 11. Si7541A Functional Diagram (All Inputs HIGH)

Figure 12 illustrates the typical NMOS SPDT switch with its associated CMOS level shifter/driver.

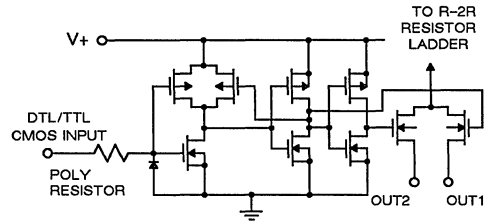


Figure 12. Simplified Schematic of One SPDT Switch

## EQUIVALENT CIRCUIT ANALYSIS

Figure 13 shows the equivalent circuit for all digital inputs low. All reference current is switched to OUT2. The current sources  $I_{LEAKAGE}$  are composed of surface and junction leakages to the substrate. The  $1/4096$  current source represents the constant 1 LSB current drain through the ladder termination resistor. For the industry-standard 7541A, the output capacitance on OUT2 (with all its switches turned on) is typically 200 pF, whereas on OUT1, it is typically 70 pF.

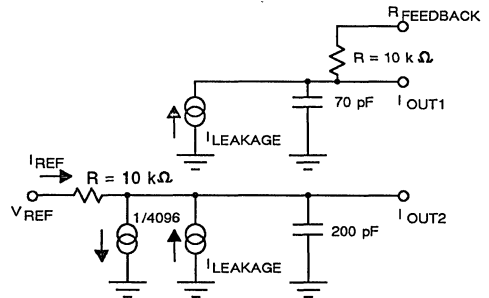


Figure 13. Si7541A Equivalent Circuit (All Inputs LOW)

The output capacitances are dependent on the digital input code and vary between the low and high values.

Analysis of the circuit for all digital inputs high, as shown in Figure 14, is similar to Figure 13; however, the on-state switches are now on OUT1, resulting in 200 pF at that terminal.

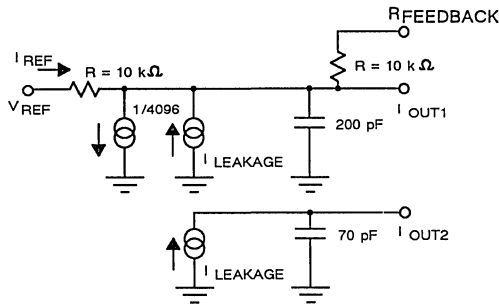


Figure 14. Si7541A Equivalent Circuit (All Inputs HIGH)

**COMPARATIVE ANALYSIS**

A comparative study was conducted to verify the achievement of design goals. Devices from three other manufacturers were tested against the Si7541A. The Si7541A met or exceeded all the speci-

fications in the industry-standard data sheet. Several areas showed considerable improvement.

Bench tests conducted in the Siliconix applications lab showed that the Siliconix Si7541A can drop into sockets using any other manufacturer's devices. Tests also demonstrated that several improvements, presented in Table 1, resulted. The highlights from this table are given below.

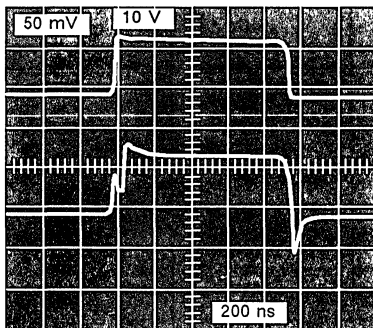
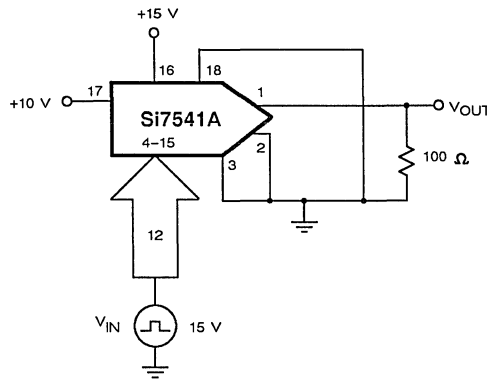
1. Input/Output Capacitances. The Si7541A has the lowest input and output capacitances (considerably lower than the data sheet specification). This translates into better dynamic performance (more speed), as seen later.
2. Input Resistance. The Si7541A devices showed the least unit-to-unit variation ( $\pm 1\%$ ). Low variation helps to reduce gain error over temperature. The vendor A's AD7541ABQ showed the highest variation of  $\pm 8\%$ .

Table 1. Comparative Chart

Manufacturer Part Number Date Code	Siliconix Si7541ASD 8642	Vendor A AD7541ABQ 8614	Vendor I AD7541BD 8625	Vendor P PM7541EX 8520
Input Capacitance: Max C <sub>in</sub> (pf)	7 (1) BEST	8.5 (2) BETTER	9.3 (4) GOOD	8.3 (1) BETTER
Output Capacitances: All zeros: C1 (pf)	48 (1) BEST	48 (1) BEST	50 (3) GOOD	98 (4) WORST
C2 (pf)	77 (1) BEST	185 (4) GOOD	170 (3) GOOD	148 (2) BETTER
All Ones: C1 (pf)	106 (1) BEST	187 (3) GOOD	160 (2) BETTER	198 (4) WORST
C2 (pf)	42 (2) BETTER	40 (2) BETTER	47 (4) GOOD	38 (1) BEST
Input Resistance (kΩ)	9.5 ± 0.5% (1) BEST	11 ± 8% (4) WORST	8.5 ± 0.5% (3) GOOD	15 ± 1.5% (2) BETTER
Logic Threshold (V)	1.16 (1) BETTER	1.64 (2) GOOD	1.5 (2) GOOD	1.64 (2) GOOD
Prop. Delay t <sub>p</sub> (ns)	42 (1) BEST	88 (3) GOOD	136 (2) WORST	95 (4) BETTER
Glitch Impulse (nV-s)	819 (1) BEST	2778 (2) GOOD	1030 (4) BETTER	3990 (3) WORST
Settling Time (ns) (to 0.01%)	640 (1) BEST	1035 (3) GOOD	750 (2) BETTER	1360 (4) WORST
Needs Prot. Schottky	NO (1) GOOD	NO (1) GOOD	YES (4) BAD	NO (1) GOOD
Overvoltage	BEST (1) BEST	GOOD (2) GOOD	WORST (4) WORST	GOOD (3) BAD
OVERALL RATING (n) = Competitive place	"(1)" BEST	(2) BETTER	(3) GOOD	(3) GOOD

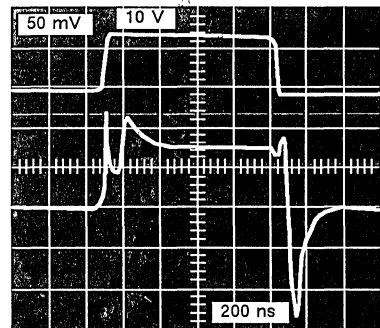
\*Disclaimer: Tests were conducted using a limited number of devices. However, the results were consistent for each manufacturer's parts, and therefore, they are considered truly representative of typical performance.

3. Input Logic Threshold. All parts tested were TTL compatible for  $V_+ = +15\text{ V}$ , and CMOS compatible for lower values of  $V_+$ . The Si7541A showed a logic threshold of 1.16 V vs. 1.5 V to 1.64V for other vendors. This guarantees the best noise immunity for military (0.8-V and 2.0-V) applications.
4. Propagation Delay. The lower input/output capacitances of Siliconix DACs allow from 2 to 8 times shorter delays than the DACs made by the other manufacturers (Figure 15).
5. Settling Time. The Si7541A devices settle faster, more than twice as fast as the slowest device tested.
6. Glitch Impulse. The Si7541A shows the smallest glitch impulse areas. Figure 16 shows a comparison of glitch impulses between the Siliconix and vendor A's parts.
7. Dynamic Performance. With a slow output op amp (OP-07), there is no appreciable difference among the four manufacturers tested (Figure 17). However, with a faster op amp (OP-27), the Siliconix parts produce the smallest overshoots and settling times (Figure 18). This improves precise operation and allows higher conversion rates.



Si7541A

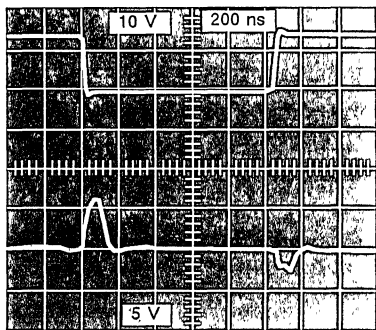
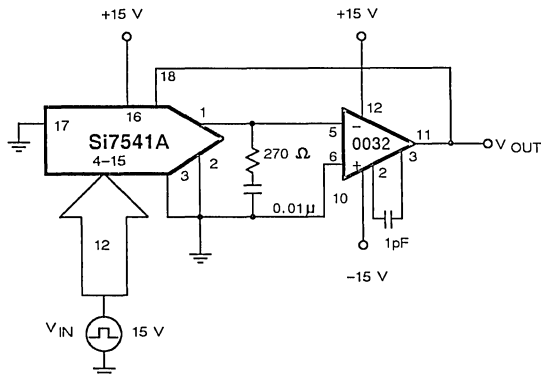
$V_{IN}$   
 $V_{OUT}$



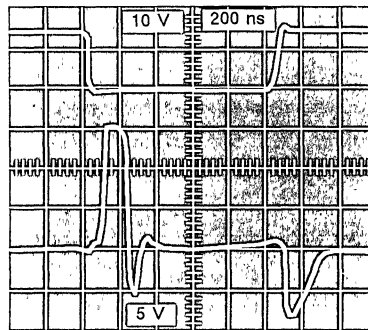
AD7541A

Figure 15. Propagation Delay and Settling Time Comparison





Si7541A

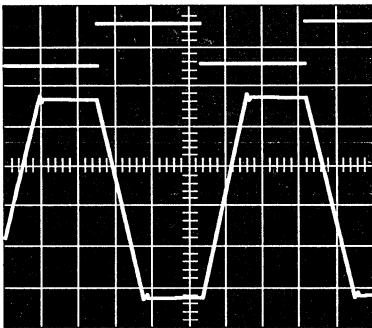
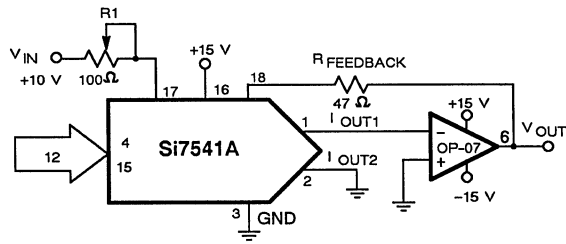


AD7541A

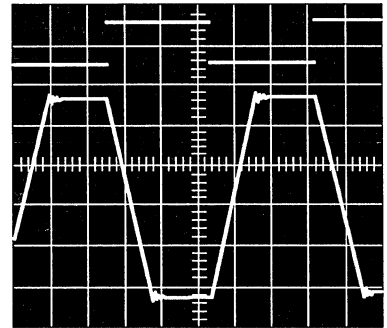
Figure 16. Glitch Impulse Comparison

8. **Overvoltage.** Vendor I's data sheet recommends Schottky protection diodes at the DAC output and contains a warning to avoid overvoltages at the logic inputs which could lead to latchup and device destruction. None of the four parts tested latched up; nevertheless, Siliconix devices displayed a superior overvoltage resistance on the

digital input pins, resulting from improved input stage design. Vendor P's parts showed some parasitic transistor action (a tendency to latchup). Vendor I's parts were the most vulnerable with an apparent parasitic diode turning on for both plus and minus polarities.

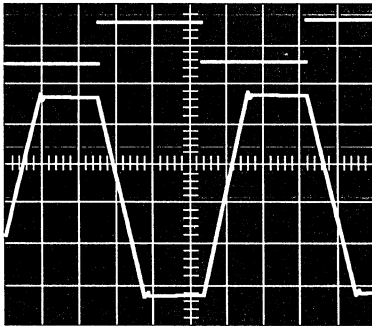


Vendor A

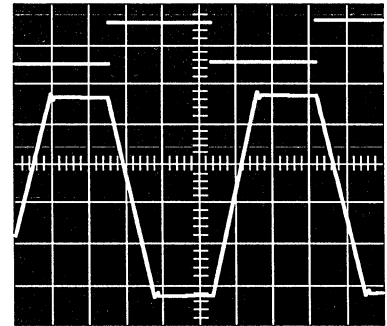


Vendor P

Scales: 10 V  
2 V  
5 μS

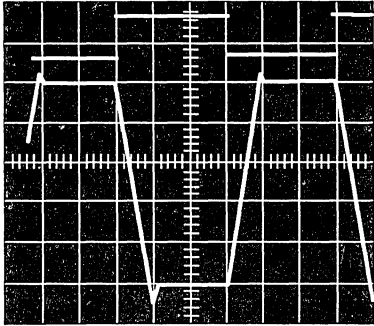
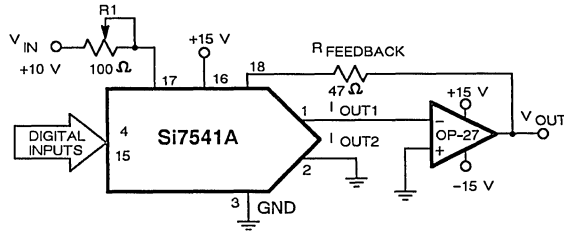


Vendor I

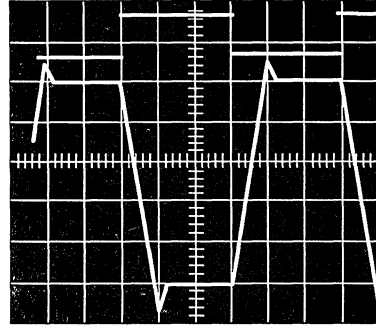


Siliconix

Figure 17. Similar Dynamic Performance with OP-07. C = 0

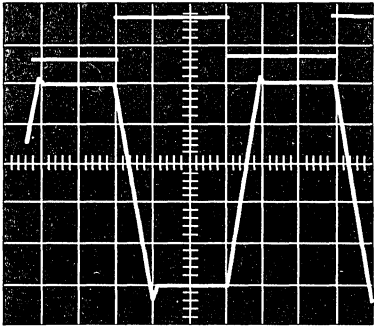


Vendor A

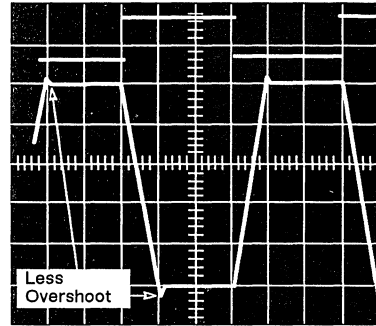


Vendor P

Scales: 10 V  
2 V  
5 μs



Vendor I



Siliconix

Figure 18. Dynamic Performance with OP-27 C = 22 pF

## TYPICAL APPLICATIONS

### Current Steering Mode

**Unipolar Binary Operation.** The circuit shown in Figure 19 is the basic building block for many DAC applications. A fixed reference voltage is applied and a 12-bit digital word controls the output current, which is converted into a voltage by a suitable buffer amplifier. The output can be selected to a resolution of 12 bits (i.e. 4096 steps) between 0 V and  $-(4095/4096) V_{IN}$ .

For best results, the output amplifier should have very low input offset voltage ( $V_{OS} < 25 \times 10^{-6} V_{IN}$ ) and low input bias currents ( $I_B < 100$  nA). Resistors R1 and R2 can be used to set up the correct full-scale output  $V_{IN}$  (i.e.  $-(4095/4096)$  for a digital input of 1111 1111 1111).

R2 should be selected according to

$$R_2 = \frac{(\text{MAX GAIN ERROR IN \%}) \cdot R_{REF} \text{ Max}}{100}$$

R1 can then be varied to produce the correct full-scale output. (R1 will be less than twice R2). R1 and R2 must have low, well-matched TCs; therefore, precision metal-film or wire-wound resistors with a TC of

50 ppm/°C are recommended. Also, since the TC of potentiometers vary with wiper position, a fixed value resistor (or two in series) should be selected for R1. An alternative method is to adjust the magnitude of  $V_{IN}$ , thus avoiding any TC mismatch between the external and the on-chip resistors.

The capacitor, C, used for phase compensation affects the overshoot and settling time of the system. The optimum value for C is dependent on the output capacitance of the Si7541A (which is code dependent), the value of the feedback resistor  $R_{FB}$ , and the unity gain-bandwidth product of the output amplifier.

A good approximation for the Si7541A is given by

$$C = \frac{10^{-7}}{\sqrt{\text{GBW}}}$$

where GBW = the gain-bandwidth product of the output amplifier

Figures 20 and 21 show the effect of different value compensation capacitors with two popular amplifiers. Although the OP-27 gives a more accurate result, it has a relatively slow slew rate when compared to the faster-slew rate FET-input op amps such as the TL071. The effect of this on the rise and fall times is apparent in these photographs ( $f = 20$  kHz).

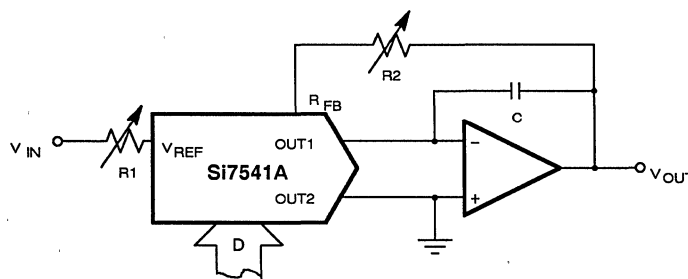
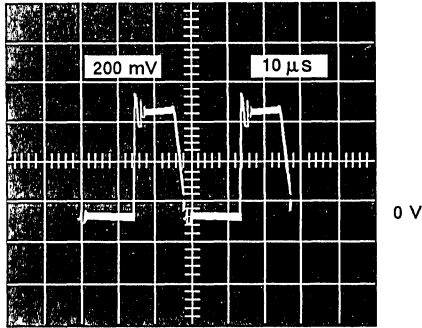
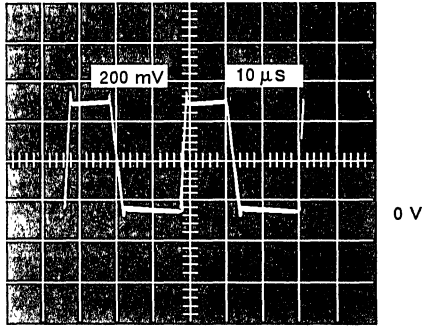


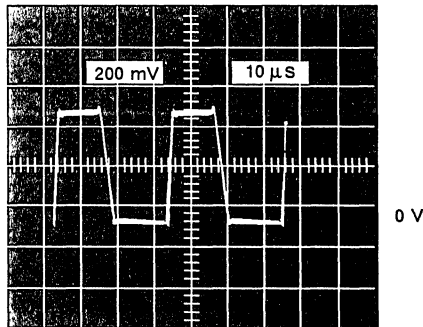
Figure 19. Unipolar Binary (current steering mode)



(a) No Compensation Capacitor  
(2 V/div)

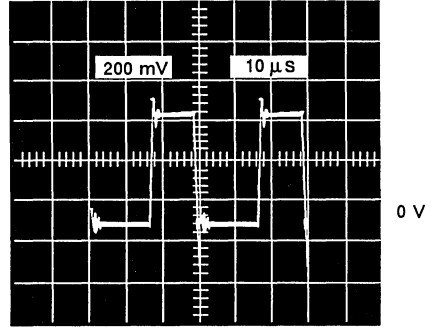


(b) Compensation Capacitor = 15 pF  
(2 V/div)

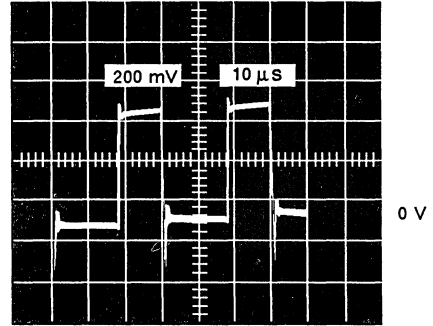


(c) Compensation Capacitor = 39 pF  
(2 V/div)

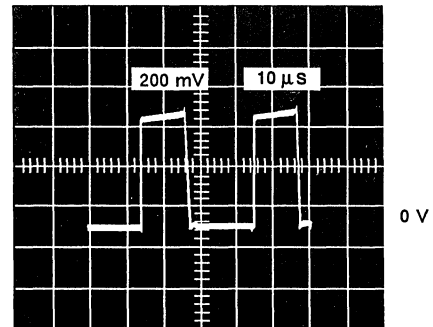
**Figure 20.** Unipolar Binary Operation Using OP-27  
(Slew Rate = 2.8 V/μs)



(a) No Compensation Capacitor  
(2 V/div)



(b) Compensation Capacitor = 15 pF  
(2 V/div)



(c) Compensation Capacitor = 39 pF  
(2 V/div)

**Figure 21.** Unipolar Binary Operation Using TL071  
(Slew Rate = 13 V/μs)

A disadvantage of unipolar current-steering DAC circuits is the requirement for opposite polarities of the reference voltage and the output. An advantage, however, is the low component count, which means the circuit is simpler and cheaper than a bipolar system.

**Bipolar Binary Operation.** There are three different coding possibilities for DACs in the bipolar mode: offset binary, two's complement, and sign and magnitude. In all of these systems, the MSB indicates the polarity. This design limits the resolution to 11 bits (i.e., 1 LSB is equivalent to  $(1/2048) V_{IN}$ ).

**Offset Binary Operation.** The relationship between the offset binary codes and the analog output is shown in Table 2. To calibrate the circuit shown in Figure 22, the digital inputs are first set to 0000 0000 0000. R1 may need to be adjusted to give the required output,  $VO = -V_{IN}$ . Next, the inputs are set to 1111 1111 1111, and R2 is adjusted for an output of  $VO = (2047/2048) V_{IN}$ . For best performance, R1 and R2 should be precision metal-film or wire-wound resistors with matched TCs (50 ppm/°C give best results as R1, R2, and R3). This circuit has two main disadvantages: a 2-step calibration procedure must be performed and the resolution is reduced to 11 bits.

Table 2. Offset Binary Code

Digital Input	Analog Output
1111 1111 1111	$+(2047/2048)V_{IN}$
1000 0000 0001	$+(1/2048)V_{IN}$
1000 0000 0000	0 V
0111 1111 1111	$-(1/2048)V_{IN}$
0000 0000 0000	$-V_{IN}$

**Two's Complement.** The two's complement is essentially the same as the offset binary coding, with the exception of the MSB, which is inverted. As shown in Figure 23, R1 is adjusted to give an output of  $VO = -V_{IN}$  for an input of 1000 0000 0000. R2 is then adjusted for  $VO = (2047/2048) V_{IN}$  with a digital word of 0111 1111 1111. This circuit has the same disadvantages as the offset binary bipolar circuit, that is, an 11-bit resolution limitation and a 2-step calibration procedure. Table 3 shows the relationship between the two's complement binary codes and the analog output voltages.

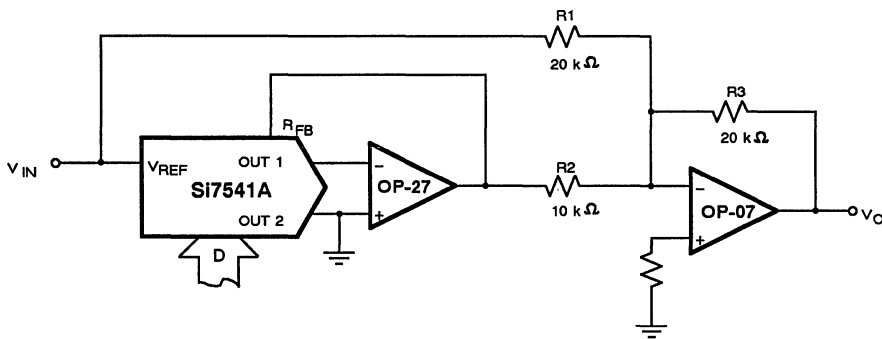
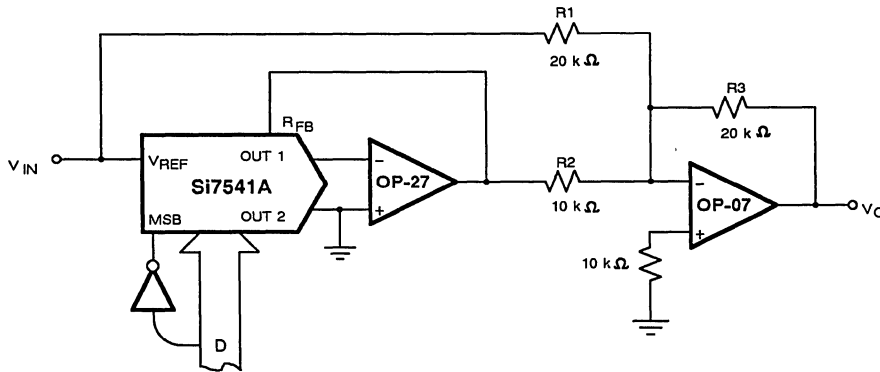


Figure 22. Offset Binary Configuration

**Table 3. Two's Complement Binary Codes**

Digital Input	Analog Output
0000 0000 0000	$-V_{IN}$
1000 0000 0000	0 V
1111 1111 1111	$2047/2048 V_{IN}$

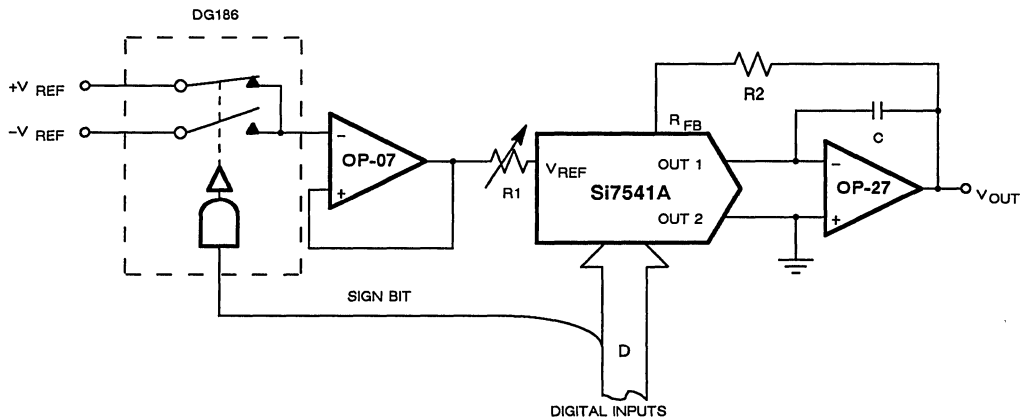


**Figure 23. 2's Complement Bipolar Configuration**

**Sign and Magnitude.** With this method of coding, the MSB is used to control an analog switch which selects either a positive or negative reference. The switch output must be buffered to ensure that any change in the  $t_{DS(ON)}$  of the switch does not affect the calibrated system (Figure 24).

calibration step (i.e. selection of R1). This step is the same as described for unipolar binary operation. Also, since the references are buffered, more than one DAC can be driven without a reference for each DAC. One disadvantage, of course, is that systems using a single DAC now need both a positive and a negative reference.

For the circuit shown in Figure 24, there is only one



**Figure 24. Sign and Magnitude Configuration**

## Voltage Switching Mode

A disadvantage of the current-steering mode is that the output impedance (capacitance and resistance) is a function of the digital word input. As mentioned earlier, a compensating capacitor is needed to ensure stability of the op amp. The value of this capacitor depends on the output impedance of the DAC which varies with digital input. The compensation capacitor must, therefore, allow for the worst-case, resulting in increased settling time and reduced bandwidth. In the voltage-switching configuration (Figure 25), this problem is avoided by using the  $V_{REF}$  pin as the output. The impedance seen at this pin is constant and independent of digital input.

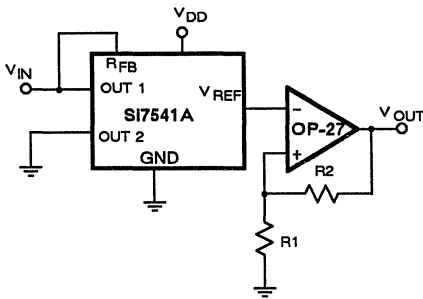


Figure 25. Si7541A In Voltage Switching Mode

The output of the Si7541A in the voltage-switching mode is a voltage of the same polarity as the reference. This mode enables a DAC system to operate from a single power supply, however, the DAC loses its multiplying abilities. The input  $V_{IN}$  must not fall more than 0.3 V below OUT2; otherwise, an internal diode will become forward biased. If not current limited, a large flow of current could result and the device could be destroyed.

Figure 26 shows the effect of supply voltage on differential non-linearity. The best results are obtained with higher supply voltages. The input voltage,  $V_{IN}$ , also affects the differential non-linearity (DNL) significantly because OUT1 and OUT2 are no longer at the same potential. As  $V_{IN}$  (OUT1) increases, the available  $V_{GS}$  for the NMOS switches connected to OUT1 is reduced, thus increasing the on-resistance of the switch. Since OUT1 and OUT2 are no longer at the same potential, the two NMOS switches in each 2R branch have a different on-resistance. The amount of current flowing in each branch now depends on the switch that is selected (i.e., the digital input), thus degrading the linearity. To minimize this effect, the

input voltage must be limited to approximately 2.5 V for a +15 V supply and 0.7 V for a +5 V supply.

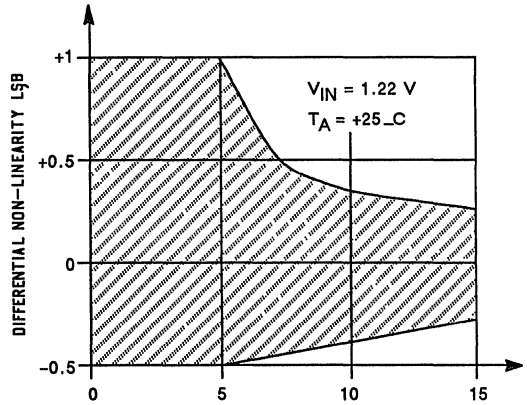


Figure 26. Differential Non-linearity vs. Supply Voltage

Output glitches due to digital switching are reduced for a DAC in this mode since OUT1 and OUT2 are connected to low impedance points and any parasitic capacitances will be discharged through these paths.  $R_{FB}$  is not used in this configuration, and the  $R_{FB}$  pin is usually tied to OUT1 to reduce any noise pickup.

Figure 27 shows a practical voltage switching DAC circuit. A buffer amplifier is needed between the reference and OUT1 to eliminate any variation in reference from the changing input resistance of the DAC. Gain is usually introduced at the output amplifier to achieve the desired full-scale output.

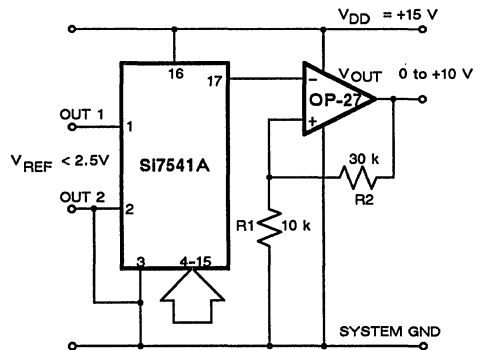


Figure 27. Operating the Si7541A from a Single Supply



In Figure 27, the negative supply for the op amp is connected to ground, and the output of the DAC ranges between 0 V and  $(4095/4096) R_{REF}$ . It is necessary, therefore, to use an amplifier which has a common-mode input range which includes the negative rail (in this case ground). Suitable amplifiers include the LM324, CA3130, and TLO91.

In some applications, it is possible to offset zero for single-supply operation, as shown in Figure 28. The output can be varied between  $V_2$  and  $[(4095/4096)V_1 + (1/4096)V_2]$ .

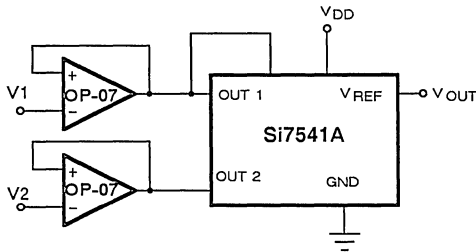


Figure 28. Offsetting Zero for Single Supply Operation

**Multiplication/Attenuation.** The Si7541A is useful as an analog multiplier or attenuator element. A signal applied at  $R_{REF}$  can be multiplied by a 12-bit digital fraction. Very little noise or distortion is introduced by

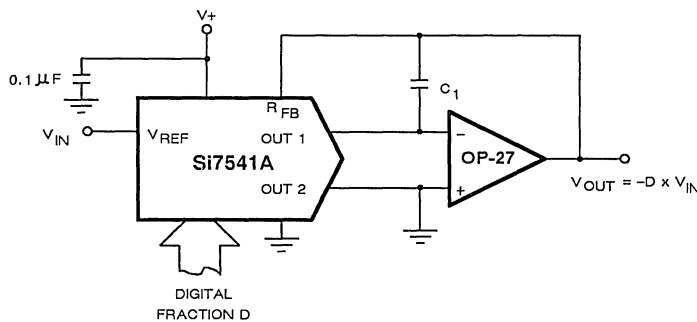


Figure 29. Attenuator Circuit

the DAC, since the attenuating network consists of well-matched thin-film resistors. Figure 29 shows a digitally controlled attenuator circuit.

The digital inputs can be used to select the amount of attenuation between  $(4095/4096) V_{IN}$  and 0 V. The maximum attenuation available is 4096:1 or 72 dB. Due to the current-to-voltage buffer, the output will be an inverted version of the input.

The low noise and distortion of this circuit makes it attractive for audio applications. The output amplifier, rather than the DAC, limits the frequency response, slew rate and amplitude of signal which can be passed. Table 4 shows the slew rate and frequency response for two different precision op amps.

Table 4. Slew Rate and Frequency Response

OP-AMP	SLEW RATE	MAX FREQ	
		-5 V to +5 V	-2.5 V to +2.5V
OP07	0.17 V/ $\mu$ s	10 kHz	5 kHz
OP27	2.5 V/ $\mu$ s	> 120 kHz	> 60 kHz

This attenuator circuit can be easily converted into a multiplier by using the output amplifier configuration shown in Figure 30. If the input and output must remain in phase, another inverting amplifier must be added to the output.

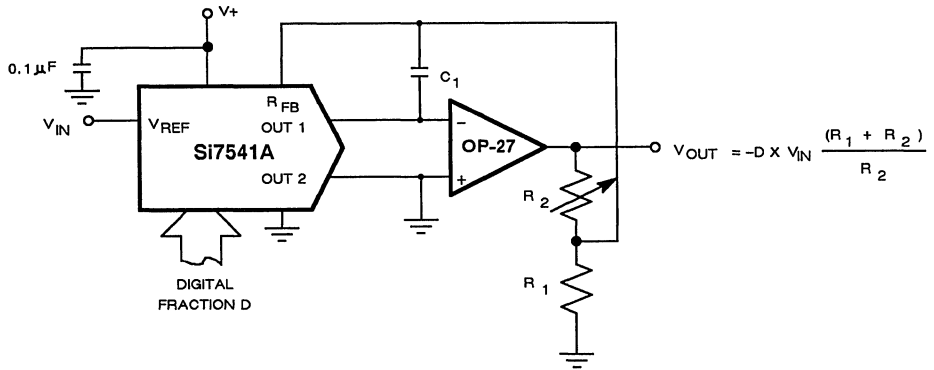


Figure 30. Multiplier Circuit

Triangle Wave Generator. In the triangle waveform generator circuit shown in Figure 31, a 12-bit counter is used to produce the digital inputs for the Si7541A. The MSB of the counter is used as a direction bit. When this bit is 0, the exclusive OR gates allow the other 11 outputs of the counter through to the DAC inputs. This condition gives a ramp of positive gradi-

ent from 0 V to  $+2047/2048 R_{REF}$  (assuming a negative reference) at the output of IC1. When the MSB = 1, the exclusive OR gates will invert the outputs of the counter, thus producing a ramp with negative gradient. Since the MSB is used as a direction indicator, this system has a resolution of 11 bits.

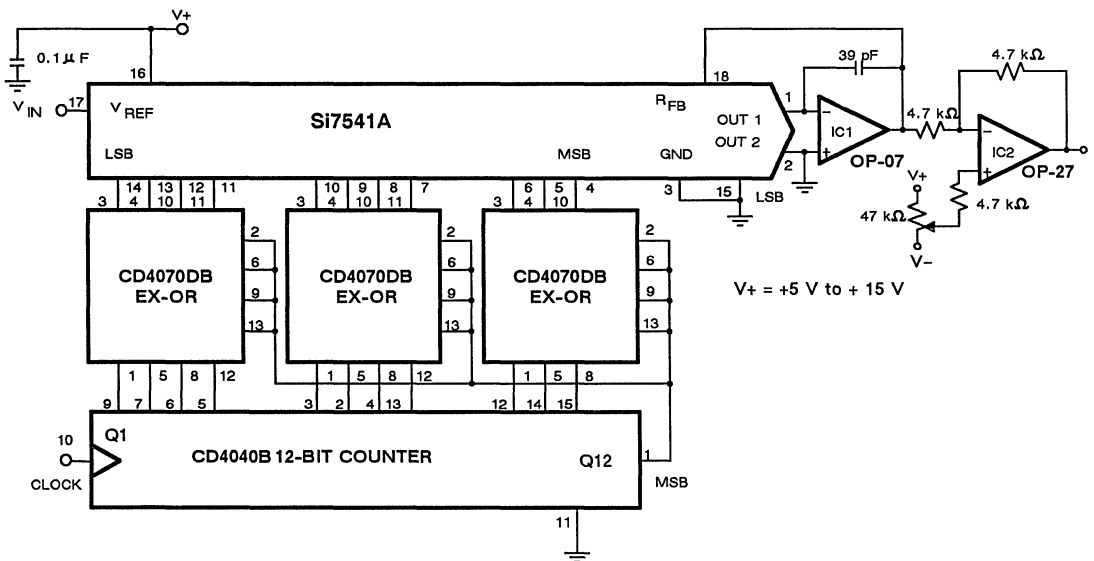


Figure 31. Triangle Wave Generator

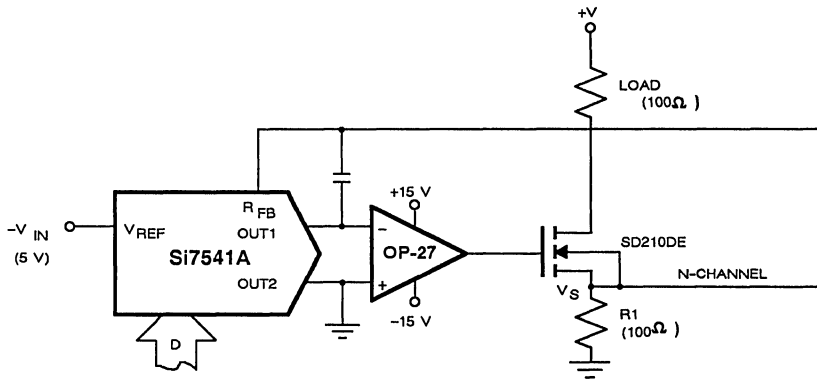


Figure 32. Programmable Current Sink

The frequency of the triangular wave is controlled simply by the clock frequency, and the amplitude of the signal is  $(1 - 2^{-11}) V_{REF}$ . IC2 can be used to both invert the polarity and to adjust the dc offset of the triangle if, for example, it must be symmetrical about zero.

**Programmable Current Sink.** A simple, yet accurate, programmable current sink can be obtained by using a small-signal MOSFET and a single resistor, as shown in Figure 32. The voltage,  $V_S$ , is determined by the product of the digital input fraction and the reference voltage (i.e.  $V_S = -D \times V_{IN}$ ). Also,  $R_{FB}$  is in parallel with  $R_1$ , since OUT1 is held at GND potential by the virtual ground of the output buffer amplifier. Voltage  $V_S$  is across this parallel resistance; therefore, the current drawn through the load is given by

$I = V_S (R_1 + V_{REF}) / (R_1 \times V_{REF})$ . Rewriting this in terms of  $V_{IN}$ ,

$$I = D \frac{V_{IN}}{R_1} \left( 1 + \frac{R_1}{R_{FB}} \right)$$

This equation can be approximated to  $I = (D \times V_{IN})/R_1$ , provided that  $R_1$  is small compared to  $R_{FB}$ . The ratio of  $R_1/R_{FB}$  determines the offset to this approximation. The maximum available current is limited by the potential drops across  $R_1$ , the MOSFET, and the load. For example, the circuit shown in Figure 32 is capable of 0 to 50 mA in steps of 12.2  $\mu$ A with a load of 100  $\Omega$ .

**Programmable Current Source.** Figure 33 shows a circuit for a programmable current source which is virtually a mirror image of the current sink circuit.

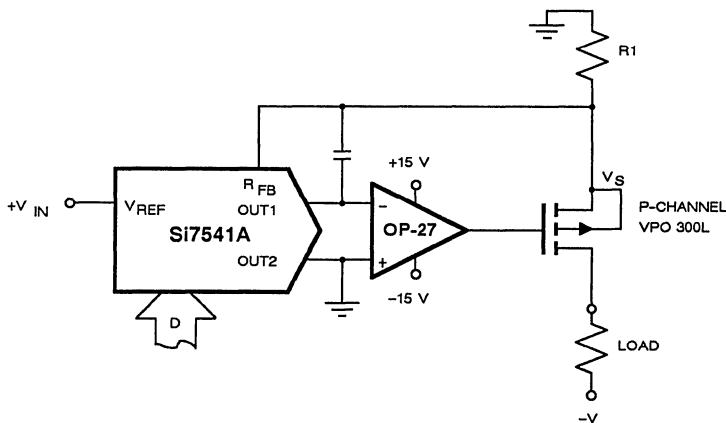


Figure 33. Programmable Current Source

**Programmable Gain Element.** The Si7541A can be configured as the feedback element of an op amp, as shown in Figure 34. In this circuit, the effective feedback resistance can be controlled by a 12-bit digital word. The output voltage is given by  $V_O = -V_{IN}/D$ , where D is a digital fraction. Therefore, the digital word 0000 0000 0000 is not permissible because it implies infinite gain. Care must be taken not to saturate the op amp when the digital input is small. At the other extreme, a 1111 1111 1111 input results in  $V_O = -(4096/4095) V_{IN}$ .

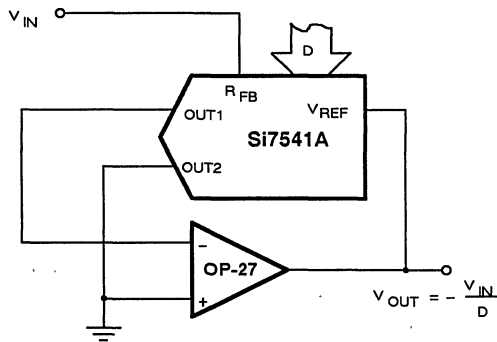


Figure 34. Si7541A as a Programmable Gain Element

**Analog-to-Digital Converters.** Several types of analog-to-digital converters (ADCs) can be easily implemented by using a DAC, a comparator, and a few logic components. The simplest is the counter ADC. This circuit uses a binary counter as the input to the DAC. A comparator compares the DAC output with the analog input signal and stops the counter when both reach the same level. The counter outputs constitute the digital word.

An improved ADC circuit is shown in Figure 35. The up/down counter controls the DAC. Based on the comparator output, the clock pulses increase or decrease the DAC output to reach the appropriate analog input voltage level.

Another popular converter is the successive approximation A/D. This circuit achieves conversion in 12 steps. The process begins by comparing the output produced by the MSB with the analog input. If it is less than  $V_{ANALOG}$ , the next bit is also turned on. If it is more, the MSB is turned off before the next bit is turned on. This process continues until all 12 bits have been weighted. In Figure 36 an Si2504 successive approximation register (SAR) controls the DAC. After 12 comparisons have been made, the digital output of the SAR produces the desired digital code. Figure 37 shows the Si7541A output during a typical conversion.

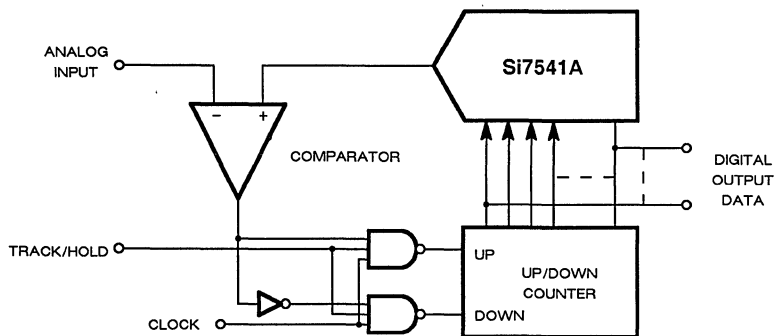


Figure 35. A 12-bit Tracking A/D Converter

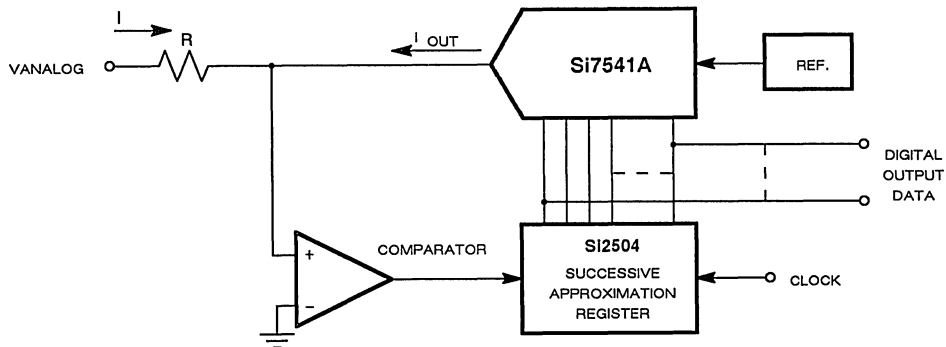


Figure 36. Successive Approximation A/D Converter

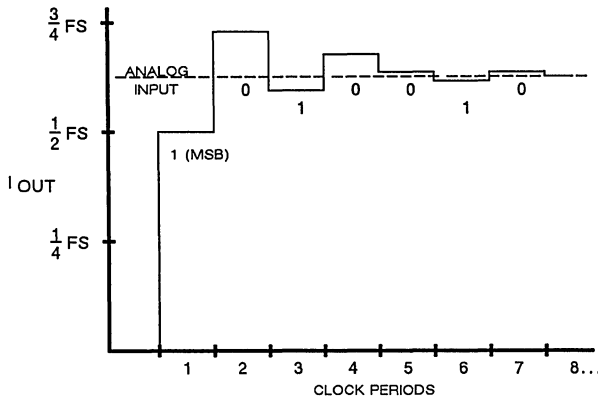


Figure 37. Si7541A Output for 12-Bit Successive Approximation Conversion

**CONCLUSION**

The general DAC operation theory presented in this application note is intended to support successful designs using the Si7541A 12-bit CMOS multiplying DAC. The capabilities of these designs will be enhanced by the improvements shown for the Siliconx Si7541A over similar products, especially in speed and dynamic performance. Example circuits and design hints have also been presented to assist the designer in using the Si7541A 12-bit DAC.

**REFERENCES**

- Dooley, Daniel. Data Conversion Integrated Circuits. New York IEEE Press, Wiley (1980).
- Loriferene, Bernard. Analog-Digital and Digital-Analog Conversion. London. Heyden & Sons Ltd. (1982).
- Analog-Digital Conversion Handbook, Third Edition. Analog Devices (1986).
- Burton, Phil. CMOS DAC Application Guide, Second Edition. Analog Devices (1986).

## APPENDIX: OTHER BASIC DAC PRINCIPLES

## Voltage References

The voltage reference provides an accurate voltage for generating binary-weighted currents. Any reference error reduces the overall system accuracy; therefore, the ideal references are characterized by accurate output voltages, low temperature drift, precise load and line regulation, and long-term stability.

**Zener References.** The least expensive reference devices are Zener diodes. Zener diodes produce a constant voltage drop when passing a constant current derived from a higher voltage. The active portion of a Zener diode is a reverse-biased p-n junction. In the forward-biased region, the diode acts much like a high-conductance silicon diode (Figure A1). In the reverse-biased region, little current flows if  $V$  is less than  $V_Z$ , the breakdown voltage. The small leakage current that flows is relatively insensitive to the magnitude of reverse voltage for fixed temperatures.

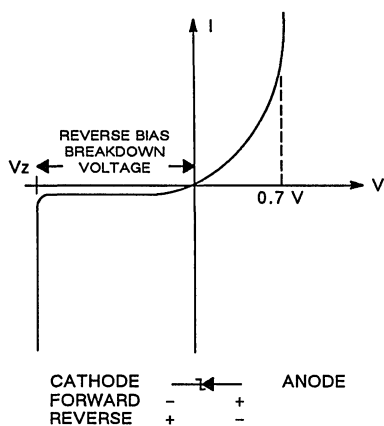


Figure A1. Zener Diode I-V Characteristic

As the reverse voltage approaches  $V_Z$ , the current increases rapidly. Therefore, Zener diodes are generally used in series with a resistor to limit the current or driven by a constant current source. These diodes provide voltage capabilities from 2 to 200 V with tolerances of 1% to 10% and power dissipations from 1/4 to 50 W.

Attractive as they seem as general-purpose voltage references, Zener diodes have many shortcomings. The voltage tolerance is generally poor, and they are

noisy and very sensitive to changes in current and temperature.

Zener diodes that breakdown in the 6-V range exhibit the best performance with very low TCs (+2 mV/°C) and relatively low sensitivity to current changes. They can be compensated by a  $V_{REF}$  (-2 mV/°C), as shown in Figure A2.

**IC References.** Monolithic ICs provide a more accurate reference (Figure A2). These devices usually include a temperature-compensated Zener diode driven by a constant-current source or a bandgap reference and a buffer output amplifier. These references provide an accurate output voltage that is virtually independent of input voltage, load current, temperature, and time. They provide voltage capabilities from 1.22 to 15 V with voltage tolerances from 0.05% to 5%, drifts of 0.5 to 100 ppm/°C, and current ranges from 400  $\mu$ A to 200 mA.

For most of these integrated circuits, the output voltage has been established by trimming ultrastable, low-temperature drift thin-film resistors under circuit operating conditions. These devices are usually short-circuit protected in both the current-sourcing and sinking directions. Table A1 illustrates some of the most popular reference voltages available.

Table A1: Typical Reference Output Voltages

Reverse Breakdown Voltage -- $V_R$ (volts)					
1.22	5.0	7.50	1.24	to 5.3,	Adjustable
1.235	6.2	10.00	5	to 15,	Adjustable
2.49	6.9	10.24	-5	to -15,	Adjustable
2.5	6.95				

**Band Gap References.** A popular voltage reference for monolithic circuitry is the "band gap" reference, which is based on an inherent physical property of the base-emitter voltage in a forward-biased silicon transistor. The  $V_{BE}$  of a silicon transistor at absolute zero (-273°C) is 1.205 V. This value is the band gap voltage of silicon at 0 °K. By amplifying the difference between the  $V_{BE}$  values of similar transistors operating at different current densities, it is possible to obtain a constant 1.205 V at any temperature.

Bandgap reference circuits are based on the circuit shown in Figure A3. For the proper ratio,  $R1/R2 V_Z = 1.205$  V. This, in turn, is amplified by the ratio  $(R4/R5 + 1)$  to give the desired output voltage. Low-TC thin-film resistors may be laser or zener-zap trimmed to increase accuracy.

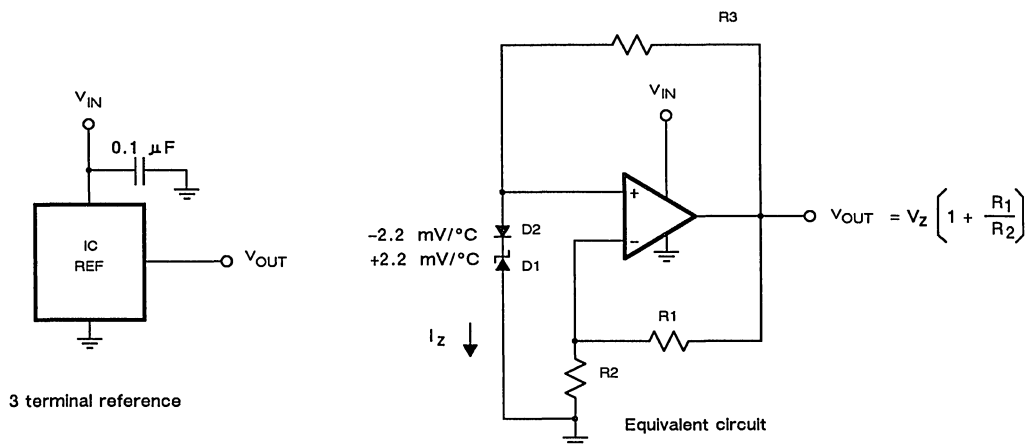


Figure A2. IC Reference

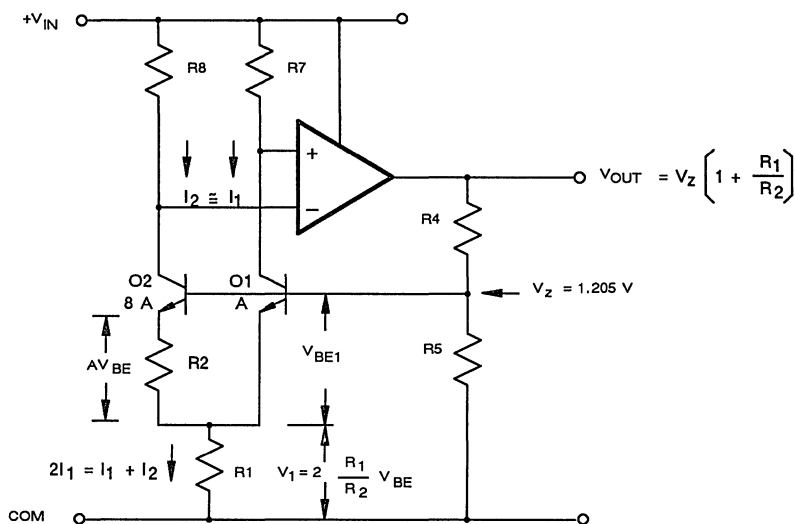


Figure A3. Bandgap Reference Regulator

Bandgap references operate from low-voltage supplies (typically  $V_{OUT} = +2 \text{ V}$ ) and have an order of magnitude lower output impedances than low-voltage Zener diodes. Bandgap references are low cost, but their output voltage usually must be buffered. In this case, the offset voltage drift of the buffer op amp must also be considered.

**Buried Zener Diodes.** Zeners have been produced in ICs using the reverse-biased breakdown voltage of the base-emitter junction of a vertical NPN transistor. This pn junction occurs at the surface of the device where breakdown may be affected by crystal imperfections, mobile charges in the oxide, and other forms of contamination. These effects cause noise and long-term stability problems.

In a buried Zener, breakdown occurs well below the surface, thus avoiding surface effects. Long-term stability of 50 ppm/year are achieved. However, because the diffusion process is less controlled under the surface, there is a greater spread in breakdown values and TCs. Therefore, the circuits are generally designed to allow trimming. Typical accuracies better than 0.1% and TCs in the order of +10 ppm/°C are achieved.

Temperature-compensated buried-Zener references usually have lower noise than bandgap references and are recommended for high-resolution applications.

Temperature-Stabilized References. To improve temperature stability in IC references, on-board heaters may be used to hold the reference elements at a constant, elevated temperature. With this approach, +1/2 ppm/°C TCs are attainable. The heater can draw hundreds of mA, making this type of device incompatible with low power systems.

## Forming DACs with Resistance Ladders

To reduce the number of resistors and their resistance range, a configuration may be used that pro-

vides a suitable attenuation, such as the one shown in Figure A4. The Si7541A is implemented using an R-2R resistance ladder.

This circuit consists of four binary-scaled resistor values for each group of 4 bits, with an attenuation of 16:1 to each successive quad. This scheme can be used for BCD conversion by using a 10:1 attenuation between quads. Furthermore, this approach can be used to design the R-2R ladder circuit illustrated in Figure A5. Most CMOS DACs are based on this circuit. The feedback resistor is integrated on-chip to track the resistance of the ladder independently of ambient temperature changes.

When only the MSB is turned on, the current contributed to the summing node, by the MSB switch, is  $I_1 = V_{REF}/2R$ . The output voltage is  $V_{OUT} = -(R/2R)V_{REF}$ . For the second bit,  $I_2 = V_{REF}/4R$ , and if only bit 2 is on,  $V_{OUT} = -(R/4R)V_{REF}$ . Continuing down the ladder, each 2R resistor passes one-half of the current. The output voltage is proportional to the sum of all the binary-weighted currents that are switched to the OUT1 node.

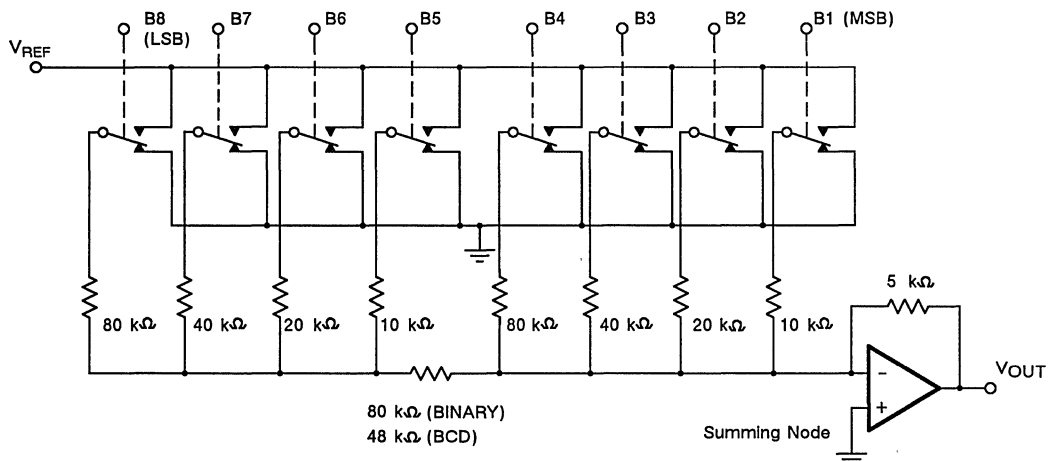


Figure A4. 8-Bit DAC using two equal-resistance quads



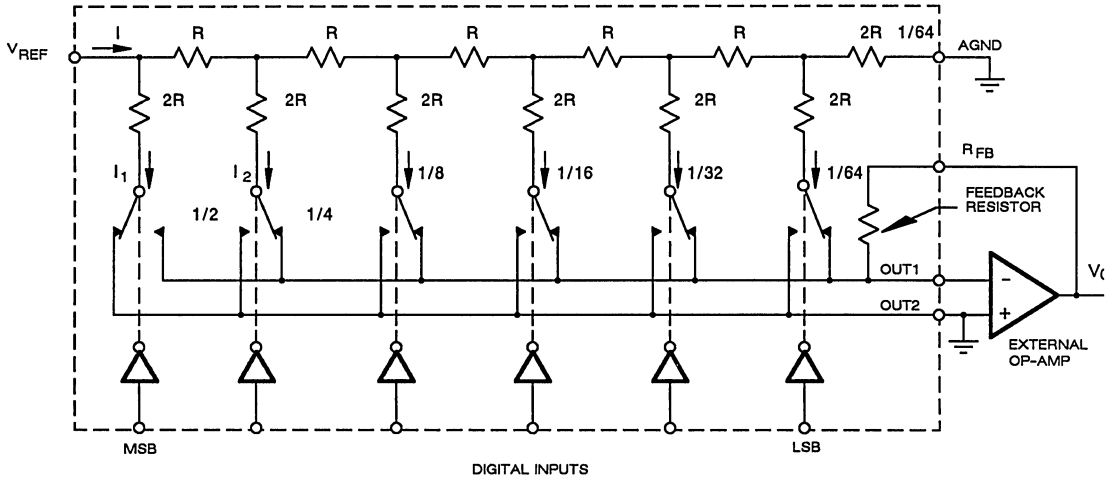


Figure A5. Current-steering DAC Using an R-2R Ladder

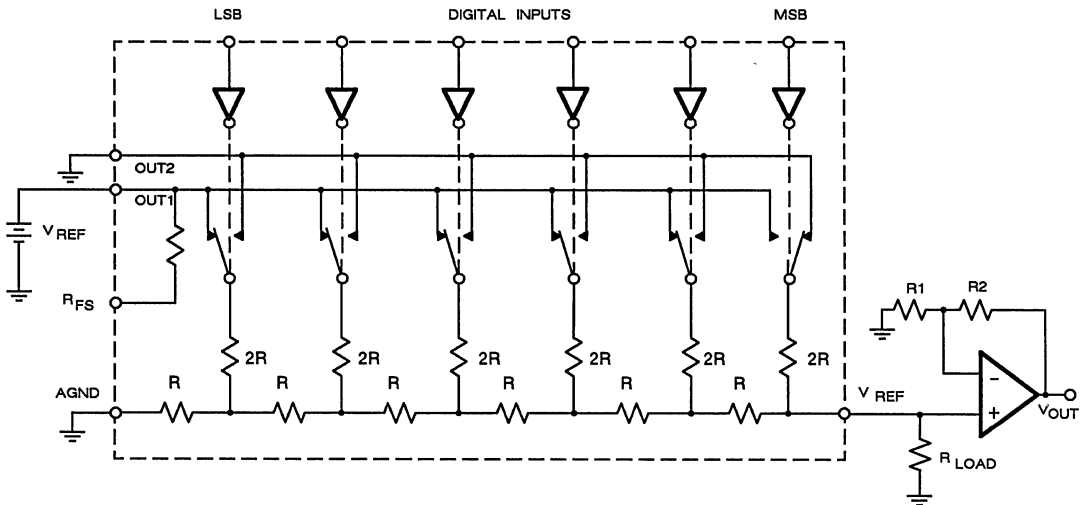


Figure A6. DAC in the Voltage Switching Mode

In CMOS DACs, the analog switches are always very close to the ground potential (within the  $V_{OS}$  of the amplifier) and the thin-film resistors are isolated from the substrate. Therefore,  $V_{REF}$  can be either positive or negative, and the device can be used with ac input signals. This operation is called multiplying.

OUT1 terminals as shown in Figure A6.

The OUT1 terminal is driven by a low-impedance reference voltage source, and the  $V_{REF}$  terminal is connected to a high-impedance load, such as the input to an operational amplifier. The reference voltage source must be bypassed to minimize the variable load and charge injection effects introduced by the DAC switches.  $R_{LOAD}$  should be more than  $4096 \times R_{OUT}$  to prevent a 0.5 LSB full-scale error.

The R-2R ladder can also be used to produce a non-inverted output voltage by swapping the  $V_{REF}$  and

The output of this circuit follows the equation:

$$V_{OUT} = D \times \frac{1 + R2}{R1} \times V_{REF}$$

where

$$D = B1/2 + B2/4 + \dots + Bn/2^n$$

The numerator of each partial fraction is the value "0" or "1" corresponding to the logic state of each digital input. Generally, the magnitude of  $V_{REF}$  is limited due to the nature of the switching elements used. The reference voltage must be less than 2.5 V to reduce the effect of unequal  $V_{GS}$  applied to the OUT1 vs. the OUT2 switches ( $\tau_{DS(ON)}$  variations).

## Switching

Switching may be performed in either voltage or current modes. The analog switches can be bipolar, CMOS, or NMOS, depending on the technology used. Each technology has advantages and limitations. Important switch characteristics that affect DAC performance are switching speed, charge injection, on-resistance, and parasitic capacitances. These characteristics play a role in determining performance such as conversion speed, accuracy, and glitching.

In the current mode (Figure A5), each leg of the ladder conducts the same current regardless of switch position. The current output is changed to a voltage output by the external operational amplifier. This circuit is simple, its constant input resistance facilitates good performance of the reference source, and it can be used for 4-quadrant multiplication. However, it can present linearity problems due to modulation of the op amp offsets caused by the code dependent output resistance. The dynamic response is slowed

down by switch capacitances, and glitches are created from charge injection coupling from the switch drivers.

In the voltage-switching mode (Figure A6), the ladder is used as aggressive attenuator, and the switches alternate between a low impedance reference voltage source and ground. The currents flowing through each switch change with the input codes. Their magnitude is not as important as the reference source ability for maintaining a fixed input voltage as the codes change. In most cases, it is necessary to decouple the reference with the parallel combination of a 10  $\mu$ F tantalum and a 0.01  $\mu$ F ceramic capacitors (see Figure A7).

The constant resistance seen by the op amp input eliminates linearity errors caused by modulation of the amplifier's offset voltage. Additionally, since the output capacitance is less and the switch transients are coupled to low impedance points, the voltage-mode circuit results in cleaner and faster response to digital code input changes. Since the output voltage has the same polarity as the reference, it is possible to operate the whole circuit from a single power supply. Finally, only a single operational amplifier is needed for bipolar digital-offset binary or two's complement operation. The accuracy is satisfactory for low values of  $V_{REF}$ , but since the  $\tau_{DS(ON)}$  of the MOSFET switches is modulated by the magnitude of the reference voltage, large values of  $V_{REF}$  can produce considerable linearity errors. Additionally, negative voltage references are not allowed in the voltage mode because a parasitic pn junction to ground will be activated, leading to possible destruction of the DAC if current is not limited.

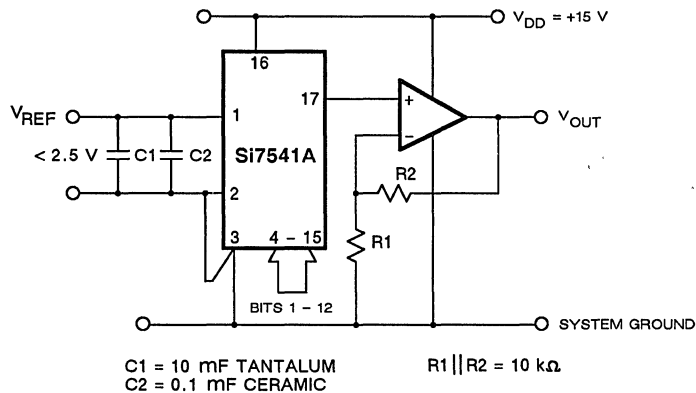


Figure A7. Single Supply Operation Using Voltage Switching

## EFFICIENT ISDN POWER CONVERTERS USING THE Si9100

By James Blanc  
June 15, 1987

One of the latest technology revolutions, an integrated worldwide telecommunications network, will be accompanied by another advance in power conversion technology. The integrated services digital network (ISDN) will allow different forms of information (voice, computer data, video, facsimile, etc.) to be transmitted over the telephone network. The International Consultative Committee for Telephone and Telegraph (CCITT) has proposed standards for the interfaces required to implement ISDN. Although the standards have yet to be formally adopted, telecommunications companies are moving ahead with pilot test programs, and semiconductor makers are developing chip sets to build ISDN hardware. Every network terminator (NT), signal regenerator (RG), and terminal equipment (TE) unit used for the implementation of ISDN will require a power converter.<sup>[1]</sup>

A major requirement of these telecom applications (due to the need for emergency-mode operation from a high-impedance source) is high-efficiency energy conversion at fractional-watt power levels. Minimization of parts count, another key factor for the design of these power converters, is sought to simultaneously achieve low cost and high reliability.

D/CMOS integrated circuit technology is ideally suited for the power requirements of ISDN. The analog and digital logic functions needed for pulse-width modulation can be implemented in CMOS to minimize quiescent current to the controller. DMOS transistors provide high-voltage power switching with both very low dynamic and gate drive losses. Integration of the CMOS controller on the DMOS power device yields the best overall performance at the lowest cost and component count.

### Design Objectives

While some differences exist between designs, there are several requirements in addition to efficiency which are common to ISDN power converter applications. These include:

- reliable start-up and operation from the high source impedance of telephone subscriber lines (U-interface only)
- current limiting to prevent failure of other network terminals when one power converter output is shorted (S-interface only)
- a free-running internal oscillator for start-up as well as independent operation, which can be synchronized to an external clock signal
- electromagnetic interference (EMI) filtering to limit conducted emissions during both start-up and normal operation, as well as during equipment connections and disconnections.

The Si9100 power IC facilitates compliance with these design requirements with a minimum number of external parts. To illustrate this capability, a discontinuous conduction mode (DCM) flyback converter was built and tested. Measured efficiency was greater than 80% for a wide range of loads, and 60% efficiency was achieved with only a 15-mW load. Before describing the circuit concepts in detail, it is instructive to note the main features of the ISDN power-feeding concept which has been endorsed by the CCITT.

### ISDN Power Feeding

Figure 1 is a block diagram of the ISDN basic access configuration. The two-wire transmission line defined at the U-interface provides a 192k-bits-per-second (bps) digital data path which connects subscriber equipment to the local telephone exchange. Although ISDN permits many new services to be offered, the basic service of voice transmission remains a vital function. Therefore, the network power feeding from batteries in the local telephone exchange remains an essential part of modern telephone system planning. The network terminal (NT) connects the local loop, called the S-bus, to the U-interface at the customer's premises. ISDN-compatible terminals (TE1) communicate at a standard 64k-bps rate over the four-wire S-bus. Non-ISDN-compatible terminal equipment (TE2), such as analog phones, must connect to the S-bus via a terminal adapter (TA).

To minimize noise-coupling problems, the S-bus must be galvanically isolated from the two-wire U-interface. The CCITT recommendations call for an off-line power converter in the NT to supply 4 W at 40 V

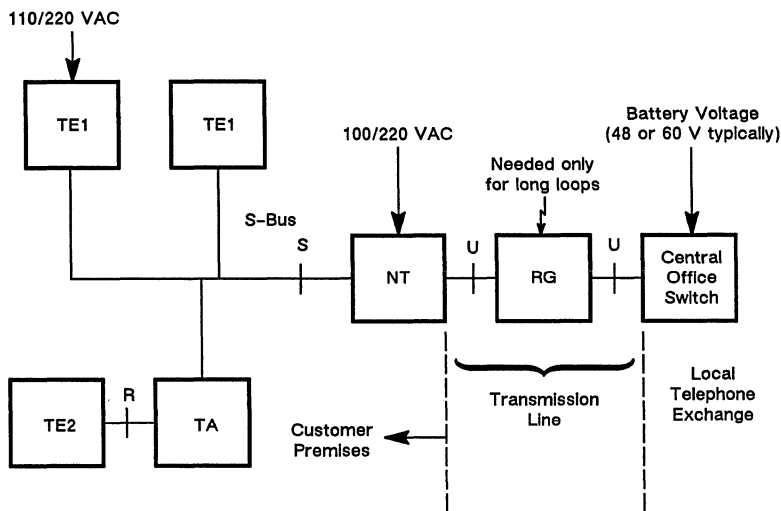


Figure 1. ISDN Basic Access Configuration

nominal to the S-bus during normal operation (for up to four telephones with full features). Other terminal equipment (e.g., fax terminals) would be fed solely from local ac power lines. In the event of a power outage, one telephone at the customer premises must be fed from the central office battery. This procedure is accomplished by reversing the voltage polarity on the S-bus. Non-priority terminals have a diode input which isolates them during emergency-mode operation. A single telephone terminal is fed via a full diode bridge, allowing it to operate during the emergency.

A signal regenerator may be required for long loops (U-interface). The Deutsche Bundespost (DBP) proposes to increase the feeding voltage from 60 V to 93 V to compensate for voltage drops on long lines requiring signal regeneration. The standard telephone line voltage used in many other parts of the world is 48 V. Whatever the voltage, the problem for power converters connected to telephone subscriber lines remains the same—they are fed from a high-impedance source.

### Source Impedance Effects

The impedance of telephone subscriber lines limits the amount of power that can be supplied to the load. Referring to Figure 2, for a battery voltage,  $V_S$ , and line resistance,  $R_S$ , the maximum power to the converter is given by Equation 1, since the power

limit occurs when source and load impedances are equal.

$$P_{MAX} = \frac{V_1^2}{R_e} = \frac{(V_S/2)^2}{R_e} = \frac{V_S^2}{4R_e} \quad (1)$$

$R_e$  is defined as the effective low-frequency input impedance of the power converter.

For a flyback converter, with waveforms as shown in Figure 3, the calculation of the low-frequency input impedance is straightforward. The coupled inductor is designed to ensure operation in the discontinuous conduction mode (DCM). This operation requires that the core flux be reset to zero during each cycle. The current is zero at turn-on and ramps up at a rate given by  $di/dt = V_1/L_p$ . The maximum value of the peak primary current,  $I_{pk}$ , is

$$I_{pk} = \frac{di}{dt} (t_{ON(max)}) = \frac{V_1}{L_p} \frac{t_s}{2} \quad (2)$$

The 50% maximum duty ratio imposed by the Si9100 controller limits the "on" time of Q1 to one-half of the switching period. The average value of the current waveform in Figure 3 is the dc current in the inductor,  $L_1$ . The current ripple in  $L_1$  is small, and the average inductor current,  $I_{DC}$ , during start-up is one-fourth the peak current value, as given by

$$I_{DC} = (I_{pk}/2) (D_{(max)}) = I_{pk}/4 \quad (3)$$

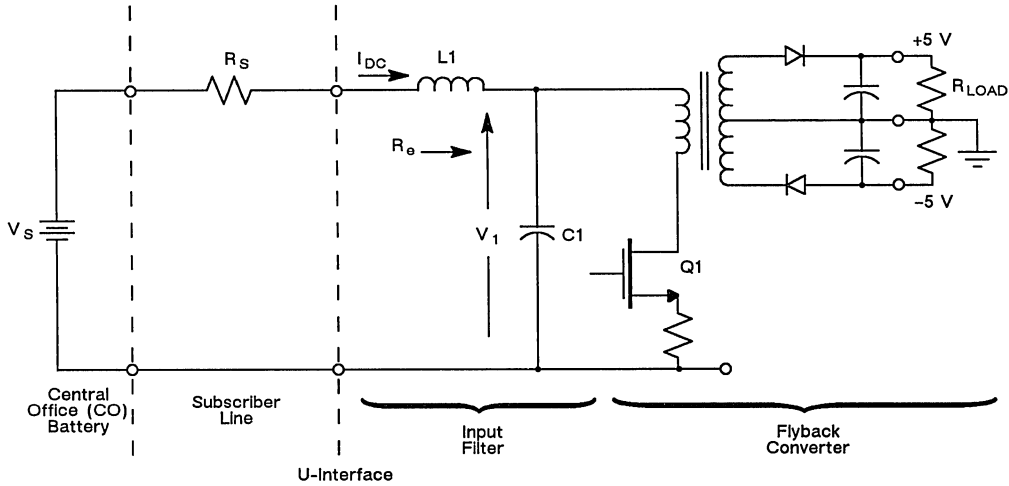


Figure 2. Power Converter with High Source Impedance

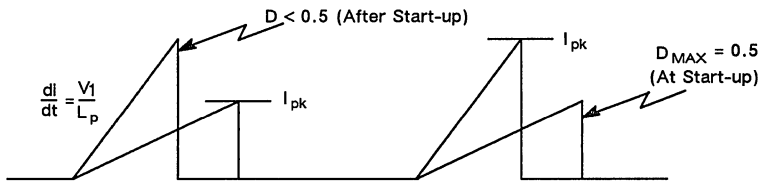


Figure 3. Primary Side Current Waveforms

Substituting this result into Equation 2 gives  $R_e$  in terms of the primary inductance,  $L_p$ , and switching frequency,  $f_s$  ( $f_s = 1/T_s$ ).

$$R_e = \frac{V_1}{I_{DC}} = 8 L_p f_s \quad (4)$$

$L_p$  effectively acts as a current limiter during start-up, thus eliminating the need for active current limiting circuitry. The value of  $L_p$  must be chosen between a minimum value, which sufficiently limits start-up current, and a maximum value, which permits the rated throughput power to the load. Assume, for example, the maximum load condition given in Table 1.<sup>[2]</sup> The input power to the converter is the output power divided by the efficiency.

$$P_{IN} = P_O/h = \frac{0.650}{0.80} = 0.813 \text{ W} \quad (5)$$

Worst-case efficiency at maximum load is assumed to be equal to 80%. The input power to the converter is given by

$$P_{IN} = 1/2 L_p I_{pk}^2 f_s \quad (6)$$

As seen from Figure 3, if  $L_p$  is doubled,  $I_{pk}$  is reduced by half. Therefore,  $P_{IN}$  varies in inverse proportion to  $L_p$ . Referring again to Figure 1, the dc analysis of the input characteristics gives

$$V_1 = V_s - I_{DC} R_s \quad (7)$$

Table 1. ISDN Power Requirements

OPERATING MODE	LOAD			MEASURED EFFICIENCY
	+5 V CURRENT	-5 V CURRENT	OUTPUT POWER	
Normal -- Active	100 mA	30 mA	650 mW	87%
Normal -- Power Down	11 mA	3 mA	70 mW	79%
Emergency -- Active	55 mA	9 mA	320 mW	88%
Emergency -- Power Down	3 mA	0 mA	15 mW	60%

Equations 2, 6, and 7 can be combined to give a quadratic equation which yields the maximum and minimum values for  $L_p$ . A graphical approach, however, gives the same answer and, at the same time, provides more insight into system behavior. After start-up has occurred, the power converter no longer presents a constant impedance at the input terminals. Instead, a constant power characteristic pertains, given by

$$P_{IN} = (V_1) (I_{DC}) = \text{constant} \quad (8)$$

The demonstration flyback converter was designed to operate from a battery voltage of 48 V and a maximum line resistance of 600  $\Omega$ . The constant power

curve for  $(V_1) (I_{DC}) = 0.813$ , with the load line defined by  $V_S = 48$  V and  $R_S = 600$   $\Omega$ , are plotted in Figure 4. The intersection of the load line with the constant power curve determines two operating points, A and B, which occur at  $(V_1, I_{DC}) = (14.6$  V, 55.7 mA) and (33.4 V, 24.3 mA). If  $V_S$  is slowly increased from zero,  $V_1$  and  $I_{DC}$  increase along the line, whose slope is  $R_e$ , from the origin to the constant power curve. This analysis is an oversimplification since a step increase in voltage is more likely to occur at power-up. However, worst-case start-up conditions occur at maximum  $R_S$ , which guarantees that the input filter is heavily overdamped. Therefore, the increase in  $V_1$  is monotonic, and the results of the simplified analysis are valid.

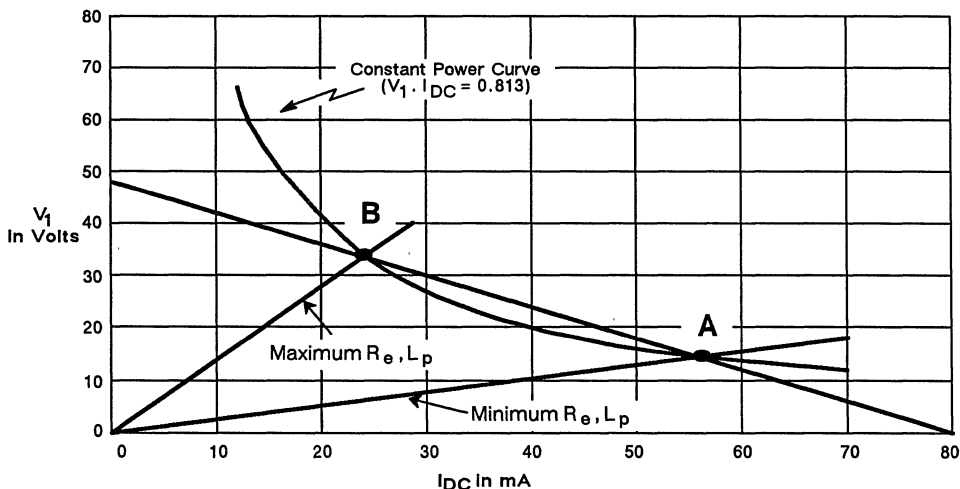


Figure 4. Flyback Converter Operating States

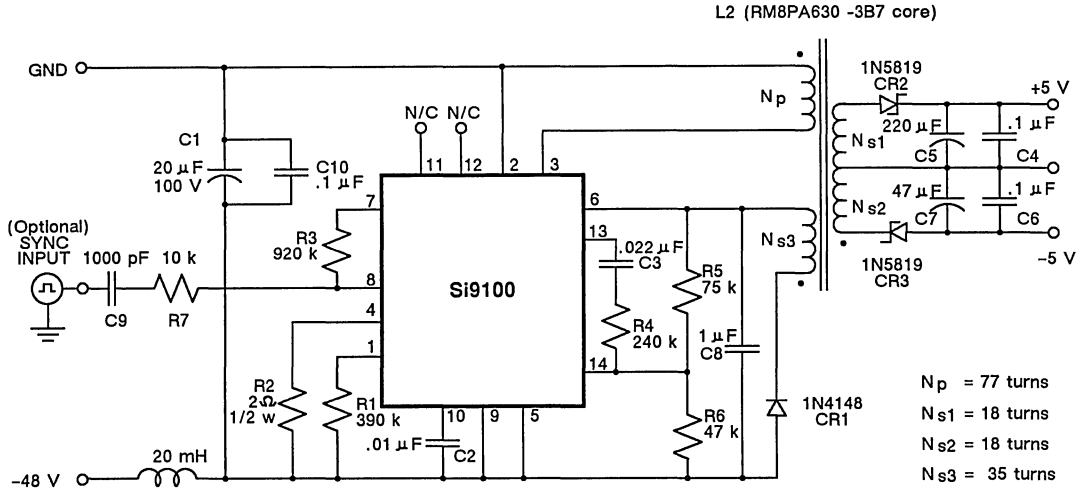


Figure 5. ISDN Flyback Converter

The lines from the origin to points A and B define the minimum and maximum values for  $R_e$ , and with Equation 4, also determine the limits for  $L_p$ .

$$R_e(\text{min}) = 14.6/0.0557 = 263 \Omega$$

$$R_e(\text{max}) = 33.4/0.0243 = 1.37 \text{ k}\Omega$$

For a switching frequency design value equal to 20 kHz, Equation 4 gives

$$L_p(\text{min}) = 1.64 \text{ mH}$$

$$L_p(\text{max}) = 8.65 \text{ mH}$$

$L_p$  may be chosen near the upper end of the permissible range for maximum start-up current limiting, or it may be chosen for maximum power transfer on a high-resistance line. Setting  $R_e = R_s = 600 \Omega$  for maximum power transfer gives

$$L_p = R_e/8f_s = \frac{600}{(8)(20,000)} = 3.75 \text{ mH}$$

The latter approach was chosen for the demonstration converter (see schematic in Figure 5). The Si9100 functional diagram is given in Figure 6 for reference.

### Converter Performance

Measured efficiency data for the flyback converter is given in the last column of Table 1. Most notable is

the 60% efficiency at a load of only 15 mW, which is allowed by the low quiescent current requirement of the CMOS control circuitry in the Si9100. Although power converters can operate at much higher frequencies, the dynamic losses incurred reduce the efficiency during the power-down state. The switching speed (30 ns typical) of the DMOS output transistor in the Si9100 permits operation above audible frequencies with very low dynamic and drive losses. Such performance cannot be achieved with bipolar transistors. A single resistor, R3, sets the oscillator frequency at approximately 34 kHz. A positive sync pulse (5 V amplitude and 0.5 µs pulse width) at 40 kHz was fed through R7 and C9 to pin 8 to demonstrate the principle of synchronization with an external clock. Typically, the free-running frequency should be set at 10 to 20% below the external clock frequency (note that the switching frequency is 1/2 of the oscillator frequency).

Start-up characteristics were verified by connecting a 600-Ω resistance from a dc power supply to the converter input terminals. Reliable start-up was demonstrated at maximum load for supply voltages as low as 44 V. With zero source resistance inserted in the line, the converter maintained regulation down to an input voltage of 23 V. In both cases, the maximum operating voltage is 70 V for the Si9100. The inductor, L1, was wound with 540 turns of #32 magnet wire

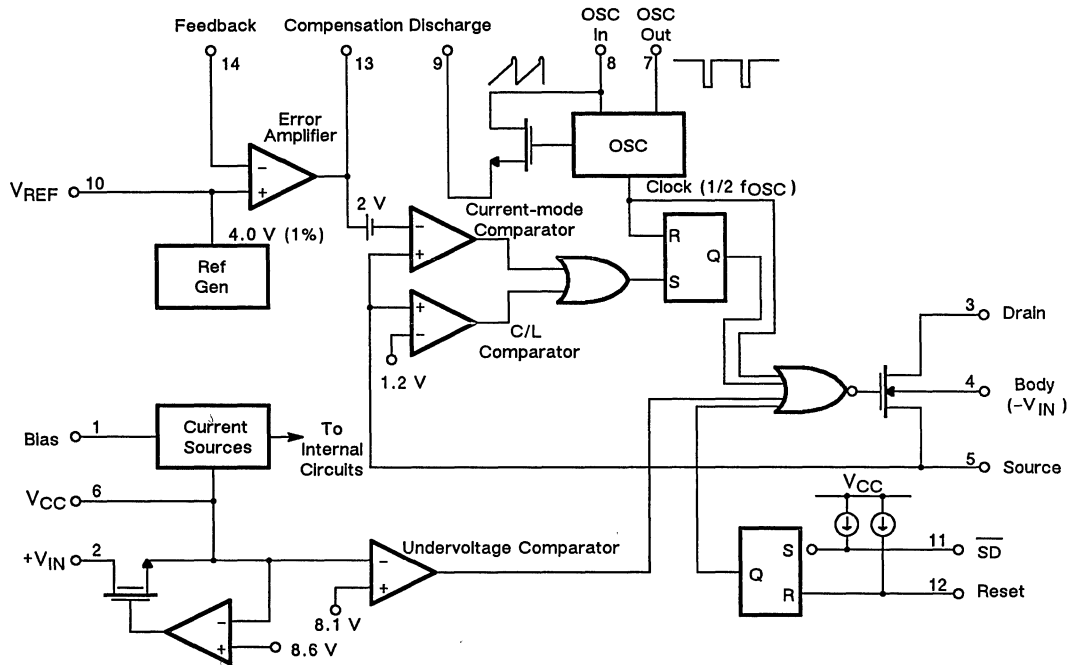


Figure 6. Si9100 Functional Diagram

on a #55206 molypermalloy powder core. The relatively high series resistance of this inductor (6  $\Omega$ ) provides series damping of the input filter. This damping reduces peaking of the filter output impedance, preventing degradation of the control loop response at the filter resonant frequency when the supply is operated from a low-resistance source.

Measured ripple on both outputs was less than 50 mV peak to peak, and regulation was better than 5% over line and load. The  $-5\text{-V}$  output increases from  $-5.05\text{ V}$  to  $-5.75\text{ V}$  when totally unloaded.

The current-mode controller of the Si9100 provides fast current-limiting response in the event of a shorted output. With either output shorted to ground, the measured value of short-circuit current drawn at the converter input was 30 mA. Any output terminal can be shorted for an indefinite period with no resulting high stress condition on the Si9100. Normal operation resumes when the short circuit is removed.

The input filtering provided by L1 and C1 provides a calculated attenuation of 68 dB at the fundamental of the switching frequency. This allows compliance with FCC Class B and VDE-0871/B requirements; however, conformance testing to these specifications was not performed. Common-mode noise coupling is minimized by the Si9100 since the MOSFET drain is electrically isolated from the package case (a 14-pin DIP). Therefore, very little parasitic capacitance exists from drain to ground. Since the Si9100 places both the driver and MOSFET on the same chip, gate driver lead lengths are reduced from a few centimeters for discrete designs to a few hundred microns.

The 5-mA/ $\mu\text{s}$  dynamic current limit required during connection of equipment to the S-bus<sup>[3]</sup> is met by selecting a suitably high value, 20 mH, for L1. Since several ohms of series resistance is desired, a small wire gauge is used and the inductor is not prohibitively large. A smaller value may be chosen for L1 where the EMI requirements are less critical.



## Summary

D/CMOS power IC technology is ideally suited for the requirements of low-power dc/dc converters, such as those required for the implementation of ISDN. A circuit design for an 85%-efficient power converter using the Si9100 SMARTPOWER IC has been presented here. Measured performance data is given, along with a graphical analysis method for ensuring reliable start-up when power is fed from a high-impedance source.

## References

1. Rosenbaum, D. and K.H. Stolp. "The Feeding Conception of the ISDN Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct.14-17, 1985, 505-512.
2. Sigloch, R. "Requirements for Small High Efficiency DC/DC Converters in Complex Communication Networks," IEEE INTELEC Conference Proceedings, Toronto, Canada, Oct 19-22, 1986, 197-202.
3. Krautkramer, W. and B. Schickling. "Remote Power Feeding of ISDN-Terminals at the Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct. 14-17, 1985, 513-519.

## A 1-WATT FLYBACK CONVERTER USING THE SI9100

James Blanc  
March 1987

The Si9100 is a monolithic D/CMOS SMARTPOWER IC which combines high-efficiency CMOS logic, a high-voltage switching transistor and high-voltage pre-regulator on a single die. It is the first low-cost, high efficiency regulator designed to operate directly from unregulated high-voltage DC power sources in areas such as telecommunications and avionics. The primary application will be in feature phones and ISDN terminals to power the logic components without exceeding the load limits set by the telecommunications industry. Power integrated circuit technology allows low-power CMOS control circuits to be combined with DMOS power transistors in the Si9100. The resulting reduced parts count decreases system cost, improves reliability, and simplifies circuit design.

The flyback converter presented here uses the Si9100 to provide an isolated  $\pm 5$  V supply rated at 1 W. Specifications for this supply are as follows:

Input Voltage . . . . . 15 to 70 VDC

Output Voltages

Maximum load . . . . . +5 V @ 167 mA,  
-5 V @ 33 mA

Minimum load . . . . . +5 V @ 32 mA,  
-5 V @ 8 mA

Regulation . . . . .  $\pm 5\%$

Maximum Ripple . . . . . 100 mV p-p

Switching Frequency . . . . . 100 kHz

Efficiency . . . . . 80% min for 1.0 W load  
75% min for 0.2 W load

A schematic for the flyback converter is found in Figure 1, with a parts list provided in Appendix B. However, before discussing the details of the power supply design, it is instructive to review the functions of the Si9100 integrated circuit.

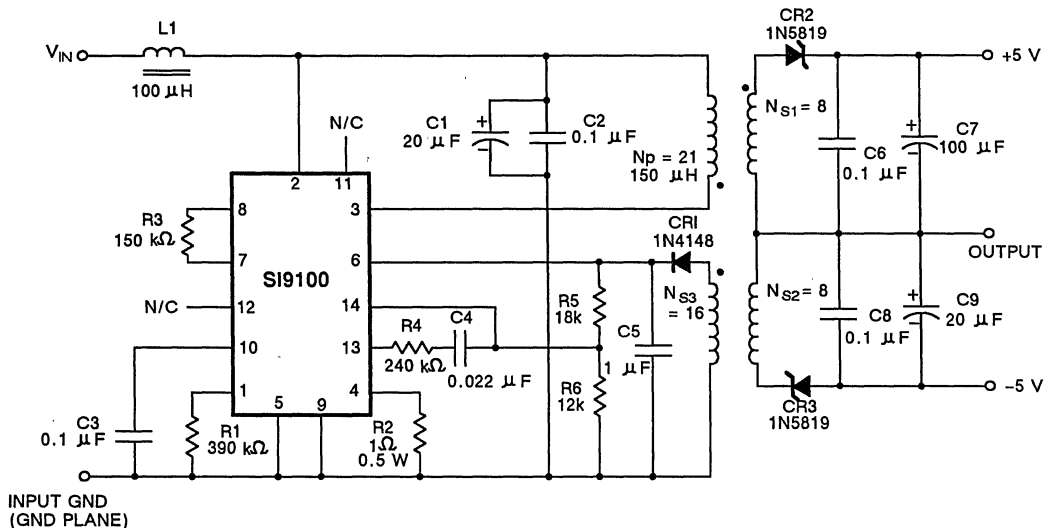


Figure 1. Schematic Diagram of the Si9100 Discontinuous Flyback Converter Circuit

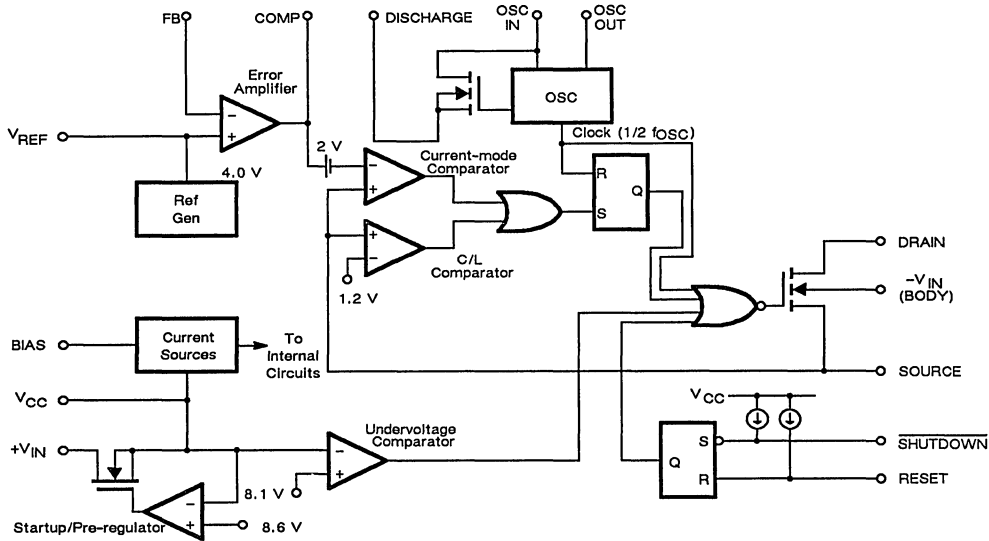


Figure 2. Si9100 Simplified Block Diagram

### Si9100 DESCRIPTION

As shown in the block diagram of Figure 2, the Si9100 combines an oscillator, pre-regulator/start-up circuit, precision voltage reference, error amplifier, current-mode controller, and a MOSFET switching transistor into one 14-pin dual-in-line package. Over-current protection, undervoltage lockout, and logic inputs for both latched and unlatched shutdown modes are also included.

### Start-up/Preregulator Circuit

A unique start-up/preregulator circuit, which is shown in Figure 3, permits the Si9100 to operate over a wide input voltage range (10 to 70 V). The input voltage for the device is connected between the +VIN (pin 2) and -VIN (pin 5) terminals. The high-voltage depletion-mode (normally ON) MOSFET acts as a current source during start-up, charging the capacitance at the VCC terminal (pin 6) directly from the input source. When VCC exceeds the 8.1 V undervoltage threshold, the output switch is enabled to provide well-defined start-up characteristics. VCC is then regulated to 8.6 V by the pre-regulator circuit. If an external voltage source greater than 8.6 V is fed to the VCC terminal, the depletion-mode MOSFET is shut off to reduce power drain from the input power source.

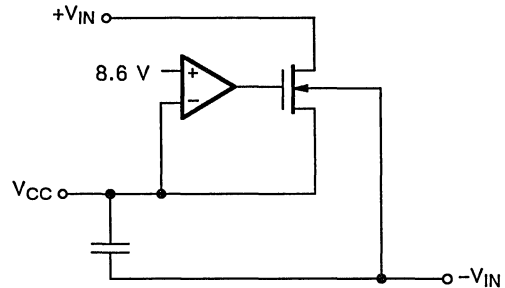


Figure 3. Schematic Diagram of the start-up section of the Si9100

### Oscillator

The oscillator requires a single resistor to set its frequency. The requirements of flux reset in single-ended converters generally dictates a maximum duty cycle of 50%. With the oscillator frequency set at two times the desired switching frequency, a flip-flop divides the clock signal by two, and the logic disables the output during every other clock cycle.

## MOSFET Switch

The MOSFET switching transistor has typical  $r_{DS(ON)}$  and  $V_{(BR)DSS}$  characteristics of  $4\ \Omega$  and  $180\ V$ , respectively. Worst case specifications are  $5\ \Omega$  and  $150\ V$ . The device is a lateral DMOS structure which has external connections for the DRAIN (pin 3) and SOURCE (pin 4). The body of the MOSFET is internally tied to the  $-V_{IN}$  terminal, which must be connected to the most negative input potential in the circuit.

## Error Amplifier

The error amplifier permits compensation of control loops for stable regulator operation. The amplifier uses PMOS input transistors to provide high input impedance ( $2\ M\Omega$  minimum), and is internally compensated for unity gain stability, with  $1\ MHz$  (typical) bandwidth and  $60^\circ$  phase margin.

## Protection

In addition to the undervoltage lockout function already described, the Si9100 provides overcurrent protection and inputs for external logic control. With a sense resistor (typically  $1\ \Omega$ ) connected from the MOSFET source to the  $-V_{IN}$  terminal, the voltage at pin 4 is proportional to the output current. When this voltage exceeds a  $1.2\ V$  reference the overcurrent comparator disables the output MOSFET. The shutdown delay is typically  $100\ ns$  ( $200\ ns$  maximum).

Logic inputs  $\overline{SHUTDOWN}$  (pin 11) and RESET (pin 12) permit the use of latched or unlatched shutdown modes. Internal current source pull-ups normally hold both logic pins high. If the  $\overline{SHUTDOWN}$  pin is pulled low while the RESET is high, then the output switch will be disabled until the  $\overline{SHUTDOWN}$  pin is again allowed to go high. This is the unlatched shutdown mode. If, however, the RESET pin is pulled low while the  $\overline{SHUTDOWN}$  pin is also pulled low, then the converter will be latched off until RESET goes high again.

## FLYBACK CONVERTER OPERATION

### Start-up

Applying input voltage to the circuit initiates charging of capacitor,  $C_1$ , through the filter inductor,  $L_1$ . The depletion-mode MOSFET, as described above, supplies current to capacitor  $C_5$  through the  $V_{CC}$  terminal of the IC. When  $V_{CC}$  reaches the undervoltage

threshold ( $8.1\ V$ ), then transistor switching begins. The  $4.0\ V$  reference and the voltage divider ratio formed by  $R_5$  and  $R_6$  cause the feedback winding,  $N_{S3}$ , to be regulated to  $+10\ V$ . After start-up is complete the feedback voltage trips the comparator to turn off the pre-regulator circuit, and the Si9100 derives its bias power from the feedback winding. The power saved by this bootstrap technique is equal to the product of the IC bias current times the difference between  $V_{IN}$  and  $V_{FB}$ :

$$\text{Power Saved} = (600\ \mu A)(48\ V - 10\ V) = 23\ mW$$

While this is not a great deal of power, it does represent 2.3% of the output for a  $1\ W$  supply. Integrated Services Digital Network (ISDN) applications require such techniques for bias power minimization in order to meet emergency-mode limits for the power-down state.

## Flyback Operation

Flyback converter operation is illustrated by the basic waveforms shown in Figure 4. When the MOSFET switch is turned on, current will ramp up in the primary at a rate given by:

$$\frac{di}{dt} = \frac{V}{L} = \frac{I_{pk}}{t_{ON}}$$

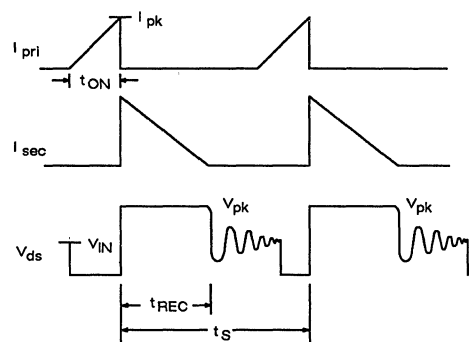


Figure 4. Flyback converter waveforms

Stored energy, given by  $1/2L_P I_{pk}^2$ , is present in  $L_2$  at the time the MOSFET is switched off. This energy is released to the secondary windings,  $N_{S1}$  through  $N_{S3}$ , during the off time, as shown by the total secondary current,  $I_{sec}$ , in Figure 4. This is the flyback principle in its simplest terms. A transformer is designed to transfer energy directly from the primary to the secondary, with as little stored energy as possible. A flyback inductor receives energy during one interval of the switching cycle, then releases this stored energy at a later interval of the switching cycle.

During the time that the secondaries are conducting, shown as  $t_{rec}$ , the magnetic flux recovers, or "resets" to zero, and the MOSFET must block the sum of the reflected voltage from the secondary and the input voltage. This requires a worst case blocking voltage of:

$$\begin{aligned} V_{pk} &= V_{IN} + \frac{N_P}{N_{S1}} (V_O + V_D) \\ &= 70 + \frac{21}{8} (5.0 + 0.5) = 85 \text{ V} \end{aligned}$$

A leakage inductance spike appears at the leading edge of the  $V_{DS}$  waveform. The spike is less than the 150 V minimum  $V_{(BR)DSS}$ , and no snubber network is required. Since the flux is reset to zero before the end of each switching cycle, current flow through the secondary is discontinuous. Consequently, this circuit is called a discontinuous-conduction-mode (DCM) flyback converter.

## Regulator Control Loop

The function of the regulator control loop is to maintain the output voltages constant as either the input line voltage or load current vary. These are termed "line regulation" and "load regulation", respectively.

A sense winding has been chosen to close the regulator loop and provide output isolation. Since the secondary windings are coupled on a common core, the volts/turn ratio is the same for  $N_{S1}$ ,  $N_{S2}$  and  $N_{S3}$ . The resulting secondary voltages will track each other quite closely. There is, however, some degradation in load regulation due to leakage (uncoupled) inductance between the  $\pm 5$  V output windings and the sense winding. This effect becomes progressively worse as the switching frequency is increased. The coupled inductor used here has been designed for

good coupling between output and sense windings in order to maintain better than 5% regulation over the 0.2 W to 1 W load range. Design details for the coupled inductor are included in Appendix A.

To analyze the system closed loop response, begin by reflecting the filter capacitance and load resistance from each output winding to the feedback winding.

$$\begin{aligned} C_{eff} &= C_5 + \left( \frac{N_{S1}}{N_{S3}} \right)^2 \cdot C_7 + C_9 \\ &= 1 \mu\text{F} + \left( \frac{8}{16} \right)^2 (100 \mu\text{F} + 20 \mu\text{F}) = 31 \mu\text{F} \end{aligned}$$

The effective load resistance,  $R_{eff}$ , can be found by assuming that the entire 1 W load is connected across the sense winding output:

$$R_{eff} = \frac{V_S^2}{P_O} = \frac{(10 \text{ V})^2}{1 \text{ W}} = 100 \Omega$$

The effective load impedance is determined at low frequency by the 100 ohm resistance and at high frequency by the capacitive reactance given by  $X_C = 1/\omega C_{eff}$ . The control-to-output transfer function thus has a pole at:

$$\begin{aligned} f_p &= \frac{1}{2\pi R_{eff} C_{eff}} \\ &= \frac{1}{2\pi (100) (31 \cdot 10^{-6})} = 51 \text{ Hz} \end{aligned}$$

To calculate the low frequency gain of the power stage, assume a 1 mV change in the error voltage,  $V_e$ , at the output of the error amplifier, and calculate the voltage change,  $\Delta V_S$ , which results at the feedback winding. Then combine the power stage gain with the error amplifier gain (including the voltage divider) to yield the total loop response. Assume for these calculations that the converter efficiency remains constant at 83.33%.

$$P_{IN} = \frac{P_O}{\eta} = \frac{1 \text{ W}}{0.8333} = 1.2 \text{ W}$$

The power input to the converter is the product of the stored inductive energy times the switching frequency.

$$P_{IN} = \frac{1}{2} L_P (I_{pk})^2 \cdot f_s$$

Rearranging to solve for  $I_{pk}$  gives:

$$I_{pk} = \sqrt{\frac{2P_{IN}}{L_P \cdot f_s}} = \sqrt{\frac{2 (1.2)}{(150 \mu H) 10^5}} = 0.4 \text{ A}$$

Since the current sense resistor,  $R_2$ , equals  $1 \Omega$ , a  $1 \text{ mV}$  change in the error voltage (at pin 13) will result in a  $1 \text{ mA}$  change in the peak inductor current, i.e.,  $\Delta I_{pk} = \Delta V_e$ . A  $1 \text{ mA}$  increase in  $I_{pk}$  causes  $P_{IN}$  to increase to:

$$P_{IN} = \frac{1}{2} L_P (I_{pk} + \Delta I_{pk})^2 \cdot f_s = \frac{1}{2} \cdot 150 \cdot 10^{-6} (0.400 + 0.001)^2 \cdot 10^5 = 1.206 \text{ W}$$

Assuming efficiency remains constant,

$$P_O = (.833) \cdot P_{IN} = 1.005 \text{ W}$$

This translates to an increase in the sense voltage to:

$$V_S = \sqrt{P_O \cdot R_{eff}} = \sqrt{(100 \cdot 1.005)} = 10.025 \text{ V}$$

The gain is given by:

$$\frac{\Delta V_S}{\Delta V_e} = \frac{10.025 \text{ V} - 10 \text{ V}}{1 \text{ mV}} = 25$$

At full load the low frequency gain of the power stage is 25 (28 dB), with a single pole in the transfer function at 51 Hz. Performing a similar calculation at the 20% load condition yields a gain of 56 (35 dB) with a pole at 10 Hz. There will also be a zero in the transfer function at approximately 30 kHz due to capacitor ESR.

The solid line in Figure 5 represents the transfer function of the converter power stage at full load. The corresponding curve at a 20% load is shown in figure 6. To complete the analysis of the control loop requires accounting for the resistive voltage divider and the error amplifier. The resistor  $R_6$  sets the DC bias condition, but does not enter into the small signal analysis.

At high frequencies the gain is  $R_4/R_5$ , with a zero occurring in the transfer function at

$$f_z = \frac{1}{2\pi (240 \text{ k}\Omega) (.022 \mu\text{F})} = 30 \text{ Hz}$$

The error amplifier response is shown in Figures 5 and 6 as dashed lines. The error amplifier response times the power stage gain gives the total loop gain, which is shown as the gray line for full load in Figure 5 and light load in Figure 6. Actual measurements of loop gain and phase yielded a loop bandwidth of 14 kHz with 68 degrees phase margin. Figure 7 is an oscilloscope photograph of the +5 V output as the load is stepped between 20% and 100% of full load. Response time is under  $200 \mu\text{s}$  with no overshoot.

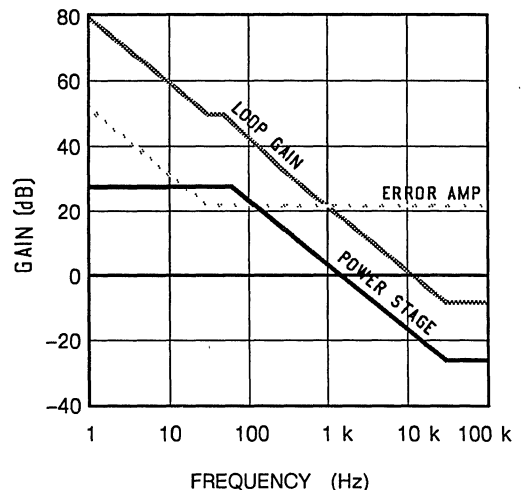


Figure 5. Loop gain at 100% load

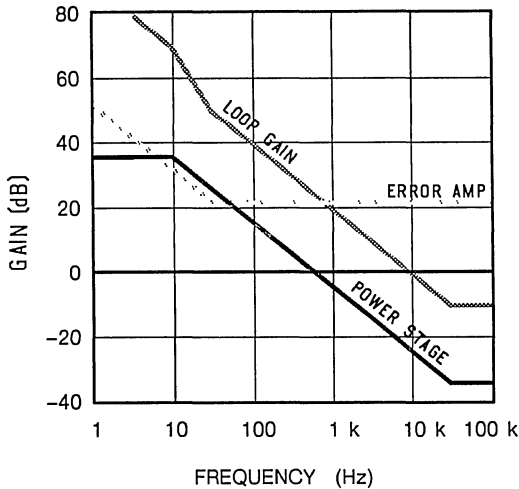


Figure 6. Loop gain at 20% load

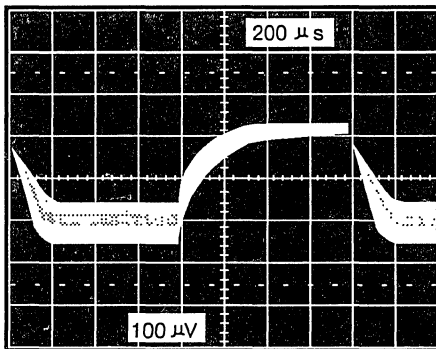


Figure 7. Step load response

**ISDN APPLICATIONS**

Integrated Services Digital Networks (ISDNs) pose some unique problems to telecom systems design engineers. Standards proposed by the International Telephone and Telegraph Consultative Committee (CCITT) recommend that input power to ISDN termi-

nal equipment (TE) meet the limits outlined in Table I<sup>1</sup>.

**Table I. ISDN power requirements**

Operating mode	Maximum input power to TE	efficiency target
Normal-active	900 mW	70 %
Normal-power down	100 mW	60 %
Emergency-active	400 mW	70 %
Emergency-power down	25 mW	40 %

The 25 mW limit during emergency power-down mode operation may be especially troublesome<sup>2</sup>. In order to supply 10 mW to the TE for such functions as memory back-up, total converter losses must be less than 15 mW. Under such light load conditions the major power loss is in the PWM controller. Only controllers implemented in CMOS can presently be expected to meet this requirement.

Although the converter circuit of Figure 1 was not designed specifically for use in ISDN terminals, with some modifications it can be used in these applications. Since CMOS logic circuits consume power only during switching transitions, the first modification which is recommended is to decrease the switching frequency. The coupled inductor, L<sub>2</sub>, can be operated at 40 to 50 kHz (change R<sub>3</sub> from 150 kΩ to 390 kΩ) without a redesign. Decreasing the frequency further requires a larger core size.

A second circuit modification which is recommended is to increase the resistances used in the voltage divider network (R<sub>5</sub> and R<sub>6</sub>). The values used in the 1 W converter will dissipate  $(10)^2 / (18\text{ k}\Omega + 12\text{ k}\Omega) = 3.33\text{ mW}$ . This loss is negligible for the 1 W converter, but it is nearly one fourth of the budgeted power loss for the ISDN supply during the emergency power-down state. Setting R<sub>5</sub> = 51.1 kΩ and R<sub>6</sub> = 34.0 kΩ reduces the voltage divider dissipation to 1.2 mW. With these two minor changes the flyback converter meets the efficiency specifications of Table I. Figure 8 illustrates the efficiency improvement at light load levels which results from the circuit changes outlined above.

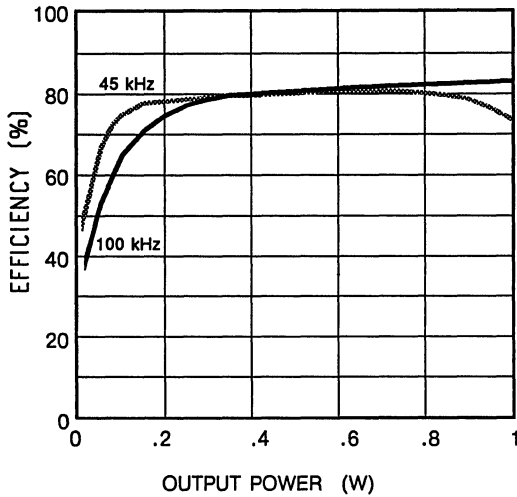


Figure 8. Efficiency vs. load curves for the flyback converter

## Other Si9100 Applications Circuits

The Si9100 has been called a "One Watt High-Voltage Switchmode Regulator" in order to describe its

most appropriate type of application--low power converters. The device is not, however, limited to 1 W designs. Figure 9 shows the maximum achievable output power as a function of minimum input voltage for several types of converters, two of which are discussed below.

## CCM Flyback Converter

By redesigning the magnetics for continuous conduction, the flyback circuit of Figure 1 can be made to provide 3 W of output power. Operation in the continuous conduction mode (CCM) introduces a right-half-plane (RHP) zero into the control-to-output transfer function of the power stage. The RHP zero incurs a phase lag without the corresponding gain rolloff caused by left-half-plane poles, and lead compensation cannot be used. Instead, the gain must be rolled off to unity (0 dB) below the RHP zero frequency. The continuous-mode flyback will, therefore, have a slower dynamic response than the DCM flyback. Also, to maintain the same output ripple for the 3 W converter, it is necessary to increase the size of the output filter capacitors.

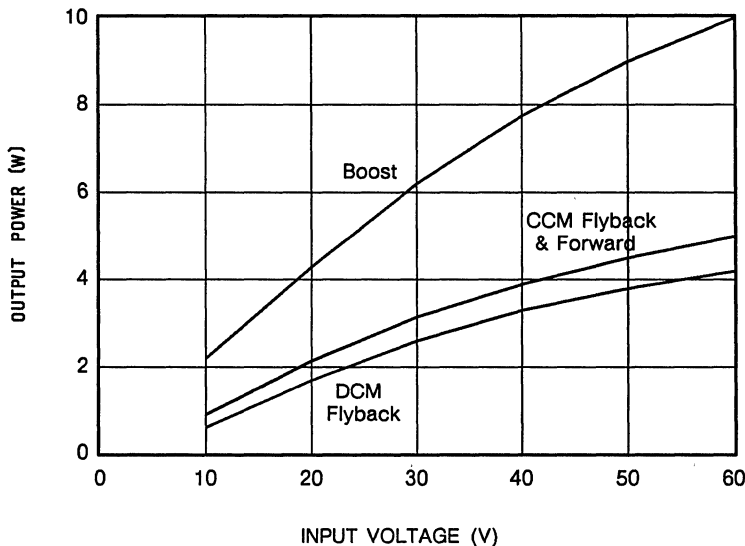


Figure 9. Maximum output power vs. minimum input voltage



## Forward Converter

Forward converters are not normally used for power supplies rated under 100 W, due to the additional cost of the output filter chokes. However, for 2 to 4 W converter applications requiring ultra-low ripple, the cost of the additional inductor may be warranted. One such application is low power instrumentation for avionics.

The forward converter of Figure 10 was designed to operate from 28 V aircraft power (MIL-STD-704D) to provide 2.5 W at 80% efficiency. A single core with multiple windings has been used to decrease cost and board space required for the output filter inductors. The input voltage range is 18 to 32 VDC; regulation is 5%; and the switching frequency is 100 kHz. Measured peak-to-peak voltage ripple was 8 mV for the +15 V output, 4 mV for the -15 V output, and 13 mV for the +5 V output, at maximum load.

Toroidal cores were used for both the transformer and the coupled output inductor to achieve very low leakage inductance. The transformer winding data is as follows:

Core - Ferroxcube #768T188-3C8

Windings - N1 = 31 turns (AWG26)

N2 = 31 turns (AWG34)

N3 = 22 turns (AWG32)

N4 = 64 turns (AWG32)

N5 = 43 turns (AWG34)

The primary and clamp windings are placed on the core first, wound bifilar to minimize leakage inductance. The +5 V output is wound next, followed by the  $\pm 15$  V outputs wound bifilar. The 10 V winding was placed on the outside. Each winding is spread over the entire circumference of the toroidal core for optimum magnetic coupling.

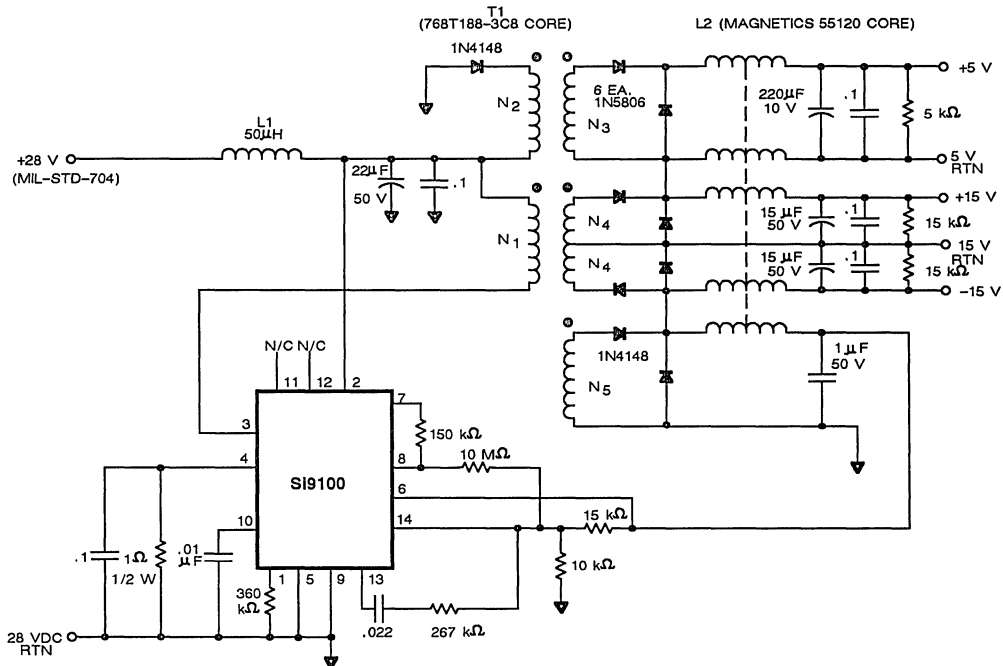


Figure 10. 2.5 W forward converter using the SI9100

Coupled inductors must have the same turns ratios as the transformer secondaries or high circulating currents result in very high output ripple. The coupled inductor,  $L_2$ , is a molypermalloy powder (MPP) toroid (Magnetics #55120) with three times the number of turns as each of the T1 secondaries. The inductor winding data is as follows:

- +5 V -- 66 turns (AWG30)
- +15 V -- 192 turns (AWG30)
- 15 V -- 192 turns (AWG34)
- +10 V -- 129 turns (AWG34)

It should be mentioned here that MIL-STD-461 EMI testing was not performed for this supply. To meet CE03 and CS01 limits, some input filter redesign is required. Although current-mode control exhibits excellent audio-susceptibility performance, it is still necessary to damp the input filter to reduce peaking

of its output impedance at the resonant frequency (Reference 3 provides useful design information regarding these requirements).

## References

- 1) Rosenbaum, D. and Stolp, K. H., "The Feeding Conception of the ISDN Basic Access," IEEE Intelec Conference, Munich, FRG, Oct 14-17, 1985, pp. 505-512.
- 2) Krautkramer, W. and Schickling, B., "Remote Power Feeding of ISDN Terminals at the Basic Access," IEEE Intelec Conference, Munich, FRG, Oct 14-17, 1985, pp. 513-519.
- 3) Middlebrook, R. D., "Input Filter Considerations in Design and Application of Switching Regulators," IEEE Industry Applications Society Annual Meeting, Oct. 11-14, 1976.

## APPENDIX A FLYBACK INDUCTOR DESIGN

### Inductance Calculation

The first step is to calculate the maximum primary inductance for discontinuous conduction at maximum load. Input power to the coupled inductor is approximately:

$$1) \quad P_{IN} = \frac{1 \text{ W}}{0.8} = 1.25 \text{ W}$$

Input power is also equal to the product of the stored energy in the magnetic field times the switching frequency:

$$2) \quad P_{IN} = \frac{1}{2} L_P (I_{pk})^2 \cdot f_s$$

The minimum primary current slope occurs at the minimum input voltage condition.

$$\left. \frac{di}{dt} \right|_{\min} = \frac{V_{IN(\min)}}{L_{P(\max)}}$$

If a maximum duty ratio of 0.45 is assumed, then the minimum current peak is given by:

$$3) \quad I_{pk} \leq \left. \frac{di}{dt} \right|_{\min} \cdot (0.45 T_S) \quad \text{or}$$

$$I_{pk} \leq \frac{V_{IN(\min)}}{L_{P(\max)}} \cdot (0.45 T_S)$$

Combining equations 2 and 3 gives:

$$\begin{aligned} P_{IN(\max)} &= \frac{1}{2} L_{P(\max)} I_{pk(\min)}^2 \cdot f_s \\ &= \frac{1}{2} L_{P(\max)} \left( \frac{V_{IN(\min)}}{L_{P(\max)}} \right)^2 (0.45 T_S)^2 f_s \\ &= \frac{1}{2} \frac{V_{IN(\min)}^2}{L_{P(\max)}} (0.45 T_S)^2 f_s \\ \therefore L_{P(\max)} &= \frac{1}{2} \frac{V_{IN(\min)}^2}{P_{IN(\max)}} (0.45 T_S)^2 f_s \\ &= \frac{1}{2} \frac{(15)^2}{1.25} (0.45 T_S)^2 10^5 = 182 \mu\text{H} \end{aligned}$$

To allow for component tolerances choose a nominal primary inductance of 150  $\mu\text{H}$ . Equation 2 then gives  $I_{pk} \approx 0.4 \text{ A}$ .

## APPENDIX A (Cont'd)

### Core Selection

The area product method was used to determine the inductor core size. Refer to "Magnetic Core Selection for Transformers and Inductors" by McLyman, for more information on magnetics design methods (Marcel Dekker, Inc., 1982).

$$A_P = \left( \frac{2 \left( E \right) \cdot 10^4}{B_m \cdot K_u \cdot K_j} \right)^{1.14}$$

where:

$E$  = Core energy storage requirement

$B_m$  = Maximum flux density

$K_u$  = Window utilization factor

$K_j$  = Current density coefficient

$$E = \frac{1}{2} L_P I_{pk}^2$$

Let  $B_m = 1500$ , gauss = .15 tesla, and  $K_u = 0.10$

$$A_P = \left( \frac{2 \left( \frac{1}{2} \cdot 150 \cdot 10^{-6} (.4)^2 \right) \cdot 10^4}{0.15(0.10) (433)} \right)^{1.14}$$

$$= 0.0233 \text{ cm}^4$$

Since the empirical equation given above applies for the area product of simple one-winding inductors, multiply by 2 for a coupled inductor. All of the secondaries combined will handle the same energy as the primary, and can therefore be allotted equal portions of the window area. The area product requirement is thus:

$$A_P = 2 \cdot 0.0233 \text{ cm}^4 = 0.0466 \text{ cm}^4$$

The EP-13 core has an area product of  $0.049 \text{ cm}^4$ , which meets this requirement. Also, this EP core can be tube-loaded for automatic insertion in high volume manufacturing applications, and is available from multiple sources (Siemens, TDK, and Amperex Ferrocube).

### Core $A_L$ Value Determination

The number of primary turns is found from:

$$L = \frac{N_P \Phi}{I_{pk}} = \frac{N_P B_m A_C}{I_{pk}}$$

Limiting the peak flux density to 0.15 Tesla gives:

$$N_P = \frac{L_P I_{pk}}{B_m A_C} = \frac{(150 \cdot 10^{-6})(.4) \cdot 10^4}{(0.15)(0.195 \text{ cm}^2)}$$

$$= 20.5 \text{ turns} \approx 21 \text{ turns}$$

This gives the following value for  $A_L$ :

$$A_L = \left( \frac{1000}{21} \right)^2 (150 \cdot 10^{-6}) = 340 \text{ mH per 1000 turns}$$

### Secondary Turns Calculation

The core flux is reset to zero during the off time for each switching cycle. To guarantee discontinuous conduction mode at the maximum load condition, it is necessary to limit the inductance of the secondary windings to some maximum value. Worst case conditions occur at the maximum switching frequency (110 kHz) and maximum  $A_L$  value (374 mH/1000 turns for 10 % tolerance). The voltage across  $N_{S1}$  during the diode conduction interval is  $V_O + V_D = 5.0 + 0.5 = 5.5 \text{ V}$ , and the negative current slope is

$$\frac{di}{dt} = \frac{I_{S1}}{t_{rec}} = \frac{V_O + V_D}{L_{S1}}$$

where  $I_{S1}$  is the peak current in the  $N_{S1}$  winding,  $t_{rec}$  is the conduction time of CR2, and  $L_{S1}$  is the inductance of  $N_{S1}$ . The rectifier conduction duty ratio is defined as:

$$d_r = \frac{t_{rec}}{T_S}$$

The load current is related to the peak secondary current and duty ratio by the equation:

$$I_{S1} = \frac{2 \cdot I_O}{d_r}$$

Combining these equations solves for the rectifier conduction duty ratio in terms of load current, inductance, and output voltage.

$$d_r = \sqrt{\left( \frac{2 \cdot I_O \cdot L_{S1}}{(V_O + V_D) \cdot T_S} \right)}$$

Setting the duty ratio < 0.45 gives:

$$d_r = \sqrt{\frac{2(.167) \cdot L_{S1}}{5.5(9.09)}} \leq .45$$

Therefore,  $L_{S1} < 30.3 \mu\text{H}$ . Since  $A_{LMAX} = 374 \text{ mH}/1000 \text{ turns}$ ,

$$L_{S1} = \left( \frac{N_{S1}}{1000} \right)^2 \cdot (0.374) \leq 30.3 \mu\text{H}$$

$$\therefore N_{S1} \leq 9 \text{ turns}$$

Use  $N_{S1} = N_{S2} = 8 \text{ turns}$ :

$$N_{S3} = (10 \text{ V} + 0.7 \text{ V}) \frac{N_{S1}}{5.5 \text{ V}}$$

$$= 15.6 \text{ turns} \approx 16 \text{ turns}$$

### Winding Order

The primary winding (1-2) is placed first over the bobbin using one strand of AWG31 magnet wire (21 turns). The highest current secondary (3-4) is wound over the primary using two strands of AWG31 (8 turns). The 10 V sense winding (7-8) is put down next, using one strand of AWG36 (16 turns). The -5 V output (5-6) is wound last using one strand of AWG31 wire (8 turns).

## APPENDIX B SI9100 FLYBACK CONVERTER PARTS LIST

U <sub>1</sub>	SI9100
L <sub>1</sub>	Inductor, 100 $\mu\text{H}$ @ 75 mA DC
L <sub>2</sub>	Coupled Inductor, GFS Mfg. # 85-787-4*
C <sub>1</sub>	20 $\mu\text{F}$ , 100 V, Aluminum Electrolytic, Sprague # 30D+TE1409
C <sub>2</sub> , C <sub>3</sub> , C <sub>6</sub> , C <sub>8</sub>	0.1 $\mu\text{F}$ ceramic
C <sub>4</sub>	.022 $\mu\text{F}$ ceramic
C <sub>7</sub>	100 $\mu\text{F}$ , 10 V, tantalum, Sprague # 196D107X9010P
C <sub>9</sub>	20 $\mu\text{F}$ , 10 V, tantalum, Sprague # 196D226X9010J
C <sub>5</sub>	1 $\mu\text{F}$ , 50 V, WIMA MKS2
CR1	1N4148
CR2, CR3	1N5819, Schottky rectifier
R <sub>1</sub>	390 k $\Omega$ , 1/4 W Carbon
R <sub>2</sub>	1 $\Omega$ , 1/2 W Carbon
R <sub>3</sub>	150 k $\Omega$ , 1/4 W Carbon
R <sub>4</sub>	240 k $\Omega$ , 1/4 W Carbon
R <sub>5</sub>	18 k $\Omega$ , 1/4 W Carbon
R <sub>6</sub>	12 k $\Omega$ , 1/4 W Carbon

\* GFS Manufacturing Company, 21 Crosby Road,  
Dover, NH, USA 03820-1409

## THE DG535/536 WIDEBAND MULTIPLEXER SUITS A WIDE VARIETY OF APPLICATIONS

Gareth Powell  
Revised February 1988

### INTRODUCTION

Analog switch IC's traditionally have found limited use in applications involving high-frequency analog or digital signals. Degradation of switch performance and intolerable signal cross-talk between channels has undoubtedly forced many designers to use bulky electromechanical switches or costly discrete designs.

At best, analog switch ICs configured in L or T arrangements (see Siliconix Application Note AN83-15) could be adopted. However, increased board space and layout complexity became major problems in configuring systems with high channel density.

The DG535/536 are compact 16-channel, single-ended multiplexer ICs, primarily designed as a cost-effective solution to video and wideband switching problems. Other applications that benefit from the devices' superior performance characteristics are:

- Digital switching
- Audio Switching
- PCM routing networks
- ATE systems
- High-channel-density multiplexing or demultiplexing systems
- High-speed multiplexing systems
- Low-level signal multiplexing

### PRODUCT DESCRIPTION

A functional block diagram of the DG535/536 is shown in Figure 1 and the switch configuration is shown in Figure 2. The device is fabricated using self-isolated, silicon-gate D/CMOS technology. This process enables the logic interface and driver circuitry, the gating and latching stages, and the switching elements to be combined in a monolithic structure.

Ease of design for large switching matrices and interface with microprocessors is accomplished with comprehensive logic gating and latching functions

available on the chip. The DG536 is housed in a small, 44-pin J-lead package, thus minimizing board size requirements. The DG535 is packaged in a 28-pin DIP. Chip select pins (CS and  $\overline{CS}$ ) permit easy stacking of devices for multichannel multiplexing systems (see Applications Section, Figure 19).

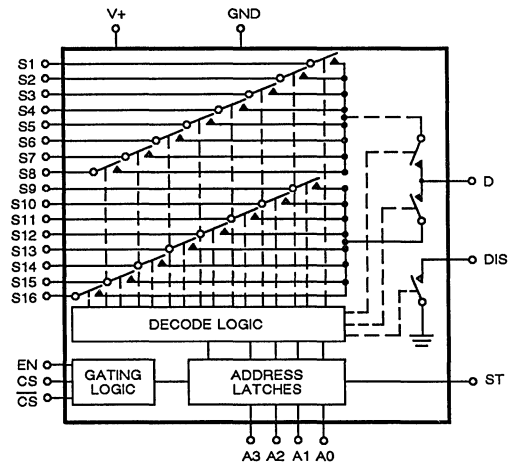


Figure 1. DG535/536 Functional Block Diagram

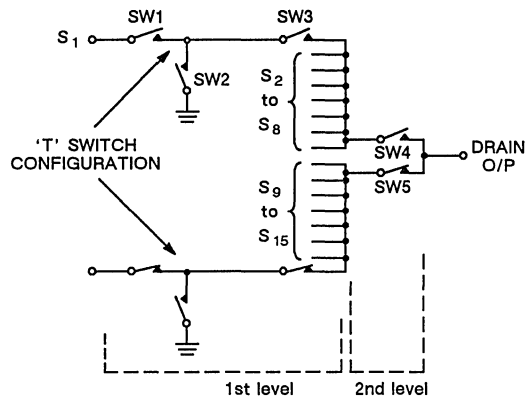


Figure 2. DG535/536 Switch Configuration

An additional feature, a DIS pin, is an open drain terminal with the source tied to the device substrate. The DIS terminal represents a high impedance to the substrate (normally ground) when the DG535/536 is disabled and a low impedance to ground when the DG535/536 is enabled. This output can be used to indicate which device in a large matrix has been enabled (see Figure 18), or it can be used to switch off circuitry following the multiplexer stages.

## MINIMIZING PARASITIC EFFECTS

The insertion loss and bandwidth of the switch are improved with DMOS transistors that offer a low on-resistance and low intrinsic capacitance (see Siliconix SD5000 data sheets). On the DG536 channel-to-channel crosstalk is minimized by physically separating each input channel with a GND pin which extends to the device substrate. This, in conjunction with careful PC board layout (see Figure 11), can yield channel-to-channel crosstalk figures better than -92 dB at 5 MHz.

Further ac performance benefits are obtained through the n-channel DMOS transistor T configurations (Figure 2). This maximizes the off-isolation, since SW2 provides a shunt path to ground for any signals fed through the parasitic capacitance associated with SW1. SW3 (working in phase with SW1) provides an extra stage of off-isolation and prevents the shunt switch (SW2) from affecting consecutive channels.

## TWO-LEVEL SWITCHING

The two-level switching system of the DG535/536 (SW4 and SW5) works in antiphase, effectively isolating half of the switch outputs from the drain (output)

of the multiplexer. These series switches serve several functions:

- They provide an extra stage of off-isolation.
- They reduce the drain output capacitance significantly and increase the multiplexing transition speed.
- They reduce the off-leakage current, which reduces the offset voltage that develops from the total off-leakage current flowing through the load resistance and/or switch ON-resistance. This enables lower analog signal levels to be handled accurately.

## SILICON GATE

Polysilicon is used as the transistor gate material for the DG535/536, as opposed to more conventional metal-gate designs. This technology minimizes the charge coupling of the control-logic signals to the switch output due to the self-aligning properties of the process. Metal-gate technology relies on photolithographically aligning the gate metal with the channel diffusions, resulting in greater overlap tolerances.

As shown in Figure 3, a PN junction exists between the p-type substrate and then n-type channel diffusions. This junction should not become forward biased by the analog signal going more negative than the substrate potential (normally ground).

Device damage could result from the current flow through the forward biased substrate-channel junction, exceeding the aluminum current handling capacity (i.e. 20 mA). Analog signal DC biasing or offsetting the device power supplies can prevent this problem. These methods are discussed in the applications section of this paper (Figure 12 and Figure 13).

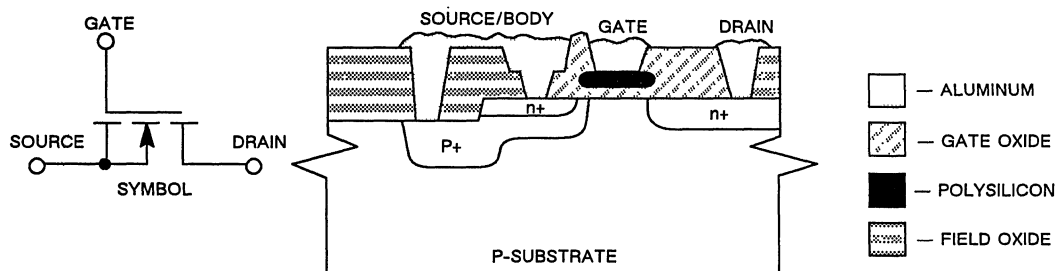
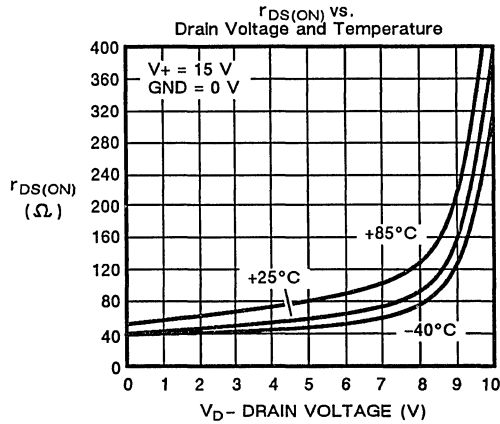


Figure 3. Cross-section of an N-channel, Silicon-gate DMOS Transistor

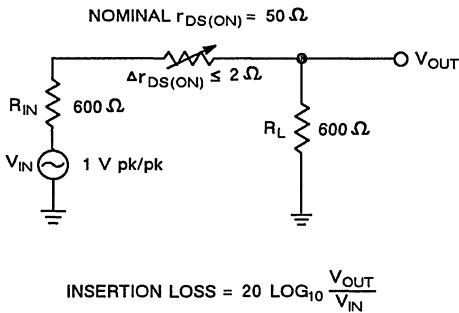
## DG535/536 DC CHARACTERISTICS

### ON-resistance

ON-resistance must be low to ensure low insertion loss, especially when the switch drives low load resistances. As shown in Figure 3, the ON-resistance remains low and fairly constant over the usable analog signal range. This makes the DG535/536 useful for audio applications that require low harmonic distortion.



**Figure 4.** ON-resistance vs. Analog Signal Characteristics of the DG535/536



**Figure 5.** 600  $\Omega$  Audio System

In a 600-ohm audio system, such as the one represented in Figure 5, the percentage of ON-resistance change relative to the load resistance is only 0.33%. The insertion loss due to the switch ON-resistance is 0.7dB.

### Leakage Current

The DG535/536 features low OFF and ON leakage currents, reducing low switching errors.

### Power Supply Current Consumption

Until now, most available video multiplexers or digital crosspoint switches relied on high-level supply currents for operation. The DG535/536 requires a total supply current of only 5  $\mu\text{A}$ , typical. This feature makes the DG535/536 ideal for systems with high channel density, such as 32-channel crosspoint matrices used in video mixing consoles or as ECL digital crosspoint replacements in large data transmission systems.

The total supply current for a 32-channel crosspoint system using the DG535/536 is approximately 320  $\mu\text{A}$ , much lower than other video multiplexers.

## DG536 AC CHARACTERISTICS

(Refer to the DG535 data sheet for the 28-pin DIP performance.)

### Bandwidth

This "ON" frequency response, as shown in Figure 6, is expressed as the frequency at which the insertion loss (at dc) increases by 3-dB. The measured bandwidth of the DG536 is greater than 300 MHz.

### Crosstalk

Crosstalk is the amount of unwanted signal apparent at a particular node due to the parasitic capacitance of the device. As the most important parameter for many applications, crosstalk is specified in a number of ways.

1. **Single-channel crosstalk** (Figure 7) is the ratio of the signal seen at the drain (output) to the signal applied to a single OFF-channel input. This is expressed by

$$\text{XTALK}_{(SC)}\ (\text{dB}) = 20\ \text{LOG}_{10} \frac{V_{OUT}}{V_{IN}}$$

Most conventional multiplexers specify this parameter on the data sheet as off-isolation. This value for the DG536 is more than twice as good as other 16-channel analog multiplexer ICs, proving the effectiveness of the T switch.

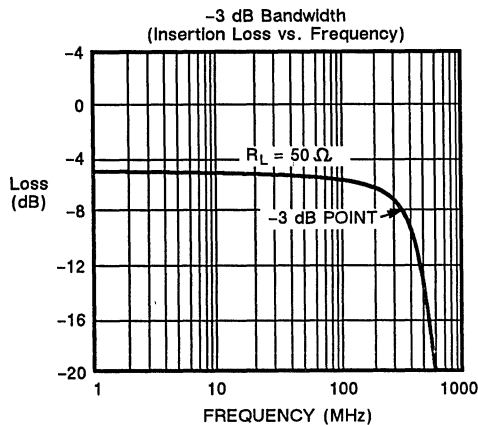
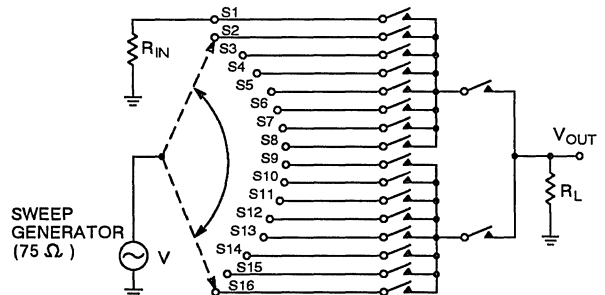
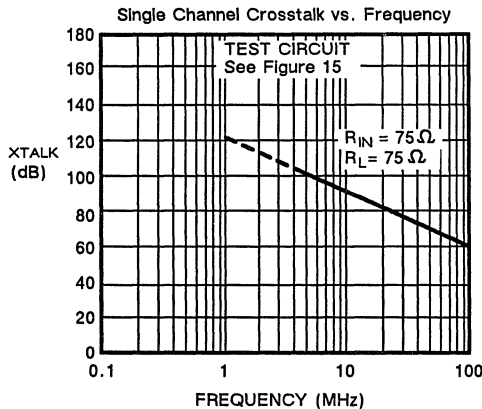
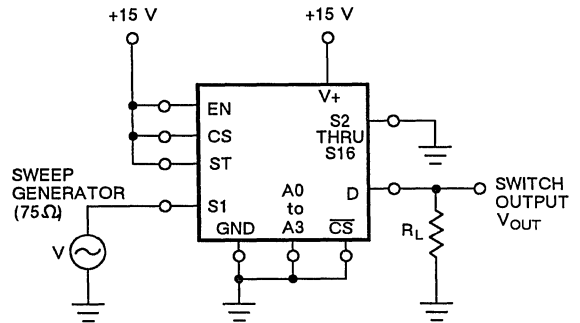


Figure 6. Bandwidth of the DG536. Please refer to the DG535 Data Sheet for 28-pin DIP performance



- NOTES:
1. Channel S1 on.
  2. Any individual channel between S2 and S16 can be selected.
  3.  $XTALK_{(SC)} = \text{Average value of } 20 \text{ LOG}_{10} \frac{V_{OUT}}{V}$  is scanned Sequentially from S2 to S16.

Figure 7. Single-channel Crosstalk vs. Frequency Graph and Test Circuit (DG536)

2. **All hostile crosstalk** (Figure 8) is the ratio of the signal measured at the drain to the signal applied simultaneously to all 15 channels (i.e., with one channel ON).
3. **Chip-disabled crosstalk** is the drain output to signal input ratio. The input signal is applied to all 16 off channels simultaneously.
4. **Adjacent input crosstalk** (Figure 10) is the ratio of the signal applied to a source (input) to the signal measured at any adjacent source. A low adjacent input crosstalk is required for video applications to avoid ghosting effects that may appear on video monitors or TV screens.



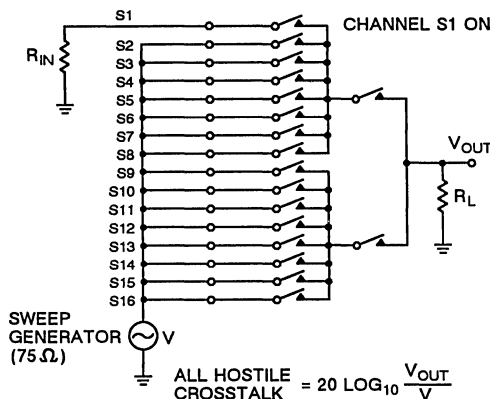
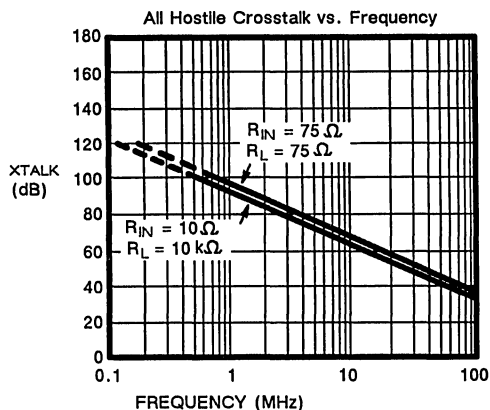


Figure 8. All Hostile Crosstalk vs. Frequency Graph and Test Circuit (DG536)

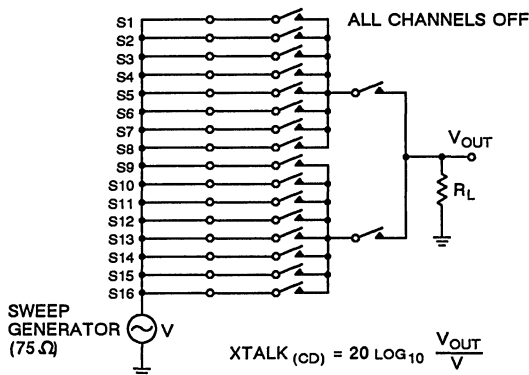
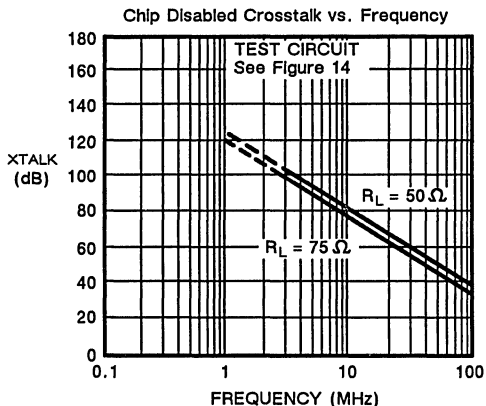


Figure 9. Chip-Disabled Crosstalk vs. Frequency Graph and Test Circuit (DG536)

## Switching Time

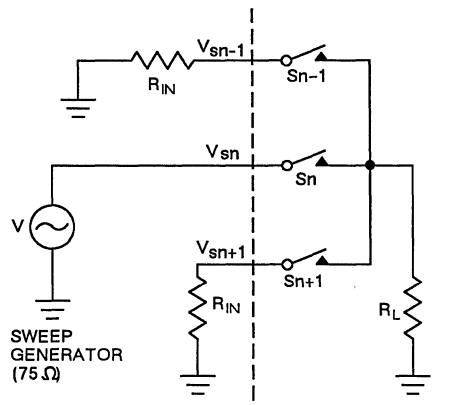
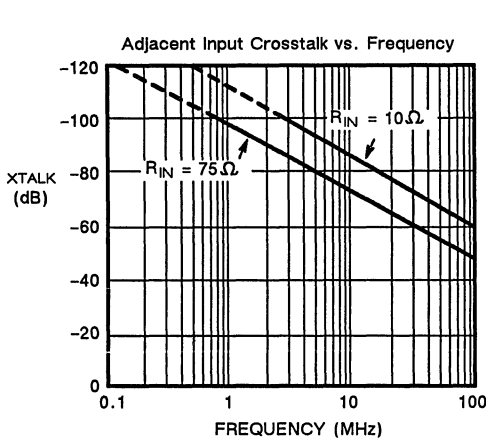
The DG535/536 switching time enables use of the device at high multiplexing rates. The low transition times ( $t_{ON} = 300$  ns maximum and  $t_{OFF} = 150$  ns maximum) make it ideal for fast multi-channel analog or digital multiplexing.

True break-before-make (BBM) switching action is guaranteed by design. This prevents shorting (crosstalk) of time adjacent input channels during transition.

## Capacitance

Capacitance determines the loading effect of the multiplexer on signal sources and affects transition times, as well as system bandwidth.

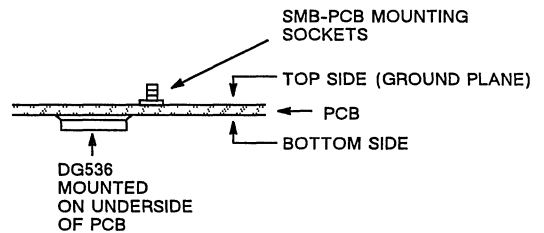
1. **OFF-state input capacitance** gives the loading of the device (in the OFF state) to a signal source. With a typical value of 2 pF, this allows efficient paralleling of many device channels in multichannel crosspoint matrices with negligible loading effects.



$$\text{INPUT CROSSTALK} = 20 \text{ LOG}_{10} \frac{V_{sn-1}}{V_{sn}} \text{ or } 20 \text{ LOG}_{10} \frac{V_{sn+1}}{V_{sn}}$$

Figure 10. Adjacent Input Crosstalk vs. Frequency Graph and Test Circuit (DG536)

2. **ON-state input capacitance** also determines the loading effects of the device ON signal sources and limits the number of parallel on channels allowed in a large matrix. In large matrixes buffering of the input signals is recommended.
3. **OFF-state output capacitance** affects the transition speed of the multiplexer. The output capacitance must be charged and discharged in turning on and off a device; thus, a low value of capacitance enables rapid transition times. Table 1 shows a comparison of DG536 capacitance to comparable 16-channel multiplexers.



## CIRCUIT BOARD LAYOUT

To optimize the high-frequency characteristics of the DG536, care must be taken in circuit board layout and interconnections. Parasitic stray capacitances caused by poor layout could degrade performance significantly. As shown in Figure 11, use of guard planes and traces between signal paths is a good layout practice. Other layout considerations include:

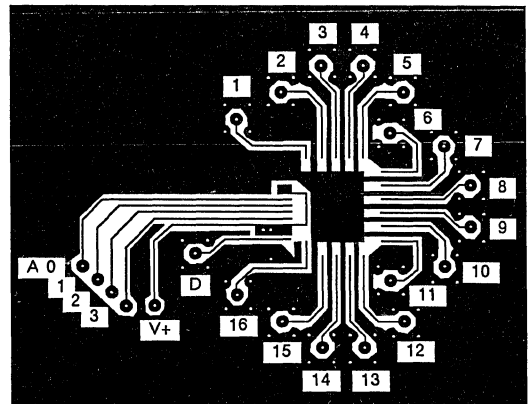


Figure 11. Circuit Board Layout for Optimal Performance (DG536)

- short signal paths
- sufficient power supply decoupling
- coaxial interconnect of leads, plugs, and sockets.
- sockets should be avoided

TABLE 1. Capacitance Value for 16-Channel Multiplexers

Parameter	DG526	DG506A	DG508A	CD4051/2/3	DG536
CS(off) (pF)	10	6	5	10	2
CD(off) (pF)	35	45	50	60	8

NOTE: These are typical values taken from data sheets.

**APPLICATIONS**

Many applications for the DG535/536 will be in video related systems. Some examples of circuit configurations are included in this section.

**VIDEO**

The DG536 was designed primarily for handling broadcast quality video signals. Optimum performance is achieved with a bias between +2.5 V and +3 V. Differential phase linearity is best at this bias level.

A general-purpose 16-channel video multiplexer is shown in Figure 12. DC biasing is achieved with the divider network R1 and R2. A differential video buffer amplifier (NE5539) removes the DC level and enables greater multiplexing rates than achieved with capacitive decoupling. The unity gain buffer amplifier

arrangement is useful for providing impedance matching and greater drive for transmission stages.

Alternatively, the device supplies can be offset to eliminate the need for 16 separate bias circuits. Such an arrangement, shown in Figure 13, could be used in a security system or in a remote industrial monitoring system. The DG535/536 positive supply and ground pins (at -3 V) should be heavily decoupled to the video camera ground connections.

The switching threshold of the device at a supply voltage of +15 V is approximately between +6 V and +8.5 V above the substrate potential (Figure 14). Since the substrate is held at -3 V, the effective switching threshold referenced to ground is between +3 V and +5.5 V. Thus, the device can still be controlled from CMOS logic signals (provided that the logic 0 (V<sub>AL</sub>) is less than 3 V and logic 1 (V<sub>AH</sub>) is greater than +5.5 V).

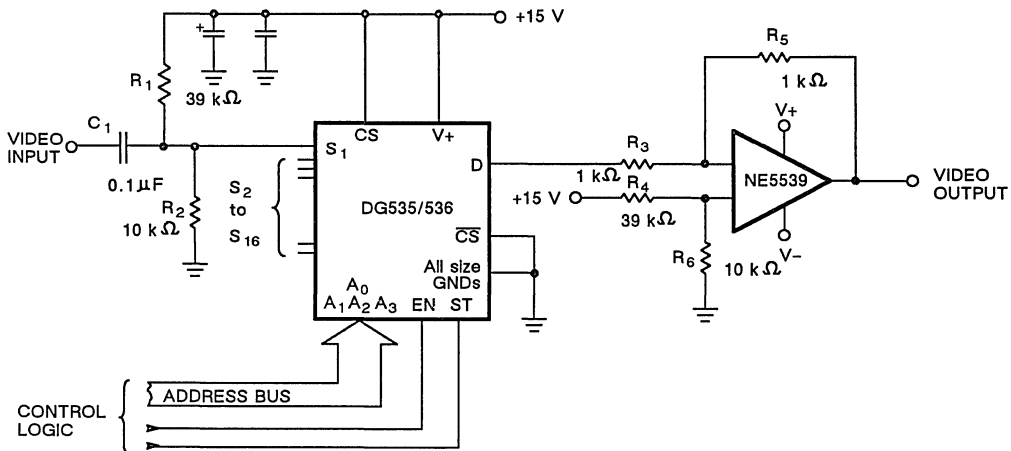


Figure 12. General-purpose 16-channel Video Multiplexer

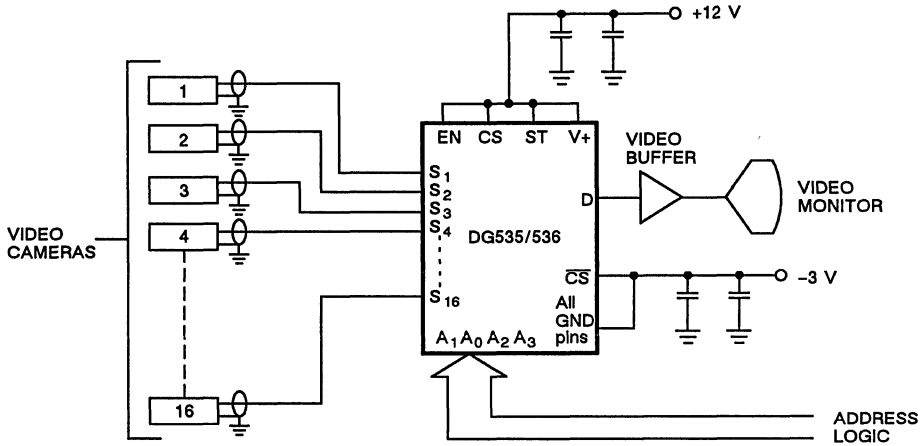


Figure 13. A Closed-Circuit Monitoring System

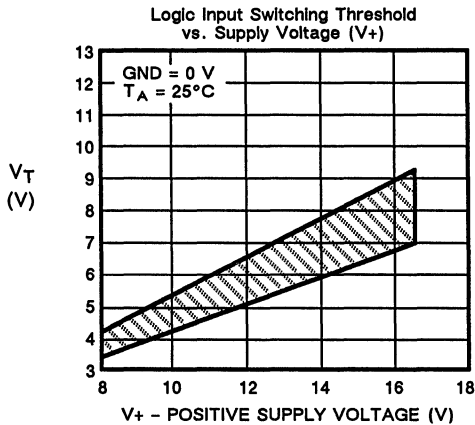


Figure 14. Logic Input Switching Threshold vs. Supply Voltage

In applications involving reduced supply voltages and offset conditions, the input switching threshold ( $V_T$ ) may be reduced below the CMOS logic "0". This may cause the address inputs to appear permanently

as logic "1" regardless of the control logic states. Therefore, control logic level shifting may be needed and can be accomplished in a number of ways with the additional benefit of providing TTL logic compatibility.

As shown in Figure 15, a comparator can be used for address logic level shifting. The Siliconix L161 comparator is ideal for use in conjunction with the DG535/536 since it features exceptionally low power consumption (typically microwatts). TTL compatibility is achieved by setting  $V_{REF}$  to +1.5 V.

While this solution maintains low power consumption, the transition speed of the system will be degraded by the response time of the comparator. However, at the expense of power consumption, the slew rate and transition speed of the L161 can be increased by reducing  $R_{SET}$  (see L161 data sheet).

To achieve fast switching, a high-speed analog switch, such as the DG271 shown in Figure 16, can be used as the interface. The high-speed switching (75 ns) and TTL logic compatibility of the DG271 makes it an ideal logic interface for the DG535/536 where "fast" multiplexing is required.

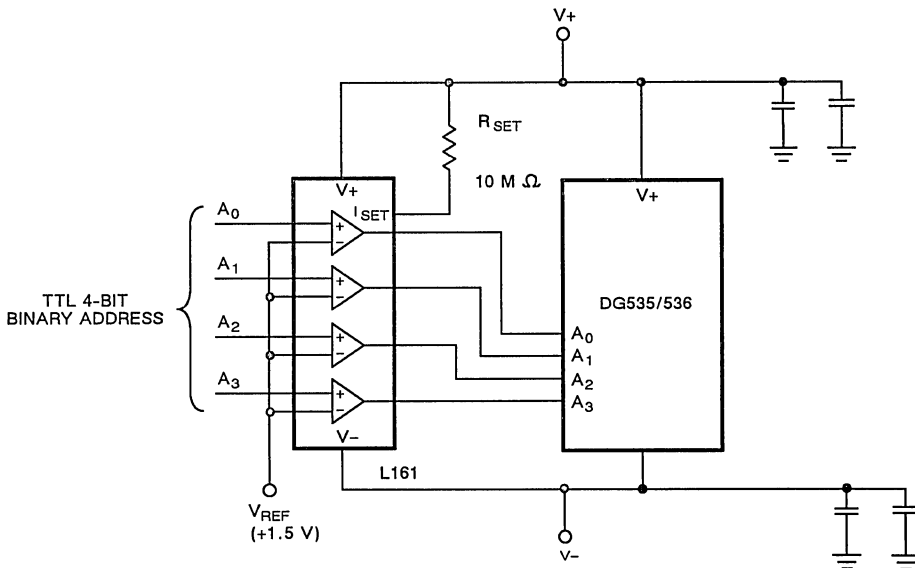


Figure 15. Using the L161 Quad Comparator for Address Logic Level Shifting

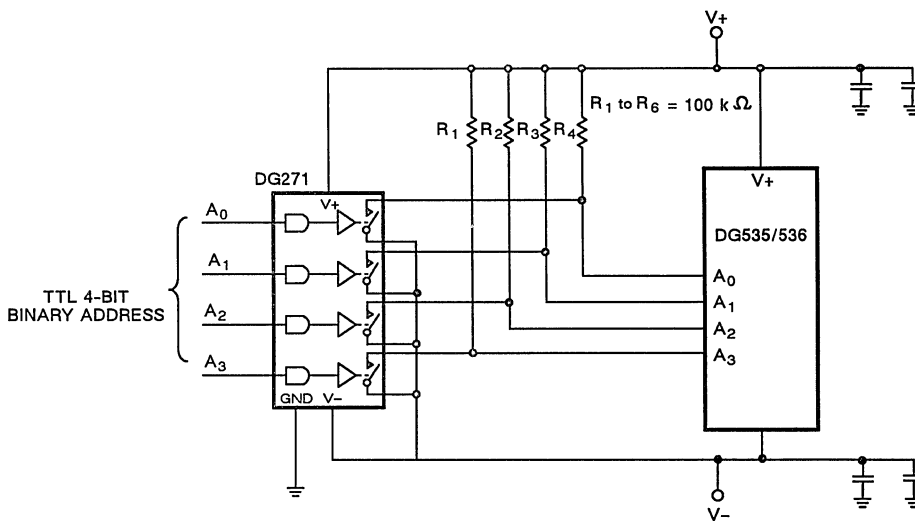


Figure 16. Using the DG271 for Address Logic Level Shifting

Another technique for achieving high-speed level translation at a reasonably low cost uses D169 dual driver ICs (see Figure 17). The D169 driver can drive up to +40 mA continuously and is therefore extremely suitable for applications where many DG535/536s are to be driven from a single address bus, such as in

multichannel crosspoints or large switching matrices. For single supply applications, TTL to CMOS level shifting can be easily accomplished using inexpensive CMOS level shifters such as the CD4504 or CD40109.

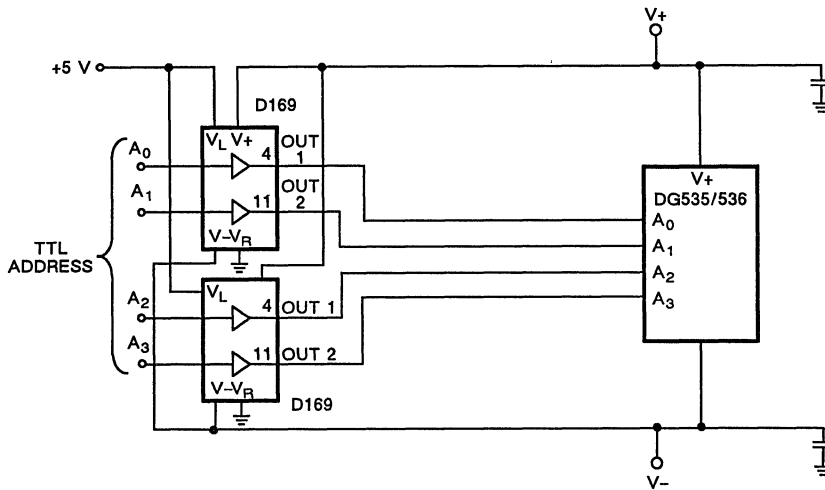


Figure 17. Level Translation using D169 Dual Driver ICs

## CROSSPOINT SWITCHING

Many analog and digital systems, such as a central router used in a video studio console (Figure 14), require crosspoint switching functions. In this application, many channels route signals to many different outputs. Due to its small outline PLCC package and low power consumption, the DG536 leads itself easily to multichannel crosspoint functions.

Figure 18 illustrates how the DIS (disable) pin can be used to indicate which output is selected. When logic 1 is applied to output select, device 1 is enabled and device 2 is disabled. With device 1 enabled, the DIS pin is connected to signal ground, thus turning LED 1 on. With device 2 disabled (due to  $\overline{CS}$  being 1), its DIS pin represents a high impedance to ground and LED 2 is off.

Any one of sixteen inputs can be connected to either output. This is achieved by applying the appropriate

CMOS logic address to the address inputs (A0 to A3) and applying the appropriate logic level to output select simultaneously.

The circuit in Figure 18 also illustrates how the chip select inputs can be used. As shown in Figure 19, a 32-channel single-ended multiplexer can be configured without external chip select circuits. This circuit makes use of the CS and  $\overline{CS}$  inputs which allow device selection from a single control line.

The basic circuit shown in Figure 18 can be extended and elaborated to give a 16 X 16 matrix for video crosspoint applications such as central routers used in video studios. This circuit, shown in Figure 20, allows source (or video input) to be connected to any video output (or any number of outputs). The strobe input (ST) on each device is used to latch the appropriate address into that particular device. By strobing the required address into each device sequentially, any crosspoint connection can be made.

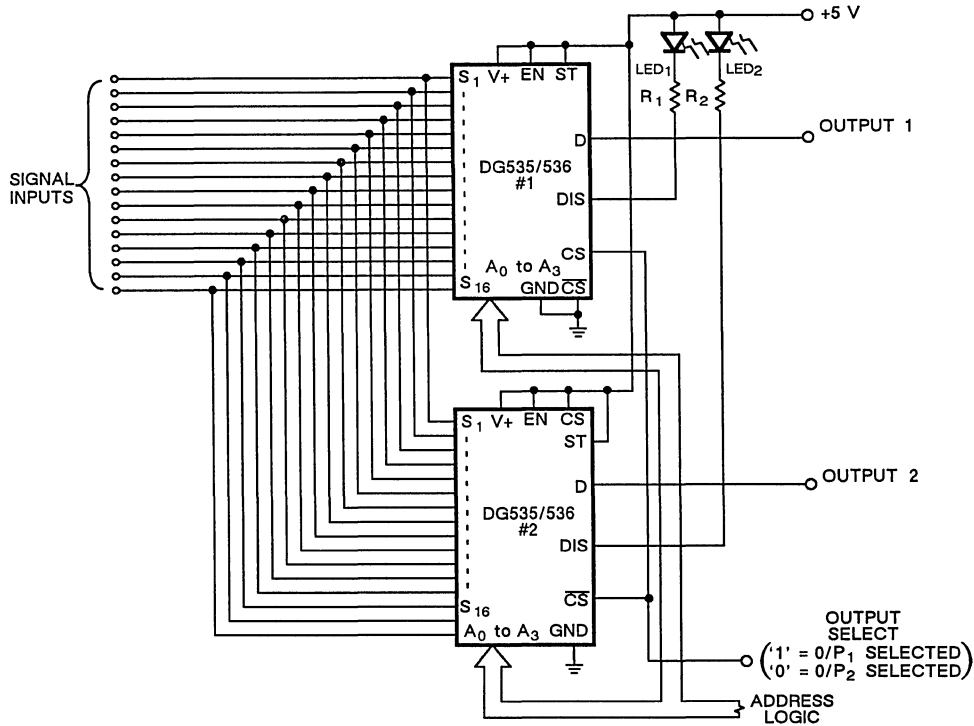


Figure 18. The DG535/536 as a 16 x 2 Matrix Switch

The DG535/536 makes an excellent digital switch due to its low channel-to-channel crosstalk, high off-isolation, and wide bandwidth specifications. In digital data transmission systems, the DG535/536 can easily handle data rates in excess of 100 Mbps.

The circuit shown in Figure 20 can be used as a digital cross-point to replace expensive, power consuming ECL crosspoint ICs. Besides handling raw digital data, the DG535/536 can also be used for other forms of data transmission, such as FSK and PCM systems.

### FSK

Frequency shift keying (FSK), commonly used in data transmission networks, relies on representing the digital code with frequency sine wave bursts. An FSK multiplexing system block diagram is shown in Figure 21. Each digital level has a specific signal frequency. The DG535/536 can be used to multiplex 16 different digital channels into a single transmission line or into a transmitter. Similarly, a DG535/536 may be used to demultiplex the data at the receiving end. Since the device can manipulate higher frequency sine waves, data can be transmitted at a higher rate than with a conventional multiplexer.

## PCM

A more commonly used and faster form of digital data transmission is known as PCM (pulse coded modulation). Used in telecommunications systems, PCM converts analog speech signals into 8-bit digital words for serial transmission. The data transfer rate used (for 4 kHz bandwidth voice signals) is 'up to 274.176 Mbps.

The DG535/536 can be used to route PCM signals in main telephone exchanges, replacing bulky hard-wired distribution frames. PCM highways can thus be rerouted remotely, under computer control, rather than manually.

RZ (returns to zero) PCM data consists of three discrete (ternary) levels to overcome long periods of zeroes (Figure 18). Digital signals can degrade beyond legibility after only a few hundred yards of travel down a transmission line. Therefore, the PCM signals must be regenerated at regular distances to avoid excessive distortion.

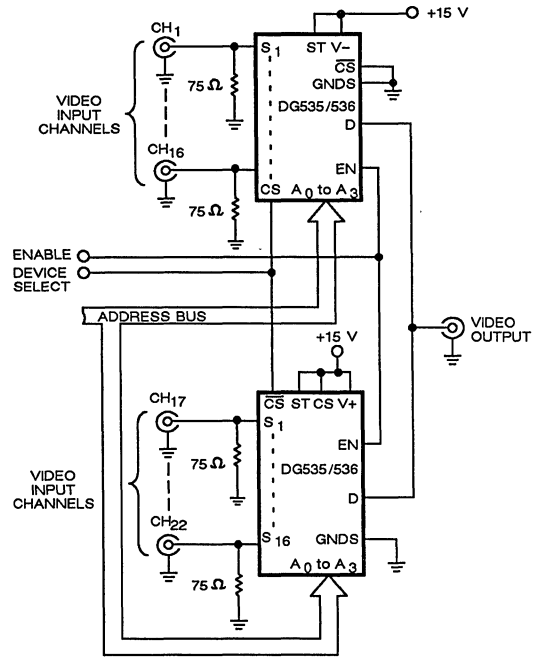


Figure 19. 32-Channel Multiplexer

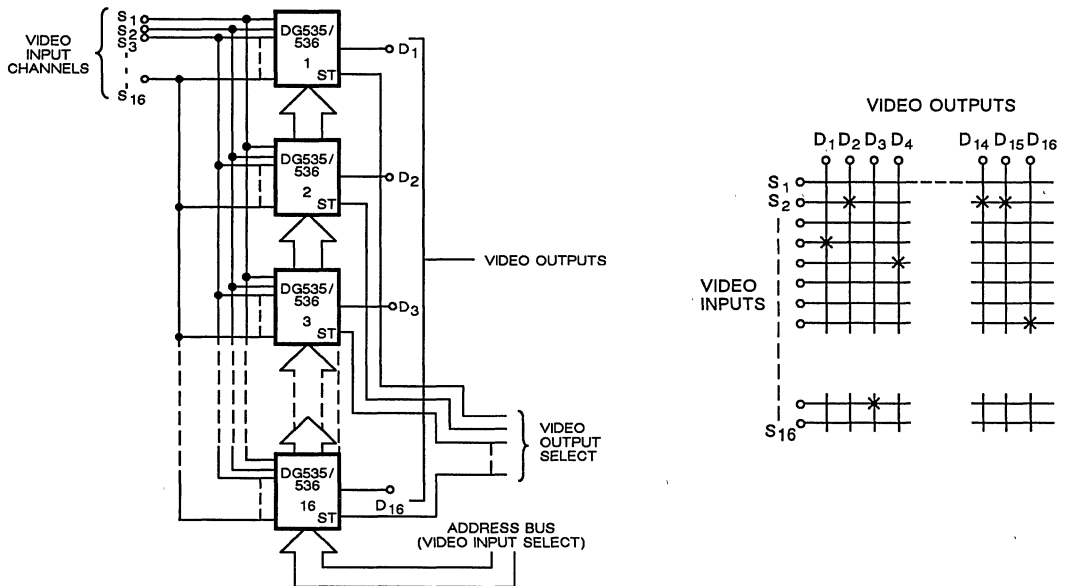


Figure 20. 16 x 16 Video Crosspoint Circuit



Figure 23 shows the architecture of a conventional binary distribution frame in a telephone exchange. Signal regeneration is applied to handle degradation during transmission and routing. Code converters are required to change the ternary PCM into binary PCM for routing within the distribution frame. Similarly, code converters are required to reconvert the binary PCM into ternary PCM for transmission.

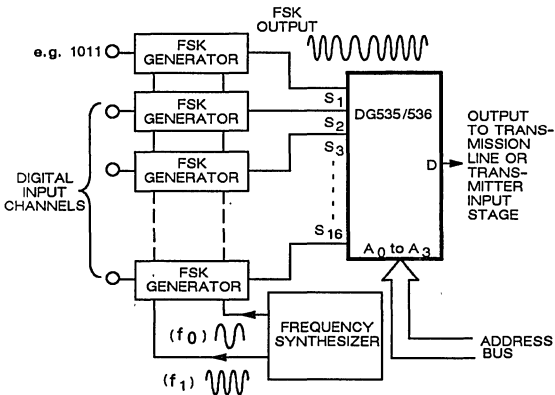


Figure 21. FSK Multiplexing System Block Diagram

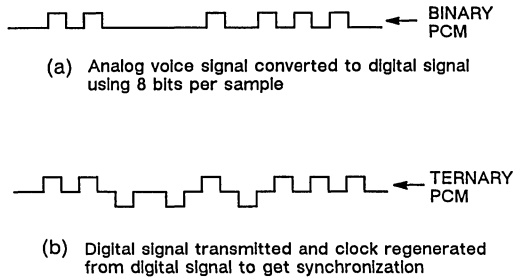


Figure 22.

Unlike digital switches which require specific digital signals, using the DG535/536 in the distribution frame (Figure 24) eliminates the need for code conversion and meticulous regeneration because it can handle analog signals.

**PROGRAMMABLE GAIN VIDEO AMPLIFIER**

The circuit shown in Figure 25 uses the DG535/536 video frequency handling capability to switch feedback resistors in a precision-programmable gain-video amplifier circuit.

Gain of the op amp is set by

$$A_v = \frac{R_1 + R_{Feedback}}{R_1}$$

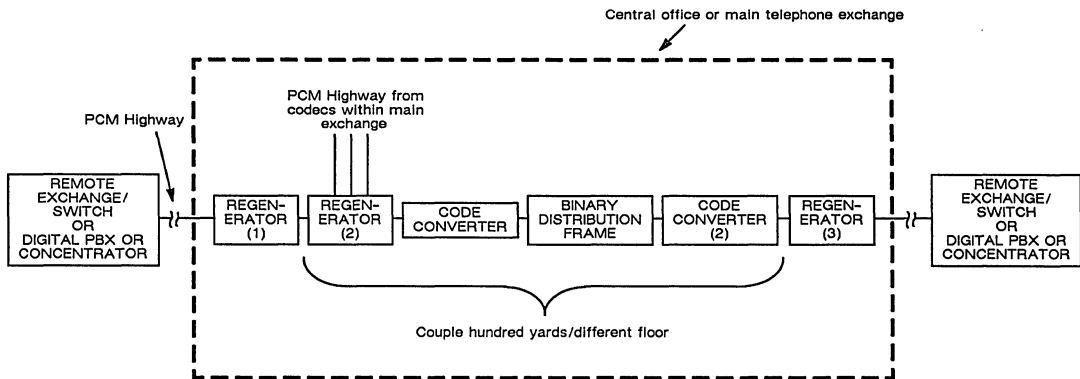


Figure 23. Binary PCM Routing Network

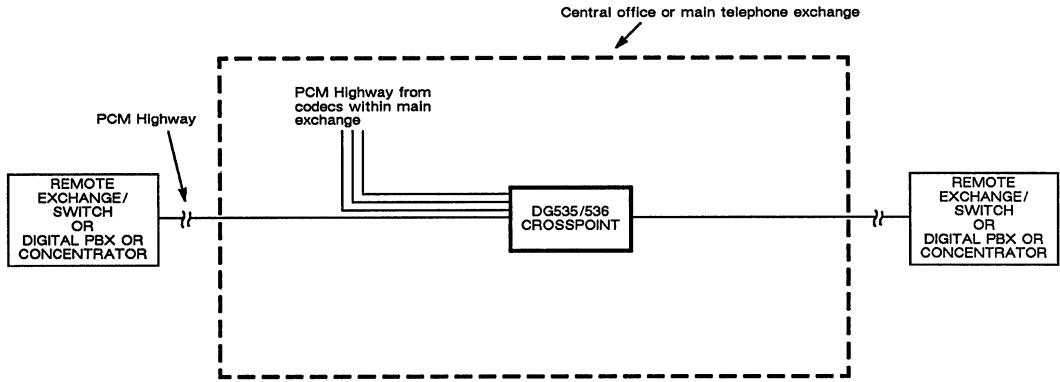


Figure 24. DG536 PCM Distribution Frame

For example, when  $R_1 = 1\text{ k}\Omega$ , the results are

Logic Input	R Feedback	Gain ( $A_V$ )
0000	$0\ \Omega$	1
0001	$1\text{ k}\Omega = (R_A)$	2
0010	$2\text{ k}\Omega = (R_B)$	3
0011	$3\text{ k}\Omega = (R_C)$	4

The low and fairly constant ON-resistance of the DG535/536 gives good gain stability, and the resistor tolerances determine the gain error of the circuit. The accuracy of the circuit is, therefore, limited by the op amp CMRR and offset, and the gain of the circuit is limited by the analog signal range of the DG535/536.

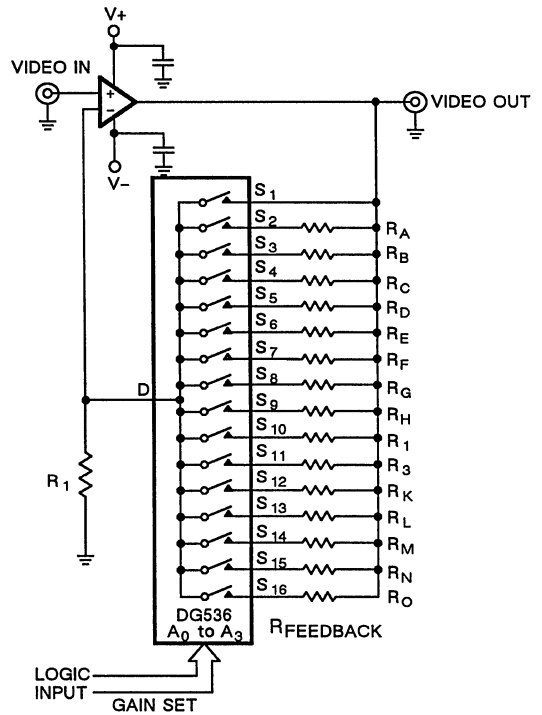


Figure 25. Precision Programmable Gain Video Amplifier

**ATE**

A simple but accurate ATE system, as shown in Figure 26, can be designed for testing digital processing boards.

The propagation delay time for each of the 16 digital signal paths can be tested individually, with negligible errors due to the very small propagation delay through the DG535/536. Also, the variation of delay times from channel to channel is less than 0.25 ns.

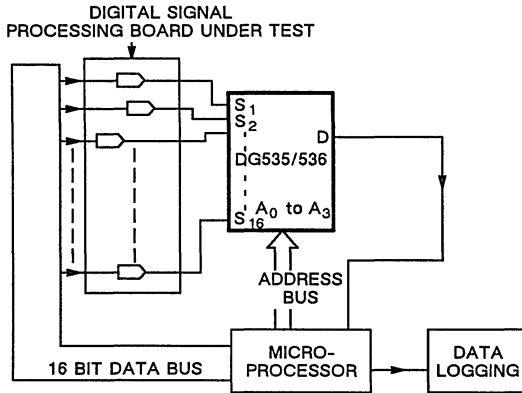


Figure 26. ATE Applications

**MICROPROCESSOR INTERFACE CIRCUITS**

On-chip data latches in the DG535/536 simplify interface with a microprocessor data bus. This eliminates the need for peripheral memory devices (such as I/O ports or D-type latch ICs) to maintain switch addressing while the processor uses its data bus for other functions.

The data latches are activated by the DG535/536 strobe input (ST). The latch is transparent when ST = logic 1, thus the device responds to changes of data at the address inputs. When ST = logic 0, the previous data is latched into the device, regardless of new data appearing at the address inputs.

The DG535/536 timing arrangements meet the requirements of popular microprocessors, such as the 8085A, 6800, and Z80. The 8085A to DG535/536 interface is shown in Figure 27, and Table 3 illustrates the timing compatibility of the DG535/536 with the 8085A and the faster 8085A-2 devices.

Figure 24 shows the complete 6800 to DG536 interface circuit. In order to have a data valid signal, it is necessary to NAND the  $\overline{R}/\overline{W}/\overline{CS}$  gate output with the  $\phi_2$  clock (usually connected to the DBE pin). This makes the interface circuit functionally compatible with the 8085A interface shown in Figure 27.

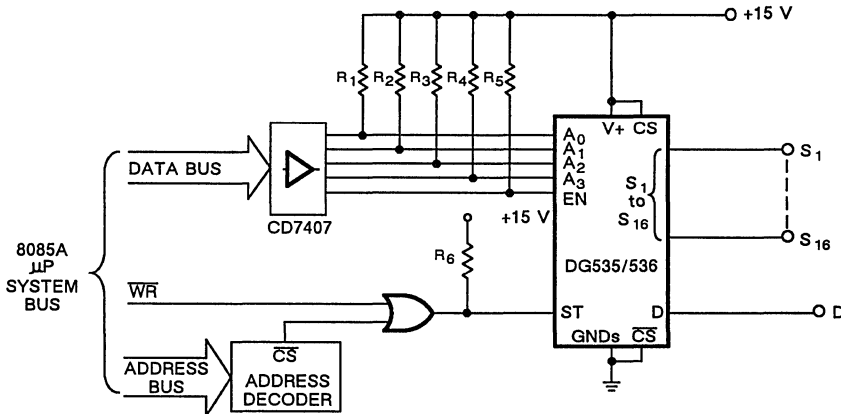


Figure 27. 8085A to DG535/536 Interface

Specification	8085A ns./min.	8085A-2 ns./min.	DG536 ns./min.
$t_{SW}$ (strobe pulse width)	400	230	200
$t_{DW}$ (data valid to strobe)	420	230	100
$t_{WD}$ (data valid after strobe)	100	60	50

Note that open collector gates and buffers could be used to level shift the TTL logic levels from the microprocessor to the CMOS levels required by the DG535/536 logic inputs.

To achieve the correct ST signal in a Z80 processor system, the  $\overline{WR}$  and  $\overline{MREQ}$  signals must be gated with the standard CS signal, as shown in Figure 29.

## LOW ANALOG SIGNAL SWITCHING/MULTIPLEXING

The DG535/536 has several uses in handling low-level analog signals (such as in medical equipment or ul-

trasound transducer multiplexing) because the device exhibits inherently low noise and offset voltages. Two factors affect offset voltage:

1. Thermoelectric offset voltage is produced by the incidental thermocouples that exist within the integrated circuit. There are many inter-metallic junctions within an IC. These junctions act as individual thermocouple, has an identical reversed counterpart. That is, from source to drain, we have gold-aluminum/aluminum/aluminum-silicon and silicon-aluminum/aluminum-gold. Therefore, if the temperature surrounding each junction is constant and equal, the thermal EMFs cancel each other, giving a zero net offset voltage. Since a thermal gradient always exists across the chip, then there is always a net thermoelectric offset voltage. For the DG535/536, the thermal EMFs produced on chip are small since the device exhibits a low power consumption (75  $\mu$ W), producing a low temperature on the die.
2. Leakage current offset is caused by leakage current flowing through the  $r_{DS}$  of an ON switch and/or the load resistance. The offset voltage developed due to leakage current is negligible since the device has very low leakage currents (a benefit incurred by the two-level system) coupled with very low ON-resistance.

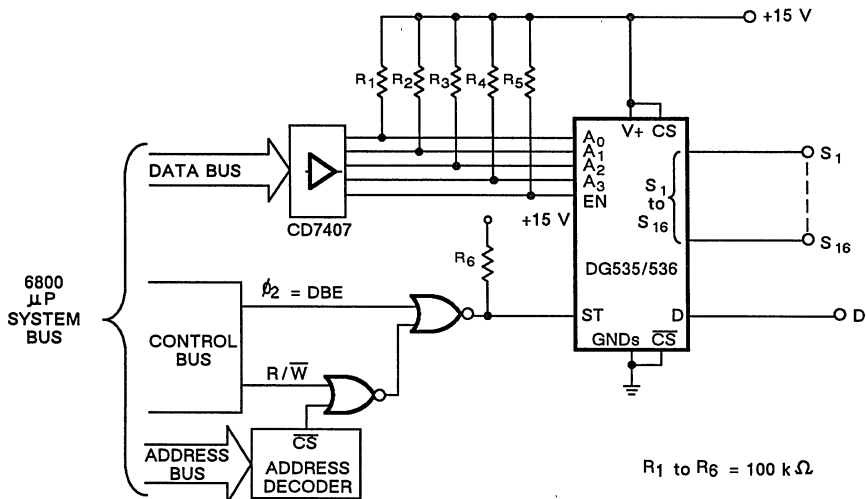


Figure 28. 6800 to DG535/536 Interface

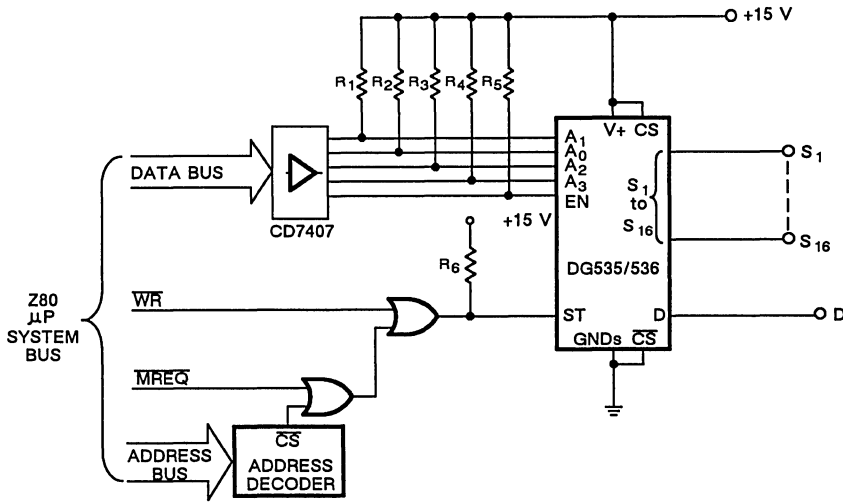


Figure 29. Z80 to DG536 Interface

For example:

$$\begin{aligned}
 V \text{ (offset)} &= I_{D(ON)} \times r_{DS(ON)} \\
 &= \pm 100 \text{ pA (typical @ } 25^\circ\text{C)} \\
 &\quad \times 55 \Omega \text{ (typical)} \\
 &= \pm 5.5 \text{ nV (typically)}
 \end{aligned}$$

The circuit shown in Figure 30 can be used to remotely monitor up to 16 different thermocouples with high accuracy. The output of the thermocouples is in the form of a small dc voltage, on the order of millivolts, with typical voltage changes on the order of tens of microvolts per °C. Thus, voltage offset developed by the switching devices can frequently limit system accuracy.

Using the differential multiplexing technique shown in Figure 30, high resolution can be achieved since the thermal EMFs produced by each DG535/536 are canceled as common mode voltages at the instrumentation amplifier inputs. To minimize pick-up and noise effects, the same PC board layout rules apply for this type of circuit. Best accuracy is achieved by ensuring that the multiplexers are kept close together in a thermally stable environment.

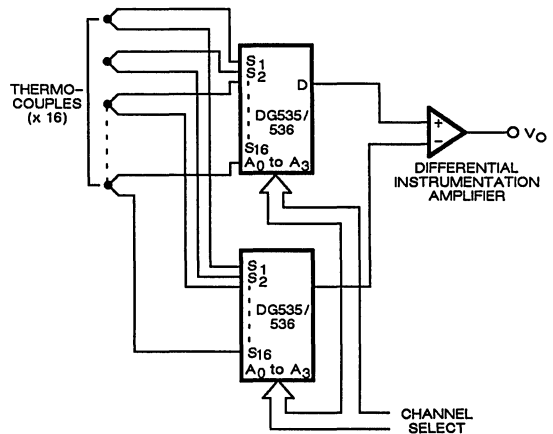


Figure 30. Thermocouple Multiplexing System

## THEORY AND APPLICATIONS OF THE Si7660 AND Si7661 VOLTAGE CONVERTERS

Doyle L. Slack  
Revised February 1988

### INTRODUCTION

Many times a simple digital circuit design can be greatly complicated by the needs of just one or two of the onboard devices. For example, analog devices often used along with digital circuits (such as op amps and data acquisition systems) are notorious for negative voltage requirements of  $-5$ ,  $-10$  or  $-15$  V when everything else in the circuit needs only positive voltages. Until recently, the only answer was to either buy a dc to dc converter module (expensive) or redesign the power supply to generate the negative voltages (expensive and wasteful in parts count and space). This Application Note presents the best alternative to this problem: the Si7660 and Si7661 monolithic voltage converters. With the Si7660 and Si7661, negative voltages from 1.5 to 20 V can be generated from a positive supply with minimum parts count and minimum cost.

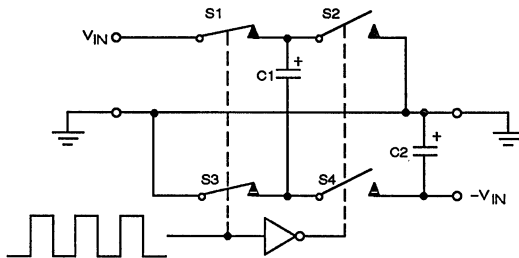


Figure 1. The Ideal Voltage Doubler

### Theory Of Operation

The basic theory behind the Si7660 and Si7661 is the same and is based on the ideal voltage doubler shown in Figure 1. Capacitor  $C_1$  is the pump capacitor, and  $C_2$  is the reservoir capacitor. The pairs of switches ( $S_1$  with  $S_3$ , and  $S_2$  with  $S_4$ ) are driven by

an oscillator/toggle circuit, providing charge and transfer cycles of equal length.

During the charge cycle,  $S_1$  and  $S_3$  are closed, and current flows into  $C_1$ , charging it to the value of  $V_{IN}$ . The oscillator toggle then changes state, and the transfer cycle begins.  $S_1$  and  $S_3$  are opened while  $S_2$  and  $S_4$  are closed, allowing  $C_1$  to dump charge into  $C_2$  until the potential across them has equalized. The oscillator/toggle then switches again, and the process starts over.

For no load conditions, the voltage inversion will be virtually perfect since the amount of charge that must be transferred from  $C_1$  to  $C_2$  will be limited to losses due to leakage from  $C_2$  and any parasitic capacitances. As the load increases,  $C_1$  must transfer more and more charge to make up for the depletion of  $C_2$  as it supplies current to the output during the charge cycle. This action causes the output voltage to drop, making the circuit appear to be a perfect inverter in series with an output resistor that varies in magnitude with the input voltage. Figure 2 shows this concept in a two port diagram of the device, and Figure 3 illustrates the typical output characteristics of both devices configured in the inverter mode.

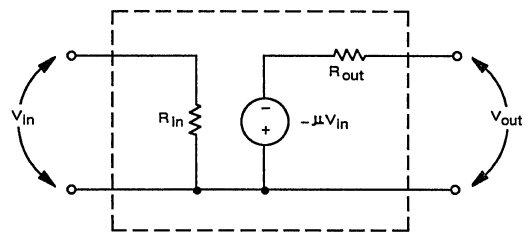


Figure 2. Two-Port Diagram of the Voltage Converter Circuit

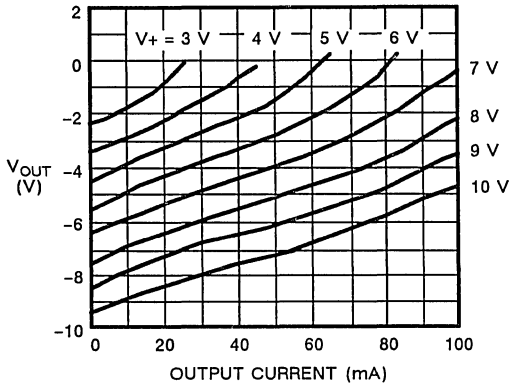


Figure 3(a). Output Characteristic of the Si7660 Voltage Converter.

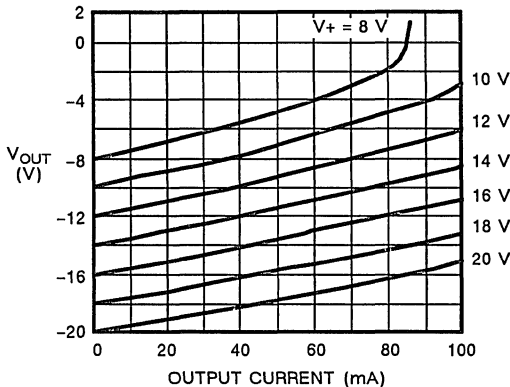


Figure 3(b). Output Characteristic of the Si7661 Voltage Converter.

## Circuit Operation

With the Si7660 and Si7661, the only parts of the doubler not included inside the package are the pump and reservoir capacitors. The internal switches are made with P-channel and N-channel MOSFETs. The main difference between the Si7660 and Si7661 is the breakdown voltage of the MOSFETs which in turn dictates the maximum input voltage. Also, the design of the Si7661 offers a much greater resistance to device latchup, which is discussed later. Since the internal sections of the two devices

are very similar, description of the operation of the Si7660 and Si7661 is combined. The internal sections of the circuit are the oscillator, divider, regulator, level translator, and substrate logic. Figure 4 shows a block diagram of the internal sections of the inverter circuit.

The oscillator supplies the signal to the divider section which in turn drives the rest of the circuit. The OSC input has an input impedance of approximately 1 M $\Omega$ . This allows the internal oscillator to be overridden by an external clock or to be slowed down by the addition of an external capacitor.

The internal regulator is a series voltage regulator with a zener reference to insure that low voltage components of the circuit are provided with no more than 5 V when the input voltage is greater than 5 V. It also provides current limiting for the oscillator and divider circuits. When the input voltage is less than 3.5 V for the Si7660 (less than 9.0 V for the Si7661), the LV pin is grounded, bypassing the internal regulator. However, when the Si7660 is operated above 3.5 V, the LV pin must be left open to provide latchup protection. For the Si7661, LV should be left open above 9.0 V for proper operation.

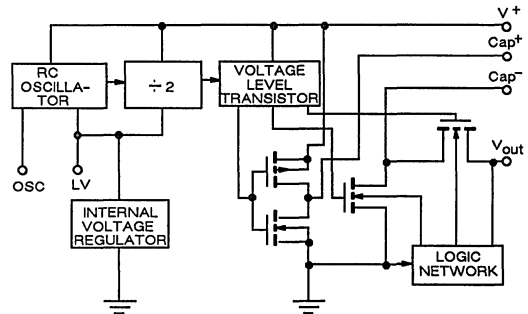


Figure 4. Block Diagram of the Voltage Converter Circuit

The divider is simply a divide-by-two counter that provides complementary outputs. Q and  $\bar{Q}$  drive the inputs of the level translators, which in turn provide the necessary switching voltages to drive the MOSPOWER switches. The built-in delay of the translators guarantee that break-before-make action occurs.

The substrate logic network insures that two things happen. First, it makes sure that the substrate-source/drain junctions of  $Q_3$  and  $Q_4$  are never forward biased, and that the ON resistance of each of the output transistors will be as low as possible for all operating conditions. Second, the network determines the most negative voltage in the device and uses it to supply power to the level translator.

Figure 5 gives the pin configuration of the Si7660 and Si7661. These devices are pin compatible with competitive products. Functionally, the Si7660 is an exact replacement of the industry standard voltage converter competition while the Si7661 provides the advantage of greater voltage range at the expense of slightly higher output resistance.

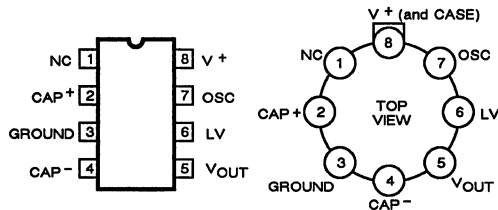


Figure 5. Pin Diagrams of the TO-99 and 8-Pin DIP Packages for the Si7660 and Si7661

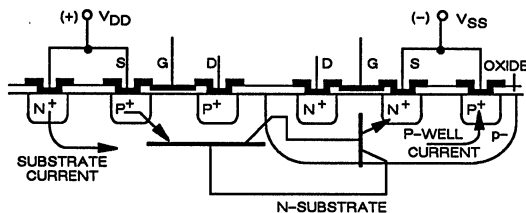


Figure 6. Intrinsic SCR Superimposed on a CMOS Gate Structure

## Latchup

Because of the basic internal four-layer geometry of CMOS devices, an SCR action can sometimes occur. Figure 6 depicts the SCR structure. This SCR action can, under certain conditions, cause the Si7660 de-

vice to latch up. As Figure 6 shows, the source of the N-channel device becomes the SCR cathode; the source of the P-channel is the anode; and either drain can act as a gate. Since an SCR does not trigger until certain conditions occur, it can sometimes cause no problems at all, yet sometimes it may be fatal to the CMOS device.

The intrinsic SCR needs three conditions to cause latchup. First, the current gain products (betas) of the two parasitic bipolar transistors must be greater than one. Second, the current flowing through the channels of the devices must be greater than the holding current of the SCR. Finally, some kind of pulse must be applied to one of the gates to trigger the SCR action.

The trigger pulse can come from several different sources. The power-up sequence of the CMOS device may cause problems if the SCR gate receives power before the other terminals. Another possible trigger source is a high slew rate across the intrinsic SCR. When the SCR is triggered, the CMOS devices are suddenly shorted out by the SCR, and the output impedance of the device becomes very low.

$Q_4$  of the Si7660 can sometimes experience the conditions to cause SCR latchup when operating at the upper end of the input voltage range. The nearby P-channel substrate logic transistors form the complementary part of the intrinsic SCR. When the SCR action does occur, the circuit suddenly appears to be a short circuit between  $V_{IN}$  and  $V_{OUT}$ . The reservoir capacitor ( $C_2$ ) rapidly discharges through this path. After  $C_2$  has discharged, the current through  $Q_4$  drops below the SCR holding value, and the circuit resets. If the conditions that originally caused the SCR action remain present, the device will latch up repeatedly. If the circuit input is not current limited, this action can sometimes dissipate too much power through  $Q_4$  and the substrate logic, resulting in damage to the device.

To prevent damage to the Si7660 when conditions for latchup occur, older versions required a diode in series with the  $V_{OUT}$  pin to block the discharge of  $C_2$  and keep the current below the holding value of the SCR. This diode was used whenever the input voltage could exceed 6.5 V at room temperature. Figure 7 shows the operating range of the improved Si7660.



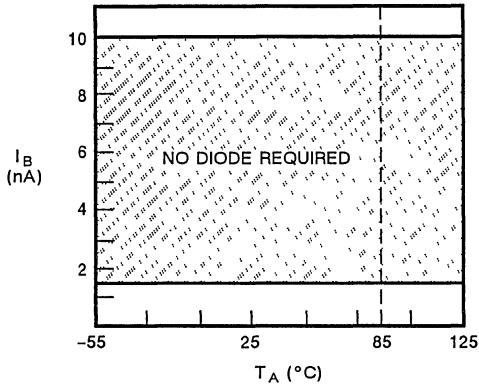


Figure 7. Range of Input Voltage and Operating Temperature for the Si7660

The Si7661 is a higher voltage device than the Si7660, and is designed on a different process. This high voltage silicon gate process reduces the parasitic betas in Q<sub>4</sub> to a value that makes it extremely difficult to produce the conditions for latchup. Because of this, the series diode is not needed for proper operation.

### General Applications

The Si7660 and Si7661 are intended for use as voltage inverters. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. In some configurations, they can even provide more than one voltage output at the same time. The possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication.

### Basic Voltage Inversion

With no load, the output voltage magnitude of the basic voltage inverter circuit shown in Figure 8 will typically be within 0.1% of the V<sub>+</sub> (input voltage) magnitude for the Si7660 and within 0.3% of the input voltage magnitude for the Si7661. As the load current increases, the output will drop as shown in Figure 9(a). The effective output resistance will vary with input voltage as given in Figure 9(b). Once the load current reaches its limit (30-40 mA for the 5 V case), the inverter can no longer regulate the voltage properly and shuts down to protect itself from extreme power dissipation.

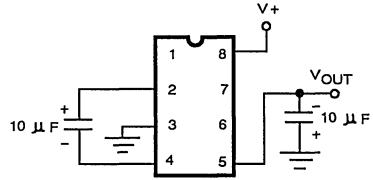


Figure 8. Schematic Diagram of the Basic Inverter Circuit

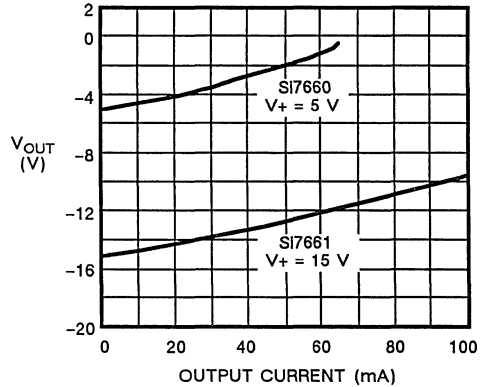


Figure 9(a). Variation of Output Voltage as a Function of Output Current

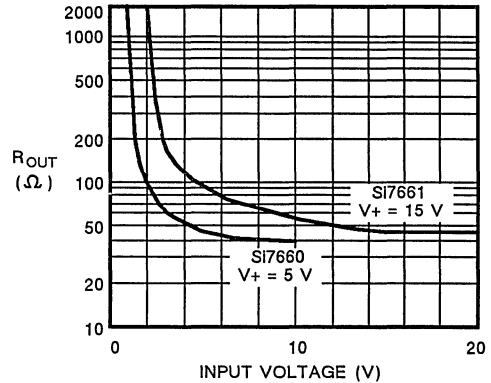


Figure 9(b). Variation of Output Resistance as a Function of Input Voltage.

**CAUTION:** At higher input voltages (for either device), the output maximum limit can cause the power dissipation to exceed the maximum rating of the package (especially plastic). Always calculate the maximum power dissipation for your design.

TABLE 1

Effect of Varying the Pump and Reservoir Capacitor Size on Output Ripple Noise.

	Capacitors ( $\mu\text{F}$ )	$V_{\text{OUT}}$ (V)	$V_{\text{R}}$ ( $mV_{\text{p-p}}$ )
Si7660	10	-3.838	150
Inverter Mode (see Figure 8)	22	-3.862	75
	47	-3.873	30
$V_+ = +5\text{ V}$	100	-3.874	26
$I_{\text{OUT}} = 10\text{ mA}$	470	-3.879	10
	1000	-3.880	5
Si7661	10	-13.849	175
Inverter Mode (see Figure 8)	22	-13.872	80
	47	-13.882	38
$V_+ = +15\text{ V}$	100	-13.883	29
$I_{\text{OUT}} = 10\text{ mA}$	470	-13.885	10
	1000	-13.890	5

The output ripple of the inverter is a function of the oscillator frequency as well as the size of the pump and reservoir capacitors. The nominal oscillator frequency is 12 kHz for the Si7660 and 10 kHz for the Si7661. Because the output ripple is important in some linear applications where supply noise is critical, Table 1 provides ripple values for different pump and reservoir capacitor values.

It is important to note that increasing the capacitor size can lead to other difficulties. The main problem is that the large capacitors may draw excessive amounts of current at turn-ON. If the current is too great, the power dissipation of the device can be exceeded causing destruction of the converter. Even when the device is running, the charge transfer under heavy loads can push the switches to their limits.

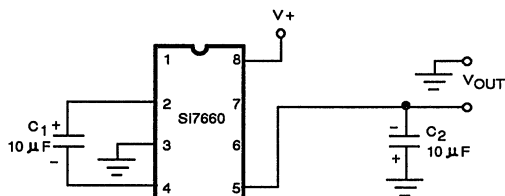


Figure 10. Inverter Circuit Connections for High Voltage Operation

As stated before, the LV pin shorts out the internal regulator at low voltages when it is tied to ground. The LV pin should be grounded for operation below 3.5 V for the Si7660 and 9.0 V for the Si7661. However, it is necessary to leave the LV pin floating for high voltage operation, as shown in Figure 10. Failure to do so could permanently damage the device. Figure 11 shows the inverter configured for low voltage operations.

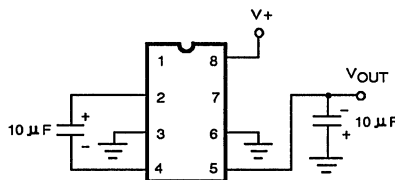


Figure 11. Inverter Circuit Connections for Low Voltage Operation

## Voltage Multiplication

Since the inverter design is based on the ideal voltage doubler, it is easy to convert the Si7660 and Si7661 devices to provide doubling of the input voltage. Figure 12 gives the schematic diagram of the

voltage doubler. This circuit requires only two additional diodes and will provide positive voltage multiplication at the expense of the voltage drops of the two diodes in series with the output. This means the positive multiplier will not be able to provide the near perfect output function like the basic inverter circuit does. The output voltage of the multiplier will be:

$$V_{OUT} = 2 (V+) - 2 V_{diode} \quad (2)$$

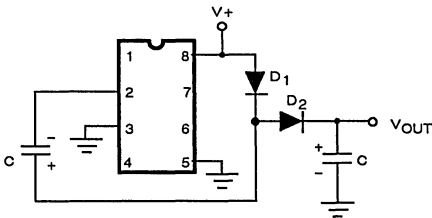


Figure 12. Voltage Doubler Schematic Diagram

The circuit of Figure 12 can also be used as a Negative-to-Positive voltage converter. To do so, set pin 8 to Ground and pins 3 and 5 to the negative input voltage, V-. The output voltage will then be:

$$V_{OUT} = | V- | - 2 V_{diode} \quad (3)$$

### Simultaneous Inversion And Multiplication

The circuit shown in Figure 13 will provide both positive multiplication and inversion at the same time. The output voltages will be the same as those given in equations 1 and 2. This configuration is limited by the load current that can be drawn out of either output before the circuit becomes overloaded.

### Parallel Connection

Although a single Si7660 and Si7661 cannot supply very large amounts of current, higher currents can be provided when several devices are connected in parallel. As shown in Figure 14, two or more inverter circuits can be paralleled to provide a lower output

resistance, providing a smaller output voltage drop for a given current. This circuit will also expand the operating output current ranges slightly. Each device must have its own pump capacitor, but the reservoir capacitor is shared between all of the devices.

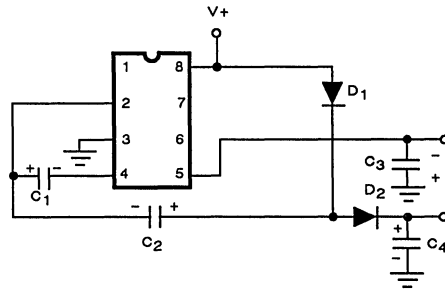


Figure 13. Combination Inverter/Multiplier Circuit

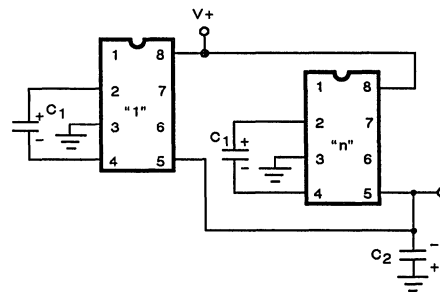


Figure 14. Paralleling Multiple Voltage Converters for Increased Current Capability

When two or more devices are paralleled, the output noise (ripple) will contain not only components at frequencies of each of the oscillators, but also at sum and difference frequencies due to a mixing action at the inverter outputs. If such noise cannot be tolerated, the OSC pin of one of the devices can be driven by an exclusive NOR gate that compares the oscillator frequencies of the two devices as shown in Figure 15. This forces the two devices to alternate their charge and transfer cycles, which will not only reduce output noise but also maximize efficiency.

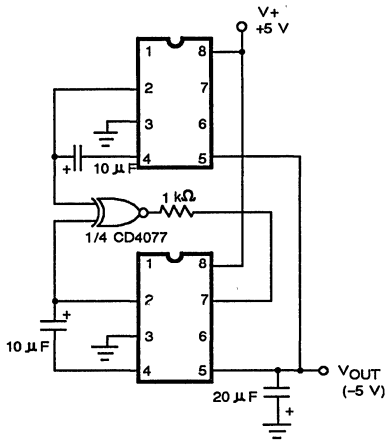


Figure 15. Synchronizing Two Si7660's or Si7661's with a Single Exclusive NOR Gate

## Series Connection

When high voltage inversion is desired, inverter circuits can be placed in series to produce voltage outside of the operating range of a single Si7660 or Si7661. Figure 16 shows two inverters cascaded to double the input voltage magnitude while inverting the voltage at the same time.

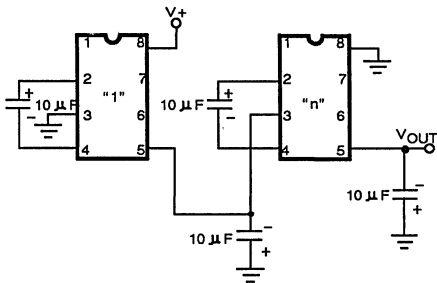
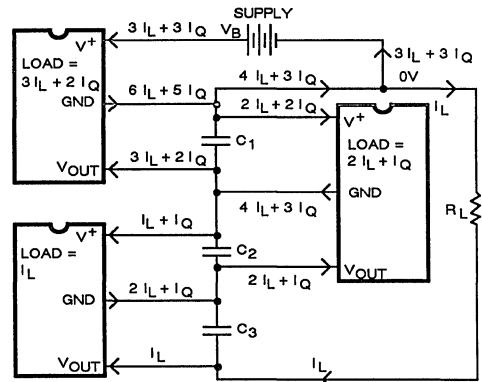


Figure 16. Cascading Devices for Greater Output Voltage Range

When cascading devices, however, the power dissipation of each device must be considered. As each new stage is added, the previous stages will be subjected to more and more load current, from both the quiescent current of the new stage and the multiplying action of the load current through each of the stages, as shown in Figure 17. As the number of cas-

caded devices increases, the effective output resistance also increases which will severely reduce the output voltage for a given current level when compared to a single inverter. This effect can be reduced by paralleling devices in the first stages, though the cost in parts increases twofold for every added stage.



$$V_{C1} = V_B - R_O (3 I_L + 2 I_Q) \quad V_{OUT} = - [3 V_B - R_O (14 I_L + 8 I_Q)]$$

$$V_{C2} = V_B - R_O (5 I_L + 3 I_Q)$$

$$V_{C3} = V_B - R_O (6 I_L + 3 I_Q)$$

Figure 17. Current Model of Cascaded Voltage Converters

## Changing The Oscillator Frequency

The typical oscillator frequencies were given in the description of the basic inverter circuit. However, Figure 18(a) shows that the maximum power efficiency is not achieved at the typical oscillator frequency. If maximum power efficiency is desired, an external capacitor can be connected between the OSC pin and ground. Figure 18(b) illustrates the effect of added capacitance on the oscillator frequency.

If synchronization with an external driver or clock is needed, the OSC pin can be driven either by a TTL or CMOS logic gate. Figure 19 provides the proper circuits for interfacing to either logic standard. Note that the TTL interface can only be directly connected to the OSC pin if the circuit is using a 5 V supply. If the input voltage is other than 5 V, some type of buffer circuit will be required. The charge/transfer transitions will occur on each rising edge of the clock.

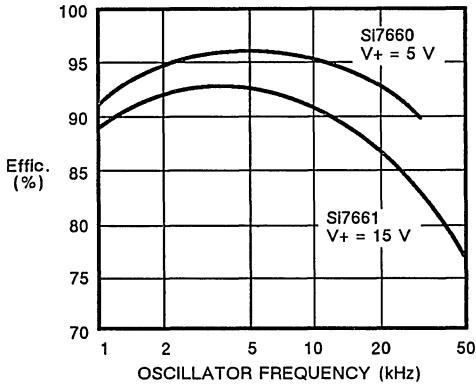


Figure 18(a). Graph of Efficiency Versus Oscillator Frequency

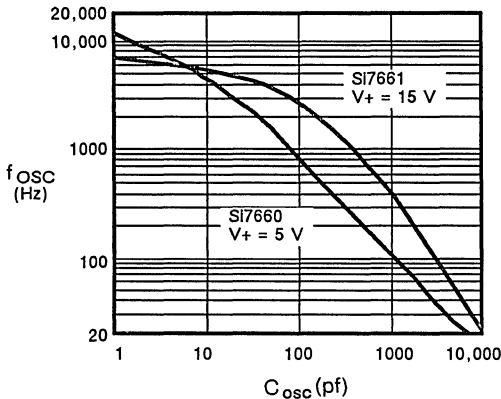


Figure 18(b). Graph of Oscillator Frequency Versus Added Capacitance

There are many places where a low current negative supply made with an Si7660 or Si7661 would do just as well as a full conventional negative supply or dc-to-dc converter module. Some examples of possible uses are power sources for operational amplifiers, dynamic RAM's, microprocessors, and data conversion products. Several examples of these systems are given below.

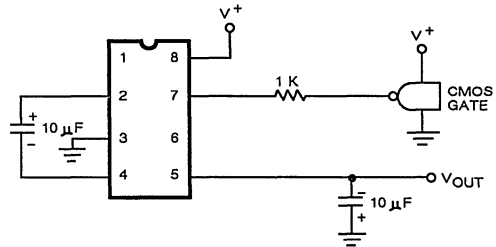


Figure 19(a). CMOS Drive Circuit for the Si7660 or Si7661

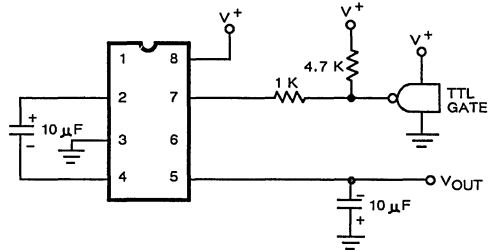


Figure 19(b). TTL Drive Circuit for the Si7660 or Si7661 (5 volt input only)

## Specific Applications

When looking at possible applications for the Si7660 and Si7661, it must be remembered that these devices are VOLTAGE sources, not CURRENT sources. Therefore, any heavy load will either greatly reduce output voltage (possibly out of the desired range) or cause the device to go into power shutdown. If the concept of VOLTAGE conversion is kept in mind, many problems will be avoided.

## Memories

Several different memory manufacturers produce 16K x 1 dynamic RAM's that have a need for a -5 V low current supply to provide substrate biasing. The National MM5290, AMD AM9016, and THOMSON MK4116 all use this type of arrangement. Table 2 gives the -5 V supply current requirements for each of these devices.

**TABLE 2**

Current Requirements of Several Different Dynamic RAMs.

Device	Operating Current ( $\mu\text{A}$ )	Standby Current ( $\mu\text{A}$ )	Refresh Current ( $\mu\text{A}$ )
MM5290 (0 to 70 °C)	200	100	200
AM9016 (0 to 70 °C)	200	100	200
AM9016 (-55 to 85 °C)	400	200	400
MK4116 (0 to 70 °C)	200	100	200

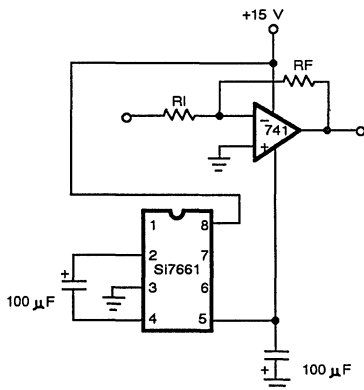
The only constraint in using the Si7660 or Si7661 for this application is when calculating the voltage fluctuations that will occur when a location is read from or written to. Make sure that the ABSOLUTE MAXIMUM current is considered so that the negative supply for the dynamic RAM will not be pulled down more than 5% (below 4.75 V) during a memory read or write. Even with the maximum current taken into account, the Si7660 or Si7661 could easily provide the negative supply voltage supply for an entire 16K x 8 dynamic memory bank.

### Op Amps

Operational amplifiers are one of the most commonly used integrated circuits and often use negative supply voltages. Although some op amps can supply high current loads, more often the current requirements involved are well within the capabilities of the Si7661.

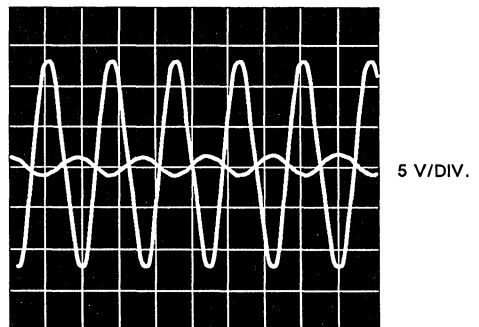
Figure 20 shows the Si7661 supplying the negative voltage to a 741 op amp configured as an inverting amplifier. As the current drain through the negative supply terminal of the op amp increases, the output voltage of the Si7661 will decrease. However, this will not affect the output capability of the op amp at its rated output current. Figure 21 illustrates this with a photograph of the input and output of the circuit in Figure 20 when a 1 k $\Omega$  load was placed on the amplifier output. The output was undistorted to 26 V peak-to-peak.

The output ripple of the Si7661 must be taken into consideration when using it as an op amp supply. Some op amps do not have adequate power supply rejection to withstand the ripple noise level of the Si7661. The pump and reservoir capacitors can be chosen to minimize this noise condition (see Table 1). The ripple should be measured at the maximum negative supply current (i.e., rated load) to determine if the Si7661 can be used to supply the op amp.

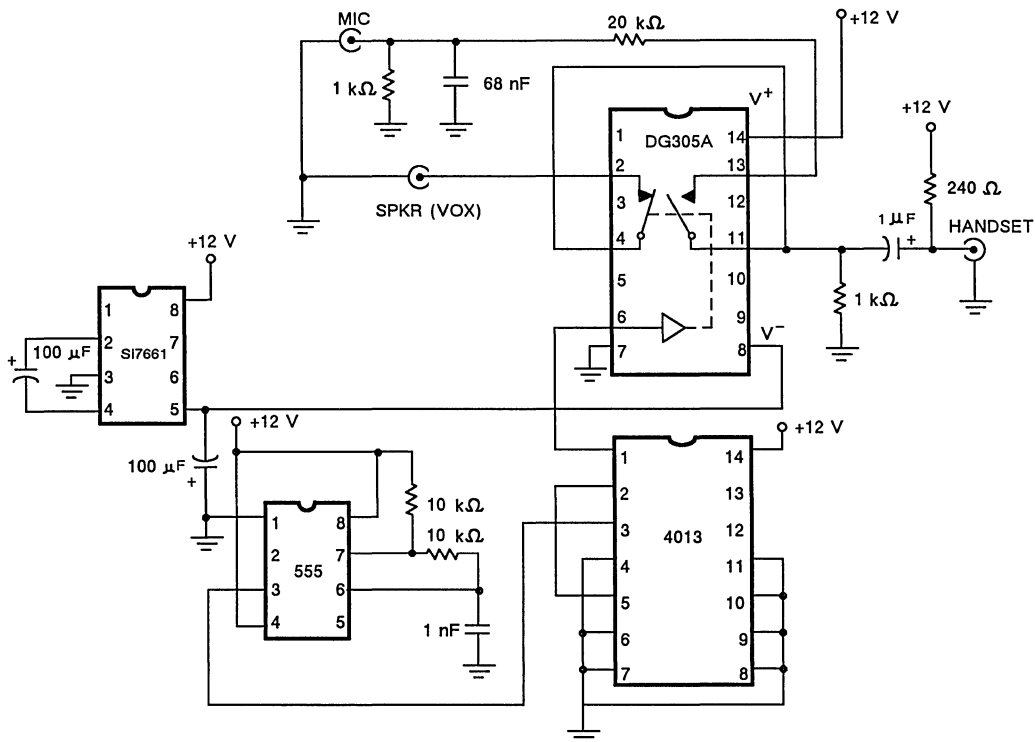


**Figure 20.** Using the Si7661 to Generate the Negative Rail for a 741 Op-amp

**Figure 21.** Output of the 741 Inverting Amplifier at Maximum Undistorted Output



500  $\mu\text{S}/\text{DIV}$ .



**Figure 22.** Using the Si7661 to Supply a Low-current Analog Switch Current

**Analog Switches**

Although in most cases the Si7660 or Si7661 cannot supply sufficient current for analog switch applications, there are some exceptions. For example, Figure 22 gives the schematic diagram of a circuit that was used to interface a Northern Telecom telephone set to an ICOM 2AT2-meter amateur radio transceiver. New designs should use the silicon-gate DG402 SPDT switch.

The analog switch provides isolation for the microphone and speaker connections of the transceiver since the telephone set uses a single path for both transmission and reception. The telephone was operated at 12 V for direct interface to the DG305A, and the supply current from the Si7661 was < 1 mA.

**Microprocessors**

Some of the older standard microprocessors need a negative supply for substrate biasing. The Intel 8080

microprocessor is a good example of this. It is an inexpensive 8-bit CPU that has many different support chips available. To provide the negative supply voltage (-5 V), a basic inverter circuit (such as in Figure 8) using an Si7660 is connected to pin 11 of the microprocessor. The 8080 negative supply draws a maximum current of 1 mA which will not pull down the supply voltage to any great degree.

**Data Conversion**

Data conversion and acquisition products often have the same problem as op amps, in that noisy supply voltages can cause operational problems. However, the problems caused here can have a much greater impact on the operation of an A/D or D/A converter. Since power supply stability can be an important factor in specifying nonlinearity for data conversion products, it is easy to understand that slight fluctuations in supply voltage could be disastrous to a precision measurement system.

The Siliconix Si7135 is a 4-1/2 digit integrating A/D converter that requires a negative supply when operating over a  $\pm$  input voltage range. Figure 23 gives the schematic diagram of a DVM circuit using the Si7661 to supply the negative voltage for the Si7135.

## Regulator Circuits

This section discusses some of the possible methods for using the Si7660 or Si7661 in constant-voltage output circuits over a given output current range. For low current inverter applications, the circuit shown in Figure 24 can be used. The output impedance of the circuit can be as low as 5  $\Omega$  with regulation up to approximately 20 mA. Note that if converters are par-

alleled on the output of this circuit, they should be synchronized to minimize output voltage fluctuations and output noise.

Another regulator application uses the Si7660 or Si7661 in a positive voltage regulator. Conventional three terminal voltage regulators have a voltage drop of greater than 1 volt between the input and output when operating with fairly heavy load currents. The circuit given in Figure 25 uses an Si7660 or Si7661 voltage converter to double the voltage which is then regulated by the op-amp and FET. This configuration allows regulation without the voltage drop as long as the input voltage does not drop below the Zener voltage plus the product of  $I_D$  times  $r_{DS(ON)}$ .

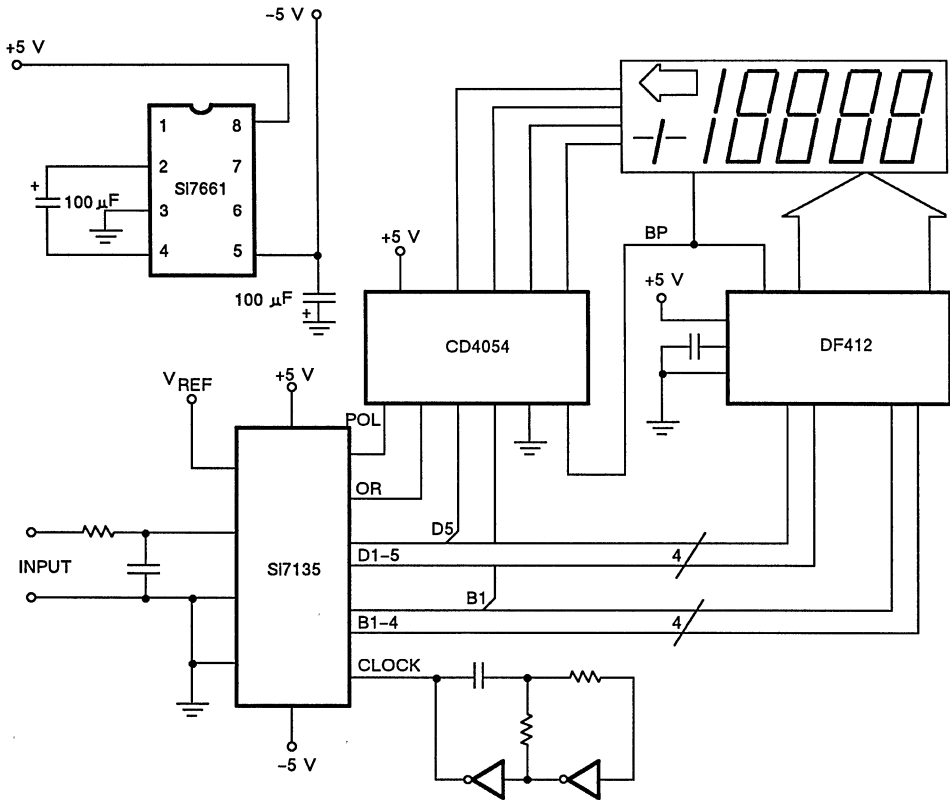


Figure 23. Si7661 Used In a DVM Circuit



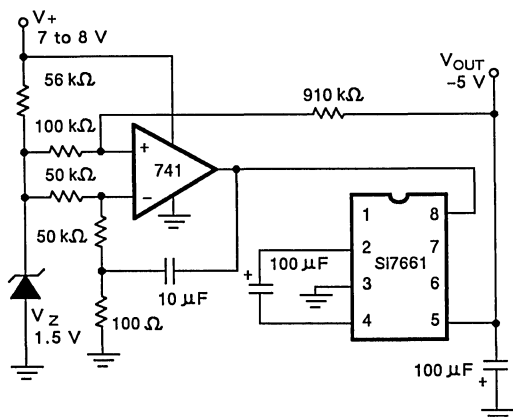
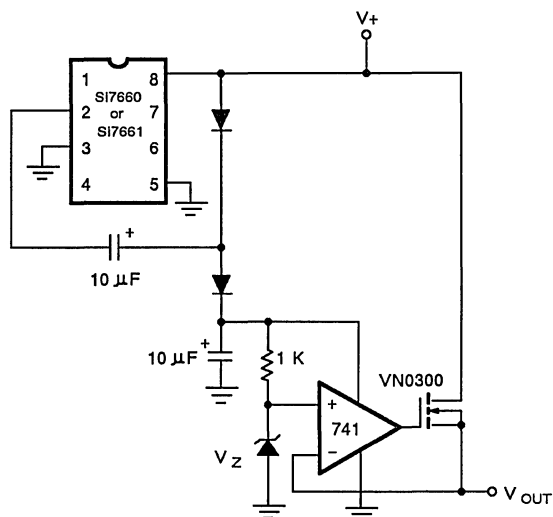


Figure 24. Low Current Inverting Regulator Circuit

Therefore, as long as the input voltage does not drop below 5.26 V, the input is guaranteed to be regulated as close to the zener voltage as can be attained by the common mode offset voltage of the op-amp. By selecting the correct zener diode, this circuit can supply more than 100 mA and can be adjusted for varying voltage outputs up to the input voltage limit of the voltage converter.

## CONCLUSION

The Si7660 and Si7661 can be inexpensive alternatives to full negative supplies in many different low cost applications. Although they are designed for generation of negative voltages, many different voltage levels can be generated with a few additional parts. The Si7660 and Si7661 are pin compatible to competitive products and function as well or better than the competition in every operating specification. The examples given here are only a few of the many possible applications that could utilize the benefits of reduced board space and cost that the Si7660 and Si7661 provide.



For  $I_D = 50 \text{ mA}$ :

$$V_{IN} > V_Z + (I_D \times r_{DS(ON)})$$

$$V_{IN} > 5.2 \text{ V} + (50 \text{ mA} \times 1.2 \Omega)$$

$$V_{IN} > 5.26 \text{ V}$$

Figure 25. Schematic Diagram of the Positive Regulator Circuit

## A SIMPLE APPROACH TO Si7135/8085 INTERFACING

By Doyle L. Slack  
December 1983

### INTRODUCTION

Many A/D conversion designs in use today are both complex and confusing, and for these reasons they are often overlooked for use in more simple applications. Up to now, many Analog-to-Digital (A/D) converter chips have not been microprocessor compatible; the interfacing schemes to make them so have been unnecessarily complicated. But now a simple, straightforward A/D converter can be constructed using only the Siliconix Si7135 and one other IC. It can be easily interfaced to most machine level or high level language computer systems using I/O ports. This system would be ideal for remote/field monitoring or storage of slowly changing conditions with minimum maintenance requirements.

### CIRCUIT COMPONENTS

The Siliconix Si7135 IC is a 4 1/2 digit integrating A/D converter intended for use as a digital volt meter (DVM) chip. Using the dual slope method of conversion, it can achieve an accuracy of  $\pm 1$  count in 20,000. Some of the other features are overrange, underrange, and polarity indications, allowing autoranging and a measurement range of  $-1.9999$  volts to  $+1.9999$  volts. At the optimum clock rate of 120 kHz, approximately 3 conversions per second are possible. Figure 1 gives the pin diagram of the Si7135.

The other half of the A/D system is the Intel 8085 microprocessor -- an inexpensive 8-bit general purpose Central Processing Unit (CPU) that can be operated with a minimum of peripheral devices. With its internal clock circuitry, the only external devices needed to make a working system are address demultiplexing, I/O ports, and memory. The latter two are supplied by the Intel 8155 RAM-I/O and 8755 EPROM-I/O chips. By connecting the data and control lines of the Si7135 A/D system to the I/O lines of the microprocessor system, the data can be read and processed in whatever way the user chooses via software.

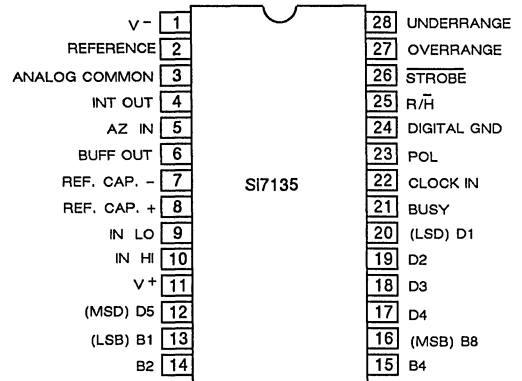


Figure 1. Pin Diagram of the Si7135  
4 1/2 Digit A/D Converter

### CIRCUIT DESCRIPTION

Figure 2 shows the schematic diagram of the Si7135 A/D converter circuit connections to an Intel 8085 microprocessor system. The Si7135 outputs are straightforward in their functions. The OVERRANGE output goes to a logic 1 when an overrange condition (down count exceeds 20,000) has occurred on the previous measurement. The UNDERRANGE output goes to a logic 1 when the input measurement is less than 10% of full scale. The POLARITY output goes high for positive readings and goes low for negative signals. RUN/HOLD is the only control signal from the microprocessor and can be used to stop the measurement cycle of the Si7135 and hold the last reading for as long as the line is held low. The other direct outputs from the Si7135 are the data lines which provide the data in BCD format for each of the 5 digits. The tricky part of the interface is the digit strobe decoding circuitry between the A/D converter and the microprocessor.

Figure 3 gives a simplified timing diagram of the A/D system. When the Si7135 BUSY line (PA7) goes high, either the data from the last reading is valid or the OVERRANGE line (PB0) is high. If an overrange is indicated, the microprocessor displays OL and waits for the next reading. If the data is valid, each of the

digit drive signals from the Si7135 goes high one at a time, sequencing from D5 to D1 repeatedly. The 4532 priority encoder condenses the 5 digit drive signals into 3 bits (PA4-PA6) which are combined with BUSY to make up the upper nibble of the input data. The BCD data lines (PA0-PA3) make up the lower nibble, and the BCD data presented corresponds to the digit drive that is high at the time. This byte, con-

taining both status and data information is decoded, and the port is read again to verify the data for the particular digit being input. After the entire voltage reading has been input, the POLARITY line (PB1) is checked, and the reading and polarity are displayed by the microprocessor. The system then waits for the next conversion. For more details on how the microprocessor handles the data, see SOFTWARE.

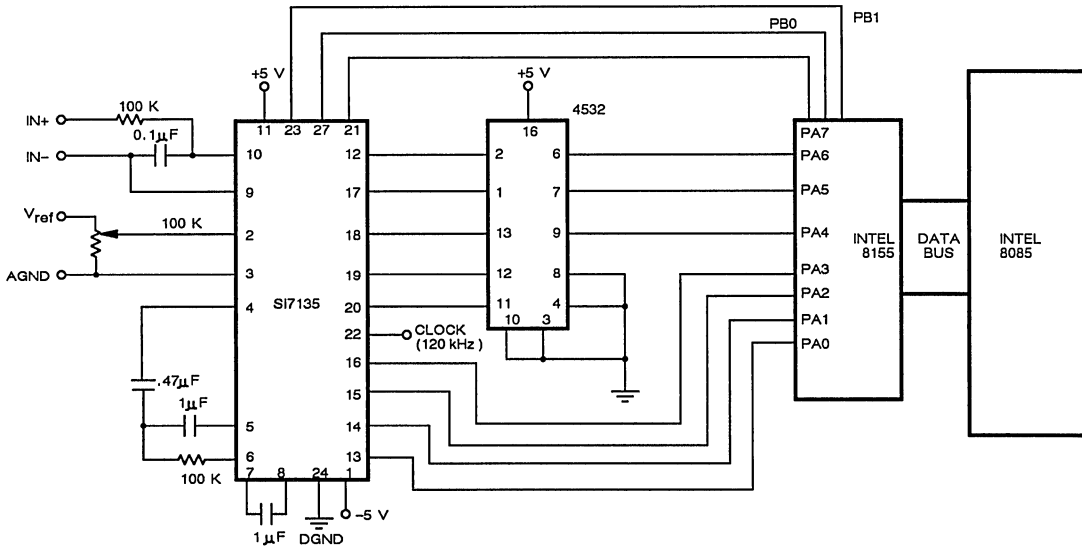


Figure 2. Schematic Diagram of the SI7135 to 8085 System Interface

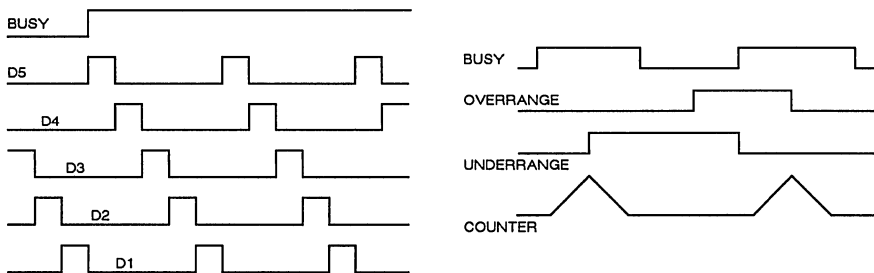


Figure 3. Timing Diagram of the SI7135 A/D Conversion System

## MULTIPLEXING SI7135 SYSTEMS

It would be desirable to be able to monitor more than one analog signal at a time, since often several different events or conditions of interest occur simultaneously. Since the conversion time of integrating converters is relatively slow, the outputs of several A/D converters can be multiplexed without the loss of time that multiplexing the inputs of a single A/D converter entails. The Si7135 system lends itself to this type of use very easily without typing up a large number of additional I/O lines. By multiplexing the outputs of each of the A/D converters, many inputs can be monitored with little additional hardware.

Figure 4(a) shows how the A/D converter systems can be multiplexed quite simply by using tri-state buffers. The RUN/HOLD line of the desired converter is pulled low when a reading is needed from that particular A/D system. The buffers for that system are then enabled, and the data from the Si7135 is read in the same manner as before. The RUN/HOLD line is then sent high, and the other converters are read sequentially in the same way. This method uses only two extra I/O lines and two 4503 buffer chips for each additional A/D converter added to the system. Figure 4(b) shows a detailed schematic of 1/3 of the multiplexed system. Each section that is added to the system is wired identically and connected to the I/O bus.

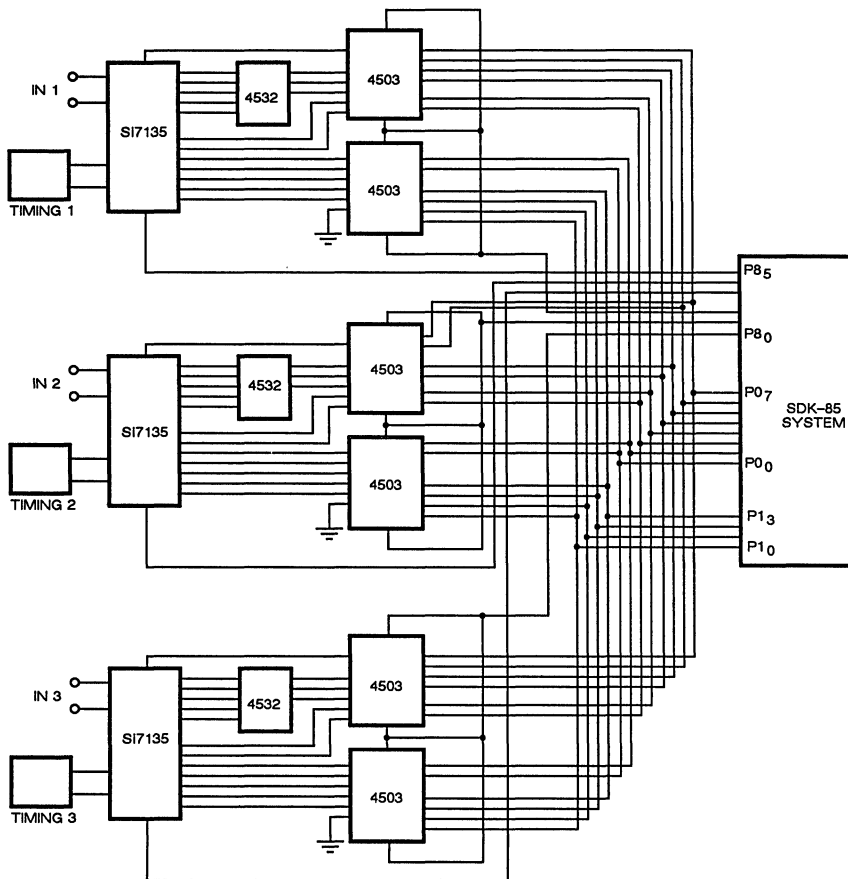


Figure 4(a). Schematic Diagram of the Multiplexed Si7135 A/D Converter System

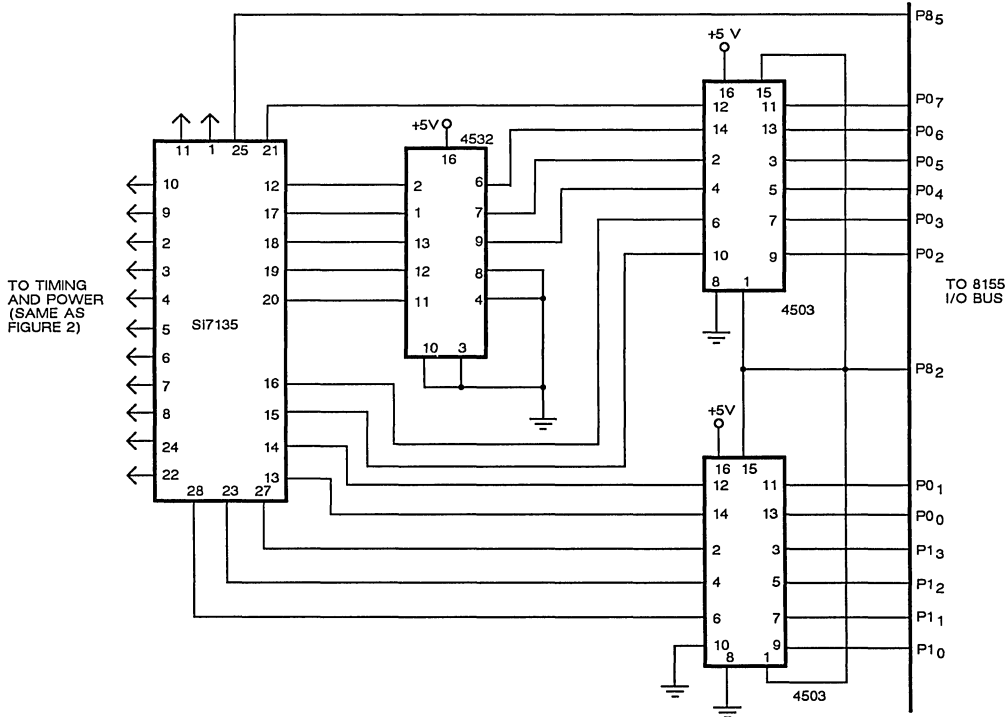


Figure 4(b). Schematic Diagram of 1/3 of the Multiplexed A/D System Shown in Figure 4(a), Including Pin Diagrams of the Components

## SOFTWARE

The software used to read the data from the Si7135 system is shown in Table 1 along with comments on what each command does. This software was written for the Intel SDK85 monitor. The UPDAD and UPDDT subroutines display the data by writing to the 8279 display controller. The OUTPT subroutine outputs the data stored at the location pointed to by the H and L registers. Only minor changes or additions to the software shown here would be required to store large amounts of readings or read several different inputs simultaneously. Also, this program does not utilize the RUN/HOLD or UNDERRANGE lines.

This program was written to run by itself on the Intel

SDK85 system. However, if the A/D converter routine is to be used as a subroutine of another program, the starting address of the subroutine should be changed to 2003H, or NO-OPs (00) should be placed in locations 2000-2002H to eliminate unintentional resetting of the stack pointer. Also, RET (C9) should replace the JUMP instructions at address locations 2037H and 207FH. The instructions at locations 202EH through 2037H should be deleted.

If multiple A/D units are to be connected to the microprocessor, a routine like the one shown in Table 2 would work well. The program shown in Figure 5 has been modified and named READ for this example, and ports 0, 1, and 8 of the SDK85 system are used for the data transfer.

TABLE 1

Program for reading in and displaying the data from the Si7135 A/D converter system.

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
2000	LXI SP, 20C2H	31 C2 20	Load stack pointer
2003	MVI A, 00H	3E 00	Set up data direction register for I/O ports
2005	OUT 02	D3 02	
2007	MVI A, 08H	3E 08	
2009	OUT 03	D3 03	
200B	IN 00	DB 00	Check for BUSY, if not, wait
200D	ANI 80H	E6 80	
200F	SUI 80H	D6 80	
2011	JNZ 200BH	C2 0B 20	
2014	IN 01	DB 01	Check for OVERRANGE. If not, continue with reading
2016	RRC	0F	
2017	JNC 203AH	D2 3A 20	
201A	MVI A, 01H	3E 01	Output OL to display
201C	MVI B, 00H	06 00	
201E	LXI H, 2082H	21 82 20	
2021	CALL OUTPT	CD B7 02	
2024	MVI A, 00H	3E 00	
2026	MVI B, 00H	06 00	
2028	LXI H, 2084H	21 84 20	
202B	CALL OUTPT	CD B7 02	
202E	IN 00	DB 00	Wait for next measurement cycle
2030	ANI 80H	E6 80	
2032	SUI 80H	D6 80	
2034	JZ 202EH	CA 2E 20	
2037	JMP 200BH	C3 0B 20	Return
203A	MVI B, 0D0H	06 D0	Set pointer to value of first strobe
203C	CALL DIGIT	CD A0 20	Get first digit and put it in the proper register
203F	MOV D, A	57	
2040	MVI B, 0C0H	06 C0	Set pointer to value of second strobe
2042	CALL DIGIT	CD A0 20	Get second digit and put it in the proper register
2045	RLC	07	
2046	RLC	07	
2047	RLC	07	
2048	RLC	07	
2049	MOV E, A	5F	
204A	MVI B, 0B0H	06 B0	Set pointer to value of third strobe
204C	CALL DIGIT	CD A0 20	Get third digit and put it with the second digit
204F	ADD E	83	
2050	MOV E, A	5F	
2051	MVI B, 0A0H	06 A0	Set pointer to value of fourth strobe
2053	CALL DIGIT	CD A0 20	Get fourth digit and put it in the proper register
2056	RLC	07	
2057	RLC	07	
2058	RLC	07	
2059	RLC	07	
205A	MOV C, A	4F	
205B	MVI B, 90H	06 90	Set pointer to value of fifth strobe
205D	CALL DIGIT	CD A0 20	Get fifth digit and put it with the fourth digit
2060	ADD C	81	
2061	PUSH PSW	F5	Save the lowest two digits
2062	CALL UPDAD	CD 63 03	Display the upper three digits
2065	POP PSW	F1	Restore the lowest two digits
2066	CALL UPDDT	CD 6E 03	Display the lowest two digits

## TABLE 1 (Cont'd)

ADDRESS	MNEMONIC	OP-CODE	COMMENTS	
2069	IN 01	DB 01	Check polarity bit for positive or negative sign	
206B	ANI 02H	E6 02		
206D	SUI 02H	D6 02	Blank the polarity position	
206F	JNZ 207AH	C2 7A 20		
2072	MVI A, 0FFH	3E FF	Return	
2074	STA 1800H	32 00 18		
2077	JMP 202EH	C3 2E 20	Put a minus sign in the polarity position	
207A	MVI A, 0FBH	3E FB		
207C	STA 1800H	32 00 18	Return	
207F	JMP 202EH	C3 2E 20		
2082	data	00		
2083	data	11		
2084	data	15		
2085	data	15		
2086	data	15		
2087	data	15		
<b>Subroutine DIGIT</b>				
20A0	IN 00	DB 00		Read port
20A2	ANI OF0H	E6 F0	Mask lower byte of data	
20A4	SUB B	90	Compare byte to pointer, if not equal then wait	
20A5	JNZ 20A0H	C2 A0 20	Read port	
20A8	IN 00	DB 00		
20AA	ANI OFH	E6 0F	Mask upper byte of data	
20AC	RET	C9	Return	

## TABLE 2

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
2080	LXI SP, 20C2H	31 C2 20	Load stack
2083	MVI A, 0FFH	3E FF	Set up data direction register for I/O ports
2085	OUT 0A	D3 0A	
2087	OUT 08	D3 08	Hold present A/D Converter
2089	MVI A, 00H	3E 00	
208B	OUT 02	D3 02	Set pointer to next A/D Converter
208D	OUT 03	D3 03	
208F	MVI A, 0DFH	3E DF	Save pointer data
2091	MVI B, 0DBH	06 DB	
2093	OUT 08	DB 08	Delay for 1/3 second
2095	RRC	0F	
2096	PUSH PSW	F5	Enable Buffers
2097	LXI D, A700H	11 00 A7	
209A	CALL DELAY	CD F1 05	Set Enable to next A/D Converter
209D	MOV A, B	78	
209E	OUT 08	D3 08	Save Enable Data
20A0	RRC	0F	
20A1	MOV B, A	47	Read Data from A/D Converter
20A2	PUSH B	C5	
20A3	CALL READ	CD 00 20	Restore Enable Data
20A6	POP B	C1	
20A7	RLC	07	Check if all A/D Converters have been read
20A8	RRC	0F	
20A9	JC 20B0H	DA B0 20	Restore Pointer Data
20AC	POP PSW	F1	
20AD	JMP 208FH	C3 8F 20	Return
20B0	POP PSW	F1	Clear the Stack
20B1	JMP 2093H	C3 93 20	Start Over

TABLE 2 (Cont'd)

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
<b>Subroutine READ</b>			
2000	IN 01	DB 01	Check for OVERRANGE. If not, continue with reading
2002	RRC	0	
2003	JNC 201AH	D2 1A 20	
2006	MVI A, 01H	3E 01	Output OL to display
2008	MVI B, 00H	06 00	
200A	LXI H, 2062H	21 62 20	
200D	CALL OUTPT	CD B7 02	
2010	MVI A, 00H	3E 00	
2012	MVI B, 00H	06 00	
2014	LXI H, 2064H	21 64 20	
2017	CALL OUTPT	CD B7 02	
201A	MVI B, 0D0H	06 D0	Set pointer to value of first strobe
201C	CALL DIGIT	CD 70 20	Get first digit and put it in the proper register
201F	MOV D, A	57	
2020	MVI B, 0C0H	06 C0	Set pointer to value of second strobe
2022	CALL DIGIT	CD 70 20	Get second digit and put it in the proper register
2025	RLC	07	
2026	RLC	07	
2027	RLC	07	
2028	RLC	07	
2029	MOV E, A	5F	
202A	MVI B, 0B0H	06 B0	Set pointer to value to third strobe
202C	CALL DIGIT	CD 70 20	Get thrd digit and put it with second digit
202F	ADD E	83	
2030	MOV E, A	5F	
2031	MVI B, 0A0H	06 A0	Set pointer to value of fourth strobe
2033	CALL DIGIT	CD 70 20	Get fourth digit and put It in the proper register
2036	RLC	07	
2037	RLC	07	
2038	RLC	07	
2039	RLC	07	
203A	MOV C, A	4F	
203B	MVI B, 90H	06 90	Set pointer to value of fifth strobe
203D	CALL DIGIT	CD 70 20	Get fifth digit and put it with the fourth digit
2040	ADD C	81	
2041	PUSH PSW	F5	Save the lowest two digits
2042	CALL UPDAD	CD 63 03	Display the upper three digits
2045	POP PSW	F1	Restore the lowest two digits
2046	CALL UPDDT	CD 6E 03	Display the lowest two digits
2049	IN 01	DB 01	Check polarity bit for positive or negative sign
204B	ANI 02H	E6 02	
204D	SUI 02H	D6 02	
204F	JNZ 205AH	C2 5A 20	
2052	MVI A, 0FFH	3E FF	Blank the polarity position
2054	STA 1800H	32 00 18	
2057	RET	C9	Return
2058	MVI A, 0FBH	3E FB	Put a minus sign in the polarity position
205C	STA 1800H	32 00 18	
205F	RET	C9	Return
2062	data	00	
2063	data	11	
2064	data	15	
2065	data	15	
2066	data	15	
2067	data	15	



## TABLE 2 (Cont'd)

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
<b>Subroutine DIGIT</b>			
2070	IN 00	DB 00	Read port
2072	ANI 0F0H	E6 F0	Mask lower byte of data
2074	SUB B	90	Compare byte to pointer, if not equal then wait
2075	JNZ 2070H	C2 70 20	
2078	IN 00	DB 00	Read port
207A	ANI 0FH	E6 0F	Mask upper byte of data
207C	RET	C9	Return

### CONCLUSION

The Siliconix Si7135 is an inexpensive, simple integrated circuit that can solve the problems associated with a design that seems far too complex for the job it is intended to do. Note that the Intel 8085 is not the only microprocessor one could interface to the Si7135. This scheme is easily adaptable to other mi-

croprocessor architectures. However it is also important to know that the comparatively slow conversion time makes multiplexing of several Si7135's to one microprocessor more practical than multiplexing the inputs to a single Si7135. With multiplexed converters, a fast, easy method of data acquisition can be achieved for a reasonable price.

# Si8601 DATA ACQUISITION SYSTEM INTERFACES FOR I/O OR MEMORY MAPPED OPERATION

By Doyle L. Slack  
Revised January, 1988

## INTRODUCTION

The Siliconix Si8601 is an 8 channel, 8-bit silicon gate CMOS Data Acquisition System containing an 8 channel multiplexer, an 8-bit A/D converter, and an output latching circuit. The A/D converter uses a binary-weighted capacitor successive approximation technique allowing fast conversion time and a true sample and hold function with low power consumption. The 8 channel multiplexer offers great flexibility by providing multi-channel data collection with only one A/D converter. However, the outstanding advantage of this device is its ease of interfacing to microprocessor systems. Both the address inputs and data outputs are latching which minimizes the time that the microprocessor and the data acquisition system must dedicate to data transfer. The outputs are tri-state, allowing direct connection to the system data bus for memory mapping. Since the Si8601 is easily wired for either I/O or memory mapped operation,

interfacing hardware and associated software for both schemes are presented here.

The Si8601 can be easily interfaced to the Intel 8085, an inexpensive 8-bit microprocessor with many available peripheral devices. The 8085 was chosen for interfacing because it makes a good example for wiring to any one of the several other similar microprocessor architectures.

The Intel 8155 RAM-I/O and 8755 EPROM-I/O chips provide both memory and I/O ports for the 8085 system and can be used to interface the Si8601 and the 8085. If the A/D converter output of the Si8601 is to be monitored at an I/O port, it can be left running constantly. The port can be sampled whenever a reading is desired. On the other hand, the memory mapped data acquisition system costs less to build because there is no need for an I/O port.

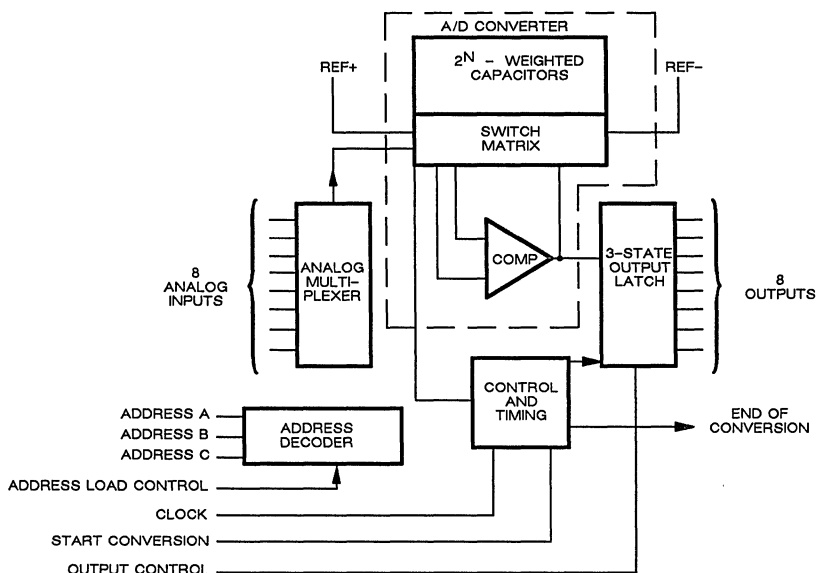


Figure 1. Block Diagram of the Si8601 Data Conversion System

## CIRCUIT DESCRIPTION

Figure 1 shows a block diagram of the Si8601. Address inputs A<sub>0</sub>, A<sub>1</sub>, and A<sub>2</sub> allow selection of the 8 channels of the multiplexer. Since the multiplexer works asynchronously with respect to the A/D converter section, care must be exercised not to change input channels during the first 9 clock cycles (sampling phase) after the SC (start conversion) pulse. Each channel has a single-ended input which has an analog range from -REF to +REF, giving a conversion range from 3 to 6.5 V. Note that only a 5 V V<sub>CC</sub> and +REF will allow TTL compatibility. The -REF input allows separation of analog and digital grounds which helps to keep noise spikes that might be present on the digital system ground from affecting the accuracy of the analog input to the Si8601. The eight tri-state data outputs provide the data to the microprocessor. A square wave signal is needed for the CLOCK input. Maximum clock frequencies of 1.4 MHz are possible. Clock duty cycle can be anywhere from 20 to 80%. The OUTPUT CONTROL (OC), START CONVERSION (START), and ADDRESS LOAD CONTROL (ALC) provide the means for the microprocessor to control the Si8601. The END OF CONVERSION (EOC) output

goes high when the conversion is finished and when the output is available at the data pins. Figure 2(a) shows the pin diagram of the Si8601, and Figure 2(b) gives the relationship of the input and output signals of the data acquisition system.

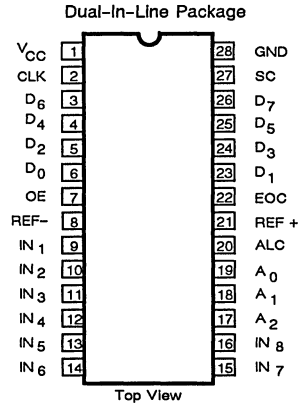


Figure 2(a). Pin Diagram of the Si8601 8-channel Data Acquisition System

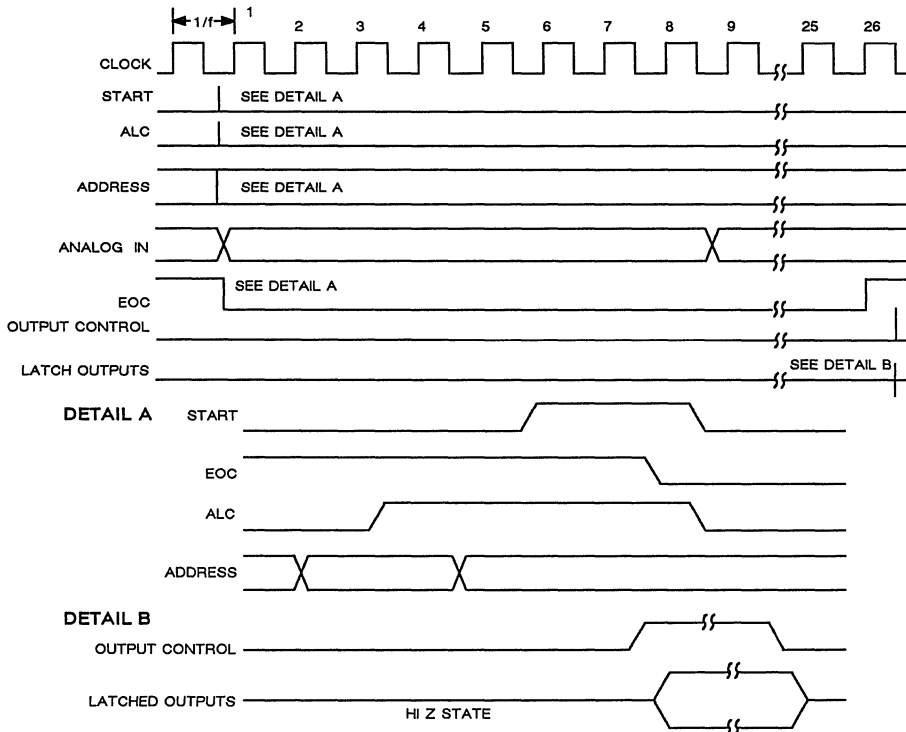


Figure 2(b). Timing Diagram of the Si8601 Data Acquisition System

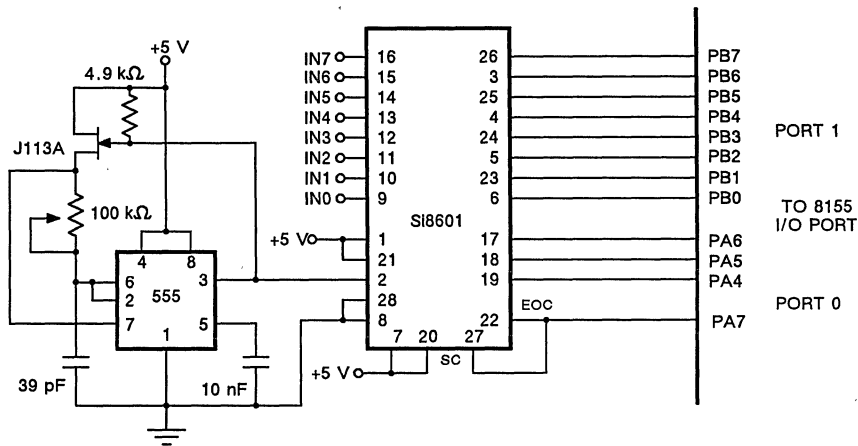


Figure 3. Schematic Diagram of the I/O Version of the Si8601 Interface

## I/O OPERATION

In the I/O mode, the Si8601 is in a free-running loop; the data outputs of the A/D converter are always enabled. The data outputs and address inputs of the data acquisition system are connected to the I/O port, and the START input is tied to the EOC line so that the system is constantly measuring the selected input channel (see Figure 3). The data handling is then accomplished by a machine language program that reads in the converted data and processes it in whatever way desired by the user. The data transfer is verified in the program by checking the EOC pin for data stability before accepting the next input.

## MEMORY MAPPED OPERATION

When operating in the memory mapped mode, the data outputs and address inputs are tied directly to their corresponding busses. The OC, START, and ALC lines are used to tri-state the Si8601 when appropriate. Figure 4 shows the schematic diagram of the memory mapped data acquisition system. Note that A15 is the only address decoding line used for this example. To eliminate memory map redundancy, a more sophisticated address decoding circuit would be needed. The NOR gates of the 4001 combine the address decoding, READ, and WRITE signals to control the data acquisition system. The EOC pin is tied to RST 6.5 of the 8085 to notify the microprocessor when the conversion has been completed and when the data outputs are ready to be read.

## SOFTWARE

The software shown here was written for use with the Intel SDK-85 development system monitor with the 8 channels of the Si8601 memory mapped at 8000H-8007H and I/O mapped through ports 0 and 1. The UPDDT and UPDAD routines are used to display the contents of the A, D, and E registers. Both programs are written in subroutine form so they can be utilized by more than one calling program. If data storage or comparison is desired, minor changes or additions to the software shown here will be necessary. The I/O oriented programs are shown in Tables 1 (a) and 1 (b). Table 1 (a) shows a simple routine that reads in and displays a single channel selected by the data stored at location 20A0H. The program in Table 1 (b) reads each of the channels and displays them for approximately 1/3 second each. Since the I/O system is constantly running, the EOC pin is monitored by the program, and data is only taken if EOC is high (data is valid).

The memory mapped system must be started when a reading is desired. This is done in Tables 2(a) and 2(b) by writing to the desired memory location, which starts the conversion. The EOC line signals an interrupt for the microprocessor, making it jump to the READ subroutine and then returning back to the main program. Table 2(a) uses the H and L registers to point to the desired channel and then displays the reading from that channel. Table 2(b) reads all 8 channels and displays each one for approximately 1/3 second.

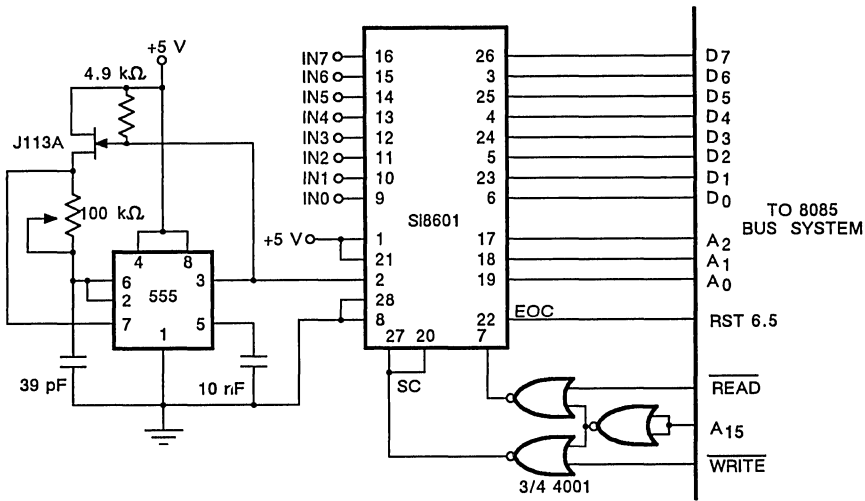


Figure 4. Schematic Diagram of the Memory Mapped Version of the Si8601 Interface

Note the asterisks in tables 1(a) and 2(a). These mark the locations where the desired input channel is selected. Figure 5 gives the locations of the channels in both the I/O and memory mapped configurations.

## CONCLUSION

The Si8601 Data Acquisition System features built-in

multi-channel capability with easy interface to most microprocessor systems. The 8085 is just one example of how this system can be constructed using only an external clock circuit and the Si8601. It has a 25  $\mu$ s conversion time and extremely low power consumption which makes it ideal for battery powered monitoring of multiple parameters or conditions in the field.

INPUT CHANNEL	I/O LOCATION	MEMORY MAPPED LOCATION
0	00	8000H
1	10	8001H
2	20	8002H
3	30	8003H
4	40	8004H
5	50	8005H
6	60	8006H
7	70	8007H

FIGURE 5. Channel locations for the Si8601 in both I/O and memory mapped configurations

TABLE 1 (a)

Program for reading one channel of the Si8601 in the I/O configuration

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
<b>Calling Program</b>			
2000	LXI SP, 20C2H	31 C2 20	Load stack pointer
2003	LXI H, 20A0H	21 A0 20	Reserve location for channel selector
*2006	MVI M, 00H	36 00	Load channel selector with desired input
2008	MVI A, 00H	3E 00	Set up data direction registers for I/O ports
200A	OUT 03	D3 03	
200C	MVI A, 7FH	3E 7F	
200E	OUT 02	D3 02	
2010	CALL READ	CD 16 20	Read the I/O port
2013	JMP 2003H	C3 03 20	Start over
<b>Subroutine READ</b>			
2016	MOV A, M	7E	Start conversion
2017	OUT 00	D3 00	
2019	IN 00	DB 00	Check to see if conversion is finished, if done, read in data
201B	RLC	07	
201C	JNC 2019H	D2 19 20	
201F	IN 01	DB 01	Read in data
2021	CALL UPDDT	CD 6E 03	Display data
2024	RET	C9	Return

TABLE 1 (b)

Program for reading all 8-channels of the Si8601 in the I/O configuration

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
<b>Calling Program</b>			
2000	LXI SP, 20C2H	31 C2 20	Load stack pointer
2003	LXI H, 20A0H	21 A0 20	Reserve location for channel selector
2006	MVI M, 00H	36 00	Load channel selector with desired input
2008	MVI A, 00H	3E 00	Set up data direction registers for I/O ports
200A	OUT 03	D3 03	
200C	MVI A, 7FH	3E 7F	
200E	OUT 02	D3 02	
2010	CALL READ	CD 16 20	Read the I/O port
2013	JMP 2003H	C3 03 20	Start over
<b>Subroutine READ</b>			
2010	MOV A, M	7E	Start conversion
2011	PUSH PSW	F5	
2012	OUT 00	D3 00	Check to see if conversion is finished, if done, read-in data
2014	IN 00	DB 00	
2016	RLC	07	
2017	JNC 2014H	D2 14 20	
201A	IN 01	DB 01	Read-in data
201C	CALL UPDDT	CD 6E 03	Display data
201F	POP PSW	F1	Restore channel selector
2020	SUI 70H	D6 70	Check to see if all channels have been read, if not, keep going
2022	JZ 2029H	CA 29 20	
2025	INR M	34	Increment channel selector
2026	JMP 2010H	C3 10 20	Read next channel
2029	RET	C9	Return

**TABLE 2 (a)**

**Program for reading one channel of the Si8601 in the memory mapped configuration**

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
<b>Subroutine BGNCNVS</b>			
2000	MOV M, A	77	Start conversion
2001	MVI A, 0CH	3E 0C	Enable the interrupt system
2003	SIM	30	
2004	EI	FB	
2005	EXI D, FFFFH	11 FF FF	Delay while conversion takes place
2008	CALL DELAY	CD F1 05	
200B	RET	C9	Return
<b>Subroutine READ</b>			
2010	MOV A, M	7E	Read-in results of the conversion
2011	CALL UPDDT	CD 6E 03	Display the results
2014	RET	C9	Return
<b>Calling Program</b>			
2020	LXI SP, 20C2H	31 C2 20	Load stack pointer
*2023	LXI H, 8000H	21 00 80	Load channel selector
2026	CALL BGNCNVS	CD 00 20	Start conversion
2029	LXI D, FFFFH	11 FF FF	Delay between readings for approximately 1/3 second
202C	CALL DELAY	CD F1 05	
202F	JMP 2023H	C3 23 20	Repeat

**TABLE 2 (b)**

**Program for reading all 8 channels of the Si8601 in the memory mapped configuration**

ADDRESS	MNEMONIC	OP-CODE	COMMENTS
<b>Subroutine BGNCNVS</b>			
2000	MOV M, A	77	Start conversion
2001	MVI A, 0CH	3E 0C	Enable the interrupt system
2003	SIM	30	
2004	EI	FB	
2005	LXI D, FFFFH	11 FF FF	Delay while conversion takes place
2008	CALL DELAY	CD F1 05	
200B	RET	C9	Return
<b>Subroutine READ</b>			
2010	MOV A, M	7E	Read-in results of the conversion
2011	CALL UPDDT	CD 6E 03	Display the results
2014	RET	C9	Return
<b>Calling Program</b>			
2020	LXI SP, 20C2H	31 C2 20	Load Stack pointer
2023	LXI H, 8000H	21 00 80	Load channel selector
2026	PUSH H	E5	Save channel selector
2027	CALL BGNCNVS	CD 00 20	Start conversion
202A	POP H	E1	Restore channel selector
202B	MOV A, L	7D	Check to see if all channels have been read, if they have, start over
202C	SUI 07H	D6 07	
202E	JZ 2023H	CA 23 20	
2031	INR L	2C	Increment channel selector
2032	JMP 2026H	C3 26 20	Go to next channel for a reading

\* = Location where desired input channel is selected.

## A HIGH QUALITY AUDIO CROSSPOINT SWITCH

By Bob Zavrel  
Revised January 1988

### INTRODUCTION

Recent advances in analog switch integrated circuits have made superior audio switch specifications possible. A crosspoint switch for the most demanding audio applications is described here. Although this switch may be used in recording studio and radio broadcast mixers where little compromise is acceptable, the low cost and small size makes this switch ideal for a much more diverse range of applications. Such applications can include audio crosspoint switches found in video systems, audio synthesizers, high quality multiplexers, and home entertainment systems.

A high quality audio frequency switch should have the following features:

1. Reasonable cost
2. Unity or variable gain
3. Very low harmonic distortion ( $< 0.01\%$ )
4. Flat response (DC to  $> 1$  MHz)
5. Low crosstalk
6. High OFF Isolation
7. Excellent phase linearity

8. High speed switching
9. Freedom from switch "popping"
10. Small size
11. Use of DC coupling only

The size of a complex audio switching array can be greatly reduced by using IC analog switches. The prototype array is an 8x2 stereo crosspoint switch mounted on a 4x7 inch board. Other switch configurations may be fabricated with little effect on the switch characteristics. This single board can replace a score of rotary switches and the bundles of audio cable often found in audio mixers. Furthermore, ground loop problems are reduced by eliminating the cable bundles.

Siliconix SD5002s were chosen because of low ON resistance, low switch capacitance, and very fast switching times. The LF347 quad op amp was chosen for its excellent audio characteristics in a quad package. Two LF347s are used in this switch providing a summing and output amplifier for each of four channels. Since the SD5002s switch into virtual grounds, they are held "normally open" by applying

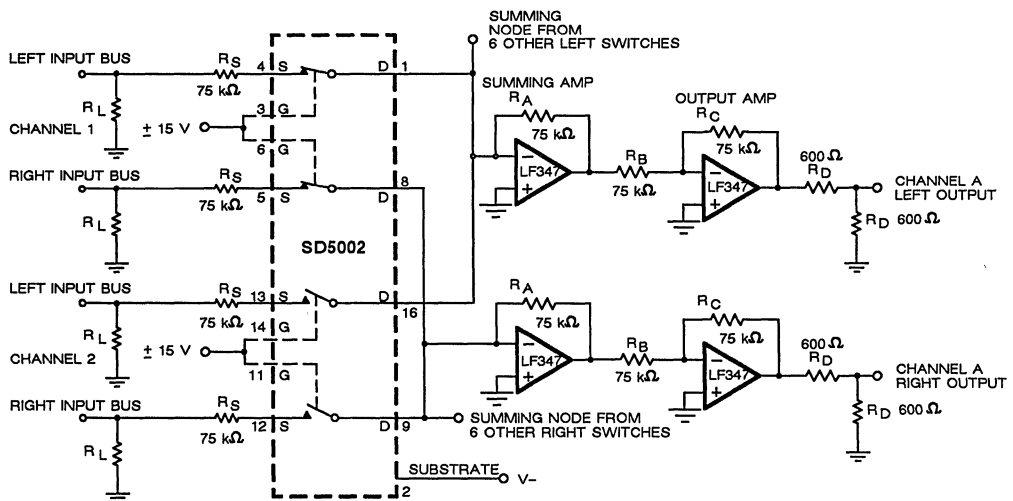


Figure 1



-15 V the switch gates. To turn them on it is sufficient to apply a  $V+$  level to the gates. For any switch configuration, the appropriate switch(es) are closed by biasing the appropriate gate(s) to the positive voltage supply. In this circuit pairs of switches are controlled together to affect the left and right channels of a stereo input simultaneously. This is accomplished simply by tying the applicable switch gates together and using a common bias.

Figure 1 shows how a single SD5002 is configured as a 2x1 stereo switch. Figure 2 shows how the circuit can be expanded into a switch matrix. Eight SD5002s are required to construct the 8x2 stereo matrix array. One  $R_L$  is required for each channel input for termination while four  $R_S$ 's are employed to feed the signal from the switches to the amplifiers. Input buses are consequently formed in front of these resistors.

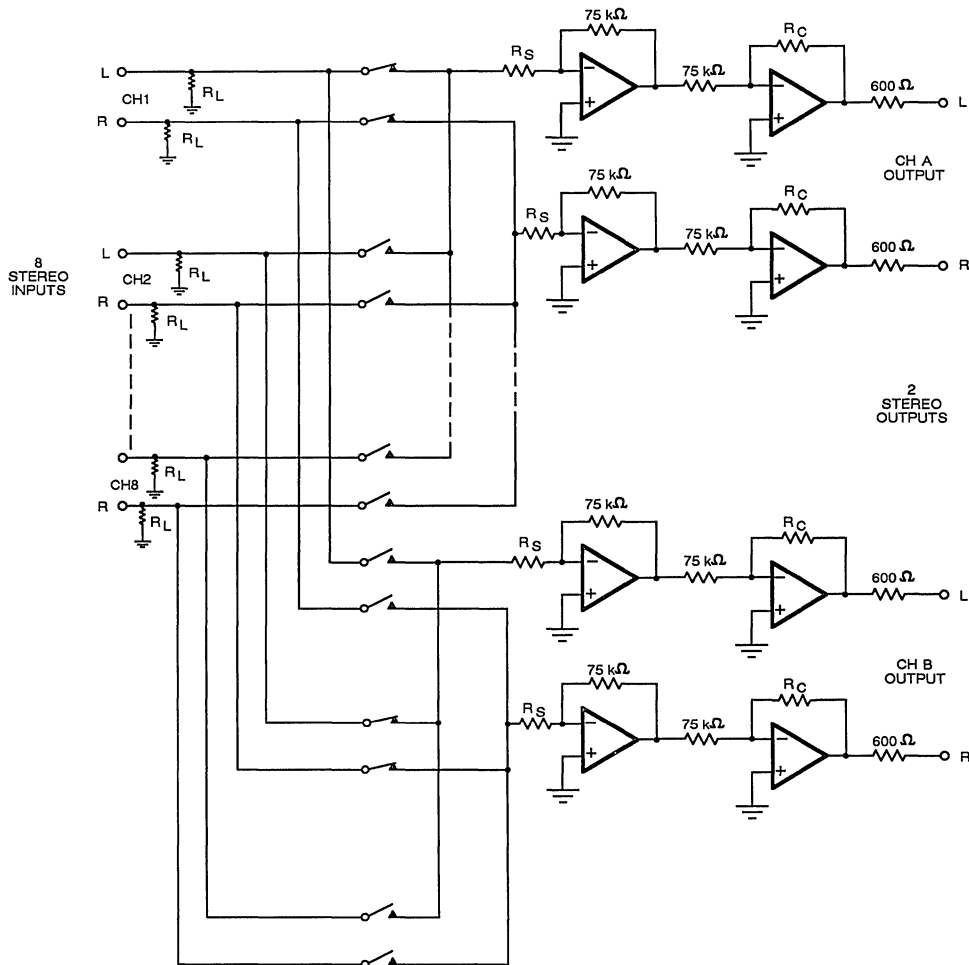


Figure 2. A High Quality 8x2 Stereo Crosspoint Switch

The SD5002 drains are connected to these input buses. A larger array will cause reduced system performance due to longer lead lengths and increased circuit capacitance. Nevertheless, large matrices can be configured with little performance compromise because of the low initial switch capacitance.  $R_L$ 's value should reflect the value of the source impedance. Deletion of  $R_L$  will seriously degrade crosstalk and off isolation performance while lower values of  $R_L$  will improve these specifications.  $R_C$  may be adjusted for a wide range of system gain while a value of about 150 k $\Omega$  will set the circuit to unity gain.  $R_D$  sets the value of the output impedance and if the switch is to feed a high impedance load,  $R_O$  should be included to maintain system performance.

Electrolytic and mica capacitors are used on the cir-

cuit board for bypassing the two power supply voltages. Supply voltage bypassing will reduce both high and low frequency noise and help stabilize the system. The entire circuit should be well shielded particularly if it will be exposed to strong rf or power line fields. Conductors carrying high current should be kept away from the circuit. Double sided PC board should be used creating a ground plane on the component side as an additional precautionary measure.

Table 1 shows the switch performance of the 8x2 crosspoint configuration.  $R_L$  was set to 10 k  $\Omega$ , reflecting the high impedance of the test oscillator's output. Regulated power supply voltages of plus and minus 9 to 15 volts may be used. The signal voltages should be kept under about 3.5  $V_{p-p}$  to maintain switch performance.

TABLE 1

Frequency (Hz)	Crosstalk (dB)	"Off" Isolation (dB)	THD
50	-74	-75	0.006
100	-74	-75	0.005
200	-74	-75	0.004
500	-74	-75	0.003
1	-74	-75	0.003
2	-73	-74	0.003
5	-70	-71	0.003
10	-67	-68	0.004
20	-62	-62	0.006
50	-55	-55	0.020
100	-50	-49	0.045

Signal voltages: 3  $V_{p-p}$

Supply voltages:  $\pm 12$  volts

# A SYSTEM SOLUTION TO HP-IL EQUIPMENT INTERFACE

Robert J. Zavrel Jr.  
December 1983

## INTRODUCTION

Siliconix manufactures several high performance components which lend themselves nicely to portable equipment. For a 4-1/2 digit HP-IL compatible DVM, Siliconix now offers a "systems solution" to the designer of such a device. With the exception of a few standard 4000 series CMOS ICs, all the special integrated circuits are offered by Siliconix. The DVM is based on the Si7135, a high-quality, single chip, dual-slope integrating A/D converter. The prototype circuit used to interface the Si7135 to the HP-IL contained 23 standard 4000 series CMOS ICs. This hardware interface solution may be simplified to a custom 28 pin DIP Interface IC "gate array". This interface allows direct connection to the Hewlett-Packard HP-IL standard "GPIO". Additionally, Siliconix offers three devices which complete the specialized DVM IC requirement. The DF412 provides a local LCD driver which allows the DVM to operate as a stand-alone device. Two SD5002 analog switches are arranged to provide an analog input multiplexer which boasts over 100 dB channel-to-channel isolation. Finally, an Si7661 voltage converter eliminates the need for a negative power supply, thus a single 5 V supply is all that is necessary.

The HP-IL "interface loop" is a data communication system designed as a portable, low cost, and high quality instrument controller. It is quite suitable for lab environments where easy programming is desirable. The powerful and popular HP-41 handheld computer or the HP-75C portable computer can be used as controllers for up to 31 "HP-IL devices" in the loop. Hewlett-Packard manufactures a wide variety of HP-IL compatible devices including a printer, timer, video interface, and DVM (Reference 1). For convenience the HP-41 will be used as the controller in this paper. A detailed description of HP-IL is beyond the scope of the paper, but a basic understanding of HP-IL is necessary to render this interface technique meaningful.

## HP-IL INTERFACE CIRCUIT/INTERFACE IC HANDSHAKING

Care must be taken to avoid confusion of terms. The HP-IL interface circuit contains two basic ICs. It is this circuit which takes the serial IL pulses and routes the data to the two-way data bus, the appropriate handshake and other control pins. Taken together this assemblage of data and control pins is called "GPIO" or "general purpose input/output". Hewlett-Packard offers four approaches to realizing the HP-IL interface circuit. Details of these approaches are available from Hewlett-Packard. The "Interface IC" interfaces the Si7135 digital outputs to the GPIO bus. (Figure 1)

Contained within the HP-IL interface circuit are the 28 pin DIP ILB3-0003 from Hewlett-Packard and the Mostek 1820-2810 40 pin single chip microcomputer. The ILB3-0003 contains multiple registers and extensive circuitry for the HP-IL interface. The microcomputer acts as an HP-IL device controller and provides the GPIO data and control pins, later to be discussed in detail. This Mostek microcomputer is made with a special mask for HP-IL and must be purchased from Hewlett-Packard. These ICs are arranged around two 8-bit data busses labeled as DA and DB. In the DVM and multiplexer circuits, the DB bus is used only for data transfers between the 1820-2810 and the ILB3-0003. The DA is used as the bi-directional bus between the 1820-2810 and the DVM. Because ASCII characters are seven-bit words, the eighth bit of the eight-bit bus should be held low when ASCII is being transmitted. The circuits described here link the GPIO standard interface to the specialized data and control pins of the Si7135 4-1/2 digit DVM chip and a multiplexer. The multiplexer circuit is also relatively simple, needing only a few standard CMOS ICs.

ASCII characters are used for all data transfer in HP-IL. Data transfer can flow to an external device such as a printer or from an external device such as a DVM. Two device modes are consequently defined

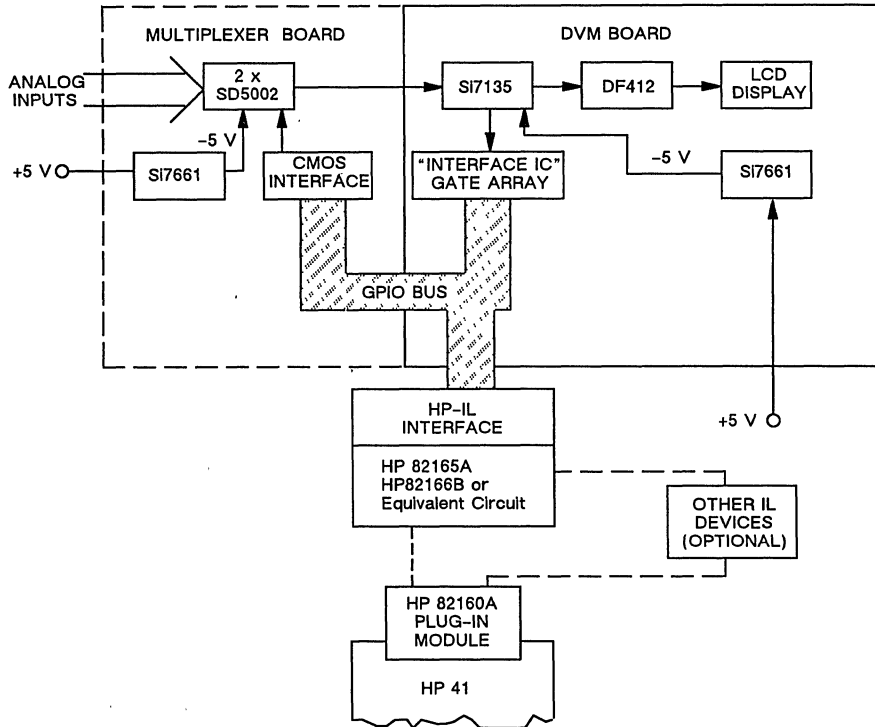


Figure 1. HP-IL Multiplexer/DVM System

as listener and talker. Data transfer between an HP-IL station and its corresponding peripheral device can utilize six "handshake" and additional command pins located on GPIO. Three handshake pins are used for the listener mode, and three are used for the talker mode. The two handshake modes are very similar. When listener is ready to accept data, a "Ready" pin is taken low (logic true). The talker may respond at this point if it has data to send with an ASCII character on the data bus and a low "Data Valid" pin. Finally, if the listener receives the data, it sets the "Data Confirmed" pin low, completing the handshake sequence.

Several levels of handshaking are possible using the three handshake pins in different combinations. For the Siliconix DVM, the talker handshaking is very simple. "Data confirmed" is not used, and the "Ready"

and "Data Valid" pins are hardwired together. "Ready" and "Data Valid" correspond to the RDYO and DAVI pins for the talker handshake. In addition, the GETO pin is used to initialize a reading which is fed to the controller. The GETO pin is set low by a "TRIGGER" command in the computer software program. The "IND" command is used after the "TRIGGER" command to actually read in decimal data from the HP-IL device. The low GETO pin sets a latch in the interface IC in turn allowing a counter to sequence seven ASCII characters to the HP-IL. The counter is sequenced as the RDYO pin is set low if three conditions are met. Sequencing is prevented during the GETO pulse by the first of three conditional "AND" gates controlling the counter. The second gate is activated by the "TRIGGER" latch. In addition, an optional third gate is provided by the "Interface IC's" ENABLE pin (to be discussed later).

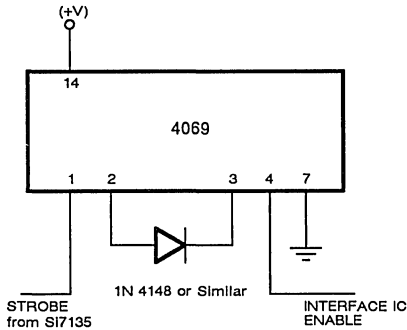


Figure 2. Optional Condition Circuit

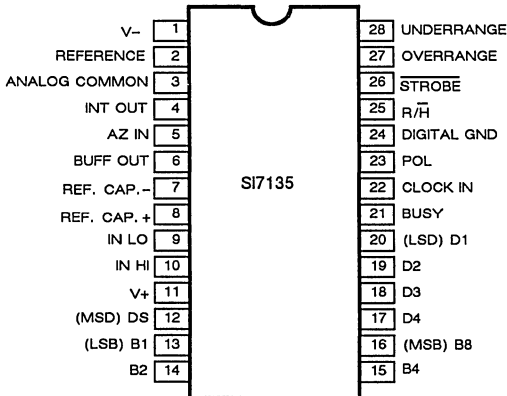


Figure 3. Si7135 Pin Out

The seven ASCII characters provide for a polarity character, five digits, and a hardwired ASCII "LF" command. This character is recognized by the controller as an "End of Data" statement. The counter is allowed to sequence one more step after the "LF" command which resets itself and the "TRIGGER" latch. The read cycle is now complete, and the interface IC is ready to send another reading. A very simple seven line program in the HP-41 will initialize the DVM, read in the data, display the data, and loop back to take another reading. This ATD program is shown in Table 1.

Table 1. ATD Program

01	LBL DVM1
02	LBL 01
03	TRIGGER
04	IND
05	VIEW X
06	GTO 01
07	END

Figure 1 shows a functional block diagram of the system that contains several levels of asynchronism. The HP-41 is asynchronous to HP-IL; HP-IL is asynchronous to the interface IC; and the "Interface IC" is asynchronous to the Si7135. The "Interface IC" must account for random events at all three levels and convert the polarity and strobed BCD outputs to the proper ASCII characters. A subtle but desirable trait of the interface is that it should not allow a reading by the HP-IL while the Si7135 is latching in new data. Additionally, the interface should not allow the latching of data while the HP-IL is reading. Either condition would result in an invalid entry. The ENABLE pin when used with the circuit in Figure 2 will prevent the counter from sequencing the ASCII characters. The result will be a repetition of a single character which will fill the HP-41 X Register. In turn, this may be checked with HP-41 software, and the data will be deleted preventing an HP-IL read during a latch change. Alternatively, this gate may be held high if an occasional invalid reading is permissible. With this configuration, about 3% of the readings will be invalid. "Invalid" is used here to describe the condition of reading in the five digit number from two separate Si7135 writings. For example, if the Si7135 latches in new data to the interface IC while the HP-IL is reading, perhaps the first two digits may be from the old voltage reading while three would be from new data. The other invalid condition is prevented by stopping the Si7135 with the "TRIGGER" activated latch. This is accomplished by setting the RUN/HOLD pin low and thus stopping the Si7135 cycle until the reading is complete.

### Si7135/"INTERFACE IC" HANDSHAKING

Data is latched into the "Interface IC" from the Si7135 by means of the four BCD data lines (Figure 4). They are routed to the proper character latch by the digit strobe pins. The polarity and most significant

digit are simultaneously latched with Digit Strobe One. The STROBE pin, which should not be confused with the five digit strobe pins, goes low five times after each voltage measurement in tandem with the sequencing five digit strobes. Thus, the latching of Si7135 data into the interface IC occurs only once during each measurement cycle as a condition of the Digit Strobe pins and the STROBE pin. There is one latch for each variable bit of the six variable ASCII characters. Non-variable bits, including the entire

"LF" command, are hardwired. These latches and hard wires feed tri-state buffers which are sequentially activated by the counter and consequently present their data to the ASCII output bus (DA) on GPIO.

Autoranging or multiple input select functions can be implemented using similar straightforward programming techniques. The under-range and over-range pins of the Si7135 are connected to the most significant digit buffer.

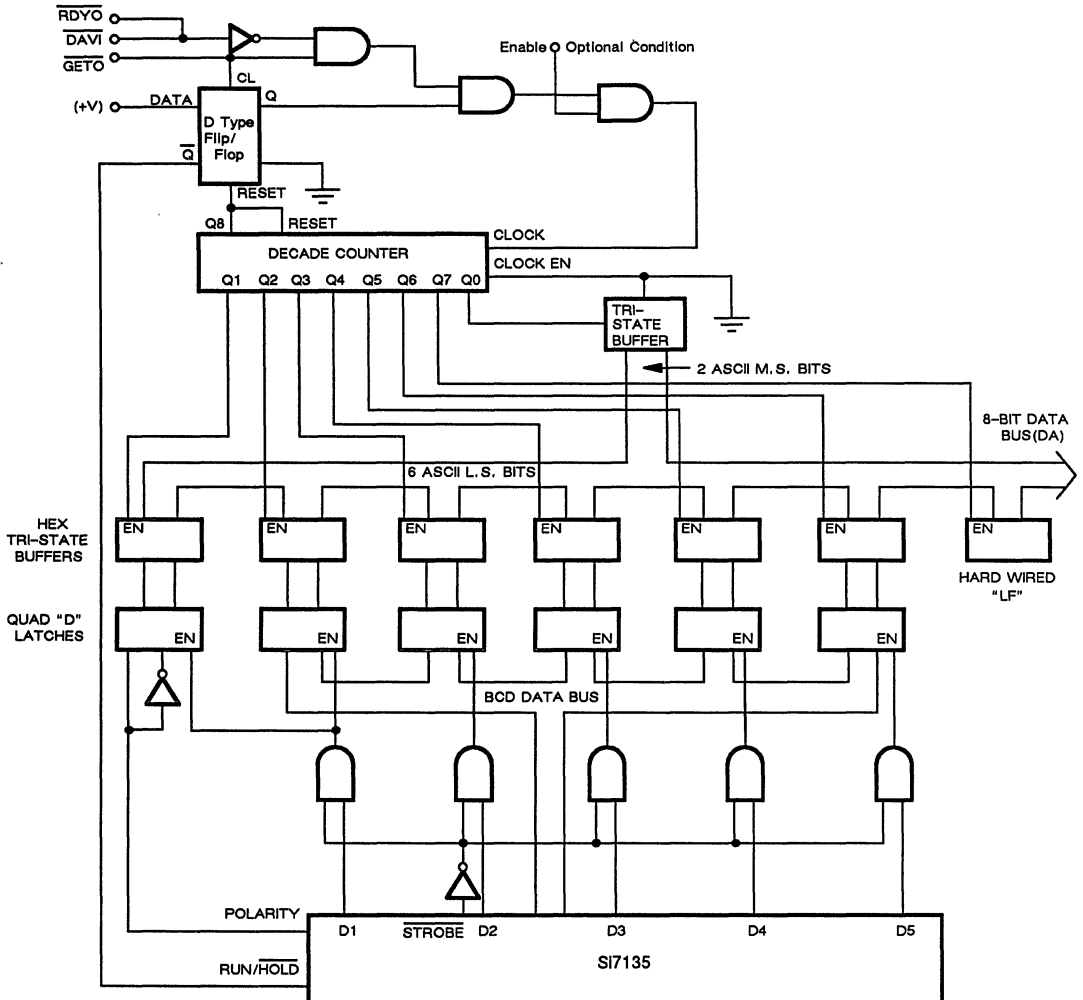


Figure 4. Simplified Circuit of Interface IC

Valid readings on the Si7135 range from -19999 to +19999. The under-range and over-range pins on the Si7135 are tied to the second and third bits of the most significant digit latch. Thus, during under-range, a numerical value slightly greater than or equal to 20,000 will be read, and 40,000 will be read during an over-range condition. These values along with the full register condition of the invalid reading discussed earlier can be checked by software. In the case of over or under-range, a subroutine can be called selecting an appropriately higher or lower scale. The scale called can also indicate the proper coefficient for correct numerical display and decimal placement. Therefore, meter calibration may take place in software if the sensor cannot be adjusted. Under and over-range as well as other Si7135 functions are optionally used by the designer. The "Interface IC" was designed to allow customizing the interface for a given set of functions and applications. The "Interface IC" is also useful with other A/D converters including the Siliconix "LD" family. Additionally, the great flexibility afforded by the software allows special readings such as dBm, dB gain, and radian measure, etc. Indeed, applications of this system seem infinite (bfd).

## HP-IL/MULTIPLEXER INTERFACE

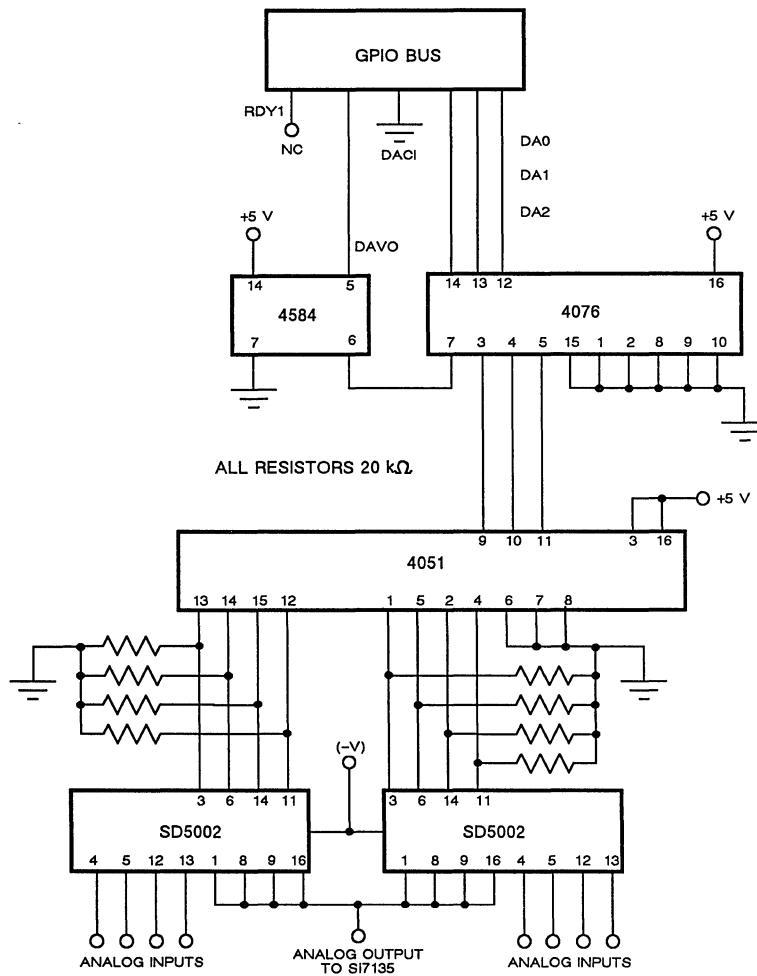
In the case of input selection, autoranging and function select, etc., the circuit in Figure 5 may be used. Here, eight inputs are used to feed the Si7135. When the multiplexer is receiving instructions, it actually becomes a listener. A relatively simple circuit is required for the interface between the SD5002s and the HP-IL; furthermore, this SD5002 circuit may be used as a stand-alone circuit for a wide range of analog switching functions. SD5002s can be configured into superior video, audio, or RF switching circuits featuring excellent cross-talk and low-distortion performance (Ref. 2 & 3). Additionally, Siliconix offers a wide range of analog switches and multiplexers to suit any application. Power control is possible with up to 650 volt power FETs and simple standard control circuits. Thus, Siliconix can be a single supplier of specialized components from the HP-IL "Interface IC" to HP-IL controlled high voltage FETs!

Three 4000 series CMOS ICs are required to interface data from HP-IL to the switch control gates. A sepa-

rate Si7661 is shown on the multiplexer circuit in case the multiplexer is built independently of the DVM. (Figure 1) If it is built independently, a higher supply voltage can be used. This will allow higher analog voltages to be switched. Siliconix also manufactures the SD210 series which are discrete switch devices; these may be used if superior channel isolation is required and/or higher signal voltages must be switched.

HP-IL/multiplexer handshaking is very straightforward. The  $\overline{\text{DAVO}}$  pin is used to enable a CMOS latch which stores the last three bits of the transmitted ASCII character. The  $\overline{\text{RDYO}}$  pin is not used while the  $\overline{\text{DACI}}$  pin is tied to ground. This is the simplest handshake scheme possible with HP-IL.

In the multiplexer, the three least significant bits of the ASCII character taken from the DA bus are used to select one of the eight analog inputs. The "OUTA" command in HP-41 software sends the contents of the Alpha Register to the IL device. The very simple hardware interface requires some special compensation in software. The most important constraint with this circuit is to send only one ASCII character at a time. This will prevent "glitches" and false data from being latched. In its normal operations mode, the HP-41 will automatically send an "End of Data" ASCII character at the end of an alpha string. The last ASCII character sent is the one which is latched into the multiplexer. For this reason, the "End of Data" character must be restrained. This is accomplished by setting Flag 17 "SF17" in the software. A more complex problem involves mathematical manipulations of numbers specifying the multiplexer channel. Such manipulations must take place with digital information - not alpha characters. Since HP-IL can only send data from the Alpha Register, these digital characters must be sent to the Alpha Register for transmission to the multiplexer. A problem arises because a decimal point "rides along" with the number to the Alpha Register. The decimal point is consequently read by the IL interface and sent as an ASCII character to the multiplexer causing a "glitch" or an invalid latch. This problem can be solved by clearing Flag 29 "CF29" and not displaying fraction data "FIXO". With these two additional simple commands, the desired numeric ASCII character will be latched into the multiplexer.



**Figure 5.** Multiplexer Schematic Diagram

## SOFTWARE EXAMPLE

Table 2 shows a simple program which will sequence the eight input multiplexer, display the input channel number, read in the voltage, display the voltage, and loop back. It is included to provide a sample program to get the system working and illustrate how the necessary commands can be arranged. The power of the HP-IL system may be appreciated when one sees only 29 lines of programming! The user will in most instances modify or rewrite programs to meet individual needs.

Details of HP software are contained in the literature provided with the applicable HP devices. The

HP82166C Interface Kit includes a very comprehensive system description of HP-IL contained in multiple volumes. One word of caution to the hardware designer; there are numerous errors and misleading diagrams in the HP booklet entitled "HP 82166A HP-IL Converter Technical Manual" (Nov. 81). The corrections to these errors are in a follow-up booklet "HP-IL/GPIO Interface HP-IL Converter Manual Supplement".

In conclusion, Siliconix offers the necessary integrated circuits to easily facilitate HP-IL interface to a low cost DVM design. This solution reduces the problem of such an interface to an easy layout task.



**Table 2**

01	LBL DVM1	16	-
02	0	17	X = 0?
03	STO 01	18	GTO 03
04	LBL 02	19	RCL 01
05	VIEW X	20	1
06	TRIGGER	21	+
07	IND	22	LBL 03
08	.0001	23	STO 01
09	*	24	CLA
10	FIX 4	25	ARCL 01
11	VIEW X	26	SF 17
12	FIX 0	27	OUTA
13	CF 29	28	GTO 02
14	RCL 01	29	END
15	7		

**REFERENCES:**

1. Electronic Design, Parzybok, Hanson, Dec. 24, 1981.
2. Siliconix Application Note: "A High Performance Video Switch", Zavrel.
3. Siliconix Application Note: "A High Quality Audio Crosspoint Switch", Zavrel.

## IMPROVED SYSTEM PERFORMANCE USING MICROPROCESSOR COMPATIBLE MULTIPLEXERS

Brian Wadsworth  
Walt Heinzer  
Revised January, 1988

### INTRODUCTION

These Siliconix CMOS multiplexers, the DG526, DG527, DG528 and DG529, feature the excellent characteristics of the DG506A-DG509A series with a bonus: latching logic. Microprocessor based systems are rapidly taking on more control tasks in electronic equipment. On-chip latching logic in a multiplexer does therefore greatly simplify the microprocessor interface design and improves system performance.

When the microprocessor is used in the "real world" of analog signals, it is often used in conjunction with analog multiplexers. Until recently, to interface the microprocessor to the multiplexer has meant the use

of some external memory device. These methods sometimes impaired system performance by compromising processor speed and always meant an increased component count. Two of these methods are illustrated in Figure 1.

With the introduction of these new multiplexers, the method of interface has been simplified. These devices have the latch function incorporated into the control circuitry of the multiplexer. Figure 2 illustrates functional diagrams of these multiplexers.

To examine the mode of operation, let us consider the DG528. The addition of the data latches on-chip has meant that two new control lines had to be introduced, i.e. WR and RS. Figure 3 shows a detailed diagram of these input latches.

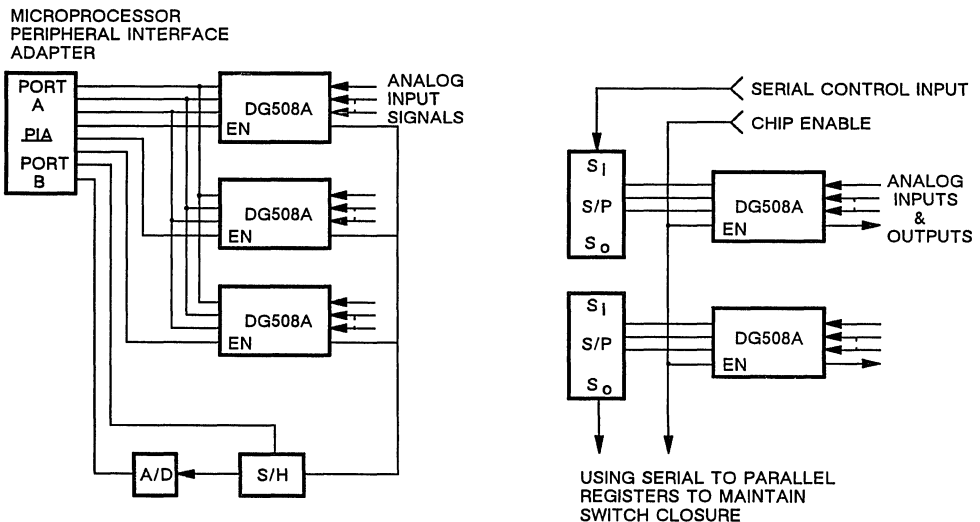


Figure 1. Traditional Methods of Driving the DG508 MUX/DMUX with a Memory Device

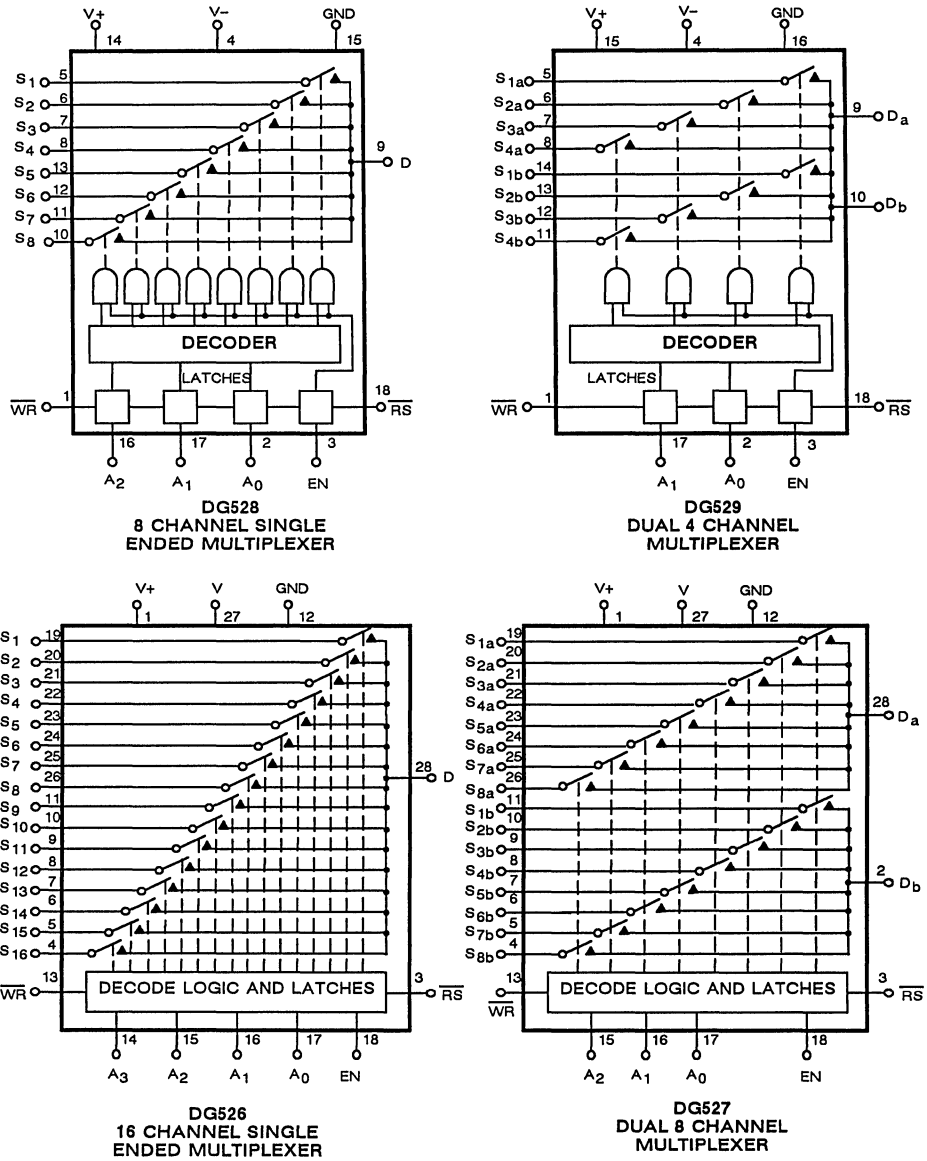


Figure 2.

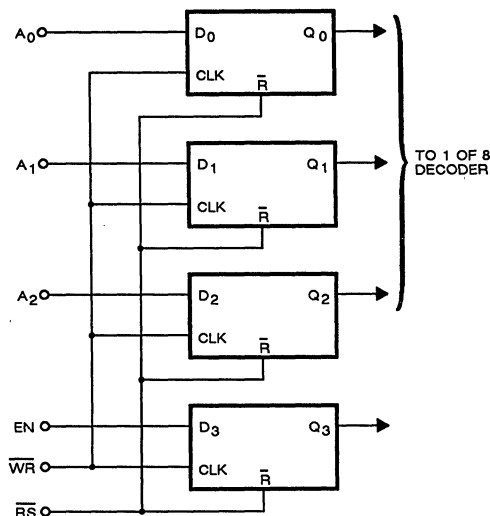


Figure 3. Detail of DG528 Input Latches

The first of these new control lines,  $\overline{WR}$  (WRITE BAR, active low) is connected to the gating input of the latches. These latches become transparent whenever  $\overline{WR}$  is driven to a logic low. During this state, data present on the address inputs is directly decoded and the appropriate switch closes. In fact, in this mode of operation ( $\overline{WR} = \text{low}$ ), the device functions identically to an earlier generation analog multiplexer, the DG508A. When  $\overline{WR}$  returns to logic high, it will save the data present on the address lines in the data register. This ensures that the switches remain in their selected state irrespective of excursions on the address inputs.

The second new control line,  $\overline{RS}$  (RESET BAR, active low), is an over riding direct reset facility. When the reset input is activated, all data latch Q outputs are forced low and all switches opened. This reset facility is especially useful in processor based systems during power-up conditions. At this time all switches can be cleared, "opened", preventing any undesirable switch action during initialization. If this initialization were left to software, it could easily take 10 to 30 instruction cycles to disable all switches. At an average  $1.3 + \mu\text{s}$  each, it means 13 to 39  $\mu\text{s}$  of undesirable switch contact could take place. Therefore the

direct reset facility provides a known safe power up initializing sequence.

The truth table shown in Figure 4 summarizes the logic control functions of the DG52X series.

## PERFORMANCE

### Logic Inputs

The logic interface circuitry of the address inputs and control lines have been designed to simplify microprocessor interfacing. Each of these inputs, due to their CMOS construction, draws very low current ( $< 10 \mu\text{A}$ ) and provides extremely low capacitive loads (typ. 25 pF). Switching thresholds of these inputs have been designed to be fully TTL compatible. These features combine to ensure that each device can be driven directly from the microprocessor data bus.

All the logic inputs to the device carry input protection circuitry to protect the device against static damage. This input protection circuit consists of diodes to both positive and negative supply rails and a series resistor. The diodes forward bias to discharge any static energy into the supply rails while the resistor limits the current during this time to protect the diodes.

DG526

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching							
X	X	X	X	X	$\overline{\downarrow}$	1	Maintains previous switch condition
Reset							
X	X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation							
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

DG527

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching						
X	X	X	X	$\overline{\downarrow}$	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

Logic "1": V<sub>AH</sub> ≥ 2.4 V

Logic "0": V<sub>AL</sub> ≤ 0.8 V

DG528

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching						
X	X	X	X	$\overline{\downarrow}$	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

DG529

A <sub>1</sub>	A <sub>0</sub>	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching					
X	X	X	$\overline{\downarrow}$	1	Maintains previous switch condition
Reset					
X	X	X	X	0	NONE (latches cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "1": V<sub>AH</sub> ≥ 2.4 V

Logic "0": V<sub>AL</sub> ≤ 0.8 V

Figure 4.

## On Chip Regulator

Also provided on-chip is a regulator which has been designed to provide stability against power supply and temperature variations. The design of this regulator ensures that:

- (a) TTL compatibility is maintained over a wide power supply variation.
- (b) Reduces the effects of temperature allowing the microprocessor timing specifications to be guaranteed over the full military temperature range,  $-55$  to  $125^{\circ}\text{C}$ .

## Interfacing

The DG52X series was designed to be fully compatible with the more popular NMOS microprocessors. In fact, the timing arrangements of the control lines were designed to be fully compatible with the 8085A-2 microprocessor. These minimum input timing arrangements are shown in Table 1. The diagrams shown in Figures 5 to 7 illustrate the ease with which these devices can be interfaced to various microprocessors.

Figure 5 illustrates the method of interfacing a DG528 to the 8085A processor. Notice that no additional

bus buffering is required between the processor data bus and the multiplexer address inputs. A standard address decoder chip is still required to generate the chip select,  $\overline{\text{CS}}$ , signal. This  $\overline{\text{CS}}$  is gated with the processor  $\overline{\text{WR}}$  output to generate the  $\overline{\text{WR}}$  signal for the DG528. These signals ensure that only when the DG528 is being addressed will information on the data bus affect switch states. This connection satisfies the processor's timing requirements since  $\overline{\text{WR}}$  will only go active low once the information on the data bus has stabilized. Figure 5 also illustrates the direct connection between the processor system  $\overline{\text{RESET}}$  and the multiplexer  $\overline{\text{RS}}$ .

The method of interface between the multiplexer and 6800 microprocessor bus is illustrated in Figure 6. In order to have a data valid signal, it is necessary to gate the  $\phi 2$  clock (often directly connected to the DBE) with R/W line. The gating of the chip select with the  $\phi 2$ . R/W combination is functionally identical to the 8080 connection.

The Z80 to multiplexer interface is shown in Figure 7. Simply by gating the  $\overline{\text{WR}}$  and  $\overline{\text{MREQ}}$  signals with the standard  $\overline{\text{CS}}$  signal allows the correct  $\overline{\text{WR}}$  signal for the multiplexer to be achieved.

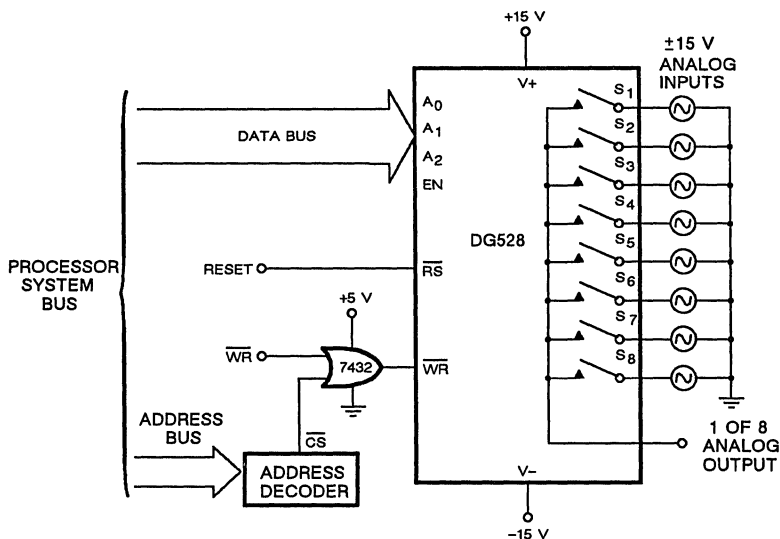


Figure 5. Complete 8085 Microprocessor to DG528 Interface

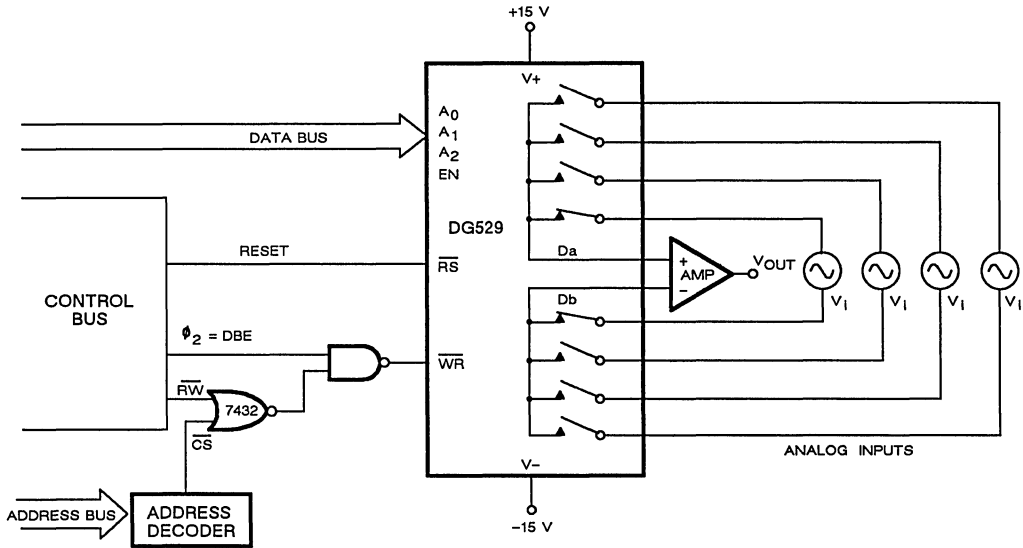


FIGURE 6. Complete 6800 Microprocessor Bus to DG529 Interface

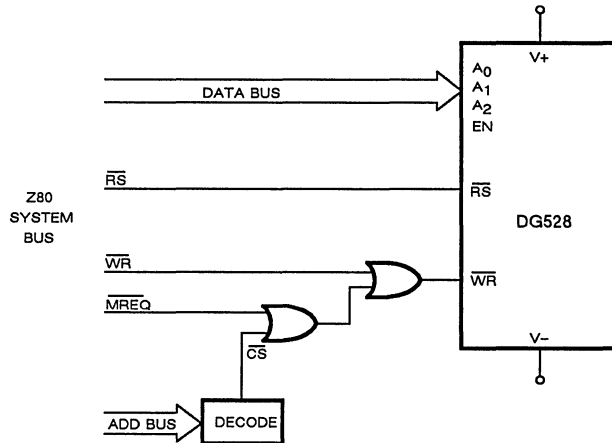


Figure 7. Z80 TO DG528 Interface

## The Process

These devices have been constructed using a high voltage CMOS process called PLUS 40. This process was designed to provide a more rugged device while at the same time offer performance improvements over the original CMOS process. Basically, two features improve the ruggedness of the device:

- (a) The gate oxides of the MOS transistors have been thickened, improving the DC rupture voltage by 33%. Combining this benefit with the improved input protection circuits and body clamped switch design results in improved static voltage immunity.
- (b) The process maximum rating has been increased. PLUS 40 CMOS devices have an absolute maximum rating of 44 V between supply rails. This means that devices can be operated at  $\pm 15$  V supplies and still be within 75% of their maximum ratings.

Another important improvement achieved on the PLUS 40 process was the introduction of an ion-implantation technique. This technique allows much greater process control which results in very uniform, repeatable device parameters. In the case of analog multiplexers, for example, we achieve better matching characteristics switch to switch.

## CHARACTERISTICS

Having discussed the performance of the device, we can now look at some of the important characteristics involved:

1. First, the most critical specification of the device is its microprocessor timing arrangements. As was mentioned earlier, the timing of these devices was designed to be compatible with the 8085A. In actual fact the timing is such that the 8085A-2 can be operated on its maximum 5 MHz clock rate. The waveforms shown in Figure 8 illustrate the timing specifications for the DG52X series.

Minimum Input Timing Requirements			
Parameter	Measured Terminal	Min Limits over full temp. range	Unit
$t_{WW}$ WRITE Pulse Width	$\overline{WR}$	300	ns
$t_{DW}$ A, EN Data Valid to WRITE (Stabilization Time)	$A_0, A_1, (A_2), E_n$ $\overline{WR}$	180	
$t_{WD}$ A, EN Data Valid after WRITE 3 (Hold Time)	$\overline{WR}$ $A_0, A_1, (A_2), E_n$		
$t_{RS}$ RESET Pulse Width	$\overline{RS}$	500	

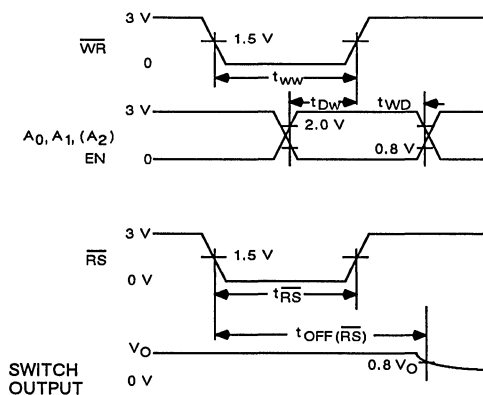


Figure 8. Timing Diagrams



2. Another parameter of importance, especially in such applications as sample and hold, is that of charge injection. The graph shown in Figure 9 shows a typical curve for this parameter. In fact all PLUS 40 devices have compensation on the output switches to reduce switching errors due to charge injection.

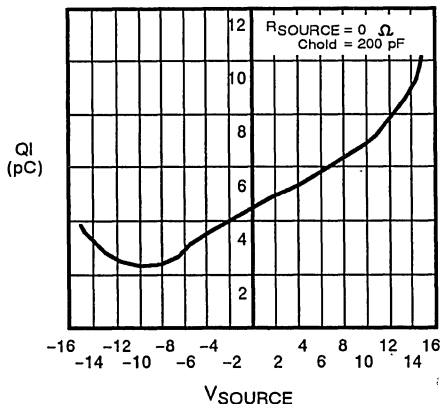


Figure 9. Charge Injection vs. Analog Signal

3. The  $V_{ERROR}$  figure of merit is sometimes used as a parameter for evaluating switch performance. This parameter is the product of  $r_{DS(ON)}$  and  $I_{D(ON)}$  switch leakage current. It is a primary contributor to switch voltage errors when switching very low level signals such as thermo-couple voltages. The DG528 has a worst case specified  $V_{ERROR}$  of 100  $\mu V$  at 125°C, while at room temperature this figure reduces to 4  $\mu V$  maximum.

## SUMMARY

We are now in a position to analyze this information to identify user benefits. These benefits can be itemized as shown below:

1. The ease of interfacing means that component count is reduced. This has the obvious benefit that overheads are reduced because component, inventory, manufacturing and production costs are reduced. Also, because component count is reduced, the systems reliability is increased.

2. Because the timing arrangements are fully micro-processor compatible, then a more efficient system performance is obtainable.
3. Much simpler power supply requirements are facilitated due to the on-chip regulator and the PLUS 40 construction.
4. Its PLUS 40 construction also means a more reliable, high performance device.

## APPLICATIONS

### Temperature Monitoring

In these systems, an array of transducers are switched one at a time to an analog-to-digital converter. Figure 10 illustrates the necessary steps in designing the front-end system. This system assumes that the transducers generate small differential signals upon which fairly large common-mode noise is superimposed. This common-mode signal can be assumed to be 50 or 60 Hz power line pick-up. Transducers with this type of characteristic would be thermistors wired in a bridge configuration.

To calculate the errors introduced by the multiplexer, assumptions about the range of the differential signal,  $V_{diff}$ , need to be made. A weighted thermistor bridge will easily have an output voltage swing of 0 to 100 mV, representing an input temperature range of 0 to 100°C. The second assumption is that the common mode noise pick-up is approximately 2 V p-p. Finally, a measurement accuracy of 1%, or 1°C is required from a bridge with nominal output impedance of 500  $\Omega$ .

There are basically two sources of errors to analyze:

- (a) DC errors contributed by the multiplexer. Figure 11 shows the steady-state differential voltage input path for one switch closed. As can be seen, the primary error source is the product of leakage currents in the signal path resistances. These leakage currents generate additional system offset voltages which, even though the bridge presents an unbalanced resistance, are acceptable.
- (b) Common-mode voltage becoming a differential error due to the resistively unbalanced signal paths. This is the major contributor toward system error.

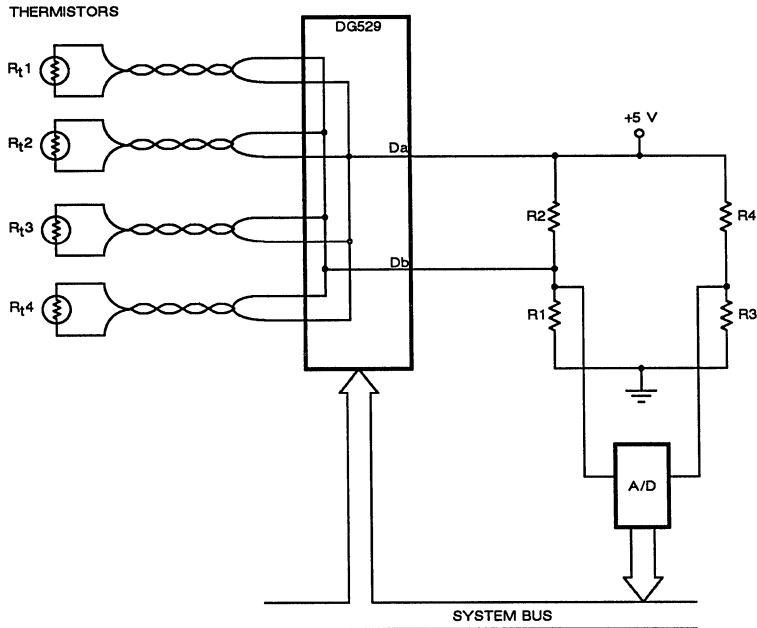


Figure 10.

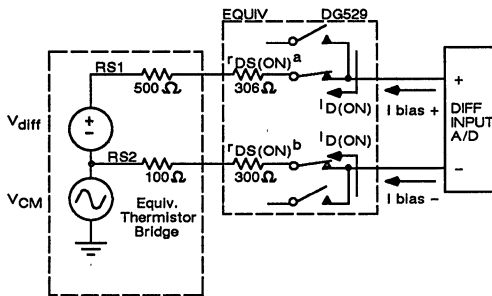


Figure 11. Steady State Errors

The total error voltage due to the DG529 is calculated as:

$$\begin{aligned}
 V_{\text{error}} &= I_{D(\text{ON})} \times (r_{DS(\text{ON})a} + 500) - I_{D(\text{ON})} \times (r_{DS(\text{ON})b} + 100) \\
 &= 10 \text{ nA} \times (306 + 500) - 10 \text{ nA} \times (300 + 100) = 4.06 \text{ } \mu\text{V}
 \end{aligned}$$

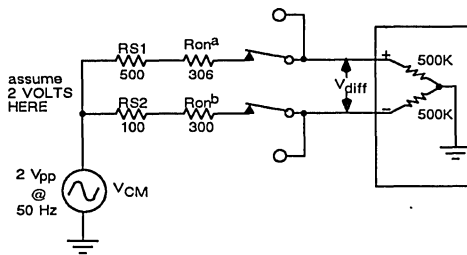
Thus the multiplexer contributes negligible offset error.

The differential input A/D would contribute an additional offset of:

$$\begin{aligned}
 V_{\text{error}} &= I_{\text{BIAS}} (+) \times (r_{DS(\text{ON})a} + 500) - I_{\text{BIAS}} (-) \times (r_{DS(\text{ON})b} + 100)
 \end{aligned}$$

Figure 12 shows how the common-mode voltage directly adds to the differential signal representing temperature. The net result is a 50 Hz differential error signal, superimposed on the DC temperature signal, of 1.6 mV p-p. This represents an error of 2°C which can be eliminated using an integrating A/D sampling at an integer multiple of the 50 Hz noise frequency.

It is worth pointing out at this point that if the bridge resistances were balanced, i.e.  $RS1 = RS2 = 500 \text{ } \Omega$ , then the multiplexer would only contribute a 0.024% error (assuming a 2% match for switch on-resistance). The dynamic characteristics of the switches are relatively unimportant in this application since temperature is a slowly varying signal.



**Figure 12.**

The instantaneous voltage appearing at the input to the A/D due to the 2 volt peak to peak common mode voltage is:

$$V_{diff} = (500 \text{ k} / (500 + 306 + 500 \text{ k}) - 500 \text{ k} / (100 + 300 + 500 \text{ k})) \times 2 = 1.6 \text{ mV}$$

The 1.6 mV adds to the thermistor output voltage signal as a superimposed 50 Hz normal mode voltage. This signal can be rejected by using an integrating A/D converter sampling at an integer multiple of the 50 Hz noise period.

**AUTOMATIC TESTERS**

In this application the dynamic performance of the switch is of importance. Figure 13 illustrates a PC board continuity tester, and this can be used to demonstrate the advantages of the DG528. To ensure that no paths (dendrites) for electro-migration are present, these testers require 30 V bias between tracks.

Figure 14 shows a technique for applying the 30 volt bias to the PC board to perform the insulation test. The sense resistor is connected in series with the insulation resistance to form a voltage divider. The output of the divider is measured by the high input impedance sense amplifier. The sense amplifier output is then compared with a programmable limit to determine the test result. The critical multiplexer specifications in this application are leakage currents

and capacitances. Leakage currents limit the maximum measurable resistances while capacitance increases the measurement settling time.

Switch leakage currents should be 10% of measured current to enable 100 MΩ resistances to be measured. Therefore maximum leakage should be:

$$\frac{10}{100} \times \frac{10}{100} \mu\text{A} = 30 \text{ nA}$$

The DG528 has a maximum I<sub>D(OFF)</sub> leakage of 10 nA at +25°C.

Capacitive loading is only critical for the test-node since it must charge through the insulation resistance. The force node is low impedance, therefore does not have a critical capacitance requirement. This capacitive loading on the test-node defines the maximum achievable speed.

C<sub>D(OFF)</sub> is specified as 25 pF for the DG528. Assuming a 100 MΩ test limit, this loading results in a 2.5 ms circuit test time-constant. If multiplexers are being cascaded and sharing the test-node then the time constant can be calculated using the formula: N X Insulation Resistance X 25 pF, where N = number of multiplexers.

The second function of the tester is continuity testing, and this is illustrated in Figure 15. This circuit design uses 4 wire sensing to eliminate errors generated by IR drops in the forcing current path. Switch and probe-to-PC Board contact-resistance no longer limit the measurement of the copper foil continuity. Testing speed is fairly fast since all impedances are low, keeping circuit time constants short. To minimize the total test time a high slew rate sense amplifier should be used.

One final point is that because the DG528 has full bi-directional switching capabilities, the insulation and continuity tests share the same set of matrix switches.

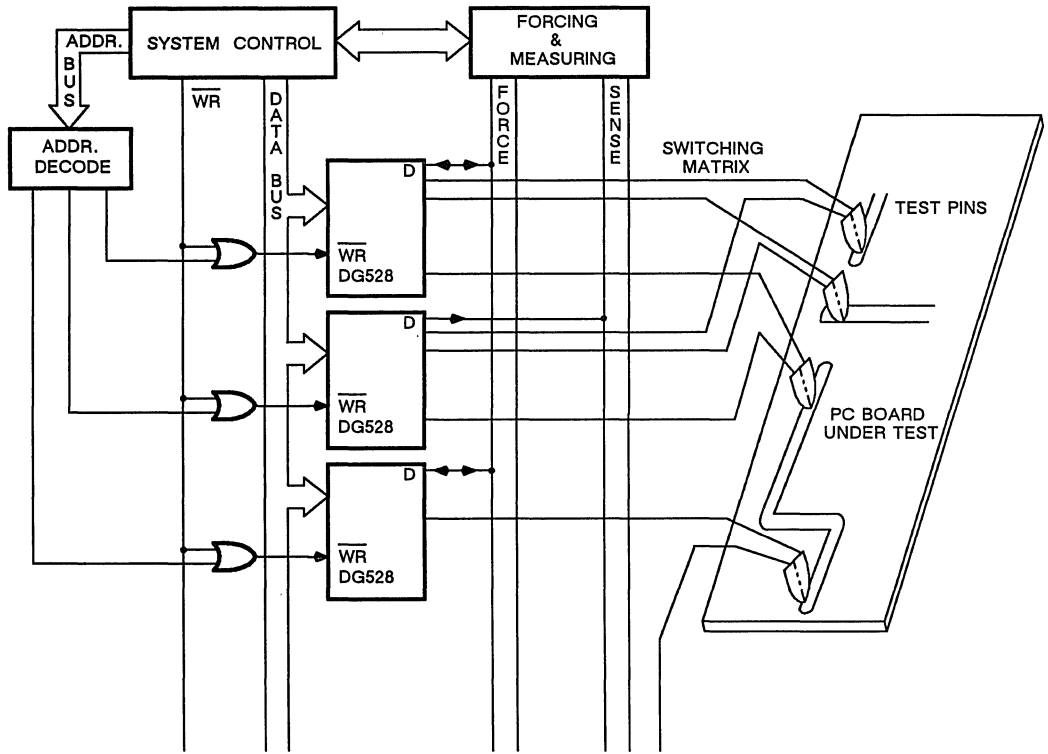


Figure 13. PC Board Continuity Tester

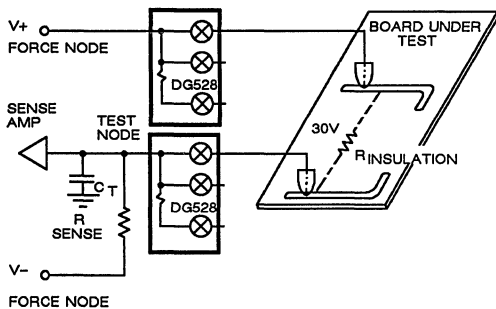


Figure 14. Simplified Circuit Highlighting the Insulation Test

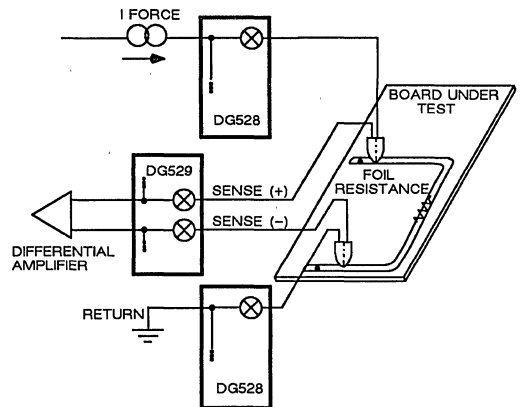


Figure 15. Simplified Circuit Highlighting the Continuity Test Using Kelvin (4 wire) Sensing

**DATA ACQUISITION**

The circuit shown in Figure 16 is intended to highlight the benefits of the microprocessor compatibility of the DG526-8. Note that this circuit also contains DG221 analog switches. The DG221 is a quad SPST switch with the same microprocessor timing arrangements and compatibility as the DG528 (with the exception of  $\overline{RS}$ ).

The adaptive gain software control algorithms available for process control systems make microprocessor based systems very attractive in these applications. Now, with the advent of the DG528, complete data acquisition systems can be simply interfaced to the processor. The software can then be written to maximize the efficiency of the system by managing the system organization.

All the components used in this circuit have been selected due to their microprocessor compatibility.

Because the gain of the sample and hold amplifier is programmable, the DG528 can multiplex signals of various magnitudes. The sample and hold amplifier

can then condition these signals for the input requirements of the A/D converter.

Conversely, the 'back-end' system utilized the DG528 as a demultiplexer where signal outputs from the D/A can be used for various functions. For example, it may be a corrective signal to a controller to reduce system error or simply a signal for an analog display.

**PROCESS CONTROL**

Figure 17 illustrates a novel use of the DG527. Differential multiplexers are generally used in process control applications to eliminate errors due to common mode signals. In this circuit however, advantage is taken of the dual multiplexing capability of the switch. This is achieved by using the multiplexer to select pairs of RC networks to control the pulse width of the multivibrator. This can be a particularly useful feature in process control applications where there is a requirement for a variable width sample "window" for different control signals.

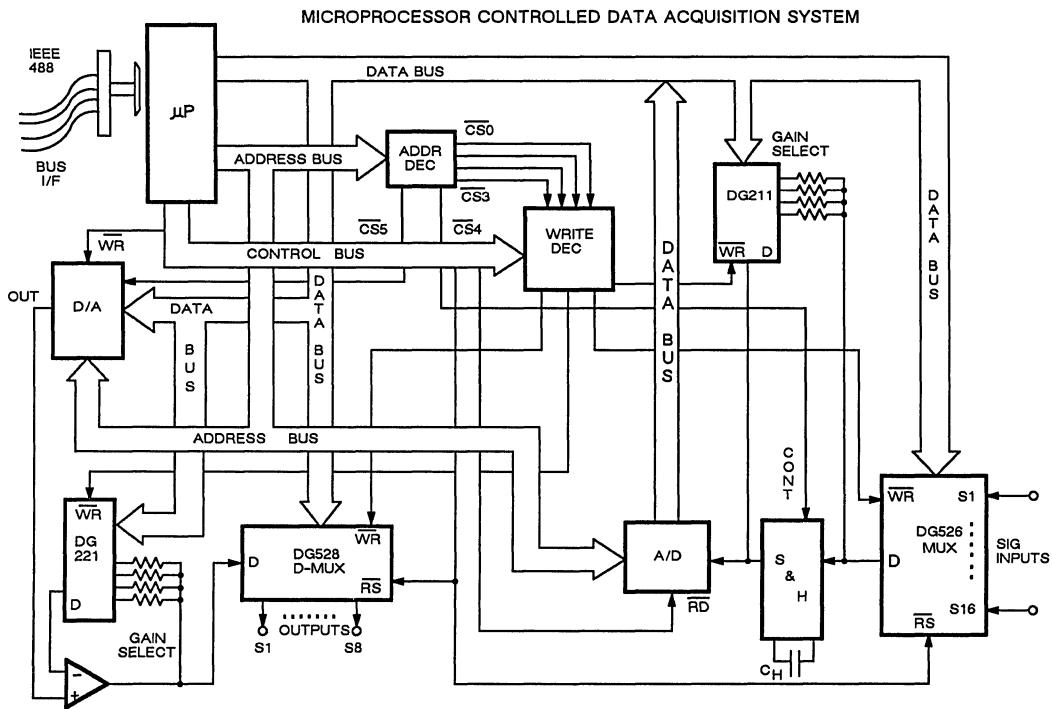


Figure 16. Enhanced System Performance using DG221, DG526 & DG528

## EXAMPLE PROGRAM

Hex Add.	Hex Code	Assembler Code	Description
(20)00	31	LXI SP, 2080H	Initialize stack pointer.
01	8φ		
02	2φ		
03	3E	MVI A, φA	Set interrupt register value.
04	φA		
05	3φ	SIM	Set interrupt mask (loads interrupt register from accumulator).
06	FB	EI	Enable interrupt at this point (when interrupt key is pressed, program runs until this point).
07	3E	MVI A, φF	Load the accumulator with the value φF Hex (this represents "enable" switch 8).
08	φF		
09	32	STA, 8400H	Store the accumulator value memory location (8400H is the location of the 528 in this application.)
0A	φφ		
0B	84		
0C	3E	MVI A, φ8	Load accumulator with the value φ8 Hex (this represents "enable" for switch 1).
0D			
0E	32	STA, 8400H	Store the accumulator value at memory location 8400 Hex.
0F	00		
10	84		
11	C3	JMP, 2006H	Jump (loop)back to the enable interrupt at location 2006 Hex and start again.
12	06		
13	20		
CE	FB	EI	When interrupt (VECT INT) key is pressed, the monitor transfers control to location 20CE Hex.
CF	76	HLT	
D0	C9	RET	

Example Program Run In the Circuit Setup of Figure 16 with the SDK-85 Development System.

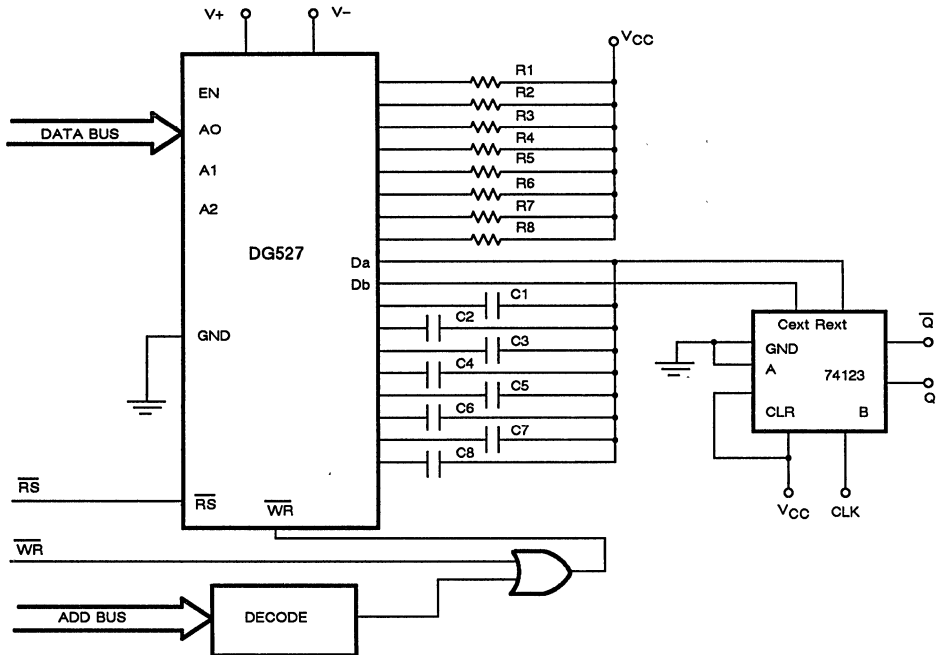


Figure 17.  $\mu$ P Selected Pulse Width Control

# A MICROPROCESSOR COMPATIBLE ANALOG SWITCH MAKES INTERFACING EASY

Brian Wadsworth  
Revised January, 1988

## INTRODUCTION

The advances made over recent years in the field of microprocessor programming have made the microprocessor a very attractive tool for systems designers. Not only does the processor significantly reduce systems component count, but the increasingly complex algorithms developed give the microprocessor greater flexibility especially for the measurement or control of analog signals.

Until recently, to interface the digital world of the microprocessor to the "real world" of analog switches has meant the use of some type of memory device. If these memory devices are not used then the processor data bus had to remain tied to the logic inputs of the analog switch. This memory function employed one of the following devices: A shift register, a flip-flop, or a special peripheral interface adapter. Some of these methods are shown in Figure 1.

The DG221 quad latching analog switch combines both functions on a single chip. These latches eliminate the requirement of "WAIT STATES" used to accommodate slower I/O functions which compromise processor speed. This simplifies the interface methods and facilitates more efficient microprocessor performance.

The data latches are activated by the  $\overline{WR}$  (active low) input. These latches become transparent whenever  $\overline{WR}$  is driven to a logic 0. At this time, the

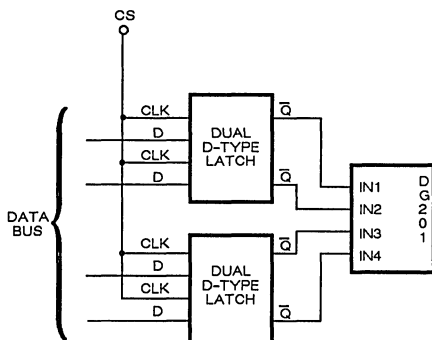
DG221 is functionally identical to the popular DG201A to which it is also pin compatible, except for pin 12 which is used for the  $\overline{WR}$  input. The logic truth table and pin configuration for the DG221 are shown in Figure 2.

## Circuit Details

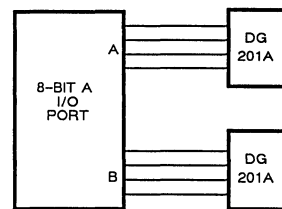
The circuit shown in Figure 3 is a simplified schematic of a single channel. It shows the logic interface circuitry, coupled with input protection, followed by D-type latches, level shift and driver circuitry, and finally the CMOS output switch.

The logic interface circuit has been designed to make microprocessor interfacing as simple as possible. The digital inputs, due to their CMOS construction, draw negligible current and provide extremely low capacitive loads ( 5 pF typ.). Full TTL input compatibility is guaranteed without the external pull-up resistor. These features combine to ensure that the DG221 can be driven directly from the microprocessor data bus without overloading the bus. The input protection circuitry consists of internal diodes to both supply rails which forward bias to discharge any static energy into the supply rails. A series resistor is included to limit the current to the forward biased diodes.

The D-type latches are driven from the  $\overline{WR}$  input and in its normal high state will isolate the output switches from excursions as the processor data change.



A. USING EXTERNAL LATCHES TO MAINTAIN SWITCH CLOSURE



B. USING I/O PORT AS GATED BUFFER

Figure 1. Traditional Methods of Interfacing using Memory Devices

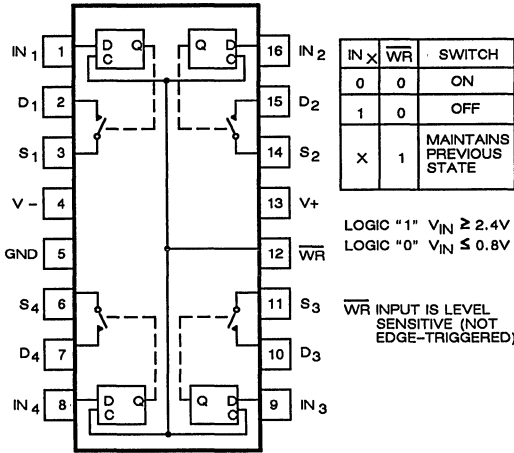


Figure 2. Pin Configuration

The level shift and driver circuitry enables a full  $\pm 15$  volt analog signal to be switched by the CMOS output switch. The switch uses body snatcher transistors in its construction to improve switching performance by snatching the body of the N-channel MOSFET to different potentials, depending on the switch state. In the OFF-state, the body is snatched to the negative rail which improves OFF-isolation by providing a low impedance path for high-frequency signals. In the ON-state, the body and source of the N-channel MOSFET are shorted, which reduces the threshold value.

A measure of switch performance is the error voltages introduced by the switching element, often referred to as the  $V_{ERROR}$  figure of merit. This error is the product of  $r_{DS(ON)}$  and  $I_{D(ON)}$  maximum leakage quoted for the device. The extremely low leakage of 5 nA max. (10 pA typ.), combined with the low ON resistance of 90  $\Omega$  max. (60  $\Omega$  typ.) of the DG221, combine to give an error voltage of 0.45  $\mu V$  maximum at room temperature. A signal level of 4.5 mV would remain 99% accurate. This switch is very suitable for low level signal switching applications.

Finally, the regulator used for the DG221 is a feature which is unique to the data latch analog switch range produced by Siliconix. It is used to maintain a constant internal reference voltage for defining digital input switching thresholds at 1.4 V, allowing the device to maintain its TTL input compatibility over large power supply variations. The regulator has also been designed to reduce the effects of temperature on parameters such as switching threshold and switching speed, thus minimizing drift due to ambient conditions over the full military temperature range of  $-55$  to  $125^{\circ}C$ .

### Interfacing The DG221

The latch timing arrangements have been designed to be fully compatible with the more popular NMOS microprocessors, e.g. 8085A, 6800, Z80. The timing arrangements for DG221 are given in Figure 4. The timing requirements of the 8085A have also been included for comparison to illustrate the full microprocessor compatibility of the DG221.

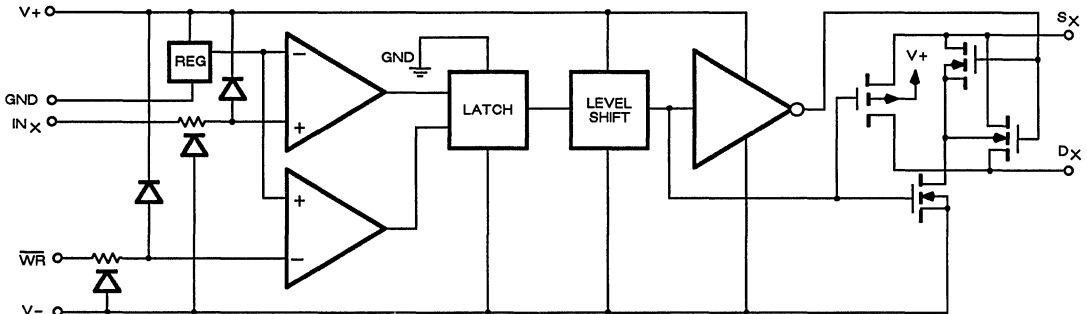


Figure 3. Functional Schematic (single channel shown)



Although the DG221 was designed primarily to be compatible with the 8085A, it can also be used in conjunction with the MC6800 series and Z80 family of processors, as the interface circuits shown in Figures 5, 6 and 7 illustrate.

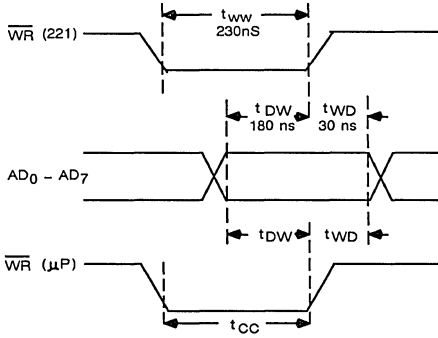


Figure 4.

$t_{ww}$  Width of Control Low ( $\overline{WR}$ )  
 $t_{DW}$  Data Valid to Trailing Edge of Write  
 $t_{WD}$  Data Valid after Trailing Edge of Write

	8085A	8085A-2	DG221
$t_{ww}$	400 (min)	400 (min)	400 (min)
$t_{DW}$	420 (min)	420 (min)	420 (min)
$t_{WD}$	100 (min)	60 (min)	30 (min)

This also illustrates how the DG221 more than meets the timing requirements of the faster 8085A-2.

All times are in nano seconds.

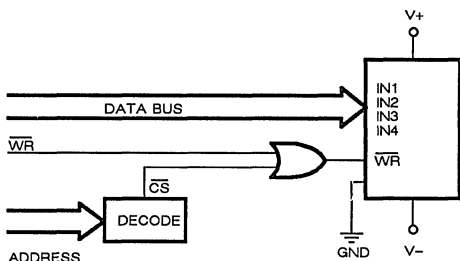


Figure 5. 8085-221 Interface

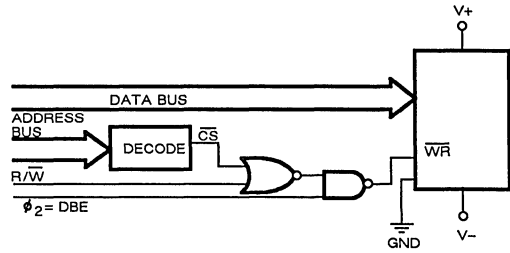


Figure 6. 6800 Interface

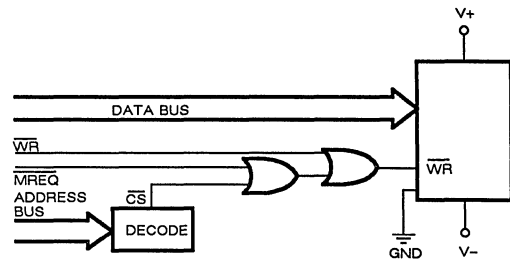


Figure 7. Z80 Interface

### Typical Applications

The DG221 is intended for use in microprocessor applications where the data latch facility can be of great benefit. The circuits included in this article are intended to highlight the benefits offered by the DG221, while at the same time generating some ideas for design engineers.

Figure 8 shows the use of the DG221 in an alarm system. The low loading offered by the DG221 to processor outputs enables several DG221's to be operated in parallel without overloading the processor outputs. A lower component count results by using the DG221 as a Mux in the alarm sensor circuit.

The amplifier shown in Figure 9 has processor-controlled gain and inputs enabling analog signals of varying magnitudes to be switched to a common amplifier. This is achieved by ensuring the amplifier has the appropriate value of feedback resistance for the correct output level. The DG221 looks into the high input impedance of the op amp so the effects of  $r_{DS(ON)}$  are negligible. Furthermore, since the DG221 can handle positive and negative signals, the unity gain connection on the op amp is possible.

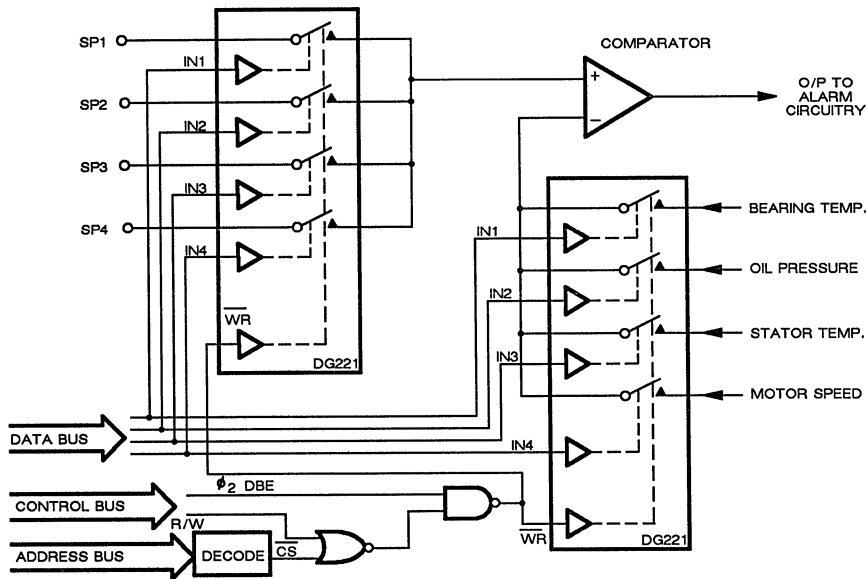


Figure 8.  $\mu$ P Controlled Alarm Monitor

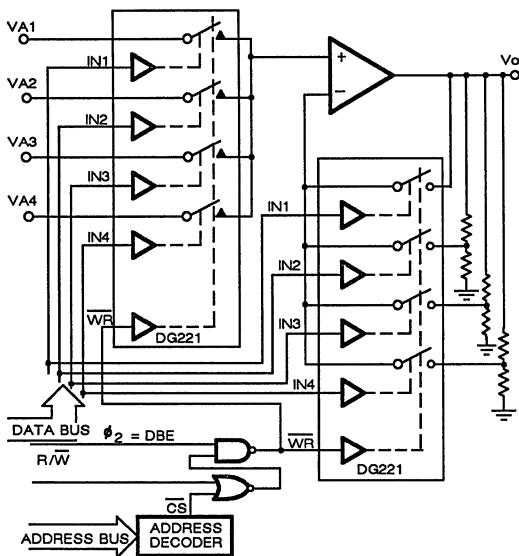


Figure 9.  $\mu$ P Controlled Variable Gain-Amplifier

Figure 10 highlights the combined use of the DG221 and DG528 in a 32-channel MUX system. Because the timing arrangements for these devices are identical, they can readily be used together. The reset facility on the DG528 is particularly useful for synchronization of channel 1 during "power up" condition. The 2-level system has several advantages over a single-level system. These are:

- (i) reduced output capacitance.
- (ii) reduced output leakage current.
- (iii) much faster switching speed, thus higher data transmission rates.

The switching of intensity and position in a CRT video display is simplified by using the DG221 in a processor-based system, as is illustrated in Figure 11. This circuit can also be adapted for radar multiplexing because the DG221 allows both the radar trace and a marker to be displayed simultaneously since it can be "programmed" to have more than one switch closed at any one instant.

The final circuit shown in Figure 12 shows the use of the DG221 and the DG528 in a remote, processor-controlled measurement system.

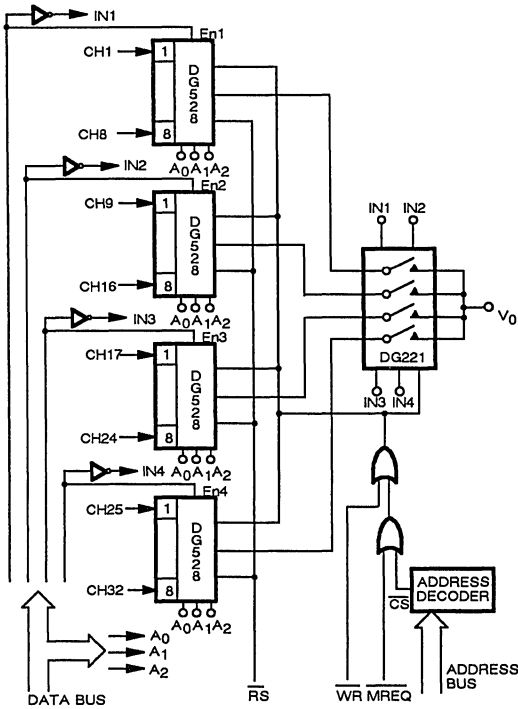


Figure 10. 2-Level 32 Channel Mux System

The DG221 is used to condition the input signals to suit the input requirements of the A/D, allowing the system to be used to measure signals of various magnitudes.

The typical area where this may be use is in automatic test equipment. In this application, the DG528 can be used as a demultiplexer to effect the illumination of the required status lamp to indicate the test result.

As was mentioned earlier, these are only example applications. Other application areas for the DG221 include: communication systems, home security, avionics, instrumentation, data acquisition, etc.

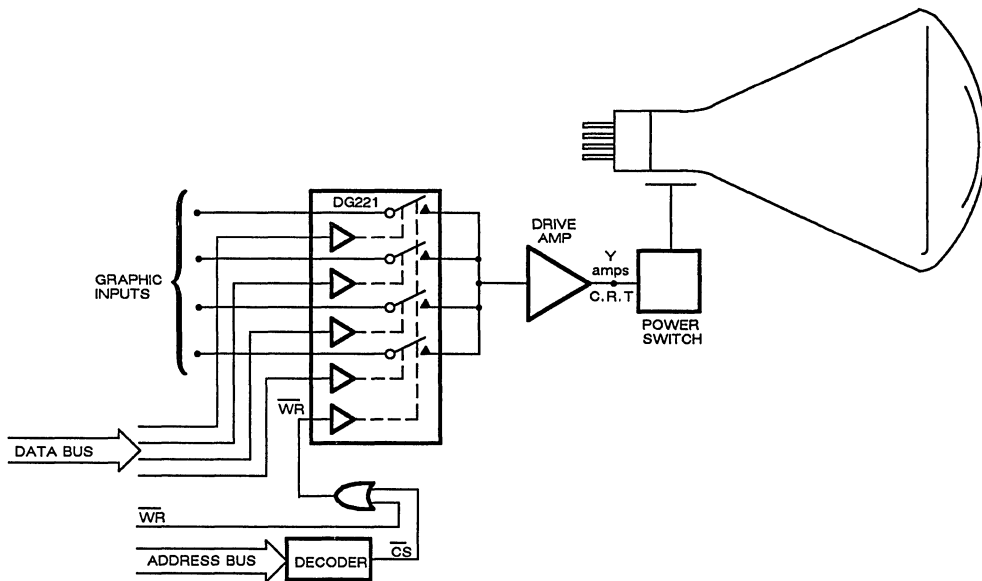


Figure 11. Simple Multiplexing

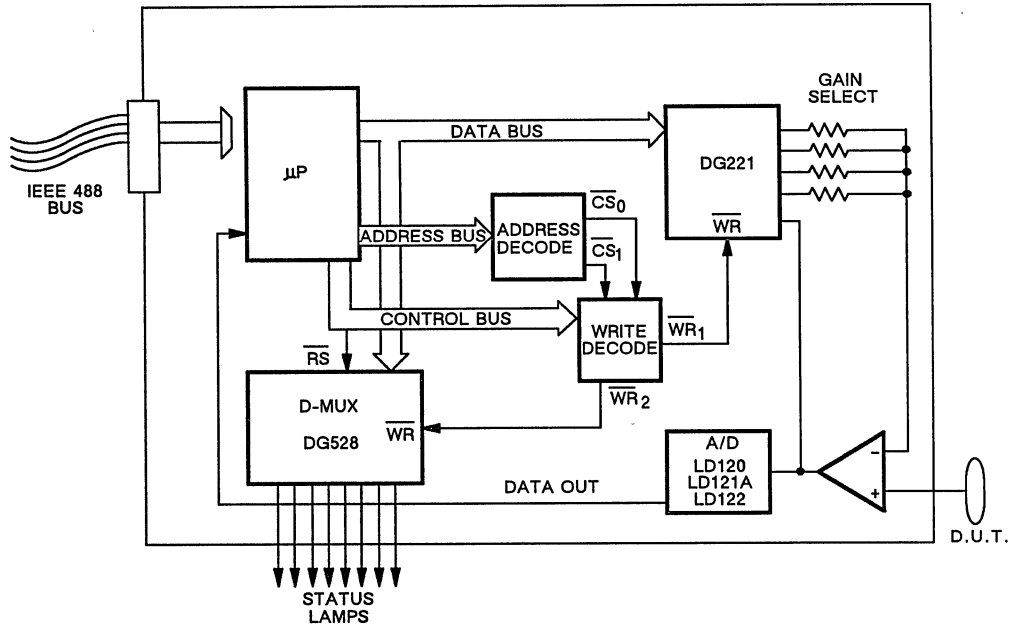


Figure 12. Remote/Processor Controlled Measurement System

## CONCLUSION

The DG221 quad switch is an extremely reliable and rugged analog switch designed primarily for microprocessor applications. The on board latches have been designed to simplify microprocessor interfacing techniques while at the same time allowing more efficient processor use.

The on board regulator gives much greater stability against circuit and ambient conditions, while switch performance achieves very low switching errors.

In short, the DG221 is synonymous with high performance, real-world microprocessor applications.

## THE PROCESS

The DG221 is fabricated on our high voltage CMOS process developed by Siliconix called PLUS 40. This process continues to use the buried layer technique for prevention of CMOS latch-up. This new process was originally designed to provide a more rugged device in transient environments. To achieve this, first

the gate oxides were made thicker to increase the dc rupture voltage by 33%. When this is combined with the logic input protection and CMOS switch body-clamping diodes, an overall improvement in static damage immunity is achieved. Secondly, the increased voltage rating means normal operation is accommodated with less stress to the device; thus, the PLUS 40 process improves reliability as well as the immunity to static damage.

To achieve this increase in process maximum breakdown voltage, an ion-implantation technique is used. This technique has the benefit of allowing greater process control to be achieved which enables very uniform repeatable device parameters to be realized. One example of this is that switch-to-switch ON resistance variation has been improved to less than 2%.

Finally, due to its PLUS 40 CMOS structure and on board regulator, a much simpler power supply design has been facilitated. The 44 V rating allows a greater margin for overvoltage while the on board regulator allows for large power supply variations.

# The DG308A Digitally Switches Analog Signals

Walt Heinzer  
September 1983

## INTRODUCTION

The latch proof CMOS DG308A interfaces easily to system power supplies since it operates from  $\pm 5$  V to  $\pm 15$  V, or it operates with a single supply from +5 V to +25 V, all CMOS logic compatible. Additionally, the DG308A consumes negligible standby power and can switch in less than 200 ns. To minimize analog signal error the DG308A has a maximum  $r_{DS(ON)}$  of 100  $\Omega$  over the full analog signal range which extends to the positive and negative power supply, at the same time OFF state signal errors are kept small by low leakage currents.

## More About The DG308A:

One channel of the four channel DG308A is shown in Figure 1 which displays the input protection, logic interface, internal level shifting and switch contact circuitry. With  $V_+ = 15$  V and  $V_- = -15$  V, a logic "1" control input ( $V_{IH} = 11$  V minimum) will close the switch, and a logic "0" ( $V_{IL} = 3.5$  V maximum) will open the switch. The ON resistance of the switch over the analog signal range has the characteristic double peaked curve shown in Figure 2. The OFF re-

sistance plotted as a leakage current in Figure 3, combined with the ON resistance characteristic of Figure 2, guarantees full ON/OFF operation between the  $V_+$  and  $V_-$  ( $\pm 15$  V) power supply rails.

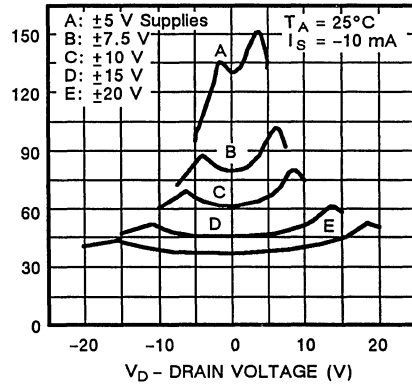


FIGURE 2.  $r_{DS(ON)}$  vs.  $V_D$  and Power Supply Voltage

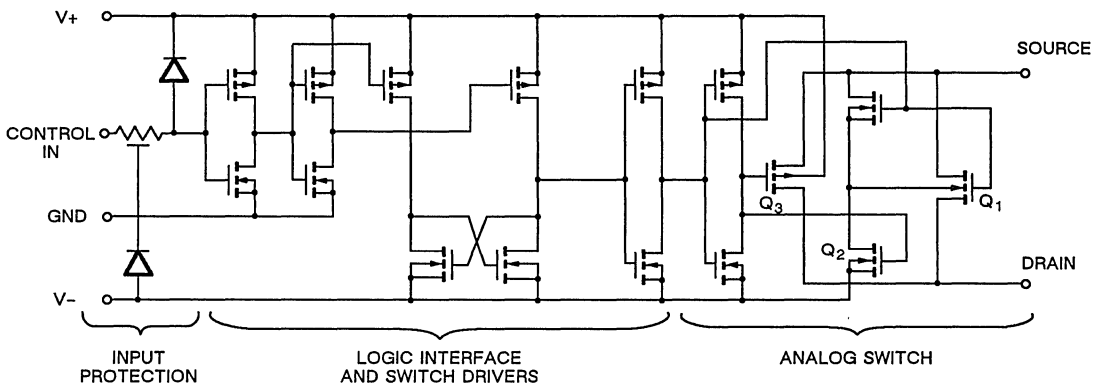


Figure 1. CMOS Schematic Diagram

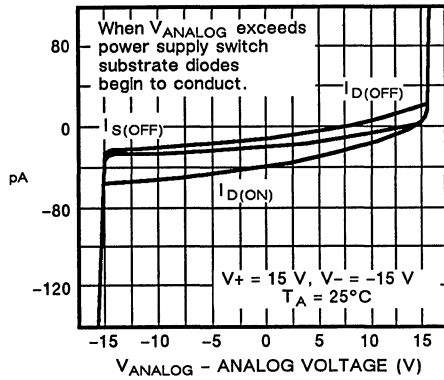


Figure 3. DG308A:  $I_{D(OFF)}$  &  $I_{D(ON)}$  vs.  $V_D$

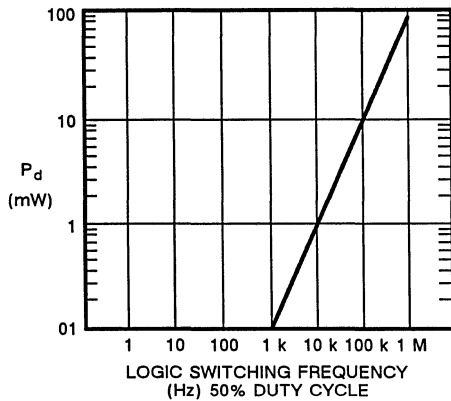


Figure 4. DG308A: Device Power Dissipation vs. Switching Frequency

Only residual leakage current flows when the circuit is either ON or OFF resulting in a power dissipation of less than 10 mW. However, as the switch toggles,

the power consumption increases in proportion to the increasing toggle frequency. Figure 4 shows the increase in power dissipation as toggling rate increases.

The actual switching time to turn ON ( $t_{ON}$ ) and turn OFF ( $t_{OFF}$ ) the switch consists of two distinct intervals: propagation delay and switch actuation. During the propagation delay interval, the CMOS logic input control signal amplifies, level shifts and begins to drive the output FET switch contacts. Switch actuation occurs rapidly as current through the switch begins or is interrupted generally occurring within 20% of the total switching time (see Figure 5). To a first approximation the turn ON time ( $t_{ON}$ ) is independent of the external circuit characteristics; however, turn OFF time ( $t_{OFF}$ ) depends on external circuit time constants. The (90% - 10%) settling time portion of switch turn off calculates as:

$$t_{\text{settling}} = 2.2 R_L [C_L + C_{D(OFF)}]$$

from 90% to 10% of  $V_O$  (see Figure 6). For the load conditions  $R_L = 1 \text{ k}\Omega$  and  $C_L = 35 \text{ pF}$ :

$$t_{\text{settling}} = 2.2 \times 1 \text{ k}\Omega \times (35 + 8) \text{ pF} = 95 \text{ ns}$$

In order to minimize the external loading effects on the  $t_{OFF}$  parameter, the DG308A specification measures between 50% of the logic control input and 90% of the output voltage  $V_O$  (Figure 5), thus only a portion of the settling time (70% of one time constant) is included in the  $t_{OFF}$  measurement. The additional settling time to the 50% point of  $V_O$  is 29 ns.

The turn ON time exceeds the turn OFF time over the full temperature and analog signal range by design. This approach results in guaranteed break-before-make switch operation in multiplexing applications.

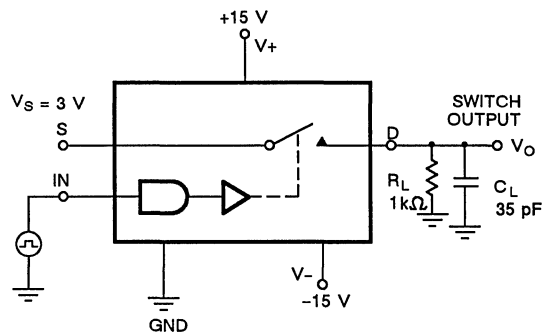
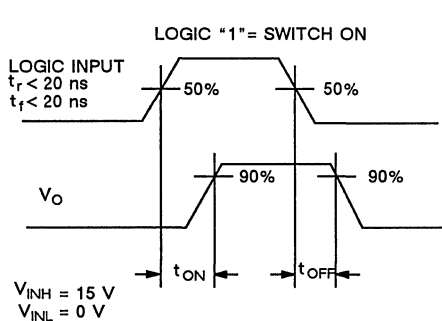


Figure 5. Switching Time Test Circuit

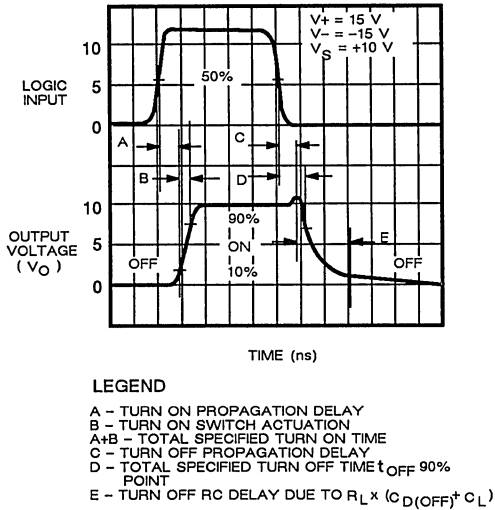


Figure 6. Switching Time

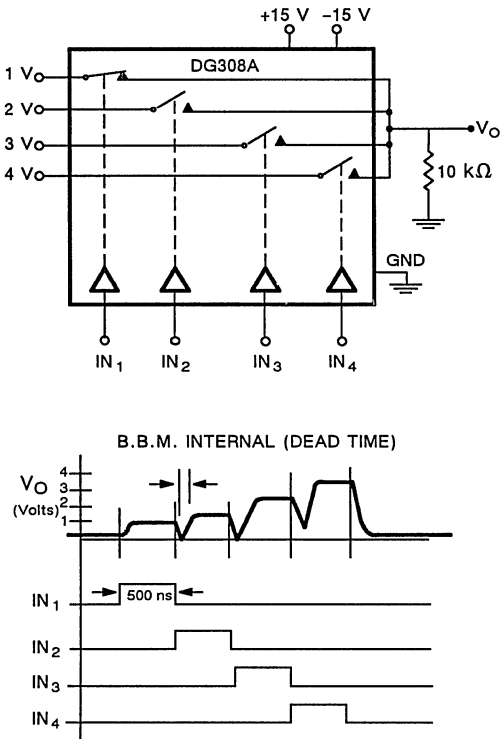
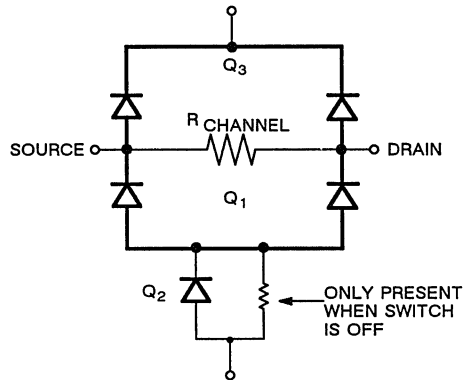


Figure 7. Four Channel Analog Multiplexer

**A Four Channel Analog Multiplexer:**

The four channel input multiplexer (Figure 7) displays the characteristic dead time achievable between channel selections resulting from  $t_{ON}$  being longer than  $t_{OFF}$ . This desirable dead time (break-before-make operation) prevents transducer signal sources from being momentarily shorted together during channel selection.

While looking at multiplexing applications of the quad switch array, a few important comments apply to signals occurring outside of the normal analog signal range of  $V+$  to  $V-$ . Often analog multiplexers receive their input signals from sources located far away. The signal sources sometimes pickup transient signals which exceed the  $V+$  and  $V-$  power rails. Under this condition the DG308A acts as a voltage clamp which can shunt transients up to 30 mA to the  $V+$  or  $V-$  power supplies. Figure 8 gives a working model of the transient clamping diodes during both switch ON and OFF states. Remember, the DG308A is constructed with a latch proof CMOS process (Reference 1).



$R_{CHANNEL} = 100 \Omega$  Max when  $IN_x = "1"$   
 $R_{CHANNEL} = 100 > 1000$  Meg Ohm when  $IN_x = "0"$

Figure 8. Typical Single Channel Overvoltage Model

When transient signals exceed the capability of the DG308A's clamping diodes, external protection circuits are required. One of the most often used and effective protection circuits are clamped series input resistors (Figure 9). This circuit has some important subtleties worth mentioning. First, the series resistor combined with the switch input capacitance of 7 pF

provides a low pass filter action that rapidly attenuates very large fast transient voltages e.g., electrostatic discharge. Second, the series connection of diodes (Zeners) tends to balance the individual leakage currents which could become a serious problem when the circuit operates at high ambient temperatures. Diode leakage current doubles with every 10°C increase in temperature. The diode leakage current flowing in the signal path generates undesirable temperature sensitive offset voltages. These offsets cause problems with low level voltage switching applications, e.g. thermocouples. The Zener diodes perform the initial voltage clamping of a transient signal. It turns out that very fast transients, like ESD, are more effectively clamped by zeners than by forward biased diodes. Regarding placement of 8-bit and 12-bit A/D converters (0.2% and 0.01%), let's look at the accuracies attainable in programmable gain amplifiers.

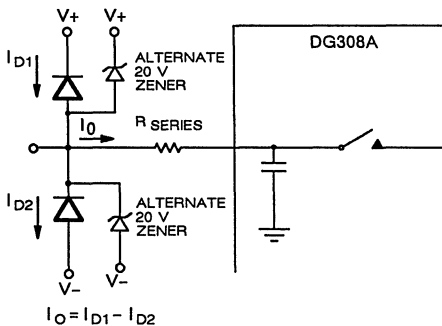


Figure 9. Series Resistance Diode Clamped Overtvoltage Protection Circuit

Figure 11 shows a common switchable gain amplifier. This circuit has two gain states X5 and X50. If the analog switch had 0 Ω ON resistance ( $r_{DS(ON)}$ ), the given values of  $R_{f1}$ ,  $R_{f2}$  and  $R_1$  would produce the circuit gains of X5 when switch 2 was closed and X50 when switch 2 was open. The  $r_{DS(ON)}$  of the analog switch produces a gain error of 0.19%.

Actual switch gain calculation:  $r_{DS(ON)} = 100 \Omega$

$$A_V(X50) = \frac{R_{f1}}{R_1 + r_{DS(ON)}} + 1 = \frac{2450K}{50K + 100} + 1$$

$$= 49.9021$$

$$(X50) \text{ Gain Error} = \frac{(50-49.9)100}{50} = 0.2\% \text{ error}$$

$$A_V(X5) = \frac{R_{f1} / [R_{f2} + r_{DS(ON)}]}{R_1 + r_{DS(ON)}} + 1$$

$$= \frac{2450K / (217.78K + 100)}{5K + 100} = 4.99374$$

$$(X5) \text{ Gain Error} = \frac{5-4.99374}{5} \times 100 = 0.12 \text{ error}$$

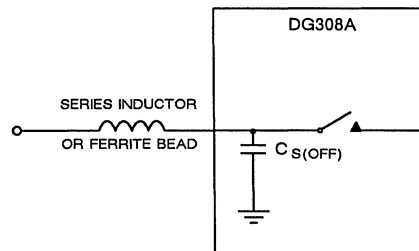


Figure 10. Series Inductance Overtvoltage Protection Circuit

The low  $r_{DS(ON)}$  of the DG308A allows us to meet the 0.2% accuracy requirement imposed by the 8-bit A/D converter. Note that the percent error in gain accuracy is larger in the high gain (X50) rather than the low gain mode (X5).

The circuit of Figure 11 also has a dummy switch (SW1), which is always closed to provide some temperature tracking between the feedback resistors and input resistors. The  $r_{DS(ON)}$  of most analog switches has a positive temperature coefficient of 0.7% per degree centigrade. The  $r_{DS(ON)}$  will double if the temperature increases by 140°C.

In order to achieve the 0.01% accuracy requirement of a 12-bit A/D converter measuring system, the programmable gain circuit can be rearranged which almost eliminates the  $r_{DS(ON)}$  gain sensitivity. The circuit of Figure 12 achieves the required 0.01% gain



accuracy by placing the analog switch in series with the high input impedance of the FET op amp. In this circuit gain accuracy is determined by the resistor ratios, which can be chosen to properly track over the operating temperature range. It turns out the weak component of the circuit (Figure 12) becomes  $r_{DS(ON)}$  the op amp due to its input offset and CMR capability.

The circuit (Figure 12) also provides high input impedance and non-inverting operation. Additionally, using suitable wide band-width clamping Zener diodes between the series resistor and analog switch is not preferred since this would increase offset error generation due to the differential diode leakage flowing across the series resistor causing an  $I_{xr}$  offset error voltage.

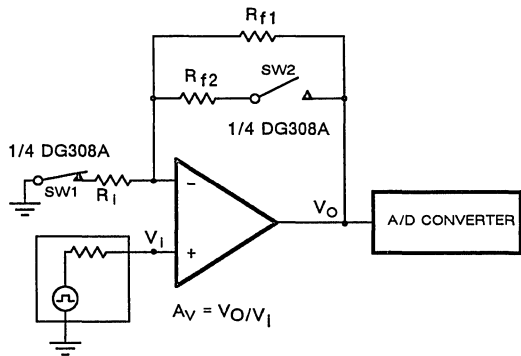


Figure 11. Programmable Gain Amplifier

One disadvantage of the series input resistor protection circuit, in Figure 9, is the increased total resistance in the signal path which will increase system noise pickup, thus degrading effective transducer signal-to-noise ratio. An alternate fast transient protection circuit shown in Figure 10 does not increase total transducer resistance but still dampens fast transients. Taking advantage of the basic properties of lossy inductance, the ferrite bead allows signal frequencies generally close to D.C. (e.g. thermal couple) to pass through the system to the amplifier. The low frequency resistance of the ferrite bead surrounding the signal lead is very low which minimizes the additional resistive contribution to the transducer signal-to-noise ratio. The high frequency operation of the series lossy inductance combined with the input

capacitance of the analog switch provide a very effective damped two-pole low-pass filter. Basically, the inductor blocks the high voltage transient from passing to the analog switch. Additionally, the lagging current passing through the inductor to a first approximation integrates according to:

$$i_L = \text{transient time } V_{IN} - V_{switch} \approx 0 \text{ dt.}$$

So far we have been discussing the transient handling capability of the DG308A at the source or drain terminals. The logic inputs ( $IN_X$ ) have protection circuits shown in Figure 1. The protection circuit will stand off input voltage transients going positive to 22 V or negative to 44 V with respect to the  $V+$  power supply terminal. The power supply terminals will handle 44 V transients from  $V+$  to  $V-$ , which translates to 22 V for a dual supply application.

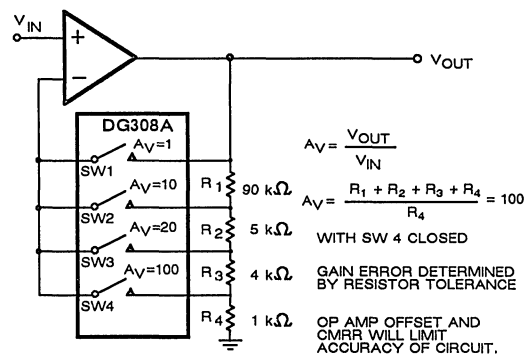


Figure 12. Precision Weighted Resistor Programmable Gain Amplifier

## Important Applications Of The DG308A

The quad single-pole single-throw DG308A is a generalized building block found in several types of electronic test equipment. Some of the electronic equipment using analog switches include intelligent instruments, computer peripheral equipment, and automatic test equipment.

We will be looking at some of the basic circuits found in these applications including programmable gain amplifiers, peak detection, velocity integrators, remote switching, and programmable filters.

## Programmable Gain Circuits:

One of the most important analog circuits found in intelligent instruments and automatic test equipment are the programmable amplifiers and programmable attenuators. The programmable gain amplifier scales the measured signal into the full-scale range of the instruments analog-to-digital converter. Consequently, the programmable gain amplifier should have better accuracy than one-half of the least significant bit of the system's A/D converter. For an 8-bit A/D converter, 1/2 LSB represents 0.2% of full-scale.

For a 12-bit A/D converter, 1/2 LSB represents 0.01% of full-scale. Keeping in mind the accuracy requirements, op amp frequency response and settling time can be easily optimized. In this circuit design it was not necessary to make  $r_{DS(ON)}$  small compared

to the gain setting resistor values. Consequently, the gain setting resistor values can be reduced until the op amp can no longer drive the total resistive load. Constructing Figure 13 (only resistor values change from Figure 12) proved that not only settling time improved, but so was the magnitude of the ever present charge injection of the analog switch. Figure 14a to 14b shows the improvement in settling time when the total divider resistance is decreased by an order of magnitude. We quantify the magnitude of charge injection originating from the analog switch in terms of Q (pico-Coulombs). The DG308A injects approximately 35 pC of charge during every switch transition.

If the amplitude of the charge injection caused transients is still objectionable, the addition of an extra buffer amplifier results in the charge compensated circuit of Figure 15.

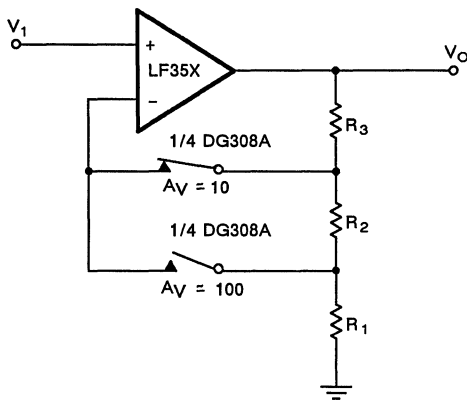


Figure 13. Precision Programmable Amplifier

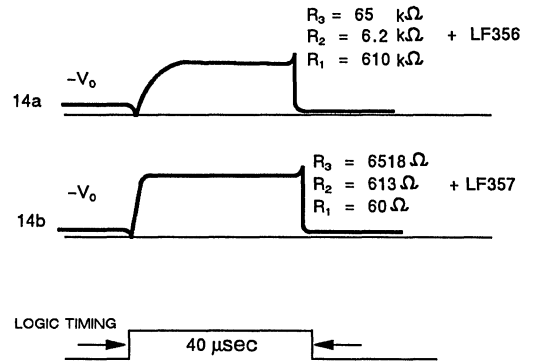


Figure 14. Logic Timing

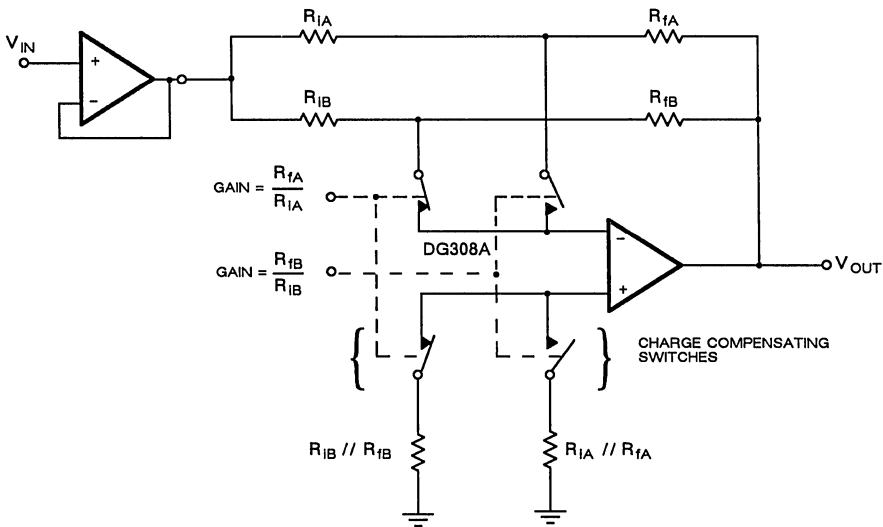


Figure 15. Charge Compensated Inverting Programmable Gain Amplifier

**Peak Detector Applications:**

The basic peak detector circuit shown in Figure 16 utilizes the DG308A as a zero-offset reset switch. That is, no voltage will be left on the capacitor after reset. A maximum of  $\pm 10$  V may be discharged directly by the DG308A since it has a maximum switch current rating of 100 mA for 1 ms. Capacitor values up to 10  $\mu$ F maximum are allowed. This peak detector circuit is commonly found in computer disk and tape drive equipment.

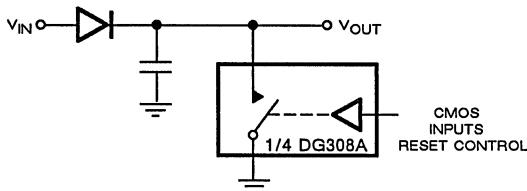
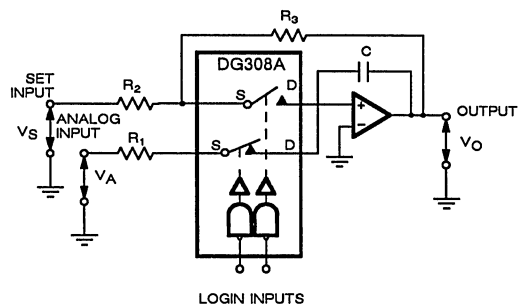


Figure 16. Basic Peak Detector

**Integrators:**

Velocity integration used in motor head positioning circuits takes advantage of settable time integrators such as Figure 17. This circuit results in precise linear integration since the set point is determined by the set voltage and  $R_3/R_2$  ratio.



- FEATURES**
- MINIMAL INTEGRATION ERROR DUE TO LOW CHARGE FEED THROUGH
  - LOW LEAKAGE

Figure 17. Three Mode Integrator

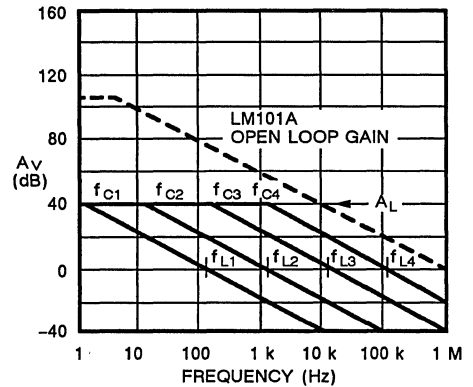
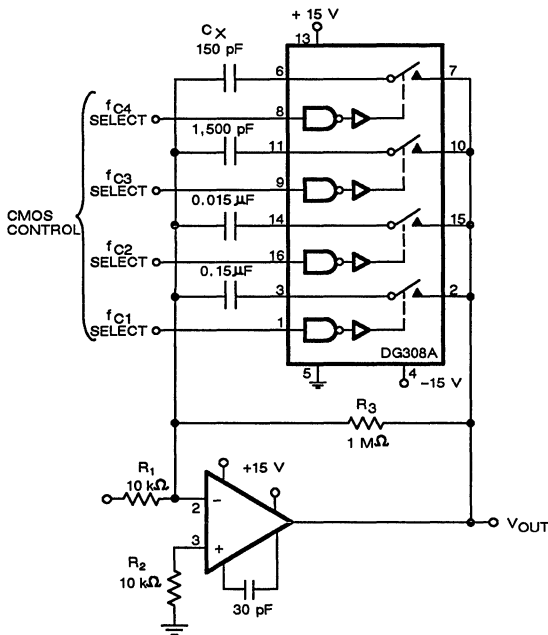
## Programmable Filters:

An active filter is sometimes used at the front end of programmable test equipment. The first order active filter shown in Figure 18 can digitally select four different break frequencies. In order to minimize the effect of switch capacitance on frequency response, the DG308A is located between the low output impedance of the op amp and the frequency determining feedback capacitors.

The  $100 \Omega r_{DS(ON)}$  of the DG308A results in an outside of selected frequency range maximum attenuation of 40 dB.

## REFERENCE:

1. *Analog Switches and Their Applications*, June 1980, AN75-1, pg. 7-57.



$$A_L \text{ (VOLTAGE GAIN BELOW BREAK FREQUENCY)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (BREAK FREQUENCY)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (UTILITY GAIN FREQUENCY)} = \frac{1}{2\pi R C_X}$$

$$\text{MAX ATTENUATION} = \frac{r_{DS(ON)}}{10 \text{ k}} = -40 \text{ dB}$$

Figure 18. Active Low Pass Filter with Digitally Selected Break Frequency

# FUNCTION/APPLICATION OF THE L161 MICROPOWER COMPARATOR

## INTRODUCTION

The L161 is a monolithic quad micropower comparator with an external control for varying its AC and DC characteristics. The variation of a single programming resistor will simultaneously alter parameters such as supply current, input bias current, slew rate, output drive capability, and gain. By making this resistor large, operation at very small supply current levels and power dissipations – typically in the low microwatt region – is possible. The L161 is therefore ideal for systems requiring minimum power drain, such as battery-powered instrumentation, aerospace systems, CMOS designs, and remote security systems.

## Description

The L161 is fabricated using standard bipolar processing. The circuit (Figure 1) is composed of five major blocks – four comparators and a common bias network.  $Q_1 - Q_6$  and  $D_1$  form a Darlington differential amplifier with double-to-single ended conversion.  $Q_6$  is a dual current source whose outputs are exactly twice the current flowing through  $Q_8$ . The collector current of  $Q_8$  is a function of the current supplied externally to  $Q_9 - Q_{10}$ , which in turn is known as the set current or  $I_{SET}$ . This set current is established by a resistor connected between the  $I_{SET}$  terminal and a voltage source, most commonly the

positive supply.  $Q_{11}$  prevents excessive current from flowing through  $Q_9$  and  $Q_{10}$  in the event the  $I_{SET}$  terminal is shorted to the positive supply; it has no effect on circuit operation under normal conditions.

The set current can be expressed as:

$$I_{SET} = \frac{[(+V) - (2 V_{BE}) - (-V)]}{R_{SET}} \quad (1)$$

where  $+V$  is the voltage to which the control resistor is connected,  $-V$  is the negative supply voltage,  $V_{BE}$  is the base emitter drop of  $Q_9$  or  $Q_{10}$  (about 0.7 V), and  $R_{SET}$  is the value of the external control resistor or set resistor. Equation 1 is simply a derivative of Ohms law. There is also an analytical relationship between  $I_{SET}$  and the total supply current:

$$\begin{aligned} I_{SUPPLY} &= [ I_{SET} \text{ (current sourced by } Q_6 \text{ to } Q_8) \\ &\quad + 2 I_{SET} \text{ (current sourced to the differential amplifier by } Q_6) \\ &\quad + 2 I_{SET} \text{ (current sourced to the comparator output by } Q_6) \\ &\quad \times 4 \text{ (the total numbers of comparators)} \\ &\quad + I_{SET} \text{ (current sourced through } Q_{11}, \\ &\quad Q_{10}, \text{ and } Q_9 \text{ to } -V) \\ &= [ I_{SET} + 2 I_{SET} + 2 I_{SET} ] \times 4 + I_{SET} \\ &= 21 I_{SET} \end{aligned}$$

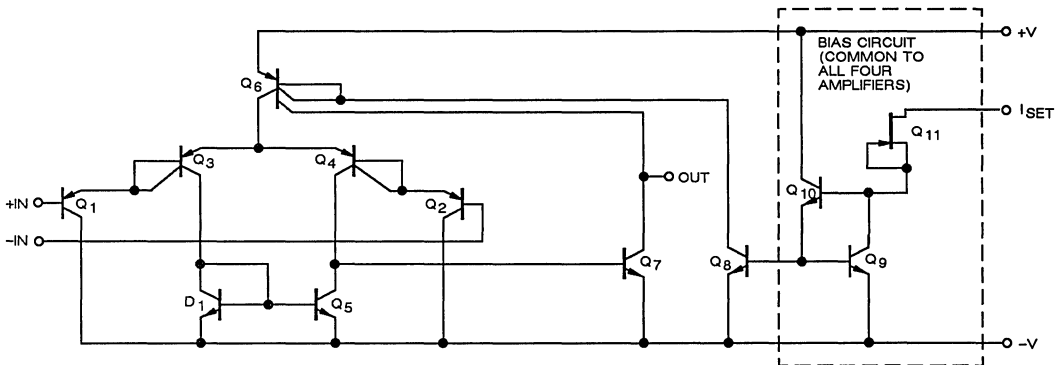


Figure 1. Schematic of One Channel of the L161 Plus the Common Bias Network

The output current pulldown capability ( $I_{OL}$ ) of the L161 is about 2 orders of magnitude greater than the high output drive current, ( $I_{OH}$ ), which allows wire-ORing the outputs.  $I_{OH}$  is simply the current sourced by  $Q_6$ :

$$I_{OH} = 2 \times I_{SET} \quad (3)$$

$I_{OL}$  is found by multiplying the current sourced by the collector of  $Q_6$  by the gain of  $Q_7$ :

$$I_{OL} = \beta(Q_7) \times 2 I_{SET} \quad (4)$$

The beta of  $Q_7$  is about 75-150.

Input bias current is a function of the betas of input devices  $Q_1$ - $Q_2$  and  $I_{SET}$ . This is difficult to express analytically because  $\beta$  varies greatly with both processing and collector current; however it is roughly proportional to the set current and can easily be determined experimentally (see Figure 2).

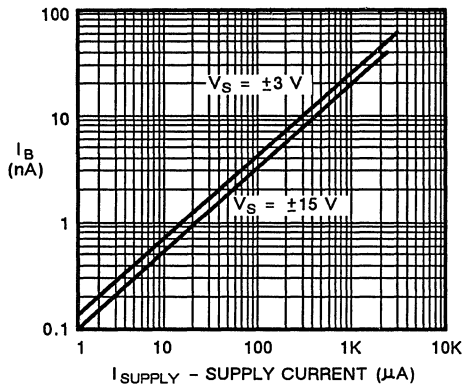


Figure 2. Input Bias Current vs. Supply Current

Gain varies logarithmically with changes in supply voltage and linearly with changes in set current. Primary causes are the decrease in output impedance of  $Q_7$  with decreasing supply voltage and an increase in transistor betas with increasing set current. Other AC parameters such as slew rate and transition time are also affected by set current; however current dependent parameters such as beta and chip capacitances make mathematical expressions imprecise. These relationships have been determined empirically and are presented in Figures 3 and 4.

The designer's ability to program the key parameters of the L161 enables him to program just enough supply current to meet his design objectives. This coupled with the L161's performance using only microwatts of power makes it ideal for any micropower or battery-powered system, as well as a replacement for existing higher power comparators. The following applications illustrate the flexibility and unique capabilities of the L161.

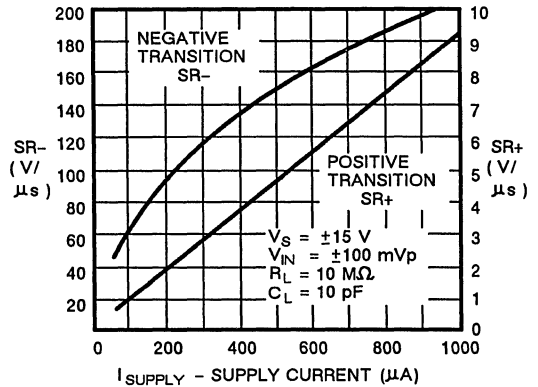


Figure 3. Slew Rate vs. Supply Current

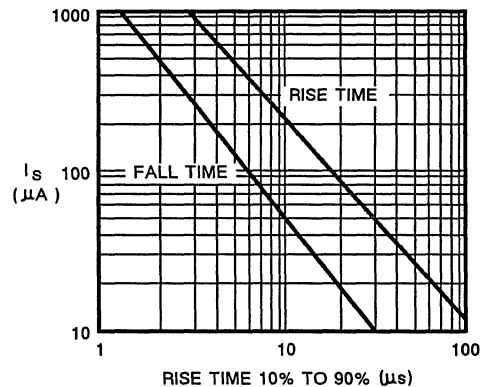
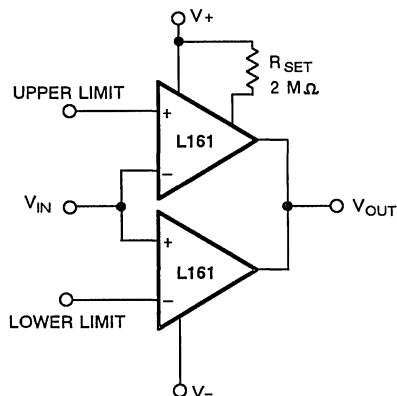


Figure 4. Rise and Fall Times vs. Supply Current With One CMOS Load

## Micropower Applications

A classic comparator application is the double-ended limit detector or window comparator shown in Figure 5.  $V_{OUT}$  is high whenever the input voltage is within the two limits. Because the Darlington input stage extends the common-mode input range below

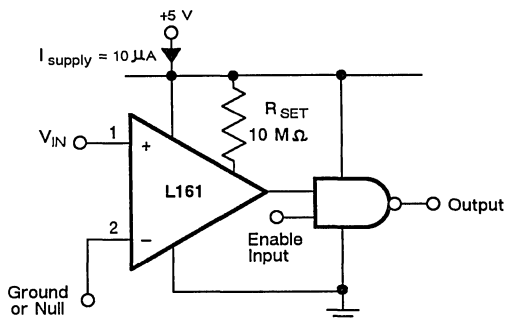
the negative supply, the lower limit may be as low as  $-0.4\text{ V}$  with the  $V^-$  terminal at ground. A comparison about ground is therefore possible with only one supply.



**Figure 5.** Double-Ended Limit Comparator with Wire OR'd Outputs

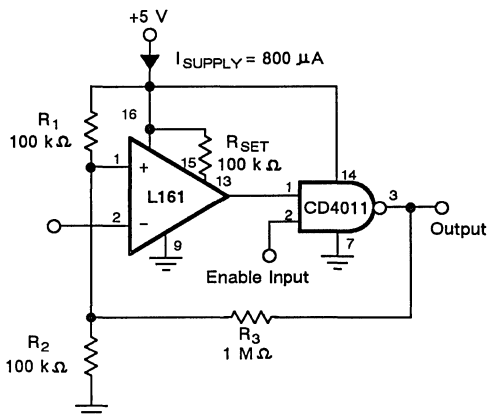
The L161 is especially suited for this application because of its wire-OR capability; low output on either comparator will pull both outputs to ground. For this example a supply current of  $90\ \mu\text{A}$  was chosen to provide a slew rate of about  $5\text{ V}/\mu\text{s}$ . If greater output drive current or decreased transition times are needed, lower  $R_{\text{SET}}$ .

The zero crossing detector shown in Figure 6 is useful in sine wave squaring circuits and A/D converters. This circuit also takes advantage of the L161's ability to detect signals below its negative rail, so only a positive supply is needed. The positive input may either be grounded or connected to a nulling voltage which cancels input offsets and enables accuracy to within microvolts of ground. The CMOS output will switch to within a few millivolts of either rail for an input voltage change of less than  $200\ \mu\text{s}$ .



**Figure 6.** Zero Crossing Detector

The circuit in Figure 6 may be modified to produce a line receiver (Figure 7). The trip point is set half way between the supplies by  $R_1$  and  $R_2$ ;  $R_3$  provides over  $200\text{ mV}$  of hysteresis to increase noise immunity. With  $800\ \mu\text{A}$  of quiescent supply current the maximum frequency of operation is about  $300\text{ kHz}$ . If response to TTL levels is desired, change  $R_2$  to  $39\text{ k}\Omega$ . The trip point is now centered at  $1.4\text{ V}$ .



**Figure 7.** CMOS Line Receiver

Mating the L161 with CMOS logic is natural since the L161 draws microamps from a single  $5\text{ V}$  supply. However, the L161 will also drive TTL when a suitable pull-up resistor is provided. Figure 8 shows this combination. Total power drain of the circuit is much heavier due to the presence of the 7401. Propagation delays through the circuit are about  $1\ \mu\text{s}$ .

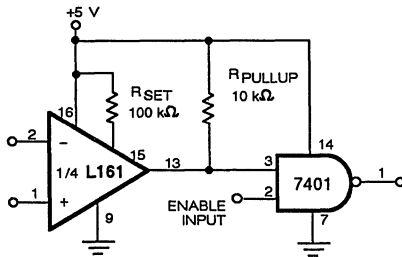


Figure 8. Driving TTL

In many situations further power savings can be achieved by reducing or eliminating  $I_{SET}$  during part of the operating time. This is desirable, for example, when a system is multiplexed at a low duty cycle. The L161 may be strobed off completely by reducing  $I_{SET}$  to zero as shown in Figure 9. The 3N163 P-channel MOSFET is OFF when the strobe input is high so no set current flows into the L161. For a low strobe input, the 3N163 turns ON, pulling  $R_{SET}$  to the positive supply and turning on the comparator. The drain-source resistance of the 3N163 (250  $\Omega$ ) is negligible compared to  $R_{SET}$ . If the negative supply terminal of the L161 is returned to ground, the 3N163 may be eliminated and  $R_{SET}$  connected directly to the output of a CMOS gate. When the L161 is strobed OFF, its outputs assume a high-impedance state; this "three state" operation facilitates the connection of many outputs to a single bus.

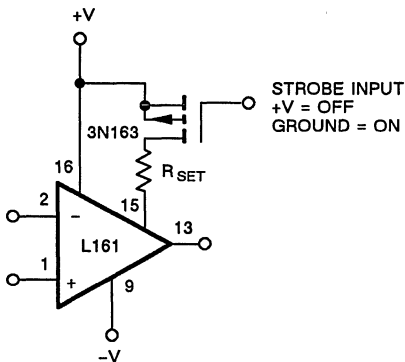


Figure 9. Strobing the L161 ON and OFF

The L161 will switch itself into a standby mode if one of its outputs is connected to the  $I_{SET}$  terminal as illustrated in Figure 10.

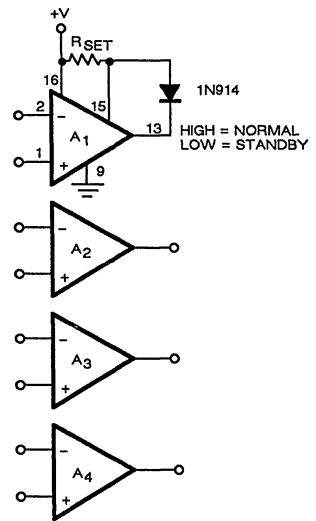


Figure 10. Switching the L161 to a Low Current "Standby" Mode

The diode blocks current when the output of  $A_1$  is HIGH, and operation of the other three comparators is normal. When the output goes low, however, the IN914 conducts most of  $I_{SET}$  to the negative supply.  $I_{OL}$  is therefore nearly equal to  $I_{RSET}$ , and (from Equations 2 and 4),

$$I_{SUPPLY} = 21 I_{SET} \text{ (actual)} \quad (5)$$

$$= \frac{21 I_{OL}}{2B} = \frac{I_{SET}}{10}$$

if a  $\beta$  of 105 is assumed. Equation (5) states that the supply current of the L161 is reduced from  $21 \times I_{R1}$  (normal operation) to  $I_{R1}/10$ , a factor of 210 (or twice whatever  $\beta$  of Q7 is). Total supply drain is simply the current through  $R_{SET}$ . This circuit has an important advantage over the previous strobe circuit: even though the L161 is operating at a greatly reduced supply current, it is still ON and continues to function. If a lesser reduction in supply current is desired, connect a resistor in series with the diode.

Figure 11 shows an L161 low battery indicator which flashes an LED when the battery voltage drops below a certain threshold. The 2N4274 emitter-base junction serves as a zener which establishes about 6 V on the L161's positive input. As the battery dies, the voltage at the negative input drops more quickly; when the low battery threshold (typically 7.5 V) is



reached, the L161 output goes HIGH. This turns on the FETlington, which discharges  $C_1$  through the LED. The interval between flashes is roughly equal to  $R_1C_1$ , which in this case is 2 seconds. By flashing the LED at a very low duty cycle, this circuit gives a low battery warning with only 10  $\mu$ A average power drain.

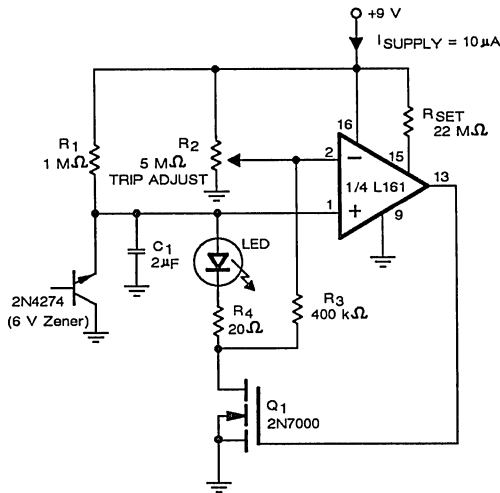


Figure 11. A Low Battery Indicator

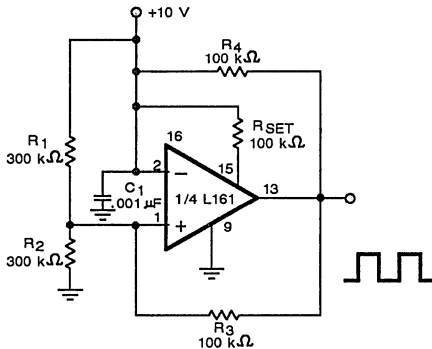


Figure 12. Squarewave Oscillator

**Waveform Generators**

Figure 12 is a square wave generator which is operable to over 100 kHz while Figure 13 depicts the typical frequency vs capacitance performance of the circuit. The low frequency limit is determined only by the size of  $C_1$ . Frequency is constant for supply volt-

ages down to +5 V; below that the charging rate of  $C_1$  in the positive direction is determined by  $I_{OH}$  and not  $R_4$ . For lower voltage operation, increase  $R_4$  (and lower  $C$  accordingly) or decrease  $R_{SET}$ .

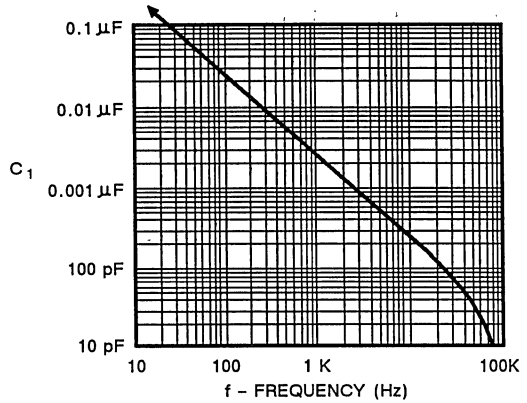


Figure 13. Frequency vs. the Value of for the Squarewave Oscillator

To generate pulses the positive and negative charging rates of the capacitor must be unequal. Figure 14 illustrates a method using diodes and unequal resistors. The duty cycle of the output pulse is equal to  $R_4/(R_4 + R_5) \times 100\%$ . For duty cycles of more than 50%,  $D_1$  can be eliminated and the duty cycle set according to the formula,

$$\text{duty cycle} = \frac{R_4 + R_5}{R_4 + 2R_5} \quad (6)$$

A similar analysis could be made for eliminating  $D_2$  when  $t < 50\%$ . Figure 13 may be used to determine frequency ( $= 1/\text{period}$ ) if  $1/2 (R_4 + R_5) = 100 \text{ k}\Omega$ .

The versatile two phase clock generator of Figure 15 uses two L161's to generate pulses of adjustable widths and phase relationships.  $IC_1$  is the heart of a ramp generator which feeds two variable window comparators formed by  $IC_{2A} - IC_{2B}$  and  $IC_{2C} - IC_{2D}$  respectively. The voltage on pin 1 of  $IC_{2A}$  ramps up as  $C_1$  charges through  $R_1$ . When this voltage exceeds approximately 5 V (the potential on pin 2 of  $IC_{1A}$ ), the output of  $IC_{1A}$  goes HIGH, forcing  $IC_{1B}$  and  $IC_{1C}$  LOW.  $C_1$  is quickly discharged by  $I_{OL}$  of  $IC_{1B}$ , and the comparators reset to their normal state ( $IC_{1A}$  LOW,  $IC_{1B}$  and  $IC_{1C}$  HIGH).

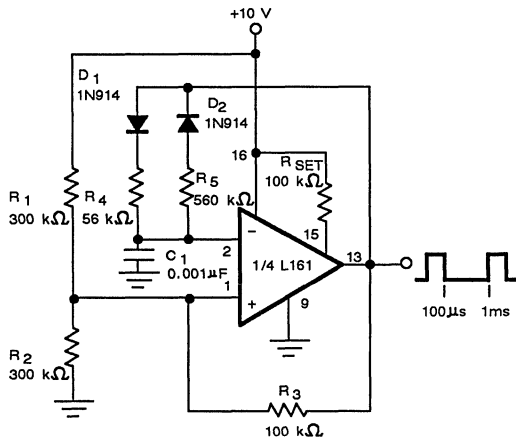


Figure 14. Pulse Generator

As the ramp rises, its value passes through the two windows defined by the differences between the voltages on  $R_4$  and  $R_5$  in the case of  $\phi_1$ , and  $R_6 - R_7$  for  $\phi_2$ .  $IC_2$  is set for a supply current of  $20 \mu A$ ; at this level its slew rate is too slow for the window comparators to respond to the fast negative transition of the ramp. By adjusting  $R_4 - R_6$ ,  $\phi_1$  and  $\phi_2$  may be set for any width up to the period of the ramp (Figure 16 contains typical waveforms). If longer pulse lengths are needed, increase  $C_1$  since  $t(\text{ramp}) = 0.7 R_1 C_1$  (neglecting  $I_{OH}$  of  $IC_{1B}$  and  $IC_{1C}$ ). A higher rep rate is obtained by lowering  $C_1$  but  $R_{S1}$  and  $R_{S2}$  may also need to be lowered to insure  $IC_1$  and  $IC_2$  have adequate slew rates.

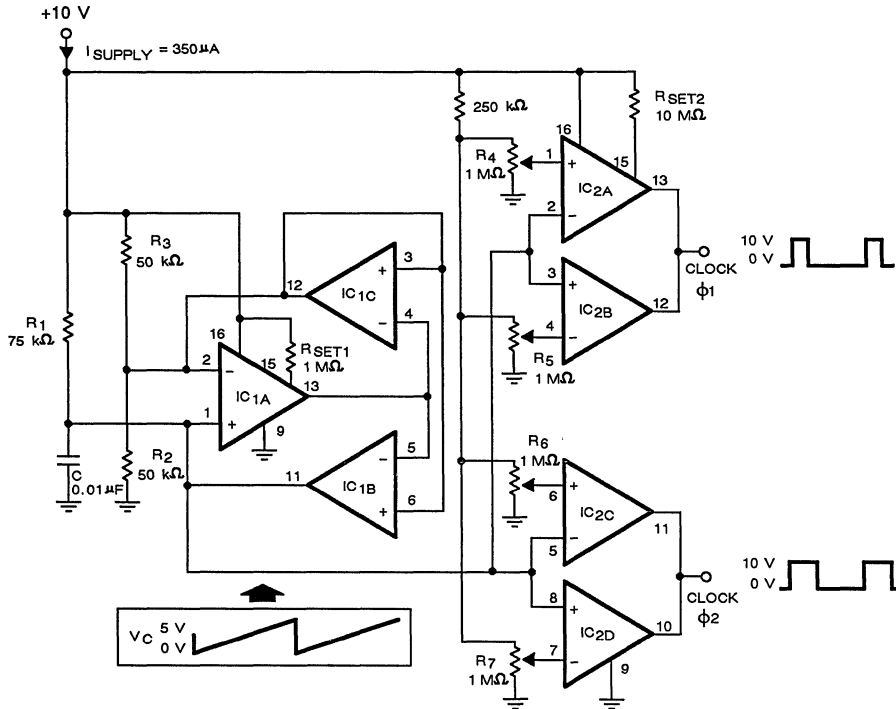


Figure 15. A Versatile 2φ Pulse Generator

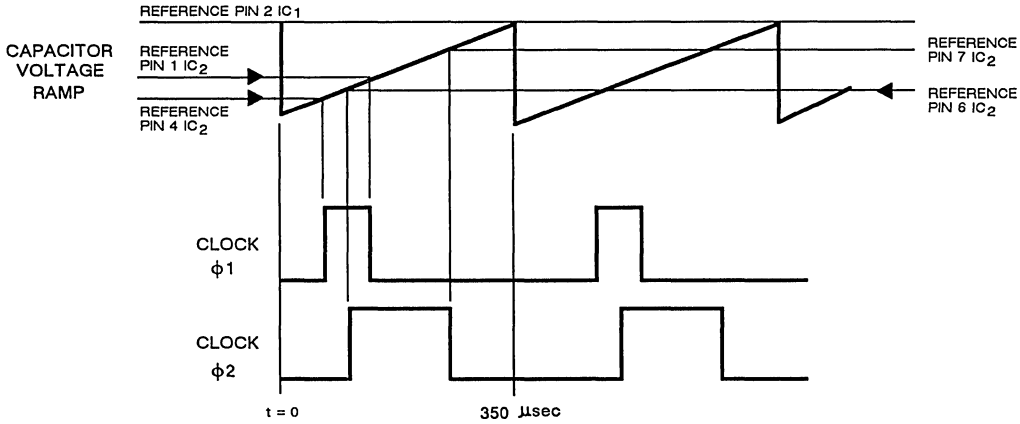


Figure 16. Waveforms of the Two Phase Pulse Generator

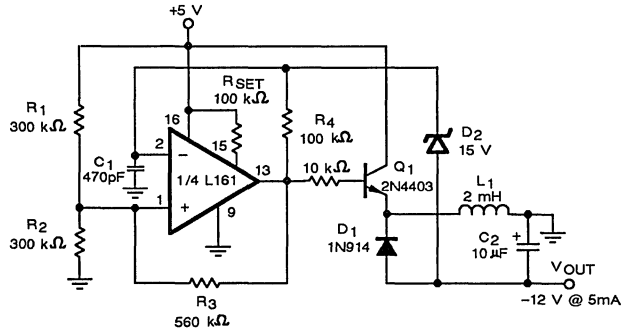


Figure 17. A Regulated DC to DC Converter

Figure 17 is a low power DC to DC converter obtained by adding a flyback circuit to the square wave oscillator. Operating frequency is 20 kHz to minimize the size of  $L_1$  and  $C_2$ . Regulation is achieved by zener diode  $D_2$ ; when the output is less than  $-12$  V, the zener breaks down and discharges  $C_1$  slightly which reduces the duty cycle of the oscillator below 50%. Maximum current available before the converter drops out of regulation is 5.5 mA at an overall efficiency of 71%. With no load the converter draws 590  $\mu$ A.

### Operational Amplifiers

While designed primarily as a comparator, the L161 will perform as an op-amp if proper compensation is applied. Figure 18 is a simple gain of 100 amplifier with a gain-bandwidth product of 20 MHz ! The primary limitation in the performance is the low slew rate (0.3 V/ $\mu$ s) imposed by  $I_{OH}$  charging  $C_{COMP}$ . The effects of slew rate and compensation are shown in Figure 19.

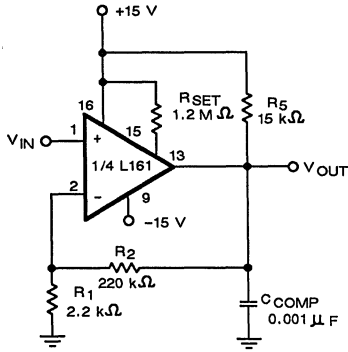


Figure 18. The L161 as an X100 Operational Amplifier

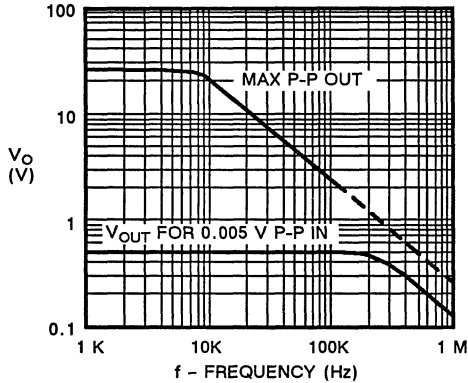


Figure 19. Frequency Response and Maximum Output for the X 100 Op Amp

A lower gain amplifier requires a larger  $C_{COMP}$ , which in turn further reduces slew rate. For this reason it may actually be advantageous in certain cases to lower the gain by placing a resistive divider at the input rather than raising  $R_1$ . Figure 20 shows a 700 microwatt X10 op amp whose slew rate is  $0.02 \text{ V}/\mu\text{s}$  and is 3 dB down at 100 kHz.

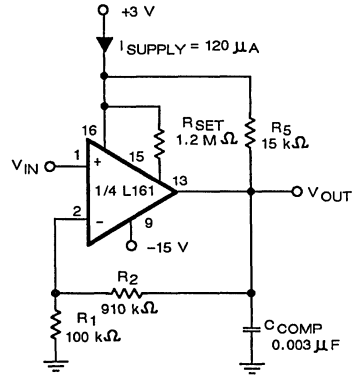


Figure 20. A Micropower X10 Op Amp

# DG300A Series Analog Switch Applications

Thomas J. Mroz  
Revised December 1984

## INTRODUCTION

To round out its analog switch line, Siliconix has introduced the DG300A to DG307A analog switch family. The DG300A to DG307A switches were designed to approach the industry standard DG180 family of JFET switches in performance while keeping the economy and low power of CMOS circuitry, and offer fast switching (typically < 150 ns) and low ON resistance (< 50  $\Omega$ ). Four switch functions, (dual SPST, SPDT, dual DPST, dual SPDT) are offered with TTL or CMOS compatible logic input options. The low ON resistance, fast switching speed and low power of these switches makes the DG300A family an excellent choice for sample and hold, digital-to-analog converters, and multiplexing elements as well as other applications requiring low offsets, fast charging of capacitors and fast switching of analog signals. The SPDT functions offer break-before-make action which aids in simplification of system design.

## DG300A Family Switch Structure

Figure 1 shows a partial schematic of a DG300A switch.

Device Q1 along with the Zener diode provide the input protection. This is accomplished by Q1 being turned off whenever the input voltage exceeds the positive supply ( $V_+$ ) and by the Zener breakdown whenever the input goes more negative than  $V_+ - V_{ZENER}$ . Q2 and Q3 form the first input buffer and are designed to set the proper input threshold. The DG300A to DG303A thresholds are typically between 1.5 and 2.5 V and are designed to interface with TTL gates employing pullups to +5 V. These switches can also be driven from CMOS gates using 5 to 15 V supplies. If 15 V CMOS drive is available, faster switching can be accomplished by using the CMOS input DG304A to DG307A switches.

DG304A to DG307A switch inputs have thresholds typically between 4 V and 6 V with  $\pm 15$  V supplies and are designed to interface with inputs switching between ground and the +15 V supply. Q4 through Q15 form additional buffers and create the necessary driving voltages for the switch devices, Q16 and Q19. Q17 and Q18 are referred to as being body snatchers, not because of midnight escapades, but because they connect the body of Q19 to either its source or the negative supply. This reduces the ON resistance and the OFF leakage of this device.

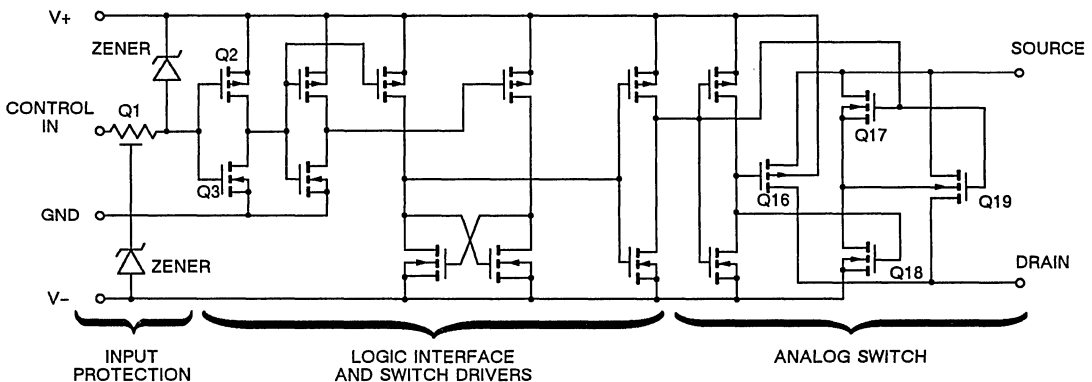


Figure 1.

## PERFORMANCE CHARACTERISTICS

### Switching Time

In measuring switching time it is important to remember that the turn-off time as seen at the load is highly dependent on the load time constant. The switching time test circuit is shown in Figure 2 below.

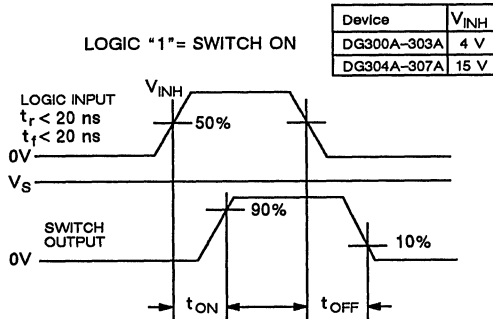


Figure 2. Switching Time Test Circuit

Turn-on time in the circuit shown in Figure 2 is governed primarily by the logic delay path and the  $r_{DS(ON)}$  of the switch. The  $r_{DS(ON)}$ ,  $C_{LOAD}$  time constant is normally shorter than the  $R_L C_L$  time constant. The two time constants are:

$$\frac{r_{DS(ON)} \times R_L}{r_{DS(ON)} + R_L} \times C_L \text{ for } t_{ON} \text{ and } R_L \times C_L \text{ for } t_{OFF}$$

These two time constants determine rise and fall times of the analog switch. When the switch is driving

a high impedance, high capacitance load such as that shown in Figure 3, which is the input of a summing amplifier having some noise filtering, it may be necessary to add a second switch (Figure 4) for rapid discharge of the filter capacitor thus preventing offsets from occurring at the summing amplifier output.

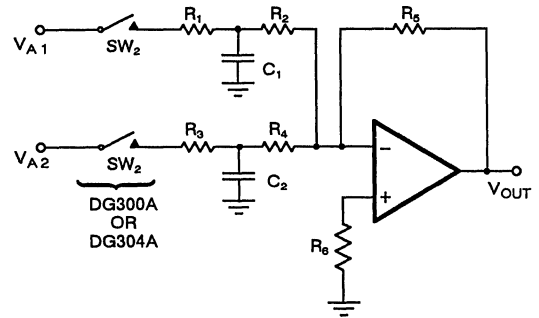


Figure 3. Summing Amplifier

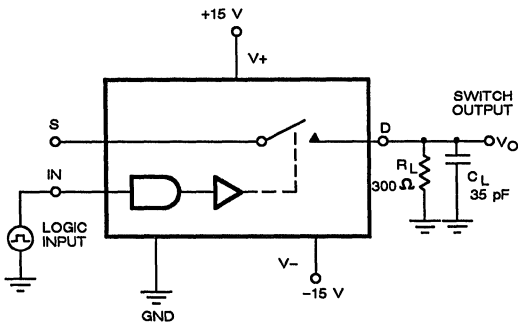


Figure 4. Improving Summing Amplifier

### Channel ON Resistance

Another important specification of an analog switch is the channel ON resistance,  $r_{DS(ON)}$ . The  $r_{DS(ON)}$  of the DG300A family of switches is typically below 40  $\Omega$  over the operating temperature range.

The two figures below show variations of  $r_{DS(ON)}$  with respect to temperature (Figure 5) and supply voltage applied to the switches (Figure 6).

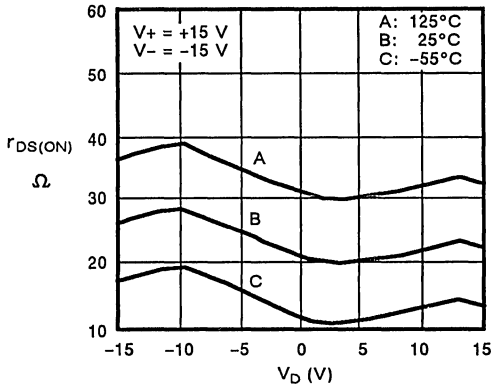


Figure 5.  $r_{DS(ON)}$  vs.  $V_D$  and Temperature

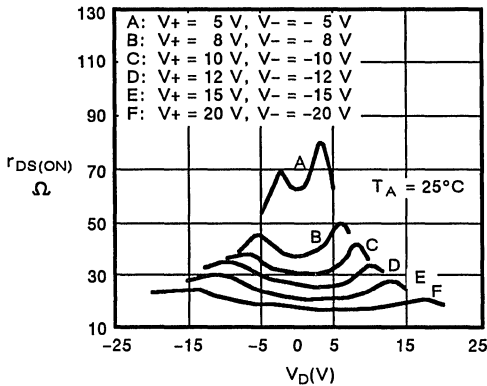


Figure 6.  $r_{DS(ON)}$  vs.  $V_D$  and Power Supply Voltage

As shown by Figure 5,  $r_{DS(ON)}$  increases as temperature increases. This is a typical FET characteristic due to the decreasing conductivity of silicon as temperature increases. This decrease in conductivity is due to the shortening of the mean free path seen by the majority carriers of the device. The change of switch resistance with respect to temperature is approximately  $0.1 \Omega/^\circ C$ .

Figure 6 also shows  $r_{DS(ON)}$  variations with respect to analog signal voltage as a function of supply voltages. Supply variations are important because the maximum gate drive available for the switch output

devices is determined by the supply voltages. Thus the change in  $r_{DS(ON)}$  is proportional to the change in supply voltage.

The variation of  $r_{DS(ON)}$  with respect to the analog voltage is due to the variation in the gate-source voltage of the "ON" switches as shown in Figure 7.

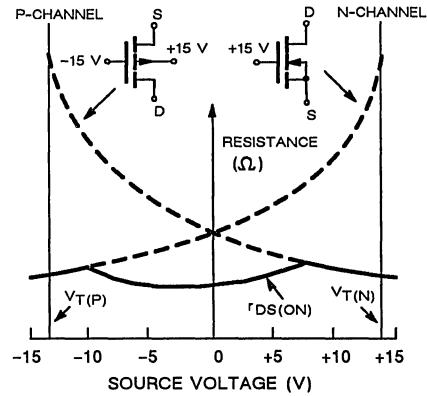


Figure 7. Resistance vs. Source Voltage of P-Channel and N-Channel FETs

In Figure 8, the complementary output pair (for illustrative purposes) is shown in a very basic schematic. When the switch is ON,  $G_1$  is tied to the negative supply and  $G_2$  is tied to the positive supply.  $V_{D1} = V_{S1} = V_{S2}$ . In order to understand the variation of  $r_{DS(ON)}$  with respect to analog voltage, the complementary pair will be broken apart and the  $r_{DS(ON)}$  of each device with respect to analog voltage examined.

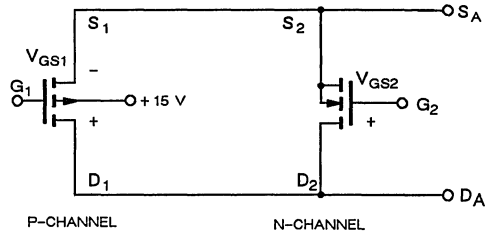


Figure 8. Complementary Output Devices (Simplified)

As Figure 7 indicates, the N-channel device with its gate tied to +15 V, begins to turn ON as its source voltage drops a threshold voltage below +15 V. Thus as the analog voltage decreases from +15 V to -15 V,  $V_{GS}$  increases from 0 V to 30 V, thus increasing the channel conductivity. The P-channel device has its gate tied to -15 V, thus as the analog signal increase from -15 V to +15 V, its  $V_{GS}$  goes from 0 V to -30 V. This results in a decreasing channel resistance. The switch resistance is the parallel combination of these two devices and the bottom curve in Figure 7 results.

## APPLICATIONS

The DG300A series of analog switches, having fast switching and low  $r_{DS(ON)}$ , lend themselves to applications such as sample and hold and high speed multiplexing. Low  $r_{DS(ON)}$  also means small offsets when switching integrators or amplifiers. Nearly constant ON resistance also means lower distortion when switching into lower impedance loads.

### Charging and Discharging Capacitors

When charging or discharging capacitors, it is important not to exceed maximum ratings of the switch. Current through the switch must be limited to 30 mA continuous or a 100 mA pulse for 1 millisecond or less having a 10% duty cycle. Exceeding maximum ratings could mean poorer reliability than could otherwise be expected. One method of preventing excessive current is by using current limiting resistors in series with the switch as shown in Figure 9. If voltage differentials between the switch input and the capacitor are small, these resistors may not be necessary because the switch resistance itself would be sufficient to limit current.

In the integrator of Figure 10,  $R_L$  controls the discharge rate of the capacitor. During reset to zero V, the reset switch is closed and the start/stop switch is open. Opening the start/stop switch with the reset open will hold the output of the integrator at its present value.

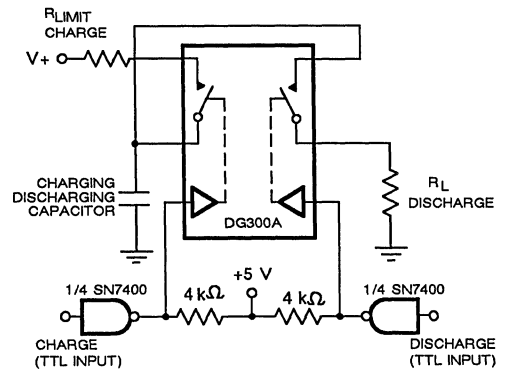


Figure 9. Using Current Limiting Resistors In Capacitive charge/Discharge Circuits

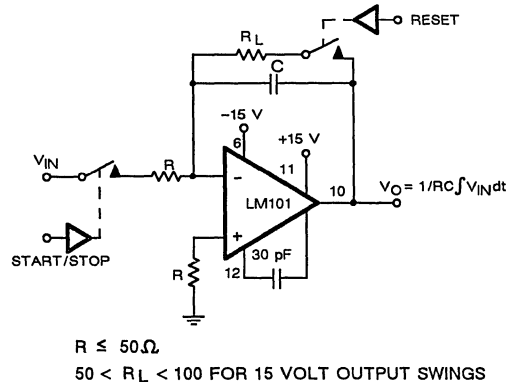


Figure 10. Integrator with Analog Reset and Start/Stop Capability

### Charge Cancellation

Figure 11 shows a sample and hold circuit using the DG303A dual SPDT switch. Any analog switch when opened will inject charge into the source and drain nodes due to gate to source and gate to drain capacitance. This charge when injected into a sample and hold capacitor will create offset errors in the sample and hold output during hold. This error can be eliminated using another switch to inject charge into a small storage capacitor (200 pF) during the same period which is then subtracted off during the hold period.



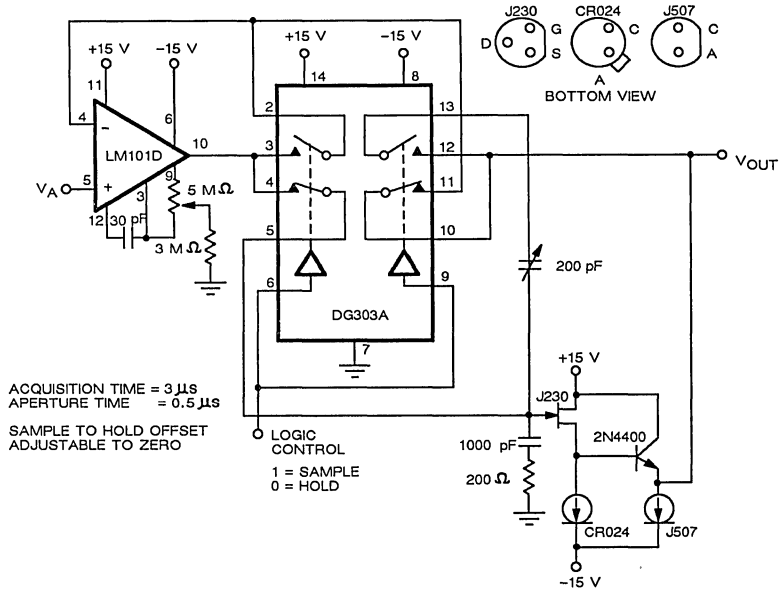


Figure 11. Sample and Hold

Fast switching times and low  $r_{DS(ON)}$  of the DG303A allow fast data acquisition with acquisition times of 3  $\mu$ s possible.

### Fast Data Multiplexing

Having high switching speed, the DG300A series

switches are ideal for fast multiplexing of data. Figures 12, 13, and 14 are applications of various DG300A switches employing their high speed in switching data.

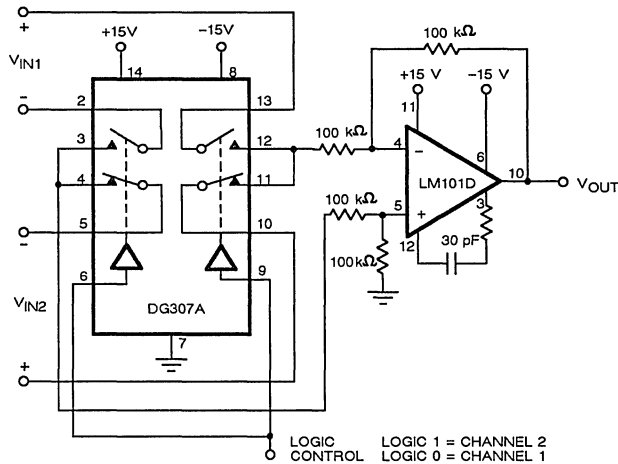


Figure 12. Basic Switched Differential Amp

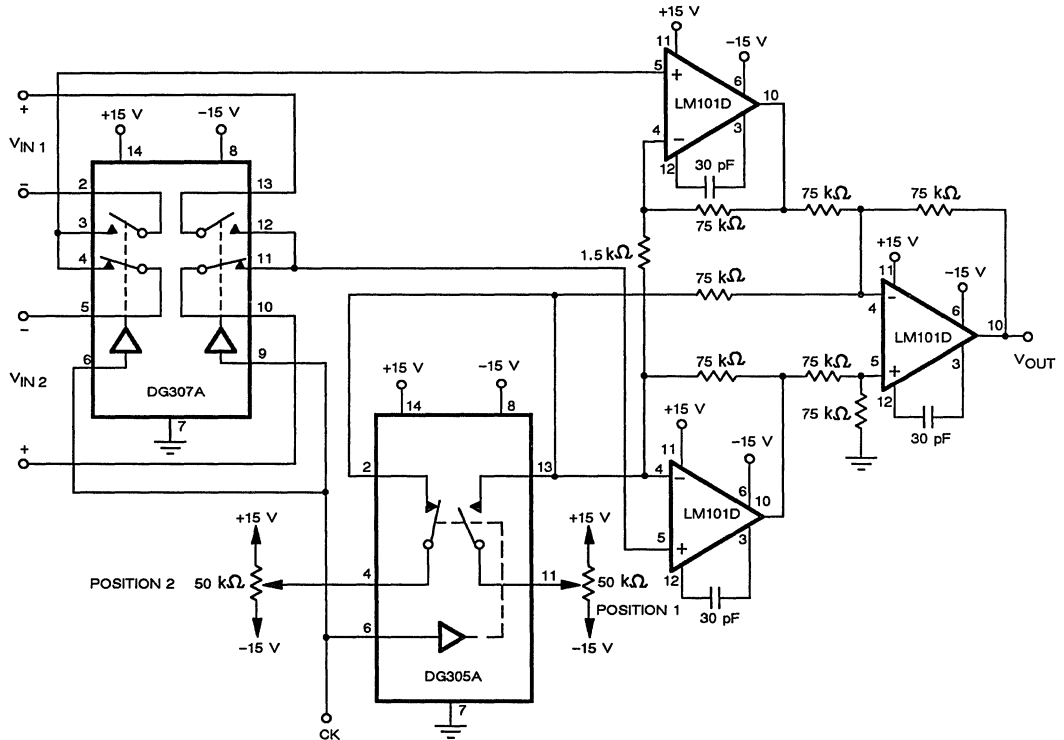


Figure 13. 2-Channel to 1-Channel Chopping Differential Amplifier With Position Adjustment

The high switching speed of the DG304A is taken advantage of in the 64-channel two level multiplex system of Figure 14. This circuit employs 4 each DG506A 16-channel multiplexers as the first MUX level and uses the high speed DG304A's in the second level to switch between DG506A outputs. CMOS digital logic forms the address logic for the multiplexers as well as the DG304's.

As one multiplexer is being sampled at the output, the other multiplexers are being switched to the next address line. This allows the overall system transition time to be shortened from 1.5  $\mu$ s to 0.25  $\mu$ s. The two level system also lowers output node capacitance and output leakage (refer to Reference 5 for details).

## Battery or Low Power Applications

The DG300A series of switches are inherently low power and are ideal candidates for applications using battery supplies. Figure 15 shows the variation of device power dissipation versus the switching frequency of the switch. It can be seen that in low frequency switching the power dissipation is negligible. One application for which this switch is ideal is in autoranging circuits for battery operated Digital Volt Meters.

Figure 16 is the schematic of a binary addressed amplifier in which the gain increases by decades as the binary input decreases from 1,1 to 0,0. Its minimum gain, as shown in the table, is 1 and its maximum gain is 1000. Since the switch is static in this type of amplifier the power dissipation of the switch will be less than a tenth of a milliwatt.

A COMPARISON OF 1 LEVEL vs 2 LEVEL  
64-CHANNEL MULTIPLEX SCHEMES

	1 LEVEL	2 LEVEL
TRANSITION TIME	1.5 $\mu$ S	0.25 $\mu$ S
OUTPUT CAPACITANCE	160 pF	120 pF
OUTPUT LEAKAGE	40 nA	16 nA

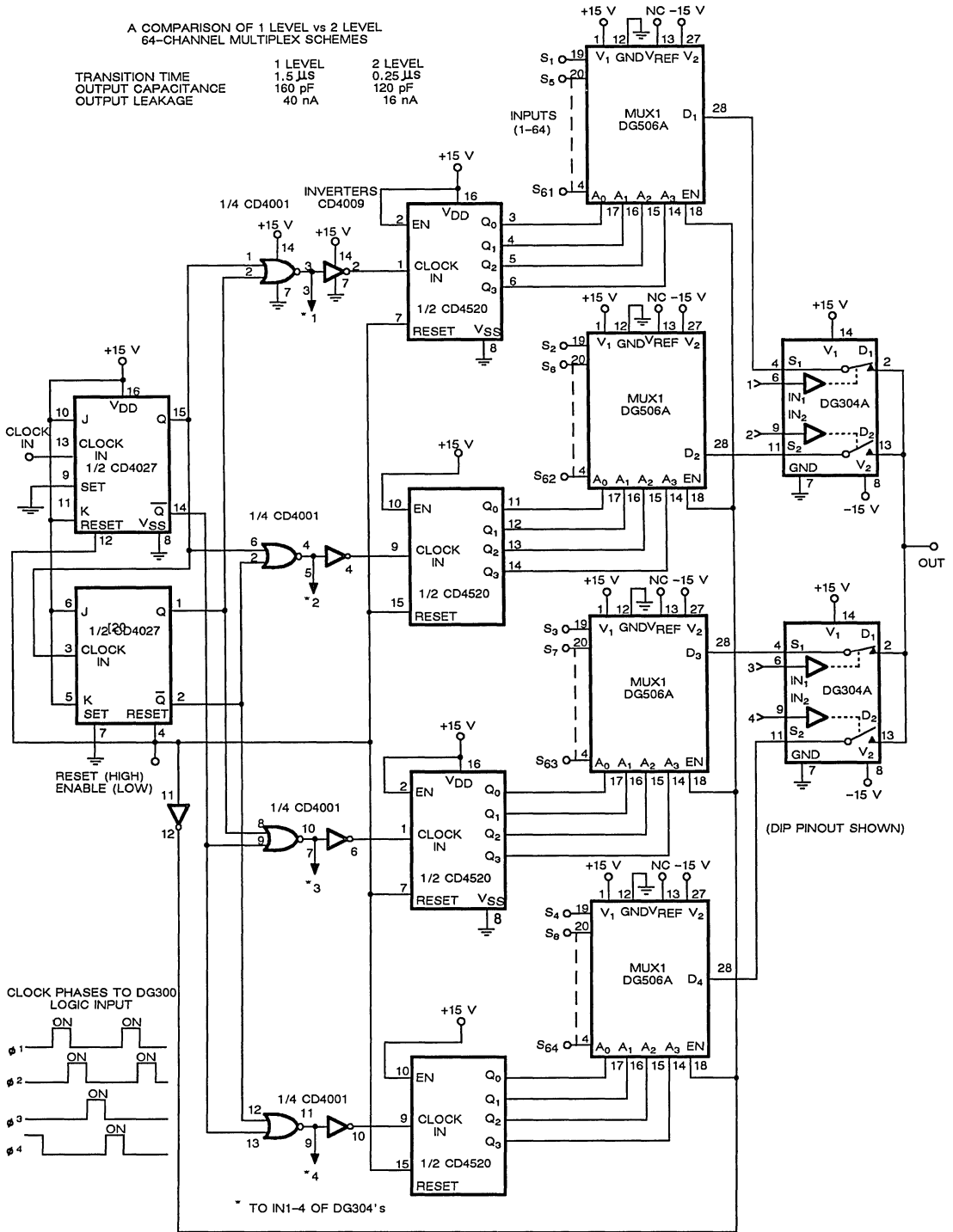


Figure 14. 64-Channel 2-Level Multiplex System Using DG304A as High Speed Switches

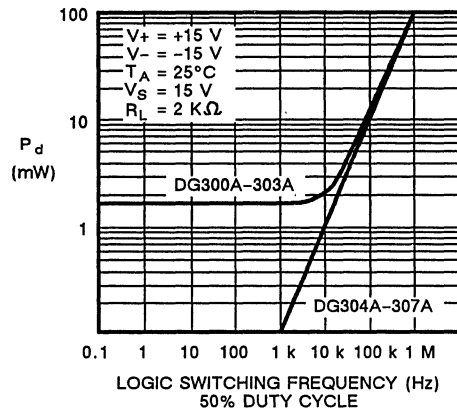


Figure 15. Device Power Dissipation vs. Switching Frequency

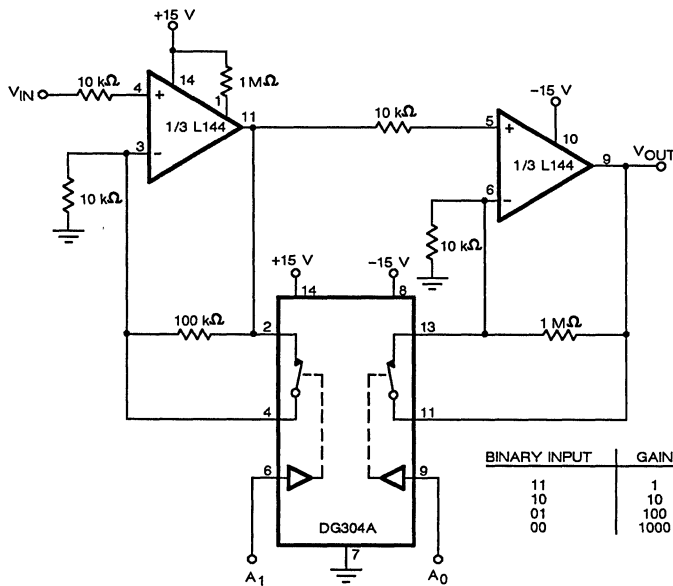


Figure 16. Low Power Binary to  $10^n$  Gain Low Frequency Amplifier

The low power of the DG307A also makes it ideal for use with the low power programmable triple op amp, the L144, in an active filter. Figure 17 shows the use of the DG307A in a switchable center frequency ac-

tive filter, allowing a decade change in center frequency. Additional information on the L144 and the active filter circuit can be found in References 6 and 7.

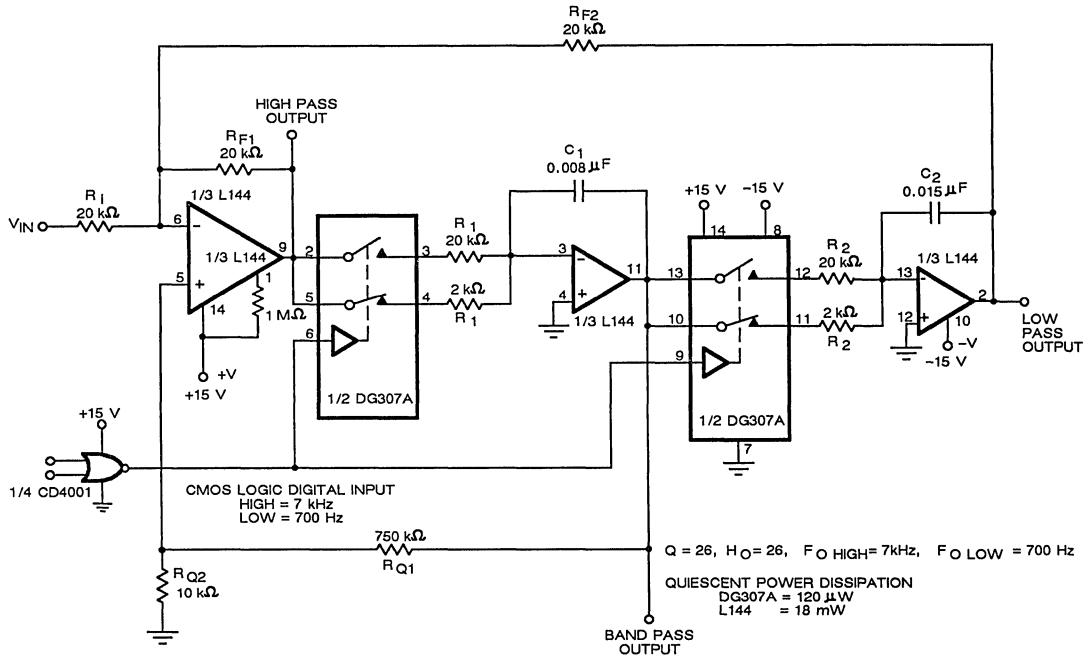


Figure 17. Low Power Active Filter with Digitally Selectable Center Frequency

Table 1

Design Procedure for the State Variable Active filter

Given:  $f_0$  (Resonant Frequency),

$H_0$  (Gain at the Resonant Frequency) and  $Q_0$

**STANDARD DESIGN**

(Assumes Infinite Op-Amp Gain)

1. Chose  $C_1 = C_2 = C$ , A CONVENIENT VALUE

2. LET  $R_1 = R_2 = R$

3. THEN  $R = \frac{1}{2\pi \times f_0 \times c}$

4. CHOOSE  $R_{11} = R_{12} = KR$ ,

WHERE  $R_{11}, R_{12} =$  A CONVENIENT VALUE

AND  $K = \frac{H_0}{Q_0}$

IF  $H_0$  IS UNIMPORTANT (i.e., GAIN CAN BE ADDED BEFORE AND/OR AFTER THE FILTER), CHOOSE  $K = 1$

5. LET  $R_{Q1} =$  A CONVENIENT VALUE

6. THEN  $R_{Q2} = \frac{R_{Q1}}{(2 + K) \times Q_0 - 1}$

A ( $f_0$ ) = THE NOMINAL OP AMP GAIN AT THE RESONANT FREQUENCY.

GBWP = THE NOMINAL GAIN-BANDWIDTH PRODUCT OF THE OPERATIONAL AMPLIFIER

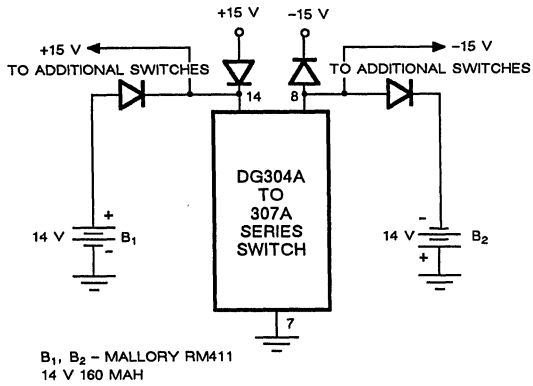


Figure 18. Long Term Supply Standby

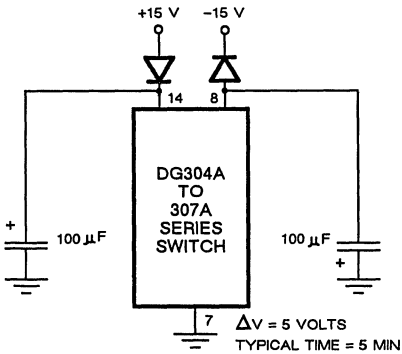


Figure 19. Short Term Supply Standby

An advantage of the DG304A to DG307A family of switches, due to their low power consumption, is the

ability to use batteries or capacitors to supply standby power to the switch. In this way errors at analog output and shorting of signals can be avoided when supply power fails. This method would also prevent loading of the analog signal by the switch which could prevent the use of the signal in other portions of a system. Figure 18 and 19 show methods of implementing standby power.

Battery lifetime should be well over 1 year with continuous standby.

## Thermocouple Applications

Because silicon in contact with aluminum creates a thermocouple, low power dissipation by the integrated analog switch will mean lower offset voltages added to thermocouple voltage. Thus, lower power dissipation translates into better potential accuracy. The DG300A series of analog switches do quite well in this type of application. Figure 20 shows a typical schematic of a thermocouple switching circuit. It is necessary to switch the thermocouples differentially in order to cancel any thermal offsets due to the switch.

## Single Supply Operation

The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs (or performance given up) while using single supplies are: 1) Increased  $r_{DS(ON)}$ ; 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied in Figures 21 to 23. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single supply operation are  $V+$  and 0 V.

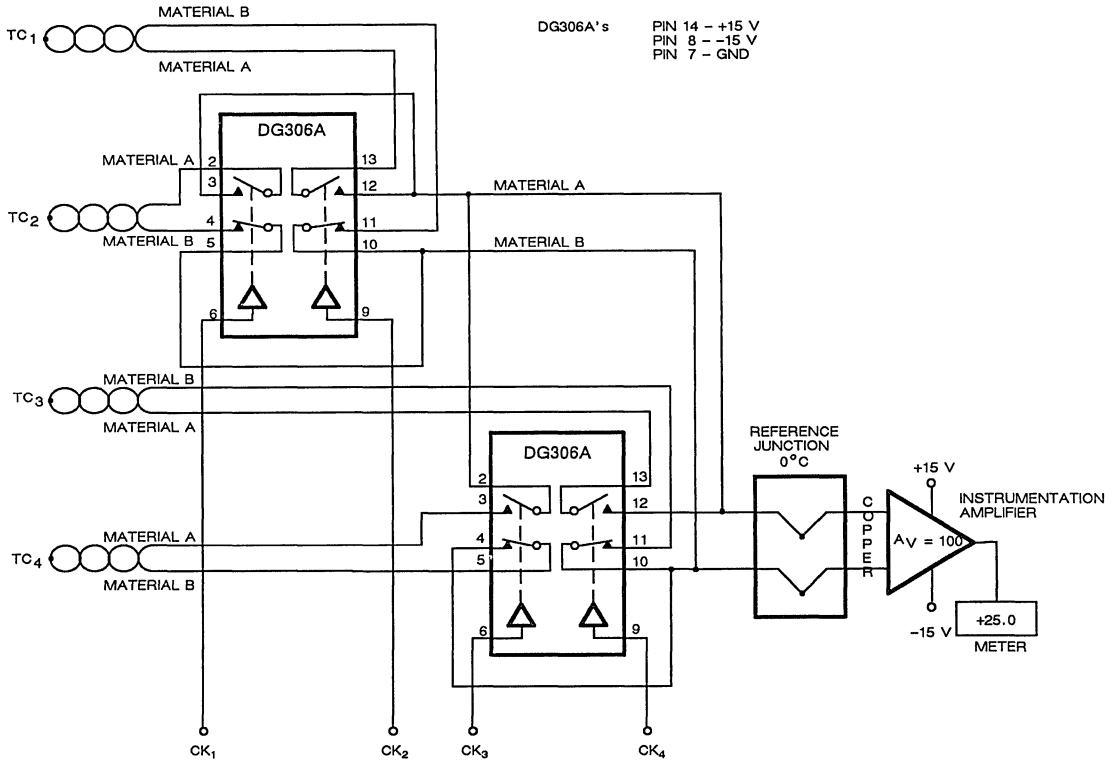


Figure 20. Thermocouple Multiplexing

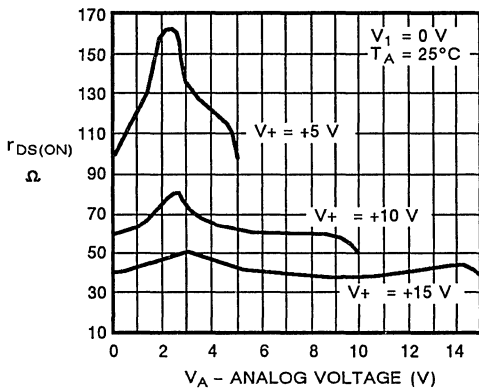


Figure 21.  $r_{DS(ON)}$  vs. Analog and Positive Supply Voltage With  $V_- = 0$  V

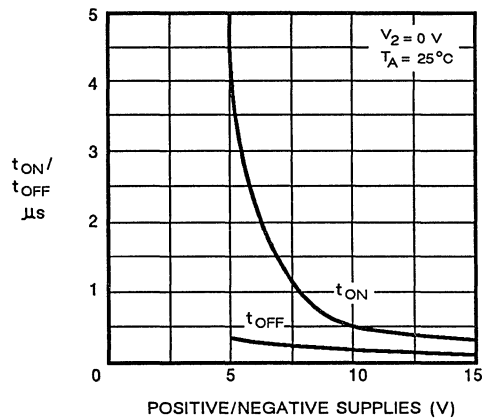


Figure 22. Switching Time vs. Power Supply Voltage

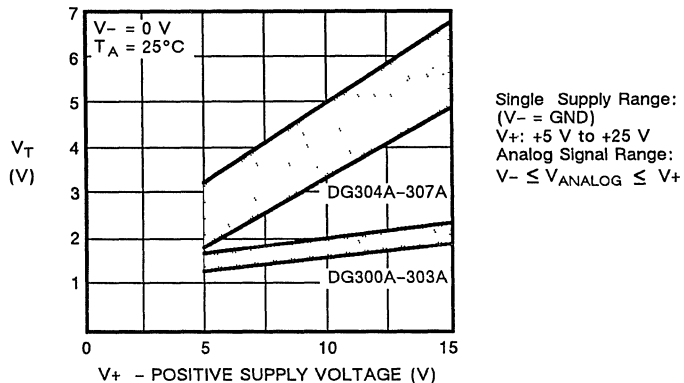


Figure 23. Input Threshold Voltage vs. Positive Supply

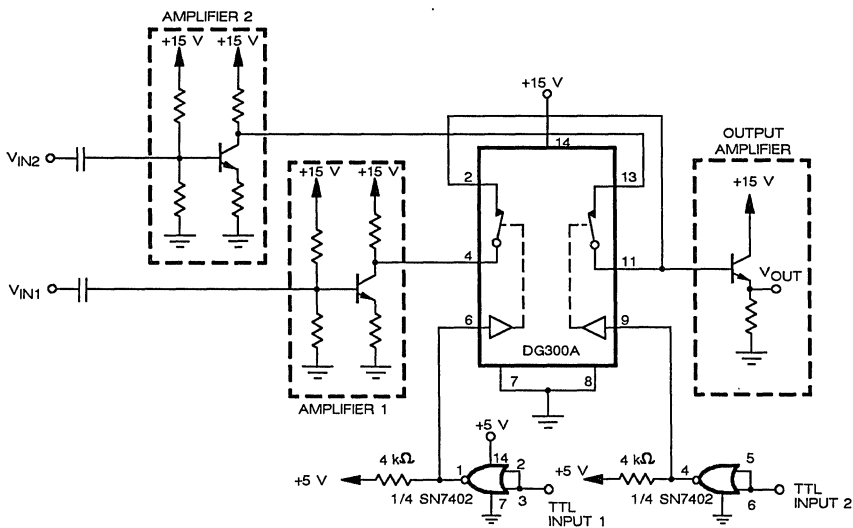


Figure 24. Switching Single Supply Amplifiers Using the DG300A



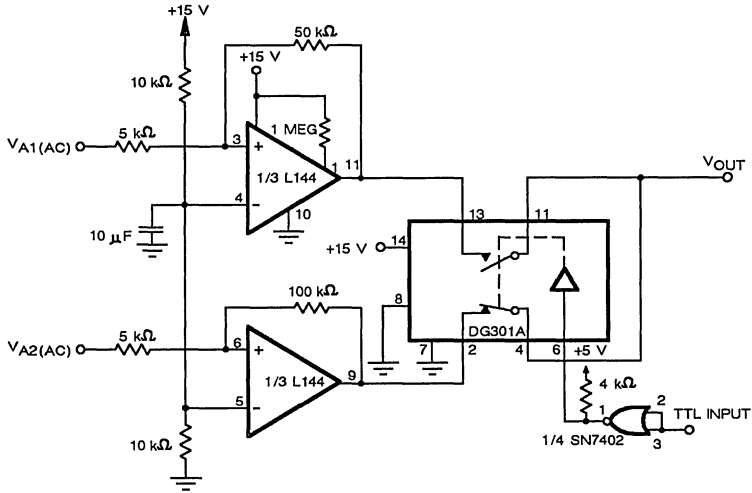


Figure 25. Single Supply Op Amp Switching

As shown in Figure 26 when switching capacitor-coupled analog signals, the coupling capacitor should appear either before or after but not on both sides of

the switch. This is necessary to keep a positive bias on the switch drain and source when the switch is turned on.

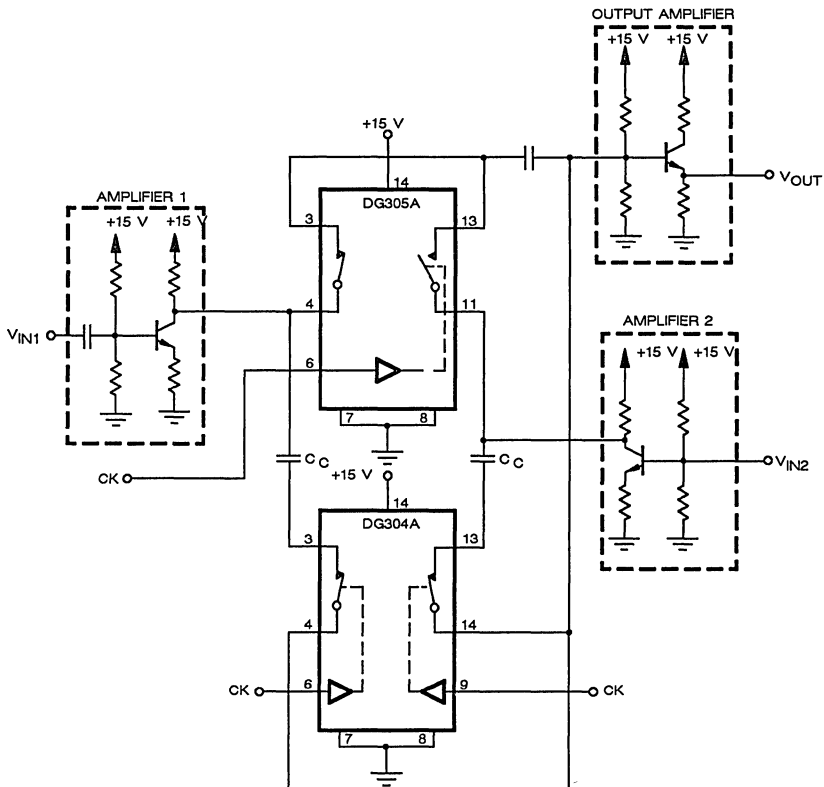


Figure 26. Proper Methods for Interfacing Capacitive Coupled Outputs to Analog Switches

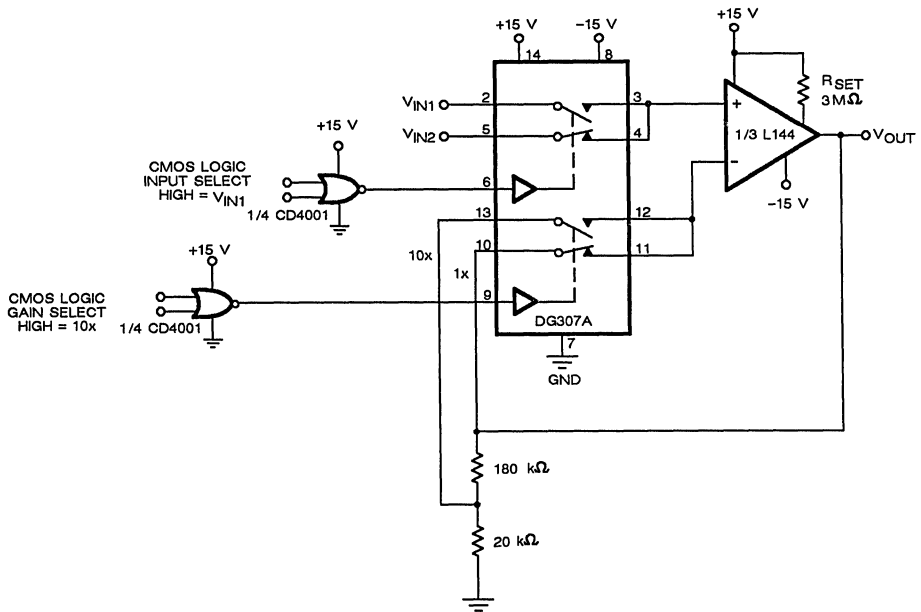


Figure 27. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain

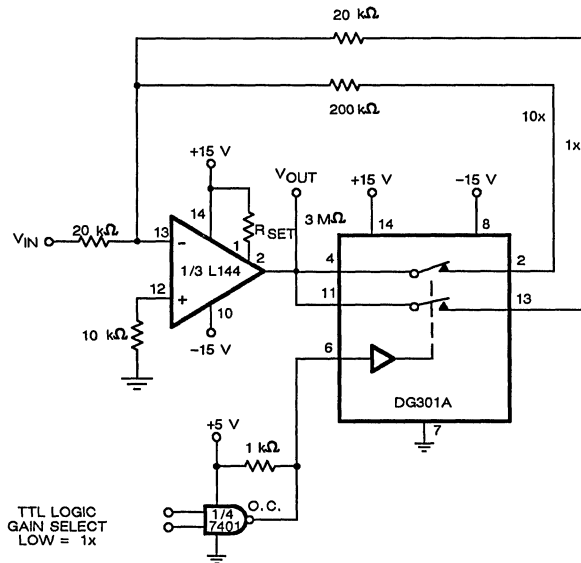


Figure 28. Low Power Inverting Amplifier with Digitally Selectable Gain

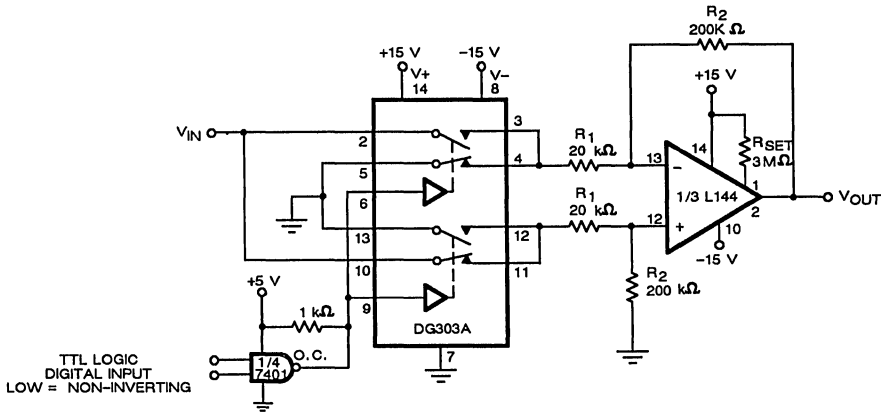
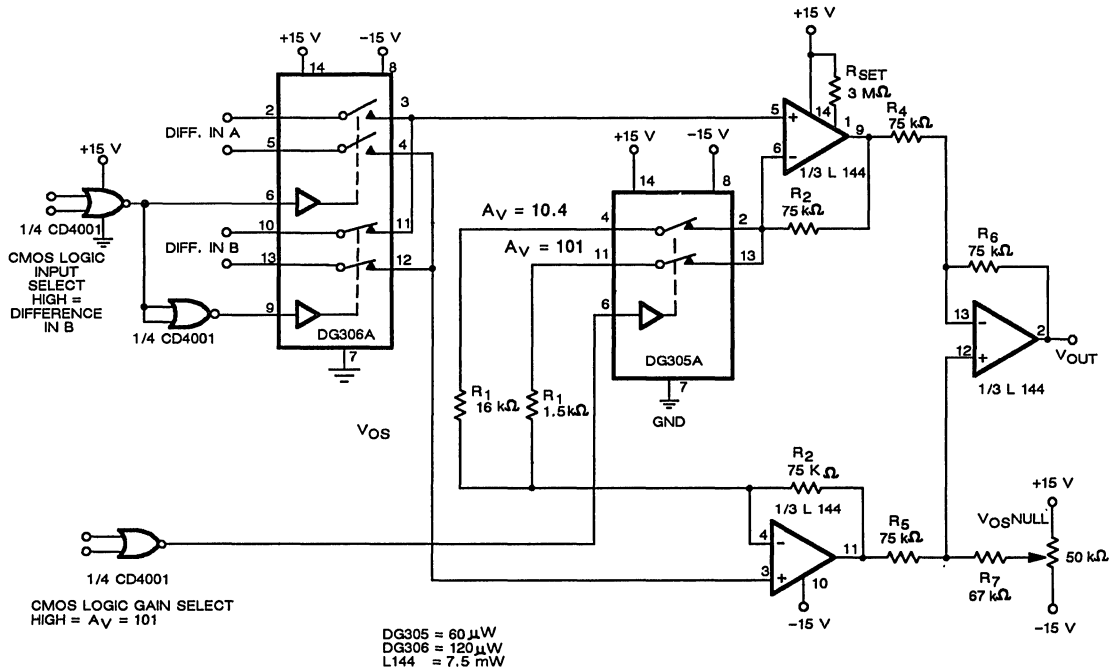


Figure 29. Polarity Reversing Low Power Amplifier



$R_{SET}$  programs L144 power dissipation, gain-bandwidth product.  
Refer to AN73-6 and the L144 data sheet

Voltage gain of the Instrumentation amplifier is:

$$A_V = 1 + \frac{2R_2}{R_1} \quad (\text{In the circuit shown, } A_{V1} = 10.4, A_{V2} = 101)$$

Figure 30. Low Power Instrumentation Amplifier Digitally Selectable Inputs and Gain

## REFERENCES

1. Lee Shaeffer, "CMOS Analog Switches – A Powerful Design Tool," Siliconix Application Note AN75-1, July 1975.
2. Gary Dixon, "Analog Switches in Sample and Hold Circuits," Siliconix Application Note AN74-2, Jan. 1976.
3. Gary Grandbois, "Build an Autoranging DMM with the LD130 A/D Converter," Siliconix Design Aid DA76-3, June 1976.
4. "Siliconix Analog Switch Data Book", June 1976.
5. J. Jenkins, "IC Multiplexer Increases Analog Switching Speeds", Siliconix Application Note AN73-2, April 1976.
6. Marvin K. Vander Kooi, "L144 Programmable Micro-Power Triple Op Amp", Siliconix Application Note AN73-6, Jan. 1975.
7. Lee Shaeffer, "Op Amp Active Filters – Simple to Design Once You Know the Game", EDN Magazine, April 20, 1976.

# CMOS ANALOG SWITCHES – A POWERFUL DESIGN TOOL

Revised January 1988

## INTRODUCTION

Siliconix CMOS analog switches combine large voltage handling capability, low power dissipation, low leakage, and direct TTL/CMOS interface capability for maximum design flexibility. In addition, a family of multiplexers is available which provides binary decoding on the chip for system simplicity. This application note describes the Siliconix CMOS DG20X switch family and DG50X multiplexers. It offers circuits which illustrate their capabilities.

## Properties of CMOS

CMOS (Complementary Metal-Oxide-Semiconductor) combines P-channel and N-channel enhancement-mode FETs in a common substrate. P-channel enhancement-mode FETs have a negative threshold voltage (the gate must be several volts more negative than the source or drain in order for current to flow between the source and the drain), while N-channel FETs have a positive threshold (Figure 1). When a P-channel FET is used as a switch (standard PMOS devices), the gate is held at the negative supply when in the ON condition, and the FET conducts for most voltages applied to the source. However, when the source voltage approaches the negative supply, the resistance approaches infinity. The result is a dead-band equal to the threshold voltage of the FET.

This problem is overcome by connecting an N-channel FET in parallel with the P-channel device. The N-channel gate is tied to the positive supply, and the FET is turned on hardest when the source is most negative. The resistance curve of the P-channel and N-channel FETs in parallel is shown in Figure 1.

The resistance curve is nearly flat for  $V_- \leq V_S \leq V_+$  (only CMOS is capable of this) but some resistance variation is normal. 20% peaking is typical for  $\pm 15$  V power supplies, with greater peaking at lower supply voltages. If the P- and N-channel FETs have different

thresholds the peaks will not be symmetrical. As the switch heats up the resistance increases 0.5%/°C.

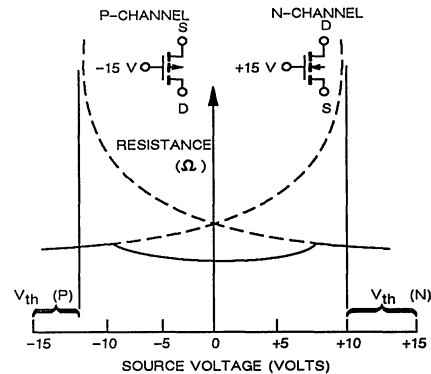
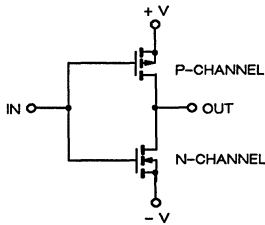


Figure 1. Resistance vs. Source Voltage of P-Channel and N-Channel FETs

Because the gates of the P- and N-channel FETs are internally switched to opposite supply voltages, one would expect that leakage currents and switching glitches would cancel when  $V_S = 0$ . This would indeed be true if the FETs were identical except for polarity. However, because the conductance of the N-doped silicon is 2.5 times greater than that of equally doped P-type silicon, it is a practical impossibility to make the leakage currents and capacitances equal for FETs of equal resistance (the P-channel is physically 2.5 times larger than the N-channel). Therefore, cancellation takes place at some intermediate voltage. Because the measured leakage is the P-channel leakage minus the N-channel leakage, small variation in the absolute value of either can make a large change in the difference. Since small amounts of impurities can greatly influence the leakage, both the magnitude and polarity of the leakage measured at the source or drain will vary greatly from unit to unit, and will depend on the analog voltage and the temperature. Even though the leakage is unpredictable, it is still less than a comparable PMOS or bipolar switch.

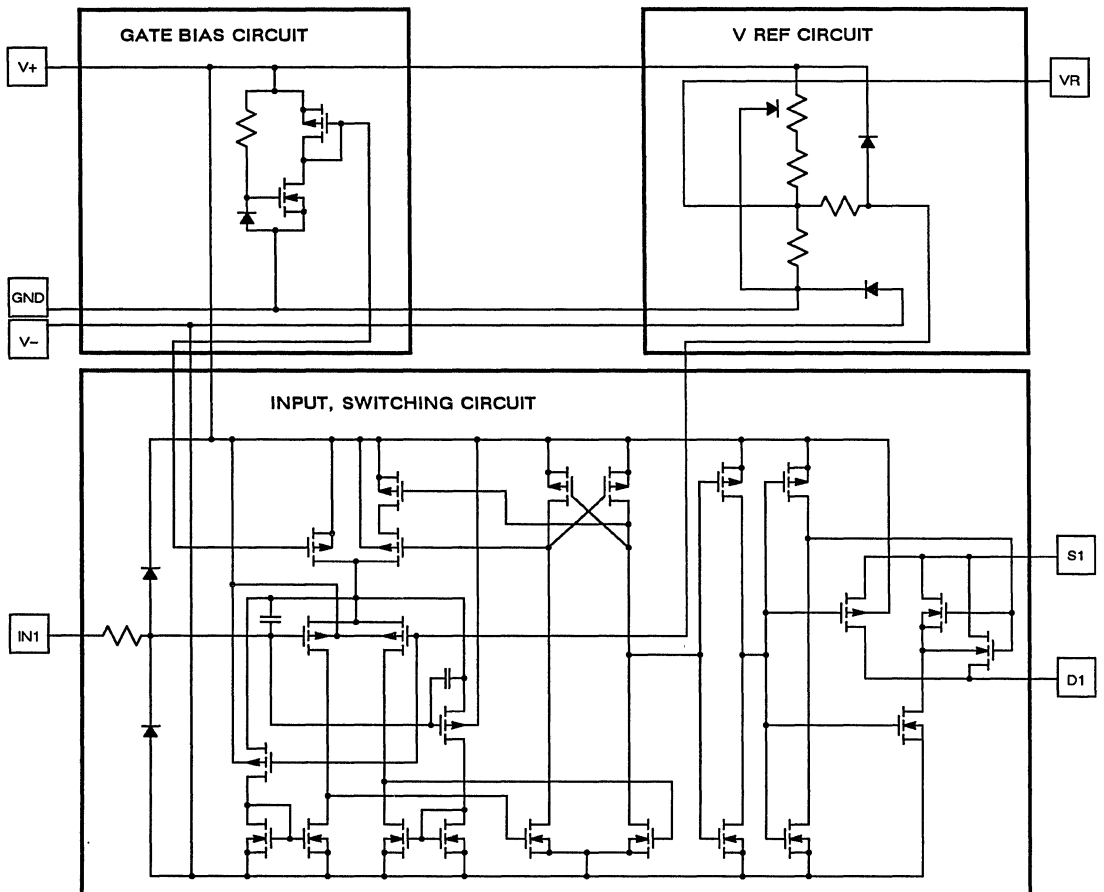


**Figure 2.** A CMOS Inverter

In addition to a large analog voltage capability, a second advantage of CMOS is low power dissipation. Figure 2 shows a digital inverter with virtually no static power dissipation. When the input is pulled high, the N-channel turns ON and the P-channel OFF. Thus the

output is tied to the negative supply through  $r_{DS(ON)}$  of the N-channel FET, while the P-channel device draws no current. If the input is changed to a negative voltage the state of the FET is reversed, pulling the output high. When a CMOS device is turned ON, the load is turned OFF; this overcomes a major disadvantage of PMOS structures, where the load is ON at all times and considerable power is drawn when the FET is ON.

The DG201A circuit can be divided into 6 sections. There is the input comparator, the bias circuit and voltage reference, the level shifter, buffer and inverter and the switch circuit. Figure 3 is the DG201A circuit.



**Figure 3.** Schematic of a Typical CMOS Switch Channel (DG200A and DG201A)

The input comparator is a differential amplifier whose threshold is set by the voltage reference, a 10 to 1 voltage divider, which is further stabilized by the "bias circuit". The threshold voltage is derived from a voltage divider and varies as  $V_+$  varies. Several feedback schemes are used to sharpen the switching point.

The level shifter buffer and inverter are CMOS and consume virtually no power. The inverter is necessary to drive the parallel connected CMOS switch.

In the switch two transistors are used to drive the body of the N-channel MOSFET. When ON, the body is tied to the N-channel source and when OFF, it is tied to  $V_-$ . This eliminates any modulation of ON switch resistance and when OFF, reduces leakage.

Because only the voltage divider and comparator differential amplifier draw any current other than leakage, the circuit consumes very little current.

All of the multiplexers (DG50XA, DG52X, etc.) contain decode circuitry enabling a binary logic input to select one of 4, 8, or 16 channels. Each multiplexer also contains an ENABLE-INHIBIT control, which shuts the device OFF when in the INHIBIT mode. This allows the common connection (drains) of several multiplexers to be paralleled, and the units can then be enabled one at a time. This is useful when more than 16 channels are involved. Also, when the device is inhibited, its power dissipation is typically less than

one-fourth the normal dissipation, for low total system power dissipation.

**Latch-Proof Operation**

Latchup was a thorny problem in first-generation CMOS switches. A cross section of two CMOS FETs (Figure 4) shows both a PNP and an NPN structure, which is connected as an SCR (PNPN). Under abnormal conditions, one or more of the PN junctions becomes forward biased, activating the bipolar transistor. This in turn activates the SCR, which appears as a short between the substrate (positive supply) and ground or  $V_-$ . Since the product of the NPN and PNP betas is often greater than 1000, this short would persist until power was removed or until the device burned up. When 200 ohm resistors were placed in series with the power supply leads, device destruction was prevented; however, only removal of the power supply would return the circuit to normal operation.

By using a "buried layer" configuration (Figure 5), Siliconix has reduced the product of the NPN and PNP betas to less than one, making latch-up impossible under any normal circumstance. The switches retain their desirable features such as low leakage, high OFF isolation, and high breakdown voltage. In addition, the latch-proof switches now have a much higher current capability (20 mA continuous, up to 100 mA peak of the DG200A).

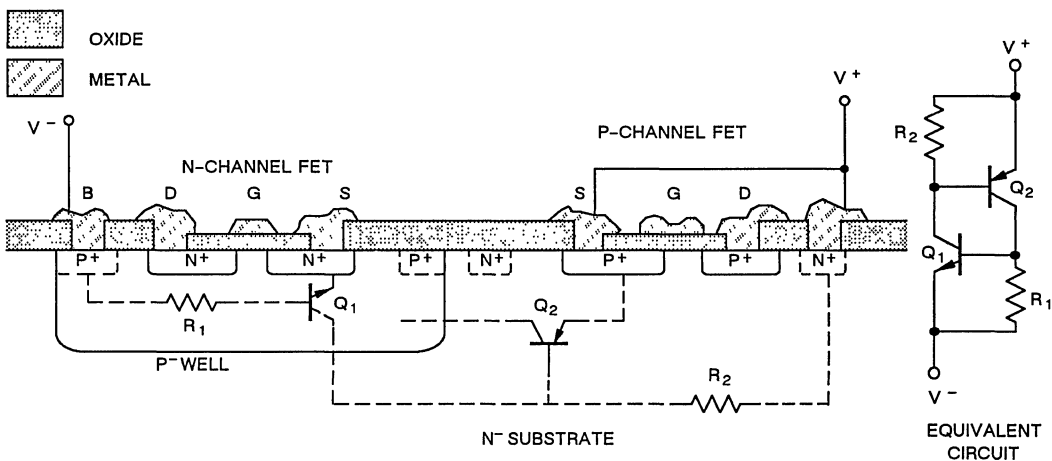


Figure 4. A Cross Section of Two CMOS FETs Showing the Parasitic Transistors and Equivalent Circuit

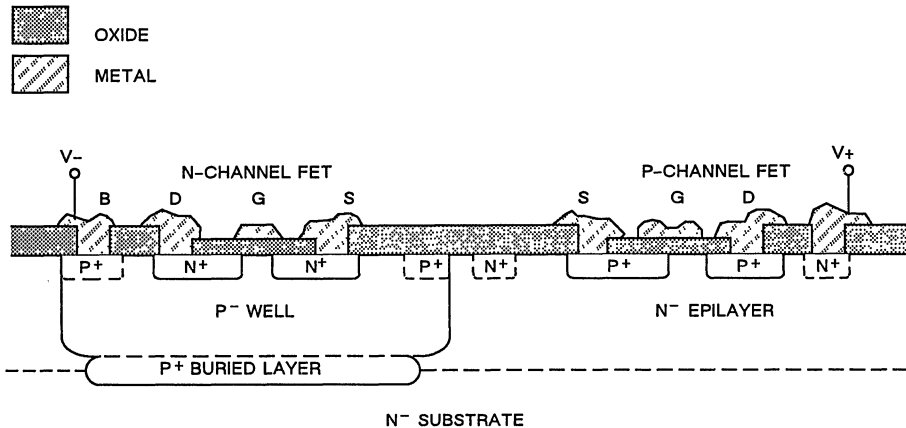


Figure 5. A Cross Section of the Siliconix "Buried Layer"

## General Switching Applications

One of the significant advantages of the CMOS structure is its ability to handle large analog voltages, since only CMOS can allow signal swings to the power supplies. A logical application is switching the outputs of operational amplifiers. The entire system can be run on  $\pm 15$  V, and the full output of the op amps (typically  $\pm 14$  V) can be used. In most cases it is advantageous to switch at the relative low impedance output of an op amp rather than at the summing junction, to minimize the effects of switch capacitance and leakage.

Figure 6 shows a novel multiplexing application. It is an adapter that allows 4 inputs to be displayed simultaneously on a single trace scope. For low frequency signals (<500 Hz) the adapter is used in the "chop" mode at a frequency of 50 kHz. The clock may be run faster, but switching glitches and the actual switching time of the DG201A limit the maximum frequency to 200 kHz. High frequencies are best viewed in the alternate mode, with a clock frequency of 200 Hz. When the clock is below 100 Hz, trace flicker becomes objectionable. One of the 4 inputs is used to trigger the horizontal trace of the scope.

Figure 7 shows a variable low-pass filter with break frequencies at 1, 10, 100 and 1 kHz. The break frequency is expressed in (1):

$$f_c = \frac{1}{2\pi R_3 C_X} \quad (1)$$

The low frequency gain is

$$A_L = \frac{R_3}{R_1} = 100 \text{ (40 dB)} \quad (2)$$

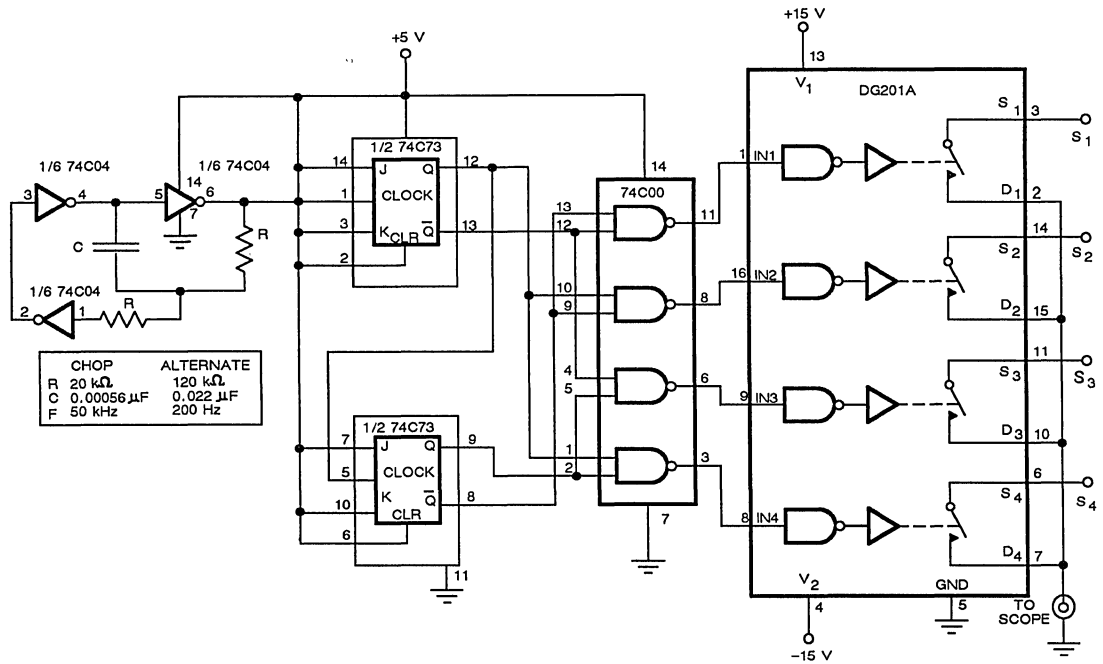
A second break frequency (zero) is introduced by  $r_{DS(ON)}$  of the DG201A, causing the minimum gain to be

$$A_{MIN} = \frac{r_{DS(ON)}}{R_1} = \frac{100 \Omega}{10 \text{ k}\Omega} = 0.01 \quad (3)$$

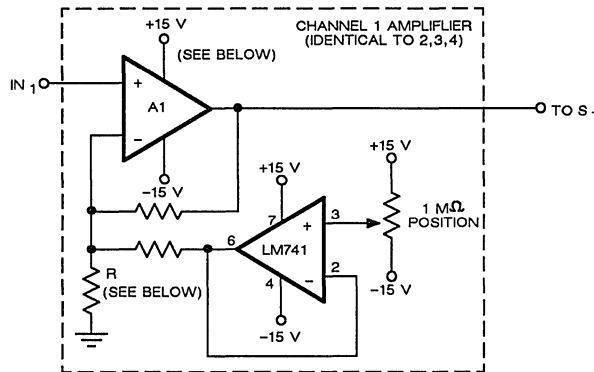
a maximum attenuation of 40 dB (80 dB relative to the low frequency gain).

The amplifier shown in Figure 8 has digitally-programmable gain and inputs. The DG200A "looks" into the high input impedance of the op amp, so the effects of  $r_{DS(ON)}$  are negligible. The DG201A is also connected in series with  $r_{IN}$  and is not included in the feedback dividers, thus contributing negligible error to the overall gain. Because the DG200A and DG201A can handle  $\pm 15$  V, the unity gain follower connection (x1) is capable of the full op-amp output range ( $\pm 12$  V).



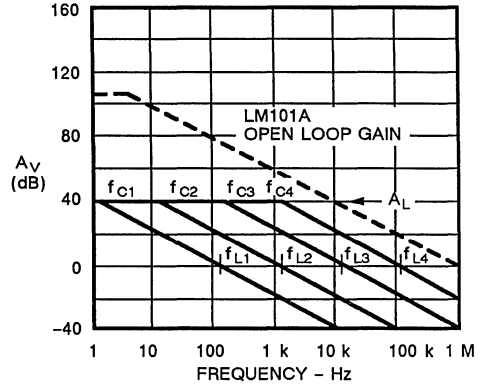
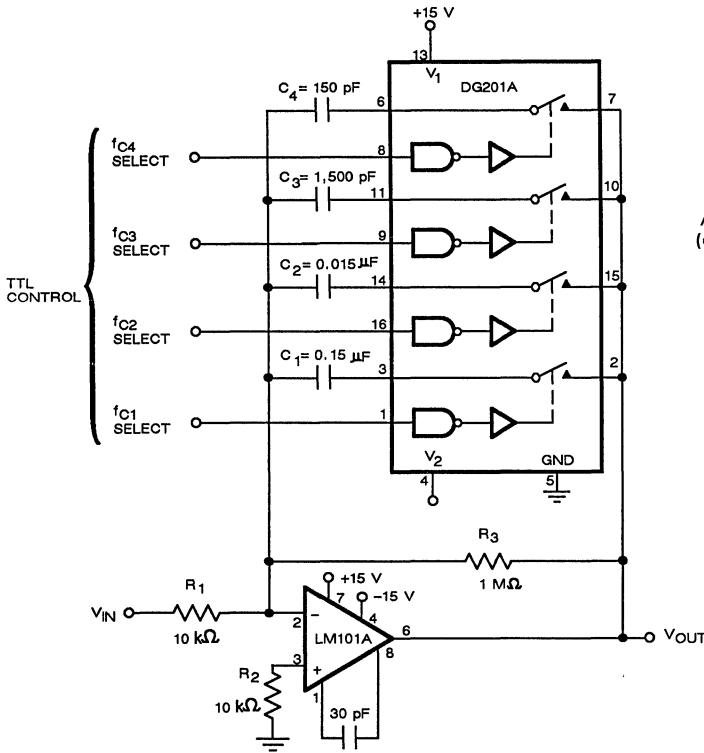


CHOP	ALTERNATE
R 20 kΩ	120 kΩ
C 0.00056 μF	0.022 μF
F 50 kHz	200 Hz



A1 IS OP AMP WITH SUITABLE BANDWIDTH, SLEW RATE, ETC., FOR DESIRED SIGNALS.  
R IS ADDED FOR EXTRA GAIN ACCORDING TO FORMULA VOLTAGE GAIN =  $2 + \frac{100 \text{ k}\Omega}{R}$

Figure 6. The "Scope Extender" Which Displays Four Channels Simultaneously on a Single Trace Scope



$A_L$  (Voltage Gain Below Break Frequency)

$$= \frac{R_3}{R_1} = 100 \text{ (40dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max Attenuation} = \frac{r_{DS(ON)}}{10 \text{ k}\Omega}$$

Figure 7. Active Low Pass Filter with Digitally Selected Break Frequency

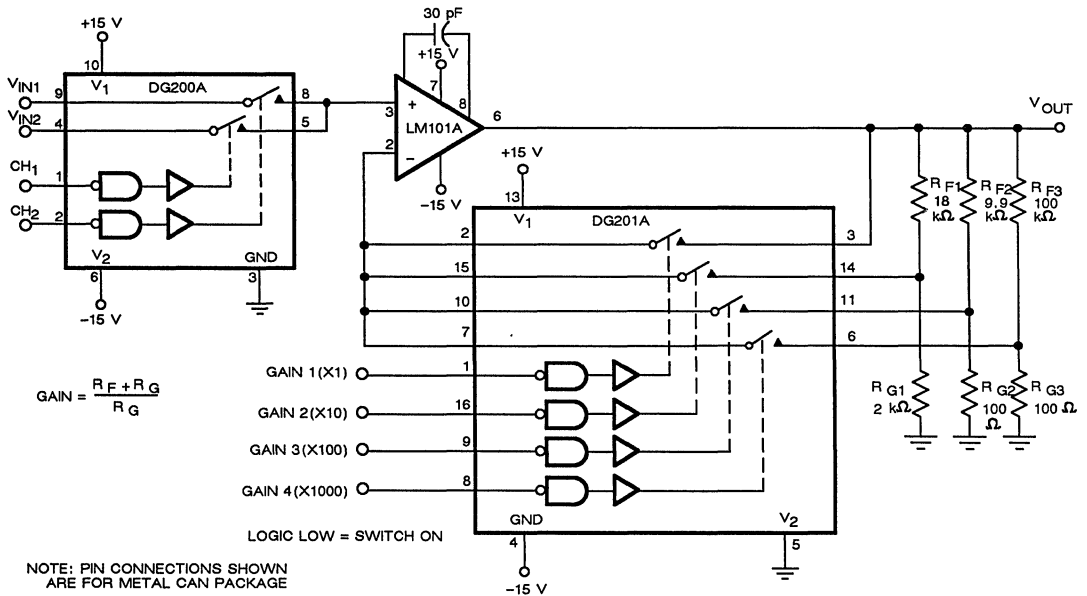


Figure 8. A Precision Amplifier with Digitally Programmable Inputs and Gains

A single DG201A contains all the switches necessary for the sample-and-hold circuit shown in Figure 9. Switch 4 provides cancellation of coupled charge (glitches), keeping the sample-to-hold offset below 5 mV over the analog voltage range (-10 to +10 V). Aperture time is typically 1 μs. Acquisition time is 25 μs, but this can be improved by using a faster slewing op amp. Droop rate is typically less than 5 mV/sec at 25°C.

The low  $r_{DS(ON)}$  and high peak current capability of the DG200A makes it ideal for discharging an integrator capacitor (Figure 10). A high logic input pulse disconnects the integrator from the analog input and discharges the capacitor. When the logic input is returned to low the integrator is triggered, having the transfer characteristic,

$$V_{OUT} = \frac{1}{10^5 C} \int_{t_1}^{t_2} V_1 dt \quad (4)$$

D<sub>1</sub> and D<sub>2</sub> prevent the capacitor from charging to over 15 V.

It is possible to operate a CMOS switch from a single supply by shifting the ground and logic inputs to an intermediate voltage, as shown in Figure 11. This allows an analog voltage range of 0 to +30 V.

A latching SPDT switch is shown in Figure 12. This is recommended when the switch is activated by a peak or limit detector, or with mechanical switches (to eliminate contact bounce). The inputs are normally low, and the switches are held in predetermined states. When either A<sub>1</sub> or A<sub>2</sub> receive a HIGH pulse, the switches assume the states given in the Truth Table (Figure 13). Simultaneously holding A<sub>1</sub> and A<sub>2</sub> HIGH will cause both switches to be OFF; the last input to go LOW upon release of the commands will determine the eventual states of the switches.

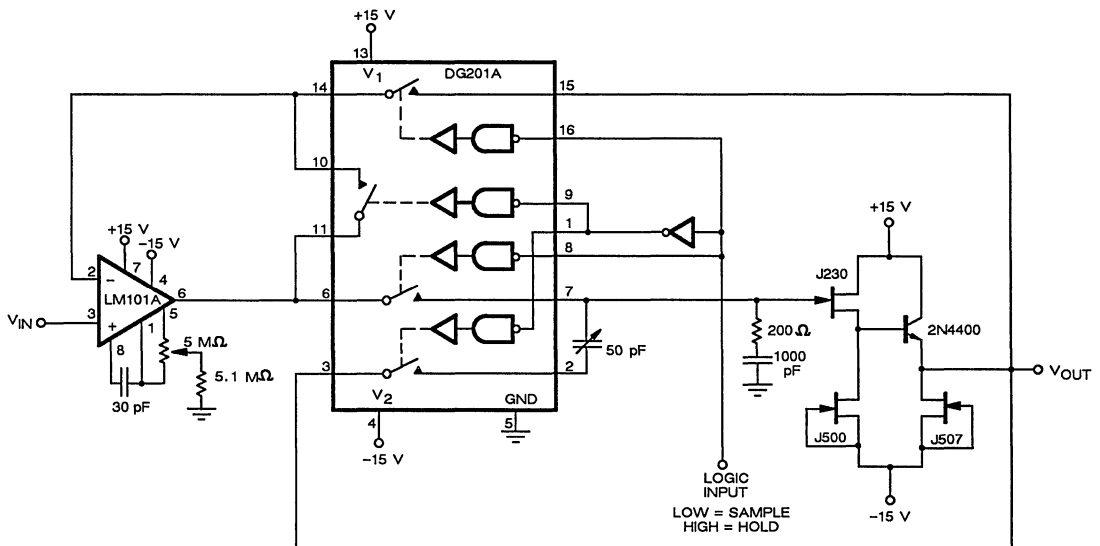


Figure 9. DG201A Sample and Hold

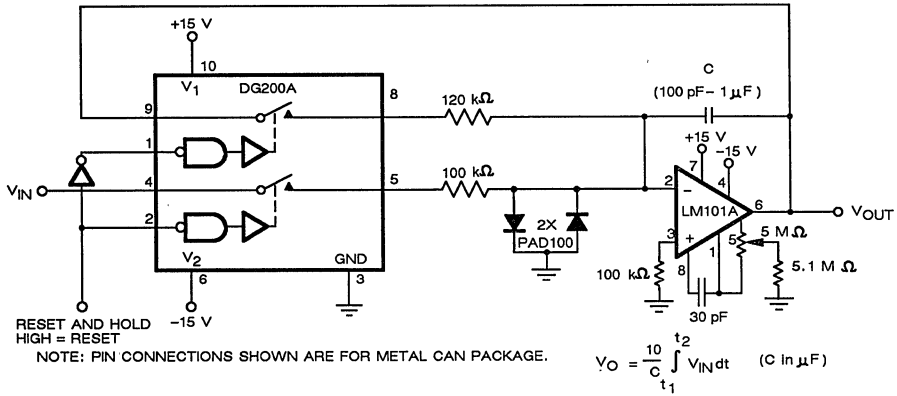


Figure 10. A Resettable Integrator

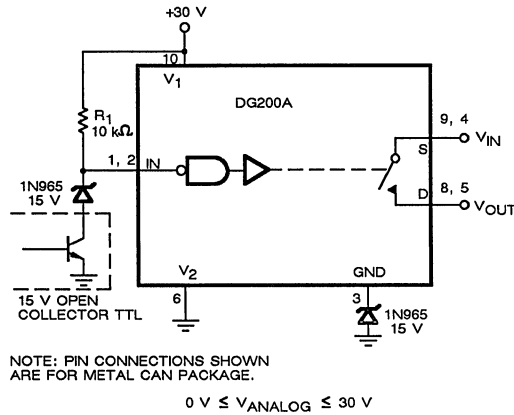


Figure 11. Operation from a Unipolar Supply

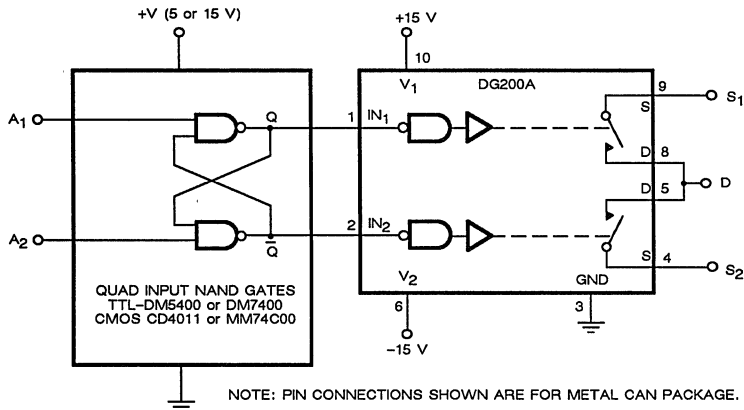
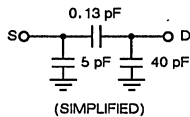
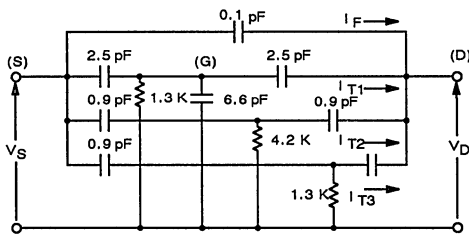


Figure 12. A Latching SPDT Switch

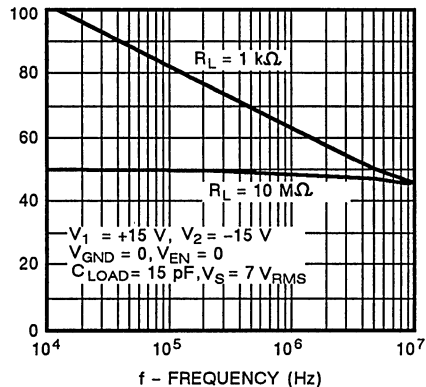
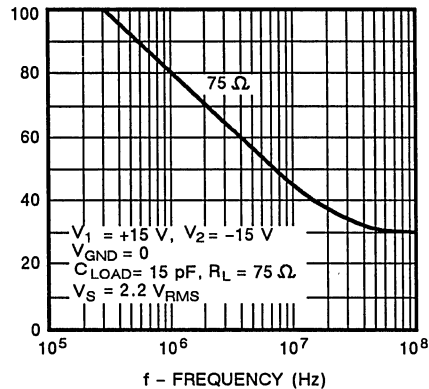
**TRUTH TABLE**

Command		State of Switches after Command	
A <sub>2</sub>	A <sub>1</sub>	S <sub>2</sub>	S <sub>1</sub>
0	0 (normal)	same	same
0	1	OFF	ON
1	0	ON	OFF
1	1	INDETERMINATE	

**Figure 13.**



When switching high frequency signals (> 100 kHz), some knowledge of the OFF characteristics are helpful. Figure 14 shows the equivalent OFF circuit of a DG200A and the accompanying graph gives the isolation under the conditions specified. 40 dB isolation at 6 MHz is good for general purpose video switching. A DG200A can achieve this easily, using the circuit shown in Figure 15 (assuming careful P.C. board layout). When greater isolation is needed, the circuit shown in Figure 16 is recommended. The "T" configuration provides over 40 dB more OFF isolation with only a slight increase in ON insertion loss.



**Figure 14.** Equivalent "OFF" Circuits and OFF Isolations of the DG200 and DG506A

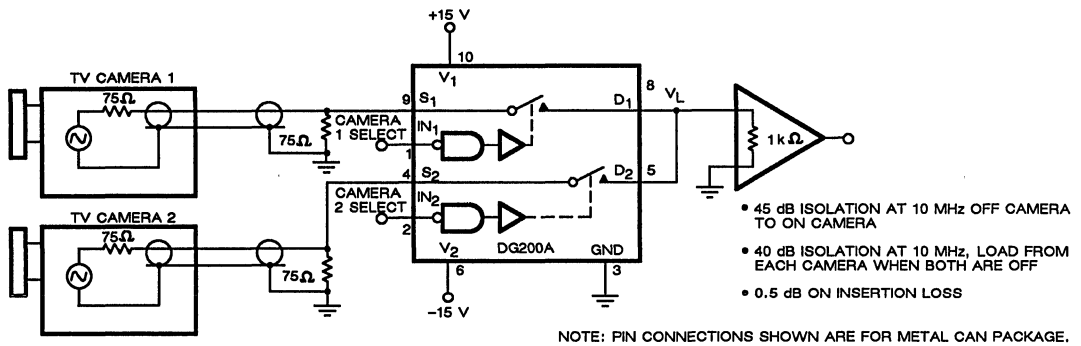


Figure 15. General Purpose Video Switch (f = DC to 10 MHz)

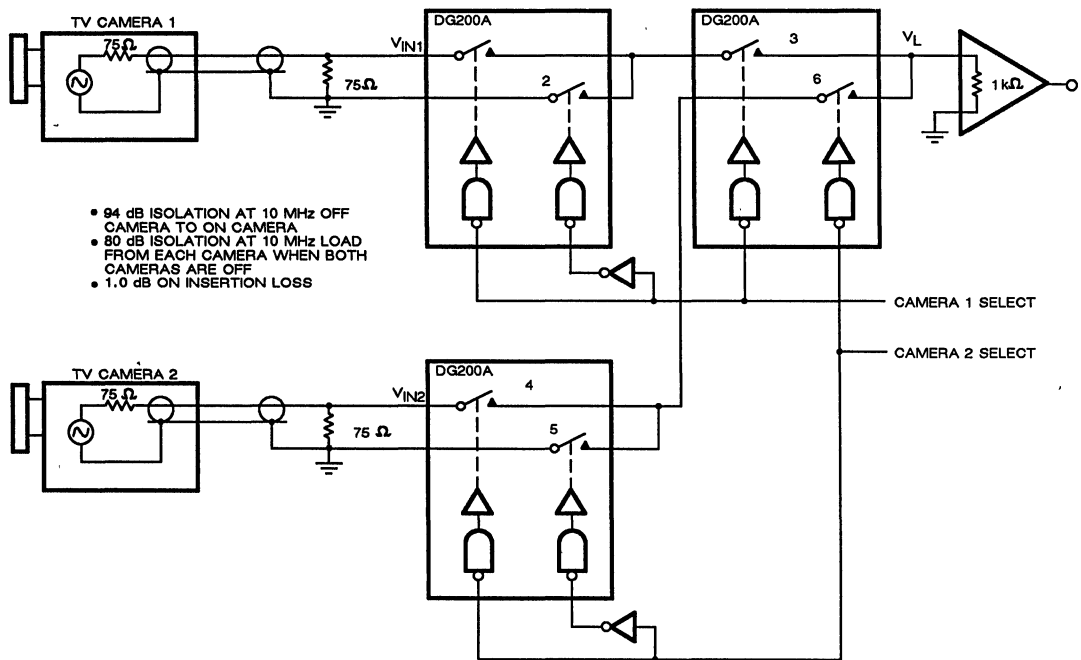


Figure 16. Video Switch with Very High OFF Isolation

Figure 14 also shows the high frequency characteristics of the DG506A and a simplified OFF equivalent circuit. The DG506A has OFF isolation which is constant when working into a capacitive load, allowing the designer to model the OFF DG506A as a capacitor of nominal value 1.13 pF. Not all sources have equal OFF isolation, however.  $S_9$  has the greatest isolation, while  $S_8$  is worse due to its proximity to the

drain. Grounding the metal lid on the package (it normally floats) increases the isolation an average of 3 dB.

An in-depth study of switching high frequency signals is presented in Siliconix applications note AN73-3, "Switching High Frequency Signals with FET Integrated Circuits."

## Multiplexing

Multiplexing allows a number of signals to be processed simultaneously through a single cable, amplifier, and data conversion system. Numerous industrial and commercial uses include factories and warehouses where conditions at remote parts of a building can be monitored and sent to a central control point over a single cable. Airplanes take great advantage of multiplex systems, both receiving and transmitting information from central points with a minimum of wire. Many hotels and motels pipe up to 16 channels of music to each room. The music desired is selected by the guest in the room. When digitizing information, the economies are readily apparent between using a \$50 multiplex system and a single A to D converter, as compared to employing a separate expensive A to D converter for each of several channels.

Figure 19 shows a typical multiplex system intended to carry one of 8 inputs into a remote location. A 5 V pulse train is sent down a separate channel to perform timing and synchronizing functions. A 15 V reset pulse is superimposed on the 5 V clock, which is detected by the MM74C00 in the receiver. Using this system, many remote points can be monitored, one at a time, at any of several locations.

A number of signals may be sent between two points simultaneously by making a slight modification in the receiver circuit (Figure 20). A second DG508A is used as a demultiplexer, allowing all 8 channels to be monitored continuously.

Often information is multiplexed into a conversion system which has a relatively slow processing time, necessitating a sample-and-hold after the multiplexer. Using the DG508A as a sample-and-hold switch combines both functions, as shown in the "one of eight sample-and-hold" circuit (Figure 17).

## Overvoltage

In certain applications the analog signal may exceed +15 V, or be present when the power supplies are off. This is a condition known as overvoltage, and it can present problems unless certain precautions are taken.

When the analog voltage exceeds the supply voltage, the source-body junction will forward bias, as shown in Figure 18. Current will flow from the signal source into the supply. If the current source capability of the

signal source and the current sink capability of the power supply are each greater than 20 mA, a resistor should be connected in series with source to limit the current.

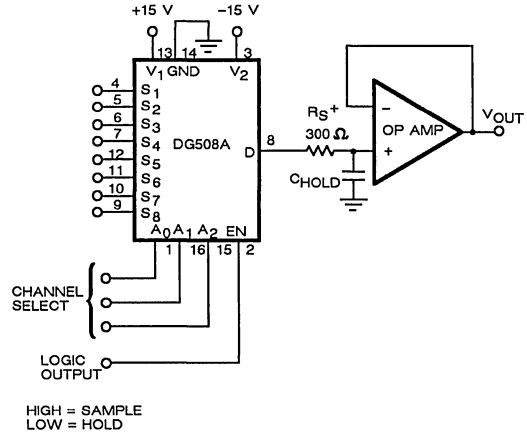


Figure 17. A One of 8-channel Sample and Hold

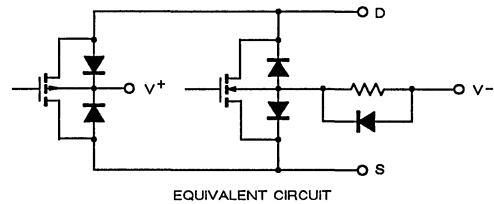
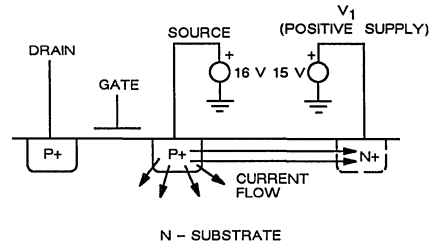


Figure 18. Current Paths During An Overvoltage Condition

If the analog signal is present when the supplies are off, diodes in series with the supplies will allow the supply pins to float and prevent excessive current from flowing. A DG508A with full overvoltage protection is shown in Figures 21a and 21b.

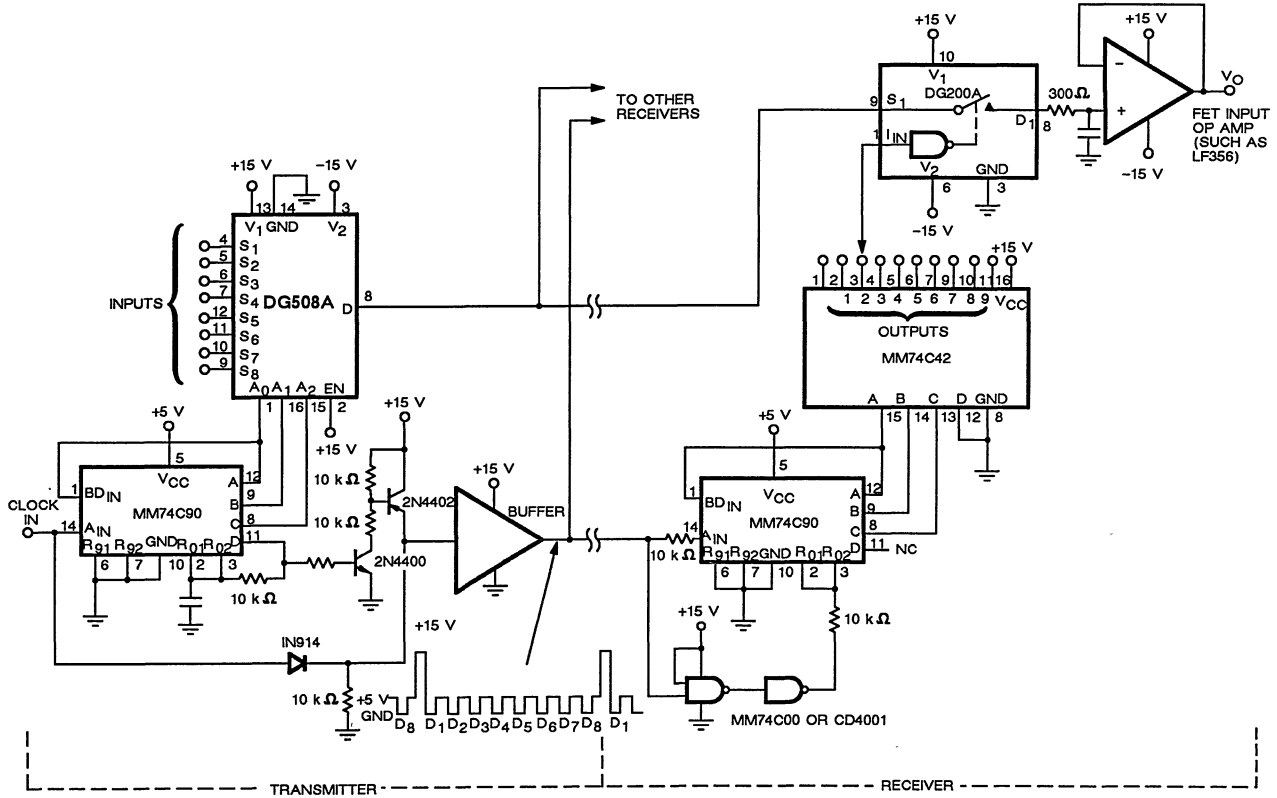


Figure 19. A One of 8-channel Transmission System



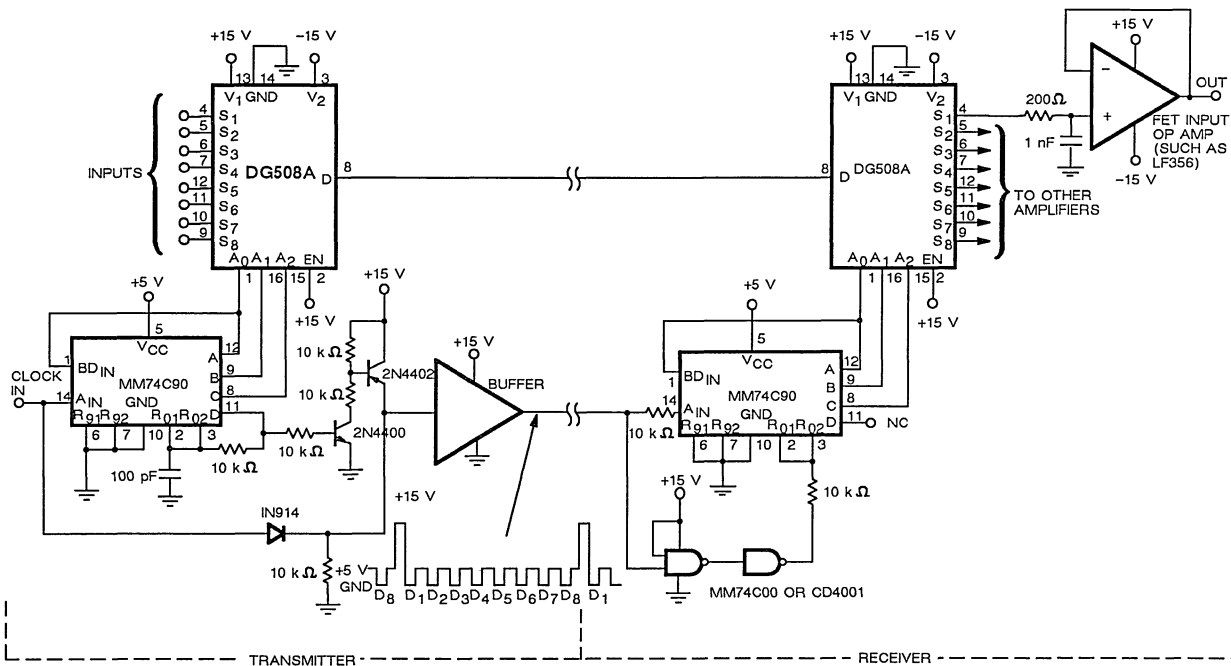
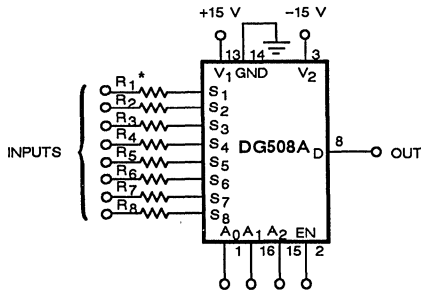


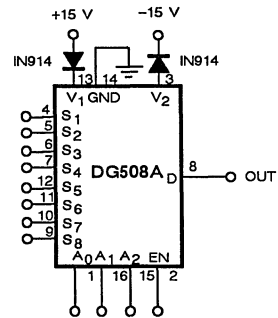
Figure 20. An 8-channel Mux/Demux System



$$* R_1 \text{ THROUGH } R_8 = \frac{\text{EXPECTED OVERVOLTAGE} - 15 \text{ V}}{20 \text{ mA}}$$

EXAMPLE:  $R = 250 \ \Omega$  WHEN  $V_{S(\text{MAX})} = 20 \text{ V}$

(A) A DG508A Protected Against Analog Signals Which Exceed 15 V



(B) A DG508A Protected Against Analog Voltages Being Present When the Power Supplies are OFF

**Figure 21.** Overvoltage Protection (shown for DG508A) is Normally Used Only When the Analog Voltage Exceeds the Power Supply Voltages, and the Signal Source is Capable of Generating Greater than 20 mA.

## 2-Level Multiplexing

When a large number of channels are multiplexed, the outputs of two or more multiplexers can be connected together and each multiplexer sequentially enabled. In the INHIBIT mode the multiplexer draws less power and its output and inputs act as open circuits. Theoretically, an infinite number of channels can be accommodated in this way; in practice the accumulated output capacitance and leakage of many paralleled multiplexers limits the speed and accuracy of the system. A much better method is the two level multiplex system, shown in Figure 22. The two level system has a bank of high speed switches at the output which sequentially switch between the 4 DG506A's. Each DG506A is able to switch during the time the other 3 are being interrogated, and they contribute leakage and capacitance at the output only when they are switched on by the DG181 (1/4 of the time). This circuit has several important advantages over a multi-unit single-level system, such as:

1. The switching speed of the system is dependent on the DG181, which is a high speed 2-channel SPST ( $t_{\text{ON}} \sim 150 \text{ ns}$ ). The slower switching time

of the DG506A ( $\sim 1 \ \mu\text{s}$ ) is not important because this switching transition can take place while the other DG506A's are being interrogated. In this way a very fast multiplex system can be made with a large number of low cost, moderate speed multi-channel multiplexers and several high speed SPST switches.

2. The output capacitance of the 2-level system is much lower than that of the single level. It consists of a single DG506A (40 pF) and several DG181's (6 pF OFF, 15 pF ON) which is much less than several DG506A's in parallel. If 64 channels are multiplexed, for instance,  $C_{\text{OUT}}$  of the 2-level system would be 72 pF, vs 160 pF for the single-level system.
3. The output leakage current is reduced by a similar amount. (From  $\pm 40 \text{ nA}$  to  $\pm 10 \text{ nA}$  in a 64-channel system).

The two level multiplex system is very useful in communications links, high speed interfacing with comparators, or wherever a large number of channels must be multiplexed at high speeds.<sup>1</sup>

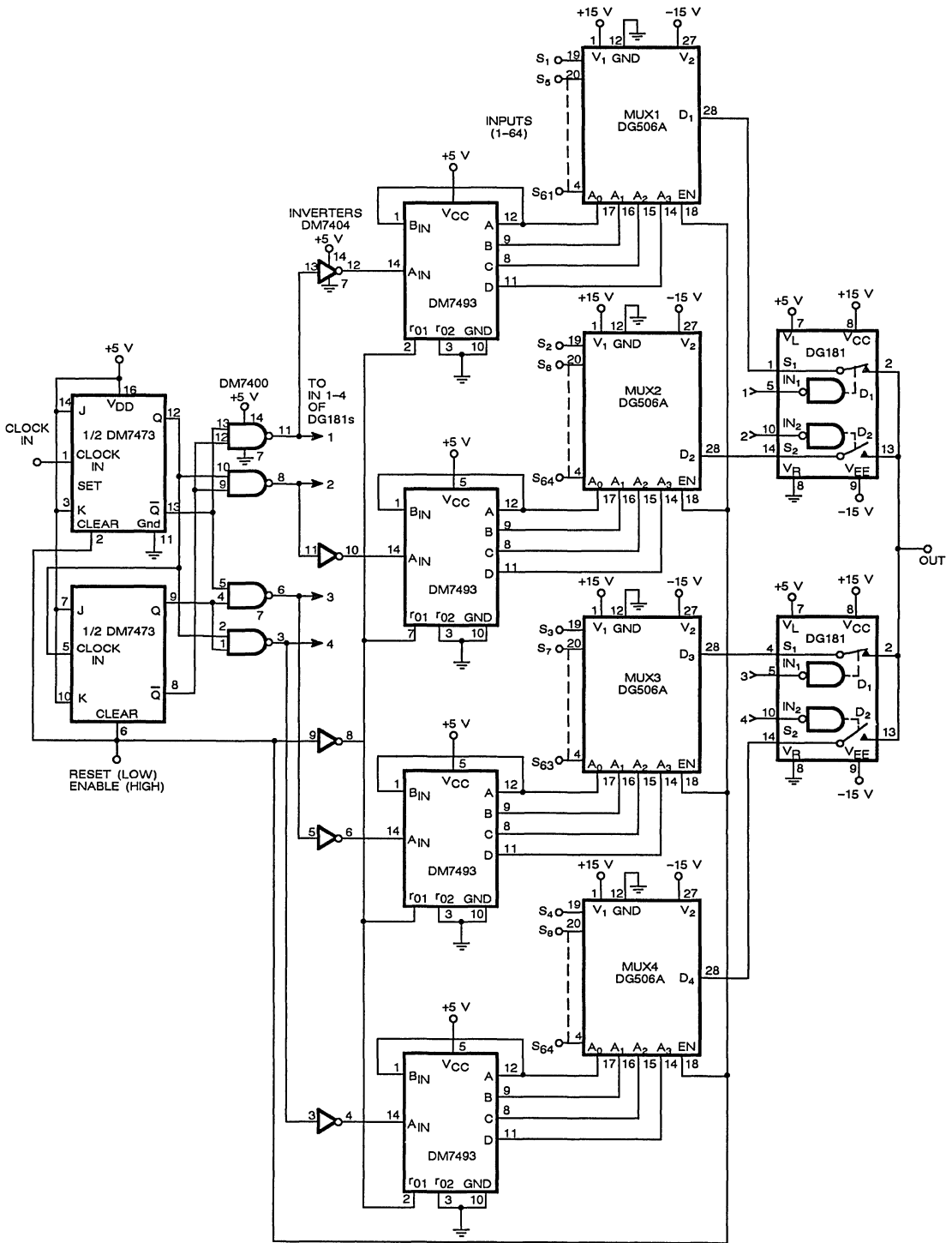


Figure 22. 64-Channel 2-Level Multiplex System

## Low Level Multiplexing

When multiplexing low level signals, extra care must be used because the signal may be masked by ac noise pickup and dc voltages generated by thermocouple effects at the connections of dissimilar metals. Much greater accuracy is obtained if the signal is handled differentially, so that ac noise and dc thermocouple effects appear as common-mode signals which can eventually be rejected. For this reason a line of differential multiplexers is available which allows improved thermal tracking and differential cancellation of leakage and switching glitches.

Figure 23 shows a thermocouple representation of a typical multiplexer mounted in a socket. If connection  $J_{1S}$  is at the same temperature as connection  $J_{1D}$ , then  $V_{1S} = V_{1D}$ . If all "S" junctions are at the same temperature as the corresponding "D" junctions, the total voltage across the multiplexer is zero. Conversely, if a temperature imbalance exists between side "S" and side "D" then the voltages will not exactly cancel and a net error voltage will appear. For this reason the multiplexer and associated connections should be mounted in a thermally-stable environment, away from hot components and with as few drafts around the chip as possible. When a DG509A is mounted in a thermally-stable environment, the

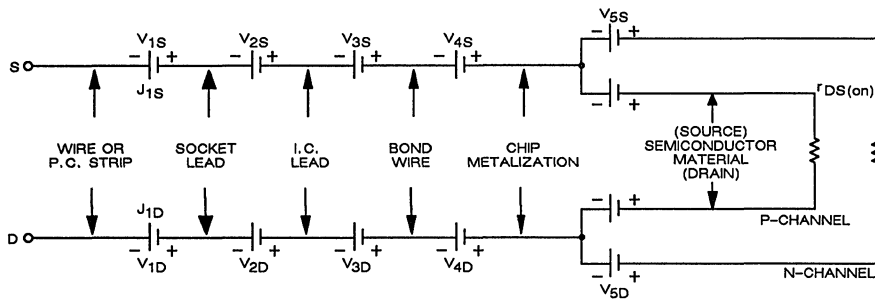


Figure 23. Thermocouple Representation of a Typical Multiplexer Switch (73)

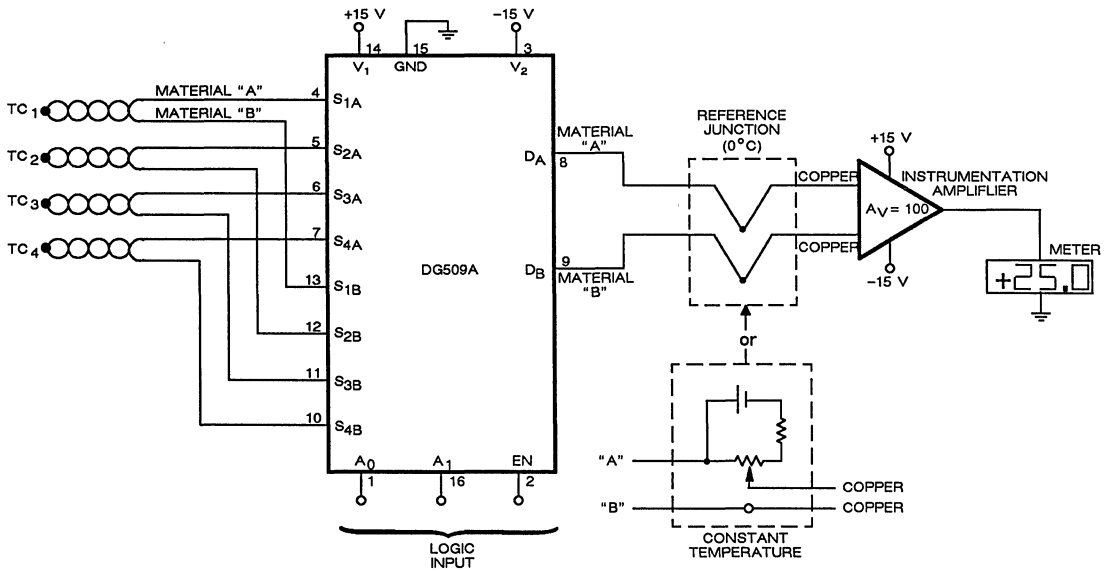
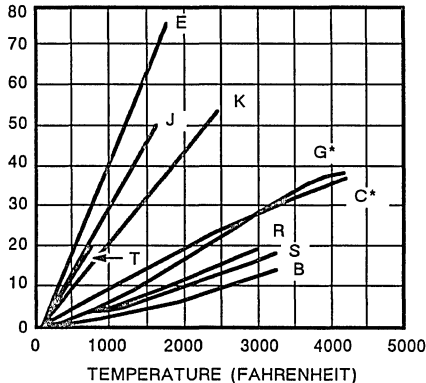


Figure 24. A Thermocouple Multiplex System (73)

typical error developed across the switch is about  $\pm 3 \mu\text{V}$  over the operating temperature range of the device. In free air, with random room drafts, it can be as high as 7 to 10  $\mu\text{V}$ . When heated with a thermal probe at 85°C (resulting in uneven temperature across the device) the absolute voltage across a switch is about 100  $\mu\text{V}$  with a 30  $\mu\text{V}$  differential error. IC multiplexers are therefore ideal in low level applications if care is exercised to insure an even temperature.

Figure 24 shows a DG509A thermocouple multiplexer. To decouple the sensors from the meter amplifier, either a reference junction at 0°C or a bucking voltage set at room temperature may be used. The latter method is simpler, but is sensitive to changes in ambient temperature. Table I shows the output of several common types of thermocouples versus temperature.<sup>2</sup>



**Table 1.** Output Voltage vs. Temperature of Several Common Thermocouples

## REFERENCES

- (1) J.O.M. Jenkins, "IC Multiplexer Increases Analog Switching Speeds," Siliconix Application Note AN73-2, February 1973.
- (2) The Omega Temperature Measurement Handbook(1975), Omega Engineering, Inc., Stamford, Conn.

## ANSI SYMBOL

T	Copper vs Constantan
E	Chromel vs Constantan
J	Iron vs Constantan
K	Chromel vs Alumel
G*	Tungsten vs Tungsten 26% Rhenium
C*	Tungsten 5% Rhenium vs Tungsten 26% Rhenium
R	Platinum vs Platinum 13% Rhodium
S	Platinum vs Platinum 10% Rhodium
B	Platinum 6% Rhodium vs Platinum 30% Rhodium

\*Not ANSI Symbol

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# ANALOG SWITCHES IN SAMPLE-AND-HOLD CIRCUITS

Gary Dixon  
Revised January 1988

## INTRODUCTION

In many cases the designers of sample-and-hold circuitry have relied upon "cut-and-try" methods to achieve good circuit performance. This Application Note provides analytic design information regarding sample-and-hold circuitry and practical design examples.

FET analog switches will meet the basic performance requirements for sample-and-hold circuitry. The criteria for choosing a given FET analog switch may seem rather simple since many of the dc data sheet parameters are similar from one switch or from one technology (JFET, PMOS, or CMOS) to another. However, the dynamic features of a switch are the primary characteristics that must be examined. This task is not easy since any measurement assumes a given set of conditions and circuitry. This Application Note will consider two major characteristics of FET analog switches. The first area is that of the large current-handling characteristics of various switches, which can have a pronounced effect on circuit settling times. The second subject involves the offset characteristics of sample-and-hold circuits which may affect the basic accuracy of system design.

For high speed sample-and-hold circuits, the large current handling capabilities of the switch can play an important role in determining settling time. As a rule, the data sheet specifications for switch ON resistance are made at low current levels, such as those found in analog signal coupling circuits. When an analog switch is required to charge a capacitor, the switch may be required to handle large instantaneous currents and voltages. The switch dynamic characteristics will vary depending upon the type of switch and the drive circuitry used.

Of the many JFET switches, the DG181-191 series is recommended for its low ON resistances and its eas-

ily determined high current characteristics. Figure 1 illustrates that the DG181, a 30  $\Omega$  device, typically enters  $I_{DSS}$  limiting at 80 mA. Further investigation indicates the DG182, a 75  $\Omega$  device, typically encounters current limiting at 30 mA. If we compare the DG181 with a CMOS device, the DG200A, we will find the DG200A has a somewhat more resistive characteristic. The DG411 series of silicon gate analog switches rivals JFET's low ON resistance and fast speeds plus offering a full  $\pm 15$  V input signal range with very low power dissipation.

Figure 2 shows the resistance characteristics of a PMOS switch, the DG172. The average ON resistance for settling purposes may be assumed to be between the minimum resistance at the most positive signal excursion and the maximum ON resistance at the most negative excursion.

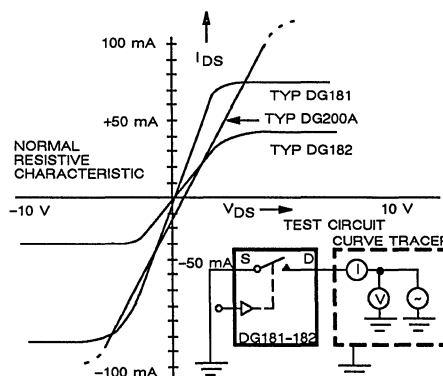


Figure 1. Current Characteristics of JFET Analog Switches (DG181 and DG182) and a CMOS Switch the DG200A

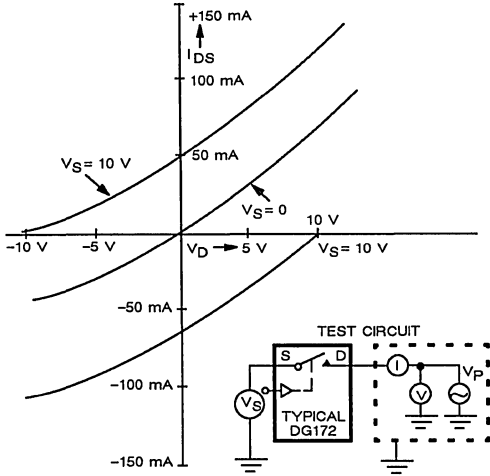


Figure 2. Characteristics of a PMOS Analog Switch

Figure 2 is based on a negative supply voltage to the DG172 of  $-20$  V. If the supply were  $-15$  V, the currents through the switch would decrease, which is a disadvantage of PMOS. The DG181 current is independent of supply voltage, while the DG200A is designed to work with  $\pm 15$  V supplies.

Let us now turn to the second subject to be covered, that of switch charge transfer or charge injection. In the past, this subject has been called switching transients, "glitches", and various other names. Switching transients affect the intrinsic accuracy of any sample-and-hold design. During the sample interval, the capacitor charges to the sample voltage. Then during the transition from sample to hold, an offset voltage is introduced into the charged capacitor. The major phenomenon is that of a capacitive voltage divider formed by the capacitive coupling between the control gate with its associated switch terminals and the storage capacitor, as shown in Figure 3.

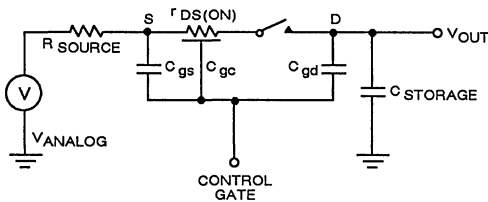


Figure 3. Equivalent Switch Circuit

Charge transfer characteristics will vary to quite an extent, depending upon various switch and circuit configurations. To provide a method of comparison for various switches, the preferred terminology is charge transfer presented in pico coulombs.

Charge transfer (Pico Coulombs) = Voltage offset x Hold capacitance (Pico Farads).

The DG181 series of JFET switches provides very good transient coupling characteristics. One of the reasons for this performance is the decrease in gate voltage swing, because the FET gate is initially clamped at the analog voltage. The JFET construction also provides an optimization of low coupling capacitance along with low ON resistance. If we now compare a PMOS switch with the JFET characteristic we are able to see a major difference.

As may be seen from the two curves of Figures 4 and 5, the charge transfer characteristics for the DG181 and DG172 are similar at  $C_L = 100$  pF and  $R_S = 0$ . It should be noted, however, that the DG172 has a typical ON resistance of  $200 \Omega$ , an increase in ON resistance of 6 times more than that of the DG181. For values of capacitance greater than  $100$  pF, the charge transfer characteristics of the DG172 are seen to be inferior to those of the DG181. The major factor which causes the storage capacitance to be value-dependent is the large distributed gate-to-channel capacitance, plus the related circuit time constants.

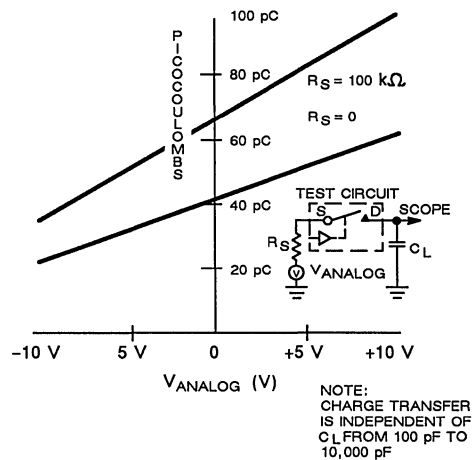


Figure 4. Typical Charge Transfer Characteristic of the DG181 JFET Switch

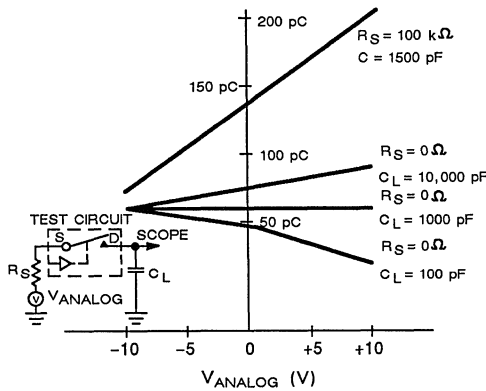


Figure 5. Typical Charge Transfer Characteristics of the DG172 PMOS Switch

CMOS devices provide an improvement over the JFET and PMOS devices since two gates with complementary control signals are involved. The two resulting “glitches” tend to cancel each other. The transient is therefore greatly reduced but is not eliminated due to design compromises. This is shown in Figure 6.

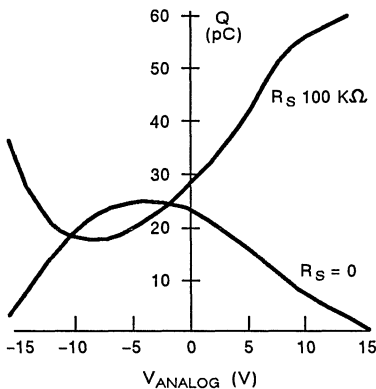


Figure 6. CMOS Charge Transfer Characteristics

When the various tradeoffs are considered, the DG181-191 family and DG411 series of analog switches provide the best overall performance for critical sample-and-hold designs. This is due in large part to their fast (150 ns) switching speeds, which allows a fast aperture time. The CMOS DG200A se-

ries comes in a distant third, with its somewhat slower switching speed (1000 ns) and higher ON resistance.

### Inverting DG181 Sample-and-Hold Circuit

The inverting sample-and-hold circuit has several inherent advantages over the other design approaches. The switch operates at a constant voltage each time, thus reducing the aperture time jitter considerably. The input configuration reduces surge currents that are usually supplied by the signal source. A slight disadvantage of this circuit is the requirement that the two feedback resistors be matched to obtain reasonable accuracy. The feedback resistance value must be carefully chosen so that the amplifier output does not enter a current-limiting mode. General purpose amplifiers with a 20 mA limit will operate with a 5 kΩ feedback network. The linear time response of the circuit is determined by the time constant ( $R_f + 2 R_{sw} C_L$ ). In this example,  $R_{sw} < R_{fi}$ ; therefore, the settling time is determined by the feedback resistance. This circuit is current-limited by the amplifier and the feedback resistance, so the large current characteristics of the switch are of little importance. The circuit is also limited by the slew rate of the amplifier. If a 1500 pF storage capacitor is used, the amplifier slew rate should be greater than 2.7 V/μs. If, as shown in Figure 7, an LM101A op amp is used (with a slew rate of 0.5 V/μs, an additional 25 μs will be required during slew rate limiting. For the circuit shown, an acquisition time of 98 μs was measured for a swing of 20 V settling into a 1 mV error band. If we now turn the task of determining the sample-to-hold offset, we must first examine the charge transfer characteristics of the switch. Since the source resistance is 5 kΩ; which is much greater than the 30 Ω  $r_{DS(ON)}$ , we must examine the characteristics near the high impedance curves ( $R_S = 100$  kΩ) on the charge transfer chart of Figure 4. The DG181 provides an offset voltage of 43 mV. The DG200A may be used in this circuit with a voltage jump of 18 mV. If a DG172 switch is used a 91 mV jump should be expected.

### Improved DG181 Inverting Sample-and-Hold Circuit

If these foregoing charge transfer errors are too large for practical use, several methods of reducing the charge transfer are possible. The first method involves increasing the capacitor size which improves the droop rate, but also requires a direct trade-off of accuracy versus speed. A second method involves



reducing the size of the switching FET, which also decreases charge transfer but increases the ON resistance. This method also requires that a trade-off be made due to the relationship of speed versus accuracy. A third and more practical method is to compensate for the charge transfer. Many circuits have been proposed in the past which vary from simple capacitors in logic circuitry to rather complex systems. The inverting sample-and-hold circuit is rather easy to compensate since it operates at a single voltage level. The basic concept involves an equal but opposite direction of the FET gate voltage. A rather unique circuit using this principle uses the two switches normally found in analog switch packages.

The compensation circuit shown in Figure 8 employs three additional components ( $R_3$ ,  $C_2$  and  $C_3$ ) to provide total offset errors which are adjustable to much less than 1 mV. One feature that the DG181 device offers is a 20% larger charge transfer from the  $D_2$  terminal. This actually makes compensation much easier since only one side of the network must be adjusted. With other switches (such as the DG200A) parameter variations may require that hold capacitors of two different sizes be used to provide adjustability. An added feature of this circuit configuration of Figure 8 is a net reduction in the system droop due to a balancing effect of the leakage currents.

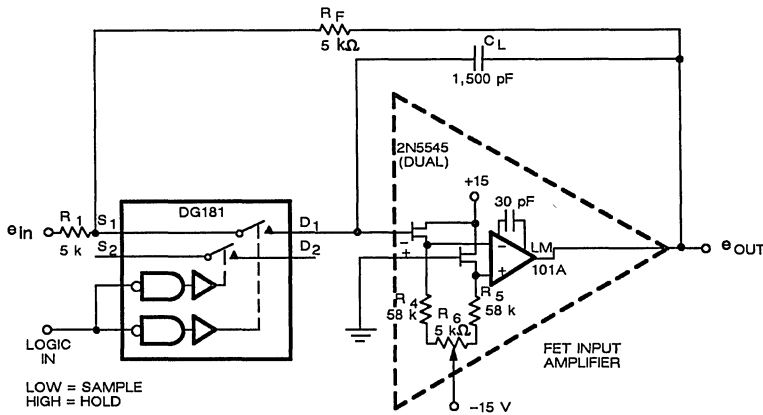


Figure 7. Inverting Sample & Hold Circuit

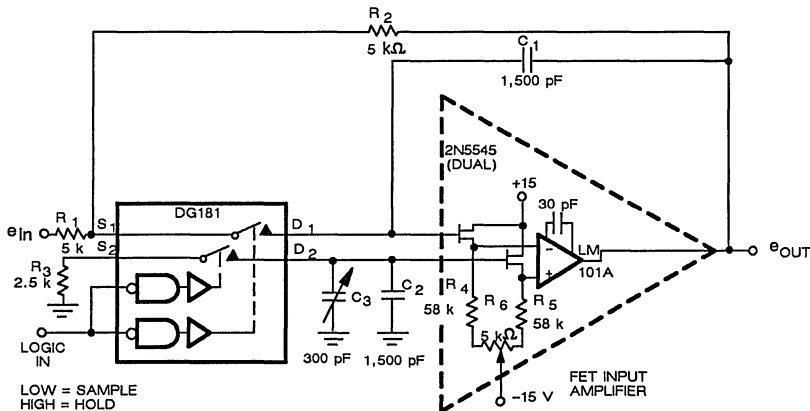


Figure 8. Improved Inverting Sample and Hold Circuit

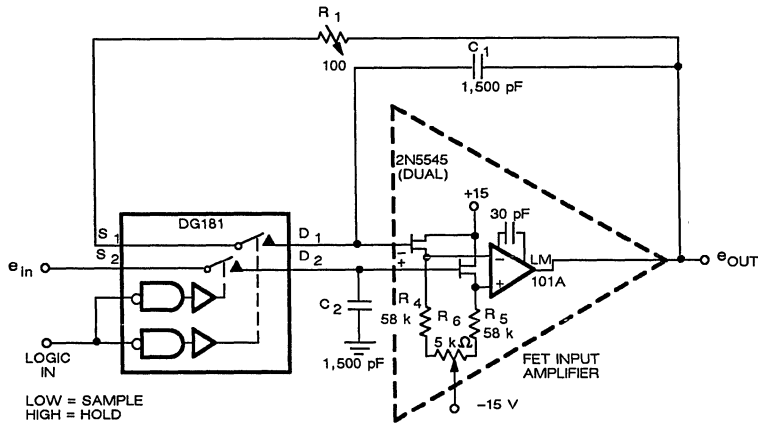


Figure 9. High Performance Non-Inverting Sample-and-Hold Circuit

### High Performance DG181 Non-Inverting Sample-and-Hold Circuit

For those designers who require much faster settling times, the high-performance sample-and-hold circuit shown in Figure 9 should be used.

As mentioned previously the DG181 JFET switch provides the best combination of settling speed and inherent charge transfer accuracy.

A typical DG181 analog switch is capable of charging a 1500 pF capacitor in 500 ns to within a 1 mV error band for a 20 V swing. This statement assumes that the signal source is able to supply the capacitor charging current of 80 mA (zero source impedance).

The offset is adjusted to zero offset for zero analog signal by changing  $R_1$ , which also provides a normalization for both source impedance and the differential charge transfer characteristic between switches. The offset varies with analog voltage from +1.4 mV at 5 V to -1.5 mV at -5 V. This reduction provides an order-of-magnitude improvement over an uncompensated circuit. In general, for the faster sample-and-hold cir-

cuits which use the non-inverting technique, the charge transfer may be adjusted to zero at one voltage only. The compensated inverting sample-and-hold approach will provide much better offset characteristics, but a sacrifice in overall speed. The non-inverting sample-and-hold circuit, however, has the disadvantages of CMRR gain errors and the source may be loaded with large sampling-surge currents.

### High-Quality DG201A Sample-and-Hold

Figure 10 shows a high-quality sample-and-hold using DG201A. The LM101A provides gain and buffers the input from storage capacitor  $C_2$ .  $R_2$  adds a zero in the open loop response to compensate for the pole caused by the switch resistance and  $C_2$ , improving the closed loop stability.  $R_1$  provides a slight delay in the digital drive to pins 1 and 9.

$C_1$  provides cancellation of coupled charge, keeping the sample-to-hold offset below 5 mV over the analog signal range of -10 to +10 V. Aperture time is typically 1  $\mu$ s, the switching time of the DG201A. Acquisition time is 25  $\mu$ s, but this can be improved by using a faster slewing op amp. Droop rate is typically less than 5 mV/sec at 25°C.

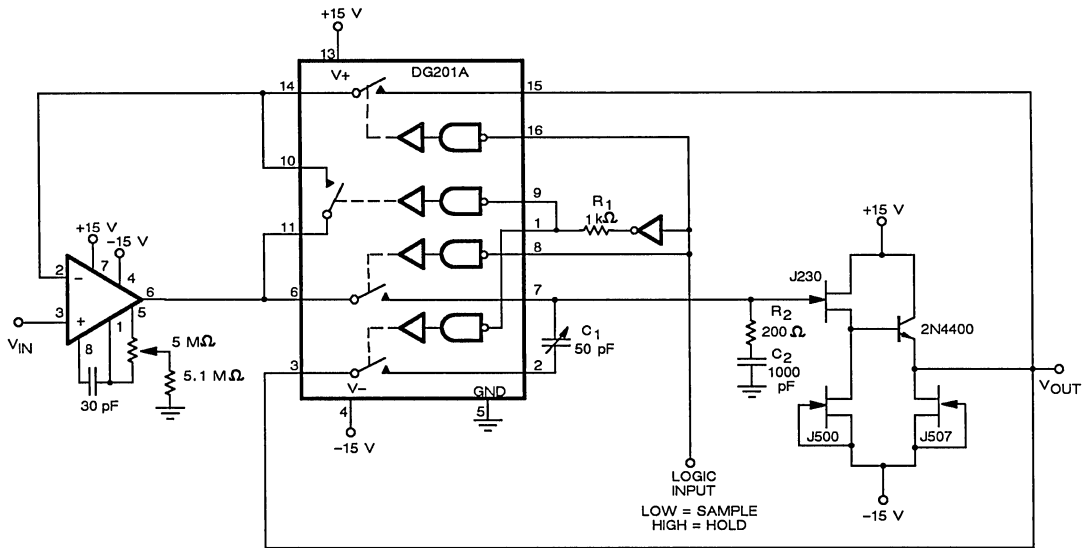


Figure 10. DG201A Sample-and-Hold

### A Fast Sample-and-Hold

Figure 11 shows a circuit where the addition of SW1 improves accuracy and settling time by putting the voltage drop across SW2 inside the feedback loop.

Acquisition times are as fast as those attainable with the DG181 and accuracy is improved thanks to the low charge injection characteristics of the DG411. The DG411 is characterized and specified for single supply operation and has ESD protection on all pins.

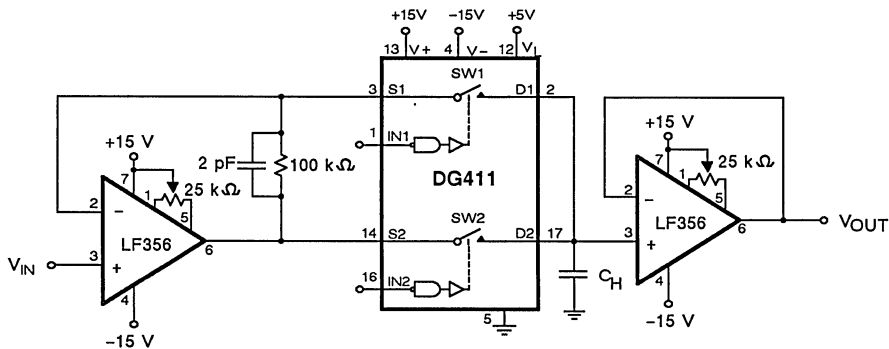


Figure 11. Fast Sample and Hold

In Figure 12 the switching transients are attenuated by synchronizing the turn-ON and turn-OFF times of one switch with those of another.

Figure 13 is a charge injection compensated sample-and-hold with less than  $\pm 5$  pC of charge transfer ( $< 5$  mV offset when  $C_L = 1,000$  pF).

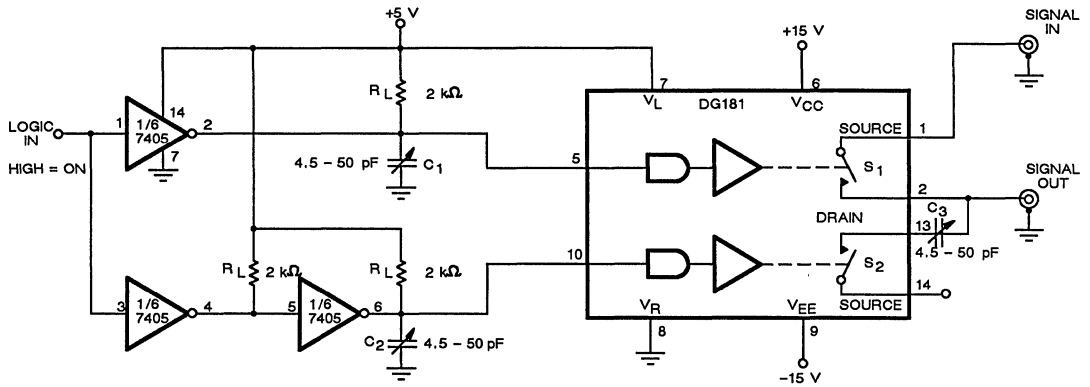


Figure 12. Attenuating Switching Transients

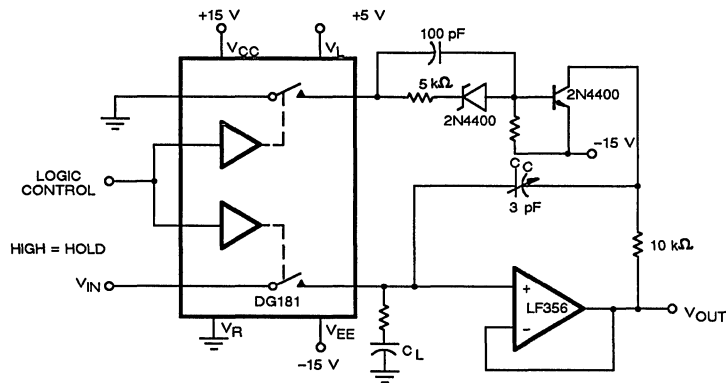


Figure 13. Charge Compensated Sample-and-Hold

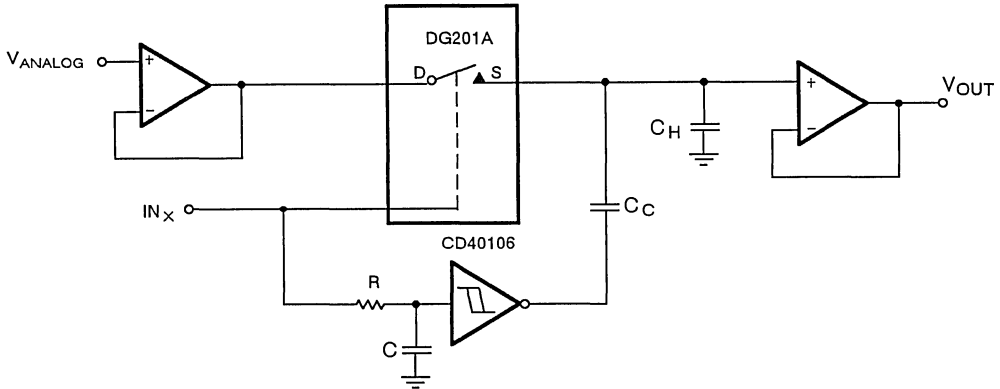


Figure 14. Simplified Compensation Method

Figure 14 is another inexpensive charge injection compensation circuit that can be tailored to get a good first order compensation. The values of  $R$  and  $C$  are chosen to obtain the proper timing.  $C_C$  is sized to dump the proper amount of compensation charge onto the hold capacitor.

**REFERENCES**

- (1) Lee Shaeffer, "CMOS Analog Switches – A Powerful Design Tool," Siliconix Application Note AN75-1, July 1975.

# FUNCTION/APPLICATION OF THE L144 PROGRAMMABLE MICROPOWER TRIPLE OP AMP

## INTRODUCTION

The L144 is a monolithic triple operational amplifier circuit with an external programming feature for power dissipation and input bias current control. It finds application in RC active filters, amplifiers, micropower comparators, and numerous general signal processing circuits. The L144 is a practical op amp wherever low current drain, low voltage, low power, or very small physical size are the controlling criteria.

This Application Note describes the L144, how to program it, what the effects of slew rate limiting are, and some practical circuit applications.

The L144 has three operational amplifiers programmed by one external current setting resistor. It operates from power supplies ranging from  $\pm 18$  V to as low as  $\pm 1.5$  V with quiescent supply currents from  $10 \mu\text{A}$  to greater than  $1 \text{ mA}$  independent of supply voltage. The schematic shown in Figure 1 reveals a general-purpose PNP input transistor op amp with an

outstanding difference. The master bias current is not set by an internal resistor strung from  $V+$  to  $V-$ , but is brought out to an external pin. This allows the user to determine the operating currents of each stage through a system of current mirrors. Of special interest to the designer are the equal collector currents of  $Q_1$  and  $Q_2$ , which are derived from the output of  $Q_4$ . These collector currents, divided by a beta of approximately 50, determine the input bias currents for each amplifier. The ratio between the set current and the collector current of  $Q_4$  is unity, which allows one to program the input bias current simply by changing the set current input of the device.

## Input Bias Current and Supply Current

The relationship between supply current, supply voltage, and the setting resistor is shown in the graph and set current model of Figure 2. The two diodes of the set current model correspond to the base-emitter junctions of  $Q_{16}$  and  $Q_{17}$ .

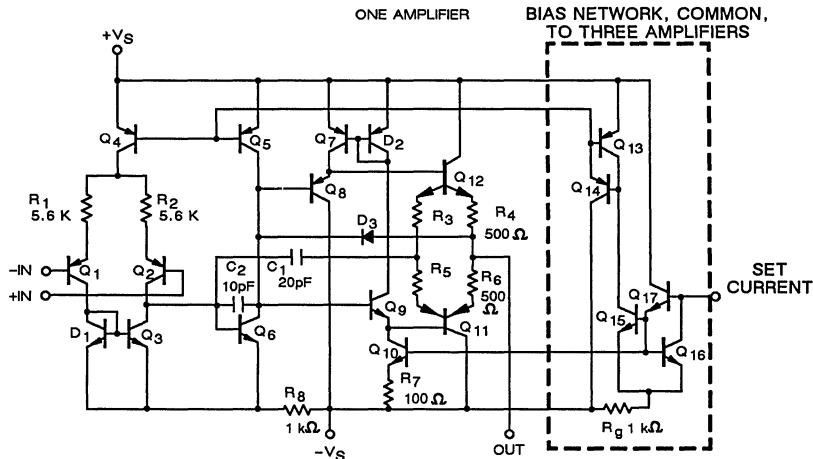
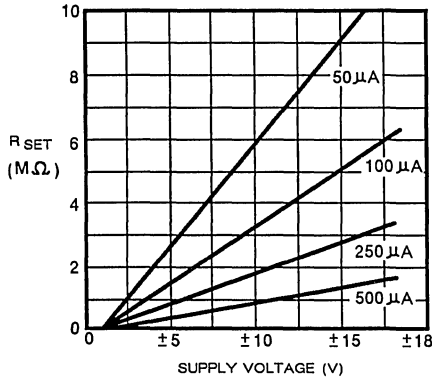


Figure 1. L144 Schematic



L144 SET CURRENT MODEL

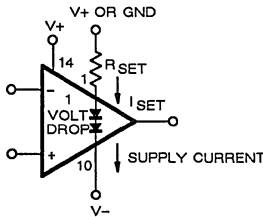


Figure 2. Supply Current vs Bias Resistor and Supply Voltage

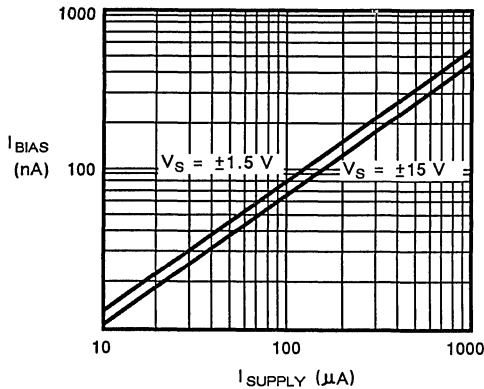


Figure 3. Input Bias Current vs. Supply Current

Figure 3 shows the essentially linear relationship between input bias current and total quiescent supply current for the L144. The low input bias currents at low supply current levels allow the L144 to maintain good input specifications even with the large feedback and load resistor values normally encountered in micropower applications.

The slightly lower input bias currents at the higher supply voltages are due to the narrower base width and higher beta encountered at  $V_S = \pm 15$  V.

**Frequency Response**

At the data sheet standard supply current of  $250 \mu\text{A}$  the typical Bode plot is as shown in Figure 4. The low frequency gain of approximately 95 dB rolls into a uniform  $-20$  dB/decade slope until after the 0 dB unity gain crossing point. The variation of open loop gain with temperature is typically  $-2$  dB per  $100^\circ\text{C}$  of temperature rise. The 600 kHz unity gain crossover gives a gain bandwidth product (GBWP) of 600,000. Figure 5 shows the variation of GBWP with supply current.

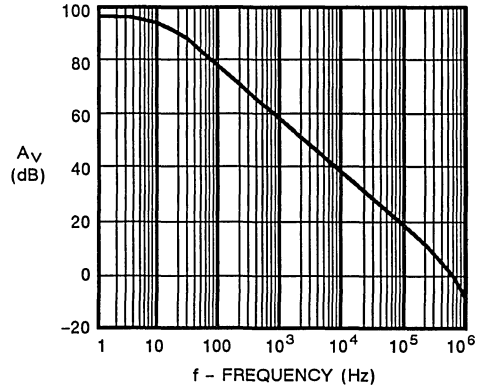


Figure 4. L144 Open Loop Gain vs. Frequency

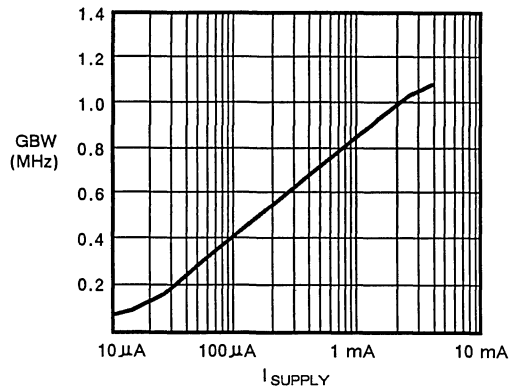


Figure 5. L144 Gain Bandwidth Product vs. Supply Current

The vertical axis is linear whereas the horizontal  $I_{CC}$  axis is logarithmic, demonstrating that the GBWP does vary with  $I_{CC}$ , but at much less than the 1-to-1 ratio observed for other parameters.

## Slew Rate

Slew rate is almost a direct function of supply current as shown in Figure 6. This follows from the fact that slew rate limiting is actually caused by the finite limits of the internal current sources (which charge and discharge the second stage compensation capacitor) varying with the externally-determined set current. An amplifier output changes from the small signal response shown on the Bode plot to a slew-rate-limited response when the rate of change of the output voltage exceeds the rate of change determined by the slew rate limit of the amplifier. Since the maximum rate of change of a sine wave is a function of peak amplitude it is possible to trade maximum frequency for peak signal amplitude when operating at low power dissipation levels. Figure 7 shows the derivation<sup>1</sup> of an equation relating slew rate  $S_R$ , sine wave amplitude  $V_{PEAK}$ , and frequency. The zero crossing of a sine wave is the point of maximum rate of change as shown after the derivative is taken and maximized. In both of the examples shown the maximum undistorted operating frequency is kept constant while juggling power dissipation, slew rate, and peak amplitude in an engineering tradeoff.

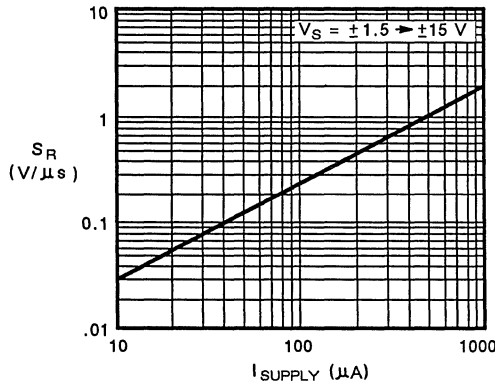
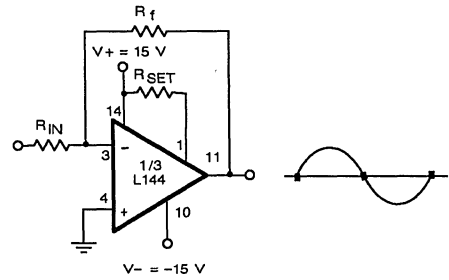


Figure 6. Slew Rate Limits vs. Supply Current



$$V_{OUT} = V_{peak} \sin 2\pi f t$$

$$\frac{dV_{OUT}}{dt} = V_{peak} 2\pi f \cos 2\pi f t$$

$$\left. \frac{dV_{OUT}}{dt} \right|_{t=0} = V_{peak} 2\pi f$$

$$S_R \equiv \frac{dV_{OUT}}{dt} \equiv \frac{V_{peak} 2\pi f}{\max}$$

$$I_{SUPPLY} = 820 \mu A, S_R = 1.5 V/\mu sec$$

$$P_D = 24 mW, V_{peak} = 10 V$$

$$f_{max} = \frac{S_R}{V_{peak} 2\pi} = 24 kHz$$

$$I_{SUPPLY} = 60 \mu A, S_R = 0.15 V/\mu sec$$

$$P_D = 1.8 mW, V_{peak} = 1 V$$

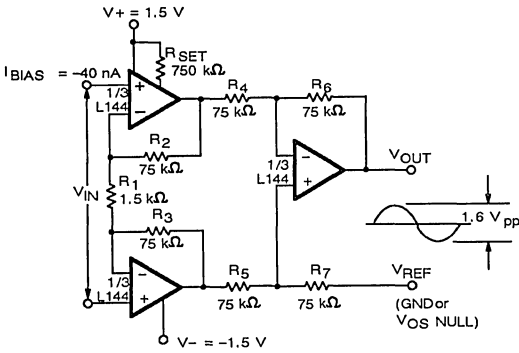
$$f_{max} = \frac{S_R}{V_{peak} 2\pi} = 24 kHz$$

Figure 7. Slew Rate Limiting

## Instrumentation Amplifier

Figure 8 shows a single L144 chip used to construct a three-amplifier classical instrumentation amplifier. The entire circuit consumes only 135  $\mu W$  of power from a  $\pm 1.5 V$  power supply. With a gain of 101 the instrumentation amplifier is ideal in sensor interface and biomedical preamplifier applications.





$$A_V = 1 + \frac{2R_2}{R_1} \quad P_D = 135 \mu W$$

$$V_{OS} \text{ (TYP) RTI} = 0.45 \text{ mV}$$

Figure 8. L144 Instrumentation Amplifier

The first stage provides all of the gain while the second stage is used to provide common mode-rejection and double-ended to single-ended conversion. The resistor  $R_1$  determines the gain of the circuit according to the equation:

$$A_V = 1 + \frac{2R_2}{R_1} \quad (1)$$

The reference point at the base of  $R_7$  can be used to determine the quiescent output voltage when there is

no differential input voltage. This provides an easy single point to zero any net offset voltage (typically 0.45 mV referred to input) and/or to insert a trim resistor to improve common mode rejection ratio (CMRR). The CMRR depends heavily on the match between  $R_4/R_6$  and  $R_5/R_7$  and can be nulled if  $R_7$  is broken into a resistor and a small-value trim potentiometer. Figure 9 shows the voltage gain and CMRR versus frequency for a typical instrumentation amplifier. The upper curve shows a calculated CMRR referred to input. The falloff and final rise in CMRR is due to the mismatch in gain rolloff between amplifiers in the first stage followed by a falloff in gain and consequent increase in rejection of the second stage.

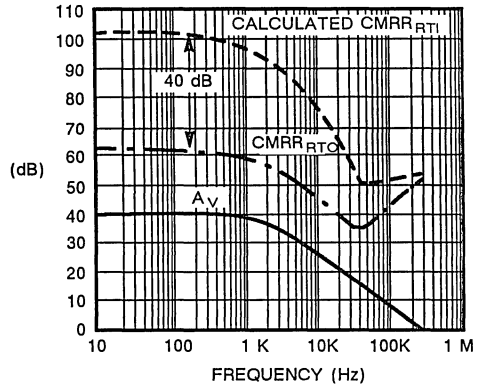
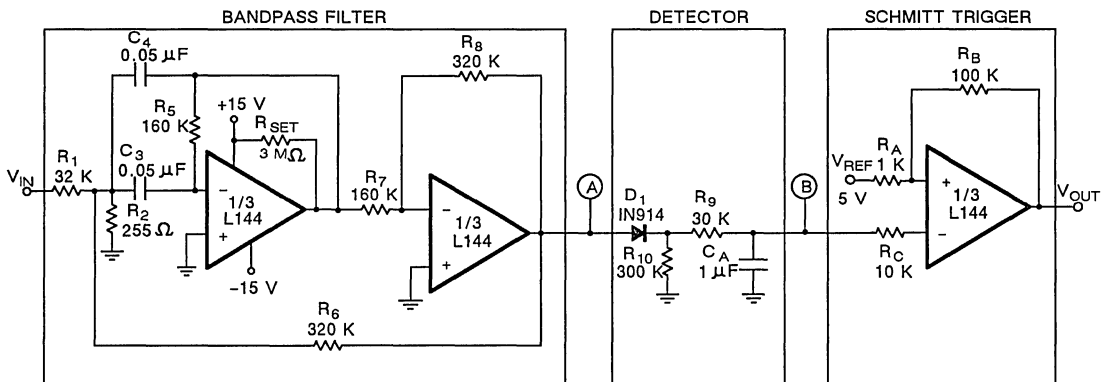


Figure 9. Common Mode Rejection Ratio and Gain vs. Frequency



$P_D = 7.5 \text{ mW}$

Figure 10. Tone Detector Circuit

## Tone Detector

Another example of a single L144 providing the amplifiers for an entire system is shown in Figure 10. This tone detector circuit is made up of a two-amplifier multiple feedback bandpass filter followed by an AC-to-DC detector section and a Schmitt Trigger. The bandpass filter (with a Q of 25) passes only 500 Hz inputs which are in turn rectified by D<sub>1</sub> and filtered by R<sub>9</sub> and C<sub>A</sub>. This filtering action in combination with the trigger level of 5 V for the Schmitt device insures that at least 55 cycles of 500 Hz input must be present before the output will react to a tone input. The actual integrating capacitor waveform shown in Figure 11 was taken with a 1 volt peak 500 Hz sine wave input. The ratio between capacitor C<sub>A</sub> charge and discharge is 1:11, due to resistors R<sub>9</sub> and R<sub>10</sub>.

For frequencies other than the 500 Hz center frequency shown in the example the relevant bandpass filter<sup>2</sup> equations are:

GIVEN:  $Q, f_o, H_o$   
(Q normally from 10 to 50) (2)

LET:  $C = C_3 = C_4$   
 $1 \leq k \leq 10$   
(k chosen for component value convenience) (3)

THEN:  $R_7 = \frac{Q}{2\pi f_o C}$  (4)

$R_7 = R_5$  (5)

$R_1 = \frac{kR_7}{H_o}$  (6)

$R_2 = \frac{R_7}{Q^2 - \frac{H_o + 1}{k}}$  (7)

$R_8 = kR_7 = R_6$  (8)

In the example shown in Figure 10 the chosen value of  $k = 2$  and the passive components used resulted in a measured Q of 23.1. The center frequency of

495.7 Hz and  $H_o$  of 9.9 were close to the calculated values of 500 Hz and 10.

The detector RC was designed to have a 3 dB down frequency of:

$$f_{3dB} = \frac{f_o}{100} \quad (9)$$

while the Schmitt trigger operated around the reference voltage with trip points determined by:

$$V_{HIGH} = \frac{V_{REF} R_B + 14 R_A}{R_A + R_B} \quad (10)$$

$$V_{LOW} = \frac{V_{REF} R_B - 14 R_A}{R_A + R_B} \quad (11)$$

where  $\pm 14$  V is the output swing with  $\pm 15$  V supplies. The measured trip points agreed with the calculated values of 5.089 V and 4.81 V within 0.2% in the circuit of Figure 10.

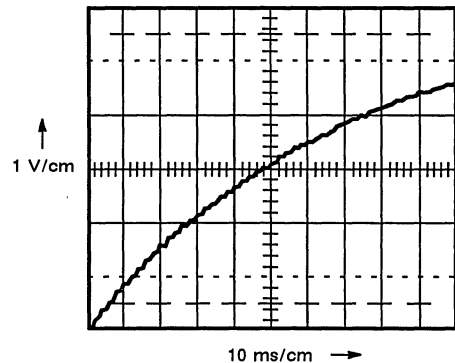


Figure 11. Detector Output Voltage vs. Time

## 3 Amplifier Active Filter

The active filter shown in Figure 12 is a state variable filter with band-pass, high-pass and low-pass outputs. It is a classical analog computer method of implementing a filter using three amplifiers and only two capacitors. With the L144 triple op amp it becomes cost-effective to use this configuration with its attendant high Q values and low sensitivities.<sup>3</sup>

The practical maximum value of Q is:

$$Q_{\max} = \frac{A_{f_0}}{3} \quad (12)$$

where  $A_{f_0}$  is the open loop gain of amplifier  $A_1$  at the resonant frequency.

The controlling design equations are:

GIVEN: Q,  $f_0$ , and  $H_0$  (bandpass output) (13)

LET:  $R_5 = R_6 = R_7, C_1 = C_2$  (14)  
(Chosen for component value convenience)

THEN:

$$\frac{R_4}{R_3} = 3H_0 - 1 \text{ for } H_0 \ll \frac{A_{f_0}}{3} \quad (15)$$

$$R_2 C_2 = \frac{H_0}{2\pi f_0 Q} \quad (16)$$

$$R_1 C_1 = \frac{Q}{2\pi f_0 H_0} \quad (17)$$

The design example shown in Figure 12 was calculated as follows:

LET:  $Q = 26$   
 $f_0 = 1 \text{ kHz}$   
 $H_0 = 26$  (18)  
 $R_5 = R_6 = R_7 = 20 \text{ k}$   
 $C_1 = C_2 = 0.008 \mu\text{F}$   
 $R_3 = 10 \text{ k}$

THEN:

$$R_4 = (3H_0 - 1) R_3 = 770 \text{ k} \approx 750 \text{ k} \quad (19)$$

$$R_2 = \frac{H_0}{2\pi f_0 Q C_2} = 19.9 \text{ k} \approx 20 \text{ k} \quad (20)$$

$$R_1 = \frac{Q}{2\pi f_0 Q H_0 C_1} = 19.9 \text{ k} \approx 20 \text{ k} \quad (21)$$

giving an actual calculated  $f_0$  and  $H_0$  of

$$H_0 = 1/3 (1 + \frac{R_4}{R_3}) = 25.3 \quad (22)$$

$$f_0 = \frac{Q}{2\pi R_1 C_1 H_0} = \frac{H_0}{2\pi R_2 C_2 Q} = 994.7 \text{ Hz} \quad (23)$$

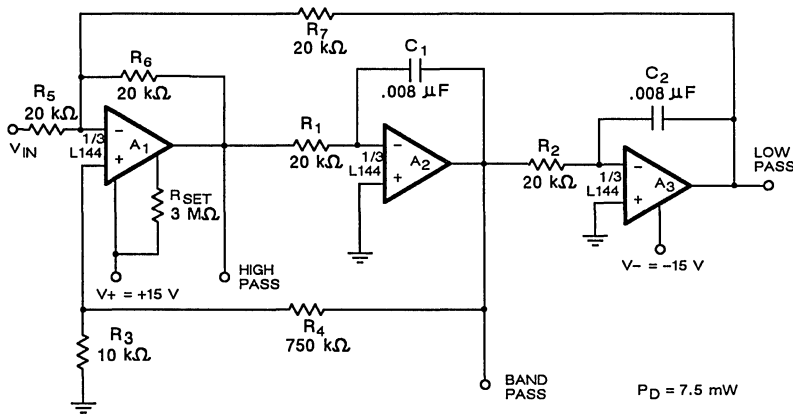


Figure 12. 3 Amplifier Active Filter

The measured values of  $Q$ ,  $H_O$ , and  $f_O$  using 1% components were 26.9, 26.3 and 996 respectively. Figure 13 shows the Bode plots of the high-pass, band-pass, and low pass outputs.

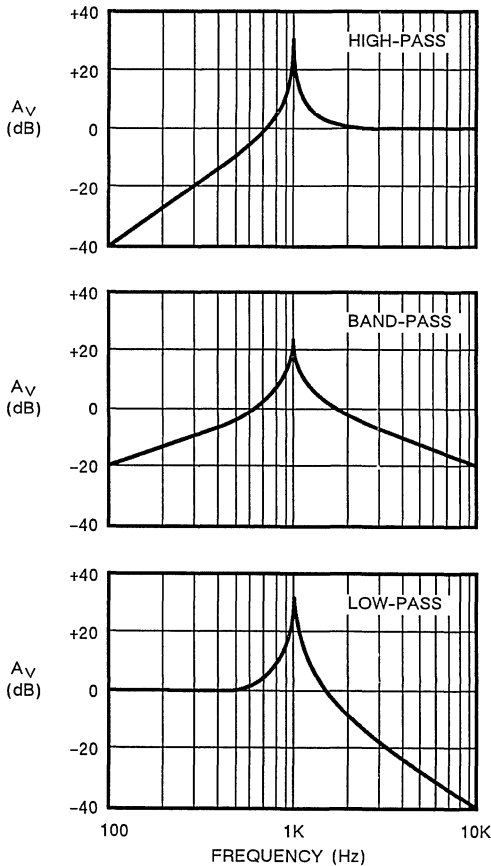


Figure 13. Bode Plots of Active Filter Output

## Micropower Double-Ended Limit Detector

The double-ended limit detector shown in Figure 14 uses three sections of an L144 and a CD4011 type CMOS NAND gate to make a very low power voltage monitor. If the input voltage  $V_{IN}$  is above  $V_{HIGH}$  or below  $V_{LOW}$  the output will be a logical high. If (and only if) the input is between the limits will the output

be low. The  $1\text{ M}\Omega$  resistors  $R_1$ ,  $R_2$ ,  $R_3$  and  $R_4$  translate the bipolar  $\pm 10\text{ V}$  swing of the op amps to a 0 to 10 V swing acceptable to the ground-referenced CMOS logic.

Total power dissipation is typically  $290\ \mu\text{W}$  while in limit and  $330\ \mu\text{W}$  while out of limit. Within the  $\pm 9\text{ V}$  input range of the circuit the comparator resolution is typically 2 mV with the offset adjust determined by trimming  $V_{HIGH}$  and  $V_{LOW}$ . Since the L144 is operating at only  $14.5\ \mu\text{A}$  of supply current the slew rate is a corresponding low  $.063\text{ V}/\mu\text{sec}$ .

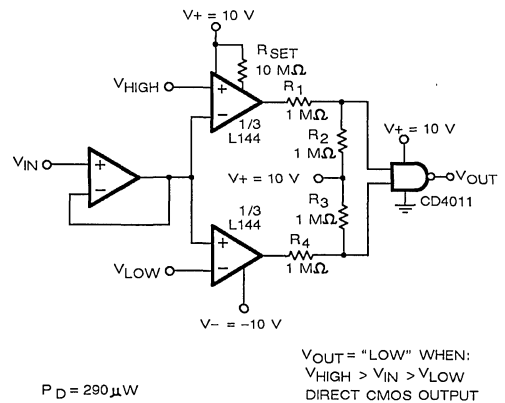


Figure 14. Double-Ended Limit Detector

## CONCLUSION

The preceding practical circuit examples are intended to show a few of the many possible applications of the L144 micropower triple op amp.

## REFERENCES

1. M.K. Vander Kooi, "Slew Rate Limiting of IC Op Amp is Easy to Predict and to Avoid," EDN, October, 1972; pp. 36-37.
2. J.G. Graeme, G.E. Tobey, and L.P. Huelsman; "Operational Amplifiers Design and Application", McGraw-Hill Co., New York, N.Y., 1971, pp. 293-295.
3. S.K. Mitra, "Active Inductorless Filters", IEEE Inc., New York, N.Y., 1971, pp. 74-78.

# IC MULTIPLEXER INCREASES ANALOG SWITCHING SPEEDS

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Revised March 1988

## INTRODUCTION

A two-level IC multiplexing system, that has significant advantages over conventional single-level systems, can improve effective switching speeds of analog systems by approximately one order of magnitude.

Analog multiplexing is the simultaneous transmission of two or more analog signals on to a single transmission line. Time-division multiplexing is widely used, each analog input being sampled sequentially and conveyed into a common output line. The signals can be transmitted directly in their analog form or they can be digitally coded by means of A/D converters and then transmitted. The latter method is used in applications requiring a very high degree of transmission accuracy.

In a system having 'n' analog inputs, a multiplexing/demultiplexing system will generally require 1/n of the total transmitting and receiving circuitry of a non-multiplexed system. Hence, system cost is reduced drastically in the former case.

Present-day requirements for analog multiplexers have necessitated the development of special circuits. These incorporate multichannel FET multiplexers which are now available in integrated-circuit form, and which possess numerous advantages over their discrete counterparts:

- (1) The use of IC's introduces a higher degree of circuit reliability;
- (2) Switch for switch, IC's are much more compact;
- (3) System layout cost is less;
- (4) Lower cost per switch.

## Single-level Multiplexing System

Fast IC multiplexers, having rapid open and close switch times, are required in many applications in

which rapid sampling of analog signals is required. In any application in which it is necessary to sample analog signals and convey them at maximum transmission rates, the ratio of  $t_1 : t_2$  must be as small as possible (where  $t_1$  represents the time between samples and  $t_2$  the sample duration time).

Applications requiring microsecond sample times clearly present considerable difficulty, because IC multiplexers which are commercially available have  $t_{ON}$  and  $t_{OFF}$  times in the region of 1–2  $\mu s$ . When used in the conventional single-level mode, a substantial loss in transmission efficiency results. Figure 1 shows a simple single-level system for analog multiplexing.

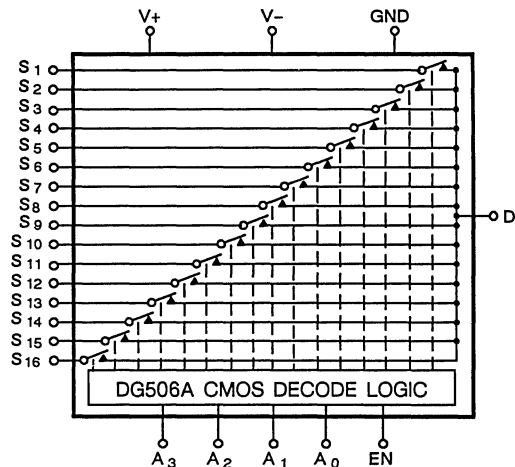


Figure 1. DG506A Used as a Single-Level Multiplex System

With a single-level system one can obtain either (a) the wave-forms shown in Figure 2(a), and be faced with inter-channel interference due to overlapping samples or, (b) the waveforms of Figure 2(b) which result in delayed channel switching, in order to eliminate interference between channels.

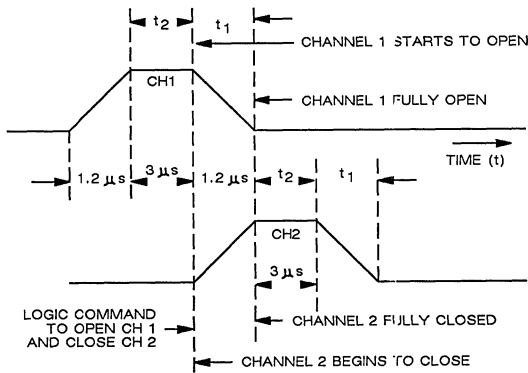


Figure 2(a). Overlapping Channels

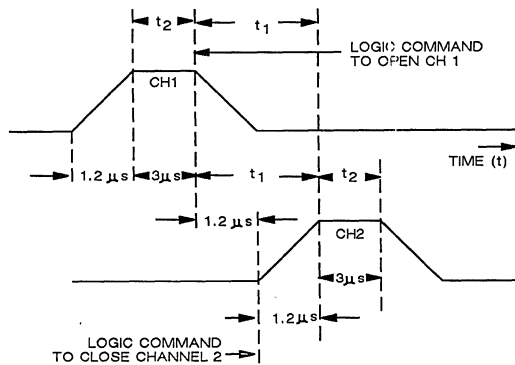


Figure 2(b). Delayed Channel Switching

If the analog sample time needed is  $3 \mu\text{s}$ , for example, system 2(a) would not be a practical proposition. System 2(b) would certainly be practical but would introduce a large wastage of transmission time due to the large ratio of  $t_1:t_2$  (Figure 2(b), in fact, indicates a 50% loss in transmission efficiency).

This problem is manifest in all commercially available IC multiplexers used in single-level systems. Other problems that result from using a single-level system are:

- (1) With a large number of separate analog inputs, the leakage currents through the OFF switches can introduce an appreciable percentage voltage error into the common output line. This is important if the analog signal being conveyed through the closed switch is in the millivolt range.

- (2) The common node output capacitance increases with the total number of analog channels being multiplexed. With 64 channels (i.e.,  $4 \times 16$  channel DG506A), the common node output capacitance will be typically 180 pF.

The charging time ( $t_1$ ) necessary for the analog signal to reach 0.25% of its final value (six time constants) will then be approximately

$$6 \times C_{\text{OUT}}(r_{\text{DS(ON)}} + R_{\text{ANALOG SOURCE}}) \quad (1)$$

If the source resistance is  $1 \text{ k}\Omega$ ,  $t_1$  will be

$$6 \times (180 \times 10^{-12} \text{ F}) \times (400 \Omega + 1 \text{ k}\Omega) = 1.51 \mu\text{s} \quad (2)$$

This decreases the effective switching speed of the multiplexer.

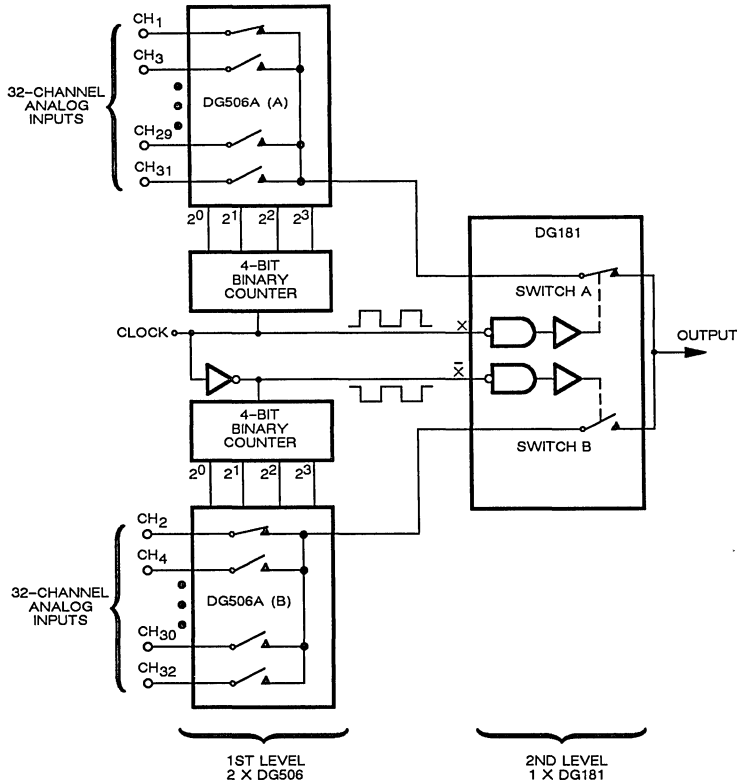
## Two-Level Multiplexing System

These problems can be overcome if a two-level multiplexer is used, which inherently provides a much faster switching system. Figure 3 shows an example of a two-level system capable of 32 channels. The first level consists of 16-channel DG506A multiplexers, the use of which offers the advantages stated in the introduction. The second level consists of two or more single channels of a DG181; this has switch open and close times of, typically, 100 ns, and has a break-before-make switching action. The DG181 is available in a dual-in-line package.

The two-level system uses the bank of high speed DG181 switches at the output to sequentially switch between the outputs of the DG506A's. Each DG506A is able to switch channels during the time the others are being interrogated. It contributes capacitance and leakage at the output only when it is switched into the output bus by a DG181.

The use of the two-level system achieves the following:

- (1) Effectively reduces the common output node capacitance of the system. It will consist of a single multiplexer output, DG506A (45 pF) and several DG181's (6 pF OFF, 14 pF ON). For a 64-channel 2-level system, for example, the output capacitance is reduced to 77 pF, compared to 180 pF of the single-level system.



**Figure 3.** 32-Channel, Two-Level Multiplex System, Comprising Two DG506s in the First Level, and a DG181 in the Second

- (2) Reduces the amount of error voltage developed as a result of leakage current flow through the OFF switches into the common output node. The leakage through the OFF switch of Figure 3 into the common output node is effectively that of a single OFF channel of the DG181 (from  $\pm 40$  nA to  $\pm 10$  nA in a 64-channel system).
- (3) Allows the system to operate in such a way that the ratio  $t_1:t_2$  is very small. In the example,  $t_1 = 200$  ns and  $t_2 = 3$   $\mu$ s.

The switching speed of the system is dependent on the DG181, which is a high-speed 2-channel SPST ( $t_{ON} \sim 100$  ns). The slower switching time of the DG506A ( $\sim 1$   $\mu$ s) is not important because this switching transition can take place while the other DG506A's are being interrogated.

With the two-level system design, more data can be transmitted with a very fast multiplex system utilizing a large number of low-cost, moderate-speed multi-channel multiplexers and several high-speed SPST switches.

**Details of the System**

A 32-channel two-level multiplexing system is shown in Figure 3. Figure 4 shows the analog switching waveforms, including the segments of the multiplexer outputs being sampled. Notice that as one multiplexer is being sampled, the other is switching. The example of the output samples shows the edge-to-edge sampling achieved by the two-level system. The logic timing diagram for the system of Figure 3 is shown in Figure 5. This illustrates the timing used by the DG181 switches to give the two-level multiplexing.

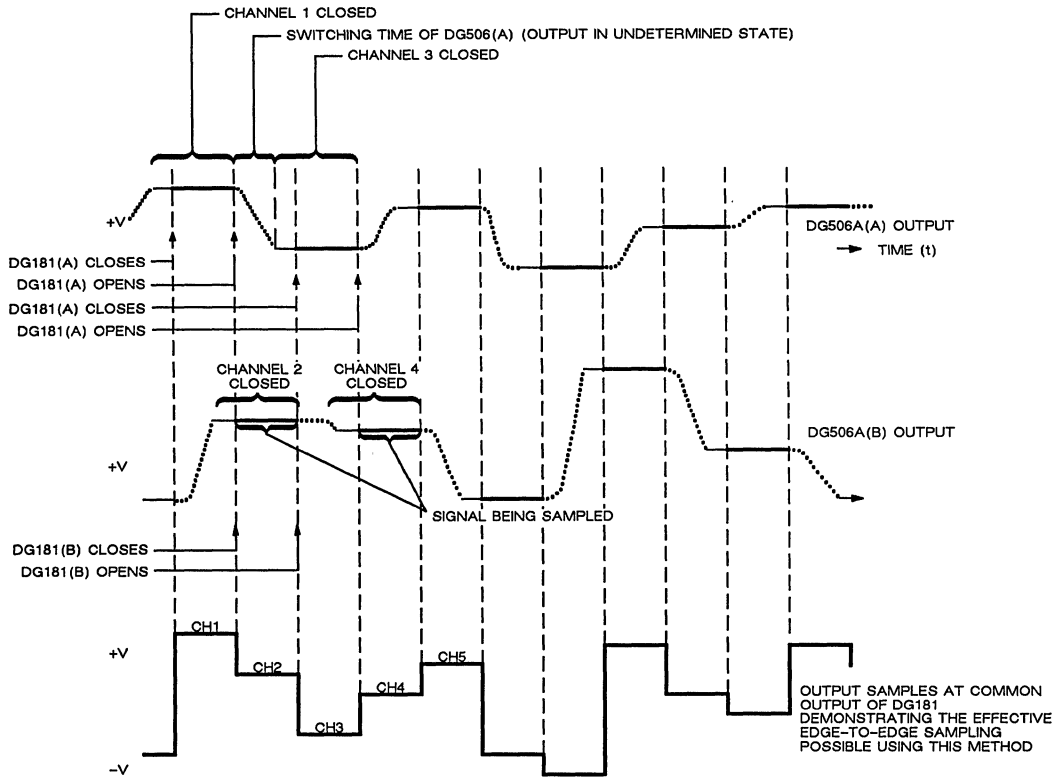


Figure 4. Two-Phase Timing Method That Eliminates the Switching Delays of the 16-Channel Multiplexers in a 32-Channel System

## Logic Control System

The digital control logic consists of a multi phase clock generator and recirculating binary counters. The number,  $N$ , of clock phases and binary counters necessary is equal to the number of multiplexers used in the first level of the system. With 16-channel DG506A's, 4-bit binary counters are needed (such as TTL DM7493) to give addressing to all 16-channels.

## 64-Channel Two-Level Multiplexer

Figure 6 shows a complete 64-channel two-level multiplex system. For the 64-channel system,  $N = 4$  and the four clock phases are generated with a two-bit

counter and decoding logic (these four phases are also shown in Figure 6). Two J-K flip-flops (TTL DM7473) are connected as a two-bit counter and toggle on the high-to-low clock edge. The NAND gates (DM7400) decode the flip-flop outputs into the four clock phases shown. The low state of the clock phase is the ON state of the corresponding DG181 switch. As a clock phase goes from a low-to-high state, the DG181 it feeds turns off and the corresponding 4-bit binary counter (DM7493) is triggered to its next address state. This causes the multiplexer to change as the output of the next multiplexer is being sampled at the output. For synchronization there is a reset available to set the system to start on the first channel when power is first applied.



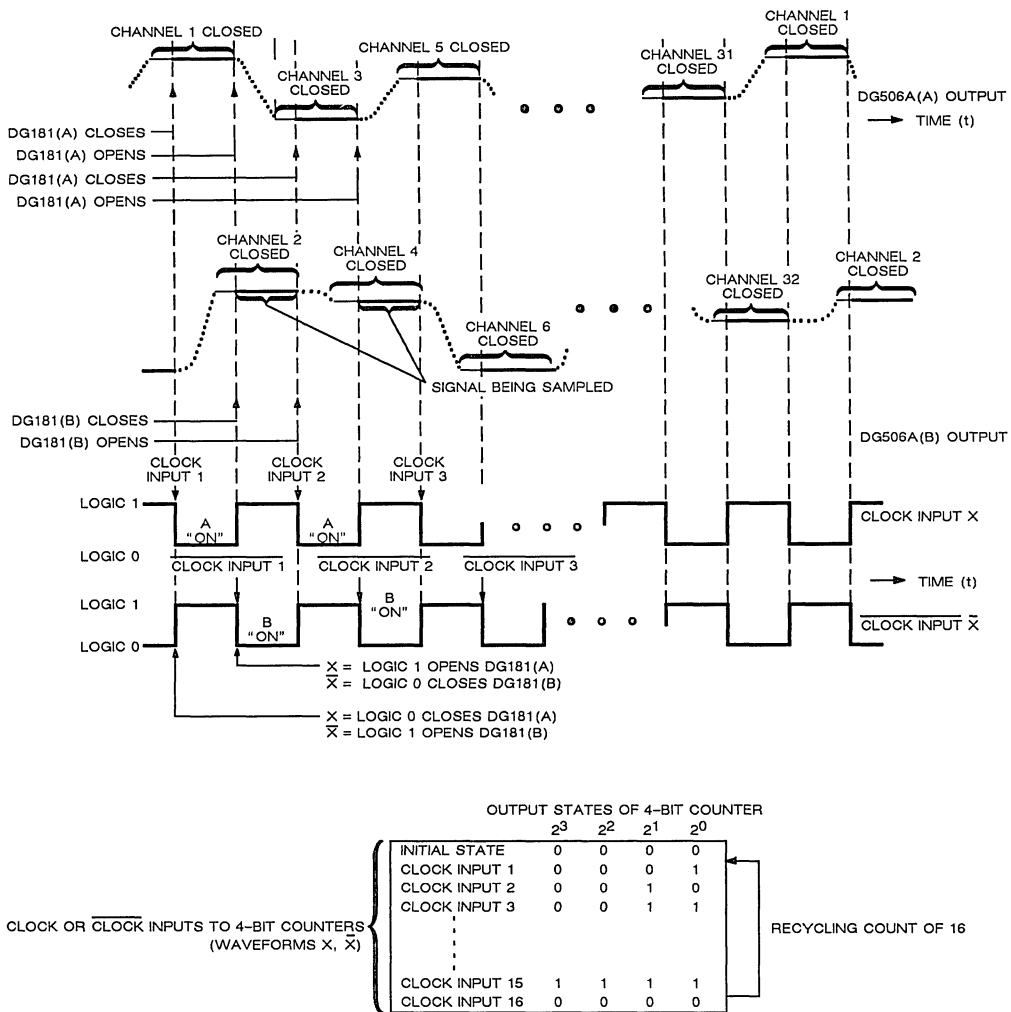


Figure 5. Logic Timing Diagram Showing Waveform Timing Sequences for a 32-Channel System

**CONCLUSION**

This system may be used for increasing data transmission rates in analog switching systems. One particular application is found in telephone switching

where, for instance, it is necessary to multiplex 32 or more channels of analog information in the form of 4 μs samples (edge-to-edge) on to a common output line.

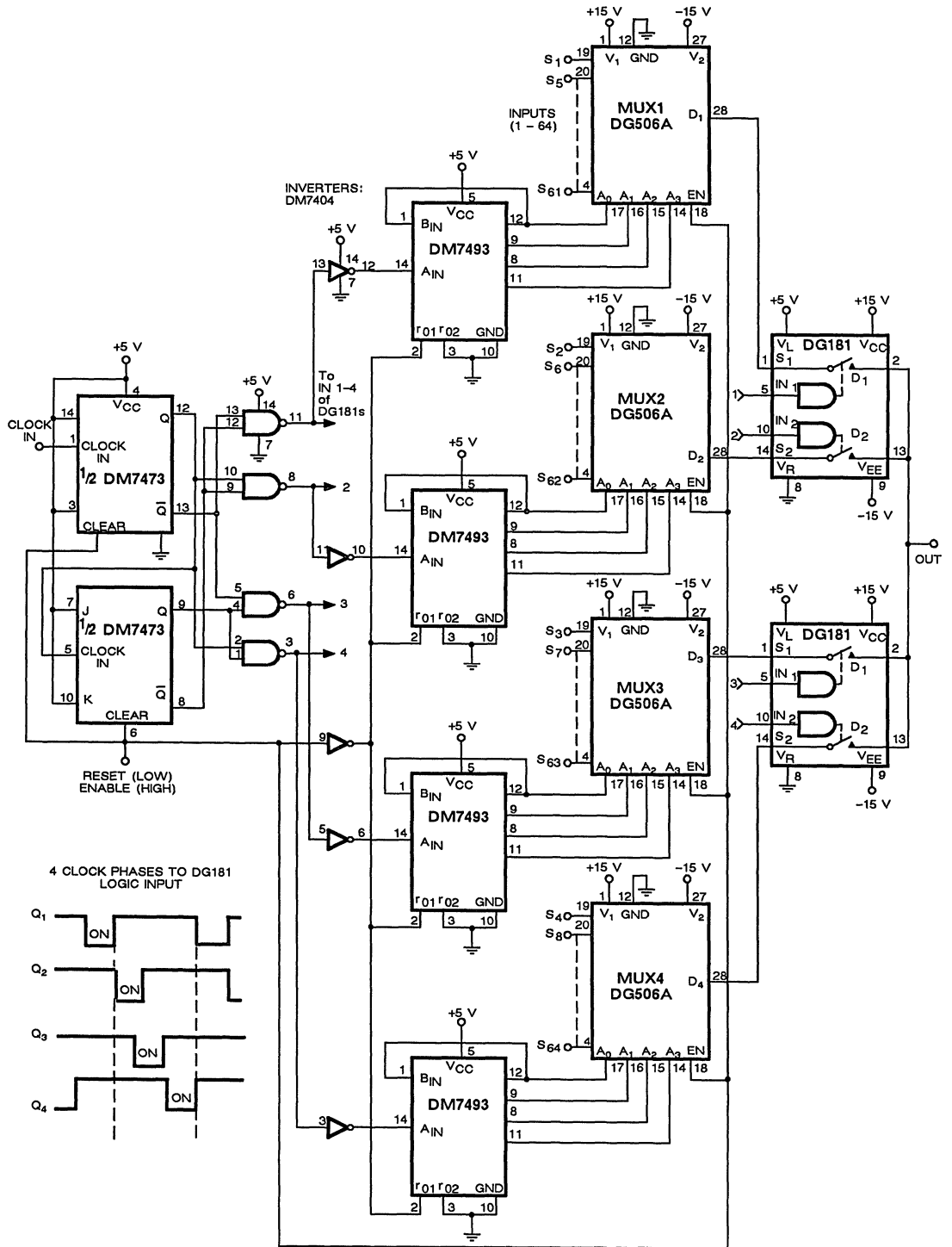


Figure 6. 64-Channel 2-Level Multiplex System

## ELIMINATE THE GUESSWORK IN YOUR ANALOG SWITCHING ERROR ANALYSIS

By Steve Moore and Van Brollini  
September 1987

### The "DGP" Philosophy

To design a precision analog system, errors must be identified and reduced to levels within the guard bands dictated by the overall system accuracy requirements. For worst-case design with analog switches and multiplexers, one must rely on data sheet minimum and maximum limits to determine the error contribution of a given channel. Many devices, however, do not have 100% tested limits for parameters critical for precision such as charge injection, variations in on-resistance, and variations in switching time. Furthermore, other parameter limits are specified on a "not tested, guaranteed-by-design" basis. Therefore, precision system designers must screen incoming devices, living with uncertainty about the actual performance of their system, or compensate by adding circuitry or selecting other expensive components.

The "DGP" family of analog switches and multiplexers brings new levels of precision to monolithic devices. This family embodies a new philosophy for the specification and testing of analog ICs. In contrast to "typical" or "guaranteed by design" specifications, all limits on the DGP family data sheet are 100% tested. Superior CMOS processing tightens the limits for leakage and extends the analog range beyond anything previously available. Devices are tested with 10% guard bands on the power supplies at the most commonly used voltages. Using new analog test capabilities, charge injection, variations in on-resistance, and switching times are also 100% tested.

### Eliminating Data Sheet Guesswork

When designing a precision data acquisition system with existing analog switch and multiplexer families, the errors introduced by these switches can be the major source of system inaccuracy. The limits for switch on-resistance and leakage currents have always had well-defined data sheet limits—even over temperature. However, it has been impossible to find

tested limits for the variations in on-resistance as the power supply, drain, or source voltages are varied. So while it is easy to predict the offsets caused by "ON"-resistance under nominal conditions, the designer must guess what effect varying supply and input levels will have. With the new DGP family of switches and multiplexers, these variations are specified to within 5% over a wide range of supply and analog voltage ranges. Therefore, it is now possible to design a fully guard-banded system.

What happens to an analog switch when the power supply voltage is varied from +13.5 V to +16.5 V (a typical  $\pm 10\%$  tolerance in a nominally +15 V supply)? With the previous generation of switches, the designer either characterized the device or used the manufacturer's typical performance curves to estimate the guard bands required to ensure system accuracy under all rated conditions. Switch "ON"-resistance could vary as much as 20% between channels and with changes in supply voltage and analog input voltage. These variations translate directly into non-linearity and gain errors. The DGP devices are tested at worst-case supply voltages to define firm design limits for operation with  $\pm 10\%$  variations in nominally  $\pm 12$  V,  $\pm 15$  V, and  $\pm 20$  V systems.

The change in "ON"-resistance from switch to switch in multiple switches and multiplexers can limit a system's channel-matching and common-mode rejection. This change has never been specified below 10%, and it is usually listed as a "typical" value, not a tested one. Variations from switch to switch are included in the DGP family tests for on-resistance variation. For example, a total of 24 supply voltage combinations and analog voltages are tested across the four channels of the DGP201A to determine changes in on-resistance specified with less than 5% total variation.

Leakage current at the source or drain can result in significant errors in sample-and-hold amplifiers and high-impedance systems. While other switch families offer leakages as low as 1 nA, the DGP family offers

a factor of four times improvement in leakage performance (down to 250 pA). Additionally, tight limits are established for the most adverse leakage conditions--that is, the worst-case extremes of the temperature and voltage ranges.

Most analog switch/multiplexer families for precision applications operate with  $\pm 15$  V supplies. CMOS technology, which allows an analog signal swing from rail to rail, provides operation with up to  $\pm 15$  V. The enhanced metal-gate CMOS technology used for the DGP family (see "Process Evolution" below) allows operation with supplies up to  $\pm 22$  V supplies, with "ON"-resistance and leakage specifications tested for those supply levels. Therefore, a wider signal range is achieved, resulting in greater system headroom and better dynamic range. These features are essential for high-resolution applications such as precision data acquisition and professional audio equipment.

## Improved AC Performance

In today's world of high-speed data acquisition, the requirements of precision systems extend into the realm of the dynamic accuracy as well as the traditionally specified dc parameters. Switch and multiplexer specifications of particular importance are charge injection (or charge transfer) and switching speed (or transition time). Charge injection occurs when the parasitic FET switch capacitance transfers a charge into a channel that is being switched on or off. Seen as a glitch which accompanies all on/off transitions, charge injection is a major source of inaccuracy in sample-and-hold amplifiers as the charge is dumped into the hold capacitor (see Figure 1). Because testing this parameter in production is difficult, the tested maximum limits for charge injection have never been specified on analog switch and multiplexer data sheets. However, the DGP201A is fully tested for charge injection with a maximum limit of 50 pC (at  $V_s = 0V$ ). The maximum error contribution of charge injection to a sample-and-hold circuit can be calculated using:

$$\Delta V = \frac{\Delta Q}{C}$$

Using this formula, the maximum voltage error for a 10,000-pF hold capacitor is 5 mV.

Switching speed can vary from channel to channel. These variations can create sampling errors, resulting in system dynamic channel mismatch. The DGP

family uses advanced ac test capability to specify a maximum variation in switching time of 50 ns.

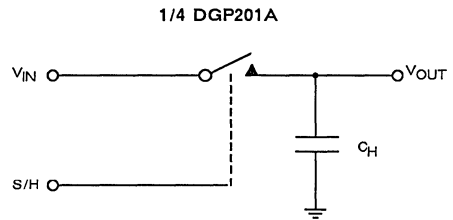


Figure 1. Simple Sample-and-Hold Circuit

## Full Range of Standard Functions

With the DGP family, Siliconix is offering the most commonly used analog switch and multiplexer configurations. These parts are all pin-for-pin replacements for existing devices, making it easy to upgrade system precision and quality. For example, the DGP201A may be used for quad switch applications, the DGP303A for dual SPDTs, the DGP508A for 8-channel multiplexers, and the DGP509A for dual 4-channel systems.

## Process Evolution

The DGP family is built using a mature metal-gate CMOS technology. Since its introduction in the early 1970s, this process has been significantly enhanced, improving to the point where today the breakdown voltage is consistently above 50 V without trade-offs for leakage or on-resistance performance. This extremely well-controlled process specification results in leakages typically below 50 pA, allowing vastly improved maximum leakage limits.

## Improved Sample-and-Hold Performance

A precision sample-and-hold amplifier can be built with the DGP201A quad analog switch. Figure 2 shows a practical sample-and-hold amplifier that uses buffering at the input and output. This circuit includes charge cancellation circuitry to minimize pedestal error due to switch charge injection.

During the sampling phase (logic input low), SW2 and SW4 are on, while SW1 and SW3 are off. This design forms a closed-loop amplifier that charges the hold capacitor, C2, through the on-state switch, SW4. C2 is charged to the value of the input voltage

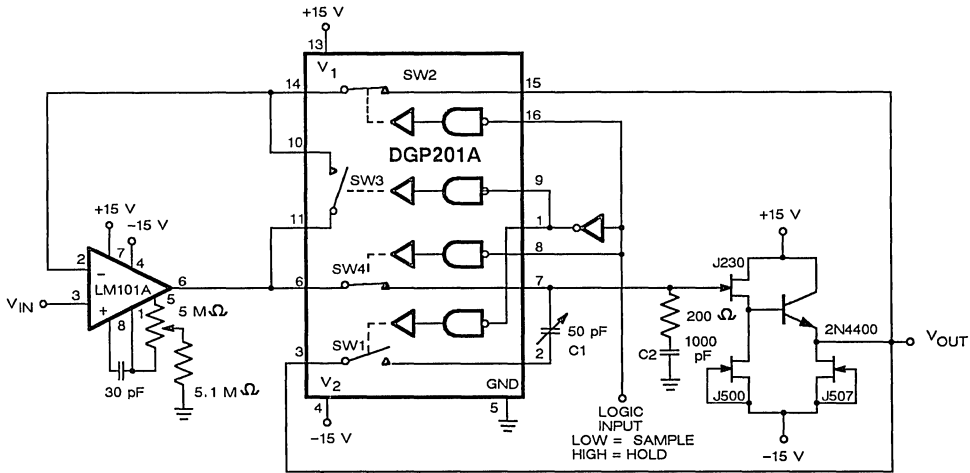


Figure 2. High Performance Sample-and-Hold Circuit with Reduced Pedestal Error and Droop Rate

being sampled. During the hold phase (logic input high), SW2 and SW4 are open, while SW1 and SW3 are closed. This configuration opens the overall loop, so the output of the sample-and-hold circuit remains fixed at the voltage stored on the hold capacitor. Closing SW3 keeps the input buffer at unity gain in the absence of overall negative feedback. Closing SW1 transfers a charge, which is equal and opposite in magnitude to the amount injected by SW4. This charge would otherwise feed into the hold capacitor and appear at the output as a pedestal (or range dependent offset) error in the sample. Using the DGP201A, with its maximum charge injection of 50 pC, the value of the charge compensation can be intelligently selected to achieve the desired level of precision.

The extremely low leakage of the DGP201A and the JFET input buffer gives this sample-and-hold function an excellent droop rate. Worst-case droop rate is calculated by

$$\Delta V/\Delta t = \Delta I/C$$

where I is the sum of leakage from the switch (250 pA maximum) and the JFET (250 pA maximum), and C is the value of the hold capacitor.

In this circuit, the maximum droop rate is 500 pA/1000 pF = 0.5 V/sec.

## Differential Data Acquisition System

Figure 3 shows a 4-channel 4 1/2-digit differential data acquisition system. The Si7135 A/D converter uses a 2.0 V full-scale range, resolving 20,000 counts which translates into a 100 μV step size. Typical leakage currents of most multiplexers can seriously degrade system accuracy, especially with high-impedance sources such as strain gauges and transducer bridges. The DGP509A, with its 2 nA maximum leakage, contributes a maximum 100 μV error (1 LSB) with a 50 kΩ source impedance. Using the DGP509A, 4-channel precision differential multiplexing is accomplished without degrading common-mode rejection or without additional decode logic.

## Precision Gain Switching Differential Amplifier

Figure 4 shows an instrumentation amplifier which uses an OP-07 precision op amp and a DGP303A to digitally select one of two gain settings. This circuit features low noise, excellent common-mode rejection, low drift, and well-defined limits for gain accuracy. Analyzing this circuit using the original DG303A and comparing it to the performance using the new DGP303A illustrates the dramatic improvement possible by upgrading to the DGP family without redesigning the circuit.

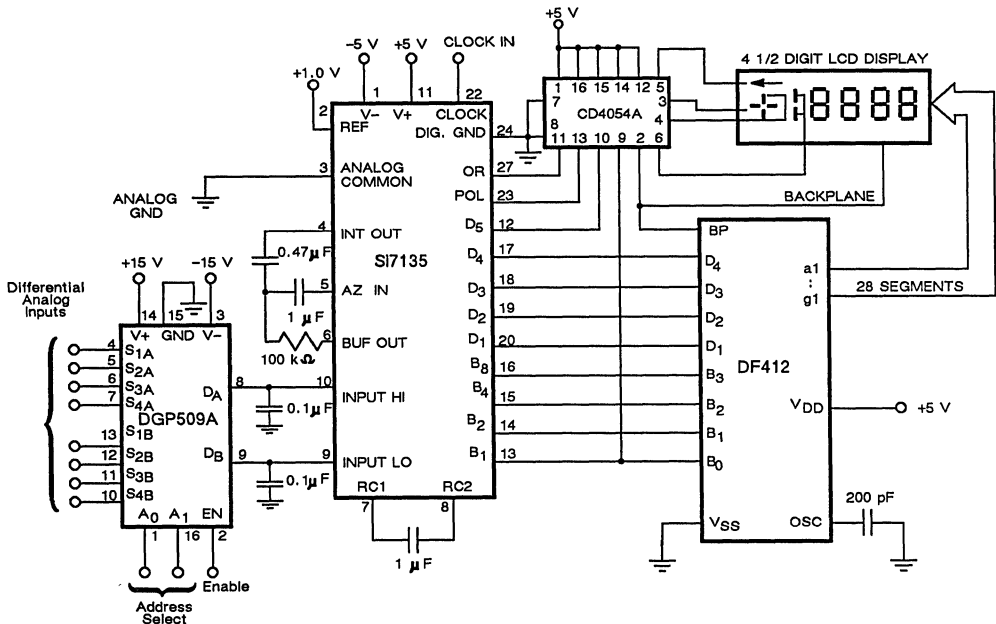


Figure 3. 4 1/2 Digit Differential Data Acquisition System

The most dramatic improvement is seen at the industrial temperature range maximum (85°C). The DGP303A switches are modeled using a resistor ( $r_{DS(ON)}$ ) in parallel with a current source ( $I_{D(ON)}$ ) for an on-state switch. For the off-state condition, the switches are modeled only as a current source ( $I_{S(OFF)}$ ).

In this example, the gain selection is unity for logic high at the logic input, and a gain of 10 is selected for a logic low. The sources for error (at maximum over temperature of -40 to +85°C) under consideration are:

$$I_B \text{ (OP-07A)} = 4 \text{ nA}$$

$$I_{D(ON)}(\text{DG303AB}) = 200 \text{ nA};$$

$$I_{D(ON)}(\text{DGP303A}) = 2 \text{ nA}$$

$$I_{S(OFF)} \text{ or } I_{D(OFF)} (\text{DG303A}) = 100 \text{ nA};$$

$$I_{S(OFF)} \text{ or } I_{D(OFF)} (\text{DGP303A}) = 1 \text{ nA}$$

$$r_{DS(ON)} = 75 \Omega$$

$$R1 = R3 = 10 \text{ k}; R2 = 100 \text{ k}$$

The input error voltage ( $V_{erti}$ ) caused by switch leakages can be approximated by:

$$V_{erti} = 10 \text{ k} (I_{D(ON)} + I_{S(OFF)} + I_B)$$

For the DG303A,

Using the DGP303A precision analog switch, the error is:

$$V_{erti} = 10 \text{ k} \times (1 \text{ nA} + 2 \text{ nA} + 4 \text{ nA}) = 70 \mu\text{V}$$

These calculations show that with the DGP switch, the error is dominated by the OP-07 bias current.

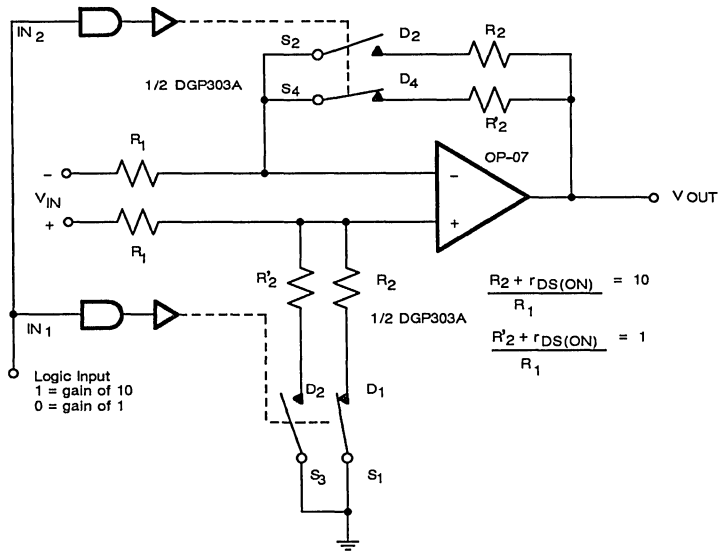


Figure 4. Precision Gain-Selectable Differential Amplifier

## MULTIPLEXER ADDS EFFICIENCY TO 32-CHANNEL TELEPHONE SYSTEM

by John A. Roberts and J.O.M. Jenkins  
Revised January 1988

Time-division multiplexing has gained wide acceptance in recent years as a means of combining multiple telephone channels on two-wire-pair transmission lines that previously accommodated only one channel. Combined with pulse-code-modulation (PCM) circuitry to convert the sampled signals to a digital format, the multiplexing techniques have generally reduced size, power consumption, and costs of plant equipment.

To achieve minimum signal loss and distortion in such systems, much effort has been directed toward building multiplexers that switch from channel to channel with minimum output rise and fall times. Such a multiplexer design, recently built and tested, provides 150 ns switching time, an order of magnitude faster than presently available circuits.

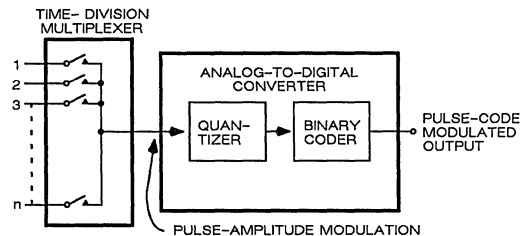
This high speed switching is achieved by applying biphasic control logic to a two-level multiplexer arrangement that takes advantage of the fast rise times and the break-before-make action of newly developed integrated circuit multiplexers.

### Telephone System Requirements

A generalized system used to time-division multiplex voice signals is shown in Figure 1. After the signals on each of analog channels have been sampled, each sample is quantized and coded into a PCM format. The new design focuses on the analog multiplexer, which feeds the analog-to-digital converter.

The sampling rate for each of the incoming channels is determined by the desired bandwidth of the voice signals being sampled, while sampling dwell time is fixed by the number of channels that must be sampled. Nyquist's sampling theory<sup>1,2</sup> states that any transmitted waveform that is band-limited to a maxi-

imum frequency of  $f_L$  can be accurately reconstructed from periodic samples taken at a rate as slow as  $2f_L$ .



Problems in overcrowding of wire-pair telephone-transmission lines are lessened by using analog time-division multiplexers followed by A/D converters.

Figure 1. Telephone's Answer

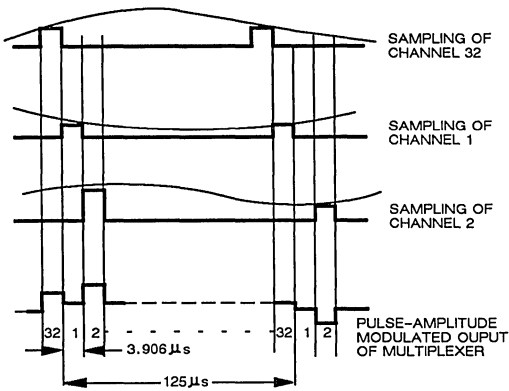
In practice, however, filters do not provide ideal cutoff at  $f_L$ , and a somewhat higher sampling rate must be tolerated. For example, to achieve less than 1% error in reconstruction accuracy, the sampling rate must be at least twice the frequency at which the unwanted signals above cutoff are reduced by 40 dB.<sup>2,3</sup> Thus, to relax difficult filtering requirements at the input-to-sampling circuitry, a voice bandwidth that is nominally limited to about 2.3 kHz is usually sampled at an 8 kHz rate, or once every 125  $\mu$ s.

### Single-Level Multiplexers

The standard configurations of today's telephone systems dictate that a fundamental group of 32-channels be multiplexed onto one line.

Therefore, with a sample frame time of 125  $\mu$ s each of 32 multiplexed channels is sampled for 125/32 or 3.906  $\mu$ s, as Figure 2 indicates.





For accurate reconstruction of a 3.3 kHz telephone signal, it must be sampled at a rate of about 8 kHz, or once every 125 μs. The hierarchy of today's telephone system makes it highly desirable to multiplex 32 speech channels during this period.

Figure 2. Tight Fit

Conventional multiplexing networks can be implemented with either discrete components or integrated circuits, such as the Siliconix DG508A (see table). This circuit multiplexes eight input channels with a switching time between channels of 1 to 1.5 μs. A 32-channel multiplexer is constructed simply by paralleling four DG508A's. Thus, in single-level switching, each of the 32 analog input channels is multiplexed through a single switching bank.

**CIRCUIT CHARACTERISTICS TABLE**

<b>DG508A: 8-CHANNEL ANALOG MULTIPLEXER</b>	
CONTROL INPUTS	
	SINGLE OUTPUT
<b>DG181: 2-CHANNEL ANALOG MULTIPLEXER</b>	
CONTROL INPUTS	
	OUTPUTS
<b>DG508A</b>	<b>DG181</b>
450 Ω	30 Ω
1.5 μs	150 μs
25 pf	20 pf
SERIES RESISTANCE (ON CHANNEL) SWITCHING TIME OUTPUT CAPACITANCE	

The problem with such a system stems from the relatively slow 1–1.5 μs switching times between channels. Depending on the design of the particular multi-

plexer, there can either be an overlap or "aliasing" between sampling pulses, which leads to crosstalk between channels, or a large separation between samples, which reduces the sampling time of a particular channel. The reduced sampling time results in lower multiplexer efficiency.

Added to the 1–1.5 μs switching time is a delay associated with the increased output-node capacitance when multiple channels are combined. For four DG508A's (32 channels), the added delay is about 200 ns. These delays further reduce the effective sampling time and bring some uncertainty into the timing strobe for the A/D converter. The node-capacitance problem can be lessened to some extent by a high performance sample-and-hold circuit between the multiplexer and the A/D converter. However, the 1–1.5 μs switching times remain, and this problem becomes acute for signals obtained from sources with output impedances of 2 kΩ and above.

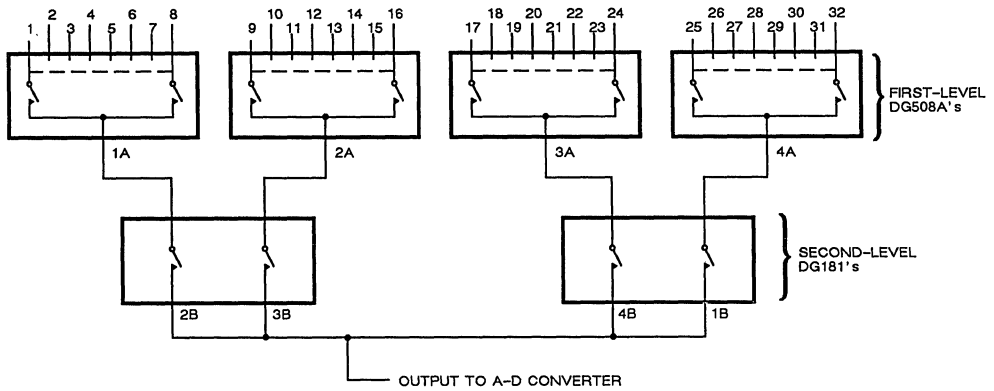
### Two-Level Multiplexing

System response time can be improved by reducing the output-node capacitance. This is achieved by using a two-level multiplexing system as shown in Figure 3.<sup>4</sup> Here, circuits with lower output capacitance (such as the DG181, with performance shown in the table) are placed in the second multiplexing level, which feeds the A/D converter.

The DG181 can switch at a speed of 150 ns. The full advantages of these speeds, however, are not realized, since interchannel sampling time is still limited by the 1–1.5 μs rise times of the DG508A's.

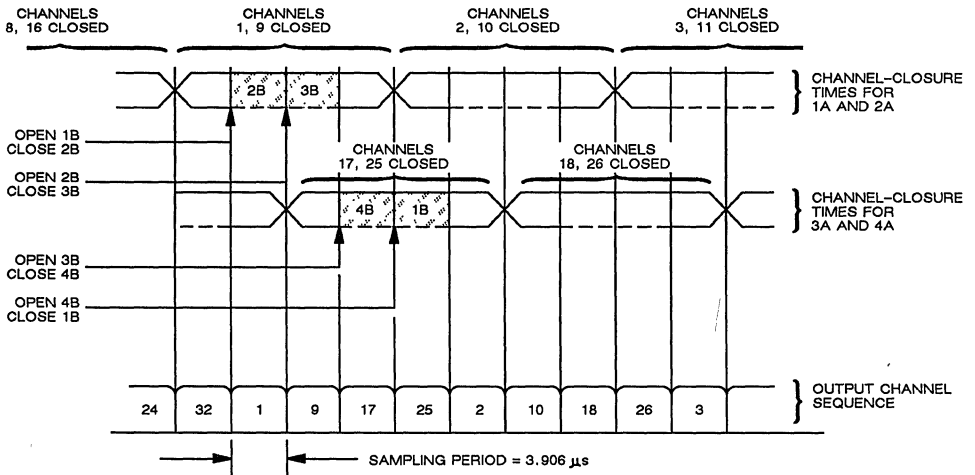
A timing sequence that makes maximum use of switching rise times of the DG181s (and therefore results in extremely high sampling efficiency) can be achieved by applying control logic to the two-level multiplexer in a manner which will give the sampling sequence shown in Figure 4. The faster switching speed and the break-before-make action of the DG181 virtually removes the possibility of overlap.

The problems caused by the relatively slow switching time of the DG508A are eliminated by ensuring that the first channels of multiplexer switches 1A and 2A (Figure 3) are already fully closed when 2B and 3B, respectively, are closed. This sequence is then repeated for each of the eight channels of the DG508A's, and the complete cycle is again repeated.



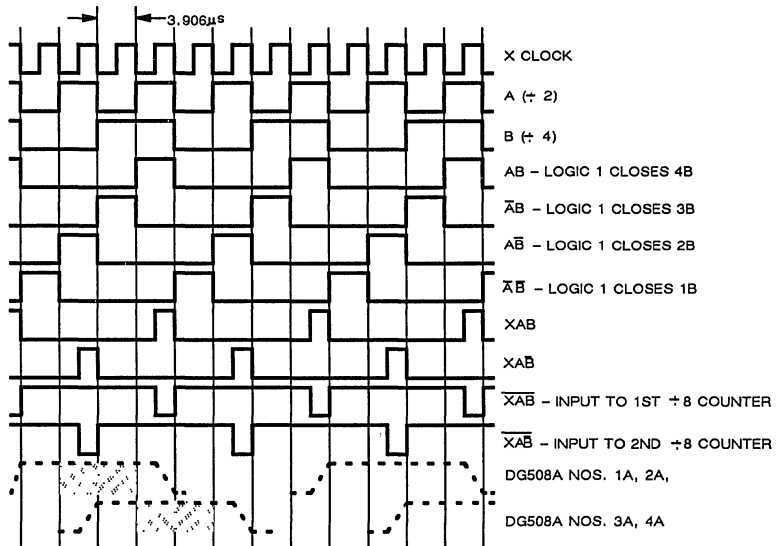
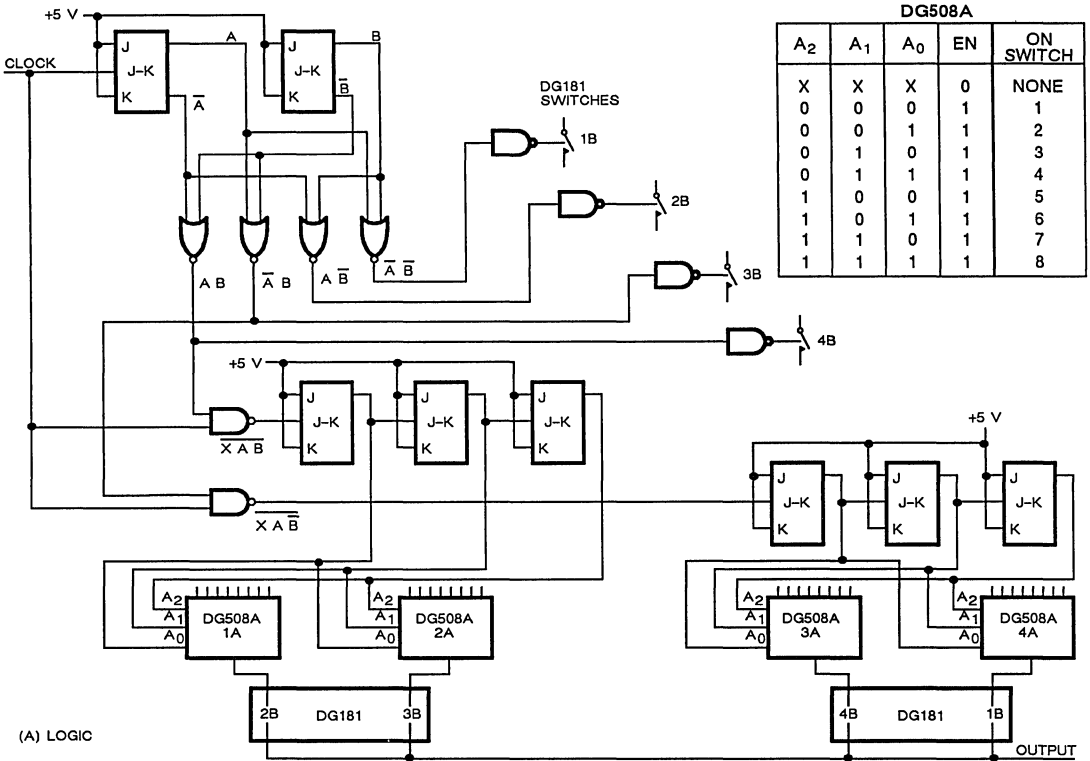
Output-node capacitance is significantly reduced when a second level of multiplexers is added. Interchannel switching time; however, is still determined primarily by the speed of the first-level switches.

Figure 3. Two-level Multiplexing



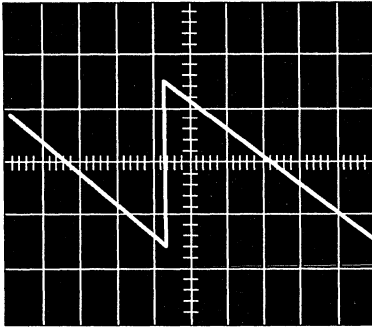
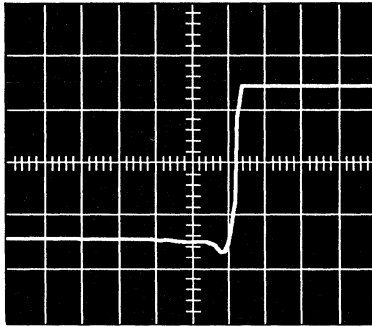
By adding two-phase control logic to the two-level multiplexer of Figure 3, the full advantage of the 150 ns switching speed of the DG181 circuits is realized. Channel numbers correspond with those in Figure 3.

Figure 4. Phase II timing



TTL control circuits (a) implement timing (b) required in two-phase, two-level multiplexing system. First-level DG508A switches are MOS circuits, and JFET technology gives the faster switching times needed in the DG181 second-level switches.

Figure 5. Logic hardware

(a) 20  $\mu$ s/DIV

(b) 200 ns/DIV

Thirty-two dc levels are sampled in a prototype multiplexer to demonstrate switching speed of the two-level two-phase design. Largest single transition, from  $-3$  to  $+3$  V is expanded in the lower trace. Vertical scale for both traces: 2 V per division.

Figure 6. Quick Switch

## Two-Phase Control Logic

The timing requirement and logic control layout for the complete circuit are shown in Figures 5a and 5b. Waveforms A and B are obtained from the input clock waveform by an asynchronous divider. The A and B

waveforms are combined to give  $AB$ ,  $A\bar{B}$ ,  $\bar{A}B$  and  $\bar{A}\bar{B}$  which are needed to close the DG181 gates sequentially. Functions  $XAB$  and  $XAB\bar{B}$  then clock two 3-bit asynchronous counters. A delay of two clock periods exists between  $XAB$  and  $XAB\bar{B}$  so that the count sequence applied to the second and third multiplexer is suitably delayed.

A prototype multiplexer with two-phase control logic has been constructed and successfully tested. Series 7400 TTL circuitry is used to implement the timing and control logic. First-level DG508A switches are MOS circuits, while JFET technology gives the faster switching times needed in the DG181 second-level switches.

To simulate all 32 analog inputs to the multiplexer, a voltage-divider network of series resistors is connected across a  $+3$  V supply. Thus, 32 dc voltage levels are consecutively tapped off the network and applied to the multiplexer input. The multiplexer output is displayed on the oscilloscope, as shown in Figure 6a. As can be seen, the largest transition is from  $-3$  to  $+3$  V. In Figure 6b, this 6 V transition is demonstrated as being accomplished in less than 100 ns.

If low-power TTL or diode-transistor logic is used in the control circuits, synchronous counters may be necessary to eliminate cumulative flip-flop delays. Although the system shown is designed for negative-edge-triggered J-K flip-flops, the circuitry can be rearranged quite simply for almost any bistable logic element.

## References

1. Schwartz, M., "Information Transmission Modulation and Noise," 2nd ed. p. 174, McGraw-Hill Book Co. 1970.
2. Shannon, C., "A Mathematical Theory of Communications," Bell System Technical Journal. pp 379-423, July 1948 and pp 623656, October 1948.
3. English, M., "Multiple systems" Electronic Products pp 28-31, May 1969.
4. Yoder, D., "Two-Level Multiplexing for Data-Acquisition Systems," pp 67-72, EEE July 1970.





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## APPLICATION NOTES & TECHNICAL ARTICLES

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- F = 1986 FET Data Book
- M = 1988 MOSPOWER Data Book
- MAH = 1985 MOSPOWER Applications Handbook

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Altamonte Springs (32701)  
Future Electronics  
380 S. Northlake Blvd.,  
Suite 1048  
(407) 767-8414  
FAX: 407-834-9318

Altamonte Springs (32701)  
Marshall  
380 S. Northlake Blvd., Ste. 1024  
(407) 767-8585  
FAX: 407-841-1916

Altamonte Springs (32701)  
Pioneer Electronics  
221 North Lake Blvd.  
(407) 834-9090  
TWX: 810-850-0177  
FAX: 407-834-0885

Clearwater (34620)  
Future Electronics  
4900 N. Creekside Drive  
(813) 578-2770  
FAX: 813-576-7600

Deerfield Beach (33441)  
Pioneer Electronics  
674 S. Military Trail  
(305) 428-8877  
TWX: 510-955-9653  
FAX: 305-481-2950

Ft. Lauderdale (33309)  
Hamilton/Avnet, #17  
6801 N.W. 15th Way  
(305) 971-2900  
TWX: 510-956-3097  
FAX: 305-971-5420

Ovelda (00700)  
Zeus Components  
1750 W. Broadway  
(407) 365-3000  
FAX: 407-365-2356

St. Petersburg (33702)  
Hamilton/Avnet, #25  
3197 Tech Drive No.  
(813) 576-3930  
TWX: 810-863-0374  
FAX: 813-577-6004

Winter Park (32792)  
Hamilton/Avnet  
6947 University Blvd.  
(407) 657-9018  
TWX: 810-853-0322  
FAX: 407-678-1878

### GEORGIA

Norcross (30092)  
Hamilton/Avnet, #15  
5825 Peachtree Corners E-D  
(404) 447-7575  
TWX: 810-766-0432  
FAX: 404-447-7526

Norcross (30071)  
Future Electronics  
3000 Northwoods Parkway  
Suite 295  
(404) 441-7676  
FAX: 404-441-7580

Norcross (30093)  
Marshall  
5300 Oakbrook Pkwy., Ste. 240  
(404) 923-6750  
TWX: 810-766-3969  
FAX: 404-923-2743

Norcross (30071)  
Pioneer/GA  
3100 F Northwoods Place  
(404) 448-1711  
FAX: 404-446-8270

### ILLINOIS

Bonsenville (60106)  
Hamilton/Avnet, #10  
1130 Thorndale Avenue  
(312) 860-7780  
TWX: 910-227-0060  
FAX: 312-860-8530

Elk Grove Village (60007)  
Pioneer/Chicago  
1551 Carmen Drive  
(312) 437-8683  
TWX: 910-222-1834  
FAX: 312-437-0551

Schaumburg (60195)  
Marshall  
1261 Wiley Road, #F  
(312) 490-0755  
TWX: 910-258-0036  
FAX: 312-490-0569

### INDIANA

Carmel (46032)  
Hamilton/Avnet, #28  
485 Grady Drive  
(317) 844-8333  
FAX: 317-844-5921

Indianapolis (46278)  
Marshall  
6990 Corporate Drive  
(317) 297-0483  
FAX: 317-297-2787

Indianapolis (46250)  
Pioneer Indiana  
6408 Castleplace Drive  
(317) 849-7300  
TWX: 810-260-1794  
FAX: 317-842-5998

### IOWA

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915 33rd Avenue  
(319) 362-4757

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Lenexa (66214)  
Marshall  
8321 Melrose Drive  
(913) 492-3121

Overland Park (66215)  
Hamilton/Avnet, #58  
9219 Quivira Road  
(913) 541-7922  
TWX: 910-743-0005

### MARYLAND

Columbia (21045)  
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6822 Oak Hall Lane  
(301) 995-3500 (MD)  
(301) 621-5410 (DC)  
FAX: 301-995-3593

Columbia (21045)  
Zeus Components  
8930-A Route 108  
(301) 997-1118  
FAX: 301-964-9784  
Galthersburg (20877)  
Marshall  
8445 Helgerman Court  
(301) 840-9450  
TWX: 710-828-9748  
FAX: 301-840-8538

Galthersburg (20760)  
Pioneer/Washington  
9100 Gaither Road  
(301) 921-0660  
TWX: 710-828-0545  
FAX: 301-921-4255

### MASSACHUSETTS

Lexington (02173)  
Pioneer  
44 Hartwell Ave.  
(617) 861-9200  
FAX: 617-863-1547

Lexington (02173)  
Zeus  
429 Marrett Road  
(617) 863-8800  
FAX: 617-863-8807

Peabody (01960)  
Hamilton/Avnet Electronics  
100 Centennial Drive  
(617) 531-7430 (Sales)  
Easylink: 62912457

Westborough (01581)  
Future Electronics  
133 Filders Road  
(617) 366-2400  
FAX: 617-366-1195

Wilmington (01887)  
Marshall  
33 Lipton Dr.  
(617) 658-0810  
FAX: 617-658-7608

### MICHIGAN

Grand Rapids (49508)  
Hamilton/Avnet, #67  
2215 29th Street S.E. A-5  
(616) 243-8805  
FAX: 616-243-0028

Grand Rapids (49508)  
Pioneer  
4505 Broadmoor Ave. SE  
(616) 698-1800  
FAX: 616-698-1831

Livonia (48150)  
Hamilton/Avnet, #66  
32487 Schoolcraft  
(313) 522-4700  
TWX: 810-242-8775  
FAX: 313-522-2624

Livonia (48150)  
Marshall  
31067 Schoolcraft  
(313) 525-5850  
FAX: 313-525-5855

Livonia (48150)  
Pioneer/Michigan  
13485 Stamford  
(313) 525-1800  
TWX: 810-242-3271  
FAX: 313-427-3720

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Eden Prairie (55344)  
Pioneer/Twin Cities  
7625 Golden Triangle Dr., Ste. G  
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TWX: 910-576-2738  
FAX: 612-944-3794

Minnetonka (55343)  
Hamilton/Avnet, #63  
12400 Whitewater Dr.  
(612) 932-0600  
TWX: 910-576-2720

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Marshall  
3800 Annapolis Lane  
(612) 550-2211  
FAX: 612-559-8321

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Hamilton/Avnet, #05  
13743 Shoreline Court  
(314) 344-1200  
TWX: 910-762-0606

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Norcross (03103)  
Hamilton/Avnet, #75  
444 E. Industrial Park Drive  
(603) 624-9400  
TWX: 710-474-3255  
FAX: 603-624-2402

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Hamilton/Avnet, #14  
One Keystone Avenue  
(609) 424-0100  
TWX: 710-940-0262  
FAX: 609-751-8624

Fairfield (07006)  
Hamilton/Avnet, #19  
10 Industrial Road  
(201) 575-3390  
TWX: 710-734-4388  
FAX: 201-882-0095

Fairfield (07006)  
Marshall  
101 Fairfield Road  
(201) 882-0320  
TWX: 710-989-7052  
FAX: 201-882-0095

Mt. Laurel (08054)  
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158 Galthersburg  
(609) 234-9100 (NJ)  
(215) 627-1920 (PA)  
TWX: 710-837-1364  
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Pinebrook (07058)  
Pioneer/NJ  
45 Route 46  
(201) 575-3510  
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FAX: 201-575-3454

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Bell Industries  
11725 Linn N.E.  
(505) 292-2700  
TWX: 910-989-0625

Albuquerque (87106)  
Hamilton/Avnet, #22  
2524 Baylor Drive S.E.  
(505) 766-1500  
TWX: 910-989-0614  
FAX: 505-243-1395

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FAX: 607-722-9562

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Summit, Inc.  
816 Main Street  
(716) 887-2800  
TWX: 710-522-1692  
FAX: 716-887-2866

East Syracuse (13206)  
Hamilton/Avnet, #08  
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(315) 437-2642  
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FAX: 315-432-0740

Fairport (14450)  
Pioneer/Rochester  
840 Fairport Park  
(716) 381-7070  
FAX: 716-381-5955

Hauspaug (11788)  
Hamilton/Avnet, #20  
933 Motor Parkway  
(516) 231-9800  
TWX: 510-224-6166

Hauspaug (11788)  
Marshall  
275 Oser Avenue  
(516) 273-2424  
FAX: 516-434-4775

Johnson City (13790)  
Marshall  
129 Brown Street  
(607) 798-1611  
TWX: 510-252-0194  
FAX: 607-797-7031

Port Chester (10523)  
Zeus Components  
100 Midland Avenue  
(914) 837-7400  
FAX: 914-937-2553

Rochester (14623)  
Hamilton/Avnet, #61  
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(716) 475-9130  
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2110 Smithtown Ave.  
(516) 737-4500  
FAX: 516-737-4520

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1085 Old Country Road  
(516) 997-8868  
TWX: 516-221-0876  
FAX: 516-957-6375

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Pioneer/Long Island  
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(516) 921-8700  
FAX: 516-921-2143

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1515 Mockingbird Lane, Ste. 801  
(704) 529-5500  
FAX: 704-527-2222

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FAX: 704-622-8564

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FAX: 919-872-4435

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Marshall  
5221 N. Blvd.  
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TWX: 910-997-5209

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FAX: 216-587-3906

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(513) 438-6700  
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FAX: 513-439-6711

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Marshall  
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(513) 898-4480  
TWX: 810-459-1735  
FAX: 513-236-0870

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Pioneer/Dayton  
4433 Interpoint Blvd.  
(513) 236-9900  
TWX: 810-459-1622  
FAX: 513-236-6133

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Zeus Components  
3500 Park Center Drive  
(513) 454-1225  
FAX: 513-454-0494

Solon (44139)  
Hamilton/Avnet, #62  
30325 Bainbridge Rd., Bldg. A  
(216) 349-5100  
FAX: 216-349-1894

Solon (44139)  
Marshall  
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FAX: 216-248-2312

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Hamilton/Avnet, #79  
777 Brooks Edge Boulevard  
(614) 882-7000  
FAX: 614-882-8650

### OKLAHOMA

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3158 S. 108th E. Ave., Ste # 274  
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5250 N.E. Elam Young Parkway  
Suite 600  
(503) 640-6000  
TWX: 910-460-2203

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Hamilton/Avnet, #27  
6024 S.W. Jean Road  
Bldg. C, Suite 10  
(503) 635-8836  
TWX: 910-455-8179

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Horsham (19044)  
Pioneer/Horsham  
261 Gibraltar Road  
(215) 674-4000  
TWX: 510-665-6778  
FAX: 215-674-3107

Pittsburgh (15222)  
Hamilton/Avnet, #43  
2800 Liberty Avenue, Bldg. E.  
(412) 281-4150  
FAX: 412-281-8662

Pittsburgh (15238)  
Pioneer/Pittsburgh  
259 Kappa Drive  
(412) 782-2300  
TWX: 710-795-3122  
FAX: 412-963-8255

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4257 Kellway Circle  
(214) 733-4300  
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FAX: 214-250-0216

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Hamilton/Avnet, #26  
1807A W. Braker Lane  
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TWX: 910-874-1319

Austin (78754)  
Marshall  
8504 Cross Park Dr.  
(512) 837-1991  
TWX: 910-997-5196

Austin (78758)  
Pioneer/Austin  
1826 Kramer Lane  
(512) 835-4000  
FAX: 512-835-9829

Austin (78758)  
Quality Components  
2120-M Braker Lane  
(512) 835-0220  
TLX: 324930

Austin (78758)  
Wyle Distribution  
2120-F W. Braker Lane  
(512) 834-9957

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Marshall  
2045 Chenault St.  
(214) 233-5200

Dallas (75240)  
Pioneer/Dallas  
13710 Omega Road  
(214) 263-3168  
FAX: 214-490-6419

Houston (77040)  
Marshall  
7250 Langtry  
(713) 895-9200

Houston (77036)  
Pioneer/Houston  
5853 Point West Drive  
(713) 988-5555  
TWX: 910-881-1606

Houston (77099)  
Wyle Distribution  
11001 S. Wilcrest, Ste. 100  
(713) 879-9953

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Hamilton/Avnet, #16  
2111 W. Walnut Hill Lane  
(214) 550-7755  
TWX: 910-860-5929

Richardson (75083)  
Wyle Distribution  
1810 N. Greenville Avenue  
(214) 235-9953  
TWX: 310-378-7663

Richardson (75081)  
Zeus Components  
1800 N. Glenville Drive  
Suite 120  
(214) 783-7010  
TWX: 910-867-9422

Stafford (77477)  
Hamilton/Avnet, #11  
4850 Wright Road 190  
(713) 240-7735  
TWX: 910-881-5523

Sugarland (77478)  
Quality Components  
1005 Industrial Boulevard  
At Bournewood  
(713) 240-2255  
FAX: 713-240-6988

### UTAH

Salt Lake City (84119)  
Hamilton/Avnet, #09  
1585 West 2100 South  
(801) 972-2800  
TWX: 910-925-4018

Salt Lake City (84115)  
Marshall  
466 Lawndale Dr., Ste. #C  
(801) 485-1551  
FAX: 801-487-0936

West Valley City (84119)  
Wyle Laboratories-EMG  
1325 W. 2200 S.  
Ste. E  
(801) 974-9953  
FAX: 801-972-2524

### WASHINGTON

Bellevue (98007)  
Marshall  
14102 N.E. 21st St.  
(206) 747-9100  
FAX: 206-641-2657

Redmond (98052)  
Hamilton/Avnet, #07  
17761 N.E. 78th Pl.  
(206) 881-6697  
FAX: 206-867-0159

Redmond (98052)  
Wyle Distribution Group  
15385 N.E. 90th Street  
(206) 881-1150  
FAX: 206-881-1567

### WISCONSIN

Milwaukee (53214)  
Marsh Electronics, Inc.  
1563 South 101st Street  
(414) 475-6000  
FAX: 414-771-2847

New Berlin (53151)  
Hamilton/Avnet, #57  
2975 Moorland Road  
(414) 784-4510  
TWX: 910-262-118

Waukesha (53186)  
Bell Industries  
W2279913 W. Mound Dr.  
(414) 547-8979  
FAX: 414-547-6547

## Canadian Distributors

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Burnaby (V5M 3Z3)  
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2550 Boundary Road  
Ste. #115  
(604) 437-6667  
FAX: 604-294-1206

Burnaby (V5G 4J7)  
ITT Multicomponents  
3455 Gardner Court  
(604) 291-8866  
TWX: 610-929-3065  
FAX: 604-291-1227

Vancouver (V5K 4X7)  
Future Electronics  
1695 Boundary Road  
(604) 294-1166  
FAX: 604-294-1206

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Downsview (M3J 1Z3)  
Future Electronics  
82 St. Regis Crescent N.  
(416) 836-4771  
TWX: 610-491-1470

Mississauga (L4V 1M5)  
Hamilton/Avnet, #59  
6845 Rexwood Drive  
(416) 877-7432  
TWX: 610-492-8867

Nepean (K2E 7L5)  
Hamilton/Avnet, #60  
190 Colonade Road  
(613) 226-1700  
TLX: 0534971

Ottawa (K2C 3P2)  
Future Electronics  
Baxter Centre  
(450) Baxter Road  
(613) 820-8313

### ALBERTA

Calgary (T2E 6Z2)  
Hamilton/Avnet, #68  
2816 21st Street N.E.  
(403) 250-9380

### QUEBEC

Pointe Claire (H9R 5C7)  
Future Electronics  
237 Hymus Boulevard  
(514) 694-7710  
TWX: 610-421-3251  
FAX: 514-695-3707

St. Laurent (H4S 1P8)  
Hamilton/Avnet, #65  
2795 Rue Halpern  
(514) 335-1000  
TWX: 610-421-3731



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### AUSTRIA

Bacher Electronics GmbH  
Rotenmühlgasse 26  
A-1120 Wien  
TEL: (0222) 835646-0  
TEL: 131532  
FAX: (0222) 834276

### BELGIUM

J.P. Lemaire S.A.  
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B-1810 Waremme  
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TEL: 24810  
FAX: (02) 460-00-271

### DENMARK

Delco A.S.  
Højrevang 13  
DK 3450 Allerød  
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FAX: (02) 27-77-70

### IRE (IRELAND)

Hill Electronics  
Klymore Park North  
Ballyfermot  
Dublin 10  
TEL: 265299  
TELX: 90708

### FINLAND

Instrumentarium Elektronikka  
P.O. Box 64  
SF 02631 Espoo 63  
TEL: (90) 528 4304  
TELX: 124426 HAVUL SF  
FAX: (90) 502 1073

### FRANCE

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52164 Antony Cedex  
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TELX: 250067  
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32 Rue Grange Dame Rose  
92260 Meudon La Forêt  
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FAX: (1) 46.30.01.29  
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5 Rue Jean Zay  
42271 St. Priest En Jarez Cedex  
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TELX: 300021  
FAX: (1) 77.93.26.31  
I.T.T. Multicomposants  
Z.I. de Courtaboeuf  
Avenue des Andes  
91940 Les Ulis  
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TELX: 603351  
FAX: (1) 64.46.95.95  
SCAIB  
80 Rue d'Arcueil  
94523 Rungis Cedex  
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TELX: 204674F  
FAX: (1) 45.60.55.49

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7000 Stuttgart 70  
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EBV Elektronik GmbH  
Oberweg 6  
D-8025 Unterhaching  
TEL: 089-61105-1  
TELX: 524535  
FAX: 089-61105-230  
EBV Elektronik GmbH  
Weimarstr 48  
7000 Stuttgart 1  
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FAX: (0711) 613750  
EBV Elektronik GmbH  
Viersener Strasse 24  
4040 Neuss  
TEL: (02101) 530072  
TELX: 8517605  
FAX: 02101-593087  
EBV Elektronik GmbH  
Klebitzrain 18  
3006 Burgwedel 1 Hannover  
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TELX: 923694  
EBV Elektronik GmbH  
Schanckstr 99  
6000 Frankfurt M. 90  
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TELX: 413250  
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TELX: 184707  
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Albert Schwelzter-Ring 36  
2000 Hamburg 70  
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TELX: 2164484  
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2280 Schleswig  
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TELX: 221334  
Ulratronik GmbH  
Gewerbestr. 4  
8036 Herrsching  
TEL: (08152) 3709-0  
TELX: 526459  
FAX: (08152) 5183  
**ITALY**  
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Via Vittorio Veneto 8  
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Elektrotechniek BV  
P.O. Box 125  
2600 AC Delft  
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TELX: 38250  
FAX: 015-619194

### NORWAY

A.S. Kjell Bakke  
Øvre Rælingsvel 20  
P.O. Box 27  
N-2001 Lillestrøm  
TEL: (02) 83-02-20  
TELX: 19407  
FAX: (02) 831455

### PORTUGAL

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1100 Lisboa  
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### SPAIN

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Corazon de Maria, No. 7  
28002 Madrid  
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TELX: 23967  
FAX: (91) 416 19 71  
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Barcelona 11  
TEL: (93) 254 90 48

### SWEDEN

Komponentbolaget NAXAB  
Box 4115  
S-171-04 Solna  
TEL: 08-985140  
TELX: 17912 KOMP  
FAX: 08-7645451

### SWITZERLAND

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Grabenstrasse 9  
8952 Schlieren  
TEL: 01-730-0455  
TELX: 829070  
FAX: 01-730-9801

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# ERRATA

The data sheets for the devices listed below contain a typographical error in the electrical tables. You will notice we have incorporated into one test table the room temperature and min/max temperature parameter limits. Some of the tables incorrectly show the minimum temperature limits for ON resistance and leakages to be the same as the 25°C room temperature specifications. This should be changed so that the minimum temperature limits match the 125°C limits.

The corrections required are to change the minimum temperature test (referenced as test #2) to be on the same line as the maximum temperature test (referenced test #3).

Example:

Incorrect

Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -10 \text{ mA}, V_D = \pm 8.5 \text{ V}$ $V_+ = 13.5 \text{ V}, V_- = -13.5 \text{ V}$	1,3 2	25		35 45		35 45	$\Omega$
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Correct

Drain-Source ON Resistance	$r_{DS(ON)}$	$I_S = -10 \text{ mA}, V_D = \pm 8.5 \text{ V}$ $V_+ = 13.5 \text{ V}, V_- = -13.5 \text{ V}$	1 2,3	25		35 45		35 45	$\Omega$
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The data sheets affected are:

D125	DG221	DG508A/509A
D129	DG243	DG526/527
D169	DG300A/301A/302A/303A	DG528/529
D470	DGP303A	DG534
DG123	DG304A/305A/306A/307A	DG535
DG125	DG308A/309	DG536
DG126/129/140	DG381A/384A/387A/390A	DG538
DG133/134/141	DG411/412/413	DG540
DG139/142/145	DG421/423/425	DG541
DG143/144/146	DG441/442	DG542
DG172	DG444/445	DG5040-5045
DG180/181/182	DG480	DG601
DG183/184/185	DG485	G118
DG186/187/188	DG501	G119
DG189/190/191	DG503	Si3002
DG200A	DG506A/507A	
DGP201A	DGP508A	





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