SiS968

MuTIOL Media I/O Programming Guide

Version 0.84

Jan. 8, 2007

Revision History

Date	Rev	Description
Sept. 4, 2006	0.15	1. Initial Release
Oct. 11, 2006	0.3	1 .update IDE Reg 54 [20:21]and [16:17] 2 .update SATA Reg 90h[24:25] 3. Add SMBus Programming Guide 4. Add EEPROM Programming Guide 5. Minor modification on chapter 2.1, 2.2, 2.8.1, 3 and 6.
Oct .20.2006	0.4	1:Update SATA Reg A2h 2:Update SATA Reg A6h 3:Update ACPI Reg 63h setting 4:Update USB 2.0 setting
Nov.6.2006	0.5	1:Update ACPI Reg B0h~B1h,Reg B9h~BBh and Reg C6h 2:Update LPC Reg 40h[0] 3:Update AHCI Reg A0h[21] and Reg 54h[22],54h[26] 4;Update ACPI Reg 79h~7Ah,Reg 7Fh and Reg B4h~b7h
Nov.21.2006	0.6	1:update PATA Reg 00h~01h,Reg 09h and 51h 2:update SATA Reg 00h~01h,Reg 56h~57.Reg 67h and Reg 81~82h 3:update PCIE Reg 46h[0] and Reg Eah[6]
Nov.29.2006	0.7	1.updata LPC Register 70h
Jan. 08. 2007	0.84	B0 Initial Release 1;Update ACPI Register 7Dh 2:Update GPIOx table 3;Update LPC Register 69h 4:Update LPC Configuration Table 5:Update LPC Register FBh 6:Update RTC Register table 7:Update PCIE Register 44h,49h,59h and 5Ah 8:Update ACPIGPWAK Table 9:Update LPC Register F6h 10:Update LPC Register 7Dh 11:Update ACPI Register 20h~29h 12:update ACPI Register C4h 13:update USB 2.0 configuraton 40h~48h 14:update ACPI register 9Dh

Content

1. PCI Devices and Functions

Bus #	Device #	Function #	Device ID	IDSEL	INTX	Device Function
Bus 0	Device 2	Function 0	0968h	AD13	N/A	LPC
Bus 0	Device 2	Function 5	5513h/1180h/1181h	AD13	INTA	IDE
Bus 0	Device 3	Function 0	7001h	AD14	INTE	USB 1.1 #0
Bus 0	Device 3	Function 1	7001h	AD14	INTF	USB 1.1 #1
Bus 0	Device 3	Function 3	7002h	AD14	INTG	USB 2.0
Bus 0	Device 4	Function 0	0191h	AD15	INTD	LAN
Bus 0	Device 5	Function 0	1183h/1184h/1185h	AD16	INTB	SATA
Bus 0	Device 6	Function 0	000Ah	AD17	INTA/B/C/D	PCI Express 0
Bus 0	Device 7	Function 0	000Ah	AD18	INTA/B/C/D	PCI Express 1
Bus 0	Device F	Function 0	7502h	AD21	INTC	HD Audio

2. LPC (Device2:Function0) Register Summary / Description

2.1. LPC Bridge Configuration Registers

Address	Access	Register Name
00-01h	RO	Vendor ID
02-03h	RO	Device ID
04-05h	RO	Command Register
06-07h	RO	Status register
08h	RO	Revision ID
09-0Bh	RO	Class Code
0Ch	RO	Cache Line Size
0Dh	RO	Master Latency Timer
0Eh	RO	Header Type
0Fh	RO	Built-in Self Test
10-2Bh	RO	Reserved
2C-2Dh	RO	Subsystem Vendor ID
2E-2Fh	RO	Subsystem ID
30-3Fh	R/W	Reserved
40h	R/W	BIOS control register
41-44h	R/W	Internal INT[A, B, C, D]N routing register
45h	R/W	Flash ROM control register
46h	R/W	INIT enable register
47h	R/W	USB Legacy IRQ controller register
48h	R/W	RTC control register
49h	R/W	PCI device HIDE register
4A-4Bh	R/W	Reserved
4C-4Fh	RO	Shadow register for ICW of Master INT
50-53h	RO	Shadow register for ICW of Slave INT
54-55h	RO	Shadow register for OCW of Master INT
56-57h	RO	Shadow register for OCW of Slave INT
58h	RO	CTC shadow register 1
59h	RO	CTC shadow register 2
5Ah	RO	CTC shadow register 3
5Bh	RO	CTC shadow register 4
5Ch	RO	CTC shadow register 5
5Dh	RO	CTC shadow register 6

5Eh	RO	CTC shadow register 7
5Fh	RO	CTC shadow register 8
60-63h	R/W	Internal INT[E, F, G, H]N routing register
64h	R/W	Priority Timer
65h	R/W	PHOLD Timer
66h	RO	Shadow register for ISA port 70h
67h	R/W	IRQ Control
68h	R/W	ACPI/SCI IRQ routing
69h	R/W	Serial Interrupt Control
6Ah	R/W	Serial Interrupt Enable
6Bh	R/W	Reserved
6Ch	R/W	APIC Control register
6D-6Eh	R/W	Reserved
6Fh	R/W	APIC Version Control
70h	R/W	High-Precision Event Timer Control Register
71h	R/W	High-Precision Event Timer BASE Address and Control Register
72-73h	R/W	IO PULLUP/PULLDOWN Select
74-75h	R/W	ACPI Base Address
76h	R/W	PCIE control
77h	R/W	Internal PCI Device Enable 1
78h	R/W	RTCRAM128 Base Address
79h	R/W	Memory Lock Control Mode
7Ah	R/W	TRAP Frequency Select Register
7Bh	R/W	Internal Control Enable
7Ch	R/W	Internal PCI Device Enable 2
7Dh	R/W	SATA IDSEL
7Eh	R/W	HDA Enable
7Fh	R/W	Test Mode
80-84h	R/W	Protect Memory Address 1
85-89h	R/W	Protect Memory Address 2
8A-8Ch	R/W	128Bytes Protect Memory Address
8D-90h	R/W	Reserved
91-93h	R/W	Watchdog Timer Base Address
94h	R/W	Reserved
95h	R/W	SIRQ control

96h	R/W	ROM Size enable bit
97h	R/W	BIOS ROM Size for FWH and SPI
98h-99h	R/W	SPI Base Address
9Ah	R/W	SMB control
9Bh	R/W	SMB Base Address
9Ch-9Fh	R/W	FWH_ID SEL 1~4
A0h-A3h	R/W	Device interrupt routing options
C0h	R/W	Link & Queue Control 1
C1h	R/W	Link & Queue Control 2
C2h-C3h	R/W	Top Bound Control
C4h-C5h	R/W	Allocation of PCI-Hole Area I
C6h-C7h	R/W	Allocation of PCI-Hole Area II
C8-C9h	R/W	Shadow RAM Read Attribute Control
CAh-CBh	R/W	Shadow RAM Write Attribute Control
CCh	R/W	SB MuTIOL™ Interface Control 1
CDh	R/W	SB MuTIOL™ Interface Control 2
CEh	R/W	SB MuTIOL™ Interface Control 3
CFh	R/W	MuTIOL (Multi-threaded IO Link) Control 1
D0h	R/W	MuTIOL (Multi-threaded IO Link) Control 2
D1h	R/W	MuTIOL (Multi-threaded IO Link) Control 3
D2h	R/W	MuTIOL (Multi-threaded IO Link) Control 4
D3h	R/W	MuTIOL (Multi-threaded IO Link) Control 5
D4h	R/W	MuTIOL™-to-PCI Non-Post Cycle Retry Behavior Control
D5h	R/W	PCI Master Characteristics Option 1
D6h	R/W	PCI Master Characteristics Option 2
D7h	R/W	PCI Arbiter Characteristics Option
D8h	R/W	PCI Slave Characteristics 1
D9h-DAh	R/W	PCI Slave Characteristics 2
DBh	R/W	PCI Slave Characteristics 3
DCh-DFh	R/W	PCI Arbiter Priority Level Control
E0h-EBh	R/W	Reserved. DO NOT CHANGE THESE REGISTERS.
EC-EEh	R/W	Gating Clock Function
EF	R/W	Reserved. DO NOT CHANGE THESE REGISTERS.
FBh	R/W	ASL EDC Function Register

2.2. LPC Bridge Configuration Registers (D2:F0)

Device	IDSEL	Function Number
LPC Bridge	AD13	0000b

Register 00h~01h Vendor ID

Power on value: 1039h

Recommended value: 1039h

Access: Read Only

Bit	Access	Description	Power On Value	Recom. Setting
15:0	RO	Vendor Identification Number Default value is 1039h	1039h	1039h

Register 02h~03h Device ID

Power on value: 0968h

Recommended value: 0968h

Access: Read Only

Bit	Access	Description	Power On Value	Recom. Setting
15:0	RO	Device Identification Number Default value is 0968h	0968h	0968h

Note: Write a 1 to Reg40 bit 6 will change the Device ID to 0008h.

Register 04h~05h Command Register

Power on value: 000Ch

Recommended value: 000Fh

Access: Read Only, Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
15:4	RO	Reserved. Read as 0	0	0

3	RO	Read as 1 to indicate that the device is allowed to monitor special cycles.	1b	1b
2	RO	Read as 1 to indicate that the device is able to become PCI bus master.	1b	1b
1	R/W	Response to Memory Space Accesses.	0b	1b
0	R/W	Response to I/O Space Accesses.	0b	1b

Register 06h~07h Status

Power on value: 0200h

Recommended value: xxxxh

Access: Read Only

Bit	Access	Description
15:14	RO	Reserved. Read as 0
13	RO/WC	Received Master-Abort This bit will be set to 1 when the current transaction is terminated with master-abort. This bit can be cleared to 0 by writing a 1 to it.
12	RO/WC	Received Target-Abort This bit will be set to 1 when the current transaction is terminated with target-abort. This bit can be cleared to 0 by writing a 1 to it.
11	RO	Reserved. Read as 0.
10:9	RO	DEVSEL# Timing The two bits are hardwired to 01 to indicate positive decode with medium timing.
8:0	RO	Reserved. Read as 0.

Register 08h Revision ID

Power on value: 01h (968B0)

Recommended value: 01h

Access: Read Only

Bit	Access	Description
7:0	RO	Revision Identification Number

Register 09h~0Bh Class Code

Power on value: 060100h

Recommended value: 060100h

Access: Read Only

Bit	Access	Description
23:0	RO	Class Code Default value is 060100h.

Register 0Ch Cache Line Size

Power on value: 00h

Recommended value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Cache Line Size

Register 0Dh Master Latency Timer

Power on value: 00h

Recommended value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	Master Latency Timer

Register 0Eh Header Type

Power on value: 80h

Recommended value: 80h

Access: Read Only

Bit	Access	Description
7:0	RO	Header Type Default value is 80h

Register 0Fh BIST

Power on value: 00h

Recommended value: 00h

Access: Read Only

Bit	Access	Description
7:0	RO	BIST Default value is 00h

Register 10h~2Bh Reserved

Power on value: 00h

Recommended value: 00h

Access: Read Only (Read as 0)

Register 2Ch~2Fh Subsystem ID & Subsystem Vendor ID

Power on value: 0000_0000h

Recommended value: 0000_0000h

Access: Read/Write or Read Only

When LPC Reg 40h bit 5 is 0, these registers are read/write.

When LPC Reg 40h bit 5 is 1, these registers are read only.

Bit	Access	Description
31:16	RW/RO	Subsystem ID
15:0	RW/RO	Subsystem Vendor ID

Register 30h~3Fh Reserved

Power on value: 00h

Recommended value: 00h

Access: Read Only (Read as 0)

Register 40h BIOS Control Register

Power on value: 00h

Recommended value: 1011_00- 1b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7	R/W	**ACPI Enable** 0: Disable 1: Enable When enabled, ACPI register at IO space address as defined in ACPI base registers (Reg 74h~75h) can be accessed.	0b	1b
6	R/W	**Device ID Selection** 0: LPC Bridge Device ID is 0968. 1: LPC Bridge Device ID is 0008.	0b	0b
5	R/W	**SSID/SVID read/write control.** 0: Read/write 1: Read only	0b	1b
4	R/W	**PCI to LPC Posted Write Buffer Enable** 0: Disable 1: Enable	0b	1b
3	R/W	**Subtractive Decode to Internal registers Enable** 0: Disable 1: Enable When this bit is enabled, SiS968 will do subtractive decode for the internal registers access.	0b	0b
2	R/W	**Reserved.**	0b	0b
1	R/W	**BIOS positive Decode Enable** When enabled and SPI is used, the memory address FFF8_0000h ~ FFFF_FFFFh and the range defined by LPC Reg 97h and Reg 96h bit 7 will be positively decoded. Otherwise, it will be subtractively decoded. For LPC ROM and FWH, the memory range of FFB0_0000h ~ FFBF_FFFFh are controlled by this bit. 0: Disable 1: Enable	0b	-
0	R/W	**Reserved**	0b	1b

Register 41/42/43/44h Internal INTAN, INTBN, INTCN and INTDN Routing Register

Power on value: 80/80/80/80h

Recommended value: - - / - - / - - / - -h

Access: Read/Write

Bit	Access	Description
7	R/W	**Routing Enable** 0: Enable 1: Disable When enabled, internal INTAN, INTBN, INTCN and INTDN will be remapped to the IRQ channel specified below.
6:4	RO	**Reserved.** Read as 0
3:0	R/W	**IRQ Routing Table**

Bits	IRQx#	Bits	IRQx#	Bits	IRQx#
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	Reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Note1: More than one of INT[A:D]N can be routed to the same IRQ line, but that IRQ line should be programmed to level-triggered mode.

Note2: For external PCI INTA#/B#/C#/D# and the interrupt pin from PCIE#1, PCIE2, PATA, SATA, Audio and GMAC, they can be routed to internal INT[A,B,C,D,E,F,G,H]N by programming LPC Reg A0h ~ A3h.

Note3: Internal INT[E,F,G,H]N routing register is defined at LPC Reg. 60h ~ 63h.

Note4: For APIC enabled mode, the internal INT[A~H]N are connected to INT[16~23] separately.

Register 45h Flash ROM Control Register

Power on value: 40h

Recommended value: 00-0_0000b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Flash EPROM Control Bit** If bit 7 is set to '0' after CPURST de-asserted, EPROM can be flashed when bit 6 is set to '1'. Once bit 7 is set to '1', EPROM can not be flashed until the system is reset.	01b	00b

5	R/W	**INTR glitch filter for K8 processor** 0: Disable 1: Enable	0b	1b(K8) 0b(P4/K7)
4:0	R/W	**Reserved**	00000b	00000b

Register 46h INIT Enable Register

Power on value: 00h

Recommended value: 20h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Hardware reset initiated by software** When both set to 1, hardware reset will be generated to CPU.	00b	00b
5	R/W	**INIT Enable** 0: Disable 1: Enable the assertion of INIT# if applicable.	0b	1b
4:2	R/W	**Reserved**	000b	000b
1	R/W	**A20M# Output Control** 0: Enable the assertion of A20M# if applicable. 1: Disable the assertion of A20M#, i.e., A20M# will be high at all times.	0b	0b
0	R/W	**Reserved**	0b	0b

Register 47h USB Legacy IRQ Controller Register

Power on value: 51h

Recommended value: 80h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**USB Legacy IRQ Enable** 0: Disable 1: Enable	0b	1b
6	R/W	**Reserved**	1b	0b
5	R/W	**Reserved**	0b	0b

4	R/W	**Reserved**	1b	0b
3	R/W	**Reserved**	0b	0b
2	R/W	**Reserved**	0b	0b
1	R/W	**Reserved**	0b	0b
0	R/W	**Reserved**	1b	0b

Register 48h RTC Control Register

Power on value: 10h

Recommended value: 12h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**RTC Extended Bank Enable (EXTEND_EN)** 0: Disable 1: Enable When this bit is enabled, the upper 128 bytes of RTC SRAM can be accessed.	0b	0b
6	R/W	**Automatic Power Control Registers (APCREG_EN) Enable** 0: Disable 1: Enable When this bit is enabled, APC registers can be accessed.	0b	0b
5	R/W	**Instant Power-Off Enable (INSTOFF_EN)** Before enabling this function, the bit1 at APC Register 04h should be enabled. System will be powered off if GPIO2_STS is set.	0b	0b
4	RO	**Internal RTC Status** 0: Disable 1: Enable (default=1)	1b	1b

3	R/W	**Upper 128-byte Lock** 0: Disable. Access to these bytes in the upper RTC RAM range does not be locked. 1: Enable. Locks reads and writes to bytes 38~3Fh in the upper 128-byte bank of the RTC RAM. Write cycles to this range will have no effect and read cycles will not return any particular guaranteed value. Write once, When the bit is enabled, the upper 38~3Fh will be locked until next reset.	0b	-
2	R/W	**Lower 128-byte Lock** 0: Disable. Access to these bytes in the lower RTC RAM range does not be locked. 1: Enable. Locks reads and writes to bytes 38~3Fh in the lower 128-byte bank of the RTC RAM. Write cycles to this range will have no effect and read cycles will not return any particular guaranteed value. Write once, When the bit is enabled, the lower 38~3Fh will be locked until next reset.	0b	-
1:0	R/W	**Reserved**	00b	10b

Register 49h Device Hide Register

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	Reserved	**00b**	**00b**
5:0	R/W	**Device Hide[5:0]** When this bit is enabled, the device which IDSEL is AD[25:20] will not see its IDSEL go active. Then the device will not respond to PCI configuration cycles and the processor will think the device is not present. 0: Disable. 1: Enable.	0	0

Register 4Ah Reserved

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Register 4Bh Reserved

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Register 4C~4Fh Shadow Register for ICW of Master INTC

Power on value: 0000_0000h

Recommended value: xxxx_xxxxh

Access: Read Only

Bit	Access	Description
31:0	RO	Reflect ICW1, ICW2, ICW3 and ICW4 of the master interrupt controller

Register 50~53h Shadow Register for ICW of Slave INTC

Power on value: 0000_0000h

Recommended value: xxxx_xxxxh

Access: Read Only

Bit	Access	Description
31:0	RO	Reflect ICW1, ICW2, ICW3 and ICW4 of the slave interrupt controller

Register 54~55h Shadow Register for OCW of Master INTC

Power on value: 0000h

Recommended value: xxxxh

Access: Read Only

Bit	Access	Description
15:0	RO	Reflect OCW2 and OCW3 of the master interrupt controller

Register 56~57h Shadow Register for OCW Slave INTC

Power on value: 0000h

Recommended value: xxxxh

Access: Read Only

Bit	Access	Description
15:0	RO	Reflect OCW2 and OCW3 of the slave interrupt controller

Register 58h CTC Shadow Register 1

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect low byte of the initial count number of CTC Counter 0

Register 59h CTC Shadow Register 2

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect high byte of the initial count number of CTC Counter 0

Register 5Ah CTC Shadow Register 3

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect low byte of the initial count number of CTC Counter 1

Register 5Bh CTC Shadow Register 4

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect high byte of the initial count number of CTC Counter 1

Register 5Ch CTC Shadow Register 5

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect low byte of the initial count number of CTC Counter 2

Register 5Dh CTC Shadow Register 6

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect high byte of the initial count number of CTC Counter 2

Register 5Eh CTC Shadow Register 7

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:0	RO	Reflect Control word (43h) of the built-in CTC

Register 5Fh CTC Shadow Register 8

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:6	RO	**Reserved.** Read as 0.
5	RO	CTC counter2 Write count pointer status
4	RO	CTC counter1 Write count pointer status
3	RO	CTC counter0 Write count pointer status
2	RO	CTC counter2 Read count pointer status
1	RO	CTC counter1 Read count pointer status

0	RO	**CTC counter0 Read count pointer status** 0: LSB 1: MSB

Register 60/61/62/63h Internal INTEN, INTFN, INTGN and INTHN Routing Register

Power on value: 80/80/80/80h

Recommended value: - - / - - / - - / - -h

Access: Read/Write

Bit	Access	Description
7	R/W	**Internal INT[E,F,G,H]N Rounting Enable** 0: Enable 1: Disable (default)
6:4	RO	**Reserved.** Read as 0.
3:0	R/W	**Internal INT[E,F,G,H]N Routing Table**

Bits	IRQx#	Bits	IRQx#	Bits	IRQx#
0000	reserved	0110	IRQ6	1100	IRQ12
0001	reserved	0111	IRQ7	1101	reserved
0010	reserved	1000	reserved	1110	IRQ14
0011	IRQ3	1001	IRQ9	1111	IRQ15
0100	IRQ4	1010	IRQ10		
0101	IRQ5	1011	IRQ11		

Table 1 Internal devices fixed interrupt routing table

Function	Interrupt Pin	Function	Interrupt Pin
USB1.1.0	INTEN	USB2.0	INTGN
USB1.1.1	INTFN	--	INTHN

Register 64h Priority Timer

Power on value: 00h

Recommended value: FFh

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Priority Timer** There are two PCI maser candidates inside the south bridge competing for the PCI bus. They are LPC/DMA/Bus master, and APIC. The local arbiter with rotating scheme is adopted to co-ordinate their requests to become PCI master. The candidate issues request to the arbiter with a higher priority is the winner and is eligible to become PCI master when PCI grant is received. The priority timer is used to set a lower limit in terms of PCI clock for the winning candidate to continue its PCI transactions. The timer will start counting as soon as the winning candidate receives the PCI grant. Upon expiration, the winning candidate's priority will become lowest among the two and if the request issued by the other master is outstanding, it will lose the ownership of PCI grant. The maximum allowable value is FFh and the minimum allowable value is 00h. Priority Timer Enable bit is Reg7B bit1.	00h	FFh

Register 65h PHOLD# Timer

Power on value: 01h

Recommended value: C1h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7:0	R/W	**PHOLD# Timer** The PHOLD# timer sets an upper limit in terms of PCI clock for the assertion time of PHOLD# initiated by LPC/DMA/Bus Master and APIC. The timer starts and continues the counting when south bridge receives PCI grant. Upon expiration, the chip will be forced to de-assert PCI request to system arbiter. The maximum allowable value is FFh and the minimum allowable value is 01h. If a larger value is programmed, the master will be able to complete more PCI transactions by preventing the system arbiter from issuing grant to other PCI master candidates. The PCI bus bandwidth can be fairly shared by all PCI master candidates by properly program this timer. **Note: Bit 0 is read only. (always = 1)**	01h	C1h

Register 66h Shadow Register for ISA port 70h

Power on value: 00h

Recommended value: xxh

Access: Read Only

Bit	Access	Description
7:0	RO	**Reflect the content of ISA port 70h register.** Note: R48B6 should be 0.

Register 67h IRQ control

Power on value: 00h

Recommended value: 12h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:5	R/W	**Reserved**	000b	000b
4	R/W	**Serial IRQ sampled IOCHK# and SMI# phase control** 0: The sampled IOCHK# and SMI# on serial IRQ will be inverted. 1: The sampled IOCHK# and SMI# on serial IRQ will be not inverted.	0b	1b
3:2	R/W	**Reserved.**	00b	00b

1	R/W	**ISA IRQ13 Enable** 0: Disable 1: IRQ13 generated by assertion of FERR.	0b	1b
0	R/W	**FERR# polarity selection** 0: Low Active 1: High Active	0b	0b

Register 68h ACPI/SCI IRQ Routing Register

Power on value: 80h

Recommended value: - -h

Access: Read/Write

Bit	Access	Description					
7	R/W	**ACPI/SCI IRQ Routing Enable** 0: Enable 1: Disable (default)					
6:4	RO	**Reserved.** Read as 0.					
3:0	R/W	**IRQ Routing Table**					
		Bits	IRQx#	Bits	IRQx#	Bits	IRQx#
		0000	INTE#	0110	IRQ6	1100	IRQ12
		0001	INTF#	0111	IRQ7	1101	IRQ13
		0010	INTG#	1000	reserved	1110	IRQ14
		0011	INTH#	1001	IRQ9	1111	IRQ15
		0100	IRQ4	1010	IRQ10		
		0101	IRQ5	1011	IRQ11		

Register 69h Serial Interrupt Control Register

Power on value: 00h

Recommended value: -0b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Serial Interrupt (SIRQ) Control** 0: Disable 1: Enable	0b	1b

6	R/W	**Quiet/Continuous Mode** When LPC R95h bit 0 is set to 1, this bit must be set to 1. 0: Continuous 1: Quiet	0b	1-
5:2	R/W	**SIRQ Sample Period** 0000: 17 slots 0001: 18 slots 0010: 19 slots :::::::::::: 1111: 32 slots	0000b	0000b
1:0	R/W	**Start Cycle length** 00: 4 PCI clocks 01: 6 PCI clocks 10: 8 PCI clocks 11: Reserved	00b	00b

Note: If SIRQ EDC function want to enable, Quiet/Continuous Mode must be first set to 0, delay some time (>2us), then set to 1. In other word, Register 69h can be programmed to 80h first, delay 5us, then programmed to C0h.

Recommendation:
1. Set the LPC Reg 69h bit 6 in continues mode first in the early BIOS boot up.
2. Set the LPC Reg 69h bit 6 in quite mode latter at the position which should be > 5us to the step 1.
3. Set the LPC 95 bit 0 to enable the SIRQ power saving mode.

Register 6Ah Serial Interrupt Enable Register

Power on value: 00h

Recommended value: - -h

Access: Read/Write

Bit	Access	Description
7	R/W	**Serial INTA Enable** 0 : Disable 1 : Enable
6	R/W	**Serial INTB Enable**
5	R/W	**Serial INTC Enable**
4	R/W	**Serial INTD Enable**
3	R/W	**Serial SMI# Enable**

2	R/W	**Serial IOCHCK# Enable**
1:0	R/W	**Reserved.**

Register 6Bh Reserved

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Register 6Ch APIC Control Register

Power on value: 80h

Recommended value: 85h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Reserved**	1b	1b
6	R/W	**HT Function Enable (Fix Destination ID as 0)** 0: Disable 1: Enable	0b	0b
5:3	R/W	**Reserved**	000b	000b
2	R/W	**IRQPA_EN** IRQ Pin Assertion register function enable. 0: Disable 1: Enable	0b	1b
1	R/W	**Reserved**	0b	0b
0	R/W	**APICEN** IOAPIC Enable. 0: Disable 1: Enable	0b	1b

Register 6D ~ 6Eh Reserved

Power on value: 00h

Recommended value:

Access: Read/Write

Register 6Fh APIC Version Control Register

Power on value: 00h

Recommended value: 14h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**APIC Version Control** The version code of APIC register is programmable and controlled by this register.

Register 70h High-Precision Event Timer Control Register

Power on value: 00h

Recommended value: 10h (HPET disable)

93h (HPET enable)

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Timer 2 Legacy INT (INT1 ~ INT19) route capable** 0: Disable 1: Enable	0b	--
6:2	R/W	**Reserved**	00b	--
1	R/W	**High-Precision Event Timer_CNT_32/64bit_SEL** 0: 64 bit 1: 32 bit	0b	--
0	R/W	**High-Precision Event Timer_EN** 0: Disable 1: Enable	0b	--

Register 71h High-Precision Event Timer BASE Address and Control Register

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7:4	R/W	**High-Precision Event Timer_BASE_ADDRESS** High-Precision Event Timer Base Address FED0_X000h. (only 0h, 1h, 2h, 4h are valid)	0	0
3:0	R/W	**Reserved.**	0	0

Register 72~73h IO Buffer PULLUP/PULLDOWN Control Register

Power on value: FFFFh

Recommended value: FFFFh

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**IO Buffer PULLUP/PULLDOWN Control.** (default = 1)	FFFFh	FFFFh

Table 2 Signals and Control bits list

Signal	Control bit	Signal	Control bit
GPIO4	R72B7	(none)	R73B7
GPIO3	R72B6	GPIO6	R73B6
GPIO2	R72B5	GPIO5	R73B5
GPIO1	R72B4	REQ4#	R73B4
GPIO0	R72B3	REQ3#	R73B3
SIRQ	R72B2	REQ2#	R73B2
LAD[3:0]	R72B1	REQ1#	R73B1
LDRQ#	R72B0	REQ0#	R73B0

Register 74~75h ACPI BASE Register

Power on value: 0000h

Recommended value: - -00h

Access: Read/Write

Bit	Access	Description
15:8	R/W	**ACPI Base Register A[15:8]** ACPI registers will be located at the address specified here.

7:0	RO	**Reserved.** Read as 0.

Register 76h PCIE Control Register

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Reserved.**	0	0
5	R/W	**PCIEXP Controller1 Enable** 0: Enable 1: Disable	0b	0b
4	R/W	**PCIEXP Controller0 Enable** 0: Enable 1: Disable	0b	0b
3:0	R/W	**Reserved**	0	0

Register 77h Internal PCI Device Enable 1

Power on value: 00h

Recommended value: 000-_0100b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:5	R/W	**Reserved**	000b	000b
4	R/W	**TPM_EN** When enable, the following address would be transferred to LPC special cycle. a. FED4_0000h ~ FED4_3FFFh b. FED4_B000h ~ FED4_BFFFh 0: Enable 1: Disable	0b	-b
3:2	R/W	**Reserved**	00b	01b

1	R/W	**Mask USB A20M# Event** 0: Disable 1: Enable	0b	1b(K8) 0b(P4/K7)
0	R/W	**Reserved.**	0b	0b

Register 78h RTCRAM128 Base Address

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**RTCRAM128_ADDR[15:8]** This field specifies bits[15:8] of the IO address space for the additional 128-byte RTC power plane RAM. The additional RTC power plane RAM could be accessed from the offset 00h to 7Fh or 80h to FFh. The offset 80h and 00h pointed to the same RAM bytes. So does FFh and 7Fh…etc.	00h	00h

Register 79h Memory Lock Control Mode

Power on value: 00h

Recommended value: 000 -_- - - -b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:5	R/W	**Reserved.**	000b	000b
4	R/W	**128Byte_ROM_WLOCK_EN** 0: Disable 1: Enable Write once. When the bit is enabled, the write cycle to the protected memory (defined by reg8Ah-8Ch) would be locked till next Reset.	0b	-

3	R/W	**128Byte_ROM_RLOCK_EN** 0: Disable 1: Enable Write once. When the bit is enabled, the read cycle to the protected memory (defined by reg8Ah-8Ch) would be locked till next Reset.	0b	-
2	R/W	**ROM1/2_WLOCK_EN** 0: Disable 1: Enable Write once. When the bit is enabled, the write cycle to the protected memory (defined by reg80h-89h) could not be access. (this bit only can be access when SMI# is active)	0b	-
1	R/W	**ROM1/2_RLOCK_EN** 0: Disable 1: Enable Write once. When the bit is enabled, the read cycle to the protected memory (defined by reg80h-89h) could not be access. (this bit only can be access when SMI# is active)	0b	-
0	R/W	**ROM1/2_LOCK_EN** 0: Disable 1: Enable Write once, When the bit is enabled, the protected memory (defined by reg80h-89h) could not be access till next reset.	0b	-

Register 7Ah TRAP Frequency Select Register

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**TRAP[1:0]** 00: 133MHz 01: 66MHz	00b	00b

5	R/W	**TRAP_SEL** 0: Disable 1: Enable When the bit is enabled, the TRAP value will change to Reg7A bit[2:1] value after next PCIRST.	0b	0b
4:0	R/W	**Reserved.**	0	0

Register 7Bh Internal Control Enable

Power on value: 00h

Recommended value: 1000_- - 00b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**DWIOR_EN** If enabled, LPC Bridge can accept a double word I/O read to the internal legacy device of south bridge. 1: Enable(Recommended) 0: Disable	0b	1b
6:4	R/W	**Reserved**	000b	000b
3	R/W	**RTCRAM_EN** When enabled, the additional 128-byte RTCRAM specified by register 78h can be accessed. 0: Disable 1: Enable	0b	-
2	R/W	**Non Targeted I/O Cycle Forward Enable** When the bit is enable, STHBDG only decode internal IO cycles. For other not target IO cycles would not be forwarded to LPC bus. 0: Disable 1: Enable	0b	-
1	R/W	**Priority Timer Enable** When the bit is disable, the priority register (Reg64) is not used. 0: Disable 1: Enable	0b	0b
0	R/W	**Reserved**	0b	0b

Register 7Ch Internal PCI Device Enable 2

Power on value: 00h

Recommended value: 0000_- - - -b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:5	R/W	**Reserved**	000b	000b
4	R/W	**SATA Controller Enable** 0: Enable 1: Disable	0b	-
3	R/W	**IDE Controller Enable** 0: Enable 1: Disable	0b	-
2	R/W	**MAC Controller Enable** 0: Enable 1: Disable	0b	-
1:0	R/W	**Reserved**	0b	-

Register 7Dh SATA IDSEL

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Reserved**	0b	0b
6	R/W	**SATA IDSEL** 0: SATA IDSEL is AD16. (default) 1: SATA IDSEL is AD19.	0b	0b
5:0	R/W	**Reserved**	0	0

Register 7Eh HDA Enable

Power on value: 08h

Recommended value: 08h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/W	**Reserved**	0000b	0000b
3	R/W	**HDA Controller Enable** High Definition Audio Controller Enable 0: Disable 1: Enable	1b	1b
2:0	R/W	**Reserved**	000b	000b

Register 7Fh Test Mode

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Reserved**	0b	0b
6	R/W	**INTR De-assertion Timing Control** 0: Disable 1: Enable	0b	1b(K8) 0b(P4/K7)
5:3	R/W	**Reserved**	000b	000b
2	R/W	**ENLPCMEMCYC** 0: for memory access cycle, only the ROM address cycle will be forwarded to LPC bus 1: PCI to LPC bridge will do a subtractive decode for those not positive responding memory access cycle and forward to LPC bus.	0b	0b
1:0	R/W	**Reserved**	00b	00b

Register 80h~84h Protected Memory Address1

Power on value: 00_0000_0000h

Recommended value: --_----_----h

Access: Read/Write

Bit	Access	Description

39:20	R/W	**Protected Memory1 Ending Address[31:12]**
19:0	R/W	**Protected Memory2 Starting Address[31:12]** When protected, the memory read/write cycle to this range would not be forwarded to BIOS ROM. This register only can be written when its control bits is disable.

Register 85h~89h Protected Memory Address2

Power on value: 0000_0000_00h

Recommended value: - - - -_- - - -_- -h

Access: Read/Write

Bit	Access	Description
39:20	R/W	**Protected Memory2 Ending Address[31:12]**
19:0	R/W	**Protected Memory2 Starting Address[31:12]** When protected, the memory read/write cycle to this range would not be forwarded to BIOS ROM. This register only can be written when its control bits is disable.

Register 8Ah~8Ch 128Bytes Protected Memory Address

Power on value: 00_0000h

Recommended value: - -_- - - -h

Access: Read/Write

Bit	Access	Description
23:0	R/W	**128Bytes Protected Memory Address[31:8]** The Memory cycle matched the address and during the range address 00-7F would be protected. When protected, the memory access cycle to the range defined by this register would not be forwarded to BIOS ROM. This register only can be written when its control bits is disable.

Register 8Dh~90h Reserved

Power on value: 1F_0000_00h

Recommended value: 1F_0000_00h

Access: Read/Write

Register 91~93h Watchdog Timer Base Address

Power on value: 0000_00h

Recommended value: - - - -_- - h

Access: Read/Write

Bit	Access	Description
23:0	R/W	**Watchdog Timer Base Register ADD[31:8]** Watchdog Timer registers could be accessed by the memory address specified by this register.

Register 94h Reserved

Recommended value: xxh

Access: Read Only

Register 95h Reserved

Power on value: 00h

Recommended value: 01h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:1	R/W	**Reserved.**	0	0
0	R/W	**SIRQ gated clock function enable** 0: Disable 1: Enable	0b	1b

Register 96h ROM Size enable bit

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7	R/W	**128-Mbit ROM size enable** For SPI flash only, when enabled, the following memory address will be responded and forward to the SPI bus. a. FF70_0000h ~ FF7F_FFFFh. 0: disable 1: enable	0b	0b
6	R/W	**SPI_CS active select** 0: select SPI_CS0N 1: select SPI_CS1N	0b	0b
5:3	R/W	**Reserved.**	000b	000b
2:1	R/W	**SPI_CLK_SEL** SPI_CLK frequency Selection 00: 16.5MHz 01: 24MHz 1x: 33MHz	00b	00b
0	R/W	**Reserved**	0b	0b

Register 97h FWH enable bit

Power on value: 00h

Recommended value: 01h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**64M-Bit_EN** Refer to 8M-Bit_EN description. For SPI flash. a. FF80_0000h ~ FF8F_FFFFh For FWH. a. FF40_0000h ~ FF4F_FFFFh b. FF00_0000h ~ FF0F_FFFFh 0: Disable 1: Enable	0b	0b

6	R/W	**56M-Bit_EN** Refer to 8M-Bit_EN description. For SPI flash. a. FF90_0000h ~ FF9F_FFFFh For FWH. a. FF50_0000h ~ FF5F_FFFFh b. FF10_0000h ~ FF1F_FFFFh 0: Disable 1: Enable	0b	0b
5	R/W	**48M-Bit_EN** Refer to 8M-Bit_EN description. For SPI flash. a. FFA0_0000h ~ FFAF_FFFFh For FWH. a. FF60_0000h ~ FF6F_FFFFh b. FF20_0000h ~ FF2F_FFFFH 0: Disable 1: Enable	0b	0b
4	R/W	**40M-Bit_EN** Refer to 8M-Bit_EN description. For SPI flash. a. FFB0_0000h ~ FFBF_FFFFh For FWH. a. FF70_0000h ~ FF7F_FFFFh b. FF30_0000h ~ FF3F_FFFFh 0: Disable 1: Enable	0b	0b

3	R/W	**32M-Bit_EN** Refer to 8M-Bit_EN description. For SPI flash. a. FFC0_0000h ~ FFCF_FFFFh For FWH. a. FFC0_0000h ~ FFCF_FFFFh b. FF80_0000h ~ FF8F_FFFFh 0: Disable 1: Enable	0b	0b
2	R/W	**24M-Bit_EN** Refer to 8M-Bit_EN description. For SPI flash. a. FFD0_0000h ~ FFDF_FFFFh For FWH. a. FFD0_0000h ~ FFDF_FFFFh b. FF90_0000h ~ FF9F_FFFFh 0: Disable 1: Enable	0b	0b
1	R/W	**16M-Bit_EN** Refer to 8M-Bit_EN description. For SPI flash. a. FFE0_0000h ~ FFEF_FFFFh For FWH. a. FFE0_0000h ~ FFEF_FFFFh b. FFA0_0000h ~ FFAF_FFFFh 0: Disable 1: Enable	0b	0b

0	R/W	**8M-Bit_EN** For SPI flash, when enabled, the following memory address will be responded and forwarded to the SPI bus. a. FFF0_0000h ~ FFF7_FFFFh For FWH, when enabled, the memory address will be responded and forwarded to the LPC bus. a. FFF0_0000h ~ FFF7_FFFFh b. FFB0_0000h ~ FFBF_FFFFh 0: Disable 1: Enable	0b	1b

Register 98h-99h SPI Base address

Power on value: 0000h

Recommended value: FED1h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**SPI Base address A[31:16]** These two LPC registers specified the memory address A[31:16] for SPI operational register. The memory address A[15:0] for SPI operational register starts from the offset 0020h.	0000h	FED1h

Register 9Ah SMB Control Register

Power on value: 00h

Recommended value: 0000_0011b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	Reserved	0b	0b
6	R/W	Reserved	0b	0b
5:3	R/W	**Reserved**	00b	00b

2	R/W	**SMB SMI Enable** SMI# assertion control when SMBus cycle is completion 0: Disable 1: Enable	0b	0b
1	R/W	**SMB HST Notify** The SMBus Host Controller support the Notify command control. 0: Disable 1: Enable	0b	1b
0	R/W	**SMB Host cycle Enable** When SMB_PCLK_GT_EN bit is 1, this bit is used to control if the SMBus host cycle could start. 0: Disable 1: Enable	0b	1b

Register 9Bh SMBus BASE Address Register

Power on value: 00h

Recommended value: --h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**SMBus Base Address Register A[15:8]** SMBus registers will be located at the address specified here.	00h	

Register 9Ch FWH_ID 1

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/W	**DX_9X_IDSEL[3:0]** These four bits define the IDSEL field for the following memory address range. FFD0_0000h ~ FFDF_FFFFh FF90_0000h ~ FF9F_FFFFh	0000b	0000b

3:0	R/W	**EX_AX_IDSEL[3:0]** These four bits define the IDSEL field for the following memory address range. FFE0_0000h ~ FFEF_FFFFh FFA0_0000h ~ FFAF_FFFFh	0000b	0000b

Note 1: Although 968 can support 8 FWH, 4 FWH are recommended to support due to the AC timing constraint.

Note 2: IDSEL for memory address FFF0_0000h ~ FFFF_FFFFh and FFB0_0000h ~ FFBF_FFFFh is 0h.

Register 9Dh FWH_ID 2

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/W	**7X_3X_IDSEL[3:0]** These four bits define the IDSEL field for the following memory address range. FF70_0000h ~ FF7F_FFFFh FF30_0000h ~ FF3F_FFFFh	0000b	0000b
3:0	R/W	**CX_8X_IDSEL[3:0]** These four bits define the IDSEL field for the following memory address range. FFC0_0000h ~ FFCF_FFFFh FF80_0000h ~ FF8F_FFFFh	0000b	0000b

Register 9Eh FWH_ID 3

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7:4	R/W	**5X_1X_IDSEL[3:0]** These four bits define the IDSEL field for the following memory address range. FF50_0000h ~ FF5F_FFFFh FF10_0000h ~ FF1F_FFFFh	0000b	0000b
3:0	R/W	**6X_2X_IDSEL[3:0]** These four bits define the IDSEL field for the following memory address range. FF60_0000h ~ FF6F_FFFFh FF20_0000h ~ FF2F_FFFFh	0000b	0000b

Register 9Fh FWH_ID 4

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/W	**Reserved**	0000b	0000b
3:0	R/W	**4X_0X_IDSEL[3:0]** These four bits define the IDSEL field for the following memory address range. FF40_0000h ~ FF4F_FFFFh FF00_0000h ~ FF0F_FFFFh	0000b	0000b

Register A0h External INTA,B,C,D# Routing Register

Power on value: 00h

Recommended value: - - h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**External INTA# Routing Control** 00 : External INTA# => INTAN 01 : External INTA# => INTBN 10 : External INTA# => INTCN 11 : External INTA# => INTDN	00b	-

5:4	R/W	**External INTB# Routing Control** 00 : External INTB# => INTBN 01 : External INTB# => INTCN 10 : External INTB# => INTDN 11 : External INTB# => INTAN	00b	
3:2	R/W	**External INTC# Routing Control** 00 : External INTC# => INTCN 01 : External INTC# => INTDN 10 : External INTC# => INTAN 11 : External INTC# => INTBN	00b	
1:0	R/W	**External INTD# Routing Control** 00 : External INTD# => INTDN 01 : External INTD# => INTAN 10 : External INTD# => INTBN 11 : External INTD# => INTCN	00b	

Register A1h PCI Express INTA,B,C,D# Routing Register

Power on value: 00h

Recommended value: - - h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7:6	R/W	**PCIE#1 INTA,B,C,D# Routing Control** 00 : INTA# => INTAN INTB# => INTBN INTC# => INTCN INTD# => INTDN 01 : INTA# => INTBN INTB# => INTCN INTC# => INTDN INTD# => INTAN 10 : INTA# => INTCN INTB# => INTDN INTC# => INTAN INTD# => INTBN 11 : INTA# => INTDN INTB# => INTAN INTC# => INTBN INTD# => INTCN	00b	-
5:4	R/W	**PCIE#2 INTA,B,C,D# Routing Control** 00 : INTA# => INTAN INTB# => INTBN INTC# => INTCN INTD# => INTDN 01 : INTA# => INTBN INTB# => INTCN INTC# => INTDN INTD# => INTAN 10 : INTA# => INTCN INTB# => INTDN INTC# => INTAN INTD# => INTBN 11 : INTA# => INTDN INTB# => INTAN INTC# => INTBN INTD# => INTCN	00b	
3:0	R/W	**Reserved**	0000b	

Register A2h PATA and SATA Interrupt Pin Routing Register

Power on value: 00h

Recommended value: - - h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:5	R/W	**PATA INTA# Routing Control** 000 : PATA INTA# => INTAN 001 : PATA INTA# => INTBN 010 : PATA INTA# => INTCN 011 : PATA INTA# => INTDN 100 : PATA INTA# => INTEN 101 : PATA INTA# => INTFN 110 : PATA INTA# => INTGN 111 : PATA INTA# => INTHN	000b	-
4:2	R/W	**SATA INTA# Routing Control** 000 : SATA INTA# => INTBN 001 : SATA INTA# => INTCN 010 : SATA INTA# => INTDN 011 : SATA INTA# => INTEN 100 : SATA INTA# => INTFN 101 : SATA INTA# => INTGN 110 : SATA INTA# => INTHN 111 : SATA INTA# => INTAN	000b	
1:0	R/W	**Reserved**	00b	

Register A3h Audio and GMAC Interrupt Pin Routing Register

Power on value: 00h

Recommended value: - - h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7:5	R/W	**Audio INTA# Routing Control** 000 : Audio INTA# => INTCN 001 : Audio INTA# => INTDN 010 : Audio INTA# => INTEN 011 : Audio INTA# => INTFN 100 : Audio INTA# => INTGN 101 : Audio INTA# => INTHN 110 : Audio INTA# => INTAN 111 : Audio INTA# => INTBN	000b	-
4:2	R/W	**GMAC INTA# Routing Control** 000 : GMAC INTA# => INTDN 001 : GMAC INTA# => INTEN 010 : GMAC INTA# => INTFN 011 : GMAC INTA# => INTGN 100 : GMAC INTA# => INTHN 101 : GMAC INTA# => INTAN 110 : GMAC INTA# => INTBN 111 : GMAC INTA# => INTCN	000b	
1:0	R/W	**Reserved**	00b	

Register C0h Link & Queue Control Register 1

Power on Value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	ASL BIST Out	0b	0b
6	R/W	**ASL BIST Enable** 0 : Disable 1 : Enable	0b	0b
5	R/W	MuTIOL specidleen	0b	0b
4	R/W	SB ASL Grant Hold	0b	0b
3	R/W	SMI Mask Inactive Select	0b	0b
2	R/W	dynamic compensation function control 0:disable 1:enable	0b	0b

1:0	R/W	**Reserved.**		

Register C1h Link & Queue Control Register 2

Power on Value: 00h

Recommended value: C0h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**PSL Transaction Weight Promotion** This two bits are used to adjust PSL transaction weight at arbitration phase 00 : 1x 01 : 2x 10 : 4x 11 : 8x	00b	11b
5	R/W	**Disable Dual Address transaction** This bit is used to disable the dual address transaction, i.e., no over 4G addressing mode. 0 : greater then 4G memory addressing 1 : less than 4G memory addressing	0b	0b
4	R/W	**4QW Data Length limitation** This bit is used to limit the maximal data length. 0 : 8QW (with PCI-E NB) 1 : 4QW (with AGP NB)	0b	-
3	R/W	**Reserved.**		
2	R/W	**Master release order** Whether care transaction ordering or not 0: keep ordering 1: release ordering	0b	0b
1:0	R/W	**Threshold of Flow Control for Downstream IO Stream** This field is used as the threshold parameter of flow control for Downstream IO streams 00: Immediately 01: Fast 10: Normal 11: Slow	00b	00b

Register C3h~C2h Top Bound Control Register

Power on value : 0000h

Recommended value : ----_----_----_-000h(K8 bit0=1)

Access: Read/Write

Bit	Access	Description
15:3	R/W	Top Bound Address[35:23]
2	R/W	**Reserved.**
1	R/W	**Reserved.**
0	R/W	No Top Bound Limit

Register C5h~C4h Allocation of PCI-Hole Area I

Power on value : 0000h

Recommended value : ----h

Access: Read/Write

Bit	Access	Description
15:13	R/W	**Size of PCI-Hole Area I (within 512 Mbytes)** Bits[15:13] Size 000 64KB 001 128KB 010 256KB 011 512KB 100 1MB 101 2MB 110 4MB 111 8MB
12:0	R/W	**Base Address of PCI-Hole Area I** This field specifies A[28:16] for the base address of the PCI-Hole area.

Register C7h~C6h Allocation of PCI-Hole Area II

Power on value : 0000h

Recommended value : ----h

Access: Read/Write

Bit	Access	Description

15:13	R/W	**Size of PCI-Hole Area II (within 512 Mbytes)** Bits[15:13] Size 000 64KB 001 128KB 010 256KB 011 512KB 100 1MB 101 2MB 110 4MB 111 8MB
12:0	R/W	**Base Address of PCI-Hole Area II** This field specifies A[28:16] for the base address of the PCI-Hole area.

Register C9h~C8h Shadow RAM Read Attribute Control

Power on value : 0000h

Recommended value : ----h

Access: Read/Write

Bit	Access	Description
15	R/W	**Shadow RAM Enable for PCI Master Access** When this bit is enabled, accesses from PCI masters toward shadow RAM area is allowed. 0: Disable 1: Enable
14:13	R/W	**Reserved**
12	R/W	**Read Accessibility of Shadow Region F0000h~FFFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
11	R/W	**Read Accessibility of Shadow Region EC000h~EFFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.

10	R/W	**Read Accessibility of Shadow Region E8000h~EBFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
9	R/W	**Read Accessibility of Shadow Region E4000h~E7FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
8	R/W	**Read Accessibility of Shadow Region E0000h~E3FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
7	R/W	**Read Accessibility of Shadow Region DC000h~DFFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
6	R/W	**Read Accessibility of Shadow Region D8000h~DBFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
5	R/W	**Read Accessibility of Shadow Region D4000h~D7FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
4	R/W	**Read Accessibility of Shadow Region D0000h~D3FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.

3	R/W	**Read Accessibility of Shadow Region CC000h~CFFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
2	R/W	**Read Accessibility of Shadow Region C8000h~CBFFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
1	R/W	**Read Accessibility of Shadow Region C4000h~C7FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.
0	R/W	**Read Accessibility of Shadow Region C0000h~C3FFFh** When this bit is set to 1, the data of the read accesses toward the corresponding region are returned from system memory. When this bit is set to 0, the data are returned from PCI bus.

Register CBh~CAh Shadow RAM Write Attribute Control

Power on value : 0000h

Recommended value : ----h

Access: Read/Write

Bit	Access	Description
15	R/W	**PCI-Hole Area II Enable** 0: Disable 1: Enable
14	R/W	**PCI-Hole Area I Enable** 0: Disable 1: Enable
13	R/W	**Monochrome Device Adapter(MDA) Existence Control** 0 : Non-existence (power-on) 1 : Existence

12	R/W	**Write Accessibility of Shadow Region F0000h~FFFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
11	R/W	**Write Accessibility of Shadow Region EC000h~EFFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
10	R/W	**Write Accessibility of Shadow Region E8000h~EBFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
9	R/W	**Write Accessibility of Shadow Region E4000h~E7FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
8	R/W	**Write Accessibility of Shadow Region E0000h~E3FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
7	R/W	**Write Accessibility of Shadow Region DC000h~DFFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
6	R/W	**Write Accessibility of Shadow Region D8000h~DBFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.

5	R/W	**Write Accessibility of Shadow Region D4000h~D7FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
4	R/W	**Write Accessibility of Shadow Region D0000h~D3FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
3	R/W	**Write Accessibility of Shadow Region CC000h~CFFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
2	R/W	**Write Accessibility of Shadow Region C8000h~CBFFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
1	R/W	**Write Accessibility of Shadow Region C4000h~C7FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.
0	R/W	**Write Accessibility of Shadow Region C0000h~C3FFFh** When this bit is set to 1, the data of the write accesses toward the corresponding region are forwarded to system memory. When this bit is set to 0, the data are forwarded from PCI bus.

Register CCh SB MuTIOL™ Interface Control 1

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	R/W	**Compensation Offset for MuTIOL™ ZAD P-MOS** This register provides 4-bit offset adjustment for ZAD P-MOS compensation.

3:0	R/W	**Compensation Offset for MuTIOL™ ZAD N-MOS** This register provides 4-bit offset adjustment for ZAD N-MOS compensation.

Register CDh SB MuTIOL™ Interface Control 2

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	R/W	**Compensation Offset for MuTIOL™ ZSTB P-MOS** This register provides 4-bit offset adjustment for ZSTB P-MOS compensation.
3:0	R/W	**Compensation Offset for MuTIOL™ ZSTB N-MOS** This register provides 4-bit offset adjustment for ZSTB N-MOS compensation.

Register CEh SB MuTIOL™ Interface Control 3

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:4	R/W	**Reserved.**
3	R/W	**MuTIOL™ I/O automatic compensation timer update mode** If this bit is set to 1 , the automatic compensation timer is enabled and the compensation value is updated only when the time is expired. Otherwise it is updated every time when the compensation value is calculated. 0: disable 1: enable
2	R/W	**MuTIOL™ I/O runtime compensation enable** If this bit is set to 1 , the automatic compensation is enabled during runtime. Otherwise it is enabled only before CPU reset de-asserted. 0: disable 1: enable
1	R/W	**MuTIOL™ I/O automatic compensation fast mode** If this bit is set to 1, the compensation value will be updated to I/O buffer any time. Otherwise, the value will be updated only when I/O buffer is idle. 0: normal mode 1: fast mode

0	R/W	**MuTIOL™ I/O compensation offset value mode** If this bit is set to 1, the compensation offset will be applied to the current compensation value. Otherwise the offset value will be ignored 0: disable 1: enable

Register CFh Link & Queue Control

Power on value : 00h

Recommended value : 45h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:5	R/W	**Top Bound SMRAM Size:** 000: 128K 001: 256K 010: 512K 011: 1M 100: 2M 101: 4M 110: 8M 111: 16M	000b	010b
4	R/W	**Top Bound SMRAM Control** 0: Disable (power on) 1: Enable	0b	0b
3	RO	**Reserved**	0b	0b
2	R/W	**SMNPQ isochronous pending enable**	0b	1b
1	R/W	**EDPCI Isochronous Request Disable** 0: enable 1: disable	0b	0b
0	R/W	**PSL Isochronous Enable** This bit is used to adjust the priority of PSL channel. 0 : normal 1 : isochronous	0b	1b

Register D0h MuTIOL (Multi-threaded IO Link) Control 2

Power on value : 00h

Recommended value : 02h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:2	R/W	**Reserved**	0	0

1	R/W	**Fully Blocked Control of Upstream Cycles for Non-Deferrable Cycle** When this bit is enabled, if a non-deferrable cycle is running in host bridge, all upstream cycles will be locked. 0 : Disable 1 : Enable	0b	1b
0	R/W	**MuTIOL&EDB Write Partition Boundary Select** 0: with 4QW 1: with 8QW	0b	0b

Register D1~D3h Reserved

Power on value : 00h

Recommended value : 00h

Access: Read/Write

Register D4h MuTIOL™-to-PCI Non-Post Cycle Retry Behavior Control

Default Value: 00h

Power on value : 00h

Recommended value : 44h

Access: Read/Write

Bit	Access	Description
7:4	R/W	**MuTIOL™-to-PCI Back-End Retry Counter** These bits control the retry times when MuTIOL™-to-PCI non-posted cycles retried on PCI bus 0000 : 1 time 0001 : 2 times
3:0	R/W	**MuTIOL™-to-PCI Frond-End Retry Counter** These bits controls the retry times when MuTIOL™-to-PCI non-posted cycles retried on PCI Bus . 0000 : 1 time 0001 : 2 times

Register D5h PCI Master Characteristics Option 1

Default Value: 00h

Power on value : 00h

Recommended value : 0110000-b

Access: Read/Write

Bit	Access	Description
7	R/W	**Burst Control** This bit controls whether or not the pseudo MuTIOL™ -to-PCI bridge generates burst cycles on PCI bus 0: Enable 1: Disable
6	R/W	**Post Write Combine Control** This bit controls whether or not the pseudo MuTIOL™ -to-PCI bridge combines posted memory write cycles that issue to PCI interface. 0: Enable 1: Disable
5	R/W	**Configuration-to-Special Cycle Conversion Control** This bit controls whether or not the pseudo MuTIOL™ -to-PCI bridge supports configuration-to-special cycle conversion. 0: Enable 1: Disable
4	R/W	**Target-Abort Behavior Control** This bit controls whether or not the pseudo MuTIOL™ -to-PCI bridge wants to try again when the PCI master cycle is replied with target-abort 0: Terminate immediately 1: Try one more time
3	R/W	**Filter out the dummy MuTIOL™-to-PCI cycles** This bit controls whether or not to filter out the dummy data transfer on PCI bus 0: Enable 1: Disable
2	R/W	**Retry always for deferrable cycles** This bit controls whether or not the pseudo MuTIOL™ -to-PCI bridge always repeat to issue cycle on PCI bus when the deferrable cycle is retried by one PCI target agent 0: Enable 1: Disable
1	R/W	**Retry right now control for non-deferable cycles** This bit controls whether or not the pseudo MuTIOL™ -to-PCI bridge issues retry status to Host bus right now when the non-deferable cycle is retried on PCI bus. 0: Enable 1: Disable
0	R/W	**PCI Express extended register enable** 0: Disable (for AGP NB) 1: Enable (for PCI-E NB)

Register D6h PCI Master Characteristics Option 2

Default Value: 00h

Power on value : 00h

Recommended value : 30h

Access: Read/Write

Bit	Access	Description
7	R/W	**Reserved**
6	R/W	**Hide configuration cycle with extensive bits.** **0: hide** **1: no hide (with PCIe)**
5	R/W	**MuTIOL™ to PCI Access Latency Control** 0: Normal 1: Fast
4	R/W	**MuTIOL™ to PCI Performance Control for Back-to-Back Transaction** 0: Normal 1: Fast
3	R/W	**Reserved.**
2	R/W	**Configuration cycle decode** 0:med 1:slow
1	R/W	**Reflection control of Host bridge/Virtual PCI-to-AGP bridge Configuration cycle** This bit will control whether or not reflect the configuration cycle of Host bridge/Virtual PCI-to-AGP bridge on PCI bus 0: Disable 1: Enable
0	R/W	**Backward Compatibility Control for emulation purpose** 0: disable 1: enable

Register D7h PCI Arbiter Characteristics Option

Power on value : 00h

Recommended value : 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	PCI IO Driving Strength Control	00b	00b

5	R/W	**Decide to judge Isochronous cycle**. 0: enable. 1: diable	0b	0b
4	R/W	**PCI Arbiter CLKRUN# Enable** This bit is used to enable CLKRUN function in PCI Arbiter. 0: disable 1: enable	0b	0b
3	R/W	**PCI Grant Parking Control** This bit will control which agent is the ownership of PCI bus parked on 0: Park on MuTIOL™ -to-PCI bridge 1: Park on the latest PCI Master agent	0b	0b
2	R/W	**PCI Arbiter changes grant when PCI bus idle** 0: disable 1: enable	0b	0b
1	R/W	**PCI Arbiter last grant asserted till PCI bus idle if no other request asserted** 0: disable 1: enable	0b	0b
0	R/W	**PCI Arbiter Disable Control** 0: enable 1: disable	0b	0b

Register D8h PCI Slave Characteristics 1

Power on value : 00h

Recommended value : 45h

Access: Read/Write

Bit	Access	Description
7:4	R/W	**Threshold Control of the space-reservation mechanism for Memory Write Maximum Completion Time Limit** 0/…/8/…/15 : smallest/…/normal/…/largest
3	R/W	**Test Mode of the space-reservation mechanism for Memory Write Maximum Completion Time Limit** Note this bit should be disabled under normal mode. 0: Disable 1: Enable
2	R/W	**Abort Disconnected Delayed Transaction** This bit controls whether or not to abort the pending delayed transaction while cycle disconnection occurs. 0: Disable 1: Enable

1	R/W	**Fully command decoding for the repeated transaction recognition of delayed transaction** This bit controls whether or not to fully command decoding for repeated transaction recognition of delayed transaction 0 : Disable 1 : Enable
0	R/W	**Prefetch function Enable** This bit controls whether or not to prefetch data successively for Read transaction. 0 : Disable 1 : Enable

Register DAh~D9h PCI Slave Characteristics 2

Power on value : 0000h

Recommended value : 0400h

Access: Read/Write

Bit	Access	Description
15:0	R/W	**Discard Timer for PCI Delay transaction** Prefetched data for delayed transaction will be discarded after this timer expiration. Unit: PCI clock

Register DBh PCI Slave Characteristics 3

Power on value : 00h

Recommended value : 0110_0001

Access: Read/Write

Bit	Access	Description
7	R/W	**Reserved**
6	R/W	**PSL Hit DRAM sel (decode PMR33 cyc or not)** 0:Yes 1:NO
5	R/W	**P4 host bus interrupt delivery** 0 : Disable 1 : Enable
4:1	R/W	**Reserved**
0	R/W	**Write Promotion enable** This bit controls whether or not to promote access priority of write cycles that initiated by PCI master agents and targeted at system memory 0 : Disable 1 : Enable

Register DFh~DCh PCI Arbiter Priority Level Control

Power on value : 00000000h

Recommended value : AAAAAAAAh

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
31:30	R/W	Reserved.	00b	10b
29:28	R/W	**External PCI Request 5 Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
27:26	R/W	**External PCI Request 4 Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
25:24	R/W	**External PCI Request 3 Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
23:22	R/W	**External PCI Request 2 Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
21:20	R/W	**External PCI Request 1 Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
19:18	R/W	**External PCI Request 0 Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
17:16	R/W	**LPC PCI Request Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
15:14	R/W	Reserved.	00b	10b
13:12	R/W	Reserved.	00b	10b
11:10	R/W	**USB 2.0 PCI Request Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
9:8	R/W	**USB 1.1 PCI Request Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
7:6	R/W	**Audio/Modem PCI Request Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b

5:4	R/W	**MAC PCI Request Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
3:2	R/W	**IDE PCI Request Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b
1:0	R/W	**MuTIOL-to-PCI Bridge PCI Request Priority Level Control** 00: highest 01: middle 10: normal 11: lowest	00b	10b

Register EC~EEh Gating Clock Function

Power on value : 0d

Recommended value : 0000_0011_0000_0001_0000_1100b

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
23:18	R/W	Reserved	000000b	000000b
17	R/W	**Gating function of PCI CLK133 root** 1: enable 0: disable	0b	1b
16	R/W	**Gating function of PCI CLK33 root** 1: enable 0: disable	0b	1b
15:11	R/W	Reserved	0000b	00000b
10:9	R/W	**PMR CLK33 pre-stop counter select** 00-4T 01-8T 10-16T 11-32T	00b	00b
8	R/W	**Gating function of PMR CLK33 domain** 1: enable 0: disable	0b	1b
7:6	R/W	**PSLSMQ CLK133 pre-stop counter select** 00-8T 01-16T 10-32T 11-64T	00b	00b
5:4	R/W	**PSLSMQ CLK33 pre-stop counter select** 00-4T 01-8T 10-16T 11-32T	00b	00b
3	R/W	**Gating function of PSLSMQ CLK133 domain** 0: enable 1: disable	0b	1b
2	R/W	**Gating function of PSLSMQ CLK33 domain** 1: enable 0: disable	0b	1b

1	R/W	**Advance gating function of PSLSMQ CLK133 domain** 1: enable 0: disable	0b	0b
0	R/W	**Advance gating function of PSLSMQ CLK33 domain** 1: enable 0: disable	0b	0b

Register F6h ASL EDC function Register

Power on value : 0d

Recommended value : 92H

Bit	Access	Description	Power On Value	Recom. Setting
4:2	R/W	**device wake up latency**	0d	4h
1	R/W	**check device clk ready**	0d	1b

Register FBh ASL EDC function Register

Power on value : 0d

Recommended value : 08H

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
3	R/W	**Support TPM for P4 platform** **0: disable (K8 platform)** **1: enable (P4 platform)**	0d	1/ 0d

2.3. Legacy ISA Registers

2.3.1. DMA Registers

Address	Access	Register Name
0000h	R/W	DMA1 CH0 Base and Current Address Register
0001h	R/W	DMA1 CH0 Base and Current Count Register
0002h	R/W	DMA1 CH1 Base and Current Address Register
0003h	R/W	DMA1 CH1 Base and Current Count Register
0004h	R/W	DMA1 CH2 Base and Current Address Register
0005h	R/W	DMA1 CH2 Base and Current Count Register
0006h	R/W	DMA1 CH3 Base and Current Address Register
0007h	R/W	DMA1 CH3 Base and Current Count Register
0008h	R/W	DMA1 Status(r) Command(w) Register
0009h	R/W	DMA1 Request Register
000Ah	R/W	DMA1 Command(r) Write Single Mask Bit (w) Register
000Bh	R/W	DMA1 Mode DMA Register
000Ch	WO	DMA1 Clear Byte Pointer
000Dh	WO	DMA1 Master Clear
000Eh	WO	DMA1 Clear Mask Register
000Fh	R/W	DMA1 Write All Mask Bits(w) Mask Status(r) Register
00C0h	R/W	DMA2 CH0 Base and Current Address Register
00C2h	R/W	DMA2 CH0 Base and Current Count Register
00C4h	R/W	DMA2 CH1 Base and Current Address Register
00C6h	R/W	DMA2 CH1 Base and Current Count Register
00C8h	R/W	DMA2 CH2 Base and Current Address Register
00CAh	R/W	DMA2 CH2 Base and Current Count Register
00CCh	R/W	DMA2 CH3 Base and Current Address Register
00CEh	R/W	DMA2 CH3 Base and Current Count Register
00D0h	R/W	DMA2 Status(r) Command(w) Register
00D2h	R/W	DMA2 Request Register
00D4h	R/W	DMA2 Command(r) Write Single Mask Bit(w) Register
00D6h	R/W	DMA2 Mode Register
00D8h	WO	DMA2 Clear Byte Pointer
00DAh	WO	DMA2 Master Clear
00DCh	WO	DMA2 Clear Mask Register

00DEh	R/W	DMA2 Write All Mask Bits(w) Mask Status Register(r)

Address	Access	Register Name
0080h	R/W	Reserved
0081h	R/W	DMA Channel 2 Low Page Register
0082h	R/W	DMA Channel 3 Low Page Register
0083h	R/W	DMA Channel 1 Low Page Register
0084h	R/W	Reserved
0085h	R/W	Reserved
0086h	R/W	Reserved
0087h	R/W	DMA Channel 0 Low Page Register
0088h	R/W	Reserved
0089h	R/W	DMA Channel 6 Low Page Register
008Ah	R/W	DMA Channel 7 Low Page Register
008Bh	R/W	DMA Channel 5 Low Page Register
008Ch	R/W	Reserved
008Dh	R/W	Reserved
008Eh	R/W	Reserved
008Fh	R/W	Reserved

Address	Access	Register Name
00480h	R/W	Reserved
00481h	R/W	DMA Channel 2 High Page Register
00482h	R/W	DMA Channel 3 High Page Register
00483h	R/W	DMA Channel 1 High Page Register
00484h	R/W	Reserved
00485h	R/W	Reserved
00486h	R/W	Reserved
00487h	R/W	DMA Channel 0 High Page Register
00488h	R/W	Reserved
00489h	R/W	DMA Channel 6 High Page Register
0048Ah	R/W	DMA Channel 7 High Page Register
0048Bh	R/W	DMA Channel 5 High Page Register
0048Ch	R/W	Reserved
0048Dh	R/W	Reserved
0048Eh	R/W	Reserved

0048Fh	R/W	Reserved

2.3.2. Interrupt Controller Registers

Address	Access	Register Name
0020h	R/W	INT 1 Base Address Register
0021h	R/W	INT 1 Mask Register
00A0h	R/W	INT 2 Base Address Register
00A1h	R/W	INT 2 Mask Register

2.3.3. Timer Registers

Address	Access	Register Name
0040h	R/W	Interval Timer 1 - Counter 0
0041h	R/W	Interval Timer 1 - Counter 1
0042h	R/W	Interval Timer 1 - Counter 2
0043h	WO	Interval Timer 1 - Control Word Register

2.3.4. Other Registers

Address	Access	Register Name
0061h	R/W	NMI Status Register
0070h	WO	CMOS RAM Address and NMI Mask Register
00F0h	WO	Coprocessor Error Register
04D0h	R/W	IRQ Edge/Level Control Register 1
04D1h	R/W	IRQ Edge/Level Control Register 2

2.4. Register Summary / Description – ACPI Summary

2.4.1. SiS968 GPIOx Multi-functions & Register Setting

Pin Name	Selected	Pin Type	Register Setting
GPIO0 (MAIN)	GPI0	I	APC1[7]=0, ACPI68[0]=1
	GPO0	O	APC1[7]=0, ACPI68[0]=0
	HTC_ACTMSG	I	When ACPIB7E[0]=1 and ACPIB8[1]=1, the GPE1[0]_STS HCT_ACTMSG or HCT_STPMSG. The HCT_ACTMSG and HCT_STPMSG are internal signals for AMD K8 processor Hardware Thermal control command.
	HTC_STPMSG		
GPIO1 (MAIN)	GPI1	I	APC1[6]=0,ACPI68[1]=1, ACPI7A[5]=1
	GPO1	O	APC1[6]=0,ACPI68[1]=0
	LDRQ1#	I	APC1[6]=1
	PCIE1_HOTPLUG	I	APC1[6]=0,ACPI68[1]=1, ACPI7A[5]=1, ACPIB7[0]=0 When the above setting are met, the interal PCIE1_HOTPLUG and PCIE2_HOTPLUG signals will set the GPE1[1]_STS and GPIO1 could be set to GPO1.
	PCIE2_HOTPLUG		
	REQ4#	I	APC1[6]=0,ACPI68[1]=1, ACPI7A[5]=0, ACPIB7[0]=1
GPIO2 (MAIN)	GPI2	I	APC1[5]=0,ACPI68[2]=1
	GPO2	O	APC1[5]=0,ACPI68[2]=0
	THERM#	I	APC1[5]=1
GPIO3 (MAIN)	GPI3	I	APC1[4]=0,ACPI68[3]=1
	GPO3	O	APC1[4]=0,ACPI68[3]=0
	EXTSMI#	I	APC1[4]=1
GPIO4 (MAIN)	GPI4	I	APC1[3]=1,ACPI68[4]=1
	GPO4	O	APC1[3]=1,ACPI68[4]=0
	CLKRUN#	I/O	APC1[3]=0,ACPI19[7]=1
GPIO5 (MAIN)	GPI5	I	APC1[2]=0,ACPI68[5]=1, ACPIB7[1]=1
	GPO5	O	APC1[2]=0,ACPI68[5]=0
	REQ5#	I	APC1[2]=1
	PCIE1_PME	I	APC1[2]=0,ACPI68[5]=1, ACPIB7[1]=0 When the above setting are met, the GPE1[5]_STS could be set by the internal PCIE1_PME and PCIE2_PME signals and GPIO5 could be set to GPO5.
	PCIE2_PME		
GPIO6	GPI6	I	APC1[2]=0,ACPI68[6]=1

(MAIN)	GPO6	O	APC1[2]=0,ACPI68[6]=0
	GNT5#	O	APC1[2]=1
GPIO7 (AUX)	GPI7	I	APC3[7]=0, APC3[6]=0, APC2[7]=0,ACPI68[7]=1
	GPO7	O	APC3[7]=0, APC3[6]=0, APC2[7]=0,ACPI68[7]=0
	GPWAK#	I	APC3[7]=0,APC3[6]=0, APC2[7]=1,APC7[5]=1, ACPI68[7]=1, APC5[3]=1
	RTC32KHZ	O	APC3[7]=0, APC3[6]=0, APC2[7]=1,APC7[5]=0, ACPI68[7]=0
GPIO8 (AUX)	GPI8	I	APC3[7]=0, APC3[6]=0, APC2[6]=0,ACPI69[0]=1
	GPO8	O	APC3[7]=0, APC3[6]=0, APC2[6]=0,ACPI69[0]=0
	RING	I	APC3[7]=0, APC3[6]=0, APC2[6]=1
GPIO9 (AUX)	GPI9	I	APC3[7]=0, APC3[6]=0, APC2[5]=0,ACPI69[1]=1
	GPO9	O	APC3[7]=0, APC3[6]=0, APC2[5]=0,ACPI69[1]=0
	HDA_SDIN2	I	APC3[7]=0, APC3[6]=0, APC2[5]=1
GPIO10 (AUX)	SLP_S5#	O	APC3[7]=0, APC3[6]=0, APC2[4]=0,APC8[6]=0, APC8[7]=0, ACPI7F[1]=0 The GPIO10 is default dedicated for SLP_S5#. Can't be set to other function.
GPIO11 (AUX)	GPI11	I	APC3[7]=0, APC3[6]=0, APC2[3]=0,ACPI69[3]=1, APC7[1]=0, APC8[4]=0
	GPO11	O	APC3[7]=0, APC3[6]=0, APC2[3]=0,ACPI69[3]=0, APC7[1]=0, APC8[4]=0
	STP_PCI#	O	APC3[7]=0, APC3[6]=0, APC2[3]=0,APC7[1]=0, APC8[4]=1, ACPI1A[3]=1
	AGPSTOP#	OD	APC3[7]=0, APC3[6]=0, APC2[3]=1
GPIO12 (AUX)	GPI12	I	APC3[7]=0, APC3[3]=0, APC2[2]=0,ACPI69[4]=1
	GPO12	O	APC3[7]=0, APC3[3]=0, APC2[2]=0,ACPI69[4]=0
	CPUSTP#	OD	APC3[3]=1
GPIO13 (AUX)	GPI13	I	APC3[7]=0, APC3[6]=0, APC2[1]=0,APC7[7]=0, ACPI69[5]=1
	GPO13	O	APC3[7]=0, APC3[6]=0, APC2[1]=0, APC7[7]=0, ACPI69[5]=0
	DPRSLPVR	O	APC3[7]=0, APC3[6]=0, APC2[1]=0, APC7[7]=1, ACPI69[5]=0
GPIO14 (AUX)	GPI14	I	APC3[7]=0,APC3[6]=0,APC2[0]=1,APC10[7]=0, ACPI69[6]=1
	GPO14	O	APC3[7]=0,APC3[6]=0,APC2[0]=1,APC10[7]=0, ACPI69[6]=0
	S3AUXSW#	OD	APC10[7]=0,APC3[7]=0,APC2 [0]=0

	AGPSTOP#	OD	APC10[7]=1
GPIO15 (AUX)	SLP_S3#	O	APC3[0]=0, APC3[5]=0, ACPI69[7]=0 The GPIO15 is default dedicated for SLP_S3# function.
GPIO16 (AUX)	GPI16	I	APC3[0]=0, APC3[5]=0, APC4[5]=0,ACPI6A[0]=1
	GPO16	O	APC3[0]=0, APC3[5]=0, APC4[5]=0,ACPI6A[0]=0
	DPRSTP#	OD	APC3[5]=1
GPIO17 (AUX)	GPI17	I	APC3[0]=0, APC3[5]=0, APC4[6]=0,ACPI6A[1]=1
	GPO17	O	APC3[0]=0, APC3[5]=0, APC4[6]=0,ACPI6A[1]=0
	GA20#	I	APC3[0]=0, APC3[5]=0, APC4[6]=0,ACPI6A[1]=1, APC1[0]=0
GPIO18 (AUX)	GPI18	I	APC3[0]=0, APC3[5]=0, APC4[7]=0,ACPI6A[2]=1
	GPO18	O	APC3[0]=0, APC3[5]=0, APC4[7]=0,ACPI6A[2]=0
	KBDRST#	I	APC3[0]=0, APC3[5]=0, APC4[7]=0,ACPI6A[2]=1, APC1[1]=0
	RTC32KHZ	O	APC3[5]=1, APC7[2]=1
GPIO21 (AUX)	GPI8	I	This pin can be used as input pin to set GPE1[8]_STS, When GPIO8 is programmed to output mode and ACPI7E[3]=1
	EESK	O	ACPI7E[3]=0
GPIO22 (AUX)	GPI11	I	This pin can be used as input pin to set GPE1[11]_STS, When GPIO11 is programmed to output mode and ACPI7E[4]=1
	EEDI	O	ACPI7E[4]=0
GPIO23 (AUX)	GPI12	I	This pin can be used as input pin to set GPE1[12]_STS, When GPIO12 is programmed to output mode and ACPI7E[5]=1
	EEDO	I	ACPI7E[5]=0
GPIO24 (AUX)	GPI15	I	This pin can be used as input pin to set GPE1[15]_STS, When GPIO15 is programmed to output mode and ACPI7E[6]=1
	EECS	O	ACPI7E[6]=0
OC8 (AUX)	GPI6	I	This pin can be used as input pin to set GPE1[6]_STS, When GPIO6 is programmed to output mode and ACPI7E[1]=0
	OCI8	I	This pin can be used as input pin to set GPE1[6]_STS, When GPIO6 is programmed to output mode and ACPI7E[1]=1, ACPIB7[5]=0
CBLIDA (MAIN)	GPI0	I	This pin can be used as input pin to set GPE1[0]_STS, When GPIO0 is programmed to output mode and ACPI7E[0]=0
	IDEA_CBLID	I	ACPI7E[0]=1

To let the GPIO MUX function is correctly selected, the above setting must be followed and all APC register reserved bit must be set to 0.

2.4.2. ACPI Registers Summary

Offset	Byte Length	Access	Name	Power
00	2	R/WC	Power Management 1 Status	MAIN
02	2	R/W	Power Management 1 Enable	AUX
04	2	R/W	Power Management 1 Control	AUX
06	1	R/W	Mail Box 1	MAIN
07	1	RO	Reserved	MAIN
08	4	RO	Power Management Timer	MAIN
0C	4	RO	Reserved	MAIN
10	4	R/W	Processor Control	MAIN
14	1	RO	Processor LVL2	MAIN
15	1	RO	Processor LVL3	MAIN
16	1	R/W	Power Management 2 Control	MAIN
17	1	R/W	Processor LVL3 Control	MAIN
18	2	R/W	Geyserville Table	MAIN
1A	2	R/W	Fix Feature Control	MAIN
1C	2	WO	PM1 Status Write Port	MAIN
1E	1	R/W	Reserved for Internal Use	MAIN
1F	1	RO	Reserved	MAIN
20	2	R/WC	General Purpose Event 0 Status	AUX
22	2	R/W	General Purpose Event 0 Enable	AUX
24	4	R/W	GPE0 Interrupt Routing	MAIN
28	2	R/W	GPE0 Trigger Mode Select	MAIN
2A	2	R/W	GPE0 Control	MAIN
2C	2	WO	GPE0 Status Write Port	MAIN
2E	1	R/WC	GPE0 Child Status	MAIN
2F	1	R/W	GPE0 Control 2	MAIN
30	2	R/WC	General Purpose Event 1 Status	MAIN
32	2	R/W	General Purpose Event 1 Enable	MAIN
34	4	R/W	GPE1 Interrupt Routing	MAIN
38	2	R/W	GPE1 Trigger Mode Select	MAIN
3A	4	RO	Reserved	MAIN
3E	2	R/W	GPE1 Input Polarity Select	MAIN

40	2	R/WC	Legacy Event Status	MAIN
42	2	R/W	Legacy Event Enable	MAIN
44	2	R/W	Reserved	MAIN
46	2	RO	Reserved	MAIN
48	1	R/W	SMI# Command Port	MAIN
49	1	R/W	Mail Box2	MAIN
4A	1	R/W	SFTMR Initial Value	MAIN
4B	1	R/W	SFTMR Control	MAIN
4C	2	RO	Reserved	MAIN
4E	2	R/WC	LEG Child Status	MAIN
50	2	R/W	I/O Port Trap 0 Programmable Address	MAIN
52	2	R/W	I/O Port Trap 1 Programmable Address	MAIN
54	1	R/W	I/O Port Trap 0 Programmable Mask	MAIN
55	1	R/W	I/O Port Trap 1 Programmable Mask	MAIN
56	2	R/W	Legacy Event Control	MAIN
58	2	WO	LEG Status Write Port	MAIN
5A	2	R/W	IRQ/NMI Wakeup Control	MAIN
5C	2	RO	I/O Address Tracker	MAIN
5E	1	RO	I/O C/BE# Tracker	MAIN
5F	1	R/W	Reserved	MAIN
60	2	R/WC*	System Poweron Source Status	AUX
62	1	R/W	System Poweron Source Control	AUX
63	1	R/WC*	System Poweroff Source Status	AUX
64	4	R/W*	GPIOx Level	AUX
68	4	R/W*	GPIOx Input/Output Selection	AUX
6C	4	RO	32-bits Random Number	AUX
70	2	R/W	IO / CFG Trap 2 Programmable Address	MAIN
72	2	R/W	IO / CFG Trap 3 Programmable Address	MAIN
74	1	R/W	IO / CFG Trap 2 Programmable Mask	MAIN
75	1	R/W	IO / CFG Trap 3 Programmable Mask	MAIN

76	2	R/W	PM_NEW Control 0	MAIN
78	1	R/W	Reserved for Internal Use	AUX
79	2	R/W*	PM_NEW Control 1	AUX
7B	1	R/W	AUX_GPIO Output Control	AUX
7C	1	R/W	PM_NEW Control 2	AUX
7D	1	R/W	PM_NEW Control 3	AUX
7E	1	R/W	NEW GPI MUX Select	AUX
7F	1	R/W	Reserved for Internal Use	AUX
80	1	R/W*	TTH/NTH Timing Control for AMD K8	MAIN
81	1	R/W	Reserved	MAIN
82	2	R/W	Timing Control 0 for AMD K8	MAIN
84	4	R/W	System Management Action Field for AMD K8	MAIN
88	4	R/W	C3/S1/VFID Timing Control for AMD K8	MAIN
8C	4	R/W*	LDTSTOP# Command for AMD K8	MAIN
90	2	R/W	Reserved for Internal Use	MAIN
92	1	R/W	C3 Defer Control 0 Enable	MAIN
93	1	R/W	Reserved for Internal Use	MAIN
94	1	R/W	C3 Defer Control 1 Enable	MAIN
95	1	R/W	Reserved for Internal Use	MAIN
96	1	R/W	C3 Defer Control 2 Enable	MAIN
97	1	R/W	Reserved for Internal Use	MAIN
98	1	R/W	C3 Defer Control 3 Enable	MAIN
99	2	R/W	Reserved for Internal Use	MAIN
9B	2	R/W	IO / CFG Trap Child Event Enable	MAIN
9D	1	R/W	Reserved for Internal Use	MAIN
9E	1	R/W	Use for Watchdog Timer control	MAIN
9F	1	R/W	Reserved for Internal Use	MAIN
A0	4	R/W	MEM/IO/CFG 0 trap programmable address	MAIN
A4	2	R/W	MEM/IO/CFG 0 trap programmable address mask	MAIN
A6	1	R/W	MEM/IO/CFG 0 trap control	MAIN
A7	1	RO	Reserved	MAIN

A8	4	R/W	MEM/IO/CFG 1 trap programmable address	MAIN
AC	2	R/W	MEM/IO/CFG 1 trap programmable address mask	MAIN
AE	1	R/W	MEM/IO/CFG 1 trap control	MAIN
AF	1	R/W	Reserved For Internal Use	MAIN
B0	2	R/W	USB 0 IO Control	AUX
B2	2	R/W	Reserved	AUX
B4	4	R/W	PM_NEW Control 4	MAIN
B8	1	R/W	C3 POP UP/DOWN Control	MAIN
B9	2	R/W	Reserved	AUX
BB	1	R/W	Reserved	AUX
BC	2	R/W	Reserved	MAIN
BE	1	R/W	PM_NEW Control 5	MAIN
BF	1	R/W	PM_NEW Control 6	MAIN
C0	1	R/W	PM_NEW Control 7	MAIN
C1	1	R/W	Reserved	MAIN
C2	2	R/W	C3 Defer Control 4 Enable	MAIN
C4	2	R/W	PM_NEW Control 8	AUX
C6	1	R/W	Reserved	AUX
C7	1	R/W	Reserved	AUX

2.4.3. ACPI Register

The following registers located at I/O base address <Base> + the indicated offset value <Offset>. The base address is programmed in the Register PCI Configuration space.

Register 00h~01h Power Management Status Register (PM1_STS)

Power on value : 0000h

Recommended value : 0000h

Power Plane: Core bit15~8

Core bit7~0

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

Bit	Access	Description	Power On Value	Recom. Setting
15	R/WC	**Wake up Status (WAK_STS)** This bit is set when the system is in the sleeping state (S1~S5) and an enabled wake-up event occurs. Upon setting this bit, the system will translate form sleep state to S0 state.	0b	0b
14	R/WC	**PCIExpress Wake Status (PCIE_WAKE_STS)** This bit is set when PCI_EXPRESS generates a WAKE event from S1/S3/S4/S5.	0b	0b
13:12	RO	Reserved	00b	00b
11	R/WC	Ignored (Power Button Override Status)	0b	0b
10	R/WC	**RTC Status (RTC_STS)** This bit is set when the RTC generates an IRQ8# in the sleeping state (S1~S5). While both RTC_EN bit and RTC_STS bit are set, a power management event is raised.	0b	0b
9	RO	Reserved	0b	0b
8	R/WC	**Power Button Status (PWRBTN_STS)** This bit is set when the power button is pressed (the PWRBTN# signal is asserted Low). If PWRBTN_STS and PWRBTN_EN are both set under S0 state, then a SCI or SMI# is raised. If PWRBTN_STS bit is set under the sleeping state (S1~S5), a WAKE event will be generated.	0b	0b
7:6	RO	Reserved	00b	00b
5	R/WC	**Global Status (GBL_STS)** When the ACPI software attempts to gain the ownership of the Global Lock, this bit would be set by the access to the BIOS_RLS.	0b	0b
4	R/WC	**Bus Master Status (BM_STS)** This is the bus master status bit. This bit is set when a system bus master is requesting the system bus.	0b	0b
3:1	RO	Reserved	000b	000b
0	R/WC	**Power Management Timer Status (PMTMR_STS)** This bit will be set if the MSB of PM_TMR is changed from '1' to '0' or '0' to '1'. While PMTMR_STS and PMTMR_EN bit are set, a power management event (SCI or SMI#) is raised.	0b	0b

Register 02h~03h Power Management Enable Register (PM1_EN)

Power on value : 0000h

Recommended value :4521h (Windows)

Power Plane: Resume bit15~8

Core bit7~0

Bit	Access	Description	Power On Value	Recom. Setting
15	RO	Reserved	0b	0b
14	R/W	**PCIExpress Wake Enable (PCIE_WAKE_EN)** This bit is used to enable the assertion of the PCIE_WAKE_STS to generate a power management event (Wake and SCI/SMI#).	0b	0b
13:11	RO	Reserved	0b	0b
10	R/W	**RTC Enable (RTC_EN)** This bit is used to enable the assertion of the RTC_STS to generate a power management event (Wake and SCI/SMI#).	0b	1b
9	RO	Reserved	00b	00b
8	R/W	**Power Button Enable (PWRBTN_EN)** This bit is used to enable the assertion of the PWRBTN_STS bit to generate a power management event (SCI/SMI#). The system always can wake up from Sx by Power Button regardless of the value of this bit.	0b	1b
7:6	RO	Reserved	00b	00b
5	R/W	**Global Enable (GBL_EN)** When the BIOS drive releases the lock, this bit is used to enable the assertion of the GBL_STS to generate a SCI.	0b	1b
4:1	RO	Reserved	0	0
0	R/W	**Power Management Timer Enable (PMTMR_EN)** This is PMTMR enable bit. If this bit and PMTMR_STS bit are set, then a power management event is generated (SCI/SMI#).	0b	1b

Register 04h~05h Power Management Control Register (PM1_CNT)

Power on value : 0000h

Recommended value : 0001h

Power Plane: Resume bit15~8

Core bit7~0

Bit	Access	Description	Power On Value	Recom. Setting
15:14	RO	Reserved	00b	00b
13	WO	**Sleep Enable (SLP_EN)** This is a write only bit and always returns a zero when read. Setting this bit to one will cause the system to enter the sleep state defined by the SLP_TYP field.	0b	0
12:10	R/W	**Sleeping Type (SLP_TYP)** Define the power-saving mode that the system should enter when the SLP_EN bit is set to one. 000 : S0 state (Working) 001 : S1 state (STPCLK#) 010 : Reserved 011 : S3 state (Suspend To RAM) 100 : S4 state (Suspend To Disk) 101 : S5 state (Soft_Off)	0	0
9:3	RO	Reserved	0	0
2	WO	**Global Release (GBL_RLS)** This bit is used by the ACPI software to raise a SMI# to the BIOS software. Writing a one to this register will generate a BIOS event to set BIOS_STS in LEG_STS.	0b	0b
1	R/W	**Bus Master Reload Enable (BM_RLD)** If enabled, a bus master request will cause any processor in the C3 state to transition to the C0 state. 0 : Disable 1 : Enable	0b	0b
0	R/W	**SCI Enable (SCI_EN)** Selects the power management event in PM1 to be either SCI or SMI#. When this bit is set, a power management event will generate SCI. When this bit is reset, a power management event will generate SMI#.	0b	1b

Register 06h Mail Box 1 Register (MAIL_BOX1)

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description

7:0	R/W	Read/Write Free Byte

Register 07h Reserved

Register 08h~0Bh Power Management Timer Register (PM_TMR)

Power on value : Free Running

Recommended value : Free Running

Power Plane: Core

Bit	Access	Description
31:24	RO	Reserved
23:0	RO	**Power Management Timer Value** This read-only field reflects the current counting of the power management timer. The PM_TMR value will be reset when the system enter one of the sleeping state (S1~S5). Reading to this field will stop the running of PM_TMR.

Register 0Ch~0FhReserved

Register 10h~13h Processor Control Register (P_CNT)

Power on value : 0000_0000h

Recommended value : 0000_0000h

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting
31:5	RO	Reserved	0	0
4	R/W	**Throttling Function Enable** This bit enables the C0 clock throttling function.	0b	0b
3:1	R/W	**Throttling Duty Cycle Control** This 3-bit field determines the duty cycle of the STPCLK# signal when the system is in the C0 throttling mode.	000b	000b

		Bits 000 001 010 011 100 101 110 111	Performance Rate 100% 12.5% 25% 37.5% 50% 62.5% 75% 87.5%		
0	RO	Reserved		0b	0b

Register 14h Processor LVL2 Register (P_LVL2)

Power on value : 00h

Recommended value : 00h

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Enter C2 Power State Register** Reading to this register returns all zeros; writes to this register have no effect. Reads to this register will also generate a " Enter C2 power state " event.	00h	00h

Register 15h Processor LVL3 Register (P_LVL3)

Power on value : 00h

Recommended value : 00h

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Enter C3 Power State Register** Reading to this register returns all zeros; writes to this register have no effect. Reads to this register will also generate a " Enter C3 power state " event.	00h	00h

Register 16h Power Management 2 Control Register (PM2_CNT)

Power on value : 00h

Recommended value : 00h

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting
7:1	R/W	Reserved	0	0
0	R/W	**ARB_DIS** This bit is used to enable and disable the system arbiter. 0: The system arbiter can grant the bus to other bus master. 1: The system arbiter is disabled.	0b	0b

Register 17h Processor LVL3 Control Register (PLVL3_CNT)

Power on value : 00h

Recommended value : 08h(P4),00h(K8)

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting
7	RO	**Geyserville Process Fail Status** This is the geyserville status bit. This bit is set when a geyserville process is fail.	0b	0b
6	R/W	**APIC Wakeup Enable** 1: Disable 0: APIC event could wakeup the system from C2/C3.	0b	0b
5	R/W	**NMI, INIT and SMI Wakeup Enable** 1: Disable 0: These special interrupts could wake the system up from C2/C3/Throttling	0b	0b
4	R/W	**Vgate# Enable** 1: During C3 process, the accessory function for Vgate# is enabled. 0: Disable.	0b	0b

3	R/W	**CPUSLP# Enable** During C3 process, the accessory function for CPUSLP# is enabled. 1 : Enable 0 : Disable	0b	0b
2	R/W	**LOHI switching timing select** 1: 32 us before CPUSLP# asserted 0: switching with CPUSLP# asserted	0b	0b
1	R/W	**GPIOx wakeup Enable** 1: If GPIOx enable bit and its corresponding status bit are set, the system could be waked up from C3. 0: Disable	0b	0b
0	WO	**Geyserville Start Bit** Writing '1' to the bit will start the special C3 process for Geyserville 1 time.	0b	0b

Register 18h Geyserville Table

Power on value : 00h

Recommended value : 0-h

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting
7:1	R/W	Reserved	0	0
0	R/W	**LO/HI#** This field is only used for Geyserville process. It is independent of normal C3. 1: AC mode 0: Battery mode	0b	-b

Register19h Control Register

Power on value : 00h

Recommended value : 00h

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**CLKRUN# Enable** If ACPI C3 pop up/down function is enabled, this function should be disable 1: Enable 0: Disable	0b	0b
6	R/W	**Sx CPU_STOP# Enable** 1 : Enable 0 : Disable	0b	0b
5	R/W	**Sx AGPSTOP# Enable** 1: Enable 0: Disable	0b	0b
4	R/W	**Sx DCSTOP[3:0]# Control Enable** 1: Enable 0: Disable	0b	0b
3	R/W	**C3 CPU_STOP# Enable** 1: Enable 0: Disable	0b	0b
2	R/W	**C3 DPRSLPVR Enable** 1: Enable 0: Disable	0b	0b
1	R/W	**C3 AGPSTOP# Enable** 1: Enable 0: Disable	0b	0b
0	R/W	**C3 DCSTOP[3:0]# Control Enable** 1: Enable 0: Disable	0b	0b

Register 1Ah~1BhACPI Fix Feature Control Register (FIX_CNT)

Power on value : 0040h

Recommended value : 0040h for P4/K7; 4040h for K8

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting

15	R/W	**Sx CPUSLP# Enable** During Sx process, the accessory function for CPUSLP# is enabled. 0 : Disable 1 : Enable	0b	0b
14	R/W	**Sx LDTSTOP# Enable** 0 : Disable 1 : Enable (for K8)	0b	0b
13	R/W	**ACPI1BhB5** The bit is used to select DE_C3M6DX_CLK from PBLK_NEW	0b	0b
12	R/W	**S1 DPRSLPVR Enable (Mobile only)** 0 : Disable 1 : Enable	0b	0b
11	R/W	Reserved	0b	0b
10:9	R/W	**PM Timer Test Mode Enable** 0 : Disable 1 : Enable The enable bits are used for internal testing.	00b	00b
8	R/W	**ACPI Fix Feature Test Mode Enable** 0 : Disable 1 : Enable	0b	0b
7	R/W	**PM1_STS Write Port Enable (PM1PORT_EN)** If this bit is enabled, writing a one to PM1_PORT register will cause the corresponding bit in PM1_STS to be set. 0 : Disable 1 : Enable	0b	0b
6	R/W	**Power Button Override Function Enable** When this bit is zero, the power button override function will be disabled. 0 : Disable 1 : Enable	1b	1b
5	R/W	**Power Button Mirror** This bit is the mirror of the stage of Power Button.	0b	0b
4	R/W	**Power Button Trigger Mode Selection** The value in this field can select the trigger mode of power button. 0: Press Edge Mode (Falling Edge) 1: Release Edge Mode (Rising Edge)	0b	0b
3	R/W	**STP_PCIL Enable** 0 : Disable 1 : Enable	0b	0b
2	R/W	Reserved	0b	0b
1	WO	**BIOS Release (BIOS_RLS)** The ACPI software can set GBL_STS by writing a one to this field.	0b	0b
0	R/W	**ACPI1AhB0** The bit is used to select DE_C3M7A0_CLK and DE_CPUSTP_CLK from PBLK_NEW	0b	0b

Register 1Ch~1Dh PM1_STS Write Port (PM1_PORT)

Power on value : 0000h

Recommended value : 0000h

Power Plane: Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	WO	**PM1_STS Write Port** Writing a one to this register will cause the corresponding field of PM1_STS to be set. Before writing to this register, PM1PORT_EN must be set.	0000h	0000h

Register 1Eh~1Fh Reserved for Internal Use

Register 20h~21h General Purpose Event 0 Status Register (GPE0_STS)

Power on value : 0000h

Recommended value : 0000h

Power Plane: Resume (Bit0~1,15 are except)

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields. When one of status and their corresponding enable bits are set in S1, a wakeup event is generated. If the status and the corresponding rerouting bits are set during working state (S0), an SCI/SMI#/IRQ will be generated. Note that IRQWAK_STS, USB3_STS, and USB2_STS can only be set during sleeping state.

Bit	Access	Description	Power On Value	Recom. Setting
15	R/WC	**IRQ / Key Board Wake Status (IRQWAK_STS)** This bit is set when one of the enabled 8259 IRQ wakeup events is generated in S1 state. Note: The IRQ wake-up events are defined in IRQWAK_CNT register.	0b	0b
14	R/WC	**USB_ALL/ USB0 Wake Status (select bit is** APC6[6]) This bit is set when USB_ALL/USB0 detects a wake up event in sleeping state.	0b	0b
13	R/WC	Reserved	0b	0b

12	R/WC	**MAC Power Management Event Status** (MACPME_STS) This bit is set when internal MAC power management event is generated.	0b	0b
11	R/WC	**PCI Power Management Event Status** (PCIPME_STS) This bit is set when PCI power management event is asserted.	0b	0b
10	R/WC	**Thermal_Trip Status (for AMD K8)** This bit is set when the processor reaches the temperature trip points.	0b	0b
9	R/WC	**PCI Express Power Management Event Status** (PCIEPME_STS) This bit is set when PCIE power management event is asserted	0b	0b
8	R/WC	**Ring Indication Status (RING_STS)** This bit is set when the RING goes active. This bit can be chosen as quite or noise mode in GPECNT register. In quite mode, RING_STS can only be set during sleeping state (S1). In noisy mode, RING_STS can be set in working and sleeping states.	0b	0b
7	R/WC	**GPWAK# Status (GPWAK#_STS) / USB2_STS** (select bit is APC6[6]) This bit will be set when GPWAK# is asserted or USB2 detects a wake up event in sleeping state.	0b	0b
6	R/WC	Reserved	0b	0b
5	R/WC	**Audio Controller Power Management Event Status (AUDPME_STS)** This bit is set when an embedded Audio controller issues a PME interrupt..	0b	0b
4	R/WC	**Reserved / USB1 Wake Status (select bit is APC6[6])** This bit is set when USB1 detects a wake up event in sleeping states.	0b	0b
3	R/WC	**SATA Controller Power Management Event Status (SATA_PME_STS)** This bit is set when an SATA controller issues a PME# interrupt.	0b	0b
2	R/WC	**EXTSMI# Status (EXTSMI_STS)** This bit is set when EXTSMI# goes active. This bit has the relevant child status bits in 2Eh.	0b	0b

1	R/WC	**Thermal Override STS / Thermal_2 STS** Thermal Override STS: (TTL level) This bit is set when THERM# goes active for a period of time delay (controlled by 2Fh[3] ← 60ns or 2sec). The input enable bit is 2Fh[0]. If THRMOR_THT is set, the system will enter thermal throttling mode for a period of time delay (controlled by 2Fh[2] ← 2sec or immediately). **Thermal_2 STS: (GTL level)** This bit will be set when THERM2# goes active for a period of time delay (controlled by 2Fh[3] ← 60ns or 2sec). The input enable bit is 2Fh[1]. If GPE0B1_EN is set, the STS can generate a SMI#. BIOS can assert Thermal Throttling by SMI routine to protect CPU.	0b	0b
0	R/WC	**Thermal Event Status (THRM_STS)** This bit is set when THERM# goes active.	0b	0b

Register 22h~23h General Purpose Event 0 Enable Register (GPE0_EN)

Power on value : 0000h

Recommended value : A000h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
15	R/W	IRQ/Key Board Wake Enable (IRQWAK_EN)	0b	1b
14	R/W	All USB Hosts Wake Enable / USB0 Wake Enable (USBALLWAK_EN / USB0WAK_EN)	0b	0b
13	R/W	Reserved	0b	0b
12	R/W	MAC Power Management Event Enable (MACPME_EN)	0b	0b
11	R/W	PCI Power Management Event Enable (PCIPME_EN)	0b	0b
10	R/W	Thermal_Trip Enable (for AMD K8)	0b	0b
9	R/W	**PCI Express Power Management Event Enable bit** 1:Enable 0:Disable	0b	0b

8	R/W	Ring Indication Enable (RING_EN)	0b	0b
7	R/W	GPWAK# / USB2_Wake Enable (GPWAK#_EN / USB2WAK_EN)	0b	0b
6	R/W	Reserved	0b	0b
5	R/W	Audio Controller Power Management Event Enable (AUDPME_EN)	0b	0b
4	R/W	Reserved / USB1 Wake Enable (/ USB1WAK_EN)	0b	0b
3	R/W	SATA_PME# Wake Enable (SATAWAK_EN).	0b	0b
2	R/W	EXTSMI# Enable (EXTSMI_EN)	0b	0b
1	R/W	Thermal Event Override Enable / Thermal Trip Enable (THRMOR_EN / THERMTRIP_EN)	0b	0b
0	R/W	Thermal Event Enable (THRM_EN)	0b	0b

Register 24h~27h General Purpose Event 0 Interrupt Routing Register (GPE0_ROUT)

Power on value : 0000_0000h

Recommended value : AAAA_AAAAh

Power Plane : Core

The following registers are GPE0 routing registers. If one of GPE0_STS is set and its corresponding GPE0_ROUT register is routing to SCI/SMI#, an SCI/SMI# will be generated.

Bit	Access	Description	Power On Value	Recom. Setting
31:30	R/W	**IRQ Wake Route (IRQWAK_ROUT)** 00 : Reserved 01 : SMI# 10 : SCI 11 : Reserved	00b	10b
29:28	R/W	USB_ALL/USB0 Wake Route (USBALL/USB0 WAK_ROUT)	00b	10b
27:26	R/W	Reserved	00b	10b
25:24	R/W	MAC Power Management Event Route (MACPME_ROUT)	00b	10b
23:22	R/W	PCI Power Management Event Route (PCIPME_ROUT)	00b	10b

21:20	RW	Thermal_Trip Event Route (for AMD K8) (THRMTRP_ROUT)	00b	10b
19:18	R/W	PCIE Power Management Event Route (PCIEPME_ROUT)	00b	10b
17:16	R/W	Ring Indication Route (RING_ROUT)	00b	10b
15:14	R/W	GPWAK# / USB2 Wake Route (GPWAK#_ROUT/ USB2WAK_ROUT)	00b	10b
13:12	RO	Reserved	00b	10b
11:10	R/W	Embedded Audio Controller Power Management Event Route (AUDPME_ROUT)	00b	10b
9:8	R/W	Reserved / USB1 Wake Route (/ USB1WAK_ROUT)	00b	10b
7:6	R/W	SATA PME Wake Route (SATA_ROUT).	00b	10b
5:4	R/W	EXTSMI# Route (EXTSMI_ROUT)	00b	10b
3:2	R/W	Thermal Event Override Route / Thermal_2 Route (THRMOR_ROUT / THERM2_ROUT)	00b	10b
1:0	R/W	Thermal Event Route (THRM_ROUT)	00b	10b

Register 28h~29h General Purpose Event 0 Trigger Mode Selection (GPE0_TRG)

Power on value : 0000h

Recommended value : 0100h

Power Plane : Core

If GPE0 is set to level trigger mode, the GPE0_STS will always be set by the active event as long as the event is not de-asserted. If GPE0_TRG is set to be edge trigger mode, the active event can only set GPE0_STS once before the active event is de-asserted.

Bit	Access	Description	Power On Value	Recom. Setting
15	R/W	IRQ Wake Trigger (IRQWAK_TRG) 0 : Level trigger mode 1 : Edge trigger mode	0b	0b
14	R/W	USBALL/ USB0 Wake Trigger (USBALL / USB0WAK_TRG)	0b	0b
13	R/W	Reserved	0b	0b

12	R/W	MAC Power Management Event Trigger (MACPME_TRG)	0b	0b
11	R/W	PCI Power Management Event Trigger (PCIPME_TRG)	0b	0b
10	R/W	Thermal_Trip Event Trigger (for AMD K8) (THRMTRP_TRG)	0b	0b
9	R/W	PCIE Power Management Event Trigger (PCIEPME_TRG)	0b	0b
8	R/W	Ring Indication Trigger (RING_TRG)	0b	1b
7	R/W	GPWAK# / USB2 Trigger (GPWAK#_TRG/ USB2_TRG)	0b	0b
6	RO	Reserved	0b	0b
5	R/W	Embedded Audio Controller Power Management Event Trigger (AUDPME_TRG)	0b	0b
4	R/W	Reserved / USB1 Wake Trigger (/ USB1WAK_TRG)	0b	0b
3	R/W	SATA PME Wake Trigger (SATA_TRG).	0b	0b
2	R/W	EXTSMI# Trigger (EXTSMI_TRG)	0b	0b
1	R/W	Thermal Event Override Trigger / Thermal_2 Trigger (THRMOR_TRG / THERM2_TRG)	0b	0b
0	R/W	Thermal Event Trigger (THRM_TRG)	0b	0b

Register 2Ah~2BhGeneral Purpose Event Control (GPE_CNT)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On VValue	Recom. Setting
15	R/W	**EXTSMI#/SLPBTN# Switch** 0: EXTSMI# 1: SLPBTN#	0b	0b
14:8	R/W	Reserved	0	0

7	R/W	**GPE0_STS Write Port Enable (GPE0PORT_EN)** If this bit is enabled, writing a one to GPE0_PORT register will cause the corresponding bit in GPE0_STS to be set. 0 : Disable 1 : Enable	0b	0b
6	R/W	**RING Indication Quiet/Noisy Mode Control (RING_CNT)** If RING is set to be quiet mode, RING_STS can only be set in S1. If the noisy mode is selected, RING_STS can be set in both working and sleeping state. This bit is recommended set to 1. 0 : Noisy mode 1 : Quiet mode	0b	0b
5	R/W	**GPIO[20:19] Function Select** 0 : Disable 1 : Enable	0b	0b
4	R/W	**Mapping Enable** When this bit is set, all PMEs of PCI devices would assert PCIPME_STS.	0b	0b
3	R/W	**Thermal Override Throttling Function Enable (THRMOR_THT)** This bit enables the thermal override throttling function. 0 : Disable 1 : Enable	0b	0b
2:0	R/W	**Thermal Override Throttling Duty Cycle Control** This 3-bit field determines the duty cycle of the STPCLK# signal when the thermal override event is generated. **Bits** — **Performance Rate** 000 — 100% 001 — 12.5% 010 — 25% 011 — 37.5% 100 — 50% 101 — 62.5% 110 — 75% 111 — 87.5%	000b	000b

Register 2Ch~2DhGPE0_STS Write Port (GPE0_PORT)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	WO	**GPE0_STS Write Port** Writing a one to this register will cause the corresponding field of GPE0_STS to be set. Before writing to this register, GPE0PORT_EN must be set.	0h	0h

Register 2Eh GPE0 Child Status Register

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:4	RO	**Reserved**	4'h0	4'h0
3	R/WC	**SLPREQ_STS** When EXTSMI# is used as a sleep button and asserted in the running mode, this bit would be asserted.	0b	0b
2	R/WC	**WAKEREQ_STS** When EXTSMI# is used as a wake event and asserted in the sleep mode, this bit would be asserted.	0b	0b
1:0	RO	Reserved	00b	00b

Register 2Fh Reserved

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:6	RO	Reserved	4'h0	4'h0

5	R/W	**AUX_PCIE_PME set GPE0B9_STS** **0: Enable** **1: Disable**	0b	0b
4	R/W	**PCIE_PME set GPE0B9_STS** **0: Enable** **1: Disable**	0b	0b
3	R/W	**THERM2_DLY_SEL** 0: THERMTRIP# set GPE1B2_STS(to assert SMI#) immediately. 1: THERMTRIP# set GPE1B2_STS after 1~2 sec.	0b	0b
2	R/W	**Thermal Throttling delay selection** 0: Throttling actives after 2 sec delay. 1: Throttling actives immediately.	0b	0b
1	R/W	**THERM2 Input Enable (THERM2_EN)** 0: Disable 1: Enable	0b	0b
0	R/W	**THERM Input Enable (THERM_EN)** 0: Disable 1: Enable	0b	0b

Register 30h~31h General Purpose Event 1 Status Register (GPE1_STS)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields. When one of status and their corresponding enable bits are set in S1, a wakeup event is generated. If the status and the corresponding rerouting bits are set during working state (S0), an SCI/SMI#/IRQ will be generated. Not that if GPIO[n] are selected as output mode or their mux-ed function, their corresponding status bits must be ignored. So do their enable and route registers must be set to zero.

Bit	Access	Description	Power On Value	Recom. Setting
15:3	R/WC	**GPIO[15:0] Status (GPIO[15:3]_STS)** This bit is set when one of GPIO[15:0] event goes active.	13'h0	13'h0

2	R/WC	**GPIO2 Status/ Instant Power-off Status** (GPIO2_STS/INSTOFF_STS) This bit is set when GPIO2 event goes active. If LPC bridge configuration register 48h[05] is enabled, the assertion of GPIO2_STS would power the machine off compulsively.	0b	0b
1:0	R/WC	**GPIO[1:0] Status (GPIO[1:0]_STS)** This bit is set when one of GPIO[1:0] event goes active.	00b	00b

Register 32h~33h General Purpose Event 1 Enable Register (GPE1_EN)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	GPIO[15:0] Enable (GPIO[15:0]_EN)	16'h0	16'h0

Register 34h~37h General Purpose Event 1 Interrupt Routing Register (GPE1_ROUT)

Power on value : 0000_0000h

Recommended value : 0000_0000h

Power Plane : Core

The following registers are GPE1 routing registers. If one of GPE1_STS is set and its corresponding GPE1_ROUT register is routing to SCI/SMI#, an SCI/SMI# will be generated.

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**GPIO[15:0] Route (GPIO[15:0]_ROUT)** 00 : Reserved 01 : SMI# 10 : SCI 11 : Reserved	32'h0	32'h0

Register 38h~39h General Purpose Event 1 Trigger Mode Selection (GPE1_TRG)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

If GPE1 is set to level trigger mode, the GPE1_STS will always be set by the active event as long as the event is not de-asserted. If GPE1_TRG is set to be edge trigger mode, the active event can only set GPE1_STS once before the active event is de-asserted.

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**GPIO[15:0] Trigger (GPIO[15:0]_TRG)** 0 : Level trigger mode 1 : Edge trigger mode	0000h	0000h

Register 3Ah~3Dh

Power on value : 0000_0000h

Recommended value : 0000_0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
31:0	RO	**Reserved**	00000000h	00000000

Register 3Eh~3Fh General Purpose Event 1 Input Polarity Select (GPE1_POL)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**GPIO[15:0] Input Polarity Select** (GPIO[15:0]_POL) 0 : Active low 1 : Active high	0000h	0000h

Register 40h~41h Legacy Event Status Register (LEG_STS)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

Bit	Access	Description	Power On Value	Recom. Setting

15	R/WC	**Software Watch Dog Timer Event Status (SFTMR_STS)** This bit is set when the software watchdog timer expires. This status bit does not have its corresponding enable bit. To clear this status bit, its source at ACPI register 4Eh, bit1 and 0 must be cleared as well.	0b	0b
14	R/WC	**Non host initiate USBSMI STS (USBSMI_STS)** This bit is set when USBSMI asserted by a general event.	0b	0b
13	R/WC	**General Purpose Event Status (GPESMI_STS)** This bit is set when the SMI# is caused by GPE0 or GPE1. This status bit does not have its corresponding enable bit.	0b	0b
12	R/WC	**Power Management Status (PM1SMI_STS)** This bit is set when the SMI# is caused by PM1. This status bit does not have its corresponding enable bit.	0b	0b
11	R/WC	**SMB Interrupt Status** This bit is set when the SMB host controller delivers its interrupt.	0b	0b
10	R/WC (host init.)	**Host initiate USBSMI STS (HOSTUSBSMI_STS)** This bit is set when USBSMI asserted by a host initiated cycle.	0b	0b
9	R/WC	**Serial IRQ SMI# Status (SIRQSMI_STS)** This bit is set when internal Serial IRQ decoder asserts an SMI#.	0b	0b
8	R/WC	**LPC SMI# Status (LPCSMI_STS)** This bit is set when internal LPC controller asserts an SMI#.	0b	0b
7	R/WC	**One Minute Status (ONEMIN_STS)** This bit is set every one minute. In legacy power management, ONEMIN_STS and ONEMIN_EN can be used to monitor the device status every one minute.	0b	0b

6	R/WC (host init.)	**ACPI Sleep Enable Status (SLPEN_STS)** This bit is set when OS writes one to SLP_EN.	0b	0b
5	R/WC (host init.)	**SMI# Command Status (SMICMD_STS)** This bit is set when OS writes a value to SMI# command port.	0b	0b
4	R/WC (host init.)	**BIOS Status (BIOS_STS)** This bit is set when the BIOS driver write a one to GBL_RLS in PM1_CNT register.	0b	0b
3	R/WC	**SPI SMI# Status (SPISMI_STS)** This bit is set when internal SPI controller asserts an SMI#.	0b	0b
2	R/WC (host init.)	**IO/CFG Trap Status (IOCFGTRAP_STS)** This bit is set when software initiates an I/O access or CFG assess to the range of IOTRAP_PORT and IOTRAP_MASK. There are 4 sets of Trap address. The TRAP2 & TRAP3 address can be set as PCI Configuration address. The child status are at 4Eh~4Fh.	0b	0b
1	R/WC	**Geyserville Process End Status (GEYEND_STS)** This bit is set when geyserville process is finished.	0b	0b
0	R/WC	**SMI# Status (SMI_STS)** This bit is set when one of the SMI# source is activated. The SMI# will be masked for 128 PCI clock after clearing this bit.	0b	0b

Register 42h~43h Legacy Event Enable Register (LEG_EN)

Power on value : 0000h

Recommended value : 4401h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15	R/W	Reserved	0b	0b
14	R/W	Non-host Initiate USBSMI# Enable	0b	1b

13:12	R/W	Reserved	00b	00b
11	R/W	SMB_SMI# enable	0b	0b
10	R/W	Host Initiate USBSMI# Enable	0b	1b
9	R/W	Serial IRQ SMI# Enable (SIRQSMI_EN)	0b	0b
8	R/W	LPC SMI# Enable (LPCSMI_EN)	0b	0b
7	R/W	One Minute Enable (ONEMIN_EN)	0b	0b
6	R/W	ACPI Sleep_En Enable (SLPEN_EN) 1: OS can not enter to the sleep state specified by SLP_TYP[2:0] and trigger SMI# if SLPEN_STS is asserted.	0b	0b
5	R/W	SMI Command Enable (SMICMD_EN)	0b	0b
4	R/W	BIOS Enable (BIOS_EN)	0b	0b
3	R/W	SPI SMI# Enable (SPI SMI_EN)	0b	0b
2	R/W	IO / CFG Trap Enable (IO / CFG TRAP_EN)	0b	0b
1	R/W	Reserved	0b	0b
0	R/W	SMI Enable (SMI_EN)	0b	1b

Register 44h~45h Reserved

Register 46h~47h Reserved

Register 48h SMI# Command Port Register (SMICMD_PORT)

Default Value: 00h

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**SMI# Command Port Value** Writing to this register will generate an SMI# command event.	00h	00h

Register 49h Mail Box 2 Register (MAIL_BOX2)

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Read/Write Free Byte**	00h	00h

Register 4Ah Software Watchdog Timer Initial Value (SF_TMR)

Power on value : ffh

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Software Watchdog Timer Initial Value** Writing to this register will reload the software watchdog timer with the value specified in this register. If the software watchdog timer expires the first time, the expired event will set the SFTMR0_STS and the timer will reload its initial value and count again. If the timer expire the second time, the expired event will set the SFTMR1_STS. The timer value can't be read from this field.	ffh	00h

Register 4Bh Software Watchdog Timer Control Register (SFTMR_CNT)

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Software Watchdog Timer Counting Enable** The software watchdog timer will start to count when this bit is set to one.	0b	0b
6	RO	**Reserved**	0b	0b
5:4	R/W	**Software Watchdog Timer Clock Select (ACPI A6HB[3:2] must be "00")** 00 : 4ms 01 : 1sec 10 : 1min 11 : 1hour	00b	00b

3:2	R/W	**Software Watchdog Timer Expiration Event 1 Routing Select** When SFTMR1_STS is set to one, an SMI#/SFTIRQ/PCIRST# will be generated according to the following combination. 00 : Reserved 01 : SMI# 10 : Reserved 11 : PCIRST#	00b	00b
1:0	R/W	**Software Watchdog Timer Expiration Event 0 Routing Select** When SFTMR0_STS is set to one, an SMI#/SFTIRQ/PCIRST# will be generated according to the following combination. 00 : Reserved 01 : SMI# 10 : Reserved 11 : PCIRST#	00b	00b

Register 4Ch~4DhReserved

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	RO	Reserved	0000h	0000h

Register 4Eh Legacy Child Status

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/WC	**PCI Configuration Read Trap [3:2] Child Status** Any PCI Configuration reading transaction of the range of TRAP[3:2]_ADDR and TRAP[3:2]_MASK will cause these bits to be set.	00b	00b

5:4	R/WC	**PCI Configuration Write Trap [3:2] Child Status** Any PCI Configuration writing transaction of the range of TRAP[3:2]_ADDR and TRAP[3:2]_MASK will cause these bits to be set.	00b	00b
3:2	RO	Reserved	00b	00b
1	R/WC	**Software Watch Dog Timer Event 1 Status** 1: It is the second time the timer is expired.	0b	0b
0	R/WC	**Software Watch Dog Timer Event 0 Status** 1: It is the first time the timer is expired.	0b	0b

Register 4Fh Reserved

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/WC	**PCI I/O Read Trap [3:0] Child Status** Any I/O reading transaction of the range of TRAP[3:0]_ADDR and TRAP[3:0]_MASK will cause these bits to be set.	0000b	0000b
3:0	R/WC	**PCI I/O Write Trap [3:0] Child Status** Any I/O writing transaction of the range of TRAP[3:0]_ADDR and TRAP[3:0]_MASK will cause these bits to be set.	0000b	0000b

Register 50h~51h Programmable 16-bits I/O Port Trap 0 Address (IOTRAP0_ADDR)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**I/O Port Trap 0 Address** Any I/O access to the range of IOTRAP0_ADDR and IOTRAP0_MASK will cause TRAP0_STS to be set to one.	0000h	0000h

Register 52h~53h Programmable 16-bits I/O Port Trap 1 Address (IOTRAP1_ADDR)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**I/O Port Trap 1 Address** Any I/O access to the range of IOTRAP1_ADDR and IOTRAP1_MASK will cause TRAP1_STS to be set to one.	0000h	0000h

Register 54h Programmable 16-bits I/O Port Trap 0 Mask (IOTRAP0_MASK)

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**I/O Port Trap 0 Mask** A one in this register will select the low 8-bit mask for IOTRAP0_ADDR.	00h	00h

Register 55h Programmable 16-bits I/O Port Trap 1 Mask (IOTRAP1_MASK)

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**I/O Port Trap 1 Mask** A one in this register will select the low 8-bit mask for IOTRAP1_ADDR.	00h	00h

Register 56h~57h Legacy Event Control (LEG_CNT)

Power on value : 0000h

Recommended value : 0040h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:8	RO	**Reserved**	8'h0	8'h0

7	R/W	**LEG_STS Write Port Enable (LEGPORT_EN)** If this bit is enabled, writing a one to LEG_PORT register will cause the corresponding bit in LEG_STS to be set. 0 : Disable 1 : Enable	0b	0b
6	R/W	**Auto-Reset Function Enable (AUTORST_EN)** If the system auto reset hardware trap function is enabled, this bit should be set to 1 in 1 second after PCIRST# de-assertion to prevent the system auto reset.	0b	1b
5:1	R/W	**Reserved**	5'h0	5'h0
0	R/W	**SMI# Mask Interval Select** If SMI_STS is cleared, the SMI# will be masked a certain time according to this register. 0 : 128 PCICLK 1 : 8 PCICLK	0b	0b

Register 58h~59h LEG_STS Write Port (LEG_PORT)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	WO	**LEG_STS Write Port** Writing a one to this register will cause the corresponding field of LEG_STS to be set. Before writing to this register, LEGPORT_EN must be set.	0000h	0000h

Register 5Ah~5Bh IRQ and NMI Enable for Wake-up Event Control (IRQWAK_CNT)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:3	R/W	Correspond to the enable bits for IRQ[15:3] to generate a wake-up event	13'h0	13'h0

2	R/W	Correspond to the enable bits for NMI to generate a wake-up event	0b	0b
1:0	R/W	Correspond to the enable bits for IRQ[1:0] to generate a wake-up event	00b	00b

Register 5Ch~5Dh I/O Address Track for SMI# (ADDR_TRACK)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	RO	**I/O Address Track** The reading value in this register reflects the address of last I/O cycle from CPU before the system enter SMI# handler.	0000h	0000h

Register 5Eh~5FhI/O Command/Byte Enable Track for SMI# (CBE_TRACK)

Power on value : 0300h

Recommended value : 0300h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:12	RO	**Reserved**	4'h0	4'h0
11	RO	**GPIO20 Input** When Register 2A[5] is set, the level of pin GPIO20 can be read from this bit.	0b	0b
10	RO	**GPIO19 Input** When Register 2A[5] is set, the level of pin GPIO19 can be read from this bit.	0b	0b
9	R/W	**GPIO20 Output Control** When Register 2A[5] is set, the output level of pin GPIO20 is controlled by this bit. 0: Output Floating 1: Output low	1b	1b

8	R/W	**GPIO19 Output Control** When Register 2A[5] is set, the output level of pin GPIO19 is controlled by this bit. 0: Output Floating 1: Output low	1b	1b
7:0	RO	**Reserved**	8'h0	8'h0

Register 60h~61h System Wakeup form S3/S4/S5 Status Register (S5WAK_STS)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Resume

The following registers are all located in resume well. They can survive as long as the standby power exists. The only way to clear the register is to write S5WAK_CLR or de-assert AUXOK.

Bit	Access	Description	Power On Value	Recom. Setting
15	RO	**Power Button Wakeup Status (PWRBTN_S5WAK_STS)** This bit will be set if power button wakes up the system from S3/S4/S5.	0b	0b
14	RO	**RTC Wakeup Status (RTC_S5WAK_STS)** This bit will be set if a RTC IRQ8# wakes up the system from S3/S4/S5.	0b	0b
13	RO	**RING Wakeup Status (RING_S5WAK_STS)** This bit will be set if RING wakes up the system from S3/S4/S5.	0b	0b
12	RO	**MACPME Wakeup Status (MACPME_S5WAK_STS)** This bit will be set if MAC power management event wakes up the system from S3/S4/S5.	0b	0b
11	RO	**PCIPME Wakeup Status (PCIPME_S5WAK_STS)** This bit will be set if PCI power management event wakes up the system from S3/S4/S5.	0b	0b
10	RO	**AUDPME Wakeup Status (AUDPME_S5WAK_STS)** This bit will be set if AC'97 power management event wakes up the system from S3/S4/S5.	0b	0b
9	RO	**Reserved**	0b	0b

8	RO	**USB1 Wakeup Status (USBC1_S5WAK_STS)** This bit will be set if USB Controller 1 wakes the system up from S3/S4/S5.	0b	0b
7	RO	**USB0 Wakeup Status (USBC0_S5WAK_STS)** This bit will be set if USB Controller 0 wakes the system up from S3/S4/S5.	0b	0b
6	RO	**GPWAK# Wakeup Status (GPWAK#_S5WAK_STS)** This bit will be set if GPWAK# wakes up the system from S3/S4/S5.	0b	0b
5	RO	**Power Supply Resume to Previous State Status (RSM_S5WAK_STS)** This bit will be set if power supply resume function wakes up the system from S5.	0b	0b
4	RO	**Reserved**	0b	0b
3	RO	**PCIExpress Wake Status (PCIE_WAKE_STS)** This bit will be set if PCIE1 / PCIE2 Controller wake up the system up from S3/S4/S5.	0b	0b
2	RO	**Reserved**	0b	0b
1	RO	**USB2 Wakeup Status (USBC2_S5WAK_STS)** This bit will be set if USB Controller 2 wakes the system up from S3/S4/S5.	0b	0b
0	RO	**Reserved**	0b	0b

Register 62h~63h System Wakeup form S3/S4/S5 Control Register (S5WAK_CNT)

Power on value : 0000h

Recommended value : 0400h

Power Plane : Resume

The following registers are all located in resume well. They can survive as long as the standby power exists.

Bit	Access	Description	Power On Value	Recom. Setting
15	RO	**GPIOFF#_STS** This bit will be set if the system is powered off due to GPIOFF#. This bit would be cleared by S5WAK_CLR.	0b	0b

14	RO	**Instant Off status (INSTOFF_STS)** This bit will be set if the system is powered off due to the assertion of GPE1B2_STS. This bit would be cleared by S5WAK_CLR.	0b	0b
13	RO	**Power Button Override Status (BTNOROFF_STS)** A '1' in this bit indicates the system is powered off due to the PWRBTN override. This bit would be cleared by S5WAK_CLR.	0b	0b
12	RO	**S3 Off Status (S3OFF_STS)** This bit will be set when the system goes to S3 sleep state. This bit would be cleared by S5WAK_CLR.	0b	0b
11	R/W	Reserved	0b	0b
10	R/W	Timing Control of the PCIRST# and PSON# while entering S3/S4/S5 0:PCIRST# assert after PSON# assert 1:PCIRST# assert before PSON# assert	0b	1b
9:8	R/W	Reserved	0b	0b
7:6	R/W	**ACPILED Output State Control** The output state of ACPILED can be controlled by the following combination when system is in S0/S1/ S3 states. If the system is in S4/S5 state, ACPILED will be set to high impedance. 00 : Output low 01 : Blink 10 : High impedance 11 : Reserved	0b	0b
5:4	RO	**Reserved**	00b	00b
3	R/W	**Watchdog Timer Power Off Status** This bit will be set when the watchdog timer expire and system power off have been taken.	0b	0b
2	R/W	**GPE0 Status Mirror Enable (GPE0_AUX_EN)** 1: The Power On status bits in Reg. 60h~61h would map into the corresponding bits in GPE0 Register.	0b	0b
1	R/W	**PM1 Status Mirror Enable (PM1_AUX_EN)** 1: The Power On status in Reg. 60h~61h would map into the corresponding bits in PM1 Register.	0b	0b

0	R/W	**S5WAK_STS Clear Status (S5WAK_CLR)** If this register is set to one, all register in S5WAK_STS will be reset to zero. When BIOS use this bit to clear the S5WAK_STS register, it should read the S5WAK_STS register to make sure all status bit is cleared to 0. BIOS must set this bit to 1 to allow the S5WAK_STS register to record next power up event.	0b	0b

Register 64h~67h General Purpose Event 1 Pin Level (GPE1_LVL)

Power on value : 0000_0000h

Recommended value : 0000_0000h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
31:19	R/W	**Reserved**	13'h0	13'h0
18:0	R/W	GPIO[14:0] LEVEL If GPIO[18;0] is set as input mode(GPIO[18:0]_IO='1'), then the status of GPIO[18:0] could be read from these bits. If GPIO[18:0] is set as output mode(GPIO[18:0]_IO='0'), then the output level of GPIO[18:0] could be controlled by these bits.	19'h0	19'h0

Register 68h~6Bh General Purpose Event 1 Input/Output Mode Select (GPE1_IO)

Power on value : FFFF_FFFFh

Recommended value : FFFF_FFFFh

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
31:19	R/W	Reserved	1FFFh	1FFFh
18:0	R/W	**GPIO[18:0] Input/Output Mode Selection** If GPIO[18:0] are referred to GPIO, the INPUT/OUTPUT mode could be selected by these bits. 0: Output Mode 1: Input Mode	3FFFFh	3FFFFh

Register 6Ch~6Fh 32-bits Random number generator

Power on value : random

Recommended value : random

Power Plane : Resume

Bit	Access	Description
31:0	RO	Random Number.

Register 70h~71h Programmable 16-bits IO/CFG Port Trap 2 Address (TRAP2_ADDR)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom Setting
15:0	R/W	**I/O Port Trap 2 Address** Any I/O or CFG access to the range of TRAP2_ADDR and TRAP2_MASK will cause TRAP2_STS to be set to one.	0000h	0000h

Register 72h~73h Programmable 16-bits IO/CFG Port Trap 3 Address (TRAP3_ADDR)

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**I/O Port Trap 3 Address** Any I/O or CFG access to the range of TRAP3_ADDR and TRAP3_MASK will cause TRAP3_STS to be set to one.	0000h	0000h

Register 74h Programmable 16-bits IO/CFG Port Trap 2 Mask (TRAP2_MASK)

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting

7:0	R/W	**I/O Port Trap 2 Mask** A one in this register will select the low 8-bit mask for TRAP2_PORT.	00h	00h

Register 75h Programmable 16-bits IO/CFG Port Trap 3 Mask (TRAP3_MASK)

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**I/O Port Trap 3 Mask** A one in this register will select the low 8-bit mask for TRAP3_PORT.	00h	00h

Register 76h~77h PM_NEW Control 0

Power on value : 0000h

Recommended value : 2080h for P4/K7; 22A0h for K8

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15	R/W	**Internal test mode** (must keep as 0)	0	0
14	R/W	**Execute Throttling with STPGNT** 0: need STPGNT 1: needn't	0	0
13:10	R/W	**Internal test mode** (must keep as 1000)	0000	1000
9	R/W	**Fast Sx/Cx STPCLK# and Fast SMI#** 0: normal 1: Assert STPCLK#/SMI# before PCI response	0	P4/K7 : 0 K8: 1
8	R/W	**Internal test mode** (must keep as 0)	0	0

7	R/W	**FERR# for S1/Cx Wake-Up Enable** 0: Disable 1: Enable	0	1
6	R/W	**Q-Latch NMI/INTR/A20M/IGNE while STPCLK# asserting** 0: Enable 1: Disable	0	0
5	RO	**K8_SYSTEM Status** 0: Non K8 system 1: K8 System	0	P4/K7 : 0 K8: 1
4	R/W	**Mask all wakeup event while Speedstep** 0: Disable 1: Enable	0b	0b
3	R/W	**Prevent to enter C3 State** 0: Disable 1: Enable	0b	0b
2:0	R/W	**Reserved**	2'h0	2'h0

Register 78h Reserved

Power on value : 00h

Recommended value : 0010-1_00b

Power Plane : Resume

7:6	R/W	**Internal Used**	2'h0	2'h0
5	R/W	**HDA BCLK_IO driving strength** 0: weak 1: strong	0b	1b
4	R/W	**Reserved**	0b	0b
3	R/W	**HDA Modem Controller Power Management Event Enable (AUDPME_EN)** This bit is the same with ACPI R22h bit5	0	1
2	R/W	**HDA PME# event select bit** 0: AUX_AZ_PME_N 1: AUX_SDIWAK_PME_N	0b	By Codec

1:0	R/W	**HDA SDIx PME# event select bits** 00: AUX_SDI1WAK_PME_N 01: AUX_SDI0WAK_PME_N 10: AUX_SDI2WAK_PME_N	00b	00b

Register 79h~7Ah PM_NEW Control 1

Power on value : 0000h

Recommended value : 1000h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
15:13	R/W	**Reserved**	000	000
12	R/W	**PWRBTN wake up selection when system is off by Instant-off** 0: can be wake up by other events 1: only wake up by PWRBTN	0	1
11	R/W	**GPIOFF will make PCIRST# asserted before PS_ON de-asserted** 0: Disable 1: Enable	0	0
10:9	RO	**Reserved**	2'h0	2'h0
8	RW	**PCIEXP BEACON wake up enable (for S3/S4/S5)** 0: Disable 1: Enable	0	0
7:0	RO	**Reserved**	00	00

Register 7Bh AUX_GPIO Output Control

Power on value : 00h

Recommended value : 00h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting

7:0	R/W	**GPIO[14:7] Output Level Control (when XPWROK='0')** 0: BXGPIO[x]= GPO[x] 1: BXGPIO[x] = '0'	00h	00h

Register 7Ch PM_NEW Control 2

Power on value : 04h

Recommended value : 4h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
7:3	R/W	**Internal test mode**	00000	01000
2	R/W	**GPIOFF#_EN** If this bit is set and GPIOFF# is asserted, the system will POWER_OFF in 64ms. 0: Disable 1: Enable	1b	1b
1	R/W	**Internal test mode** (must keep as 0)	0	0
0	R/W	PCIE_PME_WAKE set PCIEWAK_STS(ACPI60HB3) 0: Enable 1: Disable	0	0

Register 7Dh PM_NEW Control 3

Power on value : 00h

Recommended value : A8h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**LDTREQ# / AGPBUSY# through APICCLK pin Enable** 0: disable, for P4/K7 CPU 1: enable, for K8 CPU	0	1
6	R/W	**VBLANKL enable for K8**	0	0

5:4	R/W	**Input source selection of LDTREQ# / AGPBUSY#** 00: both side-band / in-band signals 01: in-band input signal 10: side-band input signal 11: all disable	00	10
3	R/W	**Reverse the input polarity of LDTREQ# / AGPBUSY# through APICCLK pin** 0: disable 1: enable	0	1
2	R/W	**Reserved**	0	0
1	R/W	**PWRBTN# internal pull up resistor Enable** **0: enable** **1: disable**	0	0
0	R/W	**GPIO7 internal pull up resistor Enable** **0: enable** **1: disable**	0	0

Register 7Eh New GPI MUX Select

Power on value : 00h

Recommended value : 00h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Reserved**	0b	0b
6	R/W	**Select GPIO15/24 to set GPE1B15_STS (to assert SMI#)** 0: Select GPIO15 1: Select GPIO24	0b	0b

5	R/W	**Select GPIO12/23 to set GPE1B12_STS (to assert SMI#)** 0: Select GPIO12 1: Select GPIO23	0b	0b
4	R/W	**Select GPIO11/22 to set GPE1B11_STS (to assert SMI#)** 0: Select GPIO11 1: Select GPIO22	0b	0b
3	R/W	**Select GPIO8/21 to set GPE1B8_STS (to assert SMI#)** 0: Select GPIO8 1: Select GPIO21	0b	0b
2	R/W	**Reserved**	0b	0b
1	R/W	**Select GPIO6/SATA_HOTPLUG/OCI7 to set GPE1B6_STS (to assert SMI#)** 0: Select GPIO6 1: Select SATA_HOTPLUG/OCI7	0b	0b
0	R/W	**Select GPIO0/CBLIDA to set GPE1B0_STS (to assert SMI#, mobile only)** 0: Select GPIO0 1: Select CBLIDA	0b	0b

Register 7Fh

Power on value : 00h

Recommended value : 00h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
7	RO	**Reserved**	0b	0b
6:4	R/W	**Reserved**	3'h0	3'h0

3	R/W	**PCIEXP WAKE# pin wake up enable (for S1/S3/S4/S5)** **0: Disable** **1: Enable**	0	1
2:0	R/W	**Reserved**	3'h0	3'h0

Register 80h TTH/NTH Timing Control for AMD K8

Power on value : 00h

Recommended value : K8:1Ch

P4/K7: 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Thermal Throttling Lock:** Write '1' only, and it will disable TTH. Once set, this bit can be cleared by PCIRST#.	0	0
6	R/W	**Reserved**	0	0
5:4	R/W	**Throttling Minimum Enable Time** These bits specified the minimum time in which STPCLK# is held in the de-asserted state during throttling. 00: None 01: 10us 10: 20us 11: Reserved	00	P4:00b K8:01b
3	R/W	**Normal Throttling Period Select** 0: STPCLK# assertion during throttling is 30us, LDTSTOP# assertion during throttling is 2us. 1: STPCLK# assertion during throttling is 244us, LDTSTOP# assertion during throttling is 16us.	0	P4:0b K8:1b

2	R/W	**Thermal Throttling Period Select** 0: STPCLK# assertion during throttling is 30us, LDTSTOP# assertion during throttling is 2us. 1: STPCLK# assertion during throttling is 244us, LDTSTOP# assertion during throttling is 16us.	0	P4:0b K8:1b
1	R/W	**Reserved**	0	0
0	R/W	**Throttling 2 Second Delay** 0: Initiate throttling immediately after THERM# is asserted. 1: There is a 2 second delay after THERM# is asserted.	0	0

Register 81h Reserved

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Reserved**	8'h0	8'h0

Register 82h~83h C3 Timing Control 0 for AMD K8

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:2	R/W	**Reserved**	14'h0	14'h0

1:0	R/W	**C3 AGPSTOP# De-assertion Delay Time Select** Specified the delay between LDTSTOP# de-assertion and AGPSTOP# de-assertion at C3. 00: 1us (minimum) 01: 32us (+/- 10%) 10: 64us (+/- 10%) 11: 128us (+/- 10%)	00	00b

Register 84h~87h System Management Action Field for AMD K8

Power on value : 0000_0000h

Recommended value : 55CB_290Eh for K8

0000_0000h for P4/K7

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
31	R/W	**Thermal Throttling LDTSTOP# Enable** 0: Disable 1: Enable	0	0
30:28	R/W	**Thermal Throttling System Management Action Field (101)**	000	101
27	R/W	**Normal Throttling LDTSTOP# Enable** 0: Disable 1: Enable	0	0
26:24	R/W	**Normal Throttling System Management Action Field (101)**	000	101
23	R/W	**Reserved**	0	1
22:20	R/W	**S3 System Management Action Field (100)**	000	100
19	R/W	**S1 LDTSTOP# Enable** 0: Disable 1: Enable	0	1

18:16	R/W	**S1 System Management Action Field (011)**	000	011
15	R/W	**Reserved**	0	0
14:12	R/W	**VID/FID System Management Action Field (010)**	000	010
11	R/W	**C3 LDTSTOP# Enable** 0: Disable 1: Enable	0	1
10:8	R/W	**C3 System Management Action Field (001)**	000	001
7	R/W	**Reserved**	0	0
6:4	R/W	**C2 System Management Action Field (000)**	000	000
3	R/W	**Reserved**	0	1
2:0	R/W	**S4/S5 System Management Action Field (110)**	000	110

Register 88h~8Bh C3/S1/VFID Timing Control for AMD K8

Power on value : 0000_0000h

Recommended value : 0000_0002h for K8

0000_0000h for K7/P4

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
31:5	R/W	**Reserved**	27'h0	27'h0
4:3	R/W	**C3/S1 LDTSTOP# Assertion Delay Timer. (C3S1LST)** The register indicates the minimum delay between STPGNT cycle and LDTSTOP# assertion. 00: 1us 01: 32us 10: 64us 11: 128us	00	00

2:0	R/W	**VID/FID LDTSTOP# Assertion Delay Timer. (VFLST)** The register indicates the period of time that LDTSTOP# is asserted after receiving the STPGNT cycle associated with a HT system management VID/FID change request or **LSCMD** being written to a 1. 000: 1us (minimum) 001: 2us (+/- 10%) 010: 4us (+/- 10%) 011: 8us (+/- 10%) 100: 16us (+/- 10%) 101: 32us (+/- 10%) 110: 64us (+/- 10%) 111: 128us (+/- 10%)	000	010

Register 8Ch~8Fh LDTSTOP# Command for AMD K8

Power on value : 0000_0000h

Recommended value : 0000_0000h for K7/K8/P4

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
31:1	R/W	**Reserved**	31'h0	31'h
0	R/W	**LDTSTOP# Command** Writing a '1' to this bit result in: (1) The SB generates a STPCLK# with SMAF bits as specified by [C3SMAF]. (2) Upon receipt of the STPGNT cycle, LDTSTOP# is asserted for a period as specified by [FVLST]. (3) After HT link reconnects, the SB generates a STPCLK# de-assertion. (4) For consistency, the C3SMAF should be programmed to 3'b010 before changing link frequency or re-sizing the link.	0	0

Register 90h~91h Reserved for Internal Use

Power on value : 00_00h

Recommended value : For P4/K7: 00_00h

For K8: 00_00h

Power Plane : Core

Register 92h C3 Defer Control 0 Enable

Power on value : 00h

Recommended value : 3fh

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Reserved**	00	00
5	R/W	**IDE_C3_WAKEUP Enable bit** 1: Enable 0: Disable	0	1
4	R/W	**PCIE_C3_WAKEUP Enable bit** 1: Enable 0: Disable	0	1
3	R/W	**PCI_C3_WAKEUP Enable bit** 1: Enable 0: Disable	0	1
2	R/W	**AZ_C3_WAKEUP Enable bit** 1: Enable 0: Disable	0	1
1	R/W	**USB_C3_WAKEUP Enable bit** 1: Enable 0: Disable	0	1
0	R/W	**GMAC_C3_WAKEUP Enable bit** 1: Enable 0: Disable	0	1

Register 93h Reserved for Internal Use

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**For C3 Clock Option of P4**	8'h0	8'h0

Register 94h C3 Defer Control 1 Enable

Power on value : 00h

Recommended value : 80h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**LPC_C3_WAKEUP Enable bit** 1: Enable 0: Disable	0	1
6:5	R/W	**Reserved**	00	00
4:0	R/W	**For throttling Clock Option**	5'h0	5'h0

Register 95h Reserved for Internal Use

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**For C3 Clock Option of K8**	8'h0	8'h0

Register 96h C3 Defer Control 2 Enable

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Reserved**	0	0
6	R/W	**LSCMD_SMAF source select**	0	0
5	R/W	**AGP_BUSY DEFERR Control** **0: Enable** **1: Disable**	0	0
4	R/W	**P4 C3 Advanced Defer Enable bit** 1: Enable 0: Disable	0	0
3:0	R/W	**For VFID Clock Option**	4'h0	4'h0

Register 97h Reserved for Internal Use

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**For Sx Clock Option**	8'h0	8'h0

Register 98h C3 Defer Control 3 Enable

Power on value : 00h

Recommended value : f0h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**LPC_SPEC_REQN** 0: Enable 1.: Disable	0	1

6	R/W	**PCIE_SPEC_REQN** 0: Enable 1.: Disable	0	1
5	R/W	**USB_SPEC_REQN** 0: Enable 1.: Disable	0	1
4	R/W	**PCI_SPEC_REQN** 0: Enable 1.: Disable	0	1
3:2	R/W	**Reserved for Sx Option**	00	00
1:0	R/W	**For Sx Clock Option**	00	00

Register 99h Reserved for Internal Use

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/W	**Reserved**	4'h0	4'h0
3	R/W	**For C3 Clock Option of K8**	0	0
2:0	R/W	**Reserved**	3'h0	3'h0

Register 9Ah Reserved for Internal Use

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Reserved**	00	00
5:0	R/W	**For C3 Clock Option of K8**	6'h0	6'h0

Register 9B~9Ch IO/CFG TRAP Child Event Enable

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15	R/W	**TRAP 3 Configuration Read Child Event Enable** 0: Disable 1: Enable	0b	0b
14	R/W	**TRAP 2 Configuration Read Child Event Enable** 0: Disable 1: Enable	0b	0b
13	R/W	**TRAP 3 Configuration Write Child Event Enable** 0: Disable 1: Enable	0b	0b
12	R/W	**TRAP 2 Configuration Write Child Event Enable** 0: Disable 1: Enable	0b	0b
11:9	R/W	Reserved	000	000
8	R/W	**K8 INT_Pending Messages Assert to Wake up C3 Enable** 0: Enable 1: Disable	0b	0b
7	R/W	**TRAP 3 IO Read Child Event Enable** 0: Disable 1: Enable	0b	0b
6	R/W	**TRAP 2 IO Read Child Event Enable** 0: Disable 1: Enable	0b	0b

5	R/W	**TRAP 1 IO Read Child Event Enable** 0: Disable 1: Enable	0b	0b
4	R/W	**TRAP 0 IO Read Child Event Enable** 0: Disable 1: Enable	0b	0b
3	R/W	**TRAP 3 IO Write Child Event Enable** 0: Disable 1: Enable	0b	0b
2	R/W	**TRAP 2 IO Write Child Event Enable** 0: Disable 1: Enable	0b	0b
1	R/W	**TRAP 1 IO Write Child Event Enable** 0: Disable 1: Enable	0b	0b
0	R/W	**TRAP 0 IO Write Child Event Enable** 0: Disable 1: Enable	0b	0b

Register 9Dh Reserved

Power on value : 00h

Recommended value : For K8:06h, For P4:0Ch

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	Reserved	0	0
6:5	R/W	Reserved for internal use	00	00

4:3	R/W	The register indicates the period of time between de_asserted CPUSTP# and de_asserted CPUSLP# 00:32US 01:8US 10:64US 11:128US	00	—
2	R/W	**USBS1_PLLOFF** For USB 1.1 / 2.0 controllers can power down PLL during S1 sleeping state. 0:disable 1:enable	0	1
1:0	R/W	**Reserved for internal use**	00	00

Register 9Eh Watchdog Timer control

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**SMIMASKx enable bit** 0: Enable 1: Disable	0	0
6:4	R/W	**Reserved for internal use**	000	000
3	R/W	**WG_FIRED_STS clear bit (WG_STS_CLR)** 0: Disable 1: Enable	0	0
2	R/W	Watchdog Timer enable bit 0:disable 1:enable	0	0

1:0	R/W	The registers are the time base of Watchdog Timer. 00:1ms 01:10ms 10:100ms 11:1sec	00	00

Register 9Fh Reserved

Power on value : 00h

Recommended value : 84h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**K8 INT_Pending Events Assert IO/W Reg1E to Wake up C3 Enable** 0: Disable 1: Enable	0	note
6:3	R/W	**Reserved**	4'h0	4'h0
2	R/W	**In C2/THT, if PCI is busy, STPGNT hold temporary selection** 0: hold STPGNT 1: don't hold STPGNT	0	1
1:0	R/W	**Reserved for Internal Use**	00	00

Note:

By K8 MSR C001_0055h Intrrupt pending message enable or disable.

If Interrupt pending message disable and want to use ACPI base address + 1Eh to wakeup C3 that need to set this bit to 1.

Register A0~A3h MEM/IO/CFG Trap 0 Programmable Address

Power on value : 00000000h

Recommended value : 00000000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**MEM/IO/CFG Trap 0 Programmable Address**	32'h0	32'h0

Register A4~A5h MEM/IO/CFG Trap 0 Programmable Address Mask

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**MEM/IO/CFG Trap 0 Programmable Address Mask**	16'h0	16'h0

Register A6h MEM/IO/CFG Trap 0 Control

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Reserved**	00	00
5:4	R/W	**MEM/IO/CFG Trap 0 selection** 00: reserved 01: MEM 10: IO 11: CFG	00	00
3:2	R/W	**Software Watchdog Timer Clock Select** 00 : Refer to ACPI 4BHB[5:4] 01 : 1ms 10 : 2ms 11 : 256us	00	00

1	R/W	**MEM/IO/CFG Trap 0 child status enable** 0: disable 1: enable	0	0
0	R/W	**MEM/IO/CFG Trap 0 r/w selection** 0: read 1: write	0	0

Register A7h MEM/IO/CFG Trap child status

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:2	RO	**Reserved**	6'h0	6'h0
1	R/WC	**MEM/IO/CFG Trap 1 child status**	0	0
0	R/WC	**MEM/IO/CFG Trap 0 child status**	0	0

Register A8~ABh MEM/IO/CFG Trap 1 Programmable Address

Power on value : 00000000h

Recommended value : 00000000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**MEM/IO/CFG Trap 1 Programmable Address**	32'h0	32'h0

Register AC~ADh MEM/IO/CFG Trap 1 Programmable Address Mask

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting

15:0	R/W	**MEM/IO/CFG Trap 1 Programmable Address Mask**	0000h	0000h

Register AEh MEM/IO/CFG Trap 1 Control

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Reserved**	00	00
5:4	R/W	**MEM/IO/CFG Trap 1 selection** 00: reserved 01: MEM 10: IO 11: CFG	00	00
3:2	R/W	**Reserved**	00	00
1	R/W	**MEM/IO/CFG Trap 1 child status enable** 0: disable 1: enable	0	0
0	R/W	**MEM/IO/CFG Trap 1 r/w selection** 0: read 1: write	0	0

Register AFh Throttling timing control

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Reserved**	0	0
6	R/W	**Reserved for Internal Use**	0	0

5:4	R/W	**STPCLK# de-asserted time selection in Throttling** 00: 1us 01: 4us 10:16us 11:32us	00	00
3:2	R/W	**Reserved for Internal Use**	0	0
1:0	R/W	**Throttling clock base selection** 00:32us 01: 8 us 10: 4 us 11: 2 us	00	00

Register B0~B1h USB Control

Power on value : 00Eh

Recommended value : 02A8h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
15:14	R/W	USB IO Extended Squelch control selection 2'b00 : extened 1T squelch control 2'b01: extened 2T squelch control 2'b10 : extened 3T squelch control 2'b11: extened 0T squelch control	00b	00b
13	R/W	**USB IO Control** **dynamic select chirp and disconnect level.** 0 : enable dynamic select chirp k and disconnect level. 1 : disable this function. Control by bit 5.	0b	0b
12	R/W	**Reserved**	0	0
11	R/W	**Disconnect / ChirpK detection level control**	0	0

10	R/W	**Full Speed slew rate control** **This bit has to match up with B0h bit7.**	0	0
9:8	R/W	**Full Speed Vcr Control** 11 : Low 10 : Medium 1 01 : Medium 2 00 : High	00	10
7	R/W	**Full Speed slew rate control** This bit and B0h bit10 are used to control FS slew rate. B0hbit10 B0hbit7 current 1 1 60uA 1 0 80uA 0 1 100uA (Recommended setting) 0 0 120uA	0	1
6	R/W	**USB IO Control** Control Squelch level 0: 140mV 1: 120mV	0	0
5	R/W	**USB IO Control** Control disconnect and chrip k level. 1: 570mV (for disconnect) 0: 430mV (for chirpK)	0	1
4:3	R/W	**USB IO Control** HS driver output impedance control 11: < 45 ohm 10: 45 ohm 01: > 45 ohm 00: >> 45 ohm	01b	01b
2	R/W	**USB IO Control** Control pre-emp current enable 0: enable pre-emphasis 1: disable pre-emphasis	1	1
1:0	R/W	**USB IO Control** Control output current HS driver output current control 11: 18.66mA 10: 19.55mA 01: 20.88mA 00: 22.22mA	10b	01b

Register B2~B3h Reserved

Power on value : 0000h

Recommended value : 0000h

Power Plane : Resume

Register B4~B7h PM_NEW Control 4

Power on value : For P4: 00_00_2F_2Fh, For K8: 40_00_00_00h

Recommended value : 00000000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting

31	R/W	**Internal Used**	0b	0b
30	R/W	**C3_ENHANCE bit for BM_STS read path** (BM_STS read zero enable, should be enabled with BM_STS auto-clear bits) 0: disable 1: enable	0	P4:0 K8:1
29	R/W	**SATA hot plug enable registers** This bit is used to enable the hot plug function of SATA and assert status to GPE1B6_STS	0b	0b
28	R/W	**PCI_EXPRESS WAKE# enable registers** This bit is used to enable the assertion of the **PCI_EXPRESS WAKE#** pin / **BEACON** events to GPE0B11_STS 0: enable 1: disable	0b	0b
27	R/W	**PCI_EXPRESS WAKE# enable registers** This bit is used to enable the assertion of the **PCI_EXPRESS WAKE#** pin / **BEACON** events to GPE1B5_STS 0: enable 1: disable	0b	0b
26	R/W	**LDTSTOP# enable bit for VBLANKL function**	0b	0b
25	R/W	**PCI_EXPRESS PME enable registers** This bit is used to enable the assertion of the **PCI_EXPRESS PME** to GPE1B5_STS 0: enable 1: disable	0b	0b
24:23	R/W	**Internal Used**	00b	00b
22	R/W	**PCI_EXPRESS PME enable registers** This bit is used to enable the assertion of the **PCI_EXPRESS PME** to GPE0B11_STS 0: enable 1: disable	0b	0b
21	R/W	This register is used to set the PM1_STS register, if **PCIEXP WAKE#** pin / **BEACON** are asserted. 0: set to PM1_STS 1: don't set to PM1_STS	0b	0b

20	R/W	This register is used to set the PM1_STS register, if **PCIEXP WAKE#** pin / **BEACON** are asserted. 0: set to PM1_STS 1: don't set to PM1_STS	0b	0b
19:0	R/W	**Internal Used**	00000h	00000h

R

Register B8h C3 POP UP/DOWN Control

Power on value : 00h

Recommended value : P4:81h, K8:44h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Auto clear BM_STS when POP_DOWN_VLD assert** 0: disable 1: enable	0b	P4:1 K8:0
6	R/W	**Auto clear BM_STS when BMREQ# de-assert** 0: disable 1: enable	0b	P4:0 K8:1
5	R/W	**Auto clear BM_STS when POP_UP_T assert** 0: enable 1: disable	0b	0b
4:3	R/W	Reserved for internal use	2'h0	2'h0
2	R/W	**Bypass deferr enable bit** 0: disable 1: enable	0b	0b
1	R/W	**IDE CBLIDA/HTC select bit** If set '1', HTC_STPMSG or HTC_ACTMSG are selected to GPI0 0: IDE CBLIDA 1: HTC Message	0b	0b
0	R/W	**C2 / C3 popup and popdown enable bit** 0: disable 1: enable	0b	P4:1 K8:0

Register B9h~BAh

Power on value : 8000h

Recommended value : ffffh

Bit	Access	Description	Power On Value	Recom. Setting
15	R/W	**USB2.0 Controller Enable** This bit indicates USB2.0 controller is enabled/disbale. 0: Disable 1: Enable	1b	1b
14	R/W	USB20 Aux 30 MHz clock Root Gated function 1: enable 0: disable	0b	1b
13:8	R/W	**USB PLL POWER DOWN function** lock pll initial value.	000000b	111111b
7	R/W	**USB PLL POWER DOWN function** 0: disable 1: enable	0b	1b
6	R/W	**USB COMP POWER DOWN function** 0: disable 1: enable	0b	1b
5:0	R/W	**USB PLL POWER DOWN function** Reset pll initial value.	000000b	111111b

Register BBh

Power on value : 80h

Recommended value : 80h

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/W	**USB port number**	1000b	1000b
3	R/W	**PLL_POWER DOWN** (for usb20 control) This bit is set when PLL has been power down. This bit should be set if enable new wake up function.	0b	0b

2	R/W	**Wakeup function enable:** 0 : original wake up function. 1 : New wakeup function (use clk32k).	0b	0b
1	R/W	**UTMI Reset Source Selection** 1: power ok 0: from APIC register	0b	0b
0	R/W	**PLL Power Down Event Selection** 1: S3 (original function) 0: S3 or S1	0b	0b

Register BC~BDh Reserved

Power on value : 0000h

Recommended value : 3FFFh

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W	**Reserved**	3'h0	3'h0

Register BEh PM_NEW Control 5

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**K8_VFID_STPGNT decode by ACPI controller** 0: Disable 1: Enable	0	0
6	R/W	**K8_C3_STPGNT decode by ACPI controller** 0: Disable 1: Enable	0	0
5	R/W	**K8_C2_STPGNT decode by ACPI controller** 0: Disable	0	0

		1: Enable		
4	R/W	**K8_THT_STPGNT decode by ACPI controller** 0: Disable 1: Enable	0	0
3	R/W	**P4_C3_STPGNT decode by ACPI controller** 0: Disable 1: Enable	0	0
2	R/W	**P4_C2_STPGNT decode by ACPI controller** 0: Disable 1: Enable	0	0
1	R/W	**P4_THT_STPGNT decode by ACPI controller** 0: Disable 1: Enable	0	0
0	R/W	**SX_STPGNT decode by ACPI controller** 0: Disable 1: Enable	0	0

Register BFh PM_NEW Control 6

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Reserved for LDT internal optional bits**	8'h0	8'h0

Register C0h PM_NEW Control 7

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**C3 DPRSLPVR assertion enable** 0: Both C3 and C4 can assert DPRSLPVR 1: Only C4 can assert DPRSLPVR	0	0

6	R/W	**ACPI_ARBDIS_ASSERT / DEASSERT Enable bit** The bit is used for Yonah CPU 1: Enable 0: Disable	0	0
5	R/W	**PCIE2_S345_OFF enable** 0: Disable 1: Enable	0	0
4:1	R/W	**Reserved**	4'h0	4'h0
0	R/W	**PCIE1_S345_OFF enable** 0: Disable 1: Enable	0	0

Register C1h Reserved

Power on value : 00h

Recommended value : 00h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Advance deferr function2** 0: Disable 1: Enable	0	0
6:0	R/W	**ACPI internal debug MUX pins**	0000000	0000000

Register C2~C3h C3 Defer Control 4 Enable

Power on value : 0000h

Recommended value : 0000h

Power Plane : Core

Bit	Access	Description	Power On Value	Recom. Setting
15	R/W	**DEFER Enable bit** **The bit should be set with ACPI92Hb[7:0]** 1: Enable 0: Disable	0	0
14	R/W	**Reserved**	0	0

13:4	R/W	**Reserved for DPRSTP# timing option**	10'h0	10'h0
3	R/W	**DPRSTP# Enable bit** 1: Enable 0: Disable	0	0
2:0	R/W	**ACPI debug port select pin**	2'h0	2'h0

Register C4~C5h PM_NEW Control 8

Power on value : 0000h

Recommended value : 0000h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
15:3	R/W	**Reserved**	13'h0	13'h0
2	R/W	**SLP_Sx output mode select to p966 mode** 1: Enable 0: Disable	0	0
1:0	R/W	**SLP_Sx output mode selection** 00: Assert SLP_S3# and SLP_S5# when system enter S3 / S5 01: Assert SLP_S3# and SLP_S5# when enter S3 state, Only assert SLP_S5# when enter S5 state 10: Only assert SLP_S3# when enter S3 state. Assert SLP_S3# and SLP_S5# when enter S5 state. 11: Only assert SLP_S3# when enter S3 state. Only assert SLP_S5# when enter S5 state	00	10

Register C6h

Power on value : 00h

Recommended value : 04h

Bit	Access	Description	Power On Value	Recom. Setting
7:1	R/W	Reserved	0000000	0000010
0	R/W	**Reserved**	0	0

Register C7h Reserved

Power on value : 00h

Recommended value : 00h

Power Plane : Resume

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Reserved**	8'h0	8'h0

2.4.4. MEM/IO/CFG Trap Program Guide Table

IO Trap	ADDR	MASK	Child Status		Child Status Enable	
			Write	Read	Write	Read
0	50~51h	54h	4Fh[0]	4Fh[4]	9Bh[0]	9Bh[4]
1	52~53h	55h	4Fh[1]	4Fh[5]	9Bh[1]	9Bh[5]
2	70~71h	74h	4Fh[2]	4Fh[6]	9Bh[2]	9Bh[6]
3	72~73h	75h	4Fh[3]	4Fh[7]	9Bh[3]	9Bh[7]

CFG Trap (IO trap 2~3)	ADDR	MASK	Child Status		Child Status Enable	
			Write	Read	Write	Read
2	70~71h	74h	4Eh[4]	4Eh[6]	9Ch[4]	9Ch[6]
3	72~73h	75h	4Eh[5]	4Eh[7]	9Ch[5]	9Ch[7]

MEM/IO/CFG Trap	ADDR	MASK	Child Status	Child Status Trap Control		Child Status Enable
				MEM/IO/CFG Selection	Write/Read	
0	A0~A3h	A4~A5h	A7h[0]	A6h[5:4]	A6h[0]	A6h[1]
1	A8~ABh	AC~ADh	A7h[1]	AEh[5:4]	AEh[0]	AEh[1]

2.4.5. ACPI GPWAK# Programming Table for S1/S3/S4/S5

Sleeping Type	S1	S3/S4/S5
GPIO Mux	APC3[7]=0,APC3[6]=0, APC2[7]=1,APC7[5]=1, ACPI68[7]=1	APC3[7]=0,APC3[6]=0, APC2[7]=1,APC7[5]=1, ACPI68[7]=1
Trigger Mode / Input Polarity	ACPI38[7]=0,ACPI3E[7]=0	
SMI / SCI Routing	ACPI35[7:6] 01 : SMI# 10 : SCI	
Wake up Enable	ACPI32[7]=1	APC5[3]=1

2.4.6. Watchdog Timer Register

The following registers located at memory base address <Base> + the indicated offset value <Offset>. The base address is programmed in the Register PCI Configuration space.

Register 00h~04H Watchdog Timer Count Register

Power on value : 0000h

Recommended value : --------h

Power Plane: Core bit31~0

Bit	Access	Description	Power On Value	Recom. Setting
31-15	RO	Reserved	00b	00b
15-0	R/W	**Watched count data** This defines the countdown time for the counter. A value of zero is reserved. The units are defined in the Units field in the Watchdog Timer Resource table (WDRT). The maximum value is defined in the Max Count field in the WDRT. Reading this register result in the current counter value. Writing to the register has no effect until a one is written to the watchdog trigger bit of the watchdog Control/Status Register.	0b	0

Register 04~08h Watchdog Timer Control/Status Register

Power on value : 0000h

Recommended value : --------h

Power Plane: Core bit31~0

Bit	Access	Description	Power On Value	Recom. Setting
31:8	RO	Reserved	0	0
7	WO	**Watchdog Trigger** Setting this bit triggers the watchdog to start a new count interval, counting down from the value that was last written to the watchdog count register. This bit is always read as zero. Setting this bit has no effect if the watchdog is disable or stopped.	0b	0b
6:4	RO	Reserved.	0b	0b
3	RO	**Watchdog Disable** This bit reflects the state of the watchdog is disable or stopped. 0=Enable 1=Disable	0b	0b
2	R/W	**Watchdog Action** This bit determines the action to be taken when the watchdog timer expires. 0=system reset 1=system power off	00b	00b
1	R/W	**Watchdog fired** When set , the watchdog expired and caused the current restart. This bit is cleared for any restart that is not caused by the watchdog timer firing. If the watchdog Action Bit is set to 1(system power off) and the watchdog fires, forcing a shutdown ,the bit will be cleared on the next power up.	0b	0b

0	R/W	**Run/Stop Watchdog** This bit is used to control or indicate whether the watchdog is in the Running and Stopped states. 1= watchdog is in the Running state 0= watchdog is in the Stooped state. If the watchdog is in the Stopped state an a 1 is written to bit 0, the watchdog move to the running state but a count interval is not started until a l is written to bit 7.If the watchdog is in the Running state ,writing a 1 to bit o has no effect.	0b	0b

2.5. Register Summary / Description – Automatic Power Control Summary

2.5.1. Automatic Power Control (APC) Registers

Address	Access	Register Name
00h	R/W	CPU Frequency Modulation and Power Supply Control
01h	R/W	GPIO Function Selection 1
02h	R/W	GPIO Function Selection 2
03h	R/W	GPIO Function Selection 3
04h	R/W	System Power ON/OFF Control 1
05h	R/W	System Power ON/OFF Control 2
06h	R/W	System Power ON/OFF Control 3
07h	R/W	Optional Selection for MAC
08h	R/W	System Power ON/OFF Control 4
09h~0Eh	R/W	MAC Address Bytes
0Fh	R/W	MAC Control Byte 1
10h	R/W	System Power ON/OFF Control 5
11h	R/W	Parameters for RTC Oscillator
12h	R/W	MAC Control Byte 2
13h	R/W	Reserved

2.5.2. RTC Registers

The RTC internal registers and 114bytes RAM could be accessed by IOW 70 with index first and IOR/W 71 with the actual data. The IO port 70h and 71h could be also used to access the extended 128 bytes RTC RAMs and the APC register. The LPC Reg48h bit 7 and 6 are used to select which registers and RAM are accessed by the IO 70h and 71h. To solve the IO access 70h and 71h sequence is intercepted by the SMI routine, the SMI routine must store the IOW 70 value and LPC Reg48h bit 7 and 6 before to access any of these three RTC registers and RAMs. And recover the IOW 70h and LPC Reg48h before exit the SMI routine.

Index	Register Name	RTC Power On Value	Power Plane
00h	Seconds	-	RTC
01h	Seconds Alarm	-	RTC
02h	Minutes	-	RTC
03h	Minutes Alarm	-	RTC
04h	Hours	-	RTC
05h	Hours Alarm	-	RTC
06h	Day of Week	-	RTC
07h	Day of Month	-	RTC
08h	Month	-	RTC
09h	Year	-	RTC
0Ah	Register A	-	RTC
0Bh	Register B	-	RTC
0Ch	Register C	-	RTC
0Dh	Register D	-	RTC
0E-7D	114 Bytes RAM	-	RTC
7Eh	114 Bytes RAM – day alarm	-	RTC
7Fh	114 Bytes RAM – mon alarm	-	RTC

Register 0Ah RTC REGA

Bit	Access	Description	RTC Power On Value	Recom. Setting

7	RO	**Update In Progress(UIP)** It is a monitor flag indicates when a clock update cycle is about to take place. 0: The update cycle will not occur in 244us. The time, calendar and alarm register are valid for access when this bit is 0. 1: The updates is in progress or soon to occur.	-	-
6:4	R/W	**Divider Select(DIV[2:0])** These three bits can only be set to 010h, others are not valid. 010: 32.768Khz is selected	-	010b
3:0	R/W	**Periodic Interrupt Rate Select (PIRS[3:0])** These three bits are used to control the periodic interrupt rate when PIE bit in Register B is enabled. 0000: None 0001: 3.90526 ms 0010: 7.8125 ms 0011: 122.070 us 0100: 244.141 us 0101: 488.281 us 0110: 976.562 us 0111: 1.953125 ms 1000: 3.90625 ms 1001: 7.8125 ms 1010: 15.625 ms 1011: 31.25 ms 1100: 62.5 ms 1101: 125 ms 1110: 250 ms 1111: 500 ms	-	-

Register 0Bh RTC REGB

Bit	Access	Description	RTC Power On Value	Recom. Setting

7	RO	**Update Cycle Inhibit (SET)** Update cycles is enables or Inhibits. 0: Update cycle occurs normally. 1: The current update cycle is aborted and no update cycle can occur.	-	-
6	RW	**Periodic Interrupt Enable (PIE)** 0: Disable 1: Enable a periodic interrupt to occur at a rate controlled by the PIRS of REGA .	0	-
5	RW	**Alarm Interrupt Enable (AIE)** 0: Disable 1: Enable. An interrupt will be generated when AF bit is set by an alarm match.	0	-
4	RW	**Update-Ended Interruprt Enable (UIE)** 0: Disable 1: Enable. An interrupt will be generated at the end of Update cycle.	0	-
3	RO	Reserved.	0	-
2	RO	**Data Mode (DM)** Read as 0. So the Time, Calendar and Alarm register format are all in BCD. 0: BCD 1: Binary	-	-
1	RO	**Hour Format (HF)** Indicates the Hour Reg format. 0:12-hour 1: The current update cycle is aborted and no update cycle can occur.	-	-
0	RO	**Daylight Savings Enable (DSE)** When enable the hours Reg will be adjusted automatically on the last Sunday in October and April for daylight saving. 0: Disable 1: Enable	-	-

Register 0Ch RTC REGC

Bit	Access	Description	RTC Power On Value	Recom. Setting

7	RO	**Interrupt request Flag (IRQF)** IRQF=(PF&PIE) | (AF&AIE) | (UF&UIE) This bit is set when the PF/AF/UF interrupt flag and corresponding enable are set. Read to this register will clear this bit. 0: No RTC interrupt occur 1: RTC Interrupt occur.	0	-
6	RO	**Periodic Interrupt Flag (PF)** Periodic interrupt status indication. When this bit and PIE are set, the IRQF will be set and a RTC interrupt will occur. Read to this register will clear it.	-	-
5	RO	**Alarm Flag (AF)** Alarm interrupt status indication. When this bit and AE are set, the IRQF will be set and a RTC interrupt will occur. Read to this register will clear it.	-	-
5	RO	**Update-Ended Flag (UF)** Update cycle end interrupt status indication. When this bit and UIE are set, the IRQF will be set and a RTC interrupt will occur. Read to this register will clear it.	-	-
3:0	RO	Reserved	-	-

Register 0Dh RTC REGD

Bit	Access	Description	RTC Power On Value	Recom. Setting
7	RO	**Valid RAM and Time Bit (VRT)** This bit reflects the BATOK pin status. Read as 0 means the BATOK has been forced logic low. After read to REGD, this bit will be set to 1 till the BATOK is forced to logic low again.	-	-
6:0	RO	Reserved	-	-

2.5.3. APC Register

The following registers located at RTC power well. Before access to these registers, the APCRAM_EN(Bus0:Device2:Function0:Reg48h) must be set to one and EXTEND_EN must be set to zero.

Register 00h CPU Frequency Modulation and Power Supply Resume Control

Power on value : 00h

Recommended value : 04h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/W	**Multiplication of CPU Core Frequency to Bus Frequency** Bit 7 mapped to NMI Bit 6 mapped to INTR Bit 5 mapped to A20M# Bit 4 mapped to IGNNE#	0000b	0000b
3	R/W	**CPU Frequency Ratio Control Selection** 0 : By Hardware Trap 1 : By bit7~4 of this register	0b	0b
2	R/W	**Jumperless Reset Counter Enable** If CPU frequency ratio is selected as jumperless setting, the jumperless reset counter will start to count after PWROK goes n . When the counter expired, the CPU frequency ratio will be switched to hardware trap setting. 0 : Disable 1 : Enable	0b	1b
1:0	R/W	**Power Supply ON/OFF State Resume Control** The value in this field determines what the power supply state the system will return when the AC power is suddenly off then on. 00 : Always Off 01 : Reserved 10 : Always On 11 : Keep previous state	00b	00b

Register 01h GPIO Function Selection 1

Power on value : 00h

Recommended value : 44h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Reserved**	0b	0b
6	R/W	**GPIO1/LDRQ1# Selection** 1: LDRQ1# 0: GPIO1	0b	1b
5	R/W	**GPIO2/THERM# Selection** 1: THERM# 0: GPIO2	0b	0b
4	R/W	**GPIO3/EXTSMI# Selection** 1 : EXTSMI# 0 : GPIO3	0b	0b
3	R/W	**GPIO4/CLKRUN# Selection** 1 : GPIO4 0 : CLKRUN#	0b	0b
2	R/W	**GPIO5/PREQ5#; GPIO6/PGNT5# Selection** 1 : PREQ5#,PGNT5# 0 : GPIO5,GPIO6	0b	1b
1	R/W	**GPIO18/KBDRST# Selection** 1 : GPIO18 0 : KBDRST#	0b	0b
0	R/W	**GPIO17/GA20# Selection** 1 : GPIO17 0 : GA20#	0b	0b

Register 02h GPIO Function Selection 2

Power on value : 00h

Recommended value : 40h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**GPIO7/GPWAK# Selection** When this bit is set to 1, the GPWAK# can be used to wakeup system from S3/S4/S5. 1 : GPWAK# 0 : GPIO7	0b	0b

6	R/W	**GPIO8/RING Selection** 1 : RING 0 : GPIO8	0b	1b
5	R/W	**GPIO9/HDA_SDIN2 Selection** 1 : HDA_SDIN2 0 : GPIO9	0b	0b
4	R/W	**Reserved**	0b	0b
3:1	R/W	**GPIO[11:13] Enable** bit 3 => GPIO11, bit 2 =>GPIO12, bit 1 => GPIO13 1 : Disable 0 : Enable	000b	000b
0	R/W	**GPIO14 Selection** 1 : GPIO14 0 : S3AUXS	0b	0b

Register 03h GPIO Function Selection 3

Power on value : 00h

Recommended value : 06h

Power Plane: RTC

Bit	Access	Description	**Power On Value**	**Recom Setting**
7:6	R/W	**Selection Mux.input signal for GPIO**	00b	00b
5	R/W	**GPIO[15:18] MUX function selection** 0: GPIO[15:18] 1: AZDOCK_RST#, AZDOCK_EN#, GA20#, KBDRST#, DPRSTP#, GVGATE#, LOHI#, VR_HILO#	0b	0b
4	R/W	**Reserved**	0b	0b
3	R/W	**CPU_STP# /GPIO12 selection** 1 : CPU_STP# : **(Mobile only, connect the pin to CPU.DPSLP#)** 0 : GPIO12	0b	0b
2	R/W	**PSON# de-assertion control** This bit is used to control the PSON# de-assertion period when a power up event occur right after PSON# de-assertion. 1: 120ms (recommended) 0: 36us You can additionally set the APC8[3] to '1' to extend the 120ms to 480ms.	0b	1b

1	R/W	**RING Polarity Control** 0 : RING is an active high signal. 1 : RING is an active low signal.	0b	1b
0	R/W	**GPIO[15:18] MUX function selection** 0: GPIO[15:18] 1: AZDOCK_RST#, AZDOCK_EN#, GA20#, KBDRST#, DPRSTP#, GVGATE#, LOHI#, VR_HILO#	0b	0b

Register 04h System Power ON/OFF Control 1

Power on value : 00h

Recommended value : 03h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**GPIO[15:18] MUX function selection** 0: GPIO[15:18] 1: AZDOCK_RST#, AZDOCK_EN#, GA20#, KBDRST#, DPRSTP#, GVGATE#, LOHI#, VR_HILO#	0b	0b
6	R/W	**GPIO[15:18] MUX function selection** 0: GPIO[15:18] 1: AZDOCK_RST#, AZDOCK_EN#, GA20#, KBDRST#, DPRSTP#, GVGATE#, LOHI#, VR_HILO#	0b	0b
5	R/W	**GPIO[15:18] MUX function selection** 0: GPIO[15:18] 1: AZDOCK_RST#, AZDOCK_EN#, GA20#, KBDRST#, DPRSTP#, GVGATE#, LOHI#, VR_HILO#	0b	0b
4	R/W	**GPIO[15:18] MUX function selection** 0: GPIO[15:18] 1: AZDOCK_RST#, AZDOCK_EN#, GA20#, KBDRST#, DPRSTP#, GVGATE#, LOHI#, VR_HILO#	0b	0b
3	R/W	**Reserved**	0b	0b
2	R/W	**Reserved**	0b	0b (MUST)
1	R/W	**ACPI S5 Function Enable (S5OFF_EN)** 0 : Disable 1 : Enable	0b	1b
0	R/W	**ACPI S3 Function Enable (S3OFF_EN)** 0 : Disable 1 : Enable	0b	1b

Register 05h System Power ON/OFF Control 2

Power on value : 00h

Recommended value : F2h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**RTC IRQ8 Wake from S3/S4/S5 Enable (RTC_S5WAK_EN)** 0 : Disable 1 : Enable	0b	1b
6	R/W	**RING Wake from S3/S4/S5 Enable (RING_S5WAK_EN)** 0 : Disable 1 : Enable	0b	1b
5	R/W	**MACPME Wake from S3/S4/S5 Enable (MACPME_S5WAK_EN)** 0 : Disable 1 : Enable	0b	1b
4	R/W	**PCIPME Wake from S3/S4/S5 Enable (PCIPME_S5WAK_EN)** 0 : Disable 1 : Enable	0b	1b
3	R/W	**SMBWAK Wake from S3/S4/S5 Enable (SMBWAK_S5WAK_EN)** 0 : Disable 1 : Enable	0b	0b
2:0	R/W	**Reserved**	0b	0b

Register 06h System Power ON/OFF Control 3

Power on value : 00h

Recommended value : C0h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**USB Wake up source select** 0: from USBPME# (new implement) 1: from USB Resume/S3WAK signals (original implement)	0b	1b
6	R/W	**USB Wakeup STS mapping** 0: Merge all STS to GPE0[14] 1: Separate USB[0,1,2,3]_STS to GPE0[14,4,7,6]	0b	1b
5	R/W	**Reserved**	0b	0b
4	R/W	**This bit configured PATA channel B as 2nd PATA IO or PCIEXPRESS hot plug IO** 0:2nd PATA IO 1:PCIEXPRESS Hot Plug IO	0b	0b
3:2	R/W	**Reserved**	0b	0b
1	R/W	**USB IO power saving in S3/S4/S5** If you connect the USB to Main power, the bit should be set to '1' before entering S3/S4/S5.	0b	0b
0	R/W	Reserved	0b	0b

Register 07h Optional Selection about MAC

Power on value : 00h

Recommended value : 0000-_0_0h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**DPRSLPVR select (Mobile only)** 0 : select GPIO13 1 : select ACPI DPRSLPVR	0b	0b
6	R/W	**VR_HILO# polarity selection** 0: default output LOW 1: default output HIGH	0b	0b
5	R/W	**GPWAK#(GPIO7) Wake from S3/S4/S5 Enable (GPWAK#_S5WAK_EN)** 0 : Disable 1 : Enable	0b	0b
4	R/W	**Reserved**	0b	0b
3	R/W	**APC LOAD** When this bit is set as 1 and then 0, the content of MAC address stored in APC register 09h to 0Eh, and MAC information in APC register 0Fh and 12h are restored into related GMAC operation registers. 0: Disable 1: Enable	0b	-
2	R/W	**RTC32KHZ/GPIO18 Selection (Mobile only)** 0: Normal GPIO18 1: RTC32KHZ Output	0b	0b
1	R/W	**APC MAC Address Valid Bit** It indicates the 48 bits MAC address(from APC registers 09h-0Eh) is valid or not. 0: Invalid 1: Valid	0b	-
0	R/W	**AUXOK optional selection for MAC** 0 : Normal 1 : The AUXOK for MAC is delayed 60~120ms from XAUXOK	0b	0n

Register 08h

Power on value : 00h

Recommended value : 08h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting

7	R/W	**GND_AUXselection** 0: GND_AUX 1: Reserved	0b	0b
6	R/W	**Enable bit for SLP_S5# (for Mobile only)** 0: disable 1: enable	0b	0b
5	R/W	**Enable bit for SLP_S3# (for Mobile only)** 0: disable 1: enable	0b	0b
4	R/W	**STP_PCI/GPIO11 Select** 0: select GPIO11 1: select STP_PCI	0b	0b
3	R/W	**Extend the timing between PSON# de-assertion and next PSON# assertion.** 0 : 120ms 1 : 480ms If you want to set the bit, please set the APC3[2] at the same time.	0b	1b
2	R/W	**Clock source of Random number gen.** 0: RTC32KHz 1: PCLK	0b	0b
1:0	R/W	Test for Random number gen.	0b	0b

Register 09~0Eh MAC Address Bytes

Power on value : 00h

Recommended value : 00h

Power Plane: RTC

Byte	Access	Description	Power On Value	Recom Setting
09~0Eh	R/W	**MAC Address** The 48-bit MAC address	00h	00h

Register 0Fh MAC Control Byte 1

Power on value : 00h

Recommended value : 74h (10/100Mb/s PHY), 77h (1000Mb/s PHY)

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Reserved**	0b	0b
6	R/W	**Input Buffer Selection Mode.** This bit controls whether MAC IO input signal for Single-end or differential mode. 0: Single end mode (MII) 1: Differential mode (RGMII)	0b	1b
5	R/W	**Magic Packet Detector Enable** This bit controls whether Rx MAC filters Magic Packet for power management or interrupt. If this bit is enabled, Rx MAC will filter every received frame for matching Magic Packet. If this bit is disabled, the Magic Packet filtering is ignored. 0: disable 1: enable	0b	1b
4	R/W	**Link Status Polling** This field controls hardware to polling PHY link status. The result is placed at **Link On/Off Indicator** bit. 0: disable 1: enable	0b	1b
3:2	R/W	**MAC Rx Clock Selection** This field selects MAC Rx clock source. 00: MII Tx Clock 01: MII Rx Clock 10: External Clock 11: Internal Clock	01b	01b
1:0	R/W	**MAC Tx Clock Selection** This field selects MAC Tx clock source. 00: MII Tx Clock 01: MII Rx Clock 10: External Clock 11: Internal Clock Note: Select 00b(MII Tx clock) for 10/100Mb/s PHY; 11b (Internal clock) for 1000Mb/s PHY.	00b	--

Register 10h

Power on value : 00h

Recommended value : 40h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**AGPSTPL/GPIO14 select** 0 : GPIO14 1 : AGPSTPL	0b	0b

6	R/W	**DEBPWROK** Debounce function on PWROK signal 0:disable 1:enable	0b	1b
5	R/W	**Reserved for internal use**	0b	0b
4:0	R/W	**Reserved for internal use**	0	0

Register 11h The Parameters of RTC Oscillator

Power on value : 00h

Recommended value : 00h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Reserved.**	00b	00b
5:3	R/W	**SR[2:0] for oscillator.—for internal use**	000b	000b
2	R/W	**Reserved**	0b	0b
1	R/W	**OSC ATE – for internal use**	0b	0b
0	R/W	**OSCPROBEN. – for internal use**	0b	0b

Register 12h MAC Control Byte 2

Power on value : 00h

Recommended value : 40h (10/100Mb/s PHY)

E0h (1000Mb/s PHY)

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**MII/RGMII Mode** This bit controls MAC/PHY interface mode. 0: MII mode 1: RGMII mode Note: Select 0b(MII mode) for 10/100Mb/s PHY; 1b (RGMII mode) for 1000Mb/s PHY	0b	-
6:5	R/W	**Operation Speed** This field controls MAC operation speed. 00b: undetermined 01b: 10Mbps 10b: 100Mpbs 11b: 1000Mbps	00b	11b
4:0	R/W	**SMI PHY Address** This field indicates the PHY address of SMI request.	0b	-

Register 13h Reserved

Power on value : 00h

Recommended value : 00h

Power Plane: RTC

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	Reserved	00h	00h

2.6. Advanced Programmable Interrupt Controller Register

The IOAPIC registers are accessed by an indirect addressing scheme using two registers (IOREGSEL and IODAT) that are located at memory address FEC0_0000h and FEC0_0010h.

To access any one of the IOAPIC registers, the IOAPIC REGSEL register is written with the address of IOAPIC register. The IOAPIC DAT register is then used to read or write the data from the IOAPIC register addressed by IOAPIC REGSEL register. All IOAPIC registers are accessed using 32 bit loads and stores.

2.6.1. IOAPIC Memory Registers

Memory Address	Byte Length	Access	Register
FEC0_0000h	1	R/W	IOAPIC Register Select
FEC0_0010h	4	R/W	IOAPIC Data
FEC0_0020h	1	WO	IRQ Pin Assertion
FEC0_0040h	1	WO	EOI

IOAPIC Register Select Register (IOREGSEL)

Memory Address: FEC0_0000h

Default Value: 0000_0000h

Access: Read/Write

Bit	Access	Description
31:8	RO	Reserved
7:0	R/W	This field specifies which IOAPIC registers to be accessed via IOAPIC Data Register.

IOAPIC Data Register (IODAT)

Memory Address: FEC0_0010h

Default Value: 0000_0000h

Access: Read/Write

Bit	Access	Description
31:0	R/W	This register contains the data to be accessed from the IOAPIC register pointed by the IOREGSEL register.

2.6.2. IOAPIC Registers

Register	Byte Length	Access	Register
00h	4	R/W	ID
01h	4	RO	Version
02h	4	RO	IOAPIC Arbitration ID
03-0Fh		RO	Reserved
10h-11h	8	R/W	Redirection Table 0
12h-13h	8	R/W	Redirection Table 1
…	.	…	…
3Eh-3Fh	8	R/W	Redirection Table 23
40h-FFh		RO	Reserved

Register 00h Identification Register (ID)

Default Value: 0000_0000h

Access: Read/Write

Bit	Access	Description
31:24	R/W	This field contains the IOAPIC identification (IOAPIC ID). The APIC bus arbitration ID for the IO APIC is also loaded when the IOAPIC ID is programmed.
23:0	RO	Reserved

Register 01h Version Register

Default Value: 0017_0000h

Access: Read/Write

Bit	Access	Description
31:24	RO	Reserved
23:16	RO	This field indicates the entry number of the highest entry in the I/O redirection table. The hardwired value 17h to indicate 24 interrupt is supported by this IOAPIC.
15	RO	This bit is set to 1 to indicate that this version of the IOAPIC has implemented the IRQ Pin Assertion Register. (LPC Reg6C bit2)
14:8	RO	Reserved
7:0	RO	This field contains the version number of the IOAPIC. (LPC Reg6F)

Register 02h IOAPIC Arbitration

Default Value: 0000_0000h

Access: Read Only

Bit	Access	Description
31:28	RO	Reserved
27:24	R/W	This filed contains the IOAPIC Arbitration ID.
23:0	RO	Reserved

2.6.3. Redirection Table Entry Registers

There are 48 I/O Redirection Table entry registers. Each even and odd registers pairs below is a dedicated entry for each interrupt signal. Unlike IRQ pins of the 8259A, the notion of the interrupt priority is completely unrelated to the position of physical interrupt input signal on the APIC. Instead, software determines the vector (the priority) for each corresponding interrupt input signal. For each interrupt signal, the operating system can also specify the signal polarity (active low or high), trigger mode (edge or level), as well as the destination and delivery mode of the interrupt. The information in the redirection register is used to translate the corresponding interrupt pin information into an inter-APIC message.

Redirection Register Mapping Table

Register	IRQ#	Register	IRQ#
10h ~ 11h	0	28h ~ 29h	12
12h ~ 13h	1	2Ah ~ 2Bh	13
14h ~ 15h	2	2Ch ~ 2Dh	14
16h ~ 17h	3	2Eh ~ 2Fh	15
18h ~ 19h	4	30h ~ 31h	16
1Ah ~ 1Bh	5	32h ~ 33h	17
1Ch ~ 1Dh	6	34h ~ 35h	18
1Eh ~ 1Fh	7	36h ~ 37h	19
20h ~ 21h	8	38h ~ 39h	20
22h ~ 23h	9	3Ah ~ 3Bh	21
24h ~ 25h	10	3Ch ~ 3Dh	22
26h ~ 27h	11	3Eh ~ 3Fh	23

APIC Interrupt Table

IRQ#	From SIRQ	From External Pin	From Internal Device
0	No	No	8259 Master

1	Yes	No	
2	No	No	8254 Counter 0, HPET0
3	Yes	No	
4	Yes	No	
5	Yes	No	
6	Yes	No	
7	Yes	No	
8	Yes	No	RTC, HPET8
9	Yes	No	Option for SCI
10	Yes	No	Option for SCI
11	Yes	No	Option for SCI
12	Yes	No	Option for SCI
13	No	No	FERR#
14	Yes	No	
15	Yes	No	
16	INTA#	INTA#	PATA
17	INTB#	INTB#	SATA
18	INTC#	INTC#	Azalia
19	INTD#	INTD#	GMAC
20	No	INTE#	USB1.1 Controller #0, Option for SCI
21	No	INTF#	USB1.1 Controller #1, Option for SCI
22	No	INTG#	USB2.0, Option for SCI
23	No	INTH#	

Note: The IRQ option for SCI is controlled by LPC Register 68h.

Redirection Table Descriptor ODD Register (RTDO)

Default Value: 0000_0000h

Access: Read/Write

Bit	Access	Description
31:24	R/W	Destination Field If the destination mode of this entry is physical mode (RTDE register bit 11 = 0), bits [27:24] contain an APIC ID. If logical mode is selected (RTDE register bit 11 = 1), The destination field potentially defines a set of processors. Bits [31:24] of the destination field specify the logical destination address.
23:0	RO	Reserved

Redirection Table Descriptor Even Register (RTDE)

Default Value: 0001_0000h

Access: Read/Write

Bit	Access	Description
31:17	RO	**Reserved**
16	R/W	**Interrupt Mask** When this bit is 1, the interrupt signal is masked. 0:Not Masked 1:Mask interrupt
15	R/W	**Trigger Mode** The trigger mode field indicates the type of signal on the interrupt pin that triggers an interrupt. 0:Edge 1:Level
14	RO	**Remote IRR** This bit is used for level-triggered interrupts. It is undefined for edge-trigger interrupts. For level-triggered interrupts this bit is set to '1' when local APIC accepts the level interrupt sent by the IOAPIC. The remote IRR bit is set 0 when an EOI message with a matching interrupt vector is received from a local APIC.
13	R/W	**Interrupt Input pin Polarity** This bit determines the polarity of the interrupt signal. 0: Active high 1: Active low
12	RO	**Delivery Status** The delivery status bit contains the current status of the delivery of this interrupt. Delivery status is read-only and writes to this bit do not affect this bit. 0: Idle (there is currently no activity for this interrupt) 1: Send Pending (The interrupt has been injected but its delivery is temporarily held up due to the APIC bus being busy or the receiving APIC unit is unable to accept interrupt at that time.

11	R/W	**Destination Mode** This bit indicates the interpretation of the Destination field. 0: Physical mode (RTDE Register bits [27:24] = APIC ID) 1: Logical mode (RTDE Register bits [31:24] = Set of processors)
10:8	R/W	**Delivery Mode** The delivery mode specifies how the APICs listed in the destination field should act upon reception of this signal. 000: Fixed Priority 001: Lowest Priority 010: SMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	R/W	**Interrupt Vector** This field contains the interrupt vector for this interrupt. Vector values ranged from 10h to FEh.

IRQ Pin Assertion Register (IRQPA)

Memory Address: FEC0_0020h

Default Value: 0000_0000h

Access: Write Only

Bit	Access	Description
31:0	WO	Reserved
4:0	WO	IRQ Number: Bits[4:0] written to this field contain the interrupt number of which interrupt will be asserted.

EOI Register (EOI)

Memory Address: FEC0_0040h

Default Value: 0000_0000h

Access: Write Only

Bit	Access	Description
31:8	WO	Reserved

7:0	WO	If a write is issued to this register, the IOAPIC compare this field with the vector field for each entry in the redirection table. If a match is occurred, the remote IRR bit of matching entry table will be cleared.

2.7. High Precision Event Timer Registers

2.7.1. Programming Requirement

Register 70h High-Precision Event Timer Control Register

Power on value: 00h

Recommended value: 00h(HPET timer disable) or 91h(HPET timer enable)

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Timer 2 legacy INT (INT1~INT19) route capable** 0: Disable 1: Enable	0	1
6:5	R/W	**Reserved.**	0	0
4	R/W	**Reserved.**	0	0
3:1	R/W	**Reserved.**	0	0
0	R/W	**High-Precision Event Timer_EN** 0: Disable 1: Enable	0	1

Register 71h High-Precision Event Timer BASE Address and Control Register

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:4	R/W	**High-Precision Event Timer_BASE_ADDRESS** High-Precision Event Timer Base Address FED0_X000h. (only 0h, 1h, 2h, 4h are valid)	0	0

3:0	R/W	**Reserved.**	0	0

2.7.2. High Precision Event Timer Memory Registers

The Timer registers are memory mapped in a non-indexed scheme. This allows the CPU to directly access each register without having to use an index register. The timer register space is 1024 bytes. The registers are generally aligned on 64-bit boundaries to simplify implementation with IA64 processors. There are four possible memory address rages beginning at (1) FED0_0000h, (2) FED0_1000, (3) FED0_2000h, (4) FED0_4000h. The choice of address range is selected by LPC bridge (Device 2, Function 0) configuration register 71h, bit[7:4]. The length of the main counter could be 64 or 32 bits, selected by the LPC Reg70h, bit 1.

2.7.2.1. Programming Requirements

1. Software must not attempt to read or write across register boundaries. For example,a 32-bit access should be to offset x0h, x4h, x8h, or xCh. 32-bit accesses should not be to 01h, 02h, 03h, 05h, 06h, 07h, 09h, 0Ah, 0Bh, 0Dh, 0Eh, or 0Fh. 64-bit accesses can only be to x0h and must not cross 64-bit boundaries.
2. Software should not write to read-only registers.
3. Software should not expect any particular or consistent value when reading reserved registers or bits.
4. Software should perform read-modify-write operations on reserved bits.

2.7.2.2. High Precision Event Timer Memory Registers

Offset	Access	Register
000-007h	Read Only	General Capabilities and ID
008-00Fh		Reserved
010-017h	Read/Write	General Config
018-01Fh		Reserved
020-027h	Read/Write Clear	General Interrupt Status

028-0EFh		Reserved
0F0-0F7h	Read/Write	Main Counter Value
0F8-0FFh		Reserved
100-107h	Read/Write	Timer 0 Config and Capabilities
108-10Fh	Read/Write	Timer 0 Comparator Value
110-11Fh		Reserved
120-127h	Read/Write	Timer 1 Config and Capabilities
128-12Fh	Read/Write	Timer 1 Comparator Value
130-13Fh		Reserved
140-147h	Read/Write	Timer 2 Config and Capabilities
148-14Fh	Read/Write	Timer 2 Comparator Value
150-3FFh		Reserved

General Capabilities and ID Register (GCID)

Offset Address: 00h

Default Value: 0429_B17F_1039_A201h

Access: RO

Bit	Access	Description
63:32	RO	**COUNTER_CLK_PER_CAP:** Main Counter Tick Period: This read-only field indicates the period at which the counter increments in femptoseconds (10^-15 seconds).
31:16	RO	**VENDOR_ID_CAP:** This read-only field indicates to SiS.
15	RO	**LEG_RT_CAP:** A 1 in this bit indicates that the hardware supports the Legacy Interrupt Route option.
14	RO	**Reserved**
13	RO	**COUNT_SIZE_CAP:** Counter Size: A 1 in this bit indicates that the main counter is 64 bits wide, 0 for 32 bits wide. This bit could be controlled by the LPC Reg70h bit 1.
12:8	RO	**NUM_TIM_CAP:** Number of Timers: The number in the register indicates the last timer. The value in this field is 02h, indicating that there are thee timers.
7:0	RO	**REV_ID:** This indicates which revision of the function is implemented. This field is read as 01h.

General Config Register(GCON)

Offset Address: 010h

Default Value: 0000_0000_0000_0000h

Access: Read/Write

Bit	Access	Description
63:2	RO	Reserved
1	RW	**LEG_RT_CNF: Legacy Route:** If the ENABLE_CNF bit and the LEG_RT_CNF bit are both set, then the interrupts will be routed as follows: Timer 0 will be routed to IRQ0 in 8259 or IRQ2 in the I/O APIC Timer 1 will be routed to IRQ8 in 8259 or IRQ8 in the I/O APIC Timer 2-n will be routed as per the routing in the timer n config registers. If the Legacy Route bit is set, the individual routing bits for timers 0 and 1 (APIC or FSB) will have no impact. If the Legacy Route bit is not set, the individual routing bits for each of the timers are used.
0	RW	**ENABLE_CNF: Overall Enable:** This bit must be set to enable any of the timers to generate interrupts. If this bit is 0, then the main counter will halt (will not increment) and no interrupts will be caused by any of these timers.

General Interrupt Status Register(GIS)

Offset Address: 020h

Default Value: 0000_0000_0000_0000h

Access: Read/Write

Bit	Access	Description
63:3	RO	Reserved
2	RW	Timer 2 Interrupt Status
1	RW	Timer 1 Interrupt Status
0	RW	Timer 0 Interrupt Status The functionality of these bits depends on whether the edge or level-triggered mode is used for this timer. For Level-Triggered Mode: This bit defaults to 0. This bit will be set by hardware if the corresponding timer interrupt is active. Once the bit is set, it can be cleared by software writing a '1' to the same bit position. Writes of 0 to this bit will have no effect. For Edge-Triggered Mode: This bit should be ignored by software. A '1' write to this bit can clear the Interrupt as well.

Main Counter Value Register (MCV)

Offset Address: 0F0h

Default Value: 0000_0000_0000_0000h

Access: Read/Write

Bit	Access	Description
63:0	RW	**Counter Value[63:0]:**Software should access this register by 32-bit access for 32-bit counter and 64-bit access for 64-bit counter. 32-bit accesses can be done to offset 0F0h or 0F4h. 64-bit accesses can be done to 0F0h. 32-bit accesses must not be done starting at: 0F1h, 0F2h, 0F3h, 0F5h, 0F6h, or 0F7h. Writes to this register should only be done while the counter is halted. Reads to this register return the current value of the main counter. 32-bit counters will always return 0 for the upper 32-bits of this register. If 32-bit software attempts to read a 64-bit counter, it should first halt the counter. Since this will delay the interrupts for all of the timers, this should be done only if the consequences are understood. It is strongly recommended that 32-bit software only operate the timer in 32-bit mode. Reads to this register are monotonic. No two consecutive reads will return the same value. The second of two reads will always return a larger value (unless the timer has rolled over to 0).

Timer n Config and Capabilities Register (TCACn)

Offset Address: Timer 0: 100h – 107h

Timer 1: 120h – 127h

Timer 2: 140h – 147h

Default Value:

Access: Read/Write

Bit	Access	Description
63:56	RO	**Reserved**
55, 54 53, 52	RO	**TIMERn_INT_ROUT_CAP:**These read-only bits are set to 1 to indicate this timer's interrupt can be routed the Interrupt 20, 21, 22 and 23. This is used in conjunction with the TIMERn_INT_ROUTE_CNF field.
51:14	RO	**Reserved**
13:9	RW	**TIMERn_INT_ROUT_CNF:** This 5-bit indicates the routing for the interrupt to I/O APIC. Software writes to this field to select which interrupt in the I/O APIC will be used for this timer's interrupt. The software must only write the valid values.
8	T0:RW T1,2:RO	**TIMERn_32MODE_CNF:** Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit will be read/write and default to 0. For Timer 1 and 2, this bit will always read as 0 and writes have no effect.(since these two timers are 32-bits)
7	RO	**Reserved**

6	T0:RW T1,2:RO	**TIMERn_VAL_SET_CNF:** Software uses this bit only for Timer 0 if it has been set to periodic mode. By writing this bit to a 1, the software is then allowed to directly set the timer's accumulator. Software does NOT have to write this bit back to 0. (it automatically clears) Software should not write a 1 to this bit if the timer is set to non-periodic mode.
5	RO	**TIMERn_SIZE_CAP:** This read-only field indicates the size of the timer. Value is 1 (64-bit) for Timer 0 if LPC Reg70h, bit 1 is 1 or Value is 0 if LPC Reg70h, bit 1 is 1. Value is 0 (32-bit) for Timers 1 and 2.
4	RO	**TIMERn_PER_INT_CAP:** A 1 in this read-only field indicates the timer can support periodic mode. Value is 1 for Timer 0. Value is 0 for Timers 1 and 2.
3	T0:RW T1,2:RO	**TIMERn_TYPE_CNF:**For Timer 0 this bit is read/write, and can be used to enable timer to generate a periodic interrupt when write a 1 to it. For Timer 1 and 2 this bit is read only and read as 0.
2	RW	**TIMERn_INT_EN_CNF:** This bit must be set to enable timer n to cause an interrupt when it time out. If this bit is 0, the timer can still count and generate appropriate status bits, but will not cause an interrupt. Default value is 0.
1	RW	**TIMERn_INT_TYPE_CNF:** 0= Indicates the timer's interrupt is Edge triggered. If another interrupt occurs, another edge will be generated. 1= Indicates the timer's interrupt is Level triggered. The interrupt will be held active until the interrupt status bit in General Interrupt Status Register is cleared.
0	RO	**Reserved**

Timer n Compare Register(TCOMn)

Offset Address: Timer 0: 108h – 10Fh

Timer 1: 128h – 12Fh

Timer 2: 148h – 14Fh

Default Value:

Access: Read/Write

Bit	Access	Description
63:0	RW	Reads to this register return the current value of the comparator. Software can access the various bytes in this register using 32-bit or 64-bit accesses. 32-bit accesses can be done to offset 1x8h or 1xCh. 64-bit accesses can be done to 1x8h. 32-bit accesses must not be done to 1x9h, 1xAh, 1xBh, 1xDh, 1xEh, or 1xFh. **If the timer is configured to non-periodic mode:** A. Writes to this register load the value against which the main counter should be compared for this timer. B. When the main counter equals the value last written to this register, the corresponding interrupt can be generated (if so enabled). C. The value in this register does not change based on the interrupt being generated. **If the timer is configured to periodic mode:** A. When the main counter equals the value last written to this register, the corresponding interrupt can be generated. B. After the main counter equals the value in this register, the value in this register is increased by the value last written to the register. C. As each periodic interrupt occurs, the value in this register will increment. When the incremented value is greater than the maximum value possible for this register (FFFFFFFFh for a 32-bit timer or FFFFFFFFFFFFFFFFh for a 64-bit timer), the value will wrap around through 0. For example, if the current value in a 32-bit timer is FFFF0000h and the last value written to this register is 20000, then after the next interrupt the value will change to 00010000h Default value for each timer is all 1's for the bits that are implemented. For example, a 32-bit timer will have a default value of 00000000FFFFFFFFh. A 64-bit timer will have a default value of FFFFFFFFFFFFFFFFh.

2.8. SMBus Registers

2.8.1. SMBus Registers Summary

Offset	Byte Length	Access	Name	Power
00	1	R/W1C	SMBus Status	MAIN
01	1	R/W	SMBus Enable	MAIN
02	1	R/W1C RO	SMBus Control	MAIN
03	1	R/W	SMBus Host Control	MAIN
04	1	R/W	SMBus Address	MAIN
05	1	R/W	SMBus Command	MAIN
06	1	R/W	SMBus Packet Error Check Data	MAIN
07	1	R/W	SMBus Byte Count	MAIN
08	1	R/W	Alias Address	MAIN
09	1	R/W	Host Notify Device Address	MAIN
0A	1	R/W	SMBus Slave Data Byte 0	MAIN
0B	1	R/W	SMBus Slave Data Byte 1	MAIN
0C	1	R/W	Reserved	MAIN
0D	1	R/W	Reserved	MAIN
0E	1	R/W	Reserved	MAIN
0F	1	R/W, RO	Debug Register	MAIN
10-2F	32	R/W	SMBus Master Data Byte 0~31	MAIN

2.8.2. SMBus Register

The SMBus I/O Base Address and Enable bits are located in LPC Register 9A-9Bh.

Register 00h SMBus Status

Power on value: 00h

Recommended value: 00h

Access: Read/Write 1 Clear

The following registers are all sticky bits and only can be cleared by writing a one to their corresponding fields.

Bit	Access	Description	Power On Value	Recom. Setting
7	R/WC	**SMBus Slave Alert (SMB_ALT_STS)** The bit would be set when the SMBALT# is active. If this bit is set, SMBus Host Controller would not respond the transaction from other SMBus masters.	0	0
6	R/WC	**Hit Alias Address (SMB_ALIAS_STS)** The bit would be set when the SMBus Host Controller becomes a slave device and gets master cycle which matches the alias address defined at Register 08h. If this bit is set, SMBus Host Controller would not respond the transaction from other SMBus masters.	0	0
5	R/WC	**Hit Host Slave Address (SMB_HOST_STS)** The bit would be set when the SMBus Host Controller becomes a slave device and gets master cycle which matches the host slave address (0001_000xb). If this bit is set, SMBus Host Controller would not respond the transaction from other SMBus masters.	0	0
4	R/WC	**SMBus Slave Completion (SMB_SLAVE_STS)** The bit would be set after the transaction between SMBus Host Controller and a master device is completed. If this bit is set, SMBus Host Controller would not respond the transaction from other SMBus masters.	0	0
3	R/WC	**SMBus Master Completion (SMB_MASTER_STS)** The bit would be set when the SMBus Host Controller accomplishes the programmed process except the cycle is not reponeded by any SMBus device.	0	0

2	R/WC	**SMBus Collision (SMB_COL_STS)** This bit would be set when a collision condition occurs and SMBus Host loses in the bus arbitration. The software should clear this bit and re-start SMBus operation.	0	0
1	R/WC	**Device Error (SMB_DERR_STS)** This bit would be set when a Device Error condition occurs. The Device Errors may cause by: Host asserts an unclaimed slave address/data. Host detects a Slave Timeout—may be a Slave error condition. Slave detects a Master Timeout.	0	0
0	RO	**SMBus Interrupt Status (SMB_INTR_STS)** A one in this field indicates a SM Bus interrupt is generated by any of above Interrupt sources and their corresponding enable bits is set.	0	0

Register 01h SMBus Enable

Power on value: 00h

Recommended value: ffh

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**SMBus Slave Alert Interrupt Enable (SMB_ALT_EN)** When this bit is set, the assertion of SMB_ALT_STS would assert SMBINTR_STS. 0 : Disable 1 : Enable	0	1

6	R/W	**Hit Alias Address Interrupt Enable (SMB_ALIAS_EN)** When this bit is set, the assertion of SMB_ALIAS_STS would assert SMBINTR_STS. 0 : Disable 1 : Enable	0	1
5	R/W	**Hit Host Slave Address Interrupt Enable (SMB_HOST_EN)** When this bit is set, the assertion of SMB_HOST_STS would assert SMBINTR_STS. 0 : Disable 1 : Enable	0	1
4	R/W	**Slave Completion Interrupt Enable (SMB_SLAVE_EN)** When this bit is set, the assertion of SMB_SLAVE_STS would assert SMBINTR_STS. 0 : Disable 1 : Enable	0	1
3	R/W	**Host Master Interrupt Enable (SMB_MASTER_EN)** When this bit is set, the assertion of SMB_MASTER_STS would assert SMBINTR_STS. 0 : Disable 1 : Enable	0	1
2	R/W	**SMBus Collision Interrupt Enable (SMB_COL_EN)** When this bit is set, the assertion of SMB_COL_STS would assert SMBINTR_STS. 0 : Disable 1 : Enable	0	1
1	R/W	**Device Error Interrupt Enable (SMB_DERR_EN)** If this bit is set, the assertion of SMB_DERR_STS would assert SMBINTR_STS. 0 : Disable 1 : Enable	0	1

0	R/W	**SMBus Interrupt Enable (SMB_INTR_EN)** This bit is used to enable the SMBus interrupt generation. If this bit is set and its corresponding status bit is asserted, ACPI LEG_STS[11] would be asserted. 0 : Disable 1 : Enable	0	1

Register 02h SMBus Control

Power on value: 00h

Recommended value: 00h

Access: Read/Write, Read/Write 1 Clear, Read Only

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Alias Slave Enable (ALIAS_EN)** 0: Disable 1: Enable When this bit is enabled and the device address meets the Alias address, SMBus Host Controller would respond this transaction. Please program the Alias address first before set this bit enabled.	0	
6	R/WC	**PEC Error Status** The bit would be set when the PEC checking is error. Write one clear.	0	0
5	RO	**Register Software Grant Status (REG_SW_GNT)** When the SMBARB arbiter parks grant for register software request, the bit is set.	0	0
4	R/W	**Reserved**	0	0
3	R/W	Reserved	0	0

2	R/W	**Timeout Enable** 0: Disable 1: Enable When this bit is set and the transition time is over specification (clk low period > 25ms), a SMBus interrupt will be generated.	0	-
1	RO	**SMBus Busy Status** Any transaction occurs on the SMBus bus would set this status**.** This bit is used to monitor the activity of SMBus and prevents the transaction from colliding.	0	0
0	RO	**Host Busy Status** This bit would be set, if the host controller is used as a SMBus master and deliver any transactions.	0	0

Register 03h SMBus Host Control

Power on value: 00h

Recommended value: 00h

Access: Read/Write, Write Only

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Reserved**	00	00
5	WO	**Kill (SMB_Kill)** This bit is set to stop all SMBus operation, including Host master and slave, all activities are set to initial state. This operation won't affect the values in R/W registers.	0	0
4	WO	**Start (SMB_START)** Writing a 1 to this bit which initiate the SMBus Host transition. The SMBus Command Protocaol bits (SMB_PTL) and the associated registers should be properly programmed before this bit is set to 1. This is a write-only bit.	0	0

3	R/W	**PEC Enable (PEC_EN)** 0 : Disable 1: Enable When this bit is set, these protocols - Send/Receive byte, Write/Read byte, Write/Read word, Process call, Block Write/Read, Block write-block read process call, would append a Packet Error Code at the end of message transfer.	0	-
2:0	R/W	**SMBus Command Protocol (SMB_PTL)** Selecting the Protocol that SMBus Host is going to execute. Reading or Writing transition is determined by SMBus Address register bit 0 (R/W bit). **Bit[3:1]** **Protocol** 000 Quick command 001 Send/Receive Byte 010 Read/Write Byte Data 011 Read/Write Word Data 100 Process Call 101 Read/Write Block Data 110 Reservd 111 Block Write - Block Read Process Call	000	---

Register 04h SMBus Address

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7:1	R/W	**SMBus Address (SMB_ADDRESS)** The field is the slave address to target device.	0	0
0	R/W	**SMBus Read/Write (SMB_RW)** 1 : Execute a read protocol 0 : Execute a write protocol This bit doesn't affect Process Call protocol.	0	0

Register 05h SMBus Command

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**SMBus Command (SMB_COMMAND)** This register contains the command code and will be sent to device.	0	0

Register 06h SMBus Packet Error Check

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Data of SMBus Packet Error Check** This register is written with 8-bit CRC value as the SMB 2.0 PEC data prior to a write transaction. For read transaction, the PEC data is loaded from the SMB to the register and is then read by software. The register is not used when PEC_EN (03h[3])='0'.	0	0

Register 07h SMBus Byte Count (SMB_COUNT)

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:6	R/W	**Reserved**	0	0
5:0	R/W	**SMBus Byte Count** The field is the byte count for Block Read/Write protocol. The byte count can not be 0. 01h: 1 byte. 02h: 2 bytes. 03h: 3 bytes. …… 20h: 32 bytes. 21~3Fh: Reserved.	0	0

Register 08h Alias Address

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:1	R/W	**Alias Address** When Host Slave receives a Device Address the same as the address in these seven bits and bit 0 is '0', an interrupt will be raised if Alias Interrupt is also enabled.	0	0

0	R/W	This bit must be set as '0', because the Host Slave accepts master Write Word protocol only.	0	0

Register 09h Host Notify Device Address

Power on value: 00h

Recommended value: 00h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Host Notify Device Address** When Host Slave receives a Host Notify Command, the byte will record the device address.	0	0

Register 0A~0Bh SMBus Slave Data Byte 0~1

Power on value: 0000 h

Recommended value: 00 h

Access: Read/Write

Register 0C~0Eh Reserved

Register 0Fh Debug Register

Power on value: 00h

Recommended value: 00h

Access: Read/Write, Read Only

Bit	Access	Description	Power On Value	Recom. Setting
7	RO	**Reserved**	0	0
6	RO	**Reserved**	0	0
5:4	R/W	**Reserved**	0	0
3:0	R/W	**SMB Debug Select[3:0]**	0	0

Register 10~2Fh SMBus Master Data Byte 0~31

Power on value:
0000000000000000_0000000000000000_0000000000000000_0000000000000000 h

Recommended value:
0000000000000000_0000000000000000_0000000000000000_0000000000000000 h

Access: Read/Write

2.9. Serial Peripheral Interface (SPI)

SPI OP registers are defined at memory-mapped space. The SPI device could be accessed through the following SPI OP registers. The SPI Register address is composed of SPIBASE [31:16] + SPI Reg Offset. SPIBASE [31:16] is defined by the LPC configuration registers 98h and 99h.

2.9.1. SPI Operational registers Summary

SPI Reg offset	Access	Register Name
21h ~ 20h	RW/RWC	SPI Status
23h ~ 22h	RW/RO	SPI Control
27h ~ 24h	RO/RW	SPI Address
2Bh ~ 28h	RW	SPI_data_0_0
2Fh ~ 2Ch	RW	SPI_data_0_1
33h ~ 30h	RW	SPI_data_1_0
37h ~ 34h	RW	SPI_data_1_1
3Bh ~ 38h	RW	SPI_data_2_0
3Fh ~ 3Ch	RW	SPI_data_2_1
43h ~ 40h	RW	SPI_data_3_0
47h ~ 44h	RW	SPI_data_3_1
4Bh ~ 48h	RW	SPI_data_4_0
4Fh ~ 4Ch	RW	SPI_data_4_1
53h ~ 50h	RW	SPI_data_5_0
57h ~ 54h	RW	SPI_data_5_1
5Bh ~ 58h	RW	SPI_data_6_0
5Fh ~ 5Ch	RW	SPI_data_6_1
63h ~ 60h	RW	SPI_data_7_0
67h ~ 64h	RW	SPI_data_7_1
73h ~ 68h	RO	Reserved
75h ~ 74h	RW	SPI Prefix Opcode
77h ~ 76h	RW	SPI Opcode Type
7Bh ~ 78h	RW	OPMENU_0
7Fh ~ 7Ch	RW	OPMENU_1
83h ~ 80h	RW	SPI protected bios range 0
87h ~ 84h	RW	SPI protected bios range 1
8Bh ~ 88h	RW	SPI protected bios range 2
8Ch	RW	SPI Reset
8Fh ~ 8dh	RO	Reserved

2.9.2. SPI Registers

Register 21h ~ 20h SPI Status Register - SPIS

Power on value: 0000h

Recommended value: 0000h

Access: RO/RWC

Bit	Access	Description	Power On Value	Recom. Setting
15:3	RO	Reserved	0b	0b

2	RWC	**Cycle done status** Hardware set this to 1 when an access completes after setting the SPIC [1] bit. This bit can be cleared by writing a 1 or hardware reset. This bit must be cleared prior to enabling the SPI SMI# assertion.	0b	0b
1	RO	Reserved	0b	0b
0	RO	**SPI cycle in progress** Hardware set this bit when starting an SPI access. This bit remains set until the cycle completes in the SPI interface.	0b	0b

Register 23h ~ 22h SPI Control Register – SPIC

Power on value: 4300h

Recommended value: 4300h

Access: RW/RO

Bit	Access	Description	Power On Value	Recom. Setting
15	RW	**SMI# enable** 0: Disable 1: Enable When set to 1, the SPI controller asserts SMI# whenever cycle done status bit is 1.	0b	0b
14	RW	**DATA cycle** When set to 1, the SPI cycle runs in the SPI interface with data. When set to 0, no data is delivered.	1b	1b
13:8	RW	**Data byte count** Specify the number of data bytes to shift in or out during the SPI cycle. When set to 000000b, there is 1 byte to transfer. When set to 000001b, there are 2 bytes to transfer. …… When set to 111111b, there are 64 bytes to transfer.	000011b	000011b
7	RO	Reserved	0b	0b

6:4	RW	**Opcode pointer** Specify one of the programmed opcodes to be used in the non atomic SPI cycle. For atomic cycle, it specifies the second command code.	000b	000b
3	RW	**Prefix opcode pointer** Specify one of the programmed prefix opcodes to be used in the SPI cycle when Atomic cycle bit is set.	0b	0b
2	RW	**Atomic cycle** When set to 1, the SPI cycle will include a prefix opcode.	0b	0b
1	RW	**SPI cycle go** When set to 1, the SPI cycle start and the Cycle In progress bit of SPI status is set o 1 till the cycle end. This bit returns 0 on read.	0b	0b
0	RO	Reserved	0b	0b

Register 27h ~ 24h SPI Cycle Address SPIA

Power on value: 0000_0000h

Recommended value: 0000_0000h

Access: RO/RW

Bit	Access	Description	Power On Value	Recom. Setting
31:24	RO	Reserved	00h	00h
23:0	RW	**SPI cycle address** Specify the shifted out SPI cycle address.	00_0000h	00_0000h

Register 2Bh ~ 28h SPI_data_0_0

Power on value: 0000_0000h

Recommended value: 0000_0000h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting

31:0	RW	For write to SPI device, these bits specify the shifted out data. For read from SPI device, these bits store the shifted in data. The least significant byte is shifted first and bit sequence is from msb to lsb.	0000_0000h	0000_0000h

Register 2Fh ~ 2Ch SPI_data_0_1

Register 33h ~ 30h SPI_data_1_0

Register 37h ~ 34h SPI_data_1_1

Register 3Bh ~ 38h SPI_data_2_0

Register 3Fh ~ 3Ch SPI_data_2_1

Register 43h ~ 40h SPI_data_3_0

Register 47h ~ 44h SPI_data_3_1

Register 4Bh ~ 48h SPI_data_4_0

Register 4Fh ~ 4Ch SPI_data_4_1

Register 53h ~ 50h SPI_data_5_0

Register 57h ~ 54h SPI_data_5_1

Register 5Bh ~ 58h SPI_data_6_0

Register 5Fh ~ 5Ch SPI_data_6_1

Register 63h ~ 60h SPI_data_7_0

Register 67h ~ 64h SPI_data_7_1

Power on value: 0000_0000h

Recommended value: 0000_0000h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
31:0	RW	Refer to SPI_data_0_0 description.	0000_0000h	0000_0000h

Register 73h ~ 68h Reserved

Power on value: 0000_0000_0000_0000_0000_0000h

Recommended value: 0000_0000_0000_0000_0000_0000h

Access: RO

Register 75h ~ 74h SPI Prefix Opcode

Power on value: 0000h

Recommended value: 0000h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
15:8	RW	**Prefix_Opcode_1**; refer to Prefix_Opcode_0 description.	00h	00h
7:0	RW	**Prefix_Opcode_0** The first command of an atomic cycle.	00h	00h

Register 77h ~ 76h SPI Opcode Type

Power on value: 0002h

Recommended value: 0002h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
15:14	RW	**Opcode_Type_7**; refer to Opcode_Type_0 description.	00b	00b
13:12	RW	**Opcode_Type_6**; refer to Opcode_Type_0 description.	00b	00b
11:10	RW	**Opcode_Type_5**; refer to Opcode_Type_0 description.	00b	00b
9:8	RW	**Opcode_Type_4**; refer to Opcode_Type_0 description.	00b	00b
7:6	RW	**Opcode_Type_3**; refer to Opcode_Type_0 description.	00b	00b
5:4	RW	**Opcode_Type_2**; refer to Opcode_Type_0 description.	00b	00b
3:2	RW	**Opcode_Type_1**; refer to Opcode_Type_0 description.	00b	00b

1:0	RW	**Opcode_Type_0** These two bits define the SPI transaction type for Opcode_0. 00: Read cycle without address field need 01: Write cycle without address field need 10: Read Cycel with address field need 11: Write cycle with address filed need	10b	10b

Register 7Bh ~ 78h OPMENU_0

Power on value: 0000_000Bh

Recommended value: 0000_000B0h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
31:24	RW	**Opcode_3**; refer to Opcode_0 description.	00h	00h
23:16	RW	**Opcode_2**; refer to Opcode_0 description.	00h	00h
15:8	RW	**Opcode_1**; refer to Opcode_0 description.	00h	00h
7:0	RW	**Opcode_0** These bits specify the command code of SPI cycle. Software could program the appropriate command code in the Opcode_0 ~ Opcode_7 registers for later SPI device access.	0Bh	0Bh

Register 7Fh ~ 7Ch OPMENU_1

Power on value: 0000_0000h

Recommended value: 0000_0000h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
31:24	RW	**Opcode_7**; refer to Opcode_0 description.	00h	00h
23:16	RW	**Opcode_6**; refer to Opcode_0 description.	00h	00h
15:8	RW	**Opcode_5**; refer to Opcode_0 description.	00h	00h
7:0	RW	**Opcode_4**; refer to Opcode_0 description.	00h	00h

Register 83h ~ 80h SPI protected bios range 0 – PBR0

Power on value: 0000_0000h

Recommended value: 0000_0000h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
31	RW	**Write protection enable** When enable, the memory read to the address range defined by bit [23:0] will not be forwarded to SPI bus. 0: Disable 1: Enable	0b	0b
30:24	RO	**Reserved**	0000000b	0000000b
23:12	RW	**Protected range limit** The bit [23:12] specify the protected memory address A[23:11] upper limit which is combined with the base bits to define a memory address range. The A[11:0] is defined as FFFh for this upper limit.	000h	000h
11:0	RW	**Protected range base** The bit [11:0] specify the memory address A[23:12] base limit which is combined with the upper limit to define a memory range. The bit 31 determines if this memory range will be forwarded to SPI bus or not. The A[11:0] is defined as 000h for the base limit.	000h	000h

Register 87h ~ 84h SPI protected bios range 1 – PBR1

Power on value: 0000_0000h

Recommended value: 0000_0000h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
31	RW	**Write protection enable** Refer to Reg 83h ~ 80h descriptions. 0: Disable 1: Enable	0b	0b
30:24	RO	**Reserved**	0000000b	0000000b

23:12	RW	**Protected range limit** Refer to Reg 83h ~ 80h descriptions.	000h	000h
11:0	RW	**Protected range base** Refer to Reg 83h ~ 80h descriptions.	000h	000h

Register 8Bh ~ 88h SPI protected bios range 2 – PBR2

Power on value: 0000_0000h

Recommended value: 0000_0000h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
31	RW	**Write protection enable** Refer to Reg 83h ~ 80h descriptions. 0: Disable 1: Enable	0b	0b
30:24	RO	**Reserved**	0000000b	0000000b
23:12	RW	**Protected range limit** Refer to Reg 83h ~ 80h descriptions.	000h	000h
11:0	RW	**Protected range base** Refer to Reg 83h ~ 80h descriptions.	000h	000h

Register 8Ch and 8Dh SPI Reset

Power on value: 0000h

Recommended value: ----h

Access: RW

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RW	**Reset the SPI controller** Write any value to one of these two registers will cause the SPI control to be reset and stop any transaction. This register should only be written when software detect the SPI interface is hang.	0000h	----h

Reserved

Register xxxx_308Fh ~ xxxx_308Dh Reserved

Power on value: 000000h

Recommended value: 000000h

Access: RO

3. 968 PATA (Device2:Function5) (Legacy Only)

3.1. PATA Configuration Space Register

Offset	Register Name	Power On Value	Power Plane
00-01h	Vendor ID	1039h	MAIN
02-03h	Device ID	5513h	MAIN
04-05h	Device Control	0000h	MAIN
06-07h	Device Status	0210h	MAIN
08h	Revision ID	01h	MAIN
09h	Programming Interface	80h	MAIN
0Ah	Sub Class Code	01h	MAIN
0Bh	Base Class Code	01h	MAIN
0Ch	Cache Line Size	00h	MAIN
0Dh	Master Latency Timer	00h	MAIN
0Eh	Header Type	00h	MAIN
0Fh	BIST	00h	MAIN
10-13h	Primary Channel Command Block Base Address	00000001h	MAIN
14-17h	Primary Channel Control Block Base Address	00000001h	MAIN
18-1Bh	Secondary Channel Command Block Base Address	00000001h	MAIN
1C-1Fh	Secondary Channel Control Block Base Address	00000001h	MAIN
20-23h	Bus Master IDE Control Registers Base Address	00000001h	MAIN
24-27h	SATA Status and Control Register IO-Mapped Base Address (Mode 0 only)	00000000h	MAIN
28-2Bh	Reserved	00000000h	MAIN
2C-2Dh	Subsystem Vendor ID	0000h	MAIN
2E-2Fh	Subsystem ID	0000h	MAIN
30-33h	Reserved	00000000h	MAIN
34h	Capabilities Pointer	58h	MAIN
35-37h	Reserved	000000h	MAIN
38-3Bh	Reserved	00000000h	MAIN
3Ch	Interrupt Line	00h	MAIN
3Dh	Interrupt Pin	00h	MAIN

3Eh	Min_Gnt	00h	MAIN
3Fh	Max_Lat	00h	MAIN
40-43h	PATA Primary Channel Master Drive Control	1E1C66B2h	MAIN
44-47h	PATA Primary Channel Slave Drive Control	1E1C66B2h	MAIN
48-4Bh	Reserved	00000000h	MAIN
4C-4Fh	Reserved	00000000h	MAIN
50-51h	PATA Controller Primary Channel Control	2180h	MAIN
52-53h	PATA Controller Secondary Channel Control	00A0h	MAIN
54-57h	PATA Controller General Control	9011962Ah	MAIN
58h-5Bh	Power Management Capabilities	80020001h	MAIN
5C-5Fh	Power Management Control and Status	00000000h	MAIN
60-61h	Primary PATA Channel I/O Buffer Control	AAFBh	MAIN
62-63h	Reserved	0000h	MAIN
64-67h	EDC Register	0000DD00h	MAIN
68h	Primary Channel Master Autotiming Control	00h	MAIN
69h	Primary Channel Slave Autotiming Control	00h	MAIN
6A-6Bh	Reserved	0000h	MAIN
6C-6Fh	Reserved	00000000h	MAIN
70-73h	Reserved	00000000h	MAIN
74-77h	Reserved	00000000h	MAIN
78-7Bh	Reserved	00000000h	MAIN
7C-7Fh	Reserved	00000000h	MAIN
80-83h	1st SATA Channel Control	407E33BEh	MAIN
84-87h	2nd SATA Channel Control	407E33BEh	MAIN
88-8Bh	Reserved	00000000h	MAIN
8C-8Fh	Reserved	00000000h	MAIN
90-93h	Miscellaneous Control	03000140h	MAIN
94-97h	Reserved	00000000h	MAIN
98-9Bh	Reserved	00000000h	MAIN
9C-9Fh	Reserved	00000000h	MAIN
A0-A3h	Reserved	39E3B14Fh	MAIN
A4-A7h	Reserved	803E2498h	MAIN
A8-ABh	Reserved	0112401Ch	MAIN
AC-AFh	Reserved	02000000h	MAIN
B0-B3h	Reserved	00000000h	MAIN
B4-B7h	Reserved	00000000h	MAIN

B8-BBh	Reserved	7F7F7F7Fh	MAIN
BC-BFh	Reserved	7F7F7F7Fh	MAIN
C0-C3h	Reserved	00000000h	MAIN
C4-C7h	Reserved	00000000h	MAIN
C8-CBh	Reserved	00000300h	MAIN
CC-CFh	Reserved	00000000h	MAIN
D0-D3h	Reserved	00000000h	MAIN
D4-D7h	Reserved	00000000h	MAIN
D8-DBh	Reserved	00000300h	MAIN
DC-DFh	Reserved	00000000h	MAIN
E0-E3h	Reserved	00000000h	MAIN
E4-E7h	Reserved	00000000h	MAIN
E8-EBh	Reserved	00000000h	MAIN
EC-EFh	Reserved	00000000h	MAIN
F0-F3h	Reserved	00000000h	MAIN
F4-F7h	Reserved	00000000h	MAIN
F8-FBh	Reserved	00000000h	MAIN
FC-FFh	Reserved	00000000h	MAIN

Register 00-01h Vendor ID

Bit	Access	Description	Power On Value	Recom. Setting
15:0	RO	**Vendor Identification Number** The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.	1039h	

Register 02-03h Device ID

Bit	Access	Description	Power On Value	Recom. Setting

<table>
<tr>
<td>15:0</td>
<td>RO</td>
<td>Device Identification Number
The device identifier is allocated as 5513 by Silicon Integrated Systems Corp.
<table>
<tr><th>5513 Enable
Reg54h Bit31</th><th>RAID Enable
Reg54h Bit25</th><th>Device ID</th></tr>
<tr><td>1</td><td>0</td><td>5513</td></tr>
<tr><td>1</td><td>1</td><td>5513</td></tr>
<tr><td>0</td><td>0</td><td>1181</td></tr>
<tr><td>0</td><td>1</td><td>1180</td></tr>
</table>
Device ID can be programming to the value set in the Reg6Ch[15:0] if Reg54h Bit24 is set.</td>
<td>5513h</td>
<td></td>
</tr>
</table>

Register 04-05h Device Control

Bit	Access	Description	Power On Value	Recom. Setting
15:11	RO	**Reserved.** Read as zero.	00000b	
10	R/W	**Interrupt Disable** When this bit is set, the assertion of the INTX in native mode is disabled. 0: INTX is enabled. 1: INTX is disabled.	0b	0b
9:3	RO	**Reserved.** Read as zero.	0000000b	
2	R/W	**Bus Master** When this bit is set, the Bus Master function is enabled. 0: disable 1: enable	0b	1b
1	RO	**Memory Space** The bit will always be read as “0” because the IDE controller doesn’t need memory space.	0b	

0	R/W	**I/O Space** When enabled, the built-in IDE will respond to any access of the IDE legacy ports in the compatibility mode, or to any access of the IDE relocated ports in the native mode. Also, any access to the PCI bus master IDE registers are allowed. 0: disable 1: enable	0b	1b

Register 06-07h Device Status

Bit	Access	Description	Power On Value	Recom. Setting
15:14	RO	**Reserved.** Read as zero.	00b	
13	R/WC	**Master Abort Asserted** This bit is set 1 when a PCI bus master IDE transaction is terminated by master abort.	0b	
12	R/WC	**Received Target Abort** The bit is set 1 when a PCI bus master IDE transaction is terminated with target abort.	0b	
11	RO	**Signaled Target Abort** The bit will always be read as 0 because the IDE controller will never signal Target-Abort.	0b	
10:9	RO	**DEVSEL# Timing DEVT** These two bits define the timing of asserting DEVSEL#. The built-in IDE always asserts DEVSEL# in medium timing, and thus the two bits are read as 01 per PCI Spec.	01b	
8:5	RO	**Reserved.** Read as zero.	0000b	
4	RO	**Capabilities List** This read-only bit indicates whether or not IDE controller implements the pointer for a New Capabilities linked list at configuration register 34h.	1b	

3	RO	**Interrupt Status** This bit is the status of INTA#, and independent of **Interrupt Disable** at Reg04H, Bit10.	0b	
2:0	RO	**Reserved.** Read as zero.	000b	

Register 08h Revision ID

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	Revision Identification Number	01h	

Register 09h Programming Interface

Bit	Access	Description	Power On Value	Recom. Setting
7	RO	**Master IDE Device** This bit is hardwired to one to indicate that the built-in IDE is capable of supporting bus master function. IDE : Read as one. RAID : Read as zero.	1b	
6:4	RO	**Reserved.** Read as zero.	000b	
3	RO	**IDE:** This bit indicates whether or not the secondary channel has a fixed mode of operation. If this bit is zero, the mode is fixed and is determined by the (read-only) value of bit 2. If this bit is one, the channel supports both modes and may be set to either mode by writing bit 2. This bit can be modified by Reg50h Bit19. **RAID:** **Reserved.** Read as zero.	0b	
2	R/W	**IDE:** Determines the mode that the secondary channel is operating in. Zero corresponds to compatibility, one means native-PCI mode. This bit is implemented as read-only if the channel supports only one mode, or read-write if both modes are supported. **RAID:** **Reserved.** Read as zero.	0b	

1	RO	**IDE:** This bit indicates whether or not the primary channel has a fixed mode of operation. If this bit is zero, the mode is fixed and is determined by the (read-only) value of bit 0. If this bit is one, the channel supports both modes and may be set to either mode by writing bit 0. This bit can be modified by Reg50h Bit3. **RAID:** **Reserved.** Read as zero.	0b	
0	R/W	**IDE:** Determines the mode that the primary channel is operating in. Zero corresponds to compatibility, one means native-PCI mode. This bit is implemented as read-only if the channel supports only one mode, or read-write if both modes are supported. **RAID:** **Reserved.** Read as zero.	0b	

Register 0Ah Sub Class Code

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	The Sub Class Code is defined for the type of the mass storage controller. 01h: IDE controller 04h: RAID controller	01h	

5513 Enable Reg54h Bit31	RAID Enable Reg54h Bit25	Sub Class Code	Device ID
1	0	01	5513
1	1	01	5513
0	0	01	1181
0	1	04	1180

Register 0Bh Base Class Code

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Base Class Code**	01h	

Register 0Ch Cache Line Size

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Cache Line Size**	00h	

Register 0Dh Master Latency Timer

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Master Latency Timer** The initial value for latency timer. The Unit is the PCI clock.	00h	80h

Register 0Eh Header Type

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Header Type**	00h	

Register 0Fh BIST

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**BIST** IDE controller does not support BIST. Reserved. Read as zero.	00h	

Register 10-13h Primary Channel Command Block BAR

Register 14-17h Primary Channel Control Block BAR

Register 18-1Bh Secondary Channel Command Block BAR

Register 1C-1Fh Secondary Channel Control Block BAR

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**Base Address Register** These register is programmable only when both operating or native mode enabled, otherwise reads as 00000001h.	00000001h	

Register 20-23h Bus Master IDE Control Register Base Address

Bit	Access	Description	Power On Value	Recom. Setting

31:0	R/W	**Bus Master IDE Control Block BAR**	00000001h	

Register 24-27h SATA Status and Control Registers IO-Mapped BAR / AHCI Base Address Register

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**SATA SCR BAR** The SCR io-mapped function is supoorted when Reg54h Bit26 is set and mode 0 (Reg54h Bit11) is selected.	00000000h	

Register 2C-2Dh Subsystem Vendor ID

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W1	**Subsystem Vendor ID**	0000h	

Register 2E-2Fh Subsystem ID

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W1	**Subsystem ID**	0000h	

Register 34h Capabilities Pointer

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Capabilities Pointer** The offset into the function PCI Configuration Space for the location of the first item in the Capabilities linked list. The register read as 58h when Reg54h Bit28 set to one.	58h	

Register 3Ch Interrupt Line

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Interrupt Line** This register is writable when both operating modes enabled or one of the two channels operating in the Native mode.	00h	

Register 3Dh Interrupt Pin

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Interrupt Pin** This register is used to tell the drivers or operation systems that which interrupt pin the SATA controller uses. The value of this register is read only as 01h and means INTA# when bothmode or native mode is enabled.	00h	

Register 40-43h PATA Primary Channel Master Drive Control

Register 44-47h PATA Primary Channel Slave Drive Control

Bit	Access	Description	Power On Value	Recom. Setting
31:30	RO	**Reserved.** Read as zero.	00b	
29:24	R/W	**Recovery Time, T_{rco}**	011110b	Note 1
23:22	RO	**Reserved.** Read as zero.	00b	
21:16	R/W	**Active Time, T_{act}**	011100b	Note 1
15:12	R/W	**Initialize Time, T_{ini}**	0110b	Note 1
11:8	R/W	**CRC Valid Setup Time, T_{cvs}**	0110b	Note 1
7:4	R/W	**UDMA Cycle Time, T_{cyc}**	1011b	Note 1
3	R/W	**ATA133 Enable Control** 0: Disable. 1: Enable	0b	Note 2
2	R/W	**Ultra DMA Mode Control** 0: Disable. 1: Enable	0b	Note 3
1	R/W	**PIO IORDY Support** 0: Disable. 1: Enable	1b	Note 4
0	RO	**Reserved.** Read as zero.	0b	

Note 1: Tini, Tact, Trco, Tcyc, Tcvs Setting

Timing for mode under UDMA Mode 5 (decimal)

	PIO 0	PIO 1	PIO 2	PIO 3	PIO 4	DMA 0	DMA 1	DMA 2
T_{ini}	6	4	2	2	2	4	2	2
T_{act}	28	28	28	7	6	21	7	6
T_{rco}	30	9	3	9	4	25	6	4

	UDMA0	UDMA1	UDMA2	UDMA3	UDMA4	UDMA5	UDMA6
T_{cyc}	11	7	5	4	2	1	N/A
T_{cvs}	6	4	3	1	1	1	N/A

Timing for mode at UDMA Mode 6 (decimal)

	PIO 0	PIO 1	PIO 2	PIO 3	PIO 4	DMA 0	DMA 1	DMA 2
T_{ini}	9	6	3	3	3	6	3	3
T_{act}	38	38	38	10	9	28	10	9
T_{rco}	40	12	4	12	5	34	12	5

	UDMA0	UDMA1	UDMA2	UDMA3	UDMA4	UDMA5	UDMA6
T_{cyc}	15	10	7	5	3	2	1
T_{cvs}	9	6	4	2	2	2	2

Note 2: When the drive operates at UDMA Mode 6, this bit must be set to 1 to select correct operating clock.

Note 3: When the drive operates at UDMA Mode, this bit must be set to 1 to select correct DMA protocol with drive.

Note 4: When the drive supports PIO Mode 3 or PIO Mode 4, this bit could be set to 1 to support IORDY checking.

Register 50-51h Primary PATA Channel Control

Bit	Access	Description	Power On Value	Recom. Setting
15	RO	**CBLIDA signal status**		
14	R/W	**IDE I/O Pad 5.6k Pull-down Resister Control** 0: open circuit (Normal Operation) 1: 5.6kohm Pull-down	0b	0b

13	R/W	**Auto Pull-down Parallel ATA Data Bus at initial state of the PIO Protocol Timing Control** 0: disabled. 1: enabled.	1b	1b
12:9	RO	**Reserved.** Read as zero.	0h	
8	R/W	**Parallel ATA PIO Command Register Timing Control** This register is used to select the slowest timing setting in Reg4XH for both Master/Slave PIO command timing. 0: disabled. 1: enabled.	1b	1b
7	R/W	**IRQ Control** When this bit is set 0, the IRQ of HD drive would pass direct to 8259. On the others hand, IDE would gate IRQ until IDE FIFO is empty. 0: Direct Mode 1: Flush Mode	1b	1b
6	RO	**Reserved.** Read as zero.	0b	
5	RO	**Reserved.** Read as zero.	0b	
4	RO	**Reserved.** Read as zero.	0b	
3	R/W	**IDE Controller Operation Mode Control** 0: IDE Controller only supports Compatibility mode. 1: IDE Controller supports both modes. (Compatibility and Native mode).	0b	1b
2	R/W	**IDE I/O Buffer Tri-state Control** 0: Output Mode (Normal Operation) 1: Tri-state Mode	0b	0b
1	R/W	**IDE Channel Enable Control** 0: Disabled 1: Enabled	0b	1b
0	RO	**Cable Type Status** 0: 80-conductor cable, or no cable is used 1: 40-conductor cable		

Register 52-53h Secondary PATA Channel Control

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**IRQ Control** When this bit is set 0, the IRQ of HD drive would pass direct to 8259. On the others hand, IDE would gate IRQ until IDE FIFO is empty. 0: Direct Mode 1: Flush Mode	1b	1b
6:4	RO	**Reserved.** Read as 010b.	010b	
3	R/W	**IDE Controller Operation Mode Control** 0: IDE Controller only supports Compatibility mode. 1: IDE Controller supports both modes. (Compatibility and Native mode).	0b	1b
2	RO	**Reserved.** Read as zero.	0b	
1	R/W	**IDE Channel Enable Control** 0: Disabled 1: Enabled	0b	1b
0	RO	**Reserved.** Read as zero.	0b	

Register 54-57h PATA General Control Register

Bit	Access	Description	Power On Value	Recom. Setting
31	R/W	**5513 Device ID Change Control** **5513 Enable** (Reg54h Bit31) / **RAID Enable** (Reg54h Bit25) / **Device ID** 1 / 0 / 5513 1 / 1 / 5513 0 / 0 / 1181 0 / 1 / 1180	1b	
30	RW	**Configuration Space Remapping Control** 0: default 1: remapping. See appendix.	0b	
29	R/W	**Retry Function for PCI IO READ when SATA Physical Layer is not ready.** 0: Disabled. 1: Enable.	0b	0b

28	R/W	**Capability Pointer Control** 0: No Capability Supported. The Register 06h, Bit 4 and Register 34h would be read as zeros. 1: Capability Supported. The Register 06h, Bit 4 would be read as 1 and the Register 34h would be read as 00000058h.	1b	1b
27	R/W	**Active Bit Control in Bus Master IDE Status Register** 0: Active status Enhancement when mismatch of PRD's and IDE transfer size. 1: 963 algorithm	0b	0b
26	R/W	**Serial ATA Status and Control Register(SCR's) IO-Mapped Control** 0: default (configuration register access mode). 1: io-mapped mode. When this bit is set, **SCR's** register can be access by io access operation. And Io-mapped base address is located on Reg24H~27H.	0b	0b
25	RW	**RAID sub class enable.** 0: sub class 01h. 1: sub class 04h.	0b	
24	R/W	**PATA ID other than 5513/5518 OR 0180/0181 Enable** This bit control Device ID 5513 or Value of Reg 6C. 0: 5513/5518 OR 0180/0181. 1: Value of Reg 6C.	0b	0b
23:22	RO	**Reserved.** Read as zero.	00b	
21:20	R/W	**Master Read Request Threshold Setting** Request trigger at rested more than 00: Not Empty 01: over 1/4 FIFO 10: over 2/4 FIFO 11: over 3/4 FIFO	01b	01b
19:18	RO	**Reserved.** Read as zero.	00b	

<table>
<tr><td>17:16</td><td>R/W</td><td>Master Write Request Threshold Setting
Request trigger at used mode than
00: Not Empty
01: over 1/4 FIFO
10: over 2/4 FIFO
11: over 3/4 FIFO</td><td>01b</td><td>01b</td></tr>
<tr><td>15:12</td><td>R/W</td><td>Ready-to-Pause Time, Trp
Must be configured as 1001b.</td><td>1001b</td><td>1001b</td></tr>
<tr><td>11</td><td>R/W</td><td>IDE Mode Selection
<table>
<tr><td rowspan="2">Mode</td><td>Dev2 Fun5</td><td>Dev5 Fun0</td></tr>
<tr><td>Master / Slave</td><td>Master</td></tr>
<tr><td rowspan="2">0</td><td>PATA1 / PATA2</td><td rowspan="2">None</td></tr>
<tr><td>SATA1 / SATA2</td></tr>
<tr><td rowspan="2">1</td><td>PATA1 / PATA2</td><td>SATA1</td></tr>
<tr><td>None</td><td>SATA2</td></tr>
</table>
BIOS can not disable Dev5 Fun0 in LPC Reg7Ch Bit4 when mode 0 is selected.</td><td>1b</td><td></td></tr>
<tr><td>10:8</td><td>R/W</td><td>Strobe Stop Time, Tss
Must be configured as 110b.</td><td>110b</td><td>110b</td></tr>
<tr><td>7</td><td>R/W</td><td>D2 Support
This bit is written as 1 to indicate SATA controller supports the D2 power management state or it indicate SATA controller doesn’t support the D2 power management state.</td><td>0b</td><td>0b</td></tr>
<tr><td>6</td><td>R/W</td><td>D1 Support
This bit is written as 1 to indicate SATA controller supports the D1 power management state or it indicate SATA controller doesn’t support the D1 power management state.</td><td>0b</td><td>0b</td></tr>
<tr><td>5:4</td><td>R/W</td><td>Output Minimum Delay Time, Tzah
Must configured as 10b</td><td>10b</td><td>10b</td></tr>
<tr><td>3:2</td><td>R/W</td><td>Envelope Time, Tenv
Must configured as 10b.</td><td>10b</td><td>10b</td></tr>
<tr><td>1:0</td><td>R/W</td><td>Acknowledge Time, Tack
Must configured as 10b.</td><td>10b</td><td>10b</td></tr>
</table>

Register 58-5Bh Power Management Capabilities

Bit	Access	Description	Power On Value	Recom. Setting
31:27	RO	**PME Support** These bits would be read as 10000b.	10000b	
26	R/W	**D2 Support** This bit is read as 1 to indicate IDE controller supports the D2 power management state or it indicate IDE controller doesn't support the D2 power management state.	0b	
25	R/W	**D1 Support** This bit is read as 1 to indicate IDE controller supports the D1 power management state or it indicate IDE controller doesn't support the D1 power management state.	0b	
24:22	RO	**Reserved.** Read as zero.	000b	
21	RO	**Device Specific Initialization** This bit would be read as 0 to indicate no special initialization is required before the generic class device driver is able to use it.	0b	
20	RO	**Reserved.** Read as zero.	0b	
19	RO	**PME Clock** This bit would be read as 0 to indicate IDE controller would not generate PME# and no PCI clock is required.	0b	
18:16	RO	**PCI PM Spec. Version** A value of 010b indicates that this function complies with Reversion 1.1 of the PCI Power Management Interface Specification.	010	
15:8	RO	**Next Item Pointer** These bits would be 00h to indicate no additional items in the capabilities list.	00h	
7:0	RO	**Capability ID** Read as 01h to identify the linked list item as being the PCI Power Management register.	01h	

Register 5C-5Fh Power Management Control/Status

Bit	Access	Description	Power On Value	Recom. Setting
31:24	RO	**State Dependent Data** Not Implemented. Read as all zeros.	00h	
23:16	RO	**PMCSR PCI to PCI Bridge Support Extensions** Not Implemented. Read as all zeros.	00h	
15	RO	**PM Status** This bit would be 0 to indicate no PME# function is supported.	0b	
14:13	RO	**Data Scale** Not Implemented. Read as all zeros.	00b	
12:9	RO	**Data Select** Not implemented. Read as all zeros.	0000b	
8	RO	**PME Enable** This bit would be 0 to indicate no PME# function.	0b	
7:2	RO	**Reserved.** Read as zero.	00h	
1:0	R/W	**Power State** This two-bit field is used to determine the current power state and to set into a new power state. The definition is given below: 00b: D0 01b: D1 10b: D2 11b: D3hot	00b	

Register 60-61h Primary PATA Channel I/O Buffer Control

Bit	Access	Description	Power On Value	Recom. Setting
15:14	R/W	**IDE I/O Buffer Driving Strength Control for DD(15:0)** 00b: Strong 01b: Middle 10b: Normal 11b: Weak	10b	10b
13:12	R/W	**IDE I/O Buffer Driving Strength Control for DIOR and DIOW** 00b: Strong 01b: Middle 10b: Normal 11b: Weak	10b	10b

11:10	R/W	**IDE I/O Buffer Driving Strength Control for CS(1:0) and DA(2:0)** 00b: Strong 01b: Middle 10b: Normal 11b: Weak	10b	10b
9:8	R/W	**IDE I/O Buffer Driving Strength Control for DMACK** 00b: Strong 01b: Middle 10b: Normal 11b: Weak	10b	10b
7	R/W	**IDE I/O Buffer Slew Rate Control for DD(15:0)** 0: Fast 1: Slow	1b	1b
6	R/W	**IDE I/O Buffer Slew Rate Control for DIOR and DIOW** 0: Fast 1: Slow	1b	1b
5	R/W	**IDE I/O Buffer Slew Rate Control for CS(1:0) and DA(2:0)** 0: Fast 1: Slow	1b	1b
4	R/W	**IDE I/O Buffer Slew Rate Control for DMACK** 0: Fast 1: Slow	1b	1b
3	R/W	**IDE I/O Buffer 5.6k Pull-down Resister Control for DMARQ** 0: open circuit 1: 5.6kohm (minimum)	1b	1b
2	R/W	**IDE I/O Buffer 10k Pull-down Resister Control for DD7** 0: open circuit 1: 10kohm (minimum)	0b	0b
1	R/W	**IDE I/O Buffer 10k Pull-down Resister Control for INTRQ** 0: open circuit 1: 10kohm (minimum)	1b	1b
0	R/W	**IDE I/O Buffer 4.7k Pull-up Resister Control for IORDY** 0: open circuit 1: 4.7kohm (minimum)	1b	1b

Register 64-67h EDC Register

Bit	Access	Description	Power On Value	Recom. Setting
31:20	RO	**Reserved.**	000h	
19:18	RO	**Reserved.**	00b	
17	R/W	**DEV clock EDC Enable** **0:disabled** **1:enabled**	0b	1b
16	R/W	**PCI clock EDC Enable** **0:disabled** **1:enabled**	0b	1b
15:14	R/W	**DEV clock EDC Enter Timer Control** **11: 32T** **10: 17T** **01: 9T** **00: 5T**	11b	11b
13:12	R/W	**DEV clock EDC Wakeup Timer Control** **11: 8T** **10: 6T** **01: 5T** **00: 4T**	01b	01b
11:10	R/W	**PCI clock EDC Enter Timer Control** **11: 32T** **10: 17T** **01: 9T** **00: 5T**	11b	11b
9:8	R/W	**PCI clock EDC Wakeup Timer Control** **11: 8T** **10: 6T** **01: 5T** **00: 4T**	01b	01b
7:4	RO	**Reserved.**	0h	
3:0	R/W	**Reserved.**	0h	

Register 68h 1st PATA Channel Master Drive Auto-Timing Control

Register 69h 1st PATA Channel Slave Drive Auto-Timing Control

Bit	Access	Description	Power On Value	Recom. Setting

7:4	RO	**Parallel ATA Device UltraDMA/DMA Mode Detection** 0000: dma mode 0 is detected. 0001: dma mode 1 is detected. 0010: dma mode 2 is detected. 1000: ultra dma mode 0 is detected. 1001: ultra dma mode 1 is detected. 1010: ultra dma mode 2 is detected. 1011: ultra dma mode 3 is detected. 1100: ultra dma mode 4 is detected. 1101: ultra dma mode 5 is detected. 1110: ultra dma mode 6 is detected. others: reserved.	0000b	
3:1	RO	**Parallel ATA Device PIO Mode Detection** 000: pio mode 0 is detected. 001: pio mode 1 is detected. 010: pio mode 2 is detected. 011: pio mode 3 is detected. 100: pio mode 4 is detected. others: reserved.	000b	
0	R/W	**Parallel ATA Device Auto-timing Enable** When this bit is set, Auto-timing function is enabled. Auto-timing function is to use hardware method to set transfer mode timing according to the Set Feature Command sent to the attached drive. 0: disabled. 1: enabled.	0b	0b

Register 6C-6Fh Reserved Register

Bit	Access	Description	Power On Value	Recom. Setting
31:16	R/W	**Reserved.**	0000h	
15:0	R/W	**Configurable Device ID.** **The CDID is only valid when Reg54h bit24 is enabled. The CDID is a programmable Device ID and provides the flexibility to configure a specific ID.**	0000h	

3.2. IDE Device Program to SATA Device Configuration Registers

We can configured ATA controller as to one parallel ATA channel and two serial ATA ports by setting Reg54h Bit11 to zero.

D2F5R54B11		Mode 0	Mode 1 (Default)
		Master / Slave	Master
D2F5	Primary Channel	**PATA1 / PATA2**	**PATA1 / PATA2**
	Secondary Channel	**SATA1 / SATA2**	None
D5F0	Primary Channel	None	**SATA1 (AHCI1)**
	Secondary Channel	None	**SATA2 (AHCI2)**

We can set the different Device ID or Class Code as the following Table.

Device ID	Features	Class Code	D2F5R54B11	D2F5R54B25	D2F5R54B31	D5F0R54B11	D5F0R54B25
D2F5 + D5F0	D2F5 + D5F0	D2F5 + D5F0	Mode	r_raid_en	r_5513_en	sr_sub_06h	sr_raid_en
5513 + 1183	2P(IDE) + 2S(IDE)	0101 + 0101	1	0	1	0	0
5513 + 1184	2P(IDE) + 2S(RAID)	0101 + 0104	1	0	1	1	1
5513 + 1185	2P(IDE) + 2S(AHCI)	0101 + 0106	1	0	1	1	0
5513 + None	2P2S(IDE) + None	0101 + None	0	0	1	X	X

When mode 1 is selected, the PATA controller configuration space 80h-FFh are reserved and read as zero. Since there are two SATA ports in PATA controller when mode 0 is selected, the PATA controller have to configured the registers related to SATA. So when mode 0 is selected, the SATA related registers (80h to FFh) will map to PATA controller.

Mode 1 (Default)	
D2F5	D5F0
Reg 00h - 7Fh PATA Regs	Reg 00h - 7Fh SATA Regs 1
Reserved	Reg 80h - FFh SATA Regs 2

Mode 0	
D2F5	D5F0
Reg 00h - 7Fh PATA Regs	None
Reg 80h - FFh SATA Regs 2	

3.3. PCI Bus Master IDE Control Registers

The PCI Bus master IDE Control Registers locate 16 bytes of I/O Space. These registers can be accessed through I/O R/W to the address defined in the Bus

Master IDE control register Base Address. This Base Address is defined in Register 20h-23h of PCI SATA configuration space.

Offset	Register Name	Power On Value	Power Plane
00h	Bus Master Primary IDE Command Register	00h	MAIN
01h	Reserved	00h	MAIN
02h	Bus Master Primary IDE Status Register	00h	MAIN
03h	Reserved	00h	MAIN
04-07h	Bus Master Primary IDE PRD Table Address	00000000h	MAIN
08h	Bus Master Secondary IDE Command Register	00h	MAIN
09h	Reserved	00h	MAIN
0Ah	Bus Master Secondary IDE Status Register	00h	MAIN
0Bh	Reserved	00h	MAIN
0C-0Fh	Bus Master Secondary IDE PRD Table Address	00000000h	MAIN

Regiser 00h Bus Master Primary IDE Command Register

Regiser 08h Bus Master Secondary IDE Command Register

Bit	Access	Description	Power On Value	Recom. Setting
7:4	RO	**Reserved.** Read as zero.	0000b	
3	R/W	**Read or Write Control** This bit defines the R/W control of the bus master transfer. When set as zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.	0b	
2:1	RO	**Reserved.** Read as zero.	00b	
0	R/W	**Start/Stop Bus Master** Writing a '1' to this bit enables bus master operation of the controller. Bus master operation begins when this bit is detected changing from a zero to a one. The contoller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halt by writing a '0' to this bit.	0b	

Regiser 02h Bus Master Primary IDE Status Register

Regiser 09h Bus Master Secondary IDE Status Register

Bit	Access	Description	Power On Value	Recom. Setting
7	RO	**Native: Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.	0b	
6	R/W	**Native: Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.	0b	
5	R/W	**Native: Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers.	0b	
4:3	RO	**Native: Reserved.** Read as zero.	00b	
2	R/WC	**Native: Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.	0b	
1	R/WC	**Native: Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory. Writing a '1' to this bit can reset it.	0b	
0	RO	**Native: Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.	0b	

Regiser 04-07h Bus Master Primary IDE PRD Table Address

Regiser 0C-0Fh Bus Master Secondary IDE PRD Table Address

Bit	Access	Description	Power On Value	Recom. Setting

31:2	R/W	**Base Address of the PRD Table** This 32-bit register contains address pointing to the starting address of the PRD table.	00000000h	
1:0	RO	**Reserved.** Read as zero.	00b	

3.4. Configuration Space Re-mapping Control

When Register 54h, Bit 30 is set to '1', there are 2 differences with above configurations. 1. Register 40h ~ 47h offsets to 70h ~ 77h; 2. Register 48h ~ 4Bh is partially configured as the same as original 5513 IDE controller. The detailed configurations are as follows:

Register 48-4Bh Original 5513 Register

Bit	Access	Description	Power On Value	Recom. Setting
31:20	RO	**Reserved.** Read as zero.	000h	
19	RO	**Reserved.** Read as zero.	0b	
18	R/W	**IDE Secondary Channel Enable Control** 0: Disabled 1: Enabled	0b	
17	R/W	**IDE Primary Channel Enable Control** 0: Disabled 1: Enabled	0b	1b
16	R/W	**IDE Primary Channel I/O Buffer Tri-state Control** 0: Output Mode (Normal Operation) 1: Tri-state Mode	0b	0b
15:6	RO	**Reserved.** Read as zero.	000h	
5	RO	**Reserved.** Read as zero.	0b	
4	RO	**Primary Cable Type Status** 0: 80-conductor cable, or no cable is used 1: 40-conductor cable	0b	
3:0	RO		0000b	

Register 70-73h Remapped 1st Parallel ATA Channel/Master Drive Control

Register 74-77h Remapped 1st Parallel ATA Channel/Slave Drive Control

Bit	Access	Description	Power On Value	Recom. Setting
31:30	RO	**Reserved.** Read as zero.	00b	
29:24	R/W	**Recovery Time, T_{rco}**	011110b	Note 1
23:22	RO	**Reserved.** Read as zero.	00b	
21:16	R/W	**Active Time, T_{act}**	011100b	Note 1
15:12	R/W	**Initialize Time, T_{ini}**	0110b	Note 1
11:8	R/W	**CRC Valid Setup Time, T_{cvs}**	0110b	Note 1
7:4	R/W	**UDMA Cycle Time, T_{cyc}**	1011b	Note 1
3	R/W	**ATA133 Enable Control** 0: Disable. 1: Enable	0b	Note 2
2	R/W	**Ultra DMA Mode Control** 0: Disable. 1: Enable	0b	Note 3
1	R/W	**PIO IORDY Support** 0: Disable. 1: Enable	1b	Note 4
0	RO	**Reserved.** Read as zero.	0b	

Note 1: Tini, Tact, Trco, Tcyc, Tcvs Setting

Timing for mode under UDMA Mode 5 (decimal)

	PIO 0	PIO 1	PIO 2	PIO 3	PIO 4	DMA 0	DMA 1	DMA 2
T_{ini}	6	4	2	2	2	4	2	2
T_{act}	28	28	28	7	6	21	7	6
T_{rco}	30	9	3	9	4	25	6	4

	UDMA0	UDMA1	UDMA2	UDMA3	UDMA4	UDMA5	UDMA6
T_{cyc}	11	7	5	4	2	1	N/A
T_{cvs}	6	4	3	1	1	1	N/A

Timing for mode at UDMA Mode 6 (decimal)

	PIO 0	PIO 1	PIO 2	PIO 3	PIO 4	DMA 0	DMA 1	DMA 2
T_{ini}	9	6	3	3	3	6	3	3
T_{act}	38	38	38	10	9	28	10	9
T_{rco}	40	12	4	12	5	34	12	5

	UDMA0	UDMA1	UDMA2	UDMA3	UDMA4	UDMA5	UDMA6
T_{cyc}	15	10	7	5	3	2	1
T_{cvs}	9	6	4	2	2	2	2

Note 2: When the drive operates at UDMA Mode 6, this bit must be set to 1 to select correct operating clock.

Note 3: When the drive operates at UDMA Mode, this bit must be set to 1 to select correct DMA protocol with drive.

Note 4: When the drive supports PIO Mode 3 or PIO Mode 4, this bit could be set to 1 to support IORDY checking.

4. USB (Device3:Function0/1/3) Register Summary / Description

There are four USB Host Controllers embedded in the SiS968chip. They are assigned as device3 function0 (say as CHC0), function1 (say as CHC1), function2 (say as CHC2), and function3 (say as EHC3). CHC0, CHC1, and CHC2 are designed base on the Open Host Controller Interface Specification for USB Release 1.0a. EHC3 is designed base on the Enhance Host Controller Interface Specification 1.0. Each of the CHC supports a 3-port Root-Hub. The whole USB system can be programmed as 8-port to 1-port.

4.1. CHC0, CHC1 CHC2 Configuration Space

4.1.1. USB1.1 Configuration Space

Configuration. Offset	Access	Mnemonic Register
00-01h	RO	VID Vendor ID
02-03h	RO	DID Device ID
04-05h	R/W	CMD Command Register
06-07h	R/W	STS Status register
08h	RO	RID Revision ID
09-0Bh	RO	CD Class Code
0Ch	RO	CL Cache Line Size
0Dh	R/W	MLT Master Latency Timer
0Eh	RO	HT Header Type
0Fh	RO	BIST Built-in Self Test
10-13h	R/W	Base address
13-2Bh	RO	Reserved
2C-2Dh	RO	Subsystem Vendor ID
2E-2Fh	RO	Subsystem ID
34h	RO	Capabilities Pointer
3Ch	R/W	INTL Interrupt line
3Dh	RO	INTP Interrupt pin
3Eh	RO	MINGNT Min Gnt
3Fh	RO	MAXLAT Max Latency
44h	R/W	Operational Mode Enable Register
45h	R/W	Operational Mode Enable Register

46h	R/W	Operational Mode Enable Register
48h	R/W	Operational Mode Enable Register
49h	R/W	Operational Mode Enable Register

Vender ID Register

Register 00-01h Vender ID

Power on Value: 1039h

Access: Read

Bit	Access	Description
15:0	RO	Vendor ID

Device ID Register

Register 02-03h Device ID

Power on Value: 7001h

Access: Read

Bit	Access	Description
15:0	RO	Device ID

Command Register

Register 04-05h Command Register

Power on Value: 0000h

Recommend Value: 0007h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
15:11	R/W	Reserved Bits These bits are always 0.	0	0
10	R/W	**Interrupt Disable** This bit disables the device from asserting **INTx#**.	0b	0b
9	R/W	**Back to Back enable** Hydra only acts as a master to a single device, so this functionality is not needed. This bit is always 0.	0b	0b

8	R/W	**SERR#(Response) Detection Enable bit** If set to 1, Hydra asserts SERR# when it detects an address parity error. SERR# is not asserted if this bit is 0.	0b	0b
7	R/W	**Wait Cycle Control** Hydra does not need to insert a wait state between the address and data on the AD lines. This bit is always 0.	0b	0b
6	R/W	**PERR# (Response) Detection Enable bit** If set to 1, Hydra asserts PERR# when it is the agent receiving data and it detects a data parity error. PERR# is not asserted if this bit is 0.	0b	0b
5	R/W	**VGA Palette Snooping bit** Not Supported. Read as 0.	0b	0b
4	R/W	**Memory Write and Invalidate Command** If set to 1, Hydra is enabled to run Memory Write and Invalidate commands. The Memory Write and Invalidate Command will only occur if the cacheline size is set to 32 bytes and the memory write is exactly one cacheline.	0b	0b
3	R/W	**Special Cycle Enable** Hydra does not run special cycles on PCI. This bit is always 0.	0b	0b
2	R/W	**PCI Master Enable** If set to 1, Hydra is enabled to run PCI master cycles.	0b	1b
1	R/W	**Memory Enable** If set to 1, Hydra is enabled to respond as a target to memory cycles.	0b	1b
0	R/W	**I/O Enable** If set to 1, Hydra is enabled to respond as a target to I/O cycles.	0b	1b

Status Register

Register 06-07h Status Register

Power on Value: 0280h

Access: Read/Write

Bit	Access	Description
15	R/W	**Detected Parity Error** This bit is set to 1 whenever Hydra detects a parity error, even if the Parity Error (Response) Detection Enable bit is disabled. Cleared by writing a 1 to it.
14	R/W	**SERR# Status** This bit is set to 1 whenever the Hydra detects a PCI address parity error. Cleared by writing a 1 to it.
13	R/W	**Received Master Abort Status** Set to 1 when Hydra, acting as a PCI master, aborts a PCI bus memory cycle. Cleared by writing a 1 to it.
12	R/W	**Received Target Abort Status** This bit is set to 1 when a Hydra generated PCI cycle (Hydra is the PCI master) is aborted by a PCI target. Cleared by writing a 1 to it.
11	R/W	**Signaled Target Abort Status** This bit is set to 1 when Hydra signals target abort. Cleared by writing a 1 to it.
10-9	R/W	**DEVSEL# timing** Read only bits indicating DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
8	R/W	**Data Parity Reported** Set to 1 if the Parity Error Response bit is set, and Hydra detects PERR# asserted while acting as PCI master (whether PERR# was driven by Hydra or not).
7	R/W	**Fast Back-to-Back Capable** Hydra does support fast back-to-back transactions when the transactions are not to the same agent. This bit is always 1.
6	R/W	Reserved Bits These bits are always 0.
5	R/W	Reserved Bits These bits are always 0.

4	R/O	**Capabilities List** This bit indicates whether a list of extended capabilities is implemented. When set, this bit indicates the presence of Capabilities. A value of 0 means that this function does not implement Capabilities.
3	R/O	**Interrupt Status** This bit reflects the state of the interrupt in the device.
2-0	R/W	Reserved Bits These bits are always 0.

Revision ID Register

Register 08h Revision ID Register

Power on Value: 0fh

Access: Read

Bit	Access	Description
7:0	RO	Functional Revision Level

Class Code Register

Register 09-0Bh Class Code Register

Power on Value: 0C0310h

Access: Read

Bit	Access	Description
23:16	RO	**Base Class** The Base Class is 0Ch (Serial Bus Controller).
15:8	RO	**Sub Class** The Sub Class is 03h (Universal Serial Bus).
7:0	RO	Programming Interface The Programming Interface is 10h (OpenHCI).

Cache Line Size

Register 0Ch Cache Line Size

Power on Value: 00h

Recommend Value: 08h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting

7:0	R/W	**Cache Line Size** This register identifies the system cache line size in units of 32-bit words. Hydra will only store the value of bit 3 in this register since the cacheline size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register will be read back as 00h.	00h	08h

Latency Timer

Register 0Dh Latency Timer

Power on Value: 00h

Recommend Value: 20h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Latency Timer** This register identifies the value of the latency timer in PCI clocks for PCI bus master cycles.	00h	20h

Header Type Register

Register 0Eh Header Type Register

Power on Value: 80h/00h (function0/function1-3)

Access: Read

Bit	Access	Description
7:0	RO	**Header Type Register** This register identifies the type of the predefined header in the configuration space. Since USB is a device of SIS968 HC0 bit7 of this register is use to identify a multifunction device. When more than one USB HC is enabled, HC0 read out value is 80h, HC1, HC2 and EHCI is 00h.

BIST

Register 0Fh BIST

Power on Value: 00h

Access: Read

Bit	Access	Description

7:0	RO	**BIST** This register identifies the control and status of Built-In-Self-Test. Hydra does not implement BIST, so this register is read only.

Base Address Register

Register 10-13h Base Address Register

Power on Value: 00h

Access: Read/Write

Bit	Access	Description
31:12	R/W	**Base Address** POST writes the value of the memory base address to this register.
11:0	RO	Always 0. Indicates a 4K-byte address range is requested.

Subsystem Vendor ID

Register 2C-2Dh Subsystem Vendor ID

Power on Value: 0000h

Access: Write Once

Subsystem ID

Register 2E-2Fh Subsystem ID

Power on Value: 0000h

Access: Write Once

Capabilities Pointer

Register 34h Capabilities Pointer

Power on Value: 00h

Access: Read Only

Bit	Access	Description
7:0	R/W	**Capabilities Pointer** This register point to a linked list of new capabilities implemented by this device. This register is only valid if the “Capabilities List” bit in the Status Register is set. When Enable PMCS (USB CFG R45B4), this field point capability list to DCh.

Interrupt Line Register

Register 3Ch Interrupt Line Register

Power on Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	**Interrupt Line** This register identifies which of the system interrupt controllers the devices interrupt pin is connected to. The value of this register is used by device drivers and has no direct meaning to Hydra.

Interrupt Pin Register

Register 3Dh Interrupt Pin Register

Power on Value: 01h/02h/03h (function0/function1/function2)

Access: R/W

Bit	Access	Description
7:0	R/W	**Interrupt Pin** This register identifies which interrupt pin a device uses. Since SiS968USBHC0 default uses INTA#, the Power on Value is set to 01h; USBHC1 default uses INTB#, the Power on Value is set to 02h; USBHC2 default uses INTC#, the Power on Value is set to 03h. This field can be set by BIOS when set USB CFG R44B7.

Min_Gnt Register

Register 3Eh Min_Gnt Register

Power on Value: 00h

Access: RO

Max_Lat Register

Register 3Fh Max_Lat Register

Power on Value: 50h

Access: RO

Register 40-43h Reserved

Register 44h Operational Mode Enable Register

Power on Value: 22h

Recommend Value: 54h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Set_InterruptPin_Enable** When this bit is set, BIOS can program Hydra's Interrupt Pin in CFG R3Dh. When this bit is 0, CFG R3Dh is read only.	0b	0b
6	R/W	**BuferUnderOrphan** When set, it will fix the problem happened in DB module. The buffer point will reset while data underrun is occurred.	0b	1b
5	R/W	**NoResp3HS** The bit is low active. When clear, the Error interrupt is reported after three consecutive USB bus transfer error.	1b	0b
4	R/W	**HcControl bit 9 and bit10 Function Enable** When this bit is set, the function of RemoteWakeupConnected and RemoteWakeupEnable in OHCI will be enabled. Otherwise, these two bits are always cleared.	0b	1b
3	R/W	**Reserved.**	0b	0b
2	R/W	**BUFUNDEREOF** Setting this bit will stop the Data Buffer Module function until next access.	0b	1b
1	R/W	**S3_WAKEUP** HC will accept wait-state write command after leaving suspend mode if there are no device attached.	1b	0b
0	R/W	**Data Buffer Region16** When set the size of the region for the data buffer is 16 bytes. Otherwise, the size is 32 bytes.	0b	0b

Register 45h Operational Mode Enable Register

Power on Value: 01h

Recommend Value: adh/afh (P4 system/ K8 system)

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Delay suspend clock enable** When this bit is set, HC generate 4T 12M clock before enter USB suspend state.	0b	1b
6	R/W	Reserved	0b	0b
5	R/W	**Set USB Power OK** This bit enable USB IO port to drive bus. When this bit is 0, HC cannot drive any signals to USB bus.	0b	1b
4	R/W	**Mask PMCS** SIS968OpenHCI host controllers optional support power management capability function. When this bit is set, HC is PCI2.2 compliant. PMCS is masked	0b	0b
3	R/W	**Drive Resume Enable** When this bit is set, HC will drive resume signal to downstream port that sent remote wakeup signal in S3 or S4	0b	1b
2	R/W	**Restore Function Enable** Setting this bit can automatically restore all OHCI OP register after resuming from S3 or S4	0b	1b
1	R/W	**Advance SMI for K8** Setting this bit can advance SMI for legacy emulator to meet K8 criterion	0b	0b(P4) 1b(K8)

0	R/W	**cfg_sie_pipeline_disable** Disable completion code return at beginning of ACK packet transmission of IN transfer. (return at end of ACK packet.)	1b	1b

Register 46h Operational Mode Enable Register

Power on Value: 00h

Recommend Value: 01h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7-1		**Reserved**		
0	R/W	**Ready_for_restore** When this bit is set, HC automatically restore OP registers after resuming from S3.	0b	1b

Register 48h Operational Mode Enable Register

Power on Value: 00h

Recommend Value: 71h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	**Bypass USB signal to USB11** When this bit set, USB Bus will not through JOPPA(USB20).	0b	0b
6	R/W	**USB over current is a wakeup source** When set this bit, USB port over current event can be a wakeup source.	0b	1b
5	R/W	**Data-in is a wakeup source** When set this bit, any data transition causes a wakeup event.	0b	1b

4	R/W	**Unplug is a wakeup source** When set this bit, unplug cause a wakeup event.	0b	1b
3	R/W	Gated function prerun counter Prerun selection : Set 1 : need 8 T to wait clock stable. Set 0 : only 5 T.	0b	0b
2	R/W	Gated function prestop counter	0b	0b
1	R/W	**Data IN wakeup function selection** When set this bit, select new wakeup function.	0b	0b
0	R/W	**Enable USB S3 wakeup function** When set this bit, HC can support S3 wakeup.	0b	1b

Register 49h Operational Mode Enable Register

Power on Value: 00h

Recommend Value: 62h

Access: Read/Write

Bit	Access	Description	Power On Value	Recom. Setting
7	R/W	Set 1 : select new wakeup function (RTC CLOCL)from s1.	0b	0b
6	R/W	**Reserved**	0b	1b
5	R/W	**Reserved**	0b	1b
4	R/W	**Debug port enable** Setting this bit enable debug port	0b	0b
3	R/W	**Aux_debug_select0** Aux debug selection	0b	0b
2	R/W	**Aux_debug_select1** .Aux debug selection	0b	0b
1	R/W	**USB wakeup event detection clock select** Setting this bit, HC use 32K clock to sample remote wakeup signal. When this bit is 0, sample clock is 1KHz	0b	1b

0	R/W	**D2 support enable** When set, this function supports the D2 Power Management State.	0b	0b

Capabilities Identifier Register

Register DCh Capabilities Identifier Register

Power on Value: 01h

Access: Read

Bit	Access	Description
7-0	RO	**ID** A value of 01h identifies the linked list item as being the PCI Power Management registers.

Next Item Pointer Register

Register DDh Next Item Pointer Register

Power on Value: 00h

Access: Read

Bit	Access	Description
7-0	RO	**Next Item Pointer** This register provides an offset into the function's PCI Configuration Space pointing to the location of next item in the function's capability list. If there are no additional items in the Capabilities List, this register is set to 00h.

Power Management Capabilities Register

Register DEh Power Management Capabilities Register

Power on Value: C9C2h

Access: Read

Bit	Access	Description

15-11	RO	**PME_Support** This field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in the power state. Bit11 XXXX1b- PME# can be asserted from D0 Bit12 XXX1Xb- PME# can be asserted from D1 Bit13 XX1XXb- PME# can be asserted from D2 Bit14 X1XXXb- PME# can be asserted from $D3_{HOT}$ Bit15 1XXXXb- PME# can be asserted from $D3_{COLD}$
10	RO	**D2_Support** When set, this function supports the D2 Power Management State.
9	RO	**D1_Support** When set, this function supports the D1 Power Management State.
8-6	RO	**Aux_Current** This field reports the 3.3V Auxiliary current requirements for the PCI function. The bit assignments apply as follows: Bit Max. Current Required 1 1 1 375mA 1 1 0 320mA 1 0 1 270mA 1 0 0 220mA 0 1 1 160mA 0 1 0 100mA 0 0 1 55mA 0 0 0 0 (self powered)
5	RO	**DSI** The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. A “1” indicates that no initialization is required.
4	RO	Reserved
3	RO	**PME Clock** This bit indicates that the function relies on the presence of the PCI clock for PME# operation.

2-0	RO	**Version** A value of 010b indicates that this function complies with Revision 1.1 of the PCI Power Management Interface Specification.

Power Management Control/Status Register

Register E0h Power Management Control/Status Register

Power on Value: 0000h

Access: Read

Bit	Access	Description
15	R/W	**PME_Status** When set, it indicates that the function would normally assert the PME# signal independent of the state of the PME_En bit. Writing a "1" will clear it and cause the function to stop asserting a PME#. Writing "0" has no effect.
14-9	RO	Reserved
8	R/W	**PME_En** When set, it enables the function to assert PME#.
7-2	RO	Reserved
1-0	R/W	**PowerState** This field is used both to determine the current power state of a function and to set the function into a new power state. For SIS968USB OpenHCI host controllers, only support D0 and D3 state. 00b – D0 01b - D1 10b - D2 11b - $D3_{HOT}$

4.2. CHC0, CHC1, CHC2 Operational Registers

The base address of these registers is programmable by the memory base address register (USB PCI configuration register offset 10-13h). These registers should be written as Dword. Bytes write to these registers may have unpredictable effects.

The OpenHCI Host Controller (HC) contains a set of on-chip operational registers that are mapped into a non-cacheable portion of the system addressable space.

These registers are used by the Host Controller Driver (HCD). According to the functions of these registers, they are divided into four partitions, specifically for Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers should be read and written as Dwords.

Reserved bits may be allocated in future releases of this specification. To ensure interoperability, the Host Controller Driver that does not use a reserved field should not assume that the reserved field contains 0. Furthermore, the Host Controller Driver should always preserve the value(s) of the reserved field. When a R/W register is modified, the Host Controller Driver should first read the register, modify the bits desired, then write the register with the reserved bits still containing the read value. Alternatively, the Host Controller Driver can maintain an in-memory copy of previously written values that can be modified and then written to the Host Controller register. When a write to set/clear register is written, bits written to reserved fields should be 0.

4.2.1. Open Host Controller Interface Operational Registers

Offset	Register Name
0	HcRevision
4	HcControl
8	HcCommandStatus
C	HcInterruptStatus
10	HcInterruptEnable
14	HcInterruptDisable
18	HcHCCA
1C	HcPeriodCurrentED
20	HcControlHeadED
24	HcControlCurrentED
28	HcBulkHeadED
2C	HcBulkCurrentED
30	HcDoneHead
34	HcFmInterval
38	HcFmRemaining
3C	HcFmNumber
40	HcPeriodicStart
44	HcLSThreshold
48	HcRhDescriptorA
4C	HcRhDescriptorB

50	HcRhStatus
54	HcRhPortStatus[1]
58	HcRhPortStatus[2]
5C	HcRhPortStatus[3]
100	HceControl
104	HceInput
108	HceOutput
10C	HceStatus

4.2.2. Control and Status Partition

Register 00h HcRevision Register

Default Value: 00000110h

Access: Read

Bit	Access	Description
31:9		Reserved
8	RO	Legacy This read-only field is 1 to indicate that the legacy support registers are present in this HC.
7:0	RO	Revision This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 11h corresponds to version 1.1. All of the HC implementations that are compliant with current OpenHCI 1.0 specification will have a value of 10h.

Register 04h HcControl Register

Default Value: 00000000h

Access: Read/Write

The HcControl register defines the operating modes for the Host Controller. Only the Host Controller Driver, except Host Controller Functional State and Remote Wakeup Connected modifies most of the fields in this register.

Bit	Access	Description
31:11		Reserved

10	R/O	RemoteWakeupEnable This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signalling. When this bit is set and the Resume Detected bit in HC Interrupt Status is set, a remote wakeup is signalled to the host system. Setting this bit has no impact on the generation of hardware interrupt.
9	RO	Remote Wakeup Connected This bit indicates whether HC supports remote wakeup signalling or not. If remote wakeup is supported and used by the system, it is the responsibility of system firmware to set this bit during POST. HC clears the bit upon a hardware reset but does not alter it upon software reset.
8	R/W	Interrupt Routing This bit determines the routing of interrupts generated by events registered in HC Interrupt Status. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.
7:6	R/W	HostControllerFunctionalState for USB 00b: UsbReset 01b: UsbResume 10b: UsbOperational 11b: UsbSuspend A transition to UsbOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of HcInterruptStatus. This field may be changed by HC only in the UsbSuspend state. HC may move from the UsbSuspend state to the UsbResume state after detecting the resume signal from a downstream port. HC enters UsbSuspend after a software reset, whereas it enters UsbReset after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signal to downstream ports.

5	R/W	BulkListEnable This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to a ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling the processing of the list.
4	R/W	ControlListEnable This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, the processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to a ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling the processing of the list.
3	R/W	IsochronousEnable This bit is used by HCD to enable/disable the processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).
2	R/W	PeriodicListEnable This bit is set to enable the processing of the periodic list in the next Frame. If cleared by HCD, the processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.

1:0	R/W	ControlBulkServiceRatio This specifies the service ratio between Control and Bulk EDs. Before processing any of the non-periodic lists, HC must compare the ratio specified with its internal count on how many non-empty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value. **CBSR No. of Control EDs Over Bulk EDs Served** 0 1:1 1 2:1 2 3:1 3 4:1

Register 08h HcCommandStatus Register

Default Value: 00000000h

Access: Read/Write

The HcCommandStatus register is used by the Host Controller to receive commands issued by the Host Controller Driver, as well as reflecting the current status of the Host Controller. To the Host Controller Driver, it appears to be a "write to set" register. The Host Controller must ensure those “written as '1'” bits become set in the register while those “written as ‘0’” bits remain unchanged in the register. The Host Controller Driver may issue multiple distinct commands to the Host Controller without concern for corrupting previously issued commands. The Host Controller Driver has normal read access to all bits.

The SchedulingOverrunCount field indicates the number of frames with which the Host Controller has detected the scheduling overrun error. This occurs when the Periodic list does not complete before EOF. When a scheduling overrun error is detected, the Host Controller increments the counter and sets the SchedulingOverrun field in the HcInterruptStatus register.

Bit	Access	Description
31:18		Reserved
17:16	RO	SchedulingOverrunCount These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if Scheduling Overrun in Hc Interrupt Status has already been set. This is used by HCD to monitor any persistent scheduling problems.
15:4		Reserved

3	R/W	OwnershipChangeRequest This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the Ownership Change field in HcInterrupt Status. After the changeover, this bit is cleared and remains so until the next request from OS HCD.
2	R/W	BulkListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop

0	R/W	HostControllerReset This bit is set by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the UsbSuspend state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 μs. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signal should be asserted to its downstream ports.

Register 0Ch HcInterruptStatus Register

Default Value: 00000000h

Access: Read/Write

This register provides status on various events that cause hardware interrupts. When an event occurs, Host Controller sets the corresponding bit in this register. When a bit is set, a hardware interrupt is generated if the interrupt is enabled in the HcInterruptEnable register and the MasterInterruptEnable bit is set. The Host Controller Driver may clear specific bits in this register by writing '1'to bit positions to be cleared. The Host Controller Driver may not set any of these bits. The Host Controller will never clear the bit.

Bit	Access	Description
31		Reserved
30	R/W	Ownership Change Status This bit is set by HC when HCD sets the Ownership Change Request field in HcCommandStatus. This event, when unmasked, will always generate an System Management Interrupt (SMI#) immediately.
29:7		Reserved
6	R/W	RootHubStatusChange Status This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.
5	R/W	FrameNumberOverflow Status This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.

4	RO	UnrecoverableError Status This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset. This event is not implemented and is hard-coded to '0'.
3	R/W	ResumeDetected Status This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the UsbResume state.
2	R/W	StartofFrame Status This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	R/W	WritebackDoneHead Status This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	R/W	SchedulingOverrun Status This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.

Register 10h HcInterruptEnable Register

Default Value: 00000000h

Access: Read/Write

Each enable bit in the HcInterruptEnable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptEnable register is used to control those events generate a hardware interrupt. When a bit is set in the HcInterruptStatus register and the corresponding bit in the HcInterruptEnable register is set and the MasterInterruptEnable bit is set, then a hardware interrupt is requested on the host bus.

Writing a '1' to a bit in this register sets the corresponding bit, whereas writing a '0' to a bit in this register leaves the corresponding bit unchanged. On read, the current value of this register is returned.

Bit	Access	Description

31	R/W	MasterInterrupt Enable A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.
30	R/W	OwnershipChange Enable 0 : Ignore 1 : Enable interrupt generation due to Ownership Change.
29:7		Reserved
6	R/W	RootHubStatusChange Enable 0 : Ignore 1 : Enable interrupt generation due to Root Hub Status Change.
5	R/W	FrameNumberOverflow Enable 0 : Ignore 1 : Enable interrupt generation due to Frame Number Overflow.
4	R/W	UnrecoverableError Enable This event is not implemented. All writes to this bit will be ignored.
3	R/W	ResumeDetected Enable 0 : Ignore 1 : Enable interrupt generation due to Resume Detect.
2	R/W	StartofFrame Enable 0 : Ignore 1 : Enable interrupt generation due to Start of Frame.
1	R/W	WritebackDoneHead Enable 0 : Ignore 1 : Enable interrupt generation due to HcDoneHead Writeback
0	R/W	SchedulingOverrun Enable 0 : Ignore 1 : Enable interrupt generation due to Scheduling Overrun.

Register 14h HcInterruptDisable Register

Default Value: 00000000h

Access: Read/Write

Each disable bit in the HcInterruptDisable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptDisable register is coupled with the HcInterruptEnable register. Thus, writing a '1' to a bit in this register clears the corresponding bit in the HcInterruptEnable register, whereas writing a '0' to a bit in this register leaves the corresponding bit in the HcInterruptEnable register unchanged. On read, the current value of the HcInterruptEnable register is returned.

Bit	Access	Description
31	R/W	MasterInterrupt Disable A '0' written to this field is ignored by HC. A '1' written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.
30	R/W	OwnershipChange Disable 0 : Ignore 1 : Disable interrupt generation due to Ownership Change.
29:7		Reserved
6	R/W	RootHubStatusChange Disable 0 : Ignore 1 : Disable interrupt generation due to Root Hub Status Change.
5	R/W	FrameNumberOverflow Disable 0 : Ignore 1 : Disable interrupt generation due to Frame Number Overflow.
4	R/W	UnrecoverableError Disable This event is not implemented. All writes to this bit will be ignored.
3	R/W	ResumeDetected Disable 0 : Ignore 1 : Disable interrupt generation due to Resume Detect.
2	R/W	StartofFrame Disable 0 : Ignore 1 : Disable interrupt generation due to Start of Frame.
1	R/W	WritebackDoneHead Disable 0 : Ignore 1 : Disable interrupt generation due to HcDoneHead Writeback.

0	R/W	Scheduling Overrun Disable 0 : Ignore 1 : Disable interrupt generation due to Scheduling Overrun.

4.2.3. Memory Pointer Partition

Register 18h HcHCCA Register

Default Value: 00000000h

Access: Read/Write

The HcHCCA register contains the physical address of the Host Controller Communication Area. The Host Controller Driver determines the alignment restrictions by writing all 1s to HcHCCA and reading the content of HcHCCA. The alignment is evaluated by examining the number of zeroes in the lower order bits. The minimum alignment is 256 bytes; therefore, bits 0 through 7 must always return '0' when read. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.

Bit	Access	Description
31:8	R/W	This is the base address of the Host Controller Communication Area.
7:0		Reserved.

Register 1Ch HcPeriodCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcPeriodCurrentED register contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

Bit	Access	Description
31:4	R/W	PeriodCurrentED This is used by HC to point to the head of one of the Periodic lists that will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0		Reserved

Register 20h HcControlHeadED Register

Default Value: 00000000h

Access: Read/Write

The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list.

Bit	Access	Description
31:4	R/W	ControlHeadED HC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0		Reserved.

Register 24h HcControlCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcControlCurrentED register contains the physical address of the current Endpoint Descriptor of the Control list.

Bit	Access	Description
31:4	R/W	ControlCurrentED This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3:0		Reserved.

Register 28h HcBulkHeadED Register

Default Value: 00000000h

Access: Read/Write

The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list.

Bit	Access	Description
31:4	R/W	BulkHeadED HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.

3:0		Reserved.

Register 2Ch HcBulkCurrentED Register

Default Value: 00000000h

Access: Read/Write

The HcBulkCurrentED register contains the physical address of the current endpoint of the Bulk list. As the Bulk list will be served in a round-robin fashion, the endpoints will be ordered according to their insertion to the list.

Bit	Access	Description
31:4	R/W	BulkCurrentED This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3:0		Reserved.

Register 30h HcDoneHead Register

Default Value: 00000000h

Access: Read/Write

The HcDoneHead register contains the physical address of the last completed Transfer Descriptor that was added to the Done queue. In normal operation, the Host Controller Driver should not need to read this register as its content is periodically written to the HCCA.

Bit	Access	Description
31:4	R/W	DoneHead When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
3:0		Reserved

4.2.4. Frame Counter Partition

Register 34h HcFmInterval Register

Default Value: 00002EDFh

Access: Read/Write

The HcFmInterval register contains a 14-bit value which indicates the bit time interval in a Frame, (i.e., between two consecutive SOFs), and a 15-bit value indicating the Full Speed maximum packet size that the Host Controller may transmit or receive without causing scheduling overrun. The Host Controller Driver may carry out minor adjustment on the FrameInterval by writing a new value over the present one at each SOF. This provides the programmability necessary for the Host Controller to synchronize with an external clocking resource and to adjust any unknown local clock offset.

Bit	Access	Description
31	R/W	FrameIntervalToggle HCD toggles this bit whenever it loads a new value to FrameInterval.
30:16	R/W	FSLargestDataPacket This field specifies a value that is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.
15:14		Reserved
13:0	R/W	FrameInterval This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

Register 38h HcFmRemaining Register

Default Value: 00000000h

Access: Read Only

The HcFmRemaining register is a 14-bit down counter showing the bit time remaining in the current Frame.

Bit	Access	Description
31	RO	FrameRemainingToggle This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14		Reserved
13:0	RO	FrameRemaining This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the UsbOperational state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.

Register 3Ch HcFmNumber Register

Default Value: 00000000h

Access: Read

The HcFmNumber register is a 16-bit counter. It provides a timing reference among events occurring in the Host Controller and the Host Controller Driver. The Host Controller Driver may use the 16-bit value specified in this register and generate a 32-bit frame number without requiring frequent access to the register.

Bit	Access	Description
31:16		Reserved
15:0	RO	FrameNumber This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after ffffh. When entering the UsbOperational state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.

Register 40h HcPeriodicStart Register

Default Value: 00000000h

Access: Read/Write

The HcPeriodicStart register has a 14-bit programmable value that determines when is the earliest time HC should start processing the periodic list.

Bit	Access	Description
31:14		Reserved

13:0	R/W	PeriodicStart After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

Register 44h HcLSThreshold Register

Default Value: 00000000h

Access: Read/Write

The HcLSThreshold register contains an 11-bit value used by the Host Controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before EOF. Neither the Host Controller nor the Host Controller Driver is allowed to change this value.

Bit	Access	Description
31:12		Reserved
11:0	R/W	LSThreshold This field contains a value that is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ≥ this field. The value is calculated by HCD with the consideration of transmission and set-up overhead.

4.2.5. Root Hub Partition

All registers included in this partition are dedicated to the USB Root Hub which is an integral part of the Host Controller though still a functionally separate entity. The HCD emulates USBD accesses to the Root Hub via a register interface. The HCD maintains many USB-defined hub features that are not required to be supported in hardware. For example, the Hub's Device, Configuration, Interface, and Endpoint Descriptors are maintained only in the HCD as well as some static fields of the Class Descriptor. The HCD also maintains and decodes the Root Hub's device address as well as other trivial operations that are better suited to software than hardware.

The Root Hub register interface is otherwise developed to maintain similarity of bit organization and operation to typical hubs that are found in the system. Below

are four register definitions: HcRhDescriptorA, HcRhDescriptorB, HcRhStatus, and HcRhPortStatus [5:1]. Each register is read and written as a Dword. These registers are only written during initialization to correspond with the system implementation. The HcRhDescriptorA and HcRhDescriptorB registers should be implemented such that they are writable regardless of the HC USB state. HcRhStatus and HcRhPortStatus must be writable during the UsbOperational state.

Register 48h HcRhDescriptorA Register

Default Value: 01000003h

Access: Read/Write

The HcRhDescriptorA register is the first register of two describing characteristics of the Root Hub. Reset values are implementation-specific. All other fields are located in the HcRhDescriptorA and HcRhDescriptorB registers.

Bit	Access	Description
31:24	R/W	PowerOnToPowerGoodTime This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2 ms.
23: 13		Reserved
12	R/W	NoOverCurrentProtection This bit describes how the overcurrent status for the Root Hub ports is reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0 : Over-current status is reported collectively for all downstream ports 1 : No overcurrent protection supported
11	R/W	OverCurrentProtectionMode This bit describes how the overcurrent status for the Root Hub ports is reported. At reset, this field should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared. 0 : over-current status is reported collectively for all downstream ports 1 : over-current status is reported on a per-port basis
10	RO	DeviceType This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.

<table>
<tr><td>9</td><td>R/W</td><td>NoPowerSwitching
These bits are used to specify whether power switching is supported or ports are always powered. SiS961A USB HC supports global power switching mode. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching.
0 : Ports are power switched
1 : Ports are always powered on when the HC is powered on</td></tr>
<tr><td>8</td><td>R/W</td><td>PowerSwitchingMode
This bit is used to specify how the power switching of the Root Hub ports is controlled. SiS961A USB HC supports global power switching mode. This field is only valid if the NoPowerSwitching field is cleared.
0: all ports are powered at the same time.
1: Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching.
If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ Clear Global Power).</td></tr>
<tr><td>7:0</td><td>RO</td><td>NumberDownstreamPorts
These bits specify the number of downstream ports supported by the Root Hub.
Both of the HC support three downstream ports.

In A version it can be programmed to 02h or 01h, HC0 is controlled by SB CFG 6C bit 0,1 and HC1 is controlled by SB CFG 6C bit 2,3. The setting is tabulated below
<table>
<tr><td>NDP’s value</td><td>SB CFG 6C bit0 or bit2</td><td>SB CFG 6C bit1 or bit3</td></tr>
<tr><td>01h</td><td>1</td><td>X</td></tr>
<tr><td>02h</td><td>0</td><td>1</td></tr>
<tr><td>03h</td><td>0</td><td>0</td></tr>
</table></td></tr>
</table>

Register 4Ch HcRhDescriptorB Register

Default Value: 00000000h

Access: Read/Write

The HcRhDescriptorB register is the second register of two describing the characteristics of the Root Hub. These fields are written during initialization to configure the Root Hub.

Bit	Access	Description
31:16	R/W	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid. SiS968USB HC implements global power switching. bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2 ... bit15: Ganged-power mask on Port #15
15:0	R/W	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2 ... bit15: Device attached to Port #15

Register 50h HcRhStatus Register

Default Value: 00000000h

Access: Read/Write

The HcRhStatus register is divided into two parts. The lower word of a Dword represents the Hub Status field and the upper word represents the Hub Status Change field. Reserved bits should always be written '0'.

Bit	Access	Description
31	WO	ClearRemoteWakeupEnable(Write) Writing a '1' clears DeviceRemoveWakeupEnable. Writing a '0' has no effect.
30:18		Reserved

17	R/W	OverCurrentIndicatorChange This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a '1'.Writing a '0' has no effect.
16	R/W	LocalPowerStatusChange(Read) The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. SetGlobalPower(Write) In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.
15	R/W	DeviceRemoteWakeupEnable(Read) This bit enables a ConnectStatusChange bit as a resume event, causing a UsbSuspend to UsbResume state transition and setting the ResumeDetected interrupt. 0 : **ConnectStatusChange** is not a remote wakeup event. 1 : **ConnectStatusChange** is a remote wakeup event. SetRemoteWakeupEnable(Write) Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.
14:2		Reserved
1	RO	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'
0	R/W	LocalPowerStatus((Read)) The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. ClearGlobalPower(Write) In global power mode (PowerSwitchingMode=0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.

Register 54h/58h/5Ch HcRhPortStatus [3:1] Register

Default Value: 00000000h

Access: Read/Write

The HcRhPortStatus[3:1] register is used to control and report port events on a per-port basis. Three or two HcRhPortStatus registers are implemented in each HC, respectively. The lower word is used to reflect the port status, whereas the upper word reflects the status change bits. Some status bits are implemented with special write behaviour (see below). If a transaction (token through handshake) is in progress when a write to change port status occurs, the resulting port status change must be postponed until the transaction completed. Reserved bits should always be written '0'. While the NDP of register 48h is 01h, the register 58 and register 5C will be read as 00000000h. While the NDP of register 48h is 02h, only register 5C is read as 00000000h.

Bit	Access	Description
31:21		Reserved
20	R/W	PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : port reset is not complete 1 : port reset is complete
19	R/W	PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : no change in PortOverCurrentIndicator 1 : PortOverCurrentIndicator has changed
18	R/W	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resynchronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0 : resume is not completed 1 : resume completed

17	R/W	PortEnableStatusChange This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0 : no change in **PortEnableStatus** 1 : change in PortEnableStatus
16	R/W	ConnectStatusChange This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0 : no change in CurrentConnectStatus 1 : change in CurrentConnectStatus Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15:10		Reserved
9	R/W	LowSpeedDeviceAttached((Read)) This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0 : full speed device attached 1 : low speed device attached

8	R/W	Port Power Status((Read)) This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing Set Port Power or Set Global Power. HCD clears this bit by writing Clear Port Power or Clear Global Power. Which power control switches will be enabled is determined by Power Switching Mode and Port Power Control Mask[NDP]. In global switching mode (Power Switching Mode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (Power Switching Mode=1), if the Port Power Control Mask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ Clear Global Power commands are enabled. When port power is disabled, Current Connect Status, Port Enable Status, Port Suspend Status, and Port Reset Status should be reset. 0 : port power is off 1 : port power is on SetPortPower(Write) The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect. Note: This bit is always reads '1b' if power switching is not supported.
7:5		Reserved
4	R/W	PortResetStatus(Read) When this bit is set by a write to SetPortReset, port reset signalling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0 : port reset signal is not active 1 : port reset signal is active SetPortReset(Write) The HCD sets the port reset signalling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.

3	R/W	PortOverCurrentIndicator(Read) This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal 0 : no overcurrent condition. 1 : overcurrent condition detected. ClearSuspendStatus(Write) The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.
2	R/W	PortSuspendStatus(Read) This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the UsbResume state. If an upstream resume is in progress, it should propagate to the HC. 0 : port is not suspended 1 : port is suspended SetPortSuspend(Write) The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.

1	R/W	PortEnableStatus(Read) This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0 : port is disabled 1 : port is enabled SetPortEnable(Write) The HCD sets PortEnableStatus by writing a '1'.Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.
0	R/W	CurrentConnectStatus(Read) This bit reflects the current state of the downstream port. 0 : no device connected 1 : device connected ClearPortEnable(Write) The HCD writes a '1' to this bit to clear the PortEnableStatus bit. Writing a '0' has no effect. The CurrentConnectStatus is not affected by any write. Note: This bit is always read '1b' when the attached device is nonremovable (DeviceRemoveable[NDP]).

4.2.6. Legacy Support Registers

Four operational registers are used to provide the legacy support. Each of these registers is located on a 32-bit boundary. The offset of these registers is relative to the base address of the Host Controller operational registers with HceControl located at offset 100h.

Table 4 Legacy Support Registers

Offset	Register	Description

100h	HceControl	Used to enable and control the emulation hardware and report various status informations.
104h	HceInput	Emulation side of the legacy Input Buffer register.
108h	HceOutput	Emulation side of the legacy Output Buffer register where keyboard and mouse data is to be written by software.
10Ch	HceStatus	Emulation side of the legacy Status register.

Three of the operational registers (HceStatus, HceInput, HceOutput) are accessible at I/O address 60h and 64h when emulation is enabled. Reads and writes to the registers using I/O addresses have side effects as outlined in the Table 4.

Table 5 Emulated Registers

I/O Address	Cycle Type	Register Contents Accessed/Modified	Side Effects
60h	IN	HceOutput	IN from port 60h will set OutputFull in HceStatus to 0
60h	OUT	HceInput	OUT to port 60h will set InputFull to 1 and CmdData to 0 in HceStatus.
64h	IN	HceStatus	IN from port 64h returns current value of HceStatus with no other side effect.
64h	OUT	HceInput	OUT to port 64h will set InputFull to 0 and CmdData in HceStatus to 1.

Register 100h HceControl Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:9		Reserved
8	R/W	A20State Indicates current state of Gate A20 on keyboard controller. Used to compare value to 60h when GateA20Sequence is active.
7	R/W	IRQ12Active Indicates that a positive transition on IRQ12 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.

6	R/W	IRQ1Active Indicates that a positive transition on IRQ1 from keyboard controller has occurred. SW may write a 1 to this bit to clear it (set it to 0). SW write of a 0 to this bit has no effect.
5	R/W	GateA20Sequence Set by HC when a data value of D1h is written to I/O port 64h. Cleared by HC on write to I/O port 64h of any value other than D1h.
4	R/W	ExternalIRQEn When set to 1, IRQ1 and IRQ12 from the keyboard controller causes an emulation interrupt. The function controlled by this bit is independent of the setting of the **EmulationEnable** bit in this register.
3	R/W	IRQEn When set, the HC generates IRQ1 or IRQ12 as long as the **OutputFull** bit in *HceStatus* is set to 1. If the **AuxOutputFull** bit of *HceStatus* is 0, then IRQ1 is generated; if it is 1, then an IRQ12 is generated.
2	R/W	CharacterPending When set, an emulation interrupt is generated when the **OutputFull** bit of the *HceStatus* register is set to 0.
1	RO	EmulationInterrupt This bit is a static decode of the emulation interrupt condition
0	R/W	EmulationEnable When set to 1, the HC is enabled for legacy emulation. The HC decodes accesses to I/O registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generates an emulation interrupt at appropriate times to invoke the emulation software.

Register 104h HceInput Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:8		Reserved

7:0	R/W	InputData This register holds data that is written to I/O ports 60h and 64h. I/O data that is written to ports 60h and 64h is captured in this register when emulation is enabled. This register may be read or written directly by accessing it with its memory address in the Host Controller's operational register space. When accessed directly with a memory cycle, reads and writes of this register have no side effects.

Register 108h HceOutput Register

Default Value: 00000000h

Access: Read/write

Bit	Access	Description
31:8		Reserved
7:0	R/W	OutputData This register hosts data that is returned when an I/O read of port 60h is performed by application software. The data placed in this register by the emulation software is returned when I/O port 60h is read and emulation is enabled. On a read of this location, the OutputFull bit in HceStatus is set to 0.

Register 10Ch HceStatus Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:8		Reserved
7	R/W	Parity Indicates parity error on keyboard/mouse data.
6	R/W	Time-out Used to indicate a time-out
5	R/W	AuxOutputFull IRQ12 is asserted whenever this bit is set to 1 and **OutputFull** is set to 1 and the **IRQEn** bit is set.
4	R/W	Inhibit Switch This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.

3	R/W	CmdData The HC sets this bit to 0 on an I/O write to port 60h and to 1 on an I/O write to port 64h
2	R/W	Flag Nominally used as a system flag by software to indicate a warm or cold boot.
1	R/W	InputFull Except for the case of a Gate A20 sequence, this bit is set to 1 on an I/O write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0	R/W	OutputFull The HC sets this bit to 0 on a read of I/O port 60h. If **IRQEn** is set and **AuxOutputFull** is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If **IRQEn** is set and **AuxOutputFull** is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and **CharacterPending** in *HceControl* is set to 1, an emulation interrupt condition exists. The contents of the *HceStatus* Register are returned on an I/O Read of port 64h when emulation is enabled. Reads and writes of port 60h and writes to port 64h can cause changes in this register. Emulation software can directly access this register through its memory address in the Host Controller's operational register space. Accessing this register through its memory address produces no side effects.

4.3. EHC3 Configuration Space

4.3.1. USB2.0 Configuration Space

Configuration. Offset	Access	Mnemonic Register
00-01h	RO	Vendor ID
02-03h	RO	Device ID
04-05h	R/W	Command Register
06-07h	R/W	Status register
08h	RO	Revision ID
09-0Bh	RO	Class Code

0Ch	RO	Cache Line Size
0Dh	R/W	Master Latency Timer
0Eh	RO	Header Type
0Fh	RO	Built-in Self Test
10-13h	R/W	Base address
14-2Bh	RO	Reserved
2C-2Dh	R/WS	Subsystem Vendor ID
2E-2Fh	R/WS	Subsystem ID
34h	RO	Capabilities Pointer
35-3Bh	RO	Reserved
3Ch	R/W	Interrupt line
3Dh	R/WS	Interrupt pin
3Eh	R/WS	Minimum Grant
3Fh	R/WS	Maximum Latency
40h-43h	R/W	Operational Mode1 Enable Register
44h-47h	R/W	Operational Mode2 Enable Register
48h-4Bh	R/W	Operational Mode3 Enable Register
50h	RO	Power Management Capability ID
51h	RO	Next Item Pointer #1
52-53h	RO	Power Management Capabilities
54h-55h	R/W	Power Management Control/Status
58h	RO	Debug Port Capability ID
59h	RO	Next Item Pointer #2
5Ah-5Bh	RO	Debug Port Base Offset
60h	RO	USB Release Number
61h	R/W	Frame Length Adjustment
62-63h	R/W	Power Wake Capabilities
64-65h	R/W	USB1.1 Port Override
70-73h	R/W	Legacy Support Extended Capability
74-77h	R/W	Legacy Support Control/Status
78-7B	R/W	Legacy Support Enable/Status

Vender ID Register

Register 00-01h Vender ID

Default Value: 1039h

Access: Read

Bit	Access	Description
15:0	RO	Vendor ID

Device ID Register

Register 02-03h Device ID

Default Value: 7002h

Access: Read

Bit	Access	Description
15:0	RO	Device ID

Command Register

Register 04-05h Command Register

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:11	R/W	Reserved Bits These bits are always 0.
10	R/W	This bit disables the device from asserting **INTx#**.
9	R/W	Reserved Bits This bit is always 0
8	R/W	SERR#(Response) Detection Enable bit If set to 1, EHC asserts SERR# when it detects an address parity error. SERR# is not asserted if this bit is 0.
7:3	RO	Reserved Bits These bits are always 0.
2	R/W	PCI Master Enable If set to 1, EHC is enabled to run PCI master cycles.
1	R/W	Memory Enable If set to 1, EHC is enabled to respond as a target to memory cycles.
0	RO	I/O Enable This bit is always 0.

Status Register

Register 06-07h Status Register

Default Value: 0290h

Access: Read/Write

Bit	Access	Description
15	RO	Detected Parity Error This bit is always 0.
14	R/W	SERR# Status This bit is set to 1 whenever the EHC detects a PCI address parity error. Cleared by writing a 1 to it.
13	R/W	Received Master Abort Status This bit is set to 1 when EHC receives a master-abort status on a PCI bus memory cycle. Cleared by writing a 1 to it.
12	R/W	Received Target Abort Status This bit is set to 1 when EHC receives a target-abort status on a PCI bus memory cycle. Cleared by writing a 1 to it.
11	R/W	Signalled Target Abort Status This bit is set to 1 when EHC responds to a memory cycle with a target abort. Cleared by writing a 1 to it.
10-9	RO	DEVSEL# timing Read only bits indicating DEVSEL# timing when performing a positive decode. Since DEVSEL# is asserted to meet the medium timing, these bits are encoded as 01b.
8	R/W	Data Parity Reported Set to 1 if the Parity Error Response bit is set, and EHC detects PERR# asserted while acting as PCI master (whether PERR# was driven by EHC or not).
7	R/O	Fast back to back permitted This bit is always 1.
6-5	R/O	Reserved Bits These bits are always 0.
4	R/O	PMCSR capability support This bit is always 1.
3	R/O	Interrupt Status This bit reflects the state of the interrupt in the device.
2-0	R/W	Reserved Bits These bits are always 0

Revision ID Register

Register 08h Revision ID Register

Default Value: 00h

Access: Read

Bit	Access	Description
7:0	RO	Functional Revision Level

Class Code Register

Register 09-0Bh Class Code Register

Default Value: 0C0320h

Access: Read

Bit	Access	Description
23:16	RO	Base Class The Base Class is 0Ch (Serial Bus Controller).
15:8	RO	Sub Class The Sub Class is 03h (Universal Serial Bus).
7:0	RO	Programming Interface The Programming Interface is 20h (USB2.0).

Cache Line Size

Register 0Ch Cache Line Size

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	Cache Line Size This register identifies the system cache line size in units of 32-bit words. EHC will only store the value of bit 3 in this register since the cacheline size of 32 bytes is the only value applicable to the design. Any value other than 08h written to this register will be read back as 00h.

Latency Timer

Register 0Dh Latency Timer

Default Value: 00h

Access: Read/Write

Bit	Access	Description

7:0	R/W	Latency Timer This register identifies the value of the latency timer in PCI clocks for PCI bus master cycles.

Header Type Register

Register 0Eh Header Type Register

Default Value: 00h

Access: Read

Bit	Access	Description
7:0	RO	Header Type Register This register identifies the type of the predefined header in the configuration space. Since EHC is a single function device and not a PCI-to-PCI bridge, the byte should be read as 00h.

BIST

Register 0Fh BIST

Default Value: 00h

Access: Read

Bit	Access	Description
7:0	RO	BIST This register identifies the control and status of Built-In-Self-Test. EHC does not implement BIST, so this register is read only.

Base Address Register

Register 10-13h Base Address Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:12	R/W	Base Address POST writes the value of the memory base address to this register.
11:0	RO	Always 0.

Subsystem Vender ID Register

Register 2C-2Dh Subsystem Vender ID

Default Value: 1039h

Access: Read/Write Special

Bit	Access	Description
15:0	R/WS	Subsystem Vendor ID BIOS set the value in this field to identify the subsystem vendor ID. Before writing to this field, BIOS must disable write-protect bits in register 40h bit 1:0.

Subsystem ID Register

Register 2E-2Fh Subsystem ID

Default Value: 7002h

Access: Read/Write Special

Bit	Access	Description
15:0	R/WS	Subsystem ID BIOS set the value in this field to identify the subsystem ID. Before writing to this field, BIOS must disable write-protect bits in register 40h bit 1:0.

Capabilities Pointer Register

Register 34h Capabilities Pointer

Default Value: 50h

Access: Read

Bit	Access	Description
7:0	RO	Capabilities Pointer This register points to the starting offset of the USB2.0 capability registers.

Interrupt Line Register

Register 3Ch Interrupt Line Register

Default Value: 00h

Access: Read/Write

Bit	Access	Description
7:0	R/W	Interrupt Line This register identifies the interrupt line that EHC interrupt pin is connected to. The value of this register is used by device drivers and has no direct meaning to EHC.

Interrupt Pin Register

Register 3Dh Interrupt Pin Register

Default Value: 04h

Access: Read/Write Special

Bit	Access	Description
7:0	R/WS	Interrupt Pin This register identifies the interrupt pin that EHC uses. Since EHC uses INTD#, this value is set to 04h.

Minimum Grant Register

Register 3Eh Minimum Grant Register

Default Value: 00h

Access: Read/Write Special

Bit	Access	Description
7:0	R/WS	Minimum Grant This register specifies the desired settings for how long of a burst EHC needs assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Maximum Latency Register

Register 3Fh Maximum Latency Register

Default Value: 50h

Access: Read/Write Special

Bit	Access	Description
7:0	R/WS	Maximum Latency This register specifies the desired setting for how often EHC needs access to the PCI bus assuming a clock rate of 33 MHz. The value specifies a period of time in units of 1/4 microsecond.

Operational Mode Enable Register

Register 40-43h Operational Mode Enable Register

Default Value: 00000000h

Recommended Value : 00004080h

Access: Read/Write

Bit	Access	Description
31	R/W	Reserved
30:28	R/W	Reserved
27	R/W	Reserved
26:	R/W	Reserved
25:24	R/W	Reserved These bits should always 0.

23	R/W	Reserved
22	R/W	Reserved
21	R/W	Reserved
20:16	R/W	Reserved
15	R/W	Reserved
14	R/W	Reserved
13	R/W	Reserved
12	R/W	Reserved
11:10	R/W	Reserved
9	R/W	Reserved
8	R/W	Reserved
7:5	R/W	Reserved
4	R/W	Reserved
3	R/W	Reserved
2	R/W	Reserved
1:0	R/W	Reserved

Register 44-47h Operational Mode2 Enable Register

Default Value: 00000000h

Recommended Value : 8177CD80h

Access: Read/Write

Bit	Access	Description
31	R/W	Reserved
30:29	R/W	Reserved
28	R/W	Reserved
27	R/W	Reserved
26:25	R/W	Reserved
24	R/W	Reserved
23	R/W	Reserved
22	R/W	Reserved
21:20	R/W	Reserved
19	R/W	Reserved
18	R/W	Reserved
17	R/W	Reserved
16	R/W	Reserved
15	R/W	Reserved

14	R/W	Reserved
13:12	R/W	Reserved
11:10	R/W	Reserved
9:8	R/W	Reserved
7	R/W	Reserved
6	R/W	Reserved
5	R/W	Reserved
4	R/W	Reserved
3:2	R/W	Reserved
1:0	R/W	Reserved

Register 48-4Bh Operational Mode3 Enable Register

Default Value: 00000000h

Recommended Value : 00078000h

Access: Read/Write

Bit	Access	Description
31:15	R/W	Reserved
14	R/W	**Reserved**
13	R/W	Reserved
12:11	R/W	**Reserved**
10:8	R/W	Reserved
7	R/W	Reserved
6:4	R/W	Reserved
3:2	R/W	Reserved
1	R/W	Reserved
0	R/W	Reserved

PCI Power Management Capability ID

Register 50h Power Management Capability ID Register

Default Value: 01h

Access: Read

Bit	Access	Description
7:0	RO	Power management capability ID A value of 01h indicates that this is a PCI power management capability field.

Next Item Pointer #1

Register 51h Next Item Pointer Register

Default Value: 00h/58h

Access: Read

Bit	Access	Description
7:0	RO	Next Item Pointer When debug port is enabled, this register will be read as 58h to point to the next capability registers.

Power Management Capabilities

Register 52-53h Power Management Capabilities Register

Default Value: C9C2h

Access: Read

Bit	Access	Description
15:11	RO	PME Support These registers specify the power states in which the function may assert PME#. The EHC does not support the D1 or D2 states.
10	RO	D2 Support The EHC does not support D2 state.
9	RO	D1 Support The EHC does not support D2 state.
8:6	RO	Aux Current The EHC reports 375mA maximum current required when in D3Cold state.
5:3	RO	Reserved These bits are always 0.
2:0	RO	Version The EHC reports 010b to indicate that it complies with PCI Power Management Spec Revision 1.1.

Power Management Control/Status

Register 54-55h Power Management Control/Status Register

Default Value: 0000h

Access: Read/Write

Bit	Access	Description

15	R/WC	PME Status This bit is set when the EHC asserts the PME#. Writing a 1 to this bit will clear it and cause the PME# to dessert.
14:9	RO	Reserved These bits are always 0.
8	R/W	PME enable A 1 in this bit enables the EHC to generate PME#.
7:2	RO	Reserved These bits are always 0.
1:0	R/W	Power State These bits control the power state for the EHC. The EHC only supports D0 and D3 state. Writing other value to this field will cause undefined behavior.

Debug Port Capability ID

Register 58h Debug Port Capability ID Register

Default Value: 0Ah

Access: Read

Bit	Access	Description
7:0	RO	Debug Port capability ID A value of 0Ah indicates that this is a PCI power management capability field.

Next Item Pointer #2

Register 51h Next Item Pointer Register

Default Value: 00h

Access: Read

Bit	Access	Description
7:0	RO	Next Item Pointer This register is hardwired to 00h to indicate the last capability in this function.

Debug Port Base Offset

Register 5A-5Bh Debug Port Base Offset Register

Default Value: 2100h

Access: Read

Bit	Access	Description

15:13	RO	Debug Port BAR Number This register is hardwired to 001h to indicate the memory base address begins at offset 10h in the EHC configuration space.
12:0	RO	Debug Port Offset This register is hardwired to 100h to indicate the debug port registers begin at offset 100h in the EHC memory range.

USB Release Number

Register 60h USB Release Number Register

Default Value: 20h

Access: Read

Bit	Access	Description
7:0	RO	USB Release Number This register is hardwired to 20h to indicate the EHC follows USB 2.0 Spec.

Frame Length Adjustment

Register 61h Frame Length Adjustment Register

Default Value: 20h

Access: Read/Write

Bit	Access	Description
7:6	RO	Reserved These registers are always 0.
5:0	R/W	Frame Length Timing Value Each decimal value change to this register corresponds to 16 bit times for high speed bus.

Port Wake Capability

Register 62-63h Port Wake Capability Register

Default Value: 01FFh

Access: Read/Write

Bit	Access	Description
15:9	RO	Reserved These registers are always 0.

8:1	R/W	Port Wake Up Capability Mask Bit positions 1 through 8 correspond to a physical port implemented on this host controller. A one in a bit position indicates that a device connected below the port can be enabled as a wake-up device.
0	R/W	Port Wake Implemented A one in this bit indicates whether the register is implemented.

USB1.1 Port Override

Register 64-65h USB1.1 Port Override Register

Default Value: 0000h

Access: Read/Write

Bit	Access	Description
15:8	RO	Reserved These registers are always 0.
7:1	R/W	USB1.1 Port7-1 Owner Bit positions 1 through 5 correspond to a physical port implemented on this host controller. A one in a bit position indicates that a device connected below the port will always be routed to USB1.1 host controller.
0	RO	USB1.1 Port 0 Owner Port 0 for the EHC must never be programmed to the USB1.1 because this port is used as debug port.

USBLEGSUP

Register 70-73h USB Legacy Support Extended Capability Register

Default Value: 00000001h

Access: Read/Write

Bit	Access	Description
31:25	RO	Reserved These registers are always 0.
24	R/W	HC OS Owned Semaphore System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as one and the HC BIOS Owned Semaphore bit read as zero.
23:17	RO	Reserved These registers are always 0.

16	R/W	HC BIOS Owned Semaphore The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will set this bit to a zero in response to a request for ownership of the EHCI controller by system software.
15:8	RO	Next EHCI Extended Capability Pointer A value of 00h indicates the end of the extended capability list.
7:0	RO	Capability ID A value of 01h identifies the capability as Legacy Support.

USBLEGCTLSTS

Register 74-77h USB Legacy Support Control/Status Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31	R/WC	SMI on BAR This bit is set to one whenever the Base Address Register (BAR) is written.
30	R/WC	SMI on PCI Command This bit is set to one whenever the PCI Command Register is written.
29	R/WC	SMI on OS Ownership Change This bit is set to one whenever the HC OS Owned Semaphore bit in the USBLEGSUP register changes.
28:22	RO	Reserved These registers are always 0.
21	RO	SMI on Async Advance Shadow bit of the Interrupt on Async Advance bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
20	RO	SMI on Host System Error Shadow bit of Host System Error bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
19	RO	SMI on Frame List Rollover Shadow bit of Frame List Rollover bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.

18	RO	SMI on Port Change Detect Shadow bit of Port Chance Detect bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
17	RO	SMI on USB Error Shadow bit of USB Error Interrupt (USBERRINT) bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
16	RO	SMI on USB Complete Shadow bit of USB Interrupt (USBINT) bit in the USBSTS register. Software must write 1 to the corresponding bit in USBSTS to clear this bit.
15	R/W	SMI on BAR Enable
14	R/W	SMI on PCI Command Enable
13	R/W	SMI on OS Ownership Change Enable
12:6	RO	Reserved These registers are always 0.
5	R/W	SMI on Async Advance Enable
4	R/W	SMI on Host System Error Enable
3	R/W	SMI on Frame List Rollover Enable
2	R/W	SMI on Port Change Detect Enable
1	R/W	SMI on USB Error Enable
0	R/W	SMI on USB Complete Enable

USBLEGENSTS

Register 78-7Bh USB Legacy Support Enable/Status Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:30	RO	Reserved These registers are always 0.
29:22	R/WC	Legacy port 8-1 owner Change Bit positions 22 through 29 correspond to a physical port on this host controller. A one in a bit position indicates that a device owner changed
21	R/WC	PMCS Change This bit is set to one whenever the PMCS changed

20	R/WC	Asynchronous Schedule Enable Change This bit is set to one whenever the Asynchronous Schedule Enable bit changed.
19	R/WC	Periodic Schedule Enable Change This bit is set to one whenever the Peridic Schedule Enable bit changed.
18	R/WC	Configure Flag Change This bit is set to one whenever the Configure Flag bit changed.
17	R/WC	HCHalted Change This bit goes to one whenever the HCHalted register makes a 0b to 1b transition.
16	R/WC	HCRESET Change This bit goes to one whenever the HCRESET register makes a 0b to 1b transition.
15:14	RO	Reserved These registers are always 0.
13:6	R/W	Legacy port 7-0 owner Change Enable
5	R/W	PMCS Change Enable
4	R/W	Asynchronous Schedule Enable Change Enable
3	R/W	Periodic Schedule Enable Change Enable
2	R/W	Configure Flag Change Enable
1	R/W	HCHalted Change Enable
0	R/W	HCRESET Change Enable

4.4. EHC3 Operational Registers

The base address of these registers is programmable by the memory base address register (EHC PCI configuration register offset 10-13h). These registers should be written as DWORD. Bytes access to these registers may have unpredictable effects.

4.4.1. EHC3 Operational Registers

Offset	Mnemonic	Power Well	Register Name
00h	CAPLENGTH	Core	Capability Register Length

01h	Reserved	Core	N/A
02-03h	HCIVERSION	Core	Interface Version Number
04-07h	HCSPARAMS	Core	Structural Parameters
08-0Bh	HCCPARAMS	Core	Capability Parameters
0C-1Fh	Reserved	Core	N/A
20-23h	USB2CMD	Core	USB2.0 Command
24-27h	USB2STS	Core	USB2.0 Status
28-2Bh	USB2INTR	Core	USB2.0 Interrupt Enable
2C-2Fh	FRINDEX	Core	USB2.0 Frame Index
30-33h	Reserved	Core	N/A
34-37h	PERIODICLISTBASE	Core	Frame List Base Address
38-3Bh	ASYNCLISTADDR	Core	Next Asynchronous List Address
3C-3Fh	Reserved	Core	N/A
60-63h	CONFIGFLAG	Aux	Configured Flag Register
64-83h	PORTSC(0-7)	Aux	Port Status/Control
100-103h	DBGPORTSC	Core	Debug Port Control/Status
104-107h	DBGUSBPID	Core	Debug Port USB PIDs
108-10Bh	DBGDBL	Core	Debug Port Data Buffer Low
10C-10Fh	DBGDBH	Core	Debug Port Data Buffer High
110-113h	DBGDA	Core	Debug Port Device Address

Host Controller Capability Register

Offset 00h CAPLENGTH – Capability Registers Length

Default Value: 20h

Access: Read

Bit	Access	Description
7:0	RO	Capability Register Length This register indicates to the length of the host controller capability registers.

Offset 02-03h HCIVERSION – Host Controller Interface Version Number

Default Value: 0100h

Access: Read

Bit	Access	Description

15:0	RO	Host Controller Interface Version Number This register indicates the EHC support the EHCI Spec Revision 1.0.

Offset 04-07h HCSPARAMS – Structure Parameters

Default Value: 0010<u>24</u>08h

Access: Read

Bit	Access	Description
31:24	RO	Reserved These registers are always 0.
23:20	RO	Debug Port Number This register identifies the first port as the debug port.
19:16	RO	Reserved These registers are always 0.
15:12	RO	Number of Companion Controller (N_CC) This field indicates the number of companion controllers associated with this USB2.0 host controller.
11:8	RO	Number of Ports per Companion Controller (N_PCC) This field indicates the number of ports supported per companion host controller.
7:4	RO	Reserved These registers are always 0.
3:0	RO	Number of Ports (N_PORTS) This field indicates the number of ports supported on this host controller.

Offset 08-0Bh HCCPARAMS – Capability Parameters

Default Value: 00<u>00</u>7<u>0</u>70h

Access: Read

Bit	Access	Description
31:16	RO	Reserved These registers are always 0.
15:8	RO	EHCI Extend Capabilities Pointer (EECP) This field indicates the existence of a capability list.
7:4	R/WS	Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliable update the isochronous schedule.

3	RO	Reserved This register is always 0.
2	R/WS	Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule.
1:0	RO	Reserved These registers are always 0.

Host Controller Operational Register

Offset 20-23h USB2CMD – USB2.0 Command Register

Default Value: 00080000h

Access: Read/Write

Bit	Access	Description
31:24	RO	Reserved These registers are always 0.
23:16	R/W	Interrupt Threshold Control This field is used by system software to select the maximum rate at which the host controller will issue interrupt.
15:12	RO	Reserved These registers are always 0.
11	R/W	Asynchronous Schedule Park Mode Enable If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1h and is R/W. Software uses this bit to enable or disable Park mode.
10	RO	Reserved This register is always 0.
9:8	R/W	Asynchronous Schedule Park Mode Count If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 3h and is R/W. This field contains a count to the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule before continuing traversal of the asynchronous schedule.
7	R/W	Light Host Controller Reset It allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controllers.

6	R/W	Interrupt on Async Advance Doorbell This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule.
5	R/W	Asynchronous Schedule Enable This bit controls whether the host controller skips processing the Asynchronous Schedule.
4	R/W	Periodic Schedule Enable This bit controls whether the host controller skips processing the Periodic Schedule.
3:2	RO	Reserved These registers are always 0.
1	R/W	Host Controller Reset (HCRESET) This control bit is used by software to reset the host controller.
0	R/W	Run/Stop (RS) When set to a 1, the host controller proceeds with execution of the schedule.

Offset 24-27h USB2STS – USB2.0 Status Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:16	RO	Reserved These registers are always 0.
15	RO	Asynchronous Schedule Status This bit reports the current real status of the Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disable.
14	RO	Periodic Schedule Status This bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disable.
13	RO	Reclamation This bit is used to detect an empty asynchronous schedule.

12	RO	Host Controller Halted (HCHalted) This bit is a zero whenever the Run/Stop bit is a one. The Host Controller sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller hardware.
11:6	RO	Reserved These registers are always 0.
5	R/WC	Interrupt on Async Advance System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USB2CMD register.
4	R/WC	Host System Error The Host Controller sets this bit to 1 when a serious error occurs during a host system access involving the Host Controller module.
3	R/WC	Frame List Rollover The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero.
2	R/WC	Port Change Detect The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transaction detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to a one after system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	USB Error Interrupt (USBERRINT) The Host Controller sets this bit to 1 when completion of a USB transaction results in an error condition.
0	R/WC	USB Interrupt (USBINT) The Host Controller sets this bit to 1 one the completion of a USB transaction, which result in the retirement of a Transfer Descriptor that had its IOC bit set.

Offset 28-2Ch USB2INTR – USB2.0 Interrupt Enable Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description

31:6	RO	Reserved These registers are always 0.
5	R/W	Interrupt on Async Advance Enable
4	R/W	Host System Error Enable
3	R/W	Frame List Rollover Enable
2	R/W	Port Change Detect Enable
1	R/W	USB Error Interrupt Enable
0	R/W	USB Interrupt Enable

Offset 2C-2Fh FRINDEX – Frame Index Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:14	RO	Reserved These registers are always 0.
13:0	R/W	Frame Index The value in this register increments at the end of each time frame.

Offset 34-37h PERIODICLISTBASE – Periodic Frame List Base Address Register

Default Value: undefined

Access: Read/Write

Bit	Access	Description
31:12	R/W	Base Address These bits correspond to memory address [31:12].
11:0	RO	Reserved These registers are always 0.

Offset 38-3Bh ASYNCLISTBASE – Current Asynchronous List Address Register

Default Value: undefined

Access: Read/Write

Bit	Access	Description
31:5	R/W	Link Pointer These bits correspond to memory address [31:5].
4:0	RO	Reserved These registers are always 0.

Offset 60-63h CONFIGFLAG – Configure Flag Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:1	RO	Reserved These registers are always 0.
0	R/W	Configure Flag (CF) Host software sets this bit as the last action in its process of configuring the Host Controller. Writing a one to this register will route all port to this host controller.

Offset 64-67h PORTSC0 – Port 0 Status and Control Register

Offset 68-6Bh PORTSC1 – Port 1 Status and Control Register

Offset 6C-6Fh PORTSC2 – Port 2 Status and Control Register

Offset 70-73h PORTSC3 – Port 3 Status and Control Register

Offset 74-77h PORTSC4 – Port 4 Status and Control Register

Offset 78-7Bh PORTSC5 – Port 5 Status and Control Register

Offset 7C-7Fh PORTSC6 – Port 6 Status and Control Register

Offset 80-83h PORTSC7 – Port 7 Status and Control Register

Default Value: 00003000h

Access: Read/Write

Bit	Access	Description
31:23	RO	Reserved These registers are always 0.
22	R/W	Wake on Over-current Enable (WKOC_E) Writing this bit to a one enables the port to be sensitive to over-current conditions as wake-up events.
21	R/W	Wake on Disconnect Enable (WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events.
20	R/W	Wake on Connect Enable (WKCNNT_E) Writing this bit to a one enables the port to be sensitive to device connects as wake-up events.
19:16	R/W	Port Test Control When this field is zero, the port is NOT operation in a test mode.
15:14	RO	Reserved These registers are always 0.

13	R/W	Port Owner This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. Software writes a one to this bit when the attached device is not a high-speed device.
12	RO	Port Power (PP) The Host Controller does not have port power control switches. Each port is hard-wired to power.
11:10	RO	Line Status These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines.
9	RO	Reserved This bit is always 0.
8	R/W	Port Reset When software writes a one to this bit, the bus reset sequence as defined in the USB Spec Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence.
7	R/W	Suspend Software writes a one to this bit to suspend the downstream port. A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when software sets the Force Port Resume from 1 to 0 or sets the Port Reset bit to 1.
6	R/W	Force Port Resume Software sets this bit to a 1 to driver resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. A write of zero to this bit will force the downstream port follows the resume sequence follows the defined sequence documented in the USB Spec Revision 2.0.
5	R/WC	Over-current Change This bit gets set to a one when there is a change to Over-current Active.
4	RO	Over-current Active 0: This port does not have an over-current condition. 1: This port has an over-current condition.
3	R/WC	Port Enable/Disable Change For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 pointer.

2	R/W	Port Enable/Disabled Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. Ports can be disabled by either a fault condition or by host software.
1	R/WC	Connect Status Change 1: Change in Current Connect Status. 0: No change.
0	R/W	Current Connect Status This value reflects the current connect status of the port.

4.5. USB 2.0-Based Debug Port Register

Offset 100-103h DBGPORTSC – Debug Port Control/Status Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31	RO	Reserved This bit is always 0.
30	R/W	Debug Port Owner Control (OWNER_CNT) When software writes a 1 to this bit, the ownership of the debug port is forced to the EHCI controller.
29	RO	Reserved This bit is always 0.
28	R/W	Debug Port Enable Control (ENABLE_CNT) This bit is a one if the debug port is enabled for operation.
27:17	RO	Reserved These bits are always 0.
16	R/WC	Transaction Done Status (DONE_STS) This bit is set by hardware to indicate that the request is complete.
15:11	RO	Reserved These bits are always 0.
10	R/W	Debug Port in Use (IN_USE_CNT) Set by software to indicate that the port is in use. Cleared by software to indicate that the port is free and may be used by other software.

9:7	RO	Debug Port exception Status (EXCEPTION_STS) This field indicates the exception when ERROR_GOOD#_STS bit is set. 000: No Error 001: Transaction Error 010: Hardware Error
6	RO	Debug Port Error/Good Status (ERROR_GOOD#_STS) Updated by hardware at the same time it set the Done bit. When set it indicates that an error occurred.
5	R/W	Debug Cycle Go (GO_CNT) Software sets this bit to cause the hardware to perform a request.
4	R/W	Debug Cycle Write/READ# Control (WRITER_READ#_CNT) 1: Perform a Write Cycle 0: Perform a Read Cycle
3:0	R/W	Debug Cycle Data Length Control (DATA_LEN_CNT) For write operation, this field is set by software to indicate to the hardware how many bytes of data in Data Buffer are to be transferred to the console. For read operation, this field is set by hardware to indicate to software how many bytes in Data Buffer are valid in response to a read operation.

Offset 104-107h DBGPID – Debug Port PIDs Register

Default Value: 00000000h

Access: Read/Write

Bit	Access	Description
31:24	RO	Reserved These bits are always 0.
23:16	RO	Received PID Status The hardware updates this field with the received PID for transactions in either direction.
15:8	R/W	Send PID Control The hardware sends this PID to begin the data packet when sending data to USB (DATA0 or DATA1).
7:0	R/W	Token PID Control The hardware sends this PID as the Token PID for each USB transaction.

Offset 108-10Fh DBGDB – Debug Port Data Buffer Register

Default Value: undefined

Access: Read/Write

Bit	Access	Description
63:0	R/W	Debug Port Data Buffer These are the 8 bytes of the data buffer.

Offset 110-113h DBGDA – Debug Port Device Address Register

Default Value: 00007F01h

Access: Read/Write

Bit	Access	Description
31:15	RO	Reserved These bits are always 0.
14:8	R/W	USB Address 7-bit field that identifies the USB device address used by the controller for all Token PID generation.
7:4	RO	Reserved These bits are always 0.
3:0	R/W	USB Endpoint 4-bit field that identifies the endpoint used by the controller for all Token PID generation.

5. GigaMAC (Device4:Function0) Registers Description

5.1. GigaMAC Configuration Registers Summary

Acronyms mentioned in the PCI Configuration Registers are defined as follows:

Access	Description
RO	Read-Only
R/W	Read Write
R/W1	Read Write-Once
RC/WC	Write-Clear Read-Clear

Offset	Register Name	Power On Value	Power Plane
00-01h	Vendor ID	1039h	Core
02-03h	Device ID	0190h/0191h/	Core
04-05h	Device Control	0000h	Core
06-07h	Device Status	0210h	Core
08h	Revision ID	02h	Core
09-0Bh	Class Code	020000h	Core
0Ch	Cache Line Size	00h	Core
0Dh	Master Latency Timer	00h	Core
0Eh	Header Type	00h	Core
0Fh	BIST	00h	Core
10-13h	Memory Base Address	00000000h	Core
14-17h	IO Base Address	00000000h	Core
2C-2Dh	Subsystem Vendor ID	0000h	Core
2E-2Fh	Subsystem ID	0000h	Core
34h	Capabilities Pointer	00h	Core
3Ch	Interrupt Line	00h	Core
3Dh	Interrupt Pin	00h	Core
40-43h	Power Management Capabilities		Core
44-47h	Power Management Control/Status		Core
60-63h	EDC Enable Register	000005C0	Core

5.1.1. GigaMAC Configuration Registers Overview

Register 00-01h Vendor ID

Power on value : 1039h

Recommended value : 1039h

Access : RO

Bit	Access	Description	Power On Value	Recom. Setting
15:0	RO	**Vendor Identification Number** This field identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.	1039h	

Register 02-03h Device ID

Power on value : 0190h/0191h

Recommended value : 0190h/0191h

Access : RO

Bit	Access	Description	Power On Value	Recom. Setting
15:0	RO	**Device Identification Number** The device identifier is allocated by Silicon Integrated Systems Corporation. 0190h: 10/100Mbps 0191h: 1000Mbps	0190h/ 0191h	

Register 04-05h Device Control

Power on value : 0000h

Recommended value : 0007h

Access : RO, R/W

Bit	Access	Description	Power On Value	Recom. Setting
15:11	RO	**Reserved**	0	
10	R/W	**Interrupt Disable** This bit controls the device's ability to assert INTA#. 0: enable 1: disable	0b	0b

9:3	RO	**Reserved**	0	
2	R/W	**Bus Master** This bit controls the device's ability to act as a master on the PCI bus. 0: disable 1: enable	0b	1b
1	R/W	**Memory Space** This bit controls the device's response to Memory Space accesses. If this bit is enabled, SiS19X will respond to any memory space access to the operation registers allocated at BAR Reg10H. If this bit is disabled, SiS19X will not respond to any memory space access cycle on the PCI bus. 0: disable 1: enable	0b	1b
0	R/W	**I/O Space** This bit controls the device's response to I/O Space accesses. If this bit is enabled, SiS19X will respond to any I/O space access to the operation registers allocated at BAR Reg14H. If this bit is disabled, SiS19X will not respond to any I/O space access cycle on the PCI bus. 0: disable 1: enable	0b	1b

Register 06-07h Device Status

Power on value : 0210h

Recommended value : 0210h

Access : RO

Bit	Access	Description	Power On Value	Recom. Setting
15:11	RO	**Reserved**	0	

10:9	RO	**DEVSEL# Timing DEVT** These two bits define the timing of asserting DEVSEL#. SiS190/191 always asserts DEVSEL# in medium timing, and thus the two bits are read as "01" per PCI Spec.	01b	
8:5	RO	**Reserved**	0	
4	RO	**Capabilities List** This bit indicates that SiS19X implements the pointer for a capabilities linked list at Reg34H.	1b	
3	RO	**Interrupt Status** This bit is the status of INTA#, and is independent of **Interrupt Disable** bit at Reg04H, Bit10.	0b	
2:0	RO	**Reserved**	0	

Register 08h Revision ID

Power on value : 02h

Recommended value : 02h

Access : RO

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Revision Identification Number**	02h	

Register 09-0Bh Class Code

Power on value : 020000h

Recommended value : 020000h

Access : RO

Bit	Access	Description	Power On Value	Recom. Setting
23:0	RO	**Class Code** 020000h: Ethernet Controller	020000h	

Register 0Ch Cache Line Size

Power on value : **00h**

Recommended value : **00h**

Access : **RO**

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Cache Line Size** Ignored by SiS19X	00h	

Register 0Dh **Master Latency Timer**

Power on value : **00h**

Recommended value : **00h**

Access : **RO**

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Initial Value for Latency Timer** Ignored by SiS19X	00h	

Register 0Eh **Header Type**

Power on value : **00h**

Recommended value : **00h**

Access : **RO**

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Header Type**	00h	

Register 0Fh **BIST**

Power on value : **00h**

Recommended value : **00h**

Access : **RO**

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**BIST** SiS19X does not support BIST.	00h	

Register 10~13h Memory Base Address

Power on value : 0000_0000h

Recommended value : XXXX_XXX0h

Access : R/W, RO

Bit	Access	Description	Power On Value	Recom. Setting
31:10	R/W	**Base** This is set by software to the base address for the Operation Registers Map.	0000000h	
9:7	RO/RW	**Size/Base** For SiS190/191, these bits are used as "BASE".	000b	
6:4	RO	**Size** For SiS190/191, these bits are hardwired as 0, which indicates that requires 128 bytes of Memory Space for the Operation Registers Map.	000b	
3	RO	**Prefetchable** Set to 0 to indicate SiS19X does not support this feature.	0b	
2:1	RO	**Type** Set to 00 indicate the base register is 32-bits wide and can be placed anywhere in the 32-bit memory space.	00b	
0	RO	**Memory Space Indicator** Set to 0 indicate SiS19X is capable of being mapped into memory space.	0b	

Register 14~17h IO Base Address

Power on value : 0000_0000h

Recommended value : 0000_XXX0h

Access : RO, R/W

Bit	Access	Description	Power On Value	Recom. Setting
31:16	RO	**Reserved**	0000h	

15:7	R/W	**Base** This is set by software to the base address for the Operation Registers Map.	00h	
6:2	RO	**Size** These bits return 0, which indicates that SiS19X requires 128 bytes of IO Space for the Operation Registers Map.	00000b	
1	RO	**Reserved**	0b	
0	RO	**IO Space Indicator** Set to 1 indicate SiS19X is capable of being mapped into IO space.	1b	

Register 2C~2Dh Subsystem Vendor ID

Power on value : 0000h

Recommended value : XXXXh

Access : R/W1

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W1	**Subsystem Vendor ID** This field can be written once and is used to identify vendor of the subsystem.	0000h	

Register 2E~2Fh Subsystem ID

Power on value : 0000h

Recommended value : XXXXh

Access : R/W1

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W1	**Subsystem ID** This field can be written once and is used to identify subsystem ID.	0000h	

Register 34h Capabilities Pointer

Power on value : 40h

Recommended value : 40h

Access : RO

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Capabilities Pointer** The offset into the function PCI Configuration Space for the location of the first item in the Capabilities linked list. Hardwired to 40h in SiS19X.	40h	

Register 3Ch Interrupt Line

Power on value : 00h

Recommended value : XXh

Access : R/W

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Interrupt Line** This field is used to set which line on the interrupt controller that SiS19X's interrupt pin is connected to.	00h	

Register 3Dh Interrupt Pin

Power on value : 01h

Recommended value : 01h

Access : RO

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Interrupt Pin** This field is used to tell the driver or operation system that which interrupt pin SiS19X uses. Always return 01h(INTA)	01h	

Register 40-43h Power Management Capabilities

Power on value : XE02_0001h

Recommended value : XE02_0001h

Access : **RO**

Bit	Access	Description	Power On Value	Recom. Setting
31:27	RO	**PME Support** This field is used to indicate PME# may be asserted from which power state. If auxiliary power source is present, this 5-bit field is 11111b indicating PME# can be asserted from D0, D1, D2, D3hot and D3cold. If auxiliary power source is absent, this 5-bit field is 01111b indicating PME# can be asserted from D0, D1, D2, D3hot but cannot be asserted from D3cold.	11111b or 01111b	
26	RO	**D2 Support** Set to 1 by SiS19X indicates that SiS19X supports D2 Power Management State.	1b	
25	RO	**D1 Support** Set to 1 by SiS19X indicates that SiS19X supports D1 Power Management State	1b	
24:22	RO	**Auxiliary Current** This field reports the 3.3Vaux auxiliary current requirement for SiS19X	000b	
21	RO	**Device Specific Initialization** This bit would be read as 0 to indicate no special initialization is required before the generic class device driver is able to use it.	0b	
20	RO	**Reserved**	0b	
19	RO	**PME Clock** Set to 0 by SiS19X to indicate that no PCI clock is required for SiS19X to generate PME#	0b	
18:16	RO	**PCI PM Spec. Version** A value of 010b indicates that SiS19X complies with Reversion 1.1 of the PCI Power Management Interface Specification.	010	
15:8	RO	**Next Item Pointer** These bits would be 00h to indicate no additional items in the capabilities list.	00h	

7:0	RO	**Capability ID** Set to 01h to indicate that the linked list item as being the PCI Power Management registers.	01h	

Register 44-47h Power Management Control/Status

Power on value : 0000_0000h

Recommended value : 0000_0000h

Access : RO, R/W

Bit	Access	Description	Power On Value	Recom. Setting
31:24	RO	**State Dependent Data** Not Implement.	00h	
23:16	RO	**PMCSR PCI to PCI Bridge Support Extensions** Not Implement.	00h	
15	R/W	**PM Status** This bit is set when SiS19X would normally assert the PME# signal independent of the state of **PME Enable** bit. Writing a '1' to this bit will clear it and cause SiS19X to stop asserting a PME# (if enabled). Writing a '0' has no effect. If auxiliary power source is present, i.e. PME# can be asserted from D3cold, then this bit must be explicitly cleared by the operating system each time the operating system initially loaded. Unchanged by hardware reset.	0b	
14:13	RO	**Data Scale** Not Implement.	00b	
12:9	RO	**Data Select** Not implement.	0000b	

8	R/W	**PME Enable** This bit controls SiS19X's ability to assert PME#. Writing a '1' enables SiS19X to assert PME#. Writing a '0', PME# assertion is disabled. If auxiliary power source is present, i.e. PME# can be asserted from D3cold, then this bit must be explicitly cleared by the operation system each time the operating system is initially loaded. Unchanged by hardware reset. 0: disable 1: enable	0b	
7:2	RO	**Reserved**	0h	
1:0	R/W	**Power State** This two-bit field is used to determine the current power state of SiS19X and to set SiS19X into a new power state. The definition is given below: 00b: D0 01b: D1 10b: D2 11b: D3hot	00b	

Register 60-63h EDC Enable Register

Power on value : 0000_05C0h

Recommended value : 0000_15EFh186Fh

Access : RO, R/W

Bit	Access	Description	Power On Value	Recom. Setting
31:14	RO	**Reserved**	0h	
13	R/W	**Reserved**	0b	0b
12	R/W	**Root_en_tx, for root gated** **'0': root gated disable** **'1': root gated enable**	0b	1b

11:9	R/W	**DCC State "PRUN" to "RUN" Counter** 000 : 2T 001 : 3T 010 : 4T 011 : 5T 100 : 6T 101 : 7T 110 : 8T 111 : 9T	010	100
8	R/W	**DCC State "PSTOP" to "STOP" Counter Enable** 0: Disable, 1T 1: Enable, 8T	1b	0b
7:6	R/W	**DCC State "RUN" to "PSTOP" Counter** 00: 4T 01: 8T 10: 16T 11: 32T	11b	01b
5	R/W	**ASL EDC Enable** 0: Disable, 1: Enable	0b	1b
4	R/W	Reserved	0b	0b
3	R/W	**TCP_CLK EDC Enable** 0: Disable, 1: Enable	0b	1b
2	R/W	**TX_CLK EDC Enable** 0: Disable, 1: Enable	0b	1b
1	R/W	**LNK_CLK EDC Enable** 0: Disable, 1: Enable	0b	1b
0	R/W	**PCI_CLK EDC Enable** 0: Disable, 1: Enable	0b	1b

6. 968 SATA (Device5:Function0) (Native and AHCI)

6.1. SATA Configuration Space Register

Offset	Register Name	Power On Value	Power Plane
00-01h	Vendor ID	1039h	MAIN
02-03h	Device ID	1183h	MAIN
04-05h	Device Control	0000h	MAIN
06-07h	Device Status	0210h	MAIN
08h	Revision ID	03h	MAIN
09h	Programming Interface	8Ah	MAIN
0Ah	Sub Class Code	01h	MAIN
0Bh	Base Class Code	01h	MAIN
0Ch	Cache Line Size	00h	MAIN
0Dh	Master Latency Timer	00h	MAIN
0Eh	Header Type	00h	MAIN
0Fh	BIST	00h	MAIN
10-13h	Primary Channel Command Block Base Address	00000001h	MAIN
14-17h	Primary Channel Control Block Base Address	00000001h	MAIN
18-1Bh	Secondary Channel Command Block Base Address	00000001h	MAIN
1C-1Fh	Secondary Channel Control Block Base Address	00000001h	MAIN
20-23h	Bus Master IDE Control Registers Base Address	00000001h	MAIN
24-27h	**Native :** SATA Status and Control Register IO-Mapped Base Address **AHCI :** AHCI Base Address	00000000h	MAIN
28-2Bh	Reserved	00000000h	MAIN
2C-2Dh	Subsystem Vendor ID	0000h	MAIN
2E-2Fh	Subsystem ID	0000h	MAIN
30-33h	Reserved	00000000h	MAIN
34h	Capabilities Pointer	58h	MAIN
35-37h	Reserved	000000h	MAIN
38-3Bh	Reserved	00000000h	MAIN

3Ch	Interrupt Line	00h	MAIN
3Dh	Interrupt Pin	01h	MAIN
3Eh	Min_Gnt	00h	MAIN
3Fh	Max_Lat	00h	MAIN
40-43h	Reserved	00000000h	MAIN
44-47h	Reserved	00000000h	MAIN
48-4Bh	Reserved	00000000h	MAIN
4C-4Fh	Reserved	00000000h	MAIN
50-51h	SATA Controller Primary Channel Control	00A8h	MAIN
52-53h	SATA Controller Secondary Channel Control	00A8h	MAIN
54-57h	SATA General Control	10910000h	MAIN
58h-5Bh	Power Management Capabilities	80020001h	MAIN
5C-5Fh	Power Management Control and Status	00000000h	MAIN
60-63h	Reserved	00020020h	MAIN
64-67h	SATA General Control 2	00000000h	MAIN
68-6Bh	EDC Register	00000DDDh	MAIN
6C-6Fh	Reserved	00000000h	MAIN
70-73h	SATA IDP Capability Register 0	00000000h	MAIN
74-77h	SATA IDP Capability Register 1	00000000h	MAIN
78-7Bh	Reserved	00000000h	MAIN
7C-7Fh	Reserved	00000000h	MAIN
80-83h	1st SATA Channel Control	407E33BEh	MAIN
84-87h	2nd SATA Channel Control	407E33BEh	MAIN
88-8Bh	Reserved	00000000h	MAIN
8C-8Fh	Reserved	00000000h	MAIN
90-93h	Miscellaneous Control	03000140h	MAIN
94-97h	Reserved	00000000h	MAIN
98-9Bh	Reserved	00000000h	MAIN
9C-9Fh	SATA PHY Control Register E	00000000h	MAIN
A0-A3h	SATA PHY Control Register A	39E3B14Fh	MAIN
A4-A7h	SATA PHY Control Register B	803E2498h	MAIN
A8-ABh	SATA PHY Control Register C	0112401Ch	MAIN
AC-AFh	SATA PHY Control Register D	02000000h	MAIN
B0-B3h	Reserved	00000000h	MAIN
B4-B7h	SATA BIST Control Register	00000000h	MAIN
B8-BBh	SATA BIST Control DATA A	7F7F7F7Fh	MAIN

BC-BFh	SATA BIST Control DATA B	7F7F7F7Fh	MAIN
C0-C3h	1st SATA Channel SStatus Register	00000000h	MAIN
C4-C7h	1st SATA Channel SError Register	00000000h	MAIN
C8-CBh	1st SATA Channel SControl Register	00000300h	MAIN
CC-CFh	Reserved	00000000h	MAIN
D0-D3h	2nd SATA Channel SStatus Register	00000000h	MAIN
D4-D7h	2nd SATA Channel SError Register	00000000h	MAIN
D8-DBh	2nd SATA Channel SControl Register	00000300h	MAIN
DC-DFh	Reserved	00000000h	MAIN
E0-E3h	Reserved	00000000h	MAIN
E4-E7h	Reserved	00000000h	MAIN
E8-EBh	Reserved	00000000h	MAIN
EC-EFh	Reserved	00000000h	MAIN
F0-F3h	Reserved	00000000h	MAIN
F4-F7h	Reserved	00000000h	MAIN
F8-FBh	Reserved	00000000h	MAIN
FC-FFh	Reserved	00000000h	MAIN

Register 00-01h Vendor ID

Bit	Access	Description	Power On Value	Recom. Setting
15:0	RO	**Vendor Identification Number** The register identifies the manufacturer of the device. SiS is allocated as 1039h by PCI SIG.	1039h	

Register 02-03h Device ID

Bit	Access	Description	Power On Value	Recom. Setting

<table>
<tr>
<td>15:0</td>
<td>RO</td>
<td>Native : Device Identification Number
The device identifier is allocated as 1183 by Silicon Integrated Systems Corp.
AHCI : Device Identification Number
The device identifier is allocated as 1185 by Silicon Integrated Systems Corp.
AHCI RAID : Device Identification Number
The device identifier is allocated as 1184 by Silicon Integrated Systems Corp.
<table>
<tr><th>RAID Enable</th><th>AHCI Enable</th><th rowspan="2">Device ID</th></tr>
<tr><td>Reg54h Bit25</td><td>Reg54h Bit11</td></tr>
<tr><td>0</td><td>0</td><td>1183</td></tr>
<tr><td>0</td><td>1</td><td>1185</td></tr>
<tr><td>1</td><td>0</td><td>1184</td></tr>
<tr><td>1</td><td>1</td><td>1184</td></tr>
</table>
</td>
<td>1183h</td>
<td></td>
</tr>
</table>

Register 04-05h Device Control

Bit	Access	Description	Power On Value	Recom. Setting
15:11	RO	**Reserved.** Read as zero.	00000b	
10	R/W	**Interrupt Disable** When this bit is set, the assertion of the INTX in native mode is disabled. 0: INTX is enabled. 1: INTX is disabled.	0b	0b
9:3	RO	**Reserved.** Read as zero.	0000000b	
2	R/W	**Bus Master** When this bit is set, the Bus Master function is enabled. 0: disable 1: enable	0b	1b

1	R/W	**Memory Space** When enabled, device will response to Memory Space Access. 0: disable 1: enable	0b	
0	R/W	**I/O Space** When enabled, the built-in IDE will respond to any access of the IDE legacy ports in the compatibility mode, or to any access of the IDE relocated ports in the native mode. Also, any access to the PCI bus master IDE registers are allowed. 0: disable 1: enable	0b	1b

Register 06-07h Device Status

Bit	Access	Description	Power On Value	Recom. Setting
15:14	RO	**Reserved.** Read as zero.	00b	
13	R/WC	**Master Abort Asserted** This bit is set 1 when a PCI bus master IDE transaction is terminated by master abort.	0b	
12	R/WC	**Received Target Abort** The bit is set 1 when a PCI bus master IDE transaction is terminated with target abort.	0b	
11	RO	**Signaled Target Abort** The bit will always be read as 0 because the IDE controller will never signal Target-Abort.	0b	
10:9	RO	**DEVSEL# Timing DEVT** These two bits define the timing of asserting DEVSEL#. The built-in IDE always asserts DEVSEL# in medium timing, and thus the two bits are read as 01 per PCI Spec.	01b	
8:5	RO	**Reserved.** Read as zero.	0000b	

4	RO	**Capabilities List** This read-only bit indicates whether or not IDE controller implements the pointer for a New Capabilities linked list at configuration register 34h.	1b	
3	RO	**Interrupt Status** This bit is the status of INTA#, and independent of **Interrupt Disable** at Reg04H, Bit10.	0b	
2:0	RO	**Reserved.** Read as zero.	000b	

Register 08h Revision ID

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	Revision Identification Number	03h	

Register 09h Programming Interface

Bit	Access	Description	Power On Value	Recom. Setting
7	RO	**Native:** This bit is hardwired to one to indicate that the built-in IDE is capable of supporting bus master function. **AHCI/AHCI RAID:** **Reserved.** Read as zero.	1b	
6:4	RO	**Reserved.** Read as zero.	000b	
3	RO	**Native:** This bit indicates whether or not the secondary channel has a fixed mode of operation. If this bit is zero, the mode is fixed and is determined by the (read-only) value of bit 2. If this bit is one, the channel supports both modes and may be set to either mode by writing bit 2. This bit can be modified by Reg50h Bit19. **AHCI/AHCI RAID:** **Reserved.** Read as zero.	1b	

2	R/W	**Native:** Determines the mode that the secondary channel is operating in. Zero corresponds to compatibility, one means native-PCI mode. This bit is implemented as read-only if the channel supports only one mode, or read-write if both modes are supported. **AHCI/AHCI RAID:** **Reserved.** Read as zero.	0b	
1	RO	**Native:** This bit indicates whether or not the primary channel has a fixed mode of operation. If this bit is zero, the mode is fixed and is determined by the (read-only) value of bit 0. If this bit is one, the channel supports both modes and may be set to either mode by writing bit 0. This bit can be modified by Reg50h Bit3. **AHCI/AHCI RAID:** **Reserved.** Read as zero.	1b	
0	R/W	**Native:** Determines the mode that the primary channel is operating in. Zero corresponds to compatibility, one means native-PCI mode. This bit is implemented as read-only if the channel supports only one mode, or read-write if both modes are supported. **AHCI:** This bit indicates that this is an AHCI HBA that has a major revision of 1 (as specified in the AHCI Version register) **AHCI RAID:** **Reserved.** Read as zero.	0b	

Register 0Ah Sub Class Code

Bit	Access	Description	Power On Value	Recom. Setting

7:0	RO	The Sub Class Code is defined for the type of the mass storage controller. 01h: IDE controller 04h: RAID controller 06h: SATA controller	01h	

RAID Enable	AHCI Enable	Sub Class Code
Reg54h Bit25	Reg54h Bit11	
0	0	01
0	1	06
1	0	04
1	1	04

Register 0Bh Base Class Code

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Base Class Code**	01h	

Register 0Ch Cache Line Size

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Cache Line Size**	00h	

Register 0Dh Master Latency Timer

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Master Latency Timer** The initial value for latency timer. The Unit is the PCI clock.	00h	80h

Register 0Eh Header Type

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Header Type**	00h	

Register 0Fh BIST

Bit	Access	Description	Power On Value	Recom. Setting

7:0	RO	**BIST** IDE controller does not support BIST. Reserved. Read as zero.	00h	

Register 10-13h Primary Channel Command Block BAR

Register 14-17h Primary Channel Control Block BAR

Register 18-1Bh Secondary Channel Command Block BAR

Register 1C-1Fh Secondary Channel Control Block BAR

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**Base Address Register** These register is programmable only when both operating or native mode enabled, otherwise reads as 00000001h.	00000001h	

Register 20-23h Bus Master IDE Control Register Base Address

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**Bus Master IDE Control Block BAR**	00000001h	

Register 24-27h SATA Status and Control Registers IO-Mapped BAR / AHCI Base Address Register

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**Native: SATA SCR BAR** The SCR io-mapped function is supoorted when Reg54h Bit26 is set. **AHCI/AHCI RAID: AHCI BAR** AHCI memory space base address register.	00000000h	

Register 2C-2Dh Subsystem Vendor ID

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W1	**Subsystem Vendor ID**	0000h	

Register 2E-2Fh Subsystem ID

Bit	Access	Description	Power On Value	Recom. Setting
15:0	R/W1	**Subsystem ID**	0000h	

Register 34h Capabilities Pointer

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Capabilities Pointer** The offset into the function PCI Configuration Space for the location of the first item in the Capabilities linked list. The register read as 58h when Reg54h Bit28 set to one.	58h	

Register 3Ch Interrupt Line

Bit	Access	Description	Power On Value	Recom. Setting
7:0	R/W	**Interrupt Line** This register is writable when both operating modes enabled or one of the two channels operating in the Native mode.	00h	

Register 3Dh Interrupt Pin

Bit	Access	Description	Power On Value	Recom. Setting
7:0	RO	**Interrupt Pin** This register is used to tell the drivers or operation systems that which interrupt pin the SATA controller uses. The value of this register is read only as 01h and means INTA# when bothmode or native mode is enabled.	01h	

Register 50-51h SATA Controller Primary Channel Control

Register 52-53h SATA Controller Secondary Channel Control

Bit	Access	Description	Power On Value	Recom. Setting
15:8	RO	**Reserved.** Read as zero.	00h	

7	R/W	**Native/AHCI: IRQ Control** When this bit is set 0, the IRQ of HD drive would pass direct to 8259. On the others hand, SATA would gate IRQ until SATA FIFO is empty. 0: Direct Mode 1: Flush Mode	1b	1b
6	RO	**Reserved.** Read as zero.	0b	
5	RO	**Reserved.** Read as one.	1b	
4	RO	**Reserved.** Read as zero.	0b	
3	R/W	**Native: SATA Controller Operation Mode Control** 0: SATA Controller only supports Compatibility mode. 1: SATA Controller supports both modes. (Compatibility and Native mode).	1b	
2	RO	**Reserved.** Read as zero.	0b	
1	R/W	**Native: SATA Channel Enable Control** 0: Disabled 1: Enabled	0b	1b
0	RO	**Reserved.** Read as zero.	0b	

Register 54-57h SATA Controller General Control Register

Bit	Access	Description	Power On Value	Recom. Setting
31:29	RO	**Reserved.** Read as zero.	000b	
28	R/W	**Native/AHCI: Capability Pointer Control** 0: No Capability Supported. The Register 06h, Bit 4 and Register 34h would be read as zeros. 1: Capability Supported. The Register 06h, Bit 4 would be read as 1 and the Register 34h would be read as 00000058h.	1b	1b

<table>
<tr><td>27</td><td>R/W</td><td>Native/AHCI: Retry Function for PCI IO READ when SATA Physical Layer is not ready.
0: Disabled.
1: Enable.</td><td>0b</td><td>0b</td></tr>
<tr><td>26</td><td>R/W</td><td>Native/AHCI: Serial ATA Status and Control Register(SCR's) IO-Mapped Control
0: default (configuration register access mode).
1: io-mapped mode. When this bit is set, SCR's register can be access by io access operation. And Io-mapped base address is located on Reg24H~27H.</td><td>0b</td><td>0b</td></tr>
<tr><td>25</td><td>R/W</td><td>Native/AHCI: RAID sub class enable.
0: sub class 01h or 06h.
1: sub class 04h.
<table>
<tr><th>RAID Enable</th><th>AHCI Enable</th><th rowspan="2">Sub Class Code</th></tr>
<tr><td>Reg54h Bit25</td><td>Reg54h Bit11</td></tr>
<tr><td>0</td><td>0</td><td>01</td></tr>
<tr><td>0</td><td>1</td><td>06</td></tr>
<tr><td>1</td><td>0</td><td>04</td></tr>
<tr><td>1</td><td>1</td><td>04</td></tr>
</table></td><td>0b</td><td></td></tr>
<tr><td>24</td><td>R/W</td><td>Native/AHCI: Legacy mode interrupt controlled by PCI Spec.
When legacy mode is selected and the bit is set, the assertion of INT14/15 is controlled by Interrupt Disable Reg04H, Bit10 and Interrupt Status at Reg06H, Bit 3 reflects the int14/15.
0: disabled.
1: enabled.</td><td>0b</td><td>0b</td></tr>
<tr><td>23</td><td>R/W</td><td>Native/AHCI: EDPCI Bus R-R PipeLine Enable
0: Disabled.
1: Enabled.</td><td>1b</td><td>1b</td></tr>
<tr><td>22</td><td>R/W</td><td>Native/AHCI: EDPCI R-R PipeLine Depth
0: Depth 3.
1: Depth 8.</td><td>0b</td><td>0b</td></tr>
</table>

<table>
<tr><td>21:20</td><td>R/W</td><td>Native/AHCI: Master Read Request Threshold Setting
Request trigger at rested more than
00: 8QW.
01: 4QW.
10: 2QW.
11: 1QW.</td><td>01b</td><td>01b</td></tr>
<tr><td>19</td><td>RW</td><td>Native/AHCI: Isochronous Tag.
When this bit is set, the transaction on EDPCI bus is tagged as the isochronous transaction
0: Disable
1: Enable</td><td>0b</td><td>0b</td></tr>
<tr><td>18</td><td>R/W</td><td>Native/AHCI: Cluster Access Tag
The indication is used to guarantee the continuous response for the cluster accesses.
0: Disabled.
1: Enabled.</td><td>0b</td><td>0b</td></tr>
<tr><td>17:16</td><td>R/W</td><td>Native/AHCI: Master Write Request Threshold Setting
Request trigger at FIFO used more than
00: 8QW.
01: 4QW.
10: 2QW.
11: 1QW.</td><td>01b</td><td>01b</td></tr>
<tr><td>15:12</td><td>RO</td><td>Reserved. Read as zero.</td><td>0000b</td><td>0000b</td></tr>
<tr><td>11</td><td>R/W</td><td>Native/AHCI: Sub Class of SATA enable
0: sub class 04
1: sub class 06
<table>
<tr><th>RAID Enable
Reg54h Bit25</th><th>AHCI Enable
Reg54h Bit11</th><th>Sub Class Code</th></tr>
<tr><td>0</td><td>0</td><td>01</td></tr>
<tr><td>0</td><td>1</td><td>06</td></tr>
<tr><td>1</td><td>0</td><td>04</td></tr>
<tr><td>1</td><td>1</td><td>04</td></tr>
</table>
Before the AHCI is enabled, this bit must be set.</td><td>0b</td><td></td></tr>
<tr><td>10:8</td><td>RO</td><td>Reserved. Read as zero.</td><td>000b</td><td>000b</td></tr>
</table>

7	RW	**Native: D2 Support** This bit is written as 1 to indicate SATA controller supports the D2 power management state or it indicate SATA controller doesn't support the D2 power management state. **AHCI: D2 Support** Read as zero.	0b	0b
6	RW	**Native: D1 Support** This bit is written as 1 to indicate SATA controller supports the D1 power management state or it indicate SATA controller doesn't support the D1 power management state. **AHCI: D1 Support** Read as zero.	0b	0b
5:0	RO	**Reserved.**	00000b	00000b

Register 58-5Bh Power Management Capabilities

Bit	Access	Description	Power On Value	Recom. Setting
31	RO	**D3 Cold PME enable** **Native :** Enabled. Read as 1. **AHCI :** Disabled. Read as 0.	1b	
30	RO	**D3 Hot PME enable** **Native :** Disalbed. Read as 0. **AHCI :** Enabled. Read as 1.	0b	
29:27	RO	**Reserved.**	000b	000b

26	RO	**Native: D2 Support** This bit is read only as 1 to indicate SATA controller supports the D2 power management state or it indicate SATA controller doesn't support the D2 power management state. **AHCI: D2 Support** Read as zero.	0b	
25	RO	**Native: D1 Support** This bit is read only as 1 to indicate SATA controller supports the D1 power management state or it indicate SATA controller doesn't support the D1 power management state. **AHCI: D1 Support** Read as zero.	0b	
24:22	RO	**Native/AHCI: Reserved.** Read as zero.	000b	
21	RO	**Native/AHCI: Device Specific Initialization** This bit would be read as 0 to indicate no special initialization is required before the generic class device driver is able to use it.	0b	
20	RO	**Native/AHCI: Reserved.** Read as zero.	0b	
19	RO	**Native/AHCI: PME Clock** This bit would be read as 0 to indicate IDE controller would not generate PME# and no PCI clock is required.	0b	
18:16	RO	**Native/AHCI: PCI PM Spec. Version** A value of 010b indicates that this function complies with Reversion 1.1 of the PCI Power Management Interface Specification.	010b	
15:8	RO	**Native/AHCI: Next Item Pointer** When IDP enable, then these bits would be 70h. If IDP is not enable then these bits would be 00h to indicate no additional items in the capabilities list. IDP can be configured by R64h Bit24 when AHCI enable.	00h	

7:0	RO	**Native/AHCI: Capability ID** Read as 01h to identify the linked list item as being the PCI Power Management register.	01h	

Register 5C-5Fh Power Management Control/Status

Bit	Access	Description	Power On Value	Recom. Setting
31:24	RO	**Native/AHCI: State Dependent Data** Not Implemented. Read as all zeros.	00h	
23:16	RO	**Native/AHCI: PMCSR PCI to PCI Bridge Support Extensions** Not Implemented. Read as all zeros.	00h	
15	RO	**Native: PM Status** This bit would be 0 to indicate no PME# function is supported. **AHCI: PM Status**	0b	
14:13	RO	**Native/AHCI: Data Scale** Not Implemented. Read as all zeros.	00b	
12:9	RO	**Native/AHCI: Data Select** Not implemented. Read as all zeros.	0000b	
8	RW	**Native/AHCI: PME Enable** This bit would be 0 to indicate no PME# function.	0b	
7:2	RO	**Native/AHCI: Reserved.** Read as zero.	00h	
1:0	R/W	**Native/AHCI: Power State** This two-bit field is used to determine the current power state and to set into a new power state. The definition is given below: 00b: D0 01b: D1 10b: D2 11b: D3hot	00b	

Register 60-63h Reserved

Bit	Access	Description	Power On Value	Recom. Setting

31:0	RO	**Reserved.**	00020020h	

Register 64-67h SATA Controller General Control Register 2

Bit	Access	Description	Power On Value	Recom. Setting
31	RW	**Native/AHCI: Auto Flush**	0b	
30	RO	**Reserved.**	0b	
29	RW	**AHCI: Aggressive Read MEM**	0b	1b
28	RO	**Reserved.**	0b	
27	RW	**AHCI: AHCI Flush**	0b	1b
26	RO	**Reserved.**	0b	
25	RW	**Native/AHCI:wthold FIX** **0: no effect** **1: change wthold to 01h**	0b	**1b**
24	RW	**Native/AHCI: IDP Enbale** **0 : disable IDP** **1 : enable IDP**	0b	
23:16	RO	**Reserved.** Read as zero.	00h	
15	RO	**Reserved.** Read as zero.	0b	
14:8	R/W	**Reserved.** Read as zero.	00h	
7	RO	**Reserved.** Read as zero.	0b	
6:0	R/W	**Reserved.** Read as zero.	00h	

Register 68-6Bh Reserved

Bit	Access	Description	Power On Value	Recom. Setting
31	R/W	**ASL FFC clock EDC Enable** **0:disabled** **1:enabled**	0b	1b
30	RO	**Reserved.**	0b	
29	R/W	**PCI clock EDC Enable** **0:disabled** **1:enabled**	0b	1b
28	R/W	**ASL EDB clock EDC Enable** **0:disabled** **1:enabled**	0b	1b
27:26	RO	**Reserved.**	00b	

25	R/W	**ASL P1 PKT clock EDC Enable 0:disabled 1:enabled**	0b	1b
24	R/W	**ASL P0 PKT clock EDC Enable 0:disabled 1:enabled**	0b	1b
23:22	RO	**Reserved.**	00b	
21	R/W	**SATA P1 SDEV clock EDC Enable 0:disabled 1:enabled**	0b	1b
20	R/W	**SATA P0 SDEV clock EDC Enable 0:disabled 1:enabled**	0b	1b
19:18	RO	**Reserved.**	00b	
17	R/W	**SATA P1 PHY clock EDC Enable 0:disabled 1:enabled**	0b	1b
16	R/W	**SATA P0 PHY clock EDC Enable 0:disabled 1:enabled**	0b	1b
15:12	RO	**Reserved.**	0b	
11:10	R/W	**ASL clock EDC Enter Timer Control 11: 32T 10: 25T 01: 17T 00: 5T**	11b	11b
9:8	R/W	**ASL clock EDC Wakeup Timer Control 11: 8T 10: 6T 01: 5T 00: 4T**	01b	01b
7:6	R/W	**SATA clock EDC Enter Timer Control 11: 32T 10: 25T 01: 17T 00: 5T**	11b	11b
5:4	R/W	**SATA clock EDC Wakeup Timer Control 11: 8T 10: 6T 01: 5T 00: 4T**	01b	01b
3:2	R/W	**PCI clock EDC Enter Timer Control 11: 32T 10: 25T 01: 17T 00: 5T**	11b	11b
1:0	R/W	**PCI clock EDC Wakeup Timer Control 11: 8T 10: 6T 01: 5T 00: 4T**	01b	01b

Register 6C-6Fh Reserved

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**Reserved.**	00000000h	

Register 70-73h SATA IDP Capability Register 0

Bit	Access	Description	Power On Value	Recom. Setting
31:24	RO	**Reserved. Read as 00h.**	**00h**	
23:20	RO	**Major Revision.**	**0001b**	
19:16	RO	**Minor Revision.**	**0000b**	
15:8	RO	**Next Capability.**	**00h**	
7:0	RO	**Capability ID.**	**12h**	

Note:Read as 00000000h if 64h[24]=0

Register 74-77h SATA IDP Capability Register 1

Bit	Access	Description	Power On Value	Recom. Setting
31:24	RO	**Reserved. Read as 00h.**	**00h**	
23:4	RO	**BAR offset 00004h (10h offset)**	**00004h**	
3:0	RO	**BAR location 1000b (20h BAR)**	**8h**	

Note:Read as 00000000h if 64h[24]=0

Register 80-83h 1st SATA Channel Control

Register 84-87h 2nd SATA Channel Control

Bit	Access	Description	Power On Value	Recom. Setting
31	RO	**Native/AHCI: PHYRDY From Phy** The bit indicates whether or not Phy established the communication with the drive successfully. 0: not ready. 1: ready.	0b	

30	R/W	**Native/AHCI: High Byte of Shadow Register Enable (48-bit Addresses)** When this bit is set, register read of sector count, sector number, cylinder low, and cylinder high returns high byte value in the shadow registers if HOB bit in the control register is set. Or the register read of sector count, sector number, cylinder low, and cylinder high can only return low byte value. 0: disable 1: enable	1b	1b
29	R/W	**Native/AHCI: Interrupt of SATA Device Disconnecting** When this bit is set, IDE controller asserts INTX# to indicate the drive off if the drive attached in the cable is removed. 0: disabled. 1: enabled.	0b	0b
28	R/W	**Native/AHCI: Interrupt of SATA Device Connecting** When this bit is set, IDE controller asserts INTX# to indicate the drive on if the drive is attached in the cable. 0: disabled. 1: enabled.	0b	0b
27	RO	**Native/AHCI: PWRDENY** The bit indicates partial or slumber power mode request is denied by the drive. 0: default. 1: the drive responses with PWRDENY.	0b	
26	RO	**Native/AHCI: PWRGNT** The bit indicates partial or slumber power mode request gets the acknowledge from the device. 0: default. 1: the drive responses with PWRGNT.	0b	

25	R/W	**Native/AHCI: Activate Slumber Power Management State** When this bit is set, P180 controller activates slumber power management mode request to both PHY and device and the result is placed at Bit24/25.. 0: disabled. 1: enabled.	0b	
24	R/W	**Native/AHCI: Activate Partial Power Management State** When this bit is set, P180 controller activates partial power management mode request to both PHY and device and the result is placed at Bit24/25. 0: disabled. 1: enabled.	0b	
23	R/W	**Native/AHCI: Auto Comma** When this bit is set, comma information is automatically generated by the data received from PHY rather than uses the comma signal sent from PHY 0: disabled. 1: enabled.	0b	0b
22	R/W	**Native/AHCI: Depth of Rx Synchronization Buffer** 0: 2 level. 1: 3 level. note: 1 level = 40 bits.	1b	1b
21:20	R/W	**Native/AHCI: Position of Push Signal of Rx Synchronization Buffer** 00: 1st byte. 01: 2nd byte. 10: 3rd byte. 11: 4th byte.	11b	11b
19	R/W	**Native/AHCI: Port 0 FIFO Release** 0: disable fifo release 1: enable fifo release to enhance receive buffer to avoid buffer overflow	1b	0b
18	R/W	**Native/AHCI: Depth of Tx Synchronization Buffer** 0: 2 level. 1: 3 level. note: 1 level = 40 bits.	1b	1b

17:16	R/W	**Native/AHCI: Position of Pop signal of Tx Synchronization Buffer** 00: 1st byte. 01: 2nd byte. 10: 3rd byte. 11: 4th byte.	10b	10b
15	R/W	**Native/AHCI:** 0: allow plug-in event to be happened when com_det is 0001 1: not allow plug-in event to be happened when com_det is 0001	0b	1b
14	RO	**Reserved.** Read as zero.	0b	
13	R/W	**Native/AHCI: Rx Error Handling Enable** When this bit is set, received data bit error is controlled to avoid state machine misbehave. 0: disabled. 1: enabled.	1b	1b
12	R/W	**Native/AHCI: Rx De-Scramble Enable** When this bit is set, received data de-scrambled. 0: disabled. 1: enabled.	1b	1b
11	RO	**Reserved.** Read as zero.	0b	
10	R/W	**Native/AHCI: Tx Continue all the time Enable** When this bit is disable, CONT primitive will be re-generated if ALIGN primitive sent. 0: disable 1: enable	0b	0b
9	R/W	**Native/AHCI: Tx Continue Enable** when this bit is set, CONT primitive is generated if the primitive is repeated for over 3 times, including CONT, HOLD, HOLDA, PMREQ_P, PMREQ_S, R_ERR, R_IP, R_OK, R_RDY, SYNC, WTRM, X_RDY 0: disabled. 1: enabled.	1b	1b

8	R/W	**Native/AHCI: Tx Scramble Enable** When this bit is set, transmitted data scrambled. 0: disabled. 1: enabled.	1b	1b
7	R/W	**Native/AHCI: Automatically set DRQ when DMA data transfer** When this bit is set, DRQ in status shadow register is automatically set to '1' when DMA data transfer. 0: disabled. 1: enabled.	1b	1b
6	R/W	**Native/AHCI: Shadow Register Response Value Control** When this bit is set, the response values of sector count, sector number, cylinder low, cylinder high are all 0's when accessing the device not existed. 0: disabled. 1: enabled.	0b	1b
5:3	R/W	**Reserved.**	111b	
2:0	R/W	**Native/AHCI: Receive Data Buffer Threshold** 000: 11 DW 001: 15 DW 010: 18 DW 011: 21 DW 100: 24 DW 101: 26 DW 110: 28 DW 111: 30 DW	110b	111b

Register 90-93h Miscellaneous Control

Bit	Access	Description	Power On Value	Recom. Setting
31:26	RO	**Reserved.** Read as zero.	000000b	
25	R/W	**Reserved**	1b	
24	R/W	**Reserved**	1b	
23:22	RO	**Reserved. Read as zero.**	00b	
21	R/W	**Native/AHCI:Port 1 Receive BIST FIS Enable** **0: disable** **1:enable**	0b	

20	R/W	**Native/AHCI:Port 0 Receive BIST FIS Enable** **0: disable** **1:enable**	0b	
19:18	RO	**Reserved. Read as zero.**	00b	
17	R/W	**Native/AHCI: Aloop Enable** **0: disable** **1:enable**	0b	
16	R/W	**Native/AHCI:Dloop Enable** **0: disable** **1: enable**	0b	
15:14	RO	**Reserved.** Read as zero.	00b	
13	R/W	**Native/AHCI:Port 1 SATA Channel Device Mode Enable** When this bit is set, the port 1 sata channel Is configured as device mode. 0: disable 1: enable	0b	
12	R/W	**Natvie/AHCI: Port 0 SATA Channel Device Mode Enable** When this bit is set, the port 0 sata channel is configured as device mode. 0:disable 1:enable	0b	
11	R/W	**Reserved.** Read as zero.	0b	
10	R/W	**Native/AHCI: TX 32b40b Input Selection** 0: TX scrambled 32 bit input 1: RX 40 bit to 32 bit input	0b	
8:6	RO	**Reserved.** Read as 101b.	101b	
5:4	R/W	**Native/AHCI:Virtual FIFO Size Selection for Sowtware** 00: full physical size 01:1/2 full physical size 10:1/4 full physical size 11:1/4 full physical size	00b	
3:0	RO	**Reserved.** Read as 000b.	000b	

Register 9C-9Fh SATA PHY Control Register E

Bit	Access	Description	Power On Value	Recom. Setting

31:0	R/W	**SATA PHY Control Register E**	00000000h	

Register A0-A3h SATA PHY Control Register A

Bit	Access	Description	Power On Value	Recom. Setting
31:22	R/W	**SATA PHY Control Register A**	0011100101b	0011100101b
21	R/W	**1.5G/3G switching setting for purpose only** **0: 1.5G** **1:3G**	1b	1b
20	R/W	**SATA PHY Control Register A**	0b	0b
19:0	R/W	**SATA PHY Control Register A**	3b14fh	3b14fh

Register A4-A7h SATA PHY Control Register B

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**SATA PHY Control Register B**	829e2518h	829e2518h

Register A8-ABh SATA PHY Control Register C

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**SATA PHY Control Register C**	4d12401ch	4d12401ch

Register AC-AFh SATA PHY Control Register D

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**SATA PHY Control RegisterD**	02000001h	02000001h

Register B0-B3h Hot Plug Status

Bit	Access	Description	Power On Value	Recom. Setting
31:0	RO	**Reserved.** Read as zero.	00000000h	

Regiser B4-B7h SATA BIST Control Register

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**Reserved.**	00000000h	

Register B8-BBh SATA BIST Control Data A

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**Reserved.**	7F7F7F7Fh	

Register BC-BFh SATA BIST Control Data B

Bit	Access	Description	Power On Value	Recom. Setting
31:0	RW	**Reserved.**	7F7F7F7Fh	

Register C0-C3h 1st SATA Channel SStatus Register

Register D0-D3h 2nd SATA Channel SStatus Register

Bit	Access	Description	Power On Value	Recom. Setting
31:12	RO	**Reserved.** Read as zero.	00000h	
11:8	RO	**Native/AHCI: IPM(Interface Power Management)** 0000: No interface power management state restriction. 0001: Interface in active mode. 0010: Interface in PARTIAL power management mode. 0110: Interface in SLUMBER power management mode.	0000b	
7:4	RO	**Native/AHCI: SPD(Speed Established)** 0000: No speed negotiation restriction. 0001: Limit speed to a rate not greater than Generation 1 communication rate.	0000b	

3:0	RO	**Native/AHCI: DET(Device Detection)** 0000: No device detected and Phy communication not established.. 0001: Device presence detected but Phy communication not established. 0011: Device presence detected but Phy communication established. 0100: PHY in offline mode or running in a BIST loopback mode.	0000b	

Register C4-C7h 1st SATA Channel SError Register

Register D4-D7h 2nd SATA Channel SError Register

Bit	Access	Description	Power On Value	Recom. Setting
31:26	RO	**Reserved.** Read as zero.	000000b	
25	R/WC	**Native/AHCI: Unrecognized FIS Type** 0: normal 1: an unrecognized FIS is received by Transport layer.	0b	
24	R/WC	**Native/AHCI: Transport State Transition Error** 0: normal 1: an transport layer state machine error occurs.	0b	
23	R/WC	**Native/AHCI: Link Sequence Error** 0: normal 1: a linker layer state machine error occurs.	0b	
22	R/WC	**Native/AHCI: Handshake Error** 0: normal 1: an R_ERR primitive is received.	0b	
21	R/WC	**Native/AHCI: CRC Error** 0: normal 1: a CRC error occurs.	0b	
20	R/WC	**Native/AHCI: Disparity Error** 0: normal 1: a disparity error occurs.	0b	
19	R/WC	**Native/AHCI: 10B to 8B Decode Error** 0: normal 1: a 10B to 8B decode error occurs.	0b	

18	R/WC	**Native/AHCI: Comm Wake** 0: normal 1: a Comm Wake signal is detected by Phy.	0b	
17	R/WC	**Native/AHCI: Phy Internal Error** 0: normal 1: an internal error occurred, which comes from phy signal com_err.	0b	
16	R/WC	**Native/AHCI: PhyRdy Chang** 0: normal 1: a PhyRdy signal changes.	0b	
15:10	RO	**Reserved.** Read as zero.	00h	
11	RO	**Native/AHCI: Internal Error.**	0b	
10	R/WC	**Native/AHCI: Protocol Error** 0: normal. 1: a violation of the serial ATA protocol is detected, including transport layer state machine error, linker layer state machine error, unrecognized FIS, or handshake error.	0b	
9	R/WC	**Native/AHCI: Communication Error** 0: normal 1: a communication error occurs, which comes from phy signal com_err.	0b	
8	R/WC	**Native/AHCI: Data Integrity Error** 0: normal 1: a buffer overflow occurs.	0b	
7:2	RO	**Reserved.** Read as zero.	00h	
1	R/WC	**Native/AHCI: Communication Error** 0: normal 1: a communication error occurs, which is phy loses the communication with device.	0b	

0	R/WC	**Native/AHCI: Data Integrity Error** 0: normal 1: a code violation, or a 10b to 8b decode error, or crc error occur.	0b	

Note : Have to write clear SError after COM RESET. (Write 0xffffffffh)

Register C8-CBh 1st SATA Channel SControl Register

Register D8-DBh 2nd SATA Channel SControl Register

Bit	Access	Description	Power On Value	Recom. Setting
31:12	RO	**Reserved.** Read as zero.	00000h	
11:8	R/W	**Native: IPM(Interface Power Management)** 0000: No interface power management state restriction. 0001: Transitions to the PARTIAL power management state disabled. 0010: Transitions to the SLUMBER power management state disabled. 0011: Transitions to the PARTAIL and SLUMBER power management state disabled.	0011b	0011b
7:4	R/W	**Native: SPD(Speed Established)** 0000: No speed negotiation restriction. 0001: Limit speed to a rate not greater than Generation 1 communication rate.	0000b	0000b
3:0	R/W	**Native: DET(Device Detection)** 0000: No device detection or initialization action request. 0001: Hardware reset to establish communication. 0100: Disable SATA and put PHY in offline mode.	0000b	0000b

Note : BIOS can issue a COM RESET by writing bit0 to '1' and then delay some I/O cycles to clear to '0' before BIOS detect HDD sequence.

6.2. PCI Bus Master IDE Control Registers

The PCI Bus master IDE Control Registers locate 16 bytes of I/O Space. These registers can be accessed through I/O R/W to the address defined in the Bus Master IDE control register Base Address. This Base Address is defined in Register 20h-23h of PCI SATA configuration space.

Offset	Register Name	Power On Value	Power Plane
00h	Bus Master Primary IDE Command Register	00h	MAIN
01h	Reserved	00h	MAIN
02h	Bus Master Primary IDE Status Register	00h	MAIN
03h	Reserved	00h	MAIN
04-07h	Bus Master Primary IDE PRD Table Address	00000000h	MAIN
08h	Bus Master Secondary IDE Command Register	00h	MAIN
09h	Reserved	00h	MAIN
0Ah	Bus Master Secondary IDE Status Register	00h	MAIN
0Bh	Reserved	00h	MAIN
0C-0Fh	Bus Master Secondary IDE PRD Table Address	00000000h	MAIN

Regiser 00h Bus Master Primary IDE Command Register

Regiser 08h Bus Master Secondary IDE Command Register

Bit	Access	Description	Power On Value	Recom. Setting
7:4	RO	**Reserved.** Read as zero.	0000b	
3	R/W	**Read or Write Control** This bit defines the R/W control of the bus master transfer. When set as zero, PCI bus master reads are conducted. When set to one, PCI bus master writes are conducted.	0b	
2:1	RO	**Reserved.** Read as zero.	00b	
0	R/W	**Start/Stop Bus Master** Writing a '1' to this bit enables bus master operation of the controller. Bus master operation begins when this bit is detected changing from a zero to a one. The contoller will transfer data between the IDE device and memory only when this bit is set. Master operation can be halt by writing a '0' to this bit.	0b	

Regiser 02h Bus Master Primary IDE Status Register

Regiser 09h Bus Master Secondary IDE Status Register

Bit	Access	Description	Power On Value	Recom. Setting
7	RO	**Native: Simplex Only** This bit is hardwired to zero to indicate that both bus master channels can be operated at a time.	0b	
6	R/W	**Native: Drive 1 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 1 for this channel is capable of DMA transfers.	0b	
5	R/W	**Native: Drive 0 DMA Capable** This R/W bit can be set by BIOS or driver to indicate that drive 0 for this channel is capable of DMA transfers.	0b	
4:3	RO	**Native: Reserved.** Read as zero.	00b	
2	R/WC	**Native: Interrupt** The bit is set by the rising edge of the IDE interrupt line to indicate that all data transferred from the drive is visible in the system memory. Writing a '1' to this bit can reset it.	0b	
1	R/WC	**Native: Error** This bit is set when the IDE controller encounters an error during data transferring to/from memory. Writing a '1' to this bit can reset it.	0b	
0	RO	**Native: Bus Master IDE Device Active** This bit is set when the start bit in the command register is set. It can be cleared when the last transfer of a region is performed, or the start bit is reset.	0b	

Regiser 04-07h Bus Master Primary IDE PRD Table Address

Regiser 0C-0Fh Bus Master Secondary IDE PRD Table Address

Bit	Access	Description	Power On Value	Recom. Setting

31:2	R/W	**Base Address of the PRD Table** This 32-bit register contains address pointing to the starting address of the PRD table.	00000000h	
1:0	RO	**Reserved.** Read as zero.	00b	

6.3. AHCI HBA Memory Registers

The AHCI HBA Memory Control Registers are based from ABAR (AHCI Base Address). These registers can be accessed through Memory R/W only. This AHCI Base Address is defined in Register 24h~27h of PCI D5F0 AHCI configuration space. 968 AHCI limit the register accesses to have a maximum size of 32-bits. 32 bits accesses must not cross a 4-byte alignment boundary. The following table indicate the layout of AHCI HBA Memory Registers.

1, IDE MODE (D2F5 Reg54h[11]) must be set as “1”.

2, Sub Class of SATA enable (D5F0 Reg54h[11]) must set as ‘1’ to make D5F0 be a SATA controller.

3. Memory Space Enable (D5F0 Reg04h[2]) must be set as ‘1’.

4. Allocate memory resource in ABAR.

Offset Start	Offset End	Register Name	Power Plane
00	1B	Generic Host Control	MAIN
1C	9F	Reserved	MAIN
A0	BF	SiS Vendor Specific registers I	MAIN
C0	FF	Reserved	MAIN
100	17F	Port 0 port control registers	MAIN
180	1FF	Port 1 port control registers	MAIN

6.3.1. AHCI Generic Host Control Registers

Offset Start	Offset End	Register Name	Power Plane
00h	03h	Host Capabilities	MAIN
04h	07h	Global Host Control	MAIN
08h	0Bh	Interrupt Status	MAIN
0Ch	0Fh	Ports Implemented	MAIN

10h	13h	Version	MAIN
14h	17h	Command Completion Coalescing Control	MAIN
18h	1Bh	Command Completion Coalsecing Ports	MAIN
A0h	A3h	AHCI SiS Vendor Register I	MAIN
B0h	B3h	AHCI SiS Vendor Register II	MAIN

Register 00h CAP – HBA –Capabilities

Bit	Access	Description	Power On Value	Recom. Setting
31	RO	**Supports 64-bit Addressing (S64A)** Indicates whether the HBA can access 64-bit data structures. SiS1184/1185 doesn't support this feature.	0b	
30	RO	**Supports Native Command Queuing (SNCQ)** Indicates whether the HBA supports Serial ATA native queuing. This bit reflects the value of bit 9 in SiS Vendor Specific registers I. This bit shall be fixed before any AHCI-aware software initializations.	1b	
29	RO	**Supports SNotification Register (SSNTF)** When set to '1', the HBA supports the PxSNTF (SNotification) register and its associated functionality. When cleared to '0', the HBA does not support the PxSNTF (SNotification) register and its associated functionality.	1b	
28	RO	**Supports Interlock Switch(SIS)** Indicates whether the HBA supports interlock switches on its ports for use in hot plug operations. This bit reflects the value of bit 19 in SiS vendor Specific registers I. This value is loaded by the BIOS prior to OS initialization.	0b	
27	RO	**Supports Staggered Spin-up (SSS)** When set to '1', indicates that the HBA supports staggered spin-up on its ports, for use in balancing power spikes. This bit reflects the value of bit 18 in SiS vendor Specific registers I. The value is loaded by the BIOS prior to OS initialization.	0b	

26	RO	**Supports Aggressive Link Power Management (SALP)** When set to '1', indicates that the HBA can support auto-generating link requests to Partial or Slumber states when there are no commands to process. The bit reflects the value of bit 5 in SiS vendor Specific registers I.	1b	
25	RO	**Supports Activity LED (SAL)** When set to '1', indicates that the HBA supports a single output pin which indicates device activity. The bit reflects the value of bit 4 in SiS vendor Specific registers I.	1b	
24	RO	**Supports Command List Override (SCLO)** When set to '1', indicates that the HBA supports the PXCMD.CLO bit and its associated functions. The bit reflects the value of bit 14 in SiS vendor Specific registers I.	0b	
23:20	RO	**Interface Speed Support (ISS)** Indicates the maximum speed the HBA can support in it's port. SiS1184/1185 in SB SiS968 can support speed up to 3Gbps, Gen 2.	0010b	
19	RO	**Supports Non-Zero DMA Offsets (SNZO)** When set to '1', indicates that the HBA can support non-zero DMA offsets for DMA Setup FISes. AHCI 1.0 HBA must have this bit cleared to '0'.	0b	
18	RO	**Supports AHCI mode only (SAM)** The SATA controller may optionally support AHCI access mechanisms only. SiS1184/1185 have value '0' of the bit and could supports AHCI mechanisms (via ABAR) and legacy interfaces, such as SFF-8038i. By setting bit 31(AE) from GHC, SiS1184/1185 could switch the support between above mechanisms and interfaces.	0b	
17	RO	**Supports Port Multiplier (SPM)** Indicates whether the HBA can support a Port Multiplier. When set, a PM using command-based switching is supported. When cleared to '0', a PM is not supported, and a PM may not be attached to this HBA. The bit reflects the value of bit 6 in SiS vendor Specific Registers I.	1b	
16	RO	**Reserved**	0b	

15	RO	**PIO Multiple DRQ Block (PMD)** If set to '1', the HBA supports multiple DRQ block data transfers for PIO command protocol. The bit reflects the value of bit 7 in SiS vendor Specific Registers I.	1b	
14	RO	**Slumber State Capable (SSC)** Indicates whether the HBA can support transitions to the Slumber state. The bit reflects the value of bit 2 in SiS vendor Specific Registers I.	1b	
13	RO	**Partial State Capable (PSC)** Indicates whether the HBA can support transitions to the Partial state. The bit reflects the value of bit 3 in SiS vendor Specific Registers I.	1b	
12:08	RO	**Number of Command Slots (NCS)** 0's based value indicating the number of command slots supported by this HBA. The bit reflects the value of bit 12 ~ bit 8 in SiS vendor Specific Registers II.	11111b	
7:5	RO	**Reserved**	000b	
4:0	RO	**Number of Ports(NP)** 0's based value indicating the maximum number of ports supported. The value is read as 00001.	00001b	

Register 04h GHC – Global HBA Control

Bit	Access	Description	Power On Value	Recom. Setting
31	RW/RO	**AHCI Enable (AE)** When set, indicates that communication to shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy and AHCI mechanisms to know when the HBA I running under an AHCI driver. When set, software shall only communicate with the HBA using AHCI. When cleared, software shall only communicate with HBA using legacy mechanisms. Software shall set this bit to '1' before accessing other AHCI registers. Due the bit value of CAP.SAM zero, GHC.AE shall be read-write and shall have a reset value of '0'.	0b	
30:02	RO	**Reserved**	0h	

01	RW	**Interrupt Enable (IE)** This global bit enables interrupts from the HBA. When cleared, all interrupt sources from all ports are disabled. When set, interrupts are enabled.	0b	
00	RW1	**HBA Reset (HR)** When set by SW, this bit causes an internal reset of HBA. All states will return to IDLE and all ports shall be re-initialized via COMRESET (if staggered spin-up is not supported). If staggered spin-up is supported, then it is the responsibly of software to spin-up each port after reset has completed. When the HBA has completed the reset, it shall reset the bit to '0'. A write of '0' shall have no effect.	00001b	

Register 08h IS – Interrupt Status Register

Bit	Access	Description	Power On Value	Recom. Setting
31:00	RWC	**Interrupt Pending Status (IPS)** If set, indicates that the corresponding port has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. Bit 1~0 is corresponded to the interrupt pending status of port 1 to port 0. All other bits are reserved.	00000000h	

Register 0Ch PI – Ports Implemented

Bit	Access	Description	Power On Value	Recom. Setting
31:00	RO	**Port Implemented (PI)** This register is bit significant. If a bit is set to '1', the corresponding port is available for software to use. If cleared, the port is not available for software to use. To SiS968, the field is 3h.	00000003h	

Register 10h VS – AHCI Version

Bit	Access	Description	Power On Value	Recom. Setting

31:16	RO	**Major Version Number (MJR)** Indicates the major version is “1” .	0001h	
15:0	RO	**Major Version Number (MNR)** Indicates the minor version is “10” .	0100h	

Register 14h CCC_CTL – Command Completion Coalescing Control

Bit	Access	Description	Power On Value	Recom. Setting
31:16	R/w	**Timeout Value (TV)** The timeout value is specified in 1 millisecond intervals. The timer accuracy shall be within 5%. hCccTimer is loaded with this timeout value. hCccTimer is only decremented when commands are outstanding on selected ports. The HBA will signal a CCC interrupt when hCccTimer has decremented to ‘0’. hCccTimer is reset to the timeout value on the assertion of each CCC interrupt. A timeout value of ‘0’ is reserved.	1b	
15:8	R/W	**Command Completions (CC)** Specifies the number of command completions that are necessary to cause a CCC interrupt. The HBA has an internal command completion counter, hCccComplete. hCccComplete is incremented by one each time a selected port has a command completion. When hCccComplete is equal to the command completions value, a CCC interrupt is signaled. The internal command completion counter is reset to ‘0’ on the assertion of each CCC interrupt. A value of ‘0’ for this field shall disable CCC interrupts being generated based on the number of commands completed, i.e. CCC interrupts are only generated based on the timer in this case.	1b	
7:3	RO	**Interrupt (INT)** Specifies the interrupt used by the CCC feature. This interrupt must be marked as unused in the Ports Implemented (PI) register by the corresponding bit being set to ‘0’. Thus, the CCC interrupt corresponds to the interrupt for an unimplemented port on the controller. When a CCC interrupt occurs, the IS.IPS[INT] bit shall be asserted to ‘1’. This field also specifies the interrupt vector used for MSI.	11111b	
2:1	RO	**Reserved**	00b	

0	R/W	**Enable (EN)** When cleared to '0', the command completion coalescing feature is disabled and no CCC interrupts are generated. When set to '1', the command completion coalescing feature is enabled and CCC interrupts may be generated based on timeout or command completion conditions. Software shall only change the contents of the TV and CC fields when EN is cleared to '0'. On transition of this bit from '0' to '1', any updated values for the TV and CC fields shall take effect.	0b	

Register 18h CCC_PORTS – Command Completion Coalescing Ports

Bit	Access	Description	Power On Value	Recom. Setting
31:00	R/W	**Ports (PRT)** This register is bit significant. Each bit corresponds to a particular port, where bit 0 corresponds to port 0. If a bit is set to '1', the corresponding port is part of the command completion coalescing feature. If a bit is cleared to '0', the port is not part of the command completion coalescing feature. Bits set to '1' in this register must also have the corresponding bit set to '1' in the Ports Implemented register. An updated value for this field shall take effect within one timer increment (1 millisecond).	00000000h	

AHCI SiS Vendor Registers

Register A0-A3h SVSR1 – SiS Vendor Specific registers I

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**AHCI SiS Vendor Register I**	0000827fh	01b0ffd3h

Register B0-B3h SVSR1 – SiS Vendor Specific registers I

Bit	Access	Description	Power On Value	Recom. Setting
31:0	R/W	**AHCI SiS Vendor Register II**	3000ffc0h	3000ffe0h

6.3.2. AHCI Port Registers

Table: Port DMA Register Address Map

X = {0,1}

Address Offset:

Port 0: ABAR + 100h

Port 1: ABAR + 180h

Offset Start	Offset End	Register Name	Power Plane
00	03	Port X Command List Base Address	MAIN
04	07	Port X Command List Base Address Upper 32-Bits	MAIN
08	0B	Port X FIS Base Address	MAIN
0C	OF	Port X FIS Base Address Upper 32-Bits	MAIN
10	13	Port X interrupt Status	MAIN
14	17	Port X Interrupt Enable	MAIN
18	1B	Port X Command	MAIN
1C	1F	Reserved	MAIN
20	23	Port X Task File Data	MAIN
24	27	Port X Signature	MAIN
28	2B	Port X Serial ATA Status	MAIN
2C	2F	Port X Serial ATA Control	MAIN
30	33	Port X Serial ATA Error	MAIN
34	37	Port X Serial ATA Active	MAIN
38	3B	Port X Serial ATA Issue	MAIN
3C	7F	Reserved	MAIN

Register Offset 00h PXCLB – Port [1:0] Command List Base Address

Bit	Access	Description	Power On Value	Recom. Setting
31:10	RW	**Command List Base Address (CLB)** Indicates the 32-bit base physical address for the command list for this port. This base is used when fetching commands to execute. The structure pointed to by this address is 1K-bytes in length. This address must be 1K-byte aligned as indicated by bits 09:00 being read only.	0000001h	
9:0	RO	**Reserved**	00h	

Register Offset 04h PXCLBU – Port [1:0] Command List Base Address Upper 32-bits

Bit	Access	Description	Power On Value	Recom. Setting
31:0	RW	**Command List Base Address Upper (CLBU)** Reserved. SiS AHCI controller doesn't 64-bit addressing.	00000000h	

Register Offset 08h PXFB – Port [1:0] FIS Base Address

Bit	Access	Description	Power On Value	Recom. Setting
31:08	RW	**FIS Base Address (CLB)** Indicates the 32-bit base physical address for receiving FISes. The structure pointed to by this address range is 256 bytes in length. This address must be 256-byte aligned as indicated by bits 07:00 being read only.	0000000h	
7:0	RO	**Reserved**	00h	

Register Offset 0ChPXFBU – Port [1:0] FIS Base Address Upper 32-bits

Bit	Access	Description	Power On Value	Recom. Setting
31:0	RW	**FIS Base Address Upper (FBU)** Reserved. SiS AHCI controller doesn't 64-bit addressing.	0001h	

Register Offset 10h PXIS – Port [1:0] Interrupt Status

Bit	Access	Description	Power On Value	Recom. Setting
31	RO	**Cold Port Detect Status (CPDS)** Reserved. SIS AHCI controller doesn't support this feature.	0b	
30	RWC	**Task File Error Status (TFES)** This bit is set whenever the status register is updated by the device and the error bit is set.	0b	

29	RWC	**Host Bus Fatal Error Status (HBFS)** Indicates that the HBA encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, such an indication would be a target or master or target abort.	0b	
28	RWC	**Host Bus Data Error Status (HBDS)** Indicates that the HBA encountered a data error (uncorrectable ECC/parity) when reading from or write to system memory.	0b	
27	RWC	**Interface Fatal Error Status (IFS)** Indicates that HBA encountered an error on the SATA interface which caused the transfer to stop.	0b	
26	RWC	**Interface Non-fatal Error Status (INFS)** Indicates that the HBA encountered an error on the SATA interface but was able to continue operation.	0b	
25	RWC	**Reserved**	0b	
24	RWC	**Overflow Status (OFS)** Indicates that the HBA received more bytes from a device than was specified in the PRD table for the command.	0b	
23	RWC	**Incorrect Port Multiplier Status (IPMS)** Indicates that the HBA received a FIS from device whose Port Multiplier field did not match what was excepted.	0b	
22	RWC	**PhyRdy Change Status (PRCS)** When set to '1' indicates the internal PhyRdy signal changed state. This bit reflects the state of P0SERR.DIAG.N. To clear this bit software must clear P0SERR.DIAG.N to '0'.	0b	
21:08	RO	**Reserved**	0b	
07	RWC	**Device Interlock Status (DIS)** When set, indicated that an interlock switch attached to this port has been opened or close, which may lead to a change in connection state of the device. This bit is only valid if both CAP.SIS and P0CMD.ISP are set to '1'.	0b	
06	RO	**Port Connect Change Status (PCS)** This bit reflects the state of PXSERR.DIAG.X. The bit is only cleared when PXSERR.DIAG.X is cleared.	0b	

05	RWC	**Descriptor Processed (DPS)** A PRD with the 'I' bit set has transferred all of its data.	0b	
04	RO	**Unknown FIS Interrupt (UFS)** When set to '1', indicates that an unknown FIS was received and has been copied into system memory. This bit is cleared to '0' by software clearing the PXSERR.DIAG.F to '0'. Note that this bit does not directly reflect the PXSERR.DIAG.F bit. PxSERR.DIAG.F is set immediately when an unknown FIS is detected, whereas this bit is set when that FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to '1' or the two bits may become out of sync.	0b	
03	RWC	**Set Device Bits Interrupt (SDBS)** A Set Device Bits FIS has been received with the 'I' bit set and has been copied into system memory.	0b	
02	RWC	**DMA Setup Bits Interrupt (DSS)** A DMA Setup Setup FIS has been received with the 'I' bit set and has been copied into system memory.	0b	
01	RWC	**PIO Setup FIS Interrupt (PSS)** A PIO Setup FIS has been received with the 'I' bit set and has been copied into system memory.	0b	
00	RW	**Device to Host Register FIS Interrupt (DHRS)** A D2H Register FIS has been received with the 'I' bit set and has been copied into system memory.	0b	

Register Offset 14h PXIE – Port [1:0] Interrupt Enable

Bit	Access	Description	Power On Value	Recom. Setting
31	RO	**Cold Port Detect Enable (CPDE)** Reserved. SIS AHCI controller doesn't support this feature.	0b	
30	RW	**Task File Error Enable (TFEE)** When set, GHC.IE is set, and PXIS.TFES is set, the HBA shall generate an interrupt..	0b	
29	RW	**Host Bus Fatal Error Enable (HBFE)** When set, GHC.IE is set, and PXIS.HBFS is set, the HBA shall generate an interrupt..	0b	

28	RW	**Host Bus Data Error Enable (HBDE)** When set, GHC.IE is set, and PXIS.HBDS is set, the HBA shall generate an interrupt..	0b	
27	RW	**Interface Fatal Error Enable (IFE)** When set, GHC.IE is set, and PXIS.IFS is set, the HBA shall generate an interrupt..	0b	
26	RW	**Interface Non-fatal Error Enable (INFE)** When set, GHC.IE is set, and PXIS.INFS is set, the HBA shall generate an interrupt..	0b	
25	RW	**Reserved**	0b	
24	RW	**Overflow Enable (OFE)** When set, GHC.IE is set, and PXIS.OFS is set, the HBA shall generate an interrupt..	0b	
23	RW	**Incorrect Port Multiplier Enable (IPME)** When set, GHC.IE is set, and PXIS.IPMS is set, the HBA shall generate an interrupt..	0b	
22	RW	**PhyRdy Change Interrupt Enable (PRCE)** When set, GHC.IE is set, and PXIS.PRCS is set, the HBA shall generate an interrupt..	0b	
21:08	RO	**Reserved**	0b	
07	RW	**Device Interlock Enable (DIE)** When set, GHC.IDE is set, and PXIS.DIS is set, the HBA shall generate an interrupt. For systems that do not support an interlock switch, this bit shall be a read-only '0'.	0b	
06	RO	**Port Change Interrupt Enable (PCE)** When set, GHC.IE is set, and PXIS.PCS is set, the HBA shall generate an interrupt..	0b	
05	RWC	**Descriptor Processed Interrupt Enable (DPE)** When set, GHC.IE is set, and PXIS.DPS is set, the HBA shall generate an interrupt..	0b	
04	RO	**Unknown FIS Interrupt Enable (UFE)** When set, GHC.IE is set, and PXIS.UFS is set, the HBA shall generate an interrupt..	0b	
03	RWC	**Set Device Bits Interrupt Enable (SDBE)** When set, GHC.IE is set, and PXIS.SDBS is set, the HBA shall generate an interrupt..	0b	
02	RWC	**DMA Setup Bits Interrupt Enable (DSE)** When set, GHC.IE is set, and PXIS.DSS is set, the HBA shall generate an interrupt..	0b	
01	RWC	**PIO Setup FIS Interrupt Enable (PSE)** When set, GHC.IE is set, and PXIS.PSS is set, the HBA shall generate an interrupt..	0b	

00	RW	**Device to Host Register FIS Interrupt Enable (DHRE)** When set, GHC.IE is set, and PXIS.DHRS is set, the HBA shall generate an interrupt..	0b	

Register Offset 18h PXCMD – Port [1:0] Command Register

Bit	Access	Description	Power On Value	Recom. Setting
31:28	RW	**Interface Communication Control (ICC)** This is a four bit field which can be used to control reset and power states of the interface. Writes to this field will cause actions on the interface. Either as primitives or an OOB sequence, and the resulting status of the interface will be reported in the PXSSTS register. **Value Definition** Fh – 7h Reserved 6h **Slumber**: This will cause the HBA to request a transition of the interface to Slumber state. The SATA device may reject the request and the interface shall remain in its current state. 5h – 3h Reserved 2h **Partial**: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state. 1h **Active**: This shall cause the HBA to request a transition of the interface into the active state. 0h **No-Op** / **Idle**: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not yet have occurred. When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state. **NOTE:** When the APLE bit (bit 26) is set, then this register should not be set to 02h or 06h.	0b	

27	RW/ RO	**Aggressive Slumber / Partial (ASP)** When set to '1', and ALPE is set, the HBA shall aggressively enter the Slumber state when it clears the PxCI register and the PxSACT register is cleared or when it clears the PxSACT register and PxCI is cleared. When cleared, and ALPE is set, the HBA shall aggressively enter the Partial state when it clears the PxCI register and the PxSACT register is cleared or when it clears the PxSACT register and PxCI is cleared. If CAP.SALP is cleared to '0' software shall treat this bit as reserved.	0b	
26	RW/ RO	**Aggressive Link Power Management Enable (ALPE)** When set to '1', the HBA shall aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. Software shall only set this bit to '1' if CAP.SALP is set to '1'; if CAP.SALP is cleared to '0' software shall treat this bit as reserved.	0b	
25	RW	**Drive LED on ATAPI Enable (DLAE)** When set to '1', the HBA shall drive the LED pin active for commands regardless of the state of P0CMD.ATAPI. When cleared, the HBA shall only drive the LED pin active for commands if P0CMD.ATAPI set to '0'.	0b	1b
24	RW	**Device is ATAPI (ATAPI)** When set to '1', the connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.	0b	
23:20	RO	**Reserved**	0000b	
19	RO	**Interlock Switch Attached to Port (ISP)** If set to '1', the platform supports an interlocked switch attached to this port. If cleared to '0', the platform does not support an interlocked switch attached to this port. When this bit is set to '1', P0CMD.HPCP should also be set to '1'. **Note: The bit is reflected by the value of bit 25,22 in SVSR1 for P1CMD.ISP and P0CMD.ISP.**	0b	

18	RO	**Hot Plug Capable Port (HPCP)** **0 = Port is not capable of Hot-Plug.** **1= Port is Hot-Plug capable.** This indicates whether the platform exposes this port to a device which can be Hot-Plugged. SATA by definition is hot=pluggable, but not all platforms are constructed to allow the device to be removed (if may be screwed into the chassis, for example). This bit can be used by system software to indicate a feature such as "eject device" to the end –user. The SiS968 takes no action in the state of this bit – it's for system software only. For example, if this bit is cleared, and a Hot-Plug event occurs, the SiS968 still treats it as a proper Hot-Plug event. **Note: The bit is reflected by the value of bit 24,21 in SVSR1 for P1CMD.HPCP and P0CMD.HPCP.**	0b	
17	RW	**Port Multiplier Attached (PMA)** This bit is read/write for HBAs that support a Port Multiplier (CAP.SPM = '1'). This bit is read-only for HBAs that do not support a port Multiplier (CAP.SPM = '0'). When set to '1' by software, a Port Multiplier is attached to the HBA for this port. When cleared to '0' by software, a Port Multiplier is not attached to the HBA for this port. Software is responsible for detecting whether a Port Multiplier is present; hardware does not auto-detect the presence of a Port Multiplier.	0b	
16	RO	**Reserved**	0b	
15	RO	**Command List Running (CR)** When this bit is set, the command list DMA engine for the port is running.	0b	
14	RO	**FIS Receive Running (FR)** When set, the FIS Receive DMA engine for the port is running.	0b	
13	RO	**Interlock Switch State (ISS)** The ISS bit reports the state of an interlocked switch attached to this port. If CAP.SIS is set to '1' and the interlocked switch is closed then this bit is cleared to '0'. If CAP.SIS is set to '1' and the interlocked switch is open then this bit is set to '1'. If CAP.SIS is set to '0' then this bit is cleared to '0'. Software should only use this bit if both CAP.SIS and P0CMD.ISP are set to '1'.	0b	

12:08	RO	**Current Command Slot (CCS)** This field is valid when P0CMD.ST is set to '1' and shall be set to the command slot value of the command that is currently being issued by the HBA. When P0CMD.ST transitions from '1' to '0', this field shall be reset to '0'. After P0CMD.ST transitions from '0' to '1', the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is P0CMD.CCS + 1. For example, after the HBA has issued its first command, if CCS = 0h and P0CI is set to 3h, the next command that will be issued is from command slot 1.	0h	
07:05	RO	**Reserved**		
04	RW	**FIS Receive Enable (FRE)** When set, the HBA may post received FISes into the FIS receive area pointed to by PxFB (and for 64-bit HBAs, PxFBU). When cleared, received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. System software must not set this bit until PxFB (PxFBU) have been programmed with a valid pointer to the FIS receive area, and if software wishes to move the base, this bit must first be cleared, and software must wait for the FR bit in this register to be cleared.	0b	
03	RW1	**Command List Override (CLO)** Setting this bit to '1' causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to '0'. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to '0' when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to '0'. A write to this register with a value of '0' shall have no effect. This bit shall only be set to '1' immediately prior to setting the PxCMD.ST bit to '1' from a previous value of '0'. Setting this bit to '1' at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to '0' before setting PxCMD.ST to '1'.	0b	

02	RO	**Power On Device (POD)** Because SiS968 doesn't support cold presence detection, this bit is read only '1'.	0b	
01	RW	**Spin-Up Device (SUD)** This bit is read/write for HBAs that support staggered spin-up via CAP.SSS. This bit is read only '1' for HBAs that do not support staggered spin-up. On an edge detect from '0' to '1', the HBA shall start a COMRESET initializatoin sequence to the device. Clearing this bit to '0' does not cause any OOB signal to be sent on the interface. When this bit is cleared to '0' and PxSCTL.DET=0h, the HBA will enter listen mode.	1b	
00	RW	**Start (ST)** When set, the HBA may process the command list. When cleared, the HBA may not process the command list. Whenever this bit is changed from a '0' to a '1', the HBA starts processing the command list at entry '0'. Whenever this bit is changed from a '1' to a '0', the PxCI register is cleared by the HBA upon the HBA putting the controller into an idle state. This bit shall only be set to '1' by software after PxCMD.FRE has been set to '1'.	0b	

Register Offset 20h PXTFD – Port [1:0] Task File Data Register

This is a 32-bit register that copies specific fields of the task file when FISes are received.

The FISes that contain this information are:

- D2H Register FIS
- PIO Setup FIS
- Set Device Bits FIS (BSY and DRQ are not updated with this FIS)

Bit	Access	Description	Power On Value	Recom. Setting
31:16	RO	**Reserved**	0h	
15:08	RO	**Error (ERR)** Contains the latest copy of the task file error register.	0h	

07:00	RO	**Status (STS)** Contains the latest copy of the task file status register. Fields of note in this register that affect AHCI hardware operation are:	7Fh	

Bit	Field	Definition
7	BSY	Indicates the interface is busy
6:4	N/A	Not Applicable
3	DRQ	Indicates a data transfer is requested
2:!	N/A	Not Applicable
0	ERR	Indicates an error during the transfer

Register Offset 24h PXSIG – Port [1:0] Signature

Bit	Access	Description	Power On Value	Recom. Setting
31:00	RO	**Signature (SIG)** Contains the signature received from a device on the first D2H Register FIS. The bit order is as follows:	FFFFFFFFh	

Bit	Field
31:24	LBA High Register
23:16	LBA Mid Register
15:08	LBA Low Register
07:00	Sector Count Register

Register Offset 28h PXSTS – Port [1:0] Serial ATA Status (SCR0: SStatus)

This is a 32-bit register that conveys the current state of the interface and host. The HBA updates it continuously and asynchronously. When the HBA transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Type	Reset	Description
31:12	*RO*	*0*	*Reserved*
11:08	RO	0	**Interface Power Management (IPM):** Indicates the current interface state: 0h Device not present or communication not established 1h Interface in active state 2h Interface in Partial power management state 6h Interface in Slumber power management state All other values reserved

07:04	RO	0	**Current Interface Speed (SPD):** Indicates the negotiated interface communication speed. 0h Device not present or communication not established 1h Generation 1 communication rate negotiated 2h Generation 2 communication rate negotiated All other values reserved
03:00	RO	0	**Device Detection (DET):** Indicates the interface device detection and Phy state. 0h No device detected and Phy communication not established 1h Device presence detected but Phy communication not established 3h Device presence detected and Phy communication established 4h Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved

Register Offset 2ChPXSCTL – Port [1:0] Serial ATA Control (SCR2: SControl)

This is a 32-bit read-write register by which software controls SATA capabilities. Writes to this register result in an action being taken by the host adapter or interface. Reads from the register return the last value written to it.

Bit	Type	Reset	Description
31:20	*RO*	*0*	*Reserved*
19:16	*RO*	*0h*	*Port Multiplier Port (PMP): This field is not used by AHCI.*
15:12	*RO*	*0h*	*Select Power Management (SPM): This field is not used by AHCI*
11:08	RW	0h	**Interface Power Management Transitions Allowed (IPM):** Indicates which power states the HBA is allowed to transition to. If an interface power management state is disabled, the HBA is not allowed to initiate that state and the HBA must PMNAK$_P$ any request from the device to enter that state. 0h No interface restrictions 1h Transitions to the Partial state disabled 2h Transitions to the Slumber state disabled 3h Transitions to both Partial and Slumber states disabled All other values reserved

07:04	RW	0h	**Speed Allowed (SPD):** Indicates the highest allowable speed of the interface. 0h No speed negotiation restrictions 1h Limit speed negotiation to Generation 1 communication rate 2h Limit speed negotiation to a rate not greater than Generation 2 communication rate All other values reserved
03:00	RW	0h	**Device Detection Initialization (DET):** Controls the HBA's device detection and interface initialization. 0h No device detection or initialization action requested 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h Disable the Serial ATA interface and put Phy in offline mode. All other values reserved This field may only be modified when P0CMD.ST is '0'. Changing this field while the P0CMD.ST bit is set to '1' results in undefined behavior. When P0CMD.ST is set to '1', this field should have a value of 0h. Note: It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.

Register Offset 30h PXSERR – Port [1:0] Serial ATA Error (SCR1: SError)

Bit	Type	Reset	Description

<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>31:16</td><td>RWC</td><td>0000h</td><td>Diagnostics (DIAG) - Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes:

<table>
<tr><td>31:27</td><td>Reserved</td></tr>
<tr><td>26</td><td>Exchanged (X): When set to one this bit indicates a COMINIT signal was received. This bit is reflected in the P0IS.PCS bit.</td></tr>
<tr><td>25</td><td>Unknown FIS Type (F): Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known.</td></tr>
<tr><td>24</td><td>Transport state transition error (T): Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.</td></tr>
<tr><td>23</td><td>Link Sequence Error (S): Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition.</td></tr>
<tr><td>22</td><td>Handshake Error (H): Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.</td></tr>
<tr><td>21</td><td>CRC Error (C): Indicates that one or more CRC errors occurred with the Link Layer.</td></tr>
<tr><td>20</td><td>Disparity Error (D): This field is not used by AHCI.</td></tr>
<tr><td>19</td><td>10B to 8B Decode Error (B): Indicates that one or more 10B to 8B decoding errors occurred.</td></tr>
<tr><td>18</td><td>Comm Wake (W): Indicates that a Comm Wake signal was detected by the Phy.</td></tr>
<tr><td>17</td><td>Phy Internal Error (I): Indicates that the Phy detected some internal error.</td></tr>
<tr><td>16</td><td>PhyRdy Change (N): Indicates that the PhyRdy signal changed state. This bit is reflected in the P0IS.PRCS bit.</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>15:00</td><td>RWC</td><td>0000h</td><td>Error (ERR): The ERR field contains error information for use by host software in determining the appropriate response to the error condition.

<table>
<tr><td>15:12</td><td>Reserved</td></tr>
<tr><td>11</td><td>Internal Error (E): The host bus adapter experienced an internal error that caused the operation to fail and may have put the host bus adapter into an error state. The internal error may include a master or target abort when attempting to access system memory, an elasticity buffer overflow, a primitive mis-alignment, a synchronization FIFO overflow, and other internal error conditions. Typically when an internal error occurs, a non-fatal or fatal status bit in the PxIS register will also be set to give software guidance on the recovery mechanism required.</td></tr>
<tr><td>10</td><td>Protocol Error (P): A violation of the Serial ATA protocol was detected.</td></tr>
<tr><td>9</td><td>Persistent Communication or Data Integrity Error (C): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.</td></tr>
<tr><td>8</td><td>Transient Data Integrity Error (T): A data integrity error occurred that was not recovered by the interface.</td></tr>
<tr><td>7:2</td><td>Reserved</td></tr>
<tr><td>1</td><td>Recovered Communications Error (M): Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.</td></tr>
<tr><td>0</td><td>Recovered Data Integrity Error (I): A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.</td></tr>
</table>
</td></tr>
</table>

Register Offset 34h PXSACT – Port [1:0] Serial ATA Active (SCR3: SActive)

Bit	Access	Description	Power On Value	Recom. Setting
31:00	R/W1	**Device Status (DS)** This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. This field is set by software prior to issuing a native queued command for a particular command slot. Prior to writing PxCI[TAG] to '1', software will set DS[TAG] to '1' to indicate that a command with that TAG is outstanding. The device clears bits in this field by sending a Set Device Bits FIS to the host. The HBA clears bits in this field that are set to '1' in the SActive field of the Set Device Bits FIS. The HBA only clears bits that correspond to native queued commands that have completed successfully. Software should only write this field when PxCMD.ST is set to '1'. This field is cleared when PxCMD.ST is written from a '1' to a '0' by software. This field is not cleared by a COMRESET or a software reset.	00000000h	

Register Offset 38h PXCI – Port [1:0] Command Issue

Bit	Access	Description	Power On Value	Recom. Setting
31	R/W1	**Command Issued (CI)** This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to '1' by software when PxCMD.ST is set to '1'. This field is also cleared when PxCMD.ST is written from a '1' to a '0' by software.	00000000h	

7. PCI Express Root Complex Port (Device6/7:Function0)Registers Summary and Description

7.1. PCI Express Root Complex Port Registers Summary (Device 6 and 7, Function 0)

7.1.1. PCI Express Root Complex Configuration Space Header Registers

REG	Register Name	Power On Value	Access Type	Power Plane
00-01h	Manufacturer's Vender ID	1039h	RO	MAIN
02-03h	Device ID	000Ah	RO	MAIN
04-05h	Command Register	0000h	RO RW	MAIN
06-07h	Status Register	0010h	RO R/WC	MAIN
08h	Revision Identification Register	00h	RO	MAIN
09-0Bh	Class Code Register	060400h	RO	MAIN
0Ch	Cache Line Size Register	00h	RW	MAIN
0Dh	Memory Latency Timer Register	00h	RO	MAIN
0Eh	Header Type Register	01h	RO	MAIN
0Fh	BIST Register	00h	RO	MAIN
10-17h	Memory Base Address Register	0	RO	MAIN
18h	Primary Bus Number	00h	RO	MAIN
19h	Secondary Bus Number	00h	RW	MAIN
1Ah	Subordinate Bus Number	00h	RW	MAIN
1Bh	Secondary Latency Timer	00h	RO	MAIN
1Ch	I/O Base Register	F1h	RW RO R/WO	MAIN
1Dh	I/O Limit Register	01h	RW RO R/WO	MAIN
1E-1Fh	Secondary Status Register	0000h	RO R/WC	MAIN
20-21h	Memory Base Register	FFF0h	RW RO	MAIN

22-23h	Memory Limit Register	0000h	RO RW	MAIN
24-25h	Prefetchable Memory Base Register	FFF1h	RO RW R/WO	MAIN
26-27h	Prefetchable Memory Limit Register	0001h	RO RW R/WO	MAIN
28-2Bh	Prefetchable Base Upper 32 Bits Register	0	RW	MAIN
2C-2Fh	Prefetchable Limit Upper 32 Bits Register	0	RW	MAIN
30-31h	I/O Base Upper 16 Bits Register	0000h	RW	MAIN
32-33h	I/O Limit Upper 16 Bits Register	0000h	RW	MAIN
34h	Capabilities Pointer	B0h	R/WO	MAIN
35-3Bh	Reserved	0	RO	MAIN
3Ch	Interrupt Line Register	00h	RW	MAIN
3Dh	Interrupt Pin Register	01h	RO R/WO	MAIN
3E	Bridge Control	00h	RO RW	MAIN
3F	Reserved	0	RO	MAIN

7.1.2. PCI Express Capability Register

REG	Register Name	Power On Value	Access Type	Power Plane
B0-B3h	Subsystem Vendor Capability Register	0000C00Dh	RO R/WO	MAIN
B4- B7h	Subsystem Vendor Identification Register	00000000h	R/WO	MAIN
C0-C3h	MSI Capability Register	0000D005h	RO R/W R/WO	MAIN
C4-C7h	Message Address Register	00000000h	RO R/W	MAIN
C8-CBh	Message Upper Address Register	00000000h	R/W	MAIN
CC-CFh	Message Data Register	00000000h	RO R/W	MAIN

D0-D3h	PCI Express Capability Register	0141F410h	RO R/WO	MAIN
D4-D7h	Device Capabilities Register	00000020h	RO R/WO	MAIN
D8-D9h	Device Control Register	0810h	RO R/W R/WS	MAIN AUX
DA-DBh	Device Status Register	0010h	RO R/WC	MAIN
DC-DFh	Link Capabilities Register	0000CC11h	RO R/WO	MAIN
E0-E1h	Link Control Register	0000h	RO R/W R/WO	MAIN
E2-E3h	Link Status Register	1011h	RO R/WO	MAIN
E4-E7h	Slot Capabilities Register	00000000h	RO R/WO	MAIN
E8-E9h	Slot control Register	03C0h	RO R/W	MAIN
EA-EBh	Slot Status Register	0040h	RO R/WC	MAIN
EC-EFh	Root Control Register	00000000h	RO R/W	MAIN
F0-F3h	Root Status Register	00000000h	RO R/WC	MAIN

7.1.3. PCI Express Power Management Register

REG	Register Name	Power On Value	Access Type	Power Plane
F4h-F7h	Power Management Capability Register	C8020001h	RO R/WO	MAIN
F8h-FBh	Power Management Status/Control Register	00000000h	RO R/W R/WS R/WCS	MAIN AUX

7.1.4. PCI Express Extended Register

REG	Register Name	Power On Value	Access Type	Power Plane
100-103h	Virtual Channel Enhanced Capability Header	13010002h	RO R/WO	MAIN
104-107h	Port VC Capability Register 1	00000000h	RO	MAIN
108-10Bh	Port VC Capability Register 2	00000000h	RO	MAIN
10C-10Dh	Port VC Control Register	0000h	RO R/W	MAIN
10E-10Fh	Port VC Status Register	0000h	RO	MAIN
110-113h	VC0 Resource Capability Register	00000000h	RO R/WO	MAIN
114-117h	VC0 Resource Control	800000FFh	RO R/W	MAIN
118-12Fh	Reserved	0	RO	MAIN
130-133h	Advanced Error Reporting Enhanced Capability Header	00010001h	RO R/WO	MAIN
134-137h	Uncorrectable Error Status Register	00000000h	RO R/WCS	MAIN AUX
138-13Bh	Uncorrectable Error Mask Register	00000000h	RO R/WS	MAIN AUX
13C-13Fh	Uncorrectable Error Severity Register	00062011h	RO R/WS	MAIN AUX
140-143h	Correctable Error Status Register	00000000h	RO R/WCS	MAIN AUX
144-147h	Correctable Error Mask Register	00000000h	RO R/WS	MAIN AUX
148-14Bh	Advanced Error Capabilities and Control Register	00000000h	RO ROS R/WS	MAIN AUX
14C-15Bh	Reserved	0	RO	MAIN
15C-15FH	Root Error Command Register	00000000h	RO R/W	MAIN
160-163h	Root Error Status Register	00000000h	RO R/WCS	MAIN AUX

164-167h	Error Source Identification Register	00000000h	ROS	AUX

Supplementary Note:

(1.1) – Apply for PCI Express Specification Rev. 1.1 only

(1.0) – Apply for PCI Express Specification Rev. 1.0 only

7.2. PCI Express Root Complex Port Registers Descriptions (Device 6 and 7, Function 0)

Register 00-01h Manufacturer's Vendor ID

Default Value : 1039h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:0	RO	**Vendor Identification Number** This field identifies the manufacturer of the device. SiS is allocated as 1039h by PCI-SIG.	1039h	

Register 02-03h Device ID

Default Value : 000Ah

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:0	RO	**Device Identification Number** The device identifier is allocated as 000Ah by Silicon Integrated System Corp.	000Ah	

Register 04-05h Command Register

Default Value : 0000h Recommend setting : 0007h

Access Type : Read-Only, Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:11	RO	**Reserved**	0	
10	R/W	**Interrupt Disable** Control the ability of a PCI Express device to generate INTx interrupt Messages. 0: enable 1: disable	0b	0b
9	RO	**Fast Back-to-Back Transactions Enable** Does not apply to PCI Express. Must be hardwired to 0.	0b	
8	R/W	**SERR# Enable** This bit, when set, enables transmission by the primary interface of ERR_NONFATAL and ERR_FATAL error messages forwarded from the secondary interface. 0: disable 1: enable	0b	0b
7	RO	**IDSEL Stepping / Wait Cycle Control** Does not apply to PCI Express. Must be hardwired to 0.	0b	
6	RW	**Parity Error Response** A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.	0b	0b
5	RO	**VGA Palette Snoop** Does not apply to PCI Express. Must be hardwired to 0.	0b	
4	RO	**Memory Write and Invalidate** Does not apply to PCI Express. Must be hardwired to 0.	0b	
3	RO	**Special Cycle** Does not apply to PCI Express. Must be hardwired to 0.	0b	
2	R/W	**Bus Master Enable** This bit controls the ability of a PCI Express Endpoint to issue Memory and I/O Read/Write Requests, and the ability of a Root or Switch Port to forward Memory and I/O Read/Write Requests in the upstream direction. 0: disable 1: enable	0b	1b

1	R/W	**Memory Space Enable** This bit controls the device's response to Memory Space accesses. 0: disable 1: enable	0b	1b
0	R/W	**I/O Space Enable** This bit controls the device's response to I/O Space accesses. 0: disable 1: enable	0b	1b

Register 06-07h Status Register

Default Value : 0010h

Access Type : Read-Only, Read/Write Clear

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15	R/WC	**Detected Parity Error** This bit is set by a device whenever it receives a Poisoned TLP, regardless of the state the Parity Error Enable bit in the Command register.	0b	
14	R/WC	**Signaled System Error** This bit is set when a device sends an ERR_FATAL or ERR_NONFATAL Message, and the SERR# Enable bit in the Command register is 1.	0b	
13	R/WC	**Received Master Abort** This bit is set when a Requestor receives a Completion with Unsupported Request Completion Status.	0b	
12	R/WC	**Received Target Abort** This bit is set when a Requestor receives a Completion with a Completion with Completer Abort Completion Status.	0b	
11	R/WC	**Signaled Target Abort** This bit is set when a device completes a Request using Completer Abort Completion Status.	0b	
10:9	RO	**DEVSEL Timing** Does not apply to PCI Express. Must be hardwired to 0.	00b	

8	R/WC	**Master Data Parity Error** This bit is set by Requestor (Primary Side for Type 1 Configuration Space header device) if the Parity Error Response bit in the Command register is 1b and either of the following tow conditions occurs: • Requestor receives a Completion marked poisoned • Requestor poisons a write Request	0b	
7	RO	**Fast Back-to-Back Transactions Capable** Does not apply to PCI Express. Must be hardwired to 0.	0b	
6	RO	**Reserved**	0	
5	RO	**66 MHz capable** Does not apply to PCI Express. Must be hardwired to 0.	0b	
4	RO	**Capability List** Indicates the presence of an extended capability list item. Since all PCI Express devices are required to implement the PCI Express capability structure, this bit must be set to 1.	1b	
3	RO	**Interrupt Status** Indicates that an INTx Interrupt Message is pending internally to the device.	0b	
2:0	RO	**Reserved**	0	

Register 08h Revision Identification Register

Default Value : 00h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	RO	**Revision ID** This register specifies a device specific revision identifier.	00h	

Register 09-0Bh Class Code Register

Default Value : 060400h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
23:0	RO	**Class Code** The Class Code register is read-only and is used to identify the generic function of the device and, in some cases, a specific register-level programming interface.	060400h	

Register 0Ch Cache Line Size Register

Default Value : 00h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	R/W	**Cache Line Size** This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.	00h	

Register 0Dh Memory Latency Timer Register

Default Value : 00h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	RO	**Memory Latency Timer** The primary/master latency timer does not apply to PCI Express. This register must be hardwired to 0.	00h	

Register 0Eh Header Type Register

Default Value : 01h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.

7:0	RO	**Header Type** A bridge returns a value of 01h to indicate that the header adheres to the PCI-to-PCI Bridge Configuration Space layout.	01h	

Register 0Fh BIST Register

Default Value : 00h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	RO	**BIST** The BIST register is an optional register used for control and status reporting of built-in-self test capability. A bridge that does not support BIST must implement this register as a read-only register that returns 0 when read.	00h	

Register 10-17h Memory Base Address Register

Default Value : 0

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
63:0	RO	**Memory Base** This field maps internal device-specific registers to a memory address range.	0	

Register 18h Primary Bus Number

Default Value : 00h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.

7:0	RO	**Primary Bus Number** This field is used to record the Bus Number of the logical PCI bus segment to which the primary interface of the bridge is connected.	00h	

Register 19h Secondary Bus Number

Default Value : 00h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	R/W	**Secondary Bus Number** This field is used to record the Bus Number of the logical PCI bus segment to which the secondary interface of the bridge is connected.	00h	

Register 1Ah Subordinate Bus Number

Default Value : 00h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	R/W	**Subordinate Bus Number Register** This field is used to record the Bus Number of the highest numbered PCI bus segment which is downstream of the bridge.	00h	

Register 1Bh Secondary Latency Timer

Default Value : 00h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	RO	**Secondary Latency Timer** This register does not apply to PCI Express. It must be read-only and hardwired to 0.	00h	

Register 1Ch I/O Base Register

Default Value : F1h Recommend setting : F1h

Access Type : Read-Only, Read/Write, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:4	R/W	**I/O Base Address** I/O Base bits corresponding to address lines 15:12 for 4-KB alignment.	Fh	Fh
3:1	RO	**I/O Addressing Capability**	000b	
0	R/WO	**I/O Addressing Capability** The definition of this register is as follows. 1: 32-bit I/O Addressing 0: 16-bit I/O Addressing	1b	1b

Register 1Dh IO Limit Register

Default Value : 01h Recommend setting : 01h

Access Type : Read-Only, Read/Write, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:4	R/W	**I/O Limit Address** I/O Limit bits corresponding to address lines 15:12 for 4-KB alignment.	0h	0h
3:1	RO	**I/O Addressing Capability**	000b	
0	R/WO	**I/O Addressing Capability** The definition of this register is as follows. 1: 32-bit I/O Addressing 0: 16-bit I/O Addressing	1b	1b

Register 1E-1Fh Secondary Status Register

Default Value : 0000h

Access Type : Read-Only, Read/Write Clear

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.

15	R/WC	**Detected Parity Error** This bit is set by the Secondary Side for a Type 1 Configuration Space header device whenever it receives a Poisoned TLP, regardless of the state the Parity Error Response Enable bit in the Bridge Control register.	0b	
14	R/WC	**Received System Error** This bit is set when the Secondary Side for a Type 1 configuration space header device receives an ERR_FATAL or ERR_NONFATAL Message.	0b	
13	R/WC	**Received Master Abort** This bit is set when the Secondary Side for Type 1 Configuration Space header device receives a Completion with Unsupported Request Completion Status.	0b	
12	R/WC	**Received Target Abort** This bit is set when the Secondary Side for Type 1 Configuration Space header device receives a Completion with Completer Abort Completion Status.	0b	
11	R/WC	**Signaled Target Abort** This bit is set when the Secondary Side for Type 1 Configuration Space header device completes a Request using Completer Abort Completion Status.	0b	
10:9	RO	**DEVSEL Timing** Does not apply to PCI Express. Must be hardwired to 0.	00b	
8	R/WC	**Master Data Parity Error** This bit is set by the Secondary side Requestor if the Parity Error Response Enable bit in the Bridge Control register is 1b and either of the following two conditions occurs: • Requestor receives Completion marked poisoned • Requestor poisons a write Request	0b	
7	RO	**Fast Back-to-Back Transactions Capable** Does not apply to PCI Express. Must be hardwired to 0.	0b	
5	RO	**66 MHz Capable** Does not apply to PCI Express. Must be hardwired to 0.	0b	
4:0	RO	**Reserved**	0	

Register 20-21h Memory Base Register

Default Value : FFF0h Recommend setting : FFF0h

Access Type : Read-Only, Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:4	R/W	**Memory Base** These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value of the range.	FFFh	FFFh
3:0	RO	**Reserved**	0	

Register 22-23h Memory Limit Register

Default Value : 0000h Recommend setting : 0000h

Access Type : Read-Only, Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:4	R/W	**Memory Limit** These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value of the range.	000h	000h
3:0	RO	**Reserved**	0	

Register 24-25h Prefetchable Memory Base Register

Default Value : FFF1h Recommend setting : FFF1h

Access Type : Read-Only, Read/Write, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:4	R/W	**Prefetchable Memory Base** These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value of the range.	FFFh	FFFh
3:1	RO	**64-bit indicator**	000b	
0	R/WO	**64-bit indicator** This field indicates support for 64-bit addressing.	1b	1b

Register 26-27h Prefetchable Memory Limit Register

Default Value : 0001h Recommend setting : 0001h

Access Type : Read-Only, Read/Write, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:4	R/W	**Prefetchable Memory Limit** These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value of the range.	000h	000h
3:1	RO	**64-bit indicator**	000b	
0	R/WO	**64-bit indicator** This field indicates support for 64-bit addressing.	1b	1b

Register 28-2Bh Prefetchable Base Upper 32 Bits Register

Default Value : 00000000h Recommend setting : 00000000h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:0	R/W	**Prefetchable Base Upper 32 Bits** Upper 32-bits of the prefetchable address base.	0	0

Register 2C-2Fh Prefetchable Limit Upper 32 Bits Register

Default Value : 00000000h Recommend setting : 00000000h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:0	R/W	**Prefetchable Limit Upper 32 Bits** Upper 32-bits of the prefetchable address limit.	0	0

Register 30-31h I/O Base Upper 16 Bits Register

Default Value : 0000h Recommend setting : 0000h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:0	R/W	**I/O Base Upper 16 Bits** Upper 16-bits of the I/O address base.	0	0

Register 32-33h I/O Limit Upper 16 Bits Register

Default Value : 0000h Recommend setting : 0000h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:0	R/W	**I/O Limit Upper 16 Bits** Upper 16-bits of the I/O address limit.	0	0

Register 34h Capability Pointer

Default Value : B0h

Access Type : Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	R/WO	**Capabilities Pointer** Point to Subsystem Vendor capability (B0h offset).	B0h	

Register 35-3Bh Reserved

Default Value : 0

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
27:0	RO	**Reserved**	0	

Register 3Ch Interrupt Line Register

Default Value : 00h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	R/W	**Interrupt Line** This register communicates interrupt line routing information.	00h	

Register 3Dh Interrupt Pin Register

Default Value : 01h Recommend setting : 01h

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:3	RO	**Interrupt Pin** This register identifies the legacy interrupt Message the device uses.	0	
2:0	R/WO	**Interrupt Pin IntA** Valid values are 1, 2, 3, and 4 that map to legacy interrupt Messages for INTA, INTB, INTC, and INTD respectively; a value of 0 indicates that the device uses no legacy interrupt Message(s).	001b	001b

Register 3Eh Bridge Control

Default Value : 00h

Access Type : Read-Only, Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7	RO	**Fast Back-to-Back Transactions Enable** Does not apply to PCI Express. Must be hardwired to 0.	0b	
6	R/W	**Secondary Bus Reset** Setting this bit triggers a hot reset on the corresponding PCI Express port.	0b	

5	RO	**Master Abort Mode** Does not apply to PCI Express. Must be hardwired to 0.	0b	
4	R/W	**VGA 16-bit Decode** This bit enables the bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB.	0b	
3	R/W	**VGA Enable** Not implemented.	0b	
2	R/W	**ISA Enable** Not Implemented.	0b	
1	R/W	**SERR# Enable** This bit controls forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary. 0: disable 1: enable	0b	
0	R/W	**Parity Error Response Enable** This bit controls the response to Poisoned TLPs. 0: disable 1: enable	0b	

Register 3Fh Reserved

Default Value : 00h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
7:0	RO	**Reserved**	0	

Register 40h~43h Reserved

Register 44h PCI Express Design Option

Bit	Access	Description	Power-Up	Recom.

7:6	R/W	**ACK update timer initial value** 00b : 960ns 01b : 1920ns 10b : 2880ns 11b : 480ns	00b	11b

Register 45h Reserved

Register 46h PCI Express Design Option

Bit	Access	Description	Power-Up	Recom.
0	R/W	**Prsnt Check** Select the reported information source of Register EA bit 6 (PCIE Slot Status Register, "Presence Detect State") 0: Reported by PCIE_PRSNT# pin (only available when PCIE Slot Capability Register, "Hot Plug Capable" bit is set to 1 (RE4 bit 6) 1: Reported by PCIE PHY detect result	0b	1b

Register 47h Reserved

Register 49h PCI Express Design Option

Bit	Access	Description	Power-Up	Recom.
1	R/W	**TX L0s/L1 PHY power saving** **Advance PHY power saving when TX L0s and L1 state** 0: Disable 1: Enable	0b	1b
0	R/W	**RX L0s/L1 PHY power saving** **Advance PHY power saving when RX L0s and L1 state** 0: Disable 1: Enable	0b	1b

Register 4Ah~58h Reserved

Register 59h PCI Express EDC Design Option

Bit	Access	Description	Power-Up	Recom.
7	R/W	**TX logic gating PCIE clock** 0: Gating disable 1: Gating enable	0b	0b
6	R/W	**HBEDB queue logic gating ASL clock** 0: Gating disable 1: Gating enable	0b	0b
5:4	R/W	**Reserved**	00b	00b
3	R/W	**HBEDB interface logic gating ASL clock** 0: Gating disable 1: Gating enable	0b	0b
2	R/W	**PCI interface logic gating PCI clock** 0: Gating disable 1: Gating enable	0b	0b
1	R/W	**PCI interface logic gating PCIE clock** 0: Gating disable 1: Gating enable	0b	0b
0	R/W	**Reserved**	0b	0b

Register 5Ah PCI Express EDC Design Option

Bit	Access	Description	Power-Up	Recom.
4	R/W	**PLL turn off when L1 state function** **0: PLL off function disable** **1: PLL off function enable**	0b	0b
3:2	R/W	**Reserved**	00b	00b
1	R/W	**RX logic gating PCIE clock in L0s state** **0: Gating disable** **1: Gating enable** **NOTE: If South Bridge's PCIE_PRSNT pin is tied to GND, but there is a possible application that user doesn't attach PCIE devices to the port, this bit should not be set to 1.** **(Example cases:** **Form factor is X1 Slot or PCIE Mini Card, and PCIE_PRSNT is tied to GND)**	0b	0b

0	**R/W**	**RX logic gating PCIE clock in L1 state** **0: Gating disable** **1: Gating enable**	**0b**	**0b**

Register 5Ch PCI Express Design Option

Bit	Access	Description	Power-Up	Recom.
3:2	R/W	**Logic workaround for Intel pro/1000 GLAN PCIE device** To workaround the device's logic issue of L1 state 2'b00: default 2'b11: Workaround enable <NOTE: PCIE link must be HOT RESET after these 2 bit are set, to let the workaround takes effect>	0b	11b

Register 5Dh~5Fh Reserved

Register B0-B3h Subsystem Vendor Capability Register

Default Value : 0000C00Dh

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:24	RO	**Reserved**	0	
23:16	RO	**Reserved**	0	
15:8	R/WO	**Next Capability Pointer** Point to the MSI Capability (C0h offset)	C0h	
7:0	RO	**SSID/SSVID Capability ID** Value of 0Dh indicates this is a PCI bridge subsystem vendor capability	0Dh	

Register B4-B7h Subsystem Vendor Identification Register

Default Value : 00000000h

Access Type : Read/Write-Once

Power Plane : Main

Note:SSVID and SSID for DTM test

Bit	Access	Description	Power-Up	Recom.
31:16	R/WO	**SSID** The SSID identifies the particular add-in card or subsystem and is assigned by the vendor.	0000h	0004h
15:0	RO	**SSVID** The SSVID identifies the manufacturer of the add-in card or subsystem.	0000h	1039h

Register EAh

Bit	Access	Description	Power-Up	Recom.
6	R/W	If register 46h bit 0 is 0 ,then define encoding are : 0b:slot empty 1b:Card present in slot Else the coding are: 0b: Not in detect state 1b: Card is in detect state		

Register C0-C3h MSI Capability Register

Default Value : 0000D005h

Access Type : Read-Only, Read/Write, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:24	RO	**Reserved**	0	
23	R/WO	**64bit address capable** If 1, the function is capable of generating a 64-bit message address. If 0, the function is not capable of generating a 4-bit message address.	0b	

22:20	R/W	**Multiple Message Enable** System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two. If a function requests four messages (indicated by a Multiple Message Capable encodings of “010”), system software can allocate either four, two, or one message by writing a “010”, “001, or “000” to this field, respectively. When MSI is enabled, a device will be allocated at least 1 message. The encodings are defined as: Encodings # of messages allocated 000 1 001 2 010 4 011 8 100 16 101 32 110 Reserved 111 Reserved	000b	000b
19:17	RO	**Multiple Message Capable** System software reads this field to determine the number of requested messages. The number of requested messages must be aligned to a power of two (if a function requires three messages, it requests four by initializing this field to “010”). The encodings are defined as: Encodings # of messages requested 000 1 001 2 010 4 011 8 100 16 101 32 110 Reserved 111 Reserved	000b	

16	R/W	**MSI Enable** If 1, the function is permitted to use MSI to request service and is prohibited from using its INTx# pin (if implemented). System configuration software sets this bit to enable MSI. A device driver is prohibited from writing this bit to mask a function's service request. If 0, the function is prohibited from using MSI to request service.	0b	0b
15:8	R/WO	**NXT_PTR** Pointer to the next item in the capabilities list. Must be NULL for the final item in the list.	D0h	
7:0	RO	**CAP_ID** The value of 05h in this field identifies the function as message signaled interrupt capable.	05h	

Register C4-C7h Message Address Register

Default Value : 00000000h

Access Type : Read/Write, Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
32:2	R/W	**Message Address** System-specified message address. If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register specify the DWORD aligned address (**AD[31::02])** for the MSI memory write transaction. **AD[1::0]** are driven to zero during the address phase.	0	
1:0	RO	**Reserved**	0	

Register C8-CBh Message Upper Address Register

Default Value : 00000000h

Access Type : Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.

31:0	R/W	**Message Upper Address** System-specified message upper address. This register is optional and is implemented only if the device supports a 64-bit message address (bit 7 in Message Control register set). If the Message Enable bit (bit 0 of the Message Control register) is set, the contents of this register (if non-zero) specify the upper 32-bits of a 64-bit message address (**AD [63:32]**). If the contents of this register are zero, the device uses the 32 bit address specified by the message address register.	0	

Register CC-CFh Message Data Register

Default Value : 00000000h

Access Type : Read/Write, Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:16	RO	**Reserved**	0	

15:0	R/W	**Message Data** System-specified message. Each MSI function is allocated up to 32 unique messages. System architecture specifies the number of unique messages supported by the system. If the Message Enable bit (bit 0 of the Message Control register) is set, the message data is driven onto the lower word (**AD[15::00]**) of the memory write transaction's data phase. **AD[31::16]** are driven to zero during the memory write transaction's data phase. **C/BE[3::0]#** are asserted during the data phase of the memory write transaction. The Multiple Message Enable field (bits 6-4 of the Message Control register) defines the number of low order message data bits the function is permitted to modify to generate its system software allocated messages. For example, a Multiple Message Enable encodings of "010" indicates the function has been allocated four messages and is permitted to modify message data bits 1 and 0 (a function modifies the lower message data bits to generate the allocated number of messages). If the Multiple Message Enable field is "000", the function is not permitted to modify the message data.	0000h	

Register D0-D3h PCI Express Capability Register

Default Value : 0141F410h

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:30	RO	**Reserved**	0	
29:25	RO	**Interrupt Message Number** This register must indicate which MSI/MSI-X vector is used for the interrupt message generated in association with the status bits in either the Slot Status register or the Root Status register of this capability structure.	00h	

24	R/WO	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled). This field is valid for the following PCI Express device/Port Types: • Root Port of PCI Express Root Complex • Downstream Port of PCI Express Switch.	1b	
23:20	RO	**Device/Port Type** Indicates the type of PCI Express logical device. Defined encodings are: 0000b PCI Express Endpoint device 0001b Legacy PCI Express Endpoint device 0100b Root Port of PCI Express Root Complex* 0101b Upstream Port of PCI Express Switch* 0110b Downstream Port of PCI Express Switch* 0111b PCI Express-to-PCI/PCI-X Bridge* 1000b PCI/PCI-X to PCI Express Bridge* 1001b Root Complex Integrated Endpoint Device 1010b Root Complex Event Collector All other encodings are reserved.	0100b	
19:16	RO	**Capability Version** Indicates PCI-SIG defined PCI Express capability structure version number. Must be 1h for devices complaint to this specification.	0001b	
15:8	R/WO	**Next Capability Pointer** The offsets to the next PCI capability structure or 00h if no other items exist in the linked list of capabilities. Point to Power Management Capability (F4 offset)	F4h	
7:0	RO	**Capability ID** This field must return a Capability ID of 10h indicating that this is a PCI Express Capability structure.	10h	

Register D4-D7h Device Capabilities Register

Default Value : 00000020h

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:28	RO	**Reserved**	0	
27:26	RO	**Captured Slot Power Limit Scale (Upstream Ports only)** Specifies the scale used for the Slot Power Limit Value. Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x The Set_Slot_Power_Limit Message or hardwired to 00b sets this value.	00b	
25:18	RO	**Captured Slot Power Limit Value (Upstream Ports only)** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. This value is set by the Set_Slot_Power_Limit Message or hardwired to 0000 0000b.	00h	
17:16	RO	**Reserved**	0	
15	RO	**Role-Based Error Reporting (1.1)** This bit, when set, indicates that the device implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1.	0b	
14	RO	**Power Indicator Present (1.0)** This bit, when set, indicates that a Power Indicator is implemented on the card or module. This bit is valid for the following PCI Express device Types: • PCI Express Endpoint device • Legacy PCI Express Endpoint device • Upstream Port of PCI Express Switch • PCI Express-to-PCI/PCI-X Bridge	0b	

13	RO	**Attention Indicator Present (1.0)** This bit, when set, indicates that an Attention Indicator is implemented on the card or module. This bit is valid for the following PCI Express device Types: • PCI Express Endpoint device • Legacy PCI Express Endpoint device • Upstream Port of PCI Express Switch • PCI Express-to-PCI/PCI-X Bridge	0b	
12	RO	**Attention Button Present (1.0)** This bit when set indicates that an Attention Button is implemented on the card or module. This bit is valid for the following PCI Express device Types: • PCI Express Endpoint device • Legacy PCI Express Endpoint device • Upstream Port of PCI Express Switch • PCI Express-to-PCI/PCI-X Bridge.	0b	
11:9	R/WO	**Endpoint L1 Acceptable Latency** This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L1 Acceptable Latency number to compare against the L1 Exit Latencies reported (see below) by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L1 entry can be used with no loss of performance. Defined encodings are: 000b Less than 1µs 001b 1 µs to less than 2 µs 010b 2 µs to less than 4 µs 011b 4 µs to less than 8 µs 100b 8 µs to less than 16 µs 101b 16 µs to less than 32 µs 110b 32 µs-64 µs 111b More than 64 µs.	000b	

8:6	R/WO	**Endpoint L0s Acceptable Latency** This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L0s entry can be used with no loss of performance. Defined encodings are: 000b Less than 64 ns 001b 64 ns to less than 128 ns 010b 128 ns to less than 256 ns 011b 256 ns to less than 512 ns 100b 512 ns to less than 1 µs 101b 1 µs to less than 2 µs 110b 2 µs-4 µs 111b More than 4 µs.	000b	
5	R/WO	**Extended Tag Field Supported** This field indicates the maximum supported size of the Tag field as a Requester. Defined encodings are: 0b 5-bit Tag field supported 1b 8-bit Tag field supported Note that 8-bit Tag field support must be enabled by the corresponding control field in the Device Control register.	1b	

4:3	RO	**Phantom Functions Supported** This field indicates the support for use of unclaimed function numbers to extend the number of outstanding transactions allowed by logically combining unclaimed function numbers with the Tag identifier. Defined encodings are: 00b No function number bits used for Phantom Functions; device may implement all function numbers. 01b First most significant bit of function number in Requestor ID used for Phantom Functions; device may implement functions 0-3. Functions 0, 1, 2, and 3 may claim functions 4, 5, 6, and 7 as Phantom Functions respectively. 10b First two most significant bits of function number in Requestor ID used for Phantom Functions; device may implement functions 0-1. Function 0 may claim functions 2, 4, and 6 as Phantom Functions, function 1 may claim functions 3, 5, and 7 as Phantom Functions. 11b All three bits of function number in Requestor ID used for Phantom Functions; device must be a single function 0 device that may claim all other functions as Phantom Functions. Note that Phantom Function support for the Device must be enabled by the corresponding control field in the Device Control register.	00b	
2:0	R/WO	**Max_Payload_Size Supported** This field indicates the maximum payload size that the device can support for TLPs. Defined encodings are: 000b 128 bytes max payload size 001b 256 bytes max payload size 010b 512 bytes max payload size 011b 1024 bytes max payload size 100b 2048 bytes max payload size 101b 4096 bytes max payload size 110b Reserved 111b Reserved.	000b	

Register D8-D9h Device Control Register

Default Value : 0810h **Recommend setting : 0810h**

Access Type : Read-Only, Read/Write, Read/Write Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recom.
15	RO	**Reserved**	0	
14:12	R/W	**Max_Read_Request_Size** This field sets the maximum Read Request size for the Device as a Requester. The Device must not generate read requests with size exceeding the set value. Defined encodings for this field are: 000b 128 bytes max read request size 001b 256 bytes max read request size 010b 512 bytes max read request size 011b 1024 bytes max read request size 100b 2048 bytes max read request size 101b 4096 bytes max read request size 110b Reserved 111b Reserved.	000b	000b
11	R/W	**Enable No Snoop** If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency.	1b	1b
10	R/WS	**Auxiliary (AUX) Power PM Enable** This bit when set enables a device to draw AUX power independent of PME AUX power.	0b	0b
9	R/W	**Phantom Functions Enable** When set, this bit enables a device to use unclaimed functions as Phantom Functions to extend the number of outstanding transaction identifiers. If the bit is cleared, the device is not allowed to use Phantom Functions.	0b	0b
8	R/W	**Extended Tag Field Enable** When set, this bit enables a device to use an 8-bit Tag field as a requester. If the bit is cleared, the device is restricted to a 5-bit Tag field.	0b	0b

7:5	RO	**Max_Payload_Size** This field sets maximum TLP payload size for the device. As a Receiver, the device must handle TLPs as large as the set value; as Transmitter, the device must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size Supported in the Device Capabilities register. Defined encodings for this field are: 000b 128 bytes max payload size 001b 256 bytes max payload size 010b 512 bytes max payload size 011b 1024 bytes max payload size 100b 2048 bytes max payload size 101b 4096 bytes max payload size 110b Reserved 111b Reserved	000b	000b
4	R/W	**Enable Relaxed Ordering** If this bit is set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering.	1b	1b
3	R/W	**Unsupported Request Reporting Enable** This bit enables reporting of Unsupported Requests when set.	0b	0b
2	R/W	**Fatal Error Reporting Enable** This bit controls reporting of Fatal errors. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_FATAL Message is generated.	0b	0b
1	R/W	**Non-Fatal Error Reporting Enable** This bit controls reporting of Non-fatal errors. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_NONFATAL Message is generated.	0b	0b
0	R/W	**Correctable Error Reporting Enable** This bit controls reporting of correctable errors. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR Message is generated.	0b	0b

Register DA-DBh Device Status Register Register

Default Value : 0010h

Access Type : Read-Only, Read/Write-Clear

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:6	RO	**Reserved**	0	
5	RO	**Transactions Pending** This bit when set indicates that the device has issued Non-Posted Requests, which have not been completed. The Port reports this bit cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism.	0b	
4	RO	**AUX Power Detected** Devices that require AUX power report this bit as set if AUX Power is detected by the device.	1b	
3	R/WC	**Unsupported Request Detected** This bit indicates that the device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.	0b	
2	R/WC	**Fatal Error Detected** This bit indicates status of Fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.	0b	
1	R/WC	**Non-Fatal Error Detected** This bit indicates status of Nonfatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register..	0b	
0	R/WC	**Correctable Error Detected** This bit indicates status of correctable errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.	0b	

Register DC-DFh Link Capabilities Register

Default Value : 0000CC11

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:24	R/WO	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.	00h	
23:21	RO	**Reserved**	0	
20	RO	**Data Link Layer Link Active Reporting Capable (1.1)** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable field of the Slot Capabilities register), this bit must be set to 1b.	0b	
19:18	RO	**Reserved**	0	
17:15	R/WO	**L1 Exit Latency** This field indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L1 to L0. Defined encodings are: 000b Less than 1µs 001b 1 µs to less than 2 µs 010b 2 µs to less than 4 µs 011b 4 µs to less than 8 µs 100b 8 µs to less than 16 µs 101b 16 µs to less than 32 µs 110b 32 µs-64 µs 111b More than 64 µs.	001b	

14:12	R/WO	**L0s Exit Latency** This field indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this Port requires to complete transition from L0s to L0. Defined encodings are: 000b Less than 64 ns 001b 64 ns to less than 128 ns 010b 128 ns to less than 256 ns 011b 256 ns to less than 512 ns 100b 512 ns to less than 1 µs 101b 1 µs to less than 2 µs 110b 2 µs-4 µs 111b More than 4 µs	100b	
11:10	R/WO	**Active State Power Management Support** This field indicates the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Reserved 01b L0s Entry Supported 10b Reserved 11b L0s and L1 Supported.	11b	
9:4	RO	**Maximum Link Width** This field indicates the maximum width of the given PCI Express Link. Defined encodings are: 000000b Reserved 000001b x1 000010b x2 000100b x4 001000b x8 001100b x12 010000b x16 100000b x32.	01h	
3:0	RO	**Maximum Link Speed** This field indicates the maximum Link speed of the given PCI Express Link. Defined encodings are: 0001b 2.5 Gb/s Link All other encodings are reserved.	0001b	

Register E0-E1h Link Control Register

Default Value : 0000h **Recommend setting : 0000h**

Access Type : Read-Only, Read/Write, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:8	RO	**Reserved**	0	
7	R/W	**Extended Synch** This bit when set forces the transmission of 4096 FTS ordered sets in the L0s state followed by a single SKP ordered set prior to entering the L0 state, and the transmission of 1024 TS1 ordered sets in the L1 state prior to entering the Recovery state.	0b	0b
6	R/W	**Common Clock Configuration** This bit when set indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock.	0b	0b
5	R/W	**Retrain Link** A write of 1b to this bit initiates Link retraining by directing the Physical Layer LTSSM to the Recovery state. Reads of this bit always return 0b. This field is not applicable and is reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches.	0b	
4	R/W	**Link Disable** This bit disables the Link when set to 1b; this field is not applicable and reserved for Endpoint devices, PCI Express to PCI/PCI-X bridges, and Upstream Ports of Switches. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.	0b	
3	R/WO	Read Completion Boundary (RCB) Indicates the RCB value for the Root Port. Defined encodings are: 0b 64 byte 1b 128 byte	0b	
2	RO	**Reserved**	0	

1:0	R/W	**Active State Power Management (ASPM) Control** This field controls the level of ASPM supported on the given PCI Express Link. Defined encodings are: 00b Disabled 01b L0s Entry Enabled 10b L1 Entry Enabled 11b L0s and L1 Entry Enabled	00b	

Register E2-E3h Link Status Register

Default Value : 1011h

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:14	RO	**Reserved**	0	
13	RO	**Data Link Layer Link Active (1.1)** This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise.	0b	
12	R/WC	**Slot Clock Configuration** This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be clear.	1b	
11	RO	**Link Training** This read-only bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state.	0b	
10	RO	**Training Error (1.0)** This read-only bit indicates that a Link training error occurred. This bit is cleared by hardware upon successful training of the Link to the L0 Link state.	0b	

9:4	RO	**Negotiated Link Width** This field indicates the negotiated width of the given PCI Express Link. Defined encodings are: 000001b X1 000010b X2 000100b X4 001000b X8 001100b X12 010000b X16 100000b X32	01h	
3:0	RO	**Link Speed** This field indicates the negotiated Link speed of the given PCI Express Link. Defined encodings are: 0001b 2.5 Gb/s PCI Express Link All other encodings are reserved.	0001b	

Register E4-E7h Slot Capabilities Register

Default Value : 00000000h

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:19	R/WO	**Physical Slot Number** This hardware initialized field indicates the physical slot number attached to this Port. This field must be hardware initialized to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to 0 for Ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Switch device or Root Port.	0	
18	RO	**No Command Completed Support (1.1)** When set to 1b, this bit indicates that this slot does not generate software notification when an issued command is completed by the Hot-Plug Controller.	0b	
17	RO	**Reserved**	0	

16:15	R/WO	**Slot Power Limit Scale** Specifies the scale used for the Slot Power Limit Value. Range of Values: 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 00b.	00b	
14:7	R/WO	**Slot Power Limit Value** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. Writes to this register also cause the Port to send the Set_Slot_Power_Limit Message. The default value prior to hardware/firmware initialization is 0000 0000b.	00h	
6	R/WO	**Hot-Plug Capable** When set to 1b, this bit indicates that this slot is capable of supporting hot-plug opertations.	0b	
5	R/WO	**Hot-Plug Surprise** When set to 1b, this bit indicates that an adapter present in this slot might be removed from the system without any prior notification. This bit is an indication to the operating system to allow for such removal without impacting continued software operation.	0b	
4	R/WO	**Power Indicator Present** This bit when set indicates that a Power Indicator is implemented on the chassis for this slot.	0b	
3	R/WO	**Attention Indicator Present** This bit when set indicates that an Attention Indicator is implemented on the chassis for this slot.	0b	
2	R/WO	**MRL Sensor Present** This bit when set indicates that an MRL Sensor is implemented on the chassis for this slot.	0b	
1	R/WO	**Power Controller Present** This bit when set indicates that a Power Controller is implemented for this slot.	0b	
0	R/WO	**Attention Button Present** This bit when set indicates that an Attention Button is implemented on the chassis for this slot.	0b	

Register E8-E9h Slot control Register

Default Value : 03C0h Recommend setting : 03C0h

Access Type : Read-Only, Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:13	RO	**Reserved**	0	
12	RO	**Data Link Layer State Changed Enable (1.1)** If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Kink Active field is changed.	0b	
11	RO	**Reserved**	0	
10	R/W	**Power Controller Control** If a Power Controller is implemented, this field when written set the power state of the slot per the defined encodings. The defined encodings are: 0b Power On 1b Power Off	0b	0b
9:8	R/W	**Power indicator Control** If a Power Indicator is implemented writes to this field set the Power Indicator to the written state. Defined encodings are: 00b Reserved 01b On 10b Blink 11b Off	11b	11b
7:6	R/W	**Attention Indicator Control** If an Attention Indicator is implemented writes to this field set the Attention Indicator to the written state. Defined encodings are: 00b Reserved 01b On 10b Blink 11b Off	11b	11b
5	R/W	**Hot-Plug Interrupt Enable** When set to 1b, this bit enables generation of an interrupt on enabled hot-plug events.	0b	0b
4	R/W	**Command Completed Interrupt Enable** If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), when set to 1b, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller.	0b	0b

3	R/W	**Presence Detect Changed Enable** When set to 1b, this bit enables software notification on a presence detect changed event.	0b	0b
2	R/W	**MRL Sensor Changed Enable** When set to 1b, this bit enables software notification on a MRL sensor changed event.	0b	0b
1	R/W	**Power Fault Detected Enable** When set to 1b, this bit enables software notification on a power fault event.	0b	0b
0	R/W	**Attention Button Pressed Enable** When set to 1b, this bit enables software notification on an attention button pressed event.	0b	0b

Register EA-EBh Slot Status Register

Default Value : 0040h

Access Type : Read-Only, Read/Write-Clear

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:9	RO	**Reserved**	0	
8	RO	**Data Link Layer State Changed (1.1)** This bit is set when the value reported in the Data Link Layer Link Active field of the Link Status register is changed.	0b	
7	RO	**Reserved**	0	
6	RO	**Presence Detect State** This bit indicates the presence of an adapter in the slot, reflected by the logical “OR” of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot’s corresponding form factor. Defined encodings are: 0b Slot Empty 1b Card Present in slot	1b	
5	RO	**MRL Sensor State** This register reports the status of the MRL sensor if implemented. Defined encodings are: 0b MRL Closed 1b MRL Open	0b	

4	R/WC	**Command Completed** If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command.	0b	
3	R/WC	**Presence Detect Changed** This bit is set when the value reported in Presence Detect State is changed.	0b	
2	R/WC	**MRL Sensor Changed** If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected.	0b	
1	R/WC	**Power Fault Detected** If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot.	0b	
0	R/WC	**Attention Button Pressed** If an Attention Button is implemented, this bit is set when the attention button is pressed..	0b	

Register EC-EFh Root Control Register

Default Value : 00000000h Recommend setting : 00000000h

Access Type : Read-Only, Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:4	RO	**Reserved**	0	
3	R/W	**PME Interrupt Enable** This bit when set enables interrupt generation upon receipt of a PME Message as reflected in the PME Status register bit. A PME interrupt is also generated if the PME Status register bit is set when this bit is set from a cleared state.	0b	0b
2	R/W	**System Error on Fatal Error Enable** If set this bit indicates that a System Error should be generated if a Fatal error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.	0b	0b

1	R/W	**System Error on Non-Fatal Error Enable** If set this bit indicates that a System Error should be generated if a Non-fatal error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.	0b	0b
0	R/W	**System Error on Correctable Error Enable** If set this bit indicates that a System Error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.	0b	0b

Register F0-F3h Root Status Register

Default Value : 00000000h

Access Type : Read-Only, Read/Write-Clear

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:18	RO	**Reserved**	0	
17	RO	**PME Pending** This read-only bit indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.	0b	
16	R/WC	**PME status** This bit indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by software by writing a 1.	0b	
15:0	RO	**PME Requestor ID** This field indicates the PCI requestor ID of the last PME requestor.	0	

Register F4-F7h Power Management Capability Register

Default Value : C8020001h

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:27	R/WO	**PME Support** For a device, this 5-bit field indicates the power states in which the device may generate a PME. Bits 31, 30, and 27 must be set to 1b for PCI-PCI Bridge structures representing Ports on Root Complexes/Switches to indicate that the Bridge will forward PME Messages.	11001b	
26	R/WO	**D2 Support** If this bit is a “1”, this function supports the D1 Power Management State.	0b	
25	R/WO	**D1 Support** If this bit is a “1”, this function supports the D1 Power Management State.	0b	
24:22	R/WO	**AUX Current** This 3 bit field reports the 3.3Vaux auxiliary current requirements for the PCI Express function.	000b	
21	RO	**DSI** The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it.	0b	
20	RO	**Reserved**	0	
19	RO	**PME Clock** Does not apply to PCI Express. Must be hardwired to 0.	0b	
18:16	RO	**Version** Set to 02h for this version of the specification.	010b	
15:8	RO	**Next Capability Pointer** This field provides an offset into the function’s PCI Express Configuration Space pointing to the location of next item in the function’s capability list. If there are no additional items in the Capability List, this register is set to 00h.	00h	
7:0	RO	**Capability ID** Must be set to 01h.	01h	

Register F8-FBh Power Management Status/Control Register

Default Value : 00000000h

Access Type : Read-Only, Read/Write, Read/Write Sticky, Read/Write-Clear

Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recom.
31:24	RO	**Data** This register is used to report the state dependent data requested by the Data Select field.	00h	
23	RO	**Bus Power/Clock Control Enable** Does not apply to PCI Express. Must be hardwired to 0.	0b	
22	RO	**B2/B3 Support** Does not apply to PCI Express. Must be hardwired to 0.	0b	
21:16	RO	**Reserved**	0	
15	R/WCS	**PME Status** This bit is set when the function would normally assert the PME# signal independent of the state of the PME Enable bit.	0b	
14:13	RO	**Data Scale** This 2-bit read-only field indicates the scaling factor to be used when interpreting the value of the Data register.	00b	
12:9	RO	**Data Select** This 4-bit field is used to select which data is to be reported through the Data register and Data_Scale field.	0000b	
8	R/WS	**PME Enable** A “1” enables the function to assert PME#. When “0”, PME# assertion is disable.	0b	
7:2	RO	**Reserved**	0	
1:0	R/W	**Power State** This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below. 00b – D0 01b – D1 10b – D2 11b – $D3_{hot}$	00b	

Register 100-103h Virtual Channel Enhanced Capability Header

Default Value : 13010002h

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:29	RO	**Next Capability Version [11:9]**	000b	
28	R/WO	**Next Capability Offset [8]**	1b	
27:26	RO	**Next Capability Offset [7:6]**	00b	
25:24	R/WO	**Next Capability Offset [5:4]**	11b	
23:20	RO	**Next Capability Offset [3:0]**	0000b	
19:17	RO	**Capability Version [3:1]**	000b	
16	R/WO	**Capability Version [0]**	1b	
15:2	RO	**PCI Express Extended Capability ID [15:2]**	0	
1	R/WO	**PCI Express Extended Capability ID [1]**	1b	
0	RO	**PCI Express Extended Capability ID [0]**	0b	

Register 104-107h Port VC Capability Register 1

Default Value : 00000000h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:12	RO	**Reserved**	0	
11:10	RO	**Port Arbitration Table Entry Size**	00b	
9:8	RO	**Reference Clock**	00b	
7	RO	**Reserved**	0	
6:4	RO	**Low Priority Extended VC Count**	000b	
3	RO	**Reserved**	0	
2:0	RO	**Extended VC Count**	000b	

Register 108-10Bh Port VC Capability Register 2

Default Value : 00000000h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:24	RO	**VC Arbitration Table Offset**	00h	
23:8	RO	**Reserved**	0	
7:0	RO	**VC Arbitration Capability**	00h	

Register 10C-10Dh Port VC Control Register

Default Value : 0000h Recommend setting : 0000h

Access Type : Read-Only , Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:4	RO	**Reserved**	0	
3:1	R/W	**VC Arbitration Select**	000b	000b
0	R/W	**Load VC Arbitration Table**	0b	0b

Register 10E-10Fh Port VC Status Register

Default Value : 0000h

Access Type : Read-Only

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
15:1	RO	**Reserved**	0	
0	RO	**VC Arbitration Table Status**	0b	

Register 110-113h VC0 Resource Capability Register

Default Value : 00000000h

Access Type : Read-Only, Read/Write-Once

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:24	RO	**Port Arbitration Table Offset**	00h	
23	RO	**Reserved**	0	
22:16	RO	**Maximum Time Slots**	00h	
15	R/WO	**Reject Snoop Transactions**	0b	
14	RO	**Advanced Packet Switching (1.0)**	0b	
13:8	RO	**Reserved**	0	
7:0	RO	**Port Arbitration Capability**	00h	

Register 114-117h VC0 Resource Control

Default Value : 800000FFh Recommend setting : 800000FFh

Access Type : Read-Only, Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31	RO	**VC Enable**	1b	
30:27	RO	**Reserved**	0	
26:24	RO	**VC ID**	000b	
23:20	RO	**Reserved**	0	
19:17	RO	**Port Arbitration Select**	000b	
16	RO	**Load Port Arbitration Table**	0b	
15:8	RO	**Reserved**	0	
7:1	R/W	**TC/VC Map [7:1]**	111,1111b	111,1111b
0	RO	**TC/VC Map [0]**	1b	

Register 130-133h Advanced Error Reporting Enhanced Capability Header

Default Value : 00010001h

Access Type : Read-Only , Read/Write One

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:20	RO	**Next Capability Offset**	0	
19:16	RO	**Capability Version**	0001b	

15:1	RO	**PCI Express Extended Capability ID [15:1]**	0	
0	R/WO	**PCI Express Extended Capability ID [0]**	1b	

Register 134-137h Uncorrectable Error Status Register

Default Value : 00000000h

Access Type : Read-Only , Read/Write-Clear Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recom.
31:21	RO	**Reserved**	0	
20	R/WCS	**Unsupported Request Error Status**	0b	
19	RO	**Reserved**	0	
18	R/WCS	**Malformed TLP Status**	0b	
17	R/WCS	**Receiver Overflow Status**	0b	
16	R/WCS	**Unexpected Completion Status**	0b	
15	RO	**Reserved**	0	
14	R/WCS	**Completion Timeout Status**	0b	
13	RO	**Reserved**	0	
12	R/WCS	**Poisoned TLP Status**	0b	
11:5	RO	**Reserved**	0	
4	R/WCS	**Data Link Protocol Error Status**	0b	
3:1	RO	**Reserved**	0	
0	R/WCS	**Training Error Status (1.0)**	0b	

Register 138-13Bh Uncorrectable Error Mask Register

Default Value : 00000000h Recommend setting : 00000000h

Access Type : Read-Only , Read/Write Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recom.
31:21	RO	**Reserved**	0	
20	R/WS	**Unsupported Request Error Mask**	0b	0b
19	RO	**Reserved**	0	
18	R/WS	**Malformed TLP Mask**	0b	0b
17	R/WS	**Receiver Overflow Mask**	0b	0b

16	R/WS	**Unexpected Completion Mask**	0b	0b
15	RO	**Reserved**	0	
14	R/WS	**Completion Timeout Mask**	0b	0b
13	RO	**Reserved**	0	
12	R/WS	**Poisoned TLP Mask**	0b	0b
11:5	RO	**Reserved**	0	
4	R/WS	**Data Link Protocol Error Mask**	0b	0b
3:1	RO	**Reserved**	0	
0	R/WS	**Training Error Mask (1.0)**	0b	0b

Register 13C-13Fh Uncorrectable Error Severity Register

Default Value : 00062011h Recommend setting : 00062011h

Access Type : Read-Only , Read/Write Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recom.
31:21	RO	**Reserved**	0	
20	R/WS	**Unsupported Request Error Severity**	0b	0b
19	RO	**Reserved**	0	
18	R/WS	**Malformed TLP Severity**	1b	1b
17	R/WS	**Receiver Overflow Error Severity**	1b	1b
16	R/WS	**Unexpected Completion Error Severity**	0b	0b
15	RO	**Reserved**	0	
14	R/WS	**Completion Timeout Error Severity**	0b	0b
13	RO	**Reserved**	1	
12	R/WS	**Poisoned TLP Severity**	0b	0b
11:5	RO	**Reserved**	0	
4	R/WS	**Data Link Protocol Error Severity**	1b	1b
3:1	RO	**Reserved**	0	
0	R/WS	**Training Error Severity (1.0)**	1b	1b

Register 140-143h Correctable Error Status Register

Default Value : 00000000h

Access Type : Read-Only, Read/Write-Clear Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recom.
31:13	RO	**Reserved**	0	
12	R/WCS	**Replay Timer Timeout Status**	0b	
11:9	RO	**Reserved**	0	
8	R/WCS	**REPLAY_NUM Rollover Status**	0b	
7	R/WCS	**Bad DLLP Status**	0b	
6	R/WCS	**Bad TLP Status**	0b	
5:1	RO	**Reserved**	0	
0	R/WCS	**Receiver Error Status**	0b	

Register 144-147h Correctable Error Mask Register

Default Value : 00000000h Recommend setting : 00000000h

Access Type : Read-Only , Read/Write Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recom.
31:13	RO	**Reserved**	0	
12	R/WS	**Replay Timer Timeout Mask**	0b	0b
11:9	RO	**Reserved**	0	
8	R/WS	**REPLAY_NUM Rollover Mask**	0b	0b
7	R/WS	**Bad DLLP Mask**	0b	0b
6	R/WS	**Bad TLP Mask**	0b	0b
5:1	RO	**Reserved**	0	
0	R/WS	**Receiver Error Mask**	0b	0b

Register 148-14Bh Advanced Error Capabilities and Control Register

Default Value : 00000000h Recommend setting : 00000000h

Access Type : Read-Only , Read-Only Sticky, Read/Write Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recom.
31:9	RO	**Reserved**	0	
8	R/WS	**ECRC Check Enable**	0b	0b
7	RO	**ECRC Check Capable**	0b	

6	R/WS	**ECRC Generation Enable**	0b	0b
5	RO	**ECRC Generation Capable**	0b	
4:0	ROS	**First Error Pointer**	0	

Register 15C-15Fh Root Error Command Register

Default Value : 00000000h Recommend setting : 00000000h

Access Type : Read-Only , Read/Write

Power Plane : Main

Bit	Access	Description	Power-Up	Recom.
31:3	RO	**Reserved**	0	
2	R/W	**Fatal Error Reporting Enable**	0b	0b
1	R/W	**Non-Fatal Error Reporting Enable**	0b	0b
0	R/W	**Correctable Error Reporting Enable**	0b	0b

Register 160-163h Root Error Status Register

Default Value : 00000000h

Access Type : Read-Only , Read/Write-Clear Sticky

Power Plane : Main, Aux

Bit	Access	Description	Power-Up	Recm.
31:27	RO	**Advanced Error Interrupt Message Number**	0	
26:7	RO	**Reserved**	0	
6	R/WCS	**Fatal Error Message Received**	0b	
5	R/WCS	**Non- Fatal Error Message Received**	0b	
4	R/WCS	**First Uncorrectable Fatal**	0b	
3	R/WCS	**Multiple ERR_FATAL/NONFATAL Received**	0b	
2	R/WCS	**ERR_FATAL/NONFATAL Received**	0b	
1	R/WCS	**Multiple ERR_COR Received**	0b	
0	R/WCS	**ERR_COR Received**	0b	

Register 164-167h Error Source Identification Register

Default Value : 00000000h

Access Type : Read-Only Sticky

Power Plane : Aux

Bit	Access	Description	Power-Up	Recom.
31:16	ROS	**ERR_FATAL/NONFATAL Source Identification**	0	
15:0	ROS	**ERR_COR Source Identification**	0	

8. High Definition Audio Digital Controller (DeviceF:Function0) Overview

Introduction

High Definition Audio Digital Controller supports the High Definition Audio interface. It supports 4 output streams and 4 input streams. It can support up to 192kHz sample rate and 32 bits sample size with 16 channels music for High Definition Audio data out.

Features:

- 32-bit PCI bus master and PCI v 2.3 compliant
- High performance bus master DMA for data transfer, and individual DMA engines for High Definition Audio PCM, modem and SPDIF.
- It supports 3 independent SDI pins for multiple CODECs. It supports High Definition Audio PCM interface with 8kHz / 11.025kHz / 16kHz / 22.05kHz / 32kHz / 44.1kHz / 48kHz / 88.2kHz / 96kHz / 176.4kHz / 192kHz sample rates, and 16-bits / 20-bits / 24-bits / 32-bits sample size with 1/2/3…/16 channels.
- It supports voice band modem CODEC v.90/v.92.

8.1. High Definition Audio PCI Configuration Register

8.1.1. High Definition Audio PCI Configuration Register Space

(D15:F0 in P968)

Offset	Register Function	Type	Reset Value
00-01h	Vendor ID	RO	1039h
02-03h	Device ID	RO	7502h
04-05h	Command	R/W	0
06-07h	Status	R/WC	0010h
08h	Revision ID	RO	0
09-0Bh	Class Code	RO	040300h
0Ch	Reserved	RO	0
0Dh	Latency Timer	RO	0
0Eh	Header Type	RO	0
10-13h	High Definition Audio OP Register Base Address	R/W,RO	0
2C-2Dh	Subsystem Vendor ID	R/WO	1039h
2E-2Fh	Subsystem ID	R/WO	1234h
30-33h	Reserved	RO	0
34h	Capabilities Pointer	RO	50h
3Ch	Interrupt Line	R/W	0
3Dh	Interrupt Pin	RO	01h
3Eh	Min. Grant	RO	34h
3Fh	Max. Latency	RO	0Bh
40-4Bh	Reserved	RO	0
4Ch	Docking Control	R/W,RO	0

4Dh	Docking Status	R/WO,RO	80
50-51h	Power Management Identifiers	RO	0001h
52-53h	Power Management Capabilities	RO	C842h
54-57h	Power Management Control and Status	R/W	0
60-61h	**Internal Test Mode Option**	**R/W**	00002000
70h	**Internal Test Mode Option**	**R/W**	1D8000E4
F0h	SiS HDA internal revision ID	RO	2

Offset 00h: Vendor ID Register

Default Value: 1039h
Length: 2 bytes

Bit	Field Name	Type	Description
15:0	Vendor ID.	RO	This is a 16-bit value assigned to SiS.

Offset 02h: Device ID Register

Default Value: 7502h
Length: 2 bytes

Bit	Field Name	Type	Description
15:0	Device ID	RO	This is a 16-bit value assigned to SiS High Definition Audio Controller.

Offset 04h: Command Register

Default Value: 00h
Length: 2 bytes

Bit	Field Name	Type	Description
15:11	Reserved		
10	INT_DIS	R/W	Disable interrupt assertion (the STS is at 6[3]) 0: Enable interrupt 1: Disable interrupt
9	Fast Back To Back Enable	RO	Not implemented.
8	SERR# Enable	RO	Not implemented.
7	Wait Cycle Control	RO	Not implemented.
6	Parity Error Response	RO	Not implemented.
5	VGA Palette Snoop	RO	Not implemented.
4	Memory write and invalidate enable	RO	Not implemented.

3	Special cycle	RO	Not implemented.
2	Bus master Enable	R/W	Control the capabilities of a PCI device to act as a master device on the PCI bus. 0: Disable 1: Enable
1	Memory space Enable	R/W	Enable the memory space address to the High Definition Audio Controller. 0: Disable 1: Enable
0	IO space Enable	RO	Not implemented.

Offset 06h: Status Register

Default Value: 0210h
Length: 2 bytes

Bit	Field Name	Type	Description
15	Detected Parity Error	RO	Not implemented.
14	Signaled System Error	RO	Not implemented.
13	Received Master Abort	R/WC	Software clears this bit by writing a '1' to it. 0: No master abort received. 1: A master abort happens while DMA running.
12	Received Target Abort	RO	Not implemented.
11	Signaled Target Abort	RO	Not implemented.
10:9	DEVSEL Timing	RO	Sis 7012 always do medium decode. The value is always 2'b01.
8	Data Parity Error Detected	RO	Not implemented.
7	Fast back to back capable	RO	Not implemented.
6	RUDF support	RO	Not implemented.
5	66MHz support	RO	Not implemented.
4	Capabilities List	RO	Hardwired to '1'. The bit indicates this function implements a list of extended capabilities of PCI power management. The 1st item is pointed to by looking at offset 34h.

3	INT_STS	RO	Interrupt status 0: No interrupt or interrupt is cleared. 1: INT# is asserted.
2:0	Reserved		

Offset 08h: Revision ID Register

Default Value: 00h
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Revision ID	RO	This register is hardwired to the value of 00h.

Offset 09h: Class Code Register

Default Value: 040300h
Length: 3 bytes

Bit	Field Name	Type	Description
23:16	Base Class	RO	A constant value of '04h' identifies the device being a multimedia device.
15:8	SUB Class	RO	A constant value of '03h' identifies the device being an High Definition Audio device.
7:0	Programming Interface	RO	A constant value of '00h' identifies the device being an audio device.

Offset 0Ch: Cache Line Size Register

Default Value: 00h
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Cache Line Size	RO	Hardwire to 8'h0.

Offset 0Dh: Latency Timer Register

Default Value: 00h
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Latency Timer	RO	Hardwire to 8'h0.

Offset 0Eh: Header Type Register

Default Value: 00h
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Header Type	RO	Hardwire to 8'h0, single function device.

Offset 10h: High Definition Audio OP Register Base Address Register

Default Value: 00000000h
Length: 4 bytes

Bit	Field Name	Type	Description
31:14	Base Address	R/W	Base address for the High Definition Audio controller's memory mapped configuration registers.
13:1	Reserved	RO	Hardwired to 0's.
0	Memory Space Indicator	RO	Hardwired to 0.

Offset 2Ch: Subsystem Vendor ID

Default Value:1039h
Length: 2 bytes

Bit	Field Name	Type	Description
15:0	Subsystem Vendor ID	R/WO	The register is implemented as write-once register. And it's not affected by the D3hot to D0 transition.

Offset 2Eh: Subsystem ID

Default Value: 1234h
Length: 2 bytes

Bit	Field Name	Type	Description
15:0	Subsystem ID	R/WO	The register is implemented as write-once register. And it's not affected by the D3hot to D0 transition.

Offset 34h: Capabilities Pointer

Default Value: 50h
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Capabilities Pointer	RO	Support PM capabilities at 50h-57h

Offset 3Ch: Interrupt Line Register

Default Value: 00h
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Interrupt Line.	R/W	Programmable.

Offset 3Dh: Interrupt Pin Register

Default Value: 01h
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Interrupt Pin	RO	Always 01h.

Offset 3Eh: Minimum Grant Register

Default Value: 34h
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Minimum Grant	RO	Always 34h.

Offset 3Fh: Maximum Latency Register

Default Value: 0Bh
Length: 1 byte

Bit	Field Name	Type	Description
7:0	Maximum Latency	RO	Always 0Bh.

Offset 4Ch: Docking Controll Register (mobile only)

Default Value: 00h
Length: 1 byte

Bit	Field Name	Type	Description
7:1	Reserved	RO	
0	Docking Attach	RW / RO	Software writes a 1 to this bit to initiate the docking sequence on HDA link. Software writes a 0 to this bit to initiate the undocking sequence on HDA link. Software must check the state of the Dock Mate bit prior to writing the Dock Attach bit. Note: This bit is read only when the Docking Support bit = 0

Offset 4Dh: Docking Status Register (mobile only)

Default Value: 80h
Length: 1 byte

Bit	Field Name	Type	Description
7	Docking Support	R/WO	A 1 indicates the HDA controller supports HDA CODEC docking. BIOS needs to check the Docking Support bit before the HDA initialization sequence. BIOS may clear this bit to 0 to disable the docking feature.
6:1	Reserved	RO	
0	Dock Mate	RO	This bit is used for software to identify the HDA docked CODEC is connected or not.

Offset 50h: Power Management Identifies

Default Value: 0001h
Length: 2 bytes

Bit	Field Name	Type	Description
15:8	Next Item Pointer	RO	Hardwired to 0's. (No other capabilities)

7:0	CAP_ID	RO	It indicates the link list item as being the PCI power management registers

Offset 52h: Power Management Capabilities

Default Value: C842h
Length: 2 bytes

Bit	Field Name	Type	Description
15:11	PM Capabilities	RO	The 5 bits indicates the power states in which the function may assert PME#. Bit (15): 1xxxxb – PME# can be asserted from D3_cold Bit (14): x1xxxb – PME# can be asserted from D3_hot Bit (13): xx1xxb – PME# can be asserted from D2 Bit (12): xxx1xb – PME# can be asserted from D1 Bit (11): xxxx1b – PME# can be asserted from D0
10	D2 support	RO	Not implemented.
9	D1 support	RO	Not implemented.
8:6	AUX current	RO	The 3 bits field reports the 3.3V_aux requirement for the PCI function. ‘001’ means 55mA.
5	DSI	RO	Hardwired to 0. Device Specific Initialization bit indicates whether the special of the function is requirement.
4	Reserved		
3	PME_CLK	RO	Hardwired to 0.
2:0	Version	RO	Hardwired to 010b. It indicates that the function complies with Revision 1.1 of the PCI Power Management Interface Specification.

Offset 54h: Power Management Control and Status

Default Value: 00000000h
Length: 4 bytes

Bit	Field Name	Type	Description
31:16	Reserved	RO	
15	PME Status	R/WC	This bit is set when the function would normally assert the PME# signal independent of the state of the PME Enable bit. Writing a ‘1’ to this bit will clear it and cause the function to stop asserting a PME# (if enabled). Writing a ‘0’ has no effect. Default value is ‘0’.
14	Data Scale	RO	Not implemented.
12:9	Data Select	RO	Not implemented.
8	PME Enable	R/W	A ‘1’ enables the function to assert PME#. When ‘0’, PME# assertion is disabled. Default value is ‘0’.
7:2	Reserved	RO	
1:0	Power State	R/W	This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the field values is given below: 00b – D0 11b – D3hot

			If software attempts to write an unsupported, optional state to this field, the data is discarded and no state change occurs. When in the D3hot state, the High Definition Audio's configuration space is available, but the operating register space is not. Additionally, the interrupts are blocked.

Offset 60h: Internal Test Mode Option 1

Default Value: 00002000h
Length: 4 bytes

Bit	Field Name	Type	Reset	Description
31:13	Reserved	R/W	-	Reserved
12	os_cad_dcc_en	R/W	1'b0	0 = OSCAD dynamic clocking gating is disable 1 = OSCAD dynamic clocking gating is enable
11	is4_dcnt_dcc_en	R/W	1'b0	0 = IS4 dynamic clocking gating is disable 1 = IS4 dynamic clocking gating is enable
10	is3_dcnt_dcc_en	R/W	1'b0	0 = IS3 dynamic clocking gating is disable 1 = IS3 dynamic clocking gating is enable
9	is2_dcnt_dcc_en	R/W	1'b0	0 = IS2 dynamic clocking gating is disable 1 = IS2 dynamic clocking gating is enable
8	is1_dcnt_dcc_en	R/W	1'b0	0 = IS1 dynamic clocking gating is disable 1 = IS1 dynamic clocking gating is enable
7	os4_dcnt_dcc_en	R/W	1'b0	0 = OS4 dynamic clocking gating is disable 1 = OS4 dynamic clocking gating is enable
6	os3_dcnt_dcc_en	R/W	1'b0	0 = OS3 dynamic clocking gating is disable 1 = OS3 dynamic clocking gating is enable
5	os2_dcnt_dcc_en	R/W	1'b0	0 = OS2 dynamic clocking gating is disable 1 = OS2 dynamic clocking gating is enable
4	os1_dcnt_dcc_en	R/W	1'b0	0 = OS1 dynamic clocking gating is disable 1 = OS1 dynamic clocking gating is enable
3	Reserved	R/W	1'b0	Reserved in p968
2	sdi2_norm_dcc_en	R/W	1'b0	0 = sdi2 static clocking gating is disable 1 = sdi2 static clocking gating is enable
1	sdi1_norm_dcc_en	R/W	1'b0	0 = sdi1 static clocking gating is disable 1 = sdi1 static clocking gating is enable
0	sdi0_norm_dcc_en	R/W	1'b0	0 = sdi0 static clocking gating is disable 1 = sdi0 static clocking gating is enable

Offset 70h: Internal Test Mode Option 2

Default Value: 1D8000E4h
Length: 4 bytes

Bit	Field Name	Type	Reset	Description
31:1	Reserved	R/W	-	Reserved
0	dcc_en	R/W	1'b0	0 = AZ dynamic clocking gating is disable 1 = AZ dynamic clocking gating is enable

8.2. High Definition Audio Memory Space Operating Registers

8.2.1. High Definition Audio Operating Register

Offset	Register function	Type	Reset Value
00-01h	Global Capability	RO	4400h
02	Minor Version	RO	0
03	Major Version	RO	01h
04-05h	Output Payload Capability	RO	003Ch
06-07h	Input Payload Capability	RO	001Dh
08-0Bh	Global Control	R/W	0
0C-0Dh	Wake Enable	R/W	0
0E-0Fh	Wake Status	R/WC	0
10-11h	Global Status	R/WC	0
14h	Extended Capabilities	R/WO	1
18-19h	Output Stream Payload	RO	003Ch
1A-1Bh	Input Stream Payload	RO	001Dh
20-23h	Interrupt Control	R/W	0
24-27h	Interrupt Status	RO	0
30-33h	Wall Clock Counter	RO	0
38-3Bh	Stream Synchronization	R/W	0
40-43h	CORB Lower Base Address	R/W, RO	0
44-47h	CORB Upper Base Address	RO	0
48-49h	CORB Write Pointer	R/W	0
4A-4Bh	CORB Read Pointer	W, RO	0
4Ch	CORB Control	R/W	0
4Dh	CORB Status	R/WC	0
4Eh	CORB Size	RO	42h
50-53h	RIRB Lower Base Address	R/W, RO	0
54-57h	RIRB Upper Base Address	RO	0
58-59h	RIRB Write Pointer	W, RO	0
5A-5Bh	RIRB Interrupt Count	R/W	0
5Ch	RIRB Control	R/W	0
5Dh	RIRB Status	R/WC	0
5Eh	RIRB Size	RO	42h
60-63h	Immediate Command Write	R/W	0
64-67h	Immediate Response Read	RO	0
68-69h	Immediate Command Status	RO, R/WC	0
70-73h	DMA Position Lower Base Address	R/W, RO	0
74-77h	DMA Position Upper Base Address	R/W	0
80-82h	Input Stream Descriptor 1(ISD1) Control	R/W, RO	0
83	ISD1 Status	RO, R/WC	0
84-87h	ISD1 Link Position in Current Buffer	RO	0
88-8Bh	ISD1 Cyclic Buffer Length	R/W	0
8C-8Dh	ISD1 Last Valid Index	RO, R/W	0
90-91h	ISD1 FIFO Size	RO	3Fh

92-93h	**ISD1 Format**	**R/W**	**0010h**
98-9Bh	ISD1 Buffer Descriptor Pointer – Lower Base Address	R/W, RO	0
9C-9Fh	ISD1 Buffer Descriptor Pointer – Upper Base Address	RO	0
A0-FFh	Additional Input Stream Descriptors A0-BF: ISD2 operating registers C0-DF: ISD3 operating registers E0-FF: ISD4 operating registers (total 4 input streams)		
100-102h	Output Stream Descriptor 1(OSD1) Control	R/W, RO	0
103	OSD1 Status	RO, R/WC	0
104-107h	OSD1 Link Position in Current Buffer	RO	0
108-10Bh	OSD1 Cyclic Buffer Length	R/W	0
10C-10Dh	OSD1 Last Valid Index	RO, R/W	0
110-111h	OSD1 FIFO Size	RO	3Fh
112-113h	OSD1 Format	**R/W**	**0010h**
118-11Bh	OSD1 Buffer Descriptor Pointer – Lower Base Address	R/W, RO	0
11C-11Fh	OSD1 Buffer Descriptor Pointer – Upper Base Address	RO	0
120-17Fh	Additional Output Stream Descriptors 140-15F: OSD2 operating registers 140-15F: OSD3 operating registers 160-17F: OSD4 operating registers (total 4 output streams)		
2030-2033h	Wall Clock Counter Alias	RO	0
2084-2087h	ISD1 Link Position in Current buffer	RO	0
20A4-20A7h	ISD2 Link Position in Current buffer	RO	0
20C4-20C7h	ISD3 Link Position in Current buffer	RO	0
20E4-20E7h	ISD4 Link Position in Current buffer	RO	0
2104-2107h	OSD1 Link Position in Current buffer	RO	0
2124-2127h	OSD2 Link Position in Current buffer	RO	0
2144-2147h	OSD3 Link Position in Current buffer	RO	0
2164-2167h	OSD4 Link Position in Current buffer	RO	0

Offset 00h: GCAP – Global Capabilities

Default Value: 4400h

Length: 2 bytes

Bit	Type	Reset	Description
15:12	RO	4	**Number of Output Streams Supported (OSS):** A value of 0000b indicates that there is no Output Stream supported. A value of maximum 15 Output Streams are supported. 0000b: No output stream supported 0001b: 1 output stream supported … 1111b: 15 output stream supported

11:8	RO	4	**Number of Input Streams Supported (ISS):** A value of 0000b indicates that there is no Input Stream supported. A value of maximum 15 Input Streams are supported. 0000b: No input stream supported 0001b: 1 input stream supported … 1111b: 15 input stream supported
7:3	RO	0	**Number of Bi-directional Streams Supported (BSS):** A value of 0000b indicates that there is no Bi-directional Stream supported. A value of maximum 30 Bi-directional Streams is supported. 00000b: No bi-directional stream supported 00001b: 1 bi-directional stream supported … 11110b: 30 bi-directional stream supported
2	RsvdP	0's	
1	RO	0	**Number of Serial Data Out Signals (NSDO):** A '0' indicates that one SDO line is supported; a '1' indicates that two SDO lines are supported. Software can enable the use of striping by setting the appropriate bit in the Stream Buffer Descriptor. 0: 1 SDO 1: 2 SDOs
0	RO	0	**64 Bit Address Supported (64OK):** A '1' indicates that the 64 bit addressing is supported by the controller for BDL addresses, data buffer addresses, and command buffer addresses. A '0' indicates that only the 32 bit addressing is available.

Table 3: Global Capabilities

Offset 02h: VMIN – Minor Version

Default Value: 00h

Length: 1 byte

Bit	Type	Reset	Description
7:0	RO	00h	**Minor Version (VMIN):** indicates minor revision number 00h of the High Definition Audio specification.

Table 4: Minor Version

Offset 03h: VMAJ – Major Version

Default Value: 01h

Length: 1 byte

Bit	Type	Reset	Description
7:0	RO	01h	**Major Version (VMAJ):** indicates major revision number 1 of

			the High Definition Audio specification.

Table 5: Major Version

Offset 04h: OUTPAY – Output Payload Capability

Default Value: 003Ch

Length: 2 bytes

Bit	Type	Reset	Description
15:7	RO	0's	**Reserved**
6:0	RO	3Ch	**Output Payload Capability (OUTPAY):** indicates the total output payload available on the link. This doesn't include bandwidth used for command and control. This measurement is in 16 bits word quantities per 48kHz frame. The default link clock speed of 24.000MHz (the data is double pumped) provides 1000 bits per frame, or 62.5 words in total. 40 bits (2.5 words) are used for command and control, leaving 60 words available for data payload. 00h: 0 word payload 01h: 1 word payload … FFh: 255 word payload

Table 6: Output Payload Capability

Offset 06h: INPAY – Input Payload Capability

Default Value: 001Dh

Length: 2 bytes

Bit	Type	Reset	Description
15:7	RO	0's	**Reserved**
6:0	RO	1Dh	**Input Payload Capability (INPAY):** indicates the total input payload available on the link. This doesn't include bandwidth used for command and control. This measurement is in 16 bits word quantities per 48kHz frame. The default link clock speed of 24.000MHz provides 500 bits per frame, or 31.25 words in total. 36 bits (2.25 words) are used for command and control, leaving 29 words available for payload. This measurement is on a per-CODEC basis. 00h: 0 word payload 01h: 1 word payload … FFh: 255 word payload

Table 7: Input Payload Capability

Offset 08h: GCTL – Global Control

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:9	RsvdP	0's	**Reserved**
8	R/W	0	**Accept Unsolicited Response Enable (UNSOL):** if UNSOL is a '1', Unsolicited Response from the CODEC(s) are accepted by the controller and placed into the RIRB. If UNSOL is a '0', Unsolicited Responses are not accepted, and dropped on the floor.
7:4	RsvdP	0's	**Reserved**
3	R/W	0's	**Dock Mated Interrupt Enable (DMIE)** 0 = Disable 1 = Enable. The DMIE bit is enabled to generate an interrupt while the docking status is asserted.
2	R/W	0's	**Dock Attach** Software writes a 1 to this bit to initiate the docking sequence on HDA link. Software writes a 0 to this bit to initiate the undocking sequence on HDA link. Software must check the state of the Dock Mate bit prior to writing the Dock Attach bit. Note: This bit is read only when the Docking Support bit = 0
1	R/W	0	**Flush Control (FCNTRL):** Writing a '1' to this bit indicates a flush. The flush is complete when Flush Status is set. Before a flush cycle is initiated, the DMA Position Buffer must be programmed with a valid memory address by software, but the DMA Position Buffer bit 0 needn't be set to enable the position reporting mechanism. Also, all streams must be stopped (the associated RUN bit must be '0'). When the flush is initiated, the controller will flush pipelines to memory to guarantee that the hardware is ready to transition to a D3 state. Setting this bit is not a critical step in the power state transition if the content of the FIFO(s) is not critical.
0	R/W	0	**Controller Reset (CRST):** Writing a 0 to this bit causes the High Definition Audio controller to be reset. All state machines, FIFO(s) and memory mapped configuration registers (not PCI Configuration Registers) in the controller will be reset. The High Definition Audio link RESET# signal will be asserted and all other link signals will be driven to their "reset" values. After the hardware has completed sequencing into the reset state, it will report a 0 in this bit. Software must read a '0' from this bit to verify that the controller is in reset. Writing a 1 to this bit causes the controller to exit its reset state and de-assert the High Definition Audio link RESET# signal. Software is responsible for setting/clearing this bit such that the minimum High Definition Audio link RESET# signal

			assertion pulse width specification is met. When the controller hardware is ready to begin operation, it will report a 1 in this bit. Software must read a 1 from this bit before accessing any controller registers. The CRST# bit defaults to a 0 after hardware reset, therefore software needs to write a 1 to this bit to begin operation. Note that the CORB/RIRB RUN bits and all Stream RUN bits must be verified cleared to zero before CRST# is written to zero (asserted) in order to assure a clean re-start. In setting or clearing CRST software must ensure that minimum link timing requirement, such as the minimum allowable time for RESET# to be enabled, are met. When CRST is 0 indicating that the controller is in reset, most registers will return to their default values on reads, and writes will have no effect. The exceptions are the WAKEEN and STATESTS registers, which are only cleared on power-on reset, and the CRST bit it's self, which will cause the controller to leave the reset state when a 1 is written to it.

Table 8: Global Control Register

Offset 0Ch: WAKEEN – Wake Enable (AUX plane)

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15	RsvdP	0	**Reserved**
14:0	R/W RSM	0's	**SDIN Wake Enable (SDIWEN):** Bits that control which SDIN signal(s) may generate a wake up event in response to a CODEC State Change request. A '1' bit in the bit mask indicates that the associated SDIN signal is enabled to generate a wake. The SDATA_IN[0] line corresponds to bit 0, etc. These bits are only cleared by a power-on reset. Software must make no assumptions about how these bits are set, and set them appropriately.

Table 9: Wake Enable

Offset 0Eh: STATESTS – State Change Status (AUX plane)

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15	RsvdZ	0	**Reserved**
14:0	R/W1CS RSM	0's	**SDIN State Change Status Flags (SDIWAKE):** Flag bits that indicate which SDIN signal(s) received a "State Change" event. The bits are cleared by writing 1's to them. The

			SDATA_IN[0] line corresponds to bit 0, etc. These bits are only cleared by a power-on reset.

Table 10: Wake Status

Offset 10h: GSTS – Global Status

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15:4	RsvdZ	0's	**Reserved**
3	R/W1C	0's	**Dock Mated Interrupt Status (DMIS)** A 1 indicates that the dock mating or unmating process has completed. Note that this bit is set regardless of the state of the DMIE bit.
2	RO	0's	**Dock Mate (DM)** This bit is used for software to identify the HDA docked CODEC is connected or not.
1	R/W1C	0	**Flush Status (FSTS):** This bit is set to a '1' by the hardware to indicate that the flush cycle initiated when the FCNTRL bit was set has completed. Software must write a '1' to clear this bit before the next time FCNTRL is set to clear the bit.
0	RsvdZ	0	**Reserved**

Table 11: Global Status

Offset 14h: ECAP – Extended Capabilities

Default Value: 01h

Length: 1 bytes

Bit	Type	Reset	Description
7:1	RsvdZ	0's	**Reserved**
0	R/WO	1	**Docking Supported (DS)** A 1 indicates the HDA controller supports HDA CODEC docking. BIOS needs to check the Docking Support bit before the HDA initialization sequence. BIOS may clear this bit to 0 to disable the docking feature.

Offset 18h: OUTSTRMPAY – Output Stream Payload Capability

Default Value: 00000h

Length: 2 bytes

Bit	Type	Reset	Description
15:0	RO	3Ch	**Output Stream Payload Capability (OUTSTRMPAY):** Indicates the maximum number of Words per frame for any

			single output stream. This measurement is in 16-bit Word quantities per 48-kHz frame. The value must not be larger than the OUTPAY register value. Software must ensure that a format which would cause more Words per frame than indicated is not programmed into the Output Stream Descriptor Register. 00h: No Limit (Stream size is limited only by OUTPAY) 01h: 1 Word payload … FFh: 255h Word payload

Table 12. Output Payload Capability

Offset 1Ah: INSTRMPAY – Input Stream Payload Capability

Default Value: 00000h

Length: 2 bytes

Bit	Type	Reset	Description
15:0	RO	1Dh	**Input Stream Payload Capability (INSTRMPAY):** Indicates the maximum number of Words per frame for any single input stream. This measurement is in 16-bit Word quantities per 48-kHz frame. The value must not be larger than the INPAY register value. Software must ensure that a format which would cause more Words per frame than indicated is not programmed into the Input Stream Descriptor Register. 00h: No Limit (Stream size is limited only by INPAY) 01h: 1 Word payload … FFh: 255h Word payload

Table 13. Input Payload Capability

Offset 20h: INTCTL – Interrupt Control

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31	R/W	0	**Global Interrupt Enable (GIE):** Global bit to enable device interrupt generation. When set to 1 the High Definition Audio device is enabled to generate an interrupt. This control is in addition to any bit in the bus specific address space, such as the Interrupt Enable bit in the PCI Configuration space.
30	R/W	0	**Controller Interrupt Enable (CIE):** Enables the general interrupt for controller functions. When set to 1 the controller generates an interrupt when the corresponding status bit get sets due to a Response Interrupt, a Response Buffer Overrun,

			and wake events.
29:0	R/W	0's	**Stream Interrupt Enable (SIE):** When set to 1 the individual Streams are enabled to generate an interrupt while the corresponding stream status bit get set. A stream interrupt will be caused as a result of a buffer with IOC=1 in the BDL entry being complete, or as a result of a FIFO error (under-run or over-run) occurring. Control over the generation of each of these sources is in the associated Stream Descriptor. These streams are numbered and the SIE bits assigned sequentially, base on their order in the register set. For instance, if there are four input streams, and four output streams, and no bi-directional stream (ISS=4, OSS=4, BSS=0), the bit assignments would be as follows: Bit 0: Input Stream 1 Bit 1: Input Stream 2 Bit 2: Input Stream 3 Bit 3: Input Stream 4 Bit 4: Output Stream 1 Bit 5: Output Stream 2 Bit 6: Output Stream 3 Bit 7: Output Stream 4 Bit 8-26: Reserved

Table 14: Interrupt Control Register

Offset 24h: INTSTS – Interrupt Status

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31	RO	0	**Global Interrupt Status (GIS):** This bit is an OR of all of the interrupt status bits in this register.
30	RO	0	**Controller Interrupt Status (CIS):** Status of general controller interrupt. This bit may be set regardless of the corresponding enable bit, but a HW interrupt will not be generated unless the corresponding enable bit is set. A 1 indicates that an interrupt condition occurred due to a Response Interrupt, a Response Overrun, or a CODEC State Change request. The exact cause can be determined by interrogating the RIRB Status register and the State Change Status register. Note that this bit is set regardless of the state of the corresponding interrupt enable bit. This bit is cleared by writing a 1.
29:0	RO	0's	**Stream Interrupt Status (SIS):** A 1 indicates that an interrupt

			condition occurred on the corresponding Stream. Note that these status bits are set regardless of the state of the corresponding interrupt enable bits. The bits are cleared by writing 1's to them. The streams are numbered and the SIS bits assigned sequentially, based on their order in the register set in the same was the SIE bits are set. Bit 0: Input Stream 1 Bit 1: Input Stream 2 Bit 2: Input Stream 3 Bit 3: Input Stream 4 Bit 4: Output Stream 1 Bit 5: Output Stream 2 Bit 6: Output Stream 3 Bit 7: Output Stream 4 Bit 8-26: Reserved

Table 15: Interrupt Status Register

Offset 30h: Wall Clock Counter

The 32 bits monotonic counter provides a 'wall clock' that can be used by system software to synchronize independent audio controllers. The counter must be implemented.

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	RO	0's	**Wall Clock Counter (Counter):** 32 bits counter that is incremented at the link bit clock rate and rolls over from FFFF_FFFFh to 0000_0000h. The counter will roll over to zero with a period of approximately 179 seconds. This counter is enabled while the BCLK starts running. Software uses this counter to synchronize between multiple controllers. The counter will be reset on controller reset.

Table 16: Wall Clock Counter

Offset 38h: SSYNC – Stream Synchronization

The Stream Synchronization bits provide a mechanism for synchronously starting or stopping two or more streams so that the streams have a common time reference.

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:30	RsvdP	0's	**Reserved**
29:0	R/W	0's	**Stream Synchronization Bits (SSYNC):** The Stream Synchronization Bits, when set, block data from being sent on

			or received from the link. Each bit controls the associated Stream Descriptor; bit 0 corresponds to the first Stream Descriptor, etc. To synchronously start a set of DMA engines, the bits in the SSYNC register are set to a 1. The RUN bits for the associated Stream Descriptors can be set to a 1 to start the DMA engines. When all streams are ready, the associated SSYNC bits can all be set to 0 at the same time, and transmission or reception of bits to or from the link will begin together at the start of the next full link frame. To synchronously stop streams, the bits are set in the SSYNC register, and the RUN bits in the Stream Descriptors are cleared by software. Note that some register may be. Bit 0: Input Stream 1 Bit 1: Input Stream 2 Bit 2: Input Stream 3 Bit 3: Input Stream 4 Bit 4: Output Stream 1 Bit 5: Output Stream 2 Bit 6: Output Stream 3 Bit 7: Output Stream 4 Bit 8-26: Reserved

Table 17: Stream Synchronization

Offset 40h: CORBLBASE – CORB Lower Base Address

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:7	R/W	0's	**CORB Lower Base Address (CORBLBASE):** Lower address of the CORB allowing the CORB Base Address to be assigned on any 1KB boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	RO	0's	**CORB Lower Base Unimplemented bits:** Hardwire to 0. This requires the CORB to be allocated with 128 bytes granularity to allow for cache line fetch optimizations.

Table 18: CORB Lower Base Address

Offset 44h: CORBUBASE – CORB Upper Base Address

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	RO	0's	**CORB Upper Base Address (CORBUBASE):** Upper 32 bits of address of the CORB. This register field must not be written

			when the DMA engine is running or the DMA transfer may be corrupted. This register is reserved, read only 0 if the 64OK bit indicates that controller doesn't support 64 bits addressing.

Table 19: CORB Upper Base Address

Offset 48h: CORBWP – CORB Write Pointer

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15:8	RsvdP	0's	**Reserved**
7:0	R/W	0's	**CORB Write Pointer (CORBWP):** Software writes the last valid CORB entry offset into the field in D-word granularity. The DMA engine fetches commands form the CORB until the Read Pointer matches the Write Pointer. Supports up to 256 CORB entries (256*4B=1KB). This field may be written while the DMA engine is running.

Table 20: CORB Write Pointer

Offset 4Ah: CORBRP – CORB Read Pointer

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15	W	0	**CORE Read Pointer Reset (CORBRPRST):** Software writes a 1 to this bit to reset the CORB Read Pointer to 0. The DMA engine must be stopped prior to resetting the Read Pointer or else DMA transfer may be corrupted. This bit will always be read as 0. (following the HDA spec 1.0)
14:8	RsvdP	0's	**Reserved**
7:0	RO	0's	**CORB Read Pointer (CORBRP):** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB Read Pointer offset in D-word granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports up to 256 CORB entries (256*4B=1KB) in the cyclic CORB buffer. This field may be read while the DMA engine is running.

Table 21: CORB Read Pointer

Offset 4Ch: CORBCTL – CORB Control

Default Value: 00h

Length: 1 byte

Bit	Type	Reset	Description
7:2	RsvdP	0's	**Reserved**
1	R/W	0	**Enable CORB DMA Engine (CORBRUN):** 0=DMA Stop 1=DMA Run (when Read Pointer lags Write Pointer) After SW writes a 0 to this bit, the HW may NOT stop immediately until the current frame is completed. SW must to read a 0 from this bit to verify the DMA engine is truly stopped, than SW can start another DMA Run.
0	R/W	0	**CORB Memory Error Interrupt Enable (CMEIE):** If this bit is set, the controller will generate and interrupt if the MEI status bit is set.

Table 22: CORB Control

Offset 4Dh: CORBSTS – CORB Status

Default Value: 00h

Length: 1 byte

Bit	Type	Reset	Description
7:1	RsvdZ	0's	**Reserved**
0	R/W1C	0	**CORB Memory Error Indication (CMEI):** If this status bit is set, the controller has detected an error in the pathway between the controller and memory. This may be an ECC bit error or any other type of detectable data error which renders the command data fetched invalid. Writing a '1' to this bit will clear the bit, but a CRST must be performed before operation continues as this indicates a severe machine error has occurred, and the current state is not trustable.

Table 23: CORB Status

Offset 4Eh: CORBSIZE – CORB Size

Default Value: 42h

Length: 1 byte

Bit	Type	Reset	Description
7:4	RO	0100	**CORB Size Capability (CORBSZCAP):** A bit mask indicating the size of the CORB supported by the controller. Bits[7:4] / CORB Size 0001 / 8B = 2 entries 0010 / 64B = 16 entries 0100 / 1024B = 256 entries 1000 / Reserved This implemented as a bit mask, for example, if the controller supported 2 entries and 256 entries, this register would have

			a value of 0101b.
3:2	RsvdP	0	**Reserved**
1:0	RO	10	**CORB Size (CORBSIZE):** The setting of the register determines when the address counter in the DMA controller will wrap around.

Bits[1:0]	CORB Size
00	8B = 2 entries
01	64B = 16 entries
10	1KB = 256 entries
11	Reserved

Table 24: CORB Size

Offset 50h: RIRBLBASE – RIRB Lower Base Address

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:7	R/W	0's	**RIRB Lower Base Address (RIRBLBASE):** Lower address of the Response Input Ring Buffer, allowing the RIRB Base Address to be assigned on any 2KB boundary. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.
6:0	RO	0's	**RIRB Lower Base Unimplemented Bits:** Hardwared to 0 to force 128 byte buffer alignment for cache line fetch optimizations.

Table 25: RIRB Lower Base Address

Offset 54h: RIRBUBASE – RIRB Upper Base Address

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	RO	0's	**RIRB Upper Base Address (RIRBUBASE):** Upper 32 bits of address of the Response Input Ring Buffer. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. This register is reserved, read only '0' if the 64OK bit indicates that the controller does not support 64 bit addressing.

Table 26: RIRB Upper Base Address

Offset 58h: RIRBWP – RIRB Write Pointer

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15	W	0	**RIRB Write Pointer Reset (RIRBWPRST):** Software writes a 1 to this bit to reset the RIRB Write Pointer and to 0's. The DMA engine must be stopped prior to resetting the Write Pointer or else DMA transfer may be corrupted. This bit will always be read as 0. (following the HDA spec 1.0)
14:8	RsvdP	0's	**Reserved**
7:0	RO	0's	**RIRB Write Pointer(RIRBWP)** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determine how many responses it can read from the RIRB. The value read indicates the RIRB Write Pointer offset in 2 Dword units (since each RIRB entry is 2 Dwords long). Supports up to 256 RIRB entries (256 x8B=2KB) in the cyclic RIRB buffer. This field may be read while the DMA engine is running.

Table 27: RIRB Write Pointer

Offset 5Ah: RINTCNT – Response Interrupt Count

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15:8	RsvdP	0's	**Reserved**
7:0	R/W	00h	**N Response Interrupt Count (RINTCNT):** 0000_0001b = 1 Response sent to RIRB …….. 1111_1111b = 255 Responses sent to RIRB 0000_0000b =256 Responses sent to RIRB The DMA engine should be stopped when changing this field or else an interrupt may be lost. Note that each Response occupies 2 Dwords in the RIRB. This is compared to the total number of responses that have been returned, as opposed to the number of frames in which there were responses. If more than one CODEC responds in one frame, then the count is increased by the number of responses received in the frame.

Table 28: RIRB Response Interrupt Count

Offset 5Ch: RIRBCTL – RIRB Control

Default Value: 00h

Length: 1 byte

Bit	Type	Reset	Description
7:3	RsvdP	0's	**Reserved**
2	R/W	0	**Response Overrun Interrupt Control (RIRBOIC):** If this bit is set, the hardware will generate an interrupt when the Response Overrun Interrupt Status bit (5Dh[2]) is set.
1	R/W	0	**RIRB DMA Enable (RIRBDMAEN)** 0 = DMA Stop 1 = DMA Run After SW writes a 0 to this bit, the HW may NOT stop immediately until the current frame is completed. SW must to read a 0 from this bit to verify the DMA engine is truly stopped, than SW can start another DMA Run.
0	R/W	0	**Response Interrupt Control (RINTCTL):** 0 = Disable Interrupt 1 = Generate an interrupt after N number of Responses are sent to the RIRB buffer OR when an empty Response slot in encountered on all SDATA_IN_x inputs after a frame which returned a response (whichever occurs first). The N counter is reset when the interrupt is generated.

Table 29: RIRB Control

Offset 5Dh: RIRBSTS – RIRB Status

Default Value: 00h

Length: 1 byte

Bit	Type	Reset	Description
7:3	RsvdZ	0's	**Reserved**
2	R/W1C	0	**Response Overrun Interrupt Status (RIRBOIS):** Hardware sets this bit to a 1 when an overrun occurs in the RIRB. An interrupt may be generated if the Response Overrun Interrupt Control bit is set. This bit will be set if the RIRB DMA engine is not able to write the incoming responses to memory before additional incoming response overrun the internal FIFO. When hardware detects an overrun the hardware will drop the responses that overrun the buffer and set the RIRBOIS status bit to indicate the error condition. Optionally, if the RIRBOIS is set the hardware will also generate an error to alert software to the problem. Software clears this bit by writing a '1' to it.
1	RsvdZ	0	**Reserved**
0	R/W1C	0	**Response Interrupt (RINTFL):** Hardware sets this bit to a 1 when an interrupt has been generated after N number of Responses are sent to RIRB buffer OR when an empty Response slot is encountered on all SDATA_IN[x] inputs (whichever occurs first).

			Software clears this flag by writing a 1 to this bit.

Table 30: RIRB Status

Offset 5Eh: RIRBSIZE – RIRB Size

Default Value: 42h

Length: 1 byte

Bit	Type	Reset	Description
7:4	RO	0100	**RIRB Size Capability (RIRBSZCAP):** A bit mask identifying the possible sizes of the RIRB Bits[7:4] – RIRB Size 0001 – 16B = 2 entries 0010 – 128B = 16 entries 0100 – 2048B = 256 entries 1000 – Reserved This implemented as a bit mask, for example, if the controller supported 2 entries and 256 entries, this register would have a value of 0101b.
3:2	RsvdP	0	**Reserved**
1:0	RO	10	**RIRB Size (RIRBSIZE):** The setting of the register determines when the address counter in the DMA controller will wrap around. Bits[1:0] – RIRB Size 00 – 16B = 2 entries 01 – 128B = 16 entries 10 – 2048B = 256 entries 11 – Reserved This value must not be changed when the RIRB DMA engine is enabled.

Table 31: RIRB Size

Offset 60h: Immediate Command Output Interface

The Immediate Command Output and Immediate Command Input registers are optional registers that provide a Programmed I/O (PIO) interface for sending verbs and receiving responses from CODEC(s). These registers can be implemented in plate forms not suited for DMA command operations. If implemented, these registers must not be used at the same time as the CORB and RIRB command/response mechanisms, as the operations will conflict.

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description

31:0	R/W	0's	**Immediate Command Write (ICW):** The value written into this register is sent out over the link during the next available frame. Software must ensure that the ICB bit in the Immediate Command Status register is clear before writing a value into this register or undefined behavior will result.

Table 32: Immediate Command Output Interface

Offset 64h: Immediate Response Input Interface

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	R/W	0's	**Immediate Response Read (IRR):** The value in this register latches the last response to come in over the link. If multiple CODEC(s) responded in the same frame, there is no guarantee as to which response will be saved here, but the address of the CODEC is indicated in the ICRADD field of the Immediate Command Status register.

Table 33: Immediate Command Input Interface

Offset 68h: Immediate Command Status

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15:8	RsvdZ	0's	**Reserved**
7:4	RO	0's	**Immediate Response Result Address (IRRADD):** The address of the CODEC that sent the response currently latched into the Immediate Response Input register.
3	RO	0	**Immediate Response Result Unsolicited (IRRUNSOL):** Indicates whether the response latched in the Immediate Response Input register is a solicited or unsolicited response.
2	RsvdZ	0	**Reserved**
1	R/W1C	0	**Immediate Result Valid (IRV):** This bit is set to a 1 by hardware when a new response is latched into the IRR register. Software must clear this bit before issuing a new command by writing a 1 to it so that the software may determine when a new response has arrived.
0	R/W	0	**Immediate Command Busy (ICB):** This bit is a 0 when the controller can accept an Immediate command. Software must wait for this bit to be '0' before writing a value in the ICW register. This bit will be clear (indicating ready) when the following conditions are met: (1) the link is running, (2) the CORB is not active (CORBRP = CORBWP or CORBEN is not set) and (3)

			there is not an immediate command already in the queue waiting to be sent. Because software controls each of these conditions, this bit will not transition to a 1 after being read a 0 without explicit software operations to cause one of the above conditions to change. Writing a 1 to this bit will cause the contents of the ICW register to be sent as a verb in the next frame. Once a response is received the IRV bit will be set and this bit will be cleared indicating ready to transmit another verb.

Table 34: Immediate Command Status

Offset 70h: DPLBASE – DMA position Lower Base Address

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:7	R/W	0's	**DMA Position Lower Base Address (DPLBASE):** Lower 32 bits of the DMA Position Buffer Base Address. This register field must not be written when any DMA engine is running or the DMA transfer may be corrupted. This same address is used by the Flush Control and must be programmed with a valid value before the FLCNRTL bit is set.
6:1	RO	0's	**DMA Position Lower Base Unimplemented Bits:** Hardware to 0 to force 128 byte buffer alignment for cache line write optimizations.
0	R/W	0	**DMA Position Buffer Enable:** When this bit is set to a '1', the controller will write the DMA positions of each of the DMA engines to the buffer in main memory periodically. Software can use this value to know what data in memory is valid data. The controller must guarantee that the values in the DMA Position Buffer that the software can read represent positions in the stream for which valid data exists in the Stream's DMA buffer. This has particular relevance in systems which support isochronous transfer, the stream positions in the software-visible memory buffer must represent stream data which has reached the Global Observation point.

Table 35: DMA Position Lower Base Address

Offset 74h: DPUBASE – DMA position Upper Base Address

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	RO	0's	**DMA Position Upper Base Address:**

			Upper 32 bits of address of the DMA Position Buffer Base Address. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted.

Table 36: DMA Position Upper Base Address

The Stream Descriptor registers control the DMA engines that transfer the payload data to and from the High Definition Audio Link. The Input, Output, and Bi-directional descriptors share the same definition, with minor changes in the definitions of some bits to accommodate the slightly different behavior of the engines.

Offset 80h: {IOB}SDnCTL – Input/Output/Bi-directional Stream Descriptor n Control

Default Value: 000000h

Length: 3 bytes

Bit	Type	Reset	Description
23:20	R/W	0's	**Stream Number (STRM):** This value reflects the Tag associated with the data being transferred on the link. When data controlled by the descriptor is sent out over the link, it will have this stream number encoded on the SYNC signal. When an Input Stream is detected on any of the SDATA_Inx signals that match this value, the data samples are loaded into the FIFO associated with the descriptor. Note that while a single SDATA_Inx input may contain data from more than one stream number, two different SDATA_Inx inputs may not be configured with the same stream number. 0000 = Reserved (Indicates Unused) 0001 = Stream 1 … 1110 = Stream 14 1111 = Stream 15
19	RO	0	**Bi-directional Direction Control (DIR):** (Bi-directional engines only. Read-Only zero for engines that are not bi-directional) For a bi-directional engine, determines the direction in which the bi-directional engine should operate. This bit can only be changed after stream reset (SRST) has been asserted and cleared, and before any other stream registers have been programmed. Because setting this bit changes the fundamental behavior of the stream and the meaning of some bits, changing this bit after any other register in the stream descriptor has been written to may lead to undetermined results. 0 = Bi-directional engine is configured as an Input Engine

			1 = Bi-directional engine is configured as an Output Engine
18	RO	0	**Traffic Priority (TP):** If set to a 1, the stream will be treated as preferred traffic if the underlying bus supports it. If set to a 0, the traffic will be handled on a 'best effort' basis. The actual meaning of this bit is specific to the hardware implementation. Depending on the hardware implementation, there may be additional restrictions on the traffic, and software should assume that the buffers associated with the stream will not be snooped or cached. On PCI Express, for example, setting the TP bit to a 1 might cause the controller to generate non-snooped isochronous traffic, while a PCI implementation may ignore this bit.
17:16	RO	0's	**Stripe Control (STRIPE):** (Output and Bi-directional engines configured for output only. Read Only zero for input streams.) If the NSDO field of the Global Capabilities register indicates that the controller supports multiple SDO lines and the CODEC has been determined to have compatible capabilities, STRIPE can be used to indicate how many of the SDO lines the stream should be striped across. 00: 1 SDO 01: 2 SDO 10~11: Reserved
15:5	RsvdP	0's	**Reserved**
4	R/W	0	**Descriptor Error Interrupt Enable (DEIE):** Controls whether an interrupt is generated when the Descriptor Error Status (DESE) bit is set.
3	R/W	0	**FIFO Error Interrupt Enable (FEIE):** This bit controls whether the occurrence of a FIFO error (over-run for input or under-run for output) will cause an interrupt or not. If this bit is not set, bit 4 in the Status register will be set, but the interrupt will not occur. Either way, the samples will be dropped.
2	R/W	0	**Interrupt On Completion Enable (IOCE):** This bit controls whether or not an interrupt occurs when a buffer completes with the IOC bit set in the descriptor. If this bit is not set, bit 3 in the Status register will be set, but the interrupt will not occur.
1	R/W	0	**Stream RUN (RUN):** When set to 1 the DMA engine associated with this input stream will be enabled to transfer data in the FIFO to main memory. When cleared to 0 the DMA engine associated with this input stream will be disabled. If the corresponding SSYNC bit is 0, input stream data will be taken from the link and moved to the FIFO and an over-run may occur.
0	R/W	0	**Stream Reset (SRST):** Writing a 1 cause the corresponding stream to be reset. The Stream Descriptor registers (except the SRST bit itself), FIFO(s)', and cadence generator for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that

			the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to begin operation, it will report a 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The RUN bit must be cleared before SRST is asserted.

Table 37: Stream Descriptor n Control

Offset 83h: {IOB}SDnSTS – Input/Output/Bi-directional Stream Descriptor n Status

Default Value: 00h

Length: 1 byte

Bit	Type	Reset	Description
7:6	RsvdZ	0	**Reserved**
5	RO	0	**FIFO Ready (FIFORDY):** The controller hardware will set this bit to a 1 while the output DMA FIFO contains enough data to maintain the stream on then link. This bit defaults to 0 on reset because the FIFO is cleared on a reset. For input, this bit indicates that a descriptor has been fetched, and the engine is ready for the RUN bit to be set. This bit is not meaningful for input streams and is therefore always zero for input streams.
4	R/W1C	0	**Descriptor Error (DESE):** During the fetch of a descriptor, something bad happened. This could be a result of a Master Abort, a Parity or ECC error on the bus, or any other error which renders the current Buffer Descriptor or Buffer Descriptor List useless. This error is treated as a fatal stream error, as the stream cannot continue running. The RUN bit will be cleared and the stream will stop. Software may attempt to restart the stream engine after addressing the cause of the error and writing a '1' to this bit to clear it.
3	R/W1C	0	**FIFO Error (FIFOE):** Set when a FIFO error occurs. Bit is cleared by writing a '1' to this bit position. This bit is set even if an interrupt is not enabled. For an input stream, this indicates a FIFO overrun occurring while the RUN bit is set. When this happens, the FIFO pointers don't increment and the incoming data is not written into the FIFO, thereby being lost. For an output stream, this indicates a FIFO under run when there are still buffers to send. The hardware should not transmit anything on the link for the associated stream if there

			is not valid data to send.
2	R/W1C	0	**Buffer Completion Interrupt Status (BCIS):** This bit is set to '1' by the hardware after the last sample of a buffer has been processed, AND if the interrupt on Completion (IOC) bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a '1' to this bit position.
1:0	RsvdZ	0	**Reserved**

Table 38: Stream Descriptor n Status

Offset 84h: {IOB}SDnLPIB – Input/Output/Bi-directional Stream Descriptor n Link Position in Buffer

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	RO	0's	**Link Position in Buffer (LPIB):** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the Cyclic Buffer Length register, and then wrap to zero.

Table 39: Stream Descriptor n Link Position in Buffer

Offset 88h: {IOB}SDnCBL – Input/Output/Bi-directional Stream Descriptor n Cyclic Buffer Length

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	R/W	0's	**Cyclic Buffer Length (CBL):** Indicates the number of bytes in the complete cyclic buffer. Link Position in Buffer (LPIB) will be reset when it reaches this value. Software may only write to this register after Global Reset, Controller Reset, or Stream Reset has occurred. Once the 'RUN' bit has been set to enable the engine, software must not write to this register until after the next reset is asserted, or undefined things will happen. CBL must represent an integer number of samples. This value should not be modified except when the RUN bit is '0'.

Table 40: Stream Descriptor n Cyclic Buffer Length

Offset 8Ch: {IOB}SDnLVI – Input/Output/Bi-directional Stream Descriptor n

Last Valid Index

Default Value: 0000h

Length: 2 bytes

Bit	Type	Reset	Description
15:8	RsvdP	0's	**Reserved**
7:0	R/W	00h	**Last Valid Index (LVI):** The value written to this register indicates the index for the last valid Buffer Descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list on continue processing. LVI must be at least 1; i.e., there must be at least two valid entries in the buffer descriptor list before DMA operations can begin. This value should not be modified except when the RUN bit is '0'.

Table 41: Stream Descriptor n Last Valid Index

Offset 90h: {IOB}SDnFIFOS – Input/Output/Bi-directional Stream Descriptor n FIFO Size

Default Value: 003Fh

Length: 2 bytes

Bit	Type	Reset	Description
15:0	RO	3Fh	**FIFO Size (FIFOS):** Indicates the maximum number of bytes that could be fetched by the controller at one time,or. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. This number maybe static to indicate a static buffer size, or may change after the data format has been programmed if the controller is able to vary its FIFO size based on the stream format.

Table 42: Stream Descriptor n FIFO Size

Offset 92h: {IOB}SDnFMT – Input/Output/Bi-directional Stream Descriptor n Format

Default Value: 0010h

Length: 2 bytes

Bit	Type	Reset	Description
15	RO	0	**Reserved**
14	R/W	0	**Sample Base Rate (BASE):** 0 = 48kHz

			1 = 44.1kHz
13:11	R/W	0's	**Sample Base Rate Multiple (MUTL):** 000 = 48kHz / 44.1kHz or less 001 = X2 (96kHz, 88.2kHz, 32kHz) 010 = X3 (144kHz) 011 = X4 (192kHz, 176.4kHz) 100~111 = Reserved
10:8	R/W	0's	**Sample Base Rate Divisor (DIV):** 000 = Divide by 1 (48kHz, 44.1kHz) 001 = Divide by 2 (24kHz, 22.05kHz) 010 = Divide by 3 (16kHz, 32kHz) 011 = Divide by 4 (11.025kHz) 100 = Divide by 5 (9.6kHz) 101 = Divide by 6 (8kHz) 110 = Divide by 7 111 = Divide by 8 (6kHz)
7	RsvdP	0	**Reserved**
6:4	R/W	001s	**Bits per sample (BITS):** 000 = Reserved 001 = 16 bits. The data will be packed in memory in 16 bit containers on 16 bit boundary 010 = 20 bits. The data will be packed in memory in 32 bit containers on 32 bit boundary 011 = 24 bits. The data will be packed in memory in 32 bit containers on 32 bit boundary 100 = 32 bits. The data will be packed in memory in 32 bit containers on 32 bit boundary 101~111 = Reserved
3:0	R/W	0's	**Number of Channel (CHAN):** Number of channels in each frame of the stream. 0000 = 1 0001 = 2 … 1111 = 16

Table 43: Stream Descriptor n Format

Offset 98h: {IOB}SDnBDPL – Input/Output/Bi-directional Stream Descriptor n BDL Pointer Lower Base Address

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:7	R/W	0's	**Buffer Descriptor List Lower Base Address (BDLLBASE):** Lower address of the Buffer Descriptor List. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. This value should not be modified except when the RUN bit is '0'.

6:0	RO	0's	Hardwire to 0 to force 128 bytes alignment for the BDL.

Table 44: Stream Descriptor n Lower Base Address

Offset 9Ch: {IOB}SDnBDPU – Input/Output/Bi-directional Stream Descriptor n BDL Pointer Upper Base Address

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	RO	0's	**Buffer Descriptor List Upper Base Address (BDLUBASE):** Upper 32 bit address of the Buffer Descriptor List. This register field must not be written when the DMA engine is running or the DMA transfer may be corrupted. This value should not be modified except when the RUN bit is '0'.

Table 45: Stream Descriptor n Upper Base Address

Offset 2030h: WALCLKA – Wall Clock Counter Alias

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description
31:0	RO	0's	**Wall Clock Counter Alias (Counter):** An alias of the Wall Clock Counter register at offset 30h. This is an alias of the counter register, and behaves exactly the same as if the Wall Clock Counter register were being read directly.

Table 46: Wall Clock Counter

The Alias registers are used in some programming models to allow the position registers to be mapped directly to user mode. Since the Wall Clock Alias and the following Link Position Alias registers are at an offset 2000h above the corresponding register in the normal High Definition Audio register range, the positions on the logical page starting at 2000h can be mapped to user mode without exposing all the DMA, control, status, and interrupt registers to be visible in user mode.

Offset 2084h, 20A4h,…: {IOB}SDnLICBA – Input/Output/Bidirectional Stream Descriptor n Link Position in Buffer Alias

Default Value: 00000000h

Length: 4 bytes

Bit	Type	Reset	Description

31:0	RO	0's	**Link Position in Buffer n Alias (LPIBA):** An alias of the "Link Position in Buffer register" for each Stream Descriptor. This is an alias of the counter register, and behaves exactly the same as if the Link Position register were being read directly. Note that all of the Link Position In Buffer registers for all of the supported input, output, and bi-directional stream engines are also alias at an offset 2000h higher, so Stream 1 Link Position in Buffer is alias at 2084h, Stream 2 LPIB is alias at 20A4h, etc.

Table 47: Link Position in Buffer *n* Alias

8.3. HDA Implement Notes

8.3.1. HDA Controller Turn on (System BIOS phase)

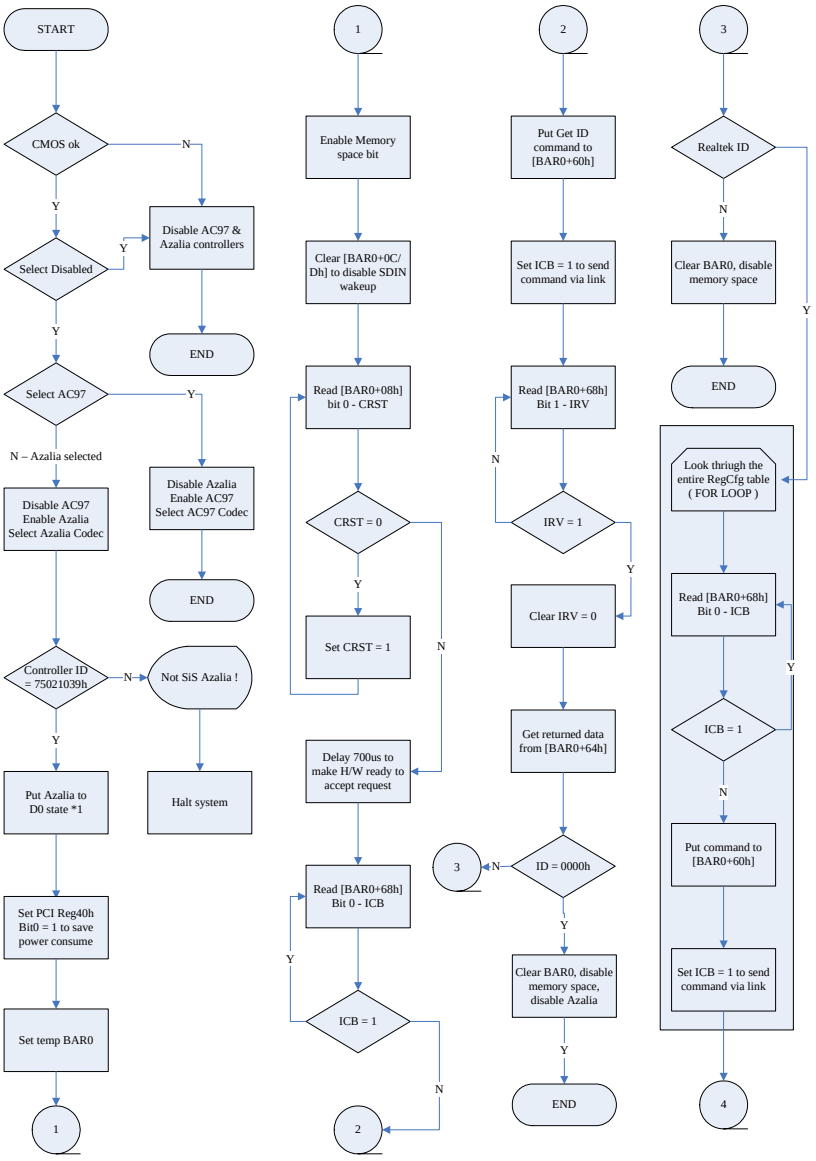
- Enable HDA Controller Sequence:
  - Enable HDA Controller Sequence:
  - Set LPC R7Eh[3]=1
- HDA device routing A→C, IOAPIC→18

8.3.2. HDA Controller/CODEC Hardware Check Sequence

- Check the controller is ready or not ? (SiS ID = 1039h HDA ID = 7502h)
- Check the internal revision ID of HDA controller ?
  - HDA configuration register + offset F0h = 1'h => 966 HDA
  - HDA configuration register + offset F0h = 2'h => 968 HDA
- Check the HDA docking suppot register, if the internal revision ID of HDA controller is F0h = 2'h
  - If the platform support HDA codec docking, set HDA PCI configuration register + offset 4Dh = 80'h
  - If the platform does not support HDA codec docking, set HDA PCI configuration register + offset 4Dh = 00'h
- Check HDA "power state" at PCI configuration registers offset 54h bit[1:0]
  - If the "power state" registers was set to D3-state (54h bit[1:0] = 11) while power off by driver, BIOS needs to set the "power state" registers to D0-state (54h bit[1:0] = 00) before doing pin configurations. Since all the operating registers are not allowed to access while controller is in D3 state specified by the HDA specification.

- Read HDA device AZBAR registers. (PCI offset 10h-13h)
- De-assert the Controller Reset (set AZBAR+08h[0]=1)
- Check both of the 2 items to know the controller is ready or not.
  - If the wall clock is running at AZBAR+30h[31:0]
  - If the Controller Reset bit(AZBAR+08h[0]) is '1'
- Wait for CODEC connection and initialization
  - For about 700us (20.83us*25 frames + 100us) specified by HDA specification.
- Issue a "get ID" command to CODEC
  - Set AZBAR+60h[31:0] = 000F0000h
  - Set AZBAR+68h[0] = 1
  - Polling the AZBAR+68h[1] = 1. If this bit is '1', means the CODEC response is ready.
  - Check the SDI number of the CODEC response at (AZBAR+68h[7:4]). If the CODEC is connected to SDI0, the 4 bits are "0000".
  - Check the CODEC response at AZBAR+64h[31:0]. If the CODEC is Realtek ALC880, the ID is 10EC0880. (If the CODEC is Realtek ALC882, the ID is 10EC0882.) Each type of CODEC has a unique CODEC ID specified by the CODEC venders. Please check it with the CODEC vendors.
  - Write Clear the return status (write AZBAR+68h[1] = 1) after you complete the check of the ID or issue any command by using the immediate-command register (at operating register offset 60h~6Fh).
- If of all the steps above are correct, it means that both of the board layout and the HW are correct and they are ready to use. You can start entering Windows and installing the driver.

8.3.3. HDA CODEC initial and pinwidget configuration flow chart



- This procedure is executed before scanning PCI devices
- The operation registers of Azalia can be accessed only when device is in D0 state

8.3.4. BIOS initial HDA CODEC sequence

Before using Microsoft default HDA driver, BIOS needs to program CODEC pin configuration first. (If you use the CODEC vendor's driver, you don't have to do these configurations in BIOS phase.) SiS demo board provides REALTEK 880 CODEC (or REALTEK 882 CODEC) for verification.

SiS demo board BIOS check the CODEC ID in the procedure of "**4.2 HDA Controller/CODEC Hardware Check Sequence**". If the CODEC IDs are not expected (REALTEK 880/882 CODEC), SiS demo board BIOS disables the HDA digital controller. It's used to high light the following "Verb Command Table" is not suitable for your current system. Now, you have to contact with your CODEC vendor to ask for their "verb command table" and replace the following one. Then, you can have the correct pin configuration setting, and the Microsoft default driver can work well on your system after entering Windows XP or Vista..

- Verb Command Table for REALTEK CODEC

```
;    NID 0x14 : 0x01014010
;    NID 0x15 : 0x01016012
;    NID 0x16 : 0x01011011
;    NID 0x17 : 0x01012014
;    NID 0x18 : 0x01A19830
;    NID 0x19 : 0x02A19C40
;    NID 0x1A : 0x01813031
;    NID 0x1B : 0x02014C20
;    NID 0x1C : 0x99331132
;    NID 0x1D : 0x411111F0
;    NID 0x1E : 0x0144711E
;    NID 0x1F : 0x01C45150
```

8.3.5. Pin Widget Configuration Sample Code

```
ProgramAzaliaRealTekCodec     proc  near
        push ds
        push es
        push di
        push esi
;-------------------------------------------------------------------------------------------------;
        xor   ax, ax
        mov   ds, ax
        mov   es, ax
        mov   eax, 80007810h
        mov   dx, 0CF8h
        out   dx, eax
        jmp   short $+2
        jmp   short $+2
        mov   dx, 0CFCh
        in    eax, dx
        jmp   short $+2
        jmp   short $+2
        mov   esi, eax              ;Save AZBAR address to esi
;-------------------------------------------------------------------------------------------------;
ChceckCODECReadyForPG:
        mov   al, byte ptr es:[esi+08h]
        test  al, 01h
        jnz   short CODECReadyForPG
        or    al, 01h
        mov   byte ptr es:[esi+08h], al
        jmp   short ChceckCODECReadyForPG
CODECReadyForPG:
;-------------------------------------------------------------------------------------------------;
WaitCODECAvailableToWrite:
        mov   al, byte ptr es:[esi+68h]
        test  al, 01h
```

```
        jz      short CODECAvailableToWrite
        or      al, 02h
        mov  byte ptr es:[esi+68h], al
        jmp   short WaitCODECAvailableToWrite
CODECAvailableToWrite:
;-------------------------------------------------------------------------------------------;
;Read CODEC Vendor ID(Verb ID=0F00h)
        mov  eax, 000F0000h             ;Get vender ID Verb command
        mov  dword ptr es:[esi+60h], eax
;-------------------------------------------------------------------------------------------;
;delay
        mov  cx, 10
@@:
        out    80h, al
        loop  short @b
;-------------------------------------------------------------------------------------------;
;start immediate command
        mov  al, 00h
        mov  byte ptr es:[esi+68h], al
        mov  al, 01h
        mov  byte ptr es:[esi+68h], al
;-------------------------------------------------------------------------------------------;
        mov  cx, 100
WaitReadVendorCommandCompleted:
        mov  al, byte ptr es:[esi+68h]
        test   al, 02h
        jnz    ReadVendorIDCommandCompleted   ;Successful
        loop  WaitReadVendorCommandCompleted
        jmp   ChceckCODECReadyForPG            ;Fail
ReadVendorIDCommandCompleted:
;-------------------------------------------------------------------------------------------;
;Read Vendor ID command complete then clear status
```

```
        mov  al, 02h
        mov  byte ptr es:[esi+68h], al
;-------------------------------------------------------------------------------------------;
;Check Vendor ID
        mov  eax, dword ptr es:[esi+64h]
        cmp  eax, 10EC0880h             ;REALTEK 880 CODEC ID
        jnz    short EndOfSetHDACODEC
;-------------------------------------------------------------------------------------------;
        mov  di, offset cs:REALTEK_10_Codec_table
LoopForCodec:
        mov  eax, dword ptr cs:[di]
        mov  dword ptr es:[esi+60h], eax
;-------------------------------------------------------------------------------------------;
        mov  cx, 10
@@:
        out    80h, al
        loop  short @b
;-------------------------------------------------------------------------------------------;
;start immediate command
        mov  al, 00h
        mov  byte ptr es:[esi+68h], al
        mov  al, 01h
        mov  byte ptr es:[esi+68h], al
;-------------------------------------------------------------------------------------------;
        mov  cx, 100
WaitStartCommandCompleted:
        mov  al, byte ptr es:[esi+68h]
        test   al, 02h
        jnz    StartCommandCompleted
        loop  WaitStartCommandCompleted
        jmp   ChceckCODECReadyForPG             ;Fail
StartCommandCompleted:
```

```
;-------------------------------------------------------------------------------------------------;
;command complete then clear status
        mov  al, 02h
        mov  byte ptr es:[esi+68h], al
;-------------------------------------------------------------------------------------------------;
        add  di, 4
        mov  eax, dword ptr cs:[di]
        cmp  eax, 00h
        jz      short EndOfSetHDACODEC
        jmp  short LoopForCodec
EndOfSetHDACODEC:
;-------------------------------------------------------------------------------------------------;
        pop  esi
        pop  di
        pop  es
        pop  ds
DoNotNeedProgramREALTEKCODEC:
        ret
ProgramAzaliaRealTekCodec    endp

;-------------------------------------------------------------------------------------------------;
REALTEK_10_Codec_table      label dword
        dd    01471C10h          ;NID 14h
        dd    01471D40h
        dd    01471E01h
        dd    01471F01h
        dd    01571C12h          ;NID 15h
        dd    01571D60h
        dd    01571E01h
        dd    01571F01h
        dd    01671C11h          ;NID 16h
        dd    01671D10h
```

```
dd    01671E01h
dd    01671F01h
dd    01771C14h        ;NID 17h
dd    01771D20h
dd    01771E01h
dd    01771F01h
dd    01871C30h        ;NID 18h
dd    01871D98h
dd    01871EA1h
dd    01871F01h
dd    01971C40h        ;NID 19h
dd    01971D9Ch
dd    01971EA1h
dd    01971F02h
dd    01A71C31h        ;NID 1Ah
dd    01A71D30h
dd    01A71E81h
dd    01A71F01h
dd    01B71C20h        ;NID 1Bh
dd    01B71D4Ch
dd    01B71E01h
dd    01B71F02h
dd    01C71C32h        ;NID 1Ch
dd    01C71D11h
dd    01C71E33h
dd    01C71F99h
dd    01D71CF0h        ;NID 1Dh
dd    01D71D11h
dd    01D71E11h
dd    01D71F41h
dd    01E71C1Eh        ;NID 1Eh
dd    01E71D71h
```

```
dd    01E71E44h
dd    01E71F01h
dd    01F71C50h          ;NID 1Fh
dd    01F71D51h
dd    01F71EC4h
dd    01F71F01h
dd    00h
```

8.3.6. HDA CODEC Detection

Before scan PCI device during POST, BIOS must determine CODEC present on the platform or not. If the HDA CODEC is not on the platform, BIOS need to disable HDA controller first.

- Detect HDA CODEC sequence
  - Set to HDA mode(Set SB R7Ch [1:0]=11b,and SB R7Eh[3]=1)
  - Enable memory space and give HDA BAR address (offset 10-13h)
  - Check HDA internal revision ID (HDA CFG F0h = 1'h => 966 HDA, F0h = 2'h => 968 HDA
  - Check HDA docking support
  - De-assert HDA controller reset. (set BAR+08h [0]=1)
  - Set "read CODEC vendor ID verb command". (Verb ID = 0F000h,write 0F000h to BAR+60h)
  - Start immediate command (set BAR+68h [0]=1)
  - Check read command successful (expect BAR+68h [1]=1,if status not ready means read command fail.)
  - Check vendor ID exist or not. (The data read from BAR+64h is not equal "0").
  - If HDA CODEC doesn't exist, clear memory enable bit and BAR address.

8.3.7. HDA CODEC Detection Sample Code.

```
;Set to Azalia Mode
    mov  eax, 8001007Ch
    mov  dx, 0CF8h
    out  dx, eax
    mov  dx, 0CFCh
    in   al, dx
    or   al, 03h
    out  dx, eax
;Enable Azalia Controller
    mov  eax, 8001007Ch
    mov  dx, 0CF8h
    out  dx, eax
    mov  dx, 0CFCh
    in   eax, dx
    and  eax, 080000h
    out  dx, eax
;Check Azlia Codec Exist?(Give HDA memory base)
    mov  eax, 80007804h
    mov  dx, 0CF8h
    out  dx, eax
    jmp  short $+2
    jmp  short $+2
    mov  dx, 0CFCh
    mov  al, 03h
    out  dx, al
    jmp  short $+2
    jmp  short $+2

    mov  eax, 80007810h
    mov  dx, 0CF8h
    out  dx, eax
    jmp  short $+2
```

```
    jmp   short $+2
    mov  dx, 0CFCh
    mov  eax, 0FEAF4000h
    mov  esi, eax            ;save AZBAR to esi
    out   dx, eax
    jmp   short $+2
    jmp   short $+2
;-------------------------------------------------------------------------------------------------------;
 ChceckAZCODECReadyForPG:
    mov  al, byte ptr es:[esi+08h]
    test   al, 01h
    jnz    short AZCODECReadyToPG
    or     al, 01h                ;De-assert the controller reset
    mov  byte ptr es:[esi+08h], al
    jmp   short ChceckAZCODECReadyForPG
AZCODECReadyToPG:
;-------------------------------------------------------------------------------------------------------;
;Read CODEC Vendor ID(Verb ID=0F00h)
    mov  eax, 000F0000h            ;Get vender ID Verb command
    mov  dword ptr es:[esi+60h], eax
;-------------------------------------------------------------------------------------------------------;
;delay
    mov  cx, 10
@@:
    out   80h, al
    loop  short @b
;-------------------------------------------------------------------------------------------------------;
;start immediate command
    mov  al, 00h
    mov  byte ptr es:[esi+68h], al
    mov  al, 01h
    mov  byte ptr es:[esi+68h], al
```

```
;-------------------------------------------------------------------------------------------------------;
   mov  cx, 200
WaitReadAZCODECID:
   mov  al, byte ptr es:[esi+68h]
   test  al, 02h
   jnz   ReadAZCODECIDOK            ;Successful
   loop  WaitReadAZCODECID
   jmp   AZCODECIDFail              ;Fail
ReadAZCODECIDOK:
;-------------------------------------------------------------------------------------------------------;
;Read Vendor ID command complete then clear status
   mov  al, 02h
   mov  byte ptr es:[esi+68h], al
;-------------------------------------------------------------------------------------------------------;
;Check Vendor ID
   mov  eax, dword ptr es:[esi+64h]
   mov  AZCODECID, eax
   cmp  eax, 00h
   jnz   short AZCODECOnBoard
AZCODECIDFail:
;clear AZBAR address
   mov  eax, 80007810h
   mov  dx, 0CF8h
   out   dx, eax
   jmp   short $+2
   jmp   short $+2
   mov  dx, 0CFCh
   mov  eax, 00h
   out   dx, eax
   jmp   short $+2
   jmp   short $+2
;clear memroy enable bit
```

```
    mov  eax, 80007804h
    mov  dx, 0CF8h
    out  dx, eax
    jmp  short $+2
    jmp  short $+2
    mov  dx, 0CFCh
    mov  al, 00h
    out  dx, al
    jmp  short $+2
    jmp  short $+2
;disable Azalia device
    mov  eax, 8001007Ch
    mov  dx, 0CF8h
    out  dx, eax
    mov  dx, 0CFCh
    in   al, dx
    and  al, not 03h
    out  dx, eax
AZCODECOnBoard:
```

9. SMBus

9.1. SMBUS Programming

9.1.1. Overview

In modern PC environment, there are two main devices, clock generator and SPD, connected to SMBus. BIOS could get some information from these two devices to initiate whole system setting in POST time. In this document, we introduce some examples to realize how to initialize these devices or else resided in SMBus.

9.1.2. Initiate SMBus Controller

In SiS968 south bridge, SMBus Base_Address = by BIOS Engineer The enable bits of SMBus are in SB register 9Ah. First of all, we have to enable SMBus, follows below two steps:

- Enable SMBus
- Enable SMBus Host Controller

Example: As described above, there are two steps for this initiation sequence as following:

Step 1 Set	SB9A [0] = 1	; Enable SMBus host Controller
Step 2 Set	SB9B [0:7]	; Set SMBus base address

After this initiation procedure, the SMBus controller is ready to accept our commands and delivery them into SMBus.

9.1.3. Read SPD

SPD is abbreviation from **Serial Presence Detect**. It defined some important information about DRAM. BIOS can read SPD to get DRAM type, optimal timing and size, etc. It simplified deeply BIOS's efforts in DRAM sizing procedure.

SPD supports read/write and send/receive *byte* protocol. We'll illustrate the read byte protocol as following:

S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	P

Fig. 1 Read Byte Protocol command sequence

Fig.1 illustrates command/data sequence of read byte protocol in SMBus. Shadow areas indicate the data is delivered by slave device (Ex. SPD). So we have to tell host controller the slave address and command code.

Example: To read data from bank 0(address = 1010000Xb)*[1] by SMBus. Suppose SMBus I/O base address is C000h.

Step 1 Clear status register C000h(Write 0FFh into I/O C000h)

Step 2 If C002h[1:0] ≠ 00, Fill 20h into I/O C0003h. Otherwise go to step 3.

Step 3 Fill slave address into I/O C004h. (Value = a1h) *[1]

Step 4 Fill intended byte index into I/O C005h. (Value = 00h) *[2]

Step 5 Fill transfer type and assert start bit on C003h. (Value = 12h)

Step 6 Waiting for 30us

Step 7 Check SMBus status register C000h. When transfer finished, bit 3(SMBMAS_STS) set indicated the transfer completed normally. If bit 1 set go to Step 1

Step 8 Read back one data byte from C010h.

Step 9Clear status register C000h.

Note:

1. The LSB in address byte indicates access type. Value 0 represents *WRITE*, and value 1 represents *READ*.
2. This register in *Read Byte Protocol* designates the offset of byte in slave device. For example, if you want to read memory type in SPD, just fill 2 into this register. And you will get the byte 2 of SPD.

9.1.4. Clock Generator Programming

In post time, BIOS gets CPU/DRAM frequency from clock generator and set optimal setting to system. Furthermore, in many systems supported jumpless feature, BIOS has to write some registers of clock generator to change system frequency and ensures systems work fine in new frequency. All clock generators support *Block Read/Write Protocol*. We discuss these two protocols as following:

Block Read Protocol

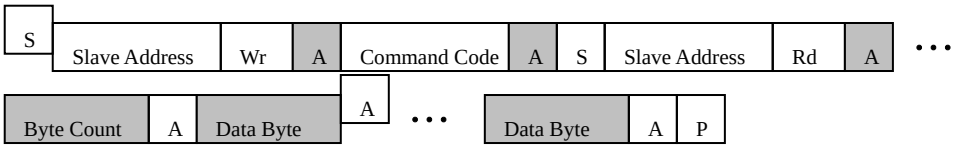


Fig. 2 Block Read command sequence

Fig.2 illustrates command/data sequence of block read protocol in SMBus. Shadow areas indicate the data is delivered by slave device (Clock generator). We shall tell the host controller slave address and command code. Note that the number of received data (Byte Count) is determined by slave device.

Example: Read data from clock generator. In this example, we suppose the byte count is less than eight and I/O base address is 80D0h. The case more than 8 bytes will be explained in below section.

Step 1 Clear status register C000h(Write 0FFh into I/O C000h)

Step 2 If C002h[1:0] ≠ 00, Fill 20h into I/O C003h. Otherwise go to step 3.

Step 3 Fill slave address into I/O C004h. (Value = D3h)

Step 4 Fill intended byte index into I/O C005h. (Value = 00h)

Step 5 Fill transfer type and assert start bit on 03h. (Value = 15h)

Step 6 Check SMBus status register C000h. When transfer finished, bit 3(SMBMAS_STS) set indicated the transfer completed normally, if bit 2 set go to Step 1

Step 7 Read bytes from C010~C02Fh. Dependent on the byte count determined by clock generator.

Step 8 Clear status register C000h.

Block Write Protocol

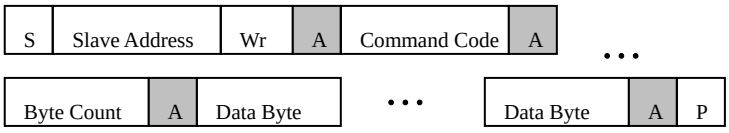


Fig. 3 Block Write command sequence

Fig.3 illustrates command/data sequence of block write protocol in SMBus. Shadow areas also indicate the data is delivered by slave device. Similar to previous section, we shall tell the host controller the slave address, command code and byte count. Block write protocol permits master device to deliver a continuous bytes to slave. Command code indicates the offset of the first byte and byte count indicates the length of continuous data sequence.

Example: To write byte 1~3 of clock generator (value = 01h, 02h and 03h). Suppose the byte count is below eight and I/O base address is C000h. The case has more than 8 bytes will be postponed to subsequent section.

Step 1 Clear status register C000h(Write 0FFh into I/O C000h)

Step 2 If C002h[1:0] ≠ 00, Fill 20h into I/O C003h. Otherwise go to step 3.

Step 3 Fill slave address into I/O C004h. (value = D2h)

Step 4 Fill offset of start byte into I/O C005h. (value = 00h)

Step 5 Fill byte count into I/O C007h. (value = 3h)

Step 6 Fill transfer type and assert start bit on 03h. (Value = 15h)

Step 7 Waiting for 30us.

Step 8 Check SMBus status register C000h. When transfer finished, bit 3(SMBMAS_STS) set indicated the transfer completed normally, if bit 1 set go to Step1

Step 10 Clear status register C000h.

9.2. Example

1. How to enable SMBUS HC ?

=> set LPC Reg9Bh bit[7:0] for SMBUS base and then set LPC Reg9Ah bit[1:0] = 11b to enable HC

Note : 9Bh bit[7:0] is for IO base bit[15:8] only

2. How to activate the SMBUS transactions ?

=> 1 example is taken to demonstrate the flow to initiate the SMBUS transactions – “Read Byte” :

a. kill bus – stop all activities of master and slave and set to initial state

```
mov dx, SMBUS_BASE + 03h
mov al, 20h          // bit5 = 1 to kill bus
out dx, al
```

b. clear status register

```
mov dx, SMBUS_BASE
in al, dx
out dx, al
```

c. setup slave address

```
mov dx, SMBUS_BASE + 04h
mov al, ( SLAVE_ADDRESS OR 01h )    // 01h is for “Read Slave”
```

```
out dx, al
```

d. setup command byte (offset in indexed mode access)

```
mov dx, SMBUS_BASE + 05h
mov al, OFFSET
out dx, al
```

e. setup protocol and start bus transfer !!!

```
mov dx, SMBUS_BASE + 03h
mov al, 12h
out dx, al
```

f. Check phase – check master complete and interrupt status

```
mov dx, SMBUS_BASE
LoopChkSts:
in al, dx
and al, 00001010b// bit3 = 1 indicates HC completed the process OK, bit1 = 1
means NG
cmp al, 08h
je jmp to next step // ← transaction successful
cmp al, 02h
je jmp to label of “Error report”        // ← transaction fails
jmp LoopChkSts
LoopChkSts
```

g. Read data back

```
mov dx, SMBUS_BASE + 10h              // 10h is the starting address for data
registers
in al, dx
```

h. Remaining tasks – clear status

```
mov dx, SMBUS_BASE
in al, dx
out dx, al
```

10 EEPROM Programming Guide

EEPROM DATA MAPPING

FM93C46 is a 1024-bit Serial CMOS EEPROM.

The Data mapping in EEPROM is:

1. **MAC :** 00h~0Bh (unit is word)

   00h~01h : Identification (0191h for 968)

   02h : TX clock(bit 0~1), RX clock(bit 2~3)

   03h : PHY address(bit 0~4), Speed(bit 5~6), RMII(bit 7)

   04h : Link change(bit 0), Magic(bit 1)

   06h~0Bh : MAC address.

MAC	00~01	01	**90/91**
	02~04		
	05~0B	MAC address	
reserved	10~7F		

APC REGISTERS SETTING

APC REGISTERS

The following table is the APC register .and its meanings

APC Registers	Default	Description
Reg. 07 Bit 3	0	0: Disable APC load 1: MAC address load from APC
Reg. 09~0Eh	0	MAC address
Reg. 0F Bit 6	0	Input buffer selection mode 0: Single end mode 1: Differential mode (GMII or RGMII)
Reg. 0F Bit 5	0	Magic packet Detector 0: Disable 1: Enable
Reg. 0F Bit 4	0	Link status polling 0: Disable 1: Enable
Reg. 0F Bit 3~2	01	RX clock 00: MII TX clock 01: MII RX clock 10: External clock 11: Internal clock

Reg. 0F Bit 1~0	00	TX clock 00: MII TX clock 01: MII RX clock 10: External clock 11: Internal clock
Reg. 12 bit 7	0	MII/RGMII selection 0: MII 1: RGMII
Reg. 12 bit 6~5	00	OP speed 00: Undetermined 01: 10M 10: 100M 11: 1000M
Reg. 12 bit 4~0	00	SMII PHY address

MAC address SETTING

IO index access

Software would use 2 way to access the APC register

1. Software would set SB reg. 48h bit 6 to 1 to enable the APC bank. Use index/data port with 70h/71h to read/write data. After access, reset the SB reg. 48h bit 6 to 0 to disable the APC bank.

2. Software would set SB reg. 48h bit 1 to 0 to enable the new re-index. Use index/data port with 78h/79h to read/write data.

EEPROM software access

G-MAC uses EEPROM to store some information about the NIC. Software should read the MAC address from EEPROM in order to fill the **RxMacUnicastAddr** register (offset 62h). There are two ways to access EEPROM via **EEPROMInterface** register (offset 3Ch):

- Serial mode
- Parallel mode

Serial Mode

There are four bits used to serially access the EEPROM in the **EEPROMInterface** register. They are **CS** (Chip Select), **SK** (Serial Clock), **DI** (Data In), and **DO** (Data Out), which directly control the interface pins between SiS190/191 and EEPROM. In the beginning of any command cycle, software driver should assert the **CS** pin and hold it during the command cycle. And then assert and deassert the **SK** pin alternately to

generate the clock input. Software may input one bit of data with **DI** pin or get one bit of output data with **DO** pin in every clock interval. The input data contains the op-code, address, and the data you want to write to EEPROM. Software should deassert the **CS** pin to finish the command cycle. The following is the instruction table.

Instruction	SB	Op. Code	Address	Data	Comments
READ	1	10	A5-A0		Read data stored in memory, at specified address.
WEN	1	00	11xxxx		Write enable must precede all programming modes.
ERASE	1	11	A5-A0		Erase selected register.
WRITE	1	01	A5-A0	D15-D0	Write selected register.
ERAL	1	00	10xxxx		Erases all registers.
WRALL	1	00	01xxxx	D15-D0	Write all registers.
WDS	1	00	00xxxx		Disable all programming instructions

Table 10.1 Instruction Table

For example, if software wants to read a word of data from EEPROM, it should follow the operations in figure 2.1. First assert the **CS** pin and generate the serial clock in the **SK** pin. Set the **DI** pin high to start an operation and set 10b to the next two bits that represents the READ op-code. And the following six bits (A5~A0) is the address where driver wants to read. **DO** pin will be deasserted in the next clock time (a dummy bit) when finishing the above sequence, and then the following 16 bits will be the output data shown on the **DO** pin. After the read command cycle is finished, driver should deassert the **CS** pin to complete this cycle.

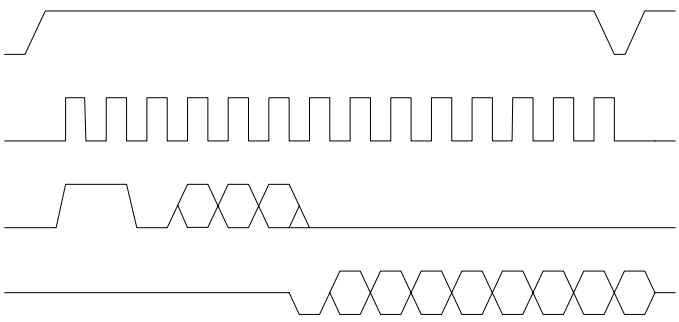


Fig 10.1 Read Operation from EEPROM

Software should perform the WEN command to enable write before it write a data to EEPROM. The WEN operation is as following:

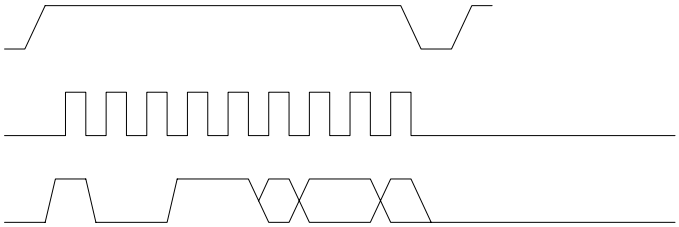


Fig 10.2 Write Enable Operation

Then software can start writing the data to EEPROM after WEN cycle completed. The EEPROM will become busy and **DO** pulse will down to low for a while when data is written to it. It is software driver's responsibility that polling the state of **DO** pin whether raised high. The WRITE operation will be completed when **DO** pin raise high. The write operation is as following:

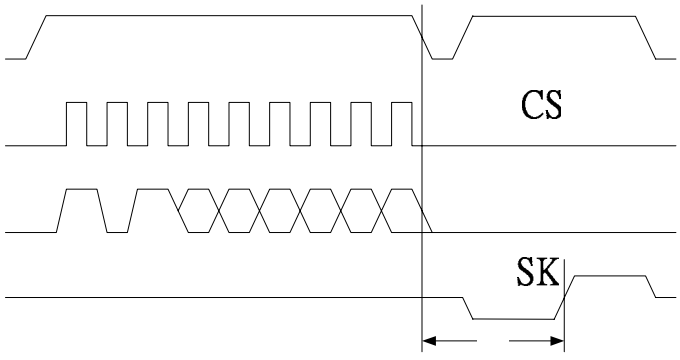


Fig 10.3 Write Operation to EEPROM

DI 1 0 0 1 1

Software should disable write after all the write operation is finished. The WDS operation is as following:

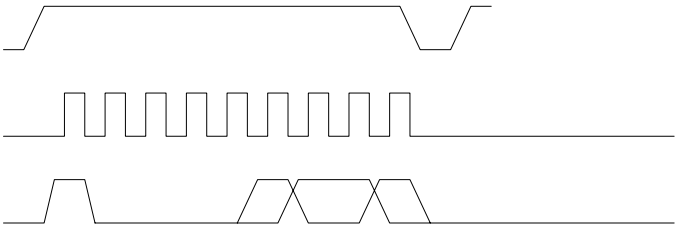


Fig 10.4 Write Disable Operation

Parallel Mode

Software can access the EEPROM with 25 bits of **EEPROMInterface** register (bit 7 ~ bit 31) in parallel mode. **EEPROMReq** bit (bit 7) should be set to start an EEPROM operation. Fill the specific op-code into the **EEPROMOperation** field and the address which driver want to access into the **EEPROMAddr** field. The data should be put into the **EEPROMData** field if it is a write operation. Then SiS190 will process the command specified by driver. The operation will be completed if the **EEPROMReq** bit was cleared by SiS190. Driver can read the 16 bits data from **EEPROMData** field if it is a read operation.

It is similar to the write operation in serial mode, driver should perform the **WEN** command before writing data to EEPROM. And remember to perform **WDS** command after all the write operations are finished.

Programming steps for APC load and Remote wakeup

APC load

Bios should program the MAC address into APC reg. 09h~0Eh. Then set APC reg. 07h bit3=1 to enable the auto-load APC register to Rx MAC unicast Address.

Set MAC PCI CFG reg. 073h bit0=1 to be Software APC MAC address's valid and then set APC reg. 07h bit3=0 to disable the auto-load. Another, BIOS need to backup the MAC unicast Address to ESCD or DMI for APC fail case.

Prepare for Remote wakeup

All of OP register should use either Word or D-word access according to GMAC OP register definitions.

1. Read the LAN's BAR register 10h to get LAN's OP base.
2. Reset PHY through Station Management Interface(SMI).
   i. Reset PHY by writing data with "80000070h" to OP_Reg 044h-047h and then read OP_Reg 044h~047h to poll bit 4 if this bit turn 0 for the access completed.
   ii. Wait a moment.
   iii. Write OP_Reg 044h-047h data with "00050h" to read PHY_Reg 00 and then read OP_Reg 044h~047h to poll bit 4 if this bit turn 0 for the access completed.

   D-word read OP_Reg 044h-047h bit[31:16] to check if PHY_Reg 00 bit15 turn 0 for PHY reset is completed.
3. Polling PHY Link status
   i. Write OP_Reg 040h-043h data with "04000000h" to set MAC Rx/Tx clock and interface mode.
   ii. Write OP_Reg 044h-047h data with "00850h" to read PHY_Reg 01 and then read OP_Reg 044h~047h to poll bit 4 if this bit turn 0 for the access completed.
   iii. Wait a moment.
   iv. Write OP_Reg 044h-047h data with "00850h" to read PHY_Reg 01 and then read OP_Reg 044h~047h to poll bit 4 if this bit turn 0 for the access completed.
   v. D-word read OP_Reg 044h-047h bit[31:16] to check PHY_Reg 01 bit2
   vi. If PHY Reg01h bit2 is 0, it means Link is OFF. Then the system only use Link-Change to do remote wakeup.
   vii. If PHY Reg01h bit2 is 1, it means Link is ON. Then the system could use Link-Change and Magic-Package to do remote wakeup.

Prepare Link Change feature for wakeup

1. Set OP_Reg 040h-043h bit0=1 to poll Link Status.
2. Poll OP_Reg 030h-033h bit22=1 to check Link Status Changed.
3. Set OP_Reg 030h-033h bit22=1 to clear Link Changed Status.
4. Set OP_Reg 030h-033h bit6=1 to enable the PME for Link Change.

Prepare Magic Package for wakeup

1. Wait for Negotiation complete.
2. Write OP_Reg 044h-047h data with “00850h” to read PHY_Reg 01 and then read OP_Reg 044h~047h to poll bit 4 if this bit turn 0 for the access completed.
3. D-word read OP_Reg 044h-047h bit[31:16] to check PHY_Reg 01 bit5
4. If PHY Reg01h bit5 is 0, it means Negotiation incompleted.Then the system only use Link-Change to do remote wakeup.
5. If PHY Reg01h bit5 is 1, it means Negotiation completed. Then check PHY Reg05h bit15.
6. If PHY Reg05h bit15(Next Page capability) is 1, the PHY would be under Gaga protocol. Then check PHY Reg06h bit1. If that bit is 1, It means link works under GMAC. Need to compare the PHY Reg09h with Reg0Ah.
7. If PHY Reg05h bit15(Next Page capability) is 0 or PHY Reg06h bit1 is 0, It means link works under 10/100Base MAC. Then compare the PHY Reg04h with Reg05h.
8. According to the comparison, set the speed to MAC OP_Reg 041h, set RX filter to MAC OP_Reg 060h-061h=00F00h, and set RX clock enable to MAC OP_Reg 010h bit0=1.
9. Clear Magic Packet Detected status to set MAC OP_Reg 070h bit31=1.
10. Enable Magic packet detector to set MAC OP_Reg 070h bit24=1.
11. Clear Magic Packet Detected Status to set MAC OP_Reg 030h-033h bit23=1.
12. Enable Magic Packet PME to set MAC OP_Reg 030h-033h bit7=1.

PHY reg. 04h Auto Negotiation Advertisement register

Bit	Name	R/W	Description
9	100Base-T4 capable	R/W	1=100Base-T4 0=Not 100Base-T4
8	100Base-TX Full-duplex capable	R/W	1=100Base-TX Full-duplex 0=Not 100Base-TX Full-duplex
7	100Base-TX Half-duplex capable	R/W	1=100Base-TX Half-duplex

			0=Not 100Base-TX Half-duplex
6	10Base-TX Full-duplex capable	R/W	1=10Base-TX Full-duplex 0=Not 10Base-TX Full-duplex
5	10Base-TX Half-duplex capable	R/W	1=10Base-TX Half-duplex 0=Not 10Base-TX Half-duplex

PHY reg. 05h Auto-Negotiation Link Partner Ability register

Bit	Name	R/W	Description
15	Next Page	RO	1=Link Partner has Next Page 0=Link Partner has no Next Page
9	100Base-T4 capable	RO	1=100Base-T4 0=Not 100Base-T4
8	100Base-TX Full-duplex capable	RO	1=100Base-TX Full-duplex 0=Not 100Base-TX Full-duplex
7	100Base-TX Half-duplex capable	RO	1=100Base-TX Half-duplex 0=Not 100Base-TX Half-duplex
6	10Base-TX Full-duplex capable	RO	1=10Base-TX Full-duplex 0=Not 10Base-TX Full-duplex
5	10Base-TX Half-duplex capable	RO	1=10Base-TX Half-duplex 0=Not 10Base-TX Half-duplex

PHY reg. 06h Auto Negotiation Expansion register

Bit	Name	R/W	Description
1	Page Received	RO LH	1=Next Page from Link Partner 0=No Next Page

PHY reg. 09h

Bit	Name	R/W	Description
9	1000Base-TX Full-duplex capable	R/W	1=1000Base-TX Full-duplex 0=Not 1000Base-TX Full-duplex
8	1000Base-TX Half-duplex capable	R/W	1=1000Base-TX Half-duplex 0=Not 1000Base-TX Half-duplex

PHY reg. 0Ah

Bit	Name	R/W	Description
11	Link partner 1000Base-TX Full-duplex capable	RO	1=1000Base-TX Full-duplex 0=Not 1000Base-TX Full-duplex
10	Link partner 1000Base-TX Half-duplex capable	RO	1=1000Base-TX Half-duplex 0=Not 1000Base-TX Half-duplex

MAC OP register 40h

Bit	Name	R/W	Description
15	MII/GMII/RGMII	R/W	1=RGMII

			0=MII/GMII
12	Full Duplex mode	R/W	1=Full Duplex 0=Half Duplex
11~10	Operation Speed	R/W	00=Undetermined 01=10Mbps 10=100Mbps 11=1000Mbps

Pseudo code

All PHY register read/write should through Station Management Interface (MAC OP register 44h~47h). Reg. 31~16 is for either read back data or write data to. Bit 15 ~11 is to put PHY register address. Bit 10 ~ 6 is PHY address, and it will be “00001b”. Bit 5 control the read/write operation, set to 1 is a write access and set to 0 is a read access. Bit 4 is a status bit to indicate if the read/write access complete, software should wait until this bit turn to 0 to indicate either data read back on bit 31 ~ 16 or the write access is complete.

All PHY registers access is through Word data.

1. Write [PHY reg. 00h bit 15 to 1] to reset PHY.
2. Read [PHY reg. 01h bit 2] to check the Link status.
3. If the Link is off, jump to step 10.
4. Read [PHY reg. 01h bit 5] to check the Negotiation.
5. If Negotiation is not complete, do some IO delay. Go to step 4 to check again. If such Negotiation fails above our limit, this link is failed. Stop to do any wakeup feature and end the process.
6. If Negotiation complete, Read [PHY reg. 04h, 05h, 06h, 09h and 0Ah].
7. If [PHY reg. 05 bit 15] is 1, check [PHY reg. 06h, bit 1]. If [PHY reg. 06 bit 1] is 1, compare [PHY reg. 09h] with [PHY reg. 0AH] to get 1000M speed. Otherwise, compare [PHY reg. 04h] with [PHY reg. 05h] to get 10M/100M speed.
8. Fill the speed and duplex mode to [MAC OP register 40h.]
9. Set either [MAC OP reg. 70h bit 24] or [APC reg. 0xfh bit5] to enable the Magic Packet Detector. Set [MAC OP reg. 30h bit 7] to enable the Magic Packet PME. End the process.

10. When Link is off, use Link change to be the wakeup event. Set [MAC OP reg. 40h bit 11~10] to “00b” to indicate the undetermined speed.
11. Set [MAC OP reg. 30h bit 6] to 1 to enable the Link Change PME. End the process.

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