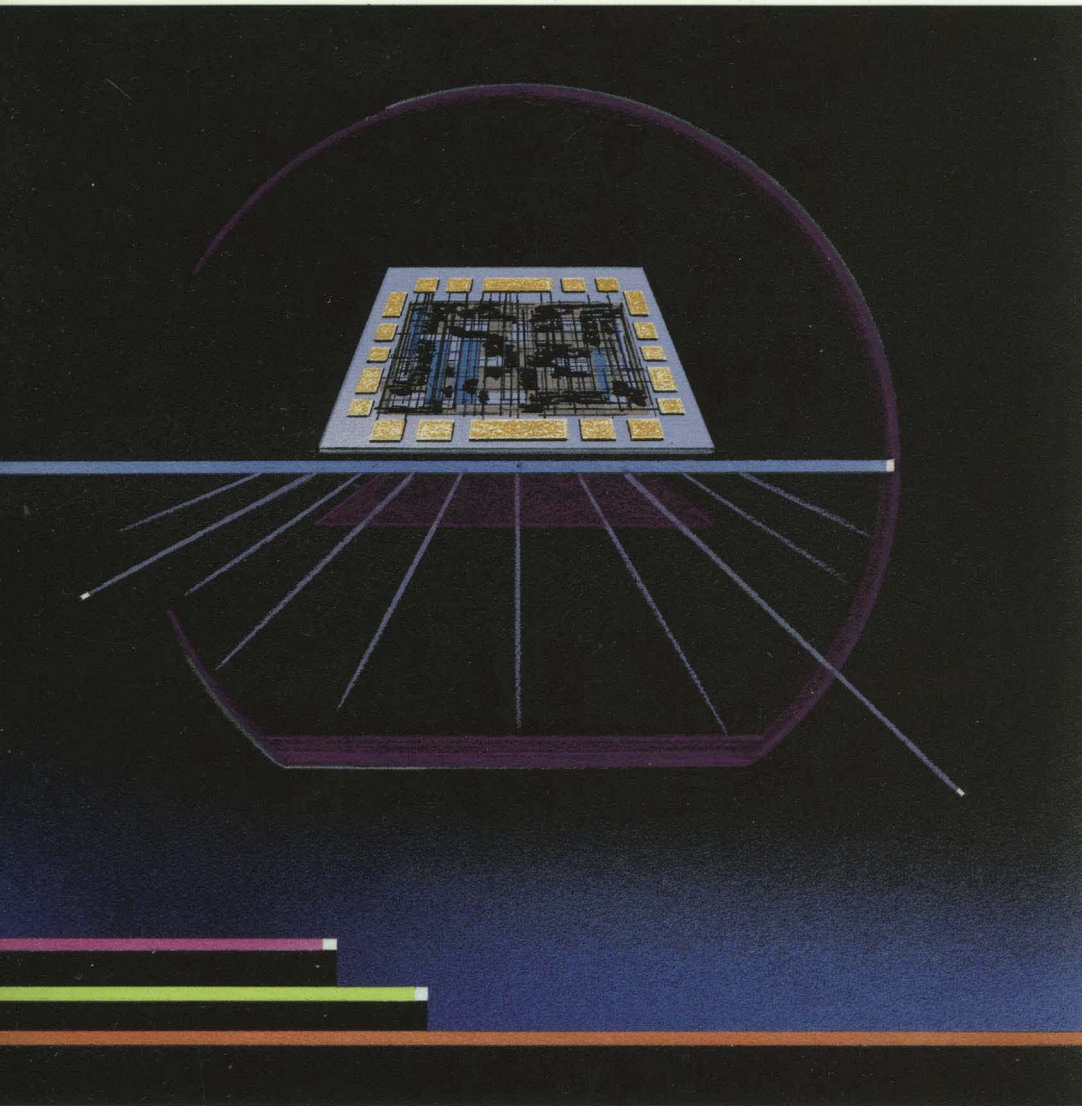


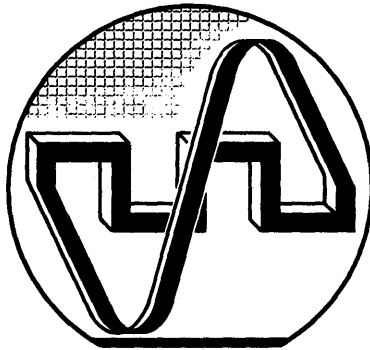
SPT ANALOG PRODUCT CATALOG

JULY 1988



- SIGNAL PROCESSING TECHNOLOGIES -

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JULY 1988 ANALOG PRODUCT CATALOG

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SPT

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This data book presents technical data for a wide variety of integrated circuits and has been organized into sections by product type. Additional sections include product selection guides, ordering information, package specifications, quality flows and application notes.

There are three types of data sheets in this book:

ADVANCE INFORMATION — These data sheets contain the description of products that are in development. The specifications are based on engineering calculations, computer simulations and/or initial prototype evaluation.

PRELIMINARY — These data sheets contain minimum and maximum specifications that are based upon initial device characterization. These limits are subject to change upon the completion of full characterization over the specified temperature and supply voltage ranges.

FINAL — These data sheets contain specifications based on a complete characterization of the device over the specified temperature and supply voltage ranges.

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TABLE OF CONTENTS

SECTION 1	- Selection Guide	1-2
	Product Cross Reference Guide	1-4
	SPT Product Identification Code	1-6
	Ordering Information	1-7
SECTION 2	- Analog to Digital Converters	
	HADC574Z 12-BIT, 25 μ s, B/MOS	2-3
	HADC674Z 12-BIT, 15 μ s, B/MOS	2-25
	HADC7572 12-BIT, 5 μ s, B/MOS	2-47
	HADC7672 12-BIT, 5 μ s, B/MOS	2-49
	HADC77100 8-BIT, 150 MSPS	2-51
	HADC77200 8-BIT, 150 MSPS	2-69
	HADC77600 10-BIT, 50 MSPS	2-89
	HADC78160 16-BIT, 3 μ s	2-103
SECTION 3	- Digital to Analog Converters	
	HDAC7541Z 12-BIT, 500 ns, B/MOS	3-3
	HDAC7542A 12-BIT, 500 ns, B/MOS	3-15
	HDAC7543A 12-BIT, 500 ns, B/MOS	3-27
	HDAC7545A 12-BIT, 500 ns, B/MOS	3-39
	HDAC10180A/B 8-BIT, 275/180 MWPS	3-51
	HDAC10181A/B 8-BIT, 275/180 MWPS	3-63
	HDAC51400 8-BIT, 385 MWPS	3-75
	HDAC52160 16-BIT, 150 ns	3-87
	HDAC97000 8-BIT, 200 MWPS	3-95
SECTION 4	- Comparators	
	HCMP96850 HIGH SPEED SINGLE	4-3
	HCMP96870A HIGH SPEED DUAL	4-13
	HCMP96900 HIGH SPEED DUAL	4-23
SECTION 5	- Filters	
	HSCF24040 7TH ORDER LOW PASS, μ P PROGRAMMABLE ...	5-3
SECTION 6	- Digital Signal Processing	
	HDSP66110 DIGITAL ARRAY SIGNAL PROCESSOR	6-7
	HDSP66210 PROGRAMMABLE ARRAY CONTROLLER	6-12

(Continued)

TABLE OF CONTENTS CONTINUED

SECTION 7 - Evaluation Boards

EB100	HADC77100 & HDAC10181/51400	7-3
EB101	HADC77200 & HDAC10181/51400	7-5
EB102	OPTIONAL BUFFER BOARD	7-7
EB103	HADC77200 PING-PONG APPLICATION	7-9
EB104	HADC574/674Z & HDAC7545A	7-11
EB105	HSCF24040	7-13
EB106	HADC77600 CAV1040 COMPATIBLE	7-15

SECTION 8 - Applications Information

AN100	EB100 EVALUATION BOARD	8-3
AN101	FLASH CONVERTERS	8-29
AN102	EB101 EVALUATION BOARD	8-41
AN103	EB103 EVALUATION BOARD	8-67
AN104	VIDEO DACS & RASTER GRAPHICS	8-83
AN106	EB104 EVALUATION BOARD	8-89
AN108	THERMAL CONSIDERATIONS	8-111
AN109	EB105 EVALUATION BOARD	8-117
AN110	EB106 EVALUATION BOARD	8-125
AN111	HSCF24040 INTERFACE REQUIREMENTS	8-139
AB100	ECL DACS WITH TTL LOGIC	8-151
AB101	VIDEO DAC EXTERNAL SYNC CIRCUIT	8-155
AB102	CHARGE SCALING DATA CONVERTERS	8-157
AB103	HADC574/674Z INPUT STRUCTURE	8-159
AB104	HADC 574/674Z TESTING ON LTS2020	8-163
AB105	GLITCH ENERGY	8-165

SECTION 9 - Quality Assurance

SECTION 10 - Package Outlines

DIE PLOTS	10-3
PACKAGING INFORMATION	10-7

SECTION 11 - Sales Representatives

AREA SALES MANAGERS	11-3
DOMESTIC REPRESENTATIVES	11-3
DOMESTIC DISTRIBUTORS	11-5
INTERNATIONAL DISTRIBUTORS	11-6
FAR EAST DISTRIBUTORS	11-6

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

PRODUCT SELECTION GUIDE

A/D CONVERTERS

PART NO.	RESOLUTION (BITS)	SAMPLE RATE (MSPS)	CONVERSION TIME (μ s)	LOGIC FAMILY	LINEARITY INT	LINEARITY DIF	FEATURES
HADC 77100A	8	150		ECL	1/2	1/2	PRE AMPLIFIER DESIGN
HADC 77100B	8	150		ECL	3/4	3/4	
HADC 77200A	8	150		ECL	1/2	1/2	DATA READY AND OVERRANGE OUTPUTS, QUARTER POINT LADDER TAPS, IMPROVED ANALOG PERFORMANCE
HADC 77200B	8	150		ECL	3/4	3/4	
HADC 77800	10	50		ECL	1	1/2	ON BOARD BUFFER, METASTABLE STATE ERROR REDUCTION
HADC 7572	12		5	TTL	1/2	1/2	ON-CHIP REFERENCE
HADC 7672	12		5	TTL	1/2	1/2	BIPOLAR INPUT WITH OPTIONAL REFERENCE
HADC 674A	12		15	TTL	1/2	1/2	
HADC 674B	12		15	TTL	1/2	1/2	
HADC 674C	12		15	TTL	1	1	MONOLITHIC, S/H FUNCTION, LOW POWER, NO NEGATIVE SUPPLY REQUIRED, NO TRANSIENTS AT INPUT
HADC 574A	12		25	TTL	1/2	1/2	FULL BIPOlar INPUT, ALTERNATES FOR HI574, HI674 AND AD574
HADC 574B	12		25	TTL	1/2	1/2	
HADC 574C	12		25	TTL	1	1	
HADC 78160	16		3	TTL	2	2	ON-CHIP REFERENCE

D/A CONVERTERS

PART NO.	RESOLUTION (BITS)	UPDATE RATE (MSPS)	SETTLING TIME (ns)	LOGIC FAMILY	LINEARITY INT	LINEARITY DIF	FEATURES
HDAC 51400	8	385	3	ECL	1/2	1/2	REF, VIDEO CONTROL
HDAC 10181A	8	275	3	ECL	1/2	1/2	REF, VIDEO CONTROL
HDAC 10180A	8	275	3	ECL	1/2	1/2	VIDEO CONTROL, ALTERNATE FOR TEC 1018
HDAC 97000	8	200	10	ECL	1/2	1/2	REF, ALTERNATE FOR AD9700
HDAC 10181B	8	180	3	ECL	1/2	1/2	REF, VIDEO CONTROL
HDAC 10180B	8	180	3	ECL	1/2	1/2	VIDEO CONTROL, ALTERNATE FOR TDC 1018
HDAC 7541Z	12		500	TTL	1/2	1/2	ALTERNATE FOR AD7541A
HDAC 7542A	12		500	TTL	1/2	1/2	ALTERNATE FOR AD7542
HDAC 7543A	12		500	TTL	1/2	1/2	ALTERNATE FOR AD7543
HDAC 7545A	12		500	TTL	1/2	1/2	ALTERNATE FOR AD7545
HDAC 52160	16		150	TTL	1	2	PARALLEL INPUT, REFERENCE

COMPARATORS

PART NO.	tr/ta (ns)	PROP DELAY (ns)	V _{cm} (V)	V _{os} (mV)	R _{in} (kΩ)	AV (V/V)	FEATURES
HCMP 96850	1.76/1.76	3.0	±2.5V	±3.0	60	4K	SYMETRICAL t _r /t _f , ALTERNATE FOR SP9685, AM6685
HCMP 96870A	1.2/1.2	2.3	±2.5	±3.0	60	4k	HIGH PERFORMANCE, ALTERNATE FOR SP9687, AM6687
HCMP 96900	1.0/1.0	5.0	+10 -3	±0.5	10,000	1k	HIGH V _{cm} RANGE, SYMETRICAL t _r /t _f AND PROP DELAY INDEPENDENT OF OVERDRIVE AND V _{cm}

FILTER

PART NO.	DYNAMIC RANGE (dB)	MAX BANDEDGE (kHz)	BANDEDGE TOLERANCE (%)	SUPPLY VOLTAGE (V)	FEATURES
HSCF 24040	85	20	±0.5	±5	7TH ORDER LOW PASS, > 76dB STOPBAND ATTENUATION, ON CHIP ANTIALIAS FILTER, DIGITALLY PROGRAMMABLE BANDEDGE AND DC GAIN

DIGITAL SIGNAL PROCESSING

PART NO.	DESCRIPTION	FEATURES
HDSP66110	DIGITAL ARRAY SIGNAL PROCESSOR (DASP)	ULTRA HIGH PERFORMANCE FFT BASED DSP SYSTEM
HDSP66210	PROGRAMMABLE ARRAY CONTROLLER (PAC)	

EVALUATION BOARDS

PART NO.	FEATURED PRODUCT	FEATURES
EB 100	HADC77100	150MSPS A/D, D/A
EB 101	HADC77200	150MSPS A/D, D/A
EB 102	N/A	100MHz BUFFER AMP, 8-BITS
EB 103	HADC77200	300MSPS PING-PONG, A/D, D/A
EB 104	HADC574/674	A/D, D/A, OPTIONAL S/H
EB 105	HSCF24040	ON BOARD OR EXTERNAL PROGRAMMING
EB 106	HADC77600	CAV1040 COMPATIBLE
EB 107	HDSP66110/HDSP66210	BUFFERED MEMORY RECURSIVE DSP SYSTEM
EB 108	HADC77600	10-BIT A/D—USE WITH EB107
EB 109	HDAC52160	16-BIT D/A—USE WITH EB107

1

PRODUCT CROSS REFERENCE GUIDE

(SPT TO INDUSTRY EQUIVALENT)

SPT PART #	ALTERNATE	DESCRIPTION	SPT PART #	ALTERNATE	DESCRIPTION
HADC574ZCCJ	AD574AJD	12-BIT RES ADC; 11-BIT LIN	HDAC7543ABMD	MP7543SD	12-BIT RES DAC; 11-BIT LIN
HADC574ZBCJ	AD574AKD	12-BIT RES ADC; 12-BIT LIN	HDAC7543AAMD	MP7543TD	12-BIT RES DAC; 12-BIT LIN
HADC574ZACJ	ADC574ALD	12-BIT RES ADC; 12-BIT LIN	HDAC7543AAMD/G	PM7543AQ	12-BIT RES DAC; 12-BIT LIN
HADC574ZCCJ	HI1-574AJD-5	12-BIT RES ADC; 11-BIT LIN	HDAC7543AAMD	PM7543BQ	12-BIT RES DAC; 12-BIT LIN
HADC574ZBCJ	HI1-574AKD-5	12-BIT RES ADC; 12-BIT LIN	HDAC7543ABMD	PM7543BQ	12-BIT RES DAC; 11-BIT LIN
HADC574ZACJ	HI-574ALD-5	12-BIT RES ADC; 12-BIT LIN	HDAC7543AAMD/G	PM7543EQ	12-BIT RES DAC; 12-BIT LIN
HADC674ZCCJ	HI674AJD-5	12-BIT RES ADC; 11-BIT LIN	HDAC7543AAID	PM7543FQ	12-BIT RES DAC; 12-BIT LIN
HADC674ZBCJ	HI-674AKD-5	12-BIT RES ADC; 12-BIT LIN	HDAC7543ABID	PM7543FQ	12-BIT RES DAC; 11-BIT LIN
HADC674ZACJ	HI-674ALD-5	12-BIT RES ADC; 12-BIT LIN	HDAC7543A	PM7543G	12-BIT RES DAC; DIE
HADC77100AJ	CX20116	8-BIT, 150 MSPS ADC \pm 1/2 LSB	HDAC7545ABID	AD7545AQ	12-BIT RES DAC; 11-BIT LIN
HDAC10180	IDT1018	8-BIT, 275 MWPS DAC	HDAC7545ABID	AD7545BQ	12-BIT RES DAC; 12-BIT LIN
HDAC10180AID	TEC1018BJ7C	8-BIT, 275 MWPS DAC	HDAC7545A	AD7545CHIPS	12-BIT RES DAC; DIE
HDAC7541ZBID	AD7541AAQ	12-BIT RES DAC; 11-BIT LIN	HDAC7545AAID	AD7545SQ	12-BIT RES DAC; 12-BIT LIN
HDAC7541ZAID	AD7541ABQ	12-BIT RES DAC; 12-BIT LIN	HDAC7545AAID/G	AD7543GCQ	12-BIT RES DAC; 12-BIT LIN
HDAC7541Z	AD7541ACHIPS	12-BIT RES DAC; DIE	HDAC7545AAMD/G	AD7545GUD	12-BIT RES DAC; 12-BIT LIN
HDAC7541ZBMD	AD7541ASD	12-BIT RES DAC; 12-BIT LIN	HDAC7545ABMD	AD7545SD	12-BIT RES DAC; 11-BIT LIN
HDAC7541ZAMD	AD7541ATD	12-BIT RES DAC; 11-BIT LIN	HDAC7545ABMD	AD7545TD	12-BIT RES DAC; 11-BIT LIN
HDAC7541Z	MP7623	12-BIT RES DAC; DIE	HDAC7545AAMD	AD7545UD	12-BIT RES DAC; 12-BIT LIN
HDAC7541ZBID	MP7623AD	12-BIT RES DAC; 11-BIT LIN	HDAC7545A	MP7545	12-BIT RES DAC; DIE
HDAC7541ZAID	MP7623BD	12-BIT RES DAC; 12-BIT LIN	HDAC7545ABID	MP7545AD	12-BIT RES DAC; 11-BIT LIN
HDAC7541ZBMD	MP7623SD	12-BIT RES DAC; 11-BIT LIN	HDAC7545ABID	MP7545BD	12-BIT RES DAC; 11-BIT LIN
HDAC7541ZAMD	MP7623TD	12-BIT RES DAC; 12-BIT LIN	HDAC7545AAID	MP7545CD	12-BIT RES DAC; 12-BIT LIN
HDAC7542ABID	AD7542AD	12-BIT RES DAC; 11-BIT LIN	HDAC7545ABMD	MP7545SD	12-BIT RES DAC; 11-BIT LIN
HDAC7542AAID	AD7542BD	12-BIT RES DAC; 12-BIT LIN	HDAC7545ABMD	MP7545TD	12-BIT RES DAC; 11-BIT LIN
HDAC7542A	AD7542CHIPS	12-BIT RES DAC; DIE	HDAC7545AAMD	MP7545UD	12-BIT RES DAC; 12-BIT LIN
HDAC7542AAID/G	AD7542GBD	12-BIT RES DAC; 12-BIT LIN	HDAC7545AAMD/G	PM7545AR	12-BIT RES DAC; 12-BIT LIN
HDAC7542AAMD/G	AD7542GTD	12-BIT RES ADC; 12-BIT LIN	HDAC7545AAMD	PM7545BR	12-BIT RES DAC; 12-BIT LIN
HDAC7542ABMD	AD7542SD	12-BIT RES DAC; 11-BIT LIN	HDAC7545ABMD	PM7545BR	12-BIT RES DAC; 11-BIT LIN
HDAC7542AAMD	AD7542TD	12-BIT RES DAC; 12-BIT LIN	HDAC7545AAID/G	PM7545ER	12-BIT RES DAC; 12-BIT LIN
HDAC7542A	MP7542	12-BIT RES DAC; DIE	HDAC7545AAID	PM7545FR	12-BIT RES DAC; 12-BIT LIN
HDAC7542ABID	MP7542AD	12-BIT RES DAC; 11-BIT LIN	HDAC7545ABID	PM7545FR	12-BIT RES DAC; 11-BIT LIN
HDAC7542AAID	MP7542BD	12-BIT RES DAC; 12-BIT LIN	HDAC7545A	PM7545G	12-BIT RES DAC; DIE
HDAC7542ABMD	MP7542SD	12-BIT RES DAC; 11-BIT LIN	HDAC97000SID	AD9700D22A	8-BIT, 200 MWPS DAC W/REF
HDAC7542AAMD	MP7542TD	12-BIT RES DAC; 12-BIT LIN	HCMP96850SID	AD9685B	HIGH SPEED COMPARATOR
HDAC7542AAMD/G	PM7542AQ	12-BIT RES DAC; 12-BIT LIN	HCMP96850SID	AM6688DL	HIGH SPEED COMPARATOR
HDAC7542AAMD	PM7542BQ	12-BIT RES DAC; 12-BIT LIN	HCMP96850SID	SP9685DG18	HIGH SPEED COMPARATOR
HDAC7542ABMD	PM7542BQ	12-BIT RES DAC; 11-BIT LIN	HCMP96870AID	AD9687B	DUAL HIGH SPEED COMPARATOR
HDAC7542AAID/G	PM7542EQ	12-BIT RES DAC; 12-BIT LIN	HCMP96870AID	AM6686DL	DUAL HIGH SPEED COMPARATOR
HDAC7542AAID	PM7542FQ	12-BIT RES DAC; 12-BIT LIN	HCMP96870AIC	AM6687LL	DUAL HIGH SPEED COMPARATOR
HDAC7542ABID	PM7542FQ	12-BIT RES DAC; 11-BIT LIN	HCMP96870AID	SP9687DG16	DUAL HIGH SPEED COMPARATOR
HDAC7542A	PM7542G	12-BIT RES DAC; DIE			
HDAC7543ABID	AD7543AD	12-BIT RES DAC; 11-BIT LIN			
HDAC7543AAID	AD7543BD	12-BIT RES DAC; 12-BIT LIN			
HDAC7543A	AD7543CHIPS	12-BIT RES DAC; DIE			
HDAC7543AAID/G	AD7543GBD	12-BIT RES DAC; 12-BIT LIN			
HDAC7543AAMD/G	AD7543GTD	12-BIT RES DAC; 12-BIT LIN			
HDAC7543ABMD	AD7543SD	12-BIT RES DAC; 11-BIT LIN			
HDAC7543AAMD	AD7543TD	12-BIT RES DAC; 12-BIT LIN			
HDAC7543A	MP7543	12-BIT RES DAC; DIE			
HDAC7543ABID	MP7543AD	12-BIT RES DAC; 11-BIT LIN			
HDAC7543AAID	MP7543BD	12-BIT RES DAC; 12-BIT LIN			

PRODUCT CROSS REFERENCE GUIDE

(INDUSTRY TO SPT EQUIVALENT)

1

ANALOG DEVICES	SPT	DESCRIPTION
AD574AJD	HADC574ZCCJ	12-BIT RES ADC; 11-BIT LIN
AD574AKD	HADC574ZBCJ	12-BIT RES ADC; 12-BIT LIN
AD574ALD	HADC574ZACJ	12-BIT RES ADC; 12-BIT LIN
AD7541AAQ	HDAC7541ZBID	12-BIT RES DAC; 11-BIT LIN
AD7541ABQ	HDAC7541ZAID	12-BIT RES DAC; 12-BIT LIN
AD7541ACHIPS	HDAC7541Z	12-BIT RES DAC - DIE
AD7541ASD	HDAC7541ZBMD	12-BIT RES DAC; 11-BIT LIN
AD7541ATD	HDAC7541ZAMD	12-BIT RES DAC; 12-BIT LIN
AD7542AD	HDAC7542ABID	12-BIT RES DAC; 11-BIT LIN
AD7542BD	HDAC7542AAID	12-BIT RES DAC; 12-BIT LIN
AD7542CHIPS	HDAC7542A	12-BIT RES DAC - DIE
AD7542GBD	HDAC7542AAID/G	12-BIT RES DAC; 12-BIT LIN
AD7542GTD	HDAC7542AAMD/G	12-BIT RES DAC; 12-BIT LIN
AD7542SD	HDAC7542ABMD	12-BIT RES DAC; 11-BIT LIN
AD7542TD	HDAC7542AAMD	12-BIT RES DAC; 12-BIT LIN
AD7543AD	HDAC7543ABID	12-BIT RES DAC; 11-BIT LIN
AD7543BD	HDAC7543AAID	12-BIT RES DAC; 12-BIT LIN
AD7543CHIPS	HDAC7543A	12-BIT RES DAC - DIE
AD7543GBD	HDAC7543AAID/G	12-BIT RES DAC; 12-BIT LIN
AD7543GTD	HDAC7543AAMD/G	12-BIT RES DAC; 12-BIT LIN
AD7543SD	HDAC7543ABMD	12-BIT RES DAC; 11-BIT LIN
AD7543TD	HDAC7543AAMD	12-BIT RES DAC; 12-BIT LIN
AD7545AQ	HDAC7545ABID	12-BIT RES DAC; 11-BIT LIN
AD7545BQ	HDAC7545ABID	12-BIT RES DAC; 11-BIT LIN
AD7545CHIPS	HDAC7545A	12-BIT RES DAC - DIE
AD7545CQ	HDAC7545AAID	12-BIT RES DAC; 12-BIT LIN
AD7545GQC	HDAC7545AAID/G	12-BIT RES DAC; 12-BIT LIN
AD7545GUD	HDAC7545AAMD/G	12-BIT RES DAC; 12-BIT LIN
AD7545SD	HDAC7545ABMD	12-BIT RES DAC; 11-BIT LIN
AD7545TD	HDAC7545ABMD	12-BIT RES DAC; 11-BIT LIN
AD7545UD	HDAC7454AAMD	12-BIT RES DAC; 12-BIT LIN
AD9700D22A	HDAC97000SID	8-BIT, 200 MWPS DAC W/REF
AD9685B	HCMP96850SID	HIGH SPEED COMPARATOR
AD9687B	HCMP96870AIS	DUAL HIGH SPEED COMPARATOR

AMD	SPT	DESCRIPTON
AM8685DL	HCMP96850SID	HIGH SPEED COMPARATOR
AM8687DL	HCMP96870AID	DUAL HIGH SPEED COMPARATOR
AM8687DL	HCMP96870AIC	DUAL HIGH SPEED COMPARATOR

HARRIS	SPT	DESCRIPTION
HI1-574AJD-5	HADC574ZCCJ	12-BIT RES ADC; 11-BIT LIN
HI1-574AKD-5	HADC574ZBCJ	12-BIT RES ADC; 12-BIT LIN
HI1-574ALD-5	HADC574ZACJ	12-BIT RES ADC; 12-BIT LIN
HI1-674AJD-5	HADC674ZCCJ	12-BIT RES ADC; 11-BIT LIN
HI1-674AKD-5	HADC674ZBCJ	12-BIT RES ADC; 12-BIT LIN
HI1-674ALD-5	HADC674ZACJ	12-BIT RES ADC; 12-BIT LIN

MICRO POWER	SPT	DESCRIPTION
MP7623DIE	HDAC7541Z	12-BIT RES DAC - DIE
MP7623AD	HDAC7541ZBID	12-BIT RES DAC; 11-BIT LIN
MP7623BD	HDAC7541ZAID	12-BIT RES DAC; 12-BIT LIN
MP7623SD	HDAC7541ZBMD	12-BIT RES DAC; 11-BIT LIN
MP7623TD	HDAC7541ZAMD	12-BIT RES DAC; 12-BIT LIN
MP7542DIE	HDAC7542A	12-BIT RES DAC - DIE
MP7542AD	HDAC7542ABID	12-BIT RES DAC; 11-BIT LIN
MP7542BD	HDAC7542AAID	12-BIT RES DAC; 12-BIT LIN
MP7542SD	HDAC7542ABMD	12-BIT RES DAC; 11-BIT LIN
MP7542TD	HDAC7542AAMD	12-BIT RES DAC; 12-BIT LIN
MP7543DIE	HDAC7543A	12-BIT RES DAC - DIE
MP7543AD	HDAC7543ABID	12-BIT RES DAC; 11-BIT LIN
MP7543BD	HDAC7543AAID	12-BIT RES DAC; 12-BIT LIN
MP7543SD	HDAC7543ABMD	12-BIT RES DAC; 11-BIT LIN
MP7543TD	HDAC7543AAMD	12-BIT RES DAC; 12-BIT LIN
MP7545DIE	HDAC7545A	12-BIT RES DAC - DIE
MP7545AD	HDAC7545ABID	12-BIT RES DAC; 11-BIT LIN
MP7545BD	HDAC7545AAID	12-BIT RES DAC; 12-BIT LIN
MP7545SD	HDAC7545ABMD	12-BIT RES DAC; 11-BIT LIN
MP7545UD	HDAC7545AAMD	12-BIT RES DAC; 12-BIT LIN

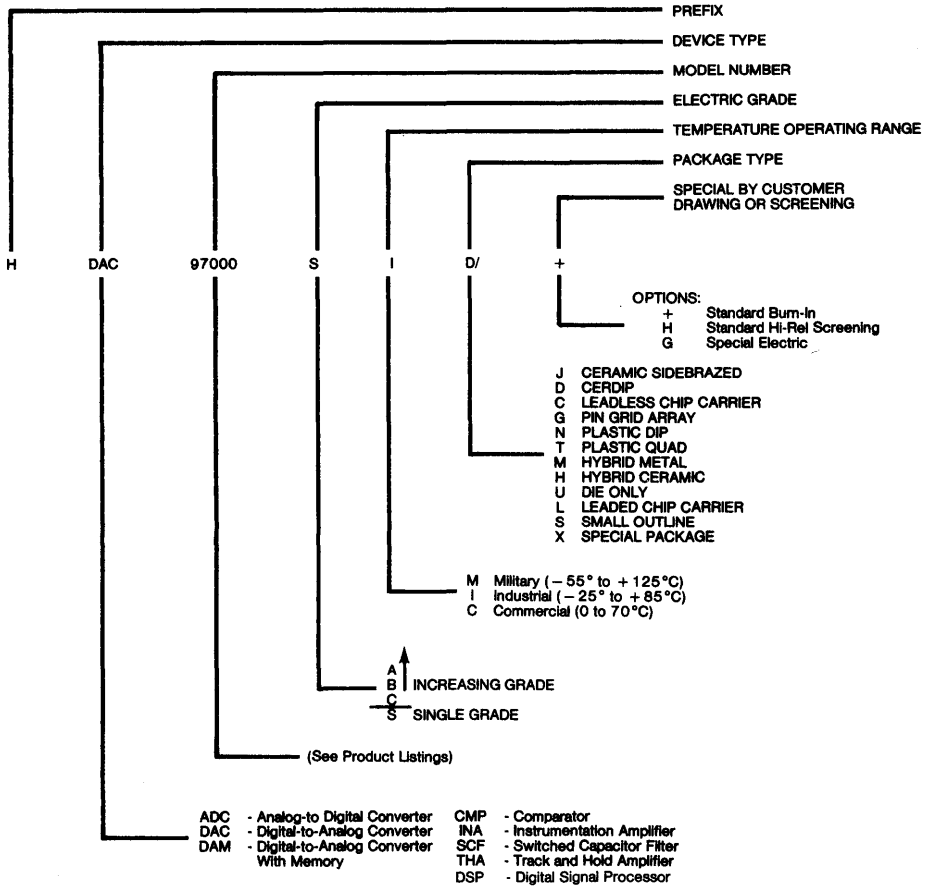
PMI	SPT	DESCRIPTION
PM7542AQ	HDAC7542AAMD/G	12-BIT RES DAC; 12-BIT LIN
PM7542BQ	HDAC7542AAMD	12-BIT RES DAC; 12-BIT LIN
PM7542BQ	HDAC7542ABMD	12-BIT RES DAC; 11-BIT LIN
PM7542EQ	HDAC7542AAID/G	12-BIT RES DAC; 12-BIT LIN
PM7542FQ	HDAC7542AAID	12-BIT RES DAC; 12-BIT LIN
PM7542FQ	HDAC7542ABID	12-BIT RES DAC; 11-BIT LIN
PM7542G	HDAC7542A	12-BIT RES DAC - DIE
PM7543AQ	HDAC7543AAMD/G	12-BIT RES DAC; 12-BIT LIN
PM7543BQ	HDAC7543AAMD	12-BIT RES DAC; 12-BIT LIN
PM7543BQ	HDAC7543ABMD	12-BIT RES DAC; 11-BIT LIN
PM7543EQ	HDAC7543AAID/G	12-BIT RES DAC; 12-BIT LIN
PM7543FQ	HDAC7543AAID	12-BIT RES DAC; 12-BIT LIN
PM7543FQ	HDAC7543ABID	12-BIT RES DAC; 11-BIT LIN
PM7543G	HDAC7543A	12-BIT RES DAC - DIE
PM7545AR	HDAC7545AAMD/G	12-BIT RES DAC; 12-BIT LIN
PM7545BR	HDAC7545AAMD	12-BIT RES DAC; 12-BIT LIN
PM7545BR	HDAC7545ABMD	12-BIT RES DAC; 11-BIT LIN
PM7545ER	HDAC7545AAID/G	12-BIT RES DAC; 12-BIT LIN
PM7545FR	HDAC7545AAID	12-BIT RES DAC; 12-BIT LIN
PM7545FR	HDAC7545ABID	12-BIT RES DAC; 11-BIT LIN
PM7545G	HDAC7545A	12-BIT RES DAC - DIE

PLESSEY	SPT	DESCRIPTION
SP9685DG16	HCMP96850SID	HIGH SPEED COMPARATOR
SP9687DG16	HCMP96870AID	DUAL HIGH SPEED COMPARATOR

SONY	SPT	DESCRIPTION
CX20116	HADC77100AJ	8-BITm 150 MWPS ADC ± ½ LSB

IDT	SPT	DESCRIPTION
IDT1018	HDAC10180	8-BIT, 275 MWPS DAC

SPT PRODUCT IDENTIFICATION CODE



ANALOG TO DIGITAL CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HADC574ZACJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC574ZBCJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC574ZCCJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC574ZAIJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	INDUSTRIAL
HADC574ZBIJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	INDUSTRIAL
HADC574ZCIJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	INDUSTRIAL
HADC574ZAMJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	MILITARY
HADC574ZBMJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	MILITARY
HADC574ZCMJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	MILITARY
HADC574ZAMJ/883C	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED*	28	MILITARY
HADC574ZBMJ/883C	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED*	28	MILITARY
HADC574ZCMJ/883C	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED*	28	MILITARY
HADC574Z	12-BIT RES ADC	LCC*	28	COM., IND., & MIL.
HADC574Z	12-BIT RES ADC	PLASTIC*	28	COMMERCIAL
HADC574Z	12-BIT RES ADC	DIE*		+ 25°C
HADC674ZACJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC674ZBCJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC674ZCCJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	COMMERCIAL
HADC674ZAIJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	INDUSTRIAL
HADC674ZBIJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	INDUSTRIAL
HADC674ZCIJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	INDUSTRIAL
HADC674ZAMJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	MILITARY
HADC674ZBMJ	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED	28	MILITARY
HADC674ZCMJ	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED	28	MILITARY
HADC674ZAMJ/883C	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED*	28	MILITARY
HADC674ZBMJ/883C	12-BIT RES ADC; 12-BIT LIN	SIDEBRAZED*	28	MILITARY
HADC674ZCMJ/883C	12-BIT RES ADC; 11-BIT LIN	SIDEBRAZED*	28	MILITARY
HADC674Z	12-BIT RES ADC	LCC*	28	COM., IND., & MIL.
HADC674Z	12-BIT RES ADC	PLASTIC*	28	COMMERCIAL
HADC674Z	12-BIT RES ADC	DIE*		+ 25°C
HADC7572	12 BIT RES ADC	*	24	COM., IND., & MIL.
HADC7672	12-BIT RES ADC	*	24	COM., IND., & MIL.
HADC77100AIJ	8-BIT, 150 MSPS ADC $\pm \frac{1}{2}$ LSB	SIDEBRAZED	42	INDUSTRIAL
HADC77100BIJ	8-BIT, 150 MSPS ADC $\pm \frac{3}{4}$ LSB	SIDEBRAZED	42	INDUSTRIAL
HADC77100AMJ	8-BIT, 150 MSPS ADC $\pm \frac{1}{2}$ LSB	SIDEBRAZED	42	MILITARY
HADC77200AIJ	8-BIT, 150 MSPS ADC $\pm \frac{1}{2}$ LSB	SIDEBRAZED	48	INDUSTRIAL
HADC77200BIJ	8-BIT, 150 MSPS ADC $\pm \frac{3}{4}$ LSB	SIDEBRAZED	48	INDUSTRIAL
HADC77200AMJ	8-BIT, 150 MSPS ADC $\pm \frac{1}{2}$ LSB	SIDEBRAZED	48	MILITARY
HADC77200AMJ/883C	8-BIT, 150 MSPS ADC $\pm \frac{1}{2}$ LSB	SIDEBRAZED*	48	MILITARY
HADC77600SCG	10-BIT, 50 MSPS ADC $\pm \frac{3}{4}$ LSB	PGA*	72	COMMERCIAL
HADC77600SIG	10-BIT, 50 MSPS ADC $\pm \frac{3}{4}$ LSB	PGA*	72	INDUSTRIAL
HADC77600SMG	10-BIT, 50 MSPS ADC $\pm \frac{3}{4}$ LSB	PGA*	72	MILITARY
HADC78160	16-BIT RES ADC	SIDEBRAZED*	40	

*Consult Factory For Availability

ORDERING INFORMATION

DIGITAL TO ANALOG CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HDAC7541ZACD	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	COMMERCIAL
HDAC7541ZBCD	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	COMMERCIAL
HDAC7541ZAID	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7541ZBID	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7541ZAMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	MILITARY
HDAC7541ZBMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	MILITARY
HDAC7541Z	12-BIT RES DAC	PLASTIC*	18	COMMERCIAL
HDAC7541Z	12-BIT RES DAC	DIE*		+ 25°C
HDAC7542AACD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	COMMERCIAL
HDAC7542AACD	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	COMMERCIAL
HDAC7542ABCD	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	COMMERCIAL
HDAC7542AAID/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7542AAID	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7542ABID	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7542AAMD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	MILITARY
HDAC7542AAMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	MILITARY
HDAC7542ABMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	MILITARY
HDAC7542A	12-BIT RES DAC	PLASTIC*	18	COMMERCIAL
HDAC7542A	12-BIT RES DAC	DIE*		+ 25°C
HDAC7543AACD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	COMMERCIAL
HDAC7543AACD	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	COMMERCIAL
HDAC7543ABCD	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	COMMERCIAL
HDAC7543AAID/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7543AAID	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7543ABID	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	INDUSTRIAL
HDAC7543AAMD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	MILITARY
HDAC7543AAMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	18	MILITARY
HDAC7543ABMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	18	MILITARY
HDAC7543A	12-BIT RES DAC	PLASTIC*	18	COMMERCIAL
HDAC7543A	12-BIT RES DAC	DIE*		+ 25°C
HDAC7545AACD/G	12 BIT RES DAC; 12-BIT LIN	CERDIP	20	COMMERCIAL
HDAC7545AACD	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	COMMERCIAL
HDAC7545ABCD	12-BIT RES DAC; 11-BIT LIN	CERDIP	20	COMMERCIAL
HDAC7545AAID/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC7545AAID	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC7545ABID	12-BIT RES DAC; 11-BIT LIN	CERDIP	20	INDUSTRIAL
HDAC7545AAMD/G	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	MILITARY
HDAC7545AAMD	12-BIT RES DAC; 12-BIT LIN	CERDIP	20	MILITARY
HDAC7545ABMD	12-BIT RES DAC; 11-BIT LIN	CERDIP	20	MILITARY
HDAC7545A	12-BIT RES DAC	PLASTIC*	20	COMMERCIAL
HDAC7545A	12-BIT RES DAC	DIE*		+ 25°C

*Consult Factory For Availability

DIGITAL TO ANALOG CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HDAC10180AID	8-BIT, 275 MWPS DAC	CERDIP	24	INDUSTRIAL
HDAC10180BID	8-BIT, 165 MWPS DAC	CERDIP	24	INDUSTRIAL
HDAC10180AMD	8-BIT, 275 MWPS DAC	CERDIP	24	MILITARY
HDAC10180BMD	8-BIT, 165 MWPS DAC	CERDIP	24	MILITARY
HDAC10180AMD/883C	8-BIT, 275 MWPS DAC	CERDIP*	24	MILITARY
HDAC10180BMD/883C	8-BIT, 165 MWPS DAC	CERDIP*	24	MILITARY
HDAC10181AID	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC10181BID	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC10181AMD	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC10181BMD	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC10181AMD/883C	8-BIT, 275 MWPS DAC W/REF	CERDIP*	24	MILITARY
HDAC10181BMD/883C	8-BIT, 165 MWPS DAC W/REF	CERDIP*	24	MILITARY
HDAC51400SID	8-BIT, 385 MWPS DAC W/REF	CERDIP	24	INDUSTRIAL
HDAC51400SMD	8-BIT, 385 MWPS DAC W/REF	CERDIP	24	MILITARY
HDAC51400SMD/883C	8-BIT, 385 MWPS DAC W/REF	CERDIP*	24	MILITARY
HDAC52160AIJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	INDUSTRIAL
HDAC52160BIJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	INDUSTRIAL
HDAC52160CIJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	INDUSTRIAL
HDAC52160	16-BIT RES DAC W/REF	DIE*		+ 25°C
HDAC97000SIJ	8-BIT, 200 MWPS DAC W/REF	SIDEBRAZED	22	INDUSTRIAL
HDAC97000SID	8-BIT, 200 MWPS DAC W/REF	CERDIP	22	INDUSTRIAL
HDAC97000SMJ	8-BIT, 200 MWPS DAC W/REF	SIDEBRAZED	22	MILITARY
HDAC97000SMD	8-BIT, 200 MWPS DAC W/REF	CERDIP	22	MILITARY

*Consult Factory For Availability

1

ORDERING INFORMATION

COMPARATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HCMP96850SID	HIGH SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96850	HIGH SPEED COMPARATOR	DIE*		+25°C
HCMP96870AID	DUAL HIGH SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96870AIC	DUAL HIGH SPEED COMPARATOR	LCC	20	INDUSTRIAL
HCMP96870AIJ	DUAL HIGH SPEED COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
HCMP96870	DUAL HIGH SPEED COMPARATOR	DIE*		+25°C
HCMP96800SIJ	DUAL HIGH SPEED COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
HCMP96800SIC	DUAL HIGH SPEED COMPARATOR	LCC	20	INDUSTRIAL
HCMP96800	DUAL HIGH SPEED COMPARATOR	DIE*		+25°C

FILTERS

HSCF24040ACJ	LOW PASS PROGRAMMABLE FILTER	SIDEBRAZED	32	COMMERCIAL
HSCF24040AMJ	LOW PASS PROGRAMMABLE FILTER	SIDEBRAZED	32	MILITARY
HSCF24040	LOW PASS PROGRAMMABLE FILTER	DIE*		+25°C

EVALUATION BOARDS

EB100A	HADC77100AIJ DEMO BOARD
EB100B	HADC77100BIJ DEMO BOARD
EB101A	HADC77200AIJ DEMO BOARD
EB101B	HADC77200BIJ DEMO BOARD
EB102B	CLC231 BUFFER BOARD
EB103	HADC77200J77300 PING-PONG BOARD
EB104	HADC574/674Z DEMO BOARD
EB105	HSCF24040 DEMO BOARD
EB106	CAV 1040 COMPATIBLE HADC77600 DEMO BOARD
EB107	HDSP66110/HDSP66210 DEMO BOARD
EB108	A/D DEMO BOARD FOR EB107*
EB109	D/A DEMO BOARD FOR EB107*

*Consult Factory For Availability

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

**FAST, COMPLETE 12-BIT μ P COMPATIBLE
A/D CONVERTER WITH SAMPLE/HOLD**

FEATURES:

- IMPROVED PIN-TO-PIN COMPATIBLE MONOLITHIC VERSION OF THE HI574A AND AD574A
- Complete 12-bit A/D Converter with Sample-Hold, Reference and Clock
- Low Power Dissipation (150mW Max)
- 12-bit Linearity (over temp)
- 25 μ s Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS:

- MILITARY/INDUSTRIAL DATA ACQUISITION SYSTEMS
- 8 OR 12-bit μ P Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

2

GENERAL DESCRIPTION

The HADC574Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI574A and AD574A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

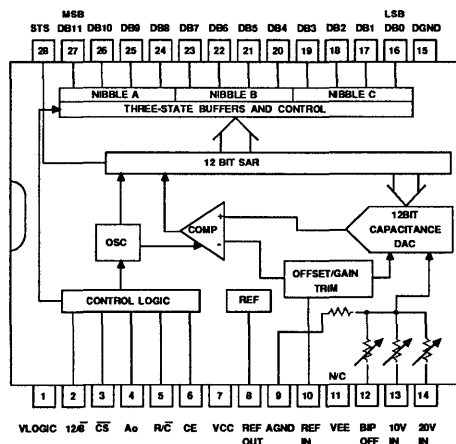
The HADC574Z features 25 μ s (Max) conversion time of 10 or 20 Volt input signals. Also, a 3-state output buffer is added for direct interface to an 8-, 12-, or 16-bit μ P bus.

The HADC574Z has standard bipolar and unipolar input ranges of 10V and 20V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

The HADC574Z is manufactured on Honeywell SPT's Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25°C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND)...0 to +16.5V
 Logic Supply Voltage (V_{LOGIC} to DGND)...0 to +7V
 Analog to Digital Ground (AGND to DGND)...-0.5 to +1V

Input Voltages

Control Input Voltages (to DGND)
 (CE, CS, Ao, 12/8, R/C)...-0.5 to $V_{LOGIC} + 0.5V$
 Analog Input Voltage (to AGND)... $\pm 16.5V$
 (REF IN, BIP OFF, 10Vin)
 20V Vin Input Voltage (to AGND)... $\pm 24V$

Output

Reference Output Voltage.....Indefinite short to GND
 Momentary short to V_{CC}

Temperature

Operating Temperature, ambient...-55 to +125(case) °C
 junction.....+175 °C
 Lead Temperature, (soldering 10 seconds).....+300 °C
 Storage Temperature.....-65 to +150 °C
 Power Dissipation.....1000mW
 Thermal Resistance (θ_{JA}).....48°C/W

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

COMMERCIAL TEMPERATURE RANGE: 0 TO +70°C

$T_A = 0$ to $70^\circ C$, $V_{CC} = +15V$ or $+12V$, $V_{LOGIC} = +5V$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HAD574ZCC		HAD574ZBC		HAD574ZAC		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	

DC ELECTRICAL CHARACTERISTICS

Resolution				12		12		12	BITS
Linearity Error		I		± 1		± 1 2		± 1 2	LSB
Differential Linearity Error		I		± 1		± 1 2		± 1 2	LSB
Unipolar Offset ; 10V, 20V	+25°C Adjustable to zero	I		± 0.1 ± 2		± 0.1 ± 2		± 0.1 ± 2	LSB
Bipolar Offset ¹ ; $\pm 5V$, $\pm 10V$	+25°C Adjustable to zero	I		± 10		± 4		± 4	LSB
Full Scale Calibration Error ¹ All Ranges	+25°C Adjustable to zero	I		0.3		0.3		0.3	% of FS
	No adjustment at +25°C	II		0.5		0.4		0.35	% of FS
	With adjustment at +25°C	II		0.22		0.12		0.05	% of FS
Temperature Coefficients	Using internal reference								
Unipolar Offset		I		± 0.2 ± 2 (10)		± 0.1 ± 1 (5)		± 0.1 ± 1 (5)	LSB (ppm/°C)
Bipolar Offset		I		± 0.2 ± 2 (10)		± 0.1 ± 1 (5)		± 0.1 ± 1 (5)	LSB (ppm/°C)
Full Scale Calibration		I		± 9 (45)		± 5 (25)		± 2 (10)	LSB (ppm/°C)

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

COMMERCIAL TEMPERATURE RANGE: 0 TO +70°C

T_A = 0 to 70°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

HADC574Z

2

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCC			HADC574ZBC			HADC574ZAC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS

Power Supply Rejection	Max change in full scale calibration											
+13.5V < V _{CC} < +16.5V or +11.4V < V _{CC} < +12.6V		I	±0.5	±2		±0.5	±1		±0.5	±1	LSB	
+4.5V < V _{LOGIC} < +5.5V		I	±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB	
Analog Inputs Ranges												
Bipolar		I	-5	+5	-5	+5	-5	+5	-5	+5	VOLTS	
			-10	+10	-10	+10	-10	+10	-10	+10	VOLTS	
Unipolar		I	0	+10	0	+10	0	+10	0	+10	VOLTS	
			0	+20	0	+20	0	+20	0	+20	VOLTS	
Input Impedance												
10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range												
V _{LOGIC}		I	+4.5	+5.5	+4.5	+5.5	+4.5	+5.5	+4.5	+5.5	VOLTS	
V _{CC}		I	+11.4	+16.5	+11.4	+16.5	+11.4	+16.5	+11.4	+16.5	VOLTS	
V _{EE}	Not required for circuit operation.											
Operating Current												
I _{LOGIC}		I	0.5	1	0.5	1	0.5	1	0.5	1	mA	
I _{CC}		I	7	9	7	9	7	9	7	9	mA	
I _{EE}	Not required for circuit operation.											
Power Dissipation												
+15V, +5V		I	110	150	110	150	110	150	110	150	mW	
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current ²		I		2		2		2		2	mA	

Note 2: Available for external loads, external load should not change during conversion. When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output.

COMMERCIAL TEMPERATURE RANGE: 0 TO +70°CT_A = 0 to 70°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCC			HADC574ZBC			HADC574ZAC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

DIGITAL CHARACTERISTICS

Logic Inputs (CE, \overline{CS} , R/C, A0, 12/8)												
Logic "1"		I	2.0	5.5	2.0	5.5	2.0	5.5			VOLTS	
Logic "0"		I	-0.5	+0.8			-0.5	+0.8			VOLTS	
Current	0 to 5.5V Input	I	±0.1	+1	±0.1	+1	±0.1	+1			μA	
Capacitance		II	5		5		5				pF	
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I _{SINK} = 1.6mA)	I		+0.4		+0.4		+0.4			VOLTS	
Logic "1"	(I _{SOURCE} = 500μA)	I	+2.4		+2.4		+2.4				VOLTS	
Leakage	(High Z State, DB11-DB0 Only)	I	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	μA
Capacitance		II	5		5		5				pF	

INDUSTRIAL TEMPERATURE RANGE -25 TO +85°C

$T_A = -25$ to 85°C , $V_{CC} = +15\text{V}$ or $+12\text{V}$, $V_{\text{LOGIC}} = +5\text{V}$, unless otherwise specified.

HADC574Z

2

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCI			HADC574ZBI			HADC574ZAI			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS

Resolution				12		12		12		12	BITS	
Linearity Error	25°C	I		±1		±1		±1		±1	LSB	
Linearity Error		I		±1		±1		±1		±1	LSB	
Differential Linearity Error		I		±1		±1		±1		±1	LSB	
Unipolar Offset; 10V, 20V	+25°C Adjustable to zero	I		±2		±2		±2		±2	LSB	
Bipolar Offset ¹ ; ±5V, ±10V	+25°C Adjustable to zero	I		±10		±4		±4		±4	LSB	
Full Scale Calibration Error ¹ All Ranges	+25°C Adjustable to zero	I		0.3		0.3		0.3		0.3	% of FS	
	No adjustment at +25°C T _{min} to T _{max}	II		0.7		0.5		0.4		0.4	% of FS	
	With adjustment at +25°C T _{min} to T _{max}	II		0.4		0.2		0.1		0.1	% of FS	
Temperature Coefficients	Using internal reference T _{min} to T _{max}											
Unipolar Offset		I		±2 (5)		±1 (2.5)		±1 (2.5)		±1 (2.5)	LSB (ppm/°C)	
Bipolar Offset		I		±2 (5)		±1 (2.5)		±1 (2.5)		±1 (2.5)	LSB (ppm/°C)	
Full Scale Calibration		I		±12 (50)		±7 (25)		±3 (12)		±3 (12)	LSB (ppm/°C)	
Power Supply Rejection	Max change in full scale calibration											
+13.5V < V _{CC} < +16.5V or +11.4V < V _{CC} < +12.6V		I		±0.5 ±2		±0.5 ±1		±0.5 ±1		±0.5 ±1	LSB	
+4.5V < V _{LOGIC} < +5.5V		I		±0.1 ±0.5		±0.1 ±0.5		±0.1 ±0.5		±0.1 ±0.5	LSB	
Analog Inputs Input Ranges												
Bipolar		I	-5	+5	-5	+5	-5	+5	-5	+5	VOLTS	
		I	-10	+10	-10	+10	-10	+10	-10	+10	VOLTS	
Unipolar		I	0	+10	0	+10	0	+10	0	+10	VOLTS	
		I	0	+20	0	+20	0	+20	0	+20	VOLTS	
Input Impedance 10 Volt Span 20 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ kΩ
		I	15	20	25	15	20	25	15	20	25	kΩ kΩ

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

INDUSTRIAL TEMPERATURE RANGE -25 TO +85°C

$T_A = -25$ to 85°C , $V_{CC} = +15\text{V}$ or $+12\text{V}$, $V_{\text{LOGIC}} = +5\text{V}$, unless otherwise specified.

HADC574Z

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCI		HADC574ZBI		HADC574ZAI		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	

DC ELECTRICAL CHARACTERISTICS

Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5	+5.5	+4.5	+5.5	+4.5	+5.5	VOLTS
V_{CC}		I	+11.4	+16.5	+11.4	+16.5	+11.4	+16.5	VOLTS
V_{EE}	Not required for circuit operation.								
Operating Current I_{LOGIC}		I	0.5	1	0.5	1	0.5	1	mA
I_{CC}		I	7	9	7	9	7	9	mA
I_{EE}	Not required for circuit operation.								
Power Dissipation $\pm 15\text{V}$, $+5\text{V}$		I	110	150	110	150	110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current ²		I		2		2		2	mA

DIGITAL CHARACTERISTICS

Logic Inputs (CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A0,12/8)									
Logic "1"		I	2.0	5.5	2.0	5.5	2.0	5.5	VOLTS
Logic "0"		I	-0.5	+0.8	-0.5	+0.8	-0.5	+0.8	VOLTS
Current	0 to +5.5V Input	I	± 0.1	+5	± 0.1	+5	± 0.1	+5	μA
Capacitance		II	5		5		5		pF
Logic Outputs (DB11-DB0, STS)									
Logic "0"	($I_{\text{SINK}} = 1.6\text{mA}$)	I		+0.4		+0.4		+0.4	VOLTS
Logic "1"	($I_{\text{SOURCE}} = 500\mu\text{A}$)	I	+2.4		+2.4		+2.4		VOLTS
Leakage	(High Z State, DB11- DB0 Only)		-5	± 0.1	+5	-5	± 0.1	+5	μA
Capacitance		II	5		5		5		pF

Note 2 Available for external loads, external load should not change during conversion.

When supplying an external load and operating on +12V supplies, a buffer amplifier must be provided for the reference output.

MILITARY TEMPERATURE RANGE -55 TO +125°C

$T_A = -55$ to 125°C , $V_{CC} = +15\text{V}$ or $+12\text{V}$, $V_{\text{LOGIC}} = +5\text{V}$, unless otherwise specified.

HAD574Z

2

PARAMETER	TEST CONDITIONS	TEST LEVEL	HAD574ZCM			HAD574ZBM			HAD574ZAM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS

Resolution			12			12			12			BITS
Linearity Error	25°C	I	± 1			± 1 2			± 1 2			LSB
Linearity Error		I	± 1			± 1			± 1			LSB
Differential Linearity Error		I	± 1			± 1 2			± 1 2			LSB
Unipolar Offset; 10V, 20V	25°C Adjustable to zero	I	± 2			± 2			± 2			LSB
Bipolar Offset ¹ ; $\pm 5\text{V}$, $\pm 10\text{V}$	25°C Adjustable to zero	I	± 10			± 4			± 4			LSB
Full Scale Calibration Error ¹ All Ranges	25°C Adjustable to zero	I	0.3			0.3			0.3			% of FS
	No adjustment at +25°C Tmin to Tmax	II	0.8			0.6			0.4			% of FS
	With adjustment at +25°C Tmin to Tmax	II	0.5			0.25			0.12			% of FS
Temperature Coefficients	Using internal reference Tmin to Tmax											
Unipolar Offset		I	± 2 (5)			± 1 (2.5)			± 1 (2.5)			LSB (ppm/°C)
Bipolar Offset		I	± 4 (10)			± 2 (5)			± 1 (2.5)			LSB (ppm/°C)
Full Scale Calibration		I	± 20 (50)			± 10 (25)			± 5 (12.5)			LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5V < Vcc < +16.5V or +11.4V < Vcc < +12.6V		I	± 0.5 ± 2			± 0.5 ± 1			± 0.5 ± 1			LSB
+4.5V < V _{LOGIC} < +5.5V		I	± 0.1 ± 0.5			± 0.1 ± 0.5			± 0.1 ± 0.5			LSB
Analog Inputs Input Ranges			-5	+5	-5	+5	-5	+5	-5	+5	VOLTS	
Bipolar		I	-10	+10	-10	+10	-10	+10	-10	+10	VOLTS	
Unipolar		I	0	+10	0	+10	0	+10	0	+10	VOLTS	
		I	0	+20	0	+20	0	+20	0	+20	VOLTS	
Input Impedance 10 Volt Span 20 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
		I	15	20	25	15	20	25	15	20	25	kΩ

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

MILITARY TEMPERATURE RANGE -55 TO +125°C

$T_A = -55$ to 125°C , $V_{CC} = +15\text{V}$ or $+12\text{V}$, $V_{\text{LOGIC}} = +5\text{V}$, unless otherwise specified.

HADC574Z

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZCM			HADC574ZBM			HADC574ZAM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS

Power Supplies Operating Voltage Range V_{LOGIC}		I	+4.5	+5.5	+4.5	+5.5	+4.5	+5.5	VOLTS
V_{CC}		I	+11.4	+16.5	+11.4	+16.5	+11.4	+16.5	VOLTS
V_{EE}	Not required for circuit operation.								
Operating Current I_{LOGIC}		I	0.5	1	0.5	1	0.5	1	mA
I_{CC}		I	7	9	7	9	7	9	mA
I_{EE}	Not required for circuit operation.								
Power Dissipation $\pm 15\text{V}$, $+5\text{V}$		I	110	150	110	150	110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current ²		I		2		2		2	mA

DIGITAL CHARACTERISTICS

Logic Inputs (CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A0,12/ $\overline{\text{B}}$)									
Logic "1"		I	2.0	5.5	2.0	5.5	2.0	5.5	VOLTS
Logic "0"		I	-0.5	+0.8	-0.5	+0.8	-0.5	+0.8	VOLTS
Current	0 to +5.5V Input	I	± 0.1	+1	± 0.1	+1	± 0.1	+1	μA
Capacitance		II	5		5		5		pF
Logic Outputs (DB11-DB0, STS)									
Logic "0"	($I_{\text{Sink}} = 1.6\text{mA}$)	I		+0.4		+0.4		+0.4	VOLTS
Logic "1"	($I_{\text{SOURCE}} = 500\mu\text{A}$)	I	+2.4		+2.4		+2.4		VOLTS
Leakage	(High Z State, DB11- DB0 Only)		-5	± 0.1	+5	-5	± 0.1	+5	μA
Capacitance		II	5		5		5		pF

Note 2 Available for external loads, external load should not change during conversion.
When supplying an external load and operating on +12V supplies, a buffer amplifier must be provided for the reference output.

CONVERT MODE TIMING CHARACTERISTICS

Typical @ 25°C, $V_{CC} = +15V$ or $+12V$, $V_{LOGIC} = +5V$, unless otherwise specified.

HADC574Z

2

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC574ZC			HADC574ZB			HADC574ZA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

AC ELECTRICAL CHARACTERISTICS

t_{DSC} STS Delay from CE		I	200			200			200			ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} CS to CE Setup		I	50			50			50			ns
t_{HSC} \overline{CS} Low during CE High		I	50			50			50			ns
t_{SRC} $\overline{R/C}$ to CE Setup		I	50			50			50			ns
t_{HRC} $\overline{R/C}$ Low During CE High		I	50			50			50			ns
t_{SAC} A0 to CE Setup		I	0			0			0			ns
t_{HAC} A0 Valid During CE High		I	50			50			50			ns
t_C Conversion Time 12-Bit Cycle	Tmin to Tmax	I	13	18	25	15	18	25	15	18	25	μs
	8-Bit Cycle	I	10	13	19	10	13	17	10	13	17	μs

Note 5: Time is measured from 50% level of digital transitions. Tested with a 100pF and 3k Ω load for high impedance to drive and tested with 10pF and 3k Ω load for drive to high impedance.

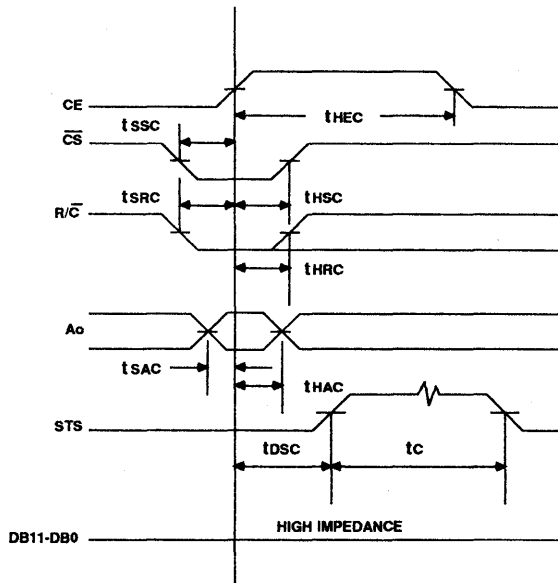


Figure 1 - Convert Mode Timing Diagram

READ MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC574ZC			HADC574ZB			HADC574ZA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC574ZC			HADC574ZB			HADC574ZA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{DD} Access Time from CE		I			150			150			150	ns
t _{HD} Data Valid After CE Low		I	25			25			25			ns
t _{HL} Output Float Delay		I			150			150			150	ns
t _{SSR} CS to CE Setup		I	50	0		50	0		50	0		ns
t _{SRR} R/C to CE Setup		I	0	0		0	0		0	0		ns
t _{SAR} A0 to CE Setup		I	50			50			50			ns
t _{HSR} CS Valid After CE Low		I	0	0		0	0		0	0		ns
t _{HRR} R/C High After CE Low		I	0	0		0	0		0	0		ns
t _{HAR} A0 Valid After CE Low		I	50			50			50			ns
t _{HS} STS Delay After Data Valid		I	300	1000		300	1000		300	1000		ns

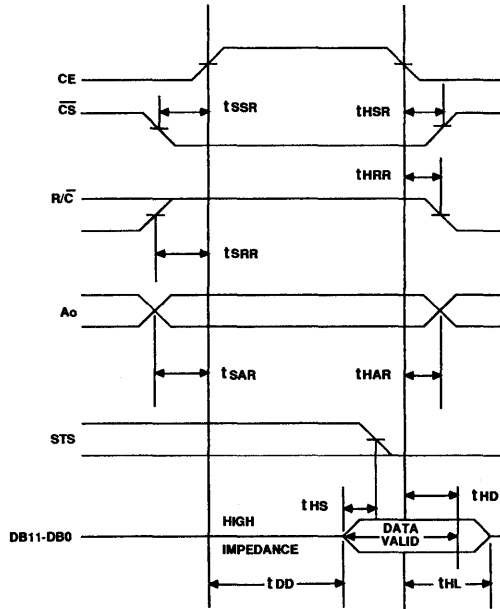


Figure 2 - Read Mode Timing Diagram

STAND-ALONE MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, Unless otherwise specified.

HADC574Z

2

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC574ZC			HADC574ZB			HADC574ZA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

AC ELECTRICAL CHARACTERISTICS

t _{HRL}	Low R/C Pulse Width	I	50			50			50			ns
t _{DS}	STS Delay from R/C	I			200			200			200	ns
t _{HDR}	Data Valid After R/C Low	I	25			25			25			ns
t _{HS}	STS Delay After Data Valid	I	300	1000		300	1000		300	1000		ns
t _{HRH}	High R/C Pulse Width	I	150			150			150			ns
t _{DDR}	Data Access Time	I			150			150			150	ns

SAMPLE AND HOLD

Acquisition Time		II	1.8	2.4	3.0	1.8	2.4	3.0	1.8	2.4	3.0	μs
Aperture Uncertainty Time		II			8			8			8	ns

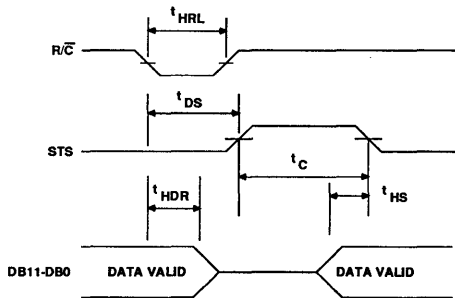


Figure 3 - Low Pulse For R/C - Outputs Enabled After Conversion

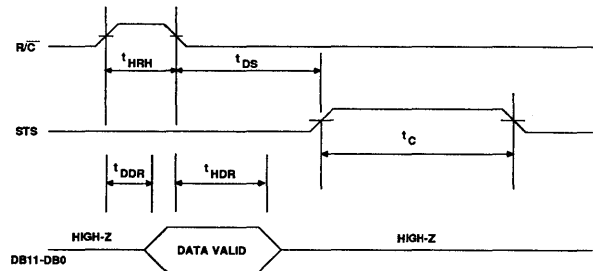


Figure 4 - High Pulse For R/C - Outputs Enabled While R/C is High, Otherwise High Impedance

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore T_{junc} = T_{case} = T_{ambient}.

TEST LEVEL

TEST PROCEDURE

I

Production tested at the specified conditions.

II

Parameter is guaranteed by design and sampled characterization data.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 7). The point used as "zero" occurs $1/2\text{LSB}$ (1.22mV for a 10 Volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and $1/2\text{LSB}$ beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC574ZAC and Bc grades are guaranteed for maximum nonlinearity of $\pm 1/2\text{LSB}$. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC574AM, BM, CC and CM grades are guaranteed to $\pm 1\text{LSB}$ maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC574Z type BC, AC, BM, and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC574Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 7 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC574Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1LSB . Figure 7 points out two missed codes in the transfer function.

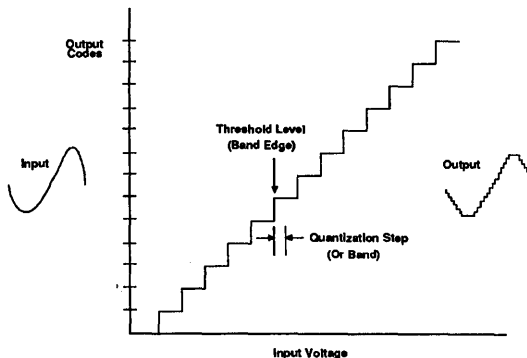


Figure 5 - Static Input Conditions

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm 1/2\text{LSB}$. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = \text{FSR}/2^N$ where FSR = full scale range and $N = 12$. Non-ideal quantization bands represent differential nonlinearity errors (See Figures 5, 6 and 7).

RESOLUTION - ACTUAL VS. AVAILABLE

The available resolution of an N-bit converter is 2^N . This means it is theoretically possible to generate 2^N unique output codes.

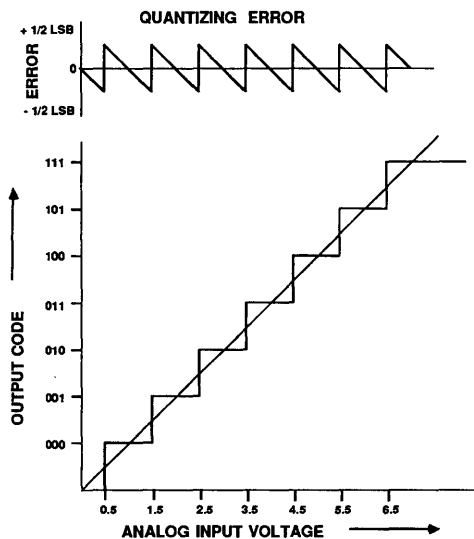


Figure 6 - Quantizing error

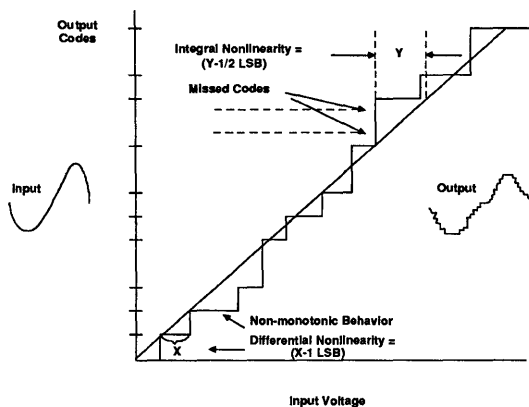


Figure 7 - Dynamic Conditions

THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rated performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC574Z, this is the time delay between the R/C falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level $1/2\text{LSB}$ above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 to 1000 0000 0000) should occur for an analog value $1/2\text{LSB}$ below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC574Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max} .

POWER SUPPLY REJECTION

The standard specifications for the HADC574Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC574Z is left-justified. This means that the data represents the analog input as a fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 7 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC574Z is a complete 12-bit Analog-To-Digital converter which consists of a single chip version of the industry standard 574. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample & hold, clock, output buffers and control circuitry to make it possible to use the HADC574Z with few external components.

When the control section of the HADC574Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC574Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within $\pm 1/2$ LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts $\pm 1\%$ and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with $\pm 15V$ supplies. If the HADC574Z is used with $\pm 12V$ supplies, or if external current must be supplied over the full temperature range, an

external buffer amplifier is recommended. Any external load on the HADC574Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC574Z appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the HADC574Z over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC574Z is disconnected from the user's sample and hold. This prevents transients occurring during conversion from being inflicted upon the attached sample and hold buffer. All other 574 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the HADC574Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC574Z acts as any other 574 device because the internal S/H is transparent. The sample/hold function in the HADC574Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HADC574Z and is controlled through the normal R/C control line (refer to Figure 8.) When the R/C line makes a negative transition, the HADC574Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with

the duration controlled by the internal clock cycle.

During T_{acq} , the equivalent circuit of the HADC574Z input is as shown in Figure 9 (the time constant of the input is independent of which input level is used.) This CDAC capacitance must be charged up to the input voltage during T_{acq} . Since the CDAC time constant is 100 nsecs., there is more than enough time for settling the input to 12 bits of accuracy during T_{acq} . The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Note that because the sample is taken relative to the R/C transition, T_{acq} is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in $T_{acq} = 2.4 \mu\text{secs} \pm 0.6 \mu\text{secs}$. between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC574Z.

APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time the actual sample is taken - i.e. the "aperture jitter" or T_{AJ} . The HADC574Z has a nominal aperture jitter of 8 nsecs. between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (See Figure 10). The magnitude of this change for a sine-wave can be calculated:

Assume a sinusoidal signal, maximum slew rate, $Sr = 2\pi f V_p$ (V_p = peak voltage, f = frequency of sine wave)
For an N-bit converter to maintain +/- 1/2 LSB accuracy :

$V_{err} \leq V_{fs}/2^{N+1}$ (where V_{err} is the allowable error voltage and V_{fs} is the full scale voltage)

From Figure 10:

$$Sr = \Delta V / \Delta T = 2\pi f V_p$$

Let $\Delta V = V_{err} = V_{fs} / 2^{(N+1)}$, $V_p = V_{in}/2$ and $\Delta T = t_{AJ}$ (the time during which unwanted voltage change occurs)

The above conditions then yield:

$$Vfs/2^{N+1} \geq \pi f_{in} t_{AJ} \text{ or } f_{max} \leq Vfs/(\pi V_{in} t_{AJ}) 2^{N+1}$$

For the HADC574Z, $T_{AJ} = 8 \text{ nsec}$,
therefore $f_{max} \leq 5 \text{ KHz}$.

For higher frequency signal inputs, an external sample and hold is recommended.

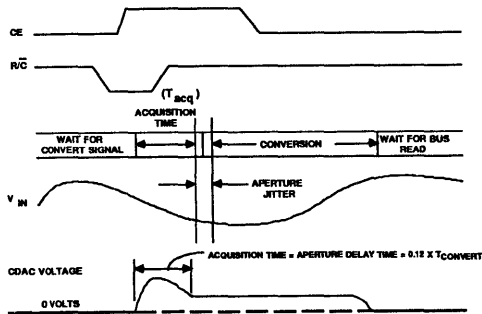


Figure 8 - Sample and Hold Function

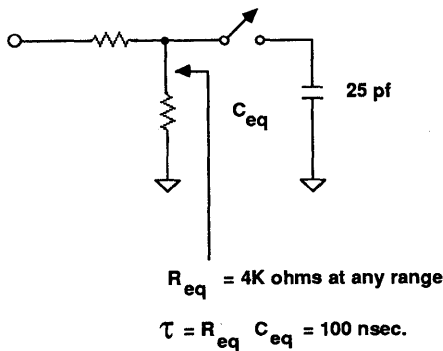


Figure 9 - Equivalent HADC574Z Input Circuit

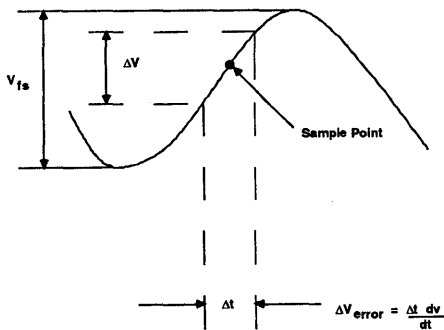


Figure 10 - Aperture Uncertainty

TYPICAL INTERFACE CIRCUIT

The HADC574Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figures 11 and 12. The two typical interface circuits are for operating the HADC574Z in either a unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the P.C. board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC574Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A $10\mu\text{F}$ tantalum and a $0.1\mu\text{F}$ ceramic type in parallel between V_{LOGIC} (pin1) and digital common (pin15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC574Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6mADC while the digital ground is 3mADC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependant currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC574Z may be operated by a μP or in the stand-alone mode. The part has four standard input ranges: 0V to +10V, 0V to +20V, $\pm 5\text{V}$ and $\pm 10\text{V}$. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of $+1/2\text{LSB}$ or $+1.22\text{mV}$ for the 10V range and $+2.44\text{mV}$ for the 20V range should be applied to the HADC574Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and $1/2\text{LSB}$ below the nominal full scale which is $+9.9963\text{V}$ for the 10V range and $+19.9927\text{V}$ for the 20V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R1 with a 50Ω , 1% metal film resistor and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

BIPOLAR

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R1

and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50Ω , 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a $\pm 5\text{V}$ range or to pin 14 for a $\pm 10\text{V}$ range. First apply a DC input voltage $1/2\text{LSB}$ above negative full scale which is -4.9988V for the $\pm 5\text{V}$ range or -9.9976V for the $\pm 10\text{V}$ range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and $1/2\text{LSB}$ below positive full scale which is $+4.9963\text{V}$ for the $\pm 5\text{V}$ range or $+9.9927\text{V}$ for the $\pm 10\text{V}$ range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

The 100Ω potentiometer R2 provides gain adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (for an LSB of 2.5mV) or 20.48V (for an LSB of 5.0mV) is more convenient. For these, replace R2 by a 50Ω , 1% metal film resistor. Then to provide gain adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 1000Ω potentiometer in series with pin 14.

CONTROLLING THE HADC574Z

The HADC574Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/C input pin. Full μP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/8, CS, A0, R/C and CE). The use of these inputs in controlling the converter's operations is shown in Table 1, and the internal control logic is shown in a simplified schematic in Figure 13.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/C. The other controls must be tied to known states as follows: CE and 12/8 are wired high, A0 and CS are wired low. The output data arrives in words of 12-bits each. The limits on R/C duty cycle are shown in Figures 3 and 4. It may have duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress.

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table 1. The latched state determines if the conversion stops with 8-bits (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

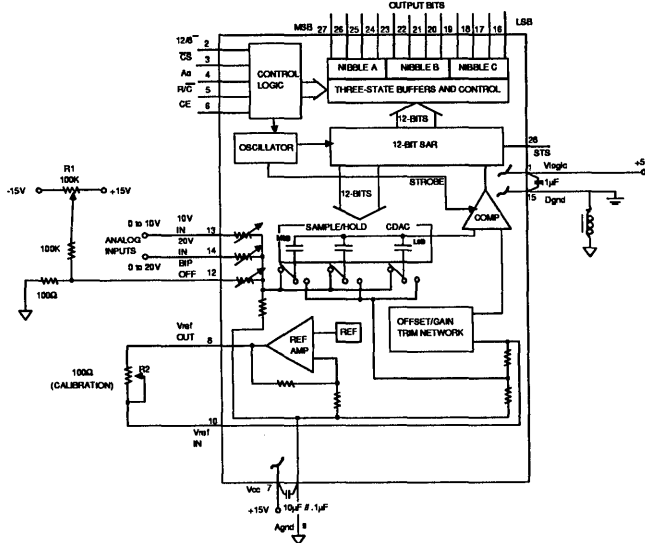


Figure 11 - Unipolar Input Connections

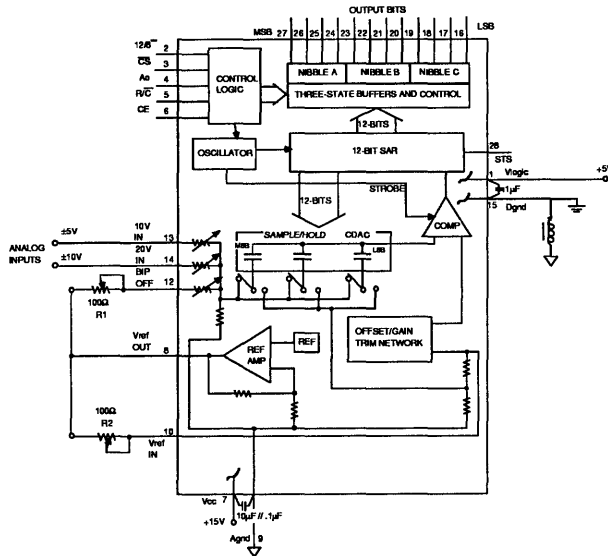


Figure 12 - Bipolar Input Connections

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, \overline{CS} , R/\overline{C} , as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new state of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

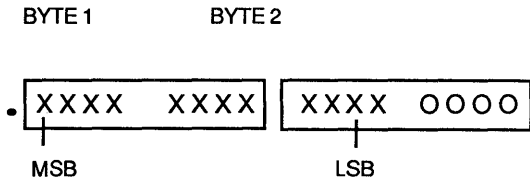
READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/\overline{C} is high, STS is low, CE is high and \overline{CS} is low. The data lines become active in response to the four conditions and output data according to the conditions of $12/\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When $12/\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The $12/\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible.

Table 1 - Truth Table for the HADC574Z Control Inputs

CE	\overline{CS}	R/\overline{C}	$12/\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

When $12/\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.

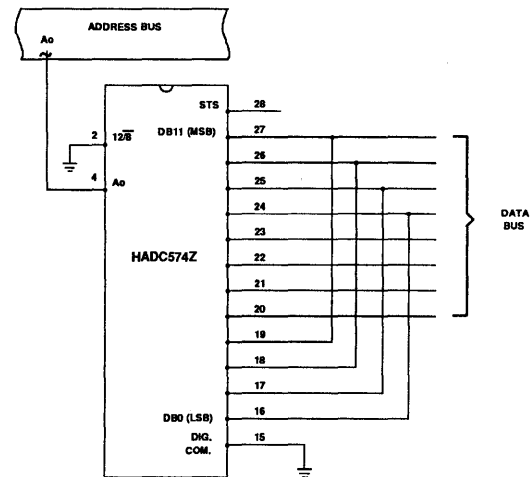


Figure 13 - Interfacing the HADC574Z to an 8-bit Data Bus

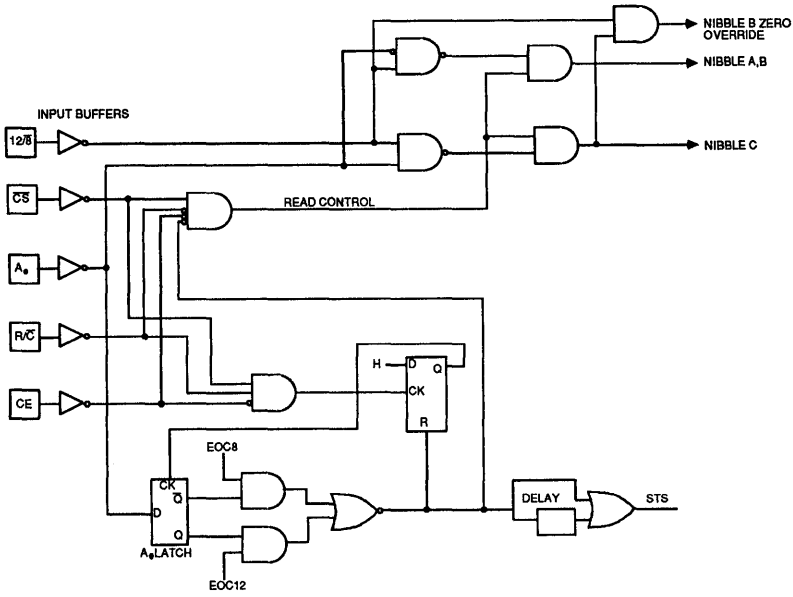


Figure 14 - HADC574Z Control Logic

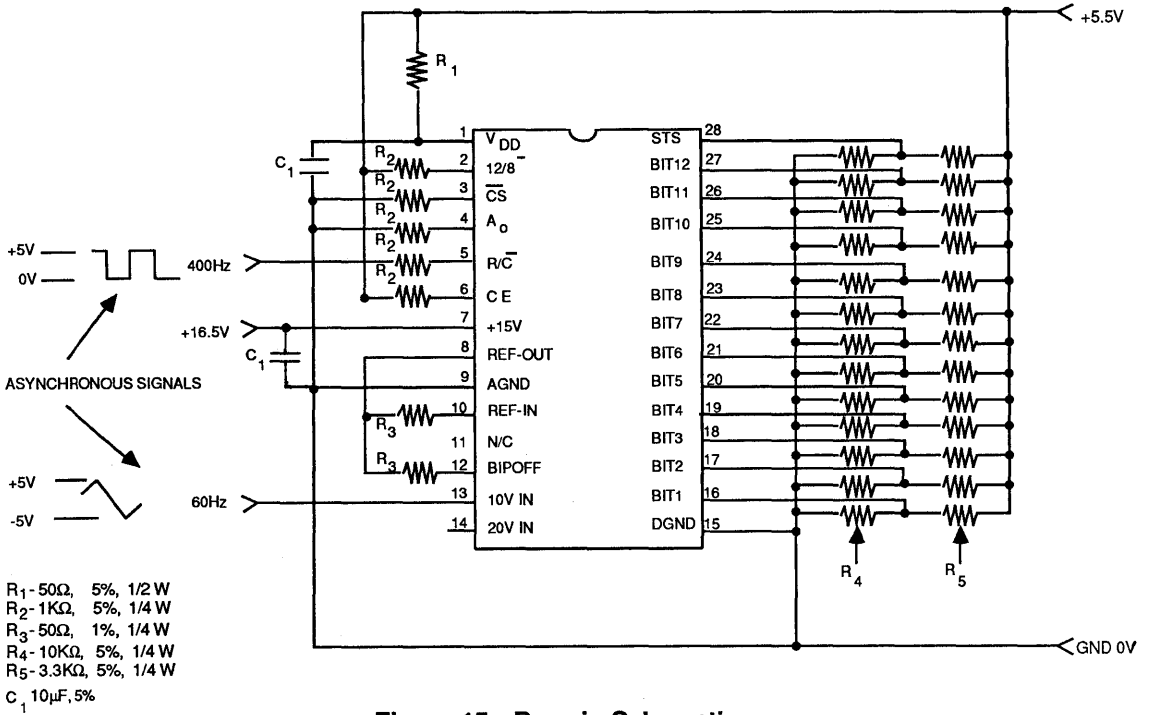
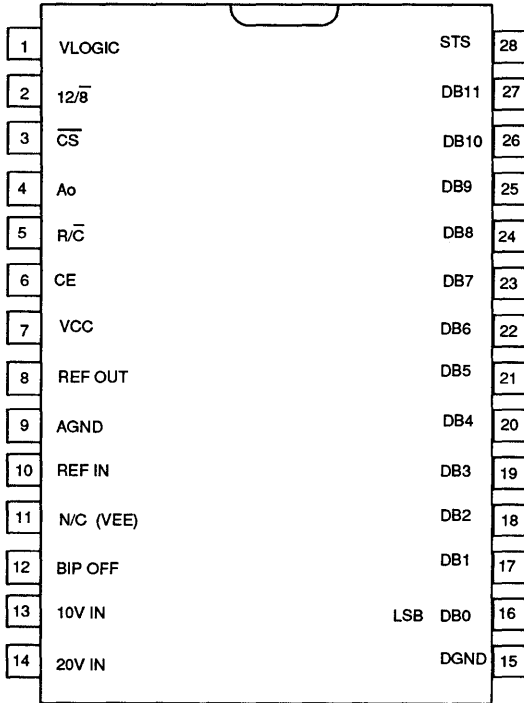


Figure 15 - Burn-in Schematic

PIN ASSIGNMENT HADC574Z

TOP VIEW



28 LEAD DIP

PIN FUNCTIONS HADC574Z

NAME	FUNCTION
V _{LOGIC}	Logic Supply Voltage, Nominally +5V
12/8	Data Mode Select
CS	Chip Select
A ₀	Byte Address/ Short cycle
R/C	Read/ Convert
CE	Chip Enable
V _{CC}	Analog Positive Supply Voltage Nominally +15V
REF OUT	Reference Output Nominally +10V
AGND	Analog Ground
REF IN	Reference Input
N/C (VEE)	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10V IN	10 Volt Analog Input
20V IN	20V Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

HADC574Z

2

**For Ordering Information See Section 1.

NOTES:

**FAST, COMPLETE 12-BIT μ P COMPATIBLE
A/D CONVERTER WITH SAMPLE/HOLD**

FEATURES:

- IMPROVED PIN-TO-PIN COMPATIBLE MONOLITHIC VERSION OF THE HI574A AND AD674A
- Complete 12-bit A/D Converter with Sample-Hold, Reference and Clock
- Low Power Dissipation (150mW Max)
- 12-bit Linearity (over temp)
- 15 μ s Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS:

- MILITARY/INDUSTRIAL DATA ACQUISITION SYSTEMS
- 8 OR 12-bit μ P Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC674Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI674A and AD674A. Included on chip is an internal reference, clock, and a sample and hold. The S/H is an additional feature not available on similar devices.

The HADC674Z features 15 μ s (Max) conversion time of 10 or 20 Volt input signals. Also, a 3-state output buffer is added for direct interface to an 8-, 12-, or 16-bit μ P bus.

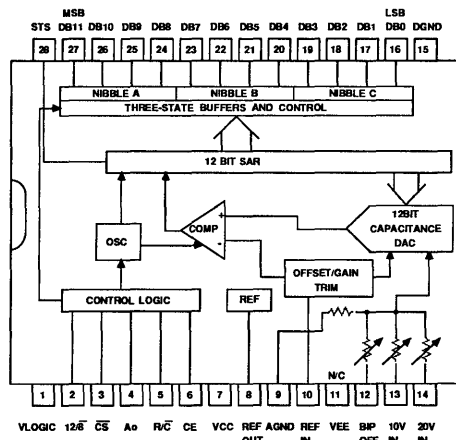
The HADC674Z is manufactured on Honeywell SPT's Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

The BEMOS process and monolithic construction reduces power consumption, ground noise, and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC674Z has standard bipolar and unipolar input ranges of 10V and 20V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25°C**Supply Voltages**

Positive Supply Voltage (V_{CC} to DGND)...0 to +16.5V
 Logic Supply Voltage (V_{LOGIC} to DGND).....0 to +7V
 Analog to Digital Ground (AGND to DGND)...-0.5 to +1V

Input Voltages

Control Input Voltages (to DGND).
 (CE, CS, Ao, 12/8, R/C).....-0.5 to V_{LOGIC} +0.5V
 Analog Input Voltage (to AGND)..... $\pm 16.5V$
 (REF IN, BIP OFF, 10Vin)
 20V Vin Input Voltage (to AGND)..... $\pm 24V$

Output

Reference Output Voltage.....Indefinite short to GND
 Momentary short to V_{CC}

Temperature

Operating Temperature, ambient.-55 to +125(case) °C
 junction.....+175 °C
 Lead Temperature, (soldering 10 seconds).....+300 °C
 Storage Temperature.....-65 to +150 °C
 Power Dissipation.....1000mW
 Thermal Resistance (θ_{JA}).....48°C/W

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

COMMERCIAL TEMPERATURE RANGE: 0 TO +70°C

$T_A = 0$ to 70°C, $V_{CC} = +15V$ or +12V, $V_{LOGIC} = +5V$, Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HAD674ZCC		HAD674ZBC		HAD674ZAC		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	

DC ELECTRICAL CHARACTERISTICS

Resolution				12		12		12	BITS
Linearity Error		I		± 1		± 1 2		± 1 2	LSB
Differential Linearity Error		I		± 1		± 1 2		± 1 2	LSB
Unipolar Offset ; 10V, 20V	+25°C Adjustable to zero	I		± 0.1 ± 2		± 0.1 ± 2		± 0.1 ± 2	LSB
Bipolar Offset ¹ ; $\pm 5V$, $\pm 10V$	+25°C Adjustable to zero	I		± 10		± 4		± 4	LSB
Full Scale Calibration Error ¹ All Ranges	+25°C Adjustable to zero	I		0.3		0.3		0.3	% of FS
	No adjustment at +25°C	II		0.5		0.4		0.35	% of FS
	With adjustment at +25°C	II		0.22		0.12		0.05	% of FS
Temperature Coefficients	Using internal reference								
Unipolar Offset		I		± 0.2 ± 2 (10)		± 0.1 ± 1 (5)		± 0.1 ± 1 (5)	LSB (ppm/°C)
Bipolar Offset		I		± 0.2 ± 2 (10)		± 0.1 ± 1 (5)		± 0.1 ± 1 (5)	LSB (ppm/°C)
Full Scale Calibration		I		± 9 (45)		± 5 (25)		± 2 (10)	LSB (ppm/°C)

Note 1: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

COMMERCIAL TEMPERATURE RANGE: 0 TO +70°C

$T_A = 0$ to 70°C , $V_{CC} = +15\text{V}$ or $+12\text{V}$, $V_{\text{LOGIC}} = +5\text{V}$, Unless otherwise specified.

HADC674Z

2

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCC			HADC674ZBC			HADC674ZAC			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS

Power Supply Rejection	Max change in full scale calibration											
$+13.5\text{V} < V_{CC} < +16.5\text{V}$ or $+11.4\text{V} < V_{CC} < +12.6\text{V}$		I	± 0.5	± 2	± 0.5	± 1	± 0.5	± 1	± 0.5	± 1	LSB	
$+4.5\text{V} < V_{\text{LOGIC}} < +5.5\text{V}$		I	± 0.1	± 0.5	± 0.1	± 0.5	± 0.1	± 0.5	± 0.1	± 0.5	LSB	
Analog Inputs Ranges												
Bipolar		I	-5	+5	-5	+5	-5	+5	-5	+5	VOLTS	
			-10	+10	-10	+10	-10	+10	-10	+10	VOLTS	
Unipolar		I	0	+10	0	+10	0	+10	0	+10	VOLTS	
			0	+20	0	+20	0	+20	0	+20	VOLTS	
Input Impedance												
10 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	k Ω
20 Volt Span			15	20	25	15	20	25	15	20	25	k Ω
Power Supplies												
Operating Voltage Range												
V_{LOGIC}		I	+4.5	+5.5	+4.5	+5.5	+4.5	+5.5	+4.5	+5.5	VOLTS	
V_{CC}		I	+11.4	+16.5	+11.4	+16.5	+11.4	+16.5	+11.4	+16.5	VOLTS	
V_{EE}	Not required for circuit operation.											
Operating Current												
I_{LOGIC}		I	0.5	1	0.5	1	0.5	1	0.5	1	mA	
I_{CC}		I	7	9	7	9	7	9	7	9	mA	
I_{EE}	Not required for circuit operation.											
Power Dissipation												
+15V, +5V		I	110	150	110	150	110	150	110	150	mW	
Internal Reference Voltage												
		I	9.9	10	10.1	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current ²		I		2		2		2		2	mA	

Note 2: Available for external loads, external load should not change during conversion.

When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output.

COMMERCIAL TEMPERATURE RANGE: 0 TO +70°C

$T_A = 0$ to 70°C , $V_{CC} = +15\text{V}$ or $+12\text{V}$, $V_{\text{LOGIC}} = +5\text{V}$, unless otherwise specified.

HADC674Z

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCC		HADC674ZBC		HADC674ZAC		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	

DIGITAL CHARACTERISTICS

Logic Inputs (CE, $\overline{\text{CS}}$, R/ $\overline{\text{C}}$, A0,12/ $\overline{\text{B}}$)									
Logic "1"		I	2.0	5.5	2.0	5.5	2.0	5.5	VOLTS
Logic "0"		I	-0.5	+0.8	-0.5	+0.8	-0.5	+0.8	VOLTS
Current	0 to 5.5V Input	I	± 0.1	+5	± 0.1	+5	± 0.1	+5	μA
Capacitance		II	5		5		5		pF
Logic Outputs (DB11-DB0, STS)									
Logic "0"	($I_{\text{Sink}} = 1.6\text{mA}$)	I		+0.4		+0.4		+0.4	VOLTS
Logic "1"	($I_{\text{Source}} = 500\mu\text{A}$)	I	+2.4		+2.4		+2.4		VOLTS
Leakage	(High Z State, DB11- DB0 Only)	I	-5	± 0.1	+5	-5	± 0.1	+5	μA
Capacitance		II	5		5		5		pF

INDUSTRIAL TEMPERATURE RANGE -25 TO +85°C

$T_A = -25$ to 85°C , $V_{CC} = +15\text{V}$ or $+12\text{V}$, $V_{\text{LOGIC}} = +5\text{V}$, unless otherwise specified.

HADC674Z

2

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCI			HADC674ZBI			HADC674ZAI			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS

Resolution			12			12			12			BITS
Linearity Error	25°C	I	± 1			± 1 2			± 1 2			LSB
Linearity Error		I	± 1			± 1 2			± 1 2			LSB
Differential Linearity Error		I	± 1			± 1 2			± 1 2			LSB
Unipolar Offset; 10V, 20V	+25°C Adjustable to zero	I	± 2			± 2			± 2			LSB
Bipolar Offset ¹ ; $\pm 5\text{V}$, $\pm 10\text{V}$	+25°C Adjustable to zero	I	± 10			± 4			± 4			LSB
Full Scale Calibration Error ¹ All Ranges	+25°C Adjustable to zero	I	0.3			0.3			0.3			% of FS
	No adjustment at +25°C Tmin to Tmax	II	0.7			0.5			0.4			% of FS
	With adjustment at +25°C Tmin to Tmax	II	0.4			0.2			0.1			% of FS
Temperature Coefficients	Using internal reference Tmin to Tmax											
Unipolar Offset		I	± 2 (5)			± 1 (2.5)			± 1 (2.5)			LSB (ppm/°C)
Bipolar Offset		I	± 2 (5)			± 1 (2.5)			± 1 (2.5)			LSB (ppm/°C)
Full Scale Calibration		I	± 12 (50)			± 7 (25)			± 3 (12)			LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5V < V _{CC} < +16.5V or +11.4V < V _{CC} < +12.6V		I	± 0.5 ± 2			± 0.5 ± 1			± 0.5 ± 1			LSB
+4.5V < V _{LOGIC} < +5.5V		I	± 0.1 ± 0.5			± 0.1 ± 0.5			± 0.1 ± 0.5			LSB
Analog Inputs Input Ranges												
Bipolar		I	-5	+5	-5	+5	-5	+5	-5	+5	VOLTS	
Unipolar		I	0	+10	0	+10	0	+10	0	+10	VOLTS	
		I	0	+20	0	+20	0	+20	0	+20	VOLTS	
Input Impedance 10 Volt Span 20 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
		I	15	20	25	15	20	25	15	20	25	kΩ

Note 1: Fixed 50Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

INDUSTRIAL TEMPERATURE RANGE -25 TO +85°CT_A = -25 to 85°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCI		HADC674ZBI		HADC674ZAI		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	

DC ELECTRICAL CHARACTERISTICS

Power Supplies Operating Voltage Range V _{LOGIC}		I	+4.5	+5.5	+4.5	+5.5	+4.5	+5.5	VOLTS
V _{CC}		I	+11.4	+16.5	+11.4	+16.5	+11.4	+16.5	VOLTS
V _{EE}	Not required for circuit operation.								VOLTS
Operating Current I _{LOGIC}		I	0.5	1	0.5	1	0.5	1	mA
I _{CC}		I	7	9	7	9	7	9	mA
I _{EE}	Not required for circuit operation.								
Power Dissipation ±15V, +5V		I	110	150	110	150	110	150	mW
Internal Reference Voltage		I	9.9	10	10.1	9.9	10	10.1	VOLTS
Output Current ²		I		2		2		2	mA

DIGITAL CHARACTERISTICS

Logic Inputs (CE, \overline{CS} , R/C, A0,12/8)									
Logic "1"		I	2.0	5.5	2.0	5.5	2.0	5.5	VOLTS
Logic "0"		I	-0.5	+0.8	-0.5	+0.8	-0.5	+0.8	VOLTS
Current	0 to +5.5V Input	I	±0.1	+5	±0.1	+5	±0.1	+5	μA
Capacitance		II	5		5		5		pF
Logic Outputs (DB11-DB0, STS)									
Logic "0"	(I _{SINK} = 1.6mA)	I		+0.4		+0.4		+0.4	VOLTS
Logic "1"	(I _{SOURCE} = 500μA)	I	+2.4		+2.4		+2.4		VOLTS
Leakage	(High Z State, DB11-DB0 Only)		-5	±0.1	+5	-5	±0.1	+5	μA
Capacitance		II	5		5		5		pF

Note 2 Available for external loads, external load should not change during conversion.

When supplying an external load and operating on +12V supplies, a buffer amplifier must be provided for the reference output.

MILITARY TEMPERATURE RANGE -55 TO +125°C

$T_A = -55$ to 125°C , $V_{CC} = +15\text{V}$ or $+12\text{V}$, $V_{\text{LOGIC}} = +5\text{V}$, unless otherwise specified.

HADC674Z

2

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCM			HADC674ZBM			HADC674ZAM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS

Resolution			12			12			12			BITS
Linearity Error	25°C	I	± 1			± 1 2			± 1 2			LSB
Linearity Error		I	± 1			± 1			± 1			LSB
Differential Linearity Error		I	± 1			± 1 2			± 1 2			LSB
Unipolar Offset; 10V, 20V	25°C Adjustable to zero	I	± 2			± 2			± 2			LSB
Bipolar Offset ¹ ; $\pm 5\text{V}$, $\pm 10\text{V}$	25°C Adjustable to zero	I	± 10			± 4			± 4			LSB
Full Scale Calibration Error ¹ All Ranges	25°C Adjustable to zero	I	0.3			0.3			0.3			% of FS
	No adjustment at +25°C T_{min} to T_{max}	II	0.8			0.6			0.4			% of FS
	With adjustment at +25°C T_{min} to T_{max}	II	0.5			0.25			0.12			% of FS
Temperature Coefficients	Using internal reference T_{min} to T_{max}											
Unipolar Offset		I	± 2 (5)			± 1 (2.5)			± 1 (2.5)			LSB (ppm/°C)
Bipolar Offset		I	± 4 (10)			± 2 (5)			± 1 (2.5)			LSB (ppm/°C)
Full Scale Calibration		I	± 20 (50)			± 10 (25)			± 5 (12.5)			LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V		I	± 0.5 ± 2			± 0.5 ± 1			± 0.5 ± 1			LSB
+4.5V < V_{LOGIC} < +5.5V		I	± 0.1 ± 0.5			± 0.1 ± 0.5			± 0.1 ± 0.5			LSB
Analog Inputs Input Ranges			-5	+5	-5	+5	-5	+5	-5	+5	VOLTS	
Bipolar		I	-10	+10	-10	+10	-10	+10	-10	+10	VOLTS	
Unipolar		I	0	+10	0	+10	0	+10	0	+10	VOLTS	
		I	0	+20	0	+20	0	+20	0	+20	VOLTS	
Input Impedance 10 Volt Span 20 Volt Span		I	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	k Ω
		I	15	20	25	15	20	25	15	20	25	k Ω

Note 1: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.

MILITARY TEMPERATURE RANGE -55 TO +125°CT_A = -55 to 125°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZCM		HADC674ZBM		HADC674ZAM		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
DC ELECTRICAL CHARACTERISTICS									
Power Supplies Operating Voltage Range V _{LOGIC}		I	+4.5	+5.5	+4.5	+5.5	+4.5	+5.5	VOLTS
V _{CC}		I	+11.4	+16.5	+11.4	+16.5	+11.4	+16.5	VOLTS
V _{EE}	Not required for circuit operation.								
Operating Current I _{LOGIC}		I	0.5	1	0.5	1	0.5	1	mA
I _{CC}		I	7	9	7	9	7	9	mA
I _{EE}	Not required for circuit operation.								
Power Dissipation ±15V, +5V		I	110	150	110	150	110	150	mW
Internal Reference Voltage		I	9.9	10 10.1	9.9	10 10.1	9.9	10 10.1	VOLTS
Output Current ²		I		2		2		2	mA

DIGITAL CHARACTERISTICS

Logic Inputs (CE, \overline{CS} , R/C, A0, 12/8)									
Logic "1"		I	2.0	5.5	2.0	5.5	2.0	5.5	VOLTS
Logic "0"		I	-0.5	+0.8	-0.5	+0.8	-0.5	+0.8	VOLTS
Current	0 to +5.5V Input	I	±0.1	+1	±0.1	+1	±0.1	+1	μA
Capacitance		II	5		5		5		pF
Logic Outputs (DB11-DB0, STS)									
Logic "0"	(I _{SINK} = 1.6mA)	I		+0.4		+0.4		+0.4	VOLTS
Logic "1"	(I _{SOURCE} = 500μA)	I	+2.4		+2.4		+2.4		VOLTS
Leakage	(High Z State, DB11- DB0 Only)		-5 ±0.1 +5		-5 ±0.1 +5		-5 ±0.1 +5		μA
Capacitance		II	5		5		5		pF

Note 2 Available for external loads, external load should not change during conversion.

When supplying an external load and operating on +12V supplies, a buffer amplifier must be provided for the reference output.

CONVERT MODE TIMING CHARACTERISTICS

Typical @ 25°C, $V_{CC} = +15V$ or $+12V$, $V_{LOGIC} = +5V$, unless otherwise specified.

HADC674Z

2

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC		HADC674ZB		HADC674ZA		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	

AC ELECTRICAL CHARACTERISTICS

t_{DSC} STS Delay from CE		I	200		200		200		ns
t_{HEC} CE Pulse Width		I	50		50		50		ns
t_{SSC} \overline{CS} to CE Setup		I	50		50		50		ns
t_{HSC} \overline{CS} Low during CE High		I	50		50		50		ns
t_{SRC} R/\overline{C} to CE Setup		I	50		50		50		ns
t_{HRC} R/\overline{C} Low During CE High		I	50		50		50		ns
t_{SAC} A0 to CE Setup		I	0		0		0		ns
t_{HAC} A0 Valid During CE High		I	50		50		50		ns
t_C Conversion Time 12-Bit Cycle	Tmin to Tmax	I	9	15	9	15	9	15	μ s
	8-Bit Cycle	I	6	10	6	10	6	10	μ s

Note 5: Time is measured from 50% level of digital transitions. Tested with a 100pF and 3k Ω load for high impedance to drive and tested with 10pF and 3K Ω load for drive to high impedance.

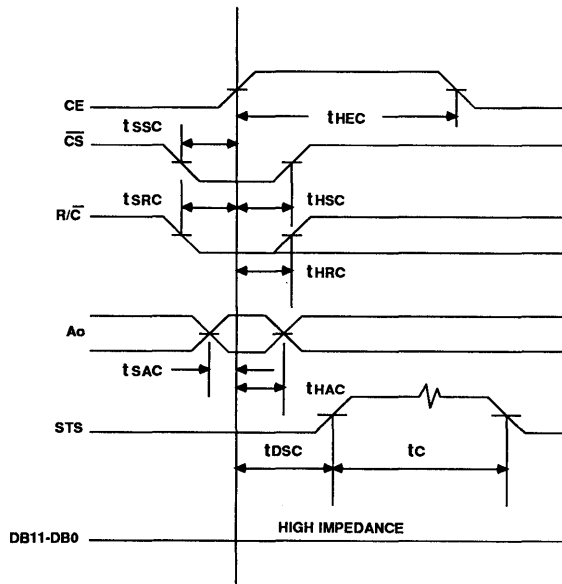


Figure 1 - Convert Mode Timing Diagram

READ MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC		HADC674ZB		HADC674ZA		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	

AC ELECTRICAL CHARACTERISTICS

t _{DD} Access Time from CE		I		150		150		150	ns
t _{HD} Data Valid After CE Low		I	25		25		25		ns
t _{HL} Output Float Delay		I		150		150		150	ns
t _{SSR} \overline{CS} to CE Setup		I	50	0	50	0	50	0	ns
t _{SRR} R/C to CE Setup		I	0	0	0	0	0	0	ns
t _{SAR} A ₀ to CE Setup		I	50		50		50		ns
t _{HSR} \overline{CS} Valid After CE Low		I	0	0	0	0	0	0	ns
t _{HRR} R/C High After CE Low		I	0	0	0	0	0	0	ns
t _{HAR} A ₀ Valid After CE Low		I	50		50		50		ns
t _{HS} STS Delay After Data Valid		I	100	600	100	600	100	600	ns

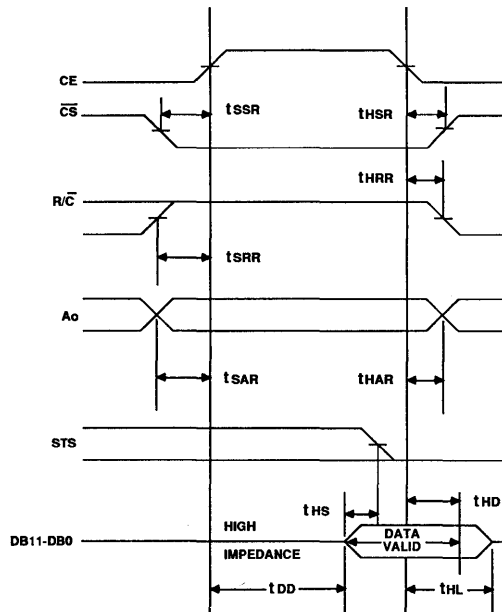


Figure 2 - Read Mode Timing Diagram

STAND-ALONE MODE TIMING CHARACTERISTICS

Typical @ +25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, unless otherwise specified.

HADC674Z

2

PARAMETER	TEST CONDITIONS NOTE 5	TEST LEVEL	HADC674ZC			HADC674ZB			HADC674ZA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

AC ELECTRICAL CHARACTERISTICS

t _{HRL} Low R/C Pulse Width		I	50			50			50			ns
t _{DS} STS Delay from R/C		I			200			200			200	ns
t _{HDR} Data Valid After R/C Low		I	25			25			25			ns
t _{HS} STS Delay After Data Valid		I	100	600		100	600		100	600		ns
t _{HRH} High R/C Pulse Width		I	150			150			150			ns
t _{DDR} Data Access Time		I			150			150			150	ns

SAMPLE AND HOLD

Acquisition Time		II	1.8	2.4	3.0	1.8	2.4	3.0	1.8	2.4	3.0	μs
Aperture Uncertainty Time		II	8			8			8			ns

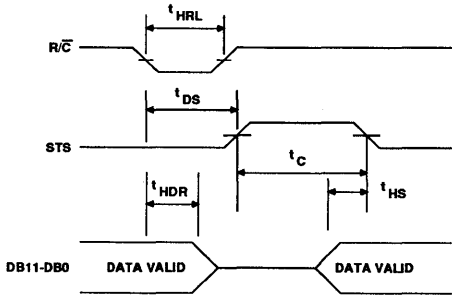


Figure 3 - Low Pulse For R/C - Outputs Enabled After Conversion

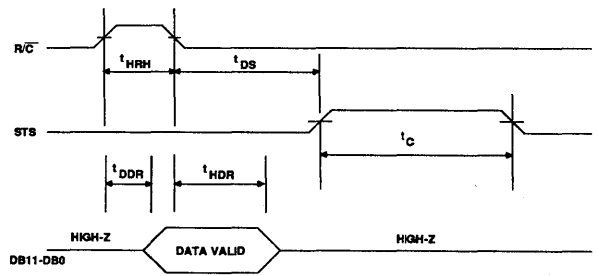


Figure 4 - High Pulse For R/C - Outputs Enabled While R/C is High, Otherwise High Impedance

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore T_{junc} = T_{case} = T_{ambient}.

TEST LEVEL

TEST PROCEDURE

I

Production tested at the specified conditions.

II

Parameter is guaranteed by design and sampled characterization data.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out (See Figure 5 and 7). The point used as "zero" occurs 1/2LSB (1.22mV for a 10 Volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC674ZAC and BC grades are guaranteed for maximum nonlinearity of $\pm 1/2$ LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC674AM, BM, CC and CM grades are guaranteed to ± 1 LSB maximum error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC674Z type BC, AC, BM, and AM grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC674Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 7 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC674Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 7 points out two missed codes in the transfer function.

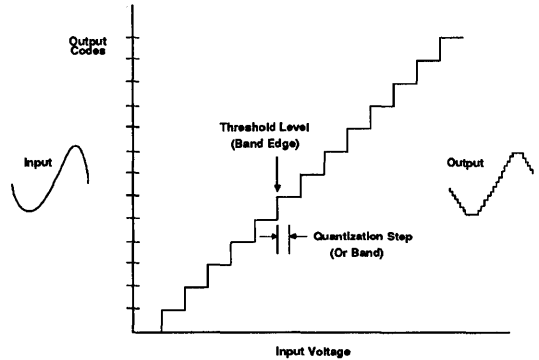


Figure 5 - Static Input Conditions

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm 1/2$ LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = \text{FSR}/2^N$ where FSR = full scale range and $N = 12$. Non-ideal quantization bands represent differential nonlinearity errors (See Figures 5, 6 and 7).

RESOLUTION - ACTUAL VS. AVAILABLE

The available resolution of an N-bit converter is 2^N . This means it is theoretically possible to generate 2^N unique output codes.

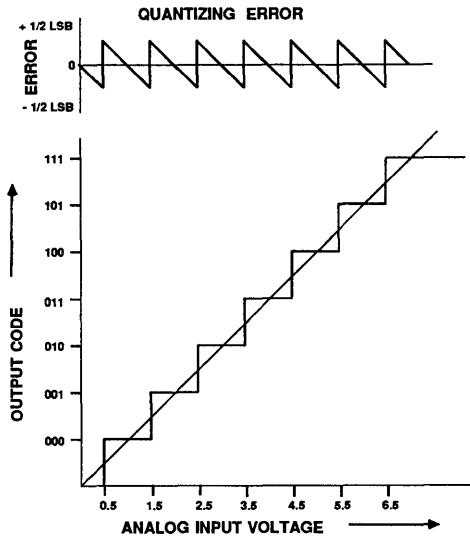


Figure 6 - Quantizing error

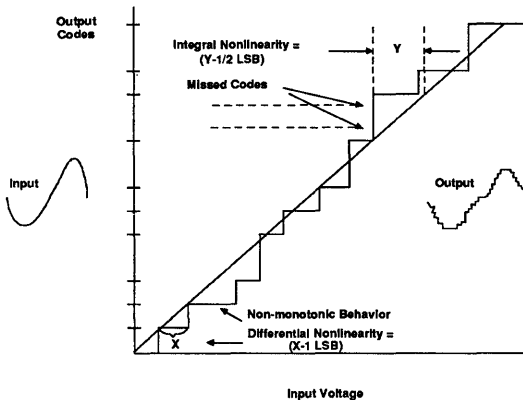


Figure 7 - Dynamic Conditions

THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rated performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

The slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC674Z, this is the time delay between the R/C falling edge and the actual start of the HOLD mode in a sample and HOLD function.

APERTURE JITTER

A specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates which converts high frequency signals with great accuracy. A sample and hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level $1/2\text{LSB}$ above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 to 1000 0000 0000) should occur for an analog value $1/2\text{LSB}$ below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

The time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC674Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2LSB below the nominal full scale (9.9963 Volts for 10.000 Volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 Volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max} .

POWER SUPPLY REJECTION

The standard specifications for the HADC674Z assume +5.00 and +15.00 or +12.00 Volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 Volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC674Z is left-justified. This means that the data represents the analog input as a fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 7 demonstrates non-monotonic behavior.

CIRCUIT OPERATION

The HADC674Z is a complete 12-bit Analog-To-Digital converter which consists of a single chip version of the industry standard 674. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample & hold, clock, output buffers and control circuitry to make it possible to use the HADC674Z with few external components.

When the control section of the HADC674Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC674Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within $\pm 1/2$ LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts $\pm 1\%$ and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with $\pm 15V$ supplies. If the HADC674Z is used with $\pm 12V$ supplies, or if external current must be supplied over the full temperature range, an

external buffer amplifier is recommended. Any external load on the HADC674Z reference must remain constant during conversion.

The sample and hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC674Z appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the HADC674Z over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC674Z is disconnected from the user's sample and hold. This prevents transients occurring during conversion from being inflicted upon the attached sample and hold buffer. All other 674 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the HADC674Z allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC674Z acts as any other 674 device because the internal S/H is transparent. The sample/hold function in the HADC674Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HADC674Z and is controlled through the normal R/C control line (refer to Figure 8.) When the R/C line makes a negative transition, the HADC674Z starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with

the duration controlled by the internal clock cycle.

During T_{acq} , the equivalent circuit of the HADC674Z in-put is as shown in Figure 9 (the time constant of the input is independant of which input level is used.) This CDAC capacitance must be charged up to the input voltage during T_{acq} . Since the CDAC time constant is 100 nsecs., there is more than enough time for settling the input to 12 bits of accuracy during T_{acq} . The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Note that because the sample is taken relative to the R/C transition, T_{acq} is also the traditional "aperture delay" of this internal sample and hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in $T_{acq} = 2.4 \mu\text{secs} \pm 0.6 \mu\text{secs}$. between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HADC674Z.

APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time the actual sample is taken - i.e. the "aperture jitter" or T_{AJ} . The HADC674Z has a nominal aperture jitter of 8 nsecs. between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (See Figure 10). The magnitude of this change for a sine-wave can be calculated:

Assume a sinusoidal signal, maximum slew rate, $Sr = 2\pi f V_p$ (V_p = peak voltage, f = frequency of sine wave)
For an N-bit converter to maintain +/- 1/2 LSB accuracy :

$V_{err} \leq V_{fs}/2^{N+1}$ (where V_{err} is the allowable error voltage and V_{fs} is the full scale voltage)

From Figure 10:

$$Sr = \Delta V / \Delta T = 2\pi f V_p$$

Let $\Delta V = V_{err} = V_{fs} \cdot 2^{-(N+1)}$, $V_p = V_{in}/2$ and $\Delta T = t_{AJ}$ (the time during which unwanted voltage change occurs)

The above conditions then yield:

$$Vfs/2^{N+1} \geq \pi Vint_{AJ} \text{ or } f_{max} \leq Vfs/(\pi Vint_{AJ})2^{N+1}$$

For the HADC674Z, $T_{AJ} = 8 \text{ nsec}$,
therefore $f_{max} \leq 5 \text{ KHz}$.

For higher frequency signal inputs, an external sample and hold is recommended.

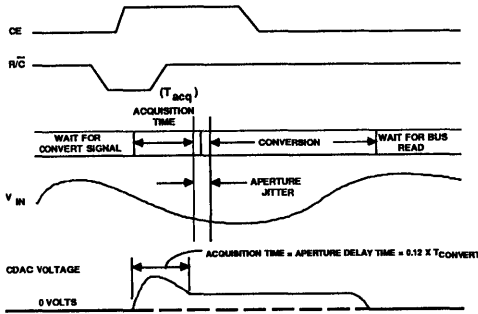


Figure 8 - Sample and Hold Function

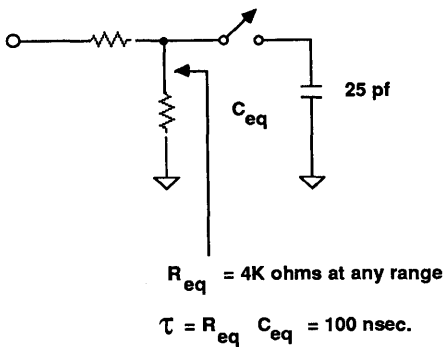


Figure 9 - Equivalent HADC674Z Input Circuit

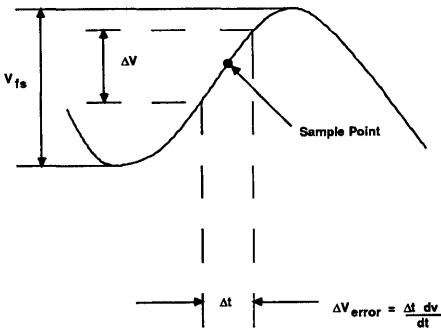


Figure 10 - Aperture Uncertainty

TYPICAL INTERFACE CIRCUIT

The HADC674Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figures 11 and 12. The two typical interface circuits are for operating the HADC674Z in either a unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the P.C. board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC674Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10µF tantalum and a 0.1µF ceramic type in parallel between V_{LOGIC} (pin1) and digital common (pin15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC674Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6mADC while the digital ground is 3mADC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependant currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC674Z may be operated by a μP or in the stand-alone mode. The part has four standard input ranges: 0V to +10V, 0V to +20V, $\pm 5\text{V}$ and $\pm 10\text{V}$. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of $+1/2\text{LSB}$ or $+1.22\text{mV}$ for the 10V range and $+2.44\text{mV}$ for the 20V range should be applied to the HADC674Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and $1/2\text{LSB}$ below the nominal full scale which is $+9.9963\text{V}$ for the 10V range and $+19.9927\text{V}$ for the 20V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R1 with a 50Ω , 1% metal film resistor and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

BIPOLAR

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R1

and R2 (See Figure 12). If adjustment is not needed, either or both pots may be replaced by a 50Ω , 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a $\pm 5\text{V}$ range or to pin 14 for a $\pm 10\text{V}$ range. First apply a DC input voltage $1/2\text{LSB}$ above negative full scale which is -4.9988V for the $\pm 5\text{V}$ range or -9.9976V for the $\pm 10\text{V}$ range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and $1/2\text{LSB}$ below positive full scale which is $+4.9963\text{V}$ for the $\pm 5\text{V}$ range or $+9.9927\text{V}$ for the $\pm 10\text{V}$ range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

The 100Ω potentiometer R2 provides gain adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (for an LSB of 2.5mV) or 20.48V (for an LSB of 5.0mV) is more convenient. For these, replace R2 by a 50Ω , 1% metal film resistor. Then to provide gain adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 1000Ω potentiometer in series with pin 14.

CONTROLLING THE HADC674Z

The HADC674Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the $\overline{\text{R/C}}$ input pin. Full μP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include $12/\overline{8}$, $\overline{\text{CS}}$, A0, R/C and CE). The use of these inputs in controlling the converter's operations is shown in Table 1, and the internal control logic is shown in a simplified schematic in Figure 13.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/C. The other controls must be tied to known states as follows: CE and $12/\overline{8}$ are wired high, A0 and $\overline{\text{CS}}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/C duty cycle are shown in Figures 3 and 4. It may have duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress.

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in Figure 13 and Table 1. The latched state determines if the conversion stops with 8-bits (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

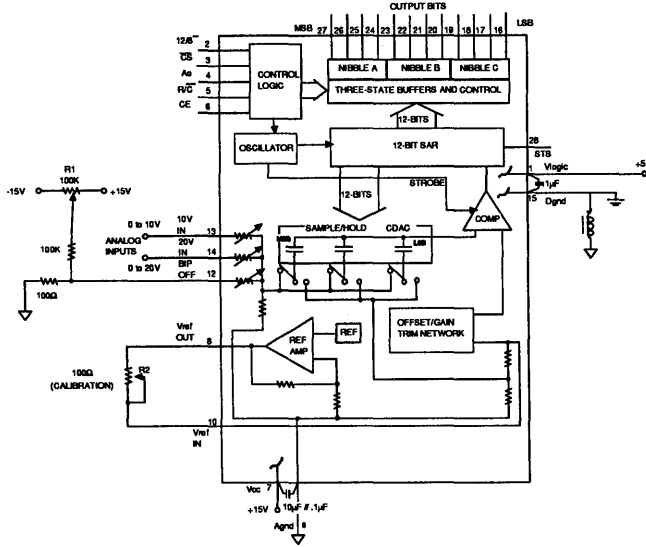


Figure 11 - Unipolar Input Connections

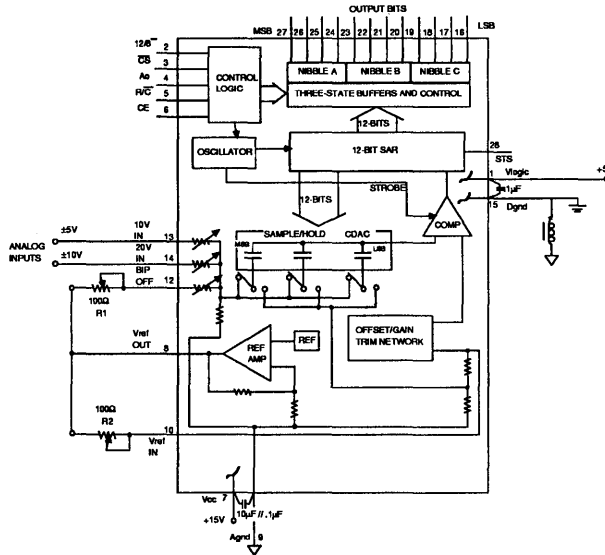


Figure 12 - Bipolar Input Connections

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, \overline{CS} , R/\overline{C} , as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new state of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

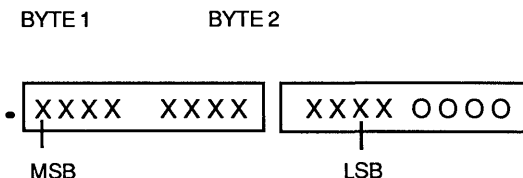
READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/\overline{C} is high, STS is low, CE is high and \overline{CS} is low. The data lines become active in response to the four conditions and output data according to the conditions of $12/\overline{8}$ and Ao. The timing diagram for this process is shown in Figure 2. When $12/\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The $12/\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible.

Table 1 - Truth Table for the HADC674Z Control Inputs

CE	\overline{CS}	R/\overline{C}	$12/\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

When $12/\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 13. The Ao control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 13 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.

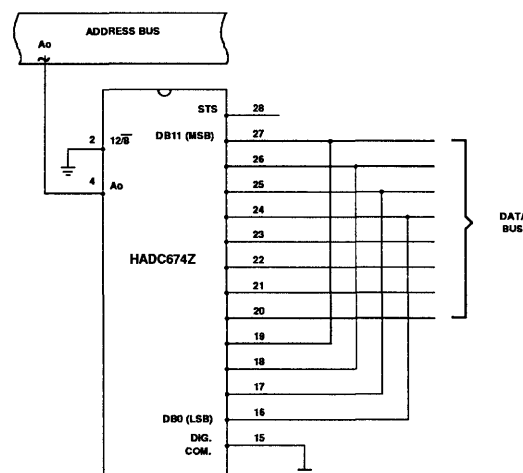


Figure 13 - Interfacing the HADC674Z to an 8-bit Data Bus

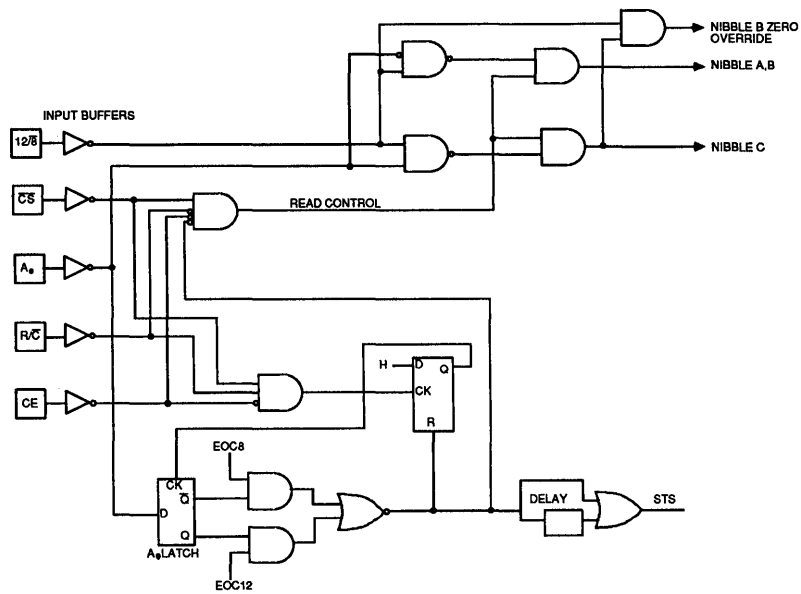


Figure 14 - HADC674Z Control Logic

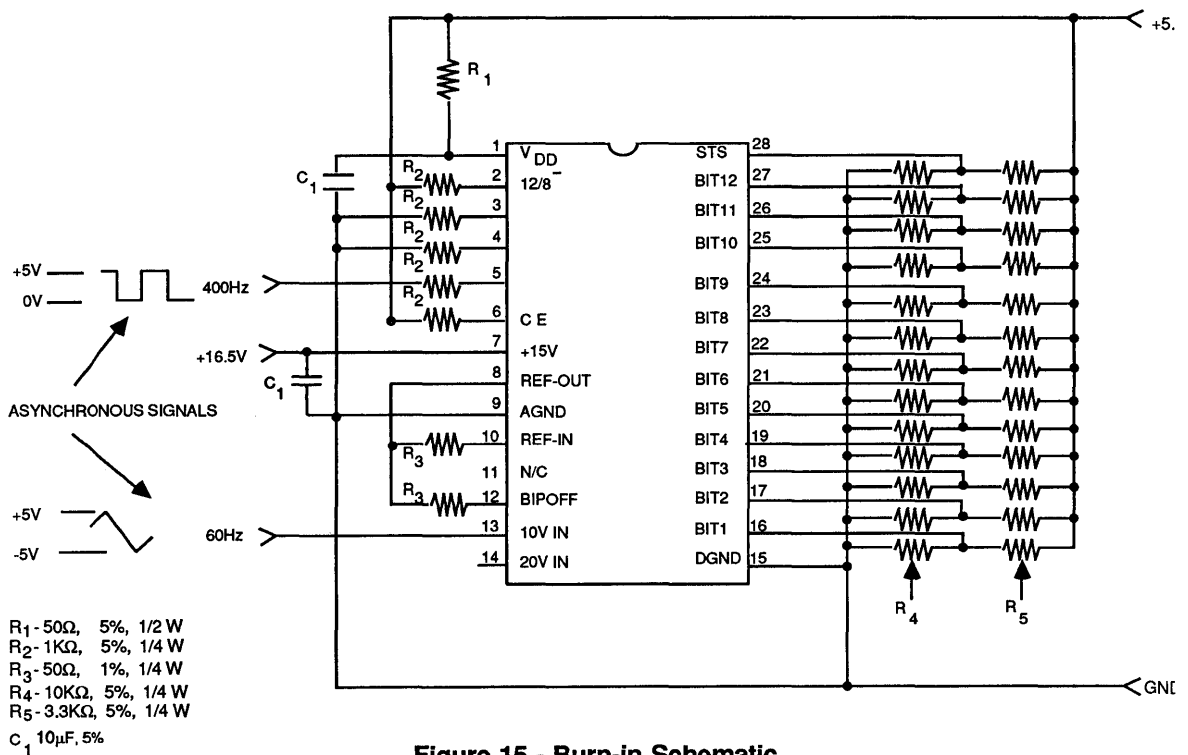
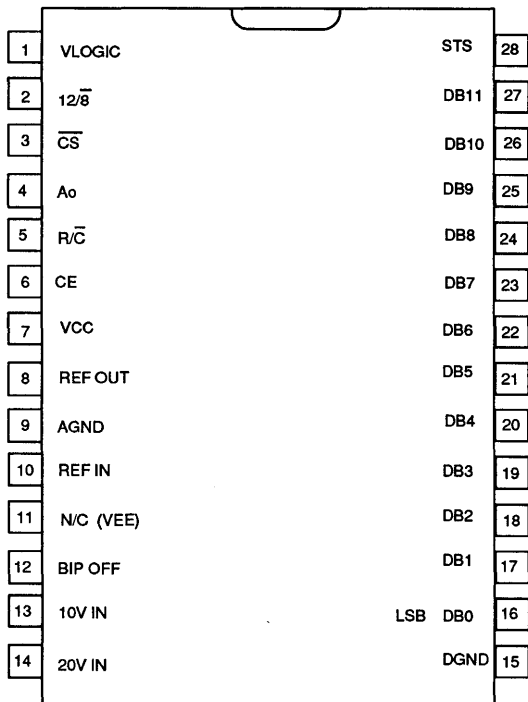


Figure 15 - Burn-in Schematic

PIN ASSIGNMENT HADC674Z

TOP VIEW



28 LEAD DIP

PIN FUNCTIONS HADC674Z

NAME	FUNCTION
V _{LOGIC}	Logic Supply Voltage, Nominally +5V
12/8	Data Mode Select
CS	Chip Select
A ₀	Byte Address/ Short cycle
R/C	Read/ Convert
CE	Chip Enable
V _{CC}	Analog Positive Supply Voltage Nominally +15V
REF OUT	Reference Output Nominally +10V
AGND	Analog Ground
REF IN	Reference Input
N/C (VEE)	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10V IN	10 Volt Analog Input
20V IN	20V Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

HADC674Z

2

**For Ordering Information See Section 1.

NOTES:

COMPLETE HIGH-SPEED 12-BIT A/D CONVERTER

ADVANCE INFORMATION

FEATURES:

- Improved Version of the AD7572
- 12-Bit Resolution and Accuracy
- High Speed; 3 and 5 μ sec Versions
- Improved Analog Input Circuitry;
 - No Dynamic Source Loading
 - High Impedance
- Improved Negative Power Supply Range;
 - -10.5 to -16.5 Volts

APPLICATIONS:

- Data Acquisition
- Instrumentation
- Process Control
- DSP System Digitizer
- Microprocessor Interface
- Personal Computer Interface

2

GENERAL DESCRIPTION

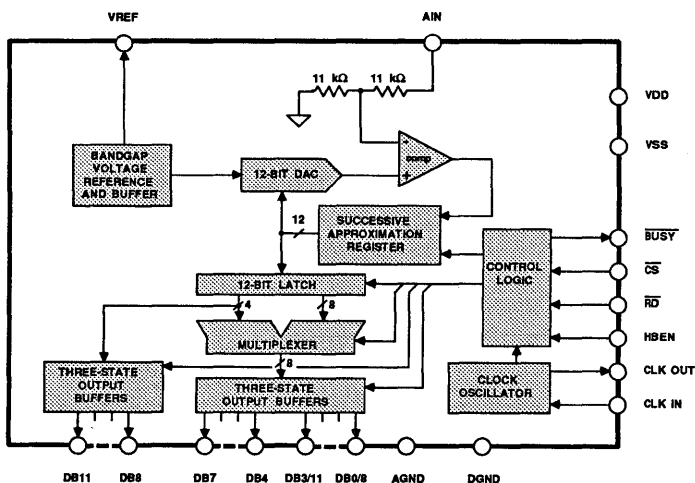
The HADC7572 is a complete 12-bit A/D converter that offers high speed with low power dissipation. This is achieved with a successive approximation architecture on a monolithic BIMOS process. Unlike the AD7572, the HADC7572 uses analog input circuitry that virtually eliminates dynamic source loading during the conversion. This minimizes the required bandwidth of the circuitry driving the HADC7572, lowers system cost and simplifies system design.

The pre-trimmed internal band-gap voltage reference assures stable operation over all operating conditions. No external trim is required to meet the specified accuracy. Device timing is controlled by the synchronous clock input, or optionally an external crystal, both provided by the user. For 0 to 5 volt unipolar operation no external components are required. Decoupling capacitors at the power supply pins are recommended.

The HADC7572 also offers an improved negative power supply range of -10.5 to -16.5 volts. This broadens application possibilities and simplifies applications that utilize negative power supplies which vary from the standard -15 volt analog supply system.

The tri-statable data outputs and high speed digital interface of the HADC7572 ensures compatibility with most popular 8, 16 and 32-bit microprocessors. The device is packaged in a 24 pin 300 mil DIP.

BLOCK DIAGRAM



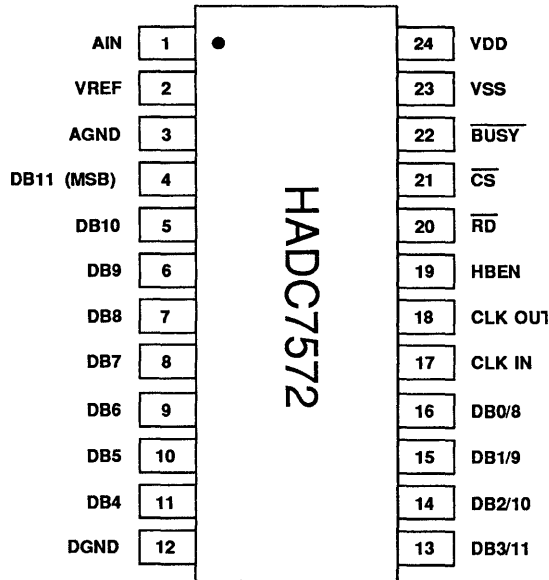
ELECTRICAL SPECIFICATIONS

VDD = 5V ±5%, VSS = -10.5 to -16.5V, F_{CLK} = 2.5 MHz, T_A = T_{MIN} to T_{MAX} Unless Otherwise Noted

Parameter	Test Conditions	Test Level (1)	Min	HADC7572 Typ	Max	Units
Integral Nonlinearity		I			±0.5	LSB
Differential Nonlinearity		I			±0.5	LSB
Gain Temperature Coefficient		I			25	ppm/°C
Logic Inputs						
V _{IH} (Input High Voltage)		I	2.0			Volts
V _{IL} (Input Low Voltage)		I			0.8	Volts
Conversion Time						
Synchronous Clock		I			5	μsec.
Asynchronous Clock		I	4.8		5.2	μsec

(1) Test Procedure: I - Production tested at the specified conditions

HADC7572 PIN OUT



**For Ordering Information See Section 1.

**COMPLETE HIGH-SPEED 12-BIT A/D CONVERTER
WITH INTERNAL VOLTAGE REFERENCE**

ADVANCE INFORMATION

FEATURES:

- Improved Version of the AD7672
- Optional Internal Voltage Reference
- 12-Bit Resolution and Accuracy
- High Speed; 3 and 5 μ sec Versions
- Improved Analog Input Circuitry; No Dynamic Source Loading High Impedance
- Improved Negative Power Supply Range; -10.5 to -16.5 Volts

APPLICATIONS:

- Data Acquisition
- Instrumentation
- Process Control
- DSP System Digitizer
- Microprocessor Interface
- Personal Computer Interface

2

GENERAL DESCRIPTION

The HADC7672 is a complete 12-bit A/D converter that offers high speed with low power dissipation. This is achieved with a successive approximation architecture on a monolithic BIMOS process.

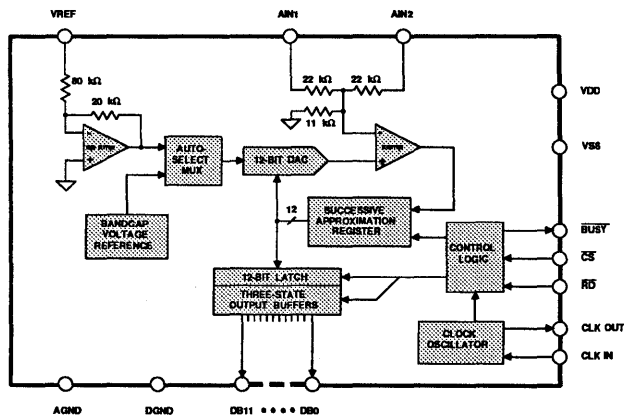
Unlike the AD7672, the HADC7672 includes an on-chip voltage reference which can be used in unipolar applications (only). Optionally, like the AD7672 an off-chip reference can be provided at the VREF pin. An internal multiplexer then automatically disconnects the internal reference. This internal/external reference option provides direct plug-in compatibility, yet allows the user to delete the external reference. The HADC7672 also uses an analog input circuit that virtually eliminates dynamic source loading during the conversion. This reduces the required bandwidth of the circuitry driving the HADC7672, further lowering system cost and simplifying system design.

Another HADC7672 enhancement is a total negative power supply range of -10.5 to -16.5 volts. This broadens application possibilities and simplifies using the -12 volt supply provided by most personal computers.

The pre-trimmed internal band-gap voltage reference assures stable operation over all operating conditions. No external trim is required to meet the specified accuracy. Device timing is controlled by the synchronous clock input, or optionally by an external crystal, both provided by the user. For 0-5 or 0-10 volt unipolar operation no external components are required. Decoupling capacitors at the power supply pins are recommended.

The tri-statable data outputs and high speed digital interface of the HADC7672 ensures compatibility with most popular 16 and 32-bit microprocessors. The device is packaged in a 24-pin 300 mil DIP.

BLOCK DIAGRAM



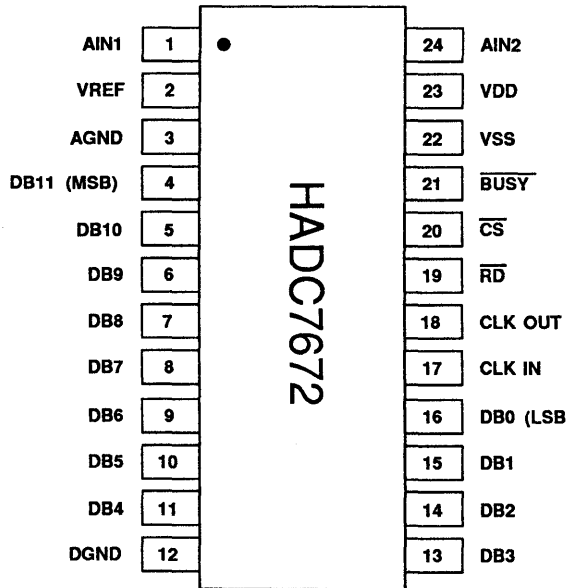
ELECTRICAL SPECIFICATIONS

VDD = 5V ±5%, VSS = -10.5 to -16.5V, F_{CLK} = 2.5 MHz, VREF = NC, T_A = T_{MIN} to T_{MAX} Unless Otherwise Noted

Parameter	Test Conditions	Test Level (1)	Min	HADC7672 Typ	Max	Units
Integral Nonlinearity		I			±0.5	LSB
Differential Nonlinearity		I			±0.5	LSB
Gain Temperature Coefficient		I			25	ppm/°C
Logic Inputs						
V _{IH} (Input High Voltage)		I	2.0			Volts
V _{IL} (Input Low Voltage)		I			0.8	Volts
Conversion Time						
Synchronous Clock		I			5	μsec.
Asynchronous Clock		I	4.8		5.2	μsec

(1) Test Procedure: I - Production tested at the specified conditions

HADC7672 PIN OUT



**For Ordering Information See Section 1.

8-BIT, 150 MSPS FLASH A/D CONVERTER

FEATURES

- 150 MSPS NOMINAL CONVERSION RATE
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Typical Power Dissipation < 2.0 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

2

GENERAL DESCRIPTION

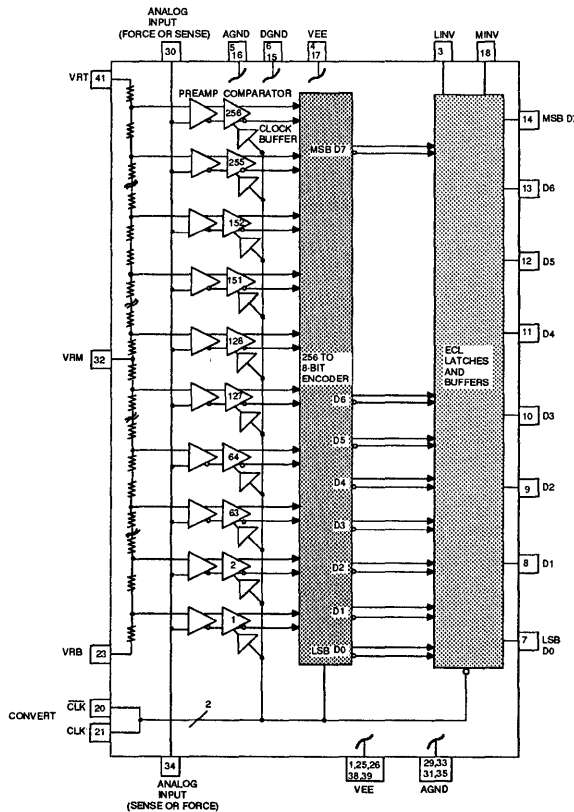
The HADC77100 is a monolithic flash A/D converter capable of digitizing a 2 volt analog input signal with full scale frequency components to 50 MHz into 8-bit digital words at a 150 MSPS update rate.

HADC77100, with nominal power dissipation of less than 1.75 Watts.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time. A single standard -5.2 Volt power supply is required for operation of the

The part is packaged in a 42 Lead Ceramic DIP that is pin compatible with the CX20116. Careful attention to design and layout has provided a device with better linearity, lower noise floor, stable input capacitance, and lower data error rates. The HADC77100 is available in Industrial and Military Temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25°C

Supply Voltages Output

Negative Supply Voltage (V_{EE TO GND}) ..-7.0 to +0.5 V
 Ground Voltage Differential.....-0.5 to +0.5V

Output

Digital Output Current.....0 to -25 mA

Input Voltage

Analog Input Voltage.....+0.5 to V_{EE} V
 Reference Input Voltage.....+0.5 to V_{EE} V
 Digital Input Voltage.....+0.5 to V_{EE} V
 Reference Current VRT to VRB.....25 mA
 Midtap Reference Current.....-6 to +6 mA

Temperature

Operating Temperature, ambient.....-65 to +150°C
 junction.....+150°C
 Lead Temperature, (soldering 10 seconds).....+300°C
 Storage Temperature.....-65 to +150°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

V_{EE} = -5.2V, R_{Source} = 10Ω, f_{clock} = 100MHz, Duty Cycle = 50% VRB = -2.00V, VRT = 0.00V, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C		HOT +85°C		COLD -25°C		UNITS
			MIN	TYP MAX	MIN	MAX	MIN	MAX	

TRANSFER CHARACTERISTICS

Integral Linearity , 77100A		II		±1 2		±1 2		±1 2	LSB
Differential Linearity , 77100A		II		±1 2		±1 2		±1 2	LSB
Integral Linearity, 77100B		II		±3 4		±3 4		±3 4	LSB
Differential Linearity, 77100B (No missing codes)		II		±3 4		±3 4		±3 4	LSB
Offset Error VRT		II	-30	30	-30	30	-30	30	mV
Offset Error VRB		II	-30	30	-30	30	-30	30	mV

ANALOG INPUT CHARACTERISTICS

Input Voltage Range		I	-2.0	0.0	-2.0	0.0	-2.0	0.0	VOLTS
Input Capacitance	Over full input range	V	56						pF
Input Resistance		V	4						kΩ
Input Current		II	175	275	225		350		μA
Clock Synchronous Input Currents		V	40						μA

TEST LEVEL CODE: See page 5.

ELECTRICAL SPECIFICATIONS**INDUSTRIAL TEMPERATURE RANGE**
 $V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50% $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

POWER SUPPLIES

Supply Current		II	330	370	370	370	370	mA
Power Dissipation		II	1.7	1.93	1.93	1.93	1.93	watts

REFERENCE

Ladder Resistance		II	100	300	100	300	80	300	Ω
Reference Bandwidth		V	50					MHz	

DIGITAL LOGIC

Output High Voltage	50 Ω to -2V	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	VOLTS
Output Low Voltage	50 Ω to -2V	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	VOLTS
Input High Voltage (MINV, LINV)		II	-1.13	-0.81	-1.07	-0.67	-1.27	-0.87	VOLTS	
Input Low Voltage (MINV, LINV)		II	-1.95	-1.48	-1.95	-1.42	-1.95	-1.50	VOLTS	

 $V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50% $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

CONVERSION TIMING, See Figure 1A

Maximum Sample Rate		V	125	150	125	125		MSPS
Clock Low Width, TPW0		V	4	3	4	4		ns
Clock High Width, TPW1		V	4	3	4	4		ns
Output Latency		IV		1	1	1		CYCLE
Output Delay, TD	Differential Clock	V		4.2				ns
Output Delay Tempco	Differential Clock	V		15				ps/°C
Output Rise Time 20% to 80%	50 Ω to -2V	V		2				ns
Output Fall Time 20% to 80%	50 Ω to -2V	V		2				ns

TEST LEVEL CODE: See page 5.

ELECTRICAL SPECIFICATIONS**INDUSTRIAL TEMPERATURE RANGE**

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50% $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

ANALOG INPUTS

Large Signal Bandwidth	$V_{in} = F.S.$	V	60						MHz
Small Signal Bandwidth	$V_{in} = 500mV PP$	V	120						MHz
Aperture Jitter		V	12						ps RMS
Aperture Delay	Differential Clock	V	1.8						ns
Aperture Delay Tempco	Differential Clock	V	7						ps/°C
Aperture Time		V	<100						ps
Settle-to-Hold Time		V	3						ns
Input Slew Rate		V	300						V/ μ s

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50% $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

SIGNAL QUALITY $f_{clock} = 100MHz$

Total Dynamic Error	$V_{in} = FS @ 1MHz$	V	46						dB
Total Dynamic Error	$V_{in} = FS @ 25MHz$	V	36						dB
Total Dynamic Error	$V_{in} = FS @ 50MHz$	V	32						dB
Signal to noise ratio	$V_{in} = FS @ 1MHz$	V	48						dB
Signal to noise ratio	$V_{in} = FS @ 25MHz$	V	43						dB
Signal to noise ratio	$V_{in} = FS @ 50MHz$	V	36						dB
Total Harmonic Distortion	$V_{in} = FS @ 1MHz$	V	44						dBc
Total Harmonic Distortion	$V_{in} = FS @ 25MHz$	V	35						dBc
Total Harmonic Distortion	$V_{in} = FS @ 50MHz$	V	24						dBc
Mean Differential Non-Linearity		V	.001						LSB
RMS Differential Non-Linearity		V	.2						LSB
Differential Gain	NTSC 40IRE mod. ramp, $F_c = 125MSPS$	V	1.0						%
Differential Phase		V	.5						DEG

TEST LEVEL CODE: See page 5.

TEST LEVEL CODES

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are performed after die reaches operating temperature

TEST LEVEL

I

II

III

IV

V

TEST PROCEDURE

100% production tested at the specified temperatures.

100% production tested at $T_a = 25^\circ\text{C}$, and sample tested at the specified temperatures.

QA sample tested only at the specified temperatures.

Parameter is guaranteed (but not tested) by design and characterization data.

Parameter is a typical value for information purposes only.

GENERAL DESCRIPTION

The HADC77100 is the fastest monolithic 8-bit parallel flash A/D converter available today. The nominal conversion rate is 150 MSPS and the analog bandwidth is in excess of 50 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low β but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash A/Ds. The preamplifiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The HADC77100 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77100 has an on-board power supply bypass of 1500pF to reduce external component needs, and the output drive capability of the device can provide full ECL swings into 50 Ω loads.

TYPICAL INTERFACE CIRCUIT

The HADC77100 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to

place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

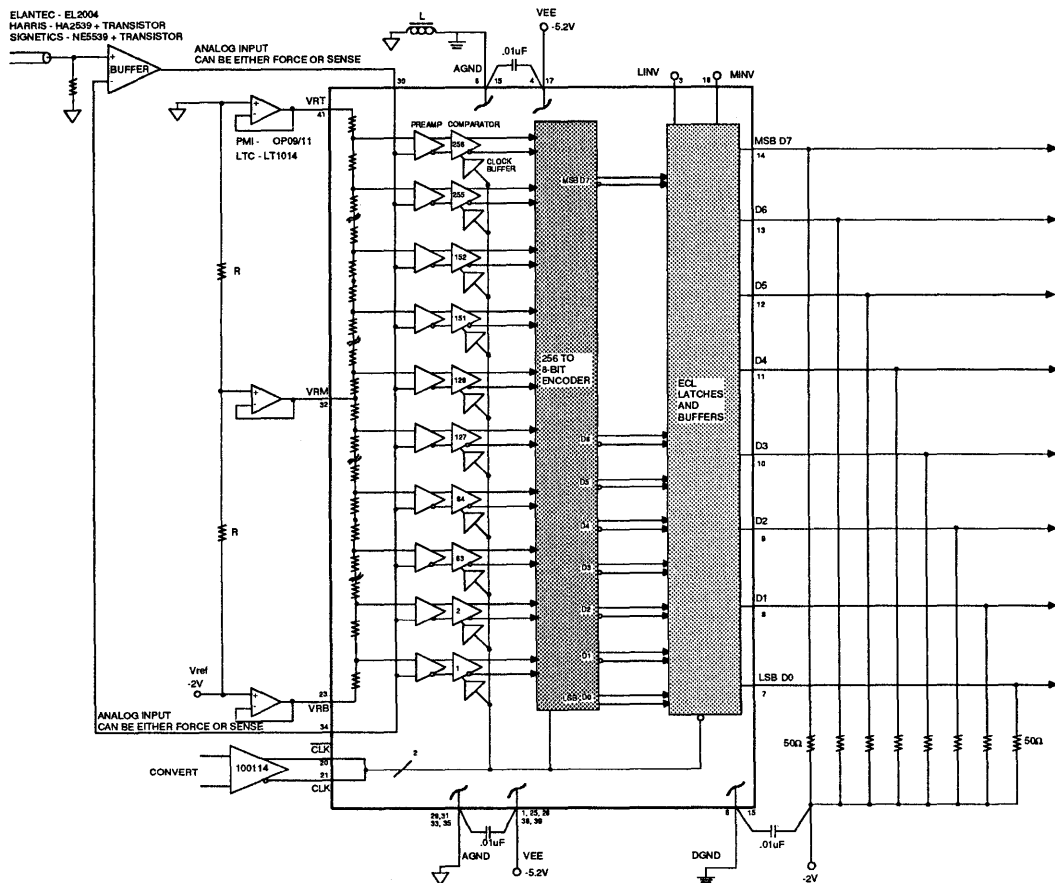
VEE, AGND, DGND

VEE is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 μ F ceramic capacitor. A 1 μ F tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 1.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77100 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836/7 transistor. Very high performance can be achieved by using a comlinear CLC100.

FIGURE 1 HADC77100 TYPICAL INTERFACE CIRCUIT



CLK, CLK (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since CLK is internally biased to -1.3V (see clock input circuit on page 12). It may be left open but a .01μF bypass capacitor from CLK to DGND is recommended. The duty cycle of the clock should be kept at 50% to avoid causing larger 2nd harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

MINV, LINV (Output Logic Control)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table 1. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to DGND through a diode or 3.9kΩ resistor.

D0 to D7 (Digital Outputs)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V the outputs can drive 130Ω to 1KΩ loads.

VRB, VRM, VRT (Reference Input)

There are two reference inputs and one external reference voltage tap. These are -2V (VRB), mid-tap (VRM), and AGND (VRT). The reference pins and tap can be driven by op amps as shown in Figure 1 or VRM may be bypassed for limited temperature operation. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired.

N/C

All "Not Connected" pins should be tied to DGND on the left side of the package and to AGND on the right side.

TABLE 1 - OUTPUT CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.
.
V _{IN}	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.
.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH}

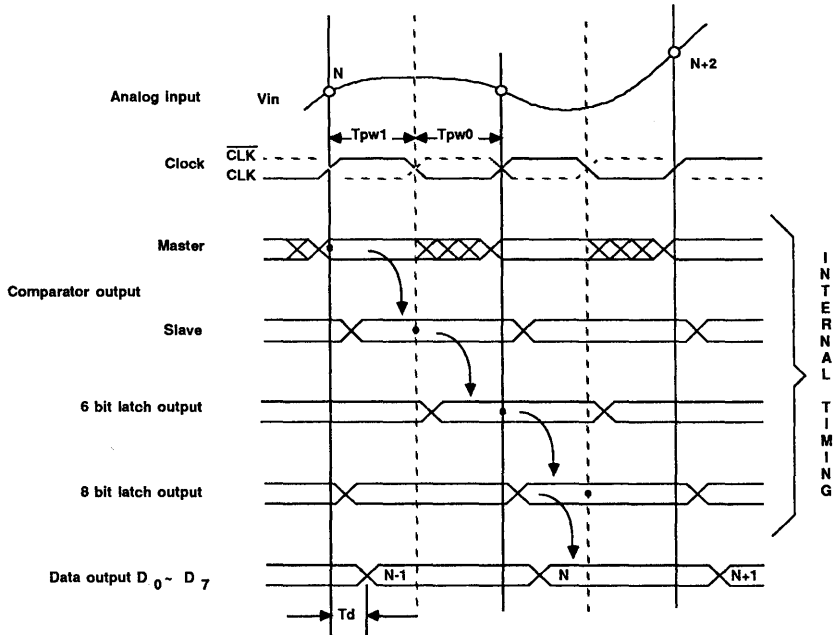
0: V_{IL}, V_{OL}

OPERATION

The HADC77100 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram on page 1. This voltage is applied

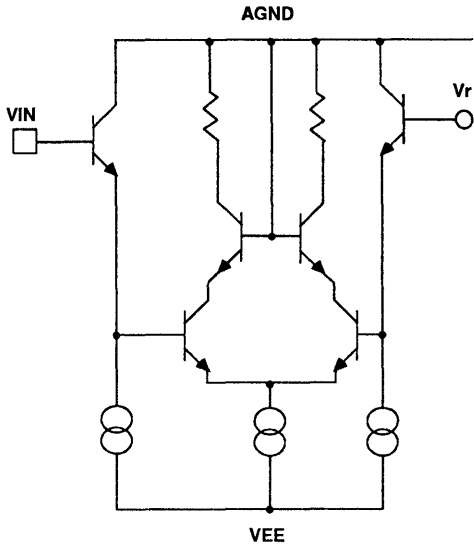
to the positive input of each preamplifier and comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT(0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from four columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions and they consist of a set of eight XOR gates. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

FIGURE 1A - TIMING DIAGRAM

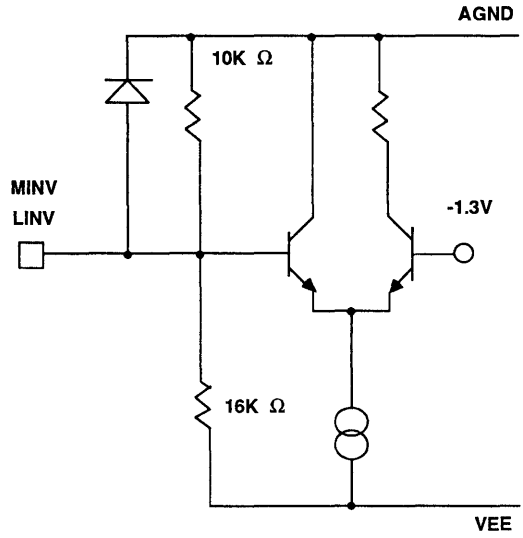


Dots (•) in the chart denote respective latch timings.

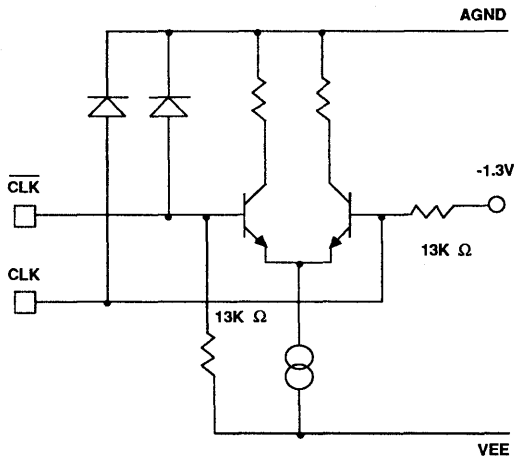
INPUT CIRCUIT



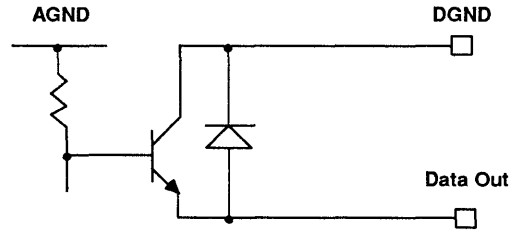
MINV, LINV INPUT CIRCUIT



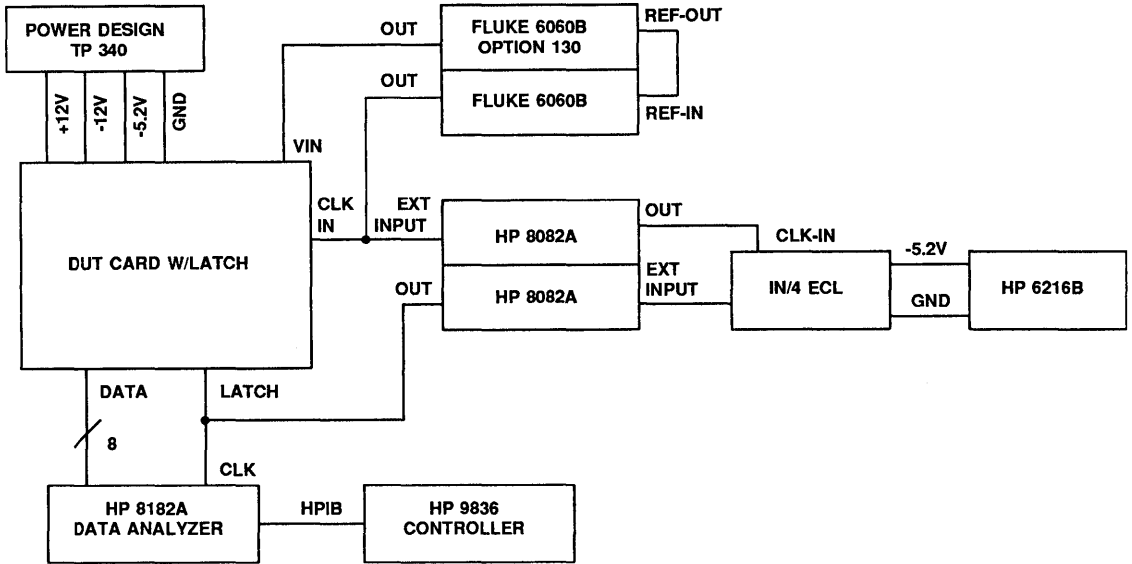
CLOCK INPUT



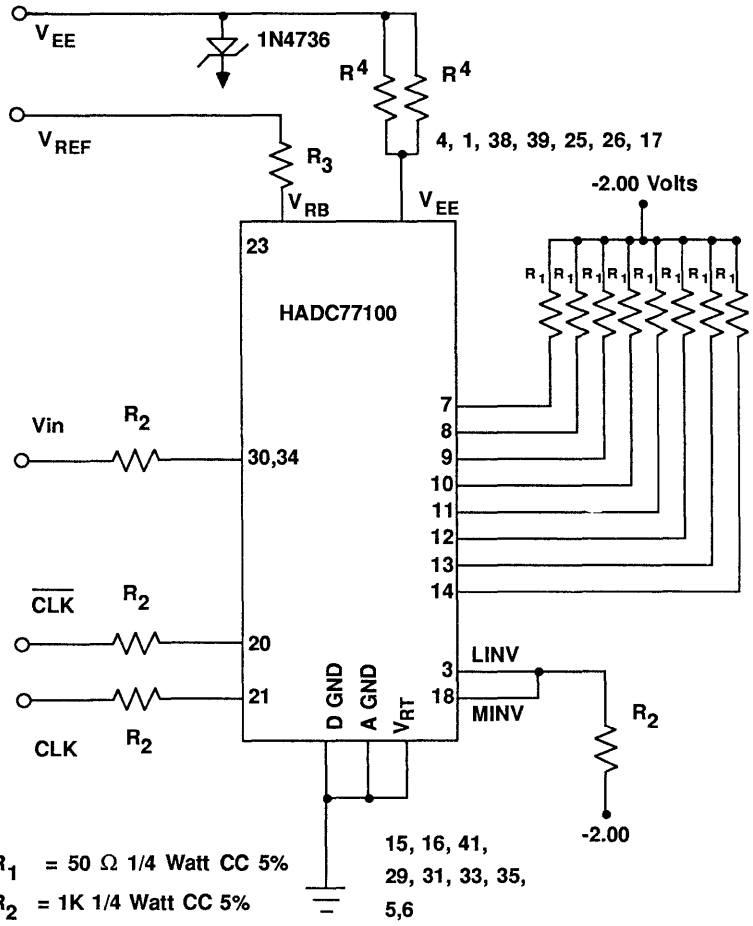
OUTPUT CIRCUIT



DYNAMIC EVALUATION



BURN-IN CIRCUIT $T_{CASE} = 125^{\circ}C$



- $R_1 = 50 \Omega$ 1/4 Watt CC 5%
- $R_2 = 1K$ 1/4 Watt CC 5%
- $R_3 = 6.5 \Omega$ 1/4 Watt CC 5%
- $R_4 = 6.5 \Omega$ 1/4 Watt CC 5%
- $V_{REF} = 2 \times -2.00$ Volts
- $V_{EE} = 2 \times -6.6$ Volts

DEFINITION OF TERMS SPECIFICATIONS

A/D CONVERTER ERROR SUMMARY

Honeywell SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 2B) while a static dc input level may appear close to the ideal (Figure 2A). That is why we are including many dynamic tests as well as the the industry standard dc specifications.

EFFECTIVE BITS (SNR)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from measured rms error for the ideal sinewave and the measured actual rms error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual rms error}}{\text{ideal rms error}}$$

Furthermore, signal-to-noise ratio (SNR) can be related to effective bits by the following formula:

$$\text{SNR(dB)} = 1.8 + 6.02 \times N(\text{eff bits})$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = \text{FSR}/2^N$ where FSR = full scale range and $N = 8$. Non-ideal quantization bands represent differential non-linearity errors (See Figures 2A and 2B).

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 2B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77100's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 2B points out two missed codes in the transfer function.

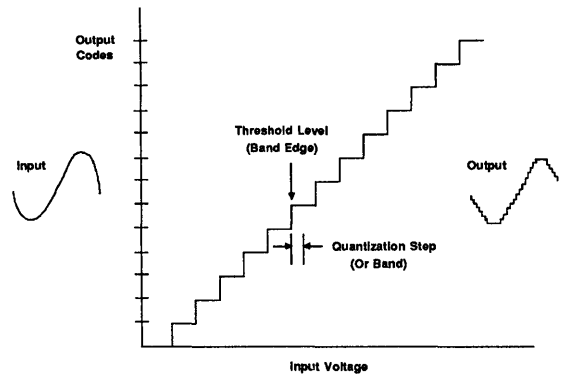


Figure 2A Static Input Conditions

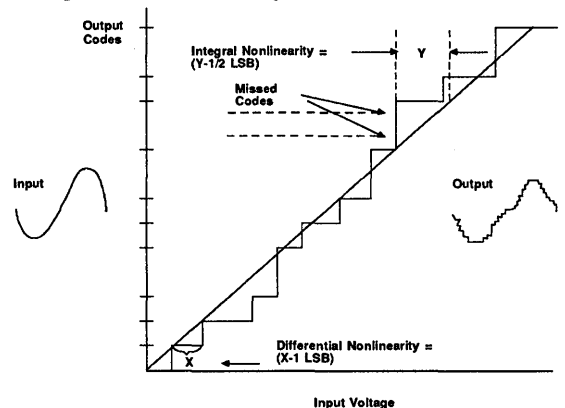


Figure 2B Dynamic Conditions

SPECIFICATIONS CONTINUED

INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 3A). Integral nonlinearity does not include any gain and offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 2B shows an integral nonlinearity error of 2 LSB. The HADC77100's integral nonlinearity can be improved by using the external reference ladder taps as shown in Figure 1. The resulting effect on the linearity is shown in Figure 3B.

APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point. See Figure 3C.

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sine wave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi f t_a$$

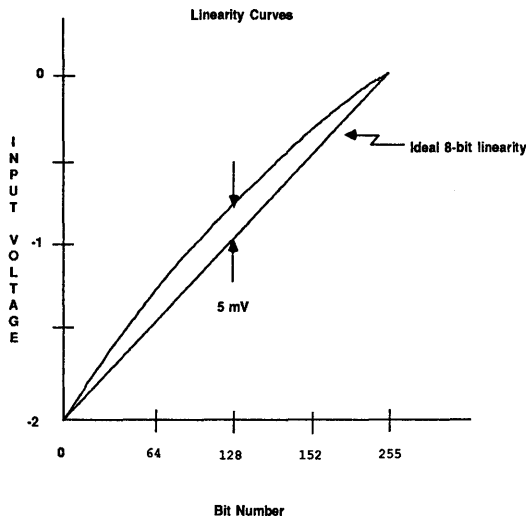


FIGURE 3A Linearity Curve with no TAP adjustment

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 4 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal frequencies.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10MHz, then from Figure 4 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70ps.

Aperture time and delay are very difficult to measure, however these values are needed to make intelligent design decisions. Honeywell SPT supplies these values for the HADC77100 based on both computer design simulations and verified by characterization of samples.

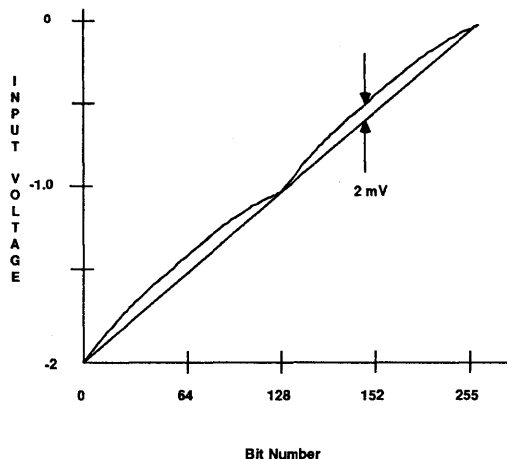


FIGURE 3B Linearity Curve with TAPS Forced to Within .5mV of Ideal

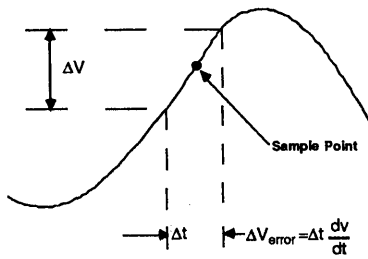


FIGURE 3C Aperture Uncertainty

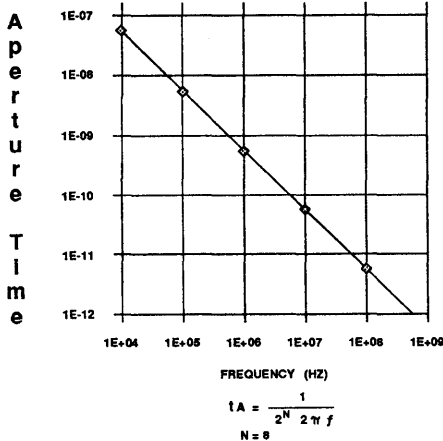
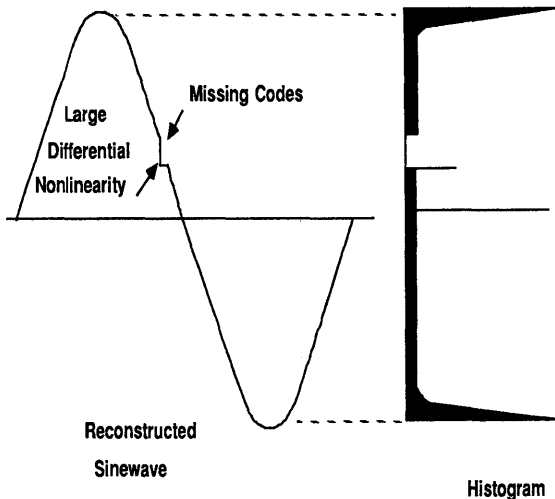


FIGURE 4 Aperture Time - Sinewaves



In the histogram test, A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FIGURE 5 Histogram Testing

CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table 2.

HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77100. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurrence along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurrence at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts (See Figure 5).

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sine-wave, caused by the integral nonlinearity, are aliased

SPECIFICATION TESTING CONTINUED:

into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table 2.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77100. Using least squared error minimization techniques, an idealized sinewave fit to the data is calculated by software. The sinewave is in the form:

$$A\sin(2\pi ft+\theta)+DC$$

where A,f, θ ,DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave, $A_0\sin(2\pi f_0 t+\theta_0)+DC_0$ is then subtracted from the digitized time record.

**TABLE 2
TESTS**

The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

(Table from H. P. Product Note 5180A-2)

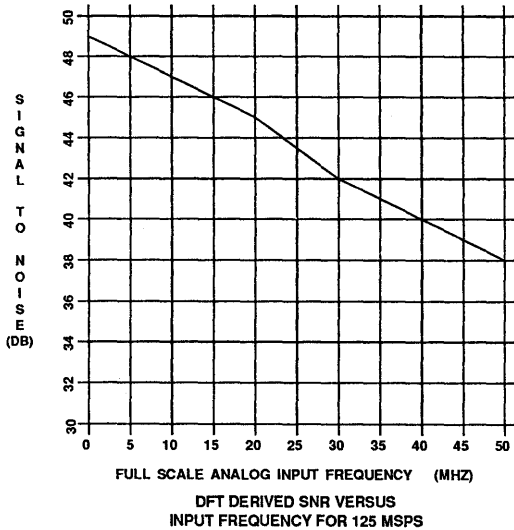
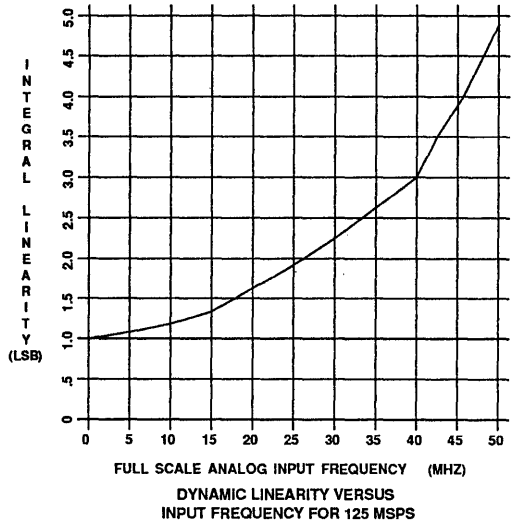
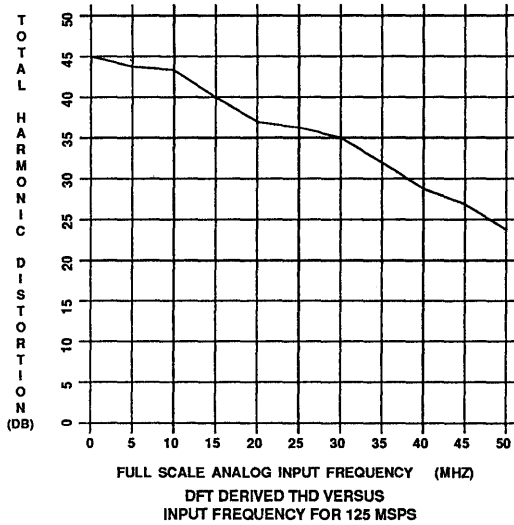
ERROR	HISTOGRAM	FFT	BEAT	
			SINEWAVE CURVE FIT	FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform)	Yes-shows up as harmonics of fundamental aliased into baseband	Yes-part of RMS error	Yes
Aperature Uncertainty	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Noise	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth.
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

The rms errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

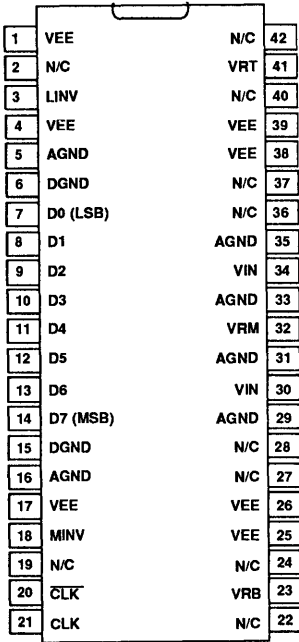
Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77100. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δf , is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

CHARACTERIZATION GRAPHS



**PIN ASSIGNMENT
HAD77100**

PIN FUNCTIONS HADC77100



NAME	FUNCTION	NAME	FUNCTION
VEE	Negative Supply Nominally -5.2V	CLK	ECL Clock Input Pin
LINV	D0 through D6 Output Inversion Control Pin	CLK	ECL Clock Input Pin
DGND	Digital Ground	VRB	Reference Voltage Bottom Nominally -2.0V
D0	Digital Data Output (LSB)	AGND	Analog Ground
D1- D6	Digital Data Output	VIN	Analog Input Can be connected to the input signal or used as Sense
D7	Digital Data Output (MSB)	VRM	Reference Voltage Tap Middle
MINV	D7 Output Inversion Control Pin	VIN	Analog Input Can be connected to the input signal or used as Sense
VRT	Reference Voltage, Top Nominally 0.0V		

**42 LEAD CERAMIC
SIDEBRAZED DIP**

**For Ordering Information See Section 1.

NOTES:

8-BIT, 150 MSPS FLASH A/D CONVERTER

FEATURES

- 150 MSPS CONVERSION RATE
- 1/2 LSB Linearity
- Preamplifier Comparator Design
- Typical Power Dissipation < 2.2 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Medical Electronics: Ultrasound, CAT Instrumentation

2

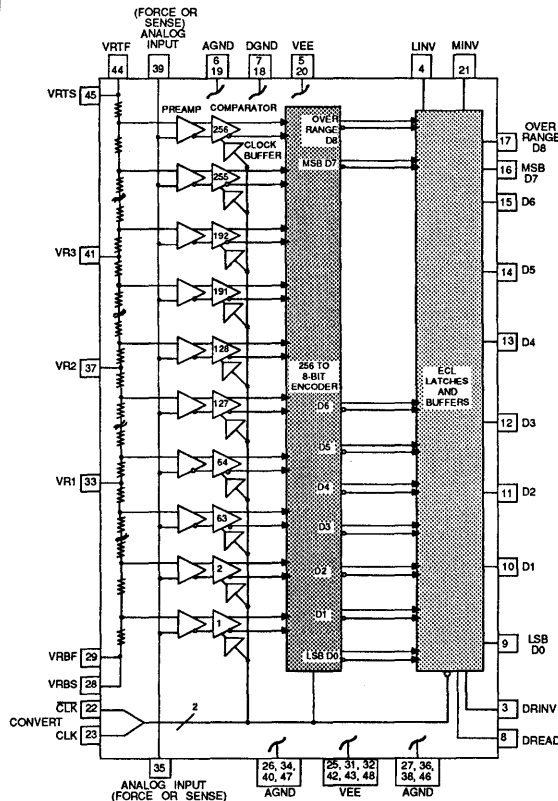
GENERAL DESCRIPTION

The HADC77200 is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components into 8-bit digital words at a 150 MSPS update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth. A single standard -5.2 Volt power supply is required for operation of the HADC77200, with nominal power dissipation of 2.2 Watts.

The part is packaged in a 48 or 42 Lead Ceramic Side-brazed DIP. The 42 Lead DIP is pin compatible with the CX20116. The HADC77200 in the 48 or 46 lead packages includes five external reference ladder TAPS to gain better control over linearity; an overrange bit for use in higher resolution systems; and a data ready output pin for ease in interfacing to high-speed memory. Careful attention to design and layout has provided a device with low noise floor, stable input characteristics, and low data error rate. The HADC77200 is available in Industrial and Military Temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25°C**Supply Voltages Output**

Negative Supply Voltage (V_{EE} TO GND) ...-7.0 to +0.5 V
 Ground Voltage Differential.....-0.5 to +0.5V

Input Voltage

Analog Input Voltage.....+0.5 to V_{EE} V
 Reference Input Voltage.....+0.5 to V_{EE} V
 Digital Input Voltage.....+0.5 to V_{EE} V
 Reference Current VRT to VRB.....25 mA
 Tap Reference Current.....-6 to +6 mA

Output

Digital Output Current.....0 to -25 mA

Temperature

Operating Temperature, ambient.....-65 to +150°C
 junction.....+150°C
 Lead Temperature, (soldering 10 seconds)....+300°C
 Storage Temperature.....-65 to +150°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS**INDUSTRIAL TEMPERATURE RANGE**

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C		HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	

**TRANSFER
CHARACTERISTICS**

Integral Linearity, 77200A		II		$\pm\frac{1}{2}$		$\pm\frac{1}{2}$		$\pm\frac{1}{2}$	LSB
Differential Linearity, 77200A		II		$\pm\frac{1}{2}$		$\pm\frac{1}{2}$		$\pm\frac{1}{2}$	LSB
Integral Linearity, 77200B		II		$\pm\frac{3}{4}$		$\pm\frac{3}{4}$		$\pm\frac{3}{4}$	LSB
Differential Linearity, 77200B (No missing codes)		II		$\pm\frac{3}{4}$		$\pm\frac{3}{4}$		$\pm\frac{3}{4}$	LSB
Offset Error VRT		II	-30	30	-30	30	-30	30	mV
Offset Error VRB		II	-30	30	-30	30	-30	30	mV

**ANALOG INPUT
CHARACTERISTICS**

Input Voltage Range		II	-2.0	0.0	-2.0	0.0	-2.0	0.0	VOLTS
Input Capacitance	Over full input range	V	45						pF
Input Resistance		V	4						k Ω
Input Current		II	300	500	450		650		μ A
Clock Synchronous Input Currents		V	40						μ A

ELECTRICAL SPECIFICATIONS

INDUSTRIAL TEMPERATURE RANGE

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $V_{RB} = -2.00V$, $V_{RT} = 0.00V$, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

POWER SUPPLIES

Supply Current		II	420	505		525		505	mA
Power Dissipation		II	2.18	2.63		2.73		2.63	watts

REFERENCE

Ladder Resistance		II	100	300	100	300	80	300	Ω
Reference Bandwidth		V		50					MHz

DIGITAL LOGIC

Output High Voltage	50 Ω to -2V	II	-0.98	-0.90	-0.82	-0.89	-0.70	-1.08	-0.91	VOLTS
Output Low Voltage	50 Ω to -2V	II	-1.95	-1.80	-1.65	-1.95	-1.65	-1.95	-1.69	VOLTS
Input High Voltage (MINV, LINV)		II	-1.13	-0.81		-1.07	-0.67	-1.27	-0.87	VOLTS
Input Low Voltage (MINV, LINV)		II	-1.95	-1.48		-1.95	-1.42	-1.95	-1.50	VOLTS

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $V_{RB} = -2.00V$, $V_{RT} = 0.00V$, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

CONVERSION TIMING, See Figure 1A

Maximum Sample Rate		IV	125	150		125		125		MSPS
Clock Low Width, TPW0		I	5	3		4		4		ns
Clock High Width, TPW1		I	5	3		4		4		
Output Delay, TD	Differential Clock	I	3	4.2	5					ns
Output Delay Tempco	Differential Clock	V		15						ps/°C
Data Ready Delay	Differential Clock	I	3	4	5					ns
Output Rise Time 20% to 80%	50 Ω to -2V	I	1.3	1.9	2.4					ns
Output Fall Time 20% to 80%	50 Ω to -2V	I	1.1	1.5	2.2					ns

ELECTRICAL SPECIFICATIONS**INDUSTRIAL TEMPERATURE RANGE**

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50%, $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

ANALOG INPUTS

Large Signal Bandwidth	$V_{in} = F.S.$	V	100						MHz
Small Signal Bandwidth	$V_{in} = 500mV PP$	V	175						MHz
Aperture Jitter		V	12						ps RMS
Aperture Delay	Differential Clock	I	0.3	1.8	2.3				ns
Aperture Delay Tempco	Differential Clock	V	4						ps/°C
Aperture Time		V	<100						ps
Acquisition Time	F.S. to $\pm 1/2$ LSB	V	5						ns
Input Slew Rate		V	800						V/ μs

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50%, $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +85°C		COLD -25°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

SIGNAL QUALITY $f_{clock} = 100MHz$

Total Dynamic Error	$V_{in} = FS @ 1MHz$	I	45	48					dB
Total Dynamic Error	$V_{in} = FS @ 25MHz$	I	36.7	38					dB
Total Dynamic Error	$V_{in} = FS @ 50MHz$	I	31	33					dB
Signal to noise ratio	$V_{in} = FS @ 1MHz$	I	46.5	49					dB
Signal to noise ratio	$V_{in} = FS @ 25MHz$	I	42.5	46					dB
Signal to noise ratio	$V_{in} = FS @ 50MHz$	I	34	38					dB
Total Harmonic Distortion	$V_{in} = FS @ 1MHz$	I	52	56					dBc
Total Harmonic Distortion	$V_{in} = FS @ 25MHz$	I	38	39					dBc
Total Harmonic Distortion	$V_{in} = FS @ 50MHz$	I	32	34					dBc
Differential Gain	NTSC 40IRE mod. ramp, $F_c = 125MSPS$	V	1.0						%
Differential Phase		V	.5						DEG

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50%, $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +125°C		COLD -55°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
TRANSFER CHARACTERISTICS										
Integral Linearity, 77200A		I	± 1 4	± 1 2		± 1 2		± 1 2		LSB
Differential Linearity, 77200A		I	± 1 4	± 1 2		± 1 2		± 1 2		LSB
Offset Error VRT		I	-30	30	-30	30	-30	30		mV
Offset Error VRB		I	-30	30	-30	30	-30	30		mV

ANALOG INPUT CHARACTERISTICS

Input Voltage Range	VRT = 0.5V VRB = -2.5V	I	-2.5	+0.5	-2.5	+0.5	-2.5	+0.5		VOLTS
Input Capacitance	Over full input range	IV	45							pF
Input Resistance		V	4							k Ω
Input Current		I	300	500		400		750		μA
Clock Synchronous Input Currents		V	40							μA

POWER SUPPLIES

Supply Current		I	420	505		535		505		mA
----------------	--	---	-----	-----	--	-----	--	-----	--	----

REFERENCE

Ladder Resistance		I	100	300	130	300	60	300		Ω
Reference Bandwidth		V	50							MHz

ELECTRICAL SPECIFICATIONS**MILITARY TEMPERATURE RANGE**

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50%, $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +125°C		COLD -55°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

DIGITAL LOGIC

Output High Voltage	50Ω to -2V	I	-0.98	-0.90	-0.82	-0.85	-0.66	-1.10	-0.95	VOLTS
Output Low Voltage	50Ω to -2V	I	-1.95	1.80	-1.65	-1.95	-1.65	-2.0	-1.70	VOLTS
Input High Voltage (MINV, LINV)		I	-1.13		-0.81	-1.07	-0.67	-1.27	-0.87	VOLTS
Input Low Voltage (MINV, LINV)		I	-1.95		-1.48	-1.95	-1.42	-1.95	-1.50	VOLTS

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +125°C		COLD -55°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

CONVERSION TIMING (See Figure1A)

Maximum Sample Rate		I	100	150		100		100		MSPS
Clock Low Width, TPW0		I	5	3		5		5		ns
Clock High Width, TPW1		I	5	3		5		5		ns
Data Ready Delay, TD		I	3	4	5	3.8	7	3.5	4.5	ns
Output Delay, TD	Differential Clock	I	3	3.4	5	4	7	3	4.5	ns
Output Rise Time (20% to 80%)	50Ω to -2V	I	1.3	1.9	2.4	1.3	4	0.5	2.2	ns
Output Fall Time (20% to 80%)	50Ω to -2V	I	1.1	1.5	2.2	1.1	4	0.5	2.2	ns

ANALOG INPUTS

Aperture Jitter		V		12						ps RMS
Aperture Delay	Differential Clock	I	0.3	1.2	2.3	0.3	2.8	0.3	2.0	ns
Aperture Time		V		<100						ps
Settle-to-Hold Time		V		5						ns
Aperture Delay Tempco	Differential Clock	V		4						ps/°C

ELECTRICAL SPECIFICATIONS

MILITARY TEMPERATURE RANGE

$V_{EE} = -5.2V$, $R_{Source} = 10\Omega$, $f_{clock} = 100MHz$, Duty Cycle = 50%, $VRB = -2.00V$, $VRT = 0.00V$, Unless otherwise specified

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	ROOM +25°C			HOT +125°C		COLD -55°C		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	

SIGNAL QUALITY $f_{clock} = 100MHz$

Total Dynamic Error	$V_{in} = FS @ 1MHz$	I	45	48	44.2	44.2	dB
Total Dynamic Error	$V_{in} = FS @ 25MHz$	I	36.7	38	36.2	36.2	dB
Total Dynamic Error	$V_{in} = FS @ 50MHz$	I	31	33	29.2	29.2	dB
Signal to noise ratio	$V_{in} = FS @ 1MHz$	I	46.5	49	45	45	dB
Signal to noise ratio	$V_{in} = FS @ 25MHz$	I	42.5	46	41	41	dB
Signal to noise ratio	$V_{in} = FS @ 50MHz$	I	34	38	32.5	32.5	dB
Total Harmonic Distortion	$V_{in} = FS @ 1MHz$	I	52	56	50.5	52	dBc
Total Harmonic Distortion	$V_{in} = FS @ 25MHz$	I	38	39	36.5	38	dBc
Total Harmonic Distortion	$V_{in} = FS @ 50MHz$	I	32	34	30.5	32	dBc

TEST LEVEL CODES

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested, at the specified condition.

TEST LEVEL

TEST PROCEDURE

I	100% production tested at the specified temperatures.
II	100% production tested at $T_a = 25^\circ C$, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

GENERAL DESCRIPTION

The HADC77200 is the fastest monolithic 8-bit parallel flash A/D converter available today. The minimum conversion rate is 150 MSPS and the analog bandwidth is in excess of 70 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This reduces clock transient kickback to the input and reference ladder. The preamplifiers also add a gain of six to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces meta-stable states that can cause errors at the output.

An additional advantage of the HADC77200 over similar devices is a better integral linearity specification over the part's entire usable range.

The specification is improved from 1/2 LSB to 1/4 LSB. The center reference ladder tap is optional as needed to further decrease this specification.

The HADC77200 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. Furthermore, the HADC77200 has an on-board power supply bypass of 1500pF to reduce external component needs, and the output drive capability of the device can provide full ECL swings into 50Ω loads.

TYPICAL INTERFACE CIRCUIT

The HADC77200 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the

best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in Figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. The function of each pin and external connections to other components are as follows:

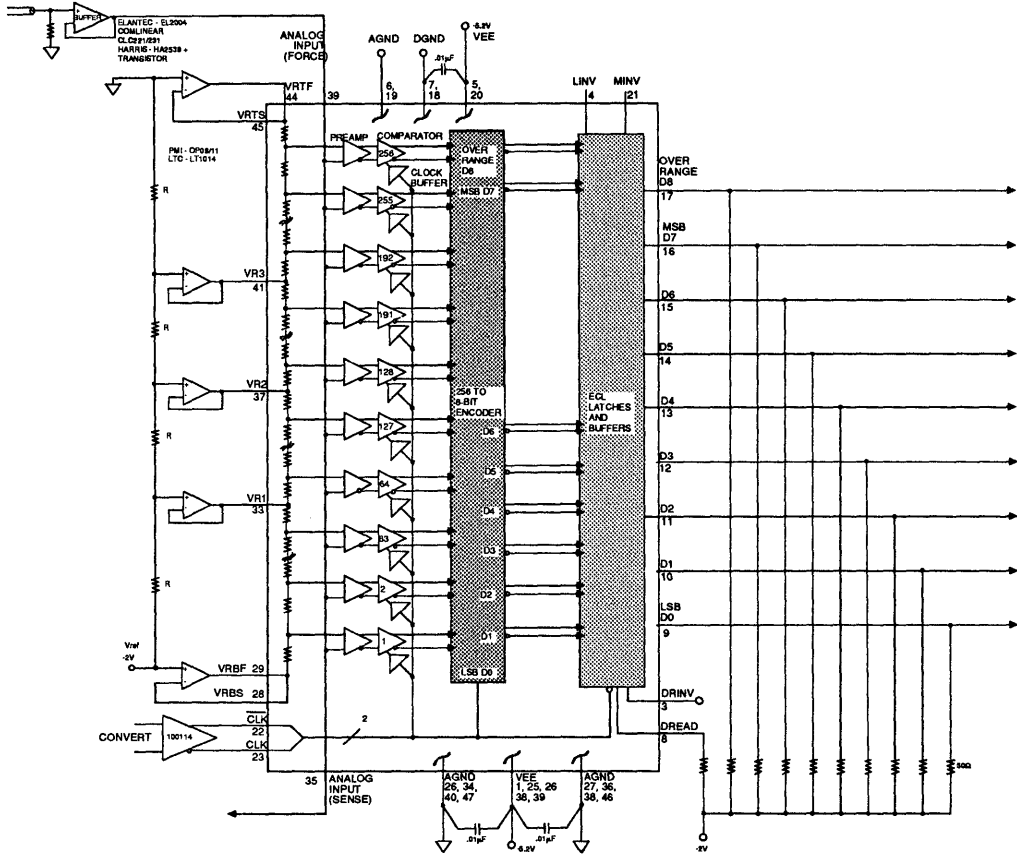
VEE, AGND, DGND

VEE is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01μF ceramic capacitor. A 1μF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in Figure 1.

VIN (Analog Input)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input "sense" and the other for input "force". This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The HADC77200 is superior to similar devices due to a preamplifier stage before the comparators. If an input buffer is needed, a Harris HA2540 may be used in conjunction with an output transistor buffer for lower frequency applications. For higher frequencies, another option is to use an Elantec EL2004 video buffer or an HA2539 and a 2N5836 transistor. Very high performance can be achieved by using a Comlinear CLC221/231.

FIGURE 1 HADC77200 TYPICAL INTERFACE CIRCUIT



CLK, CLK (Clock Inputs)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since CLK is internally biased to -1.3V (see clock input circuit on page 12). It may be left open but a .01µF bypass capacitor from CLK to AGND is recommended. The duty cycle of the clock is not important as long as minimum pulse width is maintained.

MINV, LINV (Output Logic Control)

These are digital controls for changing the output code from straight binary to two's complement, etc. For more information, see Table 1. Both MINV and LINV are in the logic "low" (0) state when they are left open. The "high" state can be obtained by tying to AGND through a diode or 3.9kΩ resistor.

D0 to D7 (Digital Outputs)

The digital outputs can drive 50Ω to ECL levels when pulled down to -2V. When pulled down to -5.2V the outputs can drive 130Ω to 1KΩ loads.

VRBF, VRBS, VR1, VR2, VR3, VRTF, VRTS (Reference Inputs)

These are five external reference voltage taps from -2V (VRB) to AGND (VRT) which can be used to control integral linearity over temperature. The TAPS can be driven by Op amps as shown in Figure 1. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired. VRB and VRT have "force" and "sense" pins for monitoring the top and bottom voltage references.

DREAD (Data Ready), DRINV (Data Ready Inverse)

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the HADC77200's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin. Timing is shown in Figure 1A.

D8 (Overrange)

This is an overrange function. When the HADC77200 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the HADC77200 into higher resolution systems.

N/C

All "Not Connected" pins should be tied to AGND.

TABLE 1 - OUTPUT CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.
.
V _{IN}	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.
.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

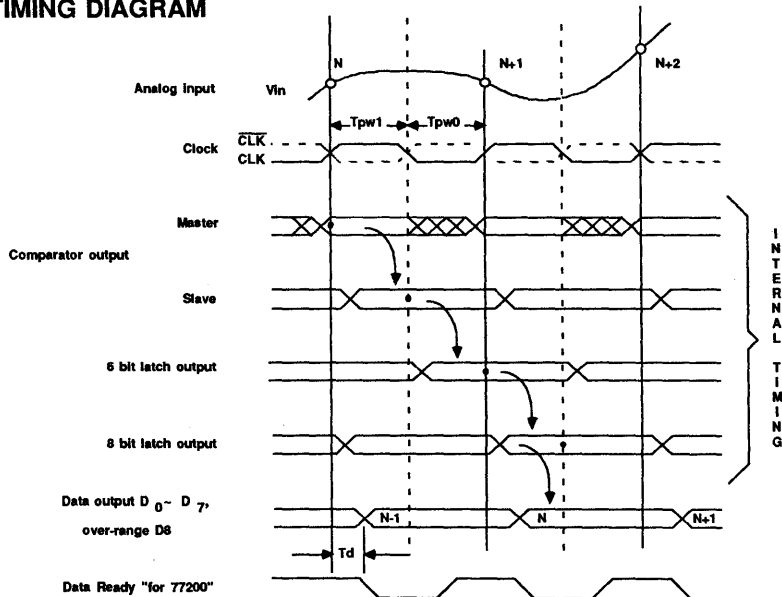
1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

OPERATION

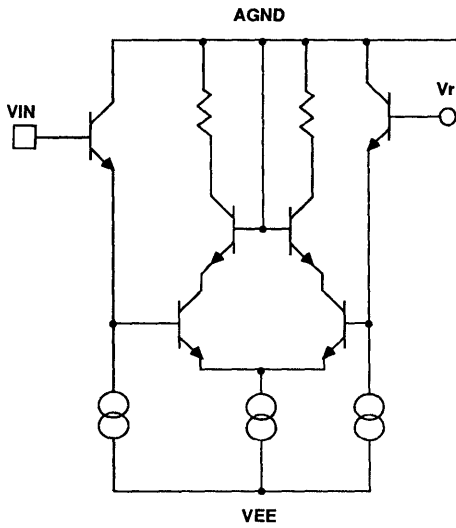
The HADC77200 has 256 preamp/comparator pairs which are each supplied with the voltage from VRT to VRB divided equally by the resistive ladder as shown in the block diagram on page 1. This voltage is applied to the positive input of each preamplifier and comparator pair. An analog input voltage applied at VIN is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to VRT(0V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from four columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions and they consist of a set of eight XOR gates. Finally, eight ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

FIGURE 1A - TIMING DIAGRAM

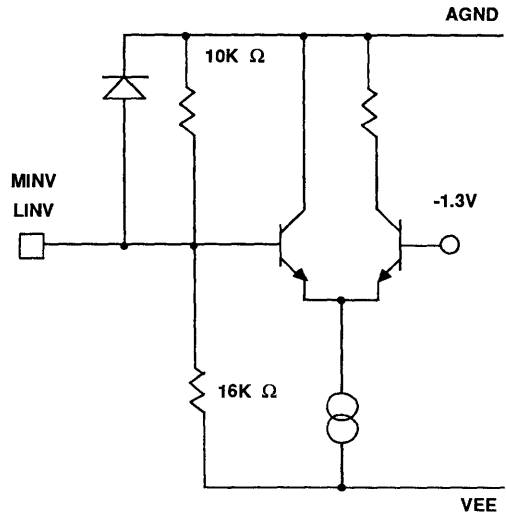


Dots (•) in the chart denote respective latch timings.

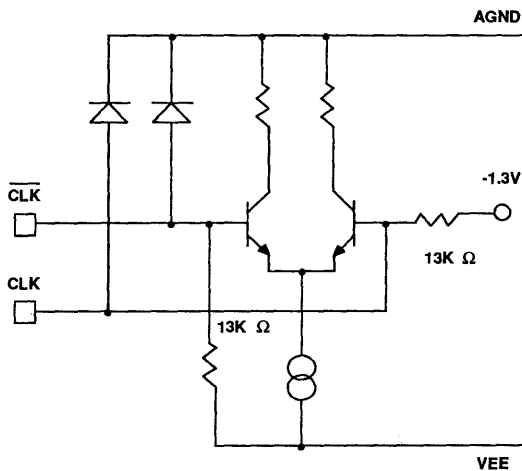
INPUT CIRCUIT



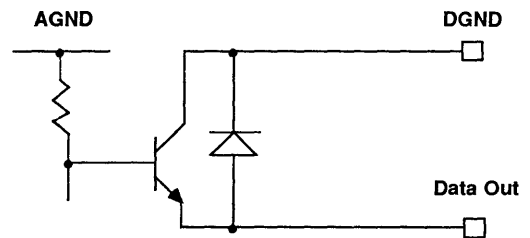
DRINV, MINV, LINV INPUT CIRCUIT



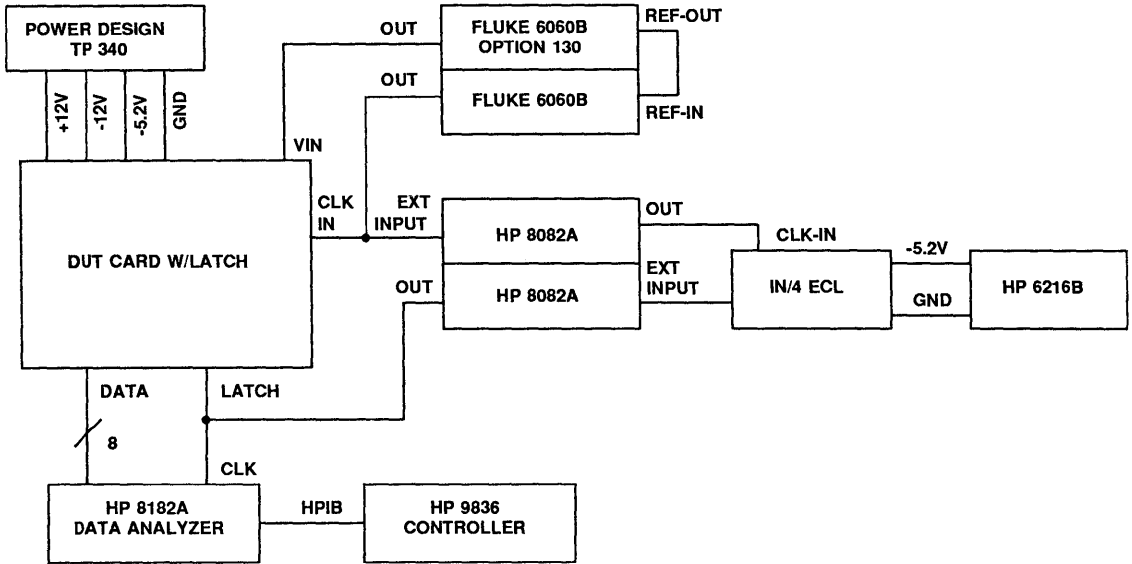
CLOCK INPUT



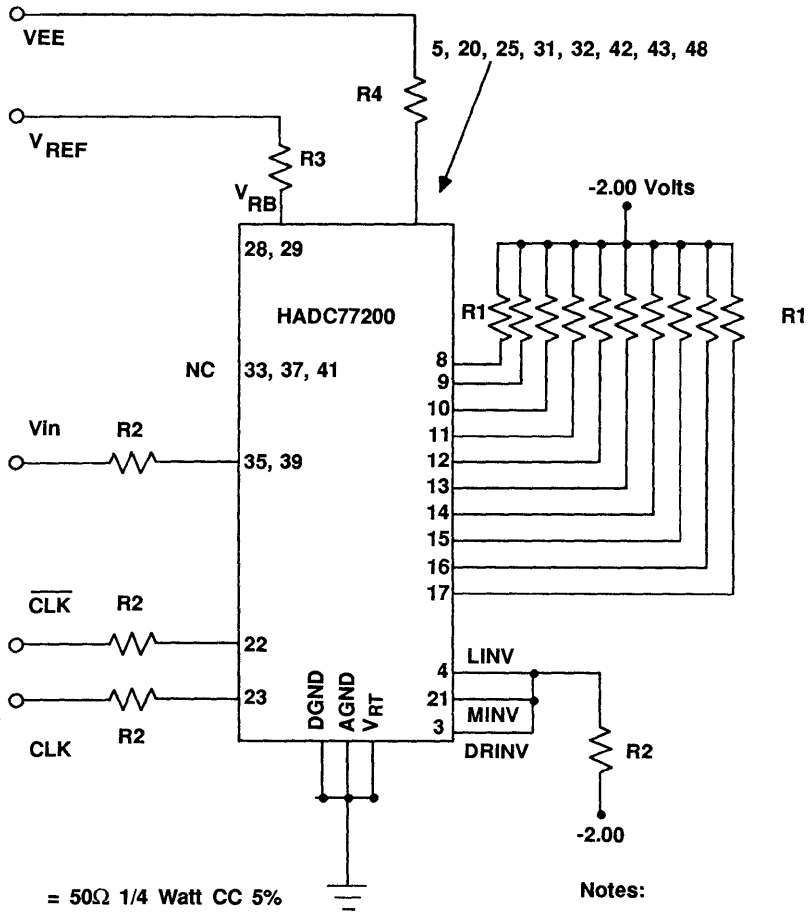
OUTPUT CIRCUIT D0 THROUGH D8, DREAD



DYNAMIC EVALUATION



BURN-IN CIRCUIT $T_{CASE} = 125^{\circ}C$



- R1 = 50Ω 1/4 Watt CC 5%
- R2 = 1KΩ 1/4 Watt CC 5%
- R3 = 6.5Ω 1/4 Watt CC 5%
- R4 = 3.25Ω 1/2 Watt CC 5%
- $V_{REF} = -2.00$ Volts
- $V_{EE} = -6.6$ Volts

Notes:

1. Pin numbers refer to dip packages

DEFINITION OF TERMS

SPECIFICATIONS

A/D CONVERTER ERROR SUMMARY

Honeywell SPT realizes that the transfer function for an A/D converter is very dependent upon the slew rate of the signal it is digitizing. The transfer function under dynamic conditions may exhibit numerous errors (Figure 2B) while a static dc input level may appear close to the ideal (Figure 2A). That is why we are including many dynamic tests as well as the the industry standard dc specifications.

EFFECTIVE BITS (SNR)

This is the difference between the measured data at the output of an A/D converter in response to a sinewave and an ideal sinewave's data best fitted to the measured data. The data is then plotted as usable (effective) output bits versus frequency. This is the most important specification since it is tested over the entire frequency range of the part and shows true dynamic performance. It also indicates the cumulative effect of many error sources. These are quantization error, dynamic differential nonlinearity, missing codes, integral nonlinearity, total harmonic distortion, aperture uncertainty and noise. Not included are DC specifications such as offset and gain errors. The result is calculated from measured rms error for the ideal sinewave and the measured actual rms error as follows:

$$\text{eff bits} = 8 - \log_2 \frac{\text{actual rms error}}{\text{ideal rms error}}$$

Furthermore, signal-to-noise ratio (SNR) can be related to effective bits by the following formula:

$$\text{SNR(dB)} = 1.8 + 6.02 \times N(\text{eff bits})$$

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). An 8-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^8 (1 part in 256). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q = \text{FSR}/2^N$ where FSR = full scale range and $N = 8$. Non-ideal quantization bands represent differential nonlinearity errors (See Figures 2A and 2B).

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 2B shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC77200's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on that part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB, which results in a differential nonlinearity of -1 LSB. Figure 2B points out two missed codes in the transfer function.

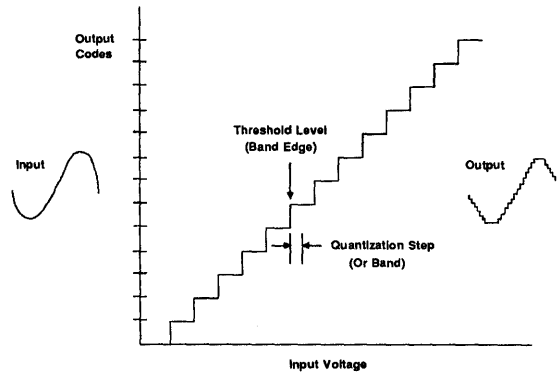


Figure 2A Static Input Conditions

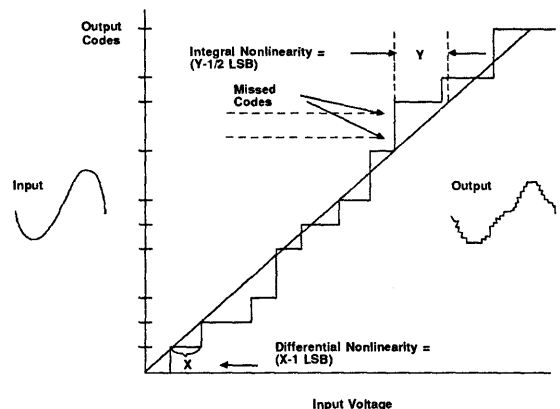


Figure 2B Dynamic Conditions

SPECIFICATIONS CONTINUED

INTEGRAL NONLINEARITY

Integral nonlinearity is the maximum deviation of the A/D transfer function from a best fit straight line (Figure 3A). Integral nonlinearity does not include any gain and offset errors. Integral nonlinearity in an A/D is generally more detrimental when digitizing full scale signals than low level signals which may fall on a part of the transfer function which is relatively linear. Figure 2B shows an integral nonlinearity error of 2 LSB. The HADC77200's integral nonlinearity can be improved by using the external reference ladder taps as shown in Figure 1. The resulting effect on the linearity is shown in Figure 3B.

APERTURE UNCERTAINTY

Aperture uncertainty is the time jitter in the sample point and is caused by short term stability errors in the timebase generating the sample (encode) command to the A/D converter. The approximate voltage error due to aperture uncertainty depends on the slew rate of the signal at the sample point. See Figure 3C.

As in any sampled data system, the aperture width affects the accuracy of the system. The aperture time can be considered an amplitude uncertainty for any input where the voltage is changing. The magnitude of this change for a sine wave can be calculated for time or voltage by the equation:

$$dV/V = 2\pi f t_a$$

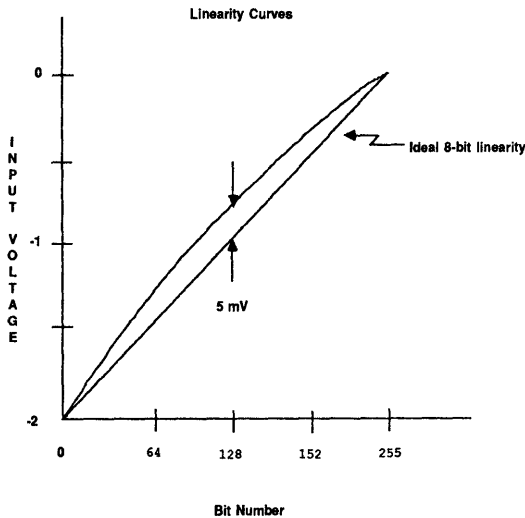


FIGURE 3A Linearity Curve with no TAP adjustment

By calculating the aperture time for a given system accuracy and comparing it to the aperture time specification of the flash converter, the need for a track and hold can be determined. The graph in Figure 4 summarizes required aperture time for 8-bit resolution high speed converters using sinusoidal frequencies.

An example using an 8-bit flash converter follows. If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10MHz, then from Figure 4 it can be determined that to assure less than 8-bits of error due to aperture alone, the A/D converter must have an aperture time of less than 70ps. Most data sheets do not state aperture time so usually a sample and hold is used. Unfortunately, the sample and holds generally available today are not faster than 70ps.

Aperture time and delay are very difficult to measure, however these values are needed to make intelligent design decisions. Honeywell SPT supplies these values for the HADC77200 based on both computer design simulations and verified by characterization of samples.

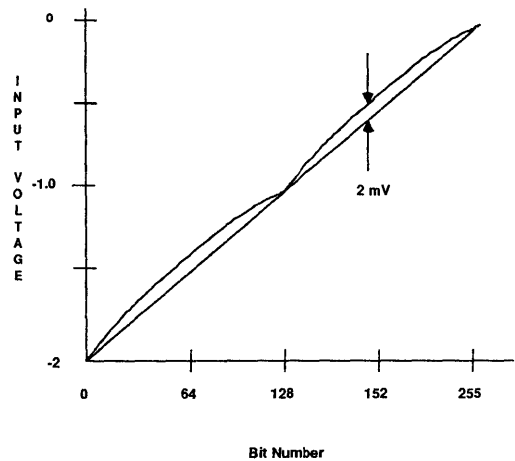


FIGURE 3B Linearity Curve with TAPS Forced to Within .5mV of Ideal

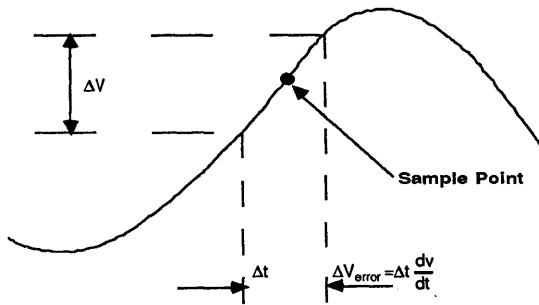


FIGURE 3C Aperture Uncertainty

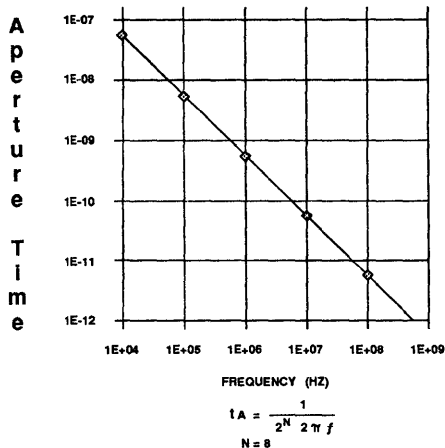
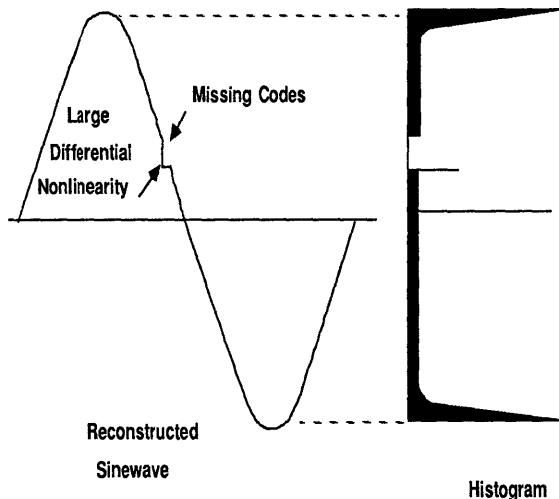


FIGURE 4 Aperture Time - Sinewaves



In the histogram test, A/D transfer function step widths larger than ideal show up as "spikes" in the histogram. Codes missing from the transfer function show up as "bins" with zero counts.

FIGURE 5 Histogram Testing

CHARACTERISTIC TESTING

TESTING

All of the following tests can be performed using Hewlett-Packard equipment as referred to in H.P. Product Note 5180A-2. Test methods available to measure the previous specifications are explained as follows and listed in Table 2.

HISTOGRAM TESTING

In histogram testing, a full scale sinewave of specified frequency is input to the HADC77200. The frequency of the sinewave is selected to be non-coherent with the sample rate of the A/D converter. Several hundred thousand samples of the signal are taken and processed into a histogram. At the end of the sampling, the histogram is plotted with possible output codes along the x-axis and frequency of occurrence along the y-axis. Above each possible output code (the x-axis is from 0 to 256), a point is plotted whose height is proportional to the total number of times that code occurs. For a sinewave input, a perfect A/D converter would produce a cusp probability density function described by the equation:

$$p(V) = \frac{1}{\pi(A^2 - V^2)^{-1/2}}$$

where A is the peak amplitude of the sinewave and p(V) is the probability of an occurrence at a voltage V. If a particular step is wider than the ideal width, then the code associated with that step will have accumulated more "counts" than a code corresponding to the ideal step. A step narrower than the ideal width will accumulate fewer counts. Missing codes are readily apparent because a missing code will show zero counts (See Figure 5).

FAST FOURIER TRANSFORM TESTING

The Discrete Fourier Transform (DFT) is another useful tool for evaluating A/D converter dynamic performance. Implemented using a Fast Fourier Transform algorithm, the DFT converts a finite time sequence of sampled data into the frequency domain. From the frequency domain representation of the data, the linearity of the A/D converter's dynamic transfer function may be measured. Harmonics of the input sine-wave, caused by the integral nonlinearity, are aliased

SPECIFICATION TESTING CONTINUED:

into the baseband spectrum and can be readily identified and measured. Additional effects can be measured as shown in Table 2.

SINEWAVE CURVE FITTING

In the sinewave curve fit test, a full scale sinewave of specified frequency is digitized by the HADC77200. Using least squared error minimization techniques, an idealized sinewave fit to the data is calculated by software. The sinewave is in the form:

$$A\sin(2\pi ft + \theta) + DC$$

where A, f, θ , DC are the parameters which are selected for a best fit to the data. The idealized best fit sinewave, $A_0\sin(2\pi f_0 t + \theta_0) + DC_0$ is then subtracted from the digitized time record.

The rms errors are then calculated and the effective bits specification is found.

BEAT FREQUENCY TEST

Beat frequency testing is a qualitative test for A/D converter dynamic performance and may be used to quickly judge whether or not there are any gross problems with the HADC77200. In this technique, a full scale sinewave input signal is offset slightly in frequency from the A/D converters sample rate. This frequency offset is selected such that on successive cycles of the input sinewave, the A/D's output ideally would change by 1 LSB at the point of maximum slope. Thus the A/D sample point "walks" through the input signal. When the data stored in memory is reconstructed using a low speed DAC, the beat frequency, Δf , is observed. Differential nonlinearities show up as nonuniform horizontal lines in the observed beat frequency waveform and missing codes show up as gaps.

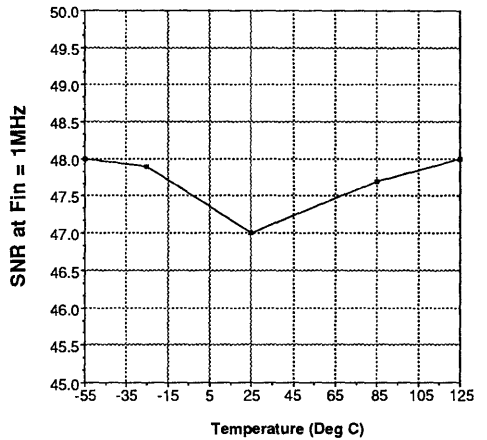
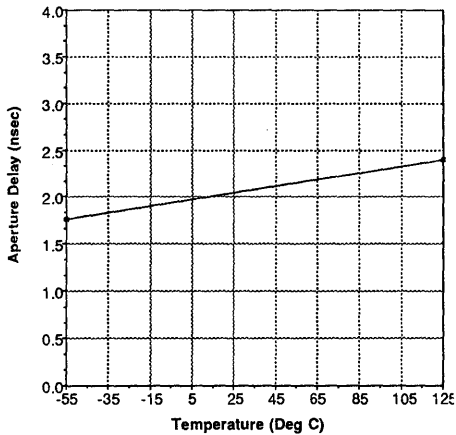
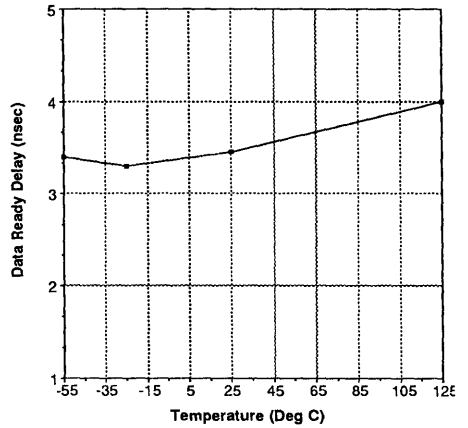
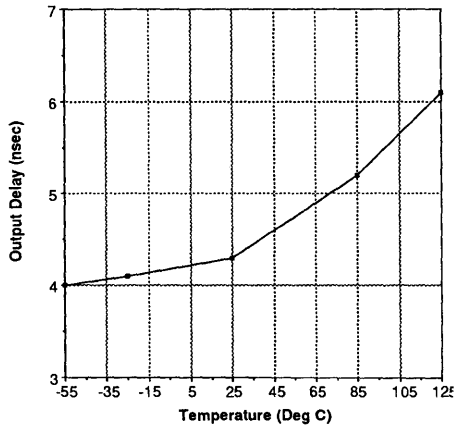
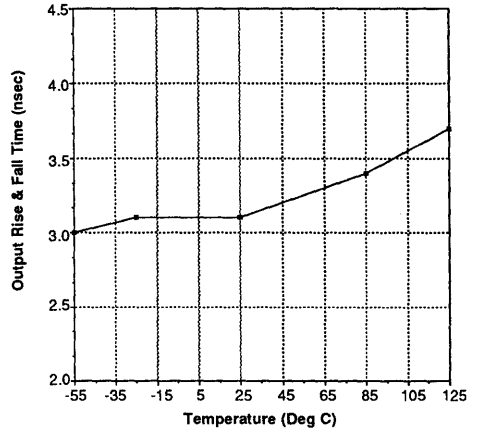
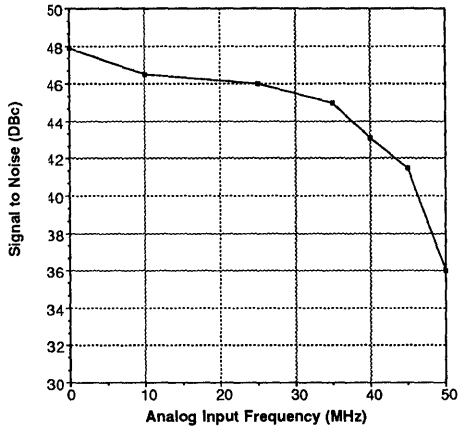
**TABLE 2
TESTS**

The following table summarizes the dynamic performance tests previously described and the dynamic errors which influence test results.

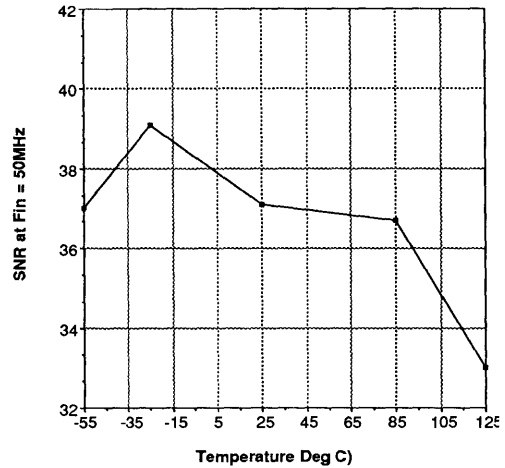
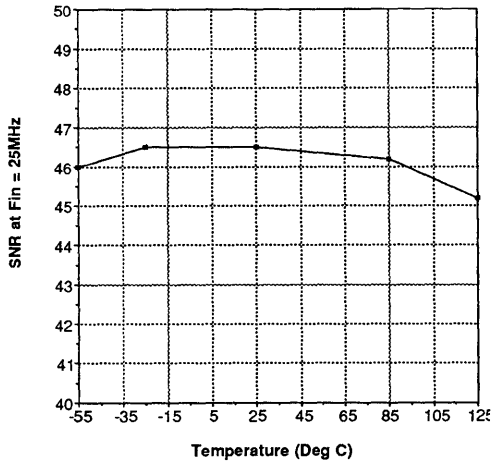
(Table from H. P. Product Note 5180A-2)

ERROR	HISTOGRAM	FFT	SINEWAVE CURVE FIT	BEAT FREQUENCY TEST
Differential Nonlinearity	Yes-shows up as spikes	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Missing Codes	Yes-shows up as bins with 0 counts	Yes-shows up as elevated noise floor	Yes-part of RMS error	Yes
Integral Nonlinearity	Yes (could be measured directly with highly linear ramp waveform)	Yes-shows up as harmonics of fundamental aliased into baseband	Yes-part of RMS error	Yes
Aperture Uncertainty	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Noise	No-averaged out. Can be measured with "phase locked" histogram.	Yes-shows up as elevated noise floor	Yes-part of RMS error	No
Bandwidth Errors	No	No	No	Yes-used to measure analog bandwidth.
Gain Errors	Yes-shows up in peak to peak of distribution.	No	No	No
Offset Errors	Yes-shows up in offset of distribution average.	No	No	No

CHARACTERIZATION GRAPHS



CHARACTERIZATION GRAPHS (con't.)



PIN ASSIGNMENT HADC77200

1	N/C	VEE	48
2	N/C	AGND	47
3	DRINV	AGND	46
4	LINV	VRTS	45
5	VEE	VRTF	44
6	AGND	VEE	43
7	DGND	VEE	42
8	DREAD	VR3	41
9	D0 (LSB)	AGND	40
10	D1	VIN	39
11	D2	AGND	38
12	D3	VR2	37
13	D4	AGND	36
14	D5	VIN	35
15	D6	AGND	34
16	D7 (MSB)	VR1	33
17	D8 (OVERRANGE)	VEE	32
18	DGND	VEE	31
19	AGND	N/C	30
20	VEE	VRBF	29
21	MINV	VRBS	28
22	CLK	AGND	27
23	CLK	AGND	26
24	N/C	VEE	25

NAME	FUNCTION	NAME	FUNCTION
VEE	Negative Supply Nominally -5.2V	CLK	ECL Clock Input Pin
LINV	D0 through D6 Output Inversion Control Pin	CLK	ECL Clock Input Pin
DREAD	Data Ready Output	DRINV	Data Ready Inverse
DGND	Digital Ground	VRBS	Reference Voltage Bottom, Sense, Nominally -2.0V
AGND	Analog Ground	VRBF	Reference Voltage Bottom, Force, Nominally -2.0V
D0	Digital Data Output Pin 1 (LSB)	VIN	Analog Input, connected to the input signal or used as Sense
D1- D6	Digital Data Output Pin 2 through Pin 6	VR1	Reference Voltage Tap 1
D7	Digital Data Output Pin 7 (MSB)	VR2	Reference Voltage Tap 2
D8	Overrange Output	VR3	Reference Voltage Tap 3
MINV	D7 Output Inversion Control Pin	VRTS	Reference Voltage Top, Sense, Nominally -2.0V
		VRTF	Reference Voltage Top, Force, Nominally -2.0V

48 LEAD CERAMIC SIDEBRAZED DIP

**For Ordering Information See Section 1.

NOTES:

10-BIT, 50 MSPS FLASH ANALOG TO DIGITAL CONVERTER

PRELIMINARY INFORMATION

FEATURES:

- Output Glitches Eliminated
- Trimmed to $\pm 3/4$ LSB
- On-Chip Input Buffer Amplifier
- Internal Gray Coded Logic for Low Noise
- Pre-amplifier/Comparator Inputs

APPLICATIONS:

- Radar
- Digital Oscilloscopes
- Video Equipment
- Spectrum Analyzers
- Medical Imaging



GENERAL DESCRIPTION

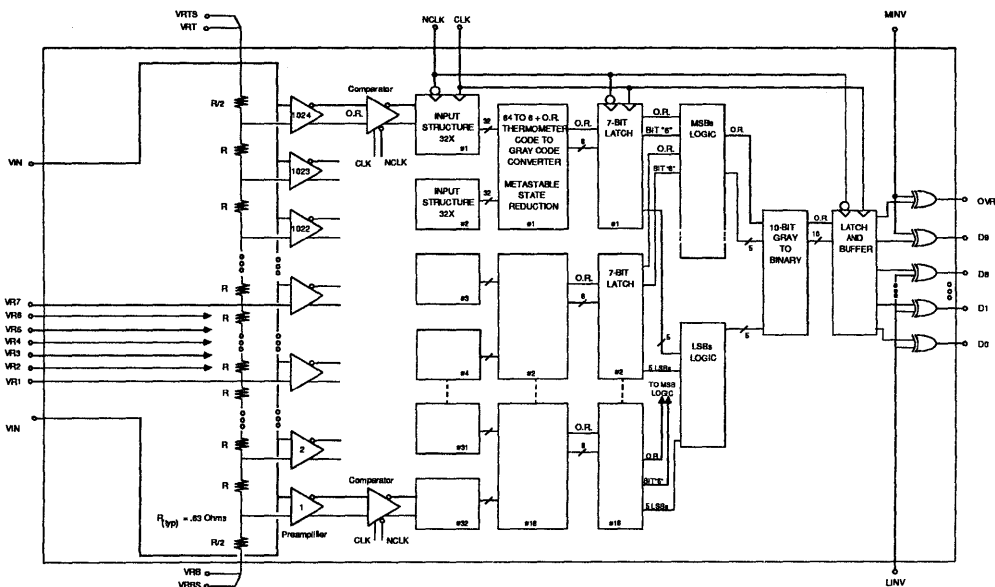
The HADC77600 is a monolithic 10-bit parallel A/D converter. The sample rate can be set up to 50MSPS (75MSPS TYPICAL) for digitizing signals up to 25MHz. The full scale input range is -1.5 to +1.5 Volts.

The HADC77600 has a wide bandwidth to allow it to be used in many applications without a track and hold. If a track and hold is required for the application, the converter has excellent step response. New design techniques have been used to eliminate random errors commonly found in flash converters.

Glitches and metastable states have been reduced to the 1 LSB level. This provides a great advantage to designers of single event detection systems for better performance than previously possible.

The device is packaged in a 72-lead Pin Grid Array (PGA) that includes on board power supply bypass capacitors equivalent to 120pF on the VEE and VCC supply pins. Power dissipation is only 4.7 Watts, and operation is guaranteed over both the commercial and military temperature ranges.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS 25°C (1)

Supply Voltages

Positive Supply Voltage (VCC to AGND).....+6.0 to -0.5V
 Negative Supply Voltage (VEE to AGND).....-6.0 to+0.5V
 GND Voltage Differential (AGND to DGND).. +0.5 to -0.5V

Input Voltages

Data, Controls (ECL, measured to AGND).....+0.5 to VEE
 Analog (VIN).....+/-1.5V for +/-1.5V Ref

Output

Applied Voltage..... -8V to +.4V

Temperature

Temperature, ambient.....-60 to +140°C
 , junction..... +150°C
 Lead Temperature (soldering 10 seconds)....+300°C
 Storage Temperature.....-65 to +150°C

Note: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

VCC = +5.0V, VEE = -5.2V, VBIAS = +2.0V, fCLOCK = 50MHz, VRT= 1.5V, VRB= -1.5V, unless otherwise specified.

DC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C		Hot +70°C		Cold -25°C		Units
			Min	Typ Max	Min	Typ Max	Min	Typ Max	
TRANSFER CHARACTERISTICS									
Integral Linearity				±1					LSB
Differential Linearity				±3/4					LSB
Offset Error VRT				-15					mV
Offset Error VRB				15					mV
ANALOG INPUT CHARACTERISTICS (ADC)									
Input Voltage Range			-1.5	+1.5	-1.5	+1.5	-1.5	+1.5	Volts
Input Capacitance				300					pF
Input Current	AT Vin = 0Volts			1.0					mA
Input Resistance				20					K Ohms
Clock Synchronous Input Currents				50					µA

ELECTRICAL SPECIFICATIONS

VCC = +5.0V, VEE = -5.2V, VBIAS = +2.0V, fCLOCK = 50MHz, VRT = 1.5V, VRB = -1.5V, unless otherwise specified.

DC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C		Hot +70°C		Cold -25°C		Units
			Min	Typ	Min	Typ	Max	Min	

POWER SUPPLY CHARACTERISTICS

Positive Supply Current				440					mA
Negative Supply Current				380					mA
Bias Supply Current				130					mA
Power Dissipation				4.7					Watts

REFERENCE CHARACTERISTICS

Positive Reference Voltage				+2.5					Volts
Negative Reference Voltage				-2.5					Volts
Reference Current				6					mA
Reference Tap Currents				0.4	1				mA
Ladder Resistance				650					Ohms
Reference Bandwidth				10					MHz

DIGITAL LOGIC CHARACTERISTICS

Output High Voltage	75 Ohms to -2V		-0.98	-0.91	-0.89	-0.70	-1.10	-0.87	Volts
Output Low Voltage	75 Ohms to -2V		-1.95	-1.65	-1.95	-1.57	-1.95	-1.65	Volts
Input High Voltage			-1.13	-0.81	-1.07	-0.67	-1.27	-0.87	Volts
Input Low Voltage			-1.95	-1.48	-1.95	-1.42	-1.95	-1.50	Volts

AC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C		Hot +70°C		Cold -25°C		Units
			Min	Typ	Max	Min	Typ	Max	

CONVERSION TIMING CHARACTERISTICS

Maximum Sample Rate			50	75					MSPS
Clock Width (tPW)	Figure 1		10						ns
Output Latency				1					Cycle
Output Delay (tD)			5	TBD		8	2		ns
Acquisition Time	Figure 2; Full Scale to .1%		20						ns
Aperture Jitter			12						psRMS
Aperture Delay (tAP)			5						ns

(1) See page 4.

ELECTRICAL SPECIFICATIONS

VCC = +5.0V, VEE = -5.2V, VBIAS = +2.0V, fCLOCK = 50MHz, VRT = 1.5V, VRB = -1.5V, unless otherwise specified.

AC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C		Hot +70°C		Cold -25°C		Units
			Min	Typ	Max	Min	Typ	Max	
SIGNAL QUALITY CHARACTERISTICS (f_{clock} = 50MHz)									
Total Harmonic Distortion	VIN = FS @ 1 MHz			60					dB
Total Harmonic Distortion	VIN = FS @ 5 MHz			TBD					dB
Total Harmonic Distortion	VIN = FS @ 10 MHz			TBD					dB
Signal to Noise Ratio	VIN = FS @ 1 MHz			62					dB
Signal to Noise Ratio	VIN = FS @ 5 MHz			TBD					dB
Signal to Noise Ratio	VIN = FS @ 10 MHz			TBD					dB
Total Dynamic Error	VIN = FS @ 1MHz			TBD					
Total Dynamic Error	VIN = FS @ 5MHz			TBD					
Total Dynamic Error	VIN = FS @ 10MHz			TBD					
Gain Flatness									
Noise Power Ratio									
Differential Gain	NTSC 140 IRE Mod. Ramp f _{clock} =13.5MHz			TBD					
Differential Phase				TBD					

(1) All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level Column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition. Unless otherwise noted, all tests performed after a three minute power soak.

Test Level I - 100% production tested at the specified temperatures.

Test Level II - 100% production tested at Ta=25°C and sample tested at the specified temperatures.

Test Level III - QA sample tested only at the specified temperatures.

Test Level IV - Parameter is guaranteed (but not tested) by design and characterization data.

Test Level V - Parameter is a typical value for information purposes only.

FIGURE 1. CONVERSION TIME CHARACTERISTICS

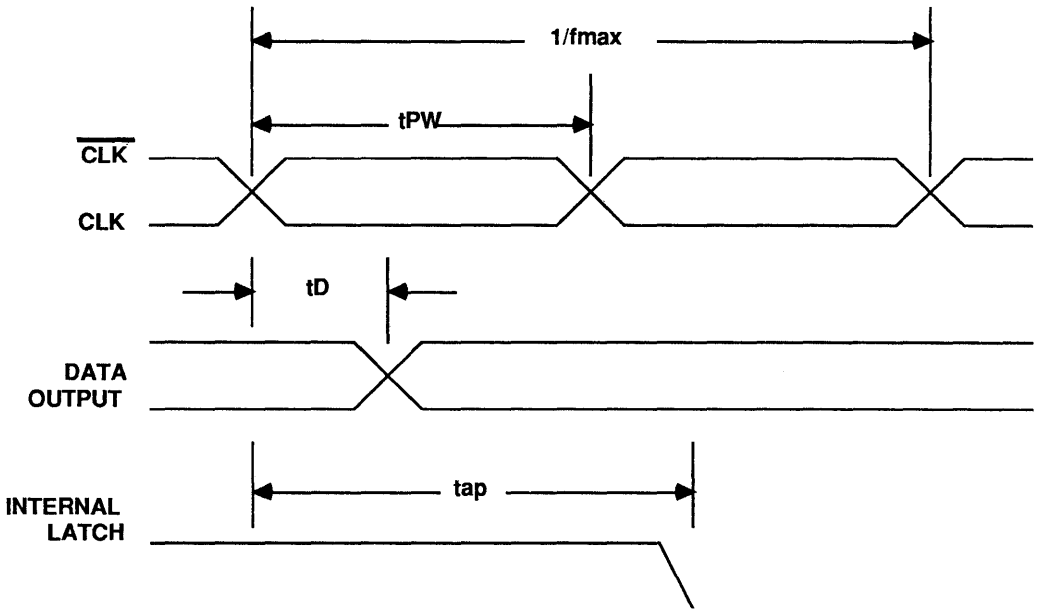
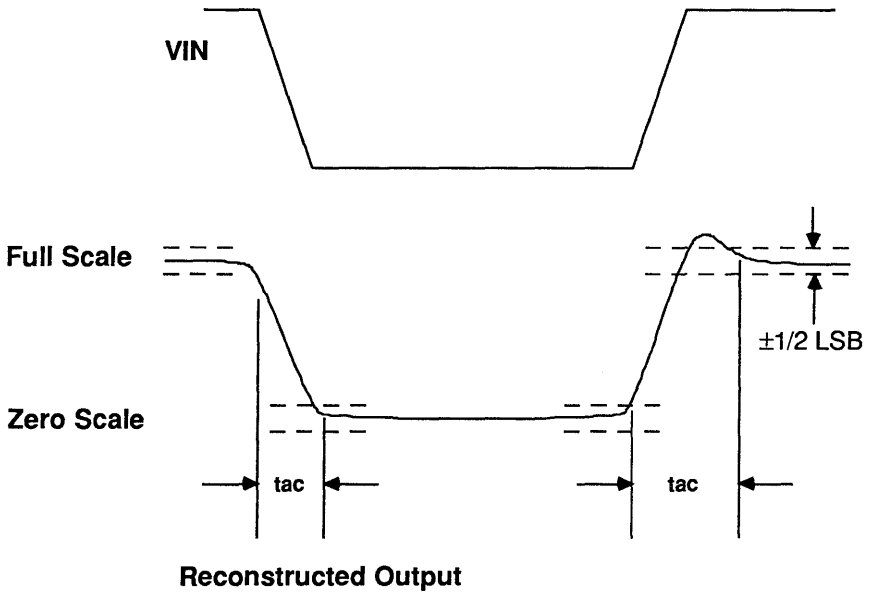


FIGURE 2. ACQUISITION TIME IS WORST CASE VALUE



DESCRIPTION

The HADC77600 is a full parallel 10-bit, 50MSPS (75MSPS Typical) flash converter with linearity trimmed to $\pm 3/4$ LSB and random error reduction to the LSB level. It is designed with preamplifier inputs to each comparator and has an on-chip input amplifier. Linearity is trimmed to better than $\pm 3/4$ LSB without affecting temperature performance or reliability. Data sheet specifications include both time and frequency domain data to assist the designer in making accurate predictions of system performance.

TRIMMING

The linearity of the HADC77600 is capable of being trimmed to at least $\pm 3/4$ LSB. The trimming is accomplished by adjusting each of the comparator offsets that is off by greater than $3/4$ LSB. The trim sites are set for bipolar adjustments so that either direction of offset is capable of being trimmed. Adjustments are done in discrete steps on metal link sites. This method of trimming completely removes resistors from the circuit. This results in a trim that does not affect either reliability of long-term stability. Stability and reliability are not effected because current carrying structures are not altered, they are either left in the circuit or they are completely removed. The resistor ladder is not altered in any manner.

ERROR REDUCTION

All flash converters prior to the HADC77600 exhibit random errors that are called metastable states or sparkle codes. These errors have the possibility of occurring at any speed or at any code. A similar error is signature error, commonly referred to as glitches. They are most likely to appear at mid, quarter or eighth scale points and the possibility of these errors increases as the input frequency increases. The latter is especially true at the very highest input frequencies that the part is capable of accepting, while random errors increase with clock frequency at a rate that appears to be exponential.

The HADC77600 addresses this problem in a new manner. First a Gray code is used to decrease the internal data synchronous noise. The Gray code also allows the addition of circuitry after the comparators to eliminate errors. The error detection is accomplished by looking for the thermometer code output from the comparators and making an error detection decision based on the comparator outputs.

This thermometer code should have the specific form of all comparators being in either a "0" or a "1" state, and all codes above a certain point should be zeroes and all below should be ones. If this does not occur then an error will be detected. Once an error is detected, the logic looks at a number of codes near the error code or codes, and makes a logical decision of what the correct

TABLE 1. LOGIC TABLE

Data Format: OVR, D9, D8, D7 through D0

MINV LINV	0 0	0 1	1 0	1 1
>+1.998V	1 1111111111	1 1000000000	0 0111111111	0 0000000000
+1.996V	0 1111111111	0 1000000000	1 0111111111	1 0000000000
+1.992V	0 1111111110	0 1000000001	1 0111111110	1 0000000001
0.0V	0 1000000000	0 1111111111	1 0000000000	1 0111111111
-0.004V	0 0111111111	0 0000000000	1 1111111111	1 1000000000
-1.996V	0 0000000001	0 0111111110	1 1000000001	1 1111111110
<-1.998V	0 0000000000	0 0111111111	1 1000000000	1 1111111111

Note: Voltages given are the mid-point for the codes.

1 = VOH, 0 = VOL.

code should have been. This logical decision can either choose the correct code or it can be off by one LSB. For this reason errors will not be any greater than 1 LSB.

REFERENCE LADDER

The ladder of the HADC77600 is composed of 1023 metal resistors of approximately .63 Ohms each and a resistor of half that value at each end of the ladder. Each resistor is actually a different value, with each value calculated to offset the typical 25°C bias current value of the preamplifiers. This results in a typical integral linearity curve that has very little, if any bow due to the effects of the summation of bias currents. The reference top and bottom are both connected to sense pins to reduce the offset of the ladder. In addition to the top and bottom reference points to the ladder there are also external taps to the ladder at 1/8 scale increments. These taps can be used to maintain the ladder's linearity if operation over a wide temperature range is required.

A better use for the ladder taps is in applications, where the linearity of the ladder is to be changed to piece-wise approximate a non-linear transfer function. This is often done to increase the dynamic range of the converter. Each ladder tap has been designed to handle the full reference current so that a wide variety of curves can be accommodated.

The top reference to the ladder is typically driven to +1.5 Volts, and the bottom of the ladder to -1.5 Volts. These points can be driven by any op amp that can supply 6mA. Care must be taken to assure that the amplifier offsets and drifts are commensurate with the system design. Ladder taps can be driven in a similar manner if desired. If they are not used they can be left open or by-passed to VRT or VRB.

INPUT PREAMPLIFIERS

The input to each comparator is buffered by a preamplifier to prevent currents caused by the dynamic switching of the comparator latches from feeding back to the input. These preamplifiers also isolate the ladder from these same currents.

CLK AND $\overline{\text{CLK}}$ INPUTS

The clock inputs are designed to be driven with differential ECL levels. Single-ended operation can be accomplished by bypassing the $\overline{\text{CLK}}$ input, which is internally biased to -1.3V, and driving CLK input.

OVER-RANGE

The over-range output can be used to either alarm the system when an over-range occurs or it can be used in applications where the dynamic range of the system is to be increased by stacking two converters. Over-range is true when the top reference (VRT) is exceeded by 1 LSB.

OPERATING TEMPERATURE RANGE

The HADC77600 is designed to operate over the full military temperature range. A custom package with the cavity down has been designed for the HADC77600. There is an internal heat sink built into the package. This package has a θ_{JA} of approximately 30°C/W. This can be reduced to 15°C/W by airflow at a rate of 500 LFPM across the package. Further reduction can be obtained by adding a heat sink.

TYPICAL APPLICATIONS CIRCUIT

The circuit in Figure 3 shows the HADC77600 in a high performance application. This circuit is intended to give the best possible results when used with the HADC77600. However, the external circuitry is not necessary in all applications. The track-and-hold (HTS-0010) and buffer-amps (CLC231s) are utilized to increase input bandwidth beyond 25MHz. This is not necessary if the device is being used below 25MHz. The buffer before the T/H is used to gain up the input signal by a factor of X1 or X2 depending on whether the input resistors are tied together or only one is connected to the input signal. This approach makes it easier to interface with 1V or 2V systems. The buffer is also used to sum in a small offset voltage to center the signal within the T/H input span of 2V. A second CLC231 buffer-amp is used after the T/H to drive the input to the HADC77600 as an option to the internal amplifier on board the ADC. This buffer is set in an inverting gain of 2 to boost the signal up to $\pm 2V$ swing to take advantage of the full dynamic range of the HADC77600. Notice the liberal use of power supply decoupling on the external devices. Shown are RF beads that increase in resistance at high frequencies, small chip capacitors for high frequency bypassing as close to the device pins as possible, and medium to low frequency capacitors for general decoupling. All of these components are not entirely necessary depending on how much digital and high frequency noise is coupled into the power supply lines by other devices on the board and at what frequency range the system is operating. Good separate digital and analog ground planes and separate supply lines will decrease the number of components needed for noise free operation.

The Maxim ICL7664ACPA is a very precise negative voltage regulator used to develop the $\pm 2V$ reference voltage for the ADC reference ladder. The ladder biases up the threshold voltage inputs for the 1024 comparators on the ADC. The external op-amps are used to correct any "bow" in the thresholds or comparators by changing the voltage at 1/4, 1/2, and 3/4 full scale to give better integral linearity. Additional op-amps or voltage sources can be tied to all five ladder taps for even more control. But again, this is optional and all that is really needed is the top (+2V) and bottom (-2V) voltage reference.

Power supply requirements are $\pm 5V$ and +2V. The +2V is generated by the LM317T adjustable voltage regulator. The reason a separate regulator is used than the one for the reference is that a lot of noise is generated on the +2V power line. The noise should not be injected into the reference circuitry.

The power supply pins to the HADC77600 do not require high frequency decoupling due to internal capacitive bypassing of 120pF. The +2V supply does require the additional component.

The ECL digital outputs are capable of driving 75 Ω loads to 10KH specifications. A convenient Thevenin equivalent 75 or 130 Ω load connected to the digital -5.2V supply can be used (see Figure 3 notes) or a 75 Ω to -2V will work as well. If the output digital signal lines are greater than an inch long, microstripline techniques should be used.

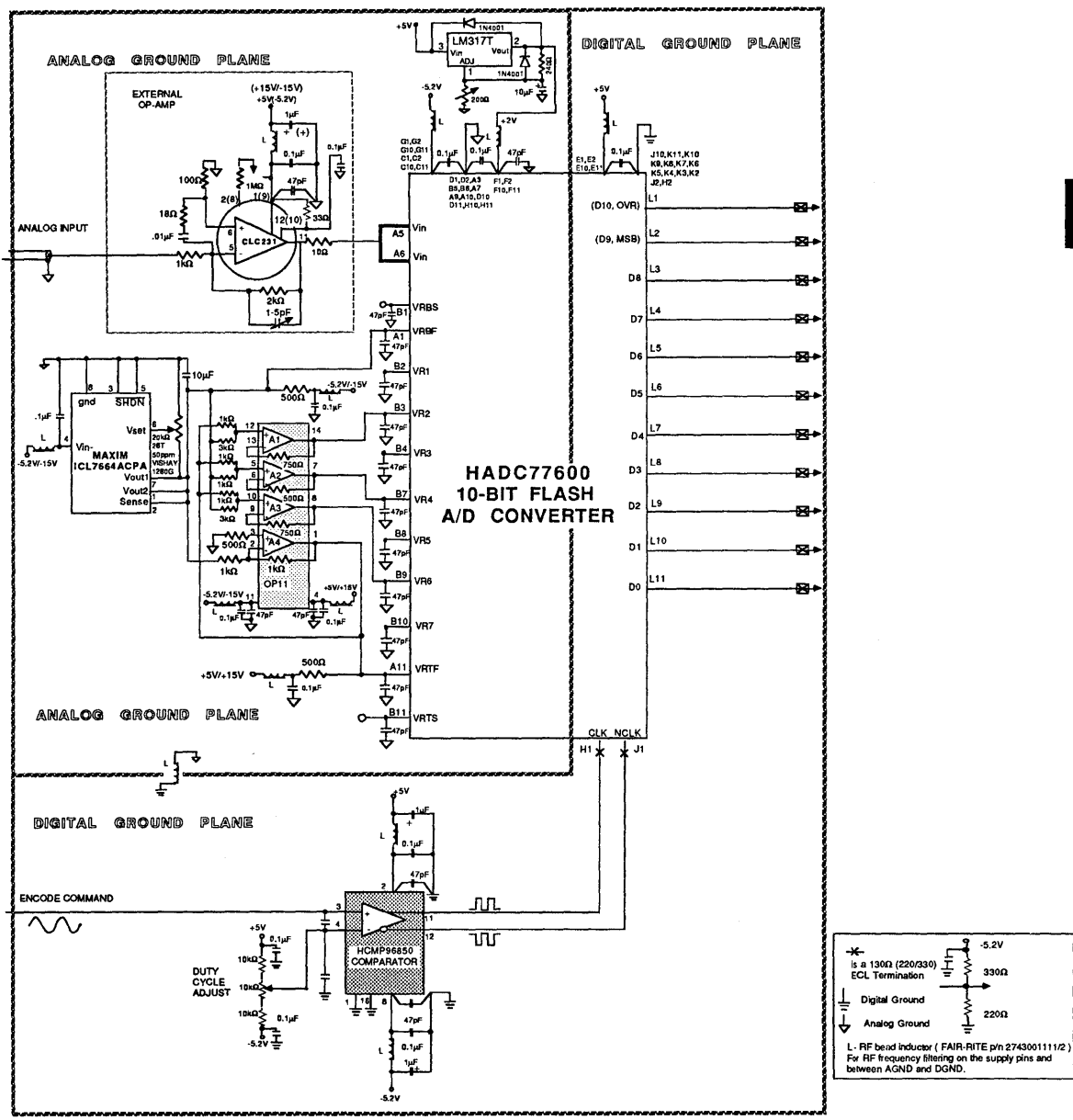


FIGURE 3 - HADC77600 TYPICAL APPLICATIONS CIRCUIT

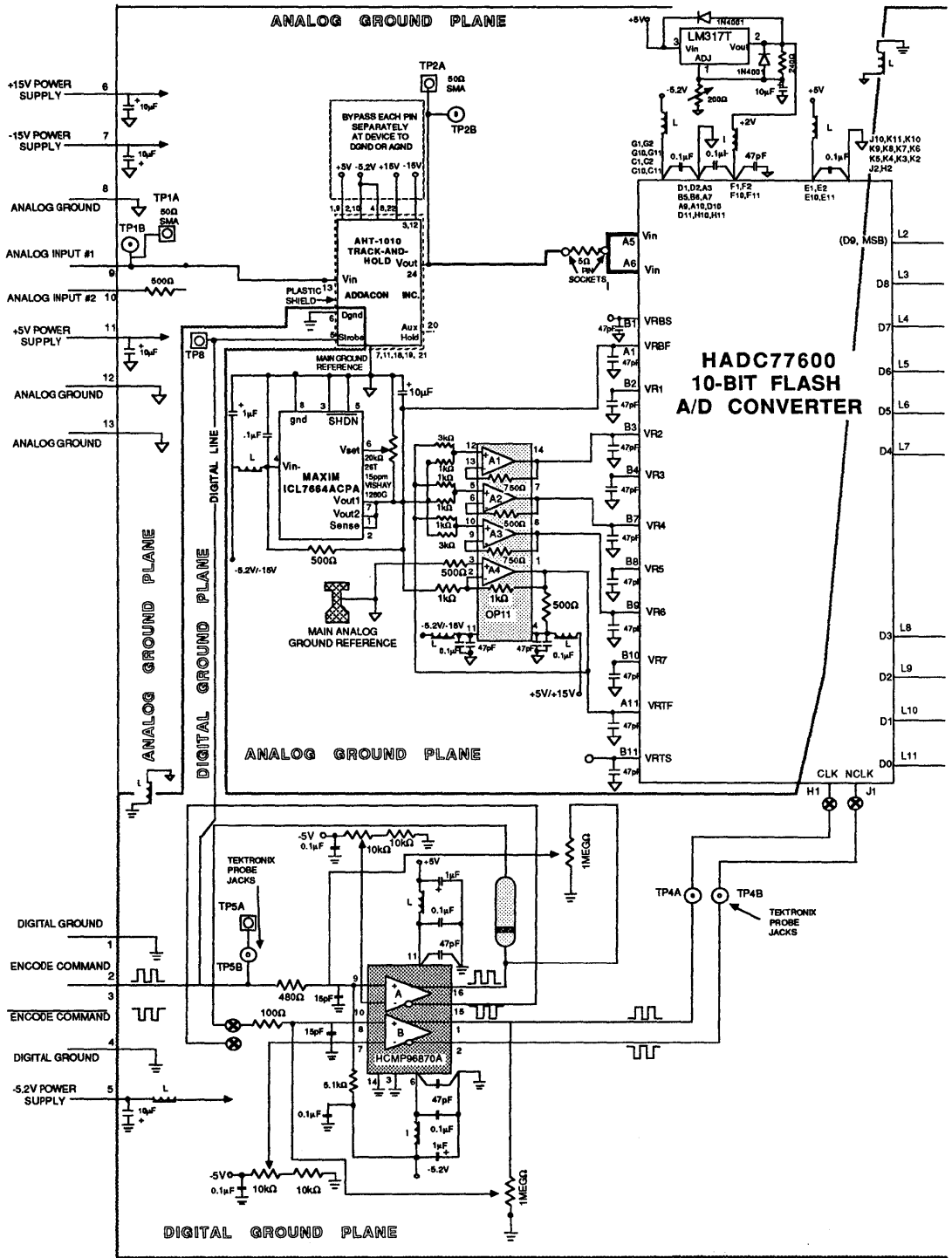


FIGURE 4 - HADC77600 WITH TRACK-AND-HOLD AMPLIFIER

DIGITAL GROUND PLANE

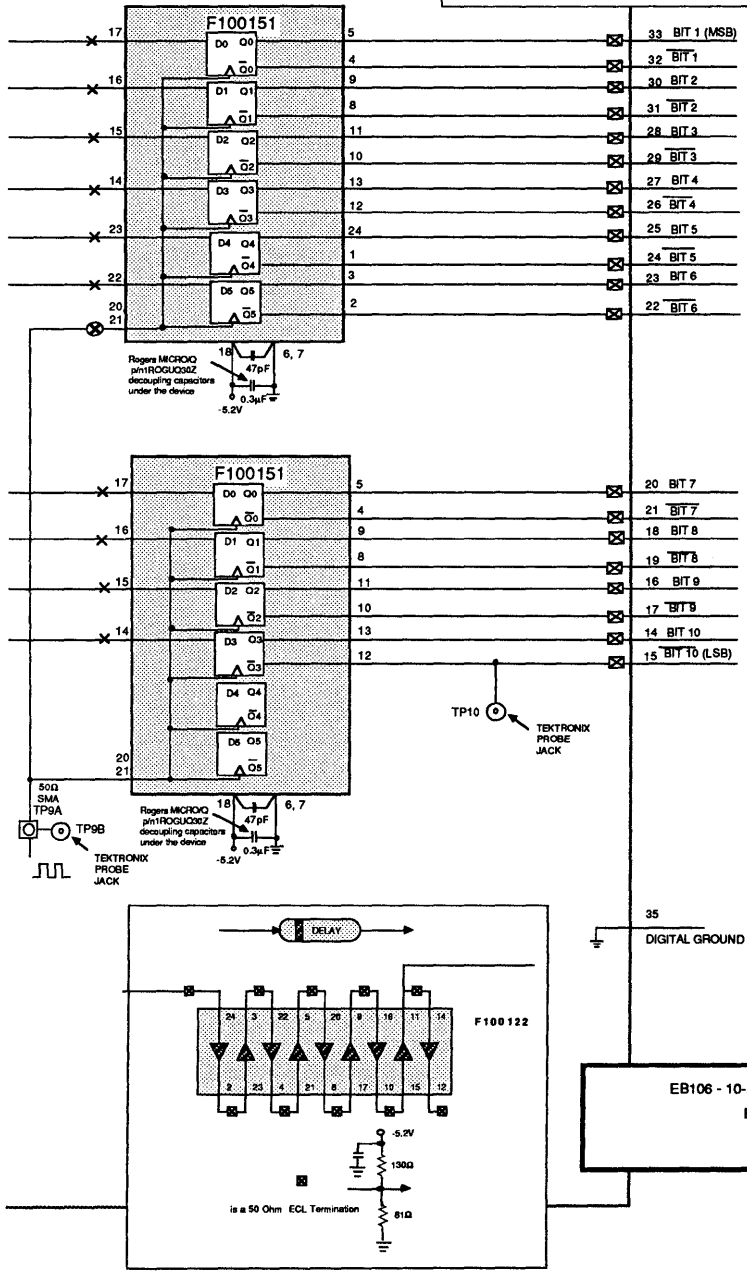
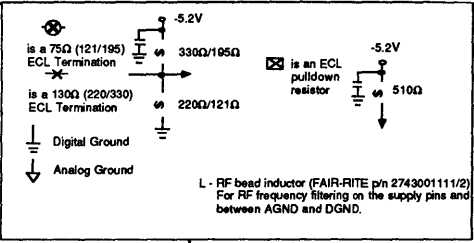


FIGURE 4 - HADC77600 WITH TRACK-AND-HOLD AMPLIFIER CONTINUED

EB106 - 10-BIT FLASH A/D CONVERTER
 EVALUATION BOARD
 07/26/88 Vii Bahadur

FIGURE 4. BURN-IN SCHEMATIC

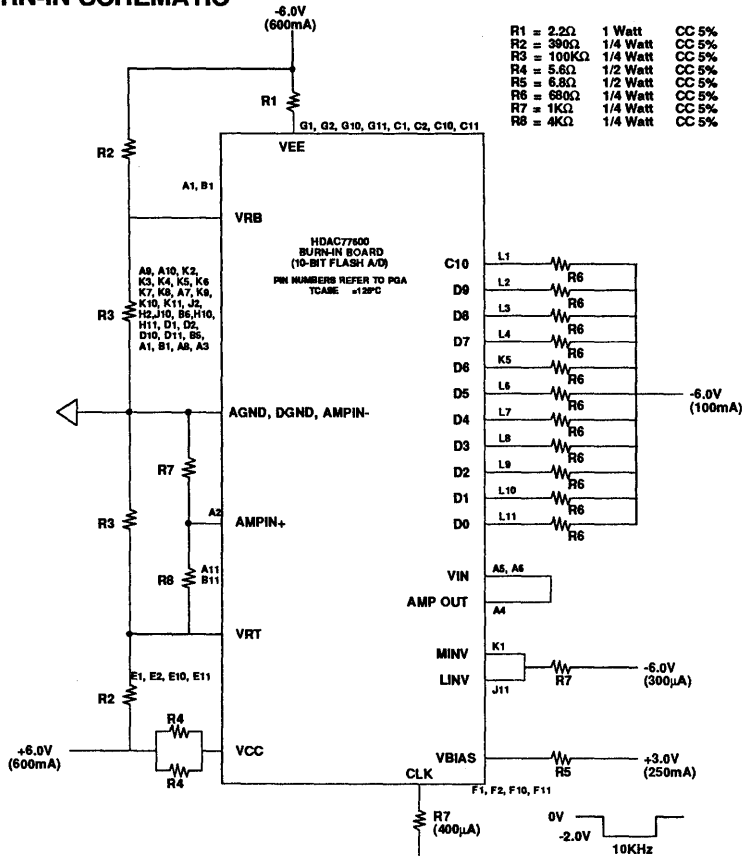
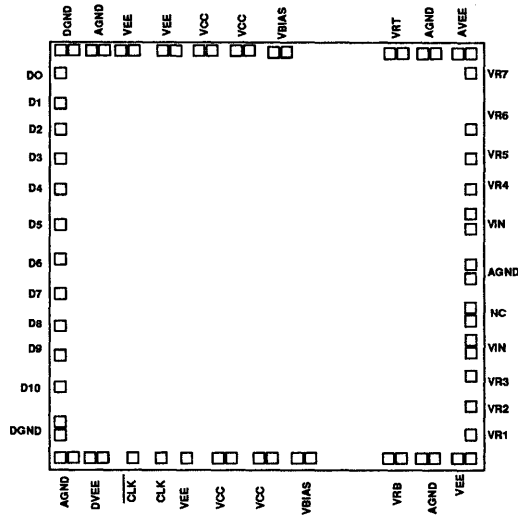


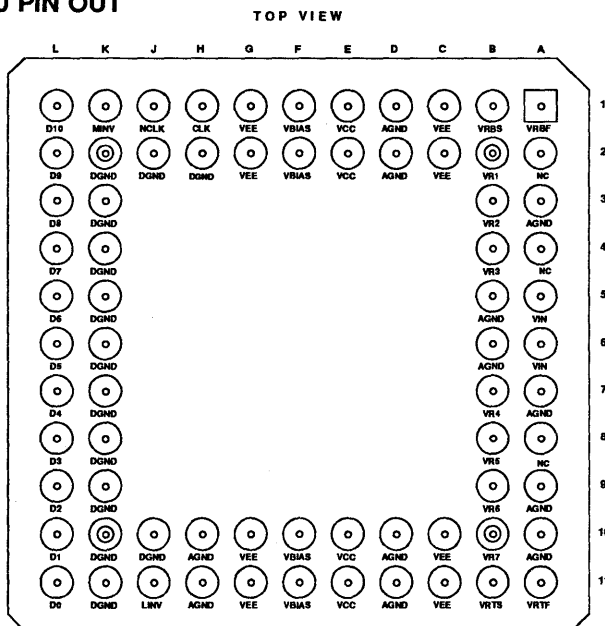
FIGURE 5. 77600 DIE PLOT



HADC77600 PIN DESCRIPTION

Pins	Description
VEE	Analog and digital negative supply. Typically -5.2 Volts.
VBIAS	Supply voltage. Typically +2.0 Volts.
VCC	Positive digital supply. Typically +5.0 Volts.
AGND	Analog ground.
DGND	Digital ground. Return for ECL outputs. Return to termination ground.
VRT	Most positive reference. Typically +1.50 Volts.
VRTS	Sense pin for the positive reference.
VRB	Most negative reference. Typically -1.50 Volts.
VRBS	Sense pin for the negative reference.
VR1 thru VR7	Reference ladder taps in 1/8 scale increments for ladder adjustments.
LINV	Data complement control for bits 0 through 8.
MINV	Data complement control for bits 9 and 10 (OVR).
VIN	Flash converter input.
D0 thru D9	Digital ECL outputs. Capable of driving 75 Ohm loads to 10KH specifications.
D10 or OVR	Over-range bit. True when the input exceeds the voltage at VRT.

HADC77600 PIN OUT



$q_{JC} < 1^{\circ}\text{C/W}$
 $q_{JA} = 25^{\circ}\text{C/W}$
 $q_{JA} \text{ w/500 LFPM air} = 14^{\circ}\text{C/W}$

Custom package contains 120pF power supply bypass capacitance on the VCC and VEE pins.

Note: Metal top of package is connected to negative VEE.

**For Ordering Information See Section 1.

NOTES:

16-BIT μ P COMPATIBLE HIGH SPEED A/D CONVERTER

ADVANCE INFORMATION

FEATURES:

- 4 μ sec Conversion Rate
- Low Power - 700 mW
- Internal Voltage Reference
- Internal or External Clock
- Parallel, Serial or 2-byte Output Options
- ± 2.5 Volt Analog Input

APPLICATIONS:

- Data Acquisition
- Instrumentation
- Digital Signal Processing
- Communication Systems
- Sonar

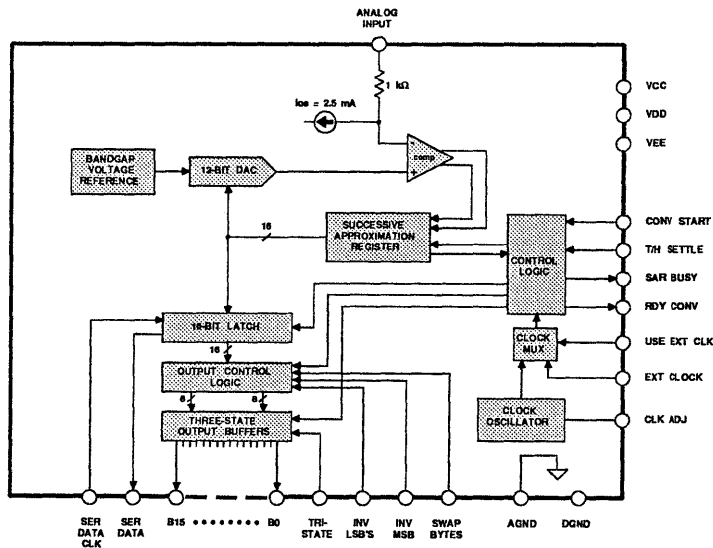
GENERAL DESCRIPTION

The HADC78160 is a complete 16-bit A/D converter which offers high speed and low power dissipation. This hybrid device utilizes a successive approximation type architecture and contains an internal clock oscillator and bandgap voltage reference. It has microprocessor-compatible control functions and can output code from the tri-statable output buffer in selectable format onto an 8 or 16 bit bus, or it can output data in a serial mode.

All input and output logic is TTL compatible. Full scale analog input range is ± 2.5 volts. The internal clock oscillator is adjustable via an external control voltage; alternatively, an external clock can be used. A large variety of available logic control pins makes the HADC78160 directly suitable for many applications, without the need for external logic circuitry.

The HADC78160 is packaged in a 40 lead, 600 mil Ceramic DIP and operates on ± 15 and $+5$ volt power supplies.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond Which Damage May Occur) 25°C (1)**Supply Voltages**

VCC to AGND	+18 V
VEE to AGND	-18 V
VDD to DGND.....	+6 V
AGND to DGND Differential	+0.5 V

Temperature

Temperature, case	-60 to +140°C
junction	+150°C
Lead Temperature (soldering 10 seconds) ..	+300°C
Storage Temperature	-65 to +150°C

Input Voltages

All Digital Inputs to DGND.....	-0.3 V to (VDD + 0.3 V)
Analog Input to AGND.....	-6 to +6 V

NOTE 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

RECOMMENDED OPERATING CONDITIONS**Supply Voltages**

VCC.....	+14.25 to +15.75 V
VEE.....	-14.25 to -15.75 V
VDD.....	+4.75 to +5.25 V

Temperature

Temperature, Ambient (1)	-25 to +85°C
--------------------------------	--------------

ELECTRICAL SPECIFICATIONS

T_A=25°C, VCC = 15V, VDD = 5V, unless otherwise specified.

Parameter	Test Conditions	Test Level (1)	Min	Typ	Max	Units
-----------	-----------------	----------------	-----	-----	-----	-------

ACCURACY SPECIFICATIONS

Integral Linearity Error		I		±0.0030		%FSR
Integral Linearity Drift		I		±2		PPM/°C
Differential Linearity Error		I		±0.0030		%FSR
Differential Linearity Drift		I		±2		PPM/°C
Gain Error		I		±0.05	±0.2	%FSR
Gain Error Drift		I		±15	±25	PPM/°C
Zero Offset Error		I		±0.05	±0.2	%FSR
Zero Offset Error Drift		I		±2	±4	PPM/°C
Minimum Resolution With Guarantee Of No Missing Codes		IV	14	15		Bits

ANALOG INPUT SPECIFICATIONS

Analog Input Range	Bipolar	I		±2.5		Volts
Analog Input Impedance		IV	5			kΩ

DYNAMIC SPECIFICATIONS

Conversion Time		I	3.5	4	4.5	μsec
-----------------	--	---	-----	---	-----	------

POWER SUPPLIES

VCC Supply Current	+15V±5%	I		5.4		mA
VEE Supply Current	-15V±5%	I		30.1		mA
VDD Supply Current	+5V±5%	I		32.0		mA
Power Dissipation		IV		693		mW

Parameter	Test Conditions	Test Level (1)	Min	Typ	Max	Units
LOGIC SPECIFICATIONS						
V _{IH}		I	2.0		5.5	V
V _{IL}		I	0		0.8	V
I _{IH}		I		10		μA
I _{IL}		I		10		μA
V _{OH}		I	3.8	4.5		V
V _{OL}		I		0.8		V
I _{OH}		I		100		μA
I _{OL}		I		3.2		mA

NOTES:

(1) ELECTRICAL CHARACTERISTICS TESTING

TEST LEVEL

TEST PROCEDURE

All electrical characteristics are subject to the following conditions:

I

100% production tested at the specified temperature.

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicate that the specification is not tested at the specified condition.

II

100% production tested at T_a=25°C, and sample tested at the specified temperature.

Unless otherwise noted, all tests performed after a 10 min. power soak.

III

QA sample tested only at the specified temperatures.

IV

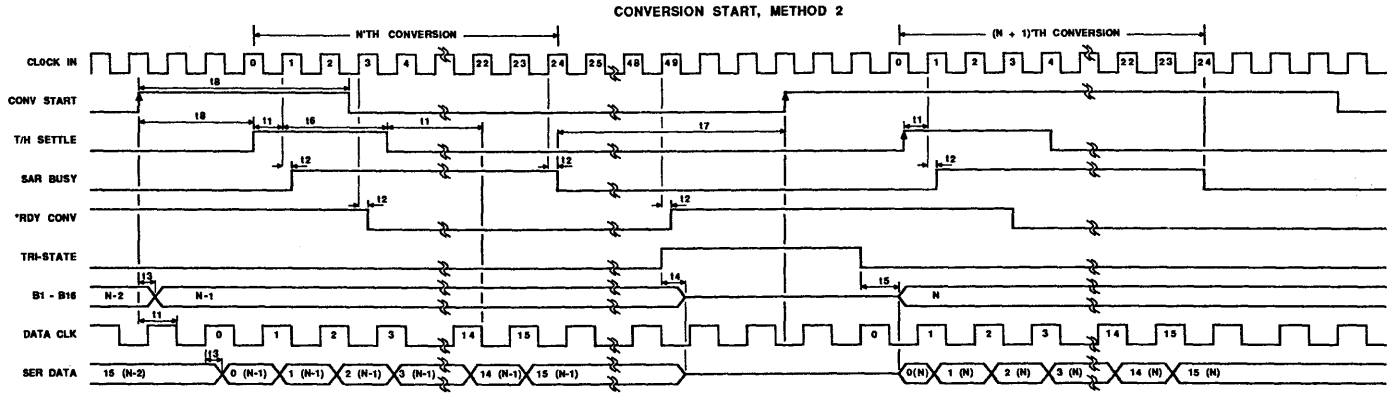
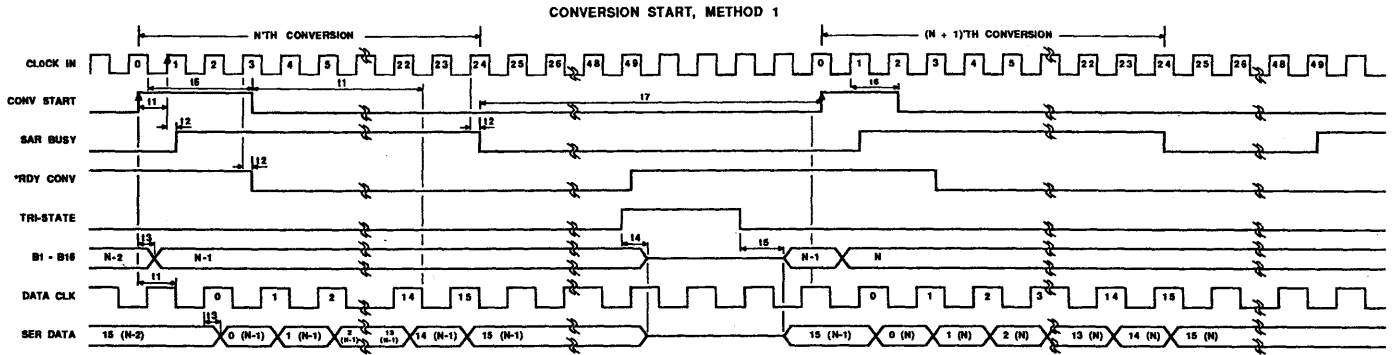
Parameter is guaranteed (but not tested) by design and characterization data.

V

Parameter is a typical value for information purposes only.

V _{IN}	DIGITAL OUTPUT			
	INV MSB = 0 INV LSB'S = 0 SWAP BYTES = 0	INV MSB = 1 INV LSB'S = 0 SWAP BYTES = 0	INV MSB = 1 INV LSB'S = 1 SWAP BYTES = 0	INV MSB = 0 INV LSB'S = 0 SWAP BYTES = 1
(VOLTS)	(MSB - LSB)	(MSB - LSB)	(MSB - LSB)	(B7 - B0 B15 - B8)
-2.499924	1 - 1	01 - 1	0 - 0	11111111 11111111
0.0	10 - 0	0 - 0	01 - 1	00000000 10000000
+2.500000	0 - 0	10 - 0	1 - 1	00000000 00000000

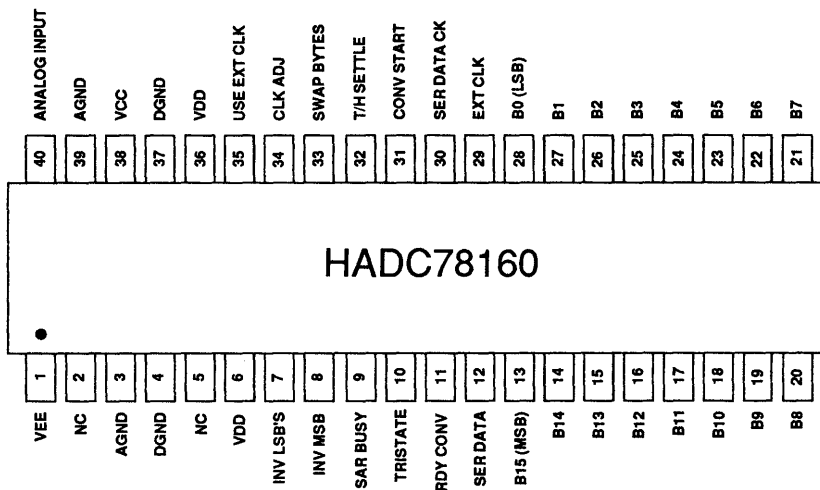
HADC78160 OUTPUT LOGIC



- t1 = 30 nsec Min; Setup Time (T/H SETTLE, CONV START, INV LSB'S, INV MSB, SWAP BYTES)
- t2 = 50 nsec Max; Output Delay Time (SAR BUSY, RDY CONV)
- t3 = 50 nsec Max; Output Delay Time (B0 - B15, SER DATA)
- t4 = 30 nsec Max; Tri-State Low to Data Valid Delay (B0 - B15, SER DATA)
- t5 = 100 nsec Max; Tri-State High to Data Valid Delay (B0 - B15, SER DATA)
- t6 = 150 nsec Min; Hold Time or Minimum Pulse Width (CONV START)
- t7 = 0 nsec Min; Optimum Restart Time (Restart earlier than clock cycle #49 will cause RDY CONV signal to be a random signal)
- t8 = 1 CLOCK IN Cycle Min; Minimum Pulse Width (CONV START) for Conversion Start, Method 2
- t9 = 1 CLOCK IN Cycle Min; CONV START to T/H SETTLE Set Up Time

* Note: RDY CONV is An Optional Output (See Note of t7)

HADC78160 TIMING



HAD78160 Pin Assignment

Pin Functions

PIN	PIN NAME	PIN FUNCTION
1	VEE	-15 volt power supply connection
2	NC	No connection
3	AGND	Analog ground connection
4	DGND	Digital ground connection
5	NC	No connection
6	VDD	+5 volt power supply connection
7	INV LSB'S	Logic input to invert outputs B0-B14, active high --(int. pulldown)
8	INV MSB	Logic input to invert output B15, active high -- (int. pullup)
9	SAR BUSY	Logic output indicating device is busy, active high
10	TRISTATE	Logic input to put B0-B15 into tristate, active high -- (int. pulldown)
11	RDY CONV	Logic output indicating device is ready, active high
12	SER DATA	Serial data output
13	B15 (MSB)	Parallel output data bit 15, most-significant-bit
14	B14	Parallel output data bit 14
15	B13	Parallel output data bit 13
16	B12	Parallel output data bit 12
17	B11	Parallel output data bit 11
18	B10	Parallel output data bit 10
19	B9	Parallel output data bit 9
20	B8	Parallel output data bit 8
21	B7	Parallel output data bit 7
22	B6	Parallel output data bit 6
23	B5	Parallel output data bit 5
24	B4	Parallel output data bit 4
25	B3	Parallel output data bit 3
26	B2	Parallel output data bit 2
27	B1	Parallel output data bit 1
28	B0 (LSB)	Parallel output data bit 0, least-significant-bit
29	EXT CLK	Input for external device timing clock
30	SER DATA CLK	Input for serial data output clock
31	CONV START	Logic input for conversion initiation, active high
32	T/H SETTLE	Logic input pin commanding SAR to wait, active low
33	SWAP BYTES	Logic input to swap B0-B7 and B8-B15, active high -- (int. pulldown)
34	CLK ADJ	Optional voltage input used to adjust internal clock
35	USE EXT CLK	Logic input to command use of EXT CLK, active high -- (int. pulldown)
36	VDD	+5 volt power supply connection
37	DGND	Digital ground connection
38	VCC	+15 volt power supply connection
39	AGND	Analog ground connection
40	ANALOG INPUT	Analog signal input

**For Ordering Information See Section 1.

NOTES:

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

CMOS, 12 BIT MONOLITHIC MULTIPLYING DAC

FEATURES

- Improved Version of the AD7541A
- Low Output Capacitance (< 75 pf.)
- Maximum Gain Error < 2 LSB (all grades)
- 12 Bit Linearity Over Temperature
- Settling Time = 500 nsecs.
- +5V to +15V operation

APPLICATIONS

- Gain Control Circuits
- Programmable Gain Amplifiers
- Programmable Filters
- Function Generators
- Digital/Synchro Converters
- Digitally Controlled Attenuation

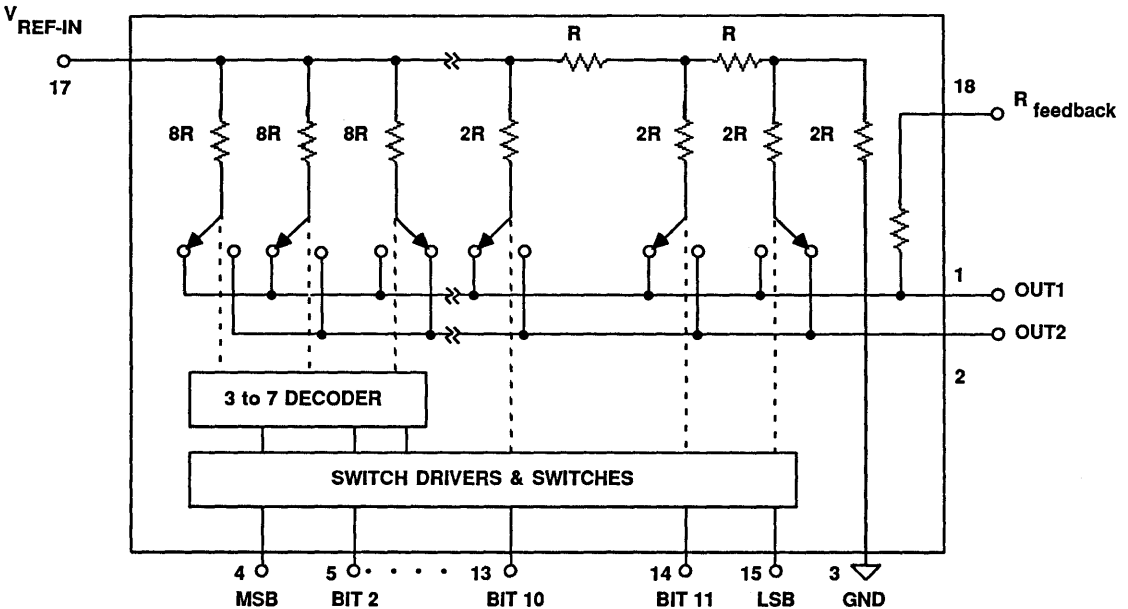
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GENERAL DESCRIPTION

The HDAC7541Z is a monolithic, low cost 12 bit digital to analog converter (DAC). It is compatible with the industry standard 7541A but with significant performance improvements in speed and gain accuracy. The HDAC7541Z is fabricated in a 3 micron, polysilicon gate

CMOS process. The excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is insured by the use of an epi process base. This eliminates the need for external Schottky clamping diodes.

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS (CONTINUED)

TEST CONDITIONS: Unless Otherwise Noted, VDD = 15V, VREF = +10V, OUT1 = 0V, AGND = DGND,
 TA = 0 to 70° C for Commercial Grade Units,
 TA = -25 to 85° C for Industrial Grade Units,
 TA = -55 to 125° C for Military Grade Units
 (Refer to Ordering Information for Grade Descriptions)

HDAC7541Z

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7541ZA			HDAC7541ZB			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	

DC ELECTRICAL CHARACTERISTICS

Output Leakage									
Pin 2	25°C	I	-5		+5	-5		+5	nA
	0-70°C/-25 to +85°C	I	-10		+10	-10		+10	
	-55 to +125°C	I	-200		+200	-200		+200	
	All digital inputs at VDD								
Reference Input Resistance	Pin 17 to GND +25°C Temp. Coefficient	I II	7	12.5	18	7	12.5	18	KΩ ppm/°C
Digital Inputs	Tmin - Tmax								
V _{IH} (High Input Voltage)		I	2.0			2.0			Volts
V _{IL} (Low Input Voltage)		I			0.8			0.8	Volts
I _{IN} (Input Current)		I			1			1	μA
C _{IN} (Input Capacitance)	V _{IN} = 0 Volts	II			8			8	pF
Power Supply									
V _{DD} Range		I	+5	+15	+16	+5	+15	+16	Volts
I _{DD}	25°C	I			1			1	mA
	Tmin-Tmax / Digital Inputs at V _{IL} or GND	I			1			1	mA
	25°C	I			3			3	mA
	Tmin-Tmax / Digital Inputs at V _{DD} or V _{IH}	I			4			4	mA
PSRR	ΔV _{DD} = ±5%	I	-	±.001	±.005	-	±.001	±.005	(Δgain%)/(ΔV _{DD} %)

AC ELECTRICAL CHARACTERISTICS

Propagation Delay	From Digital Input to 90% of Output Final Value; Note 3	II	-	50	100	-	50	100	nsecs
Digital to Analog Glitch Impulse	V _{REF} = 0V; Note 2	II	-	200	400	-	200	400	nV-sec

3

ELECTRICAL SPECIFICATIONS (CONTINUED)

TEST CONDITIONS: Unless Otherwise Noted, VDD = 15V, VREF = +10V, OUT1 = 0V, AGND = DGND,
 TA = 0 to 70° C for Commercial Grade Units,
 TA = -25 to 85° C for Industrial Grade Units,
 TA = -55 to 125° C for Military Grade Units
 (Refer to Ordering Information for Grade Descriptions)

PARAMETER	TEST CONDITIONS	TEST LEVEL	HDAC7541ZA			HDAC7541ZB			UNITS
			MIN	NOM	MAX	MIN	NOM	MAX	

AC ELECTRICAL CHARACTERISTICS

Multiplying Feedthrough Error	VREF to VOUT VREF = ±10 Volts 10KHz Sinewave	II	-	0.3	0.5	-	0.3	0.5	mV(p-p)
Output Current Settling Time	To 0.01% of full scale; Notes 2 & 3	II	-	0.5	1.0	-	0.5	1.0	µsec
Output Capacitance	Tmin-Tmax								
COUT1	Pin1; Digital Inputs = VIH	II		48	75		48	75	pF
COUT2	Pin2; Digital Inputs = VIH	II		15	25		15	25	pF
COUT1	Pin1; Digital Inputs = VIL	II		19	30		19	30	pF
COUT2	Pin2; Digital Inputs = VIL	II		38	65		38	65	pF

Note 2: Digital inputs change from 0V to VDD or VDD to 0V.

Note 3: OUT1 load: 100Ω + 13pf.

Voltage outputs derived using HOS-50 amplifier.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics that follow are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore Tj = Tc = Ta.

TEST LEVEL

I
II

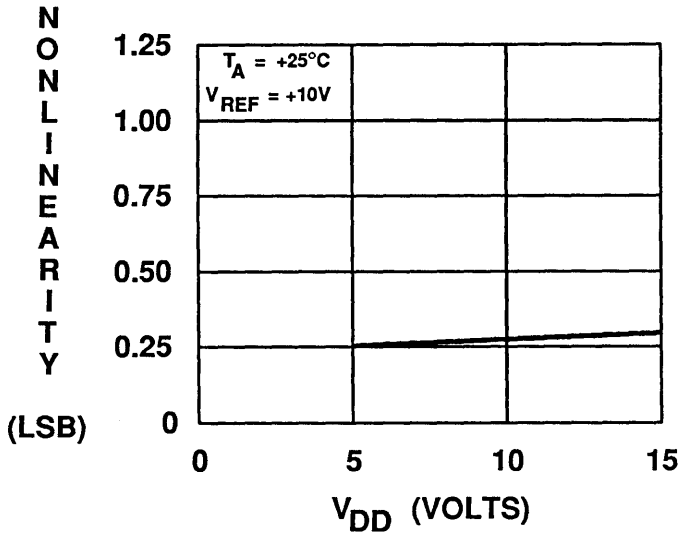
TEST PROCEDURE

Production tested.

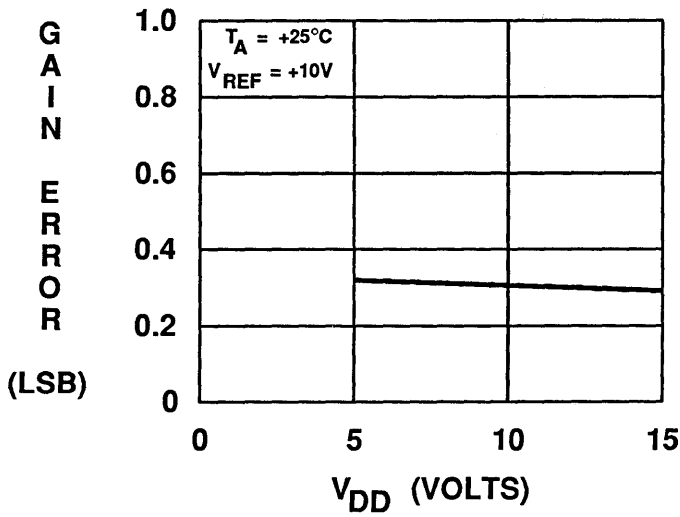
Parameter is guaranteed by design and characterization data.

TYPICAL PERFORMANCE OVER V_{DD}

NONLINEARITY vs.
SUPPLY VOLTAGE



GAIN ERROR vs.
SUPPLY VOLTAGE



TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7541Z ideal full-scale output is $-(4095)/(4096) \cdot (V_{REF})$. Gain error is adjustable to zero using external trims as shown in Figures 4 and 5.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's or at OUT2 with the DAC loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the V_{REF} terminal to OUT1 with the DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

This is a measure of the internal delay of the circuit and is

measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV-secs and is measured with $V_{REF} = GND$.

CIRCUIT DESCRIPTION

The HDAC7541Z operation is best understood from the simplified circuit description in Figure 1. The input V_{REF} is applied to an R-2R ladder network. The R-2R network divides the V_{REF} input by 2 at each stage to produce currents in the 2R legs which decrease by a factor of 2 moving toward the LSB end of the ladder.

The switches on each 2R leg allow this current to be routed to analog ground or through the feedback resistor of the external op-amp on OUT1. This op-amp resistor converts the current to a voltage again. The sum of the selected leg currents forced through $R_{feedback}$ determines the output voltage by the equation in Figure 1.

The op-amp on OUT1 creates a virtual ground point on OUT1 such that the voltage on the 2R legs is ground no matter which positions the current steering switches are in. This makes the input resistance seen by V_{REF} a constant R Ohms.

The HDAC7541Z uses a modification of this R-2R ladder which has the largest 3 bits' current provided by equally weighted resistors rather than binary scaled resistors. This "segmentation" technique improves the linearity and gain accuracy of the HDAC7541Z and lowers the glitch energy during code transitions. This internal structure, however, does not change the way the output code is selected by the user. Therefore, the simplified schematic in Figure 1 is suitable for understanding the operation of the HDAC7541Z.

EQUIVALENT CIRCUIT ANALYSIS

The equivalent output circuit of the HDAC7541Z is the key to understanding offset, linearity and settling time. Figures 2 and 3 illustrate these effects.

In Figure 2, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to OUT2. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin 17 plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 3 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to Figure 2.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in Figures 2 and 3.

The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between Figures 2 and 3, resistance at each op-amp input can change from 10K Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below:

$$\text{Offset gain} = 1 + R_{\text{feedback}}/RDAC$$

With all code bits LOW:

$$RDAC \gg R_{\text{feedback}}; \text{offset gain} = 1$$

With all code bits HIGH:

$$RDAC = 10K \text{ Ohms}; \text{offset gain} = 2$$

Thus, the offset is not amplified by a constant gain over the range of code input. This variation in offset gain is seen as a non-linearity in the voltage output over the full scale output. The magnitude of non-linearity is the difference in the gains at code extremes times the offset

voltage. In this DAC, this non-linearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (Figures 2 and 3). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (Figures 4 and 5). Although all R-2R DAC's have the need for this type of compensation, the HDAC7541Z maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7541Z.

The choice of compensation capacitor is bounded by three limits:

- C1 along with R_{feedback} determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and R_{feedback} should be smaller than secondary poles in the op-amp - as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{\text{OUT1}} + C1}$.

For an OP-27 used as an output op-amp with 8 MHz gain-bandwidth, the choice of C1 would be:

$$(2 \cdot \pi \cdot C1 \cdot R_{\text{feedback}})^{-1} = 4 \text{ MHz or } C1 = 4 \text{ pf.}$$

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7541Z's low output capacitance comes much closer to fulfilling this goal than most other 7541 compatible DAC's. Thus, faster, more well controlled settling is seen with the HDAC7541Z.

ANALOG/DIGITAL DIVISION

The transfer function for the HDAC7541Z connected in the multiplying mode as shown in Figure 1 is:

$$V_O = -V_{IN} \cdot \left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \dots + \frac{A_{12}}{2^{12}} \right)$$

where A_x assume a value of 1 for a "HIGH" bit and 0 for a "LOW" bit.

FIGURE 1
SIMPLIFIED, TYPICAL INTERFACE CIRCUIT

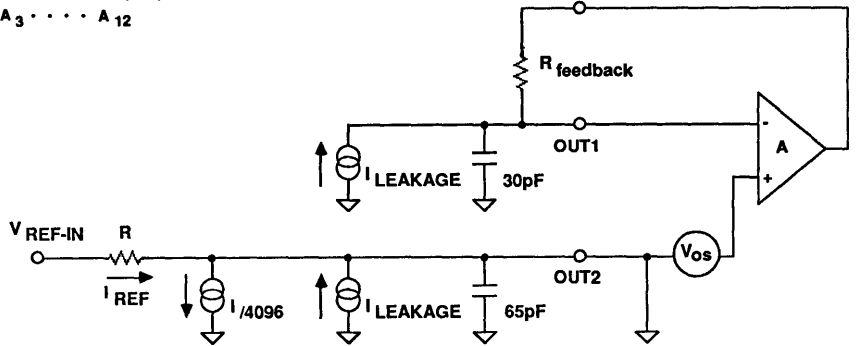
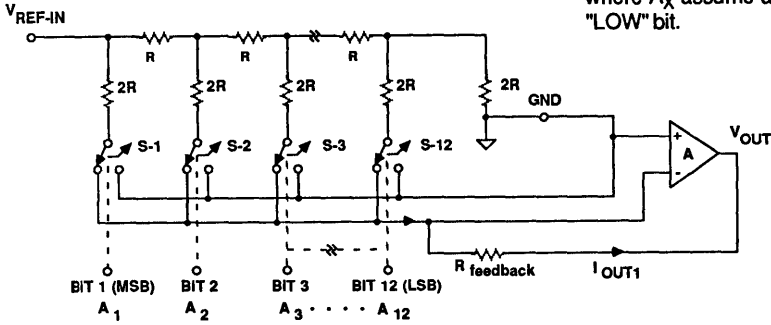


FIGURE 2
HDAC7541Z DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS LOW

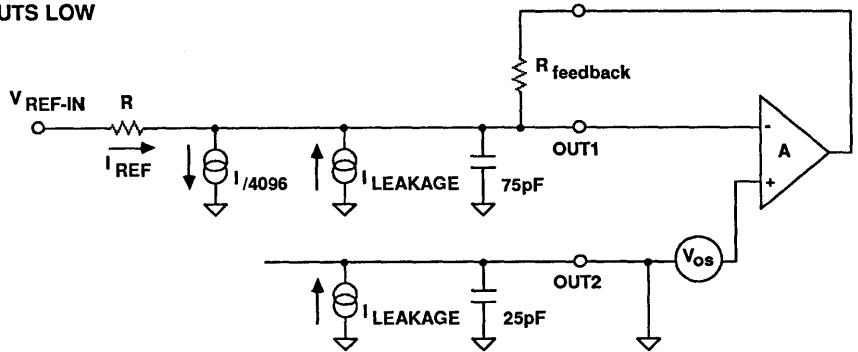


FIGURE 3
HDAC7541Z DAC EQUIVALENT CIRCUIT
ALL DIGITAL INPUTS HIGH

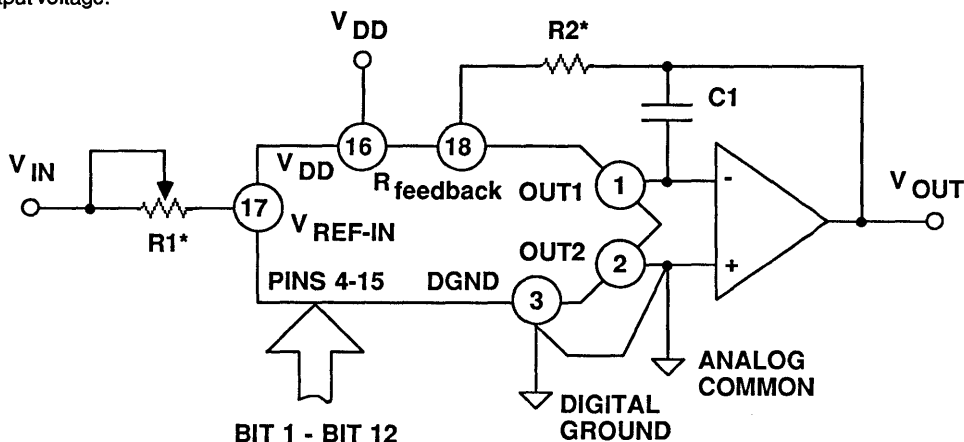
UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

Figure 4 illustrates the use of the HDAC7541Z in a unipolar (or 2 quadrant multiplication) mode. The V_{REF} is applied from pin 17 to ground voltage or an input current can be applied to pin 17. Positive or negative voltages/current can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the V_{REF} voltage out. If the source of V_{REF} is adjustable, V_{REF} could be directly adjusted for full scale calibration.

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

The op-amp used with the HDAC5741Z should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the fact that the offset effect is code dependant and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.



*REFER TO TABLE 1.

FIGURE 4 UNIPOLAR BINARY OPERATION

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7541Z in a bipolar (or 4 quadrant multiplication) mode is illustrated in Figure 5. The V_{REF} is applied from pin 17 to ground voltage or an input current can be applied to pin 17. Positive or negative voltages/current can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of V_{REF} to produce a maximum output which is half of V_{REF} in either polarity (see Table 3 for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the V_{REF} source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track one another for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate the OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

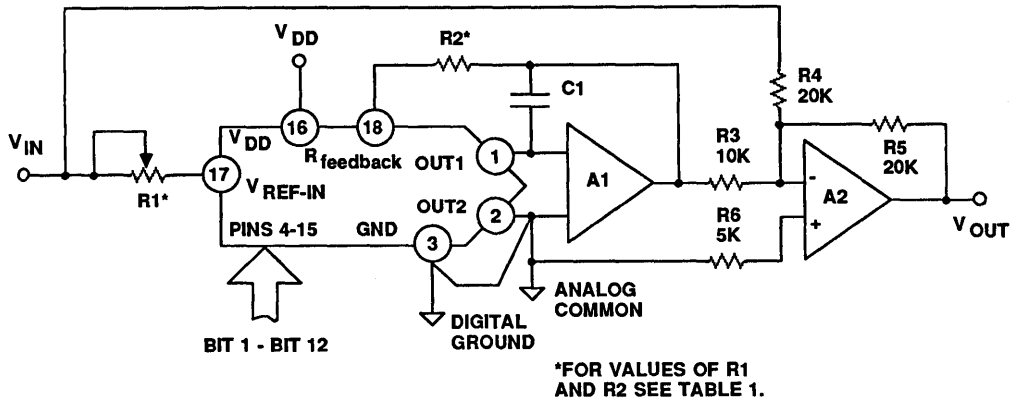


FIGURE 5: BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

TRIM RESISTOR		
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

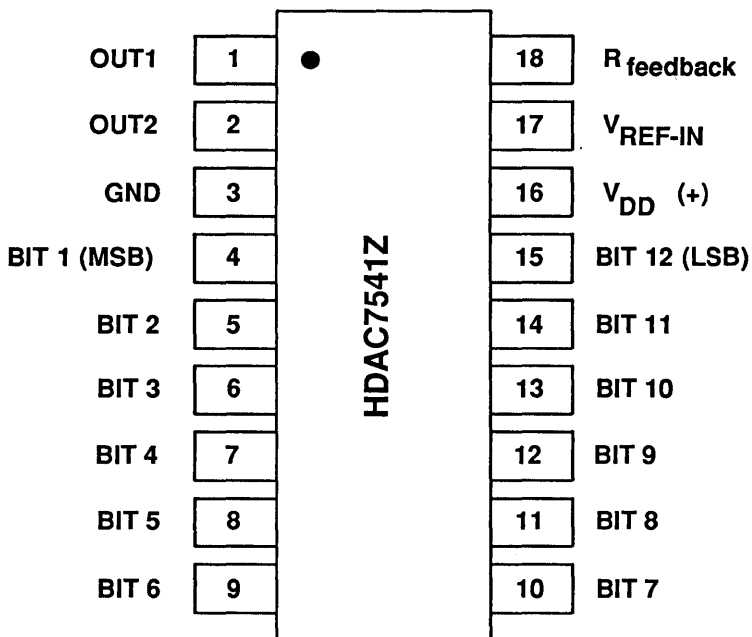
TABLE I: RECOMMENDED TRIM RESISTOR VALUES VS. GRADES

BINARY NUMBER IN DAC			ANALOG OUTPUT, V _{OUT}
MSB		LSB	
1111	1111	1111	$-V_{IN} \left(\frac{4095}{4096} \right)$
1000	0000	0000	$-V_{IN} \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$
0000	0000	0001	$-V_{IN} \left(\frac{1}{4096} \right)$
0000	0000	0000	0 Volts

TABLE II: UNIPOLAR BINARY CODE TABLE FOR CIRCUIT OF FIGURE 4

BINARY NUMBER IN DAC			ANALOG OUTPUT, V _{OUT}
MSB		LSB	
1111	1111	1111	$+V_{IN} \left(\frac{2047}{2048} \right)$
1000	0000	0001	$+V_{IN} \left(\frac{1}{2048} \right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN} \left(\frac{1}{2048} \right)$
0000	0000	0000	$-V_{IN} \left(\frac{2048}{2048} \right)$

TABLE III: BIPOLAR CODE TABLE FOR CIRCUIT OF FIGURE 5



PIN ASSIGNMENT HDAC7541Z

PIN	NAME	FUNCTION
1	OUT1	CURRENT OUTPUT 1
2	OUT2	CURRENT OUTPUT 2
3	GND	GROUND
4	BIT 1	DIGITAL INPUT (BIT 1) (MOST SIGNIFICANT BIT)
5	BIT 2	DIGITAL INPUT (BIT 2)
6	BIT 3	DIGITAL INPUT (BIT 3)
7	BIT 4	DIGITAL INPUT (BIT 4)
8	BIT 5	DIGITAL INPUT (BIT 5)
9	BIT 6	DIGITAL INPUT (BIT 6)
10	BIT 7	DIGITAL INPUT (BIT 7)
11	BIT 8	DIGITAL INPUT (BIT 8)
12	BIT 9	DIGITAL INPUT (BIT 9)
13	BIT 10	DIGITAL INPUT (BIT 10)
14	BIT 11	DIGITAL INPUT (BIT 11)
15	BIT 12	DIGITAL INPUT (BIT 12) (LEAST SIGNIFICANT BIT)
16	V _{DD}	POSITIVE POWER SUPPLY
17	V _{REF-IN}	REFERENCE INPUT VOLTAGE
18	R _{feedback}	INTERNAL FEEDBACK RESISTOR

PIN FUNCTIONS HDAC7541Z

**For Ordering Information See Section 1.

NOTES:

CMOS 12-BIT μ P BUFFERED DAC

FEATURES:

- Improved Direct Replacement for AD7542
- Maximum Gain Error < 1/2 LSB ('A/G' Grade)
- 12-Bit Linearity Over Temperature
- 0.5 μ secs. Settling Time
- Microprocessor Compatible I/O
- 4 Quadrant Multiplication
- Low Gain Drift (<3ppm/ $^{\circ}$ C)

APPLICATIONS:

- μ P Gain Control Circuits
- μ P Attenuator Control
- μ P Controlled Function Generators
- Bus Structured Instrumentation
- Process Controllers
- Industrial Controllers

GENERAL DESCRIPTION

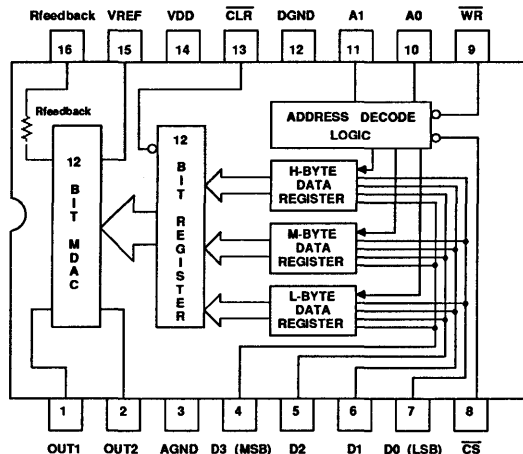
The HDAC7542A is a monolithic, low cost, multiplying 12-bit digital to analog converter (DAC) designed for direct microprocessor interface. It is compatible with the industry standard 7542 but with significant performance improvements in speed and gain accuracy.

The HDAC7542A is fabricated in a 3 micron, polysilicon gate CMOS process. Accuracy is assured by the use of Laser-trimmed thin film resistors. Use of an epi process base provides latch-up immunity. Linearity and gain accuracy are well controlled over temperature.

The data bits for selecting the DAC output are written into the HDAC7542A via a direct connection to the parallel bus of a microprocessor. Data bytes are written as 3, 4 bit groups or "nibbles" into the data registers on the chip. The input bits are double buffered on-chip. Updating the analog output is controlled via the parallel bus by writing to the chip. A clear pin ($\overline{\text{CLR}}$) allows for resetting the output to all zeros under power up or system reset conditions. All address decoding for writing to the chip registers is handled on the chip.

The HDAC7542A's direct parallel bus interconnect makes it an excellent choice for microprocessor-based instruments and industrial or process controllers utilizing microprocessors.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25°C

Supply Voltages

V_{DD} to DGND or AGND..... +7V
 AGND to DGND..... -0.3 V to VDD

Input Voltages

Digital Inputs to DGND..... -0.3 V to VDD
 VRfeedback or VREF to DGND..... ±25V

Outputs

V_{OUT1} or V_{OUT2} to GND..... -0.3 V to VDD

Temperature

Operating Temperature, ambient..... -55 to +125°C
 junction..... +150°C
 Lead Temperature, (soldering 10 seconds)..... +300°C
 Storage Temperature..... -65 to +150°C
 Power Dissipation (Any Package) to +75°C..... 450mW
 (derates above 75°C by 6 mW/°C)

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. CAUTION - ESD SENSITIVE DEVICE: The logic and analog ports of this device have special circuits to protect it against ESD damage. Although this protection should prevent permanent damage to the inputs, care should be taken in handling.

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
 T_A = 0 to 70°C for Commercial Grade Units,
 T_A = -25 to 85°C for Industrial Grade Units,
 T_A = -55 to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G		HDAC7542AA		HDAC7542AB		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	

ACCURACY

Resolution		I	-	12	-	-	12	-	-	12	-	bits
Relative Accuracy		I	-1/2	±1/4	+1/2	-1/2	+1/2	-1	+1			LSB
Differential Nonlinearity		I	-1/2	±1/4	+1/2	-1/2	+1/2	-1	+1			LSB
Gain Error, Using R _{feedback}	25°C	I	-1/2	+1/2	-2	+2	-3	+3				LSB
Gain Error, Using R _{feedback}		I	-1.5	+1.5	-3	+3	-4	+4				LSB
Gain Temperature Coefficient		II	0.3	3	0.3	3	0.3	3				ppm/°C

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
 $T_A = 0$ to 70°C for Commercial Grade Units,
 $T_A = -25$ to 85°C for Industrial Grade Units,
 $T_A = -55$ to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

DC ELECTRICAL PARAMETERS (CONTINUED)	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G			HDAC7542AA			HDAC7542AB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

OUTPUT LEAKAGE

Pins OUT1 and OUT2	25°C	I	-1	+1	-1	+1	-1	+1	nA
Pins OUT1 and OUT2	Military Grades	I	-50	+50	-50	+50	-50	+50	nA
	Other Grades	I	-10	+10	-10	+10	-10	+10	nA

INPUT RESISTANCE

Input VREF	Pin 19 to GND 25°C	I	7	12.5	18	7	12.5	18	7	12.5	18	K Ω
Input VREF Temp. Coefficient		II	-180			-180			-180			ppm/°C

LOGIC INPUTS (D0-D3, A0-A1, $\overline{\text{CS}}$, $\overline{\text{WR}}$, $\overline{\text{CLR}}$)

V_{IH} (High input voltage)		I	2.0			2.0			2.0			Volts
V_{IL} (Low input voltage)		I	0.8			0.8			0.8			Volts
I_{IN} (Input current)		I	1			1			1			μA
C_{IN} (Input capacitance)	$V_{IN} = 0\text{V}$	II	5			5			5			pF

POWER SUPPLY

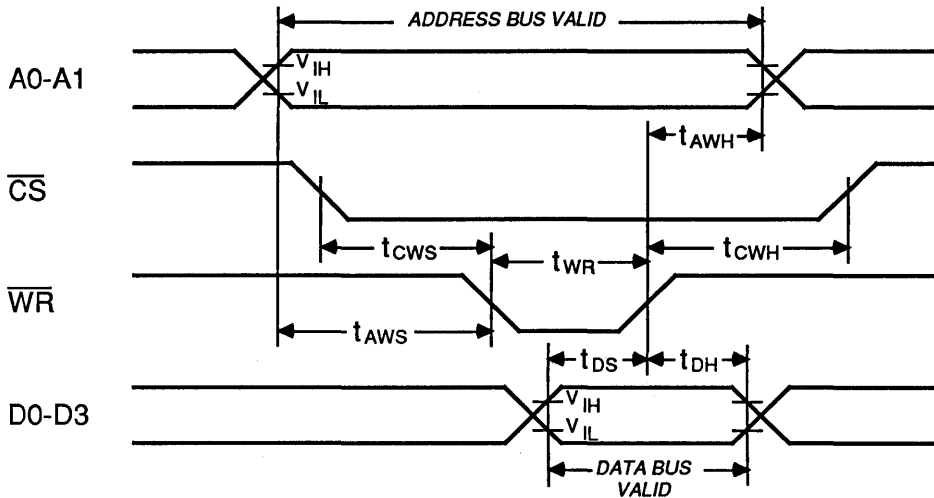
I_{DD}	All Logic Inputs at V_{IL} or V_{IH}	I	2.5			2.5			2.5			mA
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Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
 $T_A = 0$ to 70°C for Commercial Grade Units,
 $T_A = -25$ to 85°C for Industrial Grade Units,
 $T_A = -55$ to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G		HDAC7542AA		HDAC7542AB		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
Multiplying Feedthrough Error	Note 3	II	.3	.5	.3	.5	.3	.5	mVPP
C _{OUT1,2} (Output Capacitance)	DAC REG. = ALL 0'S	II		30		30		30	pF
C _{OUT1,2} (Output Capacitance)	DAC REG. = ALL 1'S	II		75		75		75	pF
Output Current Settling Time	Note 4	II	0.5	1	0.5	1	0.5	1	μsec.

NOTES: 3. VREF = ±10 V @ 10 KHz Sinewave.
 4. Measured to 0.5 LSB from falling edge of WR. Load on Pin OUT1 = 100 Ω + 13 pF

WRITE CYCLE TIMING DIAGRAM



TIMING MEASUREMENT REFERENCE LEVEL IS (V_{IH} + V_{IL})/2 UNLESS OTHERWISE INDICATED

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
 $T_A = 0$ to 70°C for Commercial Grade Units,
 $T_A = -25$ to 85°C for Industrial Grade Units,
 $T_A = -55$ to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

AC ELECTRICAL PARAMETERS (CONTINUED)	TEST CONDITIONS	TEST LEVEL	HDAC7542AA/G			HDAC7542AA			HDAC7542AB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

SWITCHING CHARACTERISTICS

t_{WR} (WRITE Pulse Width)		I	40	40	40	nsec
t_{AWH} (Address-to-WRITE hold time)		I	0	0	0	nsec
t_{CWH} (Chip select-to-Write hold time)		I	0	0	0	nsec
t_{CLR} (CLEAR pulse Width)		I	40	40	40	nsec

Input Byte Register Loading

t_{CWS} (Chip select-to-WRITE Setup Time)		I	0	0	0	nsec
t_{AWS} (Address Valid-to-WRITE Setup Time)		I	40	40	40	nsec
t_{DS} (Data Setup Time)		I	20	20	20	nsec
t_{DH} (Data Hold Time)		I	20	20	20	nsec

Internal DAC Register Loading

t_{CWS} (Chip Select-to-WRITE Setup Time)		I	0	0	0	nsec
t_{AWS} (Address Valid-to-WRITE Setup Time)		I	40	40	40	nsec

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:
 Parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL

I
II

TEST PROCEDURE

Production tested.
 Guaranteed by design and sampled characterization data.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7542A ideal full-scale output is $-(4095)/(4096) \cdot (V_{REF})$. Gain error is adjustable to zero using external trims as shown in Figures 5 and 6 and Table II.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's or at OUT2 with the DAC loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the VREF terminal to OUT1 with the DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GENERAL CIRCUIT DESCRIPTION

As shown in the Block Diagram of the cover sheet, the HDAC7542A consists of a 12-bit multiplying DAC and data input logic. The data input logic consists of three 4-bit input data registers (H, M and L-Byte) and a 12-bit DAC register. The DAC register is loaded from the three input registers. Content of the DAC Register controls the DAC's analog output level. Data entry is further described in the Interface Logic section.

Figure 1 shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7542A

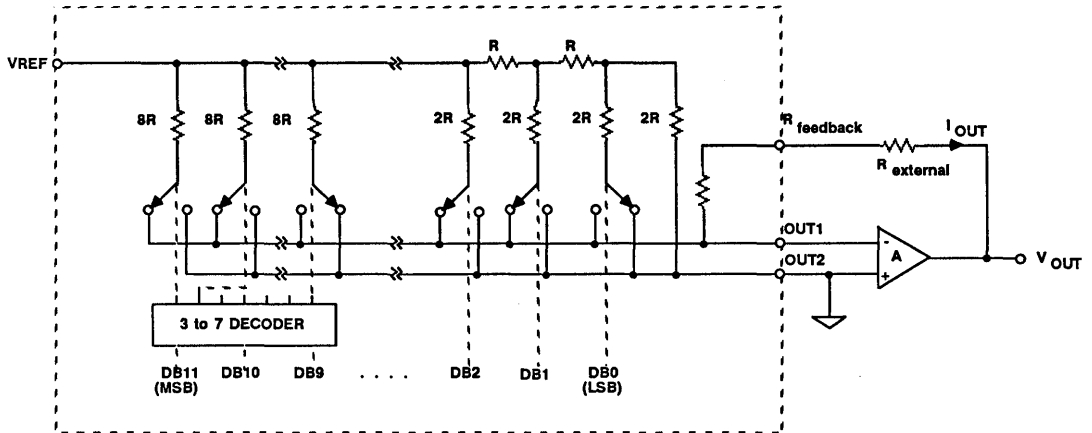


FIGURE 1 SIMPLIFIED HDAC7542A DAC CIRCUITRY (WITH EXTERNAL OP AMP)

uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7542A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the (remaining) VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switch routes the bit-weighted current of the leg to either pin OUT1 (output) or pin OUT2 (analog ground). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the 3 most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7542A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the optional external resistor of Figure 1 in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered VOUT, and in combination with the feedback resistance, maintains OUT1 at virtual ground. The transfer function of Figure 2 shows the relationship of VOUT for an equivalent R-2R resistor network, shown in the same figure. A more detailed understanding of the circuit operation and performance aspects are found in the following Equivalent Circuit Analysis section.

EQUIVALENT CIRCUIT ANALYSIS

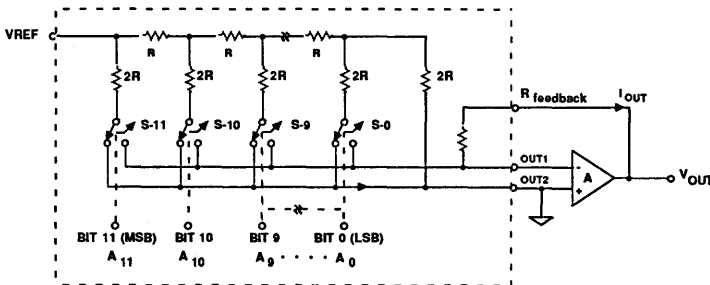
The equivalent output circuit of the HDAC7542A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In Figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to pin OUT2 which is externally connected to analog ground. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin VREF plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to Figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in Figures 3 and 4.

The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between Figures 3 and 4, resistance at each op-amp input can change from 10K Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below: (next page)



The transfer function for the equivalent network shown is:

$$V_{OUT} = -V_{REF} \cdot \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \dots + \frac{A_0}{2^{12}} \right)$$

where A_x assumes a value of 1 for a "HIGH" bit and 0 for a "LOW" bit.

FIGURE 2 EQUIVALENT R-2R RESISTOR NETWORK FOR THE HDAC7542A DAC CIRCUITRY (WITH EXTERNAL OP AMP)

FIGURE 3
HDAC7542A DAC EQUIVALENT CIRCUIT
 ALL DIGITAL INPUTS LOW
 (WITH EXTERNAL OP AMP)

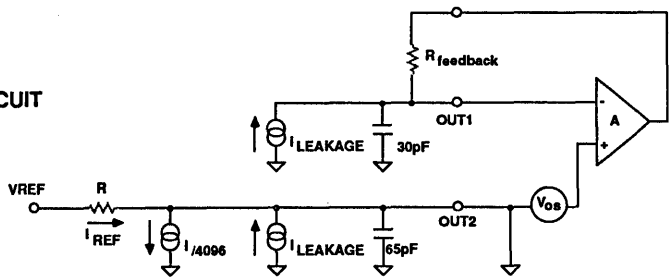
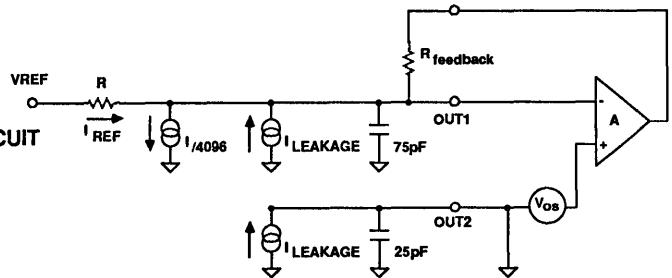


FIGURE 4
HDAC7542A DAC EQUIVALENT CIRCUIT
 ALL DIGITAL INPUTS HIGH
 (WITH EXTERNAL OP AMP)



Offset gain = $1 + R_{\text{feedback}}/RDAC$

With all code bits LOW:
 $RDAC \gg R_{\text{feedback}}$; offset gain = 1

With all code bits HIGH:
 $RDAC = R_{\text{feedback}}$; offset gain = 2

Thus, the offset is not amplified by a constant gain over the range of code inputs. This variation in offset gain is seen as a non-linearity in the voltage output over the full scale output. The magnitude of non-linearity is the difference in the gains at code extremes times the offset voltage. In this DAC, the non-linearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (Figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (Figures 5 and 6). Although all R-2R DAC's have the need for this type of compensation,

the HDAC7542A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7542A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with R_{feedback} determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and R_{feedback} should be smaller than secondary poles in the op-amp - as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{\text{OUT1}} + C1}$.

For an OP-17 used as an output op-amp with a 30 MHz gain-bandwidth, the choice of C1 would be:

$$(2 \cdot \pi \cdot C1 \cdot R_{\text{feedback}})^{-1} = 15 \text{ MHz,}$$

$$\text{or } C1 \approx 15 \text{ pf} \quad (R_{\text{feedback}} \approx 12.5 \text{ K}\Omega)$$

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7542A's low output capacitance comes much closer to fulfilling this goal than most other 7542 compatible DAC's. Thus, faster, more well controlled settling is obtained with the HDAC7542A.

HDAC7542A CONTROL INPUTS					HDAC7542A OPERATION
A1	A0	\overline{CS}	\overline{WR}	\overline{CLR}	
X	X	X	X	0	RESETS DAC REGISTER TO 0000 0000 0000 (1)
X	X	1	X	1	NO OPERATION, DEVICE NOT SELECTED
0	0	0	\uparrow	1	LOAD L-BYTE DATA REGISTER WITH DATA AT D0-D3
0	1	0	\uparrow	1	LOAD M-BYTE DATA REGISTER WITH DATA AT D0-D3
1	0	0	\uparrow	1	LOAD H-BYTE DATA REGISTER WITH DATA AT D0-D3
1	1	0	\square	1	LOAD DAC REGISTER WITH L, M, H-BYTE REG. DATA

NOTE (1):
 $\overline{CLR} = 0$ ASYNCHRONOUSLY RESETS DAC REGISTER TO 0000 0000 0000 BUT HAS NO EFFECT ON INPUT REGISTERS

0 = LOGIC LOW
 1 = LOGIC HIGH
 X = DON'T CARE
 \uparrow = POSITIVE EDGE TRIGGERED
 \square = LEVEL TRIGGERED

TABLE I INPUT LOGIC TRUTH TABLE

INTERFACE LOGIC

Data is loaded into the HDAC7542A in three 4-bit bytes through data pins D0, D1, D2 and D3. Address pins A0 and A1 select the loading of internal byte register H (high byte), M (middle Byte) or L (low byte). Address pin A0 and A1 also allow the selection of the internal 12-bit DAC register, which is loaded by the H, M and L register simultaneously. Data in the internal DAC register determines the DAC analog output value. Table I, above, provides the complete input logic truth table.

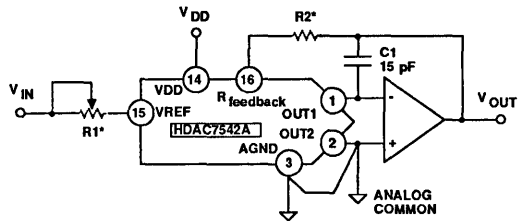
Write timing, as shown in the Write Cycle Timing Diagram of Page 4, is similar to data loading of a RAM device. Note that pin \overline{WR} is used to both load the input byte registers and the internal DAC register. The \overline{CLR} pin, when momentarily brought to logic 0, resets the internal DAC register to 0000 0000 0000. This feature is useful for system initialization since the DAC output is set to a known condition.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

Figure 5 illustrates the use of the HDAC7542A in a unipolar (or 2 quadrant multiplication) mode. Data input pins have been omitted for clarity. The VREF is applied as a voltage from pin 15 to ground or an input current can be applied to pin 15. Positive or negative voltages/currents can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the VREF voltage out. If the source of VREF is adjustable, VREF could be directly adjusted for full scale calibration (refer to table III).

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This compensates for the feedback pole caused by OUT1's capacitance.



*REFER TO TABLE II.

FIGURE 5 UNIPOLAR BINARY OPERATION

The op-amp used with the HDAC7542A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the fact that the offset effect is code dependant and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

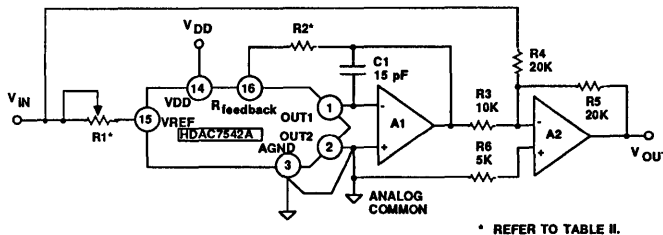
BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7542A in a bipolar (or 4 quadrant multiplication) mode is illustrated in Figure 6. The VREF is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/currents can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of VREF to produce a maximum output which is half of VREF in either polarity (see Table IV for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the VREF source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track one another for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate for OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.



* REFER TO TABLE II.

FIGURE 6 BIPOLAR OPERATION

	TRIM RESISTOR	
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

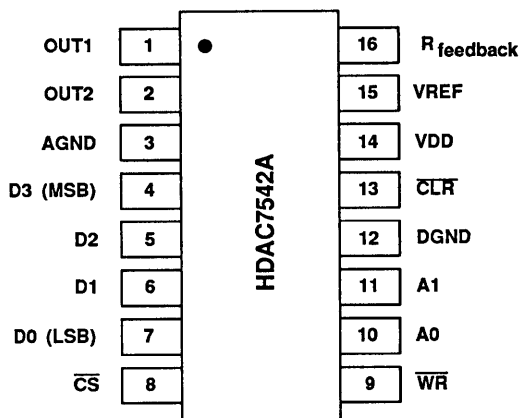
TABLE II
RECOMMENDED TRIM RESISTANCE

BINARY NUMBER IN DAC			ANALOG OUTPUT, V _{OUT}
MSB		LSB	
1111	1111	1111	$-V_{IN} \left(\frac{4095}{4096} \right)$
1000	0000	0000	$-V_{IN} \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$
0000	0000	0001	$-V_{IN} \left(\frac{1}{4096} \right)$
0000	0000	0000	0 Volts

TABLE III
UNIPOLAR BINARY CODE
FOR CIRCUIT OF FIGURE 6

BINARY NUMBER IN DAC			ANALOG OUTPUT, V _{OUT}
MSB		LSB	
1111	1111	1111	$+V_{IN} \left(\frac{2047}{2048} \right)$
1000	0000	0001	$+V_{IN} \left(\frac{1}{2048} \right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN} \left(\frac{1}{2048} \right)$
0000	0000	0000	$-V_{IN} \left(\frac{2048}{2048} \right)$

TABLE IV
BIPOLAR CODE
FOR CIRCUIT OF FIGURE 7



**HDAC7542A PIN ASSIGNMENT
(TOP VIEW)**

PIN	PIN NAME	FUNCTION
1	OUT1	ANALOG CURRENT OUTPUT 1
2	OUT2	ANALOG CURRENT OUTPUT 2
3	AGND	ANALOG GROUND
4	D3	DATA BUS INPUT 3 (MSB)
5	D2	DATA BUS INPUT 2
6	D1	DATA BUS INPUT 1
7	D0	DATA BUS INPUT 0 (LSB)
8	CS	CHIP SELECT INPUT
9	WR	DATA WRITE INPUT
10	A0	ADDRESS BUS INPUT 0
11	A1	ADDRESS BUS INPUT 1
12	DGND	DIGITAL GROUND
13	CLR	CLEAR INPUT FOR DAC REG.
14	VDD	POSITIVE POWER SUPPLY
15	VREF	REFERENCE VOLTAGE INPUT
16	Rfeedback	INTERNAL FEEDBACK RESISTOR

HDAC7542A PIN FUNCTIONS

**For Ordering Information See Section 1.

NOTES:

CMOS 12-BIT SERIAL INPUT BUFFERED MULTIPLYING DAC

FEATURES:

- Improved Direct Replacement for AD7543
- Maximum Gain Error < 1/2 LSB ('A/G' Grade)
- 0.5 μsecs. Settling Time
- 12-Bit Linearity Over Temperature
- Serial Data load With Flexible Strobe Conditions
- 4 Quadrant Multiplication
- Low Gain Drift (<3ppm/°C)

APPLICATIONS:

- Industrial and Process Controllers
- Proportional Controllers Requiring Serial Isolation or Remote Location

GENERAL DESCRIPTION

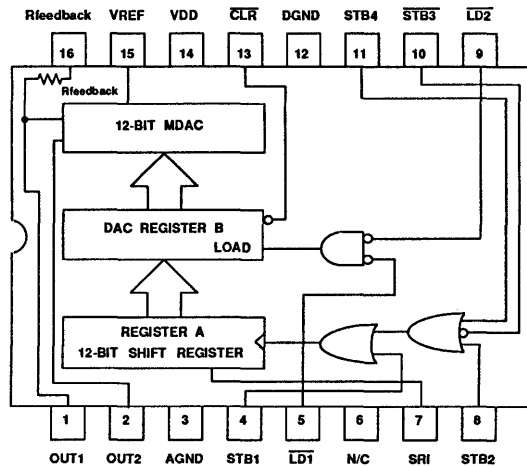
The HDAC7543A is a monolithic, low cost, multiplying 12-bit digital to analog converter (DAC) designed for serial digital input. It is compatible with the industry standard 7543 but with significant performance improvements in speed and gain accuracy.

The HDAC7543A is fabricated in a 3 micron, polysilicon gate CMOS process. Accuracy is assured by the use of Laser-trimmed thin film resistors. Use of an epi process base provides latch-up immunity. Linearity and gain accuracy are well controlled over temperature.

The data bits for selecting the DAC output are written into the HDAC7543A via a serial data port prior to latching them into the output register. The input bits are double buffered on-chip. The serial bus control pins provide a great deal of flexibility in providing the serial input strobe conditions for the data transfer. A clear pin (CLR) allows for resetting the output to all zero's under power up or system reset conditions.

The HDAC7543A's direct serial data interconnect makes it an excellent choice for industrial or process controllers which require electrical isolation or remote location. The serial bus minimizes the number of control lines which would require isolation devices or line drivers in these types of applications.

BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
 $T_A = 0$ to 70°C for Commercial Grade Units,
 $T_A = -25$ to 85°C for Industrial Grade Units,
 $T_A = -55$ to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

HDAC7543A

DC ELECTRICAL PARAMETERS (CONTINUED)	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G			HDAC7543AA			HDAC7543AB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

OUTPUT LEAKAGE

Pins OUT1 and OUT2	25°C	I	-1	+1	-1	+1	-1	+1	nA
Pins OUT1 and OUT2	Military Grades	I	-50	+50	-50	+50	-50	+50	nA
	Other Grades	I	-10	+10	-10	+10	-10	+10	nA

3

INPUT RESISTANCE

Input VREF	Pin 19 to GND 25°C	I	7	12.5	18	7	12.5	18	7	12.5	18	KΩ
Input VREF Temp. Coefficient		II	-180			-180			-180			ppm/°C

LOGIC INPUTS (STB1, STB2, STB3, STB4, LD1, LD2, CLR, SRI)

V_{IH} (High input voltage)		I	2.0			2.0			2.0			Volts
V_{IL} (Low input voltage)		I	0.8			0.8			0.8			Volts
I_{IN} (Input current)		I	1			1			1			μA
C_{IN} (Input capacitance)	$V_{IN} = 0V$	II	5			5			5			pF

POWER SUPPLY

I_{DD}	All Logic Inputs at V_{IL} or V_{IH}	I	2.5			2.5			2.5			mA
----------	---	---	-----	--	--	-----	--	--	-----	--	--	----

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,

$T_A = 0$ to 70°C for Commercial Grade Units,

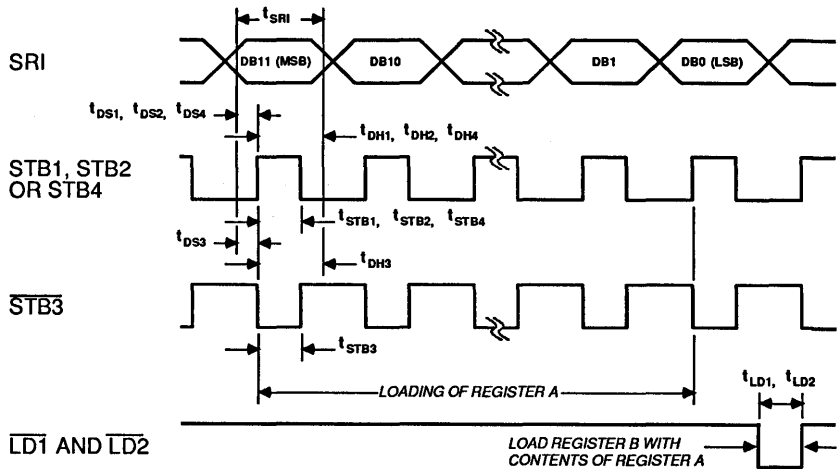
$T_A = -25$ to 85°C for Industrial Grade Units,

$T_A = -55$ to 125°C for Military Grade Units

(Please Refer to Ordering Information for Grade Descriptions)

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G MIN TYP MAX	HDAC7543AA MIN TYP MAX	HDAC7543AB MIN TYP MAX	UNITS	
SWITCHING CHARACTERISTICS							
Serial Input to Strobe Setup Time	t_{DS1}	STB1 strobed		50	50	50	nsec
	t_{DS2}	STB2 strobed		20	20	20	nsec
	t_{DS3}	STB3 strobed		0	0	0	nsec
	t_{DS4}	STB4 strobed		0	0	0	nsec
Serial Input to Strobe Hold Time	t_{DH1}	STB1 strobed		30	30	30	nsec
	t_{DH2}	STB2 strobed		60	60	60	nsec
	t_{DH3}	STB3 strobed		80	80	80	nsec
	t_{DH4}	STB4 strobed		80	80	80	nsec
t_{SRI} (SRI Data Pulse Width)			80	80	80	nsec	
t_{STB1} (STB1 Pulse Width)			40	40	40	nsec	
t_{STB2} (STB2 Pulse Width)			40	40	40	nsec	
t_{STB3} (STB3 Pulse Width)			40	40	40	nsec	
t_{STB4} (STB4 Pulse Width)			40	40	40	nsec	
$t_{LD1, LD2}$ (Load Pulse Width)			120	120	120	nsec	
t_{ASB} (Min. Time Between Strobing LSB Into Register A and Loading Register B)			0	0	0	nsec	
t_{CLR} (CLR Pulse Width)			100	100	100	nsec	

LOGIC TIMING DIAGRAM



Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = OUT2 = 0V, AGND = DGND,
 T_A = 0 to 70°C for Commercial Grade Units,
 T_A = -25 to 85°C for Industrial Grade Units,
 T_A = -55 to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

AC ELECTRICAL PARAMETERS (CONTINUED)	TEST CONDITIONS	TEST LEVEL	HDAC7543AA/G		HDAC7543AA		HDAC7543AB		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
Power Supply Rejection Ratio VDD = 4.75 to 5.25 V	+25°C	I	.005		.005		.005		%
		I	.01		.01		.01		
Multiplying Feedthrough Error	Note 3	II	.3	.5	.3	.5	.3	.5	mVPP
C _{OUT1,2} (Output Capacitance)	DAC REG. = ALL 0'S	II	30		30		30		pF
C _{OUT1,2} (Output Capacitance)	DAC REG. = ALL 1'S	II	75		75		75		pF
Output Current Settling Time	Note 4	II	0.5	1	0.5	1	0.5	1	μsec.

NOTES: 3. VREF = ±10 V @ 10 KHz Sinewave.
 4. Measured to 0.5 LSB from falling edge of LD1 and LD2. Load on pin OUT1 = 100 Ω + 13 pF.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

Parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore T_J = T_C = T_A.

<u>TEST LEVEL</u>	<u>TEST PROCEDURE</u>
I	Production tested.
II	Guaranteed by design and sampled characterization data.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7543A ideal full-scale output is $-(4095)/(4096) \cdot (VREF)$. Gain error is adjustable to zero using external trims as shown in Figures 5 and 6 and Table II.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's or at OUT2 with the DAC loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the VREF terminal to OUT1 with the DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GENERAL CIRCUIT DESCRIPTION

As shown in the Block Diagram of the cover sheet, the HDAC7543A consists of a 12-bit multiplying DAC and data input logic. The data input logic consists of a serial input data register (Register A) and a parallel DAC register (Register B). Register A loads Register B with a 12-bit parallel data word. The content of Register B controls the DAC's output. Data entry is further described in the Interface Logic section.

Figure 1 shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7543A

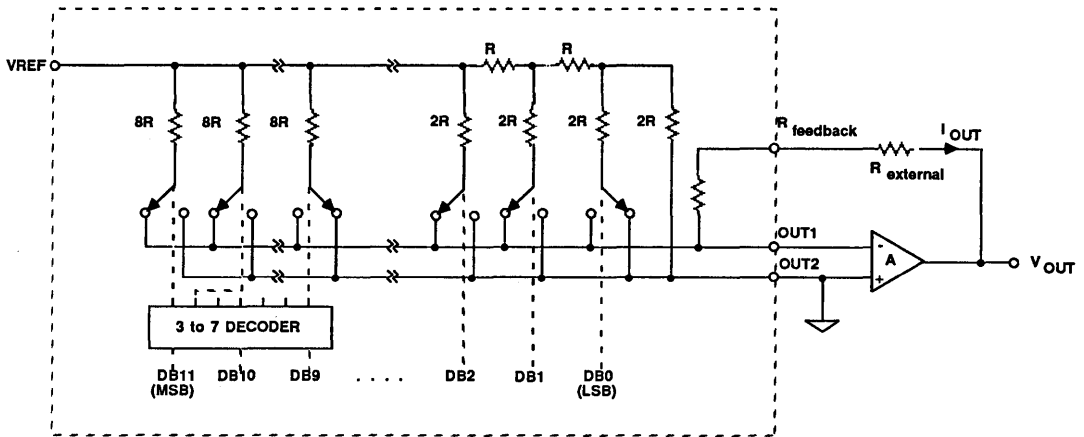


FIGURE 1 SIMPLIFIED HDAC7543A DAC CIRCUITRY (WITH EXTERNAL OP AMP)

uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7543A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the (remaining) VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switch routes the bit-weighted current of the leg to either pin OUT1 (output) or to pin OUT2 (analog ground). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the 3 most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7543A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the optional external resistor of Figure 1 in series with internal resistor $R_{feedback}$. The operational amplifier provides a buffered V_{OUT} , and in combination with the feedback resistance, maintains OUT1 at virtual ground. The transfer function of Figure 2 shows the relationship of V_{OUT} for an equivalent R-2R resistor network, shown in the same figure. A more detailed understanding of the circuit operation and performance aspects are found in the following Equivalent Circuit Analysis section.

EQUIVALENT CIRCUIT ANALYSIS

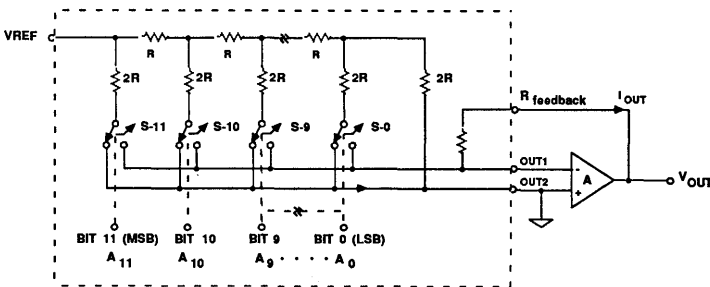
The equivalent output circuit of the HDAC7543A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In Figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to pin OUT2 which is externally connected to analog ground. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin VREF plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to Figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in Figures 3 and 4.

The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between Figures 3 and 4, resistance at each op-amp input can change from 10K Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below: (next page)



The transfer function for the equivalent network shown is:

$$V_{OUT} = -VREF \cdot \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \dots + \frac{A_0}{2^{12}} \right)$$

where A_x assumes a value of 1 for a "HIGH" bit and 0 for a "LOW" bit.

FIGURE 2 EQUIVALENT R-2R RESISTOR NETWORK FOR THE HDAC7543A DAC CIRCUITRY (WITH EXTERNAL OP AMP)

FIGURE 3
HDAC7543A DAC EQUIVALENT CIRCUIT
 ALL DIGITAL INPUTS LOW
 (WITH EXTERNAL OP AMP)

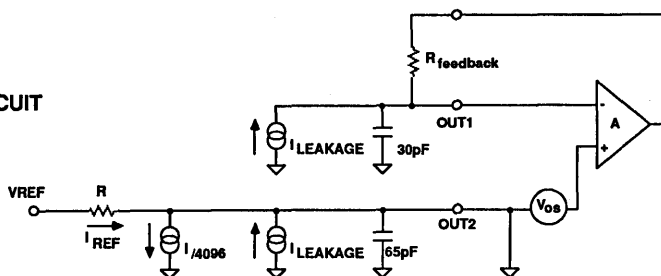
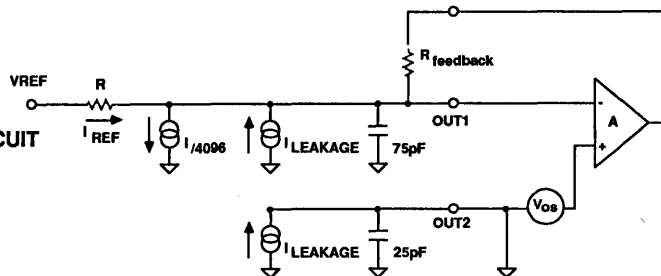


FIGURE 4
HDAC7543A DAC EQUIVALENT CIRCUIT
 ALL DIGITAL INPUTS HIGH
 (WITH EXTERNAL OP AMP)



Offset gain = $1 + R_{feedback}/RDAC$

With all code bits LOW:
 $RDAC \gg R_{feedback}$; offset gain = 1

With all code bits HIGH:
 $RDAC = R_{feedback}$; offset gain = 2

Thus, the offset is not amplified by a constant gain over the range of code inputs. This variation in offset gain is seen as a non-linearity in the voltage output over the full scale output. The magnitude of non-linearity is the difference in the gains at code extremes times the offset voltage. In this DAC, the non-linearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (Figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (Figures 5 and 6). Although all R-2R DAC's have the need for this type of compensation,

the HDAC7543A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7543A.

The choice of compensation capacitor is bounded by three limits:

- C1 along with $R_{feedback}$ determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and $R_{feedback}$ should be smaller than secondary poles in the op-amp - as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{OUT1} + C1}$.

For an OP-17 used as an output op-amp with a 30 MHz gain-bandwidth, the choice of C1 would be:

$$(2 \cdot \pi \cdot C1 \cdot R_{feedback})^{-1} = 15 \text{ MHz,}$$

$$\text{or } C1 \approx 15 \text{ pf} \quad (R_{feedback} \approx 12.5 \text{ K}\Omega)$$

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7543A's low output capacitance comes much closer to fulfilling this goal than most other 7543 compatible DAC's. Thus, faster, more well controlled settling is obtained with the HDAC7543A.

REGISTER A CONTROL INPUTS				REGISTER B CONTROL INPUTS			HDAC7543A OPERATION
STB4	STB3	STB2	STB1	CLR	LD2	LD1	
0	1	0	▲	X	X	X	DATA APPEARING AT SRI IS STROBED INTO REGISTER A (MSB FIRST)
0	1	▲	0	X	X	X	
0	▼	0	0	X	X	X	
▲	1	0	0	X	X	X	
1	X	X	X				NO OPERATION OF REGISTER A
X	0	X	X				
X	X	1	X				
X	X	X	1				
				0	X	X	SET REG. B TO 0000 0000 0000 (1)
				1	1	X	NO OPERATION OF REGISTER B
				1	X	1	
				1	0	0	LOAD REG. B WITH CONTENTS OF REGA

0 = LOGIC LOW
 1 = LOGIC HIGH
 X = DON'T CARE
 ▲ = POSITIVE EDGE
 ▼ = NEGATIVE EDGE

NOTE (1):
 CLR = 0 ASYNCHRONOUSLY RESETS REGISTER B TO 0000 0000 0000 BUT HAS NO EFFECT ON REGISTER A

TABLE I INPUT LOGIC TRUTH TABLE

INTERFACE LOGIC

Data is loaded into the HDAC7543A serially through pin SRI. The serial data is clocked into Register A with either pin STB1, STB2 or STB4 at the rising clock edge or with pin STB3 at the falling clock edge. When Register A has been loaded with the 12 data bits, the data is transferred to Register B by bringing both pin LD1 and LD2 momentarily low. Refer to the Logic Timing Diagram of page 4 for loading sequence. Table I above provides the logic truth table.

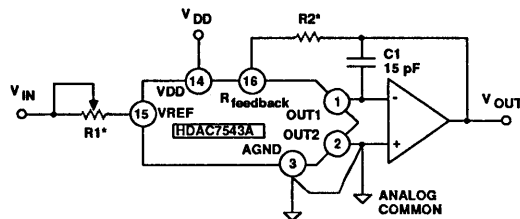
When pin CLR is momentarily brought to logic 0, Register B is reset to 0000 0000 0000. This feature is useful for system initialization since the DAC output is set to a known condition.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

Figure 5 illustrates the use of the HDAC7543A in a unipolar (or 2 quadrant multiplication) mode. Data input pins have been omitted for clarity. The VREF is applied as a voltage from pin 15 to ground or an input current can be applied to pin 15. Positive or negative voltages/currents can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of the VREF voltage out. If the source of VREF is adjustable, VREF could be directly adjusted for full scale calibration (refer to table III).

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This compensates for the feedback pole caused by OUT1's capacitance.



*REFER TO TABLE II.

FIGURE 5 UNIPOLAR BINARY OPERATION

The op-amp used with the HDAC7543A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the fact that the offset effect is code dependant and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

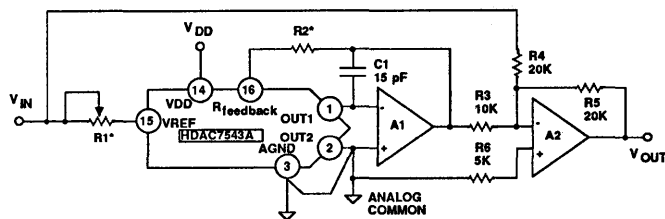
BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7543A in a bipolar (or 4 quadrant multiplication) mode is illustrated in Figure 6. The VREF is applied from pin 15 to ground voltage or an input current can be applied to pin 15. Positive or negative voltages/currents can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of VREF to produce a maximum output which is half of VREF in either polarity (see Table IV for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the VREF source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track one another for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate for OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.



* REFER TO TABLE II.

FIGURE 6 BIPOLAR OPERATION

	TRIM RESISTOR	
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

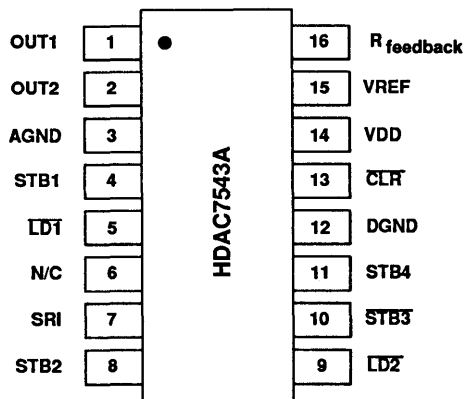
TABLE II
RECOMMENDED TRIM RESISTANCE

BINARY NUMBER IN DAC			ANALOG OUTPUT, V _{OUT}
MSB		LSB	
1111	1111	1111	$-V_{IN} \left(\frac{4095}{4096} \right)$
1000	0000	0000	$-V_{IN} \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$
0000	0000	0001	$-V_{IN} \left(\frac{1}{4096} \right)$
0000	0000	0000	0 Volts

TABLE III
UNIPOLAR BINARY CODE
FOR CIRCUIT OF FIGURE 6

BINARY NUMBER IN DAC			ANALOG OUTPUT, V _{OUT}
MSB		LSB	
1111	1111	1111	$+V_{IN} \left(\frac{2047}{2048} \right)$
1000	0000	0001	$+V_{IN} \left(\frac{1}{2048} \right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN} \left(\frac{1}{2048} \right)$
0000	0000	0000	$-V_{IN} \left(\frac{2048}{2048} \right)$

TABLE IV
BIPOLAR CODE
FOR CIRCUIT OF FIGURE 7



PIN	PIN NAME	FUNCTION
1	OUT1	ANALOG CURRENT OUTPUT 1
2	OUT2	ANALOG CURRENT OUTPUT 2
3	AGND	ANALOG GROUND
4	STB1	STROBE INPUT 1 FOR REG. A
5	LD1	LOAD INPUT 1 FOR REG. B
6	N/C	NO CONNECTION
7	SRI	SERIAL DATA INPUT
8	STB2	STROBE INPUT 2 FOR REG. A
9	LD2	LOAD INPUT 2 FOR REG. B
10	STB3	STROBE INPUT 3 FOR REG. A
11	STB4	STROBE INPUT 4 FOR REG. A
12	DGND	DIGITAL GROUND
13	CLR	CLEAR INPUT FOR REG. B
14	VDD	POSITIVE POWER SUPPLY
15	VREF	REFERENCE VOLTAGE INPUT
16	Rfeedback	INTERNAL FEEDBACK RESISTOR

**HDAC7543A PIN ASSIGNMENT
(TOP VIEW)**

HDAC7543A PIN FUNCTIONS

***For Ordering Information See Section 1.*

NOTES:

CMOS 12-BIT BUFFERED MULTIPLYING DAC

FEATURES:

- Improved Version of the AD7545
- **Maximum Gain Error < 2 LSB**
- **Low Output Capacitance (< 75 pf.)**
- **500 ns Settling Time**
- 12-Bit Linearity Over Temperature
- 8 or 16-Bit Bus Compatible

APPLICATIONS:

- μ P Controlled Gain Circuits
- μ P Controlled Function Generation
- Bus Structured Instruments
- μ P Based Control Systems

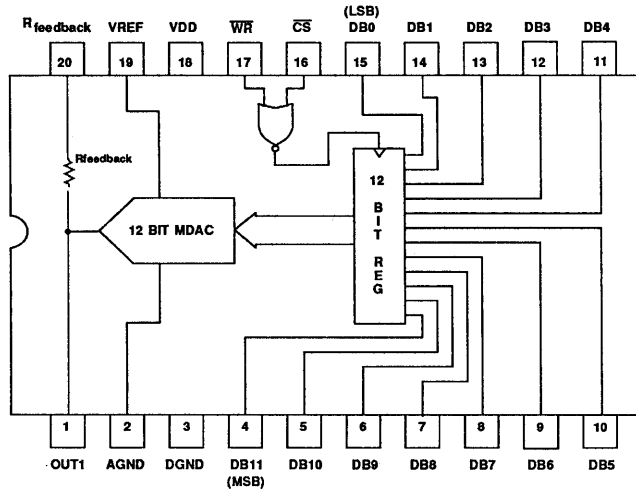
GENERAL DESCRIPTION

The HDAC7545A is a monolithic, low cost, multiplying 12-bit digital to analog converter (DAC) designed for direct microprocessor interface. It is compatible with the industry standard 7545 but has significant performance improvements in speed and gain accuracy. The HDAC7545A is fabricated in a 3 micron, polysilicon gate BEMOS process and operates from a single +5 volt (maximum) supply. Excellent linearity and gain accuracy are achieved through the use of laser-trimmed thin film resistors. Latch-up immunity is insured by the use of an epi process base; this eliminates the need for external Schottky clamping diodes for latch-up protection.

The HDAC7545A incorporates a parallel loading architecture for the DAC conversion bits. When pins \overline{CS} and \overline{WR} are low, the twelve input data registers read the bus data. This single load and convert operation allows one-cycle updating by 16-bit microprocessors.

With direct parallel bus data loading, the HDAC7545A is ideally suited for microprocessor-based instruments and industrial or process controllers.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25°C

Supply Voltages

V_{DD} to DGND.....+7V
 AGND to DGND.....-0.3 to VDD

Input Voltages

Digital Inputs to DGND.....-0.3 to VDD
 VRfeedback or VREF to DGND.....±25V

Outputs

V_{OUT1} to GND.....-0.3V to VDD

Temperature

Operating Temperature, ambient.....-55 to +125°C
 junction.....+150°C
 Lead Temperature, (soldering 10 seconds).....+300°C
 Storage Temperature.....-65 to +150°C
 Power Dissipation (Any Package) to +75°C.....450mW
 (derates above 75°C by 6 mW/°C)

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. CAUTION - ESD SENSITIVE DEVICE: The logic and analog ports of this device have special circuits to protect it against ESD damage. Although this protection should prevent permanent damage to the inputs, care should be taken in handling.

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = 0V, AGND = DGND,
 T_A = 0 to 70°C for Commercial Grade Units,
 T_A = -25 to 85°C for Industrial Grade Units,
 T_A = -55 to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

DC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7545AA/G	HDAC7545AA	HDAC7545AB	UNITS
			MIN TYP MAX	MIN TYP MAX	MIN TYP MAX	

ACCURACY

Resolution		I	- 12 -	- 12 -	- 12 -	bits
Relative Accuracy		I	-1/2 ±1/4 +1/2	-1/2 +1/2	-1 +1	LSB
Differential Nonlinearity		I	-1/2 ±1/4 +1/2	-1/2 +1/2	-1 +1	LSB
Gain Error, Using R _{feedback}	25°C	I	-1/2 +1/2	-2 +2	-3 +3	LSB
Gain Error, Using R _{feedback}	T _{min} - T _{max}	I	-1.5 +1.5	-3 +3	-4 +4	LSB
Gain Temperature Coefficient		II	0.3 3	0.3 3	0.3 3	ppm/°C

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = 0V, AGND = DGND,
 $T_A = 0$ to 70°C for Commercial Grade Units,
 $T_A = -25$ to 85°C for Industrial Grade Units,
 $T_A = -55$ to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

DC ELECTRICAL PARAMETERS (CONTINUED)	TEST CONDITIONS	TEST LEVEL	HDAC7545AA/G			HDAC7545AA			HDAC7545AB			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	

OUTPUT LEAKAGE (3)

Pin OUT1	25°C	I	-5	+5	-5	+5	-5	+5	nA
Pin OUT1	Military Grades	I	-100	+100	-100	+100	-100	+100	nA
	Other Grades	I	-10	+10	-10	+10	-10	+10	nA

INPUT RESISTANCE

Input VREF	Pin 19 to GND 25°C	I	7	12.5	18	7	12.5	18	7	12.5	18	K Ω
Input VREF Temp. Coefficient		II	-180			-180			-180			ppm/°C

LOGIC INPUTS

V_{IH} (High input voltage)		I	2.0			2.0			2.0			Volts
V_{IL} (Low input voltage)		I	0.8			0.8			0.8			Volts
I_{IN} (Input current)		I	1			1			1			μA
C_{IN} (Input capacitance) of Pins DB0 - DB11, \overline{WR} , \overline{CS}	$V_{IN} = 0\text{V}$	II	5			5			5			pF

POWER SUPPLY

I_{DD}	All Logic Inputs at V_{IL} or V_{IH}	I	4			4			4			mA
I_{DD}	Logic Inputs at 0V or VDD, 25°C	I	10	100	10	100	10	100	10	100	μA	
I_{DD}	Logic Inputs at 0V or VDD	I	500			500			500			μA

NOTE 3. Digital inputs \overline{WR} and \overline{CS} at 0 volts.

ELECTRICAL SPECIFICATIONS

Test Conditions: Unless Otherwise Noted, VDD = 5V, VREF = +10V, OUT1 = 0V, AGND = DGND,
 $T_A = 0$ to 70°C for Commercial Grade Units,
 $T_A = -25$ to 85°C for Industrial Grade Units,
 $T_A = -55$ to 125°C for Military Grade Units
 (Please Refer to Ordering Information for Grade Descriptions)

AC ELECTRICAL PARAMETERS	TEST CONDITIONS	TEST LEVEL	HDAC7545AA/G		HDAC7545AA		HDAC7545AB		UNITS
			MIN	TYP MAX	MIN	TYP MAX	MIN	TYP MAX	
Digital to Analog Glitch Impulse	VREF = AGND Note 4	II	200	400	200	400	200	400	nV-sec
Multiplying Feedthrough Error	Note 5	II	.3	.5	.3	.5	.3	.5	mVPP
C _{OUT} (Output Capacitance)	DB0-11=0V WR=CS=0V	II		30		30		30	pF
C _{OUT} (Output Capacitance)	DB0-11=VDD WR=CS=0V	II		75		75		75	pF
Output Current Settling Time	Note 4, 6	II	0.5	1	0.5	1	0.5	1	μsec.
Propagation Delay	Note 7	II	50	100	50	100	50	100	nsec.
t _{CS} (Chip select set-up time)		I	60		60		60		nsec.
t _{CH} (Chip select hold time)		I	0		0		0		nsec.
t _{WR} (WR pulse width)	t _{CS} ≥ t _{WR}	I	100		100		100		nsec.
t _{DS} (Data set-up time)		I	50		50		50		nsec.
t _{DH} (Data hold time)		I	9		9		9		nsec.

- NOTES: 4. Load on Pin OUT1 = 100 Ω + 13 pF.
 5. VREF = ±10 V @ 10 KHz Sinewave.
 6. Measured from falling edge of WR.
 7. Measured from falling edge of WR to 90% of final output value.

ELECTRICAL CHARACTERISTICS TESTING

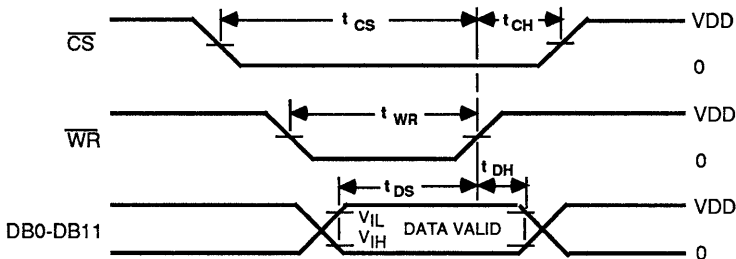
All electrical characteristics are subject to the following conditions:

Parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	Production tested.
II	Parameter is guaranteed by design and sampled characterization data.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:

\overline{CS} and \overline{WR} low, DAC responds to data inputs DB0-DB11.

HOLD MODE:

Either \overline{CS} or \overline{WR} high, data inputs DB0-DB11 are locked out; DAC holds last data present when \overline{WR} or \overline{CS} assumes high state.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB (max) over the operating temperature range ensures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the HDAC7545A ideal full-scale output is $-(4095)/(4096) \cdot (VREF)$. Gain error is adjustable to zero using external trims as shown in Figures 6 and 7 and Table I.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0's.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from the VREF terminal to OUT1 with the DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

Time required for the output of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV-secs and is measured with VREF=GND.

GENERAL CIRCUIT DESCRIPTION

As shown in the Block Diagram of the cover sheet, the HDAC7545A consists of a 12-bit multiplying DAC and a 12-bit data latch. Data at pins DB0 - DB11 is latched when both pins CS and WR are low. Current latched data establishes the digital-to-analog conversion code, therefore, conversion is actually controlled by pins \overline{CS} and \overline{WR} . This is further described in the Interface Logic section.

Figure 1 shows a simplified version of the 12-bit multiplying DAC circuitry. Note that the HDAC7545A

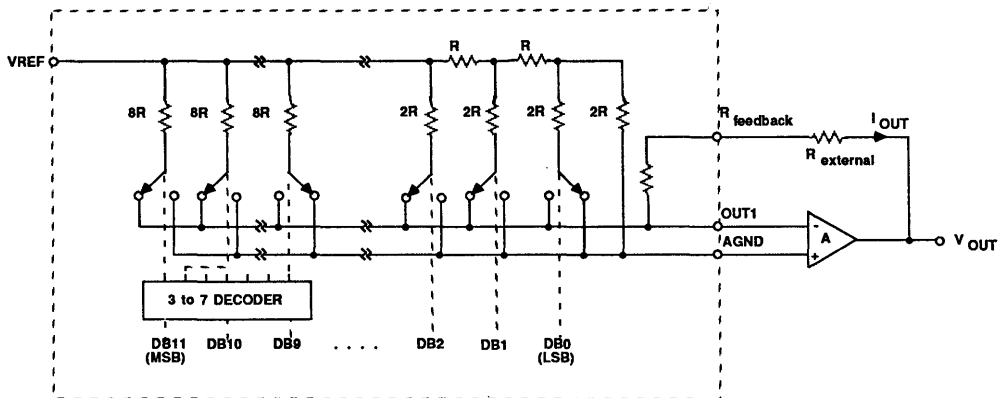


FIGURE 1 SIMPLIFIED HDAC7545A DAC CIRCUITRY (WITH EXTERNAL OP AMP)

uses a modified R-2R ladder technique that provides for superior linearity over similar devices which use the basic R-2R ladder.

A basic R-2R ladder portion is used within the HDAC7545A for the nine least-significant bits (bits 0-8). This ladder portion successively divides the (remaining) VREF input to produce a binary weighted nine-stage current division. In other words, in moving from left to right, each 2R resistor leg has half the current flow of the previous leg. Double-pole switches within each leg are controlled by the respective input data bit. The switch routes the bit-weighted current of the leg to either analog ground or to the output (pin OUT1). OUT1 is a virtual ground by means of the external active circuitry. Hence, with every switch in either position, the R-2R ladder resistive integrity is maintained. Input resistance of pin VREF is kept constant.

Modification of the basic R-2R ladder structure occurs in the 3 most-significant bits. Here, the switches of seven equally weighted current dividers are controlled by bits 9-11 via a logic decoder. Although more complex, this method provides increased accuracy. Application of the HDAC7545A is identical to similar devices that use an unmodified R-2R ladder network.

The DAC output current is converted to a voltage by the feedback resistance composed of the external resistor of Figure 1 in series with internal resistor R_{feedback}. The operational amplifier provides a buffered V_{OUT}, and in combination with the feedback resistance, maintains OUT1 at virtual ground. The transfer function of Figure 2 shows the relationship of V_{OUT} for an equivalent R-2R resistor network, shown in the same figure. A more detailed understanding of the circuit operation and performance aspects are found in the following Equivalent Circuit Analysis section.

EQUIVALENT CIRCUIT ANALYSIS

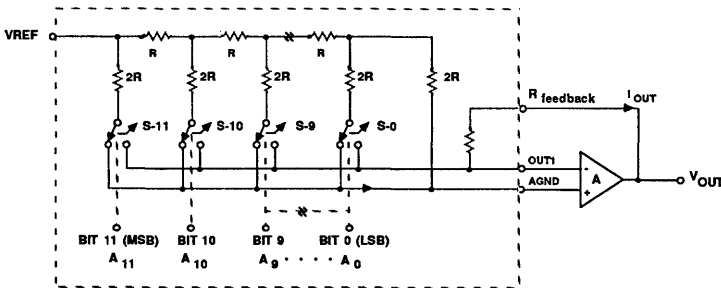
The equivalent output circuit of the HDAC7545A is the key to understanding offset, linearity and settling time. Figures 3 and 4 illustrate these effects.

In Figure 3, the equivalent unipolar operation is illustrated with an external op-amp and all switches LOW to route all current to pin OUT2. OUT2 is internally connected to AGND in packaged versions of the HDAC7545A. The current from OUT2 is composed of (4095/4096)-th's of the input current at pin VREF plus parasitic leakage currents of the switches. These leakage currents are due to both junction and surface leakage on the MOS switches. 1/4096-th of the input current passes to the ground through the ladder terminal 2R resistor. OUT1 DC current is due only to switch leakage.

Figure 4 shows the same equivalent circuit when all switches are HIGH thereby routing all current to OUT1. The conditions are symmetrical in this case to Figure 3.

The main effect of switch leakages in either case is an offset voltage from the DAC when used in voltage output mode as shown in Figures 3 and 4.

The output resistance seen at the input terminals of the op-amp varies with the code chosen. Between Figures 3 and 4, resistance at each op-amp input can change from 10K Ohms to an open for extremes in code. This causes the gain of the offsets (due to either leakage currents of the DAC or op-amp offset) to be code dependent. For example, the gain of offsets of the op-amp under these extreme cases is given below: (next page)



The transfer function for the equivalent network shown is:

$$V_{OUT} = -V_{REF} \cdot \left(\frac{A_{11}}{2^1} + \frac{A_{10}}{2^2} + \dots + \frac{A_0}{2^{12}} \right)$$

where A_x assumes a value of 1 for a "HIGH" bit and 0 for a "LOW" bit.

FIGURE 2 EQUIVALENT R-2R RESISTOR NETWORK FOR THE HDAC7545A DAC CIRCUITRY (WITH EXTERNAL OP AMP)

FIGURE 3
HDAC7545A DAC EQUIVALENT CIRCUIT
 ALL DIGITAL INPUTS LOW
 (WITH EXTERNAL OP AMP)

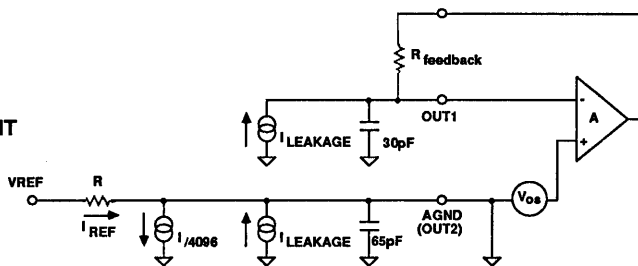
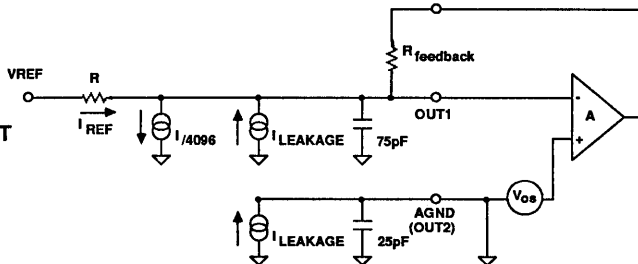


FIGURE 4
HDAC7545A DAC EQUIVALENT CIRCUIT
 ALL DIGITAL INPUTS HIGH
 (WITH EXTERNAL OP AMP)



Offset gain = $1 + R_{\text{feedback}}/RDAC$

With all code bits LOW:
 $RDAC \gg R_{\text{feedback}}$; offset gain = 1

With all code bits HIGH:
 $RDAC = R_{\text{feedback}}$; offset gain = 2

Thus, the offset is not amplified by a constant gain over the range of code inputs. This variation in offset gain is seen as a non-linearity in the voltage output over the full scale output. The magnitude of non-linearity is the difference in the gains at code extremes times the offset voltage. In this DAC, the non-linearity is equal to the offset itself. Thus, the total offset voltage of the op-amp plus leakage induced offset of the DAC and op-amp must be kept to less than 1 LSB to prevent degradation to the DAC linearity performance.

The dynamic output impedance of OUT1 and OUT2 is composed of the DAC switch capacitances to ground. OUT2 has the capacitance of the OFF switches while OUT1 has switch capacitance for ON switches.

The capacitance on OUT1 creates a feedback pole in the voltage output operation mode (Figures 3 and 4). Instability of the output amplifier can occur due to the presence of this pole. This pole's instability effect is typically compensated by the use of a feedback capacitor - C1 (Figures 6 and 7). Although all R-2R DAC's have the need for this type of compensation,

the HDAC7545A maintains faster settling times when used in the voltage output mode. This is due to the lower output capacitance of the HDAC7545A.

The choice of compensation capacitor is bounded by three limits:

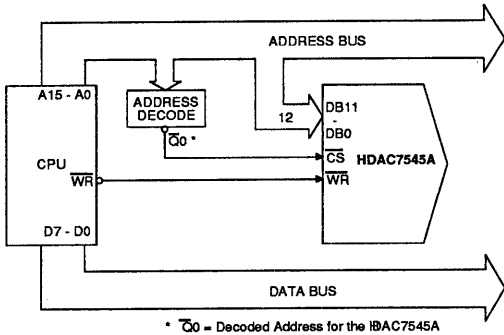
- C1 along with R_{feedback} determines the settling time of the output voltage from the op-amp; therefore C1 should be as small as possible for minimum settling time.
- The pole defined by C1 and R_{feedback} should be smaller than secondary poles in the op-amp - as a rule of thumb, about one half of the op-amp's gain-bandwidth.
- Settling time is proportional to $\sqrt{C_{\text{OUT1}} + C1}$.

For an OP-27 used as an output op-amp with an 8 MHz gain-bandwidth, the choice of C1 would be:

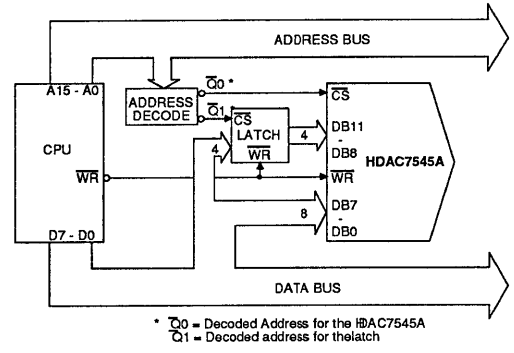
$$(2 \cdot \pi \cdot C1 \cdot R_{\text{feedback}})^{-1} = 4 \text{ MHz,}$$

$$\text{or } C1 \approx 4 \text{ pf} \quad (R_{\text{feedback}} \approx 12.5 \text{ K}\Omega)$$

Fast settling time with small amounts of ringing are obtained when the small values of C1 (given by the criteria above) are as close as possible to the DAC output capacitance. The HDAC7545A's low output capacitance comes much closer to fulfilling this goal than most other 7545 compatible DAC's. Thus, faster, more well controlled settling is obtained with the HDAC7545A.



MULTIPLEXED BUS ARCHITECTURE



SEPARATE ADDRESS/DATA BUS ARCHITECTURE

FIGURE 5 TYPICAL MICROPROCESSOR BUS INTERFACES FOR HDAC7545A

INTERFACE LOGIC

The HDAC7545A is designed to allow control of the output via a parallel microprocessor bus I/O. This section describes operation of the interface controls to accomplish this.

A typical parallel bus I/O configuration is shown in figure 5. The microprocessor provides the DAC code as well as all control signals to load the code and update the analog output. During loading the HDAC7545A accepts the DAC input code in a 12 bit word.

When the \overline{CS} pin is at logic "0", the input register of the HDAC7545A is enabled. The \overline{WR} input actually stobs the input data from the parallel bus into the HDAC7545A data register. This occurs on the falling edge of this \overline{WR} pulse. The Write Timing Diagram of page 4 defines the minimum set-up and hold times required by the control lines to successfully transfer data in this fashion.

UNIPOLAR BINARY OPERATION - 2 QUADRANT MULTIPLICATION

Figure 6 illustrates the use of the HDAC7545A in a unipolar (or 2 quadrant multiplication) mode. The VREF is applied from pin 19 to ground voltage or an input current can be applied to pin 19. Positive or negative voltages/currents can be applied. The input is multiplied by (-1) times the DAC code scaling.

R1 can be used to provide full scale output trimming capability. The adjustment is made by selecting code 1111 1111 1111 and changing R1 for (4095/4096) of

the VREF voltage out. If the source of VREF is adjustable, VREF could be directly adjusted for full scale calibration (refer to table II).

The output capacitance of OUT1 must be compensated as described in Equivalent Circuit Analysis by the use of C1 in the feedback path. This cancels the feedback pole caused by OUT1's capacitance.

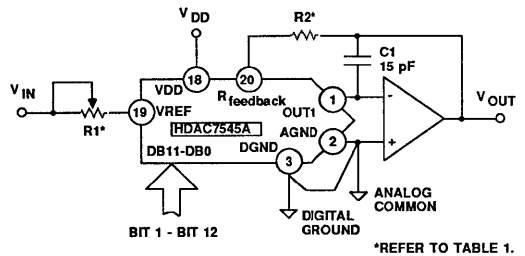


FIGURE 6 UNIPOLAR BINARY OPERATION

The op-amp used with the HDAC7545A should be selected for low offset voltage and low bias currents to reduce offset and linearity errors as described in Equivalent Circuit Analysis. The op-amp's bias currents appear as errors in the same fashion as the DAC's leakage currents. The op-amp offset voltage should be less than approximately 10% of an LSB (of the output full scale voltage). This is due to the fact that the offset effect is code dependant and contributes to the nonlinearity in proportion to its size with respect to full scale output voltage.

BIPOLAR OPERATION - 4 QUADRANT MULTIPLICATION

The use of the HDAC7545A in a bipolar (or 4 quadrant multiplication) mode is illustrated in Figure 7. The VREF is applied from pin 19 to ground voltage or an input current can be applied to pin 19. Positive or negative voltages/currents can be applied. The output is either +1 or -1 times the code scaling of the DAC. The polarity is selected by the MSB of the DAC input code.

Amplifier A1's output is subtracted from 1/2 the value of VREF to produce a maximum output which is half of VREF in either polarity (see Table 3 for the exact scaling). The MSB of the DAC selects the polarity of the output.

Full scale calibration of the output can be made by adjusting R5 or the VREF source itself. Calibration of the zero output at code 1000 0000 0000 is made by adjusting R1. It is key that R3, R4 and R5 track one another for the stability of the summation made at A2. Failure of these resistors to track will result in both gain and offset drift over temperature even though calibration is done at room temperature.

As with unipolar operation, C1 is needed to compensate for OUT1 capacitance. A1 must be selected for low offset voltage and bias current to minimize nonlinearity and offset errors.

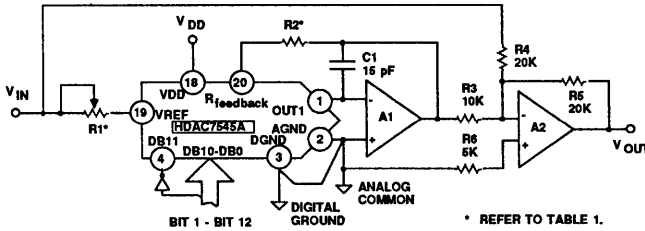


FIGURE 7 BIPOLAR OPERATION

	TRIM RESISTOR	
	"A" grades	"B" grades
R1	20Ω	100Ω
R2	6.8Ω	33Ω

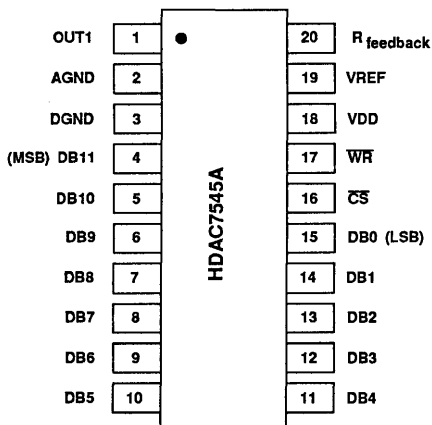
TABLE I
RECOMMENDED TRIM RESISTANCE

BINARY NUMBER IN DAC			ANALOG OUTPUT, V _{OUT}
MSB		LSB	
1111	1111	1111	$-V_{IN} \left(\frac{4095}{4096} \right)$
1000	0000	0000	$-V_{IN} \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$
0000	0000	0001	$-V_{IN} \left(\frac{1}{4096} \right)$
0000	0000	0000	0 Volts

TABLE II
UNIPOLAR BINARY CODE
FOR CIRCUIT OF FIGURE 6

BINARY NUMBER IN DAC			ANALOG OUTPUT, V _{OUT}
MSB		LSB	
1111	1111	1111	$+V_{IN} \left(\frac{2047}{2048} \right)$
1000	0000	0001	$+V_{IN} \left(\frac{1}{2048} \right)$
1000	0000	0000	0V
0111	1111	1111	$-V_{IN} \left(\frac{1}{2048} \right)$
0000	0000	0000	$-V_{IN} \left(\frac{2048}{2048} \right)$

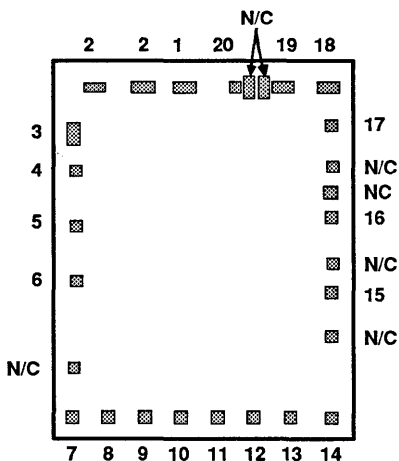
TABLE III
BIPOLAR CODE
FOR CIRCUIT OF FIGURE 7



PIN	PIN NAME	FUNCTION
1	OUT1	ANALOG CURRENT OUTPUT
2	AGND	ANALOG GROUND
3	DGND	DIGITAL LOGIC GROUND
4	DB11	INPUT DATA BIT 11 (MSB)
5	DB10	INPUT DATA BIT 10
6	DB9	INPUT DATA BIT 9
7	DB8	INPUT DATA BIT 8
8	DB7	INPUT DATA BIT 7
9	DB6	INPUT DATA BIT 6
10	DB5	INPUT DATA BIT 5
11	DB4	INPUT DATA BIT 4
12	DB3	INPUT DATA BIT 3
13	DB2	INPUT DATA BIT 2
14	DB1	INPUT DATA BIT 1
15	DB0	INPUT DATA BIT 0 (LSB)
16	CS	CHIP SELECT
17	WR	DATA WRITE
18	VDD	POSITIVE POWER SUPPLY
19	VREF	REFERENCE INPUT VOLTAGE
20	R _{feedback}	INTERNAL FEEDBACK RESISTOR

HDAC7545A PIN ASSIGNMENT (TOP VIEW)

HDAC7545A PIN FUNCTIONS



N/C = No Connection.

HDAC7545A DIE PLOT BONDING PAD LOCATION

Die Size 130 x 106 mils

**For Ordering Information See Section 1.

NOTES:

8-BIT, HIGH SPEED D/A CONVERTERS

FEATURES

- 275 MWPS Conversion Rate - A Version
- 165 MWPS Conversion Rate - B Version
- Compatible with TDC1018 with Improved Performance
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Registered Data And Video Controls
- Differential Current Outputs

APPLICATIONS

- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

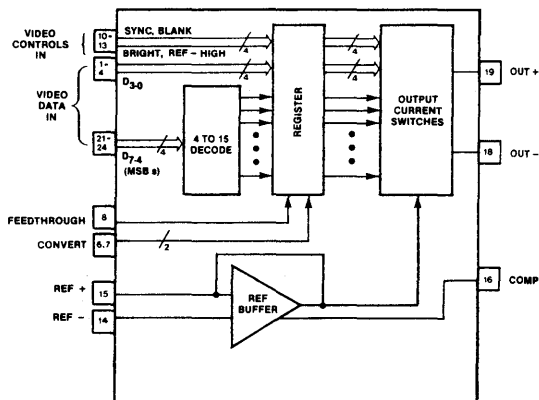
3

GENERAL DESCRIPTION

The HDAC10180 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10180 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC10180 is

pin-compatible with the TDC1018, with improved performance, and two can be used with the HDAC10181. The HDAC10180 contains data and control input registers, video control logic, reference buffer, and current switches in 24 Lead CERDIP, or ceramic sidebrazed DIP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which the useful life will be impaired)¹

Supply Voltages

V_{EED} (measured to V_{CCD})	- 7.0 to 0.5V
V_{EEA} (measured to V_{CCA})	- 7.0 to 0.5V
V_{CCA} (measured to V_{CCD})	- 0.5 to 0.5V

Temperature

Operating, Ambient	- 60 to + 140 °C
Junction	+ 175 °C
Lead, Soldering (10 seconds)	+ 300 °C
Storage	- 60 to + 150 °C

Input Voltages

CONV, Data, and Controls V_{EED} to 0.5V
(measured to V_{CCD})

$REF +$ (measured to V_{CCA})	V_{EEA} to 0.5V
$REF -$ (measured to V_{CCA})	V_{EEA} to 0.5V

Notes:

1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
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DC ELECTRICAL CHARACTERISTICS $V_{CCA} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25^\circ C, C_C = 0pF, I_{SET} = 1.105 mA$

E_{LI}	Integral Linearity Error	1.0mA < I_{SET} < 1.3mA	I	- 0.37 - 0.95	+ 0.37 + 0.95	% Full Scale LSB
E_{LD}	Differential Linearity Error	1.0mA < I_{SET} < 1.3mA	I	- 0.2 - 1/2	+ 0.2 + 1/2	% Full Scale LSB
E_G	Gain Error		I	- 5	+ 5	% Full Scale
TC_G	Gain Error Tempco		V	- 150		PPM/°C
C_{REF}	Input Capacitance, REF +, REF -		V	5		pF
V_{OCP}	Compliance Voltage, + Output		I	- 1.2	1.5	V
V_{OCN}	Compliance Voltage, - Output		I	- 1.2	1.5	V
R_{OUT}	Equivalent Output Resistance		I	20		K Ohm
C_{OUT}	Output Capacitance		V	12		pF
I_{OP}	Maximum Current, + Output		IV	45		mA
I_{ON}	Maximum Current, - Output		IV	45		mA
I_{OS}	Output Offset Current		I		1/2	LSB
V_{IH}	Input Voltage, Logic HIGH		I	- 1.0		V
V_{IL}	Input Voltage, Logic LOW		I		- 1.5	V
V_{ICM}	Convert Voltage, Common Mode Range		I	- 0.5	- 2.5	V
V_{IDF}	Convert Voltage, Differential		IV	0.4	1.2	V
I_{IL}	Input Current, Logic LOW, Data and Controls		I		120	μA

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL				UNITS
			MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS $V_{CCA} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25^\circ C, C_C = 0pF, I_{SET} = 1.105 mA$

I_{IL}	Input Current, Logic LOW, Data and Controls		I		120	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls		I	10	120	μA
I_{IC}	Input Current, Convert		I	2	60	μA
C_I	Input Capacitance, Data and Controls		V	3		pF
PSR	Power Supply Sensitivity (HDAC10180)		I	- 120	+ 120	$\mu A/V$
I_{EE}	Supply Current		I	175	200	mA

3

DYNAMIC CHARACTERISTICS $R_L = 37.5 \text{ Ohms}, C_L = 5pF, T_A = 25^\circ C, I_{SET} = 1.105 mA$

F_S	Maximum Conversion Rate	B Grade A Grade	I I	165 275		MWPS
t_{RI}	Rise Time	10% to 90% G.S.	I		1.6	ns
t_{RI}	Rise Time	10% to 90% G.S. $R_L = 25 \text{ Ohms}$	IV	1.0		ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2%	IV	7		ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.8%	IV	5.5		ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2% $R_L = 25\Omega$	IV	4.5		ns
t_{DSC}	Clock to Output Delay, Clocked Mode		I		4	ns
t_{DST}	Data to Output Delay, Transparent Mode		I		6	ns
t_{PWL}	Convert Pulse Width, LOW	B Grade A Grade	I I	3.0 1.8		ns
	Glitch Energy	Area = $\frac{1}{2} VT$	V		10	pV-s
t_{PWH}	Convert Pulse Width, HIGH	B Grade A Grade	I I	3.0 1.8		ns
BW_{REF}	Reference Bandwidth, -3dB		V		1	MHz

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN TYP MAX			UNITS
			MIN	TYP	MAX	

DYNAMIC CHARACTERISTICS $R_L = 37.5 \text{ Ohms}$, $C_L = 5\text{pF}$, $T_A = 25^\circ\text{C}$, $I_{SET} = 1.105 \text{ mA}$

t_S	Set-up Time, Data and Controls		I	1.3	1.8	2	ns
t_H	Hold Time, Data and Controls		I	0.5	0		ns
SR	Slew Rate	20% to 80% G.S.	I	400			V/ μS
FT_C	Clock Feedthrough		I			-48	dB

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

- I 100% production tested at the specified temperature.
- II 100% production tested at $T_a = 25^\circ\text{C}$, and sample tested at specified temperature.
- III QA sample tested per QA test plan TA100.
- IV Parameter is guaranteed (but not tested) by design and characterization data.
- V Parameter is a typical value for information purposes only.

APPLICATION INFORMATION

The HDAC10180 is a high speed video Digital-to-Analog converters capable of up to 275 MWPS conversion rates. This makes the devices suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The HDAC10180 is separated into different conversion rate categories as shown in Table 2.

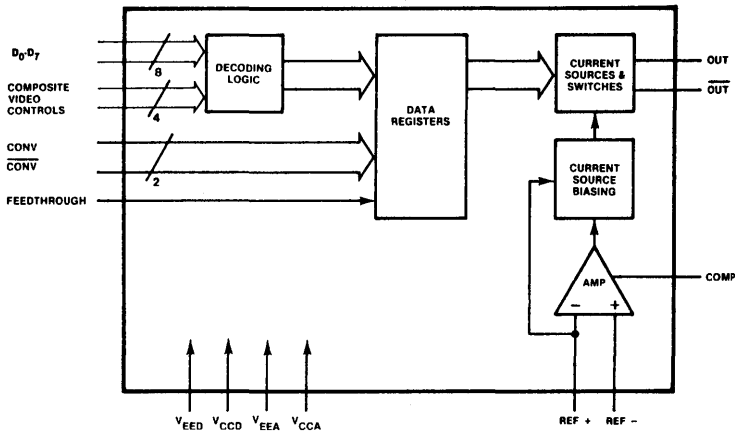
The HDAC10180 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10180 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered "VIDEO DACs".

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10180 in a color raster application is shown in Figure 2. The HDAC10180 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10180 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10180. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10180 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10180 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_s and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_s .

FIGURE 1 TIMING DIAGRAM

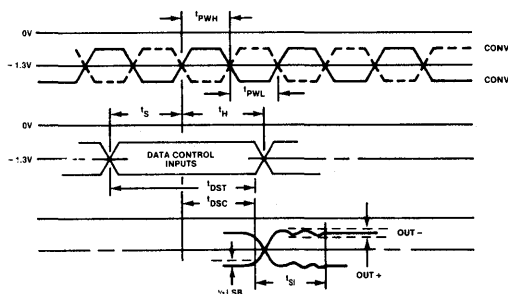
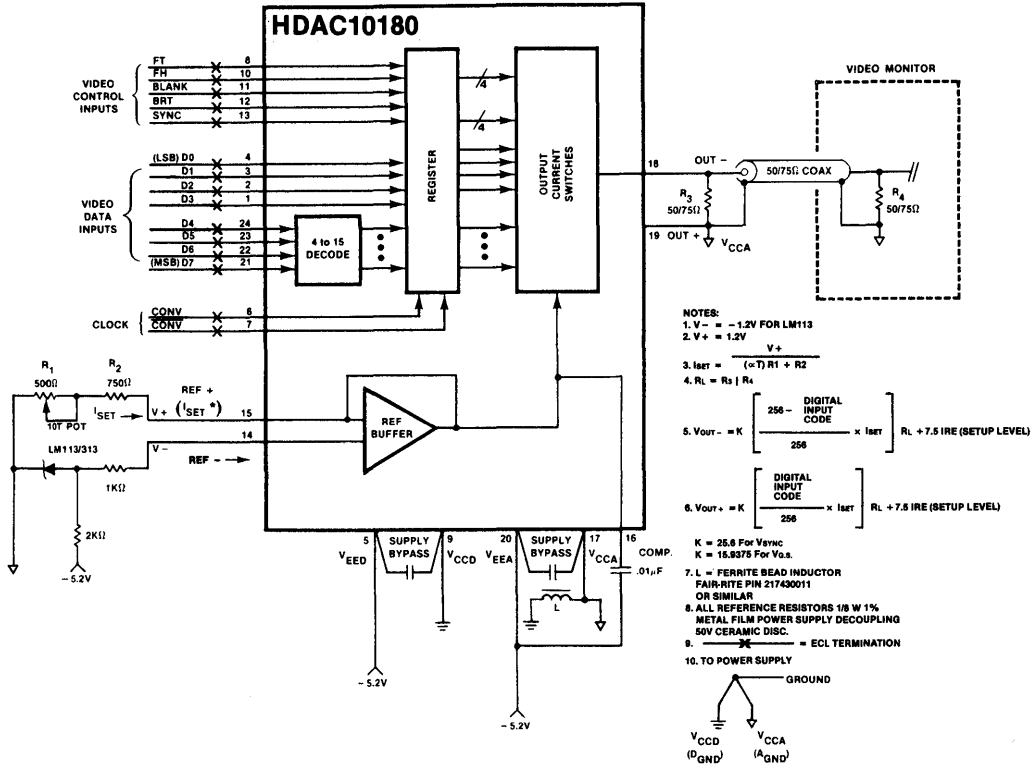


FIGURE 2 TYPICAL INTERFACE CIRCUIT



POWER CONSIDERATIONS

The HDAC10180 operates from a single standard - 5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10180 inherent supply noise rejection characteristics. As shown in Figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10180 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD} . The analog supply return is V_{CCA} . All power and ground pins must be connected in any application. If a + 5V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10180 has two reference inputs: REF - and REF +. Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy (see Figure 5).

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the REF + input on the HDAC10180. A method and equations to set I_{SET} is shown in Figure 2. The HDAC10180 uses an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF - pin should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than I_{SET} for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10180 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (C_c) should be connected between COMP and V_{EEA} as shown in Figure 2. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the C_c should be large ($.01\mu\text{F}$). The value of C_c determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of C_c can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10180 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10180 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 1).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table 1 shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 4).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10180. Since the actual switching threshold of $\overline{\text{CONV}}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of $\overline{\text{CONV}}$ is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10180 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 7, the output voltage is the product of the output current and load impedance and is between 0 and -1.07V . The OUT^- output (Figure 4) will provide a video output waveform with the SYNC pulse bottom at the -1.07V level. The OUT^+ is inverted with SYNC up.

Table 1 Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out – (mA)	Out – (V)	Out – (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

Table 2 The HDAC10180 family and speed designations.

Part Number	Update	Comments
HDAC10180A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10180B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

Figure 3: CONVert, $\overline{\text{CON}}\text{Vert}$ SWITCHING LEVELS

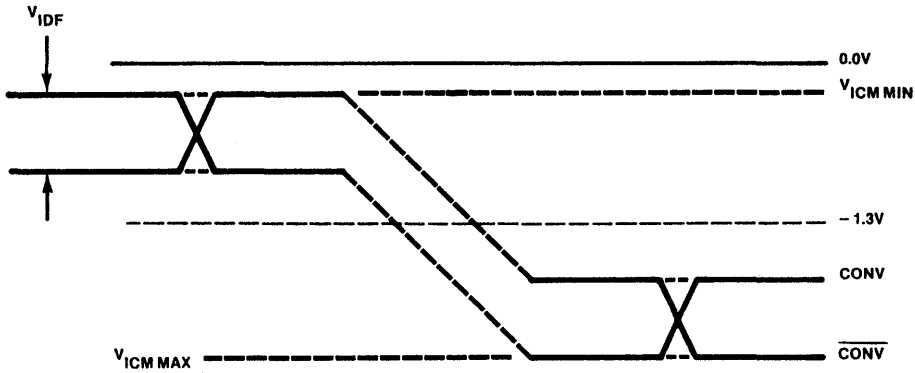


FIGURE 4 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD

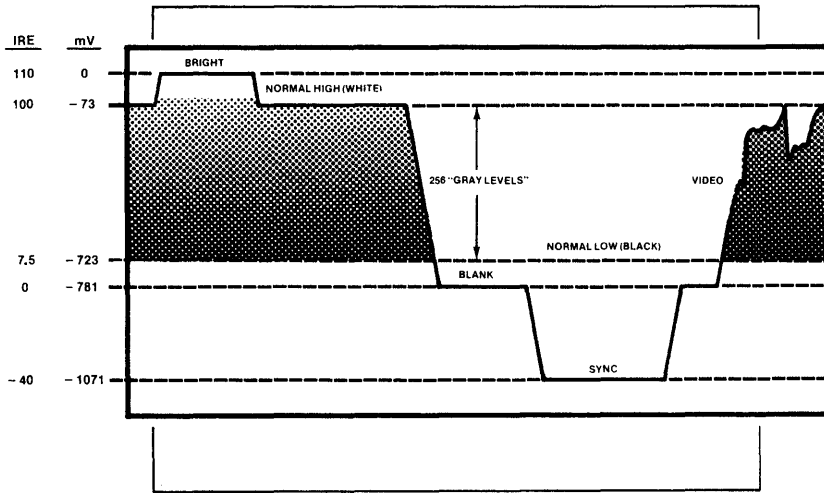


FIGURE 5 EQUIVALENT INPUT CIRCUITS—DATA, CLOCK, CONTROLS AND REFERENCE

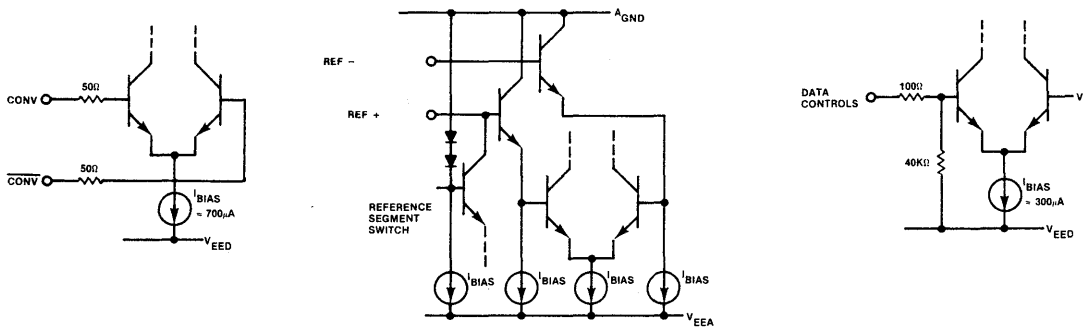


FIGURE 6 DAC OUTPUT CIRCUIT

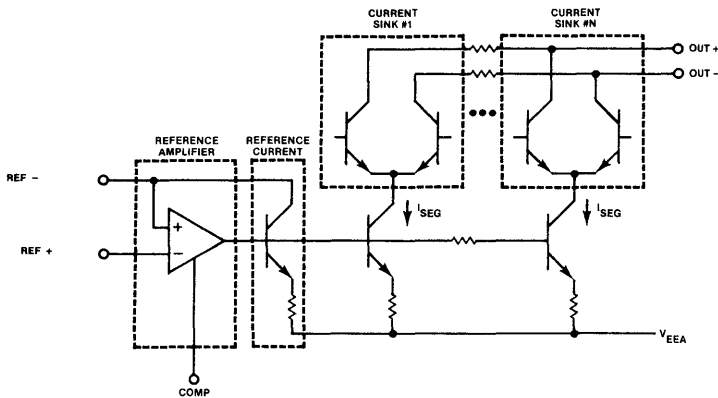


FIGURE 7A STANDARD LOAD

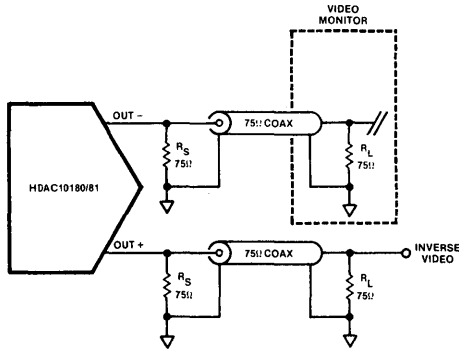
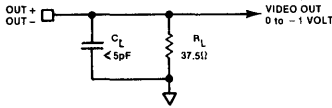


FIGURE 7B TEST LOAD



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision band-gap reference which completely eliminates the need for an external reference. The reference can supply up to 50μA to an external load, such as another DAC reference input. (See HDAC10181 Data Sheet)

The circuits shown in Figure 8 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which like the 10180, does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 is the best choice for new designs.

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

FIGURE 8 TYPICAL RGB GRAPHICS SYSTEM

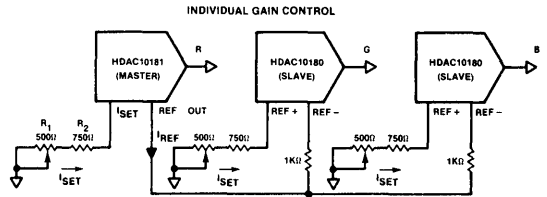
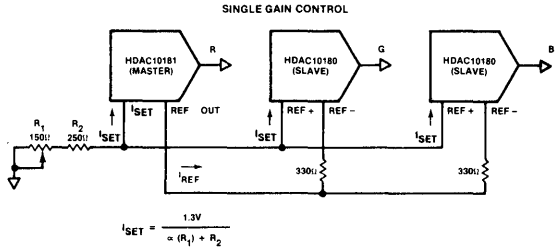
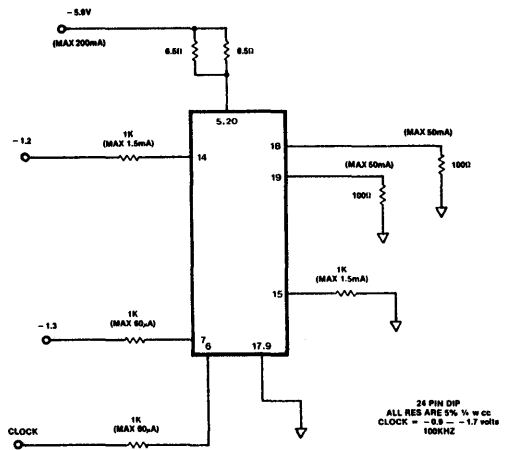
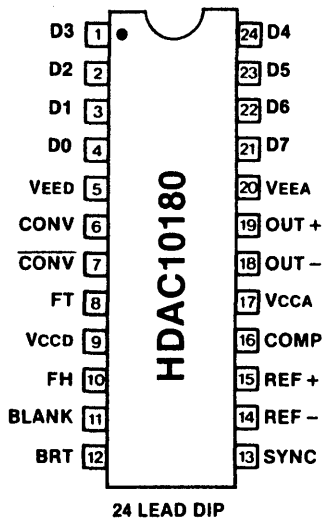


FIGURE 9 BURN-IN CIRCUIT



PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF -	Reference Current - Input
REF +	Reference Current + Input
COMP	Compensation Input
VCCA	Analog Positive Supply
OUT -	Output Current Negative
OUT +	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

***For Ordering Information See Section 1.*

NOTES:

8-BIT, HIGH SPEED D/A CONVERTERS

FEATURES

- **275 MWPS Conversion Rate - A Version**
- **165 MWPS Conversion Rate - B Version**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Stable On-chip Bandgap Reference
- Registered Data And Video Controls
- Differential Current Outputs

APPLICATIONS

- High Resolution Color or Monochrome Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

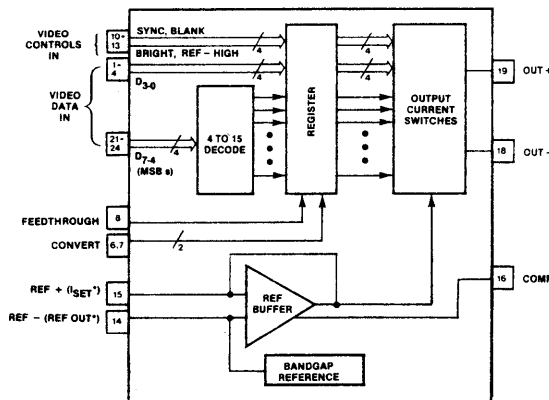
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GENERAL DESCRIPTION

The HDAC10181 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White, [Force High] Bright), the HDAC10181 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The HDAC10181 in-

cludes an internal precision bandgap reference which can drive two HDAC10180s in an RGB graphics system. The HDAC10181 contains data and control input registers, video control logic, reference, and current switches in 24 Lead CERDIP, or ceramic sidebraced DIP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which the useful life will be impaired)¹**Supply Voltages**

V_{EED} (measured to V_{CCD})	- 7.0 to 0.5V
V_{EEA} (measured to V_{CCA})	- 7.0 to 0.5V
V_{CCA} (measured to V_{CCD})	- 0.5 to 0.5V

Temperature

Operating, Ambient	- 60 to + 140°C
Junction	+ 175°C
Lead, Soldering (10 seconds)	+ 300°C
Storage	- 60 to + 150°C

Input Voltages

CONV, Data, and Controls V_{EED} to 0.5V
(measured to V_{CCD})

REF + (measured to V_{CCA})	V_{EEA} to 0.5V
REF - (measured to V_{CCA})	V_{EEA} to 0.5V

Notes:

1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
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DC ELECTRICAL CHARACTERISTICS $V_{CCA} = 0.0V$, $V_{EEA} = V_{EED} = -5.2V \pm 0.3V$, $T_A = 25^\circ C$, $C_C = 0pF$, $I_{SET} = 1.105 mA$

E_{LI}	Integral Linearity Error	$1.0mA < I_{SET} < 1.3mA$	I	-0.37 -0.95	+0.37 +0.95	% Full Scale LSB
E_{LD}	Differential Linearity Error	$1.0mA < I_{SET} < 1.3mA$	I	-0.2 - 1/2	+0.2 + 1/2	% Full Scale LSB
E_G	Gain Error	$T_A = 25^\circ C$ OVER TEMP RANGE	I	-15 -19	+15 +19	% Full Scale
TC_G	Gain Error Tempco		V	250		PPM/°C
C_{REF}	Input Capacitance, REF +, REF -		V	5		pF
V_{OCP}	Compliance Voltage, + Output		I	-1.2	1.5	V
V_{OCN}	Compliance Voltage, - Output		I	-1.2	1.5	V
R_{OUT}	Equivalent Output Resistance		I	20		K Ohm
C_{OUT}	Output Capacitance		V	12		pF
I_{OP}	Maximum Current, + Output		IV	45		mA
I_{ON}	Maximum Current, - Output		IV	45		mA
I_{OS}	Output Offset Current		I		1/2	LSB
V_{IH}	Input Voltage, Logic HIGH		I		-1.0	V
V_{IL}	Input Voltage, Logic LOW		I		-1.5	V
V_{ICM}	Convert Voltage, Common Mode Range		I	-0.5	-2.5	V
V_{IDF}	Convert Voltage, Differential		IV	0.4	1.2	V
I_{IL}	Input Current, Logic LOW, Data and Controls		I		120	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls		I	10	120	μA
I_{IC}	Input Current, Convert		I	2	60	μA

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
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DC ELECTRICAL CHARACTERISTICS $V_{CCA} = 0.0V$, $V_{EEA} = V_{EED} = -5.2V \pm 0.3V$, $T_A = 25^\circ C$, $C_C = 0pF$, $I_{SET} = 1.105 mA$

C_I	Input Capacitance, Data and Controls		V	3		pF
PSR	Power Supply Sensitivity		I	-120	+120	$\mu A/V$
I_{EE}	Supply Current		I	175	200	mA

DYNAMIC CHARACTERISTICS $R_L = 37.5 \text{ Ohms}$, $C_L = 5pF$, $T_A = 25^\circ C$, $I_{SET} = 1.105 mA$

F_S	Maximum Conversion Rate	B Grade A Grade	I I	165 275		MWPS	
t_{RI}	Rise Time	10% to 90% G.S.	I		1.6	ns	
t_{RI}	Rise Time	10% to 90% G.S. $R_L = 25 \text{ Ohms}$	V	1.0		ns	
t_{SI}	Current Settling Time, Clocked Mode	To 0.2%	V	7		ns	
t_{SI}	Current Settling Time, Clocked Mode	To 0.8%	V	5.5		ns	
t_{SI}	Current Settling Time, Clocked Mode	To 0.2% $R_L = 25\Omega$	V	4.5		ns	
t_{DSC}	Clock to Output Delay, Clocked Mode		I		4	ns	
t_{DST}	Data to Output Delay, Transparent Mode		I		6	ns	
t_{PWL}	Convert Pulse Width, LOW	B Grade A Grade	I I	3.0 1.8		ns	
	Glitch Energy	Area = $\frac{1}{2} VT$	V	10		pV-s	
t_{PWH}	Convert Pulse Width, HIGH	B Grade A Grade	I I	3.0 1.8		ns	
BW_{REF}	Reference Bandwidth, -3dB		V	1		MHz	
t_S	Set-up Time, Data and Controls		I	1.3	1.8	2	ns
t_H	Hold Time, Data and Controls		I	0.5	0		ns
SR	Slew Rate	20% to 80% G.S.	I	400		$V/\mu S$	
FT_C	Clock Feedthrough		I		-48	dB	

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

- I 100% production tested at the specified temperature.
- II 100% production tested at $T_a = 25^\circ\text{C}$, and sample tested at specified temperature.
- III QA sample tested only at specified temperatures
- IV Parameter is guaranteed (but not tested) by design and characterization data.
- V Parameter is a typical value for information purposes only.

APPLICATION INFORMATION

The HDAC10181 is a high speed video Digital-to-Analog converters capable of up to 275 MWPS conversion rates. This makes the devices suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates. In addition, the HDAC10181 includes an internal bandgap reference which may be used to drive other HDAC10180s if desired. (See HDAC10180 Data Sheet)

The HDAC10181 is separated into different conversion rate categories as shown in Table 2.

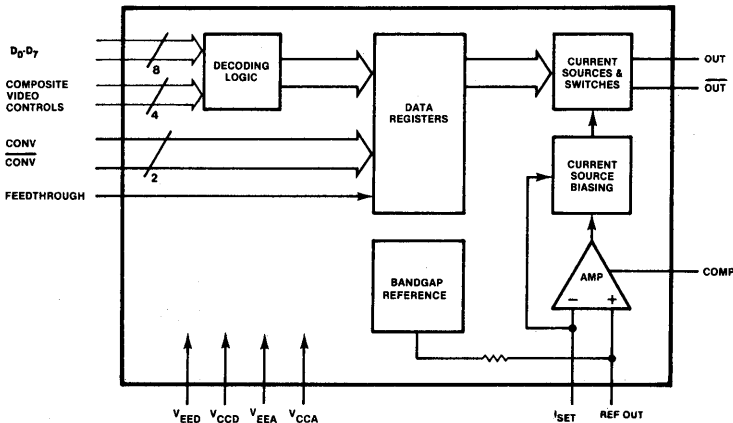
The HDAC10181 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The HDAC10181 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to

fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches. The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered "VIDEO DACs".

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the HDAC10181 in a color raster application is shown in Figure 2. The HDAC10181 requires few external components and is extremely easy to use. The very high operating speeds of the HDAC10181 requires good circuit layout, decoupling of supplies, and proper design of transmission lines. The following are several considerations that should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the HDAC10181. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a 330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC10181 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 Ohm load transmission system as shown. The source impedances of the HDAC10181 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_s and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_s .

FIGURE 1 TIMING DIAGRAM

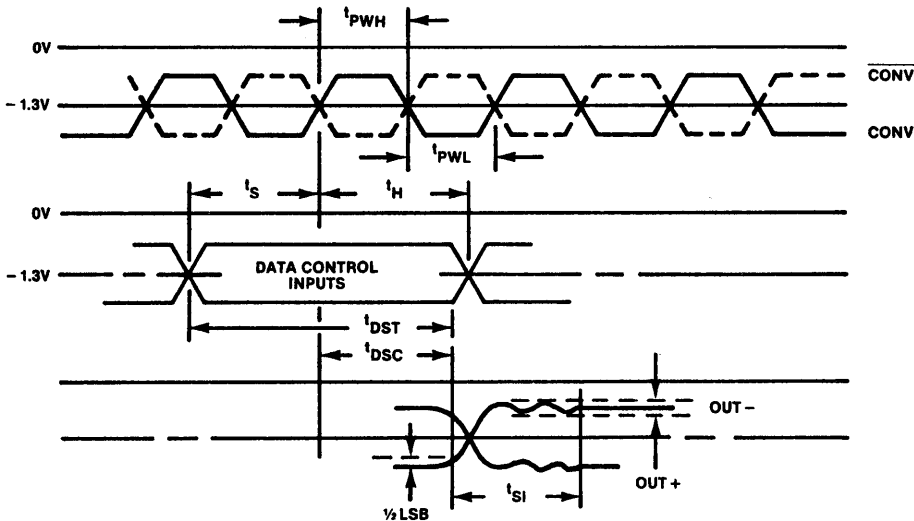
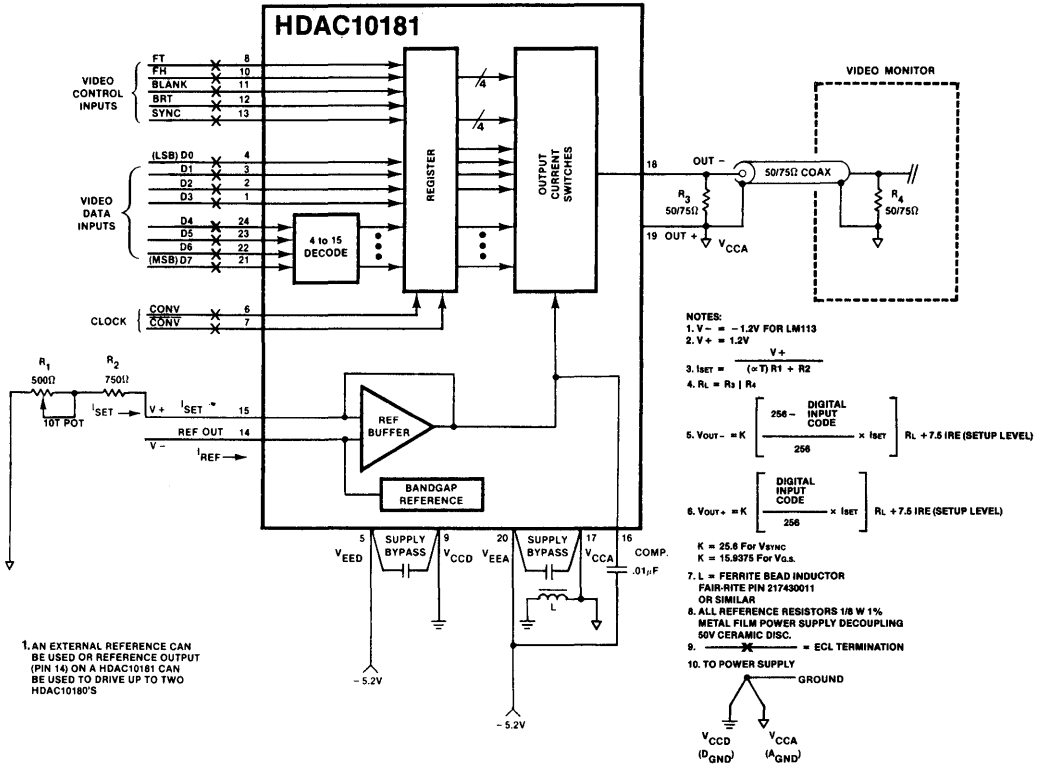


FIGURE 2 TYPICAL INTERFACE CIRCUIT



POWER CONSIDERATIONS

The HDAC10181 operates from a single standard - 5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC10181's inherent supply noise rejection characteristics. As shown in Figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC10181 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD} . The analog supply return is V_{CCA} . All power and ground pins must be connected in any application. If a + 5V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC10181 has one input (I_{SET}) and one reference output (REF OUT). Both pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier. The HDAC10181 has a bandgap reference connected internally to the inverting input of the buffer amplifier and the REF OUT.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy (see Figure 5).

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the I_{SET} input on the HDAC10181. A method and equations to set I_{SET} is shown in Figure 2. The HDAC10181 uses its own reference voltage for setting up I_{SET} as shown in Figure 2. The value for I_{SET} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased 50% more than I_{SET} for doubly terminated 75 Ohm video applications.

COMPENSATION

The HDAC10181 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor (Cc) should be connected between COMP and V_{EEA} as shown in Figure 2. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, the Cc should be large (.01 μ F). The value of Cc determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of Cc can be used to get up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The HDAC10181 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC10181 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 1).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table 1 shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 4).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC10181. Since the actual switching threshold of $\overline{\text{CONV}}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of $\overline{\text{CONV}}$ is set by this bias voltage.

ANALOG OUTPUTS

The HDAC10181 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{REF} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 7, the output voltage is the product of the output current and load impedance and is between 0 and $-1.07V$. The OUT $-$ output (Figure 4) will provide a video output waveform with the SYNC pulse bottom at the $-1.07V$ level. The OUT $+$ is inverted with SYNC up.

Table 1 Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

Table 2 The HDAC10181 family and speed designations.

Part Number	Update	Comments
HDAC10181A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
HDAC10181B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

FIGURE 3 CONVert, CONVert SWITCHING LEVELS

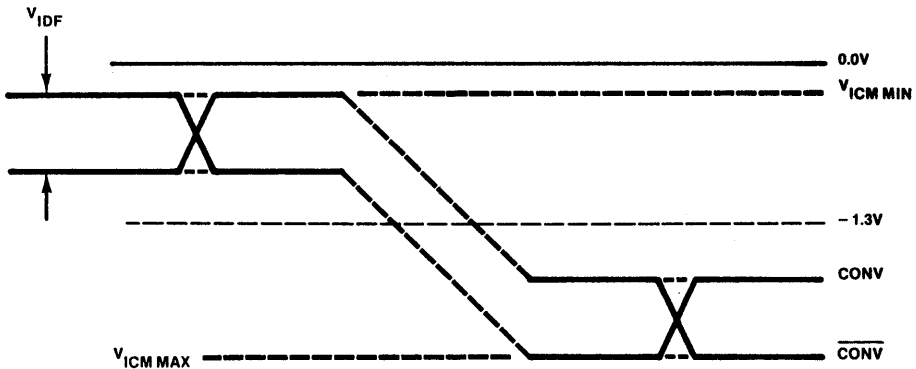


FIGURE 4 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD

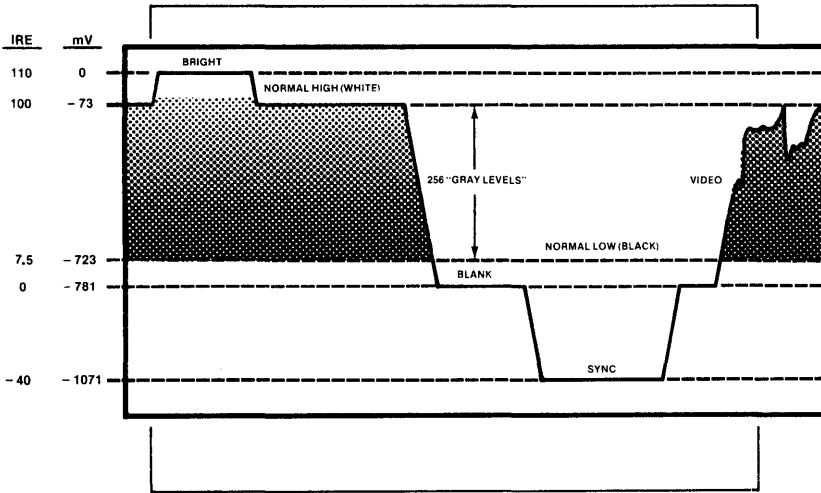


FIGURE 5 EQUIVALENT INPUT CIRCUITS—DATA, CLOCK, CONTROLS AND REFERENCE

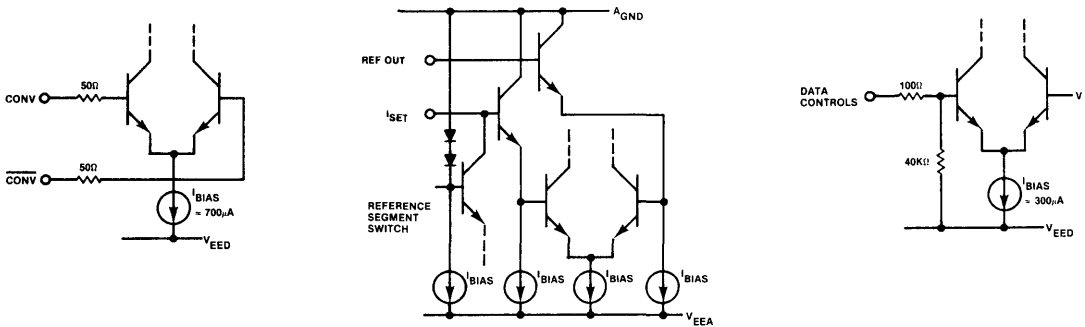


FIGURE 6 DAC OUTPUT CIRCUIT

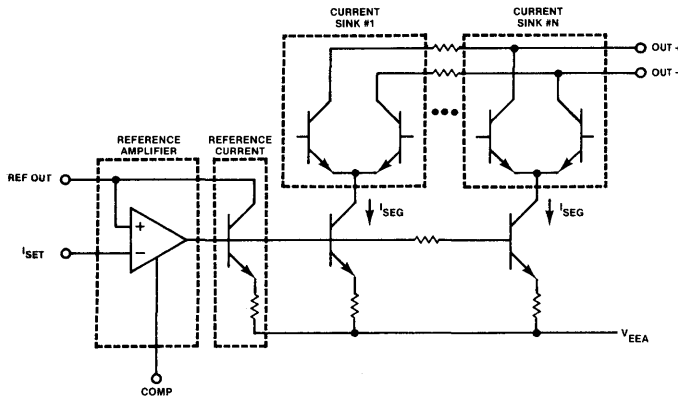


FIGURE 7A STANDARD LOAD

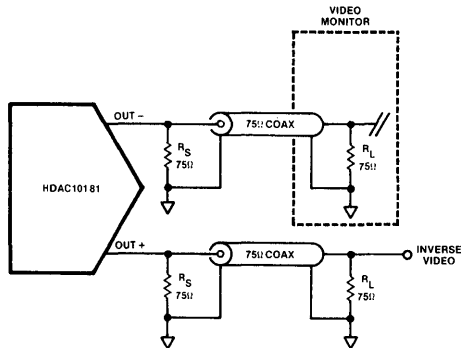
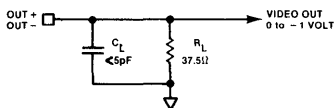


FIGURE 7B TEST LOAD



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC10181 contains an internal precision band-gap reference which completely eliminates the need for an external reference. The reference can supply up to 50µA to an external load, such as another DAC reference input.

The circuits shown in Figure 8 illustrate how a single HDAC10181 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC10181's reference output. The HDAC10180s shown are especially well-suited to be slaved to a 10181, since they are essentially 10181s without the reference. The 10180 is pin-compatible with the TDC1018, which like the 10180, does not have an internal reference. Although either the TDC1018 or HDAC10180 may be slaved from an HDAC10181, the higher performance HDAC10180 is the best choice for new designs. (See HDAC10180 Data Sheet)

No external reference is required for operation of the HDAC10181, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The HDAC10180 must use an external reference.

FIGURE 8 TYPICAL RGB GRAPHICS SYSTEM

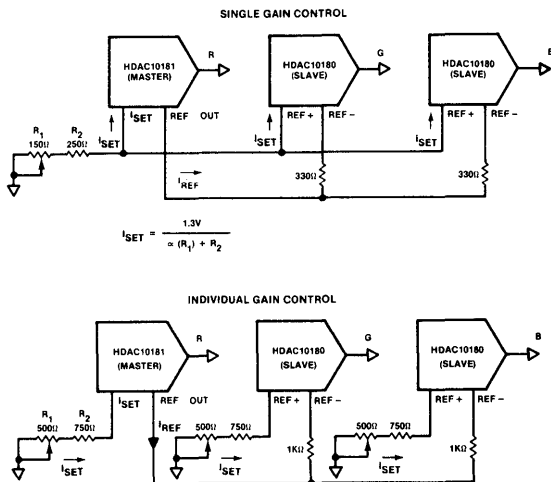
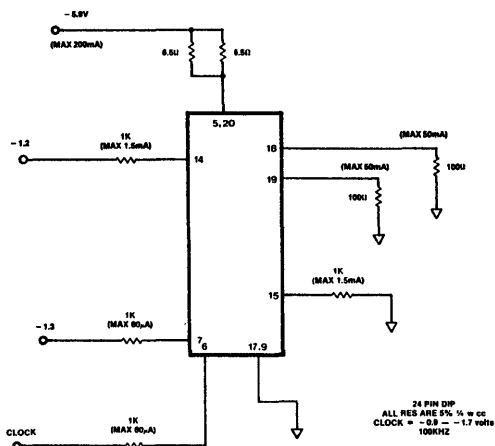
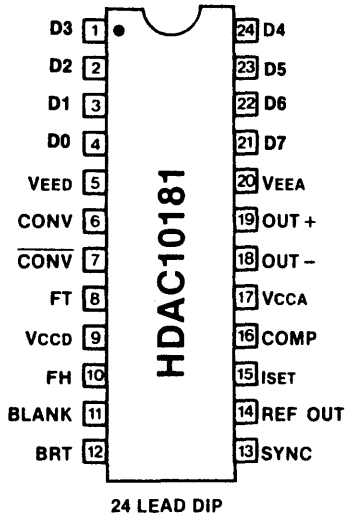


FIGURE 9 BURN-IN CIRCUIT



PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
$\overline{\text{CONV}}$	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF OUT	Reference Output
ISET	Reference Current + Input
COMP	Compensation Input
VCCA	Analog Positive Supply
OUT -	Output Current Negative
OUT +	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

***For Ordering Information See Section 1.*

NOTES:

8-BIT, ULTRA HIGH SPEED D/A CONVERTER

FEATURES

- **400 MWPS Nominal Conversion Rate**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Stable On-chip Bandgap Reference
- Registered Data And Video Controls
- Differential Current Outputs
- 50 and 75 Ohm Output Drive

APPLICATIONS

- **Raster Graphics**
- High Resolution Color or Monochrome Displays to 2K x 2K Pixels
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

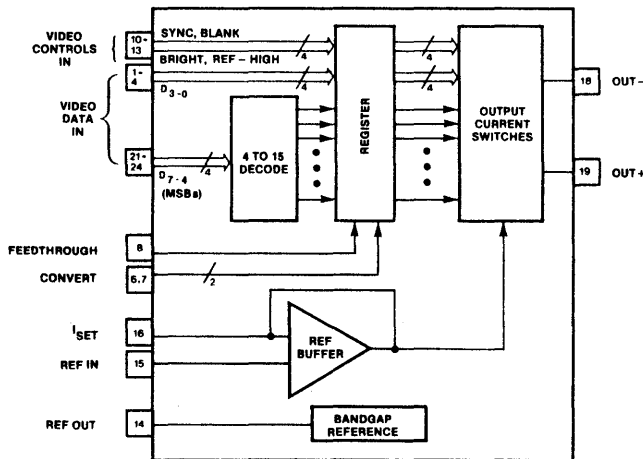
3

GENERAL DESCRIPTION

The HDAC51400 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at 400 MWPS. Complete with video controls (Sync, Blank, Reference White [Force High], Bright) the HDAC51400 directly drives doubly-terminated 50 or 75 Ohm loads to standard composite video levels. Standard set-up

level is 7.5 IRE. The HDAC51400 includes an internal precision bandgap reference which can drive two other 51400s in an RGB graphics system. The HDAC51400 contains data and control input registers, video control logic, reference, and current switches in 24 Lead CERDIP, or ceramic sidebraced DIP.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹20°C

Supply Voltages

V _{EED} (measured to V _{CCD})	- 7.0 to 0.5V
V _{EEA} (measured to V _{CCA})	- 7.0 to 0.5V
V _{CCA} (measured to V _{CCD})	- 0.5 to 0.5V

Temperature

Operating, Ambient	- 60 to + 140°C
Junction	+ 175°C
Lead, Soldering (10 seconds)	+ 300°C
Storage	- 60 to + 150°C

Input Voltages

CONV, Data, and Controls V_{EED} to 0.5V
(measured to V_{CCD})

REF + (measured to V _{CCA})	V _{EEA} to 0.5V
REF - (measured to V _{CCA})	V _{EEA} to 0.5V

Notes:

1. Operation at any Absolute Maximum Ratings is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
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DC ELECTRICAL CHARACTERISTICS

$$V_{CCA} = V_{CCD} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25^\circ C, I_{SET} = 1.105 mA$$

E _{LI}	Integral Linearity Error	1.0mA < I _{SET} < 1.8mA	I	-0.37 -0.95	+0.37 +0.95	% Full Scale LSB
E _{LD}	Differential Linearity Error	1.0mA < I _{SET} < 1.8mA	I	-0.2 - 1/2	+0.2 + 1/2	% Full Scale LSB
E _G	Gain Error		I	-5	+5	% Full Scale LSB
TC _G	Gain Error Tempco		IV	150		PPM/°C
TC _B	Bandgap Tempco		IV	100		PPM/°C
V _{REF-OUT}	Reference Voltage	(measured to V _{CCA})	IV	-1.2		V
I _{REF-OUT}	Reference Output Current		I	-50		μA
C _{REF}	Input Capacitance, I _{SET} , REF-IN		V	5		pF
V _{OCP}	Compliance Voltage, + Output		I	-1.2	1.5	V
V _{OCN}	Compliance Voltage, - Output		I	-1.2	1.5	V
R _{OUT}	Equivalent Output Resistance		I	20		K Ohm
C _{OUT}	Output Capacitance		V	9		pF
I _{OP}	Maximum Current, + Output		IV	45		mA
I _{ON}	Maximum Current, - Output		IV	45		mA
I _{OS}	Output Offset Current		I		1/2	LSB
V _{IH}	Input Voltage, Logic HIGH		I	-1.0		V

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL				UNITS
			MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS

$$V_{CCA} = V_{CCD} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25^\circ C, I_{SET} = 1.105 mA$$

V_{IL}	Input Voltage, Logic LOW	I			-1.5	V
V_{ICM}	Convert Voltage, Common Mode Range	I	-0.5		-2.5	V
V_{IDF}	Convert Voltage, Differential	IV	0.4		1.2	V
I_{IL}	Input Current, Logic LOW, Data and Controls	I			120	μA
I_{IH}	Input Current, Logic HIGH, Data and Controls	I		10	120	μA
I_{IC}	Input Current, Convert	I		2	60	μA
C_I	Input Capacitance, Data and Controls	V		3		pF
PSR	Power Supply Sensitivity	I	-120		+120	$\mu A/V$
I_{EE}	Supply Current	I		175	200	mA

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
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DYNAMIC CHARACTERISTICS

$$R_L = 37.5 \text{ Ohms}, C_L = 5pF \text{ (unless otherwise specified)}, T_A = 25^\circ C, I_{SET} = 1.105 mA$$

F_S	Maximum Conversion Rate		IV	385	400	MWPS
t_{RI}	Rise Time	10% to 90% G.S.	IV		900	ps
t_{RI}	Rise Time	10% to 90% G.S. $R_L = 25 \text{ Ohms Total}$	V		600	ps
t_{SI}	Current Settling Time, Clocked Mode	To 0.2% G.S.	IV	4		ns
t_{SI}	Current Settling Time, Clocked Mode	To 0.2% G.S. $R_L = 25 \text{ Ohms Total}$	IV	3		ns
t_{DSC}	Clock to Ouput Delay, Clocked Mode		I		4	ns
t_{DST}	Data to Output Delay, Transparent Mode		I		6	ns
t_{PWL}	Convert Pulse Width, LOW		IV	1.25		ns
t_{PWH}	Convert Pulse Width, HIGH		IV	1.25		ns
BW_{REF}	Reference Bandwidth, -3dB		V	1.25		MHz

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN TYP MAX			UNITS
			MIN	TYP	MAX	

DYNAMIC CHARACTERISTICS $R_L = 37.5 \text{ Ohms}$, $C_L = 5\text{pF}$ (unless otherwise specified), $T_A = 25^\circ\text{C}$, $I_{SET} = 1.105 \text{ mA}$

	Glitch Energy	Area = $\frac{1}{2} VT$	V	10		pV-s
t_S	Set-up Time, Data and Controls		I	1		ns
t_H	Hold Time, Data and Controls		I	0	-200	ps
SR	Slew Rate	20% to 80% G.S.	V	700		V/ μ S
FT_C	Clock Feedthrough		I		-48	dB

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

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TEST LEVEL TEST PROCEDURE

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APPLICATION INFORMATION

The HDAC51400 is a high speed video Digital-to-Analog converter capable of up to a 400 MWPS conversion rate. This makes the device suitable for driving 2048 X 2048 pixel displays at 60 to 90 Hz update rates. In addition, the HDAC51400 includes an internal band-gap reference which may be used to drive two other HDAC51400s if desired.

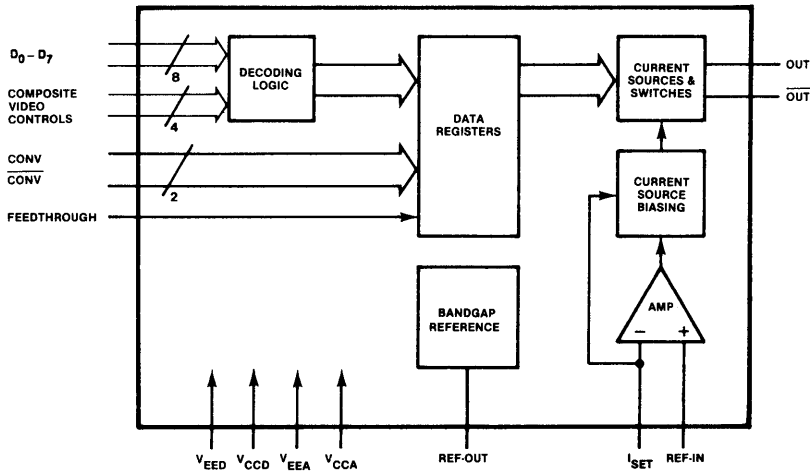
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The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation between the video control inputs and data. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered "VIDEO DACs".

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

GENERAL

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It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC51400 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a doubly terminated 50 or 75 Ohm transmission system as shown. The source impedances of the HDAC51400 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_s and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_s .

FIGURE 1 TIMING DIAGRAM

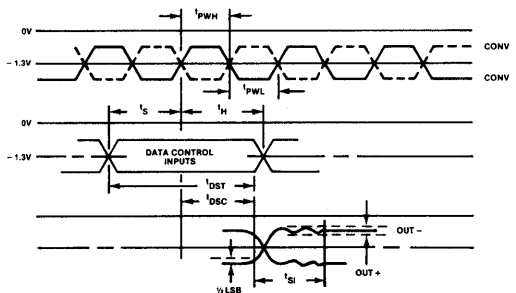
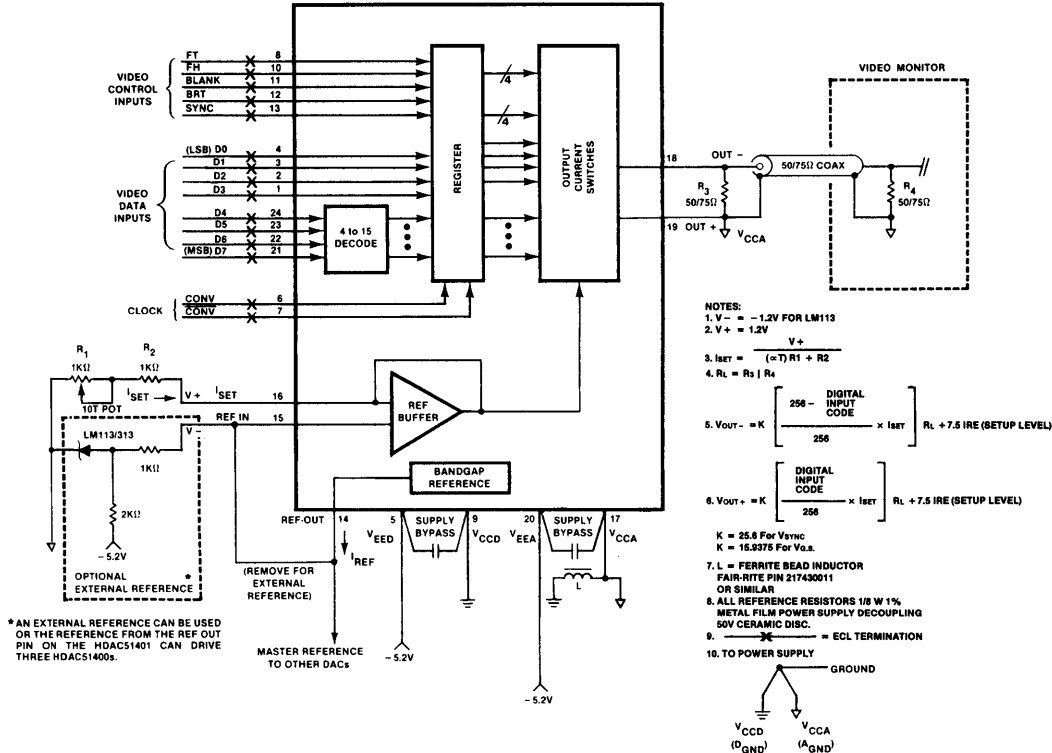


FIGURE 2 TYPICAL INTERFACE CIRCUIT



POWER CONSIDERATIONS

The HDAC51400 operates from a single standard -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC51400's inherent supply noise rejection characteristics. As shown in Figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The HDAC51400 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies can eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD} . The analog supply return is V_{CCA} . All power and ground pins must be connected in any application. If a +5V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The HDAC51400 has two reference inputs: REF IN and ISET and one reference output REF OUT. The input pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy (see Figure 5).

Since the analog output currents are proportional to the digital input data and the reference current (I_{SET}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the (I_{SET}) input on the HDAC51400. A method and equations to set I_{SET} is shown in Figure 2. The HDAC51400 can use an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the REF - IN pin should be driven through a resistor to minimize offsets caused by bias current. The value for I_{SET} can be varied with the 500 to 1K Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{SET} is increased by 50% above for doubly terminated 75 Ohm video applications.

DATA INPUTS AND VIDEO CONTROLS

The HDAC51400 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) minimizing glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than 8-bits are used.

The HDAC51400 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_s before, and a hold time of t_h after the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors (see Figure 1).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table 1 shows the video control effects on the analog output. Internal logic governs

Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 4).

Reference white video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and CONV (Figure 3). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the HDAC51400. Since the actual switching threshold of CONV is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to CONV. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The HDAC51400 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{SET} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 Ohm load to standard video levels. In the standard configuration of Figure 7, the output voltage is the product of the output current and load impedance and is between 0 and $-1.07V$. The OUT $-$ output (Figure 4) will provide a video output waveform with the SYNC pulse bottom at the $-1.07V$ level. The OUT $+$ is inverted with SYNC up.

Table 1 Video Control Operation

Sync	Blank	Ref White	Bright	Data Input	Out $-$ (mA)	Out $-$ (V)	Out $-$ (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

FIGURE 3 CONVert, $\overline{\text{CON}}\text{Vert}$ SWITCHING LEVELS

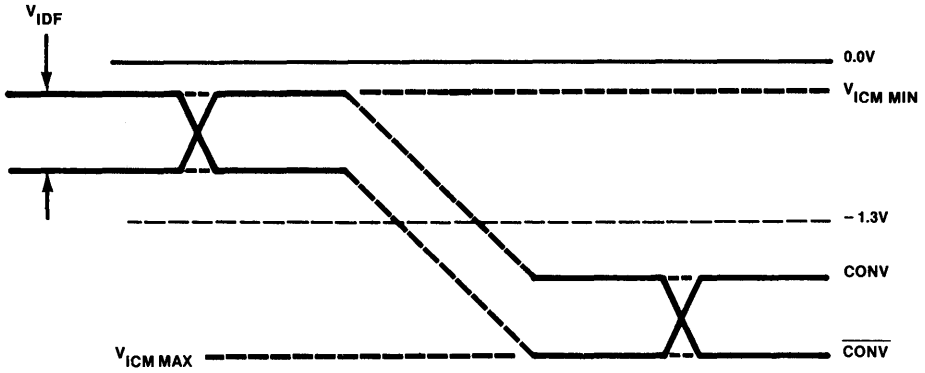


FIGURE 4 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD

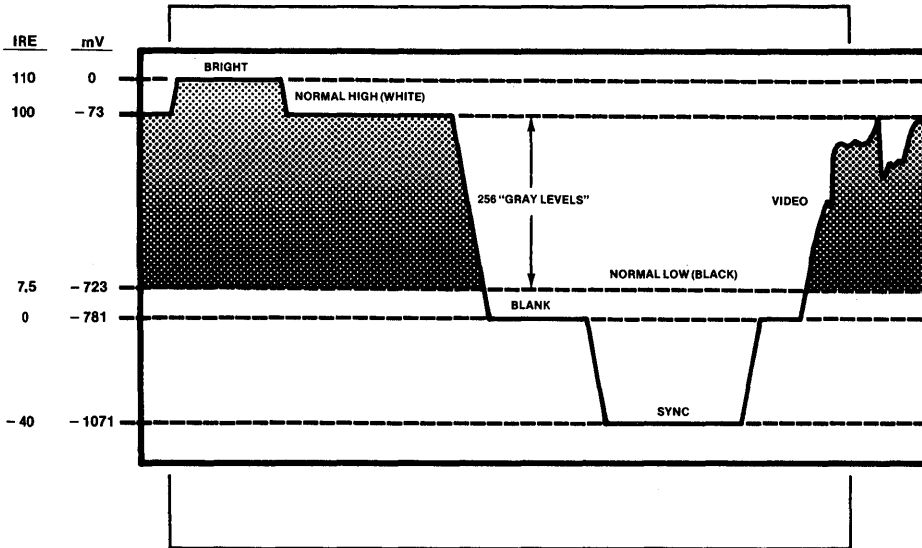


FIGURE 5 EQUIVALENT INPUT CIRCUITS—DATA, CLOCK, CONTROLS AND REFERENCE

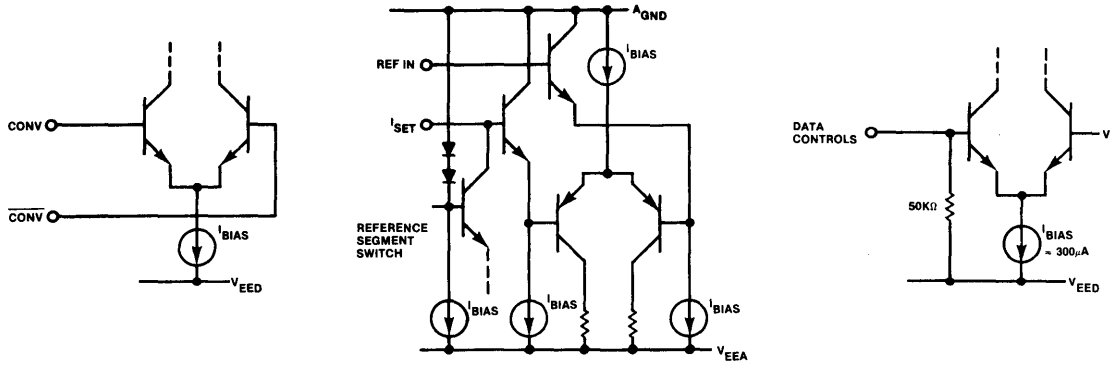


FIGURE 6 DAC OUTPUT CIRCUIT

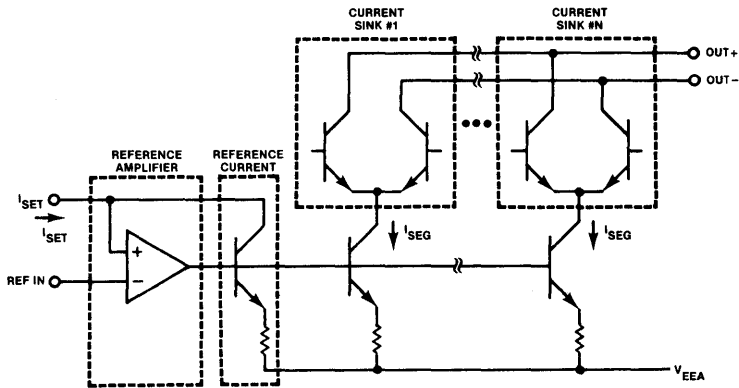


FIGURE 7A STANDARD LOAD

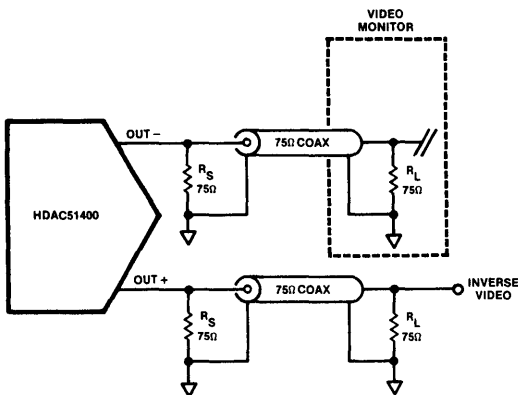


FIGURE 7B TEST LOAD

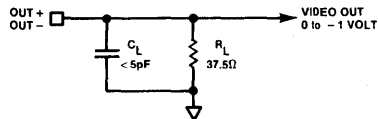
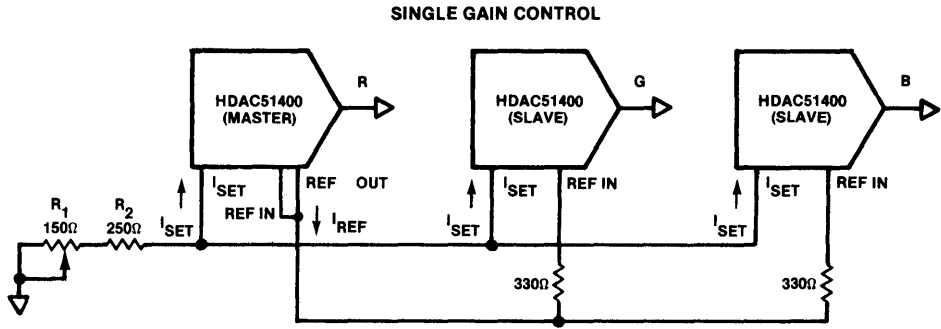
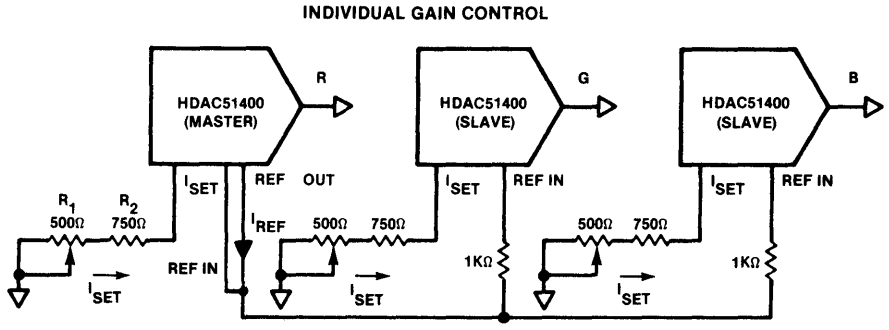


FIGURE 8 TYPICAL RGB GRAPHICS SYSTEM



$$I_{REF} = \frac{1.2V}{\alpha (R_1) + R_2}$$



TYPICAL RGB GRAPHICS SYSTEM

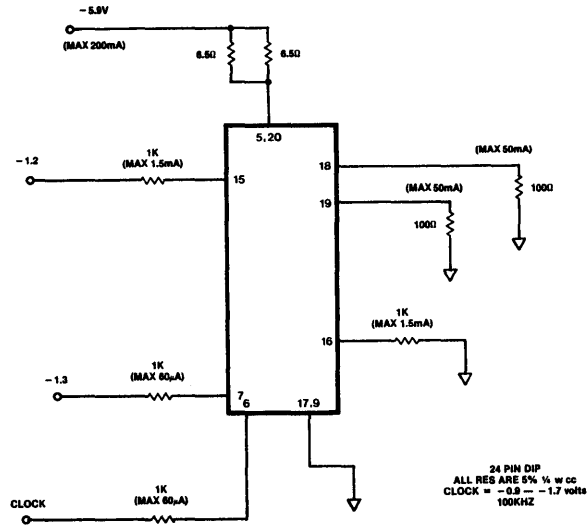
In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch. This may also eliminate the need for individual calibration of each DAC during production assembly.

The HDAC51400 contains an internal precision band-gap reference which completely eliminates the need for an external reference. The reference can supply up to 50µA to an external load. This can accommodate three DAC reference inputs.

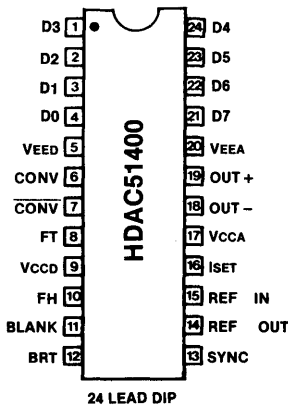
The circuits shown in Figure 8 illustrate how a single HDAC51400 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the HDAC51400's reference output.

FIGURE 9 BURN-IN CIRCUIT



PIN ASSIGNMENTS

PIN FUNCTIONS HDAC51400



NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF OUT	Reference Output
REF IN	Reference Input
ISET	Reference Current
VCCA	Analog Positive Supply
OUT -	Output Current Negative
OUT +	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

**For Ordering Information See Section 1.

NOTES:

HIGH SPEED 16-BIT DAC PRELIMINARY INFORMATION

FEATURES:

- Fast Settling Time - 150 nsec
- Excellent Linearity T. C. - 1 ppm/°C
- On-Chip Band-Gap Voltage Reference
- On-Chip Application Resistors for Gain Selection
- TTL Compatible Inputs

APPLICATIONS:

- High Speed Analog-to-Digital Converters
- Automatic Test Equipment
- Digital Attenuators
- Digital Communication Equipment
- Waveform Generators

GENERAL DESCRIPTION

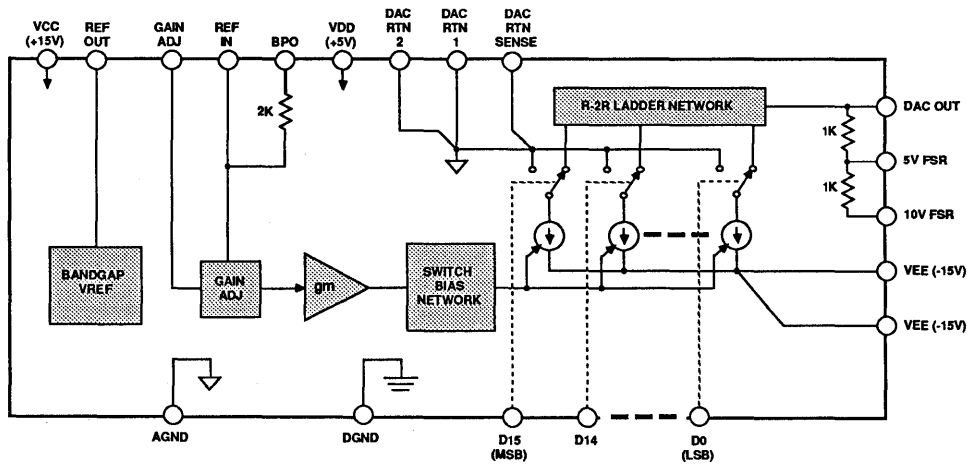
The HDAC52160 is a monolithic, high-performance, 16-bit digital-to-analog converter with unmatched stability and accuracy. With it's 150 nano-second settling time it is the highest speed 16-bit DAC in the industry. Unique features include the band-gap voltage reference and precision application resistors which greatly simplify device application. Unlike other high speed DAC's, the HDAC52160 can be used in either a current-output or voltage-output mode.

The internal application resistors support output range selections of +10 to 0, +5 to 0, +5 to -5, and +2.5 to -2.5 volts. These internal resistors, used in conjunction with an

external op amp, provide current-to-voltage conversion. Because of the high compliance voltage of the DAC output (± 2.5 volts), the HDAC52160 can also provide a direct voltage drive into a high impedance load without an external op amp.

The HDAC52160 operates with ± 15 volt analog supplies, a separate +5V digital supply and separate analog and digital grounds to provide maximum noise immunity. All logic input levels are TTL and 5 volt CMOS compatible. Laser-trimmed thin film technology ensures accuracy over time and environmental changes.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond Which Damage May Occur) 25°C (1)

Supply Voltages

VCC to AGND	+18 V
VEE to AGND	- 18 V
VDD to DGND	+6 V
AGND to DGND Differential	+ 0.5 V

Temperature

Temperature, case	-60 to + 140°C
junction	+ 150°C
Lead Temperature (soldering 10 seconds) ..	+ 300°C
Storage Temperature	-65 to + 150°C

Input Voltages

All Digital Inputs to DGND.....	-0.3 V to (VDD + 0.3 V)
REF IN to AGND	0 to +10 V

NOTE 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltages

VCC	+14.25 to +15.75 V
VEE	- 14.25 to -15.75 V
VDD	+4.75 to +5.25 V

Temperature

Temperature, Ambient (1)	-25 to +85°C
--------------------------------	--------------

NOTE1: Minimum air flow 50 LFPM.

ELECTRICAL SPECIFICATIONS

T_A=25°C, VCC = 15V, VDD = 5V, unless otherwise specified.

Parameter	Test Conditions	Test Level (1)	HDAC52160B			HDAC52160C			Units
			Min	Typ	Max	Min	Typ	Max	

ACCURACY SPECIFICATIONS

Integral Linearity Error		I	±0015	±003	±0023	±0045	%FSR
Integral Linearity Drift		I	±1	±2	±1	±2	PPM/°C
Differential Linearity Error		I	±003	±006	±003	±006	%FSR
Differential Linearity Drift		I	±1	±2	±1	±2	PPM/°C
Gain Error		I	±0.2	±0.3	±0.2	±0.3	%FSR
Gain Error Drift		I	±20	±40	±20	±40	PPM/°C
Zero Offset Error		I	±0.1	±0.2	±0.1	±0.2	%FSR
Zero Offset Error Drift		I	±10	±15	±10	±15	PPM/°C
Bipolar Offset Error		I	±10	±15	±10	±15	mV

DAC OUTPUT SPECIFICATIONS

I _{out}		V	5	5	mA
R _{out}		V	1K ±200	1K ±200	Ω
C _{out}	See Fig. 1	V	12	12	pF
Output Compliance (2)		V	±2.5	±2.5	V
Output Noise	BW = 1MHz	V	40	40	μV RMS

DYNAMIC SPECIFICATIONS

Settling Time	to .0015%	V	150	150	ns
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Parameter	Test Conditions	Test Level (1)	HDAC52160B			HDAC52160C			Units
			Min	Typ	Max	Min	Typ	Max	
LOGIC SPECIFICATIONS									
VIH(3)		I	3.75			3.75			V
VIL(4)		I			1.5			1.5	V
I _{IH}		I		5	16		5	16	μA
I _{IL}		I		1	5		1	5	μA

REFERENCE									
Reference Output Voltage		I	4.99	5	5.01	4.99	5	5.01	V
Reference Voltage Drift		I		25	±35		25	±35	PPM/°C
Max. Reference Output Load	Total Current(5)	IV		8			8		mA
Output Noise (6)	BW=1MHz	V		40			40		μV RMS

POWER SUPPLIES									
VCC Supply Current	VCC=+15V	I		4	6		4	6	mA
VEE Supply Current	VEE=-15V	I		24	35		24	35	mA
VDD Supply Current	VDD=+5V	I		6	9		6	9	mA
Power Dissipation		I		450	660		450	660	mW
PSRR, VCC	VCC=15V±5%	V		.005			.005		%G/%Ps
PSRR, VEE	VEE=-15V±5%	V		.030			.030		%G/%Ps
PSRR, VDD	VDD=5V±5%	V		.001			.001		%G/%Ps

NOTES:

(1) ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicate that the specification is not tested at the specified condition.

Unless otherwise noted, all tests performed after a 10 min. power soak.

TEST LEVEL

TEST PROCEDURE

I	100% production tested at the specified temperature.
II	100% production tested at Ta=25°C, and sample tested at the specified temperature.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

(2) Accuracy is not guaranteed beyond this limit.

(3) Accuracy is not guaranteed below this limit.

(4) Accuracy is not guaranteed above this limit.

(5) Reference Load:

REF IN = 1mA
BPO = 2.5mA

(6) Reference decoupled as shown in Figure 6.

TERMINOLOGY

Integral Linearity Error

Integral linearity error is a measure of the maximum deviation from a straight line passing through the end points of the DAC transfer function. It is measured after adjusting for zero offset error and gain error.

Differential Linearity Error

Differential linearity error is the difference between the measured change and the ideal 1 LSB change between two adjacent codes. A specified differential nonlinearity of <1 LSB ensures monotonicity.

Gain Error

Gain error, also known as full-scale error, is the deviation of the actual DAC full-scale output from the ideal full-scale output. For the HDAC52160, ideal full-scale output is $[(65,535/65,536) \cdot 5\text{mA} + \text{Offset Error}]$. Gain error and offset errors are adjustable to zero using the external trim networks shown in Figures 5 and 4, respectively.

Output Compliance

Output compliance is the allowable range of voltage swing for pin DAC OUT. Beyond the specified output compliance other specifications, such as integral nonlinearity, are not guaranteed.

GENERAL CIRCUIT DESCRIPTION

The HDAC52160 uses a unique design approach to set a new standard in monolithic DAC performance. It delivers exceptional 16-bit accuracy and stability over temperature and, at the same time, exhibits an extremely fast 150 ns settling time. On chip support functions include a stable band-gap voltage reference and the appropriate application resistors for output scaling. Inclusion of these functions both reduces the external analog component requirements and further increases accuracy. Digital circuitry on the chip is kept to a minimum (limited to the digital inputs) thus minimizing internal noise generation and providing interface flexibility.

DAC Circuitry

The HDAC52160 DAC uses an R-2R ladder for the least significant bits. This ladder, which consists of a resistor network, successively divides the (remaining) reference current to produce a binary weighted current division. In other words, in moving down the ladder, each 2R resistor leg has half the current flow of the previous leg. Each 2R resistor leg is connected to a current source that is

trimmed during manufacturing to provide the 16-bit accuracy. Bipolar switches within each leg are controlled by the respective data bit (pins D0 through D15). When the controlling data bit is low, the 2R resistor leg current is steered to pin DAC OUT. When the data bit is high, the leg current is steered to the DAC RTN pins (DAC RTN SENSE, DAC RTN 1, and DAC RTN 2), which are connected to analog ground.

Figure 1 illustrates the equivalent output circuit of the HDAC52160 showing on-chip application resistors and parasitic capacitances.

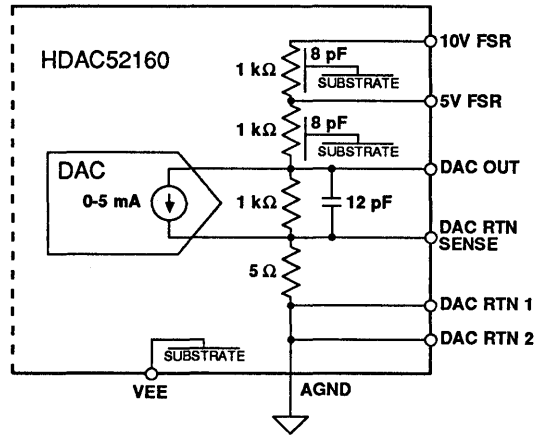


FIGURE 1. Equivalent HDAC52160 Output Circuit

APPLICATION INFORMATION

ACTIVE CURRENT - TO VOLTAGE CONVERSION

In many DAC applications, the output current needs to be converted into a usable voltage signal. The most common current-to-voltage configuration for the HDAC52160 output is shown in Figure 2. Here, an external op amp in conjunction with the internal feedback resistor(s) is used for current-to-voltage (I-to-V) conversion. The op amp both provides a buffered Vout and maintains DAC OUT at virtual ground. This way, Vout can provide up to a 10 volt output swing (using internal feedback resistors) and the Output Compliance specification (± 2.5 volts maximum) is met.

Vout swing is determined by the feedback resistance. For a 5 volt Vout swing, the op amp's output is connected to pin 5V FSR ("Full Scale Range") which

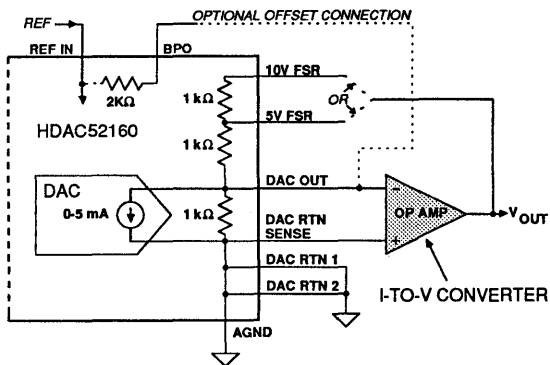


FIGURE 2. Connection of External OP AMP for Active Current-to-Voltage Conversion

provides 1 kΩ feedback resistance. A 10 volt Vout swing is derived by connecting the op amp output to pin 10V FSR. This feedback connection option is illustrated by the dotted line in Figure 2. Properly trimmed as discussed later, the connections of Figure 2, as indicated, would result in the ideal output values as listed in Table I.

To configure the bipolar output range as indicated in Table I, the BPO pin is connected to DAC OUT. This

INPUT CODE	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
1111 1111 1111 1111	0	0	-2.50 V	-5.00 V
1111 1111 1111 1110	+ 76.3 μV	+ 152.6 μV	-2.499924 V	-4.999846 V
0111 1111 1111 1111	+2.500 V	+5.00 V	0.00 V	0.00 V
0000 0000 0000 0000	+4.999924 V	+9.999846 V	+2.499924 V	+4.999846 V

TABLE 1. Normalized voltage values for programmable Output Ranges. (Using Figure 6)

connection option is illustrated by the dashed line Figure 2; this offsets the output range by half of the full scale range, so that a half-scale digital input value results in a output current value of zero.

The pin connections for the active I-to-V ranges supported by the internal application resistors are summarized in Table II.

Operational Amplifier Selection

Selection of the external op amp involves understanding the final system performance requirements in terms of

DEVICE PINS	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
BPO	NOT CONNECTED	NOT CONNECTED	CONNECTED TO DAC OUT	CONNECTED TO DAC OUT
5V FSR	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED
10V FSR	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT	NOT CONNECTED	CONNECTED TO OP AMP OUTPUT

TABLE 2. Device Pin Connection Summary for Output Range Programming (Active I-to-V Conversion Only)

both speed and accuracy. To maintain the 16-bit, ±1/2 LSB accuracy provided by DAC OUT at Vout shown in Figure 2, the op amp open loop gain (A_{vol}) must be 96 dB minimum. Any gain lower than this will contribute an error in the I-to-V conversion circuit. To maintain the 150 ns settling time capability provided by DAC OUT at Vout, the op amp must have a minimum gain bandwidth of 50 MHz and settling time of less than 100 ns to 0.0015% of full scale.

Non-Standard Output Ranges

By connecting an external resistance in series or parallel with the internal feedback resistances, it is possible to customize the voltage output range at Vout. The output range offset similarly can be customized. If these modifications are attempted, however, several cautions are in order. First, the internal resistors (used for feedback, offset, etc.) are trimmed for relative accuracy and not absolute accuracy which can vary ±20%. Since 16-bit accuracy requires matching to within 0.00075%, it is difficult to attain this precision over the wide trim range required. Second, since the internal resistors are integrated on the same monolithic chip, they will temperature track each other but not necessarily an external resistor. The temperature coefficient of these internal thin-film resistors is very low, so optimum performance is achieved by using an external resistor with a low temperature coefficient.

PASSIVE CURRENT-TO-VOLTAGE CONVERSION

Because of the HDAC52160's high voltage compliance, a voltage output can be derived directly at DAC OUT in a method suitable for some applications. By driving a load resistor directly with the current from DAC OUT, a voltage drop results producing Vout. An example of this implementation is shown in Figure 3, where an internal feedback resistor is used as the load (10V FSR is grounded to optimize settling time). By utilizing all internal resistors, this circuit offers optimized stability and matching.

Output current from the DAC ranges between 0 and 5 mA, which corresponds to an input code of all 1's and all 0's, respectively. The net 500 Ω load of Figure 3 results in a -2.5 to 0 volt output range which stays within the specified output compliance limit. An external load resistor could also be used with this circuit, however there are difficulties with this arrangement; thermal tracking is not optimum, and the gain adjustment required to overcome the absolute internal resistance and DAC output current errors is beyond the correction range provided by the trim circuit, which is described later.

Note that the input resistance of the circuit driven by V_{out} will be placed in parallel with the load resistor. This hence limits the application of Figure 3 to high impedance loads. Also note that if a buffer (or other active circuit) is used at V_{out} in Figure 3, that circuit's CMRR must be at least 100 dB to maintain the DAC's accuracy. This is an advantage of the active current-to-voltage configuration shown in Figure 2, where the input of the op amp is always at virtual ground.

OUTPUT OFFSET COMPENSATION

Although the zero offset error of the HDAC52160 is pre-trimmed to within ±0.2% of the full scale range, some

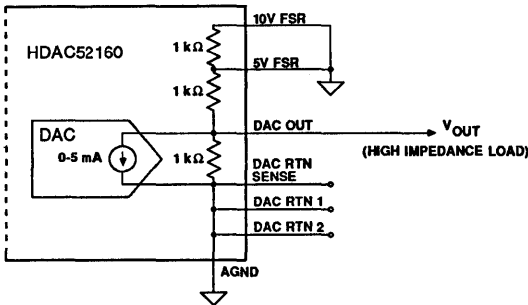


FIGURE 3. Connection of Internal Load Resistors for Passive Current-to-Voltage Conversion

applications require better accuracy. The offset trim network of Figure 4, shown connected to DAC OUT, will allow offset adjustment in excess of ±0.2 %. This trim network can be used for the active I-to-V conversion network of Figure 2 or the passive circuit of Figure 3. When using an external op amp as in Figure 3, optimum offset stability may be achieved by using the nulling network recommended by the op amp's manufacturer.

Although accuracy of the offset network components is not important, temperature tracking of the resistor and potentiometer values will affect offset trim stability. The resistors and potentiometer should have a low temperature coefficient and the potentiometer should be a high quality, multi-turn component to ensure minute adjustability and stability over time and temperature. The 0.1 μF capacitors shown (typically ceramic) are used to decouple power supply noise from the DAC output circuit.

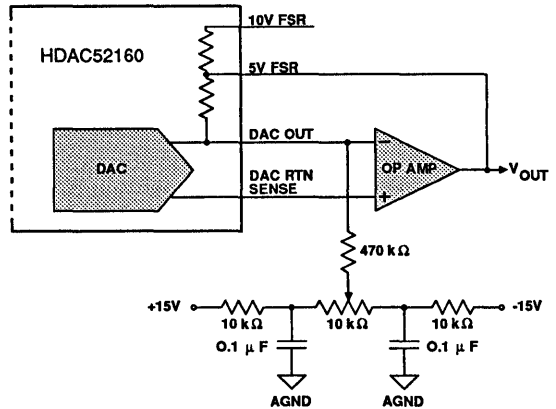


FIGURE 4. Offset Compensation Network Useful for All Output Configurations

LOGIC INTERFACE

Because of the low logic input current specification, most TTL families will adequately drive the HDAC52160, even though minimum V_{IH} is specified at 3.75 volts, a figure relatively high by TTL standards. Non-adherence to the V_{IH} spec can result in a less than specified DAC accuracy. High-Speed CMOS logic (HC) or High-Speed CMOS logic with TTL compatible inputs (HCT) are directly compatible with the HDAC52160 logic inputs.

GAIN ADJUSTMENT

With the gain error of the HDAC52160 pre-trimmed to within ±0.3% of full scale accuracy, many applications require external gain adjustments. Configuration of the external gain adjustment network is shown in Figure 5. The adjustment potentiometer is connected between two low-noise voltage sources, REF OUT and AGND, as shown. The two bypass capacitors shown further help to eliminate noise. Because of the voltage source

asymmetry in relationship to the potentiometer wiper, the adjustment range is an asymmetric -0.6% to +1%. This adjustment range does sufficiently compensate for the error of the device, and the network will work for any type of output configuration. The adjustment range can be made larger and symmetrical by using a circuit similar to the offset compensation network as shown in Figure 4, but with the consequence of introducing power supply noise (and power supply variations) into the vital voltage reference circuit.

The selection criteria for the gain adjustment network components is similar to those described for the offset compensation network; accuracy is not important, but temperature stability is.

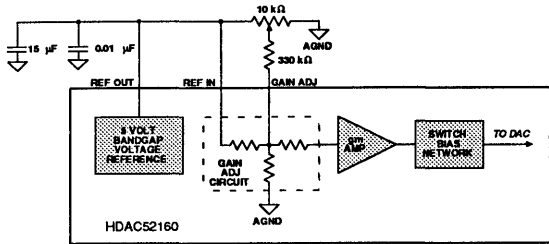


FIGURE 5. Gain Trim Network Suitable For All Output Configurations

CIRCUIT LAYOUT CONSIDERATIONS

In any analog system design, care must be taken in the circuit layout process. The design of a high-speed, 16-bit analog system offers an exceptional challenge. The integrity of the system's power supply and grounding is critical, and as with any precision analog components, good decoupling is needed directly at the device. Analog signal traces must be routed in a manner to minimize coupling from potential noise sources. With a 5 volt full-scale output voltage range, a mere 38 μVpp noise level is equivalent to 1/2 LSB. Low amplitude noise such as this is virtually impossible to eliminate without totally shielding the analog circuit portion.

The power supply must be a well-regulated, noise-free analog voltage source. As with any analog device, the PSRR performance of the HDAC52160 degrades with higher frequency components. Logic noise in the supply or ground line contains high frequency components, so separate supplies and ground returns are recommended for the analog and logic portions of the system. Radiated noise from digital signal traces and power supply traces must also be avoided. Completely shield the analog circuit portion from digital circuitry and digital power supplies and ground. A separate analog ground plane near the device should be used to shield the digital data lines going into the device; this plane should have a trace that completely surrounds the digital

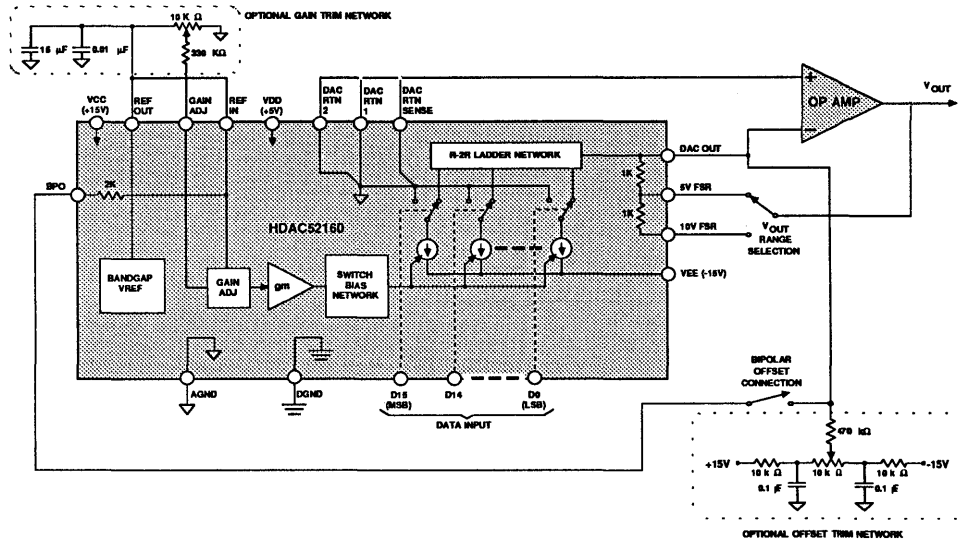


FIGURE 6. Typical HDAC52160 Application Circuit

inputs, if possible. If an analog ground plane is used with the device for shielding, keep the space between the digital guard plane and analog ground plane wide to prevent capacitive coupling. The best analog ground plane is one with the least resistance, i.e., the minimum total "squares" of surface area, regardless of size. All device grounding should be to the analog ground plane, except for the GND RTN pins which should be tied to the plane at one connection point only.

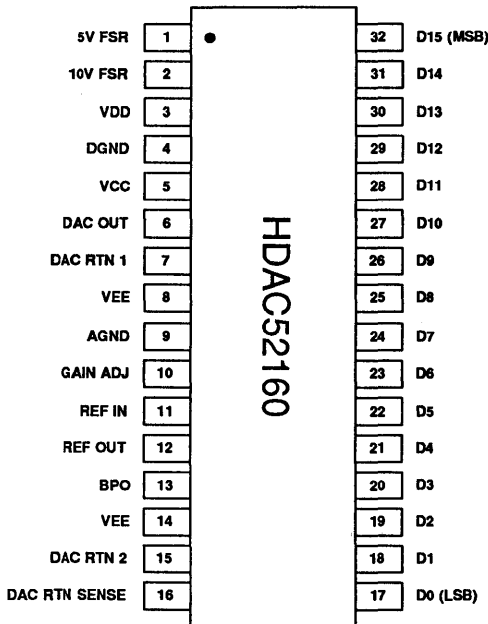
Figures 5 and 6 show the implementation of decoupling devices (0.01µF and 15µF in parallel) at pin REF OUT. These devices should be connected to the analog ground and their incorporation will minimize the overall A/D conversion noise.

Since virtually all the interfacing to the HDAC52160 is analog in nature (the logic inputs are actually analog

current switches), DGND and AGND should be tied together and treated as an analog ground. This analog ground and the systems digital ground should be inter-tied only at a single point which has a low impedance path back to the system's power supplies. This will prevent modulation of the analog ground by digital power supply currents as well as digital noise injection.

The external components should be connected to the HDAC52160 with minimum length leads to help prevent noise coupling. The inputs of the external op amp are especially sensitive, so they should have short traces and be well shielded.

To the circuit driven by the HDAC52160, voltage drop in the common analog ground will appear as voltage offset. To avoid this, the HDAC52160 is provided with the DAC SENSE pin which can be used for remote ground potential sensing.



HDAC52160 Pin Assignment

PIN	PIN NAME	PIN FUNCTION
1	5V FSR	Output range scaling application resistor
2	10V FSR	Output range scaling application resistor
3	VDD	+5 volt power supply connection
4	DGND	Digital ground connection
5	VCC	+15 volt power supply connection
6	DAC OUT	Analog current output of DAC
7	DAC RTN 1	DAC ground current return path
8	VEE	-15 volt power supply connection
9	AGND	Analog ground connection
10	GAIN ADJ	Input reference trim adjustment
11	REF IN	Input for internal or external reference
12	REF OUT	Output of internal reference
13	BPO	Output offsetting application resistor
14	VEE	-15 volt power supply connection
15	DAC RTN 2	DAC ground current return path
16	DAC RTN SENSE	DAC ground current sense connection
17	D0	Input data bit 0 (LSB)
18	D1	Input data bit 1
19	D2	Input data bit 2
20	D3	Input data bit 3
21	D4	Input data bit 4
22	D5	Input data bit 5
23	D6	Input data bit 6
24	D7	Input data bit 7
25	D8	Input data bit 8
26	D9	Input data bit 9
27	D10	Input data bit 10
28	D11	Input data bit 11
29	D12	Input data bit 12
30	D13	Input data bit 13
31	D14	Input data bit 14
32	D15	Input data bit 15 (MSB)

HDAC52160 Pin Functions

** For Ordering Information See Section 1.

8-BIT, HIGH SPEED RASTER D/A CONVERTER

FEATURES:

- **125 MWPS Conversion Rate**
- **Pin-Compatible with AD9700 with Improved Performance**
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White
- ECL Compatible
- Single Power Supply
- Stable On-Chip Bandgap Reference

APPLICATIONS:

- Color or Monochrome Displays
- High Resolution Raster Graphics
- Medical Electronics: CAT, PET, MR Imaging Displays
- CRT Terminals
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion

3

GENERAL DESCRIPTION

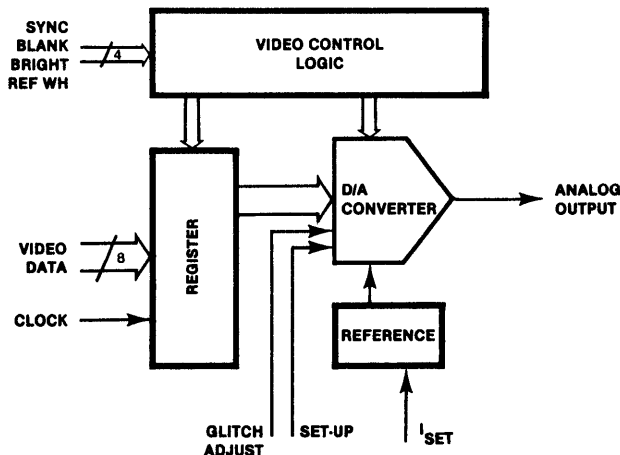
The HDAC97000 is a fully monolithic 8-bit video digital-to-analog converter specifically designed for raster graphic display applications. The HDAC97000 is complete with an 8-bit D/A converter, special video controls, on-chip bandgap reference and data registers.

Four unregistered video controls (Sync, Blank, + 10% Bright and Reference White) allow full reconstruction of RS-343-A compatible video signals from composite inputs. All data and control inputs are compatible with standard ECL.

The HDAC97000 will directly drive a doubly-terminated 75 Ohm transmission line to standard video levels.

The precision internal reference is a bandgap type, suitable for stable operation over wide temperature ranges. The HDAC97000 is fabricated using an advanced VLSI Bipolar process for excellent performance, low power consumption, and high reliability in a choice of convenient packages.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltages	
V_{EE}	- 7.0 to 0.5V
Input Voltages	
Clock, Data and Controls (measured to GND)	V_{EE} to 0.5V
Output	
Analog Output applied voltage (measured to GND)	- 3.0 to 3.0V
Analog Output applied current ²60mA
Output Short Circuit Duration	Unlimited
Temperature	
Operating, ambient	- 60 to + 140°C
junction	+ 175°C
Lead, soldering (10 seconds)	+ 300°C
Storage	- 60 to + 150°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. Current is specified as positive conventional current flowing into the device.

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN TYP MAX			UNITS
			MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS $V_{CCA} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25^\circ C, C_C = 0pF.$

I_{EE}	Supply Current		I	- 155	- 170		mA
C_{in}	Input Capacitance Clock, Data & Controls		V	3			pF
V_{OC}	Output Compliance Voltage		V	- 2		+ 0.5	V
R_{OUT}	Equivalent Output Resistance		I	560	800	1040	Ohms
C_{OUT}	Output Capacitance		V	15			pF
I_{OUT}	Maximum Output Current	$I_{REF} = MAX$	IV			- 30	mA
I_{IL}	Input Current, Logic LOW, Data & Controls		I	70	120		μA
I_{IH}	Input Current, Logic HIGH, Data & Controls		I	90	150		μA
IL	Linearity Error, Integral, Terminal Based	Notes 2, 3	I			± 0.2	% Gray Scale
DNL	Linearity Error Differential	Notes 2, 4	I			± 0.2	% Gray Scale
I_{OS}	Output Offset Current	Data = Sync = Blank = 1, Bright = 0	I	- 8	- 19		μA

ELECTRICAL SPECIFICATIONS

HDAC97000

3

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN TYP MAX			UNITS
			MIN	TYP	MAX	

DC ELECTRICAL CHARACTERISTICS $V_{CCA} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25^\circ C, C_C = 0pF.$

V_{OS} Output Offset Voltage		I	-300	-700		μV
TC_G Gain Error Tempco		IV	50			ppm/ $^\circ C$
PSS Power Supply Sensitivity	Supply to Output	I		.005		%/V
V_{EE} Supply Voltage			-4.75	-5.2	-5.5	V
V_{IL} Input Voltage, Logic LOW		I		-1.70		V
V_{IH} Input Voltage, Logic HIGH		I	-0.90			V
RESOLUTION (full scale)		I	8			Bits
LSB WEIGHT (voltage) ⁵		I	2.5			mV
LSB WEIGHT (current) ⁵		I	66.67			μA
TEMPERATURE COEFFICIENTS		IV	30			ppm/ $^\circ C$
Linearity			12			ppm/ $^\circ C$
Zero Offset			50			ppm/ $^\circ C$
Gain Error						ppm/ $^\circ C$
DATA INPUTS [Complementary Binary (CBN)]						
Logic Compatibility				ECL		V
Logic Voltage Levels "1" (Positive Logic) "0"			-0.9		-1.7	V
Input Capacitance	to VEE			5		pF
Input Resistance	to VEE			50		K Ω
REFERENCE WHITE, COMPOSITE SYNC, BLANKING AND 10% BRIGHT INPUTS						
Logic Compatibility				ECL		V
Logic Voltage Levels "1" (Positive Logic) "0"			-0.9		-1.7	V
Input Capacitance	to VEE			5		pF
Input Resistance	to VEE			50		K Ω

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS $V_{CCA} = 0.0V, V_{EEA} = V_{EED} = -5.2V \pm 0.3V, T_A = 25^\circ C, C_C = 0pF.$						
SET-UP CONTROL ^{5, 6} Ground		V		0		mV (0 IRE Units)
Open		V		-53.6		mV (7.5 IRE Units)
1K Ohm to -5.2 Supply		V		-71.4		mV (10 IRE Units)
-5.2V		V		-142.9		mV (20 IRE Units)
OUTPUT-COMPOSITE SYNC ^{5, 6} Current		V		0 or -7.6		mA (±5%)
Voltage		I		0 or -286		mV (±5%)
OUTPUT-10% BRIGHT ^{5, 7} Current		V		0 or -1.9		mA (±5%)
Voltage		I		0 or -71		mV (±5%)
OUTPUT-COMPOSITE BLANKING ^{5, 6} Current		V		0 and -1.43 -1.90 or -3.81		mA (±5%)
Voltage		I		0 and -53.6 -71 or -142.9		mV (±5%)
POWER REQUIREMENTS Current Consumption (-5.2V) Power Dissipation Power Supply Rejection		V		140 728 .025/.25		mA mW % Gray Scale/
TEMPERATURE RANGE Operating (Ambient) Storage				-25 -55	+85 +150	°C °C

DC ELECTRICAL CHARACTERISTICS NOTES

* $\theta_{CA} = 30^\circ C/W$ typical at 500 LFPM.

1. The sum of t_{pWL} and t_{pWH} must always equal or exceed the minimum conversion cycle time.
2. Gray Scale = Video White Level - Video Black Level = 643mV (nominal)
3. ± % Gray Scale = LSB (Least Significant Bit).
4. ± % Gray Scale = LSB (Least Significant Bit).
5. 90 IRE Full Gray Scale.
6. Relative to Black.
7. Reference White, Composite Sync, and Composite Blanking are enabled with logic "0"; 10% Bright is enabled with logic "1". Composite Sync or Composite Blanking control signals reset input registers.

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN TYP MAX			UNITS
			MIN	TYP	MAX	

AC ELECTRICAL CHARACTERISTICS $R_L = 37.5 \text{ Ohms}$, $C_L = 5\text{pF}$ $T_A = 25^\circ\text{C}$

F	Maximum Conversion Rate	Note 2	I	125		MWPS
T_d	Clock to Output Delay		I	4.0		ns
t_{st}	Settling Time	$\pm \frac{1}{2}$ LSB $\pm 0.2\%$ Gray Scale ³	V	10		ns
t_r, t_f	Rise/Fall Time	10% to 90% of Gray Scale ³	I		1.75	ns
SR	Slew Rate		I	300	450	V/ μ s
t_{PWL}	Clock Pulse Width, LOW ¹		I	2.5		ns
t_{PWH}	Clock Pulse Width, HIGH		I	2.5		ns
t_s	Setup Time, Data and Controls		I	2.5	1.5	ns
t_H	Hold Time, Data and Controls		I	1	-0.5	ns
PSRR	Power Supply Rejection Ratio	Supply to Output ⁵	V		-22	dB
G_E	Peak Glitch Area ("Energy")	Notes 5, 6	V	35		pico-Volt-Seconds
FT_C	Feedthrough, Clock	Data = Constant ⁷	I	-20		dB
FT_D	Feedthrough, Data	Clock = Constant ⁷				dB
SPEED PERFORMANCE-GRAY SCALE OUTPUT						
	Settling Time (Voltage Max.)		V	10		ns (to 0.4% of Gray Scale)
	Slew Rate			400		V/ μ s
	Update Rate			125		MWPS
	Rise Time			1.5		ns
	Glitch Energy			50		pV-s
STOBE INPUT						
	Logic Compatibility	Logic Loading	V	ECL		
	Logic Voltage Levels "1"	5pF and 50k Ω		-0.9		V
	(Positive Logic) "0"	To -5.2V		-1.7		V
	Set-up Time (Data)			1.5		ns
	Hold Time (Data)			0		ns
	Propagation Delay			4		ns

ELECTRICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
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AC ELECTRICAL CHARACTERISTICS $R_L = 37.5 \text{ Ohms}$, $C_L = 5\text{pF}$, $T_A = 25 \text{ to } +85^\circ\text{C}^*$

SPEED PERFORMANCE-CONTROL INPUTS	Settling Time To 10% of Final Value	V				
Composite Sync				10		ns
Composite Blank				10		ns
Reference White				10		ns
Reference Black				10		ns
10% Bright				10		ns

AC ELECTRICAL CHARACTERISTICS NOTES

* $\theta_{CA} = 30^\circ\text{C/W}$ typical at 500 LFPM.

- The sum of t_{pWL} and t_{pWH} must always equal or exceed the minimum conversion cycle time.
- MWPS-MegaWords Per Second \approx MHz.
- Gray Scale = Video White Level - Video Black Level = 643 mV (nominal).
- 20 KHz, 600mV p-p ripple superimposed on V_{EE} ; dB relative to full Gray Scale = 0dB.
- Glitch can be further reduced by trimming Glitch Adjust.
- Glitch Area (voltage time) is sometimes referred to as an "energy", although this is not dimensionally correct. The Peak Glitch Area is the maximum area deviation from the ideal output. Since glitches are typically "doublets" of symmetric positive and negative excursions, the average glitch area approaches zero.
- dB relative to full Gray Scale = 0dB, 300 MHz bandwidth limit.

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified conditions.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL TEST PROCEDURE

- I 100% production tested at the specified temperature.
- II 100% production tested at $T_a = 25^\circ\text{C}$, and sample tested at specified temperature.
- III QA sample tested only at specified temperatures.
- IV Parameter is guaranteed (but not tested) by design and characterization data.
- V Parameter is a typical value for information purposes only.

HDAC97000 VIDEO DAC CHARACTERISTICS

COMPOSITE VIDEO SIGNAL

256 gray levels plus Sync, Blank, Bright and Reference White

STEP SIZE

2.5mV

GRAY SCALE RANGE

0.6375 V Peak to Peak

HDAC97000 VIDEO DAC CHARACTERISTICS

REFERENCE WHITE LEVEL

+ 100 IRE Units (+ 0.714V) relative to Blanking Level with standard set-up,
(+ 0.6375V relative to Reference Black)

DIGITAL INPUT FOR REFERENCE WHITE

All ones (11111111)

REFERENCE WHITE CONTROLS - PIN 16

Logic "0" overrides Video Input Word and drives to Reference White Level

REFERENCE BLACK LEVEL

- 0.7085 Absolute
+ 10 IRE Units (+ 71mV) relative to Blanking Level with standard set-up

DITIGAL INPUT FOR REFERENCE BLACK

All zeros (00000000)

SET-UP CONTROL

User Programmable in four levels to set Blanking Level (relative to Reference Black)

	<u>mV</u>	<u>IRE Units</u>
1. Input Grounded	0	0
2. Input Open	- 53.6	7.5
3. Input 1K Ohm to - 5.2V	- 71.4	10 (Standard Set-up)
4. Input to - 5.2V	- 142.9	20

COMPOSITE BLANKING LEVEL (with standard set-up)

- 0.785V Absolute
- 10 IRE Units (- 71mV) relative to Reference Black

COMPOSITE BLANKING CONTROL - PIN 18

Logic "0" overrides Video Input Word and drives output negative by the amount of set-up voltage relative to the Reference Black Level

COMPOSITE SYNC LEVEL

- 1.071V absolute with standard set-up
- 40 IRE Units (- 0.286V) relative to Blanking Level

COMPOSITE SYNC CONTROL - PIN 17

Logic "0" overrides Video Input Word and drives output 0.286V negative relative to the Reference Black Level (relative values of Blank and Sync Levels sum together with both active)

10% BRIGHT LEVEL

0V Absolute
All levels are shifted down by 71mV when the 10% Bright Control is used

10% BRIGHT LEVEL - PIN 19

Logic "0" causes output to go positive by 71mV relative to Reference White Level

STROBE INPUT - PIN 11

Logic "0" to "1" transition clocks input register - input data held by latch, slave latch tracks master latch data
Logic "1" to "0" transition - slave latch holds previous data, master latch tracks input

APPLICATION INFORMATION

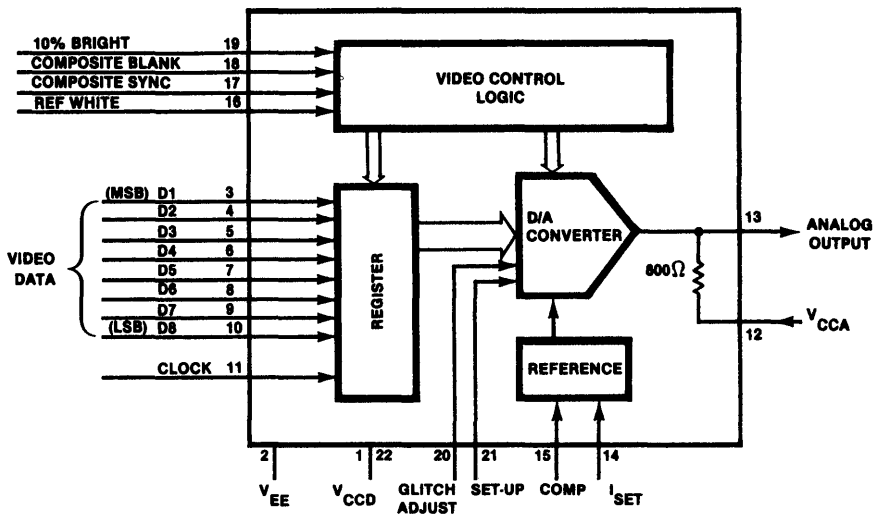
The HDAC97000 is a fully monolithic 8-bit video D/A Converter for graphic display applications. It has complete composite controls including Sync, Blank, Reference White, Set-up and 10% Bright, and will directly drive a 75 Ohm load to RS-343-A video levels. All data and control inputs are compatible with standard ECL. The HDAC97000 is packaged in a 22 lead dual-in-line package and is pin-compatible with the Analog Devices AD9700.

The video control inputs (Sync, Blank, Bright and Reference White) are used for reconstruction of RS-343-A compatible signals from video control inputs.

Video set-up level (the difference between video black and video blank) may be programmed for 0, 7.5, 10, or 20 IRE units, depending on the condition of the Set-up Select control.

The HDAC97000 uses a fully binary weighted approach utilizing current switches to implement the DAC. The upper 3 bits are segmented with interdigitated current sources for good matching and better linearity. Each data pin has latches for deskewing input data if the data arrives at different times. This prevents glitches from occurring at the output.

FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the HDAC97000 in a color raster application is shown in Figure 2. Although the HDAC97000 requires few external components and is extremely easy to use, there are several considerations that should be noted to achieve best performance. The very high operating speeds of the HDAC97000 require good circuit layout, decoupling of supplies, and proper design of transmission lines.

Video input data and controls may be directly connected to the HDAC97000. Note that all ECL inputs are terminated as close to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 Ohms, which is easily terminated using a

330 Ohm resistor to V_{EE} and a 220 Ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 Ohms to -2 Volts without the need for a 2 Volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that the stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The HDAC97000 provides separate digital and analog V_{cc} connections to simplify grounding layout.

The analog output and I_{SET} pin are configured so the device can directly drive a 37.5 Ohm impedance system as shown. The source impedance of the HDAC97000 output is 800 Ohms ± 30%, thus needing an external source-termination resistor to drive a 75 Ohm transmission line. The load resistor (R_L) must be 82.8 Ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission line has a matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of source termination resistor R_S, load resistor R_L and load terminator R_T minimizes reflections of both forward and reverse travelling waves in the analog transmission system. The return path for analog output current is V_{CCA}, which is connected internally to the source-termination resistor, R_S.

No external reference is required for operation of the HDAC97000, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges.

The HDAC97000 operates from a single standard +5 Volt or -5.2 Volt supply. Proper bypassing of the supplies will augment the HDAC97000's inherent supply noise rejection characteristics. As shown, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away. Additional decoupling can be accomplished by placing a .01μF between the compensation pin (15) and V_{CCA}. This pin connects internally to the DAC reference, which provides the DAC DC bias.

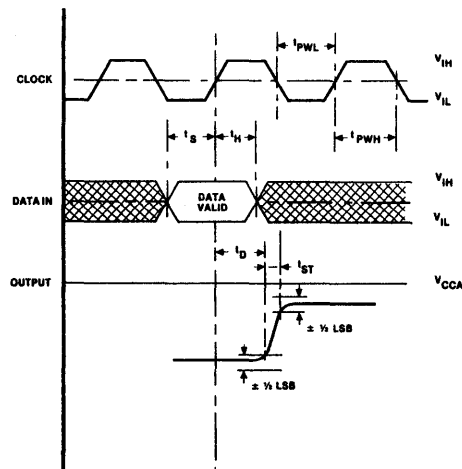
The timing diagram for the HDAC97000 is shown in Figure 1. Data to the DAC is simultaneously entered on the rising edge of the clock. Data must be valid for a set-up time of t_S before, and for a hold time of t_H after the rising edge of the clock, in order to be correctly entered. The DAC outputs will change in accordance to the clocked input data after a delay time of t_D. The settling time is specified as the time from when the DAC output is no longer within ½ LSB of the previous value until it is within ½ LSB of the new value.

The video control inputs cause the DAC output to change directly, without regard to the clock input. All video controls (Sync, Blank, Bright and Reference White) are active-Low (negative true) logic. Figure 3 illustrates the operation of Sync and Blank inputs and the resulting video output signal. As shown, both Sync and Blank must be Low to achieve the proper video Sync level. The video control input hierarchy is given in Table 1, with typical output levels for a set-up level of 10 IRE.

Set-up level is the difference between video Blank and Black levels. The HDAC97000 supports set-ups of 0, 7.5, 10, and 20 IRE, which are programmed by connecting the Set-up select input to ground (0V), not connected, to V_{EE} through a 1K Ohm resistor, or to V_{EE} (-5.2V), respectively. For most applications the 7.5 IRE option is suitable.

The Reference White input forces the DAC outputs to an all "1"'s level, which is video "white" in most systems. This is especially useful for clearing the display screen to white during system reset or power-up. The Bright input adds 10% of full-scale video to the present video level. The Bright feature is commonly used for highlighting cursors or creating overlays of video information. Sync, Blank and Reference White override the data inputs, while Bright may be applied to any video level.

FIGURE 1 TIMING DIAGRAM



SETTING OUTPUT DRIVE CAPABILITY

The current set pin (pin 14) adjusts the full-scale output current of the HDAC97000. The resistor designated R_{SET} , which governs the current into pin 14, can be calculated in relation to DAC output current as follows:

$$\text{Equation 1: } R_{SET} = \frac{90}{22.59} \left[\frac{1.23V}{V_{OUT.G.S.}/R_{LOAD}} \right]$$

Here, 1.23V is the internal reference voltage, $V_{OUT.G.S.}$ is the DAC gray scale output voltage and R_{LOAD} is the total load resistance on the analog output. In raster scan video applications, R_{LOAD} could be equivalent to the load in Figure 2. This would be the internal DAC output resistance in parallel with the output load and cable terminating resistor. If the device is being used in raster scan applications, the total output voltage is the gray scale current plus the video function currents. The value of R_{SET} using the total current (or voltage) can be calculated with equation 2:

$$\text{Equation 2: } R_{SET} = \frac{140 + B}{22.59} \left[\frac{1.23V}{V_{OUT}/R_{LOAD}} \right]$$

where B is equal to the value of the setup (BLANK) level (0, 7.5, 10 or 20). The total output voltage capability is 1.13V, which is more than adequate for composite video waveforms.

In other applications where lighter loads are used, R_{SET} can be increased, thus decreasing power dissipation since the output current is decreased. Figure 7 shows an example where this applies if a large output voltage or current swing is not needed.

GLITCH ADJUST AND COMPENSATION

Glitch adjust and compensation are optional functions that can be used to improve dynamic performance. Glitch adjust is an external adjustment of the logic threshold in the DAC switches to skew the speed in order to get an output glitch energy below the data sheet specification. This can be done with a resistive pot in conjunction with pin 20 and V_{EE} as shown in Figure 2. Adjust the pot for minimum output glitch when the input code is toggling between 01111111 and 10000000; the code transition which normally causes the largest glitch.

Compensation is accomplished by connecting a .01 μ F capacitor to pin 15. Actually this is a decoupling capacitor connected internally to the DAC biasing network. It adds more decoupling as needed if operating with a noisy supply or environment as well as decoupling internal switching noise. This is different than the AD9700, which uses the capacitor to externally compensate the voltage reference buffer amplifier. The amplifier in the HDAC97000 is internally compensated and therefore the compensation pin is used for the optional decoupling function.

FIGURE 2 HDAC97000 TYPICAL INTERFACE CIRCUIT

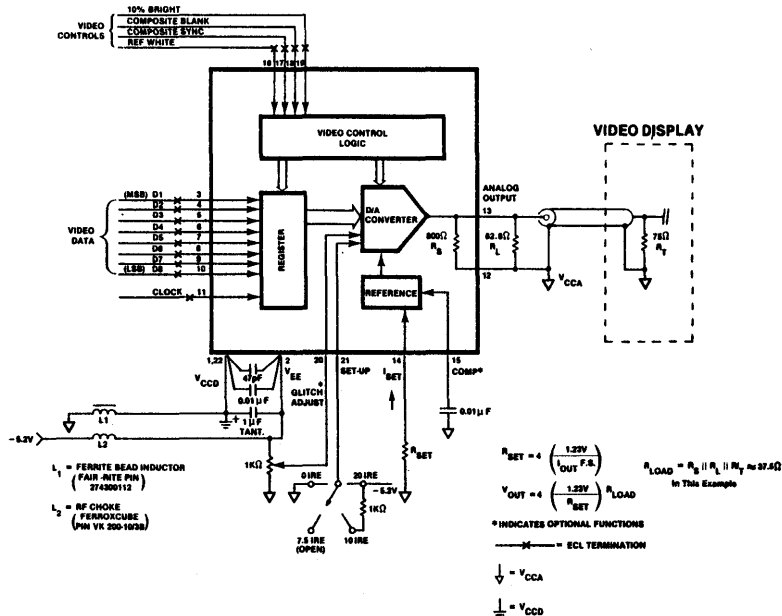


Table 1 Video Control Operation (Output values for Set-up = 10 IRE and 75 Ohm standard load)¹

Sync ^{2 3}	Blank ²	Ref White	Bright	Data Input	Out (V) ⁴	Out (IRE) ⁵	Description
0	0	1	1	XXXXXXXX	-1.071	-40	Sync Level
1	0	1	1	XXXXXXXX	-0.785	0	Blank Level
1	1	0	1	XXXXXXXX	-0.071	100	Normal White Level
1	1	0	0	XXXXXXXX	0.0	110	Enhanced White Level
1	1	1	1	11111111	-0.071	100	Normal White Level
1	1	1	0	11111111	0.0	110	Enhanced White Level
1	1	1	1	00000000	-0.7085	10	Normal Black Level
1	1	1	0	00000000	-0.6375	20	Enhanced Black Level

Notes:

1. All Video Controls are active-Low (negative true) logic.
2. Sync and Blank output levels are dependent on set-up level selected. Values indicated are set-up = 10 IRE set-up select connected through a 1K Ohm resistor to V_{EE}.
3. Sync level requires that both Sync and Blank = 0.
4. 140 IRE = 1.00 Volt.
5. All control values are subject to tolerance of ± 5% Gray Scale.
6. Analog output values shown are based on a step size of 2.5mV per LSB (used for ease of calibration). This causes the Gray Scale output to be 637.5mV rather than 643mV in the idealized video output waveform. Both values are within the tolerances of RS-343-A.

3

Table 2 Set-up Select

Set-up Control Input	Set-up Level
0 Volts (GND)	0 IRE
Not Connected	7.5 IRE
1K Ohm to -5.2V (V _{EE})	10 IRE
-5.2 Volts (V _{EE})	20 IRE

FIGURE 3 VIDEO OUTPUT WAVEFORM FOR STANDARD LOAD & 10 IRE SET-UP

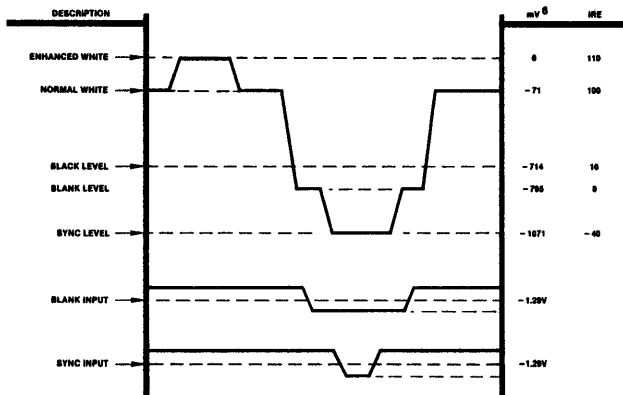


FIGURE 4 EQUIVALENT INPUT CIRCUIT, DATA, CLOCK, & CONTROL

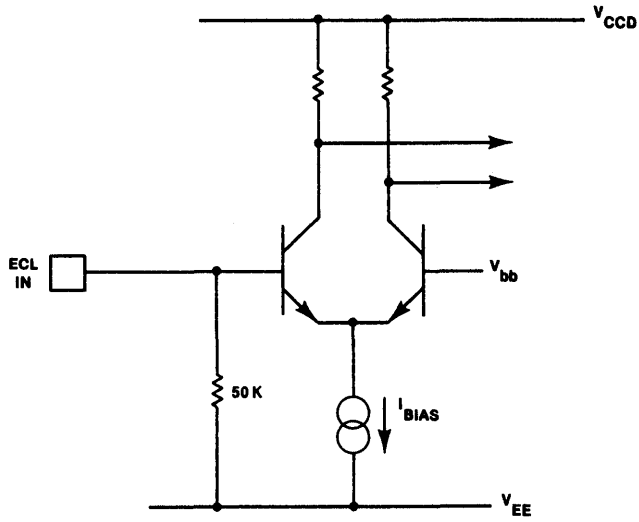


FIGURE 5 DAC OUTPUT CIRCUIT

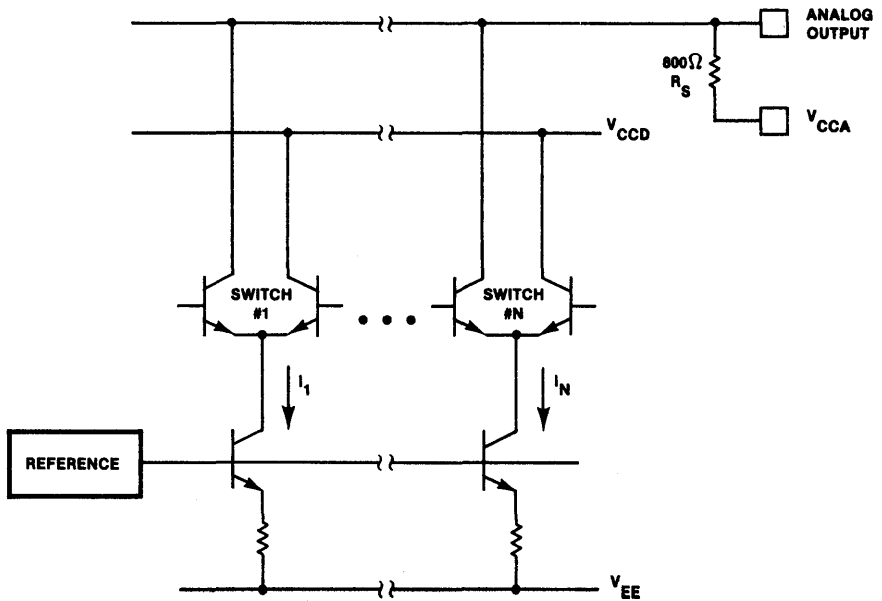
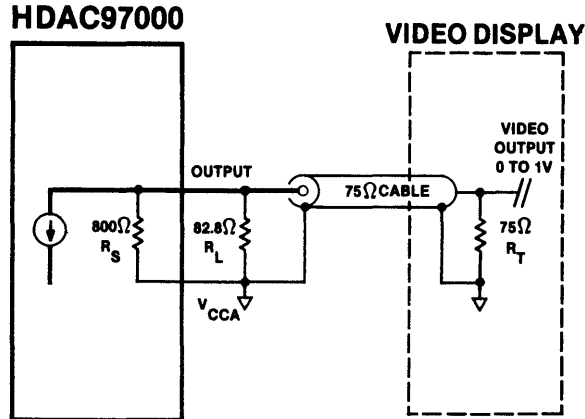


FIGURE 6 STANDARD LOAD



HDAC97000 AS A STANDARD D/A CONVERTER

The HDAC97000 is primarily designed to be used in composite video applications, but with its inherent speed, it can also be utilized in other applications requiring up to 200 MegaWords Per Second update rate.

When implemented as a standard DAC, some of the video control inputs should be connected to ground through a diode as indicated in Figure 7 (opposite page). Composite Sync and Blank as well as Reference White are connected in this manner (pin 16, 17 and 18). The set-up pin (21) is tied directly to ground and the 10% Bright pin (19) is left open. If 8-bits of resolution are not necessary, the unused inputs should be tied to ground through a diode to prevent an output offset voltage.

HDAC97000 IN A SINGLE +5V TTL LOGIC SYSTEM

The HDAC97000 is primarily designed for ECL logic systems which perform better in high-speed applications, but the DAC can be configured for TTL levels as shown in Figure 8 (opposite page). It can be used in systems that only have a +5V power supply available for the DAC. If any of the data inputs, Composite Blank and Sync or Reference White are not used, they should still be tied up to +5V as shown. If the 10% Bright is not used, it should be grounded or left open. Also, note the different set-up conditions as well as the pull-ups on the output.

FIGURE 7 STANDARD D/A CONVERTER

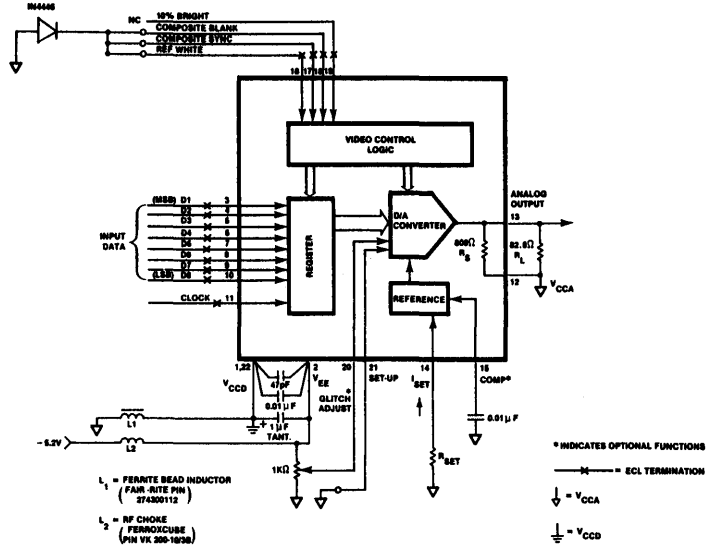
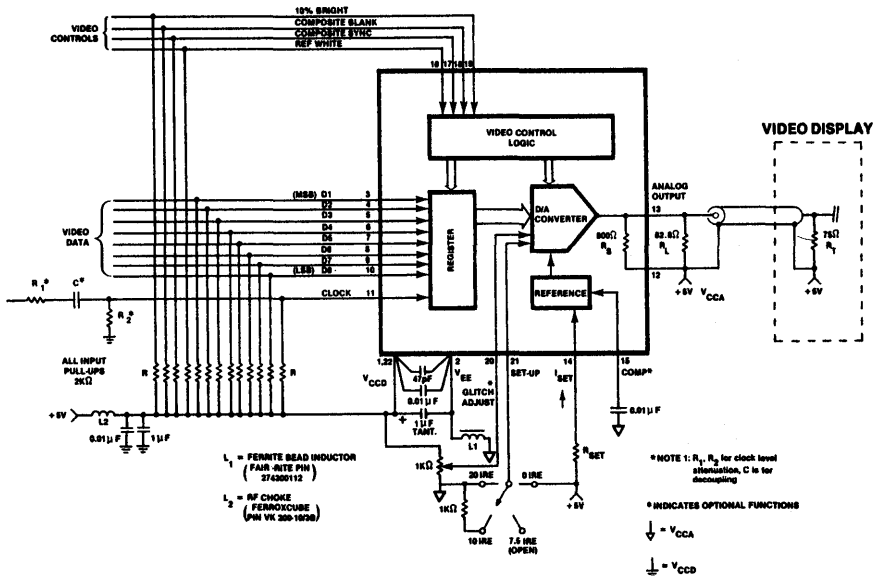
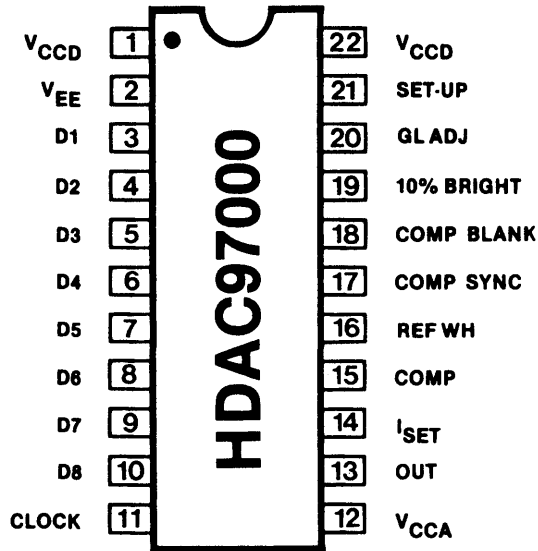


FIGURE 8 TTL-COMPATIBLE HDAC97000



PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
V _{CCD}	Positive Digital Supply
V _{EE}	Negative Supply Voltage
D1	Data Input Bit 1 (MSB)
D2	Data Input Bit 2
D3	Data Input Bit 3
D4	Data Input Bit 4
D5	Data Input Bit 5
D6	Data Input Bit 6
D7	Data Input Bit 7
D8	Data Input Bit 8 (LSB)
CLOCK	Conversion Clock Input
OUT	Analog Video Output
I _{SET}	Reference Current Set
COMP	Decoupling Capacitor Connection
REF WH	Reference White Input
COMP SYNC	Composite Video Sync Input
COMP BLANK	Composite Video Blank Input
10% BRIGHT	+ 10% Bright Input
GL ADJ	Glitch Adjust Connection
SET-UP	Video Set-Up Select
V _{CCA}	Positive Analog Supply

**For Ordering Information See Section 1.

NOTES:

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

SINGLE ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay < 2.5ns
- Propagation Delay Skew < 300ps
- 100MHz Minimum Tracking Bandwidth
- Low Offset $\pm 1\text{mV}$
- Low Feedthrough
- Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

GENERAL DESCRIPTION

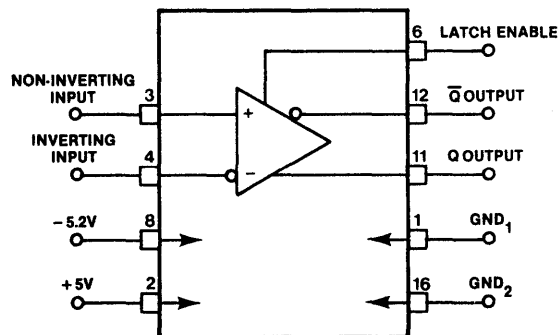
The HCMP96850 is a single, very high speed, monolithic comparator. It is pin-compatible with, and has improved performance over Plessey's SP9685 and AMD's AM6685. The HCMP96850 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96850 is available in 16 Lead DIP, or in die form.

BLOCK DIAGRAM

HCMP96850 HIGH SPEED COMPARATOR



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25°C

Supply Voltages

Positive Supply Voltage (V_{CC} measured to GND)	- 0.5 to + 6.0V
Negative Supply Voltage (V_{EE} to GND)	- 6.0 to + 0.5V
Ground Voltage Differential	- 0.5 to + 0.5V

Input Voltages

Input Voltage	- 4.0 to + 4.0V
Differential Input Voltage	- 5.0 to + 5.0V
Input Voltage, Latch Controls	V_{EE} to 0.5V

Output

Output Current	30mA
--------------------------	------

Temperature

Operating Temperature, ambient	- 55 to + 125°C
junction	+ 150°C
Lead Temperature, (soldering 60 seconds)	+ 300°C
Storage Temperature	- 65 to + 150°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

INDUSTRIAL TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = -5.2\text{V} \pm .3\text{V}$, $R_L = 50\ \Omega$ (Unless otherwise specified)						
V_{OS}	Input Offset Voltage	$R_S = 0\ \Omega$	I	-3	+3	mV
V_{OS}	Input Offset Voltage	$R_S = 0\ \Omega$, $T_{MIN} < T_A < T_{MAX}^2$	IV	-3.5	+3.5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Tempco		V	4		$\mu\text{V}/^\circ\text{C}$
I_{BIAS}	Input Bias Current		I	4	± 20	μA
I_{BIAS}	Input Bias Current	$T_{MIN} < T_A < T_{MAX}^2$	IV	7		μA
I_{OS}	Input Offset Current		I	-1.0	+1.0	μA
I_{OS}	Input Offset Current	$T_{MIN} < T_A < T_{MAX}^2$	IV	-1.5	+1.5	μA
I_{CC}	Positive Supply Current		I	3.3	5	mA
I_{EE}	Negative Supply Current		I	13.5	18	mA
V_{CM}	Common Mode Range		I	-2.5	+2.5	V
A_{VOL}	Open Loop Gain		V	4000		V/V
R_{IN}	Input Resistance		V	60		K Ω
C_{IN}	Input Capacitance		V	3		pF
C_{IN}	Input Capacitance	(LCC Package)	V	1		pF
PSS	Power Supply Sensitivity		V	70		dB
CMRR	Common Mode Rejection Ratio		V	80		dB
P_D	Power Dissipation Dual		I		250	mW

OUTPUT LOGIC LEVELS (ECL 10KH Compatible) $T_A = 25^\circ\text{C}$

V_{OH}	Output High	50 Ω to -2V	I	- .98	- .81	V
V_{OL}	Output Low	50 Ω to -2V	I	- 1.95	- 1.63	V

INDUSTRIAL TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS						
$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = -5.2\text{V} \pm .3\text{V}$, $R_L = 50\text{ Ohms}$ (Unless otherwise specified)						
t_p	Propagation Delay	10mV O.D.		2.4	3	ns
t_s	Latch Set-up Time			0.6	1	ns
$t_{p(E)}$	Latch to Output Delay	50mV O.D.			3	ns
$t_{pW(E)}$	Latch Pulse Width			2		ns
$t_{H(E)}$	Latch Hold Time				0.5	ns
t_r	Rise Time	20% to 80%		1.76		ns
t_f	Fall Time	20% to 80%		1.76		ns
f_c	Min Clock Rate			300		MHz

Notes:

- 100mV input step.
- Temperature Range - 25 to +85°C

4

MILITARY TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = -5.2\text{V} \pm .3\text{V}$, $R_L = 50\text{ Ohms}$ (Unless otherwise specified)						
V_{OS}	Input Offset Voltage	$R_S = 0\text{ Ohms}$	-3		+3	mV
V_{OS}	Input Offset Voltage	$R_S = 0\text{ Ohms}$, $T_{MIN} < T_A < T_{MAX}^2$	-4		+4	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Tempco			4		$\mu\text{V}/^\circ\text{C}$
I_{BIAS}	Input Bias Current			4	± 20	μA
I_{BIAS}	Input Bias Current	$T_{MIN} < T_A < T_{MAX}^2$	-50	7	50	μA
I_{OS}	Input Offset Current		-1.0		+1.0	μA
I_{OS}	Input Offset Current	$T_{MIN} < T_A < T_{MAX}^2$	-7		+7	μA
I_{CC}	Positive Supply Current			3.3	5	mA
I_{EE}	Negative Supply Current			13.5	18	mA
V_{CM}	Common Mode Range		-2.5		+2.5	V
A_{VOL}	Open Loop Gain			4000		V/V
R_{IN}	Input Resistance			60		KOhms
C_{IN}	Input Capacitance			3		pF
C_{IN}	Input Capacitance	(LCC Package)		1		pF

MILITARY TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
-----------	-----------------	------------	-----	-----	-----	-------

DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = -5.2\text{V} \pm .3\text{V}$, $R_L = 50\ \text{Ohms}$ (Unless otherwise specified)

PSS	Power Supply Sensitivity	Over Temp	I	70 50		dB
CMRR	Common Mode Rejection Ratio	Over Temp	I	80 68		dB
P_D	Power Dissipation		I		125	mW

OUTPUT LOGIC LEVELS (ECL 10KH Compatible) $T_A = 25^\circ\text{C}$

V_{OH}	Output High	50 Ohms to -2V	I	-.98	-.81	V
V_{OL}	Output Low	50 Ohms to -2V	I	-1.95	-1.63	V

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = 5.2\text{V} \pm .3\text{V}$, $R_L = 50\ \text{Ohms}$ (Unless otherwise specified)

t_p	Propagation Delay	10mV O.D.	I	2.4	3	ns
t_s	Latch Set-up Time		I	0.6	1	ns
$t_p(E)$	Latch to Output Delay	50mV O.D.	I		3	ns
$t_{PW(E)}$	Latch Pulse Width		V	2		ns
$t_H(E)$	Latch Hold Time		I		0.5	ns
t_r	Rise Time	20% to 80%	V	1.76		ns
t_f	Fall Time	20% to 80%	V	1.76		ns
f_c	Min Clock Rate		V	300		MHz

Notes:

- 100mV input step.
- Temperature Range -55 to $+125^\circ\text{C}$

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL

TEST PROCEDURE

- | | |
|-----|---|
| I | 100% production tested at the specified temperatures. |
| II | 100% production tested at $T_a = 25^\circ\text{C}$, and sample tested at the specified temperatures. |
| III | QA sample tested only at the specified temperatures. |
| IV | Parameter is guaranteed (but not tested) by design and characterization data. |
| V | Parameter is a typical value for information purposes only. |

GENERAL INFORMATION

The HCMP96850 is an ultra high speed single voltage comparator. It offers tight absolute characteristics which guarantee matching from package-to-package. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 Ohm transmission lines.

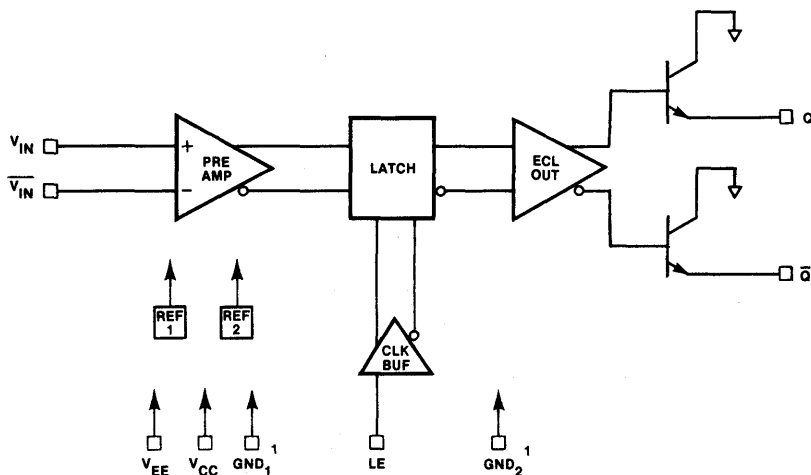
The HCMP96850 has one latch enable control and can be driven by standard ECL logic. It also has two separate ground pins, one for the output to accommodate large ground currents without affecting the rest of the circuit, while the other is for the small signal intermediate stages. The input stage is referenced to V_{CC} and V_{EE} .

This comparator offers the following improvements over existing devices:

- Short propagation delays
- Low offset voltage and temperature coefficient
- Low power
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

INTERNAL FUNCTIONAL DIAGRAM



NOTES: 1. HCMP96850 HAS SEPARATE OUTPUT AND INTERMEDIATE STAGE GROUND PINS

TYPICAL INTERFACE CIRCUIT

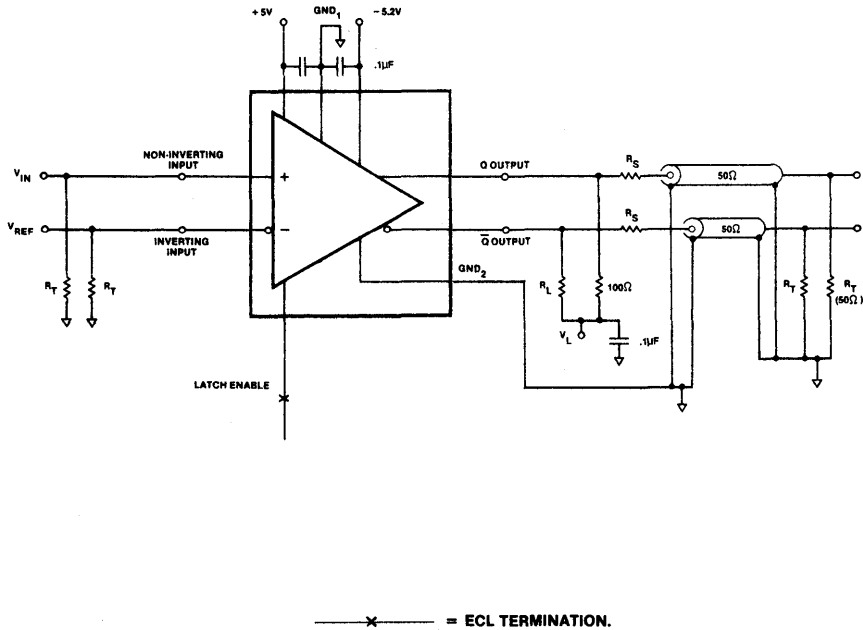
A typical interface circuit using the comparator is shown in Figure 1. Although it needs few external components and is easy to apply, there are several considerations that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96850 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques

must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The HCMP96850 is capable of driving 50 Ohm terminated lines. The termination can be directly tied to $-2.0V$, or a Thevenin equivalent terminated to the negative supply if a $-2.0V$ supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

FIGURE 1 HCMP96850 TYPICAL INTERFACE CIRCUIT



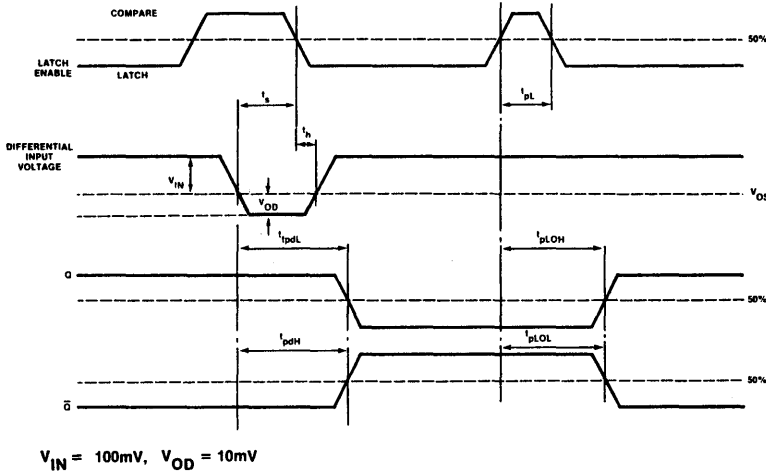
The timing diagram for the comparator is shown in Figure 2. The latch enable (LE) pulse is shown at the top. If LE is high in the HCMP96850, the comparator tracks the input difference voltage. When LE is driven low the comparator outputs are latched into their existing logic states.

enable falling edge and held for time t_{th} after the falling edge for the comparator to accept data. After t_{th} , the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pl} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL} .

The leading edge of the input signal (which consists of 10mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or \bar{Q}). The input signal must be maintained for a time t_s (set-up time) before the latch

Unused outputs must be terminated with 50 Ohms to ground while unused latch enable pins should be connected directly to ground.

FIGURE 2 TIMING DIAGRAM



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected.

SWITCHING TERMS (refer to Figure 2)

- t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.
- t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.
- t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.
- t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.
- t_s MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.
- t_h MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.
- t_{pl} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.
- $t_{pdL} - t_{pdH}$ DIFFERENTIAL PROPAGATION DELAY (SKEW) INPUT TO OUTPUT - The delay or skew between comparators.
- $t_{pLOL} - t_{pLOH}$ DIFFERENTIAL PROPAGATION DELAY (SKEW) LATCH TO OUTPUT - The skew from one comparator to another.
- V_{OD} VOLTAGE OVERDRIVE.

FIGURE 3 EQUIVALENT INPUT CIRCUIT

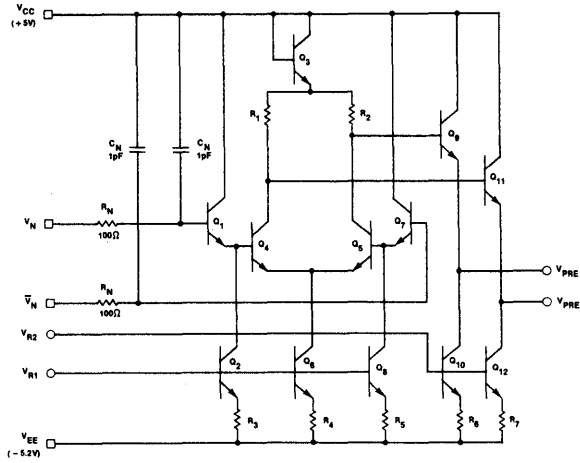


FIGURE 4 OUTPUT CIRCUIT

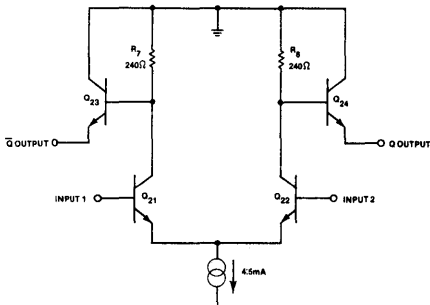


FIGURE 5A TEST LOAD

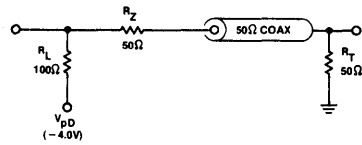
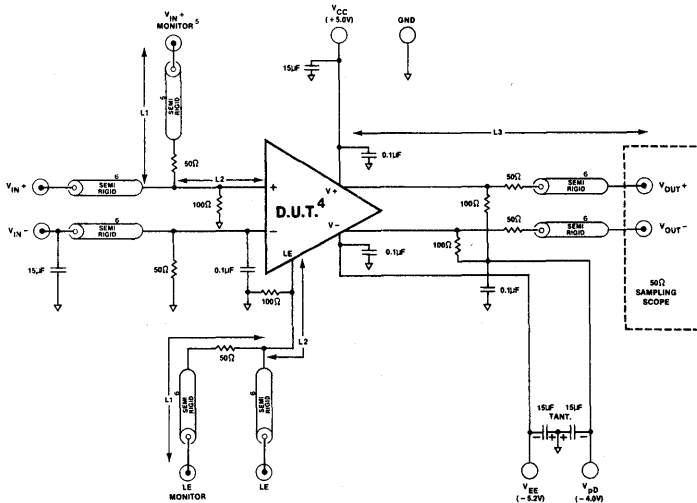
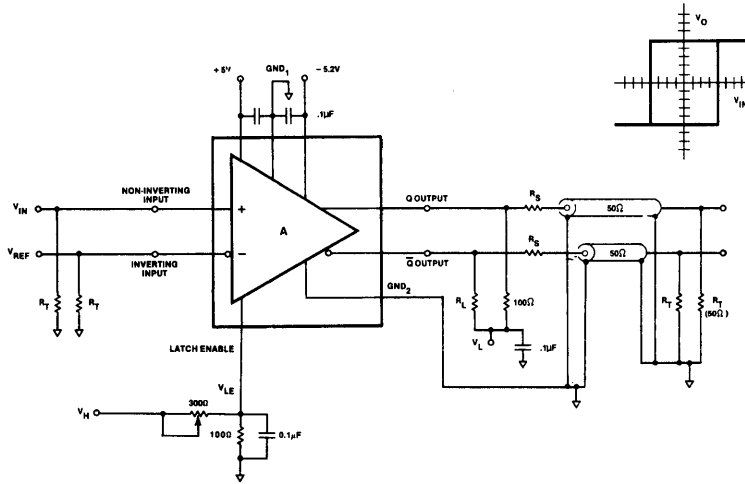


FIGURE 5B AC TEST FIXTURE



- 1. ALL BNC & SEMI RIGID COAX SHIELD ARE GROUNDED.
- 2. ALL RESISTORS 1% (50Ω = 49.9Ω).
- 3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS $L_1 = L_2 + L_3$.
- 4. D.U.T. PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
- 5. MONITOR INPUT IMPEDANCE 50Ω TO GND.
- 6. SEMI RIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

FIGURE 6 HCMP96850 WITH HYSTERESIS

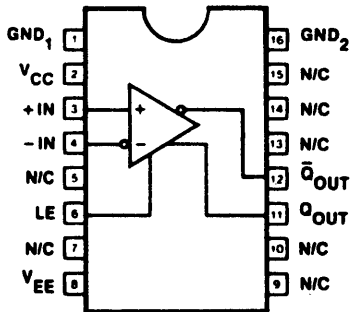


HYSTERESIS IS OBTAINED BY APPLYING
A DC BIAS TO THE LE PIN
 $V_H = -5.2V$
 $V_{LE} = -1.3V \pm 100mV$

PIN ASSIGNMENTS

PIN FUNCTIONS

TOP VIEW



16 LEAD CERDIP

NAME	FUNCTION
GND1	Circuit Ground
VCC	Positive Supply Voltage
+ IN	Non-Inverting Input
- IN	Inverting Input
N/C	No Connection
LE	Latch Enable
VEE	Negative Supply Voltage
QOUT	Output
QOUT	Inverted Output
GND2	Output Ground

**For Ordering Information See Section 1.

NOTES:

DUAL ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay < 2.3ns
- Propagation Delay Skew < 300ps
- 300MHz Minimum Tracking Bandwidth
- Low Offset $\pm 1mV$
- Low Feedthrough and Crosstalk
- Differential Latch Control – Dual Version

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

GENERAL DESCRIPTION

The HCMP96870A is a dual, very high speed monolithic comparators. It is pin-compatible with, and has improved performance over Plessey's SP9687 and AMD's AM6687. The HCMP96870 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

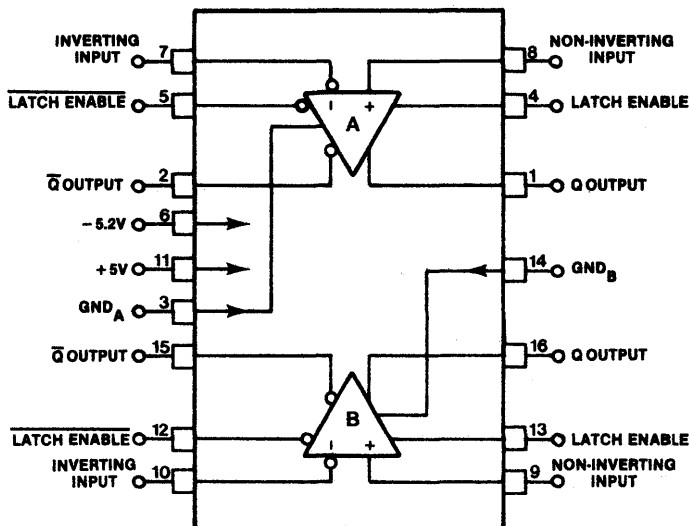
Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96870A is available in 16 Lead CERDIP, 20 Contact Leadless Chip Carriers (LCC), or in die form.

4

BLOCK DIAGRAM

HCMP96870 DUAL HIGH SPEED COMPARATOR



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)¹ 25°C

Supply Voltages

Positive Supply Voltage (V_{CC} measured to GND) - 0.5 to + 6.0V
 Negative Supply Voltage (V_{EE} to GND) - 6.0 to + 0.5V
 Ground Voltage Differential - 0.5 to + 0.5V

Input Voltages

Input Voltage - 4.0 to + 4.0V
 Differential Input Voltage - 5.0 to + 5.0V
 Input Voltage, Latch Controls V_{EE} to 0.5V

Output

Output Current 30mA

Temperature

Operating Temperature, ambient - 55 to + 125°C
 junction + 150°C
 Lead Temperature, (soldering 60 seconds) + 300°C
 Storage Temperature - 65 to + 150°C

Notes:

1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

INDUSTRIAL TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = -5.2\text{V} \pm .3\text{V}$, $R_L = 50\text{ Ohms}$ (Unless otherwise specified)						
V_{OS}	Input Offset Voltage	$R_S = 0\text{ Ohms}$	I	-3	+3	mV
V_{OS}	Input Offset Voltage	$R_S = 0\text{ Ohms}$, $T_{MIN} < T_A < T_{MAX}^2$	IV	-3.5	+3.5	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Tempco		V	4		$\mu\text{V}/^\circ\text{C}$
I_{BIAS}	Input Bias Current		I	4	± 20	μA
I_{BIAS}	Input Bias Current	$T_{MIN} < T_A < T_{MAX}^2$	IV	7	± 38	μA
I_{OS}	Input Offset Current		I	-1.0	+1.0	μA
I_{OS}	Input Offset Current	$T_{MIN} < T_A < T_{MAX}^2$	IV	-1.5	+1.5	μA
I_{CC}	Positive Supply Current		I	7	10	mA
I_{EE}	Negative Supply Current		I	27	36	mA
V_{CM}	Common Mode Range		I	-2.5	+2.5	V
A_{VOL}	Open Loop Gain		V	4000		V/V
R_{IN}	Input Resistance		V	60		KOhms
C_{IN}	Input Capacitance		V	3		pF
C_{IN}	Input Capacitance	(LCC Package)	V	1		pF
PSS	Power Supply Sensitivity		V	70		dB
CMRR	Common Mode Rejection Ratio		V	80		dB
P_D	Power Dissipation		I		250	mW

OUTPUT LOGIC LEVELS (ECL 10KH Compatible) $T_A = 25^\circ\text{C}$

V_{OH}	Output High	50 Ohms to -2V	I	- .98	-.81	V
V_{OL}	Output Low	50 Ohms to -2V	I	-1.95	-1.63	V

INDUSTRIAL TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS						
$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = -5.2\text{V} \pm .3\text{V}$, $R_L = 50\ \Omega$ (Unless otherwise specified)						
t_p	Propagation Delay	10mV O.D.		2.0	2.3	ns
t_S	Latch Set-up Time			0.6	1	ns
$t_{p(E)}$	Latch to Output Delay	50mV O.D.			3	ns
$t_{PW(E)}$	Latch Pulse Width			2		ns
$t_H(E)$	Latch Hold Time				0.5	ns
t_r	Rise Time	20% to 80%		1.2		ns
t_f	Fall Time	20% to 80%		1.2		ns
f_C	Min Clock Rate			300		MHz

Notes:

1. 100mV input step.
2. Temperature Range -25 to $+85^\circ\text{C}$

4

MILITARY TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS	
DC ELECTRICAL CHARACTERISTICS							
$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = -5.2\text{V} \pm .3\text{V}$, $R_L = 50\ \Omega$ (Unless otherwise specified)							
V_{OS}	Input Offset Voltage	$R_S = 0\ \Omega$		-3	+3	mV	
V_{OS}	Input Offset Voltage	$R_S = 0\ \Omega$, $T_{MIN} < T_A < T_{MAX}^2$		-4	+4	mV	
$\Delta V_{OS}/\Delta T$	Offset Voltage Tempco			4		$\mu\text{V}/^\circ\text{C}$	
I_{BIAS}	Input Bias Current			4	± 20	μA	
I_{BIAS}	Input Bias Current	$T_{MIN} < T_A < T_{MAX}^2$		-50	7	50	μA
I_{OS}	Input Offset Current			-1.0	+1.0	μA	
I_{OS}	Input Offset Current	$T_{MIN} < T_A < T_{MAX}^2$		-7	+7	μA	
I_{CC}	Positive Supply Current			7	10	mA	
I_{EE}	Negative Supply Current			27	36	mA	
V_{CM}	Common Mode Range			-2.5	+2.5	V	
A_{VOL}	Open Loop Gain			4000		V/V	
R_{IN}	Input Resistance			60		K Ω s	
C_{IN}	Input Capacitance			3		pF	
C_{IN}	Input Capacitance	(LCC Package)		1		pF	

MILITARY TEMPERATURE RANGE

PARAMETER	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
-----------	-----------------	------------	-----	-----	-----	-------

DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = -5.2\text{V} \pm .3\text{V}$, $R_L = 50\ \text{Ohms}$ (Unless otherwise specified)

PSS	Power Supply Sensitivity	Over Temp	I	70 50		dB
CMRR	Common Mode Rejection Ratio	Over Temp	I	80 68		dB
P_D	Power Dissipation		I		250	mW

OUTPUT LOGIC LEVELS (ECL 10KH Compatible) $T_A = 25^\circ\text{C}$

V_{OH}	Output High	50 Ohms to -2V	I	-.98	-.81	V
V_{OL}	Output Low	50 Ohms to -2V	I	-1.95	-1.63	V

AC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_{CC} = +5.0\text{V} \pm .25\text{V}$, $V_{EE} = 5.2\text{V} \pm .3\text{V}$, $R_L = 50\ \text{Ohms}$ (Unless otherwise specified)

t_P	Propagation Delay	10mV O.D.	I	2.0	2.3	ns
t_S	Latch Set-up Time		I	0.6	1	ns
$t_{P(E)}$	Latch to Output Delay	50mV O.D.	I		3	ns
$t_{PW(E)}$	Latch Pulse Width		V	2		ns
$t_{H(E)}$	Latch Hold Time		I		0.5	ns
t_r	Rise Time	20% to 80%	V	1.2		ns
t_f	Fall Time	20% to 80%	V	1.2		ns
f_c	Min Clock Rate		V	300		MHz

Notes:

- 100mV input step.
- Temperature Range -55 to $+125^\circ\text{C}$

ELECTRICAL CHARACTERISTICS TESTING

All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

TEST LEVEL

TEST PROCEDURE

- | | |
|-----|---|
| I | 100% production tested at the specified temperatures. |
| II | 100% production tested at $T_a = 25^\circ\text{C}$, and sample tested at the specified temperatures. |
| III | QA sample tested only at the specified temperatures. |
| IV | Parameter is guaranteed (but not tested) by design and characterization data. |
| V | Parameter is a typical value for information purposes only. |

GENERAL INFORMATION

The HCMP96870A is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 Ohm transmission lines.

The HCMP96870A has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

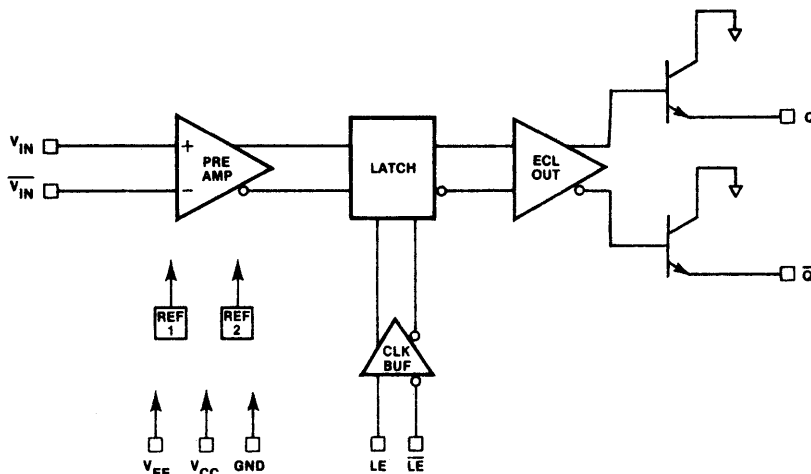
The dual comparator shares the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection. The output stage ground and intermediate ground are separated on the die, but are not bonded to the same pin.

This comparator offers the following improvements over existing devices:

- Short propagation delays
- Low offset voltage and temperature coefficient
- Low power for SMD packaging and low system power
- Good rejection between comparator channels
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

INTERNAL FUNCTIONAL DIAGRAM



TYPICAL INTERFACE CIRCUIT

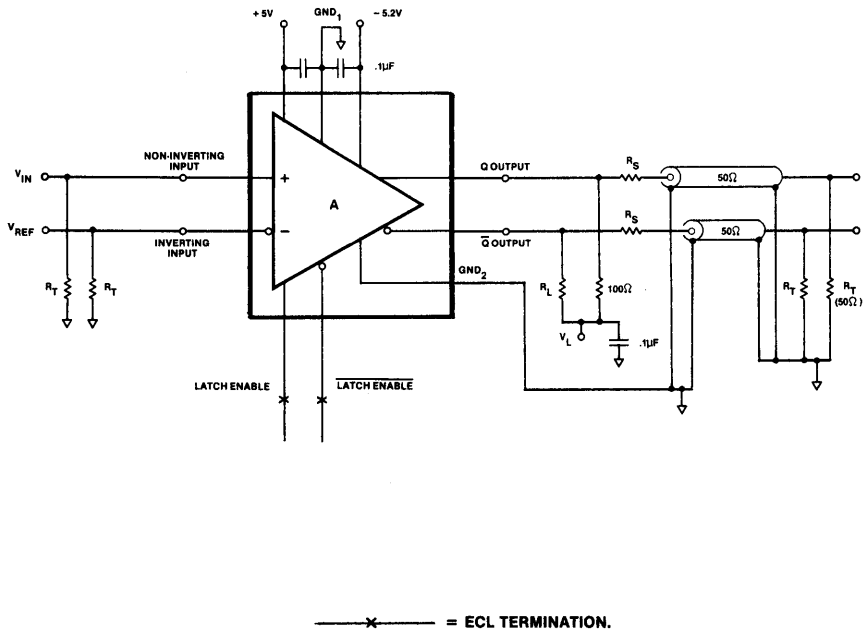
A typical interface circuit using the comparator is shown in Figure 1. Although it needs few external components and is easy to apply, there are several considerations that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96870A comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques

must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The HCMP96870A is capable of driving 50 Ohm terminated lines. The termination can be directly tied to $-2.0V$, or a Thevenin equivalent terminated to the negative supply if a $-2.0V$ supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

FIGURE 1 HCMP96870A TYPICAL INTERFACE CIRCUIT



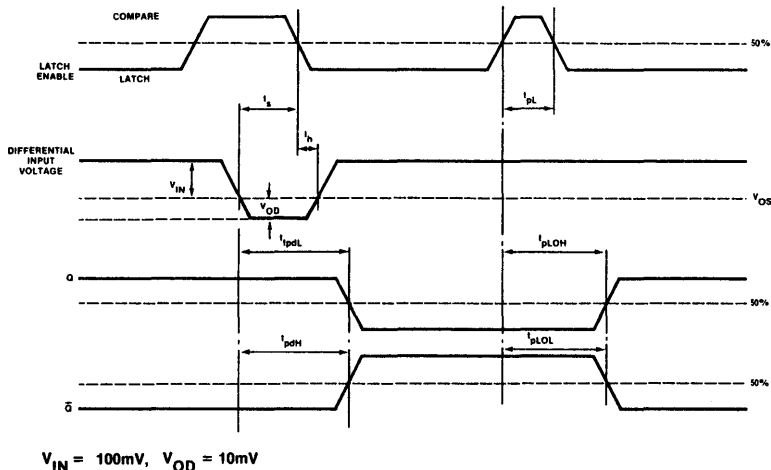
The timing diagram for the comparator is shown in Figure 2. The latch enable (LE) pulse is shown at the top. If LE is high and \overline{LE} is low in the HCMP96870A, the comparator tracks the input difference voltage. When LE is driven low and \overline{LE} high the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of 10mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or \overline{Q}). The input signal must be maintained for a time t_s (set-up time) before the latch

enable falling edge and \overline{LE} rising edge and held for time t_h after the falling edge for the comparator to accept data. After t_h , the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL} .

Unused outputs must be terminated with 50 Ohms to ground while unused latch enable pins should be connected directly to ground.

FIGURE 2 TIMING DIAGRAM



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may or may not be detected. (LE is the inverse of \overline{LE} .)

SWITCHING TERMS (refer to Figure 2)

- t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.
- t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.
- t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.
- t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.
- t_s MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

- t_h MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.
- t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire and hold an input signal change.
- $t_{pdL} - t_{pdH}$ DIFFERENTIAL PROPAGATION DELAY (SKEW) INPUT TO OUTPUT - The delay or skew between comparators.
- $t_{pLOL} - t_{pLOH}$ DIFFERENTIAL PROPAGATION DELAY (SKEW) LATCH TO OUTPUT - The skew from one comparator to another.
- V_{OD} VOLTAGE OVERDRIVE.

FIGURE 3 EQUIVALENT INPUT CIRCUIT

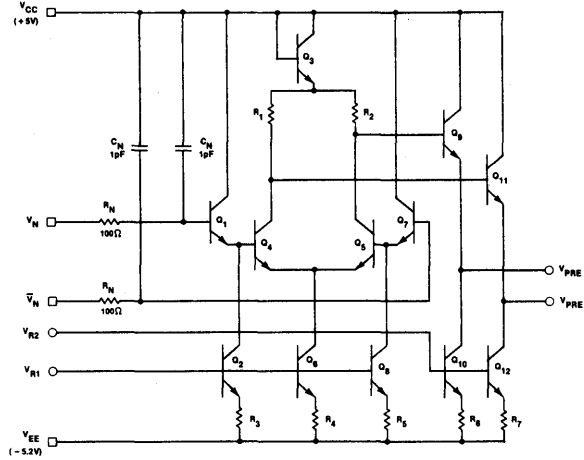


FIGURE 4 OUTPUT CIRCUIT

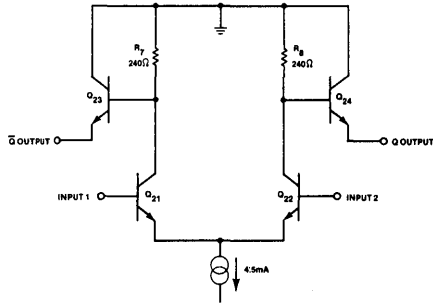


FIGURE 5A TEST LOAD

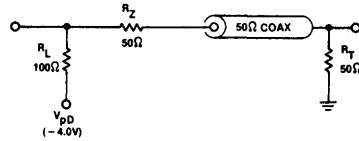
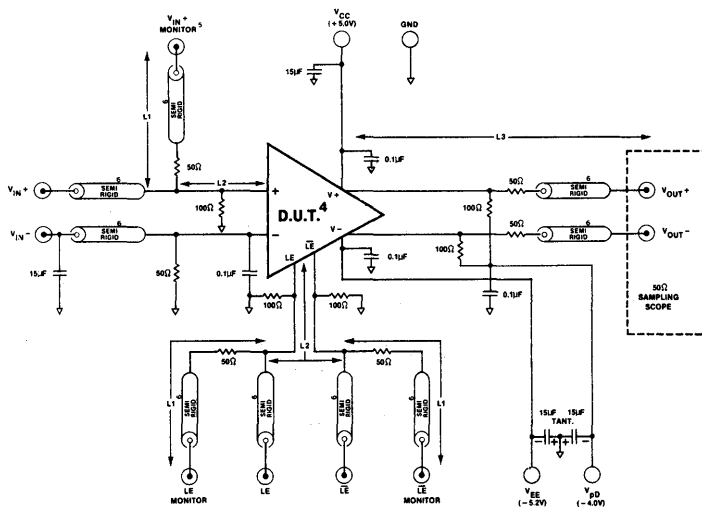
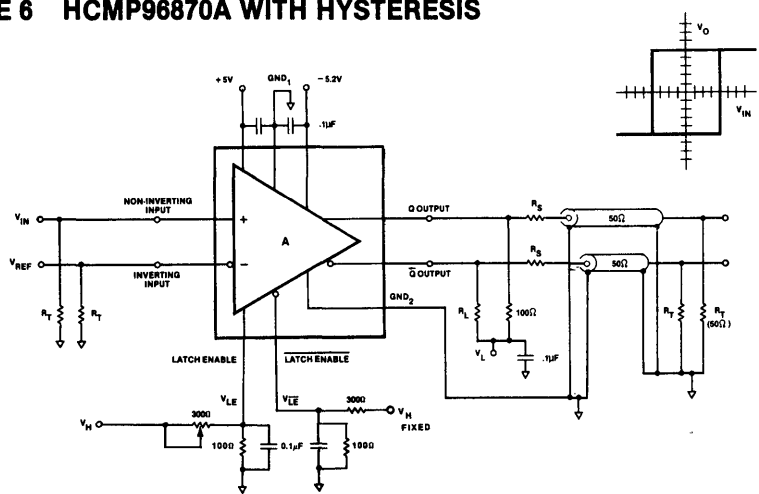


FIGURE 5B AC TEST FIXTURE



- NOTES: 1. ALL BNC & SEMI RIGID COAX SHIELD ARE GROUNDED.
 2. ALL RESISTORS 1% (50Ω = 48Ω).
 3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
 4. D.U.T. PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
 5. MONITOR INPUT IMPEDANCE 50Ω TO GND.
 6. SEMI RIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

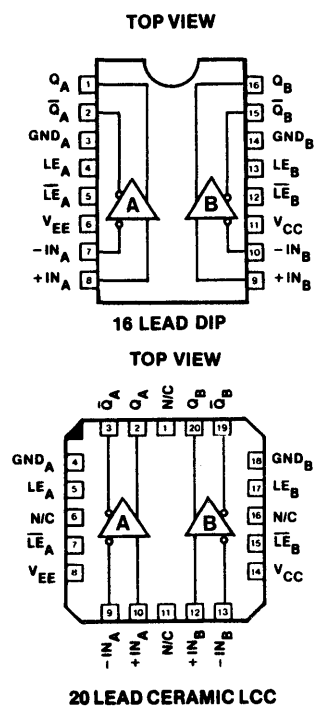
FIGURE 6 HCMP96870A WITH HYSTERESIS



HYSTERESIS IS OBTAINED BY APPLYING A DC BIAS TO THE LE PIN

$V_H = -5.2V$
 $V_{LE} = -1.3V \pm 100mV, V_{LE} = -1.3V$

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
\overline{QA}	Output A
QA	Inverted Output A
GND _A	Ground A
LE _A	Latch Enable A
\overline{LEA}	Inverted Latch Enable A
VEE	Negative Supply Voltage
- IN _A	Inverting Input A
+ IN _A	Non-Inverting Input A
+ IN _B	Non-Inverting Input B
- IN _B	Inverting Input B
VCC	Positive Supply Voltage
\overline{LEB}	Inverted Latch Enable B
LE _B	Latch Enable B
GND _B	Ground B
\overline{QB}	Inverted Output B
QB	Output B

**For Ordering Information See Section 1.

NOTES:

DUAL HIGH SPEED, WIDE VOLTAGE RANGE COMPARATOR

PRELIMINARY INFORMATION

FEATURES:

- Wide Input Range -8 To +13V
- Input Protected to 1V Above Supplies
- Constant Propagation Delays
- High Speed: 5.0ns Propagation Delay
- Linear Input Current

APPLICATIONS:

- ATE Pin Receivers
- Timing Ramp Generators
- Line Receivers
- High Speed Window Detectors

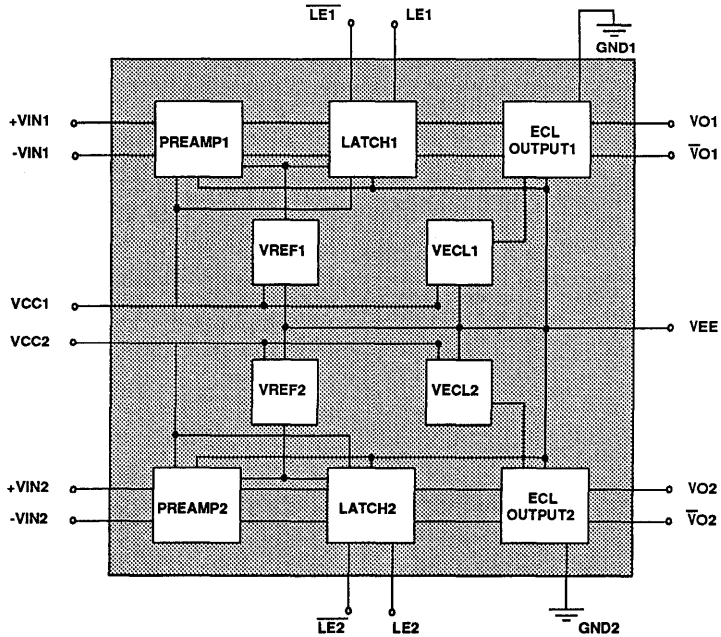
GENERAL DESCRIPTION

The HCMP96900 is a dual, high speed, wide common mode voltage comparator. It is designed for applications measuring critical timing parameters where wide common mode input voltages are required. Propagation delays are constant for varying input slew rates, common mode voltage, overdrive or polarity. Input protection is provided to one volt in excess of the power supplies to ease design of input protection circuitry.

For many applications, the comparator allows the designer to input signals directly into the comparator without the need for either very high speed voltage dividers or buffers. Therefore, designs are easy to protect, high in reliability, and lower in power and space than previous high speed comparators. The device is available in an 18-pin ceramic sidebraced dip, 20 lead LCC or in die form.

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS 25°C (1)

Operating Temperature Range.....-25 to +85°C
 Positive Supply Voltage+18.0V
 Negative Supply Voltage.....- 13.0V

Differential Supply Voltage.....24V
 Input Voltage Range.....VEE -1.0V to VCC +1.0V
 Power Dissipation.....800mW
 Differential Input Voltage.....±24.0V
 Output Current.....40mA

(1) Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

Industrial Temperature Range

V_{CC} = +12.0V, V_{EE} = -7.0V, unless otherwise specified.

DC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C			Hot +85°C			Cold -25°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage		I	-3.0	±0.8	+3.0						mV	
ΔVOS/ΔT		V		20							μV/°C	
Input Offset Current	V _{IN} = 0.0V	I		0.4	1.0						μA	
Input Bias Current	V _{IN} = 0.0V	I		10	20						μA	
ΔIBIAS/ΔV _{IN}	-2V < V _{IN} < +5V	I		0.1	0.3						μA/V	
Input Capacitance	LCC	V		2							pF	
Power Supply Rejection Ratio	ΔV = V _{sup} ± 1/2V	I	75	86							dB	
Common Mode Rejection Ratio	-3V < V _{IN} < +10V	I	80	100							dB	
Input Common Mode Range	See Figure 2	I	-3.0		+10.0						V	
Differential Input Voltage Range	Note 1	I	±13.0								V	
Gain	D.C.	V		60							dB	
Common Mode Input Resistance	-2V < V _{IN} < 5V	I		10							MΩ	
Differential Mode Input Resistance		V		2.5							MΩ	
Input Hysteresis		V		2							mV	
Positive Supply Current		I		28							mA	
Negative Supply Current		I		64							mA	
Power Dissipation		I		0.85							Watts	
Output High Voltage	50Ω to -2.0V	I	-0.98		-0.81						V	
Output Low Voltage	50Ω to -2.0V	I	-1.95		-1.63						V	
Input High Voltage (LE)		I	-1.13		-0.81						V	
Input Low Voltage (LE)		I	-1.95		-1.48						V	

(1) See page 3.

ELECTRICAL SPECIFICATIONS

Industrial Temperature Range

V_{cc} = +12.0V, V_{ee} = -7.0V, unless otherwise specified.

AC Electrical Characteristics	Test Conditions	Test Level (1)	Room +25°C		Hot +85°C		Cold -25°C		Units
			Min	Typ	Max	Min	Typ	Max	
Propagation Delay (w/LE)	100mV Overdrive	I		5.0					ns
Output Rise/Fall Time	20% to 80%	V		1.0					ns
Latch Set-Up Time		I		2.0					ns
Latch Hold Time		I		-1.0					ns
Minimum Latch Pulse Width		I		2.0					ns
t _p with 100mVOD minus t _p with 500mVOD	V _{IN} = +5.0V	V		150					ps
t _p with 100m VOD minus t _p with 500mVOD	V _{IN} = 0V	V		150					ps
t _p with 100m VOD minus t _p with 500mVOD	V _{IN} = -2.0V	V		150					ps

(1) All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level Column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition. Unless otherwise noted, all tests performed after a three minute power soak.

Test Level I - 100% production tested at the specified temperatures.

Test Level II - 100% production tested at T_a = -25°C and sample tested at the specified temperatures.

Test Level III - QA sample tested only at the specified temperatures.

Test Level IV - Parameter is guaranteed (but not tested) by design and characterization data.

Test Level V - Parameter is a typical value for information purposes only.

(2) Propagation delay with 100mV overdrive minus propagation delay with 500mV overdrive.

INPUT

The input of the HCMP96900 is designed to accept wide common mode and differential voltages. With the standard supplies of +12.0V and -7.0V the input voltage range (both common mode and differential) is +10.0V to -3.0V. If a wider or different range is desired, either supply can be changed within the following limits: The positive supply should not exceed +15.0V nor be less than +10.0V. The negative supply should not be greater than -3.3V nor be less than -12.0V. Total differential supply voltage should not exceed 22V. Input voltage range is always VCC -2.0V to VEE +4.0V, and differential input range is equal to the common mode range. (See Figure 2)

PROPAGATION DELAY

Propagation delay has been designed to be as constant as possible with a wide variety of input conditions. For all conditions given below the 25°C deltas in delays are typically 150ps, increasing to a typical 300ps at 85°C ambient. For this reason keeping the devices as cool as possible is desirable. Propagation delay has been designed to be constant, independent of edge direction, common mode voltage, input slew rate (up to 1.5V/ns) or over-drive. Over-drive deltas are specified between 100mV and 500mV because these are the types of values seen in test systems. As the over-drive becomes greater than 500mV, very little change in the delay occurs.

PULSE DETECTION

Digital ATE testing often requires the detection of pulses that are much shorter than the signals that are being measured. This is required to detect glitches in outputs from tested digital products. The HCMP96900 can detect pulses as narrow as 2.0ns in the unlatched mode and still output full ECL swings.

INPUT BIAS CURRENT

High speed comparators are often used as integrators with a current source charging a capacitor on the input.

this circuit is used to generate very fast, accurate timing pulses. The input bias currents of the HCMP96900 have a linear response over the full input voltage range. While this isn't as ideal as no change, it is much better than the nonlinear variations of previous high speed comparators. The change from -3.0V to +10.0V is typically less than 3 μ A.

LATCH ENABLE INPUTS

The timing diagram for the comparators is shown in Figure 1. The latch enable (LE) pulse is shown at the top. If /LE is high and LE low, the comparators track the input difference voltage. When /LE is driven low and LE high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal changes the comparator output after a time of tpdL or tpdH (Q or /Q). The input signal must be maintained for time t_s (set-up time) before the latch enable rising edge and held for time t_h (hold time) after the rising edge for the comparator to accept data. After time t_h, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of tpL is needed for strobe operation, and the output transitions occur after a time of tpLOH or tpLOL.

Unused latch enable pins must be connected to the specified voltages to guarantee proper operation. Latch input bias currents are typically 10 μ A.

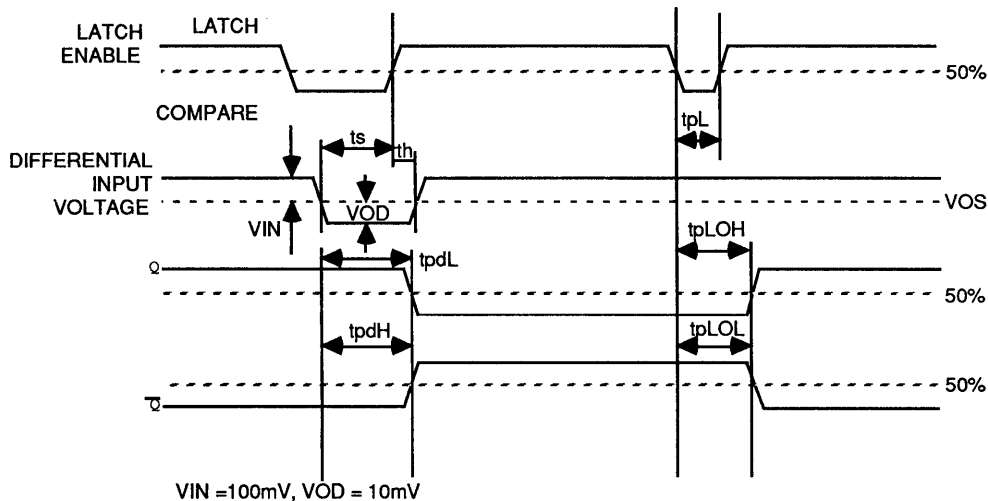
OUTPUTS

The outputs are very high speed differential ECL that are 10KH compatible and capable of driving 50 Ohm loads. The difference between these outputs and the 10KH specifications is that they have much faster rise and fall times. Unused outputs must be terminated with 50 Ω to ground.

USING ONLY ONE COMPARATOR

If it is desirable to use only one comparator of the dual package, the following pins of the unused comparator must be connected to the VEE supply: VIN+, VIN-, LE, /LE, OUT, /OUT, VCC, GND.

FIGURE 1. TIMING DIAGRAM



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry, input signals occurring before t_s will be detected and held; those occurring after t_h will not be detected. Changes between t_s and t_h may not be detected (\overline{LE} is the inverse of LE).

SWITCHING TERMS

tpdH - INPUT TO OUTPUT HIGH DELAY

The propagation delay measured from the time the input signal crossed the input offset voltage to the 50% point of an output LOW to HIGH transition.

tpdL - INPUT TO OUTPUT LOW DELAY

The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

tpLOH - LATCH ENABLE TO OUTPUT HIGH DELAY

The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to 50% point of an output LOW to HIGH transition.

tpLOL - LATCH ENABLE TO OUTPUT LOW DELAY

The propagation delay measured from the 50% point of the Latch Enable signal HIGH to LOW transition to the 50% point of an output HIGH to LOW transition.

ts - MINIMUM SET-UP TIME

The minimum time before the positive transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

th - MINIMUM HOLD TIME

The minimum time after the positive transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

tpL - MINIMUM LATCH ENABLE PULSE WIDTH

The minimum time that the Latch Enable signal must be LOW in order to acquire and hold an input signal change.

VOD - VOLTAGE OVERDRIVE

FIGURE 2. HCMP96900 SUPPLY VOLTAGES INPUT VOLTAGE RANGE

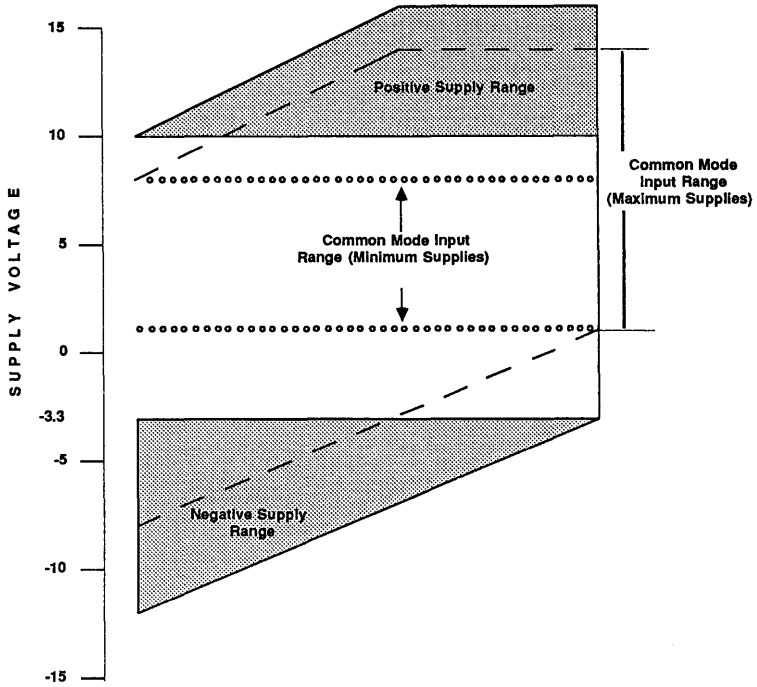
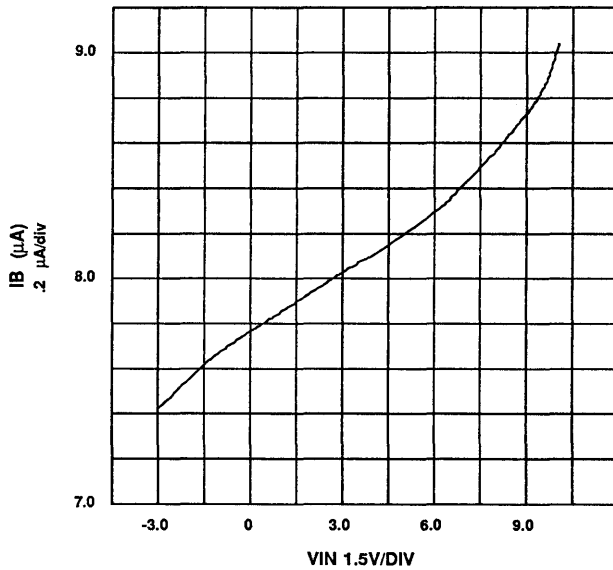
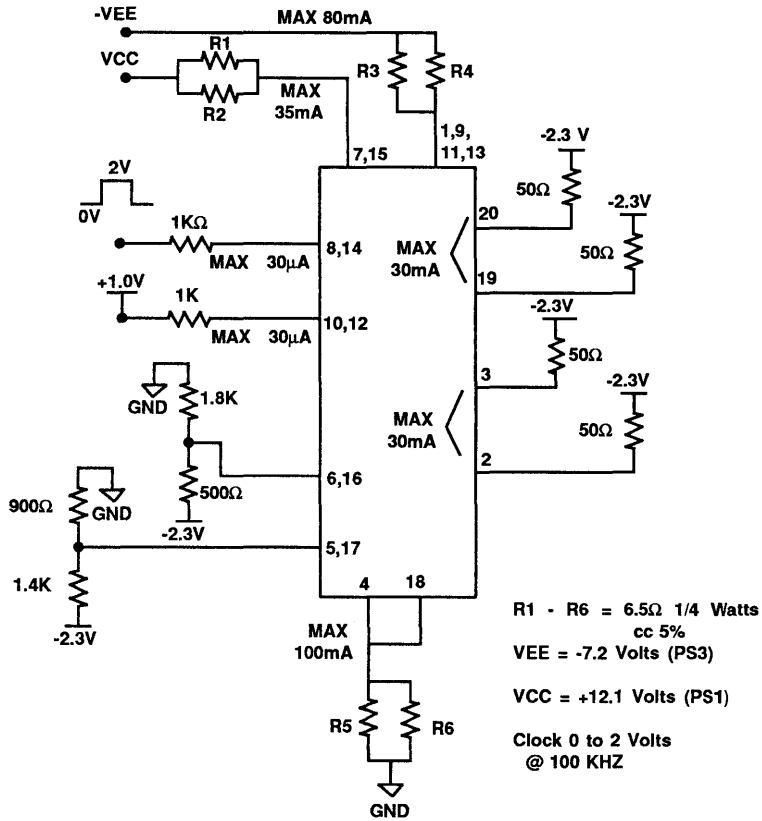


FIGURE 3. HCMP96900 VIN VERSUS IB (Common Mode)



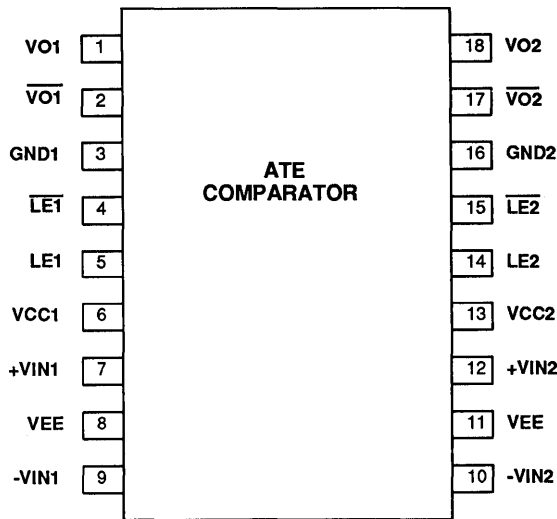
HCMP96900 BURN-IN DIAGRAM (LCC Package)

HCMP96900



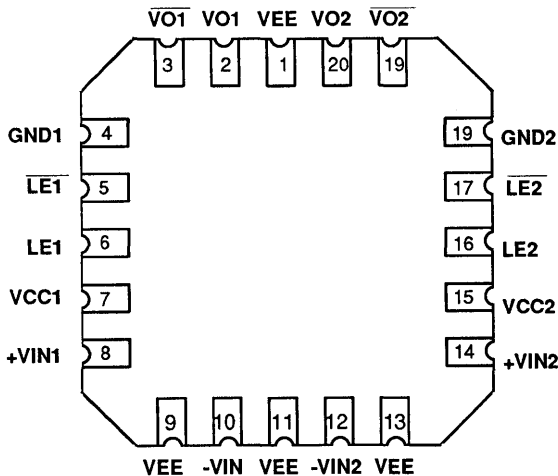
4

HCMP96900 18-PIN DIP PACKAGE



Pins	Description
VO1	Output 1
$\overline{VO1}$	Inverted Output 1
GND1	Ground 1
LE1	Latch Enable 1
$\overline{LE1}$	Inverted Latch Enable 1
VEE	Negative Supply Voltage
-VIN1	Inverting Input 1
+VIN1	Non-inverting Input 1
+VIN2	Non-inverting Input 2
-VIN2	Inverting Input 2
VCC1	Positive Supply Voltage 1
VCC2	Positive Supply Voltage 2
LE2	Latch Enable 2
$\overline{LE2}$	Inverted Latch Enable 2
VO2	Output 2
$\overline{VO2}$	Inverted Output 2
GND2	Ground 2

HCMP96900 20-PIN LCC PACKAGE



**For Ordering Information See Section 1.

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

PROGRAMMABLE 7TH ORDER LOW PASS ACTIVE FILTER

PRELIMINARY INFORMATION

FEATURES

- 85 dB Dynamic Range
- Cut Off Frequency (f_c) up to 20KHz
- On-Chip Anti-Aliasing Protection
- Programmable Bandedge Frequency for both RC and Switched Capacitor Filter
- S/H Output
- Microprocessor Compatible
- 7th Order Ladder Filter with Cosine Prefiltering Stage
- Stopband Attenuation > 76 dB at 3 f_c
- Programmable DC Gains of 1, 2, 4, 8
- On-Chip Oscillator (External Crystal)

APPLICATIONS

- 12-Bit Signal Processing Systems
- Pre-Sample Anti-Alias Filter
- Reconstruction Smoothing Filter
- Test Equipment/Instrumentation
- Spectrum Analyzers
- Medical Telemetry/Filtering
- Speech Analysis and Synthesis
- Data Acquisition Systems
- Computer Controlled Test Systems

GENERAL DESCRIPTION

The HSCF24040 is a monolithic 7th order low pass active filter system. It offers 76 dB of stop-band attenuation and 85 dB of dynamic range which makes it the first switched-capacitor filter suitable for 12-bit systems. Because of the internal 3rd order RC anti-aliasing filter, no external components are required for device operation. Both the RC filter and switched-capacitor filter have digitally programmable cut off frequencies.

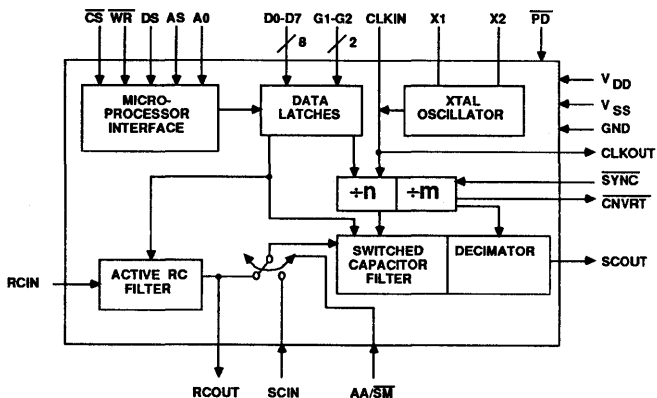
The last stage of the SC filter contains a programmable decimator which provides a sample/hold output function that reduces the sample rate at SCOUT. This ensures

that the hold period of the sampled and held output is long enough to perform an A/D conversion or be re-sampled by an external S/H.

The HSCF24040 is manufactured using Honeywell's state-of-the-art BEMOS process which allows the fabrication of low power CMOS logic, linear CMOS circuits, bipolar linear circuitry and thin film resistors on a single chip. The HSCF24040 is packaged in a 32 pin DIP, operates on a +/- 5V supply voltage and is offered in commercial and military temperature ranges.

5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond Which Damage May Occur) (1)**Supply Voltages**

VDD to GND	0 to +7 V
VSS to GND	0 to -7 V

Output Voltages

Analog Output Voltages	
SCOUT, RCOUT.....	Momentary Short to VDD

Input Voltages**Digital Input Voltages**

All except CLKIN, \overline{CS}	-0.3 V to (VDD + 0.3 V)
CLKIN, \overline{CS}	(VSS - 0.3 V) to (VDD + 0.3 V)

Analog Input Voltages

SCIN, RCIN	(VSS - 0.3 V) to (VDD + 0.3 V)
------------------	--------------------------------

Temperature

Temperature, case	-60 to + 140°C
junction	+ 150°C
Lead Temperature (soldering 10 seconds) ..	+ 300°C
Storage Temperature	-65 to + 150°C

Note (1): Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

RECOMMENDED OPERATING CONDITIONS**Supply Voltages**

VDD	+4.75 to 5.25 V
VSS	- 5.25 to -4.75 V

Temperature

Temperature, Ambient	0 to +70°C
----------------------------	------------

ELECTRICAL SPECIFICATIONS

Test Conditions: VDD = +5V, VSS = -5V, T_A = 0 to 70°C for HSCF24040ACJ, T_A = -55 to +125°C for HSCF24040AMJ, unless otherwise specified. All typical specifications are for T_A = 25°C only.

For explanation of Test Level, refer to Test Level Codes following timing diagrams.

Parameters	Test Conditions	Test Level	HSCF24040			Units
			MIN	TYP	MAX	
DC ELECTRICAL CHARACTERISTICS						
DC Gain of Combined RCF and SCF						
HSCF24040ACJ (0 to 70°C):						
SCF Gain Setting = 1.0	SCBW = 5 kHz RCBW = 7 kHz ↓	I	0.999	1.0	1.001	V/V
SCF Gain Setting = 2.0		I	1.99	2.0	2.01	V/V
SCF Gain Setting = 4.0		I	3.97	4.0	4.03	V/V
SCF Gain Setting = 8.0		I	7.92	8.0	8.08	V/V
HSCF24040AMJ (-55 to +125°C):						
SCF Gain Setting = 1.0		I	0.998	1.0	1.002	V/V
SCF Gain Setting = 2.0		I	1.98	2.0	2.02	V/V
SCF Gain Setting = 4.0		I	3.96	4.0	4.04	V/V
SCF Gain Setting = 8.0		I	7.90	8.0	8.10	V/V
DC Gain of RCF Only		I	0.95		1.05	V/V
DC Gain of SCF Only	SCF Gain Setting = 1.0	I	0.95		1.05	V/V
DC Offset Voltage, Output Referred						
RCOUT		I	-10		+10	mV
SCOUT	SCF Gain Setting = 1.0	I		±10		mV

Parameters	Test Conditions	Test Level	HSCF24040			Units
			MIN	TYP	MAX	
DC ELECTRICAL CHARACTERISTICS (CONTINUED)						
Output Drive Capability, RCOU and SCOU						
Maximum Voltage Swing	RL = 5 k Ω	I	+3.0			V
Minimum Voltage Swing	RL = 5 k Ω	I			-3.0	V
Maximum Sink/Source Current	RL = 5 k Ω	I	600			μ A
Analog Input Voltage Range (1)						
RCIN		I	-3.0		+3.0	V
SCIN; SCF Gain Setting = 1.0		I	-3.0		+3.0	V
SCIN; SCF Gain Setting = 2.0		I	-1.5		+1.5	V
SCIN; SCF Gain Setting = 3.0		I	-0.75		+0.75	V
SCIN; SCF Gain Setting = 4.0		I	-0.375		+0.375	V
Analog Input Impedance						
RCIN Resistance		I	100			k Ω
RCIN Capacitance		I			25	pF
SCIN Resistance		I	50			k Ω
RCIN Capacitance		I			25	pF
Power Supplies						
Operating Current						
IDD; Normal Mode	XTAL Oscillator Active	I		15	20	mA
IDD; Power Down Mode	XTAL Oscillator Active	I		2	4	mA
ISS; Normal Mode	XTAL Oscillator Active	I		15	18	mA
ISS; Power Down Mode	XTAL Oscillator Active	I		1	3	mA
Power Dissipation						
Normal Mode	XTAL Oscillator Active	I		150		mW
Power Down Mode	XTAL Oscillator Active	I		15		mW

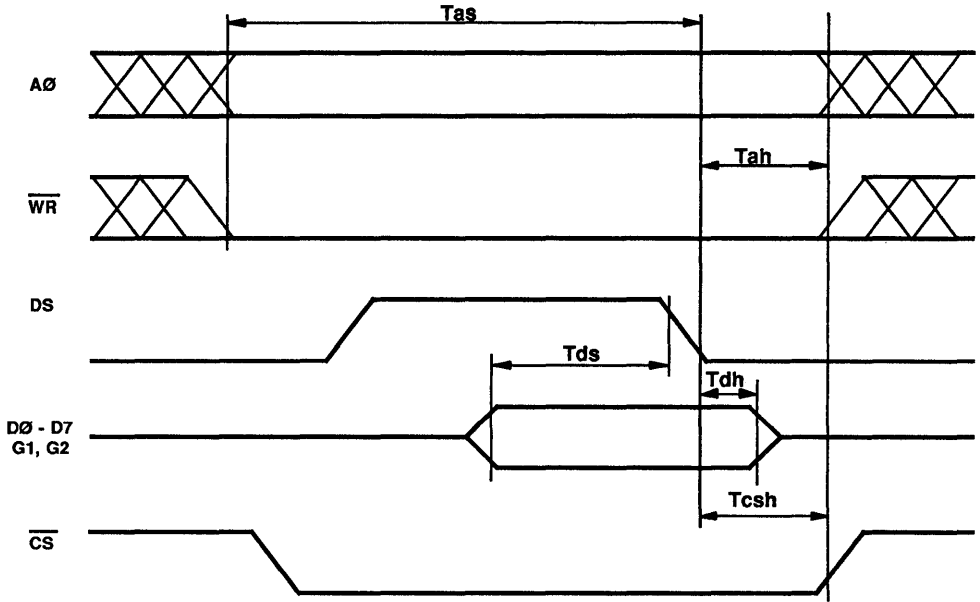
Note (1): Input voltage outside these ranges will degrade harmonic distortion performance.

Parameters	Test Conditions	Test Level	HSCF24040			Units
			MIN	TYP	MAX	
AC ELECTRICAL CHARACTERISTICS						
RC Filter (RL = 5 kΩ, CL = 50 pF)						
Programmable Bandwidth (Fo, -3dB)		I	7		80	KHz
Bandedge Tolerance, Referenced to Fo		I	-0		+5	%
Passband Response, DC to 0.25Fo Referenced to RCF DC Gain		I	-0.1		+0.1	dB
Stopband Loss, Referenced to RCF DC Gain						
0.25Fo		I			0.1	dB
Fo		I	2	3	4	dB
17.25Fo		I	72			dB
Harmonic Distortion, ±3V Sinusoidal Input at RCIN						
Magnitude of Harmonics		II		-80		dB
THD (HSCF24040ACJ)		I		0.01	0.02	%
THD (HSCF24040AMJ)		I		0.01	0.1	%
Dynamic Range		I	85	90		dB
Integrated Noise Voltage, 0.01Fo to 2.0Fo		I		50	70	μV rms
SC Filter (RL = 5 kΩ, CL = 50 pF)						
Programmable Bandwidth (Fc)		I	78		20,000	Hz
Bandedge Tolerance, Referenced to Fc		I	-0.5		+0.5	%
Passband Response, DC to Fc Referenced to SCF DC Gain		I	-0.1		+0.1	dB
Stopband Loss, Referenced to SCF DC Gain						
1.5Fc		I	30			dB
2.0Fc		I	50			dB
2.5Fc		I	66			dB
3.0Fc		I	76			dB
Harmonic Distortion, ±3V Sinusoidal Input at SCIN						
Magnitude of Harmonics		I		-72		dB
THD (HSCF24040ACJ)		I		0.05	0.075	%
THD (HSCF24040AMJ)		I		0.05	0.2	%
Dynamic Range		I	85	90		dB
Integrated Noise Voltage, 0.01Fc to 2.0Fc		I		70	100	μV rms

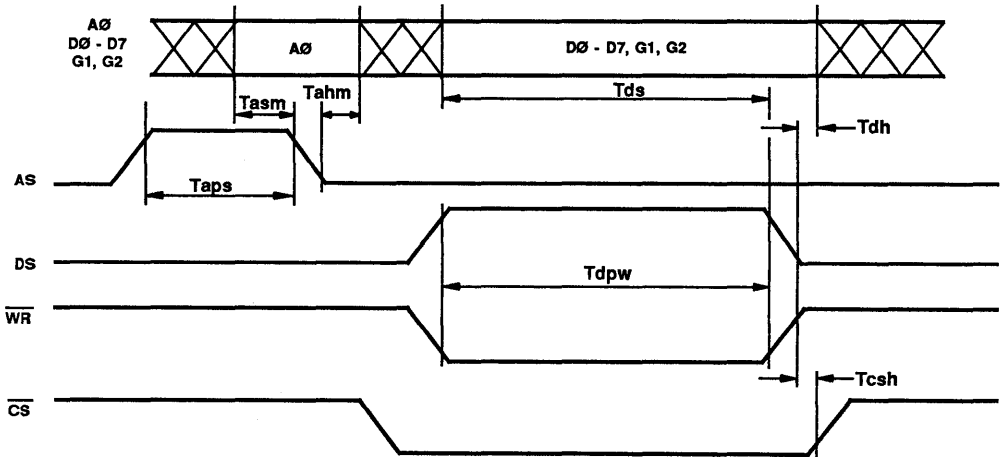
Parameters	Test Conditions	Test Level	HSCF24040			Units
			MIN	TYP	MAX	
AC ELECTRICAL CHARACTERISTICS (CONTINUED)						
Digital Inputs (Pins D0 - D7, G1, G2, $\overline{\text{SYNC}}$, $\overline{\text{CLKIN}}$, $\overline{\text{PD}}$, $\overline{\text{AA/SM}}$, A0, AS, DS, $\overline{\text{CS}}$, $\overline{\text{WR}}$)						
VIH (Input Voltage High)		I	2.0			V
VIL (Input Voltage Low)		I			0.8	V
IIN (Input Current)		I			1.0	μA
CIN (Input Capacitance)		II			10	pF
Digital Outputs (Pins CLKOUT, $\overline{\text{CNVRT}}$)						
VOL (Output Voltage Low)	Driving Standard TTL Load	I			0.4	V
VOH (Output Voltage High)	Driving Standard TTL Load	I	2.4			V
Clock Frequency						
Internal Oscillator Frequency		I	1		4	MHz
Input Clock Frequency		II	(1)		4	MHz
Microprocessor Interface Timing						
Non-Multiplexed Address/Data bus:						
Tas (Address Setup Time)		I	100			nsec
Tah (Address Hold Time)		I	10			nsec
Multiplexed Address/Data bus:						
Tasm (Address Setup Time)		I	20			nsec
Tahm (Address Hold Time)		I	10			nsec
Tds (Data Setup Time)		I	100			nsec
Tdh (Data Hold Time)		I	10			nsec
Tdpw (Data Latch Pulse width, DS or WR)		I	100			nsec
Taps (Address Latch Pulse Width)		I	50			nsec
Tcsh (Chip Select Hold, $\overline{\text{CS}}$ or $\overline{\text{WR}}$)		I	10			nsec
SCOUT Synchronization Timing						
T1 (CLKIN to CLKOUT Delay)		I			50	nsec
T2 ($\overline{\text{SYNC}}$ Delay Time)		I	100			nsec
T3 ($\overline{\text{SYNC}}$ Setup Time)		I	75			nsec
T4 ($\overline{\text{SYNC}}$ Pulse Width)		I	75		(2)	nsec
T5 (CLKIN to $\overline{\text{CNVRT}}$ Delay)		I			75	nsec

- Notes: (1) The minimum input clock frequency is constrained only by the SC filter bandwidth. SC bandwidths below 78 Hz may degrade at high temperatures due to leakage currents.
- (2) It is required that the external $\overline{\text{SYNC}}$ input return to a logic high at least 1 CLKIN clock cycle prior to the falling edge of the next $\overline{\text{CNVRT}}$ output.

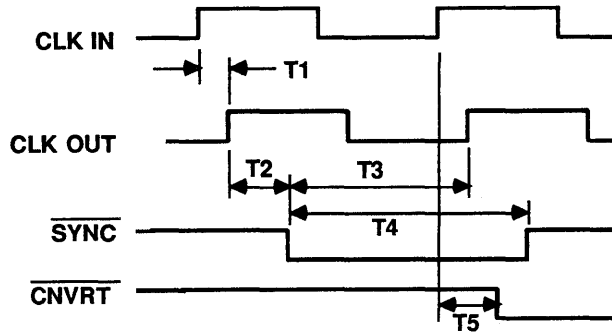
TIMING DIAGRAM FOR NON-MULTIPLEXED BUS



TIMING DIAGRAM FOR MULTIPLEXED BUS



SCOUT SYNCHRONIZATION TIMING



TEST LEVEL CODES

ELECTRICAL CHARACTERISTICS TESTING

TEST LEVEL

TEST PROCEDURE

All electrical characteristics that follow are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank sections in the data columns indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_c = T_a$.

I

Production tested at the specified temperatures.

II

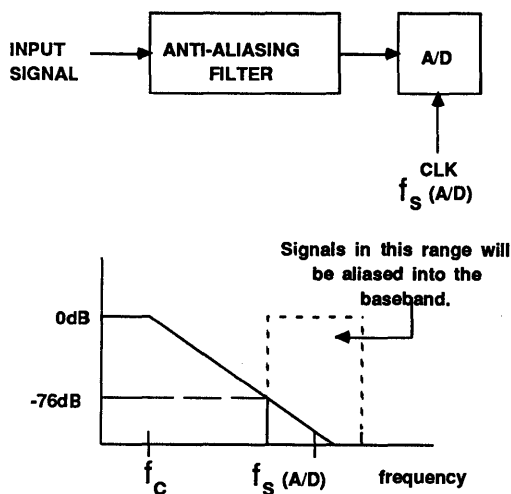
Parameter is guaranteed by design and sampled characterization data.

GENERAL DESCRIPTION

(Please refer to AN109 *EB105 Evaluation Board* and AN111 *Analog/Digital Interface Requirements For The HSC24040*, both found under Applications Information, for additional information.)

SC FILTER

SC filters are sampled data filters that provide extremely accurate and stable responses. This is because their internal "time constants" depend only upon the switching frequency and the ratios of monolithic capacitors. The switching frequency is normally derived from a crystal controlled oscillator and is thus, extremely precise. On-chip capacitor ratios are accurate to within approximately 0.1%. Therefore, high order sharp rolloff filters can be manufactured that require no post production trimming. Since the filter bandedge can be programmed by varying the frequency of the clock that controls the filter's switches, the filter bandedge can be made to track the sample rate of an external A/D converter. The filter in the HSCF24040 has 7 poles (Chebyshev approximation) to insure a minimum loss of 76dB at 3 times the bandedge so that the system A/D can sample as low as 4 times the bandedge (see Figure 1). The SC filter has a differential signal path to improve its PSRR, distortion, and dynamic range. Through digital programming, bandedges of up to 20KHz and DC gains of 1, 2, 4 or 8 can be achieved.

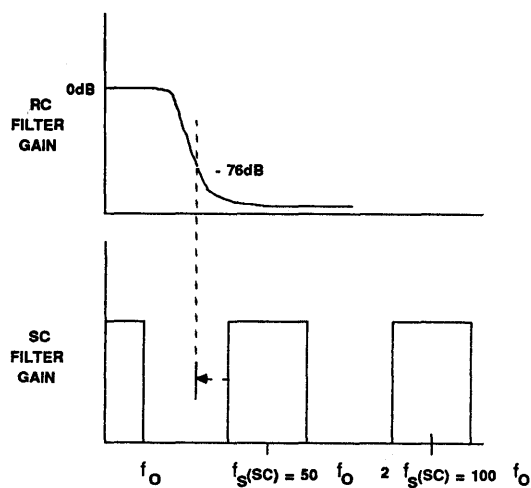


Since the filter loss is greater than 76 dB, any aliased signals will be below the 12 bit level.

FIGURE 1 - REQUIREMENTS FOR AN ANTI-ALIASING FILTER PRIOR TO A/D CONVERSION

ACTIVE RC FILTER

Although the SC filter is programmable and offers excellent performance, it does have one major drawback. Because it is a sampled data filter, it can fold or alias out-of-band energy into the desired passband in much the same way as the external A/D. Therefore, a continuous-time filter is required in front of the SC filter to provide aliasing protection. We are, however, aided by the fact that the filter sampling rate is many times greater than the bandedge frequency (50 times in this case). Thus, a low order, active RC filter with a bandedge accuracy of only 5% will suffice. This concept is illustrated in Figure 2. The bandedge for this RC filter must be programmable to insure sufficient rejection of the SC filter images located at multiples of the SC filter rate. Eight different RC filter bandedges spanning a 12-to-1 range are available on the HSCF24040. The programmability is achieved by switching different resistor and capacitor values into the filter. A single RC filter bandwidth setting (3dB) of $f_o(\text{RCF})$ will provide 76dB of anti-aliasing protection for SC filter bandwidths ranging from $f_o(\text{RCF})/5.71$ to $f_o(\text{RCF})/4$.



Note: The RC filter should provide > 76 dB of loss for several different SC filter sample rates f_s (SC).

FIGURE 2 - RC FILTER PROVIDES ANTI-ALIASING FOR SC FILTER

The topology of the RC filter has been chosen so that the DC gain and the pole Q's rely on ratio matching of the on-chip resistors and capacitors. The RC filter bandedge is laser trimmed for high accuracy during the manufacturing process.

DECIMATOR

The decimator block samples the differential output of the SC filter and converts it to a single ended signal. The decimator also provides a sample-and-hold output (SCOUT) at a programmable sample rate of $25fc$, $12.5fc$, $6.25fc$, or $4.167fc$, where fc is the SC filter bandwidth. By choosing the proper decimation rate, the hold time at SCOUT will be sufficiently long to allow an A/D conversion to take place. (An external sample and hold may be required for hold times longer than $100\mu\text{sec}$ to prevent more than 1/2 LSB of droop for a 12-bit A/D converter).

The $\overline{\text{CNVRT}}$ output is an active low digital output that indicates when the SCOUT output is valid. Applying a falling edge to the $\overline{\text{SYNC}}$ input initiates the $\overline{\text{CNVRT}}$ pulse on the next rising edge of CLKOUT . The use of the decimator block with $\overline{\text{SYNC}}$ and $\overline{\text{CNVRT}}$ insures a proper timing interface between SCOUT and an external A/D converter or sample and hold and eliminates the need for a smoothing filter at the SCOUT output.

PROGRAMMABILITY

The chip contains an 8-bit and a 2-bit data register. Data in the 8-bit register controls the SC filter bandedge, RC

filter bandedge, and the decimation rate. (A programmable divide down chain generates the SC filter clocks from the master clock. A similar divide down chain determines the decimation rate from the SC filter clocks). Data in the 2-bit register controls the programmable D.C. gain of the SC filter. The truth tables for both registers are shown in Table 1.

The SC filter's bandedge is programmed by selecting one of the divide down ratios shown in Table 1. This ratio is divided into the master clock frequency to arrive at the filter cutoff frequency. As an example, assuming a typical master clock frequency of 4 MHz and a divide down ratio of 400 (D0, D1, D2=001), the filter's bandedge would be 10kHz. Alternately, selecting a divide down ratio of 3200 (D0, D1, D2 = 100) would provide a filter bandedge of 1250Hz. With a constant master clock frequency, up to seven (7) different discrete SC filter bandedges can be obtained. An infinite number of different bandedges can be derived by varying both the divide down ratios and the master clock frequency. This provides the ultimate level in programming flexibility.

The five control signals A0, AS, $\overline{\text{WR}}$, $\overline{\text{CS}}$, and DS allow the user to directly interface to 8-bit microprocessors without additional glue logic. Both Motorola's MPX'ed and non-MPX'ed bus formats as well as Intel's MPX'ed bus format is supported. Interface connections for both the Intel and Motorola 8-bit microprocessors are shown in Table 2. In addition to the data-latch format, the D0-D7 and G1-G2 inputs can be hardwired for direct programming without the need for a latch signal by tying the $\overline{\text{CS}}$ input to VSS. A0 = 1 selects the BW registers D0-D7 and A0 = 0 selects the gain registers G1, G2.

TABLE 1 - PROGRAMMABLE FEATURES

<u>RCF BANDEGE</u>				<u>DC GAIN</u>		
<u>RCF 3dB BW</u>	<u>D7</u>	<u>D6</u>	<u>D5</u>	<u>DC GAIN</u>	<u>G1</u>	<u>G2</u>
80KHz	0	0	0	1	1	1
56KHz	0	0	1	2	1	0
40KHz	0	1	0	4	0	1
28KHz	0	1	1	8	0	0
20KHz	1	0	0			
14KHz	1	0	1			
10KHz	1	1	0			
7KHz	1	1	1			

<u>CLOCK TO SCF BANDEGE</u> <u>DIVIDE DOWN RATIO</u>				<u>DECIMATOR SAMPLE RATE</u>		
<u>fCLK/ fC</u>	<u>D0</u>	<u>D1</u>	<u>D2</u>	<u>fS/H/ fC</u>	<u>D3</u>	<u>D4</u>
200	0	0	0	25.000	0	0
400	0	0	1	12.500	0	1
800	0	1	0	6.250	1	0
1,600	0	1	1	4.167	1	1
3,200	1	0	0			
6,400	1	0	1			
12,800	1	1	X			

f_C = 0.1db Bandwidth of the SC filter.

f_{CLK} = Master clock frequency at CLKOUT.

$f_{S/H}$ = Sample rate at SCOUT output.

TABLE 2 - MICROPROCESSOR INTERFACE CONNECTIONS

HSCF24040	INTEL (MPX'ED) 8088, 8085, 8051	MOTOROLA (MPX'ED) 6801, 6803	MOTOROLA (NON-MPX'ED) 680D, 6801, 6802, 6809
\overline{CS}	Generated from A8-A15	Generated from A8-A15	Generated from A0-A15
DS	VDD Supply	E	E
\overline{WR}	\overline{WR}	R/ \overline{WR}	R/ \overline{WR}
A0	ADi	ADi	Ai
AS	ALE	AS	VDD Supply
D0-D7	AD0-AD7	AD0-AD7	D0-D7
G1-G2	ADi	ADi	Di

Note: Tying \overline{CS} to the VSS supply disables the microprocessor interface and allows D0-D7, G1-G2 to be programmed directly without the need for a latch signal.

OSCILLATOR

The HSCF24040 provides an on-chip oscillator (external crystal) for applications where a system clock is not available. The user has a choice of either the clock driven or the oscillator mode. The oscillator mode is enabled by tying the CLKIN input to VSS.

TYPICAL APPLICATION CIRCUIT

Figure 3 illustrates how the HSCF24040 might be used for smoothing the output from a D/A converter. In this case, the D/A output is fed into the SCIN input of the device. The SCIN input is enabled by tying AA/SM to ground. The SCOUT output is fed externally into the RCIN input. The smoothed output is finally brought off-chip via the RCOUT pin. (Note that the smoothed output will not correct for the inherent sin(X)/(X) droop of the original D/A converter output).

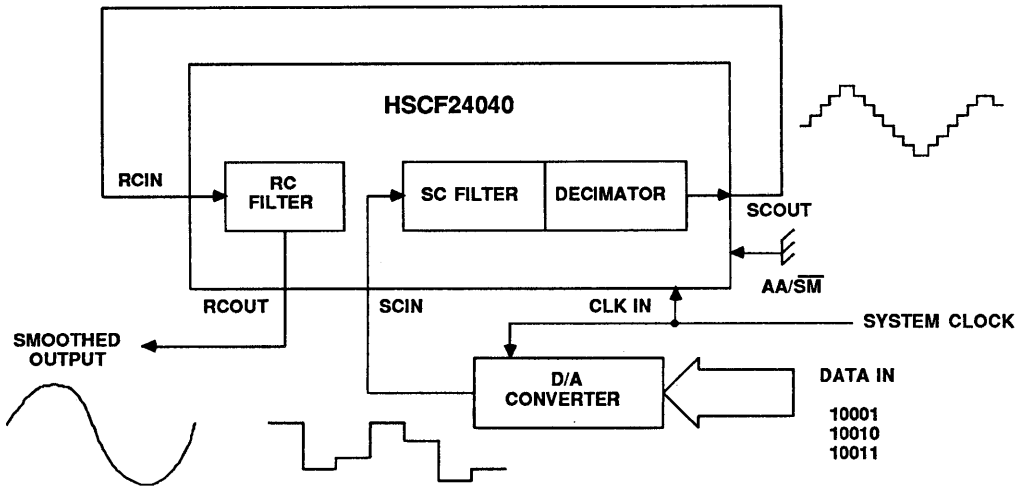


FIGURE 3 - THE HSCF24040 AS A SMOOTHING FILTER FOR A D/A CONVERTER

TYPICAL APPLICATION CIRCUIT

The HSCF24040 can be used as the band limiting filter for a 12-bit data acquisition system as shown in Figure 4. The basic function of the device is to bandlimit the input signal so that unwanted out-of-band signals are not aliased (folded) into the desired passband. The input signal enters the HSCF24040 through RCIN and is processed by the RC filter. The signal is then processed by the switched-capacitor filter and finally the decimator to facilitate its interface with the A/D converter. Figure 1 shows that for a 12-bit system the filter must provide at least 76dB of loss at the frequency $f_s - f_c$ (where f_s is the sampling rate of the A/D converter and f_c is the desired channel bandwidth).

In many applications the user may want a programmable channel bandwidth. An instrument that records signals that range from 100Hz to 20kHz would require that the A/D sample rate be variable. Figure 1 shows that the required filter bandwidth is directly proportional to the sample rate of the A/D converter. The filtering necessary for multiple sampling rates can be accomplished by using the programmable bandwidth capability of the HSCF24040 to adjust the desired filter response to the sample rate. This eliminates the need for a parallel bank of fixed bandwidth anti-aliasing filters, one for each sample rate.

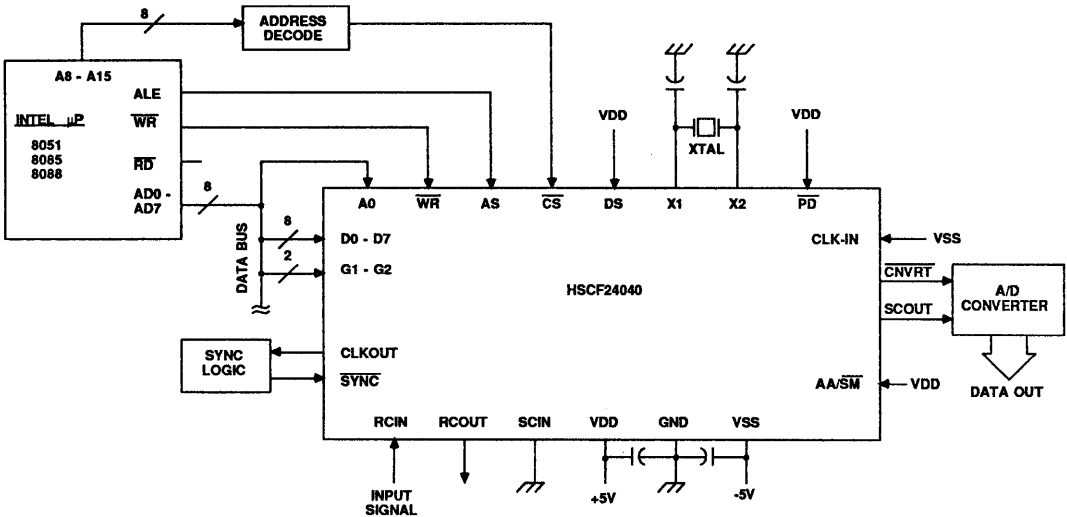


FIGURE 4 - THE HSCF24040 AS AN ANTI-ALIASING FILTER IN A 12-BIT DATA ACQUISITION SYSTEM

TOP VIEW



NAME	FUNCTION
VSS	Negative supply voltage
\overline{CS}	Chip select; active low
G1 - G2	The digital inputs that control the DC gain of the SC filter
D0 - D7	The digital inputs that control the RC filter bandedge, SC filter bandedge, and SC filter decimation rate
\overline{SYNC}	This digital input controls the sampling instant for the SC filter decimated output; active low
CLKOUT	Master clock output capable of driving 1 standard TTL load. It is a buffered version of either CLKIN or the internally generated crystal oscillator output.
VDD	Positive supply voltage
\overline{CNVRT}	This digital output indicates that the SCOUT output has settled and can now be converted or sampled (drive capability is 1 standard TTL load); active low
X1-X2	An external crystal is connected between these pins to generate an accurate clock for chip operation
CLKIN	The master clock input. Forcing CLKIN to VSS enables the on-chip oscillator (external crystal).
GND	Ground
SCOUT	SC filter output
\overline{PD}	This digital input is used to power down the analog circuitry; active low
RCOUT	RC filter output
RCIN	RC filter input
SCIN	SC filter input (only valid when AA/ \overline{SM} is forced low)
\overline{WR}	Write strobe; active low
DS	Data strobe
AA/ \overline{SM}	This digital input controls whether the input to the SC filter comes from RCOUT or SCIN
AS	Address strobe
A0	Register address select

**For Ordering Information See Section 1.

NOTES:

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

DASP-HDSP66110

Digital Array Signal Processor

PAC-HDSP66210

Programmable Array Processor

TABLE OF CONTENTS

SECTION	PAGE NO.
1.0 INTRODUCTION	6-4
1.1 DASP/PAC Chip Set	6-4
1.2 Benchmarks	6-5
2.0 DASP (HDSP66110)	6-7
2.1 DASP: Architecture	6-8
2.2 DASP: Input/Output	6-9
2.3 DASP: Function Set	6-10
2.4 DASP: Block Floating Point Arithmetic	6-10
3.0 PAC (HDSP66210)	6-12
3.1 PAC: Address Sequences and Memory Control	6-12
3.2 PAC: Control Registers	6-14
3.3 PAC: Instruction Memory	6-14
3.4 PAC: Initialization	6-15
3.5 PAC: Clock Schemes	6-15
4.0 SYSTEM ARCHITECTURES	6-16
4.1 Recursive Architecture: Dual Memory	6-16
4.2 Recursive Architecture: Dual Memory, I/O Buffered	6-17
4.3 Recursive Architecture: Single Memory	6-17
4.4 Cascaded Architecture	6-18
4.5 FFT Systems	6-19
4.6 Fast Convolution and Digital Filtering	6-20
4.7 Digital Filter System	6-20
5.0 NUMERIC PERFORMANCE	6-22
6.0 TEST FEATURES AND RELIABILITY	6-22
7.0 SPECIFICATIONS	6-22
7.1 DASP (HDSP66110)	6-22
7.2 PAC (HDSP66210)	6-22
8.0 SYSTEM DEVELOPMENT SUPPORT TOOLS	6-22
8.1 User's Guides and Application Notes	6-22
8.2 Software Simulator	6-30
8.3 Hardware Evaluation Module (EVM)	6-31

1.0 INTRODUCTION

Honeywell's HDSP66 device family is a new generation of digital signal processing (DSP) VLSI integrated circuits targeted for high performance military and commercial applications. Honeywell is a proven leader in very high performance integrated circuit technology which includes a variety of CMOS, GaAs, Bipolar and BEMOS (Bipolar Enhanced CMOS) semiconductor processes. Several Honeywell products, based on one micron class technologies, have been in production for several years. In addition, an extensive amount of research is being conducted in sub-micron VLSI technologies.

The HDSP66 family of DSP devices is produced by combining innovative architectures with high performance, production-proven processes. This combination yields extremely powerful devices which provide great advantages in terms of speed, flexibility, power dissipation, level of integration and cost.

1.1 DASP and PAC Chip Set

The Digital Array Signal Processor (DASP) (HDSP66110) and the Programmable Array Controller (PAC) (HDSP66210) are the first 1.2 micron CMOS chip set in the HDSP66 family. These devices are optimized for DSP applications based upon the Fast Fourier Transform (FFT) algorithm [References 1, 2, 3]. The DASP and the PAC implement DSP systems which process data rates up to 100 MHz in real time and perform Discrete Fourier Transforms, spectrum analysis, digital filters, correlations, convolutions and adaptive filters based upon FFT techniques. Generally, it is easier and more efficient to process signals in the frequency domain than the time domain [Reference 1 (p.110), Reference 2 (p. 198), Reference 3 (p.635 and p.889), Reference 4].

The DASP and the PAC chips use a new architectural approach that allows for a variety of FFT based DSP system configurations. The resulting systems require only 10 to 20 PAC instructions and little hardware yet perform at rates five to 50 times faster than other present solutions. Some of the applications of the DASP and the PAC are listed in Table 1. Additional applications of the DASP chip, beyond DSP, such as graphics processing, are possible due to the inclusion of general purpose functions on the DASP.

The DASP chip performs about 500 million arithmetic operations (16 bits or more) per second and operates at an I/O rate of about 5 billion bits per second. An operation is defined to be a multiply, add or equivalent operation. Unlike traditional DSP microprocessors, the DASP processes arrays of data values rather than single

TABLE 1: APPLICATION AREAS

- Medical Electronics
- High End Instrumentation
- Robotics
- Radar
- Graphics Systems
- Sonar
- Telemetry
- Electronic Warfare
- Electronic Counter Measures
- Navigation and Guidance
- Very-High-Speed Modems
- Satellite Telecommunications
- Image Processing
- Transmultiplexers
- Spread Spectrum Communications
- Digital Radio

data values. The DASP is capable of performing functions, composed of multiple arithmetic operations, on two sets of four complex values or two sets of eight real values every machine cycle (80 nanoseconds). A variety of general purpose and FFT specific functions are supported.

The Programmable Array Controller (PAC) can be used as a companion device to the DASP in FFT based DSP systems. Stand-alone DSP systems, as shown in Figure 1, can be designed by combining the DASP and the PAC with off-the-shelf single-port memories. The PAC is responsible for managing the complete system, based upon the program downloaded to its program memory during initialization. The programmability of PAC makes it applicable in various hardware and algorithmic configurations. The program, typically 10 to 20 instructions, defines the algorithm to be executed on the DSP system (e.g., spectrum analysis, digital filtering, etc.). DSP microprocessors, on the other hand, usually require hundreds or thousands of instructions.

1.2 Benchmarks

The ability to define an algorithm and various hardware configurations in the PAC allows the chip set extreme versatility in a variety of applications. The system performance can be balanced against the hardware cost by choosing the number of DASP/PAC stages and the number of memory devices in a given system. An extremely high performance DSP system can be designed by cascading multiple DASP/PAC stages. A mid-performance system can be designed by using dual memory sets around one DASP/PAC stage. A lower performance system can be based upon one memory set and one DASP/PAC stage. The benchmarks, for various sized FFT's on different system configurations, are shown in Table 2. Some

benchmarks for digital filters (fast convolution), implemented via the frequency domain, are given in Table 3. It is assumed that the incoming data frames overlap by 50%. The amount of data frame overlap is programmed into the PAC by the user. Table 3 illustrates the efficiency of using frequency domain techniques for digital filtering when the number of points in the frequency response of the filter is large. In the time domain, for example, over 350, 100-nS multiplier/accumulators are necessary to implement a 2048 pole digital filter. This can be achieved in the frequency domain with a single DASP/PAC recursive stage.

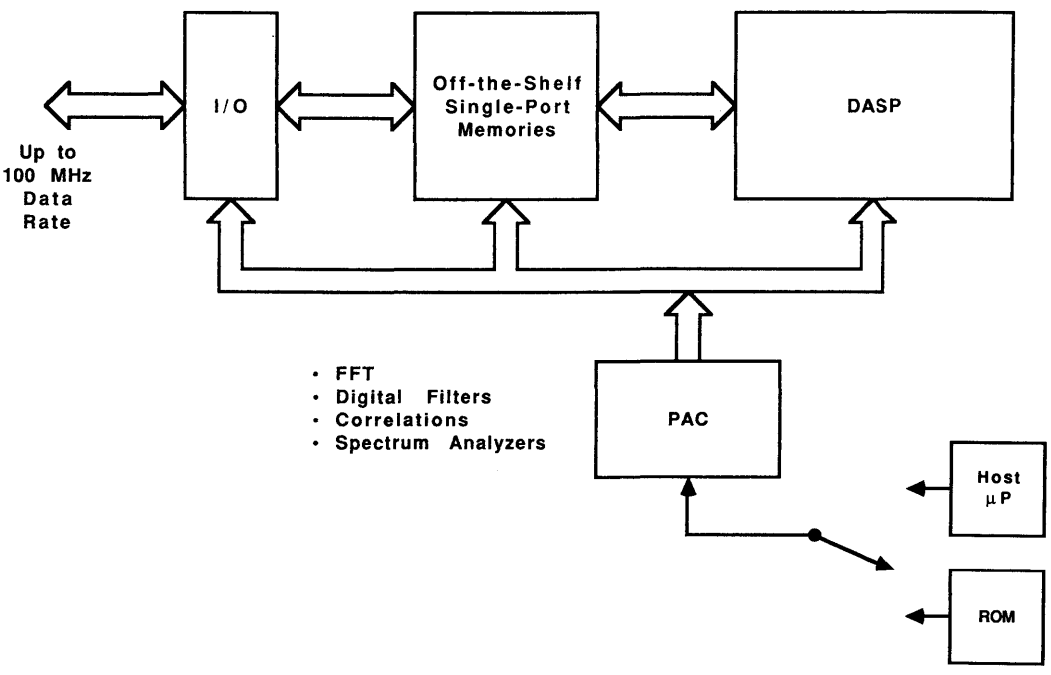


FIGURE 1: DASP/PAC BASED DSP SYSTEM

TABLE 2: FFT BENCHMARKS

NUMBER OF POINTS	SYSTEM TYPE		
	CASCADED MULTIPLE STAGES	DUAL MEMORY RECURSIVE (ONE STAGE)	ONE MEMORY RECURSIVE (ONE STAGE)
64 Real	880 nS (4 Stages)	3.52 μ S	10.56 μ S
64 Complex	1.76 μ S (3 Stages)	5.28 μ S	10.56 μ S
512 Real	5.36 μ S (6 Stages)	32.16 μ S	107.2 μ S
512 Complex	10.72 μ S (5 Stages)	53.6 μ S	107.2 μ S
1024 Real	10.48 μ S (6 Stages)	62.88 μ S	209.6 μ S
1024 Complex	20.96 μ S (5 Stages)	104.8 μ S	209.6 μ S
64K Real	0.65 mS (9 Stages)	5.85 mS	20.96 mS
64K Complex	1.31 mS (8 Stages)	10.48 mS	20.96 mS

TABLE 3: DIGITAL FILTER BENCHMARKS (50% OVERLAP)

NUMBER OF POINTS IN IMPULSE RESPONSE OF FILTER	INPUT COMPLEX DATA RATES	
	CASCADED SYSTEM (MULTIPLE STAGES)	DUAL MEMORY RECURSIVE SYSTEM (ONE STAGE)
32	25 MHz (7 Stages)	3.57 MHz
128	25 MHz (9 Stages)	2.78 MHz
512	25 MHz (11 Stages)	2.27 MHz
2048	25 MHz (13 Stages)	1.92 MHz

2.0 DASP (HDSP66110)

The DASP is a very-high-speed, block floating-point array processor that is capable of performing FFT specific and general purpose operations on arrays of data. The key features of the DASP are shown in Table 4.

TABLE 4: DASP KEY FEATURES

- Arithmetic throughput up to 500 million operations per second.
- Data I/O rate up to 5 billion bits per second.
- 16 FFT-specific and general purpose functions.
- 16/20 bit fixed point arithmetic with block floating point support for FFT functions.
- 16 bit parallel I/O buses to support static RAMs.
- Two interface options (Dual, Quad) for system trade-offs.
- 1.2 micron CMOS; typical dissipation – 2 watts.
- 269 pin ceramic PGA package.
- Performance examples:
 - Radix-4 Butterfly – 80 nS
 - Radix-2 Butterfly – 40 nS
 - Complex Multiply – 20 nS
 - Real Multiply – 10 nS
 - ALU Operation – 10 nS

2.1 DASP: Architecture

The DASP is capable of processing sixteen, 16-bit real values (or 8 complex values), and producing eight, 16-bit real values (or 4 complex values) every machine cycle (Tm). The lower limit on Tm is specified at 80 nano seconds. The block diagram of the DASP below (Figure 2) shows the internal data paths and input/output values. All input/output values are transferred every machine cycle. These values, designated as r0...r3, i0...i3, form the input data that is fed to the DASP every machine cycle. In complex arithmetic instructions (such as FFT), these values represent a set of 4 complex numbers: (r0, i0), (r1, i1), (r2, i2), (r3, i3). Another set of eight 16-bit input operands, which is called auxiliary data, is designated as c0...c3, s0...s3. In complex arithmetic instructions, these values are complex numbers [(c0, s0), (c1, s1), (c2, s2), (c3, s3)] representing auxiliary data values such as window coefficients or trigonometric coefficients. After operating upon the input operands, the device produces a set of eight 16-bit values that are termed x0...x3, y0...y3. Once again, these values represent a set of four complex numbers [(x0, y0), (x1, y1), (x2, y2), (x3, y3)] for complex arithmetic instructions. In summary, there are three I/O ports (input data, input auxiliary data and output data) on the DASP for data transfers.

First, the input data set is passed through an array of complementers to perform conjugating or complementing, if so desired. Then, the values are

passed through an array of adders which can allow data to grow to 18-bits without producing an overflow. These adders are used to perform pre-multiplication additions associated with the Decimation-In-Frequency (DIF) FFT Butterfly operations. The added values are right shifted, if so desired, then rounded to 16-bits and fed to an array of multipliers. At this stage, the multiplier array also receives a scaled set of values from the input auxiliary data port. After multiplications, the 20 most significant bits of each resulting product are retained. Next, the 20-bit product values are operated upon by the ALU array. These ALU's are used to perform post-multiplication additions associated with the complex multiplications. These ALU's can also perform general purpose arithmetic and logical operations. The 20-bit output values from the ALU's are rounded to 16-bits. These values could be complemented or conjugated, if necessary. The final values, which are fed to the data output port, are also monitored by the on-chip scale-factor generator to implement the block floating point arithmetic (discussed later). The data path operation is controlled by a function code which is externally applied. After setting up a function code, the sets of I/O values can be continuously passed through the DASP (one set every machine cycle, Tm). The DASP introduces a latency of four machine cycles from the data-inputs/auxiliary-data-inputs to the outputs. The impact of latency is virtually insignificant since the DASP primarily deals with data-arrays and a given function is typically applied to the whole array.

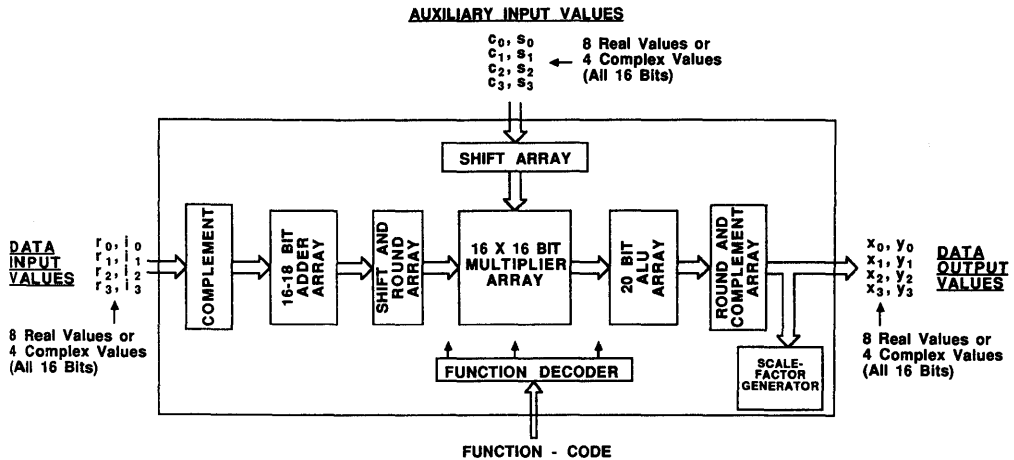


FIGURE 2: DASP BLOCK DIAGRAM AND I/O VALUES

2.2 DASP: Input/Output

Transferring the data in period T_m , as mentioned above, poses a challenge for the system architectural design. Therefore, two input/output modes have been devised for the DASP which offer trade-offs to the user. One of the modes, which is called the DUAL bus mode, is shown in Figure 3. In this scheme, each I/O port is served by two 16-bit parallel buses and transfers 8 values at intervals of T_m . Each bus, therefore, transfers a value at intervals of $T_m/4$. A clock signal at a frequency of $4/T_m$ is required to manage the DASP in the DUAL mode. The application of the DUAL bus DASP results in a simple system architecture since off-the-shelf single port memories can be used to serve each bus on the DASP. Also, the DASP input and output data ports (D1/D2, D3/D4) are bi-directional in the DUAL mode. This means that the roles of buses D1/D2 and D3/D4 can be interchanged. During a given data pass, the input data values could be fed through the D1/D2 ports and outputs produced on the D3/D4 ports (Figure 3). On the next pass, the inputs could be fed through the D3/D4 ports and outputs produced on the D1/D2 ports. As discussed later in the system applications section, the bi-directionality feature of the data ports makes the design of recursive systems very simple.

Another I/O scheme, which is shown in Figure 4, is called the QUAD bus mode and is chosen by applying a high level on the QUAD pin of the DASP. In this mode, there are four buses associated with each port of the DASP. Therefore, each bus is operated at intervals of $T_m/2$, requiring an input clock to the DASP at a frequency of $2/T_m$. In the QUAD mode, the access time on external memories is relaxed. However, the memory architecture will generally be more complicated compared to the DUAL I/O mode. In the majority of applications, four port memories are required to feed each of the three ports. In addition, the data I/O buses (D1/D2/D5/D6, D3/D4/D7/D8) are not bi-directional in the QUAD mode causing some inconvenience in the recursive system designs.

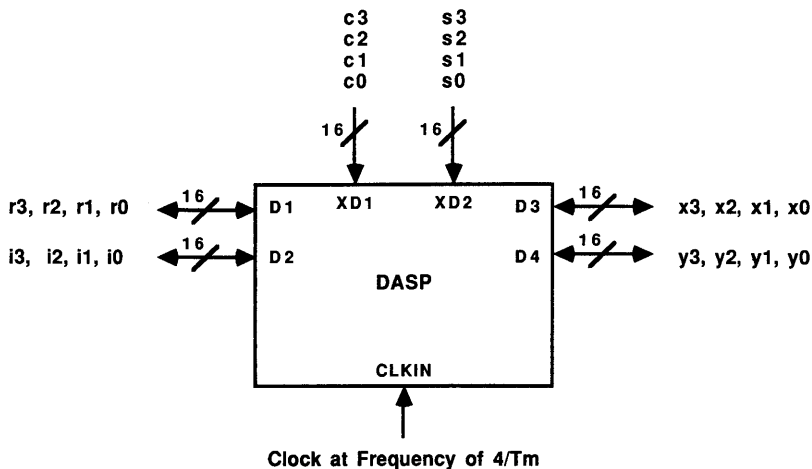


FIGURE 3: DASP DUAL BUS MODE

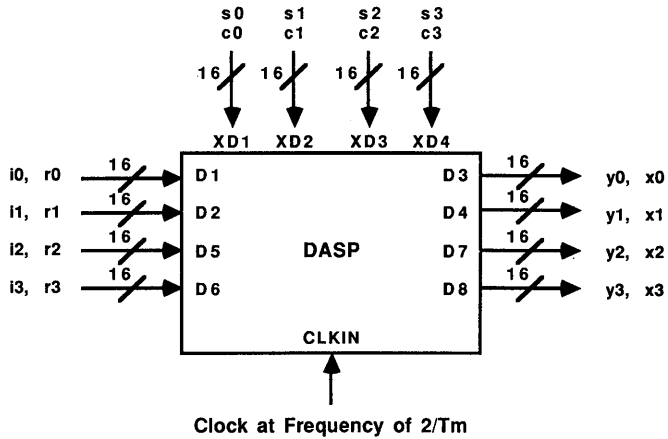


FIGURE 4: DASP QUAD BUS OPTION

2.3 DASP: Function Set

A total of 16 functions are supported on DASP (listed in Table 5). Note that the DASP is capable of implementing one function every machine cycle (period T_m). The function-code on pins FC(5:0) must be set up one machine cycle ahead of feeding the data to the processor. In typical array processing applications, such as FFT's, a function code is set up (e.g., BFLY4); then, the whole data array is clocked through the processor. The applied function will be, therefore, implemented on the whole array. As mentioned earlier, there is a latency of four machine cycles in implementing each function on the DASP.

The complex arithmetic functions support FFT processing (Table 5). The BFLY4 and BFLY2 functions can be used to implement radix-4, radix-2 or mixed-radix-4/radix-2 FFT algorithms. The functions FFTNN and FFT2N are useful for performing FFT's on real data [Reference 2 (p.166, 167)]. The FFTNN function can be used to process two frames of real-data simultaneously and obtain almost twice the performance of complex data FFT's. The BMUL function can be used to perform windowing on the input data or for general purpose complex multiplications encountered in demodulation processes. The general purpose functions, listed in Table 5, can be used to implement various arithmetic operations on real and complex data. The function BSQSM can be used to determine the magnitude-squared of the frequency spectrum for FFT applications. The general logic functions in Table 5 are useful for performing logic operations on arrays of data.

There are provisions, useful for implementing inverse-FFT's, to conjugate the inputs to, and the outputs from, the complex arithmetic functions. Similarly, the input and output data values can be complemented for the general arithmetic and logical functions. In addition, the input values can be shifted for all functions. These facilities lead to higher computational efficiency.

2.4 DASP: Block Floating Point Arithmetic

Primarily, the input and output values associated with the DASP are 16-bit fixed-point and are represented in 2's complement arithmetic (for arithmetic functions). However, on-chip intermediate values can grow to 20 bits but are rounded to 16 bits before they are transferred to the output buses. The growth in the number of bits helps to preserve an adequate signal-to-noise ratio. Still, there could be a severe loss in the signal-to-noise ratio on fixed-point arithmetic machines due to scaling, which is normally applied to prevent overflow. The block floating point scheme (Figure 5), which applies data dependent scaling, boosts the signal to noise ratio by extending the dynamic range of the fixed point arithmetic. When a BFLY4 or BFLY2 is implemented on the DASP, the magnitude of the values being produced at the output are monitored. After a complete pass through the data-array, the DASP produces a scale factor at the pins SFO(2:0) to scale the data on the next BFLY4/BFLY2 pass and prevent overflow. The scale factor is automatically applied to the input when the SFO output pins are tied to the

TABLE 5: DASP FUNCTIONS

FUNCTION MNEMONIC	DESCRIPTION	NO. OF INPUT DATA VALUES	NUMBER OF INPUT AUX. DATA VALUES	NUMBER OF OUTPUT DATA VALUES
COMPLEX ARITHMETIC CLASS				
BFLY4	Radix-4 Decimation-In-Frequency Butterfly	4 Complex	4 Complex	4 Complex
BFLY2	Two Radix-2 Decimation-In-Frequency Butterflies	4 Complex	4 Complex	4 Complex
FFTNN	Recombine N Complex-Point FFT to Two N Real Point FFTs	4 Complex	X	4 Complex
FFT2N	Recombine N Complex-Point FFT to 2N Real Point FFT	4 Complex	1 Complex	1 Complex
BMUL	Block Multiply Two Sets of Complex Numbers	4 Complex	4 Complex	4 Complex
GENERAL ARITHMETIC CLASS				
AFLOW	Arithmetic Flow Through: Pass Data	4 Complex or 8 Real	X	4 Complex or 8 Real
BMULR	Block-Multiply Two Sets of Real Numbers	8 Real	8 Real	8 Real
BMULRA	Block-Multiply Two Sets of Real Numbers and Partially-Add	8 Real	8 Real	4 Real
BSQSM	Block Square and Sum a Set of Values	4 Complex or 8 Real	X	4 Real
BADD	Block - Add Two Sets of Values	4 Complex or 8 Real	4 Complex or 8 Real	4 Complex or 8 Real
BSUB	Block - Subtract Two Sets of Values	4 Complex or 8 Real	4 Complex or 8 Real	4 Complex or 8 Real
GENERAL LOGIC CLASS				
LFLOW	Logical Flow Through: Pass Data	8 Logical	X	8 Logical
BAND	Block-AND Two Sets of Values	8 Logical	8 Logical	8 Logical
BOR	Block-OR Two Sets of Values	8 Logical	8 Logical	8 Logical
BXOR	Block-XOR Two Sets of Values	8 Logical	8 Logical	8 Logical
BCONS	Generate Block of Logical Constants at the Outputs (Zeros or Ones)	X	X	8 Logical

DSP

6

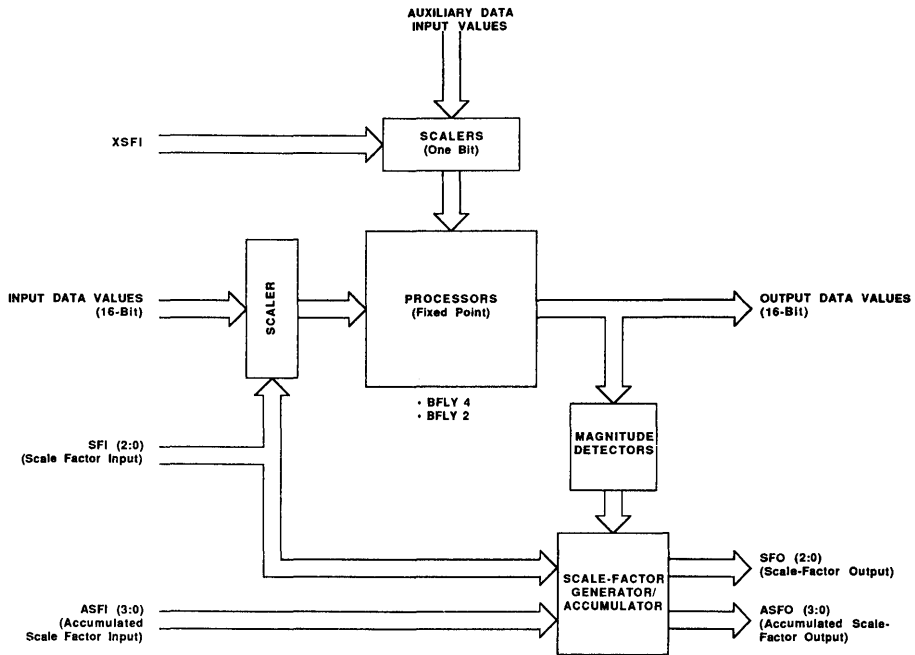


FIGURE 5: DASP BLOCK FLOATING SCHEME

corresponding SFI input pins of the same or of another DASP device (Figure 5). The DASP is also capable of accumulating various scale factors that may be applied by the processor at various stages of the algorithm. The accumulated scale factor is produced on the ASFO(3:0) pins. The ASFO from the final pass can be used to normalize the final processed data array.

3.0 PAC (HDSP66210)

The Programmable Array Controller (PAC) combined with the DASP forms a compact, complete DSP system solution. The PAC provides addressing and control for the memories and other elements in the system. The key features of the PAC are listed in Table 6 and a block diagram is shown in Figure 6.

3.1 PAC: Address Sequences and Memory Control

The core of the PAC is the five address generators: IAS, OAS, RAS, WAS and XAS. These address generators encompass all addressing sequences which are necessary to implement various FFT-based DSP

systems. The IAS and OAS generate address sequences for the input data collection memory and the output data dump memory. The RAS and WAS generate address sequences for the DASP read memory and the DASP write memory. The XAS sequencer addresses the auxiliary (coefficient) data memory. Each address generator outputs a new address every micro cycle ($T_m/4$) to support the I/O rate of the DASP. Therefore, five 16-bit addresses are generated every micro cycle on the external PAC address buses designated as ADRA, ADRB, ADRC, ADRD and ADRX. These address buses can control five distinct memories called A, B, C, D and X. The PAC provides full control of these memories by producing corresponding write strobes.

Typically, the address on each bus is used to address a pair of memories which hold Real and Imaginary data, respectively. Each memory pair will be assigned to one of the three DASP I/O ports, the input data collection buffer or the output data buffer. The PAC functions extremely well with the DUAL mode DASP and requires minimal external hardware. When the PAC is used with the QUAD mode DASP, the addresses from the PAC

TABLE 6: PAC KEY FEATURES

- Provides total system control and addressing for FFT-based DSP systems (Controls, I/O, Memories and DASP).
- Supports up to 64K point data frames (16-bit address buses).
- 32-word internal instruction memory to define user's algorithm (one instruction needed per pass).
- Optional external instruction memory space (unlimited).
- Generates various addressing sequences for FFT based applications on 5 address buses every micro cycle ($T_m/4$).
- On-chip multiplexers for assigning desired address sequences to the desired output ports.
- Compensates for pipeline latencies in the external memories.
- Control registers to define various parameters and hardware features of the system.
- Initialization by a host or by an autoboot from a ROM.
- Synchronization capability for multiple DASP and PAC devices.
- 1.2 micron CMOS process, typical dissipation — 1.2 watts.
- 180 pin ceramic PGA package.

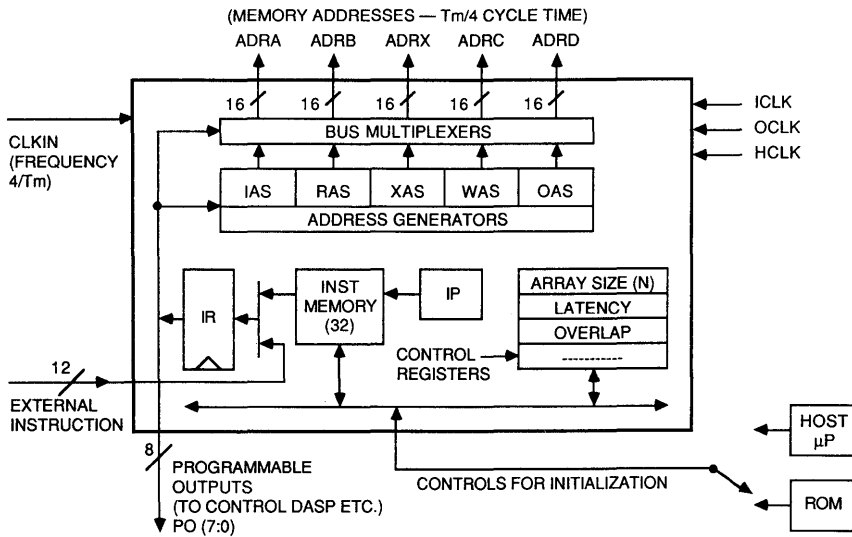


FIGURE 6: PAC BLOCK DIAGRAM

must be clocked into external registers (over a machine cycle) which, in turn, can be used to address four-port memories to feed data to the DASP I/O ports.

It is important to note that the bus multiplexers (Figure 6) have been included on the PAC so that various address sequences can be programmed to appear on the desired output buses. This allows the roles of memories in a system to be reallocated under program control. Various address sequences which are supported on the PAC are as follows:

Mnemonic:	Sequence Description
FFT0 to FFT15:	FFT: Data/Coefficient address sequences associated with an in-place, Decimation-in-frequency (DIF) FFT algorithm. The sequences span from column 0 to column 15 of a FFT flowgraph, covering up to a 64K point data array. The radix for the algorithm is defined in the control registers. Digit reversed addresses can be optionally produced in the final FFT column.
SEQ:	Sequential: A normal binary sequence for the purpose of input, output, windowing etc.
SSEQ:	Symmetric Sequential: A normal binary sequence which is symmetrical in the middle to handle symmetric windows, etc.
FFT2N:	Supports DASP's FFT2N Function: Generates addressing sequences to handle data for the recombination associated with the implementation of 2N real point FFT on the N complex-point FFT machine.
FFTNN:	Supports DASP's FFTNN Function: Generates addressing sequences to handle data for the recombination associated with the implementation of two separate N real-point FFT's on the N complex-point FFT machine.
FTRS:	Filter Sequence: The overlap/save sequence to allow overlapping of data frames.

3.2 PAC: Control Registers

The PAC also contains several user-loadable control registers which add to the versatility of the PAC (Figure 6). These registers supply various parameters to the PAC describing the configuration of the user system. Some of the registers are described below as examples.

Array Size (N):	Specifies the size of the data array to be processed. It can range from 4 points to 64K points.
Processor Latency (PLAT):	Specifies the latency of the DASP in terms of machine cycles.
Memory Latency (MLAT):	Specifies the latencies through the external memories associated with the DASP. Note that latency in a memory path is introduced if the address and/or data of a memory is being latched for high performance applications. The PAC compensates for these latencies when generating the addresses and write strobes for corresponding memories.
Overlap Size (K):	Specifies the size of the overlap in successive data frames. The overlapping is normally used for frequency-domain filtering. It can range from 0 to 50% of the array size.
Configuration (RCONFIG):	Contains system configuration-type information such as cascaded system, single-memory system, radix type.

3.3 PAC: Instruction Memory

The PAC also has a 32 word (20-bit) user loadable instruction RAM which holds the user's DSP program. The concept of a PAC instruction is somewhat different than a microprocessor instruction. In microprocessors, an instruction typically manipulates one or a couple of data values. A PAC instruction controls a full pass of the N-Point data array through the DASP, where N is defined in the appropriate PAC control register. During the pass, a programmed DASP function will be applied

to the successive sets of data values in the N-Point data array. The DASP functions and the definition of a set of data values are defined in section 2.0. One instruction controls a complete pass of the data array through the DASP. A 1024 point FFT using a radix-4 algorithm, for example, takes five instructions because the corresponding FFT flowgraph consists of five FFT columns requiring five passes through the DASP. If additional passes such as windowing or magnitude-squaring are desired, one instruction will be needed for each additional pass. Typically, algorithms such as spectrum analysis, digital filtering or convolutions (via frequency domain) can be defined on the PAC by coding 10 to 20 instructions. Therefore, the on-chip 32-word memory suffices for the majority of applications, although unlimited external program memory may be used if necessary.

The format of the 20-bit PAC instruction is shown in Figure 7. The various fields of the instruction are described below.

Programmable Outputs (PO):

The user-defined 8-bit value in this field is directly fed to the PO pins of the PAC. This can be used to control various system elements including the DASP function code.

Bus Switch Code (BSC):

This field controls the PAC bus multiplexers (Figure 6) to assign the appropriate address generators to the address buses ADRA, ADRB, ADCR and ADRD. The BSC field is also output directly to the BSC pins.

Shift X-Memory Address (XSHF):

This field defines the number of bit positions to left-shift the X-Memory (coefficient) address. This feature is useful for sharing coefficient memory for different sized FFT's, etc.

Mixed-Radix Mode (MIXMD):

This bit indicates if a mixed-radix FFT (radix-4/radix-2) is being performed. By using the mixed-radix mode, it is possible to transform a data-array in which the number of points are an odd power of 2, almost at the speed of a radix-4 system.

Node Sequence Type (NODE):

This field defines the type of addressing sequences to be produced by the five address generators of the PAC.

3.4 PAC: Initialization

The PAC control registers and instruction memory are memory mapped for ease of initialization. The PAC can be initialized by a host processor or it can autoboot itself from an external ROM. The initialization option is determined by the AUTOBOOT pin. After initialization, the processing is started by activating the GO pin. The PAC then manages the complete system. It executes the DSP algorithm by continuously looping through the program. The processing can be interrupted any time by handshake signals. The PAC can then be reinitialized for another process if so desired.

3.5 PAC: Clock Schemes

The PAC is operated by using a system clock (CLKIN) at the frequency of 4/Tm. However, additional clock inputs ICLK, OCLK and HCLK are also provided. The ICLK and OCLK manage the input data-collection and the output data-dump, respectively, at the desired rate. The HCLK manages the communication to the host processor (for initialization) at the desired rate. The independent control over these clocks provides great flexibility in designing real-time DSP systems. For very high performance cascaded systems the frequency of ICLK and OCLK approach 4/Tm. Therefore, it is possible to process complex-data to a rate of 4/Tm and real data at a rate up to 8/Tm. Multiple DASP's and PAC's can be synchronized via the SYNC pins for multiprocessing.

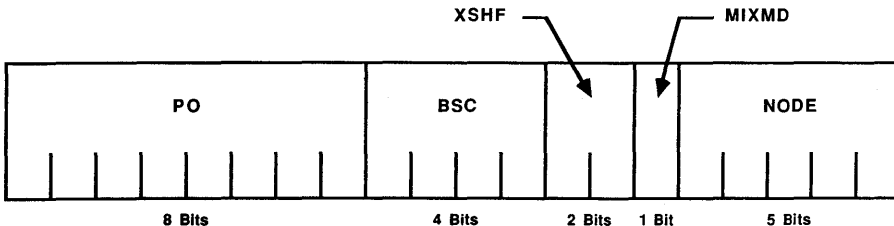


FIGURE 7: PAC INSTRUCTION FORMAT

4.0 SYSTEM ARCHITECTURES

The DASP and the PAC provide an effective means for the designer to solve many DSP problems. As mentioned earlier, the PAC is capable of handling a variety of DSP algorithms and system architectures. The designer may choose among several different system architectures supported by the PAC to achieve the desired performance. There are three basic architectures supported by PAC: recursive dual memory, recursive single memory and cascaded. The recursive dual memory architecture provides a cost effective solution with medium throughput and is extremely flexible in its programmability. The recursive single memory architecture provides the lowest throughput and the lowest cost solution. The cascaded architecture provides the maximum throughput by distributing the array processing task among multiple DASP/PAC stages. Variations on these basic architectures and user defined architectures can also be built. DASP/PAC based systems can be designed with very little effort and hardware since provisions in the device architectures were made to accommodate various system architectures.

4.1 Recursive Architecture: Dual Memory

In the recursive architecture, DSP algorithms on a single DASP/PAC stage are computed by multiple passes of the data array through a single DASP. A core stage of the recursive dual memory system is shown in Figure 8. The system employs three memory banks (B, C, X) which are all addressed and managed by the PAC. Each memory block (R and I) represents an N-word, complex data memory (Real and Imaginary Channels) where N is the size of the data array defined in the PAC. In the beginning of a process, a data frame is collected in memory B by invoking an addressing sequence on the PAC bus ADRB. The PAC begins processing by setting up a function code (e.g., BMUL, BFLY4, BFLY2) on DASP. In the first pass, the PAC transfers the data from memory B to memory C by providing the read address sequence on the bus ADRB and the write address sequence on bus ADRC. The write address sequence is appropriately staggered from the read address sequence to allow for DASP pipeline latency and any memory path latency due to the latching of address or data. During the data transfer pass, the chosen DASP function is applied to the entire N-point data array. The auxiliary data, which will be trigonometric coefficients or window coefficients in the case of FFT's, is automatically picked up from memory X using the address sequence on the bus ADRX. After the entire data array has been written into memory C, the PAC reverses the memory roles on the next pass by using its on-chip address multiplexers; memory C receives the read address sequence, the DASP receives the next

function to perform, and memory B receives the staggered write address. Data flows in the opposite direction as shown in Figure 9. Note that if the DASP is operated in the dual bus mode, no tri-state buffers are required since the DASP data buses are bi-directional. The process of alternating data directions and recursively passing the data through the DASP is repeated as many times as necessary to implement the user's entire algorithm. After all computational passes are completed, the user would then perform an I/O pass. The input and output address generators would be routed to the appropriate memory banks, and data is simultaneously loaded and unloaded. One may then repeat this entire process on a new data array.

4.2 Recursive Architecture: Dual Memory, I/O Buffered

In the previous scheme, processing resources are idle while I/O is being performed making it unsuitable for a

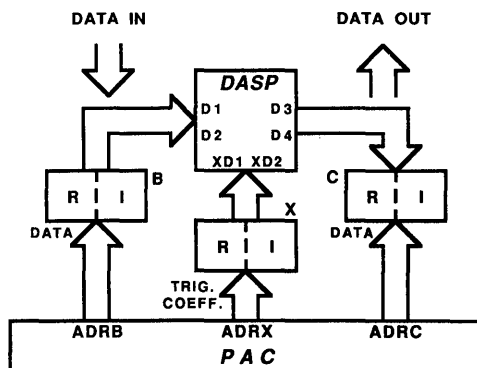


FIGURE 8: CORE DUAL MEMORY RECURSIVE STAGE

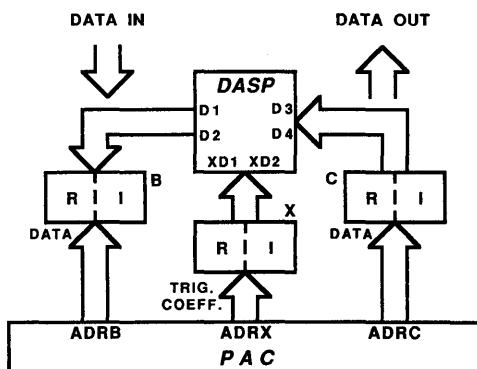


FIGURE 9: CORE STAGE - REVERSE DIRECTION

real-time system. A real-time DSP system can be configured by taking advantage of all five PAC address buses in a double buffered I/O configuration. As shown in Figure 10, two memories may be devoted to input and output while three other memories are used for processing. If the (K+1)th frame of data is being collected in memory A, the (K-1)th processed data frame is being dumped out from memory D. Memories B and C act as read and write memories for recursive execution of the DSP algorithm on the Kth frame, as discussed in the previous scheme. After the algorithm is executed, the processing can be held until the (K+1)th frame of data has been collected in memory A and dumping of the (K-1)th processed data frame from memory D has been completed. At this time, the roles of memories A and D are interchanged with those of memories B and C to begin processing of the (K+1)th frame, as shown in Figure 11. The PAC accommodates the new roles of memories by switching address sequencers among the address buses ADRA, ADRB, ADRC and ADRD. The system continues working in this fashion by reallocating the roles of memories every pass. Data may be processed in real-time by using this double buffered I/O scheme. Since the PAC has separate clocks for input (ICLK), output (OCLK) and processing (CLKIN), the clock speeds may be set so that data processing is completed before the next frame is acquired.

4.3 Recursive Architecture: Single Memory

The system cost, size and power can be vastly reduced by configuring a system around a single Data Memory, as shown in Figure 12. Since the PAC employs an in-place FFT algorithm, the read and write operations can be interleaved to one data memory. One of DASP's I/O ports is ignored and only two of PAC's address buses are utilized. The performance of such a system is halved due to the I/O bottleneck on the DASP data port. Because only one I/O port is used, it takes twice the number of cycles, compared to previous systems, to perform all the I/O operations on a single data port. Therefore, the internal computational rate of the DASP is automatically halved in order for such a system to function. As shown in Figure 12, a data frame will first be collected in memory A by invoking an address sequence on the PAC address bus ADRA. Then, the data will be processed by executing multiple passes through the DASP. During each pass, the PAC alternates between read and write cycles, providing the proper address value at the right time on address bus ADRA. Finally, the processed data is dumped out by invoking a sequential or digit-reversed sequence on the address bus ADRA.

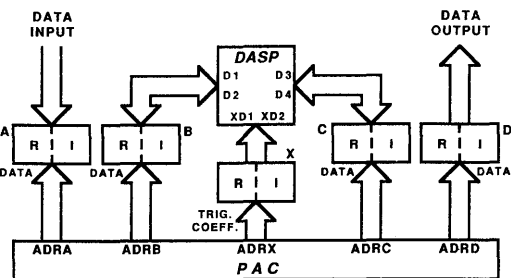


FIGURE 10: DUAL MEMORY RECURSIVE SYSTEM WITH I/O BUFFERS

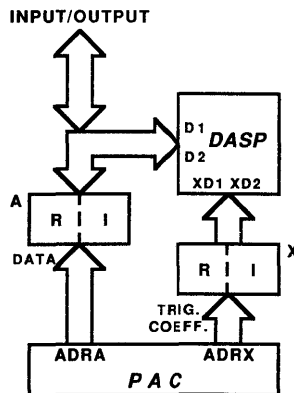


FIGURE 12: SINGLE MEMORY RECURSIVE SYSTEM

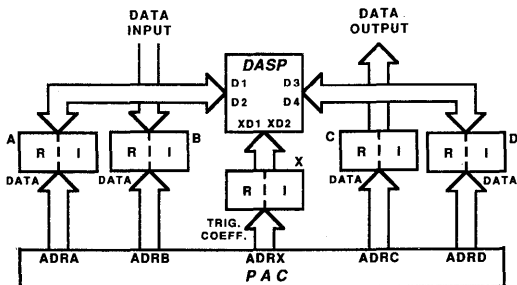


FIGURE 11: RECURSIVE SYSTEM WITH I/O BUFFERS - MEMORY REALLOCATION

4.4 Cascaded Architecture

For extremely high throughputs, several DASP/PAC stages can be cascaded. With such architectures, complex data can be processed at 50 MHz rates and real data can be processed at 100 MHz rates. In a cascaded system, several core recursive stages (Figure 8) are interconnected in a cascaded fashion to achieve the desired performance. The resultant system architecture is depicted in Figure 13. In this system, each processing node executes the same instruction on successive data input arrays, and the algorithm is distributed over several processing nodes. For example, the M columns of an FFT algorithm are executed over M processing nodes to achieve the highest performance. The data is passed from one stage to the next by the reallocation of neighboring memories to the neighbor DASP devices. In Figure 13, let us assume that the Kth data frame is being collected in memory A1. The (K-1)th data frame is being processed on node 1 by transferring the data from memory B1 to C1. Concurrently, the previous frames are being processed on other stages. The last stage is processing the (K-p)th frame to complete the processing on that frame. The (K-p-1)th processed frame is being output from memory Dp. When each processing node has completed processing, which is primarily transferring the data from one memory to another through the DASP, the memories are

reallocated, as shown in Figure 14. The memory B1 becomes the new input memory and the memory A1, which contains the Kth data frame, becomes the processing memory for the first node and so on. Note that when the system is in the mode shown in Figure 14, the PAC devices generate the write address sequence for its left neighbor and the read address sequence for its right neighbor. The PAC has two control registers to define the node type of its left and right neighbors (for a cascaded system) which enables the PAC to manage such a system. This eliminates any need for multiplexers, etc. in the address paths, enhancing the memory cycle time. The cascaded system will alternate between the configurations shown in Figure 13 and Figure 14 (at every data array pass) to execute the desired algorithm. Note that the example shown here illustrates an extremely high performance system where an algorithm, containing p passes, is distributed over p stages. A pass may be a window pass, FFT column, magnitude-square, FFTNN etc. or general purpose processing. Intermediate configurations between the cascaded system and the recursive system are also possible. A system may employ several cascaded stages, but each stage may recurse several times. In this way, the user may attain an ideal cost/performance trade-off for a given system.

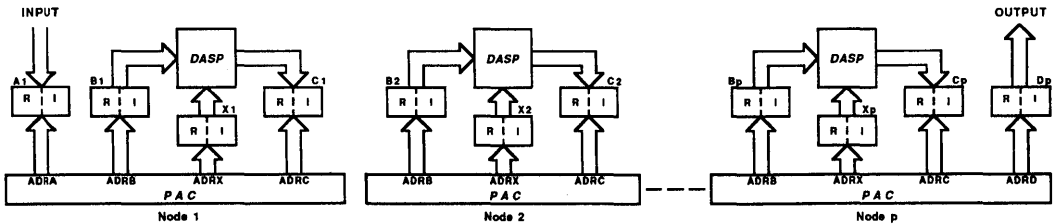


FIGURE 13: CASCDED SYSTEM

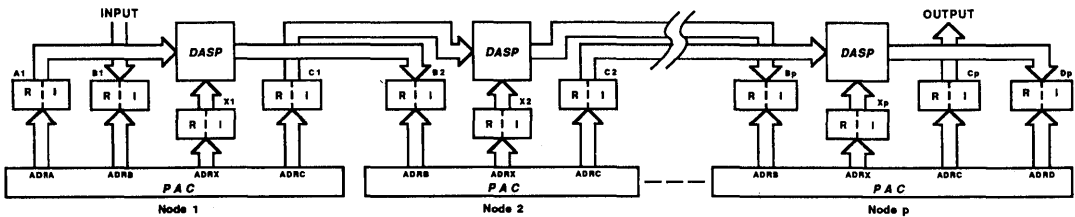


FIGURE 14: CASCDED SYSTEM - MEMORY REALLOCATION

4.5 FFT Systems

FFT systems can be easily implemented by using any of the above mentioned architectures. The algorithm is defined by programming the PAC instruction memory, and the hardware configuration is defined by appropriately programming the PAC control registers. For example, a 256 complex-point radix-4 FFT is implemented by four basic instructions of the PAC resulting in four data array passes as shown below.

- BFLY4 for FFT column 0
- BFLY4 for FFT column 1
- BFLY4 for FFT column 2
- BFLY4 for FFT column 3

This FFT algorithm can be turned into a spectrum analysis algorithm by adding two additional passes (two PAC instructions).

- BMUL for windowing
- BFLY4 for FFT column 0
- BFLY4 for FFT column 1
- BFLY4 for FFT column 2
- BFLY4 for FFT column 3
- BSQSM for magnitude-square

Note that memory for holding the window coefficients will be required in addition to the trigonometric coefficient memory. For the BMUL function, the PAC will address the window memory with a sequential or symmetric sequential sequence.

If the data is real, then two separate data sequences are combined in the input memory; one becoming real and the other imaginary. Then, a complex data FFT is performed in a normal fashion. At the end, the FFTNN function is applied to split the complex FFT into two separate real FFT's. For example, two 256-point real FFT's are executed by 5 data array passes (PAC instructions) as follows:

- BFLY4 for FFT column 0
- BFLY4 for FFT column 1
- BFLY4 for FFT column 2
- BFLY4 for FFT column 3
- FFTNN for recombining the complex FFT into two separate FFT's

At the end, two separate, transformed data frames will be left in the upper and lower part of the output data memory.

When the FFT is being performed on a data array of size N , where N is an odd power of 2, then a mixed-radix FFT can be performed, instead of a radix-2 FFT, to achieve higher performance. For example, the following passes (PAC instructions) will be required to execute a 512

point, complex FFT which also includes windowing and magnitude-square.

- BMUL for windowing
- BFLY2 for a radix-2 FFT column 0
- BFLY4 for a radix-4 mixed mode FFT column 0
- BFLY4 for a radix-4 mixed mode FFT column 1
- BFLY4 for a radix-4 mixed mode FFT column 2
- BFLY4 for a radix-4 mixed mode FFT column 3
- BSQSM for square sum

If a radix-2 FFT is desired, instead of a mixed-radix FFT in the above mentioned example, then the five butterfly passes can be replaced by nine radix-2 butterfly passes (corresponding to a radix-2 FFT flowgraph).

In the above mentioned examples, a pass means the transferring of an N -point data array from one memory to another (or to the same memory in a single memory system) through the DASP. It is possible to implement the set of those passes on a recursive dual memory system, a recursive single memory system, a cascaded memory system (where passes are distributed over multiple stages) or intermediate hybrid systems to achieve the desired performance. If the memory can be operated at a cycle time of C , then the pass will be of the duration of about NC for a dual-memory system and about $2NC$ for a single-memory system. Note that some types of passes, such as FFTNN, will not be possible on a single-memory system due to the non-in-place nature of the pass.

Formulas for determining processing times for any size FFT on various system architectures are presented in Table 7. In these formulas, N is the data array size, M is $\log_4 N$ or $\log_2 N$ and C is the memory cycle time. K is the number of optional passes for performing windowing or magnitude-squaring if desired. Note that 24 memory cycles have been added to account for the DASP data path latency and the PAC instruction switching overhead. The formulas assume a radix-4 FFT when N is a power of 4. When N is an odd power 2, a mixed-radix FFT is assumed. The FFTNN function is utilized when the data is real. Some benchmarks, based on the above mentioned formulas, for specific size FFT's are shown in Table 2, assuming a machine cycle time of 80 nS ($C = 20$ nS).

When the transform size is small, the additional 24 memory cycles per data pass added due to the pipeline effect, may become significant for some applications. In this case, the user has an option of using a dedicated

TABLE 7: FORMULAS FOR COMPUTING FFT PERFORMANCE

DSP

OPERATION	CASCADED SYSTEM	DUAL MEMORY SYSTEM (ONE STAGE)	ONE MEMORY SYSTEM (ONE STAGE)
N Complex-Point FFT/IFFT If $N = 4^M$	$(24+N)C$ (M+K Stages)	$(M+K)(N+24)C$	$2(M+K)(N+24)C$
N Complex-Point FFT/IFFT If $N = 2(4^M)$	$(N+24)C$ (M+K+1 Stages)	$(M+K+1)(N+24)C$	$2(M+K+1)(N+24)C$
N Real Point FFT/IFFT If $N = 4^M$	$\frac{(N+24)C}{2}$ (M+K+1 Stages)	$\frac{(M+K+1)(N+24)C}{2}$	$2(M+K+1)(N+24)C$
N Real Point FFT/IFFT If $N = 2(4^M)$	$\frac{(N+24)C}{2}$ (M+K+2 Stages)	$\frac{(M+K+2)(N+24)C}{2}$	$2(M+K+2)(N+24)C$

controller instead of the PAC which can eliminate the pipeline effect. Such a controller can be built by using a counter and a few PROM's.

4.6 Fast Convolution and Digital Filtering

For large sequences, a time domain convolution may be more efficiently performed by first transforming the two sequences to the frequency domain via the FFT, multiplying the spectra together and performing the inverse FFT transform on the result [Reference 2 (p.198), Reference 3 (p.633)]. This process is known as fast convolution. Often times, the linear convolution of an infinitely long sequence with a finite length, constant sequence is desired (as in digital filtering). One method for accomplishing this convolution is to break the long sequence into data arrays of length N. This data is convolved by using the above mentioned method. Because of the finite array length, the next data array must be overlapped with the previous array by an amount at least equal to the constant sequence length, K (filter length) as shown in Figure 15 [Reference 3 (p.679)]. When data is output, the first K values must be discarded, as shown in Figure 15. This I/O scheme, which is known as the "overlap/discard" method, could become very complex for LSI/MSI implementation. The PAC accommodates this overlap discard method by providing special addressing sequences, control signals, and a special control

register to set the overlap amount. A data flow diagram, illustrating the process of digital filtering in the frequency domain, is shown in Figure 16. A recursive dual memory system implementation for such a system is shown in Figure 17. Basically, two additional K-word memories (OVA and OVB) which hold the overlapped points, have been added to the recursive system architecture discussed earlier. The memories on the ADRX address bus hold the trigonometric coefficient table for the FFT, window coefficients and the desired frequency response of the digital filter. A cascaded system architecture can also be built for digital filter applications by following the schemes discussed in section 4.4.

4.7 Digital Filter System

The digital filter algorithms can be implemented on a desired system architecture by simply programming a few passes in the PAC. Let us assume that a digital filter needs to be built with 512 poles and 50% overlapping data frames. Therefore, the data frames will consist of 1024 complex points. The filter algorithm will consist of the following 11 passes (PAC instructions).

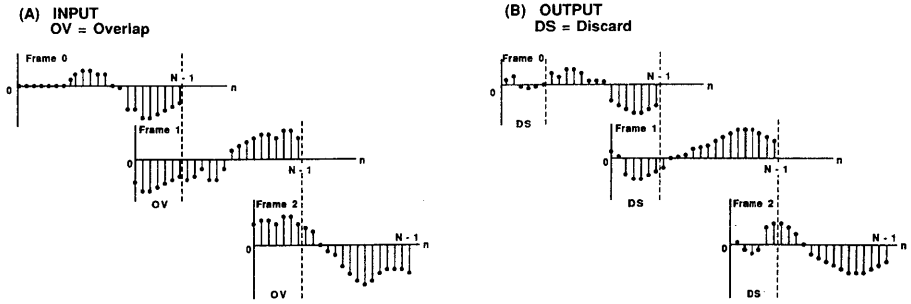


FIGURE 15: OVERLAP/DISCARD FAST CONVOLUTION

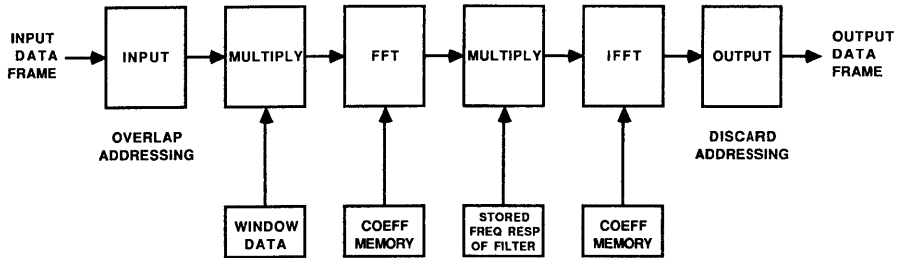


FIGURE 16: DIGITAL FILTERING IN FREQUENCY DOMAIN

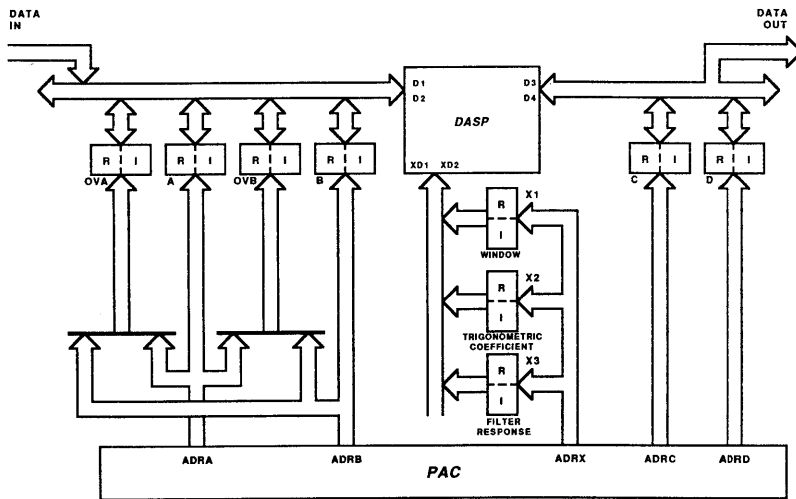


FIGURE 17: OVERLAP/DISCARD RECURSIVE SYSTEM WITH I/O BUFFERS

- BMUL for windowing
- BLFY4 for FFT Column 0
- BLFY4 for FFT Column 1
- BLFY4 for FFT Column 2
- BLFY4 for FFT Column 3
- BLFY4 for FFT Column 4
- BMUL for multiplying with filter response
- BFLY4 for IFFT Column 0
- BFLY4 for IFFT Column 1
- BFLY4 for IFFT Column 2
- BFLY4 for IFFT Column 3
- BFLY4 for IFFT Column 4

These passes can be implemented on a recursive DUAL memory architecture (Figure 17) or a cascaded system. Benchmarks for 32-, 128, 512 and 2048 pole filters, implemented with fast convolution, are stated in Table 3, assuming a machine cycle time of 80 nS.

5.0 NUMERIC PERFORMANCE

As mentioned earlier, the DASP's internal arithmetic is a mixture of 16 and 20-bit two's complement formats. Hence, the error induced by its internal quantization and rounding is significantly less than that induced by straight 16-bit arithmetic. Additionally, because of DASP's block floating point capability, the dynamic range of the input data that can be processed is increased dramatically. Figures 18 and 19 illustrate the signal-to-noise ratio as well as the dynamic range of data transformed on the DASP. The input data is 16-bit full scale random noise for the signal-to-noise ratio analysis and 12-bit (input SNR 72 dB) for the dynamic range analysis.

6.0 TEST FEATURES AND RELIABILITY

Great emphasis on test and reliability has been placed in the architecture definition, design, production and testing of the DASP and the PAC devices. The architectures of the DASP and the PAC are highly accessible from the pins, allowing an acceptable fault coverage with a moderate number of test vectors. Furthermore, all registers of the DASP and the PAC are on a serial scan path, providing an easy access to all the hardware elements. In addition to the production testing of devices, the serial scan path can also be utilized to test the integrity of the DASP and the PAC devices as a system design feature. The serial scan

path is operated through a separate interface, called the Non-Functional-Test (NFT) interface, which is independent of the normal functional pins.

7.0 SPECIFICATIONS

7.1 DASP (HDSP66110)

The DASP is packaged in a ceramic, 269 pin, Pin-Grid-Array (PGA) Package (a surface mount version will be available in the future). The key parameters of the HDSP66110 are listed in Table 8. The package is illustrated in Figure 20 and the pin description is shown in Table 9. The device is qualified for both commercial and military applications.

7.2 PAC (HDSP66210)

The PAC is packaged in a ceramic, 180 pin, PGA package (a surface mount version will be available in the future). The package is illustrated in Figure 21 and the pin description is shown in Table 10. The key parameters of the HDSP66210 are listed in Table 11.

8.0 SYSTEM DEVELOPMENT SUPPORT TOOLS

The primary emphasis in the architectures of the DASP/PAC devices is on high performance, ease of use and providing total system solutions. Therefore, a DSP system can be easily built around DASP/PAC devices with minimum of effort and a great hardware efficiency. The system development task is further eased by several support tools.

- Printed User's Guides for the DASP and the PAC
- Software Simulators for the DASP/PAC Systems (VAX VMS and IBM PC)
- Hardware Evaluation Module (EVM) for the DASP/PAC System

Figure 22 shows a typical DSP system development cycle using DASP/PAC support tools.

8.1 User's Guides and Application Notes

The DASP and PAC User's Guides contain detailed architectural descriptions, interface information, electrical/mechanical specifications and system application notes.

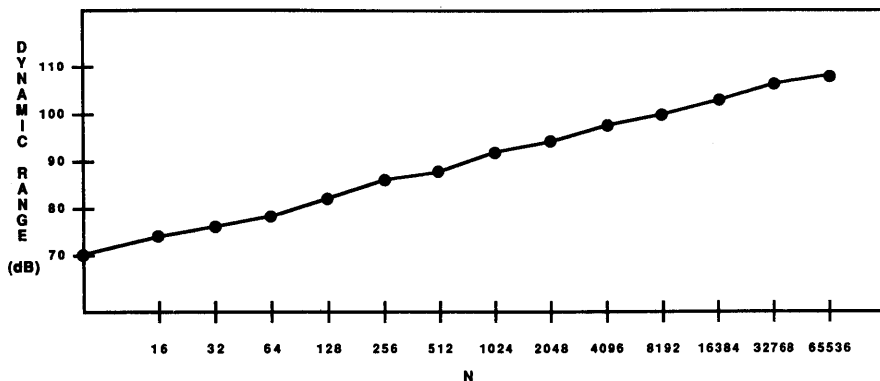


FIGURE 18: DYNAMIC RANGE PLOT

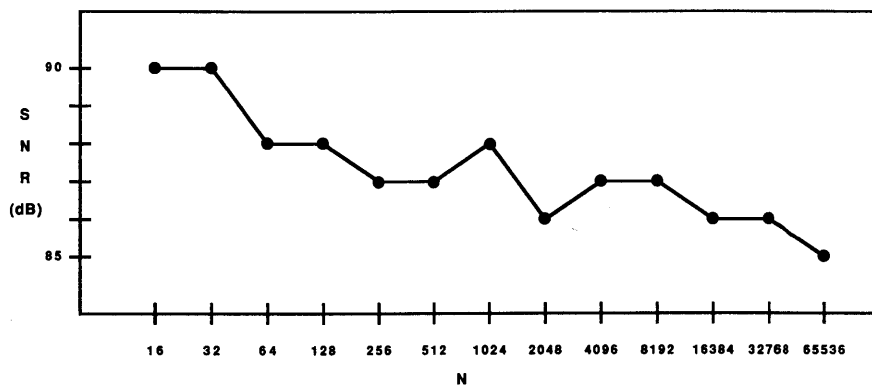


FIGURE 19: SIGNAL-TO-NOISE RATIO PLOT

TABLE 8: DASP KEY PARAMETERS

- Typical Supply Voltage: 5 Volts
- Typical Power Dissipation: 1.2 Watts
- TTL Compatible Interfaces
- Minimum Machine Cycle Time: 80 nS (T_m)
- Maximum Input Master Clock (CLKIN)
 - 25 MHz ($2/T_m$) in Quad Mode
 - 50 MHz ($4/T_m$) in Dual Mode

DSP

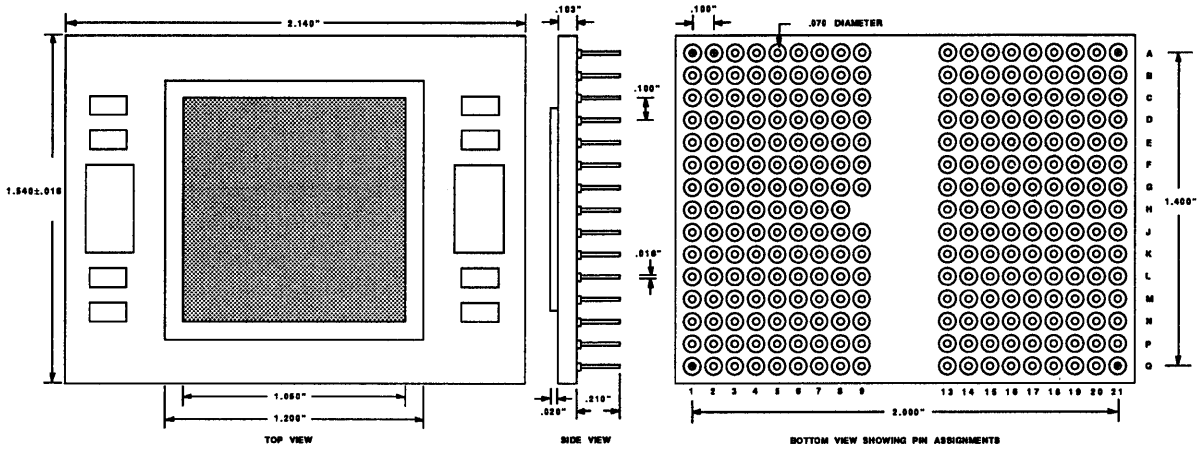


FIGURE 20: DSP PACKAGE

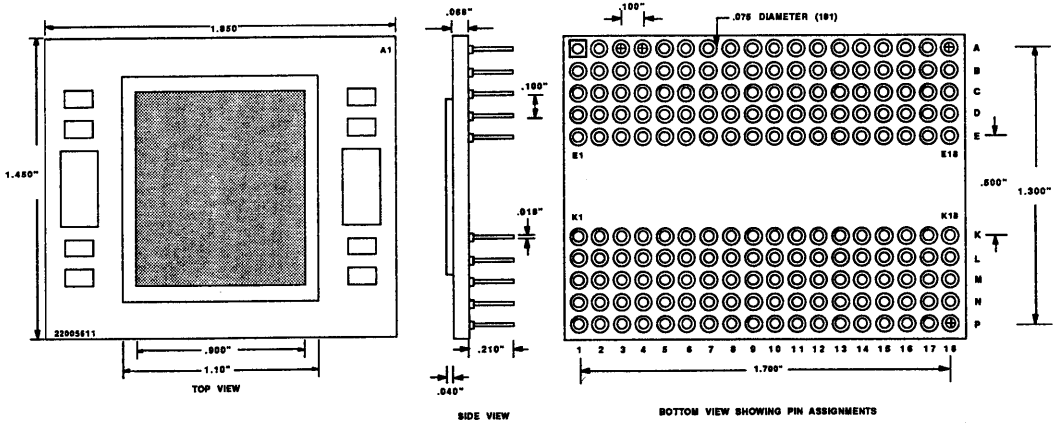


FIGURE 21: PAC PACKAGE

TABLE 9: DASP PIN DESCRIPTION

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED	
			QUAD MODE	DUAL MODE
DATA/AUX-DATA BUSES				
D1 (15:0)	I/O	I/O Data Bus	16	16
D2 (15:0)	I/O	I/O Data Bus	16	16
D3 (15:0)	I/O	I/O Data Bus	16	16
D4 (15:0)	I/O	I/O Data Bus	16	16
D5 (15:0)	I	Input Data Bus	16	None
D6 (15:0)	I	Input Data Bus	16	None
D7 (15:0)	O	Output Data Bus	16	None
D8 (15:0)	O	Output Data Bus	16	None
XD1 (15:0)	I	Input Aux Data Bus	16	16
XD2 (15:0)	I	Input Aux Data Bus	16	16
XD3 (15:0)	I	Input Aux Data Bus	16	None
XD4 (15:0)	I	Input Aux Data Bus	16	None
CONFIGURATION CONTROLS				
QUAD MUXRW	I	Quad Bus Mode Multiplexed Read Write (Single Memory System)	1	1
RVDIR	I	Reverses the Directionality of I/O Data Buses	1	1
OE'	I	Output Enable: Tristates All Data Buses if High	1	1
DATA CONTROLS				
FC (5:0)	I	Function - Code to Define Function	6	6
SFI (2:0)	I	Shift Input: Controls the Right Shift on Incoming Data	3	3
XSFI	I	Auxiliary Shift Input: Controls the Shift on Incoming Auxiliary Data	1	1
COMP (3:0)	I	Complement Control for the Input Data Buses	4	2
OVF/OVFP/OVFA	O	Overflow Outputs from Internal Processors	3	3
SHIFT FACTOR GENERATOR FOR BLOCK FLOATING POINT				
SFO (2:0)	O	Scale Factor (SF) Output: Determines Scaling for the Next Pass	3	3
ASFI (3:0)	I	Accumulated SF Input	4	4
ASFO (3:0)	O	Accumulated SF Output	4	4

DSP

6

TABLE 9: DASP PIN DESCRIPTION (Cont.)

DSP

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED	
			QUAD MODE	DUAL MODE
SHIFT FACTOR GENERATOR FOR BLOCK FLOATING POINT (CONT.)				
INITPR	I	Initializes Scale Factor Processor	1	1
RDX16	I	Configures the Scale Factor Generator for Radix-16 Mode	1	1
TIMING CONTROLS				
CLKIN	I	Clock Input: At $4/T_m$ Frequency in Dual Bus Mode and $2/T_m$ Frequency in Quad Bus Mode	1	1
SYNC	I	System Clock Synchronization Signal	1	1
MCLKOUT	O	An Output Clock Signal at Machine Cycle Rate (Frequency $1/T_m$)	1	1
CLKOUT	O	A Delayed Version of CLKIN, Compensated for Clock to Output Data Delay. Useful for Memory Writes.	1	1
BOP	I	Beginning of Pass Signal	1	1
EOP	I	End of Pass Signal	1	1
SERIAL SCAN FOR NON-FUNCTIONAL-TEST (NFT)				
NFT	I	NFT in Progress	1	1
SIN	I	Serial Scan Input	1	1
SOUT	O	Serial Scan Output	1	1
NFTR	I	Reset Registers for NFT	1	1
NFTS	I	NFT Shift in Progress	1	1
EN	I	Enable Registers for Normal Operation	1	1
SUPPLY				
VCC	I	Voltage Supply	3	3
GND	I	Ground	3	3
TOTAL PINS USED ON THE PACKAGE			244	146

TABLE 10: PAC PIN DESCRIPTION

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
ADDRESS BUSES			
ADRA (15:0)	I/O	(Output) Address Bus for Memory A/(Input) Host Address Bus	16
ADRB (15:0)	I/O	(Output) Address Bus for Memory B/(Input) Host Data Bus	16
ADRC (15:0)	O	Address Bus for Memory C	16
ADDR (15:0)	O	Address Bus for Memory D	16
ADRX (15:0)	O	Address Bus for Auxiliary Memory X	16
OE'	I	Output Enable: Tristates Address Buses if High	1
MEMORY CONTROLS			
AWE'	O	Memory A Write Strobe	1
BWE'	O	Memory B Write Strobe	1
CWE'	O	Memory C Write Strobe	1
DWE'	O	Memory D Write Strobe	1
OVAWE'	O	Filter Overlap Memory A Write Strobe	1
OVBWE'	O	Filter Overlap Memory B Write Strobe	1
OVACS'	O	Filter Overlap Memory A Chip Select	1
OVBACS'	O	Filter Overlap Memory B Chip Select	1
PASS EXECUTION CONTROLS			
BOP	O	Beginning of Pass Signal	1
EOP	O	End of Pass Signal	1
EOPR	O	End of Process Signal	1
IBUSY	O	Input Data Collection in Progress	1
OBUSY	O	Output Data Dump in Progress	1
IFULL	O	Input Memory Full	1
OEMPTY	O	Output Memory Empty	1
HOST INTERFACE/INITIALIZATION CONTROLS			
AUTOBOOT	I	Autoboot from a Memory	1
BOOTDONE	O	PAC Autoboot Complete	1
CS'	I/O	(Input) PAC Chip Select from Host/(Output) Autoboot Memory Select	1
WR'	I	Write Strobe from Host	1
RST'	I	Reset Input	1
INITPR	O	Initializes External Processor	1
GO	I	Start Instruction Execution	1
NOTE: Host Data/Address Buses Listed in "Address Buses" Above.			

DSP

6

TABLE 10: PAC PIN DESCRIPTION (Cont.)

DSP

PIN NAME	I/O TYPE	DESCRIPTION	NUMBER OF PINS USED
GENERAL COMMUNICATION SIGNALS			
PO (7:0)	I/O	(Output) Programmable Outputs from Internal Instruction/(Input) External Instruction Fields XSHF (1:0), MIXMD, NODE (4:0)	8
IP (4:0)	I/O	(Output) Internal Instruction Memory Pointer/ (Input) External PAC Instruction Field BSC (3:0)	5
BSC (3:0)	O	Bus Switch Code: Controls Internal Bus Multiplexers	4
MUXRW	O	Multiplexed Read Write (Single Memory System)	1
QUAD-MODE CONTROLS			
QAS0	O	Quad-Mode Address Strobe 0	1
QAS1	O	Quad-Mode Address Strobe 1	1
QAS2	O	Quad-Mode Address Strobe 2	1
QAS3	O	Quad-Mode Address Strobe 3	1
CLOCK SIGNALS			
CLKIN	I	System Clock Input (Frequency 4/Tm)	1
ICLK	I	Input Data Collection Clock	1
OCLK	I	Output Data Dump Clock	1
HCLK	I	Host Interface Clock	1
SYNC	I	System Clock Synchronization Signal	1
CLKOUT	O	Delayed System Clock Output (Frequency 4/Tm)	1
MCLKOUT	O	Machine-Cycle Clock Output (Frequency 1/Tm)	1
SERIAL SCAN FOR NON-FUNCTIONAL-TEST (NFT)			
NFT	I	NFT Testing in Progress	1
NFTS	I	NFT Scan in Progress	1
SIN	I	NFT Serial Scan Input	1
SOUT	O	NFT Serial Scan Output	1
SUPPLY			
VCC	I	Voltage Supply	2
GND	I	Ground	2
TOTAL PACKAGE PINS USED			156

TABLE 11: PAC KEY PARAMETERS

- Typical Supply Voltage: 5 Volts
- Typical Power Dissipation: 2 Watts
- TTL Compatible Interfaces
- Minimum Machine Cycle Time: 80 nS (T_m)
- Minimum Micro Cycle Time: 20 nS ($T_m/4$)
- Maximum Input Master Clock (CLKIN): 50 MHz ($4/T_m$)

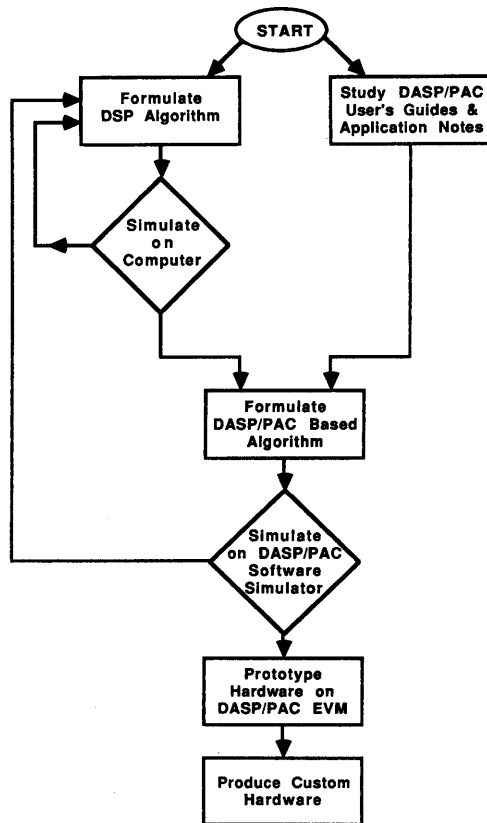


FIGURE 22: DASP/PAC SYSTEM DEVELOPMENT CYCLE

8.2 Software Simulators

Software simulators for the DASP and the PAC run on the IBM PC and VAX VMS systems. The key features of these simulators are shown in Tables 12 and 13 respectively. The IBM PC based software simulator is a menu-driven, turn-key program which integrates a and graphical display modules. The user interface is compatible with that of the EVM board, which is discussed later.

The VAX VMS based simulator can be used as a stand alone simulation tool or integrated into a larger system simulation by calling the simulator module as a subroutine. Both the DASP arithmetic system and a floating point version are supported. This enables the system designer to easily execute an algorithm on both arithmetic systems and compare the results for signal-to-noise ratio and dynamic range analysis.

TABLE 12: IBM-PC BASED SOFTWARE SIMULATOR

<ul style="list-style-type: none"> • PURPOSE — To become acquainted with DASP/PAC architectures, verify user's algorithm on DASP/PAC, use intermediate arrays for debugging hardware. • Coded in Assembly language and Z-Basic. • Data array generation capability (sinusoids). • DSP algorithm defined in the PAC instruction memory and control registers. • Algorithm executed on the DASP model. • Array display/print options. • Data/program file I/O. • Graphical displays and menu driven user interface (compatible with EVM board).
--

TABLE 13: VAX-VMS BASED SOFTWARE SIMULATOR

<ul style="list-style-type: none"> • PURPOSE — Verify algorithm on DASP arithmetic and compare results with floating point arithmetic. Higher level system simulation by calling simulator as a subroutine. • Coded in "C" language. • DASP and PAC models are integrated to execute the desired algorithm. • Algorithm defined by composing the PAC passes in an external file. • Corresponding floating point computations available for error analysis. • Simulator module may be called as a "C" subroutine.

8.3 Hardware Evaluation Module (EVM)

The EVM, which integrates the DASP/PAC and associated system hardware, allows algorithm verification on the hardware. It is capable of exercising the majority of features of the DASP/PAC devices, therefore providing great freedom to the user for system design. The key features of the EVM board are listed in Table 14. The EVM board provides an in-depth understanding of the DASP/PAC based hardware in addition to algorithm verification. A user specific system, which normally would be a subset of the EVM hardware, can be easily built after working with the EVM.

TABLE 14: EVM KEY FEATURES

- **Circuit board contains one DASP, one PAC and memories to support the processing of data arrays up to 8K size.**
- **Supports overlap/discard memories for digital filtering.**
- **Supports recursive dual memory systems.**
- **Double buffered auxiliary (coefficient) memory for FFT based adaptive systems.**
- **IBM PC interface for uploading/downloading the memories and initializing the PAC.**
- **VME bus compatible (uses PC to VME adapter board).**
- **Euro-Card 9U standard card size.**
- **Utilizes J3 connector for private I/O bus to communicate with other modules such as an A/D, D/A or another EVM.**
- **Multiple EVMs can be cascaded to emulate a cascaded DASP/PAC system.**

REFERENCES

- Reference 1: Digital Signal Processing, A.V. Oppenheim and R.W. Schaffer, Prentice-Hall, 1975
- Reference 2: The Fast Fourier Transform, E.O. Brigham, Prentice-Hall, 1974
- Reference 3: Handbook of Digital Signal Processing, D.F. Elliott, Academic Press, 1987
- Reference 4: A Unified Approach to Time-and Frequency-domain Realization of FIR Adaptive Filters, G.A. Clark, S.R. Parker and S.K. Mitra, IEEE Trans. Acoust. Speech Signal Proc., ASSP-31, 1983

***For Ordering Information See Section 1.*

NOTES:

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

FEATURES

- 150 MSPS MINIMUM CONVERSION RATE
- 70 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- Clock produced from any signal generator
- Improved Output Drive (Doubly-Terminated 50Ω)
- Optional clock divider board provided

GENERAL DESCRIPTION

The EB100 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77100A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

The HADC77100A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have

APPLICATIONS

- Evaluation of HADC77100 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

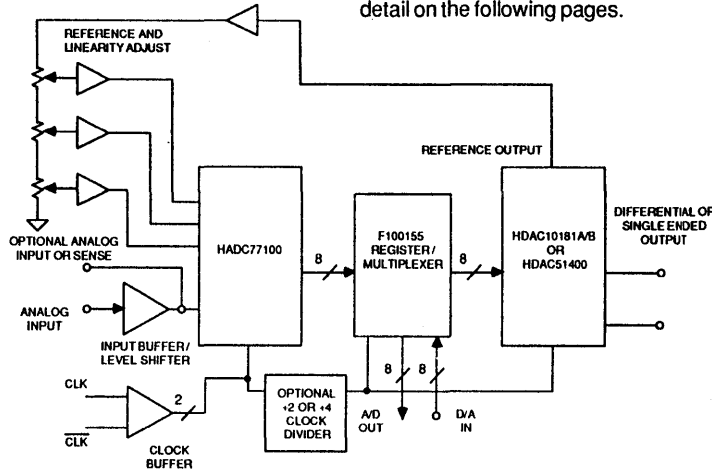
optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DACs have an internal reference to supply themselves and the HADC77100 with a stable voltage reference and gain control for different output voltage swings.

The HCMP96870 is a high speed differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2V, +5V, and ±12 to ±15 Volt power supplies are required for operation of the EB100, with nominal power dissipation of less than 10 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

7

BLOCK DIAGRAM



**For Ordering Information See Section 1.

NOTES:

FEATURES

- 150 MSPS MINIMUM CONVERSION RATE
- 70 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- ECL clock produced from any signal generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

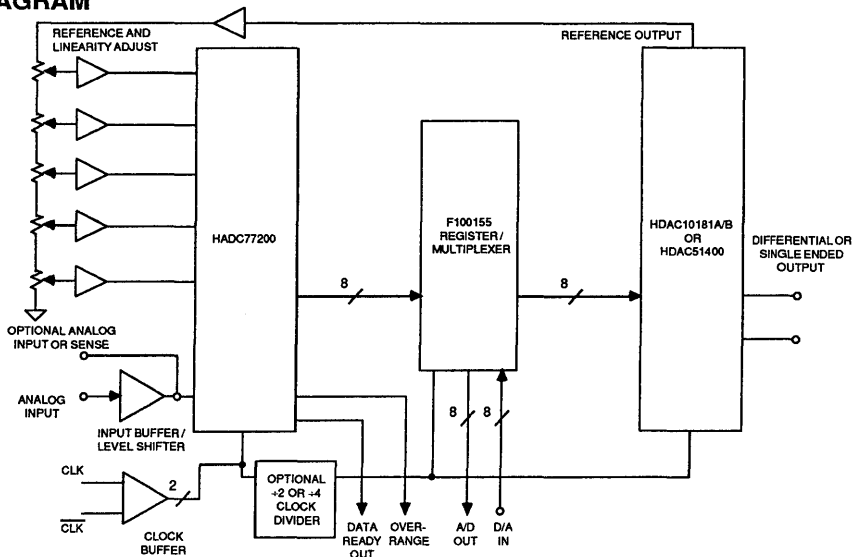
GENERAL DESCRIPTION

The EB101 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77200A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

The HADC77200A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have

BLOCK DIAGRAM



**For Ordering Information See Section 1.

APPLICATIONS

- Evaluation of HADC77200 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DACs have an internal reference to supply themselves and the HADC77200 with a stable voltage reference and gain control for different output voltage swings.

The HCMP96870 is a high speed dual differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2V, +5V, and ±12 to ±15 Volt power supplies are required for operation of the EB101, with nominal power dissipation of less than 11 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

NOTES:

FEATURES

- USE WITH EB100/101 EVALUATION BOARDS
- 70 MHz Full Scale input Bandwidth driving the converters
- Up to $\pm 100\text{mA}$ Drive current
- Low Distortion
- 15nS Settling Time

GENERAL DESCRIPTION

The EB102 is intended to demonstrate the high performance achievable with the HADC77100/200 flash A/D converters. The EB102 is a very low distortion, 70MHz buffer amplifier board. It provides for higher frequency operation than the buffer on the EB100 or EB101 evaluation boards. Included on the unit is either the Comlinear CLC221 Operational Amplifier or CLC231 Buffer-Amplifier as shown in the circuit diagram below.

The two versions are identical but are jumpered to provide for the different amplifier pinouts. The CLC221 version has the advantage of being configured up to a gain of 50 as required, and has

APPLICATIONS

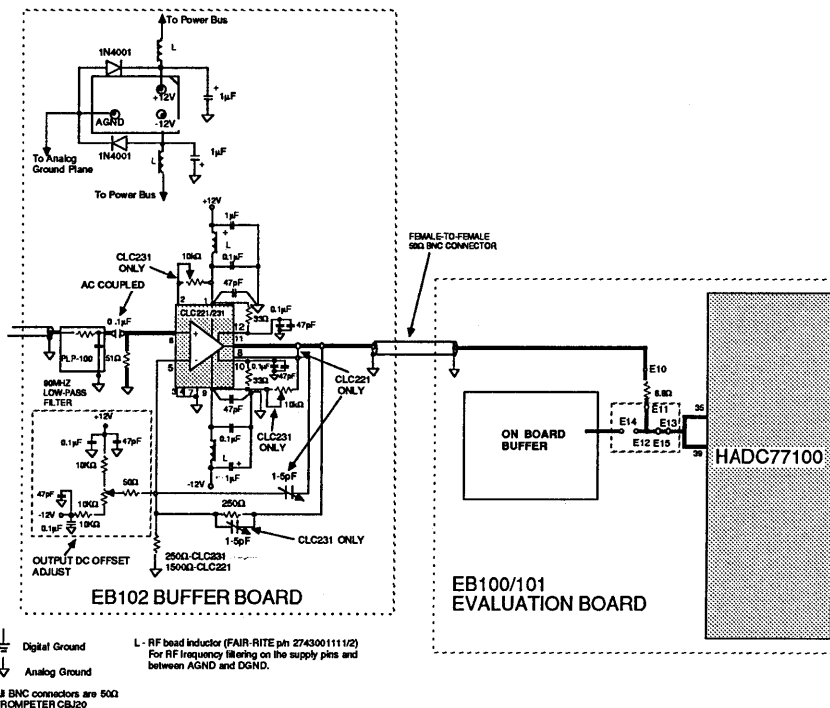
- Evaluation of HADC77100/200 A/D Converters
- High Definition Video
- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

slightly better harmonic distortion specifications. The CLC231 version has a much higher output drive capability and faster settling time.

The EB102 analog input and output are standard 50 Ω BNC connectors. Standard ± 12 to ± 15 Volt power supplies are required for operation. The board comes fully assembled, calibrated and tested.

The HADC77100/200 is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components from 50 up to 70 MHz into 8-bit digital words at a 150 MSPS update rate.

BLOCK DIAGRAM



**For Ordering Information See Section 1.

NOTES:

FEATURES

- 400 MSPS NOMINAL CONVERSION RATE
- 100 to 150 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Preamplifier Design/Optional Input Buffer
- ECL Timing skew clock generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

APPLICATIONS

- Evaluation of HADC77200 A/D Converters
- Evaluation of HDAC51400 D/A Converter
- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

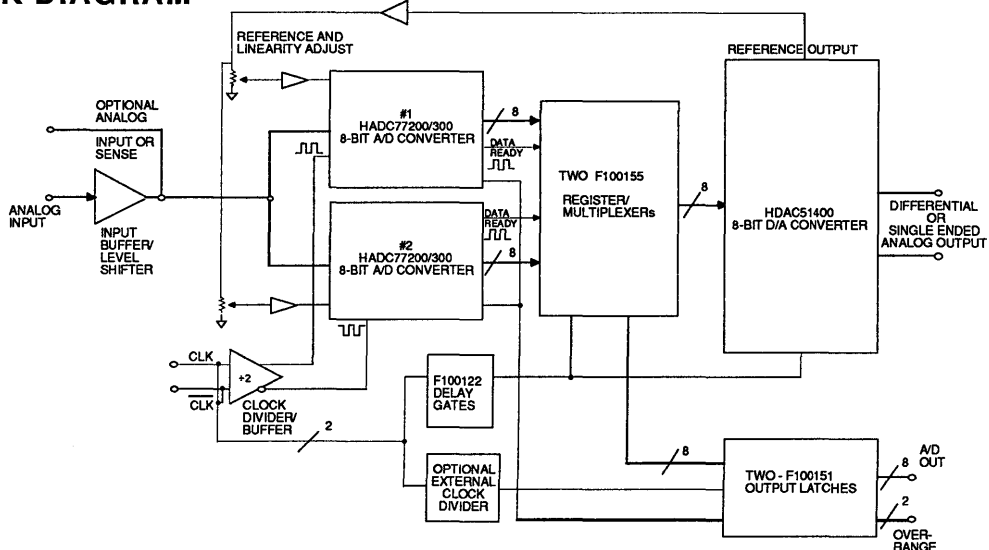
The EB103 evaluation board is intended to show the performance of the HADC77200 or flash A/D converters in a ping-ponged mode, and the HDAC51400 Ultra High Speed D/A converter for reconstruction. Included on the unit are two 100K ECL multiplexers for the combining the ping-ponged A/D converters' 16 bits of output data in to 8 bits at twice the speed. The high speed data is routed between the A/D and D/A, and also off the board as full speed or as divided down data (external clock) for slower speed FFT measurements. This is shown in the block diagram below.

The HADC77200 is a monolithic, 8-bit flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 100 MHz at a 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 is a monolithic 8-bit D/A converter capable of converting data at rates of 400 MWPS. The part has optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DAC has an internal reference to supply itself and the two HADC77200 with a stable voltage reference. It also has gain control to provide different output voltage swings so it can be used as a standard voltage output DAC.

The HCMP96870A is a dual high speed differential voltage comparator used to generate an adjustable ECL compatible clock signal for timing skew between the two A/D converters and D/A converter.

BLOCK DIAGRAM



**For Ordering Information See Section 1.

NOTES:

FEATURES:

- Provides operating environment for HADC574Z or HADC674Z and HDAC7545A Devices
- Fully Demonstrates Device Function and Resolution
- Eliminates Noisy Breadboard Evaluation Circuitry
- Buffered A/D and D/A Conversion Data Buses
- Includes Sample/Hold Amp and Output Op Amp IC's
- Unipolar or Bipolar Operation

APPLICATIONS:

- Evaluation/Comparison of HADC574/674Z Converters
- Evaluation/Comparison of HDAC7545A Converters
- System Development
- Data Acquisition Systems
- Bus Structured Instrumentation
- Process Control Systems

GENERAL DESCRIPTION

The EB104 Evaluation Board fully demonstrates the capabilities of Honeywell's HADC574/674Z and HDAC7545A 12-bit data conversion products. All of the basic power supply connections, controls lines and external components are included. The board can operate in an analog input/output fashion utilizing both A/D and D/A devices, or the devices can be operated separately. Unlike most laboratory breadboarding, the ground-planned PC board provides the necessary low-noise environment essential for 12-bit resolution. The board makes full use of connectors to allow easy hookup and operation.

Other support provided on the EB104 includes an input sample/hold amplifier, output operational amplifiers and potentiometers for offset and gain adjustments. Customization and function selections are performed by jumper pins. When considering the HADC574/674Z or HDAC7545A for system design, the EB104 Evaluation Board provides a flexible, high performance evaluation vehicle.

The EB104 is supplied with an HADC574ZBCJ and an HDAC7545AACD. It will support all 574/674 and 7545 type devices.

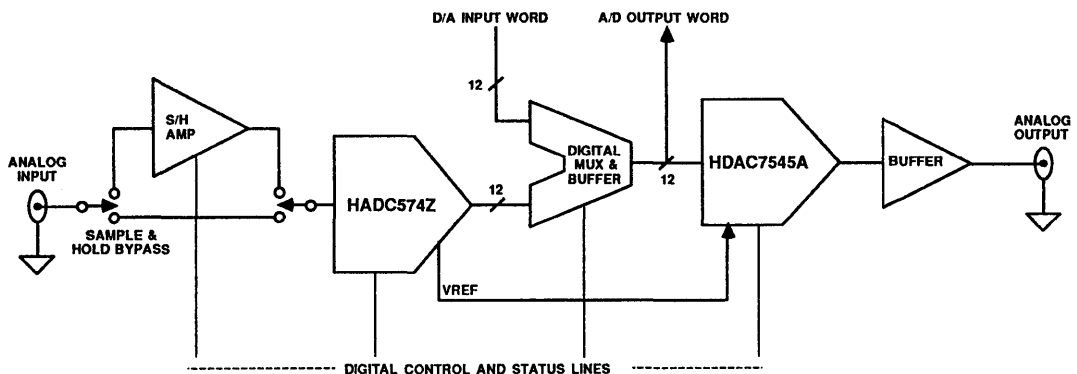


FIGURE 1 EB104 BLOCK DIAGRAM

**For Ordering Information See Section 1.

NOTES:

FEATURES

- Complete With Socketed HSCF24040ACD Device
- Demonstrates HSCF24040 Performance and Capabilities
- Toggle Switches for On-Board Control and Programming
- Connectors Allow Easy Interfacing of External Control, Programming, and Analog Signals
- Crystal Time Base
- Leaded Power Supply Connector

APPLICATIONS

- HSCF24040 Evaluation
- Prototype System Development
- Programmable General-Purpose Subassembly

GENERAL DESCRIPTION

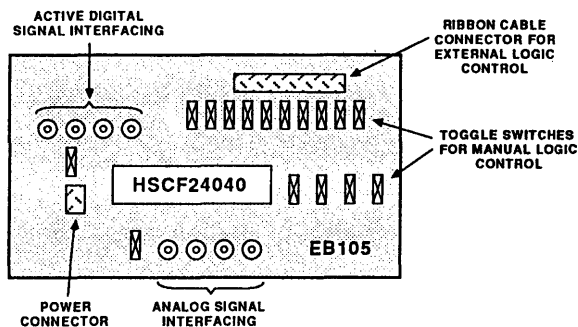
The EB105 Evaluation Board allows full exercise of the Honeywell HSCF24040 Programmable 7th Order Low Pass Active Filter. Unlike a handwired breadboard, this ground-planed, printed circuit board provides a high performance, noise-free environment. It provides full demonstration and evaluation of the superb HSCF24040 dynamic characteristics. Programming and control of the device is conveniently enabled by on-board toggle switches. Alternately, programming and control can be accomplished through the on-board ribbon cable connector. This option allows software control which can aid in system development.

By making full use of the HSCF24040, the EB105 provides an analog input and output for both the RC and

switched-capacitor filters. Both of these low-pass filters are fully programmable. Analog interfacing is accomplished with on-board BNC connectors to minimize noise and digital signal coupling. The EB105 also makes use of separate analog and digital supply grounds to further minimize digital coupling.

A clock crystal is supplied on the board which utilizes the HSCF24040 crystal oscillator feature. An external time base can be used optionally. BNC connectors are provided for external clock input and clock output, for the CONVERT output and the SYNC control line. Use of BNC connectors on these active digital lines assure a minimum of digital to analog coupling.

FIGURE 1 EB105 BOARD FEATURES



**For Ordering Information See Section 1.

NOTES:

APPLICATION NOTE FOR THE HADC77600 50MHz 10-BIT FLASH A/D CONVERTER EVALUATION BOARD WITH TRACK-AND-HOLD

by Tom DeLurio and VII Bahadur

FEATURES

- 50 MSPS TYPICAL CONVERSION RATE
- 25 MHz Full Scale input Bandwidth
- 3/4 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Preamp Comparator Design/Optional Input Buffer
- Data Ready output clock generator
- Differential Output Drive - 50 or 75Ω

APPLICATIONS

- Evaluation of the HADC77600 A/D Converter
- 10-bit Video Digitization
- Digital Oscilloscopes
- Spectrum Analyzers
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

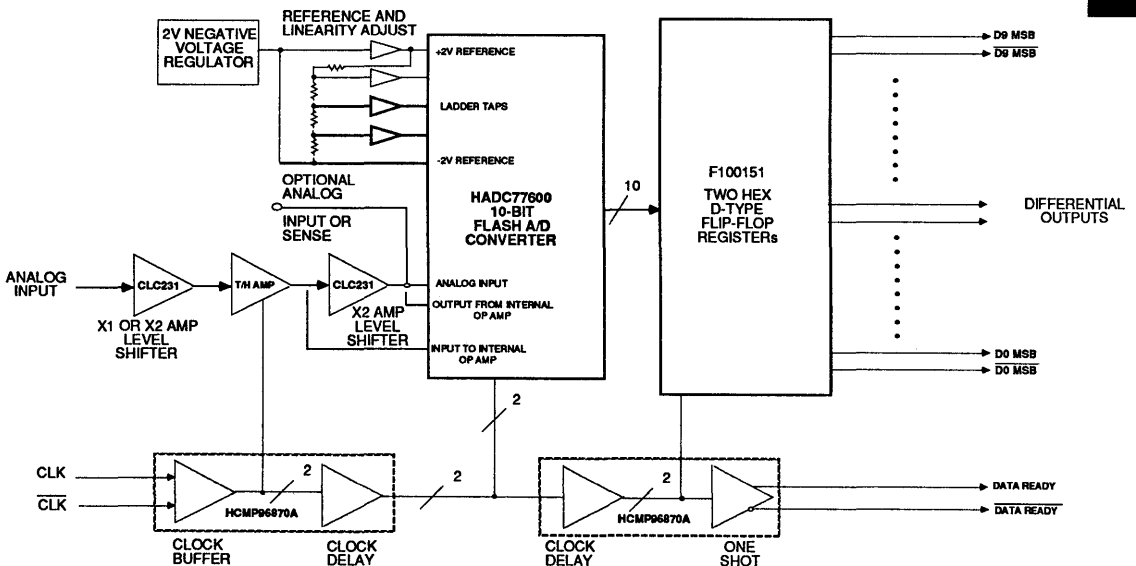
The EB106 evaluation board provides a tool to measure the performance of the HADC77600 10-bit flash A/D converter in an industry standard board level pinout. The input to the A/D converter consists of an input buffer/gain stage for a gain of 1 or 2. A track-and-hold for fast input signals, and a gain/buffer stage to drive the HADC77600 at a gain of 2 to provide a full scale input to the ADC. Included on the unit are two 100K ECL hex D-type flip-flops for differential output drive into 75Ω.

The sample rate can be set up to 50MSPS for digitizing signals up to 25MHz. The full scale input range is -1.5 to +1.5 Volts.

The HCMP96870A is a dual high speed differential voltage comparator used to generate an adjustable ECL compatible clock signal for timing skew between the track-and-hold, A/D converter, and output flip-flop registers. The comparator also produces differential data ready output pulses for use in determining when data is valid at the output pins.

An adjustable precision voltage regulator is on board for biasing up the ADC ladder reference resistors. Three of the HADC77600's seven ladder taps are adjusted using precision resistors and op amps to obtain better integral linearity.

BLOCK DIAGRAM



**For Ordering Information See Section 1.

NOTES:

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

EB100 EVALUATION BOARD 8-BIT, 150 MSPS FLASH A/D CONVERTER AND 8-BIT, 165 TO 400 MWPS RASTER D/A CONVERTER WITH REFERENCE

by Tom DeLurio Senior Applications Engineer

FEATURES

- 150 MSPS MINIMUM CONVERSION RATE
- 70 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- Clock produced from any signal generator
- Improved Output Drive (Doubly-Terminated 50Ω)
- Optional clock divider board provided

APPLICATIONS

- Evaluation of HADC77100 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB100 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77100A/B flash A/D converter and the HDAC10181A/B or HDAC54100 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

The HADC77100A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

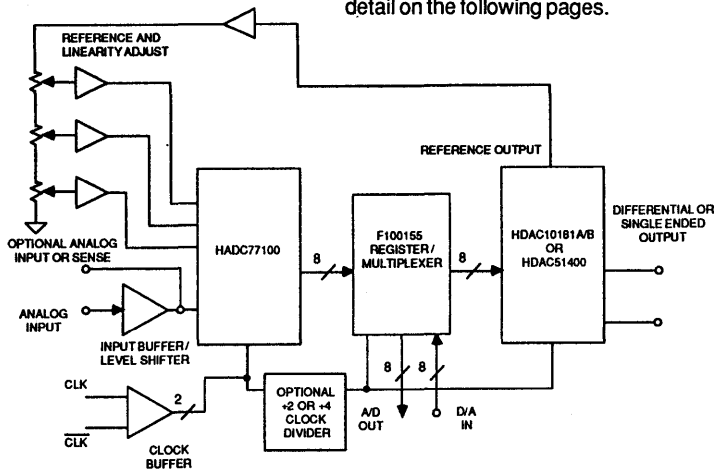
The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have

optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DACs have an internal reference to supply themselves and the HADC77100 with a stable voltage reference and gain control for different output voltage swings.

The HCMP96870 is a high speed differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2V, +5V, and ±12 to ±15 Volt power supplies are required for operation of the EB100, with nominal power dissipation of less than 10 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

BLOCK DIAGRAM



GENERAL INFORMATION

The EB100 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of Honeywell's HADC77100 8-bit A/D converter, HDAC-10181/54100 8-bit D/A converters and HCMP96870 dual comparator. The board contains circuitry for buffering the input signals, generating reference voltages, dividing the DAC and multiplexer clocks, routing input / output data, and generating ECL level differential clock signals from any signal generator. All digital inputs and outputs are 10KH and 100K ECL compatible and provisions are made for gain, offset and linearity adjustments. The board requires -5.2, +5 and ± 12 to ± 15 Volt supplies.

The EB100 evaluation board consists of seven functional sections that include an analog input buffer, A/D converter, input/output multiplexer and data latches, D/A converter, reference voltage generator, ECL clock generator, and ECL clock divider. The analog and digital grounds are separated on the board for better system grounding characteristics.

There are numerous jumper options available to switch sections in or out of the system to suit individual needs. The clock divider circuitry is on a separate board that plugs into the main board to provide divide by 2 or 4 for the multiplexer and DAC. The jumper options will be discussed in more detail in the following sections. In addition, 90MHz low pass input and output filters are on board.

ON BOARD ANALOG INPUT BUFFER

This section consists of a 90MHz low pass filter, HA2539 high frequency op-amp, and a 2N5836 rf transistor. The input impedance is 50 Ω and the gain is set at 2X so that a 1 Volt input can be applied. Compensation components are provided and can be adjusted for the desired frequency range needed. The compensation is factory adjusted for 50MHz bandwidth operation. The bandwidth of the buffer amplifier can be increased by decreasing the gain to 1X. The BNC connector shown in the schematics and layout near the output of the buffer can be used for monitoring the buffer output and input to the HADC77100. The BNC should be connected to a 50 Ω terminated oscilloscope and will provide a 10X attenuated signal.

The positive input to the HA2539 is tied to an offset adjust to center the input signal to the HADC77100 around -1V, which is needed if a 2V_{p-p} input signal is applied. The input buffer can be bypassed by removing the 6.8 Ω resistor at the emitter of the 2N5836 and the 450 Ω resistor between the BNC connector and the HADC77100. Bypass the 450 Ω resistor with a jumper wire and the HADC77100 can now be driven directly. The input impedance is 4K Ω in parallel with a 56pF distributed capacitance.

OPTIONAL ANALOG INPUT BUFFER BOARD - EB102

An alternate and higher performance input buffer is available as an option and sold separately. The EB102 is intended for users operating at the top end of the input bandwidth range of the HADC77100. The reason for a separate board is that the amplifiers utilized are quite a bit more expensive than the "on-board" buffer. But, with the added expense, increased input bandwidth with less harmonic distortion is realized.

There are two versions of the EB102 buffer board, one with a wideband op-amp (CLC221) and one with a wideband buffer amplifier (CLC231). Both versions are identical but are jumpered to provide for the different amplifier pinouts (See Figure 1A). The CLC221 version has the advantage of being configured up to a gain of 50 as required, and has slightly better harmonic distortion specifications. The CLC231 version has the advantage of a much higher output drive current and better settling time.

The Following table shows a breakdown of some of the more important specifications:

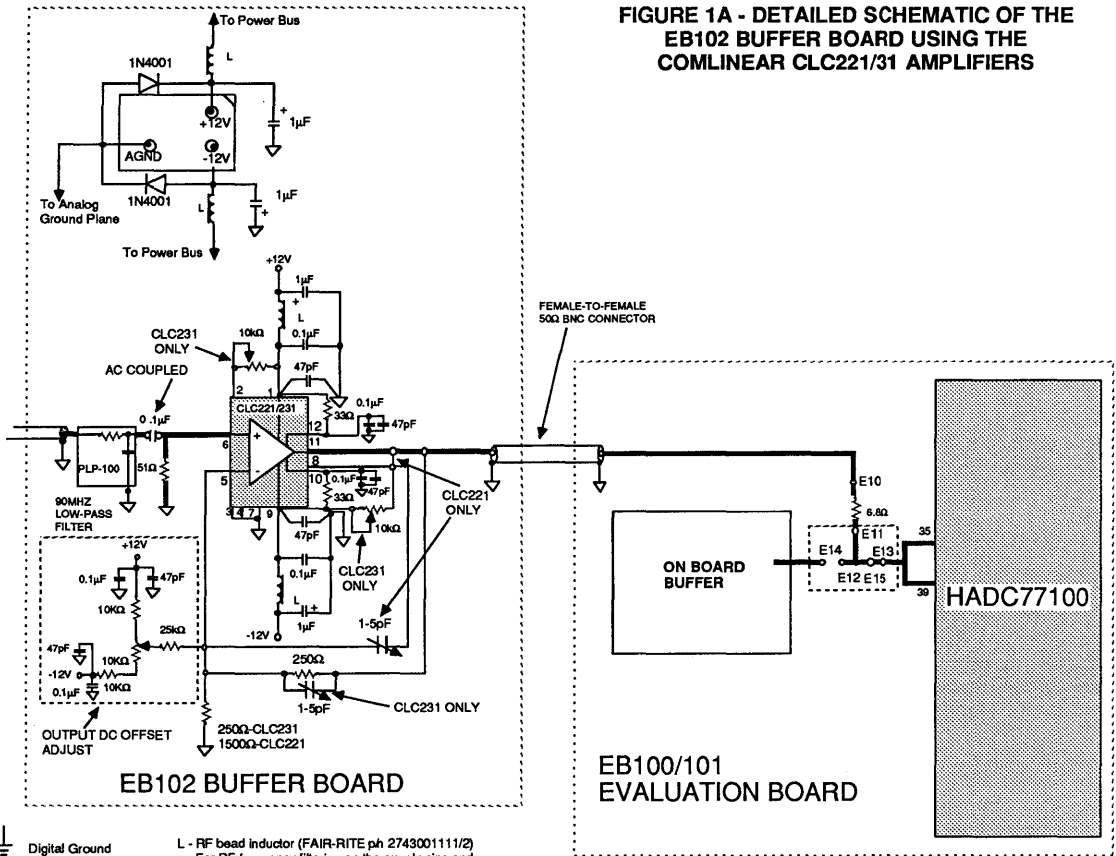
TABLE 1 - COMPARISON OF COMLINEAR CLC221/31 AMPLIFIERS



SPECIFICATION	CLC221	CLC231
Gain Range	± 1 to 50	± 1 to 5
Output (V, mA)	$\pm 12,500$	$\pm 11,100$
Slew Rate (V/ μ sec)	6500	3000
-3dB Bandwidth ($A_v=2$)	275MHz	165MHz
Settling Time (nsec, %)	15, 0.1 18, 0.02	12, 0.1 15, 0.05
Harmonic(dBc) Distortion	Second Third	-58 -59

100K ECL CLOCK GENERATOR

The ECL clock section consists of an HCMP96870 dual comparator, duty cycle and hysteresis adjust, F100131 triple D flip-flop and several jumper options. Any type high frequency signal generator can be connected to the BNC input to the comparators. Both inputs to the dual comparators are connected to the BNC. There are four outputs which generate differential 100K ECL clock signals. One set goes directly to the HADC77100 while the other two can go to the F100155 multiplexers and HDAC10181/51400 or to the clock divider circuitry.

FIGURE 1A - DETAILED SCHEMATIC OF THE EB102 BUFFER BOARD USING THE COMLINEAR CLC221/31 AMPLIFIERS



 Digital Ground
 Analog Ground
 L - RF bead inductor (FAIR-RITE ph 2743001111/2)
 For RF frequency filtering on the supply pins and between AGND and DGND.
 All BNC connectors are 50Ω TROMPETER CBJ20

The threshold input to the HCMP96870 comparators are connected together to a pot to adjust the duty cycle of the clock. The latch enable pins are also connected together to a pot to adjust hysteresis.

100K ECL CLOCK DIVIDER

The clock divider section is shown below in Figure 1B and consists of a triple D type flip-flop, which if jumpered as shown, will provide divided down clock outputs. The clock divider can be bypassed to provide a full frequency clock. The divider is provided to make it easier to monitor the HADC77100 output with a low frequency logic analyzer and to provide the DAC with a reduced sampling rate. When switching between divide by 2 or 4, the unused outputs "Q" and "Q" must be terminated. The board is initially set in the divide by 4 mode. Furthermore, the jumpers on the clock lines to the multiplexer and DAC must be removed.

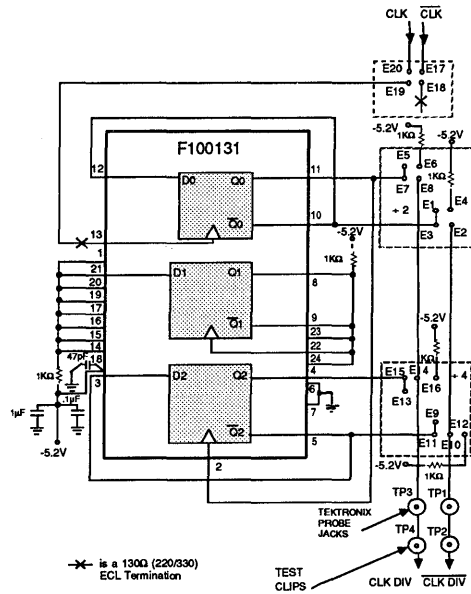


FIGURE 1B - 100K ECL CLOCK DIVIDER

REFERENCE VOLTAGE GENERATOR

The reference voltage for the HADC77100 and HDAC-10181/51400 is internally generated by the D/A converter voltage reference of approximately 1.2Volts. The A/D converters 2Volt reference, 1Volt midtap and ground are controlled by the PMI quad op-amp OP-11. The magnitude of each setting is further adjusted with potentiometer R26, R25, and R32 as shown in the detailed schematic and board layout.

INPUT/OUTPUT REGISTER AND MULTIPLEXER

The multiplexer section consists of two F100155 which select between external 8-bit digital data from the 64-pin DIN connector or data from the output of the HADC-77100. The choice is controlled by tying the SELECT pins to either an ECL high for external data or an ECL low for HADC77100 data. This data is then fed to the HDAC10181/51400 on the "Q" outputs of the F100155 and the "Q" outputs are tied to the external connector.

A/D CONVERTER SECTION

Both input pins to the HADC77100 are tied together to be either fed by the input buffer or by an external source. The MINV and LINV inputs are left open and tied internally to an ECL low. Diodes are provided to tie them high and change the output logic. The connection choices for determining the output logic are in Table 2.

D/A CONVERTER SECTION

The D/A converter section contains jumpers to use either the HDAC10181 or HDAC51400. The primary difference in the two parts is the reference voltage connections. These differences are shown in the detailed schematic in Figure 2. All EB100 boards and jumpers will be connected for the HDAC10181A part. If an HDAC51400 is indicated when the board is ordered (See last page), the board jumpers must be configured as shown in Figure 4A and 4B by the user.

The output current magnitude for the HDAC10181/51400 is controlled by a potentiometer (R36) through the DAC's Iset control pin. In addition, two 90 MHz low pass filters are provided at both out- and out+ output pins as well as 50Ω terminating resistors. The terminating resistors can be changed to 75Ω if desired. Keep in mind that the transmission line must be terminated at the receiving end with the same value resistor. The video and feedthrough controls are routed to the 64-pin DIN connector and are normally disabled.

TABLE 2 - OUTPUT LOGIC CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.
.
VIN	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.
.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: VIH, VOH
0: VIL, VOL

TABLE 2A - POTENTIOMETER AND CAPACITOR ADJUSTMENTS

NO.	FUNCTION
R26	Pot for adjusting gain to produce a 2V reference voltage for the VRB pin on the HADC77100 from the 1.2V reference voltage supplied by the HDAC10181/51400.
R25	Pot for setting the linearity adjustment or midtap pin (VRM = 1V) on the HADC77100.
R32	Pot for setting the top point (VRT) on the reference voltage ladder. Nominally set at 50mV below AGND.
R36	Pot for adjusting output current drive from the HDAC10181/51400 (See data sheets). Vout+ = 25.6(digital code X Iset)/RL
R5	Pot for setting the HCMP96870 comparator threshold voltage to adjust the ECL clock duty cycle.
R4	Pot for adjusting comparator hysteresis.
R23	Pot for adjusting up to a 2V offset voltage at the buffer output for driving the HADC77100.
R22	Pot for adjusting compensation for the buffer. This has been set for a flat response. The frequency range can be increased at the expense of gain peaking and phase margin reduction by decreasing the potentiometer resistor value.
C25	"Lead" Capacitor for controlling gain peaking in the input buffer. Used in conjunction with Pot R22 and Cap C44 for the HA2539.
C44	"Lag-lead" compensation capacitor used with R22.

POWER SUPPLY CONNECTIONS

Power to the EB100 is supplied through a six pin Molex type connector. The supply lines are color coded as shown in Figure 1C. Connect the wire end of the power supply harness to power supplies as shown by Figure 1C and the silk screen near the mating connector on the PC board itself. The power harness is attached to the board with the bevelled edges and hollow connector aligned to the mating connector.

The power requirements for the EB100 at different supplies and with or without the clock divider board is shown in Table 3. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

TABLE 3 - POWER DISSIPATION

EB100 WITH CLOCK DIVIDER, ±15V			
Voltage	Current	Power	
+15V	.145A	2.175W	
-15V	.148A	2.220W	
+5V	.006A	0.030W	
-5.2V	1.39A	7.228W	
		11.653W	
EB100 W/O CLOCK DIVIDER, ±12V			
Voltage	Current	Power	
+12V	.119A	1.428W	
-12V	.123A	1.476W	
+5V	.006A	0.030W	
-5.2V	1.27A	6.604W	
		9.538W	

AN100

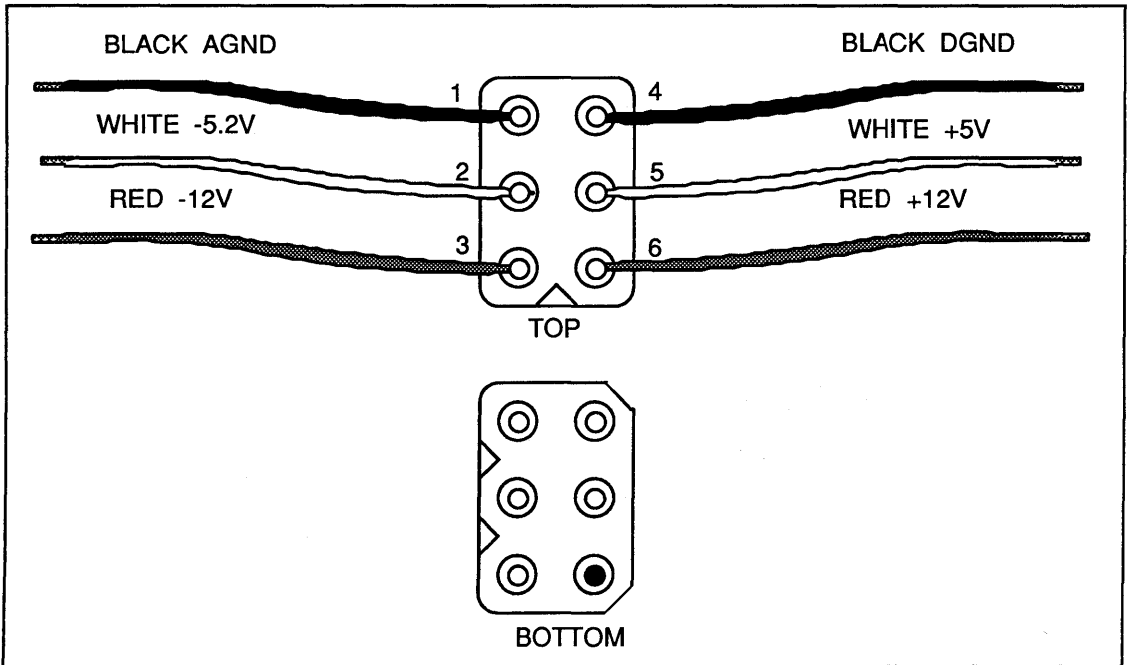


FIGURE 1C - POWER SUPPLY HARNESS CONFIGURATION

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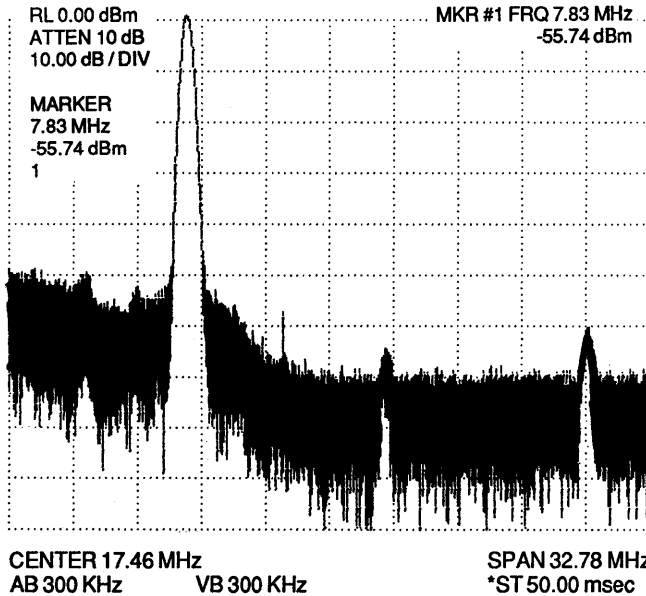
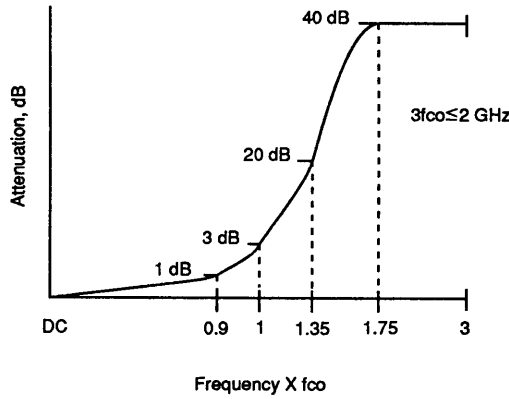
ANTI-ALIASING AND CLOCK NOISE FILTERS

The input to the EB100 buffer circuitry and the differential outputs from the D/A converter are provided with high frequency noise filters. The three filters are 90MHz low pass and are intended to be used with the full analog input frequency and full clock sampling rate of the HADC77100 A/D converter. If lower frequencies are used, the filters should be changed to filter clock noise

and harmonics for a particular application. Mini-Circuits Inc. (see below) supplies a range of low pass filters that fit into the same position as the 90MHz filters on the EB100 Evaluation board.

Also, adjustment of the clock duty cycle with potentiometer R5 will lower the overall noise floor by controlling the setup and hold time of the digital data for the multiplexers (F100155) and DAC (HDAC10181).

Low Pass
Typical Frequency Response

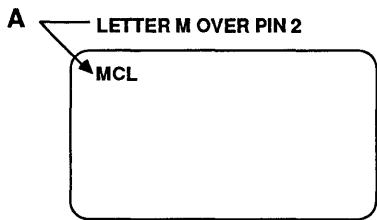


DAC OUTPUT SPECTRUM ANALYSIS OF A 10MHz INPUT FUNDAMENTAL WITH 10.7MHz (PLP-10.7) INPUT/OUTPUT LOW PASS FILTERS AND 100MHz CLOCK RATE

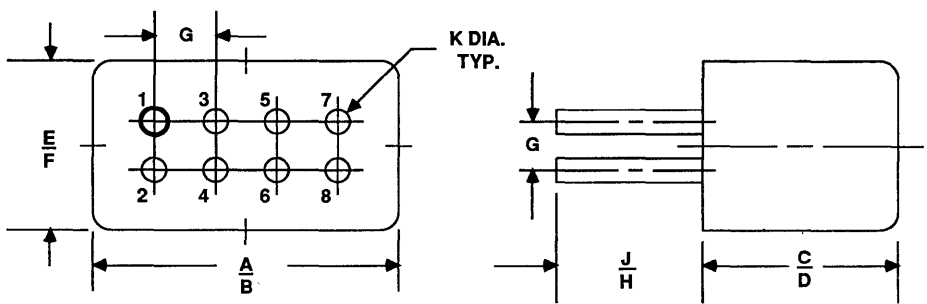
PLP
case A01

MODEL NO.	PASSBAND, MHz (loss < 1dB) Min.	f _{co} , MHz (loss 3dB) Nom.	STOP BAND, MHz			VSWR,	
			(loss > 20dB) Max.	(loss > 40dB) Max.	(loss > 40dB) Min.	Passband Typ.	Stopband Typ.
PLP-10.7	DC-11	14	19	24	200	1.7	1.7
PLP-50	DC-48	55	70	90	200	1.7	17
PLP-70	DC-60	67	90	117	300	1.7	17
PLP-100	DC-98	108	146	189	400	1.7	17

Case no.	A	B	C	D	E	F	G	H	J	K
A01	.770 19.56	.800 20.32	.385 9.78	.400 10.16	.370 9.40	.400 10.16	.200 5.08	.20 5.08	.14 3.56	.031 .79



TOP VIEW



NOTE: BLACK BEAD INDICATES PIN 1. PIN NUMBERS DO NOT APPEAR ON UNIT. FOR REFERENCE ONLY.

PIN CONNECTIONS

SEE CASE STYLE OUTLINE DRAWING

SERIES	IN	OUT	GROUND
PLP	1	8	2, 3, 4, 5, 6, 7

FIGURE 2 - DETAILED SCHEMATIC OF EB100, REVISION C

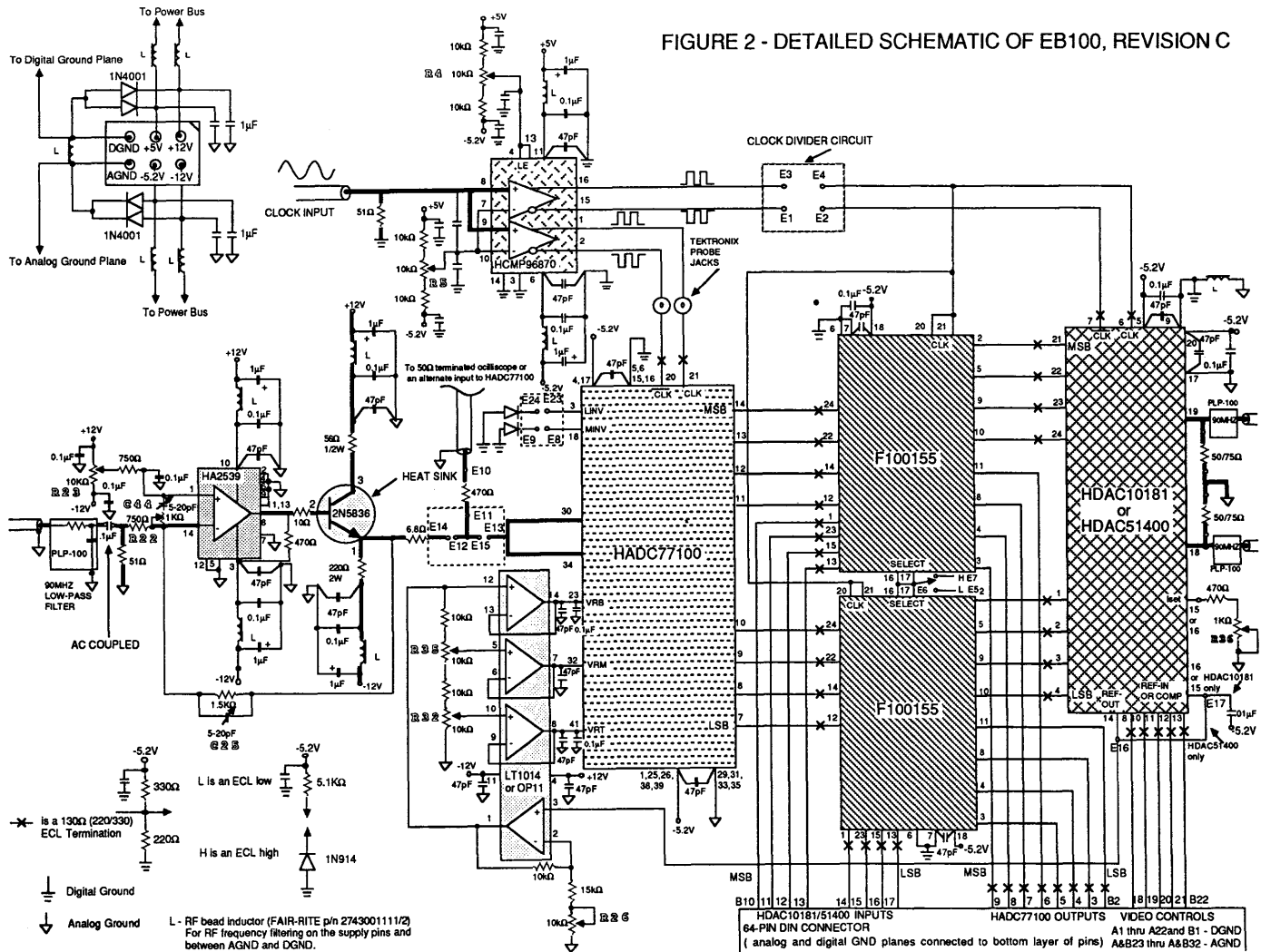


FIGURE 3 - TIMING DIAGRAM

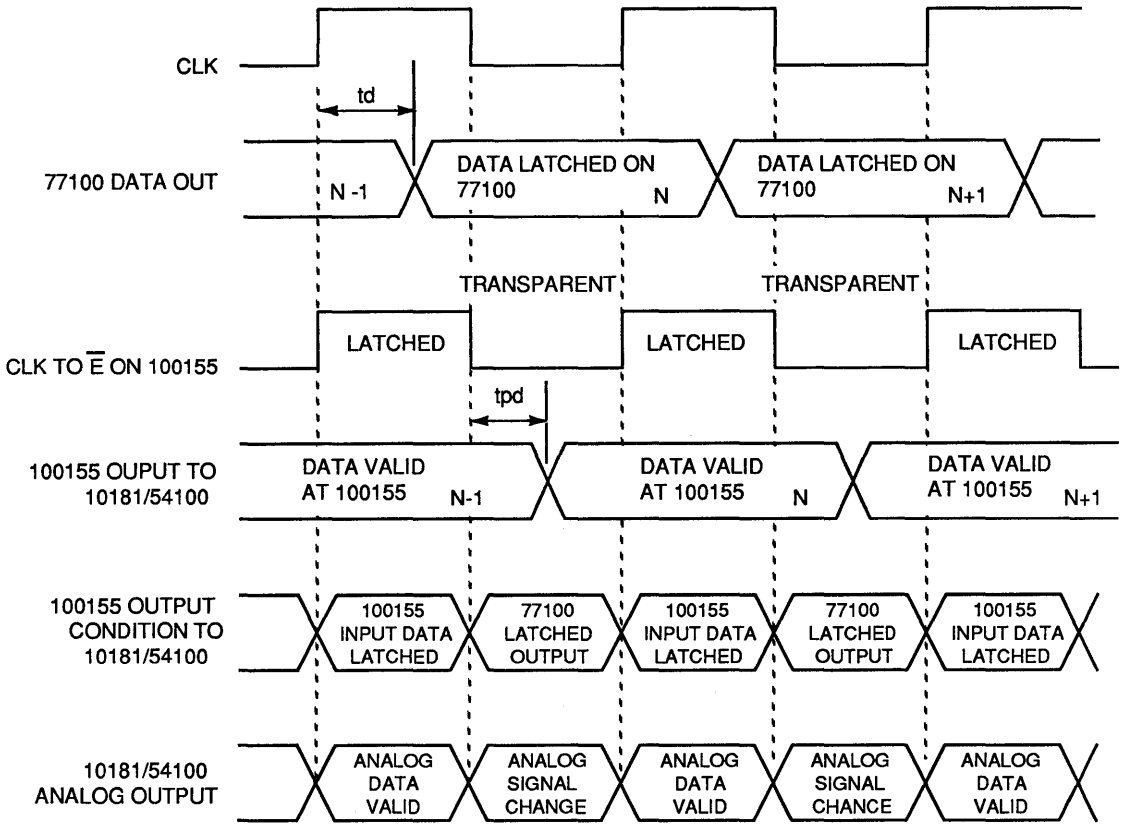
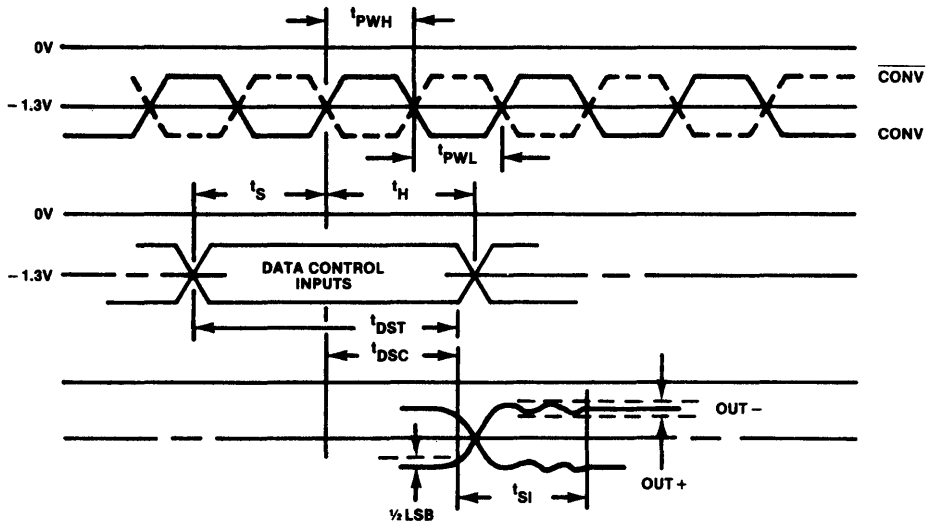


Figure 3 Continued 10181/51400 Timing Diagram

AN100



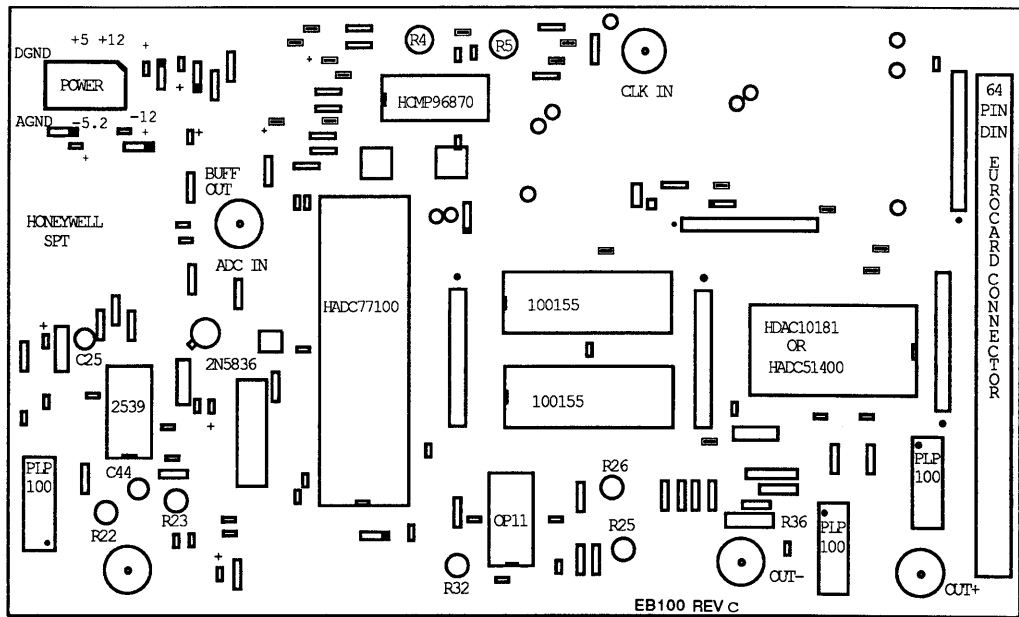
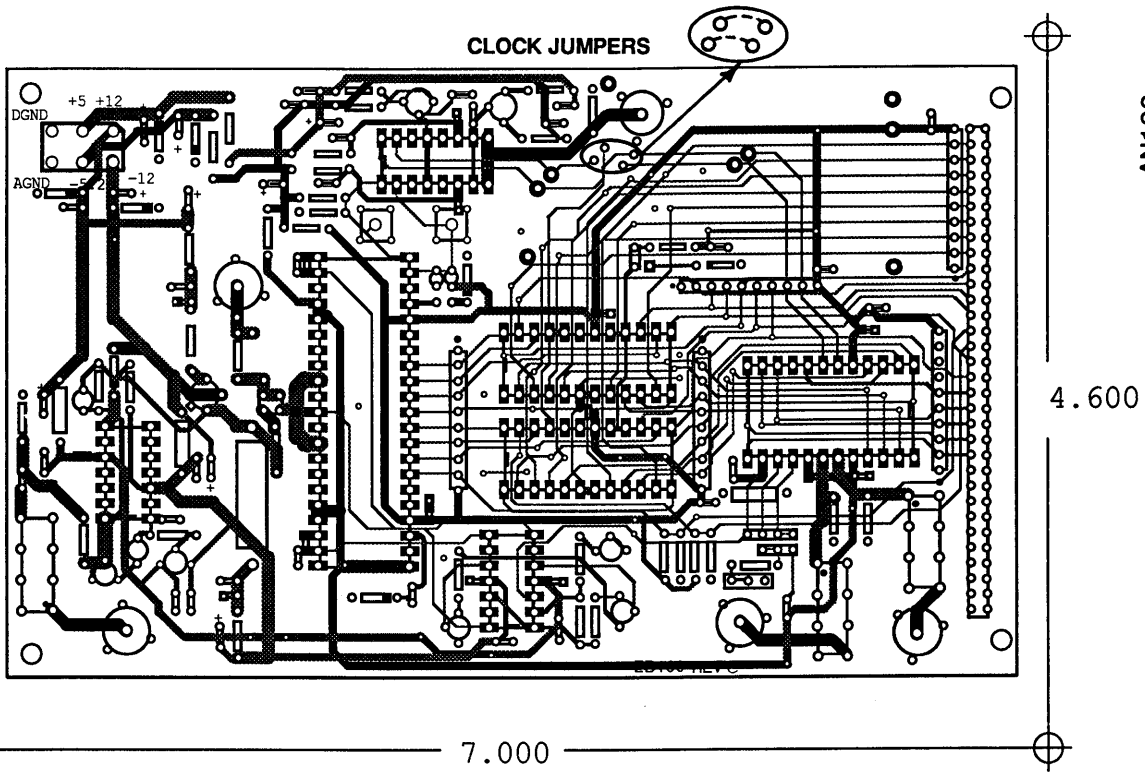


FIGURE 4A - MAIN BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

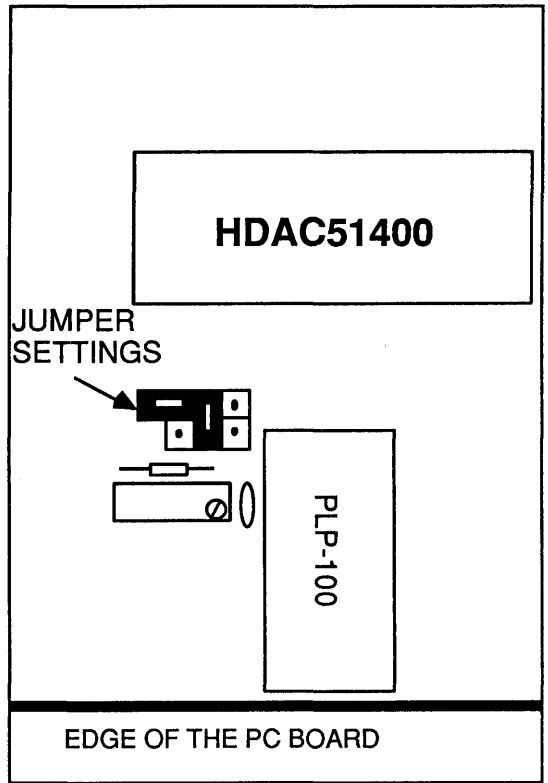
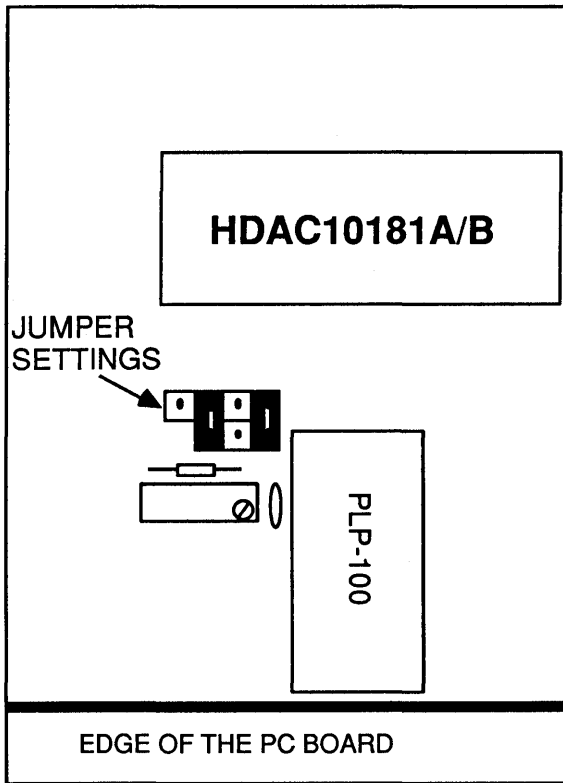


FIGURE 4B - JUMPER POSITION AND CONNECTIONS FOR EITHER THE HDAC10181A/B OR HDAC51400
(Not To Scale)

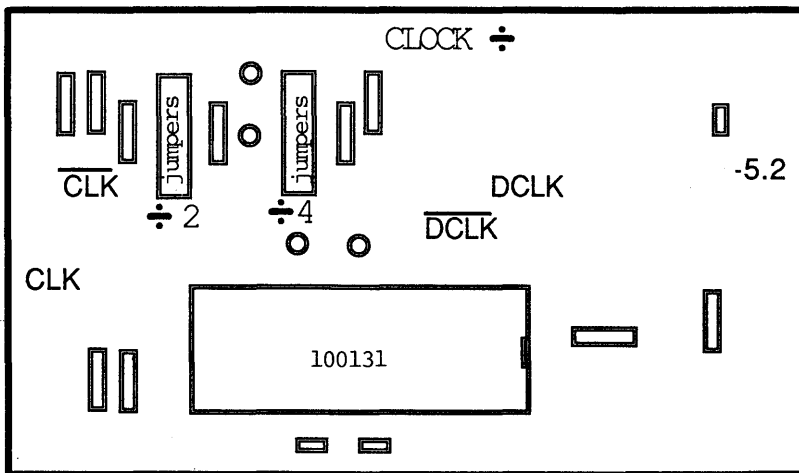
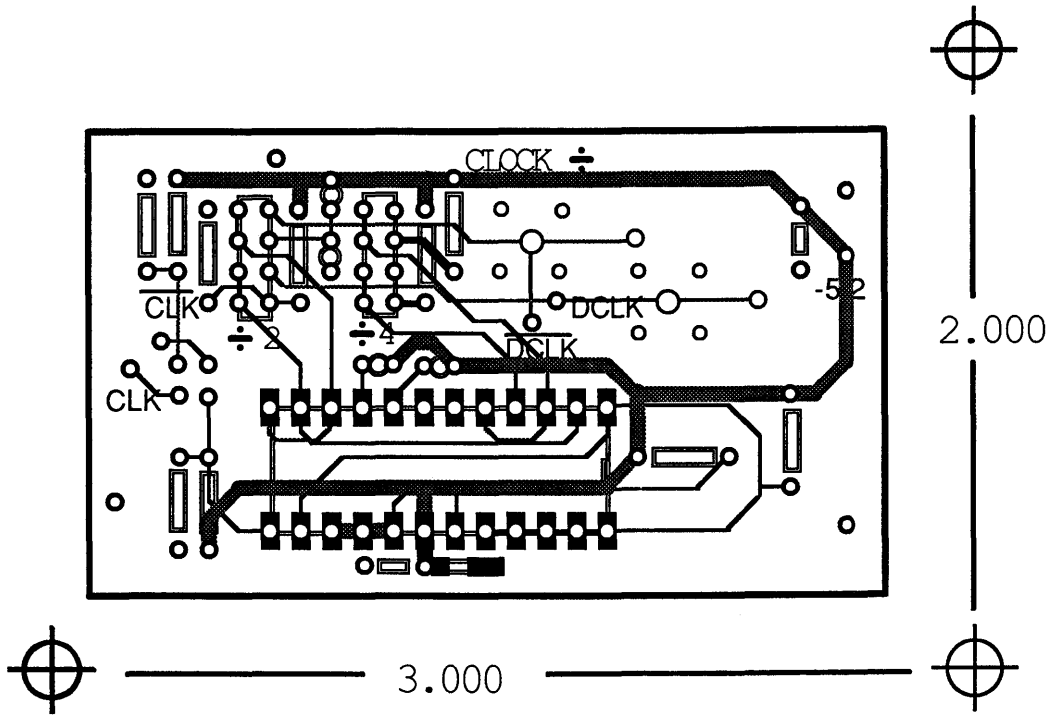


FIGURE 5 - CLOCK DIVIDER BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

EB100 REVISION C PARTS LIST

AN100

PARTS LIST			
NO.	DESCRIPTION	QTY.	MANUFACTURER / PART NO.
1	FERRITE BEAD	11	FAIR-RITE CORP.-2743001111
2	DIODE	4	1N4001
3	TRANSISTOR	1	MOTOROLA-2N5836
4	I.C.	1	HONEYWELL-HDAC10181A/B OR HDAC51400
5	I.C.	1	HONEYWELL-HCMP96870
6	I.C.	2	FAIRCHILD-F100155
7	I.C.	1	PMI-OP-11
8	I.C.	1	HONEYWELL-HADC77100B
9	I.C.	1	HARRIS-HA2539
10	FILTER	3	MINI-CIRCUITS-PLP-100
11	RESISTOR	1	240Ω, 2w
12	RESISTOR	1	56Ω, 1/2w
13	RESISTOR	1	6.8Ω, 1/8w
14	RESISTOR	7	10KΩ, 1/8w
15	SIP RESISTOR PACK	5	220/330Ω
16	RESISTOR	4	220Ω, 1/8w
17	RESISTOR	4	330Ω, 1/8w
18	RESISTOR	2	750Ω, 1/8w
19	RESISTOR	3	50Ω, 1/8w
20	RESISTOR	3	470Ω, 1/8w
21	RESISTOR	1	10Ω, 1/8w
22	RESISTOR	1	15.1Ω, 1/8w
23	RESISTOR	1	5kΩ, 1/8w
24	RESISTOR	1	1.5kΩ, 1/8w
25	POTENTIOMETER	2	BOURNS-1KΩ, 3329-H-102 & MOUSER-ME323-4290W-1kΩ
26	POTENTIOMETER	6	BOURNS-10KΩ, 3329-H-103
27	CONNECTOR, DIN	1	BELL IND.-905-72184C
28	CONNECTOR	1	MOLEX-09-18-5069
29	CAPACITOR, CHIP	16	JOHANSON-47pf 500R15N470JP4
30	CAPACITOR	10	SPRAGUE-1uf TANT, 35V
31	CAPACITOR	29	SPC TECHNOLOGY-0.1μf
32	CAPACITOR, ADJ	2	JOHANSON-47pF-9629
33	CONNECTOR, BNC	5	TRUMPETER-CBJ20, 50Ω
34	TEST POINTS	2	TEKTRONIX 131-2766-01, 136-0352-02
35	PIN RECEPTACLE	42	MILL MAX-0552-1-15-15-11-27-10-0
36	PIN SOCKET	9	SAMTEC-SL-132-G-12
37	SOCKET, 24PIN	1	SAMTEC-ICO-624-NGT
38	PRINTED CIRCUIT BOARD	1	HONEYWELL-EB100

EB100 CLOCK DIVIDER BOARD

NO.	DESCRIPTION	QTY.	MANUFACTURER / PART NO.
39	F100131	1	FAIRCHILD TRIPLE D-TYPE FLIP-FLOP
40	CAPACITOR	2	.1μF
41	TEST POINTS	2	TEKTRONIX 131-2766-01, 136-0352-02
42	RESISTOR	6	1KΩ, 1/8w 5%
43	RESISTOR	4	220Ω, 1/8w 5%
44	RESISTOR	4	330Ω, 1/8w 5%
45	CAPACITOR	1	JOHANSON-47pF CHIP
46	TEST POINTS	2	COMPONENTS CORP.-TP-102

EB102 REVISION B PARTS LIST

AN100

PARTS LIST				
NO.	REF. DESIG.	QTY.	DESCRIPTION	MANUFACTURER / PART NO.
1	C1, 3, 5, 8, 12, 13, 15	7	CAPACITOR, .1 μ f - 50V	AVX / SR205E104MAA
2	C2, 4, 7, 14	4	CAPACITOR, 47pf - CHIP	JOHANSON / 500R15N470JP4
3	C10, 11, (NOTE 3)	2	CAPACITOR, SEALTRIM 5-20pf	JOHANSON / 9629
4	CR1, 2	2	DIODE, 1N4001	
5	E1, 2	2	JUMPER PINS (HEADER STRIP)	CYPRESS / TSW-1-36-07-T-S
6	FL1	1	FILTER, 90MHz LOWPASS	MINICIRCUITS / PLP-100
7	J1, 2 (NOTE4)	2	RECEPTACLE, BNC	TRUMPETER / CBJ20
8	L1, 2	2	RF BEAD	FAIR-RITE / 2743001111/2
9	P1	1	PLUG	MOLEX / 09-18-5031
10	R1, 2	2	RESISTOR, 10K OHM	HAMILTON / AVNET / CF1/8-10K-5%-T/R
11	R4, 12	2	RESISTOR, 33 OHM	HAMILTON / AVNET / CF1/8-33-5%-T/R
12	R5	1	RESISTOR, 25K OHM	HAMILTON / AVNET / CF1/8-25K-5%-T/R
13	R7 (NOTE 1)	1	RESISTOR, 1.5K OHM	HAMILTON / AVNET / CF1/8-1.5K-5%-T/R
14	R7, 8 (NOTE 2)	2	RESISTOR, 250 OHM	HAMILTON / AVNET / CF1/8-250-5%-T/R
15	R9	1	RESISTOR, 150 OHM	HAMILTON / AVNET / CF1/8-150-5%-T/R
16	R10	1	RESISTOR, 51 OHM	HAMILTON / AVNET / CF1/8-51-5%-T/R
17	R3	1	POTENTIOMETER, 10K OHM	BOURNS / 3339-1-103
18	R6, 11	2	POTENTIOMETER, 1M OHM	BOURNS / 3339-1-106
19	C6, 9	2	CAPACITOR, 1 μ f TANT, 35V	SPRAGUE / 196 DIO5X9035HAI
20	U1 (NOTE 1)	1	I.C., OP-AMP	COMLINEAR / CLC221A1
21	U1 (NOTE 2)	1	I.C., BUFF-AMP	COMLINEAR / CLC231A1
22	PCB1	1	PRINTED CIRCUIT BOARD	HONEYWELL / EB102 REV. B

NOTES:

- 1) USE ITEM NO. 13 WITH ITEM NO. 20 AND JUMPER E1, 2.
- 2) USE ITEM NO. 14 WITH ITEM NO. 21.
- 3) USE C10 WITH ITEM NO. 21 ONLY.
- 4) J2 IS MOUNTED ON THE BACKSIDE OF PCB1.

8

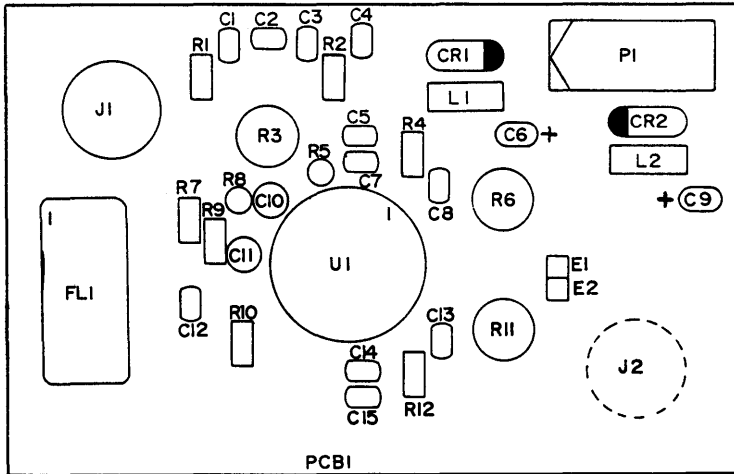
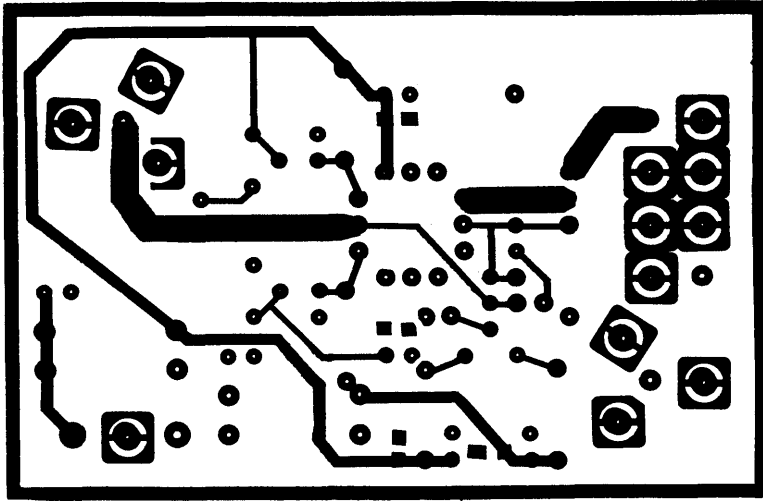


FIGURE 6 - EB102 BUFFER BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

SET-UP PROCEDURE FOR THE EB100 DEMONSTRATION BOARD

The following setup procedure is completed at Honeywell before the EB100 board is shipped to the customer. It is not necessary for the user to perform this exercise, but it is included for informational purposes.

The EB100 demonstration board is accompanied with a literature package containing the "AN100 APPLICATION NOTE", the "HAD77100", "HAD51400", "HAD10181", and "HCMP96870" data sheets, and an applications department business card. Also, a power harness, and a capacitor alignment tool are included. If there are any questions, please call the applications engineer on the card.

STEP 1

Connect the wire end of the power supply harness to power supplies as shown in Figure 1C. The power harness should be connected to the board with the bevelled edges and hollow connector aligned for correct operation.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

Table 3 (page 6) shows the power requirements for the EB100. Use the current gauges on the power supply or a DMM in line with the power lines and set on current (I). these current values will vary somewhat until all the potentiometers are adjusted. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

STEP 2

Refer to Figure 2 and 4 on the previous pages. Place a DMM probe (set to voltage selection) on the black jumpers at the input to the HAD77100 (E14). This should read -1V and is adjusted by turning potentiometer R23 (See Table 2A).

STEP 3

Again, refer to Figures 2 and 4 on the previous pages and Table 5 on this page. Place a DMM probe (set to voltage selection) on pin 3 of the OP11 and read approximately -1.2V. If it does not then check to see if the black jumpers for the HAD10181/51400 are set up

TABLE 5 - EQUIPMENT LIST

- 2- SIGNAL GENERATORS CAPABLE OF PRODUCING 1MHZ AND 20MHZ SINEWAVES AT UP TO 1Vp-p OUTPUT LEVELS INTO 50Ω. H.P. 8656A OR EQUIVALENT.
- 1- OSCILLISCOPE, EITHER H.P. DIGITIZING OSCILLISCOPE MODEL 54100D OR EQUIVALENT OR TEKTRONIX MODEL 2465.
- 1- DIGITAL MULTIMETER(DMM), KEITHLEY 197 OR EQUIVALENT.
- 4- POWER SUPPLIES CAPABLE OF PRODUCING THE POWER LISTED IN TABLE 1. 2 LAMBDA LPT-7202-FM OR EQUIVALENT.
- 5- 50Ω COAX CABLES (RG58) WITH BNC TYPE CONNECTORS.
- 1- HIGH IMPEDANCE PROBE (1MΩ) - TEKTRONIX OR H.P.

for the right part (see Figure 4B). Next set the probe on pin 1 of the OP11. This should read -2V and is adjusted by turning potentiometer R26. Now set the probe on pin 7 of the OP11. This should read approximately -1V and is adjusted by potentiometer R35. Pin 8 of the OP11 should read approximately -50mV and is adjusted by potentiometer R32.

STEP 4

Refer to Figures 2 and 4. Attach a 50Ω BNC cable to the "CLK IN" BNC connector. Attach the other end to a sinewave or signal generator set at 20MHz frequency and 1Vp-p amplitude (if 1Vp-p is not available, amplitudes down to 100mVp-p are acceptable). Put a Tektronix or H.P. high impedance probe in one or both of the probe jacks immediately below the HCMP96870 comparator. Adjust potentiometer R5 to achieve a 50% duty cycle square wave (both "high" and "low" states are the same length). Adjust potentiometer R4 if no waveform is present and/or to get rid of any jitter in the square wave (this is a hysteresis adjustment). The square wave amplitude should be approximately 900mVp-p and look like Figure 7 below.

STEP 5

Refer to Figure 2 and 4. Attach a 50Ω coax cable to the BNC connector marked "BUFFER IN". Use a second sinewave or signal generator set at 1 MHz frequency and 1Vp-p amplitude (See Figure 8). Attach another cable to the BNC connector "A/D IN / BUFFER OUT" and to an oscilloscope set at 50Ω input impedance. A 200mVp-p amplitude signal swinging around -100mVdc should appear at a 1MHz frequency (See Figure 9). If oscillation is evident (erratic signal amplitude or wrong frequency), potentiometer and capacitor C44 must be adjusted as well as capacitor C25. Adjust capacitor C25 first to minimize the oscillation. If this does not work, set it at the lowest amplitude oscillation and adjust potentiometer R22. Adjust potentiometer R22 to midturn and then adjust capacitor C44 until the oscillation stops. See Figures 10, 11, and 12.

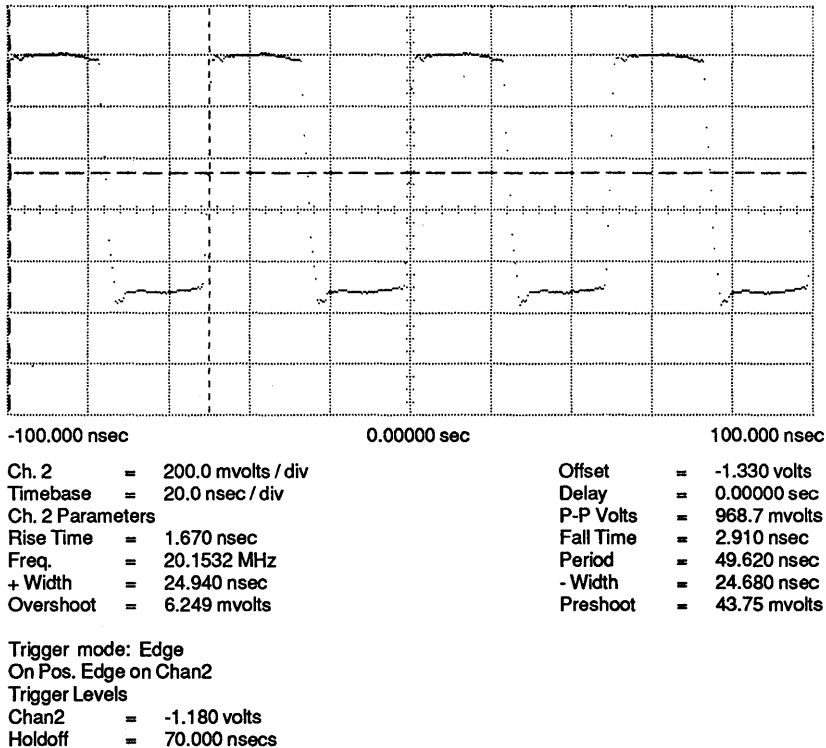
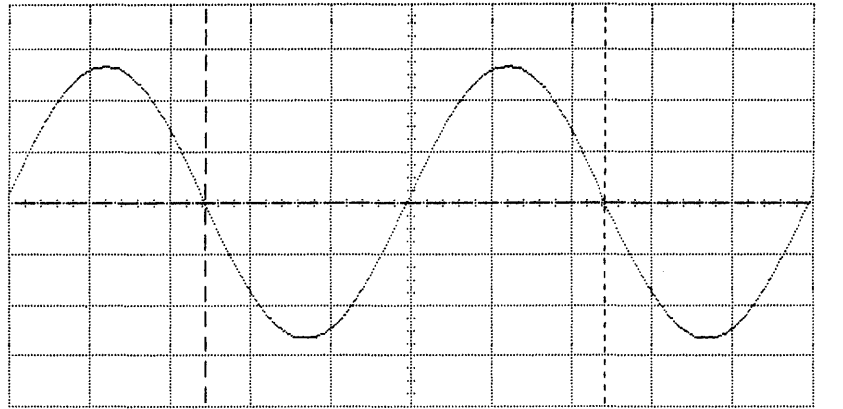


FIGURE 7 - CLOCK OUTPUT AT THE TEKTRONIX PROBE JACKS

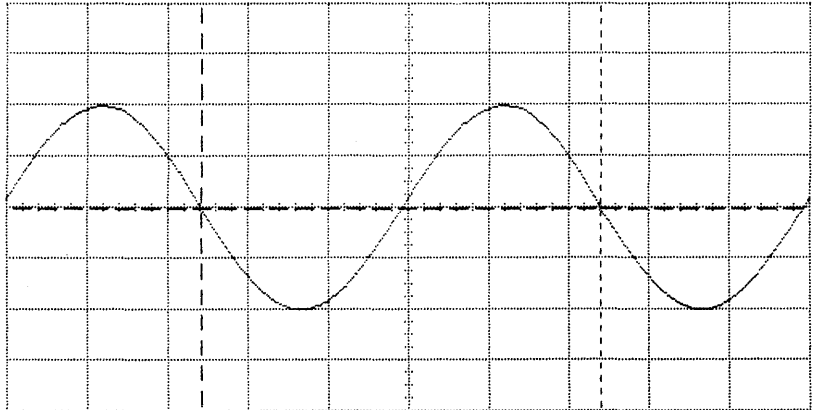
FIGURE 8 - INPUT SIGNAL TO THE BOARD (50Ω INPUT IMPEDANCE)



-1.00000 usec	0.00000 sec	1.00000 usec
Ch. 1 = 200.0 mvolts / div		Offset = 0.000 volts
Timebase = 200 nsec / div		Delay = 0.00000 sec
Ch. 1 Parameters		P-P Volts = 1.062 volts
Rise Time = 289.640 nsec		Fall Time = 289.320 nsec
Freq. = 1.00014 MHz		Period = 999.860 nsec
+ Width = 497.520 nsec		- Width = 502.340 nsec
Overshoot = 6.249 mvolts		Preshoot = 6.249 mvolts

Trigger mode: Edge
 On Pos. Edge on Chan1
 Trigger Levels
 Chan1 = 0.000 volts
 Holdoff = 70.000 nsecs

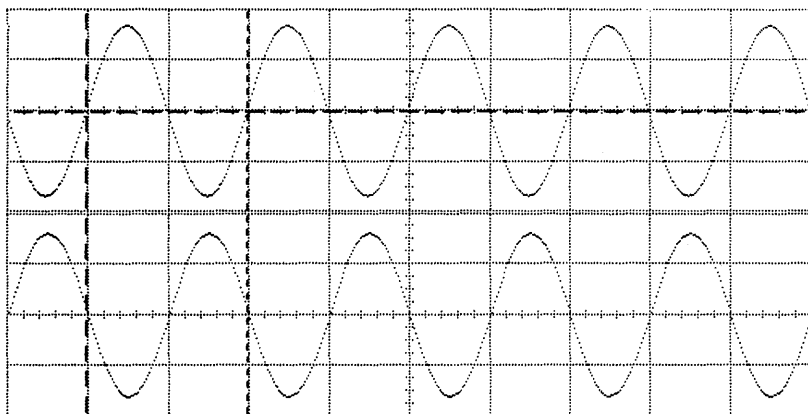
FIGURE 9 - OUTPUT SIGNAL FROM THE "BUFFER OUT" BNC CONNECTOR (50Ω IMPEDANCE)



-1.00000 usec	0.00000 sec	1.00000 usec
Ch. 1 = 50.00 mvolts / div		Offset = -100.0 mvolts
Timebase = 200 nsec / div		Delay = 0.00000 sec
Ch. 1 Parameters		P-P Volts = 200.0 mvolts
Rise Time = 294.080 nsec		Fall Time = 289.910 nsec
Freq. = 997.904 KHz		Period = 1.00210 usec
+ Width = 499.810 nsec		- Width = 502.290 nsec
Overshoot = 1.562 mvolts		Preshoot = 1.562 mvolts

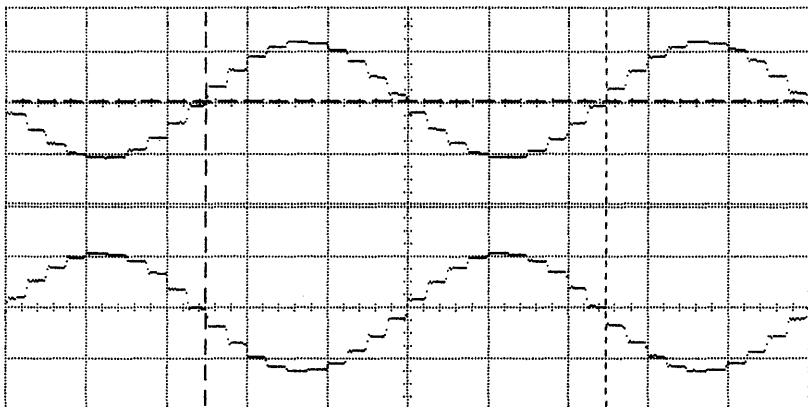
Trigger mode: Edge
 On Pos. Edge on Chan1
 Trigger Levels
 Chan1 = -100.0 mvolts
 Holdoff = 70.000 nsecs

FIGURE 12 - OSCILLATION HAS STOPPED AND THE BOTTOM WAVE-FORM IS THE SAME SHAPE AS THE TOP WAVEFORM BUT IS INVERTED



-2.50000 usec	0.00000 sec	2.50000 usec
Ch. 1 = 200.0 mvolts / div		Offset = 0.000 volts
Ch. 2 = 40.00 mvolts / div		Offset = -102.0 mvolts
Timebase = 500 nsec / div		Delay = 0.00000 sec
Ch. 1 Parameters		P-P Volts = 665.6 mvolts
Rise Time = 290.790 nsec		Fall Time = 291.830 nsec
Freq. = 999.990 KHz		Period = 1.00001 usec
+ Width = 500.180 nsec		- Width = 499.830 nsec
Overshoot = 0.000 volts		Preshoot = 0.000 volts

FIGURE 13 - OUTPUT WAVEFORMS FROM "OUT-" AND "OUT+" WITHOUT THE CLOCK DIVIDER BOARD INSERTED AND THE CLOCK JUMPERS CONNECTED AS SHOWN IN THE TOP OF FIGURE 4



-1.00000 usec	0.00000 sec	1.00000 usec
Ch. 1 = 400.0 mvolts / div		Offset = -964.0 mvolts
Ch. 2 = 400.0 mvolts / div		Offset = -544.0 mvolts
Timebase = 200 nsec / div		Delay = 0.00000 sec
Ch. 1 Parameters		P-P Volts = 912.5 mvolts
Rise Time = 290.470 nsec		Fall Time = 297.770 nsec
Freq. = 1.00264 MHz		Period = 997.370 nsec
+ Width = 499.250 nsec		- Width = 498.120 nsec
Overshoot = 6.249 mvolts		Preshoot = 6.249 mvolts

Trigger mode: Edge
 On Neg. Edge on Chan1
 Trigger Levels
 Chan1 = -964.0 mvolts
 Holdoff = 70.000 nsecs

STEP 6

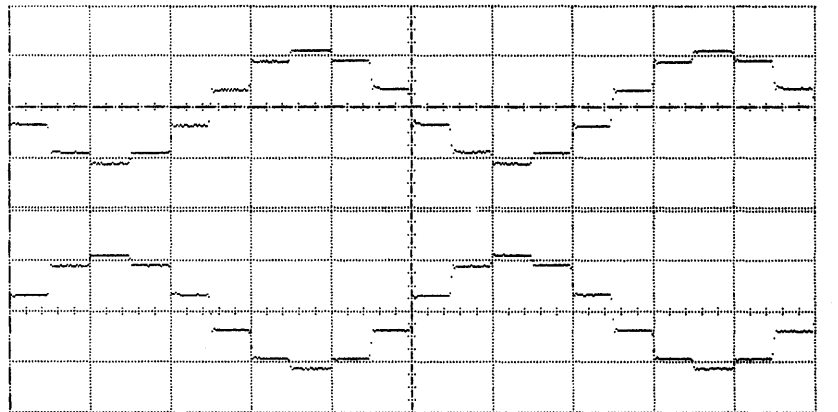
This measurement is done without the clock divider board connected and clock jumpers inserted as shown in the top of Figure 4. Again referring to Figures 2 and 4, attach a 50Ω coax cable to the BNC connector marked "OUT-" and another cable to "OUT+". Attach the other end to an oscilloscope set to 50Ω input impedance. The outputs should be the opposite of each other and at approximately a 900mV amplitude. Adjust potentiometer

R36 to achieve this level. Do not adjust too far or the signal will start deteriorating. See Figure 13. After completing step 6, remove one end of each "clock jumper" wire and leave the other end soldered to the board.

STEP 7

Insert the clock divider board and connect the shorting jumpers to the posts in the +2 configuration and compare to the waveform in Figure 14.

FIGURE 14 - "OUT-" AND "OUT+" WITH THE CLOCK DIVIDER BOARD INSERTED AND SET AT +2 MODE



-1.00000 usec

0.00000 sec

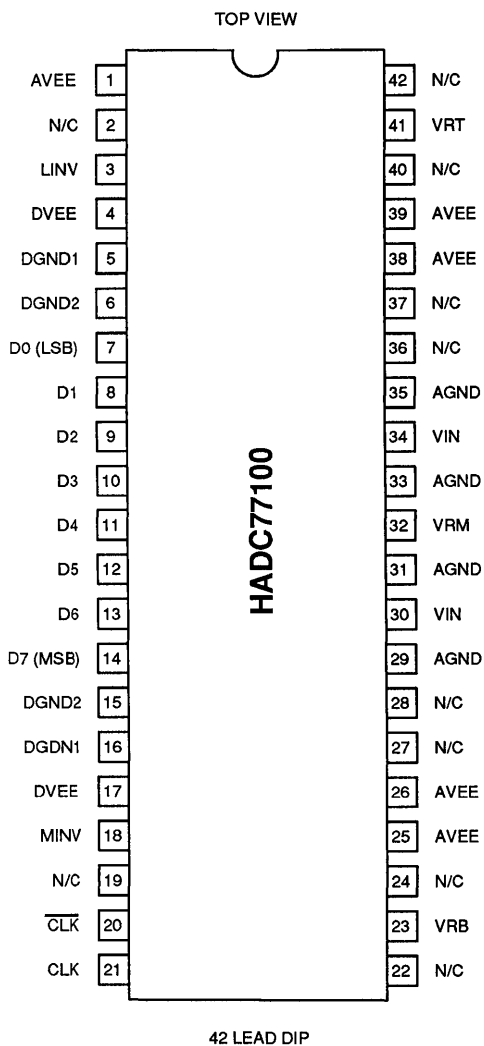
1.00000 usec

Ch. 1 = 400.0 mvolts / div
 Ch. 2 = 400.0 mvolts / div
 Timebase = 200 nsec / div
 Ch. 1 Parameters
 Rise Time = 201.240 nsec
 Freq. = 1.00255 MHz
 + Width = 499.050 nsec
 Overshoot = 100.0 mvolts

Offset = -936.0 mvolts
 Offset = -576.0 mvolts
 Delay = 0.00000 sec
 P-P Volts = 912.5 mvolts
 Fall Time = 201.350 nsec
 Period = 997.460 nsec
 - Width = 498.410 nsec
 Preshoot = 100.0 mvolts

Trigger mode: Edge
 On Neg. Edge on Chan1
 Trigger Levels
 Chan1 = -936.0 mvolts
 Holdoff = 70.000 nsecs

PIN ASSIGNMENTS HADC77100



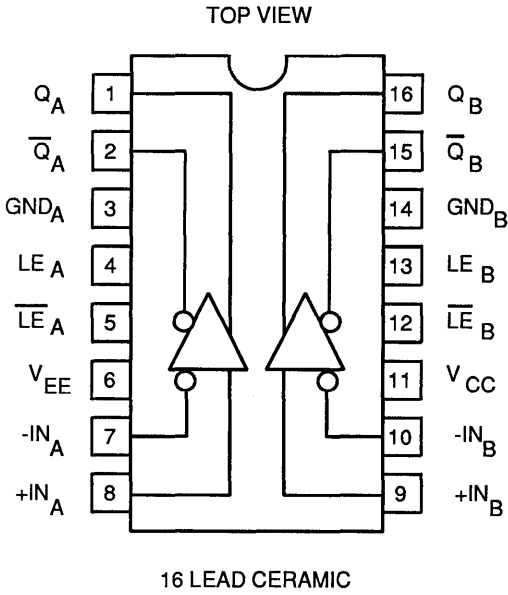
PIN FUNCTIONS HADC77100

NAME	FUNCTION
AVEE	Negative Analog Supply Nominally -5.2V
LINV	D0 through D6 Output Inversion Control Pin
DVEE	Digital Analog Supply Nominally -5.2V
DGND1	Digital Ground 1
DGND2	Digital Ground 2
D0	Digital Data Output (LSB)
D1 - D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control Pin
$\overline{\text{CLK}}$	ECL Clock Input Pin
CLK	ECL Clock Input Pin
VRB	Reference Voltage Bottom Nominally -2.0V
AGND	Analog Ground
VIN	Analog Input (can be connected to the input signal or used as Sense)
VRM	Reference Voltage Tap Middle
VIN	Analog Input (can be connected to the input signal or used as Sense)
VRT	Reference Voltage, Top Nominally 0.0V

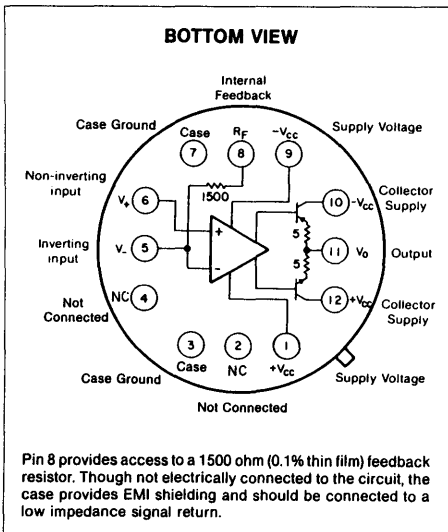
FIGURE 8B
PIN ASSIGNMENTS HCMP96870

PIN FUNCTIONS HCMP96870

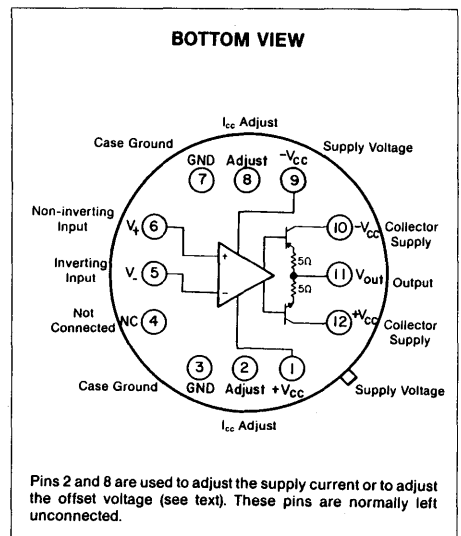
AN100



NAME	FUNCTION
\bar{Q}_A	Output A
Q_A	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
\bar{LE}_A	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Inverted Latch Enable B
\bar{LE}_B	Latch Enable B
GND_B	Ground B
\bar{Q}_B	Inverted Output B
Q_B	Output B



PIN ASSIGNMENTS
COMLINEAR CLC221

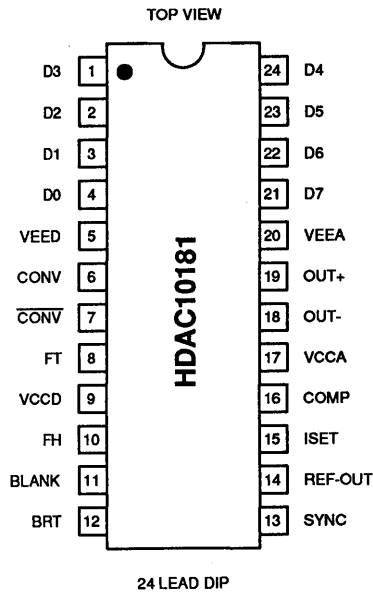


PIN ASSIGNMENTS
COMLINEAR CLC231

8

PIN ASSIGNMENTS HDAC10181

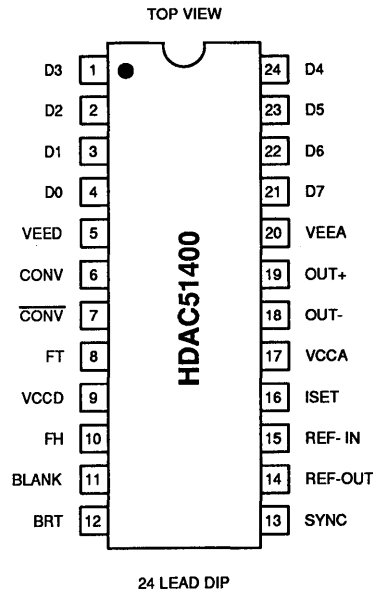
AN100



PIN FUNCTIONS HDAC10181

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
ISET	Reference Current + Input
COMP	Compensation Input
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

PIN ASSIGNMENTS HDAC51400



PIN FUNCTIONS HDAC51400

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
REF-IN	Reference Input
ISET	Reference Current
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

**SIGNAL PROCESSING TECHNOLOGY'S
PARALLEL ANALOG TO DIGITAL CONVERTERS,
by STEVE SOCKOLOV MARKETING MANAGER**

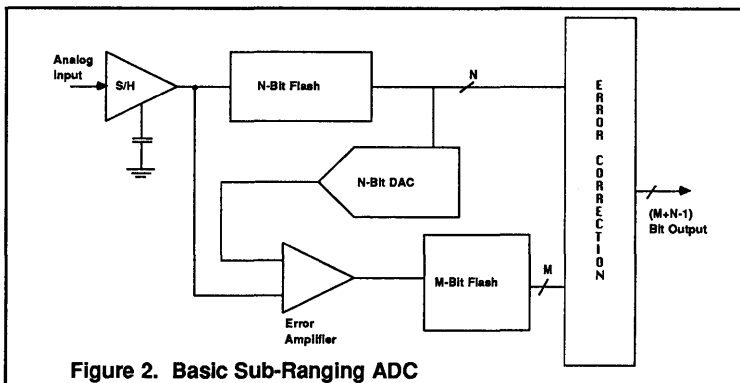
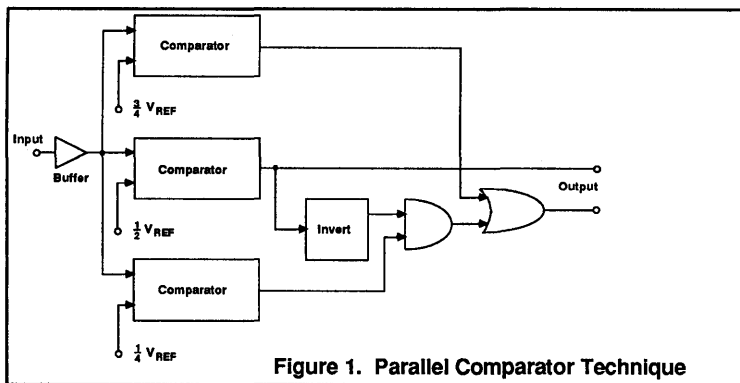
GENERAL

The fastest type of analog to digital converter known at this time is the parallel or flash converter. This type of converter (see Figure 1) has one comparator for each possible output code. This results in the fact that there are 2^N or 2^{N-1} comparators for an "N"-bit flash converter. The difference between the two numbers of comparators depends on whether or not an overrange bit is included. This can be a very large number of comparators, to fit on a single die, for values of N greater than eight.

Flash converters are now available with up to 10 bits of resolution. There are also products available that are called flash converters, but are actually a variation known as "two-step" flash converters. Almost all data sheets that now claim to have 10- or 11- bit flash converters, and even some lower resolution converters, are not true parallel converters with 2^{N-1}

comparators. These converters (see Figure 2) go by a variety of names including two-step, sub-ranging, half flash, feed forward and series/parallel converters. "Two-step" or sub-ranging converters require a different system design approach than parallel flash converters and require extra support circuits in many applications. A major advantage of these sub-ranging architectures is that they should cost less than a comparable full parallel type. Disadvantages include the need for a sample and hold (unless it is included on the device) and their problems with dynamic performance over processing and temperature have not yet been solved.

Flash converters are currently available with 4 to 10 bits of resolution with 8 bits being by far the most common configuration. There are several trade-offs that are made as resolution is increased. These are,



for a given process, as the resolution is increased and if the basic design is unchanged the speed may decrease slightly, input capacitance will almost double for each bit added, power will go up and cost will increase due to die size and the associated effect on yields. It is for all of these reasons that there are no flashes with greater than 10 bits of resolution available today.

DESCRIPTIONS

Honeywell's 8-bit flash converters, the HADC77100, 77200 and 77300 (see Figures 3A and 3B) have an input structure that improves their performance over previous flash converter designs. This structure is the inclusion of a preamplifier with inputs connected to the resistor ladder and the analog inputs of each of the 256 comparators.

After the comparator outputs (see Figure 4) the structure of the HADC77100 family of converters is similar to many other 8-bit flash converters. They are configured in four columns, each of which functions as a 6-bit converter. The outputs of each column are then

logically combined to generate the 8-bit output. Output coding can be controlled by the Most Significant Bit Invert (MINV for bit D7) line and the Least Significant Bits Invert (LINV for bits D0 through D6) line.

Figure 5 shows a macro block diagram of Honeywell's 10-bit high speed flash converter. The analog signal enters the preamplifier/comparator front end and is digitized by the comparators into a "thermometer" code. After the comparators there are 16 blocks of 64 "thermometer" code to Gray code converters. This block also contains new patented circuitry to eliminate metastable states. Gray coding was chosen because it reduces glitches and digital noise caused by switching transients and glitches caused by "OR'ing" more than 1 code. The results are reduced signature effects and improved dynamic performance. Following this first decode are the column latches. After the latches the MSBs and the overrange bits of each of the 16 banks are decoded to form the 4 MSBs. In parallel with this, the 6 LSBs from each of the 16 banks are OR'ed to form the 6 LSBs.

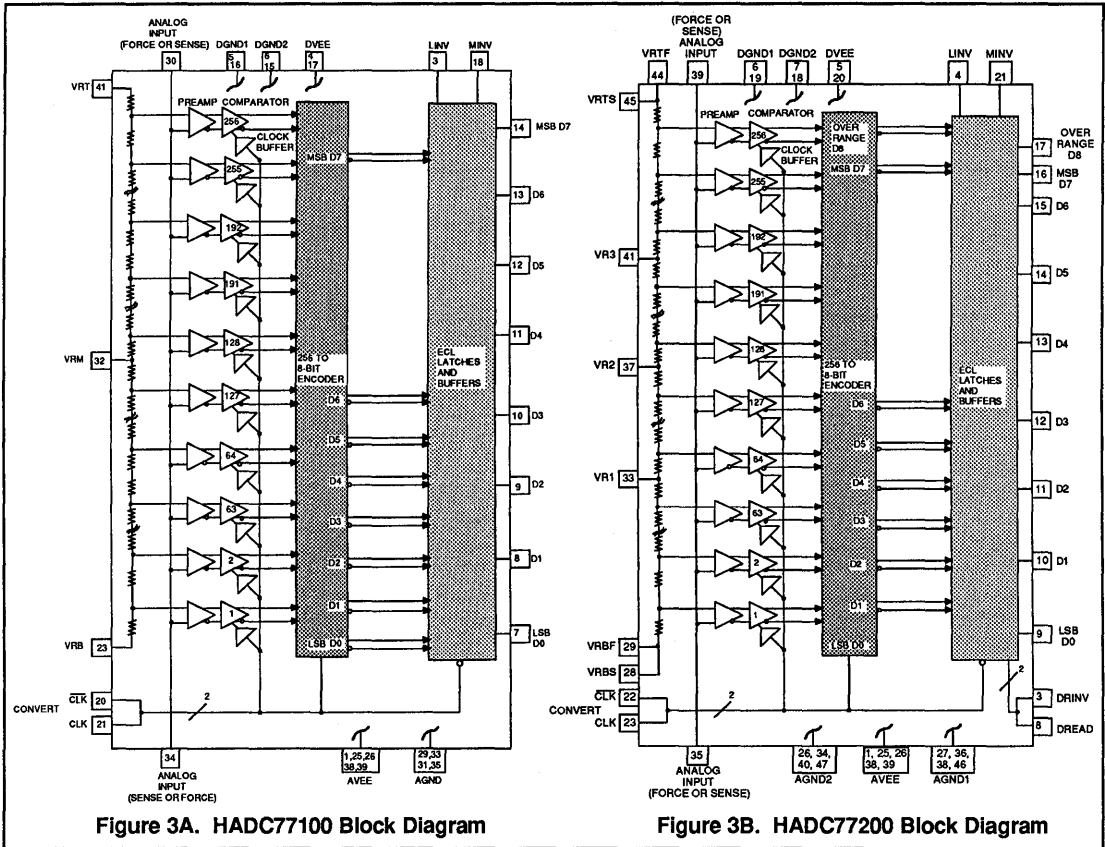


Figure 3A. HADC77100 Block Diagram

Figure 3B. HADC77200 Block Diagram

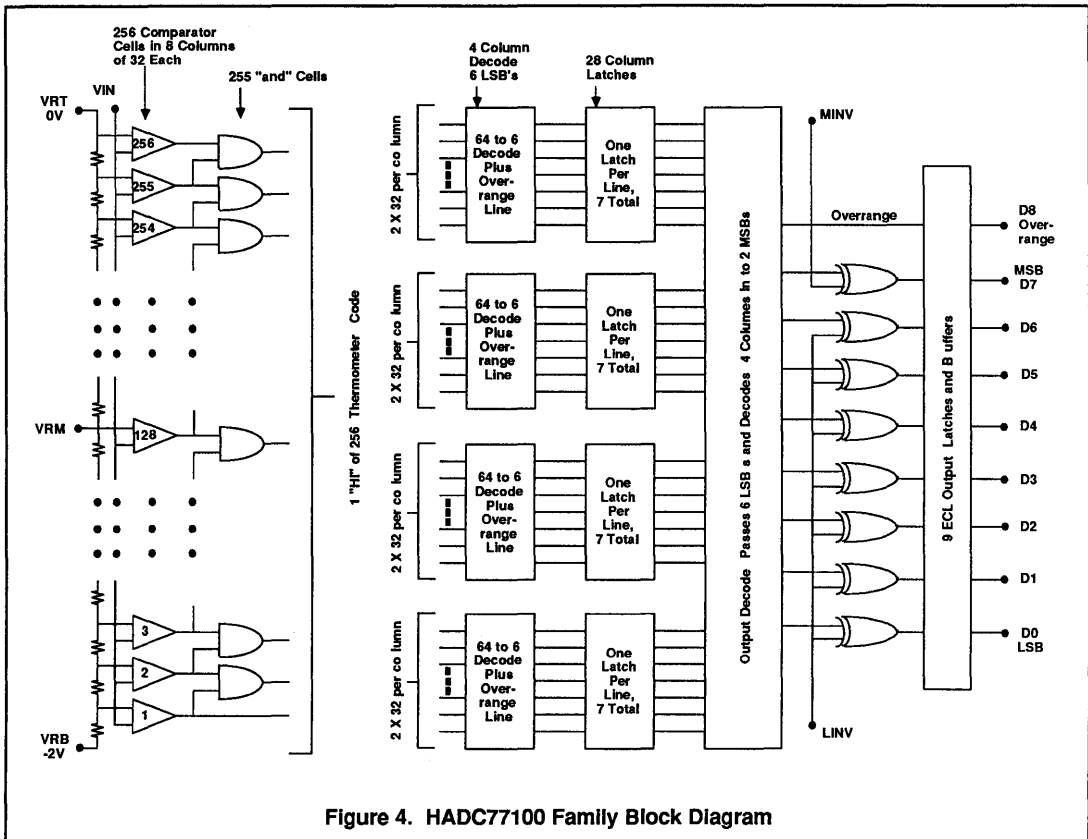


Figure 4. HADC77100 Family Block Diagram

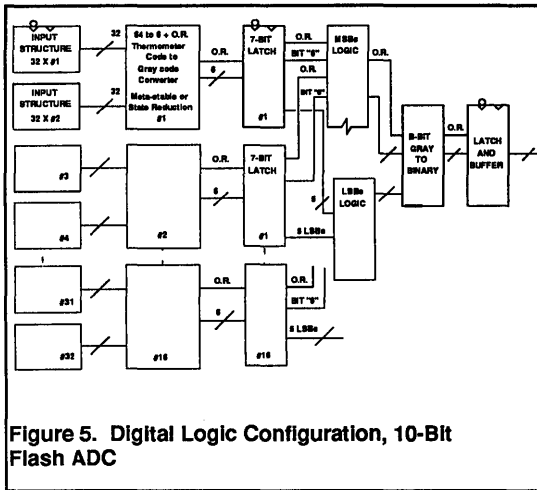
Following this first decode are the column latches. After the latches the MSBs and the overrange bits of each of the 16 banks are decoded to form the 4 MSBs. In parallel with this, the 6 LSBs from each of the 16 banks are ORed to form the 6 LSBs. All coding has been Gray code to this point and in the next block it is decoded to binary. Control bits are available to invert either the MSB and/or the LSBs to generate other common codes such as two's complement or offset binary. The final block contains the output latches and buffers.

INPUT STRUCTURE

There are two inputs to all of Honeywell's flash converters. These inputs are connected to a single point internally so they may be either tied together externally, or used as force and sense lines. Using the force and sense approach will take the effect of the lead inductance out of the input. This would not be much of an advantage at bandwidths below 50 MHz. But it will be useful at higher frequencies. Connected

directly to the inputs are the preamplifiers. The purpose of these preamplifiers is to reduce both kickback currents and the possibility of metastable states. These input amplifiers have a very high gain bandwidth product which results in greatly improved dynamic performance (over previous flash converters). Part of this improvement comes by providing gain prior to the comparator increasing its overdrive, thus reducing the chances for metastable states. Following the input to the preamplifiers the entire circuit to the output latches is differential to reduce clock synchronous noise.

Input capacitance is a very critical parameter to the users of high speed ADCs. In the best of cases this capacitance would be both low and constant. The greater the capacitance, the greater the drive requirements of the signal source and if it varies over input voltage, as it does in most semiconductor devices, then the compensation of the driving amplifier must be designed to account for the worst case. When reading input capacitance on data sheets pay



attention to the test conditions. Semiconductors have the highest capacitance with the lowest voltage across them. For worst case designs with ECL compatible converters V_{IN} is at 0.0 Volts.

In some cases, especially in testing, the converter is driven from 50 Ohm sources and this can cause a pole to appear at the input caused by the 50 Ohms in series with the input capacitance. Another characteristic of input capacitance is that it can vary with input frequency and/or input voltage. Signal Processing Technology's converter input capacitance varies only a few pico Farads with either frequency or voltage within its specified operating range.

RANDOM ERRORS -- SPARKLE CODES, GLITCHES AND METASTABLE STATES

In an ideal flash converter every comparator will be in a defined logic state (either a "0" or a "1") at the time that the latches are strobed. At the strobe all of the comparators below the input voltage would be "off" and all of the comparators above the input voltage would be "on." This is the "thermometer" code that was previously referred to.

It is possible to strobe the comparators while one of them is in its linear region. This would cause the decode logic to possibly enter either an undefined state or not have time to change states. This could result in the decode logic equation (see Figure 6) such as $A+B+C+?+E+F+G$ for the 3-bit converter shown in this example. Since the logic has been minimized to only implement the set of equations shown in Table 1, the output would be erroneous. This erroneous data is the result of a metastable state.

TABLE 1
3-BIT FLASH CONVERTER

LOGIC EQUATION	BINARY	GRAY
$\bar{A} + \bar{B} + \bar{C} + \bar{D} + \bar{E} + \bar{F} + \bar{G}$	= 000	000
$\bar{A} + \bar{B} + \bar{C} + \bar{D} + \bar{E} + \bar{F} + G$	= 001	001
$\bar{A} + \bar{B} + \bar{C} + \bar{D} + \bar{E} + F + G$	= 010	011
$\bar{A} + \bar{B} + \bar{C} + \bar{D} + E + F + G$	= 011	010
$\bar{A} + \bar{B} + \bar{C} + D + E + F + G$	= 100	110
$\bar{A} + \bar{B} + C + D + E + F + G$	= 101	100
$\bar{A} + B + C + D + E + F + G$	= 110	101
$A + B + C + D + E + F + G$	= 111	111

Another possible decode error that could result is due to differences in propagation delays and offsets of the individual comparators. These differences could result in a comparator output such as $A+B+C+D+E+F+G$. Again, the decode logic has not been designed to solve this equation and could produce erroneous data. These types of errors are often referred to as sparkle code or glitches.

Both of these error sources may appear to be random and appear as incorrect output data when compared to the analog input. Possibilities of the errors caused by metastable states increase exponentially with increased clock speeds. Sparkle codes, caused by differences in propagation delays and offsets, may appear to be random but are repeatable for given clock frequencies and input conditions. This type of error often appears as a signature error. Signature errors are caused by the way the internal structure is partitioned or laid out. An example would be if the internal structure were partitioned into blocks of eight banks of comparators, then at eighth scale intervals there may be either wider or narrower codes than those that exist at other codes. These signature errors can appear with DC inputs, but are more commonly seen at higher frequencies.

Honeywell has added proprietary logic (patent applied for) after the comparators in the 10-bit flash converter to reduce metastable states, for a given frequency, to the LSB level. The preamplifiers in the HADC77100 family flash converter reduce the metastable error rate by a theoretical factor of six. Signature effects in all Honeywell flash converter designs have also been reduced to a minimum.

DIGITAL I/O AND INTERNAL LOGIC

All digital inputs, outputs, and clock signals are ECL compatible. ECL was chosen for its low switching noise and its fast clock edges. The fast differential clocks reduce aperture width and jitter. The room temperature specifications for all ECL logic levels are the same as Motorola's 10KH, but they have been designed to operate over the full military temperature range of the converter.

Internal logic is fully differential Current Mode Logic. This is a very high speed, low power logic that has proven performance in high speed converters.

Outputs of the 10-bit flash are specified terminated to 100 Ohms. This will be to save power, since the speed of 50 Ohm termination is not required at its rated speed. Outputs of the 8-bit, 125MHz and above converters are specified with 50 Ohm termination.

CLOCKING

At this time all of Honeywell's flash converters are driven by differential ECL clocks. We realize that slower converters may be in systems that are totally TTL compatible. But in order to assure optimum performance, ECL clocks have been chosen. The relatively slow edges of TTL signals could cause hundreds of picoseconds of aperture jitter, unacceptable performance for high speed systems. Differential clocks also provide better system noise performance.

For Honeywell's flash converters clock duty cycles are designed to be 50% for the highest operating speeds. Duty cycles of 50% were chosen because they are easy to generate and are useful in applications such as ping-ponging. At sample rates below maximum, clock duty cycle is not important to the device operation. What is important at any sample rate is to assure that at least the minimum pulse width is maintained.

Clock inputs were designed to accept differential ECL levels but they may be driven in a variety of different ways. Care must be taken to assure that the method of clock driving is commensurate with the application and temperature range required. For applications where aperture delay is not a critical concern, the clock may be driven single-ended. An ECL signal, or a sine wave with ECL levels may be fed to one of the clock inputs and the other input would be tied to the ECL threshold of approximately -1.3V. The disadvantage of this method is that due to V_{BB} shifts with temperature, the aperture delay will shift $15ps/^{\circ}C$ (for the HADC77100) from a typical value of 1.8ns at $25^{\circ}C$. This temperature dependent shift is designed to track MECL 10KH logic

and can be driven single-ended without problems when driven from 10KH logic. For aperture delay critical requirements such as when the converter is used in conjunction with a track and hold or when phase information must be maintained, then differential clocking should be used. This will have much better stability ($7ps/^{\circ}C$) over temperature.

Tracking of different devices over temperature appears to be very good with almost no difference from device to device in the few HADC77100s that have been measured.

Because the inputs to the internal clock drivers have a gain stage in front of them, signals less than full ECL levels may also be used. Differential signals of greater than $\pm 100mV$ are adequate.

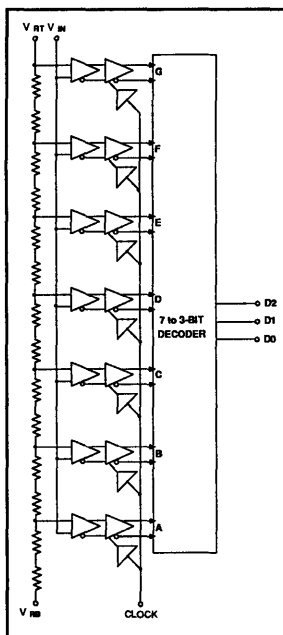


Figure 6. 3-Bit Parallel Converter Example

SPECIFICATIONS AND TESTING

All data sheet specifications with minimums or maximums will be tested at the temperatures specified unless otherwise noted. Those that have only typical numbers Honeywell intends to characterize, but not test. Honeywell's data sheets also include a Test Level to specify how the devices are tested.

Testing of flash converters at full operating speeds is extremely complicated. Honeywell uses an automated test system to perform all of the production tests on these devices. Characterization is performed using the test equipment shown in Figure 7. Since testing is so complex and costly, the user may wish to consider using Honeywell's evaluation board with bench top test equipment for incoming sample tests.

There are several tests listed in the specifications that may need explanations. It is important to understand that these devices attain new levels of performance,

and Honeywell believes that traditional analog to digital converter specifications such as gain and linearity are not the only specifications needed for high speed system design. These specifications are static and therefore are applicable to input signals that are at or near DC. Perhaps one could test a parameter such as linearity at a given frequency. This can be done using histogram testing. Another test that can be performed is a RMS sine wave curve fit. This is often referred to as "effective bits." This is a dynamic test that measures the sum of several errors and relates them to the fidelity of a sine wave.

OFFSET TESTING

Because these converters have two references, one at the top and the other at the bottom of the ladder, the traditional gain and offset specifications do not apply. Honeywell's specifications contain two offset specifications, one for each end of the ladder. The following is an example of testing for these offsets using an 8-bit converter. Any other flash converter with two reference inputs could be tested similarly using different values. Offsets will be tested by applying V_{REF+} (0.000V for the 8-bit converters) to the input and increasing the positive reference from an arbitrary voltage, say -0.100V, and finding the code transition to full scale. The difference between the voltage at which the transition occurs, plus $1/2$ LSB (3.91mV), and 0.000V is the V_{RT} offset. The V_{RB} offset will be determined in a similar manner with an input voltage of -2.000V.

DYNAMIC TESTING

The following are brief explanations of some of the dynamic tests that Honeywell performs when evaluating flash converters. For more complete explanations consult Hewlett Packard's product note 5180A-2 "Dynamic Testing of A to D Converters."

HISTOGRAM TESTING:

In this test a full scale sine wave is input to the ADC and many samples (perhaps 100,000) are taken. Then the number of times each code appears is plotted. Since a sine wave is slowest at its extremes the number of codes for zero scale and full scale are the greatest. This should make a graph with a flattened "U" shape. Honeywell's data does not exhibit this shape because the data has been normalized. This test can be conducted at different input frequencies to show response over the full dynamic range of the converter. This test can give data on differential linearity, integral linearity, mean differential linearity, RMS differential, and on the number of missing codes. The mean differential linearity is the sum of all of the differential errors. Ideally, it should be zero. Most flash converters come very close to this value at DC because this parameter measures the magnitude of the sum of superposition errors. As the analog input slew rate increases this error also increases. This is probably due to dynamic currents in the ladder.

Histogram testing does have one weakness. It measures only the number of occurrences of each code and not the order of them. For this reason, it is possible to have random errors or missing codes and because the test averages many data points a code may appear wider or narrower than it actually is.

An alternative to sine wave testing is triangle wave testing. This signal would give a very good indication of the performance of the ADC because every comparator would be tested at maximum slew rate. The difficulty with this type of test is generating a triangle wave with a very high frequency.

Square wave testing can also be used to evaluate flash converters. This test measures step response. Evaluation with square waves should be performed on flash converters whenever their input is being driven from either a multiplexer, sample and hold or will, by the nature of the input signal, be required to have good step response.

RMS DIFFERENTIAL LINEARITY ERROR:

The square root of the sum of the squares of the differential non-linearities. This error term can be an indication of the signal-to-noise ratio of the converter. The device numbered 153 shows a part that has .2 LSB of RMS DL at 10MHz and 47.5dB of SNR at the same frequency. Another device measured .28 LSB and 45.68dB at the same frequency. However, this relationship only holds true for devices that have randomly distributed DNL errors. Those with large spikes may have SNRs that are so poor they are unmeasurable.

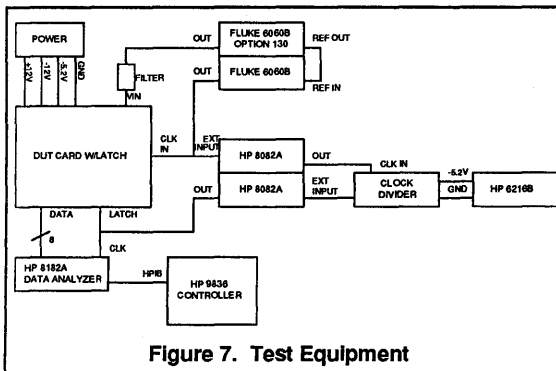


Figure 7. Test Equipment

SINE WAVE CURVE FIT (Effective Bits):

Testing flash ADCs for sine wave curve fit provides a quantitative value that represents the RMS sum of four error sources. These error sources are DNL, IL, aperture uncertainty and noise. This value could be useful in predicting over-all system performance. To adequately test performance, the converter should be tested with sample and input frequencies selected to change the output at least 1 LSB every clock cycle. This yields much more useful data about the actual performance of the converter than testing with a much lower beat frequency.

Many articles give a formula for calculating effective bits from the Total Error. This formula is given as:

$$\text{Total Error (dB)} = 1.8 + 6.02N (\text{Eff. Bits})$$

This formula will only be true in cases where the signal is a full scale sine wave. Other literature may use SNR in this formula.

To select the beat frequency for testing the converter at its full sampling frequency with the input at the Nyquist frequency, use the following formula:

$$\frac{f_s}{2^N} = \pi f_B$$

Where f_B = Beat frequency,
 f_s = Sample frequency,
 N = Number of bits.

Using the above sampling technique will exercise all digital outputs and assure one LSB code change for each clock cycle. If the application requires that the analog input be able to slew at maximum slew rate for any input, then testing using a triangle wave may be more appropriate.

FFT TESTING:

Discrete Fourier Transform testing can be used to evaluate the dynamic performance of an ADC for Signal-to-Noise Ratio (SNR) and Harmonic distortion. Honeywell defines Total Harmonic Distortion (THD) as the sum of the second through the ninth (though it is usually dominated by 2nd and 3rd) harmonics, and SNR is any remaining signal. The sum of these two parameters is the Total Dynamic Error and it is this value that can be used to calculate sine wave curve fit. These parameters are excellent indicators of flash converter performance. Signal-to-Noise Ratio is one test that needs to be carefully watched because if there are any glitches in the data the repeatability of the test is poor. This test can be used with confidence

at lower analog input bandwidths where there is a low probability of glitches but it must be used carefully when near the limit of flash converter performance.

FILTERS

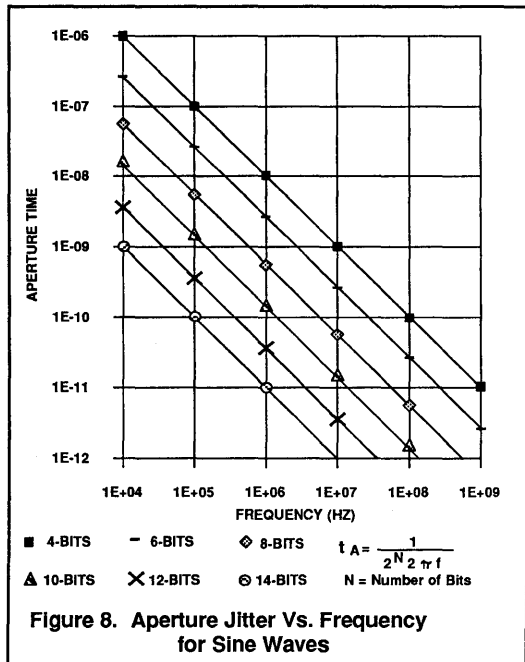
Most dynamic ADC testing requires sine waves for inputs and derive data based on that sine wave being ideal. To assure that the test signal is accurate, filters may be required to increase the purity of the input signal. Another method of testing is to eliminate the filters. This is done by measuring the harmonic contents of the input signal and digitally subtracting them from the output data.

APERTURE

As in any sampled data system the aperture jitter and width affect the accuracy of the system. If the aperture jitter time is converted to an amplitude uncertainty for any input where the voltage is changing, then the magnitude of this change for a sine wave can be calculated for time or voltage by the equation:

$$\frac{dV}{V} = 2\pi f t_a$$

By calculating the aperture jitter for a given system accuracy and comparing it to the aperture time of the flash converter, the need for a track and hold may be determined. The graph in Figure 8 summarizes required aperture jitter time for different resolution high



speed converters, for sinusoidal frequencies. The aperture width is an integration period and the signal will be integrated over its period. This would only cause a filtering effect, assuming that the aperture itself is well behaved.

An example to determine the maximum aperture jitter using an 8-bit flash converter: If the signal that is to be measured is known not to contain any sinusoidal frequencies above 10MHz, then from the graph in Figure 8, it can be determined that to assure less than 8 bits of error due to aperture jitter alone, the ADC must have an aperture jitter of less than 70ps. Most data sheets do not state aperture jitter, so to be safe the designer may wish to use a sample and hold. It may be difficult to find sample and holds that sample that fast. Since aperture times for ADCs are usually not specified, though for flash converters they can be very good, it is possible to add a sample and hold to the circuit and decrease the system performance.

Aperture width and jitter are very difficult to measure because of the extremely small time periods that are in the range of picoseconds to tens of picoseconds. Another problem is that they are not absolute numbers, but are random and are usually calculated based on statistical data. However, these values are needed to make intelligent design decisions, especially in sample and hold selection. These values are on the Honeywell SPT flash converter data sheets as typical values that have been based on both computer design simulations and verified by characterization of samples. Aperture delay is the time from the clock edge to the time that the sample is taken. Aperture jitter is the time variation in the point that the sample is taken.

Aperture delay is the delay from the time the clock is strobed until the sample is taken. Figure 9 shows a circuit based on driving both the clock input and the analog input with the same sine wave. This technique can accurately and easily measure aperture delay. It can also be used in a system to align several different channels in time. When using this technique be sure to use differential signals to the clock or errors may result.

Example using the HADC77100:

$$V_{in} = V_{offset} + A_o \sin \omega t$$

Choose $f_{in} = 30 \text{ MHz}$

$$A_o = .75$$

$$V_{offset} = -1.25V$$

Note that these voltage values will work well for any ECL flash converter with an input that swings below ground.

At ECL logic threshold, $V_1 = -1.3V$,

Measure V_2 and calculate T_2 .

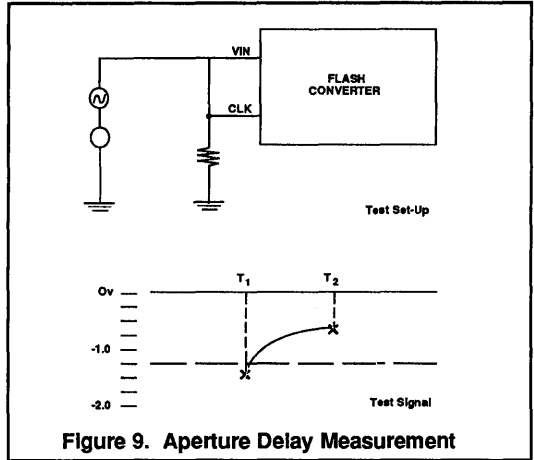
$$\text{Where } T_1 = \frac{\arcsin((V_1 - V_{offset})/A_o)}{\omega}$$

For $V_{fb} = -2.00V$ and $V_{rt} = 0.0V$,

$$V_2 = 2.0 ((\text{Code No.}/256) - 1)$$

And $T_2 = 1/\omega \arcsin((V_2 - V_{offset})/A_o)$

Aperture delay = $T_2 - T_1$



LINEARITY

Honeywell specifies both integral and differential linearities of the flash converters. Differential nonlinearity is specified from an ideal 1 LSB code width. Therefore, for a device that is specified $\pm 1/2$ LSB every code will have widths between $1/2$ LSB and $1 1/2$ LSBs wide. A device specified $\pm 3/4$ LSB could have code widths from $1/4$ LSB to $1 3/4$ LSBs wide. To have missing codes the device would need to be specified -1 LSB or greater.

Honeywell has demonstrated the capability of producing flash converters with differential linearity in excess of 9 bits without any type of trimming. The 10-bit converter is capable of being trimmed because a 10-bit converter has four times the number of comparators as an 8-bit flash converter. An offset error of only 2mV in any single comparator could destroy the linearity of

the converter. Trimming is in the form of four aluminum links that can be laser cut to select different resistors that will alter the comparator offsets. This method of trimming was chosen because no active or current carrying structure is altered. It is either in the circuit or it is completely deleted. This assures that there is no affect on either long-term stability, reliability, or on temperature performance.

Absolute linearity of converters can be adjusted by the use of external taps. The 10-bit converter can be adjusted by the use of seven external taps, and for the 8-bit converters either one or three taps are available (see Figure 7). These taps can be used to cancel the effect of the bias currents of each preamplifier (see Figure 10). If each wafer had exactly the same betas and absolute bias current, the ladder could be designed to compensate for the bias currents. This would imply that bias currents on each preamplifier could be the same, not only from device to device, but also from chip to chip. Honeywell's designs correct for these first order effects. These effects would appear as bows (see Figures 11A & 11B) in the linearity curve caused by bias currents. Honeywell's correction works very well so that at the 8-bit level this typical center tap offset is less than a millivolt. So taps are not required to maintain 8-bit linearity at room temperature.

External taps, for the 8-bit converters have half or quarter scale connections and the 10-bit converter has taps placed at eighth scale intervals to allow the user to force the ladder. Externally altering the ladder's linearity, if required, is low in cost and can also be used to change the dynamic range of the converter. Honeywell recommends the use of the PMI OP9 or OP11 quad op amps to force the ladder. These op amps have the required low offset voltage and drift.

The dynamic range of the HADC77200 can be increased by using external ladder taps to bend the ladder and create a piecewise approximation of a curve (Figure 12). There are two primary considerations for this application. The first is to assure that the low end of the scale has no missing codes due to comparator offsets. The second consideration is to assure the maximum ladder current specification is not exceeded.

In normal applications the ladder is referenced to a -2.0 Volt full scale. This results in an LSB of 7.8mV. Therefore a part that is $\pm 1/2$ LSB linear will have comparator offsets of less than half this value or 4mV. The 100 Ohm ladder will have 20mA through it, which is close to its maximum rated current of 25mA.

If a device was to be screened to be $\pm 1/4$ LSB then a 2mV LSB would be possible for the linearity point of view.

So lets start with a 2mV LSB and geometrically progress, doubling the LSB weight at a quarter, half and three quarters scales, the points available on the HADC77200. This would result in -128mV, -384mV and -896mV taps respectively. Full scale would be at -1.920V. Current in the ladder can now be calculated to be $(1920-896\text{mV})/25 \text{ Ohms} = 41\text{mA}$. This does exceed the maximum ladder current at 25 mA. But if the device is operated at room temperature there should be little effect on the devices life. Starting with a 39% lower LSB weight will soothe power problem but initial accuracy would not be good enough to guarantee no missing codes.

The above application has the ability to resolve 2mV out of a possible 1960mV or 59.8dB of dynamic range.

If the 25mA specification for the ladder is not to be exceeded then the weight of an LSB cannot exceed 9.8mV. Because of comparator offsets in our process an LSB should not be less than 2mV. A geometric progression where each LSB value changes at the quarter scale points by a factor of 1.7 times the previous LSB value could be used. The results would be within the above constraints of an LSB being between 2mV and 9.8mV. The taps would then be at -128mV, -345.6mV, -715.5mV and full scale would be at -1.3444V. Dynamic range would be 56.6dB.

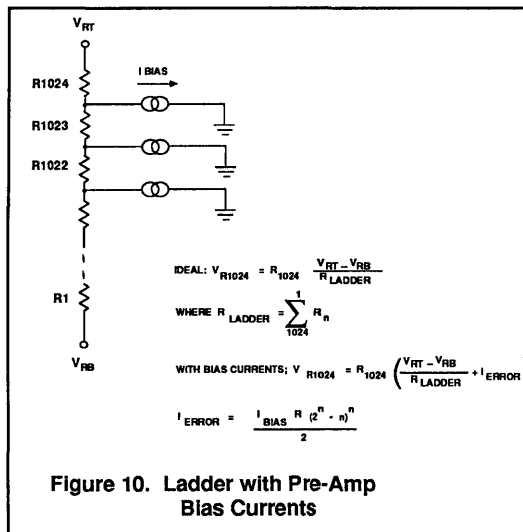


Figure 10. Ladder with Pre-Amp Bias Currents

The original assumption was that parts could be screened to $\pm 1/4$ LSB. Now that the LSB is designed to be 2mV and this is for the first 64 codes only, screening could be for the first 64 codes to $\pm 1/4$ LSB and the remaining codes to $\pm 1/2$ LSB. This may help yields and keep the cost of this screened device lower than screening all codes to a tightened specification.

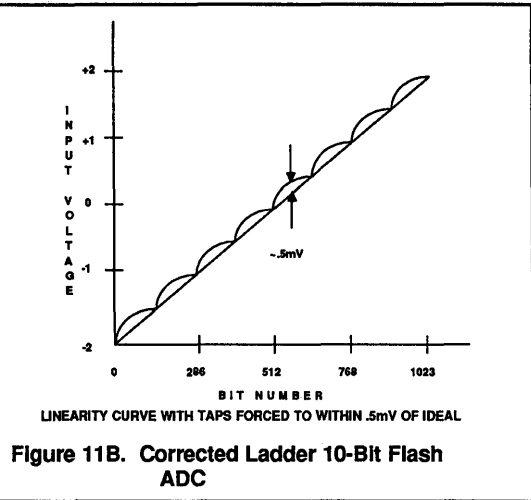
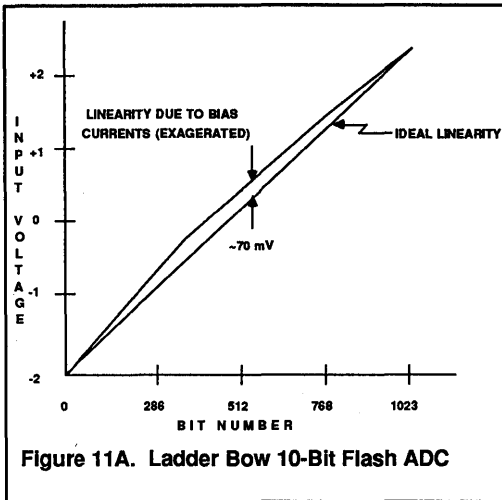


Figure 11A. Ladder Bow 10-Bit Flash ADC

Figure 11B. Corrected Ladder 10-Bit Flash ADC

The coding of the flash converter is such that V_{rt} is full scale. It may therefore be easier to start with the 2mV step in the portion of the ladder between V_{rb} and V_{r1} . The concept is the same only the taps would be switched.

Because of their very low impedance the reference ladders of flash converters have very high bandwidths. This can be used to dynamically scale the input at very high switching speeds. There is a penalty paid in the SNR and accuracy, but this may be less than that of using a programmable gain amplifier. It is not recommended to go below 500mV full scale range. This will give a range changing ability of 4 to 1 when a -2.0V reference is used.

SUMMARY OF RESULTS

V_{rt}	0.0	0.0	mV
V_{r3}	128	128	mV
V_{r2}	384	345.6	mV
V_{r1}	896	715.5	mV
V_{rb}	1920	1344.4	mV
LSB1	2.0	2.00	mV
LSB2	4.0	3.4	mV
LSB3	8.0	5.78	mV
LSB4	16.0	9.83	mV
Dyn Range	59.8	56.6	dB
Max Current	40	25	mA

INCREASING DYNAMIC RANGE

The dynamic range of a system can be increased by stacking ADCs in groups of two or four. Prior to the HADC77100, this was a very difficult task due to two

sources of error. The first error source was the static errors of the ADCs with their linearity equal to their number of bits yields greater resolution, but there is still only the accuracy of the original converters plus other errors due to offsets and differences in gain. The accuracy of the ADCs should be at least 9 bits accurate to form a 9-bit accurate 9-bit system. The second error source was due to dynamic currents flowing from the input of one converter and perturbing the input of the other device(s).

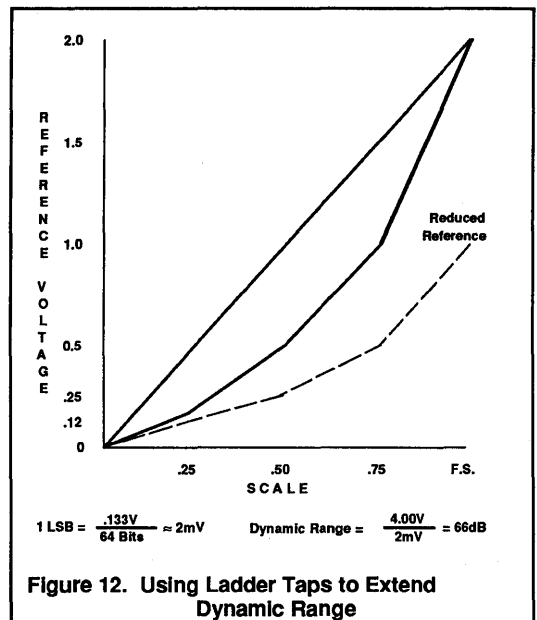


Figure 12. Using Ladder Taps to Extend Dynamic Range

Figure 13 shows an example of two 2-bit ADCs connected to form a 3-bit ADC. This example does not show the logic required to change the output code from all ones to all zeros when the overrange bit goes high. An alternative method of implementing this data conversion is to connect the overrange bit (NOTE: OVR goes True if V_{in} is greater than V_{ref} minus the offsets) to the MINV and LINV bits of each converter. The individual bits can then be wire ORed together and no additional logic is required. The delay of 6ns from INV to data out must be taken into account when setting up the timing for this method. Implementing this circuit with N-bits is identical to the 3-bit example. This stacking of ADCs has no adverse effect on the data throughput; only data output delay is affected. This method of combining ADCs does increase the input capacitance and this must be accounted for in selecting the input amplifier.

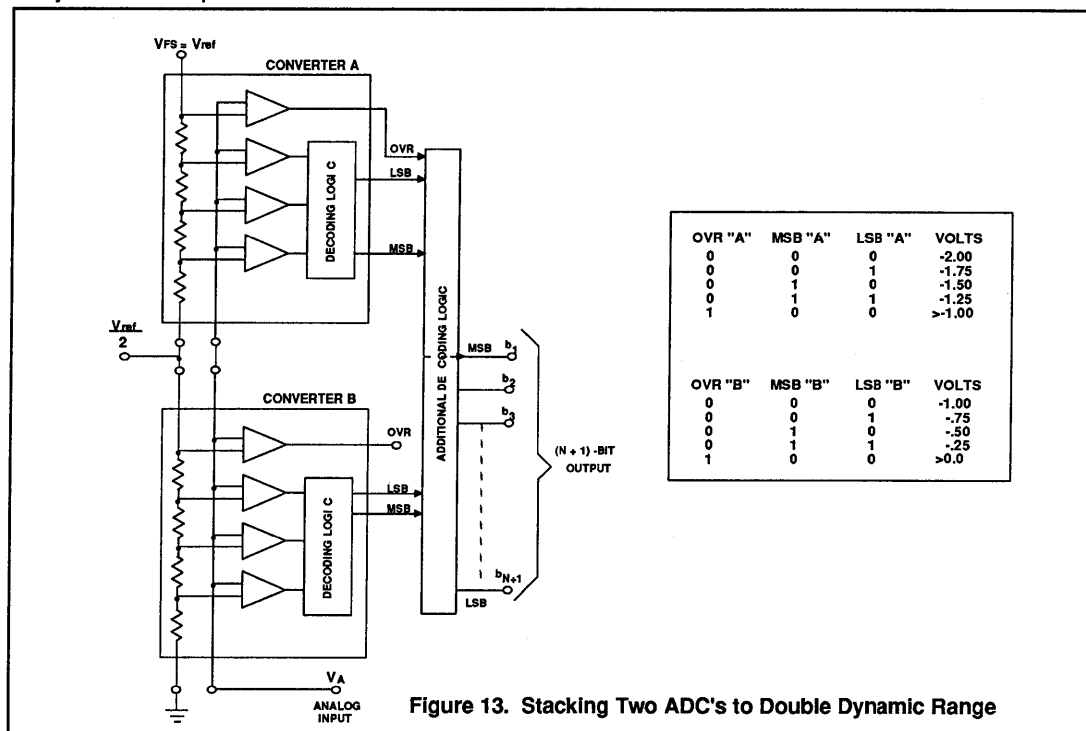
Stacking four ADCs is also possible. In this circuit, logic would have to be implemented to control the data from the overrange bits to the outputs. This circuit may have an additional clock delay to the output.

SPT can custom manufacture any of the HADC77100 family for use in stacked applications. These ADCs would then have the correct logic coding at the outputs so that additional logic and their associated delays would not be present.

INCREASING SAMPLE RATE

The sample rate of a system can often be increased by combining two flash ADCs with their clocks connected out of phase (this is known as ping-ponging) as shown in Figure 14. This technique works especially well with the HADC77100 because of several of its performance parameters. First, the greatly reduced kick-back allows both converters to be driven from the same buffer or amplifier without one converter affecting the other. This eliminates any problems that may arise from different frequency responses of separate amplifiers. Other advantages are that the excellent linearity of the HADC77100 or HADC77200 will enable the design of a true 8-bit system with sample rates of over 250MHz. The data would then be available on two separate busses, a useful feature for data rates in excess of 100MHz. By using the HADC77200 data could be easily clocked into memory or onto the data bus by using the Data Ready output.

The best advantage to using Honeywell flash converters in these applications is that they only require a single clock that has an ideal 50% duty cycle. This eases design by eliminating the need for delay lines in generating the timing signals.



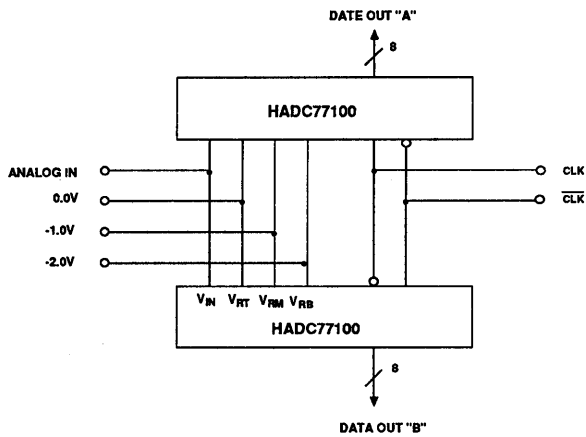


Figure 14. Ping Pong 2 ADC's for 2X Sample Rate

EB101 EVALUATION BOARD 8-BIT, 150 MSPS FLASH A/D CONVERTER AND 8-BIT, 165 TO 400 MWPS RASTER D/A CONVERTER WITH REFERENCE

by Tom DeLurio Senior Applications Engineer

FEATURES

- 150 MSPS MINIMUM CONVERSION RATE
- 70 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Low Clock Duty Cycle Sensitivity (Adjustable)
- Preamp Comparator Design/Optional Input Buffer
- ECL clock produced from any signal generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

APPLICATIONS

- Evaluation of HADC77200 A/D Converter
- Evaluation of HDAC10181/51400 D/A Converters
- High Definition Video
- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

The EB101 Evaluation Board is intended to show the performance of Honeywell Inc.'s Signal Processing Technologies HADC77200A/B flash A/D converter and the HDAC10181A/B or HDAC51400 Ultra High Speed D/A converters. The board provides for either the ADC or DAC to be tested together or separately. Included on the unit are two 100K ECL multiplexers for data routing between the A/D and D/A or on and off the board as shown in the block diagram below.

The HADC77200A/B is a monolithic flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 70 MHz into 8-bit digital words at a minimum 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

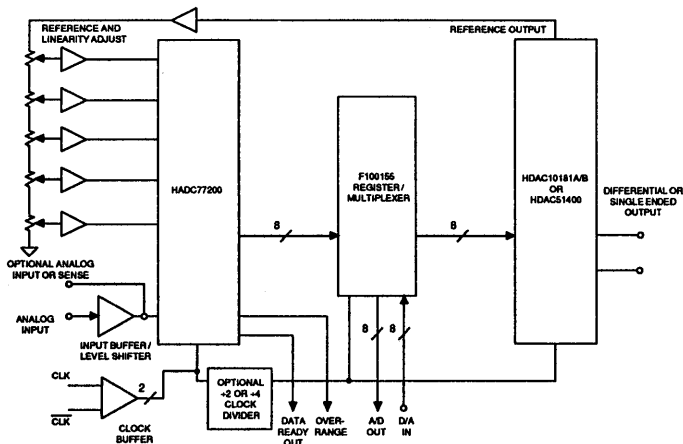
The HDAC51400 and HDAC10181A/B are monolithic 8-bit D/A converters capable of converting data at rates of 400, 275, and 165 MWPS respectively. The parts have

optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DACs have an internal reference to supply themselves and the HADC77200 with a stable voltage reference and gain control for different output voltage swings.

The HCMP96870 is a high speed dual differential voltage comparator used to generate an ECL compatible clock signal from any type signal generator.

The board is in Eurocard format with a 64-pin dual height DIN connector for digital data. The analog inputs, outputs and clock input are standard 50Ω BNC connectors. Tektronix high impedance probe jacks are provided to monitor the clock lines. Standard -5.2V, +5V, and ±12 to ±15 Volt power supplies are required for operation of the EB101, with nominal power dissipation of less than 11 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer board is available for high performance applications and is explained in more detail on the following pages.

BLOCK DIAGRAM



GENERAL INFORMATION

The EB101 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of Honeywell's HADC77200 8-bit A/D converter, HDAC-10181/54100 8-bit D/A converters and HCMP96870 dual comparator. The board contains circuitry for buffering the input signals, generating reference voltages, dividing the DAC and multiplexer clocks, routing input / output data, and generating ECL level differential clock signals from any signal generator. All digital inputs and outputs are 10KH and 100K ECL compatible and provisions are made for gain, offset and linearity adjustments. The board requires -5.2, +5 and ± 12 to ± 15 Volt supplies.

The EB101 evaluation board consists of seven functional sections that include an analog input buffer, A/D converter, input/output multiplexer and data latches, D/A converter, reference voltage generator, ECL clock generator, and ECL clock divider. The analog and digital grounds are separated on the board for better system grounding characteristics.

There are numerous jumper options available to switch sections in or out of the system to suit individual needs. The clock divider circuitry is on a separate board that plugs into the main board to provide divide by 2 or 4 for the multiplexer and DAC. The jumper options will be discussed in more detail in the following sections. In addition, 90MHz low pass input and output filters are on board.

ON BOARD ANALOG INPUT BUFFER

This section consists of a 90MHz low pass filter, HA2539 high frequency op-amp, and a 2N5836 rf transistor. The input impedance is 50 Ω and the gain is set at 2X so that a 1 Volt input can be applied. Compensation components are provided and can be adjusted for the desired frequency range needed. The compensation is factory adjusted for 50MHz bandwidth operation. The bandwidth of the buffer amplifier can be increased by decreasing the gain to 1X by changing the 1.5k Ω feedback resistor to 750 Ω . The BNC connector shown in the schematics and layout near the output of the buffer can be used for monitoring the buffer output and input to the HADC77200. The BNC should be connected to a 50 Ω terminated oscilloscope and will provide a 10X attenuated signal.

The positive input to the HA2539 is tied to an offset adjust to center the input signal to the HADC77200 around -1V, which is needed if a 2V_{P-P} input signal is applied. The input buffer can be bypassed by removing the 6.8 Ω resistor at the emitter of the 2N5836 and the 450 Ω resistor between the BNC connector and the HADC77200. Bypass the 450 Ω resistor with a jumper wire and the HADC77200 can now be driven directly. The input impedance is 4K Ω in parallel with a 56pF distributed capacitance.

OPTIONAL ANALOG INPUT BUFFER BOARD - EB102

An alternate and higher performance input buffer is available as an option and sold separately. The EB102 is intended for users operating at the top end of the input bandwidth range of the HADC77200. The reason for a separate board is that the amplifiers utilized are quite a bit more expensive than the "on-board" buffer. But, with the added expense, increased input bandwidth with less harmonic distortion is realized.

There are two versions of the EB102 buffer board, one with a wideband op-amp (CLC221) and one with a wideband buffer amplifier (CLC231). Both versions are identical but are jumpered to provide for the different amplifier pinouts (See Figure 1A). The CLC221 version has the advantage of being configured up to a gain of 50 as required, and has slightly better harmonic distortion specifications. The CLC231 version has the advantage of a much higher output drive current and better settling time.

The Following table shows a breakdown of some of the more important specifications:

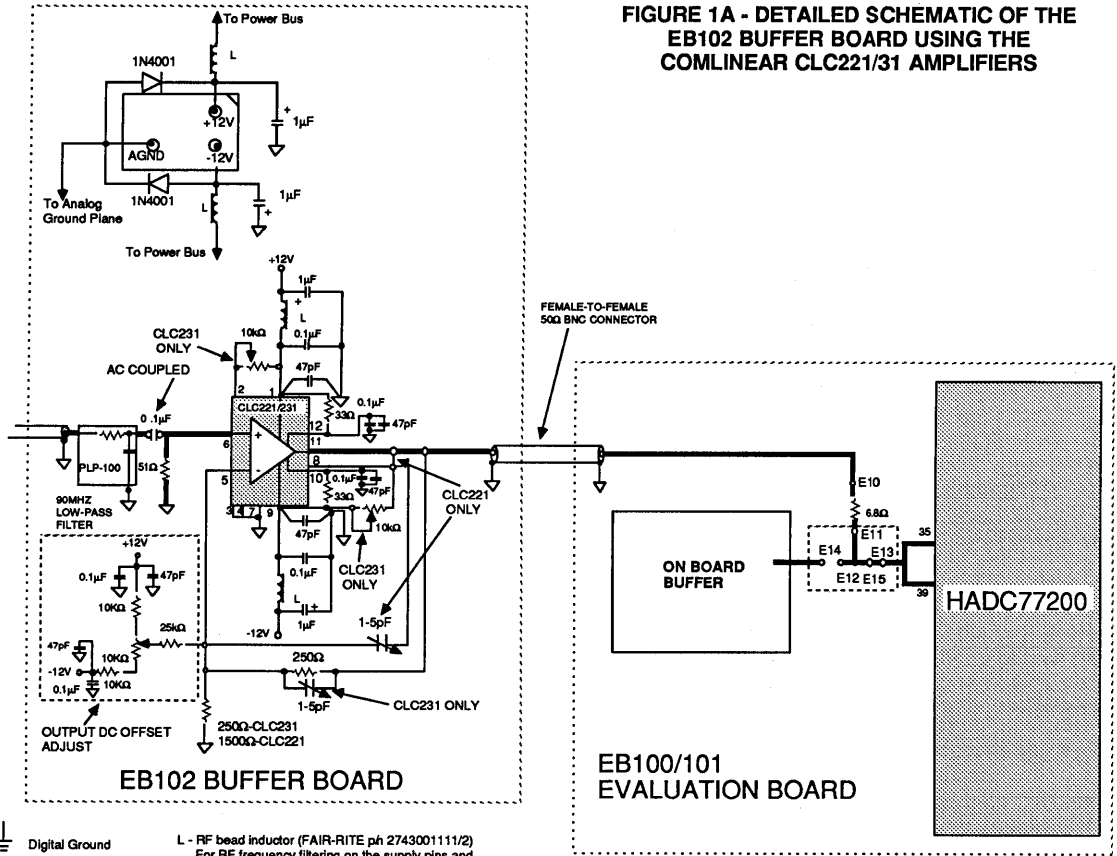
TABLE 1 - COMPARISON OF COMLINEAR CLC221/31 AMPLIFIERS

SPECIFICATION	CLC221	CLC231
Gain Range	± 1 to 50	± 1 to 5
Output (V, mA)	$\pm 12,500$	$\pm 11,100$
Slew Rate (V/ μ sec)	6500	3000
-3dB Bandwidth (Av=2)	275MHz	165MHz
Settling Time (nsec, %)	15, 0.1 18, 0.02	12, 0.1 15, 0.05
Harmonic(dBc) Distortion	Second Third	-58 -59

100K ECL CLOCK GENERATOR

The ECL clock section consists of an HCMP96870 dual comparator, duty cycle and hysteresis adjust, F100131 triple D flip-flop and several jumper options. Any type high frequency signal generator can be connected to the BNC input to the comparators. Both inputs to the dual comparators are connected to the BNC. There are four outputs which generate differential 100K ECL clock signals. One set goes directly to the HADC77200 while the other two can go to the F100155 multiplexers and HDAC10181/51400 or to the clock divider circuitry.

FIGURE 1A - DETAILED SCHEMATIC OF THE EB102 BUFFER BOARD USING THE COMLINEAR CLC221/31 AMPLIFIERS



EB102 BUFFER BOARD

EB100/101 EVALUATION BOARD

Digital Ground
 Analog Ground
 L - RF bead inductor (FAIR-RITE ph 2743001111/2)
 For RF frequency filtering on the supply pins and between AGND and DGND.

All BNC connectors are 50Ω TROMPETER CBJ20

The threshold input to the HCMP96870 comparators are connected together to a pot to adjust the duty cycle of the clock. The latch enable pins are also connected together to a pot to adjust hysteresis.

100K ECL CLOCK DIVIDER

The clock divider section is shown below in Figure 1B and consists of a triple D type flip-flop, which if jumpered as shown, will provide divided down clock outputs. The clock divider can be bypassed to provide a full frequency clock. The divider is provided to make it easier to monitor the HADC77200 output with a low frequency logic analyzer and to provide the DAC with a reduced sampling rate. When switching between divide by 2 or 4, the unused outputs "Q" and "Q" must be terminated. Furthermore, the jumpers on the clock lines to the multiplexer and DAC must be removed.

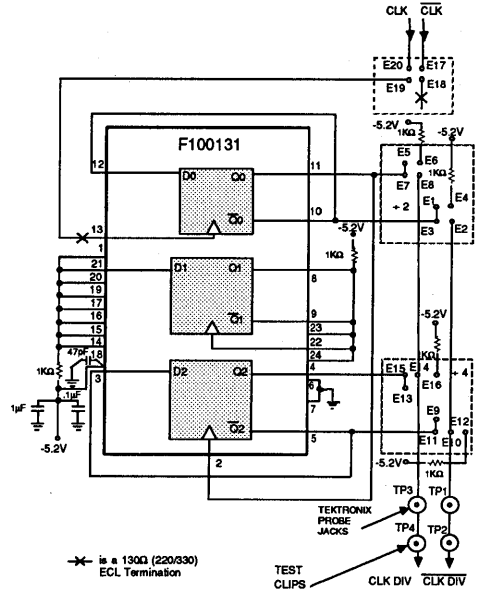


FIGURE 1B - 100K ECL CLOCK DIVIDER

REFERENCE VOLTAGE GENERATOR

The reference voltage for the HADC77200 and HDAC-10181/51400 is internally generated by the D/A converter voltage reference of approximately 1.2Volts. The A/D converter's 2Volt reference, 3 voltage midtaps and ground are controlled by two PMI quad op-amps (OP-11). The magnitude of each setting is further adjusted with potentiometer R25, R26, R32, R37, and R38 as shown in the detailed schematic and board layout.

INPUT/OUTPUT REGISTER AND MULTIPLEXER

The multiplexer section consists of two F100155 which select between external 8-bit digital data from the 64-pin DIN connector or data from the output of the HADC-77200. The choice is controlled by tying the SELECT pins to either an ECL high for external data or an ECL low for HADC77200 data. This data is then fed to the HDAC10181/51400 on the "Q" outputs of the F100155 and the "Q" outputs are tied to the external connector.

A/D CONVERTER SECTION

Both input pins to the HADC77200 are tied together to be either fed by the input buffer or by an external source. The MINV and LINV inputs are left open and tied internally to an ECL low. Diodes are provided to tie them high and change the output logic. The connection choices for determining the output logic are in Table 2.

D/A CONVERTER SECTION

The D/A converter section contains jumpers to use either the HDAC10181 or HDAC51400. The primary difference in the two parts is the reference voltage connections. These differences are shown in the detailed schematic in Figure 2. All EB100 boards and jumpers will be connected for the HDAC10181A part. If an HDAC51400 is indicated when the board is ordered (See last page), the board jumpers must be configured as shown in Figure 4A and 4B by the user.

The output current magnitude for the HDAC10181/51400 is controlled by a potentiometer (R36) through the DAC's Iset control pin. In addition, two 90 MHz low pass filters are provided at both out- and out+ output pins as well as 50Ω terminating resistors. The terminating resistors can be changed to 75Ω if desired. Keep in mind that the transmission line must be terminated at the receiving end with the same value resistor. The video and feedthrough controls are routed to the 64-pin DIN connector and are normally disabled.

TABLE 2 - OUTPUT LOGIC CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.
.
VIN	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.
.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: VIH, VOH
0: VIL, VOL

TABLE 2A - POTENTIOMETER AND CAPACITOR ADJUSTMENTS

NO.	FUNCTION
R26	Pot for adjusting gain to produce a 2V reference voltage for the VRB pin on the HADC77200 from the 1.2V reference voltage supplied by the HDAC10181/51400.
R25/ 37/38	Pots for setting the linearity adjustments at the comparator reference ladder on the HADC77200.
R32	Pot for setting the top point (VRT) on the reference voltage ladder. Nominally set at 50mV below AGND.
R36	Pot for adjusting output current drive from the HDAC10181/51400 (See data sheets). $V_{out+} = 25.6(\text{digital code } X \text{ Iset})/RL$
R5	Pot for setting the HCM96870 comparator threshold voltage to adjust the ECL clock duty cycle.
R4	Pot for adjusting comparator hysteresis.
R23	Pot for adjusting up to a 2V offset voltage at the buffer output for driving the HADC77200.
R22	Pot for adjusting compensation and bandwidth for the buffer circuitry. This has been set for maximum bandwidth by turning to the full counterclockwise range. The frequency range can be decreased by adjusting the potentiometer clockwise.
C25	"Lead" Capacitor for changing the damping factor of the input buffer, used in conjunction with Pot R22. This has been set for a flat response.

POWER SUPPLY CONNECTIONS

Power to the EB101 is supplied through a six pin Molex type connector. The supply lines are color coded as shown in Figure 1C. Connect the wire end of the power supply harness to power supplies as shown by Figure 1C and the silk screen near the mating connector on the PC board itself. The power harness is attached to the board with the bevelled edges and hollow connector aligned to the mating connector.

The power requirements for the EB101 at different supplies and with or without the clock divider board is shown in Table 3. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

TABLE 3 - POWER DISSIPATION

EB100 WITH CLOCK DIVIDER, ±15V			
Voltage	Current	Power	
+15V	.145A	2.175W	
-15V	.148A	2.220W	
+5V	.006A	0.030W	
-5.2V	1.65A	8.580W	
		13.005W	
EB100 W/O CLOCK DIVIDER, ±12V			
Voltage	Current	Power	
+12V	.119A	1.428W	
-12V	.123A	1.476W	
+5V	.006A	0.030W	
-5.2V	1.49A	7.748W	
		10.682W	

AN102

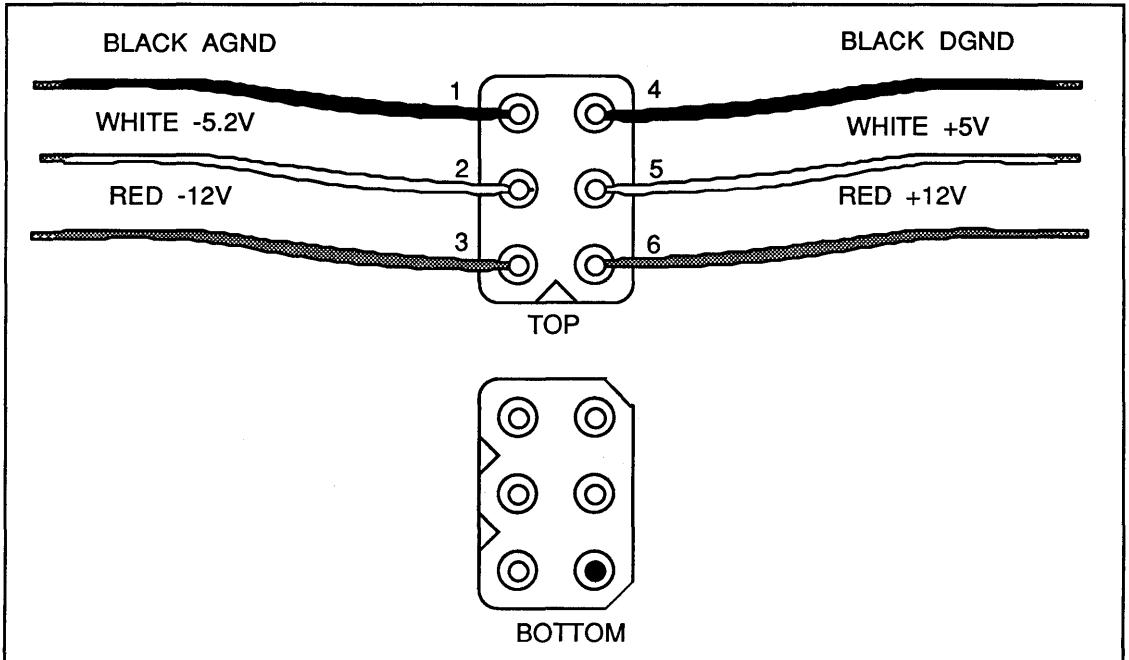


FIGURE 1C - POWER SUPPLY HARNESS CONFIGURATION

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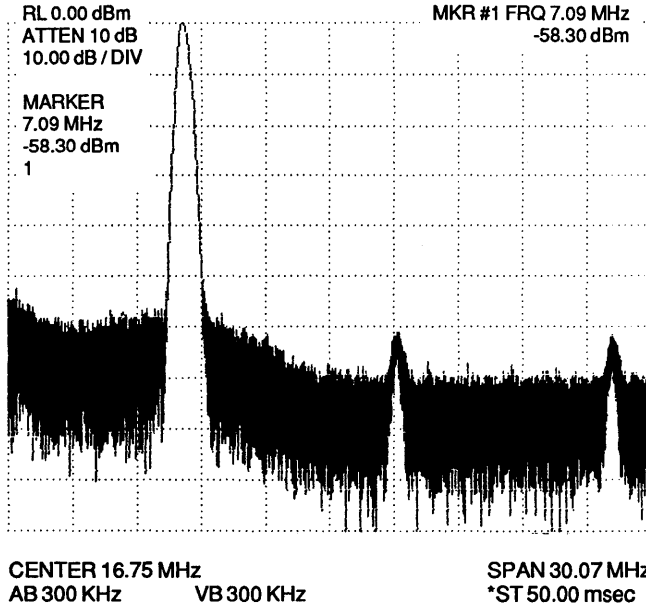
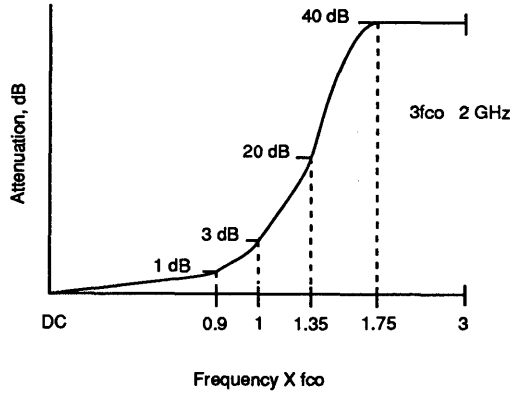
ANTI-ALIASING AND CLOCK NOISE FILTERS

The input to the EB101 buffer circuitry and the differential outputs from the D/A converter are provided with high frequency noise filters. The three filters are 90MHz low pass and are intended to be used with the full analog input frequency and full clock sampling rate of the HADC77200 A/D converter. If lower frequencies are used, the filters should be changed to filter clock noise and harmonics for a particular application. Mini-Circuits

Inc. (see below) supplies a range of low pass filters that fit into the same position as the 90MHz filters on the EB101 Evaluation board.

Additional filtering can be achieved by decreasing the bandwidth of the input buffer by adjusting the 500Ω potentiometer (R22 in Figure 4) clockwise. Also, adjustment of the clock duty cycle with potentiometer R5 will lower the overall noise floor by controlling the setup and hold time of the digital data for the multiplexers (F100155) and DAC (HDAC10181).

Low Pass
Typical Frequency Response

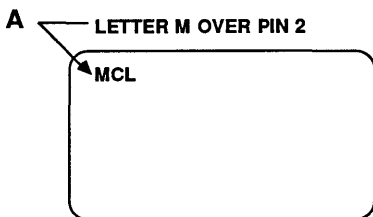


DAC OUTPUT SPECTRUM ANALYSIS OF A 10MHz INPUT FUNDAMENTAL WITH A 10.7MHz (PLP-10.7) OUTPUT LOW PASS FILTER AND 100MHz CLOCK RATE

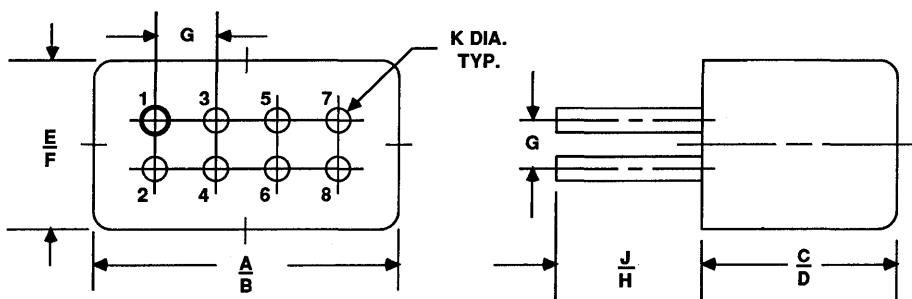
PLP
case A01

MODEL NO.	PASSBAND, MHz (loss < 1dB) Min.	f _{co} , MHz (loss 3dB) Nom.	STOP BAND, MHz			VSWR,	
			(loss > 20dB) Max.	(loss > 40dB) Max.	(loss > 40dB) Min.	Passband Typ.	Stopband Typ.
PLP-10.7	DC-11	14	19	24	200	1.7	1.7
PLP-50	DC-48	55	70	90	200	1.7	17
PLP-70	DC-60	67	90	117	300	1.7	17
PLP-100	DC-98	108	146	189	400	1.7	17

Case no.	A	B	C	D	E	F	G	H	J	K
A01	.770	.800	.385	.400	.370	.400	.200	.20	.14	.031
	19.56	20.32	9.78	10.16	9.40	10.16	5.08	5.08	3.56	.79



TOP VIEW



NOTE: BLACK BEAD INDICATES PIN 1. PIN NUMBERS DO NOT APPEAR ON UNIT. FOR REFERENCE ONLY.

PIN CONNECTIONS

SEE CASE STYLE OUTLINE DRAWING

SERIES	IN	OUT	GROUND
PLP	1	8	2, 3, 4, 5, 6, 7

FIGURE 2 - DETAILED SCHEMATIC OF EB101, REVISION C

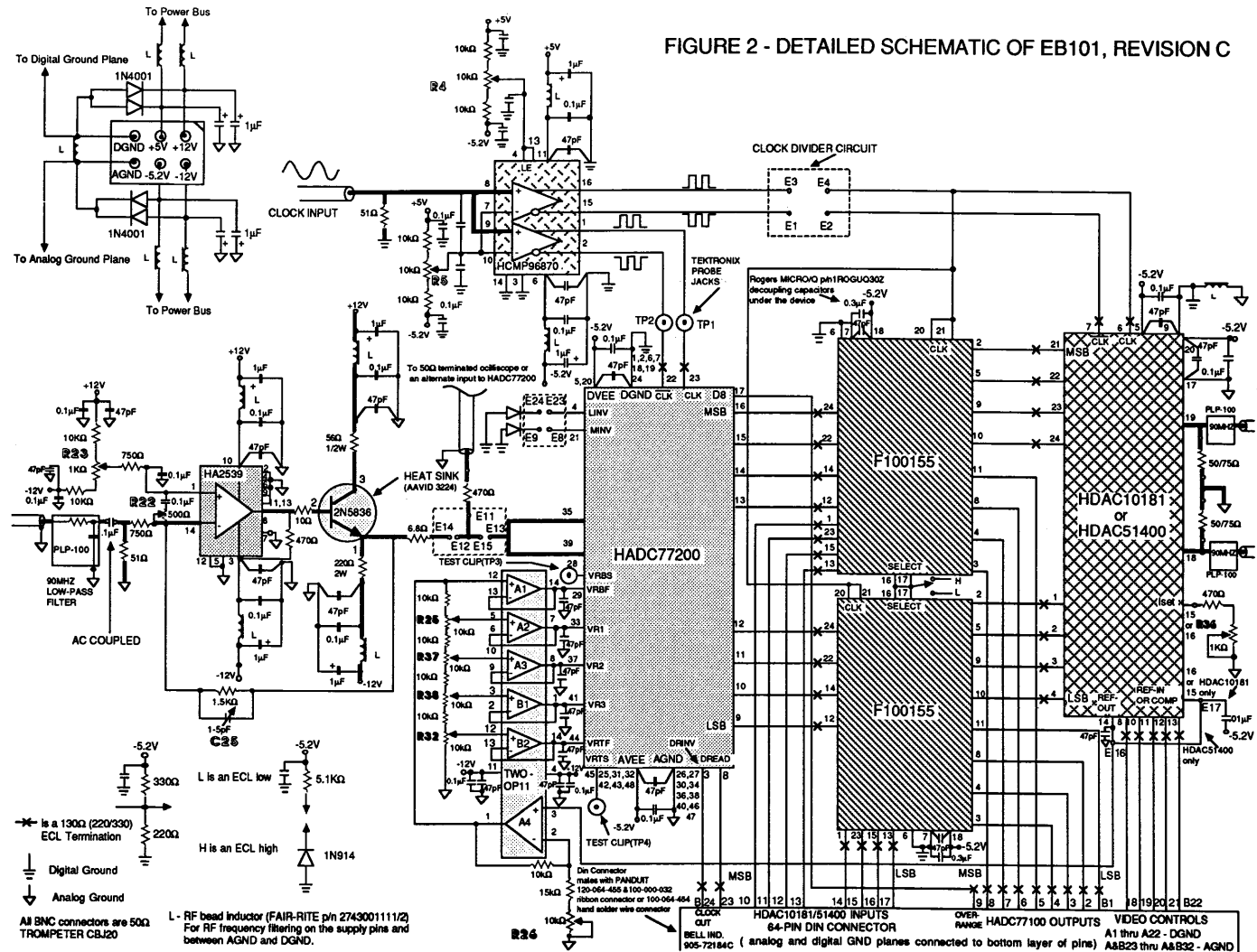


FIGURE 3 - TIMING DIAGRAM

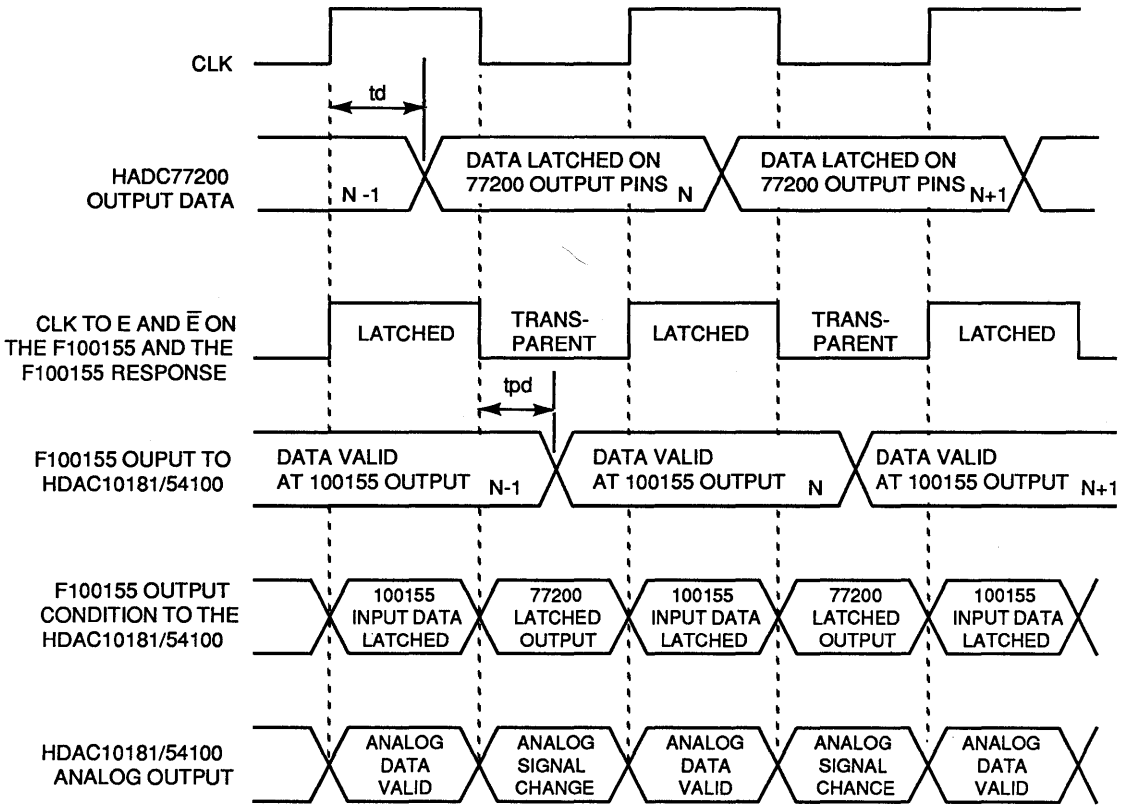
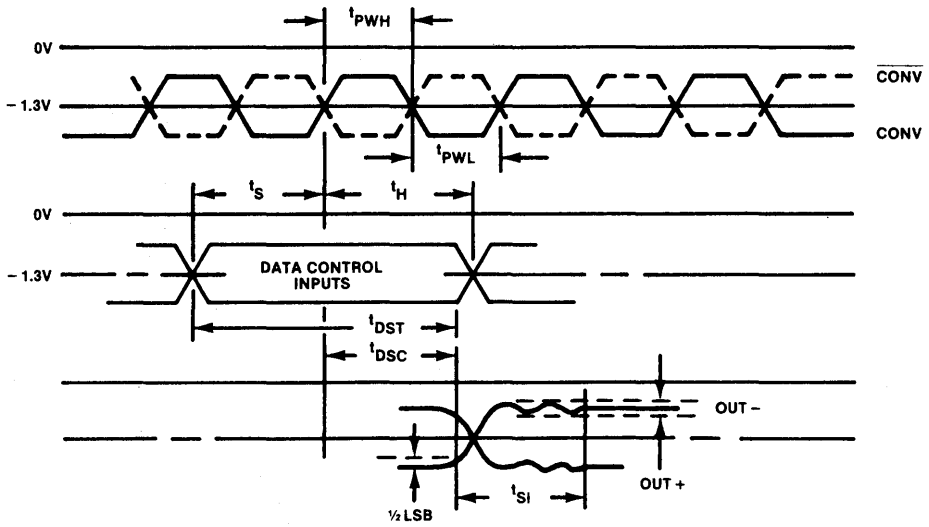
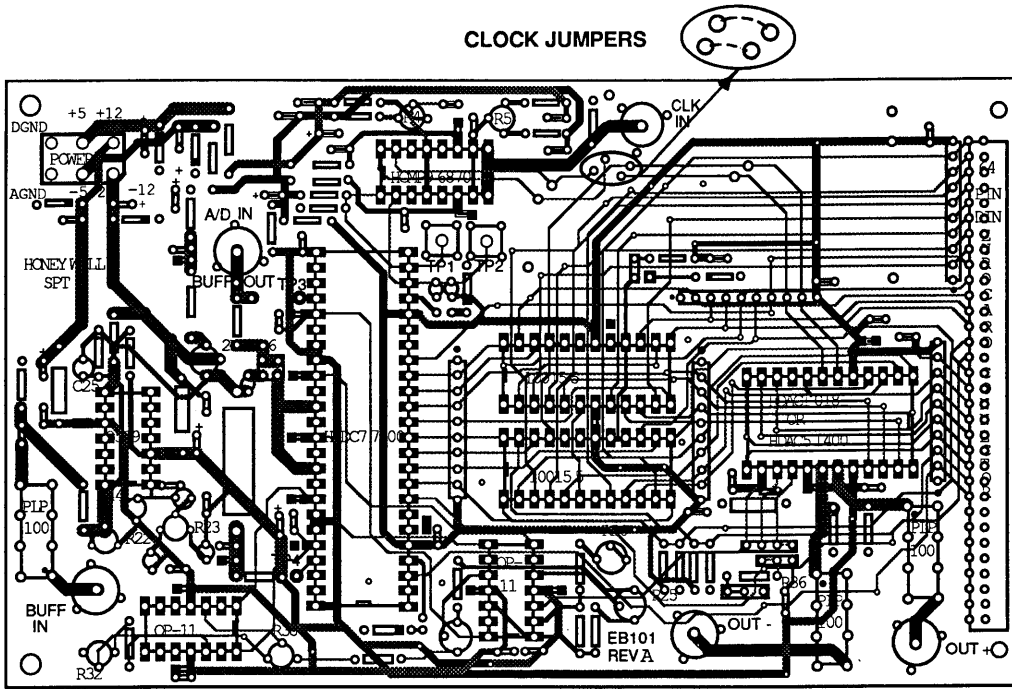


FIGURE 3 CONTINUED 10181/51400 TIMING DIAGRAM

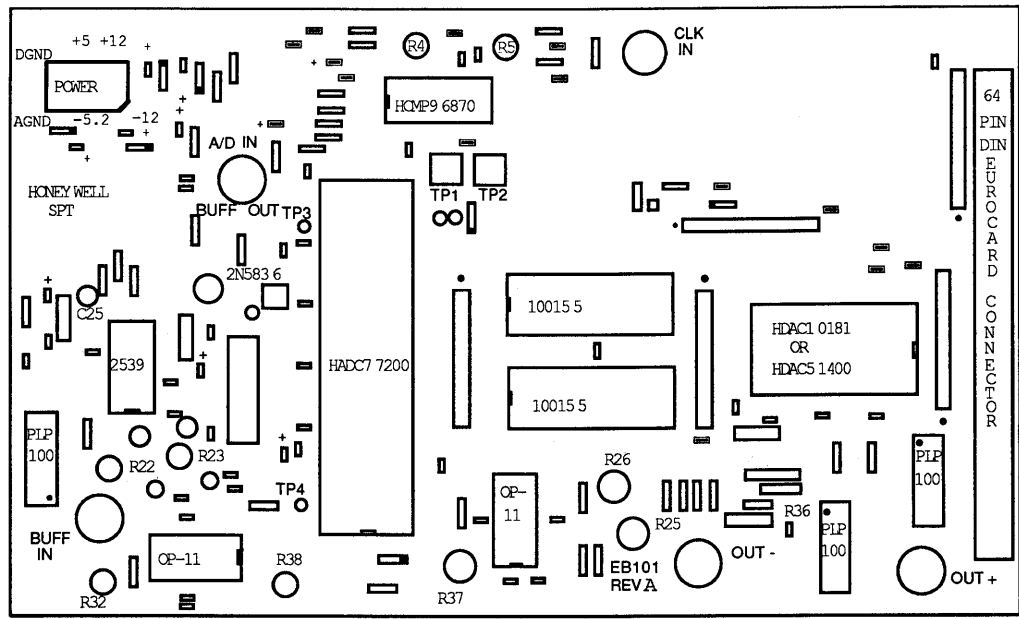
AN102





4.600

7.000



64 PIN DIN EUROCARD CONNECTOR

FIGURE 4A - MAIN BOARD LAYOUT AND COMPONENT POSITION (Not To Scale)

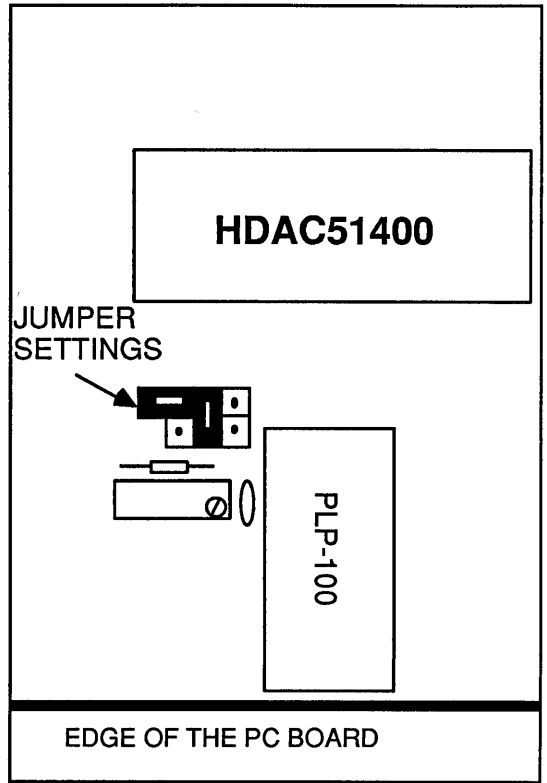
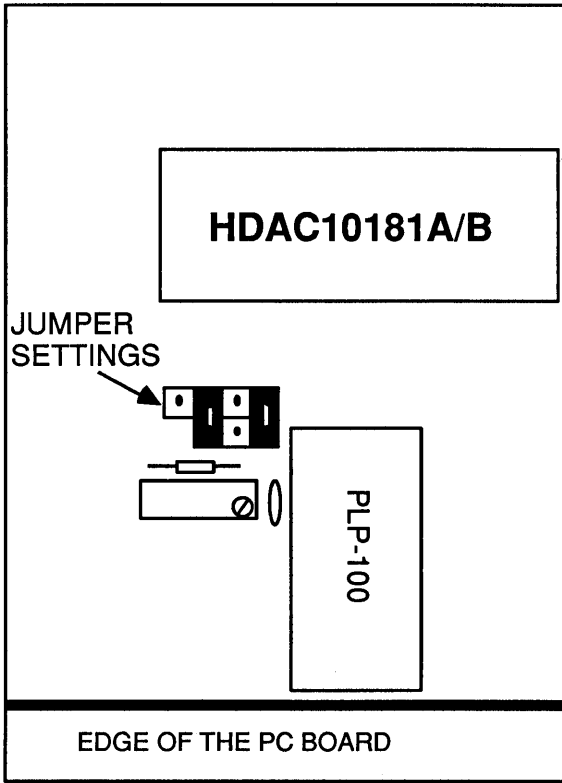


FIGURE 4B - JUMPER POSITION AND CONNECTIONS FOR EITHER THE HDAC10181A/B OR HDAC51400
(Not To Scale)

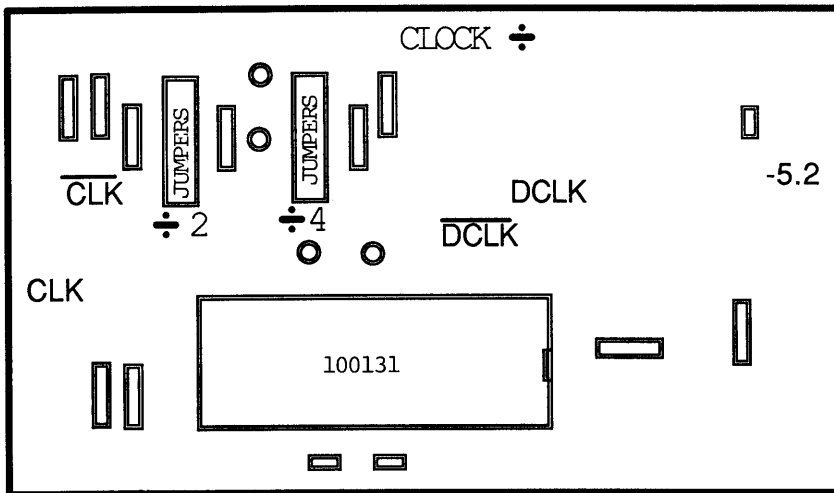
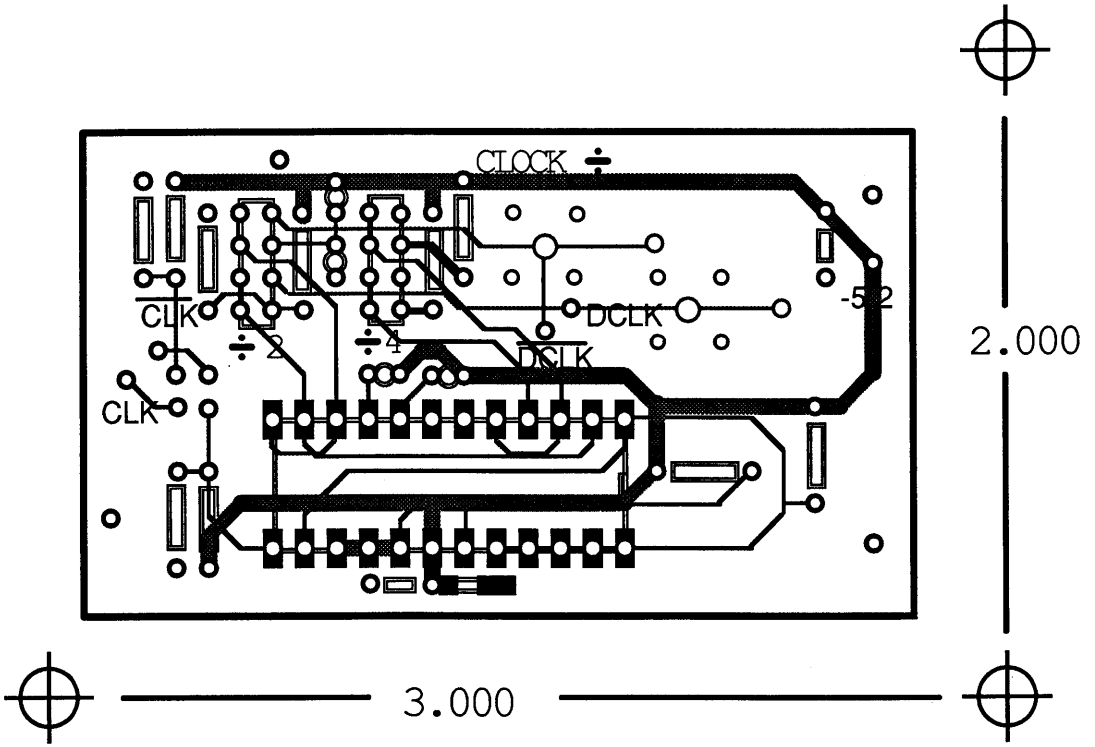


FIGURE 5 - CLOCK DIVIDER BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

EB101 REVISION C PARTS LIST

AN102

PARTS LIST			
NO.	DESCRIPTION	QTY.	MANUFACTURER / PART NO.
1	FERRITE BEAD	11	FAIR-RITE CORP.-2743001111
2	DIODE	4	1N4001
3	DIODE	3	1N914
4	TRANSISTOR	1	MOTOROLA-2N5836
5	I.C.	1	HONEYWELL-HDAC10181A/B OR HDAC51400
6	I.C.	1	HONEYWELL-HCMP96870
7	I.C.	2	FAIRCHILD-F100155
8	I.C.	2	PMI-OP-11
9	I.C.	1	HONEYWELL—HADC77200A/B
10	I.C.	1	HARRIS-HA2539
11	FILTER	3	MINI-CIRCUITS-PLP-100
12	RESISTOR	1	240Ω, 2w
13	RESISTOR	1	56Ω, 1/2w
14	RESISTOR	1	6.8Ω, 1/8w
15	RESISTOR	11	10KΩ, 1/8w
16	SIP RESISTOR PACK	5	220/330Ω
17	RESISTOR	4	220Ω, 1/8w
18	RESISTOR	4	330Ω, 1/8w
19	RESISTOR	2	750Ω, 1/8w
20	RESISTOR	3	50Ω, 1/8w
21	RESISTOR	3	470Ω, 1/8w
22	RESISTOR	1	10Ω, 1/8w
23	RESISTOR	1	15.1Ω, 1/8w
24	RESISTOR	1	5kΩ, 1/8w
25	RESISTOR	1	1.5kΩ, 1/8w
	POTENTIOMETER	2	BOURNS-1KΩ, 3329-H-102 & MOUSER-ME323-4290W-1kΩ
26			
27	POTENTIOMETER	8	BOURNS-10KΩ, 3329-H-103
28	CONNECTOR, DIN	1	BELL IND.-905-72184C
29	CONNECTOR	1	MOLEX-09-18-5069
30	CAPACITOR, CHIP	16	JOHANSON-47pf 500R15N470JP4
31	CAPACITOR	10	SPRAGUE-1uf TANT, 35V
32	CAPACITOR	29	SPC TECHNOLOGY-0.1μf
33	CAPACITOR, ADJ	1	JOHANSON-47pF-9621
34	CONNECTOR, BNC	5	TRUMPETER-CBJ20, 50Ω
35	TEST POINTS	2	TEKTRONIX 131-2766-01, 136-0352-02
36	PIN RECEPTACLE	42	MILL MAX-0552-1-15-15-11-27-10-0
37	PIN SOCKET	9	SAMTEC-SL-132-G-12
38	SOCKET, 24PIN	1	SAMTEC-ICO-624-NGT
39	PRINTED CIRCUIT BOARD	1	HONEYWELL-EB101
40	TEST POINTS	2	COMPONENTS CORP. TP-102
41	CAPACITOR	2	Q-PAK Q302
42	JUMPER PINS	18	SAMTEC

EB101 CLOCK DIVIDER BOARD

NO.	DESCRIPTION	QTY.	MANUFACTURER / PART NO.
43	F100131	1	FAIRCHILD TRIPLE D-TYPE FLIP-FLOP
44	CAPACITOR	2	.1μF
45	TEST POINTS	2	TEKTRONIX 131-2766-01, 136-0352-02
46	RESISTOR	6	1KΩ, 1/8w 5%
47	RESISTOR	4	220Ω, 1/8w 5%
48	RESISTOR	4	330Ω, 1/8w 5%
49	CAPACITOR	1	JOHANSON-47pF CHIP
50	TEST POINTS	2	COMPONENTS CORP.-TP-102

EB102 REVISION B PARTS LIST

AN102

PARTS LIST				
NO.	REF. DESIG.	QTY.	DESCRIPTION	MANUFACTURER / PART NO.
1	C1, 3, 5, 8, 12, 13, 15	7	CAPACITOR, .1 μ f - 50V	AVX / SR205E104MAA
2	C2, 4, 7, 14	4	CAPACITOR, 47pf - CHIP	JOHANSON / 500R15N470JP4
3	C10, 11, (NOTE 3)	2	CAPACITOR, SEALTRIM 5-20pf	JOHANSON / 9629
4	CR1, 2	2	DIODE, 1N4001	
5	E1, 2	2	JUMPER PINS (HEADER STRIP)	CYPRESS / TSW-1-36-07-T-S
6	FL1	1	FILTER, 90MHz LOWPASS	MINICIRCUITS / PLP-100
7	J1, 2 (NOTE4)	2	RECEPTACLE, BNC	TRUMPETER / CBJ20
8	L1, 2	2	RF BEAD	FAIR-RITE / 2743001111/2
9	P1	1	PLUG	MOLEX / 09-18-5031
10	R1, 2	2	RESISTOR, 10K OHM	HAMILTON / AVNET / CF1/8-10K-5%-T/R
11	R4, 12	2	RESISTOR, 33 OHM	HAMILTON / AVNET / CF1/8-33-5%-T/R
12	R5	1	RESISTOR, 25K OHM	HAMILTON / AVNET / CF1/8-25K-5%-T/R
13	R7 (NOTE 1)	1	RESISTOR, 1.5K OHM	HAMILTON / AVNET / CF1/8-1.5K-5%-T/R
14	R7, 8 (NOTE 2)	2	RESISTOR, 250 OHM	HAMILTON / AVNET / CF1/8-250-5%-T/R
15	R9	1	RESISTOR, 150 OHM	HAMILTON / AVNET / CF1/8-150-5%-T/R
16	R10	1	RESISTOR, 51 OHM	HAMILTON / AVNET / CF1/8-51-5%-T/R
17	R3	1	POTENTIOMETER, 10K OHM	BOURNS / 3339-1-103
18	R6, 11	2	POTENTIOMETER, 1M OHM	BOURNS / 3339-1-106
19	C6, 9	2	CAPACITOR, 1 μ f TANT, 35V	SPRAGUE / 196 DIO5X9035HAI
20	U1 (NOTE 1)	1	I.C., OP-AMP	COMLINEAR / CLC221A1
21	U1 (NOTE 2)	1	I.C., BUFF-AMP	COMLINEAR / CLC231A1
22	PCB1	1	PRINTED CIRCUIT BOARD	HONEYWELL / EB102 REV. B

NOTES:

- 1) USE ITEM NO. 13 WITH ITEM NO. 20 AND JUMPER E1, 2.
- 2) USE ITEM NO. 14 WITH ITEM NO. 21.
- 3) USE C10 WITH ITEM NO. 21 ONLY.
- 4) J2 IS MOUNTED ON THE BACKSIDE OF PCB1.

8

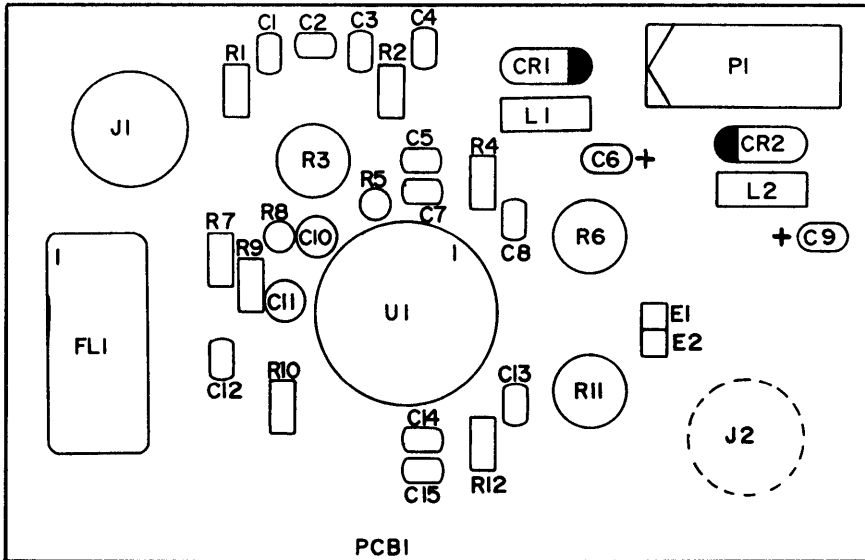
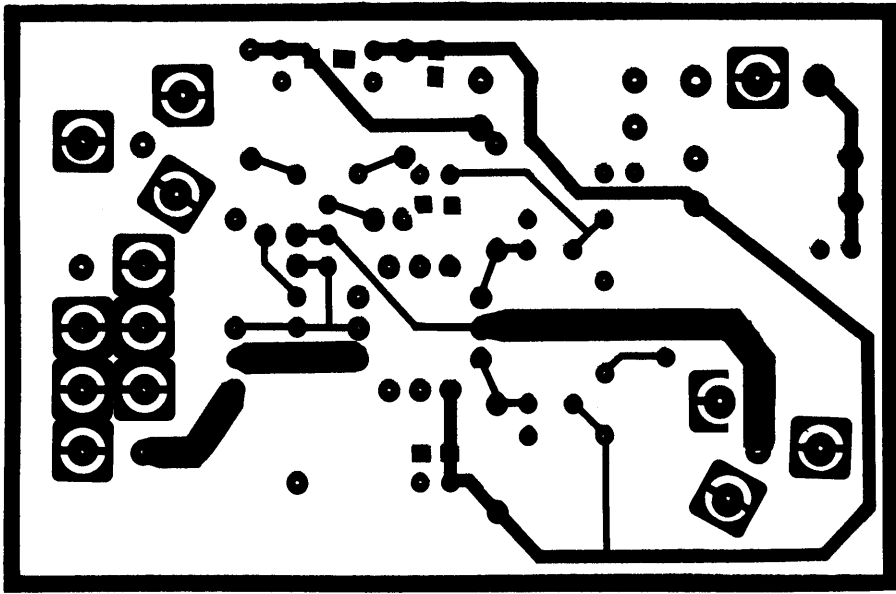


FIGURE 6 - EB102 BUFFER BOARD LAYOUT AND COMPONENT POSITION
(Not To Scale)

SET-UP PROCEDURE FOR THE EB101 DEMONSTRATION BOARD

The following setup procedure is completed at Honeywell before the EB101 board is shipped to the customer. It is not necessary for the user to perform this exercise, but it is included for informational purposes.

The EB101 demonstration board is accompanied with a literature package containing the "AN102 APPLICATION NOTE", the "HADC77200", "HDAC51400", "HDAC10181", and "HCMP96870" data sheets, and an applications department business card. Also, a power harness, and a capacitor alignment tool are included. If there are any questions, please call the applications engineer on the card.

STEP 1

Connect the wire end of the power supply harness to power supplies as shown in Figure 1C. The power harness should be connected to the board with the bevelled edges and hollow connector aligned for correct operation.

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

Table 3 (page 6) shows the power requirements for the EB101. Use the current gauges on the power supply or a DMM in line with the power lines and set on current (I). These current values will vary somewhat until all the potentiometers are adjusted. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

STEP 2

Refer to Figure 2 and 4 on the previous pages. Place a DMM probe (set to voltage selection) on the black jumpers at the input to the HADC77200 (E14). This should read -1V and is adjusted by turning potentiometer R23 (See Table 2A).

STEP 3

Again, refer to Figures 2 and 4 on the previous pages and Table 5 on this page. Place a DMM probe (set to voltage selection) on pin 3 of the OP11-A and read approximately -1.2V. If it does not, then check to see if the black jumpers for the HDAC10181/51400 are set up

TABLE 5 - EQUIPMENT LIST

- 2- SIGNAL GENERATORS CAPABLE OF PRODUCING 1MHZ AND 20MHZ SINEWAVES AT UP TO 1Vp-p OUTPUT LEVELS INTO 50Ω. H.P. 8656A OR EQUIVALENT.
- 1- OSCILLISCOPE, EITHER H.P. DIGITIZING OSCILLISCOPE MODEL 54100D OR EQUIVALENT OR TEKTRONIX MODEL 2465.
- 1- DIGITAL MULTIMETER(DMM), KEITHLEY 197 OR EQUIVALENT.
- 4- POWER SUPPLIES CAPABLE OF PRODUCING THE POWER LISTED IN TABLE 1. 2 LAMBDA LPT-7202-FM OR EQUIVALENT.
- 5- 50Ω COAX CABLES (RG58) WITH BNC TYPE CONNECTORS.
- 1- HIGH IMPEDANCE PROBE (1MΩ) - TEKTRONIX OR H.P.

for the right part (see Figure 4B). Next set the probe on pin 1 of the OP11-A. This should read -2V and is adjusted by turning potentiometer R26. Now set the probe on pin 7 of the OP11-A. This should read -2V and is adjusted by turning potentiometer R26. Now set the probe on pin 7 of the OP11-A. This should read approximately -1.5V and is adjusted by potentiometer R25. Pin 8 of the OP11-A should read -1.0V and is adjusted by potentiometer R37. On the other amplifier, OP11-B, potentiometer R38 controls the output from pin 1 and should read -0.5V. Finally, R32 sets up the output from pin 14 on OP11-B and can be set between GROUND and -50mV.

STEP 4

Refer to Figures 2 and 4. Attach a 50Ω BNC cable to the "CLK IN" BNC connector. Attach the other end to a sinewave or signal generator set at 20MHz frequency and 1Vp-p amplitude (if 1Vp-p is not available, amplitudes down to 100mVp-p are acceptable). Put a Tektronix or H.P. high impedance probe in one or both of the probe jacks immediately below the HCMP96870 comparator. Adjust potentiometer R5 to achieve a 50%

duty cycle square wave (both "high" and "low" states are the same length). Adjust potentiometer R4 if no waveform is present and/or to get rid of any jitter in the square wave (this is a hysteresis adjustment). The square wave amplitude should be approximately 900mVp-p and look like Figure 7 below.

STEP 5

Refer to Figure 2 and 4. Attach a 50Ω coax cable to the BNC connector marked "BUFFER IN". Use a second sinewave or signal generator set at 1 MHz frequency and 1Vp-p amplitude (See Figure 8). Attach another cable to the BNC connector "A/D IN / BUFFER OUT" and to an oscilloscope set at 50Ω input impedance. A 200mVp-p amplitude signal swinging around -100mVdc should appear at a 1MHz frequency (See Figure 9). If oscillation is evident (erratic signal amplitude or wrong frequency), potentiometer R22 and capacitor C25 must be adjusted. Adjust potentiometer R22 to the full counterclockwise range. Now adjust capacitor C25 to stop the oscillation. See Figures 10, 11 and 12.

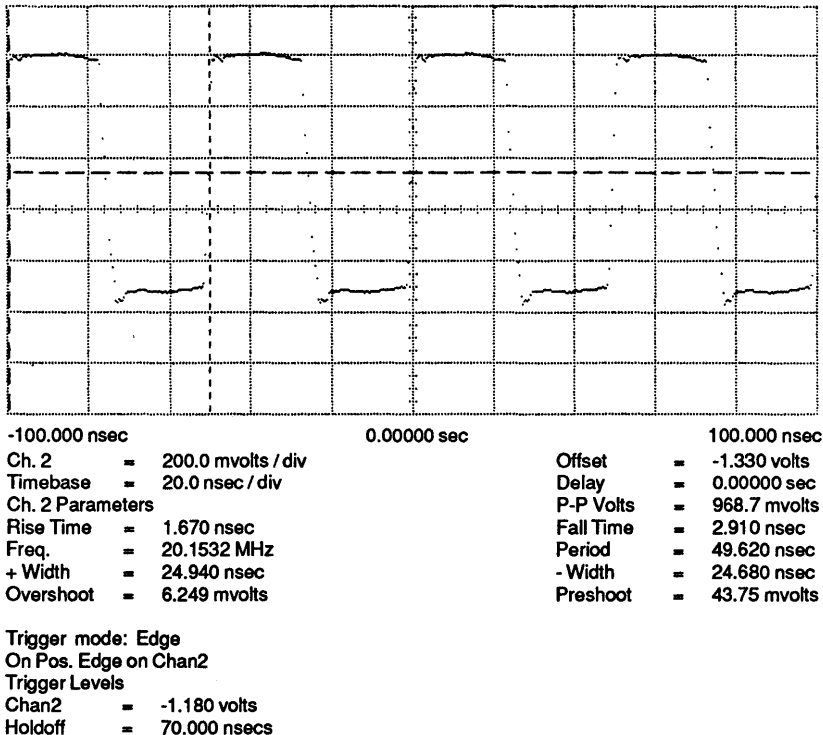
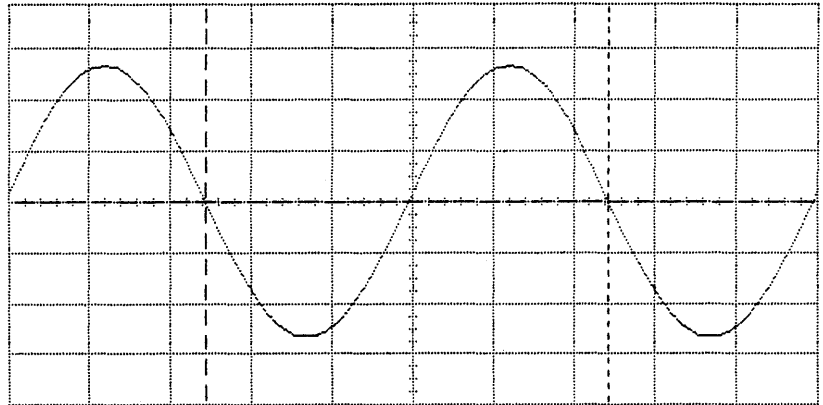


FIGURE 7 - CLOCK OUTPUT AT THE TEKTRONIX PROBE JACKS

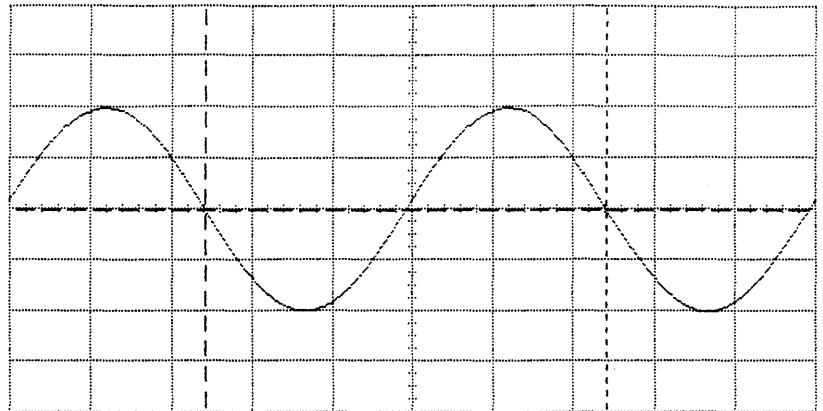
**FIGURE 8 - INPUT
SIGNAL TO THE BOARD
(50Ω INPUT
IMPEDANCE)**



-1.00000 usec		0.00000 sec		1.00000 usec
Ch. 1	=	200.0 mvolts / div	Offset	= 0.000 volts
Timebase	=	200 nsec / div	Delay	= 0.00000 sec
Ch. 1 Parameters			P-P Volts	= 1.062 volts
Rise Time	=	289.640 nsec	Fall Time	= 289.320 nsec
Freq.	=	1.00014 MHz	Period	= 999.860 nsec
+ Width	=	497.520 nsec	- Width	= 502.340 nsec
Overshoot	=	6.249 mvolts	Preshoot	= 6.249 mvolts

Trigger mode: Edge
 On Pos. Edge on Chan1
 Trigger Levels
 Chan1 = 0.000 volts
 Holdoff = 70.000 nsecs

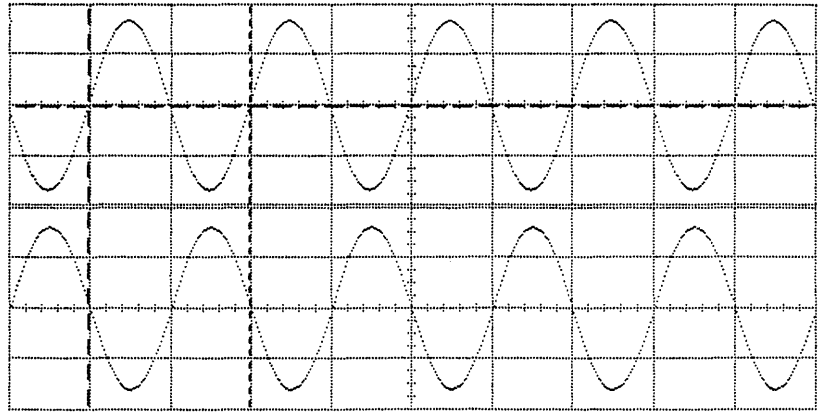
**FIGURE 9 - OUTPUT
SIGNAL FROM THE
"BUFFER OUT" BNC
CONNECTOR
(50Ω IMPEDANCE)**



-1.00000 usec		0.00000 sec		1.00000 usec
Ch. 1	=	50.00 mvolts / div	Offset	= -100.0 mvolts
Timebase	=	200 nsec / div	Delay	= 0.00000 sec
Ch. 1 Parameters			P-P Volts	= 200.0 mvolts
Rise Time	=	294.080 nsec	Fall Time	= 289.910 nsec
Freq.	=	997.904 KHz	Period	= 1.00210 usec
+ Width	=	499.810 nsec	- Width	= 502.290 nsec
Overshoot	=	1.562 mvolts	Preshoot	= 1.562 mvolts

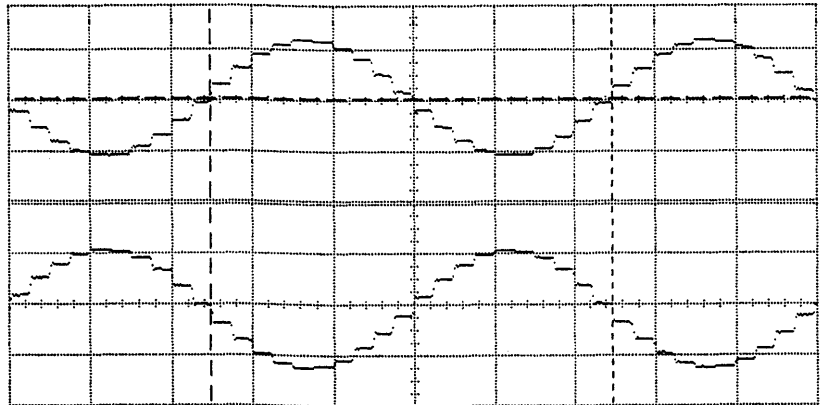
Trigger mode: Edge
 On Pos. Edge on Chan1
 Trigger Levels
 Chan1 = -100.0 mvolts
 Holdoff = 70.000 nsecs

FIGURE 12 - OSCILLATION HAS STOPPED AND THE BOTTOM WAVE-FORM IS THE SAME SHAPE AS THE TOP WAVEFORM BUT IS INVERTED



-2.50000 usec	0.00000 sec	2.50000 usec
Ch. 1 = 200.0 mvolts / div		Offset = 0.000 volts
Ch. 2 = 40.00 mvolts / div		Offset = -102.0 mvolts
Timebase = 500 nsec / div		Delay = 0.00000 sec
Ch. 1 Parameters		P-P Volts = 665.6 mvolts
Rise Time = 290.790 nsec		Fall Time = 291.830 nsec
Freq. = 999.990 KHz		Period = 1.00001 usec
+ Width = 500.180 nsec		- Width = 499.830 nsec
Overshoot = 0.000 volts		Preshoot = 0.000 volts

FIGURE 13 - OUTPUT WAVEFORMS FROM "OUT-" AND "OUT+" WITHOUT THE CLOCK DIVIDER BOARD INSERTED AND THE CLOCK JUMPERS CONNECTED AS SHOWN IN THE TOP OF FIGURE 4

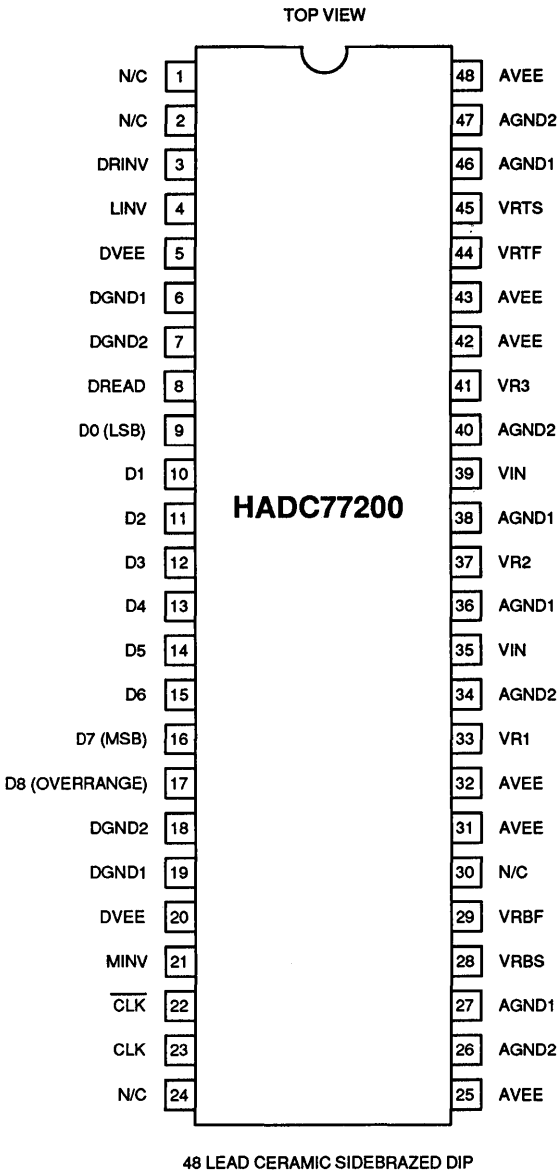


-1.00000 usec	0.00000 sec	1.00000 usec
Ch. 1 = 400.0 mvolts / div		Offset = -964.0 mvolts
Ch. 2 = 400.0 mvolts / div		Offset = -544.0 mvolts
Timebase = 200 nsec / div		Delay = 0.00000 sec
Ch. 1 Parameters		P-P Volts = 912.5 mvolts
Rise Time = 290.470 nsec		Fall Time = 297.770 nsec
Freq. = 1.00264 MHz		Period = 997.370 nsec
+ Width = 499.250 nsec		- Width = 498.120 nsec
Overshoot = 6.249 mvolts		Preshoot = 6.249 mvolts

Trigger mode: Edge
 On Neg. Edge on Chan1
 Trigger Levels
 Chan1 = -964.0 mvolts
 Holdoff = 70.000 nsecs

PIN ASSIGNMENTS HADC77200

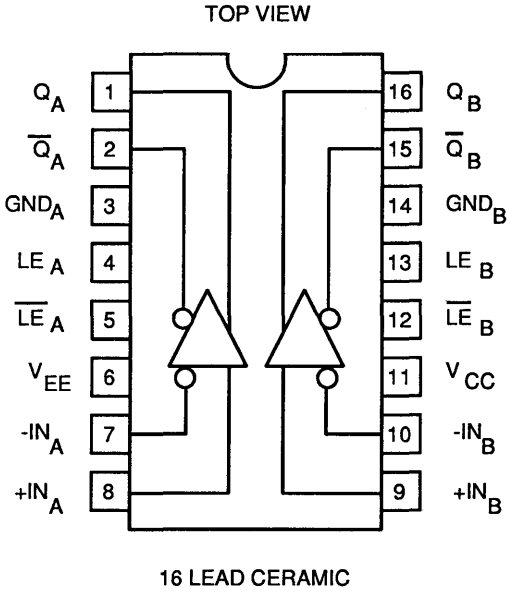
PIN FUNCTIONS HADC77200



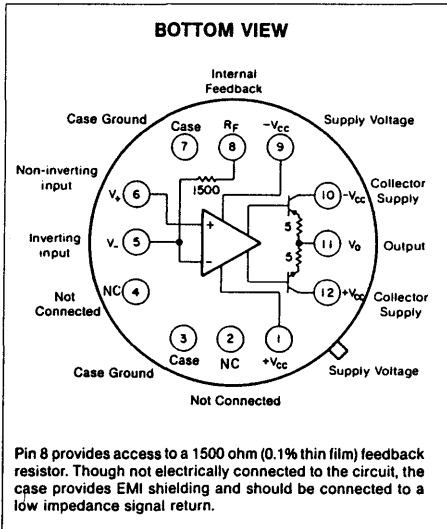
NAME	FUNCTION
DRINV	Data Ready Inverse
LINV	D0 through D6 Output Inversion Control Pin
AVEE	Negative Analog Supply Nominally -5.2V
DVEE	Digital Analog Supply Nominally -5.2V
DGND1	Digital Ground 1
DGND2	Digital Ground 2
DREAD	Data Ready Output
DO	Digital Data Output Pin 1 (LSB)
D1 - D6	Digital Data Output Pin 2 Through 6
D7	Digital Data Output Pin 7 (MSB)
D8	Ovrrange Output
MINV	D7 Output Inversion Control Pin
CLK	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
VRBS	Reference Voltage Bottom, Sense Nominally -2.0V
VRBF	Reference Voltage Bottom, Force Nominally -2.0V
VR1	Reference Voltage Tap 1
AGND1	Analog Ground 1
VIN	Analog Input, can be connected to the input signal or used as a Sense
AGND2	Analog Ground 2
VR2	Reference Voltage Tap 2
VIN	Analog Input, can be connected to the input signal or used as a Sense
VR3	Reference Voltage Tap 3
VRTS	Reference Voltage Top, Sense Nominally 0V
VRTF	Reference Voltage Top, Force Nominally 0V

FIGURE 8B
PIN ASSIGNMENTS HCMP96870

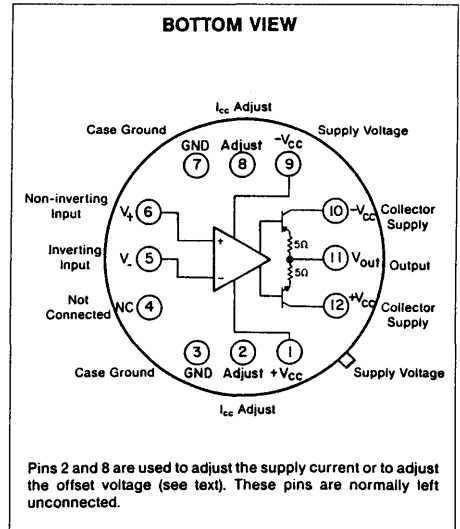
PIN FUNCTIONS HCMP96870



NAME	FUNCTION
\bar{Q}_A	Output A
Q_A	Inverted Output A
GND_A	Ground A
\overline{LE}_A	Latch Enable A
\overline{LE}_A	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
\overline{LE}_B	Inverted Latch Enable B
\overline{LE}_B	Latch Enable B
GND_B	Ground B
\bar{Q}_B	Inverted Output B
Q_B	Output B

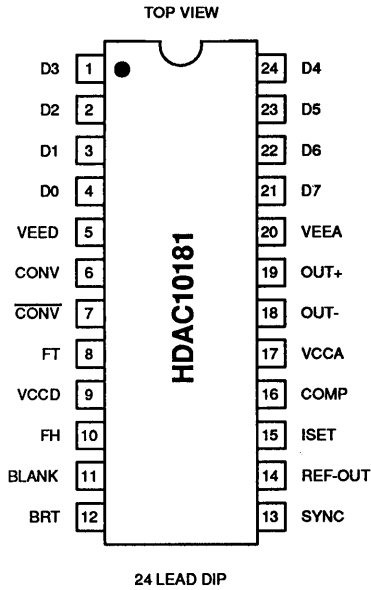


PIN ASSIGNMENTS
COMLINEAR CLC221



PIN ASSIGNMENTS
COMLINEAR CLC231

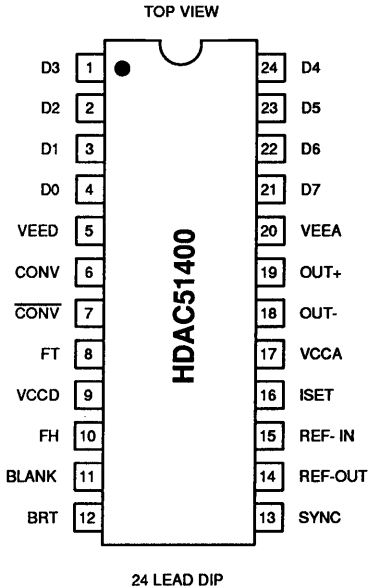
PIN ASSIGNMENTS HDAC10181



PIN FUNCTIONS HDAC10181

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
ISET	Reference Current + Input
COMP	Compensation Input
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

PIN ASSIGNMENTS HDAC51400



PIN FUNCTIONS HDAC51400

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
REF-IN	Reference Input
ISET	Reference Current
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

EB103 EVALUATION BOARD APPLICATION NOTE FOR TWO PING-PONGED 8-BIT FLASH A/D CONVERTERS Tom DeLurlo, Senior Applications Engineer

FEATURES

- 400 MSPS NOMINAL CONVERSION RATE
- 100 to 150 MHz Full Scale input Bandwidth
- 1/2 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Preamp Comparator Design/Optional Input Buffer
- ECL Timing skew clock generator
- Improved D/A Output Drive, Doubly-Terminated 50Ω

APPLICATIONS

- Evaluation of HADC77200/300 A/D Converters
- Evaluation of HDAC51400 D/A Converter
- Digital Oscilloscopes
- Transient Capture
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

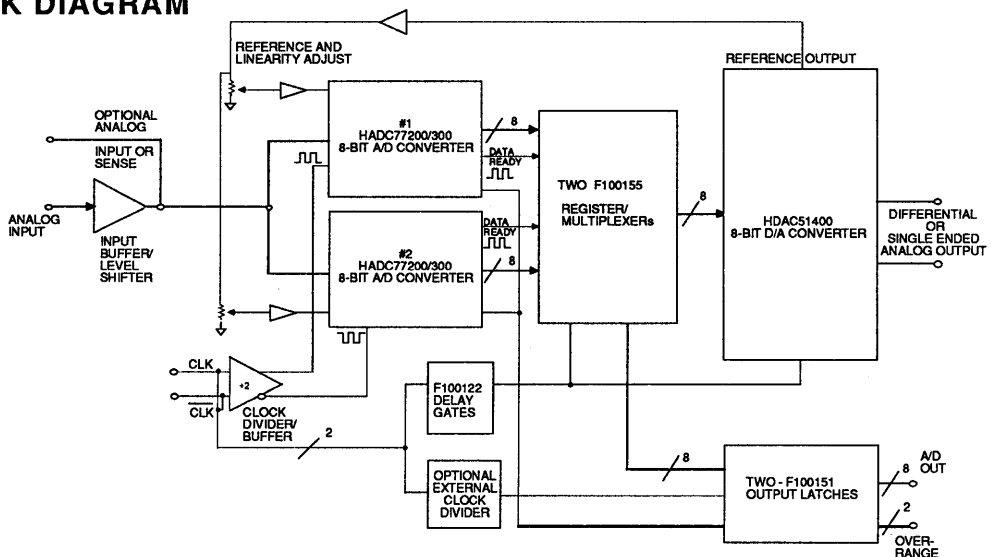
The EB103 evaluation board is intended to show the performance of the HADC77200 or flash A/D converters in a ping-ponged mode, and the HDAC51400 Ultra High Speed D/A converter for reconstruction. Included on the unit are two 100K ECL multiplexers for the combining the ping-ponged A/D converters' 16 bits of output data in to 8 bits at twice the speed. The high speed data is routed between the A/D and D/A, and also off the board as full speed or as divided down data (external clock) for slower speed FFT measurements. This is shown in the block diagram below.

The HADC77200 is a monolithic, 8-bit flash A/D converter capable of digitizing a 2 Volt analog input signal with full scale frequency components to 100 MHz at a 150 MSPS update rate. For most applications, no external sample-and-hold is required for accurate conversion due to the device's wide bandwidth.

The HDAC51400 is a monolithic 8-bit D/A converter capable of converting data at rates of 400 MWPS. The part has optional video controls and can directly drive doubly-terminated 50 or 75Ω loads to standard composite video levels. The DAC has an internal reference to supply itself and the two HADC77200 with a stable voltage reference. It also has gain control to provide different output voltage swings so it can be used as a standard voltage output DAC.

The HCMP96870A is a dual high speed differential voltage comparator used to generate an adjustable ECL compatible clock signal for timing skew between the two A/D converters and D/A converter.

BLOCK DIAGRAM



GENERAL INFORMATION

The EB103 board is a four layer board that is manufactured for true microstrip performance. The two center copper planes are welded together to form a large ground plane. The plane is broken into digital and analog grounds to provide separate grounding for digital and analog components to achieve low noise operation. The analog inputs, outputs and clock inputs are connected with standard 50 Ω BNC connectors. All interconnects achieve 50 line impedance with 50 thevenin equivalent terminations at the end of the ECL lines. Tektronix high impedance probe jacks are provided to monitor the clock lines and LSBs. Standard -5.2V, +5V, and 12 to 15 Volt power supplies are required for operation of the EB103, with nominal power dissipation of less than 30 Watts. The board comes fully assembled, calibrated and tested. An optional input buffer and linearity TAP amplifiers are on board for high performance applications.

The EB103 evaluation board is a fully assembled and tested circuit board designed to aid in the evaluation of Honeywell's HADC77200/300 8-bit Flash A/D converters, HDAC54100 8-bit Ultra High Speed D/A converter, and the HCMP96870/A dual Voltage comparator. The board contains circuitry for buffering the input signals, generating reference voltages, adjusting and dividing the A/D data and clock, and generating delays for ECL level differential clock signals. All digital inputs and outputs are 10KH and 100K ECL compatible and provisions are made for gain, offset and linearity adjustments.

There are jumper options available to adjust clock delay between the A/D and DAC as well as Potentiometers to adjust the comparator thresholds for optimum time skew performance. The external clock option provides the ability to run the output data from the F100151 flip-flops at a slower speed for connection to a logic analyzer for digital performance tests such as FFT and Histogram, etc. (see HADC77200/300 data sheet). In addition, 100MHz or 200MHz low pass input and output filters are on board for anti-aliasing and clock noise frequency rejection.

ANALOG INPUT BUFFER

The analog input buffer is shown in Figure 1. This section consists of a low pass filter, and the CLC231 high frequency buffer-amplifier (Table 1). The input impedance is 50 Ω and the gain is set at 2X so that a 1V_{pp} analog input can be applied for best operation. Compensation components are provided and can be adjusted for the desired gain/phase response required. The compensation is factory adjusted for 50MHz bandwidth operation. The gain of the buffer amplifier can be decreased by removing the 250 Ω resistor that is connected to ground on the inverting input to achieve a voltage follower. This change will increase the

available bandwidth of the amplifier. The BNC connector shown in the schematics near the output of the buffer can be used for monitoring the buffer output and input to the HADC77200/300. The BNC should be connected to a 50 Ω terminated oscilloscope and will provide a 10X attenuated signal.

The input buffer can be bypassed by removing the 6.8 resistor at the output of the CLC231 and the 470 resistor between the BNC connector and the HADC77200/300. Bypass the 470 resistor with a jumper wire and the HADC77200/300 can now be driven directly. The input impedance to the two converters is 2K in parallel with a 120pF distributed capacitance.

The negative input to the CLC231 is tied to an offset adjust to center the input signal to the HADC77200 around -1V, which is needed if a 2V_{pp} input signal is applied. Further fine adjustment is provided by the two offset adjust pins on the CLC231.

**TABLE 1 - COMLINEAR CLC231
BUFFER AMPLIFIER**

SPECIFICATION	CLC231
Gain Range	± 1 to 5
Output (V, mA)	11, 100
Slew Rate (V/ sec)	3000
-3dB Bandwidth (Av=2)	165MHz
Settling Time (nsec, %)	12, 0.1 15, 0.05
Harmonic(dBc) Second Distortion	-55 -59

100K ECL CLOCK GENERATOR

In order to ping-pong very fast A/D converters, timing between the two devices is critical since each part contributes data every other clock pulse. Therefore clock generation is somewhat complicated (See Figure 2). Furthermore, a timing delay section and skew is necessary between the A/D and DAC.

The ECL clock section consists of two HCMP96870/A dual comparators with duty cycle and hysteresis adjust

potentiometers. Also used are F100151 Hex D flip-flops, F100121 9-bit buffers, F100114 Quint Line Receivers, two low pass filters, and several jumper options for time delay.

Any type high frequency signal generator with differential ECL level outputs can be connected to the two clock BNC connectors at the inputs of the F100114 line receiver. For single-ended operation, there is a V_{bb} generator available on pin 19 which can be connected to one input of the line receiver. At least 150mV of swing must be available to achieve full output swings from the receivers in the single-ended mode.

Starting with the clock generation function for the HDAC51400 DAC and F100151 output data latches, the inverting output of one of the F100114 receivers is connected to another receiver in the same package. This is for an inversion and delay before going on to the time delay section consisting of several of the buffers in the F100121. The delay is set up to make up for time latency between the A/D converter, multiplexers and DAC. Several options are available by making a connection on the lines between the buffer outputs and PLP450 low pass filter. The filter is used to smooth out the 100K ECL output from the buffers to be used for time skew and duty cycle changes at the input to the "#1" HCMP96870A dual comparators. The time skew and duty cycle change is performed by adjusting potentiometer R2 to change the threshold of the comparator so that the devices' outputs activate at different times. The threshold inputs to the HCMP96870A comparators are connected together to a pot to also adjust the duty cycle of the clock. The latch enable pins are also connected together to a pot to adjust comparator hysteresis.

Two of the outputs of the #1 comparators are connected to the HDAC51400 clock inputs and one inverting output is connected to the F100151 output data registers that are routed to the ribbon cable connectors. The noninverting output from the comparator is fed to the F100114 receivers to obtain a differential ECL clock for the ribbon cable output. Optional external clock inputs to the HDAC51400 and F100151 are available to clock and acquire data at a slower speed. Probe test points are provided to monitor the clock lines.

The clock generation section for the two HADC77200/300s is next. The noninverting output of the first F100114 receivers is connected to the clock input of a F100151 flip-flop to divide the high speed clock in half for the A/D converters. The output is then smoothed by a 200MHz low pass filter for timing skew adjustments as before, and it is connected to the two noninverting inputs of "#2" HCMP96870A. The two comparators are configured the same way as before with hysteresis and threshold adjust. One set of differential outputs goes to the clock inputs of the "#1" A/D converter and the other set goes to the "#2" A/D converter. Probe test points are provided on each line to monitor timing skew.

VOLTAGE REFERENCE GENERATOR

There are several voltage reference options on the board to drive the two HADC77200/300 reference taps. The options are set up by soldering jumper wires across lines. The configuration shown in Figure 3 is the option that is used when the board is shipped. In this mode, the two A/D converters are driven from the same voltage reference at the top and bottom of the reference ladder. This way the A/Ds track each other. The other mode is shown in Figure 4. Here, each reference tap can be adjusted for best linearity match between the two or, if the application requires, mismatch. Each tap can be connected or just some of them according to the jumper connections made to accommodate the application. This configuration gives additional control at high speeds between the two A/D converters.

The reference voltage for the HADC77200/300 and HDAC51400 is internally generated by the D/A converter voltage reference of approximately 1.2Volts. The A/D converter's 2Volt reference, 3 voltage midtaps and ground are controlled by three PMI quad op-amps (OP-11). The magnitude of each setting is further adjusted with potentiometer R25, R26, R32, R37, and R38 per HADC77200/300 as shown in the detailed schematic (Figure 4) and board layout (Figure 5) as well as Table 3.

ANTI-ALIASING AND CLOCK NOISE FILTERS

The input to the EB103 buffer circuitry and the differential outputs from the D/A converter are provided with high frequency noise filters. The three filters are 100MHz low pass and are intended to be used with the full analog input frequency and full clock sampling rate of the HADC77200 A/D converter. The version of the board with the HADC77300 will be provided with 200MHz filters. If lower frequencies are used, the filters should be changed to filter input harmonics, clock noise, and for reconstruction filters for a particular application. Mini-Circuits inc. (see page 12) makes a range of low pass filters that fit into the same position as the 100MHz filters on the EB103 Evaluation board.

Adjustment of the clock time skews with potentiometer R2 and R5 will lower the overall noise floor by controlling the timing mismatch between the two A/D converters and the D/A converter setup and hold times.

INPUT/OUTPUT REGISTER AND MULTIPLEXER

The multiplexer section consists of two F100155 which select between each 8-bit digital data word from the output of either HADC77200/300. The choice is controlled by the SELECT pins which are tied to the DREAD (data ready) outputs of each HADC77200/300. One DREAD output is inverted by the DRINV (data ready inverse) control pin so that the output clocks are in phase. This data is then fed to the HDAC10181/51400 on the "Q" outputs of the F100155 and the "Q" outputs are tied to the F100151 hex flip-flops which are connected to the external ribbon cable connector.

A/D CONVERTER SECTION

All input pins to each HADC77200/300 are tied together to be either fed by the input buffer or by an external source. The differential clock inputs are driven 90 degrees out of phase so that when one A/D is acquiring the input signal the other is outputting data and vice-versa. The MINV and LINV inputs are left open and tied internally to an ECL low. The connection choices for determining the output logic are in Table 2.

D/A CONVERTER SECTION

The output current magnitude for the HDAC51400 is controlled by a potentiometer (R36) through the DAC's Iset control pin. In addition, two 100 MHz low pass filters are provided at both out- and out+ output pins as well as 50Ω terminating resistors. The terminating resistors can be changed to 75 Ω if desired. Keep in mind that the transmission line must be terminated at the receiving end with the same value resistor. The video and feedthrough controls are routed to the 64-pin DIN connector and are normally disabled.

A/D OUTPUT DATA SECTION

The output data from the two HADC77200/300s is available at full clock speed or at a slower speed if an external clock is used. This data is taken from the "Q" outputs of the F100155 Multiplexers and clocked into two F100151 Hex D Flip-Flops. The "Q" outputs of the flip-flops are connected to ribbon connectors for easy connection to the outside world. The external clock can be connected through 50Ω SMA connectors as shown in Figure 2 at the output of the #1 - HCMP96870A pin 2. Be sure to cut the clock trace between the comparator and SMA connector.

TABLE 2 - OUTPUT LOGIC CODING

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.
.
V _{IH}	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.
.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH}

0: V_{IL}, V_{OL}

TABLE 3 - POTENTIOMETER AND CAPACITOR ADJUSTMENTS

NO	FUNCTION
R26	Pot for adjusting gain to produce a 2V reference voltage for the VRB pin on the HADC77200 from the 1.2V reference voltage supplied by the HDAC10181/51400.
R25/ 37/38	Pots for setting the linearity adjustments at the comparator reference ladder on the HADC77200.
R32	Pot for setting the top point (VRT) on the reference voltage ladder. Nominally set at 50mV below AGND
R36	Pot for adjusting output current drive from the HDAC10181/51400 (See data sheets). V _{out} = 25.6(digital code X Iset)/RL
R2/5	Pot for setting the HCMP96870 comparator threshold voltage to adjust the ECL clock duty cycle.
R1/4	Pot for adjusting comparator hysteresis.
R23	Pot for adjusting up to a 2V offset voltage at the buffer output for driving the HADC77200.
R22/ 22A	Pot for fine adjustment of offset voltage. Used with pot R23
C25	"Lead" Capacitor for changing the damping factor of the input buffer. This has been set for a flat response.

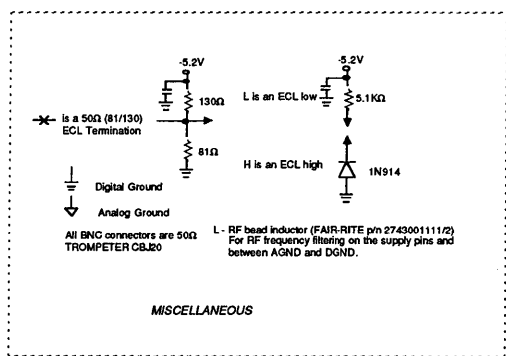
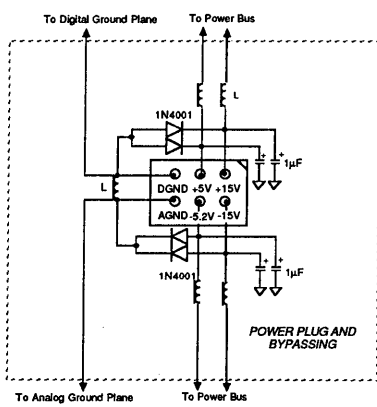
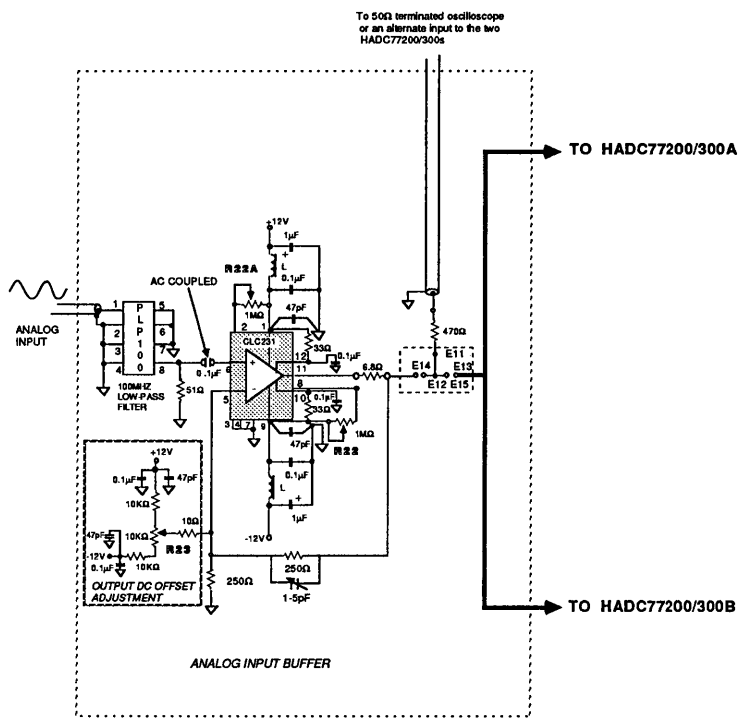


FIGURE 1 - EB103 ANALOG INPUT BUFFER, POWER SUPPLY PLUG AND TERMINATIONS.

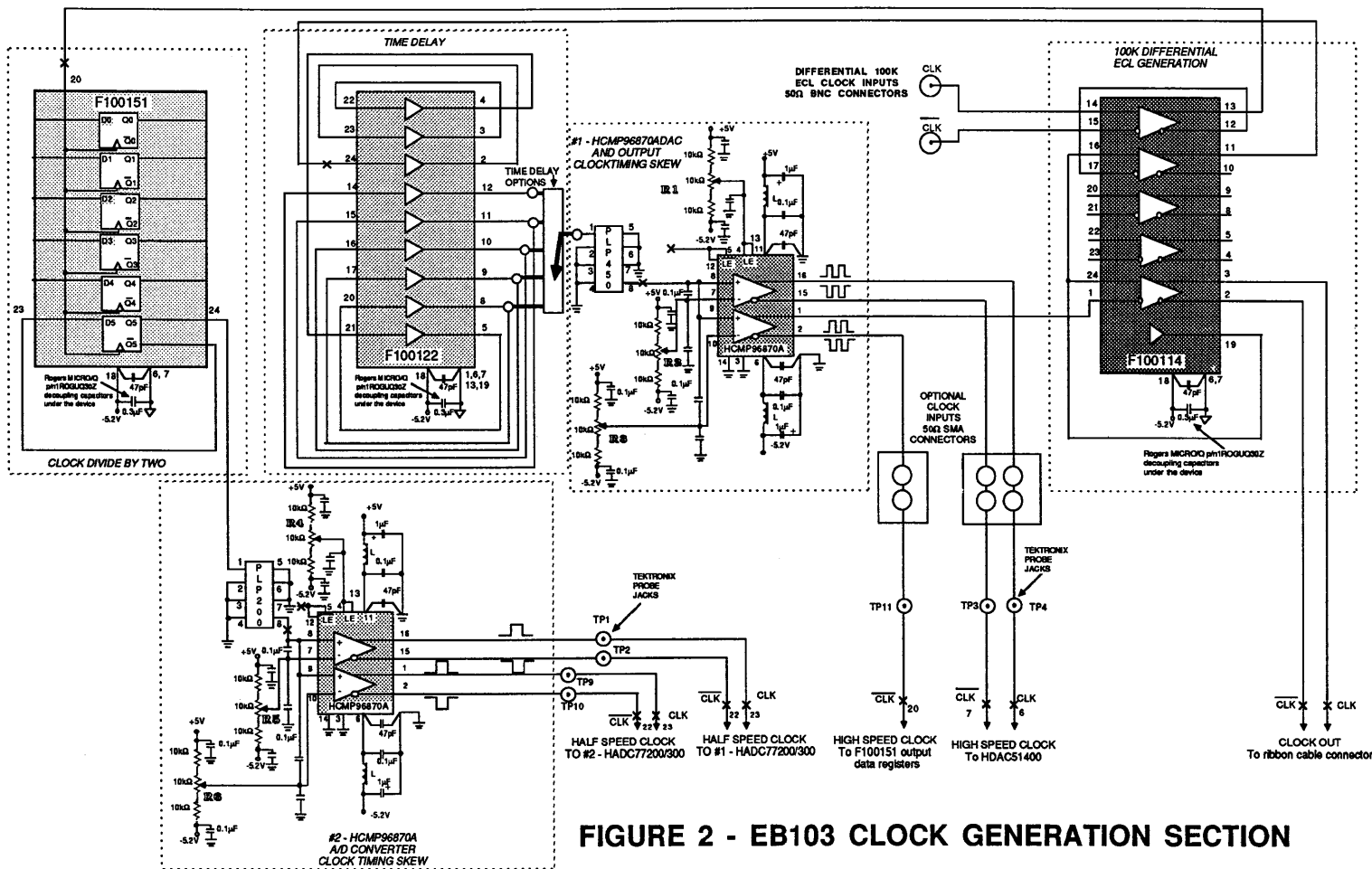


FIGURE 2 - EB103 CLOCK GENERATION SECTION

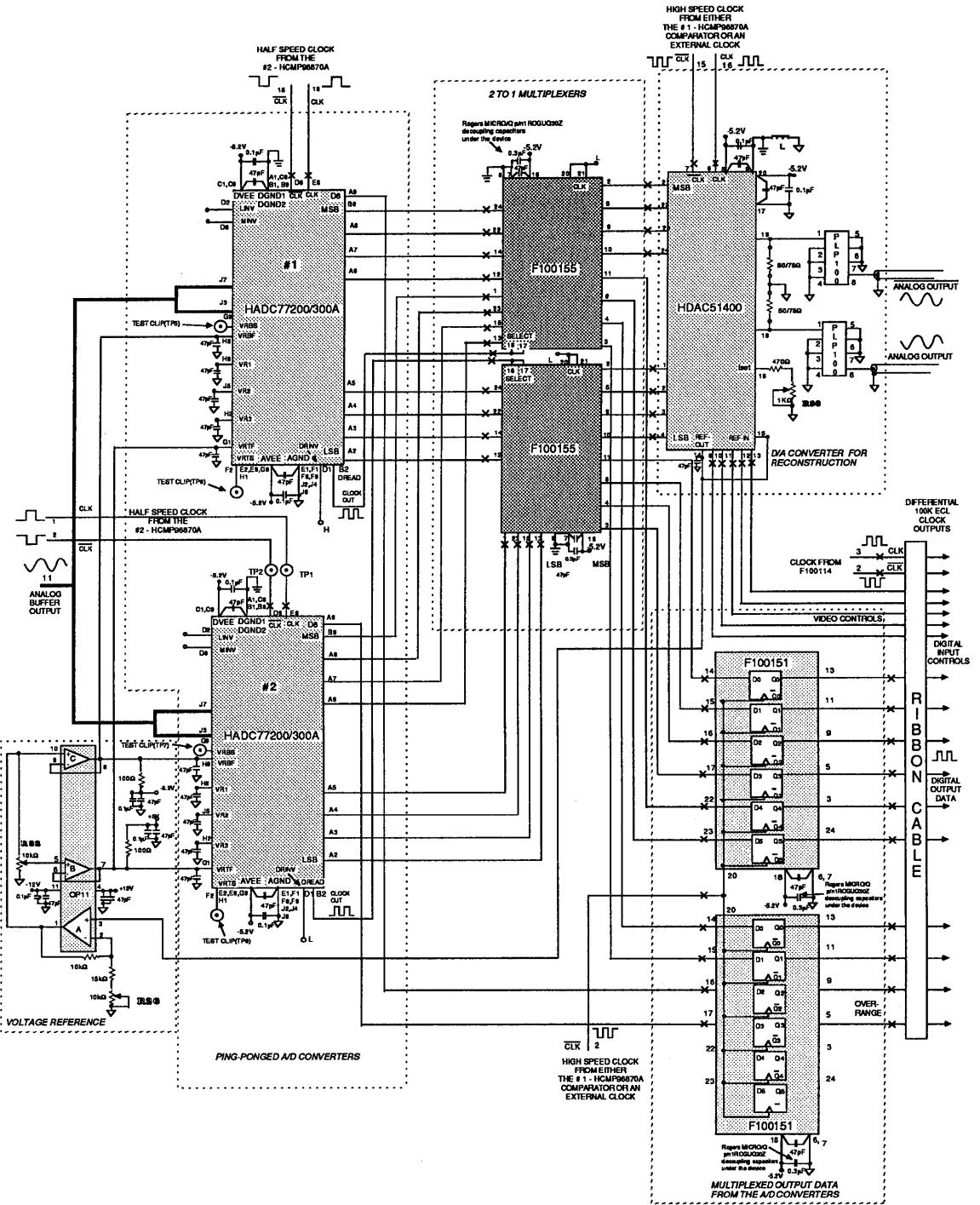


FIGURE 3 - EB103 A/D CONVERTER AND D/A CONVERTER

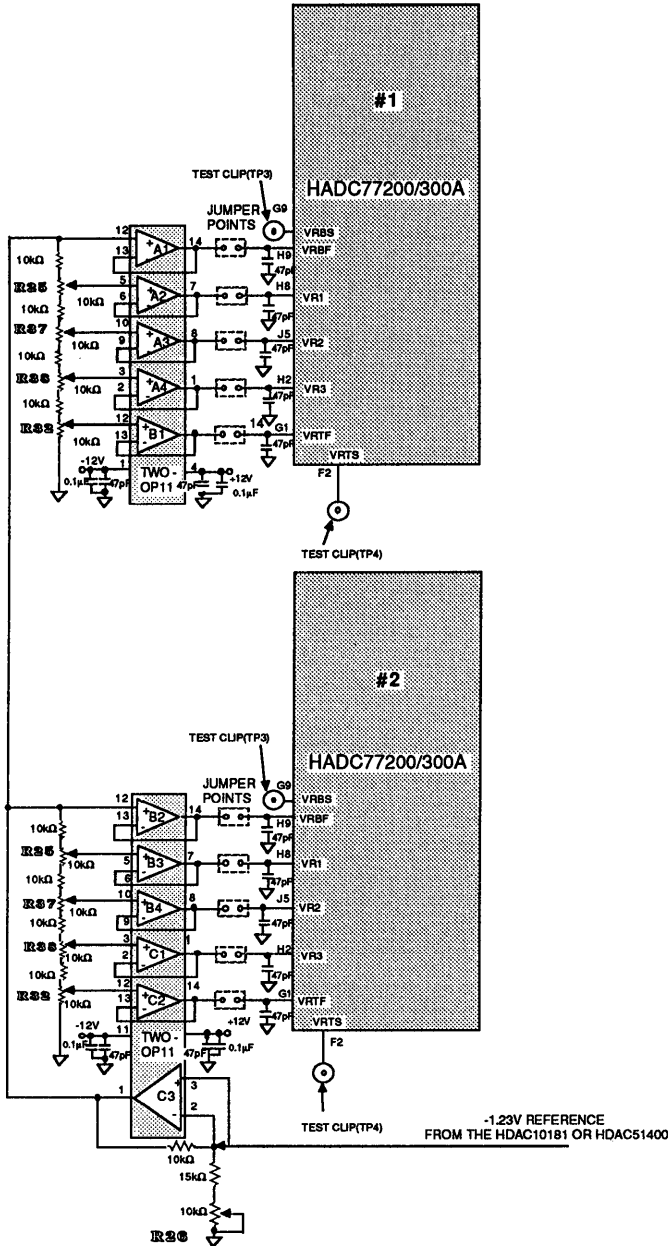
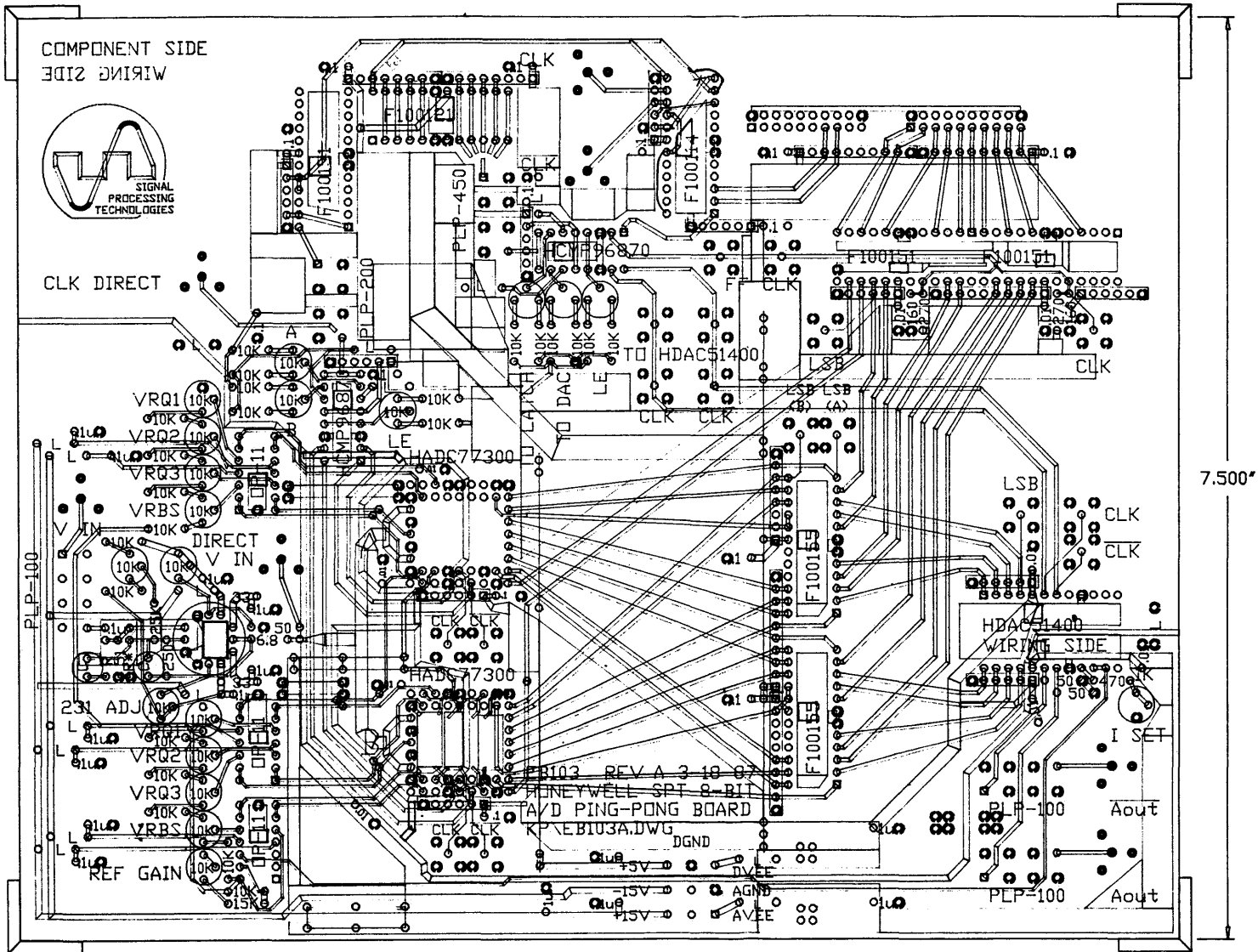


FIGURE 4 - OPTIONAL VOLTAGE REFERENCE CONTROL FOR THE TWO HADC77200/300 A/D CONVERTERS

FIGURE 5 - EB103 BOARD LAYOUT



POWER SUPPLY CONNECTIONS

Power to the EB103 is supplied through a nine pin Molex type connector. The supply lines are color coded as shown in Figure 5. Connect the wire end of the power supply harness to power supplies as shown by Figure 5 and the silk screen near the mating connector on the PC board itself. The power harness is attached to the board with the bevelled edges and hollow connector aligned to the mating connector.

The power requirements for the EB103 at different supplies is shown in Table 4. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. Supply protection diodes are on the board for any reverse polarity connection, but over-voltage protection is not provided.

TABLE 4 - POWER DISSIPATION

EB103A		
Voltage	Current	Power
+15V	.065A	.975W
-15V	.061A	.915W
+5V	.013A	.065W
-5.2V (DVEE)	4.5A	23.4W
-5.2V (AVEE)	.878A	4.56W
		29.9W

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

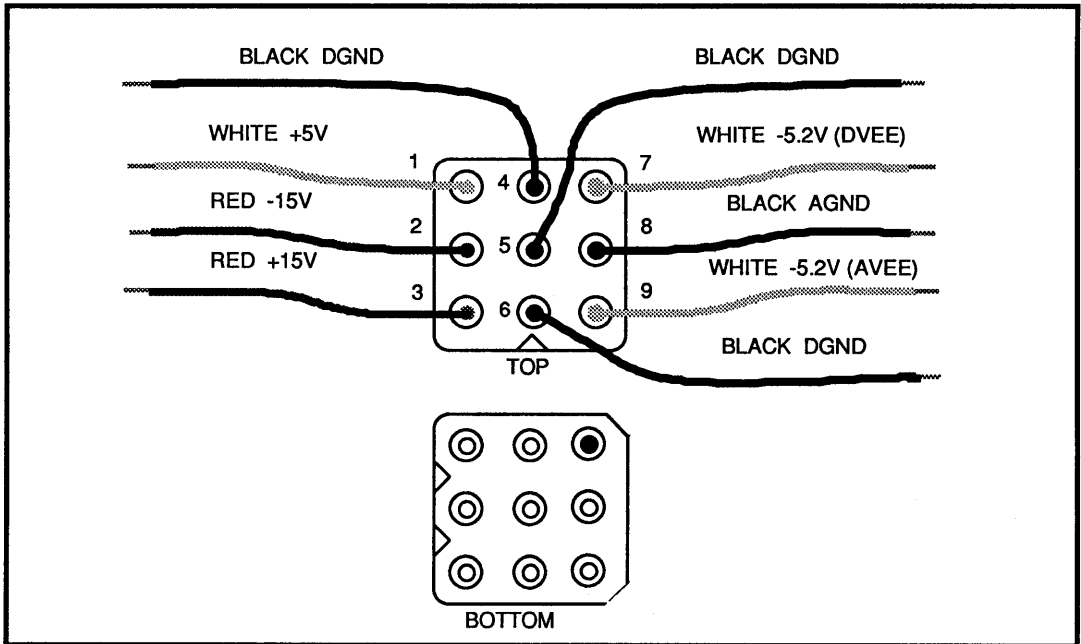
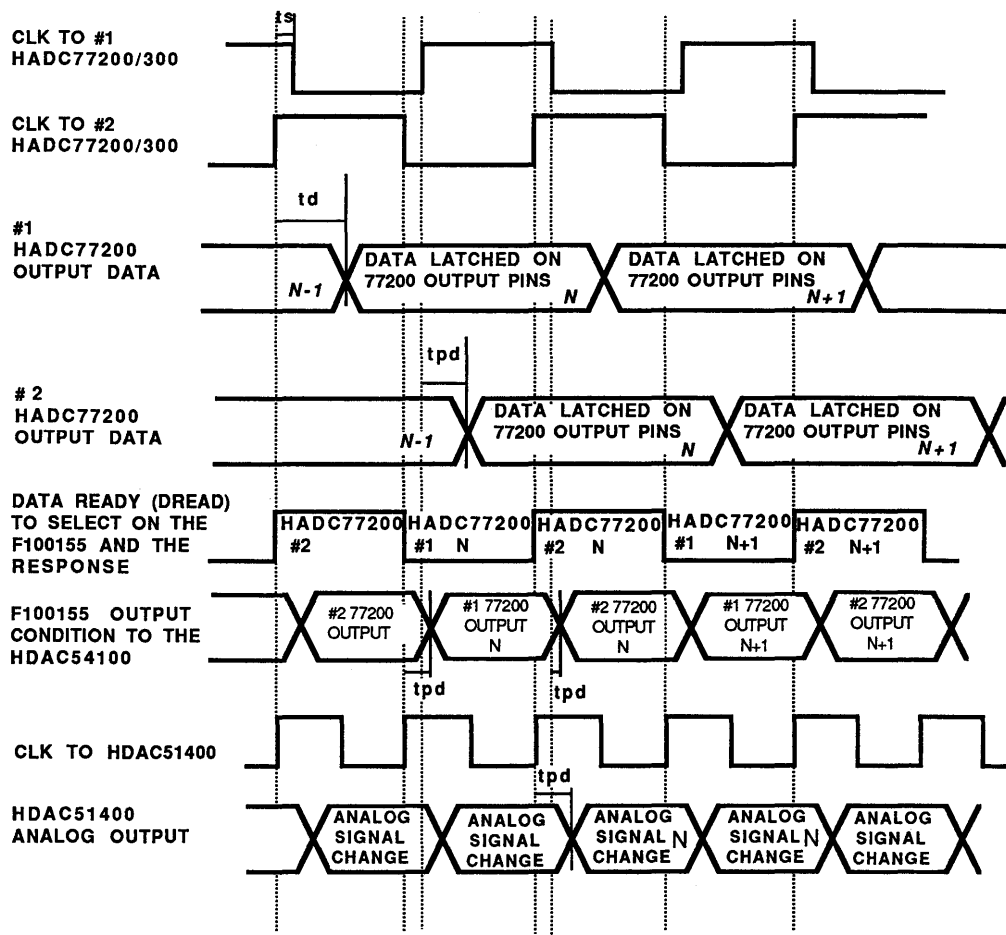


FIGURE 6 - POWER SUPPLY HARNESS CONFIGURATION

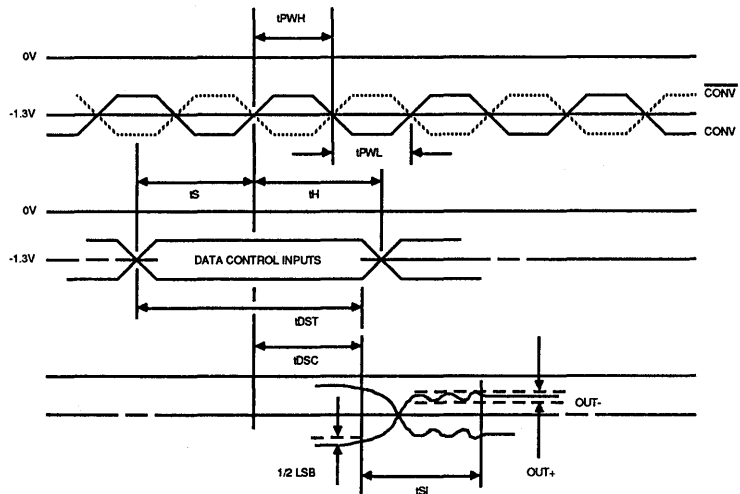
**EB103 TIMING
DIAGRAM**

FIGURE 7 - TIMING DIAGRAMS

AN103



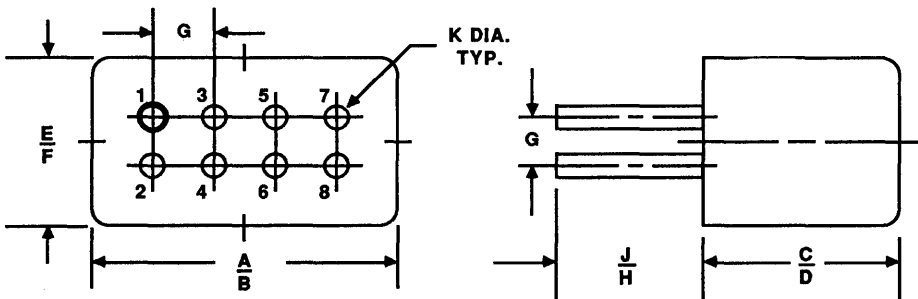
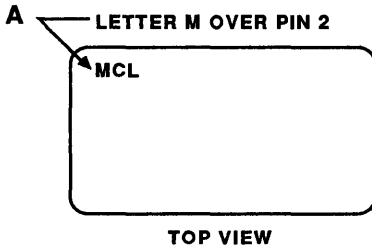
**HDAC51400
TIMING DIAGRAM**



8

MODEL NO.	PASSBAND, MHz (loss < 1dB) Min.	f _{co} , MHz (loss 3dB) Nom.	STOP BAND, MHz			VSWR,	
			(loss > 20dB) Max.	(loss > 40dB) Max.	(loss > 40dB) Min.	Passband Typ.	Stopband Typ.
PLP-10.7	DC-11	14	19	24	200	1.7	1.7
PLP-50	DC-48	55	70	90	200	1.7	17
PLP-70	DC-60	67	90	117	300	1.7	17
PLP-100	DC-98	108	146	189	400	1.7	17
PLP-150	DC-140	155	210	300	600	1.7	17
PLP-200	DC-190	210	290	390	800	1.7	17

Case no.	A	B	C	D	E	F	G	H	J	K
A01	.770 19.56	.800 20.32	.385 9.78	.400 10.16	.370 9.40	.400 10.16	.200 5.08	.20 5.08	.14 3.56	.031 .79



NOTE: BLACK BEAD INDICATES PIN 1. PIN NUMBERS DO NOT APPEAR ON UNIT. FOR REFERENCE ONLY.

PIN CONNECTIONS
SEE CASE STYLE OUTLINE DRAWING

SERIES	IN	OUT	GROUND
PLP	1	8	2, 3, 4, 5, 6, 7

FIGURE 8 - LOW PASS FILTERS

PIN FUNCTIONS HADC77200/300

NAME	FUNCTION	NAME	FUNCTION
DRINV	Data Ready Inverse	$\overline{\text{CLK}}$	Inverse ECL Clock Input Pin
LINV	D0 through D7 Output Inversion Control Pin	CLK	ECL Clock Input Pin
AVEE	Negative Analog Supply Nominally -5.2V	VRBS	Reference Voltage Bottom, Sense Nominally -2.0V
DVEE	Digital Analog Supply Nominally -5.2V	VRBF	Reference Voltage Bottom, Force Nominally -2.0V
DGND1	Digital Ground 1	VR1	Reference Voltage Tap 1
DGND2	Digital Ground 2	AGND1	Analog Ground 1
DREAD	Data Ready Output	VIN	Analog Input , can be connected to the input signal or used as a Sense.
DO	Digital Data Output Pin 1 (LSB)	AGND2	Analog Ground 2
D1-D6	Digital Data Output Pin 2 Through 6	VR2	Reference Voltage Tap 2
D7	Digital Data Output Pin 7 (MSB)	VIN	Analog Input , can be connected to the input signal or used as a Sense.
D8	Overrange Output	VRTS	Reference Voltage Top, Sense Nominally 0V
MINV	D7 Output Inversion Control Pin	VRTF	Reference Voltage Top, Force Nominally 0V

FIGURE 9 - PIN ASSIGNMENT HADC77200/300

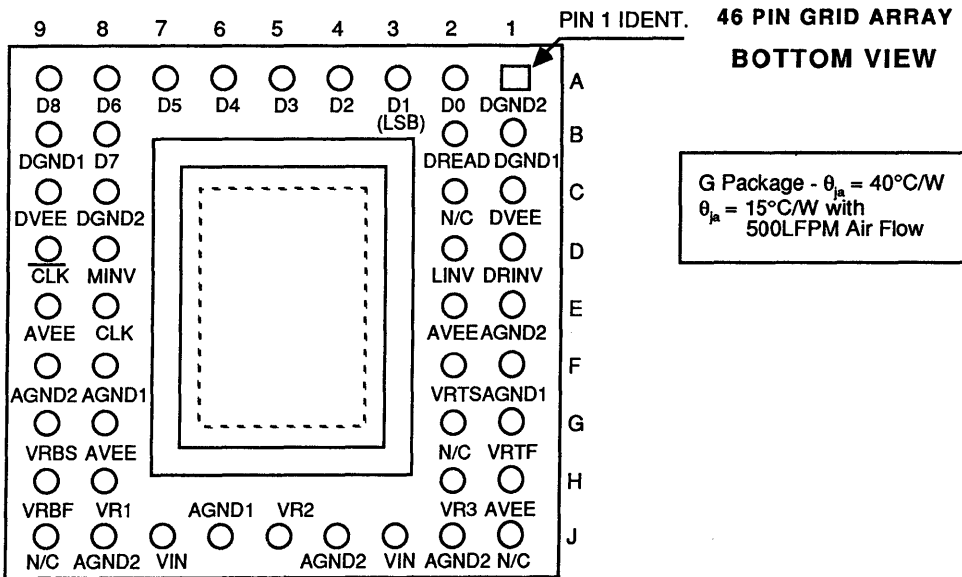
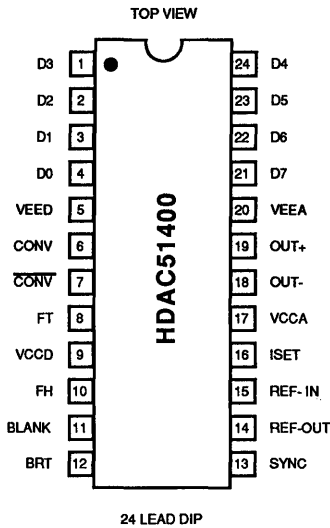


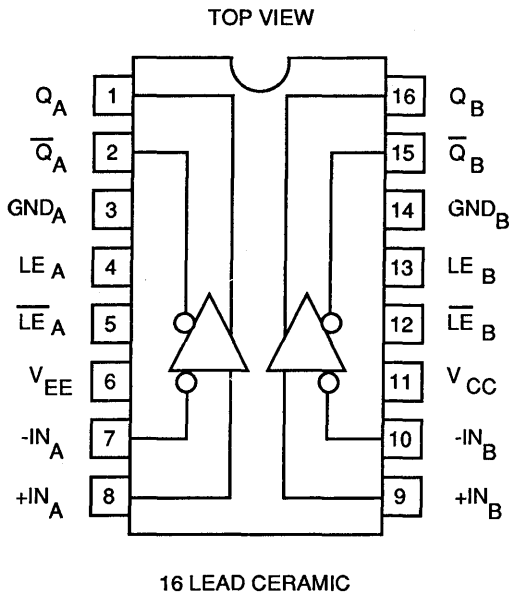
FIGURE 10 - PIN ASSIGNMENTS HDAC51400



PIN FUNCTIONS HDAC51400

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
VEED	Digital Negative Supply
CONV	Convert Clock Input
CONV	Convert Clock Input Complement
FT	Register Feedthrough Control
VCCD	Digital Positive Supply
FH	Data Force High Control
BLANK	Video Blank Input
BRT	Video Bright Input
SYNC	Video SYNC Input
REF-OUT	Reference Output
REF-IN	Reference Input
ISET	Reference Current
VCCA	Analog Positive Supply
OUT-	Output Current Negative
OUT+	Output Current Positive
VEEA	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5

FIGURE 11
PIN ASSIGNMENTS HCMP96870



PIN FUNCTIONS HCMP96870

NAME	FUNCTION
QA	Output A
QA	Inverted Output A
GND _A	Ground A
LE _A	Latch Enable A
LE _A	Inverted Latch Enable A
VEE	Negative Supply Voltage
-IN _A	Inverting Input A
+IN _A	Non-Inverting Input A
+IN _B	Non-Inverting Input B
-IN _B	Inverting Input B
VCC	Positive Supply Voltage
LE _B	Inverted Latch Enable B
LE _B	Latch Enable B
GND _B	Ground B
QB	Inverted Output B
QB	Output B

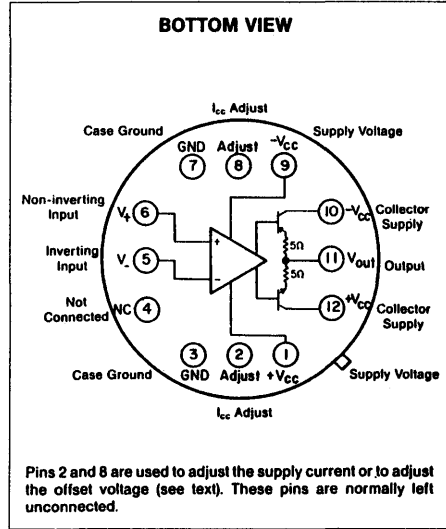


FIGURE 12 - PIN ASSIGNMENT COMLINEAR CLC231

NOTES:

VIDEO DACS AND RASTER GRAPHICS

PAUL M. BROWN

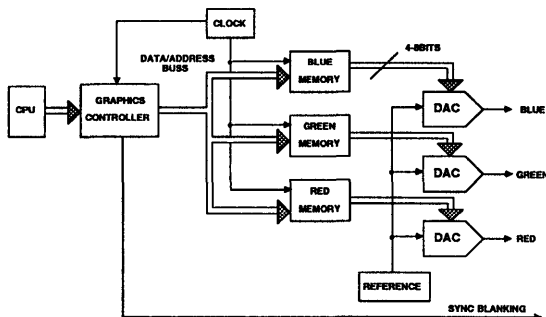
High speed DACs (digital to analog converters) and advances in CRT (cathode ray tube) technology have increased the quality and cost-effectiveness of high resolution displays. The graphics presentations available on today's personal computers and workstations range from good to nearly breathtaking. The 320X200 pixel resolution available on the IBM PC standard color display provides adequate resolution for text and simple graphics. The PC's 640X200 pixel monochrome display provides a much sharper view of text and graphics but without the dramatics of color. The IBM EGA (Enhanced Graphics Adapter) display offers color resolution to 640X350 pixels. State-of-the-art workstations, on the other hand, can achieve resolutions of over 2048X2048 pixels and palettes of nearly 17 million colors resulting in clarity rivaling 35mm film. The increasingly wide spread usage of computer terminals, personal computers and workstations for such diverse applications as word processing, desk top publishing, computer aided engineering, mechanical drafting, solids modeling and the design of integrated circuits has heightened the demand for high quality, reasonably priced graphics displays. The availability of high speed monolithic video DACs is helping to pave the way toward lowering the cost and increasing the performance of high resolution displays.

HOW VIDEO DACS ENTER THE PICTURE

The basic block diagram of a raster scan graphics system (Figure 1) has not changed dramatically in recent years. Previously, expensive laser trimmed hybrid DACs, large amounts of discrete logic and single port RAM were necessary to implement the various functions. This made high resolution graphics systems bulky, power hungry, expensive and unreliable. Now, high speed integrated circuits containing both analog and digital functions make small, efficient, reliable, reasonably priced high resolution graphics systems possible. A graphics system designed today would contain, in addition to the main processor, a graphics controller, high speed RAM, a logic array for glue logic and one or three video DACs (depending on whether the application is monochrome or color).

Graphics controllers range in function from relatively simple screen-refresh controllers, such as the Motorola 6845, to dedicated custom graphics processors. Screen-refresh controllers supply the SYNC and BLANK signals and control the flow of data between the CPU, screen buffer RAM and the video DAC. The speed and resolution of this type of controller is limited by the amount of overhead that the CPU must bear. This configuration is most frequently used in low end workstations and PCs with screen resolutions ranging from 320X200 to 1024X512. Dedicated graphics processors contain specialized instruction sets for graphics and require little CPU support. This type of architecture is found in the highest performance graphics systems.

Figure 1. Typical Raster Scan Graphics System



The image is made of pixels or dots on the screen (Figure 2). The graphics controller supplies the DAC with a digital word for each pixel in the display. Typically, the electron beam in the CRT scans across the screen in non-interlaced lines from left to right and top to bottom under the control of the horizontal and vertical SYNC and BLANK signals. The CRT is scanned one line for each pixel row in the vertical direction. As the beam scans from left to right across the face of the CRT, the video DAC receives one digital word for each pixel in the line. The refresh rate is the number of times in one second that all of the pixels in the display are redisplayed. It is easy to see that the rate at which the DAC must convert digital words to analog intensities depends upon the number of pixels per line (horizontal resolution), the number of lines (vertical resolution), the horizontal and vertical retrace (flyback) time and the refresh rate.

Figure 3 plots the DAC bandwidth (also called update rate) required for various common display resolutions. These bandwidths are calculated assuming a 60Hz refresh rate and that 30% of each frame time (the time it takes to scan one screen i.e. 1/60 of a second) is used for horizontal and vertical retrace. Another way to measure the required DAC performance is by available pixel time. The pixel time is the period during which the DAC is presented with a digital word and its output must change to the analog value of that word and illuminate the pixel. Figure 4 illustrates the approximate pixel times for various resolutions. It is important to understand that a video DAC will not settle to its rated accuracy during a pixel time but will ring above and below this level at a very high frequency. The phosphor and the human eye will serve as a low pass filter and average out these variations. The most critical concern is, therefore, the rise time of the DAC output not the settling time. A fast rise time maximizes the illumination of each pixel during the pixel time.

Figure 2. Raster Display

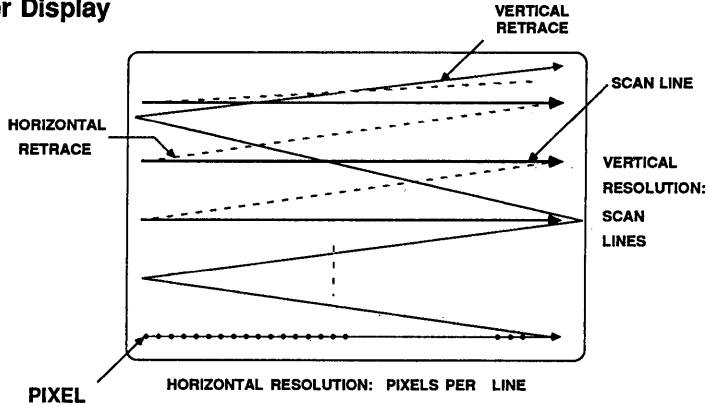
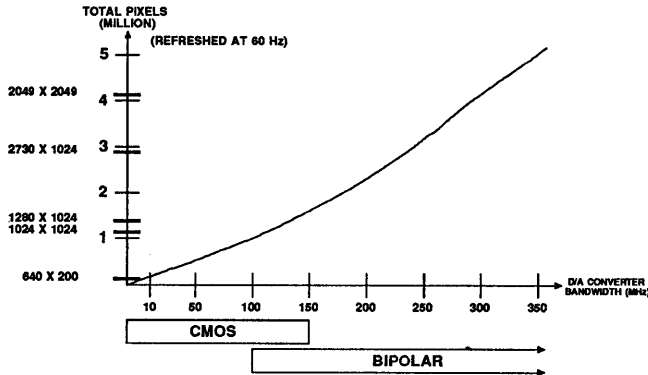


Figure 3. DAC Bandwidth vs. Resolution vs. Technology



Not only must the DAC be very fast, it must also drive a one volt signal into a doubly terminated 50 or 75 ohm load (actual impedance 25 or 37.5 ohms). Figure 5 illustrates a composite video waveform as described in the EIA RS-343 specification. The SYNC and BLANK levels are not processed through the DAC in all applications. The standard waveform (not including the 10% over bright level) is 1Vp-p which is commonly expressed as 140 IREs. An IRE, then, has a value of 7.14 mV.

The notable levels of the composite video waveform are SYNC, BLANK (the level applied during retrace and is also called "blacker than black"), REFERENCE BLACK (the darkest color), REFERENCE WHITE (the lightest color and is also called "force high") and 10% OVER-BRIGHT (sometimes called "whiter than white"). The 10% OVER-BRIGHT level is used for cursors, etc. where a large contrast is necessary with any color, even white. The portion of the waveform between reference black and reference white represents the gray scale for monochrome or potential hues for a color system. The number of discrete levels in this region depends upon the resolution of the DAC. Low end systems will use as few as 4-bits (16 levels) while high end systems intended for solids modeling applications may require 10-bits (1024 levels). Although tremendous performance is required from the DAC, it is not the only limitation on achievable resolution.

Figure 4. Pixel Time vs. Screen Resolution

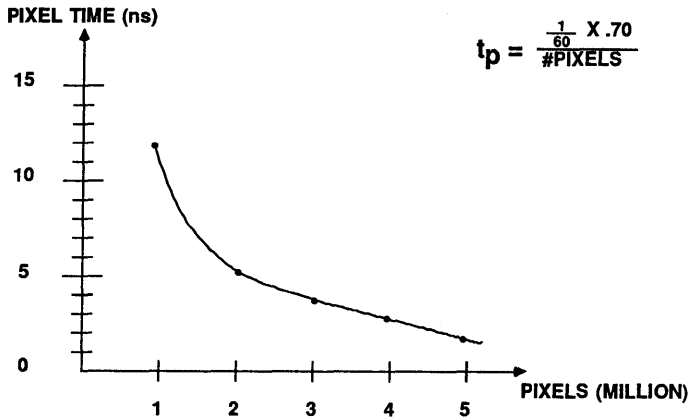
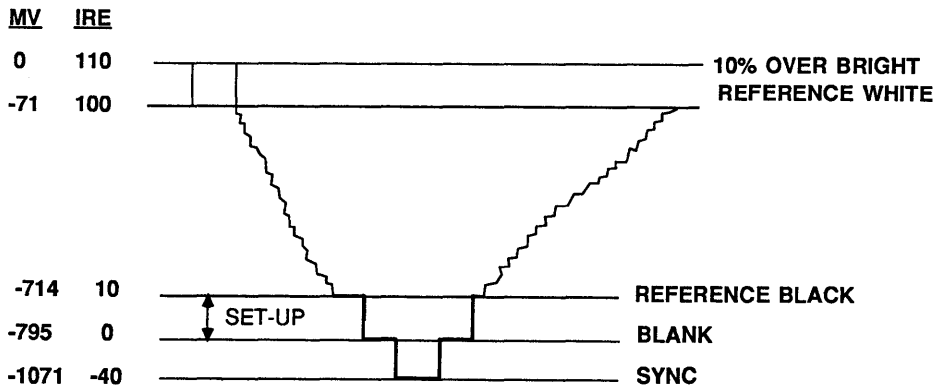


Figure 5. RS-343-A with 10 IRE Set-up



THE CRT

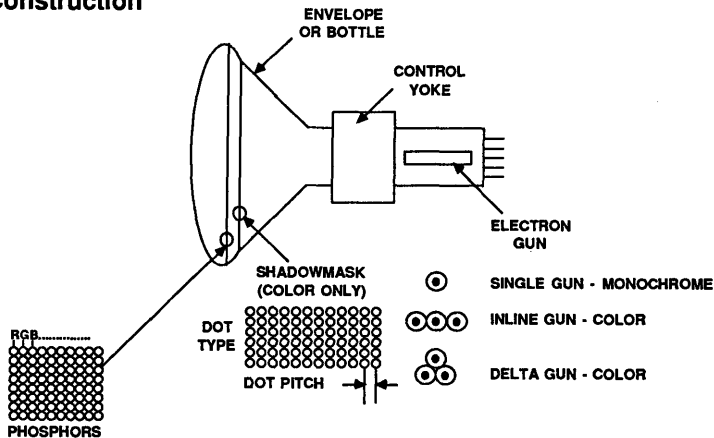
No matter how many bits of resolution or what the data rate, the graphical representation of the data depends upon the display device. The cathode ray tube or CRT is the most prevalent display technology available today. This is especially true for high resolution or color displays. The CRT (see Figure 6) consists of an evacuated glass envelope or bottle that contains an electron gun, a shadow mask (for color) and a glass surface coated with phosphors. A coil, the control yoke, is usually supplied as an integral part of the CRT. The yoke controls the deflection of the electron beam as it travels from the electron gun(s) to the phosphor coated screen. The delta gun configuration, popular in the past, requires deflection control elements that need periodic alignment. The in-line-gun, which does not require adjustment, has become the electron gun of choice in almost all applications today.

The yoke becomes a critical element for refresh rates above 40Hz due to the heat generated by the increased power necessary to drive the yoke and the back-emf that can cause arcing. A typical yoke has an inductance of $300\mu\text{H}$ and requires about 6A of drive current. The back-emf is on the order of 1200 volts. State-of-the-art yokes designed for higher resolution applications feature inductance of less than $100\mu\text{H}$ but require between 10 and 20A of drive current. The skin effect, however, increases the effective series resistance (and therefore the power dissipation) of the coil at high scan rates. Heating of the coil at higher drive currents can be minimized with the use of Litz wire. The multiple strands of Litz wire maximize the skin thickness thus reducing the effective series resistance of the coil. The lower inductance minimizes the back-emf and thus reduces the problem of arcing.

The flyback or retrace time becomes increasingly critical with higher resolution displays. The more lines of vertical resolution, the more retrace periods there are. The total time taken for horizontal and vertical retrace directly reduces the time available for writing data. This reduces each pixel time and increases the data rate required for the analog to digital converter. Typical horizontal retrace times range from 2 to $7\mu\text{s}$ per line while vertical retrace takes between 500 to $1000\mu\text{s}$ depending on display resolution and CRT design.

The most critical elements in determining CRT resolution are the beam spot size and the shadow mask. For very high resolution displays, a shadow mask dot pitch of less than .20mm is required. The phosphors on the face of the CRT are arranged in groups of red, green and blue (RGB). The electron beams from the guns are focused by the shadow mask to strike the appropriately colored phosphor. The shadow mask also insures that as the beam traces across the screen, the beam from each gun strikes only the correct color phosphor. As resolution increases, the spot size gets smaller. The smaller spot size requires more power to focus the beam and a more powerful beam to maintain the same intensity. This generates more power dissipation and more heat. The spacing between the openings on the shadow mask must also be reduced which makes the shadow mask more fragile. Only 10-20% of the beam energy strikes the phosphor. The balance of the beam heats the shadow mask causing it to bow out or dome. This mechanical deformation of the shadow mask will change the focus and blur the image. This is most apparent for the larger screen sizes. Keeping the gossamer-like shadow mask stable with localized heating from the electron beams, changes in ambient temperature and mechanical shock and vibration becomes extremely difficult. The only practical solution can be to reduce the size of the display in order to increase the mechanical strength of the shadow mask.

Figure 6. CRT Construction



VIDEO DACs

The current line-up of monolithic video DACs meets the challenge of today's high resolution graphics displays with a combination of ultra high speed process technologies and advanced architectures. The process of choice for very high speed video DACs is oxide isolated bipolar ECL. Small on-chip components reduce parasitic elements such as stray capacitance allowing high speed performance at reduced current levels. This in turn permits more circuitry to be integrated on a chip from both a die size and a power dissipation perspective.

Many of the new video DACs, such as the HDAM51100, have on chip color palettes including both address and data registers. Other possible architectures, such as found on the HDAC51600, include on-chip data multiplexers that can interleave several banks of relatively slow TTL memory into a very fast DAC to achieve the desired throughput. Having the faster circuitry such as

the color palette or the multiplexer on chip with the DAC eliminates the stray capacitances due to interchip connections. Also, the additional circuitry is fabricated on the same fast process as the DAC. All logic swings and timing will be matched and tuned for the highest performance. The cost of this higher level of integration is the loss of architectural freedom for the designer and the possible difficulty of upgrading the system later without a major revision.

Raster graphics applications can be roughly broken down into low, medium and high pixel resolution which translates directly into DAC bandwidth (update rate). Within these categories, the DACs can be sorted according to their bit accuracy. Recall that a 4-bit and an 8-bit DAC operating at a given MWPS (million words per second update rate) in a particular application will produce the same display (pixel) resolution. The 8-bit converter will, however, offer more shades of gray or more possible colors. The chart, Figure 7, lists the available monolithic video DACs, their speed, accuracy, process and special features.

Figure 7. Current Video DAC Products

Resolution	Speed MWPS	Process	Part Number	Comments
4-BITS	100	Bipolar	HDAC34020	Registered Triple DAC
	200	Bipolar	HDAC34010	Registered Triple DAC
8-BITS	100	Bipolar	HDAM51100	Registered DAC, 512 x 8 Color Look-Up with I/O
	200	Bipolar	HDAC97000	
	250	Bipolar	HDAC51600	Registered Data and Controls, Ref, 5:1 or 4:1 Data MUX
	275	Bipolar	HDAC10180A	Registered Data and Controls
	275	Bipolar	HDAC10181A	Registered Data and Controls, Reference
400	Bipolar	HDAC51400	Registered Data and Controls, Reference	

VIDEO DAC - CRITICAL PERFORMANCE PARAMETERS

SPEED - The DAC that is selected must be able to comfortably handle the required data rate with variations in power supply voltage and logic swing over the ambient temperature in which it must operate.

RISE TIME - The output of the DAC must be able to reach the intended analog value in a fraction of a pixel time. It is not important that the output settles to the final value due to the filtering effect of the phosphor and the human eye. The pixel should be illuminated at full intensity for the largest fraction of a pixel time possible.

GLITCH ENERGY - Output spikes (glitches) are a highly undesirable manifestation in any DAC and especially so in high resolution video applications. Glitches generally occur at major carries (1/4, 1/2, 3/4 and full scale) and appear as intensity variations on the screen. The magnitude of glitches is usually specified in terms of "glitch energy". This is a measure of both the amplitude and duration of the spike. A great deal of effort has gone into designing "glitch free" DACs. Some DAC architectures use special circuitry or adjustments to reduce or eliminate glitches while others are inherently "glitch free". The Honeywell line of video DACs has the lowest glitch energy in the industry.

POWER DISSIPATION - Power dissipation is important for several reasons. High power dissipation means the DAC will have a higher die temperature. This can lead to performance degradation at higher ambient temperatures and increase the load on the system power supply. Cooling will have to be provided and may require PC board layout considerations, heat sinks or forced air. (See AN108 for more information on thermal design). Many times, however, the only way to achieve the desired performance is to bite the power dissipation bullet.

RESOLUTION - The resolution of the DAC will determine the possible levels of intensity (monochrome) or the number of colors for the display. In the past, 4-bits was considered adequate. Now, most new designs are being done with eight or more bits. Solids modeling applications generally require eight to ten bits. More bits of resolution will require a correspondingly larger amount of high speed memory for support.

LOGIC COMPATIBILITY - The fastest DACs will require ECL logic to drive them at their rated speed and will therefore have ECL compatible logic inputs and require ECL power supplies. In these very high speed applications, all logic interconnections must be made using controlled impedance techniques such as microstrips or striplines to avoid undesirable reflections (ringing). Ringing caused by impedance mismatches can easily cause erroneous logic states to be sensed and will reek havoc with a high resolution display. Multiplexed DACs like the HDAC51600 allow up to five banks of relatively slow and inexpensive TTL memory to be multiplexed into a high speed DAC.

ANALOG OUTPUT DRIVE - Most monolithic video DACs will directly drive doubly terminated 50 or 75 ohm loads (25 or 37.5 ohms actual load). As speed increases, the improved bandwidth of the 50 ohm system becomes more attractive. This means that the DAC must be capable of driving a 25 ohm load.

EB104 EVALUATION BOARD INCLUDES HADC574Z 12-BIT A/D CONVERTER AND HDAC7545A 12-BIT D/A CONVERTER

Craig Wiley, Senior Applications Engineer

FEATURES:

- Provides operating environment for HADC574Z or HADC674Z and HDAC7545A Devices
- Fully Demonstrates Device Function and Resolution
- Eliminates Noisy Breadboard Evaluation Circuitry
- Buffered A/D and D/A Conversion Data Buses
- Includes Sample/Hold Amp and Output Op Amp IC's
- Unipolar or Bipolar Operation

APPLICATIONS:

- Evaluation/Comparison of HADC574/674Z Converters
- Evaluation/Comparison of HDAC7545A Converters
- System Development
- Data Acquisition Systems
- Bus Structured Instrumentation
- Process Control Systems

GENERAL DESCRIPTION

The EB104 Evaluation Board fully demonstrates the capabilities of Honeywell's HADC574/674Z and HDAC7545A 12-bit data conversion products. All of the basic power supply connections, controls lines and external components are included. The board can operate in an analog input/output fashion utilizing both A/D and D/A devices, or the devices can be operated separately. Unlike most laboratory breadboarding, the ground-planned PC board provides the necessary low-noise environment essential for 12-bit resolution. The board makes full use of connectors to allow easy hookup and operation.

Other support provided on the EB104 includes an input sample/hold amplifier, output operational amplifiers and potentiometers for offset and gain adjustments. Customization and function selections are performed by jumper pins. When considering the HADC574/674Z or HDAC7545A for system design, the EB104 Evaluation Board provides a flexible, high performance evaluation vehicle.

The EB104 is supplied with an HADC574ZBCJ and an HDAC7545AACD. It will support all 574/674 and 7545 type devices.

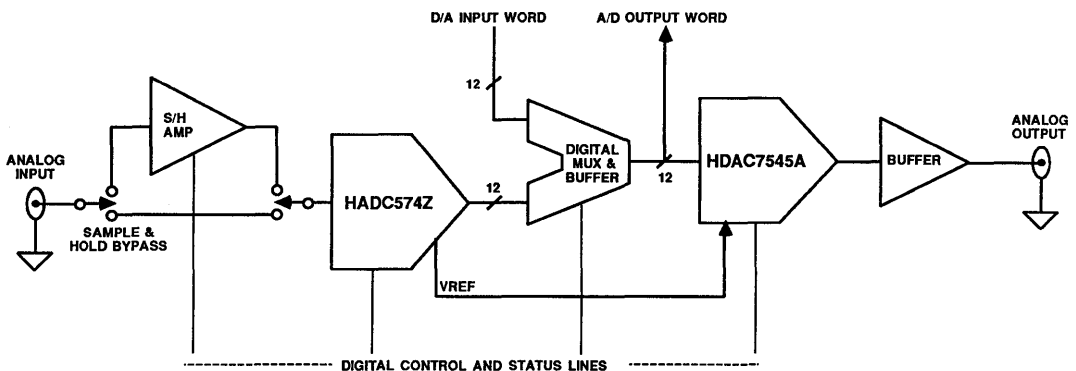


FIGURE 1 EB104 BLOCK DIAGRAM

EB104 GENERAL INFORMATION

The EB104 Evaluation Board is a fully assembled and tested circuit board developed to aide in the evaluation of Honeywell's HADC574Z or HADC674Z and HDAC7545A. A Power supply cable is supplied with the board and requires connection to +5V, +15V, and -15V. Standard BNC connectors facilitate analog input and output and 26 pin ribbon connectors provide digital interfacing. This document, along with the HADC574/674Z and HDAC7545A data sheets, is designed to serve as an operating guide.

The EB104 circuitry consists of three main sections: the Analog/Digital Conversion Section, the Multiplexer/Buffer Section, and the Digital/Analog Conversion Section.

THE A/D CONVERSION SECTION

The heart of this section is the on board HADC574Z or optional HADC674Z 12-bit A/D converter. The HA2425 sample and hold amplifier can support the A/D and can be replaced by several other types of S/H amps. Jumper pins allow the the S/H amp to be connected or bypassed. When connected, the S/H amp samples the analog input signal and outputs the it to the HADC574/674Z. When bypassed, the analog input is applied directly to the HDAC574/674Z. In either case, the 10V or 20V analog input of the HADC574/674Z can be selected with jumper pins. Another set of jumper pins allow the HADC574/674Z to be configured for either unipolar or bipolar input conditions. Trim potentiometers are used to zero the S/H amp offset voltage and trim the HADC574/674Z offset and gain values.

Control and status of the HADC574/674Z and S/H amp is facilitated by the digital control I/O ribbon connector. For convience, jumpers can be used at the ribbon connector to tie particular inputs high or low. Additionally, a jumper can be connected between the HADC574/674Z's STATUS output and the S/H amp's S/H input; this automatically provides the appropriate "Hold" command upon a user-initiated Convert command.

With the proper input control logic conditions, the HADC574/674Z can output data in one 12-bit word or two 8-bit words. When using the 8-bit mode, the EB104 has jumper pins that allow the appropriate connections between HADC574/674Z data output pins.

The 12 output data bits of the HADC574/674Z are fed to the Multiplexer/Buffer Section.

THE MULTIPLEXER/BUFFER SECTION

The main purpose of this section is to select input data for the D/A converter. It allows selection of either the A/D converter's output or user-supplied data from the data input ribbon connector. Secondly, it provides buffering between the input and output ribbon connectors and the data conversion IC's.

The multiplexer/buffer section consists solely of three 74LS157 logic IC's which are quad 2-to-1 data selectors/multiplexers. Control inputs (SELECT and STROBE) are available at the control I/O ribbon connector.

THE D/A CONVERSION SECTION

This section consists of an HDAC7545A and two OP17 op amps used for output buffering. Other types of op amps can be used as well. Again, jumper pins allow selection of output configuration: in unipolar output mode, one op amp is used, and in bipolar output mode two op amps are used. Each op amp has a trim potentiometer to null input offset voltage. The HDAC7545A has trim potentiometers to adjust the zero and full scale output.

EB104 PHYSICAL DESCRIPTION

The EB104 PC board is a 5 by 7 inch, Epoxy double-sided, copper-clad printed circuit board. All components and sockets are mounted on the top side, with the exception of the analog input/output BNC connectors which are mounted on the bottom side. Digital and analog ground and all three power supplies are connected through a single 6-pin keyed Molex power connector, for which a mating power supply cable is included with the board. For digital input and output, three 26-pin ribbon connectors are mounted. One is used for data word input, another for data word output, and the last for digital control and status. All IC's are socketed to facilitate re-selection of components, if so desired. Jumper posts on the top side, jumpered by Berg type jumpers, allow the selection of circuit options.

EB104 OPERATION

CAUTIONS

1) When handling the PC board or any of the devices use procedures necessary for protection against electrostatic discharge or device damage may result.

2) No voltages or forced currents should be applied to the EB104 prior to application of power supplies or devices may be damaged. Analog and logic signals should be applied after (or during) power up and removed before (or during) power down.

USING PRE-CONFIGURED SETUP

The EB104 is pre-configured and ready to operate as delivered with no adjustments or modifications needed. Requirements for operation are limited to power supplies, an analog signal source and an oscilloscope. The jumper-programmed function options are pre-set to provide the following conditions:

- a) S/H Amp bypassed
- b) A/D converter in -10 to +10 V bipolar input operation mode.
- c) A/D converter in free-run operation, self-generating convert command
- d) A/D converter in 12-bit conversion, 12-bit output mode.
- e) D/A converter input from A/D converter output.
- f) D/A converter in -10 to +10V bipolar output operation mode

To operate the board using this pre-established configuration, perform the following:

- 1) Connect the power supplies as outlined in the following section. Apply power.
- 3) Apply an analog signal into BNC connector jack J5, ranging between -10 and +10 volts.
- 4) Connect oscilloscope to BNC connector jack J6 to observe the reconstructed analog signal. Signal amplitude will range between -10 to +10 volts.

POWER SUPPLY CONNECTION

Power is supplied through the leaded Molex connector as detailed in Figure 2. Ensure that the beveled edges of the male and female connectors are aligned prior to coupling. Digital and Analog Ground should be connected together at the power supplies to provide maximum noise isolation. The connectors should be coupled and supplies connected prior to turning on the power supplies. With the provided components, the approximate power supply current consumption is:

- + 5 Volt supply: 16 mA
- +15 Volt supply: 16 mA
- 15 Volt supply: 15 mA

Total power dissipation is therefore about 550 mW. When evaluating 574/674 type devices from manufactures other than Honeywell, the +5V supply current will increase to approximately 28 mA, the +15V supply to 22 mA, and the -15 V supply to 45 mA. In this case the total power dissipation will be about 1.15 Watts.

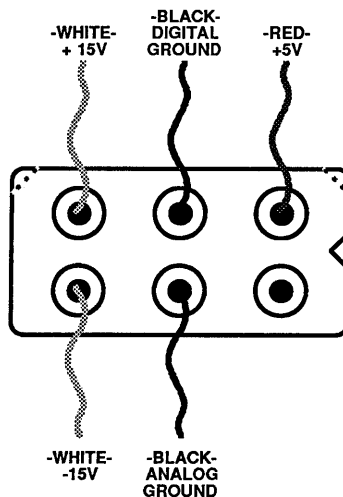


FIGURE 2
POWER SUPPLY CONNECTION

Leaded Power Connector, Top View

ANALOG/DIGITAL CONVERSION SECTION

OPTIONAL SAMPLE/HOLD AMPLIFIER USE

Because of its capacitive DAC architecture, the HADC574/674Z has an inherent sample/hold function. The EB104 is supplied with an on-board sample/hold amplifier which is bypassed in order to demonstrate this function (the Analog Input Jack J5 is tied directly to the HADC574/674Z). The HADC574/674Z's sample/hold function works well with input signal frequencies up to about 5 KHz when using a full scale input. Above this frequency, input slew-rate limiting and aperture uncertainty time may degrade performance.

The discrete sample/hold (S/H) amplifier should be used with the HADC574/674Z when either the input signal frequency is above 5 KHz or when no aperture delay can be tolerated, such as when using the unit for transient sampling. When evaluating 574/674 devices from other manufacturers, the external sample/hold amp will be needed except for very low frequencies. During the conversion cycle, these other 574/674 units perform the successive-

approximation directly on the input signal; therefore, the last bit is calculated just before the end of the 25 μ S (574) or 15 μ S (674) conversion cycle.

Figure 3 shows a simplified wiring diagram of the A/D conversion section. Note that the S/H amp can be inserted in the analog input path or bypassed. Table 1 below describes the jumper post connections for these two conditions.

JUMPER POSTS	S/H AMPLIFIER	
	IN ANALOG PATH	* BYPASSED
E11-E13	OPEN	CLOSED
E12-E14	CLOSED	OPEN
E15-E16	CLOSED	OPEN
E17-E18	OPEN	CLOSED

* EB104 AS DELIVERED

TABLE 1
JUMPER CONFIGURATION
FOR SAMPLE/HOLD UTILIZATION

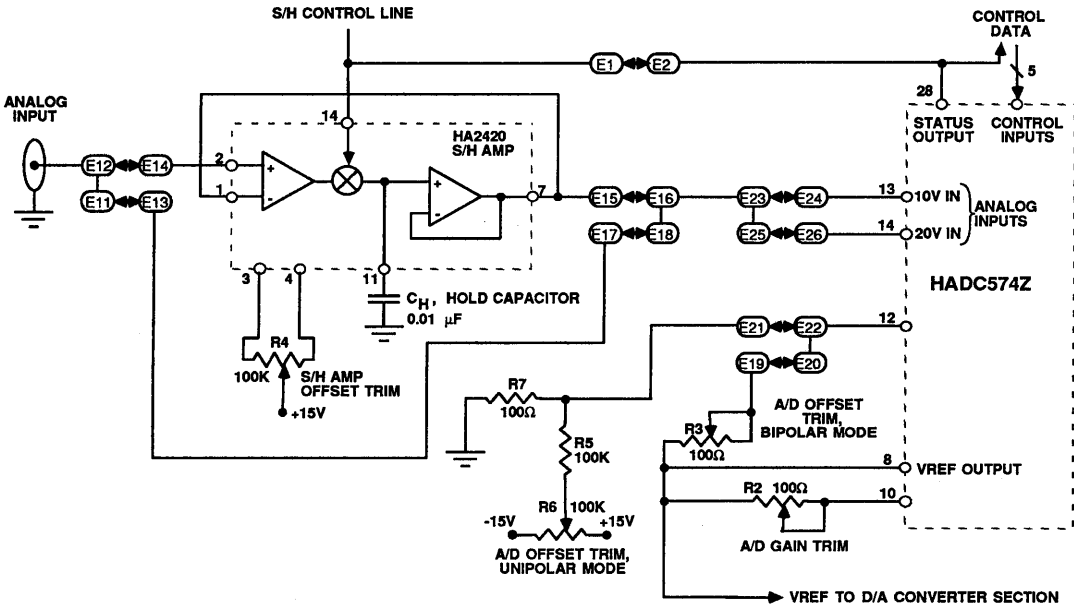


FIGURE 3
SIMPLIFIED WIRING DIAGRAM
OF ANALOG/DIGITAL CONVERSION SECTION
INPUT STRUCTURE

If operation of the EB104 will be with the sample/hold amplifier bypassed, the following section "External Sample/Hold Amplifier Operation" may be skipped.

EXTERNAL SAMPLE/HOLD AMPLIFIER OPERATION

Sample/Hold Amplifier Control

Control of the sample/hold amplifier can be performed by the HADC574/674Z's STATUS output or externally to the EB104. Table 2 describes the jumper configuration for these options. When using the STATUS output, a hold command is generated automatically when a convert command is issued to the HADC574/674Z. At the end of the conversion, STATUS returns to zero and commands the S/H amp to again track the analog input. This timing relationship can be seen in figure 4. As discussed in the next section, it is important that the STATUS output stays low long enough for the sample capacitor to charge when using this configuration.

JUMPER POSTS	S/H AMP CONTROL	
	EXTERNAL CONTROL	HADC574Z STATUS OUTPUT
E1-E2	OPEN	CLOSED

TABLE 2
JUMPER CONFIGURATION
FOR SAMPLE/HOLD CONTROL

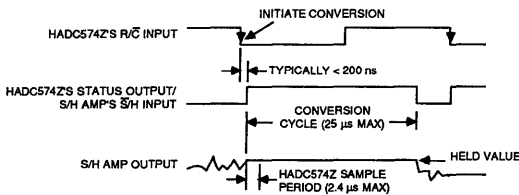


FIGURE 4
TIMING RELATIONSHIP FOR HADC574Z
R/C INPUT, STATUS OUTPUT, AND
SAMPLE/HOLD FUNCTION.

External S/H amp control allows conversion initiation and sample/hold control to be asynchronous. Separate controls are provided at the R/C and S/H pins of Jack J2. Ensure that the Convert command is issued at or after the Hold command.

Hold Capacitor Value Selection

Selection of the hold capacitor value involves trade-offs between hold droop rate and the charge time upon sampling. Larger capacitance values will discharge slower during the hold mode which is useful for long hold times prior to conversion. Smaller capacitance values, however, will better track higher frequency signals during sample mode due to the increased slew rate. Table 3 shows several capacitor values and the approximate associated system performance. The hold capacitor should be of a polystyrene or teflon type to avoid sample hysteresis.

The Manufacturer's Typical Values of Table 3 are taken from the HA2425 data sheet. The Calculated Values assume the following:

Maximum Hold Time:

$$\begin{aligned} \text{Maximum allowable error} &= 1/4 \text{ LSB} \\ &= 1.2 \text{ mV (worst case)} \end{aligned}$$

$$t(\text{max}) = [V_{\text{err}}(\text{max})]/[\text{droop rate}]$$

Maximum Signal Frequency:

$$\begin{aligned} \text{Analog signal is sine wave} \\ \text{Worse-case condition of } 20 V_{\text{p-p}} \text{ input} \\ \text{Maximum frequency limited by slew rate} \\ f(\text{max}) = (\text{slew rate})/2\pi V_{\text{p}} \end{aligned}$$

Another determining factor in sample capacitor size is acquisition time. Acquisition time is the amount of time needed for the S/H amp to again track the signal following a hold mode. Acquisition time becomes a dominant limitation when working with high sample rates. The minimum capacitor value required for the worse-case conditions using the HADC574Z can be calculated as follows:

The maximum guaranteed conversion period of the HADC574Z is 25 μs (40 KHz) and the maximum HADC574Z aperture time is 2.4 μs; therefore, the maximum S/H window = $t(\text{sample period}) - t(\text{aperture time}) = 22.6 \mu\text{s}$. It is assumed that the worst-case input conditions is a 20 KHz square wave at 20 Vpp, which would offer the highest input voltage differential between samples. Therefore, the minimum slew rate requirement would be $20\text{V}/22.6 \mu\text{s}$ or 0.885 V/μs. Reference to the HA2425 data sheet

HA2425 HOLD CAPACITOR VALUE	MANUFACTURE'S TYPICAL VALUES		CALCULATED VALUES	
	DROOP RATE	SLEW RATE (V/ μ s)	(1) MAXIMUM HOLD TIME	(2) MAXIMUM SIGNAL FREQUENCY
10 pF	600 mV/s	15	2 ms	120 KHz
100 pF	50 mV/s	15	24 ms	120 KHz
1000 pF	5 mV/s	10	250 ms	80KHz
(3) 0.01 μ F	500 μ V/s	8	2.5 s	64 KHz
0.1 μ F	60 μ V/s	0.6	20.2 s	4.8 KHz
1 μ F	20 μ V/s	0.05	60 s	400 Hz

NOTES: (1) FOR $< 1/4$ LSB DROOP, $V_{pp} = 20$ V
 (2) WITH ABILITY TO TRACK SIGNAL, $V_{pp} = 20$ V
 (3) VALUE SUPPLIED ON EB104

TABLE 3
SAMPLE CAPACITOR SIZE VS. SYSTEM
PERFORMANCE

would reveal that the largest hold capacitor value usable for these worst-case conditions is 0.05 μ F.

The EB104 comes supplied with a 0.01 μ F capacitor, which will track suitably for the highest sample rate as illustrated above for both the HADC574 and HADC674. At 8 V/ μ s slew rate, a minimum of about 3 μ s sample time is required for full scale acquisition in the 0-20 or ± 10 V range or about 1.5 μ s in the 0-10 or ± 5 V range. As seen in Table 3, droop rate is about 0.5 mV/s; maximum hold time prior to conversion is therefore 2.5 seconds if $1/4$ LSB accuracy is desired.

Calibration of the Sample/Hold Amplifier

Trim potentiometer R4 is used to zero the offset of the sample/hold amplifier. Although the HADC574/674Z also has a zero adjustment (discussed later), it's range is typically not sufficient to compensate for the external sample/hold amplifier's offset. Gain error in the sample/hold amplifier can be compensated by HADC574/674's gain adjustment. Sample/hold offset trim is performed as follows:

- 1) Configure EB104 for S/H amp in analog signal path (Table 1).
- 2) Ground Analog Input (Jack J5) by short circuiting.
- 3) Connect power supplies.
- 4) Connect a \bar{S}/H clock; a TTL compatible, 50% duty-cycle 10 KHz square wave applied to the \bar{S}/H input of Jack J2 is suitable; make sure that jumper connection E1-E2 is open.

5) Using an oscilloscope, measure the voltage between jumper post E15 and analog ground (J5 shield).

6) Adjust trim potentiometer R4 for 0 volts during Hold cycle, which occurs while the \bar{S}/H input is logic high.

Repeat of the above calibration procedure is needed only if the S/H amp chip or the hold capacitor is replaced; otherwise, all future "zero" calibration can be performed using the HADC574/674Z calibration procedure discussed below.

HADC574/674Z OPERATION

Input Range Selection

Jumper posts on the EB104 allow configuring the HADC574/674Z for input ranges of 0-10, 0-20, ± 5 , or ± 10 volts. The 0-10 and 0-20 volt ranges use what is called unipolar input operation and the ± 5 and ± 10 volt range use bipolar input operation. Feedback path of the VREF varies between unipolar and bipolar connections, while one of two input pins, 10V IN or 20V IN, are chosen for ranging. Jumper post programming for the various range options is summarized in Table 4.

JUMPER POSTS	HADC574/674Z INPUT RANGE			
	UNIPOLAR		BIPOLAR	
	0-10 V	0-20 V	± 5 V	* ± 10 V
E19-E20	OPEN	OPEN	CLOSED	CLOSED
E21-E22	CLOSED	CLOSED	OPEN	OPEN
E23-E24	CLOSED	OPEN	CLOSED	OPEN
E25-E26	OPEN	CLOSED	OPEN	CLOSED

* EB104 RANGE AS DELIVERED

TABLE 4
EB104 ANALOG INPUT RANGE OPTIONS
AND JUMPER POST PROGRAMMING

Control Logic Inputs

The EB104 jumper posts are pre-configured to provide 12-bit operation with what is probably the simplest control scheme. Pin R/ \bar{C} of Jack J2, which is connected to the R/ \bar{C} input of the HADC574/674Z, is used to both initiate the 12-bit conversion cycle and enable the 12 bit output. For the free-running

CE	\overline{CS}	R/ \overline{C}	$12/\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeros

**TABLE 5
TRUTH TABLE FOR THE HADC574/674Z
CONTROL LOGIC INPUTS**

operation, as configured, the STATUS output pin of Jack J2 triggers the R/ \overline{C} pin. This is discussed further in the next section.

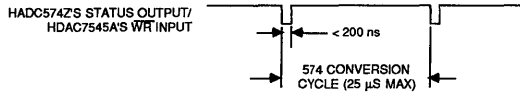
The remaining control pins are tied as follows:

CE = $12/\overline{8}$ = +5V (Logic High)
 \overline{CS} = Ao = Ground (Logic Low)

These above connections result in the chip always being enabled in 12-bit conversion mode with all 12 output bits enabled. The truth logic of Table 5 summarizes the control logic functions. Refer to the HADC574Z data sheet for further information regarding these functions.

Free-Running Operation

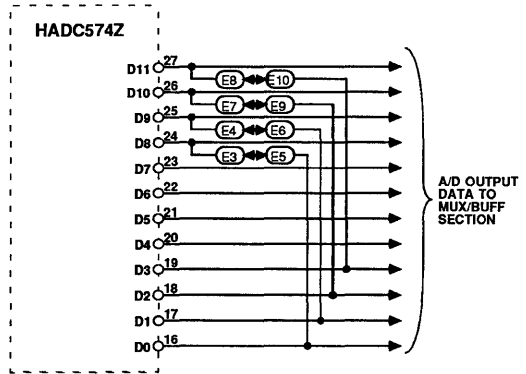
By connecting the STATUS output of Jack J2 to the R/ \overline{C} input of Jack J2, the HADC574/674Z self triggers. That is, at the end of a conversion, when STATUS goes to logic low, this automatically triggers the device for another conversion. Figure 5 shows the resultant wave form of the STATUS line when using the HADC574Z. The HADC674Z gives similar results except that conversion time is 15 μ S maximum. Note that the <200 nS STATUS logic low time is not sufficiently long enough for an external sample/hold amp control. The EB104 is pre-configured for free-running operation.



**FIGURE 5
STATUS OUTPUT TIMING OF HADC574Z IN
FREE-RUNNING MODE**

Data Output Options

The HADC574/674Z is capable of outputting a 12-bit conversion result in two 8-bit words (with 4 trailing zeros). To accomplish this, the four MSB output lines are tied to the four LSB output lines as shown in Figure 6. The EB104 has jumper posts to facilitate these connections easily. These connections are summarized in Table 6. Following a conversion, the MSB and LSB words are selected by input pin Ao as indicated in Table 5. For full information on this mode of operation, please refer to the HADC574/674Z data sheet.



**FIGURE 6
WIRING DIAGRAM OF D/A SECTION
OUTPUT**

JUMPER POSTS	OUTPUT FORMAT	
	* 12 BITS	8-BITS
E19-E20	OPEN	CLOSED
E21-E22	OPEN	CLOSED
E23-E24	OPEN	CLOSED
E25-E26	OPEN	CLOSED

* EB104 AS DELIVERED

**TABLE 6
JUMPER POSTS SELECTION
FOR OUTPUT MODE PROGRAMMING**

Calibration

The HADC574/674Z is manufactured to have only a few LSB's of zero offset and a fraction of a percentage of full scale error, depending on grade. In addition, inaccuracies in the S/H amp, if used, will contribute to the inaccuracy of the A/D Conversion Section. The EB104 includes trim potentiometers for zero and full scale adjustment to compensate for these errors which are pre-adjusted for the pre-configured operation. Shipping may effect the adjustments and alter the calibration. Re-calibration will be needed when the input range is changed, when the S/H amp utilization is changed, or when any components are replaced in this section.

Calibration involves the adjustment of the devices offset and gain. Adjustment is made so that the output of "zero" (0000 0000 0000) and "full scale" (1111 1111 1111) code values are received when the analog input's negative-most and positive-most values are input. In practice, accurate calibration is achieved by calibrating the "zero" point with an analog input voltage the equivalent of 1/2 LSB above the desired zero setting; the zero trimming is then set between the 0000 0000 0000 and 0000 0000 0001 output transition. Full scale calibration is then achieved similarly with an analog input 1/2 LSB below the maximum range; the gain trimming is then set between the 1111 1111 1111 and 1111 1111 1110 output transitions.

To calibrate the A/D section of the EB104 using the approach described above, use the following procedure:

- 1) Select S/H amp utilization and input range mode.
- 2) Apply power supplies.
- 3) If using S/H amp, adjust zero offset trim of S/H amp if not already done.
- 4) Apply an accurate programmable voltage source to EB104 Analog Input (Jack J5).

(A suitable method to accomplish this is with a variable power supply in parallel with a digital voltmeter. Voltage setting should be accurate to within 0.5 mV, which is about 1/4 LSB in the 0-10 or ± 5 volt range. A potentiometer may be required to divide and trim the input reference voltage. Noise should also be kept low, less than 1 mV if possible. Accuracy of voltage source and level of noise will affect achievable calibration.)

INPUT RANGE SELECTED	"ZERO" CALIBRATION VOLTAGE	"ZERO" TRIM POTENTIOMETER	"FULL SCALE" CALIBRATION VOLTAGE
* 0-10 V	1.22 mV	R6	9.9963 V
0-20 V	2.44 mV	R6	19.9927 V
± 5 V	-4.9988 V	R3	4.9963 V
± 10 V	-9.9976 V	R3	9.9927 V

* EB104 RANGE AS DELIVERED

TABLE 7
HADC574Z CALIBRATION VOLTAGES

- 5) Connect logic monitor to A/D data output jack J3. (This can be accomplished with a logic analyzer connected to Jack J3 or by determining the logic value of each pin with a voltmeter or oscilloscope.)
- 6) Set voltage source to zero calibration value indicated by Table 7.
- 7) Adjust zero trim potentiometer indicated by Table 7. Set to point where flickering occurs between 0000 0000 0000 and 0000 0000 0001; both codes should occur equally. (If using a scope or volt meter, monitor pin B0 of Jack J3, the LSB; ensure pin B2-B11 are still zero and not flickering.)
- 8) Set voltage source to full scale calibration value indicated by Table 7.
- 9) Adjust gain trim potentiometer R2. Set to point where flickering occurs between 1111 1111 1111 and 1111 1111 1110; again equal occurrences of code should exist.

The A/D section is now calibrated and ready for use.

Component Selection

The EB104 can be used for the evaluation and comparison of similar component types. In addition to the hold capacitor discussed earlier, both the external S/H amp and HADC574/674Z can be replaced with other devices. The HA2425 supplied on the board can be replaced with an HA2420, AD583, SMP-81, or SHM-IC-1. The HADC574/674Z can also be replaced with alternate pin compatible devices for evaluation and comparison purposes. Although pin 11 of the HADC574/674Z is not internally connected, -15 volts is supplied to the socket pad for the VEE requirement of alternate, pin compatible devices from other manufacturers.

MULTIPLIER/BUFFER SECTION

This section drives both the Digital/Analog Conversion Section and Data Output Jack J4. Input into this section is selectable from either the Analog/Digital Conversion Section or Data Input Jack J3. This allows the Analog/Digital and Digital/Analog Conversion Sections to be linked and operated together or operated separately. Digital code can be output from the HADC574/674Z through Jack J4, or data can be input directly to the HDAC7545A. All data input or output from this section is buffered. A block diagram of the Multiplier/Buffer Section is shown in Figure 7.

OPERATION

With a logic low into the SELECT input of Control Line Jack J2, the HADC574/674Z output data is selected; a logic high selects the data input into Jack J3. The STROBE input allows input data to be transferred with a logic low condition, and blocks data transfer with a logic high condition. This is shown in Table 8, Multiplexer/Buffer Section Logic Control. A Berg jumper can be used at Jack J2 to tie either the SELECT or STROBE input low (ground).

The Multiplexer/Buffer Section consists of three 74LS157 devices each of which is a quadruple 2-line-

INPUTS		OUTPUT (12 BITS)
SELECT	STROBE	
H	X	ALL OUTPUTS LOGIC LOW DATA INPUT JACK J2 SELECTED *A/D CONVERTER OUTPUT SELECTED
L	H	
L	L	

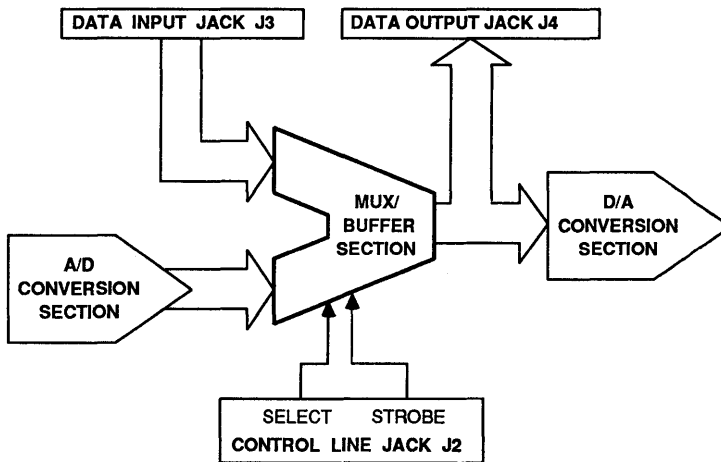
*JUMPED CONDITION AS DELIVERED

**TABLE 8
MULTIPLEXER/BUFFER SECTION LOGIC
CONTROL**

to-1-line data selector/multiplexer. The Strobe inputs and Select inputs of the three devices are tied together and controlled by the STROBE and SELECT input pins of Jack J2. Device compensation is achieved with a Q-Pak™ chip capacitor under each device. Pinout of the 74LS157 and its logic truth table is shown in the appendix.

Device Selection

The CMOS equivalent of the 74LS157 can be used in place of the bipolar devices. This will provide the advantage of reduced power supply current, but output drive will be reduced.



**FIGURE 7
MULTIPLEXER/BUFFER SECTION BLOCK DIAGRAM**

DIGITAL/ANALOG CONVERSION SECTION

The heart of this section is the HDAC7545A current output digital-to-analog converter. Parallel code received from the Buffer-Multiplexer section is input into its internal input register and can be latched. The HDAC7545A outputs a signal current corresponding to the 12-bit code residing in the input register. The analog current output of the DAC is converted to a voltage by the external op amp(s) in combination with internal resistor Rfeedback.

DATA INPUT AND LOGIC CONTROL

Input logic pins \overline{CS} and \overline{WR} control HDAC7545A operation and are available on the EB104 at the Control Line Jack J4. Pins \overline{CS} and \overline{WR} control the loading of the input register; when both pins are low, data at the input logic pins DB0-DB11 is transferred into the input register. When \overline{CS} and/or \overline{WR} goes high, the input register is locked and retains the last code condition. \overline{CS} and \overline{WR} can be tied low (grounded with Berg jumpers at J4) so that all input codes are immediately converted; this is not a good approach if a smooth continuous output is desired. Commonly, and by pin definition, pin \overline{CS} is used for chip selection and \overline{WR} for writing data into the input register.

The simplest method for loading the HDAC7545A on the EB104 is to ground \overline{CS} with a Berg jumper. Loading the input register is accomplished with a negative pulse on \overline{WR} (100 nS minimum).

In the pre-configured hook up of the EB104, pin \overline{CS} is jumpered to ground and pin \overline{WR} is connected to the STATUS output of the HDAC574Z which is in free-run operation. As shown in Figure 9, the typical timing of the HDAC574Z and HDAC7545A allows this configuration to function. Output data from the HDAC574Z is transferred to the HDAC7545A via the Multiplexer/Buffer section.

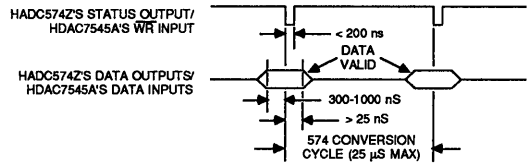


FIGURE 9
TIMING RELATIONSHIP BETWEEN
HDAC574Z AND HDAC7545A
IN PRE-CONFIGURED OPERATION

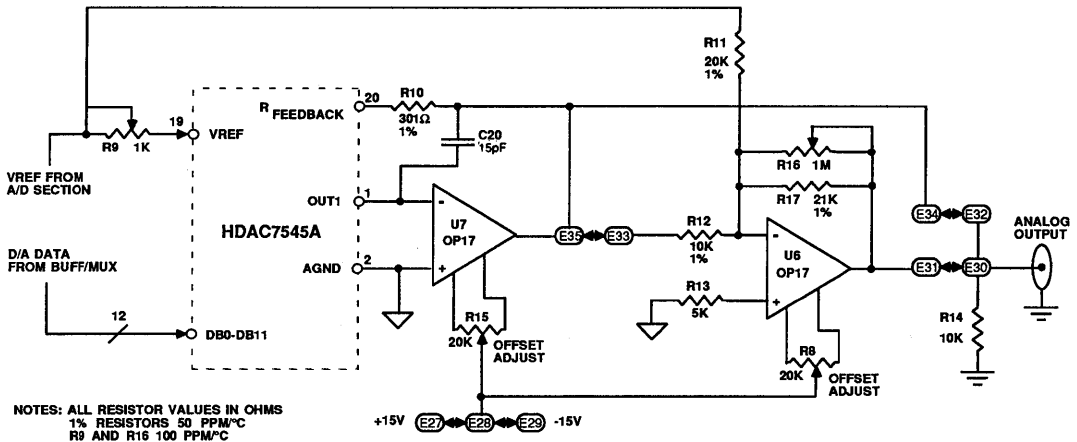


FIGURE 8
SIMPLIFIED WIRING DIAGRAM
OF DIGITAL/ANALOG CONVERSION SECTION

OUTPUT MODE SELECTION

Berg jumpers allow the selection of either a unipolar or bipolar voltage output from the Digital/Analog Conversion Section. In unipolar operation, a single op amp (U7) is used in an inverted unity gain configuration to provide an inverted 0 to -10 volt output, corresponding to full scale input codes 0000 0000 0000 to 1111 1111 1111, respectively. In bipolar operation, both op amps (U6 and U7) are used to provide a non-inverted -10 to 10 volt output, corresponding to codes 0000 0000 0000 to 1111 1111 1111; 0 volts results from code 1000 0000 0000. The jumper configuration for output mode selection is summarized in Table 9.

JUMPER POSTS	D/A SECTION OUTPUT RANGE	
	-10 TO 0 V (UNIPOLAR)	-10 TO +10 V *(BIPOLAR)
E30-E31 E32-E34 E33-E35	OPEN CLOSED OPEN	CLOSED OPEN CLOSED

* EB104 RANGE AS DELIVERED

TABLE 9
EB104 ANALOG OUTPUT RANGE OPTIONS
AND JUMPER POST PROGRAMMING

CALIBRATION

The EB104 is delivered pre-calibrated and ready to operate. However, due to vibration during shipment, recalibration may be necessary in order to obtain the 1/2 LSB accuracy achievable with the HDAC7545A. Calibration will again be necessary following any component replacement in the Digital/Analog Conversion Section with few exceptions, and also when changing between unipolar and bipolar modes.

As discussed later in the Trim and Gain Component section, the gain determining resistors used for bipolar operation are of a readily-available 1% accuracy variety. This can represent a 2% gain inaccuracy or an 80 LSB error (out of 4096 LSB's total). Therefore, when adjusting the trimming for a fraction of an LSB, the adjustment is "touchy" and can drift an entire LSB over an ambient temperature change of several degrees Celsius. Refer to the Component Selection section if additional temperature stability is desired.

Calibration Procedure

During calibration, all voltage measurements are taken from the Analog Output Jack J6. For a more accurate calibration, output noise is reduced by disabling the HAD574/674Z and forcing the input conditions through Data Input Jack J3; On Jack J2, jumper pins CE and SELECT to ground which will disable the HADC574/674Z and select input data from Jack J3. Also jumper pins WR and CS on Jack J2 to ground which will result in continuous conversion.

Unipolar Output Mode Calibration

- 1) Ensure EB104 is configured for Unipolar Output Mode.
- 2) Input 0000 0000 0000 into Jack J3.
- 3) Adjust offset trim potentiometer R15 until 0 Volts is obtained. (2.44 mV represents 1 LSB error)
- 4) Input 1111 1111 1111 into Jack J3.
- 5) Adjust Vref gain adjustment R9 until -10 Volts is obtained.

This completes the calibration for unipolar output operation.

Bipolar Output Mode Calibration

- 1) Perform steps 1 through 3 of Unipolar Output Mode Calibration
- 2) Disconnect Jumpers E33-E35 and E34-E35; Connect E30-E31.
- 3) Short pins 2 and 3 of U6 to ground.
- 4) Adjust offset trim potentiometer R8 until 0 volts is obtained; due to the high gain of the amplifier, it will be nearly impossible to actually obtain 0 volts; adjusting R8 so that the output polarity just changes is sufficient.
- 5) Connect Jumper E33-E35.
- 6) Input 0000 0000 0000 into Jack J3.
- 7) Adjust gain trim potentiometer R16 until -10 Volts is obtained. (4.88 mV represents 1 LSB error)
- 8) Input 1111 1111 1111 into Jack J3.
- 9) Adjust Vref trim potentiometer R9 until +10 Volts is obtained.
- 10) Repeat steps 6 though 9 and readjust if necessary.

This completes the calibration for bipolar output operation.

D/A SECTION COMPONENT SELECTION

Output and Trim Resistors

In conjunction with external op amp U7, the resistance of Rfeedback in series with R10 is used to convert the DAC output current to a voltage. Additionally, in bipolar output mode a summation circuit composed of op amp U6 and external resistors is used to combine Vref with the generated output voltage. Trim resistors are included to adjust for offset and full scale errors in the HDAC7545A, the Vref error, and in bipolar output mode, the resistor ratio error of the gain stage incorporating op amp U6. The component selection for unipolar output mode will be discussed first.

The worst-case gain error tolerance of the lowest-grade HDAC7545A is ± 4 LSB or approximately $\pm 0.1\%$. The maximum error of the Vref, derived from the HADC574, is approximately $\pm 0.1\%$. Therefore, when using unipolar output mode, the gain adjustment will need to be $\pm 0.2\%$ to cover worst case error. In the HDAC7545A, the resistance of Rfeedback and the resistance into VREF is typically 12.5 K Ω but can be as high as 18 K Ω . For trim purposes, R10 adds to Rfeedback and R9 (potentiometer) adds to the input resistance of Vref. Working out the gain equation using 18 K Ω as internal resistance (worse case) it is found that R10 needs to be 36 Ω minimum and R9 twice the R10 value (minimum) to provide the needed $\pm 0.2\%$ adjustment.

The best control of adjustment and stability for unipolar output operation is achieved by using the resistance values derived above. Even lower values can be used if a better grade HDAC7545A is used and/or VREF voltage is better controlled. Actual values used on the EB104 are larger: R10 is 301 Ω and R9 is 0 to 1000 Ω . These increased values are necessary to allow calibration in bipolar mode as discussed below.

In bipolar mode, the gain stage consisting of op amp U6 is configured to gain and sum Vref and the unipolar output of the DAC; $(-1) \cdot (Vref) + (-2) \cdot (\text{Unipolar Out})$. (Recall that the unipolar output is inverted.) When 0000 0000 0000 is input, the unipolar output is zero and contributes nothing; the output is therefore $(-10V) + (-2) \cdot (0) = -10$ Volts. When 1111 1111 1111 is input, the output is $(-10V) + (-2) \cdot (-10V) = +10$ Volts. The accuracy of the (-1) and (-2) gains directly affect final accuracy. In addition to the errors discussed in

unipolar output operation, bipolar output operation gain error also needs to be considered.

Because of relative ease of availability and to therefore demonstrate a practical circuit, the EB104 is supplied with fixed gain resistors of 1 % accuracy. Therefore, $\pm 2\%$ worst case gain inaccuracies can be expected. The gain adjustment of the $(-2) \cdot (Vref)$ product is first considered. To allow calibration over the maximum $\pm 2\%$ error range, R16 (feedback resistance) consists of a 21 K Ω (1%) resistor in parallel with a 1 M Ω potentiometer; R11 (input resistance) consists of a 20 K Ω (1%) resistor. Working out the gain equations with nominal resistance values, this allows a gain adjustment from $-\infty$ to $+2.8\%$ over unity. Considering worst-case resistor values, this leaves 0.8% for compensation of Vref error.

The gain of the $(-1) \cdot (\text{Unipolar Out})$ product is next considered. This product, again due to the summing amp resistor tolerances, can also vary $\pm 2\%$; this is due to the 1% tolerance of R12 combined with the trimmed R16. The Error is compensated by the same adjustment made in unipolar operation; by adjustment of R9 to change the HDAC7545A output gain. However, the 0.2% adjustment allowed earlier needs to be increased to $\pm 2\%$ to compensate for summing amp gain error. By working out the gain equations, it is found that increasing R9 to 360 ohms and R9 to about 720 provides the desired range. Practically, however, due to typical values of HDAC7545A Vref and Rfeedback resistance and available resistance values, component values of 301 Ω and 1 K Ω were chosen for R10 and R9, respectively.

Temperature coefficient of the chosen gain determining resistors is 50 ppm and 100 ppm for the fixed resistors and potentiometers, respectively. These, again are readily available values. If the components did drift in opposite directions, calculation shows that 1 LSB error would be imposed with less than 3°C change; practically, however, similar components typically track each other and insignificant change will be noted in the laboratory environment.

Further stability of the Digital/Analog section can be attained by using fixed resistors with lower accuracy tolerance and lower temperature coefficient. The better accuracy will reduce the adjustability needed for the HDAC7545A adjustment; this will then reduce the inaccuracies contributed by the external resistance due to internal/external resistor temperature differences and temperature coefficient differences.

Other 7545-Type Devices

Any competing 7545A device may be inserted in place of the HDAC7545A for evaluation. Note, however, that output compensation capacitor C20 will need be increased to the value specified by the manufacturer. Having a very uniquely low output capacitance, the HDAC7545A requires only 15 pF compensation and has a very fast settling time.

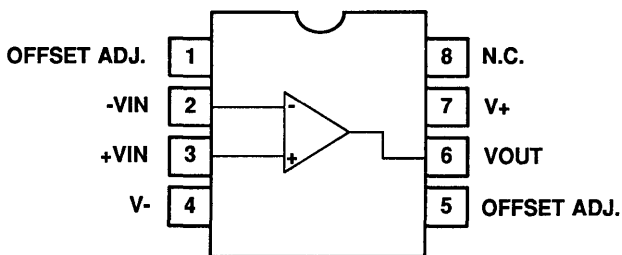
Op Amps

The high slew rate OP-17 was chosen for the EB104 to demonstrate the fast settling time of the HDAC7545A. Many other popular op amp types, having the same pin out, can be used instead. Some of these op amps require the opposite voltage polarity on the offset trim potentiometer wiper. The EB104 has Berg jumper posts that allow this polarity change. Please refer to Table 10 for the jumper position for several popular op amps.

JUMPER POSTS	OFFSET TRIM POT VOLTAGE	USED FOR OP AMPS:
E28-E29	-15 V	AD544
E27-E28	+15 V	LF155/6/7 OP07 *OP17

*SUPPLIED ON EB104

**TABLE 10
JUMPER POST CONFIGURATION
FOR POPULAR OP AMPS**



**FIGURE 10
OP AMP PIN OUT
TOP VIEW**

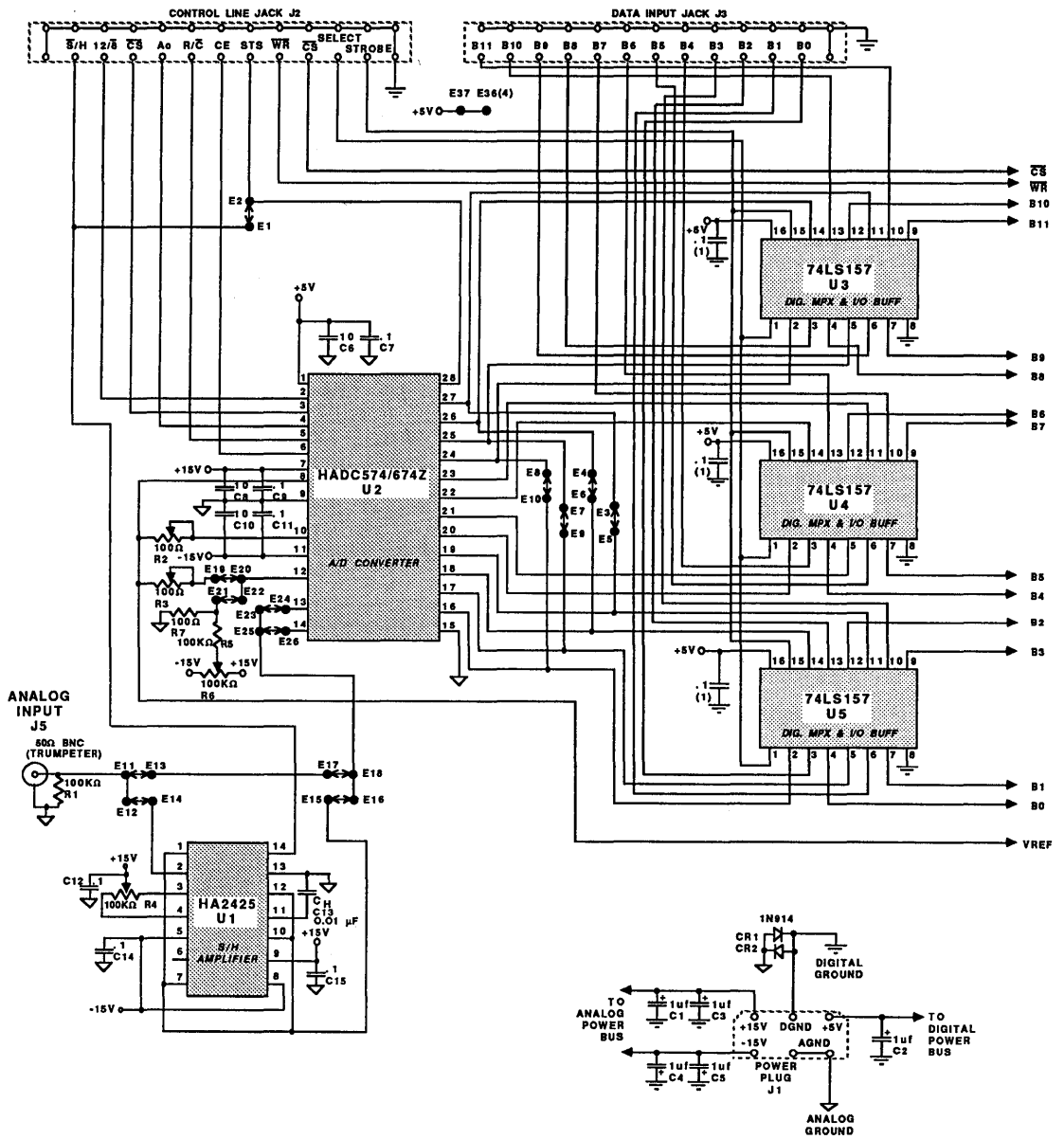
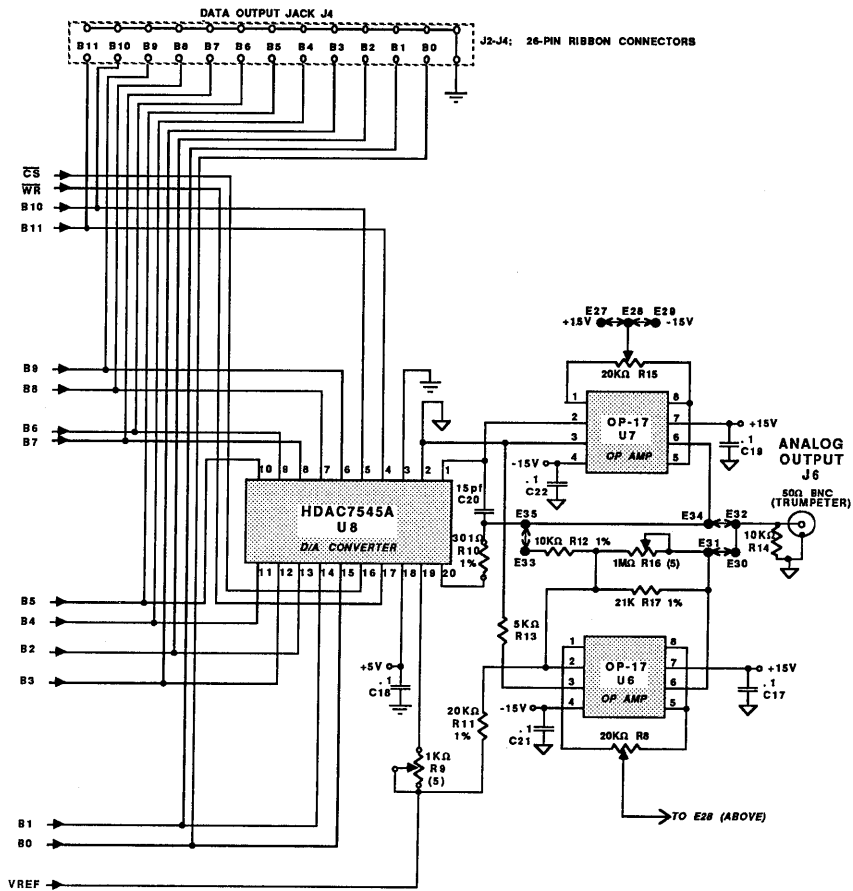


FIGURE 11 EB104 WIRING



NOTES:

- (1) U3-U5 DECOUPLING CAPACITORS MOUNTED BENEATH IC (Q-PAK™).
- (2) PINOUTS OF JACKS AND IC'S (U1-U6, U7-U8) SHOWN FROM TOP VIEW.
- (3) ALL CAPACITANCES IN μF UNLESS OTHERWISE INDICATED.
- (4) E36 AND E37 USED AS LOGIC HIGH JUMPER POSTS FOR JACK J2.
- (5) R8 AND R16 TEMP CO 100 PPM; R10, R11, R12 AND R17 TEMP CO 50 PPM.

DIAGRAM

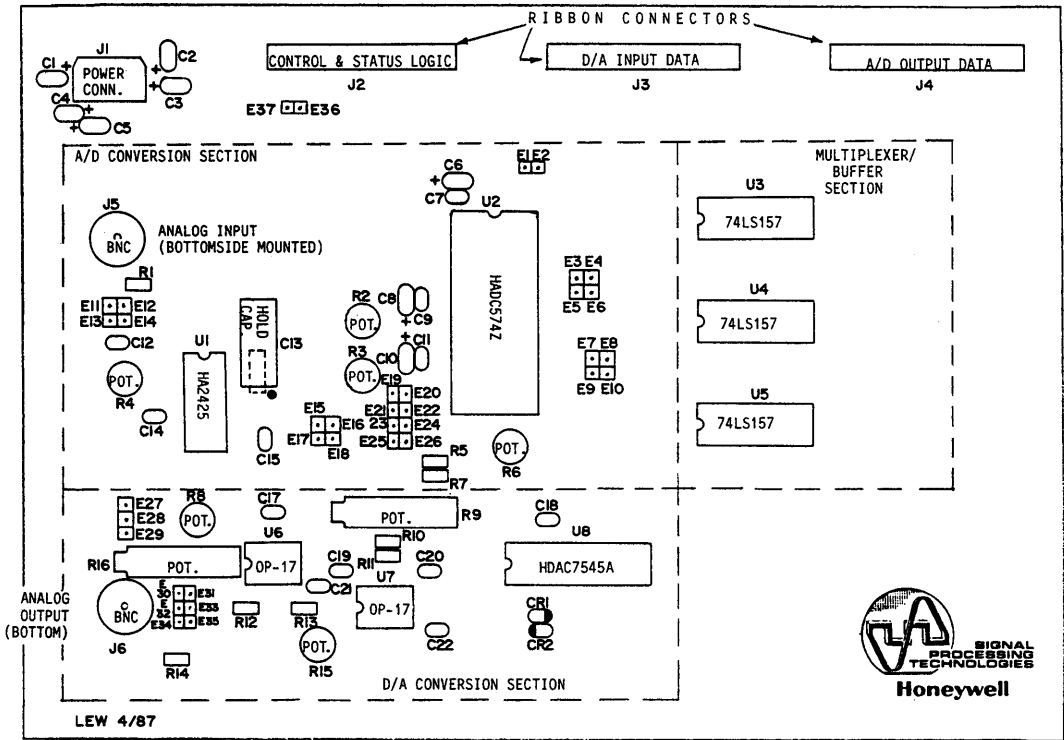
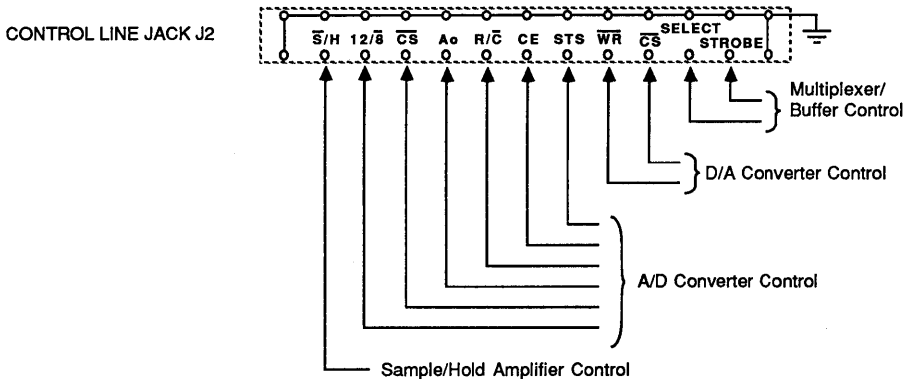


FIGURE 12
EB104 BOARD LAYOUT

Top View, Actual Size



$\overline{S/H}$ Input: "0" Allows S/H amp to track analog input; "1" holds value

$12/\overline{8}$ Input: "0" for 8-bit output format; "1" for 12-bit output format

\overline{CS} (Chip Select Bar) Input: "0" enables chip operation; "1" prevents conversion

A_o Input: "0" selects 12-bit data conversion; "1" selects 8-bit data conversion

R/\overline{C} (Read/Convert Bar) Input: "0" initiates conversion cycle;

"1" Enables data output

CE (Chip Enable) Input: "0" prevents A/D operation; "1" enables operation

STS (Status) Output: A/D status output; outputs "1" while converting

\overline{WR} (Write Bar) Input: "0" loads DAC input register; "1" locks register data

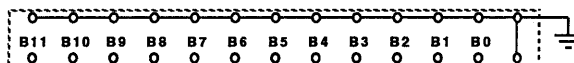
\overline{CS} (Chip Select Bar) Input: "0" enables input register; "1" disables

STROBE Input: "0" enables data transfer; "1" results in all J4 outputs as "0"

SELECT Input: "0" selects A/D output data; "1" selects J3 input data

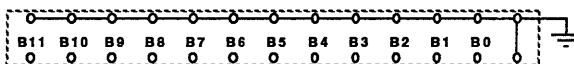
(Note "0" indicates a logic low condition, "1" indicates a logic high condition)

DATA INPUT JACK J3



Alternate input data source for D/A Conversion.
B0 is LSB, B11 is MSB

DATA OUTPUT JACK J4



Buffered output data from A/D Converter.
B0 is LSB, B11 is MSB

FIGURE 13
RIBBON CABLE CONNECTORS
PIN FUNCTION SUMMARY

Sample/Hold Utilization Options

S/H Amp in Analog Path: E12-E14, E15-E16
 S/H Amp Bypassed: E11-E13, E17-E18

Sample/Hold Control Options

S/H Amp Controlled by J2 Pin: (E36, E37 Open)
 S/H Amp Controlled by HADC574Z Status Output:
 E1-E2

HADC574Z Input Range Options

10 Volt Input Range: E23-E24
 20 Volt Input Range: E25-E26

HADC574Z Unipolar/Bipolar Input Options

Unipolar Input Conditions: E21-E22
 Bipolar Input Conditions: E19-E20

HADC574Z Output Format Options

12-Bit Output: (E3 Through E10 Left Open)
 8-Bit Output: E3-E5, E4-E6, E7-E9, E8-E10

HDAC7545A Output Format Options

Unipolar Output: E32-E34
 Bipolar Output: E30-E31, E33-E35

A/D Conversion Section

R4: S/H Amp Offset Adjustment

R2: Gain Adjustment Of A/D Conversion, Unipolar and Bipolar Modes (Same as R2 in HADC574Z data sheet, figures 11 and 12)

R3: Offset (Zero) Adjustment of A/D Conversion, Unipolar Mode Only (Same as R1 in HADC574Z data sheet, figure 11)

R6: Offset (Zero) Adjustment of A/D Conversion, Bipolar Mode Only (Same as R1 in HADC574Z data sheet, figure 12)

D/A Conversion Section

R8: Offset (Zero) Adjustment of Op Amp U6

R15: Offset (Zero) Adjustment of Op Amp U7

R16: Full Scale Output Trim for use in Bipolar Mode

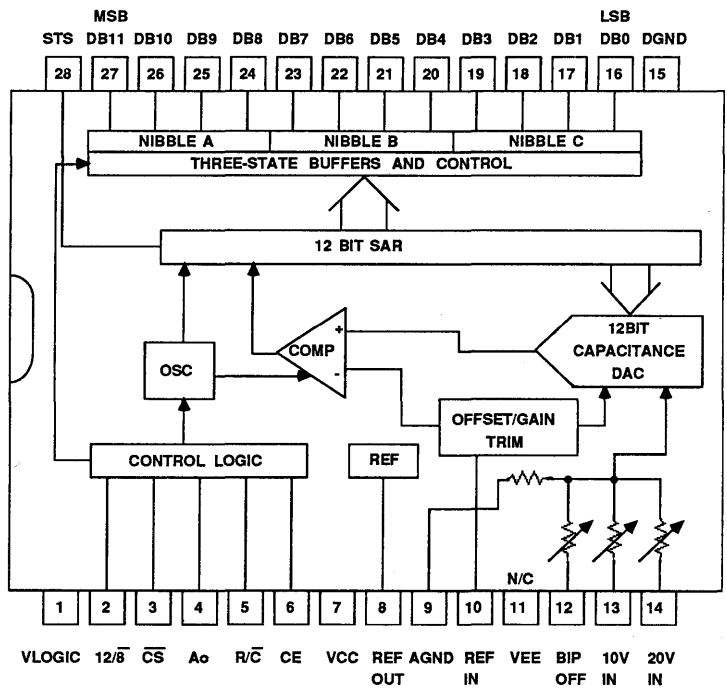
R9: (Optional Resistor, Board Delivered With Pins Jumpered) VREF Trim for D/A Conversion Adjustment; Used to Trim Full Scale Output in Unipolar Mode, or Zero Output in Bipolar Mode.

**TABLE 11
 JUMPER CONFIGURATION SUMMARY**

Operation of the EB104 is tailored by positioning the Berg-type connectors between the appropriate pin pairs. This table shows a summary of the possible options and the corresponding jumper connections. In each case, it is imperative that one option is selected, but one only. For the jumper post locations refer to Figure 12 or the PC board.

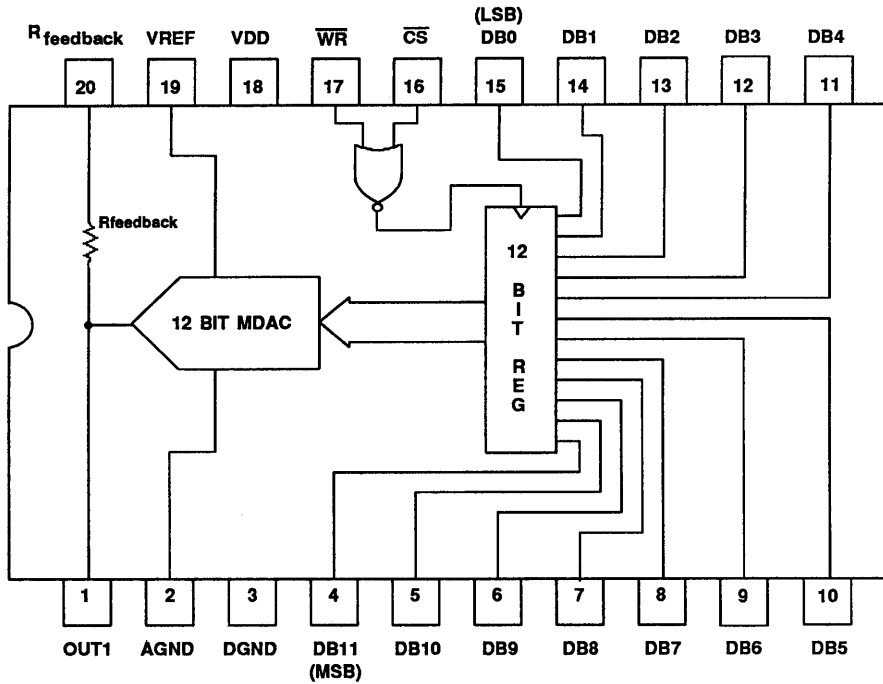
**TABLE 12
 TRIM POTENTIOMETER SUMMARY**

Multi-turn potentiometers are supplied on the EB104 to allow fine adjustment of various analog conditions. Although the EB104 is calibrated during manufacture to allow functionality, some adjustment may be necessary to obtain desired results.



PIN	PIN NAME	FUNCTION
1	V _{Logic}	LOGIC SUPPLY VOLTAGE, +5V
2	12/8	DATA MODE SELECT INPUT
3	CS	CHIP SELECT INPUT
4	A ₀	BYTE ADDRESS/SHORT CYCLE INPUT
5	R/C	READ/CONVERT INPUT
6	CE	CHIP ENABLE INPUT
7	VCC	ANALOG POSITIVE SUPPLY, +15
8	REF OUT	REFERENCE OUTPUT, +10V
9	AGND	ANALOG GROUND
10	REF IN	REFERENCE INPUT
11	N.C.	NO CONNECTION
12	BIP OFF	BIPOLAR OFFSET
13	10V IN	10 VOLT ANALOG INPUT
14	20V IN	20V ANALOG INPUT
15	DGND	DIGITAL GROUND
16-27	DB0-DB11	DIGIAL DATA OUTPUT
28	STS	STATUS OUTPUT

FIGURE 14
HADC574Z PIN ASSIGNMENT



PIN	PIN NAME	FUNCTION
1	OUT1	ANALOG CURRENT OUTPUT
2	AGND	ANALOG GROUND
3	DGND	DIGITAL LOGIC GROUND
4-15	DB0-DB11	OUTPUT DATA BITS
16	CS	CHIP SELECT
17	WR	DATA WRITE
18	VDD	POSITIVE POWER SUPPLY
19	VREF	REFERENCE INPUT VOLTAGE
20	R _{feedback}	INTERNAL FEEDBACK RESISTOR

FIGURE 15
HDAC7545A PIN ASSIGNMENT

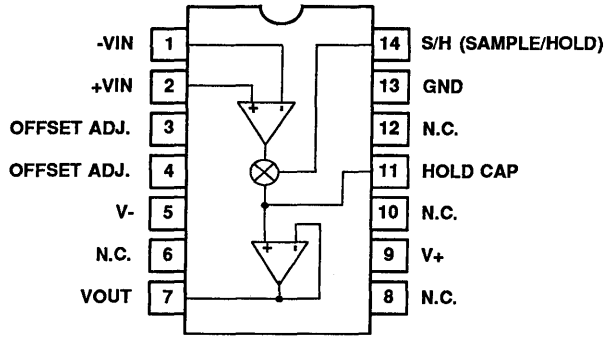
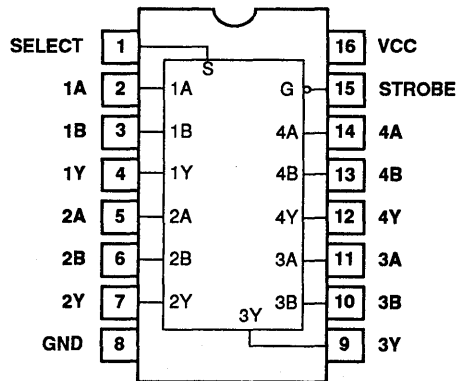


FIGURE 16
HA2425 SAMPLE/HOLD AMP PIN OUT
TOP VIEW



INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

FIGURE 17
74LS157 2-TO-1 MULTIPLEXER/SELECTOR PIN OUT
AND LOGIC TRUTH TABLE
PIN OUT FROM TOP VIEW

NO.	REF. DESIG.	QTY	DESCRIPTION	MANUFACTURER / PART NO.
1	C1-C5	5	Capacitor, 1 μ F Tantalum	
2	C6, C8, C10	3	Capacitor, 10 μ F Tantalum	
3	C7, C9, C11, C12, C14, C15, C17, C18, C19, C21, C22	11	Capacitor, 0.1 μ F	
4	C13	1	Capacitor, 0.01 μ F Polystyrene	
5	C20	1	Capacitor, 15 pF	
6	See Note (1)	3	Capacitor, 0.01 μ F Q-Pak™	Rogers Corporation
7	CR1, CR2	2	Diode, 1N914	
8	E1-E37	37	Jumper Pins	
9	J1	1	Connector, Power	Molex / 09-180-5061
10	J2, J3, J4	3	Connector, 26-Pin Ribbon Cable	TRW / 3593-5002
11	J5, J6, J7	3	Connector, BNC	Trumpeter / CBJ20
12	R1, R5	2	Resistor, 100 K Ω , 1/8 Watt, 5 %	
13	R7	1	Resistor, 100 Ω , 1/8 Watt, 5 %	
14	R10	1	Resistor, 301 Ω , 1/8 Watt, 1 %	Dale / RN55C
15	R11	1	Resistor, 20 K Ω , 1/8 Watt, 1 %	Dale / RN55C
16	R12	1	Resistor, 10 K Ω , 1/8 Watt, 1 %	Dale / RN55C
17	R13	1	Resistor, 4.99 K Ω , 1/8 Watt, 1 %	
18	R14	1	Resistor, 10 K Ω , 1/8 Watt, 5 %	
19	R17	1	Resistor, 21 K Ω , 1/8 Watt, 1 %	Dale / RN55D
20	R2, R3	2	Potentiometer, 100 Ω Multiturn	Bourns / 3339P-101
21	R4, R6	2	Potentiometer, 100 K Ω Multiturn	Bourns / 3339P-104
22	R8, R15	2	Potentiometer, 20 K Ω Multiturn	Bourns / 3339P-203
23	R9	1	Potentiometer, 1 K Ω Multiturn	Bourns / 3006P-102
24	R16	1	Potentiometer, 1 M Ω Multiturn	Bourns / 3006P-105
25	U1	1	I.C., HA2425, Sample/Hold Amp	Harris
26	U2	1	I.C., HADC574BCJ, A/D Converter	Honeywell
27	U3, U4, U5	3	I.C., 74LS157, TTL Quad Multiplexer	
28	U6, U7	2	I.C., OP-17, Operational Amplifier	PMI
29	U8	1	I.C., HDAC7545AACD, D/A Converter	Honeywell

(1) Note: Q-pak™ capacitors mounted in DIP sockets of U3, U4, U5

FIGURE 18
EB104 COMPONENT LIST

THERMAL CONSIDERATIONS FOR HIGH PERFORMANCE DEVICES

PAUL M. BROWN

INTRODUCTION

The package of an integrated circuit is its interface to the outside world. The pins and bonding wires conduct power and control voltages to and from the silicon chip (die). In addition, the pins, bonding wires and body of the package transfer heat from the die to the outside environment. Just as electrical resistance is a measure of the efficiency with which current is conducted by an electrical connection, thermal resistance measures the efficiency of heat flow. There are four thermal resistances of concern to the systems designer: θ_{JC} , the thermal resistance from the die (junction) to the package (case), θ_{CS} , the thermal resistance from the package (case) to the heat sink, θ_{SA} , the thermal resistance from the heat sink to the ambient environment, and θ_{JA} , the thermal resistance from the die (junction) to the ambient environment through the package with no additional heat sink attached.

The junction temperature and the temperature of the die can be easily calculated (see the example below) given the ambient temperature, the appropriate thermal resistance, and the power dissipated on the die. It is important to keep the die temperature under the maximum specified limit, usually 150°C, under worst case conditions; i.e. maximum ambient temperature, maximum power supply voltage, and maximum load to avoid permanent damage to the device. Reliability is also acutely affected by the junction temperature since many failure mechanisms are accelerated with an increase in temperature. An IC operating at a junction temperature, (T_J), of 125°C will typically exhibit a failure rate almost 150 times that of the same device operating at a junction temperature of 70°C.

SYSTEM THERMODYNAMICS

Thermal management in a board or system level application consists of transferring heat from an undesirable location (i.e. the die) to one where it can be dissipated into the environment without adversely affecting the system. There are three ways that heat is transferred: conduction, convection, and radiation.

Thermoconduction is the process of transferring heat through a medium from a relatively high temperature to a relatively low temperature. To maximize the conductive flow of heat, it is important to choose a medium with high thermal conductivity, such as copper or aluminum. The geometry of the medium should be chosen to yield the largest practical cross-sectional area and to shorten the conduction path. The rate of heat transfer is the greatest when there is a large difference between the high and low temperatures.

Thermoconvection, in the context of this discussion, is the transfer of heat from a solid (the IC and attached heat sinks) to a fluid (air). Convection depends upon the surface area across which the transfer takes place, the temperature difference between the solid and the fluid, and the characteristics of the fluid including: thermal expansion coefficient, specific heat, viscosity, density, and thermal conductivity. Free convection occurs when heat from the solid is conducted to the fluid in contact with it causing the fluid to become less dense and rise thus being displaced by fluid at a lower temperature. Convection is most effective if the fluid flow next to the solid is turbulent. This prevents boundary layers of fluid forming next to the solid thereby insulating the solid from the fluid.

Forced convection can be an order of magnitude more efficient than free convection. However, it is often more expensive to implement. When forced convection is used, the recommended air flow is usually between 200 and 500fpm (feet per minute). Care should be taken to insure that this air flow is turbulent.

To maximize the effectiveness of convection, it is important to mount the heat dissipating surfaces in the vertical direction for free convection or along the air flow for forced convection. The enclosure must have proper ventilation so that the flow of air is not restricted. Place low power devices close to the air source in forced convection systems to keep them at the lowest possible temperature.

Heat is also transferred via infra-red radiation. To maximize thermal radiation, it is important to choose a radiating element that has the largest effective surface area (surface area where fins do not face each other) and the highest emissivity. The radiating element must have a temperature that is high relative to that of near objects. This is especially true for the object or media (i.e. enclosure or air) that is meant to receive the radiated heat. If the "radiator" is not at the highest relative temperature, it will absorb radiated heat energy.

CALCULATING THE OPERATING DIE TEMPERATURE

A thermodynamic "circuit" can be used to easily calculate heat flow and temperature rises. Figures 1 and 2 below illustrate that heat is analogous to electrical current, temperature to voltage, and thermal resistance to electrical resistance. Ohms (volts per amp) are, therefore, analogous to °C per watt. The circuit in Figure 1 is for a device with no external heat sink and Figure 2 is for a device with an external heat sink. The minimum die temperature is the ambient temperature (if no power is dissipated).

Example: Calculate the junction temperature of an IC that dissipates one watt, has no external heat sink, operates in an ambient environment of 45°C, and has a θ_{JA} of 75°C/W.

Answer: $T_J = 120^\circ\text{C}$ (see Figure 3)

Figure 1. Basic Thermal Circuit

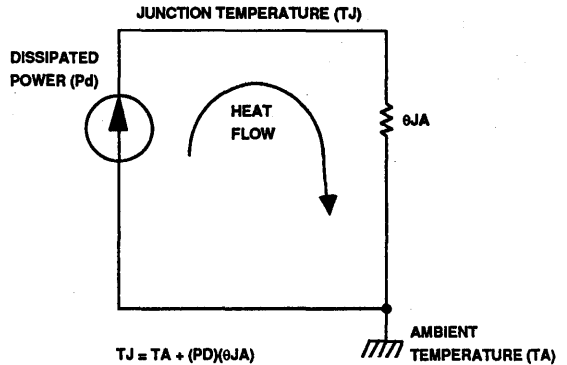


Figure 2. Thermal Circuit with External Heat Sink

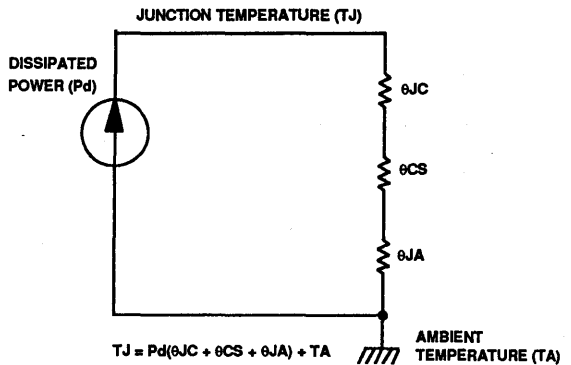
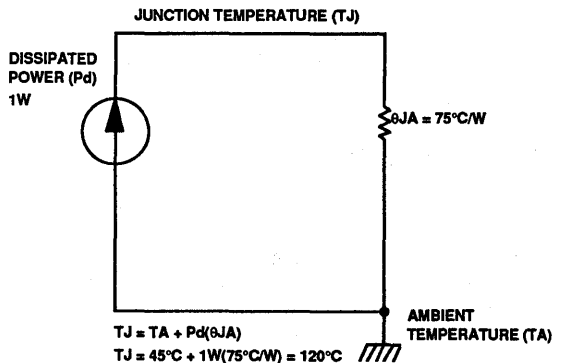


Figure 3. Junction Temperature Calculation

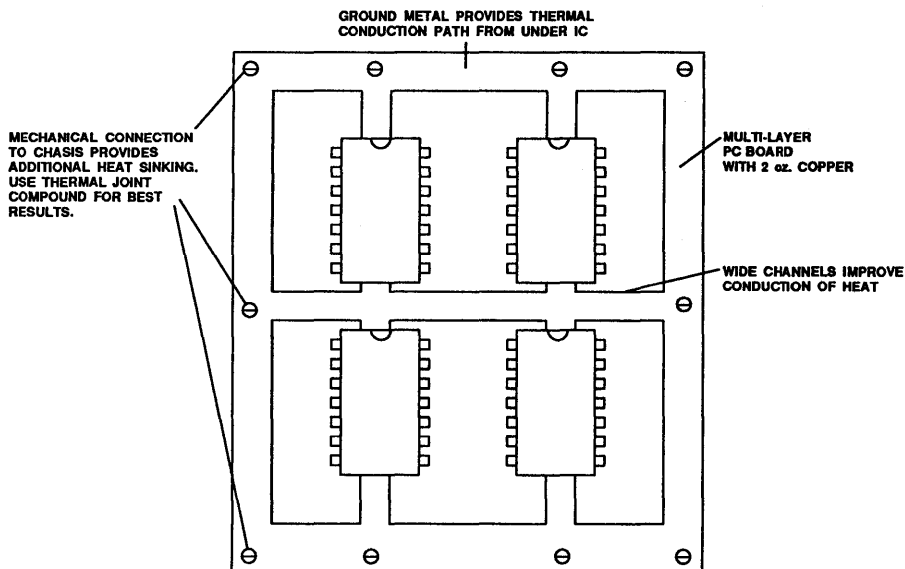


PACKAGE THERMAL RESISTANCE

The thermal resistance of an IC, both θ_{JA} and θ_{JC} , depend upon several unique product specific characteristics. Among these are: die size, the method used to attach the die to the package (glass, gold, eutectic, epoxy), bonding wire thickness, the number of bonding wires, package cavity size, package material type, package geometry and design, and package emissivity. Thermal resistance is, therefore, typically specified on the device data sheet. θ_{JA} is generally specified for a device inserted into a PC board mounted socket in still air at 25°C. This specification includes the effects of both convection and radiation. If the ambient conditions are different, i.e. moving air, θ_{JA} will be different. θ_{JC} , on the other hand, is measured with the package attached to an infinite heat sink and is a measure of thermal conduction from the die to the package.

The graphs below give a representation of the ranges of θ_{JA} and θ_{JC} that can be expected from industry standard packages. This data has been compiled from information supplied by several semiconductor and package manufacturers and is valid at sea level in still air assuming free convection. Under these conditions, approximately 70% of heat transfer occurs through convection and 30% by radiation. The thermal resistances of packages and heat sinks must be derated in other environmental conditions due to the loss in effectiveness of heat transfer. At high altitudes (770,000 ft.), only 30% of heat transfer is by convection (due to the less dense air) and 70% by radiation. In space (a very good vacuum), all heat is transferred by radiation. At ambient temperatures greater than 50°C heat transfer suffers due to decreased air density. Since there are many variables that affect thermal resistance specifications, the data supplied here is generic information and is only approximate. Consult the data sheet or the manufacturer for thermodynamic specifications of a particular device.

Figure 4. Thermal Conduction Channels



HEAT SINKING

A heat sink is a thermoconductive device that is mechanically affixed to the integrated circuit to reduce the thermal resistance from case to ambient (an infinite heat sink can only reduce θ_{JA} to θ_{JC}). Heat sinks are used with ICs that generate more heat energy than their package can effectively dissipate. Heat sinks include: devices designed to aid heat dissipation, the circuit board and its conductive traces. The ability of the circuit board to conduct heat away from the IC can be enhanced in several ways. First, whenever possible, design the P.C. board such that either a large ground or a Vcc plane is around and directly under the IC. When layout permits, wide ground traces (of 2 oz. copper) can be used to form a heat conducting channel from under the IC to the edge of the P.C. board where a good thermal connection can be made to the chassis (see Figure 4). It is important that these heat conducting channels pass under the IC since the die is usually attached to the bottom of the package (except for "cavity down pin grid arrays"). The most efficient heat conduction path is, therefore, out the bottom of the package. The package leads can also conduct a significant amount of heat away from the IC. This is especially true if 2 oz. copper traces are used. In most cases, layouts will be complicated enough that multi-layer P.C. boards will be required. This is almost unavoidable for large pin count packages or when controlled impedance techniques, such as microstrip or stripline, must be used. Multi-layer boards afford a great deal more freedom for thermal design than two layer boards. Discrete heat sink devices are available in a wide variety of forms from manufacturers, such as EG&G, Wakefield Engineering, Avid Engineering, or IERC.

Component placement is also critical. DO NOT place components that dissipate large amounts of power, such as dropping resistors, voltage regulators, etc., in close proximity to ICs that are themselves dissipating large amounts of power. Concentration of power dissipating components makes heat removal very difficult. Heat radiated by one component will be absorbed by another. Some components that appear in analog to digital and digital to analog circuitry, such as voltage references, OP amps, and buffer amplifiers, are very sensitive to temperature and should be isolated from thermal sources. Arrange components and heat sink fins to avoid blocking convection currents or forced air. Take into account the orientation that the circuit board will have when it is installed and the expected flow of convection currents and/or forced air.

It should be obvious from the above discussion that thermal design must be an integral part of the overall design of any board or system. Installing glue on or clip-on heat sinks or a fan as an afterthought is no substitute for well planned, thermal design.

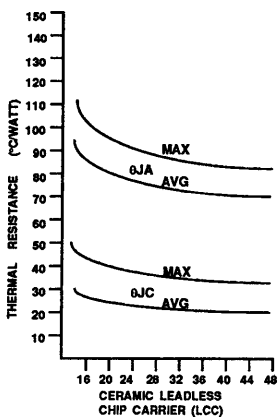
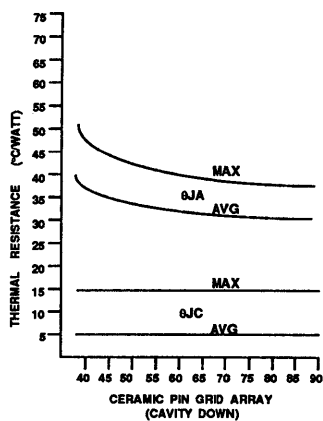
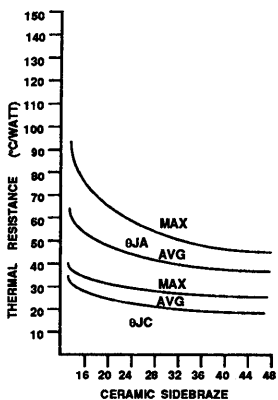
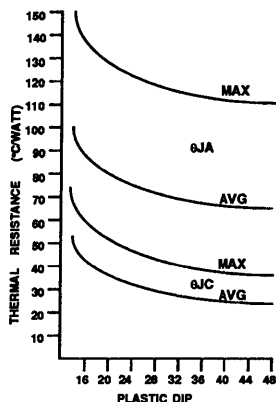
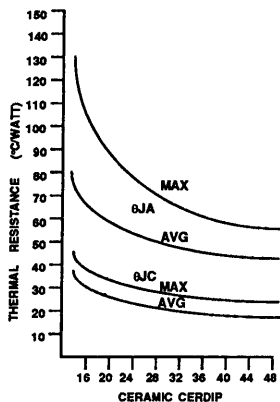
REFERENCES

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EG&G Wakefield Engineering. Standard Products Catalog. Massachusetts: EG&G Publications and Media Center, 1985.

International Electronic Research Corporation. Heat Sink/Dissipator Products and Thermal Management Guide. International Electronic Research Corporation, 1985.

Thermal Resistance Ranges for Various Package Types in Still Air (1)



(1) This is generic data. For exact values for a given product, consult a product data sheet or the manufacturer.

NOTES:

EB105 EVALUATION BOARD

INCLUDES HSCF24040 PROGRAMMABLE 7TH ORDER LOW PASS ACTIVE FILTER

Craig Wiley June 1988

FEATURES

- Complete With Socketed HSCF24040ACD Device
- Demonstrates HSCF24040 Performance and Capabilities
- Toggle Switches for On-Board Control and Programming
- Connectors Allow Easy Interfacing of External Control, Programming, and Analog Signals
- Crystal Time Base
- Leaded Power Supply Connector

APPLICATIONS

- HSCF24040 Evaluation
- Prototype System Development
- Programmable General-Purpose Subassembly

EQUIPMENT REQUIRED

- Power Supply (-5, +5 Volts)
- Analog Signal Source
- Analog Signal Monitor or Analyzer

GENERAL DESCRIPTION

The EB105 Evaluation Board allows full exercise of the Honeywell HSCF24040 Programmable 7th Order Low Pass Active Filter. Unlike a handwired breadboard, this ground-planned, printed circuit board provides a high performance, noise-free environment. It provides full demonstration and evaluation of the superb HSCF24040 dynamic characteristics. Programming and control of the device is conveniently enabled by on-board toggle switches. Alternately, programming and control can be accomplished through the on-board ribbon cable connector. This option allows software control which can aid in system development.

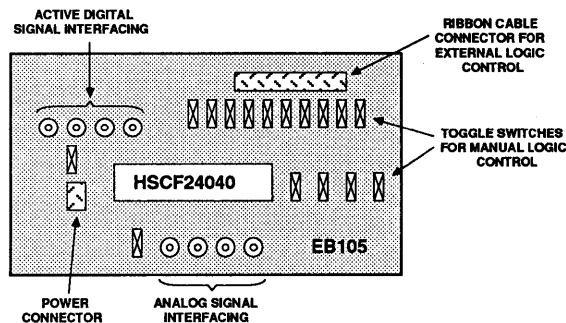
Taking full advantage of the HSCF24040 architecture, the EB105 provides an analog input and output for both the RC and switched-capacitor filters. Both of these low-

pass filters are fully programmable. Analog interfacing is accomplished with on-board BNC connectors to minimize noise and digital signal coupling. The EB105 also makes use of separate analog and digital supply grounds to further minimize digital coupling.

A clock crystal is supplied on the board which utilizes the HSCF24040 crystal oscillator feature. An external time base can be used optionally. BNC connectors are provided for external clock input and clock output, for the CONVRT output and the SYNC control line. Use of BNC connectors on these active digital lines assure a minimum of digital to analog coupling.

Application Note AN111 describes HSC24040 interfacing in detail and should be useful as a reference.

FIGURE 1 EB105 BOARD FEATURES



EB105 LAYOUT AND GENERAL INFORMATION

The EB105 contains one socketed HSCF24040 integrated circuit, an assortment of toggle switches and connectors, and a few discrete components used for power supply decoupling and logic voltage pull-up or pull-down. Board layout is shown in Figure 3. The prime function of the EB105 is to provide a low noise operating environment for the HSCF24040 and to allow ease of interface and programming for the purpose of device evaluation.

POWER SUPPLY CONNECTION

Power is supplied through the leaded Molex connector as detailed in Figure 2. Ensure that the beveled edges of the male and female connectors are aligned prior to coupling. Digital and Analog Ground should be connected together at the power supplies to provide maximum noise isolation. The male and female connectors should be coupled and the power supplies connected prior to turning on the power supplies. The power supply current consumption will be that of the HSCF24040 which is typically 15 mW.

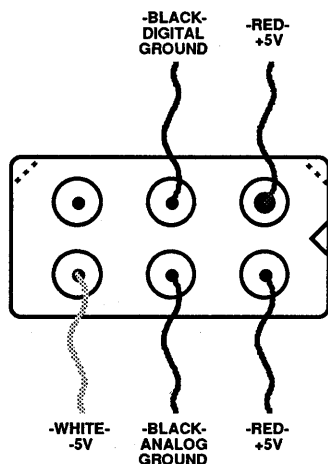


FIGURE 2
POWER SUPPLY CONNECTION
Leaded Power Connector for Jack J6
Top View

PROGRAMMING AND PARAMETER CONTROL

Operation of the EB105 must be preceded by device programming in order to establish operating characteristics. This can be accomplished manually by use of the on-board toggle switches or by software through ribbon connector jack J1. Table 1 summarizes the EB105 toggle switches, most of which are directly related to device programming. The direct programming mode, established by switch S12, allows the HSCF24040 characteristics to be changed "on the fly" by register logic switches S1-S10.

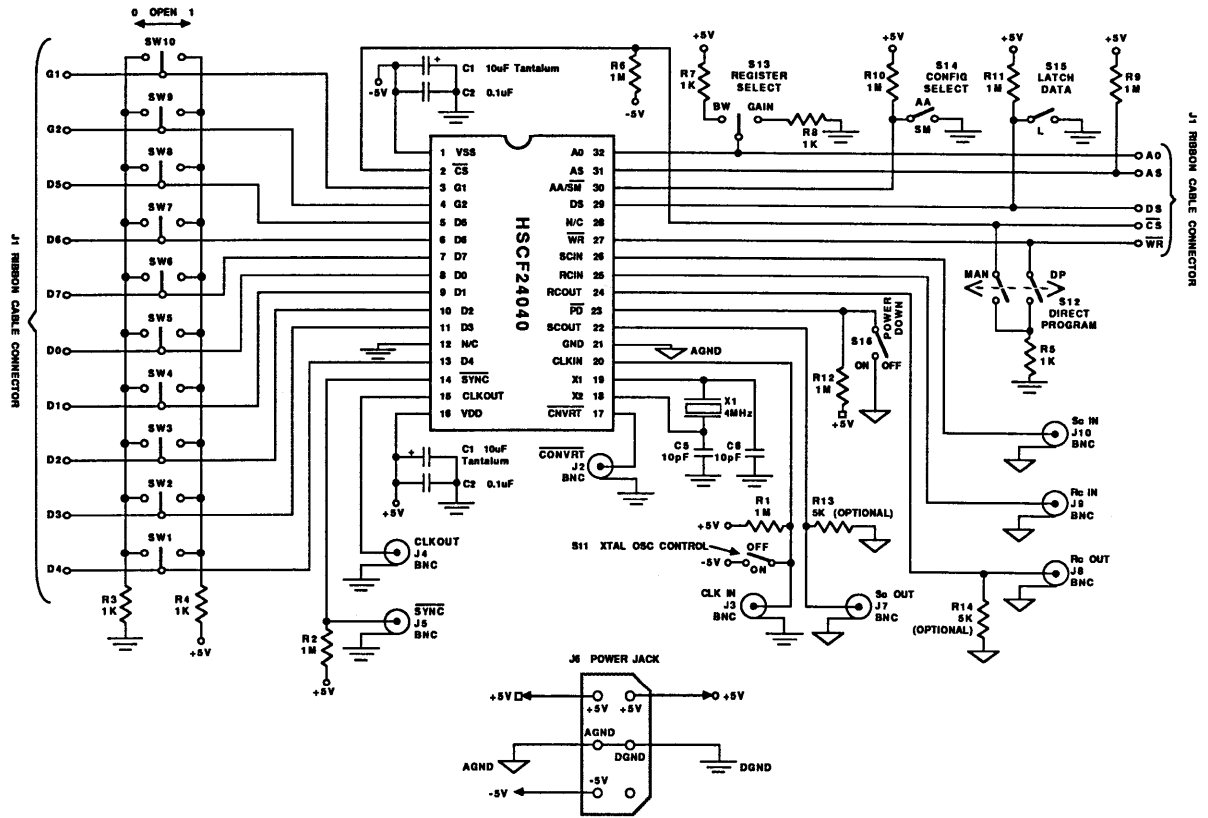
Register programming and device control can also be accomplished externally through jack J1, the ribbon cable connector. Figure 5 shows the pinout of jack J1. Note that each pin of jack J1 is connected directly to the corresponding pin of the HSCF24040. When using jack J1, ensure switches S1-S10 and S13 are in the open (center) position and S12 is in the "DP" position.

Please refer to Application Note AN111 for further information on register programming and the other input logic control.

ANALOG INTERFACING

The HSCF24040 is a low power CMOS analog circuit that is intended for applications that require driving adjacent circuitry only. The minimum output drive capability is limited to 5 kohm in parallel with 50 pF, however as much as 100 pF seldom creates a problem. Since most coaxial cable has approximately 30 pF capacitance per foot, test leads connected to Rc OUT or Sc OUT should be kept as short as possible. Excessive load capacitance will cause excessive clock feedthrough noise since the stability of the output operational amplifier is affected.

FIGURE 3
EB105 WIRING DIAGRAM



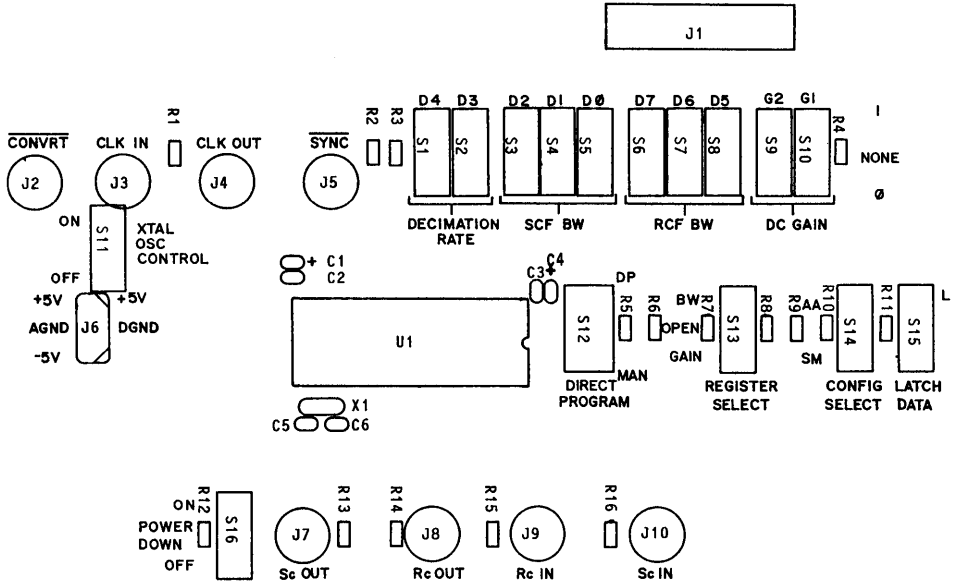


FIGURE 4
EB105 BOARD LAYOUT
Top View, Actual Size

TABLE 1 EB105 TOGGLE SWITCH SUMMARY (PART 1)**Switches S1 to S10: Register State Operators**

Position of each switch (up or down) determines the logic state of the corresponding input register upon loading. The switches will directly affect the internal logic states when the device is in the Direct Program Mode as described below. Each switch is disconnected in the center position which allows programming though jack J1.

Type: Double Pole, Single Throw, 3 Position

Positions;

UP: Loads Logic 1 State

CENTER: Disconnects switch, allows programming though Jack J1

DOWN: Loads Logic 0 State

S1: Decimator Sample Rate Bit D4

S2: Decimator Sample Rate Bit D3

S3: Clock to SCF Bandedge Divide Down Ratio Bit D2

S4: Clock to SCF Bandedge Divide Down Ratio Bit D1

S5: Clock to SCF Bandedge Divide Down Ratio Bit D0

S6: RC Filter Bandedge Bit D7

S7: RC Filter Bandedge Bit D6

S8: RC Filter Bandedge Bit D5

S9: DC Gain Bit G2

S10: DC Gain Bit G1

Switch S11: "XTAL OSC CONTROL", Crystal Oscillator Control Switch

This switch enables and disables the HSCF24040 crystal oscillator function. It is directly connected to device pin CLKIN and jack J3. When it is down in the "OFF" position it allows a clock input into jack J3 to serve as the HSCF24040 time base. When it is in the up "ON" position pin CLKIN is tied low to -5V which selects the internal crystal oscillator to serve as the time base.

Type: Single Pole, Single Throw

Positions;

UP: "ON" which enable the internal clock

DOWN: "OFF" which disables the internal clock and allows operation by the external clock

Switch S12: Direct Program Switch

Direct program mode causes the data registers for D0-D7, G1 and G2 to act transparent. When switch S12 is up in the "DIRECT PROGRAM" position, CS is pulled to VSS (-5V) by R6. This disables the A0, AS, WR, and DS inputs and places the HSCF24040 in the direct program mode. When switch S12 is down in the "MANUAL LATCH" position, input register loading is controlled by switch S15; switch S13 must be in the "BW" or "GAIN" position. Note that data latch control inputs CS, AO, AS, WR, and DS can be driven from jack J1 when S12 is in the "DP" position and S13 is in the open (center) position.

Type: Single Pole, Double Throw

Positions:

UP: "DIRECT PROGRAM" mode, D0-D7, G1, G2 latches transparent (switch open)

DOWN: "MANUAL LATCH" mode, loading controlled by S15 (switch closed)

TABLE 1 EB105 TOGGLE SWITCH SUMMARY (PART 2)**Switch S13: Register Select Switch**

This switch, which is tied directly to pin AO, selects either the D0-D7 registers or the G1, G2 registers during manual loading. It is not used in the Direct Program Mode. When in the "GAIN" (down) position, it sets pin AO to logic 0 which allows access to register bits G1 and G2. When in the "BW" (up) position, it sets pin AO to logic 1 which allows access to register D0 through D7. With switch S13 in the center position, it is disconnected and allows control of pin AO through Jack J1. The purpose of the AO pin is to allow use of an 8-bit bus to write all ten registers. The data into pin AO can be latched by a 1 to 0 logic transition on pin AS; pin AS is pulled high by resistor R9 and can be pulled low by pin AS of jack J1.

Type: Double Pole, Single Throw, 3 Position

Positions:

UP: "BW", Bits D0-D7 Latch Access

CENTER: Switch Open (Control enabled by jack J1)

DOWN: "GAIN", Bits G1, G2 Latch Access

Switch S14, "CONFIG SELECT", Filter Configuration Selection

This switch controls the logic state of HSCF24040 pin AA/SM which internally determines the analog input to the switched-capacitor filter. In the down "AA" position logic state 1 is forced which establishes the RC filter output as the SCF input. In the up "SM" position logic state 0 is forced which establishes the ScIN analog input as the input to the SCF. This switch does not have a corresponding function on Jack J1.

Type: Single Pole, Single Throw

Positions;

UP: "SM", Analog input ScIN is SCF input (Logic 0)

DOWN: "AA", RC filter output is SCF input (Logic 1)

Switch S15, "LATCH DATA" Data Strobe Control Switch

During manual loading, pushing this momentary-contact switch up into the "L" (Latch) position loads the input registers by pulling the DS input to ground. Concurrently, switch S12 must be in the "MAN" (DOWN) position or pins WR and CS must be pulled low at jack J1. This switch is not used in the Direct Program Mode.

Type: Single Pole, Single Throw, Momentary Contact

Positions;

UP: "L", Latches register data (DS = logic 0), Momentary Contact

DOWN: (DS = logic 1)

Switch 16: Power Down Switch

This switch is used to disable the analog circuitry of the HSCF24040 thus conserving power. Along with pullup resistor R12, it controls the logic state of pin PD.

Type: Single Pole, Single Throw

Positions;

UP: "POWER DOWN", Analog Portion Disabled (PD = logic 1)

DOWN: "POWER ON", Device Fully Functional (PD = logic 0)

TABLE 2 EB105 BNC CONNECTOR SUMMARY

Jack J2: "CONVRT", External A/D Converter Control Output Pin

This active low output signal indicates when the Sc OUT output is valid, i.e., when the decimator output has settled. It is used to trigger an external A/D converter or sample/hold amplifier. This jack is directly connected to the CNVRT pin of the HSCF24040.

Jack J3: "CLK IN", External Clock Input

This input jack is used to drive the HSCF24040 with an external clock. Switch S11 must be in the OFF position for this input to function. This jack is connected directly to the CLKIN pin of the HSCF24040.

Jack J4: "CLK OUT", Device Clock Output

This output jack provides a buffered version of either CLKIN or the internally generated crystal oscillator output. It is connected directly to pin CLKOUT of the HSCF24040.

Jack J5: "SYNC", Decimator Sampling Sync Input

This active low input jack resets the internal logic and counters, and can be used to synchronize the output of several devices. This jack is connected directly to pin SYNC of the HSCF24040.

Jack J7: "Sc OUT", Switched-Capacitor Filter Output

This jack is the analog output of the switched-capacitor filter after passing through the decimator. It is directly connected to the pin SCOUT of the HSCF24040. Optional load resistor R13 can be added on the EB105 board.

Jack J8: "Rc OUT", RC Filter Output

This jack is the analog output of the RC filter and is connected directly to pin RCOUT of the HSCF24040. Optional load resistor R14 can be added on the EB105 board.

Jack J9: "Rc IN", RC Filter Input

This jack is the analog input to the RC filter and is connected directly to pin RCIN of the HSCF24040.

Jack J10: "Sc IN", Switched-Capacitor Filter Input

This jack is the analog input to the Switched-capacitor filter and is directly connected to pin SCIN of the HSCF24040. This pin is internally enabled only when switch S14 "CONFIG SELECT" is up in the "SM" position.

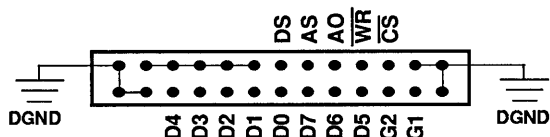


FIGURE 5
RIBBON CABLE CONNECTOR JACK J1
PIN FUNCTION SUMMARY

NOTES:

APPLICATION NOTE FOR THE HADC77600 50MHz 10-BIT FLASH A/D CONVERTER EVALUATION BOARD WITH TRACK-AND-HOLD

by Tom DeLurlo and VII Bahadur

FEATURES

- 50 MSPS TYPICAL CONVERSION RATE
- 25 MHz Full Scale input Bandwidth
- 3/4 LSB Integral Linearity (Adjustable with three reference ladder taps)
- Preamp Comparator Design/Optional Input Buffer
- Data Ready output clock generator
- Differential Output Drive - 50 or 75Ω

GENERAL DESCRIPTION

The EB106 evaluation board provides a tool to measure the performance of the HADC77600 10-bit flash A/D converter in an industry standard board level pinout. The input to the A/D converter consists of an input buffer/gain stage for a gain of 1 or 2. A track-and-hold for fast input signals, and a gain/buffer stage to drive the HADC77600 at a gain of 2 to provide a full scale input to the ADC. Included on the unit are two 100K ECL hex D-type flip-flops for differential output drive into 75Ω.

The sample rate can be set up to 50MSPS for digitizing signals up to 25MHz. The full scale input range is -1.5 to +1.5 Volts.

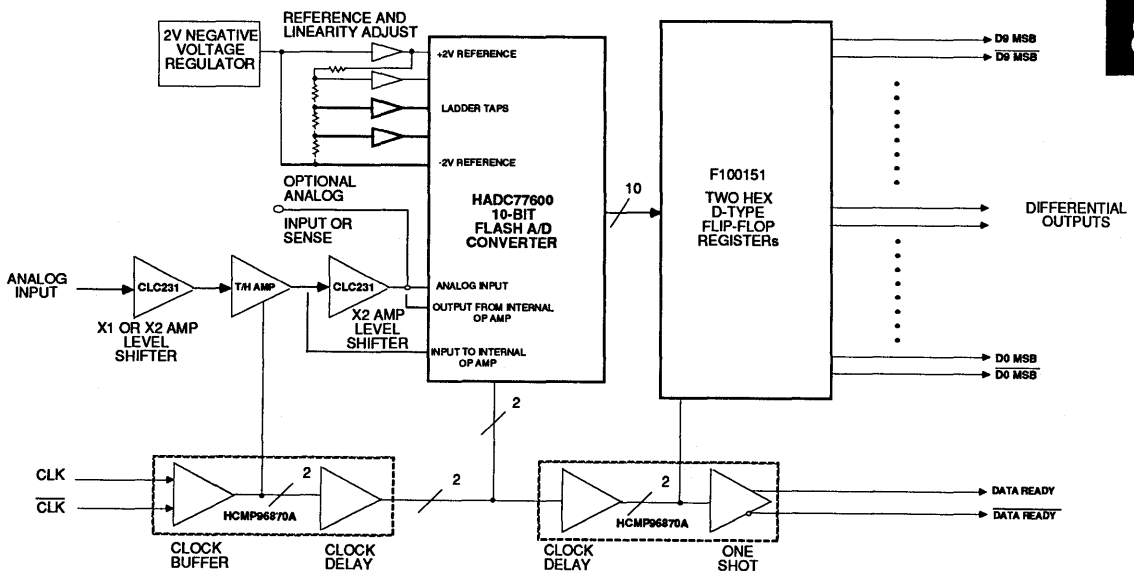
APPLICATIONS

- Evaluation of the HADC77600 A/D Converter
- 10-bit Video Digitization
- Digital Oscilloscopes
- Spectrum Analyzers
- Radar, EW
- Direct RF Down-conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

The HCMP96870A is a dual high speed differential voltage comparator used to generate an adjustable ECL compatible clock signal for timing skew between the track-and-hold, A/D converter, and output flip-flop registers. The comparator also produces differential data ready output pulses for use in determining when data is valid at the output pins.

An adjustable precision voltage regulator is on board for biasing up the ADC ladder reference resistors. Three of the HADC77600's seven ladder taps are adjusted using precision resistors and op amps to obtain better integral linearity.

BLOCK DIAGRAM



GENERAL INFORMATION

The EB106 evaluation board is a fully assembled, calibrated and tested circuit board designed to aid in the evaluation of Honeywell's HADC77600 10-bit Flash A/D converter. The board contains circuitry for track-and-hold operation, buffering and adding gain to the input signals, generating reference voltages, and programming delays for ECL level differential clock signals. All digital inputs and outputs are 10KH and 100K ECL compatible and provisions are made for gain, offset and linearity adjustments. There are adjustable capacitors available to control clock delay between the A/D, T/H and output registers as well as the data ready output signal.

The EB106 board is a four layer P C card that is manufactured for true microstripline performance. The two center copper planes are welded to a center layer of G.F. epoxy to form a large internal ground plane below the signal traces. The plane is broken into digital and analog grounds to provide separate grounding for corresponding components to achieve low noise operation. The analog and clock inputs and outputs can be connected to standard 50Ω SMA connectors for better performance or to the input/output board pins. All digital interconnects achieve 75Ω line impedance with 121/195Ω thevenin equivalent terminations at the end of the ECL lines. The lines from the outputs of the HADC77600 to the 100151 data registers are 130Ω impedance. The board output pins are connected to 510Ω pull down resistors to -5.2V, and Tektronix high impedance probe jacks are provided to monitor the clock lines and output LSBs. Standard -5.2V, +5V, and ±15 Volt power supplies are required for operation of the EB106, with nominal power dissipation of less than 15Watts. An optional input buffer, track-and-hold amplifier and linearity TAP amplifiers are on board for high performance applications.

ANALOG INPUT SECTION

The analog input section is shown in Figure 1 and 5. The input signals can either be put in through board pin 9 or 10, or through the SMA connector on the pin 9 board trace. The input traces are connected to a CLC231/EL2022 high frequency buffer-amplifier (See Table 1 for specifications). The input impedance to the board is 500Ω or 250Ω and the gain is set at 1X or 2X depending on how the two input pins are connected. If analog input #1 and #2 are connected together, the gain is set at 2X and impedance is 250Ω. If either input #1 or #2 are driven separately, the gain is 1X and impedance is 500Ω. A 1 Volt_{p-p} analog input with the 2X gain setting or 2Volt_{p-p} with the 1X setting should be applied for best operation. The negative input to the CLC231/EL2022 is tied to an offset adjust to center the input signal to the HADC77600 around ground, which is needed if a 1 or 2V_{p-p} input signal is applied. Further fine adjustment is provided by the two offset adjust pins on the CLC231/EL2022.

TRACK-AND-HOLD AMPLIFIER

The track and hold amplifier is Addacon's AHT-1010. The hold capacitor is internal to the device so no special capacitor is needed for good operation. The ADDACON's T/H could directly drive the 300pf input capacitance of the HADC77600 and provides the least amount of distortion. However Analog Devices T/H type HTS-0010KD with a Comlinear's CLC 221 buffer amp or Comlinear's T/H CLC 940 could also be used for digitization of lower analog frequencies. The clock to the T/H is buffered by a comparator to add delay to compensate for the input amplifier. Another delay is added to the clock after the T/H for the ADC to compensate for the T/H and buffer -amp.

A/D BUFFER

There are two options on the board for driving the HADC77600. The first is to use a high performance external buffer amplifier. The buffer used is either a CLC231 or EL2022. Due to the 300pF input capacitance of the ADC, compensation components are provided and can be adjusted for the desired gain/phase response required. The compensation is factory adjusted for 25MHz bandwidth operation with minimum ringing. There are two options for compensating for the input capacitance. One way is the adjustable 5-20pF capacitor in the feedback loop in parallel with the 250Ω feedback resistor. The capacitor is used in conjunction with the .1μF capacitor in series with the 75Ω resistor across the input pins (pin 5 and 6). The second compensation option is the snubber network at the output of the buffer-amp.

**TABLE 1 - COMLINEAR CLC231
BUFFER AMPLIFIER**

SPECIFICATION	CLC231
Gain Range	±1 to 5
Output (V, mA)	±11, 100
Slew Rate (V/μsec)	3000
-3dB Bandwidth (Av=2)	165MHz
Settling Time (nsec, %)	12, 0.1 15, 0.05
Harmonic(dBc) Distortion	Second Third
	-55 -59

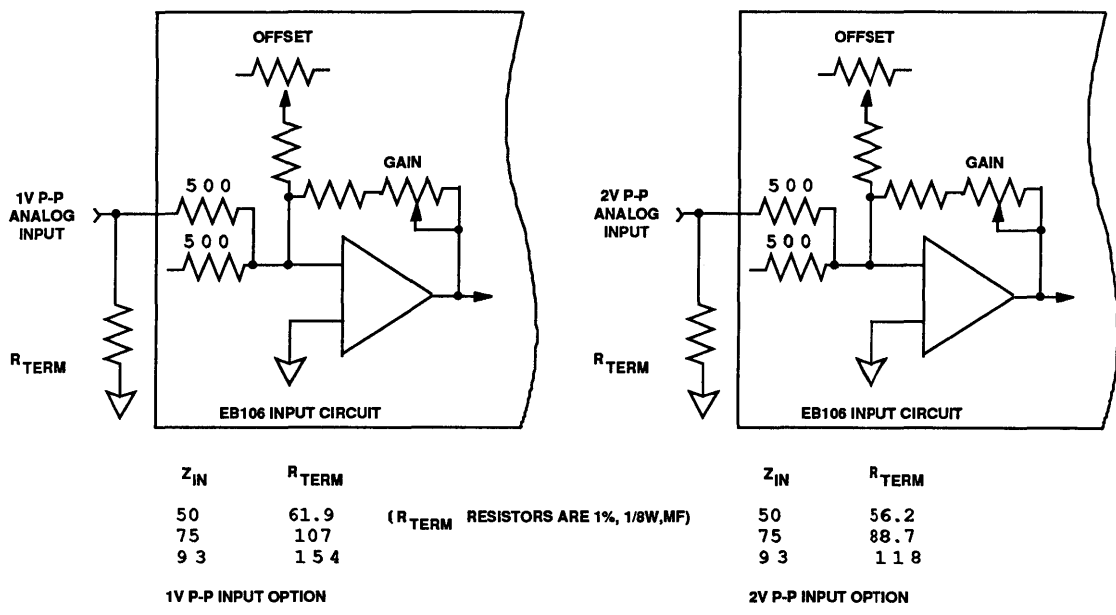


FIGURE 1 - INPUT PIN CONFIGURATIONS FOR 1V_{p-p} AND 2V_{p-p} VOLTAGE RANGE OPTIONS. WHEN DRIVING THE INPUT WITH A 50Ω OR 75Ω SOURCE, THE CORRECT TERMINATION RESISTOR MUST BE ADDED TO THE INPUT TO THE BOARD.

The gain of the buffer amplifier can be decreased by changing the 250Ω feedback resistor (connected between pins 5 and 11) to a smaller value. Do not, however, put in a value less than 125Ω. By decreasing the gain, there will be an increase in the available bandwidth of the amplifier. The BNC connector shown in the schematics near the output of the buffer-amplifier can be used for monitoring the buffer output and input to the HADC77600. The SMA should be connected to a 50Ω terminated oscilloscope and will provide a 10X attenuated signal.

The second choice for driving the ADC is to use the internal buffer amplifier provided with the HADC77600. Jumper options are included on the board to connect the input signal to the amplifier and connect the amp output to the ADC input. The external buffer-amp must be removed to operate the board in this way.

The third way is to drive the ADC directly by using a different signal route around the T/H amp. The input buffer can be bypassed by removing the 6.8Ω resistor at the output of the CLC231 and the 470Ω resistor between the SMA connector and the HADC77600. Bypass the 470Ω resistor with a jumper wire and the HADC77600 can be driven directly. The input impedance to the converter is 2KΩ in parallel with a 300pF distributed capacitance.

100K ECL CLOCK GENERATOR

Any type high frequency signal generator with differential ECL level outputs can be connected to the two clock 50Ω SMA connectors or to the board pins 2 and 3. The board can also be driven single-ended if one input pin is terminated to ground with 50Ω.

The ECL clock section consists of two HCMP96870/A dual comparators. A timing delay and skew is necessary between the T/H amplifier and A/D converter to set the time when the ADC samples the output of the T/H at various frequencies. This adjustment becomes increasingly important at high speed operation. The ideal setting would be for the ADC to receive an input after the T/H settles to a value that is ideally dc to get 10-bit accuracy. This is accomplished by the variable capacitor across the inputs of comparator B of the HCMP96870A. The capacitor in parallel with the two input resistors cause the clock signal to be ramped for more control over the switching point of the comparator. A nominal delay setting is 22ns between when the T/H amp is strobed and when the ADC receives a clock change (see Figure 3). The pulse width of the sample command clock signal should be 10 to 15ns wide. To vary the duty cycle, a threshold potentiometer can be adjusted at the input to comparators A and B.

The timing of the EB106 is based on a pipeline delay so that

TABLE 2 - POTENTIOMETER AND CAPACITOR ADJUSTMENTS

NO	FUNCTION
R1	Pot for adjusting output voltage from the ICL7664 voltage regulator to produce a -2V reference voltage for the VRBF pin A1 on the HADC77600.
R2	Pot for setting output voltage from the LM317 voltage regulator to produce a +2V power supply voltage for the HADC77600.
R18	Pot for fine adjustment of offset voltage in the positive direction to center the input signal to the HADC77600 around ground.
R22	Pot for large adjustment of offset voltage in both negative and positive direction to center the input signal to the HADC77600 around ground.
R29	Pot for fine adjustment of offset voltage in the positive direction to center the input signal to the HADC77600 around ground.
R35	Pot for fine adjustment of offset voltage in the negative direction to center the input signal to the HADC77600 around ground.
R37	Pot for fine adjustment of offset voltage in the negative direction to center the input signal to the HADC77600 around ground.
C17	"Lead" Capacitor for changing the damping factor of the input buffer. This has been set for a flat response.
C47	Cap for adjusting time delay between the T/H amplifier and the ADC.
C51	Cap for adjusting time delay between the ADC and the output data registers.
C52	Cap for adjusting time delay between the output data registers and the data ready clock signals.
C62	Cap for adjusting pulse width of the data ready differential output clocks.

data arrives at the output after a number of clock pulses due to the latency inherent in the ADC and output registers. The timing diagram in Figure represents when the true data will arrive at the output pins. Furthermore, differential output clocks (Data Ready and /Data Ready) signify when the data

settles out and is valid at the output pins. Either the rising edge Data Ready or falling edge of /Data Ready can be used as an output strobe. The adjustments for DR and /DR are only usable at 20MHz and above clock rates. The pulse width is set by C62 and can be adjusted to vary the time the DR and /DR are on. The second HCMP96870 is used for the one-shot to add additional time delay and pulse width adjustments to the data ready pulses. The equation for determining the width is:

$$t_{pw} = C(R_A + R_B) \ln \left[\frac{(1 - V_{OL}/V_{OH}) (R_A + R_B) (2 + R_2)}{(1 + V_{OL}/V_{OH}) (R_A + R_B) (R_1)} e^{+t_{pd}/C(R_A + R_B)} \right]$$

VOLTAGE REFERENCE GENERATOR

There are four voltage reference amplifiers on the board to drive three of the HADC77600 reference taps and the top reference voltage (VRTF). The bottom reference (VRBF) is driven by the Maxim ICL7664CPA precision adjustable negative voltage reference.

The reference voltage for the HADC77600 is generated by the ICL7664 and the -2Volt setting is controlled by the precision Vishay potentiometer 1280G (20KΩ 20T). The A/D converter's +2Volt reference and 3 voltage taps are controlled by one PMI quad op-amp (OP-11). The magnitude of each setting is further adjusted with potentiometer R25, R26, R32, R37, and R38 as shown in the detailed schematic (Figure 4) and board layout (Figure 5) as well as Table 2.

A/D CONVERTER SECTION

The two input pins to the HADC77600 are tied together for connection to an input signal. The pins can be connected to either the external CLC231/EL2022 or to the internal input buffer, or to an external source. There are jumpers to allow use of the internal buffer-amplifier so that the CLC231/EL2022 can be removed from the board.

The MINV and LINV inputs on the ADC are left floating but are tied internally to an ECL low. The connection choices for MINV and LINV and the corresponding output logic are shown in Table 3.

OUTPUT REGISTERS

The output data register section consists of two F100151 HEX D-type flip-flops. These provide 10 differential output data paths that are 100K ECL compatible. Each data bit has Q and /Q outputs that have 510Ω pulldown resistors to -5.2V. All outputs can drive 50 or 75Ω loads and unused output pins can be left floating.

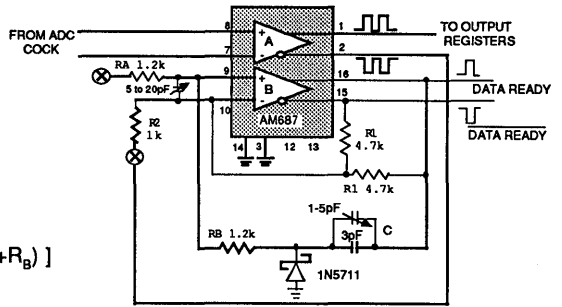


FIGURE 2 - DATA READY CLOCK GENERATOR

TABLE 3 - OUTPUT LOGIC CODING

MINV	0	0	1	1
LINV	0	1	0	1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.
.
V _{IN}	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.
.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IN}, V_{OH}

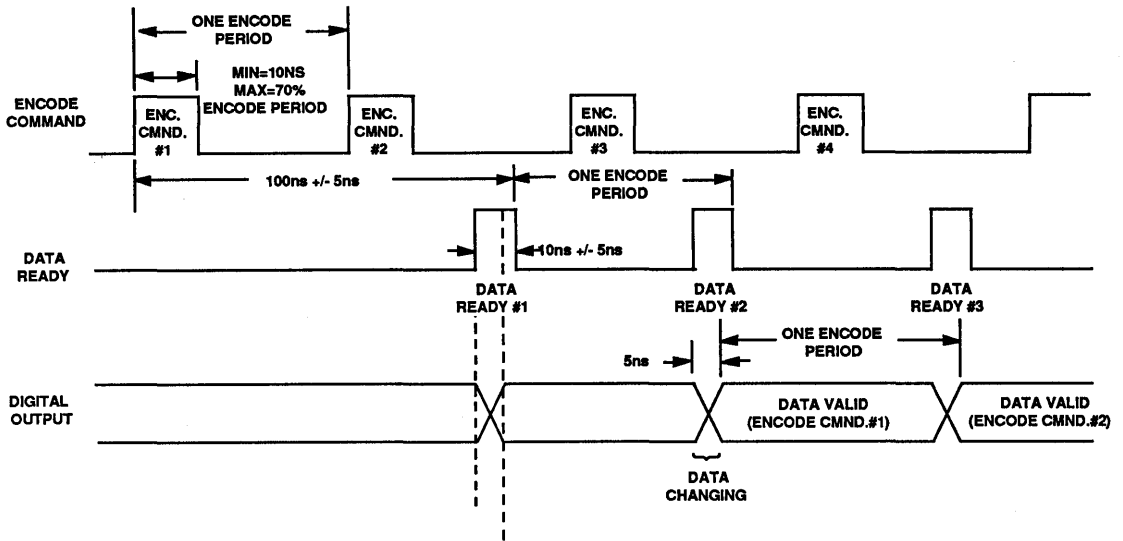
0: V_{IL}, V_{OL}

BOARD LAYOUT

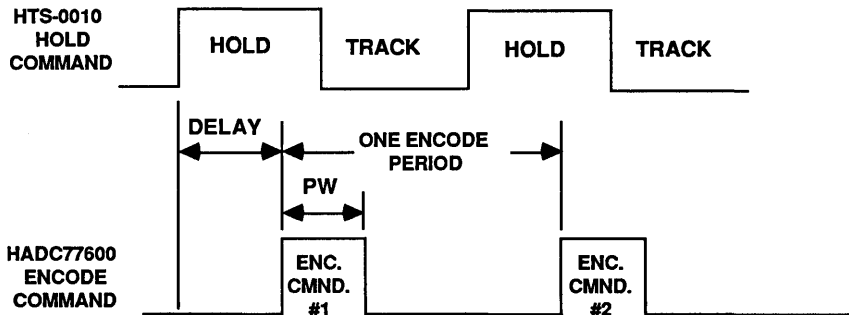
The layout of the EB106 board is shown in Figure 6. The Figure shows the position of the various potentiometers and variable capacitors for adjusting offsets and time delays. In addition, the position and types of all components are shown in Figure 6 and the parts list in Table 5. All offsets are preset for 2Vp-p bipolar inputs that swing around ground. Figure 4 and 6 show the position of the board pins and their functions. There are separate digital and analog ground pins that are connected together through an RF bead between the digital and analog ground planes. The +15V and -15V power supplies are decoupled to the analog ground plane and the +5V and -5.2V are bypassed to the digital ground plane.

FIGURE 3 - EB106 TIMING DIAGRAMS

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DATA READY OUTPUT TIMING



TIMING ADJUSTMENTS BETWEEN THE T/H AMPLIFIER AND THE HADC77600. THE DELAY BETWEEN THE T/H AND ADC AND THE PULSE WIDTH (PW) OF THE ADC CLOCK CAN ALL BE ADJUSTED FOR OPTIMAL THD AND SNR SPECIFICATIONS TO GET 10-BIT ACCURACIES.

POWER SUPPLY CONNECTIONS

Power to the EB106 is supplied through the board level pins. The supply pins are marked on the board silkscreen for the correct voltages and polarities as shown in Figure . Make sure all the supply pins are connected before powering up the board.

The power requirements for the EB106 at nominal supplies is shown in Table 4. When powering up the board, check to see if the current draw from each supply is equivalent to the numbers in the table. If there is a large difference, then recheck your connections. There are no supply protection diodes on the board for any reverse polarity connection nor is over-voltage protection provided. It is very important that the supplies be set up correctly!

TABLE 4 - POWER DISSIPATION

EB106		
Voltage	Current	Power
+15V	.128A	1.92W
-15V	.10A	1.5W
+5V	.744A	3.72W
-5.2V	1.50A	7.8W
		14.94W

DO NOT TURN ON THE POWER UNTIL ALL LEADS ARE CONNECTED TO THE SUPPLIES AND THE HARNESS IS ON THE BOARD!!

IT IS HIGHLY RECOMMENDED THAT AT LEAST 500LFPM OF FORCED AIR BE APPLIED WHEN OPERATING THE EB106.

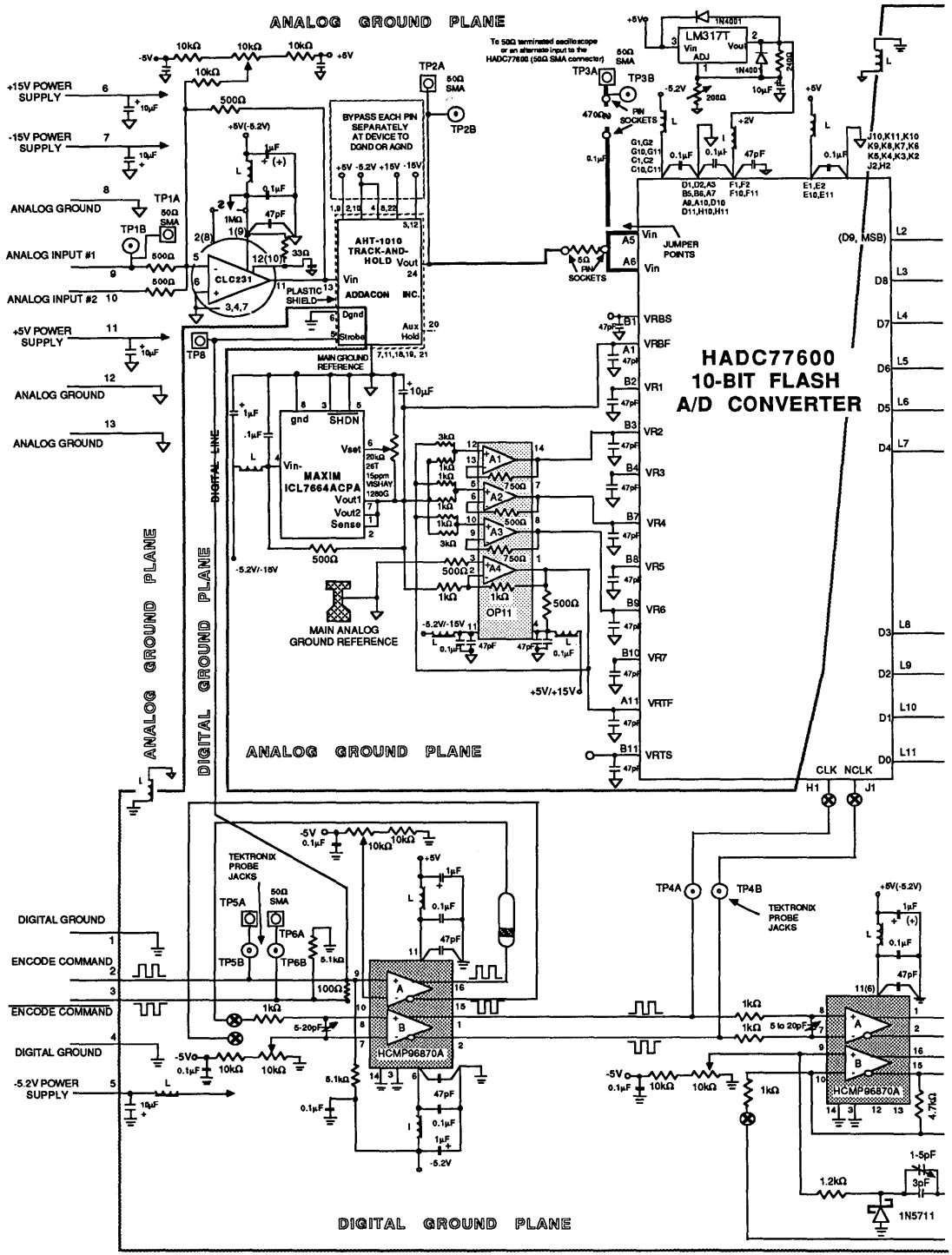
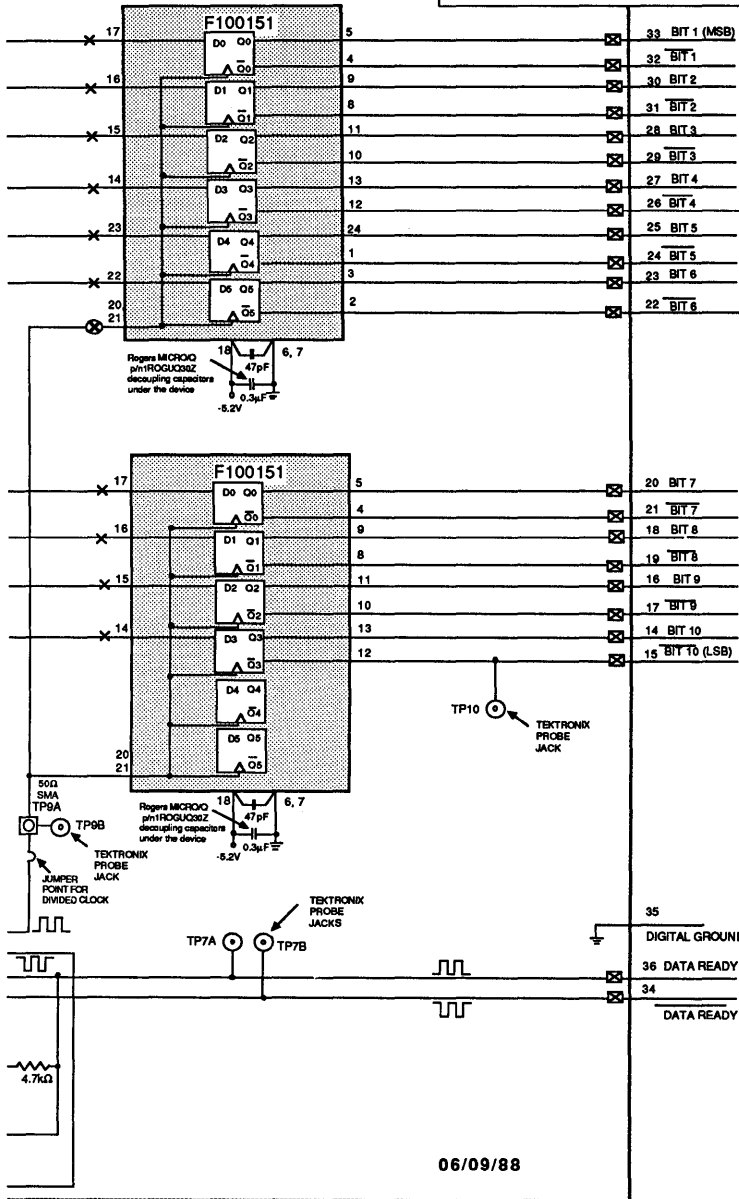
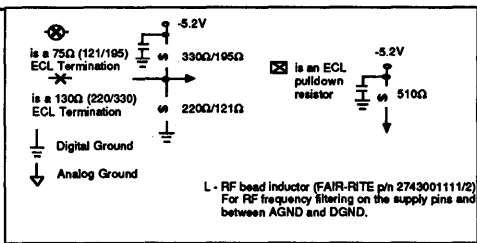


FIGURE 5 - EB106 10-BIT FLASH A/D CONVERTER EVALUATION BOARD CON-

DIGITAL GROUND PLANE



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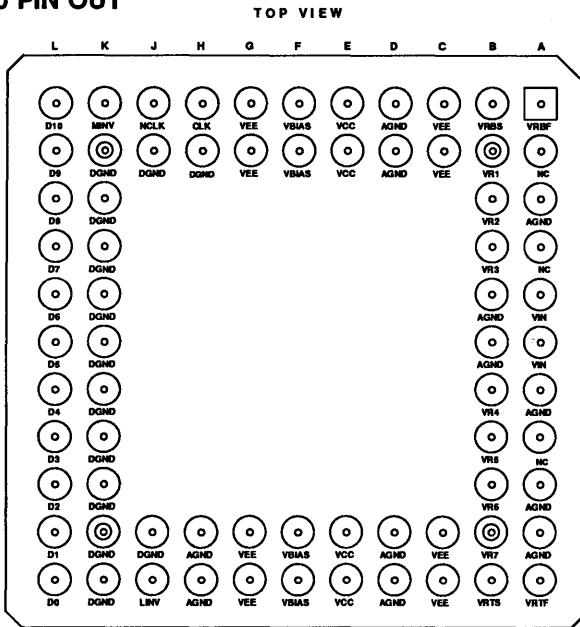
TAINING THE HADC77600 AND A TRACK-AND-HOLD AMPLIFIER.

HADC77600 PIN DESCRIPTION

Pins	Description
VEE	Analog and digital negative supply. Typically -5.2 Volts.
VBIAS	Supply voltage. Typically +2.0 Volts.
VCC	Positive digital supply. Typically +5.0 Volts.
AGND	Analog ground.
DGND	Digital ground. Return for ECL outputs. Return to termination ground.
VRT	Most positive reference. Typically +1.50 Volts.
VRTS	Sense pin for the positive reference.
VRB	Most negative reference. Typically -1.50 Volts.
VRBS	Sense pin for the negative reference.
VR1 thru VR7	Reference ladder taps in 1/8 scale increments for ladder adjustments.
LINV	Data complement control for bits 0 through 8.
MINV	Data complement control for bits 9 and 10 (OVR).
VIN	Flash converter input.
D0 thru D9	Digital ECL outputs. Capable of driving 75 Ohm loads to 10KH specifications.
D10 or OVR	Over-range bit. True when the input exceeds the voltage at VRT.

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HADC77600 PIN OUT

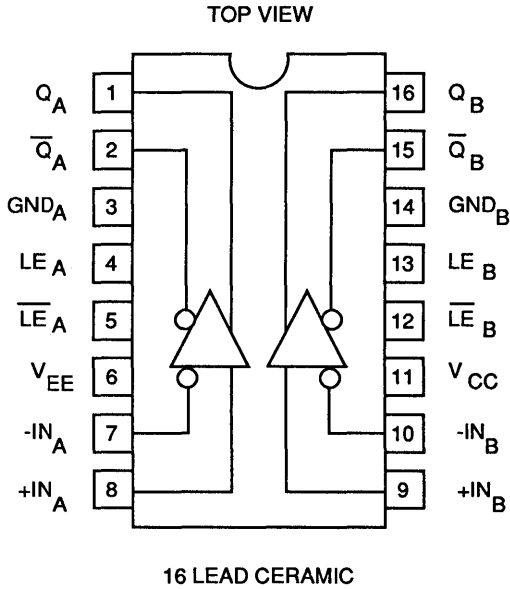


$q_{JC} < 1^{\circ}\text{C/W}$
 $q_{JA} = 25^{\circ}\text{C/W}$
 $q_{JA} \text{ w/500 LFPM air} = 14^{\circ}\text{C/W}$

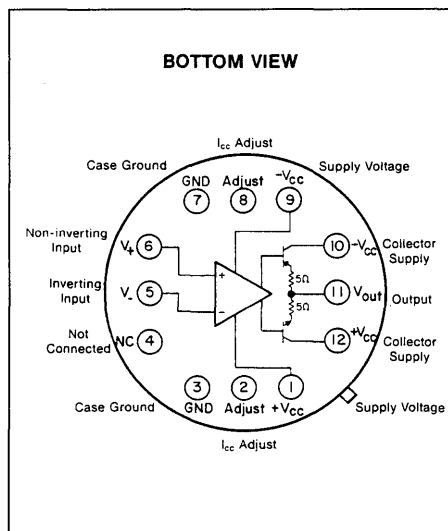
Custom package contains 120pF power supply bypass capacitance on the VCC and VEE pins.

Note: Metal top of package is connected to negative VEE.





NAME	FUNCTION
Q_A	Output A
$\overline{Q_A}$	Inverted Output A
GND_A	Ground A
$\overline{LE_A}$	Latch Enable A
LE_A	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
$\overline{LE_B}$	Inverted Latch Enable B
LE_B	Latch Enable B
GND_B	Ground B
$\overline{Q_B}$	Inverted Output B
Q_B	Output B



PIN ASSIGNMENT COMLINEAR CLC231 AND ELANTEC EL2022

NOTES:

ANALOG/DIGITAL INTERFACE REQUIREMENTS FOR THE HSCF24040

Richard D. Davis

1.1 INTRODUCTION

This technical note describes the internal workings of the HSCF24040 and assists the user in incorporating it into a system design. In particular, the interface requirements (both analog and digital) are described at length. Additionally, the system issues that determine how to choose the proper SC filter and RC filter bandwidths are discussed.

The HSCF24040 is a monolithic active filter system. Its analog signal path contains a 3rd order lowpass active RC filter (RCF), a 7th order lowpass switched-capacitor filter (SCF), and a sample-and-hold (S/H) stage. The HSCF24040 is intended to provide front end filtering for instrumentation systems of up to 12 bits. The basic function provided by the device is to bandlimit an input signal so that unwanted out-of-band components are not *aliased* or *folded* into the desired passband upon sampling by an A/D converter. For this application, the input signal to be bandlimited is applied to *RCIN* (pin 25). The output of the RC filter, *RCOUT* (pin 24), is connected internally to *SCIN* by forcing the *AA/SM* digital input (pin 30) high. The output of the S/H is provided at *SCOUT* (pin 22). This output is a *sampled-and-held* signal suitable for input to an A/D converter. The analog

signal path for this configuration is shown in Figure 1.1.

For applications where the user wishes to input signals directly into the SC filter, the *AA/SM* digital input must be forced low. This disconnects the internal path between *RCOUT* and *SCIN* and allows independent use of the RC filter and SC filter.

The bandwidths of the SC filter and RC filter and the DC gain of the SC filter are user programmable. In addition, the *hold-time* of the S/H output, *SCOUT*, is programmable. These analog attributes are controlled by 10 data inputs, *D0 - D7* and *G1 - G2*. Synchronization between the HSCF24040 and the external system (*AD*'s, *D/A*'s, *S/H*'s etc.) is provided by the *CLKOUT* and *CNVRT* outputs and the *SYNC* input.

The details of how these digital inputs control the filter attributes are described in Sections 2.0 and 3.0. The system level issues that affect the selection of the RC filter and SC filter bandwidths are discussed in Section 5.0 while details of how to actually get the proper data into the HSCF24040, including the microprocessor interface, are provided in Section 4.0.

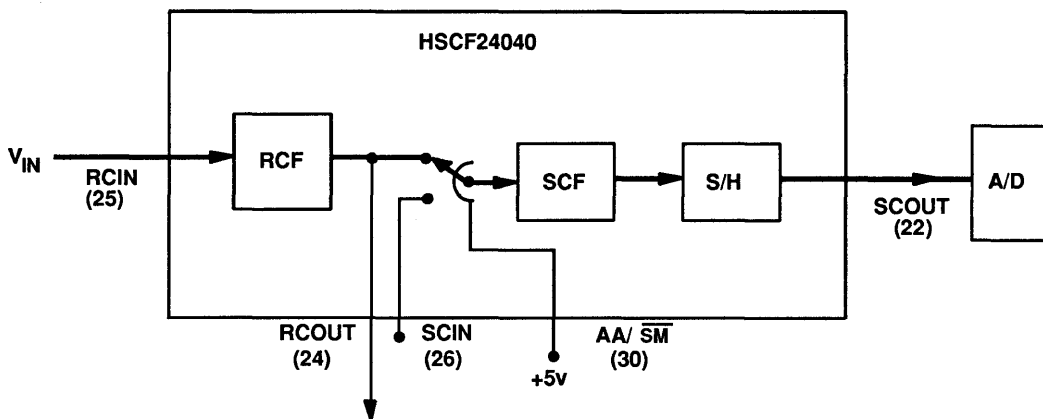


Figure 1.1 Analog Signal Path

2.0 SWITCHED-CAPACITOR FILTER AND S/H

2.1 Switched-Capacitor Basics

Switched-capacitor (SC) filters are sampled-data filters that provide extremely stable and precise filter responses. This is due to the fact that their internal *time-constants* depend only on the filter's switching frequency and the ratios of monolithic capacitors. The switching frequency is normally derived from a crystal oscillator and is therefore very precise. Ratios of on-chip capacitors are nominally accurate to 0.1%. Therefore, high order/sharp rolloff filters can be manufactured without requiring any post-production trimming. Furthermore, since the SC filter's time-constants are inversely proportional to the switching frequency, the filter's bandedge can be programmed simply by varying the frequency of the SC filter clock.

SC filters operate by transferring *charge packets* rather than continuous currents. Consider the RC integrator shown in Figure 2.1a. A voltage V_{in} causes a current V_{in}/R to flow into the feedback capacitor C . The SC integrator shown in Figure 2.1b replaces the resistor R with a switched capacitor, C_{in} . The MOSFET switches periodically toggle the capacitor between the input V_{in} and the input node of the op-amp. This is accomplished via the two-phase, non-overlapping clocks: ϕ_1 and ϕ_2 . The period of these clock signals is T_{sc} .

Every T_{sc} seconds an amount of charge equal to $C_{in}V_{in}$ is transferred to the feedback capacitor. The *average* input current is therefore $C_{in}V_{in}/T_{sc}$ and the *effective* resistance is T_{sc}/C_{in} . The time constant of the RC integrator is given by $\tau = RC$. The time constant of the SC integrator is given by $\tau = T_{sc}C/C_{in}$. Thus the time constant of the SC integrator (and therefore the filter response of an SCF built from such integrators) depends only upon the clock frequency and the ratios of on-chip capacitors.

The input to the SC filter on the HSCF24040 is *double sampling* as shown in Figure 2.2. In this case, charge is transferred on both phases of the filter clocks. Therefore, the effective input sampling rate is $f_{sample} = 2/T_{sc}$.

2.2 Filter Clocks and the SCF Bandwidth

A partial block diagram of the HSCF24040's logic, SC filter, and S/H is shown in Figure 2.3. The master clock is either provided by the user via the *CLK/IN* input (pin 20) or by using the on-chip crystal oscillator. The crystal oscillator is enabled by forcing the *CLK/IN* input to the negative supply, VSS. The crystal oscillator is disabled

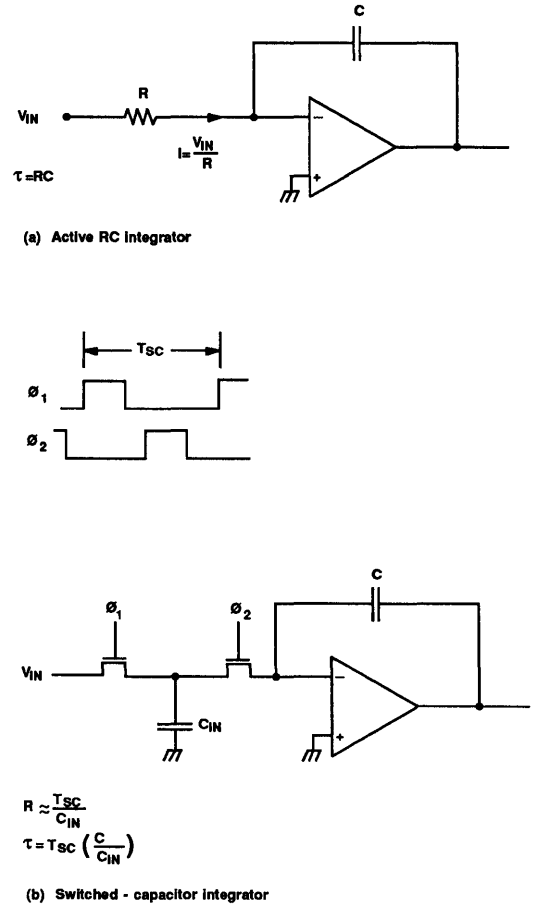


Figure 2.1 RC & SC Integrators

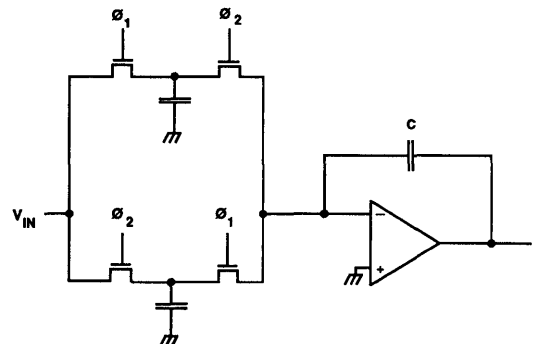


Figure 2.2 SC Double Sampling Input

as long as the CLKIN input remains between ground and the positive supply, VDD. (Thus whenever CLKIN is being driven by an external [0-VDD] clock signal the crystal oscillator is disabled.) Let us define the frequency of the master clock signal as f_{MCLK} . The master clock first enters the *programmable divide down* section. This section also generates the two-phase, non-overlapping clock signals used by the SC filter. Define the frequency of the SCF clock signals, ϕ_1 and ϕ_2 , as f_{SCF} . The relationship between the master clock frequency, f_{MCLK} , and the SCF clock frequency, f_{SCF} , depends on the input data bits D0-D2 that control the divide-down factor.

where N is the divide-down factor determined by D0-D2. These relationships are further specified in Table 2.1.

D0	D1	D2	N	f_{MCLK}/f_{SCF}	f_{MCLK}/f_c
0	0	0	4	4	200
0	0	1	8	8	400
0	1	0	16	16	800
0	1	1	32	32	1,600
1	0	0	64	64	3,200
1	0	1	128	128	6,400
1	1	X	256	256	12,800

X=don't care

TABLE 2.1

Define the bandedge or cutoff frequency of the SC filter as f_c . The relationship between the SC filter bandedge and the SC filter clock frequency is *fixed* and is given by:

$$f_c = f_{SCF} / 50$$

The relationship between the master clock frequency, the SC filter clock frequency, the SC filter bandedge, and the programming bits D0-D2 can now be given by:

$$f_{SCF} = f_{MCLK} / N$$

$$f_c = f_{SCF} / 50 = f_{MCLK} / (50 \cdot N)$$

The output of the SC filter is a *sampled-and-held* signal that changes values on the rising edge of each ϕ_1 clock and remains constant between these times. This is shown in Figure 2.4.

2.3 S/H and Programmable Decimator

The output of the SC filter is sampled by an on-chip sample-and-hold circuit (S/H). The S/H *samples* the

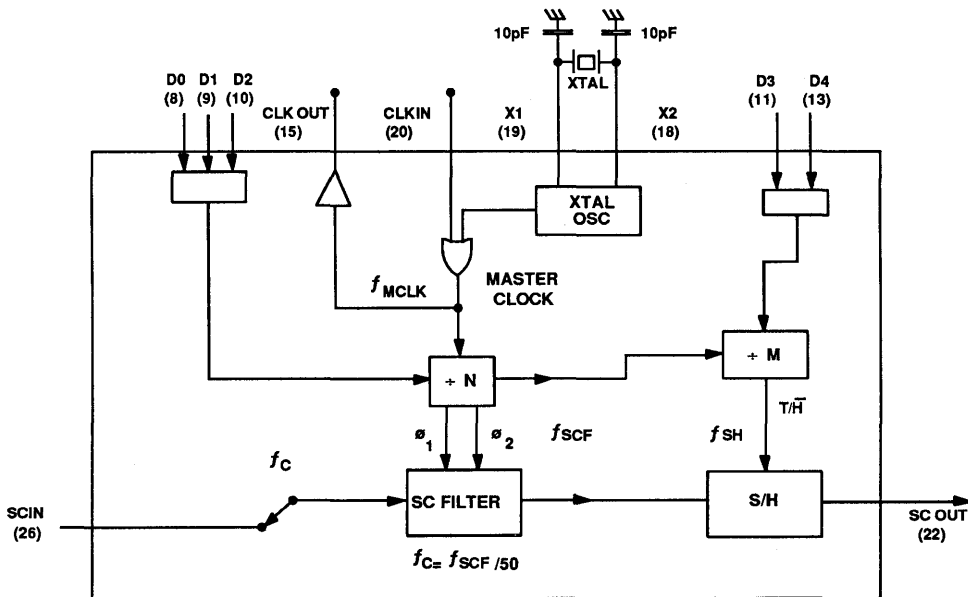


Figure 2.3 HSCF24040 Partial Block Diagram

output of the SC filter only during the time when the SC filter clock $\emptyset 2$ is high. This is illustrated in Figure 2.5. The S/H holds this input value until it takes another sample during a subsequent $\emptyset 2$. This process is controlled by the S/H logic shown in Figure 2.3. This section contains programmable divide-down logic that is controlled by the programming inputs D3 and D4.

The S/H can be programmed to wait a certain amount of time before taking another sample from the SC filter. The amount of time that the S/H waits is determined by the programming bits D3 and D4. When D3 = D4 = 0, the S/H samples on every 2nd $\emptyset 2$. When D3 = 0 and D4 = 1, the S/H samples on every 4th $\emptyset 2$. When D3 = 1 and D4 = 0, the S/H samples on every 8th $\emptyset 2$. Finally, when D3 = D4 = 1, the S/H samples on every 12th $\emptyset 2$.

The *sampled-and-held* output at SCOUT (pin 22) therefore changes values at a rate that is a *submultiple* of the SC filter clock rate f_{scf} . Let us define the sample rate of the S/H output at SCOUT by $f_{s/h}$. The relationship between the sample rate at SCOUT and the SC filter clock rate and SC filter bandedge is given in Table 2.2.

D3	D4	$f_{scf}/f_{s/h}$	$f_{s/h}/f_c$
0	0	2	25.0
0	1	4	12.5
1	0	8	6.25
1	1	12	4.1667

TABLE 2.2

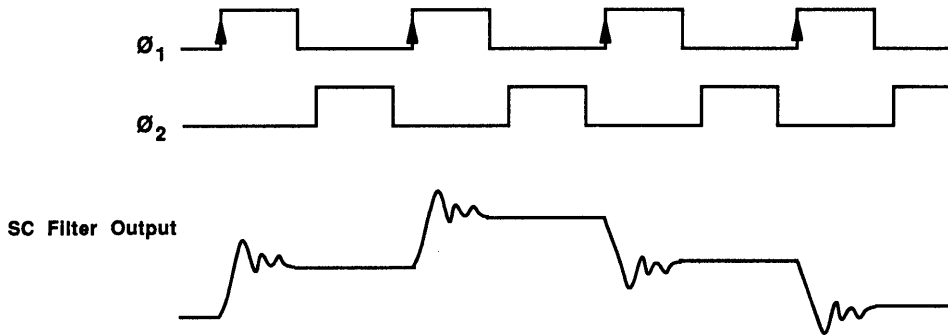


Figure 2.4 SC Filter Output

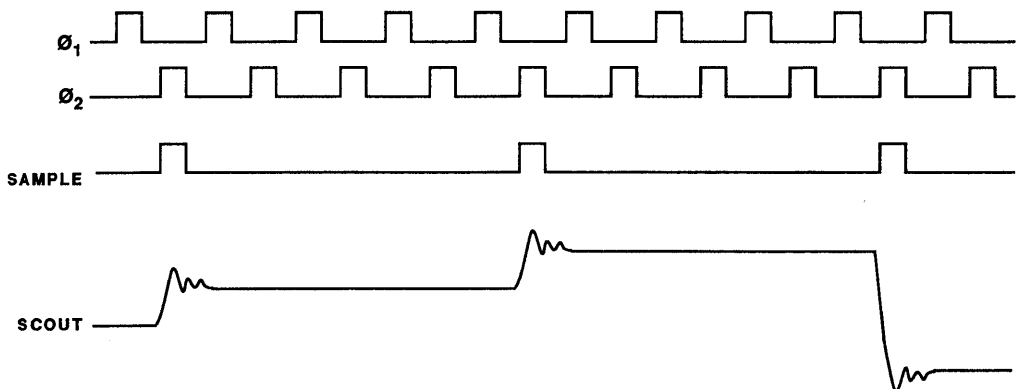


Figure 2.5 S/H Sampled SC Filter Output

Because the S/H *reduces* the sample rate at the output of the SC filter, it is also called a *decimator*. The point to remember is that the S/H *samples* every 2nd, 4th, 8th, or 12th output provided by the SC filter and *holds* this value at *SCOUT* until another sample is taken.

An example will now be given. Consider the case where a 10kHz SC filter bandwidth is desired. The output of the HSCF24040 is to be fed into a 12-bit A/D converter that converts in 20 μ sec. The master clock frequency is fixed at 4MHz.

Solution: By programming D0=D1=0 and D2=1, a 10kHz SC filter bandwidth is achieved. The output of the SC filter changes at a rate of 4MHz/8 = 500kHz. The *hold* time of the SC filter is thus only 2 μ sec and must be further increased by the on-chip S/H. If the HSCF24040 is programmed with D3=D4=1, the sample rate at *SCOUT* 500kHz/12 = 41.667kHz which results in a hold time of 24 μ sec. This meets the requirements for the A/D converter. Also note that we are converting the (now bandlimited) input signal at a rate slightly greater than 4 times the bandedge frequency of 10kHz.

2.4 Synchronization

Section 2.3 discussed how the *SCOUT* output of the HSCF24040 is a sampled-and-held signal with a programmable hold time. In order to synchronize this output with an external S/H or A/D converter, *CNVRT* output is provided. This *active low* digital output, tells the user when the *SCOUT* output has settled to a new value and can be externally sampled or converted. The timing for *CNVRT* is shown in Figure 2.6. *CNVRT* goes low on

the rising edge of the SC clock $\phi 2$ that *follows* the $\phi 2$ period when the on-chip S/H took its sample. *CNVRT* goes high on the falling edge of the SC clock $\phi 1$ that *preceeds* the rising edge of the $\phi 2$ when the next sample is taken by the S/H. Thus the *hold* time as indicated by the *CNVRT* output is either 1, 3, 7, or 11 SC filter clock periods long. The falling edge of the *CNVRT* signal is coincident with the rising edge of the master clock. It is intended that the falling edge of the *CNVRT* output be used as a strobe for triggering an external S/H or A/D converter.

The master clock signal is driven off-chip via the *CLKOUT* output (pin 15). This digital output functions independent of whether the user is supplying an external clock via the *CLKIN* input or is using the on-chip crystal oscillator.

The other part of the synchronization issue involves telling the HSCF24040 *which* master clock period should be aligned with the falling edge of the *CNVRT* signal. As an example of why this is necessary, consider the case of multiple HSCF24040's that feed a MUX prior to A/D conversion. This is shown in Figure 2.7. If it is desired that all of the HSCF24040's sample their inputs *simultaneously*, then they must all be synchronized to each other. This can be accomplished by using a common master clock for all filters and by tying all of the *SYNC* (pin 14) inputs together and supplying a negative edge on this common *SYNC* input. On the next rising edge of the master clock, two things happen: (1) the $\phi 1$ and $\phi 2$ SC filter clocks are reset beginning with the rising edge of $\phi 2$ and (2) the *CNVRT* output goes low.

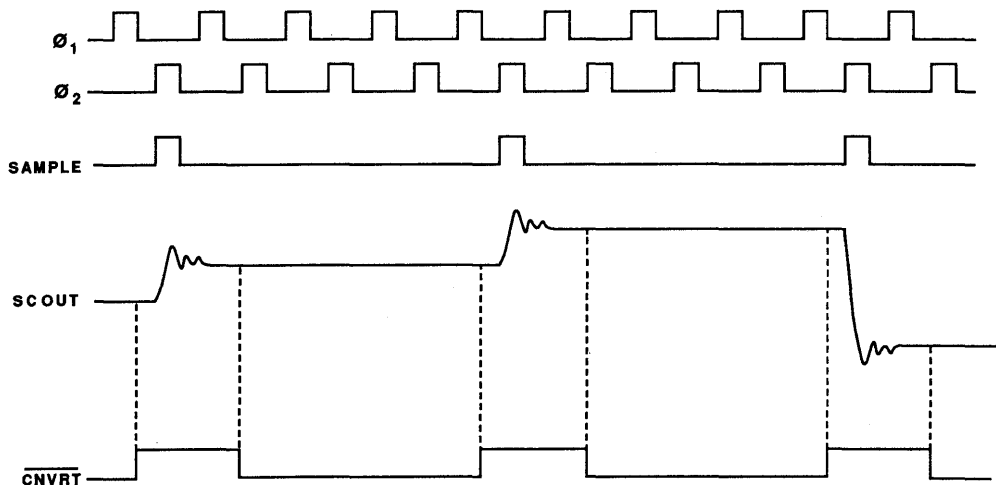


Figure 2.6 *CNVRT* Timing

Note that all of the HSCF24040 SC filter clocks are now synchronized and their \overline{CNVRT} outputs change at the same times. (This assumes of course that all of the HSCF24040's have the same values for D0-D4 and are using a common master clock.)

The actual sampling instant of the individual HSCF24040's may actually differ somewhat due to differences in the delay between the externally applied master clock and the on-chip generation of the ϕ_1 and ϕ_2 clock signals. This difference should typically be less than 10nsec.

In order for proper synchronization to occur, the falling edge of the common \overline{SYNC} input must occur at least 75nsec after the rising edge of the previous \overline{CLKOUT} period and must occur at least 75nsec before the rising edge of the next \overline{CLKOUT} period.

Once the HSCF24040's have been synchronized via the \overline{SYNC} input, they *do not* need to be re-synchronized every $1/f_{S/H}$ seconds. This is because an on-chip \overline{SYNC} signal is generated every $1/f_{S/H}$ seconds. It is required, however, that the external \overline{SYNC} input return to a logic high level at least 1 master clock cycle prior to the falling edge of the next \overline{CNVRT} output. (Otherwise, the on-chip \overline{SYNC} will not function.) If the user does not need the synchronization feature, the \overline{SYNC} input should be tied high.

It should be noted that whenever the HSCF24040 is resynchronized, the SC filter clocks, ϕ_1 and ϕ_2 are RESET. This will cause a transient in the SC filter which must die out before a valid output is obtained which takes $1/f_c$ seconds to occur, worst case. Therefore it is best to synchronize the HSCF24040 only during a power-up reset or system set-up period, and subsequently allow the internal synchronization signal to control the S/H timing.

The DC gain of the SC filter is programmable via the programming inputs G1 and G2. The relationship between SCF DC gain and these inputs is given in Table 2.3. Note that the internal signal swing of the SC filter is ± 3 volts. This means that if a gain of 8.0 is used the SC filter input must be limited to ± 0.375 volts in order to prevent clipping or distortion.

G1	G2	SCF DC Gain
0	0	8.0
0	1	4.0
1	0	2.0
1	1	1.0

TABLE 2.3

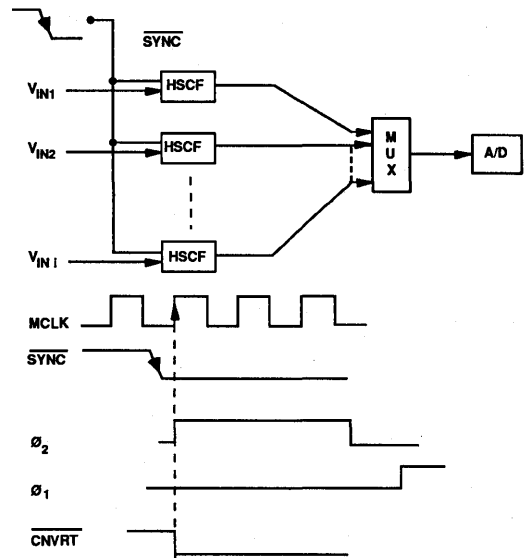


Figure 2.7 Multiple HSCF Sync

3.0 ACTIVE RC FILTER

The HSCF24040 also contains a 3rd order, active RC, lowpass filter. The DC gain of the RC filter is trimmed so that the gain through both the RC filter and SC filter is unity $\pm 0.1\%$. The RC filter's input/output signal swings are limited to ± 3 volts. The 3dB bandwidth of the RC filter is programmable via the programming inputs D5-D7. Eight different bandwidths are available ranging from 7kHz to 80kHz. The accuracy of the RC bandwidths is $+5\%$ and -0% from nominal. The bandwidths are set to this accuracy by laser trimming on-chip resistors during wafer test. The relationship between the inputs D5-D7 and the RC filter bandwidths are given in Table 3.1. The system aspects of how to choose the proper RC filter bandwidth for a particular SC filter bandwidth are discussed in Section 5.0.

D7	D6	D5	RCF 3dB Bandwidth
0	0	0	80kHz
0	0	1	56kHz
0	1	0	40kHz
0	1	1	28kHz
1	0	0	20kHz
1	0	1	14kHz
1	1	0	10kHz
1	1	1	7kHz

TABLE 3.1

4.0 DATA INPUT INCLUDING MICROPROCESSOR INTERFACE

As mentioned in Sections 2.0 and 3.0, there are 10 data inputs, D0-D7 and G1-G2, that control the analog attributes of the SC filter and RC filter. This section explains how these data inputs are read by the HSCF24040.

The HSCF24040 has two basic modes of data input: *direct program* and *data latch*. The direct program mode is entered by forcing the \overline{CS} input to the negative supply, VSS. This disables the remaining data control inputs, DS , \overline{WR} , $A0$, and AS . At the same time, the internal data latches for D0-D7 and G1-G2 are made to be transparent. This causes the values for D0-D7 and G1-G2 to be transmitted directly into the HSCF24040 and modify the filter attributes immediately. The direct program mode is useful for those applications where the 10 data inputs can be hardwired or are driven by a dedicated set of external latches. Note also that the $CNVRT$ and $CLKOUT$ outputs and $SYNC$ input are not effected by which programming mode is used.

The data latch mode is characterized by having to latch the 10 data inputs into their internal data registers. This process is controlled by the five microprocessor inputs \overline{CS} , DS , \overline{WR} , $A0$, and AS . All of these signals must range between ground and the positive supply, VDD, when in the data latch mode. An equivalent logic

diagram is shown in Figure 4.1. The three input signals \overline{CS} , DS and \overline{WR} are used to generate the actual latch signal. The $A0$ and AS inputs are used to determine which group of data inputs are being latched into the HSCF24040: D0-D7 representing bandwidth information or G1-G2 representing DC gain information.

The internal latch signal, ILATCH, is generated by inputting the signals \overline{CS} , DS , and \overline{WR} into a NAND gate. Thus Table 4.1 shows the three ways to generate a rising edge on ILATCH.

\overline{CS}	DS	\overline{WR}	ILATCH
0	1	—	—
0	—	0	—
—	1	0	—
1	X	X	1
X	0	X	1
X	X	1	1

TABLE 4.1

The rising edge on ILATCH generates a falling edge latch signal on either GAIN LATCH or BW LATCH, depending on the value of the internal REGISTER SELECT signal. If REGISTER SELECT is high, the BW LATCH is enabled. If low, the GAIN LATCH is enabled.

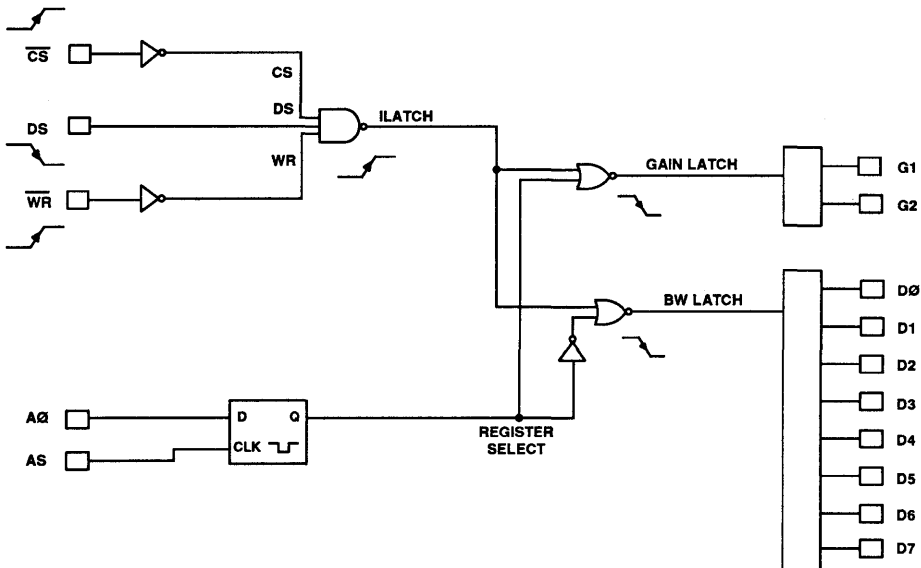


Figure 4.1 Equivalent Latch Logic

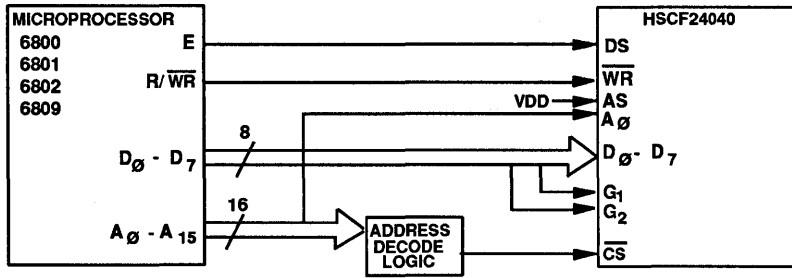


Figure 4.2 Motorola 8-bit Bus Connection

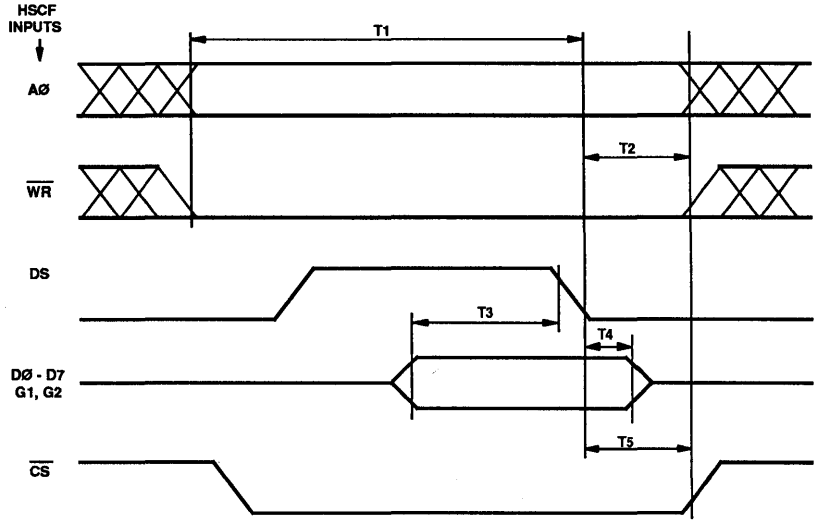


Figure 4.3 Timing Diagram for Non-multiplexed Bus

Figure 4.3 Microprocessor interface timing for non-multiplexed bus (A0 not latched)

T1 = Non-multiplexed address setup time	T1 ≥ 100nsec
T2 = Non-multiplexed address hold time	T2 ≥ 10nsec
T3 = Data setup time	T3 ≥ 100nsec
T4 = Data hold time	T4 ≥ 10 nsec
T5 = CS, WR hold time	T5 ≥ 10nsec

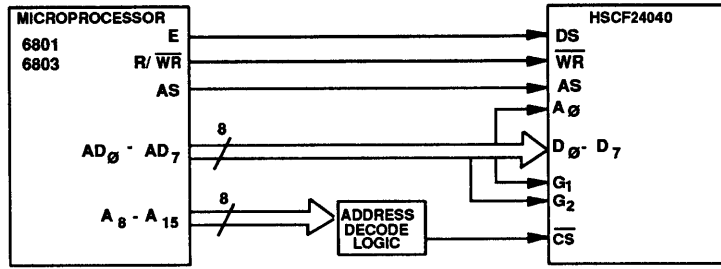


Figure 4.4 Motorola Multiplexed Bus

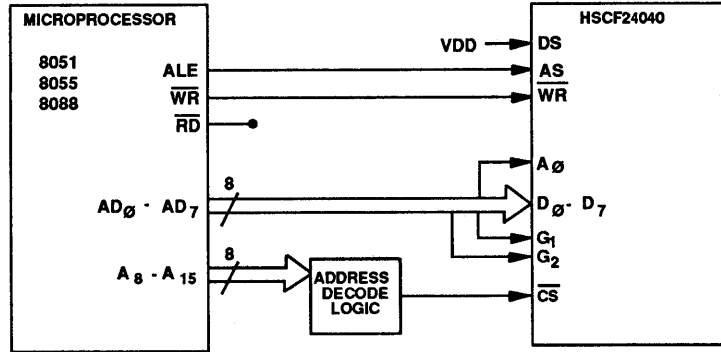


Figure 4.5 Intel Multiplexed Bus

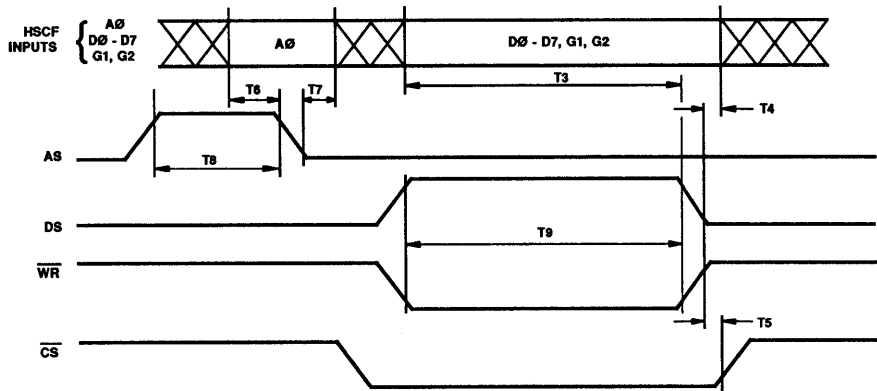


Figure 4.6 Timing Diagram for Multiplexed Bus

Figure 4.6 Microprocessor interface for multiplexed bus format (A0 latched)
 Intel uses WR to latch data. Motorola uses DS to latch data.

- | | | | |
|-----------------------------------|--------------|-----------------------------|--------------|
| T6=Multiplexed address setup time | T6 ≥ 20nsec | T5=CS hold time | T5 ≥ 10nsec |
| T7=Multiplexed address hold time | T7 ≥ 10nsec | T8=AS pulse width | T8 ≥ 50nsec |
| T3=Data setup time | T3 ≥ 100nsec | T9=Latch signal pulse width | T9 ≥ 100nsec |
| T4=Data hold time | T4 ≥ 10 nsec | | |

A0	AS	Internal Register
1	1	BW Register D0-D7
0	1	Gain Register G1-G2
X	0	BW or Gain depending on latched value of A0

TABLE 4.2

The D flip-flop, that has A0 as its D input, is only a half-latch. Therefore, when AS is high, A0 propagates directly through to the REGISTER SELECT signal. When AS goes low, the value of A0 that was present just prior to the transition is latched into the flip-flop. The relationship between A0, AS, and which register is selected is given in Table 4.2.

When using a microprocessor where the address information is valid during and entire bus cycle, there is no need to latch the value of A0 using the AS strobe input. The A0 input can simply be connected to one of the microprocessor address bits and the AS input can be tied high. A typical connection to a Motorola 8-bit non-multiplexed microprocessor bus is illustrated in Figure 4.2. The timing diagram for this case is shown in Figure 4.3. Note that two write cycles are required to write new data into both the gain and bandwidth registers.

When using a microprocessor where the address information is time-multiplexed with the data information on the same bus, the AS input must be used. An example would be the case of a Motorola 8-bit multiplexed microprocessor bus as illustrated in Figure 4.4. Figure 4.5 shows the connections necessary for an Intel 8-bit multiplexed microprocessor bus. The timing diagrams for the multiplexed bus case (both Motorola and Intel) are shown in Figure 4.6.

5.0 SYSTEM CONSIDERATIONS FOR CHOOSING BANDWIDTHS

The SC filter in the HSCF24040 is a seventh order Chebyshev lowpass. The passband ripple is less than ± 0.1 dB. Additionally, the loss for frequencies greater than 3 times the SC filter bandedge is better than 76dB. Because of this, the SCOUT output can be converted by an A/D (or re-sampled) at a rate as low as 4 times the filter bandedge while guaranteeing that all out-of-band signals aliased into the passband are smaller than 1/2 LSB at 12 bits. This is illustrated in Figure 5.1.

Although the SC filter provides excellent filtering and protection against aliasing, it does have one drawback. Because it is a sampled-data filter, it can fold or alias out-of-band energy into the desired passband just as an external A/D converter (or external S/H) would. We are aided in this case, however, by the fact that the SC filter sampling rate is many times greater than the bandedge

of interest. Recall from Section 2.1 that the SC filter input sampling rate is $2f_{scf} = 100f_c$, where f_c is the SC filter bandedge. This implies that frequencies within the band from $99f_c$ to $101f_c$, if present at the input to the SC filter, will be folded into the passband.

In order to prevent aliasing by the SC filter, it is preceded by a third order, lowpass, active RC filter. The magnitude response of the RC filter must simultaneously satisfy two conflicting constraints. The first constraint is obvious from the preceding discussion. The RC filter must provide at least 72dB of loss at 99 times the SC filter bandedge frequency. The second constraint is that the RC filter must have less than 0.05dB of *droop* at a the SC filter bandedge frequency. This guarantees that the passband response of the cascaded RC filter and SC filter is dominated solely by the SC filter passband response.

Because these two constraints on the RC filter are widely separated in terms of frequency, this goal can be met with only a 3rd order lowpass filter. Let the 3dB frequency of the RC filter be defined as f_o (RCF) and the SC filter passband be defined as f_c as before. The RC filter has 0.05dB of *droop* at f_o (RCF)/4 and greater than 72dB of loss at $17.25 \cdot f_o$ (RCF). This relationship is true for all 8 programmable RC filter bandwidths.

If an SC filter with a bandedge $f_c = f_o$ (RCF)/4 is used, the first constraint is met exactly. The second constraint is met with room to spare since the RC filter loss at $99f_c = 99f_o$ (RCF)/4 = $24.5f_o$ (RCF) is greater than 72dB. (Recall that the RC filter loss is greater than 72dB for frequencies greater than $17.25f_o$ (RCF).

In fact, this implies that the same RC filter bandwidth setting can be used with an SC filter whose bandwidth is $f_c = 0.7 f_o$ (RCF)/4. For this second case, the first constraint is met with room to spare. The second constraint, however, is met exactly since the loss at $99 f_c = (99)(0.7) f_o$ (SCF)/4 = $17.3f_o$ (SCF) equals 72dB.

This ability of a single RC filter bandwidth to accommodate a range of SC filter bandwidths (and still guarantee that any aliases are greater than 72dB down from full scale) is illustrated in Figure 5.2. Indeed, the available bandwidths that can be programmed into the RC filter (Table 3.1) allow for a continuous range of SC filter bandwidths ranging from 1.225kHz to 20kHz. Table 5.1 lists the possible range of SC filter bandwidths that can be used with the 8 programmable RC filter bandwidths and still insure full anti-aliasing protection.

The condition is somewhat more complicated when the user desires an SC filter bandwidth that is less than 1.225kHz. In this case, the anti-aliasing protection provided by the RC filter will be less than 72dB. Figure

RC Filter 3dB Bandwidth	Range of SC Filter Bandwidths		
80kHz	14kHz	to	20kHz
56kHz	10kHz	to	14kHz
40kHz	7kHz	to	10kHz
28kHz	5kHz	to	7kHz
20kHz	3.5kHz	to	5kHz
14kHz	2.5kHz	to	3.5kHz
10kHz	1.75kHz	to	2.5kHz
7kHz	1.225kHz	to	1.75kHz

TABLE 5.1

$$RCF \text{ LOSS} = 20 \log \sqrt{(1+x^2)(1.10803x^2 + (1-x^2)^2)}$$

where $x=f/f_0$ (RCF), f is the frequency, and f_0 (RCF) is the 3dB frequency of the RC filter.

Consider an example where the SC filter bandwidth is 312.5Hz. This can be achieved with a master clock frequency of 4MHz and $D0=D1=D2=1$. Table 5.2 lists the RC filter loss, the SC filter loss, and the combined RC + SC filter loss, at the critical aliasing frequencies. The RC filter bandwidth is set to 7kHz. The numbers in the RCF Loss column were found by using the formula given above.

In this example, the user will have to worry about full scale, out of band signals in a $\pm f_c$ band about $50f_c$, $100f_c$, $200f_c$, and $300f_c$. In practice, full scale out of band components do not occur due to the natural bandlimiting of the physical phenomena being measured. Any additional bandlimiting due to signal characteristics will help in preventing aliasing.

5.3 illustrates the frequency bands that can be aliased into the passband by the SC filter. One set of bands occurs at $m50 f_c \pm f_c$ where m is an even integer. Therefore, these bands occur at $(99f_c \text{ to } 101f_c)$, $(199f_c \text{ to } 201f_c)$, $(299f_c \text{ to } 301f_c)$, etc. Aliases in these bands are folded back with no attenuation from the SC filter.

Another set of frequency bands occurs at $n50f_c \pm f_c$ where n is an odd integer. Therefore, these bands occur at $(49f_c \text{ to } 51f_c)$, $(149f_c \text{ to } 151f_c)$, $(249f_c \text{ to } 251f_c)$, etc. Aliases in these bands, however, are folded back with 30dB of attenuation.

The aliasing protection provided by the RC filter with respect to the even aliasing bands is equal to the loss of the RC filter alone at those frequencies. The aliasing protection provided by the RC filter with respect to the odd aliasing bands is equal to the loss provided by the RC filter at those frequencies plus 30dB. In order to calculate the loss of the RC filter at any frequency, the following equation can be used:

Aliasing Frequency	RCF Loss	SCF Loss	Total Loss
49fc = 15.313kHz	20.5dB	30.0dB	50.5dB
99fc = 30.938kHz	38.8dB	0.0dB	38.8dB
149fc = 46.563kHz	49.4dB	30.0dB	79.4dB
199fc = 62.188kHz	56.9dB	0.0dB	56.9dB
249fc = 77.813kHz	62.8dB	30.0dB	92.8dB
299fc = 93.438kHz	67.5dB	0.0dB	67.5dB
349fc = 109.063kHz	71.6dB	30.0dB	101.6dB
399fc = 124.688kHz	75.0dB	0.0dB	75.0dB

TABLE 5.2

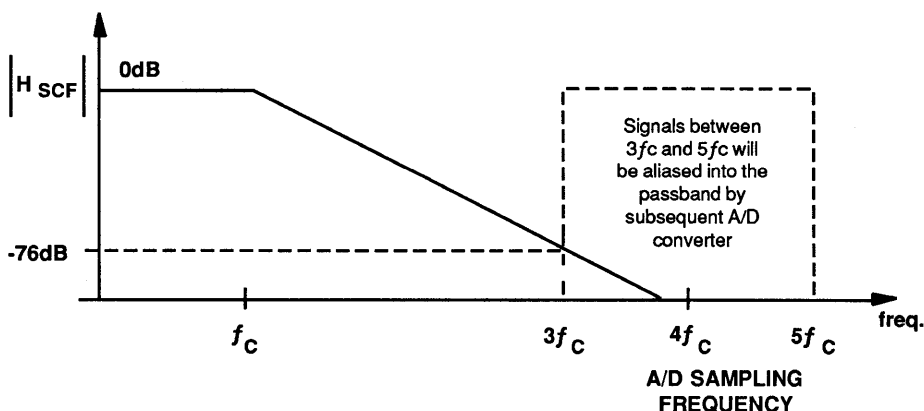


Figure 5.1 SC Filter Bandedge Loss

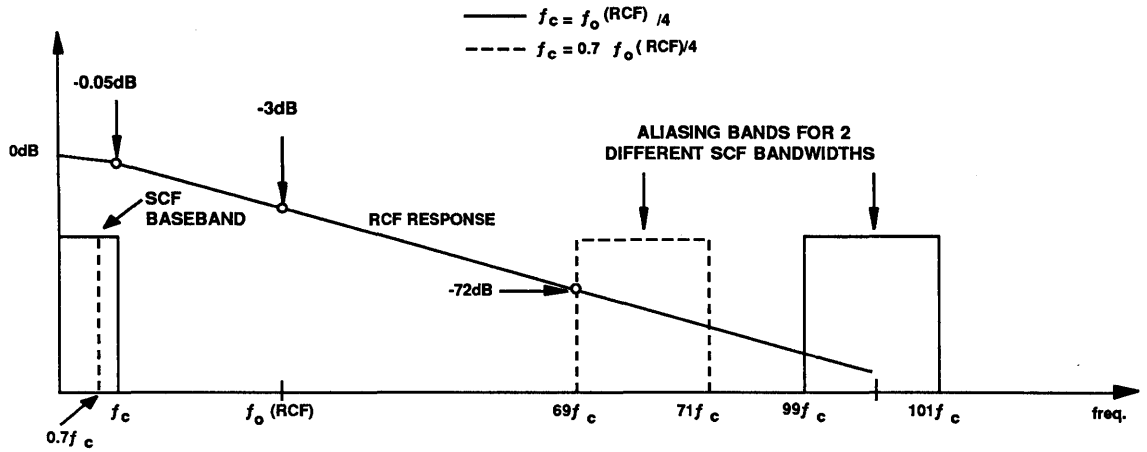


Figure 5.2 Alias Dampening from RC Filter

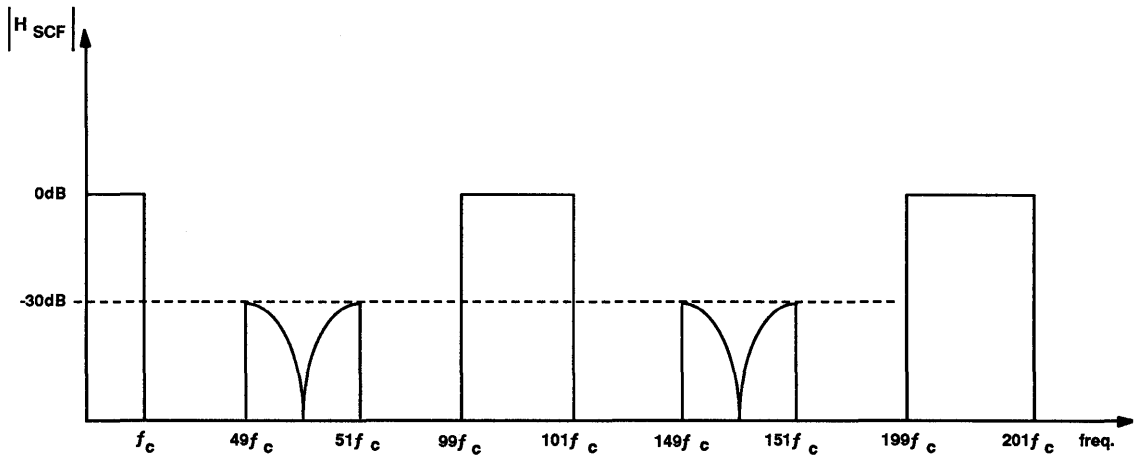


Figure 5.3 Frequency Bands Aliased into Passbands

USING ECL DACs WITH TTL LOGIC

by Tom DeLurio and Russ Moen

High speed Digital-to-Analog converters are primarily designed to perform in 10K or 100K ECL systems because of the inherent speed and low noise that is characteristic of this logic group. Unfortunately, a large number of designers, are either using high speed TTL logic with the DAC or are stuck in a +5V only environment and using pseudo ECL levels. This Application Brief will address these issues and offer solutions to overcome the perceived incompatibility between -5.2V operation and +5V operation.

Although the majority of Honeywell Signal processing Technologies' High speed DACs are optimized for ECL input levels, TTL levels can be utilized by pulling up the input pins to +5V. Additionally, the Vcc or Ground pins must also be pulled up to +5V and the Vee pins are tied to ground. And, by adding optional input voltage divider resistors, decreased noise can be realized by attenuating switching levels.

In a pseudo ECL system where the preceding DAC logic or memory is ECL but is pulled up to +5V, all that needs to be done is to pull the DAC up to the same level by shifting the ground or Vcc and Vee pins. Also, in most cases, analog output level shifting is required to bring the output down to ground potential. This is not necessary if driving an AC coupled load.

Honeywell SPT makes a variety of different ECL compatible DACs which have different types of output structures, but similar inputs. Therefore, if needed, all the circuits will have the same input level shifting but different output circuits.

The first device, the HDAC97000, is an 8-bit Video DAC that operates at 200MWPS. It has an 800Ω output source resistor and standard ECL input pins. The circuit in Figure 1 shows how to attenuate and pull up the input and video control pins for TTL levels using resistors R1 and R2. R1 is for input attenuation and R2 is the pull-up resistor for each input and control pin. The associated gain setting, setup, and glitch adjust function inputs are the same as before but just shifted up to accommodate a +5V environment. The analog output is then level shifted down to ground and resistor values are determined by the following equations:

Gain Setting

$$R_{01} = \frac{(V-V_1)R_L}{V_{3\text{ MAX}}} \quad \text{Where } R_L = R_{L1} \parallel R_{L2}$$

Where $V_{3\text{ MAX}}$ = Maximum output voltage.

$$R_{\text{SET}} = K(3^{63/64})R_{01}$$

Where $K = 160/90$ for 20IRE Setup

$$= 150/90 \text{ for 10IRE}$$

$$= 147.5/90 \text{ for 7.5IRE}$$

$$= 140/90 \text{ for 0IRE}$$

$$\frac{V_1 - V_{\text{be}}(Q_1)}{1/2 I_{\text{DAC MAX}}} \leq R_{02} \leq \frac{V_1 - V_{\text{be}}(Q_1)}{\frac{V - V_1}{10R_{01}}}$$

Example

For

$V_3 = 0$ to $+1.071\text{V}$ (0 to 150IRE), $1/2 I_{\text{DAC MAX}} \cong 18\text{mA}$,
Blank = 10IRE, $V_1 = 3.77\text{V} \cong V_2$, $R_L = 37.5\Omega$

$$R_{01} = \frac{(5\text{V} - 3.77\text{V}) 37.5}{1.071\text{V}} = 43\Omega, 1/8\text{W}$$

$$R_{\text{SET}} = 150/90 (3^{63/64}) 43\Omega = 212\Omega, 1/8\text{W}$$

DAC Midscale $\cong 18\text{mA}$

$$R_{02} \geq \frac{3.77\text{V} - .75\text{V}(Q_1 V_{\text{be}})}{18\text{mA}} \geq 168\Omega, 1/8\text{W}$$

$$R_{02} \leq \frac{3.77\text{V} - .75\text{V}}{\frac{5 - 3.77}{10(43)}} \leq 1,056\Omega, 1/8\text{W}$$

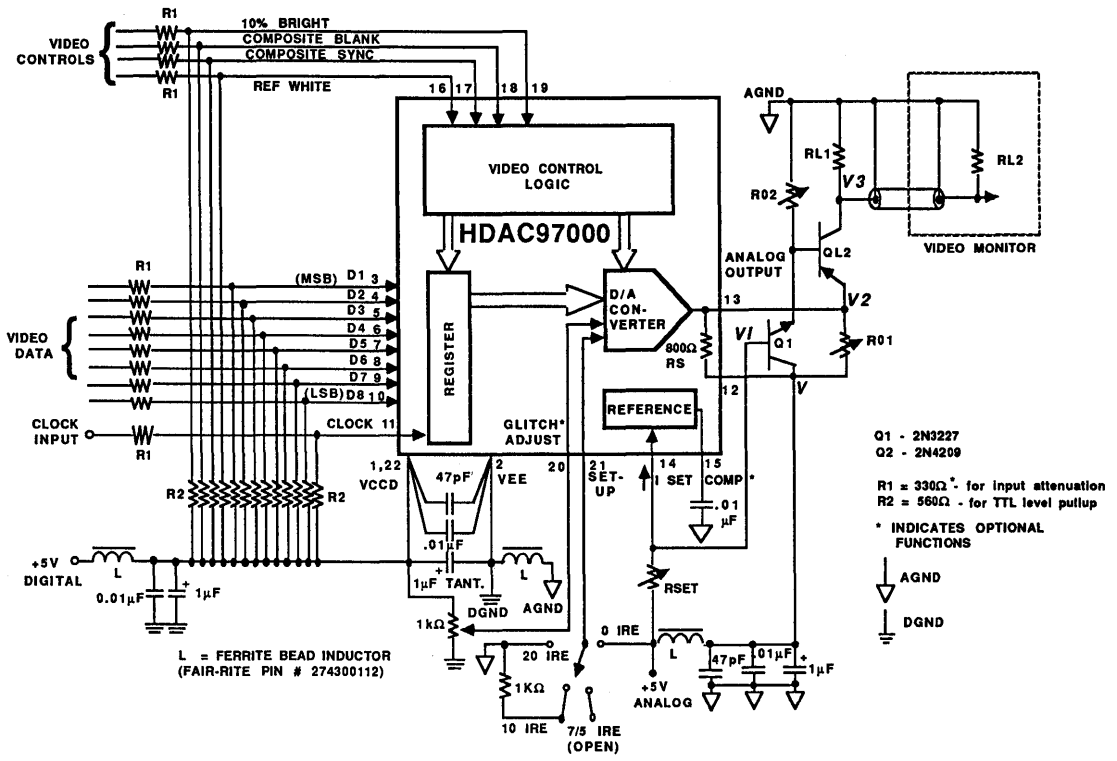
A practical method for setting up the circuit is as follows:

1. With $I_{\text{DAC out}} = 0\text{mA}$, adjust R_{01} for desired full scale voltage at V_3 .
2. $I_{\text{DAC out}} = I_{\text{MAX}}$, adjust R_{SET} for desired minimum voltage at V_3 .
3. $I_{\text{DAC out}} = 1/2$ Gray Scale, adjust R_{02} for $V_1 = V_2$.
(Readjust R_{01} and R_{SET} in steps 1 and 2)

It is important that all +5V supplies be adequately bypassed as shown in Figure 1 for input, output and power pins.

FIGURE 1 - HDAC97000 IN A TTL ENVIRONMENT.

AB100



The next devices are 8-bit High speed DACs that operate from 165, 275, and up to 400MWPS. They are respectively the HDAC10180, HDAC10181, and the HDAC51400. Each part has the same output current structures but have different voltage reference configurations. The HDAC10180 does not have an internal voltage reference and needs an external reference as shown in Figure 2. If two or more DACs are used as in an RGB monitor application, the HDAC10180s can use the reference from one HDAC10181. The HDAC51400 has a reference on board but has a separate reference out pin, whereas the HDAC10181 shares its' reference out with the reference input pin.

There are numerous ways to level shift the output from these devices to ground reference, but the circuit in Figure 2 takes advantage of the differential current output pins (OUT+ and OUT-). The equations for choosing resistor values are as follows:

For the LM113 or HDAC10181/51400 Reference Voltage
 $V_+ = +1.2V$

$$I_{SET} = \frac{V_+}{(\infty T) R_1 + R_2} \quad \infty T \text{ is the number of turns on potentiometer } R_1.$$

$$R_L = R_3 \parallel R_4$$

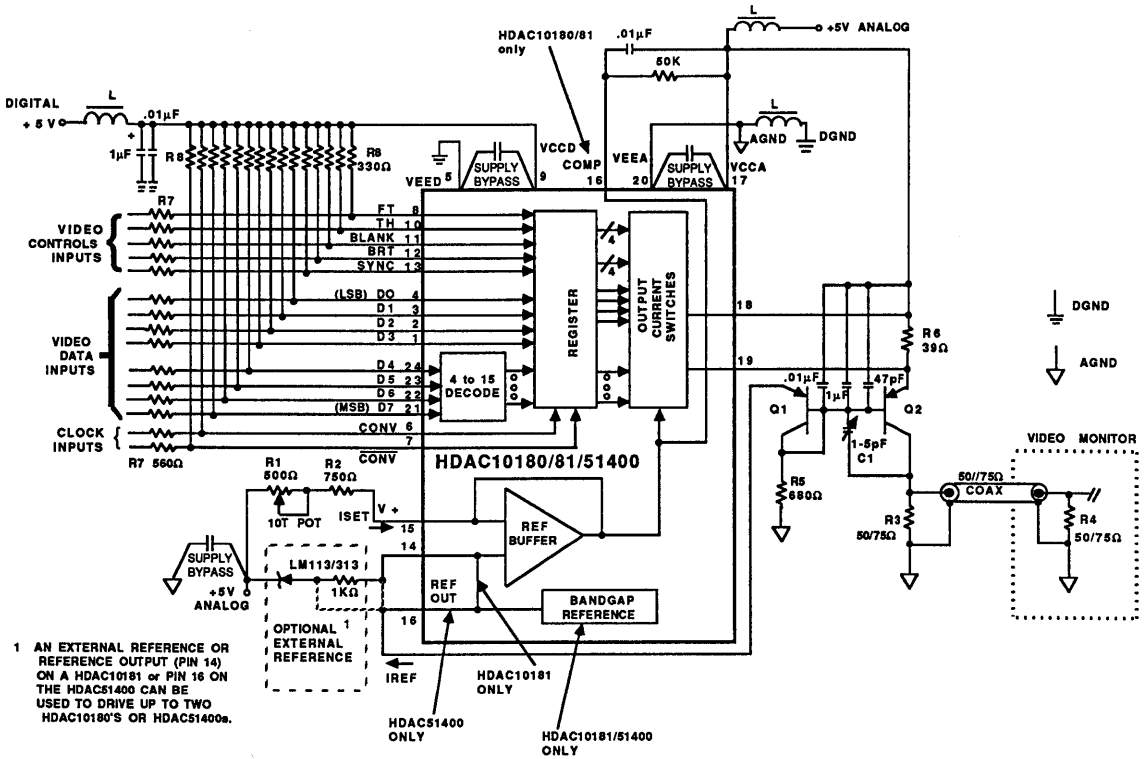
$$I_C = \left(\frac{1.2 + (V_{be1} - V_{be2})}{R_6} \right) \cdot \frac{V_{OUT}}{R_L} \quad \text{The current in } Q_2$$

$$V_{out} (F.S.) = 15.9375 (I_{SET}) R_L + 7.5IRE$$

Where Full Scale = 650mV and 7.5IRE ≈ 54mV.

7.5IRE is the monitor dc setup level and is standard on the HDAC10180/81/51400 Video DAC series.

FIGURE 2 - HDAC10180/81 AND HDAC51400 IN A TTL ENVIRONMENT.



Q1 = Q2 = 2N4209 for HDAC10180/81B
 Q1 = Q2 = 2N5583 for HDAC10180/81A
 Q1 = Q2 = 2N5583 for HDAC51400

NOTES:

EXTERNAL SYNC CIRCUIT FOR VIDEO DACs

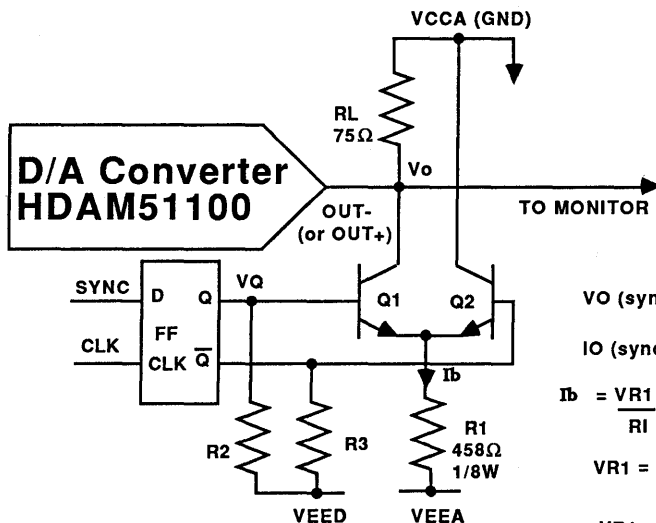
by Tom DeLurio and Russ Moen

High speed Digital-to-Analog converters and multifunction DACs with memory or multiplexers do not always have on board video SYNC pulse control inputs. This Application Brief will offer solutions to overcome the absence of video sync control pins. If needed, the circuits can equally be used for blank or 10% bright funtions as well.

Although the majority of Honeywell Signal processing Technologies' High speed DACs have video sync control inputs, some do not. Since most of SPTs DAC products are current output type devices, the sync pulse can be added directly to the output pins. One option is shown in Figure 1 using the HDAM51100 DAC with memory. This device does not have on-board sync control.

The sync pulse level is generated using an ECL type flip-flop that is clocked in phase with the DAC clock to drive a matched transistor pair. Three flip-flops can be used in series to match the clock latency of the HDAM51100 or the time can be compensated for in software.

Another option is shown in Figure 2. Here, the sync circuit takes advantage of the voltage reference available from the DACs reference output pins. This circuit is more accurate and stable than the previous one but uses more components.



$$V_O (\text{sync}) = -286 \text{ mV}$$

$$I_O (\text{sync}) = \frac{-286\text{mV}}{37.5} = 7.63 \text{ mA}$$

$$I_b = \frac{V_{R1}}{R1}$$

$$V_{R1} = V_{EEA} - V_{be1} - V_Q ("1")$$

$$V_{R1} \approx 5.2\text{V} - .83 - .875 = 3.5\text{V}$$

$$R1 \approx \frac{3.5 \text{ V}}{7.63 \text{ mA}} = 458 \Omega$$

- Q1,Q2 = Motorola MD918
- R2, R3 = ECL loads for Flip-Flop.
- R1, RL same resistor type if possible
- FF Requires three to match HDAM51100 part latency or compensate in software. Other DACs will vary (see data sheet).

FIGURE 1 - Video DACs with external SYNC control.

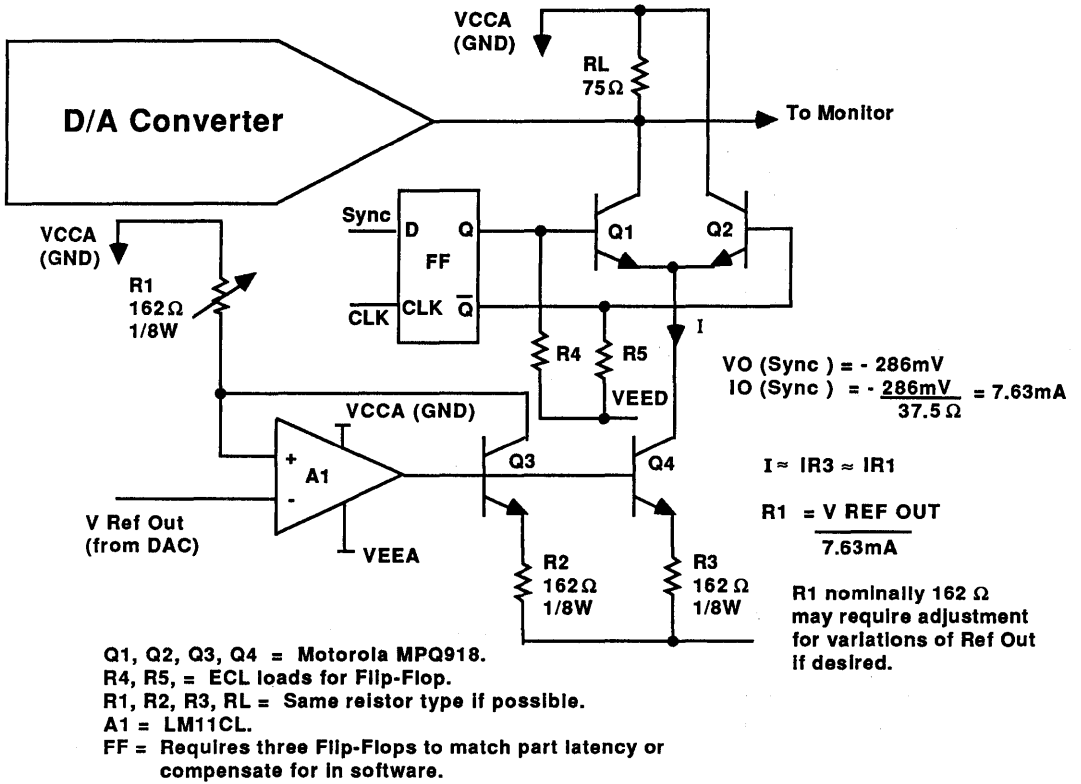


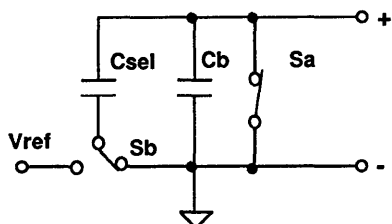
FIGURE 2 - Video DACs with external SYNC control using Internal voltage reference.

CHARGE SCALING DATA CONVERTERS

PAUL M. BROWN

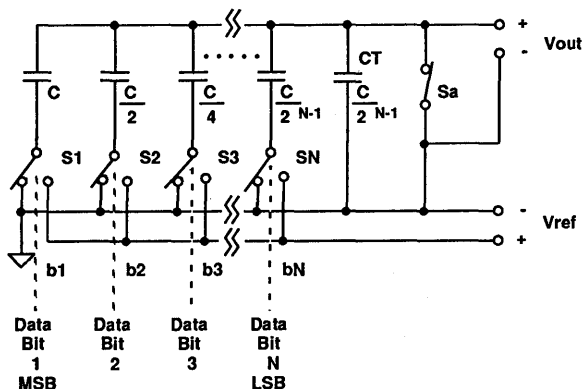
High quality polysilicon MOS capacitors, inherent in Honeywell's CMOS process, have made it possible to replace the traditional data conversion technique of current scaling with charge scaling. This technique relies on carefully matched capacitors instead of matched resistors and current sources to accomplish digital to analog conversion. The advantages of this approach include ease of manufacture, low power consumption and an inherent sample-and-hold function that substantially improves analog-to-digital converter performance yet adds no extra components. This application brief will discuss the basic charge scaling DAC (digital-to-analog converter), how it functions and how it is used in The HADC574Z and the HADC674Z to achieve the "built in" sample-and-hold function.

Figure 1. Simple Capacitive Divider



$$V_{out} = V_{ref} \frac{C_{sel}}{C_b + C_{sel}}$$

Figure 2. Capacitor DAC



Charge scaling DAC's produce an analog output voltage by distributing charge in an array of binary weighted capacitors. The weighting of the capacitive divider is determined by the incoming digital code. Figure 1 illustrates a basic capacitive divider circuit. This circuit functions in two steps. In step 1, switch Sa is closed and switch Sb is connected to ground, discharging both Csel and Cb. In step 2, Sa is opened and Sb is connected to the reference voltage Vref. Due to the relative values of Cb and Csel and the charge distribution between them, Vref is divided between the two capacitors such that $V_{out} = V_{ref} \times C_{sel}/(C_b + C_{sel})$.

Figure 2 illustrates how a capacitive DAC is implemented using the above approach. Csel is the sum of all capacitors selected by the data bits to be connected to Vref and Cb is the balance of all other capacitors, including the termination capacitance, that remain connected to ground.

The total DAC capacitance, $C_{tot} = C + C/2 + C/4 + C/8 + \dots + C/2^{N-1} + C/2^{N-1} = 2C$

$$C_{tot} = C_{sel} + C_b$$

The total selected capacitance, $C_{sel} = b_1C + b_2C/2 = b_3C/4 + \dots + b_NC/2^{N-1}$ (where $b_1 \dots b_N = 1$ or 0)

$$V_{out} = V_{ref} \times C_{sel}/C_{tot}$$

The HADC574Z/674Z use the DAC in a slightly different manner (see figure 3). The DAC output is connected to one input of a comparator and a reference voltage is applied to the other comparator input. The conversion cycle begins with a "reset". The DAC is first "zeroed" to the analog input voltage with switch S1 closed. Next, S1 opens and the SAR (successive approximation register), under control of the comparator, sets the appropriate data bits to either Vref or ground to balance the comparator inputs. The significance of this is that the input voltage is sampled only during the "reset" period. Although there is no sample-and-hold circuit in the classical sense, the sampling nature of the capacitive DAC makes the HADC574Z/674Z appear to have a built in sample-and-hold.

This sample-and-hold action substantially increases the signal bandwidth of the HADC574Z/674Z over that of similar competing devices.

EXAMPLE:

Assuming a sinusoidal signal, maximum slew rate, $Sr = 2\pi f Vp$ (Vp = peak voltage)

For an N-bit converter to maintain +/- 1/2 LSB accuracy :

$Verr \leq Vfs/2^{N+1}$ (where $Verr$ is the allowable error voltage and Vfs is the full scale voltage)

$Sr = \Delta V / \Delta T = 2\pi f Vp$

Let $\Delta V = Verr$, $Vp = Vin/2$ and ΔT = The time during which unwanted voltage changes can occur on the input signal.

This can be rewritten as:

$Vfs/2^{N+1} \geq \pi f Vin \Delta T$

or

$f_{max} \leq Vfs / (\pi Vin \Delta T) 2^{N+1}$

Let $Vfs = Vin = 20V$

AD574

ΔT = conversion time = 25 μ s typical

$f_{max} \leq 20V / [\pi(20V)(25\mu s)(2^{13})] = 1.55Hz$

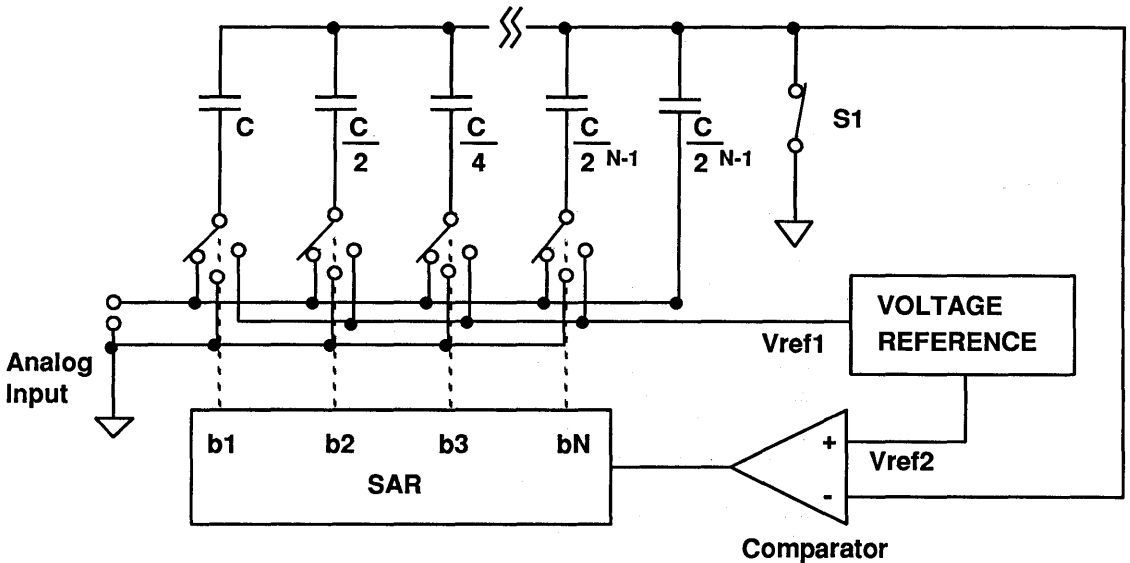
HADC574Z

ΔT = 20 ns typical (specified aperture uncertainty time)

$f_{max} \leq 20V / [\pi(20V)(20 ns)(2^{13})] = 1.94kHz$

The HADC574Z has over a 1250:1 improvement in analog bandwidth with NO ADDITIONAL COMPONENTS!

Figure 3. HDAC574/675 DAC Configuration



HADC574Z AND HADC674Z ANALOG INPUT STRUCTURE

Craig Wiley

The capacitive DAC circuitry in the HADC574/674Z provides lower power dissipation, improved accuracy, and an inherent sample/hold function as compared to the traditional R-2R ladder DAC approach used in similar devices. In many applications this inherent sample/hold function can eliminate the need for an external sample/hold amplifier and provide superior performance. Additionally, it reduces the dependence on signal source characteristics during conversion eliminating the need for signal buffering. The sample/hold function of the HADC574/674Z can reduce the external circuitry requirements of data acquisition systems when used properly. This application brief will discuss the application, advantages and limitations of the HADC574/674Z analog input structure.

CONVERSION EVENTS

Operation of the HADC574/674Z can be broken into two basic events. The first event is referred to as the sample period and begins upon an initiation of conversion. During the sample period a capacitor array within the device is connected to the analog input and is allowed to charge to the external signal voltage. The second event, longer by comparison, is the successive-approximation operation utilizing the CDAC. During the conversion period, the internal sample capacitance is switched from the input to the internal CDAC circuitry. As shown in the simplified circuit equivalent of Figure 1, SW1 is used to transfer the capacitance C_s from the input to the CDAC circuitry. Actually, SW1 consists of several parallel MOSFET switches and C_s is a capacitor array that performs the CDAC function. Please refer to application brief AB102 for more information on charge scaling data converters.

Conversion event timing of the HADC574/674Z devices is determined by an internal clock. By virtue of the differences between internal clock frequency, the HADC674Z exhibits a shorter total conversion time compared to the HADC574Z. This also results in a different sample period between the two devices which requires application considerations. Figure 2 shows the conversion event timing (minimum-maximum values) of both devices. For additional timing information please refer to the device data sheet.

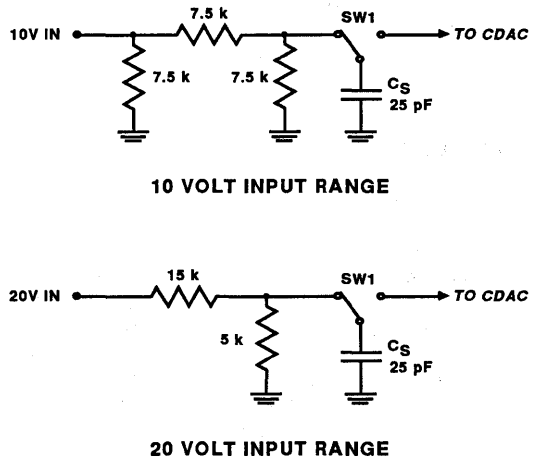
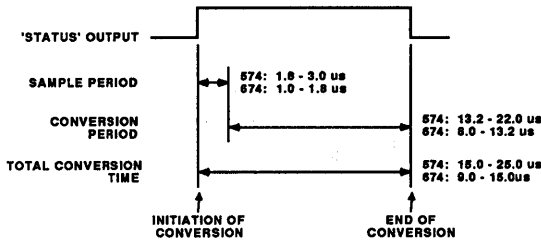


FIGURE 1
SIMPLIFIED INPUT CIRCUIT
OF HADC574/674Z
Typical values shown

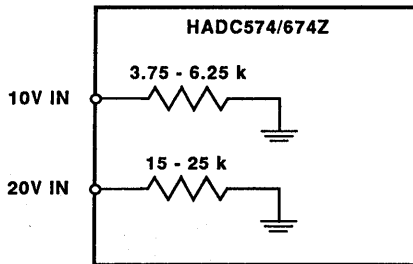
Compared to similar devices, the HADC574/674Z places less demand on the signal source stability and output characteristics. In the similar devices, the R-2R DAC is connected to the external signal source during the successive-approximation conversion operation. During the conversion, the signal source must remain stable to within a tolerable bit accuracy. Low output impedance and close proximity of the source are normally necessary to allow quick response to the changing DAC load. These requirements are normally met with a sample/hold or buffer amp. When using the HADC574/674Z's, however, direct connection can frequently be made to the voltage source without performance degradation.



**FIGURE 2
CONVERSION EVENT TIMING
OF HADC574/674Z**

DC INPUT CHARACTERISTICS

The internal input scaling resistors in the HADC574/674Z have different impedance characteristics for the 10V IN and 20V IN analog input pins. The input resistance range of these pins is shown in Figure 3. When using a high signal source impedance, the attenuation caused by the internal input resistance must be considered. For example, a signal source with an output resistance of 5 kΩ driving the 10V IN pin, which has a 5 kΩ typical input resistance, would appear to have only half the signal value. Some of this error can be compensated by the external trim network (see data sheet), but drift can result due to thermal coefficient differences between the external and internal resistances. It is therefore important to keep the source impedance as low as possible.



**FIGURE 3
DC INPUT CHARACTERISTICS
OF HADC574/674Z**

DYNAMIC INPUT CHARACTERISTICS

Input Settling

Although the sample/hold function of the HAC574/674Z provides utility, dynamically it is of modest performance when compared to dedicated sample/hold amplifiers. It can, however, provide superior noise immunity when sampling lower frequencies (below 5 kHz).

Figure 4 shows the electrical equivalent of the internal sample circuitry as it appears to Cs. The equivalent resistance using either input pin (10V IN or 20V IN) is equal, assuming zero source resistance. Figure 4 provides a usable first order approximation and ignores all other parasitic effects. The 4 kΩ resistance includes the resistance of SW1; in applications with high source resistance, source resistance effects should also be included. Charge resistance can be calculated from the circuits of Figure 1.

In Figure 4, the voltage across Cs over time is defined by:

$$\frac{e_c}{E} = 1 - e^{-t/RC} \quad (\text{equation 1})$$

where: e_c = Voltage of Cs; E = Signal Voltage;
t = time; R,C = Component Values of Figure 4.

To express Equation 1 in terms of time (t) to obtain a required charge voltage (e_c), we can rewrite equation 1 as:

$$t = -RC \ln \left(1 - \frac{e_c}{E} \right) \quad (\text{equation 2})$$

The design of a data acquisition system using the HADC574/674Z must take into account the total system settling time and the effect upon e_c , the captured signal voltage sample. The desired settling value of e_c must occur within the sample period of the device. Using equation 1, a full-scale step input will settle to within 1/2 LSB of final value in 0.9 μs. (For this calculation, $(e_c/E) = (4095.5/4096)$). Using equation 2, the final value is within 1/5 LSB after 1 μs. Therefore, even when using the HADC674Z which has minimum sample period of 1 μs, the pole introduced by the internal charge circuit is negligible.

Because this dynamically-limited sample/hold amplifier acts like a low-pass filter, it exhibits good noise immunity. An external sample/hold will usually be more susceptible to circuit noise. Even with an external sample/hold amplifier, the HADC574/674Z typically exhibits less input noise than similar 574/674 devices. Room temperature characterization shows that typical equivalent input noise of the HADC574/674Z is 1/5 LSB or 50 μV.

Dynamic Sampling Error

The bandwidth limitations of the HADC574/674Z's sample/hold feature are more apparent when performing dynamic sampling, that is, sampling of an active signal. For an AC signal voltage, the circuit of Figure 4 is low pass, phase-lag network. The transfer function of Figure 4 can be expressed as:

$$e_c = \frac{E}{1 + jwRC} \quad (\text{Equation 3})$$

where: $w = 2\pi f$

The sample circuit equivalent, shown in Figure 4, can be viewed as a single-pole low-pass filter with a half power point at 1.6 MHz. Using equation 3, the 1/2 LSB magnitude attenuation of a full scale signal occurs at 25 kHz. At 10 kHz, the attenuation is only 0.08 LSB. As discussed in the following section, since 5 kHz is about the maximum usable range, the low-pass magnitude degradation imposes insignificant error.

Phase distortion in the input network is an important error to consider in dynamic sampling applications. As signal frequency goes up, higher reactance of the sample capacitor causes an increase in phase shift. Thus, a sampled waveform at one frequency appears to be delayed in time relative to a lower frequency. Phase shifting between frequencies is illustrated in Figure 5. Using equation 3 above, it can be determined that a full-scale sinusoidal signal is allowed a maximum frequency of 195 Hz if an amplitude error of 1/2 LSB (ΔV) maximum is allowed considering the phase shift in the time domain (Δt). Most analog data, however, is in the form of a complex waveform which consists of several fundamental frequencies. Sampling of a complex waveform with excessively high frequency components will result in a distorted digital representation.

Non-Apparent Dynamic Factors

Present architecture of the HADC574/674Z results in an inherent input slew rate limitation during the sample period described earlier. Slew rate adversely affects the switches composing SW1 in Figure 1. Problems will generally be found with slew rates above 0.25 V/ μ s into the 10V IN pin or 0.5 V/ μ s into the 20V IN pin. This corresponds to full-scale sinusoidal signal of 8 kHz into either pin. To avoid problems over all operating conditions, the maximum slew rate should be conservatively limited to 0.16 μ V/s into 10V IN or 0.32 μ V/s onto 20V IN. This places the conservative input frequency limit at 5

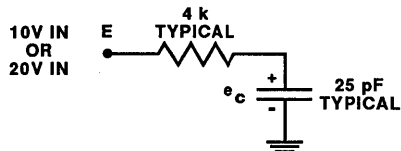


FIGURE 4
EQUIVALENT DYNAMIC CIRCUIT
OF HADC574/674Z

kHz for a full-scale sinusoidal signal. Exceeding the slew rate limitation during the sample period will result in an all "1" output for a positive-going input and an all "0" output for a negative-going input.

As described in the HADC574Z and HADC674Z data sheets, aperture jitter also places a limitation on the maximum usable input frequency. The specified 20 ns typical aperture jitter accounts for worst case changes in ambient temperature and power supply voltages. In application, however, sample-to-sample jitter typically less than 5 ns. Discrete-Fourier-transform (DFT) characterization of the HADC574Z has shown that the wide-bandwidth signal-to-noise ratio is approximately 72 dB down from the fundamental when using full-scale single-tone sinusoidal test signals up to 8 kHz. Above this frequency, the slew rate limitation described above greatly degrades the performance. Both the minimum aperture jitter and excellent linearity typically found with the HADC574/674Z provide a low dynamic distortion level which approaches ideal performance limited by 12-bit quantization error alone.

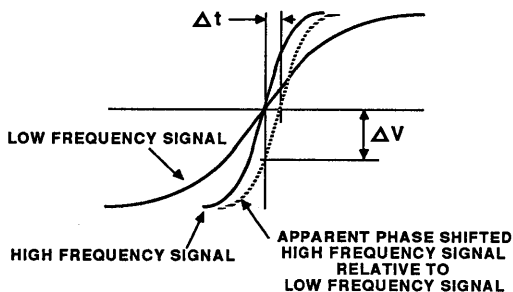


FIGURE 5
EFFECTS OF PHASE DISTORTION
THROUGH INPUT NETWORK

CONCLUSION

The analog input structure of the HADC574/674Z provides superior performance to that of similar 574/674 devices. In addition, the inherent sample/hold function can eliminate the need of an external sample/hold or buffer amplifier. Because of its dynamic limitations, use of the internal sample/hold function is limited to lower-frequency (< 5 kHz) data-acquisition applications. Systems requiring temporal (phase) accuracy during dynamic sampling or that will sample signals over 5 kHz should use an external sample/hold amplifier.

TESTING THE HADC574Z AND HADC674Z ON THE LTS2020

Craig Wiley

Minor modifications of test hardware and software are needed in order to successfully test the Honeywell SPT HADC574Z or HADC674Z devices on the LTS2020 tester. The LTS2020 is a low-cost integrated circuit test system built by Analog Devices Incorporated and is commonly used as an Incoming Inspection test station. The HADC574/674Z devices offer enhanced performance but have slight differences in test requirements compared to 574/674 devices available from other manufacturers. Hardware modifications required for the HADC574/674Z will not effect the testing of similar pin-compatible devices.

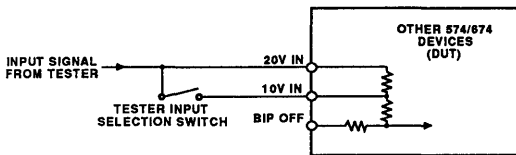


FIGURE 1

LTS2020 INPUT RANGE SWITCHING TECHNIQUE

Input structure of device shown is of 574/674 devices

This modification on the LTS0620 socket adapter involves changing relay K2 and making the appropriate wiring modifications. Using the LTS0620 schematic nomenclature, Figure 3 shows the board, as-is, and Figure 4 shows the modified version. For relay K2, a Coto 2211-05 is used to replace the existing Coto 2900-0017. The modification will provide a suitable range switching technique for the HADC574/674Z as well as all pin-compatible 574/674 devices. No software changes are required for this modification.

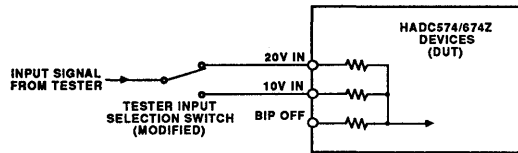


FIGURE 2

MODIFIED LTS2020 INPUT RANGE SWITCHING TECHNIQUE

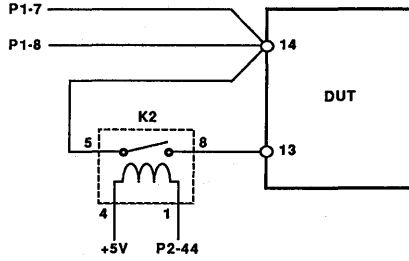
Input structure of device shown is of HADC574/674Z

HARDWARE MODIFICATION

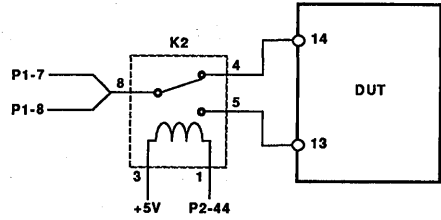
The hardware modification involves a minor change to the LTS0620 socket adapter which fits into the LTS2200-ADC family board. The socket adapter, as-is, takes advantage of the input structure common to 574/674 devices by other manufacturers. A single-pole relay is used to switch between to 20V IN and 10V IN pins of the device. This relay configuration is illustrated in Figure 1. The HADC574/674Z devices, due to the more accurate input architecture, will not function properly with this simplified switching scheme and instead requires a double pole relay as shown in Figure 2.

SOFTWARE MODIFICATIONS

Testing of HADC574/674Z devices require some software changes since the LTS2020 574/674 test software is written for the similar bipolar devices. First, since HADC574/674Z devices use the BEMOS process, the limits for the power supply current tests need to be lowered. Second, since HADC574/674Z devices do not use a -15 Volt supply (VEE pin is not internally connected) the -15 Volt tests need to be bypassed. And last, because of the internal sample/hold function, the ratio between the 8-bit and 12-bit conversion times differs from similar 574/674 devices (although they still comply with the specifications).



**FIGURE 3
UNMODIFIED LTS0620 WIRING AS
REPRESENTED BY FIGURE 1**



**FIGURE 4
MODIFIED LTS0620 WIRING AS
REPRESENTED BY FIGURE 2**

The test programs available for the LTS2020 tester are the AD574_HG for testing 574 devices and the AD674_HG for testing 674 devices. The modifications of these programs for successful testing of the HADC574Z and HADC674Z devices are listed below. These modified test programs will not be suitable for testing similar 574/674 devices and should therefore be given new names avoid confusion.

AD574_HG and AD674_HG Test Program Changes:

- 1) Line 310, change LL (Lower Limit) to -0.1 and UL (Upper Limit) to +3 (mA)
- 2) Line 340, change LL to 0 and UL to 10 (mA)
- 3) Add line 355 "GOTO 380"
- 4) Line 86, change "E" conversion factor to 0.75.
- 5) Add line 1005 "GOTO 1060".

(Comments:)

(New +5 Volt supply current limits)

(New +15 Volt supply current limits)

(Skips -15 Volt supply test since this pin is unconnected)

(New 8-bit conversion time limit)

(Skips -15 Volt pin PSSR test)

GLITCH ENERGY IN HIGH SPEED D/A CONVERTERS

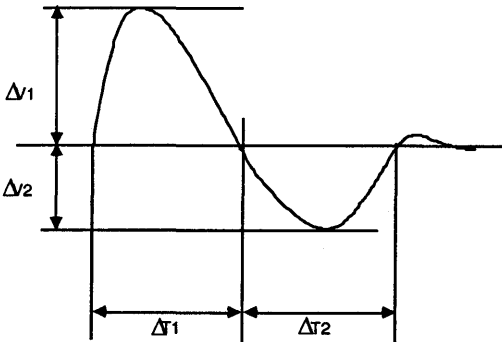
Tom DeLurlo, Senior Applications Engineer

INTRODUCTION

Glitch energy should be an important consideration when choosing a D/A converter. High speed or video D/A converters suffer from glitches and the associated output deviations much the same way as their slower speed counterparts. Fortunately, the same design that makes Honeywell SPT's high speed DACs so fast, gives them lower glitch energy than all other D/A converters. This application brief will explain how glitches manifest themselves in some applications, how to overcome these problems, and why Honeywell DACs have superior glitch performance.

GLITCH ENERGY

If a video DAC glitches while driving a raster scan video display, the resulting picture appears to have shaded lines a pixel or two wide along the entire vertical excursion of the tube and at regular intervals along the horizontal axis if the glitching is severe. In a vector stroke display, glitches can cause light or dark dots. In other applications, the glitches cause distortion, a higher noise level, and average level value inaccuracies. The worst case glitch usually occurs during a major code change such as 01111111 to 10000000 when the MSB changes state. Since this is only a 1LSB output level transition, a large transient caused by glitching can be disastrous.



$$\begin{aligned} \text{Glitch Energy +} &= \Delta V1 \text{mv} \times \Delta T1 \text{ns} = \text{GpV-s} \\ \text{Glitch Energy -} &= \Delta V2 \text{mv} \times \Delta T2 \text{ns} = \text{GpV-s} \\ \text{Glitch Energy} &= 1/2 \{ (\text{Glitch Energy +}) + (\text{Glitch Energy -}) \} \end{aligned}$$

Figure 1 - Glitch Energy impulse

A doublet type glitch is shown in Figure 1. Not all glitches are doublets, some are only negative spikes or only positive spikes. The glitch transient can be caused by a timing skew in the current switches. Or it can be caused by the DAC input data not being properly registered so that the data arrives at different times. The result, for example, is that the output may make an MSB level change before all the LSBs turn off. Therefore, the DAC output swings all the way toward maximum output and then back to the 10000000 level. Since this change is very fast, an impulse response results, and the DAC output transfer function in response to a full scale digital ramp will appear like Figure 2.

There are numerous ways to minimize the glitching by adding external circuitry to the DAC. These include a track-and-hold to track the output level of the DAC before the glitch appears, hold the level during the glitch, and then release for the next level. Another is to add variable capacitors to each digital input pin to skew the data flow so that all data arrives at the same time. Unfortunately, these methods are expensive and require fine tuning. The best solution is to use a DAC that is designed to minimize glitches. Honeywell SPT designed its' DACs with this in mind and consequently came up with the lowest glitch energy specifications in the industry!

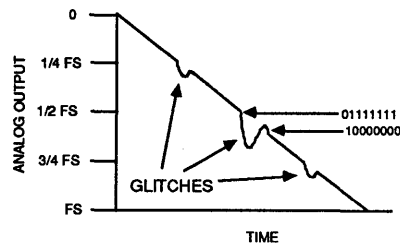


Figure 2 - Glitching DAC Transfer Function.

HONEYWELL DAC DESIGN

All of Honeywell SPTs high speed D/A converters use current switches to implement the DAC function and use a fully binary weighted approach (Figure 3) as opposed to the much more glitch prone R-2R ladder design.

In the HDAC97000 (see Table 1), the upper three bits are segmented with interdigitated current sources for good matching and linearity. Each data pin has latches for deskewing input data if the data arrives at different times. This technique prevents timing glitches from occurring at the output. In addition, a glitch adjust pin is available to

change the logic threshold in the DAC switches to skew the switching times (Figure 2). This control will provide better than data sheet specifications for glitch energy.

The HDAC10180/81 and the HDAC51100/200, HDAC51400, HDAC51600 series are segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches. The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

Table 1 - Honeywell Signal Processing Technologies' High Speed D/A Converters

PART NUMBER	DAC TYPE	CONVERSION RATE (MWPS)	GLITCH ENERGY (PICO-VOLT/SECOND)
HDAC34010	TRIPLE 4-BIT	200	4
HDAC34020	TRIPLE 4-BIT (TTL)	100	4
HDAC97000	8-BIT	200	35
HDAC10180	8-BIT	165/275	10
HDAC10181	8-BIT	165/275	10
HDAC51400	8-BIT	400	10
HDAC51100	8-BIT (512X8 MEMORY)	115	3
HDAC51200	8-BIT (512X8 MEMORY)	200	3
HDAC51600	8-BIT (5:1 MUX)	250	3

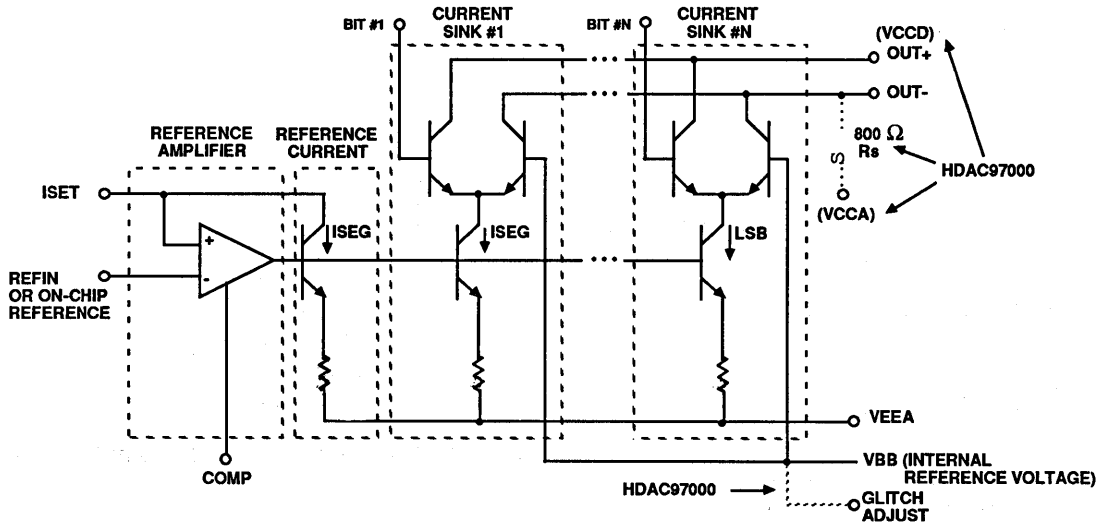


Figure 3 - Segmented D/A Converter Architecture.

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

Quality Assurance

Quality and reliability of electronic components are critical issues at Honeywell Signal Processing Technologies. Customers integrate large portions of their finished products into silicon using SPT's complex high performance integrated circuits. The quality and reliability of the end products therefore, depend heavily upon the integrated circuits they contain. Realizing the intimate relationship between its customers' success and its own, SPT has put into place a continually improving quality assurance system that makes its products among the highest quality and most reliable components available.

Quality and reliability, frequently thought to be synonymous, have quite different meanings. Quality implies that a device initially conforms to a given set of performance criteria. Reliability implies that a device continuously meets a given set of performance criteria. Figure 1 illustrates the traditional "Bathtub" Failure Rate Curve. A given sample of unscreened devices that initially meet their published specifications (high quality) will tend to have a relatively high initial failure rate (infant mortality) due to parameter drift or manufacturing defects that have gone undetected during the manufacturing process (low reliability). The failure rate during the "normal life" period is affected by devices with latent failure mechanisms that normally exhibit themselves during the infant mortality period and some devices that prematurely "wear out". Failure during the "wear out" period is caused by metal migration, long term drifts, corrosion and package failure. SPT insures the high quality of its product with rigorous 100% electrical testing. Product reliability is designed in and insured through comprehensive QA (Quality Assurance) monitoring throughout the manufacturing process and screening of the final product.

Screening operations are designed to "weed out" potential infant mortality failures before they are shipped to customers. The screening procedures that SPT uses are described below with the failure mechanisms they are designed to catch.

Pre-seal Visual

Wire bonding, die bonding, package, package leads and die are visually inspected using both a high and low power microscope. Many of the defects detectable during this inspection such as defective wire bonds, contamination, scratched metalization or other defects on the die contribute to infant mortality. This inspection is performed just prior to sealing the device.

Bond Strength

This simple test verifies the mechanical strength of the wire bond. Metalization and interconnection failures (typically opens or shorts) account for nearly half of IC failures.

Stabilization

The devices are heated to 150°C in an oven for 24 hours without electrical stress. This procedure is used as a preconditioning for subsequent testing.

Temperature Cycling

The devices are cooled to -55°C for 10 minutes then elevated to +150°C for 10 minutes with a 5 minute transfer time in-between. This procedure is carried out 10 times. Variations in physical dimensions of defective packages can cause loss of package integrity, cracking of passivation on the die, and changes in operating characteristics due to mechanical stress. This test is performed without electrical stress.

Constant Acceleration

The monolithic devices are subjected to 30,000 gs for 1 minute in the Y1 plane. This test is performed without electrical stress and can uncover mechanical weakness that was not detected by temperature cycling. Gold wire bonds are effectively tested for integrity in cavity packages (packages in which the bond wires are not encapsulated). The test is not as conclusive for aluminum wires (due to their lighter weight). Cracked die, weak die bonds, poor lid seals and improperly dressed bonding wires can also be detected during this test.

Hermetic Seal

Fine Leak
The units are placed in a helium filled vessel under 60 psig for at least 1 hour. Helium will enter the die cavity through any cracks or pin holes. The devices are removed and placed into the test chamber of a mass spectrometer leak detector. Any helium that entered the package during the previous procedure will be drawn out by the vacuum in the test chamber. The leak rate is measured by the spectrometer. An alternative method with equal or greater sensitivity using Krypton gas may be substituted for this test.

Gross Leak
After the completion of the fine leak test (if applicable), the gross leak test is performed to test for leaks greater than 10^{-3} ATM CC/sec. The devices are placed in a vacuum/pressure chamber at 5 torr for 1 hour. Before breaking the vacuum the units are covered with liquid FC-72. The pressure is then raised to 60 psig for two hours. The devices are removed from the vacuum/pressure vessel and submerged 2 in. in FC-43, heated to 125°C, for 30 seconds and visually checked for bubbles.

These tests evaluate package integrity and detect devices that might fail when exposed to an environment containing moisture or gaseous contaminants.

Pre Burn-In Electrical Test

Devices are tested 100% at 25°C for DC parameters (AC parameters and temperature extremes as required) to detect any electrical anomalies induced by the previous mechanical and thermal stresses. Serialized devices that will be burned-in may have some parameters logged at this point to test for parameter drift after burn-in is completed.

Burn-In

Burn-in is performed for a specified number of hours at 125°C with the device electrically stressed. This procedure eliminates devices with parameters that are marginal or have latent defects. Intermittent shorts caused by pinholes in the passivation will tend to become permanently shorted. Metal that is almost discontinuous due to scratches or cracks will tend to open. Corrosion and contamination on the die will tend to impact the circuit performance and will be detectable during the post burn-in electrical testing.

Post Burn-In Electrical Test

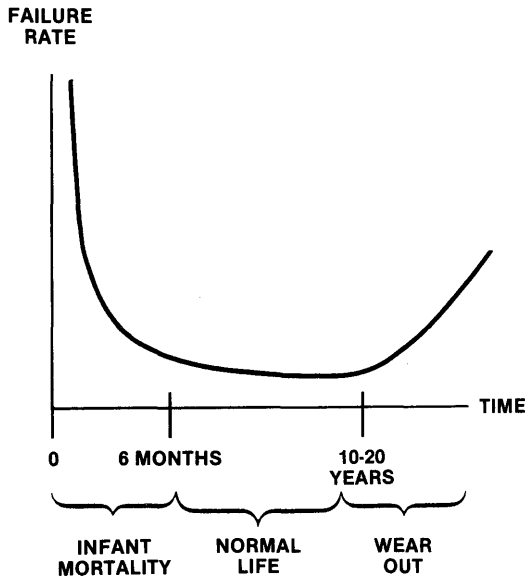
Devices are tested 100% at 25°C for DC parameters (AC parameters and temperature extremes as required) to insure that after all applicable screening the devices perform as specified.

External Visual

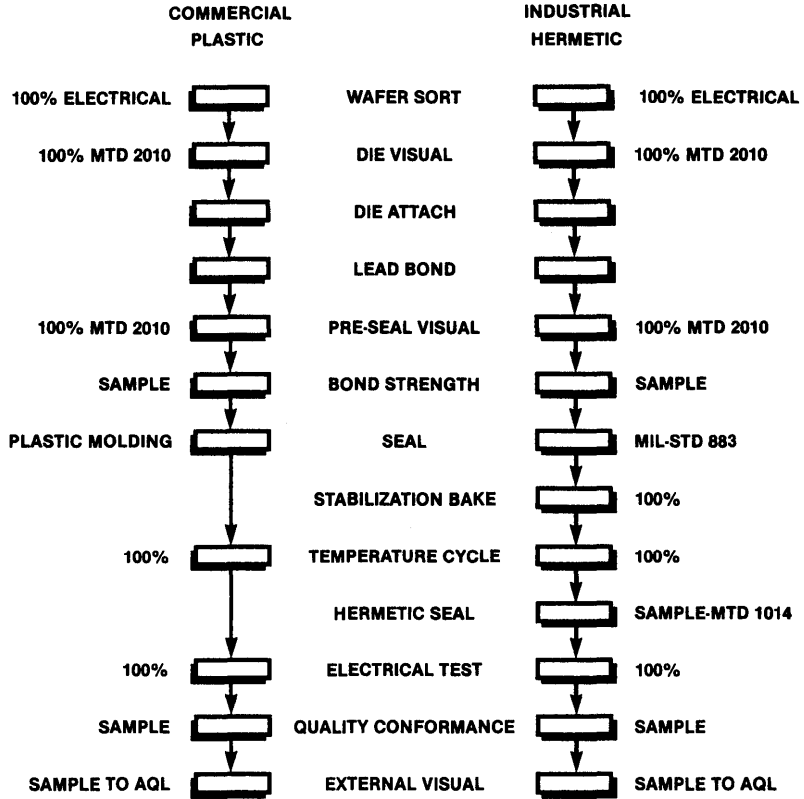
This final optical inspection insures that the packages and leads appear defect free.

Figure 2 summarizes the screening procedure and the failure mechanisms they are designed to detect. Figure 3 Quality Flow Diagrams illustrate the standard processing for SPT's various product grades. Special quality flows can be tailored to specific customer needs.

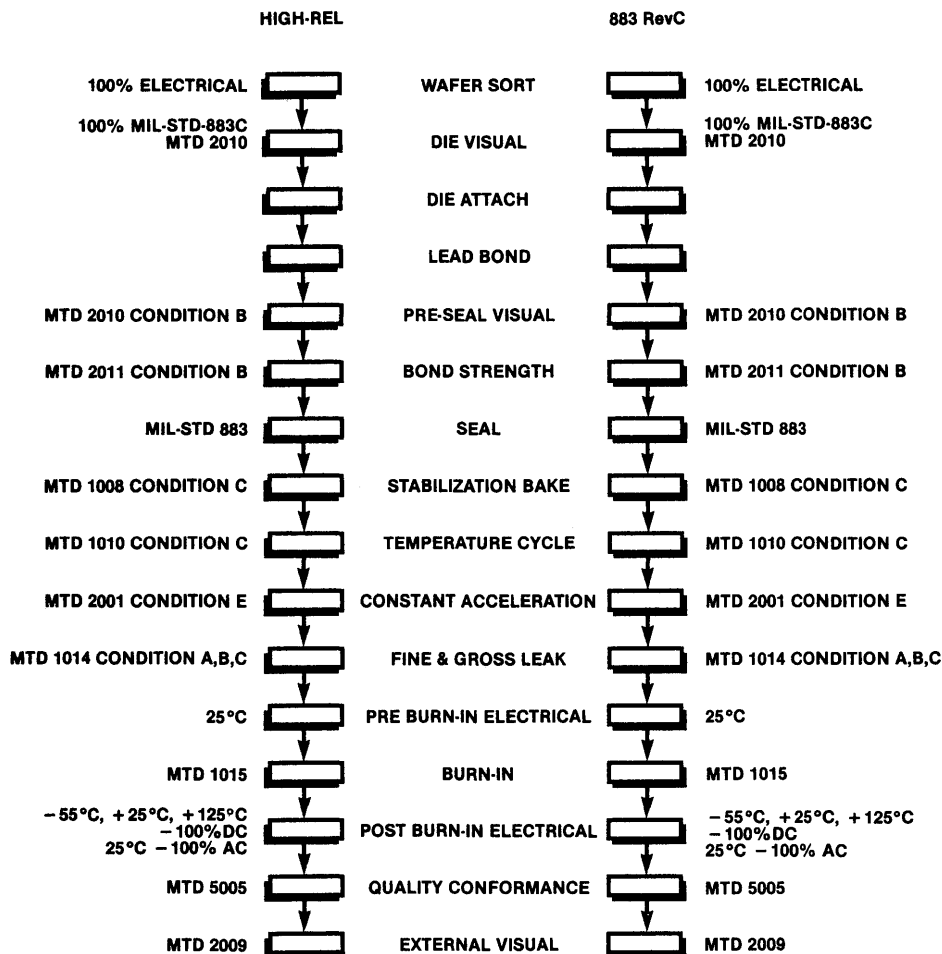
FIGURE 1: "BATHTUB" FAILURE-RATE CURVE



IN-LINE MANUFACTURING FLOW CHART



IN-LINE MANUFACTURING FLOW CHART FOR HERMETIC CAVITY TYPE PACKAGES

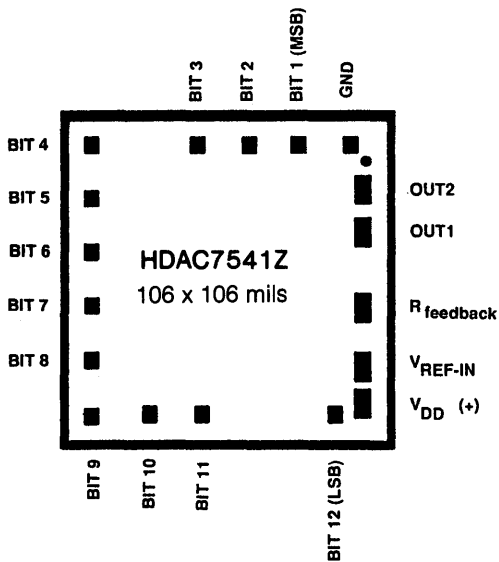
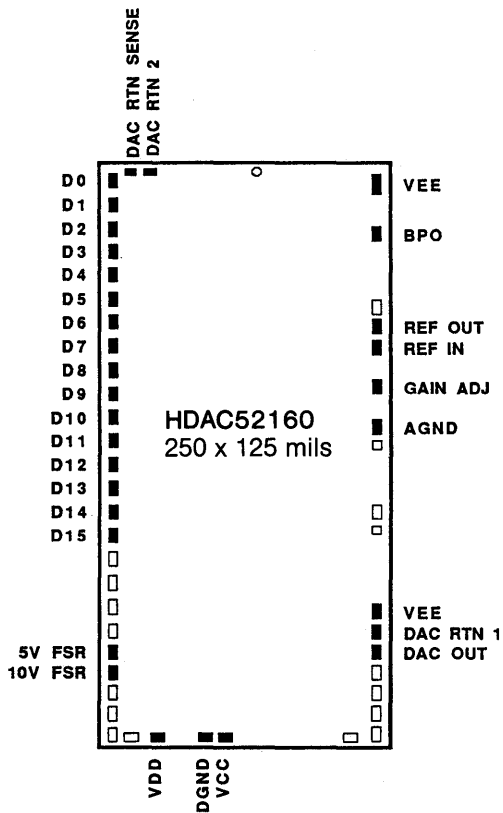
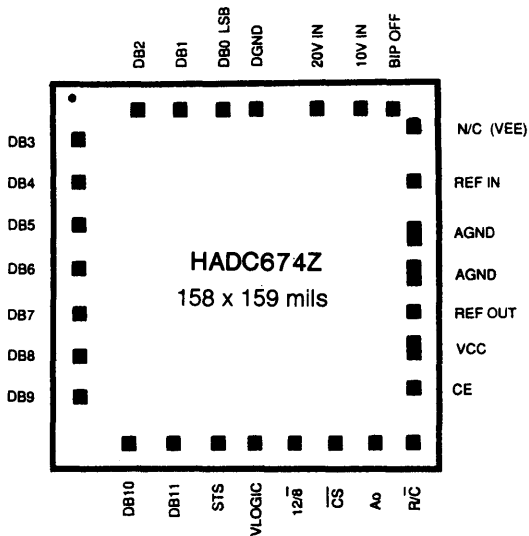
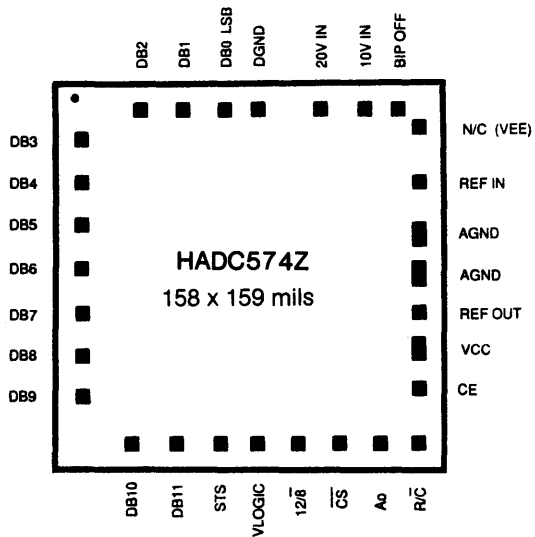


NOTE:
 GROUP A: ELECTRICAL CHARACTERISTICS
 GROUP B: PACKAGE ORIENTED TESTS
 GROUP C: LIFE TESTS — PERIODIC CONFORMANCE
 GROUP D: ENVIRONMENTAL TESTS — PERIODIC CONFORMANCE

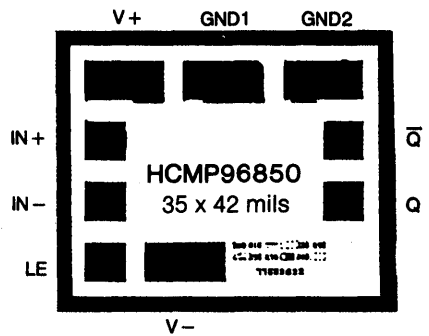
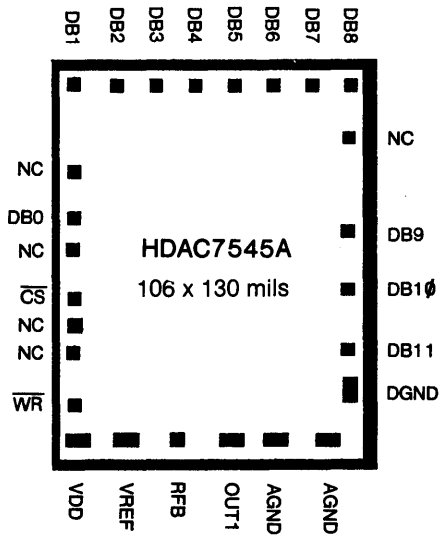
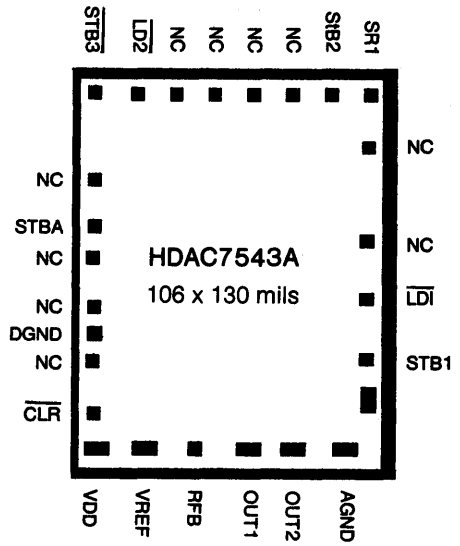
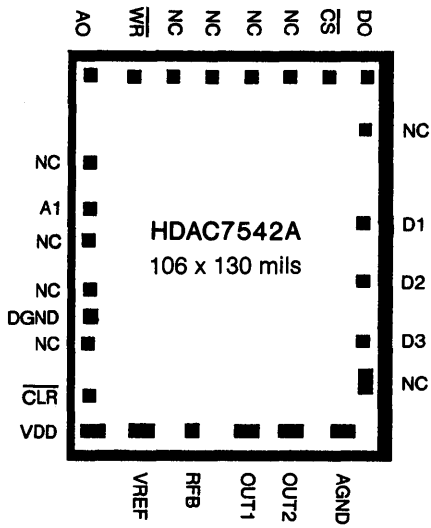
FIGURE 2: FAILURE DETECTION SUMMARY

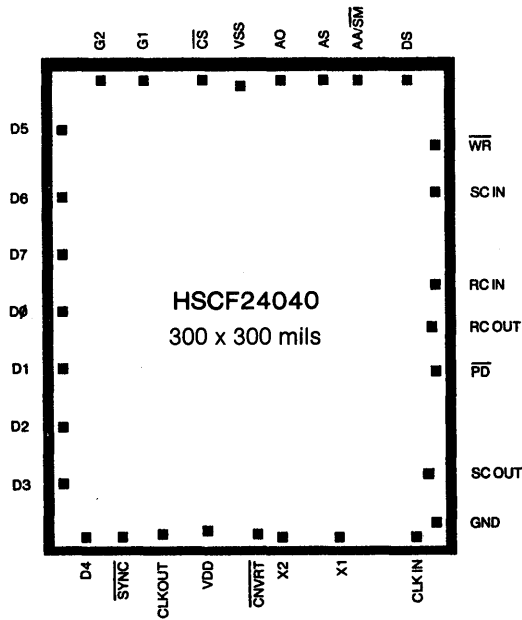
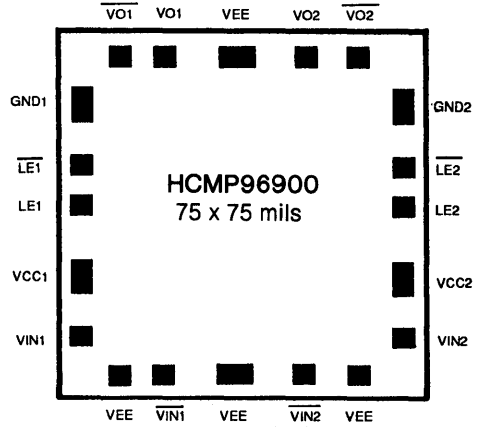
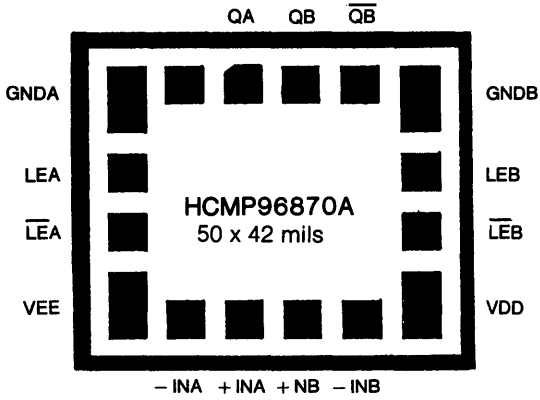
Procedure	FAILURE MECHANISM DETECTED											
	wire bonds	die bonds	loose particles	process related	surface contamination	passivation failure	defective metalization	defective package	package seal	thermal stress	package leads	electrical failure
Pre-seal Visual	✓	✓	✓	✓			✓	✓				
Bond Strength	✓											
Stabilization Bake	✓	✓		✓	✓							
Temperature Cycle	✓	✓			✓			✓	✓	✓		
Constant Acceleration	✓	✓						✓				
Leak Test								✓	✓			
Pre Burn-In Electrical												✓
Burn-In					✓	✓	✓	✓				✓
Post Burn-In Electrical												✓
External Visual								✓			✓	

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11



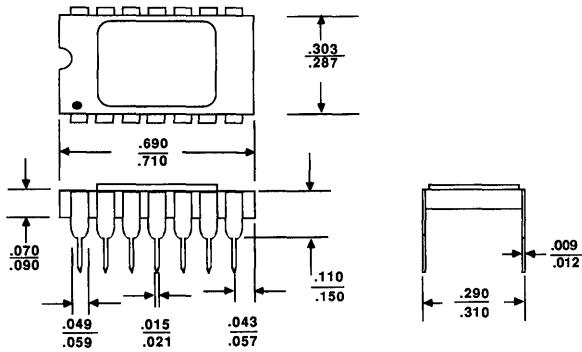
10



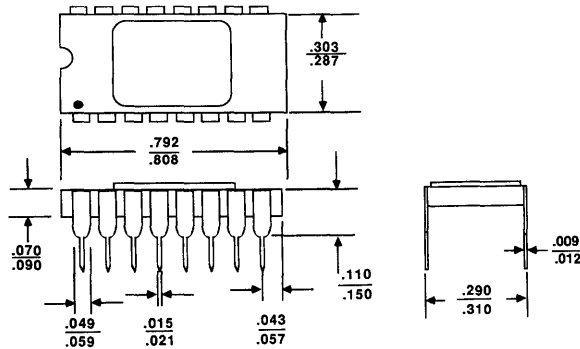


NOTES:

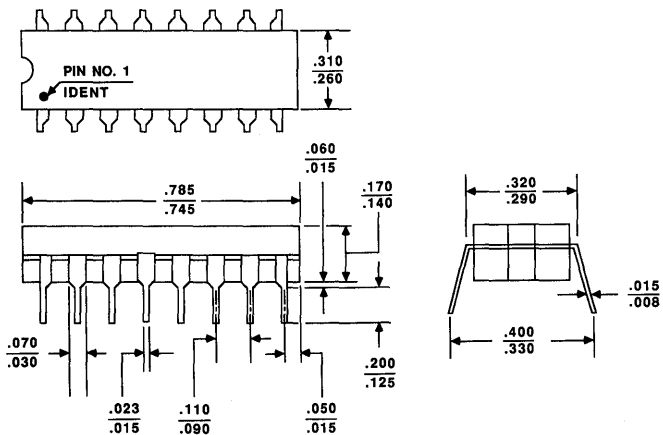
14 LEAD SIDBRAZED



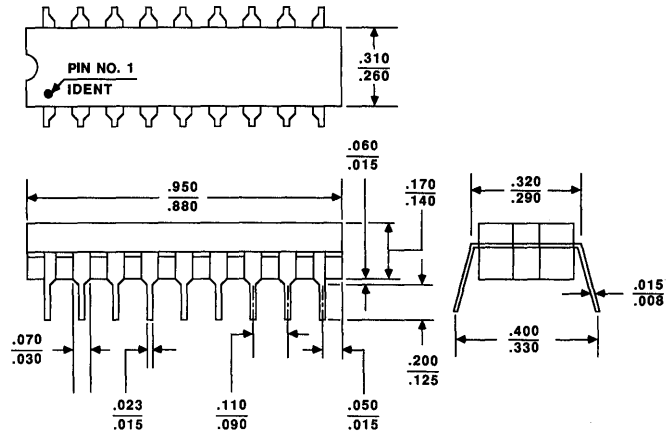
16 LEAD SIDEBRAZED



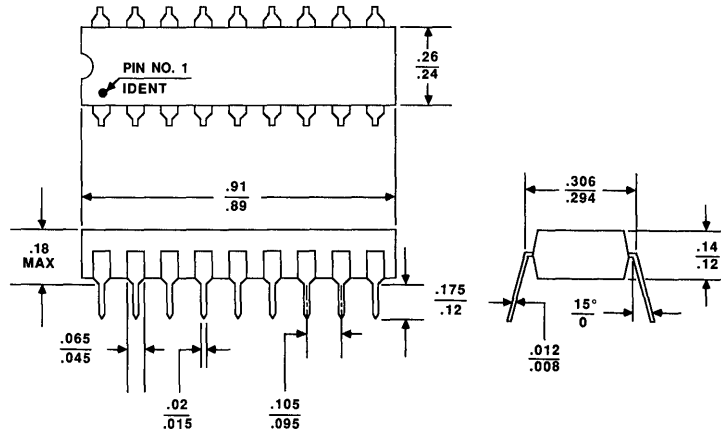
16 LEAD CERDIP



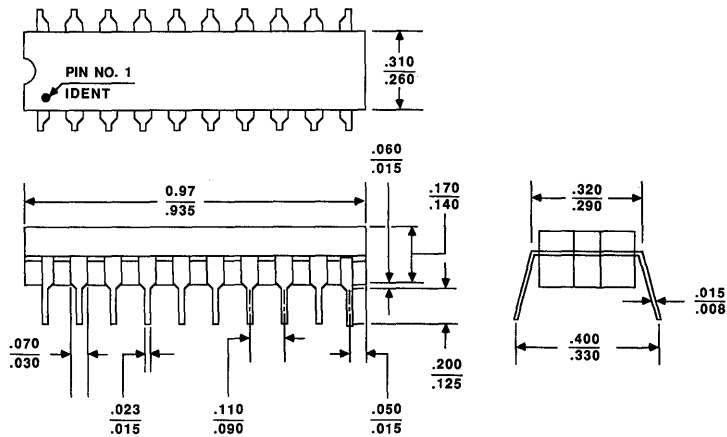
18 LEAD CERDIP



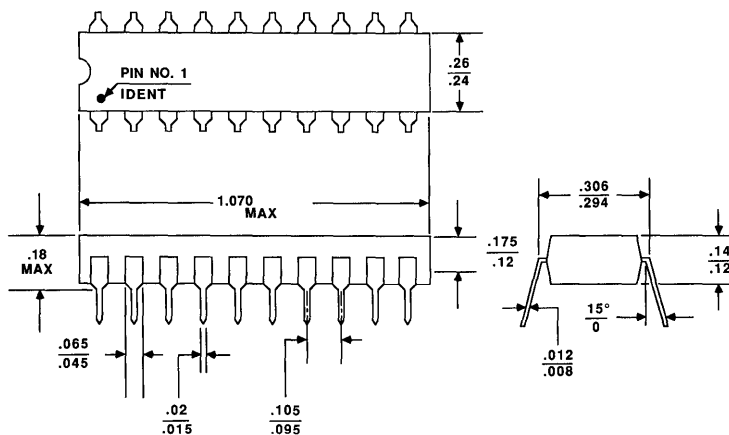
18 LEAD PLASTIC



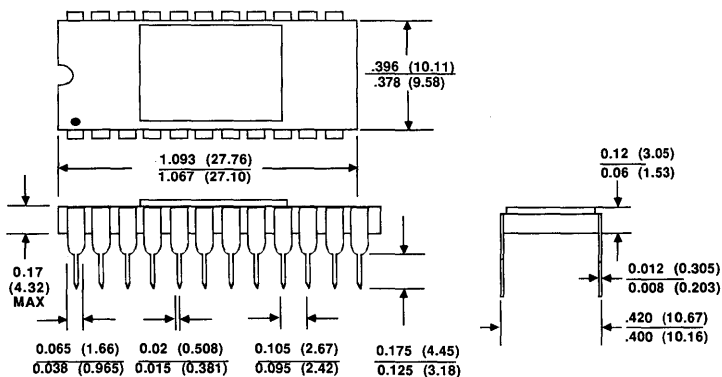
20 LEAD CERDIP



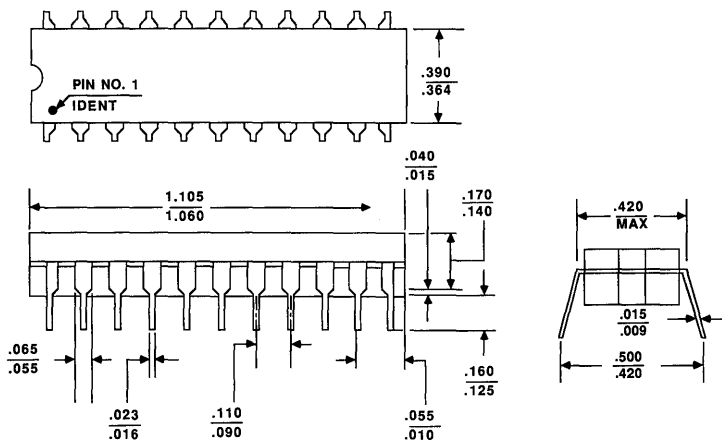
20 LEAD PLASTIC



22 LEAD SIDEBRAZED

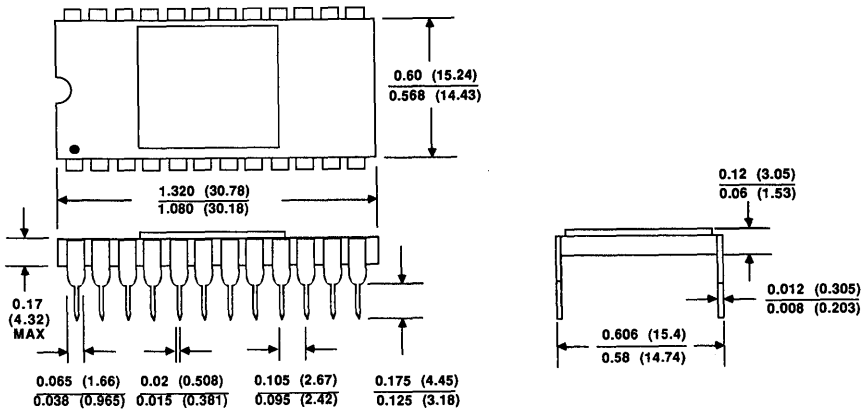


22 LEAD CerdIP

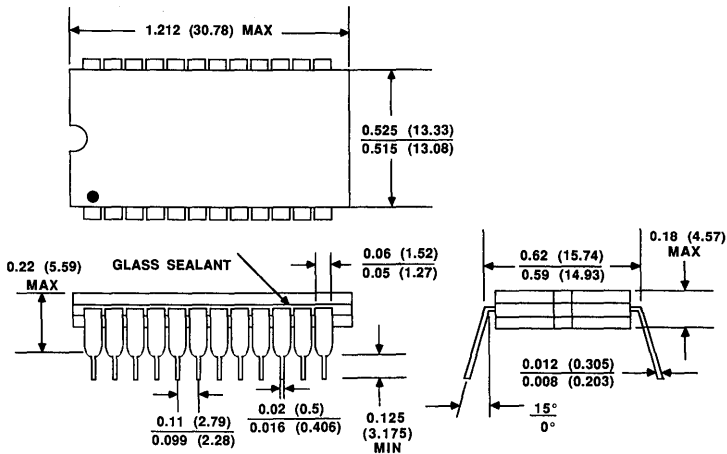


10

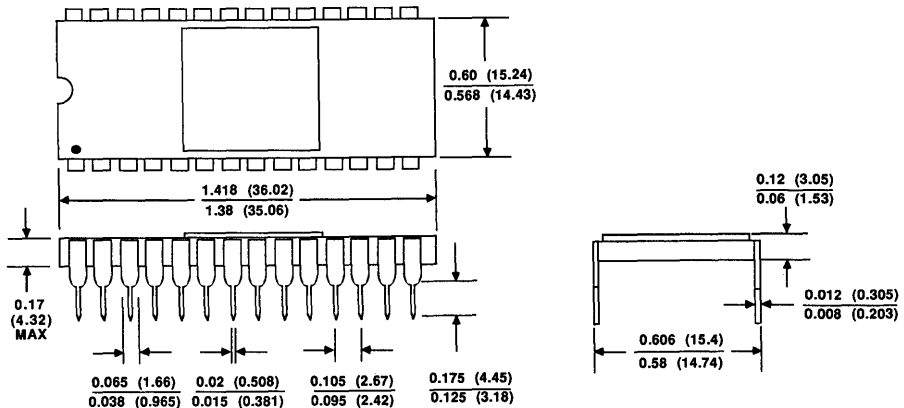
24 LEAD SIDEBRAZED



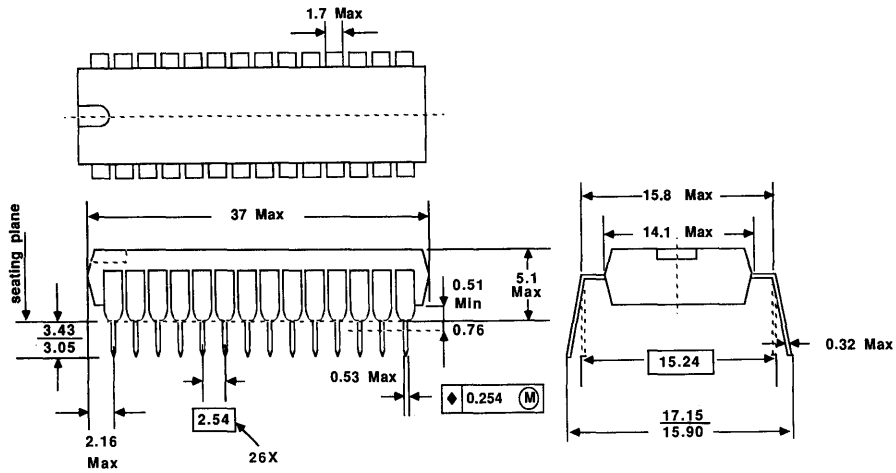
24 LEAD Cerdip



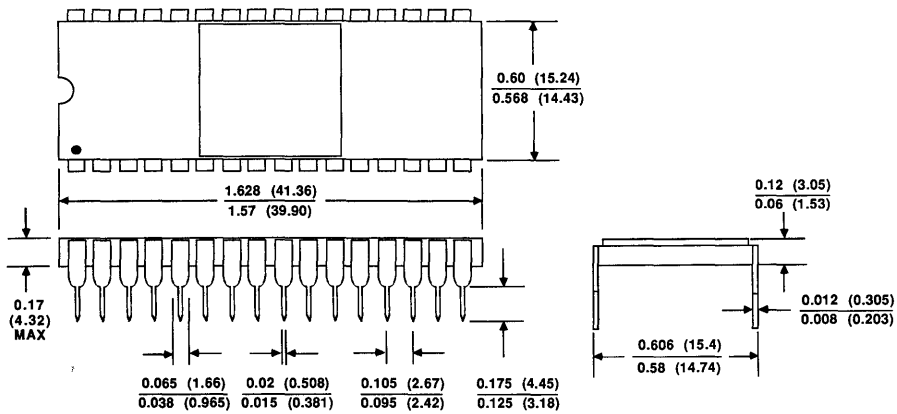
28 LEAD SIDEBRAZED



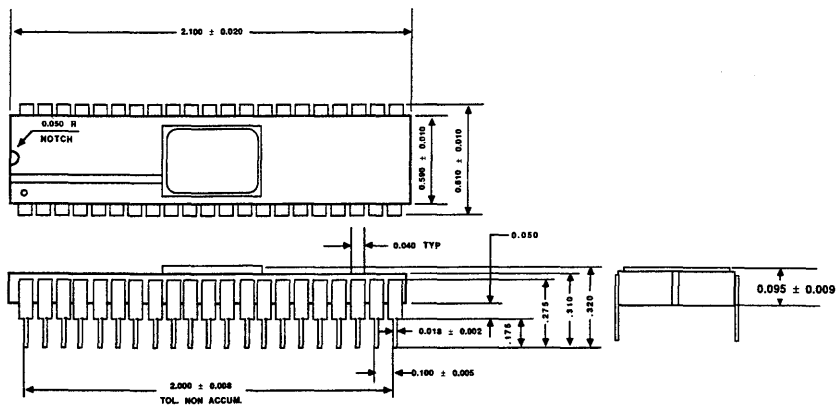
28-LEAD PLASTIC



32 LEAD SIDEBRAZED

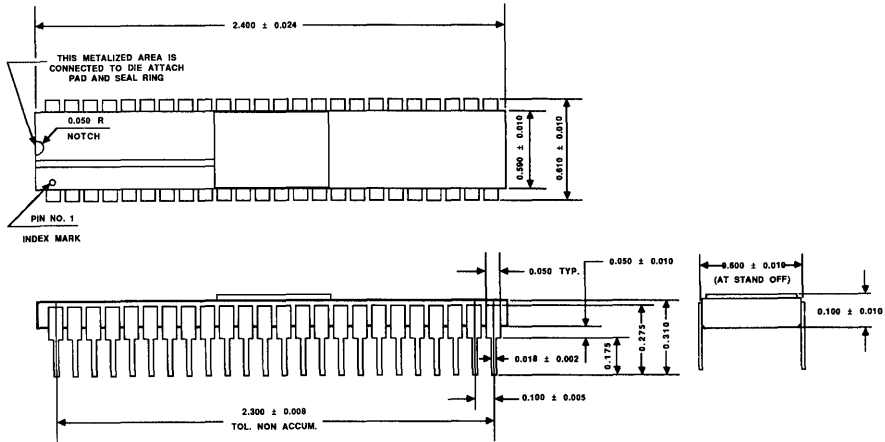


42 LEAD SIDEBRAZED

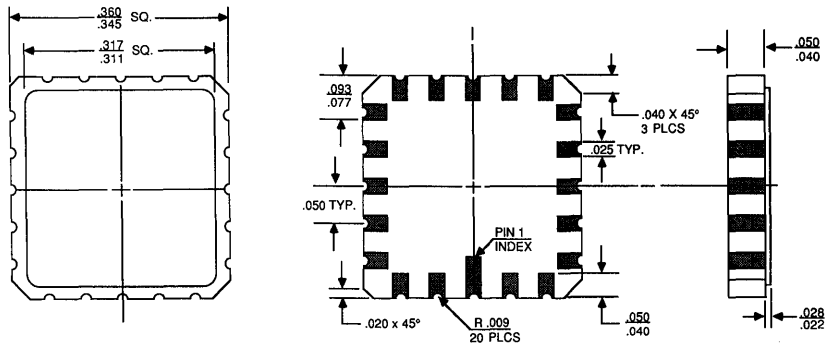


10

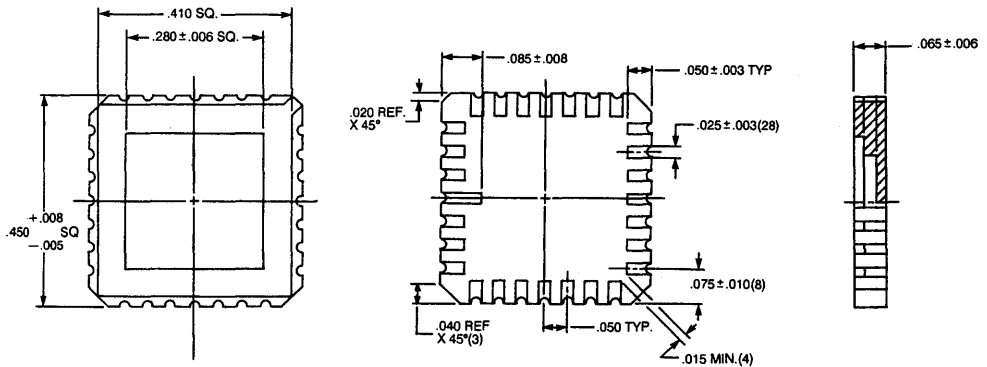
48 LEAD SIDEBRAZED



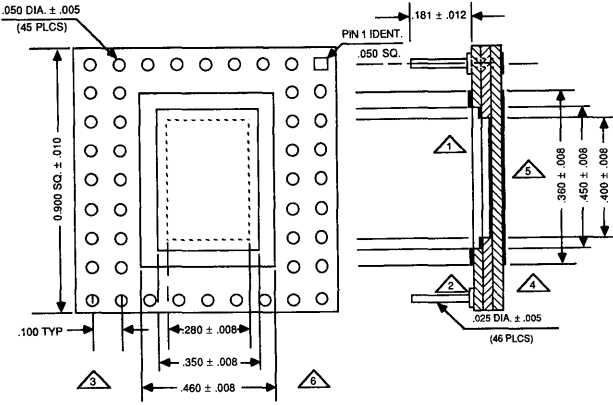
20 PIN LCC



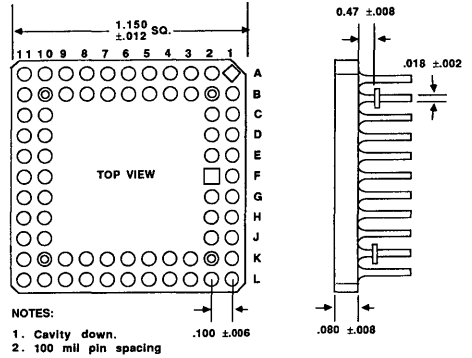
28 PIN LCC



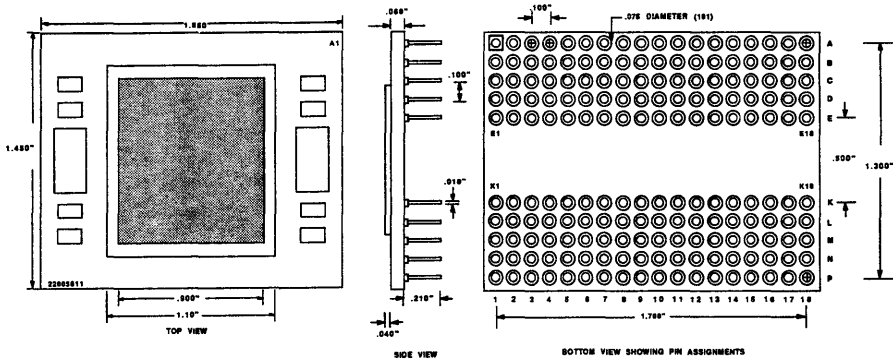
48 PIN PGA



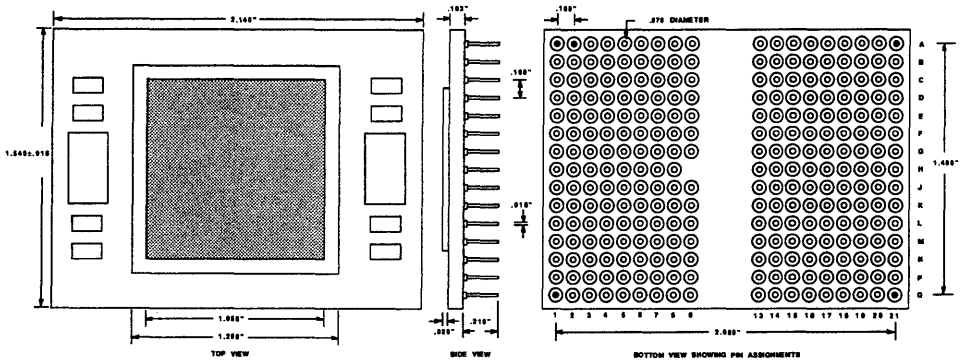
72 PIN PGA



180 PIN PGA



269 PIN PGA



**For Ordering Information See Section 1.

NOTES:

SELECTION GUIDE, CROSS REFERENCE ORDERING INFORMATION	1
ANALOG TO DIGITAL CONVERTERS	2
DIGITAL TO ANALOG CONVERTERS	3
COMPARATORS	4
FILTERS	5
DIGITAL SIGNAL PROCESSING	6
EVALUATION BOARDS	7
APPLICATIONS INFORMATION	8
QUALITY ASSURANCE	9
PACKAGE OUTLINES	10
SALES OFFICES AND REPRESENTATIVES	11

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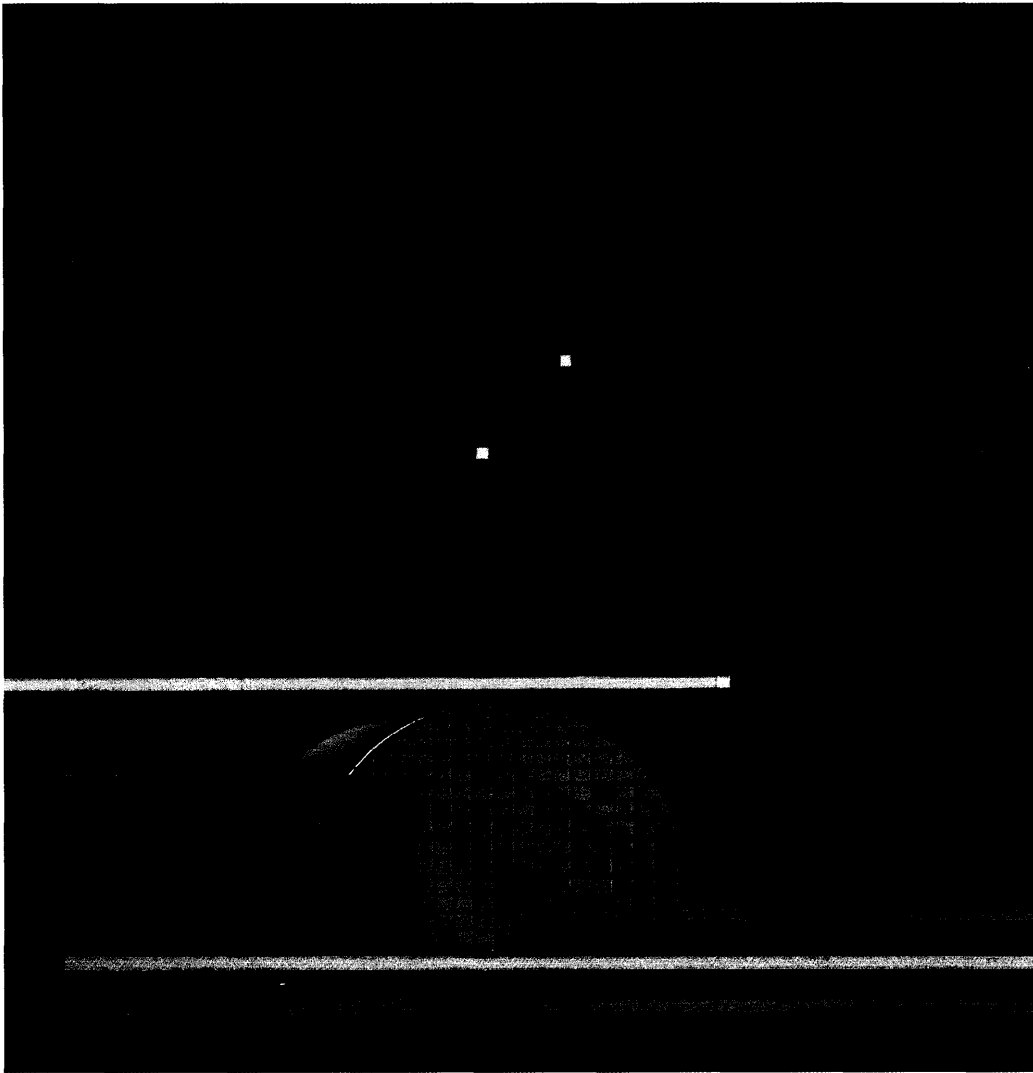
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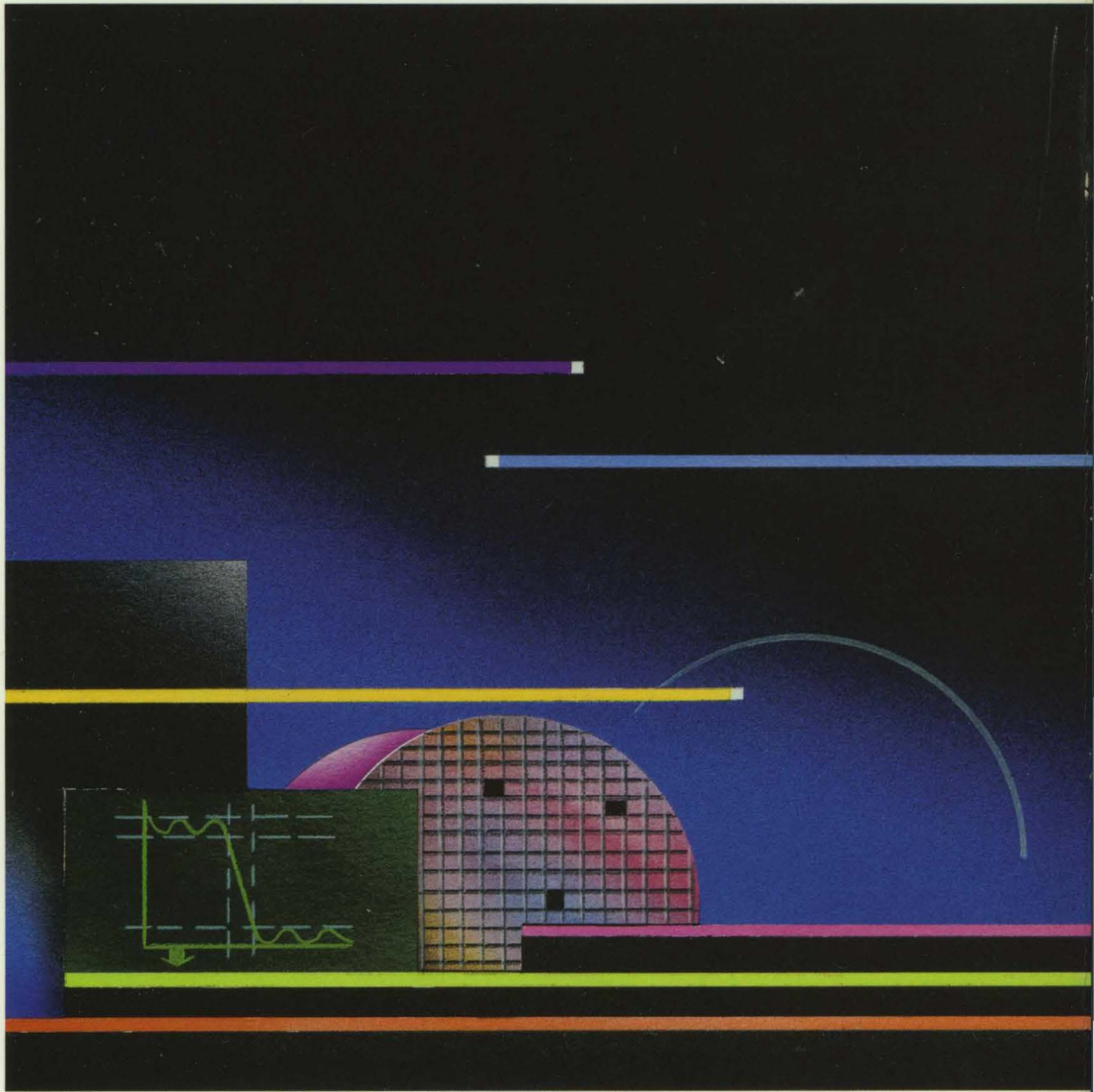
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