

*TMS320 DSP
DESIGNER'S NOTEBOOK*

Avoiding False Interrupts on the TMS320C3x

APPLICATION BRIEF: SPRA198

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Avoiding False Interrupts on the TMS320C3x



Abstract

TMS320C30 interrupts are internally latched. If the interrupt is held low for three or more cycles, multiple interrupts may occur. This document describes an external circuit that can fix this problem. Logic diagrams and a schematic are presented.



Design Problem

TMS320C30 interrupts are internally latched on the falling edge of H1 (see pp. 6-20 and 13-38 of the TMS320C3x User's Guide). If the interrupt is held low for three or more H1 cycles, multiple interrupts may occur.

Solution

The solution is to add a PAL, clocked by H1, which intercepts the interrupt. This logic will hold the interrupt ($\overline{INTx'}$) low for two H1 cycles. The external interrupt (\overline{INTx}) may be held low longer or shorter, but must go high before the interrupt can be reasserted. For four external interrupts, the same logic may be repeated in the same PAL.

Figure 1. State diagram

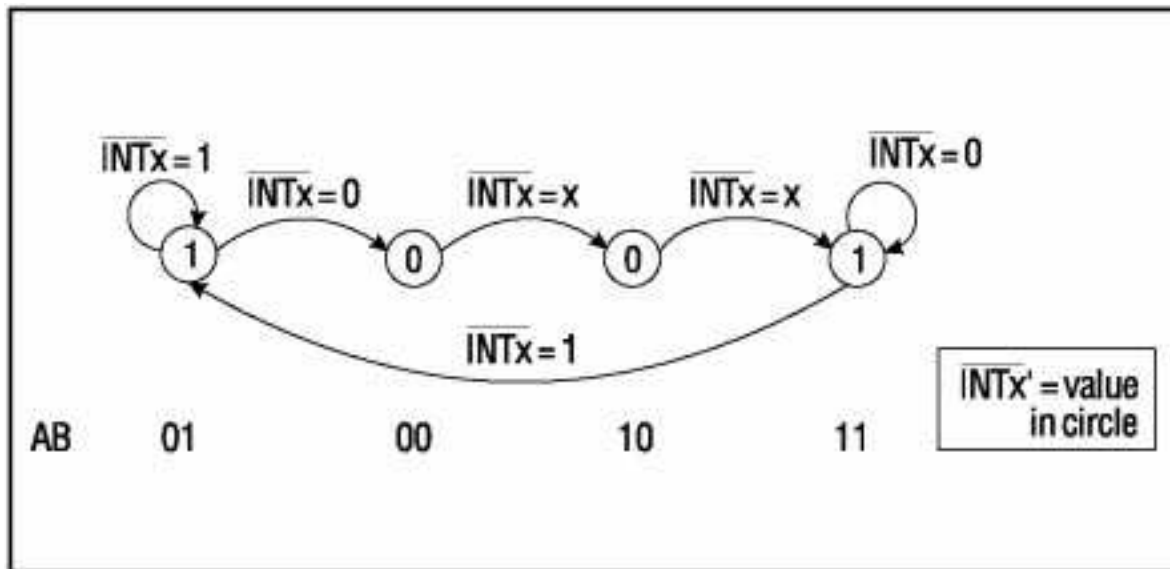


Figure 2. Karnaugh map

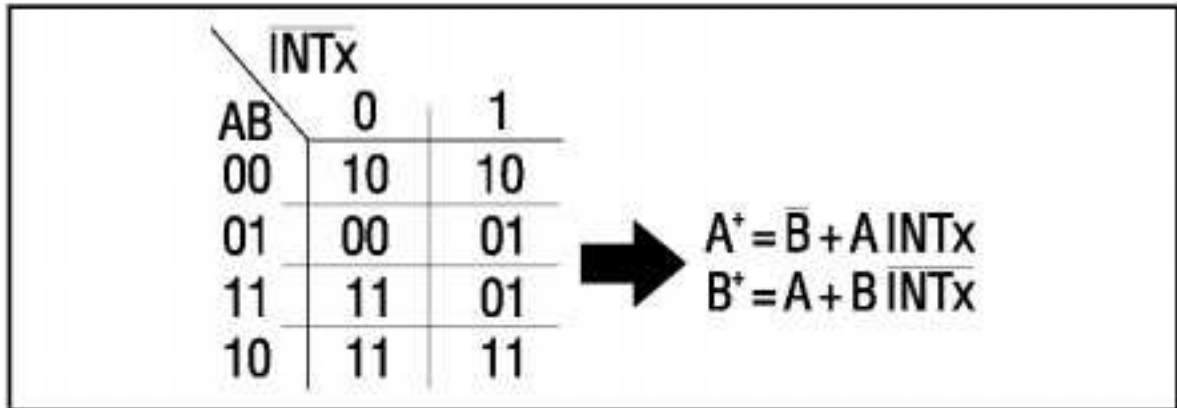


Figure 3. Logic diagram

